

Chapter 2

MODELING AND CONTROL OF PEBB BASED SYSTEMS

2.1 Introduction

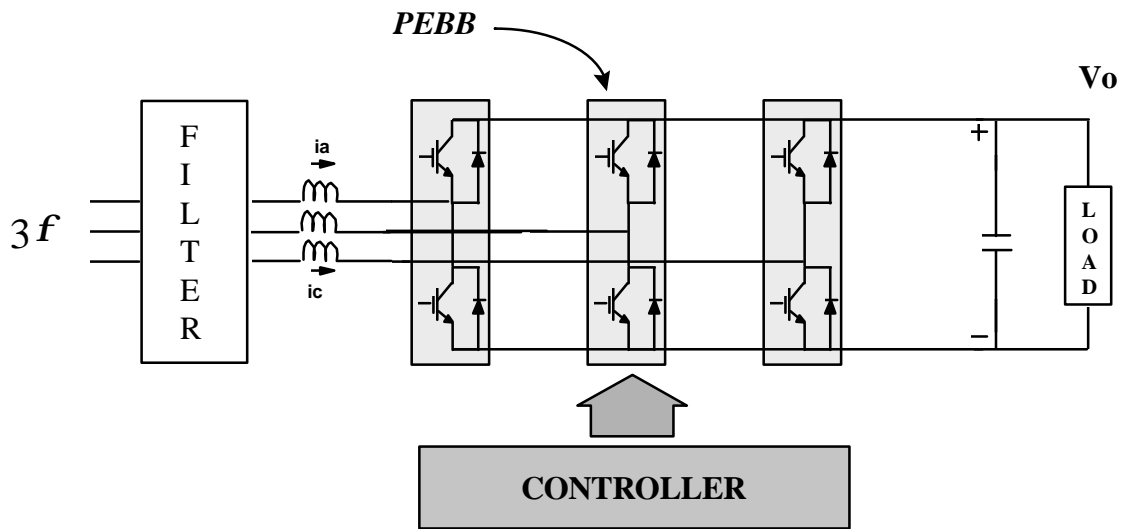
The PEBBs are fundamental building cells, integrating state-of-the-art techniques for large scale power electronics systems. Conventional power electronics systems lack high degree of integration and standardization. PEBBs help to standardize and simplify the design process. Instead of working with components, designers work at block level and this greatly reduces the design effort.

This chapter will discuss the modeling and control of systems built using modular PEBBs. Compared to the conventional systems, a PEBB based system offers advantages like system reconfiguration, hierarchical control and control intelligence. To demonstrate these ideas, a PEBB based Boost Rectifier and a Four Leg Inverter system is analyzed in this chapter. Section 2.2 discusses the three level modeling approach adopted, which is applicable for analyzing all PEBB based systems.

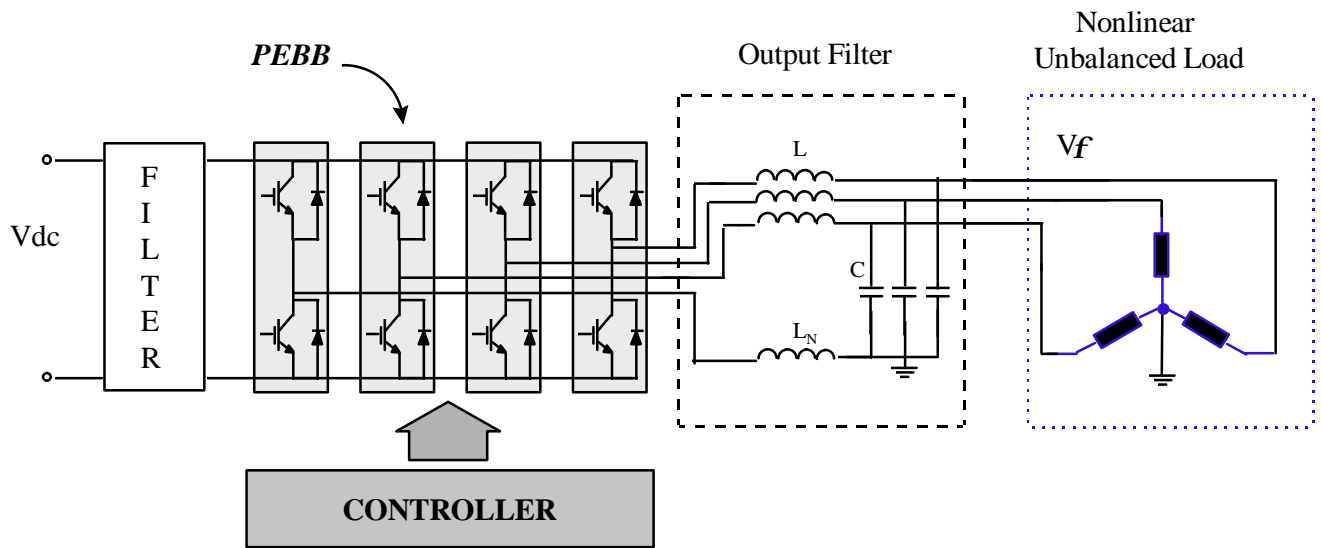
The PEBB switching cell has been identified in the previous section. Figure 2.1(a) shows three PEBB switching cells configured to form a Boost Rectifier. The Boost Rectifier converts three phase input voltage to regulated DC link voltage. Section 2.3 describes the modeling and control of the Boost Rectifier.

Figure 2.1(b) shows a three phase Four Leg Inverter composed of four PEBB switching cells. Section 2.4 describes the modeling and control of the four leg inverter. The Four Leg Inverter converts DC link voltage to provide utility power. As compared to a conventional three phase inverter, it can provide balanced three phase output voltage even in presence of unbalanced and non-linear load [7].

Each of these PEBB based converter is designed for stability and good transient performance. The PEBB based systems employ digital controllers like Digital Signal Processors (DSP) and the feedback control loop is implemented digitally using the DSP. As compared to analog controllers, digital controllers allows flexibility in system operation and system configuration. It is described in detail in later sections.



(a) Front End Boost Rectifier



(b) Three Phase Four Leg Inverter

Figure 2.1 PEBB based Boost Rectifier and Inverter system

2.2 Modeling Approach

The PEBB-based converters are modeled and simulated using SABER. A three level modeling approach is employed and three models were developed in SABER namely, Discrete Switching model, Average Large Signal model and the Small Signal model.

In the Discrete model, the power stage of the converter is modeled using ideal switches. The DSP based digital controller is modeled using MAST, a Hardware Description Language available in SABER. The Discrete model using ideal switches gives descriptive information regarding system behavior such as voltage and current switching ripple. This information is useful in the design and analysis of input EMI filter for Rectifier and VSI. Its main drawback is long simulation time and also it does not give any insight to controller design.

The Average Large Signal model is derived from the switching model using time averaging equivalent circuit approach [8]. It results in a time-invariant model which is valid at frequencies much lower than the switching frequency. Process of averaging removes the switching action of the switches in the power stage. It can be used to predict the system performance with greatly reduced simulation time. The average model in the stationary co-ordinates is transformed to obtain average model in rotating co-ordinates. This results in system variables which are DC quantities. The Average Large Signal model is perturbed and linearized around an operating point to get the Small Signal model. Based on the derived Small Signal Model, control loop design guidelines are obtained.

2.3 Modeling and Control of Front End Boost Rectifier

The three phase Boost Rectifier, as shown in Figure 2.1(a), is an attractive topology for use as a front-end power processing unit at higher power levels. It converts three phase input voltage to regulated DC link voltage. Also, it provides unity Power Factor and draws continuous input currents [5],[6]. As shown in Figure 1.2, the three phase Boost Rectifier is used in the shipboard DC DPS to provide regulated DC link voltage.

In this section, the modeling and control of PEBB based rectifier is described. An analog controller based Boost Rectifier switching model has been discussed in the literature [9]. A DSP processor based Boost Rectifier switching model is presented in this section. Also, the fault tolerance capability of a PEBB based Boost Rectifier is studied.

2.3.1 Principle of Operation

Figure 2.2 shows the three phase Boost Rectifier composed of PEBBs. Three PEBB cells with integrated gate drives are configured to form the Boost Rectifier power stage. A DSP based local controller supplies gate drive commands through a DSP interface board. The feedback control loop is implemented digitally using the DSP. The PEBB system also includes a sensor board which senses the DC link voltage, AC voltage and current and provides feedback to the local controller. The system level control in the PEBB based power

distribution is hierarchical. The local-controller has communication ports to communicate with the zonal-level controller or the host computer. The local controller is field programmable to implement the desired control strategy.

Figure 2.3 shows the Discrete switching model of the DSP controlled boost rectifier simulated using SABER. For the DC DPS application, this model serves as an important tool to observe the effect of switching ripple on the DC link and also helps in the design of input EMI filter.

The PEBB cells are modeled as ideal switches with anti-parallel diodes. The rectifier has an inner current controller in rotating co-ordinates and an outer voltage loop. The DC link voltage is sensed and compared to the voltage reference. The error voltage is passed through a compensator to generate I_{dref} (I_d current reference), as the d-channel is responsible for the power transfer. The d-q co-ordinates axis are aligned with respect to the input line voltages such that $V_q=0$. As a result, the q channel current reference, I_{qref} is set to zero in order to achieve unity power factor [5].

The input line currents are sensed and converted from stationary co-ordinates to rotating co-ordinates to generate I_d and I_q . The transformation T, from stationary to rotating co-ordinates is explained in Appendix C. The inner current controller has compensators, H_{id} and H_{iq} in d and q channels. The output of the current controller are the switch duty cycles d_d and d_q . These duty cycles, d_d and d_q are transformed from rotating to stationary co-ordinates to generate d_a and d_b . Space Vector Modulation (SVM), as explained in Appendix B is used in distributing the duty cycles [17].

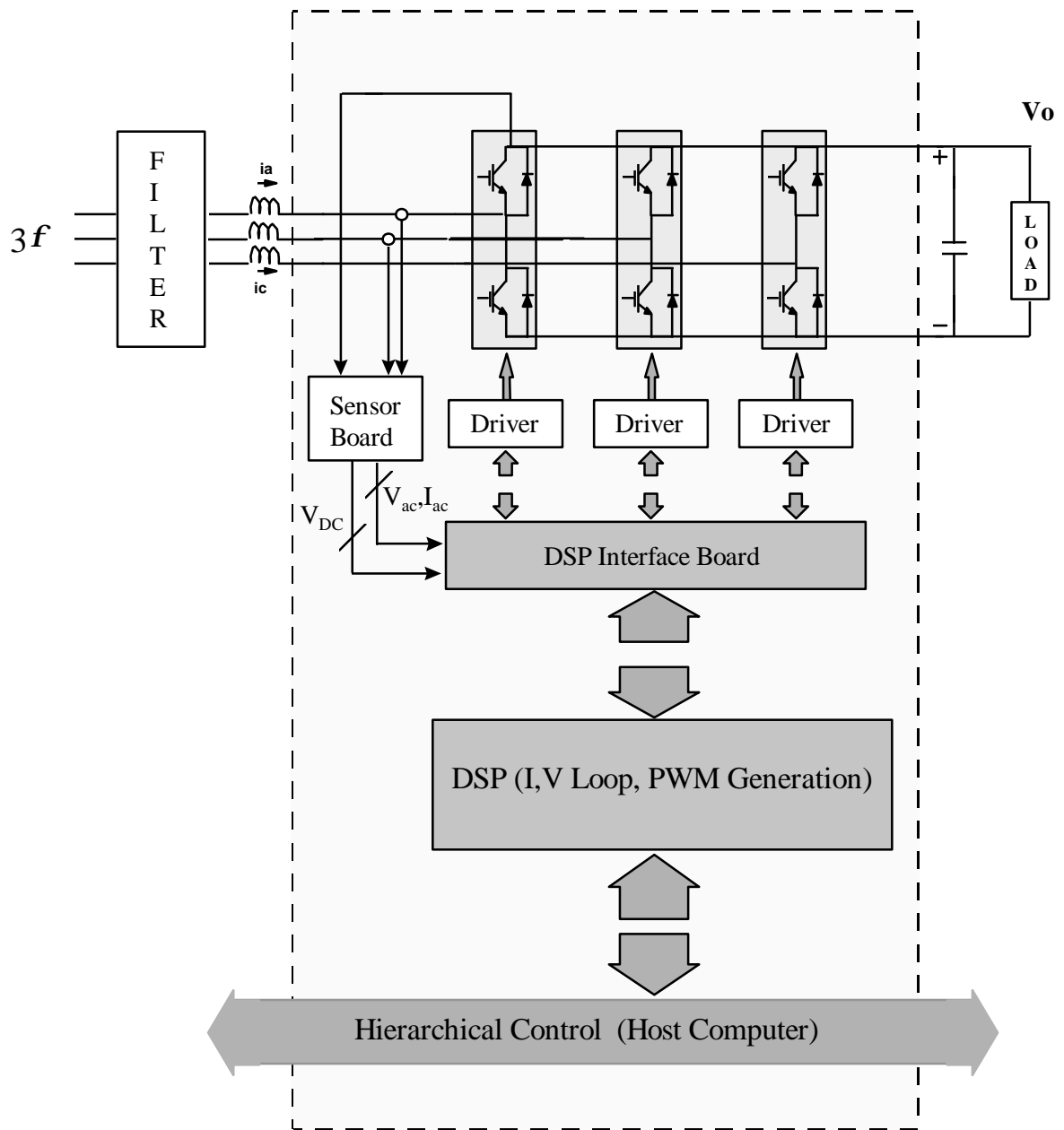


Figure 2.2 : PEBB based Three Phase Boost Rectifier : *Three PEBB cells with integrated gate drives are configured to form the Boost rectifier. The DSP based local controller communicates with the host computer.*

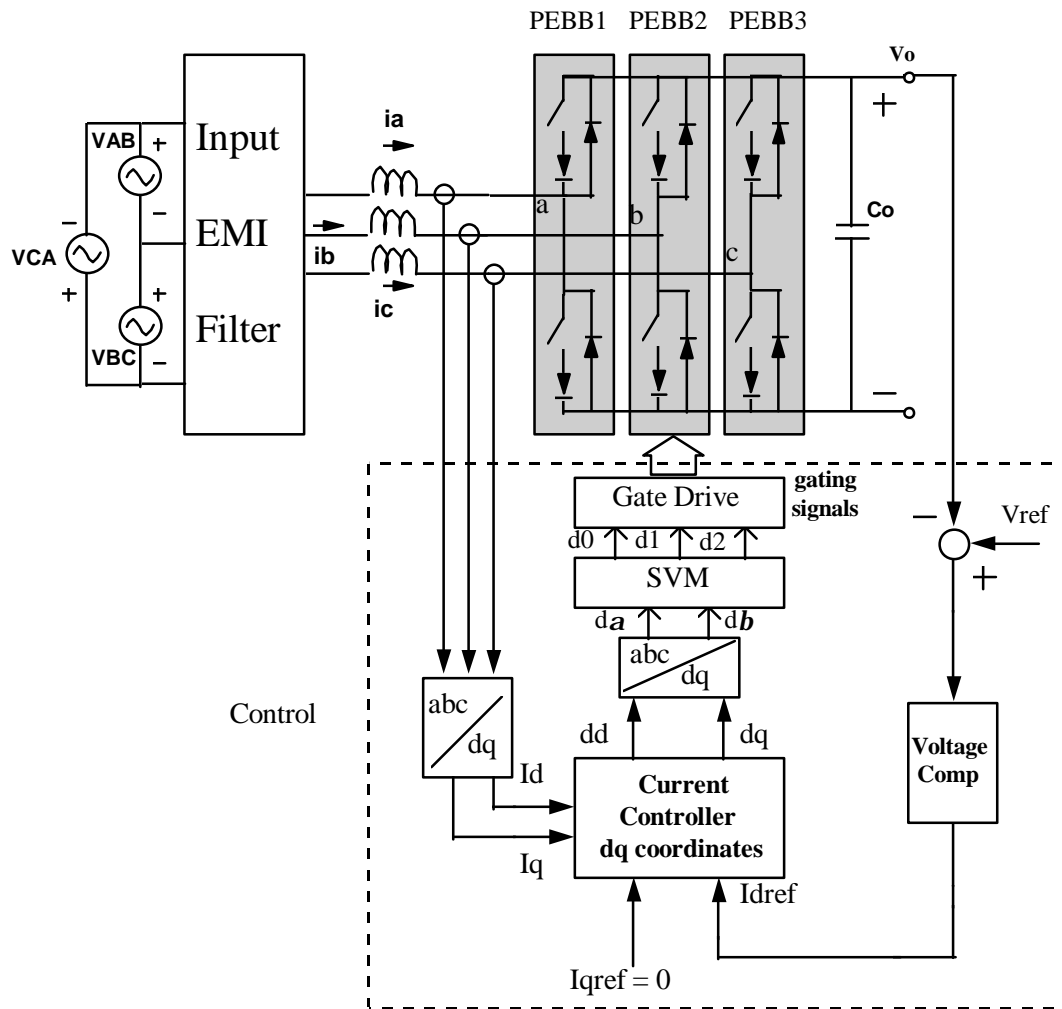


Figure 2.3 : Discrete Switching Model of the Boost Rectifier : *It provides time domain information. The boost inductor currents and the DC link voltage are sensed and fed to the compensator. The controller is shown in the dotted box.*

2.3.2 Power Stage Modeling

The Average Large Signal model of the boost rectifier is derived using time averaging equivalent circuit approach [6]. It results in a time-invariant model which is valid at frequencies much lower than the switching frequency. Figure 2.4 shows the Average Large Signal Model. Six switches in the power stage are replaced with three controlled voltage sources and a controlled current source. The output stage of the power converter remains the same.

The controlled voltage and current sources in the Average model are represented as :

$$\begin{bmatrix} V_{ab} \\ V_{bc} \\ V_{ca} \end{bmatrix} = \begin{bmatrix} d_{ab} \\ d_{bc} \\ d_{ca} \end{bmatrix} V_0 \quad \text{and,} \quad I_p = \begin{bmatrix} d_{ab} & d_{bc} & d_{ca} \end{bmatrix} \begin{bmatrix} I_{ab} \\ I_{bc} \\ I_{ca} \end{bmatrix}$$

Where $d_{ab}=(d_a-d_b)$, $d_{bc}=(d_b-d_c)$, $d_{ca}=(d_c-d_a)$ are the control duty cycles

And, d_i (i=a,b,c) are duty cycle of the upper switch in i^{th} leg.

Also, $I_{ab}=(I_a-I_b)/3$, $I_{bc}=(I_b-I_c)/3$, $I_{ca}=(I_c-I_a)/3$

Where,

I_a, I_b, I_c are the input phase currents

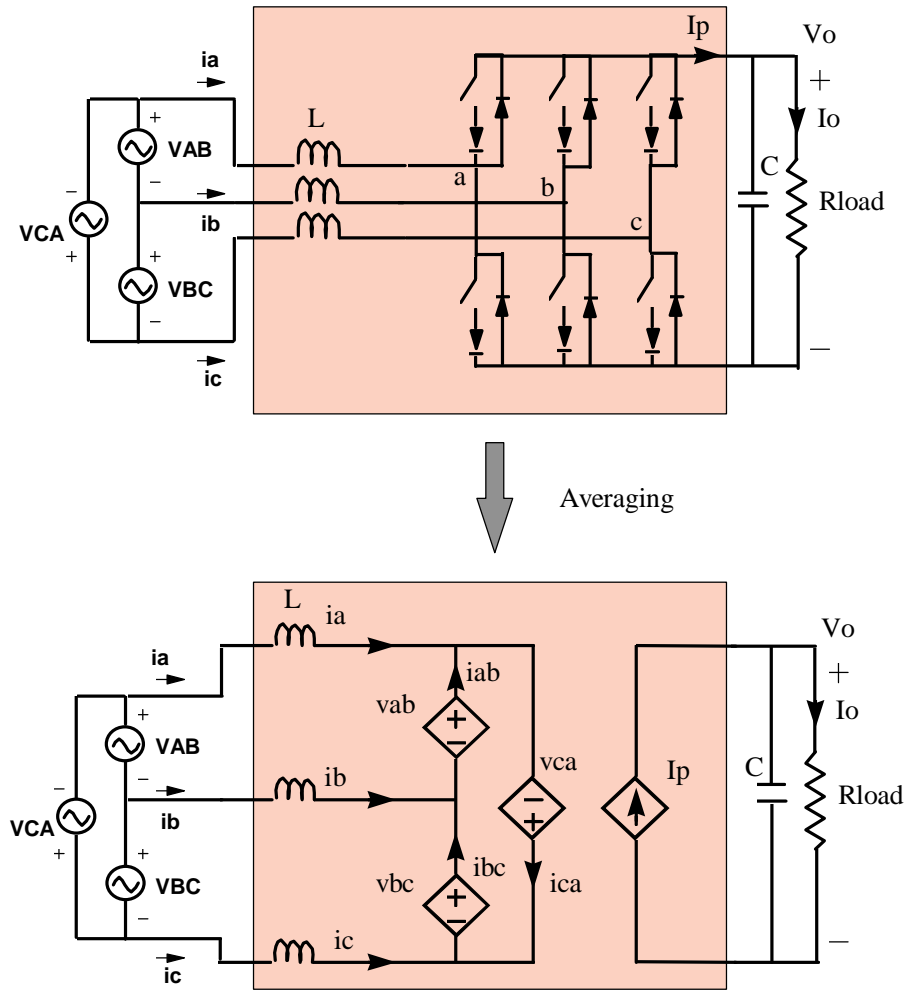


Figure 2.4 : Average Large Signal Model in Stationary Co-ordinates : *The process of averaging replaces the switches with controlled voltage and current sources.*

The complete model in stationary co-ordinates is given by :

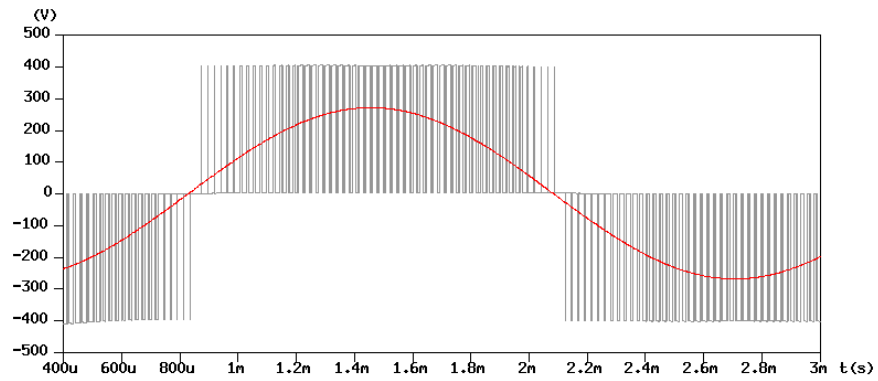
$$\frac{d}{dt} \begin{bmatrix} I_{ab} \\ I_{bc} \\ I_{ca} \end{bmatrix} = \frac{1}{3L} \begin{bmatrix} V_{AB} \\ V_{BC} \\ V_{CA} \end{bmatrix} - \frac{1}{3L} \begin{bmatrix} d_{ab} \\ d_{bc} \\ d_{ca} \end{bmatrix} V_0$$

$$\frac{d}{dt} V_0 = \frac{1}{C} \begin{bmatrix} d_{ab} & d_{bc} & d_{ca} \end{bmatrix} \begin{bmatrix} I_{ab} \\ I_{bc} \\ I_{ca} \end{bmatrix} - I_0$$

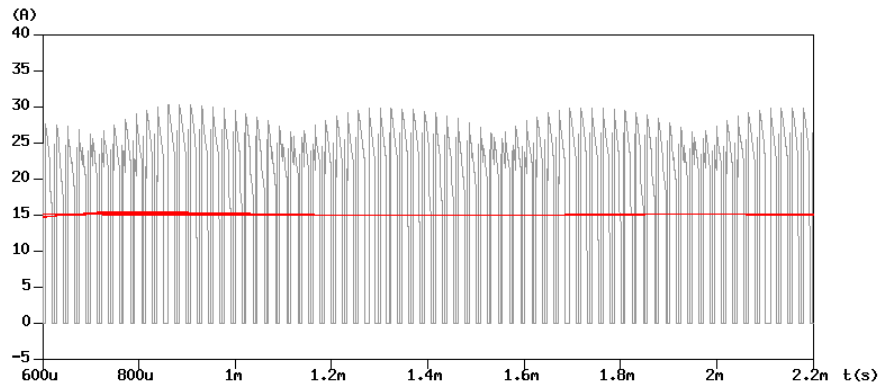
The rectifier draws sinusoidal input current and maintains unity power factor. Thus, it is evident from Figure 2.4 that the controlled voltage sources V_{ab} , V_{bc} , V_{ca} must be sinusoidal in the average sense. Since V_0 is a constant, this further implies that the desired control duty cycles d_{ab} , d_{bc} , d_{ca} must be sinusoidal.

Figure 2.5(a) gives the line-line voltage V_{ca} in switching model and average model. V_{ca} is pulse width modulated in the switching model and is a sinusoid in the average sense. Figure 2.5(b) gives the output DC rail current in the two models. The average model gets rid of the switching ripple and yields the average value of voltage and currents. These values can be controlled to get the desired output.

As the steady state duty cycle in the Average Model are sinusoids, conventional feedback control techniques cannot be used. Therefore, the transformation T, as explained in Appendix C is applied to the Average Model to produce an Average Model in rotating



(a) Line-Line voltage V_{ca}



(b) Output DC rail current

Figure 2.5 : Waveforms in switching and average models : *The average model gets rid of the switching ripple and yields the average value of the waveforms.*

co-ordinates. Figure 2.6 gives the power stage expressed in d-q co-ordinates. The desired steady state duty cycles are DC quantities and this makes it easier to design feedback controllers. It is explained in detail in section 2.3.3.

The Boost Rectifier is represented in rotating co-ordinates as :

$$V_d = 3L \frac{di_d}{dt} - d_d V_o + 3\omega L i_q$$

$$V_q = 3L \frac{di_q}{dt} - d_q V_o - 3\omega L i_d$$

$$\frac{3}{2}(d_d i_d + d_q i_q) = C \frac{dV_o}{dt} - I_o$$

The d-q reference frame is aligned with the input line-line voltages such that $V_d = V_m$ (Max. line-line voltage) , and $V_q = 0$. There is coupling between the d and q subcircuits. The steady state variables in the d-q model are DC quantities.

The average large signal model of the boost rectifier, as shown in Figure 2.6, is perturbed and linearized at an operating point to get the small signal model (Figure 2.7). The small signal model is used for frequency domain analysis. The DC operating point is given by D_d, D_q, V_o, I_d, I_q . The power stage yields open loop transfer functions namely, $V_o/d_d, V_o/d_q, i_d/d_d, i_d/d_q, i_q/d_d, i_q/d_q$. These transfer functions are valid upto half the switching frequency. Figures 2.8(a),(b) gives the open loop transfer functions V_o/d_d and V_o/d_q respectively. These transfer functions are useful for closed loop controller design.

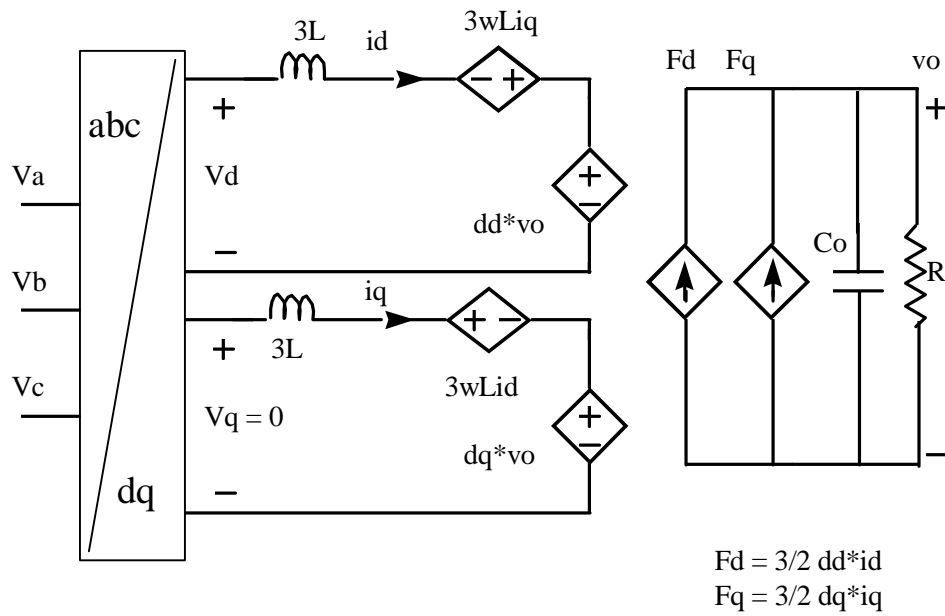
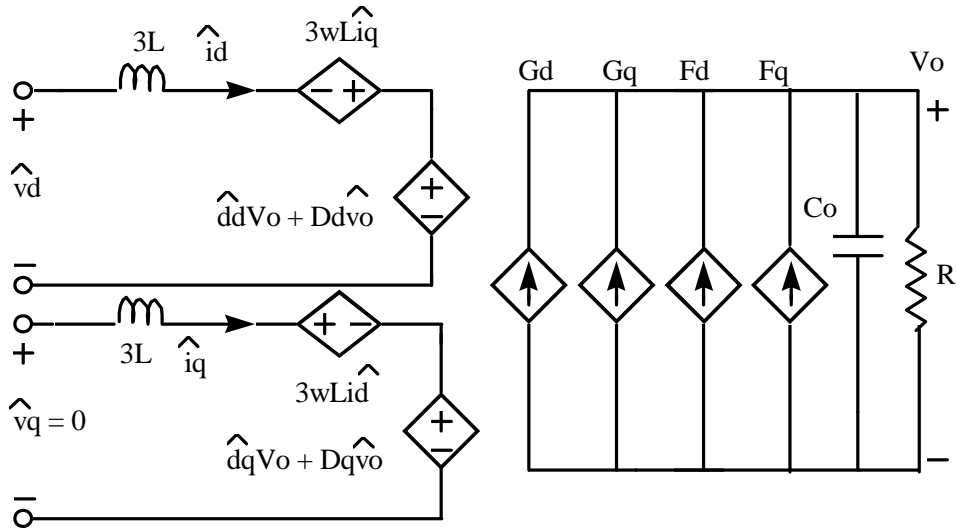


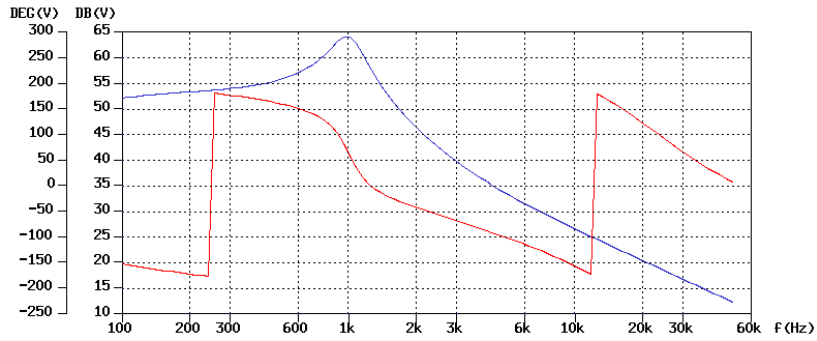
Figure 2.6 : Average Large Signal Model in Rotating Co-ordinates : *Applying the transformation T , results in the d - q model. It also results in coupling between the d and q sub-circuits shown as two voltage sources.*



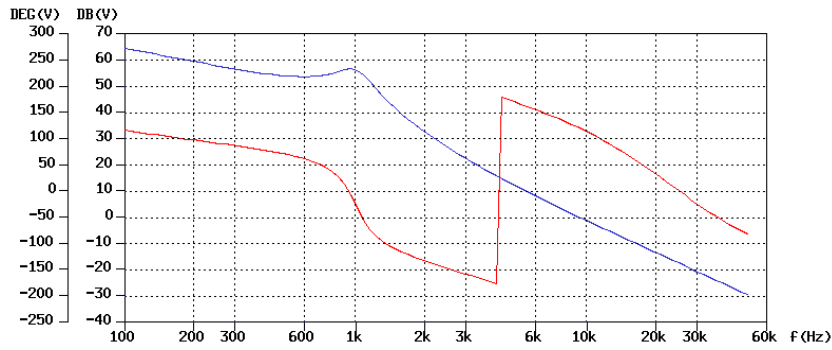
$$G_d = 3/2 D_d * \hat{i}_d \quad F_q = 3/2 d_q * I_q$$

$$G_q = 3/2 D_q * \hat{i}_q \quad F_d = 3/2 d_d * I_d$$

Figure 2.7 : Small Signal Model in Rotating Co-ordinates : *The Average Large Signal Model is perturbed and linearized at an operating point to yield this model.*



(a) Plot of V_0/d_d



(b) Plot of V_0/d_q

Figure 2.8 : Control-to-Output Voltage Transfer Function of the d & q channel : *The transfer function V_0/d_d has a complex pole around 1.2kHz and has a right half plane zero. The presence of right half plane zero deteriorates the phase of the system. The transfer function V_0/d_q is similar to V_0/d_d .*

2.3.3 Control Loop Design

The small signal model of the rectifier is utilized to design compensators. The power stage is in d-q co-ordinates and the controller is implemented in d-q co-ordinates.

Figure 2.9 gives the structure of the controller. It has an inner current loop and an outer voltage loop. The inner current controllers are H_{i_d} and H_{i_q} and H_v is the outer voltage loop compensator. I_{qref} is set to 0, as the input currents are supposed to be in phase with supply voltage and V_q is taken as 0. The d-channel transfers power to the output and the output of the voltage compensator H_v provides d-channel current reference.

As shown in Figure 2.9, the d and q channels in the power stage are coupled and the coupling is shown by the dotted arrows. As a result, it is not possible to control the d and q channels independently. Thus, the coupling in power stage is canceled by changing the current controller, as shown in Figure 2.10 (a). A cross-coupling term $3\omega L/V_0$ is introduced in both d and q channel outputs such that they cancel the coupling in the power stage. Figure 2.10 (b) shows the de-coupled power stage. Now, it is possible to design the compensator for the 2 channels independently resulting in a better performance.

Digital implementation of the current controller introduces a sampling delay, as discussed in [5]. The delay yields 180° phase lag at half the switching frequency and must be taken into account.

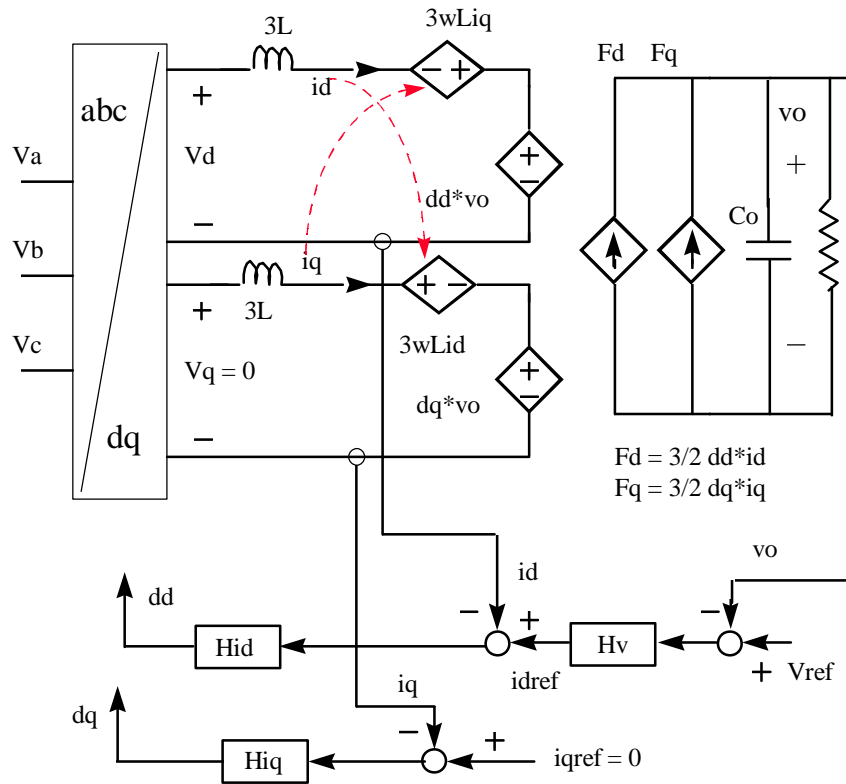
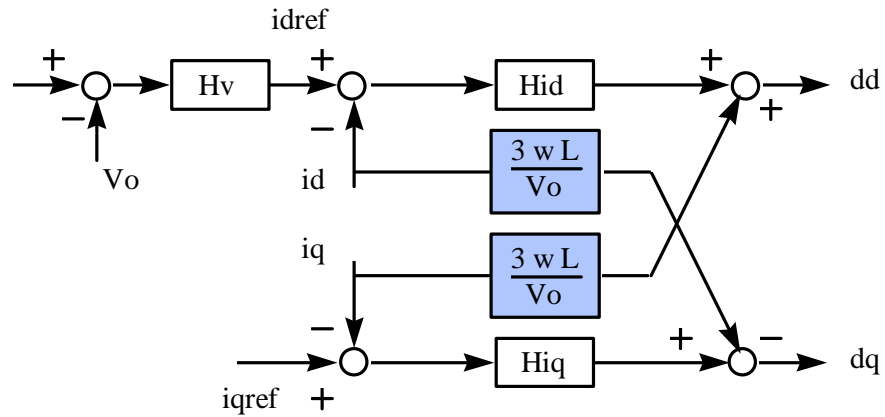
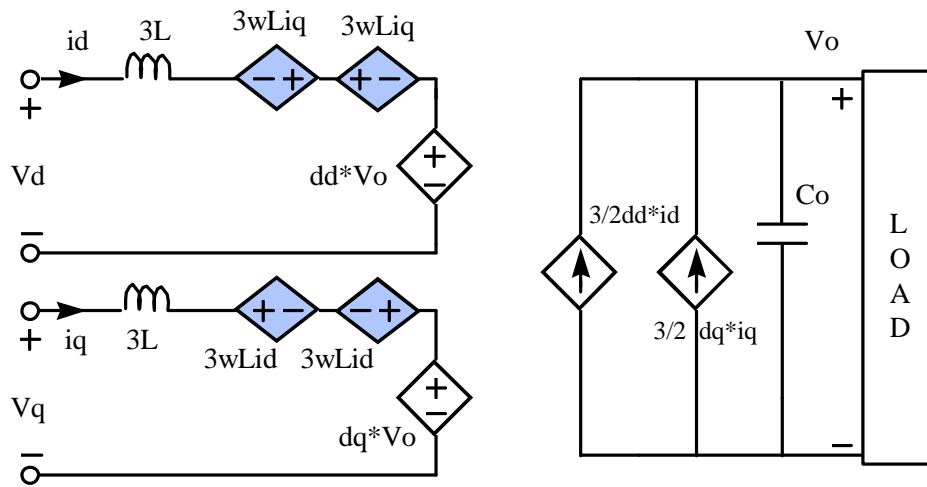


Figure 2.9 : Controller Structure as applied to Average Large Signal Model : *The coupling in the power stage is shown by the dotted arrows. It shows that d and q channels cannot be controlled independently.*



(a) Coupling in inner current controller



(b) De-coupled Power Stage

Figure 2.10 : Controller Structure incorporating Decoupling : *The new controller structure, shown in (a) includes a factor which decouples the power stage, as shown in (b).*

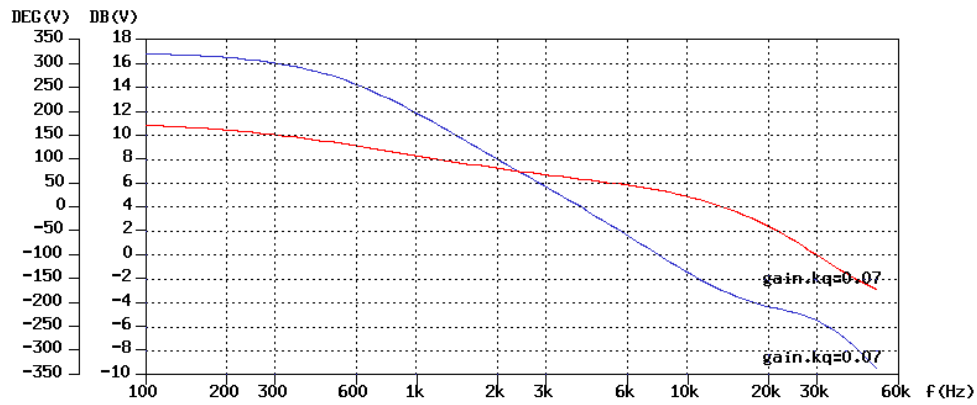
The digital delay is given by:

$$e^{-sT} = \frac{\frac{1}{12}s^2T^2 - 0.5sT + 1}{\frac{1}{12}s^2T^2 + 0.5sT + 1}, \text{ where } T = \text{Sampling Time}$$

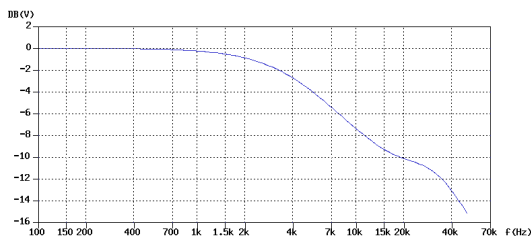
The current compensators H_{i_d} and H_{i_q} are implemented as proportional gain. The inner loop gain is limited to half the switching frequency due to the sample and hold delay. Design of the compensators depend on direct transfer functions id/id_{ref} , iq/iq_{ref} . The compensators H_{i_d} and H_{i_q} are chosen such that the transfer functions id/id_{ref} , iq/iq_{ref} are unity till the inner current loop bandwidth.

The transfer function V_o/id_{ref} , shown in Figure 2.11(a) is used to design the outer loop compensator. Fig. 2.11 (b),(c) gives the plot of iq/iq_{ref} . It can be seen that it has a wide bandwidth and that iq follows iq_{ref} at low frequencies. Plot of id/id_{ref} is also similar.

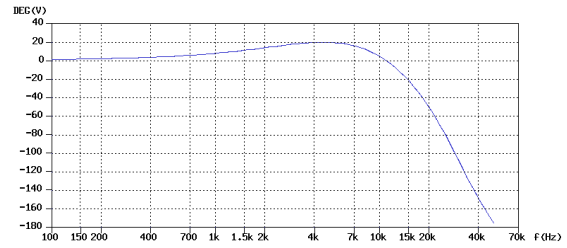
Fig. 2.11 (d),(e) gives the outer loop gain $T_v = (V_o/id_{ref}) * H_v$. The compensator is implemented as a proportional and integrator compensator as it ensures zero steady state error. The loop gain is adjusted to get good phase margin. The q channel control to inductor current transfer function is designed to be unity upto the current bandwidth i.e. 2 kHz. The outer loop gain T_v has a bandwidth of 1 kHz and phase margin of 50° .



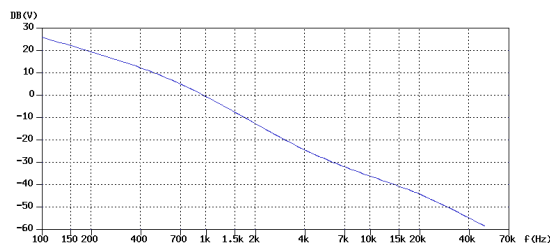
(a) Transfer function $V_0/i_{d_{ref}}$



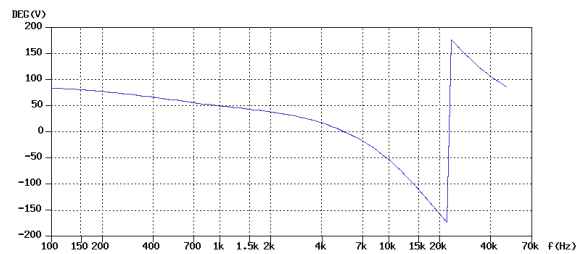
(b)



(c)



(d)



(e)

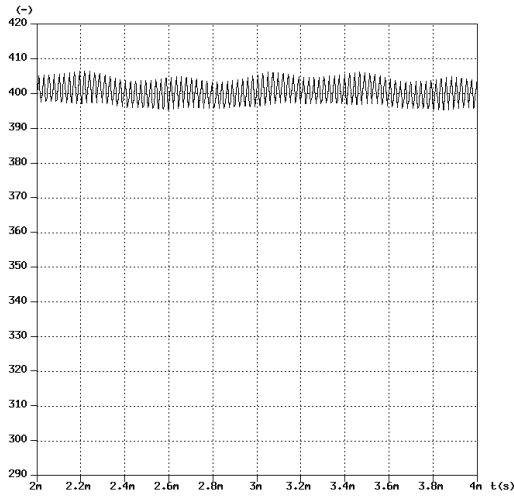
Figure 2.11 a-e :Closed Loop Transfer Functions of the Rectifier (a) $V_0/i_{d_{ref}}$ plot (b) $i_q/i_{q_{ref}}$ magnitude plot (c) $i_q/i_{q_{ref}}$ phase plot (d) T_v magnitude plot (e) T_v phase plot .

2.3.4 Simulation Results

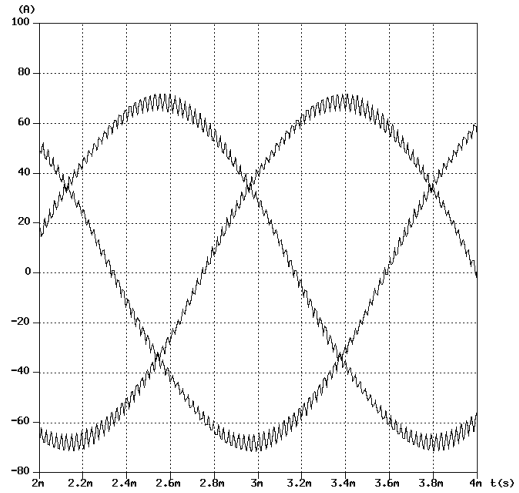
The three phase boost rectifier, shown in Figure 2.3, is designed to supply 15 kW output power and ensure PFC. The power stage parameters are given in Appendix A. The controller parameters are designed as described in section 2.3.3. An EMI filter is used to reduce the switching spikes in the input phase current.

The Discrete Switching model was implemented using SABER and MAST. Figure 2.12 (a) shows the regulated output DC link voltage. The output voltage is regulated to 400V. The switching frequency ripple information can be obtained from it. Fig. 2.12 (b) shows the balanced three phase input current drawn by the rectifier. Proportional compensators were used in the current loop and proportional-integral compensators were used in the outer voltage loop to ensure zero steady state error. The switching frequency employed was 40 kHz. The bandwidth of the outer loop is 1 kHz and it has a phase margin of 50 degrees.

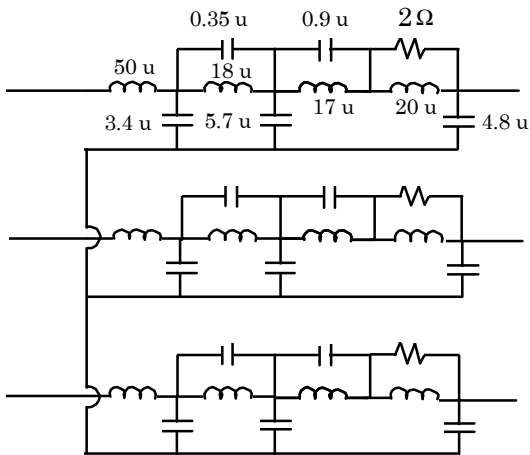
Figure 2.12 (c) shows the input EMI filter to the rectifier [9]. The filter is designed to reduce the switching ripple from the current drawn by the rectifier. Figure 2.12 (d) shows the current drawn by the EMI filter and it is in phase with the input phase voltage. The input current drawn by the EMI filter is smooth and devoid of any switching ripple. The EMI filter draws reactive current and causes phase shift between the input supply voltage and current. In order to compensate the phase shift caused by the input filter [10], I_{qref} value is chosen so as to cancel the reactive current drawn by the input filter in steady state.



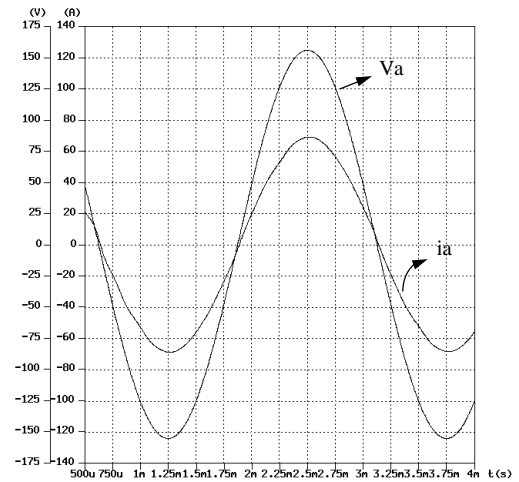
(a) Output DC Link Voltage



(b) Input current drawn by the rectifier



(c) Input EMI Filter



(d) Input Phase Current & Voltage

Figure 2.12 : Simulation Results of 15 kW Rectifier with Input EMI Filter : The switching frequency employed was 40 kHz. .

2.3.5 Fault Tolerance

The PEBB based system has the ability to reconfigure the system operation and maintain power flow in case of a fault condition. The conventional system suffers from the drawback that if one of the legs of the rectifier switches fails then the system has to be shut down. Thus we need to have redundancy in the system and this increases the cost of the system. The typical fault condition in a DC DPS system occurs as a result of failed semiconductor switches either short circuited or open circuited. This fault condition is analyzed in this section.

Figure 2.13 shows the configuration of the system composed of PEBBs. The mid point of the split dc link is connected to the supply neutral through a switch. The switch is normally open and is closed in case of a fault in one of the legs of the rectifier.

Figure 2.14 shows the configuration of the system with leg c of the rectifier failed open circuited. The neutral connection is closed and the local controller commands the current controller to change the control strategy. As the inner controller is implemented digitally, it is a matter of implementing a sub routine in the DSP which changes the control strategy.

As discussed in section 2.3.1, the controller is implementing Space Vector Modulation (SVM) control. SVM control involves current controller in rotating co-ordinates and cannot be implemented when one phase fails. As shown in Figure 2.15, the controller achieves PFC for the remaining 2 phases by using proportional - integral compensators for

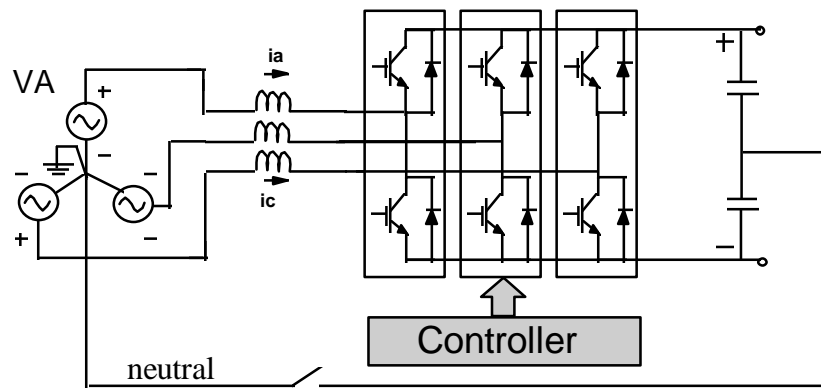


Figure 2.13 : Rectifier Configuration in Normal Operation Mode: *The midpoint of the DC link has a connection to the supply neutral. The switch is open during normal operation mode.*

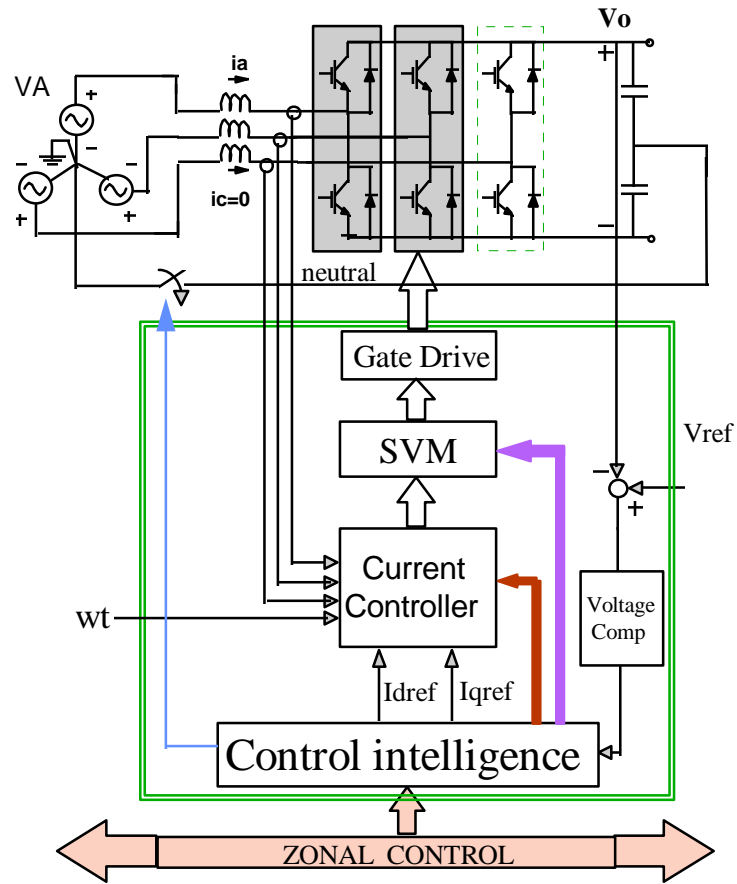


Figure 2.14 : Rectifier Configuration with Phase 'c' Open Circuited: *The rectifier is assumed to have a fault with phase c open circuited. The controller closes the switch in neutral wire..*

the inner current loop. The rectifier supplies the same rated output power by drawing 1.5 times more phase current. The control intelligence ensures that the output gate pulses are provided to the two healthy phases. The control strategy is changed to output correct gate pulses.

Figure 2.16 (a)-(d) show the simulation results for the reconfigured system during fault mode. Figure 2.16 (a) shows the input current drawn by the two active legs of the rectifier. Figure 2.16 (b) shows the current carried by the neutral wire. Figure 2.16 (c) shows that PFC is obtained for the remaining 2 phases. Figure 2.16 (d) shows the regulated DC link voltage.

The output DC link has a low frequency oscillation due to charging of the capacitors by the neutral current. Thus, capacitance of the order of 1mF is needed to reduce the output voltage ripple on the DC link. The disadvantage of the scheme is that the neutral wire carries a large current and the phase current increases to 1.5 times the normal value. But, the system is stable and can operate for the transition time till the fault is cleared away.

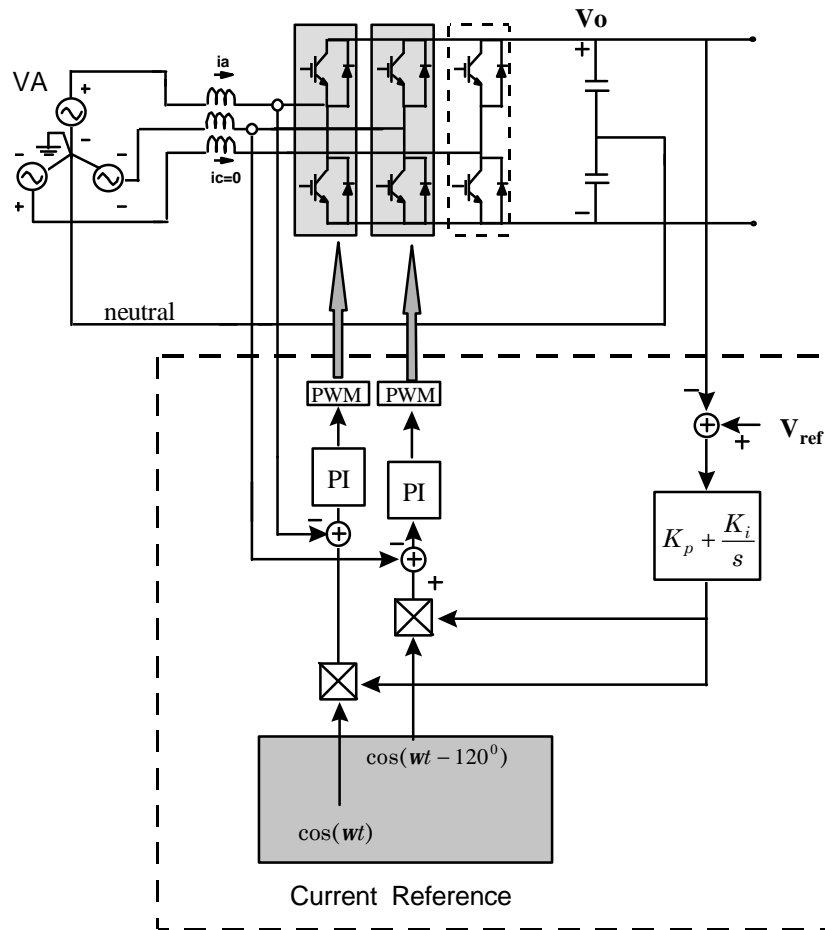
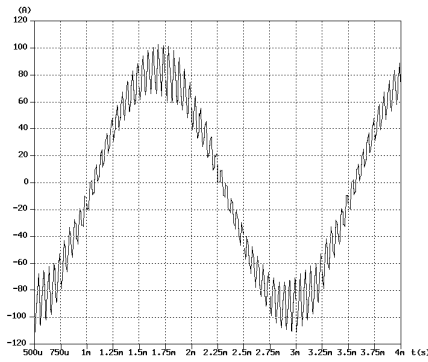
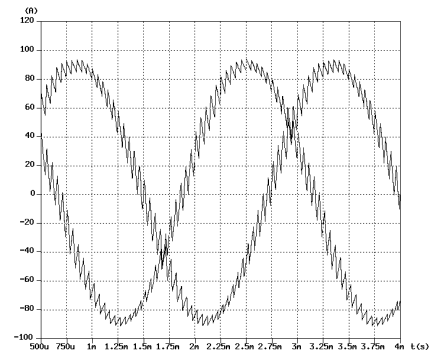


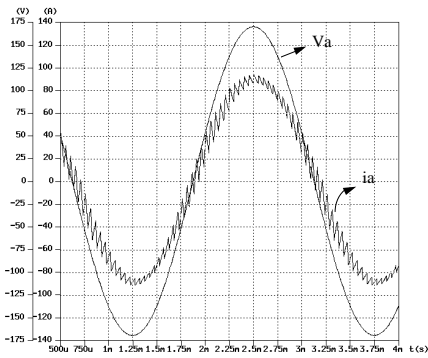
Figure 2.15 : Reconfigured Controller Structure : *The control algorithm changes such that instead of SVM technique, the two healthy phases are controlled independently with an inner current loop and a common outer voltage loop.*



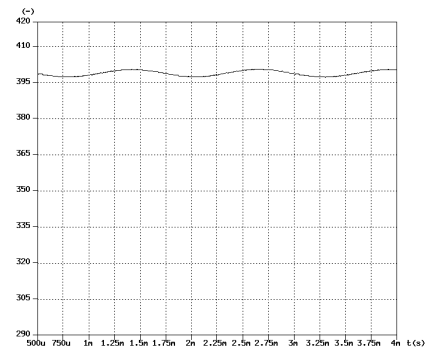
(a) Phase currents i_a , i_b



(b) Neutral current



(c) Phase current (i_a) and phase voltage (v_a)



(d) Output DC rail voltage

Figure 2.16 : Simulation Results for 15 kW Rectifier under fault mode operation
The rectifier is stable after system reconfiguration. The healthy phases carry 1.5 times the rated current. The output DC link has a low frequency oscillation due to the charging of the capacitors by the neutral current.