Thin Film Polymer Dielectrics for High-Voltage Applications under Severe Environments

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(ABSTRACT)

This thesis presents the results of research into the performance of advanced polymer dielectrics for the realization of high-power electronic circuits in a miniature form. These polymeric materials must satisfy a number of critical thermal, environmental, and electrical requirements to meet the required performance criteria for microelectronics applications. These desired attributes include thermal stability, low moisture uptake, high breakdown voltage (low leakage current), low dielectric constant, low loss tangent, high glass transition temperature, and low surface roughness. The use of these polymers allows for advanced electronic packaging techniques, resulting in improved system performance and reliability.

Research was performed using a commercially available polymer dielectric and evaluated the feasibility of utilizing these materials as interlayer dielectrics in multilayer power electronic circuits. Historically, efforts to develop advanced interlayer dielectric materials have concentrated on promoting their use in high speed digital circuits. However, dielectrics used in power electronics must meet requirements not commonly stressed in designs for digital circuits. Multilayer circuits used in power electronics place a particular emphasis on the material properties of high dielectric strength or breakdown voltage and small values for loss tangent or dissipation factor. The focus of this research has been to characterize these particular properties for a commercially available polymer dielectric.

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Chapter 1 - Introduction

1.1 Objectives and Goals of Research Work

The work presented in this thesis describes methods useful in the characterization of the electrical properties of polymer dielectrics under environmental stress.

Polymeric materials have been utilized extensively in the electronics packaging market, due to their low cost, ease of processing, chemical inertness, and attractive electrical properties. Great strides have been made in the miniaturization of electronic packages as a result of the use of thin film multilayer structures and specifically, deposited multichip module (MCM-D) techniques.

1.2 Statement of Problems

While high-density, digital circuits have made extensive use of polymer dielectric packaging materials, there has been little effort to date to incorporate these materials into high power electronic applications. Demand for smaller and lighter power supplies and related electronics has created a need for new innovations in packaging designs and materials. The use of polymeric materials in high power electronic packaging is the focus of the research described in this thesis.

To ensure proper operation of a high power electronic circuit, proper isolation must be ensured between adjacent conductors. High voltage arcing and leakage currents are typical problems encountered in high voltage circuits, and are exacerbated at high frequencies. To counter these effects, a good dielectric material must display low values for dielectric constant and loss tangent and a high value for breakdown voltage.

1.3 Techniques Used

To measure the performance of a dielectric under the high voltage and environmental stresses, a capacitor structure is commonly used. This structure may be used for both the measurements of dielectric constant and loss tangent, and then destructively tested for the

breakdown voltage of the dielectric material. Additionally, the structure can be placed under controlled conditions of temperature and humidity to evaluate the dielectric materials response to these factors.

The electrical properties of dielectric constant and loss tangent for a dielectric utilized in a thin film capacitor structure may be derived from the measurement of that structure's complex impedance. An impedance meter can perform this measurement under computer control over a span of frequencies, typically 1 kHz to 100 MHz. Once this measurement is performed and the effects of probing the structure are removed, an accurate value for the dielectric constant and loss tangent can be derived. Finally, a high voltage DC bias is placed across the capacitor to determine the breakdown voltage of the dielectric material.

1.4 Main Contributions

The work and research presented in this thesis is intended to demonstrate the applicability of polymers as materials for high voltage electronics packaging. The effects of electrical and environmental stress on these materials and specifically on their electrical properties of dielectric constant, loss tangent, and breakdown voltage are critical to the development of successful packaging materials. This thesis attempts to quantify the effects of humidity and temperature upon the electrical performance of polymeric materials.

1.5 Structure of Thesis

This thesis is organized into five chapters. The first chapter is this Introduction. Chapter 2 presents a review of the application of polymer dielectric materials to electronics packaging and the different chemistries currently available. Next, the processing of polymers in the assembly of an electronic multilayer circuit is discussed. The critical electrical, thermal, and mechanical properties of polymers are described next and finally, this chapter presents an overview of the use of polymer dielectrics in deposited multichip module (MCM-D) applications.

Chapter 3 describes the techniques used to deposit, pattern, and assemble the experimental capacitor structures used in this research. The thin film deposition and

photo-lithographic patterning techniques used are presented, highlighting the processing steps developed by the author. Design decisions for the substrates and test fixtures are presented along with justifications for choices made. Finally, a description of the environmental chamber fixture used during testing is given.

Chapter 4 presents the results of electrical testing performed to characterize the electrical performance of the polymer dielectric materials, for both ambient and elevated temperatures and humidities. The dielectric constant and loss tangent are derived from the complex impedance measured using an impedance meter, and the breakdown voltage is determined using a high voltage DC power supply.

Finally, Chapter 5 summarizes this thesis, and it also provides a brief description of future recommended work intended to extend the techniques learned during the course of the research for thesis to the characterization of other materials for electronics packaging.

Chapter 2 - Literature Review

2.1 Introduction

Current trends in microelectronic packaging have shown a need for developing advanced dielectric materials for realization of high performance interconnects of electronic devices. Much of the research has focused on developing multichip module (MCM) packaging strategies to achieve higher system performance in high speed digital applications. Recently, it has been proposed that the techniques and materials developed for these advanced packaging solutions be applied to power electronics as well [1]. Traditionally, electronic packaging for power applications has emphasized functionality over structure, topology design, and circuit density. However, current electronic markets such as wireless communications and portable computing are placing an increasing emphasis on reduced size and increased performance from power supply and conversion devices. Current printed wiring board (PWB) designs and densities have limitations in the provision of smaller size and increased thermal performance of advanced MCM-ceramic (MCM-C), and MCM-deposited (MCM-D) packaging techniques.

High density thin film interconnections allow chips or dice to be placed closer together than in conventional single chip packaging, thereby reducing propagation delay and system cycle time. This approach to packaging is known as MCM-deposited or MCM-D and its development has resulted in the creation of new materials and processes to achieve its performance gains. Dielectric materials used for thin film multichip modules must meet a number of material and electrical requirements crucial to high density microelectronic packaging, including a low dielectric constant, low dissipation factor, minimal moisture uptake and release of volatile byproducts, a smooth surface for the fabrication of fine metal traces with high resolution, and thermal stability during subsequent processing and under load. Early work on multichip modules placed a number of circuits on a common monolithic silicon substrate with SiO_2 acting as the common interlayer dielectric. The use of polymer materials as interlayer dielectrics in MCM-D thin film packaging was a relatively recent development. The interest in

polymer dielectrics can be attributed to their relatively low dielectric constants and their ease of processing. For power applications, the high currents and voltages associated with power electronic circuits require materials with specific attributes. These additional properties include a high dielectric strength or breakdown voltage and small values for loss tangent or dissipation factor.

The first polymer materials to be extensively investigated for use in MCM-D technology applications were polyimides. Their high chemical resistance and low dielectric constants made them initially attractive, but their excessive moisture absorption and reactivity with thin film metallizations have limited their use. Modifications to the monomer backbones such as the addition of photosensitive, fluorinated, and highly flexible functional groups have succeeded in eliminating the most severe drawbacks of the polyimides, but not without undesired side-effects such as poor adhesion or reduction in mechanical strength. More recently, polymers with new and novel chemistries such as benzocyclobutene (BCB), polyphenylquinoxaline (PPQ), and fluoropolymers have been introduced to the market possessing attractive properties surpassing those of standard polyimide chemistries.

2.2 Polymer Chemistry

2.2.1 Polyimides

Currently, polyimides are the material of choice for interlayer dielectrics in thin film microelectronics packaging applications, since they are based on a mature technology and satisfy the requisite properties to survive the thermal, chemical, and mechanical stresses associated with microelectronic fabrication processes. Polyimides are a class of polymers which are synthesized from two monomers, a dianhydride and a diamine. Commercial products are supplied as soluble polyamic acid (PAA) intermediates, which undergo a thermal imidization with the evolution of water to form the insoluble polyimide. These reactions are shown schematically in Figure 2.1. Various polyimide analogs have been developed to avoid some the inherent undesirable properties of polyimides, such as excessive moisture absorption and high dielectric constants. These polyimides have

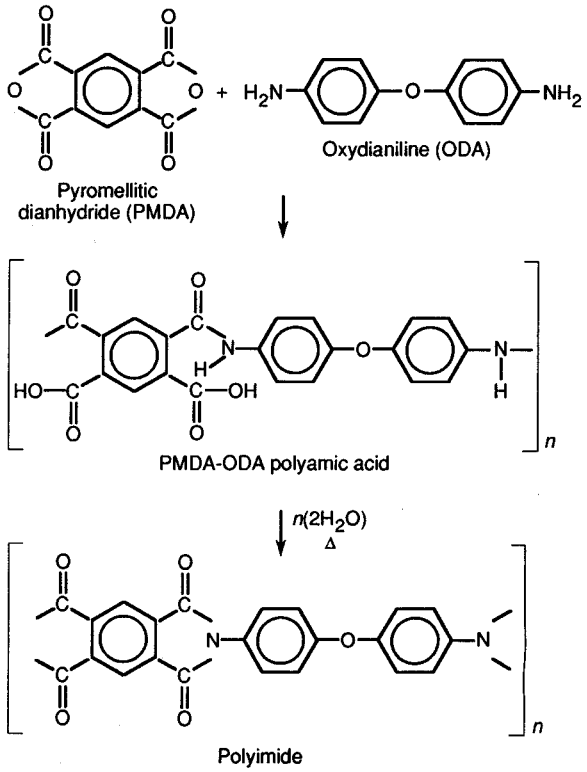


Figure 2.1 Imidization reaction of PMDA-ODA polyimide

emphasized structural modifications on the diamine and dianhydride monomers, with the inclusion of flexible bridge monomers, fluorinated and silicone monomers, and acetylene terminated poyimides. Another unique polyimide morphology known as nano-foams has been developed which incorporates voids of air (with a dielectric constant on the order of 1) in the film structure. The presence of a high percentage by volume of these voids has the effect of lowering the overall dielectric constant for the polyimide based dielectric material.

2.2.1.1 Standard Polyimides

Conventional polyimide chemistries are typically based upon the polyamic acid (PAA) formed from pyromellitic dianhydride (PMDA) and oxydianiline (ODA). Like many other aromatic polyimides, it has a linear, symmetric diimide structure that lends itself to a small effective dipole moment for the repeat units, which contributes, in part, to its low dielectric constant. The imide repeat unit is shown in Figure 2.2. This polyimide

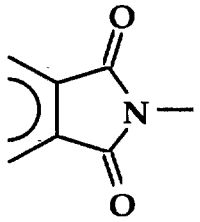


Figure 2.2 Imide repeat unit

chemistry is commonly used for interlayer dielectrics due to its attractive properties. These include a high thermal stability with a glass transition temperature, T_g > 300°C, a low dielectric constant, good chemical stability, and its ease of processing. However, its tendency to absorb moisture causes the polyimide layers to swell and their dielectric constants to increase significantly.

2.2.1.2 Low-Stress (Low CTE) Polyimides

When constructing multilayer structures on silicon wafer or ceramic substrates, the use of materials with coefficients of thermal expansion (CTE) closely matched to the substrate material and silicon devices significantly improves the reliability of interconnection structures during heating and cooling cycles. The most common polyimide backbone chemistry used to meet this requirement is based on biphenyltetracarboxylic dianhydride (BPDA) and paraphenylene diamine (PPD). These polyimides are commercialized by Olin/Ciba Geigy (OCG) under the trade name Probamide™. Another commerically available low-stress polyimide is the PIQ series, manufactured by Hitachi. Besides being low-stress, these structures also show increased thermal stability due to the polyisoindoloquinazolinedione structure shown in Figure 2.3. Other desirable properties of these polyimides include reduced moisture absorption and lower dielectric constants

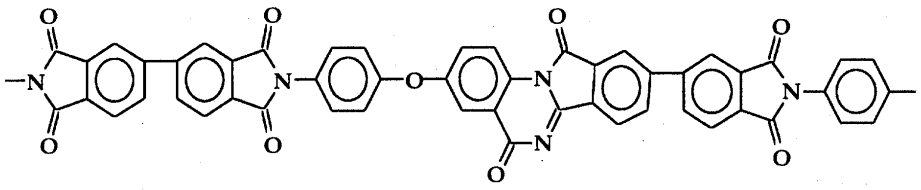


Figure 2.3 Structure of PIQ

than standard polyimides. However, the anisotropic nature of the CTE values between the Z-axis and the X-Y plane raises concerns about the ultimate reliability of the interconnect structure. Also, low-stress polyimides do not adhere well to other materials or to themselves, requiring specialized processing steps to promote the reliability of the multilayer structure.

2.2.1.3 Fluorinated Polyimides

A common approach to reducing the dielectric constant of polyimides is the inclusion of organofluorine components, in the form of pendant perfluoroalkyl groups. The polyamic acid precursor for fluorinated polyimides is commonly based on hexafluorodianhydride-oxydianiline (HFDA-ODA). The inclusion of fluorinated monomers in the polyimide backbone has been found to reduce their moisture absorption and dielectric constant. Unfortunately, these polyimides generally show an increased susceptibility to chemical attack, making their use in multilayer fabrication questionable. Recently, however, newer formulation have improved the chemical resistance of the polyimide and have demonstrated a unique wet etch capability for vias with aspect ratios approaching 1.2:1. These formulations are commercially available in polyamic acid form from Amoco under the trade name Ultradel. These polyimides have a slightly modified chemical structure based on hexafluorodianhydride-aminophenoxy-biphenyl (HFDA-APBP).

2.2.1.4 Nanofoams

Polyimide foams have been synthesized which contain pores on the scale of nanometers, hence the name "nanofoam" [2]. They are prepared from block copolymers consisting of thermally stable PMDA and thermally labile poly(propylene oxide) (PO) blocks, the latter being the dispersed phase. Foam formation is effected by thermolysis of the PO blocks, leaving pores the size and shape corresponding to the initial copolymer morphology as the degradation products slowly diffuse out of the films. The presence of air in these pores have the net effect of lowering the bulk dielectric constant of the material and values as low as 2.3 have been reported [3]. By the addition of functional groups, the polyimide can be further tailored to exhibit desirable properties such as low moisture absorption and lower reactivity with metal interconnects. To date, the use of nanofoams

in a microelectronic application has yet to be demonstrated. Their interactions with other packaging process materials and environments have also not been evaluated. Thus, incorporation of these polyimides into a thin film multilayer process may prove to be quite a challenge.

2.2.1.5 Alternative Polyimide Chemistries

An alternative polyimide formulation uses an acetylene terminated polyimide backbone. These polyimides are especially desirable in applications where planarization of the interlayer dielectric is important. During the curing of these low molecular weight oligomers, cross-linking occurs through the acetylene end groups resulting in a high temperature, high molecular weight dielectric. It is important to note that the cross-linking of the acetylene groups during cure occurs without the evolution of water. Due to the low molecular weight and the resultant high solubility of these oligomers in solvents such as n-methyl pyrrolidone (NMP), outstanding planarization is acheived. However, the reduced stress formulations of these polyimides are obtained at the expense of the planarizability of the original formulations.

Recent studies by IBM have identified polyamic ester polyimides that improve upon some of the undesirable characteristics of polyamic acids such as their high curing temperatures, reactivity with copper metallizations, and poor planarization [4]. An example of the polyamic ester structure is depicted in Figure 2.4. These polyimides do not evolve water during the curing reaction, but, release alcohol instead. Another concern with this formulation is their requirement for more processing steps than standard polyimides.

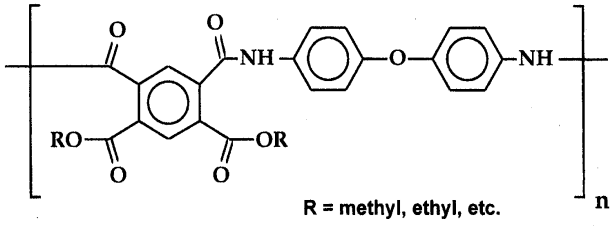


Figure 2.4 Structure of polyamic ester polyimides

2.2.2 Benzocyclobutenes (BCB)

This class of polymers has emerged as the most significant alternative to polyimides for use in multilayer interconnection structures. Polybenzocyclobutenes (PBCB) are a general class of thermoset resins derived from bisbenzocyclobutene monomers. The properties of the polymer may be tailored for particular applications by altering the reactive group in the polymer backbone, shown in Figure 2.5. BCBs are typically supplied by manufacturers in a "b-staged" or partially polymerized form where the bisbenzocyclobutene monomer incorporates the aforementioned substitutent group, as shown in Figure 2.6, and is suspended in a solution of xylene or mesitylene. In this form, the BCB prepolymer consists of low molecular weight oligomers and can be applied either by spin or spray coating techniques to the multilayer substrate. Thermal polymerization of BCBs occurs around 250°C without the evolution of byproducts, allowing partially cured structures to be deposited. Any subsequent high temperature processing, such as reflow soldering of components, will complete the curing of the deposited films. This makes BCBs particularly attractive in applications where adhesion and stress management are key concerns. Curing of BCBs must occur in an oxygen-free environment due to the rapid oxidation of the benzylic CH_2 groups to anhydride and/or carbonyl species. Oxidation of BCB films has the effect of severely degrading their

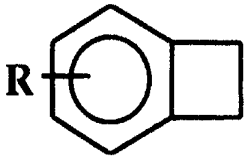


Figure 2.5 Ring structure of BCBs

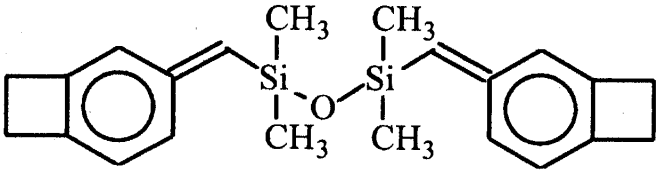


Figure 2.6 Structure of BCB precursor

electrical and physical properties. Also, BCBs tend to be less thermally stable than polyimide alternatives, showing sizeable weight loss over time at temperatures above 300°C. However, newer formulations of BCBs have been developed recently [5] which reduce the sensitivity of these polymers to oxidation and thermal degradation. Desirable attributes of BCBs include low moisture absorption (< 0.25 % by weight), low dielectric constants (2.7), and excellent planarization of multilayer substrates (70 to 90%) in their non-photosensitive formulations.

2.2.3 Fluoropolymers

The inclusion of fluorinated groups in a polymer backbone has been shown to dramatically reduce the dielectric constant and moisture sensitivity associated with traditional polymer dielectrics, especially polyimides. Polytetraflurorethylene (PTFE or Teflon) has a low dielectric constant of 2.1, the lowest of any organic material. However, PTFE is insoluble, which make deposition using traditional processing techniques difficult. An alternative method utilizes vapor deposition of PTFE in a two step process [6], but results in a conformal rather than planarizing topology. Two commercially available fluoropolymers are CYTOP and FLARE. CYTOP (Cyclic Transparent Optical Polymer) is a perfluoronated amorphous polymer, which was developed by Asahi Glass Company. CYTOP has the peculiar polymer structure shown in Figure 2.7 which is different from any other existing fluoropolymers, but CYTOP is similar to PTFE in chemical and physical characteristics. Attractive properties of this polymer include: high thermal stability (decomposition temperature> 400°C), low dielectric constrant (2.1-2.2), low water absorption (<0.01%), and excellent chemical resistance. Also, since it is a thermoplastic, it lends itself well to extrusion coating. Another fluoropolymer, produced

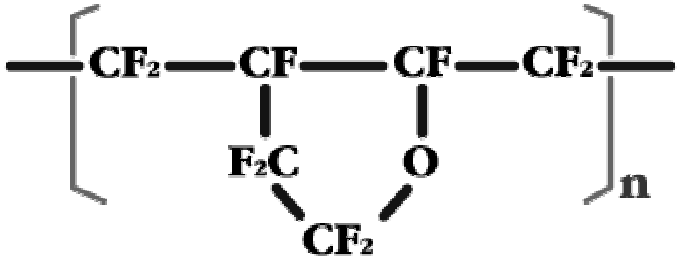


Figure 2.7 Structure of CYTOP

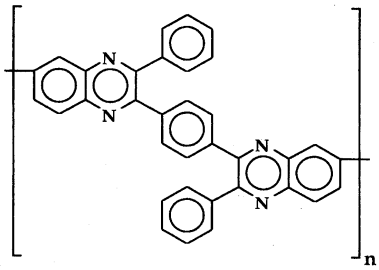


Figure 2.8 Structure of PPQ

by Raychem, is known by its trade name, FLARE. FLARE is a fluorinated poly(aryl ether) prepared by the reaction of decafluorobiphenyl with diphenols. The diphenol can be varied to change the characteristics of the polymer. The polymerization reactions are carried out in a polar aprotic solvent, such as N,N-dimethyl acetamide, using a base as catalyst to yield high molecular weight polymers. FLARE exhibits low moisture absorption (0.15%) and low dielectric constant (2.6-2.7), but reliability of thin film structures may be questionable due to their relatively low thermal stability.

2.2.4 Polyphenylquinoxaline (PPQ)

PPQs belong to a group of fully cyclized heterocyclic polymers that are produced commercially by Cemota. The formation of PPQs is a polycondensation reaction between a tetra-amine and a tetraketone. The structure of these polymers is shown in Figure 2.8. These polymers exhibit low moisture absorption (0.8%) and low dielectric constants (2.8), but have lower solubility in common solvents such as NMP, which limits the thicknesses of deposited films on multilayer substrates. Also, the use of noxious solvents such as metacresol and xylene is required for deposition processes. Another related chemistry similar to PPQ is polyquinoline (PQ), a nitrogen-containing polyheterocyclic polymer commercially available from Maxdem. PQs are a thermoplastic material which are soluble in common solvents such as NMP. After curing, the polymer appears to partially crosslink, and exhibits excellent chemical resistance. These polymers are characterized by high thermal stability (decomposition temperature>500°C), low dielectric constant (2.6-2.8), and low moisture absorption (<0.15%). Deposition and curing processes are almost identical to those use with standard polyimides.

2.2.5 Other Chemistries

In the pursuit of polymer dielectrics with properties surpassing those of standard polyimides, many new and unique chemistries have been investigated. A new class of olefinic polymers have been developed by BF Goodrich that provide many advantages over polyimide dielectrics [7]. This polymer family, based principally on polynorbornene, is produced via a transition metal catalyzed polymerization. They can be described as amorphous, hydrocarbon polymers that are characterized by a very stiff polymer backbone resulting from the steric crowding of the bulky saturated cyclic groups. Attributes that make these polymers attractive include excellent thermal and electrical performance, good adhesion to conductors and substrates, low moisture uptake, low dielectric constant, and ease of processing. Teflon-based polymers have attracted interest due to their low dielectric constants, but poor adhesion and chemical resistance have damped some of the initial enthusiasm for their use in multilayer thin film circuits. A new approach developed by Gore has been the addition of a polymerizable thermoset resin to expanded polytetrafluoroethylene (ePTFE). The resin is a methyl cyanate ester which fills the open pore structure of the ePTFE. The composition is provided partially cured by the manufacturer as a dielectric sheet which can then be laminated to the multilayer substrate and processing by conventional methods. Since no solvents are present in the polymer, problems associated with film shrinkage and outgassing of volatiles are essentially eliminated. The lamination method also ensures a high degree of planarization of the dielectric layer and no waste of material. The mechanical properties of the dielectric are almost completely dominated by the presence of the resin, ensuring good adhesion and mechanical strength. The polymer also retains attractive properties associated with fluoropolymers, including low moisture uptake (<1.0%) and low dielectric constant (2.7).

2.3 Polymer Processing

Many of the processes used to deposit, pattern, and cure thin film polymer dielectrics have been adapted from the semiconductor industry. These methods result in highly uniform coatings

2.3.1 Dielectric Deposition

Analagous to photoresist application in the IC industry, the application of organic dielectrics have evolved from traditional spin coating technology to more advanced methods such as spray and extrusion coating. The emphasis in thin film formation is to achieve the desired thickness in the fewest number of coating steps possible. Uniformity, planarity, and the absence of defects such as pinholes are the key issues relating to dielectric deposition.

2.3.1.1 Spin Coating

This method is the most commonly used in the application of polymer precursors to a substrate surface. For example, commercial polyimides are provided as solutions of a polyamic acid (PAA), that has been prepared by condensation of a dianhydride and a diamine. A commonly used aromatic polyamic acid is formed by condensation of pyromellitic dianhydride (PMDA) and oxydianiline (ODA) in n-methyl pyrrolidone (NMP) solution. This solution is then dispensed in a measured amount upon the surface of a substrate. The substrate is then spun on a vacuum chuck at a high speed (up to 5000 rpm), and the solution is evenly distributed across the substrate surface. The thickness of the deposited film is a function of the ratio of solids and solvent in the precursor solution and the spin speed. The deposited precursor is then cured in a convection furnace at temperatures sufficient (>300°C typically)to complete the polymerization of the constituents and formation of the polyimide film. The spin-coating process is shown pictorially in Figure 2.9.

This method produces films which planarize the features of the substrate such as metal traces and previous polymer layers. The effect of this planarization is to ensure consistent electrical properties of the coated and subsequently deposited circuitry across the entire substrate. Relatively thick layers of polyimides can be deposited and multiple layers may be built up on the substrate if the polymer chemistry is compatible with this process. However, the amount of waste material generated by this method is quite high as most of the precursor solution is thrown off the substrate during the spin casting process. Also

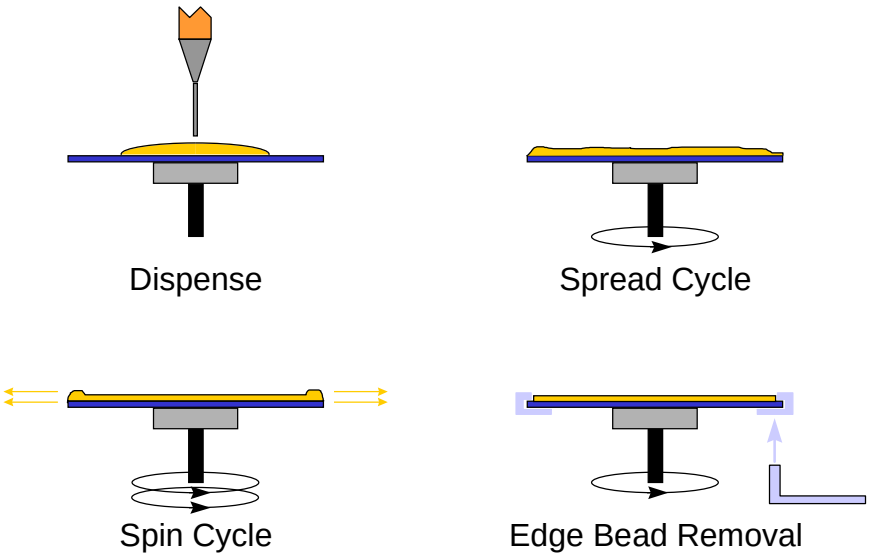


Figure 2.9 Spin-coating process

inherent to this process is the formation of edge beads which require an additional removal process prior to subsequent process steps. With the current trend toward larger substrate formats, these limitations will be exacerbated.

2.3.1.2 Extrusion Coating

This process has been proposed as a lower cost alternative to spin coating for producing highly uniform thin films on large area substrates. In extrusion coating, the extrusion head is positioned at a predetermined height above the substrate, as shown in Figure 2.10. The process fluid is metered through a precision linear orifice in the head, while the

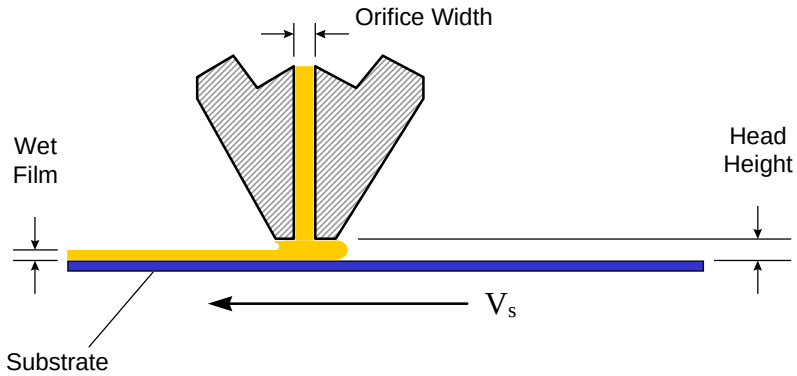


Figure 2.10 Extrusion coating process

substrate travels beneath it at a set velocity. Film thickness, T, is determined by:

$$T = \frac{R_p \cdot S_f}{V_s \cdot W} \tag{2.1}$$

where

R_p = Pump Rate (cm^3/s)
S_f = Shrinkage Factor
V_s = Transport Speed (cm/s)
W = Substrate Width (cm)

Film thicknesses from less than 1 μm to greater than 150 μm in a single coating pass have been demonstrated at uniformities of less than ± 3% on substrates up to 350 mm x 400 mm [8]. A key commercial advantage of extrusion coating is that it can be more easily integrated into high throughput microelectronics fabrication lines. Also, since the coating method is a direct apply process, waste of precursor materials is avoided. However, any variation in the substrate surface uniformity is transferred to the extrusion head during the deposition process. Furthermore, edge beads form along the leading edge of extrusion coated substrates, although not to the extent found in spin-coated films. Control schemes exist in which the fluid flow into the extrusion head and the internal head pressure are measured and passed to a computer which then determines the proper motion profile for the extrusion head to improve the uniformity of the coating along the leading edge.

Another method related to extrusion coating is curtain coating. A diagram depicting this process is shown in Figure 2.11. In curtain coating, a continuous curtain of the resin dissolved in an appropriate solvent carrier is forced through a slit while the substrates to be coated are passed under the falling curtain by a conveyor system. The distance from the coating head to the substrate is significantly larger than for other coating methods. Undeposited material can be recirculated back to the coating head. By careful control of

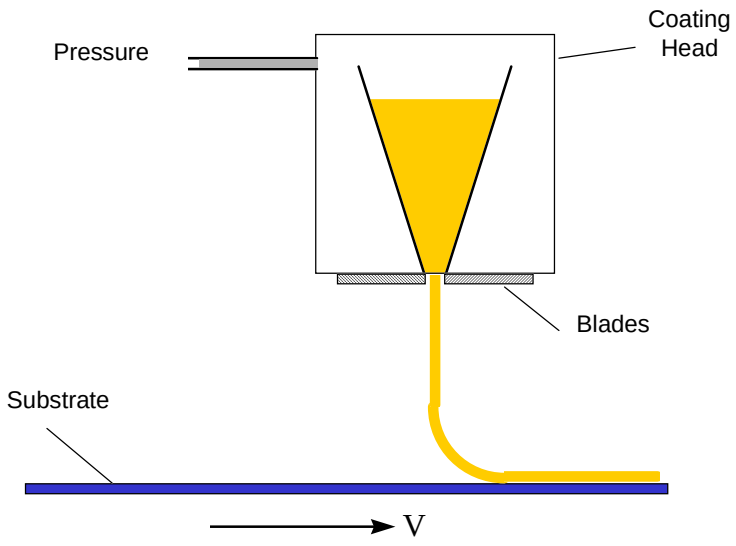


Figure 2.11 Curtain coating process

material viscosity, belt speed, and pump speed, reproducible thicknesses can be achieved and maintained over the substrate surface with < 10% variation in the overall thickness. A disadvantage of the curtain coating process is the loss of solvent from the coating material as it falls through the air. This loss must be countered by monitoring of the viscosity of the recirculated material and with periodic addition of casting solvent to maintain performance within the desired viscosity range.

Meniscus coating is another viable coating method, especially for large area substrates, as illustrated in Figure 2.12. Precursor solution is pumped out through a porous tube (with

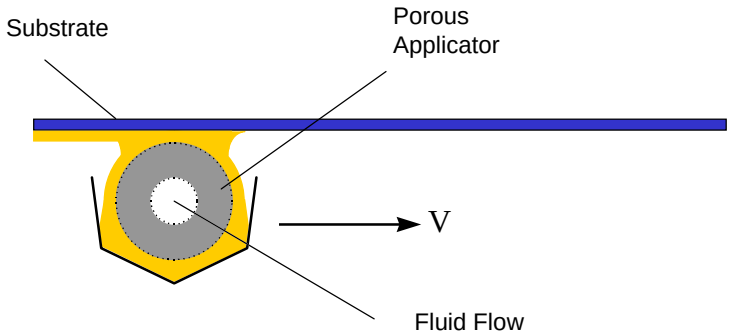


Figure 2.12 Meniscus coating process

10 μm pores) and a gravity-assisted laminar flow of the liquid is established around the periphery of the tube. The substrate is inverted and passes through the upper boundary of the flowing solution, the meniscus of which adheres to the surface of the substrate. Excess fluid that does not adhere to the substrate is collected in a reservoir and recirculated to the coating head. Process parameters include coating head to substrate height, coating velocity, solids content of the precursor solution, and evaporation rate of the carrier solvent. These variables control the coating uniformity and thickness.

2.3.1.3 Spray Coating

This deposition technique passes the substrates to be coated under a spray of polymer precursor solution. A diagram depicting this process is shown in Figure 2.13. Control of deposited film thickness is not as precise as with spin and extrusion coated substrates and some waste of precursor solution must be accepted as part of this processing technique. It is also difficult to deposit thick layers of polymer (> 20 μm). However, the high throughput of this method makes it attractive for the fabrication of passivation layers and stress buffer overcoats for devices in plastic microelectronic packaging.

2.3.1.4 Other Techniques

Recently, newer methods for polymer deposition have been reported as alternatives to standard wet processing techniques involving the use of solvents. One alternative, dry deposition process is molecular beam deposition (MBD) [9]. In this technique, the

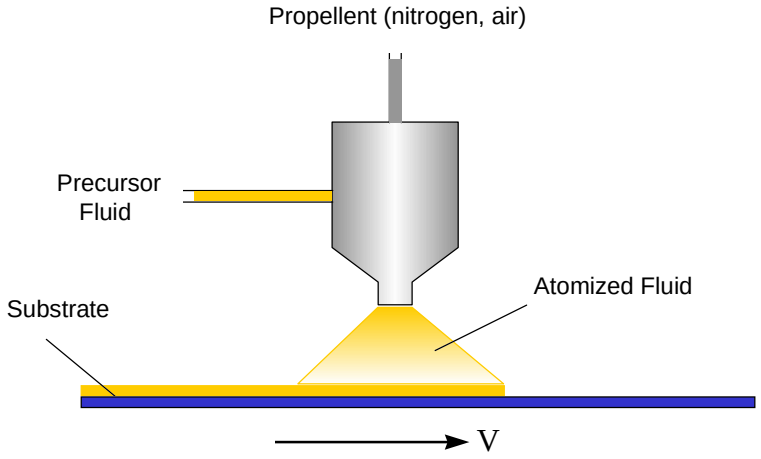


Figure 2.13 Spray coating process

constituent monomers are co-deposited on a substrate using two molecular beams, one for each monomer. The as-deposited films are then heat-treated to produce PI. The elimination of solvents from the film deposition process avoids the PAA-metal reactions that occur during the thermal curing step of the spin coating process. Such reactions lead to the formation of metal oxide particles in PI, which may adversely affect the properties of the polymer. Another significant difference between the MBD process and standard deposition techniques is that MBD films are conforming in nature and do not planarize the substrate pattern.

Another alternative deposition process recently reported is that of chemical vapor deposition (CVD) [10],[11]. Chemical vapor deposition (CVD) is a method of forming thin film coatings using the decomposition of relatively high vapor pressure gases. Gaseous precursors of the polyimide to be deposited are used to transport the materials to the substrate surface where a reaction/deposition process occurs. The deposited precursors are then thermally cured to form the polyimide. Polymer thin films can also be obtained by physical vapor deposition of monomers in the presence of an activating source such as a hot filament or quartz lamps which act as initiators for polymerization [12]. As with MBD, no solvents are involved in the deposition of the polymer and deposited films conform uniformly to the substrate surface.

A dielectric laminate technology has recently been introduced by Gore [6]. The dielectric is a microporous expanded poly-tetrafluoroethylene (ePTFE) matrix with a methyl cyanate ester resin filling the open pore structure. This composition provides a very thin but processable, solvent-free, partially cured dielectric sheet ready for lamination to a substrate. In this process, the dielectric film is laminated to the surfaces of multilayer substrates in large batches. The dielectric film is placed in a vacuum bag on top of a polished metal plate or release. The wafers or substrates are then placed on top of the dielectric and the bag is sealed and placed in an autoclave. During lamination, the resin carried in the ePTFE liquifies and polymerizes as both temperature and time in the autoclave increase. This resin flow fills buried vias and between metal lines while the

surface planarizes to the limits of the polished metal plate. This process requires a solvent-free, addition reaction resin since no volatile escape path is available. A particularly attractive feature of this technology is the ability to laminate very thick (up to 35 μm) copper foils to the dielectric before lamination to the multilayer substrate. For circuits with high current carrying requirements, this feature is especially important. However, the isotropic nature of wet etch processes make the minimum resolvable features for these thick copper foils on the order of twice the film thickness.

2.3.2 Polymer Curing

During the curing of polymer films, three primary processes take place concurrently: the loss of a carrier solvent, the polymerizing reactions, and the release of reaction byproducts. Careful control of process parameters such as temperature and curing atmosphere are critical to the creation of properly cured films.

2.3.2.1 Temperature

Curing of polyimides occurs above 300°C and is accompanied by the evaporation of n-methyl pyrrolidone solvent and the evolution of water with the closing of the imide ring, completing the polymerization. Sufficient cure time must be given to allow generated water vapor to diffuse out of the film and for the chain segments to reorient to a lower stress configuration. Silicon devices are susceptible to damage at these elevated temperatures, as migration of dopants may occur across junctions. Some applications require low temperature processing and several options exist, including BCBs which cure at 250°C, pre-imidized polyimides, and cast dielectric sheets.

2.3.2.2 Oxidation Effects

Most manufacturers recommend curing of their polymeric materials under nitrogen atmosphere to reduce the effect of oxidation on polymer properties. BCBs are inherently more susceptible to oxidation, due to the presence of benzylic and/or aliphatic functionality in the cured films. The use of anti-oxidants increases the stability of the polymer backbone in air at high temperatures. Fluorinated polyimides have also displayed a weakness to oxidation, due to oxygen attacking and cleaving the C-C bonds.

2.3.3 Patterning

There are two traditional methods for patterning polymer films, dry etching and wet processes. A diagram comparing the processing of photoimagable and non-photoimagable polymers is shown in Figure 2.14. The choice of which to use is based on the material properties of the polymer, the desired resolution of etched features, and the

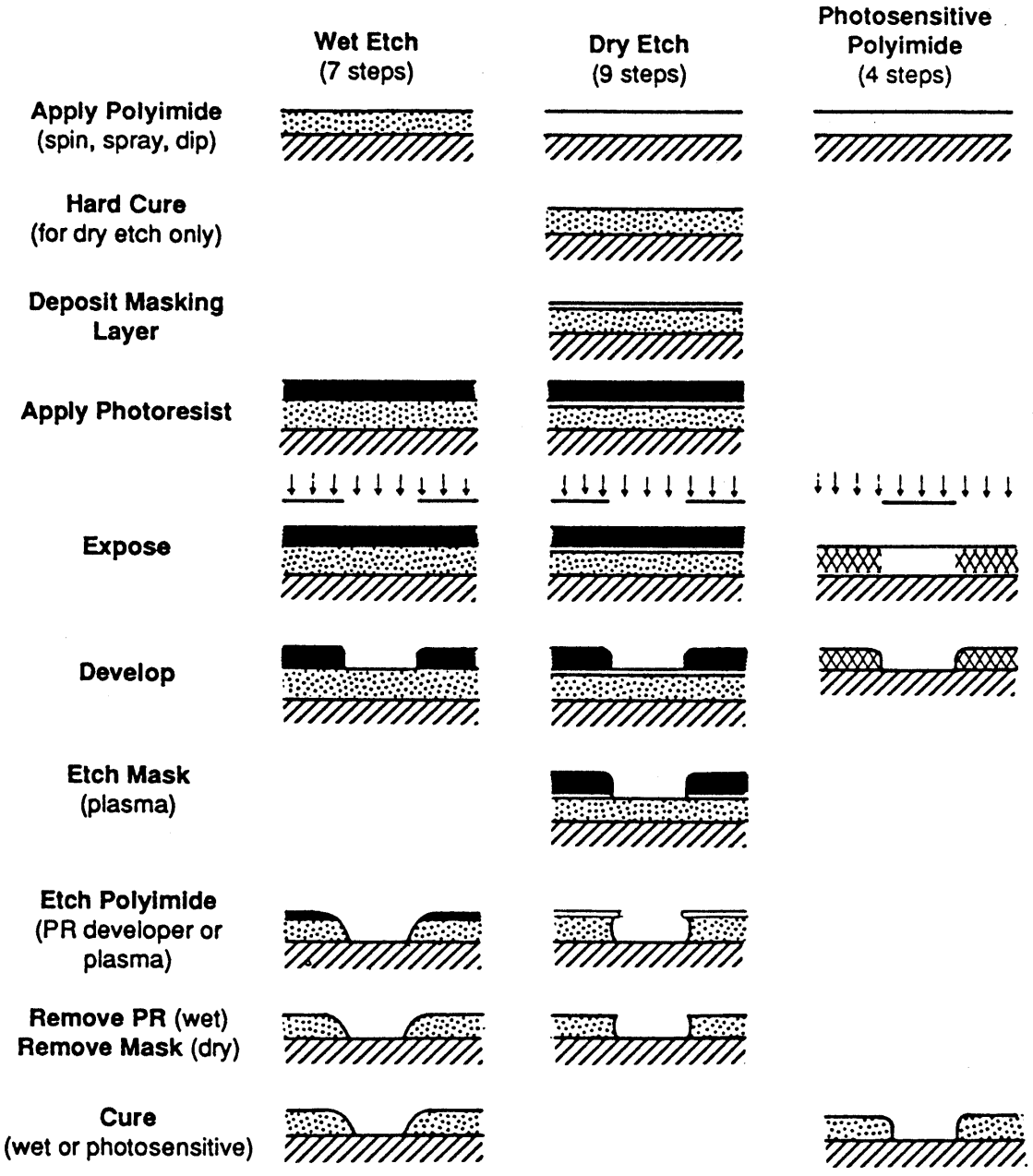


Figure 2.14 Comparison of thin film patterning processes

associated cost of each method. The use of photoimagable polymers eliminates the need for the use of masks during polymer etching, which can significantly reduce the cost and the complexity of a thin film multilayer fabrication process. An alternative approach using laser ablation of thin film layers can be employed for film patterning and has numerous advantages over traditional processing methods.

2.3.3.1 Wet Etching Methods

A key processing advantage provided by polyimides used as interlayer dielectrics is the ability to selectively remove polyimide or precursor polyamic acid by an etching process. Conventional polyamic acids are wet etched with an aqueous base. Both the exposed photoresist (positive resists are activated by exposure to UV) and the polyamic acid are dissolved by the etchant. The etchant functions by forming water soluble salts of the exposed photoresist and the polyamic acid; unexposed photoresist is insoluble and protects the polyamic acid underneath. To complete the process, unexposed photoresist is stripped with an organic solvent. The constituent of polyamic acids primarily responsible for their solubility in the etchant solution is the amic group, which forms a soluble salt in a basic solution. It is known that anything which decreases the concentration of amic acid groups tends to make the polyamic acid less soluble. Thus, non-polar substituents such as the fluorinated rigid cyclic dianhydride 6FDA or the aminophenoxy-biphenyl (APBP) diamine will decrease the polyamic acid solubility in aqueous-type etchants. Many fluorinated polyimides are subject to this effect. The etchants used with standard polyamic acids are based on aqueous solutions of either sodium hydroxide (NaOH) or tetramethylammonium hydroxide (TMAH). These hydroxide-based etchants act by depronating the polyamic acid and forming the sodium or TMAH salt of the polyamic acid as well as giving off water.

2.3.3.2 Dry Etching Methods

Dry etching using an oxygen or oxygen/fluorocarbon plasma can be utilized with standard polyimides. Plasmas can also be employed to roughen the surface of a substrate to promote adhesion of subsequent thin film layers. The final shape, profile, and size of the etched vias and patterns are determined by the masking technique employed and the

plasma properties. Typical plasma etched features have straight walls, creating stress in the surrounding material which can lead to delamination of the polymer film. Relaxing the slope of the feature walls can reduce stress and also facilitates the metallization of vias and improves step metal coverage.

2.3.3.3 Reactive Ion Etching (RIE)

This method of dry etching uses the same principles as plasma etching, but utilizes reactive gases in the plasma such as CF_4. These gases typical contain fluorine or chlorine compounds which significant increase the etch rate of the process. For example, BCBs contain silicon in their polymer backbone, making them difficult to etch using conventional wet or dry etching processes. The use of fluorine-containing RIE plasmas is employed to etch these polymers.

2.3.3.4 Laser Ablation

Laser processing has been shown to be a viable technique for thin film patterning and via formation [13]-[15]. Several key advantages are provided by the use of high energy photons to etch polymer films. Due to the fact that no solvents are needed for polymer processing, it is more environmentally sound than conventional wet-processing techniques. The laser wavelengths are shorter than those provided by standard mercury arc lamps used in conventional lithography, allowing for improved patterning resolution. Additionally, mask undercutting issues associated with wet-chemical and RIE processing are virtually eliminated, and the resulting via wall angles can be tightly controlled to between 30° and 65° by changing the focal plane during the process. Finally, since photons are considered to be “clean” particles and laser irradiation is essentially a non-contact process, ablation can be performed in air instead of in vacuum as in the case of plasma etching or ion milling, reducing the overall microelectronics manufacturing complexity and cost.

The laser ablation patterning process involves four steps: applications of the polymer, using an adhesion promoter if necessary; curing; ablation; and a cleaning treatment for debris removal. Ablative photodecomposition (APD) or the energetic removal of the thin

film material is achieved when the incident light energy density or fluence exceeds a threshold value for the polymer. Above this value, chemical bonds are broken, converting the solid material into a gas of energetic fragments. These fragments are typically deposited as a soot surrounding the ablated region and can be removed by plasma treatment or ultrasonic cleaning [16].

Polymeric materials have distinctive absorption spectra and most, especially polyimides, are particularly absorptive in the UV region. The use of ArF (193 nm), KrF (248 nm), XeCl (308 nm), and XeF (351 nm) excimer lasers is typical, and each has been shown to successfully pattern cured polymer films. For inherently poorly UV absorbing polymers, such as acrylates and PTFE, small quantities of strongly absorbing dopants have been shown to enhance the ablation of these materials [17],[18]. Significant etching will begin as a photochemical reaction (fluences of 10-60 mJ/cm^2), converting to primarily a thermal reaction at higher incident fluences. Ablation rates are a function of the absorption spectrum of the polymer and the incident fluence of the laser. Industrial excimer lasers can generate fluences from 10 to 2000 mJ/cm^2 and produce etch rates ranging from 0.1 to 5 μm per laser pulse. However, at fluences less than 200 mJ/cm^2, debris from the ablation process deposits on top of the polymer and obstructs further incident laser light [15]. Other processing considerations are the size of the beam coverage area, the homogeneity of energy across the beam area, the choice of flooding or scanning a unit cell with the beam, and overlap of successive pulses. Conventional photomasks are incapable of enduring the energy densities required by laser ablation. The special dielectric masks required by this process consist of a high-density fused silica mask blank, similar to those used for conventional photomasks, on which alternating layers of high and low index of refraction films are deposited. Not surprisingly, a similar process is used in the fabrication of laser mirrors. The finished masks are capable of withstanding fluences in excess of 700 mJ/cm^2 and the resulting high stresses encountered during ablation.

An additional application of laser ablation has been the micromachining of polyimide thin film structures [19]. The ability to control etch depths in the polymer films to as little as 50 nm/pulse is a key advantage of a laser ablation patterning process. As a single-step, noncontact process for patterning polymer films, laser ablation is gaining support as an emerging technology in microelectronics and micromechanics.

2.4 Properties of Polymer Dielectrics

The choice of polymer dielectric for a particular electronics packaging application is made based on the inherent physical properties of that material. These properties affect the performance of the package in several key areas: signal speed, power consumption, thermal stability, interaction with other materials, and wiring density. The ease with which polymers can be tailored to display certain electrical, mechanical, and thermal characteristics, and their ease of processing have made them ideal materials for use in electronics packaging.

2.4.1 Electrical Properties

Dielectrics are materials that do not conduct electricity, essentially functioning as insulators, but whose electrical performance must meet more stringent requirements. When exposed to an electric field, the electric charges in a dielectric material, including permanent and induced electric dipoles, can be moved, thus polarizing the material. Although the equilibrium polarization remains a material constant for a given electrical field, it is the dielectric constant, ε or also symbolized by κ, that is used to characterize the dielectric properties of the dielectric. In an alternating (AC) field, the dielectric constant is a complex quantity, ε^*, and is the combination of a real component, called the relative permittivity or dielectric constant, ε', and an imaginary component, called the dielectric loss or dissipation factor, ε''. This form, also called the complex dielectric permittivity, is defined by the following formula:

$$\varepsilon^* = \varepsilon' - j\varepsilon'' \qquad (2.1)$$

A key issue is the variation of both ε' and ε'' with respect to frequency. The measurement of this variation for a photosensitive polyimide was performed as part of this thesis.

2.4.1.1 Dielectric Constant

Dielectric constant (ε') is a critical electrical parameter for a microelectronic polymer dielectric. The magnitude of ε' depends on the amount of mobile (polarizable) electrical charges and the degree of mobility of these charges in the material. Because the charge mobility depends on temperature, ε' is temperature dependent, and since polarization of the material requires a finite amount of time, the frequency of the electric field also influences the measured dielectric constant. The lower the dielectric constant, the faster the signal propagation velocity, as given by:

$$V_p = c/\sqrt{\varepsilon'} \qquad (2.2)$$

where V_p is the velocity of propagation and c is the speed of light. A lower dielectric constant allows for wider signal traces and a decrease in the dielectric thickness. It also allows a designer to maintain the same characteristic impedance while lowering the line resistance and crosstalk. Characteristics of a good dielectric should include invariance of the dielectric constant with respect to frequency and temperature. Polyimides typically have dielectric constants greater than 3.0, unless they are modified through the inclusion of fluorinated groups. It has also been shown that low-stress polyimides exhibit highly anisotropic dielectric constants. Alternative polymer chemistries such as BCBs and fluoropolymers exhibit dielectric constants less than 3.0.

2.4.1.2 Dissipation Factor

Dissipation factor (ε'') and loss tangent ($\varepsilon''/\varepsilon'$ or tan δ) are also important electrical parameters, especially at high frequencies. As the frequency increases, the inertia of the charged particles tends to prevent the particle displacements from keeping in phase with the field changes. This leads to a frictional damping mechanism that causes power loss, because work must be performed to overcome these damping forces. Additionally, ohmic

losses due to free charge carriers are also included in the complex permittivity. It is customary to include the effects of both the damping and the ohmic losses in the imaginary part of the complex permittivity, ε^*:

$$\sigma = \omega\varepsilon'' \tag{2.3}$$

Using Eq. (2.3) we can rewrite Eq. (2.1) as follows:

$$\varepsilon^* = \varepsilon' - j\frac{\sigma}{\omega} \tag{2.4}$$

On the basis of Eq. (2.4) a medium is said to be a good conductor if $\sigma \gg \omega\varepsilon'$ and a good insulator if $\omega\varepsilon' \gg \sigma$. Thus, a material may be a good conductor at low frequencies, but may have the properties of a lossy dielectric at very high frequencies. In contrast, most dielectrics, including ceramics and polymers, exhibit low loss at low frequencies, but become lossy at high frequencies. In low-loss media, damping losses are very small, and the real part of ε^* in Eq. (2.4) is usually written as ε without a prime.

Low values are indicative of minimal conversions of electrical energy to heat and little overall power loss. Thus, multilayer power circuits require thin film materials that exhibit low values for dissipation factor. For example, BCBs have attractive values for ε'', typically around 0.0008, while polyimides have values near 0.002. By comparison, ceramic materials such as alumina have values for ε'' of approximately 0.0001-0.0004 (depending on purity) at 1 MHz, with little variation in their values with frequency.

2.4.1.3 Dielectric Strength

Dielectric strength or breakdown voltage define the voltage at which current begins to flow through the insulating dielectric film. For thin films, avalanche breakdown ultimately determines the breakdown strength of the polymer. Breakdown can also occur due to thermal effects as power is dissipated by the insulation, in which an exponential increase in conductivity creates thermal runaway. Most polymeric materials exhibit

values for breakdown voltage of about 10^6 V/cm. BCBs have slightly higher values, making them attractive in high voltage power applications.

2.4.2 Physical Properties

High thermal stability polymers are the most frequently used dielectric materials for TFML interconnections, although silicon oxides have been shown to provide similar performance. Polymers are attractive in general because of their attractive electrical properties, as previously discussed, ease of processing, such as deposition and patterning, and their relative stability in the presence of chemical attack and extremes of temperature and humidity. Polyimides, in particular, are generally stable above 400°C, mechanically tough and flexible, and unaffected by process solvents and chemicals. Additionally, the dielectric should planarize the interconnect topology, have a CTE closely matched with the substrate, and be able to be applied in thick layers (up to 25 μm) with low stress and no cracks or pinholes.

2.4.2.1 Water Absorption

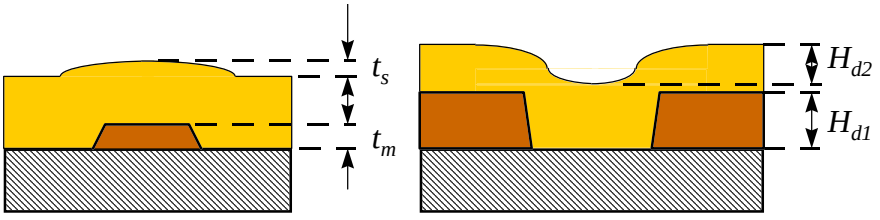
Water absorption impacts both the electrical properties and the processibility of dielectrics for multilayer circuits. The quantity usually measured is the maximum amount of water uptake, which depends upon the degree of cure, on temperature, and on relative humidity. These parameters must be given in order to provide an accurate comparison between candidate materials. Absorption of water, with a dielectric constant of about 78, raises the bulk dielectric constant of a polymer film and thus will affect circuit performance. Absorbed moisture can also cause severe damage to structures during the fabrication process. Uncontrolled outgassing of moisture from underlying layers of dielectric during subsequent high-temperature processing can result in blistering and delamination of the thin film structures being fabricated. Also, corrosion of sensitive metal interconnect structures has been reported due to excess moisture present in insulating polymer films [20]. Bakeout cycles are employed during the fabrication of multilayer thin film circuits with polymers that exhibit significant moisture absorption. Gridded ground and signal planes can be utilized to allow evolved moisture to escape from the multilayer structure, minimizing damage. Polyimides, in particular, have a

strong tendency for moisture uptake (>1.0%), but many alternative chemistries are available which directly combat this effect.

The dielectric constant of a PMDA/ODA-based polyimide increases linearly from 3.1 at 0% relative humidity to 4.1 at 100% relative humidity [21]. Other experiments have shown that the dielectric constant of a polyimide exposed to water in a heated pressure cooker increased from 3.1 to >3.5 after 25 hrs. This absorbed moisture was subsequently released after heating at 200°C for 17 hrs in air [22]. Electrical design tolerances must be able to accommodate these variations in electrical performance to maintain proper functionality of the circuit. Otherwise, the MCM must be hermetically sealed to prevent moisture from reaching the thin film, multilayer structure.

2.4.2.2 Planarization

The surface roughness of a substrate surface, either due to existing interconnect structures or the polymer deposition process, can directly affect the resolution and quality of subsequent thin film layers. Planarity of the multilayer structure must be assured if electrical properties are to be uniform across the entire substrate. One of the main functions of the dielectric layer is to planarize the underlying topography and, thus, provide a flat focal plane for the next layer. Any variation in surface smoothness can lead to poor metal step coverage, poor adhesion, thinned or weakened areas susceptible to cracking, and nonuniform electrical properties. The degree of planarization (DOP) of a polymer dielectric is given as the ratio of the step height of the dielectric covering a feature to the feature height, as depicted in Figure 2.15. The DOP for a given dielectric is



$$D.O.P = 1 - \frac{t_s}{t_m} \qquad D.O.P = 1 - \frac{H_{d2}}{H_{d1}}$$

Figure 2.15 Planarization of an isolated feature

the result of both the solids content of the polymer precursor and the shrinkage of the polymer during curing. Polymers, such as BCBs, which exhibit low shrinkage during cure have a DOP greater than 90%. Polyimides, by nature of their polymerization process, shrink up to 50% during cure, and thus exhibit a DOP of less than 30%.

2.4.2.3 Chemical Resistance

Polymer dielectrics must be resistant to the processing and cleaning chemicals used in the fabrication of the structures. The usual manifestation of poor chemical resistance is swelling, cracking, or crazing of the polymer layer. Thermosetting polymers are generally much more chemically resistant than thermoplastic materials.

2.4.2.4 Polymer/Metal Interactions

It has been proposed that the polyamic acids dissolve interfacial copper, forming Cu salts that migrate into the polymer matrix and redeposit as copper oxide upon thermal curing. Additionally, polyimides contaminated by copper can be difficult to remove using RIE processing, resulting in the formation of high resistance interconnects. Diffusion of Cu into polyimide can reportedly be blocked by chromium or titanium barrier layers.

2.4.2.4.1 Copper

The formation of oxides during the curing of polyimides deposited on copper interconnect structures and their effect on adhesion strength has been well characterized [23],[24]. Efforts to block this oxidation have focused on metal barrier layers between the copper and the polyimide comprised of titanium and chromium [25]. Adhesion of the chromium barrier layer to the polyimide can be enhanced through plasma roughening of the polyimide [26].

2.4.2.4.2 Aluminum

Aluminum has been proposed as an alternative, low-cost interconnect metal for multilayer thin film circuits. It is commonly used in IC processing, but under high current densities, there is an increased risk of electromigration failure at the connection between the aluminum line and the tungsten plug or via. This is a result of aluminum having an electromigration activation energy half that of copper. Its coefficient of thermal

expansion (CTE) and resistivity are also larger than copper, resulting in higher thermal stresses and degraded electrical performance, respectively. Research into the interaction between aluminum and polyimides has shown that little, if any, interaction occurs due to the passivating effect of the aluminum oxide [23].

2.4.2.5 Interlayer Adhesion

Adhesion of polymer interlayers in a thin film structure are strongly related to other issues such as water absorption and stress since temperature and humidity are known to severely degrade adhesion. The manifestation of adhesive failure in interlayer dielectrics is delamination of the layer from adjoining layers. Tests of polymer adhesion typically involve the use of adhesive tape or studs which offer a quantitative means of comparing the adhesion of different dielectric materials to particular interfaces. Polymer adhesion is needed at four interfaces: polymer to substrate, polymer to metal interconnect, metal to polymer, and polymer to polymer. Film adhesion is very sensitive to surface preparation. Removal of oxides and particulate contamination by cleaning is critical to ensuring adequate adhesion of deposited layers.

2.4.2.5.1 Adhesion to Metals

The adhesion of polymers to interconnect metals such as copper is influenced by any chemical interactions between the layers and their respective mechanical properties. Copper and polyimides have been shown to interact strongly, with the formation of copper oxides during polyimide curing. The use of titanium and chromium barrier layers has proven to be effective in improving interlayer adhesion as well as blocking the migration of copper into the polyimide. The relatively low values of modulus exhibited by most polymers make interconnection stress a minor issue. However, differences in coefficients of thermal expansion values for polymers and metals are a matter of concern from a reliability standpoint.

2.4.2.5.2 Adhesion to Substrates

Surface roughening of the SiO_2 or alumina substrate or the use of adhesion promoters has been shown to significantly increase the adhesive strength of polymer dielectrics to

multilayer substrates. Adhesion to previously deposited polymer layers can be enhanced by performing a soft-bake between concurrent polymer depositions and co-curing the enitre polymer stack simultaneously. This technique can be problematic for the case of polyimides, due to the evolution of water and other products from the imidization reaction, resulting in blistering and delamination of inner polymer layers. BCBs, on the other hand, evolve no by-products as a result of curing and this technique can be used successfully to build up thicker layers of dielectric.

2.4.2.5.3 Surface Treatment

Surface treatment by plasma or ion beam techniques or by "adhesion promoters" is used to induce better adhesion. Back-sputtering was originally believed to roughen the surface of the substrate, but actually increases the surface free energy. Adhesion promoters are formulated to chemically react with both the substrate and the deposited film. Polyimide adhesion promoters are usually amino silanes while BCBs require amino silanes or triethoxyvinylsilane.

2.4.3 Mechanical Properties

The mechanical properties of a polymer describe how the polymer responds to stresses imposed upon it. Although there are many measures of mechanical performance, the properties reported for thin film polymer dielectrics usually include tensile strength (maximum tensile stress that a material can withstand before irreversible yielding), tensile and flexural modulus (the ratio of tensile or flexural stress to strain), and the elongation or strain at break (the amount the film yields before it ruptures).

2.4.3.1 Glass Transition Temperature

The glass transition temperature (T_g) of a polymer is the temperature at which the material exhibits permanent deformation in response to an external load. Thermosetting polymers behave like cross-linked rubber above their known T_g value and deform, but do not flow. If subsequent processing is to occur above the polymer's T_g, the mechanical integrity of the structure may be compromised as a direct result.

2.4.3.2 Coefficient of Thermal Expansion (CTE)

The coefficient of thermal expansion (CTE) of a polymer dielectric is important because of its relationship to the thermal stress generated in a multilayer structure. Most polymer dielectrics exhibit CTEs an order of magnitude larger than the silicon devices attached to the multilayer structure. Low-stress polyimides have been developed to reduce the stresses caused by CTE mismatch, but their CTEs are highly anisotropic in nature. They exhibit a large z-axis value for CTE which negatively impacts the shear stress in the multilayer structure.

2.4.3.3 Flexural Modulus

Flexural modulus is the ratio of tensile or flexural stress to strain. Polymers can be divided into four different classes based on their mechanical performance. Soft, weak polymers have low moduli and low elongations. Hard and brittle polymers have high moduli and low strain at break. Hard and strong polymers have high moduli and moderate strain at break. In contrast, hard and tough polymers have high moduli and high strain at break.

2.4.3.4 Thermal Stability

A material is thermally stable at a given temperature when its properties do not change at that temperature. Thermal stability for a interlayer dielectric needs to be in excess of the temperatures to be encountered during subsequent processing steps of fabrication of the multilayer structure. Typical examples of high temperature process steps include die attach and reflow soldering which can require temperatures up to 350°C. Thermal stability is best determined from isothermal thermogravametric analysis (TGA) on polymer dielectric thicknesses similar to those used to fabricate the multilayer structures. Isothermal data are required since thermal degradation is limited by solid-state diffusion and therefore is thickness dependent. Standard polyimides exhibit high thermal stability and are stable in air up to 400°C. BCBs and fluorinated polyimides exhibit lower stability and undergo weight loss when exposed to temperatures above 300°C.

2.5 Thin Film Multilayer (TFML) Interconnections for Multchip Modules (MCM)

Traditionally, the development of organic dielectric materials for use in electronic packaging has focused on high density, thin film multilayer structures (TFML), where multiple, unpackaged IC devices are attached to and interconnected by the TFML substrate. The need for multichip packaging arises because of the inability to obtain the entire function on a single, large silicon device or on a wafer-scale integration (WSI) substrate at the time it is required. Semiconductor integration doubles approximately every year and a half and, given enough time, semiconductor technology will eventually provide a solution, but at increased cost and complexity. Multichip packaging can provide an immediate solution utilizing less complex devices, lowering costs and development times and in a package only slightly larger than a fully integrated solution.

Multichip packaging is widely regarded as the most intensive activity in the electronics packaging community, with research being conducted at all levels in industry, from integrated circuit fabricators and vendors to universities and professional societies. While initial efforts were focused on providing high-performance computing solutions, especially for mainframe and supercomputer applications, the market for multichip technology has more recently expanded into the areas of automotive and consumer electronics, aerospace, and telecommunications.

2.5.1 MCM-Deposited (MCM-D)

As mentioned previously, the use of organic dielectric materials for MCM packaging has focused on thin film multilayer structures, where alternating layers of metal and dielectric are deposited and patterned to provide the interconnect structure for bare IC devices attached to the TFML substrate. This method for multichip packaging is known as MCM-D and uses fabrication techniques that closely mirror those developed for the semiconductor industry. However, the semiconductor processing equipment used to manufacturer MCM-D substrates is expensive and low volume runs make it difficult to depreciate the high capital costs. Thus, MCM-D techniques tend to provide the highest possible performance, but at an associated cost making them unattractive for high volume, low-cost products.

In terms of absolute electrical performance, deposited MCM or MCM-D has been the technology of choice, especially in the area of high-performance computing, which has been a leader in the implementation of MCM for electronics packaging. MCM-D packages have an interconnection structure comprised of alternating thin film layers of deposited metals and polymers on an underlying substrate, typically ceramic or metal. This process is depicted in Figure 2.16. Since the thin films used in MCM-D may be easily patterned with relatively high resolution lithographic techniques, wiring densities are extremely high, and do not significantly effect the overall package size.

A major benefit of MCM packaging is the wiring efficiencies achievable, especially when bare silicon die are used to populate the substrate. The bare devices are attached to the

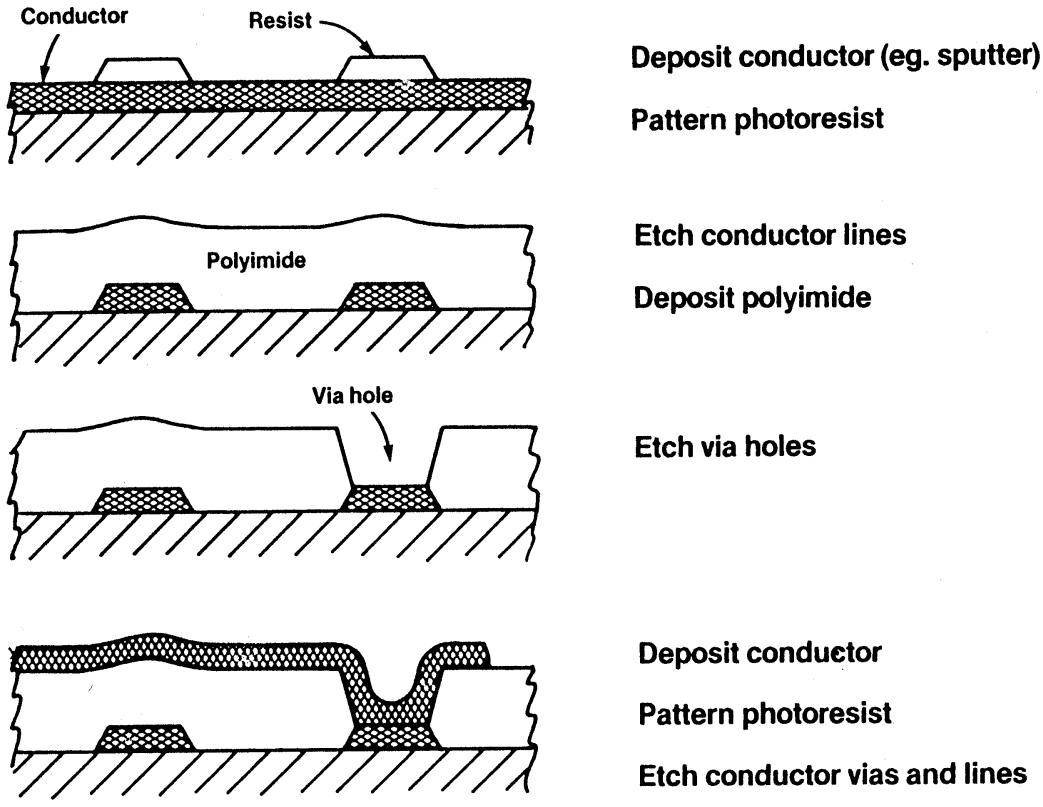


Figure 2.16 Thin film interconnection process

substrate using interconnect methods including wire bonding, tape automated bonding (TAB), or flip chip. Each of these techniques attempts to provide the closest spacing (lowest pitch) possible between devices on the substrate. In this approach, the size of the MCM package is dictated by the size of the devices attached to the substrate and the number of I/O required for each chip. This results in a package of minimum size and maximum electrical performance.

2.5.2 MCM Substrates

The key functions provided by multichip packaging are interconnecting, powering, cooling, and protecting the bare semiconductor devices. In contrast to a traditional single chip package, which connects a bare chip to a single plastic, ceramic, or metal carrier substrate, the multichip package provides the same functions with more than one bare chip on a single, common carrier.

MCM substrates are manufactured from a wide variety of materials, including ceramics, organic laminates, and metals. It is important to note, however, that few MCM substrate manufacturers perform the assembly of bare devices to the multichip substrate. This difficult and costly process is typical left to the end-user of the MCM to complete. As a result, much effort has been spent on developing techniques for the direct attachment of bare-die or chip-scale packages to low cost laminate or printed wiring board substrates, such as flip chip and chip scale packaging (CSP). Still, the benefits of multichip packaging can be realized, although not as completely as in direct bare-die attachment, by attaching prepackaged devices to the multichip substrate.

This substrate may be ceramic (MCM-C), printed wiring board or laminate (MCM-L), or, thin films deposited on a supporting substrate (MCM-D). Possible substrate options include metals, such as silicon, copper, and aluminum; ceramics, such as aluminum nitride (AlN), diamond, and alumina (Al_2O_3); and organics, such as polyimide-glass or organic/inorganic laminates. The choice of substrate is critical, since the thin film structure typically has poor thermal performance, requiring heat generated by the operating circuits to be dissipated by the underlying substrate.

2.5.2.1 Thin Film Metallization

The deposition of the thin film metal layers for MCM-D is accomplished either by evaporation, sputtering, or electroplating techniques, depending on the metal being deposited. In general, sputtering and evaporation are used for aluminum and electroplating is used for copper and gold. The precise nature of the thin vacuum deposition techniques, sputtering and evaporation, make them difficult to automate, adding additional cost to MCM fabrication. Patterning of the deposited metal is typically subtractive and is performed using wet-chemical processes.

2.5.2.1.1 Evaporation

Metal deposition by evaporation involves the thermal heating of the metal in a vacuum and subsequent condensation of the metal onto a substrate. Conventional thermal evaporation is a relatively low-energy process, resulting in a weak molecular interaction between the colliding metal atoms and the substrate. This results in typically poor adhesion for evaporated films. Since the film is deposited with the metal moving in a direct line from the source to the substrate, features with steep walls or sides are not evenly coated. This is advantageous for lift-off processing, where patterned metal films can be deposited as an additive process. The thickness of the deposited film can be controlled to within several Å, and uniformity across a substrate is highly consistent.

2.5.2.1.2 Sputtering

The sputtering process involves bombardment of a metal target source by energetic particles, typically Ar^+ in a plasma. Metal atoms are dislodged from the target and deposited onto an adjacent substrate. Due to the increased energy imparted to sputtered metal atoms, as opposed to evaporated metal, the adhesion of sputtered films is typically much better. However, undesirable substrate heating is a common problem, but can be controlled by the use of DC magnetrons to confine electrons in the plasma. Sputtering deposition rates are much lower than those for evaporation and source utilization can be irregular due to uneven flux distribution.

Sputtered metal atoms are knocked free from the source surface is essentially random directions, resulting in a conformal deposited film, with good step coverage of features. Uniformity of the sputtered film is directly related to the relative sizes of the source and substrate and the throat distance between them. Very large substrates are typically difficult to sputter coat with uniform films. Contamination of the substrate surface can degrade adhesion and can be removed by ion milling or RF sputtering. These processes ablate several hundred Å of the substrate surface prior to deposition, removing organic contaminants and may also improve adhesion through surface roughening or an increase in the surface energy of the substrate.

2.5.2.1.3 Electroplating

Electroplating involves the selective deposition of ions from a plating solution. An electrical potential is applied to a previously deposited conductive seed layer to initiate the electrochemical reaction. The substrate acts as the anode, and metal ions are reduced and deposited on exposed regions of the seed layer, typically through a patterned photoresist. This process requires additional steps to remove the seed layer after electroplating, which can be a disadvantage.

Electroplating process are dynamic in nature and therefore required tight process control to achieve accurate and consistent results. The main advantage of electroplating is its inherently high deposition rate, typically > 1 μm/min. Since electroplating is an additive process, high aspect ratio wiring features can be achieved, because feature tolerance is determined by the photoresist lithography tolerance. Uniformity over a substrate surface is much more difficult to control than for sputtering and evaporation, however.

Unlike electroplating, electroless plating does not require a continuous seed layer held at a specified voltage or current. The metal is built up by selective deposition onto a catalytic seed layer by the reduction of metallic ions in an aqueous solution. Electroless plating solutions are available for Cu, Au, and Ni, and are the plating reaction typically requires a solution pH in the range of 11.5 - 13 at a temperature between 40 and 70°C.

Because polyimides are not chemically stable in such highly alkaline solutions, bulk stability and interface problems are common.

2.5.3 Applications of Thin Film Polymer Dielectrics for Electronics Packaging

Because of its higher electrical performance, reduced space and weight, and improved reliability over single-chip packages, multichip packaging has been utilized in a broad spectrum of applications. The most predominant market for MCMs has and is expected to be in advanced computing equipment, such as mainframes, supercomputers, avionics, and spaceborne electronics. For these applications, MCM-D technology is the preferred method, achieving the highest performance in the smallest space possible. The spread of MCM technology into other markets has been slow, however, due to its increased cost and competition from traditional packaging methods. As a result, it is expected that most of the efforts in the research and development of new polymer materials for electronics packaging will focus on high-growth, high-volume markets.

Another market for polymer dielectrics which has grown considerably in recent years has been in the area of thin film stress buffer coatings for large-die devices packaged in epoxy molding compounds. Applying a relatively thick layer of polyimide over the die passivation layer reduces stress caused by the CTE mismatch between the die and the epoxy, and protects the die from the coarse composition of the molding compound. Other emerging markets for polymer dielectrics include flat-panel display materials, sensor materials, and as optical waveguides in backplanes for high-speed, fiber optic switching equipment.

2.6 Conclusions

The impetus for much of the advances in interconnect technology and microelectronics packaging has resulted from a need for improved performance, especially in terms of shorter signal paths, lower capacitive load, reduced circuit noise, and increased circuit density. These attributes were needed in order to take advantage of the huge strides being made in VLSI device speed and density, which were not being realized at the system level using conventional packaging. Multichip modules (MCMs) have features that enable

smaller, lighter systems and higher speed performance to be obtained by eliminating individual packages and their parasitics. Among currently available electronic packaging technologies, MCMs are the most efficient, providing the most electrical performance in the least space.

The performance enhancements seen from this technology come in part from the thin film polymeric dielectrics that are used in their fabrication. Polymers are attractive because of their inherently low dielectric constant, enabling high speed circuitry, and ease of processing. Polymer performance is based on the complex interrelationship between such properties as adhesion, stress, moisture absorption, and thermal and chemical properties of the polymer. The suitability of a specific polymer is highly dependent on the process chosen to fabricate the structure and the intended application of the electronic package.

Chapter 3 – Methods and Materials

3.1 Introduction

The creation of thin film multilayer structures involves a number of specialized processing techniques including RF sputtering of metals, spin-coating of polymer photoresists and polyamic acid precursors, photo-lithographic patterning, and wet-chemical etching of exposed films. Understanding the vagaries and demands of each process is critical if high yields of successful devices is desired.

This chapter describes the techniques, equipment, and processing steps developed to successfully fabricate thin film capacitor structures on ceramic substrates, and mount them into carriers for testing.

3.2 Thin Film Capacitor Design Considerations

The simplest capacitor structure which can be achieved using thin film techniques is the planar form, consisting of a layer of dielectric material sandwiched between two metal layers. Neglecting fringing effects, the capacitance for this structure can be calculated using the following equation:

$$c = \frac{\varepsilon_o \cdot \varepsilon_r \cdot A}{t} \qquad (3.1)$$

In this formula, A represents the area of the smaller metal conductor layer, t is the thickness of the dielectric, and ε_o and ε_r are the permitivity of free space and the relative permitivity of the dielectric, respectively.

Since polymer dielectrics have dielectric constants on the order of 3 or 4, structures made using these materials will have correspondingly low capacitances. However, we desire to make capacitor devices with the highest value possible, to reduce the amount of error introduced during measurements of the complex impedance. We can see from the

equation above that the two variables available for varying the capacitance are the area of the capacitor and the dielectric thickness.

We can decrease the thickness of the dielectric to increase the capacitor's value, but we must not make it so thin that breakdown voltages are undesirably small. Increasing the area of the capacitor can also increase the capacitor's value, but the error in measurements made on large area capacitors increases exponentially as the frequency of measurement increases. Previous research performed at Virginia Tech showed that for frequencies above 1 MHz, capacitor structures larger than 200 mils square displayed unacceptable measurement errors, due to resonance and fringing effects at higher frequencies [27]. For the purposes of the research presented in this thesis, the capacitor area was chosen to be 200 mils square.

Forming polymer films using spin-coating techniques and polyamic acid precursor solutions is common in the electronics packaging industry. Most films deposited using this method are in the 5 to 15 micron range in thickness, with thinner layers being more difficult to achieve, due to the high molecular weight oligimers used in the precursor solutions, to ensure good planarity and coverage across the substrate. A target thickness of 7 microns was set for the capacitor structures fabricated for this thesis, which is well within the processing thresholds of the polymer materials used.

The substrate material chosen for this thesis was high purity alumina manufactured by Coors Porcelain, which is 99.5% Al_2O_3. These substrates are 2 inches square by 0.025 inches thick and have one side which is highly polished, ensuring good planarity and adhesion. Alumina is a common substrate material for high power circuits, due to its low cost, relatively high thermal conductivity, low coefficient of thermal expansion, and insulating properties. Since alumina is a ceramic, it is not easily processed, and must either be cast into specific shapes or can be machined using lasers or diamond-tipped tools once cast.

The choice of metals used in the capacitor structure was influenced by the processing steps required to fabricate a capacitor which adheres well to the substrate, is patterned easily, and can be wire-bonded. Additionally, the metal should not exhibit influence high resistivity, since this would introduce errors that would change the impedance measurements significantly. Based on these criteria, a dual metal system consisting of copper and nickel was chosen. Copper exhibits very high conductivity, is easily processed, and can be deposited with relative ease. The inclusion of nickel is necessary, however, to allow wire-bonding to the metal layers of the capacitor. Thin layers of nickel can also be processed simultaneously with the copper, reducing the complexity of processing steps required. Four substrates using the final mask set were fabricated using only sputtered copper. An attempt was made to plate the top metal layer of the capacitors with nickel using a chemical plating solution. This process was found to produce unsatisfactory results as two of the substrates were damaged by the strongly acidic plating solution. The remaining two substrates were reserved for testing as fabricated. All subsequent substrates were dually sputtered, first with copper, then with nickel to form a surface compatible with wirebonding.

A preliminary mask set was generated to evaluate the thin film processing steps which were being developed for the fabrication of the capacitor structures. The set consisted of two metal layer masks and a dielectric layer mask, with via structures incorporated to test the multilevel wiring capabilities of the thin film processes. These are shown in Figure 3.1. The masks were prepared using AutoCAD software on a PC, and plotted on rubylith material using a diamond stylus at a 10:1 enlargement scale. The rubylith was affixed to a light box, and the mask images were transferred to photographic film, at a 1:10 reduction scale. To enable the use of a mask aligner combined with a high-intensity mercury vapor ultraviolet (UV) exposure unit, glass masks had to be fabricated from the film masks. The glass masks used in photolithography are typically glass, coated with iron oxide and coated with photoresist for ease of processing. Iron oxide is transparent to visible light, but opaque to UV wavelengths, which facilitates alignment of the mask pattern to the substrate. Unfortunately, the mask aligner only accepts 3 inch square

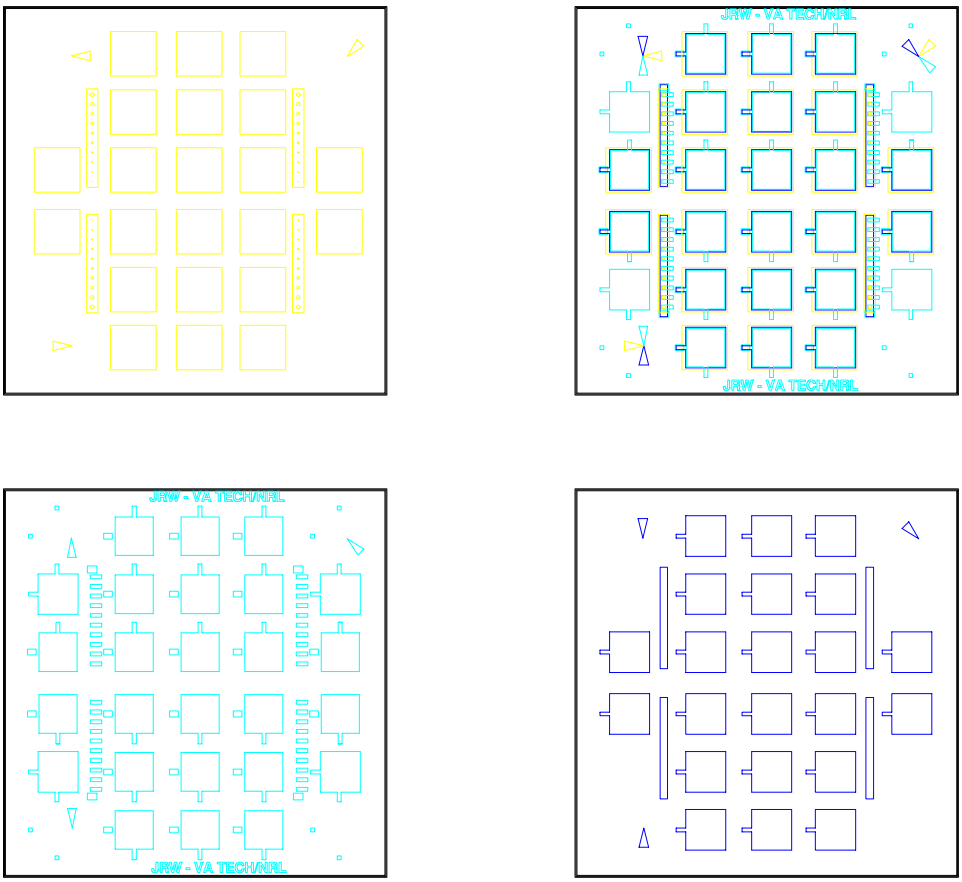


Figure 3.1 Mask set for prototype capacitor structures

plates, and 6 inch plates were the only supplies readily available. An attempt was made to scribe and cut the larger plates to allow their use in the mask aligner, but the thicker glass used in the larger plates made this difficult. For the remaining substrates, the plastic film masks were found to be adequate, since the resolutions required for the structures being fabricated were quite large.

After the initial set of substrates were fabricated, it was determined that a common carrier should be used to allow for the quick exchange of substrates during testing. The use of a closed environmental chamber requires a common test fixture which can provide connectivity from the capacitor devices under test to measurement equipment outside the chamber.

The simplest carrier is a leaded metal box, which allows the substrates to be affixed to the inside, with wirebonds from pads on the substrate to posts on the legs of the carrier. The carrier can then be inserted into sockets on a printed circuit board (PCB), which fans the signals out to connectors on its edges. Cables can then be run from these connectors, through a hole in the chamber wall, to the external measurement equipment. A number of metal (Kovar) carriers were identified as having enough I/O leads (18) to support an adequate number of test structures per substrate. The dimensions of the carrier (1 inch square) required a redesign of the initial mask set, to allow for the fabrication of four fully populated coupons and two partially populated coupons. The redesigned mask set is depicted in Figure 3.2. The fully populated coupons consists of four capacitor structures, an open circuit structure, and a short circuit structure. The latter two structures were required to reduce errors in the impedance measurements, which will be discussed more

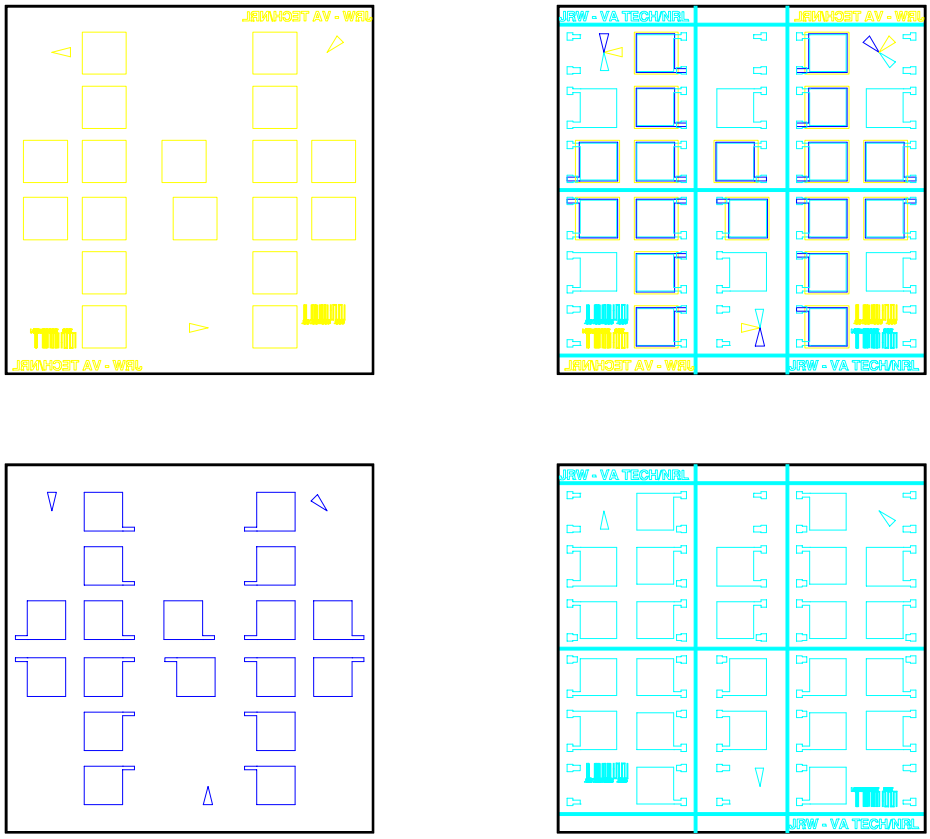


Figure 3.2 Final mask set for capacitor structures

thoroughly in Chapter 4. A partially populated coupon has both the short and open circuit structures, but only one capacitor.

Once a substrate is fully processed, it can be diced using a diamond saw to separate the individual test coupons. Ultimately, eight substrates were fabricated and diced into 32 fully populated and 16 partially populated coupons. Four of these coupons, each from different substrates, were assembled with carriers and tested in the environmental chamber.

3.3 Thin Film Metal Deposition

The deposition of thin film metals is typically performed using either evaporation or RF sputtering techniques. Since evaporation is a relatively low energy process, it does not produce adequate adhesion to ceramic substrates and was not used in the fabrication of the test coupons. Additionally, the diffusion pump used to form a vacuum in the evaporation chamber produces a hydrocarbon mist, which can contaminate the substrates and the deposited metal film. In contrast to these drawbacks, RF sputtering produces extremely pure films with excellent adhesion to most substrates, including ceramics such as alumina, but at the cost of lower deposition rates.

When the work for this thesis was begun, The Microelectronics Lab had no working sputtering chambers available, as they had been recently moved and had not been reassembled in their new location. To maintain as high a degree of cleanliness as possible, the chambers were relocated to a movable Class 1000 clean area. The author was responsible for reestablishing connectivity to water, electricity, exhaust ducting, and gas feeds for the chambers inside the clean room. Additional modifications to the existing systems were also made to improve their reliability and the quality of the sputtered films. The work involved took most of one academic semester and was completed at a significant cost to the Lab.

Both chambers use standard rough pumps to achieve vacuums on the order of 10^{-3} Torr, and molecular turbopumps to reach vacuums of $< 10^{-6}$ Torr. These pressures are

necessary to ensure that almost all atmospheric gases are eliminated from the chamber during deposition, which reduces the possibility of contamination. RF sputtering guns provide the energy necessary to free metal atoms from the surface of the target and deposit themselves on the substrates surface. Because previous research performed using these chambers had involved the use of exotic superconducting compounds, each gun was disassembled and cleaned to remove as much of these residues as possible. New water cooling feed tubes and RF cables were assembled and attached to each gun. All of the rubber o-ring seals used in the chambers were disassembled, cleaned, inspected, and reassembled. To prevent oil mist from the rough pumps from contaminating the chamber, and to facilitate the venting of the chamber after deposition, two high-vacuum valves and a filter maze were installed between the rough pump and turbopump on each chamber. Water pressure switches were also installed, which prevent the use of the RF power supplies without adequate water flow through the sputtering guns. The smaller of the two chambers can accept substrates approximately 1.5 inches square, while the larger chamber has a 4 inch square substrate holder , although the access port is 6 inches in diameter.

An optimized sputtering process was developed which consists of the following steps:

1. Clean substrates to remove contaminants.
2. Insert desired target into sputtering gun.
3. Screw center electrode into gun.
4. Attach substrate(s) to substrate holder.
5. Insert substrate holder into chamber and affix using clamps.
6. Close chamber vent port if not already closed.
7. Insert gun into chamber and hold.
8. Open vacuum valve and release gun when vacuum holds.
9. Attach and tighten clamps for substrate holder and gun.
10. Turn on PDR-C-1C, 252A, and 247C (in that order).
11. When PDR-C-1C reads < 40 mTorr, start turbopump.

12. Allow turbopump to run for at least 6 hours (overnight)
13. Turn on 290 controller. "DEGAS" for 15-20 sec.
14. Chamber is sufficiently evacuated at < 3.0 x 10^{-6} Torr.
15. Turn off 290 controller.
16. Start argon and water flow.
17. Adjust zero calibration on PDR-C-1C and 247C.
18. Close butterfly valve to 70% open using 252A.
19. Turn on RF power supply. Adjust to 60 W.
20. Turn on gas flow though mass flow controller using 247C. Wait until flow stabilizes at 10 SCCM.
21. Turn on RF output.
22. Slowly open argon inlet valve to chamber.
23. Bring chamber pressure up to ~30 mTorr, until plasma lights.
24. Once plasma has lit, maintain pressure < 30 mTorr until valve is fully open.
25. Switch 252A to S.S. (Soft Start) position. Wait until pressure stabilizes at 3.5 mTorr.
26. Switch 252A to Auto position.
27. Record sputtering start time on chamber data sheet.
28. Once sputtering time has expired, turn off RF output.
29. Record sputtering stop time on chamber data sheet.
30. Wait at least 30 min for gun to cool.
31. Turn off RF power supply. Turn off water flow.
32. Switch 252A to Open and open valve completely.
33. Turn off gas flow channel on 247C. Close argon inlet valve.
34. Wait for pressure in chamber to reach ~0 mTorr.
35. Toggle stop switch on turbopump controller.
36. Allow at least 1 hour for turbopump to spool down.
37. Close chamber vacuum valve.
38. Remove clamps from substrate holder.
39. Open chamber vent port and support substrate holder.
40. When vacuum has dissipated, holder will be released.

41. Remove holder from chamber.
42. Remove substrate from holder.

The deposition rates typically achieved for copper and nickel were approximately 1 micron of deposited metal for every four hours of sputtering. Other metals such as chromium and Nichrome™ have also been deposited using these sputtering systems.

3.4 Thin Film Metal Patterning

Patterning of the sputtered thin film metals defined the upper and lower metal layers of the capacitor structure and provided pads for wirebonding to these layers. A photolithographic process was used to define the metal patterns and is depicted in Figure 3.3. In this process, a thin layer of photosensitive polymer or photoresist is deposited on top of the metal to be patterned. The deposition of the photoresist is typically performed using a liquid solution which is dispensed onto the substrate surface, which is then spun rapidly to evenly spread the solution across the substrate. The photoresist used for this research was Shipley 1350J, which is a red, negative-acting photopolymer. The thickness of the deposited film is a function of the spin speed and directly affects the line resolution

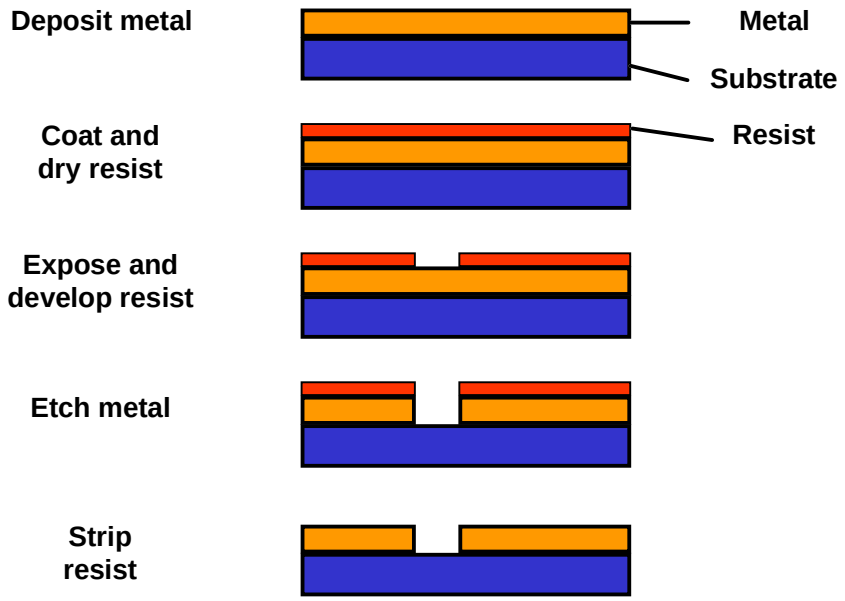


Figure 3.3 Thin film metal patterning process

achievable. Shipley recommends a range of speeds between 3000 and 5000 rpm for the 1350J formulation and a median speed of 4000 was chosen for the deposition of the photoresist in these experiments. The relatively large feature sizes in the metal layers made line resolution essentially a non-issue.

The spin-coating process requires a clean, planar surface for the even deposition of a film. All sputtered substrates were assumed to have highly pure surfaces as a result of the sputtering processes used. The following schedule was developed for the deposition of uniform photoresist films on the ceramic substrates:

1. Center substrate to be coated on spin chuck.
2. Adjust spin time and speed to 40 sec and 500 rpm, respectively.
3. Dispense approximately 1 ml of phototresist solution in center of substrate.
4. Start spin and allow solution to dynamically spread for 2 – 5 sec.
5. Ramp spin speed to 4000 rpm at quickly as possible.
6. Allow chuck to stop after spin time has elapsed.
7. Remove substrate from chuck and place on curing sheet.

Once a number of coated substrates were made and placed on a curing sheet, the sheet was placed in a convection oven at 90ºC for 30 minutes to soft-bake the polymer films. The soft-bake process removes most of the volatile solvent carrier from the photoresist film and also partially polymerizes it, making the film more robust and able to withstand subsequent processing steps. The soft-baked substrates were exposed using either the mercury vapor or thick-film exposure units and the dielectric layer mask. Exposed substrates were developed for one minute in Shipley 353 developer, which is a strongly basic, sodium hydroxide solution. Developed films were rinsed with deionized water to remove residual developer and spun dry for 30 sec at 3000 rpm.

To prepare the photoresist films for the etching processes, they were hard-baked in the convection oven for 30 minutes at 120ºC. This fully cures the films and enables them to

resist the chemical action of the etchant solutions. At these temperatures, oxidization of exposed copper surfaces was observed, which could possibly affect their interaction with subsequently deposited polyimide films. Nickel surfaces were unaffected by the hard-bake process. The hard-baked substrates were then placed in an etching bath of heated sodium persulfate. Sodium persulfate reacts readily with metallic copper and etches approximately 0.001 inches every 4 minutes. Although metallic nickel is not as reactive as copper in a solution of sodium persulfate, thin films of nickel can be slowly etched. When the sodium persulfate solution breaks through the nickel layer, it can reach the copper layer underneath, accelerating the etching process. For the sputtered films deposited in these experiments, which were on the order of 1 micron thick, the etching time was found to be 15 – 20 seconds. Once etching is complete, the substrate is rinsed with deionized water and spun dry for 30 sec at 3000 rpm. The substrate is then immersed for 1 minute in Shipley photoresist strip, n-methyl-pyrollidone (NMP), which removes the layer of photoresist. The substrate is again rinsed with deionized water and spun dry for 30 sec at 3000 rpm.

3.5 Polymer Dielectric Deposition

The choice of dielectric materials available for use in this thesis was limited to DuPont Pyralin PI-2615, a standard OMDA-PDA polyimide, Pyralin PI-2721, a photosensitized polyimide, and an experimental fluoropolymer, developed at the Naval Research Laboratory. Both of the non-photosensitive polymers required the use of dry etch methods which were not readily available to the author. As a result, all experimental studies results were performed using the PI-2721 photosensitive polymer, due to the ease with which it can be processed. Data sheets summarizing the properties and processing steps for PI-2721 can be found in Appendix B.

Pyralin PI-2721is a polymer precursor solution consisting of PMDA and ODA oligimers in a solution of NMP. Photosensitive end groups are incorporated into the polymer backbone, allowing for patterning of the soft-baked film without the use of a photoresist. The 2700 series of resins are formulated to achieve a range of cured film thicknesses,

based on the solids content of the original polymer precursor. PI-2721 can achieve film thicknesses in the range of 5 μm to 15 μm, depending on the spin-coating speed.

The equipment used for the deposition of the thin film polymers was a XYZ Model 123 spin-coater. This equipment has an integral vacuum chuck system which holds the substrates to the spin chuck during a coating sequence. The speed and time of spinning can be set using dials on the control head, but are static for the duration of a coating sequence.

Before the PI-2721 polymer was deposited, it had to be removed from refrigerated storage and allowed to warm to approximately room temperature. The precursor is sensitive to UV radiation, so all processing must take place in a UV-suppressed environment. In the Microelectronics Lab, one room is dedicated to wet processing and has UV filters in place on the fluorescent lighting in the wet stations. At this time, the mercury vapor UV source or the thick-film screen exposure unit was powered on and allowed to warm up to operating conditions. A convection oven was used for the soft and hard baking of the deposited polymer films, and was also turned on at this point. The mercury vapor UV source became inoperable during the course of this research and due to its age, replacement parts were unavailable. As a result, the remaining UV processing was performed using the thick-film exposure unit.

The spin-coating process requires a clean, planar surface for the even deposition of a film. All sputtered substrates were assumed to have highly pure surfaces as a result of the sputtering processes used. The following schedule was developed for the deposition of uniform polymer films on the ceramic substrates:

1. Center substrate to be coated on spin chuck.
2. Adjust spin time and speed to 40 sec and 500 rpm, respectively.
3. Dispense approximately 1 ml of precursor solution in center of substrate.
4. Start spin and allow solution to dynamically spread for 2 – 5 sec.

5. Ramp spin speed to 3000 rpm at quickly as possible.
6. Allow chuck to stop after spin time has elapsed.
7. Remove substrate from chuck and place on curing sheet.

The use of this schedule allowed the consistent formation of uniform films of uncured polymer precursor. Inspection of the films revealed a number of common defects, including dirt trapped in the film, bubbles, and incomplete coatings due to insufficient amounts of dispensed precursor. The first two defects were due to the age of the precursor solution used, which had most probably been improperly stored for an extended period of time, allowing a significant amount of solvent to escape from solution, increasing its viscosity and the occurrence of bubbles in the dispensed polymer precursor.

Once a number of coated substrates were made and placed on a curing sheet, the sheet was placed in a convection oven at 55ºC for 2 hours to soft-bake the polymer films. The soft-bake process removes most of the volatile solvent carrier from the precursor film and also partially imidizes it, making the film more robust and able to withstand subsequent processing steps. The soft-baked substrates were exposed using either the mercury vapor or thick-film exposure units and the dielectric layer mask. Exposed substrates were developed for one minute in DuPont DE-6018 developer, which is a solution of xylene and butryolactone. Developed films were rinsed with DuPont RI-9045 (xylene) to remove residual butryolactone and spun dry for 30 sec at 3000 rpm. Inspection of the developed substrates showed numerous pinholes and contaminants in the film, as discussed previously. The majority of the film surface, however, was free of defects and would provide adequate isolation between metal layers.

The patterned substrates were then placed on a quartz sheet and inserted into an ashing furnace to complete the curing of the polymer films. The full curing schedule for PI-2721 is shown in Table 3.1.

Starting Temperature (ºC)	Final Temperature (ºC)	Ramp Time or Hold Time	Atmosphere
Room Temperature	150	4 - 5ºC/min	Air
150	150	30 min	Air
150	300	2ºC/min	Air
300	300	30 min	Air
300	310 - 450	2ºC/min	Inert
310 - 450	310 - 450	30 – 60 min	Inert
310 - 450	Room Temperature	< 10ºC/min	Inert/Air

Table 3.1 Curing schedule for PI-2721 polyimide

Previous experience had shown this particular furnace to be incapable of maintaining a low-oxygen environment when purged with nitrogen, and the curing profile was modified to allow curing only under air. DuPont recommends a minimum curing temperature of 300ºC and all substrates were cured at this temperature under air only. Since the performance of the cured films was found to fall within specifications, this was determined to have little effect on the electrical performance of the capacitor structures. Of the eight substrate fabricated, the final four were improperly cured, due to an error in the temperature controller for the furnace, and were cured at > 300ºC under air. Referring to the processing manual for PI-2721, DuPont has determined that for temperatures above 400ºC under air, degradation of the cured films begins to occur and increases rapidly with temperature. The stability of the PI-2700 series of photosensitive polyimides is depicted in Figure 3.4. The effects of the elevated curing temperature appear to have been negligible and will be discussed more thoroughly in Chapter 4. Fully cured PI-2721 films normally are dark yellow in color, while the over-cured films were dark red in color.

3.6 Test Fixture Design

To facilitate measurement of the capacitor properties while under controlled environmental conditions of high humidity and temperature, a test fixture was designed. This fixture connects the test leads from measurement equipment outside the environmental chamber to a set of sockets which the substrate carriers described earlier

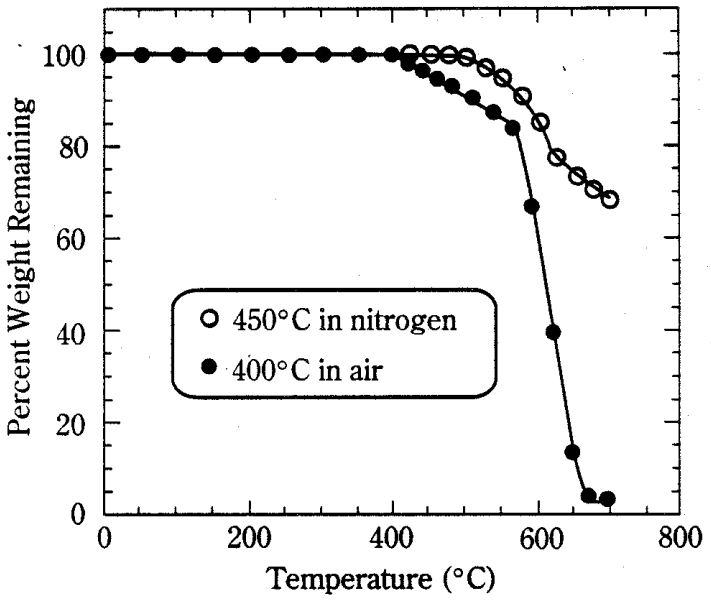


Figure 3.4 Stability of PI-2721 polyimide versus temperature

are inserted into. This metal carrier can be easily removed and exchanged with another without requiring separate fixtures for each substrate.

The simplest fixture design consists of two rows of sockets mounted to a double-sided printed circuit board (PCB). The PCB can then be patterned to spread the signals from the substrate carrier to a set of coaxial connectors along the periphery of the PCB. To reduce the magnitude of errors incurred by the impedance mismatch between the coaxial feeds and the signal traces on the PCB, a grounded co-planar waveguide structure was chosen. A schematic of this structure is depicted in Figure 3.5. This waveguide structure allows for a relatively constant impedance over a wide range of frequencies. A

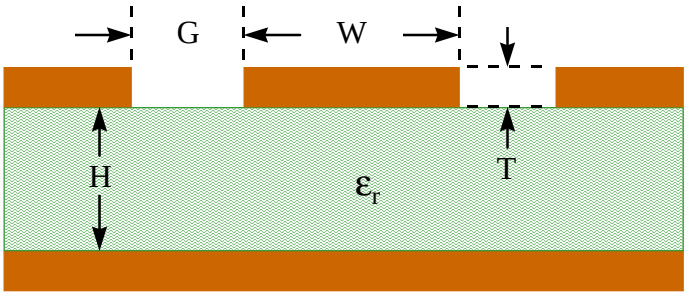


Figure 3.5 Structure of grounded, co-planar waveguide

commercially available software package called TXLINE was used to calculate the values for the width of the center conductor trace and the gap distance between the center trace and the surrounding ground layer. TXLINE uses empirical formulas to determine the characteristic impedance of a waveguide based on known physical dimensions and the dielectric constant of the substrate material [28]. These equations are discussed in Appendix A.

The variables used to determine these values were the dielectric constant of FR-4 PCB material [29], $\varepsilon_r = 4.5$, its loss tangent, $\tan \delta = 0.02$, and the dimensions of the PCB material. The double-sided, copper-clad PCB consists of two layers of 0.00135 inch thick copper bonded to either side of a 0.062 inch thick fiberglass/epoxy core [30]. A standard 6 by 6 inch board was purchased from Kepro Circuit Systems for fabrication of the test

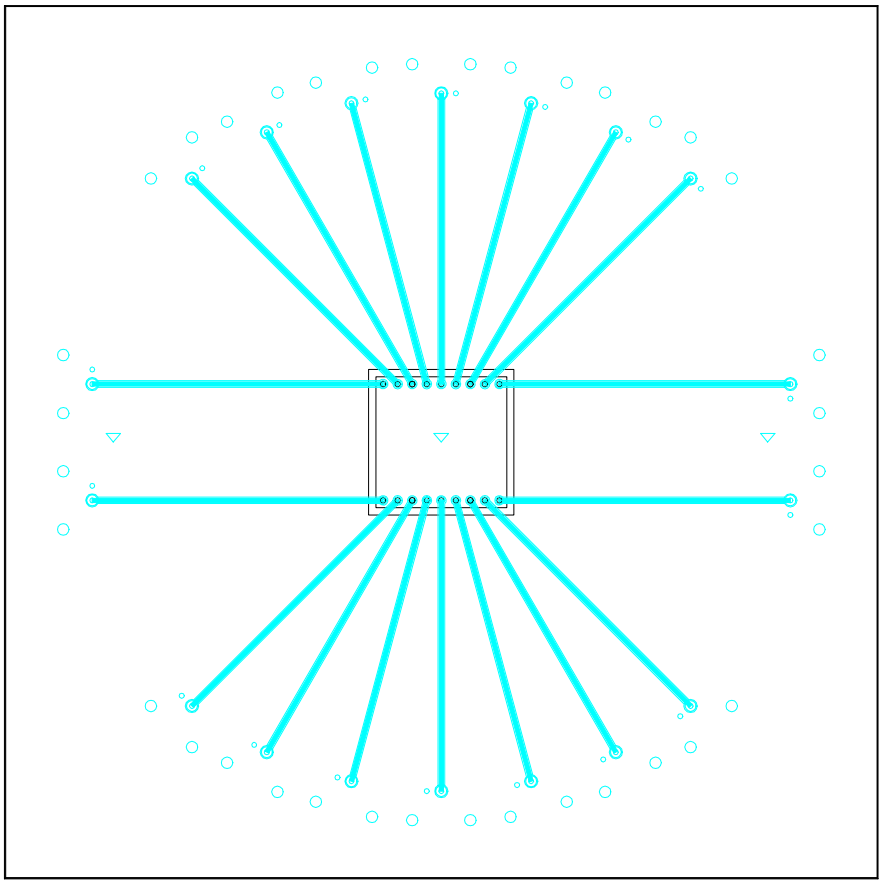


Figure 3.6 Mask for test fixture PCB

board. Using these variables and the TXLINE software, a center conductor width *W* of 0.0285 inches and gap width *G* of 0.008 inches were calculated to achieve a impedance of 49.96 Ω at 1 MHz. Using these dimensions, the pattern for the test fixture PCB, shown in Figure 3.6, was created using AutoCAD and transferred to rubylith as described previously. Due to the large size of the PCB test board, the mask pattern had to be plotted in two halves to allow the transfer of the pattern to film. The two halves were then joined into one continuous mask.

The PCB test board was patterned using standard PCB etching processes and attached to a plexiglas support using 4 inch metal standoffs. This allowed the test fixture to stand vertically in the environmental chamber and permit unobstructed exposure to both sides of the test board. This configuration also placed the test fixture in a position which required the shortest lengths of feedthrough cable, which pass signals from the connectors on the test board to the tee connectors attached to the test leads of the impedance analyzer. Opening the chamber is not possible while it is operational and feedthroughs for all eighteen connectors on the test board were assembled, permitting the simultaneous analysis of all structures on a test coupon. For the measurements undertaken by this research, the test leads were manually switched between feedthroughs to test individual devices.

Chapter 4 – Experimental Results

4.1 Introduction

This chapter presents the results of experiments performed to determine the effects of environmental conditions on the electrical performance of polymer dielectrics. The first experiment discussed is impedance measurements to determine the changes in dielectric constant and loss tangent due to the effects of high humidity and temperature. These measurements were also conducted without the presence of high humidity as a control to compare against the previous experiment. Supplementary measurements were also performed with another impedance analyzer to provide supporting data at higher frequencies, and as a check on the accuracy of the low frequency data. Upon completion of the impedance measurements, two sets of substrates were subjected to high voltage breakdown measurements. One set was allowed to remain at ambient humidity and temperature, while the other was exposed to conditions of high humidity and temperature. By comparing the results for these two sets of substrates, conclusions may be drawn with respect to electrical performance of the polymer dielectric under environmental stress.

4.2 Experimental Setup for Impedance Measurements

Four test coupons, each from separate substrates, were chosen for assembly into carriers. Two substrates, 1 and 3, were processed normally and were determined to have produces better than average devices. The remaining substrates, 5 and 6, were improperly cured at high temperature, but were included to determine the effects of oxidization on the electrical performance of the polymer dielectric.

Each substrate was sputtered with a single layer of nickel of its back, to provide a wettable surface for solder attachment to the metal carrier. A piece of Indium Corp. SN62 solder preform was dipped in 5RMA flux and placed between the legposts in each carrier. The substrate were then placed on top of the solder and the assembly was processed through an IR reflow oven with the following settings:

Upper Preheat	100
Lower Preheat	100
Upper Spike	210
Lower Spike	150
Speed	15% of maximum

Successful soldering was determined by sharply striking the corner of an inverted carrier against a benchtop. Substrates which detached from the carrier were not heated sufficiently to melt the solder preform and were reflowed a second time. All substrates reflowed successfully after no more than two reflow passes.

The final phase of assembly required wirebonds to be made between metal pads on the coupon surface and the metal posts of the carrier. An Orthodyne Electronics model 20B wirebonder with 5 mil aluminum wire was used for this purpose. Adhesion between the sputtered metal layers and the alumina substrate was found to be compromised by the wirebonding process, which creates a bond using thermosonic compression. This wirebonding technique used heat, pressure, and ultrasonic energy to create a weld between the metal surface and the aluminum wire. A completed carrier populated with a test coupon is shown in Figure 4.1. Common defects encountered were a complete delamination of the sputtered metal from the substrate surface directly underneath the wirebond. The first assembled carrier was wirebonded only hours after the reflow process and displayed the best results when wirebonded. The other three coupons were

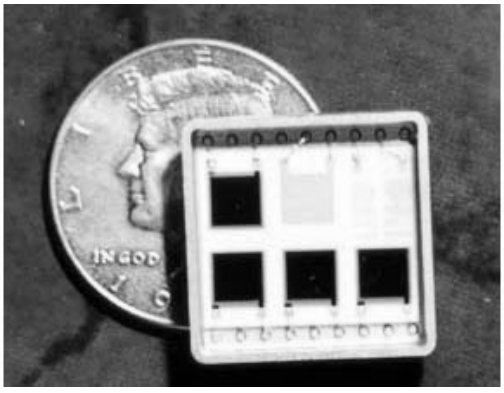


Figure 4.1 Completed carrier with test coupon

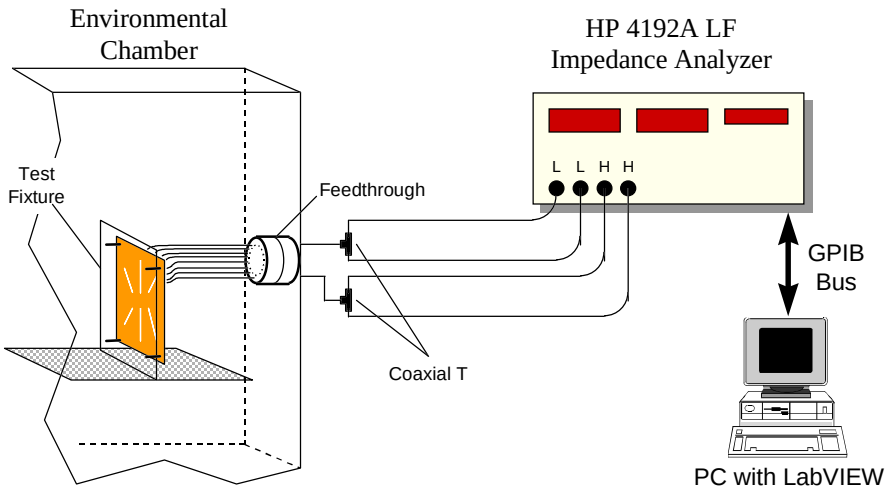


Figure 4.2 Test configuration for impedance measurements under high humidity and temperature conditions

wirebonded days to weeks later and showed poor results when wirebonded. These results can be attributed to the reactivity of the sputtered copper layer, which was deposited directly on the ceramic substrate without the benefit of a adhesion layer. Common practice in the electronics industry is the use of a titanium or chromium film to improve the adhesion of copper metallizations to a substrate surface. A workaround was developed which placed wirebonds adjacent to the wirebond pads on the coupon surface and conductive epoxy was used to connect the wirebonds to the pads. The conductive expoy is a two-part system which is mixed, applied to the coupon surface, and then cured for 20 minutes at 150ºC.

The experimental setup used for the impedance measurements is shown in Figure 4.2. The environmental chamber used was a Blue M model CFR-7652C-2 which has an operating temperature range of 3ºC to 93ºC at relative humidities between 40% and 98%. To prepare the chamber for testing, sixteen feedthroughs were fabricated which allowed connectivity from coaxial connectors on the periphery of the test board to the HP 4192A/LF Impedance Analyzer outside. The 4192A/LF uses a four-wire test lead configuration for measurement of the complex impedance of a device and can make measurements over a frequency range of 10 Hz to 13 MHz. Two test lead sets were

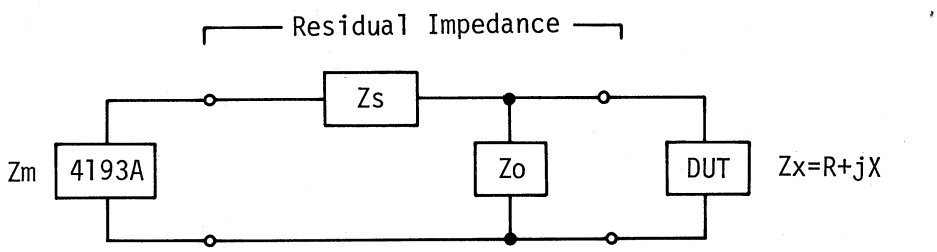


Figure 4.3 Circuit used in compensation calculations for residuals

utilized in making the impedance measurements. The HP 16048A test lead set is a simple four wire, coxial cable set and was used to connect to chamber feedthroughs via two coxial tee connectors for measurements of the test coupon capacitor structures. The HP 16334A test lead set is a comprised of a four wire cable and a two lead probe. This test set was used for measurements of undiced substrates outside the environmental chamber. In measuring the impedance of the capacitor structures, it is necessary to take into account the parasitic impedances of the measurement circuit. These parasitics include the HP 16048A test leads, feedthrough cables, copper traces on the test board, and wirebonds which can collectively be called the "probe". Figure 4.3 shows an equivalent circuit model which includes the parasitic or residual impedance of the probe. To compensate for the residual impedance of the test leads, two measurements are made as follows [31]:

1. Open circuit: attach the test leads to the cables connected to the open circuit structure and record the value displayed as Z_{oc} (i.e. $Z_m = Z_{sc} + Z_{oc}$, for $Z_{oc} >> Z_{sc}$ then $Z_m = Z_{oc}$)
2. Short circuit: attach the test leads to the cables connected to the short circuit structure and record the value displayed as Z_{sc} (i.e. $Z_m = Z_{sc}$)

Using these values, the actual impedance of the capacitor, Z_{dut} ($R_s + jX_s$), can be calculated from the equations given in Appendix A. From this impedance value, the equivalent capacitance C_s and quality factor Q of the device is given by:

$$C_s = -\frac{1}{X_s \omega} \tag{4.1}$$

$$Q = \frac{|X_s|}{R_s} \tag{4.2}$$

where ω is the angular frequency (equivalent to $2\pi f$), X_s is the imaginary part of the corrected impedance value (the capacitive reactance), and R_s is the real part of the corrected impedance value and represents the effective series resistance of the capacitor. This resistance is a single value which represents the sum of the ac losses (due to the leads, electrode plates, and junction terminations), the resistive losses due to leakage currents, and the resistive losses due to the inherent molecular polarization dielectric absorption factors of the base dielectric material. The quality factor or *Q* of the capacitor is a critical figure of merit, especially for RF tuned circuit design. For real world capacitors, *Q* values range from less than 100 for ceramic capacitors up to several thousand for polystyrene and mica capacitors.

The dielectric constant, ε_r, of the polymer can then be derived using the equation for a parallel plate capacitor:

$$C = \frac{\varepsilon_o \cdot \varepsilon_r \cdot A}{t} \tag{4.3}$$

where

A = 200 mils × 200 mils = 0.258 cm^2	Capacitor Area
t = 0.0007 cm	Dielectric Thickness
$\varepsilon_o = 8.854 \times 10^{-14}$ F/cm	Permittivity of Free Space

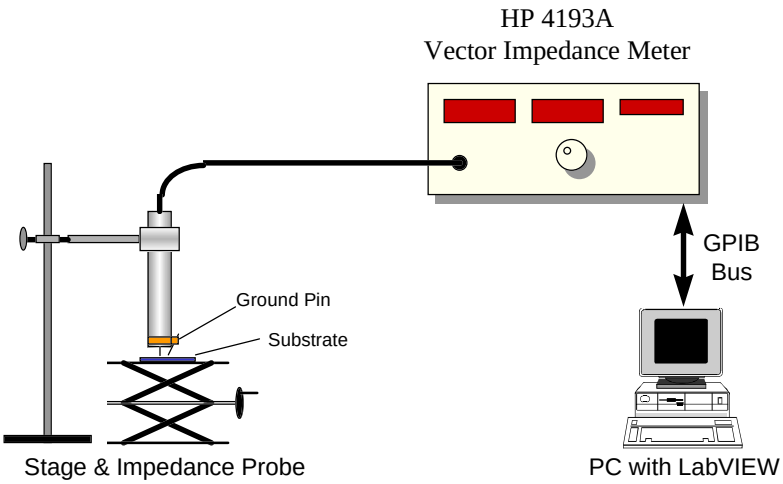


Figure 4.4 Test configuration for high frequency impedance measurements

The loss tangent of the dielectric is the ratio of effective series resistance R_s to capacitive reactance X_s. This parameter is a measure of the energy loss in the dielectric as a function of frequency. The value for the loss tangent can also be found using the reciprocal of the quality factor, Q:

$$\tan \delta = \frac{1}{Q} = \frac{R_s}{|X_s|} \tag{4.4}$$

Additonal impedance measurements were performed using an HP 4193A Vector Impedance Meter, which has a frequency range of 0.4 to 110 MHz. These measurements were performed on the two undiced substrates with copper metallization only. A comparison was made between the results achieved using the 4193A and those from the 4192A/LF for capacitors on the two undiced substrates to determine the accuracy of the 4192A/LF near its high frequency limit of 13 MHz. A diagram of the experimental setup for impedance measurements at high frequencies using the 4193A is shown in Figure 4.4. The low frequency measurements were performed using the 4192A/LF and the HP 16334A probe set in place of the 4193A.

4.3 Experimental Results for Impedance Measurements

Impedance measurements were performed on coupons from substrates 1, 3, and 5 and the undiced substrates with copper metallizations only. Coupons 1 and 5 were subjected to 93% relative humidity at 100ºF for one week, with impedance measurements made at least once a day. Coupon 3 was exposed to ambient humidity (approximately 50% R.H.) at 100ºF, as a control experiment to determine whether humidity was solely responsible for any measured change in the properties of the polymer dielectric. The two undiced substrates were used to determine the accuracy of the impedance measurements made using the 4192A/LF in the high frequency regime (above 10 MHZ). The results of these experiments are shown in Appendix C.

A diagram showing the convention used to identify the capacitors on a fully or partially populated test coupon is shown in Figure 4.5. Thus, a capacitor designated "1b" refers to coupon number 1, capacitor b. Due to the poor yield of good capacitor structures on coupons 1 and 5, measurements were made using only one capacitor on those coupons. Coupon 3 had two good capacitor structures available for measurements, while the two undiced substrates had 11 and 12 good capacitors, respectively.

By comparing the variation in dielectric constant over time for coupons 1,3, and 5, it is can be seen that the humid environment that coupons 1 and 5 were exposed had the effect of increasing the dielectric constant of the polymer films. The effect of temperature on

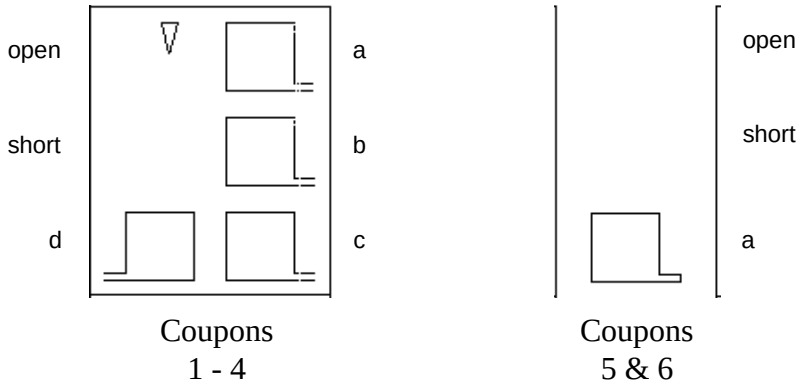


Figure 4.5 Test coupon identification scheme

dielectric constant appears to have been negligible, as evidenced by the relatively constant dielectric constants seen for coupon 3. For all coupons tested, dielectric constant decreased at an approximately linear rate. Data from the 4192A/LF Impedance Analyzer appears to incur large errors at higher frequencies. This observation was supported by measurements made using the 4193A Vector Impedance Meter on the two undiced substrates. Low frequency data for the 4192A/LF overlaps with the high frequency data from the 4193A and continues the linearly decreasing trend of the dielectric constant. Finally, the overcured dielectric used in coupon 5 had significantly higher values for its dielectric constant than the properly cured dielectric in coupon 3. This result is most probably due to degradation of the polymer at the elevated temperatures it experienced during cure.

The typical capacitance value for the thin film capacitor structures was approximately 100 to 200 pF. The variation in the capacitance was primary due to processing variation (over-temperature during cure, for example) and variations in the thickness of the deposited metals, due to the inherent anisotropic deposition pattern of the RF sputtering guns. This resulted in nonuniform resistivities across the metallized substrate surface.

Humidity also appears to have a detrimental effect on the loss tangent of the polymer dielectric. Long exposure to humidity increases the loss tangent of the polymer, while elevated temperatures appear to have no effect on this property. The values of loss tangent calculated using data from both the 4192A/LF and 4193A vary over a much wider range than those calculated for the dielectric constant. It was later discovered during the measurements for coupon 3 that one of the four test leads on the 4192A/LF was damaged. The test leads were replaced with four Ponoma (Belden 9223) low-noise, 50 Ω coaxial cables. Data taken using this configuration appears to display less noise, especially for loss tangent values.

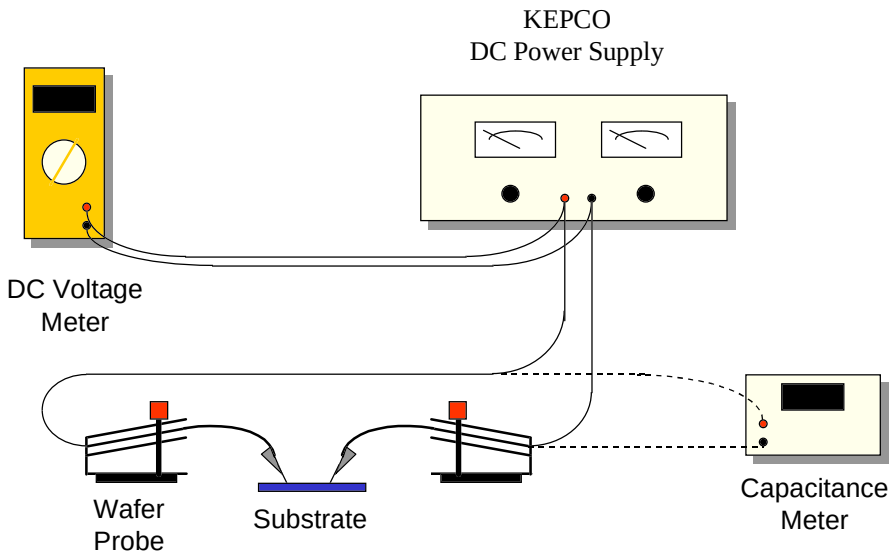


Figure 4.6 Voltage breakdown test configuration

4.4 Experimental Setup for Breakdown Voltage Measurements

The measurement of the breakdown voltage of the polymer dielectric was performed using the equipment shown in Figure 4.6. A high voltage DC power supply was connected to two wafer probes. The wafer probe pins were then held in contact with each capacitor structure on the substrate its value measured using an ESI 353 impedance meter. Capacitors which did not have capacitance values between 100 and 200 pF were marked as defective and not tested. Each good capacitor's value was recorded and then it was connected to the DC power supply. The DC voltage of the supply was ramped at approximately 5 volts/sec and settling times of 1 second every 25 volts were observed. The breakdown of the dielectric was accompanied by a loud "snap", especially for breakdown voltages above 100 volts. The breakdown voltage was then recorded along with the position of the breakdown on the capacitor surface.

4.5 Experimental Results for Breakdown Voltage Measurements

Measurements were taken for two series of substrates. The first series was allowed to remain at room temperature and humidity before testing. The second series was exposed

to 93% relative humidity at 100ºF for one week before testing. Each series consisted of samples from every substrate fabricated, and also included each of the undiced substrates. The results of the breakdown measurements are displayed in Figures 4.7 and 4.8, for the "dry" and "wet" cases, respectively.

From the data sheets in Appendix B, the breakdown field strength of Pyralin PI-2721 is given as > 2×10^6 V/cm which is equivalent to 200 V/μm. The thickness of the cured dielectric films was 7 μm, resulting in an expected breakdown field strength of 1.4 kV. The actual field strength will be affected by the curing conditions of the polyimide, especially in the case of the overcured substrates 5 through 8. Pinholes, debris, and other defects will also create conditions for premature breakdown of the dielectric film. These voids in the polymer film contain air, which creates a field intensification in the regions due to the mismatch in permittivity between the voids and the surrounding dielectric. Discharge due to ionization of the trapped gas creates a localized or partial breakdown of the polymer and over time leads ultimately to failure of the dielectric insulation.

Breakdown voltages for both series of substrates varied widely, but several trends were noted:

1. Substrates which were exposed to humidity had breakdown voltages which never exceeded approximately 700 volts.
2. The maximum breakdown voltage measured came quite close to the reported field strength given in the data sheets for PI-2721.
3. Only eight capacitors had breakdown voltages above 1000 volts.
4. The majority of capacitors had breakdown voltages below 400 volts.
5. Low voltage breakdown was localized around obvious pinholes or debris in the dielectric film.
6. High voltage breakdown was accompanied by vaporization of large portions of the top metal layer of the capacitor.

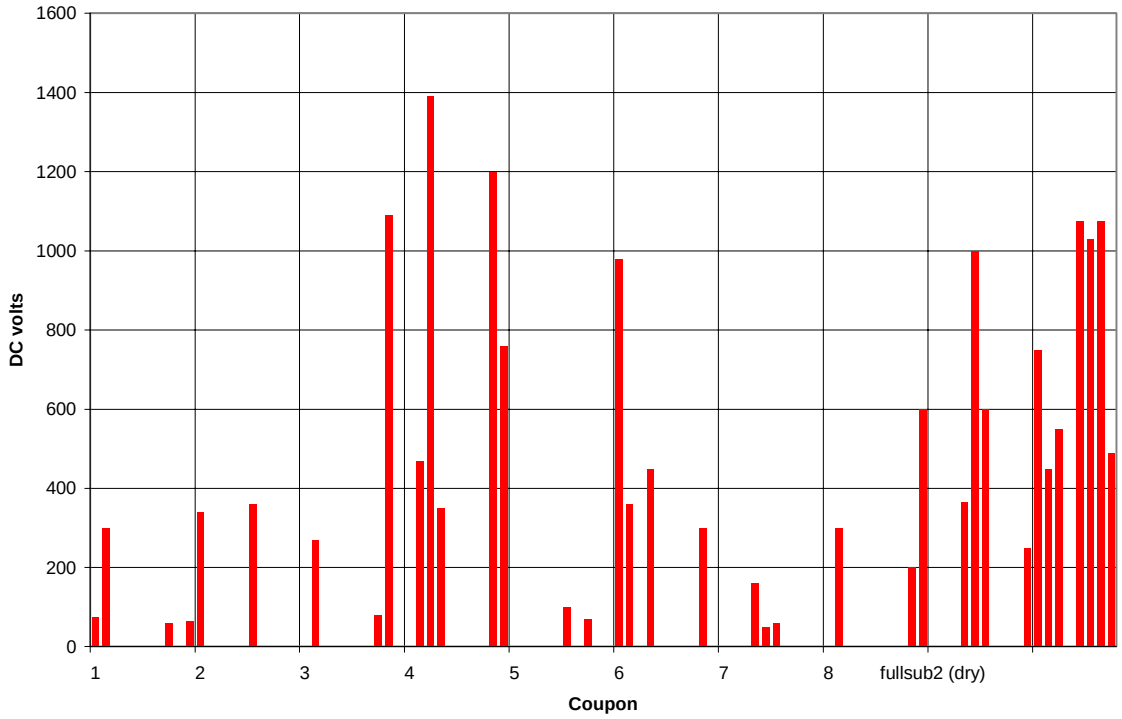


Figure 4.7 Breakdown voltage results for "dry" capacitor structures

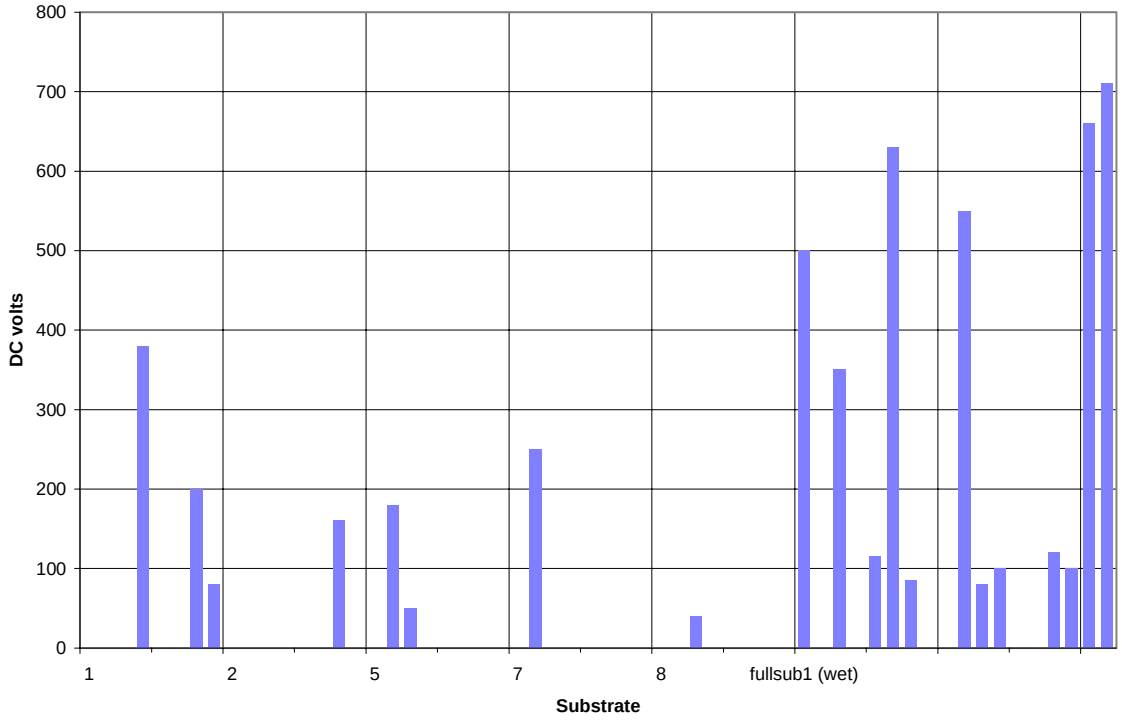


Figure 4.8 Breakdown voltage results for "wet" capacitor structures

Chapter 5 - Summary and Conclusions

5.1 Summary

The objective of this thesis was to characterize the effects of environmental stress upon the electrical performance of a thin film polymer dielectric. The particular electrical properties of interest were the dielectric constant, loss tnagent, and breakdown voltage of the polymer.

Chapter 1 was an introduction to this thesis and briefly described the contents of each chapter.

Chapter 2 provided an overview of the properties and processing methods for polymer dielectric films. It also included a discussion of thin film multilayer multichip packaging which represents the largest market segment for polymer dielectrics in electronics packaging.

Chapter 3 discussed the design considerations and processing methods used in the fabrication of the thin film capacitor structures. These structures were used to evaluate the performance of the polymer dielectric over the frequency range of 10 Hz to 110 MHz.

Chapter 4 presented the results of measurements of the impedance and breakdown field strength of the thin film capacitor structures. Impedance measurements over the frequency range of 400 kHz to 110 MHz were performed using the HP 4193A Vector Impedance Meter and from 10 Hz to 13 MHz using the HP 4192A/LF Impedance Analyzer.

5.2 Conclusions

The results presented in this thesis showed that the breakdown field strength of the polymer dielectric is influenced by the presence of residual moisture in the dielectric film. The presence of moisture is indicated by the increase over time of the measured dielectric

constant of the polymer in a high humidity environment. Elevated temperatures appeared to have little effect on the dielectric constant and were not considered to be as influential on the measured electrical performance of the polymer.

The thin film capacitor structures fabricated as part of the experimental portion of this thesis provided an accurate and reproducible method for determining the electrical properties of the polymer dielectric. Key issues encountered during their processing were adhesion between the metal layers and the ceramic substrate, the importance of maintaining a proper curing schedule, and the proper strorage and deposition of the polymer precursor solution.

A key topic for further research would be further testing on alternative polymer formulations, including BCBs, fluoropolymers, and other novel chemistries. Recent work with the NSF Center on High Performance Polymeric Adhesives and Composites at Virginia Tech has presented new and exciting opportunities for combined research.

The author is preparing to undertake continued research in the field of polymer materials for electronic packaging, particularly in the area of underfills and encapsulants for flip chip and ball grid array (BGA) packaging. Many of the issues pertaining to the performance and processing of these materials are common to all packaging methods. The experience of developing numerous thin film processes and performing the many experiments required has provided the author with a vital introduction to the use of polymeric materials for electronic packaging.

Appendix A

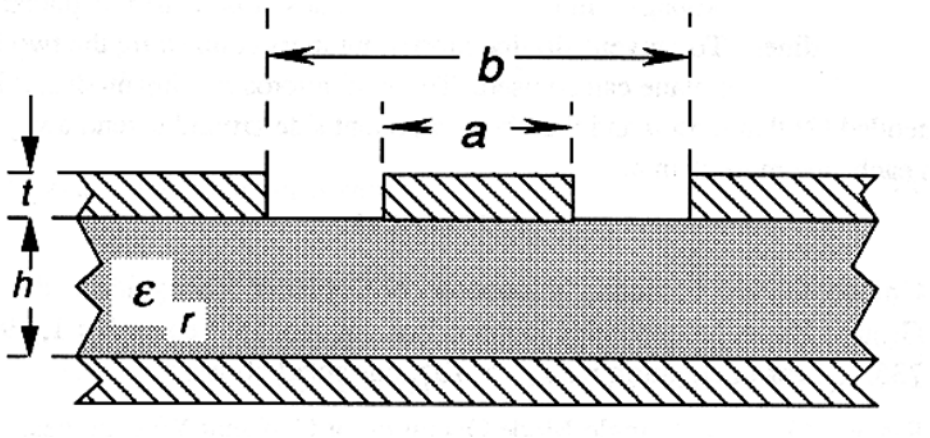


Figure A.1 Coplanar waveguide with ground

These equations can be used to analyze coplanar waveguides with ground or for microstrip lines with a signal side ground plane as depicted in Figure A.1 [28]:

$$Z_o = \frac{60.0 \cdot \pi}{\sqrt{\varepsilon_{eff}}} \frac{1.0}{\frac{K(k)}{K(k')} + \frac{K(k_1)}{K(k_1')}} \tag{A.1}$$

$$k = a/b \tag{A.2}$$

$$k_1 = \frac{\tanh\left(\frac{\pi \cdot a}{4.0 \cdot h}\right)}{\tanh\left(\frac{\pi \cdot b}{4.0 \cdot h}\right)} \tag{A.3}$$

$$k' = \sqrt{1.0 - k^2} \tag{A.4}$$

$$k_1' = \sqrt{1.0 - k_1^2} \tag{A.5}$$

$$\varepsilon_{eff} = \frac{1.0 + \varepsilon' \dfrac{K(k')}{K(k)} \dfrac{K(k_1)}{K(k_1')}}{1.0 + \dfrac{K(k')}{K(k)} \dfrac{K(k_1)}{K(k_1')}} \qquad \text{(A.6)}$$

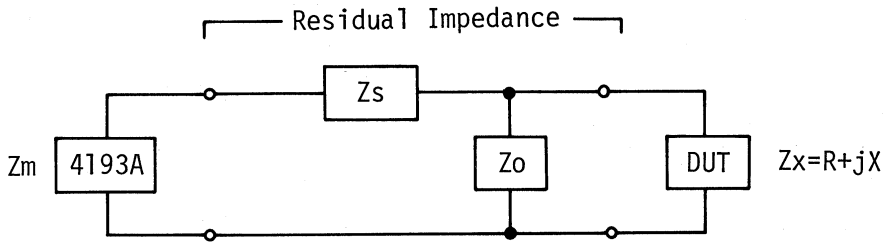
The elliptic integral ratio of *K(k)/K(k')* is a form found commonly in transmission line problems and can be approximated by:

$$\frac{K(k)}{K(k')} \cong \frac{1.0}{2.0 \cdot \pi} \ln\left(2.0 \frac{\sqrt{1.0 + k} + \sqrt[4]{4.0 \cdot k}}{\sqrt{1.0 + k} - \sqrt[4]{4.0 \cdot k}} \right) \qquad \text{if } 0.5 \le k^2 \le 1.0 \qquad \text{(A.7)}$$

$$\frac{K(k)}{K(k')} \cong \frac{2.0 \cdot \pi}{\ln\left(2.0 \dfrac{\sqrt{1.0 + k'} + \sqrt[4]{4.0 \cdot k'}}{\sqrt{1.0 + k'} - \sqrt[4]{4.0 \cdot k'}} \right)} \qquad \text{if } 0 \le k^2 \le 0.5 \qquad \text{(A.8)}$$

These equations are accurate to within 4×10^{-12}.

Appendix B



Zm =measured impedance, Zs =short-circuit impedance,
Zo =open-circuit impedance, Zx =DUT impedance.

$$|Zx| = \sqrt{R^2 + X^2}$$

$$\theta = \tan^{-1}\frac{X}{R}$$

where:

$$R = \frac{(|Z_0|\cos\theta m - |Zm|\cos\theta_0)\cdot|Zm|\cdot|Z_0|}{(|Z_0|\cos\theta m - |Zm|\cos\theta_0)^2 + (|Zm|\sin\theta_0 - |Z_0|\sin\theta m)^2} - |Zs|\cos\theta s$$

$$X = \frac{(|Z_0|\sin\theta m - |Zm|\sin\theta_0)\cdot|Zm|\cdot|Z_0|}{(|Z_0|\cos\theta m - |Zm|\cos\theta_0)^2 + (|Zm|\sin\theta_0 - |Z_0|\sin\theta m)^2} - |Zs|\sin\theta s$$

$|Z_0|$ and θ_0: Open circuit impedance and phase, respectively.
$|Zs|$ and θs: Short circuit impedance and phase, respectively.

Note

These equations assume that $Z_0 >> Zs$.

Figure B.1 Equivalent circuit model for residual impedance in measuring circuit

Appendix C

Pyralin® PD Polyimide Coatings
G-Line Products PI-2721, PI-2722, PI-2723
Data Sheet

DuPont Electronics

Semiconductor Materials, Services and Technologies

Test	PI-2721	PI-2722	PI-2723	Du Pont Test Method
Solids %	30.0 ± 1	29.7 ± 1	26.3 ± 1	TM II A-1
Viscosity, poise	35 ± 5	25 ± 5	7.5 ± 1.0	TM II H-1
Ash, max. %	0.1	0.1	0.1	TM II F
Density, 25°C, g/cc	1.16 ± 0.10	1.15 ± 0.10	1.13 ± 0.10	TM II G-1
Solvent System	NMP	NMP	NMP	TM II D
Chloride Content*, max. ppm	1	1	1	TM II C-1
Sodium Content*, max. ppm	1	1	1	TM II B
Potassium Content*, max. ppm	1	1	1	TM II B
Copper Content*, max. ppm	1	1	1	TM II B
Iron Content*, max. ppm	1	1	1	TM II B
Total Metals**, max. ppm	10	10	10	TM II I
Water Content*, max. %	1.0	1.0	1.0	TM II J
Filtration, µm abs	0.2	0.2	0.2	
Shelf Life	>3 months at 25°C, >1 year at −18°C			

*Determined on total sample
**Excluding Silicon

Figure C.1 DuPont test data sheet for photosensitive polyimide products

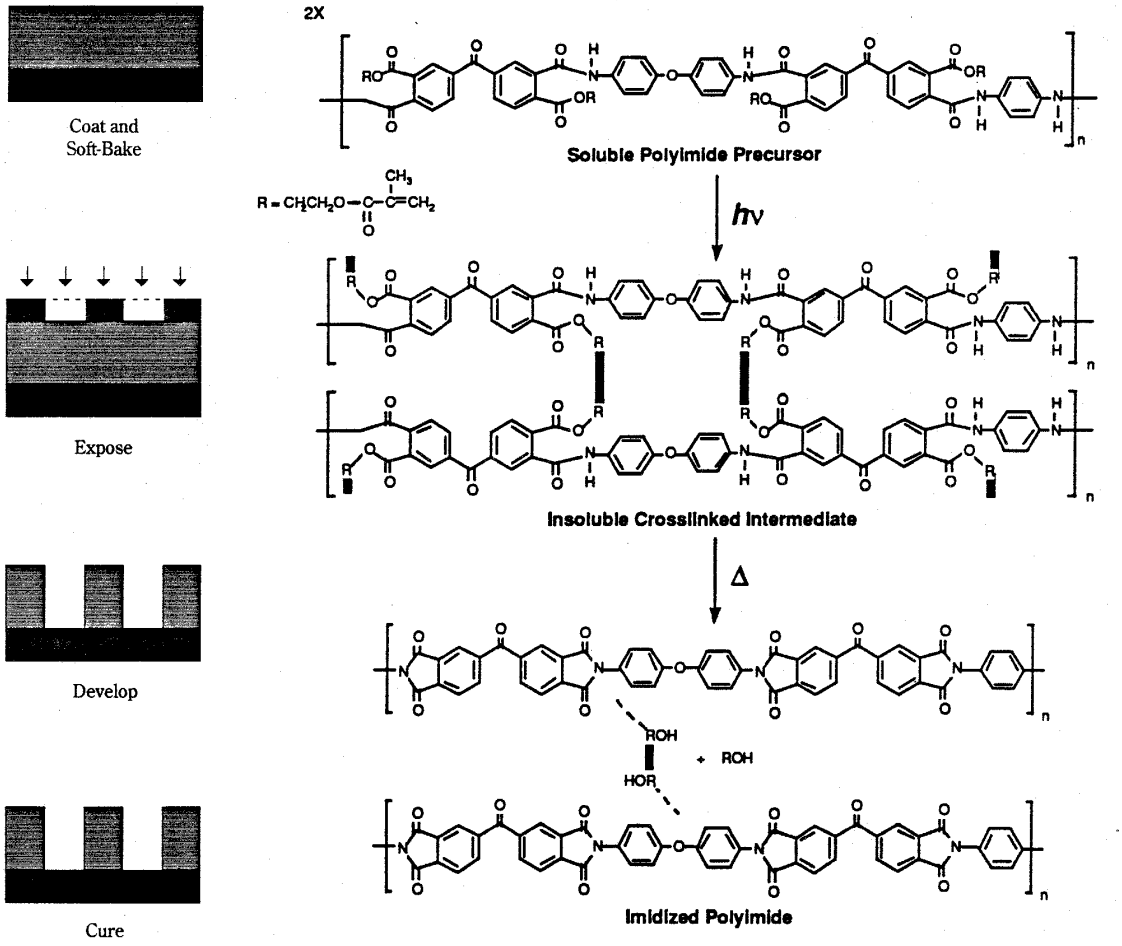


Figure C.2 Photolithographic steps and corresponding intermediates for PI-2721

TABLE 2. PROCESS SUMMARY

	PI-2721	PI-2722	PI-2723	Remarks
Spin Coat (rpm)	2500	3000	3500	30 sec
Soft-Bake (min/°C)	120/55 3/60; 3/105	90/55 3/60; 3/85	— 4/75	Oven Hot Plate
Thickness (µm)	20	10	5	After soft-bake
Exposure (mJ/cm²)	750	300	200	Contact printer
Development (sec)	25	20	15	Spin spray
Overlap (sec)	7	7	7	Developer/rinse
Rinse (sec)	20	20	20	Spin spray
Cure (min/°C) Atmosphere	30/150 + Air	30/300 + Air	30/400 Inert	Convection Oven or Diffusion Furnace
Thickness (µm)	10	5	2.5	After cure

Figure C.3 General processing steps for PI-2700 series polyimides

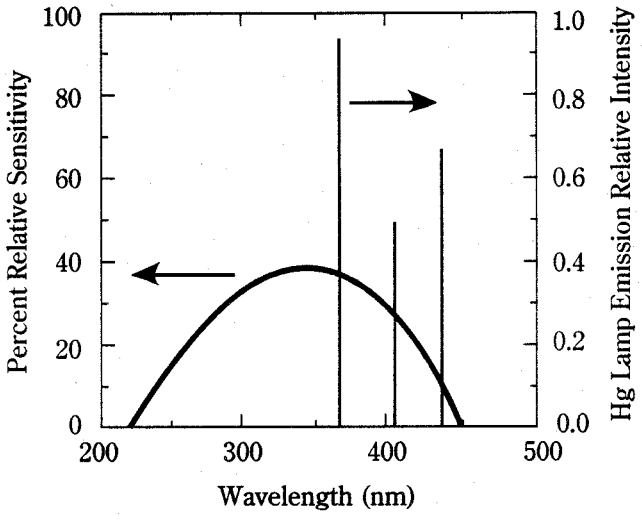


Figure C.4 Photosensitivity spectrum of PI-2700 series polyimides

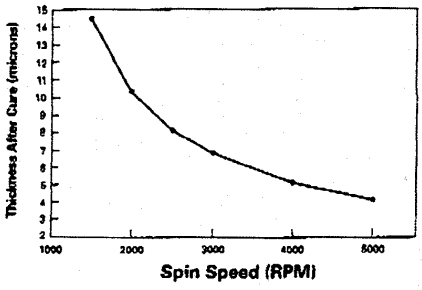
Pyralin® PD Polyimide Coatings

PI-2721, PI-2722 and PI-2723 Data Sheet

DuPont Electronics

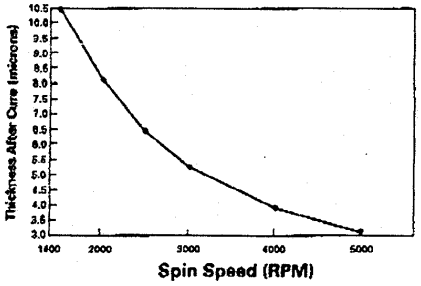
Semiconductor Materials, Services and Technologies

Spin Speed vs. Film Thickness
PI - 2721



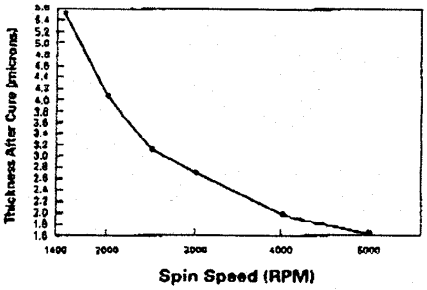
Wafer Size: 100mm
Soft-Bake: 120 min. @ 55°C
Cure: 20 min. @ 400°C in air

Spin Speed vs. Film Thickness
PI - 2722



Wafer Size: 100mm
Soft-Bake: 120 min. @ 55°C
Cure: 20 min. @ 400°C in air

Spin Speed vs. Film Thickness
PI - 2723



Wafer Size: 100mm
Soft-Bake: 120 min. @ 55°C
Cure: 20 min. @ 400°C in air

Du Pont Electronics
Barley Mill Plaza
P.O. Box 80019
Wilmington, DE 19880-0019
Product Information: 1-800-237-4357
Ordering Information: 1-800-237-2374

DU PONT

Figure C.5 Spin coating parameters for PI-2700 series polyimides

Pyralin® PD Polyimide Coatings

Technical Data Sheet for DE-6018

DuPont Electronics

Semiconductor Materials, Services and Technologies

Test	DE-6018	Test Method
Density (25°C)	1.00 ± 0.1 g/cm³	Du Pont TM II G
Solvent System	γ-Butyrolactone/Xylene 50/50 ± 5% by volume	Du Pont TM II D
Chloride Content*	4.0 ppm max.	Du Pont TM II D
Sodium Content*	0.5 ppm max.	Du Pont TM II B
Potassium Content*	0.3 ppm max.	
Copper Content*	0.3 ppm max.	
Iron Content*	0.3 ppm max.	
Water Content*	1.0 % max.	Du Pont TM II K
Filtration	0.2 micron absolute	

* Determined on total sample.

Figure C.6 Data sheet for DE-6018 developer used with PI-2700 series polyimides

Pyralin® PD Polyimide Coatings
PI-2721/PI-2722/PI-2723 Data Sheet

DuPont Electronics

Semiconductor Materials, Services and Technologies

CURED FILM PROPERTIES			
PHYSICAL	Tensile Strength	MPa	160
	Elongation	%	12
	Density	g/cm³	1.61
	Moisture Uptake (@ 100% RH)	wt %	4.3
	Young's Modulus	GPa	2.7
	Stress (10 µm Film)	MPa	42
THERMAL	Glass Transition Temperature	°C	>320
	Melting Point	°C	None
	Decomposition Temperature	°C	550
	Weight Loss (500°C in air, 2 hrs.)	%	0.5
	Coefficient of Thermal Expansion	ppm	57
	Coefficient of Thermal Conductivity	cal/cm · sec · °C	37×10^{-5}
	Specific Heat	cal/g · °C	0.26
ELECTRICAL	Dielectric Constant (@ 1 kHz)		3.3
	Dissipation Factor (@ 1 kHz)		0.002
	Dielectric Breakdown Field	V/cm	$>2 \times 10^4$
	Volume Resistivity	Ω-cm	$>10^{16}$
	Surface Resistivity	Ω	$>10^{15}$

Figure C.7 Cured film properties for PI-2700 series polyimides

Pyralin® PD Polyimide Coatings

Comparison of Pyralin® PD and Other Pyralin® Polyimides Data Sheet

DuPont Electronics

Semiconductor Materials, Services and Technologies

CURED FILM PROPERTIES					
		Units	PI-2721/22/23	PI-2546	PI-2555
PHYSICAL	Tensile Strength	MPa	160	160	180
	Elongation	%	12	60	25
	Density	g/cm³	1.61	1.42	1.45
	Young's Modulus	GPa	2.7	1.3	3.2
	Moisture Uptake (@ 100% RH)	%	4.3	3.5	3.5
	Stress (10 µm Film)	MPa	42	15	—
THERMAL	Glass Transition Temperature	°C	>320	>400	>320
	Melting Point	°C	None	None	None
	Decomposition Temperature	°C	550	580	550
	Weight Loss (500°C in air, 2 hours)	%	0.5	3.6	2.9
	Coefficient of Thermal Expansion	ppm	57	26	41
	Coefficient of Thermal Conductivity	cal/cm · sec · °C	35×10^{-4}	37×10^{-4}	35×10^{-4}
	Specific Heat	cal/g · °C	0.26	0.26	0.26
ELECTRICAL	Dielectric Constant (@ 1 kHz, 50% RH)		3.3	3.5	3.3
	Dissipation Factor (@ 1 kHz)		0.002	0.002	0.002
	Dielectric Breakdown Field	V/cm	$>2 \times 10^6$	$>2 \times 10^6$	$>2 \times 10^6$
	Volume Resistivity	Ω-cm	$>10^{16}$	$>10^{16}$	$>10^{16}$
	Surface Resistivity	Ω	$>10^{15}$	$>10^{15}$	$>10^{15}$

Figure C.8 Comparison of properties for photosensitive and non-photosensitive polyimides

Appendix D

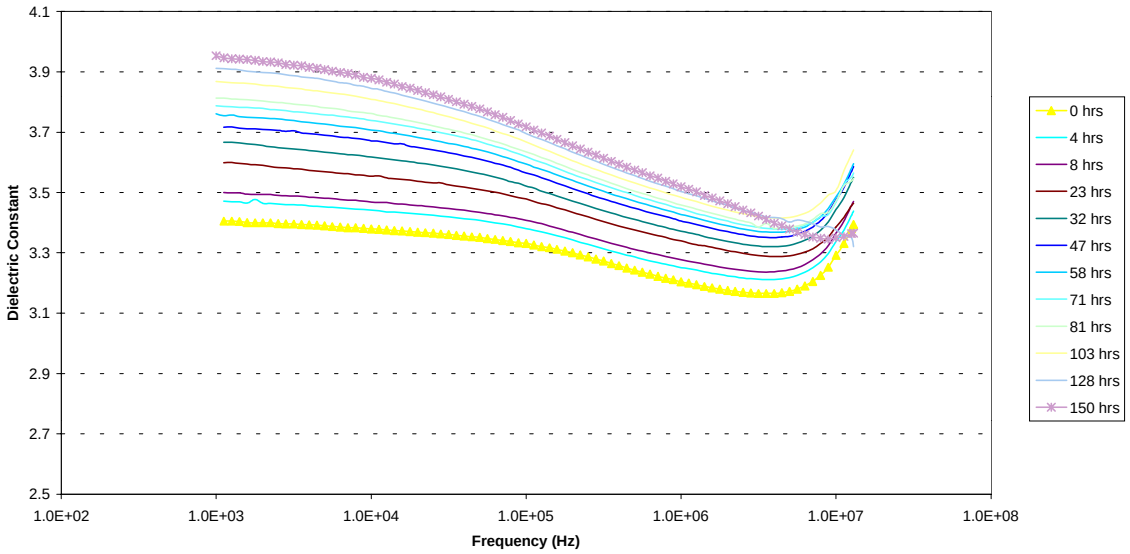


Figure D.1 Variation in ε_r of Cap 1c under 96% relative humidity

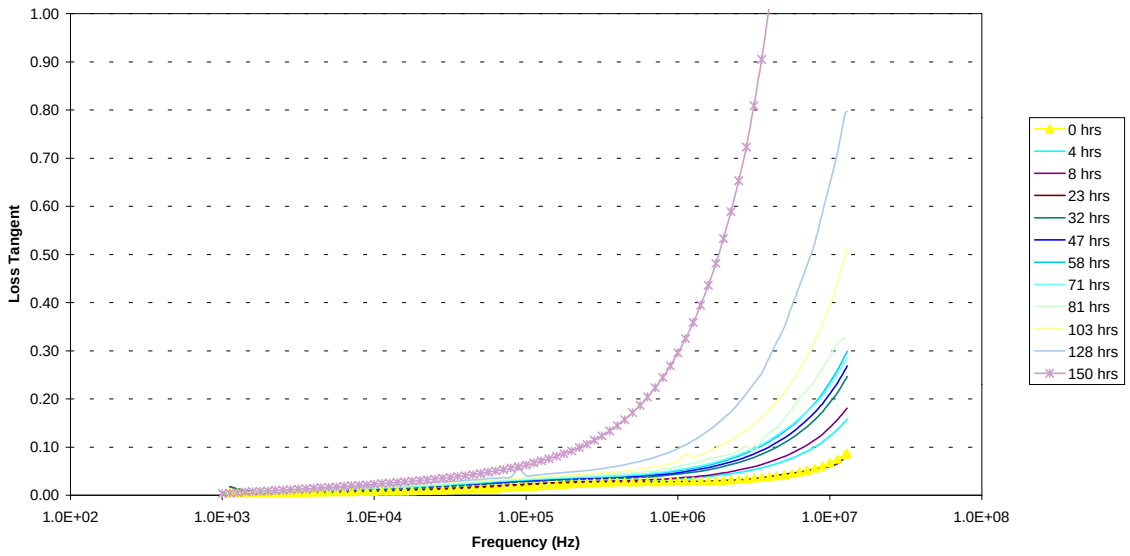


Figure D.2 Variation in tan δ of Cap 1c under 96% relative humidity

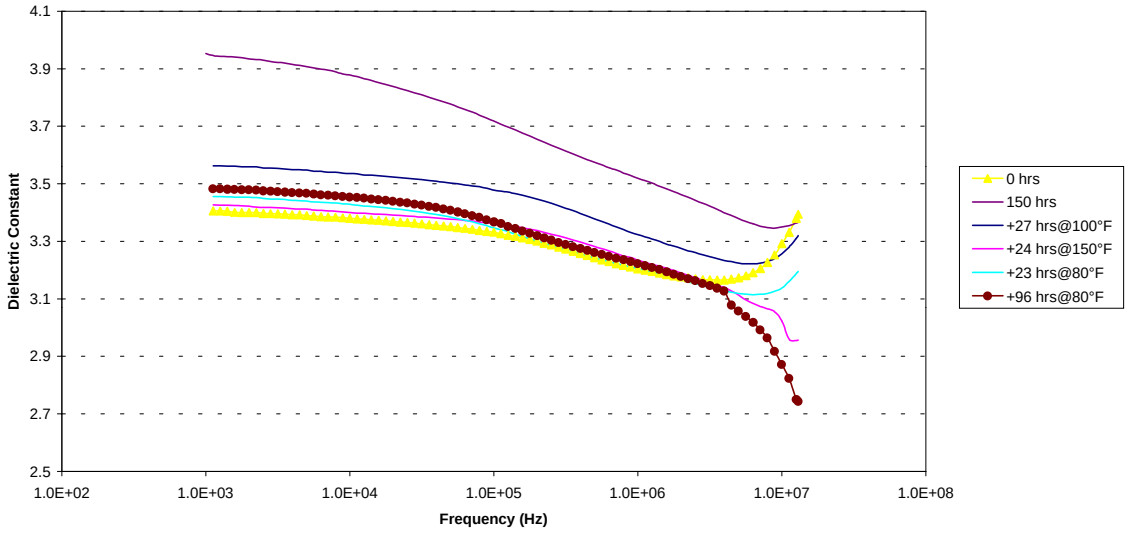


Figure D.3 Variation in ε_r of Cap 1c for humid & post-humid conditions

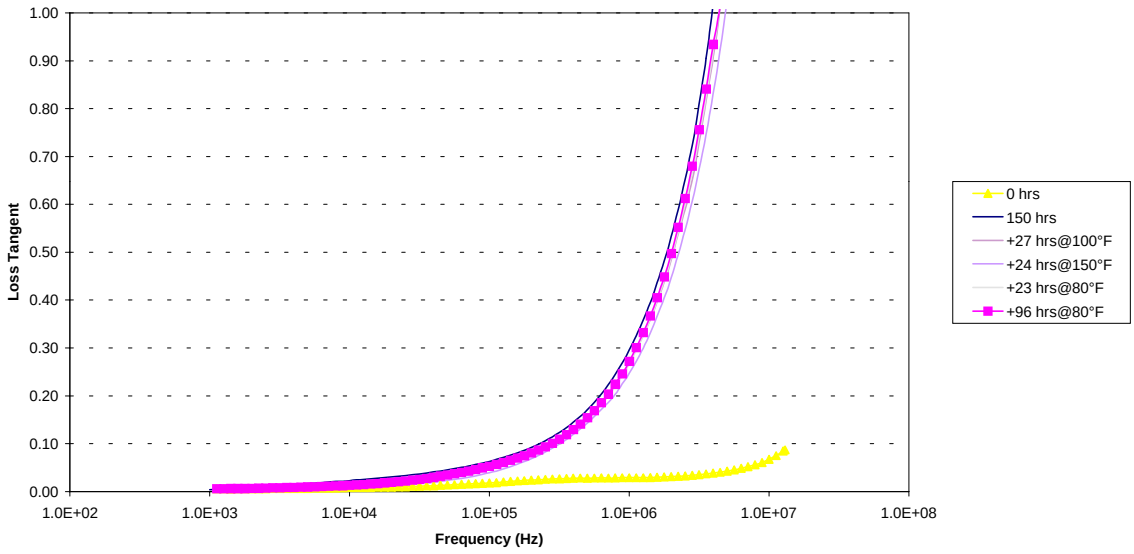


Figure D.4 Variation in tan δ of Cap 1c for humid & post-humid conditions

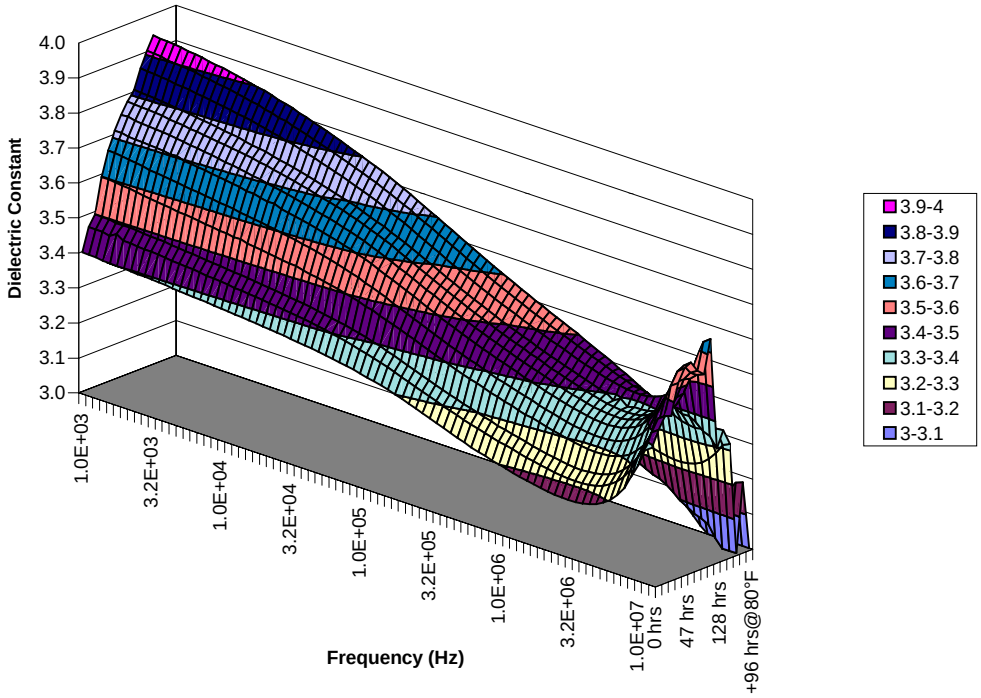


Figure D.5 Variation in ε_r of Cap 1c versus frequency and time

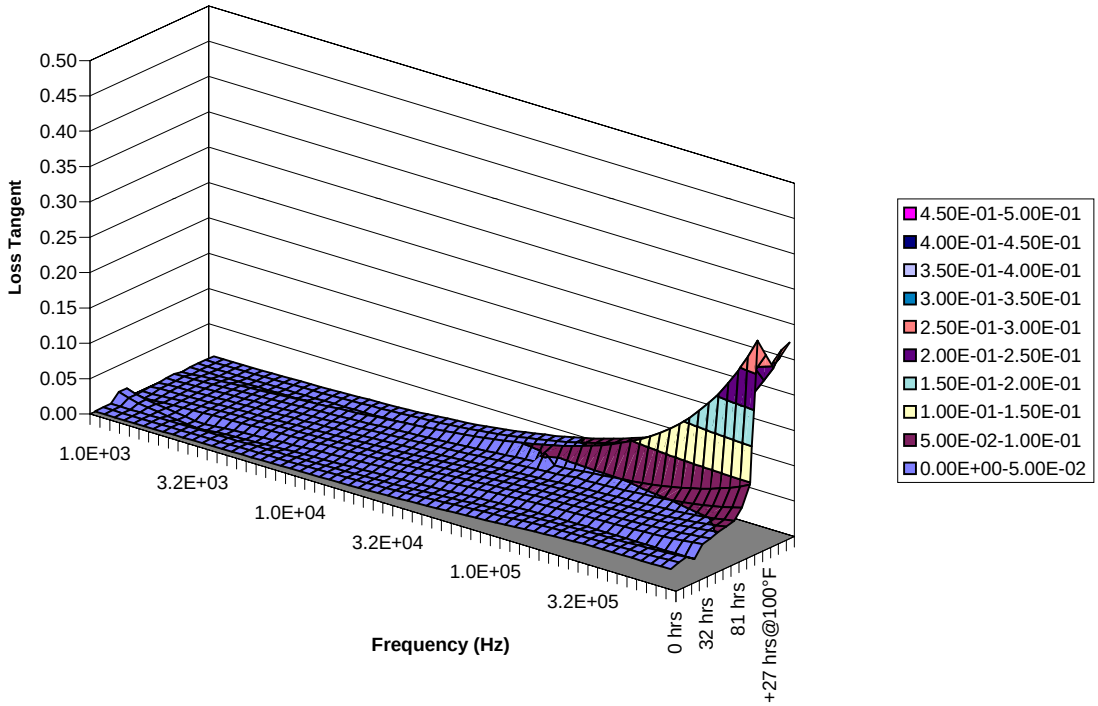


Figure D.6 Variation in tan δ of Cap 1c versus frequency and time

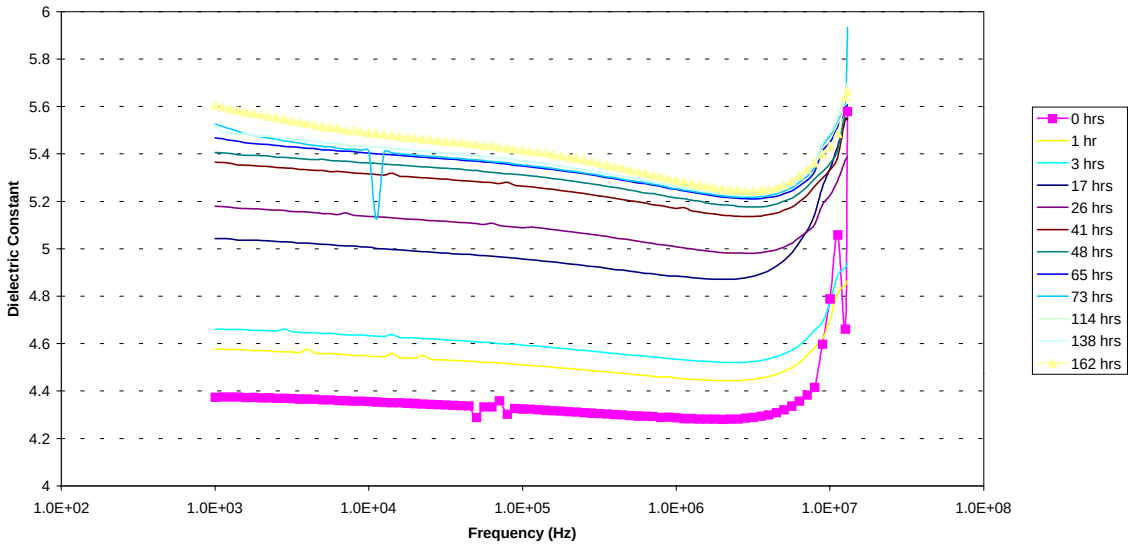


Figure D.7 Variation in ε_r of Cap 5d under 96% relative humidity

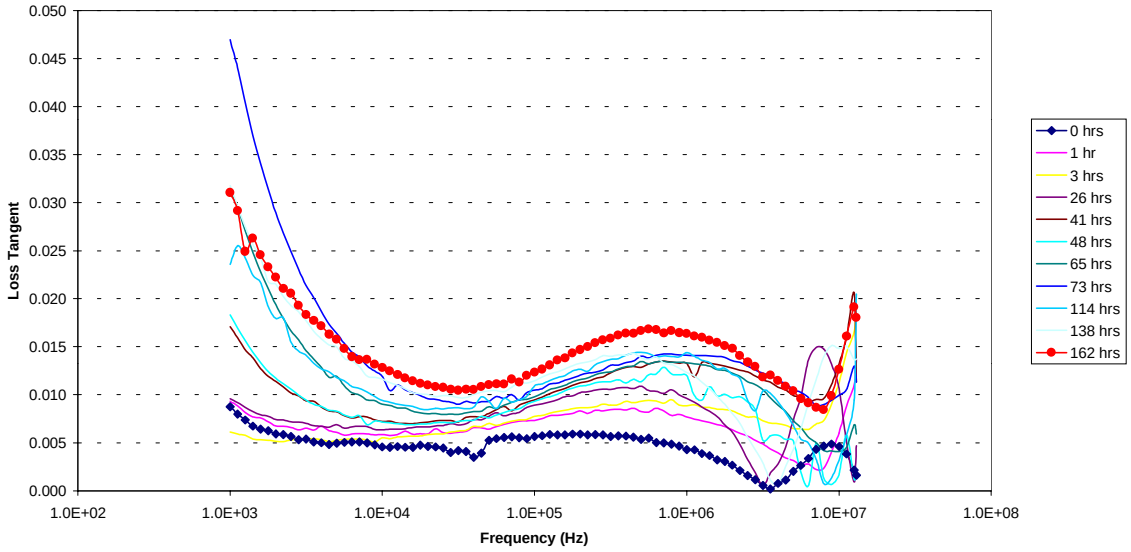


Figure D.8 Variation in tan δ of Cap 5d under 96% relative humidity

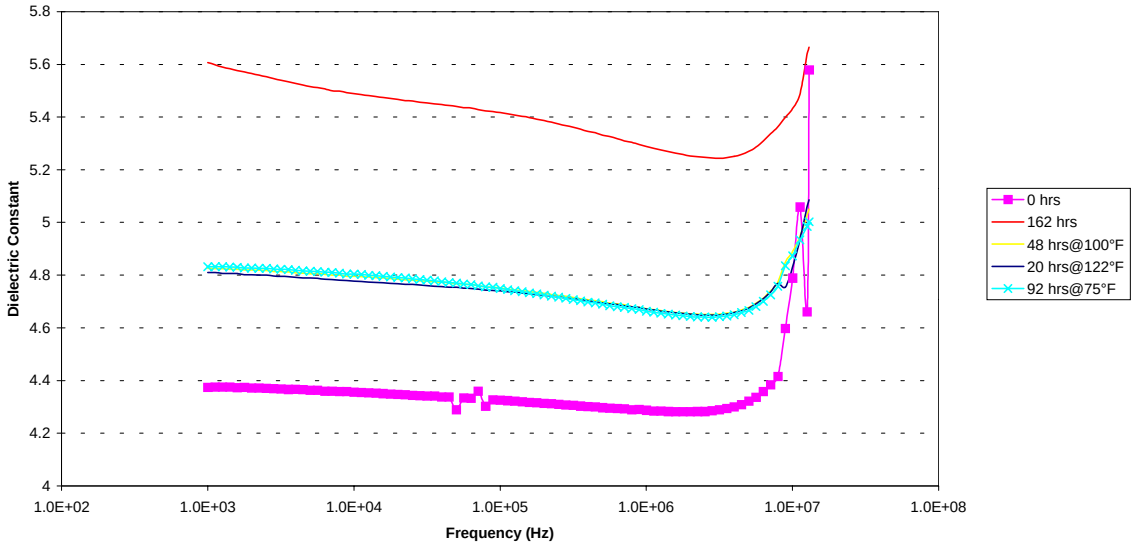


Figure D.9 Variation in ε_r of Cap 5d for humid & post-humid conditions

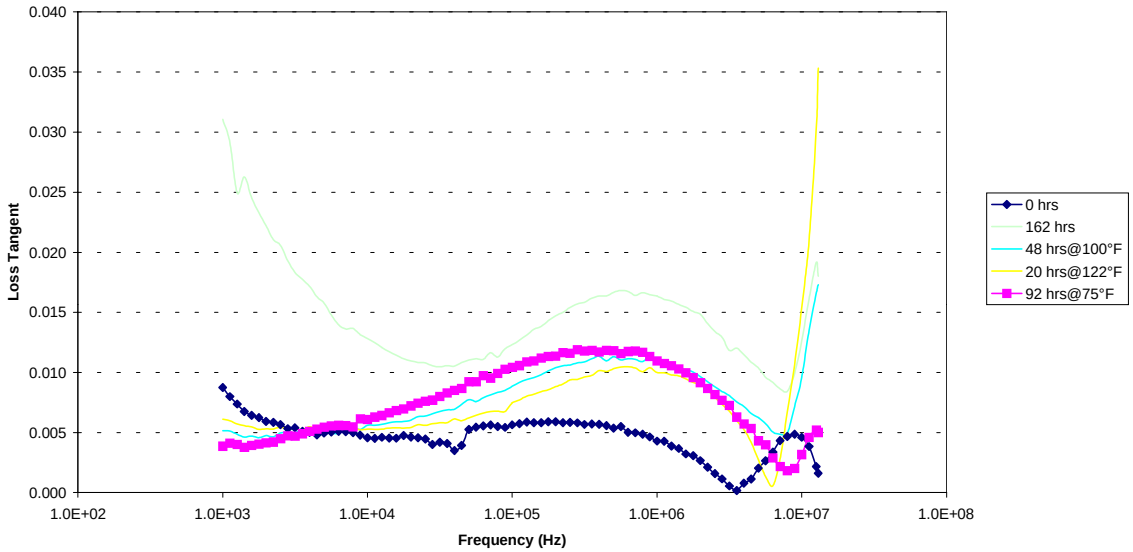


Figure D.10 Variation in tan δ of Cap 5d for humid & post-humid conditions

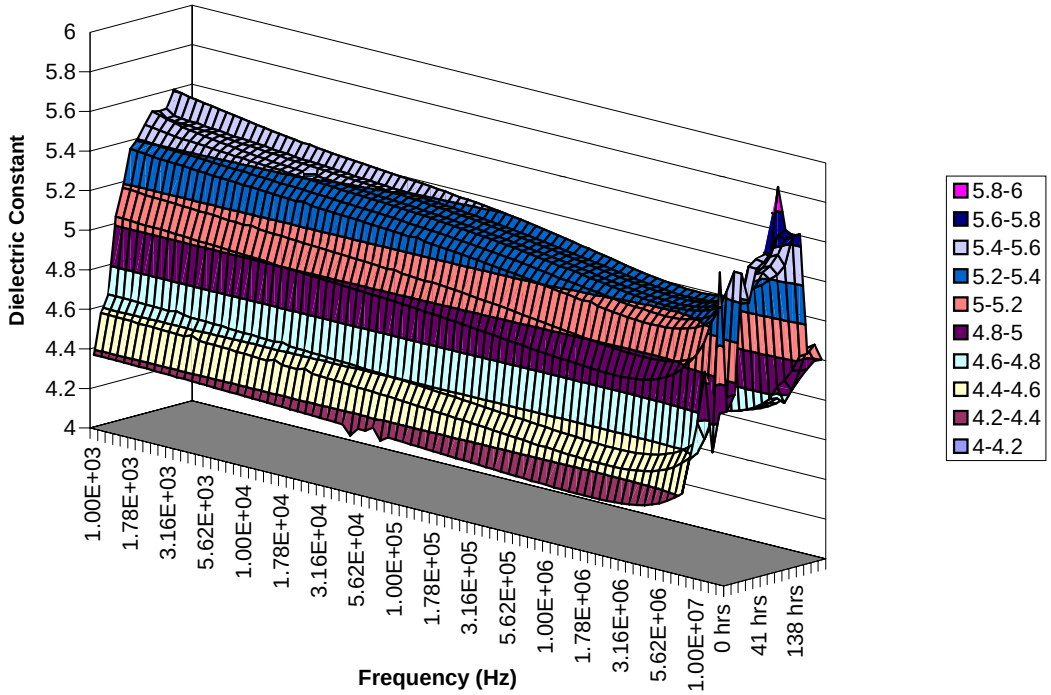


Figure D.11 Variation in ε_r of Cap 5d versus frequency and time

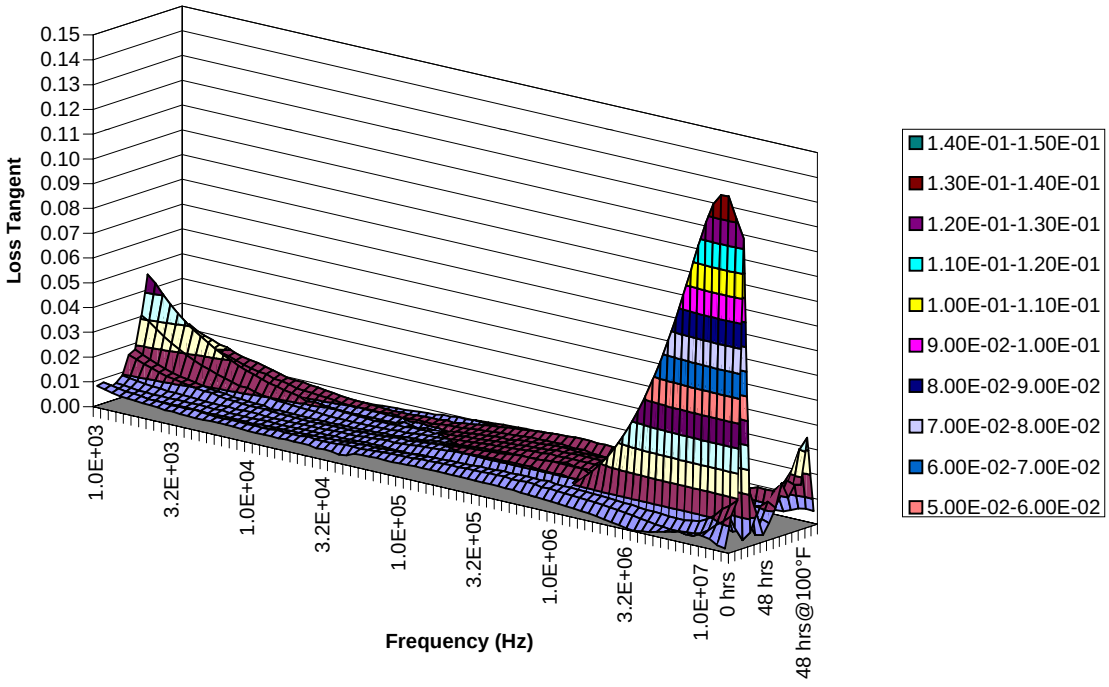


Figure D.12 Variation in tan δ of Cap 5d versus frequency and time

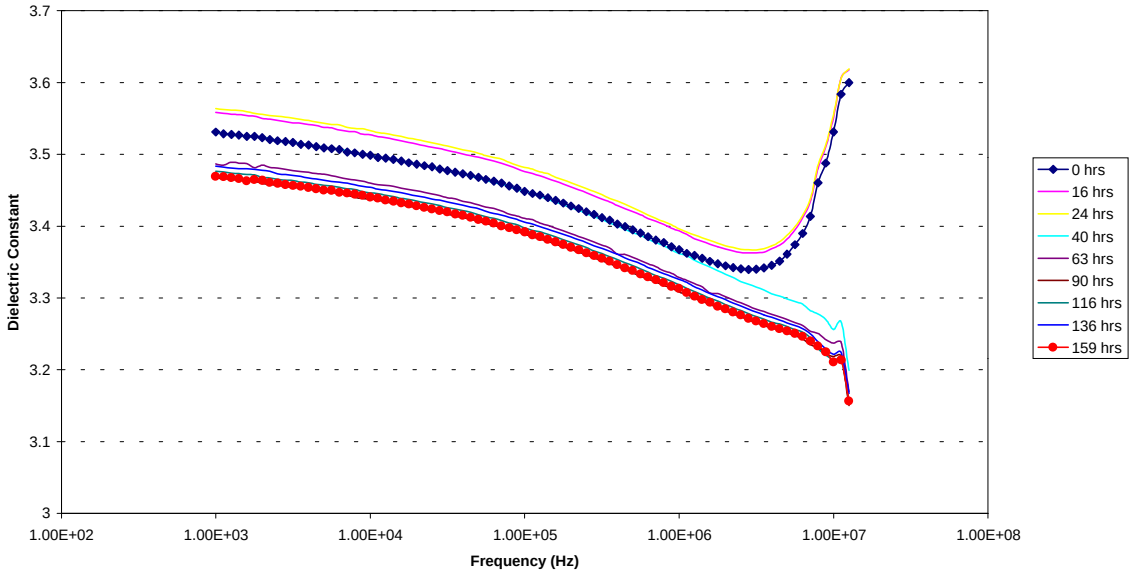


Figure D.13 Variation in ε_r of Cap 3d at 100°F & ambient humidity

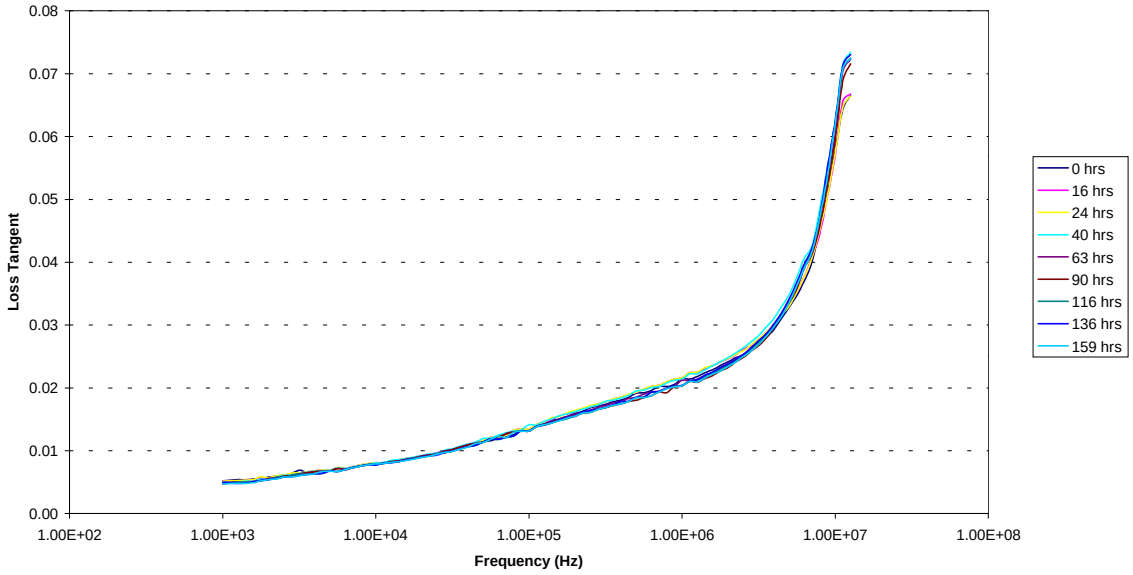


Figure D.14 Variation in tan δ of cap 3d at 100°F & ambient humidity

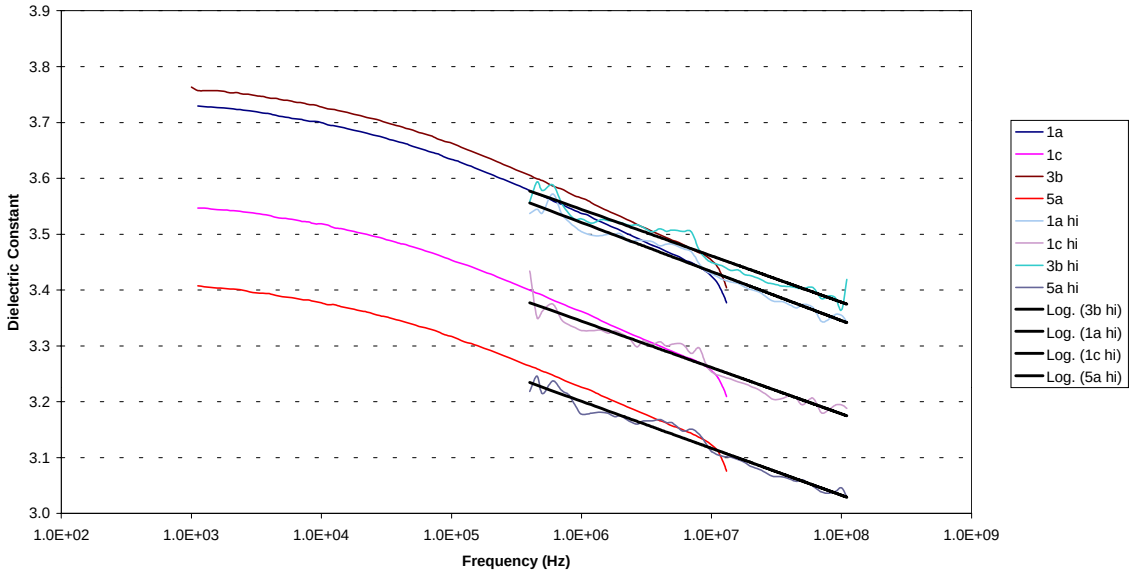


Figure D.15 Measurement variation in ε_r of substrate 1 caps at high frequency

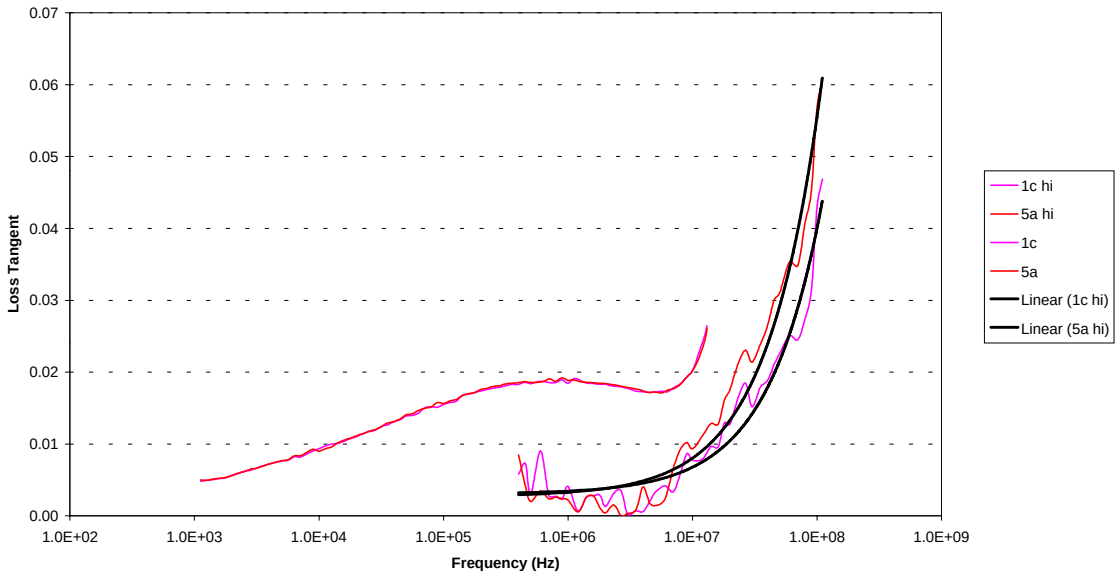


Figure D.16 Measurement variation in tan δ of substrate 1 caps at high frequency

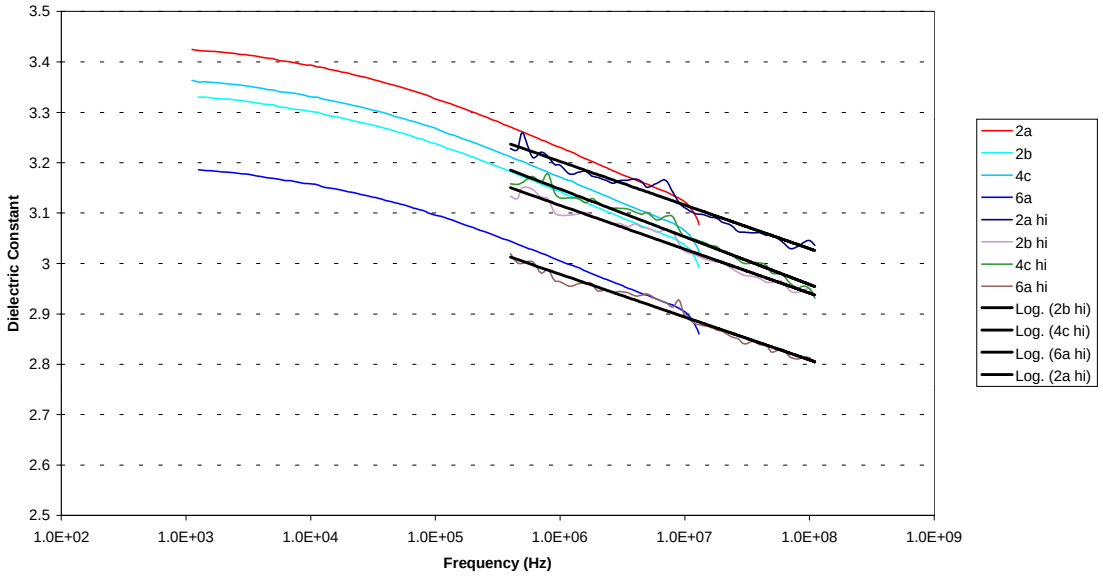


Figure D.17 Measurement variation in ε_r of substrate 2 caps at high frequency

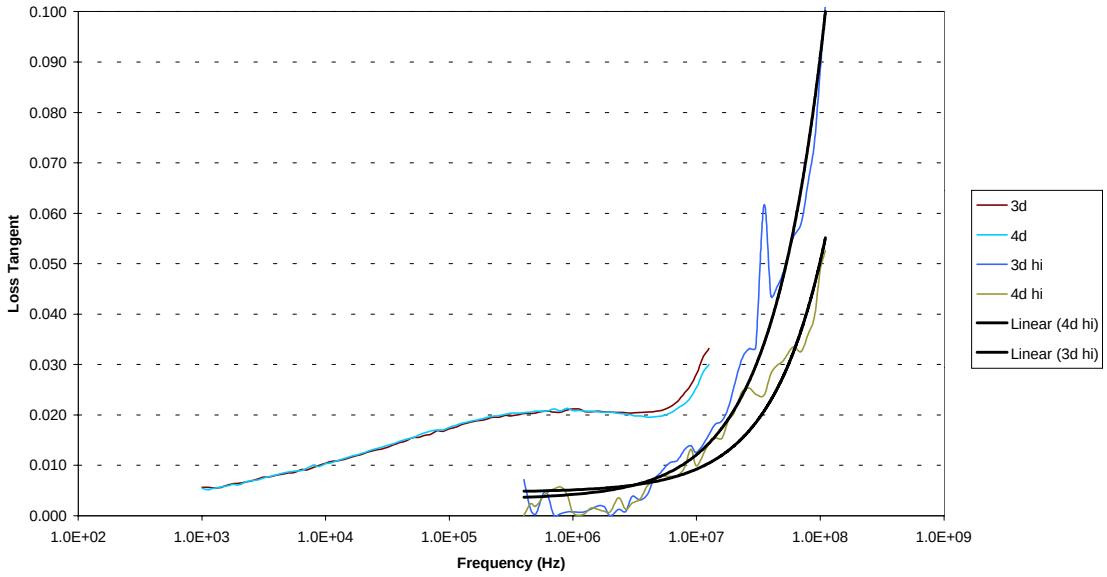


Figure D.18 Measurement variation in tan δ of substrate 2 caps at high frequency

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Vita

Mr. James R. Webster was born in San Diego, CA on May 30, 1969. In the fall of 1987, he joined the freshman engineering class at Virginia Tech. During his sophomore through senior years, he participated in the cooperative education program, working semesters and summers at the Naval Research Laboratory in Washington, D.C. He received the BSEE degree (Cum Laude) from Virginia Tech in May 1992.

After graduating from Virginia Tech, Mr. Webster was employed full-time at the Naval Research Lab, in the Tactical Technology Section of the Naval Center for Space Technology. Some of the projects he was directly involved with included Desert Hammer 92, NTC Training Rotation 94-7 (The Digitized Battalion), and Roving Sands 95.

While working on the technical support staff at Roving Sands, Mr. Webster met his future wife, Elizabeth, and they both returned to Virginia. They were married in December of 1995 and began classes simultaneously at Virginia Tech in the spring of 1996. Mr. Webster is currently finishing the requirements for his MSEE degree in the summer of 1998 and will return in the fall as a PhD candidate.