CHAPTER 3

STUDY AND IMPROVEMENT OF CCM CURRENT-SOURCE SINGLE-STAGE POWER FACTOR CORRECTION CONVERTER

3.1 Introduction

Typical single-stage power-factor-correction converters use an input inductor in series with the line diode rectifier to shape the input current waveform to meet the IEC harmonic current regulation. Depending on the continuity of input inductor current, they can be divided into two groups, the discontinuous current mode (DCM) and continuous current mode (CCM) single-stage PFC (S^2-PFC) converters. For the DCM S^2-PFC converter, the power switch suffers from very high current and voltage stresses. Also the bulk capacitor experiences excessive voltage stresses, especially at high line and light load condition. As a result, the DCM converters normally have low efficiency. Besides, due to the DCM operation, the converters require the use of a big input EMI filter which increases the total size and cost. All of the limitations of DCM S^2-PFC techniques make the CCM S^2-PFC techniques more attractive.

A novel CCM S^2-PFC converter is proposed in [B6, B7]. As discussed in chapter 2, because this converter is using an additional high frequency inductor to achieve CCM input current shaping function, it is called current source (CS) S^2-PFC converter. The circuit is shown in Fig. 3.1.

Compared to the DCM S^2-PFC converters, the CCM S^2-PFC converter is more complicate and the principle of it is not very straightforward. In chapter 2, the general necessary

PFC condition is presented. This chapter gives the detailed study of the CS S^2-PFC converter to further understand it. Also, the design consideration is given in this chapter.

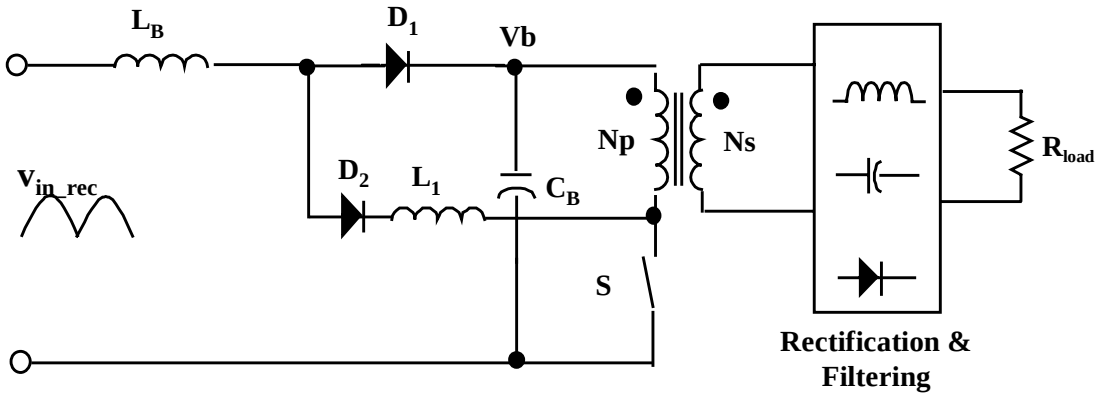


Fig. 3.1 The current source CCM single-stage PFC converter

For universal-line applications, this converter may also has some potential problems to maximize the efficiency, meet PFC specification with acceptable margin and keep the voltage stress on the energy-storage capacitor low. Specifically, this converter has a difficulty to enough margin for the IEC PFC requirement at high line because of the reduced conduction angle of the line current. In this chapter, a new technique which improves the performance of this converter is proposed. This technique employs a low frequency, low cost auxiliary switch to further improve the input current waveform and increases the efficiency. Experiments show the improvements are effective.

3.2 Circuit intuition and design consideration of current source S^2-PFC converter

3.2.1 Operation principle of the current source S^2-PFC converter

As proved in chapter 2, the necessary PFC condition of a S^2-PFC converter with an input inductor is that the node voltage $<v_y>$ must roughly follow the rectified input line voltage. In the

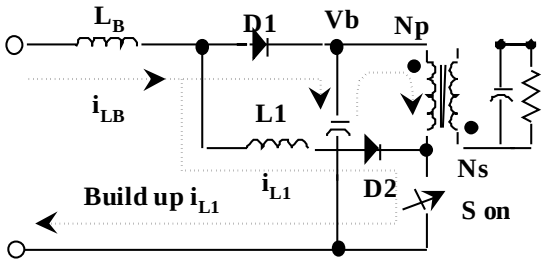
current source S^2-PFC converter, an additional high frequency inductor is used to force the voltage $<v_y>$ to meet this condition and therefore a good input current waveform is achieved.

Figure 3.2 (a) – (d) shows the detailed operating modes of the CS S^2-PFC converter with a flyback output stage. There are four operating modes during one switching cycle.

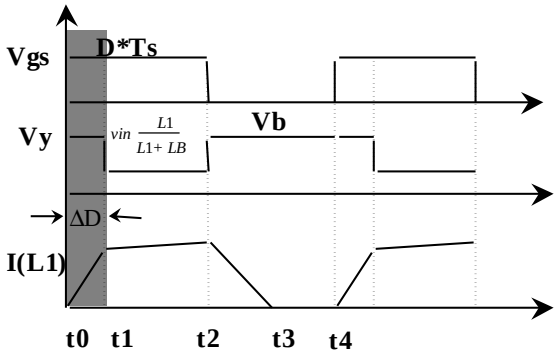
Mode 1 [t0, t1]: Before t0, the switch is off and the inductor current i_{LB} is discharged by the bulk capacitor voltage Vb. The additional inductor current i_{L1} is zero. The flyback transformer is providing energy to the output. At t0, the switch S is turned on. So the additional inductor L1 is charged by the bus voltage Vb and the current i_{L1} is built up. The input inductor current i_{LB} commutates from D1 to D2 until the current i_{L1} is equal to the current i_{LB}. The commutation duty cycle ΔD during t0-t1 is given in Eq. (3.1). It shows that when the instantaneous input voltage increases, ΔD also increases. Therefore, in mode 1, the instantaneous voltage vy remains as Vb though S is turned on. The area of vy*ΔD increases with the increase of the line voltage. At the same time, the flyback transformer is charged by the bulk capacitor voltage Vb.

$$\Delta D = D - \frac{(1+\frac{L1}{L_B})(1-\frac{v_{in\_rec}}{Vb})}{1+\frac{L1}{L_B}\cdot(1-\frac{v_{in\_rec}}{Vb})} \qquad (3.1)$$

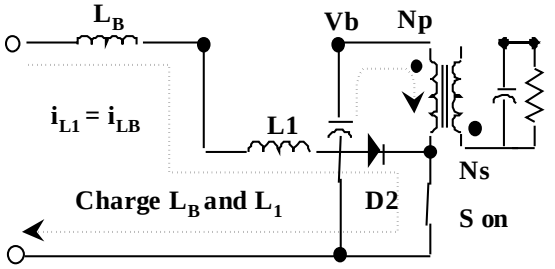
Mode 2 [t1,t2]: At t1, i_{L1} reaches i_{LB}, so all the L_B current will go through the L1 path and the diode D1 is off. Inductor L_B and L1 are in series and charged together by the rectified input voltage v_{in_rec}. So the rectified input voltage is divided by them and the instantaneous voltage $vy = v_{in\_rec}*(L1/(L1+L_B))$. Besides, the flyback transformer is still charged by the bulk capacitor voltage Vb.



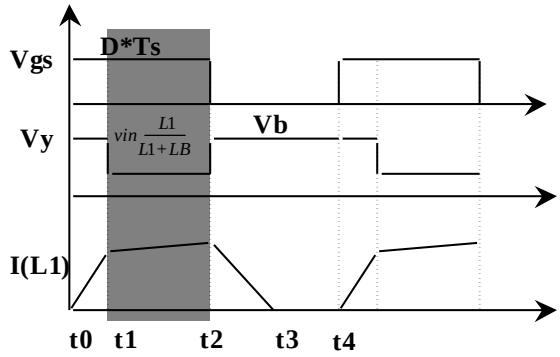
Mode 1. t0 - t1



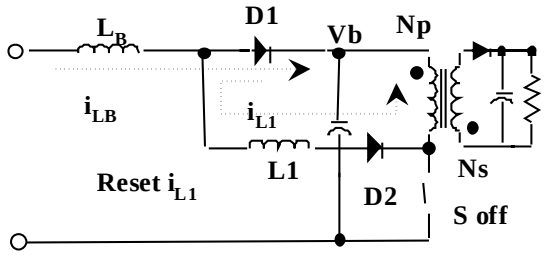
(a) Mode 1. Current commutation from L_B to L1



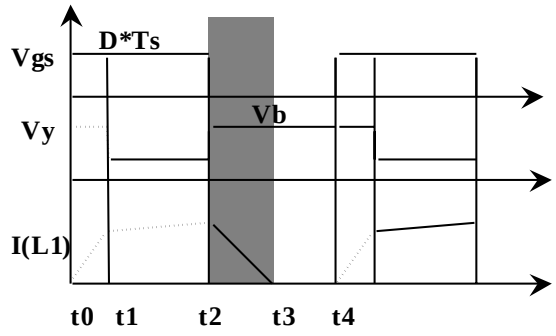
Mode 2. t1 - t2



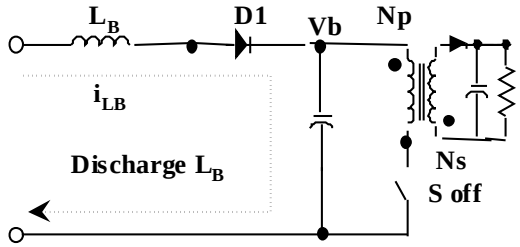
(b) Mode 2. Charge L_B and L1



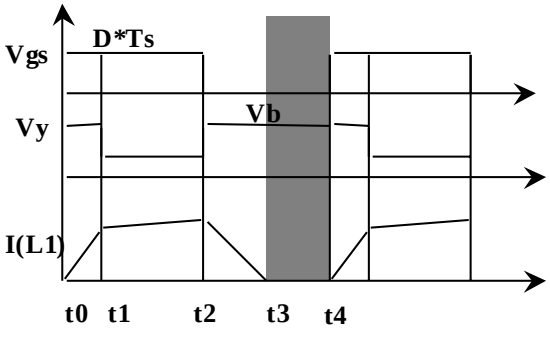
Mode 3. t2 - t3



(c) Mode 3. Discharge L_B and L1



Mode 4. t3 - t4



(d) Mode 4. Discharge L_B

Fig. 3.2 Operating modes of current source single-stage PFC converter (flyback output)

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Mode 3 [t2, t3]: At t3, switch S is turned off. The additional inductor L1 is discharged by the reflected output voltage on the transformer primary side winding. i_{L1} decreases and therefore i_{L1} will be less than i_{LB}. The difference current i_{LB}-i_{L1} goes through D1 to the bus capacitor and the instantaneous voltage vy = Vb. The input inductor L_B is discharged by Vb-V_{in_rec}. Normally, the discharge voltage on L1 is much larger than the discharge voltage on L_B, so i_{L1} decreases much faster than i_{LB}. At t=t3, i_{L1} reach zero. During mode 3, the flyback transformer is delivering energy to the output.

Mode 4 [t3, t4]: During this time interval, the inductor L1 current is zero. The input inductor L_B is discharged by the bus capacitor voltage and the flyback transformer is delivering energy to the output. This mode will end when S is turned on again, and then the circuit goes back to mode 1.

Based on the operating modes, we can see that during mode 1 and mode 2, the inductor L1 provides vy additional instantaneous value because of the commutation of inductor current and the division of rectified input voltage. The average value of vy is given in Eq. 3.2.

$$< vy >= Vb \cdot (1 - D) + [Vb \cdot \Delta D + v_{in\_rec} \cdot \frac{L_B}{L_1 + L_B} \cdot (D - \Delta D)] \qquad (3.2)$$

Equation 3.2 shows that while the instantaneous rectified input voltage v_{in_rec} increases, vy will also increase. Therefore, this converter can meet the necessary PFC conditions and it is possible for this converter to have a good input power factor.

However, the necessary PFC condition is just a quite rough condition to give the intuition that this converter is able to shape the input current. It does not show how good the input current can be and what the design consideration is. In order to further understand and optimally design this converter, further study is critical.

Another important issue of S^2-PFC converters is the bus capacitor voltage stress. Normally, DCM S^2-PFC converters without bus voltage feedback will potentially have high voltage stress because of the unbalance between the input and output power [B4, B15]. When the converter output power decreases from heavy load to light load, the input power does not decrease instantaneously. It results in a high bus capacitor voltage to depress the input power. So a bus-voltage-feedback scheme is important in limiting the bus voltage stress. However, for CCM S^2-PFC converters, this problem is much less severe than in DCM case. As shown in Fig. 3.3, when the S^2-PFC converter is working in heavy load, even at high line input, the input inductor current has a large CCM mode time interval during each half line cycle. If the output power decreases from heavy load to light load, the input current will change from CCM to DCM. Therefore, the input power already decreases a great deal even without the increasing of bus voltage or bus-capacitor-voltage feedback scheme. For example, in the current source S^2-PFC converter, the bus voltage is just around 430 Vdc while it works in the 265 Vac line and light load condition. The voltage stress is not high and a 450 V capacitor can still be used for universal line applications though the voltage margin is small.

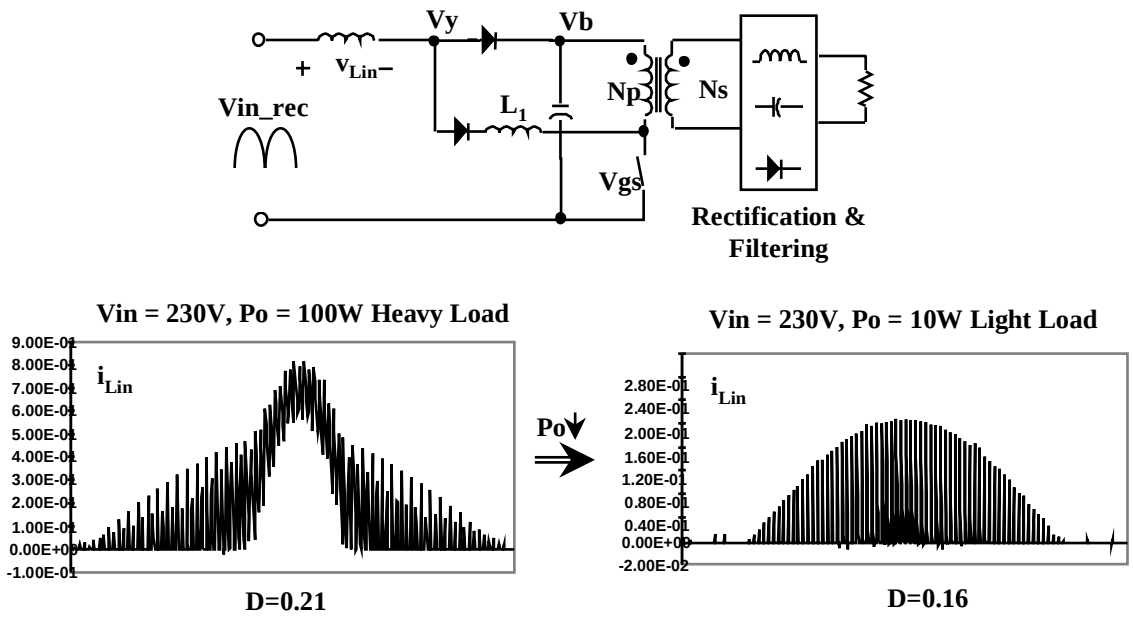


Fig. 3.3 Input current changes from CCM to DCM mode while output power decreases. Vb is limited.

In order to increase the capacitor voltage margin and also the overall efficiency, similar to the DCM S^2-PFC converters, a bus-voltage-feedback winding can be added in the CS S^2-PFC converter. Figure 3.4 shows one implementation of the voltage feedback scheme. A tapped transformer is used here to further reduce the bus capacitor voltage stress to be even lower than 400 V for universal line input. Also, the tapping winding N1 provides a direct-energy-transfer from the input to the output stage, resulting in a higher efficiency. Similar as in the DCM S^2-PFC converters, the drawback of the feedback winding N1 is that it introduces the dead input current conduction angle and hurts the input power factor. Further discussion and improvement about the tapping winding will be given in the section 3.3.

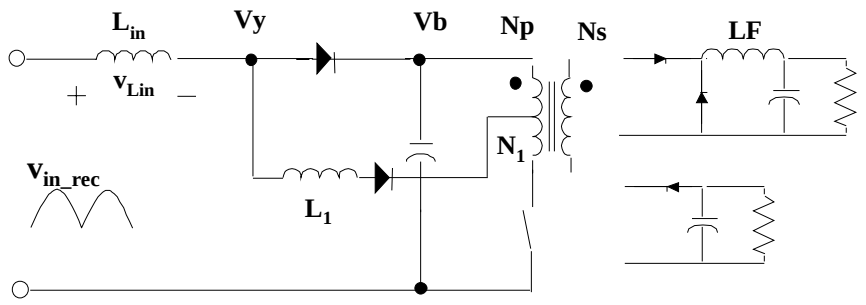


Fig. 3.4 Current source single-stage PFC converter with tapping winding

In conclusion, the CS S^2-PFC converter has good input power factor because the additional inductor L1 can make vy roughly follow the input voltage. However, further study of this converter need to be done.

3.2.2 Circuit intuitions of CS S^2-PFC converter

The necessary PFC condition explains that L1 can help the CS S^2-PFC converter to shape the input current. During every line cycle, the input inductor current waveform always has two parts: the DCM part and CCM part. As shown in Fig. 3.5 (b), when the instantaneous input voltage is low, the input current is also low and therefore the inductor current is in DCM mode. With the increase of instantaneous input voltage, the inductor current also increases and enters the CCM part. Figure 3.5(c) shows the switching waveform of the DCM operation at time ta and Fig. 3.5(d) shows the switching waveform of the CCM operation at time tb. The shadowed area is the additional part of vy introduced by the induction L1. Comparing (c) and (d), it is clear that L1 has a strong effect on vy in CCM conduction modes. Therefore, the PFC function of L1 is stronger in the CCM part than in the DCM part. However, in every line cycle, the input inductor

current always has both a DCM part and a CCM part. The waveform shows that in CS S^2-PFC converter, the DCM part current is very small compared with the CCM part current. The different effect of L1 causes the distortion of the input current and hurts the input power factor.

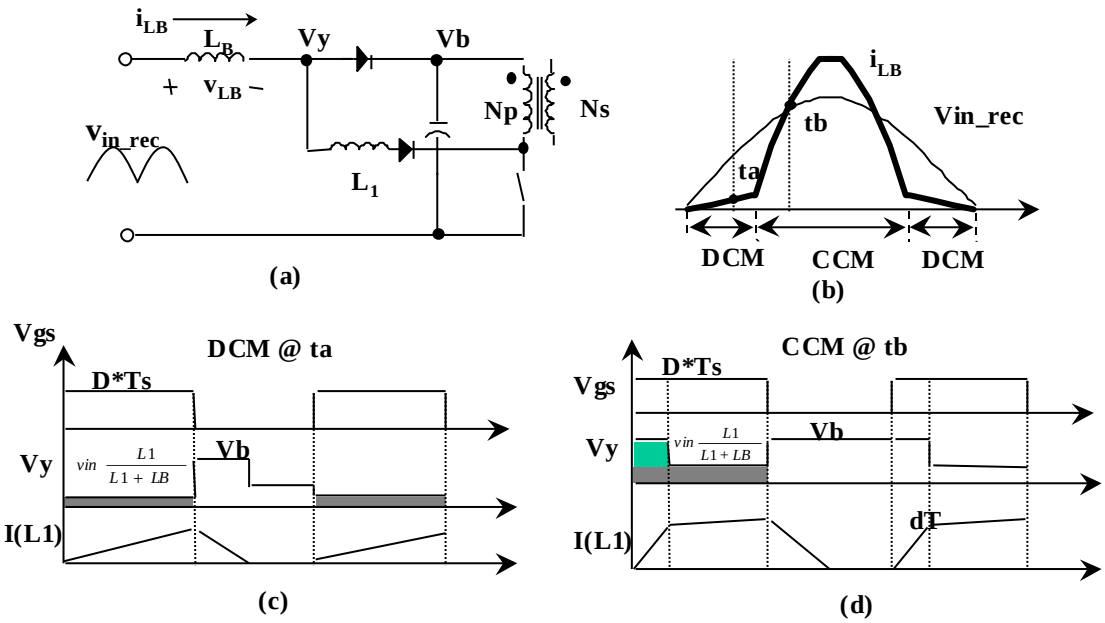


Fig. 3.5 L1 has a strong effect in the DCM input current part

This conclusion is even clearer as shown in Fig. 3.6. It shows the different input current waveforms and THD for the same converter operates at different input voltages. As shown in Fig. 3.6 (a), when the input voltage is at the 90 Vac low line, during most of the time the DCM angle is small and the input inductor mostly works in CCM mode. The current distortion is small and the input current THD is as low as 43.17%. However, if the converter operates at high line voltage as 230 Vac, the DCM angle increases a lot and the current distortion is much more severe. The THD is as high as 77.49% as in Fig. 3.6(b). There is a potential problem that the

input current may not meet the IEC current harmonics standard. From these two figures, it is clear that a large DCM angle (small CCM) angle will hurt the input power factor. Therefore, it is desirable to choose the inductor values of L_B and L1 to get a larger CCM angle.

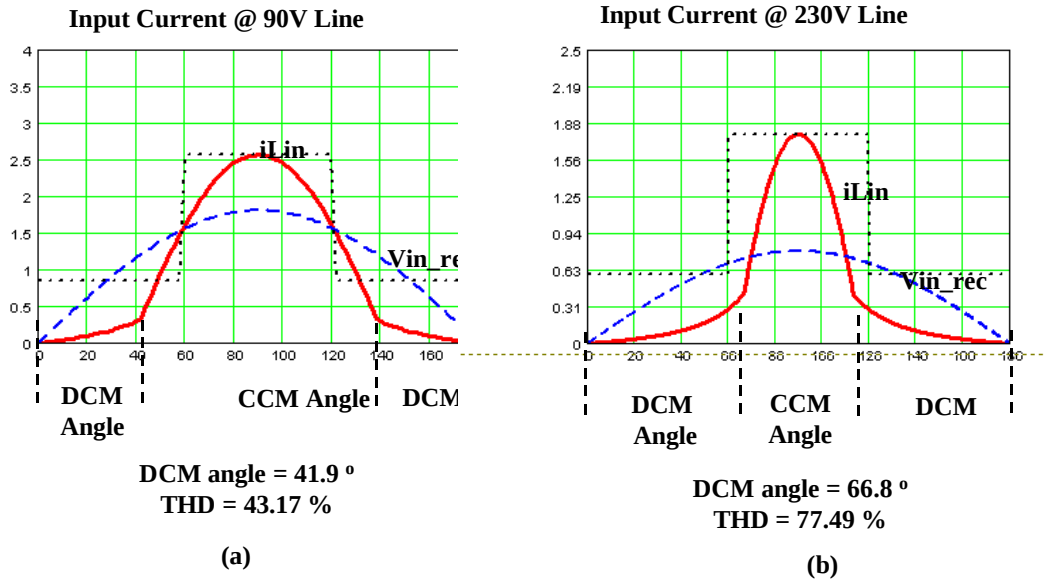


Fig. 3.6 Input current waveforms of CS S^2-PFC converter
(a) 90 Vac low line. (b) 230 Vac high line

As far as the design consideration is concerned, the most important PFC components here are the input inductor L_B and the additional inductor L1. The relationship between the inductance of these two inductors will strongly affect the input power factor. As shown before, L1 is an additional inductor used to help the input power factor. However, in fact L1 is not just a small inductor if the low input current THD is required. It is necessary to look at L1 first to understand how the change of L1 can affect the input power factor.

The first direction to look at this problem is from the point of view of satisfying the necessary PFC condition. As shown before, L1 provides an additional part of vy to meet the PFC condition. Figure 3.7 shows that a larger L1 will provide larger shadowed additional area of vy. This means a larger L1 will provide a stronger relationship of <vy> in direct proportion to v_{in_rec}. So a larger L1 is desirable.

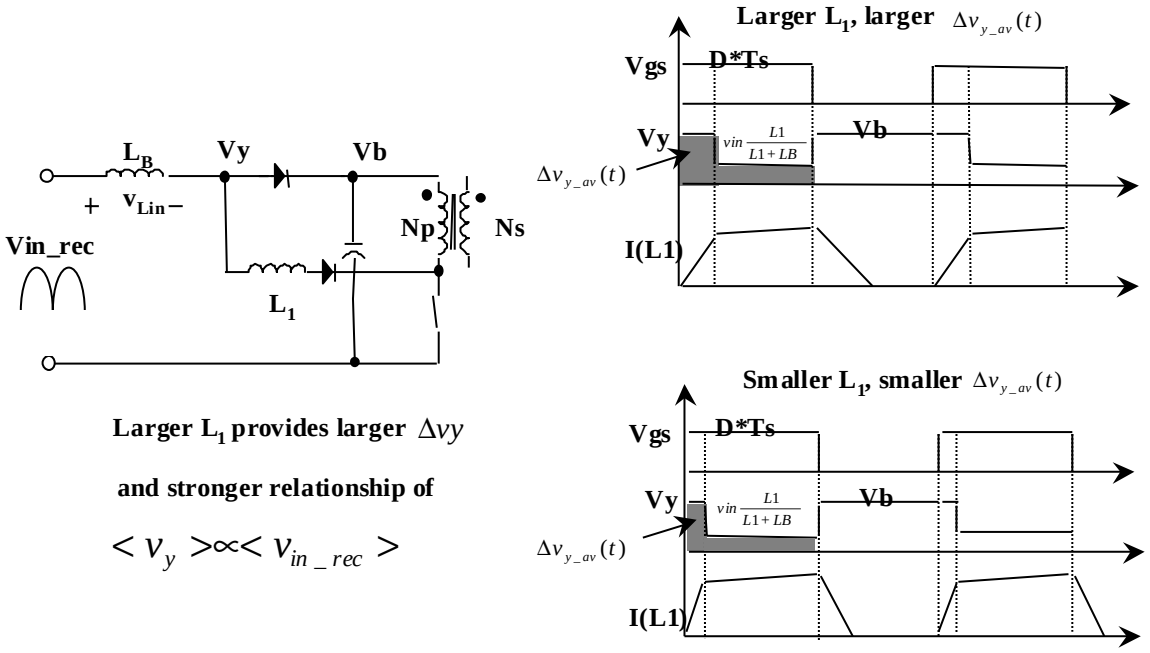


Fig. 3.7 Larger L1 improve the input power factor in CCM mode (from the point of view of satisfying the PFC condition)

However, L1 can not be too large. In a proper operation, L1 is always working in the DCM mode and therefore there will be a long commutation time. A longer commutation time will help vy have a larger additional area for it to have a stronger relationship with the input voltage. As shown in Fig. 3.8, if the L1 is too large, i_{L1} will eventually be the CCM current. The commutation time will be reduced a great deal because the initial value of i_{L1} is not zero. It will

weaken the proportional relationship between <vy> and v_{in_rec}, resulting in a lower input power factor.

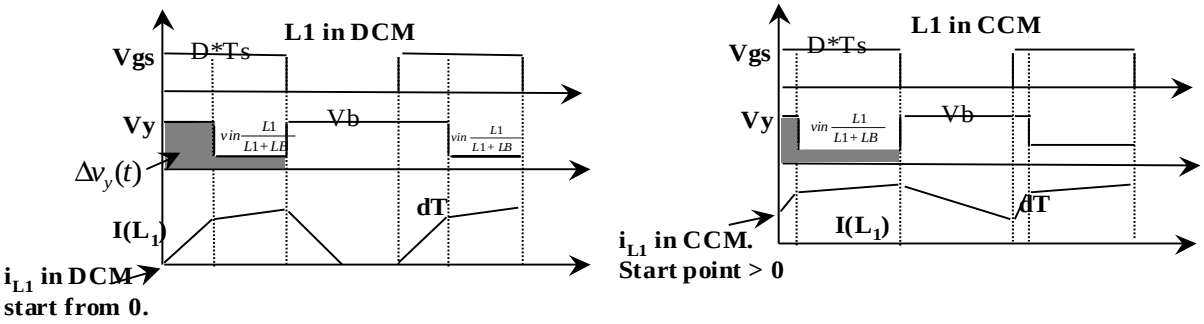
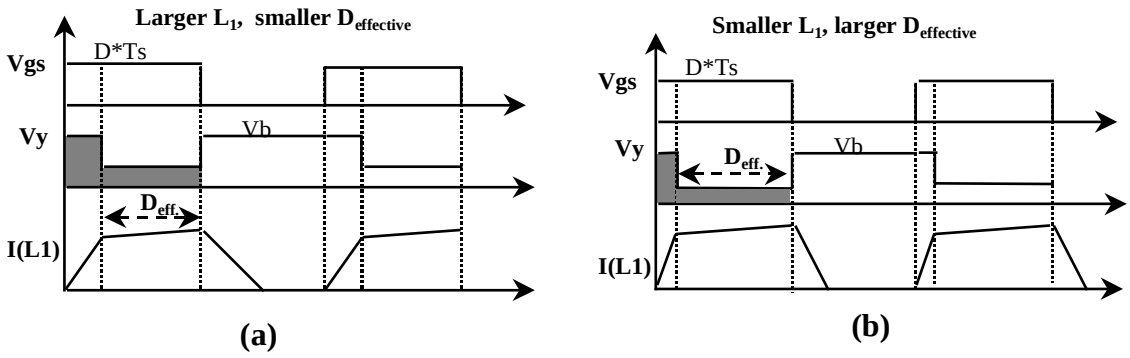


Fig. 3.8 L1 too large and it will enter CCM mode, hurts PFC

Another direction to look at how the value of L1 affects the input current is from the point of view of the DCM/CCM conduction angle. As discussed before, a larger CCM angle will be helpful in getting a better input current waveform in the CS S^2-PFC converter. Figure 3.9 (a) shows that in the CS S^2-PFC converter, the effective duty cycle D_{eff} is actually smaller than the control duty cycle because of the current commutation interval t0-t1. As shown in Fig. 3.9 (a) and (b), a larger L1 means a longer commutation time interval and a smaller effective duty-cycle D_{eff}. In a normal CCM boost converter, the bus capacitor voltage is Vb = v_{in_rec}/(1-Deff). A smaller D_{eff} means lower Vb. Although a CS S^2-PFC converter is not exactly a CCM boost converter, a smaller D_{eff} will still provide lower Vb. On the other hand, a lower Vb means the reset voltage on L_B will be lower when switch S is turned off. As a result, L_B is more likely working in CCM mode. Based on the above analysis, it can be concluded that a larger L1 will increase the CCM angle and improve the input power factor.



$$Vb = \frac{< v_{in\_rec} >}{1 - D_{eff}}.$$

Fig. 3.9 Larger L1 reduce the effective duty cycle Deff

Again, L1 cannot be too large. If L1 is too large, the effective duty cycle D_{eff} will be too small such that Vb can be even less than the peak input voltage. Therefore, there will be no adequate reset on LB, resulting in a large current distortion as shown in Fig. 3.10. So from the point of view of improving the CCM angle, a larger L1 is helpful but L1 cannot be too large again.

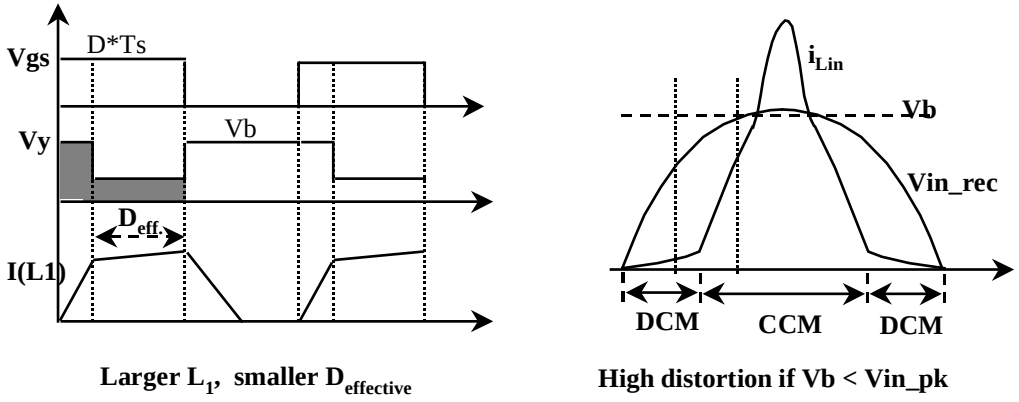


Fig. 3.10 L1 too large will make Vb be lower than Vin_pk and hurt the input current waveform

In conclusion, a larger L1 will help to shape the input current to have a lower harmonics but L1 can not be too large.

Generally, it is always true that a larger L_B will help the input power factor. It is because a larger L_B means a larger input filter and also a larger CCM conduction angle. It is always good to have a larger L_B if the input power factor is the only consideration. However, in practice a over-designed input inductor means high cost and large size for the given circuit specification. Therefore, a better way to optimize the design is to limit the total PFC magnetic cost and find the best inductance distribution between L1 and L_B to get the lowest input current THD and bus voltage stress. Figure 3.11 shows this design optimization approach.

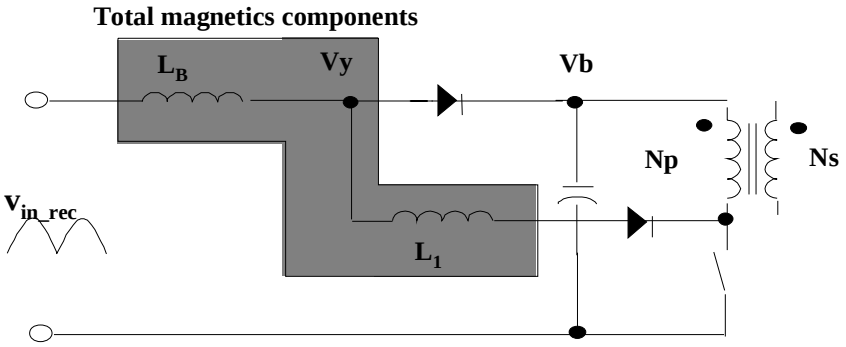
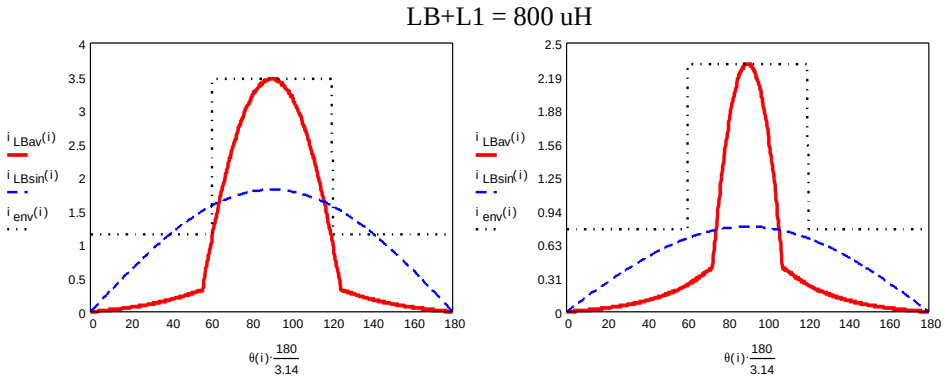


Fig. 3.11 Design optimization approach:
fixed the total PFC inductance and find the best distribution.

Figure 3.12 shows an example that even when the total inductance of L_B+L1 is fixed, a different distribution will change the THD and input power factor significantly. Therefore, it is necessary to find the optimal ratio between L1 and L_B to get the best performance with a similar cost.

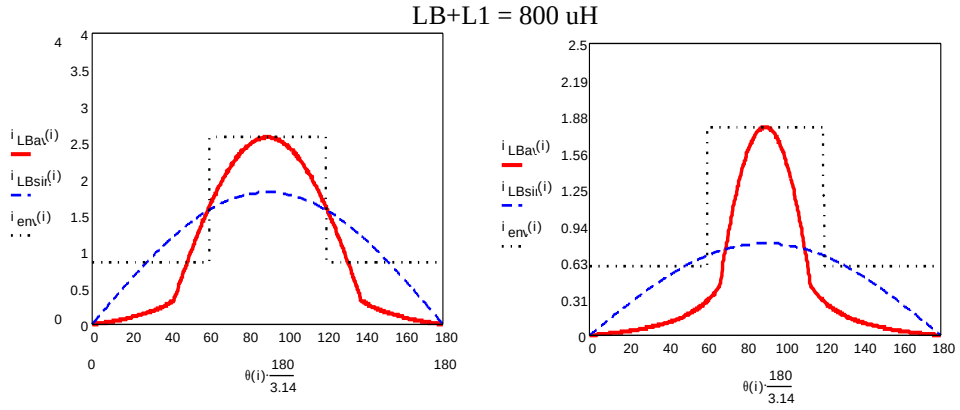
Since the CS S^2-PFC converter has complicated operating modes and it is very difficult to derive the close-form mathematical equations to solve this circuit, close loop circuit simulation is used to find the optimal $L1/L_B$ distribution. To simplify the problem, an example specification is given for the CS S^2-PFC converter. Because the high line THD of CS S^2-PFC converter is worse than the low line THD in this converter, the design optimization focuses on the high line 230 Vac case. In the example, the input voltage is universal line from 90 – 265 Vac and the output is 5 Vdc / 100 W.



THD = 68.9 @ Low Line (90Vac)

THD = 97.8 @ High Line 265Vac

(a) LB/L1 = 700uH/100uH



THD = 43.1 @ Low Line (90Vac)

THD = 77.5 @ High Line (265Vac)

(b) LB/L1 = 500uH/300uH

Fig. 3.12 Inductance distribution between LB and L1 affects the input current THD

As the first step, the total inductance is chosen as L_B+L1 = 1 mH which is a reasonable value based on the simulation when the switching frequency is 100 KHz. Figure 3.13 shows the curves obtained from a group of simulations. It is for the high line 230 Vac input and heavy load output case. Figure 3.13 (a) shows the relationship between the input current THD and the inductance ratio L1/(L1+L_B). There is a plat bottom region where the THD is relatively low. If the 5% THD design margin is chosen, then there will be a design range of inductance ratio for low input current THD. The inductance ratio of L1/(L1+L_B) is from 0.33 to 0.5 in this case. Figure 3.13 (c) shows the relationship between the DCM angle and the inductance ratio L1/(L1+L_B). Compared it to Fig. 3.13(a), it is clear that these two curves have a similar shape. It verifies the intuition that the DCM angle will affect the input power factor. Figure 3.13(c) shows the relationship between the bus capacitor voltage and the inductance ratio. It shows that with the increase of L1, the bus voltage decreases and it can be even lower than the peak input voltage which is 325 V here. Generally speaking, a lower bus voltage means less voltage stress on the power switch and a higher converter overall efficiency. So a lower bus voltage is desirable as long as the input power factor is not good enough. Considering both Fig. 3.13 (a) and (c), the optimal point of inductance ratio L1/(L1+L_B) is about 0.5.

Figure 3.14 shows that the same converter works at 100 Vac low line input. Figure 3.14 (a) shows that the CS S^2-PFC converter has much lower input current THD at low line than it has at high line. Also, the relationships between THD, DCM angle, bus voltage and the inductance ratio are similar as in the high line case. However, because the CS S^2-PFC converter can easily meet the PFC regulation at low line, so the study will only focus on the worst case, i.e., the high line input voltage case.

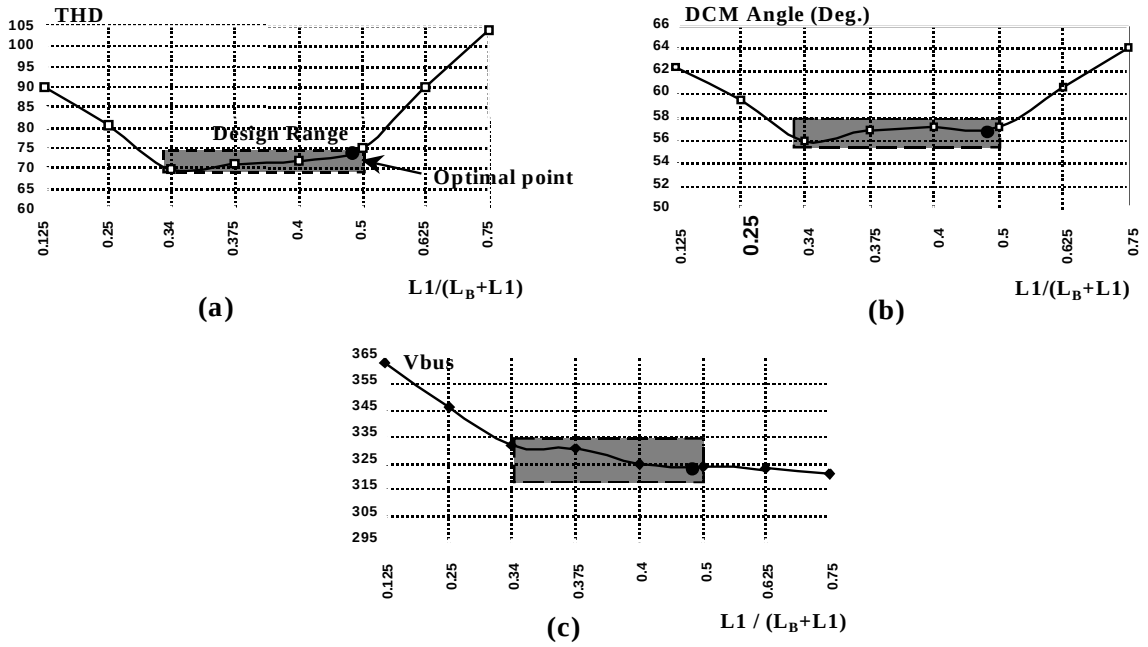


Fig. 3.13 Different inductance distribution @ 230 V line, heavy load ($L1+L_B$ = 1 mH)

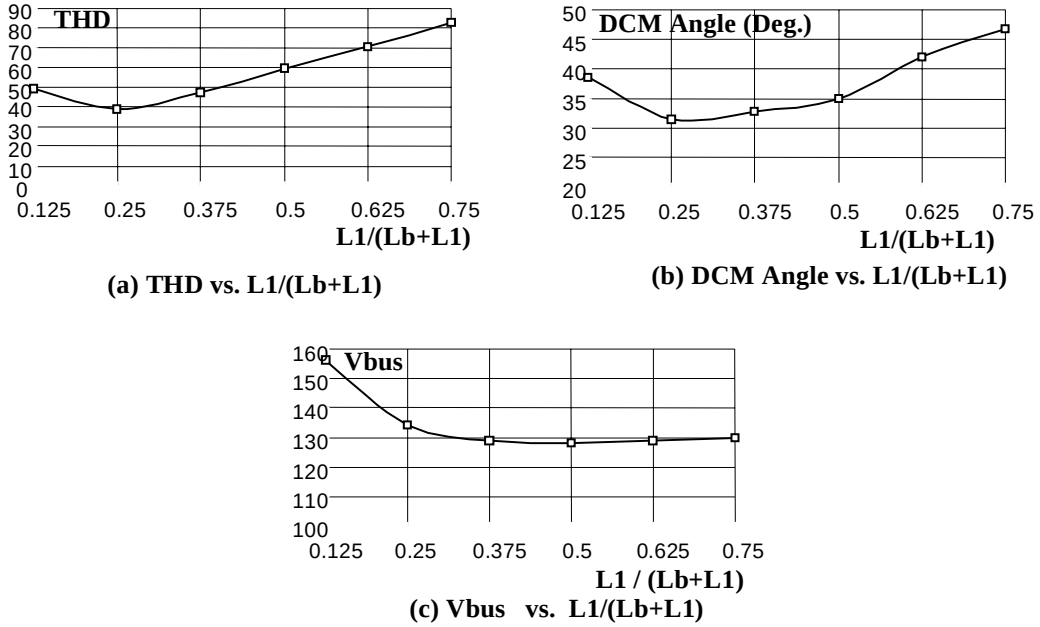


Fig. 3.14 Different inductance distribution @ 100 V line, heavy load ($L1+L_B$ = 1 mH)

Although the optimal inductance ratio is given in Fig 4.13, there is still a question of whether the ratio is strongly dependent on the total inductance value or not. To answer this

question, another case is studied in Fig. 3.15. At this time, the total inductance is changed from 1 mH to 700 uH. Figure 3.15 shows the 5% THD variation design range is 0.377 - 0.52 at this time. Compared to the previous range (0.33 – 0.5), the difference is small. Moreover, the optimal design point of inductance ratio $L1/(L1+L_B)$ is 0.51 in this case. It is also close to the previous 0.5 point. Besides, all the curves keep a similar shape. It means that the change of total inductance value (30%) does not change the optimal inductance ratio design point significantly.

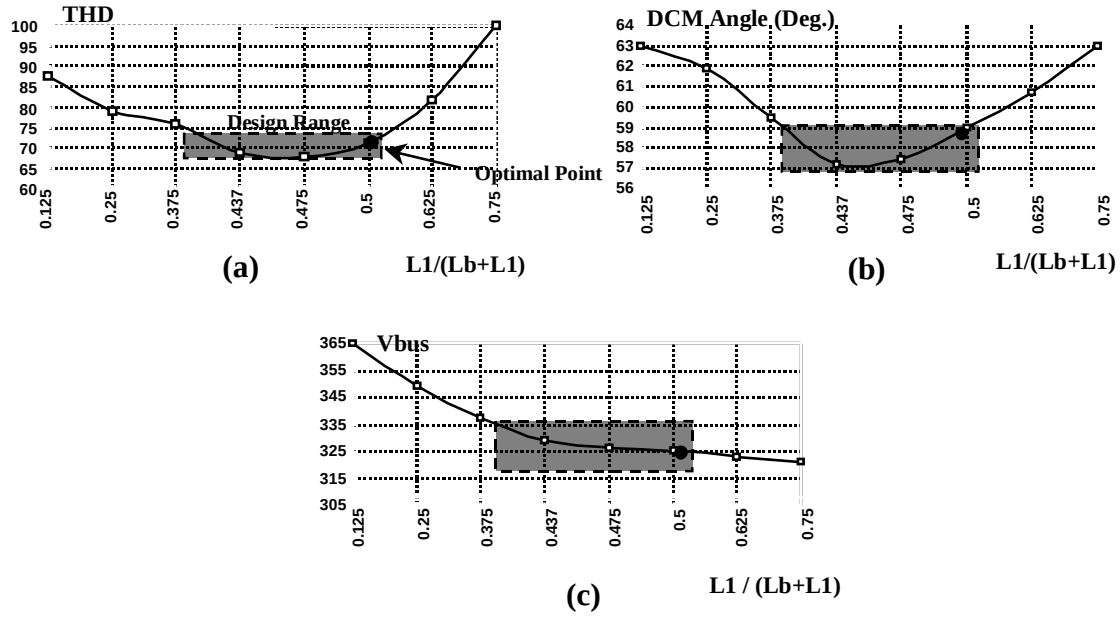


Fig. 3.15 Different inductance distribution @ 230 V line, heavy load ($L1+L_B$ = 700 uH)

There is another question. As illustrated before, to depress the bus capacitor voltage stress and improve the overall efficiency, a tapping winding N1 in Fig. 3.4 is often used. Then the question becomes, does the converter with tapping winding N1 have another different inductance distribution design range and optimal design point? To answer this question, another group of simulations is done and the results are shown in Fig. 3.16 Firstly, Fig. 3.16(a) shows that the overall input current THD is much larger than no tapping winding case in Fig. 3.16. It is

a reasonable conclusion that the feedback winding N1 introduces the dead input current conduction angle and therefore hurts the input current. However, Fig. 3.16 shows that the tapping converter has a similar design range (0.23 – 0.5) and the optimal design point remains as close to 0.5. It means the optimal point change a little even when a 25% tapping winding is used. The same optimal design point can be used no matter whether there is a tapping winding or not.

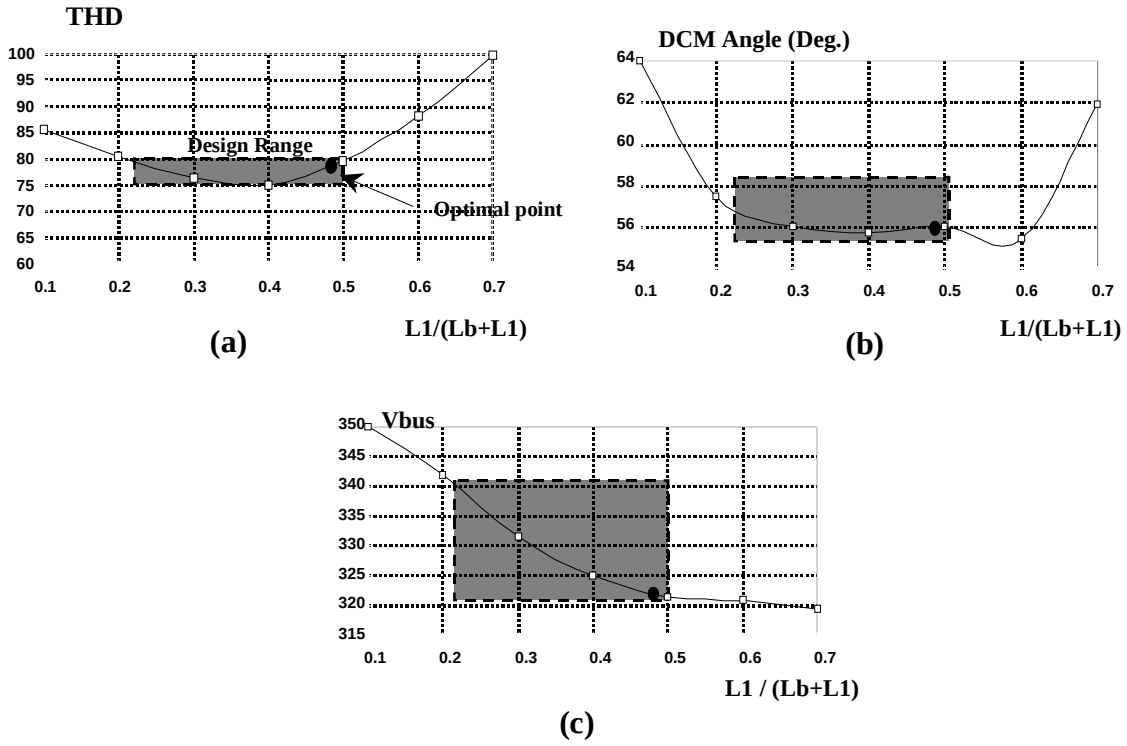


Fig. 3.16 Different inductance distribution @ 230 V line, heavy load ($L1+L_B$ = 1 mH, 25% tapping winding N1)

As a summary, the low THD design range only changes a little if the total inductance changes or a tapping winding is added. Therefore, the optimal design will be more general and simple.

3.2.3 Design consideration and program of CCM CS S^2-PFC converter

Generally, the design objectives of a universal line CS S^2-PFC converter are: (1) Limiting the bus capacitor to be lower than a particular value to give enough voltage margin for a 450 Vdc bulk bus capacitor; (2) Choosing the proper circuit parameters such as L_B and L1 to get low input current harmonics to meet the IEC PFC regulation; (3) Choosing sufficiently large tapping winding N1 for better efficiency, low voltage stress and still having adequate input power factor for the converter.

Because of the complicated operation principle of the CS S^2-PFC converter, it is very hard to derive the close-form mathematical equations as the design guideline. Therefore, using a numerical program approach to design this converter is an effective approach. A numerical analysis and MathCAD program is done by Delta Power Electronics Lab, INC. The basic concept of the CS S^2-PFC converter design program is based on the following two equations.

(1) Assume L_B flux is balanced for every switching cycle and L1 works in only DCM, Eq. 3.3 is given as:

$$i_{L_B ave}^{dcm/ccm} = i_{L_B ave}^{dcm/ccm}(V_B, D, L_1, L_B, L_F, {}^{N1}\!/_{Np}, vin, fs) \qquad (3.3)$$

Here, the V_B is the bus voltage, D is the duty cyce, L_F is the output stage inductor and fs is the switching frequency. The detailed derivation of Eq. (3.3) and (3.4) is presented in [C1].

It is necessary to point out that the L_B flux balance assumption is equivalent to saying that <vy> = v_{in_rec} during each half line cycle.

(2) Based on the input/output power balance fact, Eq. (3.4) is given as:

$$\int_0^{2\pi} [i_{L_B ave}(wt) \cdot v_{in\_rec}(wt)] dwt = \frac{Po}{\eta} \qquad (3.4)$$

Here, the Po is the output power and η is the estimated efficiency of the converter. In the program, η is chosen as 0.71 for the CS single-stage PFC converter.

Also, the voltage stress is limited to be 400 Vdc at high line, light load.

Based on the previous equations and assumptions, a design program is given as Fig. 3.17 for optimal design of a CS S^2-PFC converter for given circuit specification.

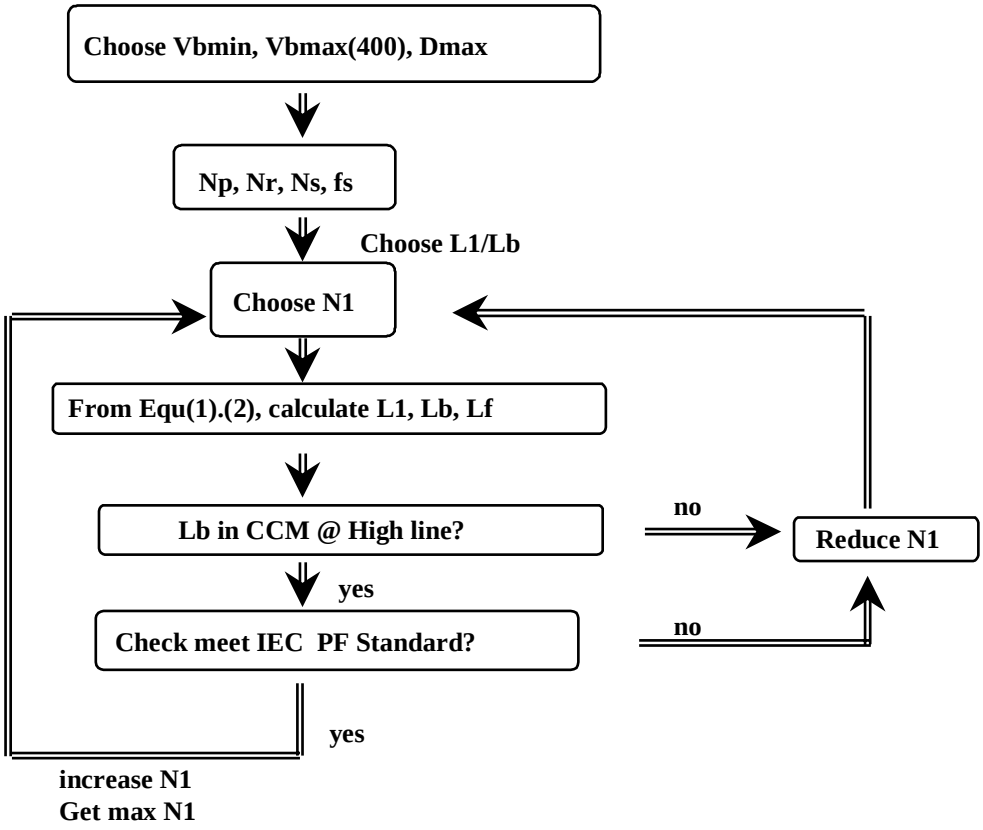


Fig. 3.17 Design program block diagram (by Delta INC.)

With this program, if the circuit specifications are input and the bus voltage stress setting point is chosen (for example, 400 V), then all the circuit parameters can be calculated numerically with the optimal inductance ratio. The design is quite different from the conventional two-stage PFC converter design. The final calculation results should be able to meet the IEC PFC regulation and the converter has the best efficiency.

3.2.4 Summary of CS S^2-PFC converter study

In this section, the detailed study on the CS S^2-PFC converter is done. It shows that a properly designed additional inductor L1 will help the CS S^2-PFC converter get a large CCM angle and give <vy> strong dependence on v_{in_rec}; therefore the best input power factor and lowest acceptable bus voltage is achieved. The design range and optimal point of inductance ratio $L1/(L1+L_B)$ is given in the example study. Also, the design procedure is presented.

3.3 Improved current source S^2-PFC converter with auxiliary switch

3.3.1 Limitation of CS S^2-PFC converter

The CS S^2-PFC converter achieves the CCM input current shaping with just one additional high frequency inductor so it is a very attractive circuit. As discussed above, the DCM/CCM angle will affect the input current waveform and input power factor significantly. For a universal-line CS S^2-PFC converter, at low line while the input current is high, the CCM angle is relatively large and therefore the input current has a nice waveform and can easily meet the IEC PFC requirement. However, while the converter is operating in the high line voltage range, the input current is low and therefore the CCM angle is reduced, which results in a more distorted input current and lower input power factor than in the low line case. There is a potential problem that this converter cannot meet the IEC PFC requirement at high line.

As presented before, the CS S^2-PFC converter has a bus voltage around 425 V. If a 450 V capacitor is used as the bulk capacitor, the voltage margin is about 5% and is not large enough. Of course a higher voltage rating capacitor can be used, but it means increasing the converter cost. For the low power cost-effective power supplies, it is very undesirable. To limit the voltage

stress and get a better efficiency, a tapped transformer can be used based on the bus-voltage-feedback concept [B10, B15]. However, as shown in Fig. 4.18, the bus-voltage-feedback tapping winding N1 will introduce dead input current conduction angle, therefore hurting the input power factor. Here, the tapping ratio is defined as the turns number of N1 over the transformer primary side turns number Np, i.e., N1/Np. Experiments show that if the tapping ratio N1/Np = 30 %, the DC bus voltage can be limited to 390 V. Figure 3.19 shows the comparison of different harmonic currents. The first column is the IEC PFC standard maximum current harmonics, the second column is the current harmonics of CS S^2-PFC converter without tapping winding and the third column is the current harmonics of S^2-PFC converter with 30% tapping winding. It shows that the 30% tapping-converter cannot meet the IEC PFC requirement. Even for the CS S^2-PFC converter without tapping winding, the current harmonics are already fairly close to the IEC standard and it makes the design very critical.

In summary, the input current waveform of the universal line CS S^2-PFC converter is not good enough at high line operation. Also, it has a small voltage margin for 450 V capacitor so a tapping winding is desirable to depress the voltage stress and increase the efficiency. However, the tapping-converter will have dead current conduction angle and therefore cannot meet the IEC PFC requirement. It makes the optimal design difficult.

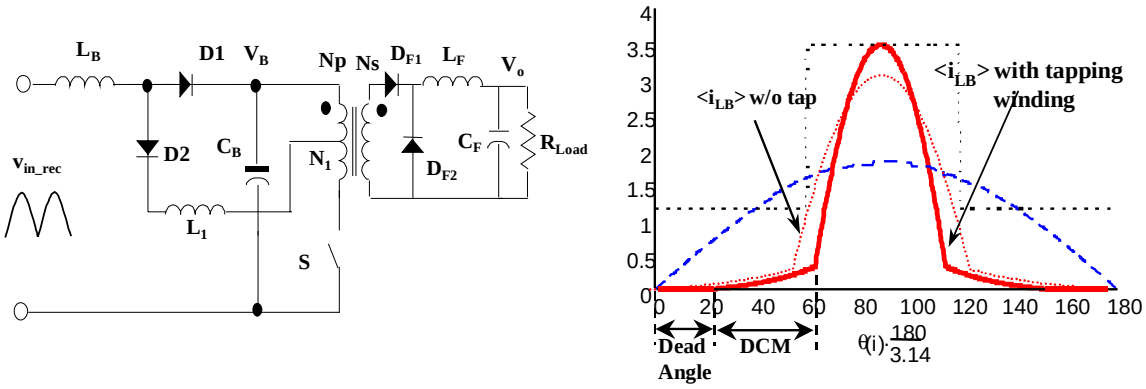


Fig. 3.18. CCM S²-PFC converter with taping winding: N1 introduces dead conduction angle and hurts PFC

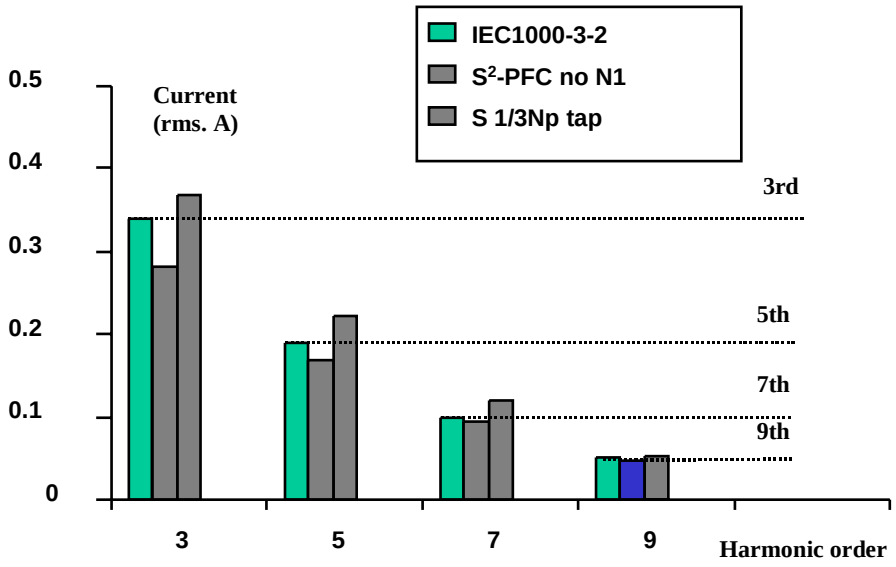


Fig. 3.19 Comparison of harmonic current of two converters @ Vin=230V, Pin = 100W, Vo = 5V

3.3.2 Improved CCM CS S^2-PFC converter with low-frequency auxiliary switch

3.3.2.1 Principle of proposed circuit

The previous input current waveforms in Fig. 3.18 show that the DCM/CCM current-difference and the current conduction dead angle cause the distortion of input current waveform. It is straightforward that during a half line cycle, if the zero-crossing part of the DCM current can be increased, the dead angle can be eliminated and the high peak part of the CCM current can be decreased, the input current will have much lower THD and better input power factor. Based on this thinking, an improved S^2PFC is proposed as shown in Fig. 3.20.

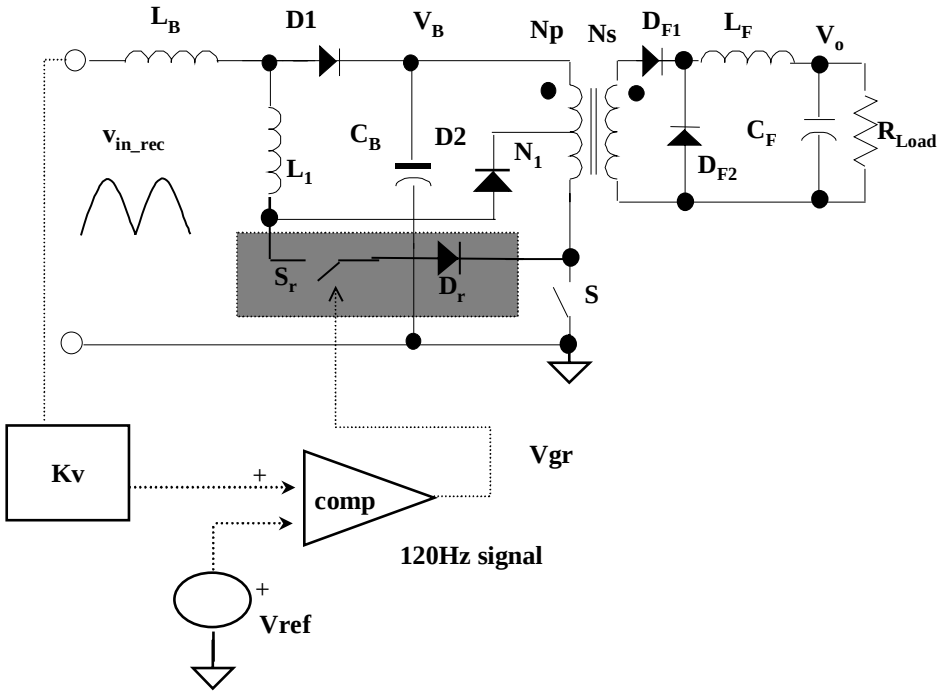
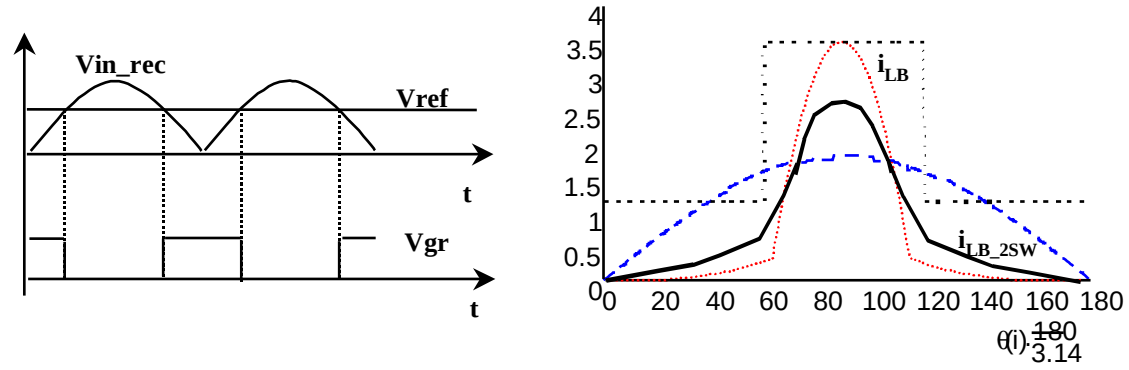


Fig. 3.20 Improved CCM S^2-PFC converter with low-frequency auxiliary switch Sr



(a) Control signal Vgr of auxiliary switch Sr **(b) Input current waveform with and w/o Sr.**

Fig. 3.21 Control timing of Sr and the improved input inductor current

In this circuit, the switch S is the main power switch and Sr is the low-frequency auxiliary switch, which helps achieve a better input current waveform. Figure 3.21(a) shows the control timing of the auxiliary switch Sr. During every half line cycle, when the instantaneous line voltage is close to the zero-crossing point, Sr is turned on to disable the tapping winding N_1, and therefore the dead angle is eliminated and the DCM part current is increased. When the instantaneous line voltage is higher than the reference voltage Vref, Sr is turned off to activate the tapping winding N_1, and therefore the bus voltage is feedback through N_1, resulting in low bus voltage stress, direct-energy-transfer and high efficiency. In this way, the disadvantage of N_1 is eliminated and the advantage of N_1 is retained. Furthermore, because the DCM current is also increased, the input current is even better than in the $N_1 = 0$ case. So the design of the previous CCM CS S^2-PFC also turns out to be easier.

One question that comes with the additional switch Sr is that whether this switch will increase the converter cost and decrease the efficiency significantly. It is necessary to point out that the additional auxiliary switch Sr is just a small current rating switch because it only conducts the small zero-crossing interval current. Therefore the conduction loss is very small. In addition, the switching frequency is just 120 Hz so the switching loss can also be ignored.

Therefore, the total loss introduced by Sr is almost negligible. It means the efficiency will not drop significantly and the switch Sr does not even need an additional heat sink. It is such a small switch that the additional cost and size is also small. From Fig. 3.20 and 3.21, it is clear that the control of Sr is simple as well. The control circuit just senses the rectified input voltage and compares it with a reference dc voltage to generate the trigger signal of Sr. The reference voltage can be a feedback voltage of the dc bus capacitor voltage Vb. Furthermore, Sr does not need an isolated gate driver because it only needs to be turned on when S is on. So the additional control circuit cost is also small. Dr is a small low current-rating high-voltage diode used to block the reverse voltage on Sr and protect the low-voltage control circuit. In summary, the additional cost and size due to Sr and its control circuit is small.

Figure 3.21 (b) shows how the auxiliary switch Sr can improve the input current waveform. The DCM current is increased and input current peak value is reduced to achieve a higher input power factor.

3.3.2.2 Experimental verifications of the proposed circuit.

Based on the previous concept, an experimental circuit is tested with the following specification and parameter values:

Input: 90 Vac – 265 Vac.

Output: 5 V, 3.3 V and 12 V multiple outputs; the total output power is 65 W.

Switching frequency: 100 kHz.

Circuit parameters: L_B = 530 μH, L_1 = 250 μH, Np = 32 turns, N_1 = 8 turns (N_1/Np=25%), Ns = 3 turns, C_B – 330 μF/450 V, S – IXTK21N100, Sr – IXYS XTP 4N50.

Figure 3.22 (a) and (b) show the experimental input inductor current waveform with and without Sr at 230 Vac input line voltage, respectively. The tapping ratio is 25% in the test circuit. It shows that the input inductor current has a dead conduction angle. The THD of the input current is 91%. Figure 3.22(b) shows the input inductor current waveform with auxiliary switch Sr at the same line condition. It is clear that the dead angle is eliminated. Besides, the current near the zero-crossing part is increased and the current peak is decreased, resulting in as low a THD as 73%. There is an 18% THD reduction.

Figure 3.23 shows the input current harmonic comparison at 110 V low line voltage. There are three different cases: (1) CS S^2PFC w/o N_1, (2) CS S^2PFC with 25% N_1, (3) improved CS S^2PFC with 25% N_1. All of them can easily meet the requirement. However, when a 230 V high line voltage is applied as in Fig.3.24, we can see that case (1) can tightly meet the IEC standard but the margin is small. Case (2) cannot meet the IEC standard. Case (3) can easily meet the standard and the margin is quite large. In case (3), with the help of the tapping winding, the bus voltage is lower than case (1). As a result, the duty-cycle in case (3) is larger than it in case (1). Therefore the DCM current in case (3) is higher than case (1), resulting in a better input current waveform. It has to be pointed out that even though case (1) can meet the standard, Fig. 3.24 shows the bus voltage stress of this one to be about 420 V at high line so the capacitor voltage margin is quite small. The improved circuit has a 400 V voltage stress and enough voltage margin. So the improved circuit will be more reliable from this point of view.

Figure 3.25 shows the THD and power factor comparison of three different circuits. It shows that the improved circuit actually improved the input current a great deal at the high line

range. Comparing (2) and (3), the maximum improvement of THD is more than 20%. This is a very big improvement.

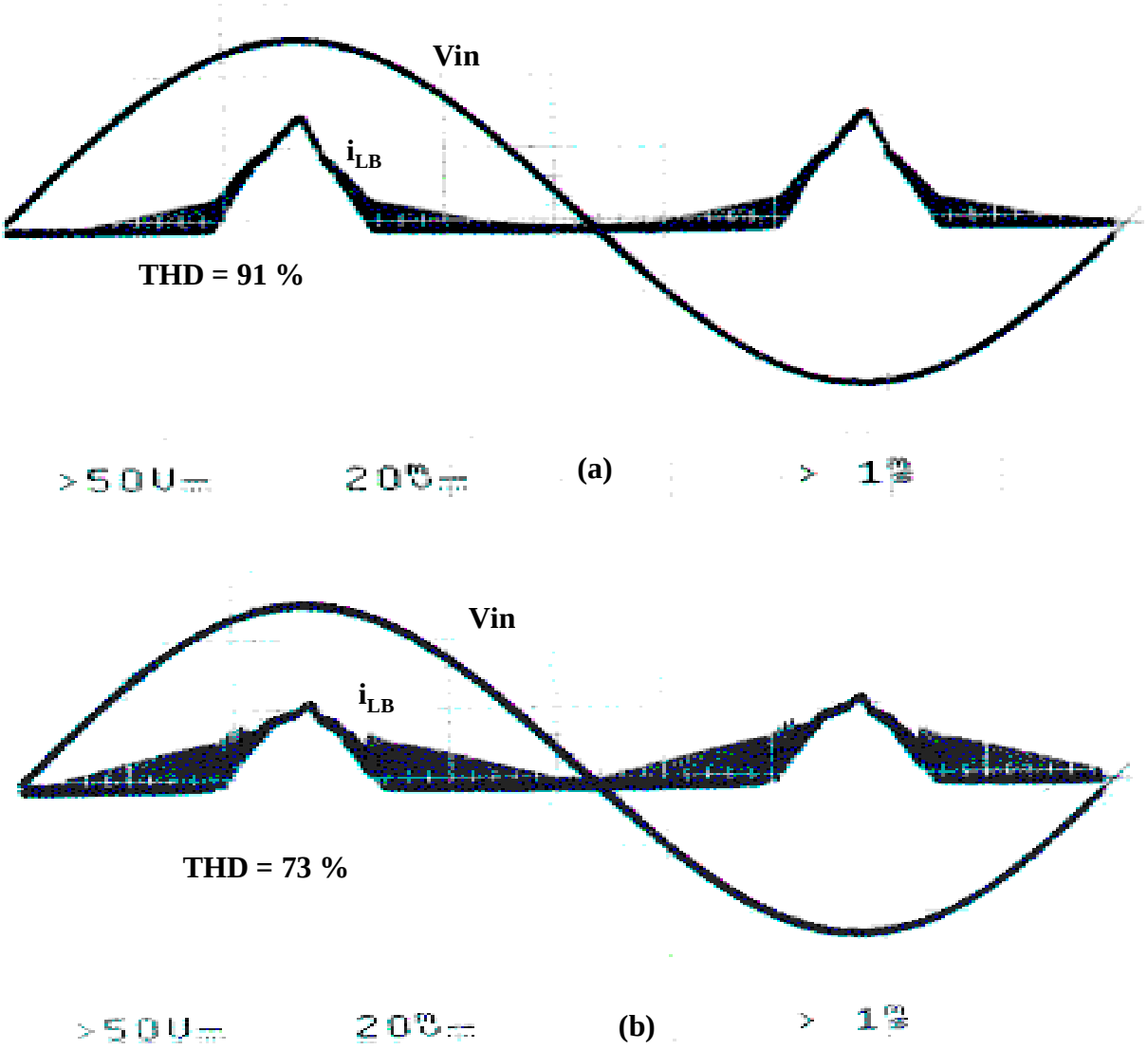
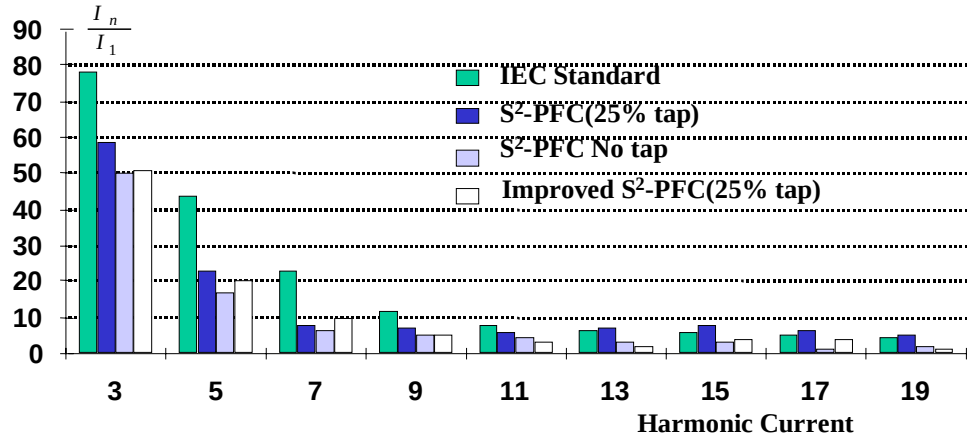
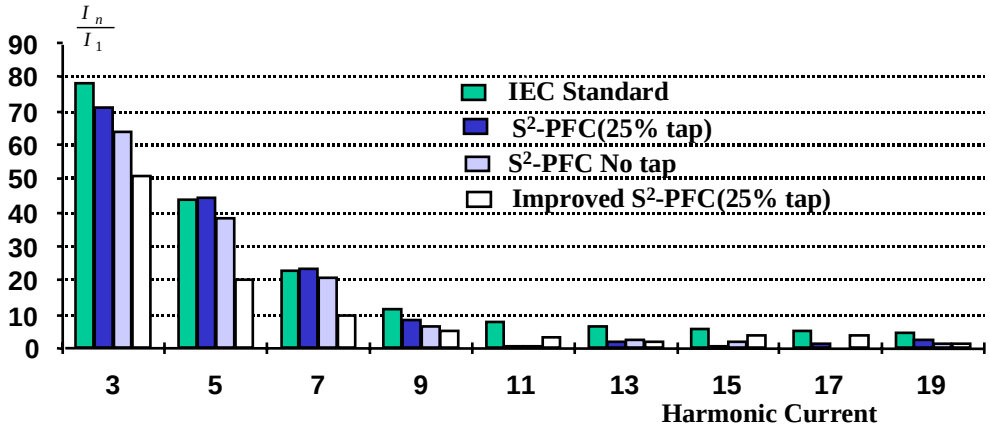


Fig. 3.22 Input inductor current waveforms
(230 Vac line, 5 V/ 13 A output)
(a) CCM S^4-PFC converter w/o Sr (25% tapping)
(b) Improved CCM S^4-PFC converter (25% tapping)



(a) Low line 100 Vrms, Po=65 W



(b) Low line 230 Vrms, Po=65 W

Fig. 3.23 Harmonic current comparison

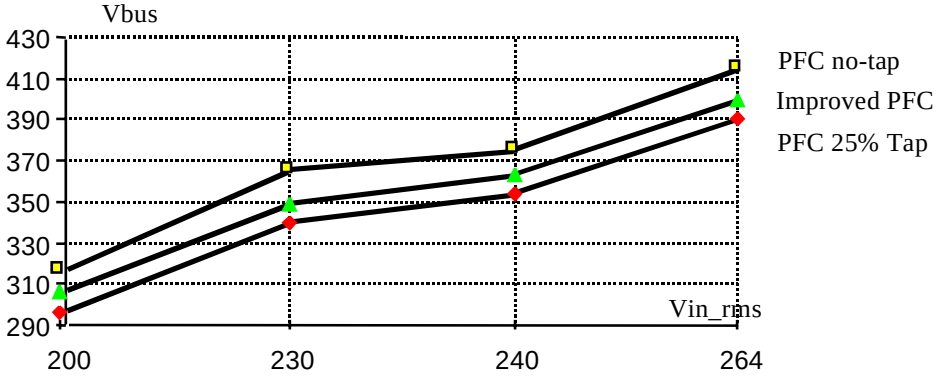


Fig. 3.24 Bus capacitor voltage stress comparison.

V_B @ 265 V line input: (450 Vdc capacitor)

PFC no-tap: 427 V

Improved PFC: 400 V

PFC 25% tap: 390 V

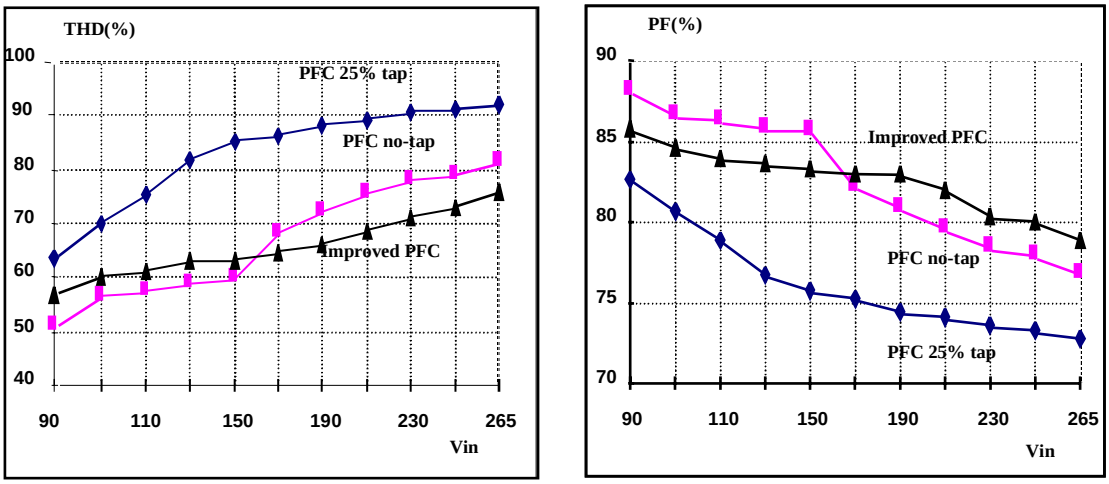


Fig. 3.25 The THD and power factor comparison for three different circuits

Figure 3.26 shows the efficiency comparison for three different circuits. It shows that 25% N_1/Np can increase efficiency about 1.5% at low line and about 0.5% at high line. The reason it works better at low line is because the current stress is higher at low line than at high line operation. This figure also shows that with a 25% tapping ratio, there is just a tiny efficiency difference whether Sr is added or not. It means the additional loss due to Sr is negligible.

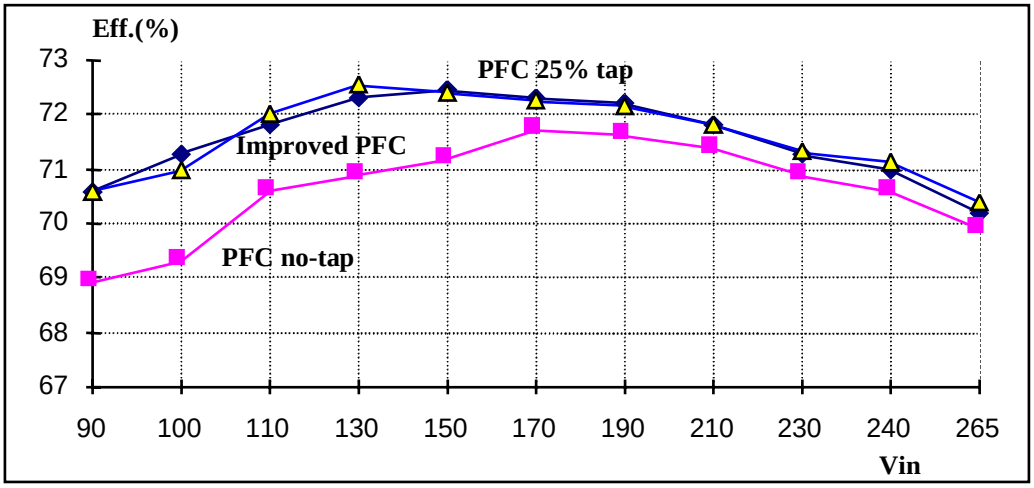


Fig. 3.26 Efficiency comparison of three different circuits

In order to further increase the efficiency and decrease the bus voltage stress, a higher N_1 is desirable. In the original CCM CS S^2PFC circuit, the N_1 value is limited by the harmonic current constraint. However, with the help of Sr, the improved circuit can have an even higher tapping ratio with better performance. Figure 3.27 shows the comparison of harmonic currents with 25% and 36.7% tapping ratio. It shows the higher tapping converter has lower harmonic currents and a larger margin to meet the IEC PFC regulation. Figure 3.28 shows the higher tapping ratio converter gives a better efficiency over full line voltage range. Also, the bus voltage stress with 36.7% tapping improved circuit is just 390 V. Of course, the tapping ratio cannot be too high; if it is, the current through Sr will be higher than the small switch can handle.

In conclusion, with the small rating auxiliary switch Sr, the improved S^4PFC converter effectively reduces the input current distortion and improves the efficiency.

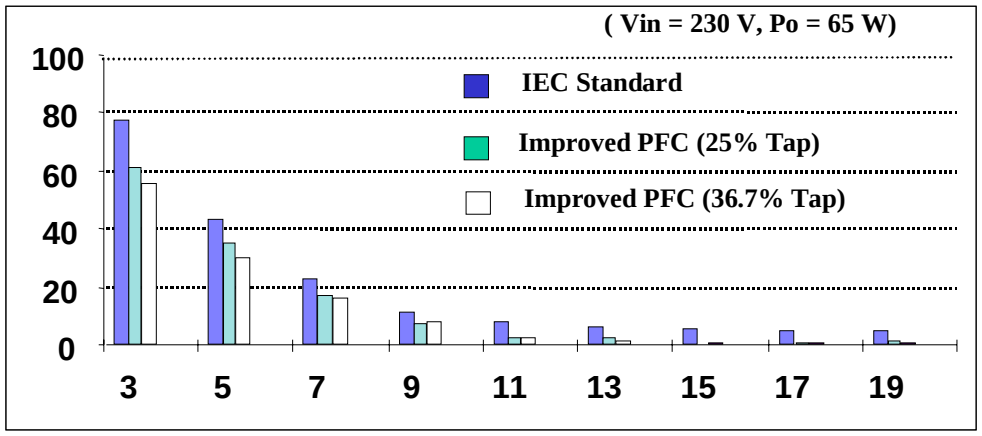


Fig. 3.27 Harmonic current comparison (different taping ratio)

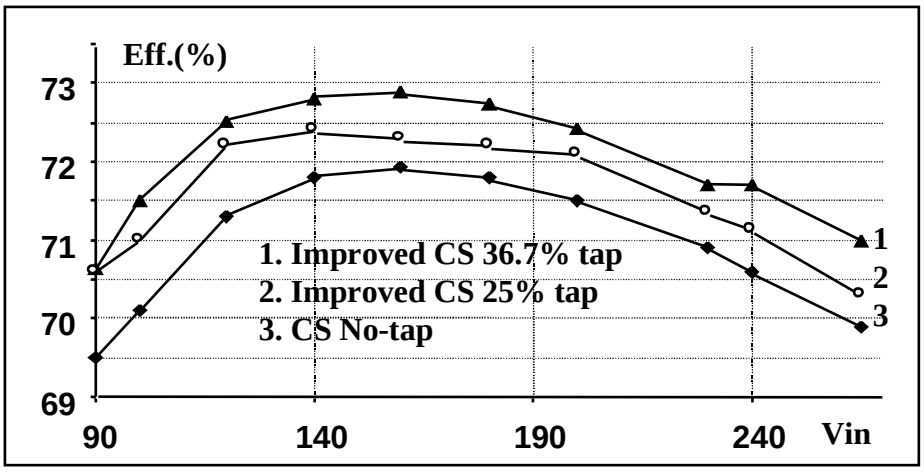


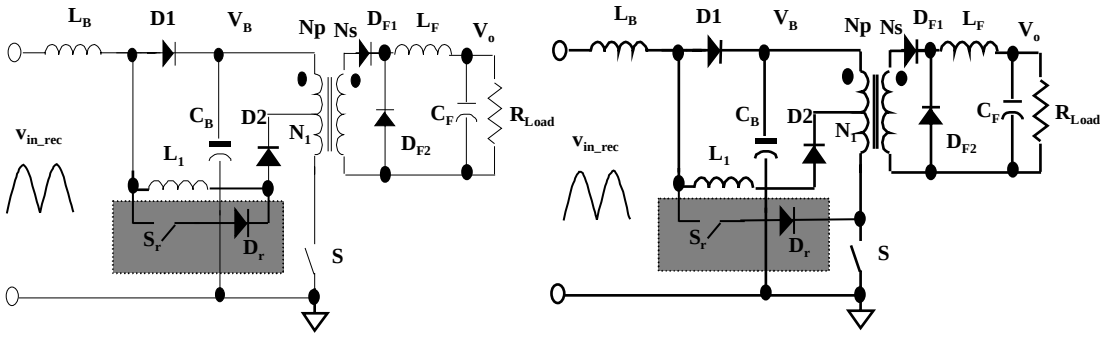
Fig. 3.28 Efficiencies for different taping ratio.
(Improved PFC converters)

3.3.2.3 Implementation variation

There are some other ways to implement the same concept on the CS single-stage PFC converter. Figure 3.29 (a) shows another application, which uses the same control approach to disable the additional inductor L_1 to increase the zero-crossing DCM current. However, this approach doesnot eliminate the dead conduction angle and may have a higher THD than the proposed approach. Also an isolated gate driver is required which is not desirable because it increases the cost. Figure 3.29 (b) shows a similar approach to disable both L_1 and N_1. This circuit will have a better input power factor but a higher bus voltage than the circuit in Fig. 3.20.

Another low cost alternative approach to improve the input current at high line is to replace the semiconductor switch Sr in Fig. 3.20 with a mechanical or electrical range selection switch. This switch is always turned on during low line and always turned off during high line to

eliminate the dead conduction angle at high line. The cost will be even lower but the high line bus voltage will be a little higher than the proposed improved circuit in Fig. 3.20.



(a) Disable L_1 to improve power factor

(b) Disable L_1 and N_1 to improve power factor

Fig. 3.29 Implementation variation of the auxiliary switch Sr on the CS single-stage PFC converter

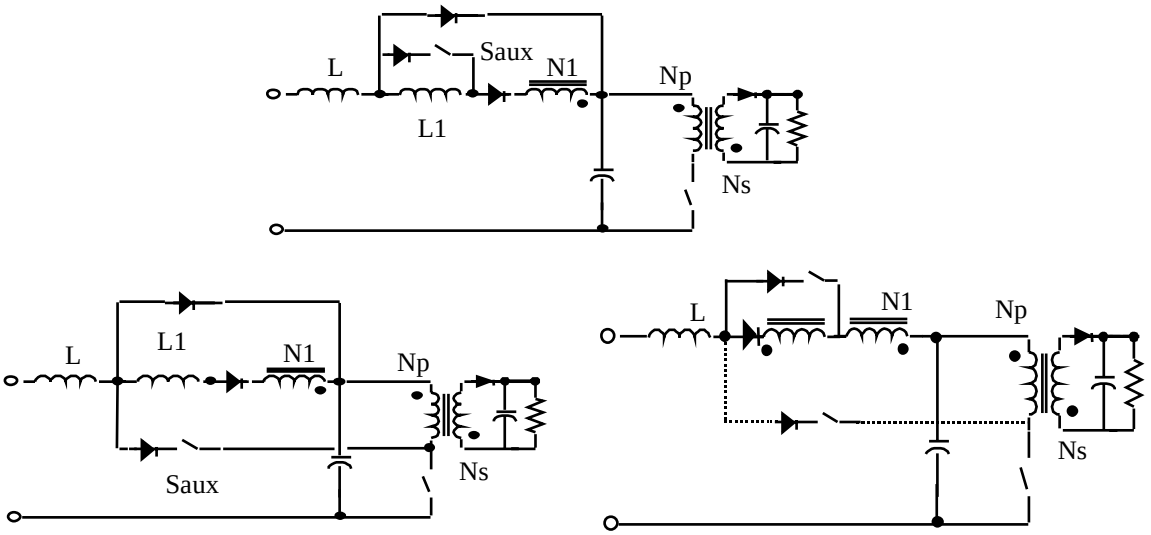


Fig. 3.30 Improved magnetic switch S^2-PFC converters with low-frequency auxiliary switch

As presented in Chapter 2, because the CCM CS magnetic switch (MS) S^2-PFC converters are the equivalent circuits of the CCM CS S^2-PFC converter, they also have the same problems as the CS S^2-PFC converter has. Therefore, the low-frequency auxiliary switch can also be added to those CCM CS MS converters to improve the input power factor. Figure 3.30 shows several different implementations.

Also, this improved PFC concept can be extended to other S^2PFC converter. Figure 3.31 shows an example of how to use this concept on a DCM S^2PFC converter to get better performance with low cost.

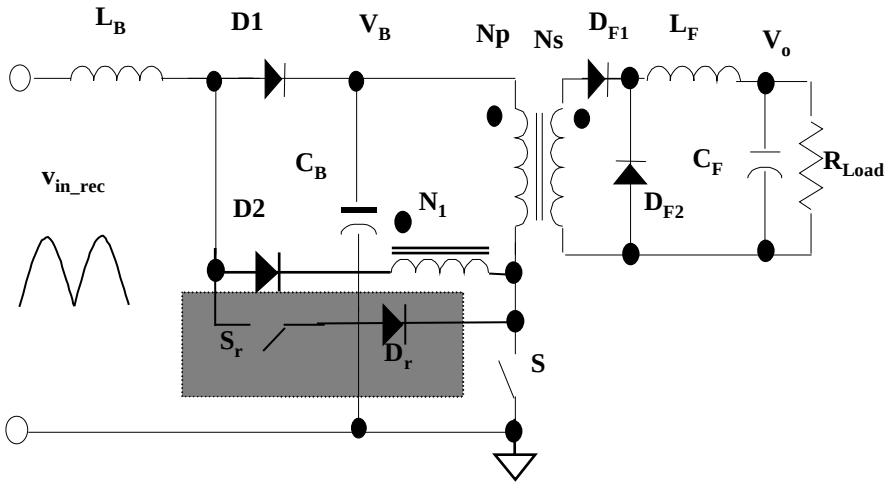


Fig. 3.31 Improved DCM S^4-PFC converter

3.4 Summary

In this chapter, a detailed study on the CCM CS S^2-PFC converter is presented. The circuit intuitions of the CCM CS S^2-PFC converter are given. It shows the inductance distribution between the input inductor and the additional inductor can give a design range and optimal point for lowest input current THD and bus voltage stress. The design consideration is

given. However, there are still some problem with the CS S^2-PFC converter regarding about the input current distortion and small capacitor voltage margin at high line. They make the optimal design of the CS S^2-PFC converter quite difficult. To make the design easy and also to get better performance, a low cost, small size and low loss auxiliary switch is introduced to the CS S^2-PFC converter. The experimental results show the improvement is effective. The implementation variations of this auxiliary-switch concept are also given.