# HIGH-FREQUENCY MULTI-RESONANT POWER CONVERSION TECHNIQUES

by

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APPROVED:

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Fred. C. Lee, Chairman
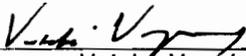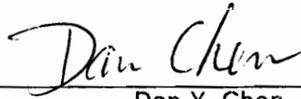
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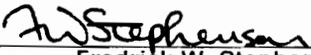
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(ABSTRACT)

The multi-resonant technique, a novel concept in dc/dc power conversion, is proposed. The essence of the multi-resonant power conversion is the effective utilization of the major parasitic reactive components of the power stage, including the leakage inductance of the power transformer, output capacitance of the power MOSFET, and junction capacitance of the rectifier. The multi-resonant operation is achieved by addition of a resonant switching network around the semiconductor switching devices.

Zero-voltage-switched multi-resonant converters (ZVS-MRCs) are proposed for high-frequency power conversion applications. ZVS-MRCs use a resonant network with one resonant inductor and two resonant capacitors. The resonant inductor is in series with the leakage inductance of the power transformer. One of the resonant capacitors is effectively in parallel with the power MOSFET, while the other resonant capacitor is effectively in parallel with the rectifier. As a result of the arrangement of the multi-resonant network, the major parasitic reactances of the power stage are utilized in the circuit. In addition, all semiconductor devices operate with zero-voltage switching, which substantially reduces the switching losses and permits efficient operation in multi-megahertz range, with moderate transistor voltage stress and wide load

range. A dc analysis is presented for the basic converter topologies: buck, boost, buck-boost, Cuk, Zeta, and SEPIC. The analysis is performed using a generalized multi-resonant switch concept.

The forward ZVS-MRC topology is employed to develop a state-of-the-art, high-density, on-board dc/dc power converter. The converter operates with a nominal input of 50 V and an output of 5 V at 10 A. The nominal switching frequency is 2.7 MHz. The complete hybridized converter has a power density of 50 W/in$^3$ and a nominal efficiency of 83%. The feasibility of increasing conversion efficiency at several megahertz by means of resonant synchronous rectification is investigated using circuit analysis with nonlinear-capacitance MOSFET and Schottky diode models.

To my wife

Elżbieta

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# 1. INTRODUCTION

Ever since the switch-mode power conversion technology was introduced, there has been a continuous effort to increase the conversion switching frequency. Higher switching frequency allows size reduction of the power transformer and the energy storage components (inductors and capacitors) used in the switching power converters, resulting in a higher power density of the equipment. In addition, the dynamic response of the power supply equipment can be made faster to improve the quality of the power supplied to the load. Most of today's switching dc/dc power converters use the pulse width modulation (PWM) technique. The PWM technique has been very widely used because of its design simplicity, high conversion efficiency, and simple control characteristics. Furthermore, various integrated PWM control circuits now are available to facilitate performance and cost optimization.

Until late 1970's, bipolar junction transistors (BJTs) were predominantly used as controlled switches in the switching power supplies. Due to the relatively low switching speeds of power BJTs, switchmode power supplies

(SMPS's) were operated at 20-50 kHz. With the introduction of the power MOSFET, switching frequencies of SMPS's were increased to the 100-200 kHz range.

Numerous attempts have been made to operate PWM converters at higher switching frequencies, up to a megahertz range [A1-A7]. The major problems encountered at elevated switching frequencies are switching losses and un-desirable oscillations caused by **parasitic reactances of the power stage**. The principal parasitic capacitances are associated with the semiconductor de-vices, although in some applications winding capacitance of the power trans-former can be a considerable problem. For high switching frequencies (>50 kHz), power MOSFETs are currently the primary choice for active switches. The passive switches are usually implemented using Schottky barrier rectifiers in low output voltage applications (up to 50 V) and $p$-$n$ junction diodes in high output voltage applications (above 50 V). The main parasitic inductance of the power converter circuit is usually the leakage inductance of the power trans-former. Other parasitic inductances, including package and lead inductances of semiconductor devices and stray inductances of the interconnections, can also play an important role in circuit's operation.

To illustrate the effects of the parasitic reactances on the converter's op-eration, a PWM buck converter circuit is considered. Figure 1.1(a) shows a simplified circuit diagram of a PWM buck converter. The circuit is assumed to operate in a continuous conduction mode, and the output filter and the load resistance are represented by a current source, $I_O$. The MOSFET output

capacitance, diode junction capacitance, and the leakage inductance are represented by $C_o$, $C_j$, and $L_{lk}$, respectively.

Switching waveforms of the converter are shown in Fig. 1.1(b). During conduction of the MOSFET, load current is flowing through the leakage inductance, and magnetic field energy is stored in $L_{lk}$. At turn-off, this energy induces a voltage spike across the MOSFET and the subsequent oscillations in the circuit formed by $L_{lk}$ and $C_o$. The uncontrolled voltage spike across the MOSFET may cause breakdown of the device, while the high frequency oscillations are a source of additional losses and noise.

A variety of turn-off snubber circuits have been proposed to suppress these oscillations and to reduce voltage stress on the MOSFET [B1-B10]. The RC and RDC snubbers are simple, but result in dissipation of the energy stored in the leakage inductance [B1-B4]. LC or regenerative snubbers [B5-B10] are designed to recover the leakage energy. The disadvantage of LC snubbers is their relative complexity. In addition, the snubber components introduce new parasitic reactances which can result in additional parasitic oscillations. Also, the switching frequency of PWM converters is limited by the finite times required for charging and discharging of the snubber components [B10].

When the power MOSFET in Fig. 1.1 is off, $V_{IN}$ is applied to the device, and energy is stored in its output capacitance. When MOSFET is turned on, this energy is dissipated in the device. If the leakage inductance is very small, the rectifier's capacitance, $C_j$, is also charged rapidly causing additional energy dissipation [J1]. If the leakage inductance is sufficiently large, parasitic oscil-
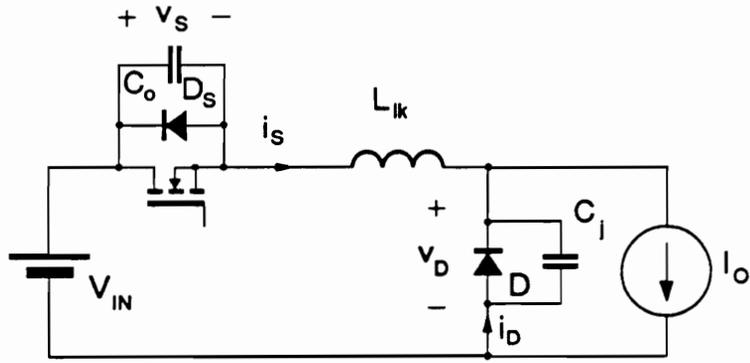
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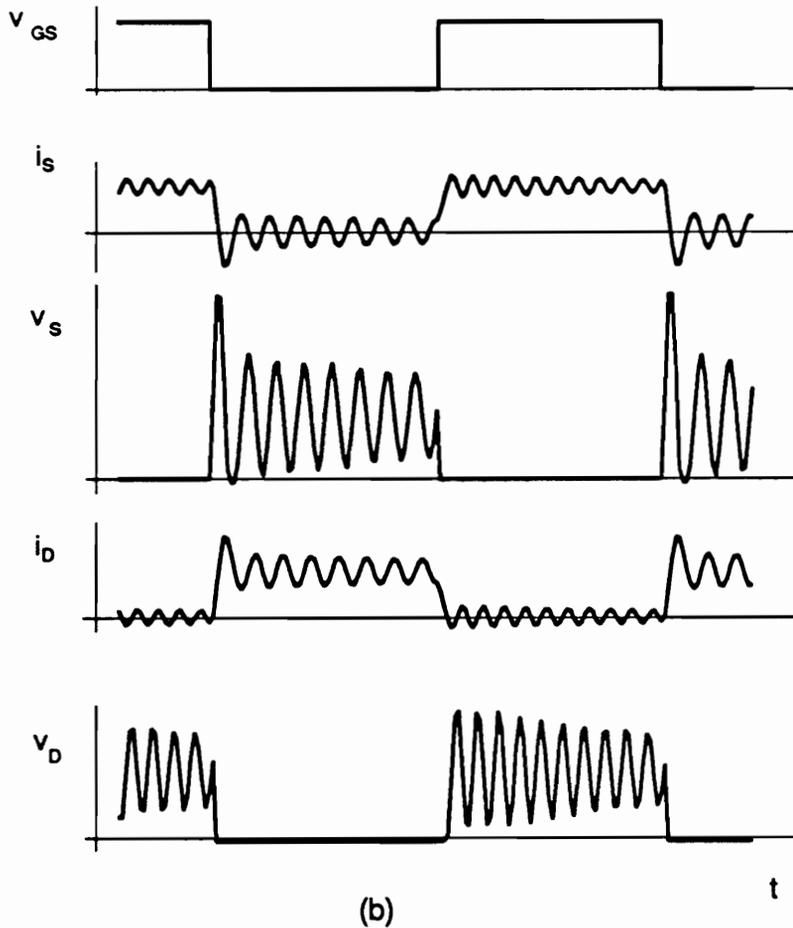


(b)

**Figure 1.1.** **Effect of parasitic reactances of the power stage on the operation of PWM buck converter: (a) Circuit diagram showing parasitic reactances. (b) Typical waveforms.**

lations will develop in the resonant circuit formed by $L_{lk}$ and $C_j$ [J1]. However, the energy required to charge $C_j$ will be dissipated after the oscillations decay. The energy loss associated with discharging of $C_o$ and charging $C_j$ is determined by the capacitance values and the magnitude of the switched voltage. The energy loss is not affected by the switching speed of the MOSFET or the value of $L_{lk}$ (provided oscillations decay completely during on-time).

Additional turn-on switching loss in the MOSFET is caused by the finite rise time of the drain current and the finite fall time of the drain voltage. This turn-on loss is directly related to the current-sourcing capability of the gate drive. The turn-on time and the loss associated with the overlap of the drain current and drain voltage can be reduced by increasing the current capability of the gate drive. Also, the presence of $L_{lk}$ can reduce or even eliminate the overlap of the drain current and voltage. In fact, a series inductance is used in turn-on snubbers to reduce the turn-on loss [B2, B7].

The input capacitance of the MOSFET is also a source of power dissipation at both turn-on and turn-off, when it is charged and discharged by the gate-drive circuit. If a typical square-wave gate drive is used, every time the power MOSFET is turned on or off, energy equal to the energy stored in the input capacitance is dissipated in the gate-drive circuit. The charge delivered to the gate-drive circuit is the sum of the charge stored in $C_{gs}$ and the "Miller" charge associated with $C_{gd}$. The amount of the Miller charge depends on the value of $C_{gd}$ and the drain voltage swing.

Since the energy stored in the parasitic reactances during each switching cycle is constant for a given set of devices and fixed operating conditions

(voltage, current, and power levels), the resulting power dissipation increases in proportion to the switching frequency. As a result, PWM converters cannot operate efficiently at elevated frequencies.

Several power conversion techniques have been proposed to alleviate the detrimental effects of the parasitic reactances and to improve the switching conditions of the semiconductor devices. These techniques include: resonant converters [C1-C23], quasi-resonant converters [D1-D55], Class E converters [E1-E26], forward resonant converter [F1-F3], and resonant transition converters [G1-G17]. Each of these techniques reduces switching losses in the power MOSFET by operating the device with either zero-current turn-off or zero-voltage turn-on. In addition, operation of certain resonant converter topologies can be made insensitive to some major parasitic reactances [J8, J10].

In particular, the quasi-resonant technique offers a general approach for improvement of the switching waveforms. The quasi-resonant converters are directly derived from PWM topologies. There are two families of quasi-resonant converters: zero-current-switched quasi-resonant converters (ZCS-QRCs) [D1-D38] and zero-voltage-switched quasi-resonant converters (ZVS-QRCs) [D39-D55]. Both families are generated from PWM topologies using the resonant-switch concept [D4, D6, D22, D24, D34, D35, D38].

Figure 1.2 shows the basic configurations of zero-current and zero-voltage quasi-resonant switches, which represent the high-frequency sub-circuits extracted from QRCs by replacing voltage sources and filter capacitors with short circuits, and filter inductors with open circuits [G1]. In the zero-
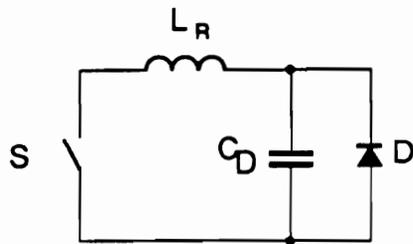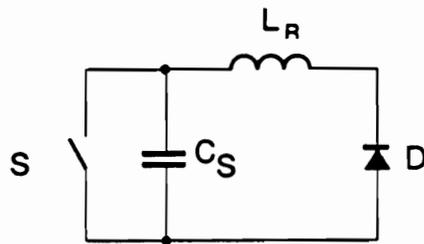
**Figure 1.2. Equivalent circuits of quasi-resonant switches: (a) Zero-current-switched. (b) Zero-voltage-switched.**

current quasi-resonant switch, active switch $S$ is in series with the resonant inductor, while the diode is in parallel with the resonant capacitor. In the zero-voltage quasi-resonant switch, the active switch is in parallel with the capacitor, and the diode is in series with the inductor. The arrangement of the resonant components with respect to the switching devices determines which parasitic reactances will be absorbed by the resonant circuit. As can be deduced from Fig. 1.2, ZCS-QRCs are insensitive to leakage inductance and the junction capacitance of the rectifier diode, while ZVS-QRCs are insensitive to leakage inductance and the output capacitance of the MOSFET.

Figure 1.3 shows a circuit diagram and PSpice-simulated waveforms of a buck ZCS-QRC. This topology is derived from a PWM buck converter by inserting an external resonant inductor, $L_{Rx}$, in series with the switch, and an external resonant capacitor, $C_{Dx}$, in parallel with the diode. The effective resonant inductance, $L_R$, is the sum of $L_{Rx}$ and $L_{lk}$. Similarly, the effective resonant capacitance $C_D$ is the sum of $C_{Dx}$ and $C_j$. Antiparallel diode $D_S$ represents the body diode of a MOSFET.

During conduction of the MOSFET, $L_R$ and $C_D$ form a resonant circuit, resulting in a sinusoidal drain current and a fall of the drain current to zero prior to turn-off. As a result, the turn-off switching loss associated with drain current/voltage overlapping is practically eliminated. Furthermore, the energy stored in $L_R$ at turn-off is zero, and the the losses and oscillations associated with inductive turn-off are eliminated.

The parasitic oscillations present in $v_S$, as shown in Fig. 1.3(b), are induced by application of the linearly rising voltage $V_{IN} - v_D$ to the series-
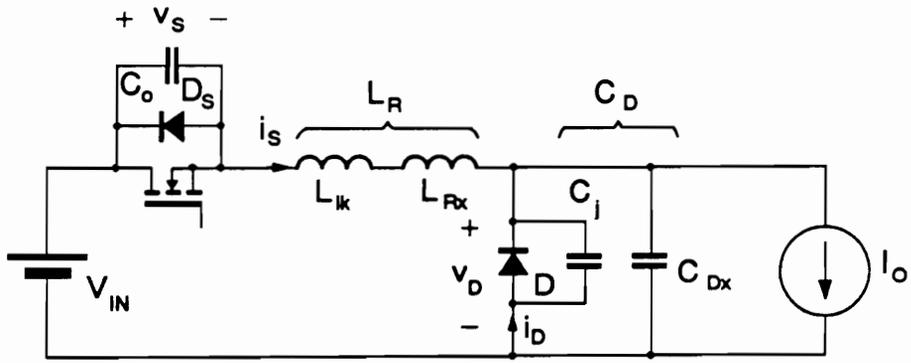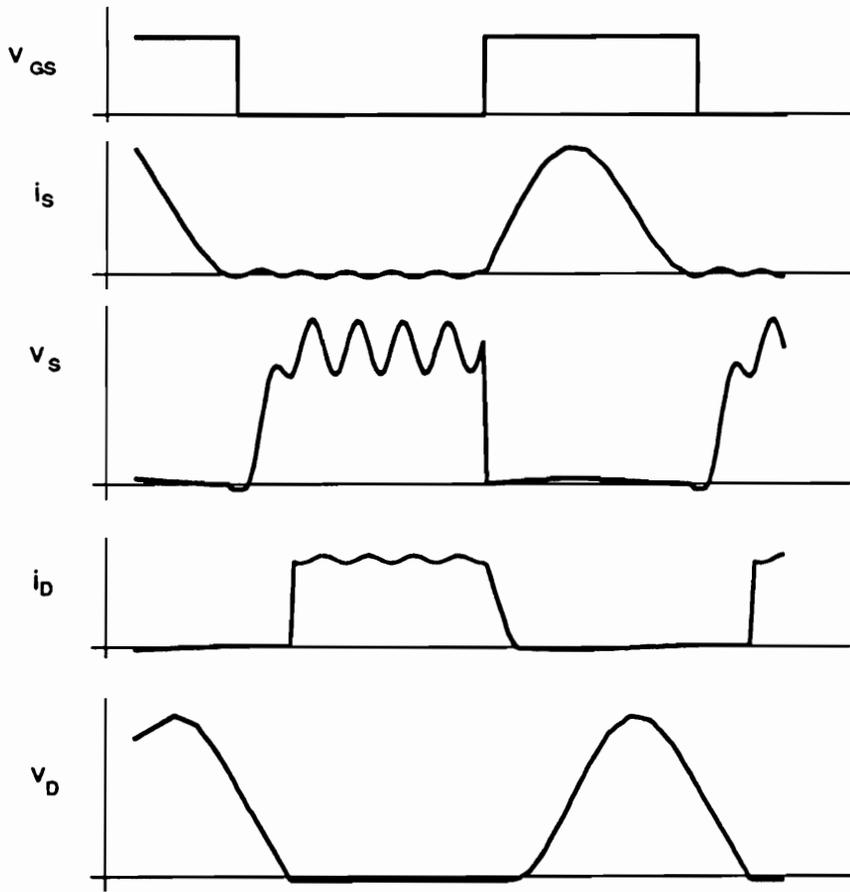
Figure 1.3.  Buck ZCS-QRC:  (a) Circuit diagram.  (b) Typical waveforms.

resonant circuit formed by $L_R$ and $C_o$ after the MOSFET is turned off. In full-wave ZCS-QRCs [D5] where the MOSFET body diode $D_S$ is used for reverse current conduction, this parasitic oscillation is further aggravated by the reverse recovery of $D_S$ [D37]. One way to reduce this problem is to use a diode in series with MOSFET to prevent $D_S$ from conducting. However, the reverse-recovery characteristics of the available fast-recovery diodes also result in considerable oscillations [D37]. Another method is to use a MOSFET with sufficiently low on-resistance and to precisely control the duration of the on-time to assure that the reverse current flows through the channel and not through the body diode of the MOSFET [D19].

Although ZCS-QRCs take advantage of zero-current turn-off of the power switch, turn-on of the device occurs when full input voltage is applied to it. This causes dissipation of the energy stored in $C_o$ and the switching Miller effect, in exactly the same way as in PWM converters.

The problem of capacitive (non-zero-voltage) turn-on is solved in ZVS-QRCs by reducing to zero the drain-to-source voltage prior to turn-on. Figure 1.4(a) shows a simplified circuit diagram of a buck ZVS-QRC. This topology is derived from its PWM counterpart by addition of an external resonant capacitor, $C_{Sx}$, in parallel with the MOSFET, and an external resonant inductor, $L_{Rx}$, in series with $L_{lk}$. The equivalent resonant inductance, $C_S$, is formed by $C_o$ and $C_{Sx}$, while the equivalent resonant inductance, $L_R$, consists of $L_{lk}$ and $L_{Rx}$.

In ZVS-QRCs, the power MOSFET operates under favorable switching conditions. At turn-off, drain current is diverted from the channel of the
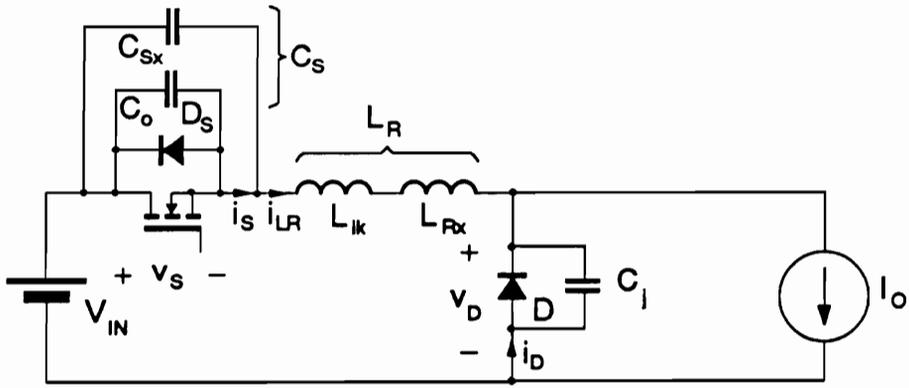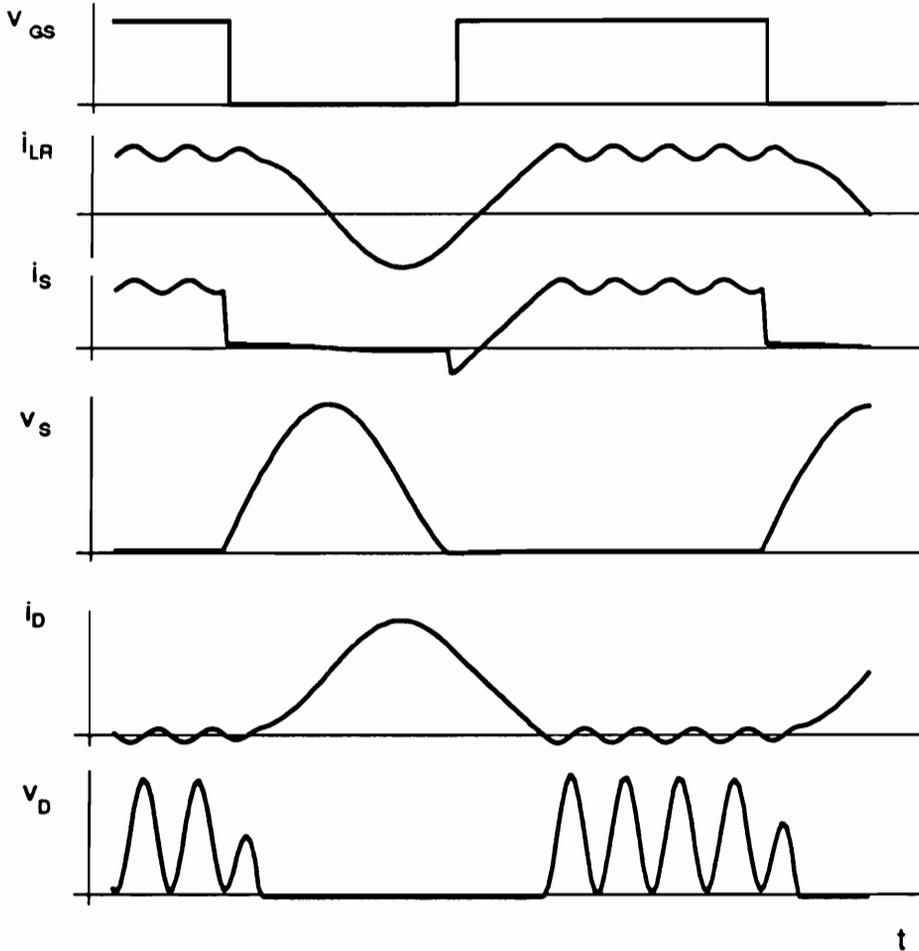
Figure 1.4. Buck ZVS-QRC: (a) Circuit diagram. (b) Typical waveforms.

MOSFET into $C_S$. Subsequently, $C_S$ is linearly charged to the input voltage by the load current. The gradual increase of $v_S$ minimizes the overlap of the switch current and voltage, thus reducing the switching losses considerably. During the off-time, the drain-to-source voltage is quasi-sinusoidal. At turn-on, $v_S$ is zero, and the capacitive turn-on loss and switching Miller effect are eliminated.

Improved switching conditions for the active switch allow operation of ZVS-QRCs at frequencies as high as 10 MHz [D49]. However, operation of ZVS-QRCs is adversely affected by the junction capacitance of the rectifier. Due to $C_j$, the diode voltage cannot change instantaneously from zero to $V_{IN}$ when the diode current is reduced to zero. Instead, a series-resonant circuit is formed by $L_R$ and $C_j$, and diode voltage is oscillatory with a peak value equal to $2V_{IN}$. Figure 1.5 shows a comparison of theoretical and experimental diode voltage waveforms in a typical ZVS-QRC.

If these oscillations decay before MOSFET is turned off, the energy associated with charging of $C_j$ will be lost, in the same way as in a PWM converter. If these oscillations do not decay before the MOSFET turn-off, the conversion-ratio characteristics will be adversely affected. This is illustrated in Fig. 1.6, which shows the conversion ratio of a buck ZVS-QRC, $M = V_O/V_{IN}$, vs. normalized frequency, $f_N = f/f_0$ (where $f_0 = 1/(2\pi\sqrt{L_R C_S})$), with normalized output current, $I_N = I_O\sqrt{L_R/C_S}/V_{IN}$, as a free running parameter. When junction capacitance of the rectifying diode, $C_j$, is assumed to be zero, the characteristics form straight lines as shown in Fig. 1.6(a). Figure 1.6(b) shows the characteristics for $C_j = 0.5C_S$. Even when $C_j$ is only half of the resonant
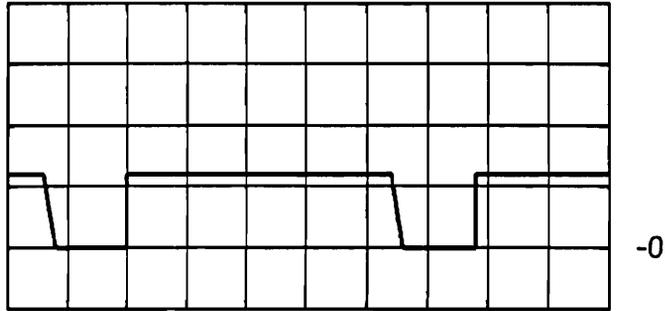
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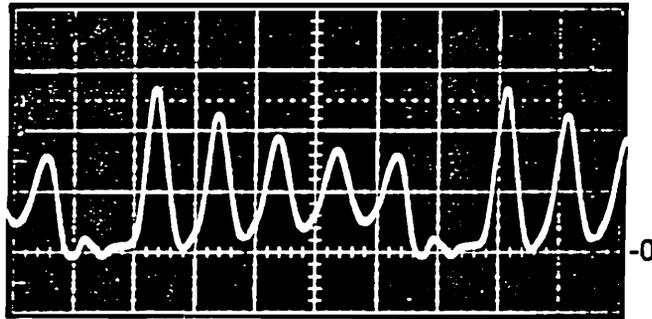


(b)

**Figure 1.5. Typical waveform of the rectifier diode voltage in ZVS-QRCs:  (a) Theoretical.  (b) Experimental.**

capacitance, the effects of $C_j$ are quite pronounced. (In high-frequency converters $C_j$ can easily be larger than $C_S$, especially if high-current diodes with large die areas are used.) The discontinuities of the characteristics imply that the zero-voltage-switching property is lost for some operating conditions. Furthermore, in regions where the slopes of the curves are positive, the converter exhibits local closed-loop instabilities. Even in those regions where the slopes are negative, the slope can be very steep making the conversion ratio very sensitive to the switching frequency and, thus, difficult to control [J1]. Another important drawback of ZVS-QRCs is an extensive voltage stress on the switching transistor. This stress is proportional to the load range [D49]. As a result, ZVS-QRCs are not suitable for applications with wide load variations.

**The present work** is dedicated to overcoming the aforementioned problems of PWM converters and QRCs by means of new circuit design techniques. The basic philosophy employed throughout this work is to create desirable switching conditions for **all** the semiconductor devices, using the natural oscillations occurring in the power circuit due to the the parasitic reactances. Following this philosophy, a novel, **multi-resonant technique** is developed and a family of multi-resonant converters is proposed. The concept of multi-resonant technique and basic multi-resonant converter topologies are introduced in Chapter 2. A generalized dc analysis of the basic topologies of ZVS-MRCs is presented in Chapter 3. Based on the analysis, design guidelines and procedures for various ZVS-MRCs are derived in Chapter 4. A computer-aided analysis of the forward ZVS-MRC is presented in Chapter 5. The application of the forward ZVS-MRC in a high-density on-board dc/dc
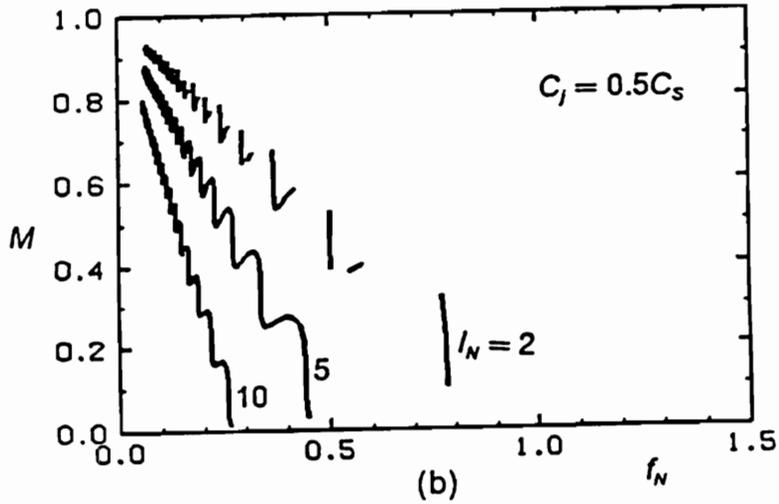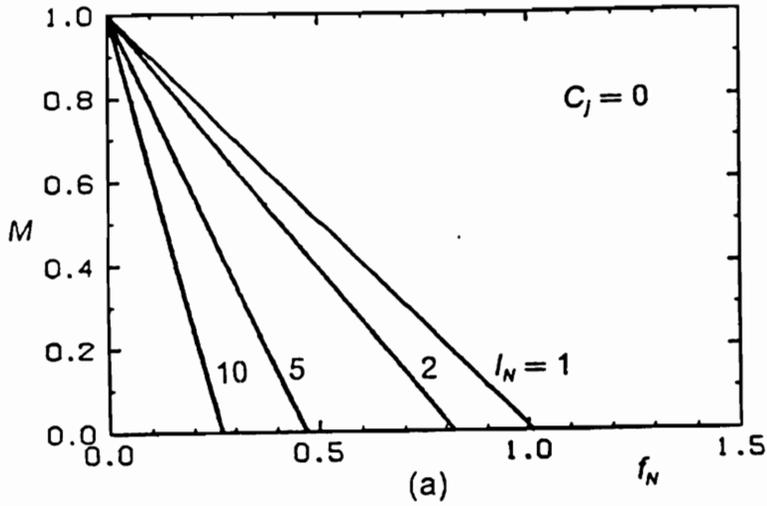
**Figure 1.6.** Effect of rectifier junction capacitance on the dc conversion-ratio characteristics of a buck ZVS-QRC: (a) Ideal characteristics at $C_j = 0$. (b) Characteristics at $C_j$ equal to one-half of the resonant capacitance across the switch.

power converter is discussed in Chapter 6. The issues related to high-frequency synchronous rectification using PWM and resonant techniques are discussed in Chapter 7. Conclusions are presented in Chapter 8. An extensive reference list is also provided.

# 2. MULTI-RESONANT CONVERTER CONCEPT

In QRCs a resonant switch with a two-element resonant network (quasi-resonant switch) is used to achieve zero-current or zero-voltage switching of the active semiconductor device. The quasi-resonant switch also effects the switching waveforms of the passive switch. In ZCS-QRCs, the passive switch operates with zero-voltage switching, while in ZVS-QRCs, it operates with zero-current switching. The concept of multi-resonance explores the possibility of using a resonant-switch with a three-element resonant network (multi-resonant switch) to achieve either zero-voltage switching of both the active and passive devices, or zero-current switching of both devices.

This chapter introduces the multi-resonant switches and proposes two families of MRCs: ZCS-MRCs and ZVS-MRCs. The ZVS-MRCs are shown to be more suitable for high-frequency power conversion applications, since the resonant elements are arranged to utilize the junction capacitances of the semiconductor devices.

## 2.1. Multi-Resonant Switches

Figure 2.1 shows the two simplest multi-resonant switches. In the zero-voltage multi-resonant switch, shown in Fig. 2.1(a), the resonant circuit is formed in a Π-network with resonant capacitors connected in parallel with the switches. In the zero-current multi-resonant switch, shown in Fig. 2.1(b), the resonant circuit is formed in a T-network with resonant inductors in series with the switching devices. During operation of an MRC, three different resonant circuits can be formed, depending on whether the active switch and diode are open or closed. This results in operation of the converter with three different resonant stages in one cycle of operation (hence the term "multi-resonant").

To introduce the basic operational principles of ZCS-MRCs and ZVS-MRCs, the buck converter is used as an example. Figure 2.2(a) shows a simplified circuit diagram of a buck ZVS-MRC. As with the quasi-resonant converters discussed in Chapter 1, continuous-mode operation is assumed, and $I_O$ models the LC output filter and the load. The resonant network consists of the resonant elements $L_R$, $C_S$, and $C_D$. Each of the resonant elements is formed by a combination of the externally added components ($L_{Rx}$, $C_{Sx}$, and $C_{Dx}$) and the parasitic elements ($L_{lk}$, $C_o$, and $C_j$). If the converter is operated at a sufficiently high switching frequency, the resonant elements can be formed exclusively by the parasitic components (i.e., $L_{Rx} = 0$, $C_{Sx} = 0$, and $C_{Dx} = 0$).
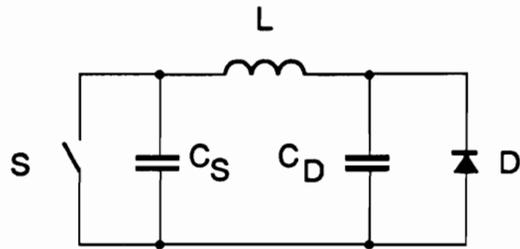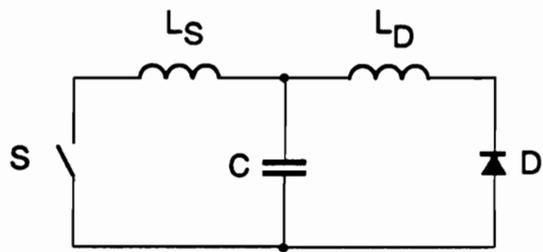
**Figure 2.1. Multi-resonant switches: (a) Zero-voltage switched. (b) Zero-current switched.**
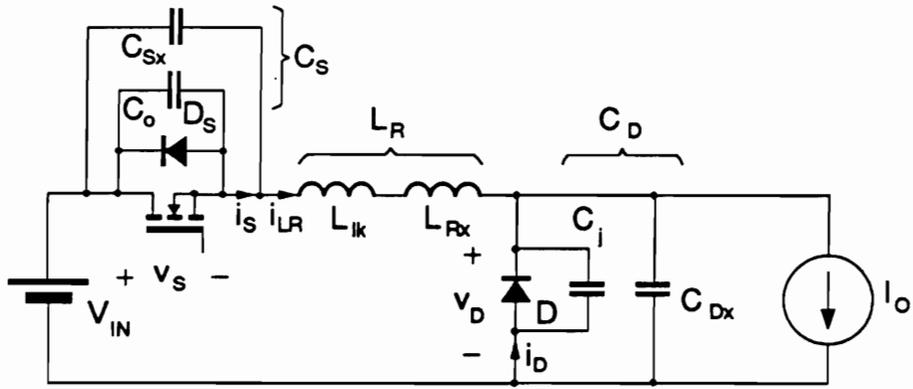
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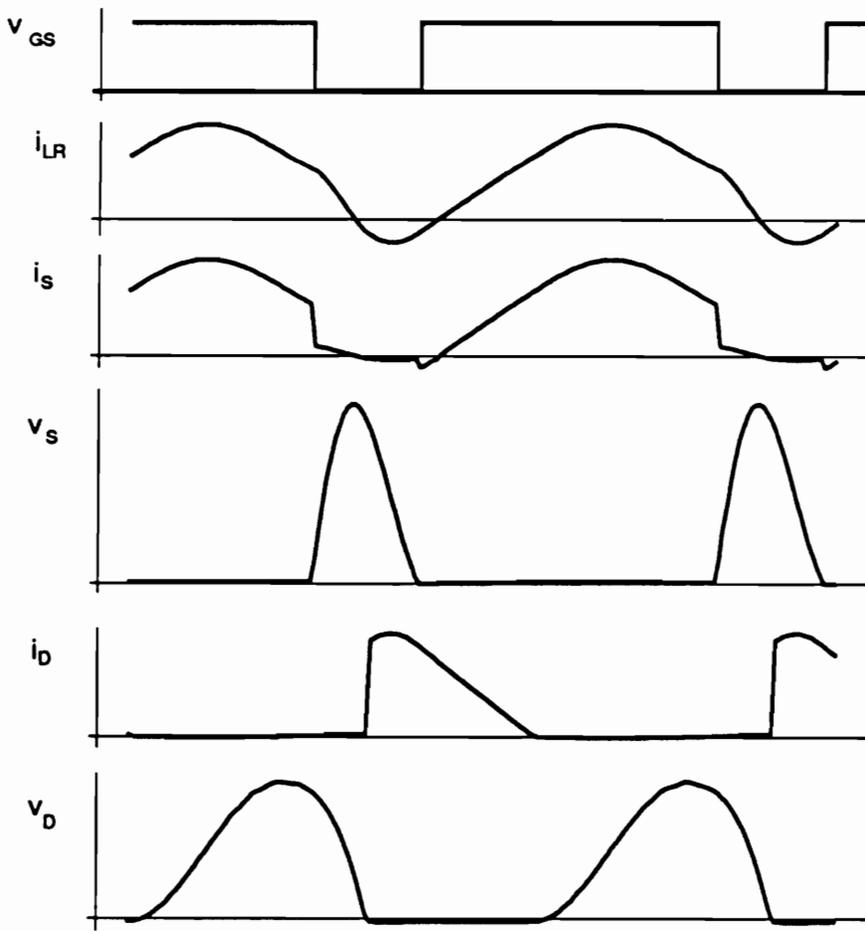


(b)

**Figure 2.2. Buck ZVS-MRC: (a) Simplified circuit diagram. (b) Typical operating waveforms.**

Typical ZVS-MRC switching waveforms are shown in Fig. 2.2(b). In ZVS-MRCs, the gate-drive signal has a constant off-time, and the on-time is adjusted to regulate the output. When the MOSFET is conducting, a resonant circuit is formed by $L_R$ and $C_D$. As a result, current $i_S$ flowing through the MOSFET and voltage $v_D$ applied to the rectifying diode are sinusoidal. When the MOSFET is turned off, a resonant circuit is formed by $L_R$, $C_D$, and $C_S$. During the resonance, $v_D$ falls to zero and diode $D$ turns on. This results in yet another resonant circuit formed by $L_R$ and $C_S$. Resonance in this circuit reduces $v_S$ to zero, allowing the MOSFET to turn on without loss.

The waveforms shown in Fig. 2.2(b) clearly indicate that the ZVS-MRC concept is very suitable for high-frequency power conversion. All the parasitic oscillations caused by the major parasitic reactances are under control. In fact, the parasitic inductances and capacitances are used in the resonant circuit. However, if external resonant capacitors $C_{Sx}$ and $C_{Dx}$ are used, the package lead inductances of the switching devices are not utilized. Usually, these inductances are significantly smaller than the leakage inductance. In addition, it is relatively easy to minimize the package inductances using suitable packaging techniques. On the other hand, if the converter is operated at a frequency sufficiently high to allow use of the parasitic capacitances only, any package lead inductances are automatically absorbed by the resonant inductance.

The circuit diagram of a buck ZCS-MRC is shown in Fig. 2.3(a). This topology results from the addition of the resonant network of Fig. 2.1(b) to the PWM buck converter. Resonant inductors $L_S$ and $L_D$ are formed by the inher-

ent leakage inductances, $L_{lk'}$ and $L_{lk''}$, and the externally added inductances, $L_{Sx}$ and $L_{Dx}$. For optimal ZCS-MRC operation, the parasitic capacitances, $C_o$ and $C_j$, should be ideally zero. However, in practical high-frequency applications, these capacitances cannot be reduced to negligible values. As a result, parasitic oscillations are present in the waveforms shown in Fig. 2.3(b).

In ZCS-MRCs, the on-time of the gate-drive signal is maintained constant, and the off-time is adjusted to obtain regulation of the output. During the off-time, main resonant circuit is formed by $C_R$ and $L_D$. Voltage across the MOSFET and current through rectifying diode $D$ are sinusoidal. The high-frequency oscillation superimposed on the MOSFET voltage and current waveforms is caused by the resonance of $L_S$, $C_o$, and $C_R$. Usually, $C_R$ is much larger than $C_o$, and the frequency of this parasitic oscillation is (approximately) $1/(2\pi\sqrt{L_S C_o}\,)$.

When the MOSFET is turned on, the energy stored in its output capacitance is dissipated, just as in PWM converters or ZCS-QRCs. During the on-time, the main resonant circuit is formed initially by $C_R$, $L_S$ and $L_D$. As a result, current $i_D$ flowing through the freewheeling diode reduces to zero, and $D$ turns off. Subsequently, a resonance between $C_R$ and $L_S$ occurs, and a parasitic oscillation is superimposed on the diode current and voltage waveforms. This oscillation occurs in the resonant circuit formed by $C_j$, $L_D$, and $C_R$. Since, typically, $C_R$ is much larger than $C_j$, the frequency of this oscillation is approximately $1/(2\pi\sqrt{L_D C_j}\,)$. The main resonance brings $i_S$ to zero, and the MOSFET is turned off at zero-current.
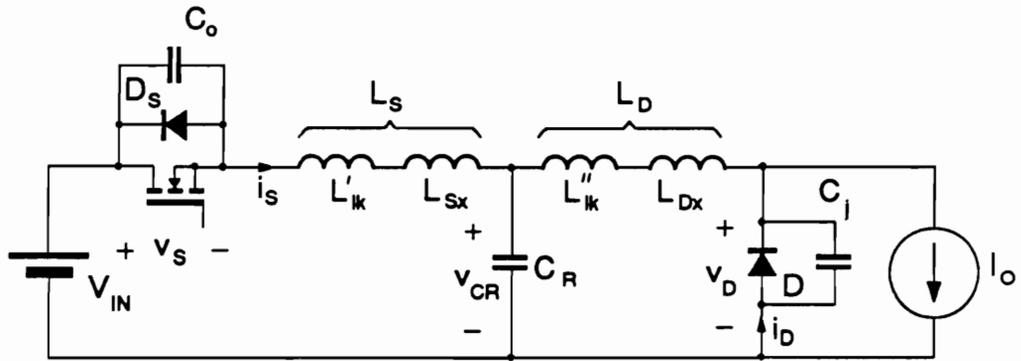
(a)
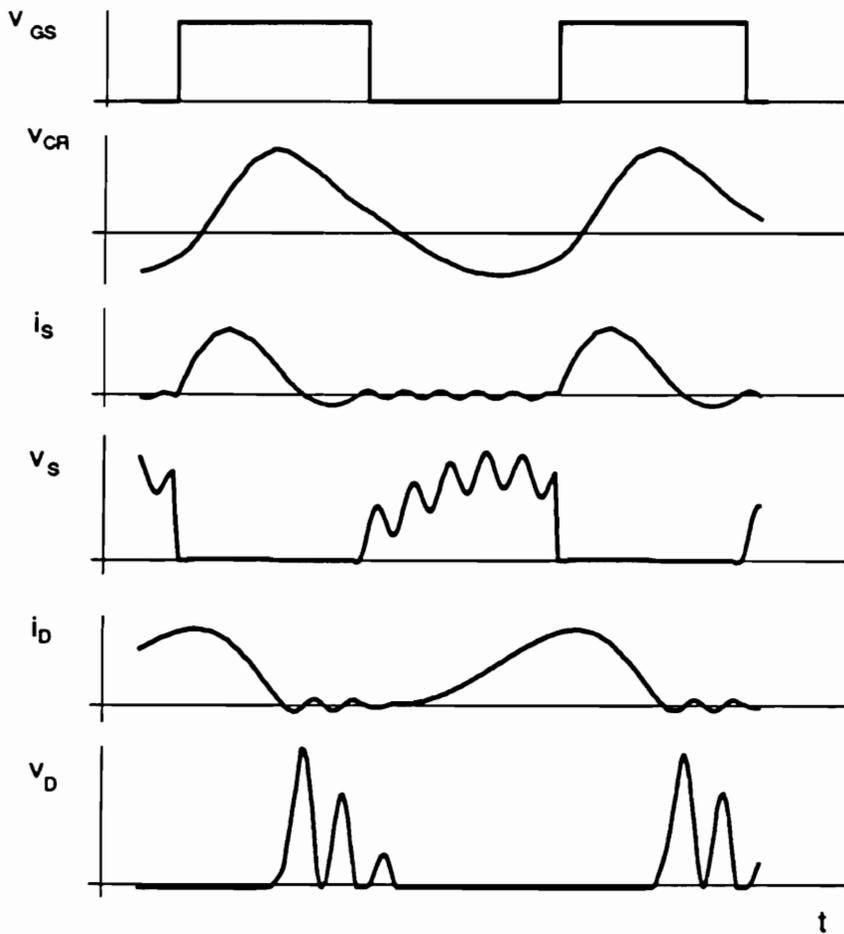


(b)

**Figure 2.3. Buck ZCS-MRC: (a) Simplified circuit diagram. (b) Typical operating waveforms.**

The waveforms and operation of the buck ZCS-MRC clearly indicate that this technique is not suitable for high-frequency applications where the leakage inductance and junction capacitances of the semiconductor devices are of primary concern. In fact, ZCS-MRCs exhibit the major problems of both ZCS-QRCs (capacitive turn-on) and ZVS-QRCs (parasitic oscillation of diode voltage). However, the ZCS-MRC technique could be very useful in high-power high-current converters using SCRs or GTOs, where inductive turn-off is of primary concern. However, since in this work the high-frequency techniques are of primary interest, the ZCS-MRC technology is not addressed in more detail.

Examination of the topology and waveforms of Fig. 2.3 leads to one more observation. Due to the presence of the parasitic capacitances of the semiconductor devices, the resonant circuit is actually formed by **five** resonant components, rather than the intended three (just as QRCs have three resonant components instead of indented two). It is conceivable that a five-element resonant network could be used to control all the resonances in a circuit of Fig. 2.3(a). This would require the use of additional resonant capacitors in parallel with $C_o$ and $C_j$, and/or an increase of the switching frequency. The practicality of such a circuit remains to be determined.

For high-frequency operation, the zero-voltage topology of Fig. 2.1(a) is clearly advantageous. This topology absorbs the parasitic output capacitance of the power FET and the junction capacitance of the rectifying diode, and provides favorable switching conditions for *both* devices. Therefore, only ZVS-MRCs are considered in the remaining part of this dissertation.

The ZVS-MRCs can be operated in either a half-wave mode, with a diode connected anti-parallel to the MOSFET, or a full-wave mode, with a diode in series with a MOSFET. However, the full-wave operation suffers from conduction losses due to the forward drop of the series diode. In addition, the series diode hinders the resonant discharge of the output capacitance of the MOSFET [D8, D49], resulting in turn-on losses similar to or even worse than those in PWM converters. This problem can be alleviated by adding a capacitance across the series diode [D49, D52]. This additional capacitance will restore the zero-voltage switching of the MOSFET, but will result in a resonant network of increased complexity compared to the original multi-resonant circuit. Due to the above reasons, only the ZVS-MRCs operating in half-wave mode are addressed in detail in this work. However, analysis of the ZCS-MRCs and full-wave ZVS-MRCs should be a subject of future investigations.

## 2.2. Basic Multi-Resonant Topologies

The procedure for converting any PWM topology into a multi-resonant topology is straightforward. To derive a ZVS-MRC from a PWM converter, the following steps are followed:

1. Resonant capacitor $C_S$ is placed in parallel with the active switch.
2. Resonant capacitor $C_D$ is placed in parallel with the rectifier.

3. Resonant inductor $L_R$ is inserted in the loop containing the switch and the diode.

The above steps should only be viewed as a simple way of describing the relative positions of the resonant components in the converter's topology. In fact, there are many possible locations of the resonant components in the circuit. These locations can be identified by application of the capacitor and inductor shift rules [T2]. This issue is essentially identical to that found in QRCs [D11, D21, D24]. The shifting of a resonant component results in a different dc bias applied to that component but does not affect the basic operation of the circuit or waveforms of the semiconductor devices.

The six basic ZVS-MRC topologies, buck, boost, buck-boost, Cuk, Zeta, and SEPIC, are shown in Fig. 2.4. In the topologies of Fig. 2.4, the resonant capacitances are shown directly in parallel with the switching devices. This placement of resonant capacitors is usually most desirable in high-frequency converters, since it minimizes the parasitic inductance introduced between the external resonant capacitance and the junction capacitance of the device. In addition, if a converter is operated at a sufficiently high frequency, the device junction capacitances could be used as the only resonant capacitances. Then, the resonant capacitors naturally assume positions indicated in Fig. 2.4.

The resonant inductance is shown in Fig. 2.4 in series with either the active or passive switching device. Obviously, different positions of $L_R$ are possible. In general, the details of the distribution of the resonant components are not critical, as long as the converter topology reduces to that shown in Fig.

BUCK

CUK

BOOST

ZETA

BUCK-BOOST

SEPIC
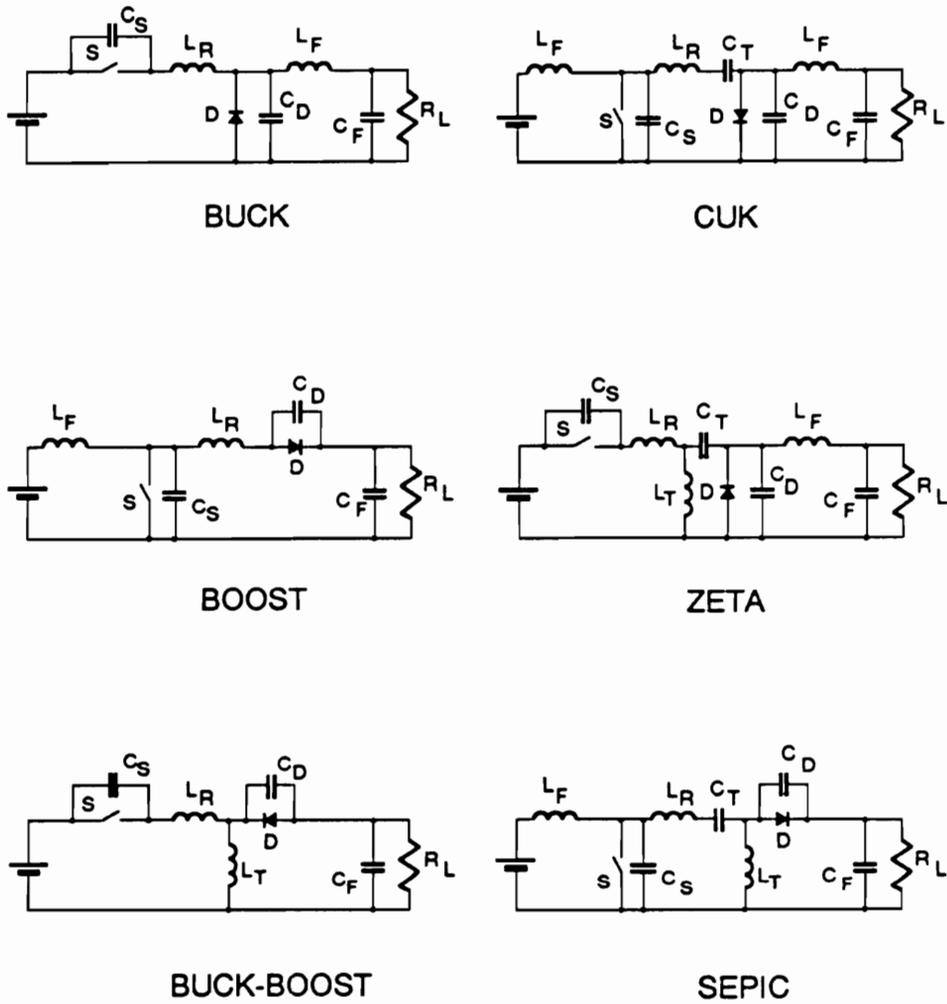
**Figure 2.4. Six basic topologies of ZVS-MRCs.**

2.1(a) when the filter capacitors and voltage sources are shorted and the filter inductors are replaced with open circuits.

## 2.3. Multi-Resonant Topologies with Isolation Transformer

In most power conversion applications, a power transformer is used in a dc/dc converter circuit to provide electrical isolation and/or desired conversion ratio. Multi-resonant converters are capable of absorbing the transformer's leakage inductance into the resonant circuit. The four basic single-ended ZVS-MRC topologies with isolation transformer are shown in Fig. 2.5. In all the converters of Fig. 2.5, resonant capacitance, $C_D$, is shown on the secondary side, directly in parallel with the rectifying diode. Placing $C_D$ on the secondary side allows absorption of the leakage inductance into the resonant circuit. In addition, at very high switching frequencies, $C_D$ can be totally provided by the junction capacitance of the rectifier. Then, $C_D$ is automatically located on the secondary side.

The disadvantage of placing the resonant capacitance on the secondary side is that the high-frequency current associated with $C_D$ will circulate through the power transformer, causing additional winding losses. Capacitance $C_D$ can be alternatively placed on the primary side of the transformer to reduce the circulating currents in the transformer. In such an arrangement, however, the leakage inductance cannot be utilized in the resonant circuit and will cause
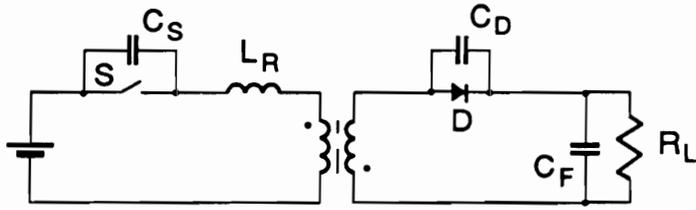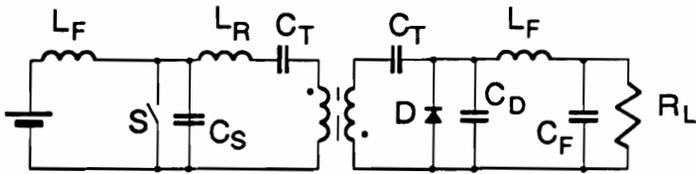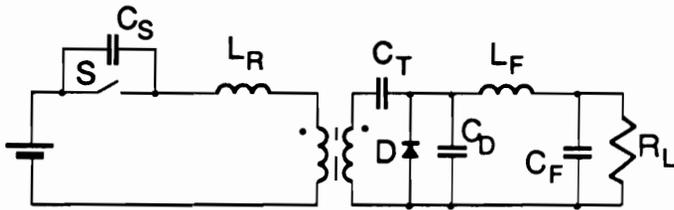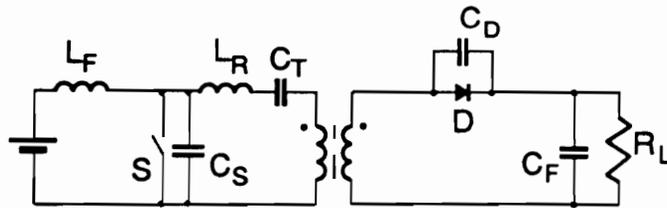
**Figure 2.5. Basic isolated topologies of ZVS-MRCs.**

parasitic oscillations by forming a resonant circuit with the junction capacitance of the rectifier.

An interesting isolated topology generated using the multi-resonant concept is the forward ZVS-MRC [H5, H6] shown in Fig. 2.6. In the forward ZVS-MRC, the resonant circuit consists of capacitance $C_S$ in parallel with the switch, resonant inductance, $L_R$, formed in part by the leakage inductance of the transformer, and resonant capacitance, $C_D$, placed on the secondary side of the transformer. The forward ZVS-MRC topology is derived from the buck ZVS-MRC by addition of the power transformer and a forward diode $D_1$. Due to the presence of $D_1$, voltage across $C_D$ can be either positive or negative. As a result, operation and characteristics of this converter are different from those of a buck ZVS-MRC. (More details on the topology and operation of forward ZVS-MRC are given in Charter 5.)

The multi-resonant switch concept can be also applied to bridge-type converters [H7, H8]. The subject of half-bridge ZVS-MRC has been treated in detail elsewhere [H9, H10] and will not be addressed in this work.

## 2.4. Experimental Converter

To demonstrate the high-frequency operation of multi-resonant converters, a buck ZVS-MRC was implemented. The circuit diagram of the converter is shown in Fig. 2.7. The converter uses a simple control circuit to regulate the
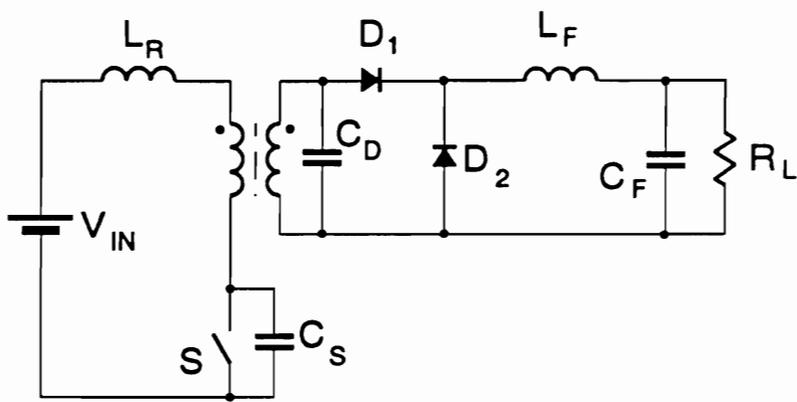
**Figure 2.6.   Forward ZVS-MRC.**

output voltage. The control circuit is not optimized for best dynamic performance. The error voltage produced by the op-amp controls the voltage controlled oscillator (VCO) formed by gates B and C. The VCO generates constant off-time pulses at a variable frequency. Power MOSFET $Q_1$ is driven by a quasi-resonant gate-drive. (Details of quasi-resonant gate drive design are given in Appendix C.)

The converter was designed with $C_N \simeq 3$ and operated with $V_{IN} = 15$ V, $V_O$ = 5 V, and a maximum output power of 20 W. Figure 2.8 shows waveforms of the circuit measured at various output power levels. The waveforms are very clean with essentially no parasitic oscillations. MOSFET voltage stress does not vary excessively as the load is varied from full load to light load.

Measured values of selected parameters are given in Table 2.1. Switching frequency varies from 4.3 MHz at full load to 7.33 MHz at less that 4% of full load. Taking into account this wide load range, the MOSFET voltage stress of less than $3V_{IN}$ is substantially reduced when compared to a voltage stress in ZVS-QRC. The MOSFET voltage stress in a ZVS-QRC with similar load range would be more than $10V_{IN}$ [D49].

## 2.5. Summary

A large family of multi-resonant topologies is proposed. It is shown that any PWM topology can be converted into a ZCS or ZVS multi-resonant
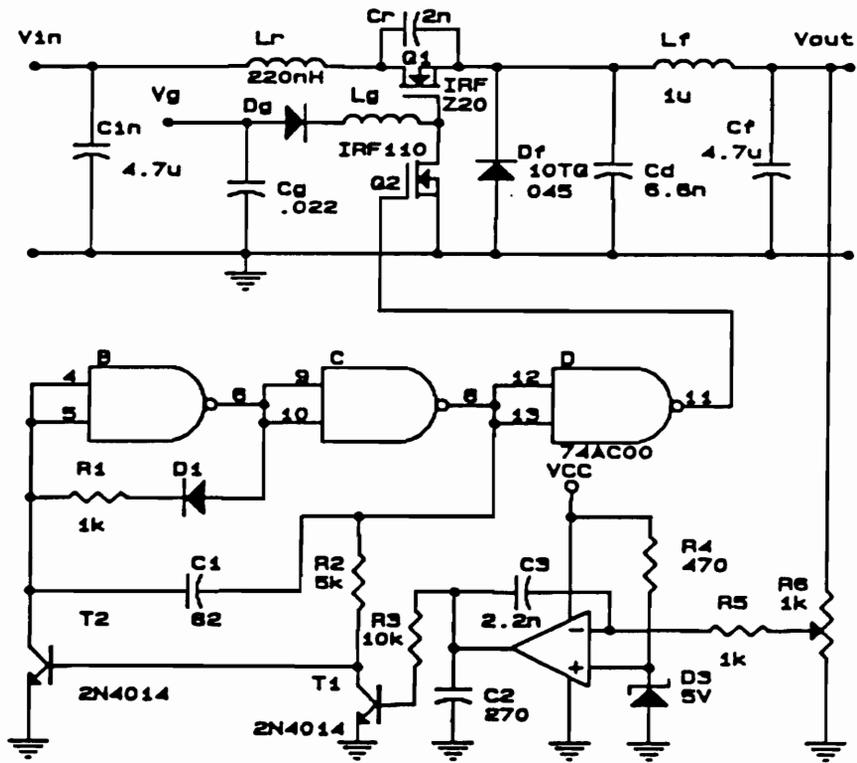
**Figure 2.7.** Circuit diagram of an experimental high-frequency buck ZVS-MRC.
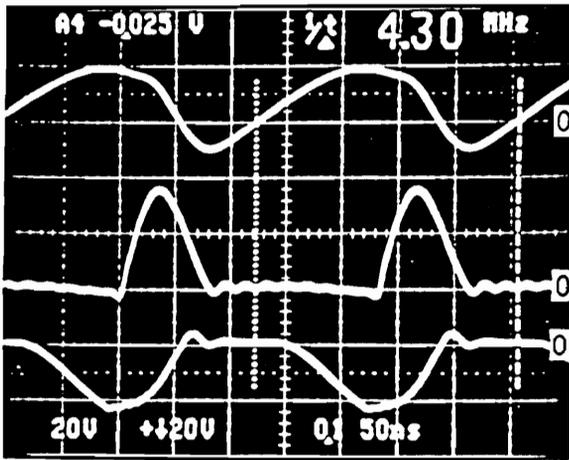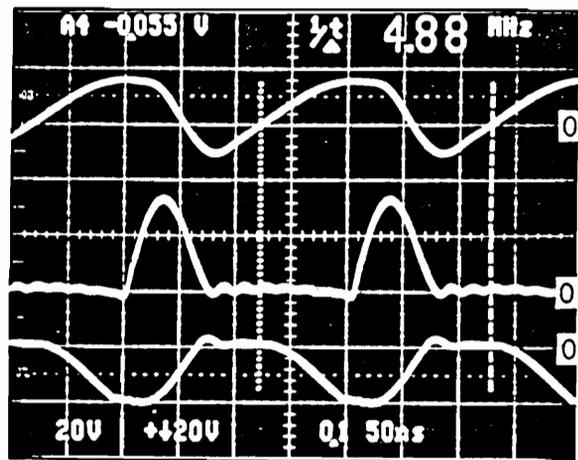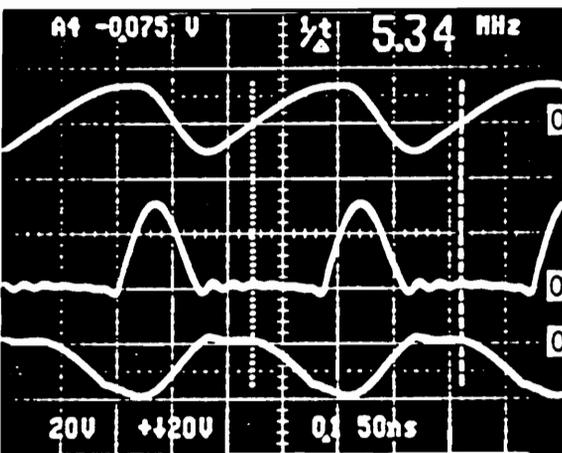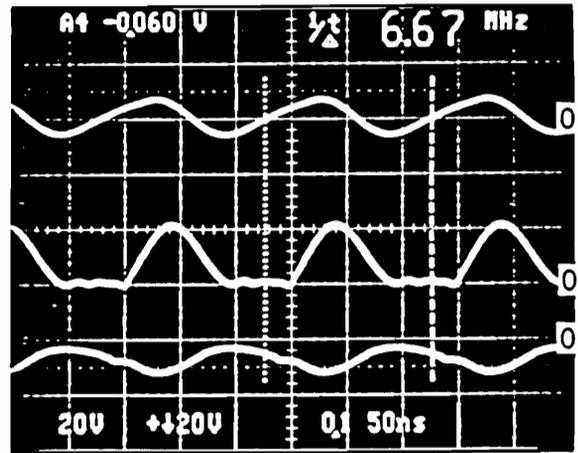
Figure 2.8. Experimental waveforms of a buck ZVS-MRC: (a) $f = 4.3$ MHz, $P_O = 20$ W. (b) $f = 4.88$ MHz, $P_O = 12.5$ W. (c) $f = 5.34$ MHz, $P_O = 7.5$ W. (d) $f = 6.67$ MHz, $P_O = 1.5$ W. $V_{IN} = 15$ V, $V_O = 7.5$ V.

**Table 2.1.  Measured parameters of an experimental buck ZVS-MRC**

| $f$ | $I_O$ | $I_{IN}$ | $P_O$ | $P_{IN}$ | $\eta$ | $V_{DSpeak}$ | $I_{Dpeak}$ |
|------|------|------|-------|-------|-------|-------|-------|
| [MHz] | [A] | [A] | [W] | [W] | [%] | [V] | [A] |
| 4.30 | 2.67 | 1.77 | 20.03 | 26.55 | 75.4 | 37.0 | 4.30 |
| 4.72 | 2.00 | 1.39 | 15.00 | 20.85 | 71.9 | 35.5 | 3.90 |
| 5.20 | 1.36 | 1.06 | 10.20 | 15.90 | 64.2 | 33.0 | 3.50 |
| 5.62 | 0.66 | 0.64 | 4.95 | 9.60 | 51.6 | 30.0 | 3.05 |
| 7.33 | 0.10 | 0.11 | 0.75 | 1.65 | 45.5 | 18.0 | 1.25 |

topology by addition of three resonant components to the basic topology. The ZVS-MRC topologies are more suitable for high frequency operation due to their ability to absorb the major reactances of the power stage, including the leakage inductance of the power transformer and junction capacitances of the semiconductor devices. In ZVS-MRCs, all semiconductor devices operate with zero-voltage switching, resulting in a substantial reduction of the switching losses. One significant advantage of ZVS-MRCs over ZVS-QRCs is a dramatic reduction of the transistor voltage stress in applications with a wide load range.

# 3. DC ANALYSIS OF BASIC ZVS-MRCS

Analysis of multi-resonant converters can be performed using the three-terminal switch concept [D22-D24,T3]. The generalized switch approach simplifies the analysis of various converter topologies, by identifying a common nonlinear switch network for all basic topologies. Then, the analysis is reduced to a derivation of an equivalent average model of the three-terminal switch.

This chapter presents a dc analysis of the basic ZVS-MRCs operating in half-wave, continuous-conduction mode. For clarity of presentation, the generalized multi-resonant switch is defined so that its analysis is equivalent to analysis of the buck ZVS-MRC. The dc characteristics of other converters are obtained by a relatively straightforward manipulation of the results obtained for the buck converter.

## 3.1. Generalized ZVS Multi-Resonant Switch

The generalized, three-terminal ZVS multi-resonant switch (ZVS MRS) is shown in Fig. 3.1. The terminals are called A (active), P (passive), and C (common). The ZVS MRS consists of an active switch, S, rectifier (passive switch), D, resonant inductor, $L_R$, and two resonant capacitors, $C_S$ and $C_D$. Resonant components are located in consistency with the parasitic reactances of the power circuit. In particular, $L_R$ absorbs the transformer leakage inductance, and $C_S$ and $C_D$ absorb the transistor and rectifier junction capacitances. Diode $D_S$ represents body diode of a MOSFET. This diode will cause operation in half-wave mode. (Although full-wave operation is possible, it is not considered here for the reasons explained in Chapter 2.)

The ZVS MRS contains three reactive components: $L_R$, $C_S$, and $C_D$. To fully characterize the resonant network of ZVS MRS, three parameters must be used. The following normalized parameters are used here: resonant frequency

$$f_0 = \frac{1}{2\pi\sqrt{L_R C_S}} \quad , \tag{3.1}$$

characteristic impedance

$$Z_0 = \sqrt{\frac{L_R}{C_S}} \quad , \tag{3.2}$$

and ratio of capacitances
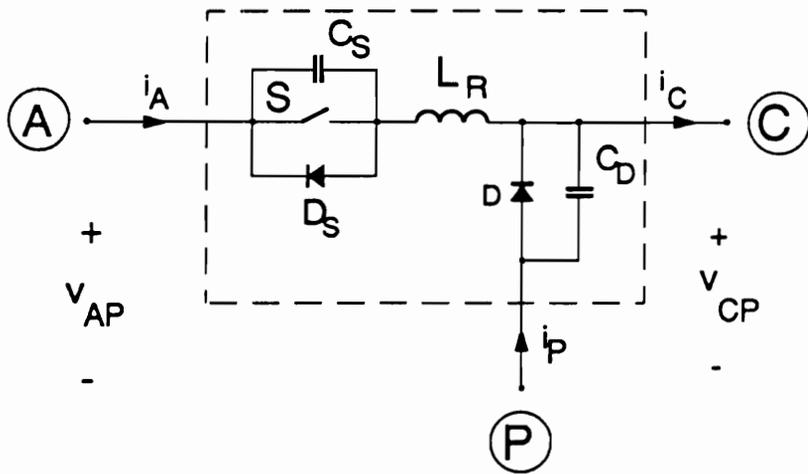
**Figure 3.1.   Generalized zero-voltage-switched multi-resonant switch.**

$$C_N = \frac{C_D}{C_S} \quad . \tag{3.3}$$

A dc voltage gain of ZVS MRS is defined as:

$$\mu_{MR} = \frac{V_{CP}}{V_{AP}} \quad , \tag{3.4}$$

where $V_{CP}$ and $V_{AP}$ are the steady-state average values of the terminal voltages $v_{CP}$ and $v_{AP}$. In a normalized form, $\mu_{MR}$ can be represented as a function of three parameters: $C_N$, defined by (3.3), a normalized switching frequency

$$f_N = \frac{f}{f_0} \quad , \tag{3.5}$$

and a normalized current through the "common" terminal

$$I_N = \frac{I_C Z_0}{V_{AP}} \quad . \tag{3.6}$$

The relationships between the ZVS MRS and the basic converter topologies, can be established using Fig. 3.2. Figure 3.2(a) shows a conventional representation of the six basic topologies of ZVS-MRCs. Figure 3.2(b) shows the same converter topologies rearranged to show how the three-terminal switch fits into these topologies. In Fig. 3.2 the battery represents input supply, the voltage source represents output-filter capacitor paralleled with load resistance, $L_F$ is input or output filter inductance, $C_T$ is a large,

energy-transfer capacitor, $L_T$ is a large, energy-transfer inductor, and $L_R$, $C_S$, and $C_D$ are resonant components.

For each basic converter, the conversion-ratio and the normalized current can be expressed as follows.

Buck ZVS MRC:

$$M = \frac{V_O}{V_{IN}} = \frac{V_{CP}}{V_{AP}} = \mu_{MR} \quad , \tag{3.7}$$

$$I_N = \frac{I_C Z_0}{V_{AP}} = \frac{I_O Z_0}{V_{IN}} \quad . \tag{3.8}$$

Boost ZVS MRC:

$$M = \frac{V_O}{V_{IN}} = \frac{V_{AP}}{V_{AC}} = \frac{V_{AP}}{V_{AP} - V_{CP}} = \frac{1}{1 - \mu_{MR}} \quad , \tag{3.9}$$

$$I_N = \frac{I_C Z_0}{V_{AP}} = \frac{I_{IN} Z_0}{V_O} = \frac{I_O Z_0}{V_{IN}} \quad . \tag{3.10}$$

Buck/boost, Cuk, ZETA, and SEPIC ZVS MRCs:

$$M = \frac{V_O}{V_{IN}} = \frac{V_{CP}}{V_{AC}} = \frac{V_{CP}}{V_{AP} - V_{CP}} = \frac{\mu_{MR}}{1 - \mu_{MR}} \quad , \tag{3.11}$$

$$I_N = \frac{I_C Z_0}{V_{AP}} = \frac{(I_{IN} + I_O) Z_0}{(V_{IN} + V_O)} = \frac{I_O(1 + M) Z_0}{V_{IN}(1 + M)} = \frac{I_O Z_0}{V_{IN}} \quad . \tag{3.12}$$

The buck/boost, Cuk, ZETA, and SEPIC converters have identical dc conversion-ratio characteristics, except that buck/boost and Cuk converters
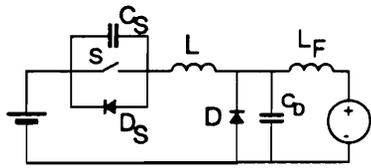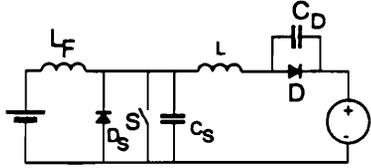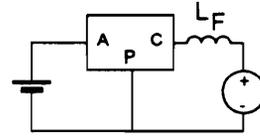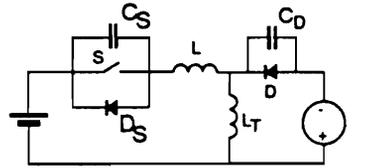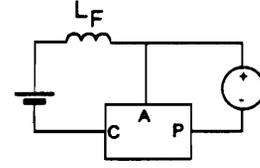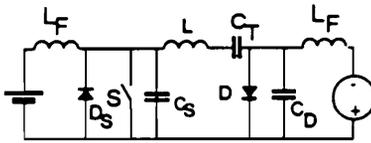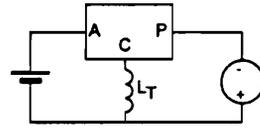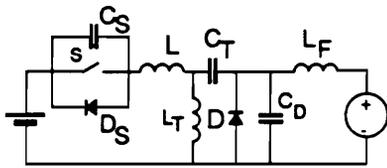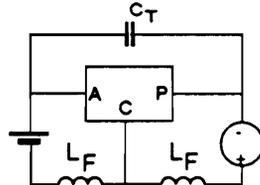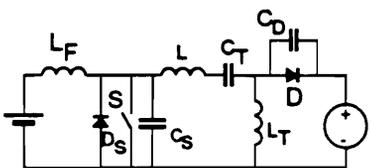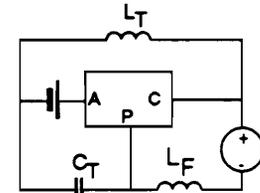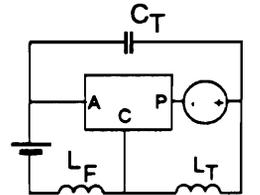
Figure 3.2.   Basic ZVS-MRCs:  (a) Circuit  diagrams.   (b) Equivalent
models using ZVS MRS.

invert the voltage. It can also be seen from (3.8), (3.10), and (3.12) that the normalized current, $I_N$, is expressed uniformly for all six converters as the normalized output current. Therefore, once voltage gain $\mu_{MR}$ is determined for the three-terminal switch, the dc conversion-ratio for each basic converter can be determined using (3.7), (3.9), and (3.11).

## 3.2. DC Analysis of Buck ZVS-MRC

Analysis of the ZVS MRS could be performed independently of any particular converter topology. However, it follows from (3.7) that $\mu_{MR}$ is simply the conversion ratio of buck ZVS MRC. For convenience and clarity of presentation, characteristics of ZVS MRS are obtained analyzing the buck topology.

A simplified circuit diagram of a buck ZVS-MRC is shown in Fig. 3.3. Diode $D_S$ represents the MOSFET's antiparallel diode. The following assumptions are used in the analysis:

1. The output filter inductance is very large, and the output filter and load can be represented by a constant current source, $I_O$.

2. All components are ideal, *i.e.*, all parasitic resistances are zero, and the semiconductor devices have zero conduction voltage drops and zero switching times.
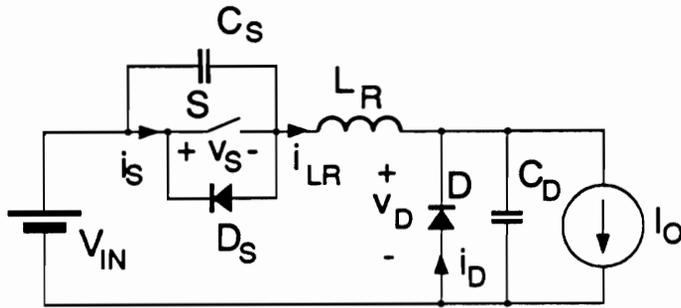
Figure 3.3.   Circuit diagram of buck ZVS-MRC.
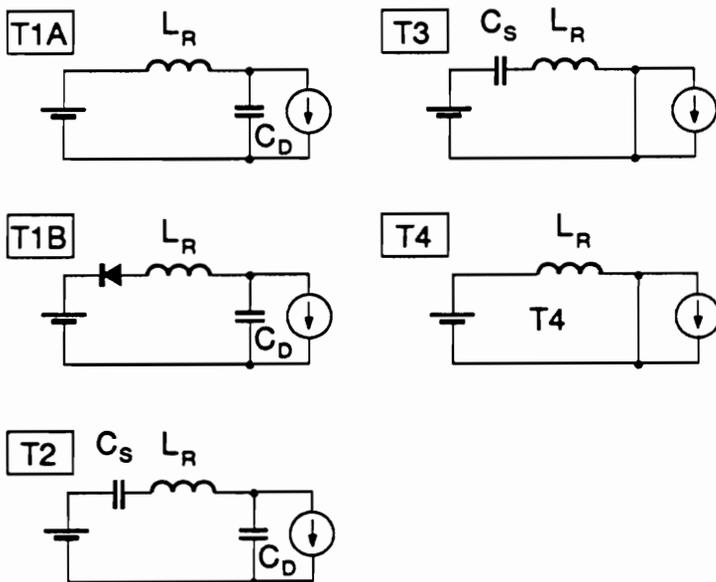


Figure 3.4.   Topological stages of buck ZVS-MRC.

Figure 3.4 shows five topological stages that the converter can enter during one switching cycle. Stages T1A and T1B are topologically identical. However, during Stage T1A, inductor current $i_{LR}$ is positive and flows through the conducting switch S. During Stage T1B $i_{LR}$ is negative and flows through diode $D_S$. The major difference between the two stages is that stage T1A can be terminated by the control signal turning off switch S, while during stage T1B, switch S does not control the circuit.

A sequence of topological stages during one cycle of circuit operation determines the **mode of operation**. Due to the complicated nature of the multi-resonant network, a large number of operating modes exist. The most practical modes are those that result in zero-voltage turn-on of switch S. Figure 3.5 indicates the two most important modes that result in zero-voltage switching. Other modes have also been identified [H17]. The flowchart shown in Fig. 3.5 explains the algorithm used for calculation of the dc characteristics. The two operating modes will be referred to as T1A-T2-T3-T4 and T1A-T2-T1B-T4, according to the sequence of topological stages characteristic to each mode. Typical waveforms associated with each mode are shown in Figs. 3.6 and 3.7. Tables 3.1 through 3.5 show state equations and their solutions in the time domain for each topological stage. To simplify notation in Tables 3.1-3.5, time is referenced to the beginning of each topological stage.

The algorithm starts with stage T1A and initial conditions $i_{LR}(0) = I_O$, $v_S(0) = 0$, and $v_D(0) = 0$. It can be seen from (3.13.i) that during stage T1A voltage $v_D$ is always positive and consequently, diode $D$ is reverse-biased.
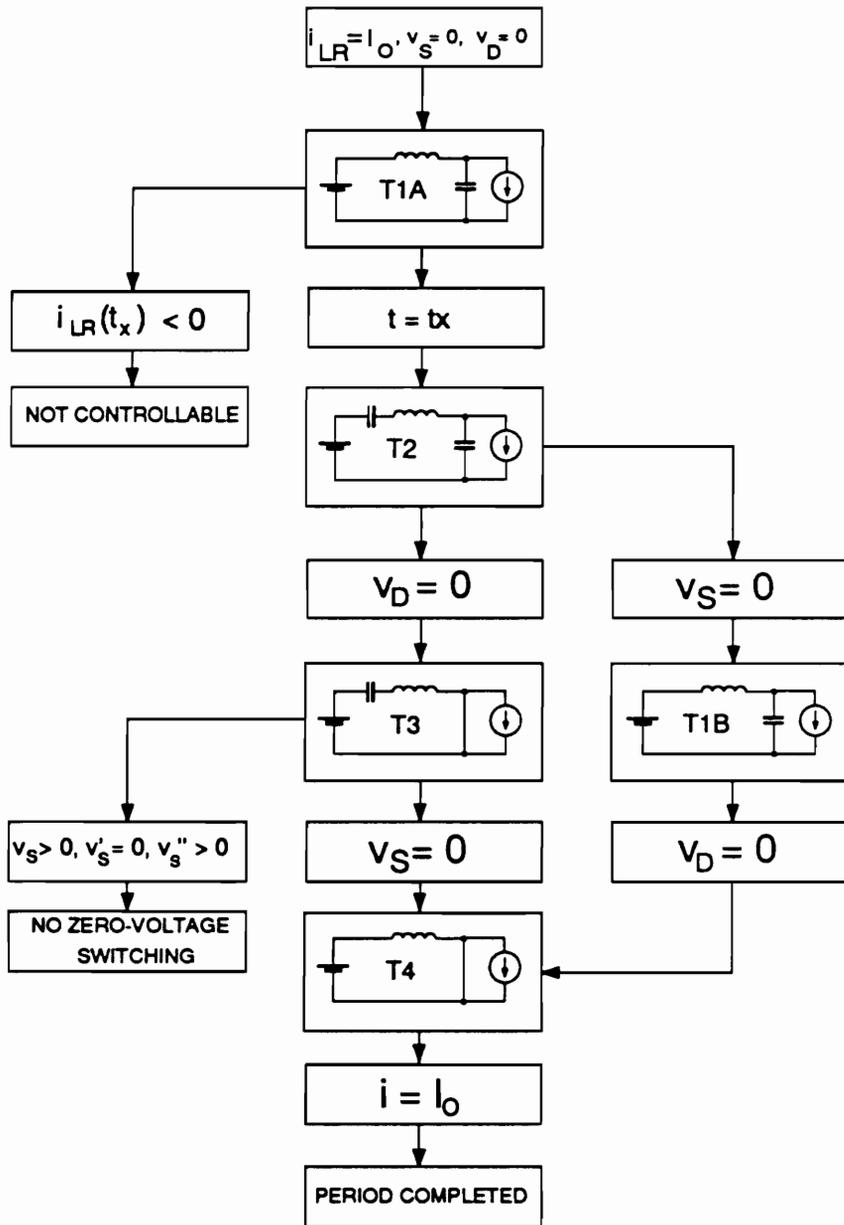
**Figure 3.5. Topological modes and switching conditions for buck ZVS-MRC.**
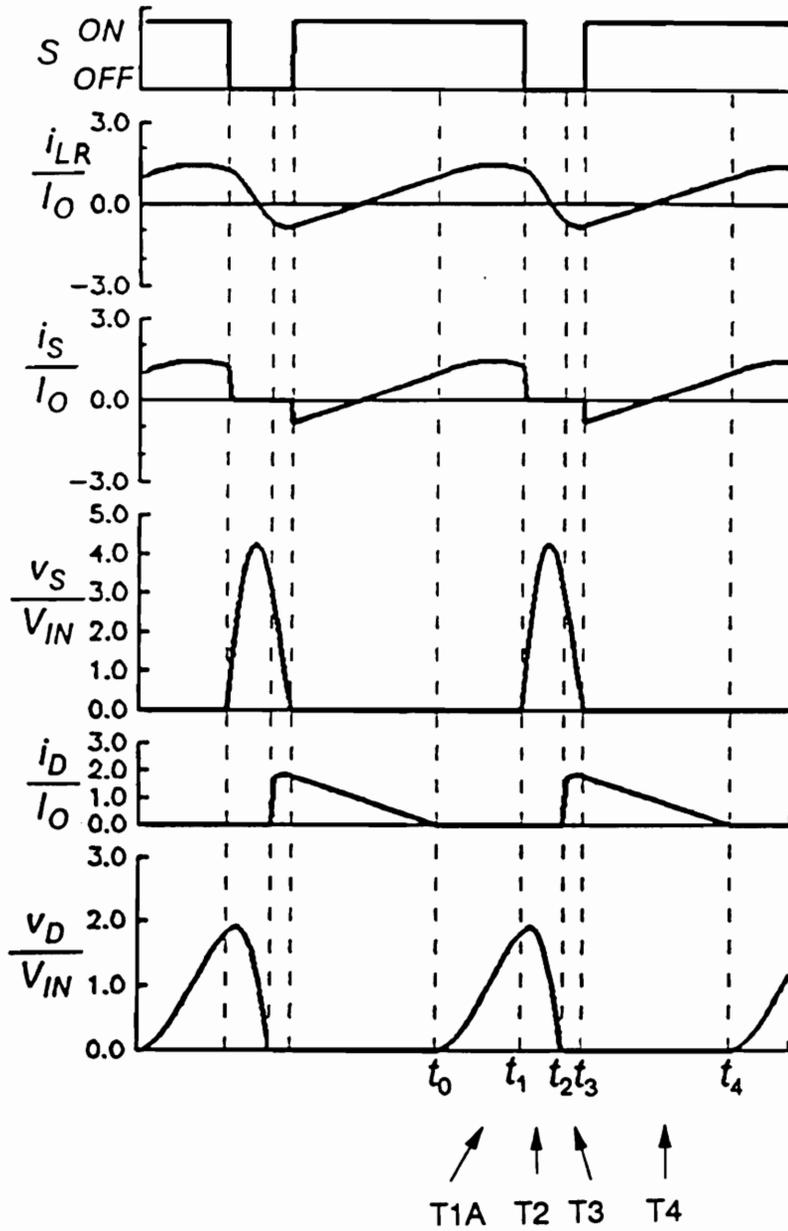
**Figure 3.6.** **Typical waveforms of buck ZVS-MRC in mode T1A-T2-T3-T4.**
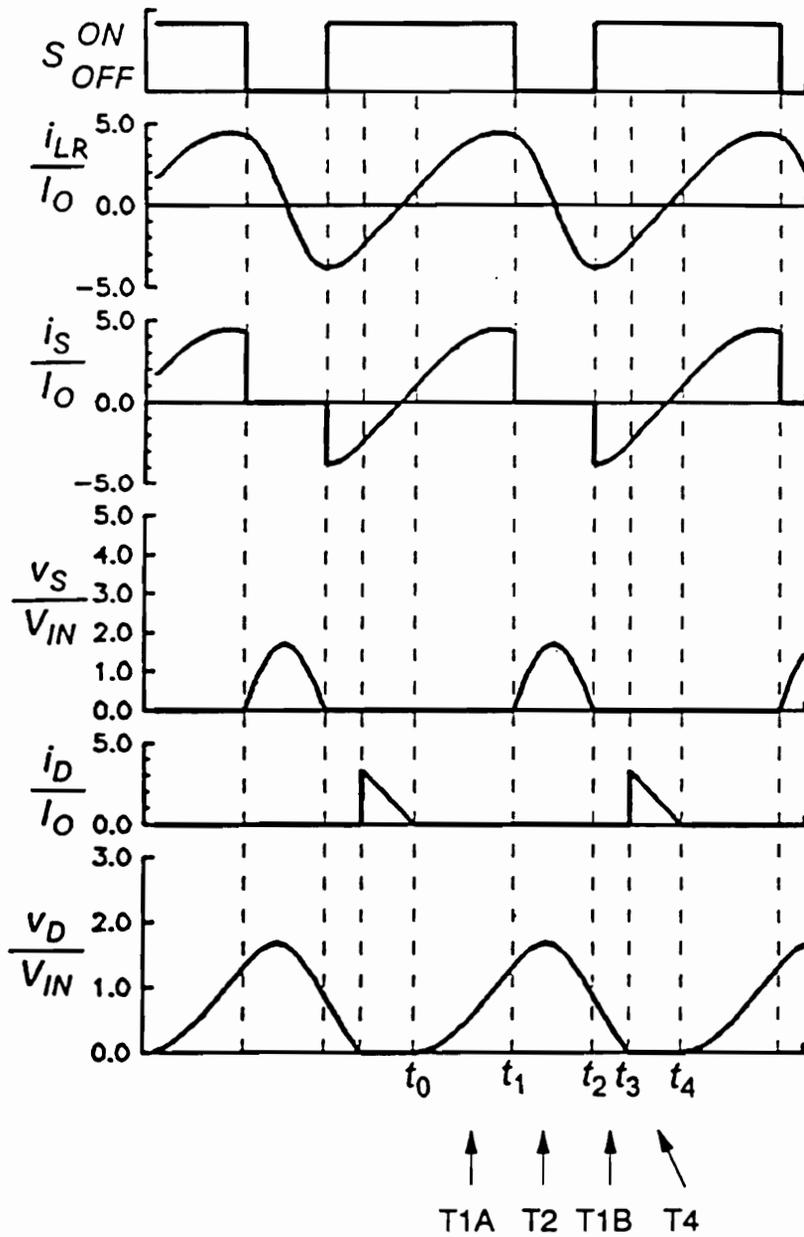
**Figure 3.7.** Typical waveforms of buck ZVS-MRC in mode T1A-T2-T1B-T4.

## Table 3.1. Topological stage T1A.

---

**Initial Conditions**



$$i_{LR}(0) = I_O \qquad (3.13.a)$$

$$v_S(0) = 0 \qquad (3.13.b)$$

$$v_D(0) = 0 \qquad (3.13.c)$$

---

**State Equations**

$$L_R \frac{di_{LR}}{dt} = V_{IN} - v_D \qquad (3.13.d)$$

$$C_S \frac{dv_S}{dt} = 0 \qquad (3.13.e)$$

$$C_D \frac{dv_D}{dt} = i_{LR} - I_O \qquad (3.13.f)$$

---

**Time-Domain Solutions**

$$i_{LR}(t) = \frac{V_{IN}}{Z_D} \sin \omega_D t + I_O \qquad (3.13.g)$$

$$v_S(t) = 0 \qquad (3.13.h)$$

$$v_D(t) = V_{IN}(1 - \cos \omega_D t) \qquad (3.13.i)$$

---

**Resonant Circuit Parameters**

$$\omega_D = \frac{1}{\sqrt{L_R C_D}} \qquad (3.13.j)$$

$$Z_D = \sqrt{\frac{L_R}{C_D}} \qquad (3.13.k)$$

---

## Table 3.2. Topological stage T1B.

---

**Initial Conditions**
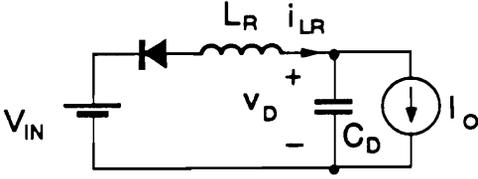


$$i_{LR}(0) \qquad (3.14.a)$$

$$v_S(0) = 0 \qquad (3.14.b)$$

$$v_D(0) \qquad (3.14.c)$$

---

**State Equations**

$$L_R \frac{di_{LR}}{dt} = V_{IN} - v_D \qquad (3.14.d)$$

$$C_S \frac{dv_S}{dt} = 0 \qquad (3.14.e)$$

$$C_D \frac{dv_D}{dt} = i_{LR} - I_O \qquad (3.14.f)$$

---

**Time-Domain Solutions**

$$i_{LR}(t) = [V_{IN} - v_D(0)] \frac{1}{Z_D} \sin \omega_D t + [i_{LR}(0) - I_0] \cos \omega_D t + I_0 \qquad (3.14.g)$$

$$v_S(t) = 0 \qquad (3.14.h)$$

$$v_D(t) = V_{IN}(1 - \cos \omega_D t) + v_D(0) \cos \omega_D t + Z_D[i_{LR}(0) - I_0] \sin \omega_D t \qquad (3.14.i)$$

---

**Resonant Circuit Parameters**

$$\omega_D = \frac{1}{\sqrt{L_R C_D}} \qquad (3.14.j)$$

$$Z_D = \sqrt{\frac{L_R}{C_D}} \qquad (3.14.k)$$

---

## Table 3.3. Topological stage T2.

---

**Initial Conditions**



$$i_{LR}(0) \tag{3.15.a}$$

$$v_S(0) = 0 \tag{3.15.b}$$

$$v_D(0) \tag{3.15.c}$$

---

**State Equations**

$$L_R \frac{di_{LR}}{dt} = V_{IN} - v_D - v_S \tag{3.15.d}$$

$$C_S \frac{dv_S}{dt} = i_{LR} \tag{3.15.e}$$

$$C_D \frac{dv_D}{dt} = i_{LR} - I_O \tag{3.15.f}$$

---

**Time-Domain Solutions**

$$i_{LR}(t) = i_{LR}(0) \cos \omega_{SD}t + \frac{I_O C_S}{C_S + C_D}(1 - \cos \omega_{SD}t) + [V_{IN} - v_D(0)]\frac{1}{Z} \sin \omega_{SD}t \tag{3.15.g}$$

$$v_S(t) = \frac{i_{LR}(0) \sin \omega_{SD}t}{\omega_{SD}C_S} + \frac{I_O t}{C_S + C_D} - \frac{I_O \sin \omega_{SD}t}{\omega_{SD}(C_S + C_D)} \tag{3.15.h}$$

$$+ [V_{IN} - v_D(0)]\frac{C_D}{C_S + C_D}(1 - \cos \omega_{SD}t)$$

$$v_D(t) = v_D(0) + \frac{i_{LR}(0) \sin \omega_{SD}t}{\omega_{SD}C_D} + [V_{IN} - v_D(0)]\frac{C_S}{C_S + C_D}(1 - \cos \omega_{SD}t) \tag{3.15.i}$$

$$- \frac{I_O t}{C_S + C_D} - \frac{I_O}{\omega_{SD}C_D}\frac{C_S}{C_S + C_D} \sin \omega_{SD}t$$

---

**Resonant Circuit Parameters**

$$\omega_{SD} = \frac{1}{\sqrt{L_R C}} \tag{3.15.j}$$

$$Z = \sqrt{\frac{L_R}{C}} \tag{3.15.k}$$

$$C = \frac{C_S C_D}{C_S + C_D} \tag{3.15.l}$$

---

## Table 3.4.  Topological stage T3.

---

**Initial Conditions**
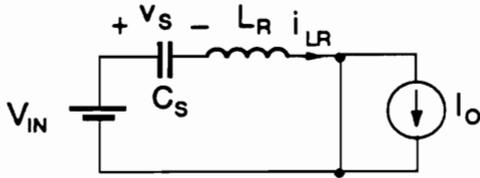


$$i_{LR}(0) \tag{3.16.a}$$

$$v_S(0) \tag{3.16.b}$$

$$v_D(0) = 0 \tag{3.16.c}$$

---

**State Equations**

$$L_R \frac{di_{LR}}{dt} = V_{IN} - v_S \tag{3.16.d}$$

$$C_S \frac{dv_S}{dt} = i_{LR} \tag{3.16.e}$$

$$C_D \frac{dv_D}{dt} = 0 \tag{3.16.f}$$

---

**Time-Domain Solutions**

$$i_{LR}(t) = [V_{IN} - v_S(0)] \frac{1}{Z_0} \sin \omega_0 t + i_{LR}(0) \cos \omega_0 t \tag{3.16.g}$$

$$v_S(t) = v_S(0) \cos \omega_0 t + Z_0 i_{LR}(0) \sin \omega_0 t + V_{IN}(1 - \cos \omega_0 t) \tag{3.16.h}$$

$$v_D(t) = 0 \tag{3.16.i}$$

---

**Resonant Circuit Parameters**

$$\omega_0 = \frac{1}{\sqrt{L_R C_S}} \tag{3.16.j}$$

$$Z_0 = \sqrt{\frac{L_R}{C_S}} \tag{3.16.k}$$

---

## Table 3.5.    Topological stage T4.

---

**Initial Conditions**
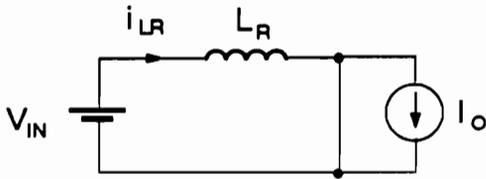


$$i_{LR}(0) \qquad (3.17.a)$$

$$v_S(0) = 0 \qquad (3.17.b)$$

$$v_D(0) = 0 \qquad (3.17.c)$$

---

**State Equations**

$$L_R \frac{di_L}{dt} = V_{IN} \qquad (3.17.d)$$

$$C_S \frac{dv_S}{dt} = 0 \qquad (3.17.e)$$

$$C_D \frac{dv_D}{dt} = 0 \qquad (3.17.f)$$

---

**Time-Domain Solutions**

$$i_{LR}(t) = \frac{V_{IN}}{L_R} t + i_{LR}(0) \qquad (3.17.g)$$

$$v_S(t) = 0 \qquad (3.17.h)$$

$$v_D(t) = 0 \qquad (3.17.i)$$

---

Therefore, the only way to terminate stage T1A is to turn off $S$ after a pre-scribed time duration, $t_x$.

Time $t_x$ represents the duration of stage T1A and is **not** identical to the on-time, but constitutes only a part of the on-time. The duration of $t_x$ affects the on-time and the switching period by determining the initial conditions for the subsequent topological stage T2. In general, it is difficult to determine $t_x$ such that the desired switching period is obtained. However, as $t_x$ is varied from zero to infinity, switching period varies from a certain minimum value to infinity. Therefore, the dc conversion-ratio characteristics can be determined by varying $t_x$ and recording both the resulting switching period and conversion ratio.

Although, the duration of $t_x$ can be adjusted from zero to infinity, not all values of $t_x$ are acceptable. It follows from (3.13.g) that if $V_{IN}/Z_D > I_O$, it is possible that for some values of $t_x$, the inductor current (given by (3.13.g)), is negative at $t = t_x$. In such a situation, diode $D_S$ is conducting and S does not control the circuit. Thus no solution for such $t_x$ can be found. If $i_{LR}(t_x) > 0$, S is turned off, and stage T2 is entered with certain initial conditions for $i_{LR}$ and $v_D$, and a zero initial condition for $v_S$.

Expressions for resonant current and voltages during stage T2 are given in Table 3.3. Stage T2 terminates when either $v_S$ falls to zero and $D_S$ turns on, or $v_D$ falls to zero and D turns on. It should be noted that, since (3.15.i) contains a linear negative term, $v_D$ will eventually fall to zero. Thus, termination of T2 is always assured for $I_O > 0$. Upon termination of T2, the circuit enters either Stage T3 or Stage T1B.

Expressions for the resonant current and voltages are given in Table 3.4 for stage T3, and in Table 3.2 for stage T1B. During Stage T3, either $v_S$ falls to zero (causing a transition to T4), or zero-voltage turn-on cannot be achieved. (Lack of zero-voltage switching is detected when both the first and second time derivatives of $v_S$ are positive, i.e., the waveform of $v_S$ increases and bends upwards.) If stage T1B is entered instead of stage T3, the resonant current and voltage are as shown in Table 3.2. Stage T1B is terminated when $v_D$ falls to zero, causing a transition to Stage T4.

It can be seen that both stages T1B and T3 are followed by stage T4. Once the circuit enters stage T4, both $v_S$ and $v_D$ are zero, and $i_{LR}$ is increasing linearly from its initial negative value. For proper operation, $S$ is turned on during T4 before $i_{LR}$ becomes positive. The inductor current increases linearly until it reaches $I_O$, resulting in a transition from T4 to T1A. This completes one cycle of operation.

To determine the conversion ratio and switching frequency, the duration of each topological stage must be determined. The duration of T1A is simply a specified time, $t_x$, and the duration of T4 can be calculated from (3.17.g), knowing that $i_{LR} = I_O$ at the end of T4.

The duration of T2 is found by numerically solving the transcendental equations (3.15.h) and (3.15.i) for final conditions $v_S = 0$ or $v_D = 0$, whichever occurs first. Since (3.15.h) and (3.15.i) can have many solutions, care must be taken while solving them. A bisection method [T4] is used. (A Newton method [T4] could be used to speed up the convergence, but it tends to be unstable because the derivatives of (3.15.h) and (3.15.i) change signs periodically.) The

durations of T3 and T1B can also be found numerically, by solving (3.16.h) for final condition $v_S = 0$ and (3.14.i) for final condition $v_D = 0$.

Once the operating mode and duration of each topological sequence are determined, the waveforms of $i_{LR}$, $v_S$, and $v_D$ are uniquely defined, and the conversion ratio can be calculated by finding an average value of $v_D/V_{IN}$ over the switching period. Expressions for time integrals of $v_D$ during each topological stage are given in Table 3.6. Listings of the FORTRAN programs used for generating the dc characteristics are given in Appendix A.

The ZVS-QRCs use a constant off-time, variable on-time control. As in ZVS-QRCs [D46], the actual duration of the off-time varies with operating conditions. However, the antiparallel diode of the MOSFET turns on when the voltage across the MOSFET drops below zero. In practical circuits, this allows operation with a constant duration of the gate-drive pulse during the off-time. The antiparallel diode automatically adjusts the effective off time.

Interesting operating conditions exist when $I_N = 1$, $C_N = 1$, and $f_N = 0.5$. Typical waveforms for a buck converter operating at these conditions are shown in Fig. 3.8. It can be seen that both the active and passive devices practically operate with both zero-voltage **and** zero-current switching. Although some transitions do not occur exactly at zero, for practical purposes these switching conditions can be considered **ideal**. However, this type of operation does not appear to be suitable for practical applications due to the high sensitivity to operating conditions.

## Table 3.6.   Analytical expressions for time integrals of diode voltage.

**Stage T1A**

$$\int_0^t v_D(t)dt = V_{IN}t + \frac{V_{IN}}{\omega_D} \sin \omega_D t \qquad (3.18)$$

**Stage T1B**

$$\int_0^t v_D(t)dt = V_{IN}t + \frac{1}{\omega_D}[v_D(0) - V_{IN}] \sin \omega_D t + \frac{1}{\omega_D}[i_{LR}(0) - I_O]Z_D(1 - \cos \omega_D t) \quad (3.19)$$

**Stage T2**

$$\int_0^t v_D(t)dt = v_D(0)t + \frac{i_{LR}(0)}{\omega_{SD}^2 C_D}(1 - \cos \omega_{SD}t) - \frac{C_S}{C_S + C_D}[V_{IN} - v_D(0)](t - \frac{1}{\omega_{SD}} \sin \omega_{SD}t)$$

$$-\frac{1}{2}\frac{I_O}{C_S + C_D}t^2 - \frac{I_O}{\omega_{SD}^2 C_D}\frac{C_S}{C_S + C_D}(1 - \cos \omega_{SD}t) \qquad (3.20)$$

**Stage T3**

$$\int_0^t v_D(t)dt = 0 \qquad (3.21)$$

**Stage T4**

$$\int_0^t v_D(t)dt = 0 \qquad (3.22)$$
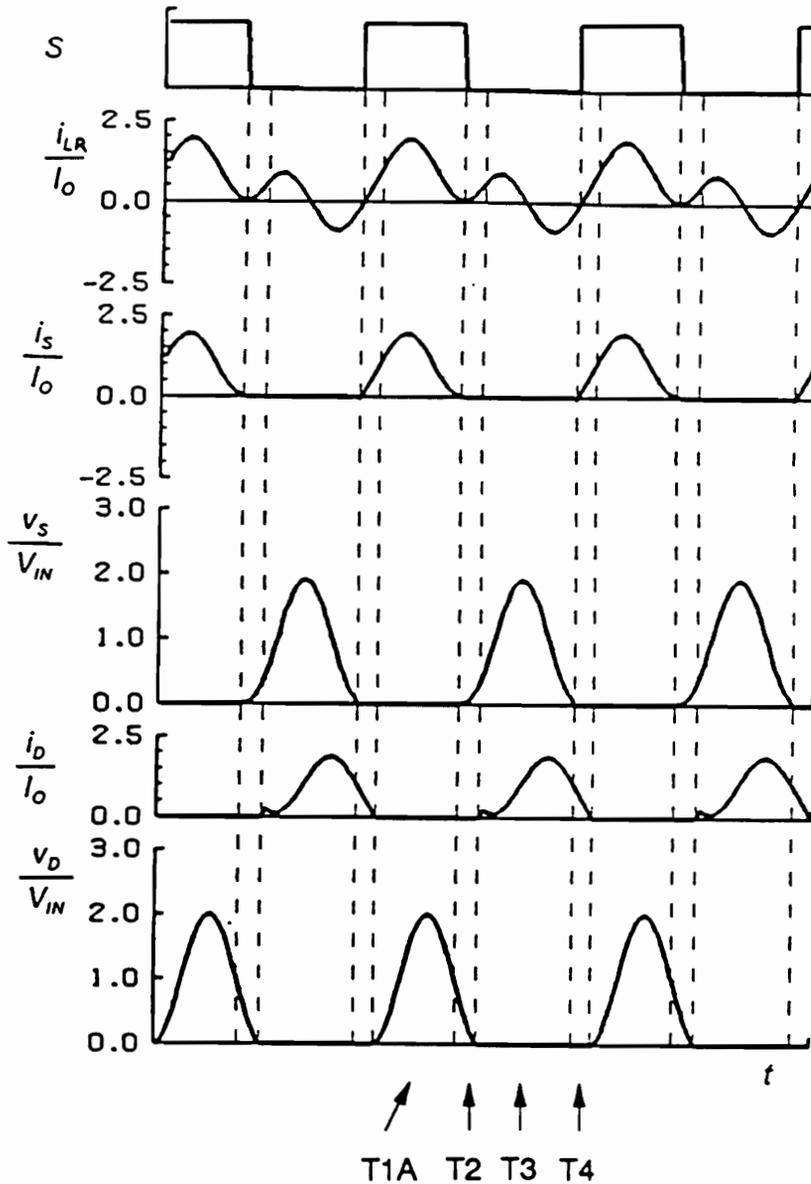
**Figure 3.8.** Special waveforms of buck ZVS-MRC: Operating conditions: $I_N = 1$, $C_N = 1$, and $f_N = 0.5$. At these operating conditions both the transistor and the diode operate with essentially zero-current and zero-voltage switching.

## 3.3. DC Characteristics of Basic ZVS-MRCs

The dc characteristics of ZVS-MRCs are determined using the algorithm of Fig. 3.5. The most straightforward way of representing the dc characteristics for a specified value of $C_N$ is to draw lines for constant values of the normalized output current, $I_N$. In order to vary switching frequency, duration of Mode T1A, $t_x$, is varied from zero to a certain maximum value. When $t_x$ is varied from zero to infinity, switching frequency varies from maximum frequency to zero. Switching frequency and conversion ratio are the output parameters of the algorithm.

Figure 3.9 shows the conversion-ratio characteristics of the buck ZVS-MRC for three values of $C_N$ with a normalized load current as a parameter. Figure 3.9(a) shows the conversion-ratio characteristics for $C_N = 1$. For heavy loads, when $I_N > 1$, the characteristics are similar to those of a buck ZVS-QRC, as shown in Fig. 1.6(b). However, for lighter loads, when $I_N \leq 1$, the ZVS-MRC (unlike the ZVS-QRC) achieves the zero-voltage switching, although only in a limited range of conversion-ratio values.

When $C_N$ is increased, zero-voltage switching is achieved for a wider range of conversion ratio at light loads, as shown in Figs. 3.9(b) and 3.9(c) for $C_N = 2$ and $C_N = 5$, respectively. It can be observed that if the minimum switching frequency is limited, it is possible to assure that the operating point is always within the region where the characteristics have a negative slope. This allows ZVS-MRCs to overcome the instability found in ZVS-QRCs. For
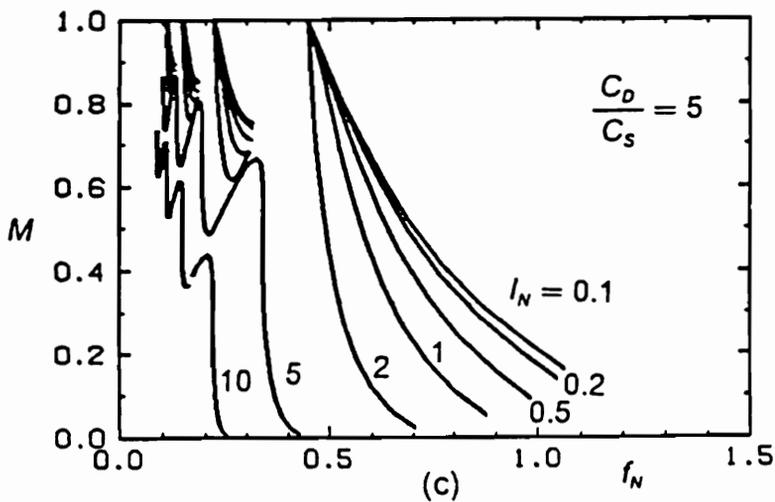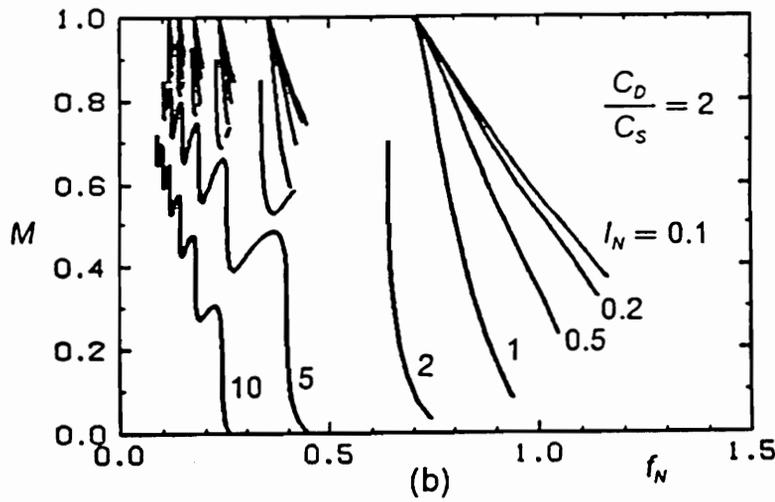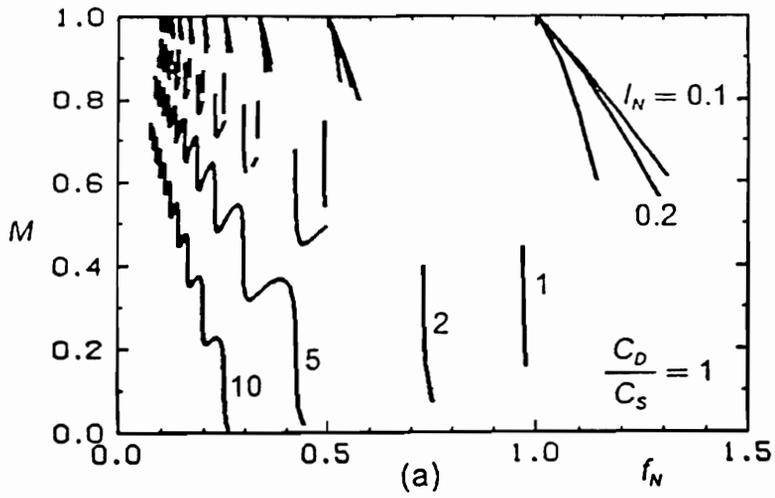
**Figure 3.9.** Conversion-ratio characteristics of buck ZVS-MRC: (a) $C_N$ = 1. (b) $C_N$ = 2. (c) $C_N$ = 3. Normalized load current $I_N$ is a running parameter.

example, Fig. 3.10(a) shows dc conversion-ratio characteristics of a buck ZVS-MRC with $C_N = 3$, for a limited range of switching frequency, $f_N > 0.5$. The line superimposed on the characteristics depicts the locus of the operating point for $M = 0.5$ and $I_N$ varying from 0 to 1.66. Figure 3.10(b) shows corresponding plots of the transistor voltage stress. The voltage stress is less than $3V_{IN}$ for all loads at $M = 0.5$.

The relatively low voltage stress combined with a very wide load range is one of the important features of ZVS-MRCs. Figure 3.11 shows typical normalized transistor voltage stress as a function of load in a buck ZVS-QRC (dotted lines) and in a buck ZVS-MRC (solid line). The voltage stress in the ZVS-QRC is proportional to the load range. For the converter with 10:1 load range (top dotted line), the voltage stress at full load is 11 times the input voltage [D49]. The ZVS-MRC operates from no load to full load with the voltage stress only three times the input voltage. Therefore, the ZVS-MRC has significantly better voltage stress characteristics than those of the ZVS-QRC.

The representation of dc characteristics of ZVS-MRCs with $I_N$ as a running parameter is simple to obtain since $I_N$ is an input parameter to the algorithm shown in Fig. 3.5. However, for design purposes, it is often convenient to use dc characteristics with normalized load resistance as a running parameter. Normalized load resistance is defined as

$$R_N = \frac{R_L}{Z_0} \quad , \tag{3.23}$$
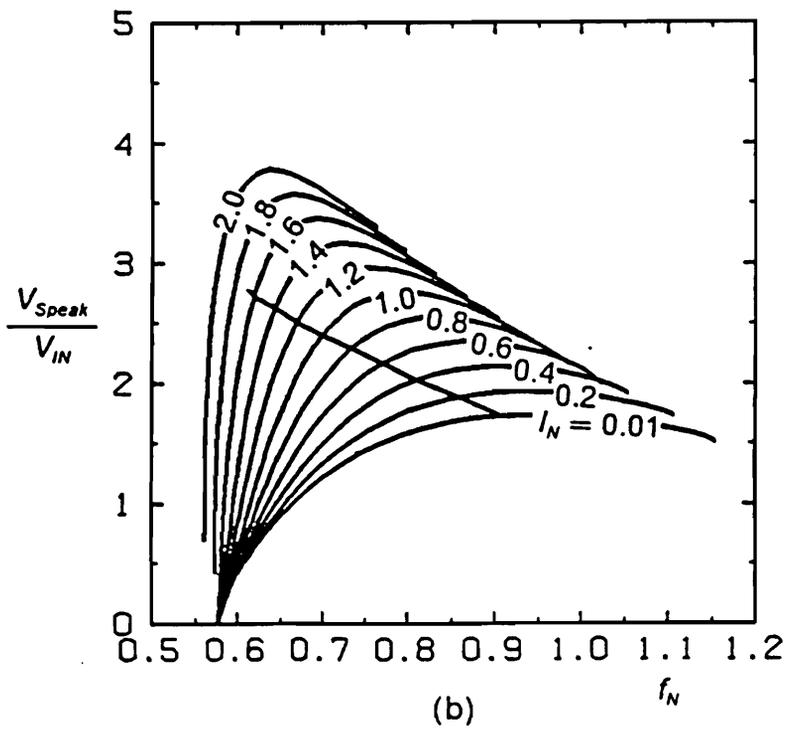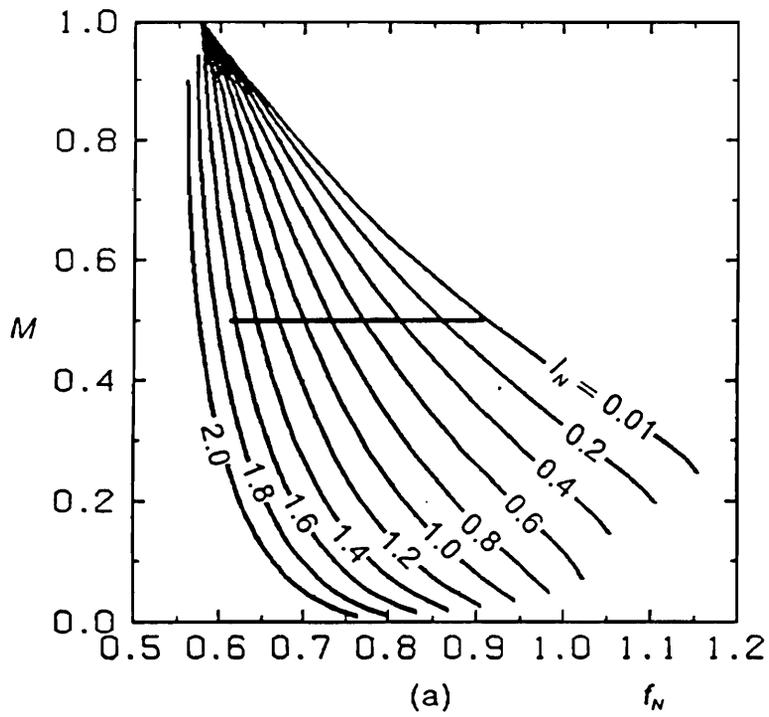
**Figure 3.10.** Example operating point loci for buck ZVS-MRC: $C_N = 3$, $M = 0.5$, and $I_N \leq 1.6$. (a) DC conversion ratio. (b) Transistor voltage stress.
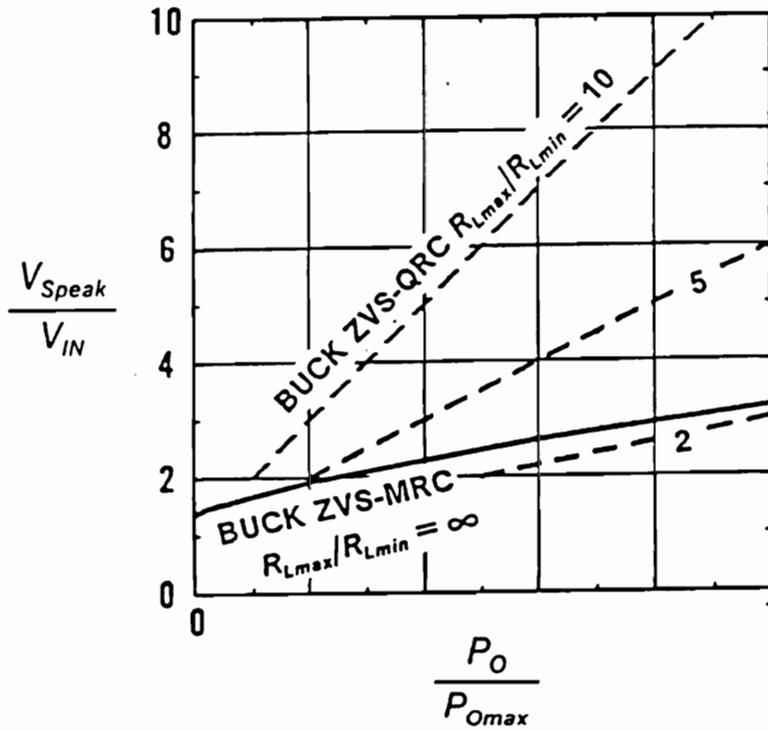
**Figure 3.11.  Comparison of transistor voltage stress in ZCS-QRC and ZVS-MRC.**

where $R_L$ is the load resistance, and $Z_0$ is the characteristic impedance defined by (3.16.k). Parameters $R_N$ and $I_N$ are related by the Ohms law in a normalized form

$$R_N = \frac{M}{I_N} \quad . \tag{3.24}$$

Since the algorithm of Fig. 3.5 does not allow *a priori* selection of $R_L$, it is necessary to use a numerical method for obtaining dc characteristics with $R_N$ as a running parameter. A Newton method can be easily implemented for this purpose, as shown in Appendix A.

Figures 3.12 through 3.14 show conversion-ratio and MOSFET voltage-stress characteristics of a buck ZVS-MRC, with $R_N$ as a running parameter. The characteristics are plotted only in the region with a negative slope.

To obtain the dc characteristics for the boost ZVS-MRC, the algorithm of Fig. 3.5 is used. The conversion ratio obtained from this algorithm is equal to the voltage gain $\mu_{MR}$ of the multi-resonant switch. Therefore, the conversion ratio of the boost converter can be found using (3.9). Figure 3.15 shows conversion-ratio and MOSFET voltage-stress characteristics of a boost ZVS-MRC with $C_N = 3$.

The dc characteristics of the buck-boost (as well as Cuk, ZETA, and SEPIC) ZVS-MRC are derived in a similar fashion, using (3.11). Figure 3.16 shows the conversion ratio and MOSFET voltage stress of a buck-boost ZVS-MRC with $C_N = 3$. Figures 3.17 through 3.19 show more detailed characteristics for other values of $C_N$.
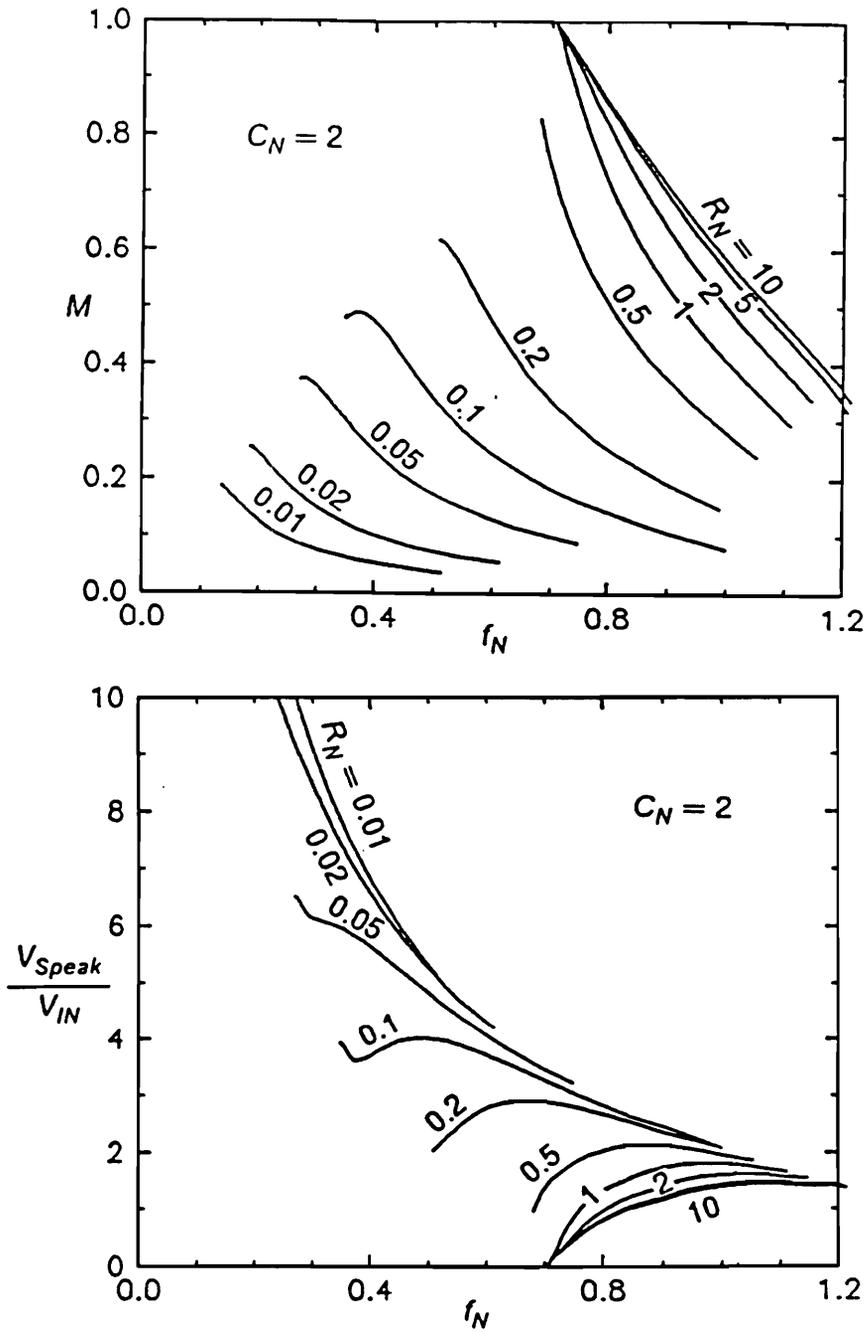
**Figure 3.12.** Conversion ratio and MOSFET voltage stress for buck ZVS-MRC: $C_N = 2$. Normalized load resistance $R_N$ is a running parameter.
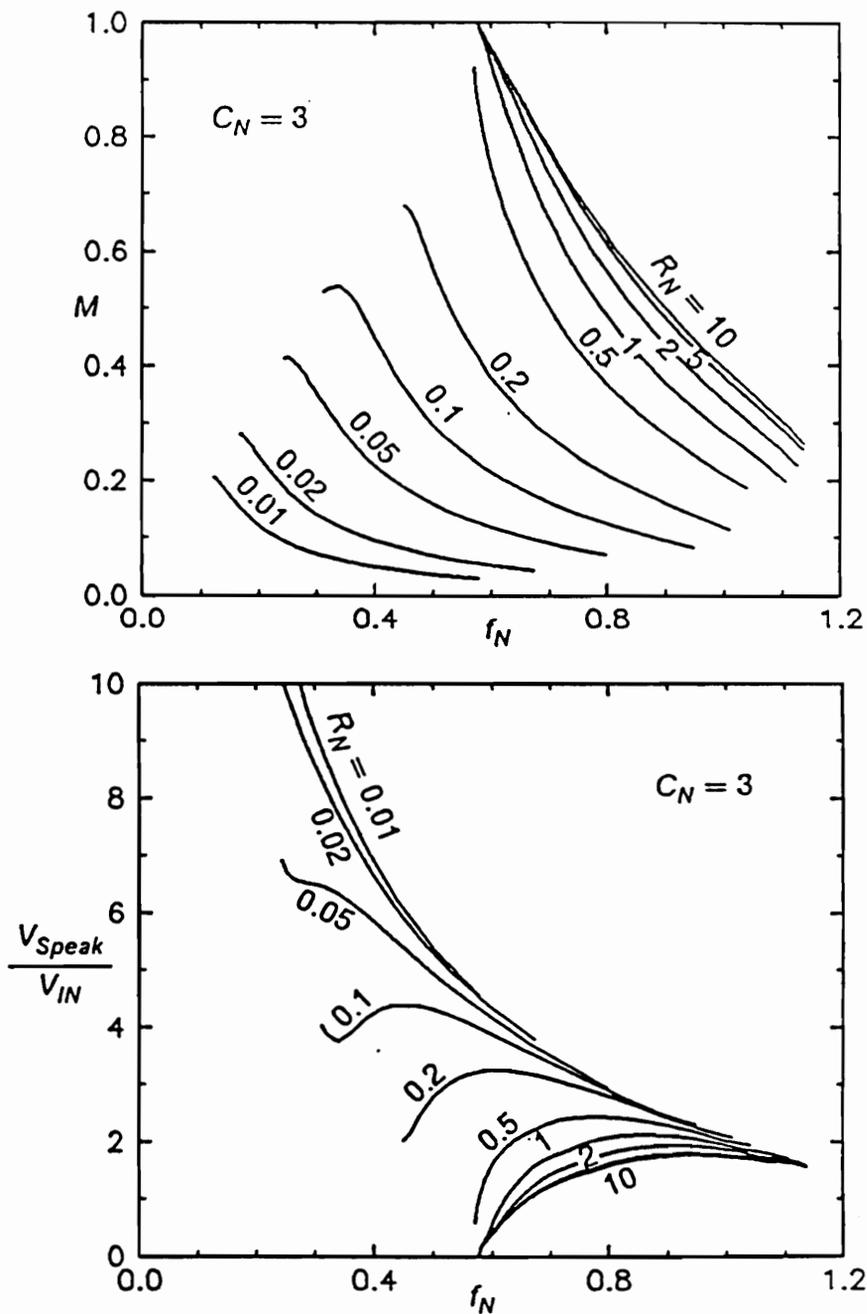
Figure 3.13. Conversion ratio and MOSFET voltage stress for buck ZVS-MRC: $C_N = 3$. Normalized load resistance $R_N$ is a running parameter.
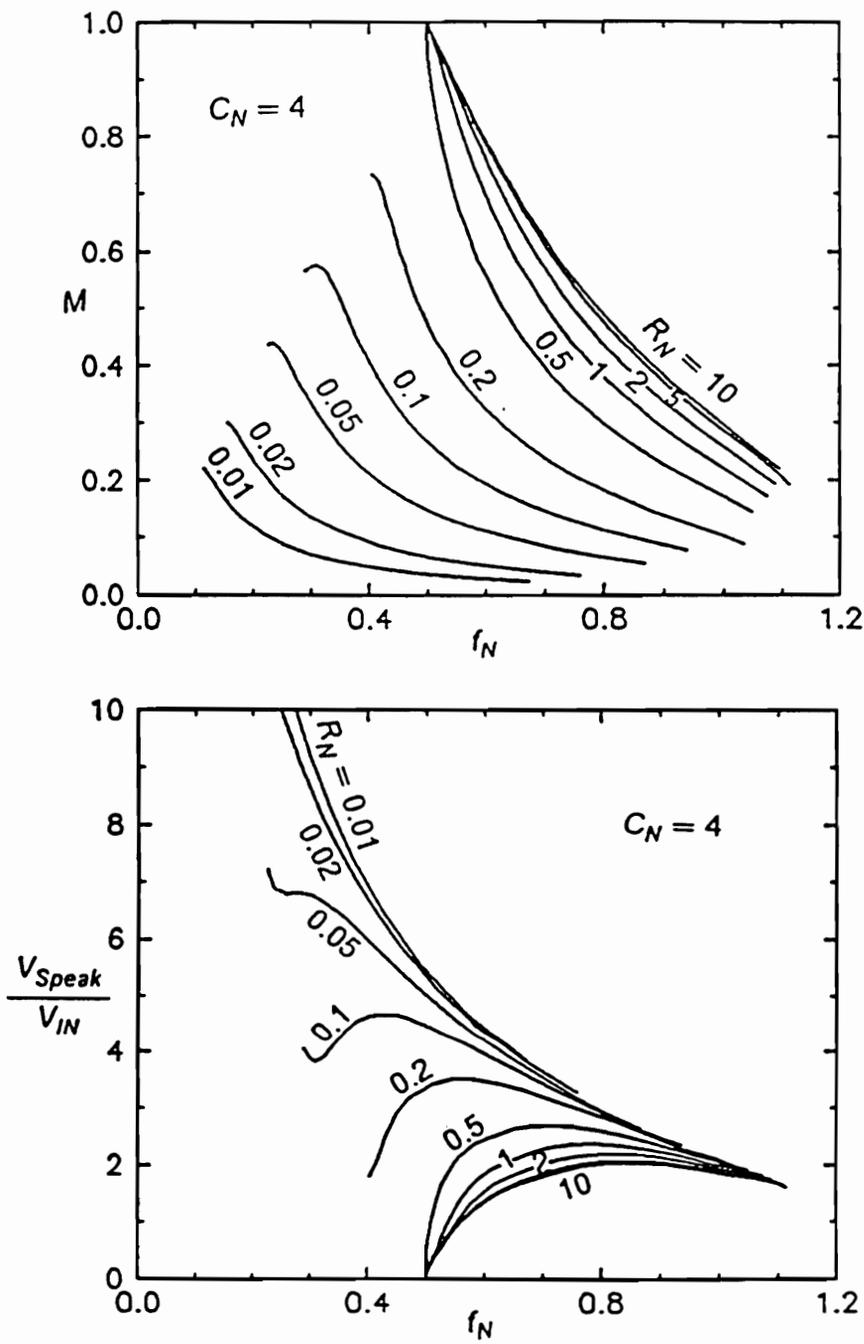
**Figure 3.14.** Conversion ratio and MOSFET voltage stress for buck ZVS-MRC: $C_N = 4$. Normalized load resistance $R_N$ is a running parameter.
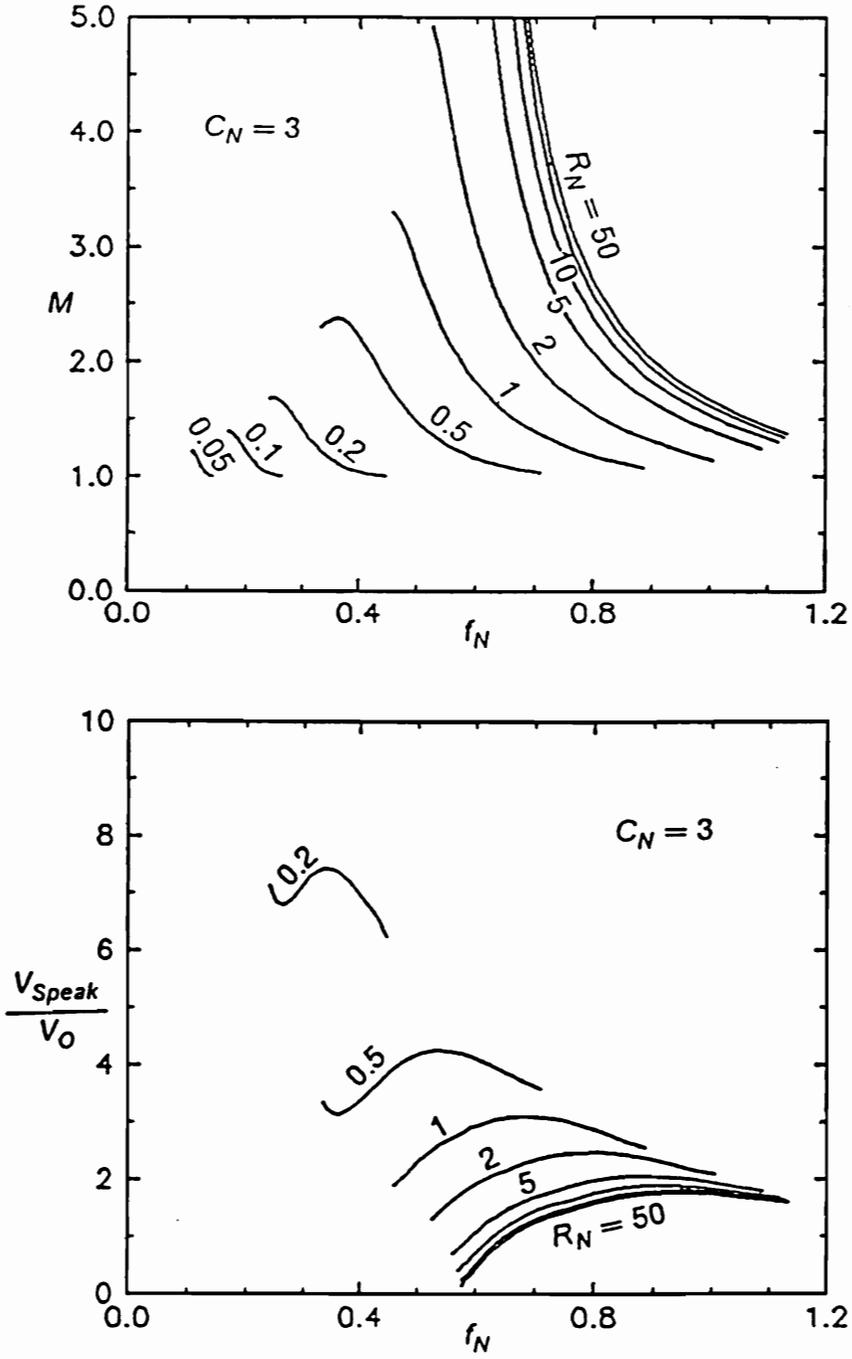
**Figure 3.15.** Conversion ratio and MOSFET voltage stress for boost ZVS-MRC: $C_N = 3$. Normalized load resistance $R_N$ is a running parameter.
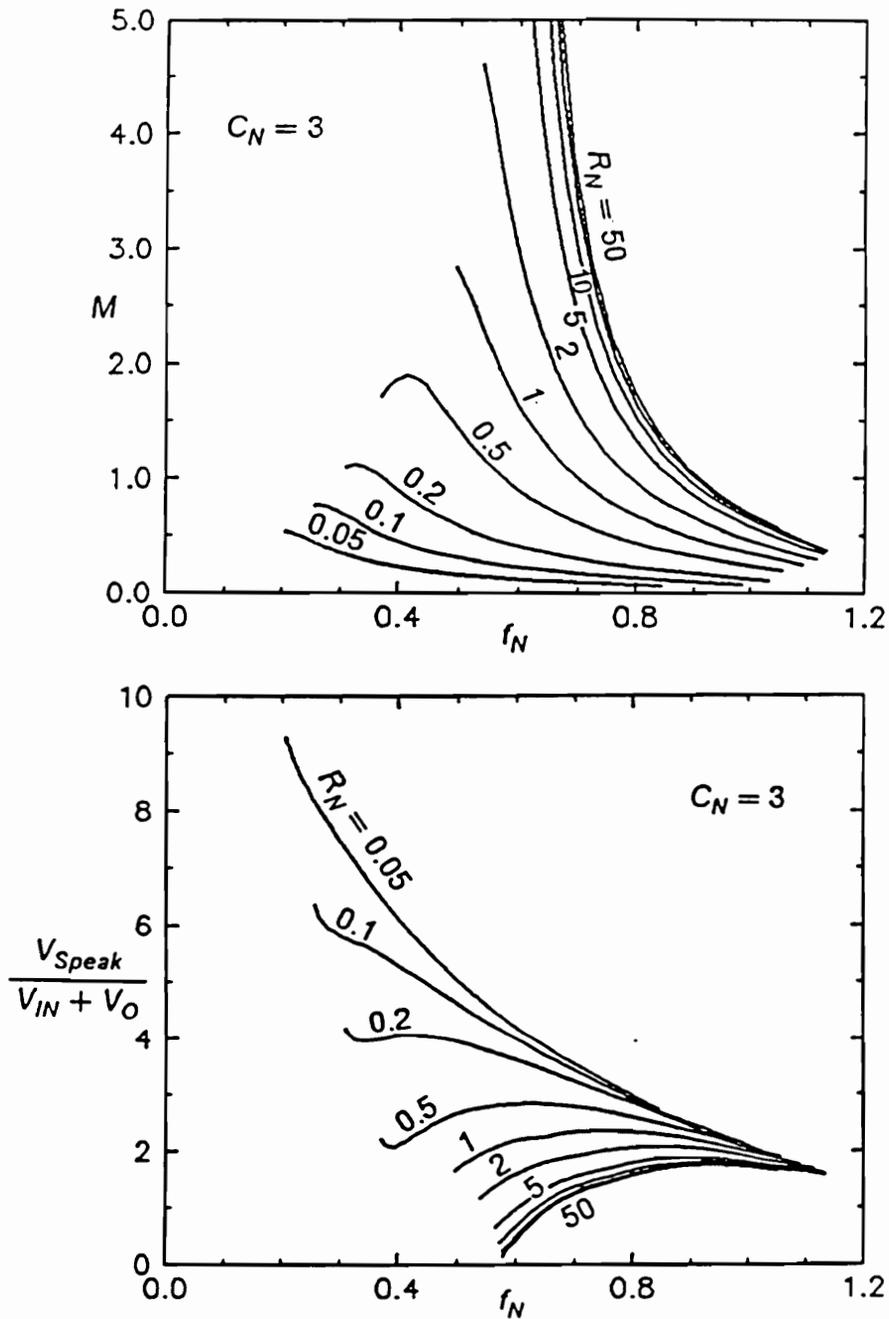
**Figure 3.16.** Conversion ratio and MOSFET voltage stress for buck-boost ZVS-MRC: $C_N = 3$. Normalized load resistance $R_N$ is a running parameter.
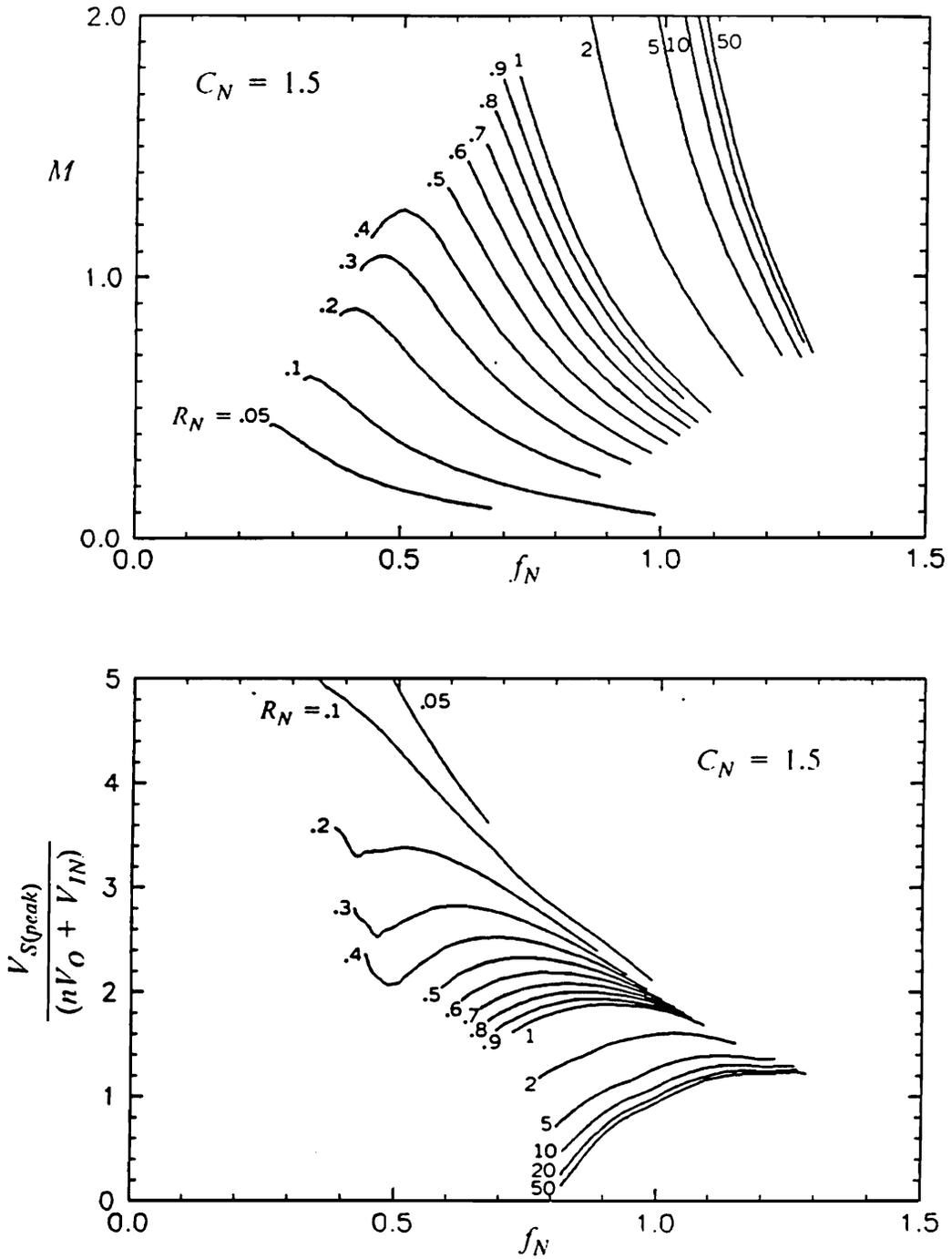
**Figure 3.17.** Conversion ratio and MOSFET voltage stress for buck-boost ZVS-MRC: $C_N = 1.5$. Normalized load resistance $R_N$ is a running parameter.
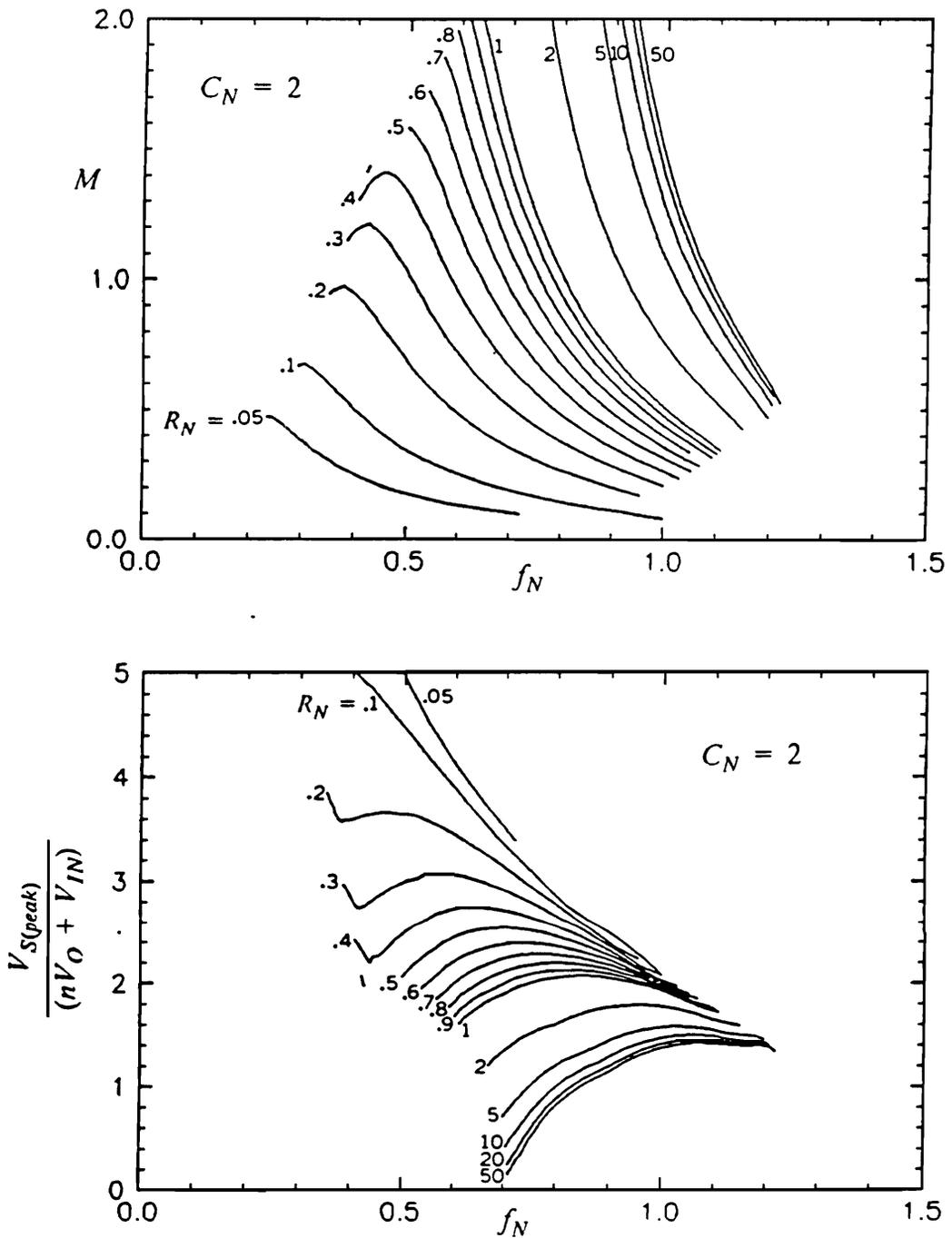
**Figure 3.18.** Conversion ratio and MOSFET voltage stress for buck-boost ZVS-MRC: $C_N = 2.0$. Normalized load resistance $R_N$ is a running parameter.
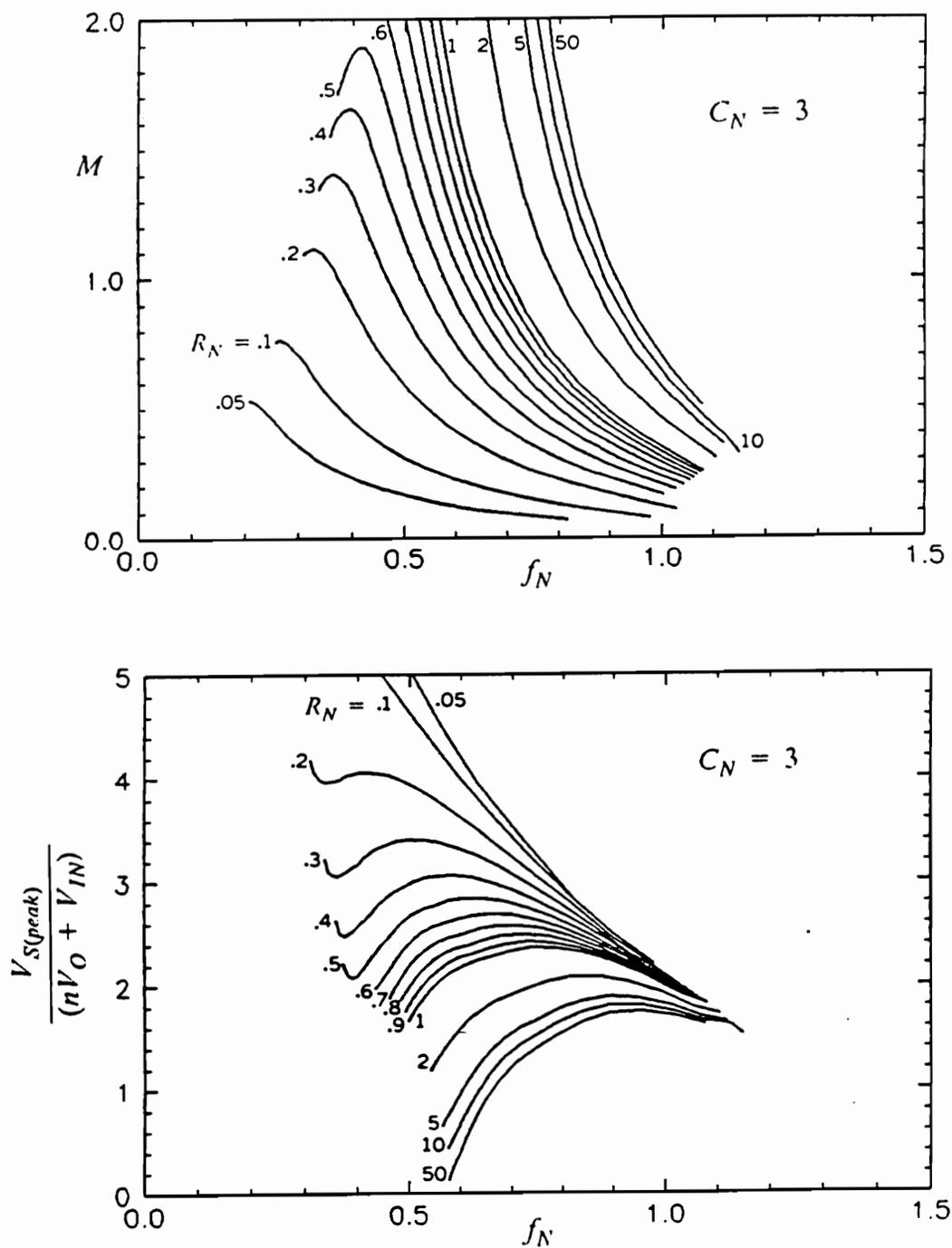
**Figure 3.19.** Conversion ratio and MOSFET voltage stress for buck-boost ZVS-MRC: $C_N = 3.0$. Normalized load resistance $R_N$ is a running parameter.

## 3.4. Experimental Verification

To verify the analysis, a buck ZVS-MRC was built with $C_N = 3$. The circuit diagram of the converter and its component values are shown in Fig. 3.20. The converter was operated open-loop, and its dc characteristics were measured at $V_{IN} = 10$ V. The experimental conversion-ratio and MOSFET voltage-stress characteristics are shown in Fig. 3.21, and are in good agreement with the theoretical characteristics of Fig. 3.13. Figure 3.22 shows experimental waveforms obtained at various operating conditions.

## 3.5. Summary

The three-terminal, generalized multi-resonant switch is used to perform dc analysis of basic ZVS-MRCs. Two operating modes with zero-voltage switching are identified as being the most important in practical applications. Conversion-ratio and MOSFET voltage-stress characteristics are derived for basic converter topologies: buck, boost, buck-boost, Cuk, Zeta, and SEPIC. The three-terminal switch concept reduces the analysis of all these topologies to a derivation of the dc characteristics for the switch, and the analysis does not need to be repeated for each topology. The theoretical characteristics are verified experimentally using a buck converter topology. It is shown, both the-oretically and experimentally, that ZVS-MRCs are characterized by a moderate
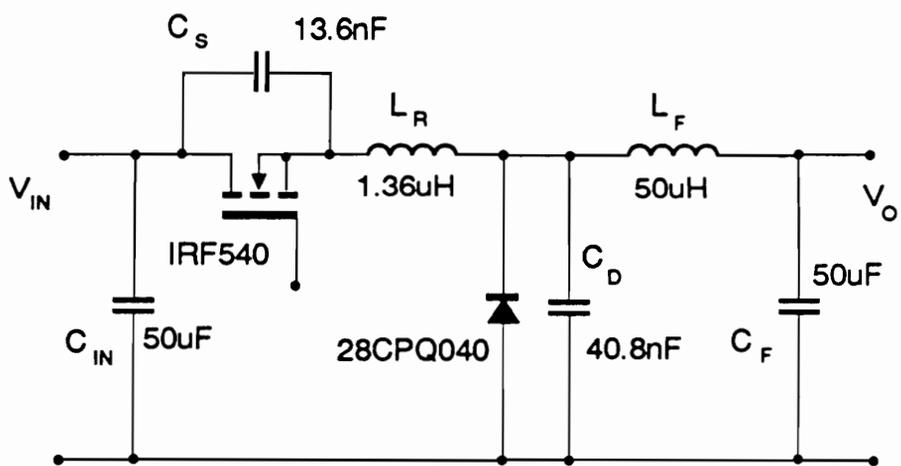
**Figure 3.20.  Circuit diagram of an experimental buck ZVS-MRC.**
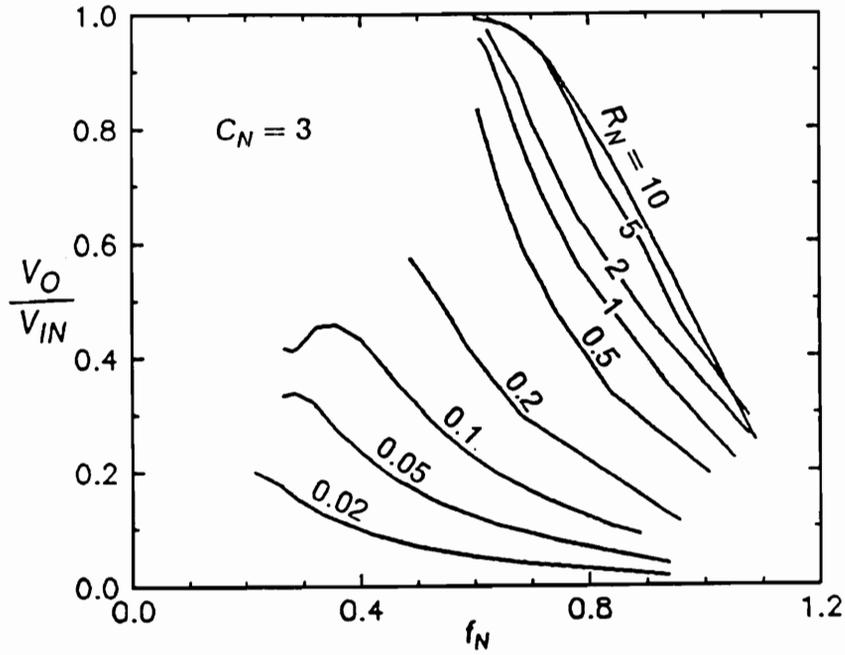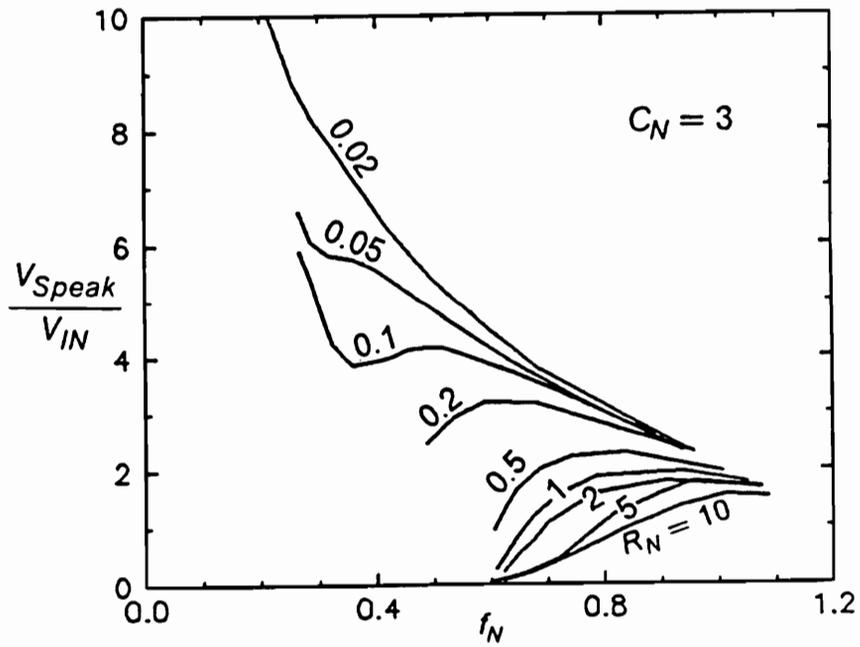
**Figure 3.21.** Measured dc characteristics of buck ZVS-MRC: (a) Conversion ratio. (b) MOSFET voltage stress.
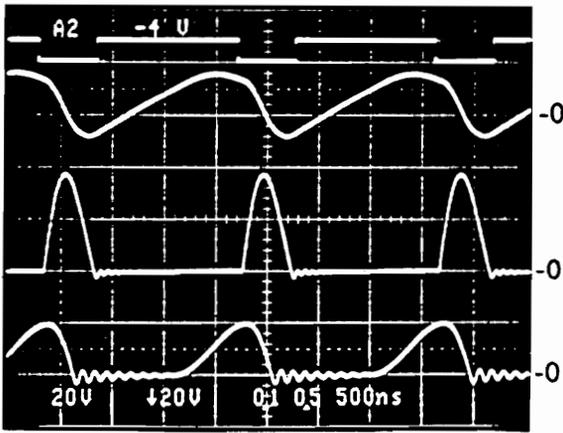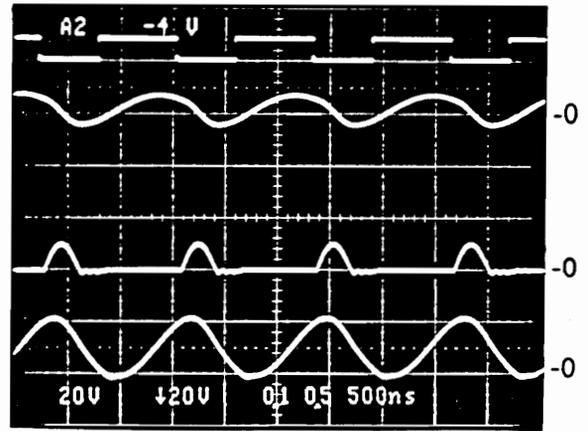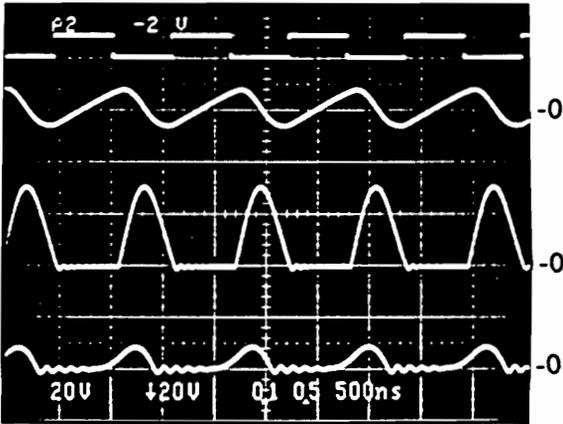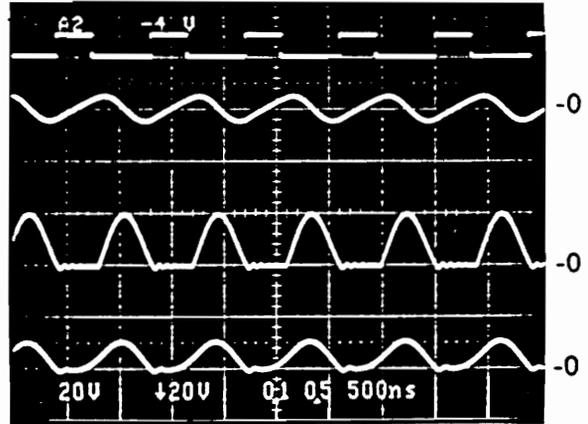
**Figure 3.22.** **Experimental waveforms of buck ZVS-MRC:**
(a) f = 522 kHz, $R_L = 1\ \Omega$, $V_O = 4.1$ V.
(b) f = 880 kHz, $R_L = 1\ \Omega$, $V_O = 1.5$ V.
(c) f = 765 kHz, $R_L = 10\ \Omega$, $V_O = 8.5$ V.
(d) f = 1130 kHz, $R_L = 10\ \Omega$, $V_O = 3.4$ V.

transistor voltage stress (of the order of 3 times the input voltage for buck converter) and a practically unlimited load range. These characteristics represent a considerable improvement over ZVS-QRCs, where a wide load range results in an excessive transistor voltage stress.

# 4. DESIGN GUIDELINES FOR ZVS-MRCS

To establish design guidelines for ZVS-MRCs, it is necessary to find the current and voltage stresses for both the active switch and rectifier, and determine trade-offs among the various stresses. In general, it is difficult to give device stresses for ZVS-MRCs using simple, analytical expressions. An example of precise stress analysis using normalized characteristics is presented for a buck ZVS-MRC. Based on the stress trade-offs, design guidelines are established, and design procedures are proposed for basic ZVS-MRCs, including buck, boost, and flyback converters.

## 4.1. Design Trade-Offs in ZVS-MRCs

To evaluate the effect of different design parameters on performance of the converter, a buck ZVS-MRC is designed using different combinations of

parameters $C_N$ and $I_{ON}$. Subsequently, stress analysis is performed to determine the design trade-offs and guidelines. The converter is designed for the following specifications:

- Input voltage range $V_{IN}$ = 10 - 20 V.
- Output voltage $V_O$ = 5 V.
- Load range $I_{OUT}$ = 0 - 5 A.
- Minimum switching frequency $f_{min}$ = 2 MHz.

From the above specifications, the conversion-ratio range is:

- $M_{min}$ = 5/20 = 0.25.
- $M_{max}$ = 5/10 = 0.5.

The first step in the design is the selection of the ratio $C_N = C_D/C_S$. Figures 4.1 and 4.2 show conversion-ratio characteristics of buck ZVS-MRC for different values of $C_N$. From the conversion-ratio characteristics it can be seen that $C_D/C_S$ should be greater than 3 to provide the required line/load regulation. It is not clear, however, what exact value of $C_D/C_S$ should be chosen.

A second parameter that needs to be chosen is the maximum normalized load current, $I_{ONmax} = (I_{Omax}Z_0)/V_{INmin}$. To investigate the effect of the $C_N$ and $I_{ONmax}$ on the converter's performance, four different designs are considered:

**Design 1:** $C_N$ = 3 and $I_{ONmax}$ = 2

**Design 2:** $C_N$ = 3 and $I_{ONmax}$ = 5

**Design 3:** $C_N = 5$ and $I_{ONmax} = 2$

**Design 4:** $C_N = 5$ and $I_{ONmax} = 5$

Figures 4.3 through 4.10 show the operating ranges stress analysis for the four selected designs. Since the procedure is identical in each case, only Design 1 is described in detail.

Figure 4.3 shows the conversion ratio characteristics of a buck ZVS-MRC at $C_N = 3$. The maximum value of the normalized output current is selected (by an arbitrary choice) as 2.0. As a result, the operating range extends over the area shaded in Fig. 4.3.

Figure 4.4 shows normalized characteristics of transistor current and voltage stresses. The normalized current stress, shown in Fig. 4.4(a), has a characteristic plateau for each value of the normalized load current. In the plateau region, the on-time is sufficiently long to result in a duration of stage T1A equal to or longer than one-fourth of the resonant period associated with T1A (*i.e.*, $\omega_D t_x \geq \pi/2$, see Chapter 3 for details). The value of the normalized current stress in the plateau region increases as the load current decreases. This is caused mainly by the fact that the load current is a normalizing factor for the current stress. As a result, normalized current stress increases to infinity as the load current reduced to zero.

To find a precise value of the current stress it would be necessary to consider every value of the normalized current stress in the operating region (shaded area in Fig. 4.4(a)) and multiply it by the corresponding output current. Such a procedure would be very impractical. However, in many practical
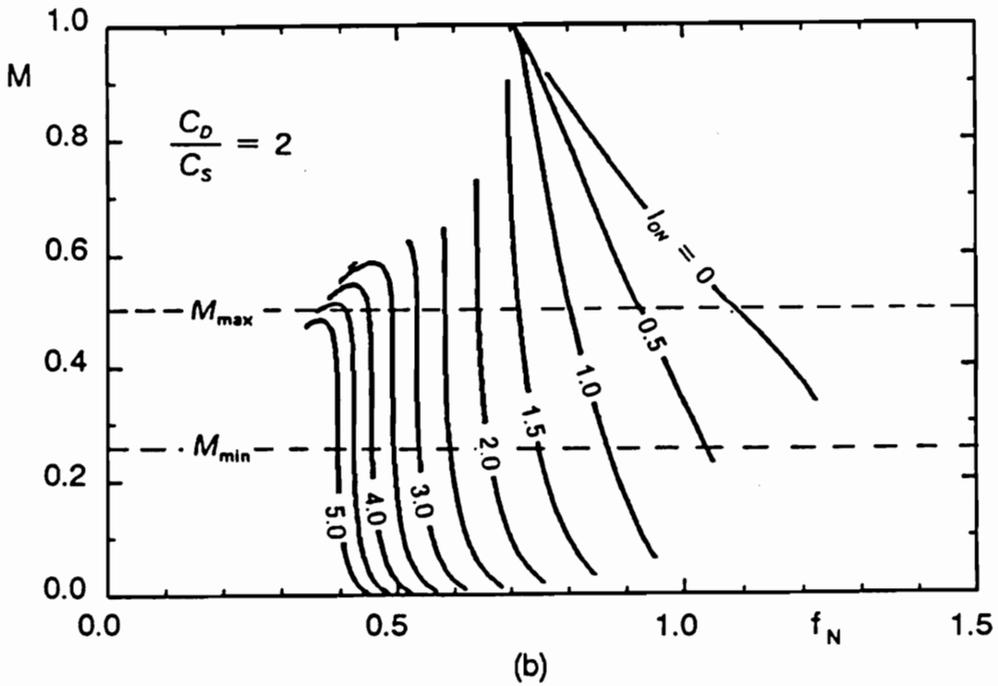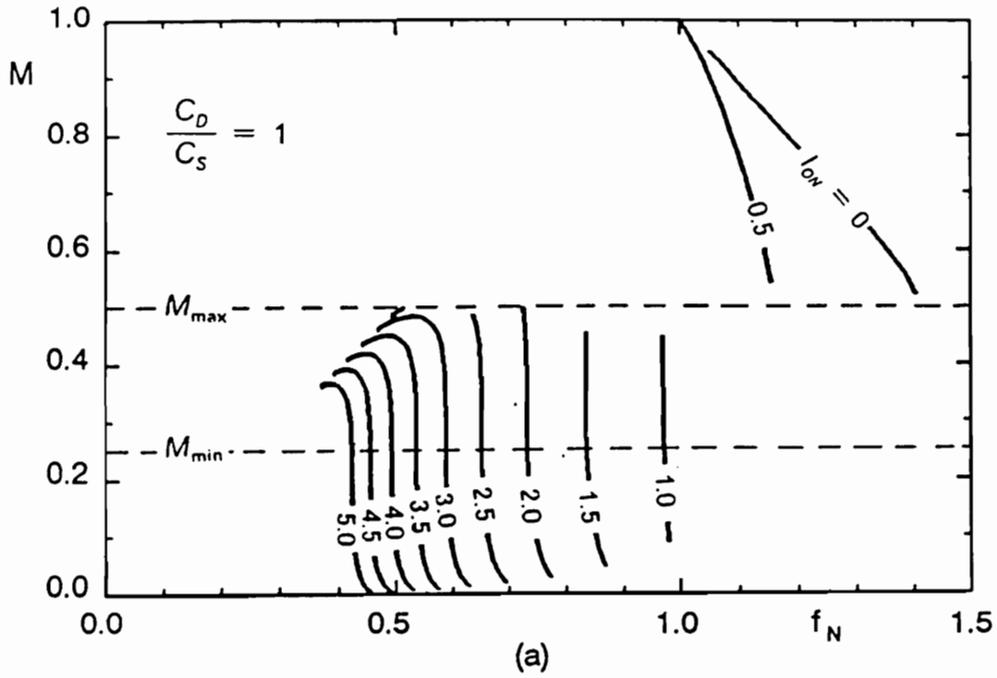
**Figure 4.1. Specified conversion-ratio range superimposed on conversion-ratio characteristics of buck ZVS-MRC: (a) $C_N$ = 1. (b) $C_N$ = 2.**
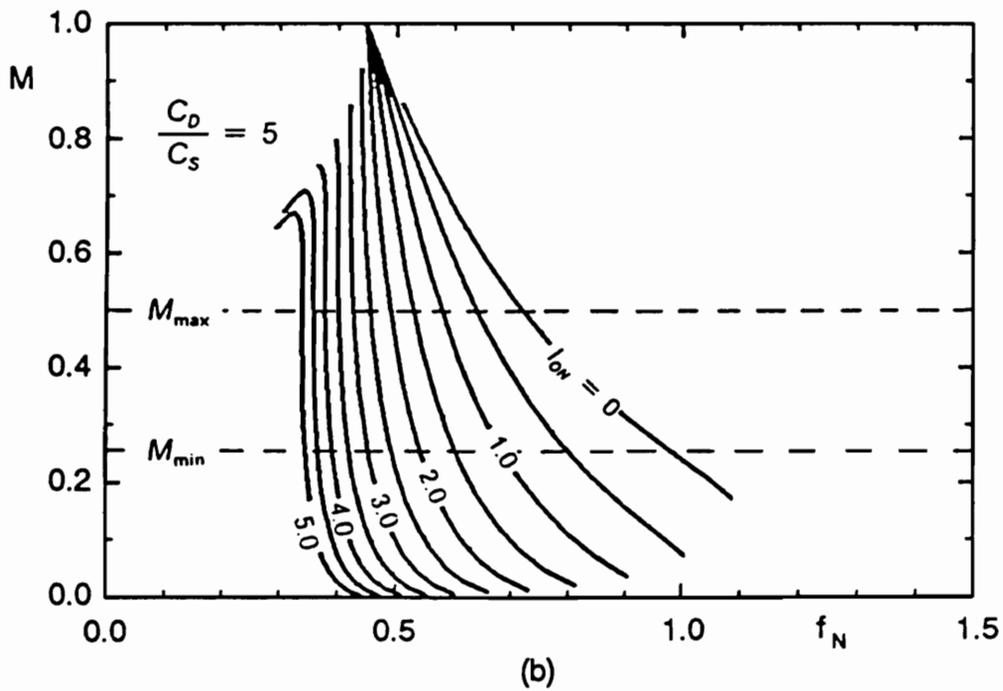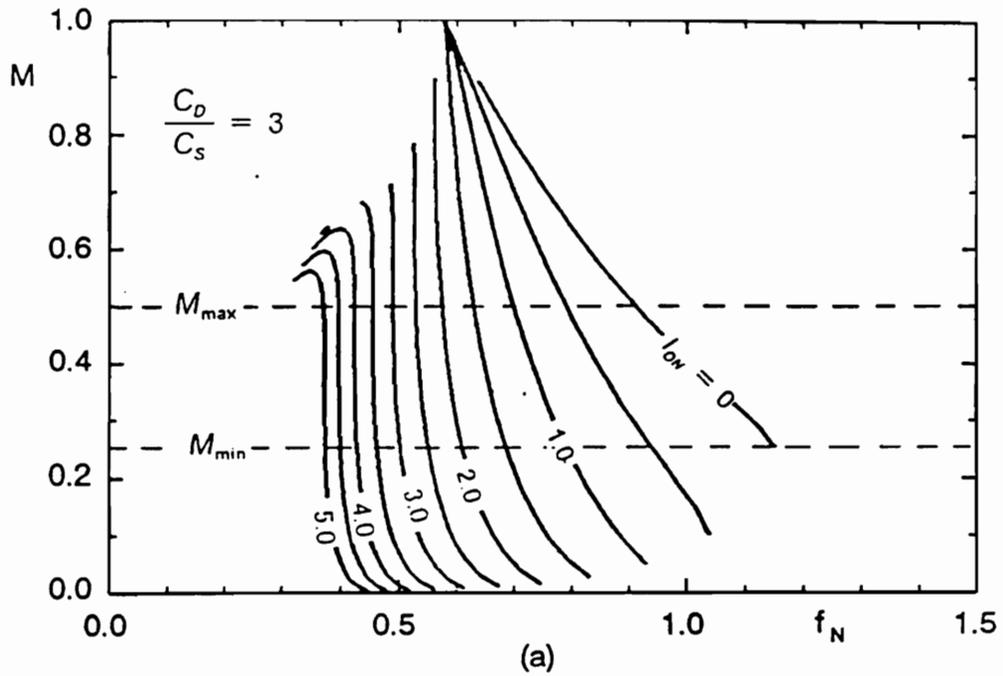
**Figure 4.2.** Specified conversion-ratio range superimposed on conversion-ratio characteristics of buck ZVS-MRC: **(a)** $C_N$ = 3. **(b)** $C_N$ = 5.

situations the maximum current stress occurs in the vicinity of the point corresponding to a full load and high line (FL-HL). For practical purposes, it can be assumed that the maximum transistor current stress occurs at full load and high line, and it is sufficient to calculate the stress for one point only.

The transistor voltage stress characteristics for $C_N = 3$ are shown in Fig. 4.4(b). In general, it is difficult to predict at exactly what condition the voltage stress will be maximum. Therefore, in general, it is necessary to examine the voltage stress characteristics for all operating conditions corresponding to full load. In many practical designs, however, the maximum voltage stress occurs at full load and high line.

The transistor current and voltage stresses for the four designs are summarized in Table 4.1. The following trade-offs can be observed:

- increased $C_N$ increases both the current and voltage stresses, and
- increased $I_{ONmax}$ (i.e., increased $Z_0$) reduces current stress but increases voltage stress.

Thus, a trade-off between the transistor current stress and voltage stress can be observed. Current stress can be reduced at the cost of increased voltage stress and *vice versa*. Therefore, for a given MOSFET, conversion efficiency can be improved by increaseing $Z_0$, which reduces current stress and increases voltage stress. This approach, however, is only effective if voltage stress does not exceed the specified MOSFET's voltage rating. Otherwise, a

**Table 4.1.** Comparison of transistor current and voltage stresses.

| | $\dfrac{C_D}{C_S} = 3$ | $\dfrac{C_D}{C_S} = 5$ | |
|---|---|---|---|
| $I_{ONmax} = 2$ | 13 A | 15 A | $I_{SMAX}$ |
| | 56 V | 64 V | $V_{SMAX}$ |
| $I_{ONmax} = 5$ | 8 A | 9 A | $I_{SMAX}$ |
| | 80 V | 90 V | $V_{SMAX}$ |
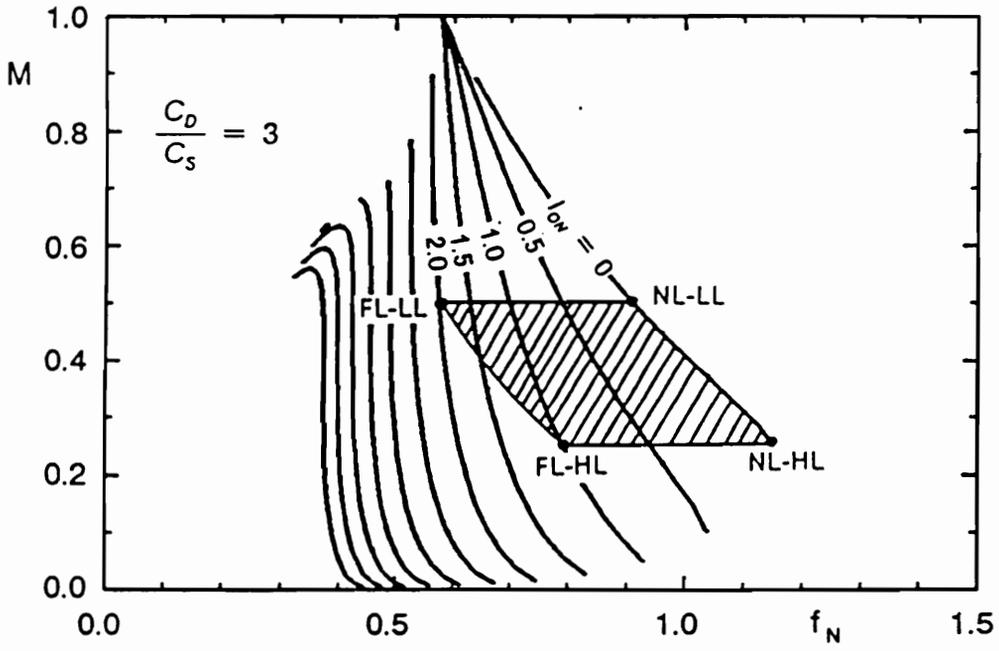
**Figure 4.3.  Conversion-ratio characteristics for Design 1.**
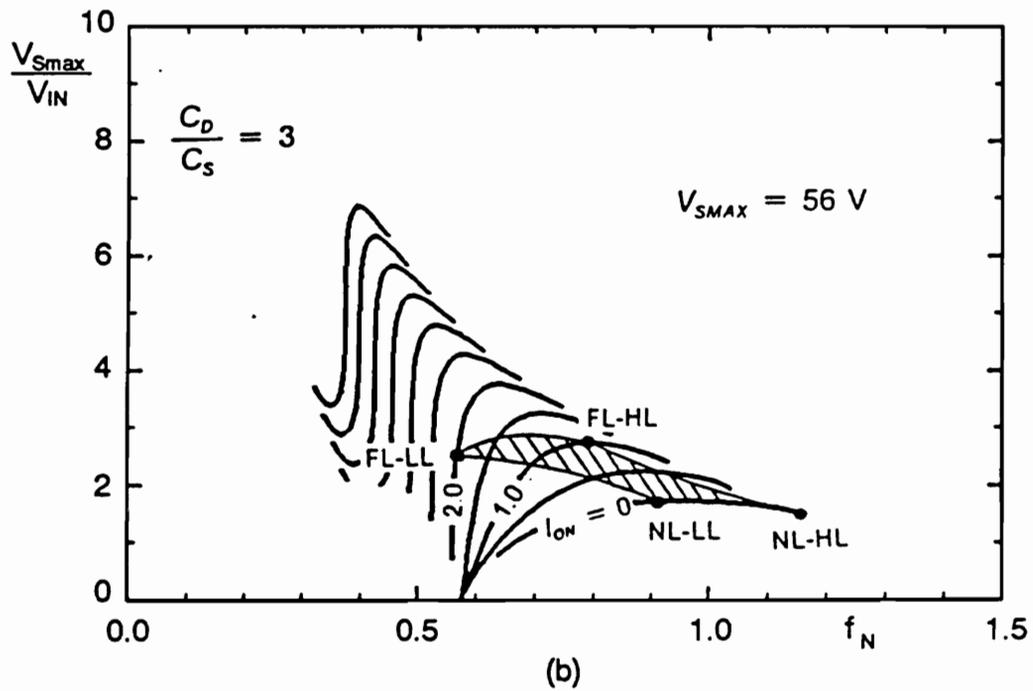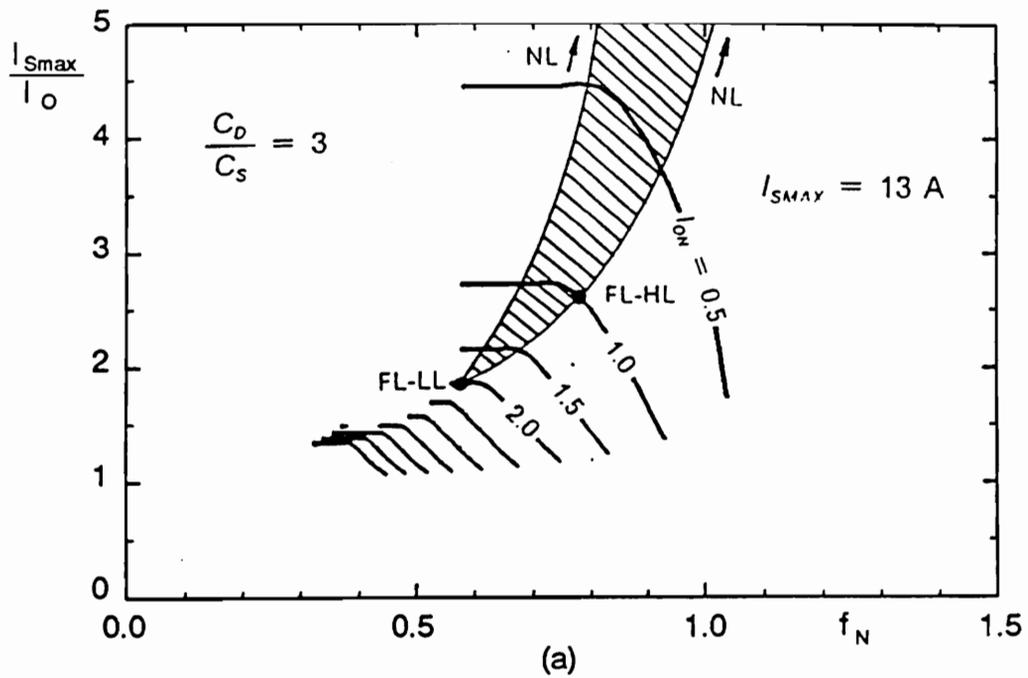
Figure 4.4. Stress characteristics for Design 1: (a) Normalized transistor current stress. (b) Normalized transistor voltage stress.
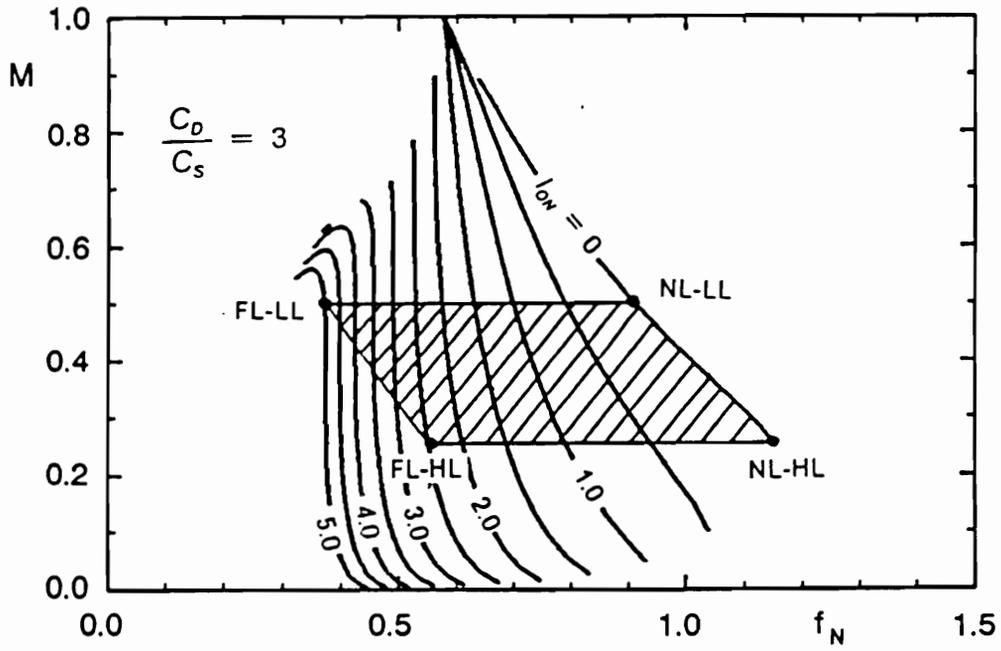
**Figure 4.5. Conversion-ratio characteristics for Design 2.**
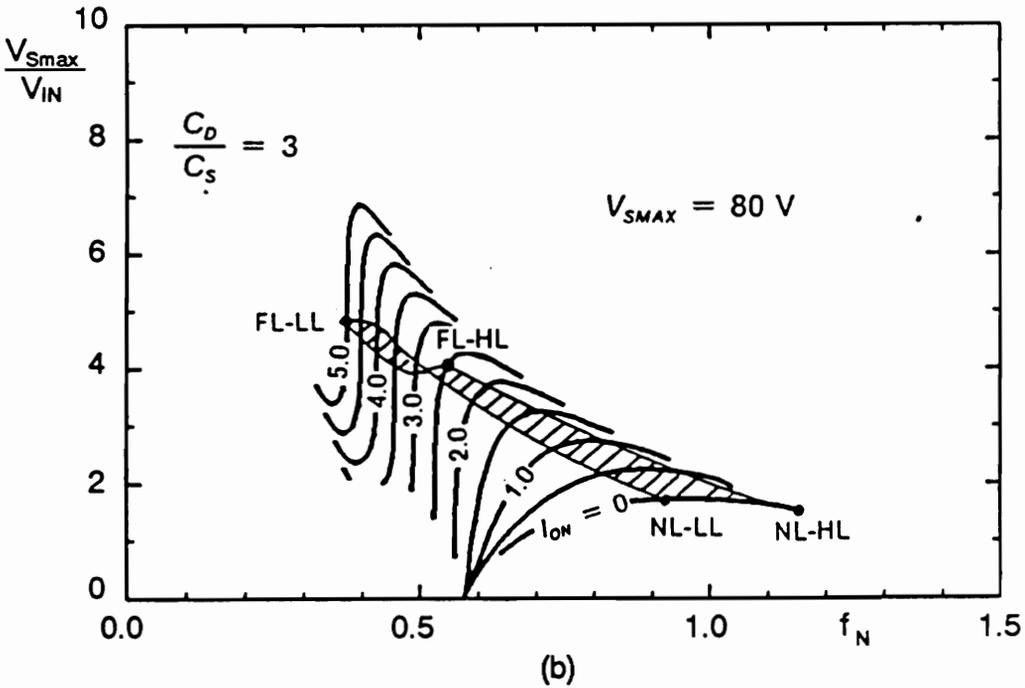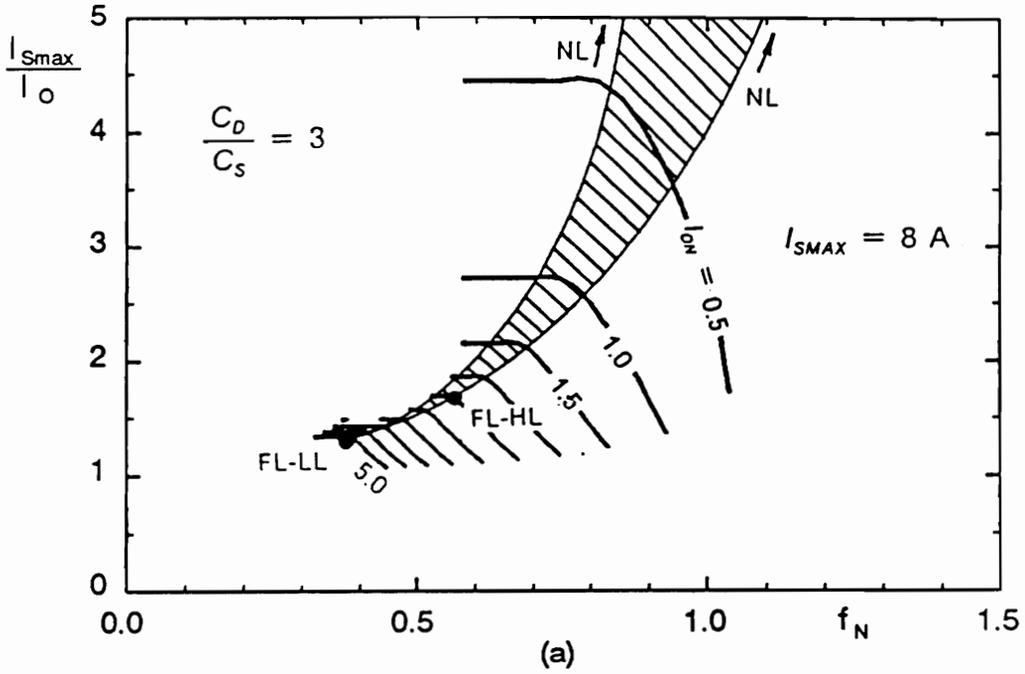
Figure 4.6. Stress characteristics for Design 2: (a) Normalized transistor current stress. (b) Normalized transistor voltage stress.
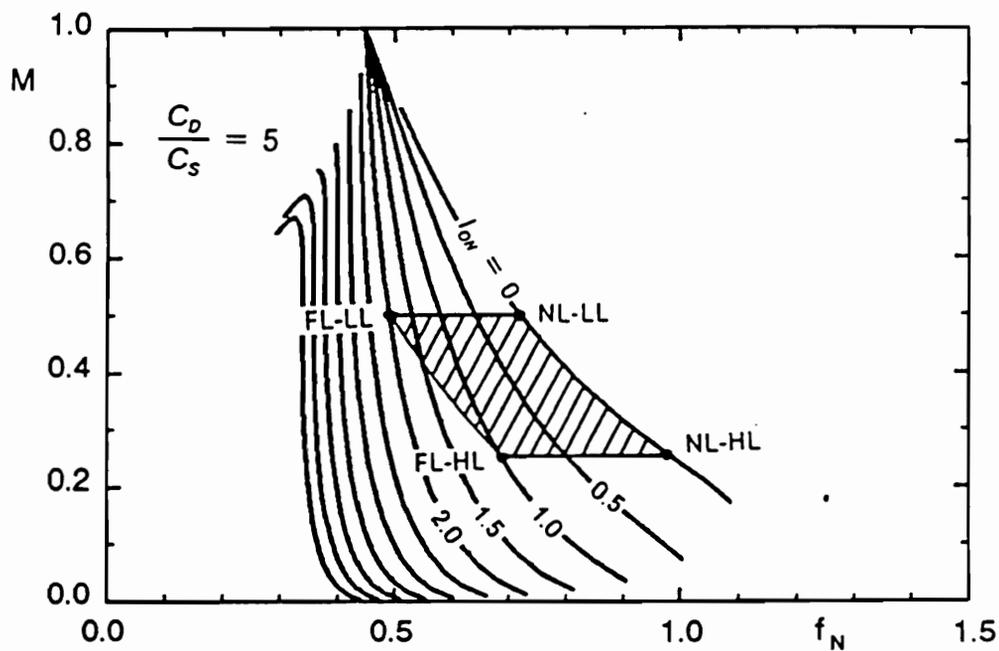
**Figure 4.7. Conversion-ratio characteristics for Design 3.**
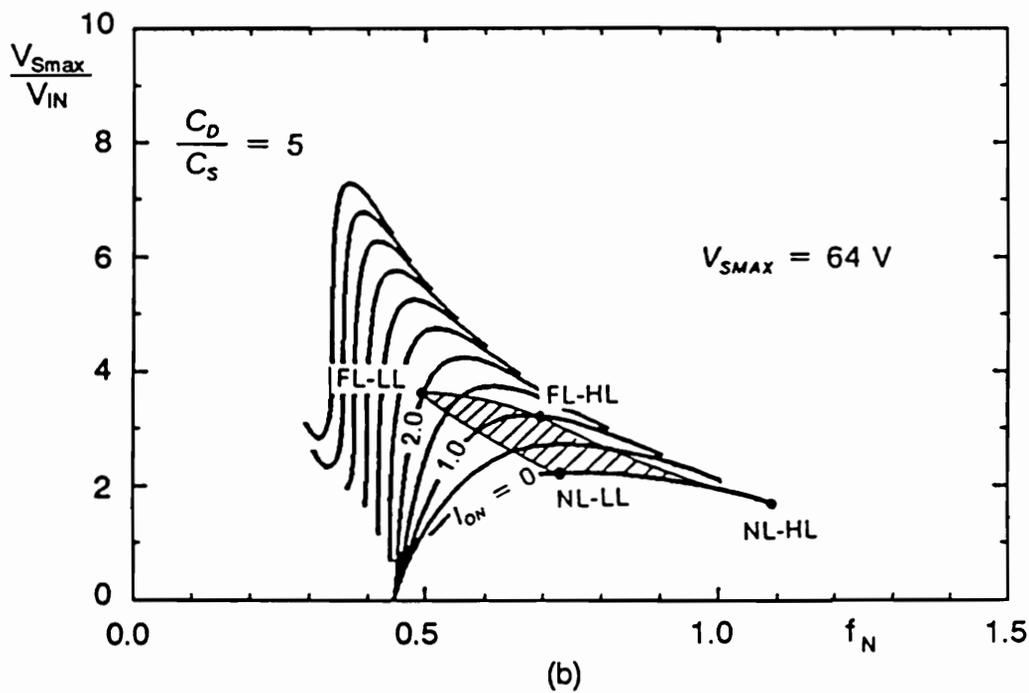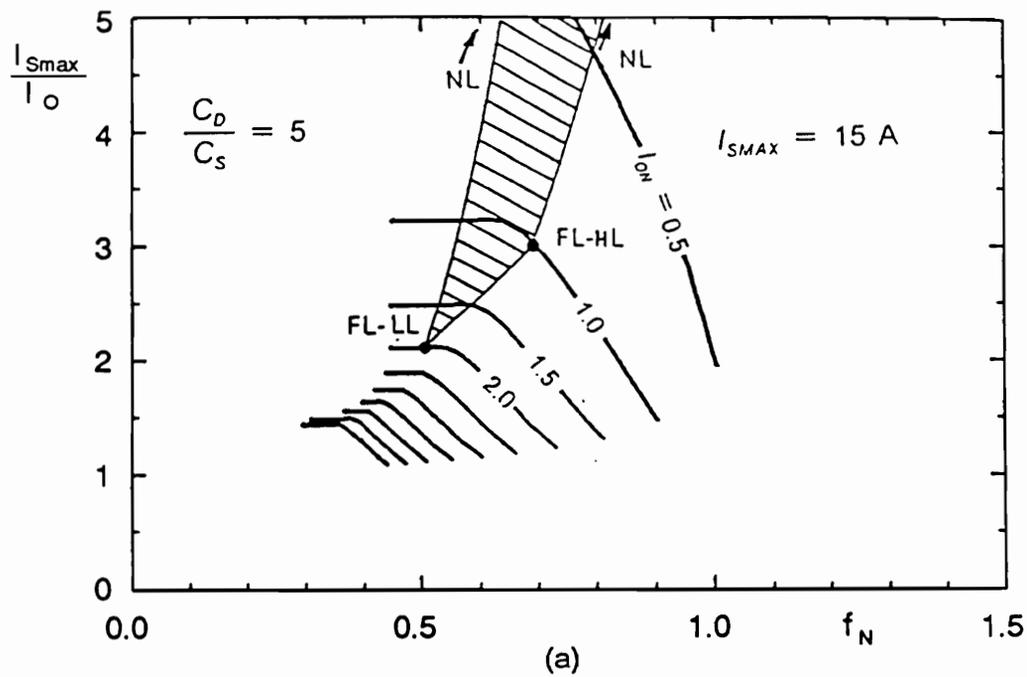
Figure 4.8. Stress characteristics for Design 3: (a) Normalized transistor current stress. (b) Normalized transistor voltage stress.
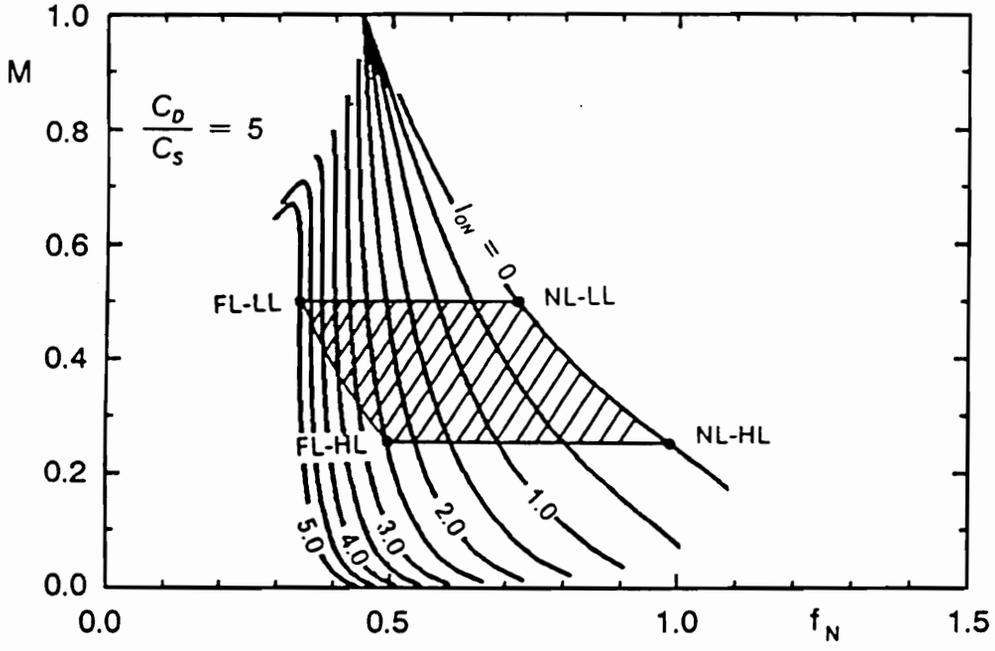
**Figure 4.9.   Conversion-ratio characteristics for Design 4.**
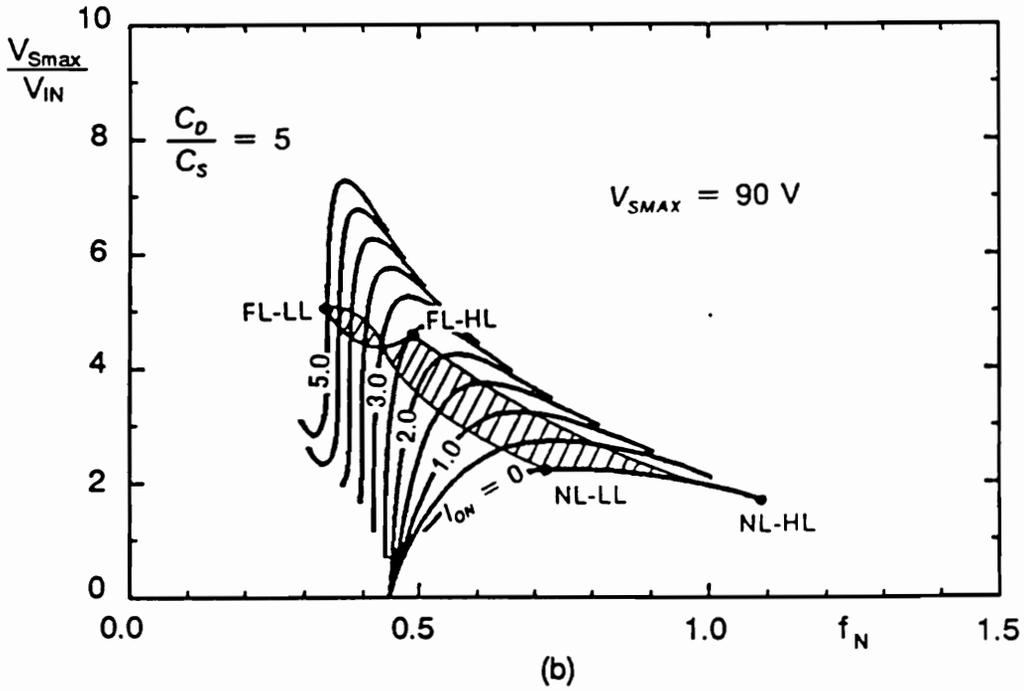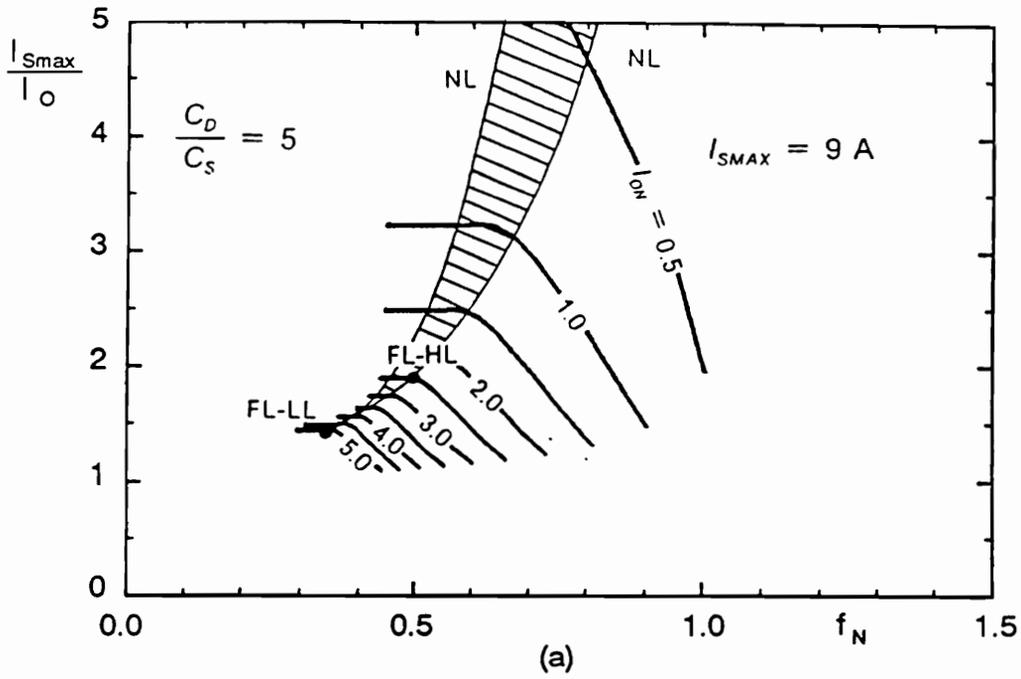
**Figure 4.10.** Stress characteristics for Design 4: (a) Normalized transistor current stress. (b) Normalized transistor voltage stress.

MOSFET with a higher voltage rating and higher on resistance must be used, resulting in an increase of conduction loss.

## 4.2. Device Stresses in ZVS-MRCs

The transistor voltage stress can be precisely determined using the dc characteristics obtained from the analysis presented in Chapter 3. However, other stresses are difficult to present in a form of a conveniently normalized graph. For design purposes, it is desirable to determine approximate expressions for the transistor current stress and diode current and voltage stress. This can be achieved by examination of the expressions derived in Chapter 3 for the resonant current and voltages. The derivation of the approximate device stresses is discussed in Appendix B.

### 4.2.1. Buck ZVS-MRC

**Transistor Current Stress**

$$I_{Smax} \leq I_{Lmax} \leq \frac{V_{INmax}}{Z_D} + I_{Omax} = V_{INmax} \frac{\sqrt{C_N}}{Z_0} + I_{Omax} \qquad (4.11)$$

**Rectifier Voltage Stress**

$$V_{Dmax} \leq 2V_{INmax} \qquad (4.12)$$

**Rectifier Current Stress**

$$I_{Dmax} \leq 2I_{Omax} + V_{INmax} \frac{\sqrt{C_N}}{Z_0} \qquad (4.13)$$

## 4.2.2. Boost ZVS-MRC

**Transistor Current Stress**

$$I_{Smax} \leq V_O \frac{\sqrt{C_N}}{Z_0} + I_{INmax} \qquad (4.14)$$

**Rectifier Voltage Stress**

$$V_{Dmax} \leq 2V_O \qquad (4.15)$$

**Rectifier Current Stress**

$$I_{Dmax} \leq 2I_{INmax} + V_O \frac{\sqrt{C_N}}{Z_0} \qquad (4.16)$$

### 4.2.3. Flyback, Cuk, ZETA, and SEPIC ZVS-MRCs

**Transistor Current Stress**

$$I_{Speak} \leq nV_O\left(1 + \frac{1}{M}\right)\frac{\sqrt{C_N}}{Z_0} + \frac{I_{Omax}}{n}(1 + M) \tag{4.17}$$

**Rectifier Voltage Stress**

$$V_{Dmax} = 2V_O\left(1 + \frac{1}{M_{min}}\right) \tag{4.18}$$

**Rectifier Current Stress**

$$I_{Dpeak} \leq 2I_{Omax}(1 + M) + n^2V_O\left(1 + \frac{1}{M}\right)\frac{\sqrt{C_N}}{Z_0} \tag{4.19}$$

To find a conservative estimate on the rectifier current stress, (4.19) should be evaluated for both $M_{min}$ and $M_{max}$, and a higher value of $I_{Dpeak}$ should be chosen as a maximum stress.

## 4.3. Design Procedures for ZVS-MRCs

A design procedure can be established for ZVS-MRCs based on the trade-offs described in the previous sections. Two rules should be followed while designing ZVS-MRCs:

1. Parameter $C_N$ should be minimized to reduce both current and voltage stress.

2. Characteristic impedance, $Z_0$, should be maximized to reduce the current stresses; the maximum value of $Z_0$ is limited by the maximum voltage stress allowed on the switching transistor.

### 4.3.1. Design Procedure for Basic Nonisolated Converters

The following design procedure is applicable to any of the six basic ZVS-MRCs. The input data consists of:

1. Minimum and maximum conversion ratios, $M_{min}$ and $M_{max}$,

2. minimum switching frequency, $f_{min}$, and

3. maximum transistor voltage stress.

It is assumed that the converter will operate from no load to full load.

The design procedure is as follows:

1. Using the dc conversion ratio characteristics, select a minimum value of $C_N$ such that the specified range of M is covered by the conversion-ratio characteristics for some high value of $R_N$ (e.g. $R_N = 50$). This will assure zero-voltage switching at light loads.

2. Using the dc conversion-ratio and transistor voltage stress characteristics for the selected $C_N$, choose a minimum value of the normalized load re-

sistance, $R_{Nmin}$, for which the corresponding conversion-ratio curve covers the specified range of M, and transistor voltage stress does not exceed the specified maximum voltage stress.

3. Calculate $Z_0 = R_{Lmin}/R_{Nmin}$.

4. From the dc conversion-ratio characteristics, find $f_{Nmin}$ corresponding to $M_{max}$ and $R_{Lmin}$. Calculate the resonant frequency:

$$f_0 = \frac{f_{min}}{f_{Nmin}} \tag{4.20}$$

5. Calculate the resonant components:

$$L = \frac{Z_0}{2\pi f_0} \quad , \tag{4.21}$$

$$C_S = \frac{1}{2\pi f_0 Z_0} \quad , \tag{4.22}$$

$$C_D = C_N C_S \quad . \tag{4.23}$$

6. Estimate the transistor and diode stresses using expressions (4.11)-(4.19).

### 4.3.2. Example Design of Buck ZVS-MRC

To illustrate the design procedure, a buck ZVS MRC is designed for the following specifications:

- $V_{IN} = 10 - 18$ V,

- $V_O = 5$ V,

- $I_O = 0 - 5$ A,

- $f_{min} = 450$ kHz, and

- $V_{Smax} = 75$ V (a 100 V MOSFET is assumed).

From the design specifications, $M_{min} = 0.27$, $M_{max} = 0.5$, and $R_{Lmin} = V_O/I_{Omax}$ $= 1\ \Omega$. The design follows steps 1-6 of the design procedure and is illustrated in Figs. 4.11 and 4.12.

1. Using Fig. 4.11, $C_N = 3$ is selected as optimum, since for $C_N = 2$ the conversion ratio characteristics at light loads do not cover M = 0.27.

2. Using Fig. 4.12, $R_{Nmin} = 0.1$ is selected as optimum, since it is approximately the smallest value of $R_N$ for which the corresponding conversion-ratio characteristic covers the specified conversion ratio range and does not cause excessive voltage stress (for $R_N = 0.1$, $V_{Smax} \simeq 4V_{INmax} = 72V$ at full load and high line).

3. $Z_0 = R_{Lmin}/R_{Nmin} = 1/0.1 = 10$

4. From Fig. 4.3, $f_{Nmin} = 0.375$, and $f_0 = 450$ kHz / 0.375 = 1.2 MHz.

5. From (4.21), $L = 1.33\ \mu$H, from (4.22), $C_S = 13.3$ nF, and from (4.23) $C_D = 3C_S = 39.8$ nH.

6. From (4.11), $I_{Smax} \leq 8.12$, from (4.12), $V_{Dmax} \leq 36$ V, and from (4.13), $I_{Dmax} \leq 13.11$.
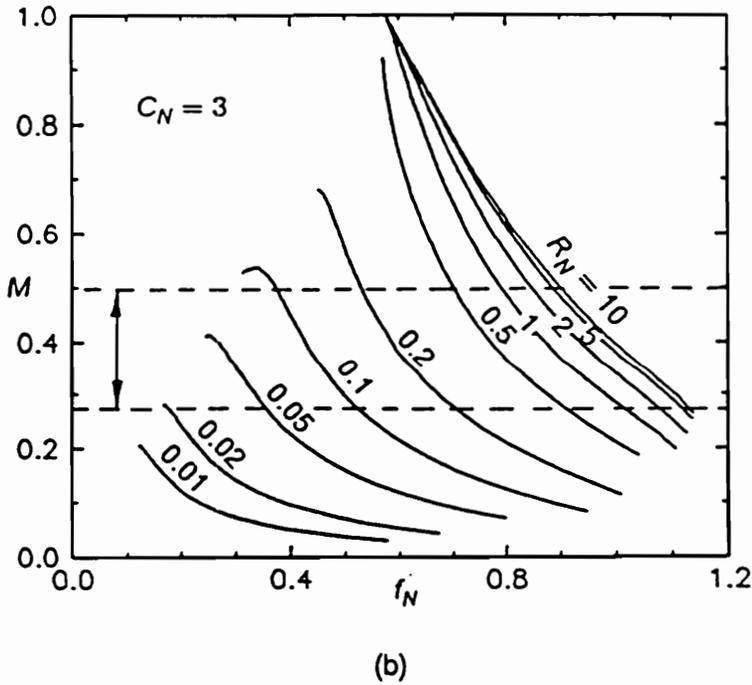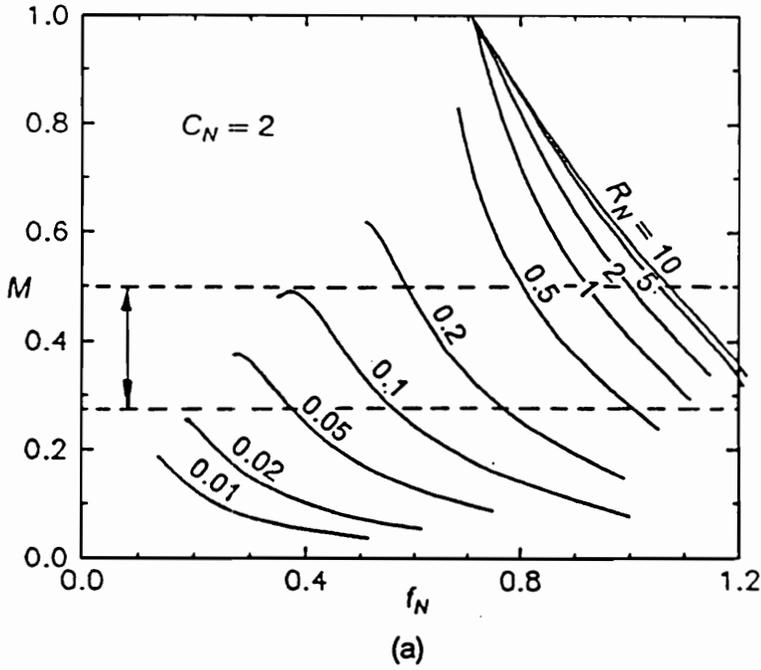
**Figure 4.11.** Selection of normalized capacitance ratio: (a) At $C_N = 2$, the conversion-ratio characteristics do not cover the required conversion range; such a design would result in non-zero switching at high line and light load. (b) At $C_N = 3$ the required conversion ratio range is covered by the characteristics.
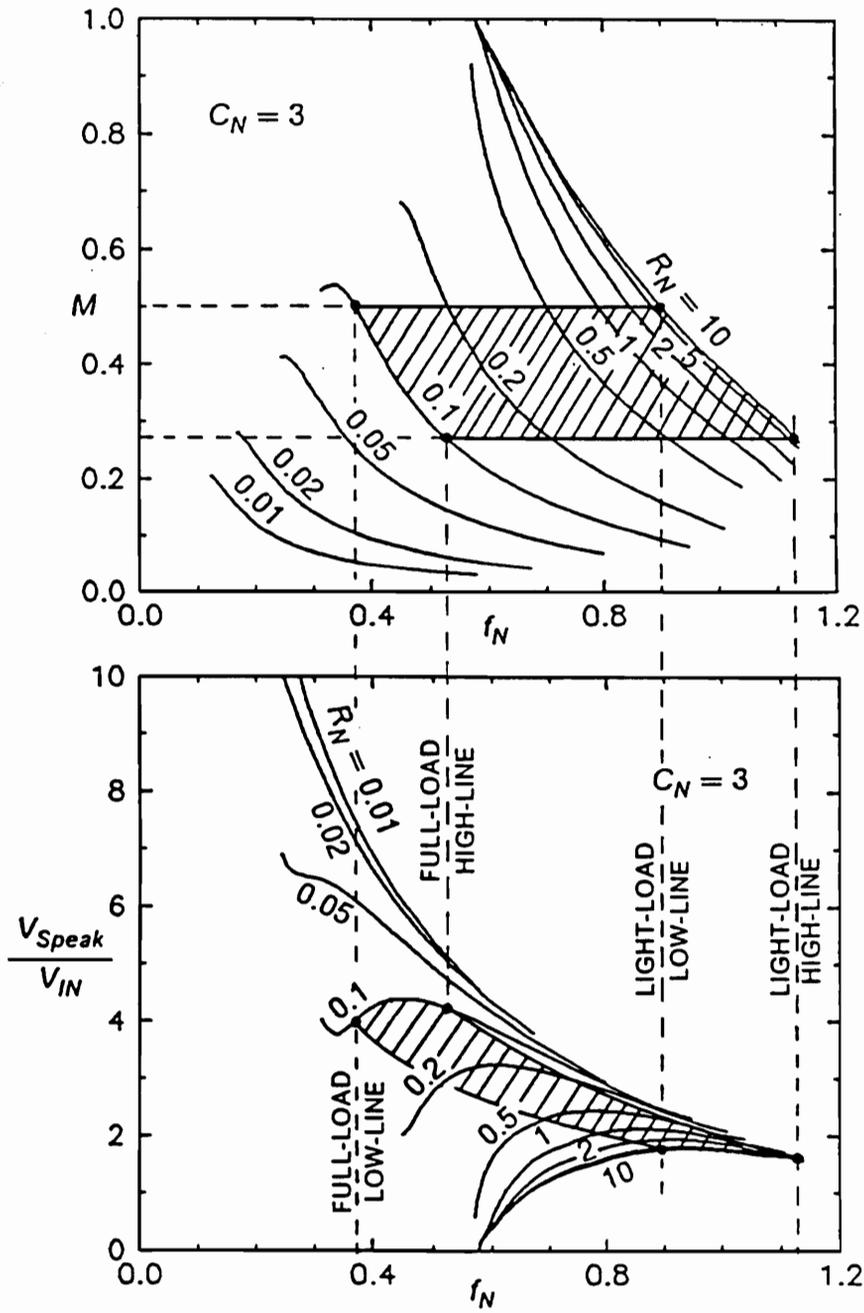
**Figure 4.12.** Conversion-ratio and transistor voltage stress operating ranges.

The above design corresponds to the experimental converter presented in Chapter 3. The measured conversion-ratio and transistor voltage stress characteristics are shown in Fig. 3.21. The experimental characteristics of Fig. 3.21 are in good agreement with the theoretical characteristics of Fig. 4.12. However, due to power dissipation in the practical circuit, the conversion-ratio is reduced at heavy loads. Therefore, in practical designs, conversion ratio should be specified with some extra margin to compensate for power dissipation. One way to do that is to specify the effective conversion-ratio as

$$M_{eff} = \frac{V_o}{\eta V_{IN}} \quad . \tag{4.24}$$

The above expression compensates the for the decrease in the conversion ratio by treating the losses as part of the load.

### 4.3.3. Design Procedure for Isolated Flyback ZVS-MRCs

As explained previously, design of up/down converters, such as the flyback ZVS-MRC, is complicated due to the parabolic dependance of the transistor voltage stress on the conversion-ratio and the additional degree of freedom (turns ratio) added to the system when an isolation transformer is used. A design procedure is presented here using the flyback converter example, but it is applicable to all four up/down converters, including the Cuk, Zeta, and SEPIC topologies. The presented design procedure explicitly uses the assumed full-load efficiency to improve precision of the design.

Design Specifications:

- minimum input voltage $V_{INmin}$,

- maximum input voltage $V_{INmax}$,

- full load efficiency $\eta_{FL}$,

- output voltage $V_O$,

- minimum switching frequency $f_{Smin}$, and

- full load output current $I_{Omax}$

It is assumed that the converter will operate from no load to full load. The transformer turns ratio must be optimized to achieve desirable trade-offs among the stresses of the semiconductor devices.

Several values of turns ratio must be considered in optimizing the design. One possible initial choice of primary-to-secondary turns ratio $n$ is

$$n_{ini} = \frac{\eta_{FL} V_{INmax}}{V_O} \quad . \tag{4.25}$$

Several $n$'s in the vicinity of $n_{ini}$ should be considered. For each $n$ considered, the following steps should be followed.

1.  Determine the maximum and minimum values of the conversion ratio:

$$M_{max} = \frac{n V_O}{\eta_{FL} V_{INmin}} \quad , \tag{4.26}$$

$$M_{min} = \frac{nV_O}{V_{INmax}} \qquad . \tag{4.27}$$

2. Using the dc characteristics, determine minimum values of both $C_N$ and $R_{Nmin}$ that can support the conversion-ratio range.

3. Calculate the characteristic impedance:

$$Z_0 = \frac{n^2 R_{Lmin}}{R_{Nmin}} \qquad . \tag{4.28}$$

4. Using the dc characteristics, determine MOSFET voltage stress.

5. Estimate transistor current stress using (4.17).

6. Estimate rectifier voltage stress using (4.18).

7. Estimate rectifier current stress using (4.19).


Based on the stress analysis, select an optimum value of n. By now, the following parameters should have been determined: $M_{min}$, $M_{max}$, $C_N$, and $R_{Nmin}$.

Using the dc conversion-ratio characteristics, determine $f_{Nmin}$ and calculate resonant frequency

$$f_0 = \frac{f_{Smin}}{f_{Nmin}} \qquad . \tag{4.29}$$

Calculate resonant components ($L_R$ and $C_S$ located on the primary and $C_D$ on the secondary side):

$$L = \frac{Z_0}{2\pi f_0} \quad , \tag{4.30}$$

$$C_S = \frac{1}{2\pi f_0 Z_0} \quad , \tag{4.31}$$

$$C_D = n^2 C_N C_S \quad . \tag{4.32}$$

## 4.3.4. Example Design of Flyback ZVS-MRC

**Design Specifications:**

- $V_{INmin} = 20$ V,

- $V_{INmax} = 30$ V,

- $\eta_{FL} = 0.75$,

- $V_O = 5$ V,

- $f_{Smin} = 1$ MHz,

- $I_{Omax} = 5$ A.

It is assumed that the converter will operate from no load to full load.

### Turns Ratio Selection

Initial choice of turns ratio:

$$n = \frac{\eta_{FL} V_{INmax}}{V_O} \simeq 4$$

Turns ratio values of 2, 3, 4, and 5 will be considered. Since the procedure is identical for each $n$, only the case $n = 3$ is presented with all details. Table 4.2 shows values of the conversion ratio for low and high line, calculated using (4.17) and (4.18) for each value of $n$.

For $n = 3$ ($C_N = 2$), the dc characteristics are shown in Fig. 4.4. In this case the characteristic impedance is

$$Z_0 = \frac{n^2 R_{Lmin}}{R_{Nmin}} = 45$$

From Fig. 4.13, transistor voltage stress at full load and high line is:

$$V_{Speak(HL - FL)} = 3.5(nV_O + V_{INmax}) = 3.5(3 \times 5 + 30) = 158V \quad ,$$

while at low line and full load it is:

$$V_{Speak(LL - FL)} = 3.6(nV_O + V_{INmax}) = 3.6(3 \times 5 + 20) = 126V \quad .$$

Although it is possible that the maximum voltage stress occurs at some $V_{IN}$ between high and low line, for practical purposes it is sufficient to assume that the maximum transistor voltage stress is $V_{Smax} \simeq 158$ V.

Transistor current stress at high line and full load is:

$$I_{Speak(HL - FL)} \simeq 3 \times 5\left(1 + \frac{1}{0.5}\right)\frac{\sqrt{2}}{45} + \frac{5}{3}(1 + 0.5) = 3.9A \quad ,$$

while at low line and full load, it is:

**Table 4.2.  Design parameters for different values of turns ratio.**

| n | $M_{min}$ | $M_{max}$ | $C_N$ | $R_{Nmin}$ |
|---|---|---|---|---|
| 2 | 0.33 | 0.67 | 3.0 | 0.1 |
| 3 | 0.50 | 1.00 | 2.0 | 0.2 |
| 4 | 0.67 | 1.33 | 1.5 | 0.5 |
| 5 | 0.83 | 1.67 | 1.5 | 0.8 |
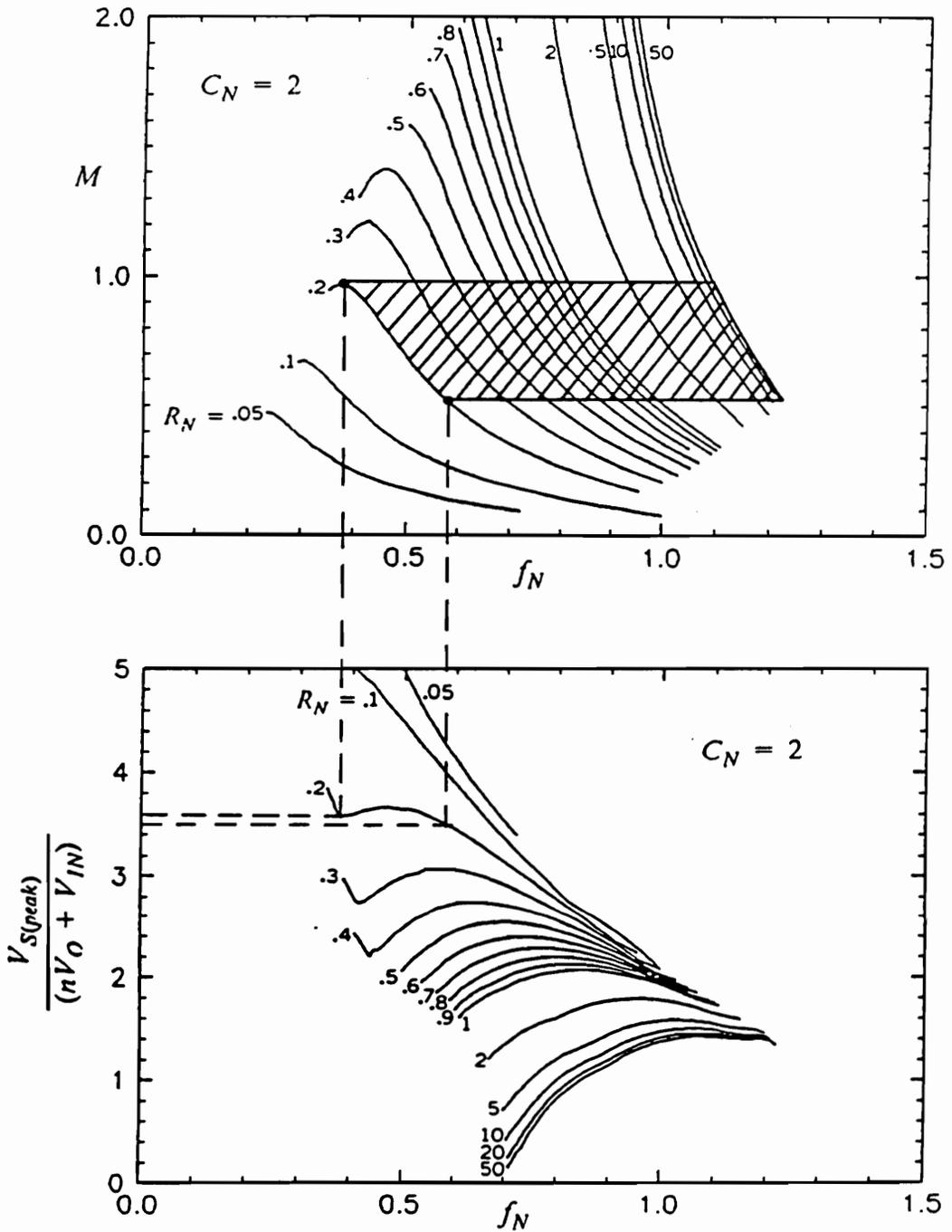
**Figure 4.13.** Operating range of a flyback converter at n = 3.

$$I_{Speak(LL-FL)} \simeq 3 \times 5(1+1)\frac{\sqrt{2}}{45} + \frac{5}{3}(1+1) = 4.28A \quad .$$

Therefore, the maximum current stress occurs at low line and full load $I_{Smax}$ = 4.28 A.

Rectifier voltage stress is:

$$V_{Dmax} \leq 2 \times 5\left(1 + \frac{1}{0.5}\right) = 30V \quad .$$

Rectifier current stress at high line and full load is:

$$I_{Rpeak(HL-LL)} \leq 2 \times 5(1+0.5) + 3^2 \times 5\left(1 + \frac{1}{0.5}\right)\frac{\sqrt{2}}{45} = 19.2A \quad ,$$

while at low line and full load it is:

$$I_{Rpeak(LL-LL)} \leq 2 \times 5(1+1) + 3^2 \times 5(1+1)\frac{\sqrt{2}}{45} = 22.8A \quad .$$

Therefore, maximum rectifier current stress occurs at low line and full load, and $I_{Dmax} \leq 22.8A$.

Table 4.3 gives a comparison of stresses for different turns ratio values. Turns ratio n = 3 is selected as optimum for a 200 V MOSFET.

From Fig. 4.13,

$$f_{Nmin} = 0.39 \quad ,$$

and

**Table 4.3.  Stress comparison for different values of turns ratio**

| n | $C_N$ | $R_{Nmin}$ | $V_{DSmax}$ | $I_{Dmax}$ | $V_{Rmax}$ | $I_{Rmax}$ |
|---|---|---|---|---|---|---|
| - | - | - | [V] | [A] | [V] | [A] |
| 2 | 3.0 | 0.1 | 192 | 5.3 | 40 | 18.8 |
| 3 | 2.0 | 0.2 | 158 | 4.3 | 30 | 22.8 |
| 4 | 1.5 | 0.5 | 115 | 4.3 | 25 | 28.7 |
| 5 | 1.5 | 0.8 | 110 | 4.3 | 22 | 34.6 |

$$f_0 = \frac{10^6}{0.39} = 2.56 MHz \quad .$$

The values of resonant components are calculated using (4.21)-(4.23):

$$L = \frac{45}{2\pi 2.56 \times 10^6} = 2.8 \mu H \quad ,$$

$$C_S = \frac{1}{2\pi 45 \times 2.56 \times 10^6} = 1.38 nF \quad ,$$

$$C_D = 3^2 \times 2 \times 1.38 \times 10^{-9} = 24.9 nF \quad .$$

## 4.3.5. Experimental Flyback ZVS-MRC

To verify the design procedure for the flyback converter, an experimental flyback converter was built using the design specifications and component values given in the previous section. Figure 4.14 shows a circuit diagram of the experimental converter.

Figure 4.15 shows primary-side waveforms at full load. Waveforms at 20% of full load are shown in Fig. 4.16. Rectifier voltage at high and low line is shown in Fig. 4.17 for full load current. Table 4.4 gives a comparison of the predicted and measured device stresses. It can be noted that the transistor current and voltage stresses have been predicted very precisely. However, the estimates for diode current and voltage stresses are very conservative.
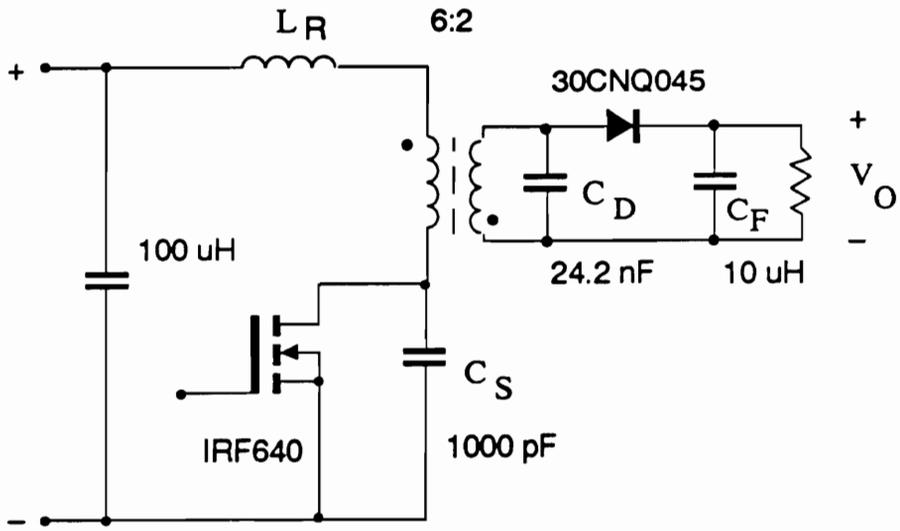
**Figure 4.14.    Experimental flyback converter.**
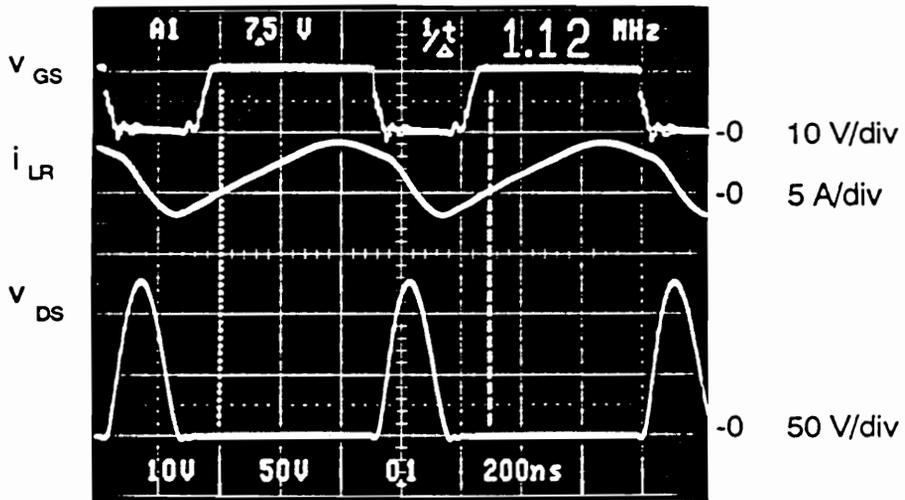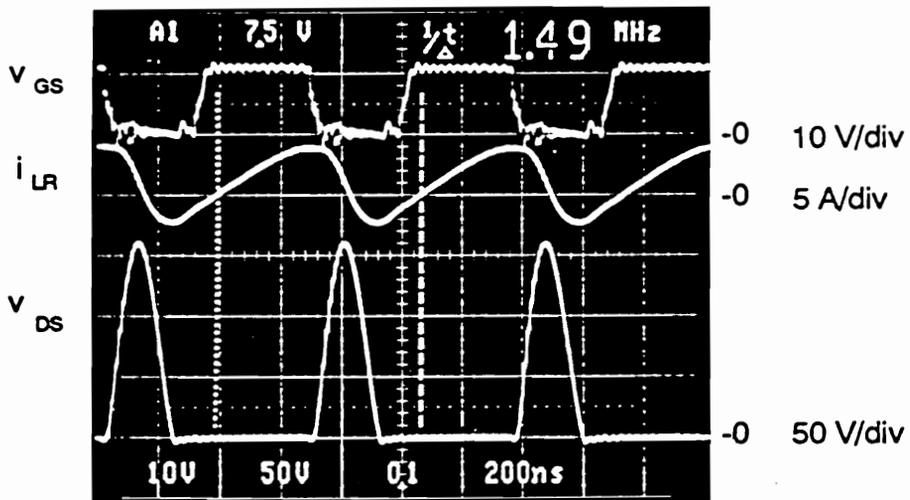
**Figure 4.15.** Waveforms of a flyback ZVS-MRC at full load of 5 A: (a) $V_{IN} = 20$. (b) $V_{IN} = 30$ V.

$V_{GS}$

$i_{LR}$

$V_{DS}$

-0    10 V/div

-0    5 A/div

-0    50 V/div

(a)



$V_{GS}$

$i_{LR}$

$V_{DS}$

-0    10 V/div

-0    5 A/div

-0    50 V/div
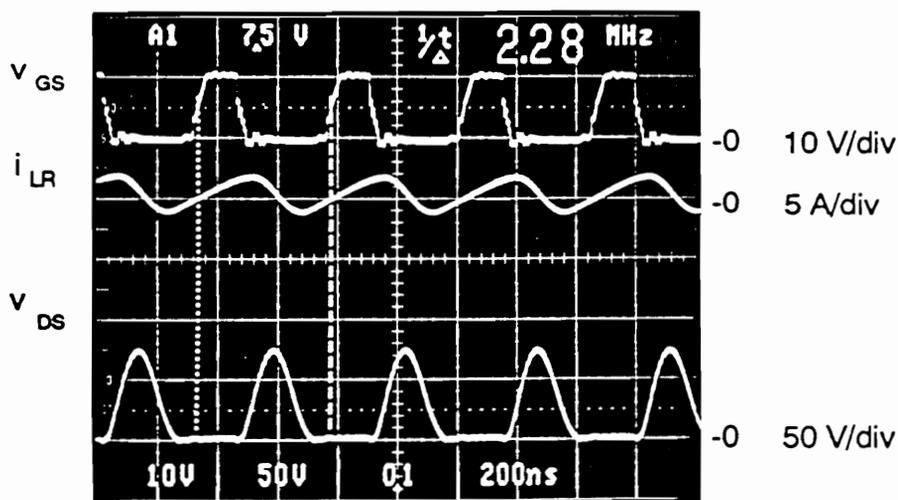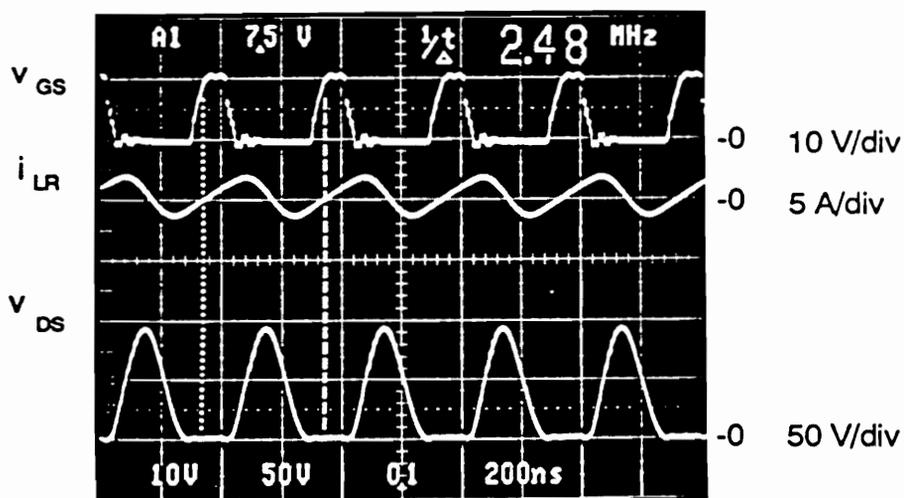
(b)

**Figure 4.16.    Waveforms of a flyback ZVS-MRC at light load of 1 A:    (a) $V_{IN} = 20$. (b) $V_{IN} = 30$ V.**

$v_D$    -0    10 V/div

(a)



$v_D$    -0    10 V/div
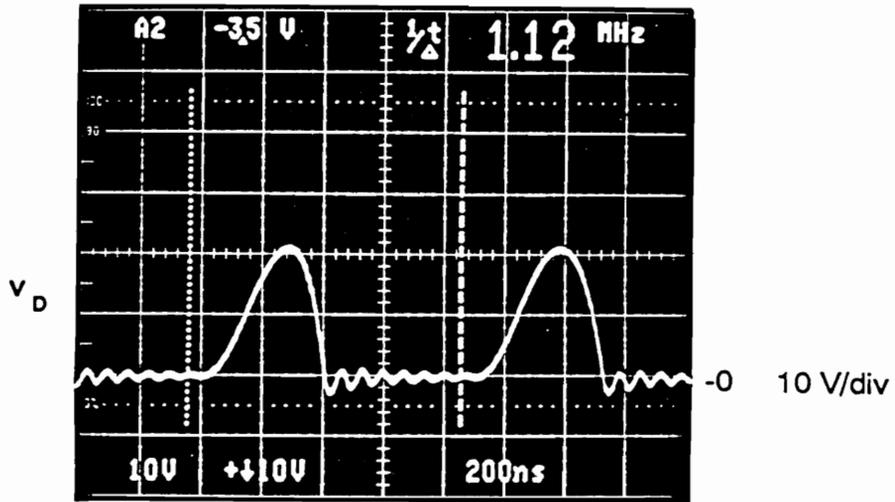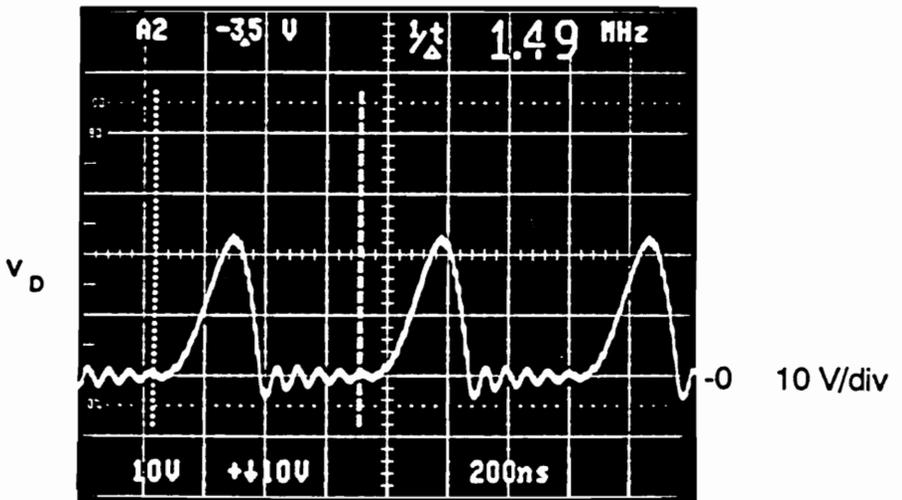
(b)

Figure 4.17.   Rectifier voltage in a flyback ZVS-MRC at full load of 5 A:   (a) $V_{IN} = 20$. (b) $V_{IN} = 30$ V.

**Table 4.4. Comparison of predicted and measured stresses in flyback ZVS-MRC**

| Stress | Predicted | Measured |
|---|---|---|
| $V_{Smax}$ [V] | 158 | 160 |
| $I_{Smax}$ [A] | 4.28 | 4.25 |
| $V_{Dmax}$ [V] | 30 | 23 |
| $I_{Dmax}$ [A] | 22.8 | 14 |

## 4.4. Summary

A stress analysis has been used to determine design guidelines for ZVS-MRCs. The two major rules for optimum design of the resonant network in ZVS-MRCs require that $C_N$ be minimized, and $Z_0$ be maximized. The maximum value of $Z_0$ is limited by the acceptable transistor voltage stress.

Design procedures are presented for basic nonisolated converters (buck and boost) and up/down converters with or without isolation transformers. Example designs are presented for buck and flyback converters, and experimental circuits are built to verify the design procedures. The experiments show that the design procedures are reasonably accurate and practical. The only significant discrepancy is due to rather conservative (approximately +30%) estimates of the rectifier current and voltage stresses.

# 5. FORWARD ZVS-MRC

The PWM forward topology has been used successfully in many applications, mostly in the 50-200 W range. Due to its single-ended operation, the forward converter is simple, requires only one nonisolated gate drive, and as a result, is very cost effective. The forward ZVS-MRC is one of the most attractive converters in the family of the multi-resonant converters. Its operation, analysis, and characteristics are somewhat different from those of the buck ZVS-MRC. This is due to the interactions of the magnetizing inductance of the power transformer with the resonant circuit. This chapter introduces the forward ZVS-MRC topology and describes its operating principles.

## 5.1. Topological Variations

The forward ZVS-MRC is derived from the buck ZVS-MRC; in a similar way the PWM forward converter is derived from the PWM buck converter. Figure 5.1 shows a basic forward ZVS-MRC topology arising when a transformer and a forward diode $D_1$ are added to the buck topology.

The forward ZVS-MRC topology has the capability of incorporating all essential parasitic reactances associated with the components of the power circuit. The output capacitance of the power MOSFET supplies part or all of the primary resonant capacitance. Since the resonant-inductor current flows through the transformer and the secondary resonant capacitor, both the primary and secondary leakage inductances of the transformer are included in the resonant tank.

For high-frequency operation, it is desirable to operate the rectifier in such a manner that the junction capacitances of the diodes are used in the resonant circuit. In the forward ZVS-MRC, the junction capacitances of the diodes can be absorbed by the secondary resonant capacitance. When the secondary voltage is positive, the forward diode is conducting, and the secondary resonant capacitance is in parallel with the reverse-biased freewheeling diode. Similarly, when the secondary voltage is negative, the freewheeling diode is conducting, and the resonant capacitance is in parallel with the reverse-biased forward diode. Therefore, the junction capacitances of the diodes are incorporated in the resonant circuit.
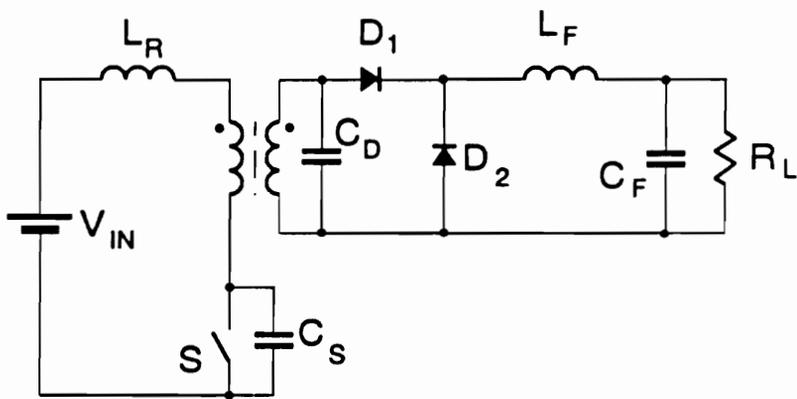
**Figure 5.1.** Basic circuit diagram of the forward ZVS-MRC.
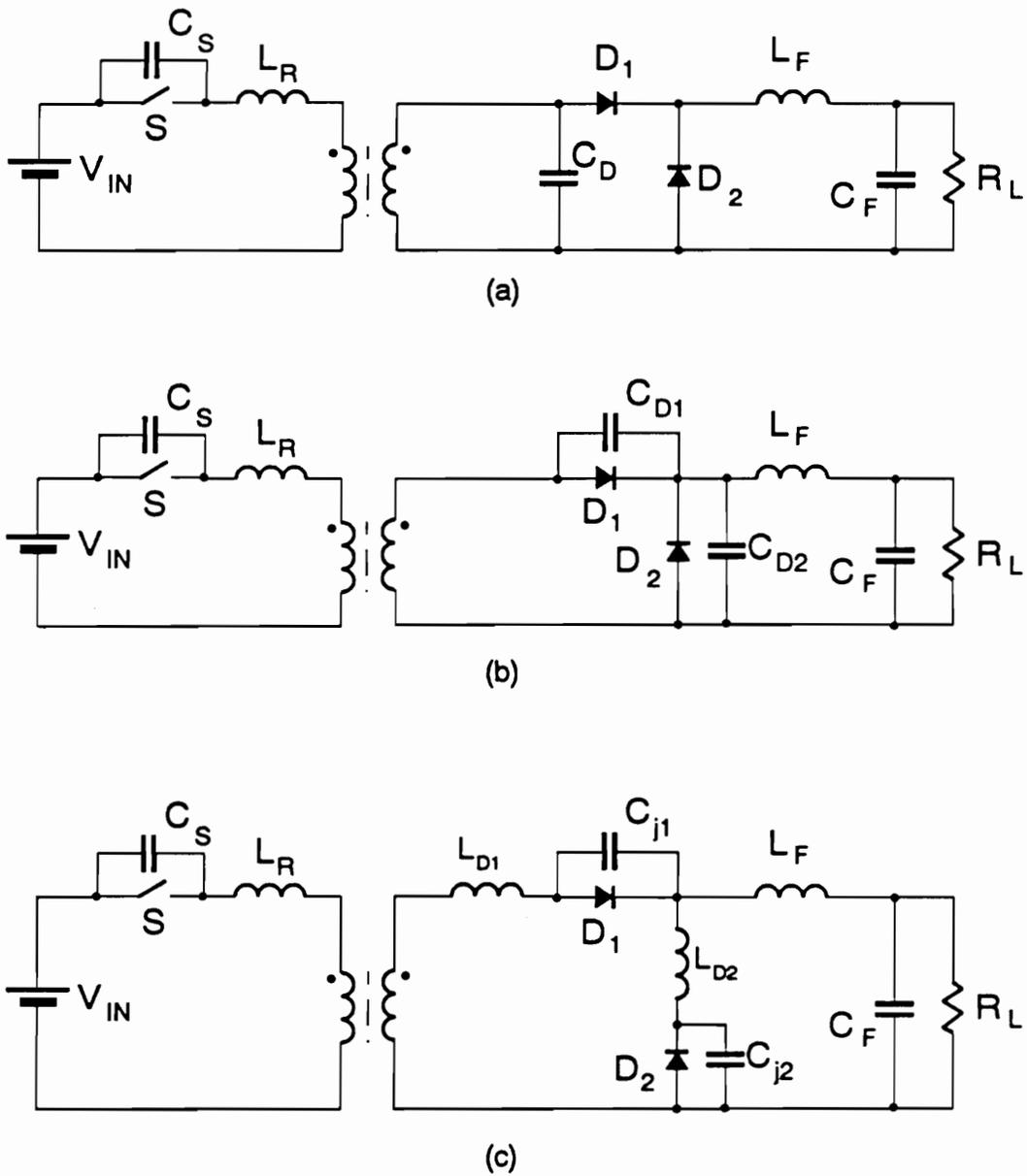
Figure 5.2. **Topological variations of the forward ZVS-MRC: (a) Secondary-side resonant capacitance allows utilization of the leakage inductance of the transformer. (b) Secondary-side capacitance can be placed directly across the rectifiers. (c) If the junction capacitances of the rectifiers are used solely for the resonant capacitance, the package and wiring inductances of the rectifiers can also be absorbed by $L_R$.**

Topological variations of the forward ZVS-MRC are shown in Fig. 5.2. In the basic configuration shown in Fig. 5.2(a), capacitor $C_D$ is placed across the secondary winding of the power transformer. The operation of the circuit does not change if the resonant capacitance is provided exclusively by capacitances in parallel with the diodes, as shown in Fig. 5.2(b). If the junction capacitances of the rectifiers are sufficiently large, they can provide all of the secondary resonant capacitance. In such a case, the package and wiring inductances of the rectifiers can be entirely absorbed by the resonant inductance, as shown in Fig. 5.2(c). Resonant capacitance $C_D$ could be placed on the primary side of the transformer. However, in such an arrangement the leakage inductance and junction capacitances of diodes $D_1$ and $D_2$ cannot be utilized in the resonant circuit.

## 5.2. Converter Operation

Figure 5.3 shows a simplified circuit diagram of the forward ZVS-MRC and typical operating waveforms. The output filter and load are modeled with a constant current source. A bidirectional active switch is assumed (e.g. power MOSFET with its antiparallel diode). Operation of the forward ZVS-MRC is different from that of a buck ZVS-MRC. Due to the presence of the forward diode, $D_1$, voltage across the secondary-side resonant capacitance $C_D$ can be positive or negative, thus providing an automatic transformer reset mech-
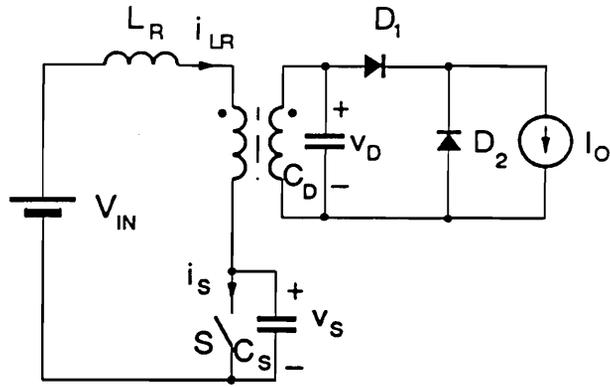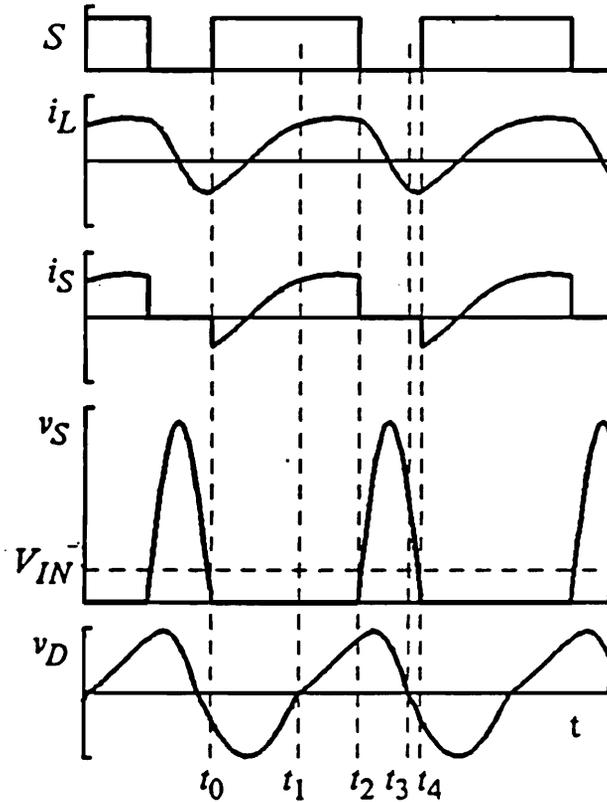
Figure 5.3. Operation of the forward ZVS-MRC: (a) Simplified circuit diagram. (b) Operating waveforms.

anism similar to that of the secondary-side-resonant forward ZCS-QRC [D32]. The volt-second product across $C_D$ is equal to the volt-second product applied to the transformer. If the net volt-second product applied to the transformer is positive during one cycle, it will cause the magnetizing current to increase. The increase of the magnetizing current will cause $C_D$ to be charged more negatively during next cycle, which will subsequently decrease the magnetizing current. This automatic reset mechanism eliminates the need for an external resetting circuit.

There are five topological stages, shown in Fig. 5.4, that can be formed by the circuit. A typical topological sequence corresponding to the waveforms of Fig. 5.3 is described below.

**Topological Stage A** $[t_0 - t_1]$. The active switch is turned on at $t_0$, with $v_S$ = 0 and $v_D < 0$. Resonance of inductor $L_R$ and capacitance $C_D$ causes $i_{LR}$ to increase. The combined currents of the resonant inductor and the magnetizing inductance charge $v_D$ to zero, causing $D_1$ to turn on and $D_2$ to turn off.

**Topological Stage B** $[t_1 - t_2]$. During this stage, conduction of switch S continues. The resonant circuit is still formed by $L_R$ and $C_D$, but the rate at which $v_D$ increases is reduced because part of the resonant current is flowing through the load. This stage ends when S is turned off at $t_2$.

**Topological Stage C** $[t_2 - t_3]$. After S is turned off, the resonant circuit is formed by all three resonant components. During this stage, $v_S$ reaches its peak value. Secondary voltage reduces to zero, turning $D_1$ off and $D_2$ on.

**Topological Stage D** $[t_3 - t_4]$. During this stage, voltage across the switch is reduced to zero. The cycle is completed when the switch is turned on at $t_4$.
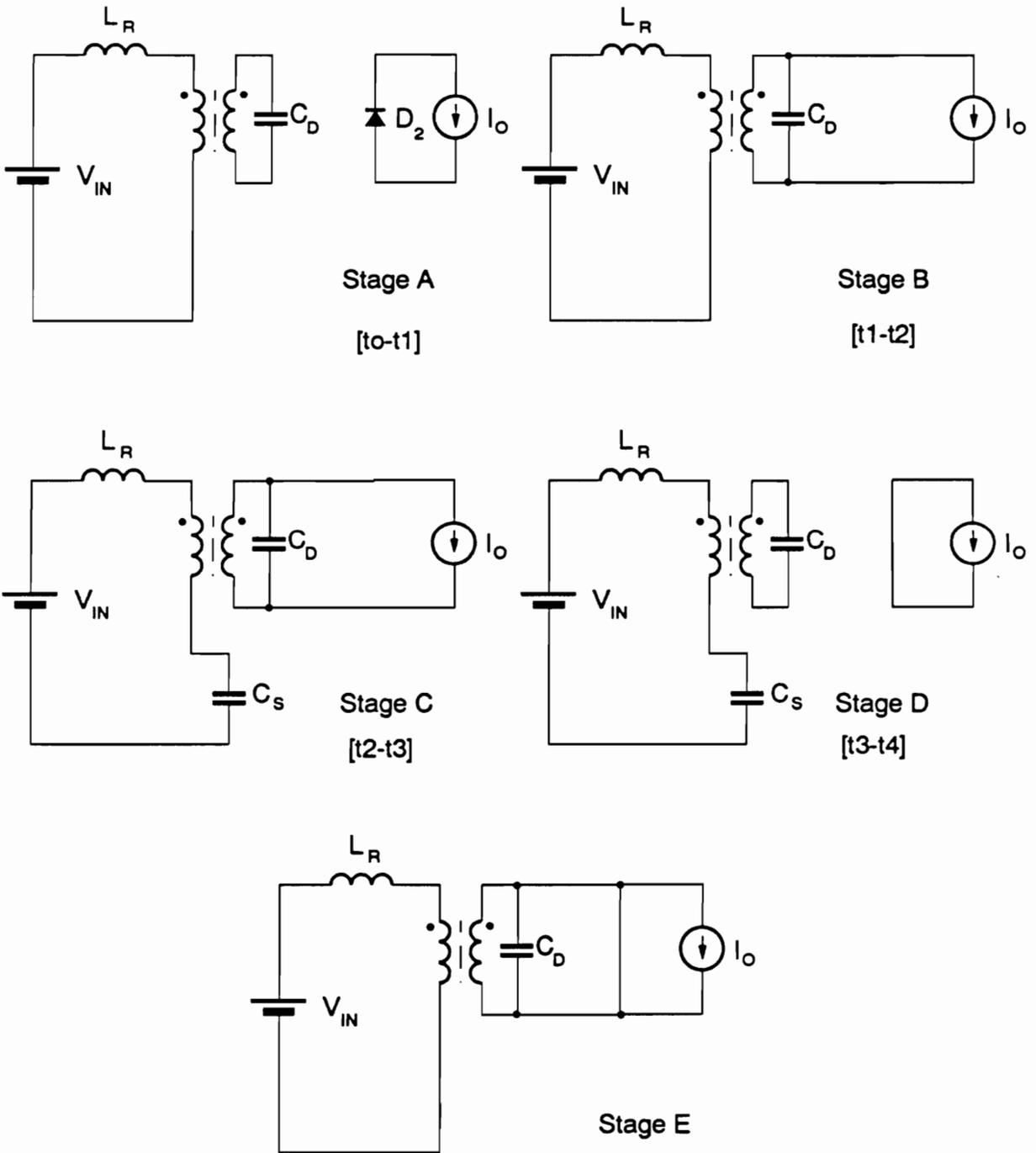
**Figure 5.4.** Topological stages of forward ZVS-MRC.

**Topological Stage E** may be present in the sequence of topological stages at certain operating conditions. Such conditions may be created at the end of Stage A, when voltage across the transformer becomes zero at $t_1$. If at $t_1$ the difference between the resonant-inductor current and the magnetizing current $(i_{LR} - I_M)$ is greater than the primary-reflected load current, Stage B will be entered. Otherwise, Stage E will be entered, since the current flowing from the transformer secondary winding at $t_1$ will be less than the load current, forcing both diodes, $D_1$ and $D_2$, to conduct. During Stage E the resonant-inductor current increases linearly until $i_{LR} - I_M$ becomes equal to the primary-reflected load current. This will turn off freewheeling diode D2 and cause transition to Stage C.

A detailed analysis of the operation of the forward ZVS-MRC is relatively involved [H16] and is not performed here. Instead, computer circuit simulation techniques are used to gather basic information about characteristics of the converter.

## 5.3. DC Characteristics

To gain an initial insight in the circuit operation, the forward ZVS-MRC was simulated using the Analog Workbench simulation program on an Apollo Workstation. The circuit diagram of the simulated circuit is shown in Fig. 5.5. The circuit is in a normalized form. The values of the resonant components are

selected so that the forward voltage drop of the rectifiers is small, compared to the output voltage. To achieve this, the characteristic impedance, $Z_0 = \sqrt{L_R/C_S}$, is set to 100 $\Omega$, and the input voltage is set to 100 V. The value of the magnetizing inductance is set to five times the value of the resonant inductance. This ratio of the magnetizing and resonant inductances is typical for the experimental converters described in Chapter 6. The value of $C_D$ is set to a value providing a desired $C_N = C_D/(N^2 C_S)$. Since $Z_0/V_{IN} = 1$, the load current corresponds directly to the normalized output current ($I_N = I_{OUT} Z_0/V_{IN}$).

The circuit was simulated for three values of $C_N$. For each $C_N$, $I_N$ was varied from 1 to 4, and switching frequency was varied to obtain the dc characteristics. Results of the simulation are presented in Tables 5.1-5.3. The normalized parameters are defined as follows:

$$f_N = \frac{f}{f_0} \quad , \tag{5.1}$$

$$f_0 = \frac{1}{2\pi\sqrt{L_R C_S}} \quad , \tag{5.2}$$

$$I_{MN} = \frac{I_M Z_0}{V_{IN}} \quad , \tag{5.3}$$

$$Z_0 = \sqrt{\frac{L_R}{C_S}} \quad , \tag{5.4}$$

$$M = \frac{V_{OUT} N}{V_{IN}} \quad , \tag{5.5}$$
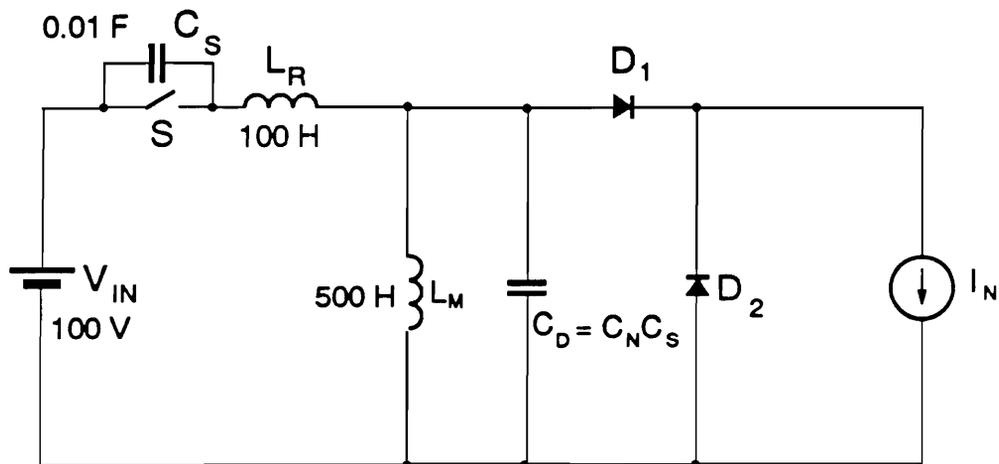
**Figure 5.5.** Simplified circuit of forward ZVS-MRC used in SPICE simulation.
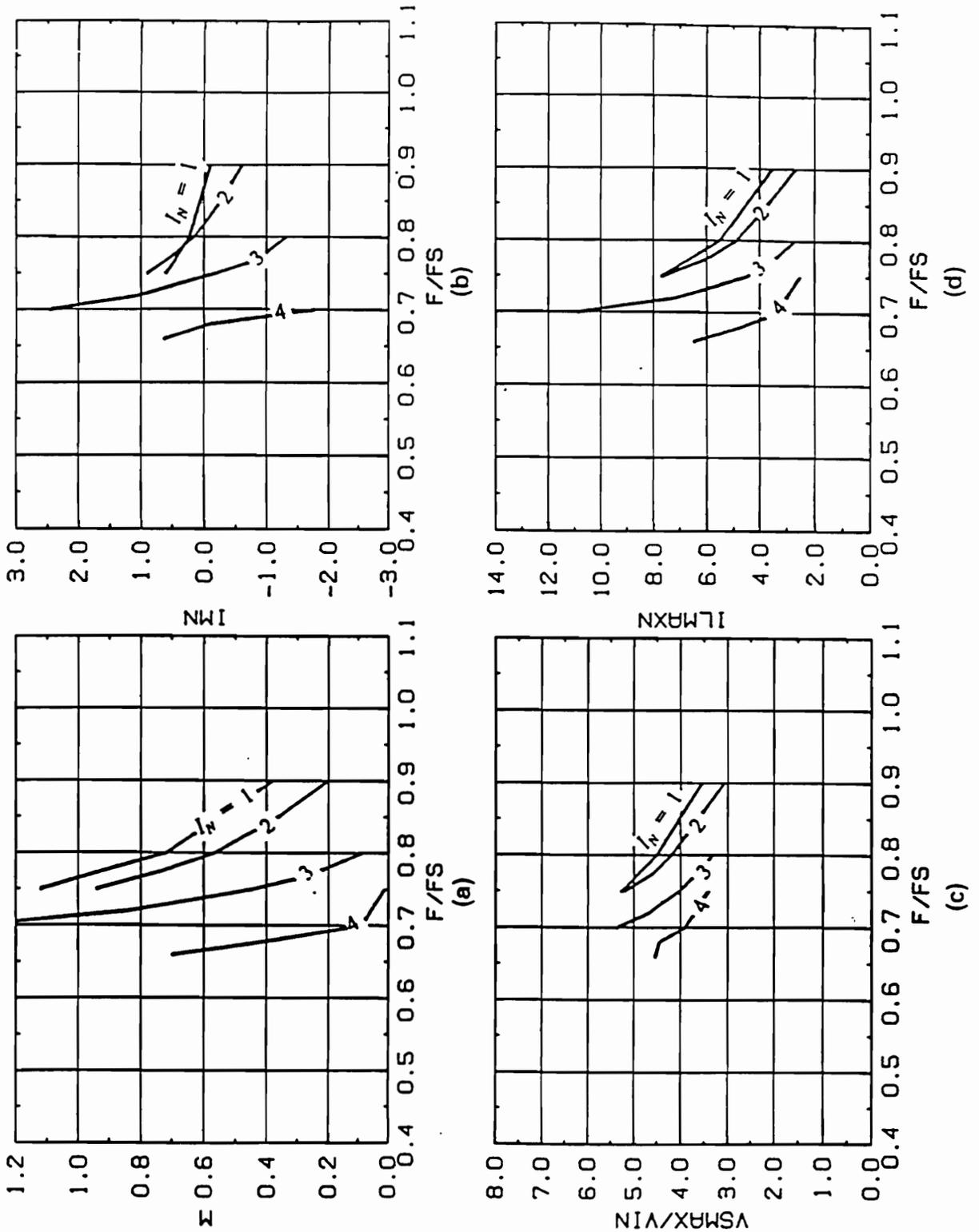
**Figure 5.6. Characteristics of forward ZVS-MRC at CN = 3: (a) Voltage conversion ratio. (b) Magnetizing current. (c) Transistor voltage stress. (d) Resonant inductor peak current.**
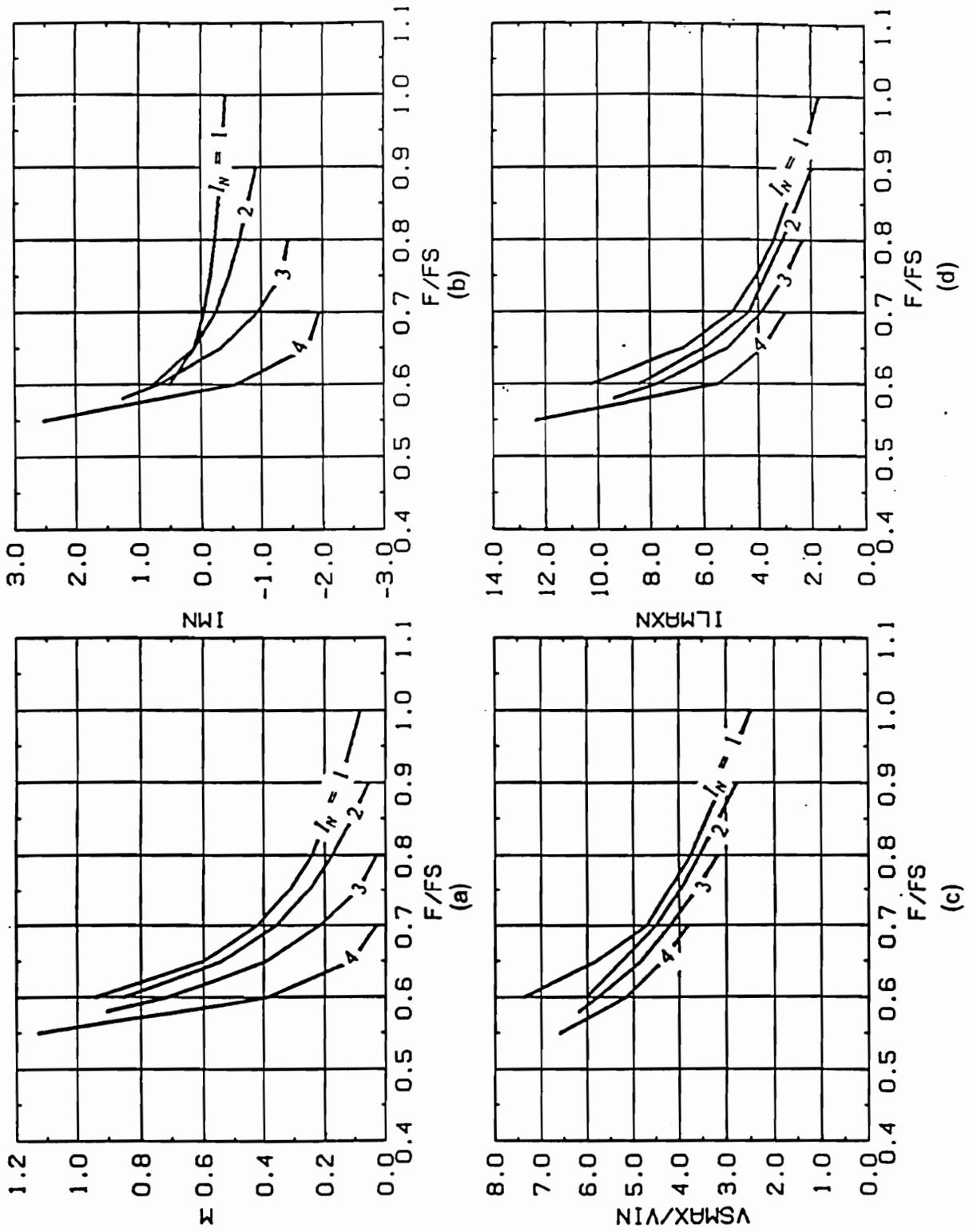
**Figure 5.7. Characteristics of forward ZVS-MRC at CN = 5: (a) Voltage conversion ratio. (b) Magnetizing current. (c) Transistor voltage stress. (d) Resonant inductor peak current.**
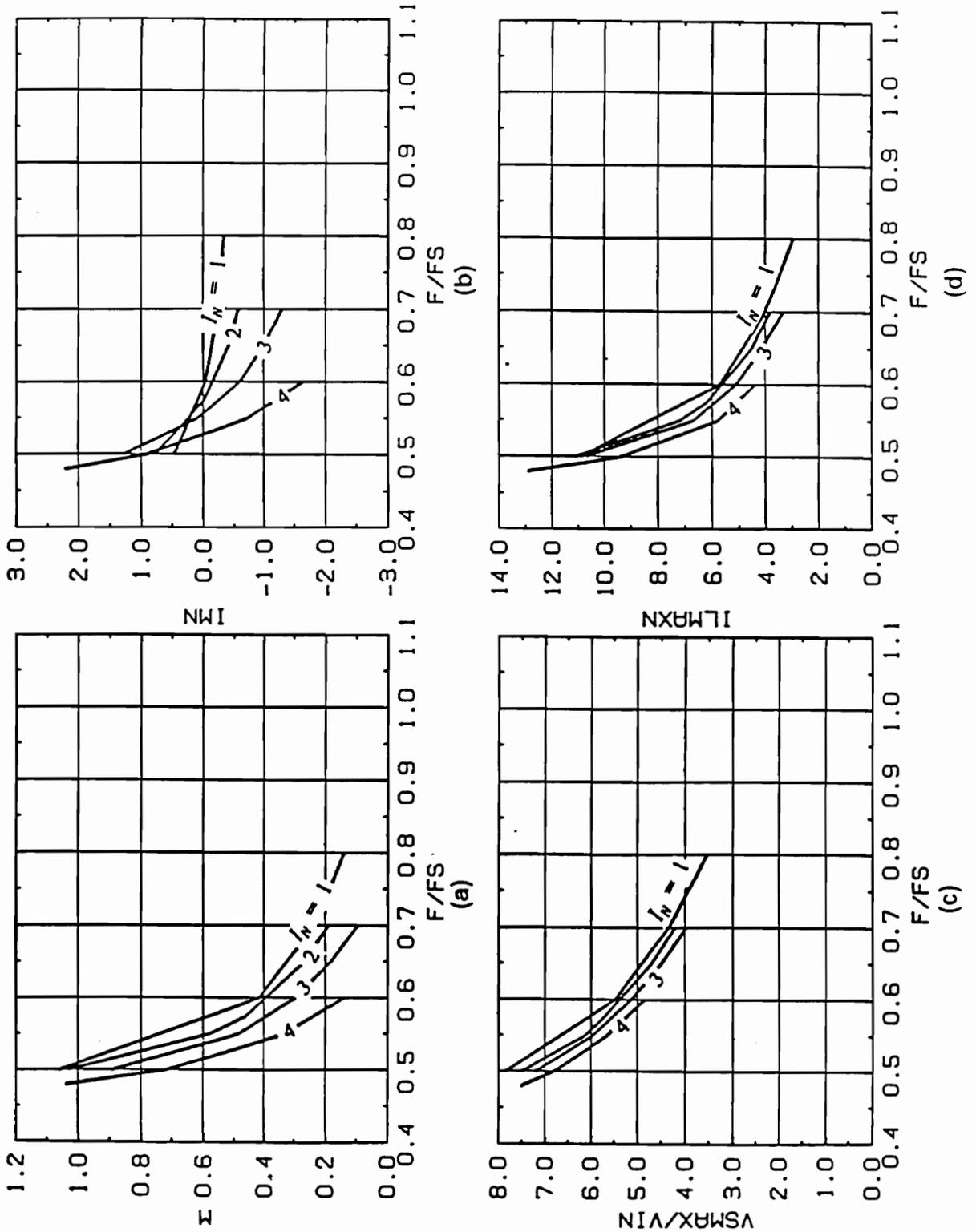
**Figure 5.8.** Characteristics of forward ZVS-MRC at CN = 7: (a) Voltage conversion ratio. (b) Magnetizing current. (c) Transistor voltage stress. (d) Resonant inductor peak current.
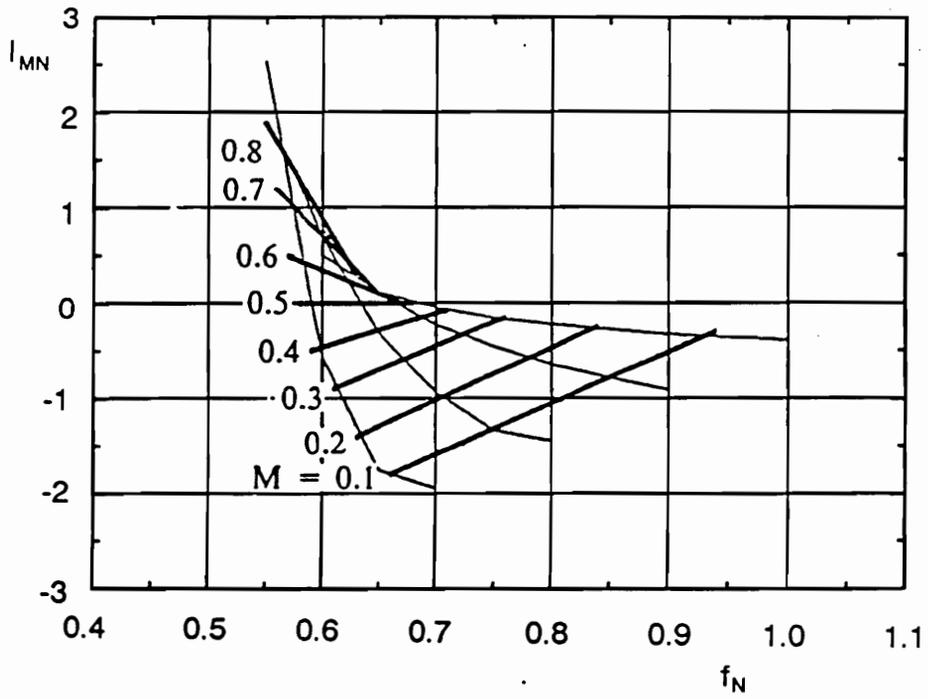
**Figure 5.9. Magnetizing current characteristics at CN = 5.**
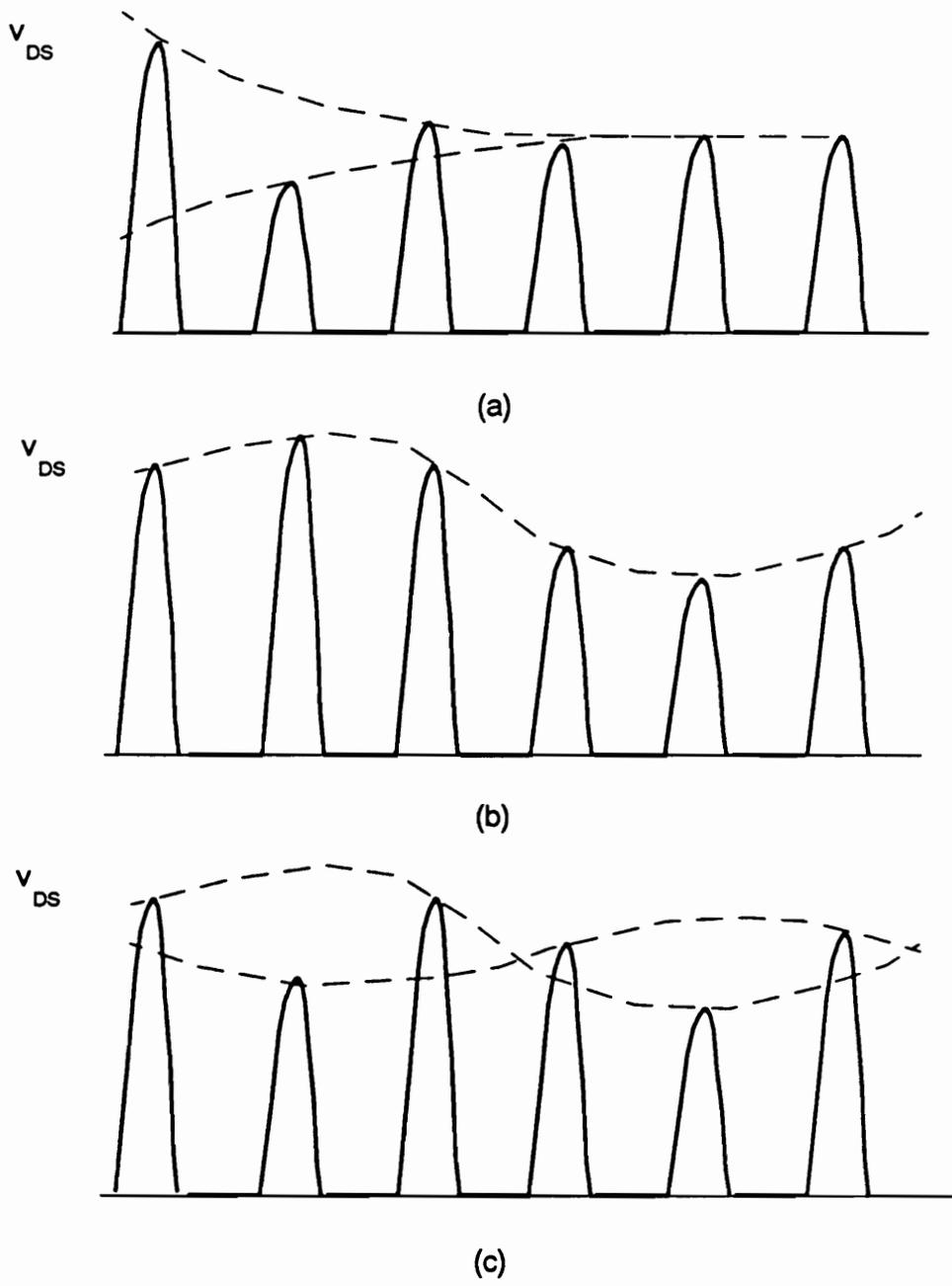
**Figure 5.10. Three types of transient oscillations observed during simulation:** (a) Sub-harmonic oscillations. (b) Low-frequency oscillations. (c) Sub-harmonic oscillations superimposed on low-frequency oscillations.

$$I_N = \frac{I_{OUT}Z_0}{NV_{IN}} \quad , \tag{5.6}$$

where N is the transformer turns ratio. Figures 5.6-5.8 show selected dc characteristics of the converter at different values of $C_N$.

One of the important results of the analysis is determination of the characteristics of the dc magnetizing current, $I_M$. Figure 5.9 shows $I_M$ versus switching frequency, with conversion ratio, M, as a running parameter, at $C_N = 5$. It can be seen that for M = 0.5, $I_M$ is approximately zero, regardless of the load (switching frequency changes when load resistance changes). For M > 0.5, $I_M$ is positive, while for M < 0.5 it is negative. For M different than 0.5, the magnitude of $I_M$ increases when the load current increases (switching frequency decreases). This behavior of the dc magnetizing current can be explained as follows. From Fig. 5.5,

$$I_M = I_{IN} - DI_O = I_O(M - D) \quad . \tag{5.7}$$

where $I_M$ is the dc magnetizing current, $I_O$ is the dc output current, and D is the duty ratio, defined as the ratio of the conduction time of diode D1 to the switching period. It can be seen, from (5.7), that the magnetizing current becomes zero when M = D. However, for most operating conditions, D is approximately equal to 0.5. Therefore, the magnetizing current is approximately zero when M = 0.5. It should be noted here that M is the conversion ratio of the normalized converter (with transformer turns ratio 1:1), and not the overall conversion ratio. Therefore, the value of M can, in general, be set to any de-

sired value by an appropriate selection of the transformer turns ratio. As a result, the magnitude of the magnetizing current can be controlled by adjusting the transformer turns ratio.

During the computer simulation of transients, the converter exhibited sub-harmonic oscillations at half of the switching frequency, causing an increase in the voltage stress. Also, low-frequency oscillations were noticed at light loads. Three types of oscillations observed during transients are illustrated in Fig. 5.10. The exact mechanism of these oscillations has not been explained. The low-frequency oscillation is most likely caused by the transformer's resetting mechanism.

## 5.4. Summary

The forward ZVS-MRC has significantly different behavior and characteristics than a buck ZVS-MRC. This is caused by the presence of the magnetizing inductance of the transformer and the forward diode in the rectifying circuit. The capacitor in parallel with the rectifier not only serves as a resonant component, but also provides means for resetting the transformer core. The transformer operates with a dc magnetizing current. The value of this current is a strong function of the operating conditions.

The forward ZVS-MRC topology has a number of desirable characteristics. The semiconductor devices operate with zero-voltage switching for a wide

**Table 5.1.** DC characteristics of forward ZVS-MRC at CN = 3.

| $f_N$ | $I_{MN}$ | M | $\dfrac{V_{Smax}}{V_{IN}}$ | $\dfrac{V_{Dmax}}{V_{IN}}$ | $I_{Lmax}$ | $I_N$ |
|-------|----------|-------|-------|-------|-------|-------|
| 0.750 | 0.595 | 1.120 | 5.27 | 3.890 | 7.73 | 1 |
| 0.800 | 0.232 | 0.721 | 4.52 | 2.520 | 5.52 | |
| 0.900 | -0.097 | 0.381 | 3.56 | 1.320 | 3.55 | |
| 1.000 | -0.265 | 0.214 | 2.83 | 0.725 | 2.36 | |
| 1.050 | -0.330 | 0.150 | 2.49 | 0.516 | 1.88 | |
| 0.750 | 0.899 | 0.942 | 5.21 | 3.360 | 7.66 | 2 |
| 0.775 | 0.501 | 0.733 | 4.58 | 2.490 | 6.00 | |
| 0.800 | 0.156 | 0.568 | 4.20 | 1.930 | 4.91 | |
| 0.850 | -0.260 | 0.365 | 3.65 | 1.250 | 3.72 | |
| 0.900 | -0.603 | 0.204 | 3.09 | 0.720 | 2.71 | |
| 0.70 | 2.460 | 1.330 | 5.38 | 4.200 | 10.9 | 3 |
| 0.72 | 1.060 | 0.844 | 4.70 | 2.670 | 7.23 | |
| 0.75 | -0.206 | 0.448 | 4.05 | 1.470 | 4.52 | |
| 0.77 | -0.844 | 0.261 | 3.75 | 0.970 | 3.62 | |
| 0.80 | -1.310 | 0.091 | 3.33 | 0.454 | 2.72 | |
| 0.66 | 0.627 | 0.701 | 4.54 | 2.050 | 6.51 | 4 |
| 0.68 | -0.068 | 0.379 | 4.46 | 1.350 | 4.74 | |
| 0.70 | -1.770 | 0.091 | 3.92 | 0.507 | 3.37 | |
| 0.75 | 0.000 | 0.012 | 3.43 | 0.134 | 2.54 | |

**Table 5.2.** DC characteristics of forward ZVS-MRC at CN = 5.

| $f_N$ | $I_{MN}$ | M | $\dfrac{V_{Smax}}{V_{IN}}$ | $\dfrac{V_{Dmax}}{V_{IN}}$ | $I_{Lmax}$ | $I_N$ |
|---|---|---|---|---|---|---|
| 0.60 | 0.512 | 0.942 | 7.39 | 3.950 | 10.3 | 1 |
| 0.65 | 0.120 | 0.604 | 5.83 | 2.330 | 6.74 | |
| 0.70 | -0.044 | 0.425 | 4.71 | 1.530 | 4.95 | |
| 0.75 | -0.145 | 0.317 | 4.23 | 1.140 | 4.10 | |
| 0.80 | -0.222 | 0.242 | 3.76 | 0.869 | 3.43 | |
| 0.90 | -0.331 | 0.147 | 3.07 | 0.513 | 2.46 | |
| 1.00 | -0.394 | 0.083 | 2.50 | 0.292 | 1.73 | |
| 0.60 | 0.785 | 0.856 | 6.03 | 3.000 | 8.45 | 2 |
| 0.65 | 0.115 | 0.544 | 5.27 | 1.920 | 5.97 | |
| 0.70 | -0.232 | 0.361 | 4.51 | 1.280 | 4.36 | |
| 0.75 | -0.453 | 0.253 | 3.99 | 0.896 | 3.76 | |
| 0.80 | -0.636 | 0.175 | 3.57 | 0.628 | 3.11 | |
| 0.85 | -0.776 | 0.112 | 3.16 | 0.420 | 2.52 | |
| 0.90 | -0.909 | 0.056 | 2.79 | 0.238 | 1.98 | |
| 0.58 | 1.260 | 0.906 | 6.18 | 3.050 | 9.43 | 3 |
| 0.60 | 0.700 | 0.720 | 5.79 | 2.440 | 7.76 | |
| 0.65 | -0.316 | 0.394 | 4.84 | 1.370 | 5.12 | |
| 0.70 | -0.930 | 0.216 | 4.20 | 0.782 | 3.91 | |
| 0.75 | -1.330 | 0.090 | 3.65 | 0.407 | 2.99 | |
| 0.80 | -1.440 | 0.029 | 3.19 | 0.176 | 2.35 | |
| 0.55 | 2.540 | 1.130 | 6.60 | 3.600 | 12.40 | 4 |
| 0.60 | -0.559 | 0.391 | 5.17 | 1.340 | 5.48 | |
| 0.65 | -1.750 | 0.111 | 4.37 | 0.540 | 3.85 | |
| 0.70 | -1.940 | 0.029 | 3.81 | 0.213 | 2.99 | |

**Table 5.3.** DC characteristics of forward ZVS-MRC at CN = 7.

| $f_N$ | $I_{MN}$ | M | $\dfrac{V_{Smax}}{V_{IN}}$ | $\dfrac{V_{Dmax}}{V_{IN}}$ | $I_{Lmax}$ | $I_N$ |
|---|---|---|---|---|---|---|
| 0.500 | 0.473 | 1.060 | 7.85 | 4.030 | 10.90 | 1 |
| 0.600 | -0.033 | 0.418 | 5.49 | 1.540 | 5.76 | |
| 0.700 | -0.239 | 0.231 | 4.36 | 0.853 | 4.03 | |
| 0.800 | -0.327 | 0.141 | 3.55 | 0.509 | 2.94 | |
| 0.500 | 0.781 | 1.030 | 7.50 | 3.605 | 11.13 | 2 |
| 0.550 | 0.249 | 0.581 | 6.15 | 2.080 | 7.22 | |
| 0.575 | -0.011 | 0.461 | 5.73 | 1.670 | 6.23 | |
| 0.650 | -0.407 | 0.266 | 4.72 | 0.970 | 4.56 | |
| 0.700 | -0.573 | 0.191 | 4.23 | 0.703 | 3.83 | |
| 0.50 | 1.282 | 0.893 | 7.20 | 3.100 | 10.70 | 3 |
| 0.55 | 0.098 | 0.486 | 5.97 | 1.730 | 6.72 | |
| 0.60 | -0.585 | 0.295 | 5.15 | 1.070 | 5.14 | |
| 0.65 | -0.989 | 0.182 | 4.52 | 0.679 | 4.14 | |
| 0.70 | -1.300 | 0.097 | 3.99 | 0.414 | 3.35 | |
| 0.48 | 2.220 | 1.040 | 7.52 | 3.450 | 12.90 | 4 |
| 0.50 | 0.912 | 0.720 | 6.80 | 2.440 | 9.37 | |
| 0.55 | -0.714 | 0.335 | 5.66 | 1.210 | 5.82 | |
| 0.60 | -1.630 | 0.140 | 4.86 | 0.615 | 4.42 | |

load range, practically from no load to full load. All major parasitic reactances of the power stage are absorbed by the resonant circuit. The latter, however, is only true if the resonant capacitance, $C_D$, is placed on the secondary side of the power transformer. Otherwise, the leakage inductance and junction capacitances of the rectifiers cannot be utilized in the resonant circuit. Another advantage is the automatic resetting mechanism provided by the resonant capacitance in parallel with the transformer. This feature significantly simplifies the converter's design and reduces the number of components necessary for a proper operation. Another advantage is a possibility of short-circuit protection by limiting the minimum switching frequency.

In summary, the forward ZVS-MRC is an attractive topology suitable for medium power levels (20-100 W). It is capable of operating at frequencies in the multi-megahertz range and is suitable for applications requiring high power density at medium power levels.

# 6. DESIGN OF HIGH-FREQUENCY HIGH-DENSITY ON-BOARD POWER SUPPLIES

The ever-increasing density of modern electronic equipment poses new challenges for power supply design. One area of intense research and development is design of on-board (also called on-card, board-mount, or point-of-load) dc/dc converters for distributed power systems. To be compatible with modern equipment, an on-board converter must have a high power density and a low profile. For some applications, such as on-board dc/dc converters for very high speed integrated circuit (VHSIC) systems, power densities as high as 50 W/in$^3$ are required, and even higher power densities are desirable. A typical requirement for the profile of an on-board converter is 0.25 in.

This chapter presents the development of high-density, high-efficiency, low-profile dc/dc converters with single or multiple outputs using the multi-resonant technology.

Two versions of a 50 W converter are developed: a single-output and a multiple-output. The single-output converter is designed for VHSIC applications and provides 5 V at a maximum load current of 10 A. The multiple-output converter has a closed-loop regulated 5 V output with maximum output current of 5 A and two cross-regulated $\pm$12 V outputs capable of supplying 1.2 A each.

# 6.1. Single-Output Converter Design

The single-output converter is designed for VHSIC loads. Such converters may be used as on-card regulators in a distributed power system, where power is delivered to the computer card via a pre-regulated 50$\pm$5 V bus.

### 6.1.1 Power Stage

The forward ZVS-MRC topology is chosen for the power stage of the on-board converter. The power stage, shown in Fig. 6.1, employs a resonant inductor, L1, in series with power transformer T1. Two resonant capacitors are used: the primary-side resonant capacitor, C2, is in parallel with the power switch, while the secondary-side resonant capacitor, C3, is placed across the secondary winding of T1.

The resonant circuit is characterized by three parameters:
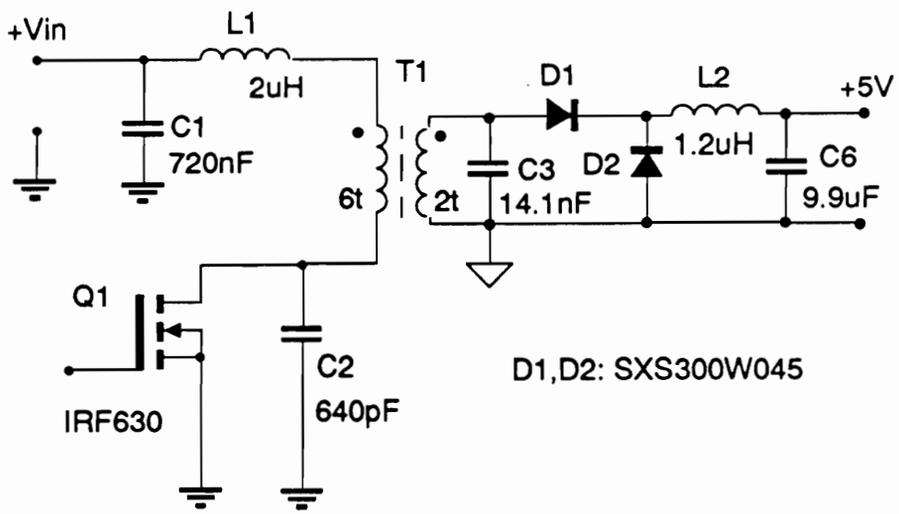
**Figure 6.1. Power stage of the single-output converter.**

$$f_0 = \frac{1}{2\pi\sqrt{L_1 C_2}} \quad , \tag{6.1}$$

$$Z_0 = \sqrt{\frac{L_1}{C_2}} \quad , \tag{6.2}$$

$$C_N = \frac{C_3}{N^2 C_2} \quad , \tag{6.3}$$

where N is the transformer's primary-to-secondary turns ratio.

The first step in the design process is the selection of N. The transformer in a forward ZVS-MRC operates with dc bias. To reduce losses in the transformer core, it is desirable to minimize this bias [M26]. This can be achieved by a proper selection of the turns ratio N. As explained in Chapter 5, the primary dc magnetizing current, $I_M$, is equal to the difference between the dc input current, $I_{IN}$, and the dc output current, $I_O$, reflected to the primary side and multiplied by rectifier duty ratio, D (defined as the ratio of conduction time of D1 to the switching period),

$$I_M = I_{IN} - \frac{I_O D}{N} \quad . \tag{6.4}$$

The exact value of D depends on the circuit's operating conditions. Typically, D is in the range of 0.45 to 0.5.

A total conversion ratio, $M_T$, can be defined by treating losses in the circuit as part of the load:

$$M_T = \frac{V_O}{\eta V_{IN}} \quad , \tag{6.5}$$

where $\eta$ is efficiency of the converter. Consequently, the input current is

$$I_{IN} = I_O M_T \quad . \tag{6.6}$$

Substituting (6) into (4):

$$I_M = \frac{I_O}{N} (N M_T - D) \quad . \tag{6.7}$$

From (6.7) it can be seen that if $N M_T = D$, the magnetizing current is zero. In practice, $M_T$ varies with input voltage. Magnetizing current can be reduced to zero at nominal input voltage by selecting:

$$N = \frac{D}{M_{Tnom}} \quad , \tag{6.8}$$

where $M_{Tnom}$ is $M_T$ at nominal input voltage.

Assuming $V_{INnom} = 50$ V, $V_O = 5$ V, $\eta = 80\%$, and D = 0.45, $M_{Tnom}$ is 0.125, and according to (6.8), N = 3.6. For practical reasons such as the limited window area in a low-profile transformer, the turns ratio is selected to be N = 3. Consequently, the maximum magnetizing current occurs at full load and high line and can be found using (6.7): $I_M = 10/3 \times (3 \times 0.114 - 0.45) = -0.36$A.

The resonant circuit component values, shown in Fig. 6.1, are optimized experimentally using the design guidelines established in Chapter 4, *i.e.*, $C_N$

is minimized, and $Z_0$ is maximized. Reduction of $C_N$ decreases the circulating energy and associated conduction losses in the transformer, power MOSFET, and resonant inductor. Increased $Z_0$ results in a lower amplitude resonant inductor current and reduced conduction losses in the primary-side components (Q1, L1, and the primary winding of T1). The optimized resonant circuit parameters (including the effect of the parasitic capacitances of the switches and the leakage inductance of the transformer) are: $f_0 = 3.8$ MHz, $Z_0 = 52$ $\Omega$, and $C_N = 2.5$.

To minimize the ESR of the resonant capacitors, NPO ceramic chip capacitors are used for C2 and C3. C2 utilizes two 270 pF and one 100 pF, 500 V capacitors, while C5 uses three NPO, 4.7 nF, 100 V capacitors in parallel.

Since the multi-resonant topology absorbs the rectifier's junction capacitance into the resonant circuit, it is possible to use large-die-area, low-drop Schottky diodes to minimize conduction loss in the rectifier. In the experimental converter, the diodes are 300x300 mil$^2$ Schottky rectifiers with current and voltage ratings of 120 A and 45 V.

## 6.1.2. Control Circuit

The forward ZVS-MRC uses a variable-frequency control. To maintain zero-voltage switching of the power MOSFET, the off-time pulse is constant, and the frequency is varied by changing the on-time.
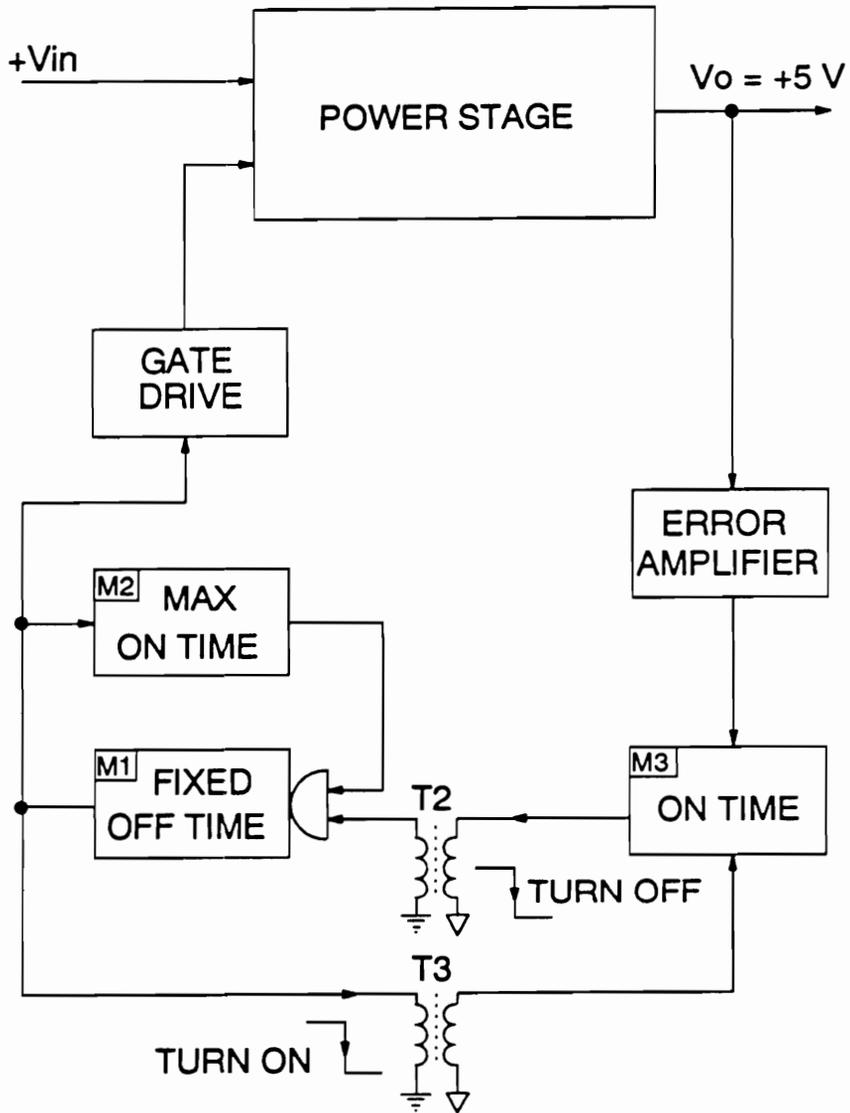
**Figure 6.2. Control circuit block diagram.**

The functional block diagram of the control circuit is shown in Fig. 6.2. Gate drive is controlled by a fixed off-time, variable on-time oscillator. The off-time is set by single-shot M1, located on the primary side. During start-up, when the output voltage is below 5 V, duration of the on-time (maximum on-time) is set by single-shot M2. To achieve a soft start, duration of the pulse produced by M2 is initially limited and then gradually increased. When the output voltage reaches 5 V, the error amplifier is activated, and its output determines the duration of the pulse generated by single-shot M3. M3 is triggered at the end of the off-time through pulse transformer T3. At the end of the on-time (whose duration is controlled by the error amplifier), M3 sends (through T2) a turn-off command to the primary control circuit. The maximum on-time, limited by M2, is adjusted to be slightly longer than the longest on-time encountered during normal operation. (The longest on-time occurs at full load and low line). This provides a simple short-circuit protection scheme by limiting the minimum switching frequency.

The implementation of the control circuit is shown in Fig. 6.3. A MOTOROLA MC34151 driver is used as a gate driver for Q1. The on- and off-time single-shots M1-M3 are implemented using advanced-CMOS logic. The constant off-time is adjusted by R1 and C9. The maximum on-time is set by R2 and C10. The error amplifier is a single-supply, MOTOROLA MC33071 op-amp.
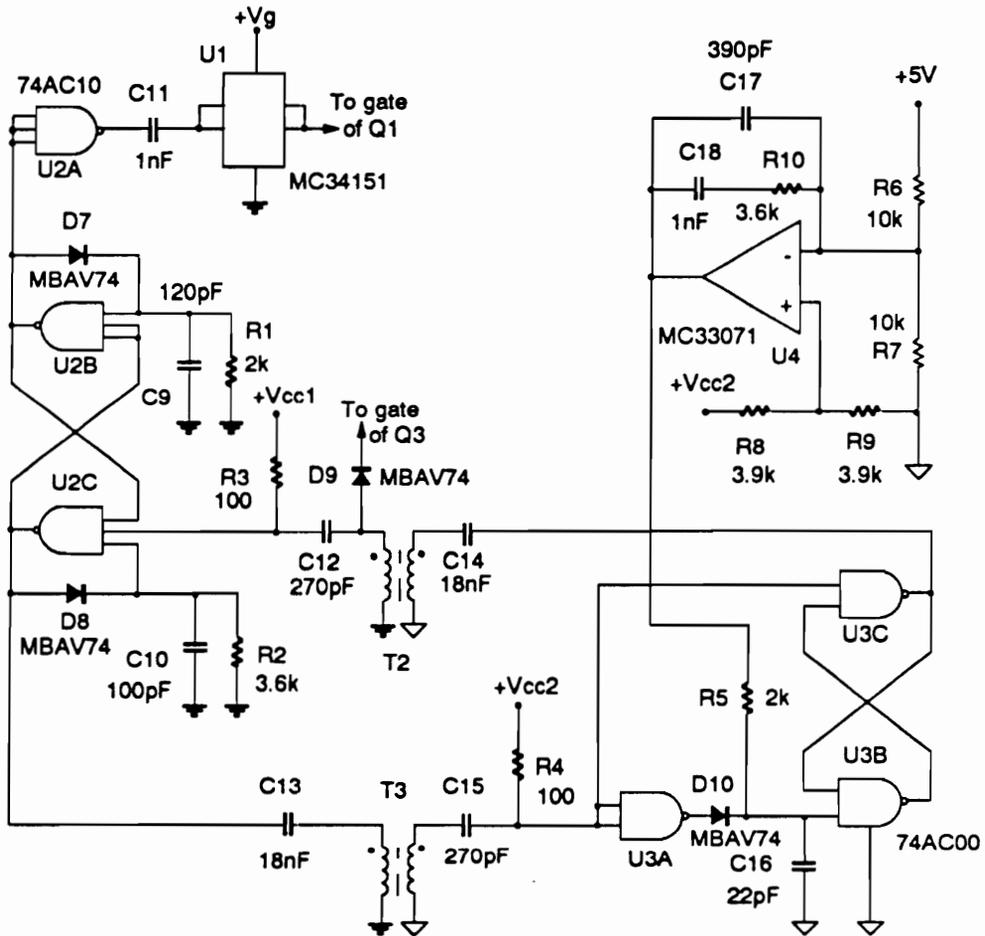
**Figure 6.3.  Control circuit implementation.**

### 6.1.3. Self Bias Circuit

Fig. 6.4 shows the start-up and self-bias circuits. Self-bias voltages Vcc1 and Vg are derived for the primary-side control circuit from the power transformer using auxiliary windings. During start-up, power for the primary control is derived from the input voltage, using Zener diode D13 and MOSFET Q2. After initial application of the input voltage, Q3 is off, and Q2 operates in the active region and provides a regulated voltage of approximately 8 V (12 V from the Zener diode minus 4 V gate threshold voltage) to gate driver U1 and voltage regulator U5. The start-up circuit remains active until the output voltage reaches 5 V and the secondary control starts sending control pulses through transformer T2 to adjust the on-time (see Fig. 6.3). In addition to the control function, these pulses are used to turn on Q3 and consequently, disable the start-up circuit to avoid excessive power dissipation. This scheme provides a reliable start-up sequence that ensures a proper bias voltage is derived from the input until the converter output is regulated. Bias for the secondary-side control circuit is derived from the rectifier voltage using peak detector D14-C22 and voltage regulator U6.
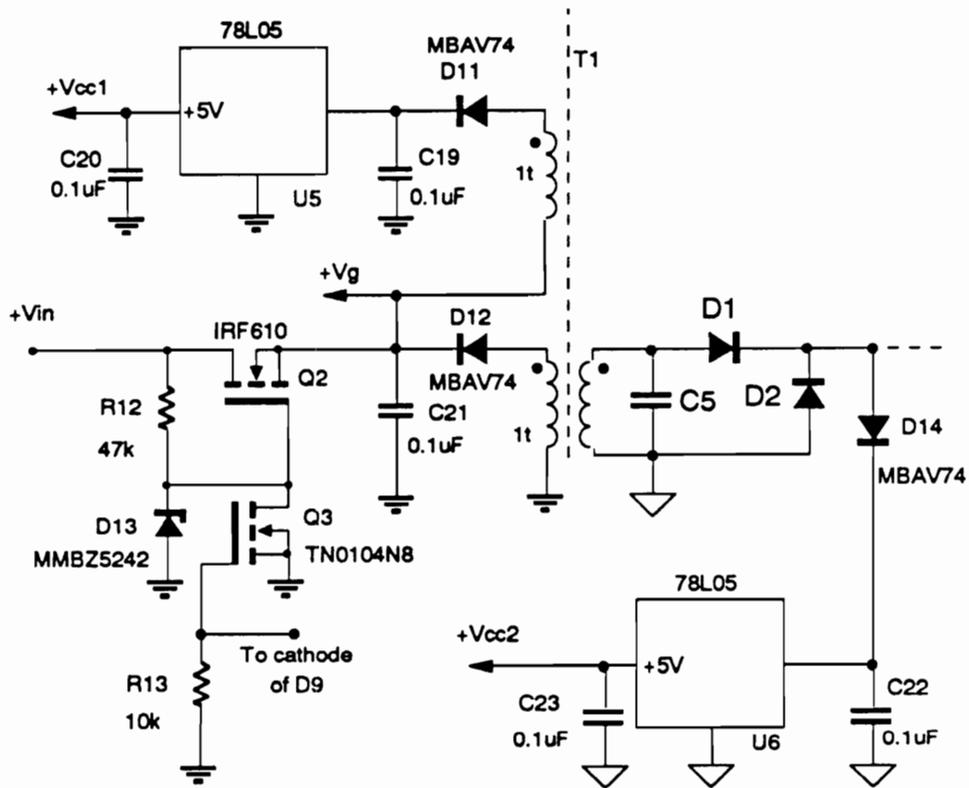
**Figure 6.4. Start-up and self-bias circuit.**

### 6.1.4. Low-Profile Magnetics

There are three magnetic components in the power stage: resonant inductor L1, power transformer T1, and output-filter inductor L2. All these components are designed to fit into the package with a low profile of 0.25 in.

The resonant inductor is built with a powdered iron toroidal core T44-6 (MICROMETALS) and with a winding of 22 turns of 100/44 Litz wire. The inductor operates with a peak ac flux density of 24 mT at the full load of 10 A and a nominal line of 50 V.

Figure 6.5(a) shows the EI core used for the power transformer. The core is custom made of CQ100 (Ceramic Magnetics) ferrite. Due to the high density of the converter, dimensions of the core are essentially limited by the available height and footprint area inside the package. Figure 6.5(b) shows a cross-sectional view of the transformer. The primary winding consists of six turns of 100/44 Litz wire, while the secondary winding has two turns of 5-mil copper foil. AWG#30 magnet wire is used for the auxiliary windings. This particular winding arrangement is chosen for its simple arrangement (easy to assemble) and low resistance. The winding arrangement optimization is described in Appendix D. The magnetizing inductance of the transformer is 12 $\mu$H, and the leakage inductance measured from the primary side, with secondary shorted, is 180 nH.

Figure 6.6 shows construction of the transformer. The secondary consists of two U-shaped foil strips. The assembly of the transformer starts with placing the first turn of the secondary inside the E-part of the core, as shown in Fig.

(a)



| PRIMARY WINDING SIX TURNS LITZ WIRE 100/44 | | Q1 CORE |

SECONDARY WINDING (TWO TURNS)

AUXILIARY WINDINGS
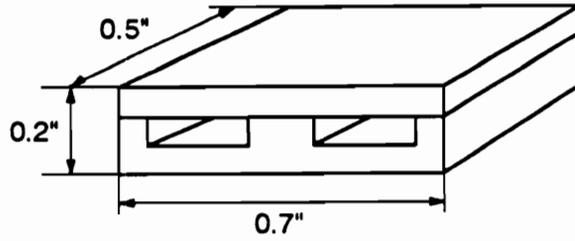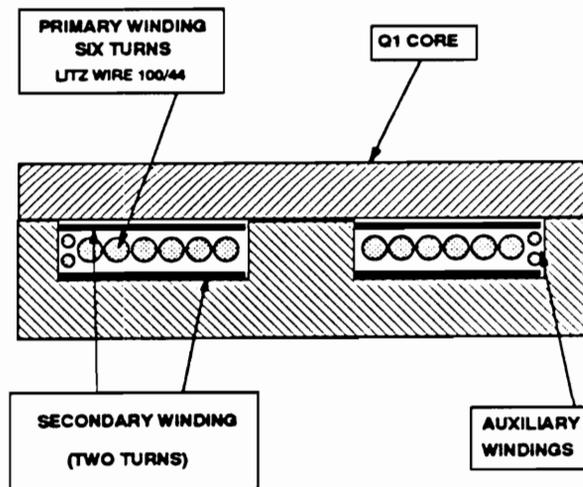
(b)

**Figure 6.5. Power transformer design for the single-output converter: (a) Core dimensions. (b) Transformer cross-section.**
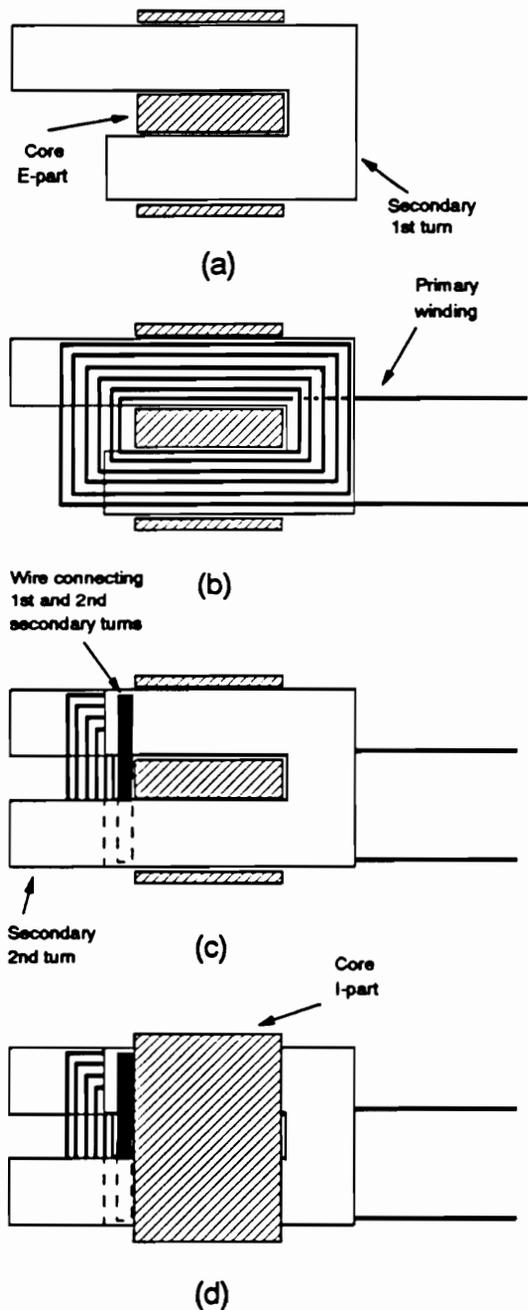
**Figure 6.6.** Construction of the low-profile transformer: (a) The first turn of the secondary winding is placed inside the E-part of the core. (b) The primary winding is placed in the core. (c) The second turn of the secondary winding is placed on top of the primary winding, and a wire is added to connect the secondary turns. (d) The I-part is attached to close the magnetic path.

6.6(a). The six turns of primary winding are wound inside the core, Fig. 6.6(b). The second turn of the secondary is then placed on top of the primary winding, as shown in Fig. 6.6(c). Finally, the I-part of the core is attached on top of the transformer, as depicted in Fig. 6.6(d). The first and second turns of the secondary winding are connected with a wire soldered to the shorter ends of each foil.

The output-filter inductor has a modified H7F-SMD ER 14.5 core (TDK) and a winding of two turns of 175/44 Litz wire. The core design is the same as that shown in Fig. 6.18(b).

### 6.1.5. Hybridization

The entire converter, including gate drive, self-bias, and control circuits, is placed in a 0.25×2×2 in³ aluminum package. Layout of the hybridized converter is shown in Fig. 6.7. Power stage, gate drive, and the primary and secondary control circuits are assembled on an alumina substrate with thick-print silver conductors. Surface-mount components are used throughout. Power rectifiers, the secondary-side resonant capacitor, and the output filter capacitor are placed on a copper-clad alumina substrate with etched conductors. The 10 mil copper on this substrate helps minimize conduction losses in the secondary, high-current circuit. The power transformer and resonant inductor are attached directly to the bottom of the package using a thermoconductive epoxy.

0.25"

L1

POWER TRANSFORMER

D2
C3
D1

C4

OUTPUT

INPUT

INPUT FILTER
POWER MOSFET
GATE DRIVE

START-UP
AND
SELF-BIAS

L2

PRIMARY-SIDE
CONTROL

SECONDARY-SIDE
CONTROL

2"

2"
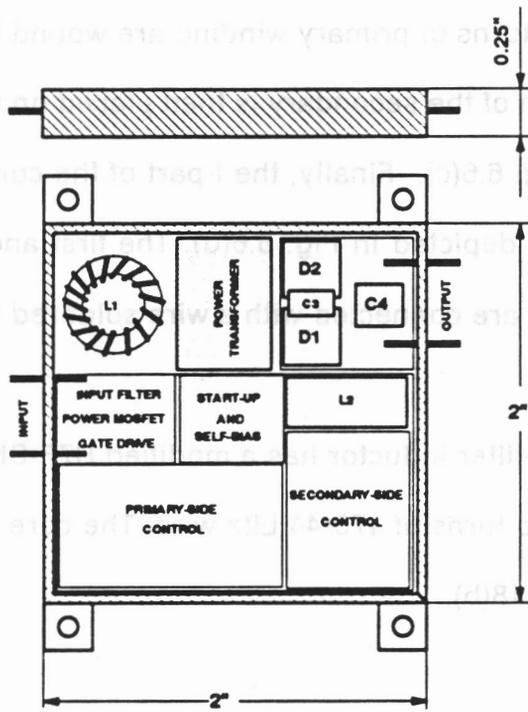
(a)
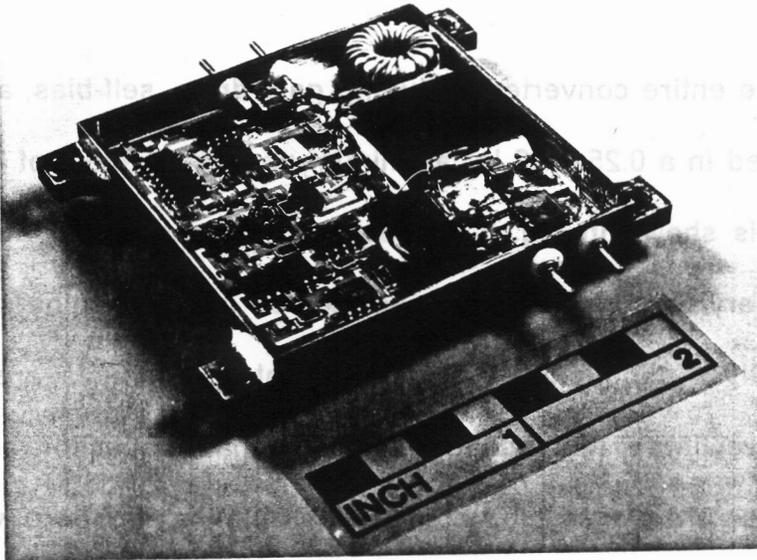
(b)

**Figure 6.7. Hybridized converter: (a) Layout. (b) Photograph.**

INCH
1
2

The power density of the complete converter is 50 W/in³, while the power density of the power stage only is approximately 100 W/in³. When an integrated controller is used, it will be feasible to increase the overall power density to approximately 75 W/in³.

# 6.2. Electrical Performance of the Single-Output Converter

All measurement results are obtained for the complete power supply, including gate drive, control, and self-bias circuits. Measurements are performed for input voltages from 10V to 60 V, and load currents from 0 to 12 A.

### 6.2.1. Switching Waveforms

Typical waveforms at nominal line of 50 V and full load of 10 A are shown in Fig. 6.8. At these conditions, the MOSFET voltage stress is approximately 190 V, and its current stress is 3.5 A. The power MOSFET operates with zero-voltage switching. Voltage measured across the secondary winding of the power transformer is semi-sinusoidal with no parasitic oscillations. Since this voltage is applied to the rectifiers, D1 and D2 also operate with zero-voltage switching. The voltage stress on each diode is approximately 20 V, or $4 \times V_O$.
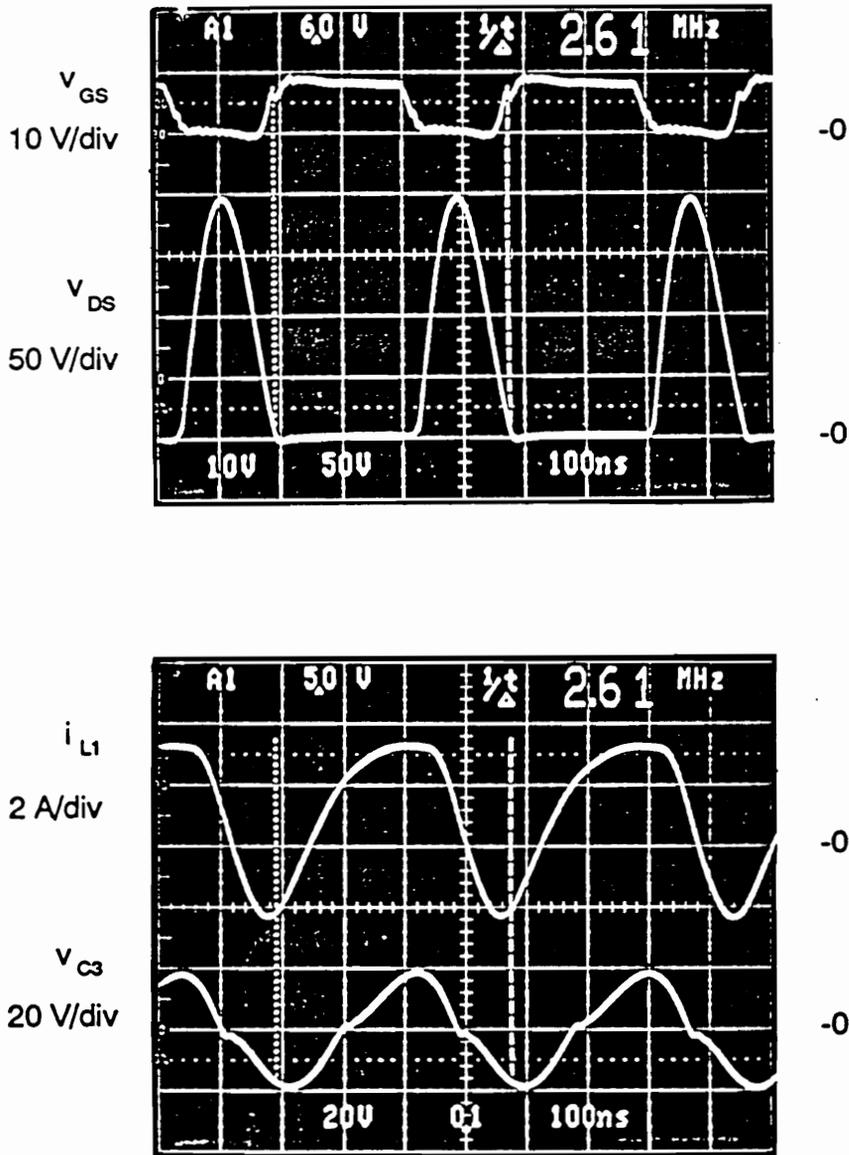
Figure 6.8. Waveforms at nominal line and full load.

## 6.2.2. Static Characteristics

Measured parameters of the converter at various levels of input voltage are given in Table 6.1. All measurements were made for a complete power supply including gate drive, control, and self-bias circuits. The measurements were performed for wide range of input voltages, from 10V to 60 V, to demonstrate the behavior of the supply at extreme line conditions. At line voltages higher than 50 V, the supply can support loads as high as 12 A. When line voltage is reduced below 44 V, the output voltage drops below 5 V at full load but can be maintained at 5 V for lower output currents. Figure 6.9(a) shows the range of input voltage and output current for which the converter can regulate output voltage at 5 V. For line voltages higher than 50 V, a 12 A load can be supported. When the line voltage is reduced below 43 V, the output voltage falls below 5 V at full load but can be maintained at 5 V for lower output currents.

The switching frequency range for all load/line conditions is shown in Fig. 6.9(b). For the specified operating range (shaded area), the switching frequency varies from 2.5 to 3.85 MHz. Therefore regulation of the output voltage is achieved with $\pm 20\%$ frequency modulation for the full range of input voltage (45-55 V) and load current (0-10 A).

The voltage stress on the power MOSFET is shown in Fig. 6.9(c). The maximum voltage stress at $V_{in} = 55$ V is 208 V. The IRF630 device used in the experimental converter has a measured breakdown voltage of 240 V.

**Table 6.1. Measured dc characteristics of forward ZVS-MRC.**

| $V_{IN}$ | f | $I_{IN}$ | Vo | Io | $V_{Speak}$ | Pin | Po | Pdiss | $\eta$ |
|---|---|---|---|---|---|---|---|---|---|
| V | MHz | A | V | A | V | W | W | W | % |
| 60 | 2.71 | 1.230 | 5.07 | 12.0 | 232 | 73.80 | 60.84 | 12.96 | 82.4 |
| 60 | 2.98 | 1.032 | 5.07 | 10.0 | 221 | 61.90 | 50.70 | 11.20 | 81.9 |
| 60 | 3.20 | 0.833 | 5.08 | 8.0 | 210 | 49.98 | 40.64 | 9.34 | 81.3 |
| 60 | 3.33 | 0.645 | 5.08 | 6.0 | 205 | 38.70 | 30.48 | 8.22 | 78.8 |
| 60 | 3.50 | 0.456 | 5.09 | 4.0 | 200 | 27.36 | 20.36 | 7.00 | 74.4 |
| 60 | 3.67 | 0.268 | 5.10 | 2.0 | 197 | 16.08 | 10.20 | 5.88 | 63.4 |
| 60 | 3.69 | 0.169 | 5.10 | 1.0 | 192 | 10.14 | 5.10 | 5.04 | 50.3 |
| 60 | 3.94 | 0.090 | 5.10 | 0.1 | 174 | 5.40 | 0.51 | 4.89 | 9.4 |
| 55 | 2.54 | 1.339 | 5.07 | 12.0 | 225 | 73.65 | 60.84 | 12.81 | 82.6 |
| 55 | 2.85 | 1.121 | 5.07 | 10.0 | 208 | 61.66 | 50.70 | 10.96 | 82.2 |
| 55 | 3.10 | 0.903 | 5.08 | 8.0 | 200 | 49.66 | 40.64 | 9.02 | 81.8 |
| 55 | 3.30 | 0.704 | 5.09 | 6.0 | 193 | 38.72 | 30.54 | 8.18 | 78.9 |
| 55 | 3.43 | 0.506 | 5.09 | 4.0 | 189 | 27.83 | 20.36 | 7.47 | 73.2 |
| 55 | 3.55 | 0.298 | 5.10 | 2.0 | 186 | 16.39 | 10.20 | 6.19 | 62.2 |
| 55 | 3.61 | 0.188 | 5.10 | 1.0 | 181 | 10.43 | 5.10 | 5.33 | 49.3 |
| 55 | 3.85 | 0.089 | 5.10 | 0.1 | 164 | 4.90 | 0.51 | 4.39 | 10.4 |
| 50 | 2.34 | 1.468 | 5.07 | 12.0 | 223 | 73.40 | 60.84 | 12.56 | 82.9 |
| 50 | 2.71 | 1.220 | 5.07 | 10.0 | 197 | 61.00 | 50.70 | 10.30 | 83.1 |
| 50 | 2.98 | 0.990 | 5.08 | 8.0 | 186 | 49.50 | 40.64 | 8.86 | 82.1 |
| 50 | 3.20 | 0.760 | 5.08 | 6.0 | 181 | 38.00 | 30.48 | 7.52 | 80.2 |
| 50 | 3.36 | 0.550 | 5.09 | 4.0 | 178 | 27.50 | 20.36 | 7.14 | 74.0 |
| 50 | 3.45 | 0.317 | 5.10 | 2.0 | 175 | 15.85 | 10.20 | 5.65 | 64.4 |
| 50 | 3.54 | 0.198 | 5.10 | 1.0 | 171 | 9.90 | 5.10 | 4.80 | 51.5 |
| 50 | 3.84 | 0.079 | 5.10 | 0.1 | 153 | 4.35 | 0.51 | 3.84 | 11.7 |
| 45 | 2.50 | 1.359 | 5.08 | 10.0 | 185 | 61.60 | 50.80 | 10.36 | 83.1 |
| 45 | 2.85 | 1.091 | 5.08 | 8.0 | 171 | 49.10 | 40.64 | 8.46 | 82.8 |
| 45 | 3.08 | 0.843 | 5.09 | 6.0 | 166 | 37.94 | 30.54 | 7.40 | 80.5 |
| 45 | 3.23 | 0.605 | 5.09 | 4.0 | 166 | 27.23 | 20.36 | 6.87 | 74.8 |
| 45 | 3.34 | 0.347 | 5.10 | 2.0 | 162 | 15.62 | 10.20 | 5.42 | 65.3 |
| 45 | 3.43 | 0.219 | 5.10 | 1.0 | 160 | 9.86 | 5.10 | 4.76 | 51.8 |
| 45 | 3.71 | 0.079 | 5.10 | 0.1 | 144 | 3.56 | 0.51 | 3.05 | 14.3 |
| 40 | 2.46 | 1.379 | 5.08 | 9.0 | 168 | 55.16 | 45.72 | 9.44 | 82.8 |
| 40 | 2.67 | 1.230 | 5.08 | 8.0 | 159 | 49.20 | 40.64 | 8.56 | 82.6 |
| 40 | 2.95 | 0.943 | 5.09 | 6.0 | 155 | 37.72 | 30.54 | 6.68 | 81.0 |
| 40 | 3.17 | 0.675 | 5.09 | 4.0 | 153 | 27.00 | 20.36 | 6.64 | 75.4 |
| 40 | 3.26 | 0.387 | 5.10 | 2.0 | 152 | 15.48 | 10.20 | 5.28 | 65.9 |
| 40 | 3.34 | 0.248 | 5.10 | 1.0 | 148 | 9.92 | 5.10 | 4.82 | 51.4 |
| 40 | 3.56 | 0.089 | 5.10 | 0.1 | 135 | 3.56 | 0.51 | 3.05 | 14.3 |
| 30 | 2.63 | 1.250 | 5.09 | 6.0 | 122 | 37.50 | 30.54 | 6.96 | 81.4 |
| 30 | 3.38 | 0.109 | 5.10 | 0.1 | 112 | 3.27 | 0.51 | 2.76 | 15.6 |
| 20 | 2.69 | 1.032 | 5.10 | 3.0 | 91 | 20.64 | 15.30 | 5.34 | 74.1 |
| 20 | 3.08 | 0.159 | 5.10 | 0.1 | 86 | 3.18 | 0.51 | 2.67 | 16.0 |
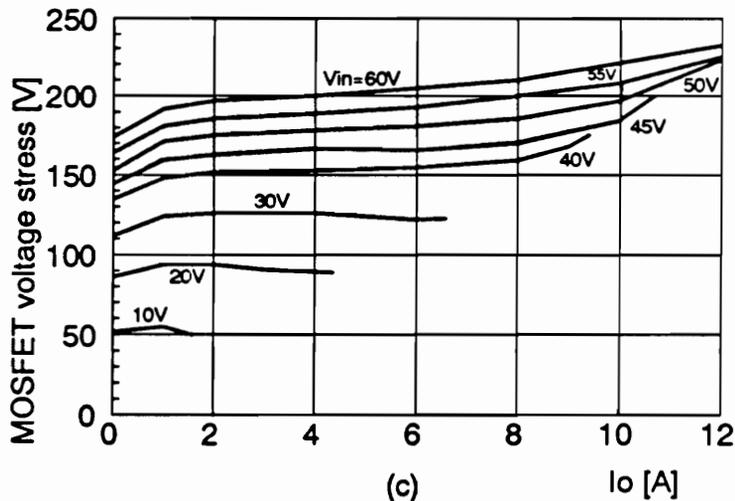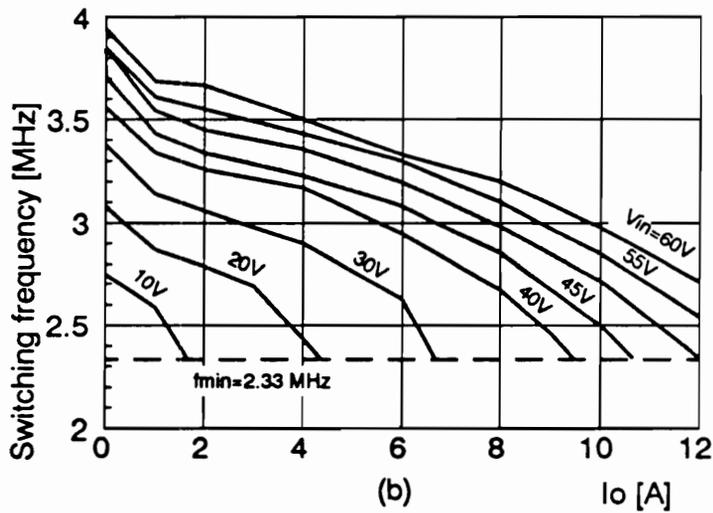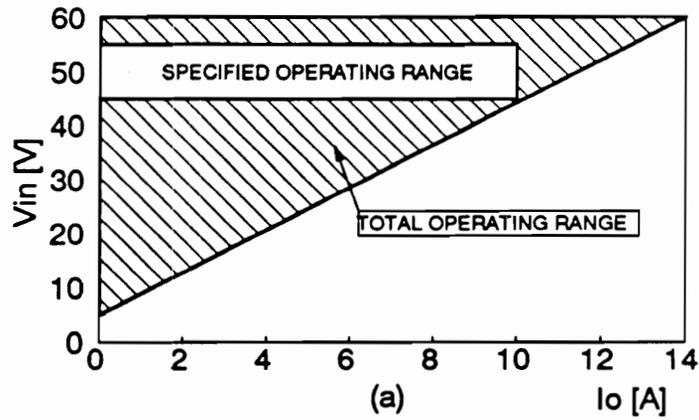
Figure 6.9. Measured dc characteristics of a forward ZVS-MRC: (a) Operating range. (b) Switching frequency range. (c) MOSFET voltage stress.

Figure 6.10(a) shows the converter's efficiency at various line and load conditions. The shaded area depicts the specified operating conditions. A maximum efficiency of 83% is achieved at full load and nominal line. Figure 6.10(b) illustrates dependence of the efficiency on the load current at nominal line. At medium and light loads, efficiency is reduced; however, it is still higher than 80% for loads above 30 W. The reduced efficiency at medium and light loads does not cause a thermal problem, since the highest power dissipation occurs at full load.

The power loss distribution was estimated using the circuit waveforms and device characteristics such as winding resistance, core loss, on-resistance, etc., (either measured, calculated, or acquired from data books), and current and voltage waveforms measured in the experimental converter. To simplify the loss analysis, it was assumed that the ac conduction loss and core loss are caused by the first harmonic only. The estimated loss distribution is shown in Table 6.2. Almost one-third of the power dissipation is caused by conduction loss in the rectifier diodes. A significant improvement of the conversion efficiency could be achieved if the rectification losses are reduced using synchronous rectification. However, to avoid excessive switching loss caused by the large input capacitances of the low on-resistance MOSFETs used in synchronous rectifier applications, resonant gate-drive schemes may be necessary.
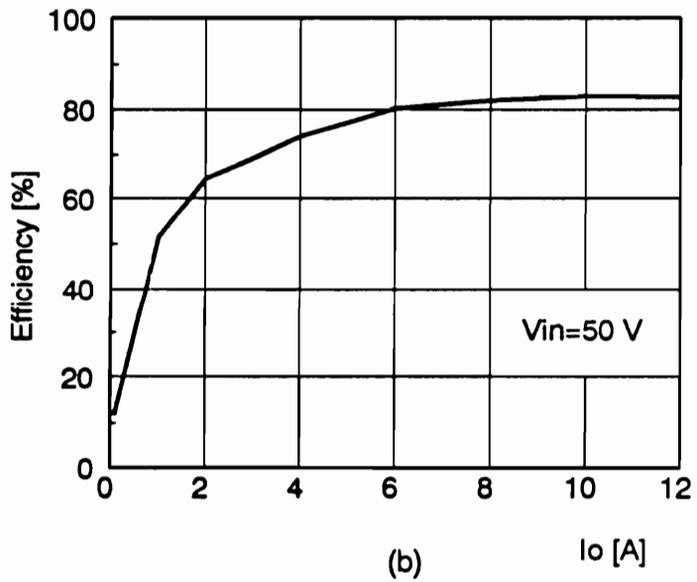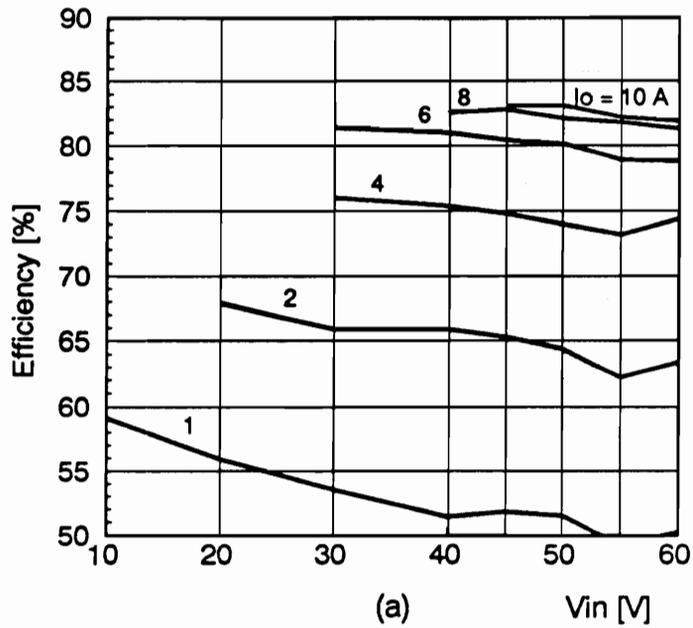
**Figure 6.10.** Overall efficiency of the single-output converter: (a) As a function of input voltage. (b) As a function of output current.

**Table 6.2.   Power dissipation distribution.**

| Component | | [W] | [W] | [%] |
|---|---|---|---|---|
| Resonant Inductor | Core<br>Winding | 0.87<br>0.36 | 1.23 | 11.9 |
| MOSFET | Conduction on-time<br>Conduction off-time | 1.60<br>0.06 | 1.66 | 16.1 |
| Transformer | Core<br>Prim. wind.<br>Sec. wind. | 0.99<br>0.27<br>0.26 | 1.52 | 14.8 |
| Resonant Capacitors | Primary<br>Secondary | 0.08<br>0.08 | 0.16 | 1.6 |
| Rectifying Diodes | Due to Io<br>Due to Cj | 3.00<br>0.25 | 3.25 | 31.6 |
| Filter Inductor | Core<br>Winding | 0.15<br>0.32 | 0.47 | 4.6 |
| Control | Primary and gate drive<br>Secondary | 0.85<br>0.20 | 1.05 | 10.2 |
| Unidentified losses | | | 0.96 | 9.2 |
| Total | | | 10.3 | 100 |

### 6.2.3. Dynamic Characteristics

The small-signal characteristics were obtained in a slightly different version of the converter. This version was designed for a wider input-voltage range (40-60 V). Figure 6.11 shows a simplified circuit diagram of the power stage used for evaluation of the dynamic performance. Details of the design of this converter are given in [H19].

To evaluate the small-signal characteristics of the converter, small-signal measurements were performed using an HP4194A Impedance/Gain-Phase Network Analyzer. The control-to-output transfer function characteristics are shown in Figs. 6.12(a) and 6.12(b) for light load and heavy load, respectively. The transfer function was measured from the output of the error amplifier to the output voltage.

The compensation network uses a single zero placed at 44 kHz, which corresponds approximately to the corner frequency of the output filter. A high-frequency pole is provided by the operational amplifier. The loop-gain characteristics at the nominal line of 50 V are shown in Fig. 6.13 for full load and light load. Crossover frequency is a function of line and load, and varies from 28 kHz at light load and high line to 87 kHz at full load and high line. A stability phase margin of 42 degrees or better and a gain margin of 10 dB or better are achieved for all operating conditions.

Figure 6.14 shows output impedance characteristics at full load and light load and nominal input voltage. Audiosusceptibility characteristics are plotted in Fig. 6.15.
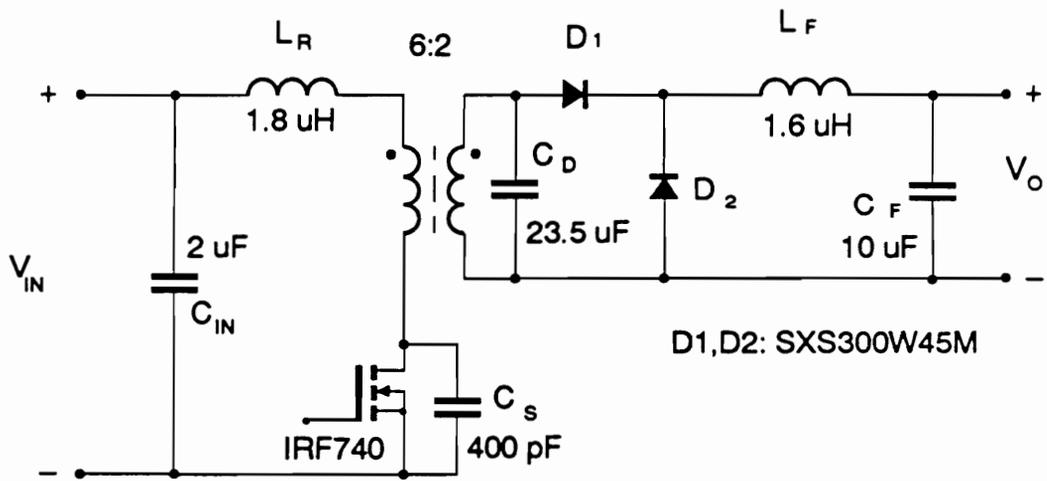
**Figure 6.11. Power stage of a forward ZVS-MRC used for small-signal measurements.**
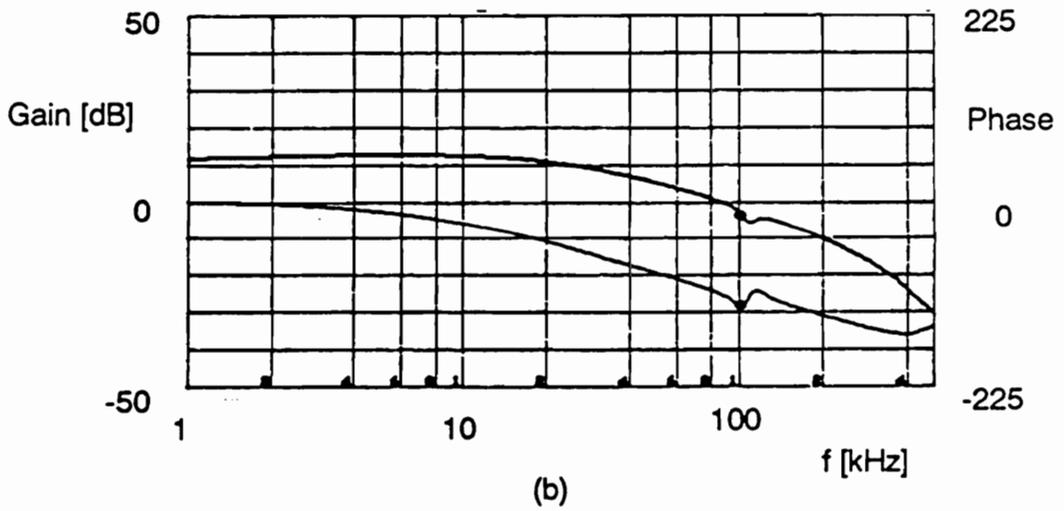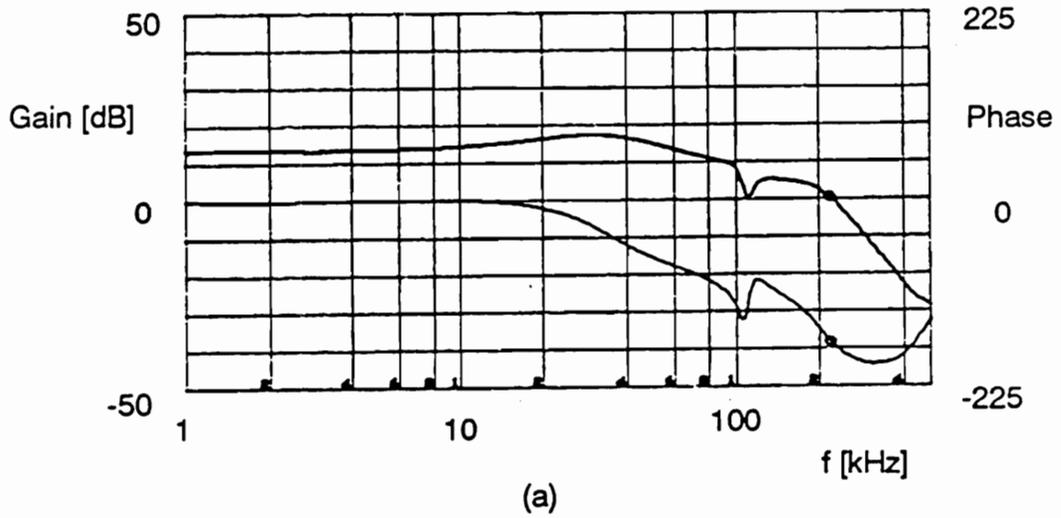
**Figure 6.12.** Control-to-output transfer function at nominal line of 50 V: (a) Full load of 10 A. (b) Light load of 1 A.
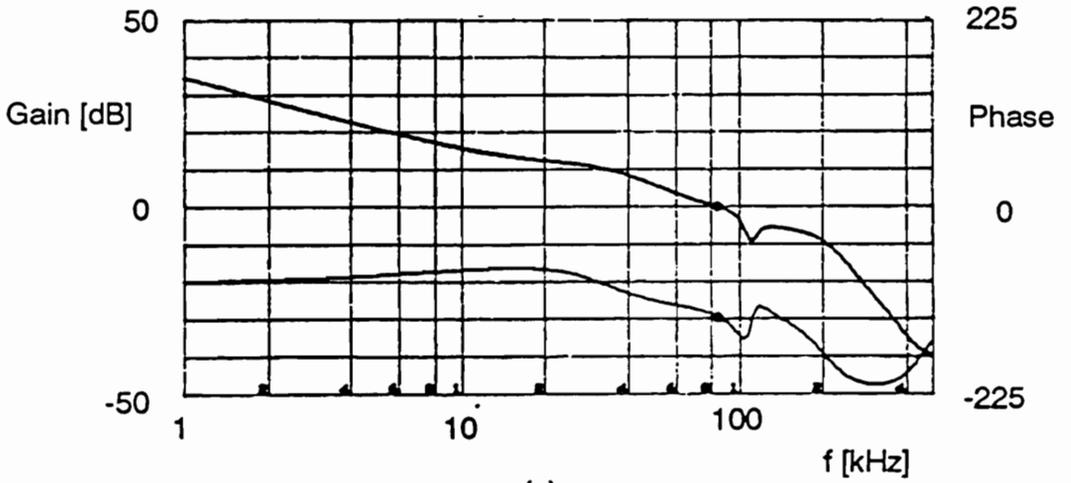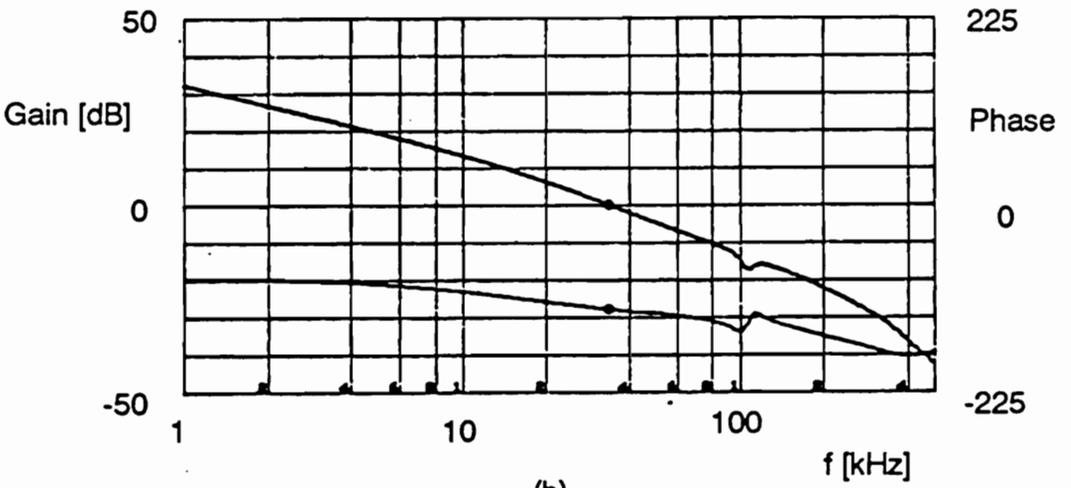
**Figure 6.13.** Loop-gain transfer function at nominal line of 50 V: (a) Full
load of 10 A. (b) Light load of 1 A.
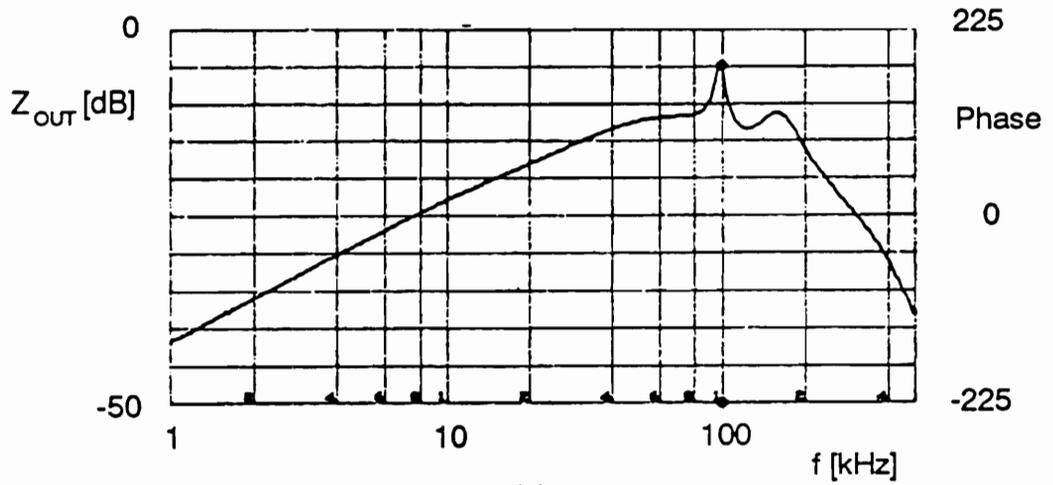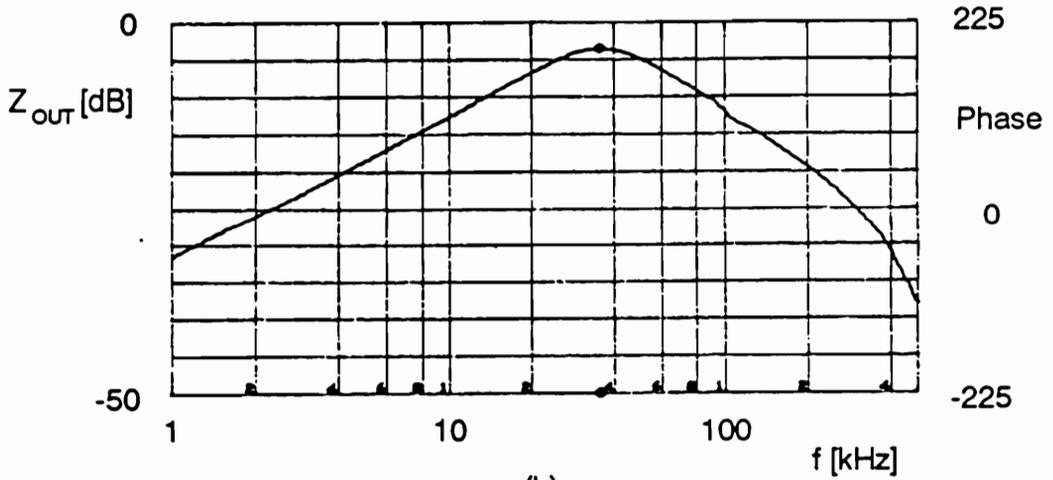
**Figure 6.14.** Output impedance at nominal line of 50 V: (a) Full load of 10 A. (b) Light load of 1 A.

Audiosusceptibility [dB]



(a)

Audiosusceptibility [dB]
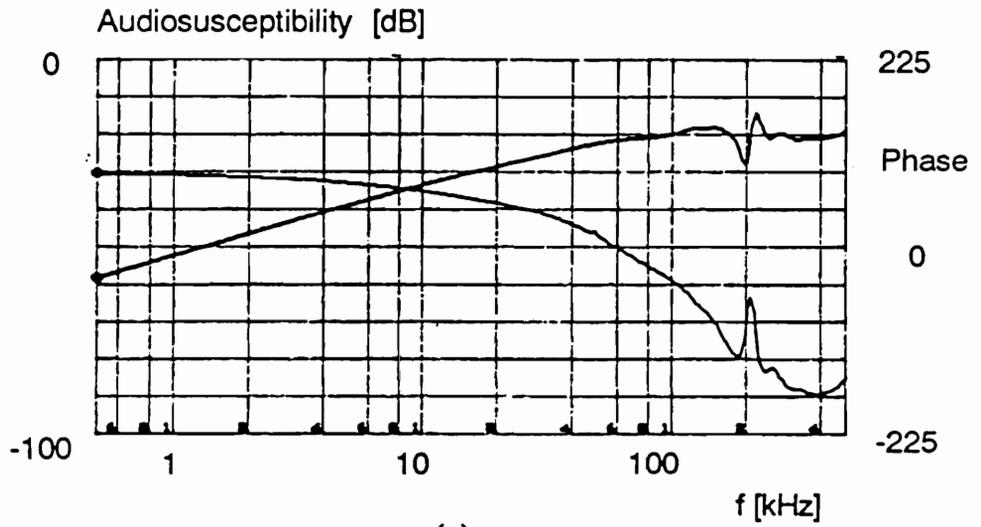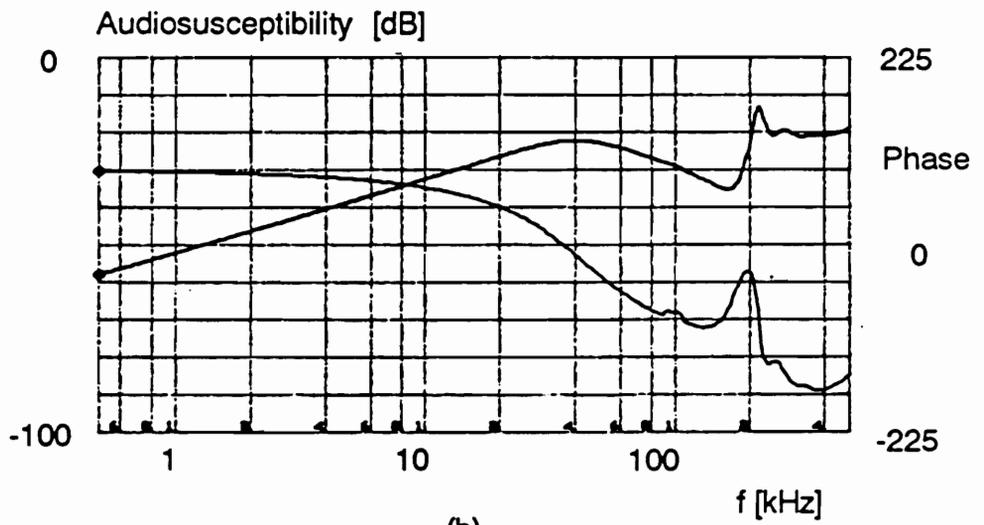


(b)

**Figure 6.15.   Audiosusceptibility at nominal line of 50 V:   (a) Full load of 10 A. (b) Light load of 1 A.**

The transient response of the converter to a step load current change of 1 A is shown in Fig. 6.16. In Fig 6.16(a), load current changes from 9 to 10 A, while in Fig. 6.16(b), load current changes from 1 A to 2 A. The settling time is approximately 20 $\mu$s. The output voltage overshoot is approximately 160 mV (worst case) at high line and light load.

# 6.3. Multiple-Output Converter Design

The multiple-output converter is designed to operate with a nominal input voltage of 50 V and three outputs: +5 V @ 5 A, +12 V @ 1.2 A, and -12 V @ 1.2 A. The +5 V output is closed-loop regulated, and the ±12 V outputs are cross regulated using multiple windings on the power transformer and a coupled output-filter inductor design.

Design of the multiple-output converter is based on the single-output converter design. The control and bias circuits remain unchanged. The same magnetic structures are used, but the winding arrangements are modified.

### 6.3.1. Power Stage Design

A circuit diagram of the multiple-output power stage is shown in Fig. 6.17. The primary side is identical to that of the single-output converter. On the secondary side, the resonant capacitance is formed by capacitors C3-C5,
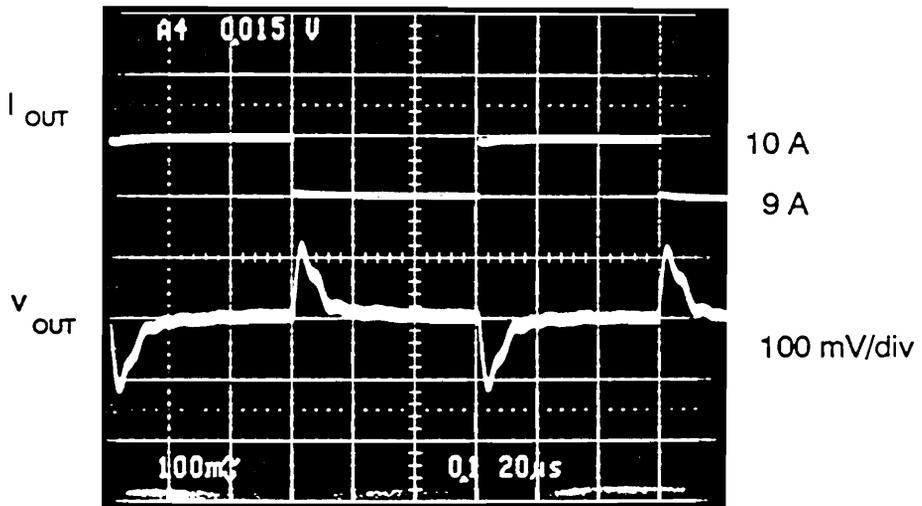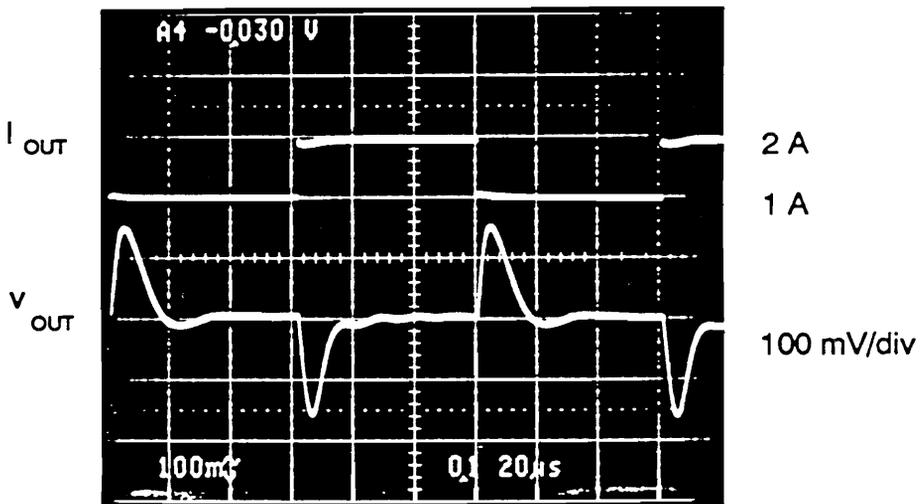
Figure 6.16.   Transient response at nominal line of 50 V:   (a) At heavy load. (b) At light load.

placed across each secondary winding. Turns ratios of the transformer are 6:2:5:5. Output filter inductors are wound on a common core, with turns ratios identical to that of the transformer, *i.e.*, 2:5:5. A coupled-inductor design is used to minimize filter inductor size and to provide good dynamic cross-regulation. All diodes are Schottky rectifiers; D1 and D2 are rated at 30 A and 45 V, while D3-D6 are rated at 1.1 A and 100 V.

### 6.3.2. Magnetics Design

Figure 6.18(a) shows the design of the multiple-winding transformer. The power transformer has a core identical to that used for the single-output con-verter. The $+5$ V winding is formed by two turns of 5 mil copper foil, while the primary winding and windings for the $\pm12$ V outputs are 50/44 Litz wire. The winding structure is symmetrical to provide identical coupling of each of the $\pm12$ V windings to the primary winding and to the $+5$ V winding. Leakage inductance measured from one of the 12 V windings, with the $+5$ V winding shorted, is 140 nH.

The configuration of the output-filter inductor is shown in Fig. 6.18(b). The $+5$ V winding is two turns of 5 mil copper foil, while the $\pm12$ V windings are 5 turns of 75/44 Litz wire. As in the transformer, the winding structure of the inductor is symmetrical to provide identical coupling between each of the $\pm12$ V windings and the $+5$ V winding. Leakage inductance measured from the 12 V winding, with the 5 V winding shorted, is 150 nH.
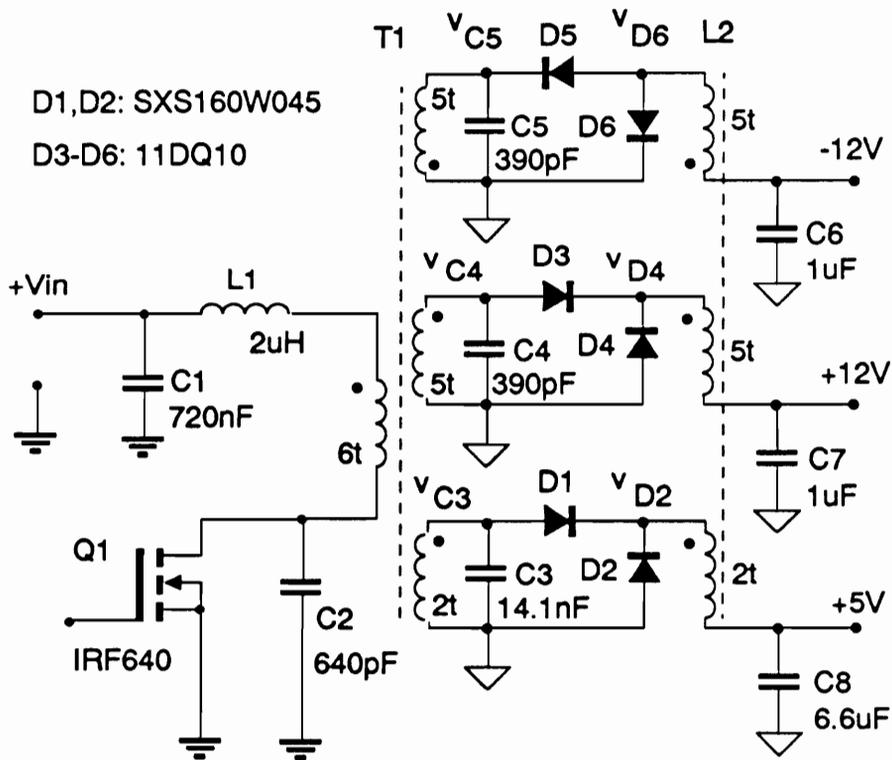
**Figure 6.17. Power stage of the multiple-output converter.**
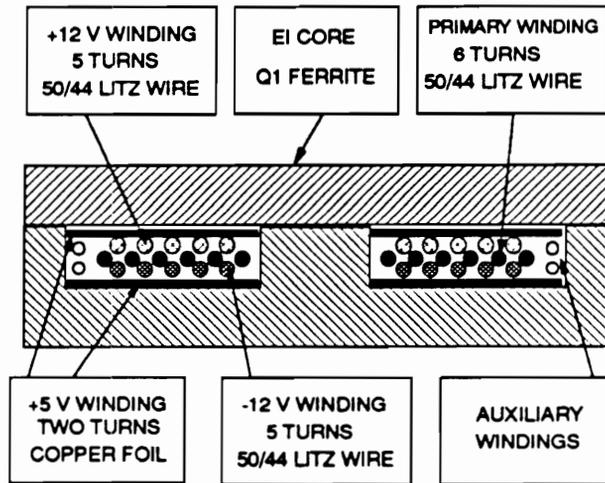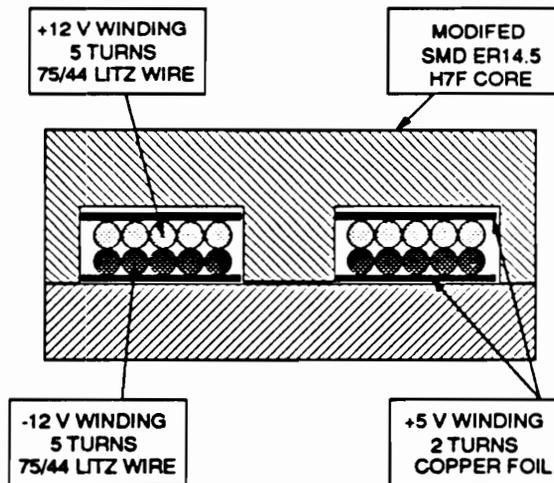
**Figure 6.18. Low-profile magnetics for the multiple-output converter: (a) Power transformer. (b) Output-filter inductor.**

## 6.4. Multiple-Output Converter Performance

### 6.4.1. Switching Waveforms

Typical switching waveforms of the multiple-output converter are shown in Figs. 6.19 and 6.20. As in the single-output converter, primary waveforms of $v_{DS}$ and $i_{L1}$ show no parasitic oscillations. Secondary waveforms however, do display some parasitic oscillations. These oscillations are caused by leakage inductances between the output windings of T1. Therefore, unlike the primary-to-secondary leakage, leakage inductances formed between the output windings of the multiple-winding transformer are not absorbed by the multi-resonant circuit. It should be noted that waveforms of the + 12 V and -12 V outputs are highly symmetrical, which confirms previous statements about symmetry of the transformer and inductor windings.

A conversion efficiency of 79% was measured with full load at each output, and Vin = 50 V. This efficiency figure is lower than that for the single-output converter mainly due to increased conduction losses in the transformer and filter inductor, caused by the thinner conductors used for the windings. These winding losses could be reduced if the profile of the package is increased.
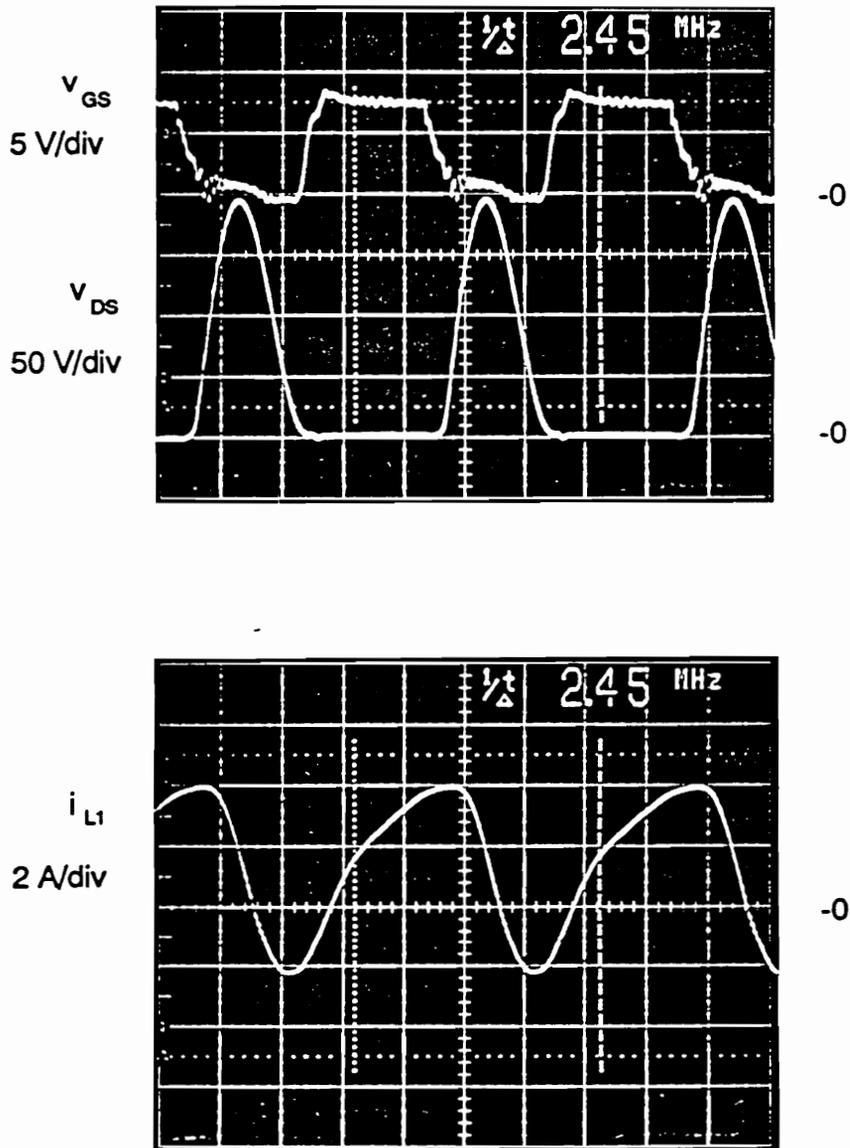
**Figure 6.19. Primary waveforms in multiple output converter:** $V_{IN} = 50$ **V. All outputs fully loaded.**
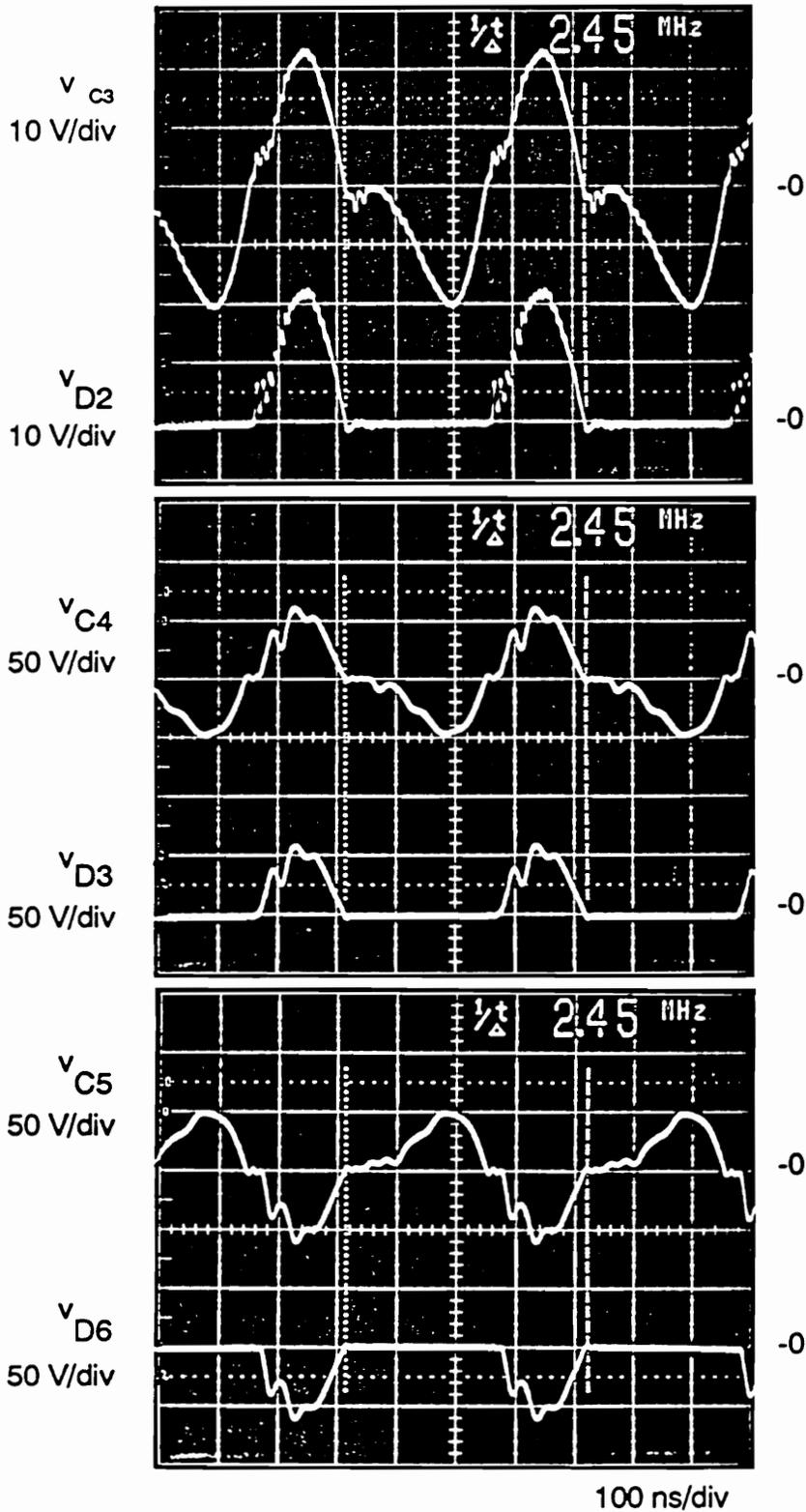
**Figure 6.20.** Secondary waveforms in multiple-output converter: $V_{IN} =$ 50 V. All outputs fully loaded.

## 6.4.2. Crossregulation

As in any converter with multiple outputs, the cross-regulated output voltage is affected by variations of the load current of the main output. In the experimental converter, there is a high degree of symmetry between the +12 V and -12 V outputs, due to symmetrical design of the transformer and filter inductor. The difference in output voltage for these two outputs with identical load resistances is usually less than 100 mV. Therefore, cross-regulation characteristics are presented here for the +12 V output only.

Figure 6.21(a) shows voltage Vo(+12) measured at the +12 V output, as a function of input voltage and +5 V load current. The cross-regulated output voltage is not strongly dependent on the input voltage. However, as the 5 V output current decreases, the cross-regulated output voltage also decreases. This can be seen in Fig. 6.21(b), which shows output voltage Vo(+12) as a function of the +5 V load current and +12 V load resistance. If the load range of the main output is limited to 20-100% and the load range of the cross-regulated output is 10-100% (shaded area in Fig. 6.21), the cross-regulated output voltage Vo(+12) is maintained at 12 V $\pm$1 V ($\pm$8% tolerance).

The cross regulation is significantly affected by the selection of the rectifiers. The rectifier's resistance is responsible for variations of the cross-regulated output voltage in response to a change in load current. In general, reduction of the rectifier's resistance (*i.e.*, increase of the die size) results in improved cross regulation. This is also the case in a MRC with **non-coupled** inductors. However, in a MRC with **coupled** inductors, an increase in the die
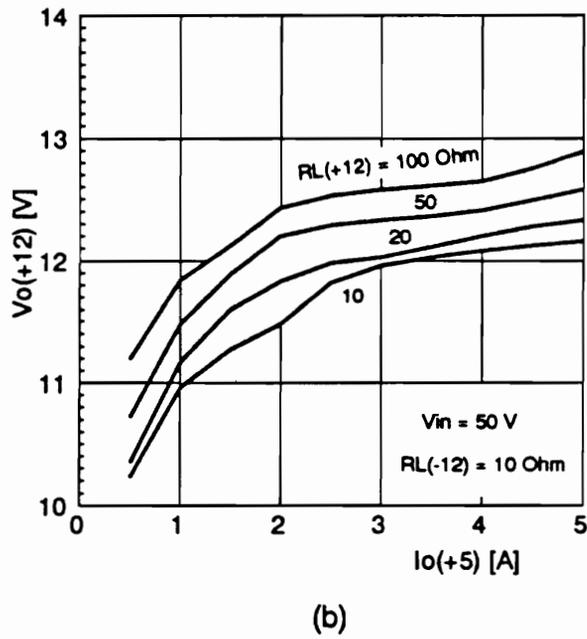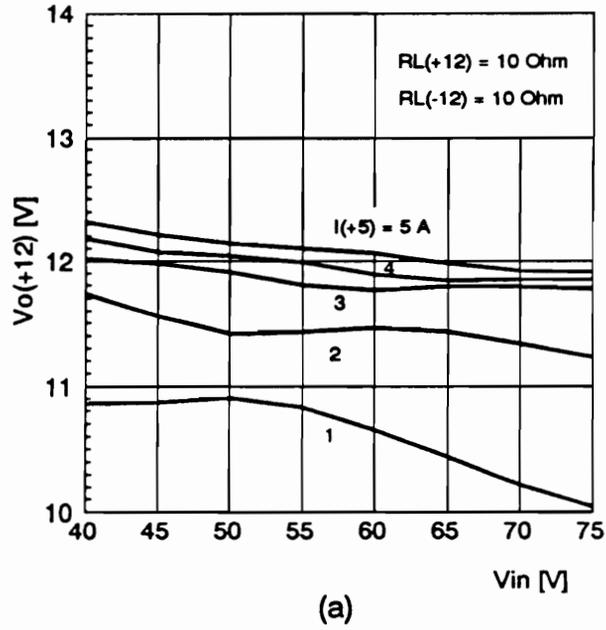
**Figure 6.21.** Cross-regulated output voltage: (a) As function of input voltage. (b) As function of main output current.
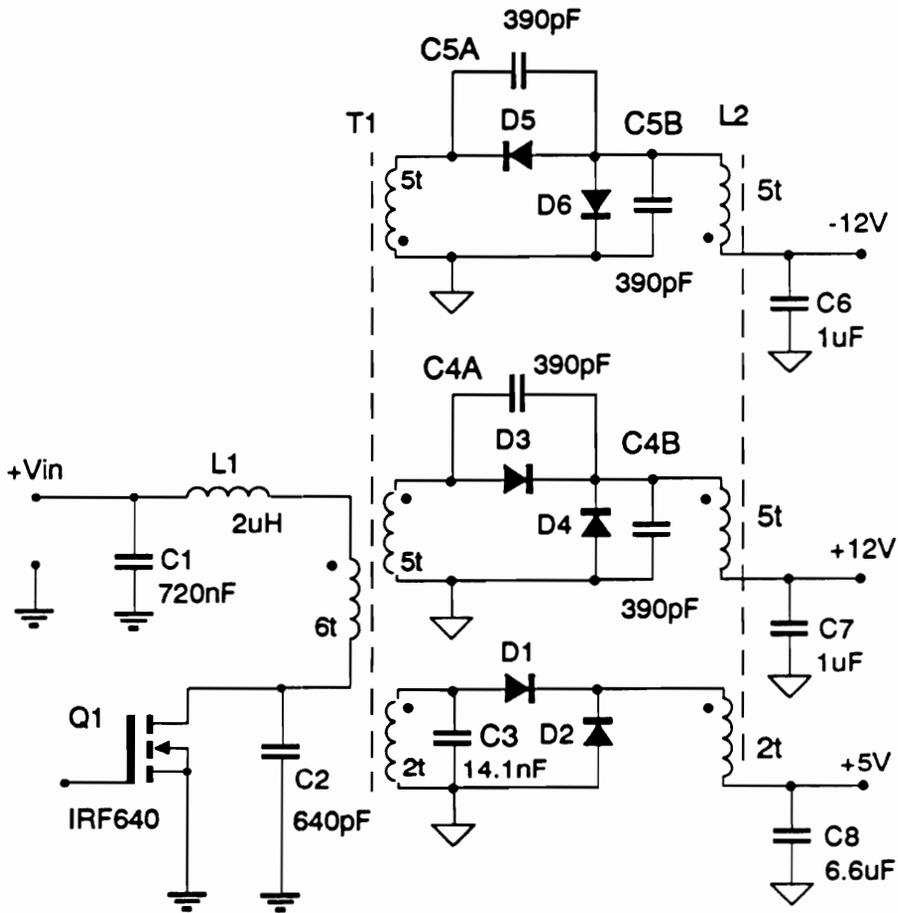
**Figure 6.22.** **Power stage of multiple-output converter with rearranged resonant capacitors on the secondary side.**
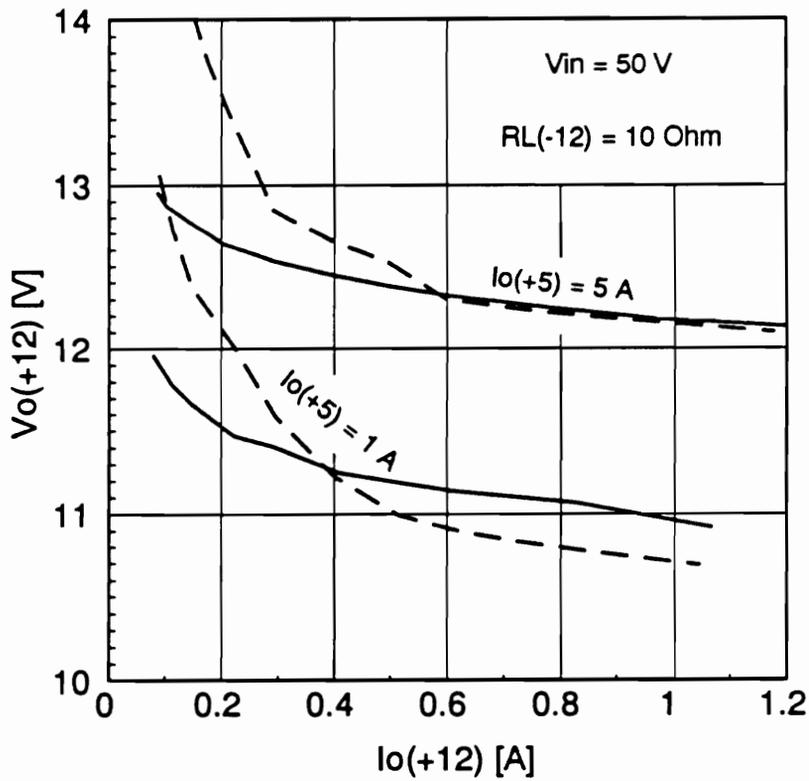
**Figure 6.23.** Cross-regulated output voltage as function of the +12 V load current: Dashed lines are for resonant capacitors placed across rectifying diodes (Fig. 6.17); solid lines are for resonant capacitors across transformer (Fig. 6.22).

size, and consequently, higher value of the junction capacitance, causes deterioration of the cross regulation. This is verified experimentally by rearranging the resonant network as shown in Fig. 6.22. To simulate increased capacitance associated with the rectifiers, resonant capacitors C4 and C5 (see Fig. 6.17) are removed from the circuit and each is replaced by two capacitors of identical value placed in parallel with rectifiers D3-D6 (capacitors C4A, C4B, C5A, and C5B in Fig. 6.22). (As explained in Chapter 5, such a rearrangement does not affect the resonant circuit's parameters.)

Figure 6.23 shows the cross-regulated output voltage, Vo(+12), as a function of the +12 V output current. Solid lines represent results obtained in circuit of Fig. 6.17, while dashed lines correspond to the circuit of Fig. 6.22. The circuit with the higher rectifier capacitance suffers worse cross-regulation. A similar result is obtained when D3-D6 are replaced by larger rectifiers with higher junction capacitances. Therefore, to improve cross-regulation, junction capacitance of the rectifiers should be minimized. However, when reduction of junction capacitance is achieved by using die with a smaller area, diode resistance is increased. Therefore, a trade-off exists in selecting the size of the rectifier. More precise analysis of this phenomenon remains to be performed.

## 6.5. Summary

A successful implementation of high-density, single- and multiple-output MRCs is presented. Each converter is designed to fit into a 2×2×0.25 in³ package, for overall power density of 50 W/in³. Switching frequency range is 2.5 to 4 MHz. The single-output converter operates from 45-55 V input and provides 5 V @ 10 A. An efficiency of 83% is achieved at full load and nominal line for the complete converter including gate-drive, control, and self-bias.

The multiple-output converter has three outputs: +5 V @ 5 A, +12 @ 1.2 A, and -12 V @ 1.2 A. Closed-loop regulation is used for the 5 V output, while the ±12 V outputs are cross-regulated with ±8% tolerance for a load range of 20-100% on the main output and 10-100% on the cross-regulated outputs. A coupled-inductor design is used for all outputs to reduce the size of the filter and improve dynamic cross-regulation.

Based on these examples of single- and multiple-output converters, it is concluded that the multi-resonant technique is a promising technology for high-density on-board converters. It is feasible to develop a family of converters with various input voltages and different number of outputs. The forward ZVS-MRC is very forgiving of circuit parasitics and allow high operating frequencies without requiring exotic devices, components, or layout techniques.

# 7. HIGH FREQUENCY SYNCHRONOUS RECTIFICATION

One of the major factors limiting the efficiency of low-voltage dc/dc converters is the conduction loss in the output rectifiers. Even Schottky rectifiers have too high conduction losses for applications requiring extremely high efficiency (*e.g.* 90% at 5 V output). To reduce rectification losses, power MOSFETs could be used as synchronous rectifiers [R1-R5]. However, at high switching frequencies, gate-drive losses offset the reduction of conduction losses, yielding the synchronous rectifier impractical. This chapter provides insight into limitations of various synchronous rectification schemes. The quantitative analysis is performed for a 50 W converter with a 5 V output.

## 7.1. Frequency Limitations of PWM Synchronous Rectifiers

In PWM circuits operating at lower switching frequencies, power dissipation in a MOSFET synchronous rectifier is determined mainly by conduction losses. However, at higher switching frequencies, power dissipation is dominated by power loss in the gate drive circuit caused by abrupt charging and discharging of the MOSFET parasitic capacitances. An additional problem with synchronous rectifiers at higher switching frequencies is the precise control requirement. In most converter topologies, synchronous rectifiers should never be allowed to turn on simultaneously, lest a short circuit condition be created. A dead time is usually introduced in the drive signals to avoid cross-conduction; however, to avoid a reverse recovery problem, the dead time must be sufficiently short to prevent the parasitic body diode from turning on. As a result, the efficiency of the rectifier is very sensitive to the gate drive dead time [R5]. Indeed, newer designs using synchronous rectifiers at switching frequencies as high as 1 MHz suffer from gate-drive circuit complexity [R7, R18] and gate-drive power dissipation [R19]. In general, the major obstacle in applying the synchronous rectifier at frequencies above 1 MHz is the lack of a simple means to implement efficient and reliable gate drive circuitry.

To determine losses in a PWM synchronous rectifier, the asymmetrical rectifier configuration shown in Fig. 7.1(a) is considered. This type of rectifier is commonly used in single-ended converters. In push-pull or half-bridge con-

verters, a symmetrical rectifier is used, with the load connected to the center tap on the power transformer. The loss analysis for the asymmetrical configuration is also valid for the symmetrical arrangement, assuming square waveforms with 50% duty ratio.

The circuit of Fig. 7.1(a) can be represented by a simplified model shown in Fig. 7.1(b). Current source, $I_O$, represents the output filter and load, assuming the current ripple in $L_f$ is negligible. Voltage source, $V_{sq}$, represents the square-wave voltage applied to the rectifier through the power transformer. It is assumed that the leakage inductance of the transformer is negligible.

Waveforms corresponding to Fig. 7.1(b) are shown in Fig. 7.1(c). In the analysis a 50% duty ratio is assumed. The secondary voltage is a symmetrical square wave with amplitude of $2V_O$. The inter-electrode voltage waveforms are shown for device Q1. Waveforms of device Q2 are identical, but shifted by 180°. The gate-to-source voltage varies between zero and $V_{gson}$, with zero rise and fall time. Such a waveform implies an idealized gate drive circuit with an infinite sourcing and sinking current capability. In practice, the current capability of any gate drive is limited, resulting in switching loss in the drain circuit due to overlap of the drain voltage and current. This switching loss is strongly dependent on the current capability of the driver. In the following analysis it is assumed that the gate-drive is ideal, *i.e.*,

1.  there is no drain voltage/current overlap,

2.  the gate drive voltage is perfectly synchronized with the input voltage, $V_{sq}$, so that the body diode is never allowed to conduct, and
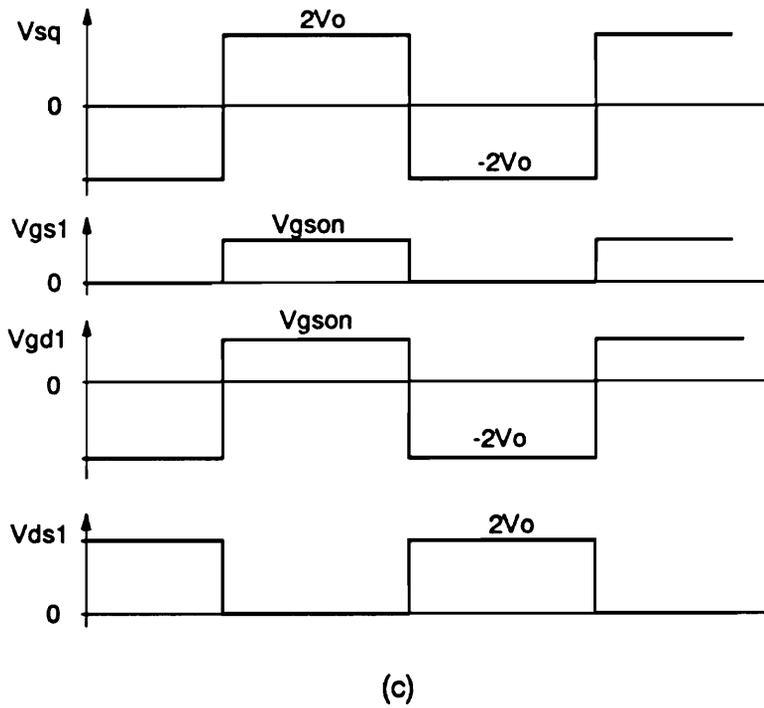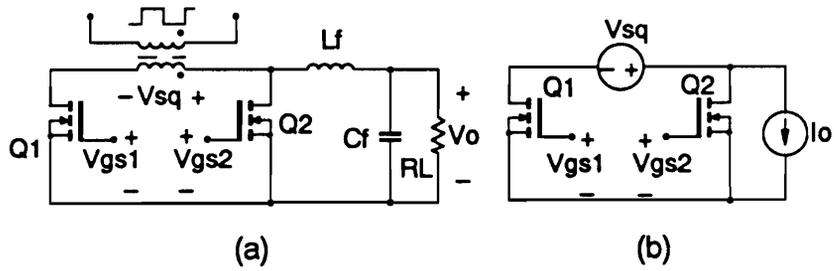
Figure 7.1.  Square-wave synchronous rectifier:   (a) Typical circuit.  (b) Equivalent circuit.  (c) Idealized waveforms.

3. $V_{gs1}$ and $V_{gs2}$ are shifted exactly by 180°, so that there is no cross-conduction of Q1 and Q2.

It should be noted that implementation of a gate drive with such ideal characteristics at megahertz frequencies would be impossible, thus the efficiencies calculated in this analysis represent the most optimistic case.

With the assumption of an ideal gate drive, losses in the rectifier comprise two components: conduction losses due to the load current flowing through the on-resistances of Q1 and Q2, and the switching losses due to charging and discharging of the MOSFET capacitances. The total conduction loss in Q1 and Q2 is:

$$P_{cond} = I_o^2 R_{ds} \quad , \tag{7.1}$$

where $R_{ds}$ is the on-resistance of the MOSFET at a given $V_{gs}$.

The energy lost during each switching cycle in each capacitance is:

$$E = [V_{max} - V_{min}] \int_{V_{min}}^{V_{max}} C(v) dv \quad . \tag{7.2}$$

The total switching power losses for the two devices, Q1 and Q2, due to their gate-to-source capacitances, is:

$$P_{gs} = 2f C_{gs} V_{gson}^2 \quad , \tag{7.3}$$

where f is the switching frequency. The total loss due to $C_{gd}$ is

$$P_{gd} = 2f[V_{gson} + 2V_o] \int_{-2V_o}^{V_{gson}} C_{gd}(v)dv = P_{gdp} + P_{gdn} \quad , \tag{7.4}$$

where

$$P_{gdp} = 2f[V_{gson} + 2V_o] \int_{0}^{V_{gson}} C_{gdp}(v)dv \quad , \tag{7.5}$$

$$P_{gdn} = 2f[V_{gson} + 2V_o] \int_{-2V_o}^{0} C_{gdn}(v)dv \quad . \tag{7.6}$$

The total loss due to $C_{ds}$ is:

$$P_{ds} = 4fV_o \int_{0}^{2V_{ds}} C_{ds}(v)dv \quad . \tag{7.7}$$

The total power loss in the rectifier is:

$$P_{PWM} = P_{cond} + P_{gs} + P_{gd} + P_{ds} \quad , \tag{7.8}$$

and the rectification efficiency is:

$$\eta_{PWM} = \frac{P_o}{P_o + P_{PWM}} \quad , \tag{7.9}$$

where $P_O = I_O V_O$ is the output power.

To minimize the conduction losses, given by (7.1), it is necessary to reduce the on-resistance, $R_{ds}$. This can be achieved by increasing the gate-drive voltage, $V_{gson}$. However, increased $V_{gson}$ results in increased switching losses given by (7.3) and (7.4). Therefore, a trade-off exists between the conduction and switching losses. To find an optimum value of $V_{gson}$, the total losses are calculated for various values of $V_{gson}$. (The on-resistance as a function of $V_{gs}$ is given in Appendix E, Table E.1.)

A MATHCAD program used to perform the calculations is listed in Appendix F. The numerically calculated efficiency curves are shown in Fig. 7.2(a). At lower frequencies, efficiency always improves as $V_{gson}$ is increased. However, as the frequency increases, gate drive losses quickly offset any reductions in conduction losses. As a result, the optimum value of $V_{gson}$ is relatively low for frequencies in the megahertz range. For example, at frequencies from 4 to 10 MHz, the highest efficiency occurs at $V_{gson} = 5$ V.

Another way to reduce conduction losses is to parallel two or more devices (or use a larger die area). Figure 7.2(b) shows total losses for a PWM synchronous rectifier where Q1 and Q2 are both implemented using two MOSFETs in parallel, resulting in halved on-resistance and doubled device capacitances. In this arrangement, efficiency is improved at low frequencies, but reduced at higher frequencies. At frequencies in excess of 2.5 MHz, the optimum value of $V_{gson}$ is 4 V. If this optimization process is continued, the maximum attainable efficiency can be determined as a function of the number of paralleled devices, n. The result is as shown in Fig. 7.3 for n = 1 through 5.
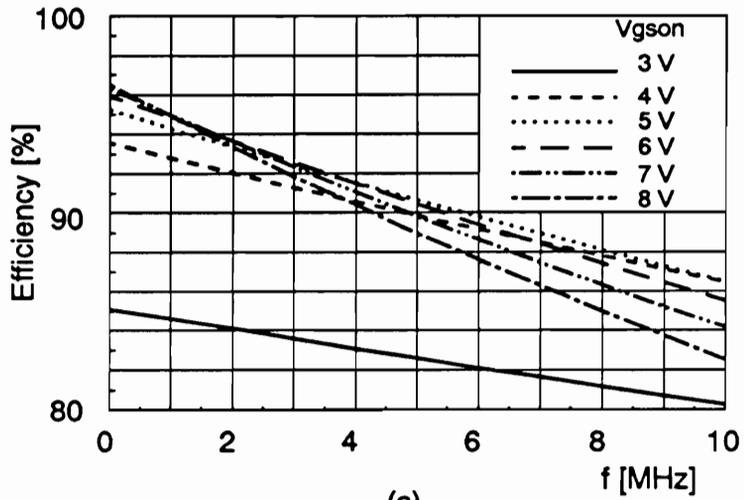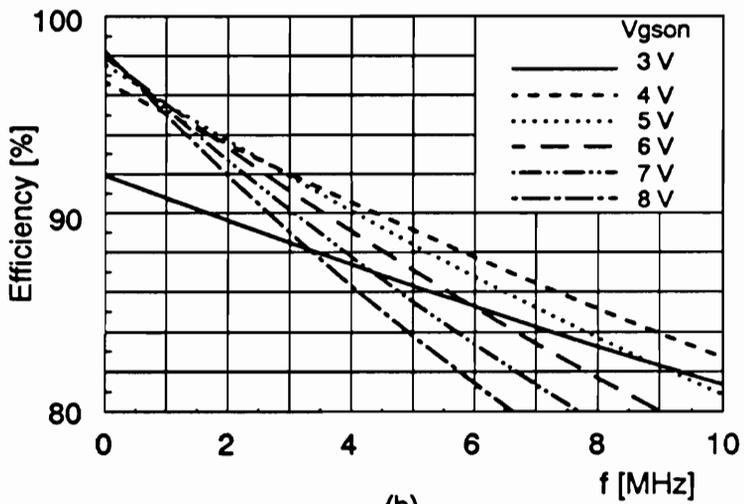
**Figure 7.2.** Efficiency of square-wave synchronous rectifier: (a) For n=1 (each synchronous rectifier uses one MOSFET device). (b) For n=2 (each synchronous rectifier device uses two paralled MOSFETs).

Since a Schottky rectifier using a 60CNQ030 Schottky diode can provide effi-
ciency of approximately 93%, the PWM synchronous rectifier offers a signif-
icant efficiency improvement only up to approximately 1 MHz.

# 7.2. Resonant Synchronous Rectifier

The resonant synchronous rectifier is an attempt to avoid the gate-drive
losses associated with charging and discharging of the parasitic inter-
electrode capacitances of the semiconductor devices, by using these parasitic
capacitances as part of the resonant circuit.

### 7.2.1. Concept of Resonant Synchronous Rectification

One method commonly used to simplify the gate drive is use of auxiliary
windings on the power transformer connected between the gate and source
of the MOSFET [R7]. An even simpler way to use the power circuit waveforms
to drive the rectifiers is to interconnect the devices so that the gate-to-source
voltage of one device is the same as the drain-to-source voltage of the other
[R8]. Figure 7.4 shows such an arrangement for an asymmetrical (half-wave)
rectifier. A symmetrical (full-wave) rectifier can be realized by taking the output
current from a center tap on the transformer.
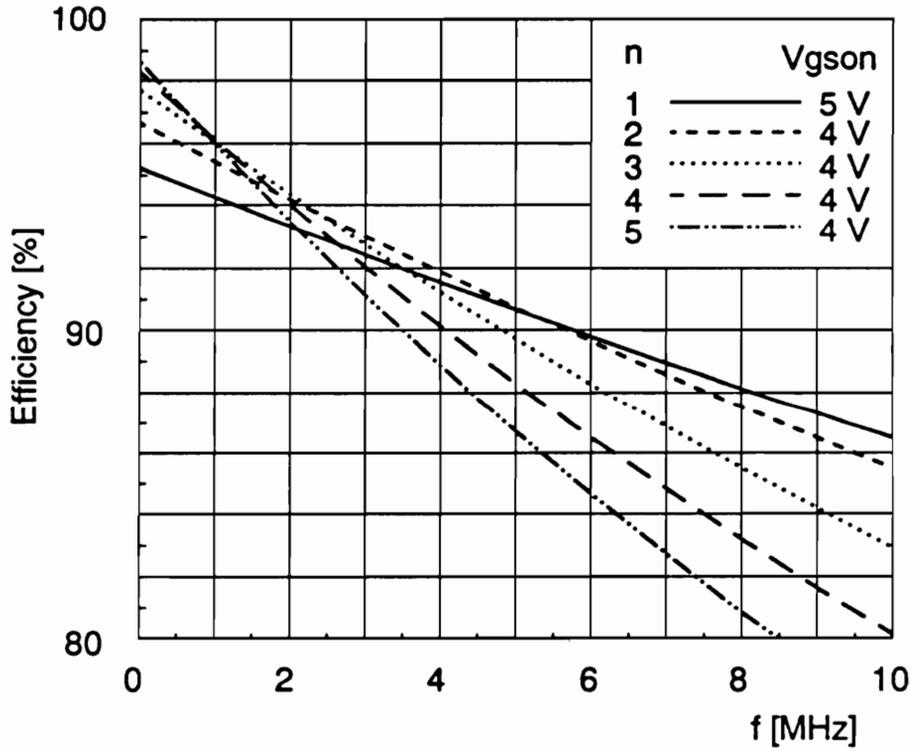
**Figure 7.3. Efficiency attainable in square-wave synchronous rectifier: Parameter n represents the number of paralleled MOSFETs.**
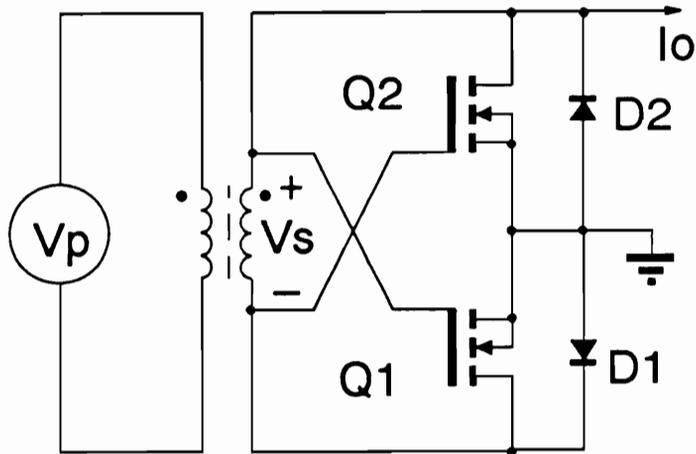
**Figure 7.4.** Interconnection of two MOSFETs to allow gate control by the power circuit.

When the secondary voltage, $v_S$, is positive, the output current flows initially through diode D1. As a result, $v_{GS}$ of Q2 is close to zero and Q2 is off and blocks the positive secondary voltage. At the same time, gate of Q1 is charged to $v_S$, and Q1 turns on. When $v_S$ is negative, the situation is opposite, *i.e.*, $v_S$ is blocked by Q1/D1, and Io flows through D2/Q2.

If used in a PWM circuit, this scheme does nothing to solve the major problem of gate drive loss; the MOSFET capacitances are still abruptly charged and discharged, resulting in a $CV^2$-type energy loss. The only advantage is the simplification of the drive circuit. However, if the circuit of Fig. 7.4 is used in conjunction with a resonant topology, gate-drive losses can be significantly reduced. If the parasitic capacitances of the MOSFET rectifiers are effectively connected in parallel with a resonant capacitor, it is possible to recover the energy stored in these capacitances. Such a solution has been proposed for the dual forward resonant converter [F3]. Other topologies that are suitable for such an application include the series-parallel converter [R5], half-bridge and forward MRCs, and Class E converters. For example, Fig. 7.5(a) shows the forward ZVS-MRC with a diode rectifier. Figure 7.5(b) shows the same topology with a resonant synchronous rectifier, and typical waveforms at 5 V; 10 A output are shown in Fig. 7.5(c). The secondary voltage waveform across the resonant capacitor $C_d$ is very close to a sine wave. It can be also seen from Fig. 7.5(b) that *all* the parasitic capacitances of the MOSFETs are effectively in parallel with the resonant capacitor $C_d$. The gate-to-drain capacitances of both devices are directly connected across $C_d$, while the gate-to-source and drain-to-source capacitances are connected in parallel with $C_d$
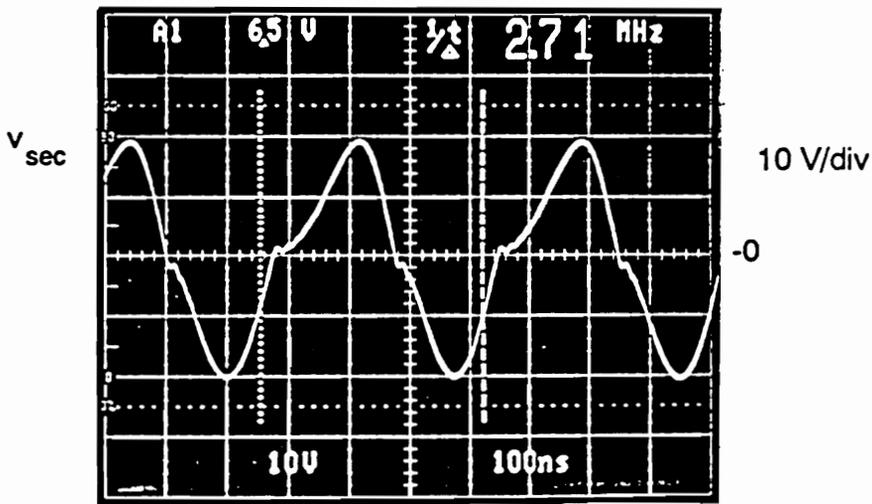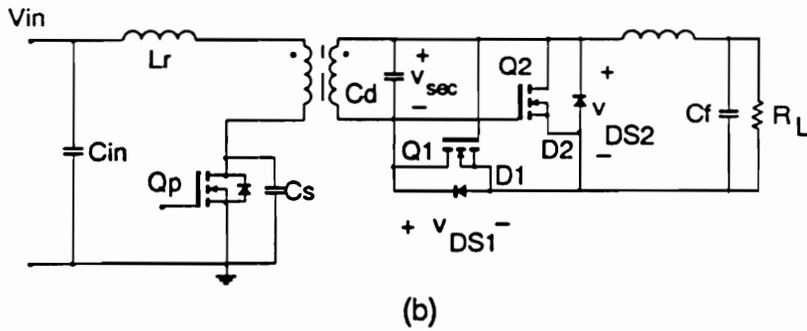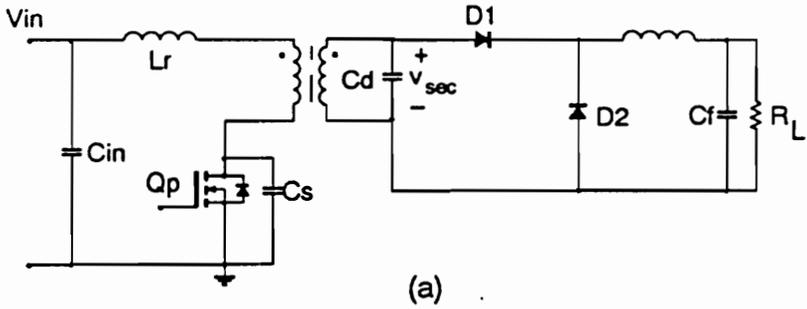
Figure 7.5. Forward ZVS-MRC: (a) With diode rectifier. (b) With MOSFET resonant synchronous rectifier. (c) Typical waveforms at 5 V, 10 A output and 50 V input.

through a conducting rectifier for one half of the switching cycle, and are shorted for the other half. As a result, the equivalent resonant capacitance is $C_d + 2C_{gd} + C_{gs} + C_{ds}$.

Since the parasitic capacitances are absorbed by the resonant circuit, the gate can be charged and discharged in a resonant fashion, without the gate-drive losses encountered in square-wave drivers. However, the circulating currents flowing through the parasitic capacitances will cause power dissipation in the parasitic resistances, particularly the gate resistance.

Figure 7.6 shows an equivalent circuit diagram of the resonant synchronous rectifier of Fig. 7.5(b). The output filter and load are modeled by the current source, Io. The secondary voltage is modeled as an ideal sine wave voltage source with amplitude $\pi V_O$ (resulting in an average voltage $V_O$ across current source $I_O$). This equivalent model is also valid for other resonant converter topologies, provided the resonant voltage applied to the rectifier is approximately sinusoidal.

## 7.2.2. Model of the Resonant Synchronous Rectifier Device

At any switching frequency, efficiency of the rectifier can be maximized by using an optimum size MOSFET die. As in the case of the PWM rectifier, variations in the die size are modeled by connecting n devices in parallel, as shown in Fig. 7.7(a). Figure 7.7(b) shows a model of the MOSFET/diode device used in the loss analysis. The diode is replaced with the model of Fig. E.1
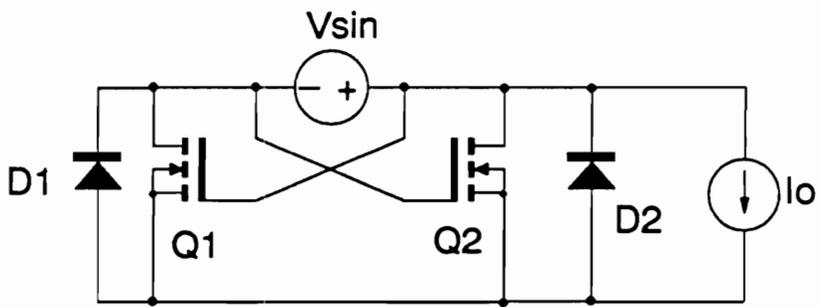
**Figure 7.6.   Equivalent circuit of the resonant synchronous rectifier.**
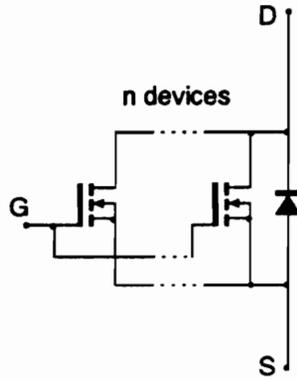
(a)
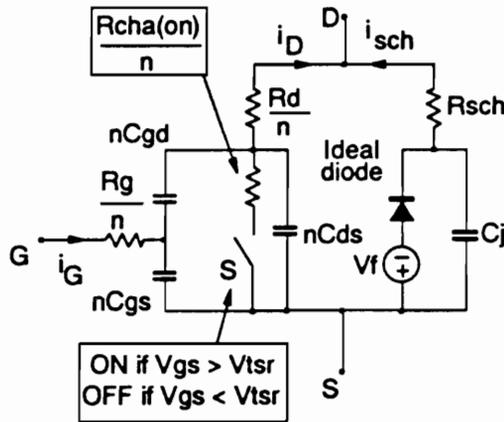


(b)

**Figure 7.7.** Model of the resonant synchronous rectifier device: (a) Rectifier comprising n MOSFETs and a diode. (b) Model of the rectifier.

(Appendix E). MOSFET devices are replaced with a model using an ideal voltage-controlled switch, S, equivalent MOSFET resistances, and nonlinear interelecterode capacitances. (See Appendix E for details on the MOSFET model and its parameters.) The use of an ideal switch in this model greatly simplifies the analysis.

The key parameter associated with the use of an ideal switch in the resonant synchronous rectifier model is the threshold voltage, $V_{tsr}$, at which the switch is turned on. To determine the value of $V_{tsr}$, the circuit shown in Fig. 7.8(a) is considered. When the device of Fig. 7.7(a) conducts the load current, the current sharing between the MOSFET(s) and the Schottky diode, and the forward voltage drop, are controlled by the gate-to-source voltage applied to the MOSFET device. This process is illustrated in Fig. 7.8(b), which shows the device i-v characteristics. The Schottky diode is represented by the forward voltage drop $V_f$, an ideal diode, and resistance $R_{sch}$. The MOSFET is modeled as a voltage-controlled resistance $R_{ds}$. (See Appendix E for relation between $R_{ds}$ and $V_{gs}$ in a single MOSFET.) The value of $R_{ds}$ depends on the number of paralleled devices, n, and the gate-to-source voltage. Waveforms of the MOSFET/diode rectifier device during conduction period are shown in Fig. 7.9. The solid waveforms correspond to the device model of Fig. 7.8(a), while the dotted waveforms indicate the simplified model of Fig. 7.7(b). When $V_{gs}$ is less than the MOSFET threshold voltage, $V_t$, $G_{ds}$ is zero and the output current flows through the diode, resulting in a voltage drop $I_o R_{sch} + V_f$. At $t = t_1$, $V_{gs}$ exceeds $V_t$ and the MOSFET gradually turns on. As $R_{ds}$ is reduced, current $i_d$ flowing through the MOSFET increases, while the Schottky current, $i_{sch}$, decreases.
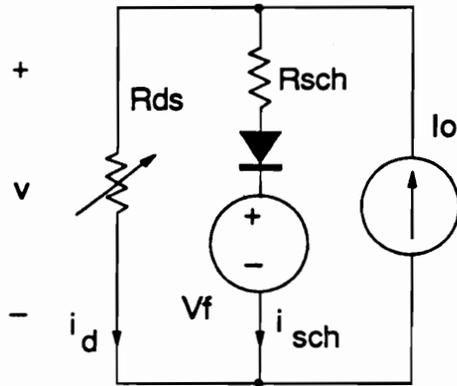
(a)
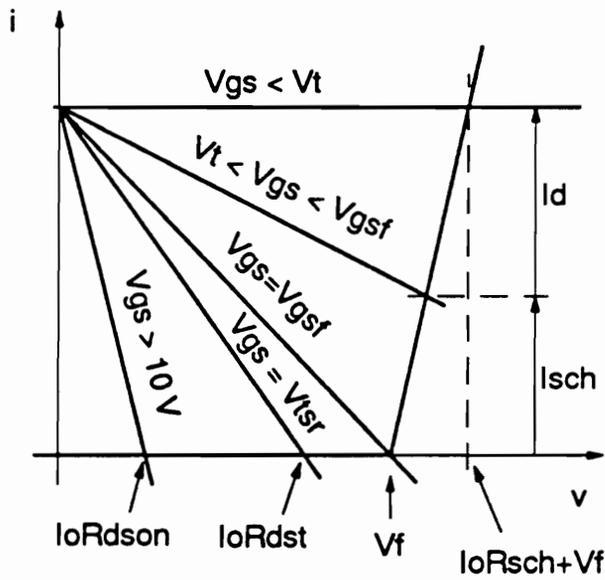


(b)

**Figure 7.8.  Model of the MOSFET/diode device during conduction:  (a) Equivalent circuit.  (b) Definition of the threshold voltage $V_{tsr}$ on the devices' i-v characteristics.**

The current sharing is governed by the device characteristics, as shown in Fig. 7.8(b). At $t = t_2$, $R_{ds}$ is sufficiently low to completely divert the load current into the MOSFET, and the Schottky diode turns off. Subsequently, the voltage drop decreases as the MOSFET resistance decreases. At $t_4$, $V_{gs}$ reaches $V_{gson} = 10$ V, and the MOSFET is fully turned on.

In the model shown in Fig. 7.7(b), the continuously varying channel and accumulation layer resistance $R_{cha}$ is replaced with a constant resistance, $R_{cha(on)}$, equal to $R_{cha}$ at $V_{gs} = 10$ V (2.5 m$\Omega$), and the voltage controlled switch, S. The switch is off until $V_{gs} < V_{tsr}$ and is fully on when $V_{gs} > V_{tsr}$, where $V_{tsr}$ is the threshold voltage defined for the resonant synchronous rectifier device. At $V_{gs} = V_{tsr}$ the voltage drop across the rectifier is

$$V_{dst} = \frac{V_f + I_o R_{sch} + I_o(R_{dson}/n)}{2} \quad , \tag{7.10}$$

which is halfway between the values corresponding to the fully on and fully off states of the MOSFET device. The device model of Fig. 7.7(b) is designed to approximate the conduction loss in the rectifier (MOSFET and diode combined) by replacing the continuous waveforms in Fig. 7.9 (solid lines) with the abruptly switched waveforms (dashed lines).

Performing an analysis of the circuit of Fig. 7.8(a) it can be determined that for $V_{dst} \leq V_f$,

$$G_{dst} = \frac{1}{n}\left[\frac{2I_o}{V_f + I_o R_{sch} + I_o(R_{ds}/n)}\right] \tag{7.11}$$
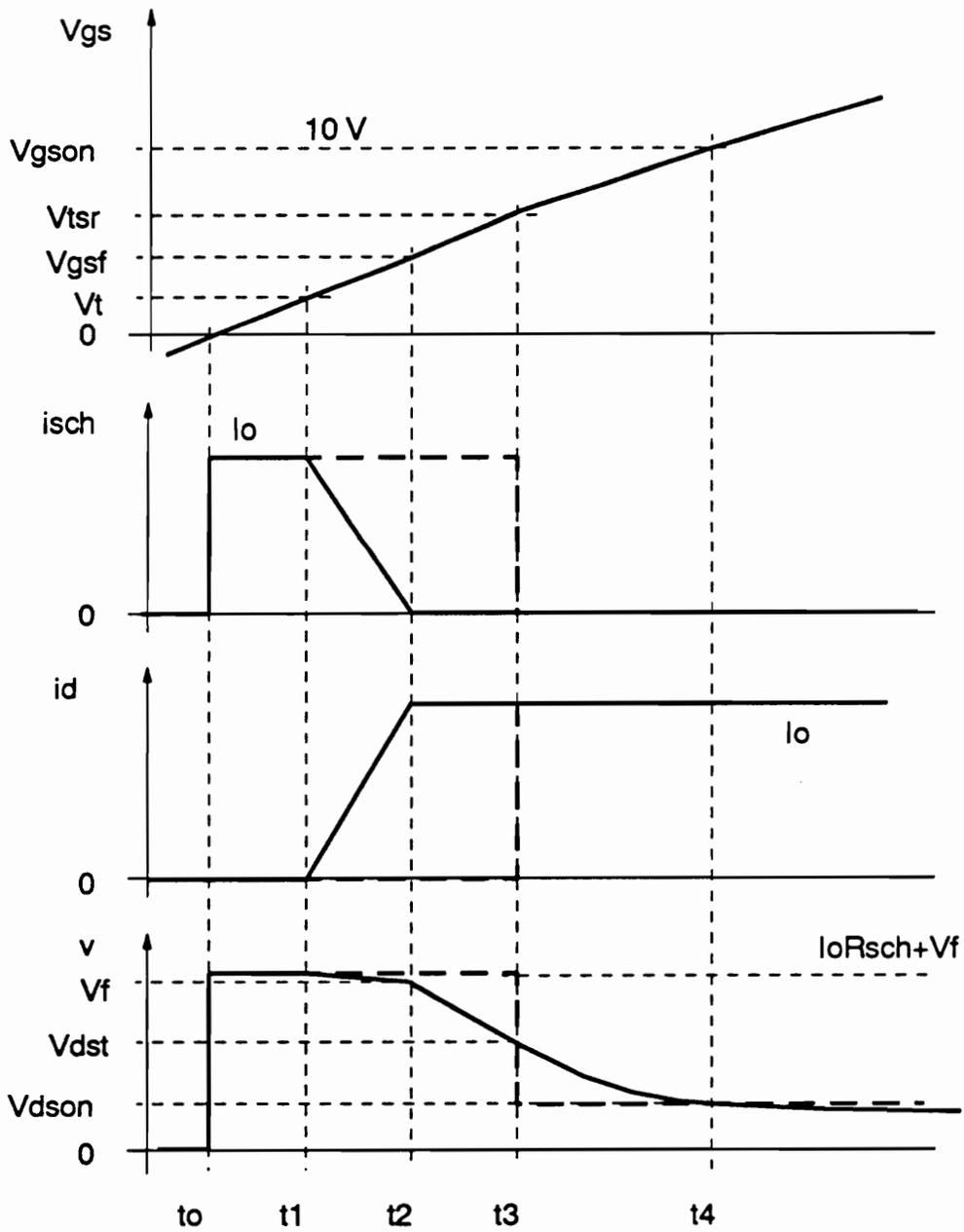
**Figure 7.9.    Diode and MOSFET waveforms during conduction of the output current:    Dotted lines show waveforms corresponding to the model used in the analysis.**
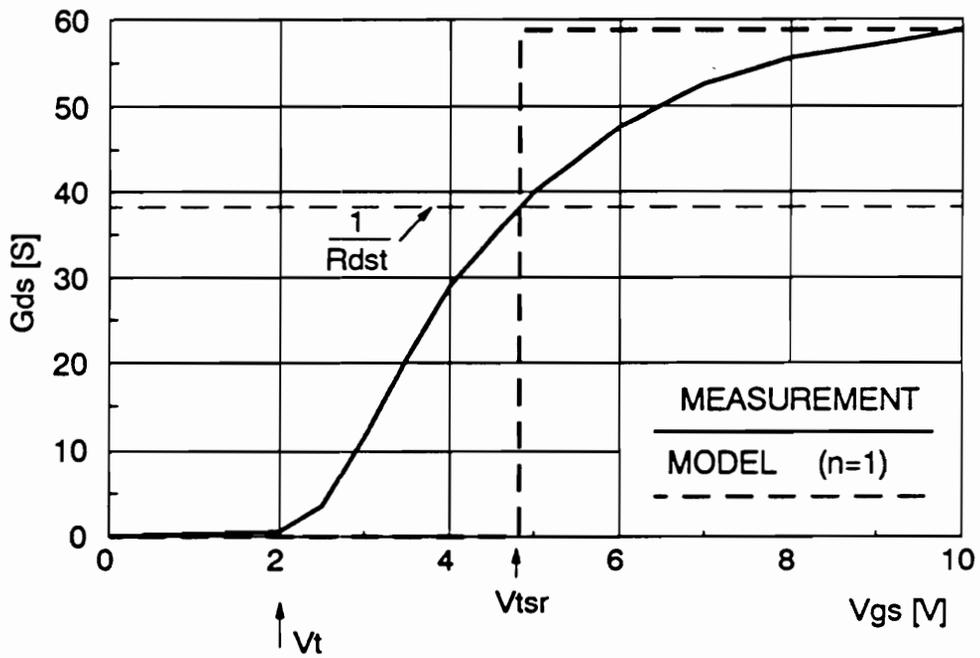
**Figure 7.10.   MOSFET conductance as a function of the gate-to-source voltage.**

is the conductance of the MOSFET device necessary to make the conduction drop equal to $V_{dst}$. Characteristics of $G_{ds} = 1/R_{ds}$ for n = 1 are shown in Fig. 7.10. The solid line indicates measurements from Table D.1, while the dotted line corresponds to the model of Fig. 7.7(b). To determine $V_{tsr}$, MOSFET conductance characteristic of Fig. 7.10 is used. Values of $V_{tsr}$ for n = 1 through 5 are listed in Table 7.1.

### 7.2.3. Operation of the Resonant Synchronous Rectifier

Figure 7.11(a) shows a circuit resulting from replacing the MOSFETs and diodes in Fig. 7.6 with the model of Fig. 7.7(b). As Q1 and Q2 turn on and off, four equivalent circuits are formed, shown in Figs. 7.11(b)-(e). Typical waveforms are shown in Fig. 7.12. (These waveforms are generated using a MATHCAD program given in Appendix F.)

During period $[t_0, t_1]$, the equivalent circuit is shown in Fig. 7.11(b). $V_{sin}$ is positive, and diode D1 is conducting the load current and the currents circulating through $C_{gs}$ of Q1, $C_{ds}$ of Q2, and $C_j$ of D2. Circulating currents also flow through drain resistance of Q2 and resistance of diode D2. Due to conduction of D1, $V_{gs}$ of Q2 is essentially zero; thus Q2 is off, and its drain-to-source voltage is equal to $V_{sin}$. The same voltage is also applied directly between the gate and source of Q1. However, Q1 remains off since $V_{sin} < V_{tsr}$. Capacitances $C_{ds}$ of Q1 and $C_{gs}$ of Q2 effectively disappear from the circuit since they are shorted by conducting D1.

**Table 7.1.  Threshold voltage for different numbers of paralleled devices.**

| n | $G_{dst}$ | $V_{tsr}$ |
|---|---|---|
|   | [S] | [V] |
| 1 | 37.74 | 4.80 |
| 2 | 22.74 | 3.60 |
| 3 | 16.00 | 3.25 |
| 4 | 12.42 | 3.10 |
| 5 | 10.15 | 2.90 |
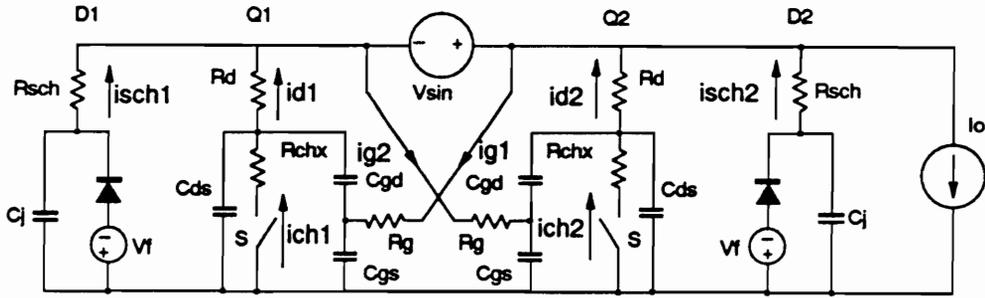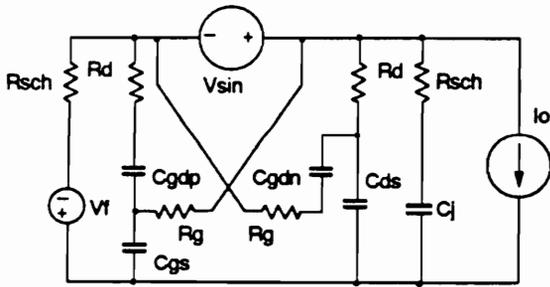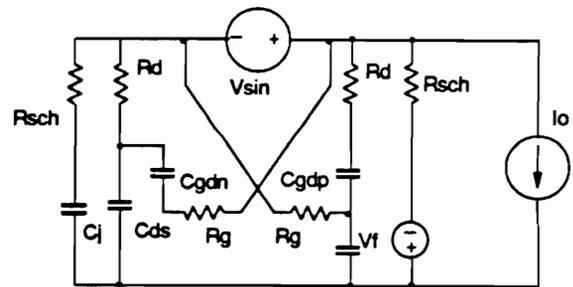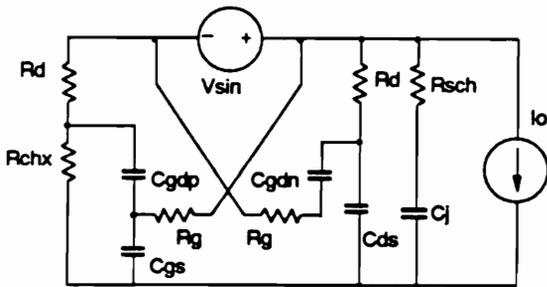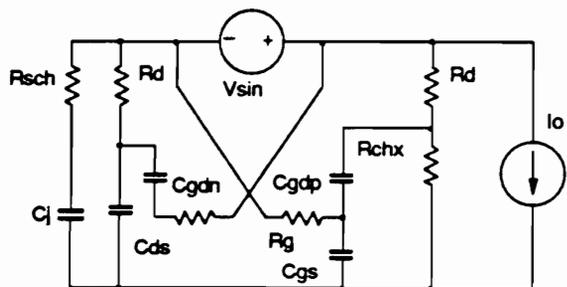
Figure 7.11. Model of the resonant synchronous rectifier (n=1): (a) Complete circuit model. (b)-(e) Topological stages.
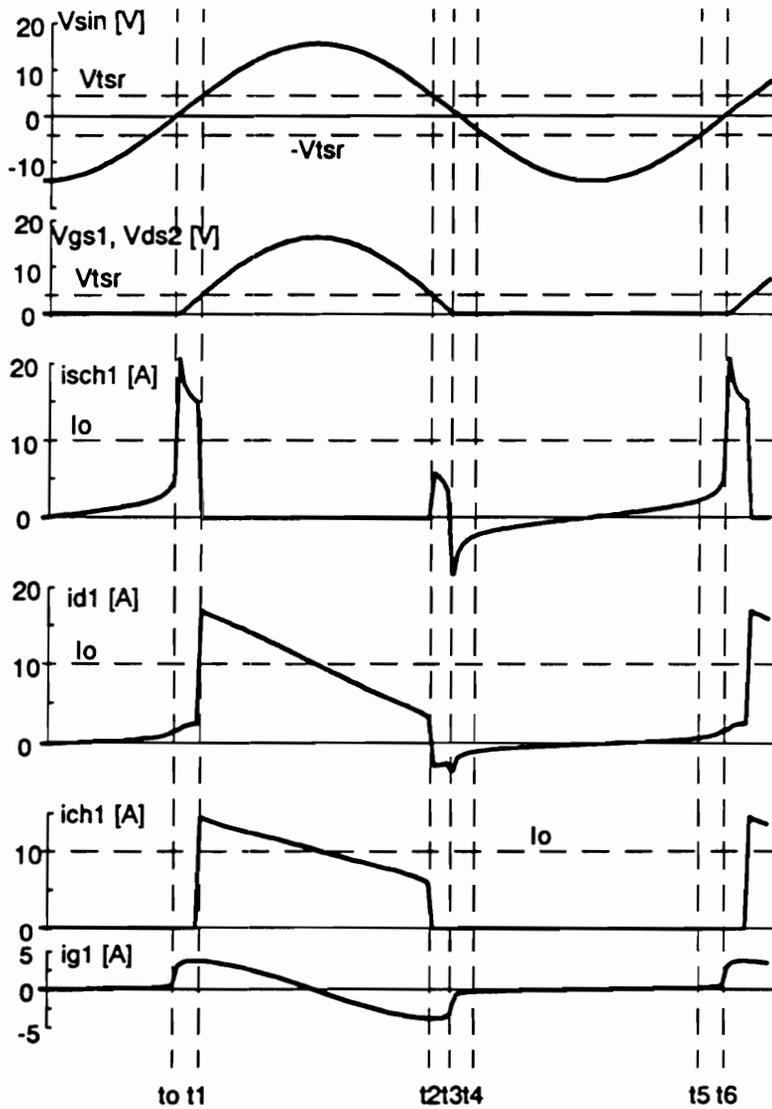
**Figure 7.12.** Waveforms of the resonant synchronous rectifier: $n=2$, $f=7$ MHz, $I_O = 10$ A, and $V_O = 5$ V.

At $t = t_1$, $V_{sin}$ exceeds $V_{tsr}$, Q1 turns on, and D1 turns off. The equivalent circuit is shown in Fig. 7.11(c). The load current and the circulating currents flow through Q1 until $V_{sin}$ falls below $V_{tsr}$ at t=t2, when Q1 turns off. The circuit then returns to the topology of Fig. 7.11(b), and the load and the circulating currents flow through D1.

At $t = t_3$, load current is switched from D1 into D2. Operation during period $[t_3,t_6]$ is similar to that during $[t_0,t_3]$, but the load current is conducted by D2 and Q2. The equivalent circuit corresponding to periods $[t_3,t_4]$ and $[t_5,t_6]$ is shown in Fig. 7.11(d), and the equivalent circuit for $[t_4,t_5]$ is shown in Fig. 7.11(e).

The waveforms shown in Fig. 7.12 are calculated for n=2 and f=7 MHz. (It is shown in Section 7.2.4 that n = 2 is an optimum for f = 7MHz, see Fig. 7.13.) It can be seen, from Fig. 7.12, that amplitudes of the circulating currents are of the same order of magnitude as the load current, resulting in substantial rms currents. In addition, at the beginning of the conduction period, the current flowing through the rectifier is higher than $I_o$, while at the end of the conduction period, this current is lower than $I_o$. It can be determined, using (7.11) and Fig. 7.10, that the value of the threshold voltage $V_{tsr}$ should be at $t_1$ higher, and at $t_2$ lower than that calculated for a constant current, equal to $I_o$. As a result, the diode will conduct for a longer time at the beginning of the conduction period (increasing the conduction loss) and for a shorter time at the end of the conduction period (decreasing the conduction loss). In the following loss analysis, it is assumed that these two effects compensate each other, and

$V_{tsr}$ is assumed constant and is determined based on the value of the load current $I_O$.

An important feature of the resonant synchronous rectifier circuit is that during the zero-transition of $V_{sin}$ both MOSFETs are off, and switching of the load current is performed by the Schottky diodes. This automatically prevents the body diodes of Q1 and Q2 from conducting. But overall, most of the load current is conducted by the MOSFET devices. Therefore, the resonant synchronous rectifier configuration successfully combines the simple and fast switching action of Schottky diodes with the low conduction loss of the MOSFET device.

### 7.2.4. Loss Analysis of a Resonant Synchronous Rectifier

To find the currents flowing through each parasitic capacitance, we first notice that for any RC sub-circuit formed in the model of Fig. 7.11, voltage across the capacitance is approximately equal to $V_{sin}$ (except during the time when the capacitance is shorted by a conducting rectifier), provided the switching frequency is much lower than the corner frequency of that RC sub-circuit, i.e., $f << 1/(2\pi RC)$. Since the largest time constant is formed by $R_g$ and $C_{gs} + C_{gdpl}$, the corresponding corner frequency is over 200 MHz, and this assumption holds well up to at least 20 MHz.

Using the above assumption, current through each capacitance can be expressed as:

$$i_C = C \frac{dV_{\sin}}{dt} = A(t)C \quad , \tag{7.12}$$

where

$$A(t) = \omega \pi V_o \cos \omega t \quad . \tag{7.13}$$

The expressions for currents through the Schottky diode D1, and drain, channel, and gate resistances of Q1 are given in Table 7.2. The expressions for currents in D2 and Q2 are identical, but the waveforms are shifted by 180°.

The total power dissipation in the rectifier is

$$P_{RSR} = 2\left[ I_o V_f \frac{\omega t_{tsr}}{\pi} + (I_{sch}^{rms})^2 R_{sch} + (I_d^{rms})^2 R_d + (I_{ch}^{rms})^2 R_{cha} + (I_g^{rms})^2 R_g \right] \tag{7.14}$$

where

$$\omega t_{tsr} = \sin^{-1}\left( \frac{Vtsr}{\pi V_o} \right) \quad , \tag{7.15}$$

and $I_{sch}^{rms}$, $I_d^{rms}$, $I_{ch}^{rms}$, and $I_g^{rms}$ are rms values of $i_{sch1}$, $i_{d1}$, $i_{ch1}$, and $i_{g1}$ given in Table 7.2. The total efficiency of the resonant synchronous rectifier is

$$\eta_{RSR} = \frac{P_o}{P_o + P_{RSR}} \quad . \tag{7.16}$$

Figure 7.13 shows $\eta_{RSR}$ as a function of the switching frequency for different numbers of paralleled devices, n. Calculations of the rms currents were performed numerically using the device model of Fig. 7.7(b) with nonlinear

**Table 7.2.   Currents in diode D1 and MOSFET Q1.**

|  | $0 < V_{sin} < V_{tsr}$ |
|---|---|
| $i_{sch1}$ | $I_O + A(t)(C_{gs} + C_{ds} + C_j)$ |
| $i_{d1}$ | $A(t)C_{gdp}$ |
| $i_{ch1}$ | $0$ |
| $i_{g1}$ | $A(t)(C_{gs} + C_{gdp})$ |
|  | $0 < V_{tsr} < V_{sin}$ |
| $i_{sch1}$ | $0$ |
| $i_{d1}$ | $I_O + A(t)(C_{gdp} + C_{gs} + C_{ds} + C_j)$ |
| $i_{ch1}$ | $I_O + A(t)(C_{gs} + C_{ds} + C_j)$ |
| $i_{g1}$ | $A(t)(C_{gdp} + C_{gs})$ |
|  | $V_{sin} < 0$ |
| $i_{sch1}$ | $A(t)C_j$ |
| $i_{d1}$ | $A(t)(C_{ds} + C_{gdn})$ |
| $i_{ch1}$ | $0$ |
| $i_{g1}$ | $A(t)C_{gdn}$ |
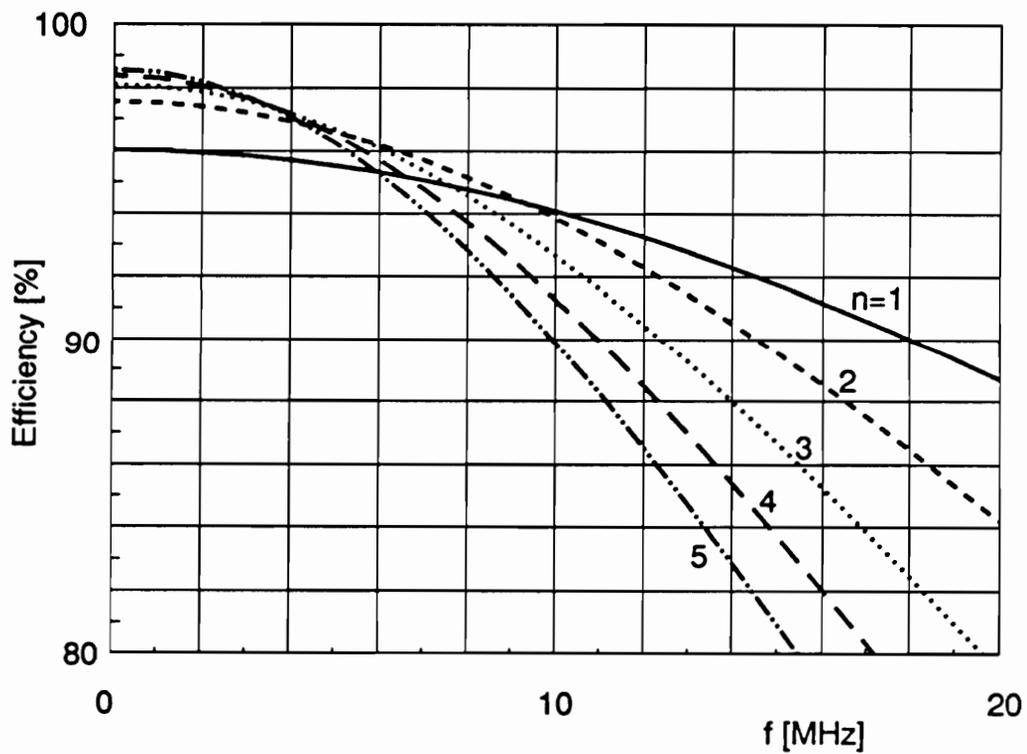
**Figure 7.13.** Efficiency of the resonant synchronous rectifier vs. frequency: Parameter n represents number of paralleled MOSFETs.

capacitances. (A MATHCAD program used for performing the efficiency calculations is given in Appendix F.) At any switching frequency, there is an optimum number of paralleled MOSFETs (or a die size) that results in the highest efficiency. For example, in the 5 to 10 MHz range, the optimum device size is equivalent to $n = 2$.

### Simplified Model

Once we have obtained results using a precise device model with nonlinear capacitances, the question arises as to what would be the accuracy of a simplified model using linear capacitances. The major part of the loss due to circulating currents is caused by rms current through $R_g$. This current is dominated by the components related to $C_{gdp}$ and $C_{gs}$. Therefore, in the simplified model we assume $C_j = C_{ds} = C_{gdn} = 0$ and, in addition, $C_{iss} = C_{gs} + C_{gdpl} = const$.

Power dissipation in the simplified model is

$$\eta'_{RSR} = 2\left[ I_o(V_f + I_o R_{sch})\frac{\omega_{tsr}}{\pi} + I_o^2(\frac{1}{2} - \frac{\omega_{tsr}}{\pi})R_{ds(on)} + \frac{\omega^2 \pi^2 V_o^2}{2}(C_{gs} + C_{gdpl})^2 R_g \right] \quad .$$

$$(7.17)$$

Figure 7.14 compares the results obtained with the full and simplified models. The simplified model provides quite accurate results even at frequencies exceeding 10 MHz. Its main advantage is that all the necessary device parameters can be obtained by very simple measurements.
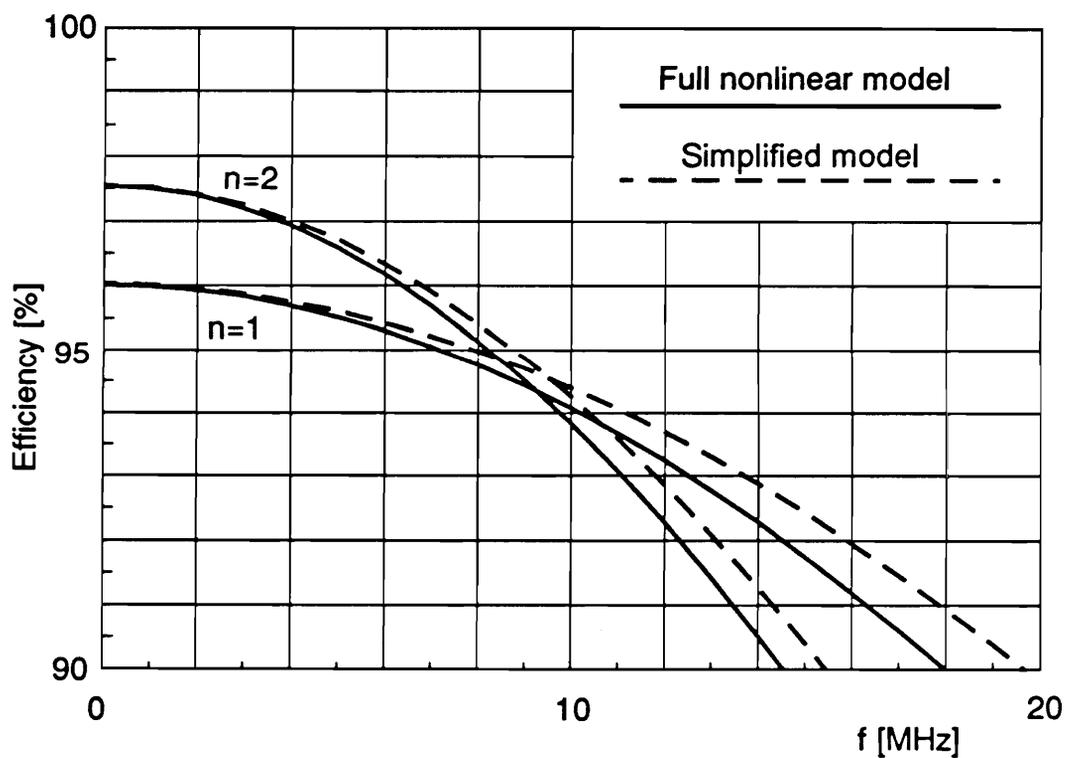
**Figure 7.14.** Efficiency of the resonant synchronous rectifier at n = 1 and n = 2: Solid lines represent results obtained using the full nonlinear capacitance model. Broken lines represent results obtained using the simplified model of the MOSFET.

## 7.3. Synchronous Rectifier Operating in a Resonant Converter with a Square Gate Drive

So far two synchronous rectifier circuit topologies have been considered: a PWM topology where both the power circuit and the gate drive are operated with square waveforms; and a resonant topology, where both the power circuit and the gate drive are operated in a resonant fashion. One more important and practical configuration is a resonant topology with a synchronous rectifier using a square wave gate drive.

The equivalent circuit diagram of this rectifier topology is shown in Fig. 7.15(a). The circuit corresponds to a rectifier section of a resonant converter, such as the forward MRC of Fig. 7.5(a). The gate drive, however, is implemented using ideal square-wave drivers, similar to those described for the PWM rectifier. As Q1 and Q2, in Fig. 7.15(a), are turned on and off, the circuit operates in the topological stages shown in Figs 7.15(b) and 7.15(c).

Fig. 7.16 shows the circuit waveforms during the topological stage of Fig. 7.15(a). The gate drive signal $V_{gs1}$ is perfectly synchronized with the input voltage $V_{sin}$. As a result, no Schottky diodes are required for commutation of the load current from Q1 to Q2 and *vice versa* (theoretically, at least). In addition, the conduction losses can be kept at a minimum since the MOSFETs always conduct the load current.

There are three sources of losses in the circuit of Fig. 7.15(a). The conduction losses:
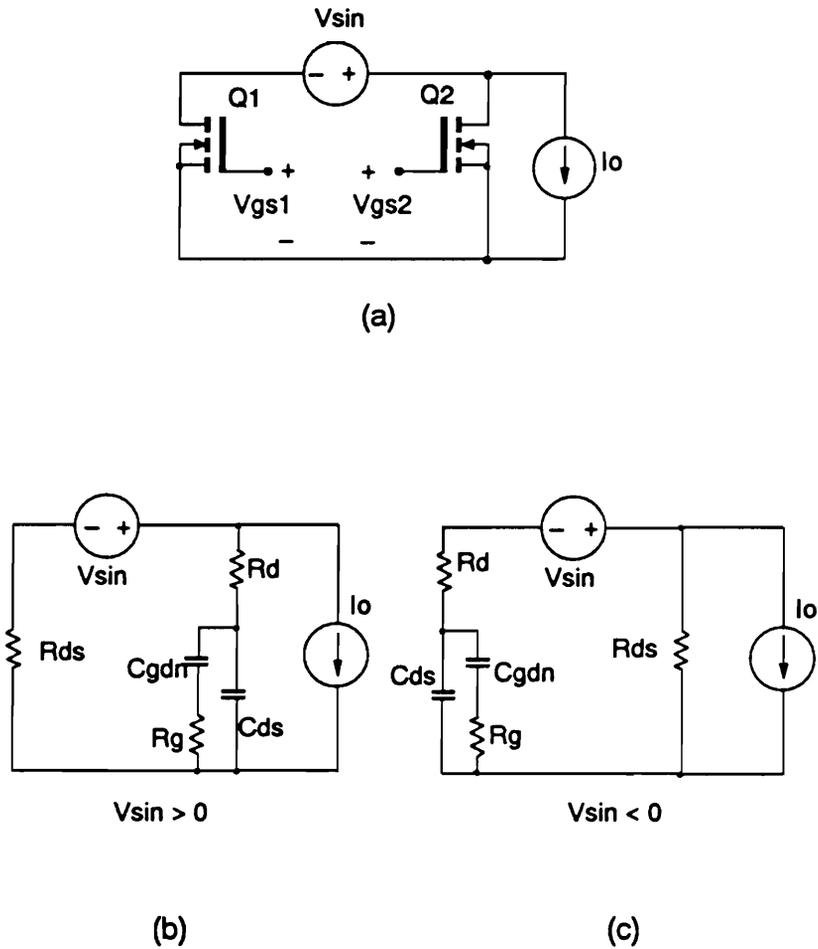
**Figure 7.15. Resonant rectifier with square-wave gate drive: (a) Simplified circuit. (b) Topological stage for $V_{sin} > 0$. (c) Topological stage for $V_{sin} < 0$.**
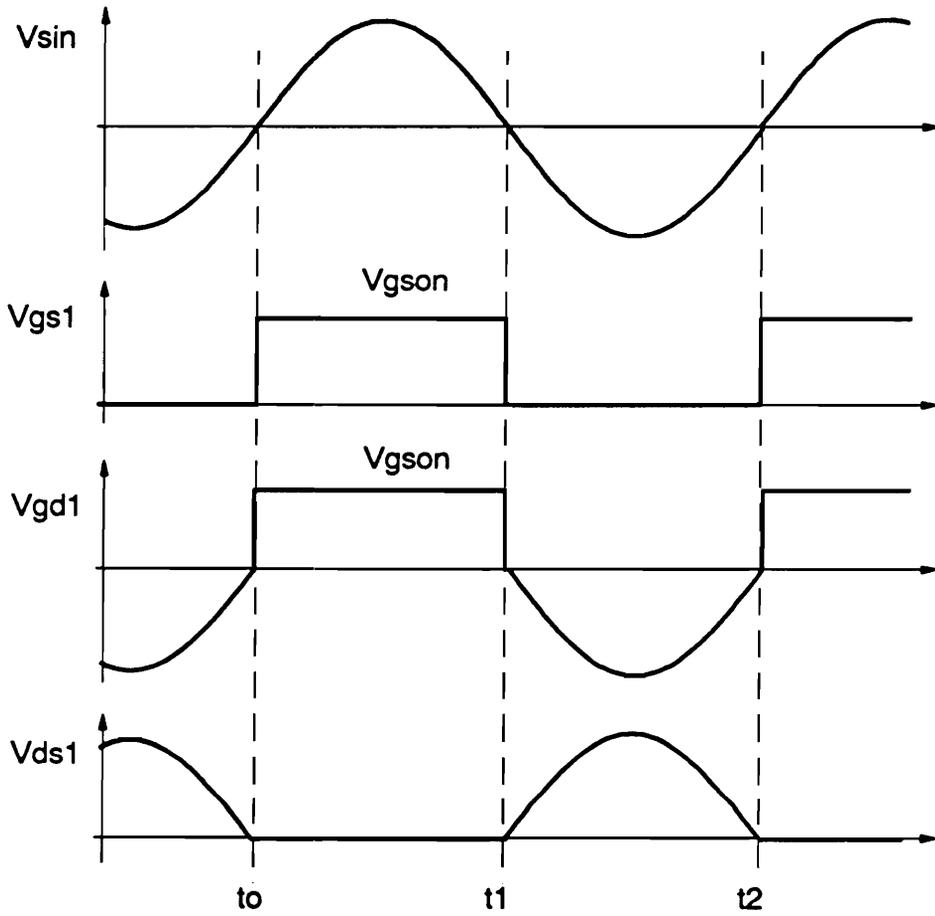
**Figure 7.16.** Waveforms of the resonant rectifier with square-wave gate drive.
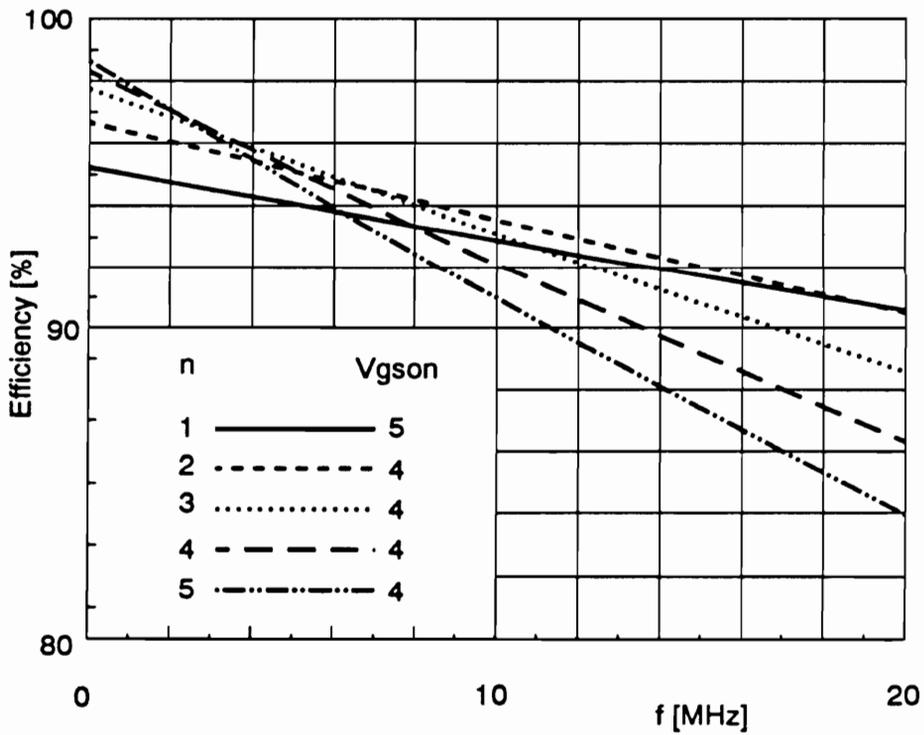
**Figure 7.17.** **Efficiency of the resonant rectifier with square-wave gate drive:** **Parameter n represents the number of paralleled MOSFETs.**

$$P_{cond} = I_o^2 R_{ds} \quad , \tag{7.18}$$

switching losses due to abrupt charging and discharging of the MOSFET input capacitances:

$$P_{sw} = 2fC_{gs}V_{gson}^2 + 2fV_{gson}\int_0^{V_{gson}} C_{gdp}(v)dv \quad , \tag{7.19}$$

and losses in the parasitic resistances due to circulating currents:

$$P_{cir} = 2(I_g^{rms})^2 R_g + 4(I_{cir}^{rms})^2 R_{ds} + 2(I_{cir}^{rms})^2(R_{ds} - R_d) \quad , \tag{7.20}$$

where $I_g^{rms}$ and $I_{cir}^{rms}$ are rms values of the circulating currents defined as follows:

$$i_g = \begin{cases} A(t)C_{gs}, & 0 \le \omega t < \pi \\ 0, & \pi \le \omega t < 2\pi \end{cases} \quad , \tag{7.21}$$

and

$$i_{cir} = \begin{cases} A(t)(C_{gdn} + C_{ds}), & 0 \le \omega t < \pi \\ 0, & \pi \le \omega t < 2\pi \end{cases} \quad . \tag{7.22}$$

In the above expressions, $R_{ds}$ is the MOSFET on-resistance controlled by $V_{gs}$, and A(t) is given by (7.13). The total loss is then:

$$P_{diss} = P_{cond} + P_{sw} + P_{cir} \quad . \tag{7.23}$$

As in the PWM synchronous rectifier, efficiency (defined as $P_O/(P_O + P_{diss})$) can be optimized for any switching frequency and device size by adjusting the gate drive signal amplitude $V_{gson}$. The optimized efficiency curves are shown in Fig. 7.17 for different numbers of paralleled devices. The results are calculated for a gate resistance of 0.25 $\Omega$.

# 7.4. Comparison of Resonant and PWM Synchronous Rectifiers

Efficiency is the major issue in the comparison of different synchronous rectifier schemes. Figure 7.18 shows optimized efficiencies of the three synchronous rectifier schemes considered in previous sections. Efficiencies of the synchronous rectifiers with square-wave gate drivers are practically independent of the gate resistance. On the other hand, the efficiency of the resonant synchronous rectifier is strongly affected by $R_g$. Therefore, resonant synchronous rectifier efficiency curves are plotted for different values of $R_g$. The curve for $R_g = 0.25$ $\Omega$ corresponds to the experimental GE MOSFET device. The curve for $R_g = 1\Omega$ represents a fictitious device with all characteristics identical to those of the experimental GE device but with gate resistance typical for a commercial low on-resistance, 50 V MOSFET. Efficiency curves for $R_g = 0$, 0.05, and 0.1 $\Omega$ indicate possible efficiency improvements with reduced gate resistance.
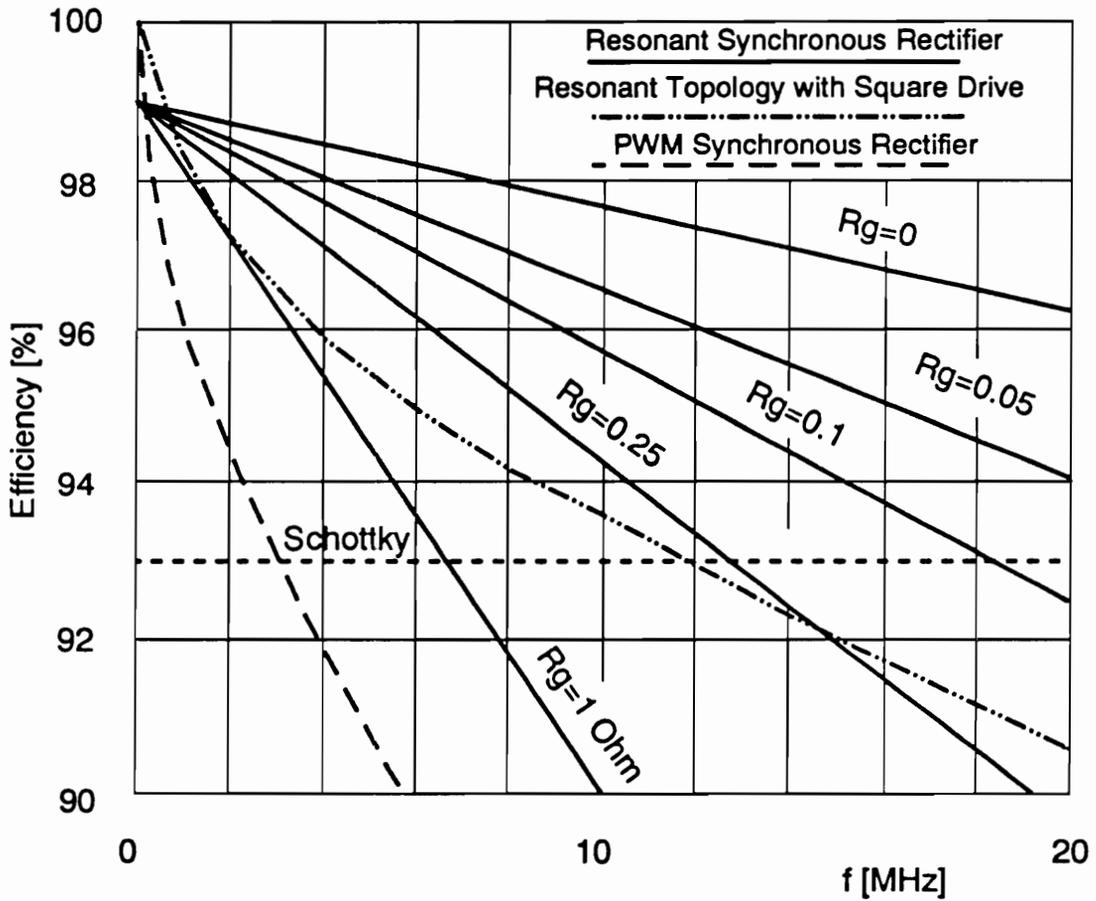
**Figure 7.18.** Comparison of the efficiencies attainable in resonant and square-wave synchronous rectifiers.

It is obvious from Fig. 7.18 that the PWM synchronous rectifier is not suitable for high frequency applications due to its limited efficiency. The resonant power stage topology provides much higher efficiency at frequencies exceeding 1 MHz, with both the square-wave and resonant gate drive arrangements. The choice between the resonant and square-wave gate drives is dictated by the gate resistance. For $R_g = 1$ $\Omega$, the square drive provides better results. However, for $R_g = 0.25$ $\Omega$ or less, the resonant gate drive approach is clearly superior.

Another consideration in the comparison of the synchronous rectifier schemes is the circuit complexity and cost. In this respect, the resonant synchronous rectifier is extremely attractive, since it does not require any gate drive circuitry. However, two Schottky diodes are necessary to conduct the load current when the MOSFETs are off. Discrete diodes could be eliminated if MOSFET devices with integrated Schottky diodes are used [S13].

## 7.5. Summary

The main problems encountered in the application of MOSFET synchronous rectification at frequencies in the megahertz range are the gate drive complexity and power dissipation. In the resonant synchronous rectifier, the MOSFETs are driven in a resonant fashion by the power circuit. As a result, the gate drivers are eliminated, thus reducing the circuit complexity. In addition,

the energy stored in the parasitic capacitances is partially recovered, and switching losses are reduced. To facilitate commutation of the load current from one rectifier to another, the MOSFET devices are used in conjunction with Schottky diodes. The MOSFETs are on during most of the switching period, thus reducing the conduction losses. However, switching of the load current is performed by the Schottky diodes with the MOSFET devices off. In this manner, the low conduction loss of MOSFET synchronous rectifiers is combined with the fast switching of Schottky diodes. The major cause of frequency-dependent losses in the resonant synchronous rectifier is the power dissipation in the parasitic gate resistance. If this resistance is reduced in future MOSFET designs, the resonant synchronous rectifier technique could be applied at 10 MHz with significant improvement of efficiency over PWM synchronous rectifier or Schottky diode rectifiers.

# 8. CONCLUSIONS

This dissertation presents a new power conversion technology--the multi-resonant technique. The essence of the multi-resonant power conversion technique is the effective utilization of the major parasitic components of the power stage including the leakage inductance of the power transformer, output capacitance of the power MOSFET, and junction capacitance of the rectifier. The multi-resonant operation is achieved by appropriate design of a resonant switching network around the semiconductor switching devices.

Zero-voltage-switched multi-resonant converters (ZVS-MRCs) are proposed for high-frequency power conversion applications. ZVS-MRCs use a resonant network with one resonant inductor and two resonant capacitors. The resonant inductor is in series with the leakage inductance of the power transformer. One of the resonant capacitors is effectively in parallel with the power MOSFET, while the other resonant capacitor is effectively in parallel with the rectifier.

As a result of the arrangement of the multi-resonant network, the major parasitic reactances of the power stage are utilized in the circuit. In addition, all semiconductor devices operate with zero-voltage switching, which substantially reduces the switching losses and permits efficient operation in multi-megahertz range.

The family of multi-resonant converters consists of a considerable number of topologies, since any PWM topology can be transformed into its multi-resonant counterpart by replacement of the active/passive semiconductor devices with the multi-resonant switch network. (Addition of external resonant components may not be necessary if the circuit is operated at frequencies sufficiently high to use the intrinsic parasitic reactances of the power stage as the resonant components.) A dc analysis is presented for the basic converter topologies: buck, boost, buck-boost, Cuk, Zeta, and SEPIC. The analysis is performed using a generalized multi-resonant switch concept. Based on the generalized analysis, a set of design guidelines is established. It is found that to optimize the efficiency of ZVS-MRCs, the ratio of resonant capacitances, $C_N$, should be minimized. The limit on the minimum value of $C_N$ is set by the desired range of conversion-ratio. Too small $C_N$ does not provide sufficiently wide range of the conversion ratio, while excessively large $C_N$ results in a reduced conversion efficiency. The characteristic impedance of the resonant circuit, $Z_0$, is the second parameter that requires careful selection. The choice of $Z_0$ is related to the trade-off between high transistor voltage stress (high $Z_0$) and high transistor current stress (low $Z_0$). To achieve minumum con-

duction losses for a given MOSFET device, $Z_0$ should be maximized within allowable transistor voltage stress limit.

Of all the ZVS-MRCs, the forward ZVS-MRC is deemed particularly attractive for board-mount power supply applications. This topology is derived from the buck ZVS-MRC by adding a power transformer and a forward diode. Unlike the PWM forward converter, the forward ZVS does not require any special transformer resetting mechanism. The transformer's core is reset by interactions between the magnetizing inductance and one of the resonant capacitors. However, due to these interactions, characteristics of the forward ZVS-MRC are different from those of buck ZVS-MRCs.

A computer-aided dc analysis of the forward ZVS-MRC is presented. Conversion-ratio characteristics are generated for selected values of $C_N$. The nature of the interactions between the magnetizing inductance and the resonant network is explained qualitatively, and to some extent, quantitatively.

The forward ZVS-MRC topology is employed to develop a high-density, state-of-the-art, on-board dc/dc power converter. The converter operates with a nominal input of 50 V and an output of 5 V at 10 A. The nominal switching frequency is 2.7 MHz. The complete hybridized converter (including power stage, control, and self-bias circuits) has a power density of 50 W/in³ and a nominal efficiency of 83%.

The efficiency achieved in the experimental converter is as good or better than those obtained in other state-of-the-art converters recently developed in the industry [E13, F3, G7, G13]. However, further improvement of the efficiency is required for successful implementation of a distributed power system con-

cept. The most significant improvement of the conversion efficiency could be achieved by replacing Schottky diodes in the rectifier stage with synchronous rectifiers. Although a significant reduction of the conduction losses can be achieved when large-area MOSFETs are used as sysnchronous rectifiers, the switching losses associated with the inter-electrode capacitances of the MOSFET device increase with the die size of the device. As a result, at high switching frequencies the enegy losses due to these capacitances can offset the reduction of the conduction losses.

One way to reduce switching losses in the synchronous rectifier is to use a resonant topology, such as the forward ZVS-MRC, and arrange the synchronous rectifier devices so that all of their inter-electrode capacitances, including the gate-to-source capacitances, become part of the resonant circuit. As a result, the synchronous rectifier devices are driven by the power stage in a resonant fashion. A loss analysis is presented to compare the effectivness of the square-wave and resonant synchronous rectifier circuits, for a converter with 5 V, 10 A output. It is shown that the square-wave approach is most efficient at frequencies below approximately 1 MHz. The resonant synchronous rectifier could extend this range to approximately 5 MHz with similar overall losses. In addition, the resonant synchronous rectifier is extrmely easy to use, since it does not require any gate-drive circuit.

The analysis and experiments presented in this dissertation provide a considerable body of knowledge on the operation, characteristics, and design of multi-resonant converters. The discovery of the multi-resonant technology provides numerous research opportunities for future quest for new and better

power conversion technologies. The following research areas are of considerable interest for future work:

- **Zero-current-switched MRCs.** The ZCS-MRCs have not been addressed in this work because they are not deemed suitable for very high-frequency applications where power MOSFETs are used. However, due to the turn-off switching characteristics of minority-carrier, high-power semiconductor devices (such as SCR, GTO, and MCT), ZCS topologies are very desirable for high-power conversion circuits. Since for minority-carrier devices zero-current switching is beneficial, and increased peak current does not cause cause significantly increased losses, the ZCS-MRCs may offer advantages for certain high-power high-current applications.

- **Investigation of higher-order MRCs.** The MRCs discussed in this dissertation contain (effectively) only three resonant components. However, resonant circuits of higher complexity are conceivable. For example, ZCS-MRCs actually have a five-component resonant network, if the parasitic capacitances of the semiconductor devices are not neglected. Investigation of higher-order multi-resonant circuits may uncover other topologies of interest. However, it is difficult to predict the practical value of such topologies.

- **Detailed dc analysis of the forward ZVS-MRC.** The operation of the forward ZVS-MRC is considerably different from that of the buck ZVS-MRC. The computer-aided analysis presented in this dissertation does not treat

the subject in desirable detail and depth. Further study is required to gain better understanding of this circuit.

- **Small-signal analysis of ZCS and ZVS MRCs.** Small-signal models for MRCs should be developed to allow optimum design of control circuits. The possibility of using multiple control loops for MRCs should be investigated.

- **Analysis of crossregulation in multiple-output ZVS-MRCs.** The cross-regulation characteristics of ZVS-MRCs are affected by the power transformer design (coupling between the output windings), output filter design (coupled or non-coupled inductors), design of the multi-resonant circuit (distribution of the resonant capacitance among the windings), and choice of the rectifiers (junction capacitance and resistance). An analysis of these relations would be very valuable in understanding the cross-regulation characteristics.

- **Experimental verification of the resonant synchronous rectifier concept.** The theoretical analysis presented in this dissertation for the resonant synchronous rectifier indicates that such a rectification scheme could be advantageous at high switching frequencies. However, this concept has not been verified experimentally, because of lack of availability of suitable devices. However, as the semiconductor devices are improved, it should be possible to verify experimentally the resonant synchronous rectifier concept, particularly if a dedicated device with low gate resistance is available.

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# Appendix A. PROGRAMS FOR CALCULATION OF

# DC CHARACTERISTICS OF ZVS-MRCS

```
C-------------------------------------------------------------------
C    THIS PROGRAM GENERATES SINGLE OPERATING POINT RESULTS
C-------------------------------------------------------------------
      IMPLICIT REAL*8 (A-H,O-Z)
      REAL*8 IN,M
      CD = 3.
      IN = 1.0
      TXN = 0.27
      CALL POINT(CD,IN,TXN,F,M,VSMAX)
C-------------------------------------------------------------------
C    FOR BOOST CONVERTER INSERT HERE: M = 1/M
C    FOR B/B CONVERTER INSERT HERE:  M = M/(1-M)
C-------------------------------------------------------------------
      WRITE(2,101)F,M
      WRITE(3,101)F,VSMAX
101   FORMAT(4E12.4)
      END
```

```
C-----------------------------------------------------------------
C     THIS PROGRAM GENERATES SINGLE LINE FOR IN = CONST.
C-----------------------------------------------------------------
      IMPLICIT REAL*8 (A-H,O-Z)
      REAL*8 IN,M
      CD = 2.
      IN = 1.0
      TXNMAX = 0.75
      NTX = 10
      DTXN = TXNMAX/(NTX-1)
      TXN = 0.0
      DO 1 J = 1,NTX
        CALL POINT(CD,IN,TXN,F,M,VSMAX)
        TXN = TXN + DTXN
        WRITE(2,101)F,M
        WRITE(3,101)F,VSMAX
    1 CONTINUE
  101   FORMAT(4E12.4)
      END
```

```
C------------------------------------------------------------------------
C    THIS PROGRAM GENERATES SINGLE OPERATING POINT FOR A GIVEN RN
C------------------------------------------------------------------------
      IMPLICIT REAL*8 (A-H,O-Z)
      REAL*8 IN,M
      REAL*8 MP,RN,INGUES,MDOT,INP
      EPSNWT = 0.01
      CD = 3.0
      RN = 0.2
      TXN = 0.25
      INGUES = 1./10./RN
      IF(INGUES.LT.0.01) INGUES = 0.01
      IN = INGUES
      NCOUNT = 1
  6     VSMAX = 0.
        CALL POINT(CD,IN,TXN,F,M,VSMAX)
C------------------------------------------------------------------------
C    FOR BOOST CONVERTER INSERT HERE: M = 1/M
C    FOR B/B CONVERTER INSERT HERE:  M = M/(1-M)
C------------------------------------------------------------------------
        IF(F.EQ.-1.)GOTO 4
        DRN = M/IN-RN
        IF(ABS(DRN).LT.EPSNWT*RN) GOTO 4
        NCOUNT = NCOUNT + 1
        IF(NCOUNT.GT.20) THEN
          F = -1.
          M = -3.
          GOTO 4
        ENDIF
        DIN = IN/10000.
        INP = IN
        MP = M
        IN = INP + DIN
        CALL POINT(CD,IN,TXN,F,M,VSMAX)
C------------------------------------------------------------------------
C    FOR BOOST CONVERTER INSERT HERE: M = 1/M
C    FOR B/B CONVERTER INSERT HERE:  M = M/(1-M)
C------------------------------------------------------------------------
        IF(M.EQ.-1.) GOTO 4
        MDOT = (M-MP)/DIN
        IN = INP-INP*(MP-RN*INP)/(MDOT*INP-MP)
        IF(IN.LT.0.01)IN = 0.01
        GOTO 6
  4     INGUES = IN
      WRITE(2,101)F,M
      WRITE(3,101)F,VSMAX
101     FORMAT(2E12.4)
      END
```

```
C-------------------------------------------------------------------
C     THIS PROGRAM GENERATES SINGLE LINE FOR A GIVEN RN
C-------------------------------------------------------------------
      IMPLICIT REAL*8 (A-H,O-Z)
      REAL*8 IN,M
      REAL*8 MP,RN,INGUES,MDOT,INP
      CD = 3.0
      RN = 0.2
      TXNMAX = 0.75
      NTX = 100
      DTXN = TXNMAX/(NTX-1)
      TXN = 0.0
      EPSNWT = 0.01
      INGUES = 1./10./RN
      IF(INGUES.LT.0.01) INGUES = 0.01
      DO 1 J = 1,NTX
         IN = INGUES
         NCOUNT = 1
6        VSMAX = 0.
         CALL POINT(CD,IN,TXN,F,M,VSMAX)
C-------------------------------------------------------------------
C     FOR BOOST CONVERTER INSERT HERE: M = 1/M
C     FOR B/B CONVERTER INSERT HERE:  M = M/(1-M)
C-------------------------------------------------------------------
         IF(F.EQ.-1.)GOTO 4
         DRN = M/IN-RN
         IF(ABS(DRN).LT.EPSNWT*RN) GOTO 4
         NCOUNT = NCOUNT + 1
         IF(NCOUNT.GT.20) THEN
           F = -1.
           M = -3.
           GOTO 4
         ENDIF
         DIN = IN/10000.
         INP = IN
         MP = M
         IN = INP + DIN
         CALL POINT(CD,IN,TXN,F,M,VSMAX)
C-------------------------------------------------------------------
C     FOR BOOST CONVERTER INSERT HERE: M = 1/M
C     FOR B/B CONVERTER INSERT HERE:  M = M/(1-M)
C-------------------------------------------------------------------
         IF(M.EQ.-1.) GOTO 4
         MDOT = (M-MP)/DIN
         IN = INP-INP*(MP-RN*INP)/(MDOT*INP-MP)
         IF(IN.LT.0.01)IN = 0.01
         GOTO 6
4        INGUES = IN
         WRITE(2,101)F,M
         WRITE(3,101)F,VSMAX
         TXN = TXN + DTXN
1     CONTINUE
101   FORMAT(2E12.4)
      END
```

```
C------------------------------------------------------------------------
C    MAIN SUBROUTINE FOR CALCULATION OF DC CHARACTERISTICS
C    OF THE MULTI-RESONANT SWITCH (OR BUCK ZVS-MRC)
C------------------------------------------------------------------------
C    INPUT PARAMETERS:
C        CAPACITANCE RATIO, CD
C        NORMALIZED OUTPUT CURRENT, IN
C        TX NORMALIZED WITH RESPECT TO RESONANT PERIOD OF STAGE T1A
C    OUTPUT PARAMETERS
C        CONVERSION-RATIO M,
C        MOSFET VOLTAGE STRESS, VSMAX
C        NORMALIZED SWITCHING FREQUENCY, F
C------------------------------------------------------------------------
      SUBROUTINE POINT (CD,IN,TXN,F,M,VSMAX)
      IMPLICIT REAL*8 (A-H,O-Z)
      REAL*8 IN,IINIT,M,I,INAUX
      INTEGER S
      LOGICAL CONT,ZVS
C------------------------------------------------------------------------
      COMMON /PI/        PI
      COMMON /RESCKTPAR/   CDAUX,W,WD,Z,ZD,Y,YD
      COMMON /CONTRPAR/    ETN,EI,EVS,EVD,NSPP
      COMMON /IN/         INAUX
      COMMON /VSMAX/       VSMAXAUX
C------------------------------------------------------------------------
C    CDAUX AND INAUX ARE AUXILIARY VARIABLES IDENTICAL TO CD AND IN
C------------------------------------------------------------------------
      CDAUX = CD
      INAUX = IN
C------------------------------------------------------------------------
      PI = 4*ATAN(1.)
C------------------------------------------------------------------------
      ETN = 0.01
      EI = 0.01
      EVS = 0.01
      EVD = 0.01
      NSPP = 10
C------------------------------------------------------------------------
      WD = 1/SQRT(CD)
      ZD = SQRT(1./CD)
      YD = 1/ZD
      C = CD/(1. + CD)
      W = 1/SQRT(C)
      Z = SQRT(1./C)
      Y = 1/Z
C------------------------------------------------------------------------
      TD = 2*PI/WD
      TX = TXN*TD
C------------------------------------------------------------------------
      TON = 0.
      TOFF = 0.
      VDAREA = 0.
      ZVS = .TRUE.
      CONT = .TRUE.
      CALL T1A(TX,IINIT,VDINIT,VDAREA,TON.CONT)
```

```fortran
      IF(.NOT.CONT) THEN
        F=-1.
        M=-2.
        RETURN
      ENDIF
      CALL T2(S,IINIT,VSINIT,VDINIT,VDAREA,TOFF)
      IF(S.EQ.1) THEN
        CALL T1B(IINIT,VDINIT,VDAREA,TON)
        IF(TON.EQ.-1.)THEN
          F=-1.
          M=-1.
          RETURN
        ENDIF
      ELSE
        CALL T3(IINIT,VSINIT,VDAREA,TOFF,ZVS)
        IF(.NOT.ZVS)THEN
          F=-1.
          M=-1.
          RETURN
        ENDIF
      ENDIF
      CALL T4(IINIT,TON)
      P=TON+TOFF
      FS=0.5/PI
      F=1/P/FS
      VO=VDAREA/P
      M=VO
C-------------------------------------------------------------
C     VSMAXAUX IS AN AUXILIARY VARIABLE IDENTICAL TO VSMAX
C-------------------------------------------------------------
      VSMAX=VSMAXAUX
C-------------------------------------------------------------
      RETURN
      END
C-------------------------------------------------------------
C+ + + + + + + + + + + + + + + + + + + + + + + + + +
C-------------------------------------------------------------
      SUBROUTINE T1A(TX,IINIT,VD,VDAREA,TON,CONT)
      IMPLICIT REAL*8 (A-H,O-Z)
      REAL*8 IN,I,IINIT
      LOGICAL CONT
C-------------------------------------------------------------
      COMMON /IN/        IN
C-------------------------------------------------------------
      I=AI1(TX,IN,0.)
      VD=VD1(TX,IN,0.)
      VDAREA=VDA1(TX,IN,0.)
      TON=TX
      IF(I.LT.0.) CONT=.FALSE.
      IINIT=I
      RETURN
      END
C-------------------------------------------------------------
C+ + + + + + + + + + + + + + + + + + + + + + + + + +
C-------------------------------------------------------------
      SUBROUTINE T1B(IINIT,VDINIT,VDAREA,TON)
```

```
      IMPLICIT REAL*8 (A-H,O-Z)
      REAL*8 IN,IINIT,I
      LOGICAL CONT
C-----------------------------------------------------------------
      COMMON /PI/          PI
      COMMON /RESCKTPAR/        CD,W,WD,Z,ZD,Y,YD
      COMMON /CONTRPAR/         ETN,EI,EVS,EVD,NSPP
      COMMON /IN/          IN
C-----------------------------------------------------------------
      DT=2*PI/WD/NSPP
      ET=ETN*2*PI/WD
C----------------
C    GOUP2ND=1. MEANS VD GOES UP FOR 2ND TIME
C    GODOWN=1.  MEANS VD WAS GOING DOWN
C    VDP= VD PREVIOUS
C------------------
      GODOWN=0.
      GOUP2ND=0.
      VDP=VDINIT
      T=0.
      GOTO 3
    2 T=T-DT
      DT=DT/2
    3 T=T+DT
      I=AI1(T,IINIT,VDINIT)
      VD=VD1(T,IINIT,VDINIT)
      IF(GODOWN.EQ.1.)THEN
       IF(VD.GT.VDP)THEN
         TON=-1.
         RETURN
       ENDIF
      ELSE
       IF(VD.LT.VDP)GODOWN=1.
      ENDIF
      IF(VD.LT.-EVD) GOTO 2
      IF(I-IN.GT.EI) GOTO 2
      IF(ABS(VD).LT.EVD) GOTO 4
      IF(ABS(I-IN).LT.EI) GOTO 4
      GOTO 3
    4 IF(DT.GT.ET) GOTO 2
      VDAREA=VDAREA+VDA1(T,IINIT,VDINIT)
      TON=TON+T
      IF(ABS(I-IN).LT.EI) I=IN
      IINIT=I
      VDINIT=VD
      RETURN
      END
C-----------------------------------------------------------------
C+ + + + + + + + + + + + + + + + + + + + + + +
C-----------------------------------------------------------------
      SUBROUTINE T2(S,IINIT,VSINIT,VDINIT,VDAREA,TOFF)
      IMPLICIT REAL*8 (A-H,O-Z)
      REAL*8 IN,IINIT,I
      INTEGER S
C-----------------------------------------------------------------
      COMMON /PI/          PI
```

```
      COMMON /RESCKTPAR/     CD,W,WD,Z,ZD,Y,YD
      COMMON /CONTRPAR/      ETN,EI,EVS,EVD,NSPP
      COMMON /VSMAX/         VSMAX
C------------------------------------------------------------------
      DT = 2*PI/W/NSPP
      ET = ETN*2*PI/W
      VSINIT = 0.
      T = 0.
      GOTO 3
    1 S = 0
    2 T = T-DT
      DT = DT/2
    3 T = T + DT
      I = AI2(T,IINIT,VSINIT,VDINIT)
      VS = VS2(T,IINIT,VSINIT,VDINIT)
      VD = VD2(T,IINIT,VSINIT,VDINIT)
      IF(VS.GT.VSMAX)VSMAX = VS
      IF(VS.LT.-EVS) GOTO 2
      IF(VD.LT.-EVD) GOTO 2
      IF(ABS(VS).LT.EVS) THEN
        S = 1
        GOTO 4
      ENDIF
      IF(ABS(VD).LT.EVD) THEN
        S = 0
        GOTO 4
      ENDIF
      GOTO 3
    4 IF(DT.GT.ET) GOTO 1
      VDAREA = VDAREA + VDA2(T,IINIT,VSINIT,VDINIT)
      TOFF = TOFF + T
      IINIT = I
      VDINIT = VD
      VSINIT = VS
      RETURN
      END
C------------------------------------------------------------------
C+ + + + + + + + + + + + + + + + + + + + + + + + + + +
C------------------------------------------------------------------
      SUBROUTINE T3(IINIT,VSINIT,VDAREA,TOFF,ZVS)
      IMPLICIT REAL*8 (A-H,O-Z)
      REAL*8 IN,IINIT,I
      INTEGER S,D,ZVSTES
      LOGICAL ZVS
C------------------------------------------------------------------
      COMMON /PI/            PI
      COMMON /CONTRPAR/      ETN,EI,EVS,EVD,NSPP
      COMMON /VSMAX/         VSMAX
C------------------------------------------------------------------
C    TP - PREVIOUS TIME
C    ZVSTES = 1: TEST FOR POSSIBLE NONZERO SWITCHING
C    VSP    : PREVIOUS VALUE OF T
C    DVSP   : PREVIOUS VALUE OF DVS
C    DVS    : DERIVATIVE OF VS
C------------------------------------------------------------------
      DT = 2*PI/NSPP
```

```
        ET = ETN*2*PI
        ZVSTES = 1
        TP = 0.
        DVS = 1
        VS = 0.
        T = 0.
        GOTO 3
    1   S = 0
    2   T = T-DT
        DT = DT/2
    3   T = T + DT
        VSP = VS
        DVSP = DVS
        I = AI3(T,IINIT,VSINIT)
        VS = VS3(T,IINIT,VSINIT)
        IF(VS.GT.VSMAX)VSMAX = VS
        IF(ZVSTES.EQ.1)THEN
          DVS = VS-VSP
          IF(DVS.GT.0.AND.DVSP.LE.0)THEN
            IF(DT.LE.ET) THEN
              ZVS = .FALSE.
              RETURN
            ELSE
              GOTO 2
            ENDIF
          ENDIF
        ENDIF
        IF(VS.LT.-EVS) THEN
          ZVSTES = 0
          GOTO 2
        ENDIF
        IF(ABS(VS).GT.EVS) GOTO 3
        IF(DT.GT.ET) GOTO 1
        TOFF = TOFF + T
        IINIT = I
        VDINIT = 0.
        VSINIT = VS
        RETURN
        END
C-------------------------------------------------------------
C+ + + + + + + + + + + + + + + + + + + + + + + + + +
C-------------------------------------------------------------
        SUBROUTINE T4(IINIT,TON)
        IMPLICIT REAL*8 (A-H,O-Z)
        REAL*8 IN,IINIT,I
C-------------------------------------------------------------
        COMMON /IN/          IN
C-------------------------------------------------------------
        T = IN-IINIT
        TON = TON + T
        RETURN
        END
C-------------------------------------------------------------
C+ + + + + + + + + + + + + + + + + + + + + + + + + +
C-------------------------------------------------------------
        FUNCTION AI1(T,IINIT,VDINIT)
```

```fortran
      IMPLICIT REAL*8 (A-H,O-Z)
      REAL*8 IN,IINIT
C-------------------------------------------------------------
      COMMON /RESCKTPAR/   CD,W,WD,Z,ZD,Y,YD
      COMMON /IN/          IN
C-------------------------------------------------------------
      AI1 = (1.-VDINIT)*YD*SIN(WD*T) + (IINIT-IN)*COS(WD*T) + IN
      RETURN
      END
C-------------------------------------------------------------
C+ + + + + + + + + + + + + + + + + + + + + + + +
C-------------------------------------------------------------
      FUNCTION VD1(T,IINIT,VDINIT)
      IMPLICIT REAL*8 (A-H,O-Z)
      REAL*8 IN,IINIT
C-------------------------------------------------------------
      COMMON /RESCKTPAR/   CD,W,WD,Z,ZD,Y.YD
      COMMON /IN/          IN
C-------------------------------------------------------------
      VD1 = 1.-COS(WD*T) + VDINIT*COS(WD*T) + ZD*(IINIT-IN)*SIN(WD*T)
      RETURN
      END
C-------------------------------------------------------------
C+ + + + + + + + + + + + + + + + + + + + + + + +
C-------------------------------------------------------------
      FUNCTION AI2(T,IINIT,VSINIT,VDINIT)
      IMPLICIT REAL*8 (A-H,O-Z)
      REAL*8 IN,IINIT
C-------------------------------------------------------------
      COMMON /RESCKTPAR/   CD,W,WD,Z,ZD,Y,YD
      COMMON /IN/          IN
C-------------------------------------------------------------
      COSWT = COS(W*T)
      SINWT = SIN(W*T)
      AI2 = IINIT*COSWT-W*VSINIT*SINWT + (1.-VDINIT + VSINIT/CD)*Y*SINWT
      +   + IN/(1. + CD)*(1-COSWT)
      RETURN
      END
C-------------------------------------------------------------
C+ + + + + + + + + + + + + + + + + + + + + + + +
C-------------------------------------------------------------
      FUNCTION VS2(T,IINIT,VSINIT,VDINIT)
      IMPLICIT REAL*8 (A-H,O-Z)
      REAL*8 IN,IINIT
C-------------------------------------------------------------
      COMMON /RESCKTPAR/   CD,W,WD,Z,ZD,Y,YD
      COMMON /IN/          IN
C-------------------------------------------------------------
      COSWT = COS(W*T)
      SINWT = SIN(W*T)
      VS2 = VSINIT*COSWT + 1./W*IINIT*SINWT + IN*T/(1. + CD)-
      +   IN/W/(1. + CD)*SINWT +
      +   (1.-VDINIT + VSINIT/CD)*CD/(CD + 1.)*(1-COSWT)
      RETURN
      END
C-------------------------------------------------------------
```

```
C+ + + + + + + + + + + + + + + + + + + + + + +
C--------------------------------------------------------------------
      FUNCTION VD2(T,IINIT,VSINIT,VDINIT)
      IMPLICIT REAL*8 (A-H,O-Z)
      REAL*8 IN,IINIT
C--------------------------------------------------------------------
      COMMON /RESCKTPAR/   CD,W,WD,Z,ZD,Y,YD
      COMMON /IN/          IN
C--------------------------------------------------------------------
      COSWT = COS(W*T)
      SINWT = SIN(W*T)
      VD2 = VDINIT + VSINIT/CD*COSWT + 1./W/CD*IINIT*SINWT +
     +    (1.-VDINIT + VSINIT/CD)/(1. + CD)*(1-COSWT)-IN*T/(1. + CD)-
     +    VSINIT/CD-IN/W/CD/(1. + CD)*SINWT
      RETURN
      END
C--------------------------------------------------------------------
C+ + + + + + + + + + + + + + + + + + + + + + + +
C--------------------------------------------------------------------
      FUNCTION AI3(T,IINIT,VSINIT)
      IMPLICIT REAL*8 (A-H,O-Z)
      REAL*8 IN,IINIT
C--------------------------------------------------------------------
      AI3 = (1.-VSINIT)*SIN(T) + IINIT*COS(T)
      RETURN
      END
C--------------------------------------------------------------------
C+ + + + + + + + + + + + + + + + + + + + + + + +
C--------------------------------------------------------------------
      FUNCTION VS3(T,IINIT,VSINIT)
      IMPLICIT REAL*8 (A-H,O-Z)
      REAL*8 IN,IINIT
C--------------------------------------------------------------------
      COMMON /RESCKTPAR/   CD,W,WD,Z,ZD,Y,YD
C--------------------------------------------------------------------
      VS3 = VSINIT*COS(T) + IINIT*SIN(T) + 1-COS(T)
      RETURN
      END
C--------------------------------------------------------------------
C+ + + + + + + + + + + + + + + + + + + + + + + +
C--------------------------------------------------------------------
      FUNCTION VDA1(T,IINIT,VDINIT)
      IMPLICIT REAL*8 (A-H,O-Z)
      REAL*8 IN,IINIT
C--------------------------------------------------------------------
      COMMON /RESCKTPAR/   CD,W,WD,Z,ZD,Y,YD
      COMMON /IN/          IN
C--------------------------------------------------------------------
      VDA1 = T + 1./WD*(VDINIT-1.)*SIN(WD*T) +
     +     1./WD*(IINIT-IN)*ZD*(1-COS(WD*T))
      RETURN
      END
C--------------------------------------------------------------------
C+ + + + + + + + + + + + + + + + + + + + + + + +
C--------------------------------------------------------------------
      FUNCTION VDA2(T,IINIT,VSINIT,VDINIT)
```

```
      IMPLICIT REAL*8 (A-H,O-Z)
      REAL*8 IN,IINIT
C--------------------------------------------------------------------
      COMMON /RESCKTPAR/   CD,W,WD,Z,ZD,Y,YD
      COMMON /IN/          IN
C--------------------------------------------------------------------
      SINWT = SIN(W*T)
      COSWT = COS(W*T)
      VDA2 = VDINIT*T + 1./W/CD*VSINIT*SINWT + IINIT/W/W/CD*(1-COSWT) +
     +      (1.-VDINIT + VSINIT/CD)/(1. + CD)*(T-1./W*SINWT)-
     +      0.5*IN/(1. + CD)*T*T-VSINIT/CD*T-
     +      IN/W/W/CD/(1. + CD)*(1-COSWT)
      RETURN
      END
C--------------------------------------------------------------------
C + + + + + + + + + + + + + + + + + + + + + + + +
C--------------------------------------------------------------------
```

# Appendix B. DEVICE STRESSES IN ZVS-MRCS

Approximate expressions for transistor current stress and diode current and voltage stress in basic ZVS-MRCs can be found by examination of expressions derived in Chapter 3 for resonant current and voltages. The voltage stress of the transistor is best determined using the normalized transistor voltage stress characteristics given in Chapter 3.

## B.1. Buck ZVS-MRC

### Transistor Current Stress

As can be seen from Figs. 3.6 and 3.7, the peak value of the transistor current occurs during stage T1A. Since during T1A the active switch (transistor) current is equal to the resonant inductor current, the maximum peak current of the switch can be found by substituting $\omega_D t = \pi/2$ into (3.13.g) and using the maximum values for $I_O$ and $V_{IN}$:

$$I_{Smax} = I_{Lmax} \leq \frac{V_{INmax}}{Z_D} + I_{Omax} = V_{INmax} \frac{\sqrt{C_N}}{Z_0} + I_{Omax} \quad . \tag{B.1}$$

The expression on the right-hand side of (B.1) is an absolute maximum value of the transistor current stress. In many practical situations the stress will be lower than that given by (B.1) because (B.1) is calculated using the input voltage at high line, $V_{INmax}$. If a design calls for a substantial input voltage range, at high line stage T1A may be terminated *before* the resonant inductor current reaches the peak value corresponding to $\omega_D t = \pi/2$. In such a case, the actual current stress will be lower than that predicted by (B.1). Nevertheless, in most practical situations (B.1) is sufficient for estimating transistor current stress.

### Rectifier Voltage Stress

The peak value of the diode voltage occurs either during topological stage T1A or during T2. If the on-time is sufficiently long to allow a half-cycle oscillation during T1A (if $\omega_D t_x \geq \pi$), the peak of $v_D$ will occur during T1A. In such a case, the maximum peak value of $v_D$ can be found by substituting $\omega_D t_x = \pi$ into (3.13.i):

$$V_{Dpeak} = 2V_{IN} \quad . \tag{B.2}$$

If the peak of $v_D$ occurs during T2, its value must be *less* than $2V_{IN}$. This can be explained as follows. The initial conditions for T2 are the final conditions of T1A. If, during T1A, $v_D$ has reached its peak value (*i.e.*, $\omega_D t_x \geq \pi$), the initial value of the resonant inductor current is $i_{LR} \leq I_O$ and consequently, the initial value of the current flowing into $C_D$ is less than or equal to zero. Therefore, $v_D$

either peaks exactly at the beginning of T2 (when $\omega_D t_x = \pi/2$) and is equal to $2V_{IN}$, or it does not peak at all during T2. If $v_D$ has not reached its peak during T1A ($\omega_D t_x < \pi/2$), the initial condition for the resonant inductor current during T2 is $i_{LR}(0) > I_O$ and consequently, the initial current flowing through $C_D$ at the beginning of T2 will be greater than zero. As a result, $v_D$ will be increasing initially and will eventually peak during T2. However, the value of the peak must be lower than that given by (B.2) since the resonant inductor current during T2 decreases faster during T2 than during T1A, due to the additional impedance of $C_S$ introduced in the resonant circuit at the transition from T1A to T2. As a result, $v_D$ during T2 reaches a lower peak value than it would reach during T1A. In conclusion, under any conditions the diode voltage stress cannot exceed $2V_{IN}$. Therefore, the diode voltage stress is limited by:

$$V_{Dmax} \leq 2V_{INmax} \qquad . \qquad (B.3)$$

The stress given by (B.3) is an upper limit, since in most practical converters the peak diode voltage at high line occurs during stage T2, and as explained, it cannot reach value of $2V_{IN}$. However, for practical applications (B.3) gives a sufficient approximation of diode voltage stress.

### Rectifier Current Stress

Rectifier current stress can be estimated by noting that the peak diode current occurs when the resonant inductor peaks in the negative direction. The magnitude of the negative peak of the resonant inductor current is always lower than the magnitude of the positive peak; therefore, the upper limit on the rectifier current stress is given by the following expression:

$$I_{Dmax} \leq 2I_{Omax} + V_{INmax} \frac{\sqrt{C_N}}{Z_0} \quad . \tag{B.4}$$

The result given by the above expression is, analogous to (B.3), a conservative estimate of the device stress.

## B.2. Boost ZVS-MRC

The stresses in boost ZVS-MRC are found using an approach similar to that described for buck converter:

**Transistor Current Stress:**

$$I_{Smax} \leq V_O \frac{\sqrt{C_N}}{Z_0} + I_{INmax} \quad . \tag{B.5}$$

**Rectifier Voltage Stress:**

$$V_{Dmax} \leq 2V_O \quad . \tag{B.6}$$

**Rectifier Current Stress:**

$$I_{Dmax} \leq 2I_{INmax} + V_O \frac{\sqrt{C_N}}{Z_0} \quad . \tag{B.7}$$

## B.3. Flyback, Cuk, ZETA, and SEPIC ZVS-MRCs

Expressions for stresses in the up/down (flyback, Cuk, Zeta, and SEPIC) converters are found using the same approach as that used for buck and boost ZVS-MRCs. However, two complications are encountered with the up/down converters. One is that the stresses are parabolic functions of the conversion ratio, a situation similar to that found in QRCs [J7]. As a result, it is difficult to predict whether the maximum stresses occur at low, high, or at some intermediate value of the input voltage. One practical way to estimate the stresses is to calculate the stress expressions for both high and low line, and use the higher value as an estimate.

The second complication encountered in the up/down converters is related to the possibility of using a transformer in these topologies. The turns ratio of the transformer, $n$, affects the transistor current and voltage stress, and the diode current stress. As a result, $n$ must be selected for optimum device stresses.

Assuming the transformer turns ratio is known, the upper limits on the device stresses are given below:

**Transistor Current Stress**:

$$I_{Speak} \le nV_O\left(1 + \frac{1}{M}\right)\frac{\sqrt{C_N}}{Z_0} + \frac{I_{Omax}}{n}(1 + M) \quad . \tag{B.8}$$

To determine a conservative estimate of the transistor current stress, (B.8) should be evaluated for both $M = M_{min}$ and $M = M_{max}$, and a higher value of $I_{Speak}$ should be used as an estimate for $I_{Smax}$.

**Rectifier Voltage Stress:**

The maximum rectifier voltage stress occurs at low line,

$$V_{Dmax} = 2V_O\left(1 + \frac{1}{M_{min}}\right) \quad .$$

(B.9)

**Rectifier Current Stress:**

$$I_{Dpeak} \leq 2I_{Omax}(1 + M) + n^2 V_O\left(1 + \frac{1}{M}\right)\frac{\sqrt{C_N}}{Z_0} \quad .$$

(B.10)

To find a conservative estimate on the rectifier current stress, (B.10) should be evaluated for both $M_{min}$ and $M_{max}$, and a higher value of $I_{Dpeak}$ should be chosen as a maximum stress.

# Appendix C. QUASI-RESONANT GATE DRIVE

The concept of a quasi-resonant gate drive is based on the observation that in ZVS-QRCs and ZVS-MRCs fast switching is critical only during turn-off. The switching loss, caused by the nonzero product of the drain-to-source voltage and the drain current, occurs only during turn-off. Therefore, in ZVS-QRCs and MRCs, the fall time of the gate-to-source voltage should be minimized to achieve fast turn off. Rise time of the gate-to-source voltage, however, can be much longer, since turn-on occurs during the conduction period of the MOSFET's body diode, which occupies a substantial portion of the switching period. Thus, fast turn-off can be achieved in a conventional, dissipative manner, while turn on can be obtained using a resonant technique. Such operation of the gate drive should theoretically reduce power dissipation in the gate-drive circuit by half, without increasing power dissipation in the power circuit.

A circuit implementation of the quasi-resonant gate drive is shown in Fig. C.1(a). The gate-drive circuit consists of a single supply voltage, one switch, a
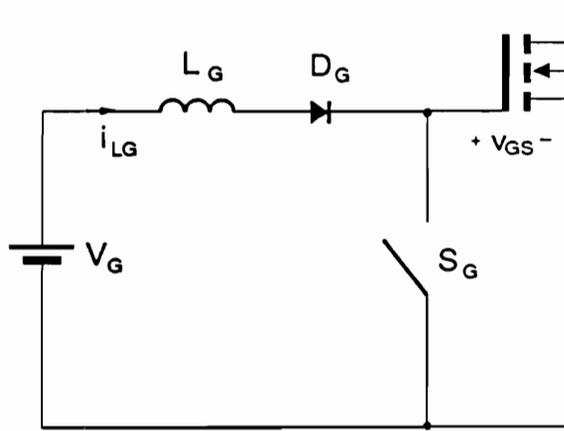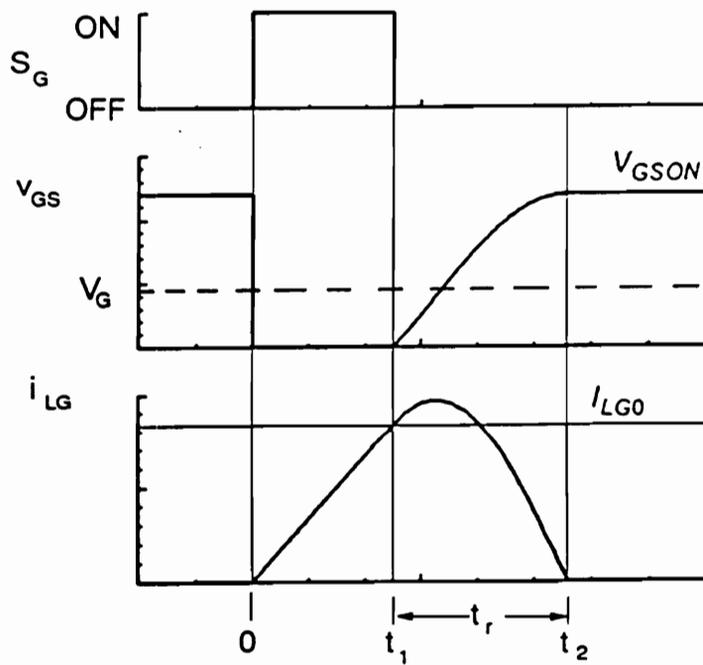
Figure C.1. Quasi-resonant gate drive: (a) Circuit diagram. (b) Theoretical waveforms.

diode, and a resonant inductor. When switch $S_G$ is on, the MOSFET is off, and voltage $V_G$ is applied to inductance $L_G$. During this stage, current in the inductance increases and eventually reaches at $t_1$ a value of:

$$I_{LG0} = \frac{V_G}{L_G} t_1 \quad , \tag{C.1}$$

as shown in Fig. C.1(b).

At $t_1$, $S_G$ turns off, and $L_G$ and $C_{iss}$ form a resonant circuit. During this stage of operation, the state equations are:

$$L_G \frac{di_{LG}}{dt} = V_G - v_{GS} \quad , \tag{C.2}$$

$$C_{GS} \frac{dv_{GS}}{dt} = i_{LG} \quad . \tag{C.3}$$

The time solutions are:

$$v_{GS}(t) = \omega_0 V_G t_1 \sin \omega_0(t - t_1) + V_G(1 - \cos \omega_0(t - t_1)) \quad , \tag{C.4}$$

$$i_G(t) = \frac{V_G t_1}{L_G} \cos \omega_0(t - t_1) + \frac{V_G}{Z_0} \sin \omega_0(t - t_1) \quad , \tag{C.5}$$

where

$$\omega_0 = \frac{1}{\sqrt{L_G C_{GS}}} \quad , \tag{C.6}$$

$$Z_0 = \sqrt{\frac{L_G}{C_{GS}}} \quad . \tag{C.7}$$

When current $i_{LG}$ reaches zero, resonance is stopped by diode $D_G$.

The rise time of the gate-to-source voltage (from zero to $V_{GSON}$) is:

$$\omega_0 t_r = \pi - \arctan\omega_0 t_1 \quad .$$ (C.8)

The gate-to-source voltage during on-time is:

$$\frac{V_{GSON}}{V_G} = \omega_0 t_1 \sin \omega_0 t_r + 1 - \cos \omega_0 t_r \quad .$$ (C.9)

Figure C.2(a) shows the relation between $t_r$ and $t_1$. Fig. C.2(b) shows $V_{GSON}$ as a function of $t_1$. It can be seen, from Fig. C.2(b), that the quasi-resonant gate drive boosts the input voltage. It should be noted, however, that the voltage gain depends only on $t_1$, and not on the switching frequency. As a result, $V_{GSON}$ is fixed in converters operating with constant off-time, such as ZVS-QRCs or ZVS-MRCs.

Due to the resonance of $L_G$ and $C_{iss}$, the loss of energy due to the charging of $C_{iss}$ is practically eliminated. The losses in the quasi-resonant gate drive consist mainly of the energy dissipated when $C_{iss}$ is abruptly discharged at turn-off. Ideally, power dissipation in the gate drive is reduced by approximately half, compared to conventional gate-drive circuits. However, this figure is reduced in practical circuits due to conduction losses in $S_G$ and $D_G$ and dissipation in the gate resistance of the MOSFET.

The concept of quasi-resonant gate drive was verified experimentally in the circuit shown in Fig. C.3(a). The measured gate-to-source voltage is shown in Fig. C.3(b). Power dissipation in the gate drive was approximately 0.31
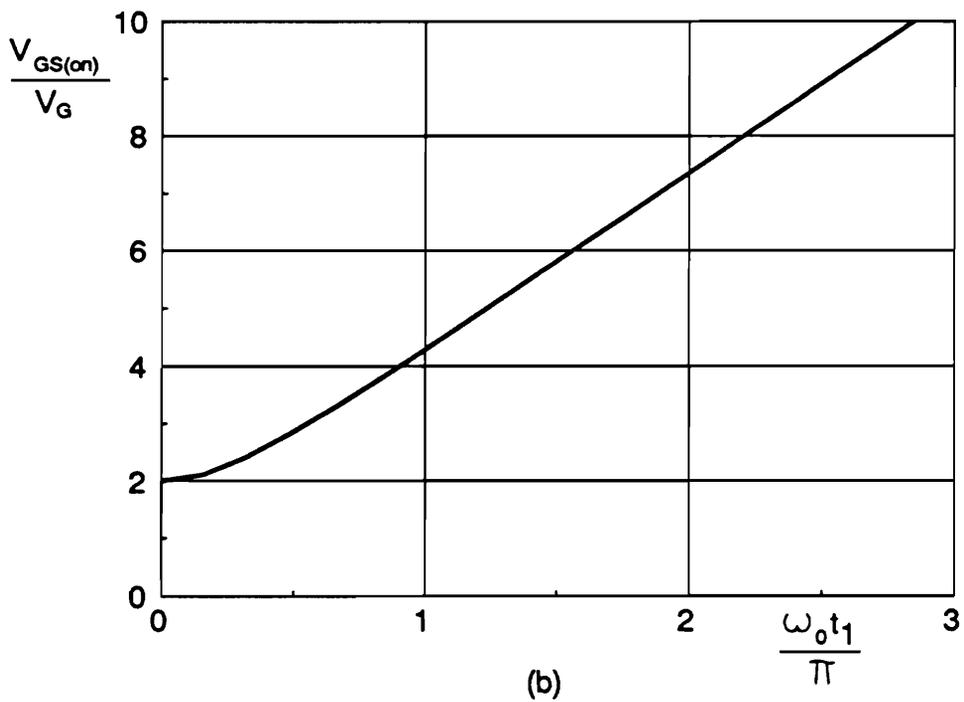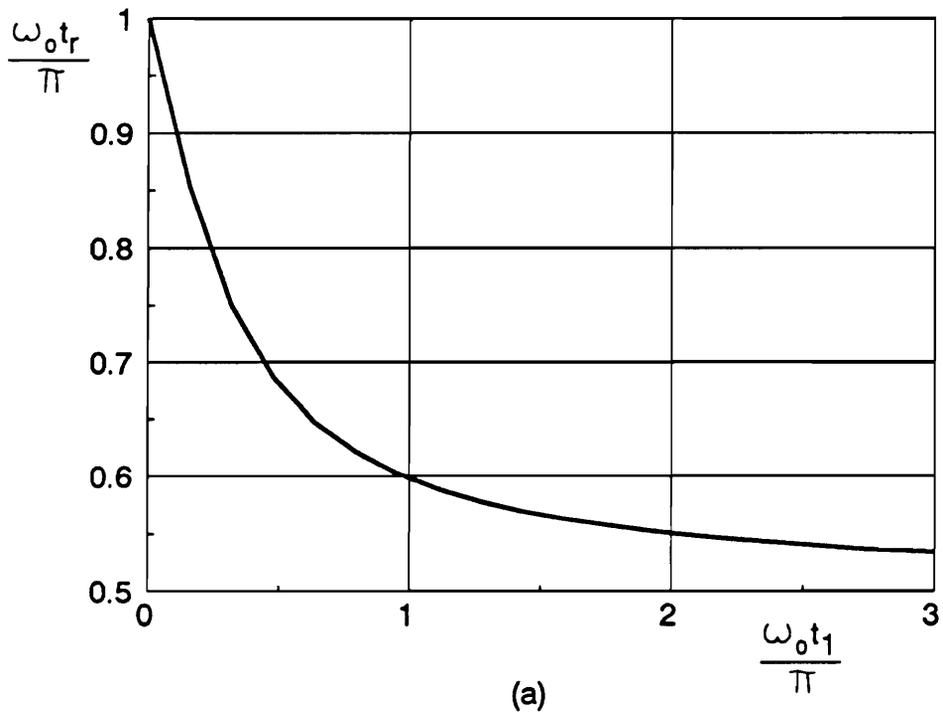
**Figure C.2.** Parameters of the quasi-resonant gate-drive: (a) Rise time of $V_{GS}$. (b) Voltage gain.
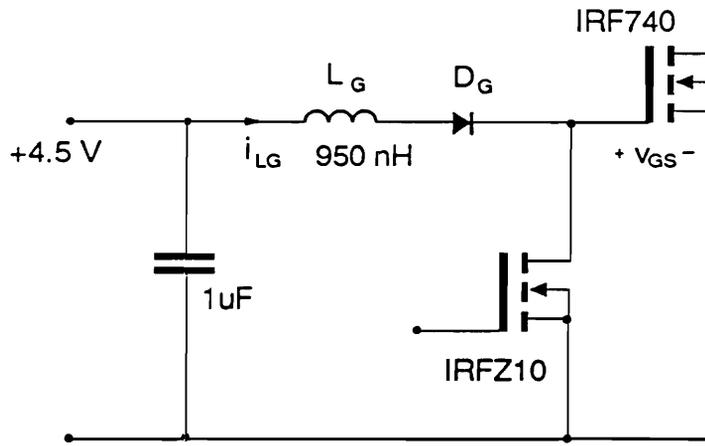
(a)
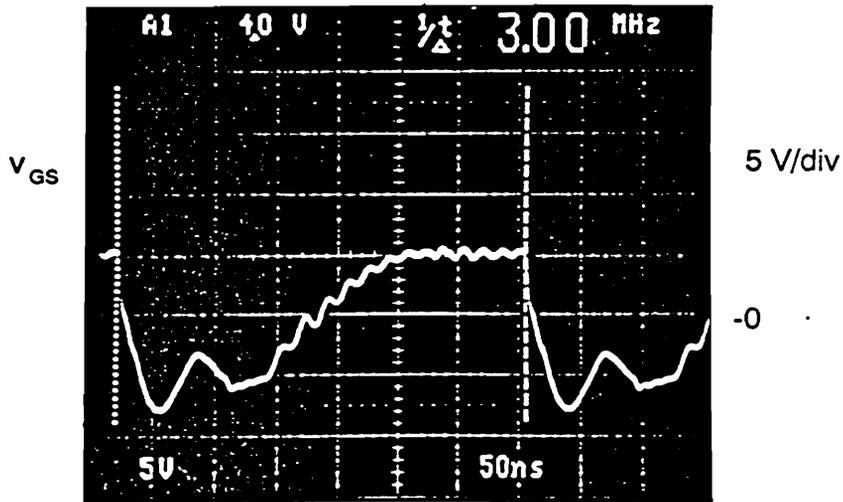


(b)

**Figure C.3.** **Experimental quasi-resonant gate drive: (a) Circuit diagram. (b) Measured $v_{GS}$**

W/MHz, which is only about 55% of the power dissipated in a classical totem-pole gate drive.

Figure C.4 shows a circuit diagram of a quasi-resonant gate drive designed for a 5 MHz, 50 W, forward ZVS-MRC for on-board applications [H19]. The power MOSFET, Q1, is driven by a GaAs BJT, Q2. The base drive for Q2 is implemented using five advanced-CMOS inverters in parallel.

Figure C.5(a) shows waveforms of the gate-to-source voltage and drain-to-source voltage of Q1. The resonant turn-on and very clean waveforms are evident. The GaAs transistor provides an excellent fall time, approximately 2.5 ns, as shown in Fig. C.5(b).
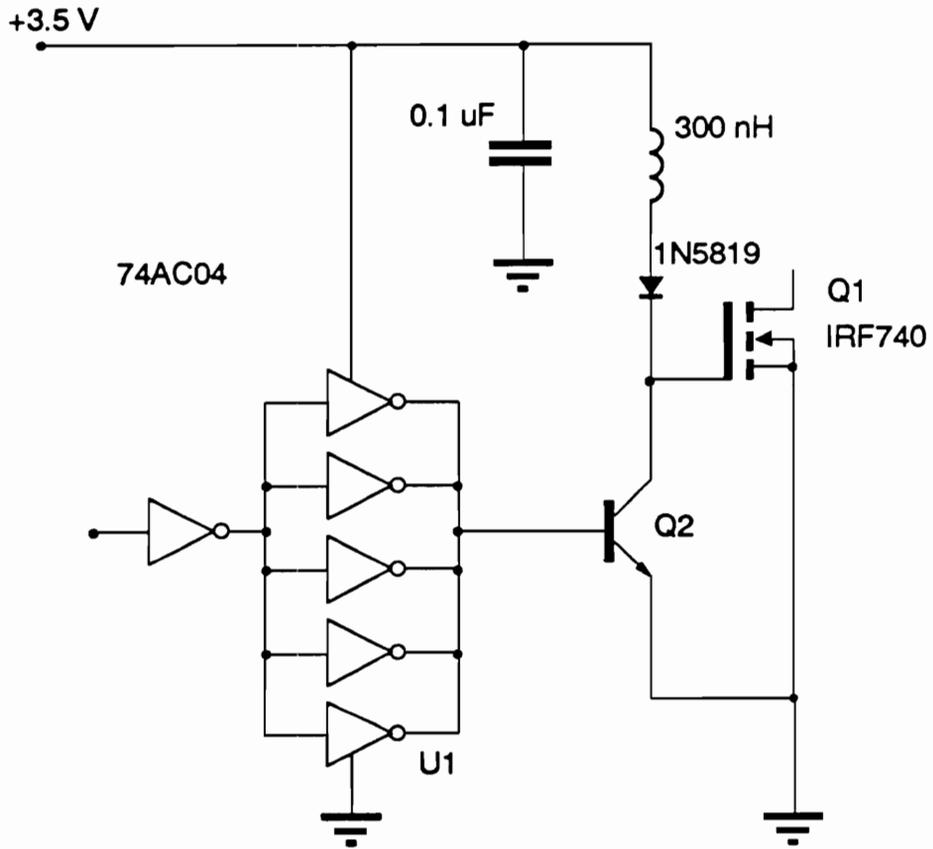
**Figure C.4.** Circuit diagram of a fast quasi-resonant gate drive.
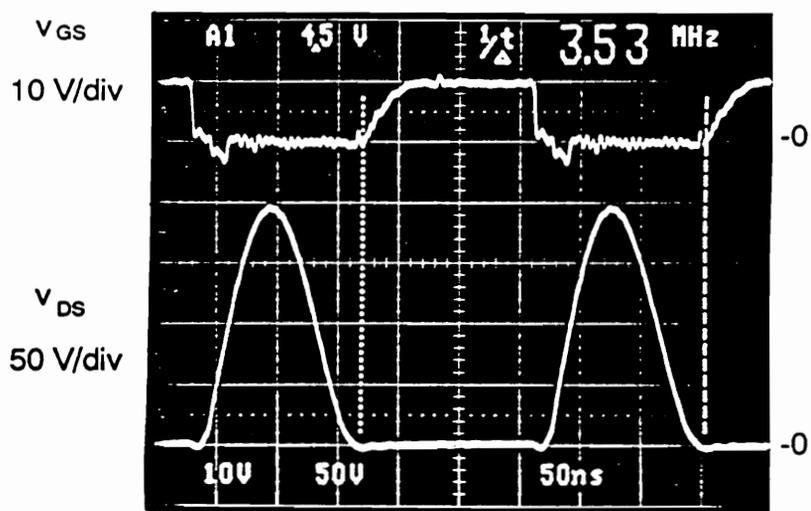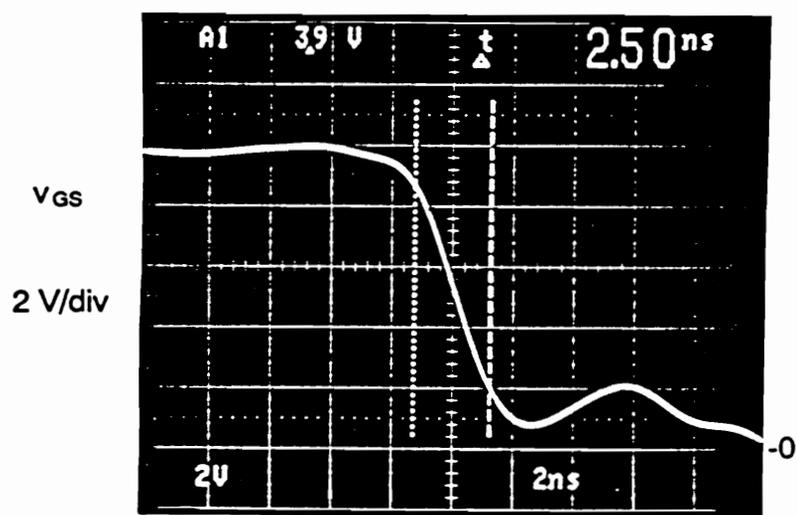
**Figure C.5.** Waveforms of the fast quasi-resonant gate drive: (a) Gate-to-source and drain-to-source voltage waveforms of Q1. (b) Gate-to-source voltage of Q1 with an expanded time scale.

# Appendix D. WINDING RESISTANCE OF A

# LOW-PROFILE TRANSFORMER

The winding arrangement is an important part of the design of any high-frequency transformer. Various winding configurations are examined here to establish an optimum winding structure for the low-profile transformer used in the on-board converter discussed in Chapter 6. The windings are combinations of Litz wire, solid wire, and foil. For each winding type, the total short-circuit resistance is calculated using the method presented in [M1, M32]. Theoretical predictions are compared to the measurements of the actual transformers.

Figure D.1 shows a general cross-sectional view of the low-profile transformer. The winding arrangement is formed by six turns of primary wire and two turns of secondary winding foil.

The first considered transformer, T1, uses a six-turn primary and a two-turn secondary, as illustrated in Fig. D.2(a). The winding arrangement of T1 is
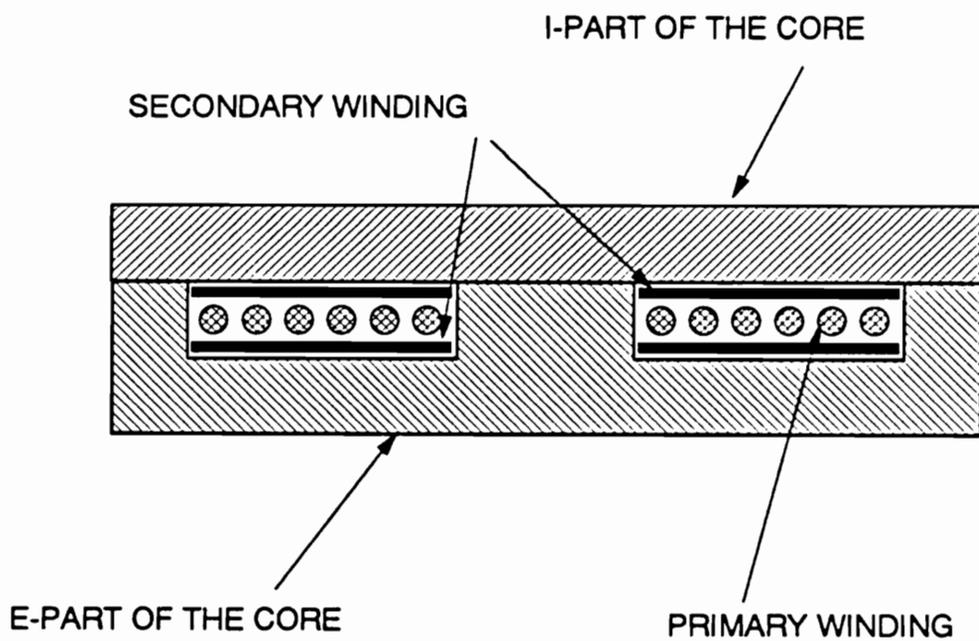
**Figure D.1.** **Cross-sectional view of the low-profile transformer.**
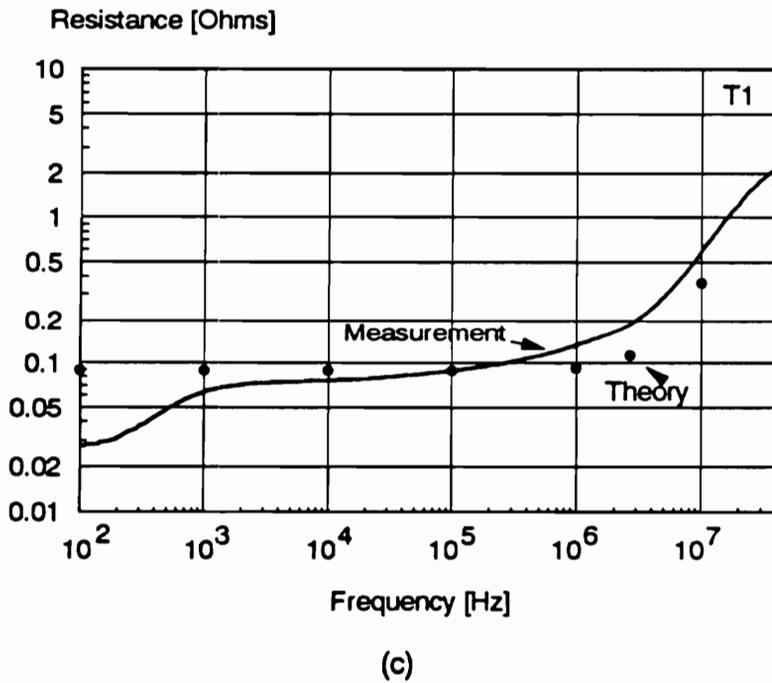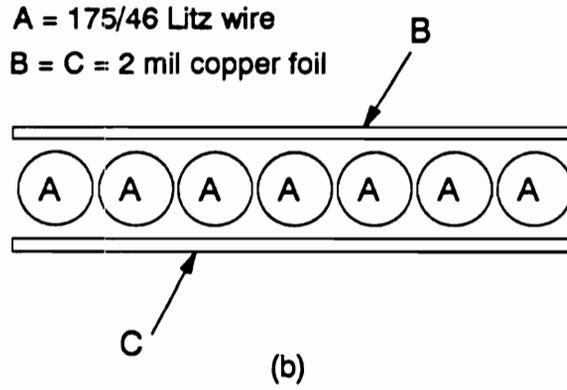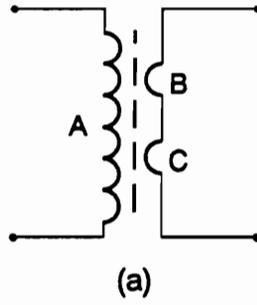
Figure D.2. Transformer T1: (a) Electrical winding configuration. (b) Physical winding arrangement. (c) Winding resistance.

shown in Fig. D.2(b). The primary winding is a 175/46 Litz wire in one layer sandwiched between the two turns of the secondary. The secondary winding is made of 2 mil copper foil. The thickness of the foil approximately equal to the skin depth at the operating frequency (1.7 mils at 2.7 MHz) is chosen. One skin depth is sufficient, since high-frequency currents flow only on one side of the foil, that facing the secondary winding. The advantage of this winding arrangement is its simple construction.

The theoretical values of the primary winding resistance, $R_{prim}$, the secondary winding resistance, $R_{sec}$, and the total winding resistance reflected to the primary, $R_{tot}$, are given in Table D.1. The measured and theoretical resistance of the winding is shown in Fig. D.2(c). This resistance represents the total winding resistance of the primary and secondary, measured on the primary side with the secondary winding shorted.

The predicted and measured resistances agree well in the mid-frequency range. In this range, the skin and proximity losses are negligible, and the resistance is essentially equal to the equivalent dc resistance of the primary and secondary windings. At low frequencies, the effect of finite magnetizing inductance can be observed. As the frequency is reduced, the magnetizing inductance starts shorting the secondary, and the resistance reduces to the resistance of the primary winding only.

At frequencies above 100 kHz, the proximity effects increase the resistance. The difference between the predicted and measured values is caused by nonideal field distribution in the window. Theoretical analysis assumes an ideal field distribution, shown in Fig. D.3(a). The idealized field lines are al-
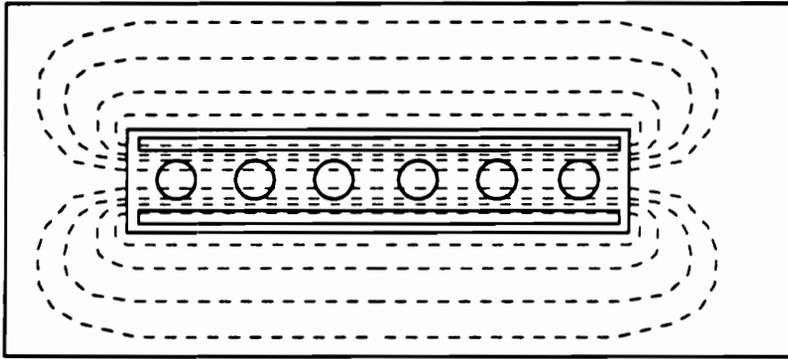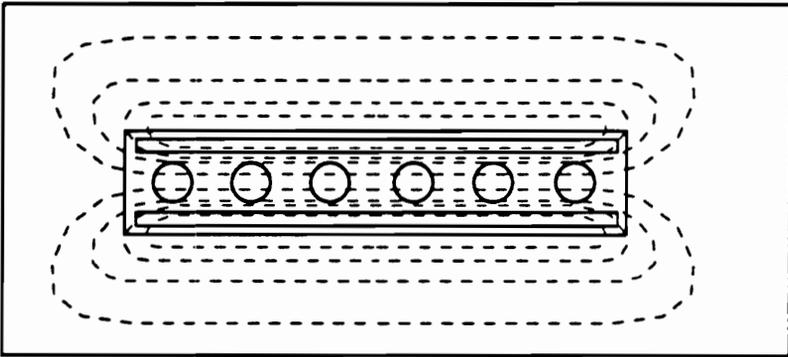
**Figure D.3.** **Magnetic field distribution in the transformer:** **(a) Idealized.** **(b) Practical.**

**Table D.1.   Theoretical winding resistance of T1.**

| $f$ | $R_{prim}$ | $R_{sec}$ | $R_1$ |
|:---:|:---:|:---:|:---:|
| [Hz] | [m$\Omega$] | [m$\Omega$] | [m$\Omega$] |
| 10 k | 25.7 | 7.02 | 88.9 |
| 100 k | 25.7 | 7.02 | 88.9 |
| 1 M | 27.8 | 7.23 | 92.9 |
| 2.7 M | 38.6 | 8.21 | 112.4 |
| 10 M | 220.5 | 15.72 | 362.0 |
| 40 M | 1390.9 | 32.57 | 1684.0 |

A = 175/46 Litz wire

B = C = 5 mil copper foil
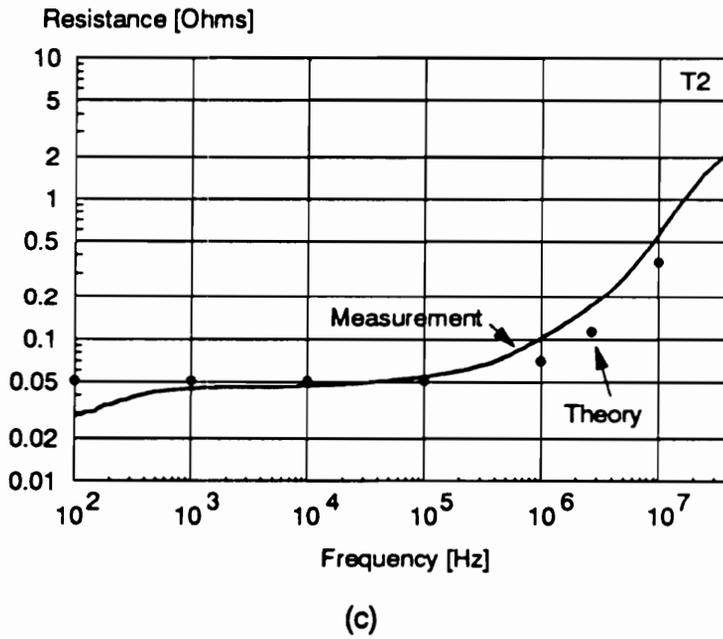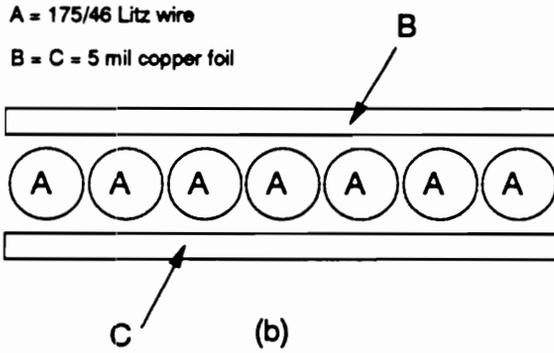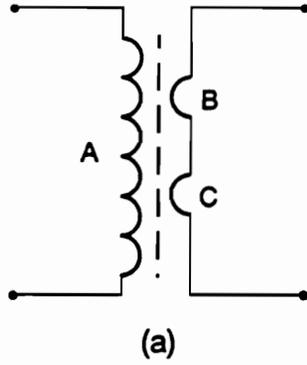
Resistance [Ohms]

**Figure D.4.** **Transformer T2: (a) Electrical winding configuration. (b) Physical winding arrangement. (c) Winding resistance.**

ways parallel to the winding layers. In practical situations, however, the field lines are distorted due to fringing effects [M9]. Typical distortion of the magnetic field in a practical transformer is depicted in Fig. D.3(b). The magnetic field at the edges of the winding has a component perpendicular to the surface of the winding layers. As a result, eddy currents are induced in the windings, particularly in the secondary foil winding. The losses due to these additional eddy currents are not accounted for in the analysis. This explains the difference between theoretical and actual measurements at high frequencies.

The winding arrangement of the second transformer, T2, is shown in Figs. D.4(a)-(b). The only difference between T2 and T1 is a thicker, 5 mil foil used for the secondary winding in T2. Theoretical values of winding resistances for T2 are given in Table D.2. The measured and predicted winding resistances of T2 are shown in Fig. D.4(c).

Figure D.5 shows a comparison of the measured winding resistances of T1 and T2. The low-frequency resistance of T2 is lower, due to the thicker foil used for the secondary winding in T2. As the frequency is increased, however, the skin depth, $\Delta$, becomes less than 5 mils ($\Delta$ = 5 mils at 300 kHz), resulting in a higher relative increase of the winding resistance in T2 than that in T1 (at 2 MHz, $\Delta$ = 2 mils). Beyond 2 MHz, both the 2 mil and 5 mil foils represent essentially the same resistance, since in both the available copper area is limited by the skin depth.

As mentioned previously, the fringing field causes additional losses in the foil conductor. Figure D.5 shows that thicker foil does not result in increased losses due to the fringing field. (High-frequency resistance is not affected by
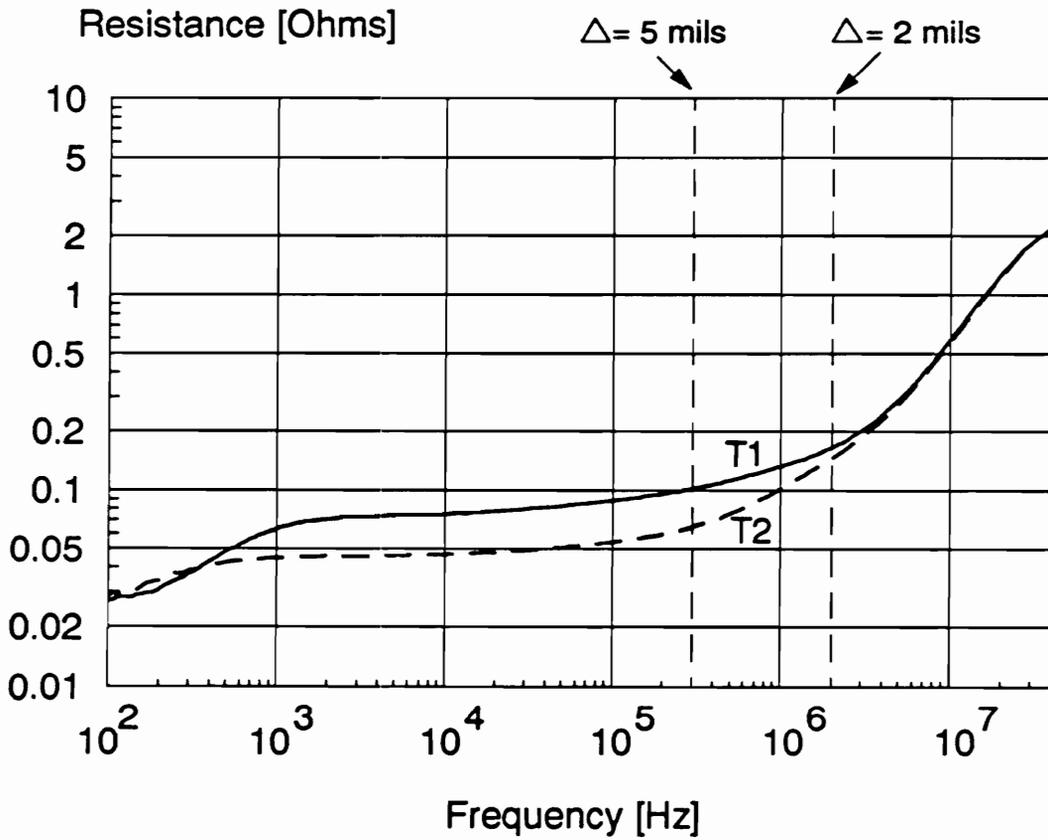
**Figure D.5.** Comparison of winding resistances of T1 and T2: A thicker foil in T2 reduces only the low-frequency resistance.

**Table D.2. Theoretical winding resistance of T2.**

| f | $R_{prim}$ | $R_{sec}$ | $R_1$ |
|:---:|:---:|:---:|:---:|
| [Hz] | [mΩ] | [mΩ] | [mΩ] |
| 10 k | 25.7 | 2.81 | 51.0 |
| 100 k | 25.7 | 2.81 | 51.0 |
| 1 M | 27.8 | 4.69 | 70.0 |
| 2.7 M | 38.6 | 8.23 | 112.6 |
| 10 M | 220.5 | 15.60 | 360.9 |
| 40 M | 1390.9 | 32.44 | 1682.8 |

A = AWG#20 Solid copper wire
B = C = 5 mil copper foil
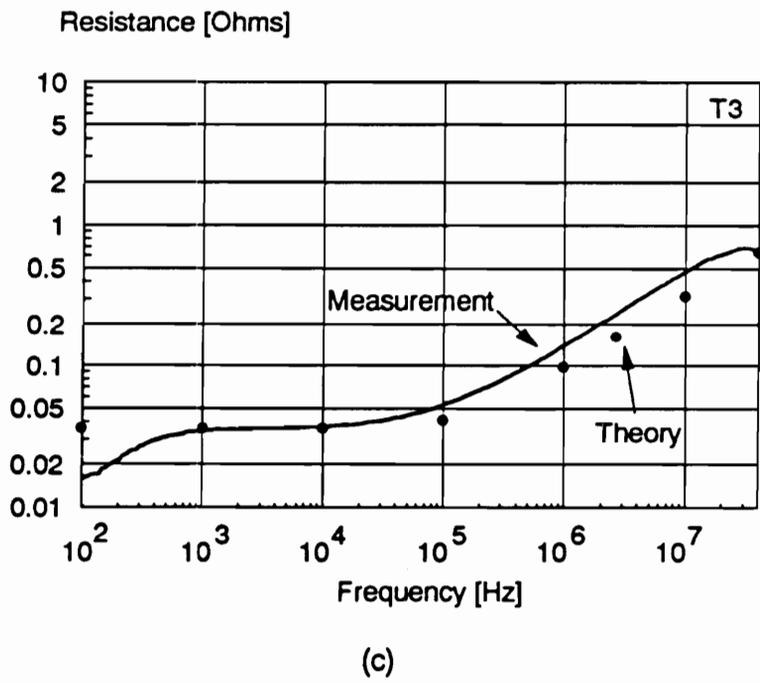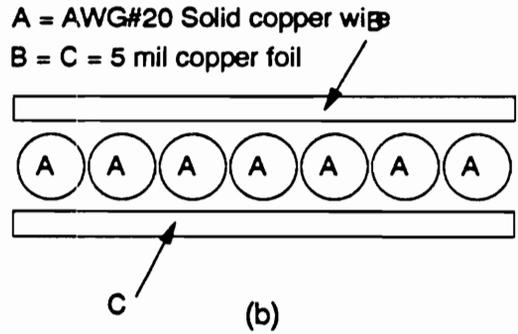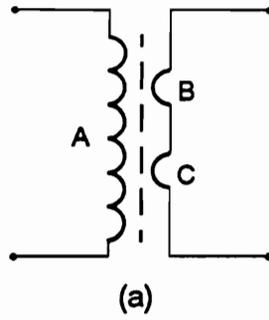
Figure D.6.   Transformer T3:   (a) Electrical winding configuration.   (b) Physical winding arrangement.  (c) Winding resistance.

the thickness of the foil.) This can be explained by the fact that the field cannot penetrate the foil much deeper than one skin depth. As a result, the fringing effect losses are essentially identical for any foil thicker than one skin depth.

To illustrate the difference between the performance of Litz wire and solid wire, transformer T3 was designed. The windings of T3 are shown in Figs. D.6(a)-(b). The winding arrangement and the secondary winding of T3 are identical to those of T2, but the primary winding uses a solid round wire, AWG#20. Theoretical values of the winding resistance of T3 are given in Table D.3. The measured and predicted winding resistances of T3 are shown in Fig. D.6(c). As in the case of T1 and T2, the low-frequency resistance is relatively well predicted, but the fringing effects cause discrepancy at high frequencies.

Figure D.7 compares the measured resistances of T2 and T3. The solid wire has a lower resistance at low frequencies, since the solid AWG#20 wire has a larger effective copper cross-sectional area than the 175/46 Litz wire. In the frequency range from 100 kHz to 10 MHz, however, Litz wire provides a clearly superior performance. At very high frequencies, above approximately 10 MHz, the solid wire results in a lower resistance than the Litz wire because when the wire diameter is much greater than the skin depth (case of the solid wire), the proximity effects are reduced compared to a situation where the wire diameter is comparable to the skin depth [M1]. (At 10 MHz, $d/\Delta = 1.5$ for the Litz wire and $d/\Delta = 37$ for the solid wire.)

As explained previously, the difference between the predicted and measured winding resistance at high frequencies is caused by fringing effects illustrated in Fig. D.3 and also shown in Fig. D.8. It can be deduced from Fig.
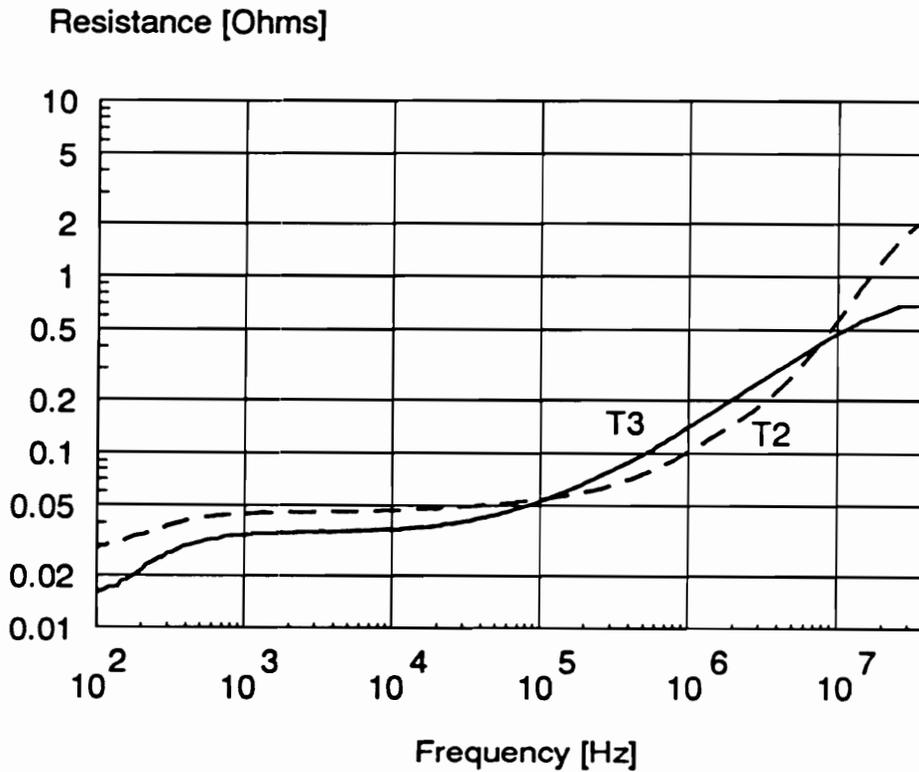
Resistance [Ohms]



**Figure D.7. Comparison of winding resistances of T2 and T3: Solid wire results in a lower winding resistance at low and very high frequencies, while Litz wire is better at frequencies above 100 kHz and below 10 MHz.**

**Table D.3. Theoretical winding resistance of T3.**

| f | $R_{prim}$ | $R_{sec}$ | $R_1$ |
|:---:|:---:|:---:|:---:|
| [Hz] | [mΩ] | [mΩ] | [mΩ] |
| 10 k | 10.8 | 2.81 | 36.1 |
| 100 k | 16.0 | 2.81 | 41.3 |
| 1 M | 55.7 | 4.69 | 98.0 |
| 2.7 M | 90.7 | 8.23 | 164.8 |
| 10 M | 177.4 | 15.60 | 317.8 |
| 40 M | 354.8 | 32.44 | 646.8 |

Litz wire inside

Foil outside

(a)

Litz wire outside

Foil inside

(b)
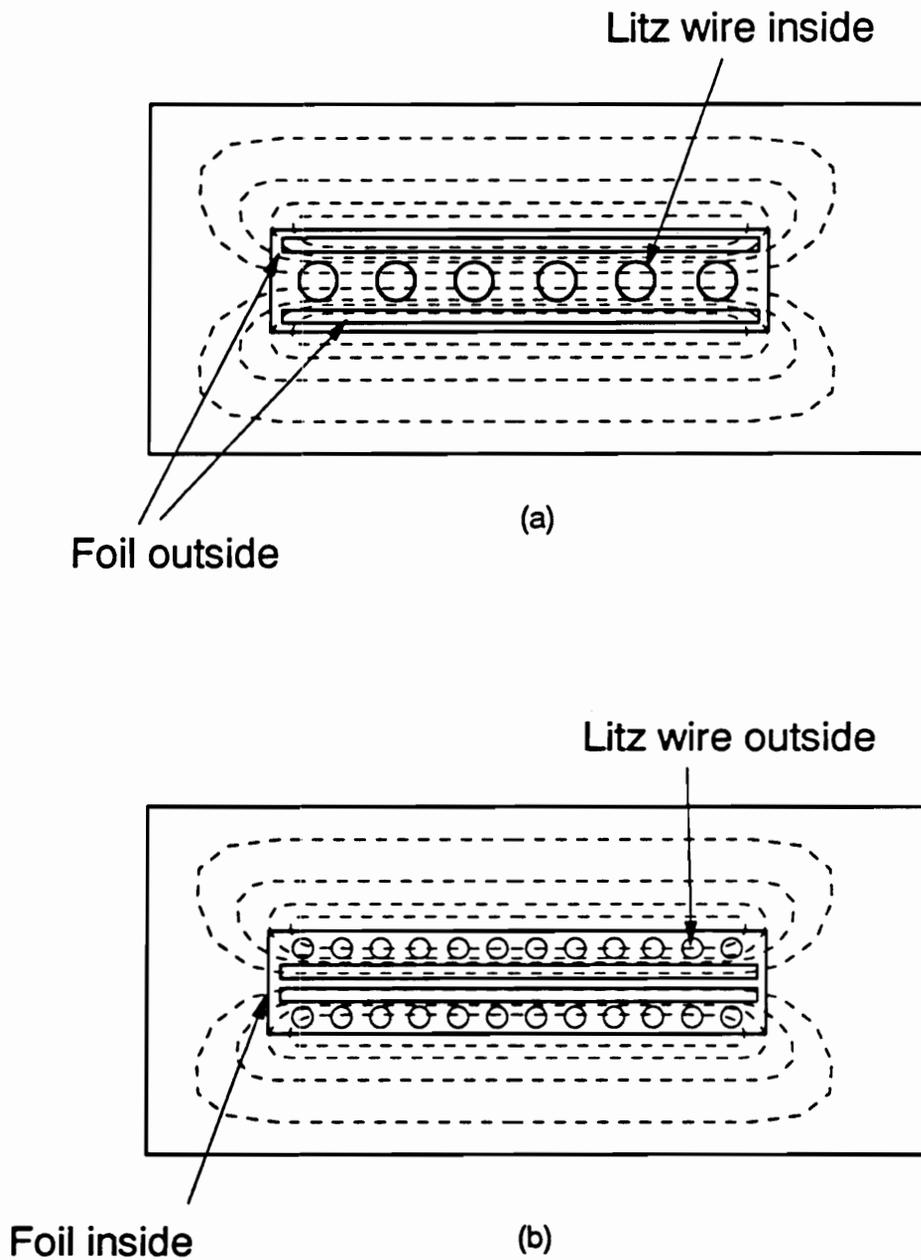
Figure D.8.   Rearrangement of windings to reduce fringing field losses: (a) Foil winding close to the perimeter of the window causes higher losses due to the fringing field. (b) Winding with foil moved towards the center of the window has reduced losses.

(a)
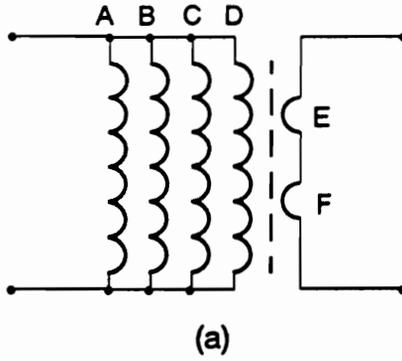
A = B = C = D = 40/46 Litz Wire

E = F = 2 mil copper foil



(b)

Resistance [Ohms]



Frequency [Hz]

(c)
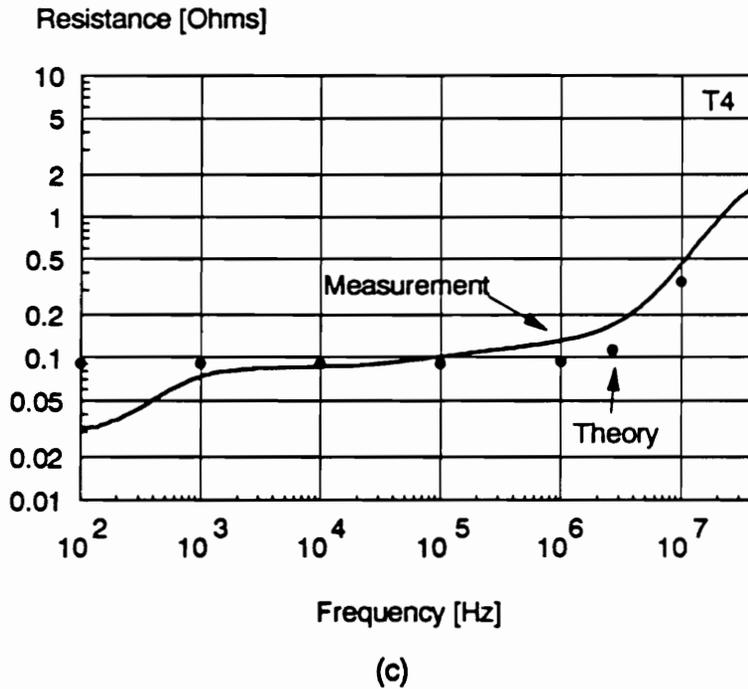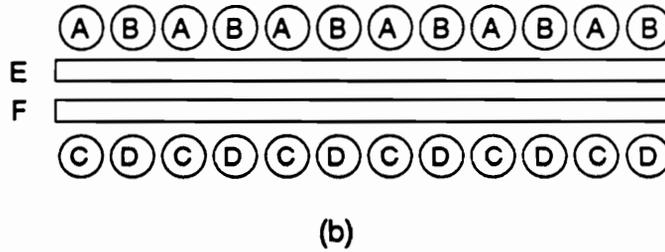
**Figure D.9.    Transformer T4:   (a) Electrical winding configuration.   (b) Physical winding arrangement.  (c) Winding resistance.**

**Table D.4.  Theoretical winding resistance of T4.**

| $f$ | $R_{prim}$ | $R_{sec}$ | $R_1$ |
|:---:|:---:|:---:|:---:|
| [Hz] | [mΩ] | [mΩ] | [mΩ] |
| 10 k | 28.2 | 7.02 | 91.4 |
| 100 k | 28.2 | 7.02 | 91.4 |
| 1 M | 30.2 | 7.23 | 95.2 |
| 2.7 M | 40.3 | 8.21 | 114.2 |
| 10 M | 207.6 | 15.72 | 349.0 |
| 40 M | 1410.0 | 32.57 | 1703.1 |

**Table D.5.  Theoretical winding resistance of T5.**

| $f$ | $R_{prim}$ | $R_{sec}$ | $R_1$ |
|:---:|:---:|:---:|:---:|
| [Hz] | [m$\Omega$] | [m$\Omega$] | [m$\Omega$] |
| 10 k | 12.5 | 2.81 | 37.8 |
| 100 k | 12.5 | 2.81 | 37.8 |
| 1 M | 18.3 | 2.95 | 44.8 |
| 2.7 M | 32.8 | 3.71 | 66.1 |
| 10 M | 62.5 | 8.12 | 135.6 |
| 40 M | 125.0 | 16.21 | 270.9 |

D.8(a) that the transverse component of the field is large near the corners of the window and vanishes in the plane parallel to the windings and located at half the height of the window. Since proximity losses are reduced by the use of bunched conductors, it seems logical to move the secondary foil windings towards the center of the window where the transverse field is reduced, and put the primary winding of Litz wire at the top and bottom of the window, as shown in Fig. D.8(b). Such a winding arrangement is used for transformer T4, as shown in Fig. D.9(b). To arrange a symmetrical structure of the windings, the primary winding is wound with four sections (A-D) of 40/46 Litz wire connected in parallel, as illustrated in Fig. D.9(a). Sections A and B are above, while sections C and D are below the secondary winding. The secondary winding is made of 2 mil copper foil.

Theoretical values of the winding resistance of T4 are given in Table D.4. The measured and predicted winding resistances of T4 are shown in Fig. D.9(c). It can be seen that despite the rearrangement of the winding, the difference between theory and measurement at higher frequencies is still significant. To determine whether switching the positions of the primary and secondary had any effect on the losses due to the fringing field, winding resistances of T1 and T4 are compared in Fig. D.10. In the low-frequency region, the winding resistance of T4 is slightly higher than that of T1 because of a lower number of strands in the primary winding of T4. The total number of strands in T4 is $4 \times 40 = 160$, while in T1 it is 175. This results in a slightly higher low-frequency winding resistance of T4.
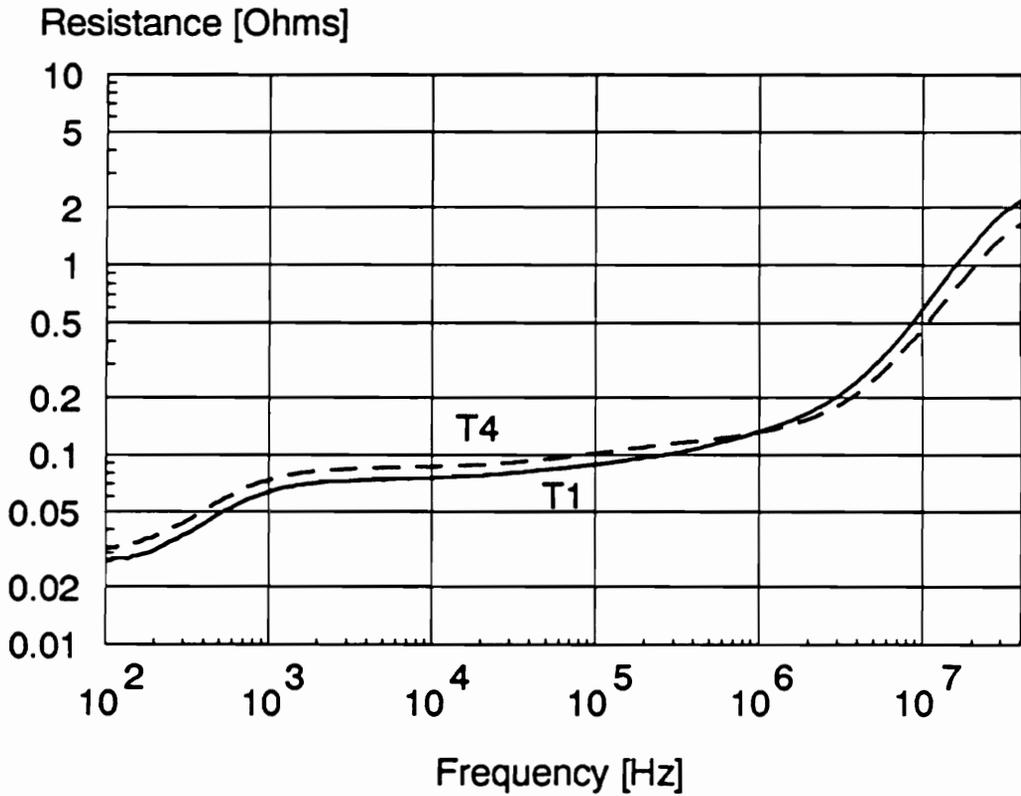
**Figure D.10.** Comparison of winding resistances of T1 and T4: When the foil winding is placed in the center of the window, the fringing effects in the foil are reduced, and the winding resistance is reduced at high frequencies.
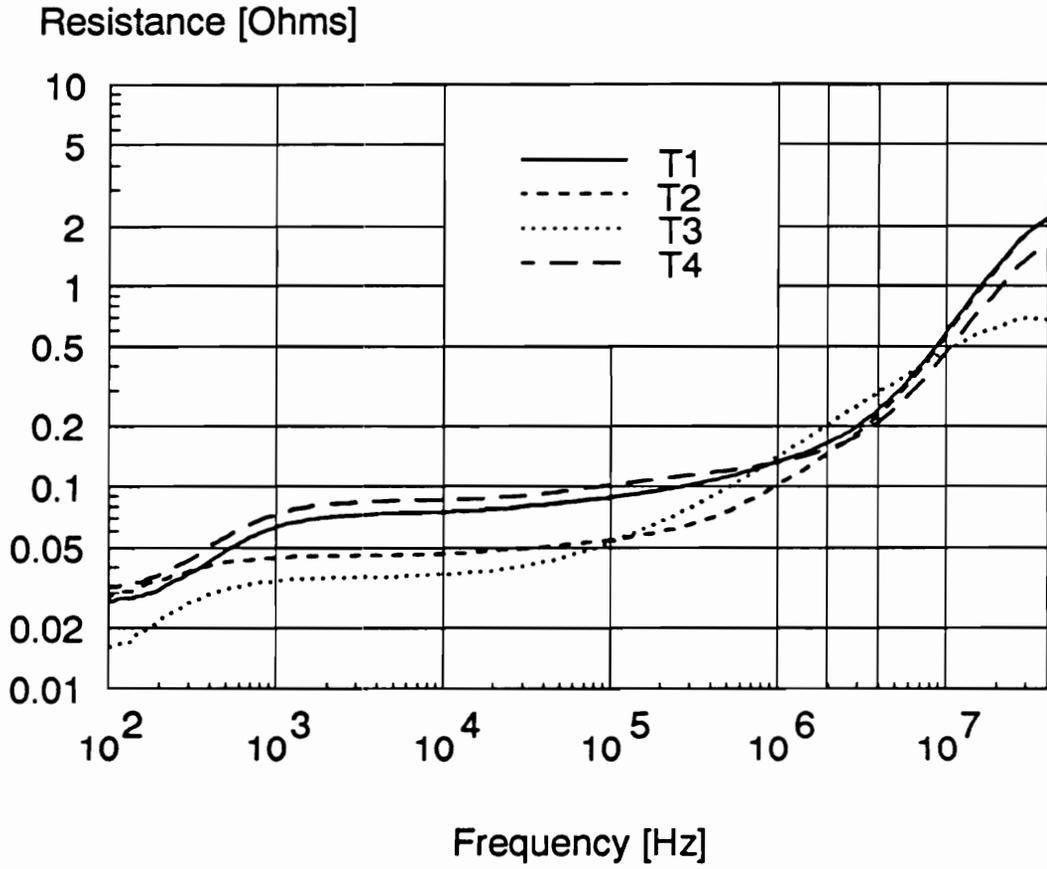
Resistance [Ohms]



Figure D.11. Comparison of winding resistances of transformers T1-T4

A   B   C   D



(a)
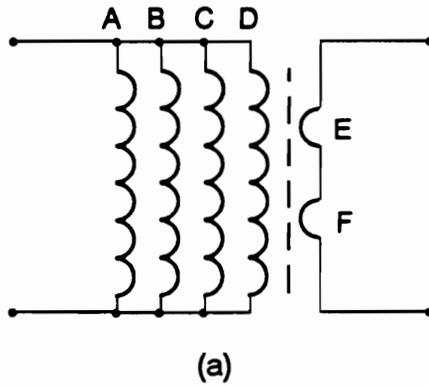
A = B = C = D = E = F = 5 mil copper foil



(b)
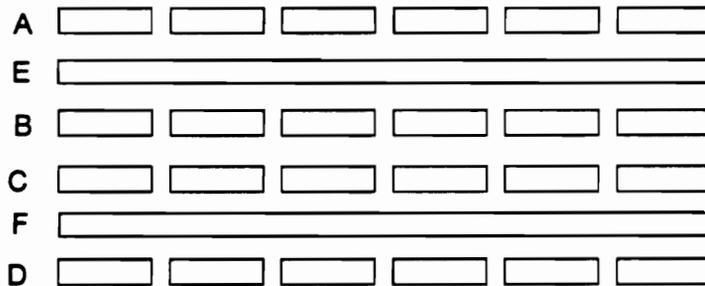
**Figure D.12.   Transformer T5:   (a) Electrical winding configuration.   (b) Physical winding arrangement.  (c) Winding resistance.**

In the high-frequency region, however, the winding resistance of T4 is lower than that of T1. This can be only attributed to the interchanged positions of the foil and Litz-wire windings, since both T1 and T4 use foil of identical thickness. Therefore, it has been verified that the loss due to fringing effects can be reduced by placing the foil winding in the middle of the window. However, the improvement is limited, since the winding resistance of the transformer with such an winding arrangement is still substantially higher than that predicted, as shown in Fig. D.9(c).

The measured winding resistances of the four investigated transformers are compared in Fig. D.11. The shaded area indicates the switching frequency range of the converter. As explained in Chapter 6, the switching frequency of this converter is in the approximate range of 2 to 4 MHz. At a full load of 10 A (50 W) and a nominal input voltage of 50 V, the switching frequency is 2.7 MHz. As can be seen from Fig. D.11, all the transformers with Litz-wire primary are essentially equivalent in the frequency range of interest. Transformer T3, which uses solid wire for the primary winding, has a higher resistance in the high-frequency region. Transformer T2 was chosen as the most practical for the on-board converter. T2 has a lower dc resistance of the secondary winding than both T1 and T4. This helps reduce losses due to the dc current in the secondary. In addition, the winding arrangement of T2 is much simpler to manufacture than that of T4.

Based on the considerations presented for transformers T1 through T4, one major conclusion is that the winding resistance is limited primarily by the resistance of the secondary winding. In these transformers, the winding struc-

ture forces the secondary winding current to flow on one side of the foil, that facing the primary winding. To reduce the high-frequency resistance of the secondary winding, it is necessary to arrange the windings so that the secondary current flows on both sides of the foil. This can be achieved by interleaving the secondary and primary windings. However, due to limited window height, this is difficult to achieve using Litz wire for the primary winding.

An alternative approach would be to use windings printed on flexible foil. One possible arrangement of the windings is shown in Figs. D.12(a-b). The primary consists of four six-turn spiral windings connected in parallel. Each turn of the secondary foil is sandwiched between two of the primary winding sections. As a result, the secondary current will flow on both sides of the secondary-winding foil and one side of the primary-winding foil. Table D.5 shows the theoretical winding resistance of this transformer. It can be seen that at 2.7 MHz, the theoretical winding resistance of T5 is almost two times lower than that of T1, T2, or T4. However, fabrication of such a winding is rather complicated, particularly with respect to the interconnections of the winding sections. Due to these practical difficulties, T5 has not been built for experimental verification.

To summarize, it has been shown that in the 100 kHz to 10 MHz frequency range, Litz wire provides lower winding resistance than solid wire. Use of foil winding causes losses attributed to fringing effects. These losses are not affected by the foil thickness (provided the foil is at least one skin depth thick). If the high-frequency current is confined to only one side of the foil, use of foil thicker than approximately 1.2 times the skin depth does not reduce the re-

sistance at the operating frequency. However, since a thicker foil does not cause increased losses due to the fringing effects, a thicker foil is recommended for applications with a substantial dc current. A design with a foil secondary winding sandwiched between spiral foil sections of the primary winding seems to be a good alternative, but is difficult to implement using conventional winding techniques.

# Appendix E. DEVICE MODELS FOR SYNCHRONOUS RECTIFIER ANALYSIS

To facilitate the analytical comparison of various rectifier schemes, only one type of Schottky rectifier and one type of MOSFET device are considered for the 50 W, 5 V output application. The diode chosen is a 60 A, 30 V dual Schottky center tap rectifier 60CNQ030 (International Rectifier). The MOSFET is an experimental 50 V DMOS FET device developed by General Electric [R4, S10]. The MOSFET was chosen for its superior on-resistance, input capacitance, and gate resistance.

### Diode Model

Figure E.1 shows the diode model used in the analysis. The Schottky rectifier is modeled by an ideal diode in series with voltage source, $V_f$, representing the forward voltage drop; a series resistance $R_{sch}$; and a nonlinear junction capacitance $C_j$. From the measured forward i-v characteristic of the diode (1/2 of the package), shown in Fig. E.2(a), $V_f = 0.34$ and $R_{sch} = 2$ m$\Omega$

The measured reverse leakage current is 0.1 mA at 15 V and is negligible in the loss analysis. Figure E.2(b) shows the junction capacitance, $C_j$, measured as a function of the reverse voltage. In the device model, $C_j$ is approximated by:

$$C_j = 10.6 \sqrt{\frac{\phi_{sch}}{\phi_{sch} + V_{sch}}} \quad [nF] \quad , \qquad (E.1)$$

where $\phi_{sch} = 0.5$ V. As can be seen from Fig. E.2(b), this expression provides a good approximation of the measured $C_j$.

### MOSFET Model

The model of the MOSFET device is shown in Fig. E.3. Fig. E.4 shows the measured i-v characteristics of the device operating in the third quadrant. In Table E.1 the on-resistance, $R_{ds}$, and conductance, $G_{ds} = 1/R_{ds}$, are shown as functions of the gate-to-source voltage. Since the device is intended for use in parallel with a Schottky diode and at 10 A load current, the on-resistance is measured at $- V_{ds} = 0.35$ V for drain currents less than 10 A, and at 10 A for $- V_{ds} < 0.35$ V.

The drain-to-source resistance, $R_{ds}$, is formed by a number of resistances in the device current path. The major components of $R_{ds}$ are listed in Table E.2 with their relative contributions in a fully on device at $V_{gs} = 10$ V. These relative contributions are approximated based on the data given for a 25 V device [S10], assuming that the 50 V device has a $2^{2.5}$ times higher resistance of the epitaxial layer. The resistances for the model of Fig. E.3 are obtained by assuming that $R_{cha}$ is formed by the channel and accumulation layer resistances,
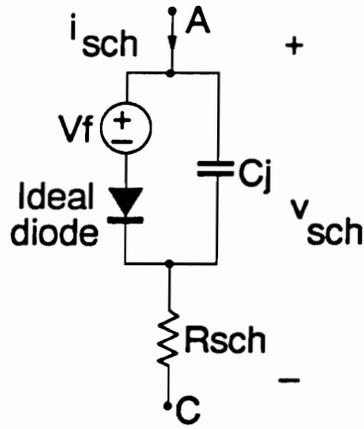
**Figure E.1.   Schottky diode circuit model.**
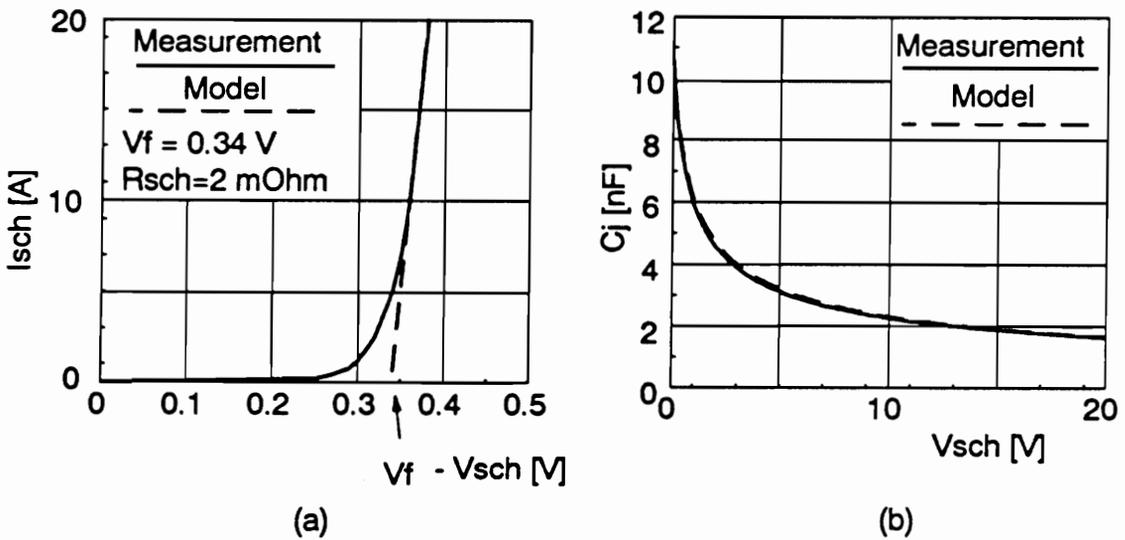


**Figure E.2.   Characteristics of the 60CNQ030 Schottky diode:   (a) Forward voltage drop.   (b) Junction capacitance vs. reverse voltage.**
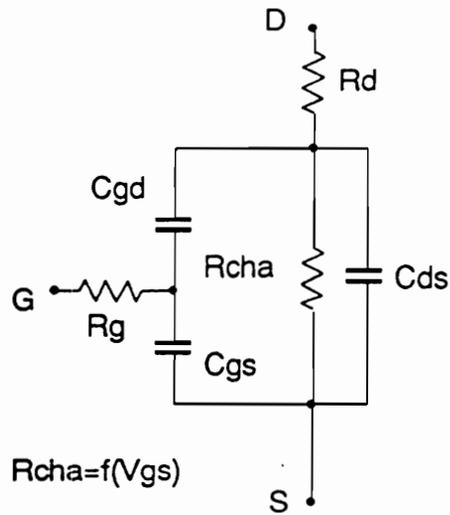
**Figure E.3.   MOSFET circuit model.**
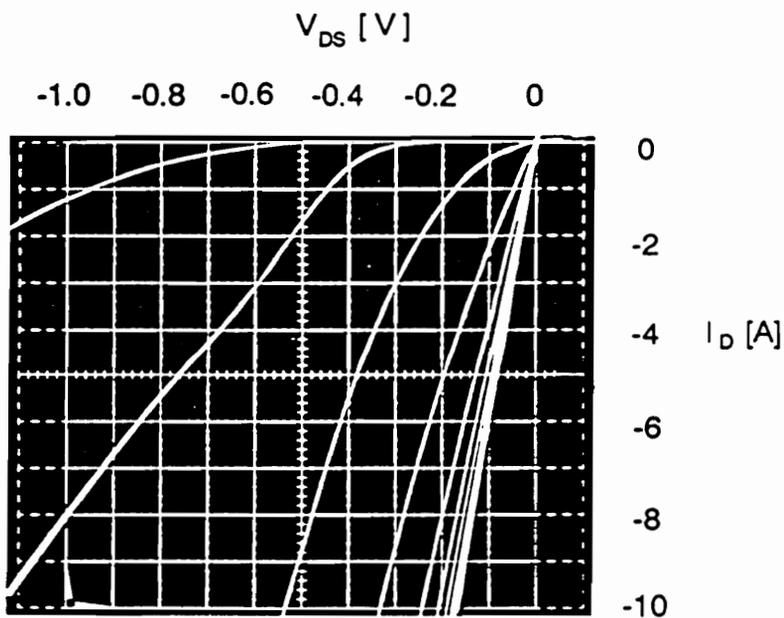


**Figure E.4.   Third quadrant i-v characteristics of the experimental GE MOSFET:   Vertically: 1 A/div. Horizontally: 0.1 V/div. Gate-to-source voltage: 1 to 10 V in 1 V steps.**

**Table E.1. MOSFET on-resistance as function of gate-to-source voltage.**

| Vgs | -Vds | -Id | Rds | Gds |
|-----|------|-----|-----|-----|
| [V] | [V] | [A] | [Ω] | [S] |
| 2.0 | 0.350 | 0.19 | 1.8400 | 0.54 |
| 2.5 | 0.350 | 1.26 | 0.2780 | 3.60 |
| 3.0 | 0.350 | 4.00 | 0.0875 | 11.43 |
| 3.5 | 0.350 | 7.20 | 0.0486 | 20.57 |
| 4.0 | 0.345 | 10.00 | 0.0345 | 28.99 |
| 4.5 | 0.289 | 10.00 | 0.0289 | 34.60 |
| 5.0 | 0.250 | 10.00 | 0.0250 | 40.00 |
| 6.0 | 0.210 | 10.00 | 0.0210 | 47.62 |
| 7.0 | 0.190 | 10.00 | 0.0190 | 52.63 |
| 8.0 | 0.180 | 10.00 | 0.0180 | 55.56 |
| 9.0 | 0.175 | 10.00 | 0.0175 | 57.14 |
| 10.0 | 0.170 | 10.00 | 0.0170 | 58.82 |

**Table E.2.    MOSFET on-resistance components.**

| Component | % of Rds(on) | Total % of Rds(on) | Circuit model |
|-----------|--------------|--------------------|--------------|
| Channel <br> Accumulation layer | 3 <br> 12 | 15 | Rcha <br> 2.5 m$\Omega$ |
| JFET region <br> Epitaxial layer <br> Substrate | 12 <br> 68 <br> 5 | 85 | Rd <br><br> 14.5 m$\Omega$ |

and $R_d$ is formed by the JFET region, epitaxial layer, and substrate. Since $R_{ds}$ of a fully on device is 17 m$\Omega$ at $V_{gs}$ = 10 V, $R_{cha}$ = 2.5 m$\Omega$ and $R_d$ = 14.5 m$\Omega$.

To complete the MOSFET device model, the values of the inter-electrode capacitances $C_{gs}$, $C_{gd}$, and $C_{ds}$ must be determined. The usual way of representing MOSFET input, output, and reverse capacitances as functions of the drain-to-source voltage (used in most data books) is not useful here, because each inter-electrode capacitance must be determined independently as a function of its own voltage. Therefore, a method is proposed allowing determination of the device capacitances based on a set of simple measurements. The first simplifying assumption in this method is that the gate-to-source capacitance is constant. This is approximately true in power MOSFET devices because the gate-to-source capacitance is formed by the gate/source overlap capacitance, the gate-channel capacitance, and the capacitance between the gate and source metallizations, and it is largely independent of bias [S20]. To determine capacitance $C_{gs}$, the input capacitance, $C_{iss}$, is measured at $V_{ds}$ = 50 V, as shown in Fig. E.5(a). At this bias condition, $C_{gd}$ and $C_{ds}$ have relatively small values, and it can be assumed that the contribution of the series combination of $C_{gd}$ and $C_{ds}$ to $C_{iss}$ is negligible, i.e., $C_{iss} \simeq C_{gs}$. The value of $C_{gs}$ acquired in this way is 890 pF. The exact value of $C_{gs}$ will be determined later, when the values of $C_{ds}$ and $C_{gd}$ are known.

Next, the gate-to-drain capacitance at $V_{gd} > 0$, $C_{gdp}$, is determined by measuring $C_{iss}$ as a function of the gate-to-source dc voltage at $V_{ds}$ = 0, as shown in Fig. E.5(b). The measured $C_{iss}$ is shown in Fig. E.6(a). Since we as-
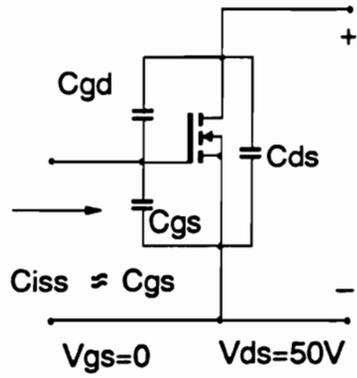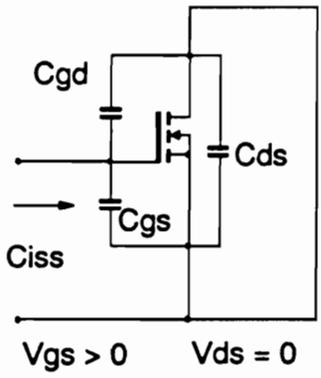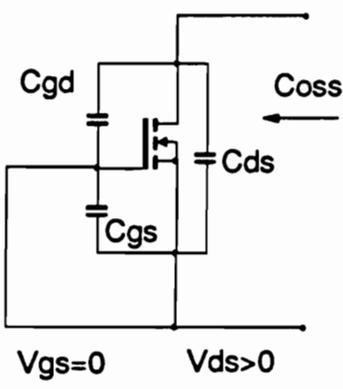
Figure E.5. Bias conditions for measurement of MOSFET capacitances: (a) Measurement of $C_{gs}$. (b) Measurement of $C_{gs} + C_{gdp}$. (c) Measurement of $C_{gdn} + C_{ds}$.
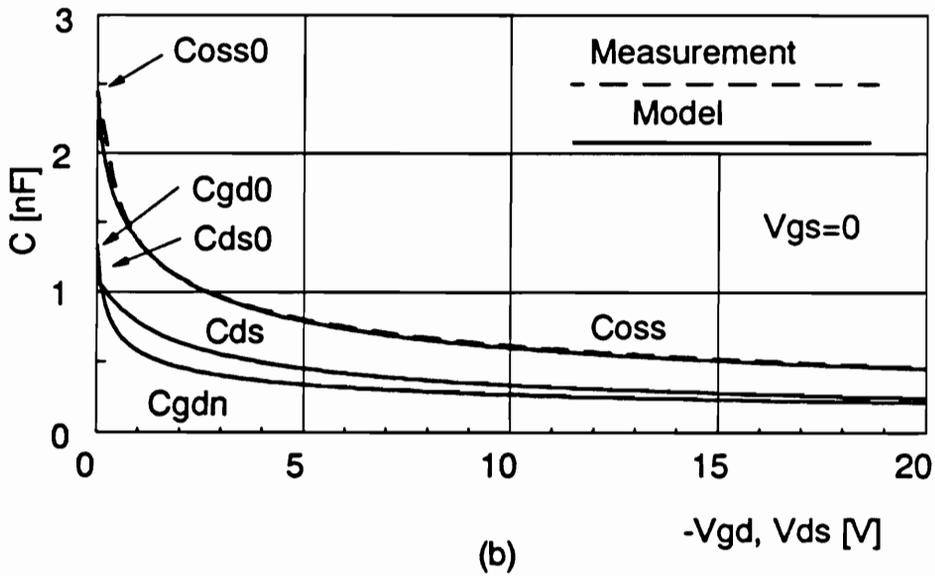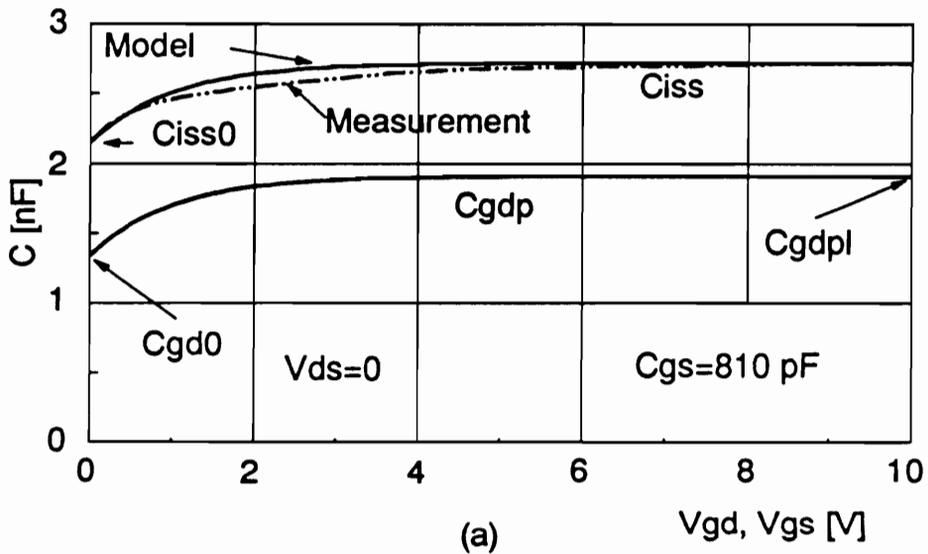
Figure E.6.  GE MOSFET capacitances:  (a) Input capacitance. (b) Output capacitance.

sumed a constant $C_{gs}$, $C_{gdp} = C_{iss} - C_{gs}$. To model the nonlinearity of $C_{gdp}$, the following function is used:

$$C_{gdp} = C_{gdpl} - (C_{gdpl} - C_{gd0})e^{-V_{gd}} \quad , \tag{E.2}$$

where $C_{gdpl} = C_{iss}(V_{gd} = 10V) - C_{gs} = 2.15\text{nF} - 0.89\text{nF} = 1.26$ nF is the gate-to-drain capacitance in the plateau region, and $C_{gd0} = 1.26$ nF is $C_{gdp}$ at $V_{gd} = 0$ V.

To determine the drain-to-source capacitance, $C_{ds}$, and the gate-to-drain capacitance at $V_{gd} < 0$, $C_{gdn}$, the output capacitance, $C_{oss}$, is measured as a function of $V_{ds}$ at $V_{gs} = 0$, as shown in Fig. E.5(c). Since $C_{ds}$ is essentially a capacitance of the p-n body diode, it can be approximated by:

$$C_{ds} = C_{ds0}\sqrt{\frac{\phi_{ds}}{\phi_{ds} + V_{ds}}} \quad , \tag{E.3}$$

where $C_{ds0}$ is $C_{ds}$ at $V_{ds} = 0$. The value of $\phi_{ds}$ is determined by the manufacturing process and device design, but for most practical purposes it can be assumed to be 1 V. Since $C_{gd0}$ has been already determined, the value of $C_{ds0}$ is easily found as $C_{oss0} - C_{gd0}$; $C_{ds0} = 2.45$ nF - 1.26 nF = 1.19 nF.

Now $C_{gdn}$ is determined as $C_{oss} - C_{ds}$ and plotted as a function of $V_{ds}$. An expression approximating $C_{gdn}$ is found by curve fitting on a computerized impedance analyzer:

$$C_{gdn} = C_{gd0}\left(\frac{0.1}{0.1 - V_{gd}}\right)^{0.35} \quad . \tag{E.4}$$

The model can be now refined by calculating the equivalent capacitance, $C_{eq}$, representing the series combination of $C_{gdn}$ and $C_{ds}$, both biased at $V_{ds} = V_{gd} = 50$ V. From (3) and (4), $C_{eq} = 80$ pF. Therefore, the refined value of the gate-to-source capacitance is $C_{gs} = 890$ pF - 80 pF = 810 pF. Consequently, $C_{gd0} = C_{iss0} - C_{gs} = 1.34$ nF, $C_{gdpl} = C_{iss}(V_{gs} = 10V) - C_{gs} = 1.91$ nF, and $C_{ds0} = C_{oss0} - C_{gd0} = 1.11$ nF. The refined model is summarized in Table E.3, and the resulting capacitance curves are shown in Fig. E.6.

## Table E.3. MOSFET capacitance model.

$$C_{gs} = 0.81 \text{ nF}$$

$$C_{gdp} = C_{gdpl} - (C_{gdpl} - C_{gd0})e^{-V_{gd}}, \quad V_{gd} > 0$$

$$C_{gdn} = C_{gd0}\left(\frac{0.1}{0.1 - V_{gd}}\right)^{0.35}, \quad\quad V_{gd} < 0$$

$$C_{ds} = C_{ds0}\sqrt{\frac{1}{1 + V_{ds}}}$$

$$C_{gd0} = 1.34 \text{ nF} \quad C_{gdpl} = 1.91 \text{ nF} \quad C_{ds0} = 1.11 \text{ nF}$$

# Appendix F. MATHCAD PROGRAMS FOR LOSS

# ANALYSIS OF SYNCHRONOUS RECTIFIERS

```
----------------------------------------------------------------------
                    PWM RECTIFIER
----------------------------------------------------------------------
```

$i := 0 .. 10$ $\qquad f_i := 1 \cdot i \cdot 10^6 \qquad w := 2 \cdot \pi \cdot f$

```
----------------------------------------------------------------------
```
APPLICATION SPECS: $\qquad Vo := 5 \qquad Io := 10 \qquad Po := Io \cdot Vo$
```
----------------------------------------------------------------------
```
MOSFET TYPE: GE-50V
```
----------------------------------------------------------------------
```

$n := 1$

$Cgs := n \cdot 0.81 \cdot 10^{-9} \qquad Cgdp1 := n \cdot 1.91 \cdot 10^{-9} \qquad Cgd0 := n \cdot 1.34 \cdot 10^{-9}$

$Rdson_3 := \dfrac{0.0875}{n}$

$Rdson_4 := \dfrac{0.0345}{n}$ $\qquad m := 3 .. 10 \qquad Vgson_m := (m)$

$Rdson_5 := \dfrac{0.025}{n}$ $\qquad \phi gd := 0.1$

$Rdson_6 := \dfrac{0.021}{n}$ $\qquad Cgdn(v) := Cgd0 \cdot \left[ \dfrac{\phi gd}{\phi gd + v} \right]^{0.35}$

$Rdson_7 := \dfrac{0.019}{n}$ $\qquad Cgdp(v) := Cgdp1 - (Cgdp1 - Cgd0) \cdot \exp(-v)$

$Rdson_8 := \dfrac{0.018}{n}$ $\qquad \phi ds := 1$

$Rdson_9 := \dfrac{0.0175}{n}$ $\qquad Cds0 := n \cdot 1.11 \cdot 10^{-9}$

$Rdson_{10} := \dfrac{0.017}{n}$ $\qquad Cds(v) := Cds0 \cdot \left[ \dfrac{\phi ds}{\phi ds + v} \right]^{0.5}$

$u := 0, 1 .. 20$

$Pon_{m,i} := Io^2 \cdot Rdson_m$

$Pgs_{m,i} := 2 \cdot Cgs \cdot Vgson_m^2 \cdot f_i$

$Cds(u), Cgdp(u), Cgdn(u)$

$Pgdp_{m,i} := 2 \cdot f_i \cdot \left[ Vgson_m + 2 \cdot Vo \right] \cdot \displaystyle\int_0^{Vgson_m} Cgdp(v)\, dv$

$Pgdn_{m,i} := 2 \cdot f_i \cdot \left[ Vgson_m + 2 \cdot Vo \right] \cdot \displaystyle\int_0^{2 \cdot Vo} Cgdn(v)\, dv$
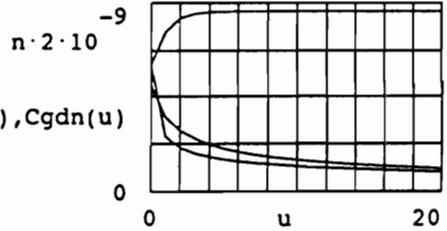
$$Pds_{m,i} := 4 \cdot Vo \cdot f_i \cdot \int_0^{2 \cdot Vo} Cds(v) \, dv$$

$$P := Pon + Pgs + Pgdp + Pgdn + Pds$$

$$E_{m,i} := \frac{Po}{Po + P_{m,i}}$$

$E_{(3,i)}, E_{(4,i)}, E_{(5,i)}, E_{(6,i)}, E_{(7,i)}, E_{(8,i)}, E_{(9,i)}, E_{(10,i)}$
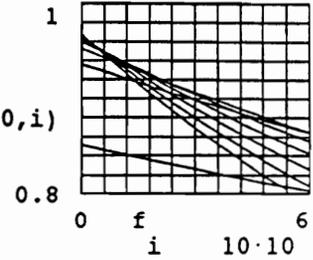


$$Eout_{i,0} := E_{3,i} \qquad\qquad Eout_{i,4} := E_{7,i}$$

$$Eout_{i,1} := E_{4,i} \qquad\qquad Eout_{i,5} := E_{8,i}$$

$$Eout_{i,2} := E_{5,i} \qquad\qquad Eout_{i,6} := E_{9,i}$$

$$Eout_{i,3} := E_{6,i}$$

$$Eout := augment(f, Eout)$$

$$Eout =$$

| | | | | | | |
|---|---|---|---|---|---|---|
| 0 | 0.851 | 0.935 | 0.952 | 0.96 | 0.963 | 0.965 | 0.966 |
| $1 \cdot 10^6$ | 0.846 | 0.928 | 0.943 | 0.948 | 0.95 | 0.949 | 0.948 |
| $2 \cdot 10^6$ | 0.841 | 0.92 | 0.933 | 0.937 | 0.936 | 0.934 | 0.93 |
| $3 \cdot 10^6$ | 0.836 | 0.913 | 0.924 | 0.926 | 0.923 | 0.919 | 0.912 |
| $4 \cdot 10^6$ | 0.831 | 0.906 | 0.915 | 0.915 | 0.911 | 0.904 | 0.896 |
| $5 \cdot 10^6$ | 0.826 | 0.899 | 0.907 | 0.905 | 0.898 | 0.89 | 0.88 |
| $6 \cdot 10^6$ | 0.821 | 0.892 | 0.898 | 0.894 | 0.886 | 0.876 | 0.864 |
| $7 \cdot 10^6$ | 0.817 | 0.885 | 0.889 | 0.884 | 0.875 | 0.863 | 0.85 |
| $8 \cdot 10^6$ | 0.812 | 0.878 | 0.881 | 0.874 | 0.863 | 0.85 | 0.835 |
| $9 \cdot 10^6$ | 0.807 | 0.871 | 0.873 | 0.865 | 0.852 | 0.838 | 0.821 |
| $1 \cdot 10^7$ | 0.803 | 0.865 | 0.865 | 0.855 | 0.842 | 0.825 | 0.808 |

$$WRITEPRN(out) := Eout$$

```
-----------------------------------------------------------------------
                    RESONANT SYNCHRONOUS RECTIFIER
                  PRECISE MODEL USING NUMERICAL INTEGRATION
-----------------------------------------------------------------------
```

$$i := 0 .. 20$$

FREQUENCY
RANGE
$$f_i := 1 \cdot i \cdot 10^6 \qquad\qquad \text{TOL} := 1$$

Integration
tolerance

$$w := 2 \cdot \pi \cdot f$$

```
-----------------------------------------------------------------------
```

APPLICATION SPECS:    $Vo := 5$      $Io := 10$

$$A(wt,i) := w_i \cdot x \cdot Vo \cdot \cos(wt) \qquad v(wt) := x \cdot Vo \cdot \sin(wt)$$

```
-----------------------------------------------------------------------
```

MOSFET TYPE: GE-50V

```
-----------------------------------------------------------------------
```

$$n := 1 .. 5$$

$$Rch(n) := \frac{0.0025}{n} \qquad\qquad Cgs(n) := n \cdot 0.81 \cdot 10^{-9}$$

$$Cgd0 := 1.34 \cdot 10^{-9}$$

$$Rd(n) := \frac{0.0145}{n} \qquad\qquad Cgdplateau := 1.91 \cdot 10^{-9} \qquad \phi gd := 0.1$$

$$Cds0 := 1.11 \cdot 10^{-9} \qquad \phi ds := 1$$

$$Rg(n) := \frac{0.25}{n}$$

$$Cgdp(wt,n) := n \cdot (Cgdplateau - (Cgdplateau - Cgd0) \cdot \exp(-v(wt)))$$

$$Cds(wt,n) := n \cdot Cds0 \cdot \sqrt{\frac{\phi ds}{\phi ds + v(wt)}} \qquad\qquad Cgdn(wt,n) := n \cdot Cgd0 \cdot \sqrt{\frac{\phi gd}{v(wt) + \phi gd}}$$

$$Vtsr_1 := 4.8 \qquad Vtsr_3 := 3.25$$
$$Vtsr_2 := 3.6 \qquad Vtsr_4 := 3.1 \qquad Vtsr_5 := 2.9$$

```
-----------------------------------------------------------------------
```

DIODE TYPE: 60CNQ030

```
-----------------------------------------------------------------------
```

$$Rsch := 0.002 \qquad \phi d := 0.5$$
$$Vf := 0.34 \qquad\qquad\qquad Cj0 := 10.6 \cdot 10^{-9}$$

$$Cj(wt) := Cj0 \cdot \sqrt{\frac{\phi d}{v(wt) + \phi d}}$$

```
-----------------------------------------------------------------------
```

$$wtl(n) := \operatorname{asin}\left[\frac{Vtsr_n}{\pi \cdot Vo}\right] \qquad rmst(f,i,a,b,n) := \frac{1}{2 \cdot \pi} \cdot \int_a^b f(wt,i,n)^2 \, dwt$$

```
-----------------------------------------------------------------------
```

$$Cx1(wt,n) := Cgs(n) + Cds(wt,n) + Cj(wt)$$
$$Cx2(wt,n) := Cgdn(wt,n) + Cds(wt,n)$$
$$Cx3(wt,n) := Cgdp(wt,n) + Cgs(n) + Cds(wt,n) + Cj(wt)$$
$$Cx4(wt,n) := Cds(wt,n) + Cj(wt)$$
$$Cx5(wt,n) := Cgdp(wt,n) + Cgs(n)$$

```
--------------------------------------------------------------------
ischl(wt,i,n) := A(wt,i)'Cxl(wt,n)
Ischl%(n,i) := rms%(ischl,i,0,π,n) - rms%(ischl,i,wtl(n),π - wtl(n),n)
isch2(wt,i,n) := A(wt,i)'Cj(wt)
Isch2%(n,i) := rms%(isch2,i,0,π,n)
                 2 wtl(n)
Isch%(n,i) := Io '————————— + Ischl%(n,i) + Isch2%(n,i)
                    π
--------------------------------------------------------------------
idl(wt,i,n) := A(wt,i)'Cgdp(wt,n)
Idl%(n,i) := rms%(idl,i,0,π,n) - rms%(idl,i,wtl(n),π - wtl(n),n)
id2(wt,i,n) := A(wt,i)'Cx3(wt,n)
Id2%(n,i) := rms%(id2,i,wtl(n),π - wtl(n),n)
id3(wt,i,n) := A(wt,i)'Cx2(wt,n)
Id3%(n,i) := rms%(id3,i,0,π,n)
                                                π - 2'wtl(n)    2
Id%(n,i) := Idl%(n,i) + Id2%(n,i) + Id3%(n,i) + ————————————— 'Io
                                                     2'π
--------------------------------------------------------------------
ich(wt,i,n) := A(wt,i)'Cxl(wt,n)
                                        π - 2'wtl(n)    2
Ich%(n,i) := rms%(ich,i,wtl(n),π - wtl(n),n) + ————————————— 'Io
                                             2'π
--------------------------------------------------------------------
igl(wt,i,n) := A(wt,i)'Cgdn(wt,n)
ig2(wt,i,n) := A(wt,i)'Cx5(wt,n)
Ig%(n,i) := rms%(igl,i,0,π,n) + rms%(ig2,i,0,π,n)
--------------------------------------------------------------------
```

$$E_{n,i} := \frac{wtl(n)}{\pi} \cdot Io \cdot Vf + Isch\%(n,i) \cdot Rsch + Ich\%(n,i) \cdot Rch(n)$$

$$E_{n,i} := E_{n,i} + Id\%(n,i) \cdot Rd(n) + Ig\%(n,i) \cdot Rg(n)$$

$$E := 2 \cdot E \quad Po := Io \cdot Vo$$

$$E_{n,i} := \frac{Po}{Po + E_{n,i}}$$

$$E_{(1,i)}, E_{(2,i)}, E_{(3,i)}, E_{(4,i)}, E_{(5,i)}$$
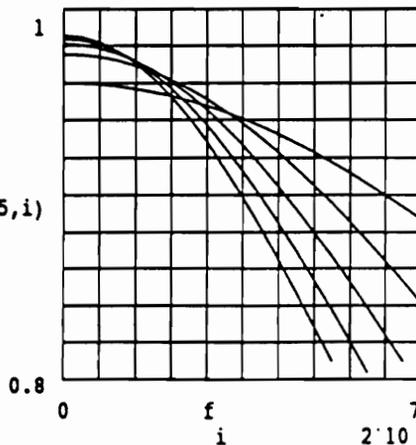
```
-----------------------------------------------------------------------
LOSS IN RESONANT SYNCHRONOUS RECTIFIER - SIMPLE MODEL
-----------------------------------------------------------------------
```

$$i := 0 \,..20 \qquad f_i := 1 \cdot i \cdot 10^6 \qquad w := 2 \cdot \pi \cdot f$$

```
-----------------------------------------------------------------------
```

APPLICATION SPECS:   $Vo := 5$   $Po := 50$
```
------------------------------------------
```
$$Io := \frac{50}{Vo}$$

MOSFET TYPE: GE-50V
```
-----------------------------------------------------------------------
```

$$n := 1 \,..5$$

$$Cgdpl_n := n \cdot 1.91 \cdot 10^{-9}$$

$$Rg_n := \frac{0.25}{n} \qquad Rdson_n := \frac{0.017}{n}$$

$$Cgs_n := n \cdot 0.81 \cdot 10^{-9}$$

$$Vtsr_1 := 4.8 \quad Vtsr_3 := 3.25$$

$$Vtsr_2 := 3.6 \quad Vtsr_4 := 3.1 \quad Vtsr_5 := 2.9$$

```
-----------------------------------------------------------------------
```
DIODE TYPE: 60CNQ030    $Rsch := 0.002$    $Vf := 0.34$
```
-----------------------------------------------------------------------
```

$$Psch_{n,i} := 2 \cdot \frac{Vtsr_n}{\pi^2 \cdot Vo} \cdot Io \cdot (Vf + Io \cdot Rsch)$$

$$Prdson_{n,i} := Io^2 \cdot \left[ 1 - 2 \cdot \frac{Vtsr_n}{\pi^2 \cdot Vo} \right] \cdot Rdson_n$$

$$Prg_{n,i} := \frac{w_i^2 \cdot \pi^2 \cdot Vo^2}{2} \cdot \left[ Cgs_n + Cgdpl_n \right]^2 \cdot Rg_n$$

$$P := Psch + Prdson + Prg$$

$$E_{n,i} := \frac{Po}{Po + P_{n,i}}$$



$$E_{(1,i)}, E_{(2,i)}, E_{(3,i)}, E_{(4,i)}, E_{(5,i)}$$

```
------------------------------------------------------------------------
RESONANT CKT + PWM DRIVE    PRECISE MODEL USING NUMERICAL INTEGRATION
            EFFICIENCY AS A FUNCTION OF GATE-TO-SOURCE VOLTAGE
------------------------------------------------------------------------
                       i := 0 ..20
FREQUENCY                         6        TOL := 1
RANGE                  f  := 1·i·10
                        i                  Integration
                                           tolerance
                       w := 2·π·f
------------------------------------------------------------------------
APPLICATION SPECS:     Vo := 5      Io := 10

A(wt,i) := w ·π·Vo·cos(wt)        v(wt) := π·Vo·sin(wt)
            i
------------------------------------------------------------------------
MOSFET TYPE: GE-50V
------------------------------------------------------------------------
  n := 1                                            -9
                                 Cgs := n·0.81·10
        0.0145                                  -9
 Rd :=  ------                   Cgd0 := 1.34·10
          n                                              -9
                                 Cgdplateau := 1.91·10        φgd := 0.1
                                                 -9
        0.25                     Cds0 := 1.11·10              φds := 1
 Rg :=  ------
          n
```

$Cgdpv(v) := n \cdot (Cgdplateau - (Cgdplateau - Cgd0) \cdot exp(-v))$

$Cgdp(wt) := n \cdot (Cgdplateau - (Cgdplateau - Cgd0) \cdot exp(-v(wt)))$

$$Cds(wt) := n \cdot Cds0 \cdot \sqrt{\frac{\phi ds}{\phi ds + v(wt)}} \qquad Cgdn(wt) := n \cdot Cgd0 \cdot \sqrt{\frac{\phi gd}{v(wt) + \phi gd}}$$

```
------------------------------------------------------------------------
            0.0875              0.0345              0.025               0.021
 Rdson  := ------     Rdson := ------     Rdson := ------     Rdson  := ------
      3       n            4       n           5       n           6       n

            0.019               0.018               0.0175              0.017
 Rdson  := ------     Rdson := ------     Rdson := ------     Rdson  := ------
      7       n            8       n           9       n          10       n
------------------------------------------------------------------------
m := 3 ..10       Vgson  := m
                       m
------------------------------------------------------------------------
```

$$rmst(f,i,a,b) := \frac{1}{2 \cdot \pi} \cdot \int_{a}^{b} f(wt,i)^2 \; dwt$$

```
------------------------------------------------------------------------
id(wt,i) := A(wt,i)·(Cgdn(wt) + Cds(wt))
Id%(i) := 2·rmst(id,i,0,π)
```

```
------------------------------------------------------------------
Ich%(i) := 0.5·Id%(i)
------------------------------------------------------------------
ig(wt,i) := A(wt,i)·Cgdn(wt)
Ig%(i) := rms%(ig,i,0,π)
------------------------------------------------------------------
```

$$P_{m,i} := 2 \cdot Ich\%(i) \cdot \left[ Rdson_m - Rd \right] + 2 \cdot Id\%(i) \cdot Rd + 2 \cdot Ig\%(i) \cdot Rg$$

$$P_{m,i} := P_{m,i} + Io^2 \cdot Rdson_m + 2 \cdot Cgs \cdot Vgson_m^2 \cdot f_i$$

$$P_{m,i} := P_{m,i} + 2 \cdot f_i \cdot Vgson_m \cdot \int_0^{Vgson_m} Cgdpv(v)\ dv$$

Po := Io·Vo

$$E_{m,i} := \frac{Po}{Po + P_{m,i}}$$

$$Eov_i := (0.9 - 0.96) \cdot \frac{f_i}{10^7} + 0.96$$



$$E_{(3,i)}, E_{(4,i)}, E_{(5,i)}, E_{(6,i)}, E_{(7,i)}, E_{(8,i)}$$

```
----------------------------------------------------------------------
RESONANT CKT + PWM DRIVE     PRECISE MODEL USING NUMERICAL INTEGRATION
   EFFICIENCY AS A FUNCTION OF NUMBER OF DEVICES IN PARALLEL
----------------------------------------------------------------------
```

$$i := 0\ ..20$$

FREQUENCY
RANGE $\quad f_i := 1\cdot i\cdot 10^6 \qquad\qquad$ TOL $:= 1$

$\qquad\qquad\qquad$ Integration
$\qquad\qquad\qquad$ tolerance

$$w := 2\cdot\pi\cdot f$$

----------------------------------------------------------------------
APPLICATION SPECS:$\quad$ Vo $:= 5 \qquad$ Io $:= 10$

$$A(wt,i) := w_i\cdot\pi\cdot Vo\cdot\cos(wt) \qquad v(wt) := \pi\cdot Vo\cdot\sin(wt)$$

----------------------------------------------------------------------
MOSFET TYPE: GE-50V
----------------------------------------------------------------------

$$n := 1\ ..5$$

$$Cgs(n) := n\cdot 0.81\cdot 10^{-9}$$

$$Rd(n) := \frac{0.0145}{n} \qquad Cgd0 := 1.34\cdot 10^{-9}$$

$$Cgdplateau := 1.91\cdot 10^{-9} \qquad \phi gd := 0.1$$

$$Rg(n) := \frac{0.25}{n} \qquad Cds0 := 1.11\cdot 10^{-9} \qquad \phi ds := 1$$

$$Cgdpv(v,n) := n\cdot(Cgdplateau - (Cgdplateau - Cgd0)\cdot\exp(-v))$$

$$Cgdp(wt,n) := n\cdot(Cgdplateau - (Cgdplateau - Cgd0)\cdot\exp(-v(wt)))$$

$$Cds(wt,n) := n\cdot Cds0\cdot\sqrt{\frac{\phi ds}{\phi ds + v(wt)}} \qquad Cgdn(wt,n) := n\cdot Cgd0\cdot\sqrt{\frac{\phi gd}{v(wt) + \phi gd}}$$

----------------------------------------------------------------------
$$Rdson_n := \frac{0.0345}{n} \qquad Rdson_1 := \frac{0.025}{1}$$
----------------------------------------------------------------------
$$Vgson_n := 4 \qquad Vgson_1 := 5$$
----------------------------------------------------------------------

$$rms\%(f,i,a,b,n) := \frac{1}{2\cdot\pi}\cdot\int_a^b f(wt,i,n)^2\ dwt$$

----------------------------------------------------------------------
$$id(wt,i,n) := A(wt,i)\cdot(Cgdn(wt,n) + Cds(wt,n))$$
$$Id\%(i,n) := 2\cdot rms\%(id,i,0,\pi,n)$$
----------------------------------------------------------------------
$$Ich\%(i,n) := 0.5\cdot Id\%(i,n)$$
----------------------------------------------------------------------
$$ig(wt,i,n) := A(wt,i)\cdot Cgdn(wt,n)$$
$$Ig\%(i,n) := rms\%(ig,i,0,\pi,n)$$

$$P_{n,i} := 2 \cdot Ich\%(i,n) \cdot \left[ Rdson_n - Rd(n) \right] + 2 \cdot Id\%(i,n) \cdot Rd(n) + 2 \cdot Ig\%(i,n) \cdot Rg(n)$$

$$P_{n,i} := P_{n,i} + Io^2 \cdot Rdson_n + 2 \cdot Cgs(n) \cdot Vgson^2 \cdot f_i$$

$$P_{n,i} := P_{n,i} + 2 \cdot f_i \cdot Vgson_n \cdot \int_0^{Vgson_n} Cgdpv(v,n) \, dv$$

$$Po := Io \cdot Vo$$

$$E_{n,i} := \frac{Po}{Po + P_{n,i}}$$

$$Eov_i := (0.9 - 0.96) \cdot \frac{f_i}{7 \cdot 10} + 0.96$$

$$E_{(1,i)}, E_{(2,i)}, E_{(3,i)}, E_{(4,i)}, E_{(5,i)}$$

```
--------------------------------------------------------------------
                    RESONANT SYNCHRONOUS RECTIFIER
                PRECISE WAVEFORMS WITH NONLINEAR CAPACITANCES
--------------------------------------------------------------------
```

$m := 80$

$i := 0 ..m \qquad f := 7 \cdot 10^{6} \qquad w := 2 \cdot \pi \cdot f$

```
--------------------------------------------------------------------
```

APPLICATION SPECS:   $Vo := 5 \qquad Io := 10$

```
--------------------------------------------------------------------
```

MOSFET TYPE: GE-50V

```
--------------------------------------------------------------------
```

$n := 2$

$$Cgs := n \cdot 0.81 \cdot 10^{-9}$$

$$Cgdpl := n \cdot 1.91 \cdot 10^{-9} \qquad Cgd0 := n \cdot 1.34 \cdot 10^{-9}$$

$$Cgdp(v) := Cgdpl - (Cgdpl - Cgd0) \cdot \exp(-v)$$

$$Cds0 := n \cdot 1.11 \cdot 10^{-9} \qquad \phi gd := 0.1$$

$\phi ds := 1$

$$Cds(v) := Cds0 \cdot \sqrt{\frac{\phi ds}{\phi ds + v}} \qquad Cgdn(v) := Cgd0 \cdot \sqrt{\frac{\phi gd}{v + \phi gd}}$$

```
--------------------------------------------------------------------
```

DIODE TYPE: 60cnq030

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--------------------------------------------------------------------
```

$Rsch := 0.002$

$Vf := 0.34 \qquad\qquad Cj0 := 10.6 \cdot 10^{-9} \qquad \phi d := 0.5$

$$Cj(v) := Cj0 \cdot \sqrt{\frac{\phi d}{v + \phi d}}$$

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--------------------------------------------------------------------
```

PARAMETER CALCULATION

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--------------------------------------------------------------------
```

$Vtsr_1 := 4.8 \quad Vtsr_2 := 3.6 \quad Vtsr_3 := 3.25 \quad Vtsr_4 := 3.1 \quad Vtsr_5 := 2.9$

$$wtl := \operatorname{asin}\left[\frac{Vtsr_n}{\pi \cdot Vo}\right]$$

```
--------------------------------------------------------------------
```

$$wt_i := \frac{2 \cdot \pi}{m} \cdot i \qquad v_i := \pi \cdot Vo \cdot \sin\left[wt_i\right] \qquad A(i) := w \cdot \pi \cdot Vo \cdot \cos\left[wt_i\right]$$

$Cx1(v) := Cgs + Cds(v) + Cj(v)$
$Cx2(v) := Cgdn(v) + Cds(v)$
$Cx3(v) := Cgdp(v) + Cgs + Cds(v) + Cj(v)$
$Cx4(v) := Cds(v) + Cj(v)$
$Cx5(v) := Cgdp(v) + Cgs$

$$vgs_i := if\left[wt_i < \pi, 0, -v_i\right] \qquad vgs_m := vgs_0$$

---

$$\text{il}_i := \text{if}\left[\text{wt}_i < \pi, 0, -A(i)\cdot\text{Cx1}\left[-v_i\right] + \text{Io}\right] \qquad \text{il}_m := \text{il}_0$$

---

$$\text{isch}_i := -A(i)\cdot\text{Cj}\left[v_i\right] \qquad\qquad\qquad \text{ich} := \text{il}$$

$$\text{isch}_i := \text{if}\left[\text{wt}_i < \pi, \text{isch}_i, \text{il}_i\right] \qquad\qquad \text{ich}_i := \text{if}\left[v_i > -\text{Vtsr}_n, 0, \text{il}_i\right]$$

$$\text{isch}_m := \text{isch}_0$$

$$\text{isch}_i := \text{if}\left[v_i > -\text{Vtsr}_n, \text{isch}_i, 0\right]$$

---

$$\text{id}_i := -A(i)\cdot\text{Cx2}\left[v_i\right]$$

$$\text{id}_i := \text{if}\left[\text{wt}_i < \pi, \text{id}_i, -A(i)\cdot\text{Cgdp}\left[-v_i\right]\right]$$

$$\text{id}_i := \text{if}\left[v_i > -\text{Vtsr}_n, \text{id}_i, -A(i)\cdot\text{Cx3}\left[-v_i\right] + \text{Io}\right]$$

$$\text{id}_m := \text{id}_0$$

---

$$\text{ig}_i := -A(i)\cdot\text{Cgdn}\left[v_i\right]$$

$$\text{ig}_i := \text{if}\left[\text{wt}_i < \pi, \text{ig}_i, -A(i)\cdot\text{Cx5}\left[-v_i\right]\right]$$
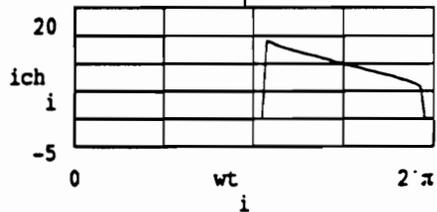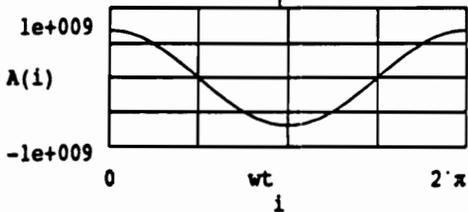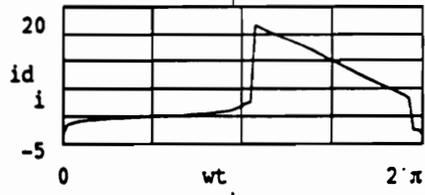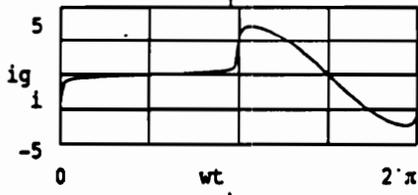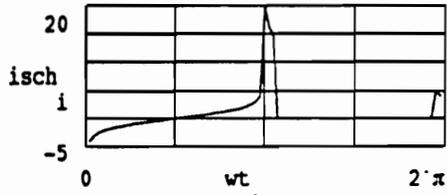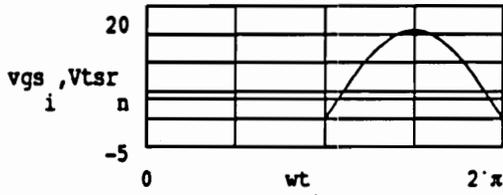
# Vita

The author was born on March 23, 1959 in Warsaw, Poland. He received his M.S. degree in electronics engineering from the Technical University of Warsaw, Warsaw, Poland in 1984. In 1985, he enrolled in Virginia Polytechnic Institute and State University as a doctoral student. His doctoral research concentrated on high-frequency resonant power conversion techniques. For his research, he was awarded first place in the 1989-1990 Ph.D. Research Award Competition organized by the College of Engineering, VPI&SU. He also was granted three U.S. patents on the multi-resonant technology developed during his doctoral study. The author is a member of the IEEE Power Electronics Society and the Sigma Xi Scientific Research Society.