New Concepts in Front End Design for Receivers with Large, Multiband Tuning Ranges

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Abstract

This dissertation presents new concepts in front end design for receivers with large, multiband tuning ranges. Such receivers are required to support large bandwidths (up to 10's of MHz) over very large tuning ranges (30:1 and beyond) with antennas that are usually narrowband, or which at best support multiple narrow bandwidths. Traditional techniques to integrate a single antenna with such receivers are limited in their ability to handle simultaneous channels distributed over very large tuning ranges, which is important for frequency-agile cognitive radio, surveillance, and other applications requiring wideband or multiband monitoring. Direct conversion architecture is gaining popularity due to the recent advancements in CMOS–based RFIC technology. The possibility of multiple parallel transceivers in RF CMOS suggests an approach to antenna–receiver integration using multiplexers. This dissertation describes an improved use of multiplexers to integrate antennas to receivers. First, the notion of sensitivity–constrained design is considered. In this approach, the goal is first to achieve sensitivity which is nominally dominated by external (environmental) noise, and then secondly to improve bandwidth to the maximum possible consistent with this goal. Next, a procedure is developed for designing antenna-multiplexer-preamplifier assemblies using this philosophy. It is shown that the approach can significantly increase the usable bandwidth and number of bands that can be supported by a single, traditional antenna. This performance is verified through field experiments. A prototype multiband multimode radio for public safety applications using these concepts is designed and demonstrated.

This dissertation is dedicated to

my mother Hasina Sardar, my wife Rimi Ferdous,

and my advisors:

Dr. S. W. Ellingson, Dr. M. K. Howlader, Dr. Y. W. Kang, & Dr. S. M. L. Kabir

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Chapter 1

Introduction

Wideband radios with multiband capability are becoming increasingly important in various applications such as public safety, military communication, and cognitive radio. However, the design of such radios becomes complicated with expansion in the number and width of frequency bands. Design issues include interfacing a single antenna with a transceiver, designing a suitable wideband RF front end, and processing multiple channels simultaneously. In this dissertation, we describe and demonstrate new concepts for front end design for transceivers with large, multiband tuning ranges intended to address these issues.

This chapter briefly introduces the multiband multimode radio (MMR) and the challenges behind its development. Section 1.1 ("Multiband Multimode Radio (MMR)") describes MMR and Section 1.2 ("Application Example: Public Safety") discusses one of the applications currently driving the development of MMR. Section 1.3 ("Traditional Front End Design") presents traditional approaches to MMR front end design. Section 1.4 ("Current Trends in Front End Design") summarizes the current research trends in front end design, and existing limitations. Section 1.5 ("Problem Statement") poses the specific problem that this dissertation addresses. Section 1.6 ("Contributions") summarizes the research contributions of this dissertation and Section 1.7 ("Organization of this Dissertation") describes the organization of the remainder of this dissertation.

1.1 Multiband Multimode Radio (MMR)

MMR is a class of radio which can operate in multiple frequency bands using multiple modes. MMR is not new; for example, radios have long been available that provide AM and FM modes over frequencies ranging from a few MHz to a few GHz. An example of a state-of-the-art commercial MMR is the dual-mode (CDMA/GSM) quad-band cellular phone, which is multiband primarily to accommodate regional and international roaming. There are also many high-performance low-cost handheld transceivers capable of 3– or 4–band operation widely available for amateur radio applications. Low cost is possible for these MMRs due primarily to the following reasons: (1) each band individually has a small tuning range and is limited to one mode or a family of very similar modes, (2) modest performance requirements, and (3) extremely large production volumes.

Present-day MMRs are constrained in the number of bands and modes that can be supported. One of the emerging issues is that most MMRs are traditionally designed to communicate through only one band at a time, i.e., simultaneous operation in multiple bands is typically not supported. However, simultaneous multiband operation is desirable in public safety radios; for example, where first responders may want to talk in one channel and simultaneously receive data using another frequency band. Furthermore, current MMRs are limited by small instantaneous bandwidth (10's of kHz to a few MHz), small tuning ranges (a few percent bandwidth), and the physical limitations of existing antennas.

There is a need for a new class of MMR which provides simultaneously very large instantaneous bandwidth (up to 10's of MHz) to process multiple channels concurrently and very large (30:1 or beyond) tuning ranges to cover multiple frequency bands. Additional motivation arises from the desire for "future–proof" radios using software defined radio (SDR) technology [1] and to support seamless interoperability among many existing disparate standards. Examples include public safety [2, 3] and military communications [4]. Another reason is that frequency–agile cognitive radio (CR) and certain government surveillance applications benefit from this MMR. In the CR application, this benefit is due to need to search for "white spaces"; that is, unused spectrum.

In order to accommodate various bands and modes, designers are currently working hard to tightly integrate various disparate band-specific circuits in a one single radio, which in turn increases the

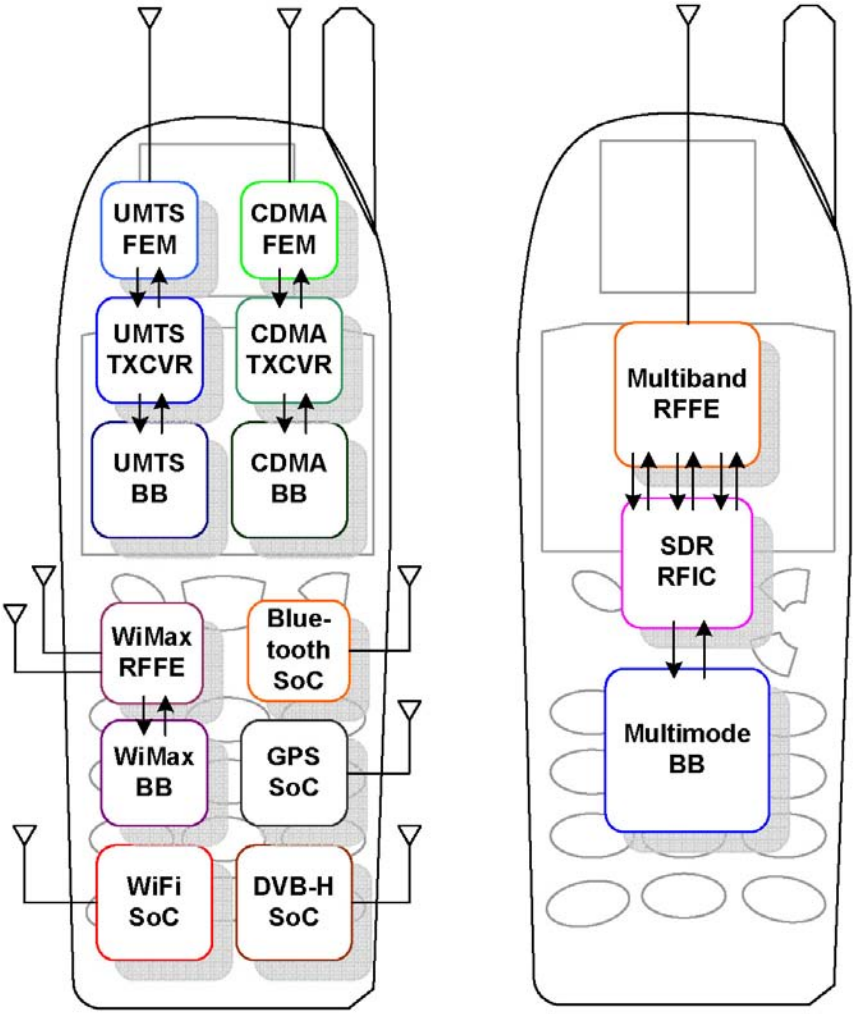
cost, power consumption, and requires multiple antennas. This is illustrated in Figure 1.1(a).

The emergence of new wideband, radio–frequency integrated circuits (RFIC) which can cover large range of frequencies and support multiple modes is motivating designers to develop MMR using the concept shown in Figure 1.1(b) [5]. Note that even if all bands and modes can be supported using a common chipset, the antenna remains a problem, and there is a need for a multiband RF front end (RFFE) to integrate a single antenna with a wideband receiver. This dissertation addresses this front end problem and presents a new concept to antenna integration with the RF front end which may be better suited to modern MMR applications.

1.2 Application Example: Public Safety

To understand the need for improved MMR, we now consider an application example. Wireless communication is an essential component of public safety operations [6, 7]. First responders have benefited from many technical advances in the wireless area in recent years including new modes for voice and data communications, cellular and satellite communications, and wireless local area networks (WLAN). At the same time, this profusion of new technology has aggravated a looming crisis of interoperability. Incompatible equipment, rigid and fragmented spectrum allocations, and continuing reliance on proprietary and "closed" systems are some of the key problems preventing seamless communications among first responders. Table 1.1 summarizes public safety communications in terms of frequency bands which are used, and the modes of communications that are used in each band.

Currently, the dominant paradigm for interoperability in public safety communications is based on network infrastructure. This is illustrated in Figure 1.2(b). In this approach, disparate radio networks are integrated through the use of radios that are combined back-to-back and serve as relays. A limitation of this approach is poor support for uncoordinated users, i.e., unanticipated users utilizing technology not supported by the network infrastructure as illustrated in Figure 1.2(c). Classic examples of such users include military units, state and federal agencies, and non-profit organizations acting in a support role during disaster response and other various crisis operations. However, this problem exists to some extent wherever first responders rely on cellular, WLAN, and



(a) (b)

Figure 1.1: Illustration of multiband multimode radio using (a) different chipsets for various bands/modes, (b) one single chipset for all bands/modes. Adopted from an illustration by Bitwave Semiconductor (www.bitwave.com) (used with permission, see Appendix I).

Table 1.1: Frequency bands and modes commonly used for public safety mobile radio communications in the United States. TIA–603 includes narrowband analog FM.

Band	**Frequency (MHz)**	**Mode(s)**
HF	25–30	TIA–603 [8]
VHF	30–50 138–174 220–222	TIA-603 TIA–603, P25 [9] Voice/Data (not TIA–603)
UHF	406–512	TIA–603, P25
700 MHz	764-776 794-806	TIA-603, TIA-902 [10], P25, IEEE 802.16(e) TIA-603, TIA-902, P25, IEEE 802.16(e)
800 MHz	806-817 824-849 851-862 869-894	TIA-603, P25 Cellular uplink (many modes) TIA-603, P25 Cellular downlink (many modes)
PCS	1850–1990	PCS (many modes)
ISM	2400-2483	IEEE 802.11
4.9 GHz	4940-4990	IEEE 802.11, Voice over IP (VoIP), Universal Mobile Telecommunication System (UMTS)/ Time Division Duplex (TDD)

other technologies which are too expensive or complex to be accommodated by existing network-based interoperability devices. Other solutions – including deployments of multiple sets of handsets and terminals, and loan of equipment to uncoordinated users – usually entail undesirable additional operational, training, and logistical difficulties.

An alternative to network-based interoperability that better serves uncoordinated users is *user-based interoperability*. In this approach, shown in Figure 1.2(d) existing infrastructure continues to operate without modification, but is accessed in a seamless and transparent manner by means of a single MMR, which is deployed to the users. Ideally, users equipped with such radios would be able to communicate in any public safety radio system, immediately and without prior technical coordination. Furthermore, MMRs using SDR technology could eventually lead to simplification, standardization, and improved future-proofing of radio infrastructure.

Such technology has long been of interest to the U.S. military, which faces similar interoperability challenges and has invested considerable resources on the problem. However, military requirements differ considerably from those of the public safety community. Thus, military SDR-based MMR technology has limited applicability to public safety applications [11]. Nevertheless, military SDRs

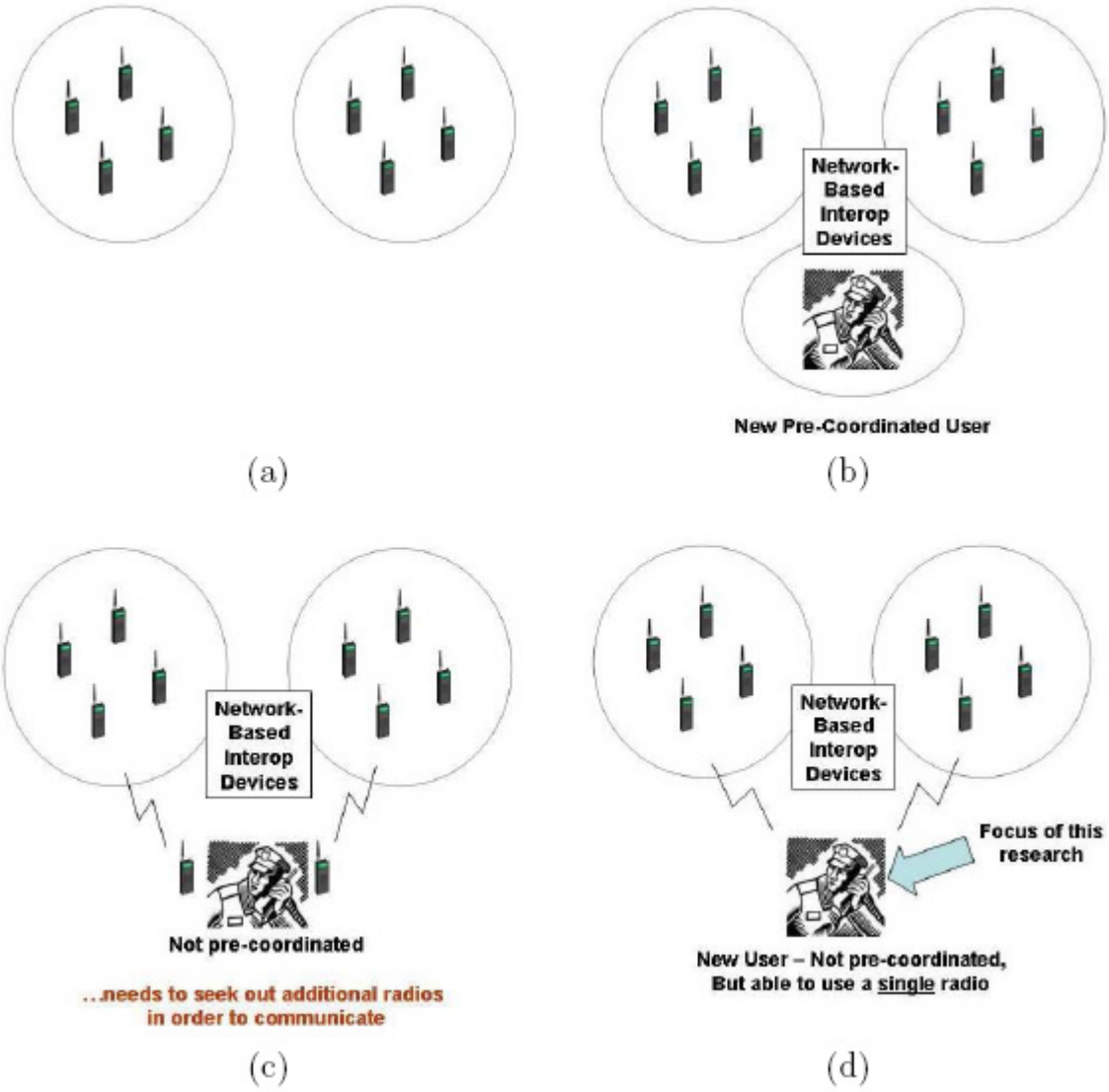


Figure 1.2: Interoperability between two disparate radio networks. (a) Two groups, using incompatible bands/modes. (b) Network-based interoperability. (c) Introducing a new uncoordinated user. (d) User-based interoperability.

including the Thales MBITR and the Harris Falcon–II radios have been considered in field tests with public safety agencies [12].

Two recently–announced MMRs, the Harris *Unity* XG–100P[1], and the Thales *Liberty*[2], are reported to cover all the public safety frequency bands in 136–870 MHz, with maximum bandwidth up to 25 kHz. The vendors indicate that these radios will be available sometime in 2009, however, details on the architecture and performance of these radios is not publicly available yet.

1.3 Traditional Front End Design

The term "front end" refers to the combination of components in a transceiver between the antenna and the first frequency conversion stage, including antenna matching circuits, bandpass or channelization filters, preamplifiers (on receive side) and power amplifiers (PAs) (on transmit side), and their associated matching circuits. The design of an RFFE for MMR is a complex problem. To illustrate this, Figure 1.3 shows a *simplified* block diagram of the receiver section of a low-cost handheld commercial MMR for amateur radio communications, the Yaesu VX-7R. This radio is desired for operation in the frequency bands 50–54 MHz, 144–148 MHz, 220–222 MHz, and 420–450 MHz with channel bandwidth up to 25 kHz. Double conversion superheterodyne architecture is used to generate the 450 kHz intermediate frequency (IF) at which AM and narrowband FM are detected. Triple conversion architecture is used to generate the 1 MHz IF for wideband FM.

The small antennas used by handheld MMRs are inherently narrowband, exhibiting a wide range of impedances over the tuning range, which in turn imposes difficulties to get good matching between the antenna and the radio using traditional matching techniques. To illustrate this, Figure 1.4 shows the measured impedance–frequency characteristics of the "rubber duck" antenna provided with the VX-7R. The calculated impedance mismatch efficiency (IME) (defined in Section 3.1) assuming a preamplifier with 50Ω input impedance is shown in Figure 1.5. Note that this antenna is only able to achieve efficient matching with the preamplifier at certain frequencies. The need for dramatically larger instantaneous bandwidth and tuning ranges in emerging MMR applications make this antenna–receiver integration an even more daunting task.

[1] http://www.rfcomm.harris.com/talkasone/
[2] http://www.thalesliberty.com

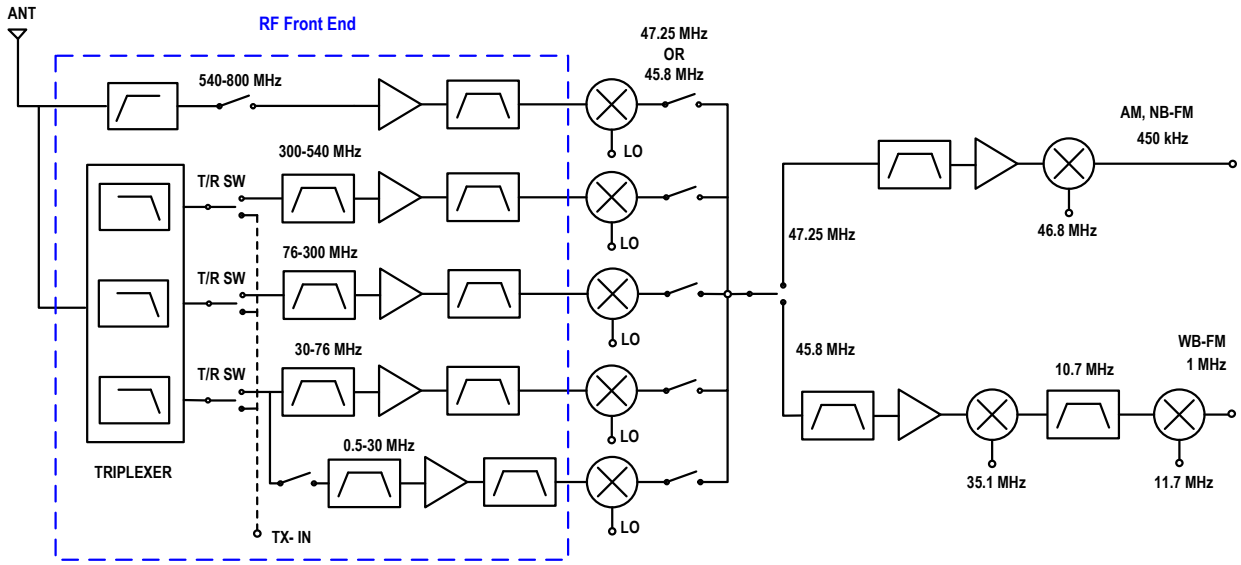


Figure 1.3: Receiver section of VX-7R multiband radio [13].

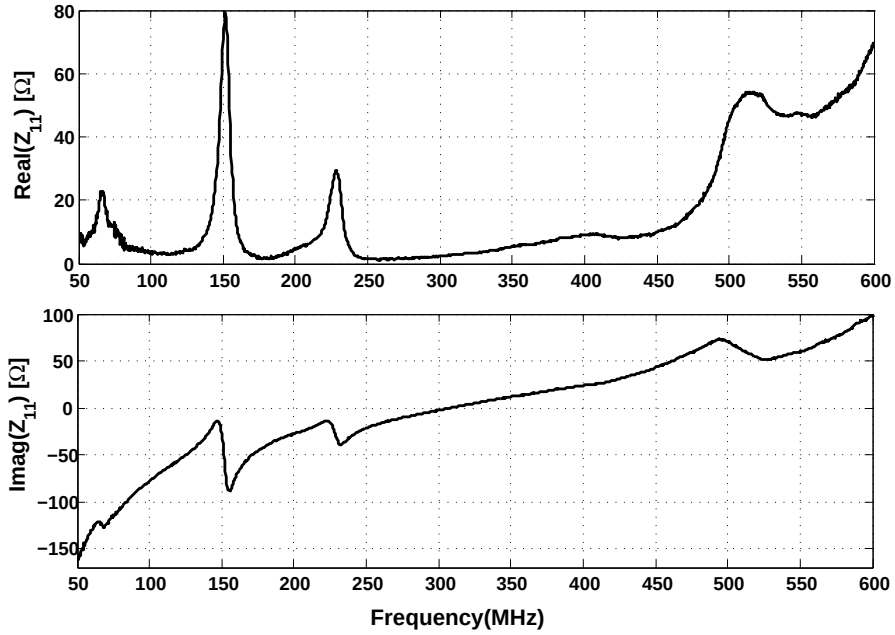


Figure 1.4: Antenna impedance of VX-7R multiband radio (measured by the author with the assistance of Virgina Tech Antenna Group).

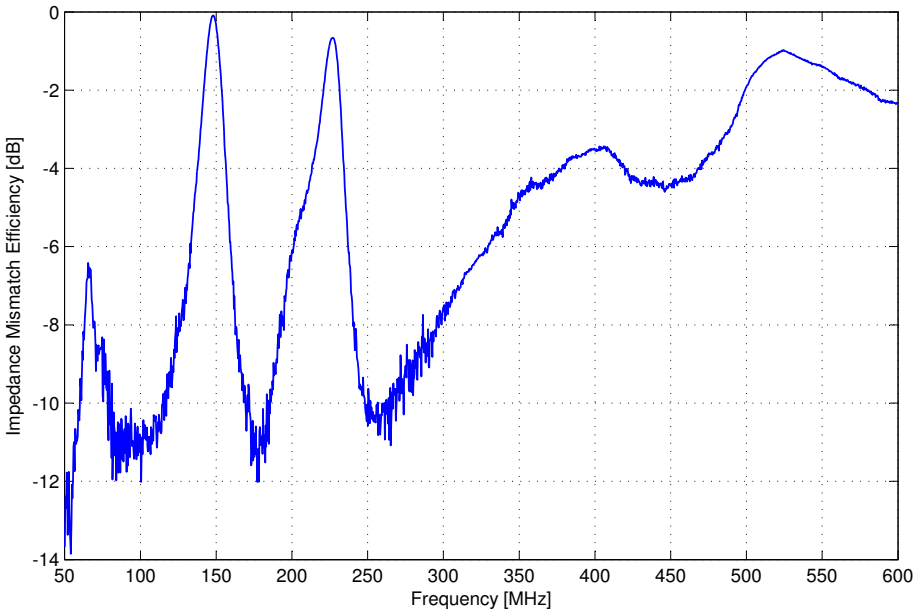


Figure 1.5: Calculated IME (loss due to reflection at the antenna–receiver interface) between the VX-7R antenna and a preamplifier with input impedance 50Ω.

1.4 Current Trends in Front End Design

As shown in Figure 1.3, existing front end designs for MMRs commonly use multiplexers (e.g., diplexers, triplexers, etc.) to channelize incoming signals. Traditional design methodologies for multiplexers assume standard input or output impedances [14]. These are useful over frequency ranges in which antennas are approximately resonant, but are of limited value outside this range. Although there is much recent work in compact ultrawideband (UWB) antennas [15, Chapter 4], this is mostly not relevant to the applications of interest, due to their awkward and bulky shapes at frequencies below 1 GHz [16].

RF micro-electromechanical systems (MEMS) switches [17] can be used to implement reconfigurable antennas. Cummings (2003) discusses the viability of RF MEMS for designing reconfigurable antennas [18]. Anagnostou *et al.* (2006) describe an RF MEMS-based reconfigurable antenna that radiates similar patterns over three widely separated frequencies [19]. However, this approach has limitations as described below and in Section 3.4.

A more practical alternative for mobile and portable radio below 1 GHz is active matching, which

seeks to match the antenna and transceiver using switch–selectable impedances instead of just a fixed one [20, Chapter 4]. Typically, a microprocessor directs the switches to configure the electrical components into any one of a number of impedance matching circuits. However, the size of the tuning circuits increases with decreasing frequency and increasing number of desired bands to be covered.

An approach similar to above (using different switching technology) which is now a popular idea is the implementation of reconfigurable front ends using MEMS switches, e.g., [21]. This approach is presently limited by immature device technology (switches with the necessary power handling and reliability are in many cases not available) [22], increased complexity (more control signals), and provide matches which are narrowband in the same sense as those provided by traditional active tuners.

1.5 Problem Statement

This dissertation seeks to address and improve upon the state–of–the–art in front end design for transceivers with large, multiband tuning ranges. To make the scope of this research manageable, this dissertation is restricted in scope to the receive side only. Thus, this work is *directly* applicable to receive-only devices (e.g., surveillance and white space seekers) as well as the receive section of transceivers where this functionality can be isolated (e.g., as in fully time division duplex (TDD) systems). The extension of this work to frequency division duplex (FDD) and fully integrated transceiver systems is left as future work. From this point forward, the term "front end" refers specifically the receive portion of the front end.

This work consists of the following elements :

- Traditional monopole antennas used in current mobile/handheld radios are narrowband in nature. Traditional antenna–receiver interfacing provides matching only in a narrow range of frequencies, whereas wideband matching is difficult and fundamentally limited by the physics of antennas (as explained in Section 3.2). We would like to improve the effective bandwidth of radios using traditional monopole antennas currently in use. Our concept is to improve

bandwidth by allowing the impedance mismatch to degrade in a controlled way such that the sensitivity remains acceptable, and is nominally limited only by external noise. In order to implement this concept there should be a clear idea about the external noise environment. So our first task is to quantify and reformulate what is known about external noise from previous studies.

- Although the above concept has already been demonstrated in a limited way for application in radio astronomy, no attempt has been made to investigate this concept for mobile radio applications. So our next task is to repeat previous work, however, using an antenna more closely related to monopoles used in our applications of interest.

- Current multiplexer design methodologies assume standard input/output impedances, thereby imposing the restriction that the antenna–multiplexer interface must be a fixed standard impedance. We would like to remove this restriction while simultaneously employing the principle of external noise domination mentioned above. This combination of approaches appears to be completely new and no previous study along these lines has been found. We demonstrate designs based on these concepts both analytically and in field conditions.

- To assess the pros and cons of the above concepts in a practical application, we would like to design and demonstrate a complete MMR for the public safety application.

1.6 Contributions

The main contribution of this dissertation is to incorporate sensitivity–constrained approach in impedance matching to perform antenna–receiver interfacing for receivers with large, multiband tuning ranges. Original contributions of this research include the following items.

1. Presently there is no simple standard way to take the effect of external sources of noise into account when specifying the noise figures of receivers with large, and multiband tuning ranges. In this dissertation, the concept of a subjective "optimum" noise figure specification has been developed to serve this purpose (Section 4.2). This concept should be useful in the design of the next generation wideband receivers for software-defined and cognitive radio systems.

2. A receiver has been designed and used to demonstrate the principle of external noise–dominated sensitivity (Section 4.4). Although this principle has been demonstrated before using dipoles, the specific contribution here is demonstration using a VHF monopole antenna which is more similar to the antennas used in mobile and portable radios. This experiment also provides a performance baseline for other measurements in this dissertation.

3. A new antenna–receiver integration methodology using multiplexers is developed (Section 5.3). This approach is not limited by the assumption of standard/constant impedance at the antenna–receiver interface, and emphasizes performance not from an impedance–matching perspective, but rather from the perspective of system sensitivity. This approach is shown to significantly increase the usable bandwidth without changing the design of the antenna or adversely affecting sensitivity.

4. The approach is demonstrated in field conditions, again with a VHF monopole antenna (Section 5.4) with a multiplexer for the bands 10–28 MHz, 32-50 MHz, and 54-80 MHz.

5. RF front end multiplexers are designed (Sections 6.1 and 6.2) for application to MMR for the public safety frequency bands 138–174 MHz, 220–222 MHz, 406–512 MHz, and 764–862 MHz. These are demonstrated to have the expected performance in simulation, although some difficulties are encountered in hardware implementation.

6. A complete MMR has been designed and built employing the multiplexer from Section 6.2 with a state–of–the–art CMOS–based direct conversion RFIC, and demonstrated in the above public safety frequency bands using a simple traditional narrowband monopole antenna (Chapter 7).

1.7 Organization of this Dissertation

The remainder of this dissertation is organized as follows.

- Chapter 2 ("Receiver Design Fundamentals & Trends") provides a review of the relevant concepts and trends related to receiver design.

- Chapter 3 ("Antenna–Receiver Interfacing") provides a review of the fundamental limitations of antenna–receiver matching, with some examples.

- Chapter 4 ("Sensitivity-Constrained Front-End Design") presents the concept of designing a sensitivity–constrained front end, incorporating the effect of external noise. The concept is demonstrated in a field experiment.

- Chapter 5 ("Multiplexer Design") presents the new multiplexer design methodology, and reports experimental verification.

- Chapter 6 ("Multiplexer Application to a Multiband Multimode Radio") describes the design and performance analysis of front end multiplexers developed using the new design methodology, now for applications in the public safety bands 138–174 MHz, 220–222 MHz, 406–512 MHz, and 764–862 MHz. The multiplexers are developed for a generic rod monopole antenna and for an actual short monopole antenna.

- Chapter 7 ("Design & Development of a Multiband Multimode Radio") describes the design and development of a complete prototype MMR for public safety application employing the proposed front end and frequency conversion design concepts described in the previous chapters.

- Chapter 8 ("Conclusions") summarizes the findings of this research and makes recommendations for future work.

Chapter 2

Receiver Design Fundamentals & Trends

This chapter provides a brief review of receiver design fundamentals and trends. Various components of a receiver and issues related to receiver design are also presented here. This chapter is organized as follows. In Section 2.1 ("Anatomy of a Radio "), a description of the various parts of a radio is presented. Section 2.2 ("Antennas") describes the antenna circuit and impedance model. The various parameters of a receiver from a system design perspective are discussed in Section 2.3 ("Receiver System Design Parameters"). Section 2.4 ("Receiver Architectures") describes various frequency conversion architectures. Section 2.5 ("New Possibilities for MMR with RFICs") introduces some relevant recent developments in RF integrated circuit (RFIC) technology and their implications for MMR design. Finally, Section 2.6 ("Summary") summarizes this chapter.

2.1 Anatomy of a Radio

Figure 2.1 shows a block diagram of a typical radio. As we can see there is a single antenna connected with a front end through a matching circuit. This matching circuit can be a fixed or a variable matching circuit, the main function of which is to match the front end with the antenna in such a way that acceptable sensitivity can be achieved during reception and acceptable power

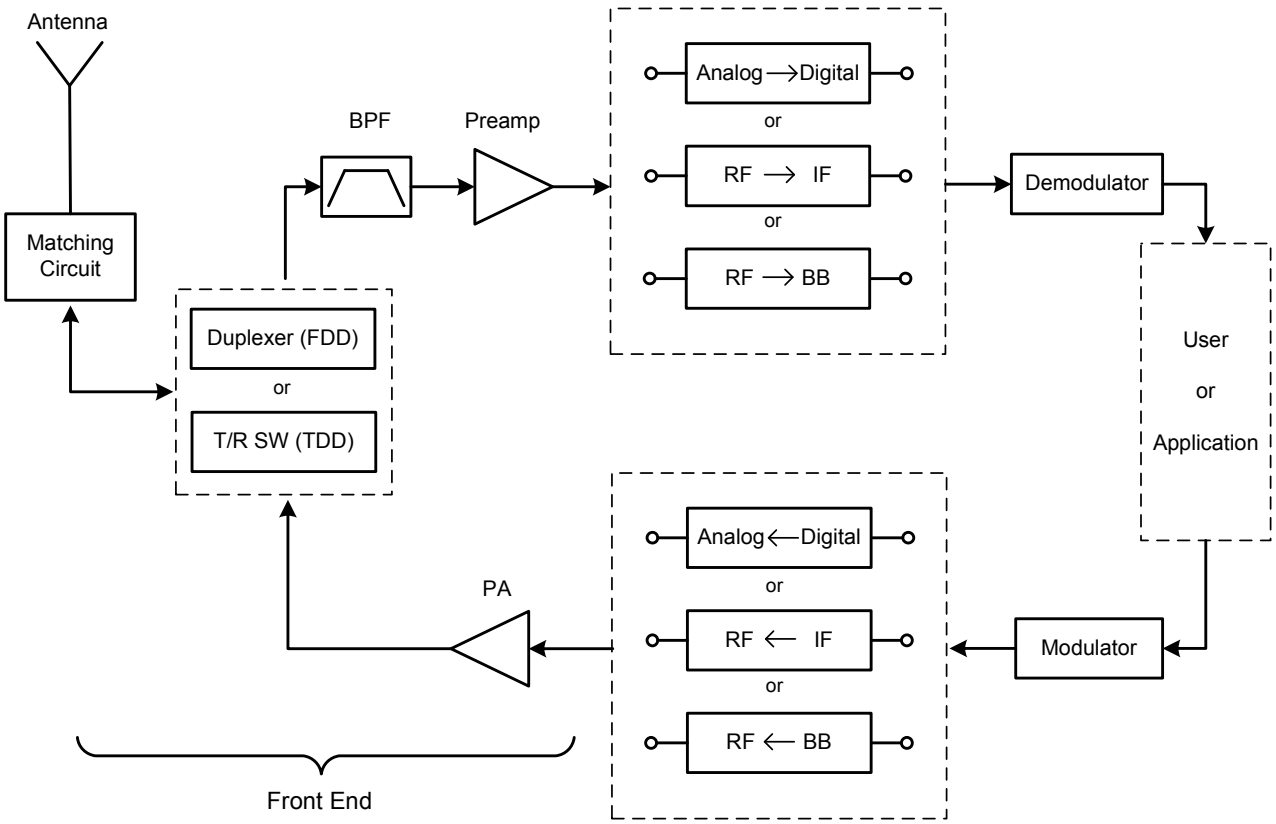


Figure 2.1: Block diagram of a typical radio.

transfer can be obtained during transmission. If the transceiver is time–division duplexed (TDD) then a transmit/receive (T/R) switch is used to route the incoming or outgoing RF signal to the receiver or from the transmitter, respectively. On the other hand, if the system is frequency–division duplexed (FDD) then a duplexer is placed at the transceiver's front end to allow simultaneous transmit/receive on different frequencies while using the same antenna.

The receive path consists of a bandpass filter (BPF) and a preamplifier to amplify the incoming RF signals. Traditionally, this preamplifier sets the receiver's noise figure (F), and thus sensitivity. Depending on the receiver architecture, the incoming RF signal can be processed in one of three ways: (1) For *direct sampling* architecture the incoming analog RF signal is digitized using an analog to digital converter (ADC); (2) For *superheterodyne* architecture it is downconverted to an intermediate frequency (IF) before digitization; or (3) For *direct conversion* architecture this is downconverted to a complex–valued (zero center frequency) baseband (BB) signal before digitiza-

tion. After digitization, the received signal is further processed or demodulated in a demodulator. The same sequence of operations, but in reverse order, are performed in the transmitter side of the block diagram.

2.2 Antennas

An antenna converts signals in the form of guided electromagnetic energy (in transmission lines) to signals in the form of unguided electromagnetic energy (in radio waves), and vice versa. Antennas are normally reciprocal devices; i.e., behave the same on transmit as on receive. In this section we describe how antennas can be modeled for receiver design studies. This section also presents some antenna impedance models, which can be used as a tool to model antenna impedance in the later chapters of this dissertation.

As shown in Figure 2.2, an antenna can be modeled as impedance Z_A for transmission [23]. Moreover, in that figure the transmitter is modeled as a voltage source v_g in series with the impedance Z_g. The antenna impedance Z_A can be expressed as

$$Z_A = R_A + jX_A \tag{2.1}$$

where R_A represents dissipation, which can be expressed as

$$R_A = R_{rad} + R_{loss} \tag{2.2}$$

where R_{rad} represents radiated power that leaves the antenna and never returns, and R_{loss} represents ohmic loss associated with finite conductivity. For the antennas of interest here, $R_{loss} << R_{rad}$ typically and can be neglected. The input reactance X_A represents power stored in the near field of the antenna; i.e. the non-radiating field.

Figure 2.3 shows the Thevenin equivalent circuit model for an antenna in receive mode. Here, v_A is the open-circuit voltage, which is the voltage generated at the terminals of an open-circuited antenna in response to an incident electric field, and Z_g now represents the input impedance of the receiver. As a consequence of reciprocity, the impedance of an antenna is identical during reception

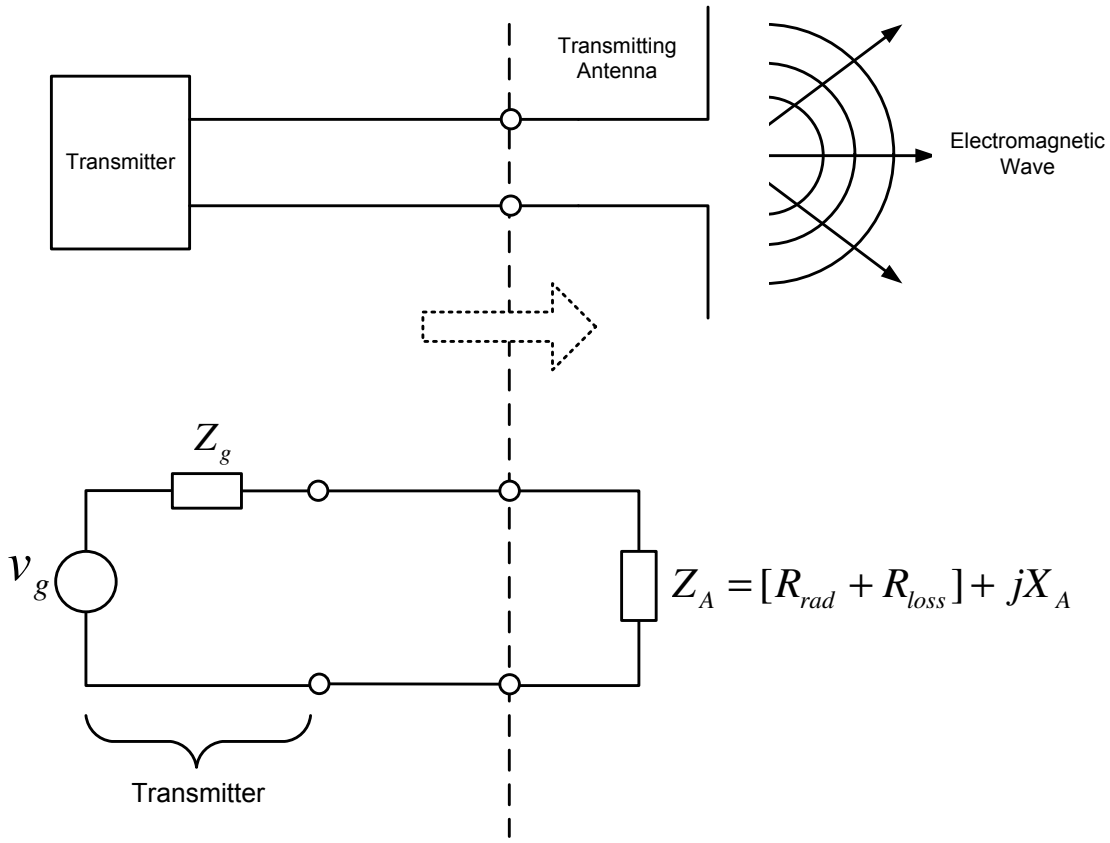


Figure 2.2: Circuit model for antenna during transmission of signals.

and transmission.

The impedance Z_A is the ratio of the voltage to current at the antenna terminals. For the purpose of antenna–receiver integration, it is useful to know this parameter before starting to design an RF front end. The impedance of a lossless short dipole, the length of which is very small compared to its wavelength, can be represented as [23]

$$R_A \cong R_{rad} \approx 80\pi^2 \left(\frac{h}{\lambda}\right)^2 \ \Omega \tag{2.3}$$

$$X_A \approx -\frac{60}{\pi\left(\frac{h}{\lambda}\right)}\left[\ln\left(\frac{h}{a}\right) - 1\right] \ \Omega \tag{2.4}$$

where h is the half-length and a is the radius of the dipole. In this dissertation, our intention is to pay special attention to the same type of simple straight monopole antennas which are already very popular in hand–held and mobile transceivers. An ideal monopole antenna is obtained by replacing one half of an ideal dipole antenna with an infinite ground plane. Due to the simple relationship between the monopole and dipole, dipole impedance can easily be transformed to monopole impedance using the relationship

$$Z_{A,monopole} = \frac{1}{2} Z_{A,dipole}. \tag{2.5}$$

Various numerical methods, including the method of moments (MoM) and the finite difference time domain (FDTD) method, are used to calculate antenna impedance for more complex or realistic antennas for which simple expressions are not available. However, these methods provide only numerical results (e.g., a list of impedance versus frequency), rather than an equivalent circuit of the impedance of an antenna. For the purposes of RF front end design, however, the latter is often more useful. Methods which produce circuit models for canonical antenna types (such as dipoles) include [24–26]. We prefer the method of Tang, Tieng, and Gunn [25] due to its simplicity and ability to accurately model the impedance of a dipole antenna over a broad bandwidth using an equivalent circuit of just four components. This method will be referred to as "TTG" in this dissertation. The TTG approach provides a circuit model for Z_A of the form shown in Figure 2.4. Equations 2.6 through 2.9 show the calculations for the values of the circuit elements. Note that

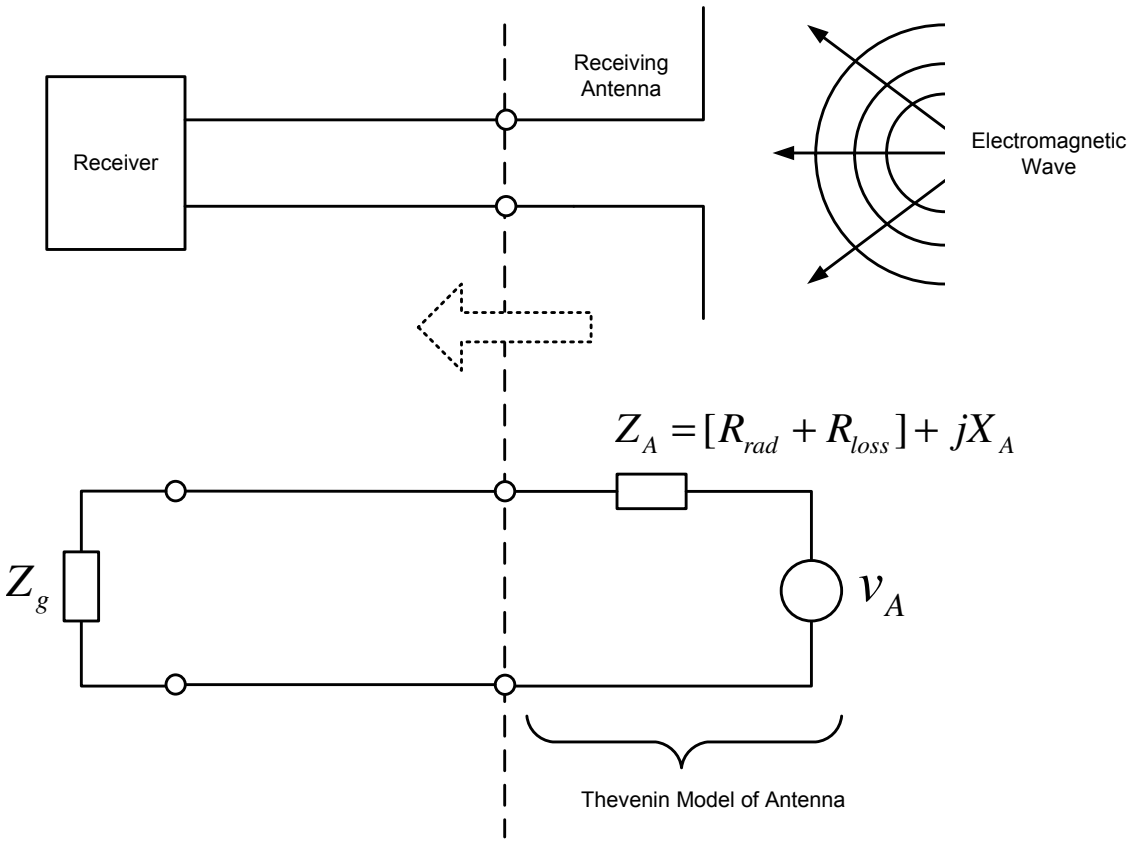


Figure 2.3: Circuit model for antenna during reception of signals.

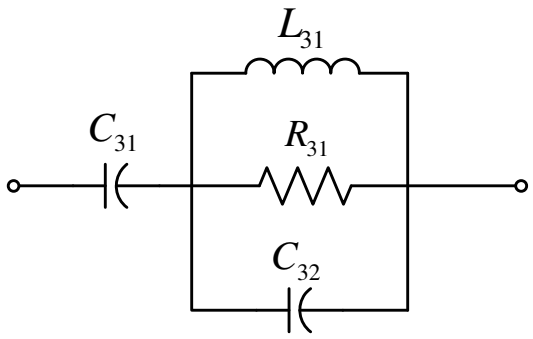


Figure 2.4: TTG circuit model for Z_A for a dipole antenna.

the constants h and a are in meters, and the TTG model is only applicable for straight dipoles.

$$C_{31} = \frac{12.0674h}{\log(2h/a) - 0.7245} \quad \text{pF} \quad (h \text{ in meters}) \tag{2.6}$$

$$C_{32} = 2h\left\{\frac{0.89075}{[\log(2h/a)]^{0.8006} - 0.861} - 0.02541\right\} \quad \text{pF} \quad (h \text{ in meters}) \tag{2.7}$$

$$L_{31} = 0.2h\left\{[1.4813\log(2h/a)]^{1.012} - 0.6188\right\} \quad \mu\text{H} \quad (h \text{ in meters}) \tag{2.8}$$

$$R_{31} = 0.41288\,[\log(2h/a)]^2 + 7.40754(2h/a)^{-0.02389} - 7.27408 \quad \text{k}\Omega \tag{2.9}$$

2.3 Receiver System Design Parameters

This section briefly describes some useful system–level parameters of a receiver. This section is organized as follows. Section 2.3.1 ("Digitization") and Section 2.3.2 ("Sensitivity and Gain") describe digitization and the issues related to receiver's sensitivity, respectively. In Section 2.3.3 ("Linearity"), various linearity parameters are defined. Finally, Section 2.3.4 ("Selectivity") discusses selectivity.

2.3.1 Digitization

Digitization is the process of converting an analog signal into digital form. An analog to digital converter (ADC) is used to perform this digitization. An ADC requires the magnitude of the input

signal in a particular range to digitize it properly. For example, most modern high–speed ADCs output full scale when the input signal level is about 1 V_{pp} at 50Ω input impedance, i.e., at about +3 dBm. It also has its own internal noise due to quantization, which is rounding error between the analog input to the ADC and the output digitized value. The quantization noise of an ideal ADC is

$$P_Q = -1.76 - 6.02N_b \ \ [\text{dB relative to } P_{clip}] \tag{2.10}$$

where N_b is the number of bits of the ADC, and P_{clip} is the input power corresponding to the maximum level the ADC can properly encode. However, due to the additional analog noise (approximately 2 dB typically) generated by the digitizer, a simpler and more realistic expression is

$$P_Q \cong -6N_b \ \ [\text{dB relative to } P_{clip}] \tag{2.11}$$

The problem of determining the nominal gain and N_b for a particular receiver is now considered. Let P_t be the total power input to the receiver at the antenna terminals. This power is the sum of P_{ext} (total external noise power received by the receiver), and P_S (total power due to external signal sources). The minimum required gain in the analog signal path, G_{min}, and the maximum allowed gain, G_r, are given by

$$G_{min} = \frac{P_Q \gamma_q}{P_{ext}} \text{ , and} \tag{2.12}$$

$$G_r = \frac{P_{clip}\delta_r}{P_t}, \tag{2.13}$$

respectively, where γ_q is the minimum desired ratio of external noise to quantization noise at the input of the ADC, and δ_r is the maximum desired ratio of maximum acceptable input power to P_{clip}. The ratio δ_r (typically about -10 dB) is chosen to accommodate temporary increases in power due to intermittent signals and the spurious co-phasing of individual signals. Now, the quantization noise power referenced to the input of the ADC is

$$P_Q = P_{clip} 10^{-6N_b/10}. \tag{2.14}$$

The ratio γ_q then given by

$$\gamma_q = \frac{P_{ext} G_r}{P_Q} = \frac{P_{ext}}{P_t} \delta_r 10^{6N_b/10}. \tag{2.15}$$

It is desirable for external and internal noise to dominate over quantization noise. Thus γ_q is typically chosen to be around 10. Solving for N_b yields [27]

$$N_b \geq 1.67 \log_{10} \left(\frac{P_t \gamma_q}{P_{ext} \delta_r} \right). \tag{2.16}$$

The number of bits required for quantization noise to be dominated by external noise by a factor of γ_q at the output of the ADC can be calculated using Equation 2.16. In this process, P_{ext} and P_S must be known, and γ_q and δ_r are design parameters.

2.3.2 Sensitivity and Gain

Sensitivity in a receiver can be defined as the minimum input signal power required to produce a predetection (i.e., input to demodulator) output signal having a specified signal to noise ratio (SNR). This input level is known as minimum detectable signal (MDS) and is given by

$$\text{MDS} = \delta k T_0 B F \tag{2.17}$$

where δ is the minimum predetection SNR needed to detect a signal, k is Boltzmann's constant (1.38×10^{-23} J/K), T_0 is the noise reference temperature (290 K), and B is the detection bandwidth of the receiver. F represents the *noise figure* of the receiver.

Noise figure is a characterization of the additional noise contribution of an RF stage and is defined as the ratio of the SNR at the input of an RF stage to the SNR at the output of an RF stage; i.e.,

$$F = \frac{S_i / N_i}{S_o / N_o} \tag{2.18}$$

where S_i and S_o is the signal at the input and output, respectively; and N_i and N_o is the noise at the input and output, respectively.

Often in radio design, noise figure is specified, as opposed to minimizing or specifying MDS [28]. This approach makes it possible to overspecify the receiver's noise figure during the design process. This fact is especially true for the frequencies at VHF and below, where the receiver noise can be dominated by the external environmental noise. An emphasis in the work reported in this

dissertation is to determine the extent to which this observation can be used to improve the usable bandwidth of front ends. Chapter 4 describes this approach in more detail.

The purpose of gain (G) in a receiver is to increase the power of the received signal to a level greater than that of the quantization noise of the ADC. However, gain which introduces excessive additional noise defeats the purpose. In a well-designed receiver, environmental noise should dominate over internal analog noise if possible; and quantization noise should be dominated by both the environmental and internal analog noise. By combining these two conditions the receiver gain requirement can be bounded as follows:

$$\frac{P_{clip}\delta_r}{P_t} \geq G \geq \frac{\gamma_q P_{clip} 10^{-0.6N_b}}{P_{ext}}. \tag{2.19}$$

A traditional receiver design might proceed as follows: (1) We specify the sensitivity (MDS), which then sets the receiver's noise figure; (2) N_b is determined using Equation 2.16; and then (3) The range of required total gain is calculated using Equation 2.19.

Another way to specify the sensitivity of receivers used for voice communication is audio signal–to–noise–and–distortion ratio (SINAD). A typical specification for SINAD is that it must be at least 12 dB for a 1 kHz audio tone [8]. The relationship between predetection SNR and SINAD is described for analog FM in Appendix A. The analysis in the appendix shows that 12 dB SINAD corresponds to 6.5 dB predetection SNR for a modulation bandwidth of 12.5 kHz and an audio bandwidth of 3 kHz.

2.3.3 Linearity

Linearity is the desirable property that the output signal voltage (or current) varies in direct proportion to the input signal voltage (or current), i.e., the output-to-input signal ratio is always the same. Any practical analog system is only approximately linear, with the deviation from linearity increasing with increasing power. Assuming that the input voltage signal applied to an amplifier is v_{in}, then the output voltage v_{out} can be expressed as (weakly non–linear)

$$v_{out}(t) = \alpha_0 + \alpha_1 v_{in}(t) + \alpha_2 v_{in}^2(t) + \alpha_3 v_{in}^3(t) + \ldots \tag{2.20}$$

where α_i is the i^{th} order coefficient with $i = 0, 1, 2, 3, ...$ The above equation describes a linear system if $\alpha_i \equiv 0$ for $i > 1$.

An amplifier usually maintains approximately constant gain for low-level input signals. However, at higher input levels, it goes into compression and the gain decreases. A graphical illustration of this compression is shown in Figure 2.5. In other words, as the input signal increases in power, a point is reached where the power of the signal at the output is not amplified by the same amount as the smaller signal. At the point where the input signal is amplified by an amount 1 dB less than the ideal gain, the *1 dB compression point* (P1) has been reached. A common requirement is that input power P1 should be greater than the largest expected input signal power. Using Equation 2.20, the corresponding voltage can be expressed as [29]

$$\sqrt{0.145 \left| \frac{\alpha_1}{\alpha_3} \right|} \tag{2.21}$$

This non–linear transfer function also leads to the generation of intermodulation products at the output of the receiver. These intermodulation products can fall into the spectrum of interest and interfere with the desired received signals. This is illustrated in Figure 2.6, in which for any two tones at frequencies ω_1 and ω_2, the second-order intermodulation products (IM2s) appear at frequencies $\omega_1 \pm \omega_2$. Moreover, the third-order intermodulation products (IM3s) appear at frequencies $2\omega_1 \pm \omega_2$ and $\omega_1 \pm 2\omega_2$, respectively.

To characterize the non–linearity and the level of intermodulation products, there are two other useful parameters: the second order intercept point (IP2), and the third order intercept point (IP3). A graphical illustration of these parameters are also shown in Figure 2.5. The *input–referred second-order intercept point* IIP2 is defined as the level of two equal-strength input tones at the point at which the resulting IM2s have the same power as the input tones, as they appear in the output. The *input–referred third-order intercept point* IIP3 is defined as the level of two equal-strength input tones at the point at which the resulting IM3s have the same power as the input tones, as they appear in the output. Using Equation 2.20, the voltage corresponding to IIP3 can be expressed as [29]

$$\sqrt{\frac{4}{3} \left| \frac{\alpha_1}{\alpha_3} \right|}. \tag{2.22}$$

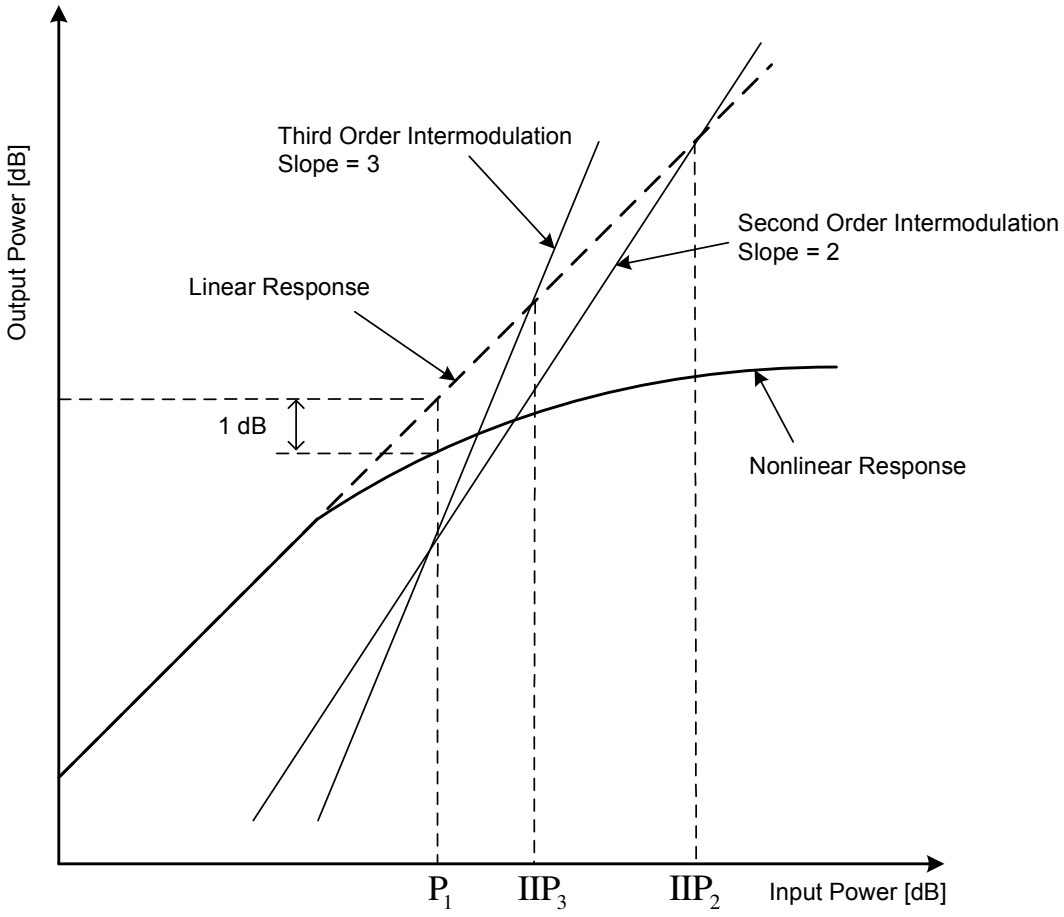


Figure 2.5: Graphical explanation of P1, IIP2, and IIP3.

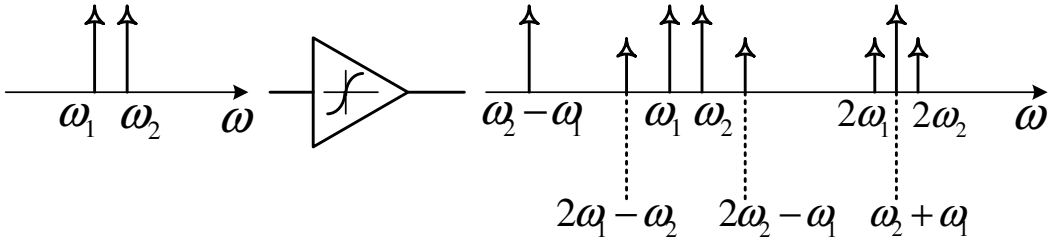


Figure 2.6: Intermodulation products.

The relationship between P_1 and IIP3 can be found by combining Equations 2.21 and 2.22 to yield

$$\frac{\text{P1}}{\text{IIP3}} \approx -9.6 \text{ dB}. \tag{2.23}$$

Typically, improvements in sensitivity and linearity are mutually exclusive. This can be demonstrated using the simple example shown in Figure 2.7 consisting of three components: a preamplifier, a variable attenuator, and a second amplifier. Note that in the figure OIP3 is the output third order intercept point and noise figure of the attenuator is inverse to the attenuation. Total gain, IIP3, and noise figure can be calculated using a stage–cascade gain, noise figure, and third order intercept (GNI) analysis, described in Appendix B. Figure 2.8 shows the effect of total gain on linearity (IIP3) and sensitivity (MDS). Note that improvement in MDS as attenuation is decreased is accompanied by degradation in IIP3, and vice versa. Thus, it is difficult to achieve jointly optimum MDS and IIP3. As a result, some trade–offs need to be made; e.g., to accept good sensitivity, trading off linearity; or vice versa. This problem can be managed to some extent by incorporating *selectivity* in the RF front end in order to suppress intermodulation products. This is discussed next.

2.3.4 Selectivity

The selectivity of a receiver is defined as its ability to respond only to the desired frequency band and reject unwanted frequencies including those likely to contribute to the intermodulation products. Bandpass filters, filter banks, or tunable filters may be used to implement selectivity. *Preselection* refers to the implementation of selectivity specifically in the RF front end of a receiver. Typically, for

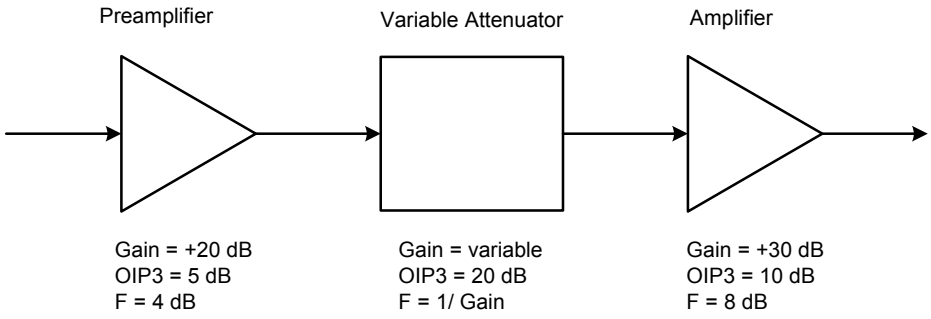


Figure 2.7: Simple receive system for linearity–sensitivity trade-off analysis.

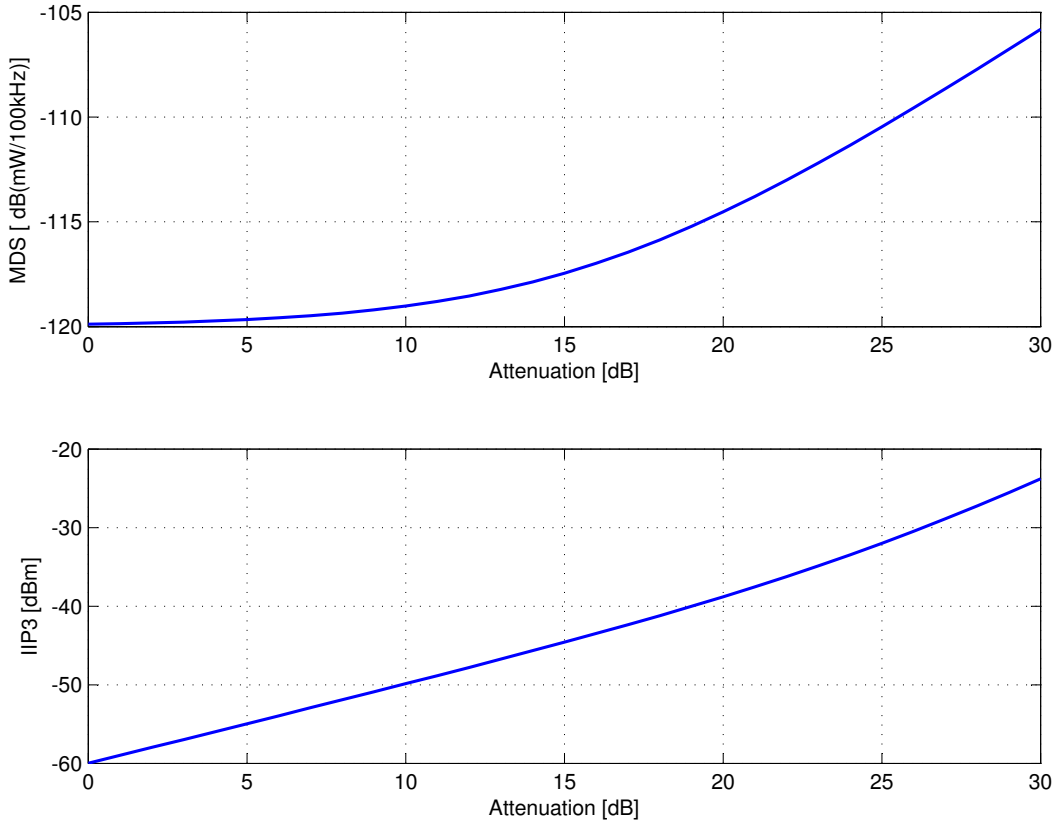


Figure 2.8: Sensitivity (MDS) and IIP3 versus attenuator setting for the simple receiver model shown in Figure 2.7

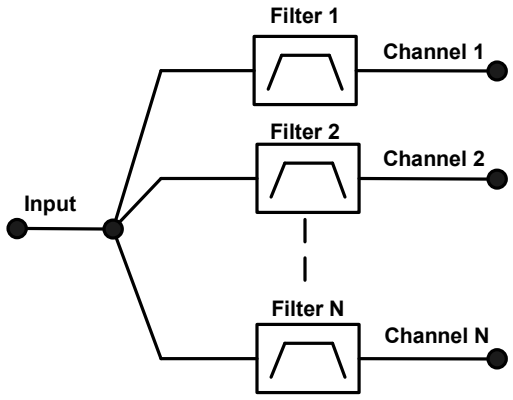


Figure 2.9: N-channel multiplexer using bandpass filters.

single band radios operating over narrow fractional bandwidth, a single fixed or tunable bandpass filter is adequate to perform preselection. However, it is often not possible to implement preselection in a multiband radio or a radio which operates over large range of frequencies using a single bandpass filter. A multiplexer can be a possible solution in this case. A multiplexer is a parallel or series combination of filters to separate the RF input into multiple frequency bands. Figure 2.9 shows an example of a multiplexer using parallel bandpass filters. An example of the implementation of selectivity in superheterodyne receiver using a triplexer and bandpass filters is shown in Figure 1.3.

2.4 Receiver Architectures

This section describes some of the relevant architectures for receivers. Section 2.4.1 ("Superheterodyne Architecture") briefly discusses the widely-used superheterodyne architecture. Section 2.4.2 ("Direct Sampling Architecture") describes direct sampling architecture, which can be the ideal (but still not practical) receiver architecture for MMR. Finally, the direct conversion architecture is discussed in Section 2.4.3 ("Direct Conversion Architecture"). Each section discusses the pros and cons of the architectures for application to MMR.

2.4.1 Superheterodyne Architecture

A superheterodyne (also known as a "superhet") receiver is a receiver in which the frequency of the RF signal is mixed with a locally–generated "local oscillator" (LO) for conversion to an intermediate frequency (IF). Superhet receivers have been in use for a long time and have been quite popular since the early days of radio communication. One, two, or more stages of conversion can be used in superhet architecture. Figure 2.10 provides a block diagram of a single–conversion superhet receiver. The receiver consists of a preselector bandpass filter, a preamplifier, and a mixer to convert the input RF frequency f_{RF} to the IF frequency f_{IF}. f_{LO} is the frequency supplied by the LO to the mixer.

This frequency conversion process also allows an undesired frequency called the "image frequency" that is capable of producing the same IF that the desired input frequency produces. For example, the image frequencies in Figure 2.10 would be $f_{LO} \pm f_{RF}$ depending on the side of signal injection (If $f_{LO} > f_{RF}$ then it is called high–side injection, and if $f_{LO} < f_{RF}$ then it is called low–side injection). This "image frequency" can be mixed with f_{LO}, produce f_{IF}, and can create interference to proper reception of the signal. One of the major chores in the design of superhet receivers is the suppression of unwanted image frequencies, which needs to be filtered out using an image rejection filter preceding the mixer. Since this undesired signal is never filtered to "zero" amplitude in practical receivers, usually designer does the frequency planning (to select the suitable IF and LO frequencies) in such a way that the image frequencies do not fall into the desired band of frequencies. However, the frequency planning becomes complicated and daunting for a receiver with large tuning range, because it is difficult to avoid image frequencies inside the desired frequency band.

There is a another problem which also limits the tuning range of a superhet receiver. This is due to the interference of the "half–IF frequency", which is located halfway between the frequencies of the LO and the incoming RF signal. The half–IF signal is downconverted into the IF band by mixing with the second harmonic of the LO signal [29, p.126]. Although this problem can be avoided with adequate filtering in the front–end, or by using low–distortion amplifiers and mixers, it is hard to mitigate adequately for MMR with large tuning ranges.

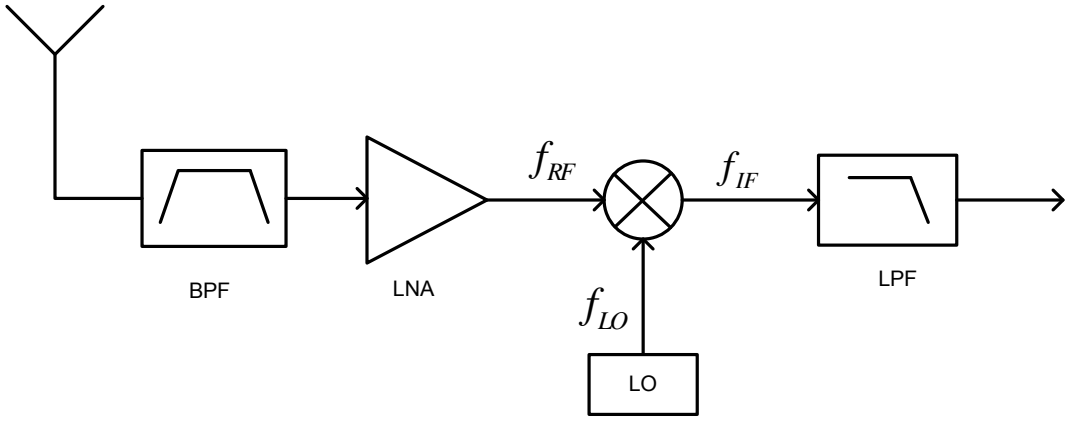


Figure 2.10: A single–conversion superheterodyne receiver architecture.

Figure 1.3 (Chapter 1) is an example of a "divide-and-conquer" type of superhet receiver. "Divide-and-conquer" design is commonly used to implement multiband capability and to minimize the above mentioned limitations in the design of a superhet–based receiver. In this approach, the large tuning range is decomposed into multiple narrower bands, each of having their own frequency conversion stage. Usually, for receivers with narrow tuning ranges, the single conversion superhet architecture is sufficient. However, using two (or more) conversion stages instead of a single conversion approach allows the LO and IF frequencies to have more separation, thus to avoid image frequencies in the desired band.

"Divide-and-conquer" superhet architecture is the method of choice for present-day MMR. The primary advantages of the superhet are the ability to put gain and selectivity at frequencies other than RF (i.e., at the IF). However, the complexity of the circuit, cost, and power consumption increases with the increasing number of tuning ranges. In "divide-and-conquer" systems, these problems are replicated in each parallel RF path. Therefore, alternative frequency conversion architectures are of interest. Two possibilities are described in the following two sections.

2.4.2 Direct Sampling Architecture

In direct sampling architecture, the RF signal itself is digitized, and frequency conversion is performed in the digital domain instead of the analog domain. A simplified block diagram of a direct

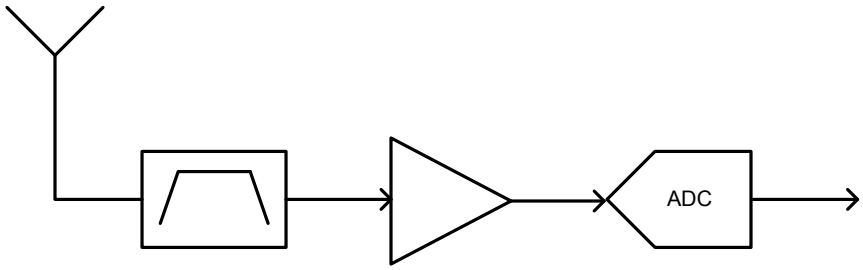


Figure 2.11: Block diagram of a direct sampling receiver.

sampling receiver is shown in Figure 2.11. The RF bandpass filter is used to select the desired band and a preamplifier is used to amplify the signal to the input requirements of the ADC.

Digitization requires sample rate more than twice the highest bandwidth of interest. If it is needed to design a MMR to operate in the frequency range of 100 MHz to 1 GHz using direct sampling, then the required sampling speed for the ADC would be at least 2 GSPS (billion samples per second). Achieving this is currently difficult, expensive, and power–intensive [30, 31]. As an example the theoretical power consumption of a ADC operating at rates of 100s of MSPS is currently on the order of watts. This is clearly a high value of power consumption for consideration to be included in a mobile radio.

Even if high power consumption is acceptable, the RF design becomes a challenge due to the linearity issues, especially for IM2s. Since direct sample architecture needs to pass the entire tuning range, the IM2s are usually passed through the preamplifier and ADC, and thus corrupting the desired signal. The only way to minimize this problem is to use narrowband filter, however, that will limit the tuning range of the direct sampling receiver. In other words, the overall tuning range of the direct sampling architecture is very much limited by the IM2s. From the above discussions we can conclude that currently direct sampling may not be a generally–suitable architecture for MMR.

2.4.3 Direct Conversion Architecture

In a direct conversion receiver (DCR), the incoming RF signal is directly mixed down to an analog baseband signal with a center frequency of zero. A block diagram of a DCR is shown in Figure 2.12.

The RF signal is directly converted to complex baseband in-phase (I) and quadrature-phase (Q) signals using a single LO set to the frequency to be received. The benefits of this architecture include: elimination of IF stages; channel filtering and amplification are relatively easier at baseband compared to at RF; reduced ADC requirements; power consumption reduction due to reduced components and lower sampling rate; and wide tuning range, limited only by the initial BPF. However, DCR has been in limited use in the past due to some major implementation drawbacks compared to the superhet architecture [32, 33]. These include

1. *DC Offsets*

   An incidental DC offset voltage is caused by self–mixing; the LO leakage actually mixes with the original LO signal creating a DC voltage which can corrupt the signal of interest, lowering the SNR, and more importantly, possibly saturating the baseband amplifier stages. Figure 2.13 demonstrates the generation of DC offset and LO leakage in a DCR. Furthermore, LO leakage through the RF sections is a large consideration in a design, since it can cause in–band interference due to the proximity of the LO signal to the frequency of the incoming RF. A similar effect occurs if a large interferer leaks from the preamplifier or mixer input to the LO port and is multiplied by itself.

2. *I/Q Imbalance*

   As shown in Figure 2.12, a DCR incorporates quadrature downconversion. It is difficult to achieve constant amplitude and 90° phase over a large frequency range.

3. *Phase Noise*

   As the down–converted RF signal is usually small in amplitude compared to the LO, and nearly the same frequency, additional SNR degradation due to the phase noise of the LO is often significant in DCR.

4. *Even–Order Distortion*

   Non-linearities in the mixer and preamplifier produce even–order intermodulation, which (especially second–order) introduces undesirable spectral components at baseband, and also degrades the receiver sensitivity. Superhet receivers are susceptible primarily only to odd–order intermodulation effects because even–order terms lie far outside the (narrow) tuning

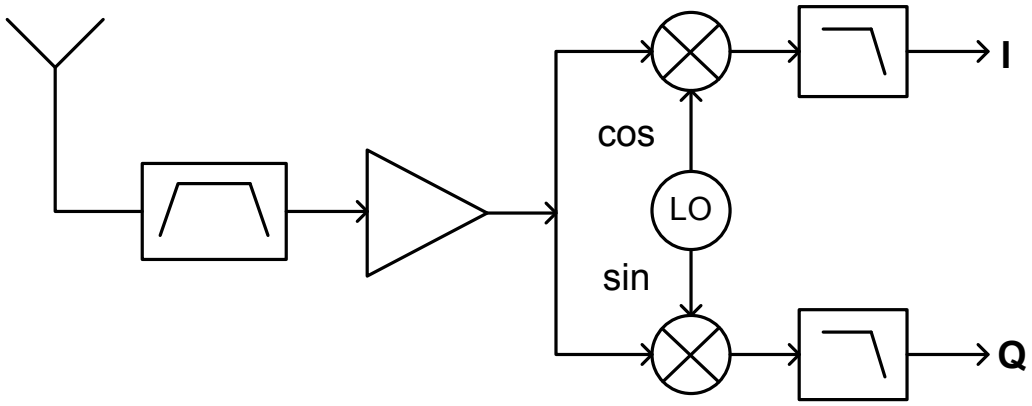


Figure 2.12: Block diagram of a direct conversion receiver.

range (as shown in Figure 2.6). In direct conversion, on the other hand, the undesired component due to even–order distortion can corrupt the down–converted signal of interest, because two high frequency interferes can generate a low frequency even–order distortion product which can pass through the mixers from the RF input to the baseband output.

Due to recent advancements in circuit implementation all of the problems can be alleviated to some extent. These techniques are discussed briefly in the next section.

2.4.4 Modern Techniques to Overcome Direct Conversion Limitations

This section presents emerging techniques to solve the inherent limitations, discussed in the previous section, of direct conversion architecture. Section 2.4.4.1 ("Chopper Stabilization") presents a technique called chopper stabilization that reduces noise injected near DC, DC offset, and second–order intermodulation products. Section 2.4.4.2 ("Differential Implementation") discusses the advantages of differential implementation of DCR.

2.4.4.1 Chopper Stabilization

Chopper stabilization (or "chopping") [34], also known as "dynamic matching" [35], is an effective method for mitigating in–band noise injected near DC, DC offset, and second–order intermodulation products. Figure 2.14 illustrates the concept of chopping for an amplifier. Mixers are located at

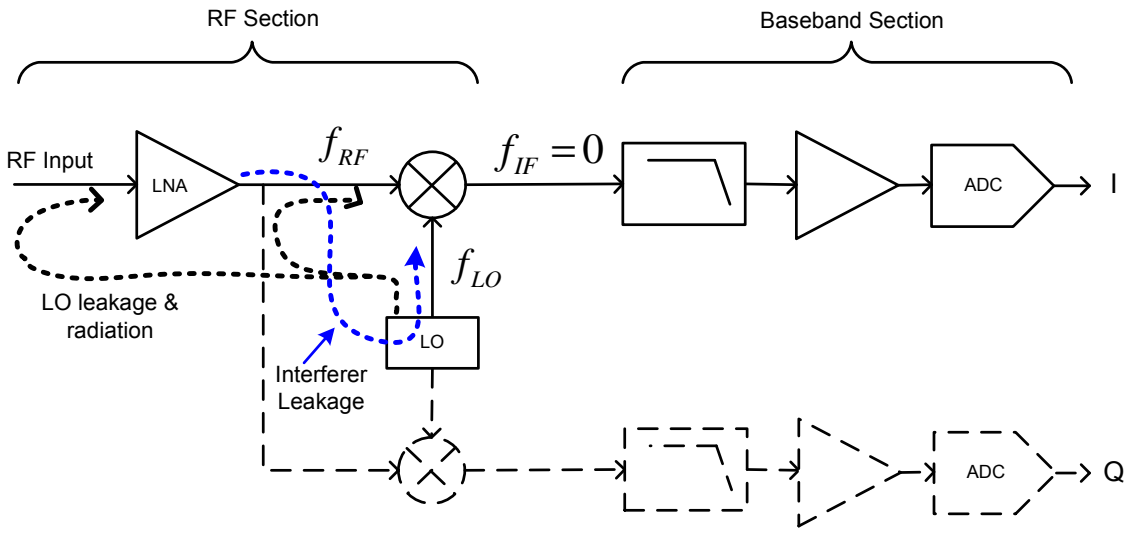


Figure 2.13: LO leakage and interface leakage in a direct conversion receiver (shown for one baseband section only).

the input and output of an amplifier that multiply the incoming RF signal by $+1$ or -1 at a "chopping frequency" of f_{chop}. At the input of the first mixer the desired RF signal (green square block) is shown with two strong interferers (red dotted arrow). The first mixer shifts the desired RF signal and the interferers up by f_{chop}. At the output of the amplifier the desired signal is still centered around f_{chop} but there is also a DC offset and flicker noise component (purple triangle) as well as second–order distortion products (blue small dotted arrow) due to the imperfections of the amplifier. These signals are shown in red dotted arrows. The second mixer shifts the desired signal back down to its original frequency and at the same time shifts the unwanted components up by f_{chop}. Therefore, no unwanted signals reside in the desired signal band, and thus these impairments are easily removed by lowpass filtering.

This approach is difficult to implement in discrete circuits and traditional RFIC technologies, but is quite simple to implement in CMOS RFIC technology. Thus, the emergence of CMOS RFIC technology has led to a resurgence of interest in direct conversion architecture specifically.

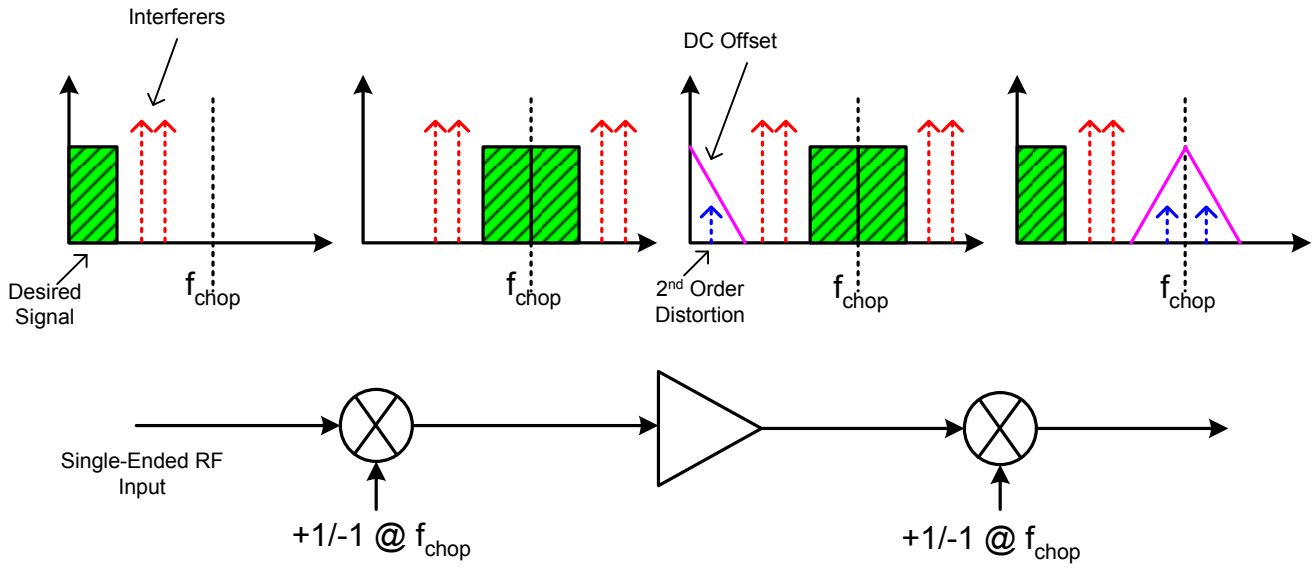


Figure 2.14: Illustration of chopper stabilization technique.

2.4.4.2 Differential Implementation

Conventional (single ended) circuits use the voltage on a single conductor to convey the signal and the voltage is measured with respect to ground. Differential circuits, in contrast, split the signal across the two conductors in such a way that it can be defined as the voltage difference between the conductors, and independent of the reference (ground) potential. Differential circuits provide improvements in rejection of electromagnetic interference, increased common-mode signal rejection, and increase in dynamic range rejection of even-order harmonic distortion [36]. The DC offset and the even orders of intermodulation distortion can be reduced using differential implementation. Thus, differential signaling can greatly improve the performance of a DCR.

To illustrate, let us assume that V_{i1} and V_{i2} are the input voltages to the differential RF block shown in Figure 2.15. Since differential implementation requires equal magnitude and opposite phase input signals, if $V_{i1} = A\sin(\omega t)$ then $V_{i2} = -V_{i1} = -A\sin(\omega t)$. Now, using Equation 2.20, the second–order non–linearity of the output voltage in the two output paths would be

$$V_{o1}^{(2)} = \alpha_{21} V_{i1}^2 = \alpha_{21} \frac{A^2}{2}(1 - \cos(2\omega t)) \tag{2.24}$$

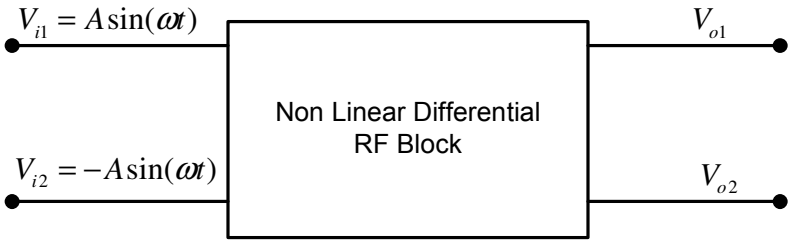


Figure 2.15: RF block with a differential input and output.

$$V_{o2}^{(2)} = \alpha_{22} V_{i2}^2 = \alpha_{22} \frac{A^2}{2}(1 - \cos(2\omega t)) \tag{2.25}$$

where α_{21} and α_{22} are the coefficients of second–order non–linearity for the signal path of first and second conductor, respectively. Since the signal conveyed by a differential transmission line is defined to be the voltage difference across the conductors, the second–harmonic voltage is

$$V_{out}^{(2)} = \frac{A^2}{2}(\alpha_{21} - \alpha_{22})(1 - \cos(2\omega t)) \tag{2.26}$$

For a perfectly–balanced differential circuit, $\alpha_{21} = \alpha_{22}$, which makes the second–harmonic term zero. The same canceling result occurs for the DC term and all even–order terms. In a similar way it is possible to show the common–mode rejection property of differential circuits.

The same kind of chopping technique presented in the previous section can be implemented very easily using differential circuitry, as shown in Figure 2.16. The mixers are replaced by switches which simply swap the conductors of the differential pairs. Using this technique in a CMOS DCR has been shown to provide at least 11 dB improvement of second–order distortion and 30 dB improvement of the noise floor at 1 kHz, compared to that of same DCR without this technique [35].

2.5 New Possibilities for MMR with RFICs

This section discusses how emerging RFIC technology has opened new possibilities to design and develop radios with large, multiband tuning ranges. An example has already been shown for chopping in DCR in the previous section. First, we describe the reason behind the growing popularity

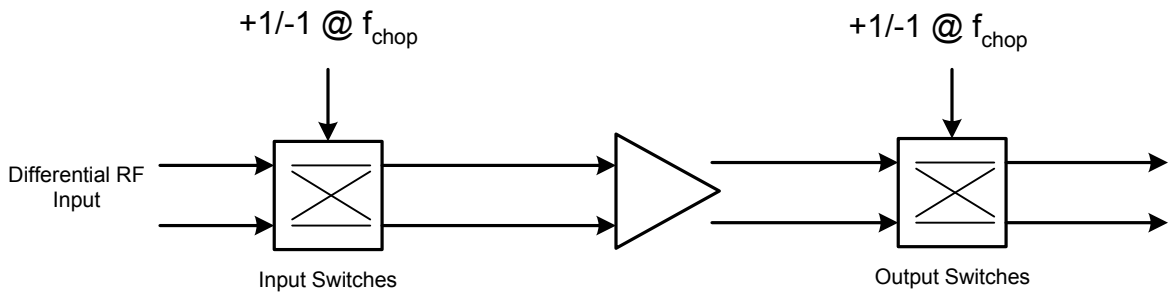


Figure 2.16: Illustration of differential implementation of the chopper stabilization technique.

of the CMOS process for RFICs. Then we present an example of a recent CMOS–based direct conversion RFIC. We present some reasons why multiplexers become important to achieve MMR using these RFICs.

CMOS is very popular in modern digital circuitry due to its high density, high speed, and inexpensive process. However, it is very difficult to implement RF circuity in CMOS due to process variations and inaccurate design models [37]. In recent years, these problems have been greatly mitigated. Since CMOS has the capability of implementing dense circuitry at reduced cost, multiple transceivers can be implemented on a single chip, or multiple low–cost RFICs can be connected in parallel for multiband operation. It is also possible to implement a lot of "tweaking parameters" inside the RFIC to increase the performance of MMR. For example, these tweaking parameters can be implemented as internal capacitors in series with internal switches. Fine adjustments in filter responses is then possible by selecting capacitors to be added or removed as needed. Another advantage is that the power consumption and cost of the MMR can be greatly reduced.

A few examples of recent work in this area includes an SDR receiver developed by Bagheri *et. al.* in [38]. This is a 90 nm CMOS DCR operating in the 800 MHz to 5 GHz band with reconfigurable bandwidth from 100 kHz to 8 MHz. Another transceiver RFIC, which is configurable from 700 MHz to 3.8 GHz for protocols with bandwidth of 25 kHz to 20 MHz, has been developed by Bitwave Semiconductor in 130 nm CMOS [39]. This IC has only one receive and one transmit path. Terocelo [1] has developed an RFIC for 500 MHz to 6 GHz in 65 nm CMOS. In 2007, Motorola Research Laboratories developed a multiband direct conversion RFIC using 90 nm CMOS [40].

[1] http://www.terocelo.com

Figure 2.17 shows the functional block diagram of this RFIC. A detailed description including a performance analysis of this IC is presented in Chapter 7. This IC is designed for the operation from 100 MHz to 2.5 GHz. Five receive paths and three transmit paths have been implemented in the same IC. Since they share a common baseband section, only one receive and one transmit path can be selected at a time. However, since the anticipated cost is so low (approximately $50 [41]), it is possible to use multiple chips without much impact on MMR cost. Future chips with multiple independent baseband sections are possible. The most recent versions of this IC have integrated ADC/DAC. We use version 4 of this chip (as shown in Figure 2.17) to build a prototype MMR for public safety application as described in Chapter 7.

Note that there are two categories of RFIC: Those with a single receive path, and those with multiple receive paths. If we want to build a MMR using an RFIC having single receive path then we require multiple RFICs to cover multiple bands. On the other hand, a single RFIC with multiple receive paths itself might be sufficient for a MMR. Figure 2.18 shows two kinds of possible MMR architectures using RFIC and a multiplexer. Figure 2.18(a) shows a "blocking" architecture in which one single RFIC is used and each of its receive paths are connected to the multiple channels of a multiplexer. This is the scheme that is possible with Motorola RFIC version 4, and which is implemented in the prototype MMR in Chapter 7. On the other hand, Figure 2.18(b) shows a "non-blocking" architecture in which multiple RFICs are connected to the multiple channels of a multiplexer. The advantage of "non-blocking" architecture is that it is possible to receive or transmit on multiple channels simultaneously.

From the above discussion it is clear that in order to get the advantage of these RFICs for MMR, an RF front end is required which channelizes the incoming RF signal into separate bands (i.e., implementation of selectivity) for the receive paths of the RFIC. We prefer to use a multiplexer to implement this RF front end.

2.6 Summary

This chapter presented a brief review of the various parts and parameters related to design of a receiver. "Divide-and-conquer" superheterodyne architecture is favored to design MMR presently

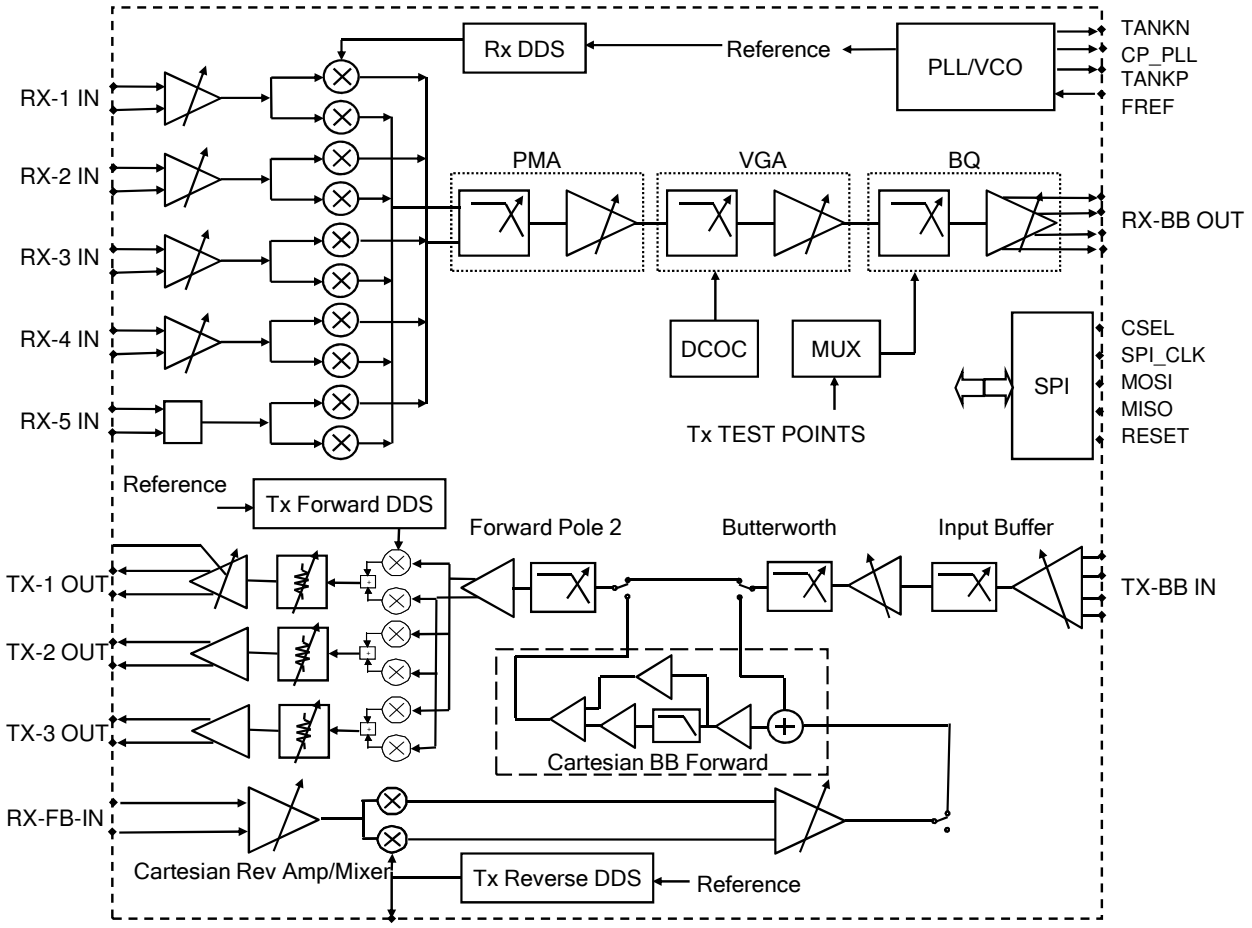
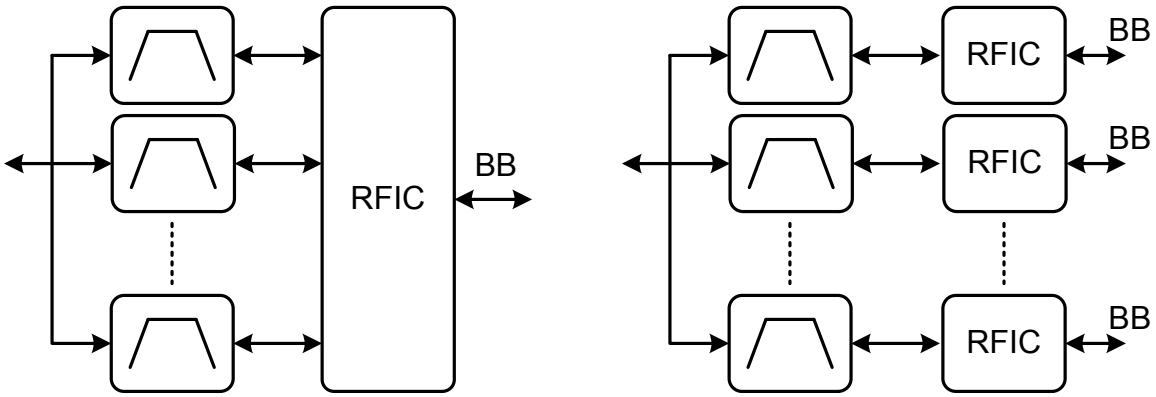


Figure 2.17: Functional block diagram of the Motorola RFIC version 4 (used with permission, see Appendix I).



(a) Blocking (b) Non-Blocking

Figure 2.18: Possible architectures to design a MMR using multiplexer and RFICs.

due to its ability to cover large tuning range with the necessary selectivity. However the complexity, cost, and power requirements increase with increase in the number of desired frequency bands. Direct conversion architecture is emerging as an alternative due to the advantages of small form factor, low cost, reduced bill of materials, and low power consumption. Traditionally this architecture is suffered from multiple number of implementation problems, however, most of which can now be mitigated to a far greater extent due to the advancement of CMOS RFIC technology. Moreover, the emergence of practical inexpensive CMOS RFICs, are motivating us to design a MMR using these wideband direct conversion RFICs. However, in order to design a MMR using a single traditional antenna, a new kind of RF front–end consisting of a multiplexer is needed for the antenna–receiver integration. As a first step in identifying a suitable multiplexer design, the next section describes the fundamental limits of antenna–receiver matching and also discusses some traditional techniques to achieve wideband matching.

Chapter 3

Antenna–Receiver Interfacing

Wideband impedance matching (i.e., matching over large fractional bandwidths) is made difficult by the fundamental limitations of impedance matching. This chapter reviews these limitations as well as various wideband matching techniques and their limitations. This chapter is organized as follows. Section 3.1 ("Antenna Matching & Parameters") describes some basic parameters of matching. Fundamental limitations of matching are reviewed in Section 3.2 ("Fundamental Limitations"). Section 3.3 ("Wideband Matching using Passive Components") summarizes techniques for wideband matching using passive components. Section 3.4 ("Antenna Tuning using Variable Reactors") reviews some current research trends in antenna matching using variable reactors. In Section 3.5 ("Non-Foster Impedance Matching"), a wideband matching technique using *active* components is briefly described. This chapter is summarized in Section 2.6 ("Summary").

3.1 Antenna Matching & Parameters

Usually, receivers are designed assuming frequency–independent input impedance of standard real value (e.g., 50Ω), shown as Z_L in Figure 3.1. However, over wide tuning ranges the antenna impedance Z_A is frequently quite different from Z_L and it varies significantly with frequency, as shown in Figure 1.4. An impedance–matching network is used to manage the impedance mismatch between the antenna and the receiver as shown in Figure 3.1.

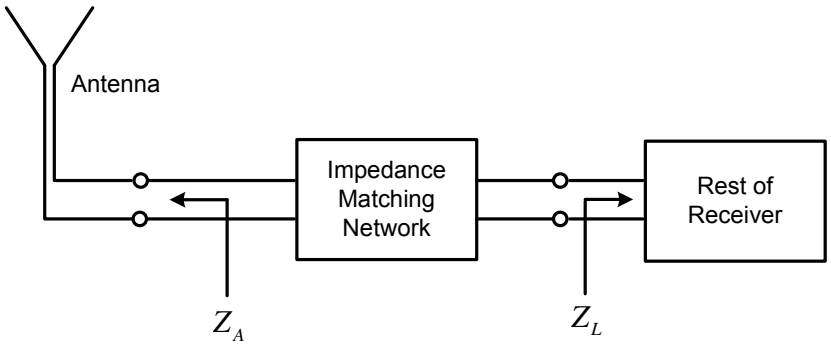


Figure 3.1: General configuration for antenna matching.

Usually, the impedance–matching network is designed to provide the maximum power transfer. From this perspective, the ideal impedance–matching network has three requirements: (1) input impedance should be the conjugate of the antenna impedance, i.e., Z_A^*, (2) the network should be lossless, i.e., no ohmic elements (especially resistors) should be present in the matching circuit, and (3) the output impedance should be Z_L^*, i.e., real-valued. A matching circuit having these three properties will result in all available power (i.e., what the antenna can generate into a conjugate matched load) being delivered to the rest of the receiver. The question of how good the matching actually needs to be depends on the requirements of the application.

Antenna–receiver impedance–matching is commonly narrowband in nature (i.e., bandwidth is 10% or less). For example, a design is optimized for the center frequency, but the result works well enough over a small band of frequencies around the design frequency. The match can be perfect at the center frequency, but degrades away from it. However, wideband matching is needed for the MMR applications identified in Chapter 1, since these operate over large fractional bandwidths possibly using a single antenna. The ability to achieve an acceptable match over a bandwidth of 10% or more is fundamentally limited by a bound on the product of gain and bandwidth. Section 3.2 ("Fundamental Limitations") discusses this in more detail.

The impedance match between an antenna and the receiver can be characterized in terms of voltage standing wave ratio (VSWR), defined as

$$\rho = \frac{1 + |\Gamma|}{1 - |\Gamma|}, \tag{3.1}$$

where Γ is the voltage reflection coefficient at the antenna–receiver interface. When there is no impedance matching network this is defined as

$$\Gamma = \frac{Z_L - Z_A^*}{Z_L + Z_A^*}. \tag{3.2}$$

In this dissertation, it is also useful to characterize the antenna–receiver interface in terms of its impedance mismatch efficiency (IME). IME is defined as the fraction of power available at the antenna terminals which is successfully transferred to the receiver, which is simply $1 - |\Gamma|^2$. This is nominally 1 but is often much less than 1 due to the impedance mismatch. IME determines how much power is available to the receiver due to impedance mismatch. However, the performance of the impedance matching network, specifically the efficiency of power transfer from antenna to the input of the receiver (excluding the matching circuit) should be known. This is given by another performance metric known as transducer power gain (TPG). TPG is defined as the ratio of power delivered by a matching network to the rest of the receiver to the power delivered to a conjugately–matched load attached directly to the antenna.

The concept of TPG can be demonstrated using Figure 3.2. In this figure, the antenna is represented by the impedance Z_A in series with the voltage source v_A, and the receiver (excluding the matching network) is represented by the impedance Z_L. P_A is the power available from the antenna into a conjugate–matched load, P_{in} is the power transferred to the matching network, P_{out} is the power output from the matching network (incident on the rest of the receiver), and P_L is the power transferred to Z_L (rest of the receiver). Thus:

$$\begin{aligned} \text{TPG} &= \frac{P_L}{P_A} \\ &= \frac{P_L}{P_{out}} \cdot \frac{P_{out}}{P_{in}} \cdot \frac{P_{in}}{P_A} \\ &= G_{ref,out} \cdot G_{match} \cdot G_{ref,in} \end{aligned} \tag{3.3}$$

where $G_{ref,in}$ and $G_{ref,out}$ is the power gain due to reflection at the input and output of the matching network, respectively; and G_{match} is the power gain of the matching circuit assuming perfectly matched input and output. According to the analysis presented in [42], $G_{ref,in}$ and

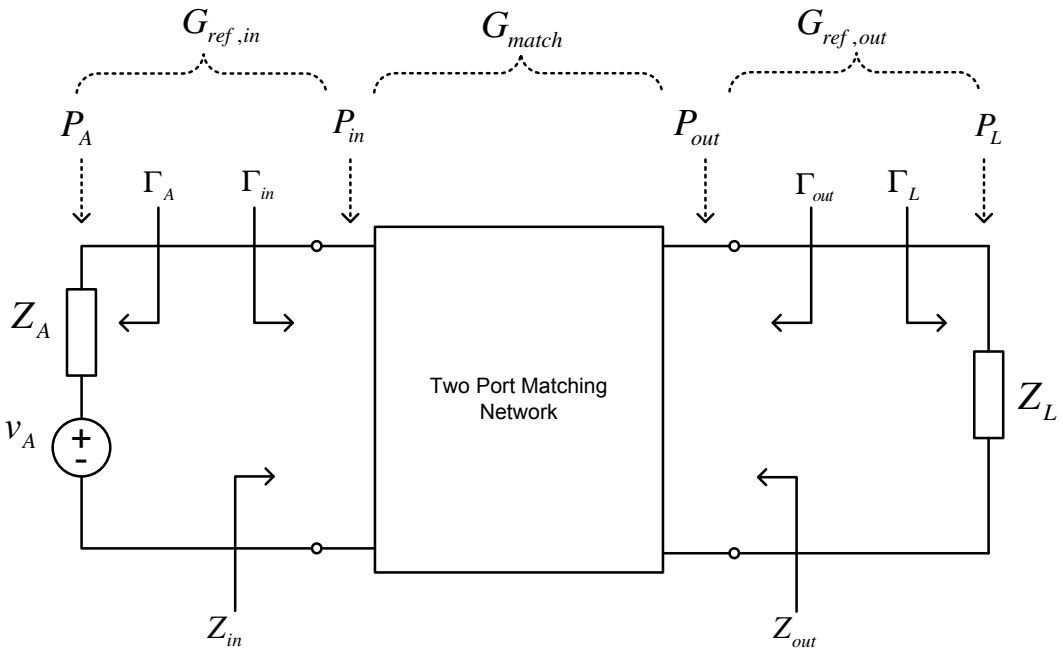


Figure 3.2: Block diagram to calculate transducer power gain.

$G_{ref,out}$ are

$$G_{ref,in} = \frac{1 - |\Gamma_{in}|^2}{|1 - \Gamma_A \Gamma_{in}|^2} , \tag{3.4}$$

$$G_{ref,out} = \frac{1 - |\Gamma_L|^2}{|1 - \Gamma_{out} \Gamma_L|^2} , \tag{3.5}$$

where Γ_A, Γ_{in}, Γ_{out}, and Γ_L are the voltage reflection coefficients indicated in Figure 3.2. Also:

$$\Gamma_A = \Gamma_{in}^* = \frac{Z_A - Z_{in}^*}{Z_A + Z_{in}^*}, \tag{3.6}$$

$$\Gamma_L = \Gamma_{out}^* = \frac{Z_L - Z_{out}^*}{Z_L + Z_{out}^*}, \tag{3.7}$$

where Z_{in} and Z_{out} are the input and output impedance of the matching network indicated in Figure 3.2. Substitution of Equations 3.4 and 3.5 into 3.3 yields:

$$\text{TPG} = \frac{1 - |\Gamma_{in}|^2}{|1 - \Gamma_A \Gamma_{in}|^2} G_{match} \frac{1 - |\Gamma_L|^2}{|1 - \Gamma_{out} \Gamma_L|^2}. \tag{3.8}$$

As a special case, if input and output of the matching network is completely matched with the

impedance of the source and load, respectively, then the value of all the reflection coefficients would be zero and we have TPG = G_{match}.

3.2 Fundamental Limitations

Matching may be difficult, so it is important to know the actual requirements, and it is also useful to know the fundamental limits, so that we can get the idea about how reasonable our matching goal or requirement is. This section presents some of the fundamental limitations of antenna matching.

3.2.1 Bode–Fano Limit

It is not always possible to get unity TPG even if there is no loss in the matching circuit, due to the trade-off between the bandwidth of a matching circuit and the TPG through that matching circuit. This trade-off has been described by Bode and Fano [43, 44]. They primarily presented a systematic study of the origin and nature of the theoretical limitations on the tolerance and bandwidth of match and of their dependence on the characteristics of the given load impedance. The basic idea of their work is: while the operating bandwidth at the input to the matching circuit increases as a function of the number of tuning circuits, there is an upper limit to the bandwidth that can be realized. The first investigation related to this fundamental limit was made by Bode for the case of an impedance Z_L consisting of a resistance R in parallel with a capacitance C, and he showed that in this case the fundamental limitation takes the form [44]

$$\int_{-\infty}^{+\infty} \ln\left|\frac{1}{\Gamma(\omega)}\right| d\omega \leq \frac{\pi}{RC} \qquad \text{(Parallel RC)}. \tag{3.9}$$

Let us assume the voltage reflection coefficient $\Gamma(\omega)$ is constrained to be unity outside the frequency range ω_L to ω_H and $\Gamma(\omega)$ is constrained to be constant in ω_L to ω_H, as shown in Figure 3.3. Then, Equation 3.9 can be solved for the minimum reflection coefficient

$$\Gamma_{min} = \exp\left(-\frac{\pi}{B\omega_0 RC}\right) \qquad \text{(Parallel RC)} \tag{3.10}$$

where $\omega_0 \equiv \sqrt{\omega_H \omega_L}$ and $\mathrm{B} = (\omega_H - \omega_L)/(\omega_H \omega_L)$. This reflection function, which is illustrated in Figure 3.3, can be fit exactly using a polynomial of infinite degree, corresponding to a matching network having infinite number of elements. As a result the above reflection value of $|\Gamma_{min}|$ can be achieved only with a matching network having infinite number of circuit elements. The following are two insights that can be gained from Equations 3.9 and 3.10:

1. To obtain the best possible match over the widest bandwidth, the reflection coefficient should be equal to one outside of the passband, as this allows for $|\Gamma|$ to be minimized inside the passband.

2. If the bandwidth needs to be increased, this can be done only by decreasing the TPG, i.e., increasing $|\Gamma|$) through the matching circuit.

The above result is specific to parallel RC impedances, whereas we are interested to know the fundamental limitations of matching for antenna–receiver integration generally. In general this is quite difficult, however there are approximations relevant to a few more special cases. For example, the impedance of an electrically–short antenna can be approximated by a series RC or series RL circuit. The following equations show the Bode–Fano bounds for the series RC and series RL impedances [45]

$$\int_{-\infty}^{+\infty} \omega^{-2} \ln \left| \frac{1}{\Gamma(\omega)} \right| d\omega \leq \pi RC \qquad \text{(Series RC)} \tag{3.11}$$

$$\int_{-\infty}^{+\infty} \omega \ln \left| \frac{1}{\Gamma(\omega)} \right| d\omega \leq \frac{\pi R}{L} \qquad \text{(Series RL)} \tag{3.12}$$

and the resulting Γ_{min}'s assuming $\Gamma(\omega)$ is the form of Figure 3.3 are

$$\Gamma_{min} = \exp\left(-\frac{\pi RC\omega_0}{\mathrm{B}}\right) \qquad \text{(Series RC)} \tag{3.13}$$

$$\Gamma_{min} = \exp\left(-\frac{\pi R}{L\omega_0 B}\right) \qquad \text{(Series RL).} \tag{3.14}$$

Although these bounds are useful to know the maximum achievable bandwidth given a TPG constraint, in reality it is not reasonable to specify a matching circuit with an infinite number of circuit components. Fano obtained a modified version of the relationship presented above (Equation 3.9)

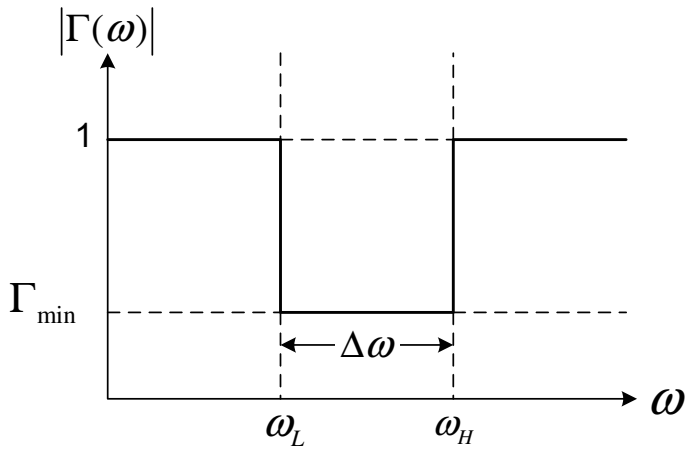


Figure 3.3: Illustration of the Bode-Fano limit.

for a matching circuit using a n^{th} order Chebyshev topology [43], and finds

$$\Gamma_{min} = \frac{\cosh nb}{\cosh na} \tag{3.15}$$

where the values of a and b can be estimated as follows [45]

$$a = \sinh^{-1}\left[\delta\left(1.7\delta^{-0.6} + 1\right)\sin\frac{\pi}{2n}\right] \tag{3.16}$$

$$b = \sinh^{-1}\left[\delta\left(1.7\delta^{-0.6} - 1\right)\sin\frac{\pi}{2n}\right] \tag{3.17}$$

where the matching parameter $\delta = 1/(BQ_L)$, and Q_L is defined as

$$Q_L = \frac{|X_s|}{R_s} = \frac{R_p}{|X_p|} \tag{3.18}$$

where the impedance to be matched (i.e., Z_L) is represented as R_s and X_s connected in series, or R_p and X_p connected in parallel.

As an example of the bound used in a practical application, Figure 3.4 shows the bandwidth calculated for various VSWR (ρ) for a monopole antenna 20 cm long with 5 mm radius. The antenna impedance is calculated using the TTG method, and approximated as a series RC circuit where the values of R and C are computed at 156 MHz. Equation 3.13 is then used to calculate the bandwidth. It should be noticed that coverage of the frequency range 138–174 MHz (36 MHz

bandwidth around 156 MHz a public safety band) can be achieved only for $\rho \geq 7$, and that better VSWR is possible only by reducing the bandwidth.

3.2.2 Foster's Reactance Theorem

Foster's Reactance Theorem [46] states that the first derivative of the reactance of a passive lossless circuit with respect to frequency is always positive. This is obvious for single inductors and capacitors, as shown in the following equations

$$X_L(\omega) = j\omega L \; ; \; \frac{\partial}{\partial \omega}(X_L(\omega)) = jL > 0 \tag{3.19}$$

$$X_C(\omega) = \frac{-j}{\omega C} \; ; \; \frac{\partial}{\partial \omega}(X_C(\omega)) = \frac{j}{\omega^2 C} > 0 \tag{3.20}$$

This gives additional insight as to why broadband matching is very difficult using only passive reactances. This can be demonstrated using an example. If it is desired to perfectly match the antenna impedance shown in Figure 1.4 to a purely resistive input impedance of a receiver then it is needed to use a matching circuit which exactly cancels the antenna reactance over the desired bandwidth. Over the frequency range where the slope is positive (including resonance), the corresponding ideal matching circuit's input reactance has a negative slope, and therefore cannot be achieved using only passive lossless reactive components, such as capacitors and inductors. While it is possible for the matching circuit to cancel the reactance exactly at one frequency, it is not possible to cancel the reactance exactly over a range of frequencies.

An attempt to sidestep this limitation is Non–Foster Matching, discussed in Section 3.5.

3.3 Wideband Matching using Passive Components

This section reviews some existing wideband matching techniques using fixed–value passive components. Section 3.3.1 ("Analytical Techniques") discusses some classical analytical techniques and their limitations, whereas Section 3.3.2 ("Real Frequency Technique") presents a popular iterative technique. The model used is as shown in Figure 3.5, which shows an antenna of known impedance $Z_A(f) = R_A(f) + jX_A(f)$ connected to a receiver modeled as a matching network in cascade with

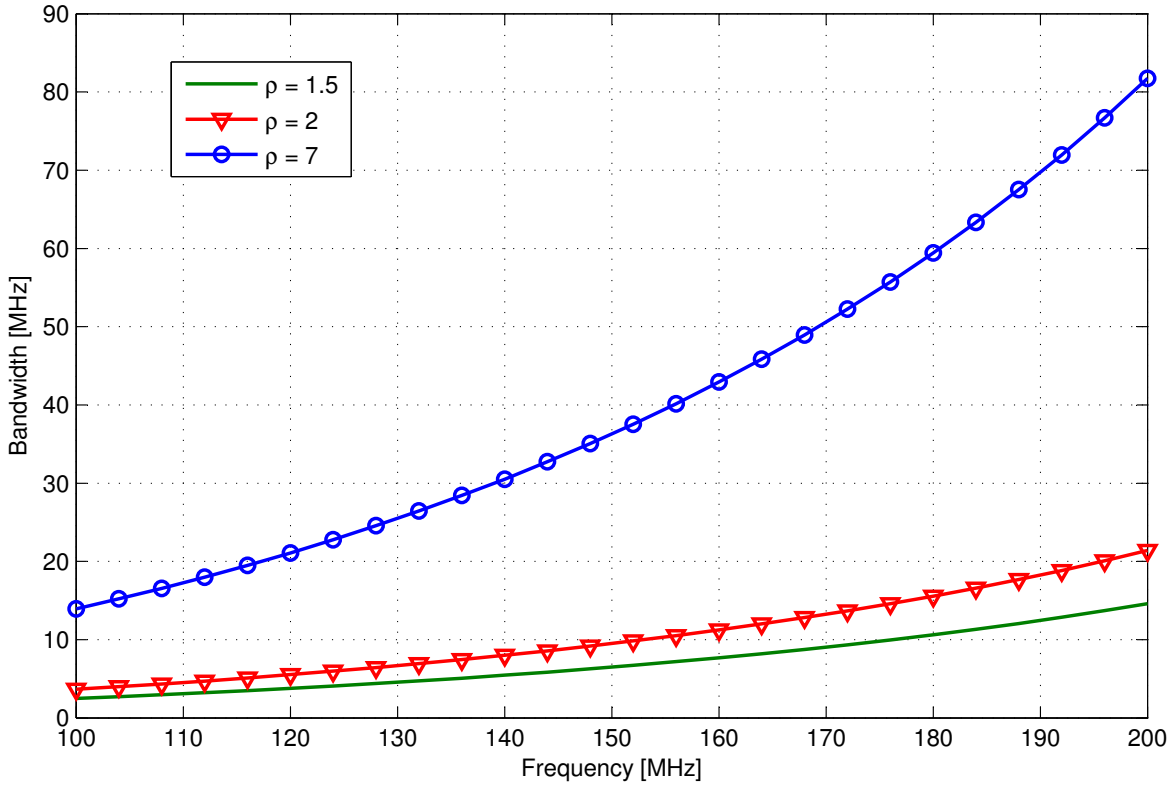


Figure 3.4: Matching bandwidth for various VSWR estimated using an approximate form of the Bode–Fano bound for a monopole antenna 20 cm long with 5 mm radius.

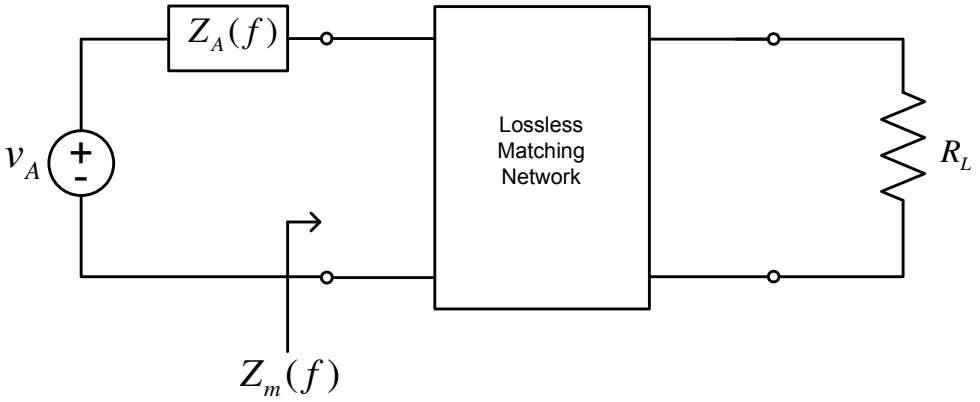


Figure 3.5: Configuration to demonstrate the matching techniques.

a resistive load R_L.

3.3.1 Analytical Techniques

An example of a classical broadband matching technique using passive reactances is discussed in [47]. The first step is to define how good the match should be at the center frequency, i.e. selecting the value of ρ (input VSWR). Subsequent steps are most easily explained in terms of the Smith Chart. A constant ρ (VSWR) circle and impedance curve are drawn. The next step is to add reactance (L or C, series or parallel) in such as a way that the impedance at mid–frequency is shifted towards the constant VSWR circle as much as possible. The second network element is selected to position the mid-frequency impedance to accept the maximum permissible VSWR, and the remaining two elements are selected to "wrap" or shift the end portions of the impedance curve (i.e. impedance at the high and low frequencies in the desired bandwidth) to within the desired VSWR circle. Thus the first two elements set the efficiency of the match, and the last two elements determine the bandwidth.

Demonstrating this method, Figure 3.6 shows a four–element matching circuit to match a monopole antenna 1.97 m long and 21 mm diameter (This antenna to be used in field experiments in Chapter 4) to a 50Ω load over the frequency range 10–28 MHz. This design assumes the simulated impedance of the antenna shown in Figure 4.15. To find out the Bode–Fano limit, the antenna is modeled as a series RC impedance, the values ($R = 4.9\Omega$ and $C = 32.0$ pF) of which are calculated

from the antenna impedance at the geometric mean frequency (i.e., 16.7 MHz) of this frequency range. According to the approximate Bode–Fano limit, the maximum theoretical TPG is then –10.4 dB, which is calculated using Equation 3.13 with TPG (in dB) $= 10\log_{10}(1 - |\Gamma_{min}|^2)$. Figure 3.7 shows the TPG achieved by the designed four–element network. This matching circuit clearly performs well around 19 MHz but quickly degrades at higher and lower frequencies. Although the match could be improved by adding more components to the circuit, the design process using this graphical method will become intractable. As is, this matching circuit provides about 5 MHz bandwidth for –10.4 dB minimum TPG.

Other approaches allow matching circuits of higher order, but are based on assumptions about the source impedance; e.g., requiring certain network topologies such as series RC or parallel RL. An example is a method described by Rhea [48, 49]. He describes a matching technique that begins with a Chebyshev filter with constant (e.g. 50Ω) termination impedance and modifies it. This method is only applicable to antenna impedance which can be modeled as series RC or parallel RL. In this method the reactive part of the impedance of the antenna is absorbed in the filter reactance, i.e., the reactance of the component (in the filter) which is close to the antenna needs to be changed in such a way that the combination of the antenna reactance and the new value of this component's reactance are equal to the original value of this reactance. The procedure is as follows: First, a Chebyshev filter for which the input and output impedances are both equal to the load impedance is designed for the desired band of frequencies. Then the value of absorption reactance can be found from

$$C_{series} = \frac{B}{2\pi g R_A f_c} \qquad \text{(Series RC)} \tag{3.21}$$

$$L_{shunt} = \frac{B \times R_A}{2\pi g f_c} \qquad \text{(Parallel RL)} \tag{3.22}$$

where f_c is the geometric center frequency, B is the fractional bandwidth, g is the value of the Chebyshev lowpass prototype element (component value of the prototype with termination impedance 1Ω) adjacent to the source [50], R_A is the source resistance, C_{series} is the minimum series capacitor value which can be absorbed, and L_{shunt} is the minimum shunt inductor value which can be absorbed.

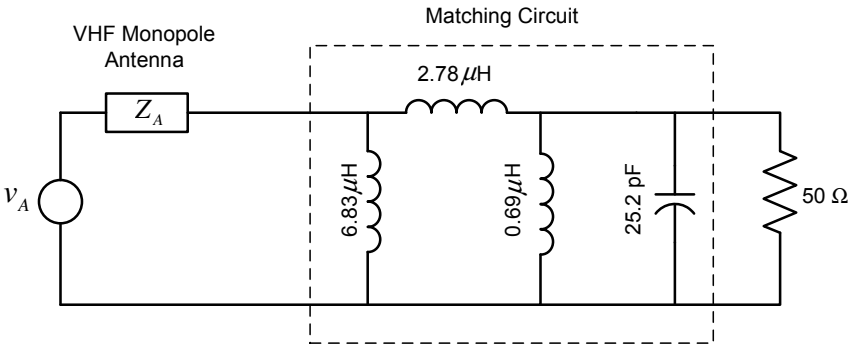


Figure 3.6: Four element matching network using method in [47].

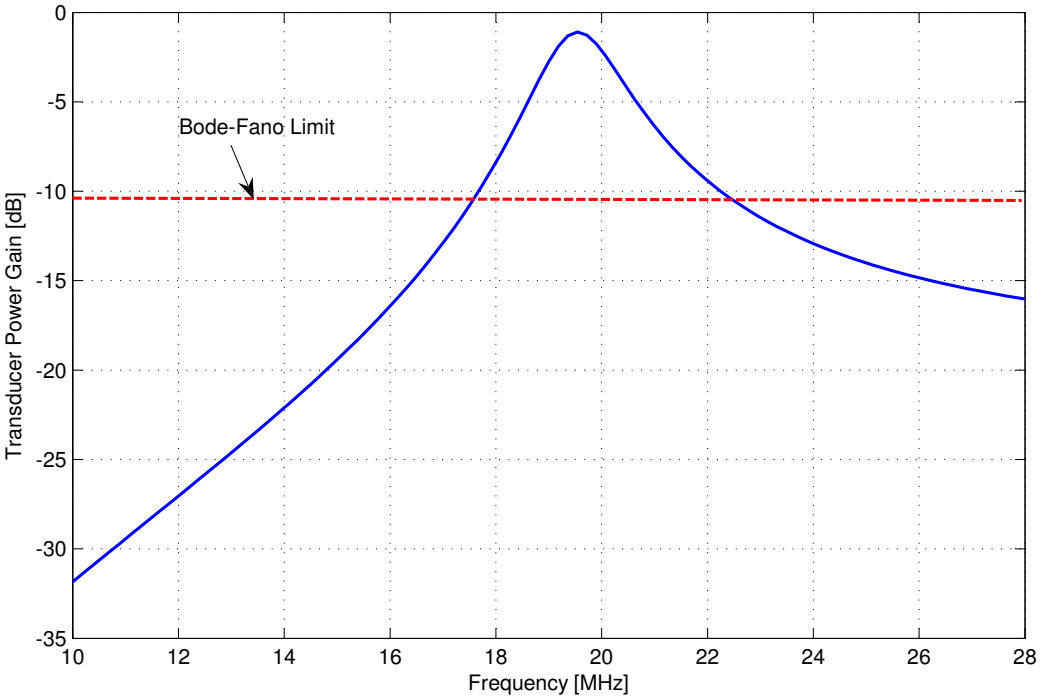


Figure 3.7: Performance (TPG) of the four element matching network.

This method is simple to use, however does not work for all possible RC or RL. In particular, it fails for the large reactances; e.g., for electrically–short antennas. Specifically, the ability to absorb the reactive impedance of the source decreases as the required bandwidth increases (which of course is expected).

This limitation can be demonstrated using an example. Suppose we wish to match the same antenna described earlier in this section with a 50Ω load from 10 to 28 MHz using a seven-section Chebyshev bandpass filter. The minimum value of series capacitance that can be absorbed can be found using Equation 3.21. Here, $f_c = 16.73$ MHz, B=1.1, and $|\Gamma_{min}| = 0.95$ (this Γ_{min} is calculated from the Bode–Fano limit). The required ripple of the Chebyshev filter is

$$L_A = -10 \log(1 - |\Gamma_{min}|^2). \tag{3.23}$$

For a required passband ripple of 10.4 dB, the final g-value for a seven-section Chebyshev filter is 9.51, and the value of C_{series} is 224.6 pF; i.e., a series capacitance of 224.6 pF or larger can be accommodated using this method. Since the series capacitance for our matching problem is 32.0 pF (calculated from the series RC approximation of the impedance of the VHF monopole at the geometric center frequency of 16.7 MHz in frequency range 10–28 MHz), this method fails to produce a realizable design. Our investigation reveals that for this particular antenna this method is useful in the frequency range 34.5 MHz to 37.5 MHz only (note that the approximate resonance frequency of this antenna is 36.0 MHz).

A more thorough treatment of broadband matching using analytic methods is presented by Chen in [51–54]. Even though his methods are quite general, they are limited once again by the fact that only certain categories of complex impedances can be accommodated; e.g., parallel RC, parallel RC with series L, and certain others. In particular this methodology does not apply to antenna impedance models we are interested in, such as the series RC model (for electrically short antennas), and the TTG circuit model (over large frequency ranges). A detailed demonstration of how this method fails to work for antenna impedances obtained from the TTG model is presented by Taylor in [27, Appendix D].

3.3.2 Real Frequency Technique

Having demonstrated the limitations of closed form analytical techniques, we now consider a popular iterative numerical technique. In [55, 56], Carlin introduces a method called the Real Frequency Technique (RFT) to achieve broadband matching of an antenna having arbitrary impedance to a resistive load. An important advantage of this method with respect to methods based on circuit models is its capability to work with experimental (i.e., measured) impedance data. For this reason, this technique is advantageous for matching impedances not easily expressible in forms of circuit models, such as antennas. The RFT method consists of the following two steps to find out and realize the impedance $Z_m(f) = R_m(f) + jX_m(f)$ of the matching circuit shown in Figure 3.5:

1. *Optimization of* $Z_m(f)$

   The purpose of the optimization step is to find a realizable $Z_m(f)$ that optimizes TPG over the desired frequency range. To begin, $R_A(f)$ is approximated by a number of straight line segments, i.e., in a piecewise linear fashion, with frequency break points at $0 < f_0 < f_1 \ldots < f_n$ corresponding to the available impedance data values. Once this is done, $R_A(f)$ is entirely specified in terms of the slopes of the line segments, which may now be viewed as unknown parameters for the optimization problem. The next step is to find the slopes which optimize TPG at the frequency break points. Once the line segments describing $R_m(f)$ have been found, the corresponding reactance function $X_m(f)$ can be determined from the Hilbert transform [57, Sec. 3.4].

2. *Realization of* $Z_m(f)$

   After finding $Z_m(f)$, the next step is to find a lossless LC network that has this impedance. The process starts by constructing $\hat{R}_m(f)$, an approximation to the original piecewise linear $R_m(f)$ in the form of a rational polynomial, employing the methods suggested by Carlin and Yarman in [56]. Next step is to convert $\hat{R}_m(f)$ to $\hat{Z}_m(s)$, a rational polynomial, where $s = j\omega$ is the complex frequency, using the Gerwetz procedure [45]. The final step is the interpretation of $\hat{Z}_m(s)$ as a lossless LC network terminated in R_L using the Darlington synthesis procedure [57].

Yarman [58] improved this technique, eliminating the numerical evaluation of the Hilbert transformation to improve the computational efficiency. The main idea of his modification is the generation of the unit–normalized scattering parameters S_{11}, S_{12}, S_{21}, and S_{22} of the lossless matching circuit from the unknown – but initialized – numerator polynomial $h(p)$ of the unit–normalized reflection coefficient $S_{11} = h(p)/g(p)$. The term $g(p)$ is the Hurwitz polynomial and can be calculated from $h(p)$. The unknown real coefficients $h_0, h_1, h_2, \ldots, h_n$ of $h(p)$ are determined using a nonlinear optimization routine such that TPG is maximized over a specified pass band. The matching network can then be realized as a lossless network with resistive termination and synthesized using long division from these optimized scattering parameters.

Figure 3.8 shows the matching circuit designed using this version of RFT (known as simplified RFT) to match the same antenna described earlier to a 50Ω load for 10–28 MHz. The performance of this circuit is presented in Figure 3.9. This matching circuit is designed using the MATLAB code supplied in [59] using the simulated impedance data shown in Figure 4.15. Note that this matching circuit provides much more uniform performance over the desired frequency range. In this case 14.4 MHz bandwidth is achieved for –10.4 dB minimum TPG. The improvement in performance compared to the four–element technique (Figure 3.7) is significant, but comes at the expense of a greater number of matching sections.

Although the RFT method seems very attractive to solve the wideband matching problem, it is very complicated to implement. Optimization is an inherent part of this technique, and it is generally unconstrained and multidimensional in nature. Although there are other techniques available to perform this optimization [60], there is no guarantee that the optimization will converge, or converge to the global optimum.

3.4 Antenna Tuning using Variable Reactors

When the achievable bandwidth–TPG trade–off is insufficient for an application, the use of variable reactances may be considered to increase the range of frequencies over which a TPG requirement can be met. Figure 3.10 shows the concept of antenna-receiver interfacing using variable reactors. By changing the impedance of reactors we can achieve good impedance matching at at least one

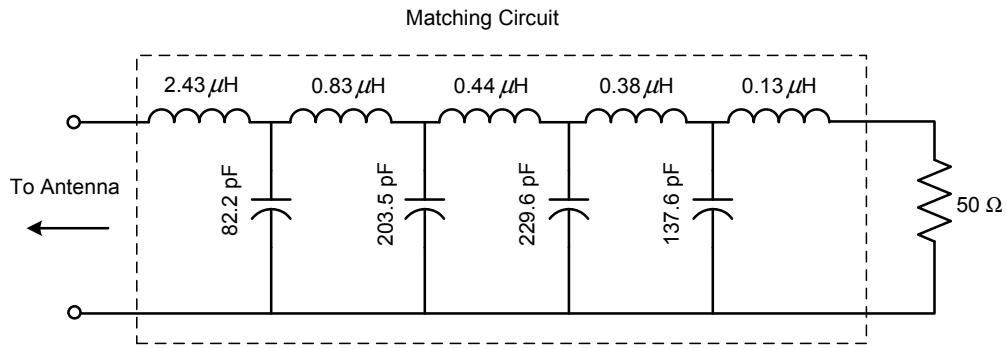


Figure 3.8: Matching circuit calculated using RFT method.

frequency at a time.

There are several methods for realizing variable reactances [61]. One is to use fixed inductors or capacitors in banks in where the switching within these banks can be done using electromechanical RF switches, PIN diodes or other semiconductor switches, or RF microelectromechanical switches (MEMS). Another approach is to use mechanically–variable reactances such as motor-driven geometry changers (inductors and capacitors) or varactor diodes (voltage-variable capacitors). Examples of the latter are: in [62], Zhou and Melde developed a compact wideband antenna tuner (for 0.9–1.3 GHz, 2.25–2.75 GHz, and 3.6–5.0 GHz) using four varactor diodes, which are variable from 0.5 to 6 pF each. Although their tuner significantly improves match over about a 20% bandwidth around the tuned frequency, the performance of matching is worse outside this range. Park and Rebeiz [63] also present a tunable filter with three different predefined bandwidth characteristics using variable reactors. The tuner is demonstrated in the frequency range 800-1400 MHz with 5% bandwidth.

Examples of MEMS-based tunable filters are introduced by Entesari and Rebeiz in [64, 65]. Although MEMS have great potential particularly in terms of size and power consumption, some intrinsic drawbacks remain. These include low switching speed, limitation in power handling capacity, high actuation voltage, low reliability, and complex packaging requirements due to vulnerability to environmental conditions [22]. Thus, while it is clear that MEMS exhibit great potential for use in variable matching circuits, this technology not yet quite ready and is not expected to be sufficiently mature for some years to come.

For both types of antenna tuners, there is the issue that implementation of antenna–receiver match-

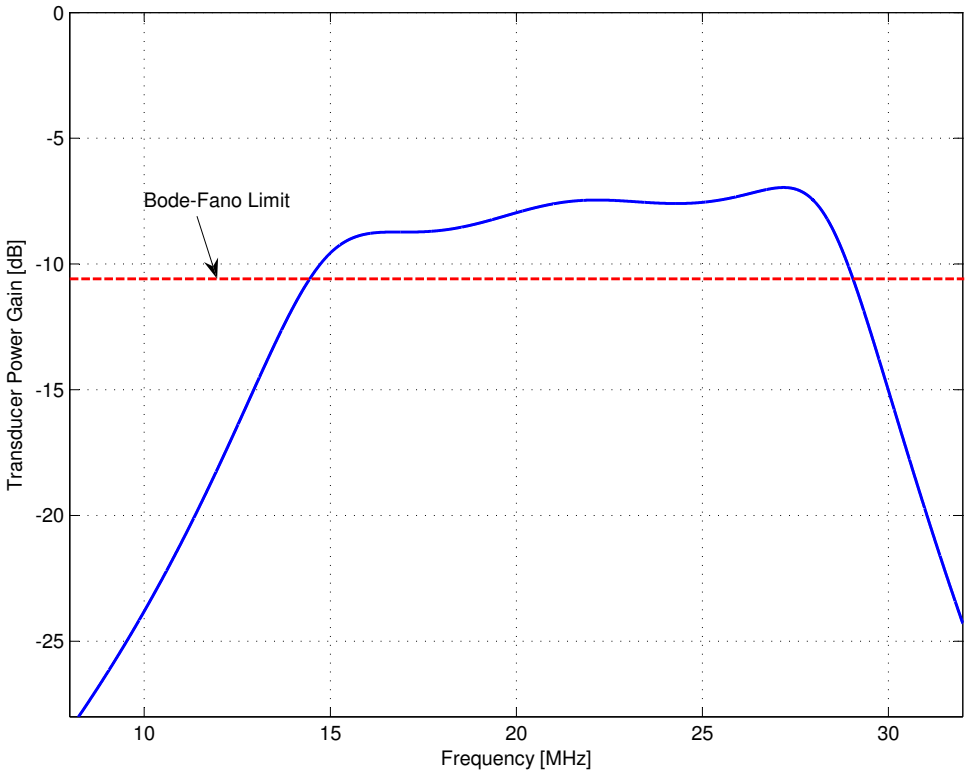


Figure 3.9: Performance (TPG) of the matching circuit calculated using RFT method. Compare to Figure 3.7.

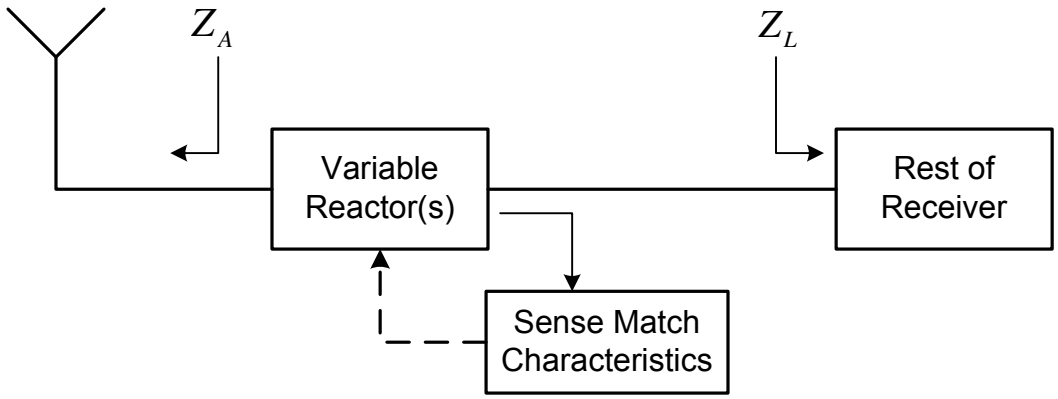


Figure 3.10: Antenna tuning using variable reactors.

ing in this way is bulky and limited to providing one band at a time. Since in emerging MMR applications it is desired to have operation on multiple bands simultaneously (as shown in Figure 2.18) it is needed to implement multiple variable matching circuits in parallel, further increasing bulk and cost.

3.5 Non-Foster Impedance Matching

The matching limitation using passive components described in Section 3.2.2 ("Foster's Reactance Theorem") can in principle be overcome using *active* elements in the matching circuit. Unlike passive elements, active elements can have negative reactance slope. This bypasses the fundamental gain–bandwidth limitations imposed by Foster's Reactance Theorem, and is called Non–Foster impedance matching. Figure 3.11 shows a comparison between traditional matching using passive reactances, and the Non–Foster matching concept.

Non-Foster matching can be achieved by using active circuits called negative impedance converters (NICs) [66, 67]. An ideal NIC is a two-port device for which the impedance at one port is the negative of the impedance connected to the other port. Figure 3.12 shows a canonical "floating" NIC circuit implemented using an ideal op–amp.

Bahr (1977) demonstrated Non–Foster matching to a short monopole antenna for the frequency range 30–60 MHz in [68]. The current state of the art is summarized in [69] and [70]. An example of non-Foster matching of a 125 MHz-resonant monopole using a floating NIC based on NE85630 bipolar junction transistors (BJTs) is provided in [70]. Using a traditional technique to match this antenna at 60 MHz with an impedance bandwidth of about 5%, a peak efficiency of about 83% is achieved. The non-Foster match is shown to achieve $\geq$83% efficiency from 65 MHz to at least 90 MHz. The efficiency declines to 80% at 60 MHz and the matching circuit becomes unstable below about 30 MHz. In [69], a similar investigation is described using another NE85630-based floating NIC to match a 6–inch monopole antenna. In this case, it is shown that the non-Foster match improves sensitivity by $\sim$ 6 dB over the band 20–110 MHz with respect to a traditional match.

The non-Foster impedance matching technique is not commonly used in broadband antenna matching due to the many challenges associated with realizing NICs at radio frequencies. For example,

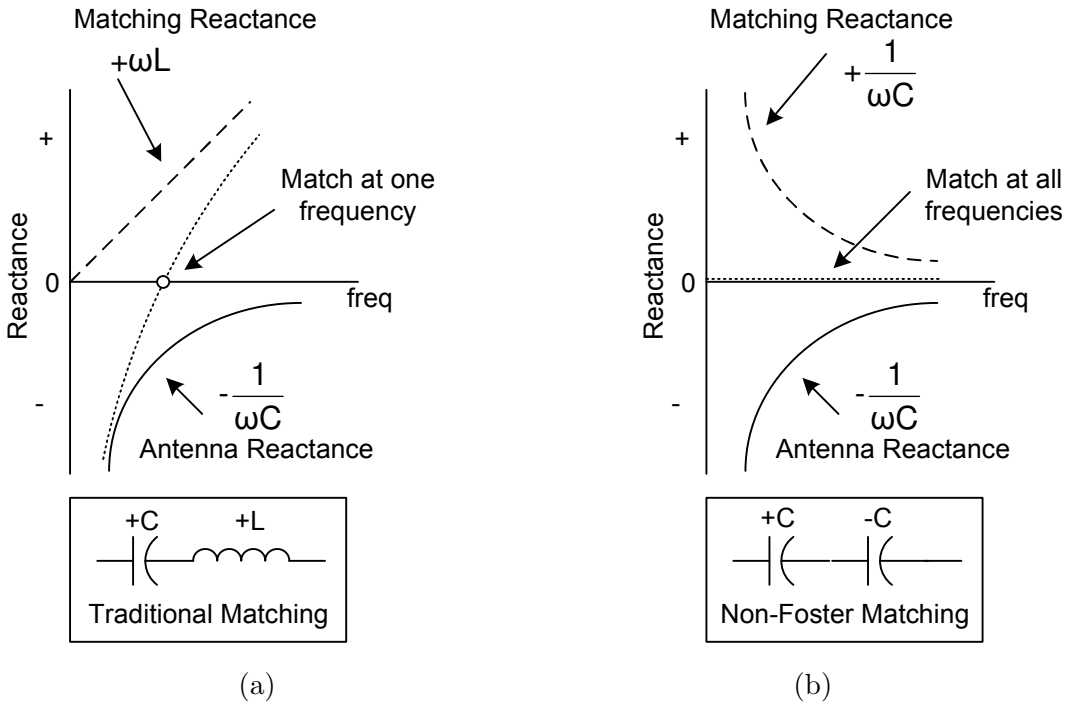


Figure 3.11: Matching a capacitive reactance (such as that of an electrically small monopole) using (a) traditional matching, (b) non-Foster matching (adapted from [66]).

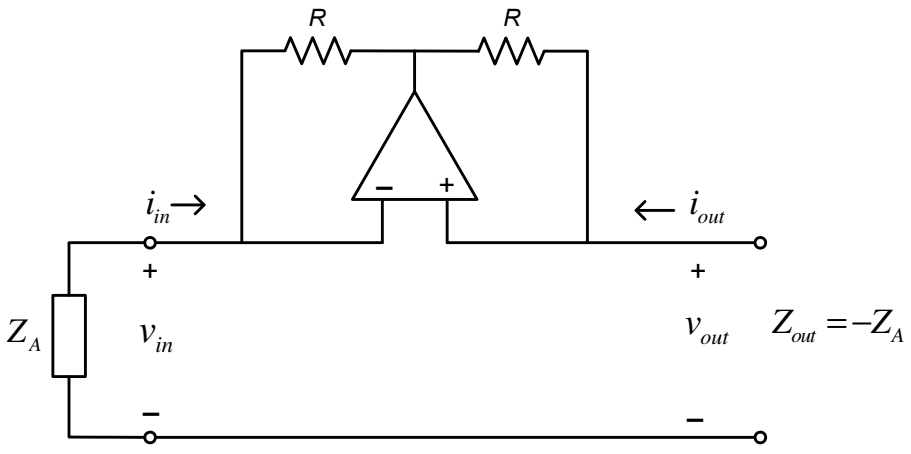


Figure 3.12: Basic NIC circuit using op-amp.

since a NIC depends on shifting the phase of an incoming signal by 180°, any parasitic phase difference between the signals will prevent a perfect negative impedance conversion. Also, load impedance significantly affects the operation (especially the stability) of the circuit [71]. Since it uses active circuitry with frequency–variable input impedance, it suffers from stability, linearity, and noise issues. In general, it is not mature enough to apply into MMR application. However, it might be an attractive future work to extend the research presented here.

3.6 Summary

Wideband matching of an antenna to a receiver is very difficult in MMR due to the fundamental limitations of the Bode–Fano bound and Foster's Reactance Theorem. In this chapter, several matching techniques as well as their limitations have been discussed using examples in which a VHF monopole antenna (1.97 m long and 21 mm diameter) is matched to a 50Ω load over the frequency range 10–28 MHz. A matching circuit (consisting of four passive components), which is designed using a classical method achieved 5 MHz bandwidth at the TPG calculated from Bode–Fano limit (–10.4 dB). Although the matching bandwidth can be increased using more components in the matching circuit, the design becomes intractable with the increase of components using classical methods. A higher order match can be achieved using RFT, an iterative technique which does not require the antenna impedance in circuit form. RFT provides 14.4 MHz bandwidth at -10.4 dB TPG to match the above antenna. However, the implementation of RFT is complex and depends heavily on optimization, which might not converge and is nevertheless still bound by fundamental limits. Antenna tuning is limited to providing a match for only one narrow band at a time. Non–Foster matching is another alternative, but suffers from stability, linearity, and noise issues. In summary, none of these approaches is entirely satisfactory for the purposes of MMR as laid out in Chapter 1. In the next chapter, we will consider an alternative approach which bypasses fundamental limitations of antenna matching in a different way.

Chapter 4

Sensitivity-Constrained Front-End Design

Wideband matching is fundamentally limited by the Bode–Fano limit and Foster's reactance theorem presented in the previous chapter. Hence antenna–receiver integration is very difficult, especially for a receiver covering a large range of frequencies. However, if a receiver is already external noise–dominated then further improvement of antenna–receiver matching does not necessarily improve the overall sensitivity. Presently there is no simple standard way to take this into account when specifying matching and noise figure requirements of receivers, especially with large, multiband tuning ranges.

This chapter describes the effect of external noise on matching and sensitivity. This chapter is organized as follows. Section 4.1 ("Noise Characterization") describes the various external sources of noise and Section 4.2 ("Optimum Noise Figure Specification") describes an "optimum noise figure" specification for multiband receivers based on the findings. Section 4.3 ("Implications for Design of Antenna Matching") describes some antenna matching implications due to external noise. In Section 4.4 ("Experimental Verification"), a field experiment is performed to verify the theoretical developments of the previous sections. Finally, Section 4.5 ("Summary") summarizes this chapter.

4.1 Noise Characterization

The sensitivity of a receiver is related to signal to noise ratio, which in turn depends on noise. In order to build a sensitivity-constrained front-end we need to account for the effect of noise in our front-end design. Section 4.1.1 ("Sources of Noise") describes common noise sources and Section 4.1.2 ("Noise Modeling") presents noise modeling. Finally, Section 4.1.3 ("Characterization of Environmental Noise") discusses how these noise sources can be characterized to obtain the parameters to be used in the noise model.

4.1.1 Sources of Noise

Primarily two kinds of noise sources are present in any RF front end: Internal noise, which is generated by electrical components internal to the system; and external noise, which comes from the environment. This section briefly discusses these two noise sources.

An important source of internal noise is Johnson noise (also known as "thermal noise"), which is associated with ohmic losses in an antenna or in electronic components of a radio system. This is generated by the thermal agitation of the electrons inside electrical circuits. Shot noise and flicker noise are also examples of internal noise.

External noise sources may be classified as (1) natural, such as noise from the atmosphere, from the Sun and the planets, Galactic noise generated by astrophysical processes [72], noise due to the radiation of cosmic microwave background (CMB), and thermal noise from the Earth itself; and (2) anthropogenic, i.e., from industrial and other man–made activities. The external noise delivered to a receiver includes natural noise plus additional noise resulting from human activity. These contributions have been measured and characterized in considerable detail, and are conveniently described in a report by the International Telecommunication Union (ITU) [73]. Figure 4.1 shows the power spectral density (PSD) of various external noise environments calculated using the models provided in [73]. Noise due to the CMB contributes about 2.7 K to the antenna temperature. On the other hand, among the terrestrial noise sources, the ground generally radiates a noise temperature of roughly equal to ambient temperature (about 290 K), part of which is received by the antenna. Atmospheric noise is caused by natural atmospheric processes, primarily due to lightning discharges

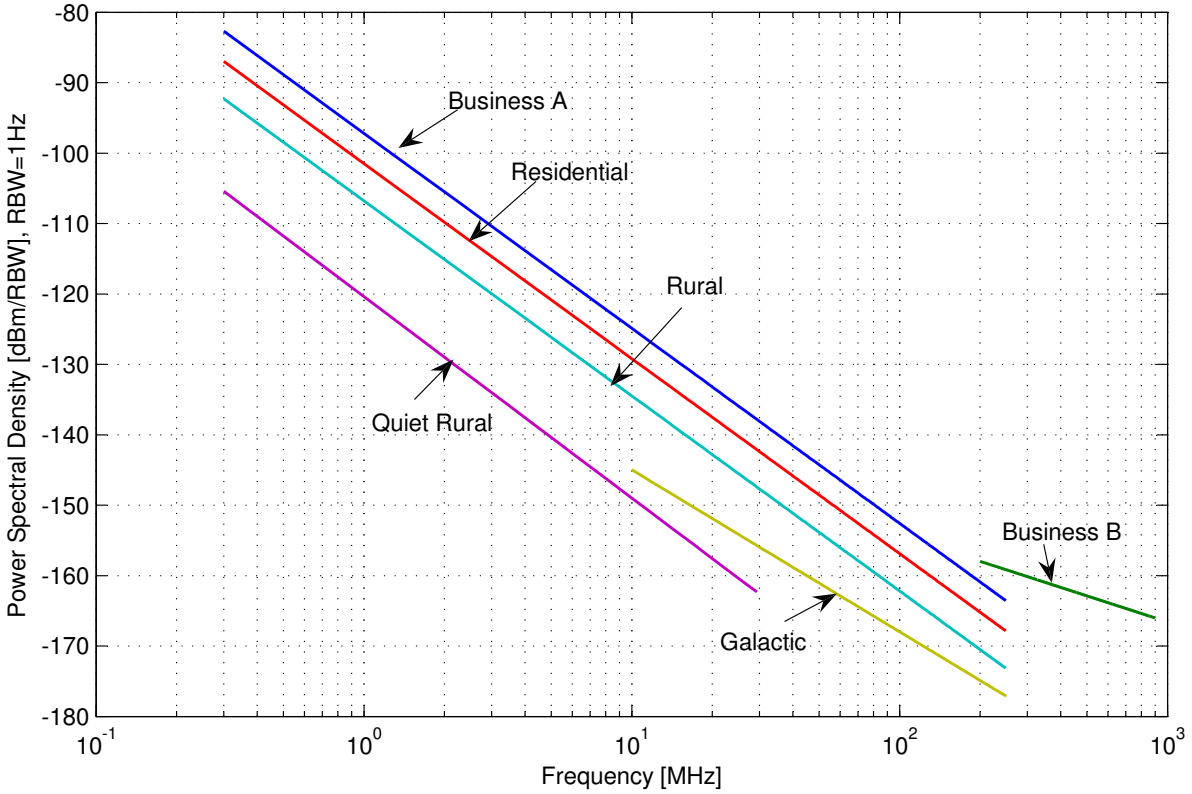


Figure 4.1: PSD of various noise environments calculated using the data provided in [73].

in thunderstorms. Depending on location man–made noise is categorized as "Business A", "Business B", "Residential", "Rural", and "Quiet rural" in [73]. The characterization of these noise sources will be addressed in greater detail in Section 4.1.3.

4.1.2 Noise Modeling

Johnson noise generated in a resistor can be modeled as a voltage source, representing the noise of the non-ideal resistor, in series with an ideal noise–free resistor. The root mean square (RMS) magnitude of the noise voltage due to Johnson noise is given by

$$\tilde{v}_n = \sqrt{4kT\Delta f R} \tag{4.1}$$

where k is Boltzmann's constant (1.38×10^{-23} J/K), T is the physical temperature of resistor, Δf is bandwidth, and R is the resistance of the ideal resistor. The voltage induced at the terminals of

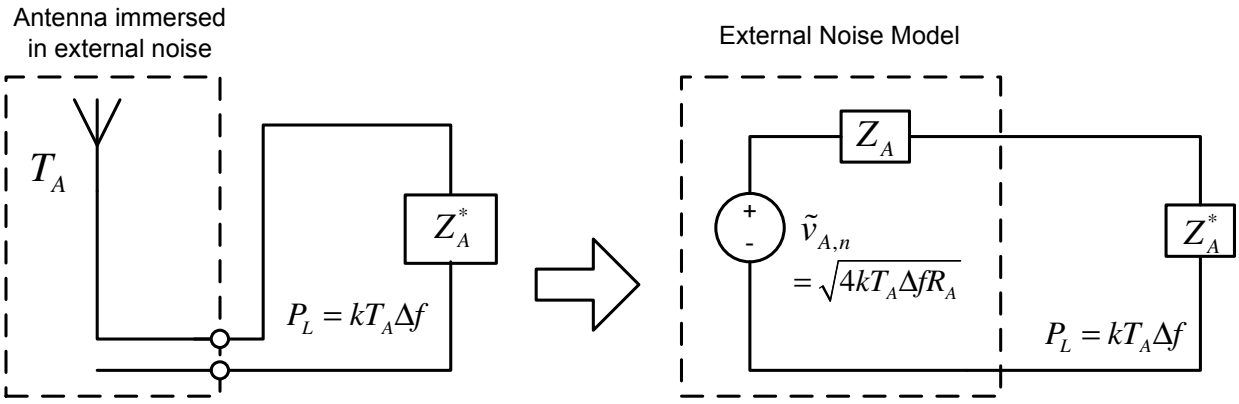


Figure 4.2: Modeling external noise of an antenna immersed in external noise temperature T_A.

an antenna by external noise can be modeled in the same manner as internal noise; i.e., as a voltage source in series with an impedance. Figure 4.2 shows the concept of modeling environmental noise delivered by an antenna immersed in external noise at noise temperature T_A. In the figure, $\tilde{v}_{A,n}$ and Z_A represent the noise voltage and antenna impedance respectively, P_L represents the power transfer assuming a perfectly matched load, and R_A is real part of the antenna impedance Z_A.

Since later sections of this chapter require knowledge of external noise, the next section describes this characterization of environmental noise sources in detail.

4.1.3 Characterization of Environmental Noise

The median noise figure values for any of the external noise models described in [73] is given by

$$F = c - d \log_{10} f \quad [\text{dB}] \tag{4.2}$$

where f is the frequency in MHz, and c and d are given in Table 4.1. Figure 4.3 shows the median noise figure of these environmental noise sources. It should be noted that the values of c and d provided in Table 4.1 is only valid in the frequency range of 0.3 to 250 MHz for all environmental noise sources with some exceptions, such as the "Quiet Rural" model is valid from 0.3 to 30 MHz, the Galactic background model is valid from 10 to 250 MHz, and the "Business B" model is valid from 200 to 900 MHz.

Table 4.1: Median values for noise model parameters [73].

Environment Category	c	d
Business A	76.8	27.7
Business B	44.3	12.3
Residential	72.5	27.7
Rural	67.2	27.7
Quiet Rural	53.6	28.6
Galactic Noise	52.0	23.0

In our research we are interested to know how much PSD is contributed by external noise to the input of a RF front end, to determine whether the front–end is external noise dominated or not. It is convenient to use noise temperature for the calculation of PSD instead of noise figure. Hence we would like to transform this characterization to a more convenient form expressed in noise temperature. From Equation 4.2 we see that external noise can be accurately described in terms of a mean noise temperature T_A following the power law af^{-b}. This also can be expressed in terms of Gaussian statistics with a variance σ^2 with respect to location within a given noise environment. Table 4.2 presents a modified version Table 4.1, including the values of a and b. In Table 4.2, 'Celestial' refers to the combination of Galactic noise and the CMB. In [73], 'Business A" is used in 0.3 to 250 MHz and 'Business B" is used in 200 to 900 MHz. In the new characterization, these are merged into a single model which is similar to 'Business A" below 130 MHz and similar to 'Business B" below 900 MHz. This modification is done simply extending the "Business B" curve below 200 MHz to find the intercept point with "Business A". Figure 4.4 shows the new median noise figures using Table 4.2.

The statistical variation of mean noise power with respect to location is expressed in terms of "decile variations", D_u and D_l, the upper and lower decile values (i.e., the values exceeded 10 percent and 90 percent of the time) of the variability of noise power. The decile values are not only dependent on frequency, but also upon the actual location in various noise sources environment. Assuming that the noise distribution is symmetric about the mean, D_u is approximately equal to D_l. The values of D_u and D_l are provided in [73]. We can find the standard deviation σ, i.e., the square root of variance with respect to location, of noise from the given decile values. The area under the

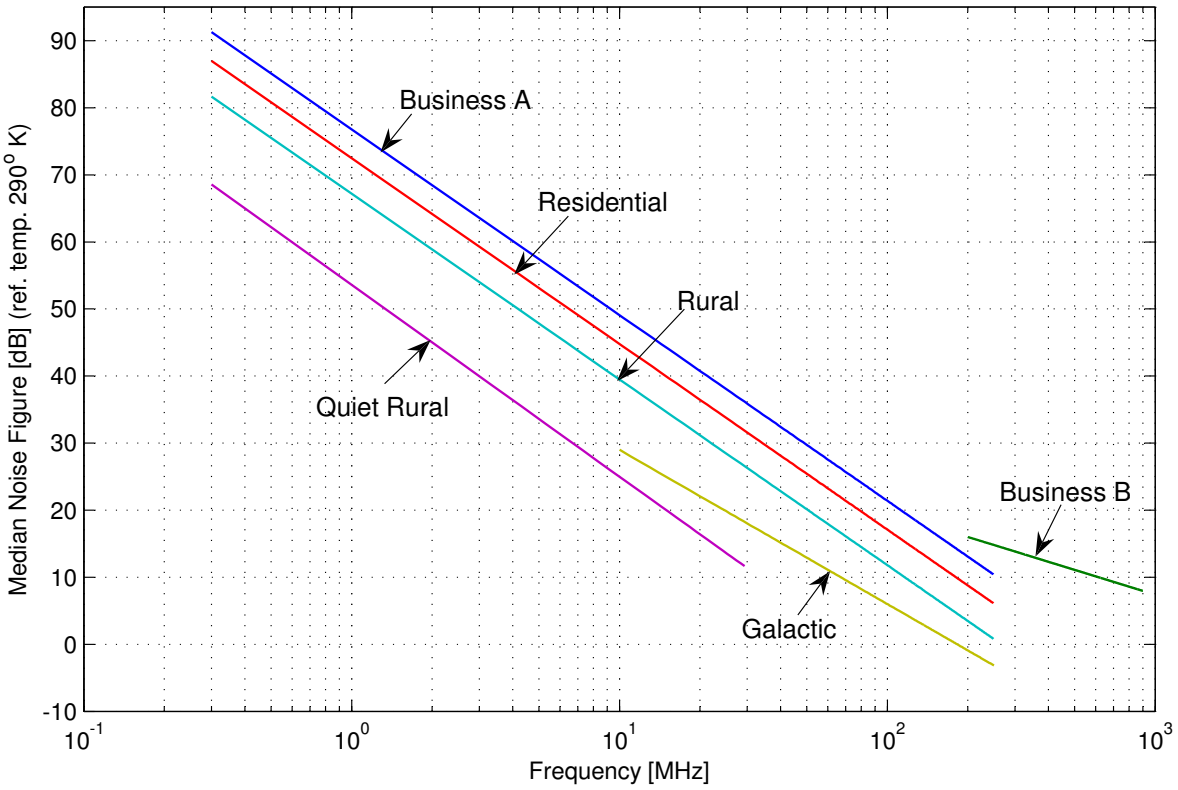


Figure 4.3: Median noise figures for various external noise sources using the model provided in [73].

Table 4.2: Parameters for mean noise temperature $T_A = af^{-b}$ [K].

Frequency (MHz)		**Quiet Rural**	**Rural**	**Residential**	**Business A/B**	**Celestial**[1]
3–30	a	9.53×10^{24}	6.33×10^{25}	2.14×10^{26}	5.75×10^{26}	1.07×10^{23}
	b	2.86	2.77	2.77	2.77	2.52
30–100	a	–	6.33×10^{25}	2.14×10^{26}	5.75×10^{26}	1.07×10^{23}
	b	–	2.77	2.77	2.77	2.52
100–130	a	–	6.33×10^{25}	2.14×10^{26}	5.75×10^{26}	1.07×10^{23}
	b	–	2.77	2.77	2.77	2.52
130–250	a	–	6.33×10^{25}	2.14×10^{26}	1.87×10^{14}	1.07×10^{23}
	b	–	2.77	2.77	1.23	2.52
250–900	a	–	–	–	1.87×10^{14}	1.07×10^{23}
	b	–	–	–	1.23	2.52
900–3000	a	–	–	–	–	1.07×10^{23}
	b	–	–	–	–	2.52
σ		5.3 dB[2]	5.3 dB	4.5 dB	6.6 dB[3]	–[4]

[1] Add 2.7 K to account for CMB
[2] Decile values not available from [73], using $D_l = D_u = 6.8$ dB as for "Rural".
[3] Decile values not available from [73], using $D_l = D_u = 8.4$ dB as for "Business B".
[4] Varies over about 2 dB depending on time of day; see [74].

Gaussian probability distribution function between $-n\sigma$ and $+n\sigma$ is

$$erf\left(\frac{n}{\sqrt{2}}\right) = \text{Area} \tag{4.3}$$

where erf is the error function. We find that 80% of the samples are within 1.28σ of the mean. Therefore, the value of σ can be calculated from this relation, and has been summarized also in Table 4.2.

To illustrate the use of Table 4.2, suppose a radio is to be designed to operate at 60 MHz at a location that could be considered "Residential" in the ITU sense. According to Table 4.2, the external noise temperature for 60 MHz in a residential area is $73,303$K. This calculation is valid for 95% of locations in the "Residential" noise source environment (i.e. the value of confidence factor n is 2). Note that the Celestial noise contributes approximately 3000K to the total external noise in this case.

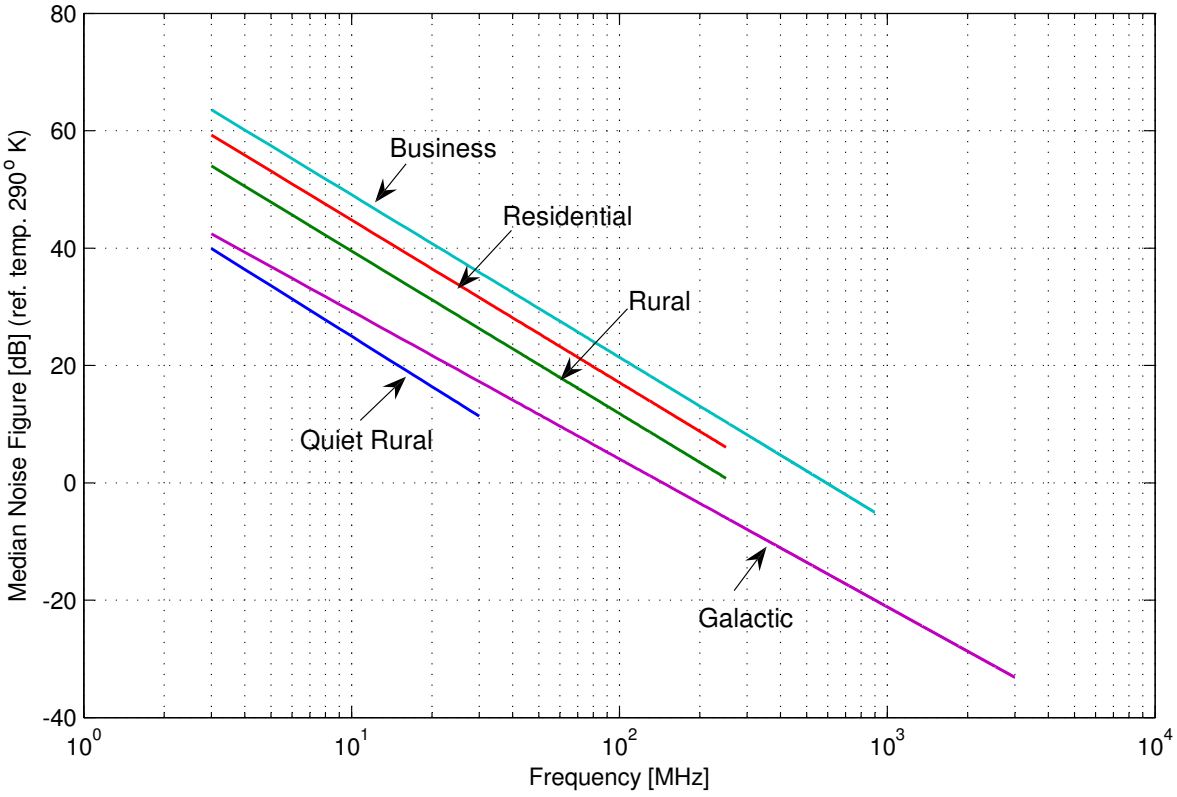


Figure 4.4: Median noise figures for various external noise sources using the model presented in Table 4.2.

4.2 Optimum Noise Figure Specification

This section presents and demonstrates a specification and a methodology to find out the "optimum" noise figure for a receiver. This is not a traditional optimum point. A receiver's sensitivity depends on the total noise of the receiver, which includes the noise generated internally and the noise received from the environment. Usually sensitivity increases with the improvement of the internal noise figure of a receiver. However, when a receiver is external noise–dominated, then after a certain threshold further improvement of the receiver's internal noise figure does not necessarily improve the sensitivity significantly. Rather, it complicates the circuit design, and thus increases the total design cost. This subjective point at which further improvements in noise figure do not significantly improve sensitivity, but only increases complexity, is what we refer to as the "optimum" point. This concept is particularly useful for receivers with large, multiband tuning ranges. The value in this specification is that it (1) prevents the designer from over–specifying the receiver noise figure and (2) can be exploited in our proposed work as a loosened constraint in the sense that we can tolerate a poor–quality match where we are safely external noise-dominated, or in other situations where the best possible noise figure is not required or desired.

Let us assume that an antenna is connected to a preamplifier, which can be described in terms of its input impedance Z_p, gain G_p, and noise temperature T_p. Now the PSD due to the external noise temperature T_A at the output of the preamplifier, referenced to the input of the preamplifier, is given by

$$S_{ext} = \eta k T_A \left[1 - |\Gamma|^2\right] G_p \tag{4.4}$$

where η is the antenna efficiency associated with the loss due to the finite conductivity of the materials used to make the antenna and absorption by the imperfect (nonperfectly-conducting) ground, and $\Gamma = (Z_p - Z_A^*)/(Z_p + Z_A^*)$. The preamplifier–generated noise at the output of the receiver can be expressed in terms of the preamplifier's input–referenced noise temperature T_p as

$$N_p = k T_p G_p \tag{4.5}$$

Now the total PSD at the output of receiver can be expressed as

$$\begin{aligned} S_{out} &= S_{ext} + N_p \\ &= (\eta T_A \left[1 - |\Gamma|^2\right] + T_p) k G_p \end{aligned} \tag{4.6}$$

The ratio γ of external noise to internally–generated noise at the input of the receiver is thus

$$\begin{aligned} \gamma &= \frac{S_{ext}}{N_p} \\ &= \eta \frac{T_A}{T_p} \left[1 - |\Gamma|^2\right] \end{aligned} \tag{4.7}$$

The optimal preamplifier temperature T_p is that which is sufficiently small to make S_{ext} dominant over N_p. This can be achieved by γ on the order of 10 or so. However, smaller γ – perhaps even $\gamma < 1$ – might be appropriate depending on the application and the need to trade off sensitivity for improved linearity or reduced cost. For example (and as shown in Figures 2.7 and 2.8), if we decrease T_p (i.e., improve sensitivity) then it reduces linearity. The corresponding noise factor is computed from noise temperature using

$$F_{opt} = \frac{T_{opt}}{T_0} + 1 \tag{4.8}$$

where

$$T_{opt} = \eta \frac{T_A}{\gamma} \left[1 - |\Gamma|^2\right] \tag{4.9}$$

is the optimal value of T_p, and T_0 is the reference noise temperature (290 K).

To illustrate the concept, an example is presented here for the frequency range of 3 MHz to 3 GHz. For receiver noise figure specification purposes, one should choose the applicable category of man-made noise, determine the associated noise temperature, and subtract from this some margin n representing the confidence with which the designer wishes to be sure this value is not exceeded. n is conveniently described in units σ. Figure 4.5 shows the optimum noise figure $10 \log_{10}(F_{opt})$ for $\gamma = 10$ and $n = 2\sigma$ in various environments assuming $\eta \left[1 - |\Gamma|^2\right] = 1$ (i.e., perfectly matched antenna with no ground loss). The specification shown in Figure 4.5 is the linear sum of celestial noise plus that of the most relevant man-made noise category, reduced by the specified margin.

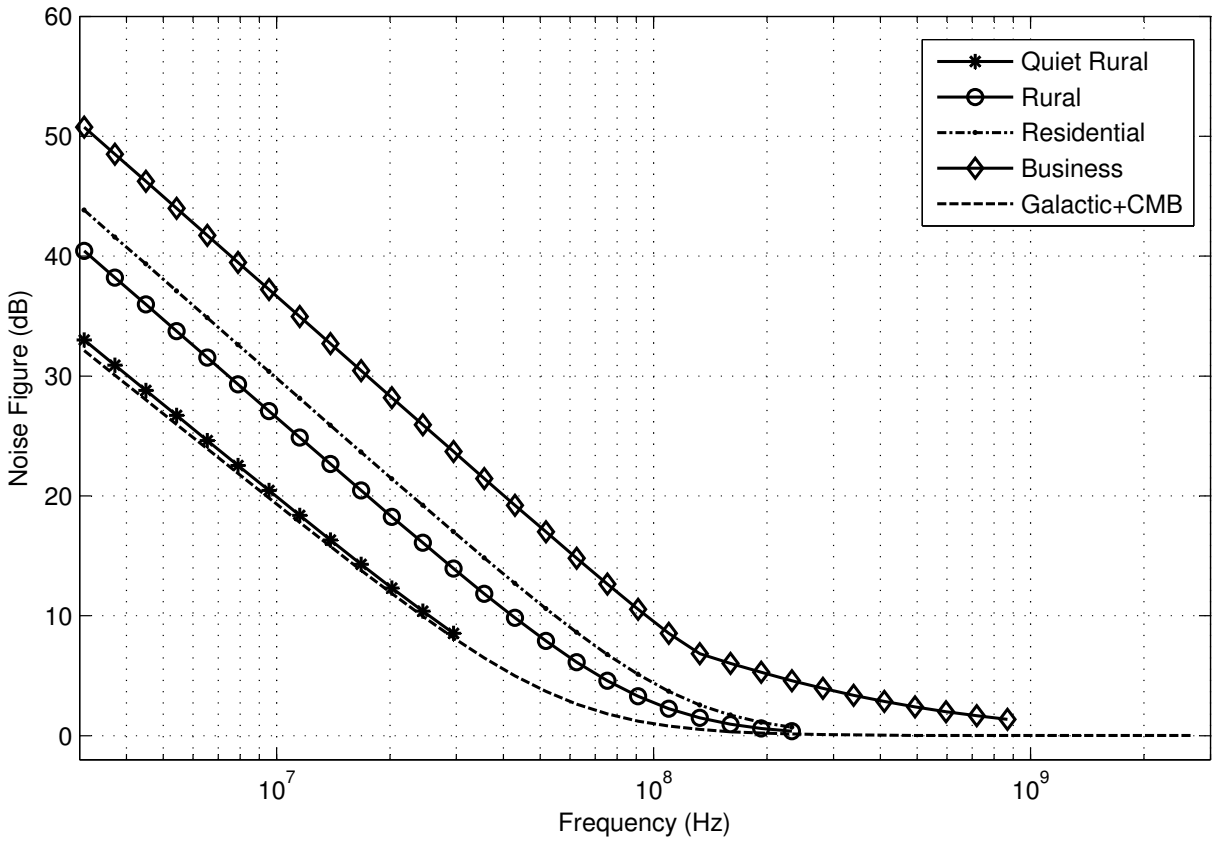


Figure 4.5: Example of the optimum noise figure specification. Lines with markers show the maximum noise figure for which the sensitivity of a receiver is limited by the noise generated by its own front end (by a factor of 10 over external noise) in 95% of locations that can be classified as the indicated type. The irreducible mean contribution from the combination of Galactic background noise and the CMB is also shown.

For example, if a receiver is required to operate at 200 MHz in a "Business" environment, then according to the specification the noise figure should be 6 dB in order to ensure sensitivity is dominated by external noise by a factor of 10 over 95% of locations.

It should be noted that the specification described here does not take into account individual sources of radio frequency interference and impulsive noise; these are separate considerations. Also, the values in Table 4.2 are based on the measurements reported in [73], which may not be universally valid or representative of new sources of man-made noise. However, we can easily modify this table employing some corrective measures such as increasing n, or making site-specific measurements and extracting from them applicable values of a and b. It can also be modified using noise measurements

reported by others. Some examples follow. Rogers *et. al.* presented external noise measurements from 70 to 1500 MHz in suburban and rural environments of Northeast [75]. In [76], Wagstaff and Merricks presented measurements of man–made noise from 100 MHz to 3 GHz with bandwidths up to 10 MHz. Gorka *et. al.* presented some man–made noise measurements for the medium wave band based on measurements performed in Spain and Mexico [77]. Note that the measurements reported in [73] also do not contain any information about indoor noise sources. It is also possible to change/modify our noise specification incorporating indoor noise sources if it is known.

4.3 Implications for Design of Antenna Matching[5]

In the previous section we demonstrated that the optimum noise figure for a receiver is not necessarily the minimum possible noise figure. Thus, the best possible match between antenna and receiver is not necessarily the one which maximizes TPG. We now wish to know how good the match must be to get reasonable noise figure. As we know from the previous section, if an RF front–end is strongly dominated by external noise; then any additional improvement in match would not significantly improve sensitivity.

Figure 4.6 shows the contributions to the PSD at the preamplifier output for a lossless antenna ($\eta = 1$) for several fixed values of ρ, assuming preamplifier gain $G_p = +22$ dB and noise temperature 288.6 K (i.e., noise figure $F = 3.0$ dB). The $\rho = 1$ curve corresponds to a perfectly–matched condition for all frequencies (for illustration purposes only, perfect matching at all frequencies is not practically feasible) and impedance mismatching increases with the increasing values of ρ. This plot provided some insight for understanding how good matching must be at any given frequency to obtain Galactic noise–limited operation. Note that below 100 MHz, a preamplifier with a very modest noise figure (i.e., noise temperature on the order of a few hundred degrees Kelvin) can be sufficient to obtain a very large γ even if the antenna is badly matched. Note also that the highest Galactic noise–limited frequency is determined by the noise figure of the preamplifier. For example, Figure 4.6 illustrates that even for $\rho = 10$ the front–end is externally noise dominated up to about 80 MHz for a preamplifier with 3 dB noise figure.

[5] This is an extension of an analysis originally presented in [78].

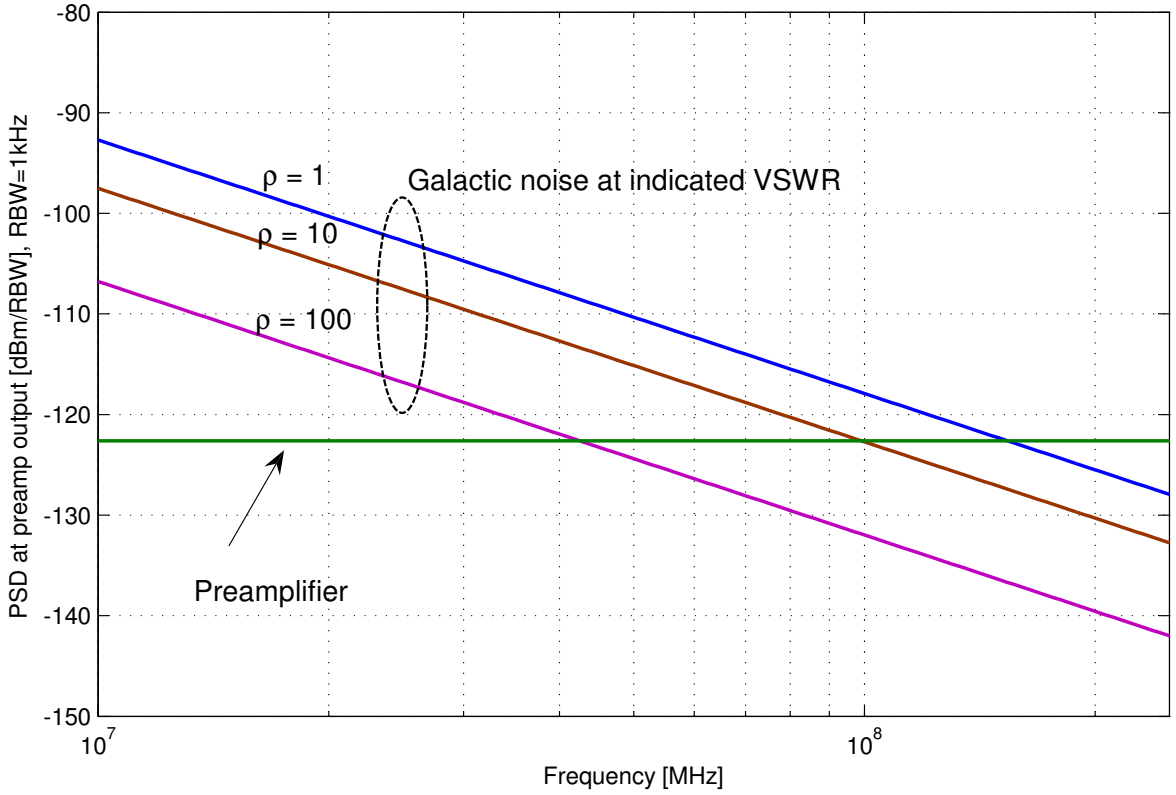


Figure 4.6: Contributions to the PSD at the preamplifier output for a lossless antenna ($\eta = 1$) by Galactic noise. In this plot, preamplifier gain and noise figure are chosen to be $G_p = +22$ dB and $F = 3.0$ dB, respectively.

Since Galactic noise is unavoidable, it is the worst case scenario for receiver design. As shown in Figure 4.4, radios are often used in areas where the noise PSD is much greater than the PSD of Galactic noise. Figure 4.7 repeats Figure 4.6, but now assuming "Residential" noise. As we can see the frequency range over which internal noise is dominated by external noise is greatly increased. This frequency range of noise–limited operation is further increased for even noisier environments, such as "Business".

In summary, a receiver can be external noise–dominated even for a large mismatch between the antenna and preamplifier, depending on noise environment and frequency. An important caveat is that the parameters of a preamplifier (Z_p, G_p, and T_p) exhibit some frequency dependence; however, this variation is typically insignificant compared to the effect of the frequency dependence of Z_A. This will be demonstrated in Section 4.4. Also, T_p can be sensitive to the impedance match at the preamplifier input, however this effect is technology-dependent and is difficult to model in a generic way. In this section, it is assumed that this variation is insignificant compared to other effects (and is also confirmed in Section 4.4), and this issue can be considered for future study. As we pointed out in Chapter 2, our intention is to employ a multiplexer to match an antenna with a preamplifier.

4.4 Experimental Verification

In this section, we verify the theory developed in the previous sections by performing an experiment in field conditions. This experiment considers a VHF monopole antenna in a situation which is limited only by Galactic noise and some radio frequency interference (RFI). This experiment will also serve as a starting point for additional experiments pertaining to multiplexer development in Chapter 5. This section is organized as follows. Section 4.4.1 ("Experiment Design") and Section 4.4.2 ("Antenna Design") describe the design of the experiment and the VHF monopole antenna, respectively. Section 4.4.3 ("Data Collection") describes the process of data collection and discusses how some problems encountered during the measurement were mitigated. Finally, results are presented in Section 4.4.4 ("Results").

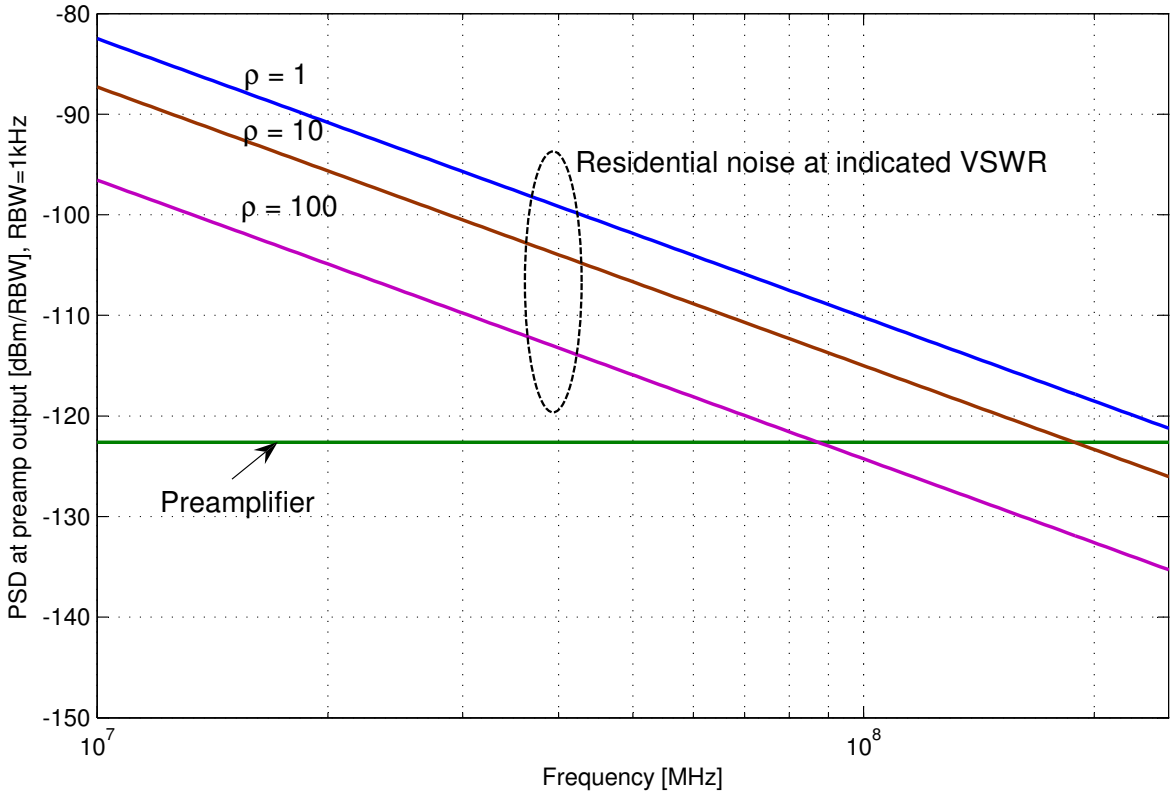


Figure 4.7: Same as Figure 4.6, but now assuming "Residential" noise.

4.4.1 Experiment Design

The goal of this experiment is to verify the theory of Section 4.2; specifically Equation 4.4. At the same time, we are developing and validating instrumentation needed for the measurement of the performance of multiplexers described in later chapters. Since the PSD of Galactic noise is accurately known, easily accessed, and confirmed through some previous measurements [72, 74], it is chosen as the noise environment for this experiment. This is in contrast to man–made external noises which varies dramatically depending on location, and also as a function of the daily cycle of human activity. However, the PSD of Galactic noise is very weak, and thus this experiment is best done at frequencies where it is strongest. Thus the frequency range in which we make the measurements is 10–80 MHz. Another motivation is that if our front end is Galactic noise–limited, then definitely it will be external noise–limited for all other environments.

Similar experiments have been reported in the past. For example, Ellingson, Simonetti, and Patterson [74] presented a dipole for a 29–47 MHz radio telescope array and demonstrated the performance by measuring Galactic noise. The main differences in the current study is the use of a monopole antenna instead of a dipole, and a somewhat larger fractional bandwidth of interest.

Figure 4.8 shows a block diagram of our experiment setup, which consists of three sections: antenna, receiver, and data acquisition. A simple VHF monopole antenna, the description of which is presented in detail in Section 4.4.2, was developed for this experiment. A spectrum analyzer is used as a data acquisition tool to measure the PSD at the output of the receiver, the main task of which is to amplify the received noise with sufficiently low noise figure so that it can dominate the internal noise of spectrum analyzer. The receiver also performs some filtering to reduce the level of intermodulation due to radio frequency interference (RFI) signals outside the frequency range of interest. The PSD measured at the input of the spectrum analyzer can be calibrated to the antenna terminals by removing the gain transfer function of the receiver from accounting for IME. The PSD at the antenna terminals can also be calculated independently, from theoretical considerations. If the difference between these two PSDs are sufficiently small then we can confidently say that the measurement results confirm the theory in the previous sections.

Figures 4.9 and 4.10 show various parts of the receiver. Table 4.3 shows a summary of gain, noise

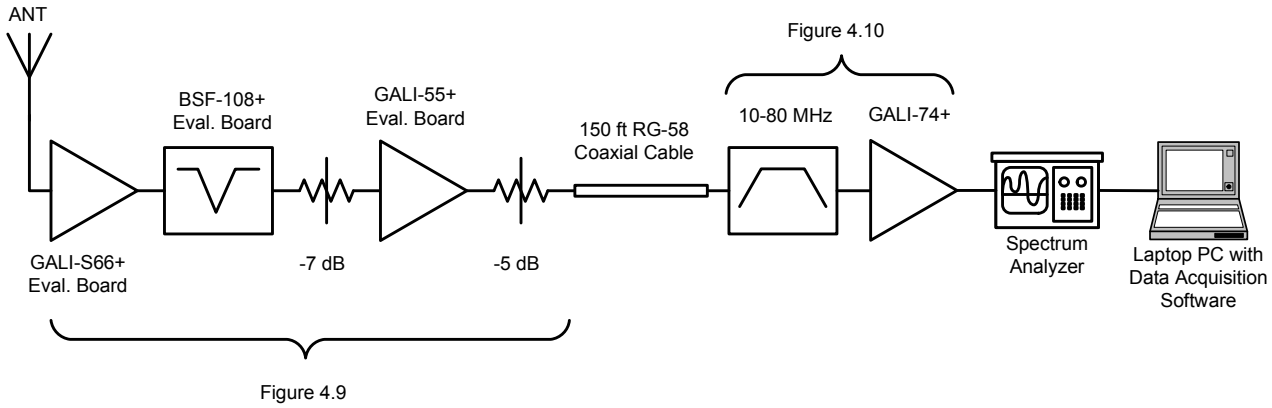


Figure 4.8: Block diagram of the field experiment setup.

figure, and third order intercept (GNI) analysis. The first component, which is an evaluation board for the GALI-S66+ amplifier from Minicircuits[6], is selected to have sufficiently low noise figure (2.7 dB). This amplifier board is connected to a 88-108 MHz bandstop filter (BSF-108+ from Minicircuits) to reduce the total amount of out–of–band RFI power input by blocking high power broadcast FM radio stations. Attenuators were used between the amplifier stages to optimize the trade–off between sensitivity and linearity. A long cable (approximately 150 ft) was used to separate the antenna from the data acquisition system, in order to avoid interference from the spectrum analyzer and PC. This cable introduces $1-9$ dB loss over the frequency range $10-80$ MHz (increasing with increasing frequency). The analog receiver section shown in Figure 4.10 is borrowed from the Eight-meter-wavelength Transient Array (ETA) [79, 80]. However, only part of the receiver is used (a single GALI-74+ amplifier and a bandpass filter modified for $10-80$ MHz). Finally, the output of this receiver is connected to a spectrum analyzer, Model FSH3 from Rhode & Schwarz. The spectrum analyzer is connected to a laptop PC with data acquisition software, which is developed in LabWindows[7].

The design requirements for this experiment are: (1) The gain of the receiver should be sufficiently high for external noise to dominate over the spectrum analyzer's internal noise, (2) The noise figure of the receiver should be sufficiently low, and (3) the 1 dB compression point (P1) of the receiver should be high enough to make intermodulation due to RFI negligible. The total gain, IIP3, and

[6] http://www.minicircuits.com
[7] http://www.ni.com/lwcvi/

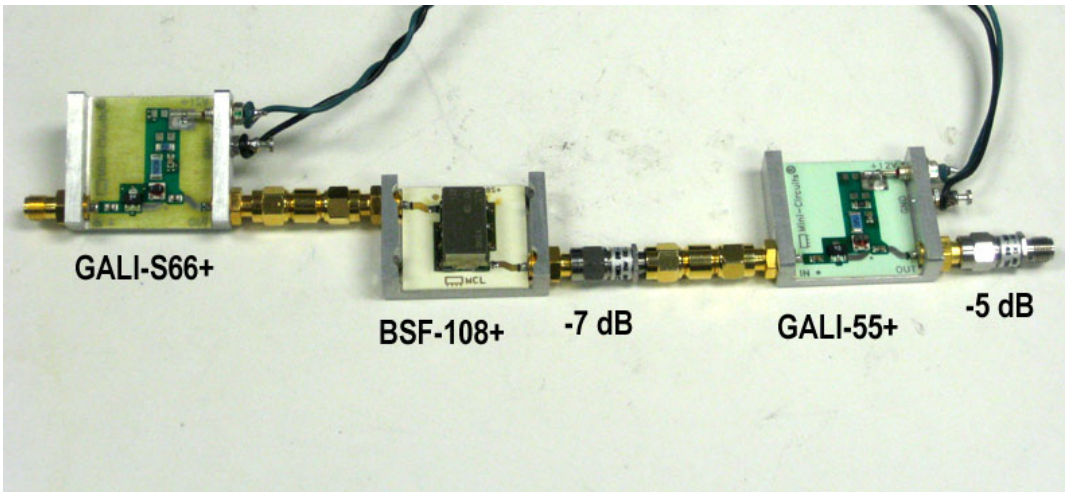


Figure 4.9: Image of the components used in the receiver (the part which is close to antenna) during the field experiment.

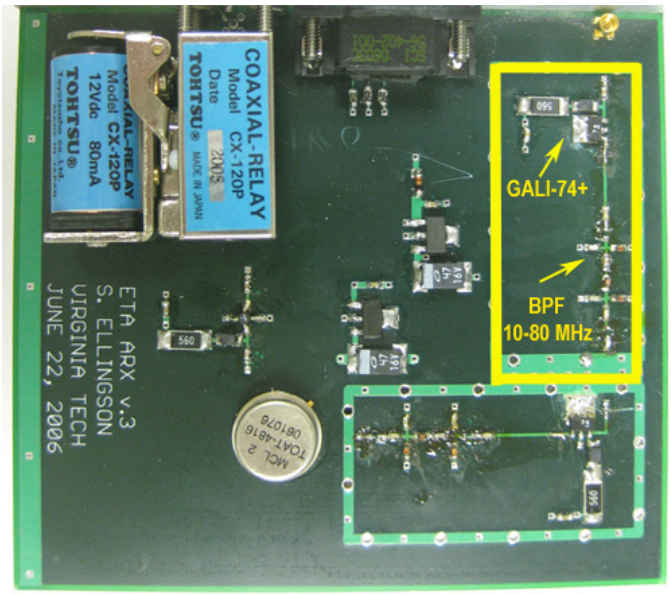


Figure 4.10: The components used in the receiver (the part which is close to data acquisition) of the field experiment.

Table 4.3: GNI stage–cascade analysis of the measurement system used for field experiment (calculated for 80 MHz).

		Stage			Cascade		
Stage	**Component**	**Gain (dB)**	**F (dB)**	**IIP3 (dBm)**	**Gain (dB)**	**F (dB)**	**IIP3 (dBm)**
1	GALI-66	22.0	2.7	−4.0	22.0	2.7	−4.0
2	Notch Filter	−1.5	1.5	200.0	20.5	2.7	−4.0
3	Attenuator	−7.0	7.0	200.0	13.5	2.7	−4.0
4	GALI-55	21.9	3.3	6.6	35.4	2.9	−8.7
5	Attenuator	−5.0	5.0	200.0	30.4	2.9	−8.7
6	cable	−9.0	9.0	200.0	21.4	2.9	−8.7
7	BPF	−1.5	1.5	200.0	19.9	2.9	−8.7
8	GALI-74	24.0	2.7	14.0	43.9	2.9	−11.6

noise figure of the complete measurement system can be determined from the stage values of G, IIP3, and F using a GNI analysis, as described in Appendix B. Table 4.3 summarizes the results of the GNI analysis of the measurement system. The calculated gain and the noise figure of the receiver is 44.9 dB and 2.9 dB, respectively. The IIP3 and the P1 of our system is approximately −11.6 dBm and −21.2 dBm (from Equation 2.23), respectively. The gain is sufficiently high to dominate over the spectrum analyzer's internal noise, which is −95 dBm/kHz. The total RFI power expected at the antenna terminals is −54 dBm (determined from the measurement), which is approximately 32 dB below the P1 of our system; thus linearity is sufficiently high to prevent significant compression or intermodulation. As a result, we can conclude that this receiver fulfills the design requirements and is suitable for our experiment. The transfer function of the entire receiver from the antenna terminals to the input of the spectrum analyzer was measured, and is shown in Figure 4.11.

4.4.2 Antenna Design

A VHF monopole antenna is used in this experiment, because monopole antennas are simple to design, and easy to analyze and build. A monopole antenna is also single–ended and therefore does not require a balun. Also relevant is the fact that antennas used in mobile and portable radios are more similar to monopoles than to dipoles.

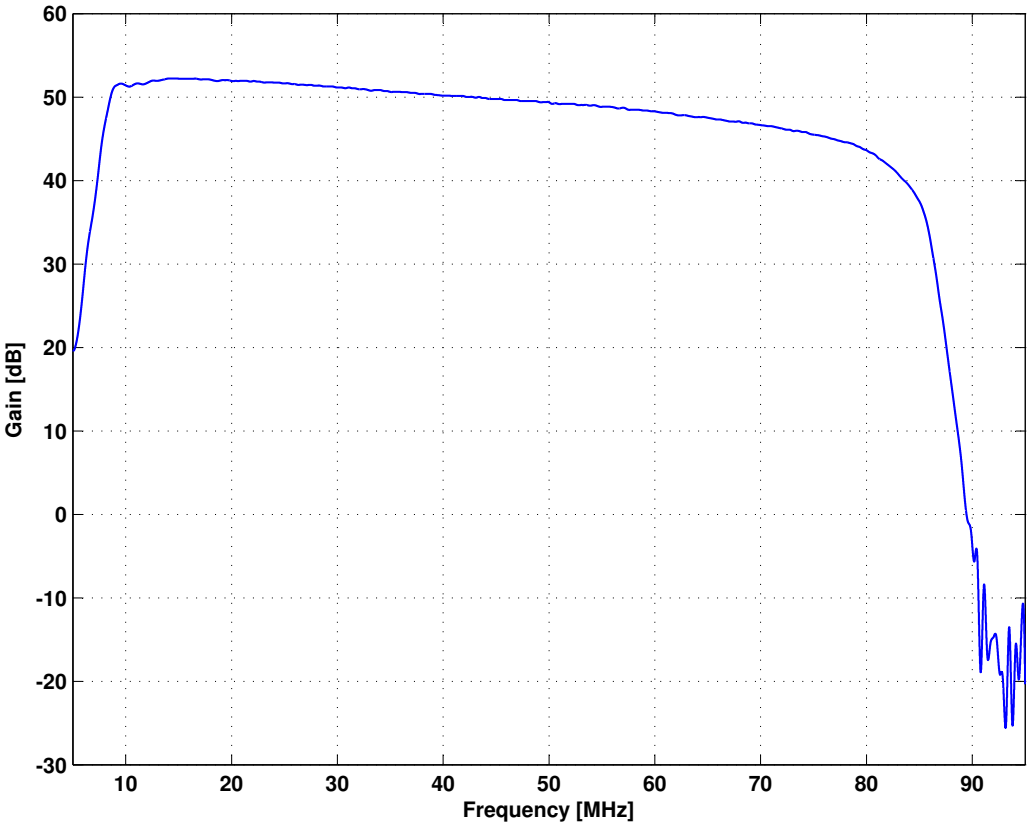


Figure 4.11: Transfer function of the receiver used in the field experiment.

The monopole antenna, shown in Figure 4.12, results from applying image theory to a half-wave dipole. According to this theory, if a conducting plane is placed below a single element of length $L/2$ carrying a current, then the combination of the element and its image acts identically to a dipole of length L except that the radiation occurs only in the space above the plane. We used a copper pipe 1.97 m long and 21 mm in diameter as our VHF monopole antenna.

Since the Earth is not a perfect ground, a ground screen is used above the Earth ground. Figure 4.13 shows the dimensions of the ground screen. It should be noted that the particular size and shape of the ground screen was determined solely by the materials on hand, and is in no sense optimized. Reflectix brand foil insulation[8], which consists of two layers of aluminum foil with plastic bubble laminated between the foil layers (mostly used for thermal insulation) is used as for the ground screen for this experiment. The antenna is connected to the input of the receiver using a custom-made "pig-tail" coaxial cable shown in Figure 4.14(a). To make the antenna stand upright during the measurement, a wood dowel was inserted into the copper pipe and also driven into the ground, as shown in Figure 4.14.

Commercial software FEKO[9], which simulates an antenna using the Method of Moments (MoM), is used to model this antenna as copper wire of circular cross section. In our simulation, the ground screen is included above the the Earth ground, which is assumed to have conductivity $\sigma = 5 \times 10^{-3}$ S/m and relative permittivity $\epsilon_r = 13$. Figure 4.15 shows the resulting simulated antenna impedance as well as the measured values. Simulated results indicate that this antenna is resonant at around 36 MHz and the radiation resistance at the resonant frequency is 33.4Ω. The measurement is in close agreement, indicating resonance at 34.6 MHz. However, it is noticeable from Figure 4.15 that there are some discrepancies between the measured and simulated antenna impedance. Since during the antenna impedance measurement we could not use any filter or other components to block strong RFI that exists below 20 MHz (see Figure 4.18), we suspect that below 20 MHz this may cause measurement error. The reason behind the discrepancy above 40 MHz is not known. However, the difference between the measured and simulated impedance in that range has little effect on IME. This is illustrated in Figure 4.16, which shows the calculated IME between the VHF monopole antenna and a preamplifier with $Z_p = 50\Omega$, using both the simulated

[8] Model#ST16025, http://www.reflectixinc.com
[9] http://www.feko.info

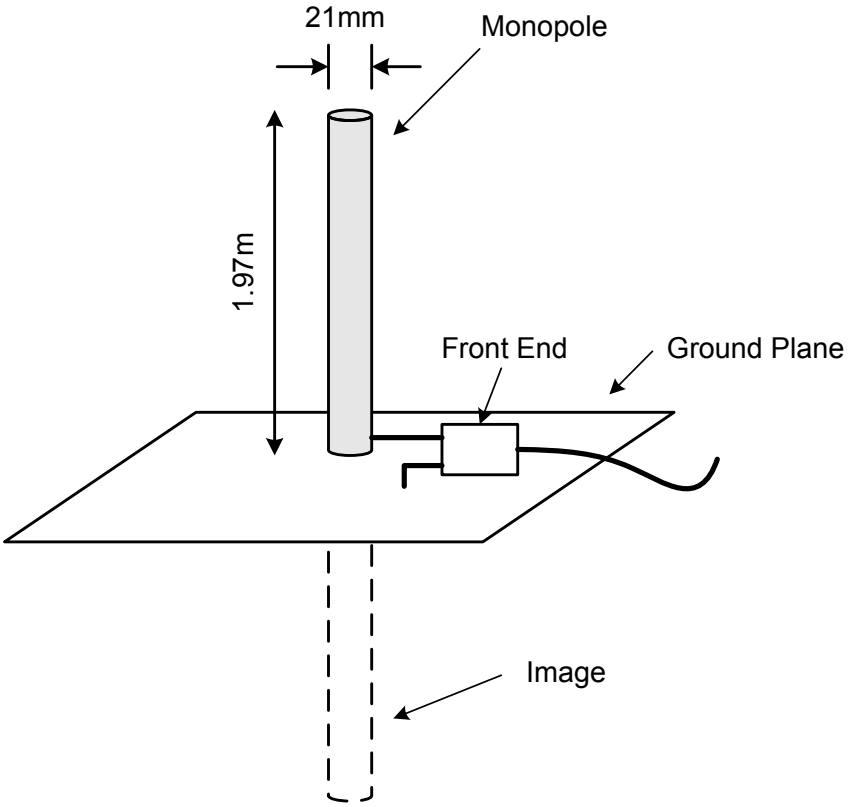


Figure 4.12: The dimensions of the monopole antenna used in the field experiment.

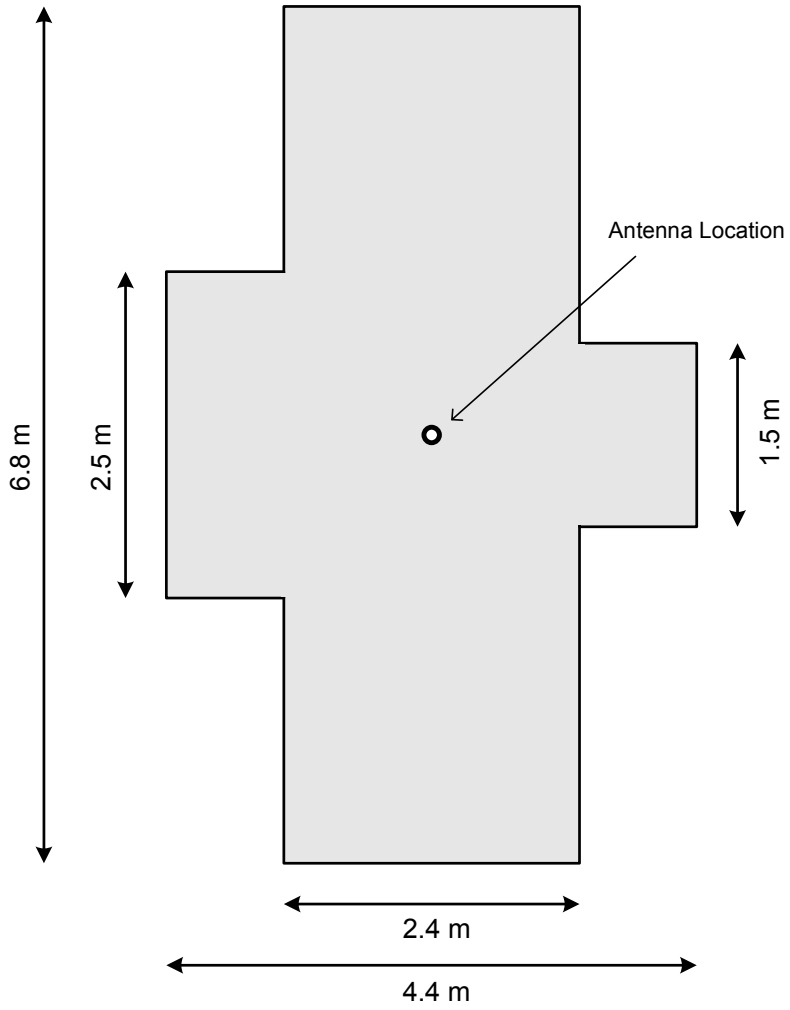
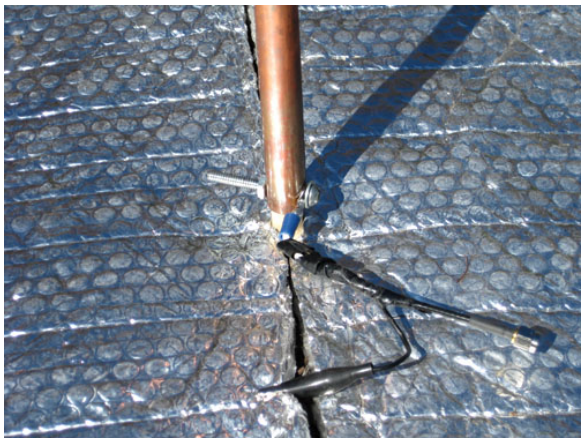


Figure 4.13: The dimensions of the ground screen used in the field measurement as well as in the simulation.



(a) Pig–tail cable connection

(b) Base of the monopole

Figure 4.14: Antenna construction details.

and measured antenna impedance. Since the agreement in IME above 35 MHz is very good, no further investigation was deemed necessary.

4.4.3 Data Collection

To ensure linear and unbiased measurement of the noise spectrum, the spectrum analyzer was configured to use "sample" mode detection, as opposed to the default "quasi–peak" detection mode. 1 kHz resolution bandwidth (RBW) was used.

Figure 4.17 shows the image of the experimental setup. This experiment was performed at Pandapass Pond, which is a recreation park maintained by US Forest Service and located approximately 5 miles from Blacksburg, VA. The measurement was performed from 11:00 am to 5:00 pm local time on November 29, 2008.

The PSD measured at the output of the receiver is shown in Figure 4.18. Strong RFI is noticeable in the frequency range 10-20 MHz and also around 88 MHz. However, the most prominent RFI present is the ATSC digital TV signal which is located around 60-66 MHz frequency range. Nevertheless, the data is suitable for our purposes, as will be demonstrated in Section 4.4.4.

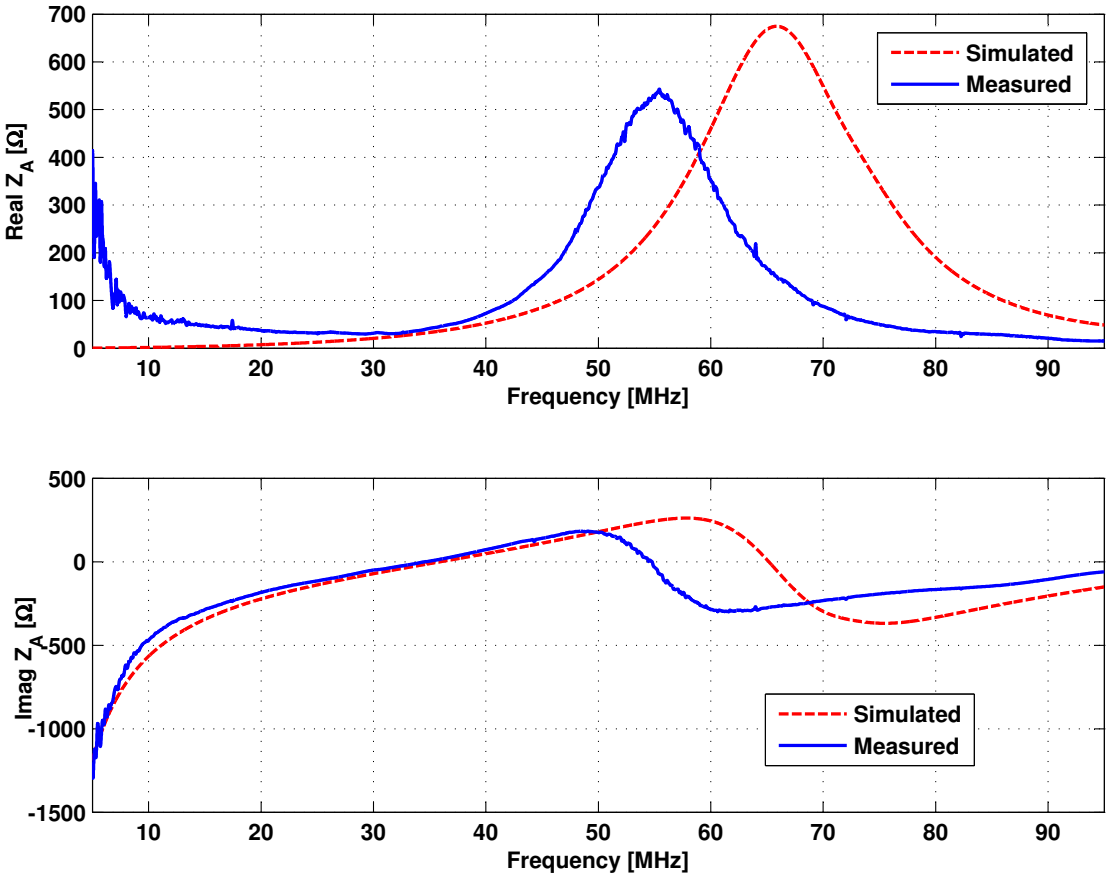


Figure 4.15: Simulated and measured impedance of the VHF monopole antenna.

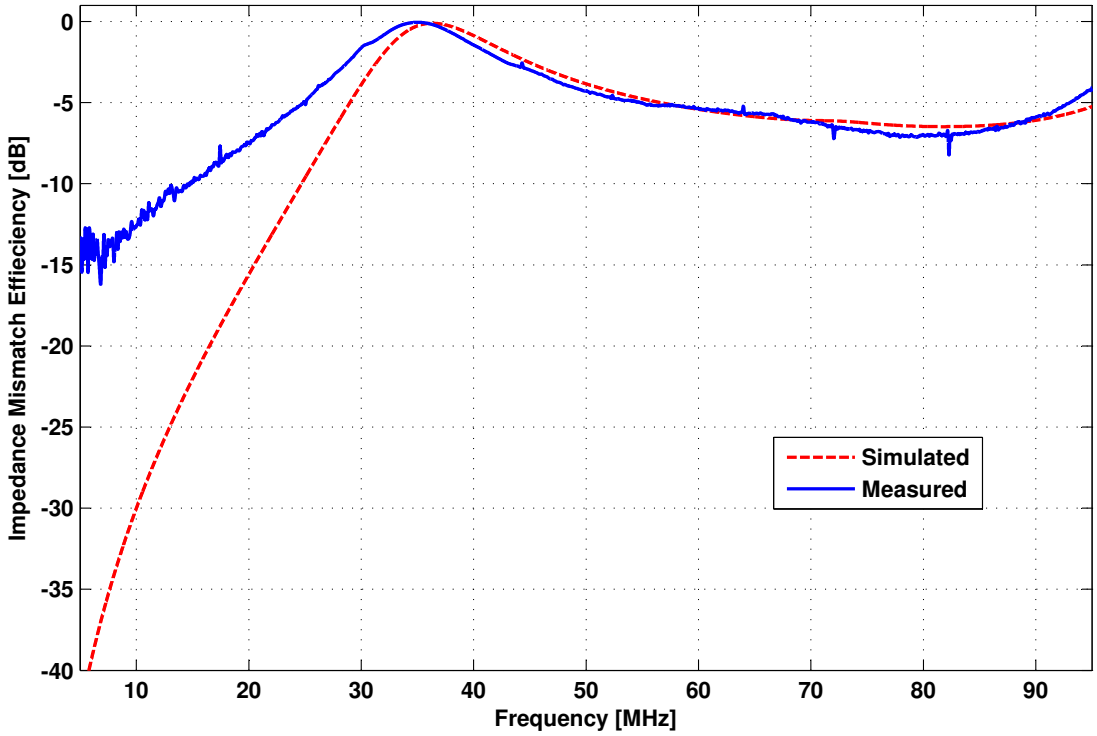


Figure 4.16: Calculated IME between the VHF monopole antenna and a preamplifier with $Z_p = 50\Omega$ using both the simulated and measured antenna impedance.

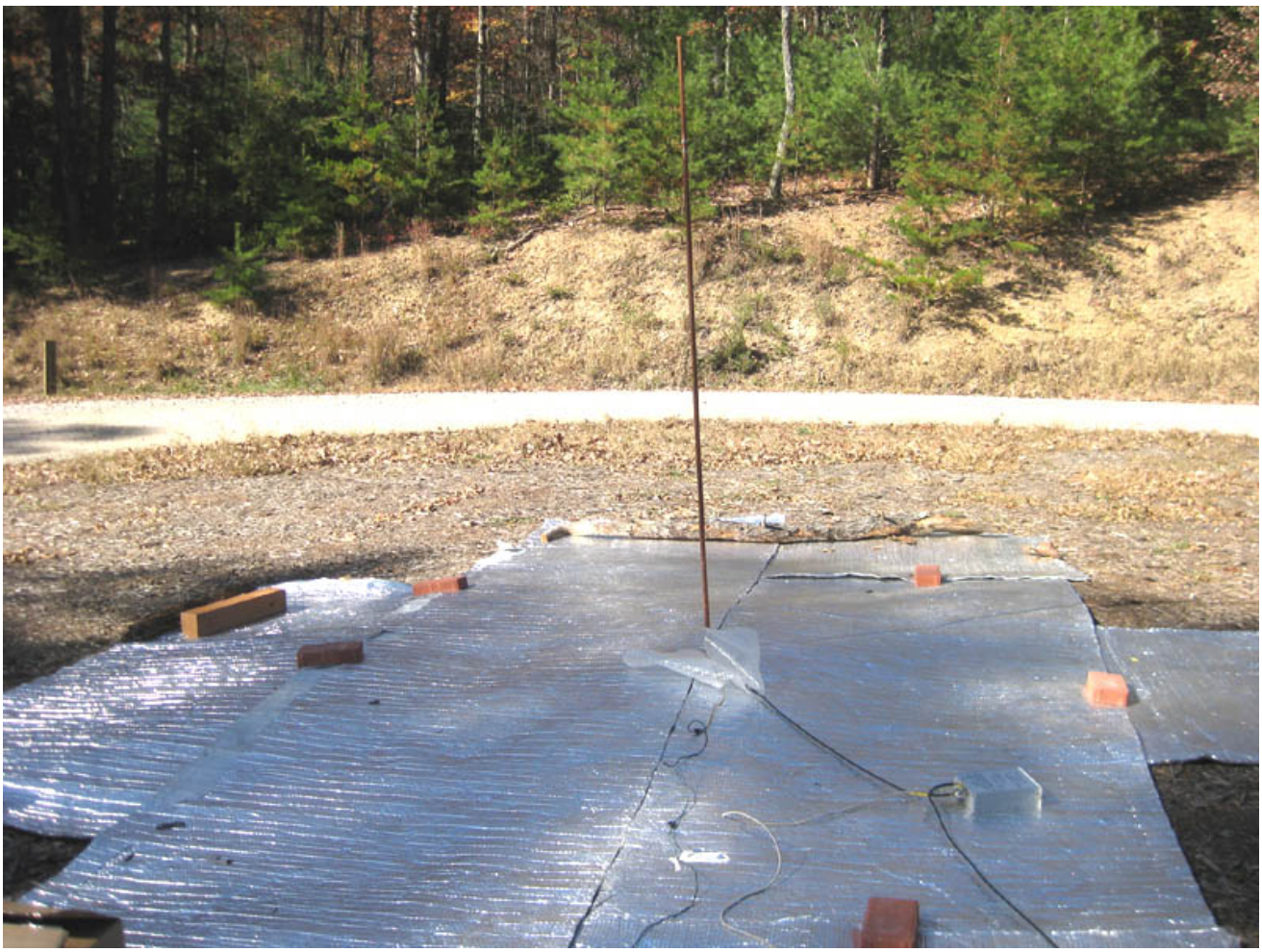


Figure 4.17: Antenna and ground screen setup during the field experiment.

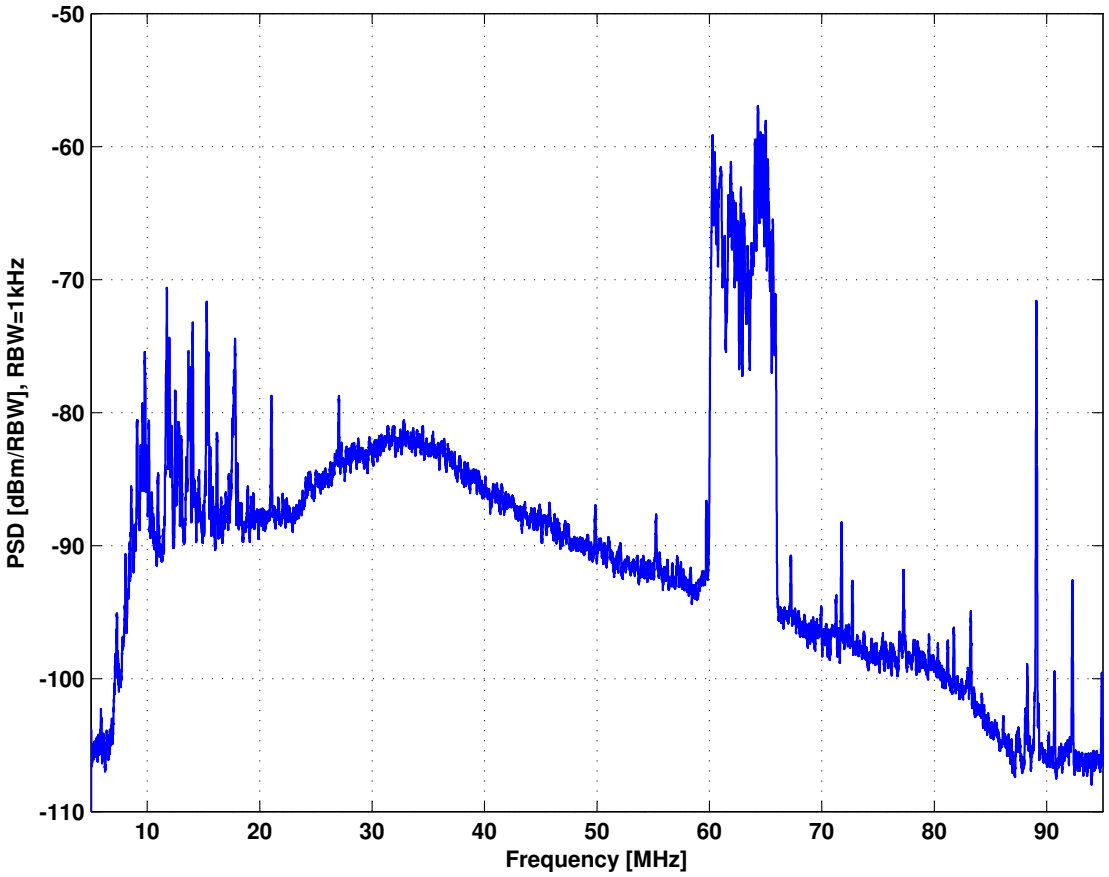


Figure 4.18: Measured integrated PSD at the input of spectrum analyzer. Integrated over 500 ms with 1 kHz spectral resolution.

4.4.3.1 Problems Overcome

In the first attempts of this experiment using a preliminary version of the receiver, we observed intermodulation due to the strong RFI signals apparent in Figure 4.18. This problem was solved by (1) adding the BSF–108+ FM reject filter shown in Figure 4.8, and (2) introducing additional attenuators between amplifier stages also as shown in Figure 4.8. Further investigation revealed that low–level RFI from our measurement instruments was also appearing in the measured data. The RFI was emitted from the data acquisition laptop PC, and also from an inverter which was used to convert DC power into AC for the spectrum analyzer and laptop PC. To solve this problem, the inverter was shut down during the measurement (the spectrum analyzer and the laptop PC used their own internal batteries) and the laptop PC was relocated approximately 150 ft away from the antenna using coaxial cable.

4.4.4 Results

Figure 4.19 shows the PSD of Galactic noise S_{in} referenced to the antenna terminals, i.e., at the input of the receiver, including IME. Figure 4.19 also shows two predicted PSD curves; one computed using the IME computed from the *measured* antenna impedance, and the second computed using the IME from the *simulated* antenna impedance from Section 4.4.2. Modifying Equation 4.4, the predicted value of S_{in} is calculated as

$$S_{in} = \eta k T_A \left[1 - |\Gamma|^2\right] \tag{4.10}$$

where T_A is calculated as explained in the next paragraph.

The previously defined Galactic noise model provides the median value of the noise temperature. However, in reality Galactic noise varies by approximately 3 dB as a function of time of day, and this variation depends on the antenna pattern also. Therefore, in order to get a precise prediction of PSD it is needed to use a more detailed and accurate model. This is done using a computer code developed by K. Deshpande [81]. This code predicts antenna temperature due to Galactic noise taking into account the location on the earth, antenna pattern, date, and time. It provides the antenna temperature for the frequency of 38 MHz, however this temperature can be extrapolated

to other frequencies using the factor $(\nu/(38\text{MHz}))^{-2.55}$, where ν is the frequency in MHz [74]. In summary, one of the main differences between the calculation of the Galactic noise temperature in this way and using Table 4.2 is that this calculation includes the diurnal variation as well as the antenna pattern and is thus more precise, whereas the calculation from Table 4.2 does not include these.

The prediction curves in Figure 4.19 also incorporate ground loss, which is estimated using the FEKO antenna simulation as follows: The antenna is simulated in transmission mode and the total radiated power is measured. This is done twice: once for realistic lossy ground ($\sigma = 5 \times 10^{-3}$ S/m, $\epsilon_r = 13$), and once for perfectly conducting ground. The ratio of these radiated powers then provides the ground loss efficiency. The finite ground screen was included during the simulation for realistic lossy ground. On the other hand, for the perfectly conducting ground simulation, this finite ground screen was excluded and the perfectly electric conducting ground plane was assumed to be infinite. Figure 4.20 shows result. Note that the computed efficiency (η) varies between –5.3 dB and –3.4 dB.

Referring to Figure 4.19, note that the measured PSD closely follows the predicted PSD estimated using the simulated antenna impedance. However, the measured PSD does not closely follow the predicted PSD estimated using the measured antenna impedance, specifically at the lower frequency region (below 35 MHz). The reason behind this probably the RFI–induced discrepancies between the measured and simulation antenna impedance observed in Figure 4.15; thus the simulated result is judged to be more accurate. Figure 4.21 shows the ratio of the predicted and the measured PSD for the two different cases: in the first case predicted PSD is calculated using the simulated antenna impedance, and in the second case predicted PSD is calculated using the measured antenna impedance. Note the agreement is very good between 35 and 70 MHz, and the "dropout" just above 60 MHz corresponds to the ATSC digital TV signal (Channel 3, 60–66 MHz). The discrepancy between simulated and measured results below 35 MHz corresponds to the difference in IME identified above. However, neither is particularly accurate in this region, perhaps because the antenna reactance is very large (thus, important to know precisely) in this frequency range. The error above 70 MHz probably due to the low γ; i.e., increasing contribution of internal noise relative to external noise.

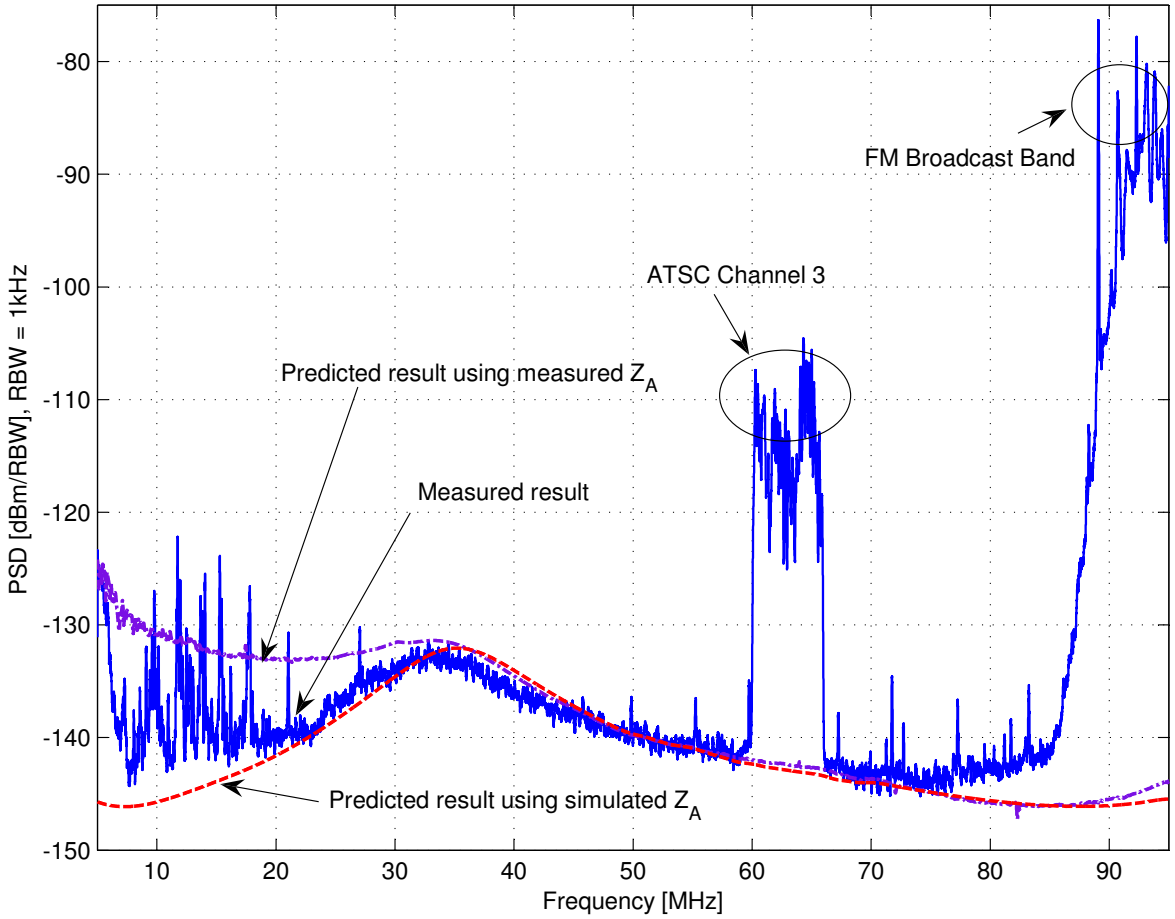


Figure 4.19: PSD referenced to the antenna terminals.

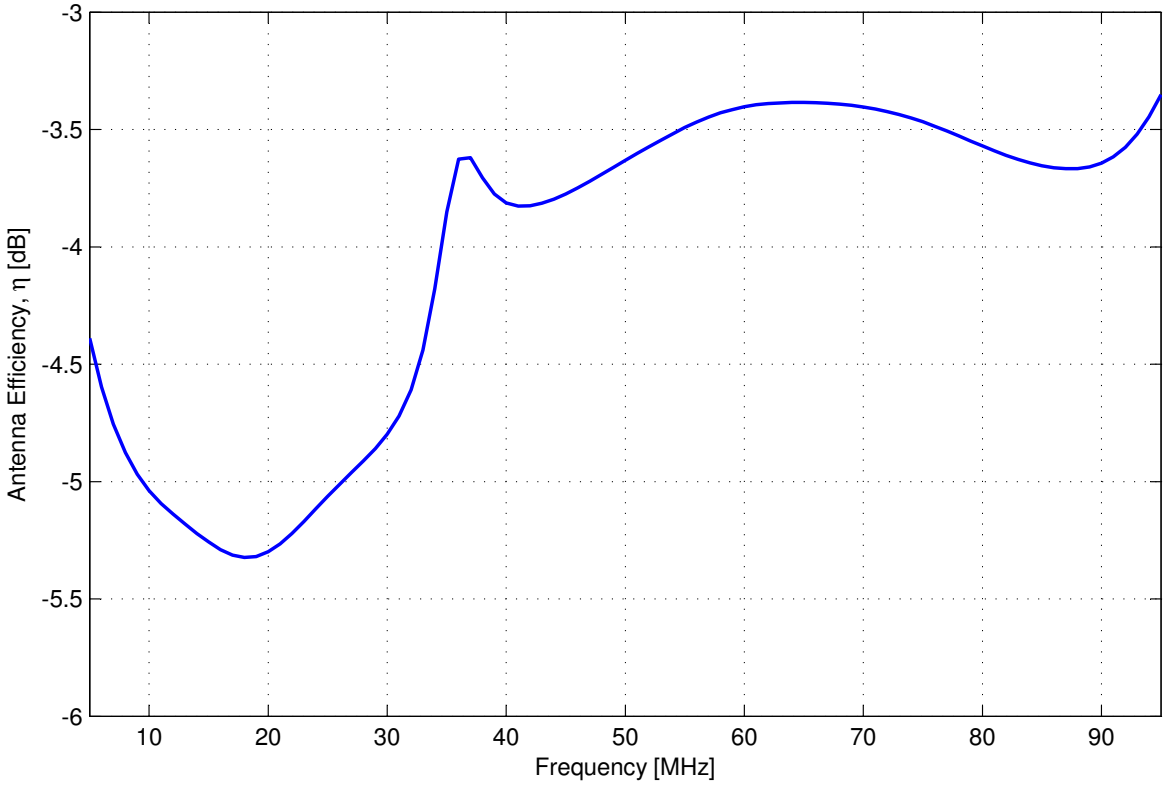


Figure 4.20: Antenna efficiency (η) assuming realistic ground with the ground screen shown in Figure 4.13 on it.

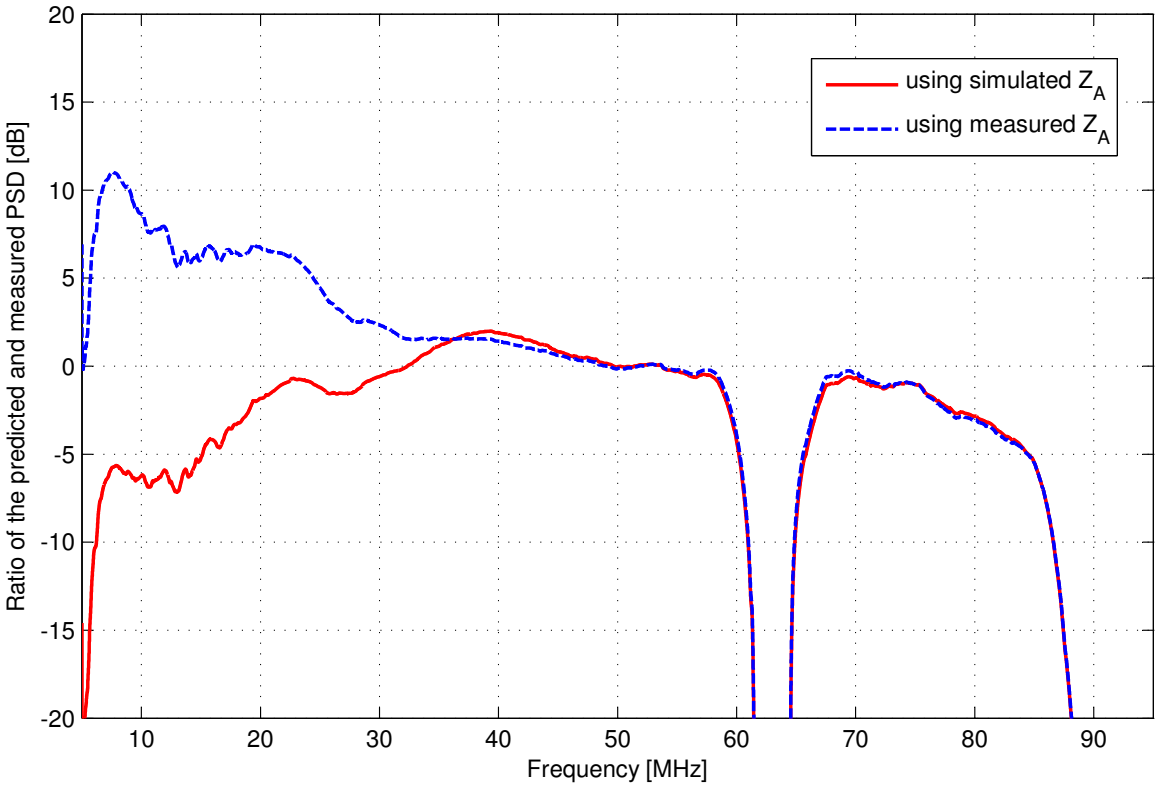


Figure 4.21: Ratio of the predicted to the measured PSD.

4.5 Summary

This chapter presented a concept to achieve "optimum" noise figure of a receiver from a sensitivity point of view. If a front end is external noise–dominated then the matching requirement between an antenna and a receiver can be loosened, and even a poor quality match can potentially provide nearly the best possible sensitivity. The concept was validated through a field experiment measuring Galactic noise using a VHF monopole antenna. Our measurement results closely follow the predicted results over much of the frequency range 20–75 MHz and discrepancies can be attributed to measurement or modeling errors. This experiment will be expanded in the next chapter to measure the performance of a new kind of sensitivity–constrained multiplexer. The next chapter describes the design methodology and performance analysis of this multiplexer.

Chapter 5

Multiplexer Design

Our goal is to present a design concept to build an RF front end for MMR to cover a large range of frequency bands using just a single antenna. As is pointed out in Chapter 2, in order to facilitate this, it is needed to incorporate a multiplexer in our design. A multiplexer also plays an important role to perform "preselection", i.e., implementation of selectivity before frequency conversion to manage intermodulation effects. Although antenna impedance varies significantly with frequency, most of the traditional methodologies of multiplexer design assume constant input/output impedance and do not consider external noise effects (described in Section 4.3). This chapter presents a new multiplexer design methodology incorporating the concept described in Chapter 4.

The organization of this chapter is as follows. Section 5.1 ("Classical Multiplexer Design Theory") discusses the classical theory of multiplexer design including its limitations. Current research trends in multiplexer design are presented in Section 5.2 ("Research Trends in Multiplexer Design"). Section 5.3 ("Sensitivity-Constrained Multiplexer Design") describes the new sensitivity–constrained multiplexer design concept. This design concept is demonstrated implementing an actual multiplexer for a VHF monopole antenna. The design description as well as detailed performance analyses are presented in Section 5.4 ("VHF Monopole Multiplexer Design Example"). This chapter is summarized in Section 5.5 ("Summary").

5.1 Classical Multiplexer Design Theory

A multiplexer is a parallel or series combination of filters which is used to separate the input into multiple frequency bands. Multiplexers are traditionally designed such that the impedance at all ports is a standard value, such as 50 Ω. Common multiplexer types include diplexers (1:2 ports) and triplexers (1:3 ports). An example of how a triplexer is used appears in Fig. 1.3. This section briefly introduces classical multiplexer design theory and its limitations, which we want to overcome in our design methodology.

It might at first appear that the design of the multiplexer could easily be accomplished by designing the filters using any standard filter design procedures, and then connecting the filters in parallel or series. However, in reality some interaction exists between the filters which could result in very poor performance. This is demonstrated in Figures 5.1 and 5.2. Figure 5.1 shows the schematic of two filters (a highpass and a lowpass) designed for 140 MHz cutoff frequency (at –1 dB) assuming constant 50Ω termination impedance. Figure 5.2 compares the TPG performance when they are connected individually and when they are connected together to 50Ω termination impedance. It should be noted how the TPG performance get worse by simply connecting these filters together. This interaction may be small for the filters with non–overlapping passbands, or filters with narrow bandwidth (say, on the order of 1% bandwidth or less) and with guard bands between channels. However for other cases, especially for filters with overlapping passbands, this interaction can be significant. Therefore, an objective of multiplexer design is to employ techniques in order to avoid those undesirable interactions between the filters.

Figures 5.3 and 5.4 show multiplexers for parallel–connected channels and for series–connected channels, respectively. A useful reference on multiplexer design is Matthaei, Young and Jones [14], which describes several methods to design multiplexers using these architectures. It presents design methodology using narrow-band filters with guard bands between channels, as well as multiplexers with contiguous passbands. These methods rely on the use of susceptance– or reactance–annulling networks (as shown in Figure 5.3 and 5.4) to mitigate or reduce the imaginary part of the multiplexer's total input admittance or reactance, respectively. Ideally, the combination of an annulling network and the total input impedance of a multiplexer should provide a nearly constant total input

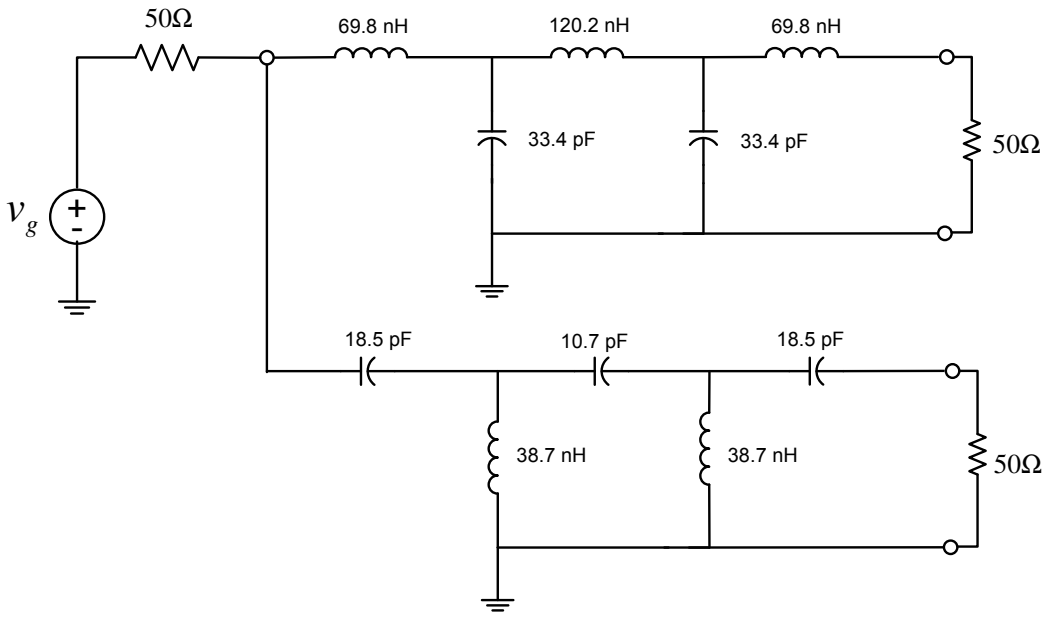


Figure 5.1: Circuit diagram of a diplexer. Each of the channels are designed for 50Ω termination impedance.

admittance or reactance, which approximates the generator conductance (G_g) or resistance (R_g), across the operating band of the multiplexer. In Figure 5.3, Y_i $(i = 1, 2, \ldots, n)$ represents the input admittance (i.e. the reciprocal of impedance) of the corresponding multiplexer channels, which are terminated by a constant conductance G_L. B represents the value of susceptance in the annulling network the purpose of which is to cancel the combined input admittance Y_{in} between channel filters. v_g represents the voltage generated by the source (antenna in our case). In Figure 5.4, Z_i $(i = 1, 2, \ldots, n)$ represents the input impedance of the corresponding multiplexer channels, which are terminated by a constant resistance R_L. Z_{in} is the total input impedance of the multiplexer and X represents the value of reactance in the annulling network.

A strategy for classical design proceeds as follows. Consider the parallel form of Figure 5.4. In [44], Bode shows that if the real part of an admittance (e.g., Y_{in} in Figure 5.3) has the rectangular form

$$\begin{aligned} \mathrm{Re}\,\{Y_{in}\} &= 0 \quad , \text{for } 0 \leq \omega < \omega_a \\ &= G_L \quad , \text{for } \omega_a \leq \omega < \omega_b \\ &= 0 \quad , \text{for } \omega_b \leq \omega < \infty \end{aligned} \tag{5.1}$$

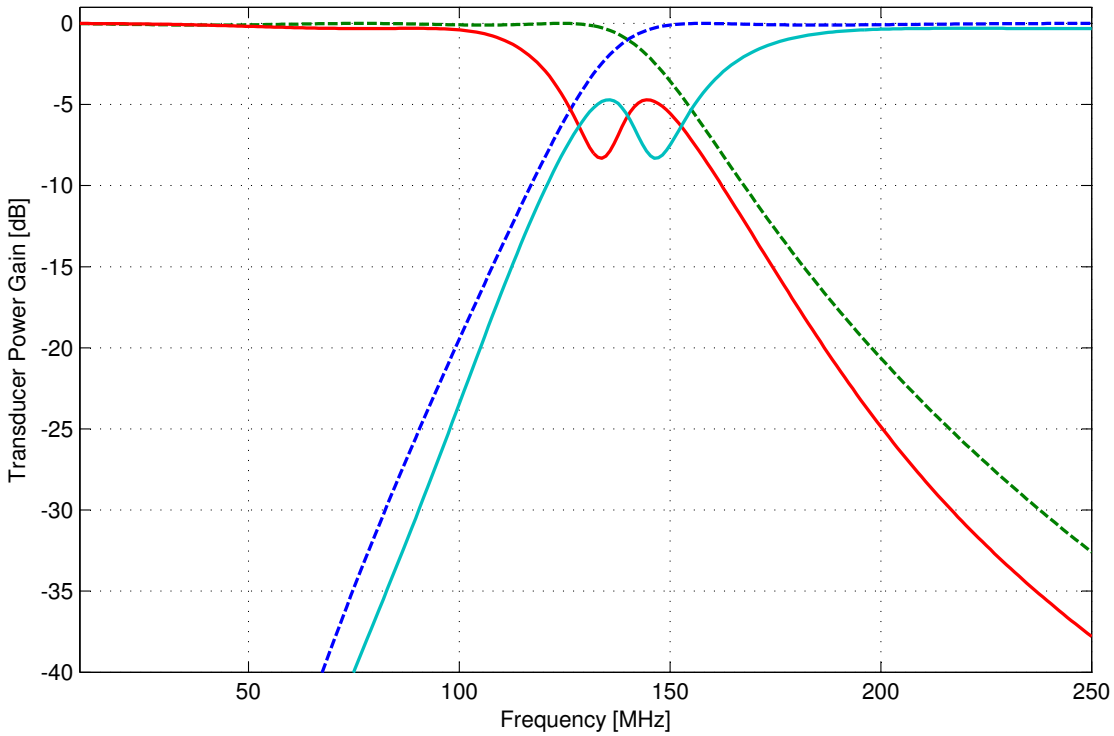


Figure 5.2: Performance (TPG) of the diplexer in Figure 5.1, assuming 50Ω source impedance. Each channels are designed for 50Ω termination impedance. Solid lines represent the results when the input ports of the diplexer channels are connected together and dotted lines represent the results when each of the channels are connected with the source separately.

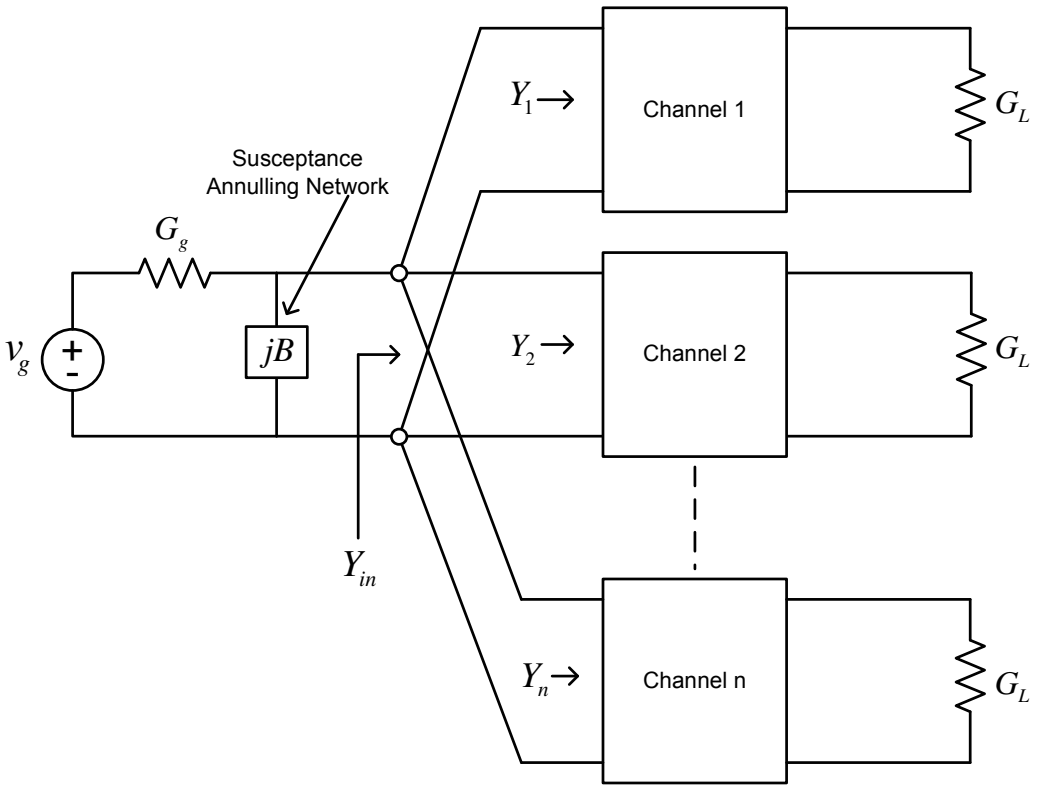


Figure 5.3: A parallel–connected multiplexer.

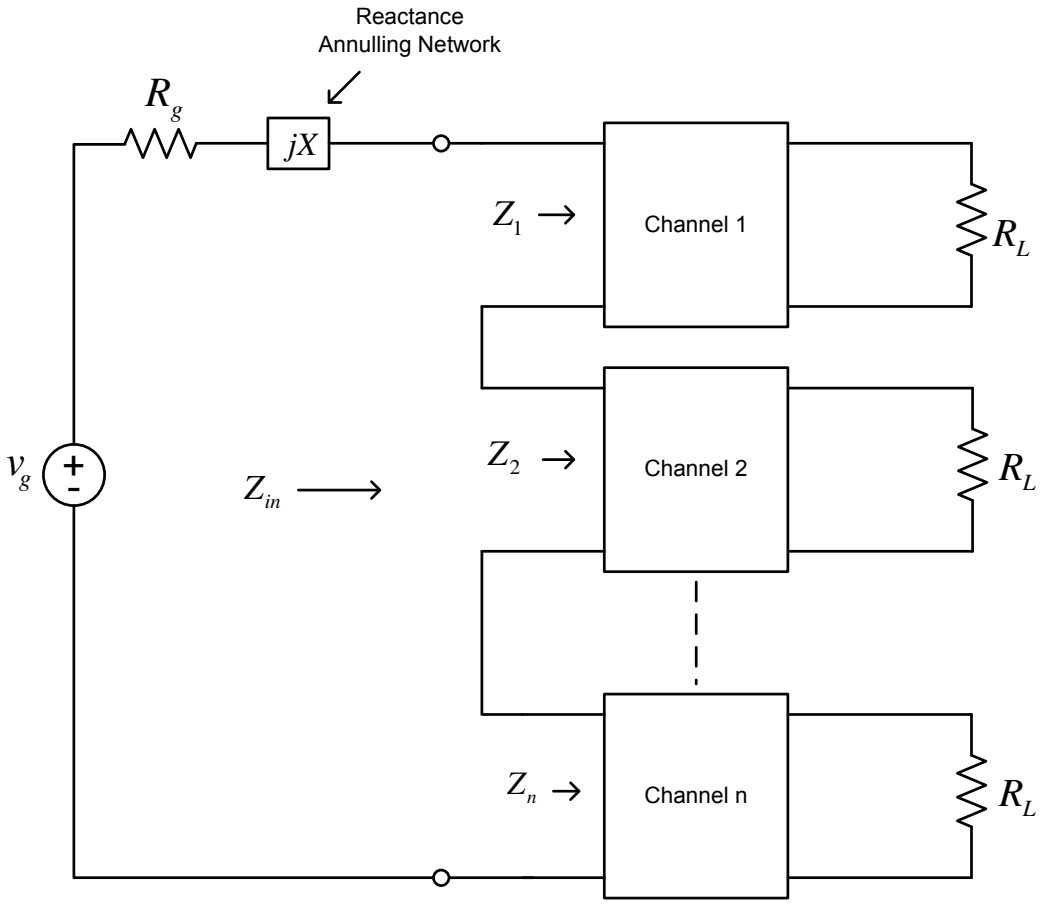


Figure 5.4: A series–connected multiplexer.

then the imaginary part of the admittance can be expressed as

$$\mathrm{Im}\{Y_{in}\} = \frac{G_L}{\pi} \ln \left| \frac{1 + \frac{\omega}{\omega_0} w - \left(\frac{\omega}{\omega_0}\right)^2}{1 - \frac{\omega}{\omega_0} w - \left(\frac{\omega}{\omega_0}\right)^2} \right| \tag{5.2}$$

where $\omega_0 = \sqrt{\omega_a \omega_b}$ and $w = (\omega_b - \omega_a)/\omega_0$. Thus a suitable annulling reactance exists for at least one frequency in $\{\omega_a, \omega_b\}$, and the bandwidth is limited by the tradeoff with TPG in the same manner as described in Section 3.2.

Figure 5.5 shows the antenna matching application. Traditionally, the antenna impedance $Z_A(\omega)$ is assumed to be a real, constant value over the frequency range of interest. Let us call this R_{A0}. The resulting design equation becomes

$$R_{A0} = Z_{mux}(\omega) = Z_{match}(\omega) \parallel Z_{in}(\omega). \tag{5.3}$$

The above equation needs to be solved for $Z_{match}(\omega)$ to realize a matching circuit which transforms the complex–valued input impedance of the multiplexer to a constant value, so that it can match with R_{A0}. The exact solution of this equation is very complex (perhaps not even possible) and the complexity increases with the number of channels. Alternatively, an approximate solution can potentially be found using a perturbation approach, i.e., starting with a crude initial solution, linearizing the design equation in the region of that solution, and then iterating to get the desired result. This approach permits the use of any design to implement the channelizing filters, but is not guaranteed to yield a realizable or useful solution for the matching circuit. Typically, optimization yields at best a loose fit to the requirement implied by Equation 5.3. The associated annulling network is typically a parallel–resonator circuit.

The main problem with this state of affairs with respect to what is required for MMR receiver front ends is that $Z_A(\omega)$ cannot be assumed to be constant (even approximately) over large bandwidth, as is demonstrated in Fig. 1.4. This issue has only recently begun to be addressed, as will be discussed in the next section.

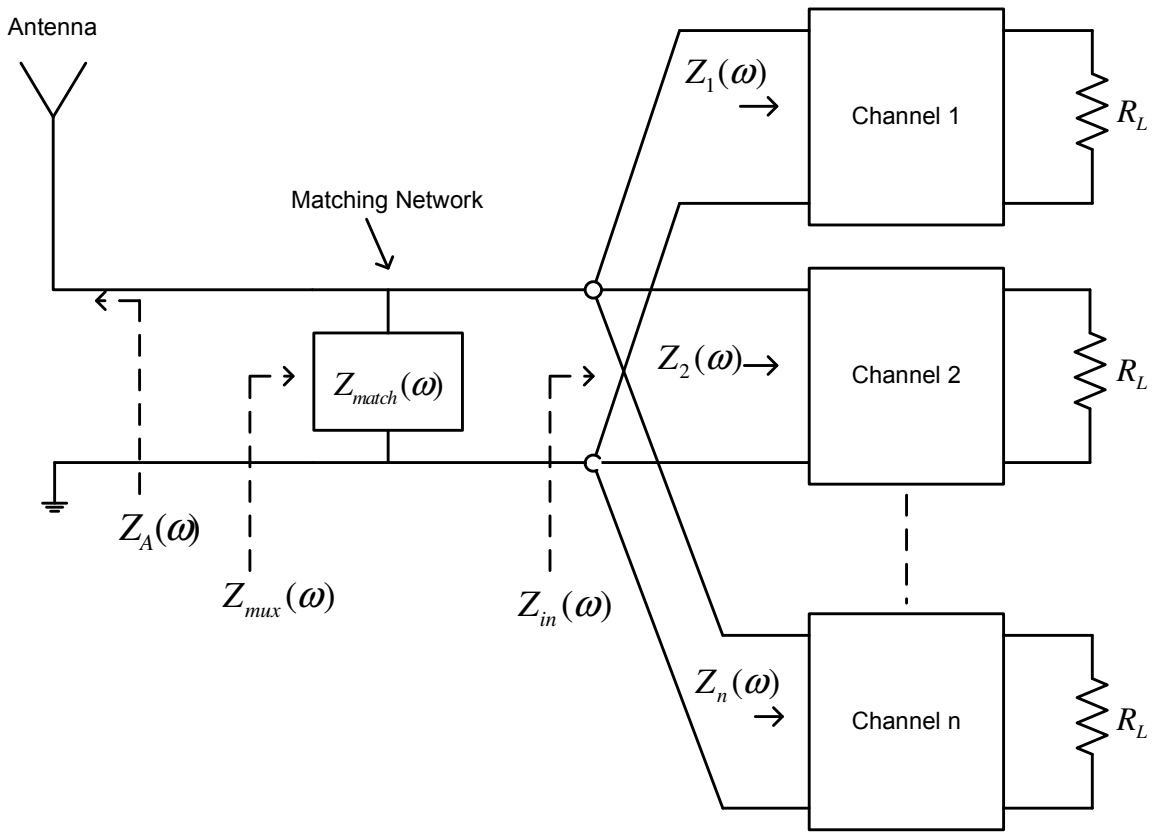


Figure 5.5: Multiplexer with parallel connected channels, input of which is connected with a matching circuit and an antenna.

5.2 Research Trends in Multiplexer Design

This section describes some recent research trends in multiplexer design.

Most of the current work on multiplexer design is for high frequency (GHz or more) applications. Some examples are as follows. An example of a wideband 10–35 GHz six-channel microstrip multiplexer was described by Hong and Cheng (2006) in [82]. Each of the channels contain filters centered at 10 GHz, 12 GHz, 19 GHz, 21 GHz, 32 GHz, and 35 GHz. All of these filters are parallel–coupled microstrip bandpass filters composed of half–wavelength resonators with 500 MHz bandwidth. Deng (2006) described a matching circuit for microstrip triplexer to minimize the interaction among the bandpass filters [83]. His methodology was demonstrated designing a multiplexer with channels centered at 1.48 GHz, 1.75 GHz, and 1.98 GHz. Each of the channels provide approximately 5% fractional bandwidth. Another recent example of multiplexer design is a microstrip four-channel multiplexer for a dual-band WLAN-UWB receiver, proposed by Lai and Jeng (2005) in [84]. Each of the output ports consists of a dual–band bandpass filter: one with two passbands from 2.1 to 2.9 GHz and from 5.1 to 5.9 GHz (for WLAN), and other with two passbands from 3.1 to 4.9 GHz and from 6.1 to 8.2 GHz (for UWB). In this work a Genetic algorithm (GA) technique was employed to determine circuit topology and to overcome the interaction between the filters. GA techniques might be useful in future development of a design methodology (the approach we present in Section 5.3) to optimize the multiplexer channel filters.

An example of an innovative multiplexer design which uses passive circuit components in a frequency range of greater interest was presented by Galbraith *et. al.* (2008) in [85]. A 20–channel multiplexer with contiguous channels was demonstrated from the frequency range 20–90 MHz. The design of this multiplexer is inspired by the cochlea of the human inner ear. The cochlea separates sound into frequency bands with high selectivity using a very simple techniques; the analogous electrical circuit is also relatively simple and effective. However, this approach is limited in the fractional bandwidth of the channels, and thus is not entirely suitable for wideband mobile/portable MMR applications.

A common feature of all of these above examples is the use of standard input/output impedances, which is a constraint we wish to relax. However, researchers are only very recently beginning to

think about this. In [86], Wu and Meng (2007) present a direct synthesis approach for general Chebyshev filters terminated by a complex load at one end and a real valued load on the other. They presented a methodology to normalize the assumed complex matched impedance at one end of the filter to the same real valued matched impedance as that at the other end of the filter so that the existing synthesis techniques for general Chebyshev filters can be applied. The design process starts with selecting the complex impedance (which needs to be matched) at the center frequency of the filter. Then it is normalized to the reference impedance using the proposed design methodology. Finally, they determine the necessary coefficients to realize the circuit. A diplexer, the filters of which are centered at 1.74 GHz and 1.85 GHz frequency, is demonstrated using this process. The bandwidth of both filters is approximately 80 MHz. Although this methodology helps to design filters for complex termination impedance, it is still limited to achieve good matching only at a single frequency per band instead of wide range of frequencies. This design methodology is also limited to the use of filters with narrow fractional bandwidth.

In summary, no existing technique is entirely satisfactory for mobile/portable MMR, for the following reasons. Most of the previous techniques are for high frequency (GHz or more) and are less useful to design multiplexers for low frequency (less than GHz), where discrete inductors and capacitors must typically be used in lieu of wavelength–scale structures such as microstrip lines and waveguides. The previous techniques are also limited by the use of either standard input/output impedance or at best constant complex input/standard output impedance. Most of the described techniques are also limited to narrow fractional bandwidth. We would like to relax these limitations by using the concept described in Chapter 4 to design a new kind of sensitivity–constrained multiplexer. The next section describes this concept in more detail.

5.3 Sensitivity-Constrained Multiplexer Design

This section explains the concept of sensitivity–constrained multiplexer design. To bypass some of the difficulty associated with antenna matching, we propose an alternative design goal emphasizing system sensitivity over impedance matching. This is motivated by the observation, made in Section 4.2, that external noise can be very strong in practical scenarios, especially at low frequencies.

According to Equation 4.7, the ratio of external (unavoidable) noise to internally generated noise is

$$\gamma(\omega) = \eta \frac{T_A(\omega)}{T_p} \left[1 - |\Gamma(\omega)|^2\right] \tag{5.4}$$

where in this case reflection coefficient $\Gamma(\omega)$ is

$$\Gamma(\omega) = \frac{Z_{mux}(\omega) - Z_A^*(\omega)}{Z_{mux}(\omega) + Z_A^*(\omega)}. \tag{5.5}$$

Clearly, sensitivity is optimized by minimizing $|\Gamma(\omega)|$ (i.e., good matching) and minimizing T_p (i.e., low noise design). However, once γ is high (greater than about 5 or so), additional effort to minimize $|\Gamma(\omega)|$ or T_p will have little effect on sensitivity. Furthermore, if acceptable γ can be achieved for a poor $|\Gamma(\omega)|$ – as is possible when T_A is large – improvements in $|\Gamma(\omega)|$ are actually counter-productive, since this limits the design by imposing unnecessarily strict matching requirements.

Our proposed technique starts with designing each of the multiplexer channel filters for standard (e.g., 50Ω) input and output impedance, connecting the input port of the multiplexer channels together to the antenna, and then performing the optimization of the multiplexer channels according to the following principles:

1. The ratio γ at the multiplexer output should be large, and
2. The multiplexer TPG should be "reasonably flat" over the passband.

Let the TPG of the channels be $T_i(\omega)$, where $i = 1, 2, \ldots, n$ represents the channel number; and the value of components (i.e., inductors or capacitors) used in the channels is $X_{i,j}$, where $j = 1, 2, \ldots, p$ represents the component numbers in each channel. The optimization is

$$\min_{\{X_{i,j}\}} \quad \sum_{i=1}^{n} \int_{\omega_{a,i}}^{\omega_{b,i}} \left[T_i(\omega) - T_{BF,i}\right]^2 d\omega \tag{5.6}$$

where $T_{BF,i}$ is the theoretical TPG calculated using the Bode–Fano bound at the center frequency of each channel; $\omega_{a,i}$ and $\omega_{b,i}$ are the lower and higher cutoff frequencies of each channel respectively. This attempts to find $X_{i,j}$'s such that the best possible fit to the optimum estimated per–channel

TPGs is obtained. Note that the quality of the fit is assessed using a mean–square error criteria. Since it is likely that a perfect solution will not be found, we also specify a criteria for stopping the optimization:

$$T_i(\omega)|_{max} - T_i(\omega)|_{min} < \epsilon_i \tag{5.7}$$

where $T_i(\omega)|_{max}$ and $T_i(\omega)|_{min}$ are the maximum and minimum values of the TPG over channel i, and ϵ_i is a "flatness" constraint for each channel. Note that the starting point of selecting ϵ_i can be the ripple of the Chebyshev filters which are originally designed for each channel. If the optimization does not converge then depending on the need the value of ϵ_i can be increased.

Any multivariable optimization technique can be used to optimize the component values. The optimization does not require or depend on any particular algorithm. This design methodology is demonstrated in the next section.

5.4 VHF Monopole Multiplexer Design Example

In this section we demonstrate the method of sensitivity–constrained multiplexer design proposed in Section 5.3, and evaluate the design in field conditions to confirm that the results are as expected. In this design example, we add a three–channel multiplexer to the VHF monopole antenna described in Section 4.4.2, and use the same experimental system to conduct new measurements. This section is organized as follows. Section 5.4.1 ("Problem Statement") demonstrates the limitation of classical (constant impedance) multiplexer design in the specific context of this example. Section 5.4.2 ("Multiplexer Design") presents an improved design using the sensitivity–constrained approach. Section 5.4.3 ("Experiment Design") and Section 5.4.4 ("Data Collection") presents the field experiment and data collection methodology, respectively. Finally, results are presented in Section 5.4.5 ("Results").

5.4.1 Problem Statement

Our goal is to interface the antenna shown in Figure 4.15 to separate receiver inputs corresponding to the 10-28 MHz, 32-50 MHz, and 54-80 MHz bands. The interface concept of this multiplexer

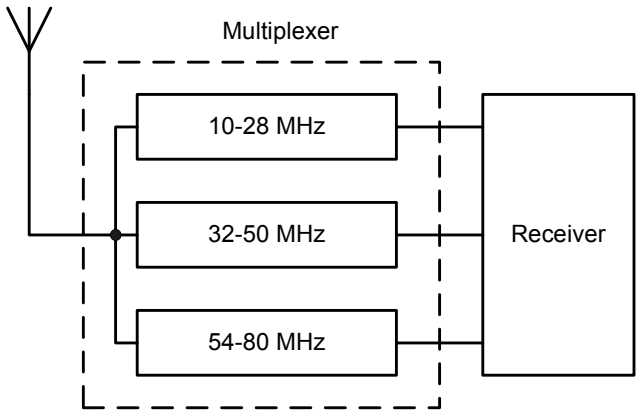


Figure 5.6: Multiplexer interfacing concept.

is shown in Figure 5.6. We initially design the multiplexer channels for constant 50Ω frequency–independent input and output impedances, neglecting the possibility of interaction. Each of the channels of this multiplexer are designed using the 7^{th} order Chebyshev topology shown in Figure 5.7. The component values of these filters is presented in Table 5.1.

Figure 5.8 shows the performance of this initial multiplexer assuming constant 50Ω antenna impedance. Once interfaced to the antenna, however, the result is as shown in Figure 5.9. Note that the performance is dramatically degraded, especially in the 10–28 MHz band. The fractional bandwidth of the first channel is very large (approximately 110%), which is makes it more difficult to get good matching over the entire frequency band. The next section presents the multiplexer design using the methodology described in Section 5.3 to improve the overall performance of this multiplexer from sensitivity point of view.

5.4.2 Multiplexer Design

The design procedure of the VHF monopole multiplexer including the performance analysis is presented in this section. This section is organized as follows. Section 5.4.2.1 ("Optimization") presents the optimization criteria and simulated performance of the multiplexer. Circuit board implementation and lab measurement results are discussed in Section 5.4.2.2 ("Implementation & Lab Results").

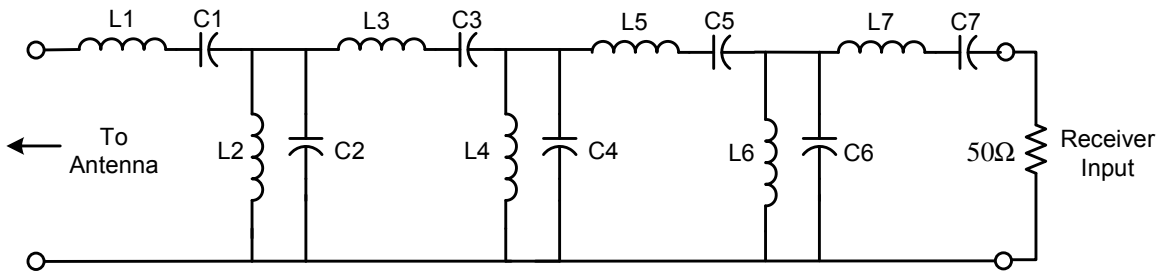


Figure 5.7: Circuit topology of each multiplexer channel. The inputs of the three channels are connected in parallel.

Table 5.1: Component values of the multiplexer channels designed for constant 50Ω input and output impedances.

Component	**Channel–1**	**Channel–2**	**Channel–3**
L1 (nH)	768.1	768.1	531.7
C1 (pF)	117.8	20.6	11.0
L2 (nH)	406.7	71.2	38.1
C2 (pF)	222.5	222.5	154.0
L3 (nH)	1166.4	1166.4	807.5
C3 (pF)	77.6	13.6	7.3
L4 (nH)	380.7	66.6	35.6
C4 (pF)	237.7	237.7	164.6
L5 (nH)	1166.4	1166.4	807.5
C5 (pF)	77.6	13.6	7.3
L6 (nH)	406.7	71.2	38.1
C6 (pF)	222.5	222.5	154.0
L7 (nH)	768.1	768.1	531.7
C7 (pF)	117.8	20.6	11.0

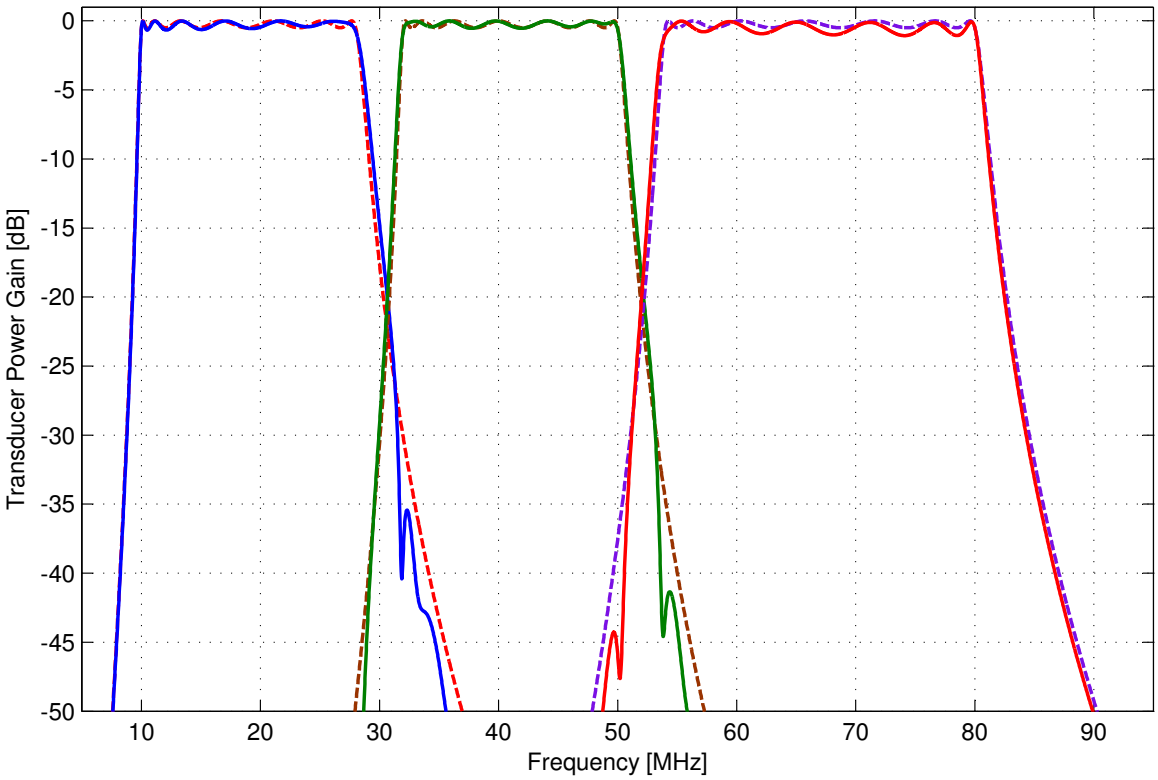


Figure 5.8: Performance (TPG) of the initial (50Ω–in, 50Ω–out) multiplexer, assuming constant 50Ω source impedance. Solid lines represent the results when input port of all multiplexer channels are connected together and dotted lines represent the results when each of the channels are connected with the source separately.

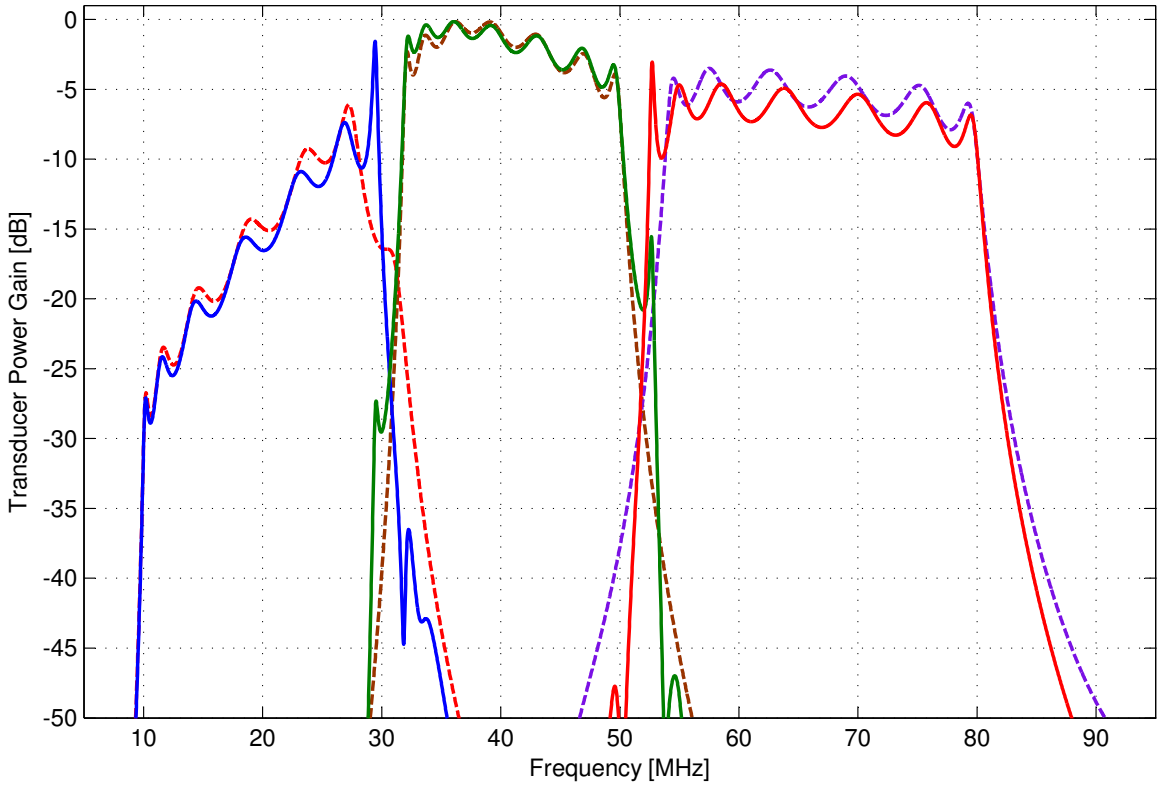


Figure 5.9: Performance (TPG) of initial (50Ω–in, 50Ω–out) multiplexer, assuming the simulated impedance of the VHF monopole. Solid lines represent the results when input ports of all multiplexer channels are connected together and dotted lines represent the results when each of the channels are connected with the source separately.

Table 5.2: Maximum theoretical TPG calculated from Bode–Fano limits assuming best fit RC/RL antenna impedances. n is the order of Chebyshev matching filter.

Parameter	**Channel–1 (10–28 MHz)**	**Channel–2 (32–50 MHz)**	**Channel–3 (54–80 MHz)**
f_0	16.73 MHz	40 MHz	65.73 MHz
B	110%	40%	50%
$Z_A(f_0)$	$4.9 - j296.5\ \Omega$	$52.5 + j48.0\ \Omega$	$674.4 - j41.6\ \Omega$
R	4.9 Ω	52.5 Ω	674.4 Ω
Series C or L	32.0 pF	191.0 nH	58.2 pF
$\lvert\Gamma(f_0)\rvert_{min}$	0.95	4.8×10^{-4}	1.2×10^{-56}
TPG ($n = \infty$)	−10.4 dB	≈ 0 dB	≈ 0 dB
TPG ($n = 7$)	−13.8 dB	≈ 0 dB	≈ 0 dB

5.4.2.1 Optimization

Before starting the optimization we need to have an idea about the theoretically best possible TPG, i.e., the maximum possible TPG for both infinite number of matching sections as well as 7^{th} order Chebyshev topology in a matching circuit, from the Bode–Fano bound using the equations in Section 3.2.1 for each multiplexer channel. To calculate the Bode–Fano bound, the antenna impedance is approximated using a series RC or series RL model in our desired frequency band. The procedure is specifically as follows:

1. For each channels' geometric center frequency (f_0), the impedance of the VHF monopole antenna is calculated.

2. From this impedance we calculate the value of the series resistance R, and the series capacitance C or series inductance L (depending on the positive or negative reactance value). Figure 5.10 shows the antenna impedance calculated from the series RC and series RL approximation of the VHF monopole antenna, compared to the actual (simulated) values.

3. Using these values and the fractional bandwidths of each channel, the theoretical TPG is calculated using Equations 3.13 to 3.18. The results are shown in Table 5.2. This table also shows the TPG limit for a matching circuit using 7^{th} order Chebyshev topology.

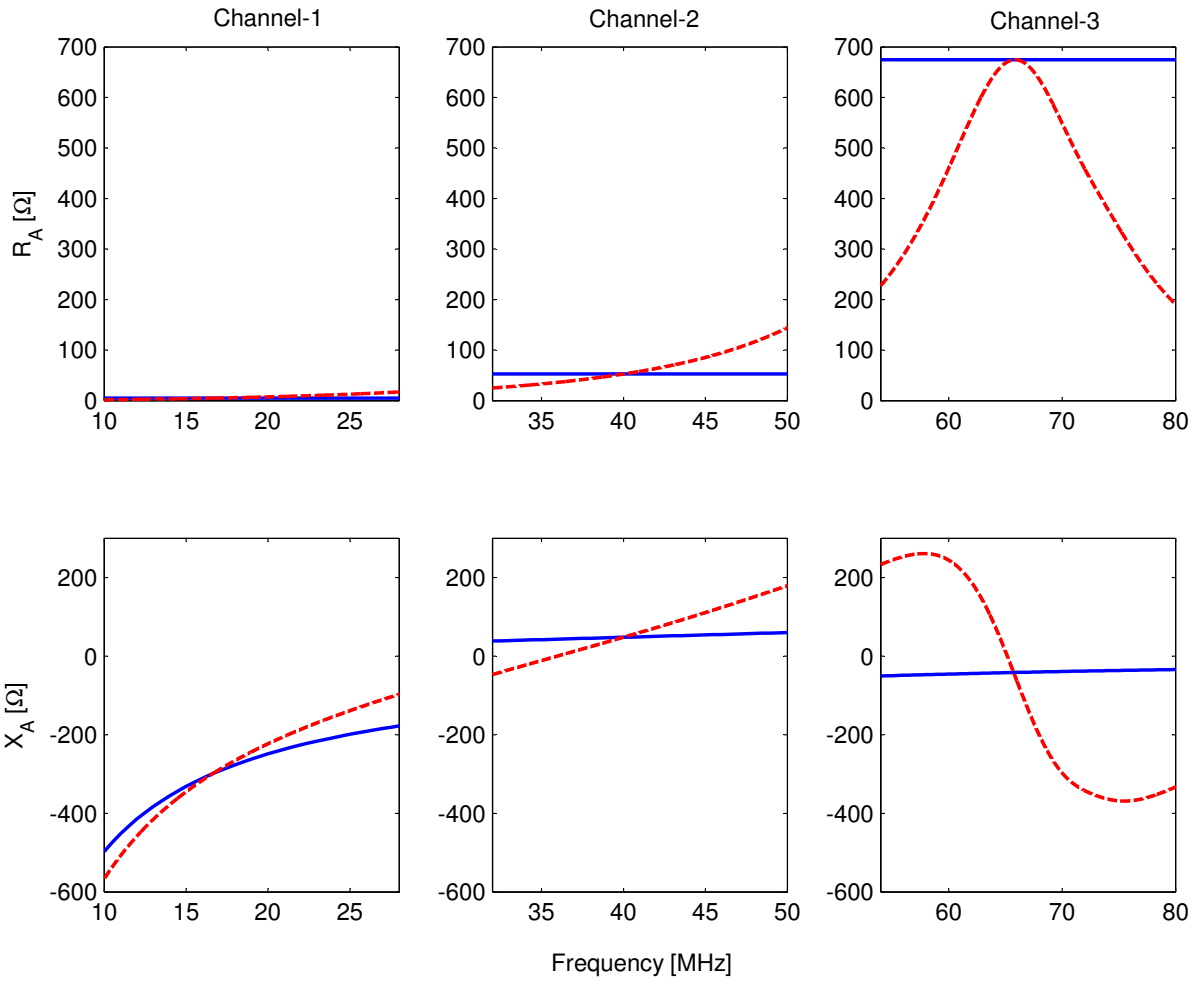


Figure 5.10: Antenna impedance calculated from center frequency series RC or series RL approximation (as appropriate) of the VHF monopole antenna. Solid lines represents the approximation and dotted lines represent the original value.

The multiplexer filters are optimized following the methodology described in Section 5.3. In this design we used the simulation software GENESYS from Agilent Technologies[1], which uses the "pattern search" algorithm described in [87], to perform our optimization. Since the original 7^{th} order Chebyshev filters were designed for 1 dB ripple, initially the ϵ_i's were chosen to be 1 dB for all channels. However, better results were obtained when the values of the ϵ_i's were changed to 10 dB, 3 dB, and 2 dB for Channels 1, 2, and 3, respectively. The optimized component values are presented in Table 5.3 along with closest standard values, and the performance results are shown in Figures 5.11 and 5.12. Note that the optimization significantly improves the performance of Channel 1 and 3. The degradation due to the use of standard component values affects primarily Channel 3.

Figure 5.13 shows the values of γ for various preamplifier noise figures such as 2 dB, 3 dB, and 4 dB, assuming Celestial noise as external noise environment. Figure 5.14 shows the same result assuming "Residential" noise as external noise environment. Note that the noise ratio is increased significantly for "Residential" noise compared to Celestial noise. It should also be noted that this design achieves large γ (factor of 5 or so) for the worst case of Celestial noise, despite poor TPG, for a preamplifier noise figure of 3.0 dB, which is a reasonable noise figure to be achieved using currently available RF devices. Based on the above performance results we can conclude that the proposed design methodology yields a significantly improved multiplexer. The next section presents a lab measurement of the implemented multiplexer.

5.4.2.2 Implementation & Lab Results

The optimized multiplexer was implemented and fabricated in a two–layer printed circuit board using the standard component values shown in Table 5.3 (see Figure 5.19 for an image). Appendix C provides details of the design, PCB layout, and bill of materials (BOM).

We performed a lab test of the multiplexer, so as to anticipate the field experiment results. Since it was not practical to perform this lab test with the source impedance of the actual antenna, we instead measured the S_{21} (forward voltage gain) parameter through each of the channels using

[1] http://eesof.tm.agilent.com/products/genesys

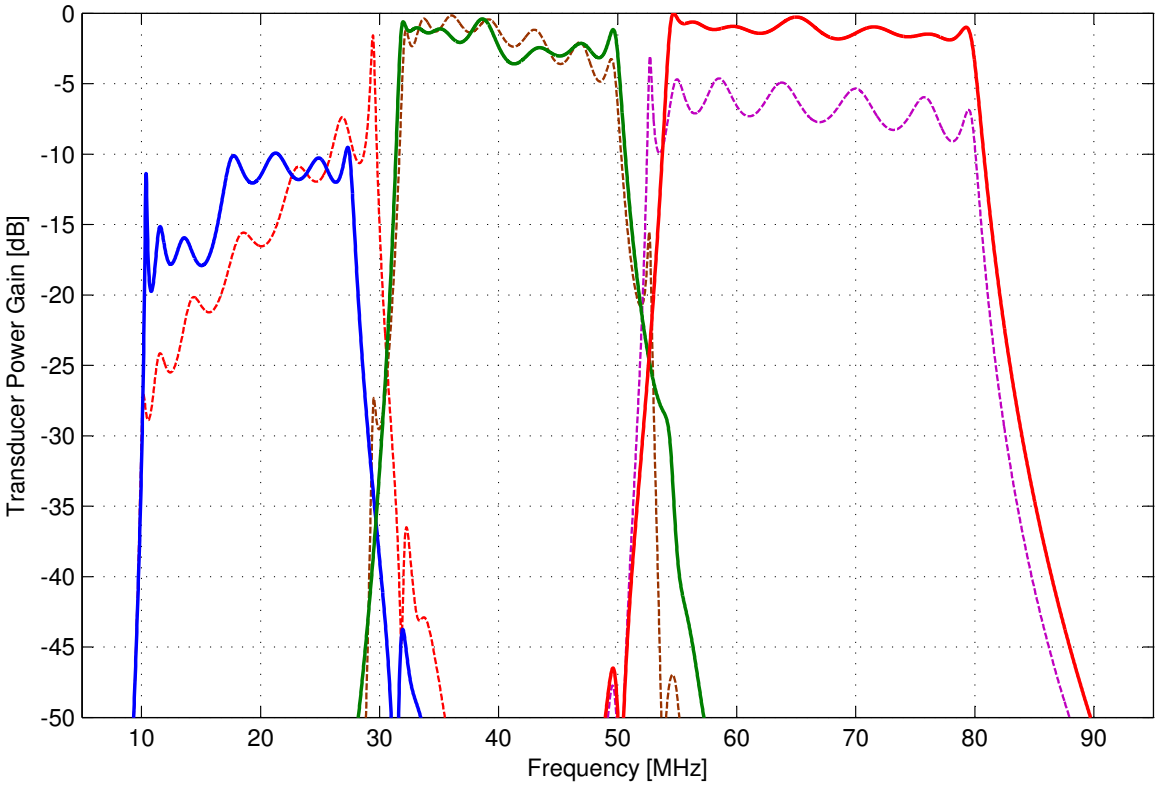


Figure 5.11: Performance (TPG) of optimized multiplexer, assuming simulated impedance of VHF monopole. Solid lines represent the results after optimization and dotted lines represent the results before optimization.

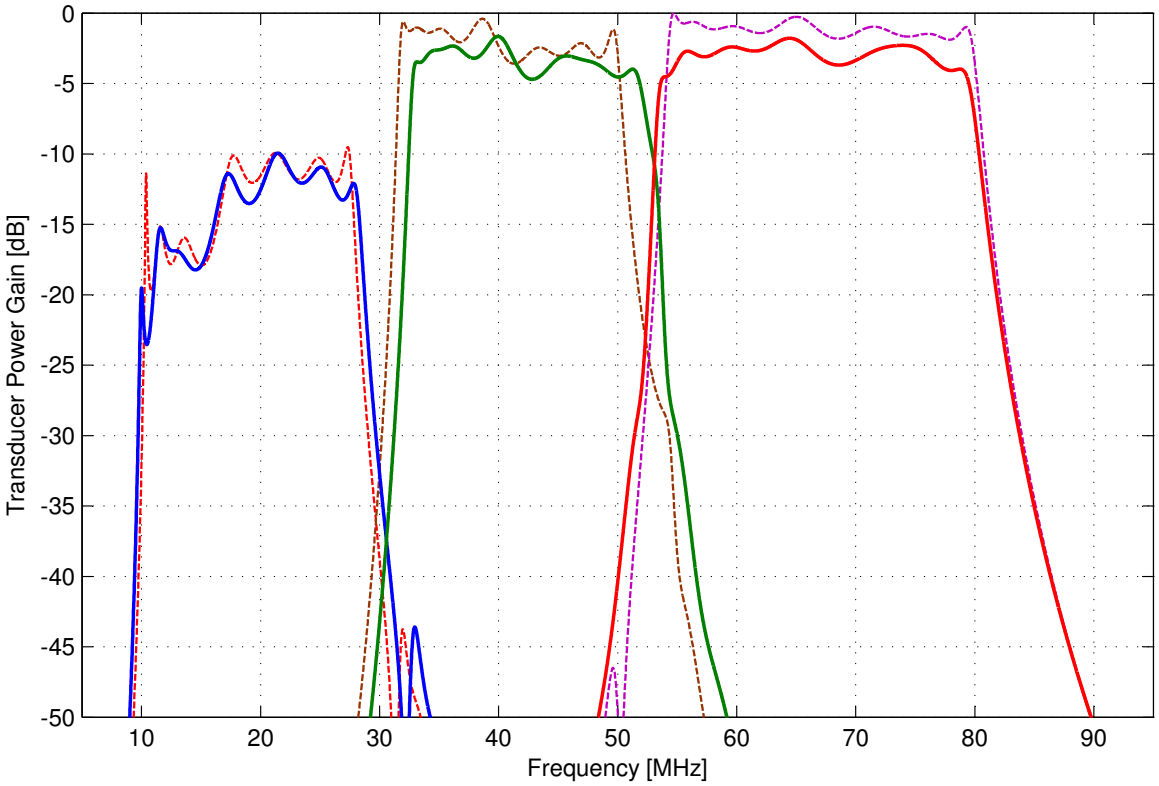


Figure 5.12: Performance (TPG) comparison of optimized multiplexer for original and standard component values. Solid lines represent the performance using standard component values and dotted lines represent the performance using original values.

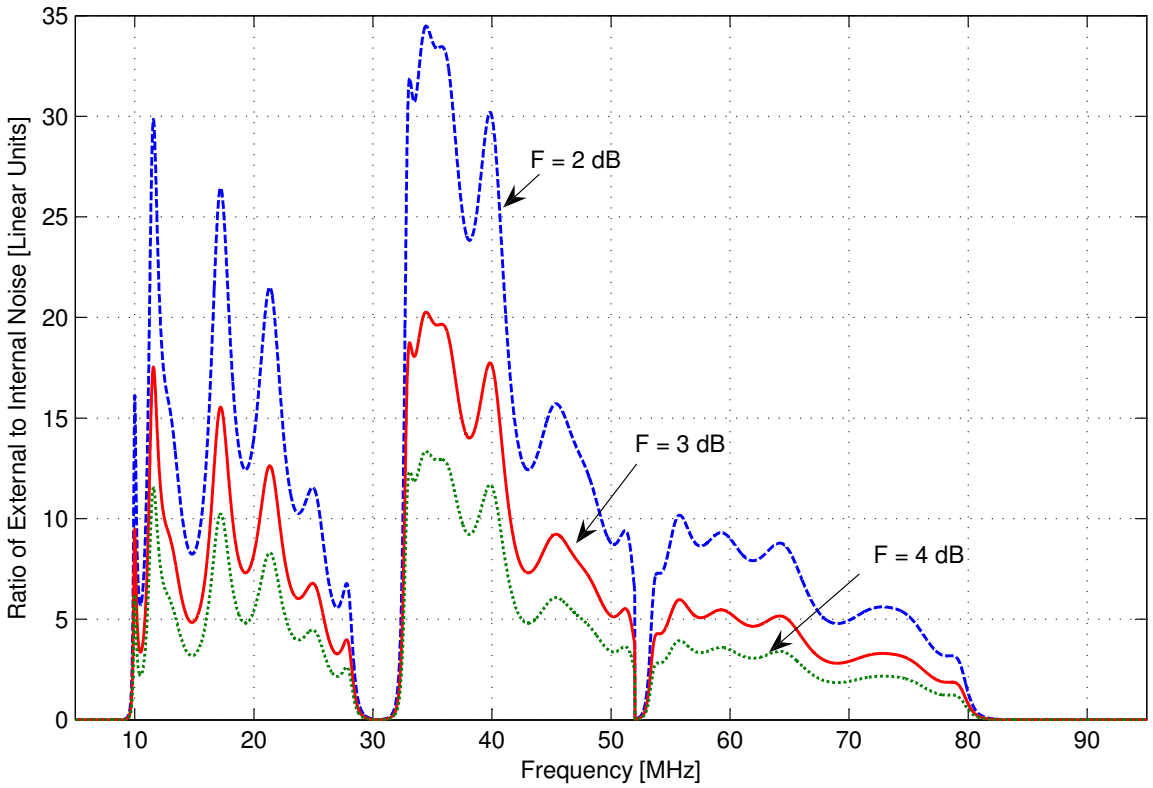


Figure 5.13: Performance (γ) of optimized multiplexer (using standard component values) for 2, 3, and 4 dB preamplifier noise figures, assuming simulated impedance of the VHF monopole antenna and Celestial noise.

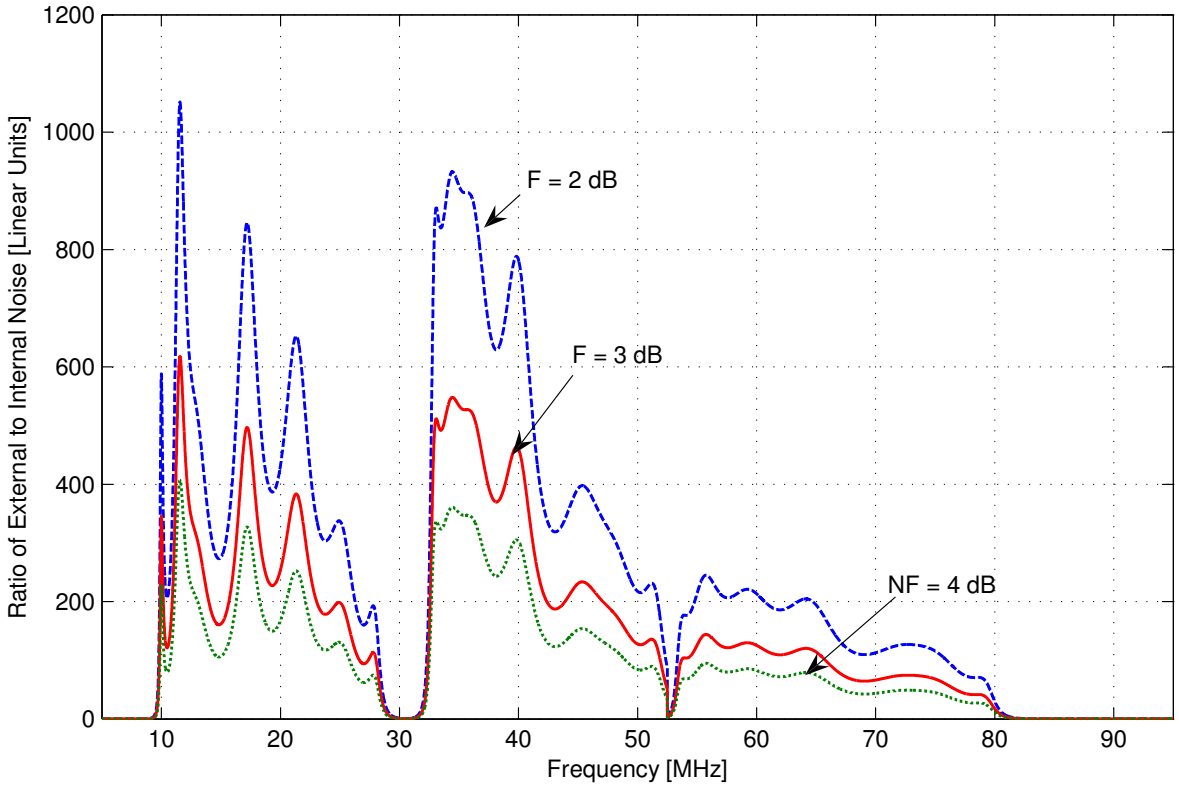


Figure 5.14: Performance (γ) of optimized multiplexer (using standard component values) for 2, 3, and 4 dB preamplifier noise figures, assuming simulated impedance of the VHF monopole antenna and "Residential" noise.

Table 5.3: Original and nearest standard component values for the multiplexer after the optimization for the simulated impedance of the VHF monopole antenna.

Component	**Channel–1**		**Channel–2**		**Channel–3**	
	Original	Standard	Original	Standard	Original	Standard
L1 (nH)	1201.9	1198.0	1179.7	1198.0	1.3	22.0
C1 (pF)	10000.0	10000.0	15.8	15.0	17.1	18.0
L2 (nH)	545.9	538.0	102.2	100.0	41.5	47.0
C2 (pF)	183.9	180.0	152.8	150.0	133.9	120.0
L3 (nH)	1500.0	1498.0	1441.8	1456.0	906.2	960.0
C3 (pF)	54.6	56.0	10.8	10.0	6.3	6.2
L4 (nH)	433.9	538.0	78.2	82.0	35.1	39.0
C4 (pF)	214.8	180.0	204.9	180.0	165.8	150.0
L5 (nH)	1332.9	1336.0	1194.4	1198.0	795.9	784.0
C5 (pF)	64.0	68.0	13.3	12.0	7.3	7.5
L6 (nH)	368.4	380.0	69.7	68.0	34.2	33.0
C6 (pF)	235.9	220.0	231.5	220.0	170.2	180.0
L7 (nH)	753.2	737.0	594.6	538.0	383.8	380.0
C7 (pF)	109.5	120.0	27.3	27.0	15.2	15.0

50Ω source and load impedance. We then compared this to the S_{21} calculated using simulation. The TPG for the 50Ω input condition is calculated in GENESYS using both the measured and simulated S_{21}. Figure 5.15 shows the results. Although Channel 1 agrees with the simulation result closely, the other two channels are little bit off from the simulation result. The reason behind this is believed to be due to parasitic reactances in the PCB layout. A similar problem is described in [85], in which the authors intended to implement a multiplexer in approximately the same frequency region (20–90 MHz) using similar (air–core) inductors. They claimed to have solved the problem with the assistance of simulations accounting for board parasitics using the full–wave electromagnetic simulator "Sonet EM" from Sonet Software, Inc[2]. They also used trimmer capacitors to facilitate fine adjustments. We did not try to implement these solutions due to the schedule and funding limitations of our project.

The TPG for the field measurement can be predicted using the measured S_{21} of the multiplexer. The simulated S_{21} is replaced with the measured S_{21}, and the predicted TPG is then calculated using the actual antenna impedance as the source impedance. Figure 5.16 shows the predicted TPG for the field experiment. Figure 5.17 shows the values of γ for various preamplifier noise figures

[2]http://www.sonnetsoftware.com/

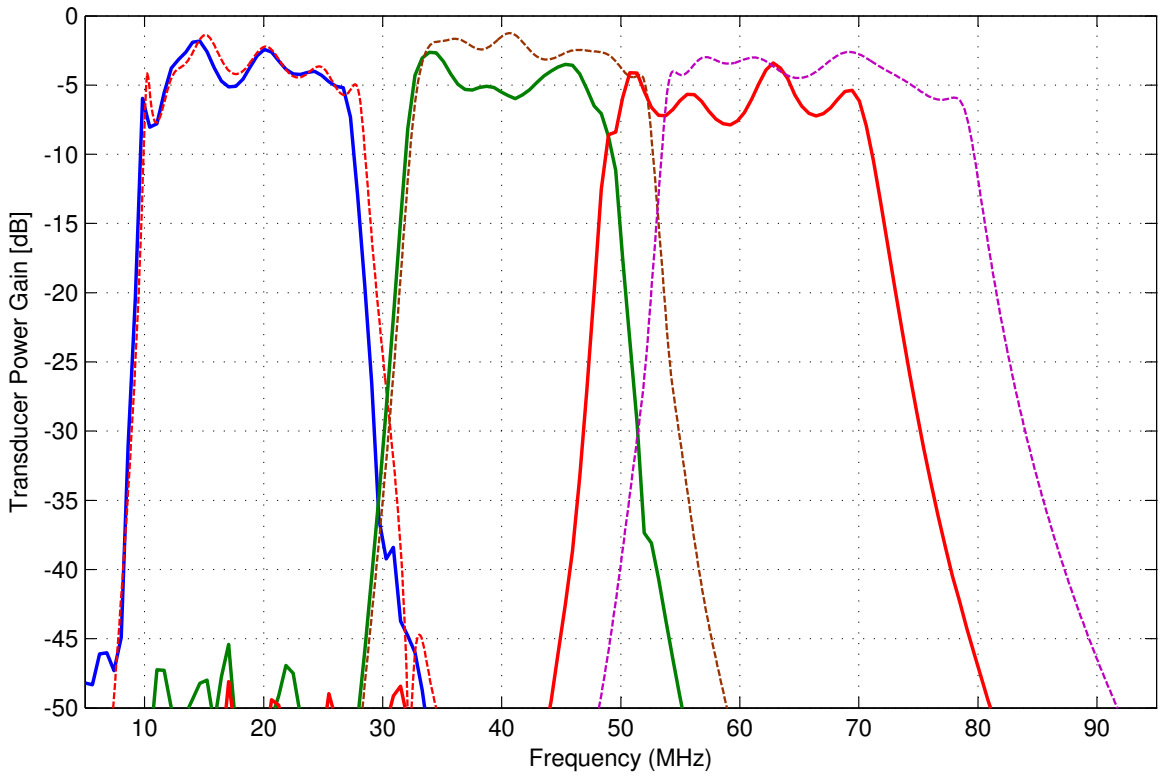


Figure 5.15: Lab measurement of the optimized (standard component values given in Table 5.3) multiplexer assuming 50Ω source and load impedances. Solid lines represent the measurement results and dashed lines are the results from simulation. (Note that this result is not representative of actual performance, since the source impedance is 50Ω as opposed to Z_A). Three channels are measured separately and shown on the same plot.

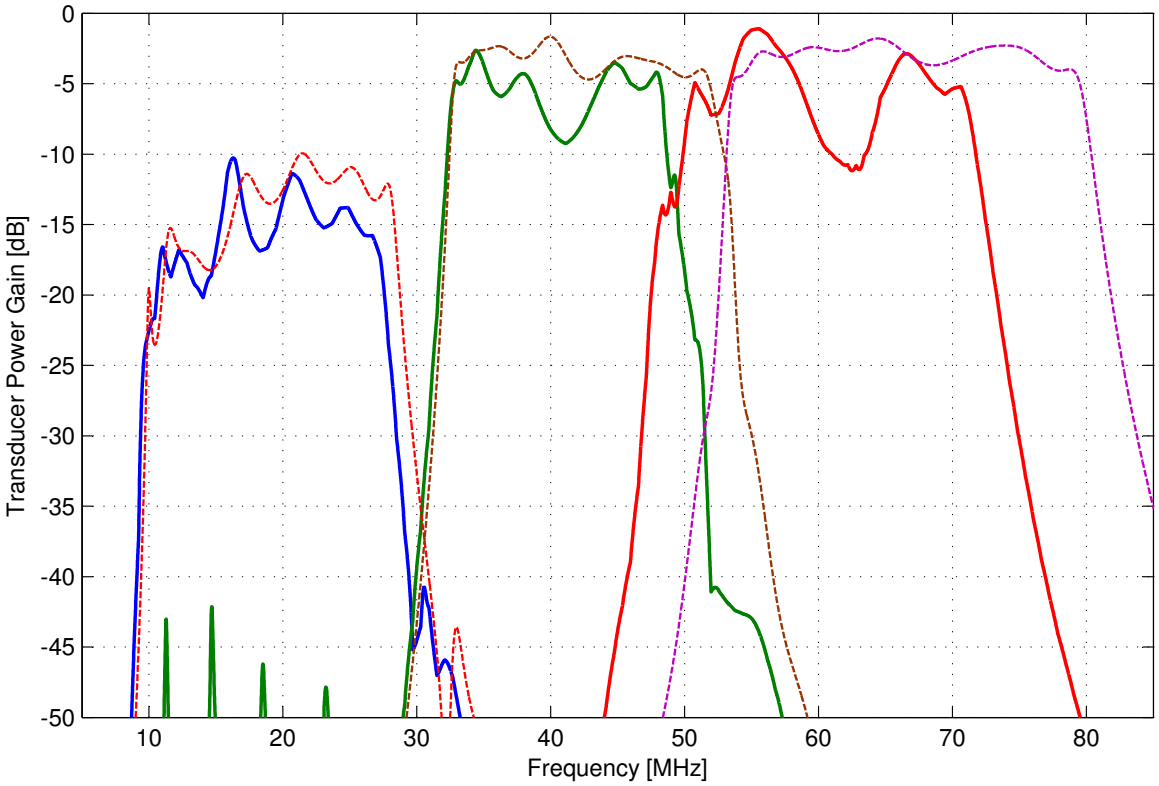


Figure 5.16: Predicted TPG of the optimized multiplexer assuming the simulated antenna impedance as source, and using the S_{21} measurements described in the text. Solid lines represent the resulting TPG and dashed lines represent the same result using S_{21} from the simulation.

such as 2 dB, 3 dB, and 4 dB, assuming Celestial noise as external noise environment. It should be noted that this design still achieves large γ (factor of 5 or so) for the Celestial noise, despite poor TPG for preamplifier noise figure of 3.0 dB. However, the performance degrades compared to the performance shown in Figure 5.13 (from simulation) due to the actual board level implementation difference shown in Figure 5.15.

5.4.3 Experiment Design

This section describes the methodology and theoretical analysis to calculate the performance of the implemented multiplexer from the field measurement results. Figure 5.18 shows a simplified block diagram of our experiment, which consists of an antenna, a multiplexer, and a preamplifier. The output of the preamplifier is measured by a spectrum analyzer having 50Ω input impedance. The

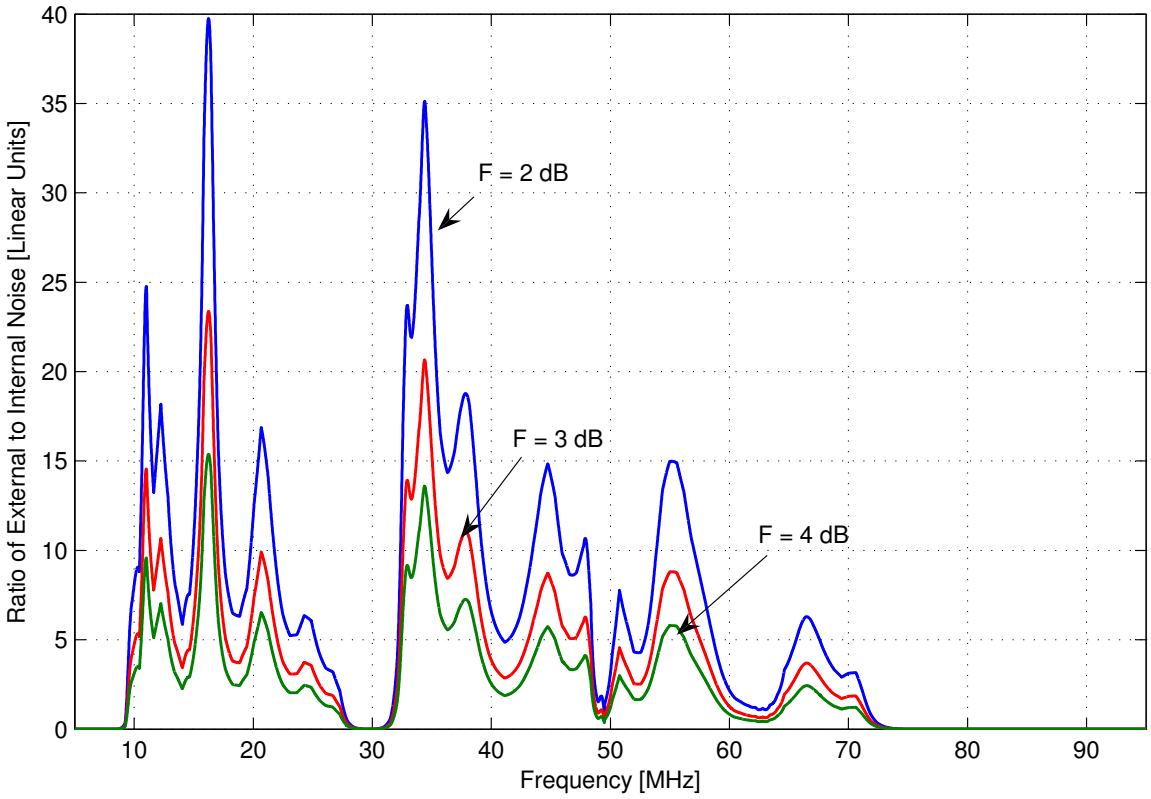


Figure 5.17: Performance (γ) of optimized implemented multiplexer (using standard components) for 2, 3, and 4 dB preamplifier noise figures, assuming simulated impedance of the VHF monopole antenna and Celestial noise as external noise environment, based on the S_{21} measurements described in the text.

antenna is the same antenna described in Chapter 4, and the preamplifier represents the receiver described in Chapter 4.

The PSD at the antenna terminals is

$$S_A = \eta k T_A \tag{5.8}$$

When no multiplexer is used, we have

$$S_{out}^{(1)} = S_A \left(1 - \left|\Gamma_A^{(1)}\right|^2\right) G_P + k T_P G_P \tag{5.9}$$

where $\Gamma_A^{(1)}$ in this case (no multiplexer in Figure 5.18) is Γ_P, i.e., the reflection coefficient at the interface of antenna and the preamplifier, T_P is the noise temperature of the preamplifier, and G_P is the total gain of the preamplifier. An estimate of S_A, the PSD that the antenna delivers to a perfectly matched load, is therefore given by

$$\hat{S}_A = \frac{S_{out}^{(1)} - k T_P G_P}{\left(1 - \left|\Gamma_A^{(1)}\right|^2\right) G_P} \tag{5.10}$$

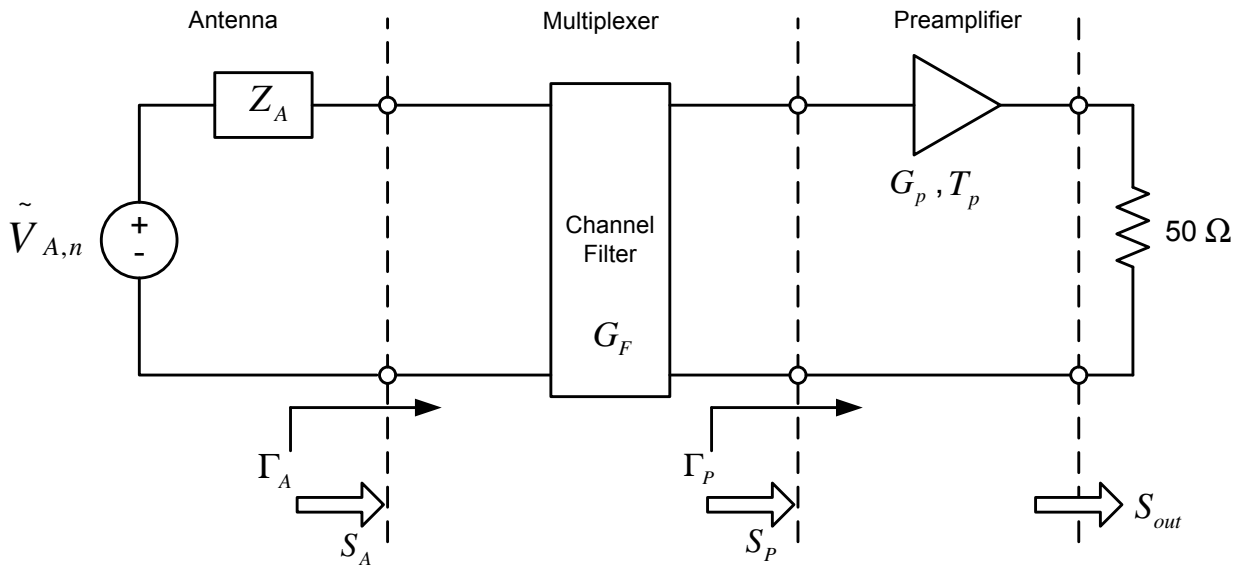


Figure 5.18: Analysis of the experiment used to determine multiplexer channel TPG.

When the multiplexer is included, we have

$$S_{out}^{(2)} = S_P^{(2)} G_P + kT_P G_P \tag{5.11}$$

Now the PSD $S_P^{(2)}$ delivered to the preamplifier by the multiplexer channel under test can be estimated as

$$\hat{S}_P^{(2)} = \frac{S_{out}^{(2)} - kT_P G_P}{G_P} \tag{5.12}$$

Combining Equations 5.10 and 5.12, the TPG of the multiplexer can be calculated from measurements of $S_{out}^{(1)}$ and $S_{out}^{(2)}$ as

$$\text{TPG} = \frac{\hat{S}_P^{(2)}}{\hat{S}_A} = \frac{S_{out}^{(2)} - kT_P G_P}{S_{out}^{(1)} - kT_P G_P} \left(1 - \left|\Gamma_A^{(1)}\right|^2\right) \tag{5.13}$$

5.4.4 Data Collection

Figure 5.19 shows the multiplexer as used during the field measurement. Figure 5.20 shows the integrated $S_{out}^{(2)}$ for all three channels, and $S_{out}^{(1)}$.

5.4.5 Results

From the measurements of $S_{out}^{(1)}$ and $S_{out}^{(2)}$ the TPG for each multiplexer channel is calculated using Equation 5.13, where the value of T_p is obtained from the preamplifier noise figure ($F = 2.9$ dB) calculated in Table 4.3, and G_p can be found from Figure 4.11. Figure 5.21 shows the resulting measured TPG as well as the predicted TPG. Note that some strong RFI is present (especially at lower frequencies) in our measurement data . In our calculation process, we performed window averaging to make the measurement data smooth, thereby reducing the effect of RFI. However, we can get the idea from the Figure 5.21 that the measured performance closely follows the predicted performance.

Note that the measured responses do not roll off sharply at the band edges as the predicted responses do. This is because after the cutoff frequencies of multiplexer filters the receiver becomes dominated by its internal noise instead of external noise.

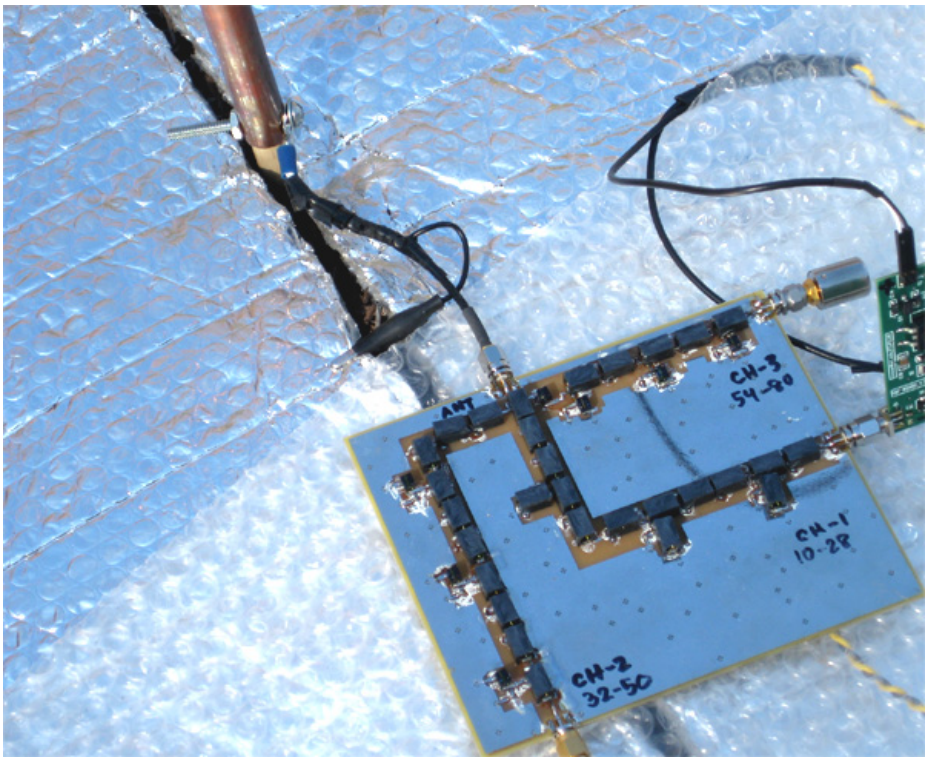


Figure 5.19: The multiplexer in the process of field testing.

Figure 5.22 shows the ratio of the measured and the predicted TPG of the multiplexer. The measured TPG is within approximately ±5 dB for Channel 1, ±3 dB for Channel 2, and ±4 dB for Channel 3, with respect to the predicted TPG. The large and rapidly frequency–varying difference between the predicted and measured TPG for Channel 1 is primarily due to RFI, which has been reduced but not completely eliminated by the averaging described above. Channels 2 and 3 are less affected by this problem, as expected. The mean ratio over each channel is very close to the expected value of unity, with the error being attributable to a combination of differences in the ripple structure in the frequency responses, and incompletely suppressed RFI. This seems to be confirmed by the fact that Channel 2, which contains less RFI compared to the other channels, provides TPG performance close to the predicted TPG compared to the other channels.

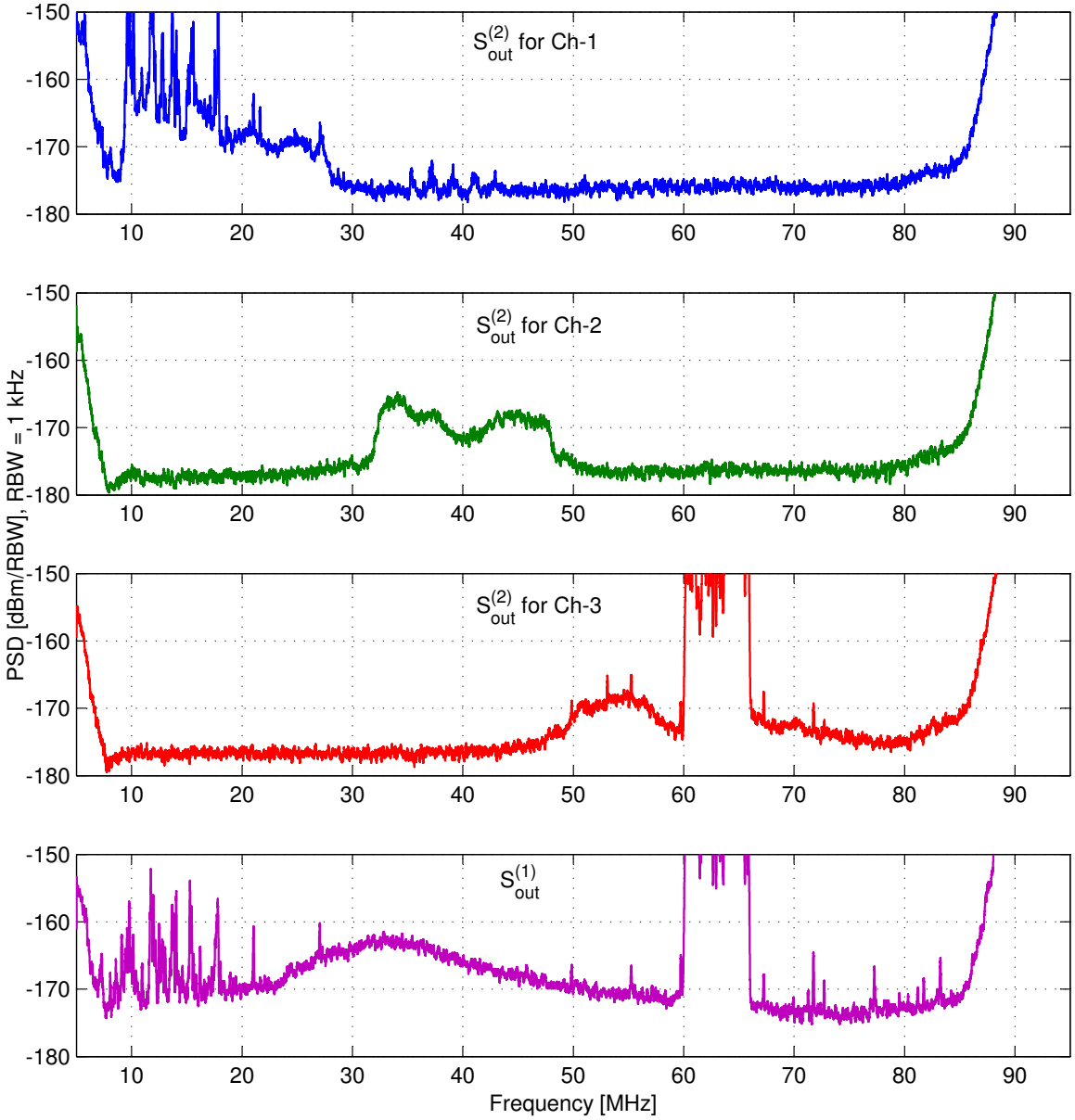


Figure 5.20: Measured integrated PSD for each multiplexer channel, and also without the multiplexer. Integrated over 500 ms with 1 kHz spectral resolution.

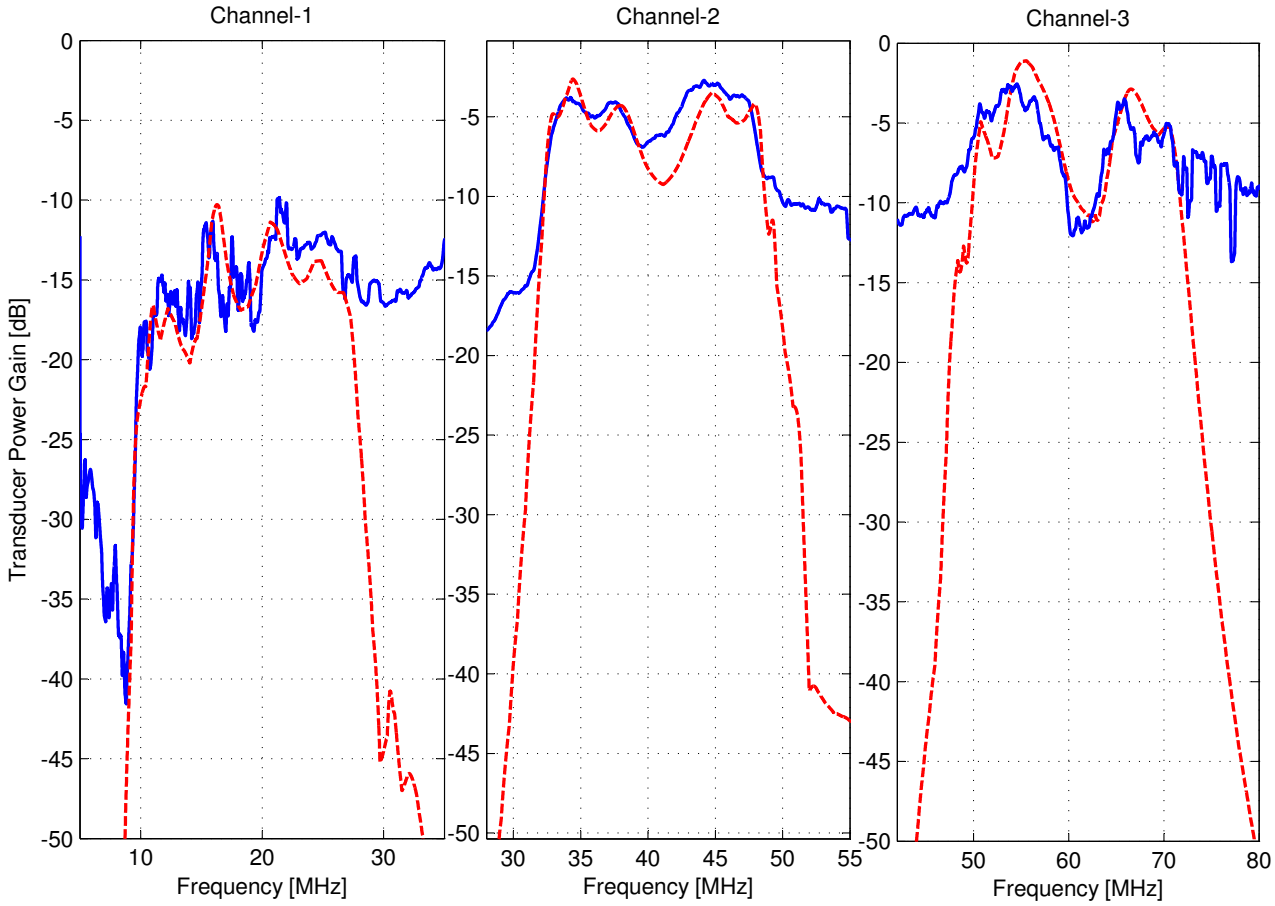


Figure 5.21: Performance (TPG) of the multiplexer as built with standard component values. Solid lines represent the measured TPG from the field experiment and dotted lines represent the predicted TPG based on the S_{21} measurements shown in Figure 5.16.

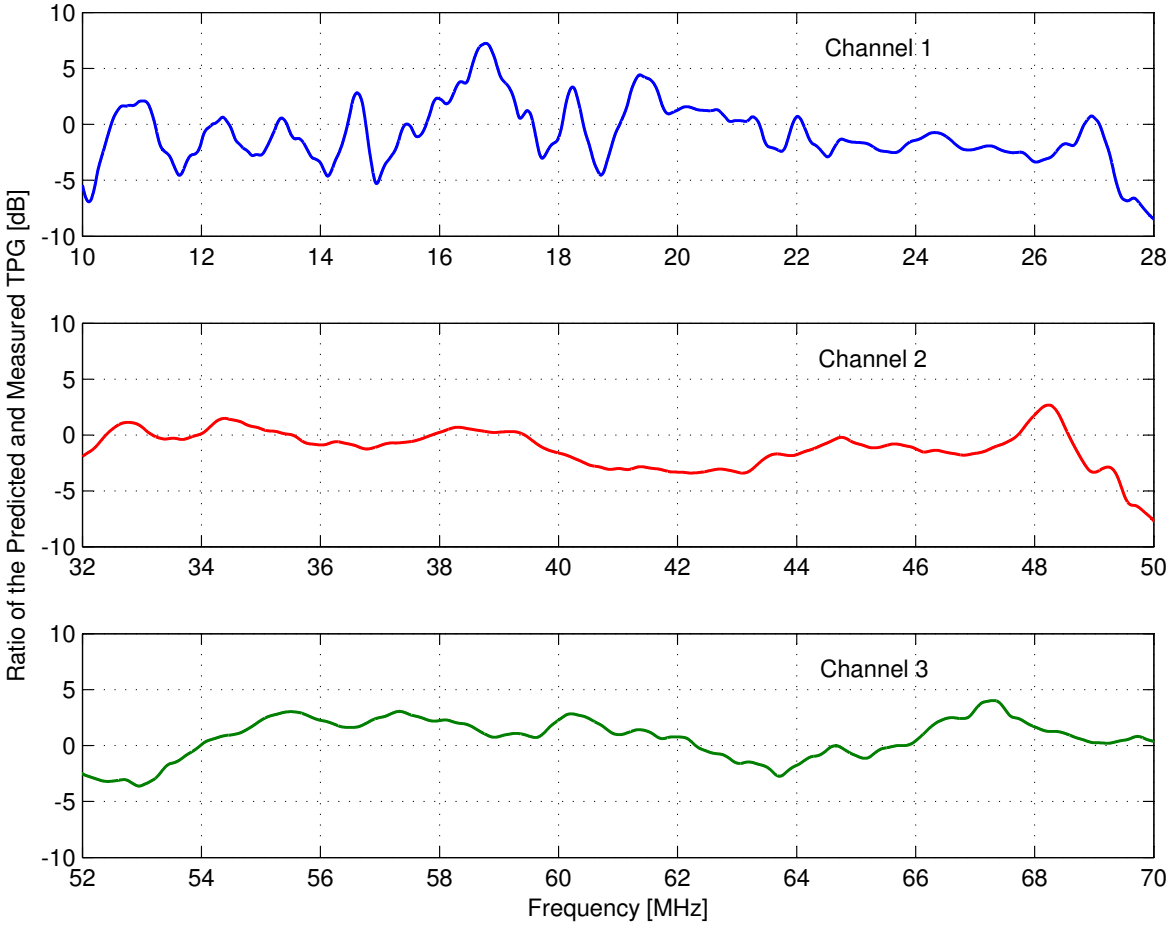


Figure 5.22: Ratio of the predicted to the measured TPG.

5.5 Summary

This chapter presented a multiplexer design methodology emphasizing sensitivity, rather than match efficiency, exploiting the dominance of environmental noise over a receiver's internal noise. We demonstrated the technique by designing and implementing a multiplexer to interface with a VHF monopole antenna for operation in three frequency bands – 10–28 MHz, 32–50 MHz, and 54-80 MHz. It has been shown from the field experiment that the performance (TPG) of the multiplexer follows the predicted performance. Despite poor TPG, the designed multiplexer achieves large γ (factor of 5 or so) in an environment consisting primarily of Celestial (as opposed to man–made) noise environment for a preamplifier noise figure of 3 dB. The ratio γ in environments including significant man–made noise would be much greater. The performance of this multiplexer can be further improved incorporating the parasitic effects (from the PC board) in the design during the board level implementation. Next chapter describes the design of a multiplexer to integrate a MMR receiver with a single antenna to operate at frequencies above 100 MHz.

Chapter 6

Multiplexer Application to a Multiband Multimode Radio

A multiband multimode radio has been designed and developed at Virginia Tech for public safety applications. In this radio, the Motorola RFIC described in Section 7.3 is interfaced with a single monopole antenna using a four channel multiplexer, based on the design concepts of Chapter 5. This chapter presents the design and performance analysis of this multiplexer (the rest of the radio is described in Chapter 7). Initially, this multiplexer is designed for a simple 20 cm monopole antenna of 5 mm radius, to provide a generic example of performance [88]. Section 6.1 ("Multiplexer Design for a Generic Monopole Antenna") presents the design and performance analysis of this multiplexer. Then a multiplexer is designed for a commercially–available monopole antenna 18 cm long and 6 mm diameter. The design and performance analysis of this multiplexer is discussed in Section 6.2 ("Multiplexer Design for a Real Antenna"). Section 6.3 ("Summary") summarizes this chapter.

6.1 Multiplexer Design for a Generic Monopole Antenna

We wish to interface a monopole antenna to separate receiver inputs using the multiplexer architecture and frequency bands shown in Figure 6.1 incorporating the same design procedure described in Chapter 5. Initially, the multiplexer channels are designed for a constant 50Ω termination

impedance using the 5^{th} order Chebyshev topology shown in Figure 6.2.

The starting component values for this design are presented in Table 6.1. The performance of this multiplexer, assuming constant 50Ω antenna impedance, is shown in Figure 6.3. It should be noted that the interaction between the channels is negligible when antenna impedance is assumed to be 50Ω since the multiplexer is designed for constant 50Ω termination impedance and the presence of wide separation between channels.

6.1.1 Optimization

The VT MMR is designed to achieve performance comparable to existing radios, using the same monopole–type antennas already in use. Hence the multiplexer for this radio is designed to accommodate a generic "rod" monopole antenna 20 cm long and 5 mm in radius, the dimensions of which are comparable to antennas used by existing radios. Another reason for considering this antenna first is because we want to explore the performance of our proposed technique using a simple and easy–to–model antenna first, and we will design it for an actual antenna later.

The monopole is modeled in the manner shown in Figure 2.3, as a voltage source in series with an antenna impedance Z_A which is equal to one–half the impedance of corresponding dipole (obtained using image theory) in free space. We obtain a circuit model for Z_A using the TTG method described in Section 2.2. The circuit model and associated impedance are shown in Figure 6.4 and 6.5, respectively. Figure 6.5 also shows the impedance calculated using the method of moments (MoM) for comparison purpose only. Note that both methods of analysis are in reasonable agreement between 100 and 450 MHz. The TTG method resulted in a circuit model that is resonant at 341 MHz, slightly lower than the anticipated resonance of 347 MHz, which was correctly predicted by the MoM. The TTG method produces a radiation resistance of approximately 30Ω at resonance, whereas MoM produces 36Ω at resonance. From this comparison we can conclude that the circuit model attained from the TTG method is a reasonable characterization of the impedance of a dipole or monopole antenna over at least half of our desired range of frequencies (138–862 MHz). In fact the TTG model is suitable for our purposes over the entire range of interest. This is demonstrated by the calculated IME shown in Figure 6.6.

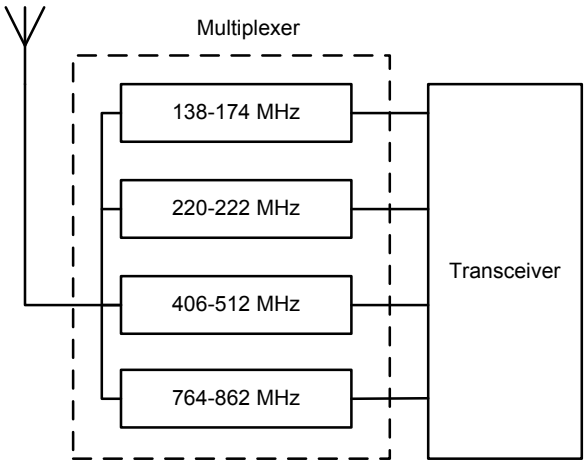


Figure 6.1: Interfacing concept of the multiplexer designed for the VT MMR.

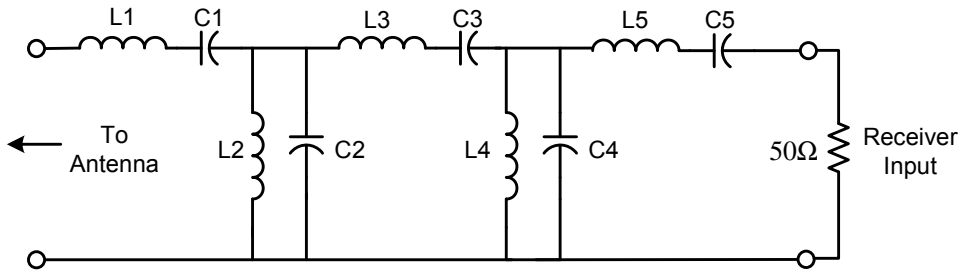


Figure 6.2: Circuit topology of each multiplexer channel in the VT MMR. The inputs of the four channels are connected in parallel.

Table 6.1: Starting (pre–optimization) component values of the multiplexer designed for the VT MMR. Each of the channels are designed for constant 50Ω input and output impedances.

Component	**Channel–1**	**Channel–2**	**Channel–3**	**Channel–4**
L1 (nH)	377.1	1357.4	111.2	114.9
C1 (pF)	2.8	0.4	1.1	0.3
L2 (nH)	9.7	1.3	3.1	0.9
C2 (pF)	108.7	391.4	39.0	42.8
L3 (nH)	561.6	2021.9	173.4	182.0
C3 (pF)	1.9	0.3	0.7	0.2
L4 (nH)	9.7	1.3	3.1	0.9
C4 (pF)	108.7	391.4	39.0	42.8
L5 (nH)	377.1	1357.4	112.2	114.9
C5 (pF)	2.8	0.4	1.1	0.3

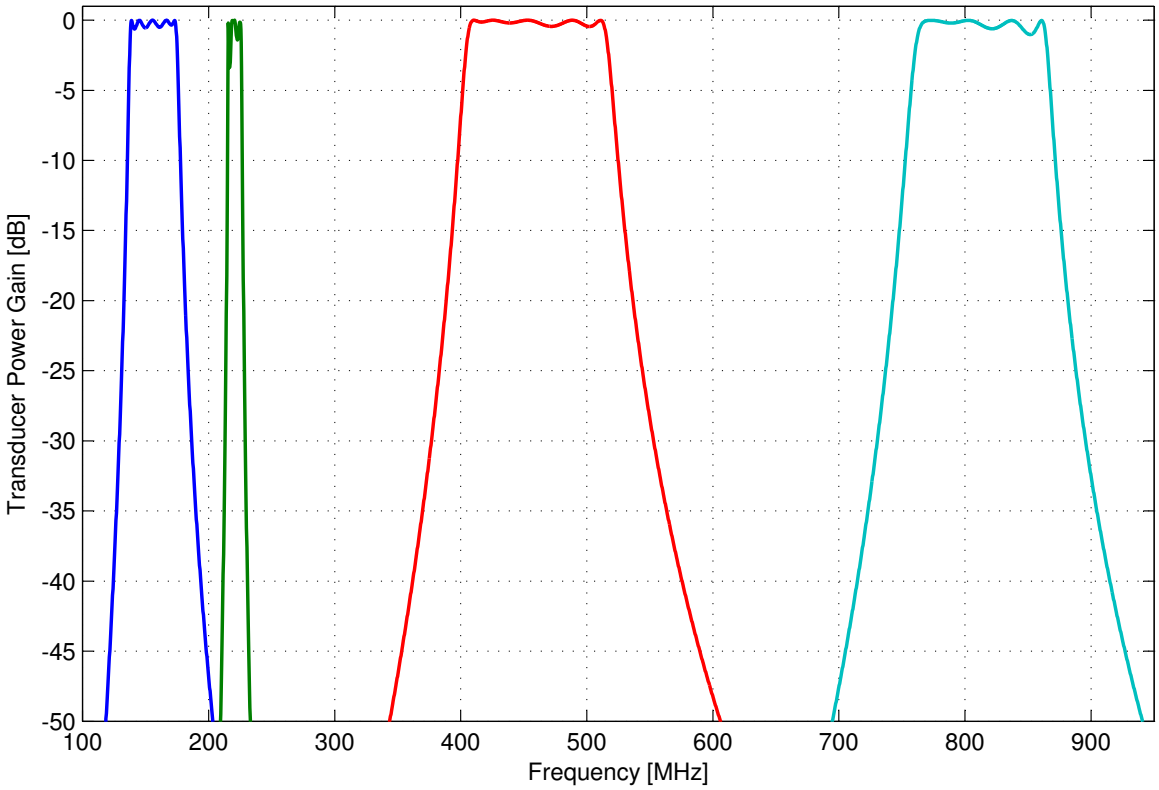


Figure 6.3: Performance (TPG) of initial (50Ω–in, 50Ω–out) multiplexer designed for the VT MMR, assuming constant 50Ω antenna impedance.

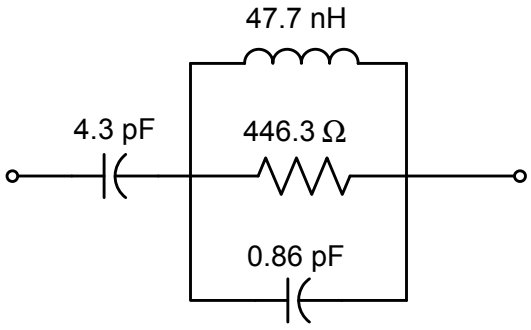


Figure 6.4: Circuit model used to calculate the impedance of generic rod antenna using the TTG model.

Table 6.2: Maximum theoretical TPG calculated from Bode–Fano limit. (n is the order of Chebyshev matching filter).

Parameter	**Channel–1 (138–174 MHz)**	**Channel–2 (220–222 MHz)**	**Channel–3 (406–512 MHz)**	**Channel–4 (764–862 MHz)**
f_0	154.96 MHz	220.99 MHz	455.93 MHz	811.52 MHz
B	23%	0.9%	23%	12%
$Z_A(f_0)$	$4.5 - j194.0\ \Omega$	$9.8 - j101.9\ \Omega$	$66.5 + j77.8\ \Omega$	$446.2 - j41.5\ \Omega$
Series C or L at f_0	5.3 pF	7.1 pF	27.2 nH	4.7 pF
$\lvert\Gamma(f_0)\rvert_{min}$	0.73	≈ 0	≈ 0	≈ 0
TPG ($n = \infty$)	−3.3 dB	≈ 0 dB	≈ 0 dB	≈ 0 dB
TPG ($n = 5$)	−4.3 dB	≈ 0 dB	≈ 0 dB	≈ 0 dB

Figure 6.7 shows the antenna impedance for each multiplexer channel calculated from the series RC and series RL approximation of the monopole antenna. The maximum theoretical TPG calculated from Bode–Fano limit using the series RC and series RL approximations of the impedance of this simulated antenna is shown in Table 6.2. Note that this table contains theoretical TPG for a matching circuit with infinite number of matching sections as well as for a matching circuit with 5^{th} order Chebyshev topology. The multiplexer channels are optimized following the methodology described in Section 5.3. Since the original 5^{th} order Chebyshev filters was designed assuming 0.5 dB ripple, initially ϵ was chosen 0.5 dB for all channels. However, to converge the optimization the values of ϵ were changed to 1 dB, 3 dB, 1 dB, and 1 dB for Channels 1, 2, 3, and 4, respectively. The optimized component values are shown in Table 6.3.

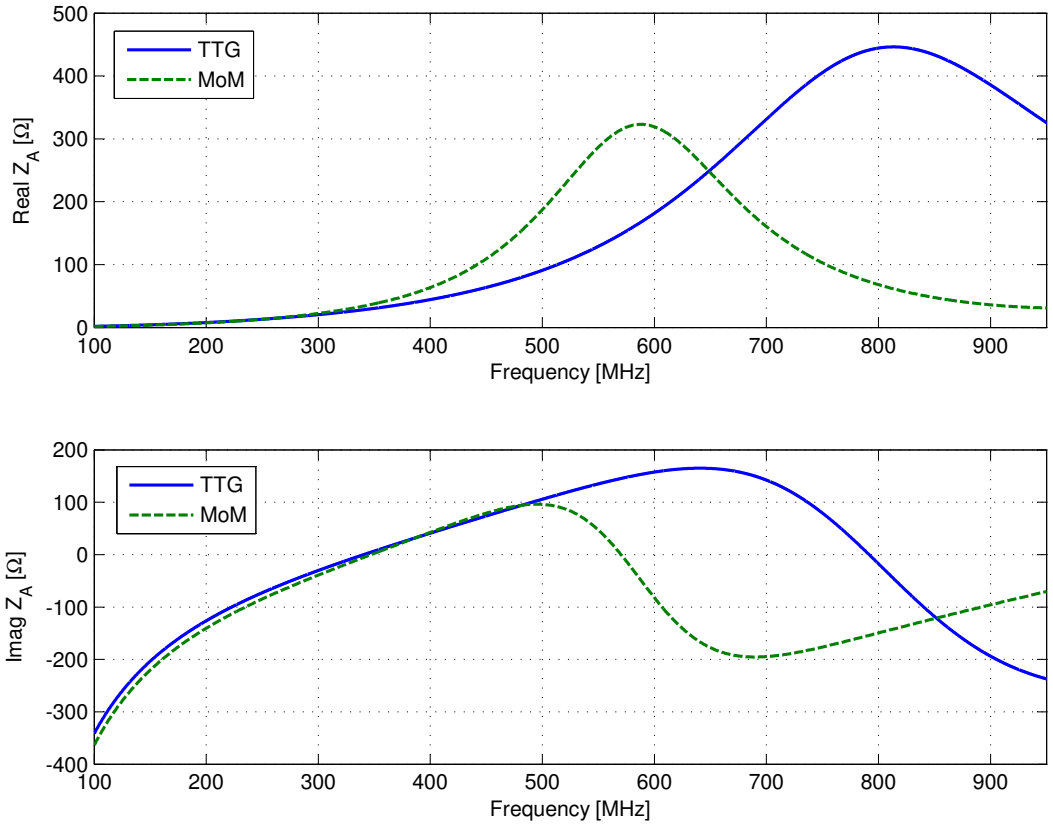


Figure 6.5: Impedance of the generic rod antenna. Solid lines represent the result using TTG model and dotted lines represent the result using the method of moments.

Table 6.3: Component values of the multiplexer optimized for the generic rod antenna (TTG model).

Component	**Channel–1**	**Channel–2**	**Channel–3**	**Channel–4**
L1 (nH)	290.6	1322.5	82.5	81.1
C1 (pF)	6.9	0.4	1.1	0.3
L2 (nH)	7.6	1.3	3.1	0.9
C2 (pF)	136.1	389.4	39.0	42.8
L3 (nH)	402.9	2101.2	173.4	182.0
C3 (pF)	2.6	0.3	0.7	0.2
L4 (nH)	8.3	1.2	3.1	0.9
C4 (pF)	125.1	437.5	39.0	42.8
L5 (nH)	207.2	1301.4	112.2	114.9
C5 (pF)	5.1	0.4	1.1	0.3

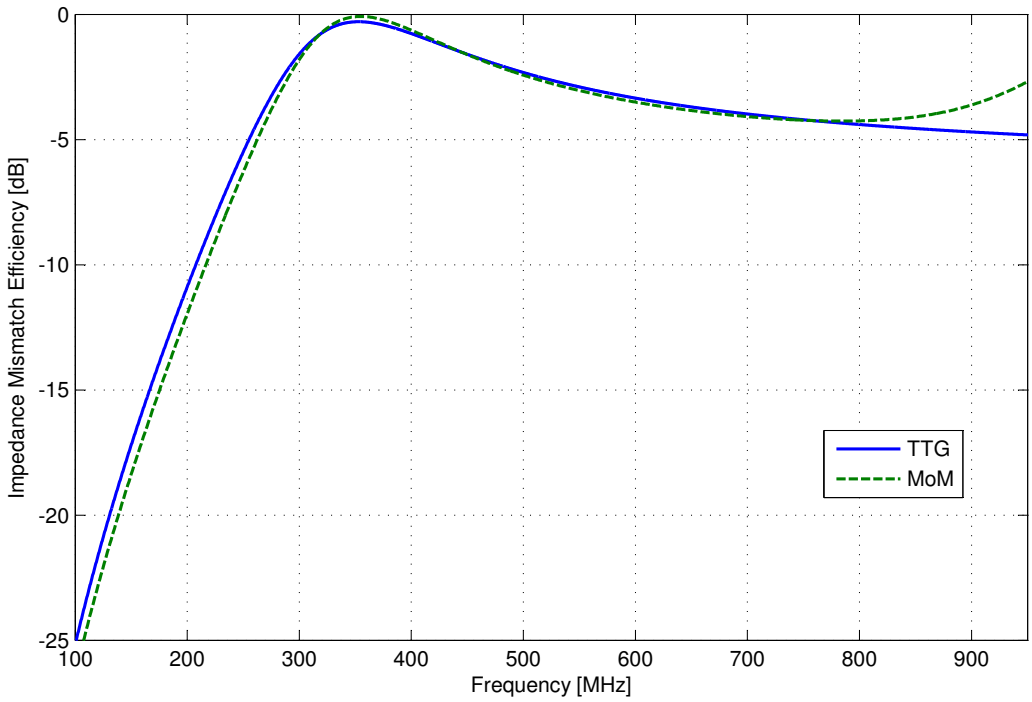


Figure 6.6: Calculated IME between the antenna and a preamplifier with $Z_p = 50\Omega$. The solid line represents the result using the generic rod antenna (TTG circuit model) and the dotted lines represents the result using antenna impedance simulated from the method of moments.

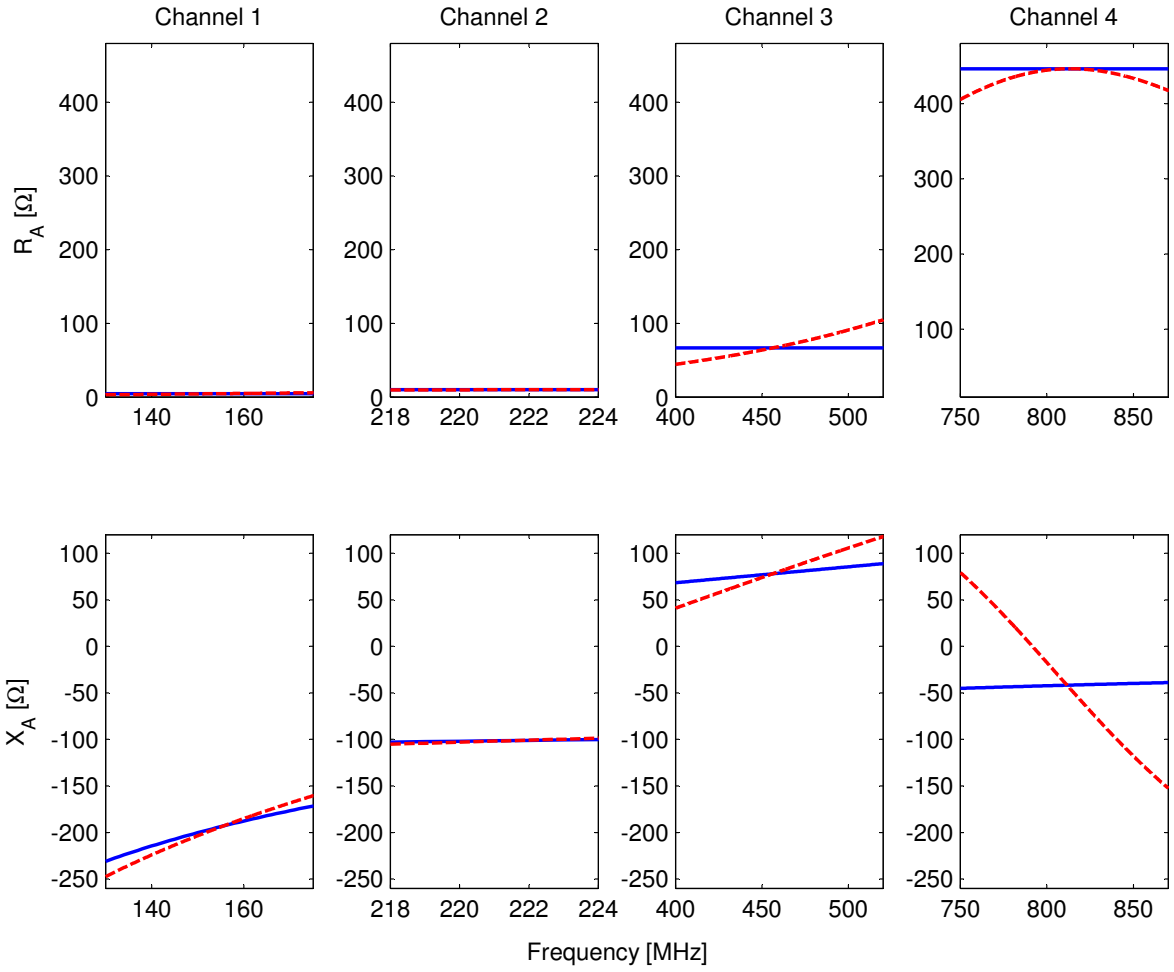


Figure 6.7: Antenna impedance calculated from series RC or series RL approximation of the rod antenna. Solid lines represent the series RC or RL approximation and the dotted lines represent the actual values.

6.1.2 Results

The performance of the optimized multiplexer is shown in Figure 6.8. Channels 1 and 2 achieve approximately flat TPG at –8.2 dB and –1.2 dB, respectively, compared to theoretical TPG of –4.3 dB and ≈ 0 dB, respectively. The shortfalls can be explained by the variation in Z_A with frequency as shown in Figure 6.7; The Bode–Fano bounds calculated using the series RC and RL approximations do not account for this variation. Channels 3 and 4 achieve TPG close to the approximate theoretical value of 0 dB. Figure 6.9 shows the performance expressed in γ (i.e. ratio of external to internal noise) assuming the Celestial noise environment. Note that for Celestial noise in the frequency bands of interest, γ is very poor and internal noise actually dominates the external noise.

A more reasonable scenario for public safety use would be to assume "Residential" or "Business" noise. Figure 6.10 shows the recalculated performance for "Residential" noise environment. This design achieves large γ (factor of 5 or so) in the first two channels, despite poor TPG, for noise figures as high as 2.0 dB. It should be noted that the performance in Figure 6.10 will be even better if we consider "Business" noise envrionment.

Is the performance shown in Figure 6.10 adequate? To answer this question definitively we must consider the actual sensitivity achieved. The PSD of noise at the output of a preamplifier following the multiplexer, referenced to antenna terminals, can be calculated as

$$S_N = k \left[\eta T_A + \frac{T_P}{(\text{TPG})} \right] B. \tag{6.1}$$

This can be interpreted as the $\delta = 1$ sensitivity of the receiver for signal bandwidth of B Hz. Figure 6.11 shows the calculated S_N for "Residential" noise assuming $T_p = 170$ K (2 dB noise figure) attached to each multiplexer output and $B = 12.5$ kHz. Note that the S_N is approximately –123 dBm at the center frequency of first channel (i.e., 155 MHz). As noted in Section 2.3.2, we can obtain an estimate of the 12 dB SINAD sensitivity for analog FM in this case by requiring predetection SNR of 6.5 dB, corresponding to –116.5 dBm at the antenna terminals at 155 MHz. However, this is extremely conservative since the noise in this case is dominated by external noise by a factor of at least 6 dB at this frequency (see Figure 6.10), whereas the SINAD sensitivity

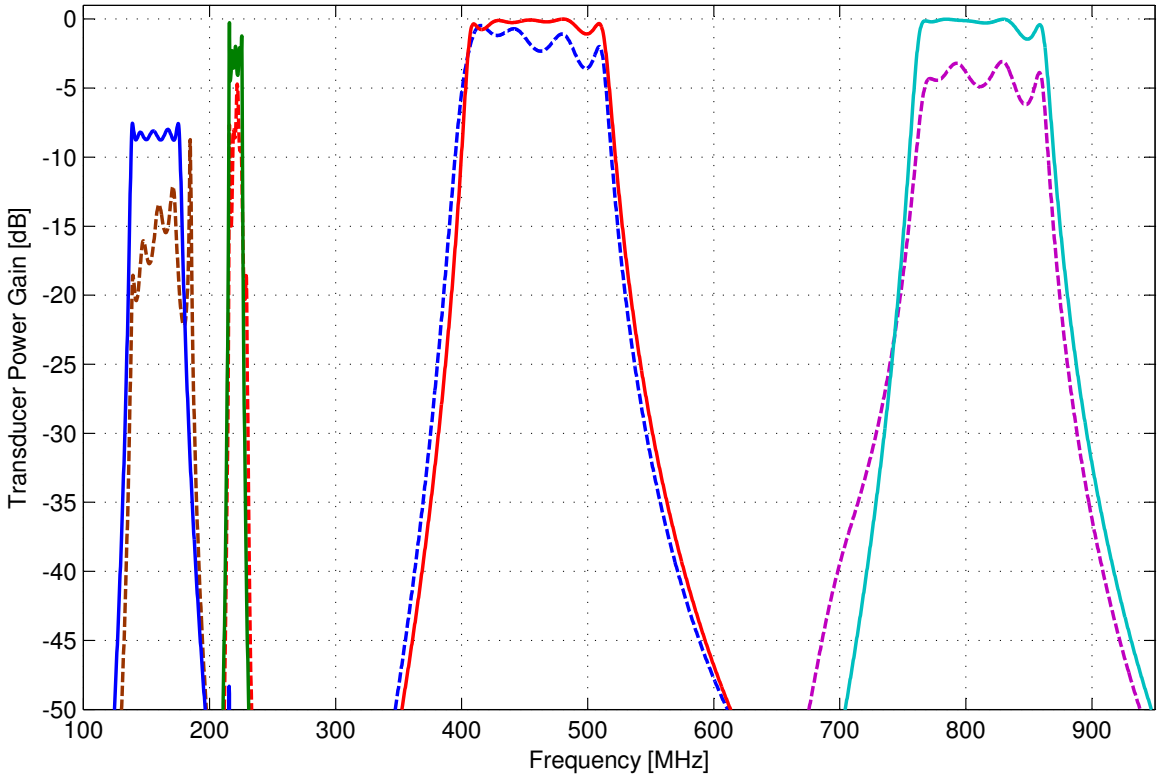


Figure 6.8: Performance (TPG) of the optimized multiplexer designed for the generic rod antenna. Solid lines represent the results after optimization and dotted lines represent the results before optimization.

is with respect to *internal* noise. Since for other channels/frequencies S_N is even lower, we can say that this design conservatively achieves –116.5 dBm or better sensitivity for analog FM with $B = 12.5$ kHz for 12 dB SINAD. Since the corresponding TIA–603 [8] requirement is –116 dBm, we can conclude that the performance of this front end is satisfactory.

6.2 Multiplexer Design for a Real Antenna

We used a low–cost commercially–available monopole antenna, the dimensions of which are very close to the simulated antenna discussed in the previous section, in the actual front–end design for the VT MMR. This is a quarter–wave monopole antenna intended for operation in the 418 MHz

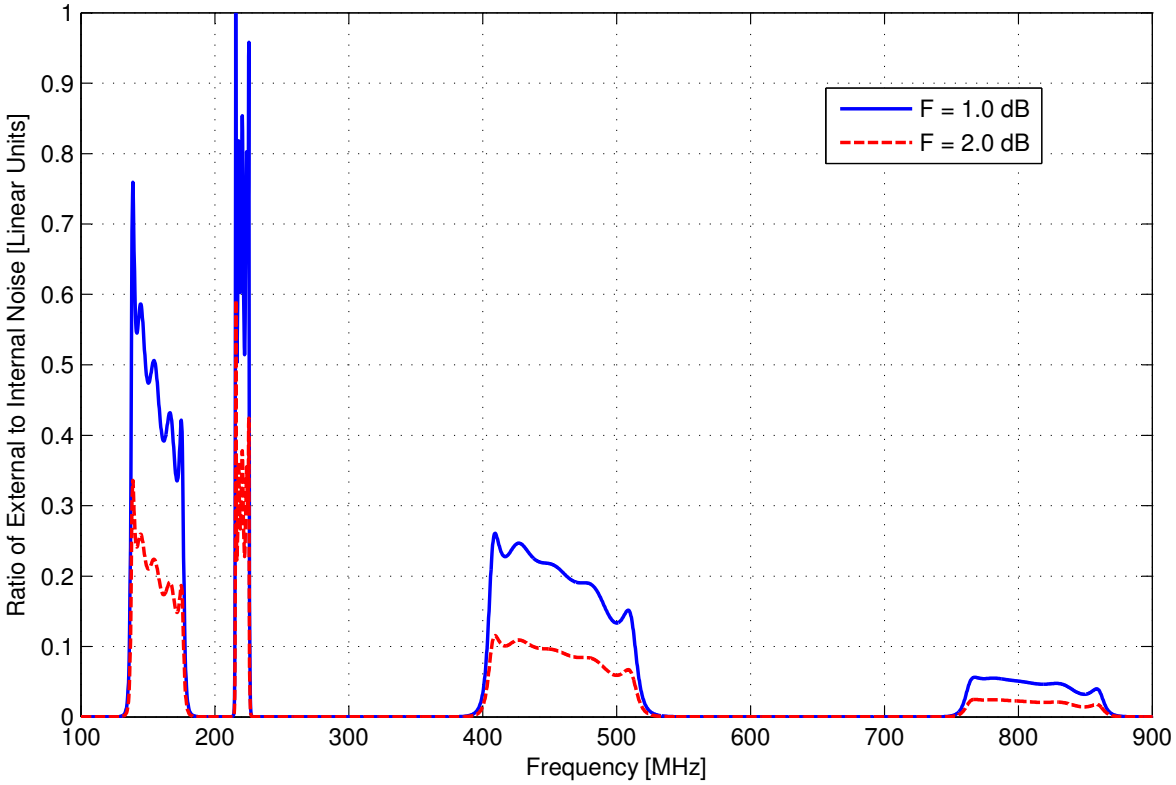


Figure 6.9: Performance (γ) of optimized multiplexer for the generic rod antenna, assuming Celestial noise environment.

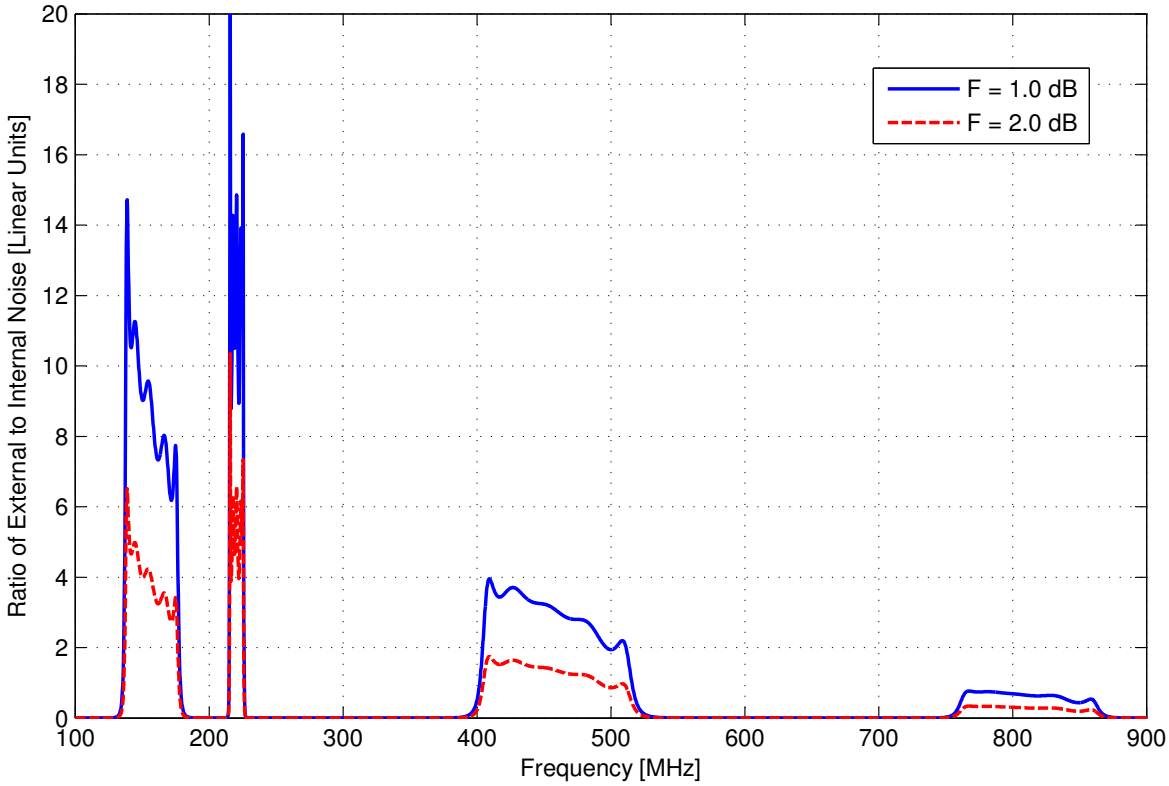


Figure 6.10: Performance (γ) of the optimized multiplexer for the generic rod antenna, assuming "Residential" noise environment.

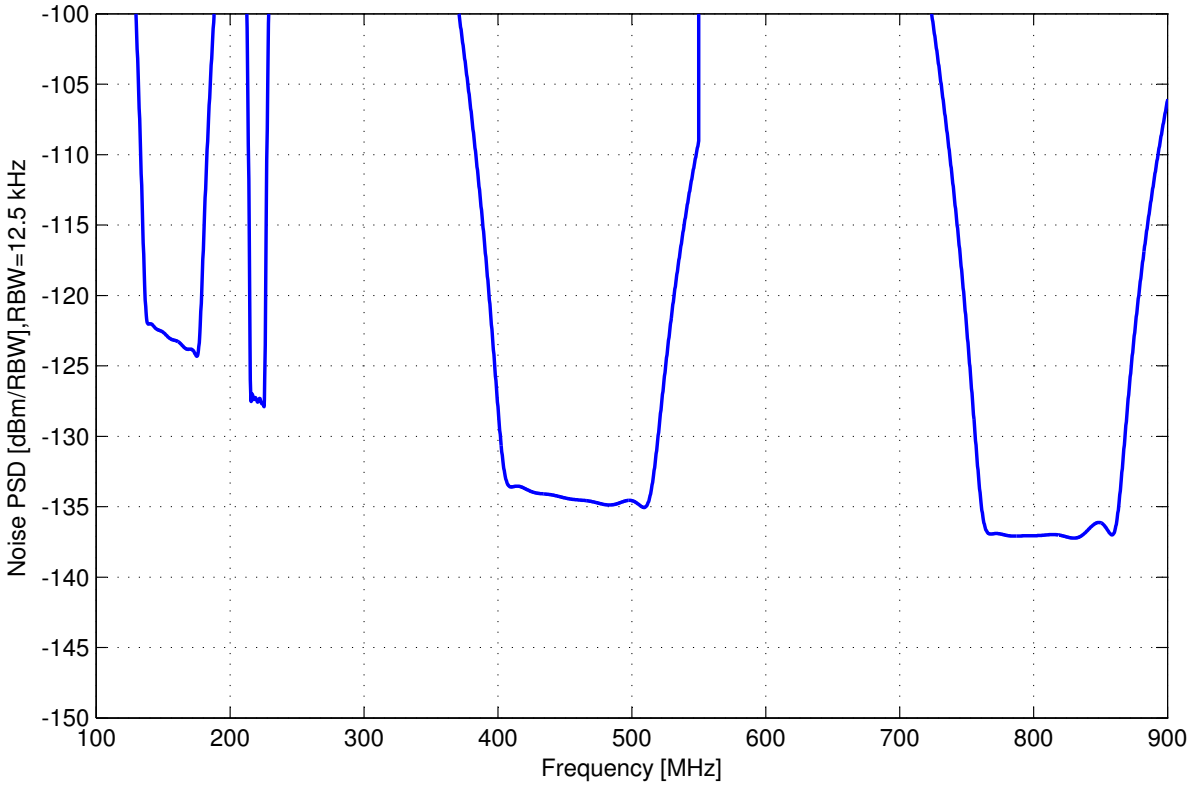


Figure 6.11: Noise PSD at the output of the preamplifier referenced to antenna terminals (rod antenna). Assuming "Residential" noise as external noise source and a preamplifier with 2 dB noise figure.

frequency band, Model ANT-418-CW-QW from Antenna Factor, Inc.[1]. The electrical specifications from the manufacturer are 418 MHz center frequency, typical VSWR < 1.9 at center frequency, 80 MHz bandwidth, and 50Ω impedance. Figure 6.12 shows the exact dimensions of this antenna. The measured impedance and IME are shown in Figures 6.13 and 6.14, respectively. It should be noted that the impedance bandwidth of this commercial antenna is smaller compared to the generic rod antenna described in the previous section. For example, for –3 dB IME the generic rod antenna achieves approximately 282 MHz bandwidth, whereas this commercial antenna achieves approximately 175 MHz. The next section describes the optimization of multiplexer channels for this antenna.

6.2.1 Optimization

The maximum theoretical TPG calculated from the Bode–Fano limit using the series RC and series RL approximations of the impedance of this antenna is shown in Table 6.4. Figure 6.15 shows the antenna impedance calculated from the series RC and series RL approximations of the antenna for each of the multiplexer channel frequency ranges. The maximum theoretical TPG is -1.4 dB for the first channel and approximately 0 dB for other channels. Note that this TPG is calculated for a matching circuit with 5^{th} order Chebyshev topology. Following the methodology described in Section 5.3, multiplexer channels are optimized. Since the original 5^{th} order Chebyshev filters was designed assuming 0.5 dB ripple, initially ϵ was chosen 0.5 dB for all channels. However, to converge the optimization the values of ϵ were changed to 2 dB, 3 dB, 1 dB, and 3 dB for Channels 1, 2, 3, and 4, respectively. Table 6.5 shows the component values after optimization.

6.2.2 Results

The performance of the multiplexer expressed in TPG is shown in Figure 6.16. Channels 1 and 2 achieve approximately flat TPG around –6.5 dB and –2.0 dB, respectively, compared to theoretical maximum TPG of –1.4 dB and ≈ 0 dB, respectively. The Bode-Fano bound calculated using series RC and RL approximation (shown in Figure 6.15) is for center frequency only and do not include

[1] http://www.antennafactor.com

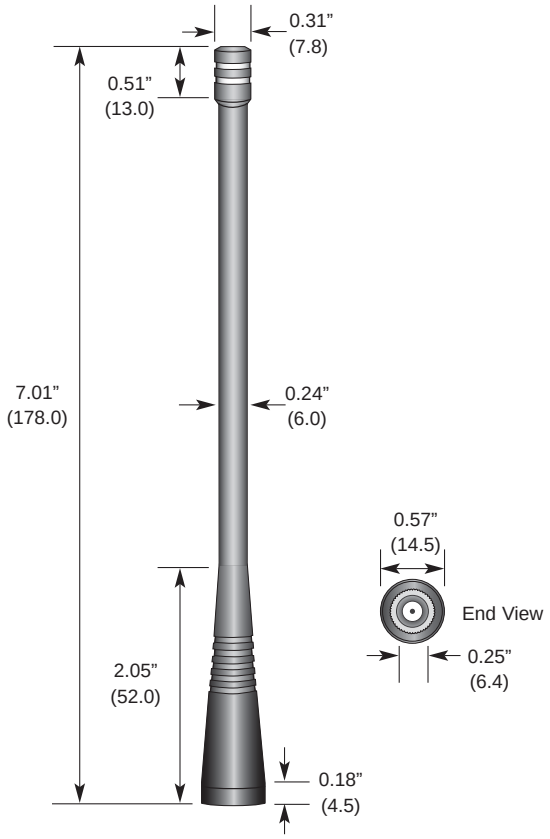


Figure 6.12: The exact dimensions of antenna, Model ANT-418-CW-QW from Antenna Factor, Inc. [89] (used with permission, see Appendix I). Units in parentheses are in mm.

Table 6.4: Maximum theoretical TPG calculated from the Bode–Fano limit. (n is the order of Chebyshev matching filter).

Parameter	**Channel–1 (138–174 MHz)**	**Channel–2 (220–222 MHz)**	**Channel–3 (406–512 MHz)**	**Channel–4 (764–862 MHz)**
f_0	154.96 MHz	220.99 MHz	455.93 MHz	811.52 MHz
B	23%	0.9%	23%	12%
$Z_A(f_0)$	$8.1 - j140.3\ \Omega$	$8.3 - j98.0\ \Omega$	$91.9 + j30.6\ \Omega$	$6.1 - j28.4\ \Omega$
Series C or L at f_0	7.3 pF	7.3 pF	10.7 nH	6.9 pF
$\lvert\Gamma(f_0)\rvert$	0.5	≈ 0	≈ 0	≈ 0
TPG ($n = \infty$)	−1.2 dB	≈ 0 dB	≈ 0 dB	≈ 0 dB
TPG ($n = 5$)	−1.4 dB	≈ 0 dB	≈ 0 dB	≈ 0 dB

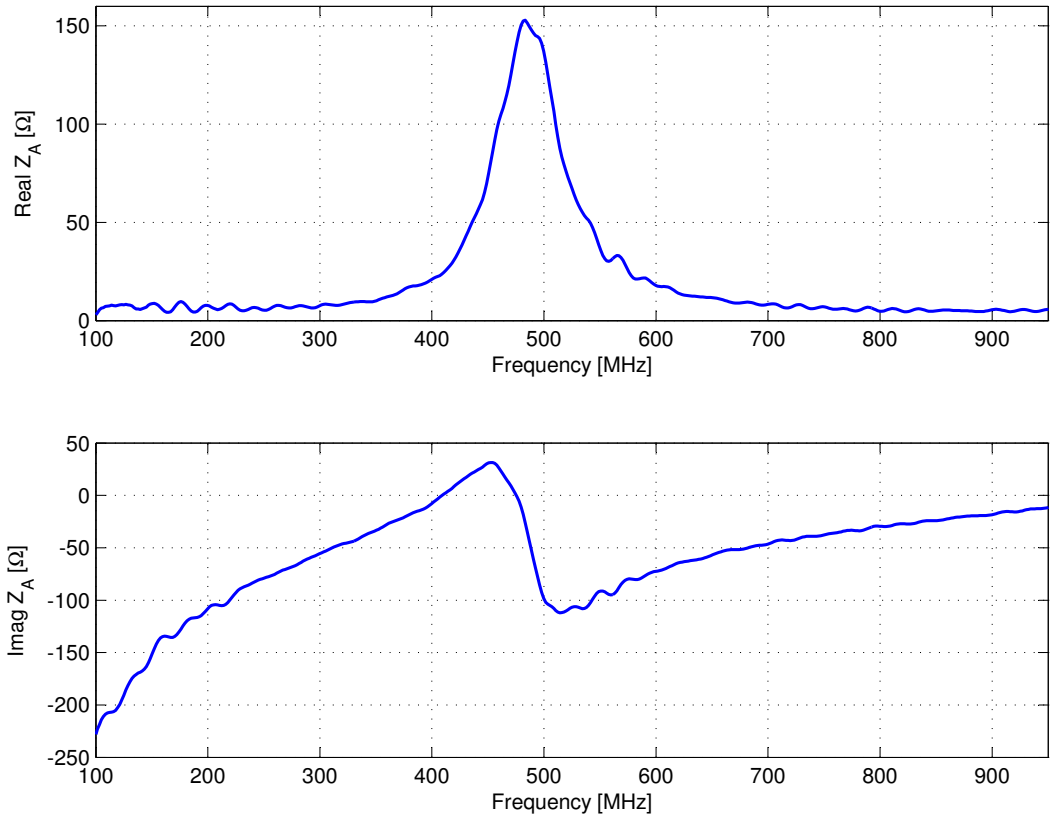


Figure 6.13: Measured impedance of antenna, Model ANT-418-CW-QW from Antenna Factor, Inc.

Table 6.5: Original and nearest standard component values of the multiplexer optimized for the antenna, Model ANT-418-CW-QW from Antenna Factor, Inc.

Component	**Channel–1**		**Channel–2**		**Channel–3**		**Channel–4**	
	Orig.	Std.	Orig.	Std.	Orig.	Std.	Orig.	Std.
L1 (nH)	307.3	306.0	1352.5	1350.0	121.5	120.0	133.5	130.0
C1 (pF)	5.4	5.4	0.4	0.4	1.1	1.1	0.3	0.3
L2 (nH)	7.7	7.8	1.3	1.3	3.2	3.1	1.0	1.2
C2 (pF)	140.0	139.0	404.6	399.0	38.1	39.0	39.1	33.8
L3 (nH)	426.2	426.0	2032.9	2027.0	174.1	175.0	181.5	178.0
C3 (pF)	2.5	2.5	0.3	0.3	0.7	0.7	0.2	0.2
L4 (nH)	9.1	9.0	1.3	1.3	3.1	3.1	1.0	1.2
C4 (pF)	117.5	118.0	393.1	393.0	38.9	39.0	37.7	33.7
L5 (nH)	246.1	246.0	1379.4	1380.0	110.7	110.0	107.9	105.6
C5 (pF)	4.3	4.3	0.4	0.4	1.1	1.1	0.4	0.4

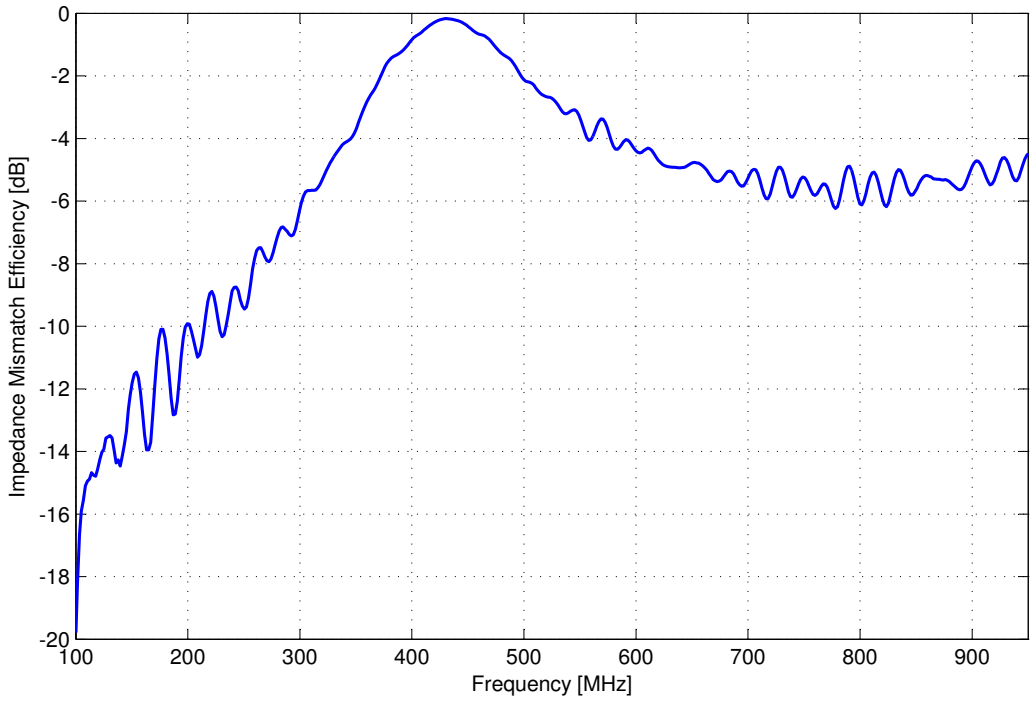


Figure 6.14: Calculated IME between the antenna, Model ANT-418-CW-QW from Antenna Factor, Inc., and a preamplifier with $Z_p = 50\Omega$ using the measured antenna impedance.

any frequency variation. This might be the reason behind the TPG difference mentioned above. On the other hand, Channel 3 achieved TPG of –1 dB, which is close to the approximate theoretical value of $\approx$ 0 dB. On the other hand, Channel 4 achieved –5.5 dB compared to the theoretical value of $\approx$ 0 dB. However, this degradation of TPG does not have that much effect on the overall sensitivity for this channel. This can be explained using Figures 6.11 and 6.19. As we notice from the figures that for this antenna the S_N calculated at the center frequency of the Channel 4 (i.e., 811 MHz) is increased to –134.5 dBm compared to the previous value of –136.5 dBm. So the degradation of TPG actually makes the sensitivity worse only by 2 dB.

Figure 6.17 shows the performance expressed in γ for Celestial noise environment. γ is very poor and internal noise actually dominates the external noise in this case. Figure 6.18 shows the same analysis for "Residential" noise. In this case we achieve large γ (factor of 5 or so) in the first two channels, despite poor TPG, for preamplifier noise figure as high as 2.0 dB. Channel 3 and 4 are clearly not external noise–dominated in this case. It should be noted that the TPG for the fourth channel is poor compared to the TPG calculated for the generic rod antenna. The reason

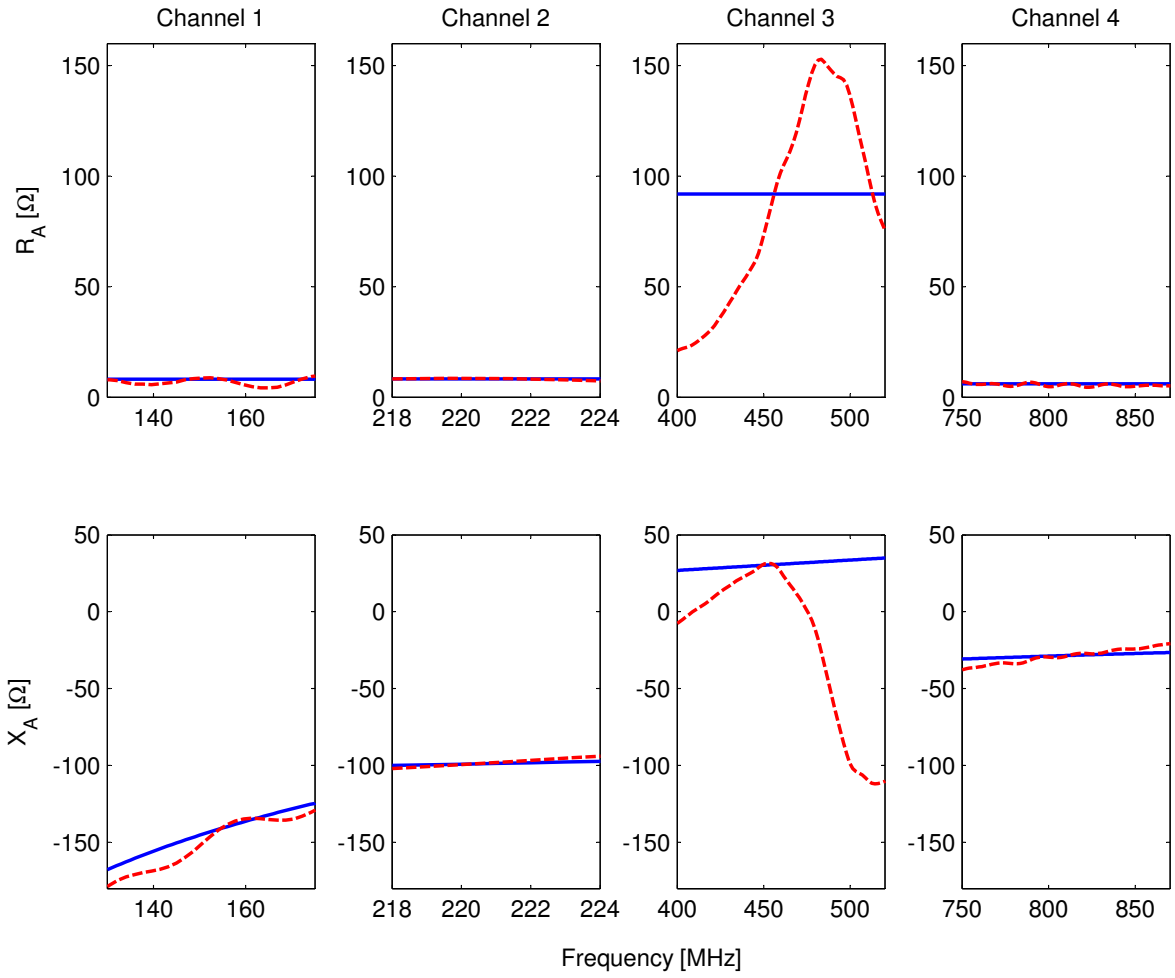


Figure 6.15: Antenna impedance calculated from series RC or series RL approximation of the ANT-418-CW-QW. Solid lines represent the approximation and dotted lines represent the actual values.

behind this might be the smaller impedance bandwidth of this antenna compared to the generic rod antenna.

To assess whether this performance is adequate in the public safety application, Figure 6.19 shows the PSD of total noise at the output of a preamplifier with 2 dB noise figure referenced to the antenna terminals (i.e., S_N) with $B = 12.5$ kHz. Note that the S_N is approximately –123.5 dBm at the center frequency of the first channel (i.e., 155 MHz). We can obtain an estimate of the 12 dB SINAD sensitivity for analog FM in this case by requiring predetection SNR of 6.5 dB, corresponding to –117.0 dBm at the antenna terminals at 155 MHz. However, this is extremely conservative since the noise in this case is dominated by external noise by a factor of at least 7 dB at this frequency (see Figure 6.18), whereas the SINAD sensitivity is with respect to *internal* noise. Since for other channels/frequencies S_N is even lower, we can say that this design achieved –117.0 dBm or better sensitivity (typical value is –116 dBm [8]) for analog FM with $B = 12.5$ kHz for 12 dB SINAD. As a result we can conclude that the performance of this front end is satisfactory.

6.2.3 Implementation and Lab Results

This multiplexer was designed and fabricated as a four–layer printed circuit board (PCB), the details of which are presented in Appendix E. (The assembled multiplexer board is shown in Figure 7.13.) The S_{21} parameter of each of the channels using 50Ω termination was measured and compared with the S_{21} calculated from the simulation results using the same termination (instead of antenna impedance). Figure 6.20 shows the results assuming 50Ω source and load impedance. The performance of the implemented multiplexer is worse (especially Channels 2–4) compared to the simulated performance. In particular the performance of Channel 4 is completely unacceptable. This is mainly for two reasons: (1) Due to the parasitic effects from the PCB layout, and (2) Because suitable standard components are not available. In our application inductors with high Q (100 or higher) and high series resonant frequency (SRF) (higher than 1 GHz) are needed. Similarly it is desired to have capacitors with high Q (10,000 or higher) and low equivalent series resistance (ESR) (possibly 0Ω). However, "Q" of the inductors we used are between 12 to 25, and many of them has SRF below 700 MHz (the frequency of which falls into our desired frequency bands). On the other hand, Q of the capacitors we used in the range of 100 to 1000, and ESR is in the range

of 0.2 to 0.5 Ω.

As we mentioned in the previous chapter, this problem might be improved by including the effects of board parasitics (from PCB) during the simulation of this multiplexer. Moreover, trimmer capacitors can be used to perform fine adjustments to the components. Since the frequency range of channel 4 is close to GHz range, we might consider using microstrip type of design to implement this channel. So the combination of using microstrip and passive components can be an alternative approach for implementing this multiplexer. However, due to schedule and funding limitations we did not able to experiment with this.

We were unable to obtain TPG from the S_{21} results shown in Figure 6.20, because the S_{21} measurement were scalar (magnitude–only) opposed to coherent (magnitude and phase). We were also unable to make a validating field measurement using Celestial noise, as Celestial noise is far too weak in this frequency regime to be detectable using the simple equipment available in Chapter 4 and 5. Thus, the best estimate of "bottom line" performance for this antenna–multiplexer combination, assuming suitable components can be found, is as shown in Figures 6.16–6.18.

6.3 Summary

This chapter described the design of two multiplexers for application in public safety MMR as discussed in Section 1.2. The first multiplexer was designed for a generic rod antenna. The TPG performance of this multiplexer closely follows the theoretical (approximate series RC/RL based) Bode–Fano limit. The second multiplexer was designed for an actual commercial monopole antenna of similar length and radius. Although the TPG performance of this multiplexer is not as good as the previous one (especially Channel 4), this has only a slight effect (less than 2 dB degradation) on sensitivity. In both cases γ (i.e., the ratio of external noise to internal noise) is a factor of 5 or so, and sensitivity is –116.5 dBm or better (for B = 12.5 kHz and 12 dB SINAD) for a preamplifier noise figure of 2 dB. Although simulation results indicate satisfactory performance for all four channels, due to the parasitic effects of the PC board and lack of suitable components, the constructed multiplexer does not exhibit acceptable performance.

A complete description of the VT MMR is provided in the next chapter.

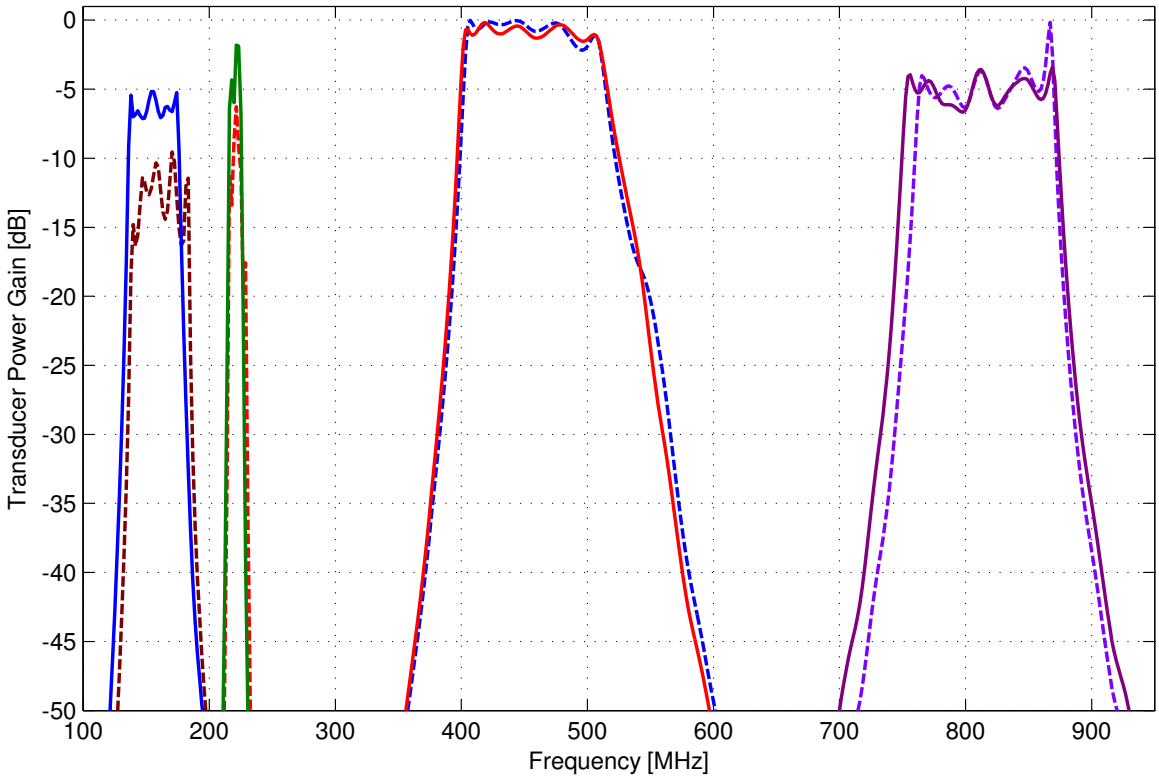


Figure 6.16: Performance (TPG) of the optimized multiplexer (using standard component values) designed for the ANT-418-CW-QW. Solid lines represent the results after optimization and dotted lines represent the results before optimization.

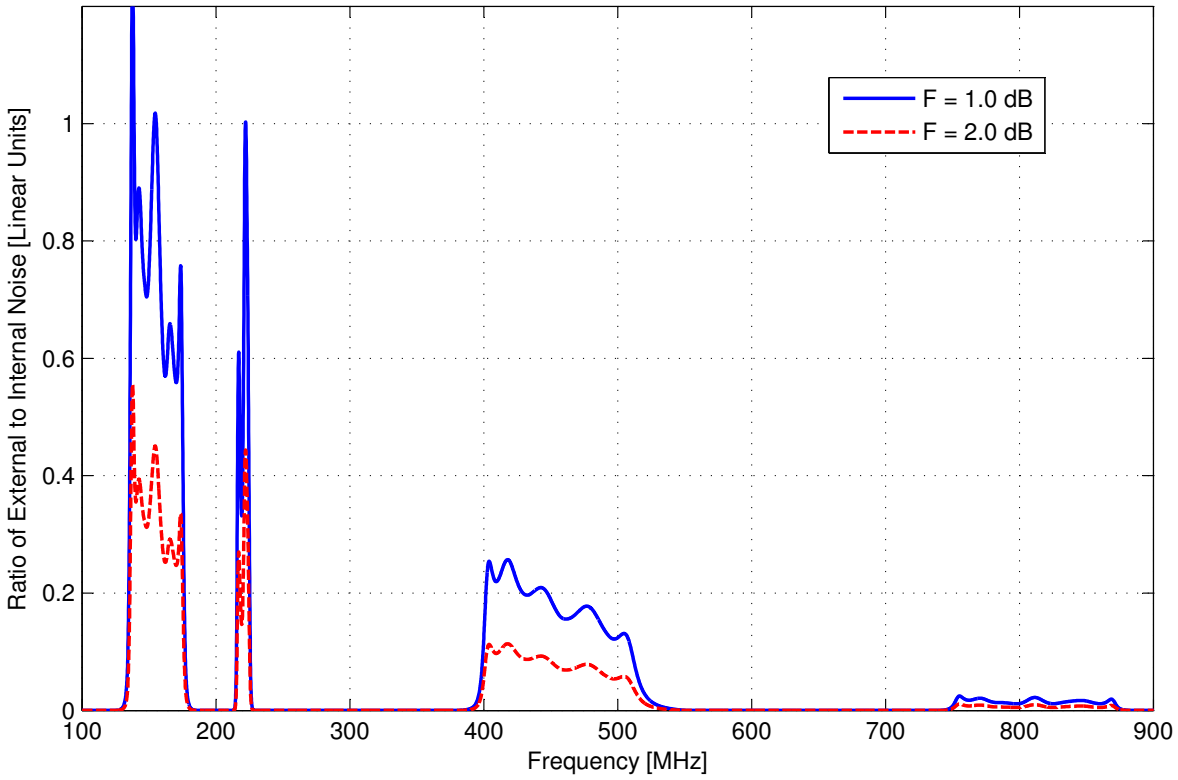


Figure 6.17: Performance (γ) of optimized multiplexer (using standard component values) for the ANT-418-CW-QW, assuming Celestial noise environment only.

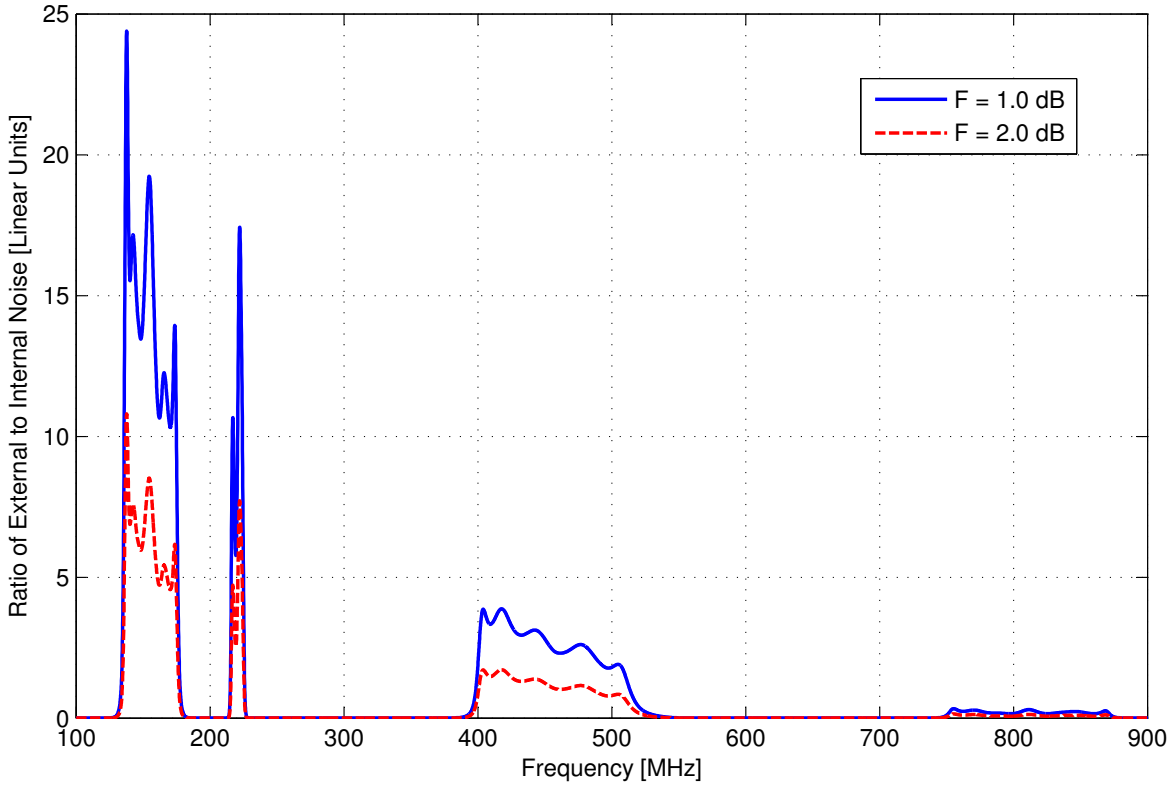


Figure 6.18: Performance (γ) of optimized multiplexer (using standard component values) for the ANT-418-CW-QW, assuming "Residential" noise environment.

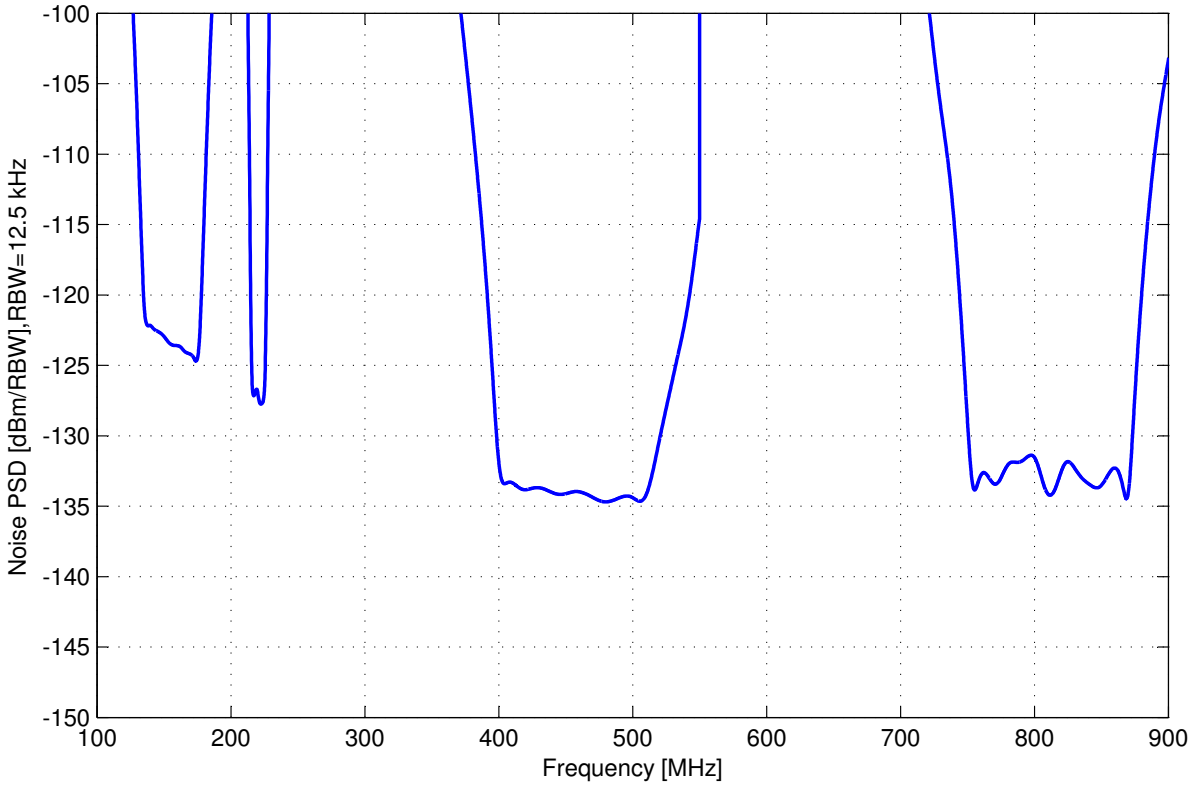


Figure 6.19: Noise PSD at the output of the preamplifier referenced to antenna ANT-418-CW-QW terminals assuming "Residential" noise environment and a preamplifier with 2 dB noise figure. Using standard component values in the multiplexer.

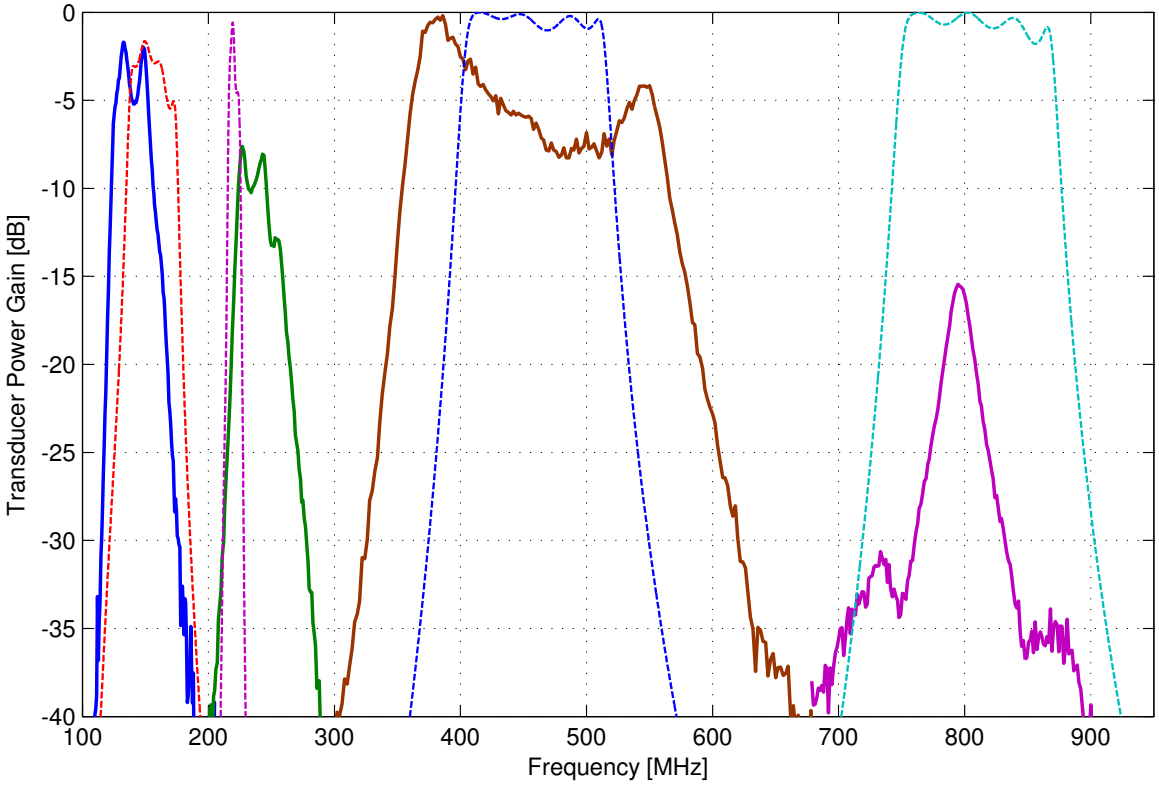


Figure 6.20: Lab measurement of the optimized (using standard component values given in Table 6.5) multiplexer designed for the ANT-418-CW-QW, using instead 50Ω source and load impedances. Solid lines represent the measurement results and dashed lines are the results from simulation. (Note that this result is not representative of actual performance, since the source impedance is 50Ω as opposed to Z_A).

Chapter 7

Design & Development of a Multiband Multimode Radio

This chapter presents the design and development of a MMR for public safety applications, which provides the opportunity to demonstrate the sensitivity–constrained RF multiplexer design concept (Sections 5.3 and 6.2) using direct conversion architecture (Section 2.4.3). Figure 7.1 shows the VT MMR prototype. This chapter is organized as follows. Section 7.1 ("Overview of the Project") presents a brief overview of the VT MMR project. An early design concept for this radio is presented in Section 7.2 ("Original Superhet Architecture"). Then the availability of a CMOS–based direct conversion RFIC motivated us to modify the architecture. An overview and performance analysis of this RFIC is presented in Section 7.3 ("Motorola RFIC: Description & Performance Analysis"). Section 7.4 ("Direct Conversion Architecture") describes the architecture developed using the new RFIC. A description of the developed prototype is presented in Section 7.5 ("Prototype Design"). This chapter is summarized in Section 7.6 ("Summary").

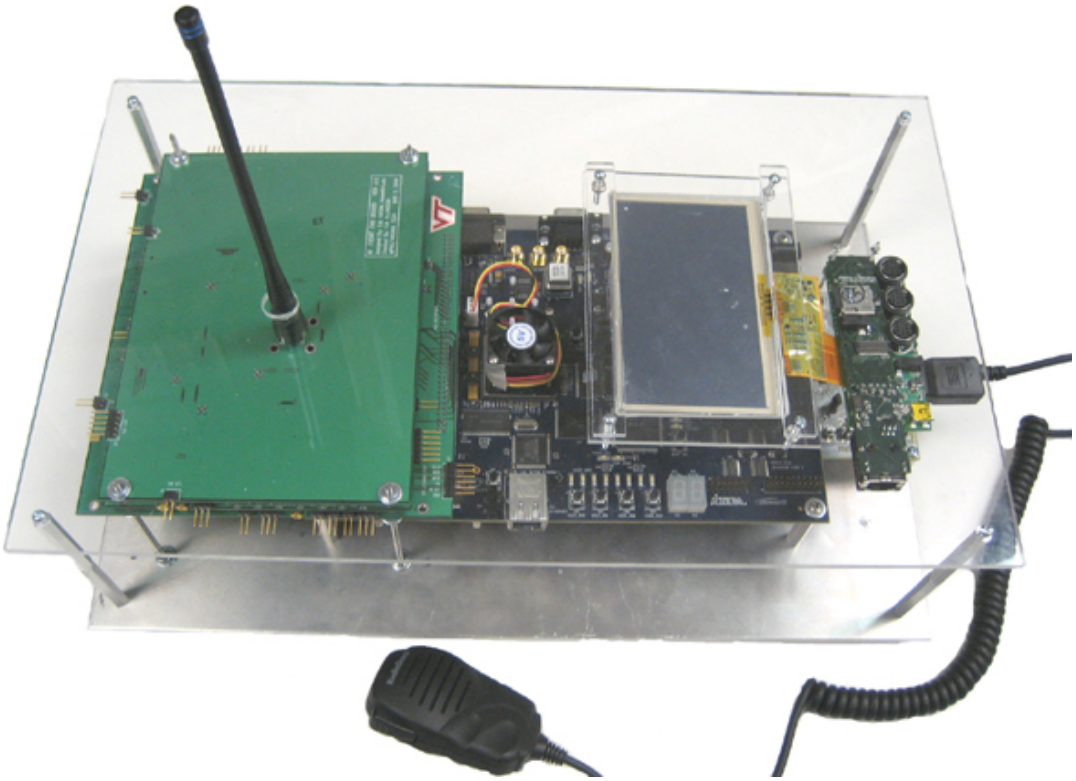


Figure 7.1: VT MMR prototype.

7.1 Overview of the Project

At Virginia Tech, we are working to develop a MMR to solve the interoperability issues among the public safety organizations[1]. This issue has already been discussed in Section 1.2 ("Application Example: Public Safety"). We are working to develop a radio which would be able to communicate in any public safety radio system, immediately and without prior technical coordination. This research is part of a project sponsored by the U.S. Department of Justice [90, 91].

The goal of the VT MMR project is to develop and demonstrate a single radio which can operate in the frequency bands shown in Table 1.1 using any mode; and be able to operate on multiple frequency bands simultaneously. It should be noted that following guidance from the sponsor, it was decided to limit the frequency range of interest to bands above 100 MHz; i.e., not to include the VHF low band (25–50 MHz). Also, for reasons to be discussed in Section 7.2, we decided to focus our attention on bands below 1 GHz. Thus, the total frequency range of interest is from 138 MHz to 862 MHz.

Table 7.1 shows the sensitivity requirement from the standards document TIA–603 [8] for analog FM communication below 1 GHz. It also shows for comparison the performance of the final VT MMR (Section 7.5) as well as the performance of other currently available MMRs with similar design goals.

7.2 Original Superhet Architecture

Figure 7.2 shows the initial strawman design of the VT MMR, which was a more traditional design based on the "divide–and–conquer" superhet architecture. It is noticeable from Table 1.1 that the spectrum used for public safety applications below 1 GHz is relatively concentrated into just a few, relatively narrow but contiguous "chunks" of spectrum; namely "VHF" (138–174 and 220–222 MHz), "UHF" (406–512 MHz), and the 700 MHz and 800 MHz bands. Bands above 1 GHz do not use the same narrowband voice modes prevalent below 1 GHz, but rather use cellular protocols (around 1900 MHz), unlicensed spectrum around 2.4 GHz using IEEE 802.11 modes (Wi–Fi), and

[1] VT MMR Project Website: http://www.ece.vt.edu/swe/chamrad/

Table 7.1: Performance comparison of MMRs below 1 GHz.

Receiver Specifications	**TIA–603 Specification**	**Thales AN/PRC–148**[a] [92]	**Harris AN/PRC–152**[b] [93]	**VT MMR**
Manufacturer	–	Thales	Harris	Virginia Tech
Application	–	Military	Military	Public Safety
Frequency	–	30–512 MHz	30–512 MHz	138–174 MHz, 220–222 MHz, 406–512 MHz, 764–862 MHz
Sensitivity[c]	–116 dBm	–116 dBm	–116 dBm	−119.5 dBm, −121.5 dBm, −122.5 dBm, −120.5 dBm

[a] http://www.thales.com
[b] http://www.harris.com
[c] for analog FM, 12 dB SINAD & 12.5 kHz bandwidth

dedicated spectrum around 4.9 GHz. Our plan was to use existing chipsets and separate antennas for the frequencies above 1 GHz. There are many off–the–shelf chipsets available to cover these bands/modes. Moreover, the antennas used at these frequencies are relatively compact, and can be tightly integrated into the case of the radio (as are antennas used by most modern mobile phones and devices). However, efficient antennas for bands below 1 GHz are too large to be implemented as other than traditional monopole–type antennas. At the same time, it is undesirable to implement more than one such antenna. Being limited to one antenna, and nevertheless requiring a good match and sensitivity at all frequencies of interest, we investigated the use of an RF multiplexer as reported in Chapter 6. As a result, our primary interest was in design elements supporting operation at frequencies below 1 GHz.

As shown in Figure 7.2, wideband frequency converters with wide tuning range are used to process frequencies below 1 GHz. These are referred to as the RF downconverter (RFDC) and the RF upconverter (RFUC) in Figure 7.2. It was proposed to implement two RFDCs. Each has an instantaneous bandwidth of 40 MHz. This makes it possible to receive many channels simultaneously in up to two widely-separated bands. Since it is difficult to imagine a scenario requiring simultaneous *transmission* in two widely separated bands below 1 GHz, only one RFUC with 40

MHz bandwidth was proposed.

In Figure 7.2, the PCS, 2.4 GHz, and 4.9 GHz bands use separate signal paths, each with their own antenna. For antenna–transceiver integration a triplexer was planned for below 1 GHz, and a system referred to as the "sub-GHz front end" (SGFE) was planned for duplexing receive and transmit as well as switching radios to triplexer input bands. In other words, the SGFE interfaces receiver and transmitter as well as to interface each frequency converter to the antenna. Work on the SGFE was just beginning when work on this design was halted due to the change of architecture.

The analog IF signals from RFDCs are digitized and pass through digital downconverters (DDCs), which tune within the digital passband and output complex baseband signals with selectable bandwidth and sample rate [94]. This digitized baseband signal is subsequently processed in a FPGA and an embedded microprocessor. The RFUC does the same in reverse using a digital up converter (DUC).

7.2.1 RF Downconverter (RFDC)

Figures 7.3 and 7.4 show a block diagram and image of the designed superhet-based RFDC board respectively, whereas Table 7.2 shows the summary of the characteristics. Appendix D ("Superheterodyne Downconverter") presents a detailed description of the RFDC. The RFDC tunes 138-894 MHz continuously using an "up–down" conversion architecture. The IF at the output of the RFDC board is 78 MHz with an instantaneous bandwidth of 40 MHz. The gain, noise figure, and input third-order intercept point (IIP3) of the downconverter are 47 dB, 4.5 dB, and –32 dBm, respectively. The downconverter layout occupies 139 cm^2 and consumes 280 mA at 9 VDC, however no specific attempt was made to minimize footprint or power consumption in this prototype. The parts cost of the downconverter is about $185 in small quantities. Note that the current consumption of this RFDC is large for a mobile radio application. Since two RFDCs and one RFUC are needed in this design, the total current consumption of the radio would have been much higher and may not have been a practical or feasible design.

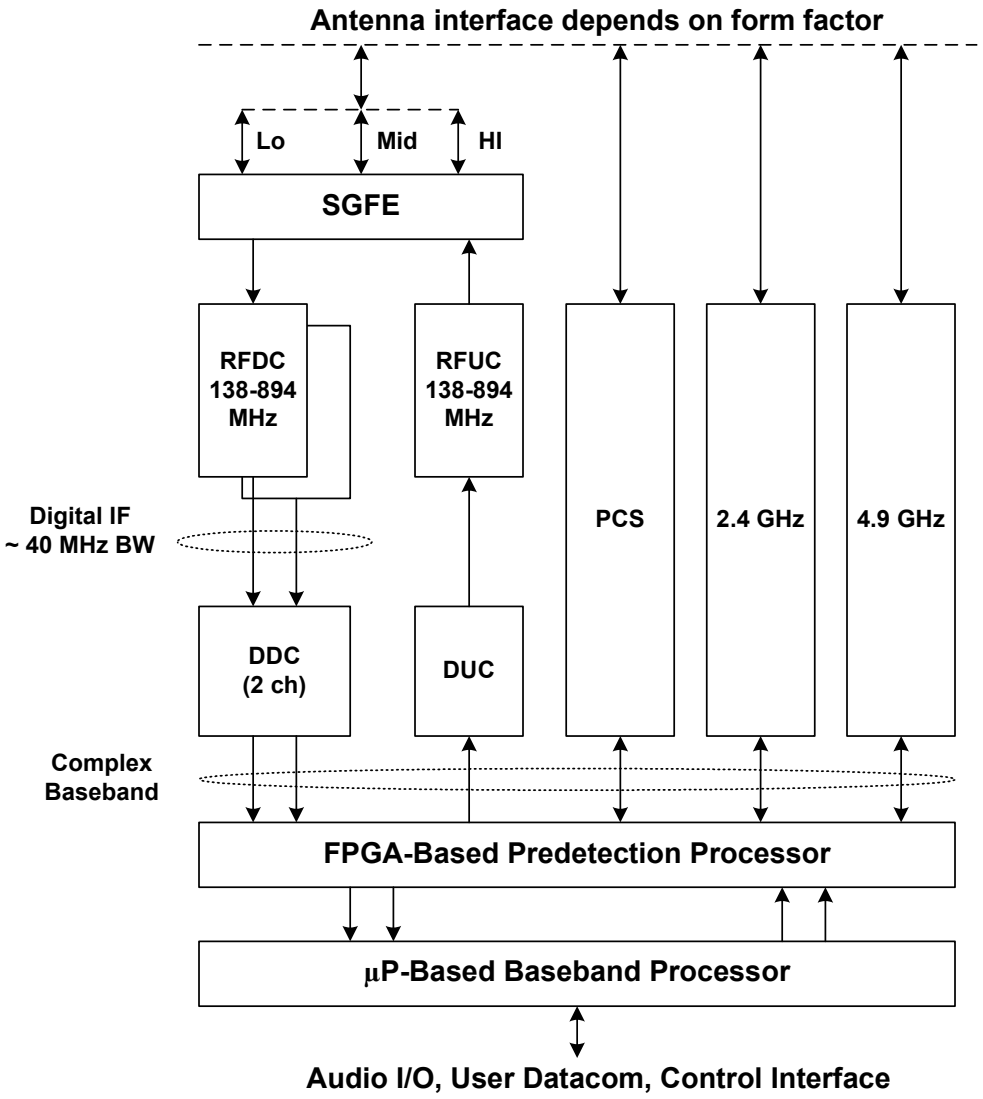


Figure 7.2: Original strawman design for the VT MMR using superhet architecture.

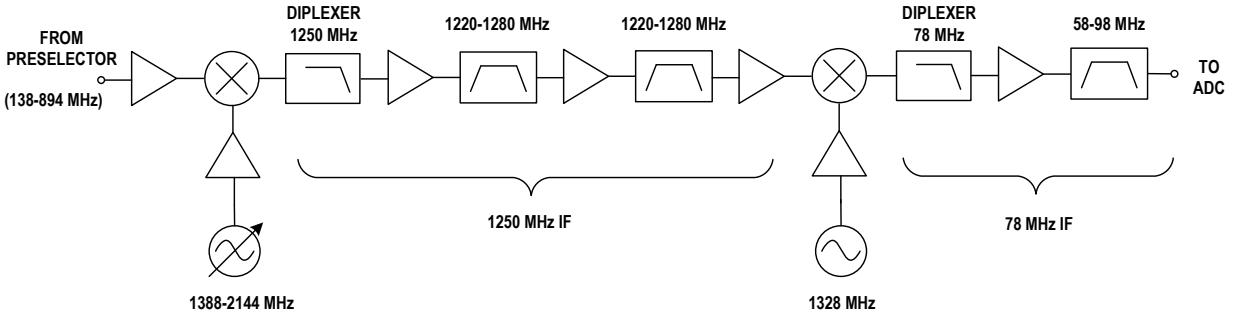


Figure 7.3: Block diagram of the superhet–based RF downconverter designed for the VT MMR.

Table 7.2: Characteristics summary of the RF downconverter designed for the original (superhet–based) VT MMR.

Parameter	**Measured Performance**	**Units**
Tuning Range	138–894 (continuous)	MHz
Instantaneous 3 dB Bandwidth	40.0	MHz
Gain	50.5 (max.) 47.0 (avg.) 35.4 (min.)	dB
IIP_3	–28.0 (max.) –32.0 (avg.) –34.0 (min.)	dBm
Noise Figure	4.5	dB
Power	2.52 (0.28 A @ 9.0 V)	W
Output IF Center Frequency	78.0	MHz
Dimensions	3.5×6.0	in

7.2.2 RF Upconverter (RFUC)

Using a similar philosophy, a superhet–based RFUC was also designed which tunes 138-894 MHz continuously using the same frequency plan as the RFDC. Figure 7.5 shows this board. However, the decision to change to the new architecture was made before measurements were performed for this board, and the design was not documented in a separate report.

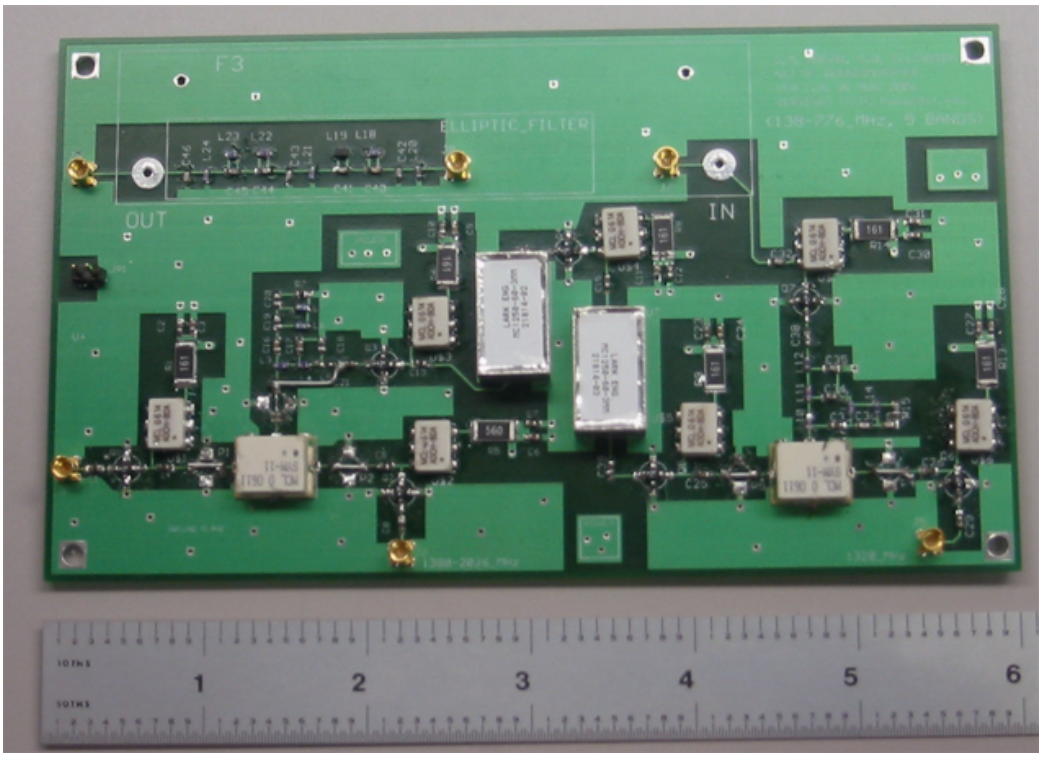


Figure 7.4: RFDC developed for the original (superhet–based) VT MMR.

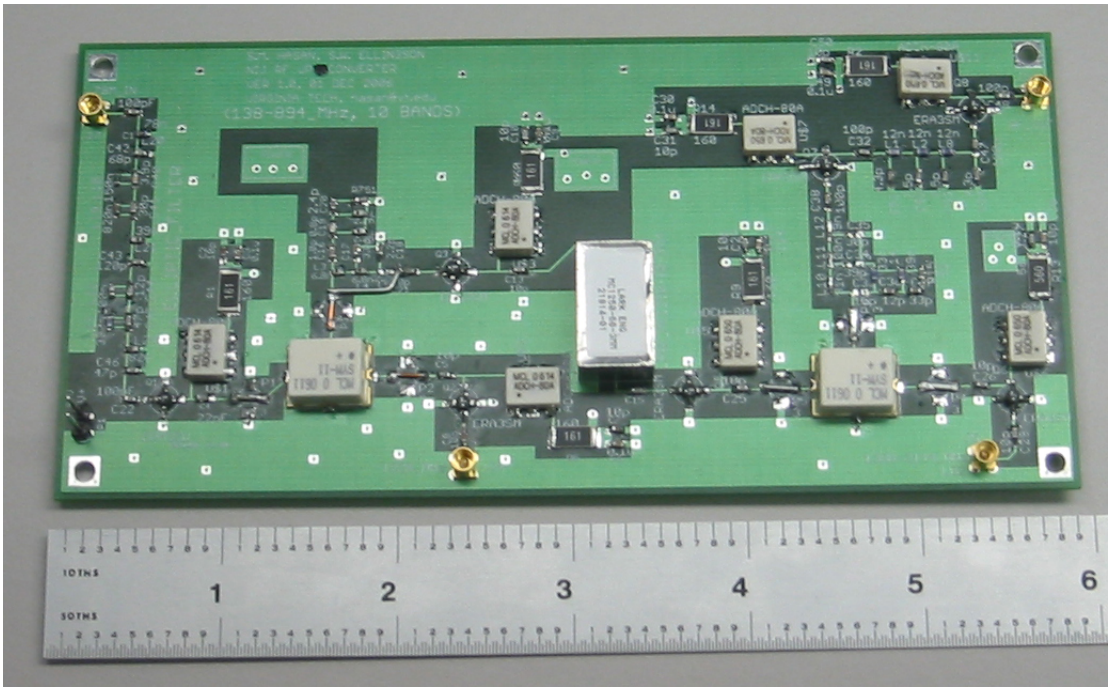


Figure 7.5: RFUC developed for the superhet–based VT MMR.

7.3 Motorola RFIC: Description & Performance Analysis

This section presents a description and performance analysis of the Motorola RFIC, which is used in the final VT MMR prototype. An overview of this IC is presented in Section 7.3.1 ("Overview of the Motorola RFIC"). A brief description of the evaluation board which we developed to measure the performance of the RFIC appears in Section 7.3.2 ("RFIC Evaluation Board"). Section 7.3.3 ("Receiver Measurement Results") presents a performance analysis related to the receiver part. (As discussed in Section 1.3, our primary concern in this dissertation is with the receiver as opposed to the transmitter, and therefore this is our emphasis in this section)

7.3.1 Overview of the Motorola RFIC

Motorola Research Laboratories recently developed a multiband direct conversion RFIC using a 90 nm CMOS process [40]. Figure 2.17 shows the internal block diagram of this RFIC. Table 7.3 shows a summary of performance of the receiver section in RFIC version 4, as provided by Motorola.

This IC is designed for operation in the frequency range of 100 MHz to 2.5 GHz. Three independent direct digital synthesizers (DDS) are used to provide local oscillator (LO) signals to the receivers, to the transmitters, and to the reverse transmit signal sources from a common 1 GHz phase locked loop (PLL). There are two options to supply only one externally provided reference signal to the RFIC: we can either supply 31.25 MHz at –10 dBm or 1 GHz at –10 dBm. In our case we chose to supply the 1 GHz reference signal.

There are five receiver paths which share a common analog baseband lowpass filter section. The bandwidth of this filter is programmable from 4.5 kHz to 10 MHz in approximately 10% steps. There are provisions for DC offset correction and dynamic matching (See Section 2.4.3 for descriptions of this technology). Similarly, there are three transmitters which share a common baseband input. Differential baseband in-phase and quadrature-phase inputs are applied to programmable low pass filters (similar to those of the receiver) with bandwidth in 10% steps from 6 kHz to 10 MHz bandwidth. There are three selectable transmitter paths with up to 75 dB (30 dB continuous and 45 dB stepped power control) of on–chip programmable gain available.

Table 7.3: RFIC version 4 receiver performance summary, as provided by Motorola [40].

Parameter	**Value**
Frequency Range	100 MHz – 2.5 GHz
Receiver Noise Figure	7 dB
Receiver Gain	48 dB
Receiver IIP2	+60 dBm
Receiver IIP3	–6 dBm
Receiver Current Drain	40 mA
LO Phase Noise	–123 dBc/Hz @ 25 kHz
LO Frequency Resolution	15 Hz
LO Current Drain per DDS	80 mA

All the parameters of the RFIC can be controlled and configured using a serial port interface (SPI) link, which consists of five signals: chip select, clock, reset, serial input, and serial output. In order to operate this IC and to set the various parameters, a minimum of 262 registers must be programmed through SPI.

Prior to using this RFIC in our design, we evaluated it using two separate evaluation boards. The first evaluation board was provided by Motorola. The second evaluation board was built by us and is described in Section 7.3.2. We found performance to be generally consistent with the specifications published by Motorola.

7.3.2 RFIC Evaluation Board

We designed and developed an evaluation board, which contains RFIC version 4, in order to validate Motorola's performance specifications and to ensure that we were able to reproduce their main results when the chip was integrated into a design developed by us. Figure 7.6 shows this evaluation board. The design of this board fully documented in [95]. This board contains all the circuitry needed to evaluate this IC including power circuit, SPI circuit, etc. All of the RF input/output (i.e. receive and transmit) ports require differential signals. Since our RF front end (including filters, preamplifiers), measurement instruments, and other related components are single–ended, we used on–board baluns to convert single–ended signals to differential, and vice–versa in all five receive and three transmit ports. To interface to the differential baseband ports we used two peripheral boards

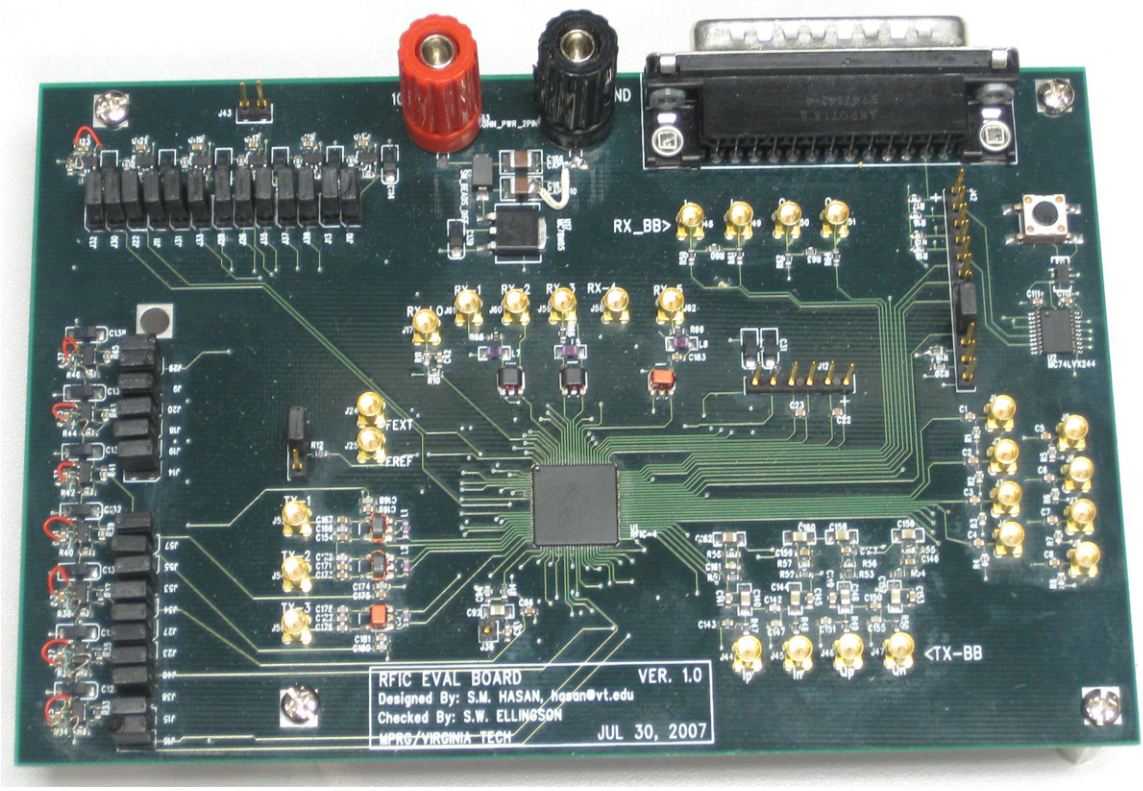


Figure 7.6: VT evaluation board for Motorola RFIC version 4. The IC itself is the square chip in the center of the board.

provided by Motorola: one converts a differential input signal to a single–ended output signal; and the other board converts a single–ended signal to a differential output signal to supply baseband input to the transmitter.

In our measurements we used a LabView[4] program, which was also developed by Motorola, to control the functionality of the RFIC via SPI. Figure 7.7 shows a screenshot of this program. The default settings which are used during the measurement of the RFIC receiver are presented in Table 7.4. Additional details of the testing are documented in [96].

[4] http://www.ni.com/labview

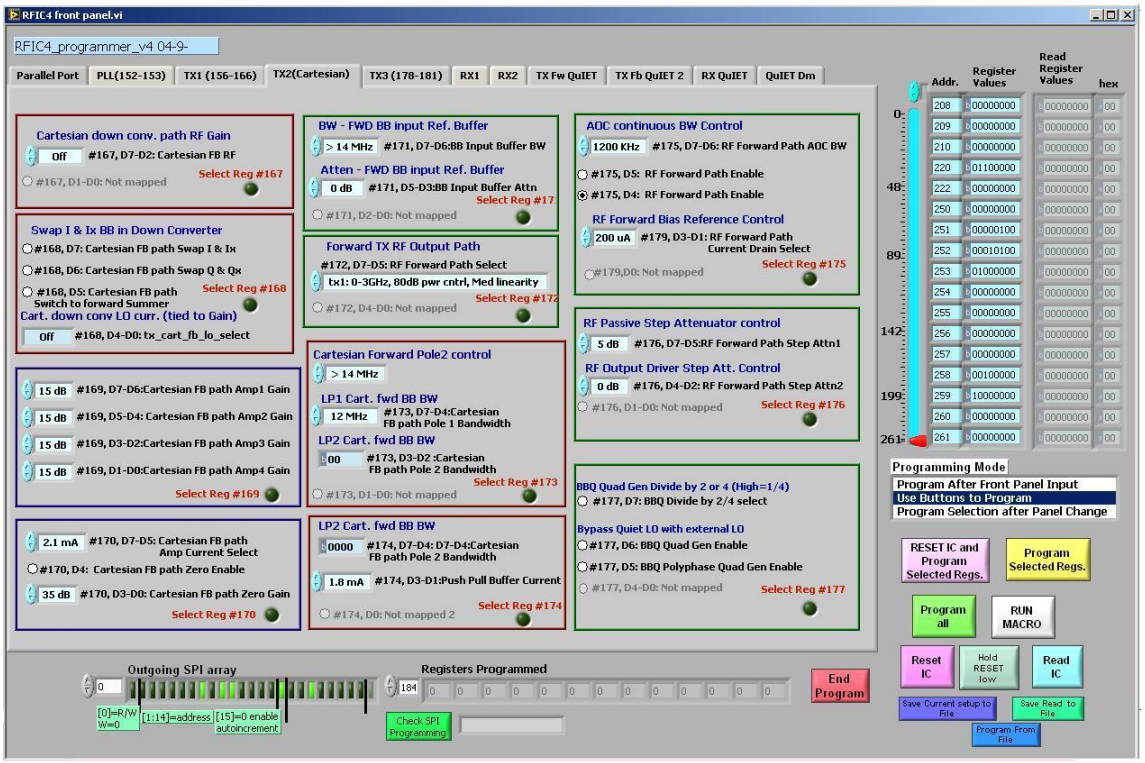


Figure 7.7: Snapshot of the LabView program used to configure the RFIC through an SPI link.

Table 7.4: Default settings for the receiver operation of the Motorola RFIC during the performance analysis experiment [97].

Parameter	**Address, Bits**	**Setting**	**Function/Value**
LNA Control	205, 7:5	001b	LNA 1 enable
LNA Bias	205, 4:3	00b	2 mA
Filter Enable	195, 0	1b	Enable
Filter Output	196, 0	1b	Enable
External Cap	195, 7	0b	Disable
Chopper Clock	195, 1	0b	Disable
Chopper	195, 6:4	00b	Disable
Bi-Quad Q	198, 7:5	000b	0.8
Bi-Quad Gain	198, 4:3	10b	6 dB
Bi-Quad Resistor	198, 2:0	000b	1.4 kΩ
Bi-Quad Capacitor	203, 204, 1:0, 7:0	00b, 00h	2 pF
VGA Resistor	199, 7:5	000b	2.5 kΩ
VGA Capacitor	202, 203, 7:0, 7:5	00h, 000b	1 pF
VGA Gain	200, 2:0	000b	14 dB
PMA R_{in} Resistor	199, 4:2	000b	1 kΩ
PMA R_f Resistor	199, 1:0	00b	5 kΩ
PMA Capacitor	200, 201, 7:3, 7:0	00000b, 00h	1 pF
Compensation Control	203, 4:2	000b	
DCOC DAC Enable	192, 0	1b	Enable
DCOC DAC Setting	192, 7:3, 193, 7:3	10111b, 10011b	
DCOC DAC Step	192, 2:1	00b	0.5 μA
DCOC Comparator	193, 1	0b	Disable
DCOC Enable	193, 0b	0b	Disable
RC Tune	194, 7	0b	Disable
RC Tune Ramp	194, 6	0b	Disalbe
On-channel Detector	196, 7	0b	Disable
Off-channel Detector	196, 6	0b	Disable

7.3.3 Receiver Measurement Results

This section presents the RFIC receiver section measurement results using the above evaluation board, which have been taken using the first of five receive ports of the RFIC. Table 7.5 summarizes the receiver measurement results in public safety frequency bands. These results apply to the RFIC without any attempt to optimize configurable settings internal to the chip.

Fig. 7.8 shows the gain–frequency characteristics. This is power gain, measured with respect to 50 Ω termination. Although the gain rolls off a little bit in the VHF and PCS bands, it is steady in the UHF, 700 MHz and 800 MHz bands. We can see that the gain lies between 45 and 52 dB, which is consistent with Motorola's specification in Table 7.3.

Figure 7.9 shows the input 1 dB compression point for the RFIC receiver. The input 1 dB compression point varies between –35 and –14 dBm, and it improves once we cross into the UHF band. Although it was not measured, we can estimate the IIP3 using Equation 2.23; it varies between –25 and –4 dBm. It should be noted that the IIP3 specification provided by Motorola shown in Table 7.3 (–6 dBm) is measured at 800 MHz. From our measurement we achieve –16 dBm IIP3 at 800 MHz which is approximately 10 dB lower than Motorola's specification. Discussion with Motorola suggests that this difference probably due to the associated external circuitry (e.g., balun) used in the evaluation board [41]. However, this fact has not been confirmed due to the unavailability of IIP3 information in the balun manufacturer's datasheet.

The measurement results of image rejection for the RFIC receiver are shown in Figure 7.10. We performed these measurements using the default parameters, which are optimized for 800 MHz, and did not attempt to optimize the performance for other frequencies. For that reason, the image rejection is high in the 800 MHz frequency band compared to the other bands. We observed the worst image rejection with these settings is in the PCS band; approximately 9 dB. Although presumably the performance achieved at 800 MHz could be achieved at other frequencies with some tuning of the parameters in Table 7.4, due to schedule and funding limitations we did not attempt to do this.

Table 7.5: Measured receiver performance of the RFIC in public safety frequency bands.

Band	**Freq. (MHz)**	**Gain (dB)**	P_{1dB} **(dBm)**	**Image Rejection (dB)**
VHF	156.0	47.8	−33.0	27.6
	221.0	49.8	−33.0	24.9
UHF	459.0	48.8	−34.0	19.4
700 MHz	770.0	50.0	−27.0	28.7
	800.0	49.8	−26.0	30.0
800 MHz	811.5	50.1	−24.0	35.7
	836.5	51.0	−23.0	42.2
	856.5	51.1	−23.0	38.4
	881.5	50.6	−22.0	28.4
PCS	1920.0	42.2	−14.0	9.20
		10V @ 0.11A (1.1 W)[a] total for the evaluation board		

[a]Current drain for the RFIC alone: 40 mA @ 2.5 V for RF/BB; 80 mA @ 2.5 V for LO

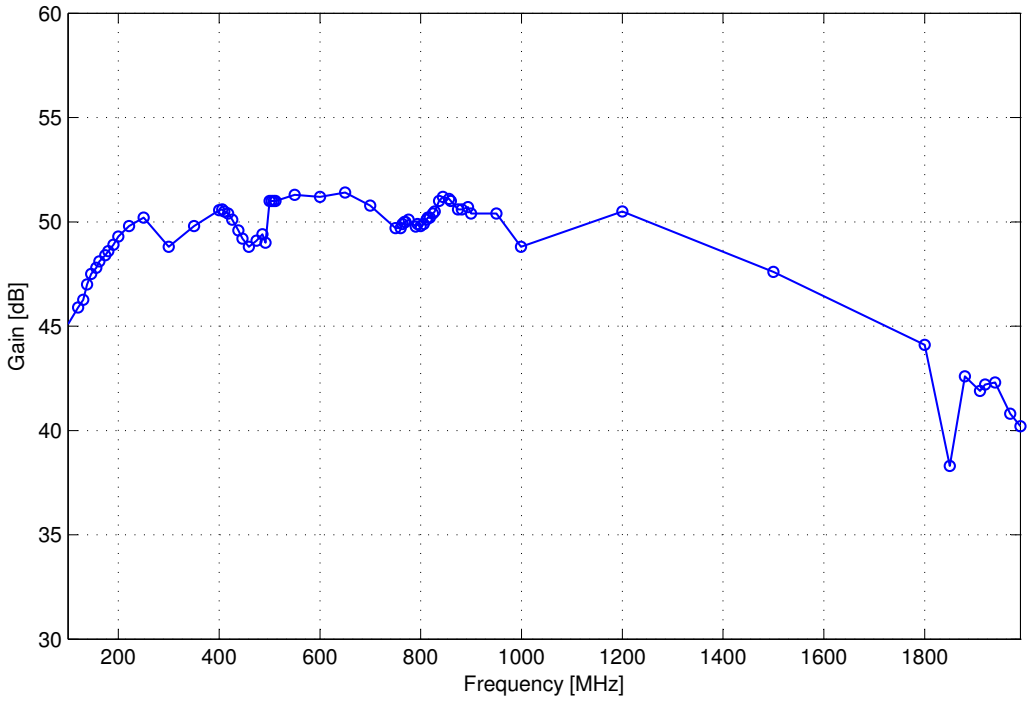


Figure 7.8: Gain measured in the first receiver port of the RFIC.

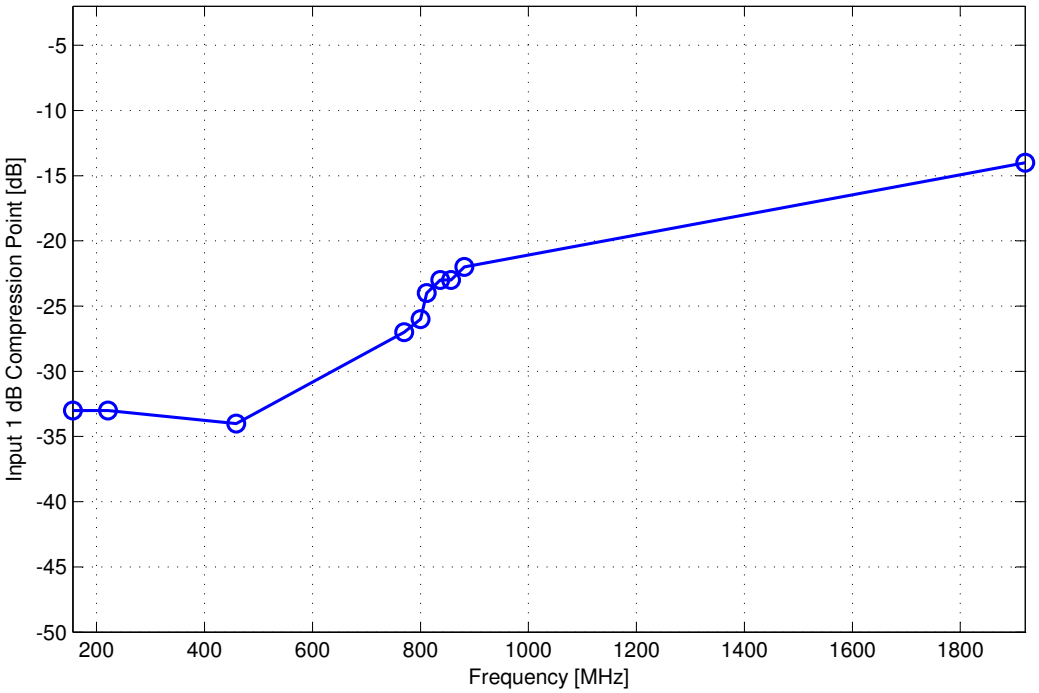


Figure 7.9: Input 1 dB compression point measured in the first receiver port of the RFIC.

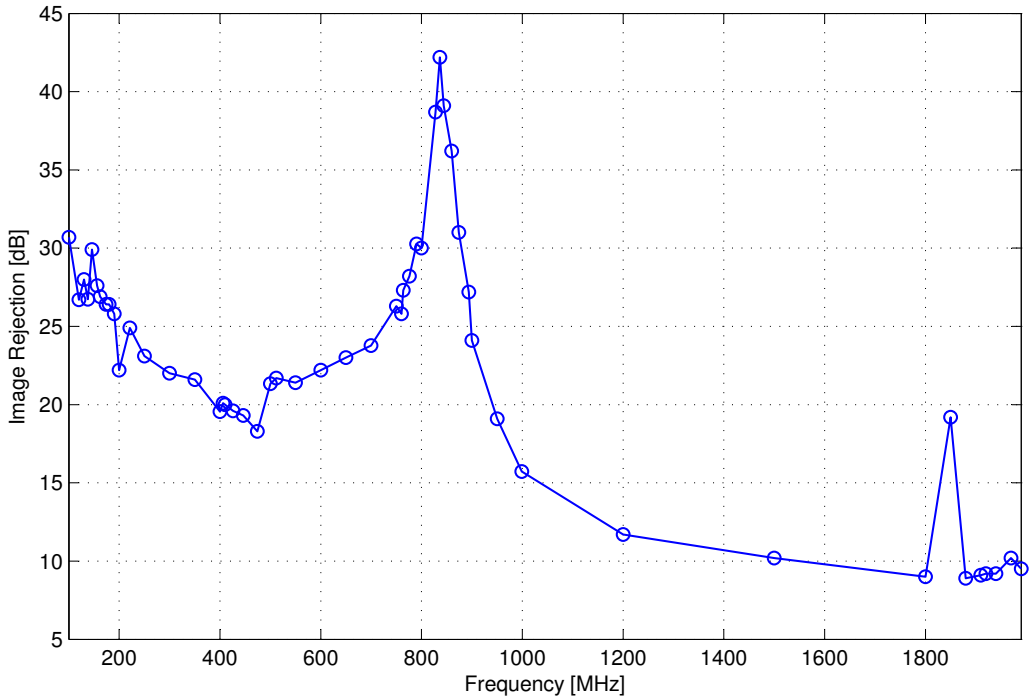


Figure 7.10: Image rejection measured in the first receiver port of the RFIC.

7.4 Direct Conversion Architecture

Figure 7.11 shows a system diagram of the VT MMR prototype using direct conversion architecture, incorporating the Motorola RFIC. It should be noted that this design eliminates the need for separate RFDC, RFUC, DDC and digital DUC ICs, and thereby dramatically reduces the power, component count, and total cost of the radio. For example, the cost of the RFIC is estimated to be $50 [41]; however, the implementation cost of just one RFDC is approximately $185.

The antenna of Section 6.2 (Figure 6.12) is attached to a RF multiplexer, which divides the signal into four bands: 138-174 MHz, 220-222 MHz, 406-512 MHz, and 764-862 MHz using the multiplexer of Section 6.2. The RF front end (RFFE) board shown in Figure 7.11 contains this multiplexer as well as RF switches to control the receive/transmit selection. After additional filters, attenuators, and preamplifiers the outputs of this board are connected to the receiver inputs of the RFIC board to convert the incoming RF signal to baseband differential I and Q analog signals. A/D converters residing on the ADC/DAC board digitize these signals and send them to the FPGA board for further processing.

In transmit mode the FPGA board sends the modulated baseband signal to the ADC/DAC board, which converts the digital transmit signal to analog I and Q signals and sends these to the RFIC board. The RFIC upconverts this signal to the desired carrier frequency. Two inputs of the RFFE board are connected to the two transmit ports of the RFIC board and are switched to multiplexer channels as indicated in Figure 7.11.

Our ADC/DAC board contains a frequency synthesizer to supply a 1 GHz (–10 dBm) reference frequency (F_{ref}) to the RFIC board. This synthesizer requires an external 10 MHz reference signal (1.0 to 3.3 V_{pp}), which is generated by a DAC that resides on the FPGA board. The RFIC can alternatively be operated using a 31.25 MHz reference signal, which can be supplied either externally or from the FPGA board. We encountered difficulty making the RFIC work using either the 1 GHz reference or the FPGA–sourced 31.25 MHz reference, so we supplied 31.25 MHz F_{ref} from an external signal source. The FPGA board supplies the 4 MHz sample clock for the ADC/DAC board.

As shown in Figures 7.1 and 7.11, the prototype consists of six boards – RFFE board, RFIC board,

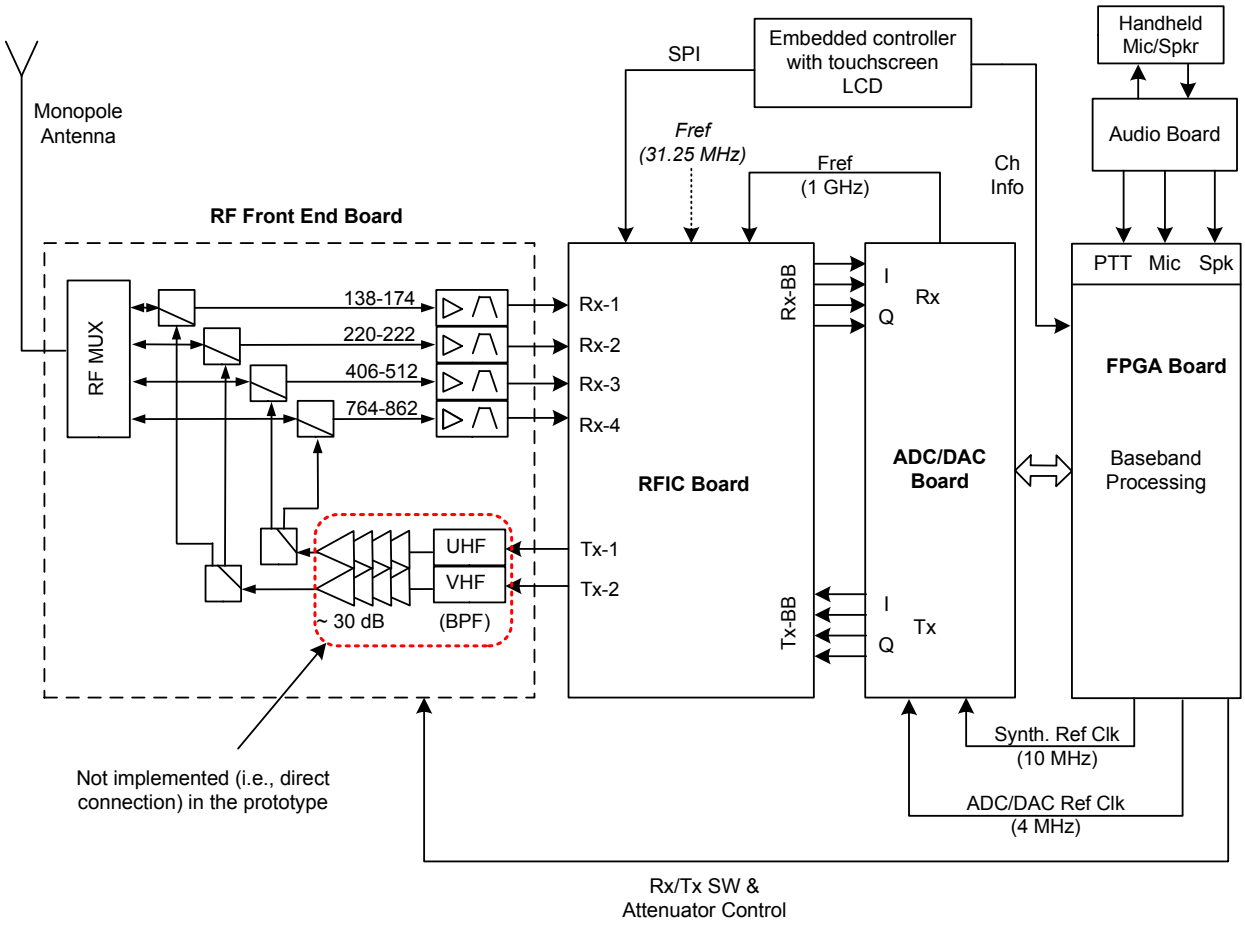


Figure 7.11: System diagram of the final VT MMR prototype (using the Motorola RFIC).

ADC/DAC board, FPGA board, audio control board, and user interface board. The first three boards are stacked together and connected directly, i.e., without cable, using male–female MMCX RF connectors in order to achieve a more compact arrangement. The ADC/DAC board is also connected with the FPGA board using a 80–pin square 0.1-in header using the "Analog Devices Interface" (ADI) pin assignment scheme. A detailed description of the audio board and the user interface of this radio is provided in Appendix H. The next section describes the design of other parts in more detail.

7.5 Prototype Design

This section presents the design overview of the developed VT MMR prototype. Section 7.5.1 ("RFFE Board") and Section 7.5.2 ("RFIC Board") describe the RFFE board and the RFIC board, respectively. The description of the ADC/DAC board and the FPGA board is presented in Section 7.5.3 ("ADC/DAC Board") and Section 7.5.4 ("FPGA Board"), respectively. Section 7.5.5 ("GNI Analysis") presents a GNI analysis/performance summary of the radio. At the end, Section 7.5.6 ("Current Status") presents the current status of this prototype.

7.5.1 RFFE Board

Figures 7.12 and 7.13 show the board-level implementation of the designed RFFE board. A block diagram of this board is shown in Figure 7.14. A detailed description including the circuit diagram, PCB layout, and bill of materials are presented in Appendix E. Since we are using a monopole in this radio, it requires a ground plane. As shown in Figure 7.12, the top layer of this board serves as the ground plane for our antenna. All other components including multiplexer, filters, amplifiers, and RF switches are placed at the bottom layer as shown in Figure 7.13.

7.5.2 RFIC Board

The RFIC board in the current VT MMR prototype is an evolution from the evaluation board described in Section 7.3.2, and is shown in Figure 7.15. Appendix F documents the design in detail

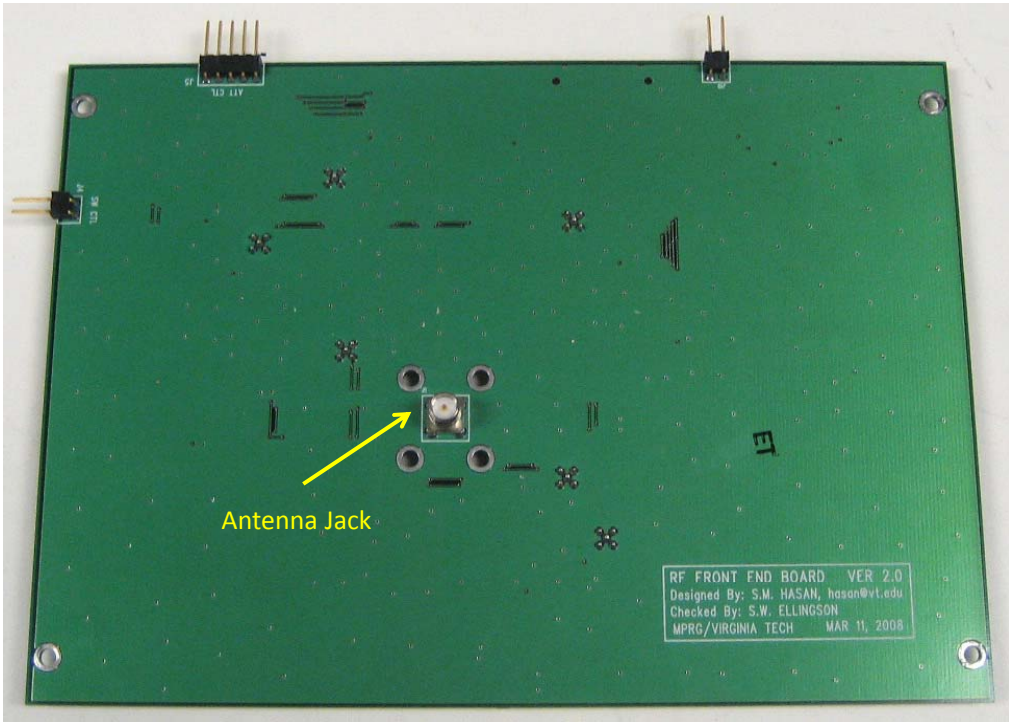


Figure 7.12: RFFE board for the VT MMR (top view); ground screen side.

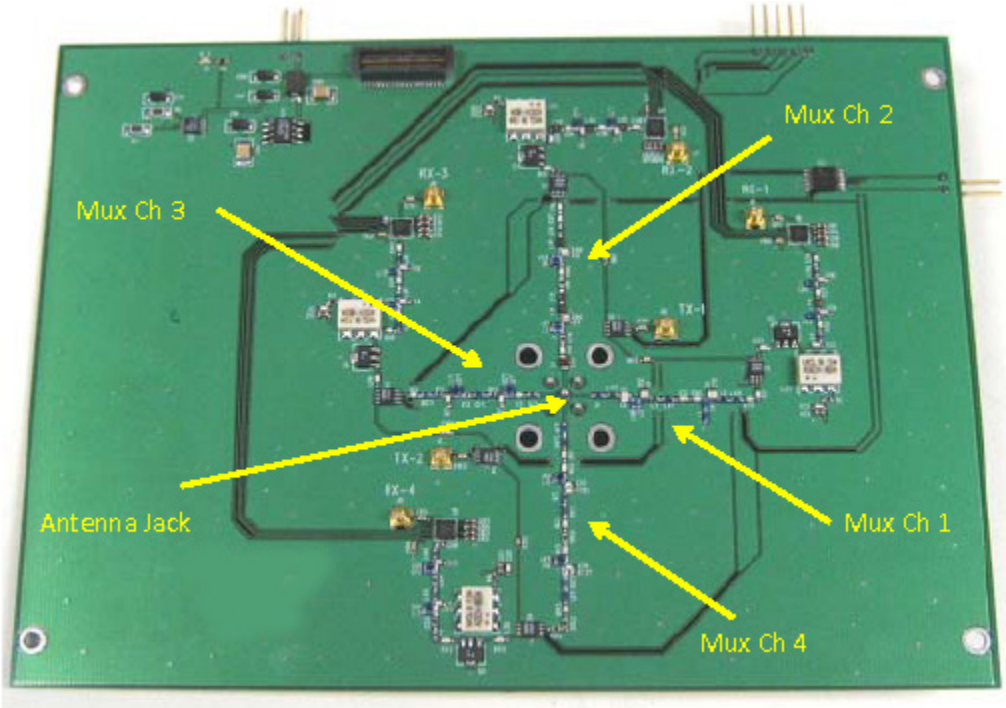


Figure 7.13: RFFE board for the VT MMR (bottom view); component side.

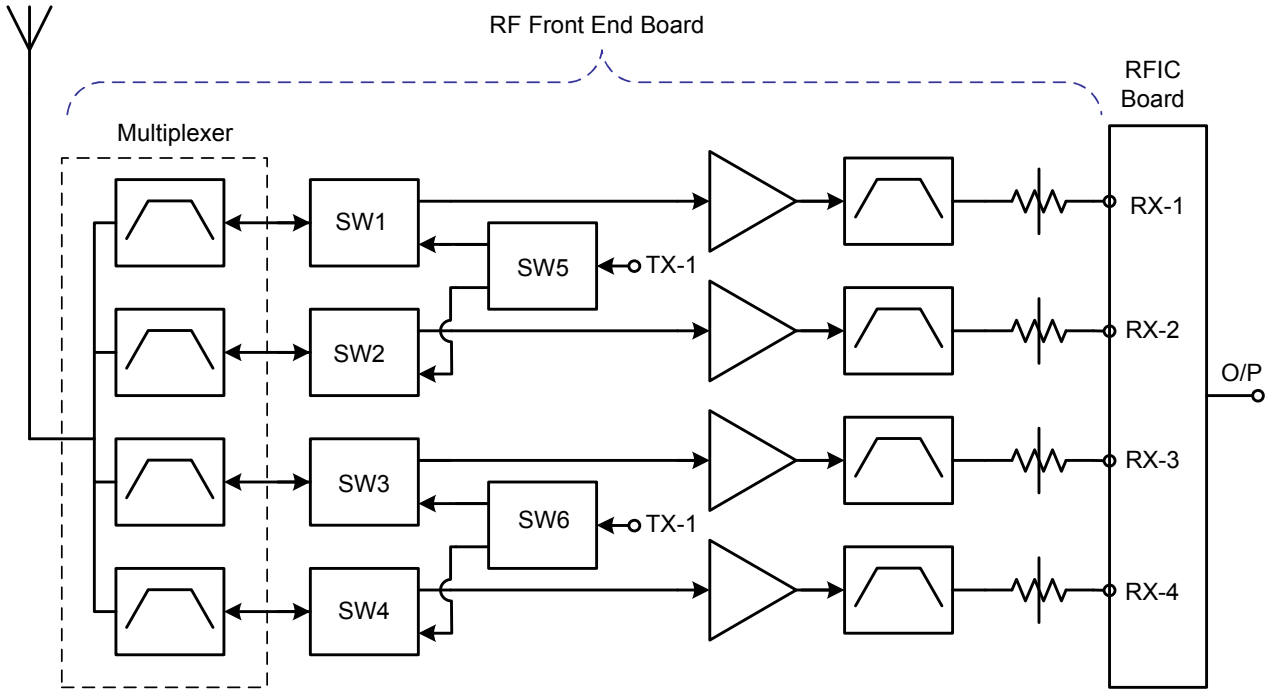


Figure 7.14: Block diagram of the RFFE board.

including the schematic, PCB layout, and bill of materials.

Since the receivers in the RFIC require differential signals, transformers have been used as baluns to convert single-ended signals to/from RFFE to differential signals. Ports Rx-1 to Rx-4 use the ETC1-1-13 1:1 transformer (frequency range 4.5 to 3000 MHz) from M/A-COM [2]. Similar to the receiver section, the RFIC also provides the transmitter output in differential form, which is converted into single-ended using a transformer. Since the impedance for the RFIC transmitter ports is 200Ω, we use a 1:4 transformer, Model ETC4-1T-7 (frequency range 6 to 1000 MHz) from M/A-COM.

Like the performance of the evaluation board, at 800 MHz the measured gain of the receiver section of this RFIC board is also 50 dB, input 1dB compression point is –26 dBm, and the image rejection is around 30 dB[3]. Note that the performance of this RFIC, specifically the image rejection, can be improved significantly if we optimize the various programmable parameters as discussed in

[2]http://www.macom.com

[3]Although not specifically of interest in this study, we also looked at transmit. Transmitter output power at 800 MHz is 1.5 dBm, output 1 dB compression point is 1.6 dBm, and sideband rejection is 17 dB.

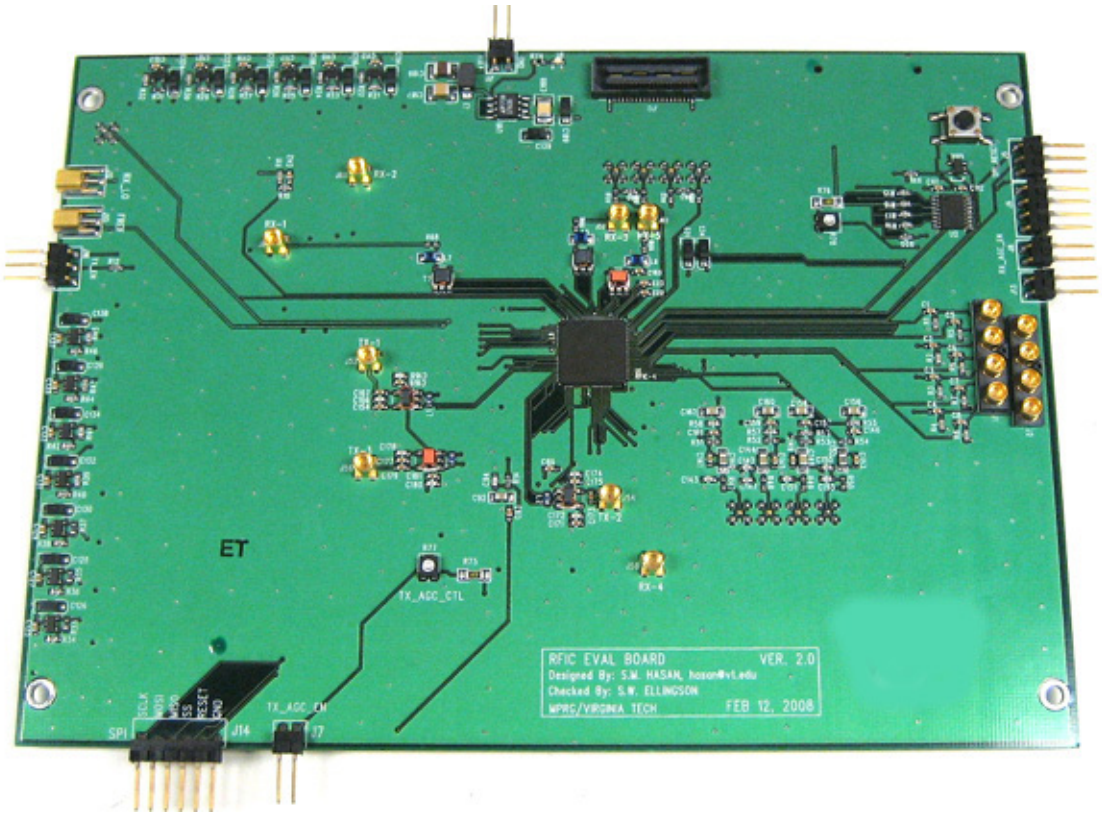


Figure 7.15: RFIC board for the VT MMR.

Section 7.3.3. The implemented RFIC board consumes 1.1W power (10V @ 110 mA) during reception and consumes 1.7W (10V @ 170 mA) power during transmission.

7.5.3 ADC/DAC Board

Figure 7.16 shows the ADC/DAC board. A detailed description of this board including the circuit diagram, PCB layout, and bill of materials is presented in Appendix G.

The differential I and Q signals from the RFIC board are digitized using the AD9248 A/D converter from Analog Devices[4]. This is a dual 14-bit ADC sampling 4 MSPS (in our design) which consumes about 65 mA at 3V. Similarly, the AD9761 dual 10-bit D/A converter is used to generate differential analog I and Q signals. This is an interpolating DAC which samples at 4 MSPS and consumes about 50 mA at 3V. A compelling feature of this part is the availability of internal interpolation

[4]http://www.analog.com

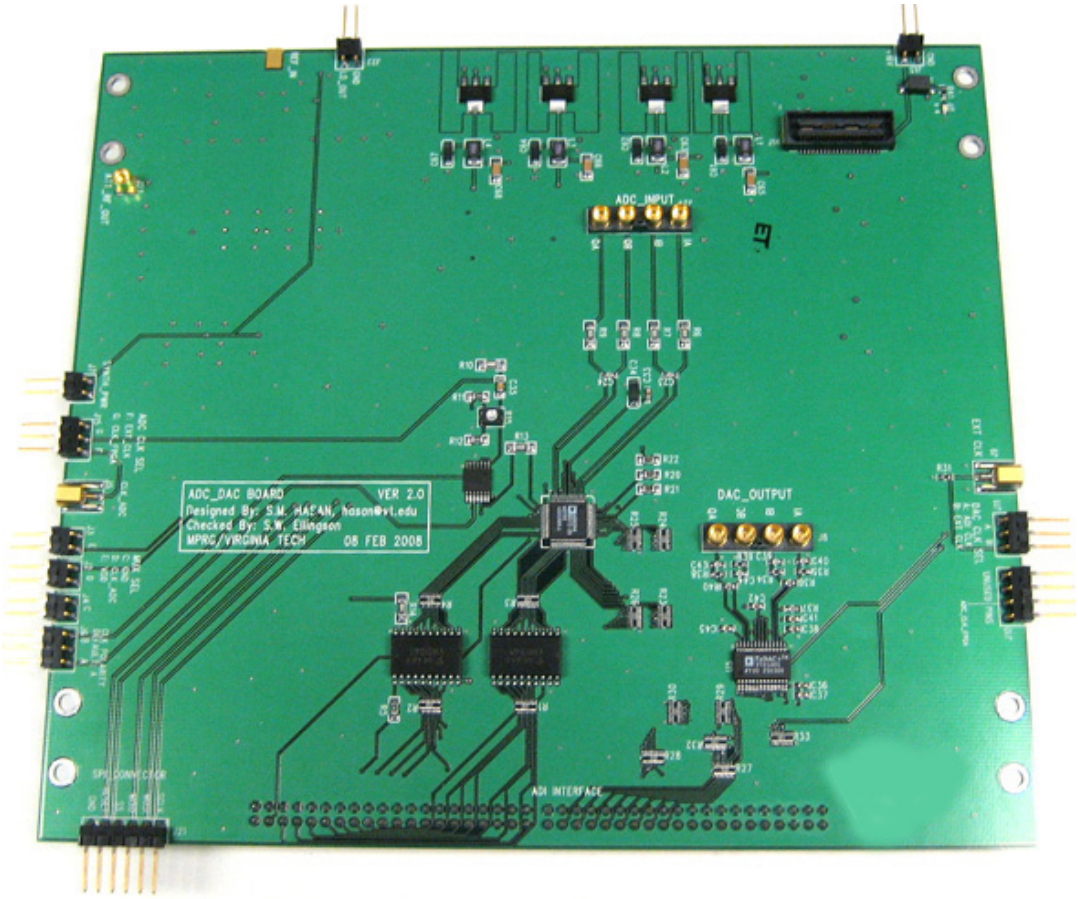


Figure 7.16: ADC/DAC board for the VT MMR (frequency synthesizer on reverse side).

filters which lead to a significantly reduced requirement for anti-alias filtering. This board also contains a frequency synthesizer to supply 1 GHz reference frequency to the RFIC board.

7.5.4 FPGA Board

To process digital baseband signals in the VT MMR, we used a Stratix II DSP development board, which contains a Stratix II EP2S60F1020C4 FPGA, from Altera[5]. This board was selected based on our familiarity with this board due to work in other projects, as well as the availability of a suitable audio CODEC, Model TLV320AIC23PW, from Texas Instruments[6]. All digital signal processing is performed in the Stratix II FPGA. This FPGA is overkill for this application; only

[5]http://www.altera.com
[6]http://www.ti.com

about 5% of the logic elements are used for single–channel analog FM. However, this is useful to facilitate experimentation with multiple simultaneous modes (e.g. voice and data communication simultaneously) at a later time. The FPGA firmware is written completely in Verilog HDL.

7.5.5 GNI Analysis

This section describes some considerations in planning of the analog signal path of the VT MMR as well as presents a GNI analysis. The analog signal path is defined here as the section beginning at the antenna terminals and ending at the input to the ADC. This signal path contains all the circuitry in the RFFE board (which includes multiplexer, amplifier, additional filtering and attenuators) and the RFIC transceiver board.

In order to receive the signal and digitize it appropriately, the amplitude of the signal input to the ADC should meet the specification/requirement of the ADC. The relevant parameters and design constraints are shown in Table 7.6, see also Section 2.3.1 for additional explanation. Note that P_Q is calculated using 11.8 bits, which is the effective number of bits (ENOB) of the ADC we are using [98]. A summary of the analysis is provided in Table 7.7, which shows the values for N_b, G_{min}, G_r corresponding to our frequency bands. It should be noted that P_{ext} (total external noise power received by the receiver) is calculated using Table 4.2. P_S (total power due to external signal sources) is set to be the largest value which results in $G_r/G_{min} \geq 3$ dB in each band. P_t (total power input to the receiver at the antenna terminals) is the sum of P_S and P_{ext}. For all the above calculations, signal bandwidth is assumed to be 12.5 kHz, which is currently the most common bandwidth for analog FM voice communication.

Tables 7.8 to 7.11 provide the results of GNI analysis of the VT MMR receiver for each multiplexer channel. Because the implemented multiplexer did not perform properly (see Section 6.2.3), these calculations assume the nominal design represented by Figure 6.16. The gain of the multiplexer channel indicated here is the TPG shown in Figure 6.16 at the center frequency of each channels. Since the ohmic loss of the multiplexers and filters are not known exactly, the noise figure is set to 1 dB for these components. It should also be noted that the value of IIP3 for the RFIC is chosen from the specification of Motorola provided in Table 7.3. The gain of the RFIC is adjustable, and is changed from the default 50 dB to 53 dB and 63 dB for the channels 3 and 4, respectively, to fulfill

Table 7.6: ADC specifications and associated design constraints for the VT MMR.

Parameter	**Value**	**Definition**
P_{clip}	+4 dBm	ADC full scale
P_Q	–66.8 dBm	ADC quantization noise power, referenced to ADC input
γ_q	+3 dB	Desired ratio of P_{ext} to P_Q
δ_r	–10 dB	Maximum acceptable input power relative to P_{clip}

Table 7.7: Design implications (N_b, G_{min}, G_r) corresponding to various choices of frequency range and response. Gain here defined is defined from antenna terminals to ADC input.

Frequency	P_t	P_{ext}	N_b	G_{min}	G_r
138-174 MHz	–67.7 dBm	–122.5 dBm	11.3	58.7 dB	61.7 dB
220-222 MHz	–73.3 dBm	–128.1 dBm	11.3	64.3 dB	67.3 dB
406-512 MHz	–80.5 dBm	–135.3 dBm	11.3	71.5 dB	74.5 dB
764-862 MHz	–88.1 dBm	–142.9 dBm	11.3	79.1 dB	82.1 dB

the gain requirements. Tables 7.8 to 7.11 also indicate the sensitivity for each multiplexer channel. Sensitivity is calculated using Equation 2.17 assuming $\delta = 6.5$ dB SNR (corresponding to 12 dB audio SINAD, for analog FM with $B = 12.5$ kHz bandwidth). The presented GNI analysis confirms that the designed radio achieved –119.5 dBm or better sensitivity, which compares favorably to the sensitivity requirement of TIA–603 standard as well as the sensitivity of some existing MMRs as shown in Table 7.1.

7.5.6 Current Status

The radio is able to operate in the 138–174 MHz, 220–222 MHz, 406–512 MHz, and 764–862 MHz public frequency bands, although performance is impaired by the multiplexer implementation problem discussed in Section 6.2.3. If that problem can be overcome, and the RFIC parameters are optimized, then performance will be very good, as indicated in Tables 7.8 to 7.11. However, even in its current condition, over the air reception and transmission of narrowband analog FM signals has been demonstrated in each of the bands.

The transmit part of this radio has not been implemented completely. The current design only uses the amplification internal to the RFIC and achieves maximum +6 dBm transmit output power. +30 dBm to +36 dBm would be required for a practical radio. Although the low TPG of the

Table 7.8: GNI analysis of the analog signal path of the VT MMR for multiplexer Channel 1 (138–174 MHz).

Stage	**G (dB)**	**IIP3 (dBm)**	**F (dB)**
Multiplexer	–5.5	200.0	1.0
RF Switch	–0.5	48.0	0.5
Preamp	25.0	12.9	2.7
Filter	–1.0	200.0	1.0
Attenuator	–6.0	30.0	6.0
RFIC Board	50.0	–6.0	7.0
Cascade Analysis	62.0	–18.0	7.3
Sensitivity	–119.5 dBm		

Table 7.9: GNI analysis of the analog signal path of the VT MMR for multiplexer Channel 2 (220–222 MHz).

Stage	**G (dB)**	**IIP3 (dBm)**	**F (dB)**
Multiplexer	–2.0	200.0	1.0
RF Switch	–0.5	48.0	0.5
Preamp	25.0	12.9	2.7
Filter	–1.0	200.0	1.0
Attenuator	–4.0	30.0	4.0
RFIC Board	50.0	–6.0	7.0
Cascade Analysis	67.5	–23.5	4.9
Sensitivity	–121.5 dBm		

Table 7.10: GNI analysis of the analog signal path of the VT MMR for multiplexer Channel 3 (406–512 MHz).

Stage	**G (dB)**	**IIP3 (dBm)**	**F (dB)**
Multiplexer	–1.0	200.0	1.0
RF Switch	–0.5	48.0	0.5
Preamp	25.0	12.9	2.7
Filter	–1.0	200.0	1.0
Attenuator	–1.0	30.0	1.0
RFIC Board	53.0	–6.0	7.0
Cascade Analysis	74.5	–27.5	4.2
Sensitivity	–122.5 dBm		

Table 7.11: GNI analysis of the analog signal path of the VT MMR for multiplexer Channel 4 (764–862 MHz).

Stage	**G (dB)**	**IIP3 (dBm)**	**F (dB)**
Multiplexer	–3.5	200.0	1.0
RF Switch	–0.5	48.0	0.5
Preamp	25.0	12.9	2.7
Filter	–1.0	200.0	1.0
Attenuator	–1.0	30.0	1.0
RFIC Board	63.0	–6.0	7.0
Cascade Analysis	82.0	–25.0	5.7
Sensitivity	–120.5 dBm		

multiplexer is not problem for receiver, this would be a problem for transmit since good matching (to achieve maximum power transfer) is required in order to mitigate the reflection of transmitted power back into the transmit and receive sections of the radio. We did not address this issue in the present work. For that reason, there is a need to modify the current design to increase the transmission efficiency; perhaps by connecting the transmitter to the antenna through a separate set of (variable) matching circuits. However, this left is left for future work.

Table 7.12 shows the power consumption of the VT MMR. The radio consumes approximately 1.51A current at 16V. We use a 4 A·h battery, which lasts for about 1.5 hours at this current draw. As shown in the table, the FPGA board and user interface circuitry consume approximately 88% of the total power. However, no attempt has been made to optimize the power consumption, and in a practical implementation, these could easily be made dramatically less.

7.6 Summary

This chapter presented a description of a prototype multiband multimode radio based on direct conversion architecture for public safety application. This prototype was designed to operate in all the public safety frequency bands from 100 MHz to 1 GHz using just a single narrowband monopole antenna, the size and shape of which is similar to those used by traditional mobile radios. The multiplexer described in Section 6.2 is used to integrate the antenna with the receiver. This radio advances the state–of–the–art in MMR by allowing a single traditional antenna to cover all bands

Table 7.12: Power consumption of the VT MMR prototype.

Board	**Power**	**Current Drain**
RFFE	0.18 W	16V @ 10 mA
RFIC	1.70 W	16V @ 110 mA
ADC/DAC	0.99 W	16V @ 60 mA
FPGA	13.28 W	16V @ 830 mA
User Interface & Others	8.00 W	16V @ 500 mA
Total	**24.16 W**	**16V @ 1.51 A**

over a very large tuning range to be received with sensitivity which is comparable to existing radios which require antenna changes to accomplish the same goal. Table 7.1 shows this comparison. Limitations of this radio are also discussed in Section 7.5.6.

Chapter 8

Conclusions

This dissertation described new concepts to design RF front ends focusing on the development and evaluation of *sensitivity–constrained* RF multiplexers which allow the integration of a single antenna to a receiver with large, multiband tuning ranges. Chapter 4 ("Sensitivity-Constrained Front-End Design") describes the concept of sensitivity–constrained design, develops the associated theory and analysis, and provides a demonstration in field conditions. In Chapter 5 ("Multiplexer Design"), this concept was extended to the design of multiplexers and once again verified through field measurements. In Chapter 6 ("Multiplexer Application to a Multiband Multimode Radio") this approach was used to design a multiplexer for a public safety MMR with a small monopole antenna. In Chapter 7 ("Design & Development of a Multiband Multimode Radio), we described a complete multiband multimode radio using the multiplexer of Chapter 6.

In this chapter, principal findings and topics for future research are suggested.

8.1 Findings

The principal findings in this dissertation are as follows:

1. Sections 4.2 and 4.3 describe an "optimum" noise figure specification for wideband receivers, which accounts for the trade–off between antenna–receiver match efficiency and bandwidth,

and emphasizes external noise dominance. To support this work, existing noise models were reformulated into a more convenient form.

2. In Section 4.4, a sensitivity–constrained front end for the frequency range 10–80 MHz was developed to demonstrate that it is possible to design an external noise–limited front end even for the lowest possible (Galactic) noise environment. Although this fact is already known for horizontal dipoles [74], we demonstrated it in this study for a vertical VHF monopole antenna more similar to antennas used in vehicle mobile radios and over a larger frequency range. This experiment setup was then available for testing our multiplexer design concept.

3. Section 5.3 described an approach to multiplexer design to integrate a single antenna with multiple wideband receivers to achieve improved usable bandwidth over traditional methods. The key is to emphasize external noise dominance over good antenna–receiver matching. In this way, uniform performance over large bandwidths is possible. A three channel (10–28 MHz, 32–50 MHz, and 54-80 MHz) multiplexer for a VHF monopole antenna was designed and performance was validated through field experiment (in Section 5.4). Despite poor TPG, all three channels of the designed multiplexer were demonstrated to be strongly Galactic noise–dominated for a preamplifier noise figure of 3 dB.

4. The application of the proposed multiplexer design technique to public safety MMR was demonstrated in Sections 6.1 and 6.2 by designing two multiplexers: (1) One for a generic rod antenna 20 cm long and 5 mm radius, and (2) Another for a commercially–available monopole antenna with similar dimensions. Each of the multiplexers has four channels (138–174 MHz, 220–222 MHz, 406–512 MHz, and 764–862 MHz). (This result has been published [88]) We found that although the TPG performance of the multiplexer designed for the commercial antenna was not as good as the multiplexer designed for the generic rod antenna, the difference did not have a significant effect on the overall sensitivity of the radio. Figures 6.11 and 6.19 show that both multiplexers achieve –123.0 dBm or better sensitivity (δ = 0 dB, 12.5 kHz bandwidth) for the desired range of frequencies assuming preamplifier noise figure of 2 dB. For analog FM, this corresponds to –116.5 dB for 12 dB SINAD.

5. The design and development of a complete public safety MMR using a direct conversion wideband RFIC from Motorola and employing the multiplexer designed in Section 6.2 is

described in Chapter 7 (Also, reported in [90]). We were not able to achieve the nominal performance of the multiplexer in practice due to limitations in available surface–mountable capacitors and inductors, as discussed in Section 6.2.3. However, we have demonstrated that if this limitation can be overcome, then this radio achieves –119.5 dBm or better sensitivity (12 dB SINAD & 12.5 kHz bandwidth) for analog FM, which is 3.5 dB better than TIA–603 standard for analog FM receivers. A summary of performance is shown in Tables 7.8 to 7.11.

8.2 Future Work

The recommended future investigations are as follows:

1. The external noise characterization shown in Table 4.2 is based on the ITU noise report [73], which may not be universally valid or representative of current or new sources of man-made noise. So this noise characterization should be updated making new measurements or using the latest noise measurements reported by others.

2. To achieve the nominal performance of the implemented multiplexer, simulations accounting for board parasitics, and incorporation of trimmer capacitors to facilitate fine adjustments, should be considered.

3. In this study, no attempt was made to optimize the antenna – the burden was solely on the multiplexer. Antenna–multiplexer co–design (i.e., to design antenna and multiplexer together to achieve jointly optimum performance) should be considered as a possible way to further increase the overall performance.

4. Investigation of the use of non–Foster matching techniques should be considered. A serious concern in the use of non–Foster matching is the known challenges of stability, linearity, and noise figure associated with the amplifier stages employed in NICs as described in Section 3.5. So to develop a suitable wideband NIC with low noise figure can be a new research topic.

5. RFIC designers usually prefer differential design due to the advantages described in Section 2.4.4.2. However, the concept discussed in this dissertation emphasizes single–ended

circuitry. In order to make the proposed work more useful for practical implementation (e.g., eliminating the need for balun transformers) differential implementation of this work should be considered.

6. Since this dissertation is mainly focused on the receiver, the transmitter part of the VT MMR is not designed to achieve acceptable transmission efficiency. Future research is needed to complete the integration of a single antenna to both of the transmitter and the receiver to achieve good transmission efficiency as well as acceptable receive sensitivity.

Appendix A

Relationship Between Predetection SNR and SINAD

The purpose of this appendix is to explain the relationship between the predetection signal–to–noise ratio (SNR) and the audio signal–to–noise–and–distortion ratio (SINAD) for an analog FM demodulation[1]. SINAD is defined as ratio of the signal including noise and distortion to the noise and distortion component for an analog FM receiver.

In [99, pp. 169–172], Jakes gives the relationship between the audio signal power, S_0, and the signal power, S, as:

$$S_0 = \left(1 - e^{-\rho}\right)^2 S \tag{A.1}$$

where ρ is the predetection SNR. The total audio noise, N, is given by:

$$N = \frac{a\left(1 - e^{-\rho}\right)^2}{\rho} + \frac{8\pi BW e^{-\rho}}{\sqrt{2(\rho + 2.35)}} \tag{A.2}$$

where B is the input signal bandwidth in Hz, W is the baseband lowpass cutoff frequency in Hz, and a is $B/(2W)$.

We want to know S_0/N as a function of ρ. A difficulty arises in doing this, because S_0 is a function of S, whereas N is not. Jakes deals with this by making the assumption that "the RMS frequency

[1] This appendix based on notes provided by S.W. Ellingson, Virginia Tech, dated 1996.

deviation is 10 dB less than half the noise bandwidth minus the top baseband frequency, so that the signal deviation peaks do not often exceed the IF bandwidth (Carsons's Rule)". This is expressed as follows:

$$S = \frac{\pi^2 (B - 2W)^2}{2} \tag{A.3}$$

Using this assumption, S_0/N as a function of ρ is plotted in Figure A.1 for analog FM radio receivers (assuming $B = 12.5$ kHz, $W = 3.0$ kHz).

Now consider what this means in terms of audio SINAD. SINAD is defined as $(S+N+D)/(N+D)$, where D is the audio harmonic distortion. Typically receivers to have D/S less than 5% for a –50 dBm input signal. N should be negligible for this condition, so this implies a SINAD of 21 dB. This D/S relationship should not change significantly as the input level is reduced to the sensitivity level; that is, the RF level which results in 12 dB audio SINAD. Thus, the SINAD at this level should be dominated by S and N, with negligible contribution from D. If $(S + N)/N = 12$ dB, then $S/N = 11.7$ dB; not a significant difference. Therefore, the S/N that results in a 12 dB audio SINAD should be about 6.5 dB.

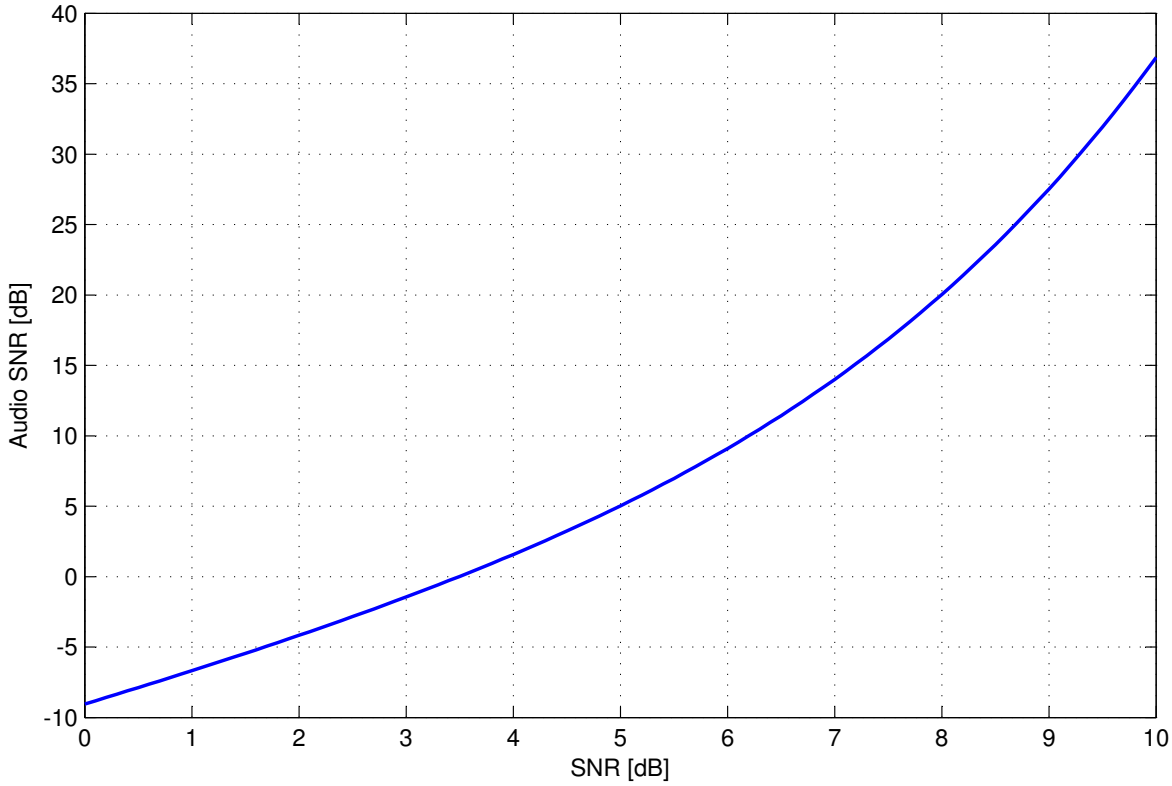


Figure A.1: Audio SNR as a function of predetection SNR for analog FM ($B = 12.5$ kHz).

Appendix B

GNI Analysis

The total gain, noise figure, and intermodulation intercept point of a receiver can be determined using a stage-cascade gain, noise figure, and third order intercept (GNI) analysis. Figure B.1, which shows a block diagram of a general receiver chain, is used to demonstrate this analysis [29]. G_i, F_i, and IIP3_i represents the gain, noise figure, input third order intercept point of each of the stages, respectively, where $i = 1, 2, 3, \ldots, n$.

The cascade (total) gain is

$$G_{total} = G_1 G_2 \ldots\ldots G_n. \tag{B.1}$$

The cascade (combined) noise figure of the stages in the receiver chain is

$$F_{total} = F_1 + \frac{(F_2 - 1)}{G_1} + \frac{(F_3 - 1)}{G_1 G_2} + \ldots\ldots + \frac{(F_n - 1)}{G_1 G_2 \ldots G_{n-1}}. \tag{B.2}$$

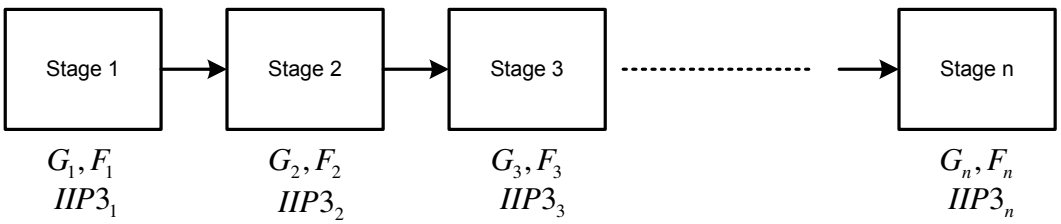


Figure B.1: Block diagram of a general receiver chain for GNI analysis. All the component values are in linear units (i.e., not dB).

The cascade IIP3 is given by

$$\frac{1}{\text{IIP3}_{total}} = \frac{1}{\text{IIP3}_1} + \frac{G_1}{\text{IIP3}_2} + \frac{G_1 G_2}{\text{IIP3}_3} + \ldots\ldots + \frac{G_1 G_2 \ldots G_n}{\text{IIP3}_n}. \tag{B.3}$$

The output third order intercept point (OIP3) is sometimes of interest. The relationship to IIP3 is simply $\text{OIP3} = G \cdot (\text{IIP3})$.

Appendix C

VHF Multiplexer Board

This appendix presents details of the design of the multiplexer board for the VHF monopole antenna discussed in Section 5.4 ("VHF Monopole Multiplexer Design Example"). Figure C.1 shows the schematic of the multiplexer board. The PCB layout of the implemented multiplexer board is presented in Figure C.2. The bill of materials for this board is shown at the end of this appendix.

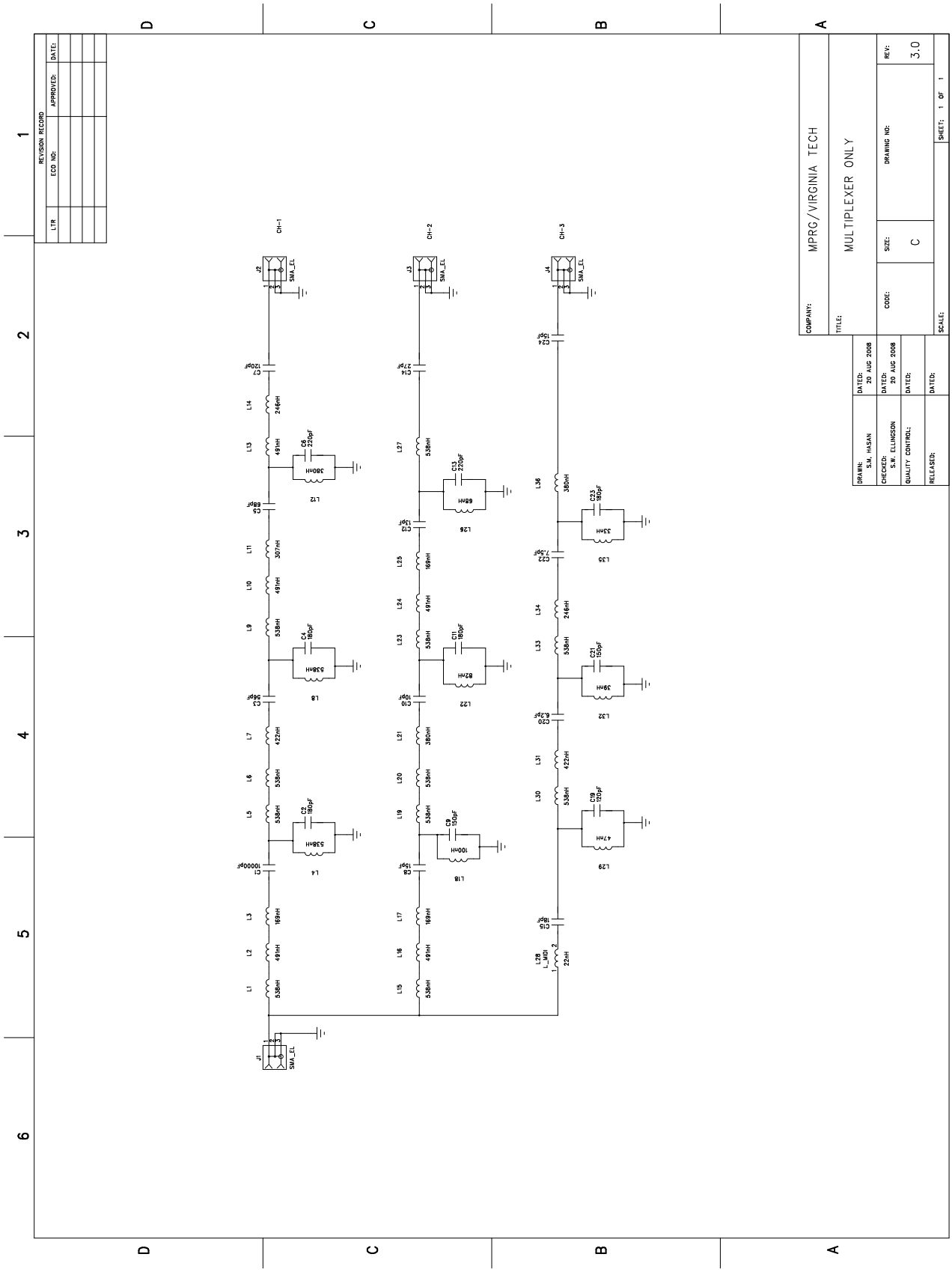


Figure C.1: Schematic of the multiplexer designed for the VHF monopole antenna.

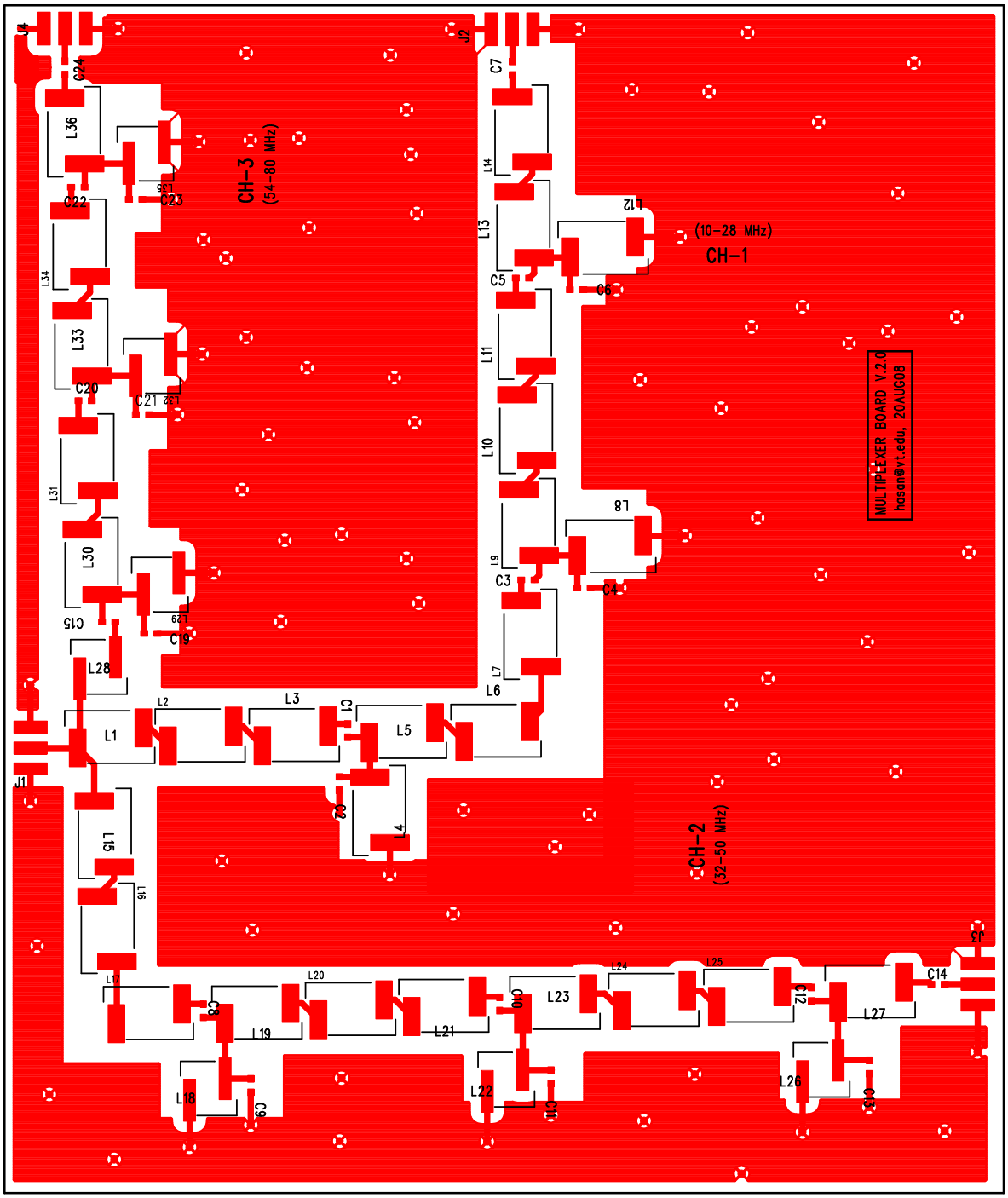


Figure C.2: Top layer of the multiplexer board designed for the VHF monopole antenna.

Bill of Materials
VHF Multiplexer Board
MPRG/Virginia Tech
Prepared by: SM Hasan, Date: AUG 11, 2008

Item	Qty	Reference	Part Name	Package	Manufacturer	Manufacturer Part #	Distributor	Distributor Part #	Description
1	1	C1	10000pF 50V	CAP-0603	Kemet	C0603C103J5RACTU	Digikey	399-1092-1-ND	SURFACE MOUNT CAPACITOR 0603 Size
2	1	C10	10pF 50V	CAP-0603	Kemet	C0603C100J5GACTU	Digikey	399-1049-1-ND	SURFACE MOUNT CAPACITOR 0603 Size
3	2	C7 C19	120pF 50V	CAP-0603	Kemet	C0603C121J5GACTU	Digikey	399-1062-1-ND	SURFACE MOUNT CAPACITOR 0603 Size
4	1	C12	13pF 100V	CAP-0603	Murata Electronics	GRM1885C2A130JA01D	Digikey	490-1330-1-ND	SURFACE MOUNT CAPACITOR 0603 Size
5	2	C9 C21	150pF 50V	CAP-0603	Panasonic - ECG	ECJ-1VC1H151J	Digikey	PCC151ACVCT-ND	SURFACE MOUNT CAPACITOR 0603 Size
6	2	C8 C24	15pF 50V	CAP-0603	Panasonic - ECG	ECJ-1VC1H150J	Digikey	PCC150ACVCT-ND	SURFACE MOUNT CAPACITOR 0603 Size
7	4	C2 C4 C11 C23	180pF 50V	CAP-0603	Panasonic - ECG	ECJ-1VC1H181J	Digikey	PCC181ACVCT-ND	SURFACE MOUNT CAPACITOR 0603 Size
8	1	C15	18pF 50V	CAP-0603	Panasonic - ECG	ECJ-1VC1H180J	Digikey	PCC180ACVCT-ND	SURFACE MOUNT CAPACITOR 0603 Size
9	2	C6 C13	220pF 50V	CAP-0603	Panasonic - ECG	ECJ-1VC1H221J	Digikey	PCC221ACVCT-ND	SURFACE MOUNT CAPACITOR 0603 Size
10	1	C14	27pF 50V	CAP-0603	Panasonic - ECG	ECJ-1VC1H270J	Digikey	PCC270ACVCT-ND	SURFACE MOUNT CAPACITOR 0603 Size
11	1	C3	56pF 50V	CAP-0603	Kemet	C0603C560J5GACTU	Digikey	399-1057-1-ND	SURFACE MOUNT CAPACITOR 0603 Size
12	1	C20	6.2pF 50V	CAP-0603	Murata Electronics	GRM1885C1H6R2DZ01D	Digikey	490-1394-1-ND	SURFACE MOUNT CAPACITOR 0603 Size
13	1	C5	68pF 50V	CAP-0603	Kemet	C0603C680J5GACTU	Digikey	399-1058-1-ND	SURFACE MOUNT CAPACITOR 0603 Size
14	1	C22	7.5pF 50V	CAP-0603	Murata Electronics	GRM1885C1H7R5DZ01D	Digikey	490-1398-1-ND	SURFACE MOUNT CAPACITOR 0603 Size
15	3	L3 L17 L25	169nH	IND_MAXI	Coil Craft	132-12SMGLB	Coil Craft	132-12SMGLB	Surface Mount Inductor Maxi Size
16	2	L14 L34	246nH	IND_MAXI	Coil Craft	132-15SMGLB	Coil Craft	132-15SMGLB	Surface Mount Inductor Maxi Size
17	1	L11	307nH	IND_MAXI	Coil Craft	132-16SMGLB	Coil Craft	132-16SMGLB	Surface Mount Inductor Maxi Size
18	3	L12 L21 L36	380nH	IND_MAXI	Coil Craft	132-17SMGLB	Coil Craft	132-17SMGLB	Surface Mount Inductor Maxi Size

Item	Qty	Reference	Part Name	Package	Manufacturer	Manufacturer Part #	Distributor	Distributor Part #	Description
19	2	L7 L31	422nH	IND_MAXI	Coil Craft	132-18SMGLB	Coil Craft	132-18SMGLB	Surface Mount Inductor Maxi Size
20	5	L2 L10 L13 L16 L24	491nH	IND_MAXI	Coil Craft	132-19SMGLB	Coil Craft	132-19SMGLB	Surface Mount Inductor Maxi Size
21	13	L1 L4-6 L8-9 L15 L19-20 L23 L27 L30 L33	538nH	IND_MAXI	Coil Craft	132-20SMGLB	Coil Craft	132-20SMGLB	Surface Mount Inductor Maxi Size
22	1	L18	100nH	IND_MIDI	Coil Craft	1812SMSR10GLB	Coil Craft	1812SMSR10GLB	Surface Mount Inductor Midi Size
23	1	L28	22nH	IND_MIDI	Coil Craft	1812SMS22NGLB	Coil Craft	1812SMS22NGLB	Surface Mount Inductor Midi Size
24	1	L35	33nH	IND_MIDI	Coil Craft	1812SMS33NGLB	Coil Craft	1812SMS33NGLB	Surface Mount Inductor Midi Size
25	1	L32	39nH	IND_MIDI	Coil Craft	1812SMS39NGLB	Coil Craft	1812SMS39NGLB	Surface Mount Inductor Midi Size
26	1	L29	47nH	IND_MIDI	Coil Craft	1812SMS47NGLB	Coil Craft	1812SMS47NGLB	Surface Mount Inductor Midi Size
27	1	L26	68nH	IND_MIDI	Coil Craft	1812SMS68NGLB	Coil Craft	1812SMS68NGLB	Surface Mount Inductor Midi Size
28	1	L22	82nH	IND_MIDI	Coil Craft	1812SMS82NGLB	Coil Craft	1812SMS82NGLB	Surface Mount Inductor Midi Size
29	4	J1-4	SMA Female Edge Mount	SMA Connector	Linx Technologies	CONSMA003.062	Digikey	CONSMA003.062-ND	CONN FEMALE EDGE MT FOR .062" BD

Appendix D

Superheterodyne Downconverter

This appendix documents the design of the superheterodyne RF downconverter board (RFDC) for the VT MMR discussed in Section 7.2 ("Original Superhet Architecture"). Figures D.1 and D.2 show the schematic of the RFDC board. The PCB layout of the implemented RFDC board is shown in Figure D.3. The bill of materials for this board is shown at the end of this appendix.

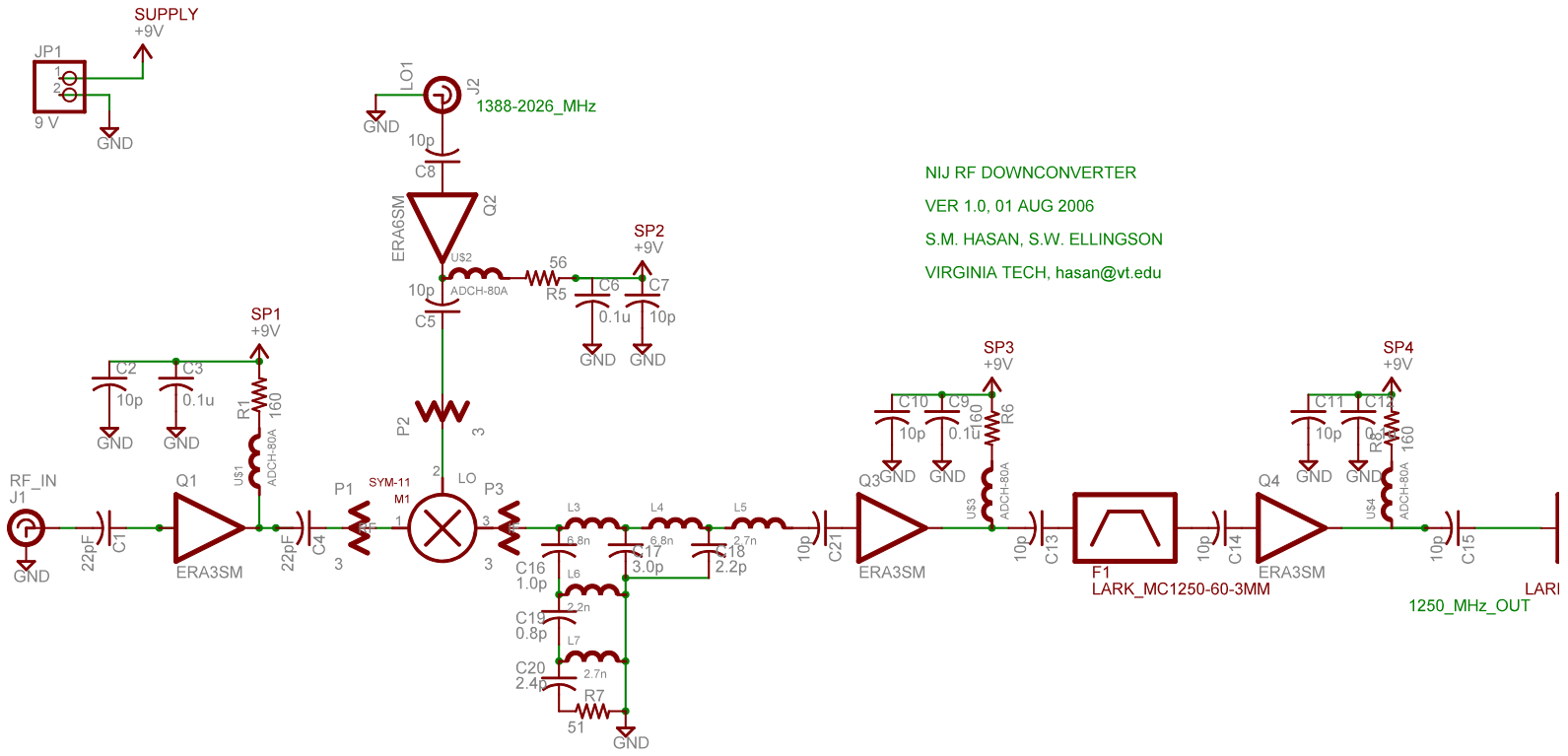


Figure D.1: Schematic of the superheterodyne RF downconverter board designed for the initial VT MMR prototype (continues in Figure D.2).

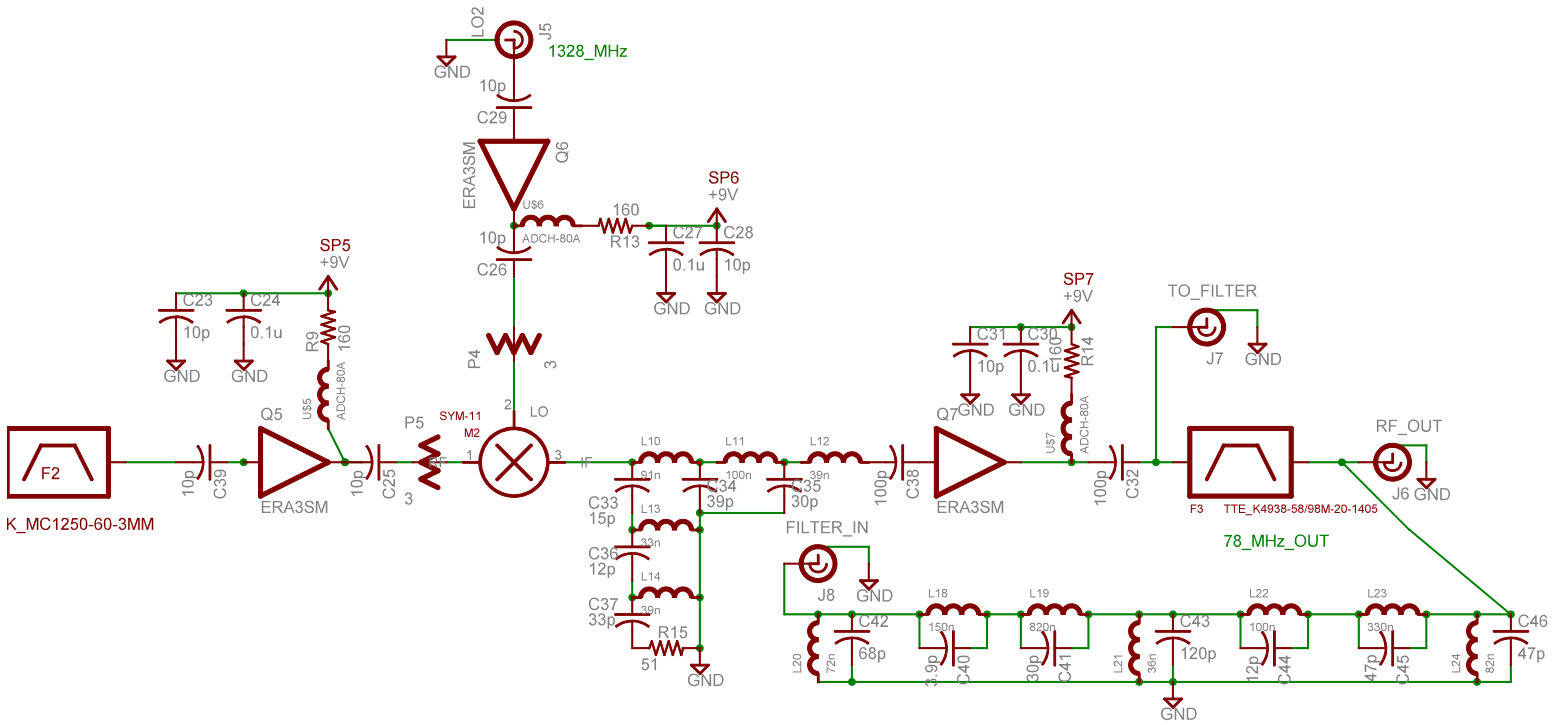


Figure D.2: Schematic of the superheterodyne RF downconverter board designed for the initial VT MMR prototype (continued from Figure D.1).

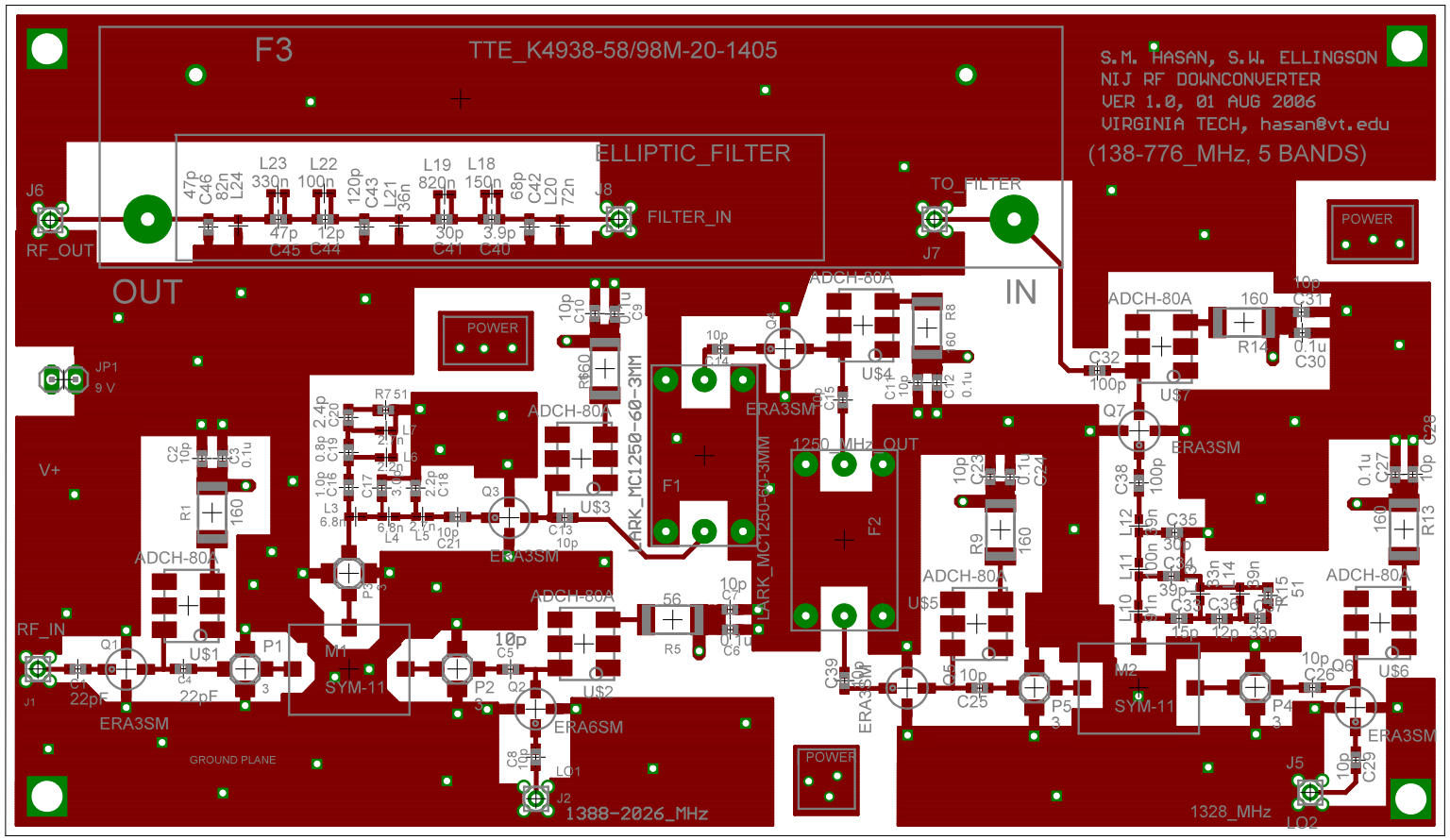


Figure D.3: Top layer of the superheterodyne RF downconverter board designed for the initial VT MMR prototype.

Bill of Materials
NIJ RF Downconverter Board, Version 1.0
MPRG/Virginia Tech
Prepared by: SM Hasan, Date: AUG 01, 2006

Item	Qty	Reference	Part Name	Package	Manufacturer	Mfg. No.	Distributor	Distributor No.	Description
1	17	C2, C5, C7, C8, C10, C11, C13, C14, C15, C21, C23, C25, C26, C28, C29, C31,	10p	C0603	TDK Corporation	C1608C0G1H100D	Digikey	445-1269-1-ND	CAP CER 10PF 50V C0G 0603
2	2	C1, C4	22p	C0603	TDK Corporation	C1608C0G1H102J	Digikey	445-1293-1-ND	CAP CER 1000PF 50V C0G 5% 0603
3	7	C3, C6, C9, C12, C24, C27, C30	0.1u	C0603	TDK Corporation	C1608Y5V1H104Z	Digikey	445-1324-1-ND	CAP CER .10UF 50V Y5V 0603
4	1	C16	1.0p	C0603	AVX Corporation	06035J1R0BBTTR	Digikey	478-2808-1-ND	CAP CERAMIC 1.0PF 50V 0603 RFSMD
5	1	C17	3.0p	C0603	AVX Corporation	06035J3R0BBTTR	Digikey	478-2817-1-ND	CAP CERAMIC 3.0PF 50V 0603 RFSMD
6	1	C40	3.9p	C0603	AVX Corporation	06035J3R9BBTTR	Digikey	478-2819-1-ND	CAP CERAMIC 3.9PF 50V 0603 RFSMD
7	1	C18	2.2p	C0603	AVX Corporation	06035J2R2BBTTR	Digikey	478-2814-1-ND	CAP CERAMIC 2.2PF 50V 0603 RFSMD
8	1	C19	0.8p	C0603	AVX Corporation	06035J0R8PBTTR	Digikey	478-2806-1-ND	CAP CERAMIC .8PF 50V 0603 RF SMD
9	1	C20	2.4p	C0603	AVX Corporation	06035J2R4BBTTR	Digikey	478-2815-1-ND	CAP CERAMIC 2.4PF 50V 0603 RFSMD
10	2	C36, C44	12p	C0603	AVX Corporation	C1608C0G1H120J	Digikey	445-1270-1-ND	CAP CER 12PF 50V C0G 5% 0603
11	1	C33	15p	C0603	TDK Corporation	C1608C0G1H150J	Digikey	445-1271-1-ND	CAP CER 15PF 50V C0G 5% 0603
12	2	C35, C41	30p	C0603	Murata Electronics	GRM1885C1H300JA01D	Digikey	490-1414-2-ND	CAP CER 30PF 50V 5% C0G 0603
13	1	C37	33p	C0603	TDK Corporation	C1608C0G1H330J	Digikey	445-1275-2-ND	CAP CER 33PF 50V C0G 5% 0603
14	1	C34	39p	C0603	TDK Corporation	C1608C0G1H390J	Digikey	445-1276-2-ND	CAP CER 39PF 50V C0G 5% 0603
15	2	C45, C46	47p	C0603	TDK Corporation	C1608C0G1H470J	Digikey	445-1277-2-ND	CAP CER 47PF 50V C0G 5% 0603
16	1	C42	68p	C0603	TDK Corporation	C1608C0G1H680J	Digikey	445-1279-2-ND	CAP CER 68PF 50V C0G 5% 0603
17	2	C32, C38	100p	C0603	TDK Corporation	C1608C0G1H101J	Digikey	445-1281-2-ND	CAP CER 100PF 50V C0G 5% 0603
18	1	C43	120p	C0603	TDK Corporation	C1608C0G1H121J	Digikey	445-1282-2-ND	CAP CER 120PF 50V C0G 5% 0603
19	2	F1, F2	LARK_MC1250-60-3MM	MC1250	Lark Engineering Inc	LARK_MC1250-60-3MM	Lark Engineering Inc	LARK_MC1250-60-3MM	LARK FILTER
20	1	F3	TTE_K4938-58/98M-20-1405	TTE20	TTE Inc	TTE_K4938-58/98M-20-1405	TTE Inc	TTE_K4938-58/98M-20-1405	TTE FILTER
21	6	J1, J2, J5, J6, J7, J8	MMCX	MMCX	Emerson	135-3711-201	Digikey	J821-ND	MMCX CONN

Item	Qty	Reference	Part Name	Package	Manufacturer	Mfg. No.	Distributor	Distributor No.	Description
22	1	JP1	9V	1X02	Mill-Max Manufacturing	890-90-036-10-800000	Digikey	89090-03610800000-ND	SQUARE HEAD
23	1	L6	2.2n	0402/0603	Coil Craft	0603CS-2N2X_LU	Coil Craft	0603CS-2N2X_LU	Inductor
24	2	L5, L7	2.7n	0402/0603	Coil Craft	0402CS-2N7X_LU	Coil Craft	0402CS-2N7X_LU	Inductor
25	2	L3, L4	6.8n	0402/0603	Coil Craft	0603CS-6N8X_LU	Coil Craft	0603CS-6N8X_LU	Inductor
26	1	L13	33n	0402/0603	Coil Craft	0603CS-33NX_LU	Coil Craft	0603CS-33NX_LU	Inductor
27	1	L21	36n	0402/0603	Coil Craft	0603CS-36NX_LU	Coil Craft	0603CS-36NX_LU	Inductor
28	2	L12, L14	39n	0402/0603	Coil Craft	0603CS-39NX_LU	Coil Craft	0603CS-39NX_LU	Inductor
29	2	L20	72n	0402/0603	Coil Craft	0603CS-72NX_LU	Coil Craft	0603CS-72NX_LU	Inductor
30	1	L24	82n	0402/0603	Coil Craft	0603CS-82NX_LU	Coil Craft	0603CS-82NX_LU	Inductor
31	1	L10	91n	0402/0603	Coil Craft	0603CS-91NX_LU	Coil Craft	0603CS-91NX_LU	Inductor
32	2	L11, L22	100n	0402/0603	Coil Craft	0603CS-R10X_LU	Coil Craft	0603CS-R10X_LU	Inductor
33	1	L18	150n	0402/0603	Coil Craft	0603CS-R15X_LU	Coil Craft	0603CS-R15X_LU	Inductor
34	1	L23	330n	0402/0603	Coil Craft	0603CS-R33X_LU	Coil Craft	0603CS-R33X_LU	Inductor
35	1	L19	820n	0402/0603	JW Miller	PM1008-R82K-RC	Digikey	M8475CT-ND	INDUCTOR CHIP .82UH 10% SMD
36	2	M1, M2	SYM-11	TTT167	Mini Circuits	SYM-11	Mini Circuits	SYM-11	MIXER
37	4	P1, P2, P3, P4	3	AF320	Mini Circuits	PAT-3	Mini Circuits	PAT-3	PAT
38	1	Q2	ERA-6SM	WW107	Mini Circuits	ERA-6SM	Mini Circuits	ERA-6SM	AMPLIFIER
39	6	Q1, Q3, Q4, Q5, Q6, Q7	ERA-3SM	WW107	Mini Circuits	ERA-3SM	Mini Circuits	ERA-3SM	AMPLIFIER
40	1	R5	56	R2512	Panasonic - ECG	ERJ-1WYJ560U	Digikey	P56XCT-ND	RES 56 OHM 1W 5% 2512 SMD
41	6	R1, R6, R8, R9,R13, R14	160	R2512	Panasonic - ECG	ERJ-1TYJ161U	Digikey	PT160XTR-ND	RES 160 OHM 1W 5% 2512 SMD
42	2	R7, R15	51	R0603	Susumu Co Ltd	RR0816Q-510-D	Digikey	RR08Q51DCT-ND	RES 51 OHM 1/16W .5% 0603 SMD
43	7	U$1, U$2, U$3, U$4, U$5, U$6, U$7	ADCH-80A	CD542	Mini Circuits	ADCH-80A	Mini Circuits	ADCH-80A	RF CHOKE

Appendix E

RF Front End Board

This appendix documents the design of the RF front end (RFFE) board for the VT MMR discussed in Section 7.5.1 ("RFFE Board"). Note that the design of the multiplexer implemented in this board is already described in detail in Section 6.2 ("Multiplexer Design for a Real Antenna"). This appendix documents the design of the rest of the board.

E.1 Board Overview

A block diagram of the RFFE board is shown in Figure 7.14. In this section, Figure E.1 and Table E.1 show the input/output ports of the RFFE board.

A schematic of the multiplexer section including the RF switches, which control the receive/transmit selection, is shown in Figure E.2. Table E.3 shows the receive/transmit switch control signals. Figure E.3 show the schematic of the amplifier section. This figure also contains the circuit diagram of four 5^{th} order Chebyshev bandpass filters, which are connected at the output of the amplifiers, to perform additional filtering. The frequency responses of these filters are shown in Figure E.5.

To control the gain of the received signal, we use a 5-bit digitally–controlled attenuator, Model HMC470LP3 from Hittite Microwave Inc. Figure E.4 shows a schematic of the attenuator section. Table E.2 shows how attenuator control signals are used to request various levels of attenuation.

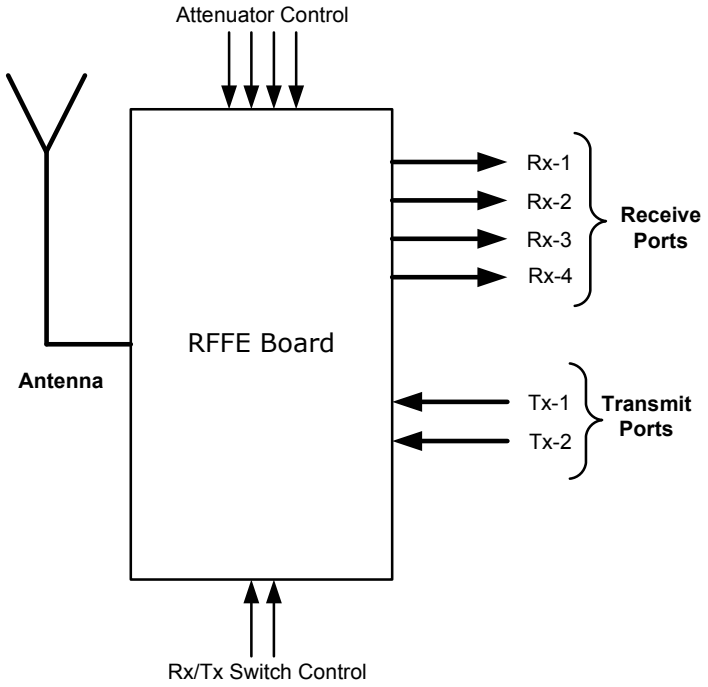


Figure E.1: Summary of input/output ports of the RFFE board.

Table E.1: Description of input/output ports of the RFFE board.

Function	**Port Name**	**Conn. Name**	**Characteristics**
Receive Ports	RX-1	J6	RF Mux Ch-1 receive port
	RX-2	J7	RF Mux Ch-2 receive port
	RX-3	J8	RF Mux Ch-3 receive port
	RX-4	J9	RF Mux Ch-4 receive port
Transmit Ports	TX-1	J2	RF Mux Ch-1 or Ch-2 transmit port
	TX-2	J3	RF Mux Ch-3 or Ch-4 transmit port
Attenuator Control	ATT_CTL	J5	Attenuator control signals
Rx/Tx switch	SW_CTL	J4	Rx/Tx switch control signals

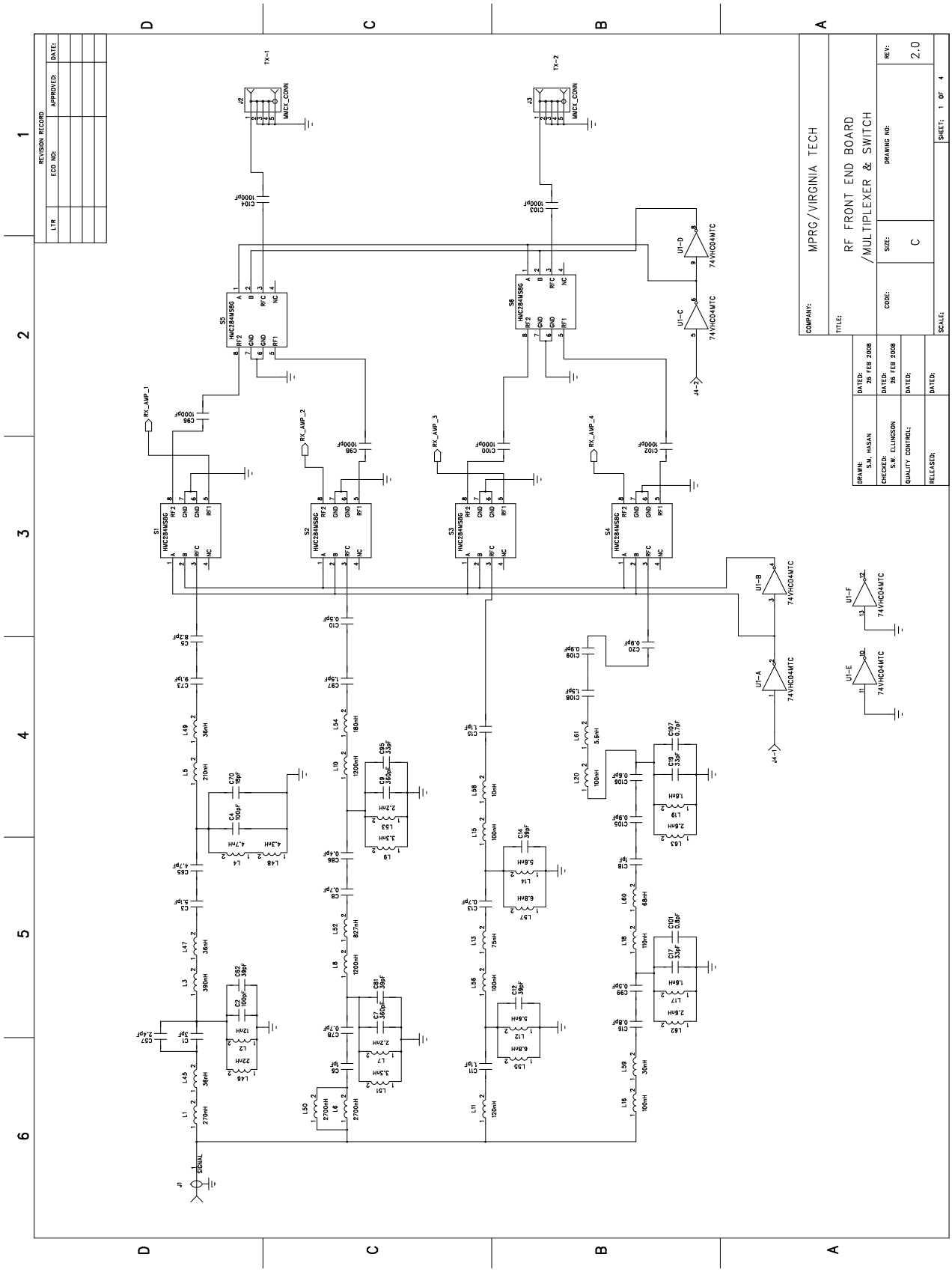


Figure E.2: Schematic of the multiplexer and switch section of the RFFE board.

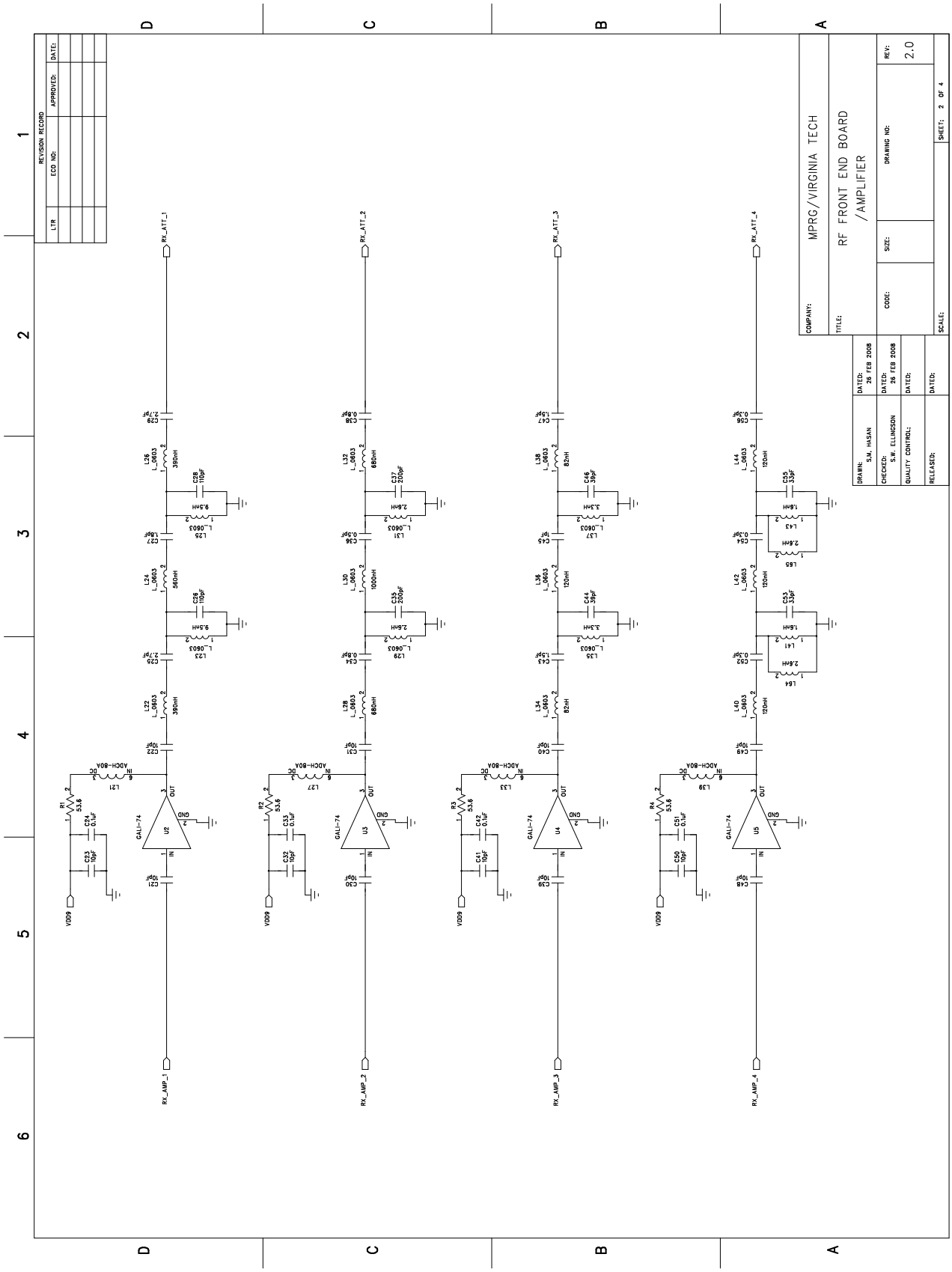


Figure E.3: Schematic of the amplifier section of the RFFE board.

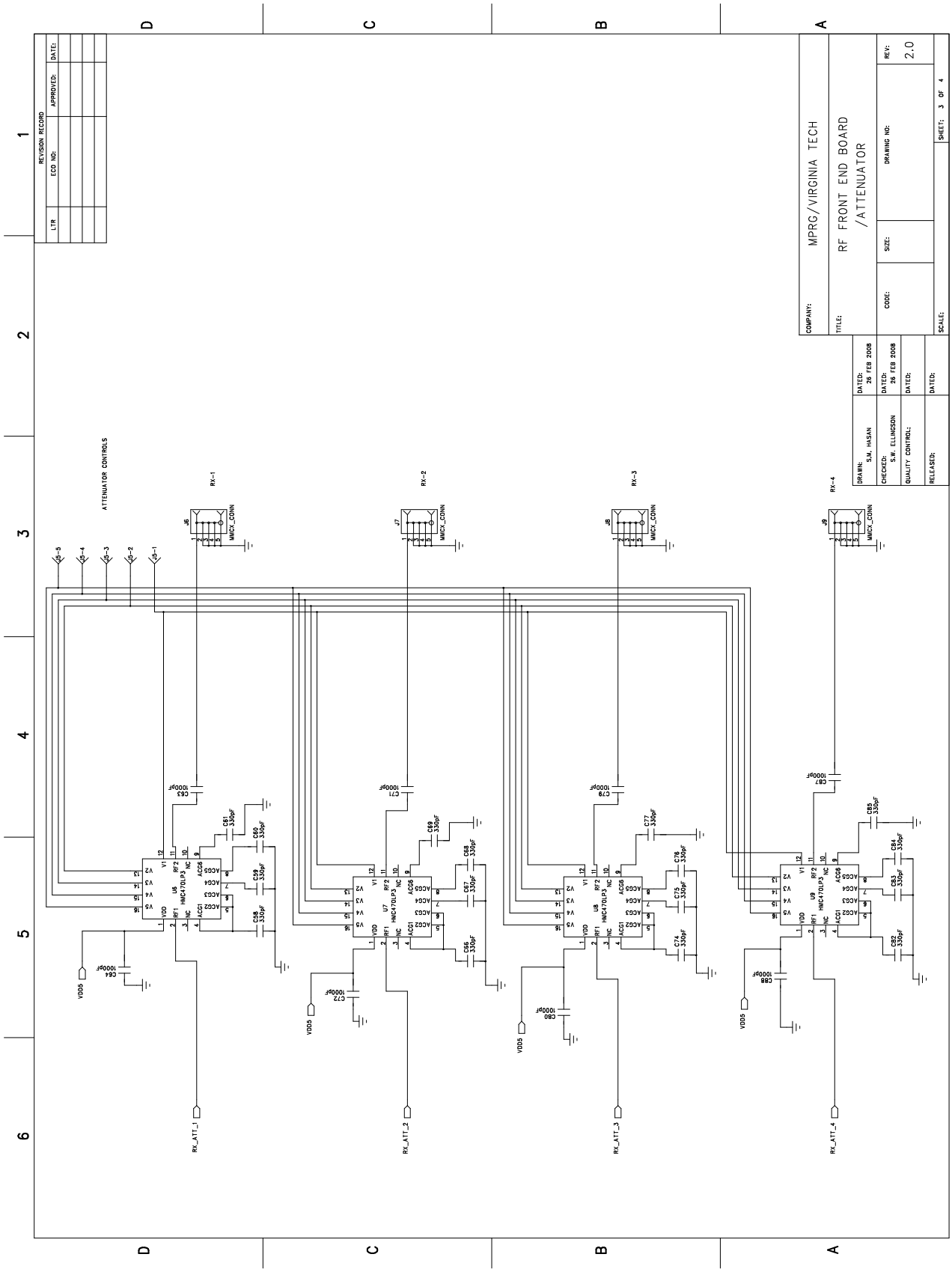


Figure E.4: Schematic of the attenuator section of the RFFE board.

Table E.2: Attenuator control signals in the RFFE board.

V1 16dB	**V2** 8dB	**v3** 4dB	**V4** 2dB	**V5** 1dB	**ATT State**
High	High	High	High	High	Insertion Loss
High	High	High	High	Low	1 dB
High	High	High	Low	High	2 dB
High	High	Low	High	High	4 dB
High	Low	High	High	High	8 dB
Low	High	High	High	High	16 dB
Low	Low	Low	Low	Low	31 dB

Table E.3: Receive/Transmit switch control signals in the RFFE board.

S0	**S1**	**Rx/Tx Mode**
High	X	RX Mode
Low	Low	TX Mode (Ch.1 or Ch.3)
Low	High	TX Mode (Ch.2 or Ch.4)

One 9V supply voltage for amplifiers and one 5V supply voltage for RF switches and attenuators are created from a single 16V power source. Schematics are shown in Figure E.6. This 16V input voltage is fed into a 1.1A low–dropout regulator IC (Model LT1965) to create a 9V positive voltage. The 5V regulated voltage is supplied by the 500 mA low–dropout regulator IC (Model LT763). Both of these regulator ICs are manufactured by Linear Technology Inc[1].

A summary of the cost for one RFFE board is given in Table E.4. Since we prepared just two boards for the present study using the quickest manufacturing time, the PCB fabrication and assembly cost is not representative of the cost to build the same device in large quantities.

E.2 Layout, and Bill of Materials

The PCB layout is shown in Figures E.7 and E.8. Note that since the antenna is connected at the top layer of this board, this layer act as a ground plane for the antenna. For that reason, all other components are placed on the bottom layer of this board. The bill of materials for this board is shown at the end of this appendix.

[1] http://www.linear.com

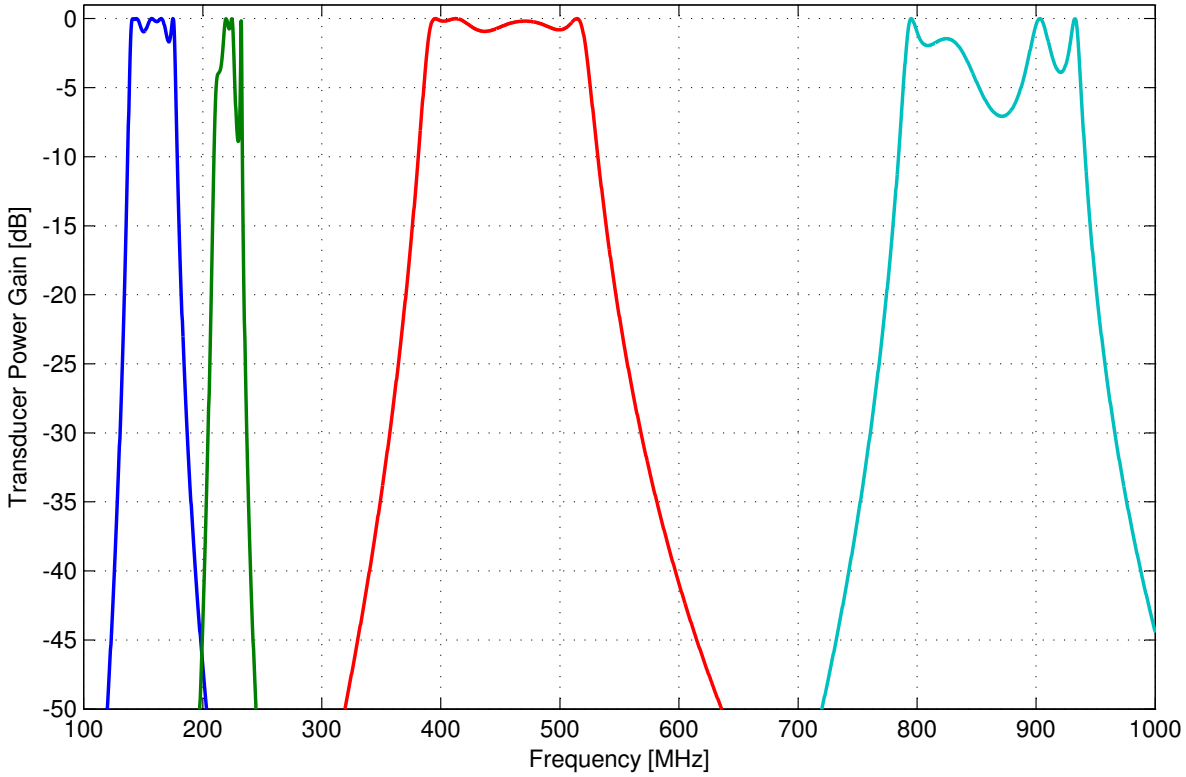


Figure E.5: Frequency responses of the 5^{th} order Chebyshev filters implemented in the RFFE board.

Table E.4: Summary of cost for one RFFE board.

Component	**Quantity**	**Price(US $)**
Regulator ICs	2	8.58
Amplifiers	4	18.80
RF Chokes	4	59.00
Attenuators	4	15.32
RF Switches	6	7.08
Capacitors	109	16.35
Inductors	61	45.75
Resistors	7	1.00
MMCX Connectors	6	60.30
Other Connectors	5	10.00
Other Components	3	3.50
	Subtotal	**245.68**
PC Board	1	450.00
PC Board Assembly	1	925.00
	Total	**1620.68**

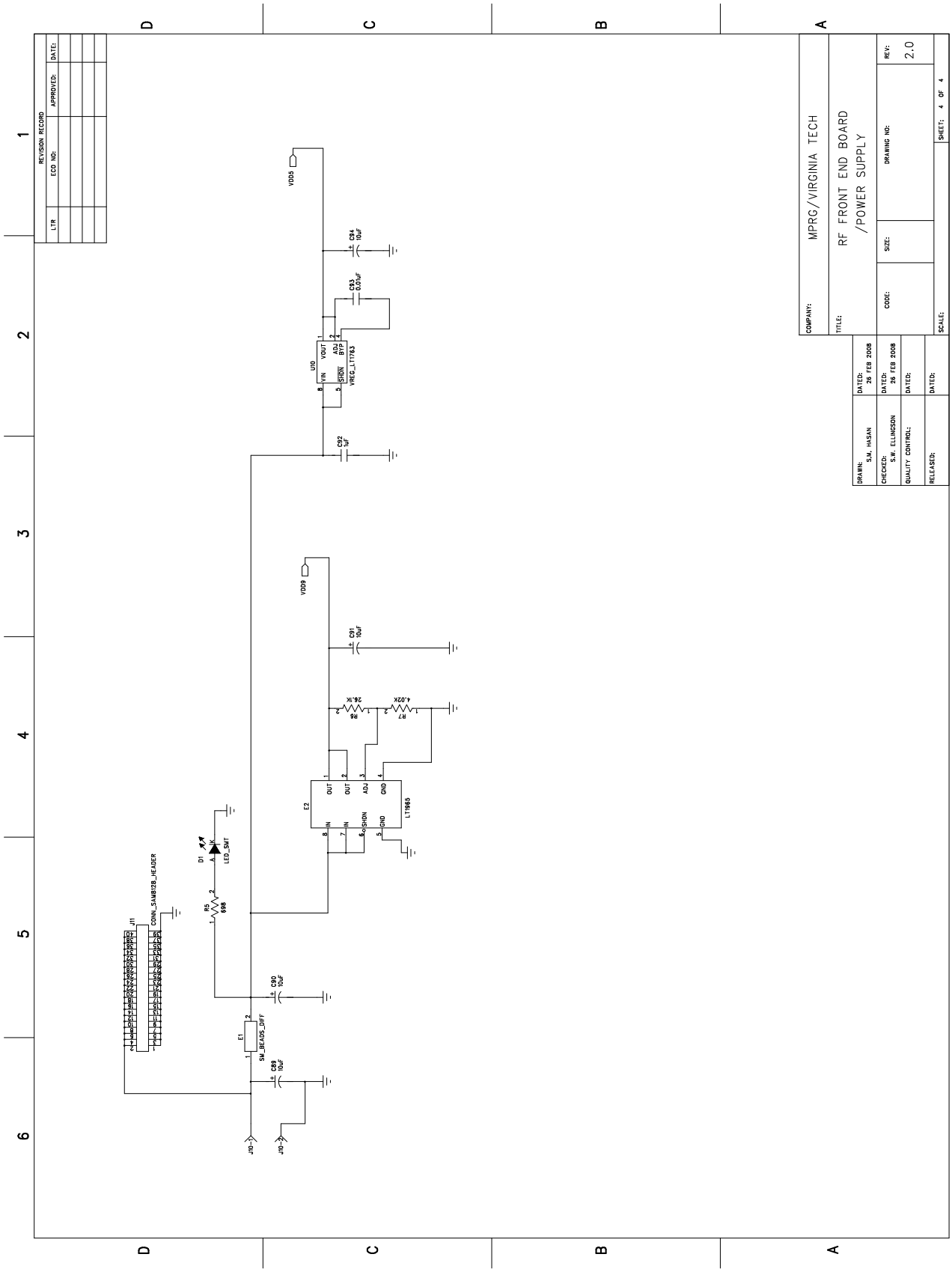


Figure E.6: Schematic of the power supply section of the RFFE board.

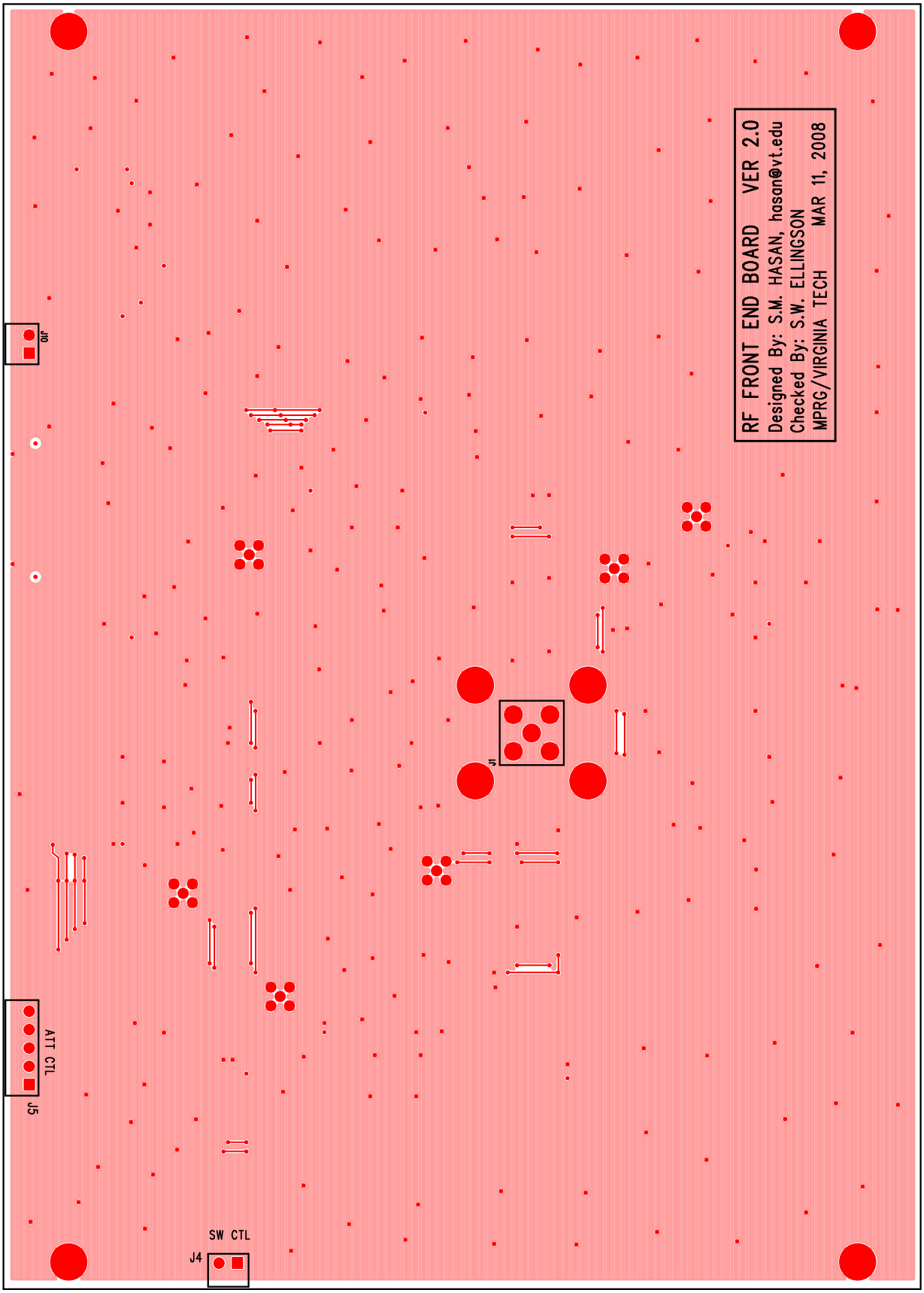


Figure E.7: Top layer (also ground plane for antenna) of the RFFE board.

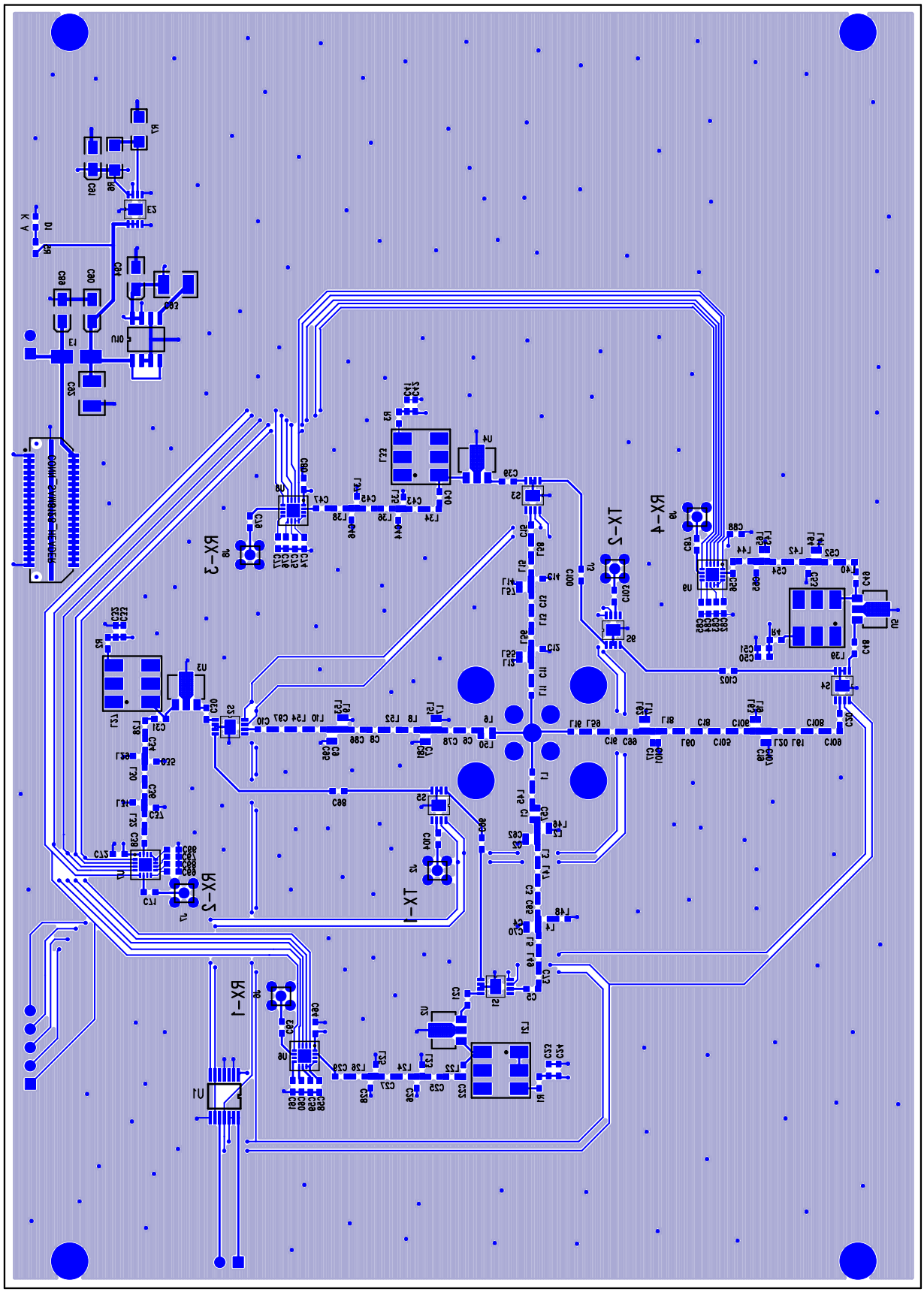


Figure E.8: Bottom layer (component side) of the RFFE board.

Bill of Materials
RFFE Board, Ver.2.0
MPRG/Virginia Tech
Prepared By: S.M. Hasan, Date: MAR 11, 2008

Item	Qty	Reference	Part Name	Package	Manufacturer	Manufacturer Part#	Distributor	Distributor Part#	Description
1	1	U1	74VHCT04AMTC	14-TSSOP	FAIRCHILD	74VHCT04AMTC	Mouser	512-74VHCT04AMTC	HEX INVERTER
2	4	L21 L27 L33 L39	ADCH-80A	CD542	Minicircuits	ADCH-80A+	Minicircuits	ADCH-80A+	RF Choke
3	1	C93	0.01uF 100V	CAP_1210	AVX Corporation	12101C103KAT2A	Digikey	478-1608-1-ND	SURFACE MOUNT CAPACITOR 0.098 X 0.126 INCHES
4	1	C92	1uF 100V	CAP_1210	AVX Corporation	12101C105KAT2A	Digikey	478-2570-1-ND	SURFACE MOUNT CAPACITOR 0.098 X 0.126 INCHES
5	4	C24 C33 C42 C51	0.1uF 50V	CAP_0603	Murata Electronics	GRM188R71H104KA93D	Digikey	490-1519-1-ND	SURFACE MOUNT CAPACITOR 0603 Size
6	3	C52 C54 C56	0.3pF 50V	CAP_0603	AVX Corporation	06035J0R3PBTTR	Digikey	478-2801-1-ND	SURFACE MOUNT CAPACITOR 0603 Size
7	1	C86	0.4pF 250V	CAP_0603	AVX Corporation	SQCSVA0R4BAT1A	Digikey	478-3483-1-ND	SURFACE MOUNT CAPACITOR 0603 Size
8	3	C10 C36 C99	0.5pF 100V	CAP_0603	Murata Electronics	GQM1885C2AR50CB01D	Digikey	490-3551-1-ND	SURFACE MOUNT CAPACITOR 0603 Size
9	1	C106	0.6pF 250V	CAP_0603	AVX Corporation	SQCSVA0R6BAT1A	Digikey	478-3484-1-ND	SURFACE MOUNT CAPACITOR 0603 Size
10	4	C8 C13 C78 C107	0.7pF 50V	CAP_0603	AVX Corporation	06035J0R7PBSTR	Digikey	478-4445-1-ND	SURFACE MOUNT CAPACITOR 0603 Size
11	4	C16 C34 C38 C101	0.8pF 250V	CAP_0603	AVX Corporation	SQCSVA0R8BAT1A	Digikey	478-3485-1-ND	SURFACE MOUNT CAPACITOR 0603 Size
12	3	C20 C105 C109	0.9pF 50V	CAP_0603	AVX Corporation	06035J0R9PBTTR	Digikey	478-2807-1-ND	SURFACE MOUNT CAPACITOR 0603 Size
13	2	C11 C15	1.1pF 250V	CAP_0603	AVX Corporation	SQCSVA1R1BAT1A	Digikey	478-3487-1-ND	SURFACE MOUNT CAPACITOR 0603 Size
14	4	C43 C47 C97 C108	1.5pF 250V	CAP_0603	AVX Corporation	SQCSVA1R5BAT1A	Digikey	478-3489-1-ND	SURFACE MOUNT CAPACITOR 0603 Size
15	1	C27	1.8pF 250V	CAP_0603	AVX Corporation	SQCSVA1R8BAT1A	Digikey	478-3490-1-ND	SURFACE MOUNT CAPACITOR 0603 Size
16	14	C63-64 C71-72 C79-80 C87-88 C96 C98 C100 C102-104	1000pF 50V	CAP_0603	AVX Corporation	06035C102KAT2A	Digikey	478-1215-1-ND	SURFACE MOUNT CAPACITOR 0603 Size
17	2	C2 C4	100pF 50V	CAP_0603	AVX Corporation	06035A101KAT2A	Digikey	478-3717-1-ND	SURFACE MOUNT CAPACITOR 0603 Size
18	12	C21-23 C30-32 C39-41 C48-50	10pF 250V	CAP_0603	AVX Corporation	SQCSVA100JAT1A	Digikey	478-3502-1-ND	SURFACE MOUNT CAPACITOR 0603 Size
19	2	C26 C28	110pF 100V	CAP_0603	Murata Electronics	GRM1885C2A111JA01D	Digikey	490-1352-1-ND	SURFACE MOUNT CAPACITOR 0603 Size
20	1	C70	18pF 250V	CAP_0603	AVX Corporation	SQCSVA180JAT1A	Digikey	478-3505-1-ND	SURFACE MOUNT CAPACITOR 0603 Size
21	3	C6 C18 C45	1pF 250V	CAP_0603	AVX Corporation	SQCSVA1R0BAT1A	Digikey	478-3486-1-ND	SURFACE MOUNT CAPACITOR 0603 Size

Item	Qty	Reference	Part Name	Package	Manufacturer	Manufacturer Part#	Distributor	Distributor Part#	Description
22	1	C57	2.4pF 250V	CAP_0603	AVX Corporation	SQCSVA2R4BAT1A	Digikey	478-3493-1-ND	SURFACE MOUNT CAPACITOR 0603 Size
23	2	C25 C29	2.7pF 250V	CAP_0603	AVX Corporation	SQCSVA2R7BAT1A	Digikey	478-3494-1-ND	SURFACE MOUNT CAPACITOR 0603 Size
24	2	C35 C37	200pF 100V	CAP_0603	Murata Electronics	GRM1885C2A201JA01D	Digikey	490-1358-1-ND	SURFACE MOUNT CAPACITOR 0603 Size
25	16	C58-61 C66-69 C74-77 C82-85	330pF 50V	CAP_0603	Panasonic	ECJ-1VC1H331J	Digikey	PCC331ACVCT-ND	SURFACE MOUNT CAPACITOR 0603 Size
26	5	C17 C19 C53 C55 C95	33pF 250V	CAP_0603	AVX Corporation	SQCSVA330JAT1A	Digikey	478-3511-1-ND	SURFACE MOUNT CAPACITOR 0603 Size
27	2	C7 C9	360pF 100V	CAP_0603	Murata Electronics	GRM1885C2A361JA01D	Digikey	490-1364-1-ND	SURFACE MOUNT CAPACITOR 0603 Size
28	6	C12 C14 C44 C46 C62 C81	39pF 250V	CAP_0603	AVX Corporation	SQCSVA390JAT1A	Digikey	478-3512-1-ND	SURFACE MOUNT CAPACITOR 0603 Size
29	1	C1	3pF 250V	CAP_0603	AVX Corporation	SQCSVA3R0BAT1A	Digikey	478-3495-1-ND	SURFACE MOUNT CAPACITOR 0603 Size
30	1	C65	4.7pF 250V	CAP_0603	AVX Corporation	SQCSVA4R7CAT1A	Digikey	478-3498-1-ND	SURFACE MOUNT CAPACITOR 0603 Size
31	1	C3	5.1pF 100V	CAP_0603	Murata Electronics	GQM1885C2A5R1CB01D	Digikey	490-3559-1-ND	SURFACE MOUNT CAPACITOR 0603 Size
32	1	C5	8.2pF 250V	CAP_0603	AVX Corporation	SQCSVA8R2CAT1A	Digikey	478-3501-1-ND	SURFACE MOUNT CAPACITOR 0603 Size
33	1	C73	9.1pF 50V	CAP_0603	Murata Electronics	GQM1885C1H9R1CB01D	Digikey	490-3569-1-ND	SURFACE MOUNT CAPACITOR 0603 Size
34	4	C89-91 C94	10uF 16V	CAP_3216	Rohm	TCA1C106M8R	Digikey	511-1473-1-ND	CAP TANTALUM
35	1	J11	CONN_SAM8128_HEADER	Plug	Samtec Inc	QTE-020-01-X-D-A	Digikey	SAM8128-ND	HIGH SPEED HEADER 40 PINS
36	1	J1	CONN_RPSMA-THROUGH	SMA	Linx Technologies	CONREVSMA001	Digikey	CONREVSMA001-ND	SMA Through Hole Connector
37	4	U2-5	GALI-74	DF782	Mincircuits	GALI-74+	Minicircuits	GALI-74+	Monolithic Amplifier
38	6	S1-6	HMC284MS8G	MS8G	HITTITE	HMC284MS8G	HITTITE	HMC284MS8G	RF SWITHC
39	4	U6-9	HMC470LP3	LP3	HITTITE	HMC470LP3	HITTITE	HMC470LP3	5 BIT DIGITAL ATTENUATOR
40	1	D1	LED_SMT	SMT	LITE-ON	LTST-C190GKT	Digikey	160-1183-1-ND	LIGHT EMITTING DIODE
41	1	E2	LT1965	MSOP8G	LINEAR TECHNOLOGY	LT1965	Digikey	LT1965IMS8E#PBF-ND	LINEAR LDO REGULATOR
42	4	L17 L19 L41 L43	1.6nH	L_0603	Coilcraft	0603CS-1N6X_LU	Coilcraft	0603CS-1N6X_LU	Surface Mount Inductor 0603 Size
43	1	L30	1000nH	L_0603	Coilcraft	0603LS-102X_LB	Coilcraft	0603LS-102X_LB	Surface Mount Inductor 0603 Size
44	4	L15-16 L20 L56	100nH	L_0603	Coilcraft	0603CS-R10X_LU	Coilcraft	0603CS-R10X_LU	Surface Mount Inductor 0603 Size
45	1	L58	10nH	L_0603	Coilcraft	0603CS-10NX_LU	Coilcraft	0603CS-10NX_LU	Surface Mount Inductor 0603 Size
46	1	L18	110nH	L_0603	Coilcraft	0603CS-R11X_LU	Coilcraft	0603CS-R11X_LU	Surface Mount Inductor 0603 Size
47	2	L8 L10	1200nH	L_0603	Coilcraft	0603LS-122X_LB	Coilcraft	0603LS-122X_LB	Surface Mount Inductor 0603 Size
48	5	L11 L36 L40 L42 L44	120nH	L_0603	Coilcraft	0603CS-R12X_LU	Coilcraft	0603CS-R12X_LU	Surface Mount Inductor 0603 Size

Item	Qty	Reference	Part Name	Package	Manufacturer	Manufacturer Part#	Distributor	Distributor Part#	Description
49	1	L2	12nH	L_0603	Coilcraft	0603CS-12NX_LU	Coilcraft	0603CS-12NX_LU	Surface Mount Inductor 0603 Size
50	1	L54	180nH	L_0603	Coilcraft	0603CS-R18X_LU	Coilcraft	0603CS-R18X_LU	Surface Mount Inductor 0603 Size
51	2	L7 L53	2.2nH	L_0603	Coilcraft	0603CS-2N2X_LU	Coilcraft	0603CS-2N2X_LU	Surface Mount Inductor 0603 Size
52	6	L29 L31 L62-65	2.6nH	L_0603	Coilcraft	0604HQ-2N6XJLB	Coilcraft	0604HQ-2N6XJLB	Surface Mount Inductor 0603 Size
53	1	L5	210nH	L_0603	Coilcraft	0603HP-R21X_LU	Coilcraft	0603HP-R21X_LU	Surface Mount Inductor 0603 Size
54	1	L46	22nH	L_0603	Coilcraft	0603CS-22NX_LU	Coilcraft	0603CS-22NX_LU	Surface Mount Inductor 0603 Size
55	2	L6 L50	2700nH	L_0603	Coilcraft	0603LS-272X_LB	Coilcraft	0603LS-272X_LB	Surface Mount Inductor 0603 Size
56	1	L1	270nH	L_0603	Coilcraft	0603HP-R27X_LU	Coilcraft	0603HP-R27X_LU	Surface Mount Inductor 0603 Size
57	4	L9 L35 L37 L51	3.3nH	L_0603	Coilcraft	0603HP-3N3X_LU	Coilcraft	0603HP-3N3X_LU	Surface Mount Inductor 0603 Size
58	1	L59	30nH	L_0603	Coilcraft	0603HP-30NX_LU	Coilcraft	0603HP-30NX_LU	Surface Mount Inductor 0603 Size
59	3	L45 L47 L49	36nH	L_0603	Coilcraft	0603HP-36NX_LU	Coilcraft	0603HP-36NX_LU	Surface Mount Inductor 0603 Size
60	3	L3 L22 L26	390nH	L_0603	Coilcraft	0603CS-R39X_LU	Coilcraft	0603CS-R39X_LU	Surface Mount Inductor 0603 Size
61	1	L48	4.3nH	L_0603	Coilcraft	0603HP-4N3X_LU	Coilcraft	0603HP-4N3X_LU	Surface Mount Inductor 0603 Size
62	1	L4	4.7nH	L_0603	Coilcraft	0603HP-4N7X_LU	Coilcraft	0603HP-4N7X_LU	Surface Mount Inductor 0603 Size
63	3	L12 L14 L61	5.6nH	L_0603	Coilcraft	0603HP-5N6X_LU	Coilcraft	0603HP-5N6X_LU	Surface Mount Inductor 0603 Size
64	1	L24	560nH	L_0603	Coilcraft	0603LS-561X_LB	Coilcraft	0603LS-561X_LB	Surface Mount Inductor 0603 Size
65	2	L55 L57	6.8nH	L_0603	Coilcraft	0603HP-6N8X_LU	Coilcraft	0603HP-6N8X_LU	Surface Mount Inductor 0603 Size
66	2	L28 L32	680nH	L_0603	Coilcraft	0603LS-681X_LB	Coilcraft	0603LS-681X_LB	Surface Mount Inductor 0603 Size
67	1	L60	68nH	L_0603	Coilcraft	0603HP-68NX_LU	Coilcraft	0603HP-68NX_LU	Surface Mount Inductor 0603 Size
68	1	L13	75nH	L_0603	Coilcraft	0603HP-75NX_LU	Coilcraft	0603HP-75NX_LU	Surface Mount Inductor 0603 Size
69	1	L52	827nH	L_0603	Coilcraft	0603LS-821X_LB	Coilcraft	0603LS-821X_LB	Surface Mount Inductor 0603 Size
70	2	L34 L38	82nH	L_0603	Coilcraft	0603HP-82NX_LU	Coilcraft	0603HP-82NX_LU	Surface Mount Inductor 0603 Size
71	2	L23 L25	9.5nH	L_0603	Coilcraft	0603HP-9N5X_LU	Coilcraft	0603HP-9N5X_LU	Surface Mount Inductor 0603 Size
72	6	J2-3 J6-9	MMCX_PLUG	MMCX	Emerson	135-3801-201	Digikey	J601-ND	MMCX CONNECTOR
73	2	J4 J10	RA_SINGLEHEADER_2PIN	Male Header	TYCO	87232-2	Digikey	A28764-ND	2-Pin R/A Single Row Header

Item	Qty	Reference	Part Name	Package	Manufacturer	Manufacturer Part#	Distributor	Distributor Part#	Description
74	1	J5	RA_SINGLEHEADER_5PIN	Male Header	TYCO	87232-5	Digikey	A28770-ND	5-Pin R/A Single Row Header
75	4	R1-4	53.6 1/10W	RES_0603	Panasonic	ERJ-3EKF53R6V	Digikey	P53.6HCT-ND	SURFACE MOUNT RESISTOR 0603 Size
76	1	R5	698 1/10W	RES_0603	Rohm	MCR03EZPFX6980	Digikey	RHM698HCT-ND	SURFACE MOUNT RESISTOR 0603 Size
77	1	R6	26.1K 1/4W	RES_1206	Rohm	MCR18EZHF2612	Digikey	RHM26.1KFCT-ND	SURFACE MOUNT RESISTOR 1206 Size
78	1	R7	4.02K 1/14W	RES_1206	Rohm	MCR18EZHF4021	Digikey	RHM4.02KFCT-ND	SURFACE MOUNT RESISTOR 1206 Size
79	1	E1	SM_BEADS_DIFF	SMT	FAIR-RITE PRODUCTS CORP	2743019447	Mouser	623-2743019447LF	SM BEADS DIFFERENTIAL
80	1	U10	REGULATOR	SO-8	Linear Technology	LT1763CS8-5	Digikey	LT1763CS8-5-ND	Linear Regulator

Appendix F

RFIC Board

This appendix documents the design of the RFIC board for the VT MMR discussed in Section 7.5.2 ("RFIC Board").

F.1 Board Overview

Figure F.1 and Table F.1 shows all the input/output ports of the RFIC board. Figure F.2 shows the schematic of the RFIC section. Figures F.3 and F.4 show the schematics of the receiver section of this board.

Schematics of the transmitter section of this board are shown in Figures F.3 and F.5. Similar to the receiver section, the RFIC also provides the transmitter outputs in differential form, which is converted into single-ended using a transformer. TX-1 and TX-2 ports use the M/A-COM ETC4-1T-7 1:4 transformer (frequency range 6 to 1000 MHz). The TX-3 port uses the M/A-COM ETC1.6-4-2-3 1:4 transformer (frequency range 500 to 2500 MHz).

Figure F.6 shows the schematic of the power supply section. The RFIC has several power supply pins which require either 1.2V or 2.5V supply voltage. These supply voltages are created in two steps. First, the main 10V input voltage is fed into the positive regulator IC MC78M05 to create a 5V positive voltage. This 5V voltage is supplied to the input of several voltage regulator ICs TPS76901, which provide the required output voltage of 1.2V or 2.5V.

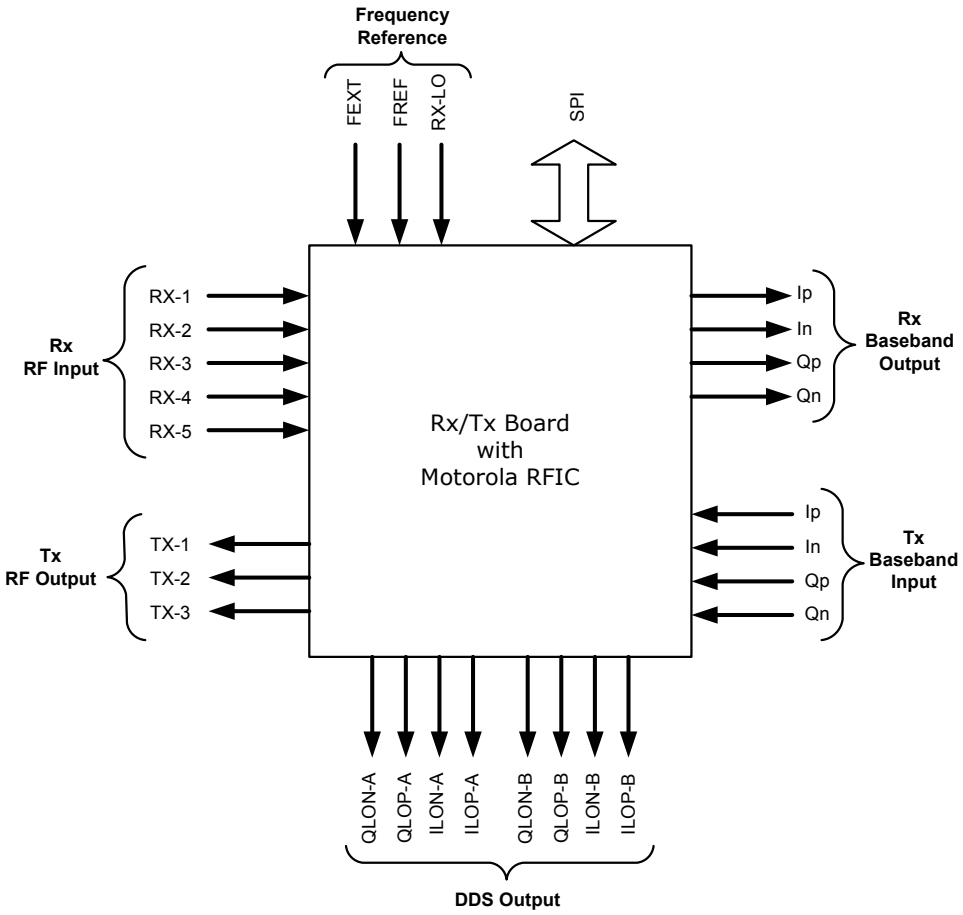


Figure F.1: Summary of input/output ports of the RFIC board.

Table F.1: Description of input/output ports of the RFIC board.

Function	**Port Name**	**Conn. Name**	**Characteristics**
Rx RF Input	RX-1	J61	RF input, 100 MHz to 2.5 GHz
	RX-2	J60	
	RX-3	J59	
	RX-4	J58	
	RX-5	J62	RF input, 500 MHz to 2.5 GHz
Tx RF Output	TX-1	J52	RF Output, 100 MHz to 1000 MHz
	TX-2	J54	
	TX-3	J56	RF Output, 500 MHz to 2.5 GHz
Rx Baseband Output	RX_BB_Ip	J4-A	Baseband in-phase differential signal output
	RX_BB_In	J4-B	
	RX_BB_Qp	J4-C	Baseband quadrature-phase differential signal output
	RX_BB_Qn	J4-D	
Tx Baseband Input	TX_BB_Ip	J3-A	In-phase differential signal max. 2V peak-peak
	TX_BB_In	J3-B	
	TX_BB_Qp	J3-C	Quadrature-phase differential signal max. 2V peak-peak
	TX_BB_Qn	J3-D	
Freq. Reference Input	RX_LO	J12	External LO input to the mixer
	FEXT	J24	1GHz external input used when bypassing the PLL
	FREF	J15	31.25 MHz reference for PLL
DDS Output	QLON-A	J1-A	DDS Rx positive calibration output
	QLOP-A	J1-B	DDS Rx negative calibration output
	ILON-A	J1-C	DDS Tx forward positive calibration output
	ILOP-A	J1-D	DDS Tx forward negative calibration output
	QLON-B	J2-A	DDS Tx feedback positive calibration output
	QLOP-B	J2-B	DDS Tx feedback negative calibration output
	ILON-B	J3-C	DDS Tx feedback differential positive output
	ILOP-B	J3-D	DDS Tx feedback differential negative output
TX AGC Enable	TX_AGC	J7	Transmit AGC enable/disable
RX AGC Enable	RX_AGC	J8	Receive AGC enable/disable
SPI	SPI	J41	serial port interface to PC
Power	PWR	J11	Power Supply Input

Figure F.7 shows the schematic of the SPI section. All the parameters of the RFIC can be controlled using serial port interface (SPI), which consists of five signals - chip select, clock, reset, serial input, and serial output. Octal bus buffer IC MC74LVX244 is used to control the chip select, clock, reset and serial input signals. Serial output signal goes through the inverter IC TC7S04.

A summary of the cost for one RFIC board is given in Table F.2. Since we prepared just two boards for the present study, the PCB fabrication and assembly cost is not representative of the cost to build the same device in large quantities.

Table F.2: Summary of the cost for one RFIC board. (*The cost of the RFIC is a very rough estimate provided by Motorola.)

Component	**Quantity**	**Price(US $)**
Motorola RFIC		70.00*
Other ICs	18	14.40
Capacitors	187	35.70
Inductors	8	6.00
Resistors	73	9.80
MMCX Connectors	15	90.40
Other Connectors	36	51.90
	Subtotal	**278.20**
PCB Board	1	450.00
PCB Board Assembly	1	925.00
	Total	**1653.20**

F.2 Schematic, Layout, and Bill of Materials

Schematics of the RFIC board are shown in Figures F.2 to F.7. The PCB layout of the implemented RFIC board is shown in Figures F.8 to F.10. The bill of materials for this board is shown at the end of this appendix.

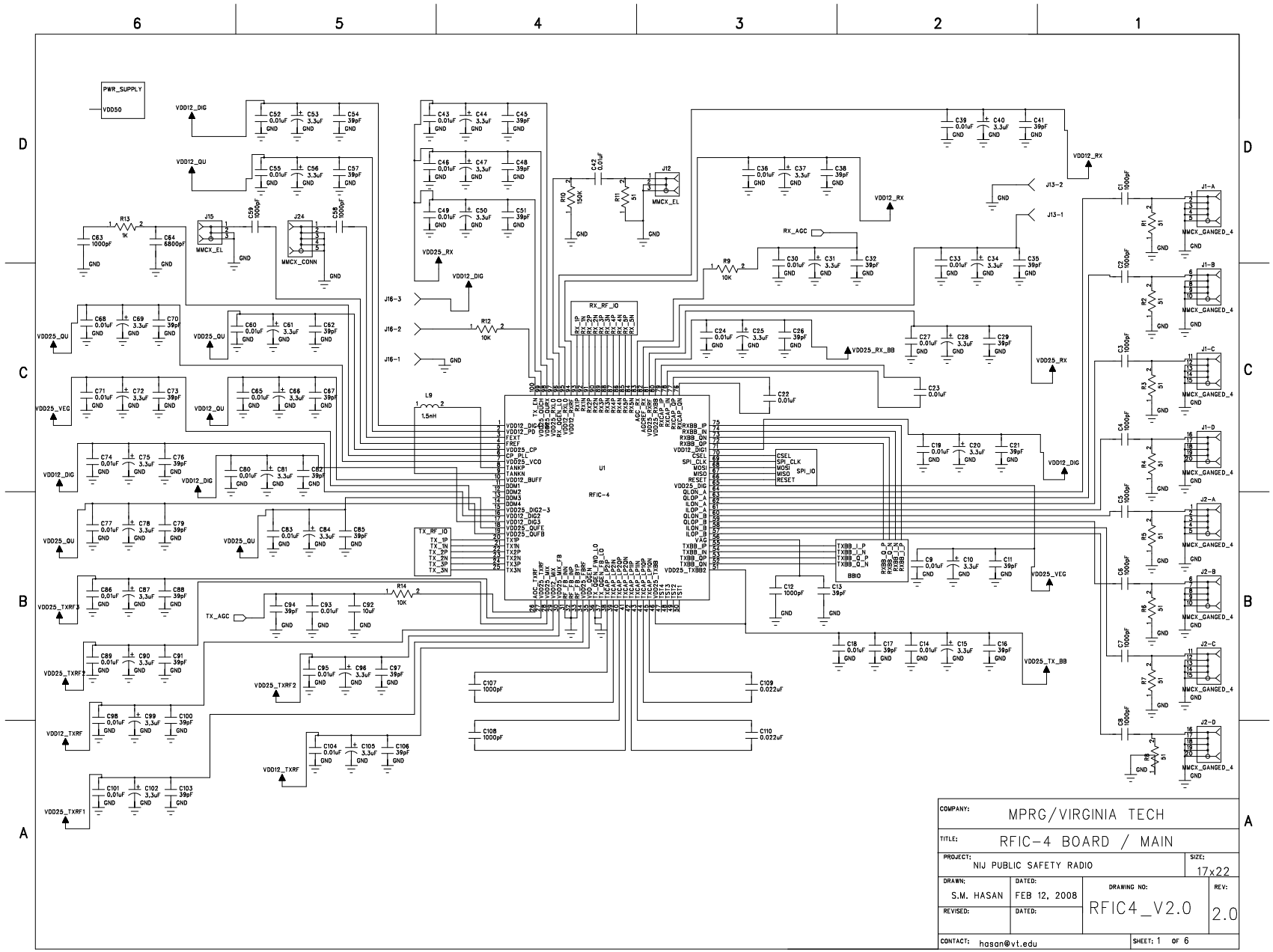


Figure F.2: Schematic of the RFIC section of the RFIC board.

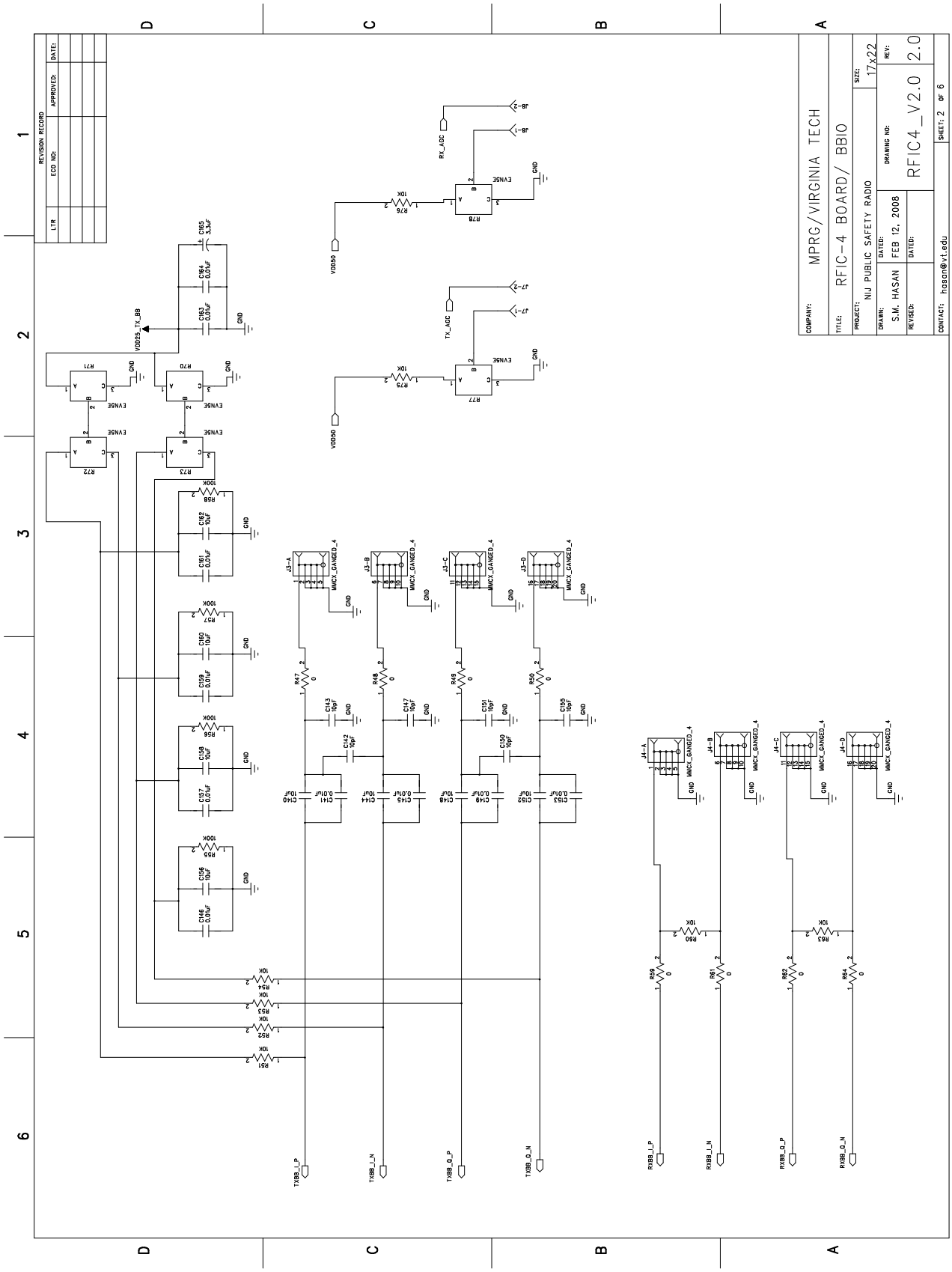


Figure F.3: Schematic of the baseband section of the RFIC board.

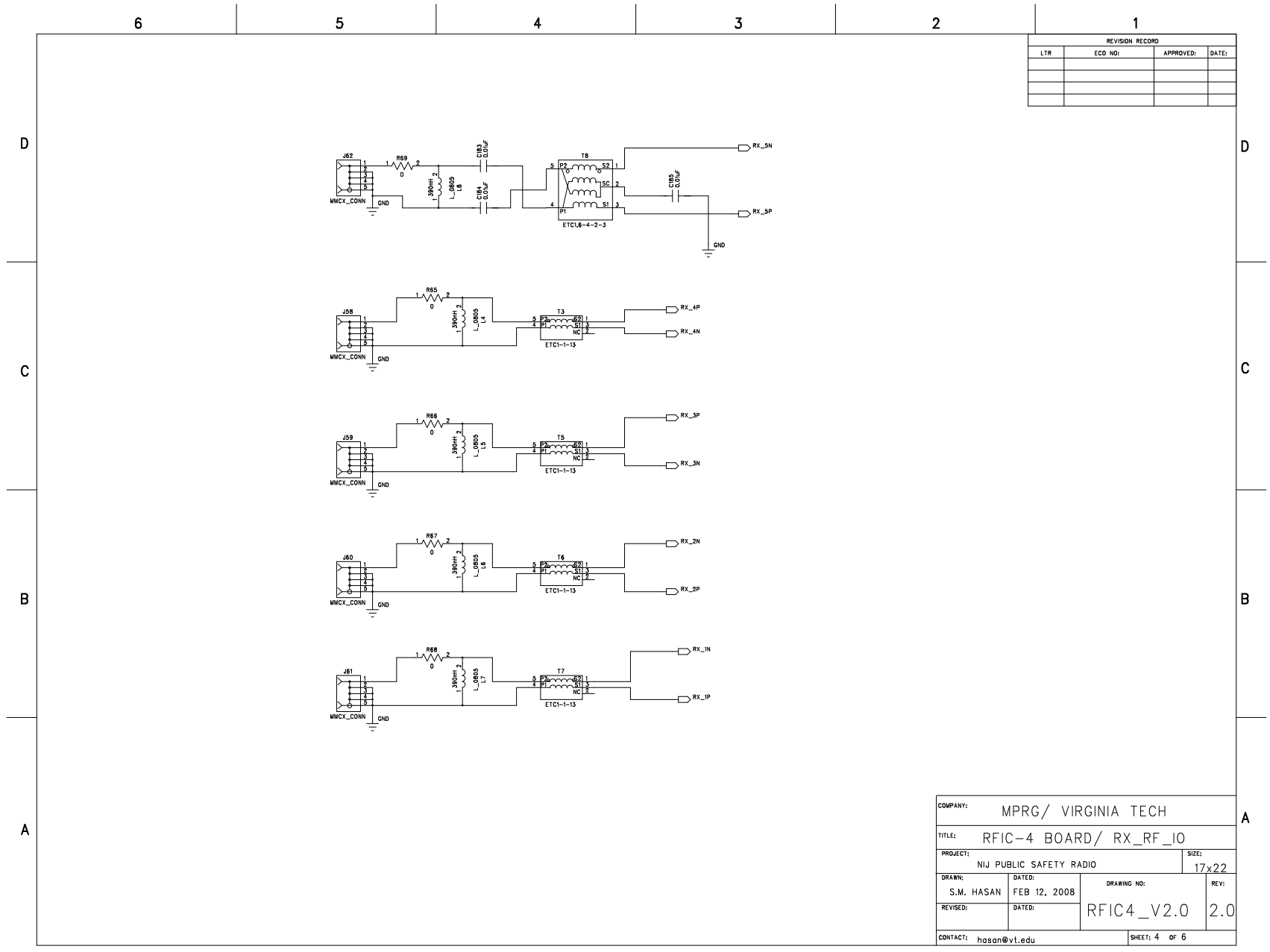


Figure F.4: Schematic of the receiver section of the RFIC board.

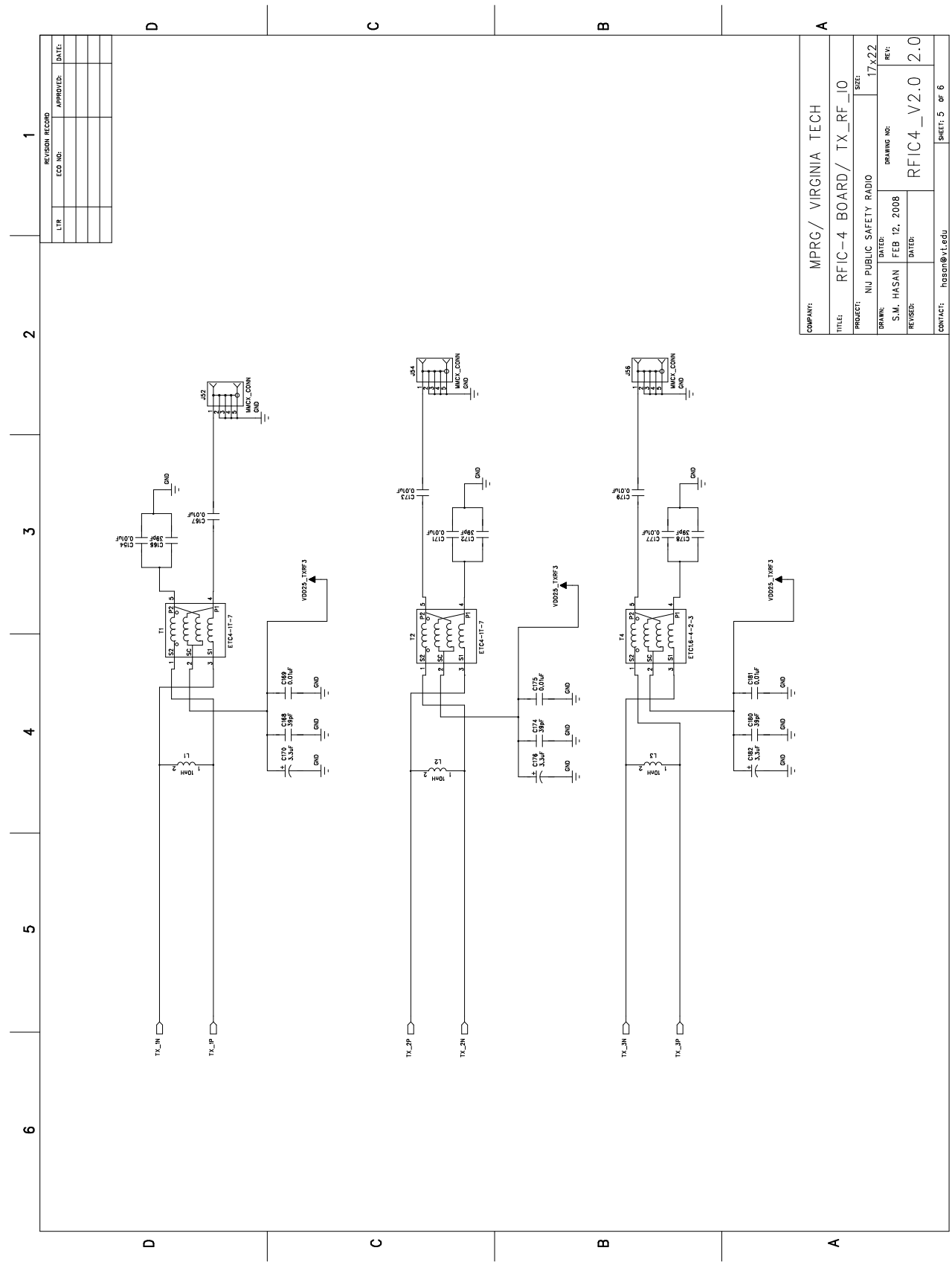


Figure F.5: Schematic of the transmitter section of the RFIC board.

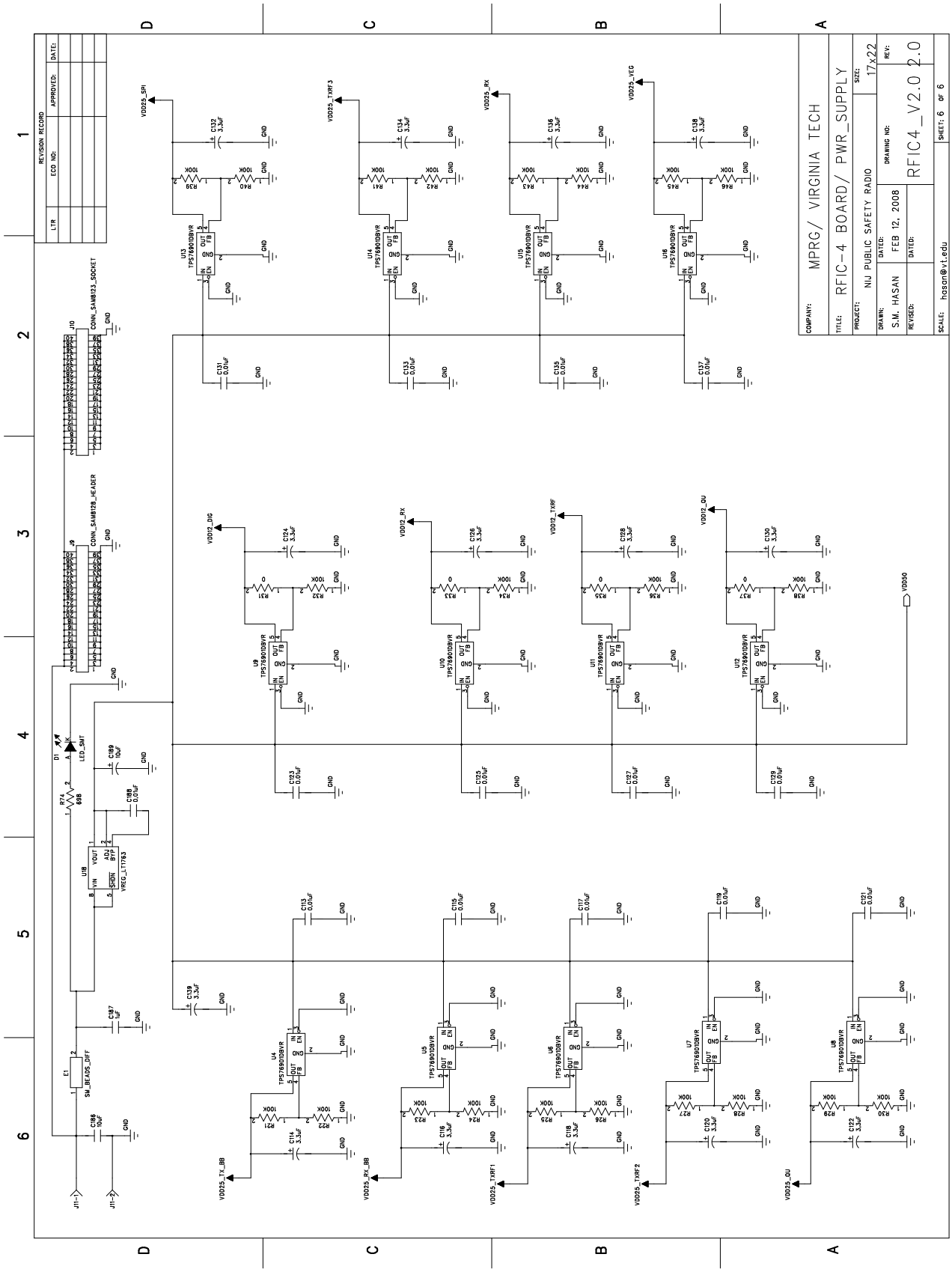


Figure F.6: Schematic of the power supply section of the RFIC board.

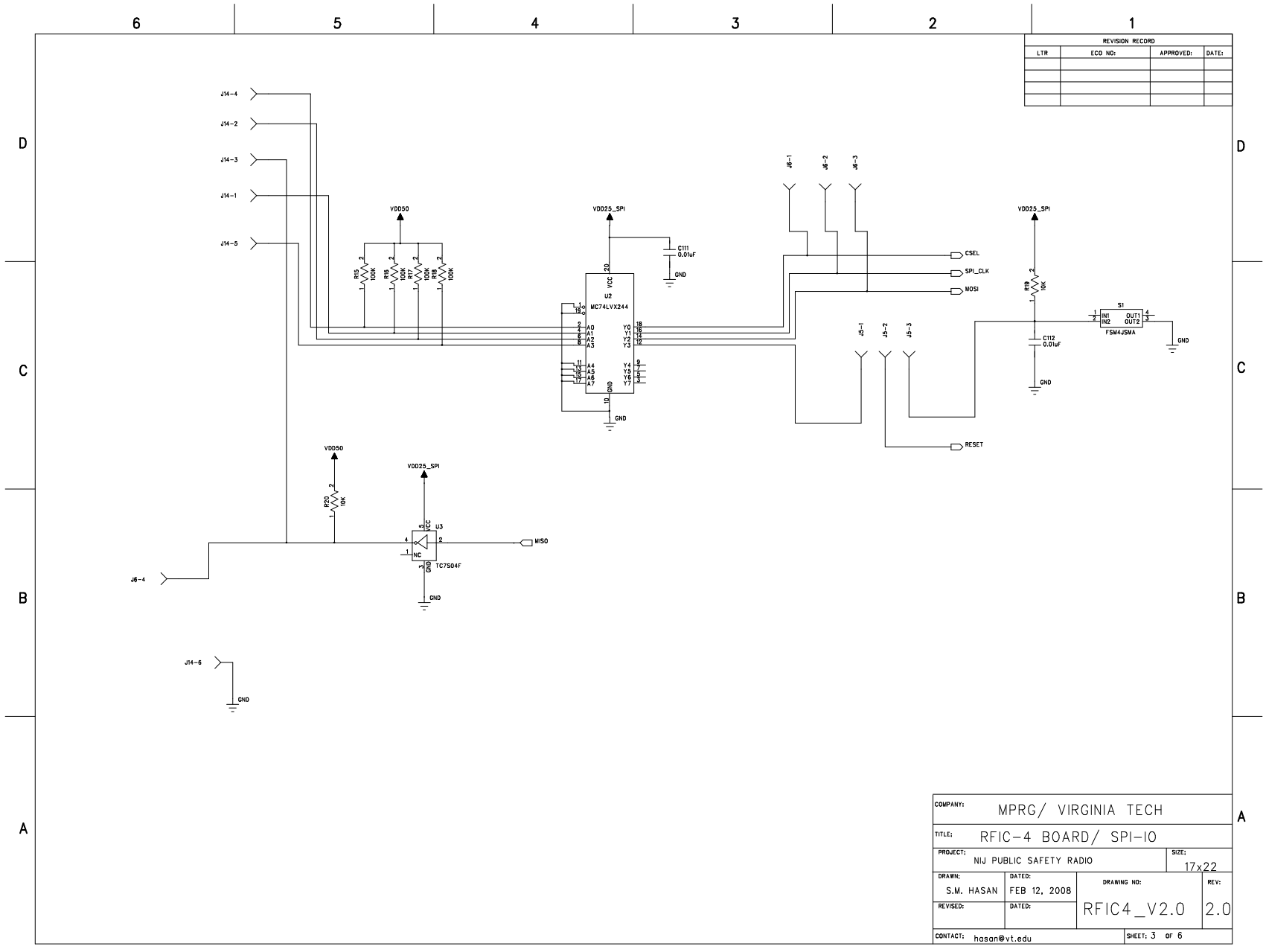


Figure F.7: Schematic of the SPI section of the RFIC board.

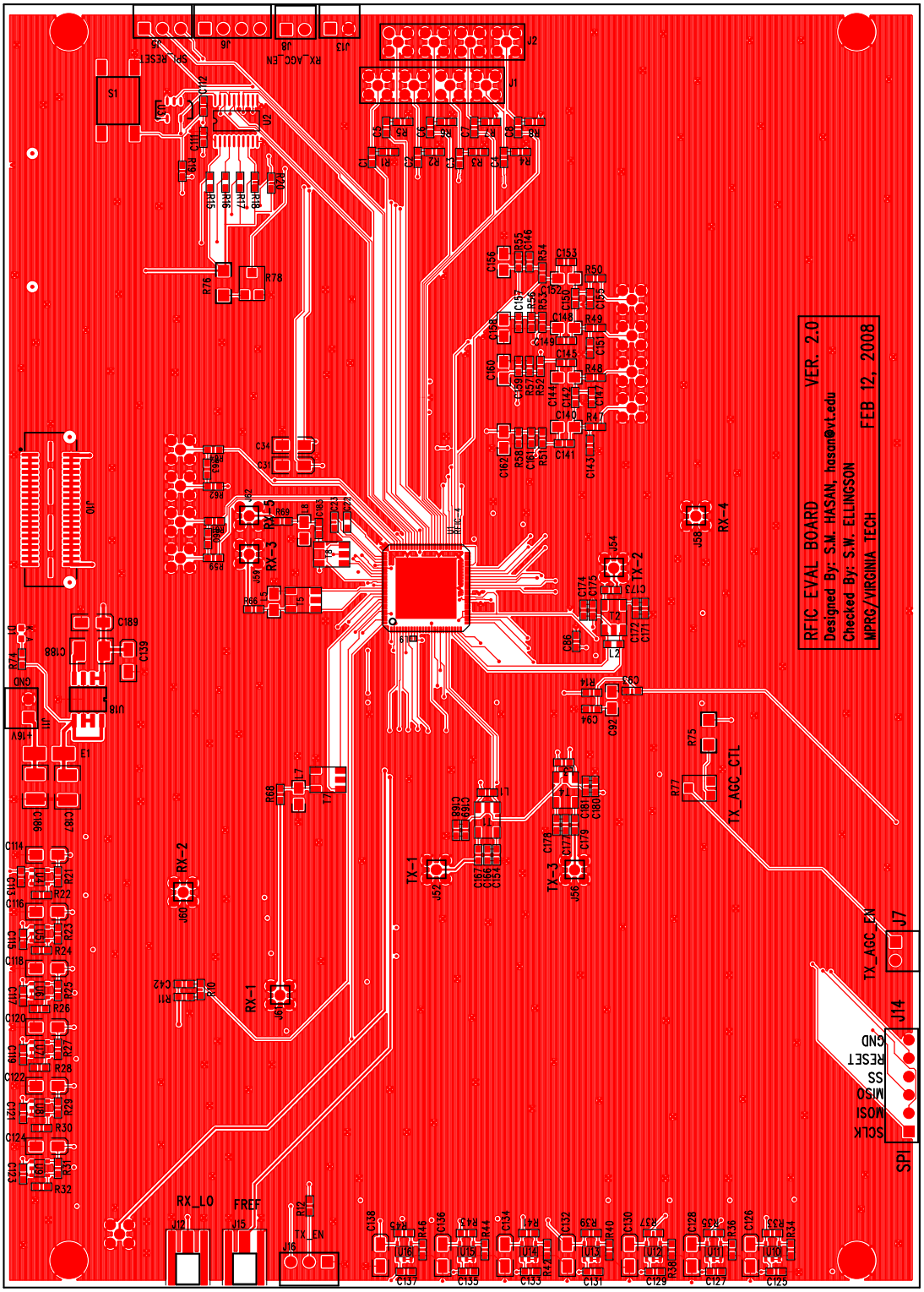


Figure F.8: Top layer of the RFIC board.

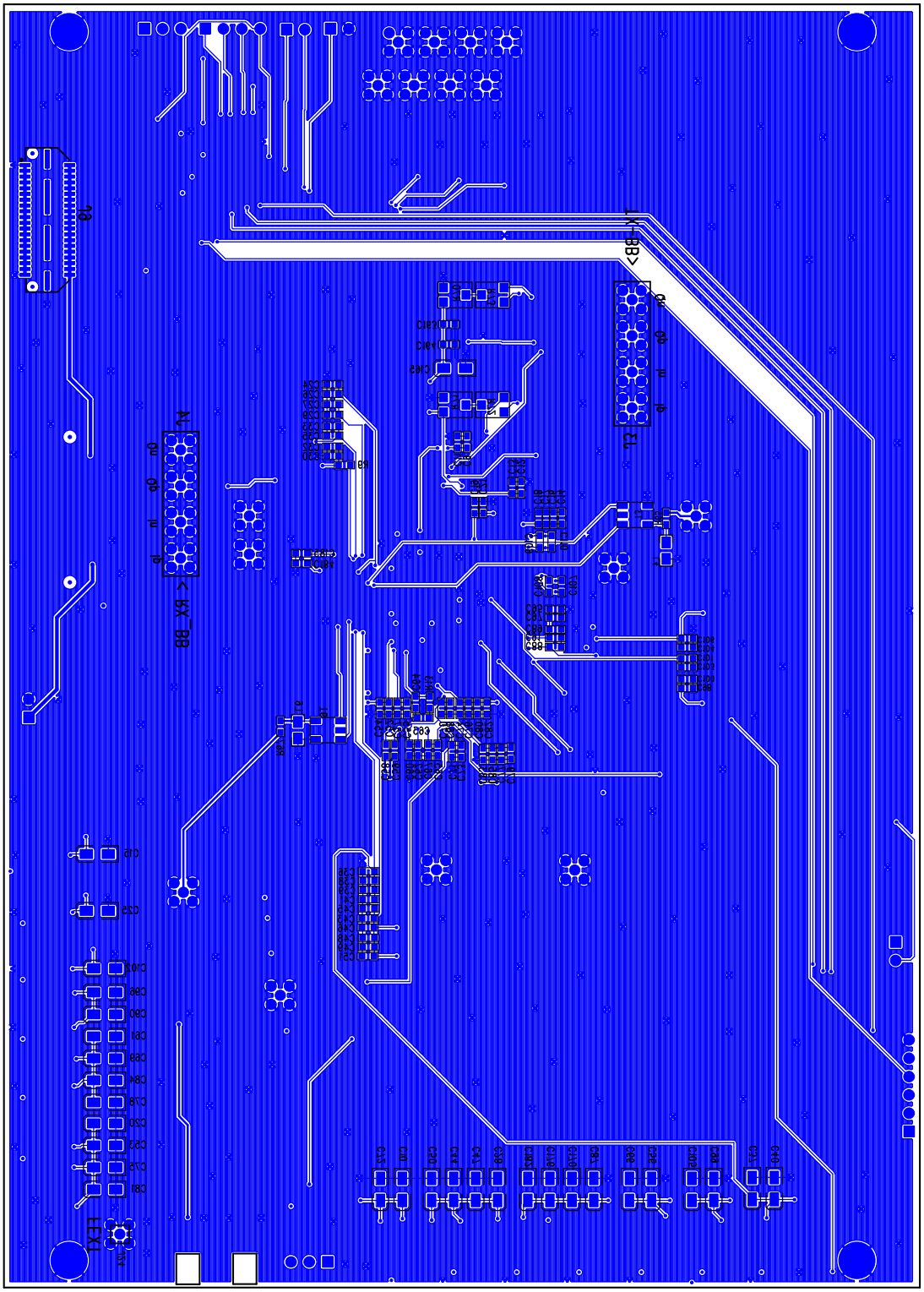


Figure F.9: Bottom layer of the RFIC board.

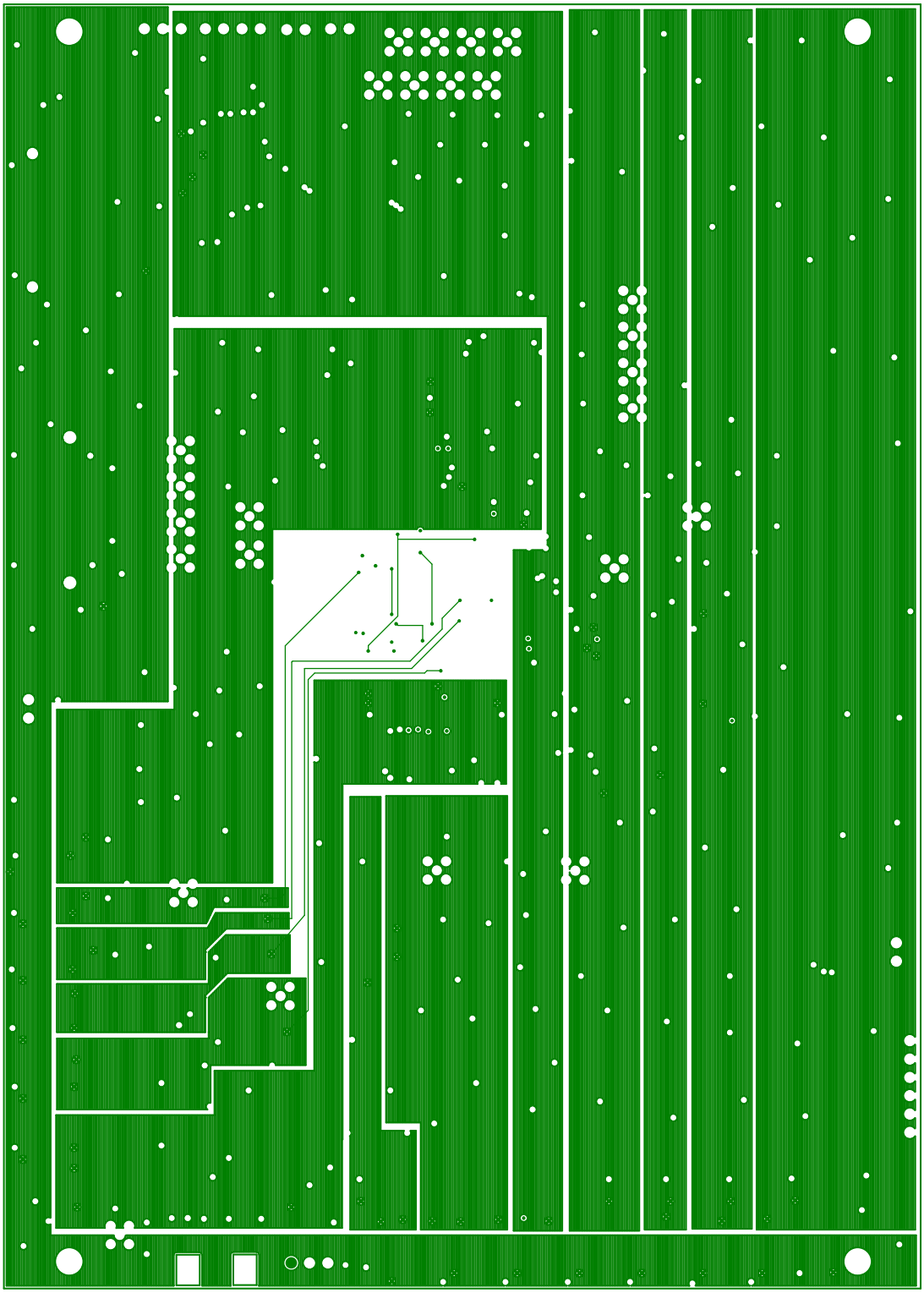


Figure F.10: Power layer of the RFIC board.

Bill of Materials
NIJ RFIC-4 Board, Version 2.0
MPRG/Virginia Tech
Prepared by: SM Hasan, Date: FEB 20, 2008

Item	Qty	Reference	Part Name	Package	Manufacturer	Manufacturer Part#	Distributor	Distributor Part#	Description
1	1	C186	10uF 10V	CAP-1210	Taiyo Yuden	LMK325BJ106KN-T	Digikey	587-1370-1-ND	SURFACE MOUNT CAPACITOR 0.098 X 0.126 INCHES
2	1	C187	1uF 100V	CAP-1210	AVX Corporation	12101C105KAT2A	Digikey	478-2570-1-ND	SURFACE MOUNT CAPACITOR 0.098 X 0.126 INCHES
3	1	C188	0.01uF 100V	CAP-1210	AVX Corporation	12101C103KAT2A	Digikey	478-1608-1-ND	SURFACE MOUNT CAPACITOR 0.098 X 0.126 INCHES
4	70	C9 C14 C18-19 C22-24 C27 C30 C33 C36 C39 C42-43 C46 C49 C52 C55 C60 C65 C68 C71 C74 C77 C80 C83 C86 C89 C93 C95 C98 C101 C104 C111-113 C115 C117 C119 C121 C123 C125 C127 C129 C131 C133 C135 C137 C141 C145-146 C149 C153-154 C157 C159 C161 C163-164 C167 C169 C171 C173 C175 C177 C179 C181 C183-185	0.01uF 50V	CAP-0603	Kemet	C0603C103K5RACTU	Digikey	399-1091-1-ND	SURFACE MOUNT CAPACITOR 0603 Size
5	2	C109-110	0.022uF 16V	CAP-0603	Panasonic ECG	ECJ-1VB1C223K	Digikey	PCC1754CT-ND	SURFACE MOUNT CAPACITOR 0603 Size
6	14	C1-8 C12 C58-59 C63 C107-108	1000pF 50V	CAP-0603	Kemet	C0603C102K5RACTU	Digikey	399-1082-1-ND	SURFACE MOUNT CAPACITOR 0603 Size
7	6	C142-143 C147 C150-151 C155	10pF 50V	CAP-0603	AVX Corporation	06035A100JAT2A	Digikey	478-1163-1-ND	SURFACE MOUNT CAPACITOR 0603 Size
8	37	C11 C13 C16-17 C21 C26 C29 C32 C35 C38 C41 C45 C48 C51 C54 C57 C62 C67 C70 C73 C76 C79 C82 C85 C88 C91 C94 C97 C100 C103 C106 C166 C168 C172 C174 C178 C180	39pF 50V	CAP-0603	AVX Corporation	06035A390JAT2A	Digikey	478-1170-1-ND	SURFACE MOUNT CAPACITOR 0603 Size

Item	Qty	Reference	Part Name	Package	Manufacturer	Manufacturer Part#	Distributor	Distributor Part#	Description
9	1	C64	6800pF 50V	CAP-0603	Panasonic ECG	ECJ-1VB1H682K	Digikey	PCC1782CT-ND	SURFACE MOUNT CAPACITOR 0603 Size
10	9	C92 C140 C144 C148 C152 C156 C158 C160 C162	10uF 6.3V	CAP-0805	AVX Corporation	08056D106KAT2A	Digikey	478-1417-1-ND	SURFACE MOUNT CAPACITOR 0805 Size
11	46	C10 C15 C20 C25 C28 C31 C34 C37 C40 C44 C47 C50 C53 C56 C61 C66 C69 C72 C75 C78 C81 C84 C87 C90 C96 C99 C102 C105 C114 C116 C118 C120 C122 C124 C126 C128 C130 C132 C134 C136 C138-139 C165 C170 C176 C182	3.3uF 6.3V	CAP-3216, TANT	Rohm	TCA0J335M8R	Digikey	511-1440-1-ND	CAP TANTALUM
12	1	C189	10uF 16V	CAP_3216, TANT	Rohm	TCA1C106M8R	Digikey	511-1473-1-ND	CAP TANTALUM
13	1	J10	CONN_SAM8123_SOCKET	Socket	Samtec Inc	QSE-020-01-L-D-A	Digikey	SAM8123-ND	High Speed Socket 40 pins
14	1	J9	CONN_SAM8128_HEADER	Plug	Samtec Inc	QTE-020-01-X-D-A	Digikey	SAM8128-ND	High Speed Plug 40 pins
15	4	T3 T5-7	ETC1-1-13	SM-22	MACOM	ETC1-1-13	Richardson Electronics	ETC1-1-13	TRANSFORMER
16	2	T4 T8	ETC1.6-4-2-3	SM-22	MACOM	ETC1.6-4-2-3	Richardson Electronics	ETC1.6-4-2-3	TRANSFORMER 500-2500 MHz
17	2	T1-2	ETC4-1T-7	SM-22	MACOM	ETC4-1T-7	Richardson Electronics	ETC4-1T-7	TRANSFORMER 6-1000 MHz
18	2	R77-78	Pot 10K	SMD	Panasonic ECG	EVN-5ESX50B14	Digikey	P5E103CT-ND	TRIMMER POTENTIOMETER
19	4	R70-73	Pot 1K	SMD	Panasonic ECG	EVN-5ESX50B13	Digikey	P5E102CT-ND	TRIMMER POTENTIOMETER
20	1	S1	Switch Tact	SMD	Tyco Electronics	FSM4JSMA	Digikey	450-1129-ND	
21	1	D1	LED, Green	SMT	LITE-ON	LTST-C190GKT	Digikey	160-1183-1-ND	LIGHT EMITTING DIODE
22	1	L9	1.5nH	L_0201	Coilcraft	0201CS-1N5XJLU	Coilcraft	0201CS-1N5XJLU	Surface Mount Inductor 0201 Size
23	3	L1-3	10nH	L-0603	Coilcraft	0603CS-10NXJBW	Coilcraft	0603CS-10NXJBW	Surface Mount Inductor 0603 Size
24	5	L4-8	L_0805,390nH	L-0805	Coilcraft	0805CS-391XJBC	Coilcraft	0805CS-391XJBC	Surface Mount Inductor 0805 Size
25	1	U2	MC74LVX244	TSSOP-20	Fairchild Semiconductor	74LVX244MTCX	Digikey	74LVX244MTCXCT-ND	OCTAL BUS BUFFER

Item	Qty	Reference	Part Name	Package	Manufacturer	Manufacturer Part#	Distributor	Distributor Part#	Description
26	8	J52 J54 J56 J58-62	MMCX_JACK	MMCX	Amphenol Connex	262104	Digikey	ACX1275-ND	MMCX CONNECTOR
27	1	J24	MMCX_PLUG	MMCX	Emerson	135-3801-201	Digikey	J601-ND	MMCX CONNECTOR
28	2	J12 J15	MMCX_EL_JACK	MMCX	Johnson Components	135-3711-801	Digikey	J603-ND	END LAUNCH MMCX JACK
29	2	J1-2	MMCX_GANG_JACK	MMCX	Samtec Inc	GRF1-J-P-04-E-ST-TH1	Digikey	SAM8069-ND	MMCX GANGED JACK
30	2	J3-4	MMCX_GANG_PLUG	MMCX	Samtec Inc	GRF1-P-P-04-E-ST-TH1	Digikey	SAM8076-ND	MMCX GANGED PLUG
31	4	J7-8 J11 J13	RA_SINGLEHEADER_2PIN	Male Header	Tyco Electronics	87232-2	Digikey	A28764-ND	R/A HEADER
32	2	J5 J16	RA_SINGLEHEADER_3PIN	Male Header	Tyco Electronics	87232-3	Digikey	A28766-ND	R/A HEADER
33	1	J6	RA_SINGLEHEADER_4PIN	Male Header	Tyco Electronics	87232-4	Digikey	A28768-ND	R/A HEADER
34	1	J14	RA_SINGLEHEADER_6PIN	Male Header	Tyco Electronics	87232-6	Digikey	A28772-ND	R/A HEADER
35	17	R31 R33 R35 R37 R47-50 R59 R61-62 R64-69	0 1/10W	RES-0603	Vishay/Dale	CRCW06030000Z0EA	Mouser	71-CRCW0603-0-E3	SURFACE MOUNT RESISTOR 0603 Size
36	30	R15-18 R21-30 R32 R34 R36 R38-46 R55-58	100K 1/16W	RES-0603	Sasumu Co Ltd.	RR0816P-104-D	Digikey	RR08P100KDCT-ND	SURFACE MOUNT RESISTOR 0603 Size
37	11	R9 R12 R14 R19-20 R51-54 R60 R63	10K 1/16W	RES-0603	Panasonic ECG	ERA-3AEB103V	Digikey	P10KDBCT-ND	SURFACE MOUNT RESISTOR 0603 Size
38	1	R10	150K 1/16W	RES-0603	Sasumu Co Ltd.	RR0816P-154-D	Digikey	RR08P150KDCT-ND	SURFACE MOUNT RESISTOR 0603 Size
39	1	R13	1K 1/16W	RES-0603	KOA Speer	RN731JTTD1001B25	Mouser	660-RN731JTTD1001B25	SURFACE MOUNT RESISTOR 0603 Size
40	9	R1-8 R11	51 1/16W	RES-0603	Sasumu Co Ltd.	RR0816Q-510-D	Digikey	RR08Q51DCT-ND	SURFACE MOUNT RESISTOR 0603 Size
41	1	R74	698 1/10W	RES-0603	Rohm	MCR03EZPFX6980	Digikey	RHM698HCT-ND	SURFACE MOUNT RESISTOR 0603 Size
42	2	R75-76	10K 1/4W	RES-1206	Rohm	MCR18EZPJ103	Digikey	RHM10KERCT-ND	SURFACE MOUNT RESISTOR 0603 Size
43	1	U1	RFIC-4	QFN-100	MOTOROLA				SDR RFIC
44	1	E1	SM_BEADS_DIFF	SMD	FAIR-RITE PRODUCTS CORP	2743019447	Mouser	623-2743019447LF	SM BEADS DIFFERENTIAL
45	1	U3	TC7S04F	SSOP-5	TOSHIBA	TC7S04F(T5L,F,T)	Digikey	TC7S04FTFCT-ND	INVERTER
46	13	U4-16	TPS76901DBVR	SOT-23-5	TEXAS INSTRUMENTS	TPS76901DBVR	Digikey	296-11029-1-ND	LINEAR REGULATOR
47	1	U18	REGULATOR	SO-8	LINEAR TECHNOLOGY	LT1763CS8-5	Digikey	LT1763CS8-5-ND	LINEAR REGULATOR

Appendix G

ADC/DAC Board

This appendix documents the design of the ADC/DAC board for the VT MMR discussed in Section 7.5.3 ("ADC/DAC Board"). This board also contains a frequency synthesizer to supply 1 GHz reference to the RFIC board.

G.1 Board Overview

Figure G.1 and Table G.1 present all the input/output ports of the ADC/DAC board.

Figure G.2 shows the schematic of the ADC section in the ADC/DAC board. The AD9248 dual 14-bit A/D converter from Analog Devices has been selected to convert the analog signal to digital signal in our design to operate the receiver section. The differential in-phase (I) and quadrature-phase (Q) inputs are applied to the input ports of the ADCs. Although this ADC has two output ports (data port A and data port B), the output data from the dual ADCs can be multiplexed onto a single output port. In our case only data port B is enabled to supply the multiplexed digitized signals from the two ADCs. The FPGA board shown in Figure 7.11 supplies the reference clock for both of the A/D converters through the ADI connector in this IC. There is also an option to supply reference clock from external source other than the FPGA board. The data port B is connected to a 40-pin connector (J1) through two octal bus buffer ICs (74VHC541) and 22 ohm resistor pads. The unused data port A is terminated with 22 ohm resistors and connected to a 40-pin header

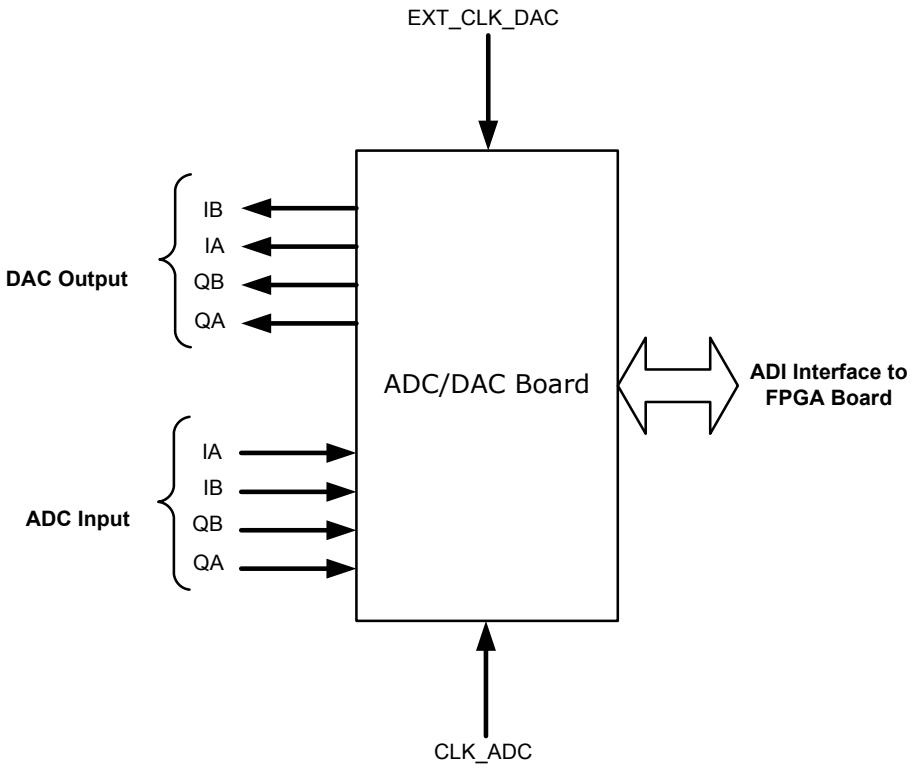


Figure G.1: Summary of the ADC/DAC board I/O.

Table G.1: Description of input/output ports of the ADC/DAC board.

Function	**Port Name**	**Conn. Name**	**Characteristics**
DAC Output	IB	J8-A	Differential Output
	IA	J8-B	of I-Channel
	QB	J8-C	Differential Output
	QA	J8-D	of Q-Channel
ADC Input	IA	J24-A	Differential Input
	IB	J24-B	of I-Channel
	QB	J24-C	Differential Input
	QA	J24-D	of Q-Channel
CLK ADC Input	CLK_ADC	J5	ADC Reference Clock (4 MHz)
CLK DAC Input	EXT_CLK	J9	External DAC Clock (4 MHz)
Synthesizer Output	RF_OUT	J27	RF analog output from the synthesizer (50Ω, +10 dBm)
ADI Interface	ADI	J1, J12	ADI interface to FPGA

connector (J11).

Figure G.3 shows the circuit diagram of the DAC section in the ADC/DAC board. The AD9761 dual 10-bit D/A converter from Analog Devices has been selected to convert the digital signal to analog signal in our design for the transmission operation. Similar to the ADC section, the DAC provides the differential in-phase (I) and quadrature-phase (Q) analog output signals from the digital I and Q input signal. Similar to the ADC section, the reference clock is supplied from an FPGA board through the ADI connectors. This also has an option to receive reference clock from external source other than the FPGA board. The input of the data port is connected to a 40-pin connector (J12) through 22 ohm resistor pads.

Figure G.4 shows the schematic of the power supply section in the ADC/DAC board.Three separate 3V supply voltages and one 2.5V supply voltage for ADC, and two separate 5V supply voltages for DAC have been created from a single 10V power source. First, the main 10V input voltage is fed into a 3A low–dropout regulator IC (LT1529) to create a 5V positive voltage. This 5V voltage is supplied to the input of the four low–dropout regulator ICs (ADP3339), which provides the required output voltage of 3V and 2.5V. Two positive voltage regulator ICs MC78M05 generate the 5V supply voltages for the DAC directly from the 10V power supply.

Figure G.5 shows the schematic of the synthesizer section. We use a frequency synthesizer, Model LFSW35105-100, from Synergy Microwave Corporation[1]. This synthesizer is capable of providing frequency output 350 to 1050 MHz using just a single 10 MHz (1 V_{pp} to 3 V_{pp}) reference frequency. The FPGA board shown in Figure 7.11 contains a DAC, which is used to supply this 10 MHz reference signal to the synthesizer.

Table G.2 shows the jumper settings of the PCB.

A summary of the cost for one ADC/DAC board is given in Table G.3. Since we prepared just two boards for the present study using the quickest manufacturing time, the PCB fabrication and assembly cost is not representative of the cost to build the same device in large quantities.

[1] http://www.synergymwave.com

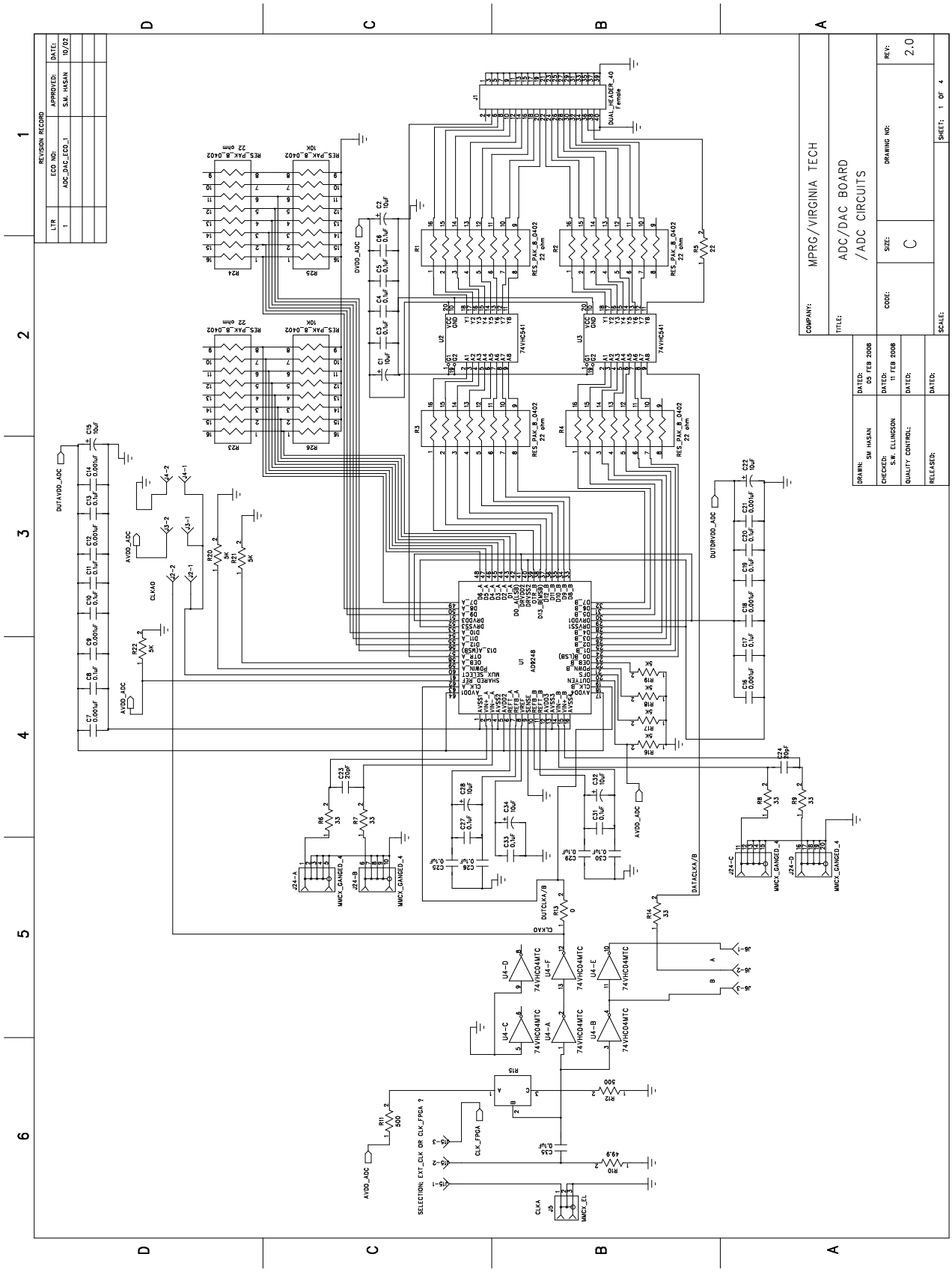


Figure G.2: Schematic of the ADC section of ADC/DAC board.

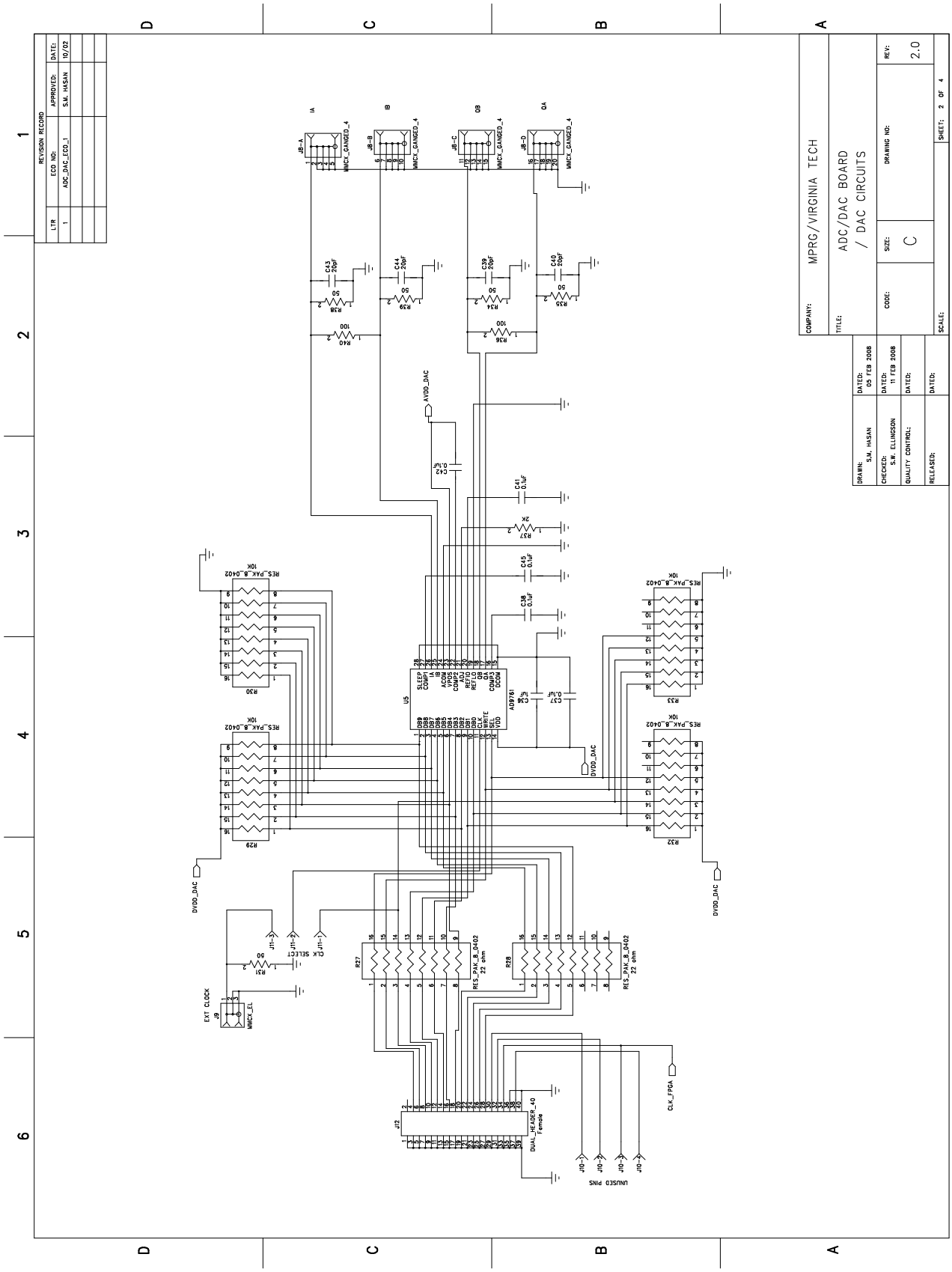


Figure G.3: Schematic of the DAC section of ADC/DAC board.

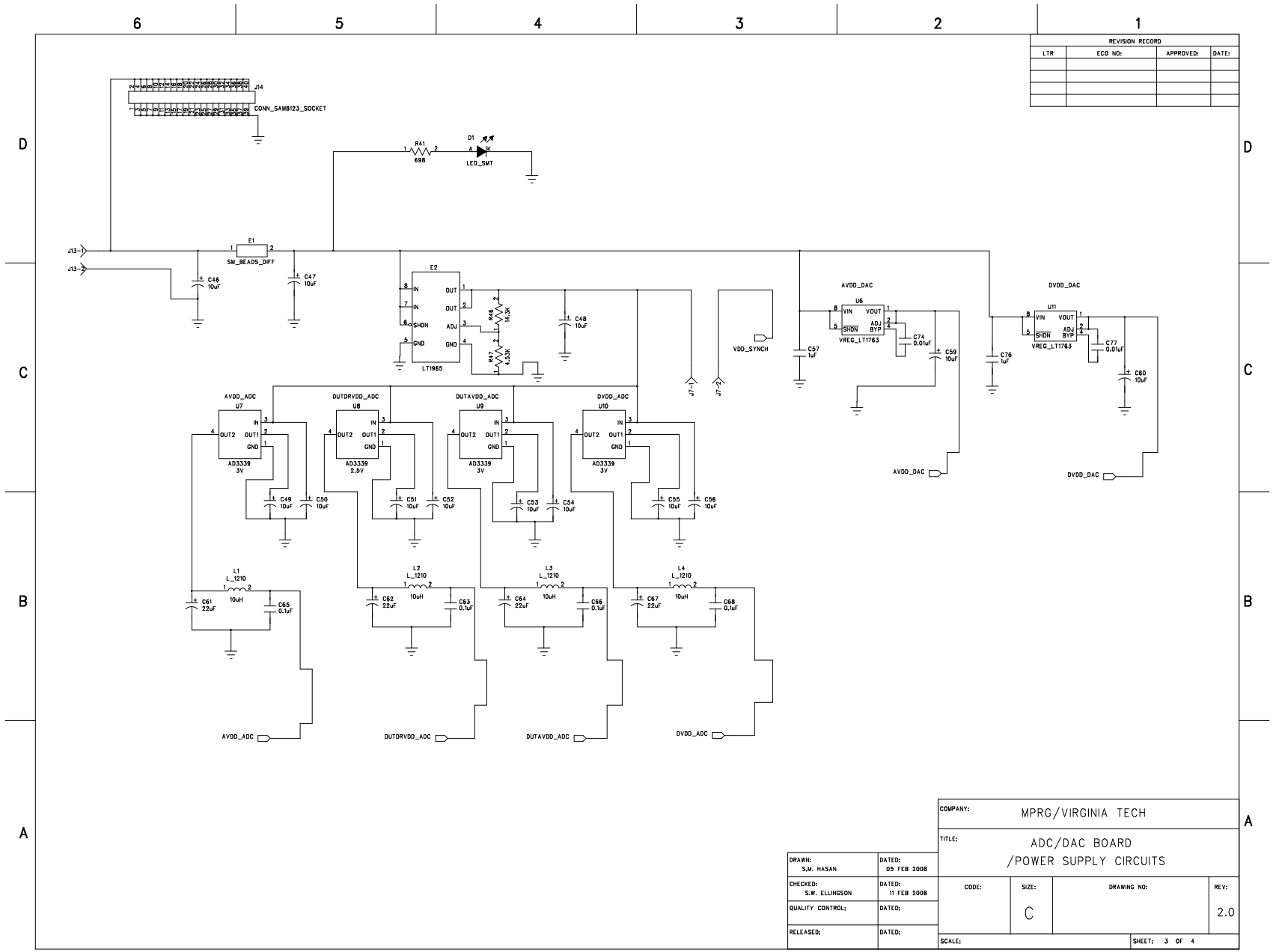


Figure G.4: Schematic of the power supply section of ADC/DAC board.

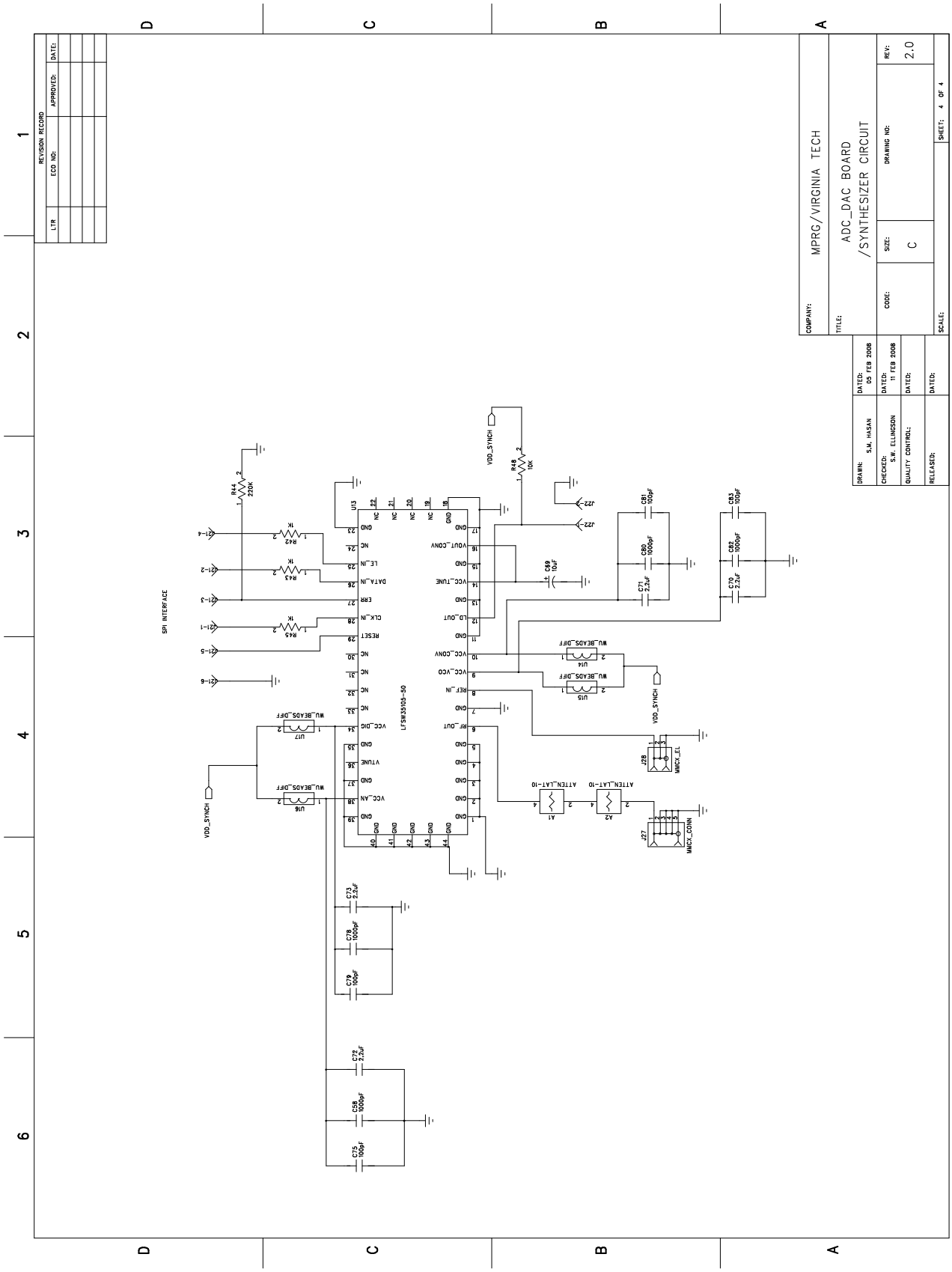


Figure G.5: Schematic of the synthesizer section of ADC/DAC board.

Table G.2: Jumper settings of the ADC/DAC board.

Jumper	**Description**	**Normal Setting**	**Comment**
J21	Power	In	3V supply to ADC
J22	Power	In	2.5V supply to ADC
J23	Power	In	3V supply to ADC
J24	Power	In	3V supply to ADC
J25	Power	In	5V supply to DAC
J26	Power	In	5V supply to DAC
J8	Mux Select	Out	Connect MUX_SEL pin to Clock
J9	Mux Select	Out	Connect MUX_SEL pin to VDD
J10	Mux Select	In	Connect MUX_SEL pin to GND
J7	Clock Polarity	A	Position B select the opposite polarity
J14	DAC Clock Select	A	'A' selects the clock from the FPGA board and 'B' selects the clock from an external source

G.2 Layout, and Bill of Materials

The PCB layout of the implemented ADC/DAC board is shown in Figures G.6 to G.8. The bill of materials for this board is shown at the end of this appendix.

Table G.3: Summary of the cost for one ADC/DAC board.

Component	**Quantity**	**Price(US $)**
ADC & DAC ICs	2	43.20
Other ICs	10	26.00
Capacitors	68	5.00
Inductors	4	1.00
Resistors	41	4.00
Synthesizer	1	150.00
MMCX Connectors	6	36.00
Other Connectors	16	23.50
Other Components	17	3.50
	Subtotal	**292.20**
PC Board	1	450.00
PC Board Assembly	1	925.00
	Total	**1667.20**

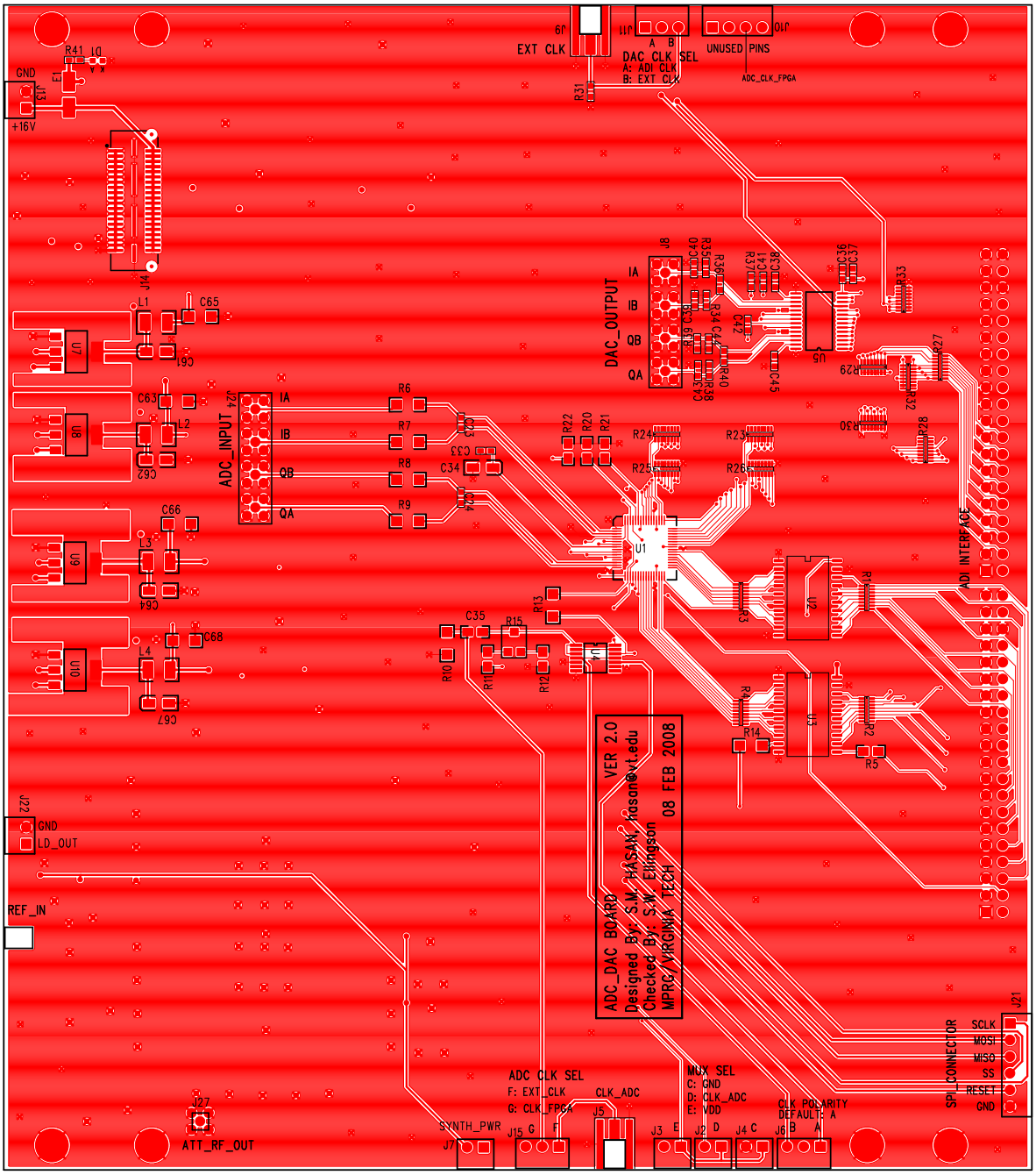


Figure G.6: Top layer of the ADC/DAC board.

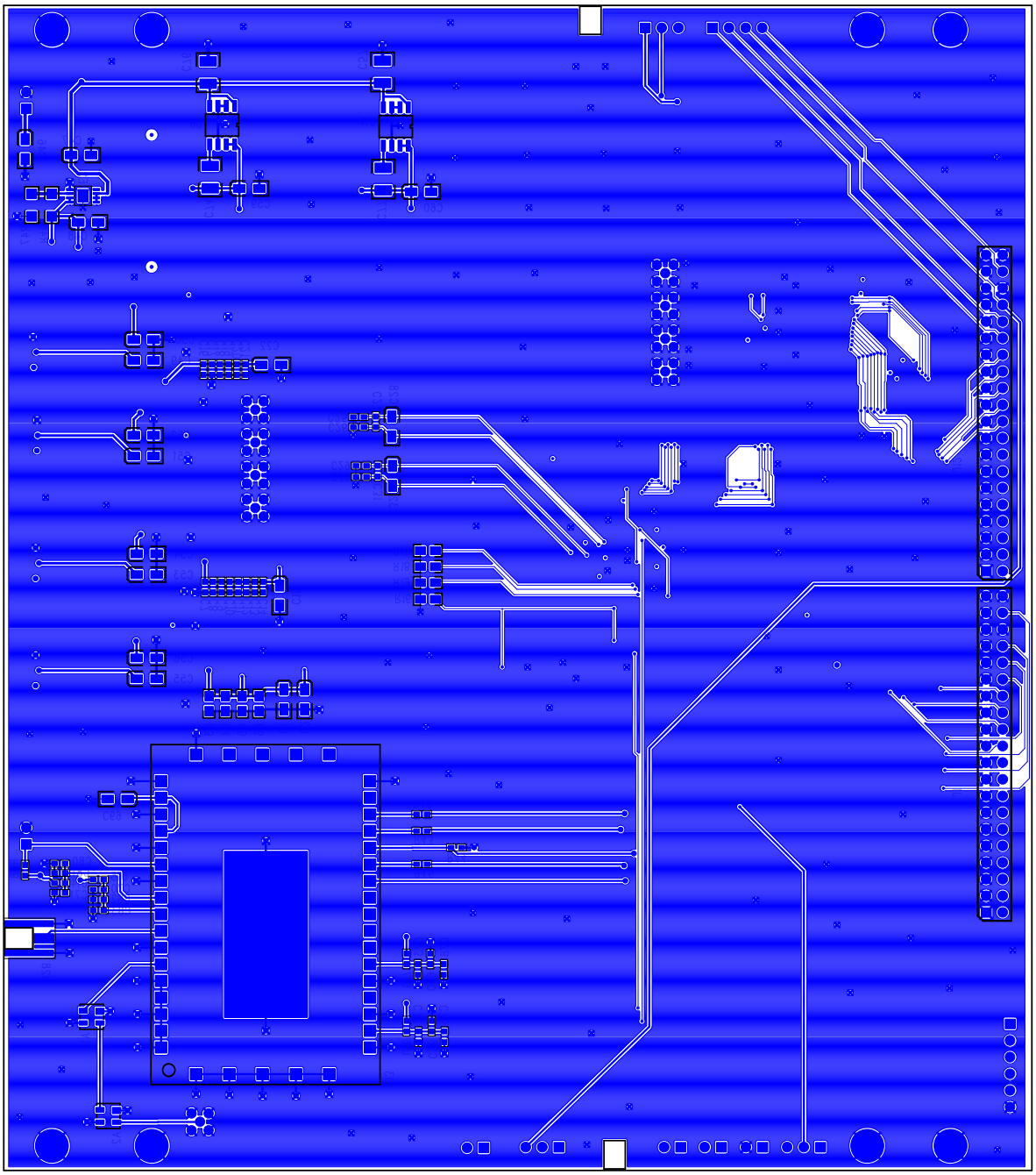


Figure G.7: Bottom layer of the ADC/DAC board.

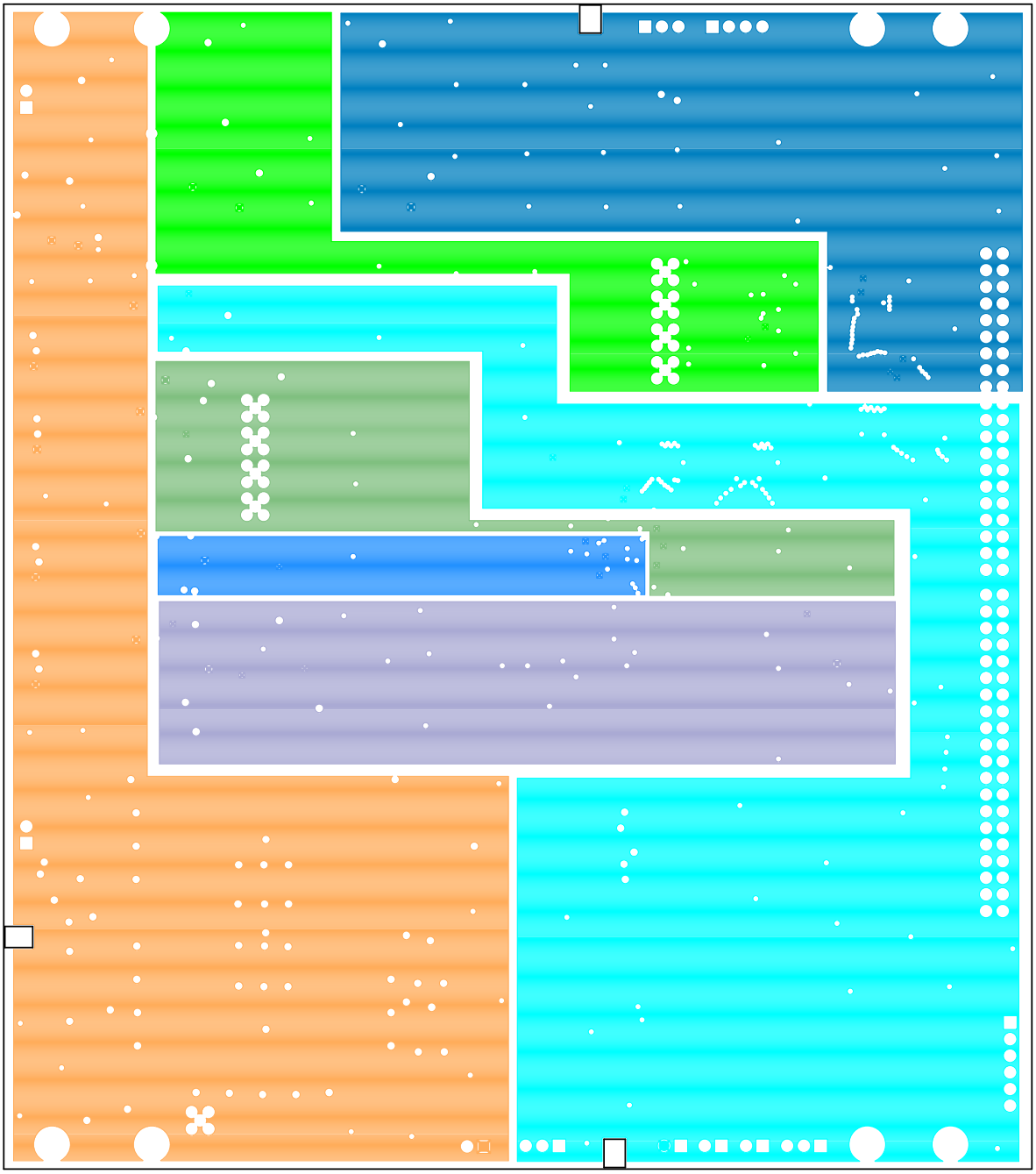


Figure G.8: Power layer of the ADC/DAC board.

Bill of Materials
NIJ ADC_DAC Board, Ver. 2.0
MPRG/Virginia Tech
Prepared By: S.M. Hasan, Date: FEB 20, 2008

Item	Qty	Reference	Part Name	Package	Manufacturer	Manufacturer Part#	Distributor	Distributor Part#	Description
1	2	U2-3	74VHC541	20-SOL	TOSHIBA	TC74VHC541FW	Digikey	TC74VHC541FW-ND	OCTAL BUS BUFFER
2	1	U4	74VHC04MTC	14-TSSOP	FAIRCHILD SEMICONDUCTOR	74VHC04MTC	Digikey	74VHC04MTC-ND	HEX INVERTER
3	1	U8	AD3339,2.5V	SOT-223	Analog Devices	ADP3339AKCZ-2.5-R7	Digikey	ADP3339AKCZ-2.5-R7CT-ND	Low Dropout Regulator
4	3	U7 U9-10	AD3339,3V	SOT-223	Analog Devices	ADP3339AKCZ-3-RL7	Digikey	ADP3339AKCZ-3-RL7CT-ND	Low Dropout Regulator
5	1	U1	AD9248	64-LQFP	Analog Devices	AD9248BSTZ-20	Digikey	AD9248BSTZ-20-ND	14-Bit Dual A/D Converter
6	1	U5	AD9761	28-SSOP	ANALOG DEVICES	AD9761ARSZ	Digikey	AD9761ARSZ-ND	DUAL 10-BIT DAC
7	2	A1-2	Attenuator	MMM168	Minicircuits	LAT-10+	Minicircuits	LAT-10+	SMD Fixed Attenuator
8	2	C74 C77	0.01uF 100V	CAP_1210	AVX Corporation	12101C103KAT2A	Digikey	478-1608-1-ND	SURFACE MOUNT CAPACITOR 0.098 X 0.126 INCHES
9	2	C57 C76	1uF 100V	CAP_1210	AVX Corporation	12101C105KAT2A	Digikey	478-2570-1-ND	SURFACE MOUNT CAPACITOR 0.098 X 0.126 INCHES
10	7	C7 C9 C12 C14 C16 C18 C21	0.001uF	CAP_0603	Panasonic-ECG	ECJ-1VB1H102K	Digikey	PCC1772CT-ND	SURFACE MOUNT CAPACITOR 0603 Size
11	19	C8 C10-11 C13 C17 C19-20 C25-27 C29-31 C33 C37-38 C41-42 C45	0.1uF	CAP_0603	Murata Electronics	GRM188R71H104KA93D	Digikey	490-1519-1-ND	SURFACE MOUNT CAPACITOR 0603 Size
12	4	C58 C78 C80 C82	1000pF 50V	CAP_0603	AVX Corporation	06035C102KAT2A	Digikey	478-1215-1-ND	SURFACE MOUNT CAPACITOR 0603 Size
13	4	C75 C79 C81 C83	100pF 50V	CAP_0603	AVX Corporation	06035A101KAT2A	Digikey	478-3717-1-ND	SURFACE MOUNT CAPACITOR 0603 Size
14	1	C36	1uF	CAP_0603	Panasonic-ECG	ECJ-1VB1C105K	Digikey	PCC2224CT-ND	SURFACE MOUNT CAPACITOR 0603 Size
15	4	C70-73	2.2uF 10V	CAP_0603	Panasonic-ECG	ECJ-1VB1A225K	Digikey	PCC2397CT-ND	SURFACE MOUNT CAPACITOR 0603 Size
16	6	C23-24 C39-40 C43-44	20pF	CAP_0603	Murata Electronics	GRM1885C2A200JA01D	Digikey	490-1334-1-ND	SURFACE MOUNT CAPACITOR 0603 Size
17	5	C3-6 C35	0.1uF	CAP_0805	Kemet	C0805C104K5RACTU	Digikey	399-1170-1-ND	SURFACE MOUNT CAPACITOR 0805 Size
18	4	C63 C65-66 C68	0.1uF	CAP_1206	Kemet	C1206C104K5RACTU	Digikey	399-1249-1-ND	SURFACE MOUNT CAPACITOR 1206 Size

Item	Qty	Reference	Part Name	Package	Manufacturer	Manufacturer Part#	Distributor	Distributor Part#	Description
19	21	C1-2 C15 C22 C28 C32 C34 C46-56 C59-60 C69	10uF 16V	CAP_3216	Rohm	TCA1C106M8R	Digikey	511-1473-1-ND	CAP TANTALUM
20	4	C61-62 C64 C67	22uF 10V	CAP_3216	Rohm	TCA1A226M8R	Digikey	511-1465-1-ND	CAP TANTALUM
21	1	J14	CONN_SAM8123_SOCKET	Socket	Samtec Inc	QSE-020-01-L-D-A	Digikey	SAM8123-ND	High Speed Socket 40 pins
22	2	J1 J12	DUAL_HEADER_40	Female Header	Sullins Electronics	PPPC202LFBN-RC	Digikey	S7123-ND	Header Female
23	1	R15	Pot 10K	SMT	PANASONIC	EVN-5ESX50B14	Digikey	P5E103CT-ND	TRIMMER POTENTIOMETER
24	1	D1	LED, Green	SMT	LITE-ON	LTST-C190GKT	Digikey	160-1183-1-ND	LIGHT EMITTING DIODE
25	1	U13	SYNTHESIZER	280LF	SYNERGY	LFSW35105-50	SYNERGY	LFSW35105-50	FREQUENCY SYNTHESIZER
26	1	E2	REGULATOR	MSOP8G	Linear Technology	LT1965	Digikey	LT1965IMS8E#PBF-ND	Linear Regulator
27	4	L1-4	10uH	L-1210	Panasonic-ECG	ELJ-FA100JF	Digikey	PCD1817CT-ND	Surface Mount Inductor 1210 Size
28	1	J27	MMCX_JACK	MMCX	Amphenol Connex	262104	Digikey	ACX1275-ND	MMCX CONNECTOR
29	3	J5 J9 J28	MMCX_EL_JACK	MMCX	Johnson Components	135-3711-801	Digikey	J603-ND	END LAUNCH MMCX JACK
30	2	J8 J24	MMCX_GANG_JACK	MMCX	Samtec Inc	GRF1-J-P-04-E-ST-TH1	Digikey	SAM8069-ND	MMCX GANGED JACK
31	6	J2-4 J7 J13 J22	RA_SINGLEHEADER_2PIN	Male Header	TYCO	87232-2	Digikey	A28764-ND	R/A HEADER
32	3	J6 J11 J15	RA_SINGLEHEADER_3PIN	Male Header	TYCO	87232-3	Digikey	A28766-ND	R/A HEADER
33	1	J10	RA_SINGLEHEADER_4PIN	Male Header	TYCO	87232-4	Digikey	A28768-ND	R/A HEADER
34	1	J21	RA_SINGLEHEADER_6PIN	Male Header	TYCO	87232-6	Digikey	A28772-ND	R/A HEADER
35	2	R36 R40	100 1/10W	RES-0603	Panasonic-ECG	ERJ-3GEYJ101V	Digikey	P100GCT-ND	SURFACE MOUNT RESISTOR 0603 Size
36	1	R48	10K 1/10W	RES-0603	Rohm	MCR03EZPJ103	Digikey	RHM10KGCT-ND	SURFACE MOUNT RESISTOR 0603 Size
37	3	R42-43 R45	1K 1/10W	RES-0603	Yageo Corporation	RC0603JR-071KL	Digikey	311-1.0KGRCT-ND	SURFACE MOUNT RESISTOR 0603 Size
38	1	R44	220K 1/10W	RES-0603	Rohm	MCR03EZPJ224	Digikey	RHM220KGCT-ND	SURFACE MOUNT RESISTOR 0603 Size
39	1	R37	2K 1/10W	RES-0603	Panasonic-ECG	ERJ-3GEYJ202V	Digikey	P2.0KGCT-ND	SURFACE MOUNT RESISTOR 0603 Size

Item	Qty	Reference	Part Name	Package	Manufacturer	Manufacturer Part#	Distributor	Distributor Part#	Description
40	1	R41	698 1/10W	RES-0603	Rohm	MCR03EZPFX6980	Digikey	RHM698HCT-ND	SURFACE MOUNT RESISTOR 0603 Size
41	5	R31 R34-35 R38-39	49.9 1/10W	RES-0603	Panasonic-ECG	ERJ-3EKF49R9V	Digikey	P49.9HCT-ND	SURFACE MOUNT RESISTOR 0603 Size
42	1	R5	22 1/8W	RES-0805	Panasonic-ECG	ERJ-6GEYJ220V	Digikey	P22ACT-ND	SURFACE MOUNT RESISTOR 0805 Size
43	2	R11-12	499 1/8W	RES-0805	Panasonic-ECG	ERJ-6ENF4990V	Digikey	P499CCT-ND	SURFACE MOUNT RESISTOR 0805 Size
44	7	R16-22	4.99K 1/8W	RES-0805	Rohm	MCR10EZHF4991	Digikey	RHM4.99KCCT	SURFACE MOUNT RESISTOR 0805 Size
45	1	R13	0 1/4W	RES-1206	Panasonic-ECG	ERJ-8GEY0R00V	Digikey	P0.0ECT-ND	SURFACE MOUNT RESISTOR 1206 Size
46	1	R46	14.3K 1/4W	RES-1206	Rohm	MCR18EZHF1432	Digikey	RHM14.3KFCT-ND	SURFACE MOUNT RESISTOR 1206 Size
47	5	R6-9 R14	33 1/4W	RES-1206	Panasonic-ECG	ERJ-8GEYJ330V	Digikey	P33ECT-ND	SURFACE MOUNT RESISTOR 1206 Size
48	1	R47	4.53K 1/4W	RES-1206	Rohm	MCR18EZHF4531	Digikey	RHM4.53KFCT-ND	SURFACE MOUNT RESISTOR 1206 Size
49	1	R10	49.9 1/4W	RES-1206	Panasonic-ECG	ERJ-8ENF49R9V	Digikey	P49.9FCT-ND	SURFACE MOUNT RESISTOR 1206 Size
50	6	R25-26 R29-30 R32-33	RES_PAK_8_0402,10K	RES-0402	CTS	741X163103JP	Digikey	741X163103JPCT-ND	RESISTOR PAK 8- 0402
51	8	R1-4 R23-24 R27-28	RES_PAK_8_0402,22 ohm	RES-0402	CTS	741X163220JP	Digikey	741X163220JPCT-ND	RESISTOR PAK 8- 0402
52	1	E1	SM_BEADS_DIFF	SMT	FAIR-RITE PRODUCTS CORP	2743019447	Mouser	623-2743019447LF	SM BEADS DIFFERENTIAL
53	2	U6 U11	REGULATOR	SO-8	Linear Technology	LT1763CS8-5	Digikey	LT1763CS8-5-ND	Linear Regulator
54	4	U14-17	WU_BEAD_DIF	BEAD_0603	WUERTH ELECTRONICS	74279266A	Digikey	732-1598-1-ND	SMD FERRITE CORE

Appendix H

Audio Board & User Interface

This appendix documents the design of the audio board and the user interface implemented for the VT MMR prototype.

Figure H.1 shows the audio board. This board has an interface to connect a hand–held push–to–talk (PTT) type of microphone and speaker and contains a volume control for speaker and microphone. It also has internal circuitry to the detect the PTT signal, so that whenever the PTT button is pressed, the radio configures itself for transmit mode. Figure H.2 shows the schematic of the audio board. The PCB layout of the implemented audio board is shown in Figure H.3. The bill of materials for this board is shown at the end of this section.

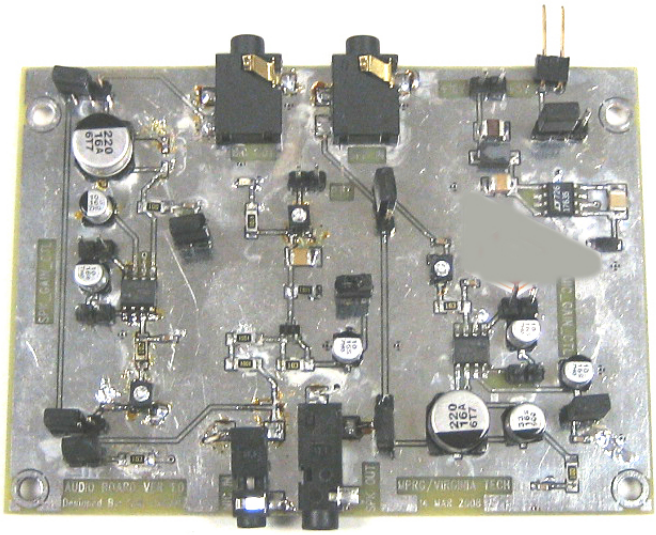


Figure H.1: Audio board.

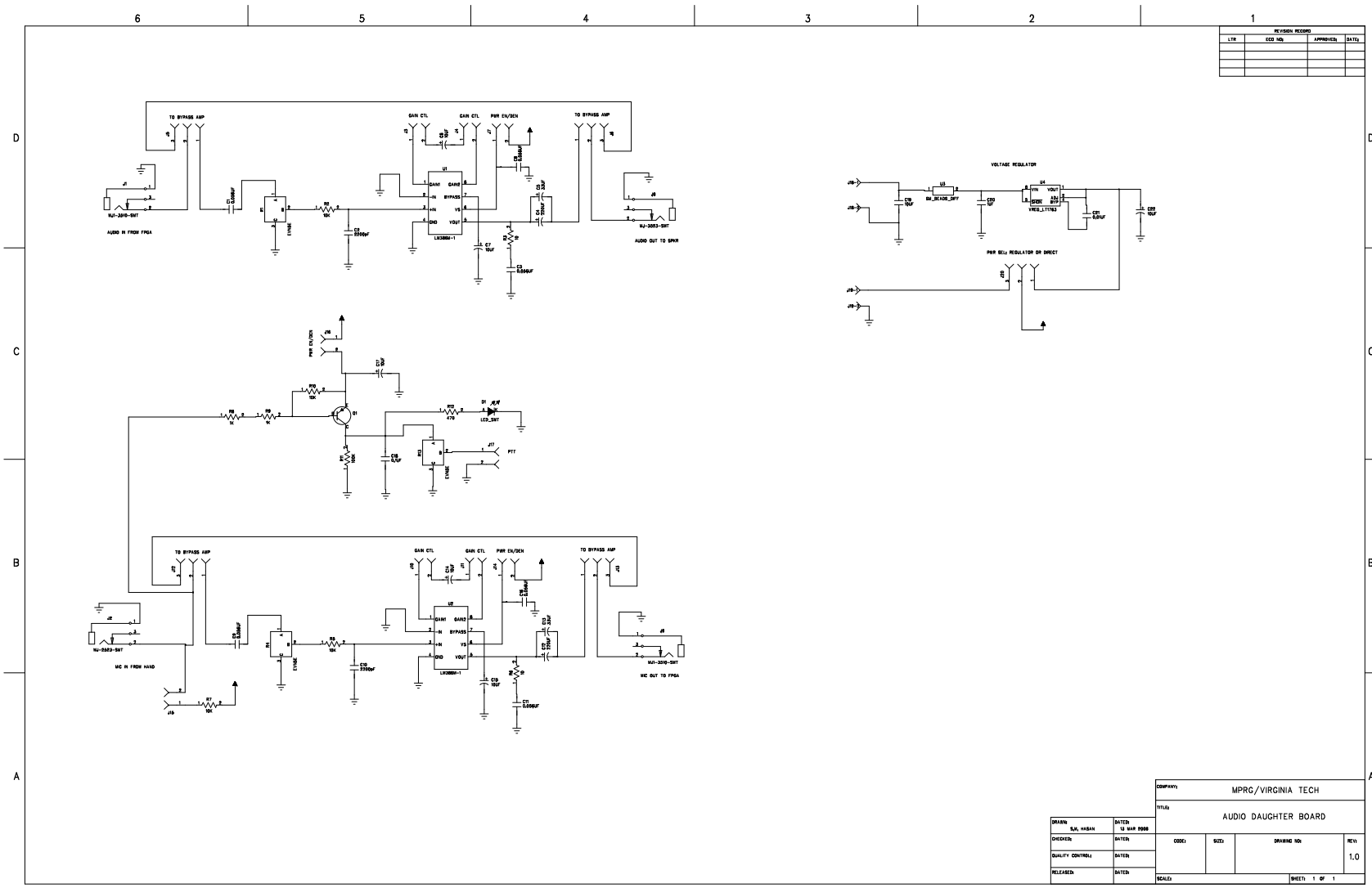


Figure H.2: Schematic of the audio board.

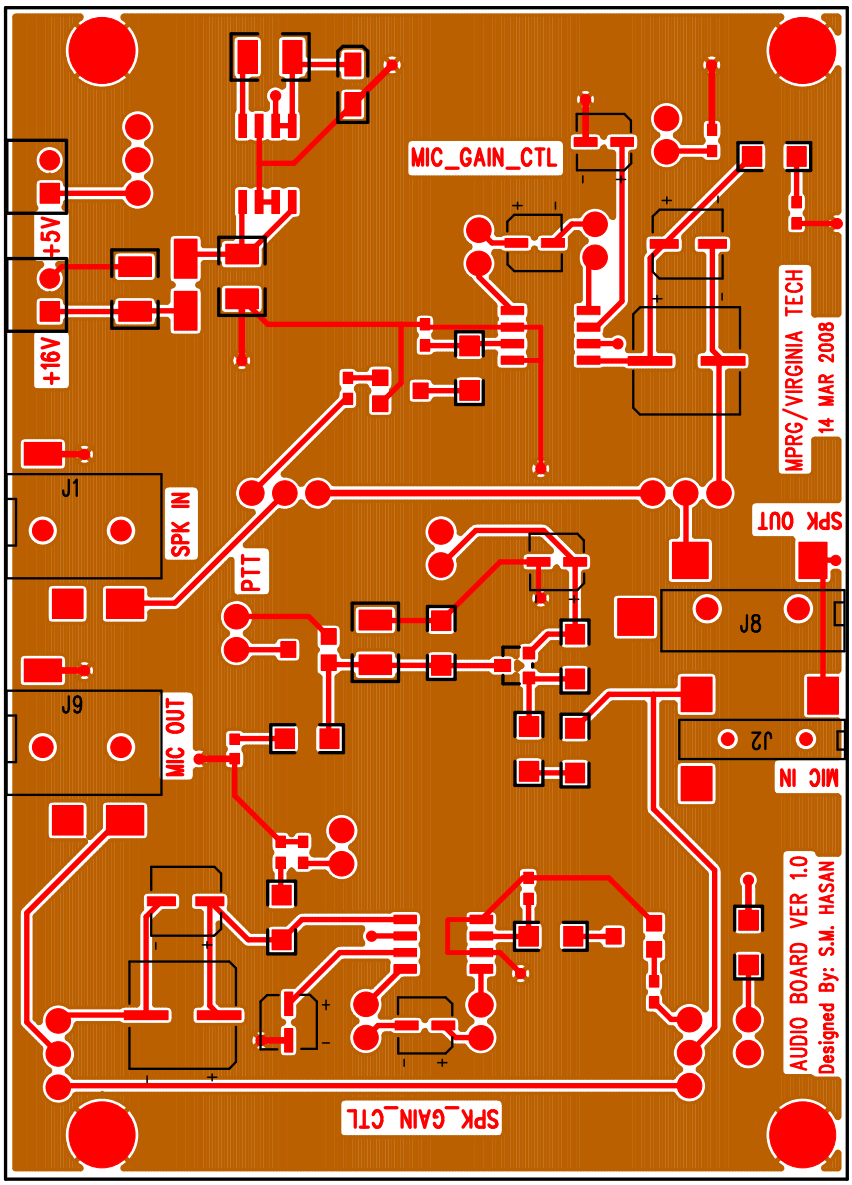


Figure H.3: Top layer of the audio board.

Bill of Materials
Audio Board, Version 1.0
MPRG/Virginia Tech
Prepared By: SM Hasan, Date: MAR 15, 2008

Item	Qty	Reference	Part Name	Package	Manufacturer	Manufacturer Part#	Distributor	Distributor Part#	Description
1	1	C21	0.01UF 100V	CAP-1210	AVX Corporation	12101C103KAT2A	Digikey	478-1608-1-ND	SURFACE MOUNT CAPACITOR 0.098 X 0.126 INCHES
2	1	C18	0.1UF 100V	CAP-1210	AVX Corporation	12101C104JAT2A	Digikey	478-3813-1-ND	SURFACE MOUNT CAPACITOR 0.098 X 0.126 INCHES
3	1	C19	10UF 16V	CAP-1210	AVX Corporation	1210YD106KAT2A	Digikey	478-1629-1-ND	SURFACE MOUNT CAPACITOR 0.098 X 0.126 INCHES
4	1	C20	1UF 100V	CAP-1210	AVX Corporation	12101C105KAT2A	Digikey	478-2570-1-ND	SURFACE MOUNT CAPACITOR 0.098 X 0.126 INCHES
5	6	C1 C3 C8-9 C11 C16	0.056UF 25V	CAP-0603	Panasonic ECG	ECJ-1VB1E563K	Digikey	PCC2278CT-ND	SURFACE MOUNT CAPACITOR 0603 Size
6	2	C2 C10	2200pF 50V	CAP-0603	Murata Electronics	GRM188R71H222KA01D	Digikey	490-1500-1-ND	SURFACE MOUNT CAPACITOR 0603 Size
7	1	C22	10UF 16V	CAP-3216, TANT	Rohm	TCA1C106M8R	Digikey	511-1473-1-ND	CAP TANTALUM
8	5	C6-7 C14-15 C17	10UF 16V	CAP_ELEC_B	Panasonic ECG	ECE-V1CA100SR	Digikey	PCE3062CT-ND	CAPACITOR AL ELEC B
9	2	C5 C13	33UF 16V	CAP_ELEC_C	Panasonic ECG	ECE-V1CA330WR	Digikey	PCE3180CT-ND	CAPACITOR AL ELEC C
10	2	C4 C12	220UF 16V	CAP_ELEC_E	Panasonic ECG	ECE-V1CA221UP	Digikey	PCE3275CT-ND	CAPACITOR AL ELEC E
11	9	J3-4 J7 J10-11 J14-17	CONN_DUAL_HDR_2PIN	HEADER_2PIN	Tyco Electronics	1-87215-0	Digikey	A26564-ND	2-Pin Dual Header
12	5	J5-6 J12-13 J20	CONN_HEADER_3PIN	HEADER_3PIN	Tyco Electronics	87220-3	Digikey	A26544-ND	3-pin Single Row 0.100 Header
13	3	R1 R4 R13	10K Pot	EVN5E	Panasonic ECG	EVN-5ESX50B14	Digikey	P5E103CT-ND	TRIMMER POTENTIOMETER

14	1	D1	LED Green Clear	LED_PAD	LITE-ON	LTST-C190GKT	Digikey	160-1183-1-ND	LIGHT EMITTING DIODE
15	2	U1-2	LM386M-1	SO-8	NATIONAL SEMICONDUCTOR	LM386M-1/NOPB	Digikey	LM386M-1-ND	AUDIO POWER AMPLIFIER
16	1	J2	MJ-2523-SMT	MJ-2523-SMT	CUI Inc	MJ-2523-SMT	Digikey	CP-2523MJCT-ND	2.5mm SURFACE MOUNT AUDIO JACK MONO
17	1	J8	MJ-3523-SMT	MJ-3523-SMT	CUI Inc	MJ-3523-SMT	Digikey	CP-3523MJCT-ND	2.5mm SURFACE MOUNT AUDIO JACK MONO
18	2	J1 J9	MJ1-3510-SMT	MJ1-3510-SMT	CUI Inc	MJ1-3510-SMT	Digikey	CP1-3510MJCT-ND	
19	1	Q1	MMBT3906LT1	SOT23	ON Semiconductor	MMBT3906LT1G	Digikey	MMBT3906LT1GOSCT-ND	GENERAL PURPOSE PNP SILICON TRANSISTOR
20	2	J18-19	RA_SINGLEHEADER_2PIN	SINGLEHEADER_2	TYCO	87232-2	Digikey	A28764-ND	2-Pin R/A Single Row Header
21	2	R3 R6	10 1/4W	RES-1206	Rohm	MCR18EZPJ100	Digikey	A28764-ND	SURFACE MOUNT RESISTOR 1206 Size
22	1	R11	100K 1/4W	RES-1206	Rohm	MCR18EZPF1003	Digikey	RHM100KFRCT-ND	SURFACE MOUNT RESISTOR 1206 Size
23	4	R2 R5 R7 R10	10K 1/4W	RES-1206	Rohm	MCR18EZPJ103	Digikey	RHM10KERCT-ND	SURFACE MOUNT RESISTOR 1206 Size
24	2	R8-9	1K 1/4W	RES-1206	Rohm	MCR18EZPF1001	Digikey	RHM1.00KFRCT-ND	SURFACE MOUNT RESISTOR 1206 Size
25	1	R12	470 1/4W	RES-1206	Rohm	MCR18EZPF4700	Digikey	RHM470FRCT-ND	SURFACE MOUNT RESISTOR 1206 Size
26	1	U3	SM_BEADS_DIFF	SM_BEADS	FAIR-RITE PRODUCTS CORP	2743019447	Mouser	623-2743019447LF	SM BEADS DIFFERENTIAL
27	1	U4	VREG_LT1763	SO-8	Linear Technology	LT1763CS8-5	Digikey	LT1763CS8-5-ND	Linear Regulator

A detailed description of the user interface designed for the VT MMR prototype appears in [100]. Figure H.4 shows the image of the embedded controller (Gumstix "LCD pack" [1]) including the touchscreen LCD interface which is used as the user interface for controlling the VT MMR. See Figure 7.1 for this is it appears installed in the radio.

The Gumstix controller communicates with the RFIC through the serial peripheral interface (SPI) and it also sends the multiplexer channel select information to the FPGA. In SPI communication the Gumstix controller act as the master and the RFIC act as the slave. General-purpose input/output (GPIO) pins in the Gumstix controller are used to perform this SPI operation. Generally, data can be transferred in both directions simultaneously when the slave select signal is low active. However, SPI communication in this design is only one way at current stage. That is why the signal MISO in Figure H.5 is connected with the dotted line. The signal RESET shown in Figure H.5 is required to reset the RFIC before starting to program it.

The Gumstix controller selects a channel and sends the corresponding channel information to the FPGA board. The FPGA board processes the channel information and then sends them to the RFFE board. Table H.1 is the truth table for the channel selection. Table H.2 shows the GPIO pin mapping.

[1] http://www.gumstix.com

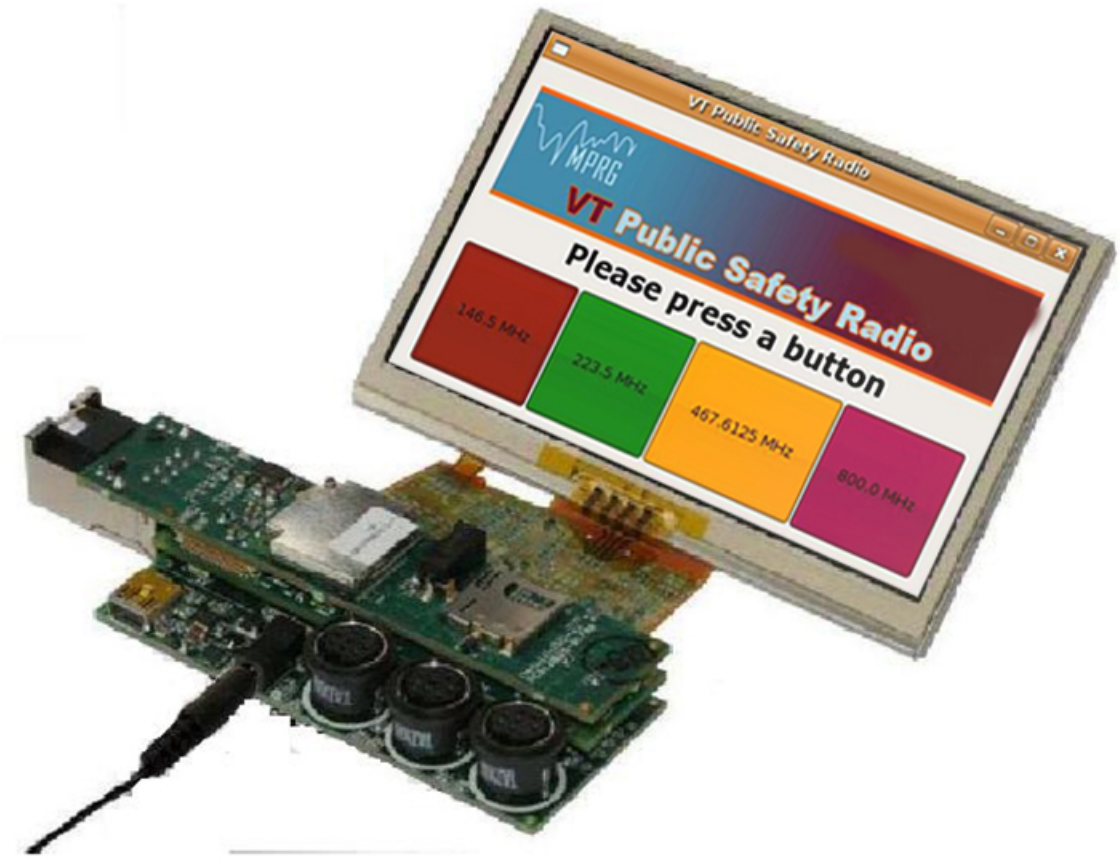


Figure H.4: The Gumstix embedded controller including the touchscreen LCD interface.

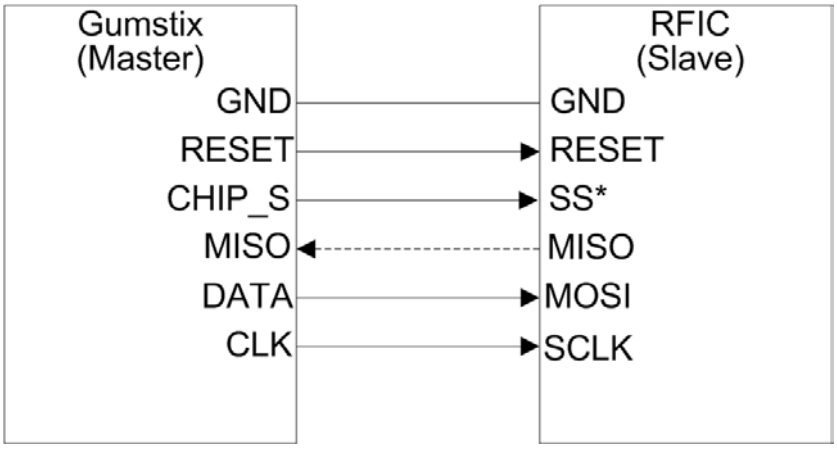


Figure H.5: SPI communication between the Gumstix controller and the RFIC.

Table H.1: Channel selection truth table.

Control Signals		**Channel Number**
CH_A	CH_B	
Low	Low	1
Low	High	2
High	Low	3
High	High	4

Table H.2: GPIO pin definition.

Pin Name	**Pin Number**			**Signal Name**
	consoleLCD16–vx Board	RFIC/FPGA Board		
	NSSP–1	RFIC Board	J14–6	GND
GPIO< 13 >	NSSP–2		J14–2	DATA
GPIO< 11 >	NSSP–3		J14–5	RESET
GPIO< 14 >	NSSP–4		J14–4	CHIP_S
GPIO< 19 >	NSSP–6		J14–1	CLK
GPIO< 44 >	BTUART–5	FPGA Board	J27–9	CH_A
GPIO< 45 >	BTUART–6		J27–11	CH_B

Appendix I

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