Thermo-Mechanical Reliability of Low-Temperature Sintered Attachments on Direct Bonded Aluminum (DBA) Substrate for High-Temperature Electronics Packaging

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Abstract

This study focused on the development and evaluation of die-attach material and substrate technology for high-temperature applications. For the die-attach material, a low-temperature sintering technique enabled by a nanoscale silver paste was developed for attaching large-area (>100 mm^2) semiconductor chips. The nanoscale silver paste can be sintered at a much lower temperature (<300 ^oC) than in the conventional sintering process (>800 ^oC), and at the same time reached about 80 vol% bulk density. Analyses of the sintered joints by scanning acoustic imaging and electron microscopy showed that the attachment layer had a uniform microstructure with micron-sized porosity with the potential for high reliability under high temperature applications.

We also investigated the effects of a large temperature cycling range on the reliability of direct bonded aluminum (DBA) substrate. DBA substrates with different metallization were thermally cycled between -55 ^oC and 250 ^oC. Unlike with the DBC substrate, no delamination of aluminum from the aluminum nitride ceramic base-plate was observed for the DBA substrates. However, aluminum surface became roughened during the thermal cycling test. It was believed that in the high-temperature regime, the significant amount of thermomechanical stress and grain-scale deformation would cause recrystallization and grain-boundary sliding in the aluminum layer, which would further lead to the observed increase in surface roughness. The influence of metallization over the aluminum surface on the extent of surface roughness was also characterized.

In addition to evaluating the reliability of nanoscale silver paste and DBA substrate individually, this work also conducted experiments that characterize the compatibility of nanoscale silver paste on DBA substrate in terms of reliability in a high-temperature environment. In the large-area attachment, the sintered silver was found to be very compliant with the deformed aluminum. The device-to-silver and silver-to-substrate interfaces remain intact after up to 800 cycles. No large scale delamination and horizontal cracks were observed. However, some vertical crack lines began to show after certain number of cycles. It was believed that these vertical cracks were caused by the thermomechanical stresses in the sintered silver layer. In addition, with regard to the thermal performance, since most of the heat was generated from the semiconductor devices and were transferred vertically through the die-attach material to substrate, these vertical cracks were also considered more advantageous than horizontal cracks.

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Chapter 1. INTRODUCTION

Electronics packaging provides mechanical support, device protection, cooling, and electrical connection and isolation for power electronics components. The overall performance of a single chip power package, a multichip power module, and an entire power system is not only determined by the power devices and the electrical circuits, but also strongly depends on the packaging technology.

There is a growing demand for electronic signal processing at elevated temperatures. With the rising power density in electronic systems due to miniaturization and the increase in switching frequency [1], current and future needs in under-the-hood automotive [2], aircraft [3], aerospace [4,5], and well-logging industries [6] require the operation of electronics at temperatures greater than 200^{o}C [7,8]. In addition, replacing silicon (Si) devices with wide-bandgap semiconductor devices that are capable of operating at higher temperatures, e.g. silicon carbide (SiC) and gallium nitride (GaN), could alleviate the cooling difficulties of high-power and high-density electronics, whose own waste heat would increase internal temperatures beyond reasonable limits for conventional device technologies [9,10]. However, the packaging supporting such wide-bandgap devices is inadequate in electrical interconnection, thermal management, and thermomechanical reliability in high-temperature operation environments. Many systems must operate under derated conditions or must accept severe mass penalties required by coolant systems to maintain electronic temperatures below critical levels. High-temperature packaging technologies and design methodologies are therefore becoming a necessity, as they are essential to realizing high performance and high reliability in electronic systems. Figure 1.1 shows the schematic layout of a simplified packaging structure containing most of the packaging components.

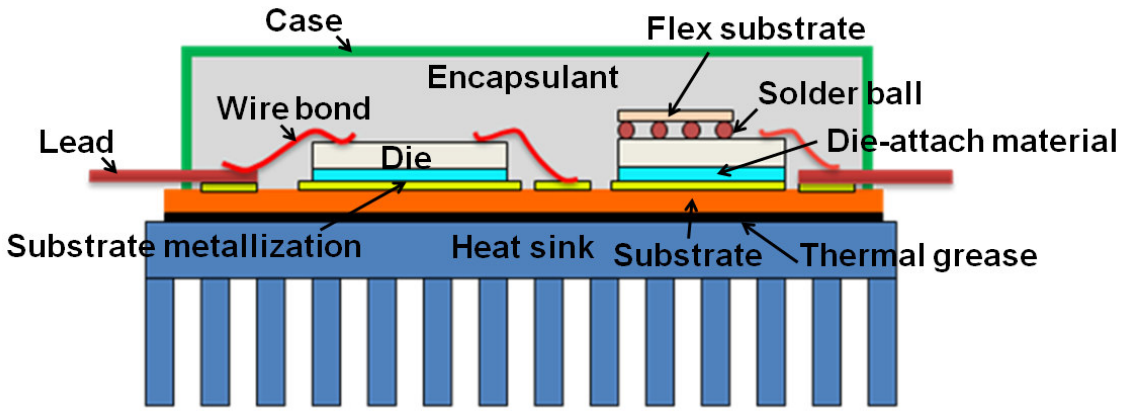


Figure 1.1. Schematic layout of a simplified package.

A basic power semiconductor module mainly consists of seven parts:

- Power semiconductor chips – Si, SiC, GaN (IGBT, MOSFET, JET, …);
- Insulating substrate with metallization (circuit conductor) – usually a ceramic or Si-based substrate with Au, Ag, or Cu with metallization;
- Baseplate – Cu metal, Cu composites, carbon-reinforced composite, AlSiC, etc;
- Bonding material – Typically Pb-based solder, Pb-free solder, etc;
- Encapsulate material – Typically conformal coating for environmental and mechanical protection;
- Power interconnections – Large Al or Au wires for interconnections, pressure-type contact, and metal terminals;
- Plastic case and cover – Thermoset and thermoplastic material.

These materials are all bonded together and are in close contact with each other. Since the materials behave differently under various environmental electrical and thermal stresses, building a power electronics module with high performance and high reliability relies heavily on the study and the selection of

these materials. Thermal, electrical, mechanical, and chemical properties are the major properties that should be considered in material selection.

The ability to use electronic systems at elevated temperatures will not only make new products possible but it will also decrease the cost and increase the reliability of current products by removing the need for large, heavy, complex cooling systems and the cabling and interconnections required for remote placement of the electronics. However, there are many technical challenges involved in developing electronic systems that will operate at elevated temperature. These range from proper IC design to the appropriate use of passives, and from the development of robust packaging structures to the use of the latest thermal management techniques.

1.1. Significance of high-temperature electronics packaging

Electronics that operate and control functional systems must currently be protected from extreme environments [11]. Major benefits to system architecture would result if cooling systems for electronics components could be eliminated without compromising system performance (e.g., power, efficiency, speed). The existence of commercially available high-temperature electronic packaging would provide significant benefits in such area as:

- Sensors and controls for automobiles and aircraft;
- High-power switching devices for electric power industry, electric vehicles, etc.; and
- Control electronics for the deep-well drilling and nuclear power industry.

Because of the requirement of operating in a high-temperature environment, the following section is dedicated to a short survey of the most relevant applications that are currently in great need of new high-temperature electronics packaging techniques. These types of systems currently experience harsh

industrial environments and temperatures in excess of 150 ^{o}C, but are only capable of surviving this environments for short durations [12]. Future systems will increase the duration of high temperature exposure many times and will operate at higher temperatures as shown in Table 1.1[13,14]. Depending on the application, these higher temperatures are typically accompanied by severe environmental conditions [15,16].

Table 1.1. Temperature requirements for applications in harsh environments.

Industry	Operating temperature requirements
Automotive	150 ^{o}C to 200 ^{o}C
Aircraft	250 ^{o}C to 300 ^{o}C (jet engines and avionics) 860 ^{o}C (skin conditions at Mach 5)
Spacecraft	200 ^{o}C to 400 ^{o}C
Well-logging	175 ^{o}C (oil), 225 ^{o}C (gas), 300 ^{o}C (steam), > 600 ^{o}C (geothermal)
Nuclear power systems	200 ^{o}C to > 400 ^{o}C, radiation hardened

Automotive industry

The automotive industry is often cited as the primary near-term for high-temperature electronics. While the automotive environment is stressful to electronic systems, the stress is rarely in the form of simple heat. Conventional vehicle architectures with an open-bottomed front engine compartment, generous underhood and underbody airflows, a metal heat-dissipating body and frame structure, and access to a water-cooling circuit leave very few locations within a vehicle that regularly achieve temperatures significantly above 100 ^{o}C. These locations are mainly near the exhaust system or brakes and can usually be avoided when placing electronic components. Occasional problems with reliability due to high temperatures (as high as 150 ^{o}C) have been addressed by combinations of heat shielding, redirected airflow, blowers, or simple component relocation. Except for rare cases of architectural errors, the major challenge to

reliability of automotive electronics is the combination of rapidly changing environmental stresses (temperature and humidity cycling), exposure to corrosions and solvents, and an economic mandate for low-cost packaging. With careful attention to device and circuit layout, wire-bond and lead-frame integrity, the choice and use of polymer packaging materials, and strict process control, automotive electronics actually meet or exceed military specifications at a small fraction of the cost and volume [17-19].

However, power electronics are rapidly proliferating in automobiles. Figure 1.2 [20] indicates several systems that include high-power actuators. Full, active suspension requires several tens of kilowatts. Electric and hybrid vehicles are totally dependent on power electronics for efficient operation of motor and braking systems.

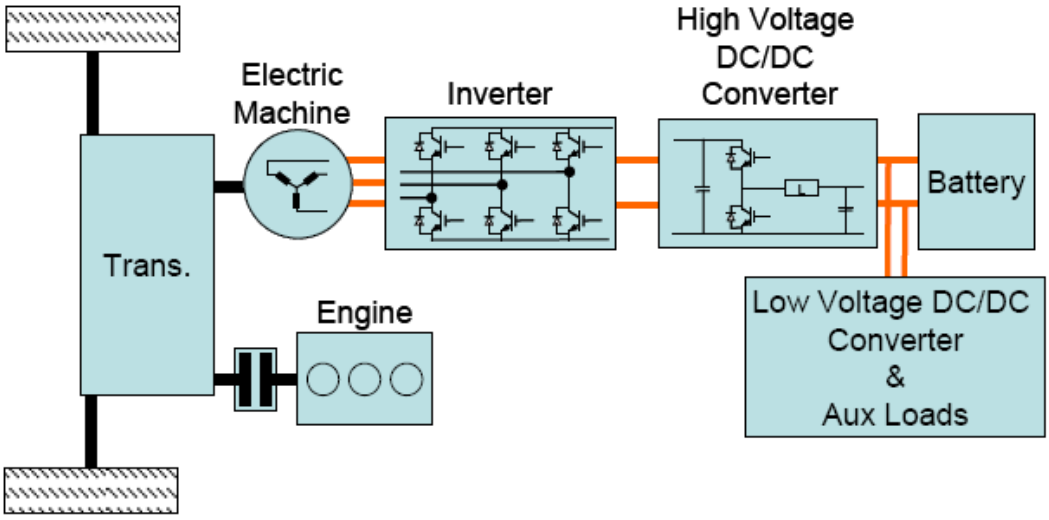


Figure 1.2. Parallel hybrid vehicle configuration [20].

There are two types of high-temperature issues for power electronics. First, in conventional combustion-powered vehicles, the electronics must be placed somewhere that is preferably near or within the device they control. For example, the drivers for electric, active front-suspension components share the underhood environment, while the motor and alternator for torque leveling are cooled only by

the engine oil and may reach 300 ^{o}C. For electric and hybrid vehicles, the wiring weight, resistive losses, and radio frequency emissions are minimized by placing the power electronics within the motor housing. To minimize weight, these motors are sized such that they may produce several times their continuous-service power for periods of several seconds. This translates to a rapid temperature rise that is currently limited to 180 ^{o}C only by the magnetic properties of the permanent magnet rotor. Integral power electronics must survive repeated and rapid excursions to at least this temperature. Second, power devices generate considerable internal heat. This heat must be dissipated to prevent thermal runaway and destructive failure. In many locations, a heat-sink for large amounts of heat is unavailable. The smaller package size afforded by a higher-temperature packaging technology is of considerable value in terms of thermal management.

In summary, two clear needs can be identified for automotive electronics. First is the need for a low-cost, highly reliable technology for operation at an intermediate temperature, perhaps 200 ^{o}C. This need might be served by modification of current silicon-based technology. Second is the need for power electronics able to function in elevated ambient temperatures with restricted heat-sinking. As current silicon-based power technology is largely limited by internal heat generation, a switch to a wide-bandgap semiconductor is dictated.

Gas turbine engines

High-temperature electronics are essential to the development of multiplexed systems for gas turbine engine control. In present control systems, all electronics are centralized in a protected area that is cooled with ambient air or fluid. This architecture has proven satisfactory for some time, but as the requirements for engine control become increasingly complex, the wire harness and connectors associated with point-to-point architecture have become major weight and reliability issues. A solution to this problem is to introduce a

multiplexed architecture in which wire harnesses are replaced with common busses, a change that demands high-temperature electronics.

The environments for electronics in an aircraft engine cover a wide range: 175 – 800 ^{o}C. Early phases of the application require electronics and optics to operate at 175 ^{o}C, while an intermediate phase calls for 250 ^{o}C. It is anticipated that the heat-sink temperatures may be as high as 350 ^{o}C [21]. While it is neither desirable nor cost effective to construct the whole system to survive the highest temperatures, any increase in operating temperatures offers a corresponding increase in design flexibility.

Aerospace industry

Engines demand the highest temperature requirements for current aircraft, but temperature requirements will rise in many other critical areas as vehicle speed increases. An example is the control of the engine inlet guide vane for the high-speed civil transport, which requires that the moderately complex electronics driving the guide vane actuate for prolonged periods at 200 ^{o}C.

In high-performance aircraft, a generic problem appears: as speed and altitude increase, the ability to dissipate waste heat into the atmosphere decreases [12]. There are no locations in the aircraft that remain below 125 ^{o}C or that can be conveniently reached by the cooling system. Many electronics systems, including avionics, radars, and communications equipment, must be derated in performance to maintain even the minimal acceptable reliability at the margins of their operating ranges. When cooling to the temperature of the outside air is insufficient, the cooling techniques currently in used force tradeoffs between speed, altitude, and systems shutdown.

Space vehicles and exploration

Problems directly related to high temperature are rare once in space. Space is cold, and intense sunlight may be reflected with high efficiency. However, there

are several situations in which high temperature may be an issue. First, the sensing and control of rocket boosters and thrusters may require proximity to the hot plumbing associated with combustion. Such problems and issues are very similar to those for aircraft jet engines, with the exception that maintainability and long-term reliability are less important. Second, some space exploration vehicles must enter hot environments. A proposed balloon-borne probe of Venus' atmosphere must operate at 325 ^{o}C, while a Venus lander must endure 460 ^{o}C [22]. Closer approaches to Mercury or the sun would also require higher-temperature electronics. Third, material and design factors that support high-temperature electronics operation would also enhance resistance to upsets and damage from the unavoidable flux of cosmic radiation [23].

Well-logging industry

Deep wells for the exploitation of petroleum and other minerals, and geothermal applications comprise an important market for high-temperature electronics. Modern petroleum exploration involves elaborate probing of wells during drilling. For this reason, oil exploration companies have been some of the earliest customers for high-temperature electronics. Earlier efforts have resulted in fairly complex circuits built of discrete devices that are able to operate for periods of several hundred hours at temperatures up to 300 ^{o}C. Since it is expensive to withdraw and replace probes during drilling, reliability is of extreme importance. A more sophisticated component would enable far more reliable and effective logging tools. Figure 1.3 [24] depicts the temperature environments of many well-known deep wells around the world.

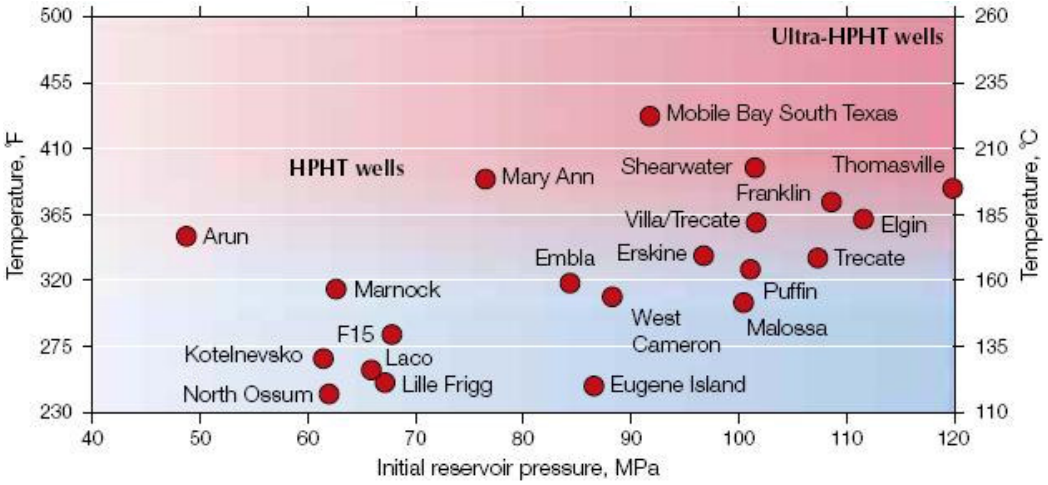


Figure 1.3. Temperature and pressure conditions of various deep wells [24].

1.2. Current technologies for device attachment

Electronic systems are manufactured by packaging and interconnecting semiconductor and other devices on a common interconnection substrate. The semiconductor devices may be individually packaged and then assembled onto the substrate, or unpackaged devices may be assembled onto the substrate and then the entire assembly packaged. Selection of proper die-attach material is important not only in providing sufficient mechanical bonding strength of the attached device to the substrate, but it is also crucial in the overall packaging thermal management. Some of the basic characteristics of a die-attach material are:

- Sufficient adhesion to the device and to the substrate so that the device does not debond from the substrate;
- Compliancy, to provide stress relaxation behavior to reduce thermomechanical stresses on the device;
- High thermal conductivity to facilitate thermal management;
- CTE that matches the device and substrate;
- Reasonable low processing temperature, while retaining stability at operating temperature.

Currently there are three major techniques used in bonding the devices to the substrate: reflow of solder alloys, curing of conductive epoxy, and low-temperature joining technique (LTJT). In the following section, basic principles and working mechanisms of these attaching techniques are introduced.

1.2.1. Solder reflow

Solders are alloys of two or more metals. When these metals are alloyed together, the melting point of the alloy can be considerably lower than the melting point of either of the individual starting metals. This is the phenomenon which makes the soldering process possible. In the soldering process, the solder is placed between two metal surfaces to be soldered. Heat is applied to warm the solder alloy and eventually melt the solder layer. During melting, the molten solder dissolves a portion of these two surfaces and, when the solder cools, a junction or solder unit is formed, joining the two metal surfaces.

For electronics packaging applications, the most commonly used interconnect material is eutectic tin-lead (63Sn-37Pb) solder. The eutectic SnPb solder is the standard by which all other interconnect materials are compared. The SnPb eutectic alloy melts at approximately 183 ^{o}C and solder processing is normally performed around 220 ^{o}C. Figure 1.4 [25] shows the suggested temperature profile of using this solder. This solder has a two-phase structure: a tin-rich phase and a lead-rich phase. Figure 1.5 [26] depicts a SnPb phase diagram showing the melting temperature as a function of composition.

For high temperature applications, solder alloys must have a small two-phase region for ease of processing. A eutectic alloy has the optimum condition, a direct transformation from liquid to solid. If the two-phase region is too large, the joint members have the opportunity to move with respect to one another during solidification. This results in an irregular, coarse, and sometimes cracked

joint surface that often has poor mechanical properties. Therefore, most solder alloys for interconnections are eutectic alloys.

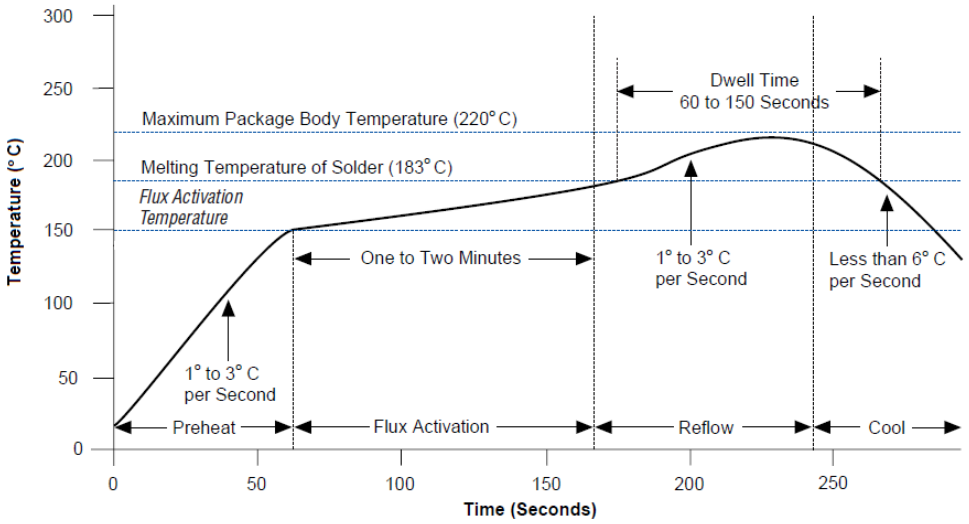


Figure 1.4. Suggested heating profile for Sn37Pb eutectic solder [25].

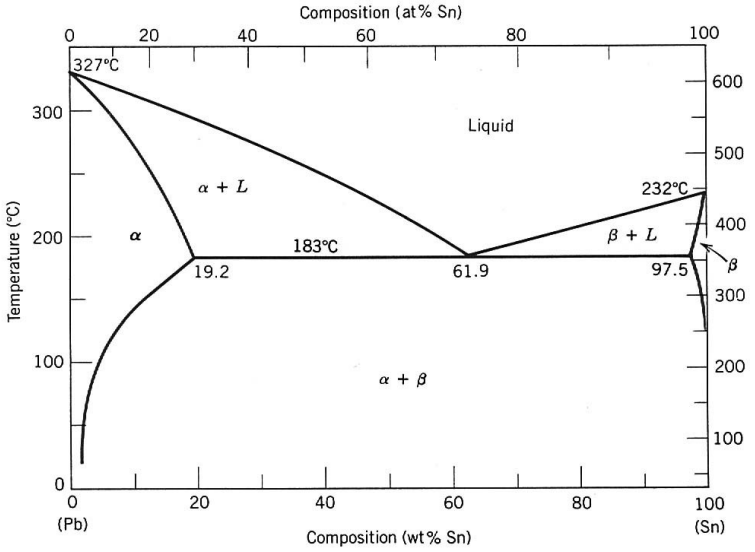


Figure 1.5. SnPb phase diagram [26].

SnPb solder wets metalized surfaces well when the surfaces are clean. Flux is often used to remove oxides on the metalized surfaces and assist in the spreading of the solder. As the solder wets and spreads over the surface, the tin reacts with the metallization to form an intermetallic compound. After solidification, eutectic SnPb solder has excellent electrical conductivity. The solder also has

adequate time-dependent deformation characteristics allowing it to take strain caused by the CTE mismatch in joined materials without damaging the component or board. The mechanical and thermomechanical stability of the alloy is sufficient for many electronics packaging applications.

High-lead solder is a high operating temperature interconnect alternative. Although the composition is outside the eutectic, the two-phase temperature band is small. The high lead-content 95Pb-5Sn solder alloy has a melting point of 300^{o}C. This alloy has found extensive use as a first-level solder interconnect for flip-chip applications joining chips to chip carriers. Other alloys similar to the 95Pb5Sn alloy have similar properties, 95.5Pb1Sn1.5Ag was developed to minimize intermetallic growth on silver metallization, and also has a high melting point of 309 ^{o}C [27]. These alloys consist of a matrix of large lead grains with small precipitates of tin in the bulk of the solder joint.

With a melting temperature above 300 ^{o}C, the high lead-content solder alloys offer the ability to make interconnects that will not melt for almost all high-temperature electronics applications. However, there are a few drawbacks of these alloys. The low tin-content of the alloys raises the melting temperature and also decreases wetting behavior. The reaction of tin at the metallization interface enhances wetting, and as the tin-content decreases, the wetting behavior suffers [28]. The processing temperature for the high lead-content solders must also exceed 340 ^{o}C to get good solder reflow. The processing equipment and other electronic packaging materials must be redesigned to withstand these temperatures.

Lead-free solder alloys that are best suited for high temperature applications are based on the Sn3.5Ag and the Sn5Sb eutectic alloys. Potential ternary additions of antimony, silver, bismuth, or copper can be made to the tin-silver solder. Table 1.2 lists a few eutectic alloy compositions, and their related melting

temperatures. This set of alloys melts in the range of 210 ^{o}C to 234 ^{o}C. At these melting temperatures, the operating temperature of the electronics systems can be raised to above 200 ^{o}C.

Table 1.2. Melting temperatures of some high-temperature solder alloys.

Alloy composition (wt. %)	Melting temperature (^{o}C)
63Sn37Pb	183
95Pb5Sn	300
95Sn5Sb	234
96.5Sn3.5Ag	221
Sn4.7Ag1.7Cu	217
Sn3.4Ag4.8Bi	210

The wetting performance of the high tin-content solders is not as good as that of lead-containing alloys, but results in the formation of good joints by reflow or wave-soldering methods. The presence of lead improves wetting by lowering the surface tension of molten tin. High tin-content solders have a higher surface tension, so they do not wet as well as Sn37Pb, but they react with the substrate metallization to form a good metallurgical bond, as proven by the interfacial intermetallic layer that forms.

A drawback of SnAg and SnSb alloys is that their response to time-dependent deformation is much slower than SnPb (roughly an order of magnitude slower at the same stress level), so damage can be imposed on the jointed components. These solders also exhibit a brittle fracture mode when deformed in tension. The failure path is along the interface between the intermetallic and the solder [29]. The energy required for fracture is about half that for Sn37Pb, which fails through the solder. This failure mode could be important when tensile stresses are imposed at room temperature and lower. The thermomechanical fatigue life of the high tin-content, lead-free solder is better

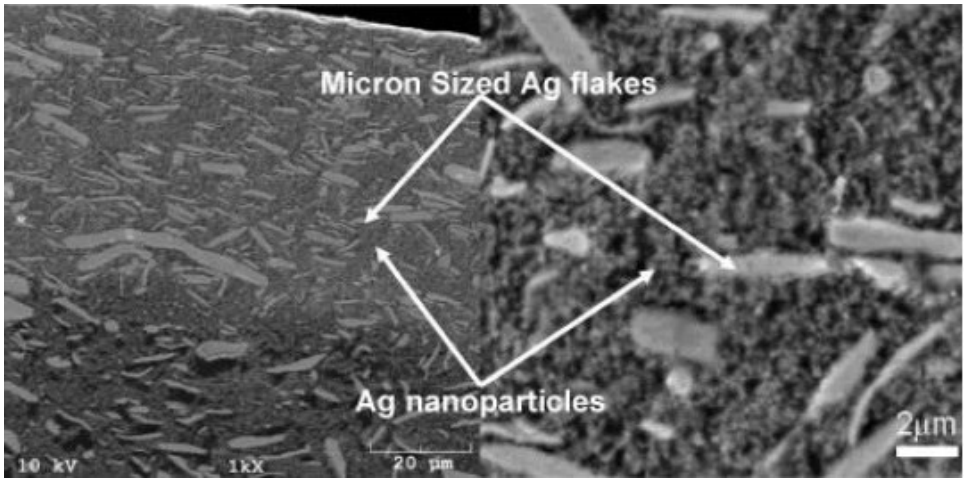
than that of lead-based alloys. The Sn3.5Ag and SnAgCu alloys have lives about 10% longer than SnPb; SnAgBi has a life over twice that of SnPb. This is due to the limited microstructural evolution that occurs in the tin-matrix of lead-free alloys and the limited time-dependent deformation of the alloys. The tin-grain size in SnAg solders is much finer than in high lead-content alloys, so the deformation mechanism of grain boundary sliding and rotation does not result in the rapid failure found with 95Pb5Sn. Thus, one of the benefits in using a high-temperature lead-free solder is improved reliability under thermomechanical fatigue conditions.

1.2.2. Conductive epoxy

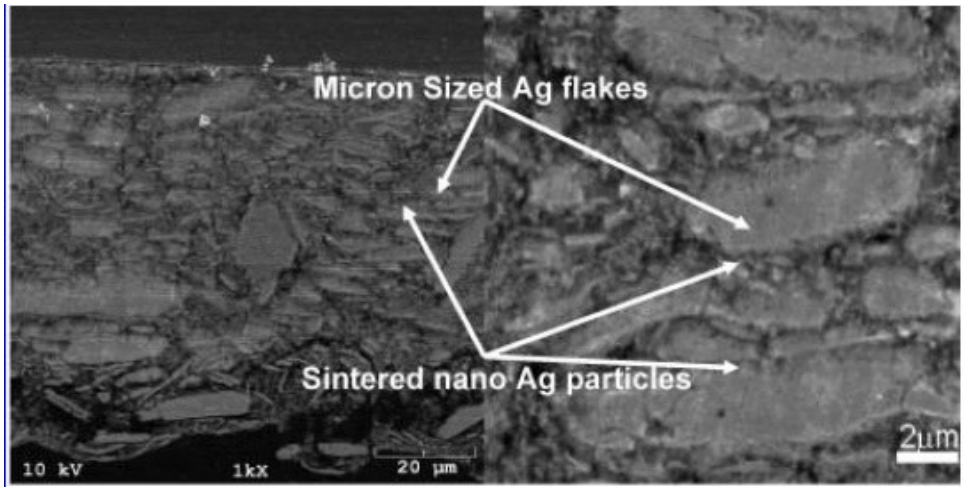
Electrically conductive adhesives (ECAs) are composite materials consisting of a dielectric curable polymer and metallic conductive particles. ECAs are low processing temperature alternatives to solder alloys. The polymer is an adhesive material that chemically reacts with metals to form a bond. The metallic particles in the adhesive form a network in the cured joint that forms a conduction path from the package to the board. The number of cross-links determines the glass transition temperature (Tg) of the polymer. In general, the more-cross links, the higher the glass transition temperature. A curing agent is added to a thermoplastic material to cause the cross-linking reaction. Curing can be performed using UV light, heat, or catalysts. Thermosetting materials are harder than thermoplastic, but can be processed and cured below Tg and do not become “molten” above Tg. The curing operation is not reversible, making repair difficult.

A number of metals have been used for the conductive portion of the ECA. The metals typically are in the forms of flakes, plates, rods, fibers, or spheres. The size of the metal particles ranges between 5 and 20 μm. For the ECA to have suitable strength and electrical conduction requires a tradeoff in metal filler content. The greater the metal content, the better the electrical conduction, but the poorer the strength of the adhesive. The metal content depends on whether

the adhesive is an isotropic or anisotropic conductor, but does not usually exceed 40% by volume. Figure 1.6 shows the SEM images of two ECAs with different metallic filler concentration [30].



(a)



(b)

Figure 1.6. SEM images of electrically conductive adhesives with silver particles and flakes as conductive filler (a) 20% and (b) 60% [30].

The types of metal used in ECAs are silver, gold, nickel, or copper or variations of these. The silver-filled ECAs are the most common, because of the cost of the metal is moderate and it has good electrical conductivity and low reactivity with oxygen. Gold has better physical properties than silver but the cost is too high for most applications. Nickel is less expensive, but also has lower

conductivity and has been found to corrode when aged in a humid environment resulting in poor adhesion between the nickel and the epoxy matrix. Copper fillers oxidize rapidly and delaminate from the polymer matrix.

The bonding surface being joined must be oxide-free for the adhesive to form a cohesive joint. Bare copper gives very poor adhesion. The adhesives do not wet or react with metal oxides, and thus are very similar to solders. To overcome this problem, the copper can be plated with nickel and a thin layer of gold. Gold is an excellent bonding surface because its surface oxide is negligible and it provides a diffusion barrier for the nickel.

One of the greatest concerns with the reliability of silver-filled conductive adhesive is silver migration. In this mechanism, the silver is ionized and migrates in a humid environment, forming electrically conductive dendrites that can result in electrical shorts between interconnects. Silver migration can only occur if the silver particles are directly exposed to a corrosive, humid environment. The silver in ECA joints is encapsulated inside the polymer, and it is difficult to promote dendrite growth from within the joint if corrosion does occur. A survey of previous studies indicates that silver migration has never been observed in any accelerated corrosion tests [31,32].

1.2.3. Low-temperature joining technique (LTJT)

In the late 1980s, an alternative technique for the joining of large-area silicon devices with molybdenum plates was discovered [33]. The so called low-temperature joining technique (LTJT) is based on the sintering of silver powders and flakes. These silver powders and flakes are covered with an organic additive to protect them from low temperature (room temperature) agglomeration and aggregation. This additive is an ingredient for the production process of the silver powders, and would be oxidized and burned out when the temperature reaches 210 ^{o}C or above. Therefore for LTJT process, an environment with adequate

oxygen is needed to help remove the excessive organic additive around the silver particles and flakes [34]. Unlike the solder reflow process, the mechanical bonding of the LTJT technique is formed by a sintering process. This sintering process contains no reaction in liquid phase, because the melting point of silver is 960 ^{o}C, much higher than the processing temperature. Therefore it is predicted that the interconnection formed by the LTJT technique possesses good stability even at temperatures higher than the processing temperature.

Because the sintering bonding strength is based on the atomic diffusion of silver into joined materials, the bonded surface must have compatible metallization with silver. The diffusivity of silver atoms in these metallization layers must be reasonably high so that the as-formed bonding has a certain mechanical strength. In addition, the bonded materials must exhibit oxide-free surfaces [35]. Often the surfaces are prepared with a diffusion barrier consisting of nickel and a thin noble metal finish or high purity electroless plating of silver, gold or platinum. The standard LTJT process consists of the following steps:

- Application of silver paste (powders and flakes with organic solvent);
- Drying (low temperature organic solvent evaporation);
- Placing the components/devices;
- Sintering of the silver paste, with pressure assistance.

Silver paste can be applied using by screen printing, stencil printing, spray coating, automated dispensing, or through a foil transfer method. The silver flakes are suspended in organic solvent with a viscosity adjustable to the respective application method. After applying the silver paste, the organic solvent has to be evaporated at a relatively low temperature, about 150 ^{o}C. By removing the organic solvent, the green density of the silver flakes is significantly increased; thus the densification rate can be increased during the sintering process. Components or devices will be placed on top of the paste after the drying stage. A

hardened rubber is employed to cover the components, mainly to prevent direct mechanical contact between the metallic hydraulic press and the semiconductor devices, thereby protecting the devices during the process.

For the sintering process, a hydraulic press is used to provide uniaxial and isostatic pressure. Up to 40 MPa pressure is usually applied at 230-250 ^{o}C to help promote the sintering of the silver flakes, as well as to secure the devices in place. The sintered silver has a porosity of about 15%, and provides excellent thermal, electrical, and mechanical properties compared with solder alloys. Table 1.3 shows the properties of the sintered silver after the standard LTJT process [32,36].

Table 1.3. Material properties of the sintered LTJT silver layer.

Melting temperature	961	^{o}C
Density	8.9	g/cm^{3}
Electrical conductivity	4.1	10^{5} (Ω-cm)$^{-1}$
Thermal conductivity	250	W/m-K
Specific heat	0.245	J/g-K
Coefficient of thermal expansion	20	10^{-6}/K
Young's modulus	52	GPa
Tensile strength	150	MPa
Shear strength	40	MPa

Because of the high melting temperature of silver, LTJT is expected to have high reliability even at temperatures above 300 ^{o}C. The thermal conductivity is more than three times better than that of soft solder attachment. With a thinner bondline thickness, of about 20 to 30 μm, a very low thermal resistance can be achieved. In addition, the electrical conductivity is much better than that of solder too. Figure 1.7 shows one diode attached to the DBC substrate by LTJT technique [37]. Notice that LTJT is also employed to attach silver ribbons to the top of the diode, which also has the potential to replace wire-bond or ribbon bond to provide greatly improved reliability during power cycling and thermal cycling tests.

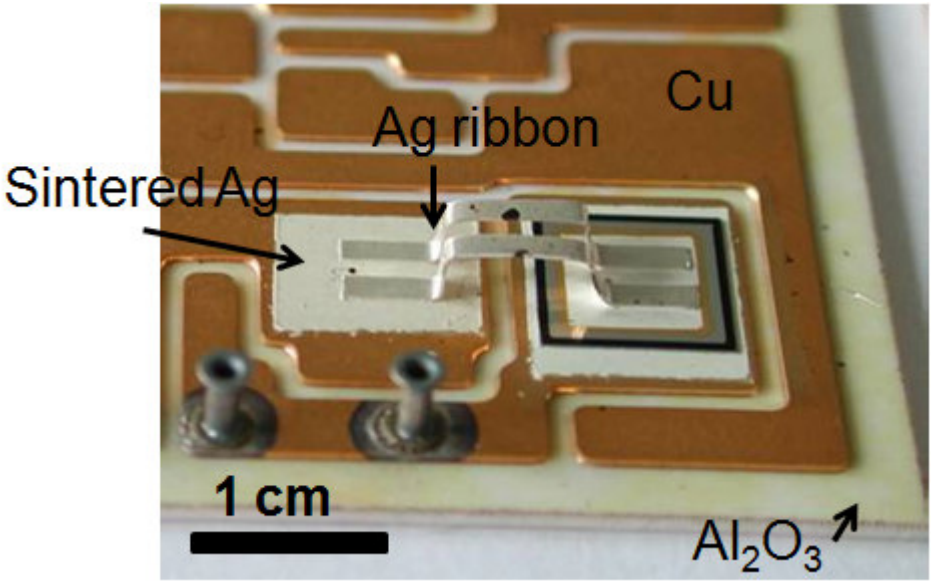


Figure 1.7. Diode attached to DBC substrate by LTJT technique [37].

Because of the high melting temperature of the sintered silver, it is expected that the reliability of the LTJT layer is much better than that of the solder layer. A significant improvement in the temperature cycling reliability test can be obtained by applying the LTJT technique in a large-area device attachment [38]. The results show at least 10 times longer lifetime for sintered silver than standard solder layers. Power cycling results of modules with an LTJT layer between a silicon chip and DBC substrate also prove the excellent stability of the LTJT layer. The main failure of the tested modules is the wire-bond lift-off [39]. When the top-side wire-bond interconnection is replaced by another LTJT layer, the power cycling capability was found to be over two times higher than that of single-sided LTJT.

Table 1.4 lists some basic properties of the sintered silver layer compared with properties of some solder alloys. With the exceptionally high application temperature, excellent electrical and thermal properties, and proven long life-time in temperature cycling and power cycling tests, LTJT has become more and more popular in the power module industry, and is now finding its way in replacing many of the solder alloys and conductive epoxies in various applications.

Table 1.4. Material properties of sintered silver compared with solder alloys.

COMPARISON OF MATERIAL PARAMETERS FOR THE SILVER-DIFFUSION SINTER LAYER AND A STANDARD SOLDER LAYER. (MPA IS MEGA-PASCALS)					
PARAMETER	UNITS	Ag PURE SILVER	Ag SINTER LAYER	SnAg SOLDER LAYER	Ag vs. SnAg FACTOR
Liquidus	°C	961	961	221	4
Electric Conductivity	MS/m	68	41	7.8	5
Thermal Conductivity	W/mK	429	250	70	4
Density	Gr/cm3	10.5	8.5	8.4	1
CTE	µm/mK	19.3	19	28	1
Tensile Strength	MPA	139	55	30	2

1.3. State-of-the-art substrate technologies for power electronics packaging

A major challenge in today's high-temperature electronics packaging is the lack of reliable packaging materials with good performance, especially for the substrate and the die-attach materials. While components, such as semiconductor devices, die-attach, wire-bond, connectors, and housing materials, are the key areas attracting the most concerns, much of the reliability of the electronic system is determined by the quality and the performance of the substrates and the interconnections.

Electronic systems are manufactured by packaging and interconnecting the semiconductor and other devices on a common interconnection substrate. The semiconductor devices may be individually packaged and then assembled onto the substrate, or unpackaged devices may be assembled onto the substrate and then the entire assembly is packaged. The substrate provides:

- Mechanical support for the components;
- Conductive traces for electrical interconnection between the various active and passive elements;
- Heat removal path from the devices.

In addition, resistive and dielectric layers may be included to form resistors and capacitors directly on the substrate. In general, the substrates may be fabricated using organic or inorganic technology. However, since most of the organic materials used as packaging substrate cannot withstand temperature as high as 250 ^{o}C, only the inorganic substrate technologies are considered in this research, and are discussed below.

1.3.1. Insulating substrate

The insulating substrate serves as the supporting structure for the circuit of the power modules. It acts as the surface for depositing conductive, dielectric, and resistive materials that form the passive circuit elements [40]. It is also a base for mechanical support for all active and passive chip components; therefore it must be strong enough to withstand different environmental stresses. Electrically, the insulating substrate must be an insulator to isolate various conductive paths of the circuit. It must be able to withstand an RMS AC voltage of 2500 V applied between any terminal and the case, including the base plate, for one minute [38]. For many applications, as the power density of the module becomes higher and higher, the heat generated from the power devices must be able to efficiently dissipate to the environment. Therefore the substrate material should have sufficient thermal conductivity to remove the heat from the devices.

In addition, a high degree of surface smoothness is required for adhesion of films, fine conductor lines, and spacings. Surface flatness is desirable to minimize processing problems during screen-printing, photomasking, etc. Non-flat surface lead to microcracks and poor localized thermal conduction. The substrate material most suitable for power applications should be determined by the electrical, thermal, mechanical, and chemical requirements. Table 1.5 and Table 1.6 [41,42] list some of the mechanical and thermal properties of the most popular insulating substrate material used in industry.

Table 1.5. Mechanical Properties of Insulating Substrates [41].

Material	Tensile Strength (MPa)	Flexural Strength (MPa)	Elastic Modulus (GPa)	Surface Finish (μm)	Density (kg/m^3)	Machineability
Al_2O_3 (96%)	127.4	317	310.3	1.0	3970	Good
Al_2O_3 (99%)	206.9	345	345	1.0	3970	Good
AlN	310	360	310	1.0	3260	Good
BeO	230	250	345	15	3000	Good
SiC	17	440	412	-	3160	Fair
SiO_2	96	30	69	-	2190	Good
Si_3N_4	96	932	314	-	2400	Good
IMS	392	6	-	-	2700	Good

Table 1.6. Thermal Properties of Insulating Substrates [42].

Material	Thermal Conductivity (W/m-K)	CTE (ppm/K)	Heat Capacity (J/kg-K)	Maximum Use Temperature (^oC)	Melting Point (^oC)
Al_2O_3 (96%)	24	6.0	765	1600	2323
Al_2O_3 (99%)	33	7.2	765	1600	2323
AlN	150 - 180	4.6	745	>1000	2677
BeO	270	7.0	1047	-	2725
SiC	120	4.6	675	>1000	3100
SiO_2	1.5	0.6	-	>800	-
Si_3N_4	70	3.0	691	>1000	2173
IMS	4	25	-	-	-

Notice that most of the material properties are functions of temperature, it is of practical use to measure and quantify how these properties change with temperature. Figure 1.8 [43] and Figure 1.9 [44] depict the thermal conductivities and coefficients of thermal expansion (CTEs) of some insulating substrate materials that change with temperature. It is important to use the right number when designing a reliable power module.

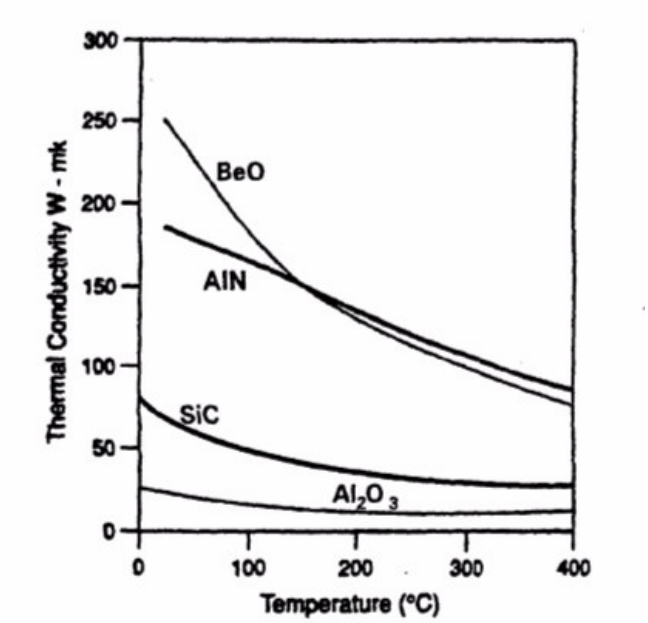


Figure 1.8. Thermal conductivities of some ceramics [43].

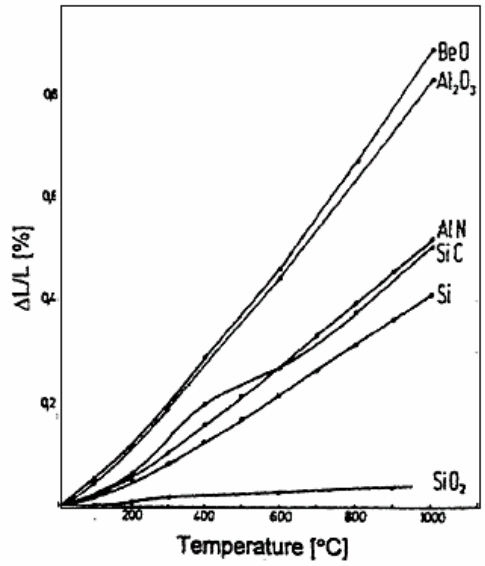


Figure 1.9. Thermal expansions of some ceramics in comparison to those of SiC and Si [44].

1.3.2. Metallization technologies

For power semiconductor applications, the metallization on the insulating substrates should possess the following characteristics [45-47]:

- Thermal:
  - High thermal conductivity (> 200 w/K-m);

- Matching CTE with insulating substrate;
- High thermal stability – greater than 1000 ^{o}C in order to be compatible with the direct bonding and brazing operations;
- High thermal fatigue capability – greater than 1000 cycles with no failure at the interface with the substrate;

- Electrical:
  - Able to conduct high current density;
  - Low electrical resistivity – typically, ohmic drop across the metallization should not exceed one-tenth of the IGBT's V_{CESAT}.
- Mechanical:
  - Strong adhesion to the substrate – high peeling strength;
  - Al wire-bondable;
  - Solderable for standard solder;
  - Compatible with standard processing equipment;
- Chemical:
  - Photo-etchable – designed pattern can be easily formed;
  - High chemical resistance against standard processing solvents;
  - Non-toxic;
  - Good corrosion resistance;
  - Chemically inert.

In the following section, several state-of-the-art metallization techniques including thick film, thin film, insulated metal substrate (IMS), and direct bonded copper (DBC) are briefly reviewed. These metallization techniques are widely used in applications with different power densities and operating temperature requirements.

1.3.2.1 Thick film

In the thick-film hybrid process, the ceramic and glass/ceramic dielectrics can be metallized prior to firing (co-fired) or after firing. The individual layers are deposited onto the pre-fired ceramic or glass/ceramic substrate by screen printing then firing.

The typical thickness of the conductor in thick-film technology is about 15 µm to 200 µm. Gold-based conductor systems can be used to fabricate thick-film hybrids for 300 ^{o}C operation [48], and should be suitable up to 500 ^{o}C [49]. A silver-based conductor is an alternative to a gold-based system. It has a lower cost but is susceptible to silver migration at high temperatures. Also, silver-based conductors react with either aluminum or gold wire bonding. The aluminum-silver couple is prone to corrosion; and for the gold wire, silver is found rapidly diffuse into the gold, creating a void around the bond at high temperatures [50]. Therefore, silver-based conductors are not typically used above 200 ^{o}C.

Most of today's thick-film technology use alumina substrates. Only a few thick-film pastes have been developed that are compatible with aluminum nitride (AlN) substrates, which are specifically designed for high-temperature applications. However, their use at elevated temperatures has yet to be evaluated.

1.3.2.2 Thin film

Thin-film materials are generally deposited by vacuum deposition (evaporation, sputtering, chemical vapor deposition), spin coating, and plating, after which the patterns are formed by photolithography and etching. Thin-film technology is compatible with alumina, aluminum nitride, and glass/ceramic substrates. The resulting fine-line patterns are particularly suitable for high-density interconnections and high-frequency application.

The typical thickness of the conductor in the thin-film technology is about 2.5 µm or less, and the current-carrying capability is limited to a few amperes. For high-temperature applications with aluminum metallized semiconductor devices, aluminum substrate metallization provides a mono-metallic interconnection system with aluminum wire bonding. However, for moderate current densities, the electromigration of aluminum becomes a concern at high temperatures.

Like thick-film technology, gold is also commonly used as conductor layer in thin-film technology. As gold does not adhere well to a typical ceramic substrate and dielectric materials, an adhesion layer, made of materials such as chrome, titanium, or titanium-tungsten, is always required. As a consequence, use of multilayer composite metal conductors leads to reliability concerns at elevated temperatures due to inter-diffusion problems. Diffusion of the adhesion layer through the barrier and the gold layer at elevated temperatures results in loss of adhesion and an increase in the electrical resistivity of the thin film, which is associated with impurity scattering.

1.3.2.3 Insulated metal substrate (IMS)

Insulated metal substrate consists of a metal base-plate covered by a thin dielectric layer and a copper conductor layer (about 20 – 200 µm thick). For the metal base-plate, aluminum is often used because of its high thermal conductivity, low density, good machineability, and low cost. The dielectric layer (about 50 – 100 µm thick) is mostly formed by a polyimide-based or epoxy-based polymer, which is inherently poor in thermal conductivity. Research is looking at replacing the polymeric dielectric layer with a thin glass ceramic layer to increase the overall thermal conductivity. However, the layer thickness, thermal conductivity, and dielectric strength of this layer are often a tradeoff.

Figure 1.10 is a schematic of a typical IMS. Because of the structure, the electrical components can only be mounted on the conducting (copper) side of the IMS, while there is no limitation of where the components can be mounted with thick-film technology, thin-film technology, and in the later-introduced direct bonded copper (DBC) substrate, as long as conductor traces are formed on both side of the substrate.

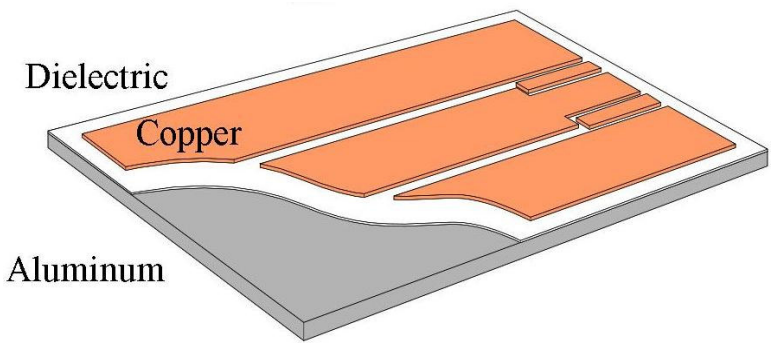


Figure 1.10. Schematic of IMS.

1.3.2.4 Direct bonded copper (DBC)

Direct bonded copper substrate has been widely used in power electronics industry since mid 1980's. Characteristic features of DBC substrate are thick solid copper conductors (0.15 – 0.65 mm) bond on both side of an alumina or aluminum nitride base-plate. At a range of about 10 – 15 ^{o}C below the copper melting temperature, copper and oxygen form a eutectic bonding between the copper layer and the alumina base-plate. In the same manner, two layers of copper can be fused together to increase the thickness of the conducting layer, and therefore increase the current carrying capacity of the substrate. Figure 1.11 [51] shows the DBC formation process.

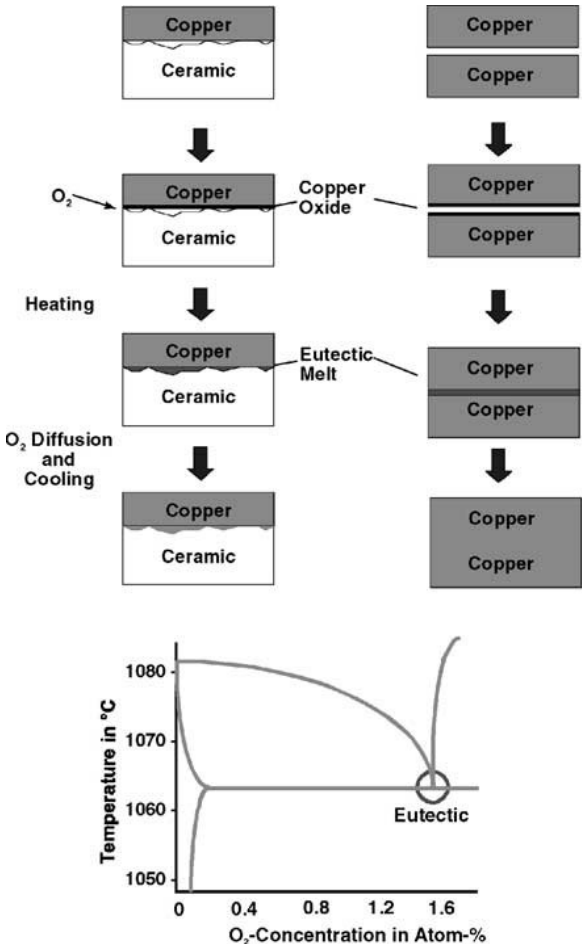


Figure 1.11. DBC forming process [51].

DBC probably is the most widely used substrate material in power electronics due to its high current-carrying capacity (about 100 amperes), high thermal and electrical conductivity, and controlled coefficient of thermal expansion (CTE) (6 – 8 ppm/K for alumina-based DBC and 4 - 5 ppm/K for aluminum nitride-based DBC), which matches well with that of semiconductor devices (2.3 - 4.7 ppm/K for Si, and 4.5 – 4.9 ppm/K for SiC). In addition, DBC is replacing complicated assemblies based on lead-frames and refractory metalized substrates due to ease of assembly. The DBC technology allows bonding of copper to alumina and aluminum nitride. The fusing of one copper layer to another has been developed to establish efficient water-cooling devices with sophisticated internal micro channel structures for cooling high-power laser diodes and other

high-power-density electronics [52]. DBC substrate also provides advantages in lower weight compared with many other heavy metal substrates, which is one of the most critical points in space applications. Figure 1.12 is a schematic of a typical DBC substrate, and Figure 1.13 [53] shows a typical power module based on DBC substrate.

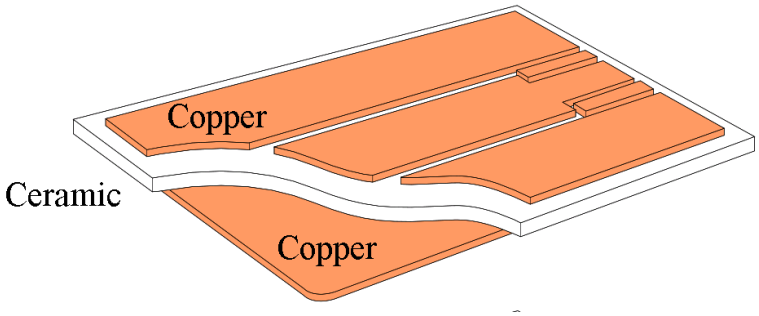


Figure 1.12. Schematic of DBC substrate.

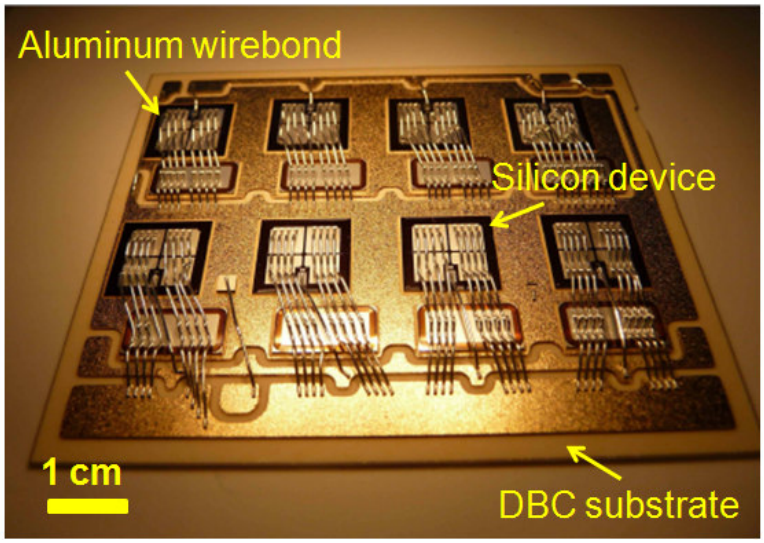


Figure 1.13. Traditional power module based on DBC [53].

A significant amount of work has been documented on the thermal performance or heat dissipation issues for DBC substrate. Hussein *et. al.* [54] have studied the effects of metallization thickness and the type of ceramic baseplate used in DBC substrate in terms of thermal management, and they found that the addition of copper metallization on Al_2O_3 improves its thermal dissipation characteristics. However, any metallization thickness on top of high

thermal conductivity substrates like AlN and BeO would deteriorate its performance. This indicates that minimal copper thickness is beneficial for these substrates. It has also been proposed [55] that a large reduction in temperature rise can be achieved from increasing the substrate's thermal conductivity by substituting AlN or BeO for the standard Al_2O_3. Adding a copper layer to Al_2O_3 reduces the thermal resistance almost as much as switching to bare AlN or BeO. While a metallization layer may reduce the temperature rise, it also increases the spacing required to minimize the thermal interaction. Hopkins *et. al.* [56] has compared DBC-Al_2O_3, DBC-AlN and DBC-BeO substrates by empirically measuring the equivalent thermal conductivities of these substrates, and they found that DBC-BeO has highest equivalent thermal conductivity followed by DBC-AlN and DBC-Al_2O_3, respectively. A substantial gain in overall equivalent conductivity is realized when copper is added to Al_2O_3 substrates. By comparing the electrical and thermal effects of copper conductor thickness on ceramics, it is also found that for DBC with AlN and BeO as baseplate, thermal conductance decreases upon a decrease in metallization thickness. However, for DBC with Al_2O_3 as baseplate, an optimum copper thickness of 305 μm has been suggested to maximize the conductance [57].

1.4. Motivation of developing sintering technique on DBA substrate

As introduced and discussed in the aforementioned sections, section 1.1 to 1.3, die-attach materials and substrate technologies are two of the most dominant issues in the manufacture of modern power electronics modules. The selection of die-attach materials and substrate technologies should be based not only on the basic properties they possess, such as electrical, mechanical and thermal properties, but should also emphasize the materials' manufacturability and long-term reliability. With regard to the manufacturability, the state-of-the-art die-attach material, solder alloys, and the state-of-the-art substrate technology,

DBC, both proved themselves as easy to adapt with excellent compatibility with other packaging technologies. However, when the targeted application temperature is raised from below 150 °C to 200 °C and above, both solder alloys and DBC substrate encounter big problems in reliability.

1.4.1. Materials for large-area attachment

The reliability of a system is the ability of that system to meet the required specifications for a given period of time. The reliability is measured in a number of ways, including the failure rate, expressed as a probability distribution function, and the mean time to failure (MTTF), which represents the length of time the system that is expected to operate until the first failure.

At the moment, maximum temperatures of about 125 °C are tolerable during typical operation of power electronic circuit boards. This limit is not set by the active elements made of silicon. Si-chips are theoretically able to operate as high as 200 °C, and the envisioned switch to silicon carbide would raise the bar to 500 °C [58-62]. However, today's interconnection materials are not suitable to reliably endure temperatures of 200 °C, let alone 500 °C. The state-of-the-art technology in attaching a semiconductor chip to a circuit board is soldering. The solder provides mechanical bonding and conduction of both current and heat. For decades industry used the eutectic alloy of tin and lead, Sn63Pb37 (T_M=183 °C). Due to worldwide regulations banning poisonous materials from electronic products, such as the Restriction on Hazardous Substances (RoHS) issued by the European Union, substitutes for lead-containing solders have to be found. Basic lead-free solder alloys are usually comprised of mostly tin (>96%), balanced with silver and copper. Their melting points are about 220 °C. As a rule of thumb, solder materials can be reliably used up to a homologous temperature T_h of 80% of their absolute melting temperature, before creep effects lead to quick degradation. Figure 1.14 [63] shows that SnAgCu solders are not suitable for

temperatures exceeding 125 °C. High-temperature solders, which can be operated continuously at 200 °C, do exist. However, they suffer disadvantages of either high price (AuSn, AuGe, AuSi) or poor processability (BiAg, ZnAl). Moreover, their operating temperatures are also limited by their melting temperatures, which make them unable to meet the operating capabilities of SiC-devices. Therefore, other means of interconnection have to be found.

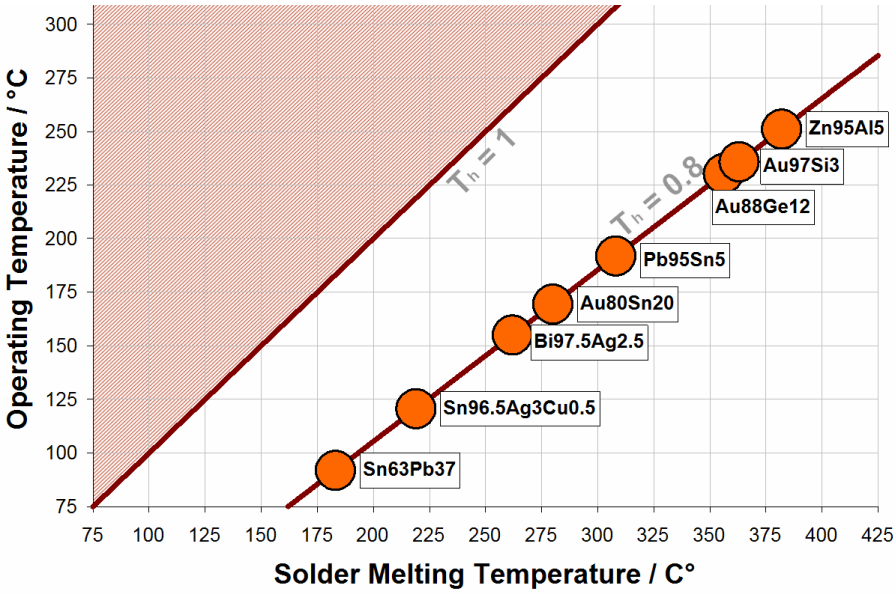


Figure 1.14. Maximum operating temperatures of solders versus their melting temperatures. Red area shows two phase region/liquid zone. Materials can only be reliably operated below the line *Th*=0.8 [63].

Another drawback that limits the use of solder alloys in many packaging applications is the fact that they cannot create a void-free interface, especially as the power devices are getting bigger and bigger. As explained in section 1.2.1, solders would form strong bonding with both the substrate and the device metallization by forming Sn-M intermetallics, where M can be Ag, Au, or Cu. The minimum requirement for the substrate and the device metallization is the cleanness. An oxidized metal surface would significantly degrade the bonding performance formed by solder alloys. Therefore, regardless of what forms of

solder are being used, whether it's solder paste or solder preform, flux is often used to clean the interface from metal oxide, and to further prevent them from oxidation during the reflow process.

However, flux is a mixed chemical that would burn-out at a relatively low temperature, normally 20 ^{o}C lower than the solder melting temperature [64,65]. During the cooling-down step of a solder reflow process, these flux in gas phase have to find paths to escape from the solder layer that is undergoing solidification process. Special attention should be paid to the design of the reflow profile to completely activate the flux so as to remove the surface oxidation, and to properly cool down the assembly to solidify the solder layer. Too fast a cooling rate would cause the flux gas to get trapped in the solder layer, resulting in a large area of voids in the attachment layer. Too slow a cooling rate would allow sufficient grain growth in the solder alloy, therefore lowering the inherent strength of the solder layer and also degrading the long-term reliability when subject to temperature cycling and temperature soaking tests. Figure 1.15 shows an X-ray image of a 10 mm x 10 mm bond line solder layer.

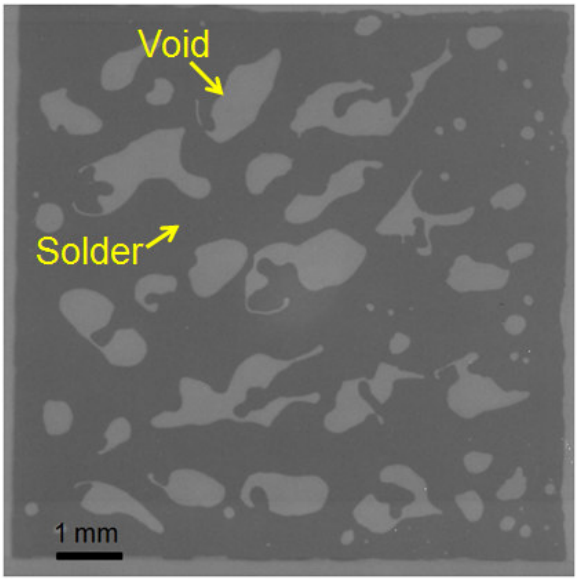


Figure 1.15. X-ray image of a 10mm x 10 mm solder bondline.

In the X-ray image, the darker region represents the good bonding area without voids, the lighter region represents the voids trapped in the solder layer. Notice that the gas formation during the solder reflow is a random process, the trapped voids are found randomly distributed under the device. For this specific sample, the void area is calculated to be close to 30%, which would greatly affect the performance of the attachment, from thermal, electrical and mechanical points of view. Although methods can be applied to reduce the void concentration in the reflow process, the added work and the extra steps would lower the convenience of using solder in manufacture.

1.4.2. Thermomechanical reliability of the substrate technology

Direct bonded copper is now in the dominant position as the state-of-the-art substrate technology in power electronics industry. In addition, its high current-carrying capacity, high thermal and electrical conductivity, and controlled coefficient of thermal expansion (CTE) mean it is unmatched by other technologies to an extent. However, DBC has its own liability. In to the manufacture process, the copper conduction layer is bonded to the base ceramic layer, Al_2O_3 or AlN, by a Cu-O eutectic bond. The bonding strength of this eutectic layer is so strong that the delamination of the copper layer from the base ceramic layer at the bonding interface is seldom observed, even after a long-term reliability test. However, the bottle-neck of the DBC structured substrate lies in the toughness of the base ceramic layer.

CTE mismatch between DBC copper conduction layer and base ceramic leads to thermomechanical constrains in the ceramic and copper layer. The mechanical characteristics of copper exhibit a yield stress of 70 MPa, and a high plastic strain rate [66], which cause the copper to have significant strain hardening behavior. Due to the strain hardening of copper, mechanical constraints increase in the ceramic material during temperature cycling. If the constraints in the

ceramic layer reach the rupture strength of the ceramic, a fracture would appear in the ceramic material. More details are explained and discussed in Chapter 3 which targets the thermomechanical reliability of the substrate material for high temperature electronics packaging.

1.5. Objectives and outline of this dissertation

A major challenge in today's high-temperature electronics packaging is the lack of reliable packaging materials with good performance, especially for the substrate and the die-attach materials. Since the chip-level packaging is the fundamental that connects the semiconductor devices' terminals to a substrate and provides signal and power communications among the devices, the overall performance of the packaging is highly dependent on the electrical, thermal, and mechanical characteristics of these packaging materials. Based on these motivations, the objectives of this study are to do the following:

1. Design and develop the process of using nanoscale silver paste for device attachment with good thermal and mechanical performance, which could be compatible with DBA substrate for high-temperature applications;
2. Study the thermomechanical reliability of DBA substrate under a large temperature cycling range, and investigate the behavior of aluminum under massive thermomechanical stress;
3. Evaluate the compatibility and reliability of low-temperature sintering of nanoscale silver paste on the DBA substrate under a large temperature cycling range. Not only will the reliability of sintered silver be investigated, but the influence of DBA characteristics on sintered silver layer will also be studied.

The significance of this study can be considered as following: (1) First of all, to develop a process of using nanoscale silver paste for device attachment to fill

the need for a die-attach material which could reliably offer good electrical, thermal, and mechanical performance during high-temperature operation. (2) Secondly, based on the results from the thermomechanical reliability test of DBA substrates and the observations from the microstructural evolution of aluminum, suggestions can be made in the manufacturing process to design the substrate material to have higher resistance to the mechanisms that cause the failure, and hence to prolong the lifetime of DBA substrates for high-temperature electronics packaging. (3) Combining DBA substrate and nanoscale silver paste gives a potential solution for high-temperature packaging applications. The effects of the substrate behavior on the die-attach material and the limitations of a sintered silver attachment can be identified.

Based on the aforementioned objectives, this study is divided into the following tasks:

Chapter 1 has provided an overview of current technologies of electronics packaging, including die-attachment, substrate materials, and metallization.

Chapter 2 details the development of low-temperature sintering of nanoscale silver paste for large-area device attachment. This chapter focuses on the design and development of the process of a low-temperature sintering of nanoscale silver paste for device attachment. Operating parameters such as temperature, time, pressure, and even the device size are taken into consideration in the design process, and their impacts on the characteristics of the sintered silver are also investigated. As explained in the study objective, the development of die-attach material enables the real use of substrate material for high-temperature application, and could be used to further evaluate the substrate impact on overall packaging performance.

Chapter 3 contains an evaluation of the thermomechanical reliability of DBA substrate. This chapter first presents the conventional failure mode of DBC

substrate during the thermomechanical reliability test. The observed delamination of copper from ceramic baseplate is ascribed to the stress generated at the copper-ceramic interface, due to the CTE mismatch between the copper and the ceramic layer. DBA is then explored in more detail, and a comparison is made with DBC substrate from a thermomechanical point of view. Accelerated temperature cycling test is performed to investigate the reliability of DBA substrate under a large temperature range. Some of the preliminary observations and characterizations are also reported in this chapter.

Chapter 4 studies the compatibility of sintering technology on the DBA substrate. The effect of substrate characteristics on the die-attachment shear-strength will be discussed. This chapter combines the results of the previous two chapters. Nanoscale silver paste is used as a die-attach material on the surface-treated DBA substrate. The mechanical strength and the reliability of the sintered silver are used to characterize the overall performance of the assembly.

Chapter 5 summarizes the entire study of high-temperature die-attach material and substrate technology.

Chapter 2. LOW-TEMPERATURE SINTERING OF NANOSCALE SILVER PASTE FOR LTJT

2.1. Low-temperature sintering of nanoscale silver paste

Nanoscale silver paste, a lead-free material consisting of silver nanoparticles mixed with organic binders and surfactants, can be sintered at 250 °C – 300 °C to form sufficiently strong bonding. Figure 2.1 shows a simplified schematic of making the silver paste. First, nanoscale silver particles, 50 – 100 nm, are mixed with short-chain surfactant to form a barrier coating layer around the particles to prevent coagulation and aggregation at low-temperature. Some long-chain polymers, used as binders, are then added to the mixture to form linkages among the individual particles, so that the mixture becomes a paste [67]. The mixture is thoroughly dispersed in solvent with ultrasound agitation to improve the paste uniformity. To make the paste more applicable in different applications, organic thinner is added into the mixture to adjust the paste viscosity. A uniform silver paste can be ready after adequately drying off the low-temperature solvent in air.

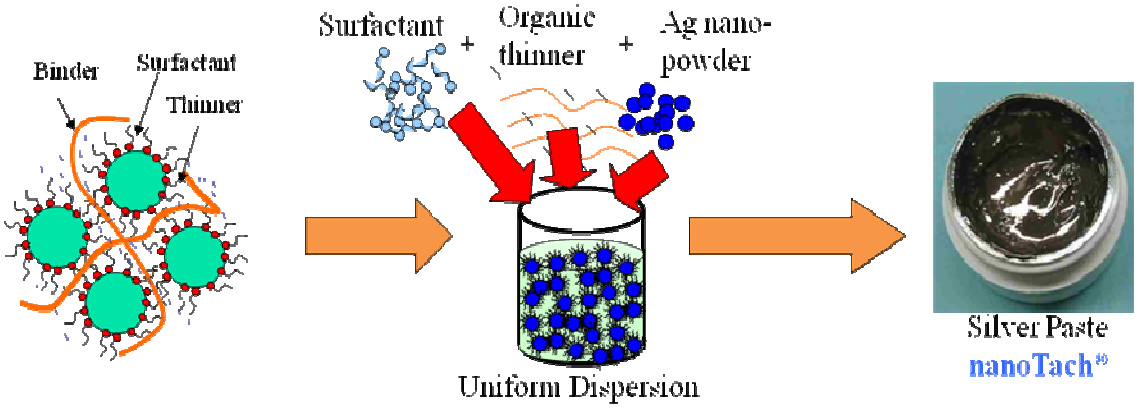


Figure 2.1. Process flow of making nanoscale silver paste.

Sintering of nanoscale silver paste utilizes the large thermodynamic driving force, so that the particles' densification rate can still be high at low temperatures.

Unlike reflow soldering, where the maximum operating temperature is limited by the alloy melting point, sintered silver joints are capable of operation beyond the processing temperature. The practical operating temperature range is limited by processes rather than the melting point. Properties of sintered silver layer are also superior to those of solder. Table 2.1 lists some of the measured properties of the sintered silver and other die-attach materials.

Table 2.1. Properties of die-attach materials.

Material	Processing temperature (^oC)	Use temperature (^oC)	Electrical conductivity 10^5 $(\Omega \cdot cm)^{-1}$	Thermal conductivity (W/cm·K)	Die-shear strength (MPa)
PbSn solder	217	< 183	0.69	0.51	35
SAC solder	260	< 225	0.75	0.70	35
AuSn solder	310	< 280	0.625	0.58	30 ~ 60
High-Pb solder	340	< 290	0.45	0.23	35
HYSOL glass	450	< 350	0.67	0.80	30
Silver epoxy	150	< 200	0.1	0.1	10 ~ 40
Nano-silver paste	**275**	**< 961**	**3.8**	**2.4**	**25 ~ 40**

In this study, the use of the nanomaterial is extended to attach large chips by introducing a low pressure up to 5 MPa. Scheuermann [68] and Schwarzbauer [69] explored sintering of silver pastes for joining power chips to substrate, and lower the sintering temperature of silver pastes below 300 ^oC, Scheuermann and Schwarzbauer and more recently others [67,70,71] applied quasi-hydrostatic pressure on the chip/substrate assembly to speed up the sintering kinetics of silver paste at low temperatures. With pressure of about 40 MPa or 400 kg-force on a 100 mm^2 chip, the silver die-attach layer underwent significant densification to density of 80% at 250 ^oC and had excellent thermal and electrical conductivities. The sintered silver joints were also reported [72] to be reliable. However, the need for such high pressure significantly limits production throughput, complicates manufacturing process, and places critical demands on substrate flatness, thickness of the chips, etc.

To minimize or eliminate the use of pressure for the low-temperature chip joining technique, nanoscale metal particles are used to lower the sintering temperature. This approach utilizes the large thermodynamic driving force for densification in place of the applied mechanical force. Based on the science of sintering, the driving force for densification of a particle compact would increase with decreasing particle size. Thus the densification rate, which is a product of thermodynamic driving forces and kinetics, of a nanoparticle compact can still be high at low temperatures despite of slow atomic diffusion kinetics at low temperatures. Measurements on the thermal and electrical properties showed five-fold improvement over solder and metal filled epoxy. Because of the porous structure, sintered silver possesses low elastic modulus of around 9 GPa, making the sintered joint very compliant and acting as a stress absorbing layer between the device and the substrate. In terms of bonding strength, sintered silver joint gives average die-shear strength close to 25 MPa, which is comparable to solders and metal filled epoxies. The sintered silver also exhibits excellent reliability in thermal-aging and thermal-cycling tests. No significant drop in die-shear strength was found from the thermal-aging tests at 300 ^{o}C for at least 400 hours. The sintered silver did not undergo significant microstructural evolution at this temperature because it is still substantially below the melting point. Excellent reliability and mechanical properties were obtained with the sintered joints, and they were demonstrated to support high-temperature operation of SiC devices with outstanding reliability [73,74].

In this study, nanoscale silver paste was used to make the attachment of large-area (> 100 mm^2) power semiconductor devices. With the increase in device size, solvent evaporation and binder burnout became much more difficult. Not only the heating profile needed to be modified, the whole attaching procedure had to be changed accordingly. In this chapter, the fundamentals of sintering were

firstly being introduced, followed by explaining the design of attaching procedure using nanoscale silver paste.

2.1.1. Fundamentals of sintering

Sintering is a heating process that causes particles to bond together, resulting in significant strengthening and improved thermal, electrical properties [75]. Sintering often refers to processes involved in the heating of powder compacts where mass-diffusion transport is appreciable. During the sintering process, the applied pressure accelerates mass transformation thus shortening the sintering time, improving the sintering microstructure. The sintered material usually has significantly improved thermal, electrical and mechanical properties than the initial powder system due to much denser structure. Sintering of powder compacts is an important process in the manufacture of conventional and advanced ceramic and metallic materials with various applications. There is no phase transition during the sintering process, and thus the bonding among particles is achieved only by solid-state diffusion. Sintering offers an opportunity to form a bonding below the melting temperature of interconnecting materials.

There are several dominant mass transfer mechanisms operative in the sintering of metal compacts [76,77]. At low temperatures, it is controlled by surface diffusion and results in neck formation between particles and/or significant grain growth, but little actual densification. At higher temperature, either grain boundary diffusion or lattice diffusion dominates the sintering process and leads to densification. If a non-densifying mechanism, such as surface diffusion, is allowed to proceed, it will consume the driving force needed for densification, making it difficult to achieve high density later in the sintering process. Nanoscale materials are particularly susceptible to this problem because they have very high surface area to volume ratio. The high surface area to volume ratio enhances the surface diffusion rate at very low temperature. The non-densifying diffusion may

round the particles, enlarge the particle size and/or even aggregate the particles. Figure 2.2 [78] depicts the diffusion paths during the sintering process.

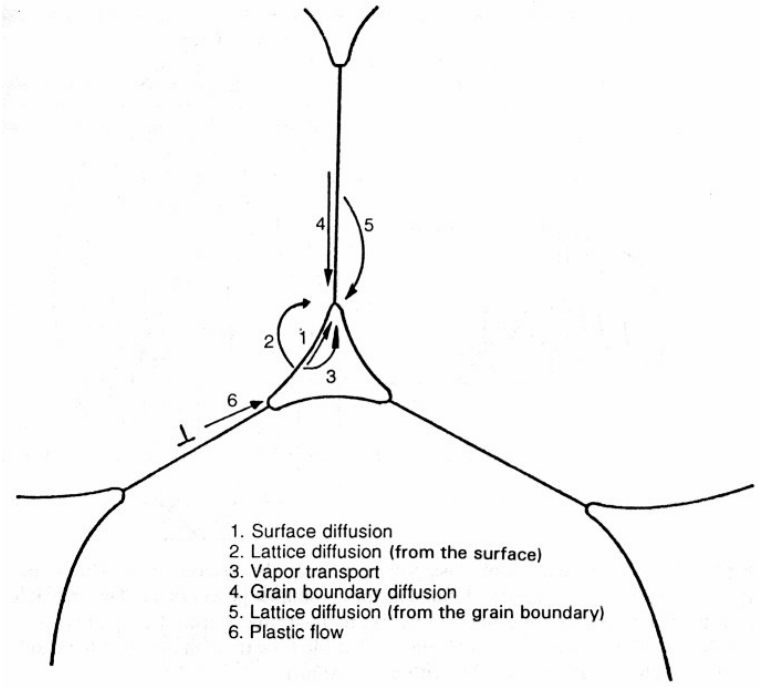


Figure 2.2. Matter transport paths. Note that only paths 4, 5, and 6 result in densification [78].

Table 2.2. The transport paths, sources and sinks of matter during sintering.

Transport Path	Source of Atoms	Sink of Atoms	Densification
1. Surface diffusion	Surface	Neck	No
2. Lattice diffusion	Surface	Neck	No
3. Vapor diffusion	Surface	Neck	No
4. Boundary diffusion	Grain boundary	Neck	Yes
5. Lattice diffusion	Grain boundary	Neck	Yes
6. Plastic flow	Dislocations	Neck	Yes

Table 2.2 shows the sources and the sinks of matter for each of these mechanisms. All these transports of matter can cause neck growing and thus consume the sintering driving force, but only three of them result in the densification of the powder compact. Therefore, in designing a complete sintering process, it is important to advance the diffusion(s) that would result in the

densification of metallic particles and in the mean time prevent the happening of the mechanisms that only form the necking among the particles.

2.1.2. Effect of applied pressure on sintering

During the sintering process, mass flows from regions of higher chemical potential to regions of lower chemical potential, and how it flows is determined by the transport mechanism. Therefore, from thermodynamic point of view, sintering is an irreversible process in which a free energy decrease is brought about by a decrease in surface area. In the solid-state sintering, the driving force for sintering is the excess surface energy of a powder compact which undergoes a sintering phenomenon and results in the reduction in the total interfacial energy.

When pressure is applied to the powder compact during the sintering process, this pressure is transmitted through particle-to-particle contacts and thus the local stress at the contact points between particles is significantly higher than the nominal pressure. For example, from Hertzian contact theory [79], the maximum stress, σ_0 is given by

$$\sigma_0 = \frac{3P}{2\pi a^2} \qquad 2.1$$

Where *P* is the applied load and *a* is the contact area between the two particles. Thus, the local stresses during pressure-assisted sintering are likely much larger than the yield strength of the metal, particularly during the early stages of compaction when the contact area between particles is small.

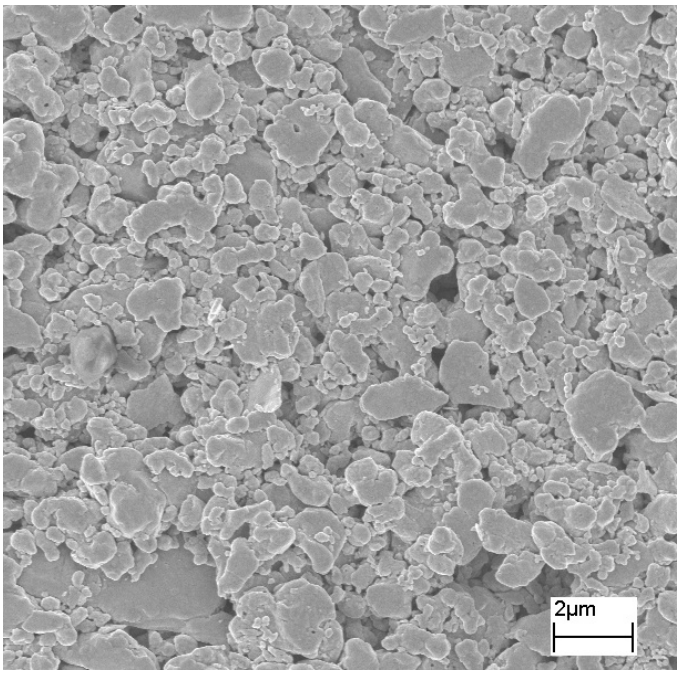
Coble's model [80] for pressure-enhanced densification has been used to explain the influence of pressure on densification kinetics. In that model, the densification rate, d*D*/d*t* is given by:

$$\frac{1}{D}\frac{dD}{dt} = \frac{15}{2}\left(\frac{D_{gb}\delta_{gb}\Omega}{G^3RT}\right)\left(P_a\phi + \frac{2\gamma_{SV}}{r}\right) \qquad 2.2$$

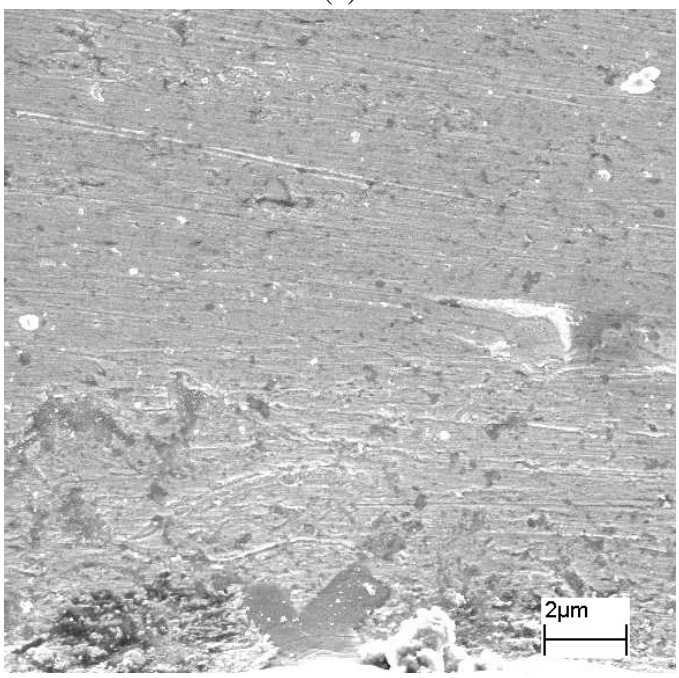
Where D_{gb} is the grain boundary diffusivity, $\delta_{gb}$is the effective width of the grain boundaries where grain boundary diffusion occurs, Ω is the atomic volume of Ag = 1.03 × 10^{-5} m^3 mol^{-1}, G is the grain size, R is the gas constant, T is temperature, P_a is the applied pressure, ϕ is the pressure multiplication factor acting at the particle contacts, γ_{SV} is the surface/vapor interfacial energy, and r is the pore radius.

In Zach Zhang's previous work on pressure-assisted low-temperature sintering of micro-scale silver paste for die-attach [67], it is demonstrated that when applying a quasi-hydrostatic pressure during the sintering process, the sintering temperature can significantly be lowered. With the assistance of a large external pressure (up to 40 MPa) the micron-size silver particles can be sintered at a temperature as low as 240 ^oC for a few minutes. The measured results show a significant improvement in electrical conductivity, thermal conductivity and mechanical strength of the attachments.

Figure 2.3 [81] shows the micro-scale silver paste sintered under different conditions: (a) at 250 ^oC without any externally applied pressure; (b) at 250 ^oC with an applied pressure of 10MPa during the sintering stage. SEM observations indicate that the applied pressure significantly assists the densification process even at a temperature as low as 250 ^oC. It is believed that the pressure helps the densification by (1) eliminating some fraction of pores through compression/deformation, and (2) increasing the contact area among the silver particles, therefore speeds up the free surface area reduction.



(a)



(b)

Figure 2.3. SEM images of micro-scale silver paste sintered at 250^{o}C (a) with no externally applied pressure, and (b) with 10 MPa pressure applied during the sintering stage [81].

In this study, the use of the nanoscale silver paste is extended to attach large chips by introducing a low pressure up to 5 MPa during the densification stage.

Attachment of large chips to substrates with silver, gold, and copper metallization was demonstrated. Analyses of the sintered joints by scanning acoustic imaging and electron microscopy showed that the attachment layer had a uniform microstructure with micron-sized porosity with the potential for high reliability under high temperature applications.

2.1.3. Effect of particle size on sintering

Although it is demonstrated that applying a pressure up to 40 MPa is able to lower the sintering temperature to 240 ^{o}C, the large externally applied pressure may cause problems as (1) increases manufacture difficulty, and (2) potentially damaging to semiconductor devices. Therefore, a strategy of replacing microscale silver particles with nanoscale silver particles was presented and studied.

From equation 2.2, it is clear that the densification rate of a particle compact is not only relying on the applied pressure, but also a dependent on the particle size. Therefore, besides applying large external pressure, reducing particle size to nanoscale is another approach to increase the sintering driving force. Thermodynamically, nanoscale materials have significantly higher driving force than microscale particles, which can compensate for the low mobility and drive the densification rate to a high level even at a low temperature. In Figure 2.4, the predicted densification rate is plotted against temperature for materials with a range of grain sizes from 5 to 500 nm.

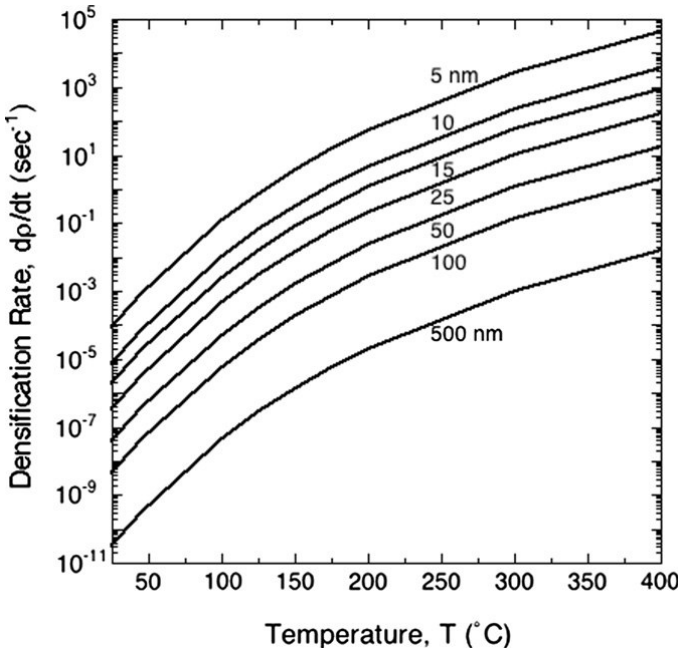


Figure 2.4. The effect of temperature on densification rate for Ag with different grain sizes at an initial density of 0.9 and a pressure of 500 MPa.

It is apparent that the predicted densification rate is strongly dependent on both temperature and grain size. For example, at a temperature of 100 ^{o}C, the predicted densification rate is increased by approximately seven orders of magnitude by decreasing the particle size from 500 nm to 5 nm. The predicted densification rate is increased by three orders of magnitude by increasing the temperature from room temperature to 100 ^{o}C and increased another two orders of magnitude upon increasing the temperature from 100 ^{o}C to 175 ^{o}C.

However, the fact that solid-state sintering depends on atomic diffusion leads to several challenges for low-temperature sintering, such as agglomeration, aggregation and non-densification diffusion. The agglomeration and aggregation in the initial powder systems result in the effective radius that is much larger than the real radius of particles and thus the low-temperature sinterability of nanoscale materials can be lost. The non-densification diffusion at relatively low-temperature consumes the driving force during the heat treatment processing and contributes little densification. Unfortunately, agglomeration, aggregation, and

non-densification diffusion can easily occur during the preparation, storage, and processing of nanoscale materials.

2.2. Experimental Procedure

2.2.1. Thermal characteristics of nanoscale silver paste

To help design an optimal time-temperature heating profile, thermal characteristics of the nanoscale silver paste were measured by thermogravimetric analysis (TGA) and differential scanning calorimetry (DSC). Figure 2.5 shows the equipment (NETZSCH STA 449) used to measure the TG and DSC characteristics of the nanoscale silver paste. The paste was heated in air from 25^{o}C to 600 ^{o}C at a rate of 5 K/min.

The TGA and DSC results were used to design a heating profile consisting of a drying segment to properly drive off most of the organic solvents and a ramp-up stage for sintering. Figure 2.6 demonstrates the position to place the testing samples in the chamber of the equipment.

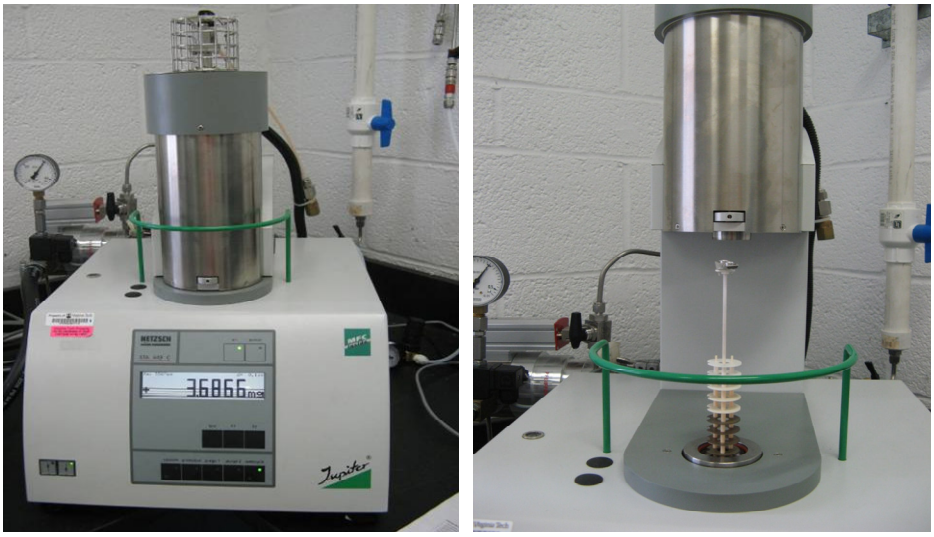


Figure 2.5. TGA & DSC measurement setup (NETZSCH STA 449).

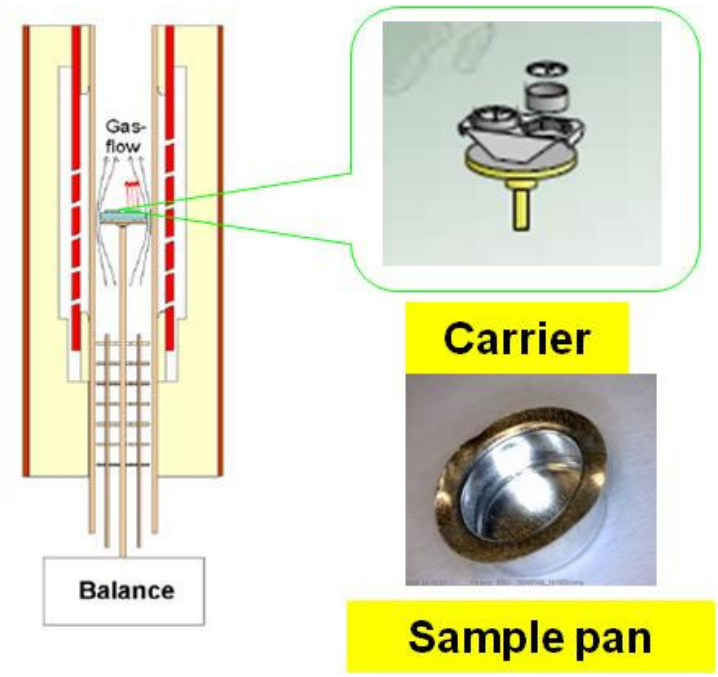


Figure 2.6. Schematic of sample location in NETZSCH STA 449.

2.2.2. Design of low-temperature sintering heating profile

The biggest challenge of large-area device attachment using a non-solder metal paste is to maintain sufficient device-paste and substrate-paste contact throughout the whole process to maximize strength and interface heat-dissipation path. For smaller device attachment, where the pathways for solvent evaporation and binder burnout are short, no additional drying of the paste is needed before mounting the device, and no external pressure is necessary in the sintering stage to obtain sufficient bond strength, e.g., 20 MPa. However, when the device size is larger than 5mm × 5mm, the solvent evaporation is not fast enough before the paste undergoes sintering, and the weight of the device itself is not enough to maintain interfacial contact during the eventual shrinkage of the paste layer due to evaporation and against the pressure caused by the binder burnout outgassing. A two-phase heating profile was therefore designed as a workaround for issues such as excessively long solvent evaporation time required, large shrinkage and

near-simultaneous binder burnout and densification. The heating profile was arrived at after considering the objective (low temperature), the need to keep the processing time reasonably short, bonding strength desired, and the experimental results. The combined TGA/DSC result was useful in determining the minimum temperature at which the binder can be burned off quickly. Earlier tests using transparent substrates of varying sizes (essentially glass or quartz covering the paste) showed drying to progress inward, which implied that increasing the device area would adversely affect the device attachment if the drying stage was not modified accordingly. A similar trend was observed for the binder burnout, with the center slightly lagging the outlying areas even after the peak temperature was reached. Finally, a cutoff time was made on the sintering stage after looking at the shear strength results. Figure 2.7 depicts the general methodology in designing the heating profile for sintering of silver paste. Notice that for different combinations of paste thickness, device size, and allowed pressure during sintering, heating profile can be adjusted accordingly.

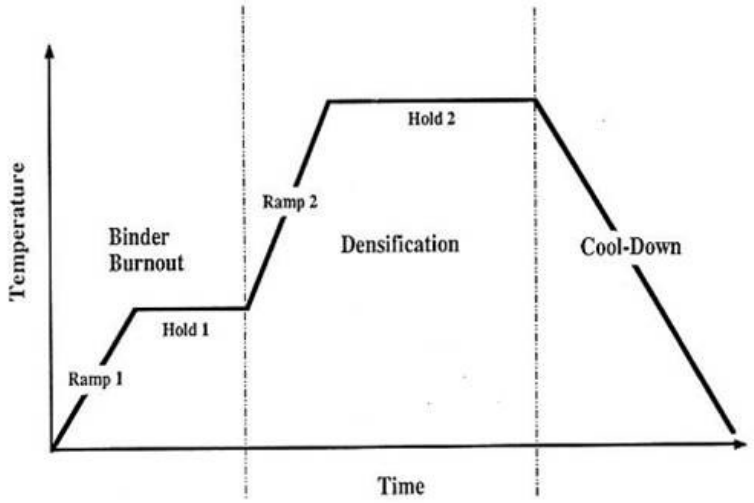


Figure 2.7. Schematic of heating profile for sintering of nanoscale silver paste.

To characterize the corresponding shrinkage profile of the paste arising from solvent and binder removal and densification of silver particles, an optical setup was employed, shown in Figure 2.8 [82].

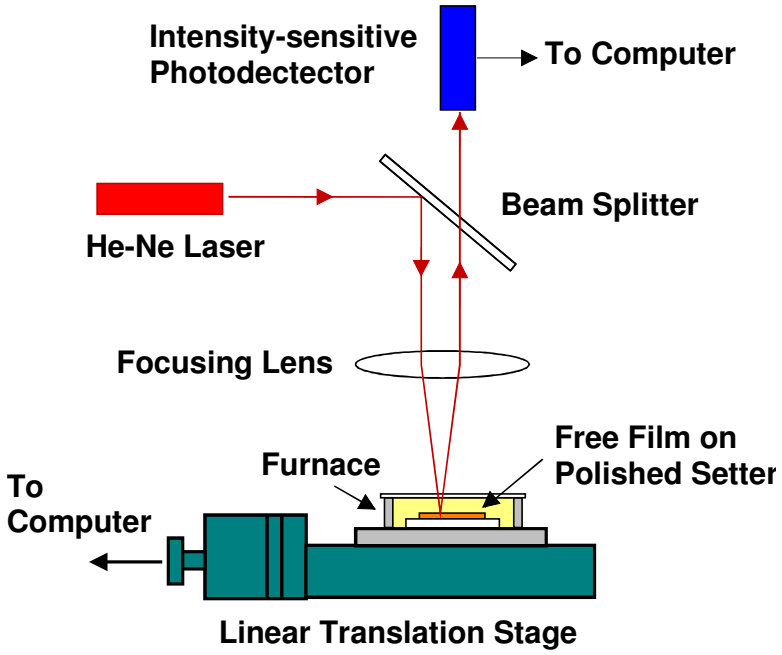


Figure 2.8. Schematic of Choe *et. al*. [10] optical setup used for measuring shrinkage profiles of constrained-sintering films [82].

A hot plate for better temperature uniformity and overall sample stability was used to replace the miniature high-temperature heater. Photo of the optical setup used to measure the thickness shrinkage profile of the paste films is shown in Figure 2.9.

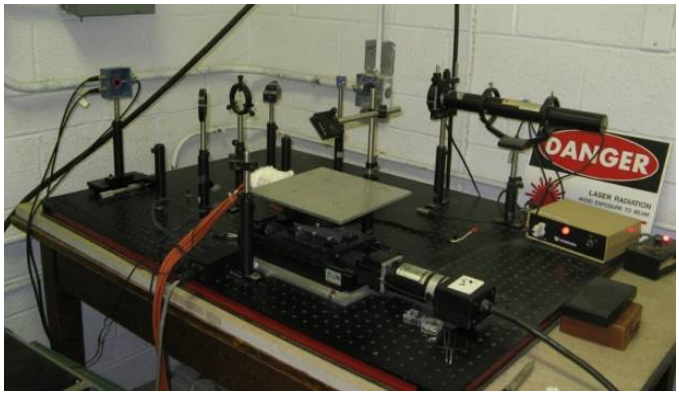


Figure 2.9. Photo of the optical setup for paste thickness shrinkage measurement.

To obtain a thickness shrinkage profile of the paste, the material was stencil-printed on a ceramic substrate to cover about half of its surface. A small piece of thin (about 250 µm thick) alumina was placed on top of the film. A piece of alumina (600 µm thick) was placed on the uncovered area of the substrate. A piece of silicon serving as mirror was then carefully bridged across the thick and thin alumina. As one end of the silicon dropped in height due to film shrinkage, the silicon would tilt and its tilt angle was monitored by reflecting a laser beam off the silicon surface onto a position-sensitive detector. The hot-plate temperature could be programmed to follow a certain heating profile and controlled to within ± 2 ℃ up to 450 ℃. As the silver sample shrinks in thickness because of solvent evaporation, binder burn-out, or densification, the silicon "mirror" would tilt and change the angle of the reflected laser beam. This angle change was recorded by a position-sensitive detector connected to a computer. Figure 2.10 shows the schematic of the optical setup for measuring the paste shrinkage profile.

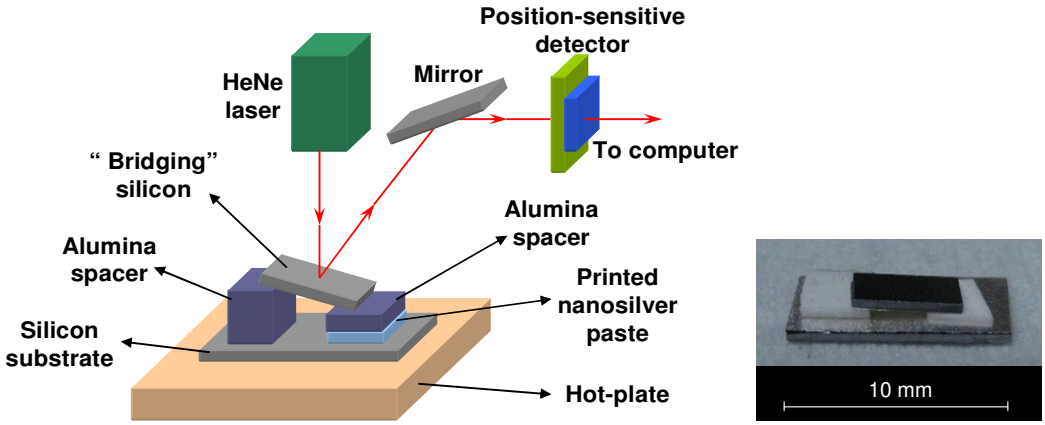


Figure 2.10. Schematic of the optical setup used for measuring shrinkage profiles of nanosilver paste samples placed in a cantilever assembly.

2.2.3. Development of bonding procedure of using nanoscale silver paste

As described in section 2.1, organic thinners were added into the silver paste to adjust the viscosity of the paste. Therefore, by changing the amount of thinner

as well as the solvent content, nanoscale silver paste can be applied to substrate by either printing or dispensing. Depending on the desired pattern size and the requirements on bondline thickness, printing and dispensing can be easily selected. Figure 2.11 shows the pictures of an automated dispensing machine.

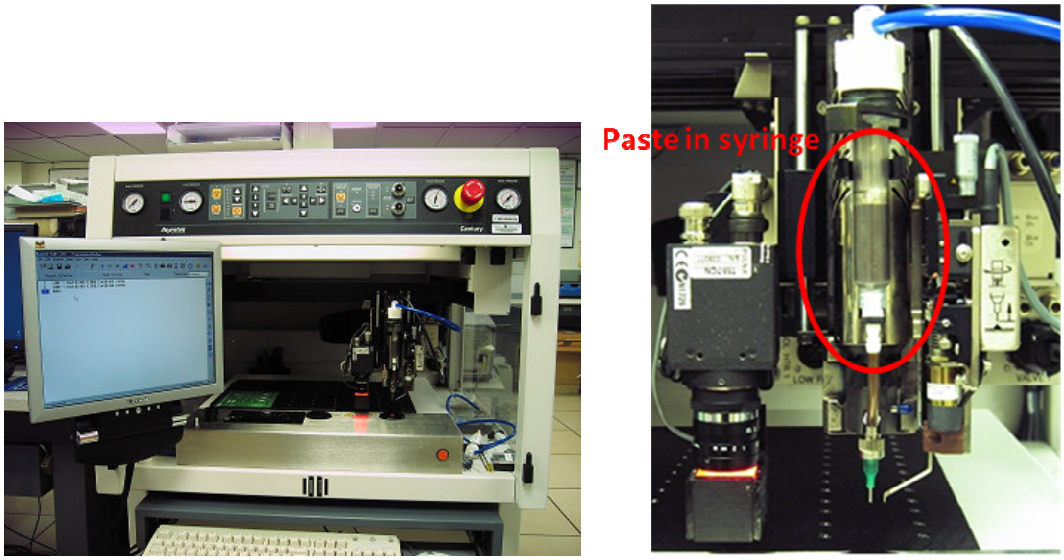


Figure 2.11. Automated dispensing machine.

Low viscosity silver paste was initially placed in a 10 cm^3 syringe. By adjusting the dispensing pressure and the dispensing pattern, paste can be easily applied onto any flat substrate. Figure 2.12 shows two dispensed pattern on Al_2O_3 ceramic plate.

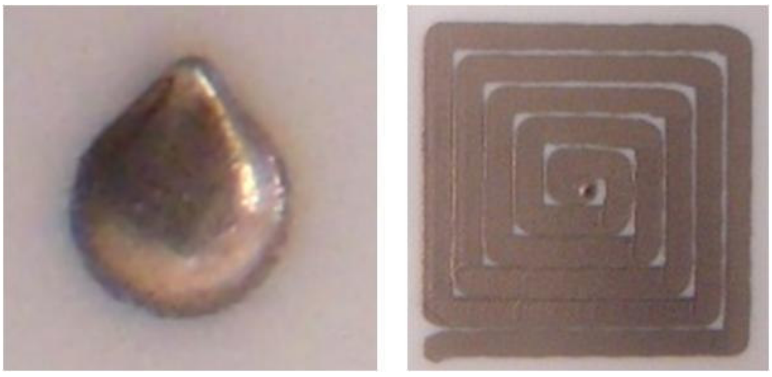


Figure 2.12. Dispensed silver paste patterns on Al_2O_3 plate.

Dispensing is very flexible in small device attachment. Once a dome pattern is formed on substrate, by placing the device on top of the dome and pressing the

device to a pre-determined thickness, an intimate device-paste interface can be easily formed. However, when used to attach large-area device, > 10 x 10 mm^2, it was found not convenient to apply the silver paste by dispensing method. Stencil printing, or screen printing, was recommended. For the stencil printing technique, a stainless steel stencil with certain thickness was firstly fabricated by either chemical etching or laser cutting to form the designed pattern. A squeegee, made by either aluminum or rubber, was used to print the silver paste so as to uniformly cover the stencil openings. Stencil printing and screen printing were very effective in forming complex printing patterns as well as large-area attachment. Figure 2.13 shows a stainless stencil with various patterns. In this study, since the objective was to design the process of attaching large-area device with nanoscale silver paste, stencil printing was used to make most of the samples. In addition, dispensing method was employed in making the small-area device (3 x 3 mm^2) attachment in characterizing the die-shear strength of the sintered silver.

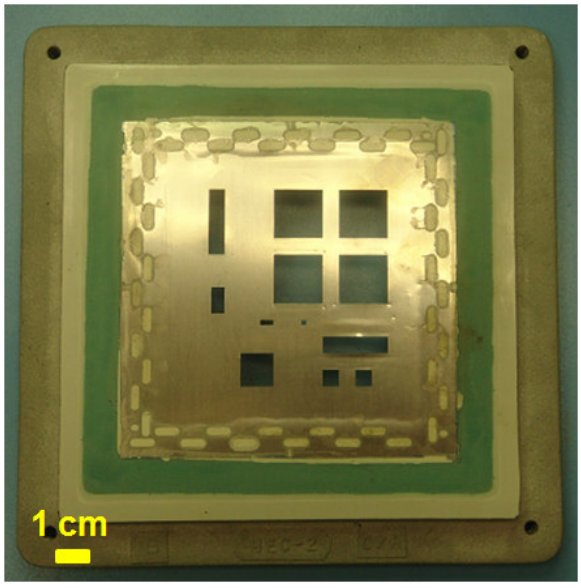


Figure 2.13. Stainless steel stencil for large-area device attachment.

2.2.3.1. Small (< 3×3 mm^2) device attachment

Small device (3 x 3 mm^2) attachments were fabricated for the purpose of characterizing the shearing strength of the sintered silver. As described in the

previous section, section 2.1, the sintering of silver paste involves the drying of solvent at low-temperature and the organic binder burnout at relatively high-temperature, the paste's thickness was found to be crucial in determining the sintering quality. Table 2.3 summaries some advantages and disadvantages of thick bondline and thin bondline. Notice that both the solvent dry out and binder burnout required evaporation path for gases to escape from the paste layer, a thick paste would induce much more tiny "cracks" than thin bondline. Therefore, it was observed that the attachment with thicker bondline usually had low bonding strength than the one with thinner bondline.

Table 2.3. Comparisons between thick bondline and thin bondline.

	Pros	Cons
Thin bondline	Less out-gassing, easier to form strong bonding	Less compliant, less reliable
Thick bondline	More thermomechanically stable	Cracking during sintering

Because of the importance of bondline thickness, a simple setup, shown in Figure 2.14, was made to determine the paste thickness during the assemble process. The setup contained three parts, including two parallel glass plates for plating samples, a micrometer for measuring the bondline thickness, and a spring-loaded steel bracket for applying adequate force. When making the attachment, the total thickness of device and substrate was initially measured by the micrometer. After zero the micrometer, rotated the tuner to a pre-determined thickness, e.g., 50 µm. Applied silver paste by either dispensing or printing on the substrate, and mounted the device on top of the paste. The assembly would be placed between two glass plates to make sure the paste under the device is uniform. Because the micrometer was back turned by 50 µm, which meant the bracket as well as the upper glass plate was raised by 50 µm. Therefore, once the assembly was pressed by the upper glass, the paste layer was easily determined to be 50 µm.

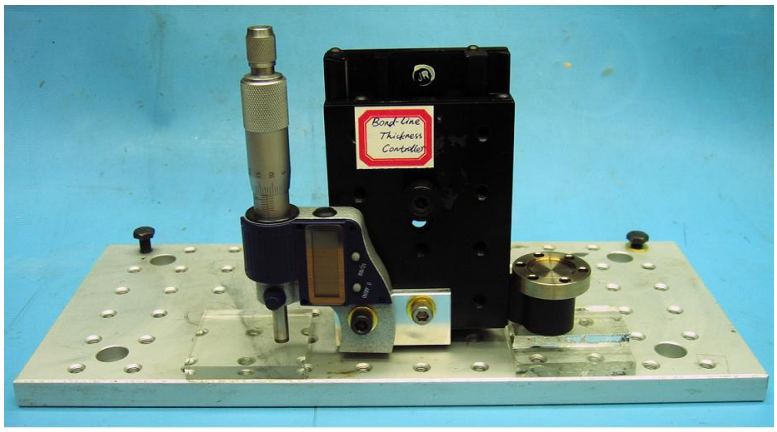


Figure 2.14. Home-made bondline thickness control setup.

2.2.3.2. Medium and large (>3×3 mm^2) device attachment

Because silver paste becomes very resistive when device area became sufficient large, it was neither practical nor accurate to use the thickness control setup to control the bondline thickness. Silver paste was mostly applied by stencil printing technique. The paste thickness was determined by the thickness of the stencil, although up to 10 μm variation can be found in most of the samples.

2.2.4. Attachment bonding strength measurement

Bonding strength is one of the most important properties of a die-attach material. Not only the post-process bonding strength is crucial, but also the changes of bonding strength with testing time is informative to understand the physical and chemical evolutions in the die-attach layer. In this study, shearing strength of the sintered silver joint was measured.

For small device attachment (3 x 3 mm^2), silicon or silicon carbide, or dummy devices made by high density Al_2O_3 were used. After applying the paste on the substrate and determined the paste's thickness, the assembly went through a designed heating profile to dry off low temperature solvent and burned out organic binder and eventually sinter the silver nanoparticles. A home-made setup was then used to measure the die-shear strength of these small attachments, shown

in Figure 2.15 and Figure 2.16. The main piece of this setup was a load-cell. Testing sample would be clamped on top of the load-cell. A shearing motion would be provided by a drill press, shown in Figure 2.15.

Figure 2.15. Setup to measure die-shear strength.

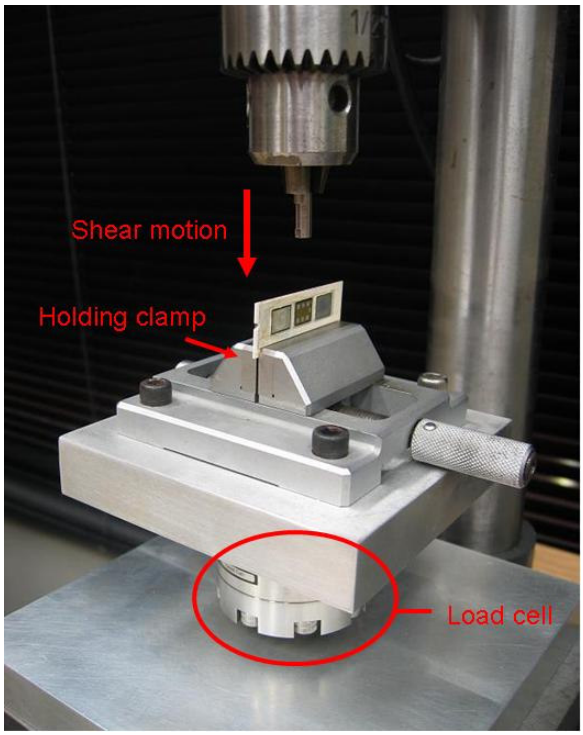


Figure 2.16. Shearing force measurement setup.

Once the load-cell measured forces from the drill press, it transformed the force into voltage signal and sent to a data acquisition box, which can be

monitored using a laptop. Figure 2.17 shows some measurement data after a series of pressing.

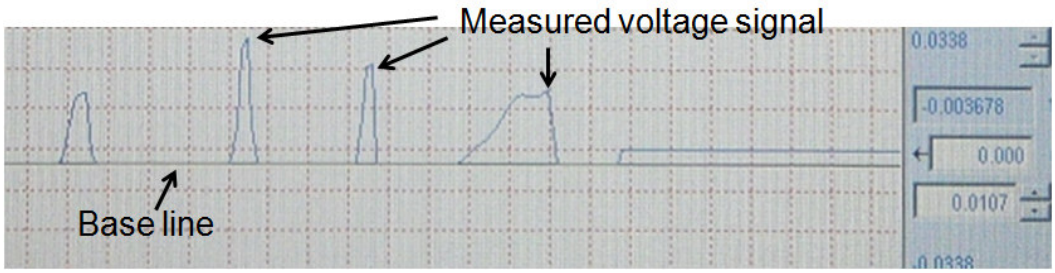


Figure 2.17. Samples of shearing strength measurement.

For large-area device attachment, because silicon chips were brittle and tended to crack during the shearing test, the die-shear strength was difficult to obtain. Therefore, a lap-shear test sample made up of copper plates joined together by the nanoscale silver paste was prepared. All the copper members were plated with nickel and then silver. The bonding area between two members was 10 × 10 mm^2 to duplicate the contact area of an actual device. The joining process followed the same time-temperature heating profile was used for the chip attachments. The shear strengths of the lap-shear samples were measured using a ComTen 95 series tester (ComTen Industries, Pinellas Park, FL) at a rate of 8 × 10^{-5} m/s. Figure 2.18 shows a schematic of the lap-shear sample and the test configuration. Flexible clamps were used to hold the specimen to avoid twisting the joint. Figure 2.19 shows the picture of the real setup.

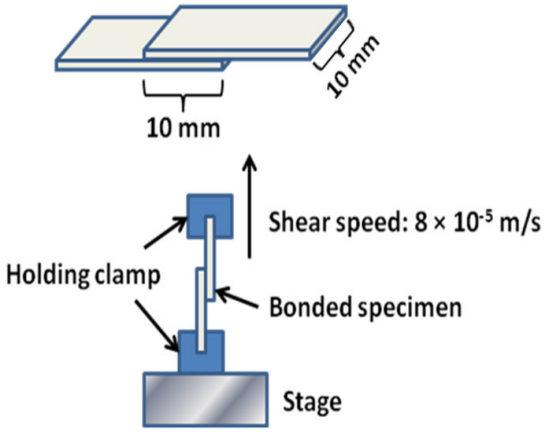


Figure 2.18. Schematic of the lap-shear specimen and the test configuration.

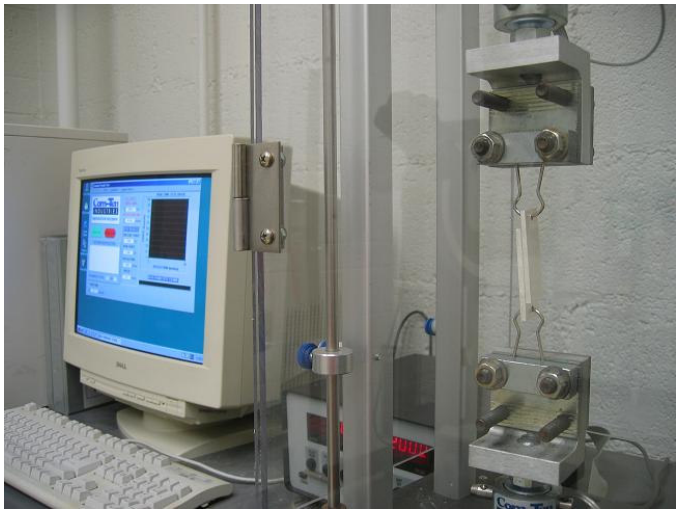


Figure 2.19. Photo of large-area lap-shear bonding strength measurement.

2.2.5. Accelerated thermo-mechanical reliability test

Electronic packaging is required to be highly reliable, especially in certain applications, such as automotive and aerospace industries. It is desirable to remove those units which are prone to infant mortality prior to releasing the remainder of the units to the field. This is usually accomplished by subjecting the circuits to some form of accelerated testing. Accelerated testing is designed to increase the failure rate of circuits by subjecting them to one or more extremes of temperature, humidity, bias, or mechanical stress. In this manner, units with inherent defects will fail earlier and may be removed from further processing. In this study, high-temperature aging and temperature cycling tests are selected to determine the reliability of the sintered silver joint.

2.2.5.1. High-temperature aging test

High-temperature aging test is effective in removing those failures which are caused by chemical reaction. These failures include intermetallic formation and corrosion. Equation 2.3 [83] shows that the rate of a chemical reaction approximately doubles every time the temperature is increased by 10 ^{o}C. Therefore, one hour at 125 ^{o}C is equivalent to 2^{10} hours, or 1024 hours, at 25 ^{o}C.

Many failures are further accelerated by the presence of bias or moisture. Elevated temperature in combination with an applied potential will accelerate inversion phenomena, particularly in the vicinity of device contact.

$$R_1/R_2=\exp(E_a/K)[(1/T_2)-(1/T_1)] \quad 2.3$$

Testing samples were made by attaching 3 x 3 mm^2 silicon devices to silver plated DBC substrate using sintering of nanoscale silver paste. Samples were then aged in an oven, shown in Figure 2.20, which held the temperature at 250 ^oC, for up to 1000 hours. Die-shear strength of the attached samples was measured after every 100 hours' aging. For each measurement, die-shear strength of at least 5 samples were measured and recorded.

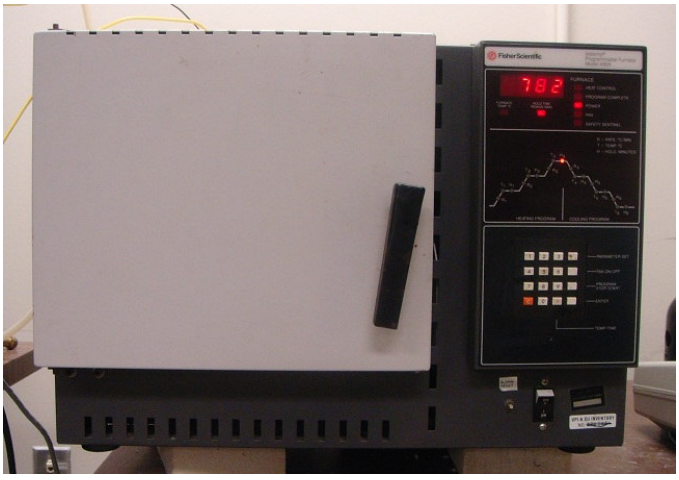


Figure 2.20. High-temperature oven used for aging test.

2.2.5.2. Temperature cycling test

Temperature cycling, or alternating the sample between hot and cold extremes at a predetermined rate, is an effective method for stressing wire bonds, solder joints, die bonds, and hermetic seals. The alternating hot and cold temperatures act to flex the junctions, promoting the propagation of microcracks or voids which occur as a result of intermetallic compound formation, mismatched CTEs, improper wire-bonding parameters, and similar phenomena. Temperature

cycling is becoming more prevalent, particularly in the automotive industry. At least two failure mechanisms are exhibited in this procedure that is reflective of actual performance conditions. As a circuit is cooled, any moisture present tends to condense on the surface of the hybrid. In ordinary temperature cycling with no bias, this would likely have no effect. In the presence of bias, however, the conditions exist for metal migration. The most stressful condition which a die bond, particularly a power die bond, can be subjected to is to have power applied at cold temperature. The resulting heat generated creates larger temperature gradients and higher stresses between the die and the substrate than exhibited under any other conditions. From observation, a significant percentage of circuit failures occur at the point when power is applied. Typical temperature-cycling schedules are 10 to 50 cycles for use as a screen, and up to 1000 cycles at the same extremes to simulate end of life. In this study, testing samples were temperature cycled between -40 ^{o}C and 150 ^{o}C in a Tenney® environmental chamber, shown in Figure 2.21. Figure 2.22 depicts the programmed temperature profile for the cycling test. Similar to the high-temperature aging test, die-shear strength was measured after every 100 cycles.

Figure 2.21. Tenney® environmental cycling chamber for temperature cycling test.

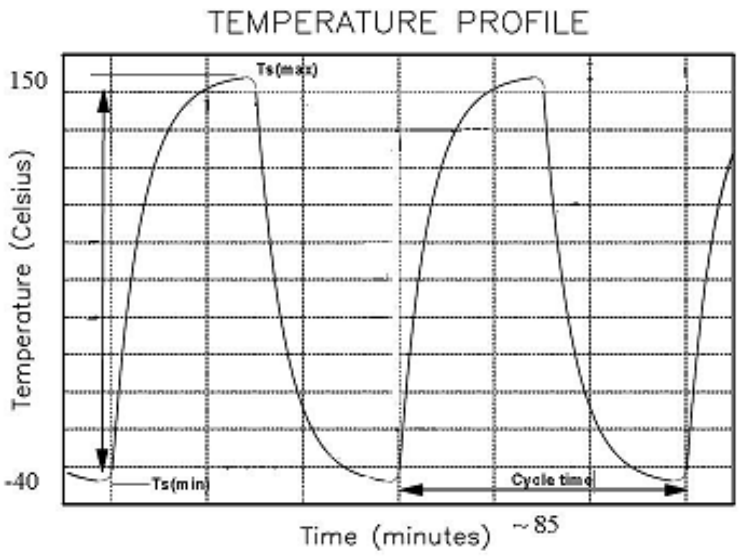


Figure 2.22. Temperature cycling profile for reliability test.

2.2.6. Characterization of the sintered silver bondline

2.2.6.1. X-ray inspection

X-ray is one of the emerging technologies for non-destructive testing and inspection of electronic packages, especially when packages are being encapsulated. Quality improvement can be made by accurately detecting flaws and defects such as solder voiding, bridging, solder ball alignment [84-86]. However, one of the shortcomings of X-ray inspection is that conventional X-ray cannot pass through dense materials such as copper and lead. Therefore in some cases of devices attached on thick copper substrate, X-ray is not very efficient to identify the flaws.

In this study, X-ray was employed to inspect the bondline conditions of large-area semiconductor devices attached to DBC/DBA substrate using sintered silver joint.

2.2.6.2. Scanning acoustic microscopy (SAM)

SAM is another non-destructive inspection method sensitive to defects beneath the surfaces of packages. SAM scan sends high-frequency (10 MHz to

200 MHz) ultrasound waves to the sample. The sound waves are reflected when encountering layers or interfaces with different acoustic impedance. Therefore, SAM is capable of detecting voids, cracks, and delaminations within packages. The percentage of voiding in large area attachment in power modules, for example, can be detected and calculated from SAM scanning [87,88].

In this study, together with X-ray, SAM was also employed in characterizing the bondline conditions of large-area device attached on DBC/DBA substrate using sintered silver joint. Similar to X-ray inspection, due to the porous structure of the sintered silver, SAM image cannot read as only black and white region.

2.2.6.3. Scanning electron microscopy (SEM)

SEM is a powerful tool in inspecting the microstructure of electronic components and material interfaces. Major steps include sectioning and cutting, mounting, planar grinding, polishing and etching.

Most samples need to be sectioned to the area of interest using abrasive cutting or diamond wafer cutting. The latter is a better approach to cut electronic components because it causes less damage to the samples. Next, a mounting operation protects the specimen edge and maintains the integrity of a material's surface features. This step is done by encapsulating specimen using mounting resins (acrylic resins, epoxy resins, and polyester resins). Depending on the encapsulation depth of the site of interest, a second sectioning may be needed. A subsequent planar grinding planarizes the sample cross-sections and exposes the exact area of interest. A sequentially decreasing grit/particle size of the silicon carbide abrasive paper is normally used. For electronic components that have multiple materials with various hardness, it is recommended that fine abrasives such as 800 or 1200 grit SiC be used after sectioning to prevent brittle devices such as silicon from cracking. A coarser grit abrasive might produce more damage to the specimen that sectioning. Hard ceramic substrates, such as

alumina, should be rough polished with diamond lapping films to minimize edge rounding. For SEM analysis, polishing of the specimen using diamond or alumina fine powder is usually required. The particle size starts from 5 μm, 1 μm, and can be as fine as 0.05 μm. Ultrasonic cleaning is recommended after every particle size polishing to thoroughly clean the surface because residual powder from last polishing step may contaminate the next level polishing mixtures and cause scratches on the sample surfaces. Figure 2.23 shows some polished samples.

Figure 2.23. Fine polished samples.

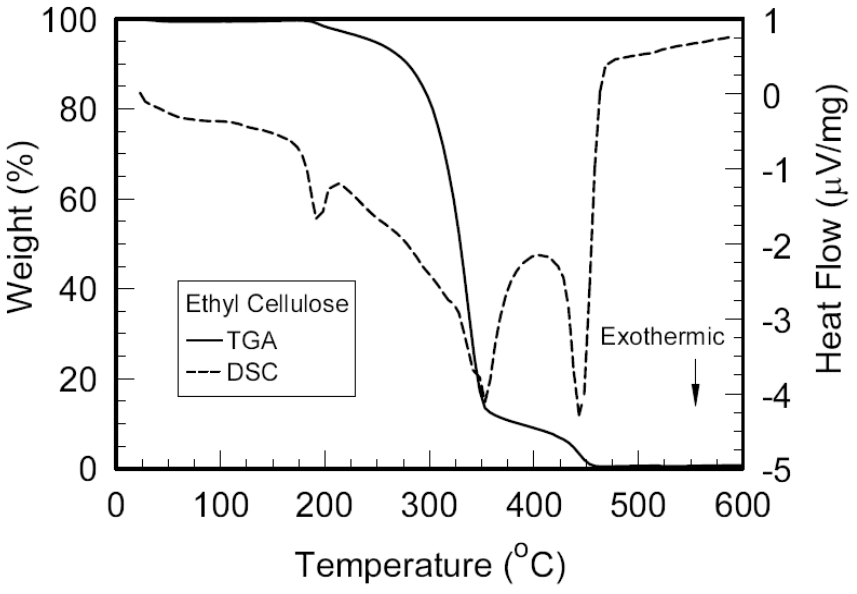
And at last, selective etching can be used to inspect the microstructural features such as grain boundaries and phases. The purpose of etching is to optically enhance these microstructural features. Etching selectively alters these microstructural features based on composition, stress, or crystal structure. The most common technique for etching is selective chemical etching and numerous formulations have been used over the years [89].

2.3. Experimental Results and Discussion

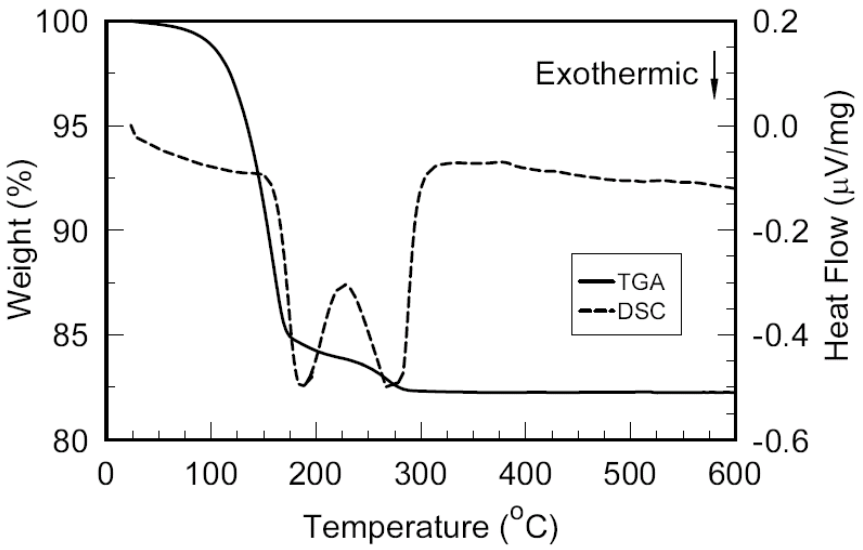
2.3.1. Thermal gravimetric analysis (TGA) result

To help design an optimal time-temperature heating profile, thermal characteristics of the nanoscale silver paste were measured by thermogravimetric analysis (TGA) and differential scanning calorimetry (DSC). Silver paste was

heated in air from 25 ^{o}C to 600 ^{o}C at a rate of 10 K/min. Figure 2.24(a) shows the TGA and DSC results. Weight loss started immediately upon heating because of evaporation of solvents in the paste. After much of the solvents evaporated, a further loss in weight came from an exothermic reaction in the paste with a peak at around 180 ^{o}C, as seen from the DSC curve. A second exothermic reaction, which also produced a weight loss, showed a peak at about 275 ^{o}C. Based on the TGA result, the silver content in the paste was approximately 82 weight % after the second exothermic reaction, at which stage all the organics appeared to have been removed as evident from the flat TGA trace beyond that point. The actual decomposition/burnout of the binder (ethyl cellulose) is significantly higher as shown in Figure 2.24(b), which at first glance would eliminate it as a suitable binder. However, the silver nanoparticles appeared to have a catalytic function that lowered the burnout temperature by as much as 170 ℃. This observation was based on the shift in position of the two biggest peaks in the DSC scan as well as the accompanying weight loss.



(a)



(b)

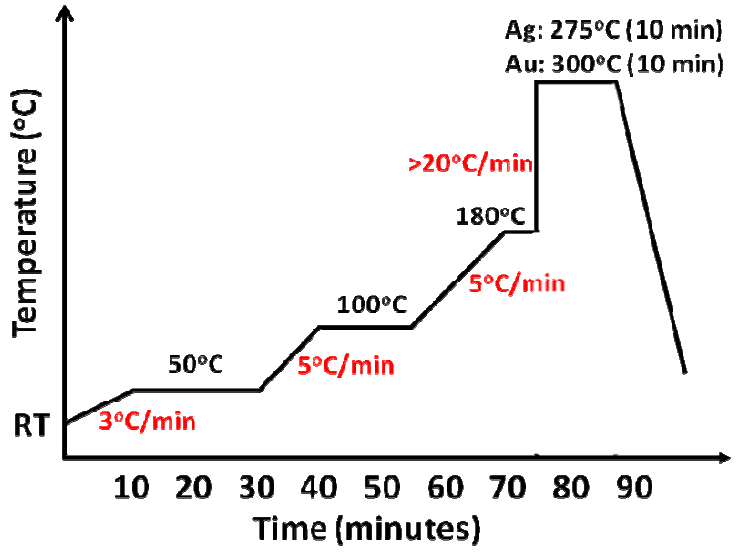
Figure 2.24. TGA and DSC traces of (a) the nanoscale silver paste heated in air at 10 K/min and (b) the ethyl cellulose binder.

Since these curves are dynamic scans, not obtain under steady state conditions, it is reasonable to assume that at longer heating times, it is possible to attain near-complete organics burnout at 275 ℃. The TGA and DSC results were then used as guides to design a heating profile consisting of a drying segment to properly drive off most of the organic solvents and a second stage for sintering.

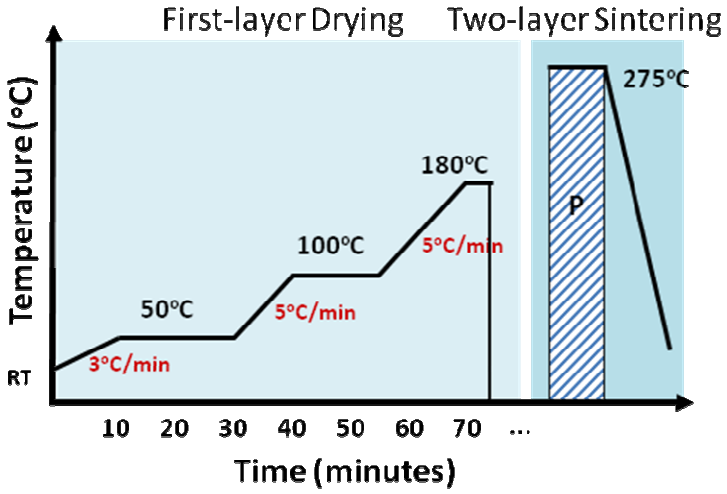
2.3.2. Heating profile for device attachment

Figure 2.25 shows the heating profile used to dry and sinter the nanoscale silver paste. The three drying steps at 50 °C, 100 °C, and 180 °C were designed to gradually remove the organic solvents in the paste to a high green density prior to sintering. A programmable hot-plate, shown in Figure 2.26, was used to control the heating rate as well as soaking time at each temperature step. For small device attachment, as the amount of gases to evaporate from the paste layer was not very significant, no externally applied pressure was needed during the sintering stage. Heating profile shown in Figure 2.25(a) was found effective to obtain a reasonably high bonding strength. Ideally the longer the drying process,

the less organics to burnout at higher temperature, and the better the bonding performance. However, it became not practical in manufacture if too much time was used in the drying stage. A total 70 minutes drying stage plus 10 minutes sintering at around 275 ^{o}C was therefore designed for small-device attachment.



(a)



(b)

Figure 2.25. Designed heating profile for sintering of nanoscale silver paste.

Figure 2.26. Programmable hot-plate.

For large-area device attachment, binder burnout became much more severe than small device attachment, a low pressure up to 5 MPa was found useful and effective in getting high bonding strength. Figure 2.25(b) shows the designed profile for large-area attachment. The initial drying process was basically the same as that of small area device attachment. However, if device area reached 10 x 10 mm^2, it was recommended to prolong the drying time, so as to dry off as much as organics in the paste layer before the sintering stage.

During sintering, a fast heating rate about 100 K/min is used to ramp up the temperature. This was based on observations [90,91] that rapid heating of a nanoparticle powder produces a denser material. The reason was to minimize the aggregation at lower temperatures of the nanoparticles prior to densification, which happened once the organic molecules separating the particles disappeared. Particle aggregation effectively reduced the densification rate because aggregated particles behaved as larger particles and possessed less driving force for sintering. Rapidly raising the temperature prevented the sintering particles from spending too much time at the low-temperature regime and thus avoided the aggregation process. The paste was sintered in a custom-built hot press so that an external

pressure could be applied. The simple hot press design consisted of a heating plate mounted on an off the shelf translation stage, shown in Figure 2.27.

Similar to the die-shear strength measurement setup, hardened steel was machined and polished to provide pressure. A force gauge was used to measure the peak force when pressing the sample. A temperature controller was setup to control the temperature, the heating rate, as well as the soaking time of the hot plate. Here, the purpose of the applied pressure was two-fold. Firstly, the pressure forced enhanced contact to the extent physically allowable between the chip and the paste given any surface roughness and curvature of the chip and substrate, and satisfied the need to counter the out-gassing pressure due to the burn-out of organics during the sintering stage. Secondly, the pressure helped in gaining a more uniform and denser sintered microstructure while at the same time compensating for the lower sintering temperature to some extent.

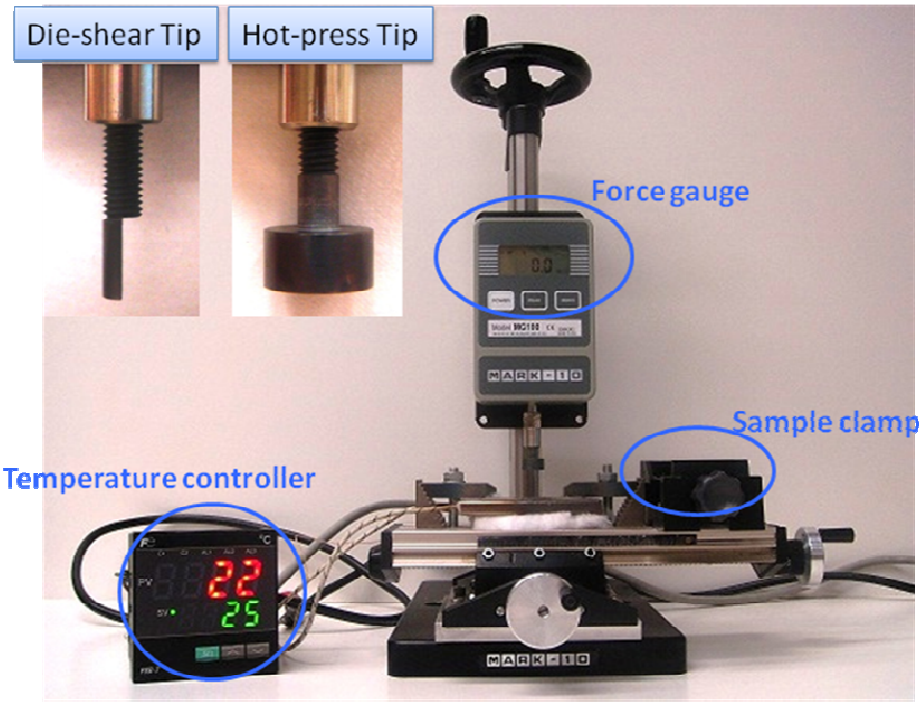


Figure 2.27. Hot-press setup for pressure assisted sintering of silver paste.

As for the soak time at the sintering temperature, a period of 20 minutes was used for chips greater than 100 mm^2; shorter times were needed for smaller chips.

The actual assembly/sample temperature was initially different from the designed profile when transitioning from the drying stage to the sintering stage due to the finite heat diffusion rate that resulted in a temperature gradient from the heater to the assembly.

2.3.3. Thickness shrinkage of nanoscale silver paste

Figure 2.28 shows thickness shrinkage profiles of the three covered paste samples in the sandwiched construction. A comparison between these and the TGA weight-loss resulted from the same set of samples pointed to a direct correlation: as the paste lost organic components by evaporation and combustion, the die-attach thickness would shrink. Like the slower weight-loss kinetics found in a larger chip assembly, the thickness shrank at slower rates with a bigger chip. The total thickness shrinkage in each of the three samples amounted to about 50%. A closer examination of the shrinkage profiles in Figure 2.28 showed that the thickness of the 5 mm x 5 mm sample actually increased when temperature ramp-up from 50 ℃ to 100 ℃.

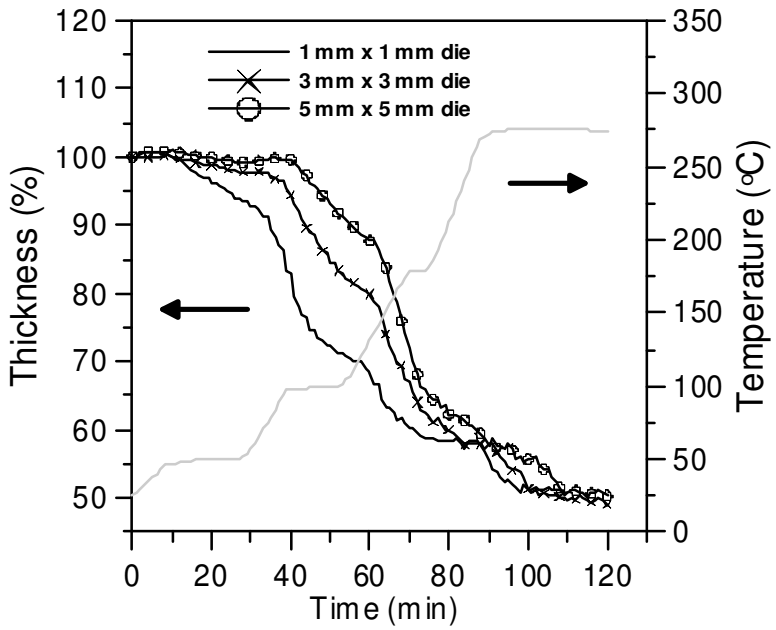


Figure 2.28. Thickness shrinkage results of 1 mm x 1 mm, 3 mm x 3 mm, and 5 mm x 5 mm die-attach samples measured *in situ* in the optical setup.

This was believed to be caused by a rapid build-up of vapor pressure of the solvent as it was escaping slowly underneath the large chip, thus leading to the chip pushed upward. Therefore, the use of pressure in the large-area device attachment was considered effective against this push-up effect.

2.3.4. Attachment bonding strength

Figure 2.29 shows representative pictures of devices attached on substrates. Silicon and silicon carbide devices ranging from 4 mm^2 to 16 mm^2 were used. Both had silver as backside metal for attachment. Four types of substrate were used: (1) alumina direct-bond-copper (DBC) electroplated with about 10 μm nickel and then 10 μm silver; (2) alumina DBC electroplated with about 10 μm nickel and then 1 μm gold; (3) Kovar™ metallized with a few micronmeters-thick gold; and (4) copper electroplated with 10 μm silver. To attach the devices, paste was firstly been printed onto a substrate using a stencil or a spacer to a thickness between 50 μm and 100 μm, and then pressed the devices, one at a time, on the wet silver print with a little wiggling/sliding motion to ensure good wetting on device backside. Here, too much pressing pressure (>400 kPa) should be avoided to prevent squeezing out the paste and burying or shorting the device.

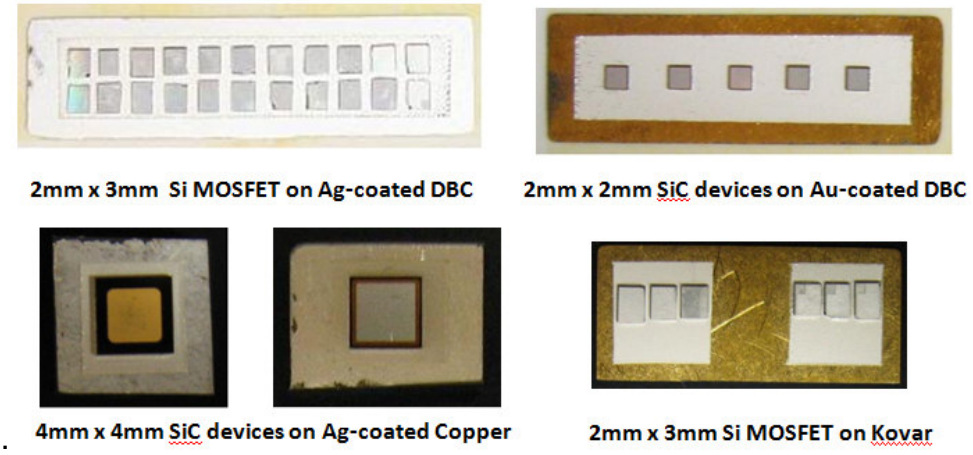


Figure 2.29. Examples of small device attachment.

Figure 2.30 shows the typical values obtained on the die-shear strengths from Ag- and Au-coated substrate surfaces. The die-shear strength was affected by the sintering temperature, sintering time, device and substrate metallization, and applied pressure. A high sintering temperature enhanced the densification leading to stronger bonds. The metallization on the surfaces to be joined played a role because it partly determined whether the failure during shearing was by adhesive failure (at the interfaces), cohesive failure (within the die-attach layer) or both. In both cases, the die-shear strengths were generally greater than 20 MPa and averaged at around 25 MPa, which was comparable to the published die-shear strengths obtained in our earlier work and those found in soldered and epoxy.

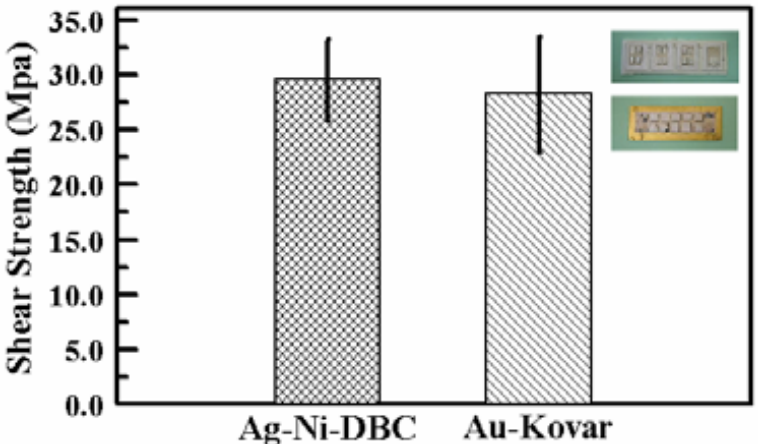


Figure 2.30. Measurements of die-shear strengths on devices mounted on Ag- and Au-coated substrates.

To make large-area chip attachments, the nanoscale silver paste was stencil-printed onto a substrate to a thickness of 50 to 100 μm and dried according to the profile in Figure 2.25(b). After cooling down from 180 ^{o}C, a thin fresh paste layer of 5 to 10 μm was printed onto the dried film. This second layer acted as a wetting layer between the dried paste and the chips. To ensure good wetting, a slight wiggling/sliding motion was placed on the chips as they were mounted. Then, the attached assemblies were sintered in the hot press with the heating

plate set at 275 ^{o}C and the pressure adjusted to a specified value between 0 and 5 MPa.

Figure 2.31 shows some representative pictures of large-area chips attached on substrates. Silicon chips ranging from 4.4 × 4.4 mm^2 to 13.6 × 13.6 mm^2 were mounted onto four types of substrates: (1) alumina direct-bond-copper (DBC) electroplated with 5 to 10 μm nickel followed by a final 5 to 10 μm silver layer; (2) gold plated Kovar™ substrate; (3) copper plate electroplated with 5 to 10 μm silver; and (4) bare copper plate. Chip thickness varied from 0.3 to 0.5 mm.

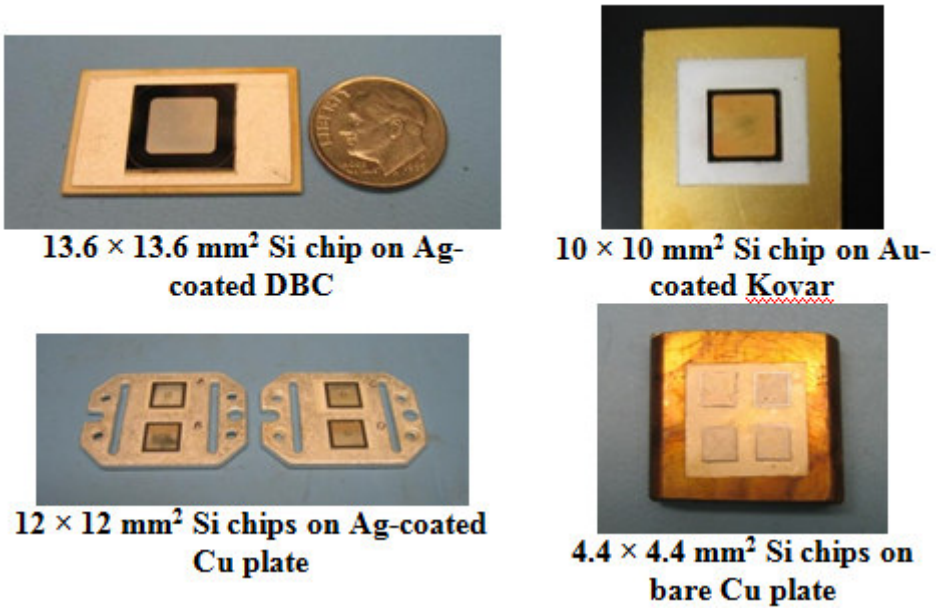


Figure 2.31. Examples of attached Si chips on four types of substrates using the nanoscale silver paste and the sintering process.

Since the sintering process required oxygen for organics burn-out, the surface metallization of the substrate and chips was preferably silver or gold to prevent oxidation. However, it was still possible to bond chips to bare copper surface as shown in Figure 2.31 by reducing the oxygen partial pressure in the air to a level that was low enough to prevent significant oxidation in copper but high enough for organic burn-out.

As introduced in section 2.2.4, to measure the bonding strength of large-area attachment, lap-shear copper samples were fabricated. Figure 2.32 shows a

lap-shear sample.

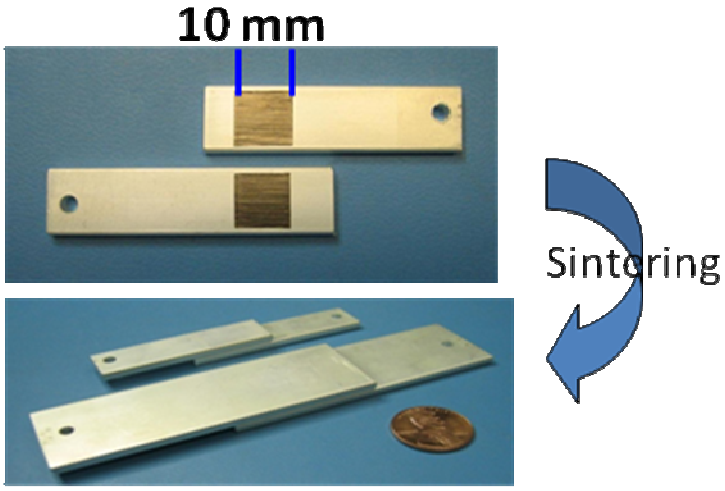


Figure 2.32. Lap-shear sample for large-area bonding strength measurement.

Figure 2.33 shows a typical load vs. displacement plot obtained on a lap-shear sample sintered at 5 MPa. From the maximum load at which the sample broke, the bonding strength was calculated to be 29.1 MPa. The large displacement obtained in the test was the result of flexible clamps used in holding the sample and was accounted for in the analysis.

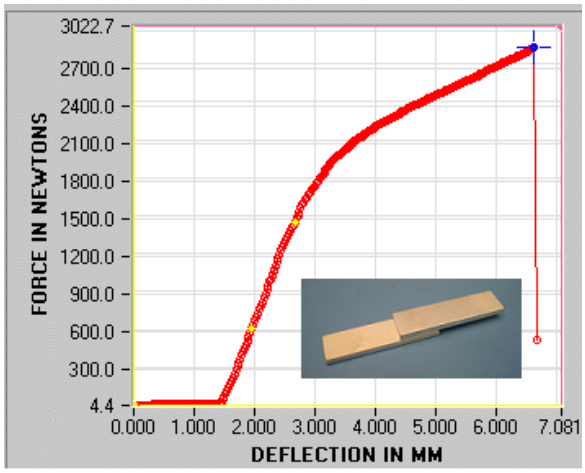


Figure 2.33. Load-displacement trace from a lap-shear sample sintered at 5 MPa.

Figure 2.34 is a plot of the shear strengths of the Cu-to-Cu lap-shear samples bonded with the nanoscale silver paste with applied pressure ranging from 0 MPa

to 5 MPa. Five samples were made for each pressure level. The average strengths were 7.7, 15.3, 21.3, and 31.6 MPa for pressures of 0, 1, 3, and 5 MPa, respectively.

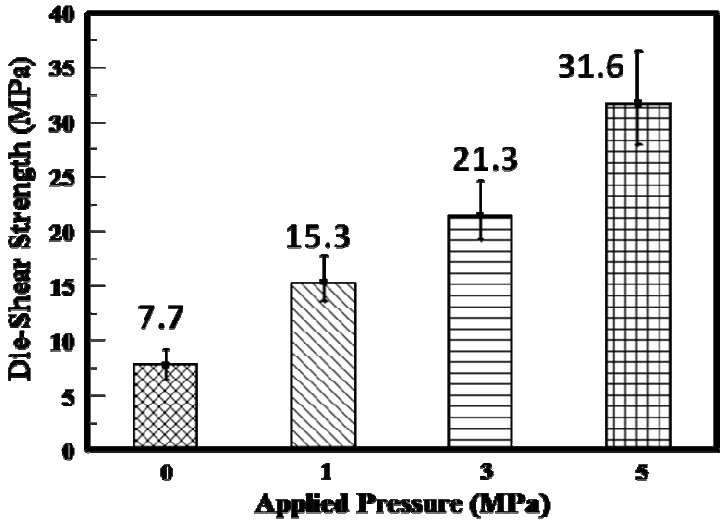


Figure 2.34. The shear strengths of Cu-to-Cu lap-shear samples prepared at four different pressures.

The changes in bondline thickness were also measured when pressure was applied. Table 2.4 lists the average bondline thickness measured from the samples with different applied pressure during the sintering stage. It is clear that when the applied pressure increased, the bondline thickness decreased slightly, which corresponded to more dense structure after sintering, and therefore possessed stronger inherent strength.

Table 2.4. Bondline thickness of samples with different applied pressure.

Applied Pressure (MPa)	0	1	3	5
Bondline Thickness (μm)	36.87	36.57	34.98	33.66

Another qualitative evaluation of bonding strength of large chips on DBC substrate involved breaking the attached substrate over an edge. If chip cracks along with the DBC substrate without being delaminated, the bonding strength

was said to be strong. Figure 2.35 shows a cracked large chip-to-DBC attachment demonstrating strong bonding strength of the sintered joint.

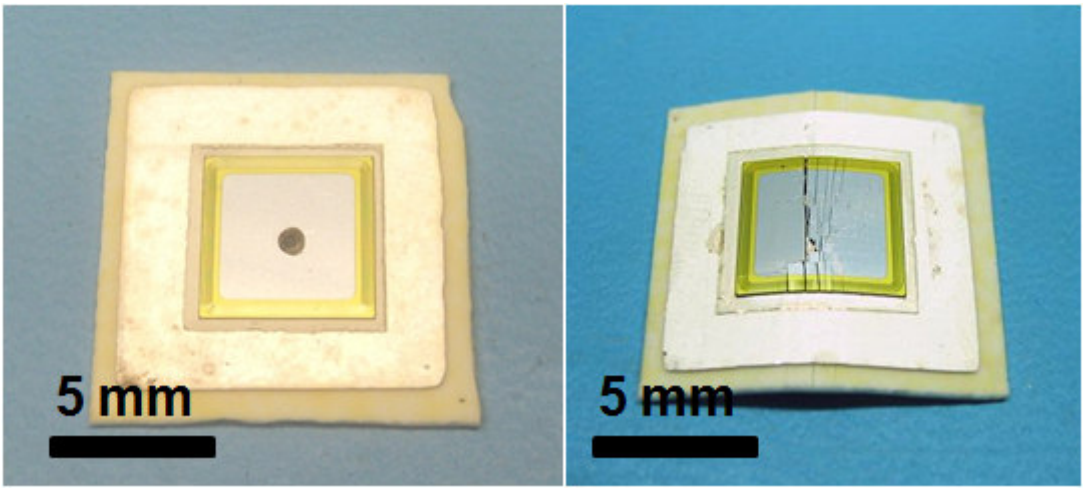


Figure 2.35. Demonstration of strong bonding of a large chip sinter-joined on a DBC substrate.

2.3.5. Thermo-mechanical reliability of the sintered silver

The resistance of the sintered silver die attachment under temperature cycling was also investigated. The cycling temperature range was set from -40 ℃ to 150 ℃, which was cited as a typical on-engine temperature range in an automotive environment. The results for both types of substrate were shown in Figure 2.36 and Figure 2.37. The cycling test was cut off at 600 cycles for samples on the alumina DBC and 800 cycles for those on Kovar because there were not enough samples of each to continue. Additional samples were fabricated to extend the cycling test. In both cases, the die-shear strength of the joints gradually declined. In the case of the die attachments on the alumina DBC, the shear strength declined by about a third of the initial strength. On the other hand, the shear strength of samples on the Kovar™ substrates declined by only around 25% and appears to have stabilized. The slower deterioration might due to the smaller CTE mismatch with the Kovar™ substrate (5 ppm/℃). If a 50% drop in die-shear strength was considered as the failure point, then the joints should be reliable past the 1000-cycle mark. At any rate, the results showed that the

sintered silver was resilient enough to withstand the temperature range to which it was subjected. An even higher temperature range was planned for future testing.

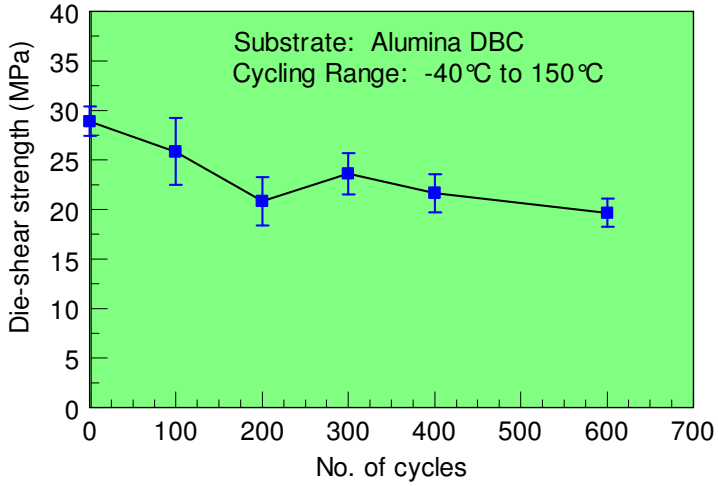


Figure 2.36. Results of temperature cycling of mechancial devices mounted on Ag-coated alumina DBC.

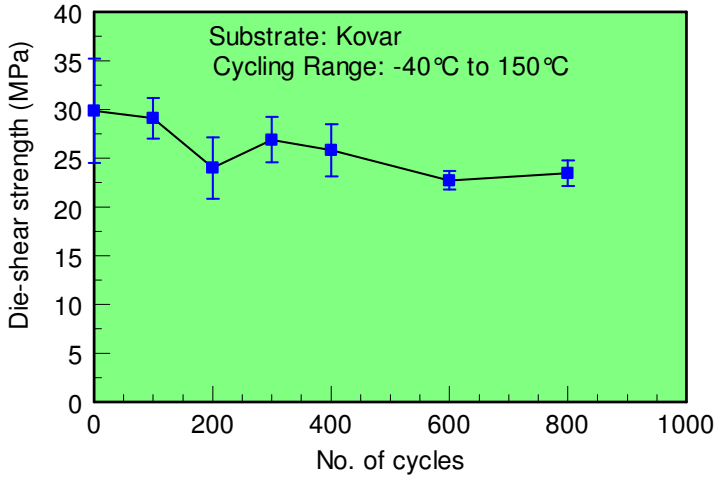


Figure 2.37. Results of temperature cycling of mechanical devices mounted on Au-coated Kovar™ substrates.

Figure 2.38 is a plot of die-shear strength versus aging time from devices attached on Ag-coated DBC substrates that were heated at 300 ^{o}C in an oven. Taking into consideration the scatter in die-shear strengths, it was believed that the aging had no significant effect on the joint strength. In recent studies on using lead-free solder for die-attach [92-95], the authors reported a drastic decrease in

bonding strength after aging. The decrease was attributed to microstructural changes in the solder alloy at the aging temperature. In our case, since the aging temperature of 300 ^{o}C was much lower than the 961 ^{o}C, melting point of silver, and the sintering process had spent much of the surface/interfacial free energies, it was not expected that the sintered microstructure would undergo significant microstructural evolution. The sintered microstructure was likely to densify a little further at the aging temperature. This would strengthen the joint by increasing the cohesion of the attachment as well as adhesion between the attachment and its adherents (i.e. device and substrate).

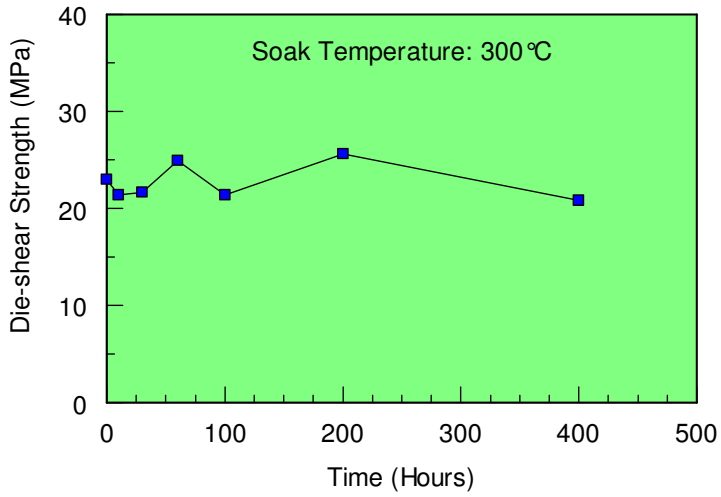
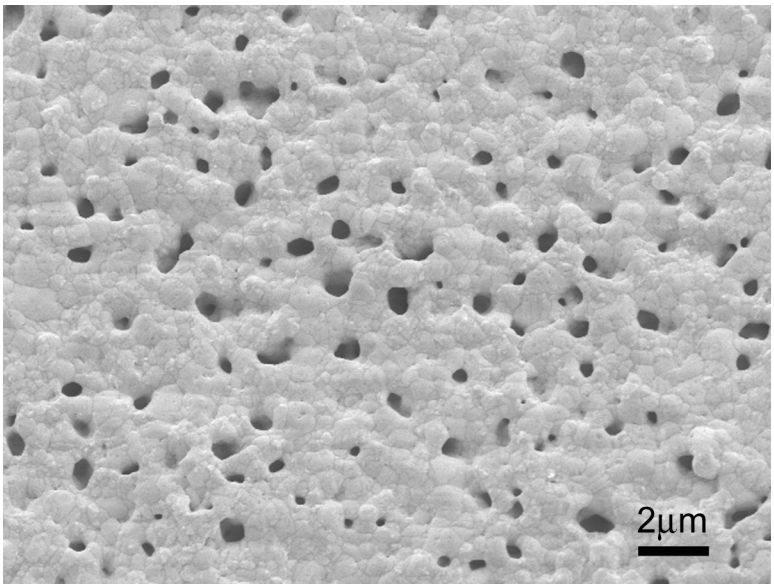


Figure 2.38. Results of die-shear strength vs. dwell time from an aging test at 300^{o}C.

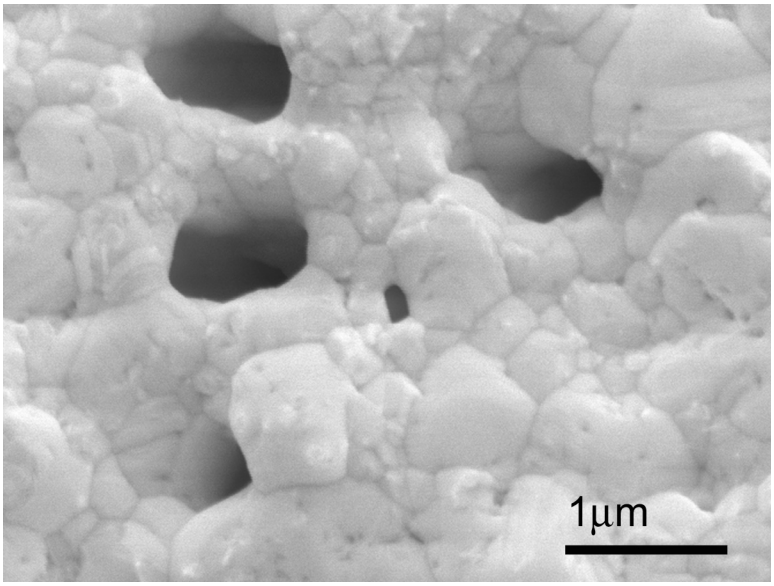
2.3.6. Characterization of attachment bondline

Figure 2.39 shows the microstructure of the sintered silver joint. The starting average size of the silver particles in the paste was less than 100 nm. During sintering, the pores were diminished through atomic diffusion, the extent of which depends on factors such as green microstructure, temperature, and time constraint. Particles either grew by feeding on the adjacent particles or were consumed by neighboring particles. Because the sintering temperature was very low and the paste was at the peak temperature for a relatively short time, and due

to the constraint from the adherent surfaces, the pores were not expected to disappear completely. The pores were in the sub-micrometer to low micrometer range. The relative density of the sintered silver was around 80% as measured by the volume displacement method although the surface structure seems to indicate a higher figure because it was smoothed out by sintering. The effect of surface constraint still existed and the previous work on constrained sintering of metal paste films also showed a significant retardation of the sintering kinetics leading to a more porous structure. The porous structure should produce a more compliant joint while eliminating hot spots that were encountered in solder joints. It was possible that the microstructure would further evolve when exposed to high temperature as the densification process was cut off due to the relatively short hold at the peak temperature during die attachment. This was especially true if reheating was above the bonding temperature, such as 300 ℃ or higher. Any gains in the mechanical, electrical and thermal properties would likewise be small.



(a)



(b)

Figure 2.39. Scanning electron microscope images of the uncovered nanoscale silver paste on a substrate sintered at 275℃: (a) 10,000X magnification and (b) 50,000X magnification

Figure 2.40 is an image of a sintered chip attachment obtained from scanning acoustic microscopy (SAM). The Si chip with dimensions of 13.6 × 13.6 mm^2 was attached on a silver plated alumina DBC substrate at 275 ^oC and 3 MPa for 20 minutes. The SAM image showed a relatively uniform bonding interface with few small voids. A uniform bonding interface such as this would be less likely to form hot spots underneath the chip and was expected to have high reliability under temperature or power cycling. Large voids forming underneath the device, as was often observed in soldered joints could result in lower load-bearing area and potential stress concentrations within the attachment, especially at locations adjacent to voids. Such elevated local stress was likely to shorten the lifetime of the joint. A uniform distribution of much smaller voids and a larger effective bond area was therefore more favorable.

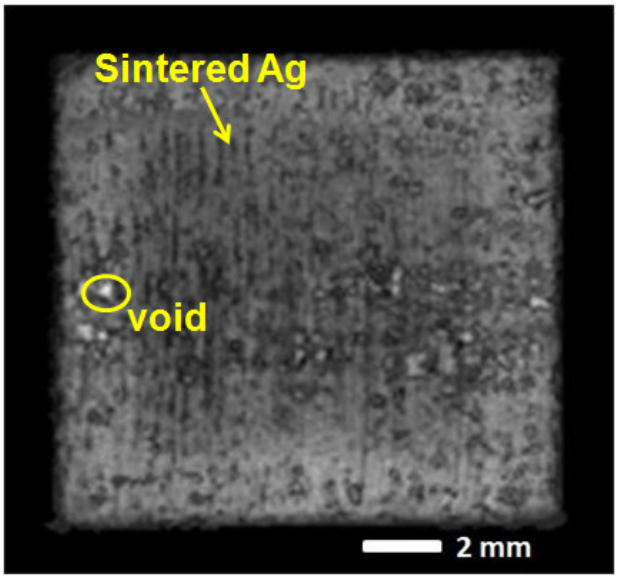


Figure 2.40. SAM image of a sintered 13.6 x 13.6 mm^2 chip attachment.

Figure 2.41 shows an X-ray transmission image of a 12 x 12 mm^2 silicon device attached on DBC substrate using nanoscale silver paste. Similar to the above SAM image, no obvious voids or delamination can be found from the X-ray image. Compare to the X-ray image obtained from solder alloys, large-area attachment by the sintering technique certainly had superior bonding performance.

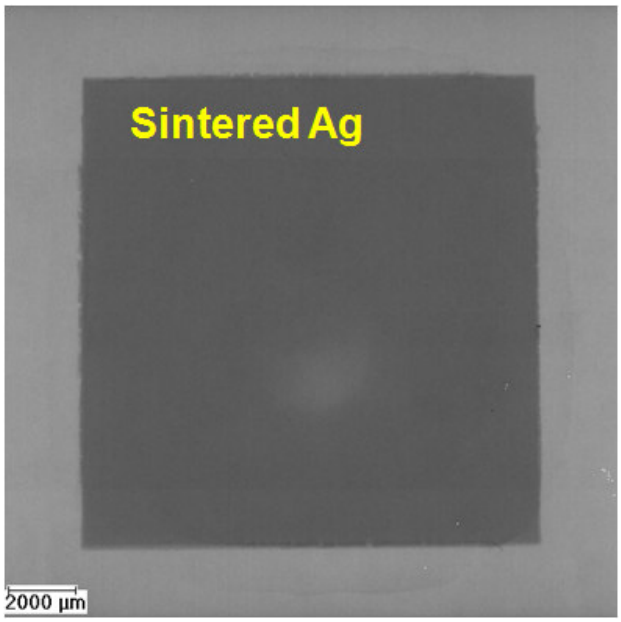
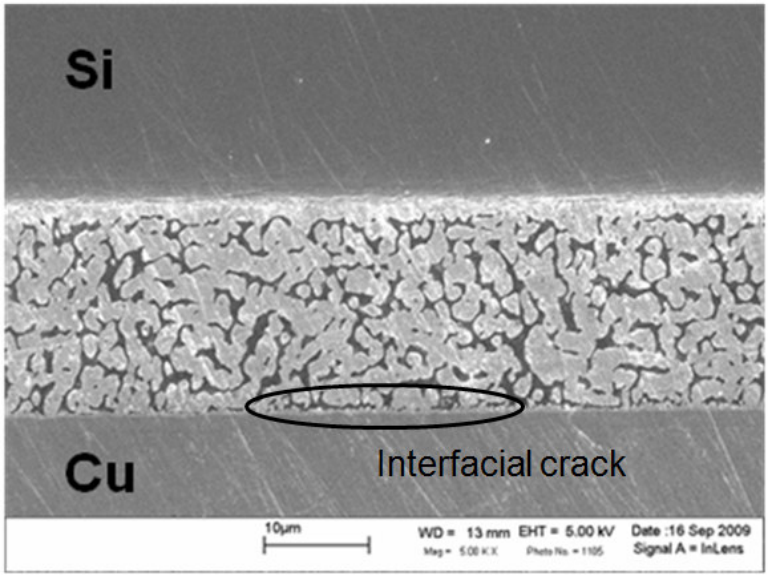


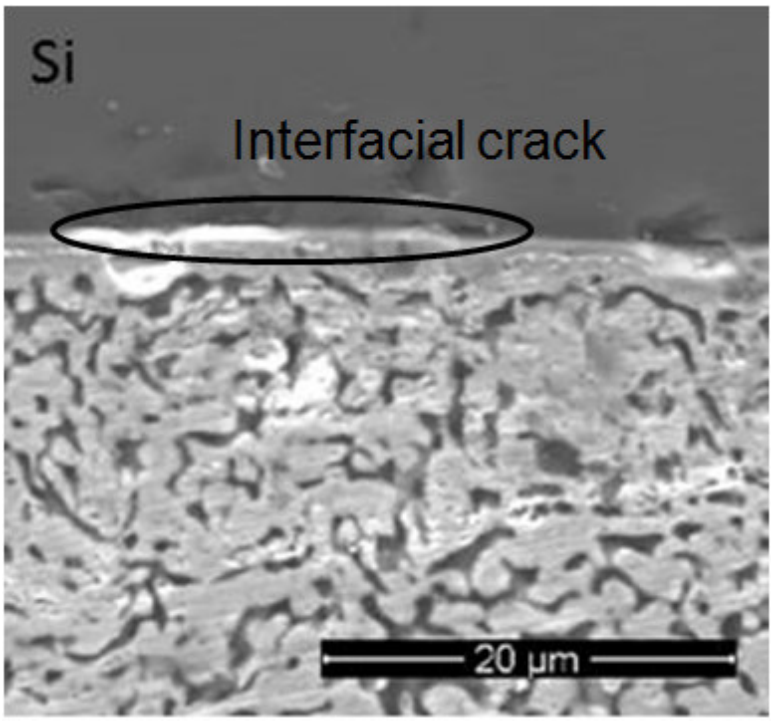
Figure 2.41. X-ray image of a sintered 12 x 12 mm^2 chip attachment.

Figure 2.42 shows cross-sectional SEM microstructures of the sintered 12 ×

12 mm^2 chip attachments bonded to copper substrates at 0 MPa, 1 MPa, and 5 MPa. The sintered microstructure at 0 MPa, Figure 2.42(a) and (b), contained wide, elongated pores. Its relative density was approximately 75 %, consistent with a volume-displacement measurement. The microstructures of the sintered attachments under pressure, Figure 2.42(c) and (d), showed higher density and finer porous lines with increasing pressure. A closer examination at the interface between the chip and the sintered silver at 0 MPa also revealed some possible voids or gaps at the interface. However, when a low pressure of 1 MPa was applied, a near-complete chip-to-sintered paste bonding interface was obtained. An image obtained by energy dispersive x-ray (EDX) analysis shown in Figure 2.43 taken at an interface spot in the 1 MPa-bonded sample, showed interface continuity. This was also observed in the 5 MPa sample.



(a)



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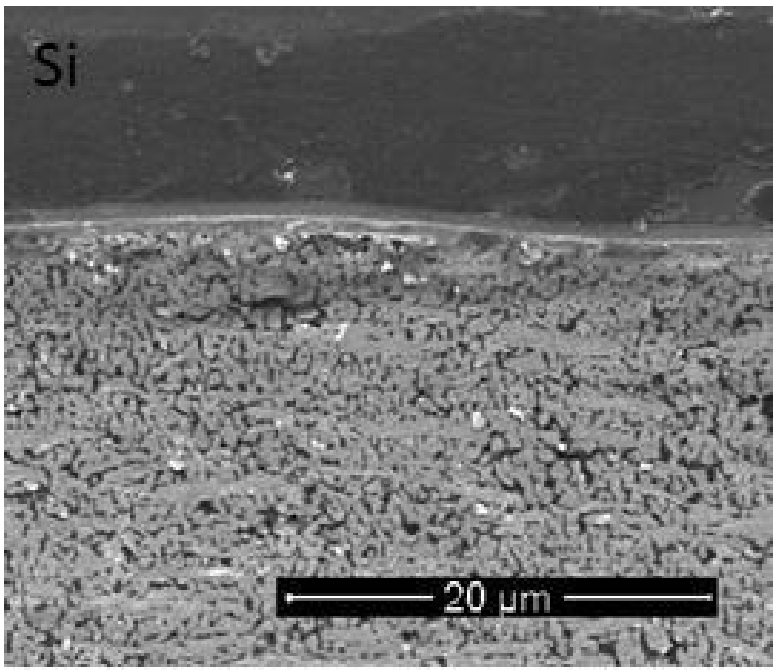
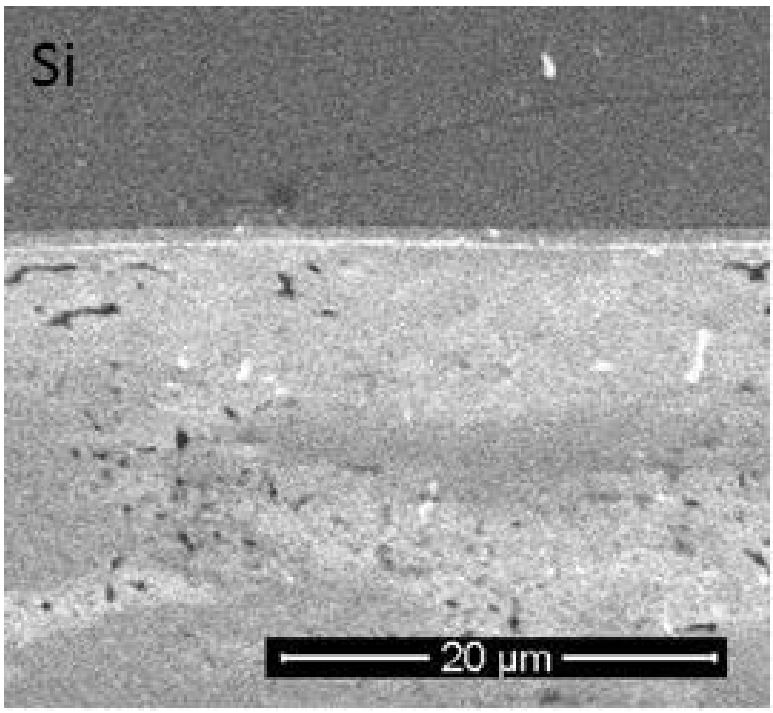


(c)



(d)

Figure 2.42. Cross-sectional SEM images of the sintered Ag joints at: (a) and (b) 0 MPa; (c) 1 MPa; and (d) 5 MPa.

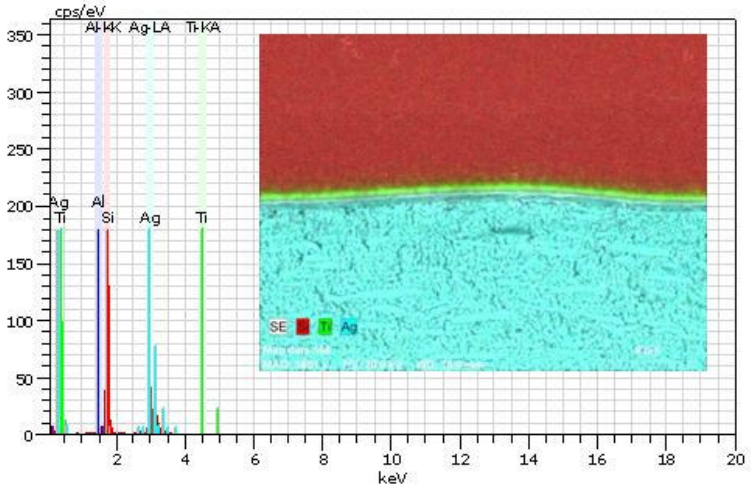
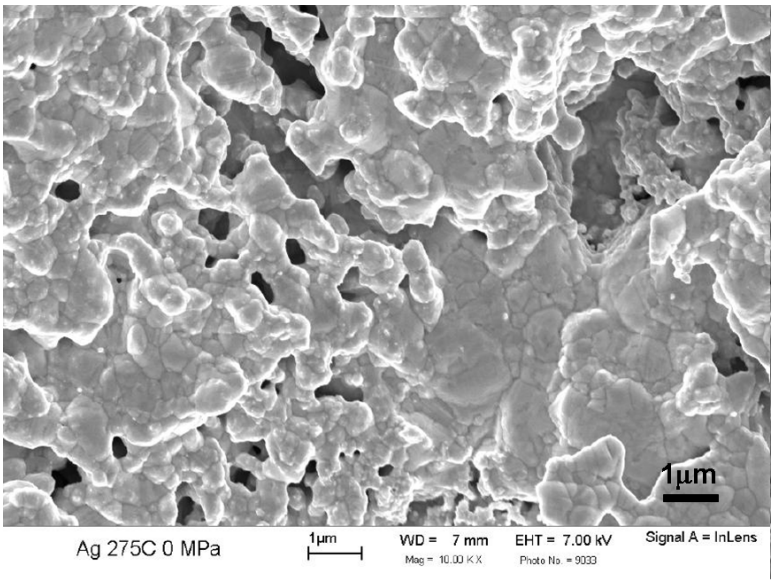


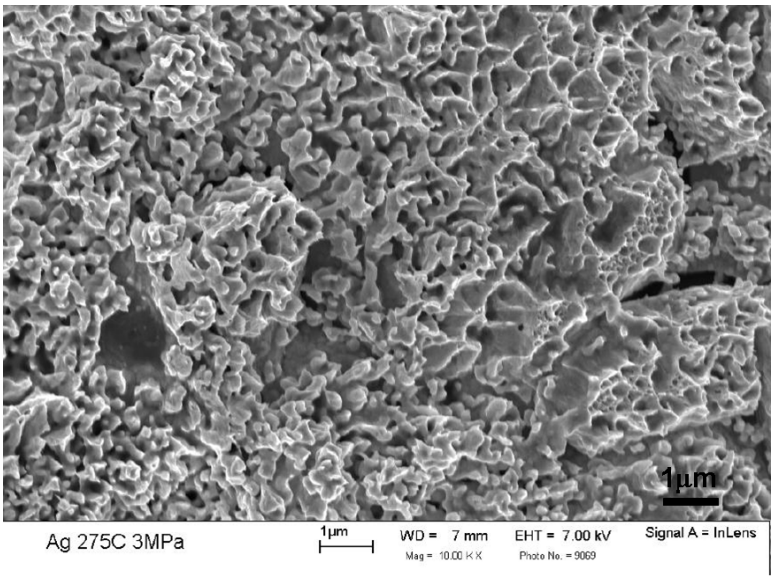
Figure 2.43. EDX mapping across the chip-to-silver paste interface in the 1 MPa bonded sample.

Figure 2.44 [96] shows the microstructures along the shearing plane of sintered silver from the sheared-off joints formed at 0 MPa, 3 MPa, and 5 MPa. Failure in the 0 MPa sample occurred mostly along the chip-paste interface, which we refer to as an adhesive failure. The corresponding microstructure as shown in

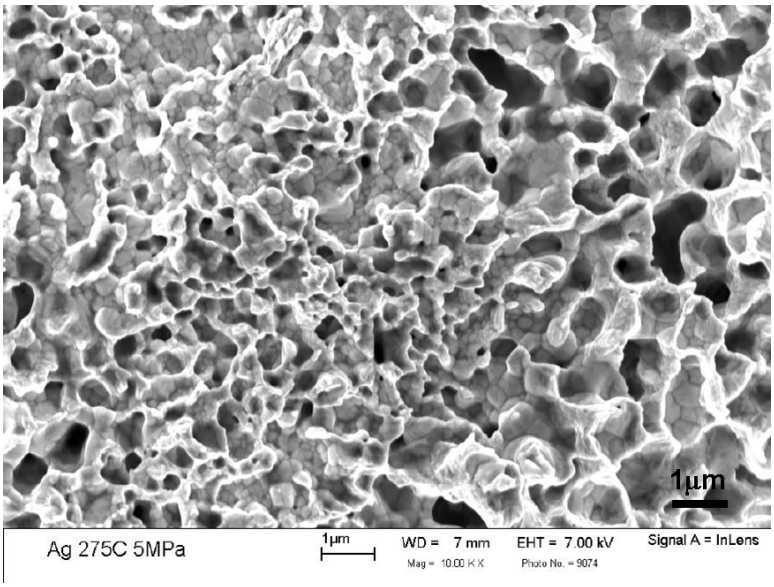
Figure 2.44(a) revealed little deformation in the grain structure. In contrast, samples sintered under 3 MPa and 5 MPa pressures failed primarily within the sintered layer (cohesive failure), and their corresponding microstructures, Figure 2.44(b) and (c), showed considerable plastic deformation in the grain structures, reminiscent of ductile failure. This was expected since silver was a ductile metal. Thus the samples sintered under pressure primarily exhibit the strength of the attachment layer itself. If it were possible to conduct shearing tests on free-standing specimens, this was what we should expect to observe. On the other hand, the shear strength from the first sample (0 MPa) also reflected the nature of the interface (device or substrate), which in this case was weaker than the sintered microstructure. In many cases, due to unavoidable defect formation during the attachment procedure, the failure will be mixed-mode with one mode dominating depending on the initial state of the interface and the level of applied pressure. Thus, at some pressure level, failure would become almost entirely cohesive as was observed in the experiments.



(a) 0 MPa



(b) 3 MPa



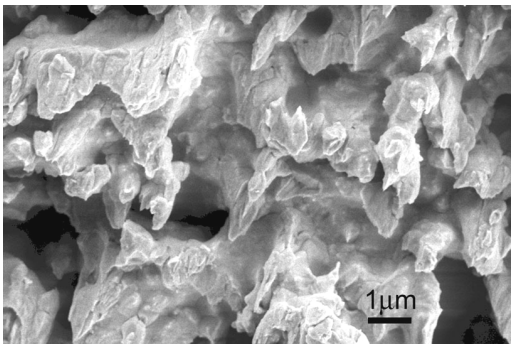
(c) 5 MPa

Figure 2.44. Plane-view SEM images of sintered silver from the sheared-off joints formed at (a) 0 MPa, (b) 3 MPa, and (c) 5 MPa [96].

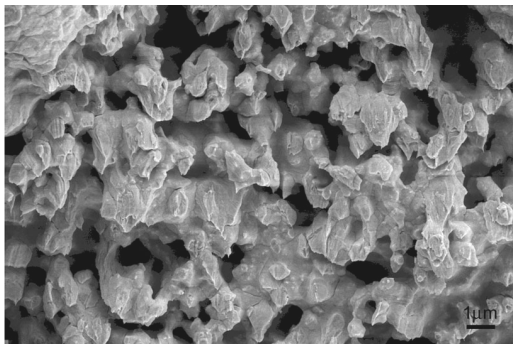
The microstructural observations were consistent with the shear strength vs. pressure result shown in Figure 2.36. Using a low pressure, as low as 1 MPa, during the sintering stage prevented the out-gassing organics from detaching the chip at the interface and from loosening the nanoparticle packing, which would lead to wide porous lines. The microstructures of sintered silver under pressure, even at 5 MPa, were still porous with a relative density of about 80%. It was

believed that the porous microstructure was more compliant and able to relieve thermomechanical stresses based on previous mechanical tests of porous samples of the sintered material (lower effective elastic modulus). Coupled with a higher melting temperature of 961 ℃, which made it less susceptible to creep-related deformation at elevated temperature, it was expected to be more reliable compared to soldered joints. Given that silver also had high thermal conductivity, low-temperature, low-pressure sintering of nanoscale silver paste had the potential to be a superior lead-free solution for large-area chip attachment for high-temperature applications.

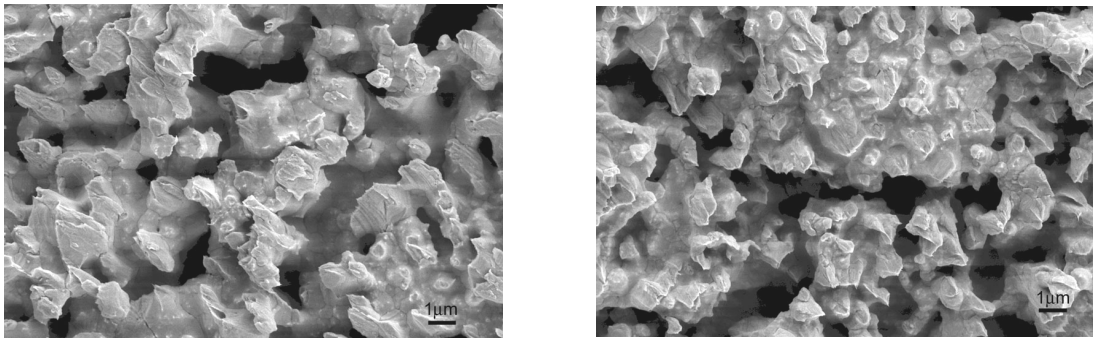
Figure 2.45 shows the microstructure of sintered silver before and after temperature cycling, -40 - 150 ^{o}C. No obvious change can be found from the sintered structure after up to 800 cycles. Silver retained its porous structure; with slightly increase in porosity. This again confirmed the hypothesis that with low elastic modulus, sintered silver was compliant to thermomechanical stresses. Sintered silver joint possessed superior temperature-cycling reliability than joints formed by solder alloys.



As-sintered



100 cycles



300 cycles 800 cycles

Figure 2.45. SEM of sintered silver joint before and after temperature cycling.

2.4. Summary of low-temperature sintering of nanoscale silver paste

A nanoscale silver paste that can be used as a lead-free die-attachment had been developed. It can be sintered at temperatures below 300 ℃ and was capable of high temperature operation. The joint that was formed after sintering contained sub-micrometer to micrometer-scale pores. This type of microstructure gave a very low elastic modulus, 9 GPa, which was substantially lower than those of bulk silver and high-temperature solder alloys. Its electrical and thermal conductivities were around five times higher than those of solder alloys. Typical die-shear strength of around 30 MPa can be obtained at 300 ℃ or lower sintering temperature at a dwell time of 10 minutes. Temperature cycling results indicated that the nanoscale silver die-attach material had good resistance to thermal cycling. This combination of properties made it a suitable candidate material for attaching SiC devices for elevated temperature operation.

For large-area device attachment, a modified heating profile was designed and used to sinter the nanoscale silver paste. Up to 5 MPa pressure was applied during the sintering stage. Strong attachment of large chips to substrates with silver, gold, and copper metallization was demonstrated. Analysis of the sintered joint by scanning acoustic imaging and electron microscopy showed that the attachment layer had a uniform microstructure consisting of micron-sized pores to offer excellent reliability for high temperature applications.

Chapter 3. THERMO-MECHANICAL RELIABILITY OF DIRECT BONDED ALUMINUM (DBA) SUBSTRATE

3.1. Significance of substrate reliability in electronics package

The substrate in electronics packaging must provide mechanical support for the components, thermal dissipation, and electrical interconnection. Mechanical integrity, high thermal conductivity, and high electrical current capability are the most desirable properties of a good substrate technology. However, substrate reliability has been a long time concern in electronics packaging, and becomes even more serious when operating at higher temperature. At an elevated temperature, organic board based substrates have low glass transition temperature, T_g, and are naturally not suitable for reliable use. Ceramic based hybrid technologies are now in the dominant position. However, due to the huge CTE mismatch between the conduction material, usually copper, and the base ceramic plate, Al_2O_3, AlN, or BeO, the DBC structured technology tend to have problem in mechanical integrity. The conduction copper layer is often found delaminated from the ceramic plate, which eventually causes failure in the whole packaging. In this study, a new substrate material, direct bonded aluminum, is studied. The thermomechanical reliability of DBA substrate is investigated, mainly through the high-temperature cycling test from -55 ^oC to 250 ^oC. Features such as the metal-ceramic interface integrity, aluminum surface hardness, aluminum surface roughness, and the underlying microstructure are measured and characterized.

3.1.1. Thermomechanical failure of DBC substrate

Ceramic hybrid approach is the state-of-the-art technology of designing electronics for use above 125 ^oC. There are three ceramic materials which are

typically used for substrate in this approach: aluminum oxide (Al_2O_3), beryllium oxide (BeO), and aluminum nitride (AlN). Among them, aluminum oxide is the cheapest and therefore the most common of the three. The advantage of Al_2O_3 is the close match between its coefficient of thermal expansion (4.2 ppm) and that of silicon (2.6 – 3.5 ppm). This lessens the thermomechanical fatigue stresses which are generated during the -55 ^oC to 250 ^oC temperature swing typical of high temperature electronics systems. However, the disadvantage of Al_2O_3 is its poor thermal conductivity, which makes it acceptable for systems operate in high ambient temperatures, but not acceptable for systems where a significant fraction of the heat is generated by the device and must be dissipated through the substrate.

For high temperature power electronics, a better choice is BeO which has a significantly higher thermal conductivity. Its main drawback is the CTE mismatch with silicon (7.2 ppm for BeO vs. 2.8 ppm for Si), which increases the thermomechanical stresses induced during power or thermal cycling. Other drawbacks include it high cost, 10 times more expensive than Al_2O_3, and its potential toxicity.

The third ceramic alternative, AlN, combines the CTE match of Al_2O_3 with the high thermal conductivity of BeO [97]. While AlN also has a high cost, its primary drawback has traditionally been difficulty in developing adherent metallization. This issue may have been solved with the use of active braze materials [98,99]. Packages metalized in this way survived exposure to 350 ^oC for over 2000 hours exhibiting very limited diffusion and oxidation and no loss of adhesion.

Although DBC outperforms many other substrate materials in current carrying capacity, high toughness, high thermal and electrical conductivity, and controlled overall CTE, due to the fact that it is a sandwich-structured material, it

performs poorly in the thermomechanical reliability test. The big difference in aluminum and ceramic (AlN) CTE generates tremendous amount of thermomechanical stress during the operation at high temperature and the situation becomes even worse in the reliability test. Figure 3.1 [100] shows a typical initial failure mode of DBC under cyclic thermomechanical stress.

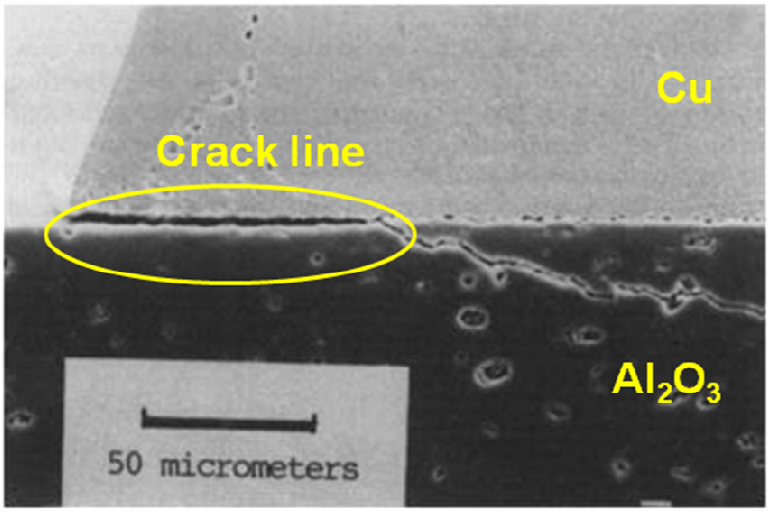
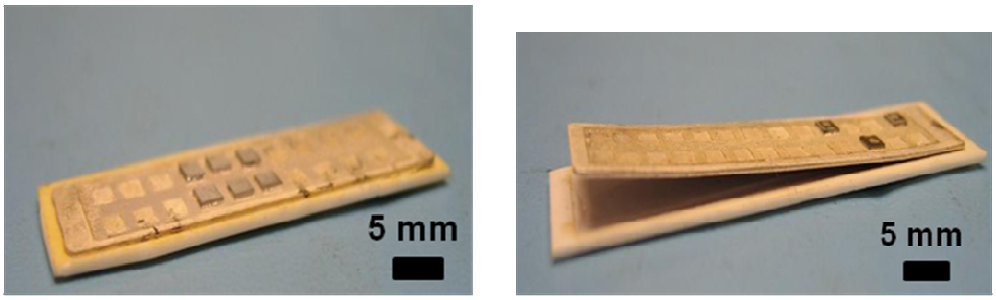


Figure 3.1. Initial crack formation of DBC at the metal-ceramic interface [100].

Under thermomechanical stress, cracks will initiate at the copper edge, propagate a short distance along the metal-ceramic interface, penetrate into the ceramic layer, and eventually cause the delamination of copper layer. Figure 3.2 shows a later stage of this delamination problem of DBC. For the specific DBC sample shown in Figure 3.2, it underwent 600 temperature cycles from – 40 to 125 ^{o}C.

In addition, if the targeted temperature is raised to 250 ^{o}C, more severe delamination problem would happen at earlier stage. It only takes 20 cycles to completely peel the copper from the ceramic, and causes completely substrate failure. Therefore, finding a substrate material with better thermomechanical reliability than DBC becomes a critical issue for high-temperature electronics packaging, and must be resolved.



(a) (b)

Figure 3.2. DBC substrate (a) original DBC; (b) copper peeled-off from DBC.

3.1.2. Advantages of DBA over DBC

The reason aluminum is replacing copper conducting layer lies in the excellent thermomechanical reliability that DBA substrate offers in the accelerated temperature cycling test. Comparing with copper, aluminum has lower elastic modulus (70 GPa for aluminum, 110 – 128 GPa for copper), which makes DBA substrate less susceptible to thermomechanical fatigue failure for the long-term reliability; also the lower yield stress (20 MPa for aluminum, and 33 - 70 MPa for copper), together with the lower elastic modulus, of aluminum, than copper makes DBA substrate generate less thermomechanical interfacial stress between the metal and the ceramic baseplate; and thirdly, the flatter plastic strain rate of aluminum would result in less strain hardening of aluminum than copper when under significant stress during the temperature cycling test. Figure 3.3 shows the stress-strain relations for both copper and aluminum. Therefore, combining these attributes together, DBA substrate is theoretically more reliable than DBC substrate from the thermomechanical point of view. In addition, on an equal weight of cross section and equal cost basis, aluminum is a better conductor than copper.

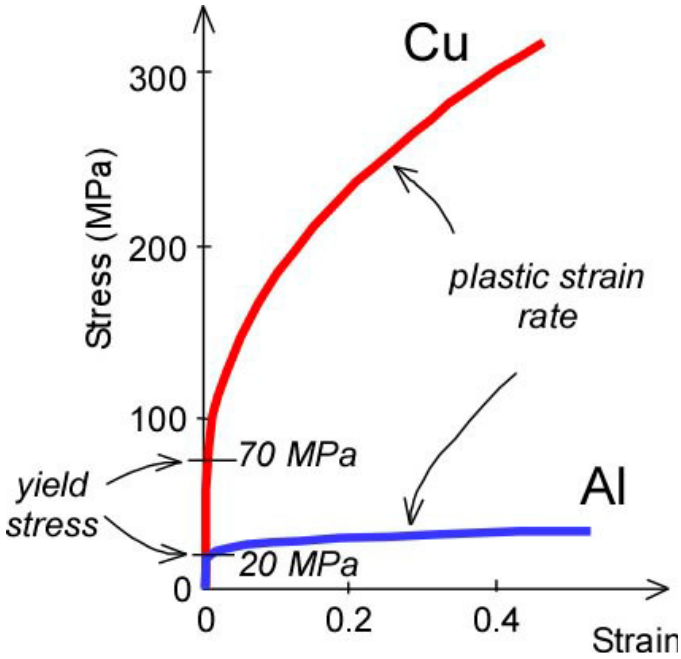


Figure 3.3. Mechanical characteristics of copper and aluminum.

Although DBA offers superior thermomechanical performance than DBC, it is worth noting that DBA suffers in two aspects for being used as a substrate material in electronics packaging: (1) Unlike copper, fresh aluminum can be easily oxidized, and form the aluminum oxide layer on the surface. This compact, stable oxide layer prevents aluminum from conventional electroless and electro-plating of other metal layer, which is an essential step for aluminum to be compatible with die-attach materials such as solder alloys and nanoscale silver paste. Additional surface treatment has to be prior to the plating which would complicate the overall process and brings more reliability issues. (2) As stated in the introduction session, the targeted temperature for this study is 250 ^{o}C (523 K), which corresponds to about 56% of the aluminum melting point (933 K). Tremendous microstructural evolution would occur under the thermomechanical stress caused by the CTE mismatch of aluminum and ceramic baseplate at this temperature. Therefore very different behavior is expected from DBA compared to DBC during the thermomechanical reliability test.

Studies at low-temperature already shown that DBA substrate is indeed more reliable than most of the other substrate techniques, Table 3.1 [101] presents some of the comparison of DBA with conventional DBC substrate from the thermomechanical reliability point of view. Therefore in this study, we would like to extend the thermomechanical reliability of DBA to higher temperatures, to evaluate whether DBA is indeed qualified for high-temperature packaging.

Table 3.1. Comparison of DBA and DBC substrate [101].

		AlN-DBC	AlN-DBA
CTE (ppm/K)		~4.5	~4.7
Thermal conductivity (W/mK)		150~180	150~180
Electrical resistivity (Ω cm)		>10^{14}	>10^{14}
Dielectric constant		8.6	8.7
Reliability	-40℃ ⇔ 125℃/in gas	delamination after 600cyc	no cracks after 3000 cyc.
	-78℃/liq. ⇔ 350℃/in gas	delamination after 5cyc	no cracks after 20 cyc.
	-55℃/liq. ⇔ 125℃/liq.	break after 1000cyc	no cracks after 3000 cyc.

3.2. Experimental Procedure

DBA substrates were purchased from Denka Inc. Japan. The aluminum-nitride base plate thickness was 650 µm AlN, with 300 µm thick 99.3% aluminum on each side. Figure 3.4 shows the photo of a DBA substrate and a schematic of the DBA cross section.

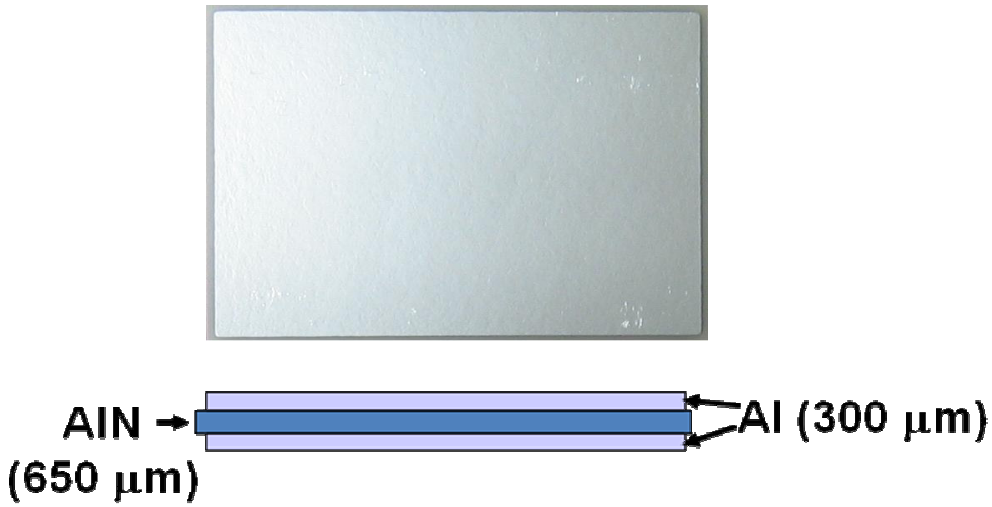


Figure 3.4. DBA sample obtained from Denka.

3.2.1. Sample preparation

Chemical Etching of Circuitry Patterns on DBA Substrate

Since the metal used in DBA was pure aluminum, it was easily etched by warm ferrite chloride acid solution. For the purpose of simplicity, Kapton™ tape was used to create the patterns on the aluminum surface instead of standard etching resist.

The etch process was done in a spray etch chamber, and when warm ferrite chloride acid solution was used, the aluminum etch speed was about 1-mil every minute, and the etch quality was excellent with sharp edges. After the aluminum was etched off, AlN plate can be sliced by laser to form small pieces for further study.

Metallization of DBA Substrate

Introduced in the previous part, DBA was designed and manufactured as an alternative of DBC from the thermo-mechanical reliability point of view [102]. However, the biggest challenge of using DBA in electronic packaging is the strategy of metalizing the aluminum surface, to be able to incorporate with

commonly used die-attach and thermal dissipating materials. For most of the substrates used in electronic packaging, the surface is nickel, silver, or gold finishing accordingly to applications requirements. Nickel finishing is mostly used in a moderate environment, such as medium temperature, dry air, and low power applications. On the other hand, when temperature, humidity, and power density are more of a concern, silver or gold finishing is much preferred because of their excellent thermal and electrical conductivity, as well as high resistance to oxidation and corrosion. In practice, a Ni-Ag or Ni-Au double layer structure is often used to protect the copper or aluminum surface. Electrolytic or electroless plated nickel layer acts as a diffusion barrier between copper and silver/gold to minimize the interdiffusion between copper and silver/gold layer [103]. The copper-silver/gold interdiffusion is the root cause for the failure of solder bumps and many other die-attach materials when subject to cyclic thermal tests [104].

It is always difficult to plate aluminum and its alloys with any metal or metallic base surface coating, either by a cathodic or electroless deposition due to the tenacious oxide layer present on aluminum. Aluminum and its alloys have high affinity for oxygen which results in a rapidly growing thin oxide film on freshly cleaned and etched aluminum surfaces. It is difficult to plate aluminum substrates covered with such an oxide film with good adhesion. An appropriate pre-treatment process is an essential surface conditioning step before any plating is carried out. The most satisfactory and practical method available for aluminum preparation prior to further deposition is zincating [105,106], with the purpose of [107]:

- Increase the corrosion resistance;
- Reach a higher abrasion resistance;
- Increase the soldering and welding properties;
- Increase the electrical contact ability.

Zincating is an electrochemical exchange reaction between zinc complexes in solution and the aluminum substrate, depositing zinc crystallites at the expense of aluminum dissolution. The zinc deposition protects the surface, effectively providing a basis for subsequent deposition. During the zincating process the aluminum oxide is firstly dissolved in the zincating solution as follows;

$$Al_2O_3 + 2NaOH + 3H_2O \rightarrow 2NaAl(OH)_4 \qquad 3.1$$

The oxidation of aluminum drives reduction of the zinc ion to produce a layer of zinc metal through a galvanic displacement reaction as follows, and is schematically shown in Figure 3.5;

$$3Na_2(ZnOH)_4 + 2Al_{(substrate)} \rightarrow 2NaAl(OH)_4 + 4NaOH + 3Zn_{(deposited)} \qquad 3.2$$

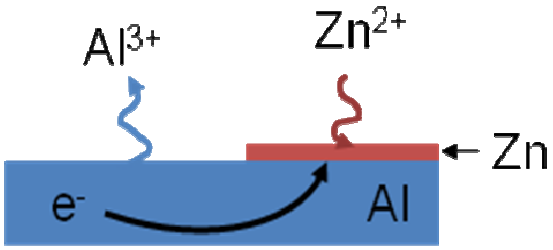


Figure 3.5. Schematic of zincating treatment on aluminum.

A zincate treatment is composed as:

- Degreasing: mildly alkaline aqueous immersing cleaning, to remove polishing pastes;
- Etching: highly alkaline solution to remove oxides;
- Desmutting: acid solution to remove the pickling residues of etching;
- Zincate treatment: the zincate treatment can be applied two times, the first zincate layer is removed in nitric acid, and then the aluminum surface is immersed again into the zincate solution. The second zincate layer has a better adherence, finer crystals and is denser.

Before executing the zincate process, pre-cleaning of the aluminum surface was done. A piece of DBA was soaked in acetone and alcohol for 10 minutes respectively, with ultrasonic agitation, to remove the residual contaminations and polymer left by the Kapton tape during the patterning step. After rinsed with DI water, the zincate treatment and the nickel & silver plating was carried out as shown in Figure 3.6.

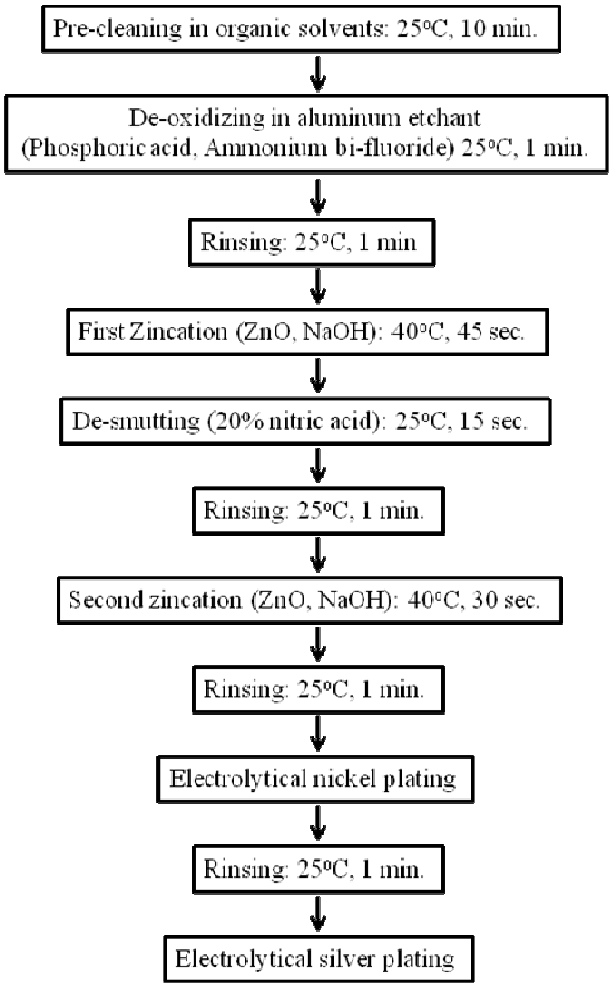


Figure 3.6. Flowchart of the complete re-metallization process of DBA.

The zincating process usually consisted of a double dip into the zincate solution to produce a uniform layer of zinc on the aluminum surface [99]. And there were also some concerns on the zinc thickness from the packaging point of view:

- too thin → not effective as an anchor for electroplated layers;
- too thick → adhesion problem (form of zinc crystals, act as corrosion starting point, further cause blistering of the layer).

In a zincate process, the aluminum is dissolved by two competing reactions, displacement reaction between aluminum and zinc ions, and chemical etching of aluminum at high pH solution. The dissolution of aluminum at high pH is slower than the displacement reaction of aluminum with zinc. The electrode potentials and dissolutions of aluminum were measured with immersion time by Lee [108]. From their results, the electrode potentials were stabilized within 20 seconds when zincate process was completed and aluminum started to be dissolved at high pH. And then the zincate time needs to be controlled within 20 seconds to minimize aluminum dissolution at high pH. During the nucleation stage, zinc particles preferentially formed clusters on convex area, corresponding to the peaks or edges of aluminum surface. The dissolution of aluminum continued on all surfaces. However, zinc deposition did not occur only on all surfaces, since zinc complex ion cannot reach the inside of the holes [109]. The entrance into the holes of the zinc complex ion is suppressed by electrochemical displacement reaction between aluminum and zinc ions, leading to the dissolution of electronegative aluminum and deposition of electropositive zinc complex ion. Even though the multiple zincate process is performed, the deep holes cannot be covered by zinc. These phenomena can be explained in Figure 3.7 [110]. The aluminum is dissolved from all surfaces. However, electrons are supplied through highly conductive aluminum, and the zinc particles are deposited on convex area as seen in Figure 3.7(a). In addition, when zinc is deposited on a convex area, the diffusion path is shorter from zincate solution as shown in Figure 3.7(b). The combined results indicate that zinc nucleation sites correlate to the surface roughness and electrochemical properties [111-114].

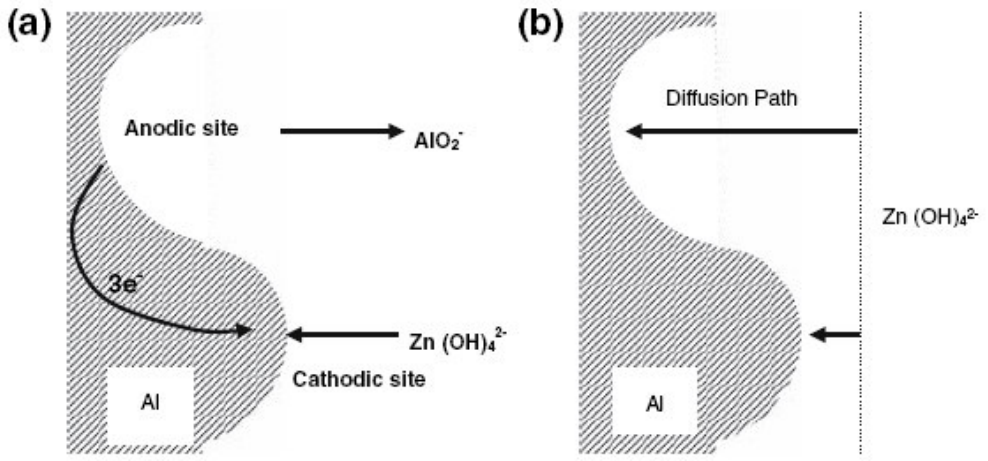
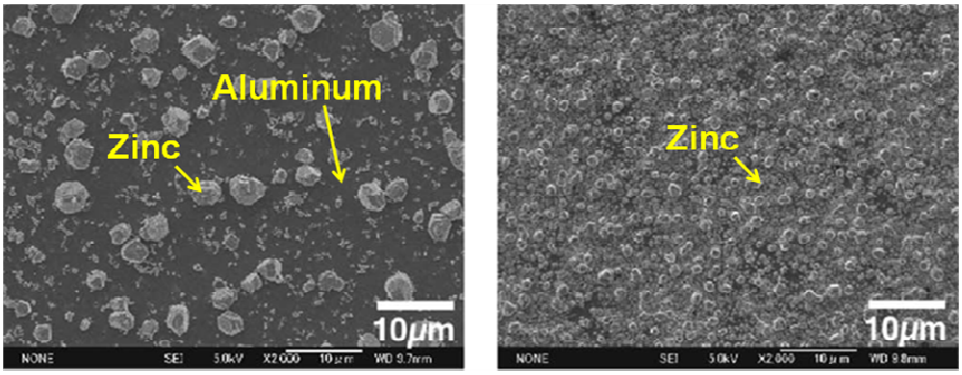


Figure 3.7. Schematic of zinc nucleation by two phenomena of (a) electron transfer and (b)mass transport [110].

Figure 3.8 [111] shows SEM images of Al films after the first and the second zincate processes. Zinc was deposited in both the first and second zincate. A more uniform deposition feature can be found on film with second zincation treatment. After the zinc layer was built up on the aluminum surface, the following deposition of metal can be either electrolytic or electroless plating with copper, nickel, or chromium. As nickel is often used as the diffusion barrier layer in electronic packaging [115], electroless plating of nickel is the most commonly applied approach post the zincating process. However, due to the high phosphor content that most of the electroless nickel plating baths contain, the interdiffusion of nickel and phosphor will result in Kirkendall voids [116,117], which have strong effects on the die-attach joint reliability. Therefore from the reliability point of view, for an electronic packaging to survive large temperature range excursions, electrolytic plating of nickel and silver was preferred.



1st zincation 2nd zincation

Figure 3.8. SEM images of Al substrate after (a) 1st zincation and (b) 2nd zincation [111].

3.2.2. Metallization characterization

Zincating and Plating Quality Examination

After the DBA substrate was properly metallized by the zincating process, and further electroplated with nickel and silver, preliminary testing was done by the surface scratch test, tape test, and thermal treatment test to tell whether the adherence strength of the plating layer to the aluminum surface was strong enough for used in electronic packaging. To characterize the microstructural adhesion between the plating layers, SEM was employed to examine the cross section of the metallized sample, and correspondingly to measure the plating thickness.

Metallization Solderability Test

After the metallization was qualified, the substrate was incorporated with die-attach materials to test the material's compatibility. Four types of die-attach materials were selected: lead-tin (Pb37Sn) eutectic solder alloy, gold-tin (Au20Sn) eutectic solder alloy, high-lead (Pb5Sn) solder alloy, and nanoscale silver paste. For the three types of solder alloys, a temperature reflow was applied at 30–50 ^{o}C higher than their melting temperature, which were 183 ^{o}C, 280 ^{o}C, and 310 ^{o}C for lead-tin, gold-tin, and high-lead solder alloys, respectively. For the nanoscale

silver paste, as it was different from solder reflow process, a specific designed drying and sintering profile was employed to sinter the paste at relatively low temperature, as shown in Figure 2.24(a). Five mechanical devices were attached to the metallized DBA substrate by each type of die-attach material, and their bonding strength was measured to judge the Solderability/Sinterability of the metallization layer on DBA.

3.2.3. Accelerated temperature cycling test

From the thermomechanical reliability point of view, thermal cycling test was conducted to investigate how reliable the DBA substrate was, as well as the metallization layer. Since high temperature applications were being targeted, a conventional cycling range was no longer applicable in our project. The thermal cycling range was set to -55 ^{o}C - 250 ^{o}C. The cycling test was carried out in a Tenney environmental cycling chamber. Due to limitations of the equipment, a separate heating setup was designed and incorporated with the cycling chamber to realize the thermal cycling function.

Because the cycling chamber could not heat up to 250 ^{o}C, a hot plate was employed. The hot plate was controlled by an external power supply. A timer was further employed to control the turn-on and cut-off time of the power supply. The chamber was set stable at -55 ^{o}C during the cycling (however it would raise several degrees during the cycling). When the power supply for the hot plate was turned on, all the samples and the hot plate would be heated up to 250 ^{o}C, in about 18 minutes. A thermocouple was employed to measure the temperature right under the testing sample, and was also used to control the external power supply. As the whole cycling chamber was kept at low temperature, after the power was turned off, all the samples and the hot plate itself would cool down to the chamber's ambient temperature, -55 ^{o}C, in about 35 minutes. Figure 3.9

shows the recorded cycling profile used in this project. One cycle is about 53 minutes.

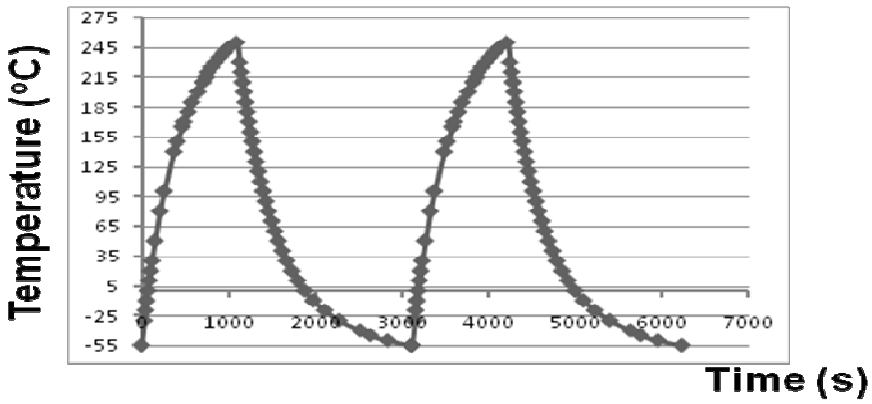


Figure 3.9. Temperature cycling profile.

To double check the temperature on testing samples, multiple thermocouples were placed as close as possible to various samples. Figure 3.10 shows a schematic of the placement of thermo-couple in the temperature cycling chamber. And Table 3.2 lists some of the measured temperatures at each point of interest.

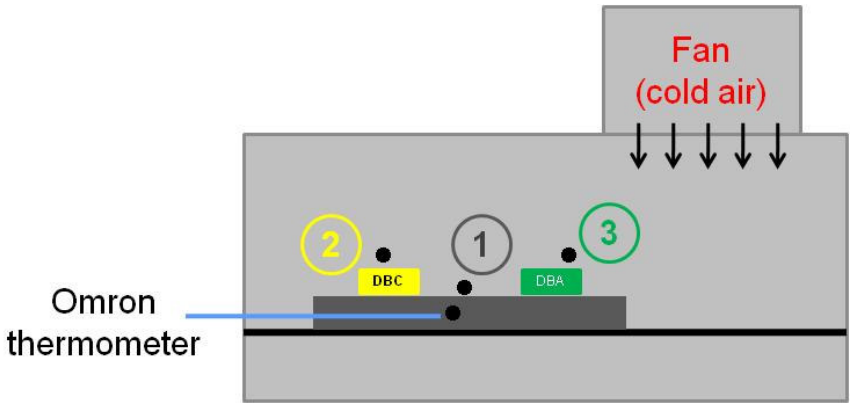


Figure 3.10 Schematic of thermo-couple placement in temperature cycling chamber.

Because the testing samples were heated up by a hot-plate placed underneath, the temperature on the sample surface should be lower than the surface temperature of the hot plate. An 8 °C to 12 °C temperature drop was found on samples with different structure. When the hot-plate was turned off, all

the samples were cooled down by cold air coming from a fan, the temperatures on samples were able to reach almost the same temperature as that of the chamber.

Table 3.2. Measured temperatures at each points of interest.

	Omron	1 (Hotplate)	2 (Top of DBC)	3 (Top of DBA)
Initial	-55 ^{o}C	-54.6 ^{o}C	-55.5 ^{o}C	-55.2 ^{o}C
Highest	227 ^{o}C	250 ^{o}C	238.6 ^{o}C	242.3 ^{o}C
Lowest	-55 ^{o}C	-54.2 ^{o}C	-55.4 ^{o}C	-55.3 ^{o}C

At any pre-determined number of cycles, two to three pieces of testing DBA substrate samples were taken out of the cycling chamber to examine the aluminum-ceramic interface integrity, measure the aluminum surface hardness, characterize the aluminum surface roughness, and analyze the microstructural evolution of the aluminum layer.

3.2.4. Metal-ceramic interface examination

SEM was employed for the observation of the aluminum-ceramic interface integrity. Buehler® Epoxicure™ resin was used to make the SEM samples. After the compound epoxy cured, the cross-section of the sample was polished by using carbide paper with 240, 320, 600, and 1200 grit, followed by fine polishing on cloth using 5, 1, 0.3, and 0.05-μm alumina.

3.2.5. DBA surface roughness measurement

The targeted temperature, 250 ^{o}C (523K), which corresponded to 0.56T_M of aluminum, was high enough for microstructural evolution to take place, such as creep, grain-boundary rotation, grain-boundary sliding, recrystallization, etc. Therefore, it was informative to measure the surface roughness, of the temperature cycled DBA, to visualize the macroscopic effects of those microstructural changes. Another reason to quantify the aluminum surface roughness was for the determination of the effects of the surface roughness on

the die-attachment performance. For either solder alloys or nanoscale silver paste, with bond-line of only 10 to 50 µm, substrate roughness is thought to have a strong effect on the die-attach bonding strength, as well as the thermomechanical reliability of the die-attach layer.

A Dektak® profilometer was used to measure the aluminum surface roughness, and is shown in Figure 3.11. Each sample was scanned three to five times across the whole aluminum area. Surface roughness was determined by calculating the standard deviation of the measured data.

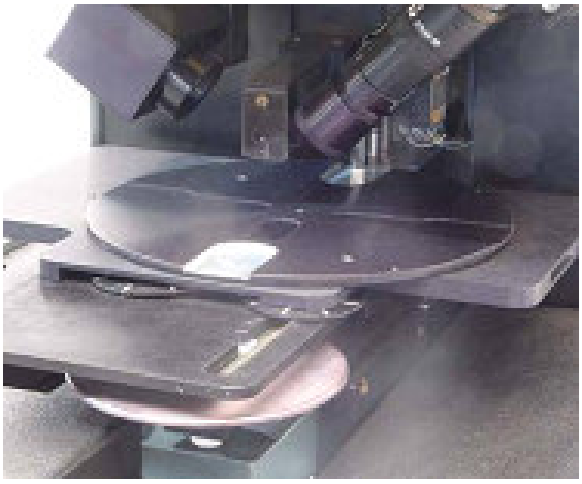


Figure 3.11. Dektak® profilometer.

3.2.6. Aluminum microstructure characterization

In addition, SEM was also employed for the microstructure analysis of the temperature cycled DBA samples. The same sample preparation process was adopted as described in Section 3.2.4. In order to reveal the grain structure of aluminum, 10% HF acid is used to attack the grain-boundary and therefore show the grain structure. After the samples were polished, they were immersed in HF for 15 seconds, and followed by rinsing in DI water and dried in hot air. To reveal the grain structure of aluminum, electron backscattered diffraction (EBSD) was also used.

3.3. Experimental Results and Discussion

3.3.1. Metallization Solderability / Sinterability

Figure 3.12 shows a DBA substrate patterned and then etched by ferrite chloride. Because it was out of the scope of this study to fabricate any conducting traces on the substrate, a piece of DBA was patterned into rectangular shapes, and was later split into 12 pieces using a diamond scraper to scribe lines between the rectangular shape, and then brek them off.

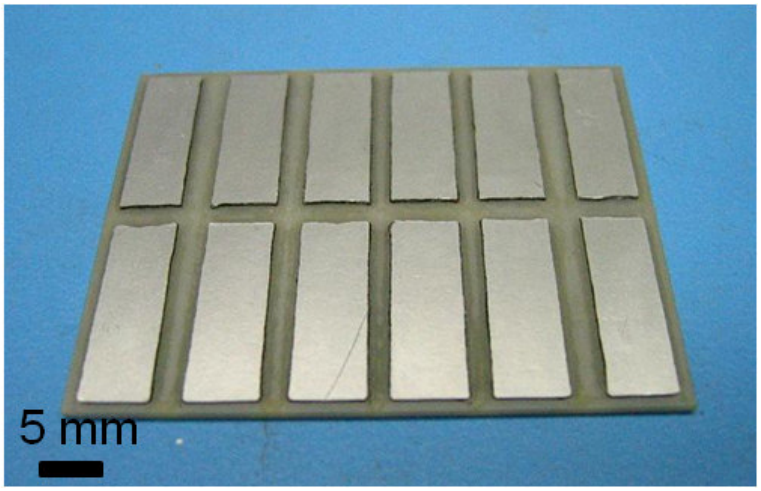


Figure 3.12. Pattern etched DBA substrate.

As described in Section 3.2.1, bare aluminum DBA was metallized by zincating and then electroplating nickel and silver. Four types of die-attach materials were tried on the metallized surface to test the solderability/sinterability of the metallization, as shown in Figure 3.13. From the observation of the solder wetting angle, and the average die-shear strengh obtained from all the die-attachments, the metallization layer was with excellent compatibility with solder alloys and nanoscale silver paste.

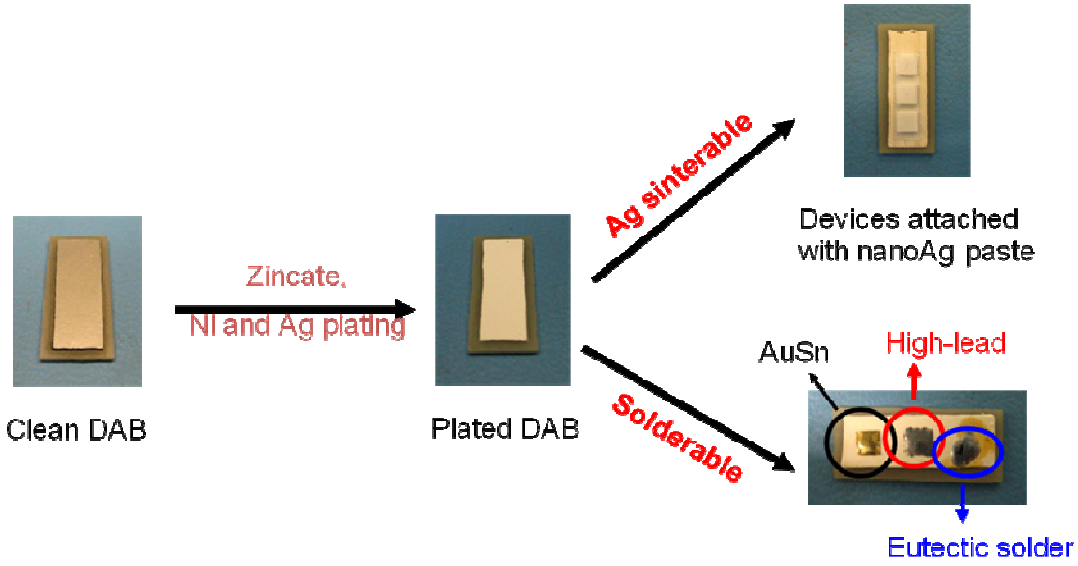


Figure 3.13. Metallization solderability and sinterability test.

The cross section of the metallized DBA was also characterized by SEM to quantify the metallization intimacy to the substrate aluminum layer, as well as the individual plating thickness of nickel and silver. Figure 3.14 shows a characteristic cross-sectional SEM image of the metallized DBA.

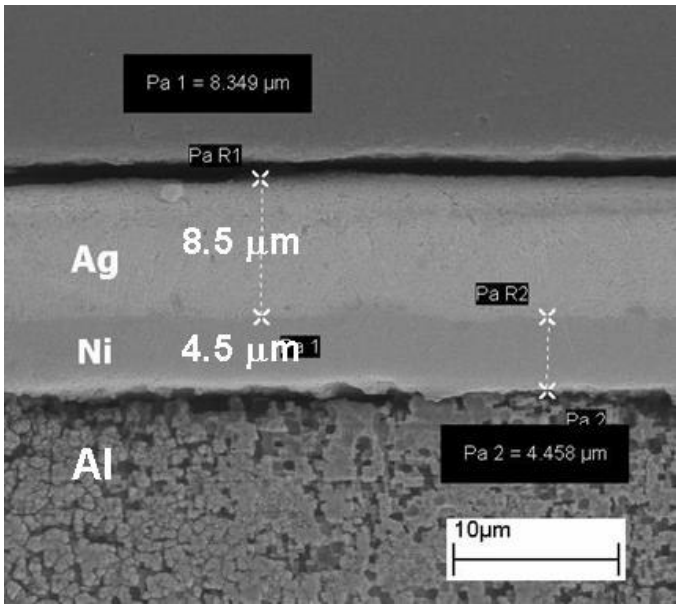


Figure 3.14. Cross-sectional SEM of the metallization layer.

Two electroplated layers, nickel and silver, were well identified, with nickel plating thickness of 4.5 µm, silver thickness of 8.5 µm. Since the die-attachments

showed average die-shear strength as compared to other known good substrate, it was reasonable to assume that the aluminum-metallization interface was continuous and very intimate.

3.3.2. Metal-Ceramic Interface Integrity Examination

For the substrate material, especially the sandwich-structured material like DBC, the most common failure mode was that the conductor layer delaminated from the ceramic baseplate. Therefore, the integrity of the metal-ceramic interface was one of the most relevant features of the temperature-cycled substrate to investigate. DBA samples were thermally cycled from -55 to 250 ^{o}C for up to 1500 cycles, and their cross sections were checked by SEM at pre-determined number of cycles, such as 50, 100, 200, 400, and 800 cycles. Figure 3.15 shows one of the typical cross-sectional SEM images of the temperature cycled DBA substrate (after 800 cycles).

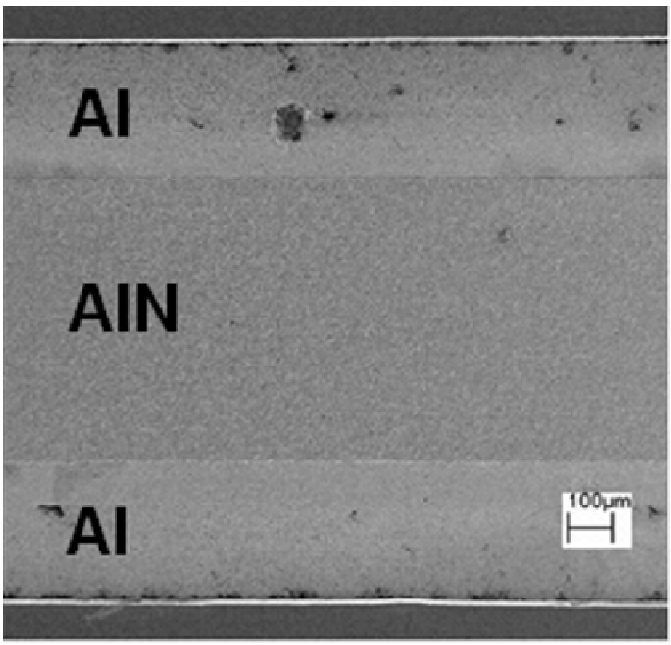


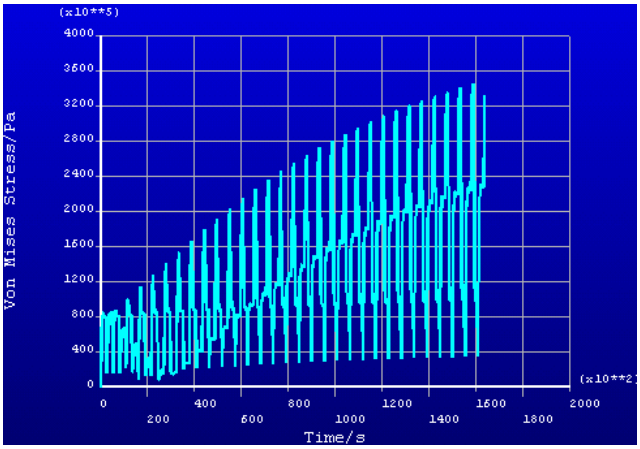
Figure 3.15. Cross-sectional SEM of temperature cycled DBA (after 800 cycles).

As noted, the aluminum-aluminum nitride interface kept intact after 800 temperature cycles from -55 to 250 ^{o}C, which showed to be a great advantage

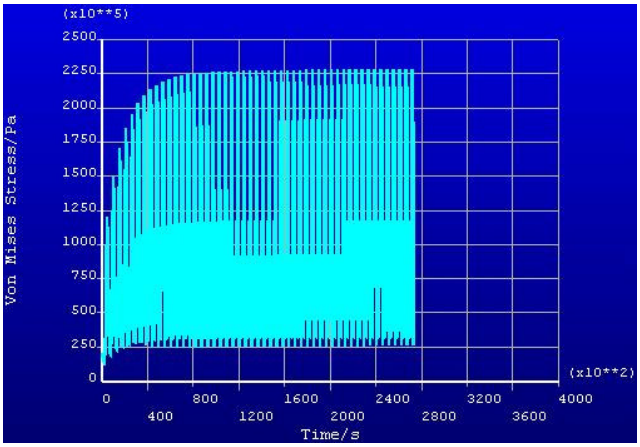
compared with DBC substrate. A typical DBC substrate would have completely failed, since copper delaminated from a ceramic baseplate, after only about 20 cycles. The more than 40 times increase in lifetime certainly made DBA a much better candidate for high-temperature packaging.

3.3.3. Stress accumulation at metal-ceramic interface

By replacing copper with aluminum, due to the less elastic modulus and less strain hardening properties of aluminum, less thermomechanical stress was supposed to build up at the Al-AlN interface than the Cu-AlN interface. Finite element method was used to simulate the thermomechanical stress accumulation at the metal-ceramic interface during temperature cycling test. Commercial available software, ANSYS, was employed for simulation. Figure 3.16 shows the change of thermomechanical stresses at the metal-ceramic interfaces. Thickness of the metal layer was defined as 310 µm, and for ceramic layer, AlN, was 635 µm. The maximum stress values were located in the ceramic at the corner joint with the metallization layer. Due to the strain hardening of both metal, mechanical constrains regularly increase in the ceramic material during temperature cycling. If constraints in AlN ceramic layer reached the rupture strength, 270 MPa for AlN, fracture would appear in the AlN baseplate. Therefore it was clear that for AlN-DBC, it only took around 20 cycles for AlN to reach 270 MPa, while for AlN-DBA, due to the low elastic modulus of Al and very little strain hardening effect of Al, the rupture strength of AlN ceramic might be never reached. This explained why there was no delamination of Al from AlN baseplate ever observed during temperature cycling, while most of AlN-DBC samples failed at around 20 - 40 cycles. Similar result, shown in Figure 3.17, was obtained by L. Dupont *et. al.* [118].



(a)



(b)

Figure 3.16. Von Mises stress in AlN ceramic during temperature cycling (a) AlN-DBC and (b) AlN-DBA.

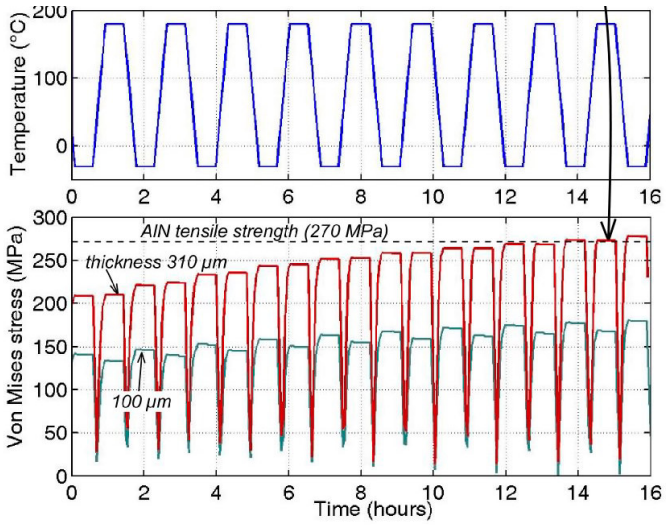
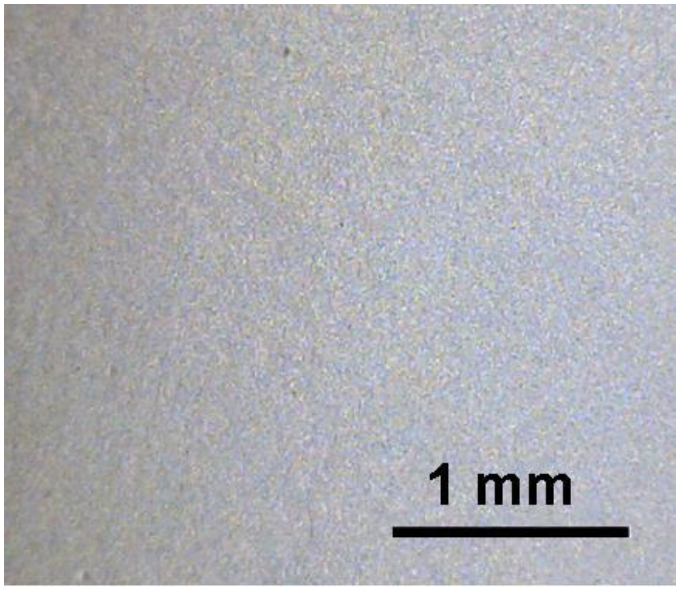


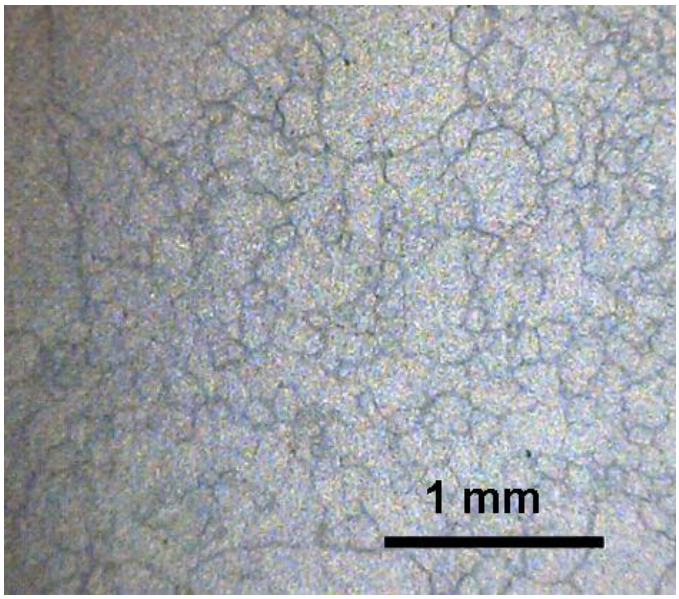
Figure 3.17. Von Mises stress in ceramic during temperature cycling [118].

3.3.4. Surface Roughening of Aluminum

Delamination of aluminum from the ceramic baseplate was not observed for up to 1500 temperature cycles, but DBA underwent a surface roughening problem. Increased surface roughness of aluminum was observed after about 150 temperature cycles, and became more severe as the thermal cycling continues. Figure 3.18 shows the SEM image of a DBA substrate after temperature cycling. It was clear that there was no feature and pattern could be seen on the DBA surface without temperature cycling. However, after 100 temperature cycles, some irregular features were shown, which most likely depicted the grain pattern of aluminum. When more temperature cycling was applied to sample, aluminum surface became rougher and rougher. Although there was no direct observation that those roughened sites were located at the grain boundaries of aluminum, it was believed that the grain boundary movement of aluminum under massive thermomechanical stresses was the main reason that caused the surface roughening effect of aluminum.



(a)



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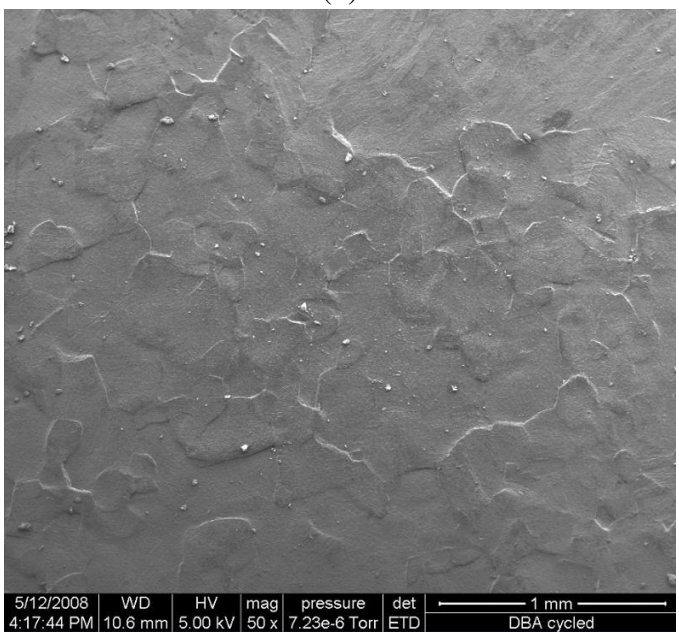


(c)

Figure 3.18. SEM images of DBA substrate after (a) 0 cycles, (b) 100 cycles, and (c) 300 cycles.

Figure 3.19 shows the results of DBA surface roughness measurements using a Dektak® profilometer. The standard deviation of the measurements was calculated and was used to represent the substrate surface roughness. While the surface roughness of the DBA before thermal cycling was 0.68 μm, it was then increased to 7.08 μm after 300 cycles, a more than 10 times increase.

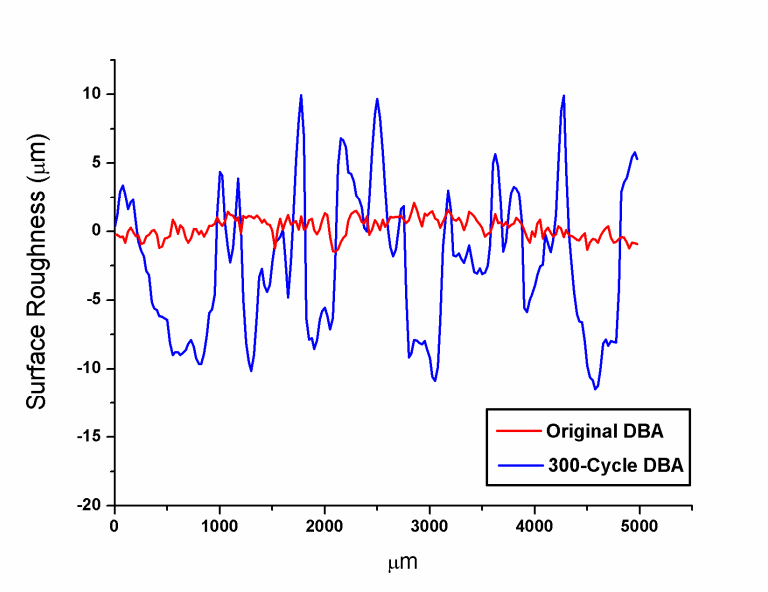


Figure 3.19. Surface roughness of DBA substrate after 300 temperature cycles.

This phenomenon was believed due to the massive thermomechanical stresses induced during temperature cycling. The relatively low melting point of aluminum (660 ^{o}C) and the large CTE of aluminum (24 ppm/K) made the effect of thermomechanical stresses on aluminum more profound in high temperature regime. In the high temperature regime of the cycling, while the temperature got close to the annealing temperature of aluminum, ranging from 200 ^{o}C to 400 ^{o}C, plastic deformation would occur, induced high level of recrystallization and grain-boundary rotation, thus resulted in drastic microstructural evolution. Deformed grains were replaced by a new set of un-deformed grains that nucleated and grew until the original grains had been entirely consumed. The internal thermomechanical stress caused by the CTE mismatch between aluminum and ceramic base-plate could be therefore released to some extent. However, as a side effect of this stress releasing process, the aluminum surface became rougher with increased thermal cycling number.

Similar to the DBA substrate with only the aluminum metallization, samples' surfaces with electroless-plated nickel or electro-plated nickel and then silver

metallization also became rougher during the thermal cycling test. Figure 3.20 shows the optical microscopic image of a cycled DBA substrate with electroless nickel metallization , the image interposes in the upper-left corner was an overall view of the cycled DBA substrate. Reported in [118], cracks were observed in the nickel layer. The river-pattern cracks of 5 to 6 μm in width started to show after 150 cycles.

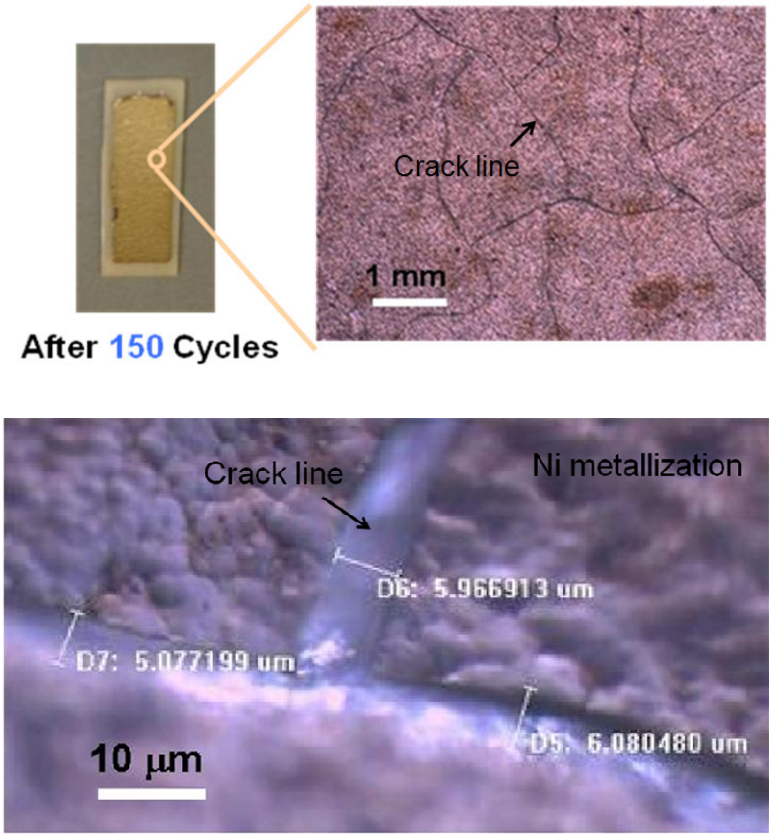


Figure 3.20. Optical microscopic image of cycled DBA substrate with electroless nickel metallization (after 150 thermal cycles).

Figure 3.21 shows the surface roughness measurement results of DBA substrates with different materials as metallization. While all the samples showed increased surface roughness during the thermal cycling, it was noticed that the samples with electroless-plated nickel and the samples with electro-plated nickel and then silver possessed a smoother surface than the samples with only the

aluminum metallization. It was believed that the plated nickel layer played an important role against the deformation caused by the aluminum. With high melting point, 1455 ^{o}C, no significant microstructural evolution could be induced in the nickel during the cycling. Therefore the stress-releasing deformation of nickel layer was much smaller than the aluminum. Secondly, the higher elastic modulus and hardness of nickel than aluminum made the nickel plating capable of constraining the aluminum layer to some extent. Although this constraining mechanism cannot hold after the nickel layer started to crack, it delayed the surface from getting rougher. Given that the sample with electro-plated nickel had thicker nickel layer than the sample with electroless-plated nickel, this constraining mechanism was more reasonable, and the surface was smoother at any given cycling number.

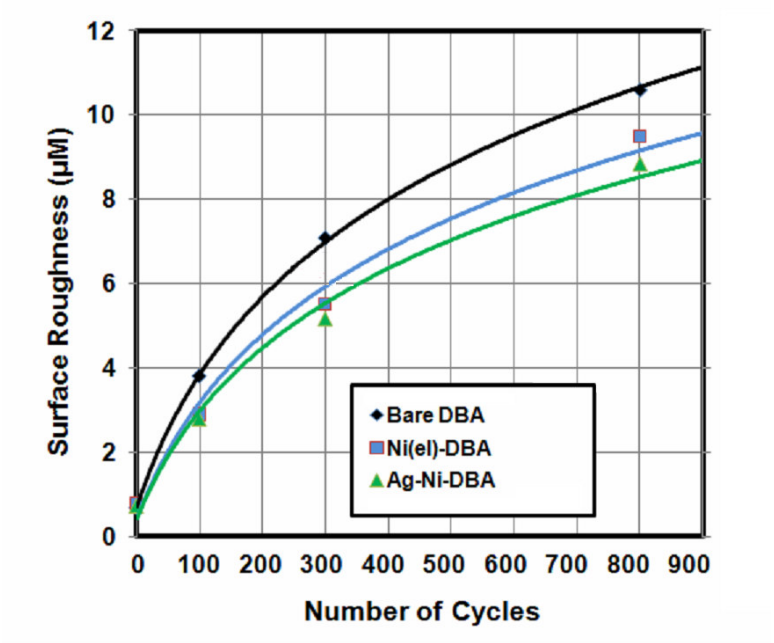


Figure 3.21. Surface roughness of cycled DBA substrate with different type of metallization layers.

3.3.5. Microstructure Evolution of Aluminum

Due to the CTE mismatch between the aluminum layer and the ceramic base-plate, thermomechanical stress did build up along the aluminum-ceramic

interface, as well as inside the bulk aluminum layer, during the thermal cycling test. And given the fact that the DBA surface became rougher after the cycling, it was important to investigate the aluminum microstructure. Microstructure evolution of aluminum was characterized by scanning electron microscopy (SEM) and electron backscattered diffraction (EBSD). By understanding the physical mechanism(s) that caused the aluminum roughening effect, methods can be taken to increase the resistance of aluminum against the massive thermomechanical stress. Figure 3.22 shows a SEM image of a DBA substrate after 800 thermal cycles. Tremendous amount of voids can be found in the aluminum layer, ranging from sub-micron to several micronmeters. Although it was possible to introduce some relatively larger voids and scratches by polishing during the sample preparation, as can be identified in the SEM image, the smaller voids were still considered not caused by the sample preparation.

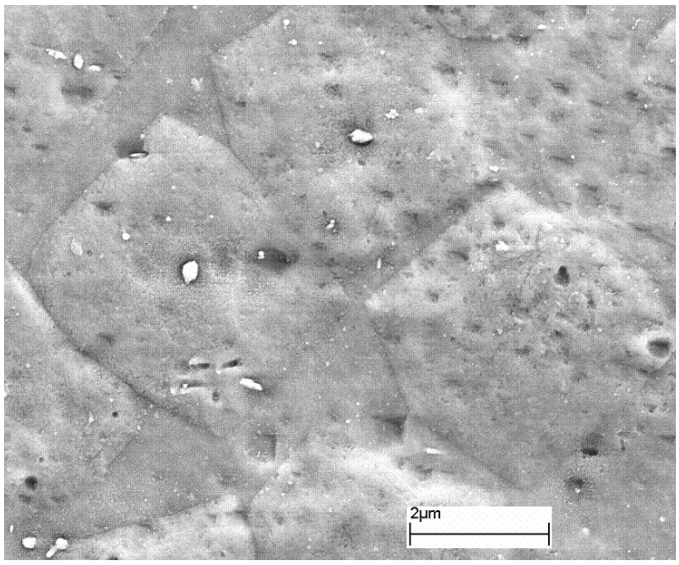


Figure 3.22. SEM image of a temperature cycled DBA substrate (800 cycles).

Three aluminum grains can be easily identified from the SEM image. While two of them are closely aligned along the grain boundary, the third grain, the one on the right lower side, was detached from the grain boundary. It was believed that the mechanism of causing the separation of grains along the grain boundary

involved grain-boundary sliding [119,120] which occurred under action of shear stresses acting on the boundaries. And because it was an energy driven process, grain-boundary sliding became more active with increased temperature. Figure 3.23 shows a schematic of the formation of voids due to grain-boundary sliding. With accumulated voids, microstructural deformation would happen, and eventually resulted in roughening of the aluminum surface.

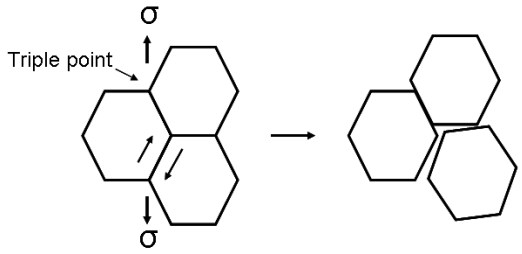


Figure 3.23. Schematic of the formation of voids due to grain-boundary sliding.

Figure 3.24 shows an optical image of one DBA sample after temperature cycling. It was noticed that the roughening effect was highly anisotropic, this random thickening of the aluminum layer took place as mass was locally "piled-up" during the heating cycle. The formation of roughened aluminum was not reversible, since more and more roughened surface was observed after continuous temperature cycling. The stress levels in these less thickened regions might be considerably higher than the remaining films.

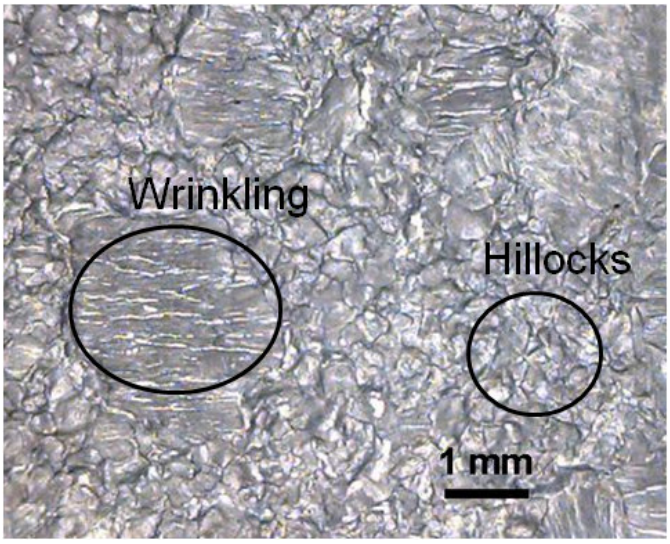
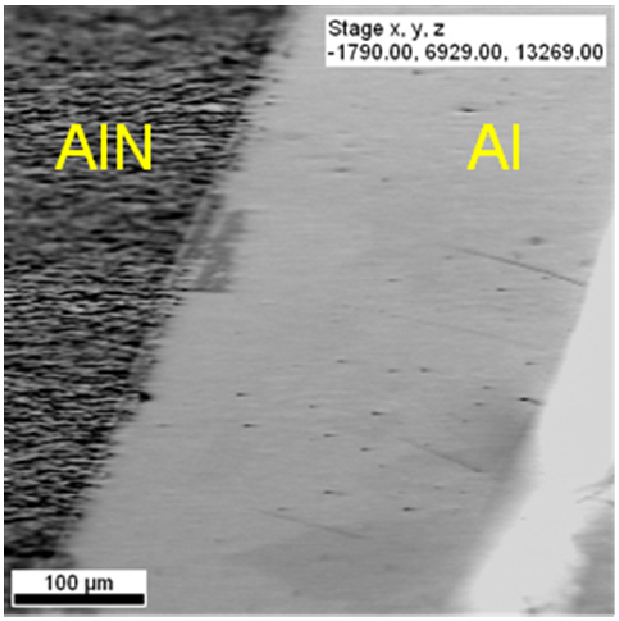


Figure 3.24. Optical image of a DBA sample after temperature cycling.

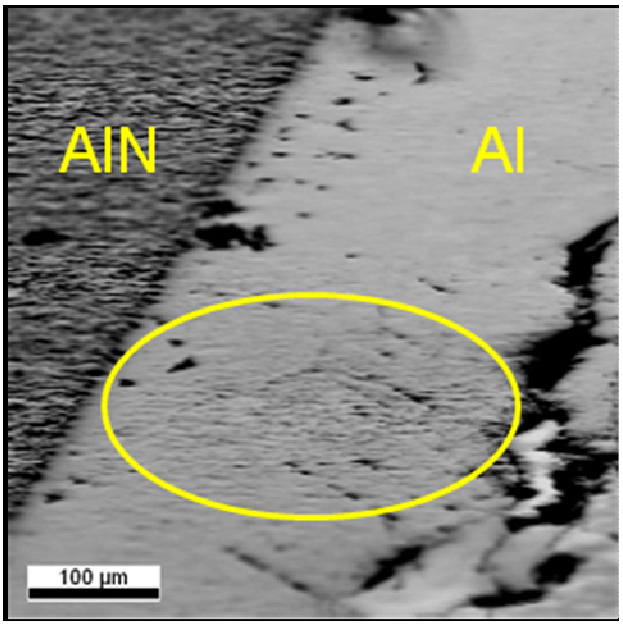
To further understand the mechanism(s) that caused the aluminum layer to roughen. EBSD was employed to characterize the changes/evolutions in the grain structure of aluminum. For EBSD characterization, the overall requirement of sample preparation was much higher than that for normal SEM characterization. After the sample was polished with 9, 5, 1, 0.3, and 0.05 μm of diamond powder, an up to 2 hours' final polish was done in a vibration polisher. Sample was immersed in a suspension of colloidal silica with particle size of 0.05 μm. The silica suspension not only polished the sample by mechanical striking the surface, but also chemically removed the roughened region by slow etching.

Figure 3.25 shows two SEM images of the DBA samples before and after temperature cycling. Figure 3.25(a) shows a DBA sample before temperature cycling. No obvious patterns, scratches, and voids can be found from the polished surface. While Figure 3.25(b) shows a DBA sample after temperature cycling. The polished surface was much more defective than the sample without temperature cycling. In addition to the pores close to the Al-AlN interface, some regions were found to have rippling effects. EBSD analysis was done on these regions and reveals the significant change of the grain structure of aluminum after temperature cycling.

Figure 3.26 shows the grain patterns of the different regions of a DBA sample without temperature cycling. It is clear that before temperature cycling, the grain size of aluminum is ranging from 50 to 500 μm. Figure 3.26(b) shows the confidential level map of Figure 3.26(a) region, with blue lines illustrated the regions with non-identified grain orientation. In addition to the grain boundaries, some straight lines were also shown in blue color that was believed representing the scratches due to polishing.

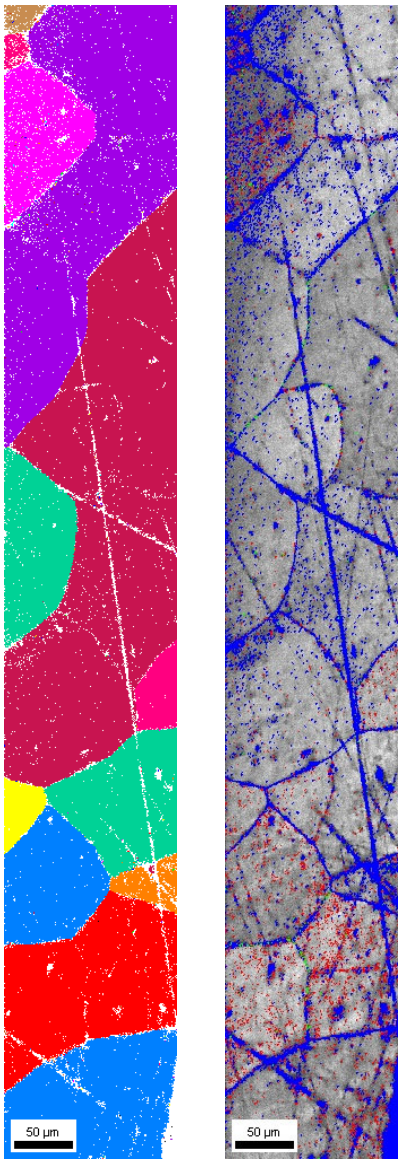


(a)



(b)

Figure 3.25. SEM images of DBA sample (a) before temperature cycling, and (b) after temperature cycling (800 cycles).

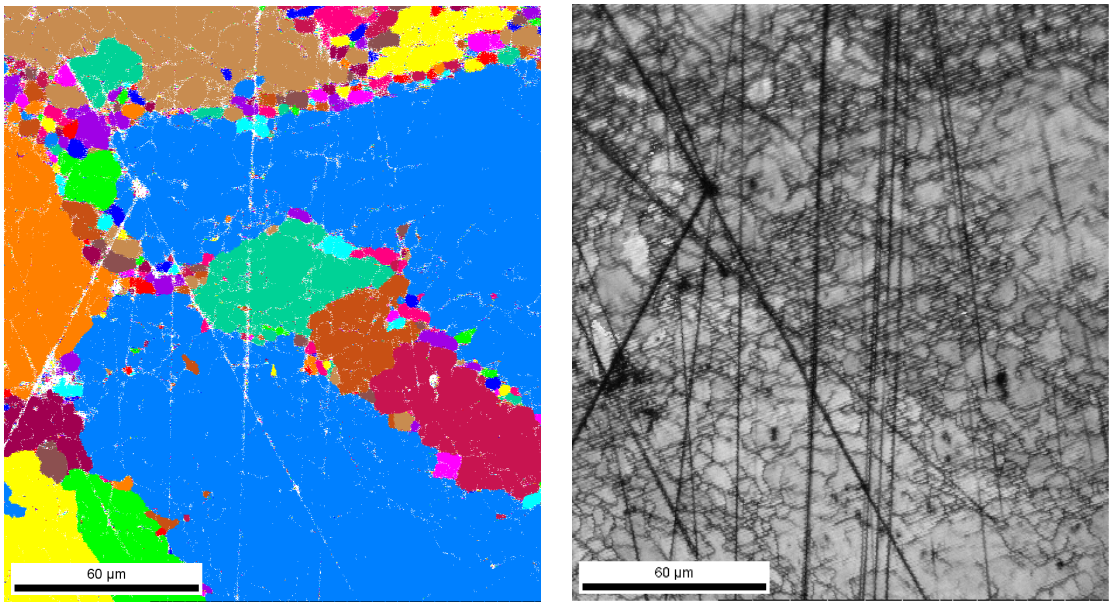


(a) (b)

Figure 3.26. Grain pattern of aluminum without temperature cycling (a) EBSD grain pattern of aluminum, and (b) confidential map of aluminum grain pattern.

Figure 3.27 shows the grain patterns of a DBA sample after temperature cycling. Different from the images shown in Figure 3.26, many small grains of less than 5 µm can be found in the EBSD pattern. Based on the size and the location of these small grains, it was believed that they were new grains either formed within the existing large grains, or formed along the grain boundaries. Figure 3.27(b) shows the orientation map of the grains in the same region. Grey regions

stood for area with clearly defined orientation, whereas black lines stood for regions with uncertain orientation. Compare two images, it can be seen that not only the grain boundaries showed undefined orientation, but also many sites within the large grains appeared to have non-determined orientation. Aluminum was supposed to undergoing significant recrystallization and recovery during temperature cycling.



(a) (b)

Figure 3.27. Grain pattern of aluminum after temperature cycling (after 800 cycles) (a) EBSD grain pattern of aluminum, and (b) confidential map of aluminum grain pattern.

Figure 3.28 shows the Ashby's deformation-mechanism map [121] of aluminum. It is clear that at 250 ^{o}C (523 K), 0.56T_M of aluminum, when shear stress reached 1MPa, aluminum would undergo creep deformation. When shear stress was slightly above 10 MPa, aluminum would suffer plastic deformation, tremendous recrystallization would happen at this temperature.

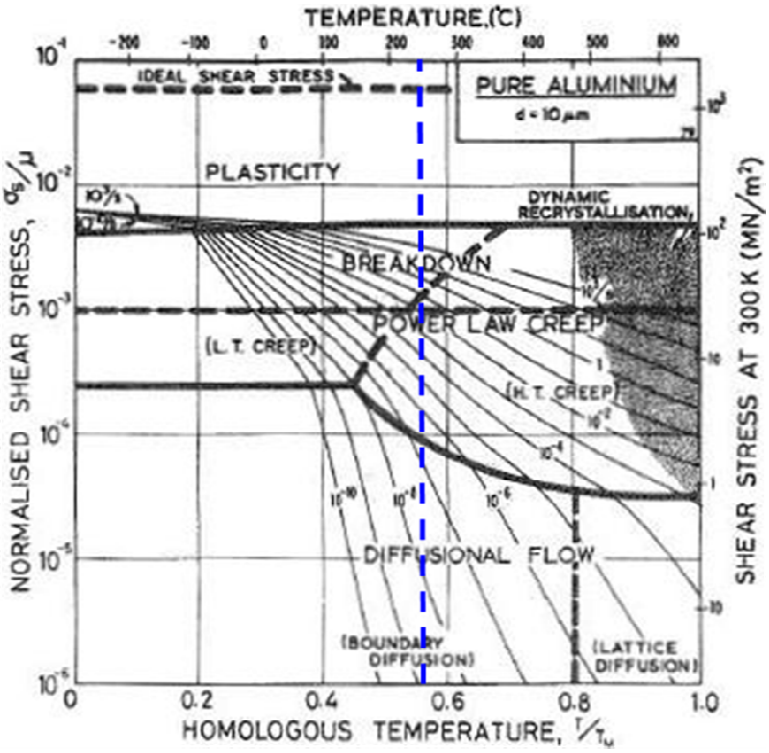


Figure 3.28. Deformation-mechanism map of aluminum [121].

During temperature cycling process, aluminum was under tremendous thermomechanical stress due to CTE mismatch of aluminum and aluminum nitride baseplate. Therefore, aluminum was likely to deform plastically, and excess line defects (dislocations) and some excess point defects were introduced into the bulk aluminum. At high temperature, the density of these excess defects can be reduced by means of annealing, which typically included recovery, recrystallization, and grain growth. During the recrystallization process, aluminum atoms had to move from one lattice arrangement in the deformed region into a new and more perfect one. By introducing more nucleation site and more grains with different orientations, thermomechanical stresses in the bulk aluminum can be effectively reduced. However, consider the situation when aluminum was exposed to air, a thin protective oxide layer would form on the surface. This oxide layer may hinder diffusional creep processes that tend to relieve any externally induced stresses in the film. These stresses can then be reduced by the formation

of hillocks under the oxide [122,123] or on top of the oxide where it was broken or defective [124], shown in Figure 3.29.

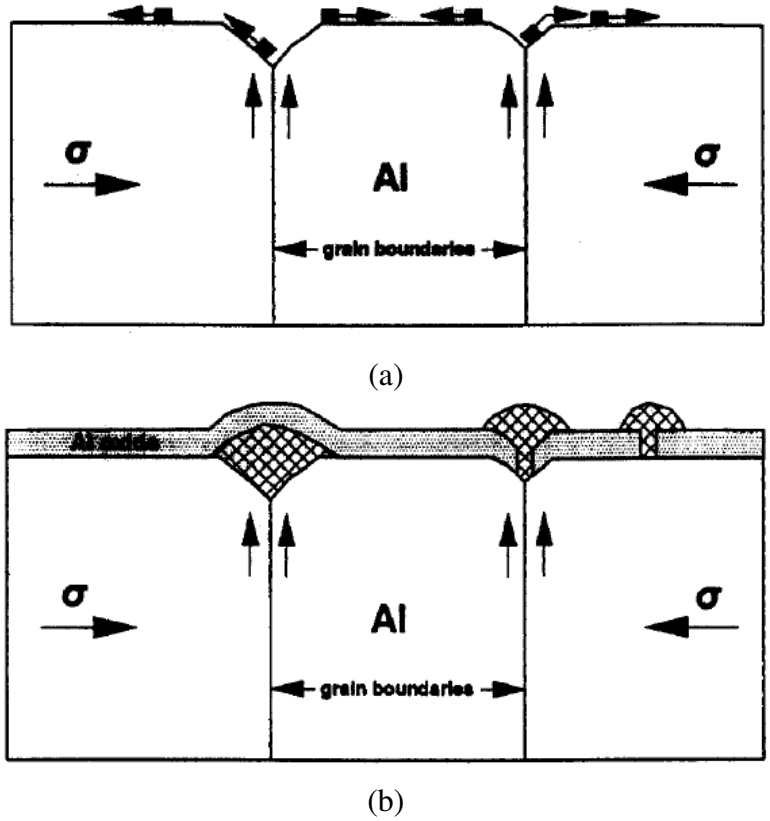
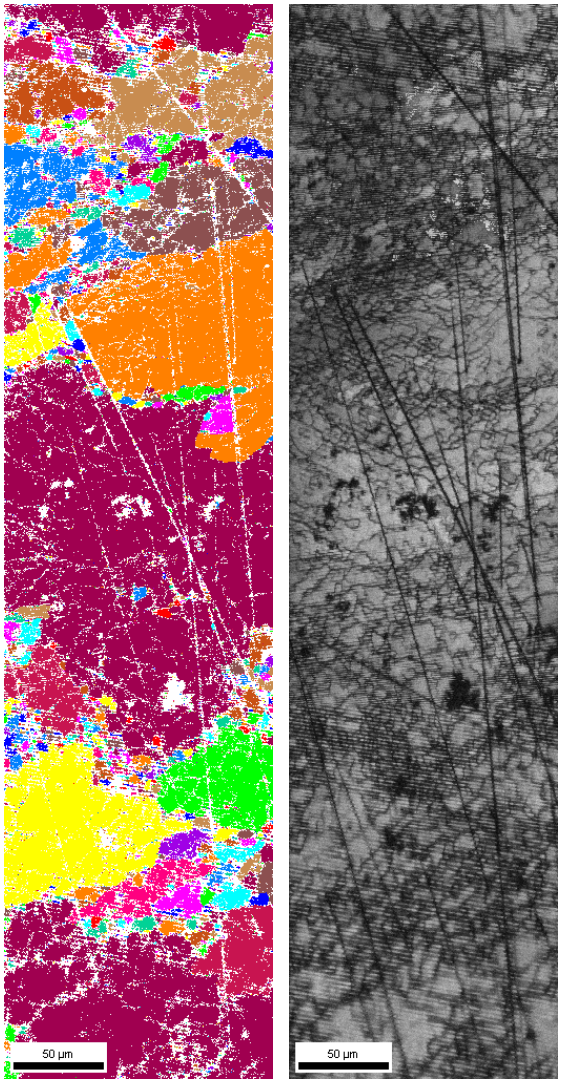


Figure 3.29. Models for atoms diffusion when aluminum is subjected to compressive stress: (a) no surface oxide layer, and (b) with surface oxide layer [124].

The surface oxide appeared to be very flexible and hillocks would be expected to form preferentially under the oxide at locations such as grain boundaries, where out-diffusion was most rapid. This mechanism also explains why electroplating of Ni & Ag on top of Al surface would help delaying the surface roughening of Al. The Ni & Ag plating layer protected Al from oxidation, and because the CTE mismatch of Al to Al_2O_3 was larger than that of Al to Ni or Al to Ag, thermomechanically induced compressive stress at the Ni-Al interface was smaller than that of Al_2O_3-Al interface, therefore less hillocks can be formed.

Another phenomenon can be observed from the EBSD analysis was the paralleled line region with undefined orientation, shown in Figure 3.30. In Figure

3.30(b), it is easy to identify regions with paralleled lines with different line density and direction.



(a) (b)

Figure 3.30. Grain pattern of aluminum after temperature cycling (a) EBSD grain pattern of aluminum, and (b) confidential map of aluminum grain pattern..

These parallel lines further proved that those regions were once belonging to one big grain with defined orientation. These lines would result when grains were suitably oriented with respect to the applied stress. Wrinkling would occur in those grains that contain shear planes which experienced a maximum resolved shear stress greater than the critical resolved shear stress for plastic flow on that plane, shown in Figure 3.31 [125]. Once more than one place being oriented in such a

way, as to experience nearly the same resolved shear stress, then multiple slip would occur resulting in the cross patterns seen in some grains in Figure 3.24.

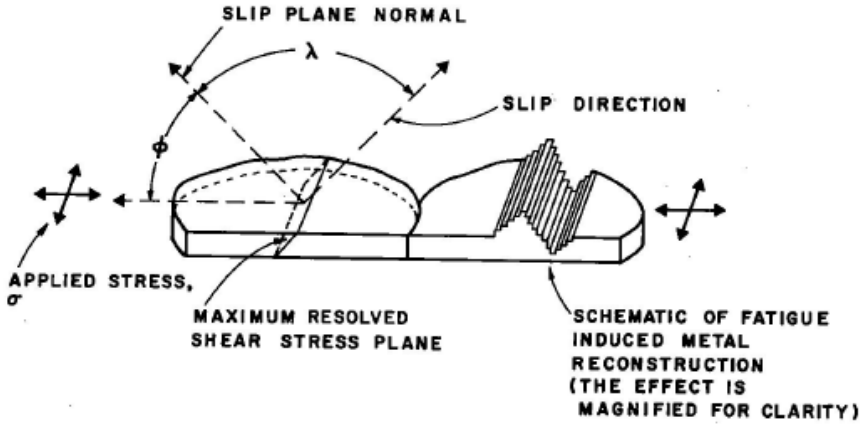


Figure 3.31. Critical resolved shear stress for plastic flow [125].

3.4. Summary of DBA Thermomechanical Reliability

The reliability of DBA substrate under the condition of large range thermal cycling (-55 ^{o}C to 250 ^{o}C) was studied. Due to the low elastic modulus of aluminum and less strain hardening of aluminum, thermomechanical stress induced at the Al-AlN interface was much less than that of DBC substrate, no delamination of aluminum from ceramic base-plate was observed for up to 1500 thermal cycles.

However, the aluminum surface was found to be roughened after the cycling test, which could be the biggest obstacle for DBA to be used for high-temperature electronics packaging. Based on microstructure characterization of temperature cycling DBA, significant recrystallization was observed. It is believed that, for aluminum with small grains, at high temperature (250 ^{o}C), under tremendous thermomechanical stress, hillocks would form on the aluminum surface as a means to relieve the compressive stresses, especially at grain boundaries. It is also observed that by metalizing aluminum with Ni and Ag would help delaying the formation of hillocks, which can also be explained by the stress relieving theory. For some of the large size grains, as they were under recrystallization and

recovery processes, they were firstly broke into many small grains, and then continue to undergo the formation of hillocks. For some other large grains that were suitably aligned to the applied stress, wrinkling would occur in those grains that contain shear planes which experienced a maximum resolved shear stress greater than the critical resolved shear stress for plastic flow on that plane. Therefore in a temperature cycled DBA substrate, the typical pattern on the aluminum would be the combination of many small hillocks randomly distributed on the surface, and a few wrinkling patterns with mostly paralleled striations.

Chapter 4. THERMOMECHANICAL RELIABILITY OF LOW-TEMPERATURE SINTERED ATTACHMENTS ON DIRECT BONDED ALUMINUM SUBSTRATE

4.1. Introduction

Substrate features, such as flatness, roughness, surface metallization, and contamination, have a great impact on the die-attach materials. Depending on the type of die-attach material, different substrate features have different levels of influence. In this study, as the surface roughening of DBA substrate had been observed in the accelerate temperature cycling test, the effect of DBA surface roughness on the die-attach shear strength was investigated. Due to its unique feature of processing at low-temperatures, while it could reliably be used at high-temperatures, nanoscale silver paste was used as the die-attach material. Another reason that nanoscale silver paste was selected was attributed to its low Young's modulus which was measured to be only about 9 GPa. This Young's modulus value - lower than almost all the solder alloys – allowed the sintered silver layer to be more compliant under stress. Therefore it was expected that under the influence of surface roughening, the die-attach bonding strength of sintered silver would probably suffer much less than most other materials. In addition to mechanical bonding strength, other properties like thermal conductivity and electrical conductivity are often more close to specific applications and are theoretically more sensitive to the microstructural change of the die-attach material. In this study, large-area devices were attached to the DBA substrate using a low-temperature sintered silver joint. The attachments were then thermally cycled between -55 ^{o}C and 250 ^{o}C to accelerate failure in both the

sintered silver and DBA substrate. The cross-section of the attachment was characterized by SEM.

4.2. Experimental Procedure

DBA substrate had been metallized with nickel and silver to be compatibility with sintering of nanoscale silver paste. Small devices, 3 x 3 mm^2, were used to characterize the bonding strength of the sintered silver during temperature cycling. On the other hand, 10 x 10 mm^2 silicon dummy devices were used to characterize the microstructural change of the sintered silver for large-area attachment. All the assemblies were then being temperature cycled between -55 ^oC and 250 ^oC for up to 800 cycles. Figure 4.1 shows one typical large-area sample for temperature cycling.

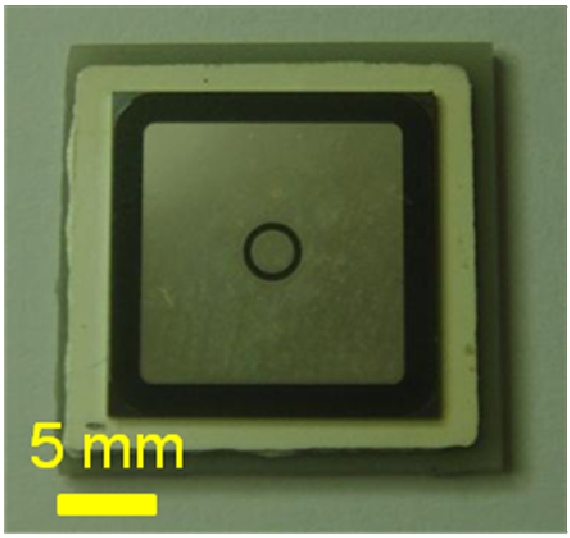


Figure 4.1. Large-area silicon device attached on DBA substrate for temperature cycling test.

4.2.1. Die-attachment Shear Strength on Roughened DBA

Two sets of testing were done to investigate the effect of DBA surface roughness on the die-shear strength. The first experiment was done by applying nanoscale silver paste directly on a surface roughened DBA, then mount the

devices and sintered the silver paste, to quantify the die-shear strength of sintered silver on an already roughened substrate.

DBA substrates used in this test were the ones already being temperature cycled. As introduced in Section 3.2.6, the surface roughness of DBA would increase as increasing the number of temperature cycles. Therefore, bare-aluminum DBA samples with 0, 100, 300, and 800 cycles were used. After the samples were taken out of the cycling chamber, they were later cleaned to take off the surface contamination caused by the cycling chamber, and then properly metallized by zincating and following electroplating of nickel and silver. The metallization layer was applied after the temperature cycling for the purpose of minimizing the detachment of metallization layer off the substrate aluminum. Average 10 pieces of mechanical devices were attached to the roughened DBA substrate by low-temperature sintering of nanoscale silver paste, and the corresponding die-shear strength was also measured.

4.2.2. Accelerated Temperature Cycling of Sintered Silver on DBA

The second experiment was done by simulating the real conditions in real applications. DBA substrates were metallized at the very beginning of the test, and mechanical devices were then attached to the flat, smooth DBA substrate by using nanoscale silver paste. After the die-attachments were assembled, all the testing samples were placed in the temperature cycling chamber for the thermomechanical reliability test. Not only the DBA substrate would undergo surface roughening issue, the die-attach material, sintered silver, would also suffer the microstructural change, which typically degraded the die-attachment performance. However, since this was more close to the real application, the testing results were supposed to be more meaningful than the first experiment.

4.2.3. Reliability of Large-Area Device Attachment on DBA

Large-area silicon devices, 10 x 10 mm^2, were attached on DBA substrate using low-temperature sintering of silver technology. Similar to the test method in Section 4.2.2, after the sintering was finished, all the assemblies were placed in the temperature cycling chamber for the thermomechanical reliability test. The attachments would be examined by SEM after certain number of cycles. Microstructural change of the sintered silver was characterized.

4.3. Experimental Results and Discussion

4.3.1. Die-attachment Shear Strength versus Substrate Roughness

Figure 4.2 shows the relation of measured die-shear strength versus DBA surface roughness. Because the original smooth DBA substrate did not go through the temperature cycling, the average die-shear strength of sintered silver was about 32 MPa.

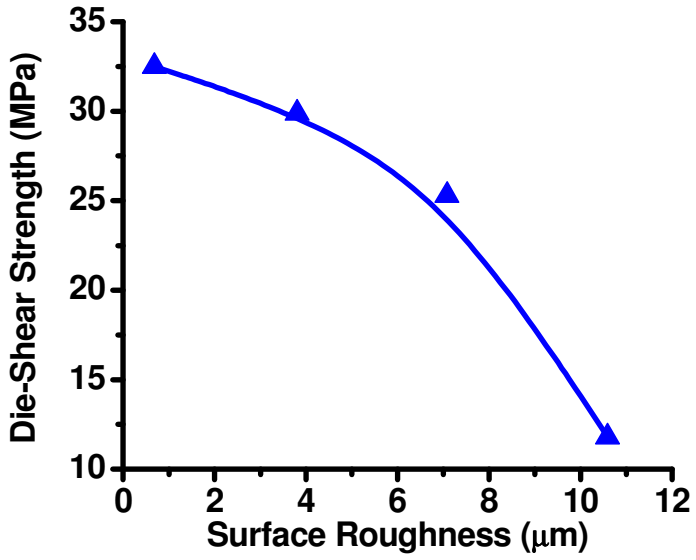


Figure 4.2. Die-attach strength versus DBA surface roughness.

However, as the substrate roughness was increased to 4, 7, and almost 11 μm, the average die-shear strength dropped tremendously. This was expected

because the bond-line thickness of the sintered silver was only about 20 µm. Although the sintered silver was believed and measured to be “soft”, 7 and 11 µm thickness changed would corresponding to 33% and almost 50% of the overall bond-line thickness, which was considered out of the tolerance of the sintered silver.

4.3.2. Reliability of Sintered Silver on Roughening DBA

Figure 4.3 shows the measured die-attach shear strength versus number of temperature cycles. The previously measured DBA surface roughness was also plotted for the purpose of comparison.

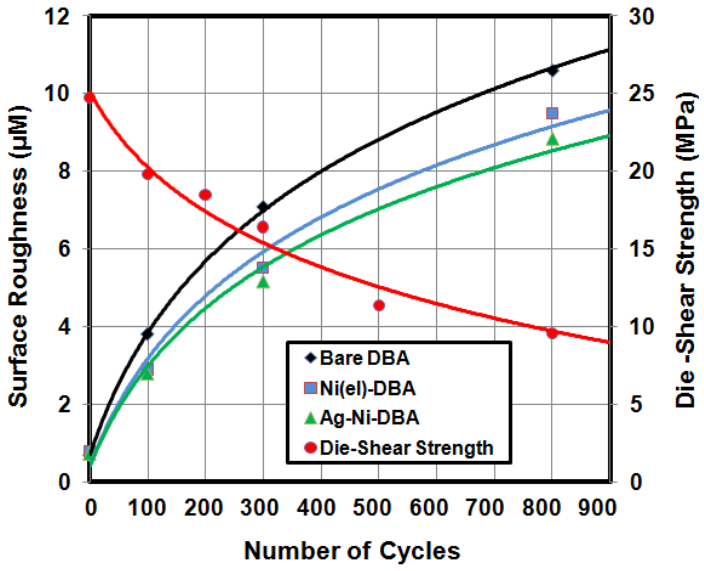


Figure 4.3. Die-shear strength of sintered silver versus number of temperature cycles.

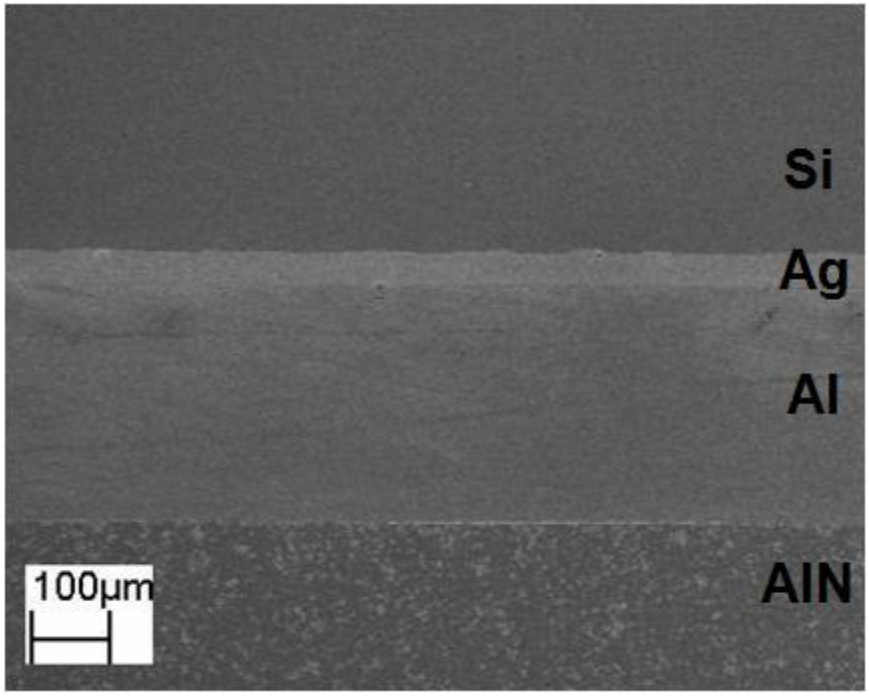
As expected, the die-shear strength dropped tremendously after the temperature cycling. It was believed that not only the DBA roughening would cause the die-attach material to have lower bonding strength, the sintered silver itself would also suffer the microstructural change, and as a consequence degraded the mechanical performance.

Compare the results of sintered silver in Figure 4.2 and Figure 4.3, similar die-shear strength can be found after 800 temperature cycles. When the

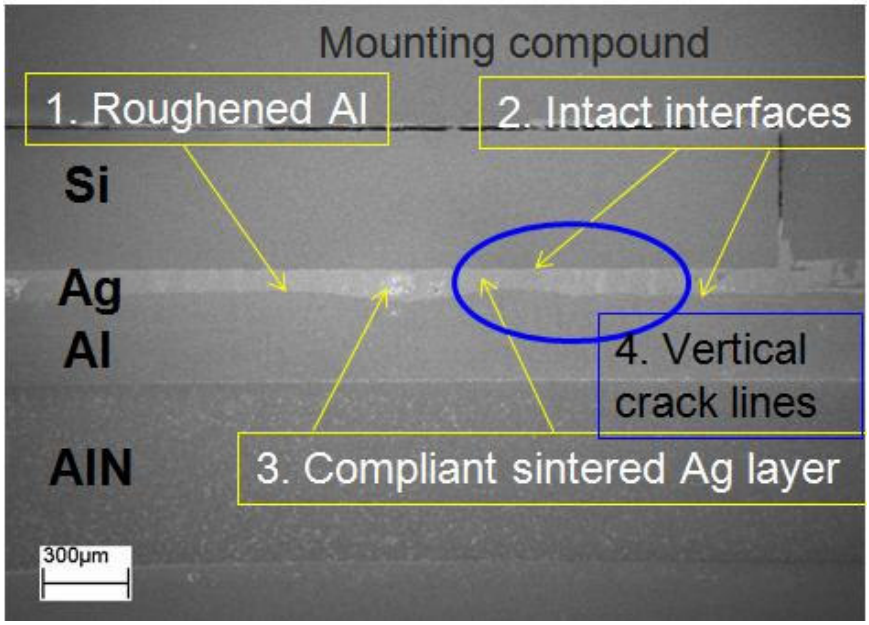
roughness of DBA reached about 10 μm and attach device later, the average die-shear strength was about 11.5 MPa; whereas when attach the device before temperature cycling and measure the die-shear strength later, the average strength obtained was around 10 MPa. This observation suggested that the microstructural change of sintered silver did not contribute much to the degradation of die-shear strength.

4.3.3. Reliability of Large-Area Sintered Silver on Roughening DBA

Large-area device attachments had been cycled in cycling chamber for up to 800 cycles. Figure 4.4 shows the cross-sectional SEM images of large-area attached samples before and after temperature cycling.



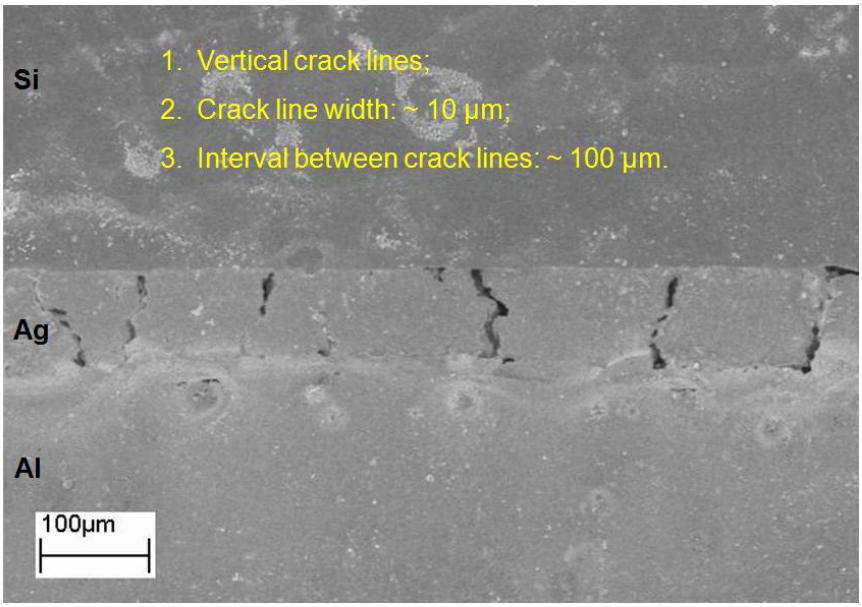
(a)



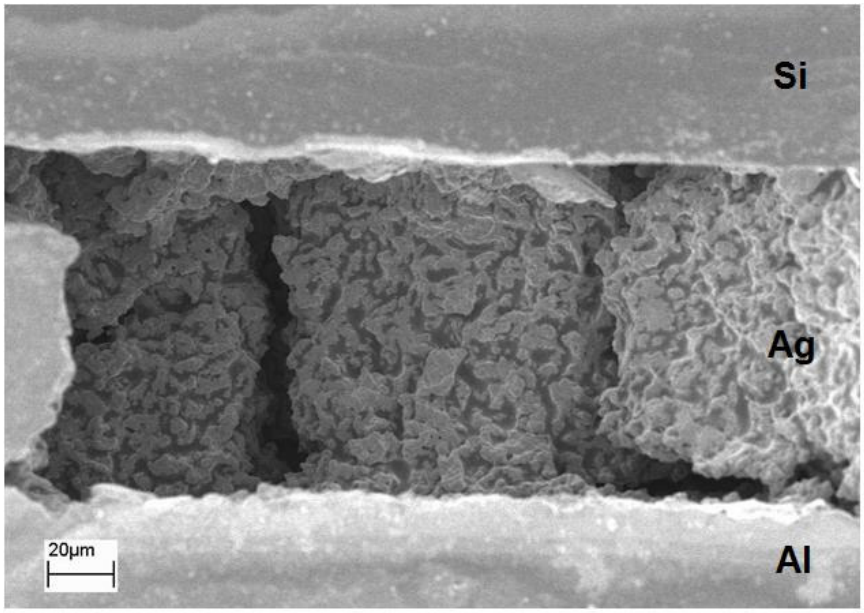
(b)

Figure 4.4. Cross-sectional SEM of large-area attachment for temperature cycling (a) before temperature cycling, and (b) after 800 temperature cycles.

Some features can be found from the sample after temperature cycling: (1) aluminum surface of DBA substrate got roughened, as discussed in Chapter 3; (2) the device-to-silver and silver-to-substrate interfaces remained intact even after cycling, no obvious horizontal cracks along the interfaces were observed; (3) sintered silver deformed with the roughened aluminum. Due to its porous structure and low elastic modulus, sintered silver was supposed to be very compliant to thermomechanical stresses; and (4) some vertical cracks in the sintered silver layer were found after temperature cycling. Images with higher magnification are shown in Figure 4.5.



(a)



(b)

Figure 4.5. Cross-sectional SEM of large-area attachment for temperature cycling (a) vertical crack lines, and (b) representative of 3D vertical crack lines.

Figure 4.5(a) shows some representative vertical cracks in the sintered silver layer after temperature cycling. The vertical cracks appeared to be periodical with the width of the crack lines of 10 µm and the width of the silver column was around 100 µm. Furthermore, during the sample preparation process, a small

piece of sintered silver was peeled off from the attachment layer by polishing, from which provided us a chance to characterize the features of the sintered silver underneath. Not surprisingly, vertical cracks were also found in the exposed underneath silver, and the width of the crack lines was also around 10 μm. Therefore, it was concluded that the vertical crack lines were truly the 3D characteristics of the sintered silver after temperature cycling.

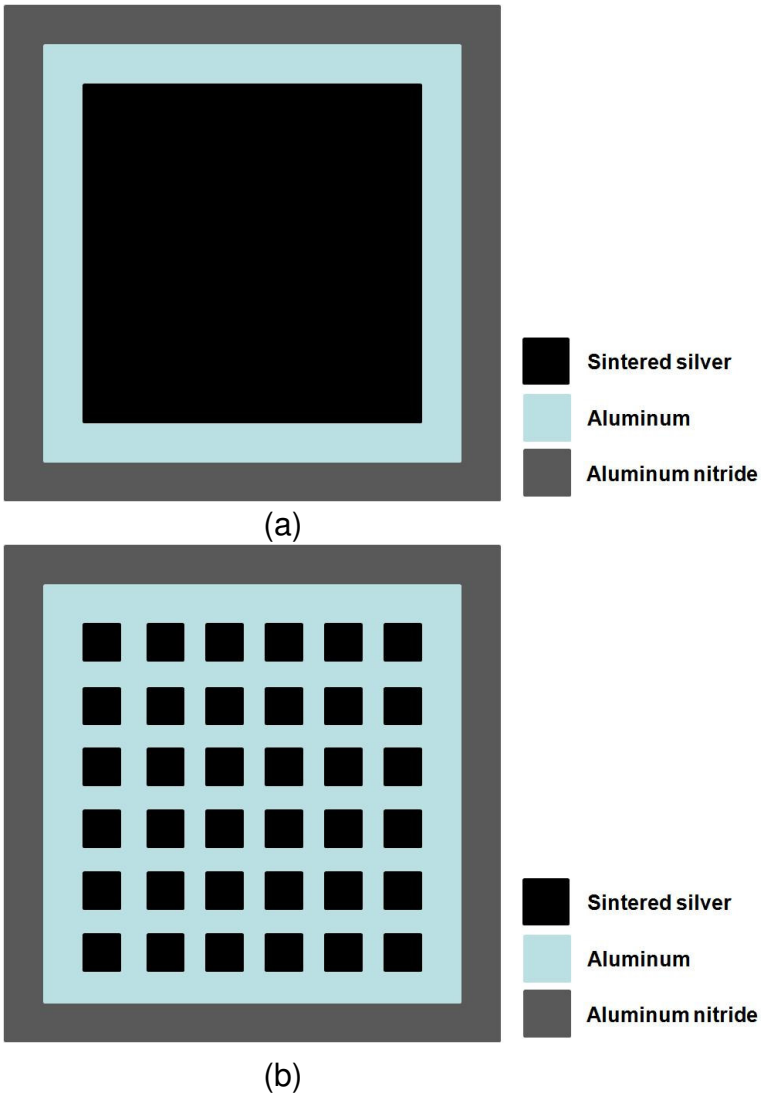
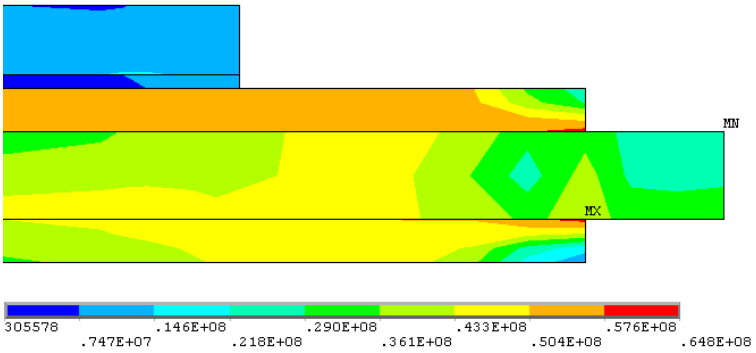


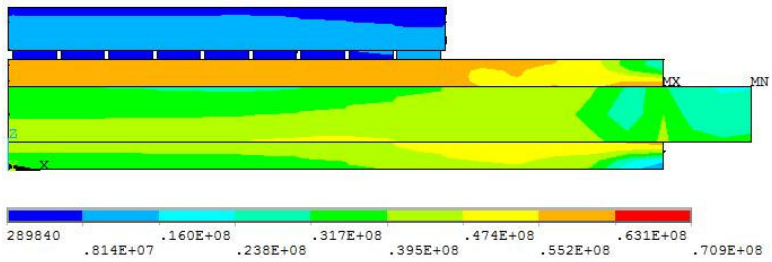
Figure 4.6. Schematic of large-area attachment on DBA using sintering of nanoscale silver paste (a) before temperature cycling, and (b) after temperature cycling (with vertical cracks).

Figure 4.6 shows the schematic of large-area attachment on DBA substrate using sintered silver before and after temperature cycling. As proposed in the last

paragraph, the sintered silver was highly likely to show the grid pattern after temperature cycling. Finite element analysis had also been utilized to compare the stress and strain level of the two attachment features, and is shown in Figure 4.7. The simulation predicted the stress of the assembly after 50 temperature cycles, and was showing the stress when temperature came back to room temperature, 25 ^{o}C.



(a)



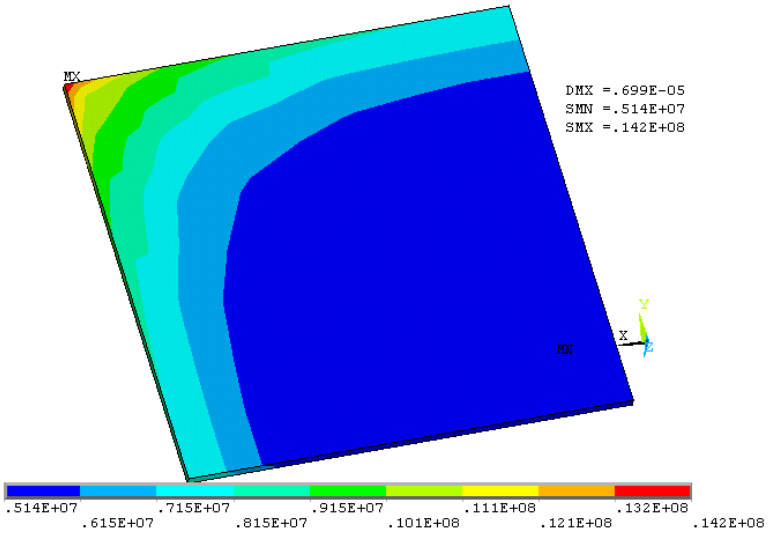
(b)

Figure 4.7. Finite element simulation of stress of assembly at 25^{o}C (a) Continue silver attachment, and (b) Sintered silver with grid pattern.

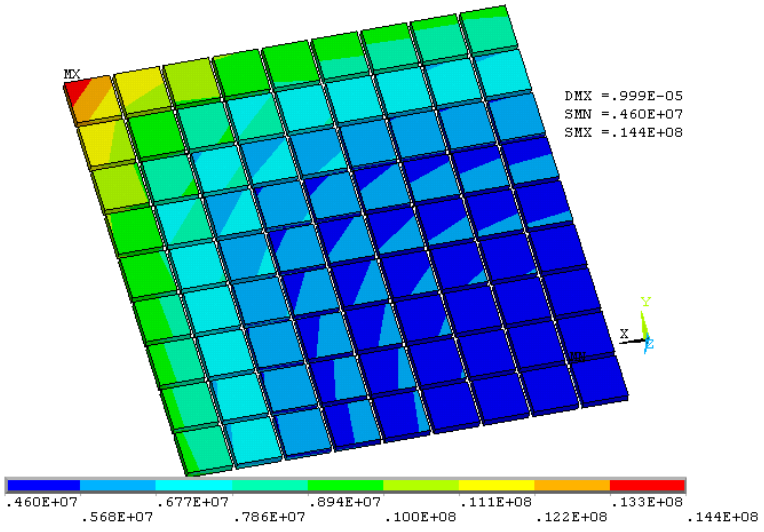
From the stress distribution figures, it is clear that the when the sintered silver shows grid pattern, the stress at the outer layer of silver was compatible to that of without grid pattern. However, if the grid pattern was shown in the silver layer, the stress cannot be effectively transferred to the inner layer of silver, made the inner layer subjected to lower stress. On the contrary, if the silver layer was a complete piece, the stress can be transferred into the inner layer. And once there was a

horizontal crack formed in the silver layer, it was able to penetrate into the inner layer without too much difficulty, since the silver layer was continuous.

With regard to the stress distribution at lower temperature (-55 ^{o}C), simulation results showed that the structure with grid-pattern was able to generate less stress at the outer layer of silver than that of one continuous piece structure, as shown in Figure 4.8.

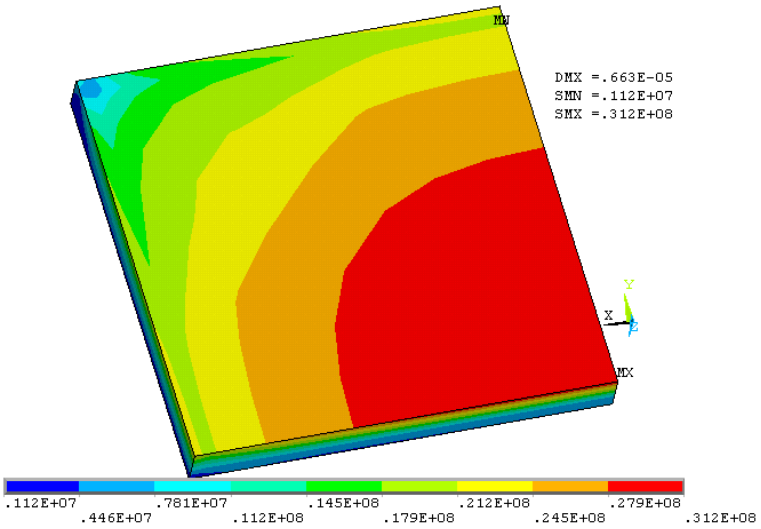


(a)

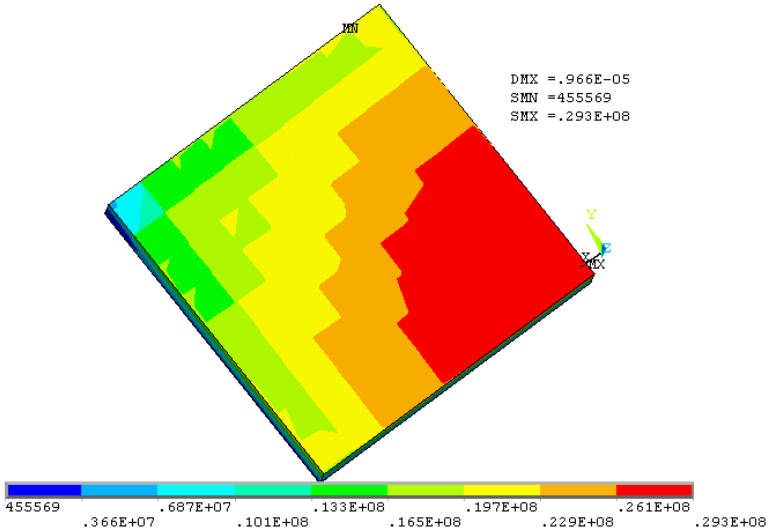


(b)

Figure 4.8. Finite element simulation of stress in the silver layer at -55 ^{o}C (a) continue silver attachment, and (b) sintered silver with grid pattern.



(a)

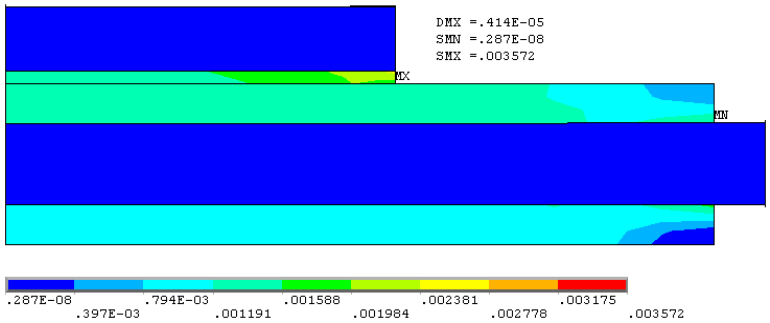


(b)

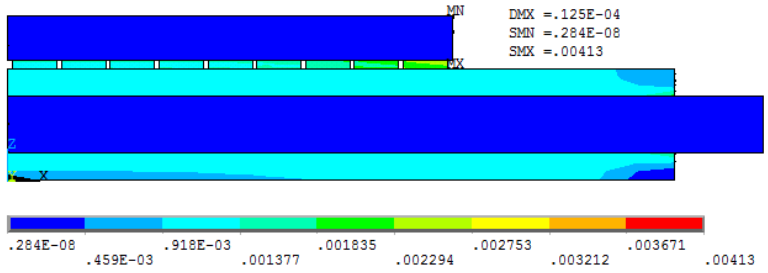
Figure 4.9. Finite element simulation of stress in the device-silver interface at -55°C after 50 cycles (a) continue silver attachment, and (b) sintered silver with grid pattern.

Figure 4.9 shows the stress distribution at the device-sintered silver interface at 50 °C after 50 temperature cycles. It is clear that with the grid-pattern, the maximum stress at the device-sintered silver interface was 29.3 MPa, while in the continuous silver attachment the maximum interfacial stress was 31.2 MPa. Therefore it was reasonable to conclude that grid-patterned silver allowed less thermomechanical stress generated at the device-silver interface than that of one continuous silver attachment.

In addition to the stress distribution, total strain of the assemblies was also simulated by finite element method, shown in Figure 4.10.



(a)

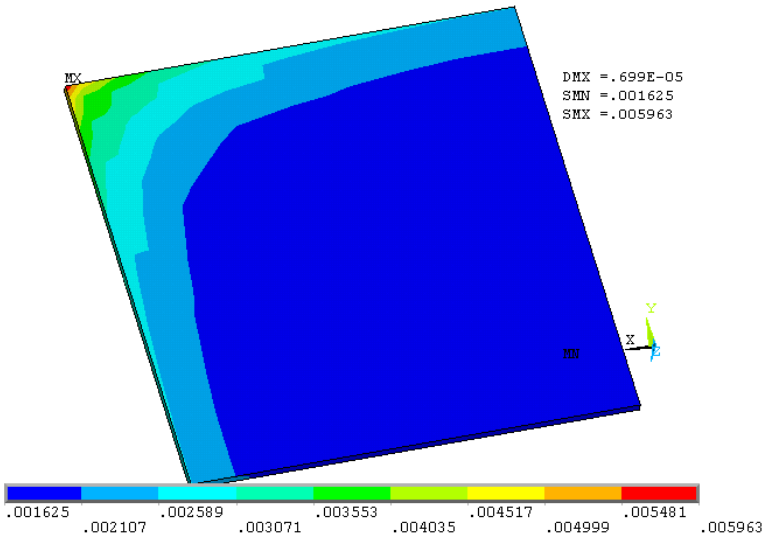


(b)

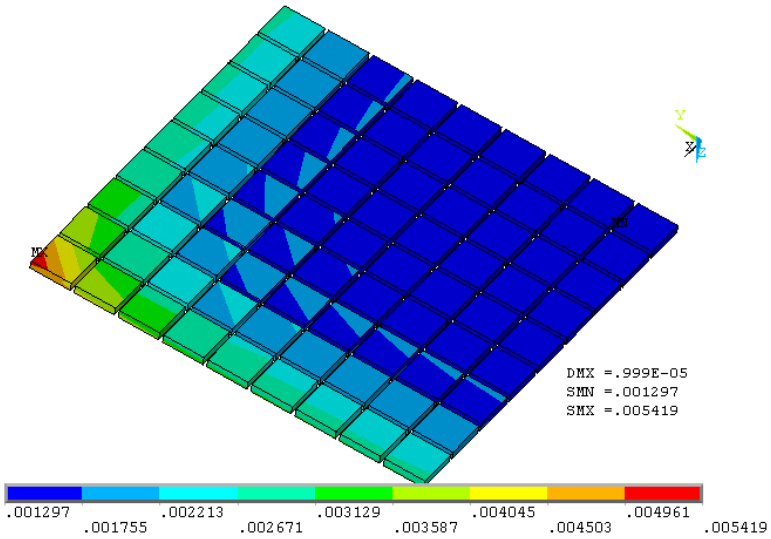
Figure 4.10. Finite element simulation of strain of assembly at 25°C (a) with continue silver attachment, and (b) sintered silver with grid pattern.

Similar to the stress simulation results, although the strains in two structures were about the same, the strain in the grid-patterned silver decreased quickly to a lower level. While in the continuous silver structure, the strain appeared to be continuing and decreases slowly as moving into the inner layer of silver.

Also when the strain at lower temperature was considered, Figure 4.11 shows the strains distribution in the silver layer at -55 °C. The highest strain in the grid-patterned silver was about 0.54%, at the outmost corner. While when the silver layer was one continuous piece, the highest strain was about 0.60%. Since the strain level at lower temperature was almost doubled than that of room temperature, and was generally considered more important to fail the assembly, the attachment with grid-patterned silver can be considered more reliable than the one continuous silver attachment.



(a)



(b)

Figure 4.11. Finite element simulation of strain of assembly at -55 ^{o}C (a) with continue silver attachment, and (b) sintered silver with grid pattern.

Figure 4.12 shows the strain accumulation in the silver layer during the temperature cycling process. It is clear that when the sintered silver appears the grid-pattern, the strain accumulation was always smaller than the sample with continuous silver attachment.

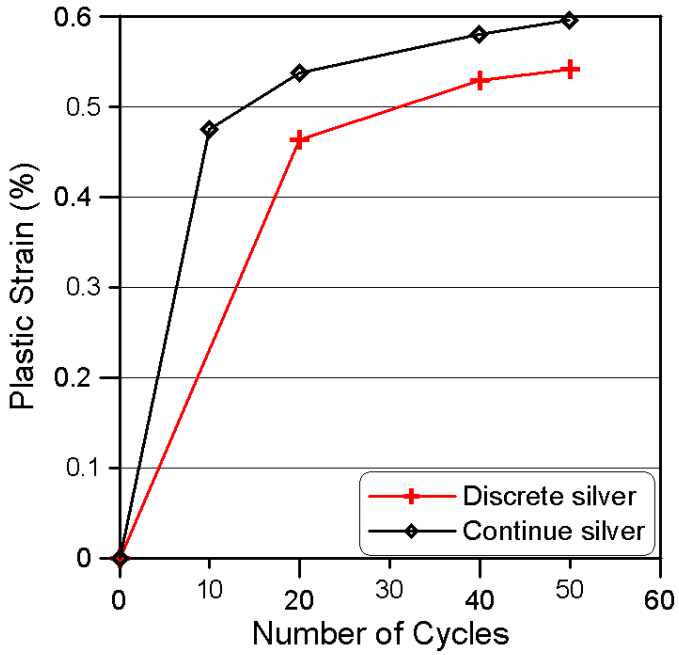


Figure 4.12. Increase of strain in the sintered silver layer during the first 50 temperature cycles.

It is believed that, like many other materials [126,127], the energy needed to nucleate a crack in the sintered silver is much higher than the energy to propagate the crack. Once the grid pattern is formed in the sintered silver layer, failure of the silver attachment will involve multiple crack nucleation processes and propagation processes.

$$Ndisc = aNnucl + bNprop \quad (4.2)$$

where *a* represents the number of grids in the sintered silver layer, and *b* is a constant smaller than 1. Since *Nnucl* is normally much bigger than *Nprop,* it is obvious that the lifetime of an attachment with discrete sintered silver can be much longer than an attachment with continuous sintered silver. The sintered silver with grid-pattern was therefore considered as more thermomechanically reliable than the silver layer with only one continuous piece.

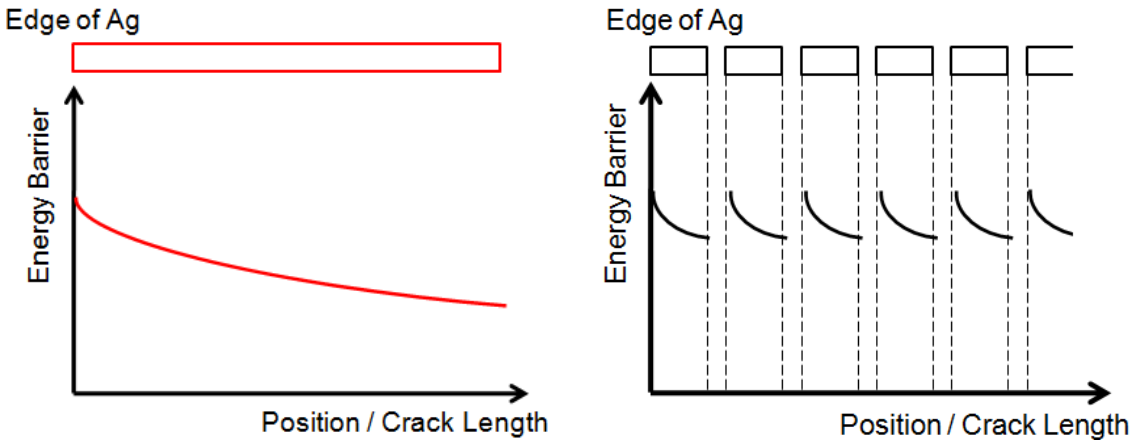


Figure 13.13 shows the schematics of the hypothesized energy levels that needed to cause a complete failure in the sintered silver layer. Denote the numbers of cycles to complete fail an attachment with continuous sintered silver and discrete sintered silver to be N_{cont} and N_{disc}, respectively, and N_{nucl} to be the number of cycle to create a new crack, N_{prop} to be the number of cycle for crack to propagate in the sintered silver. The following equations can be obtained,

$$N_{cont} = N_{nucl} + N_{prop} \quad 4.1$$

$$N_{disc} = aN_{nucl} + bN_{prop} \quad 4.2$$

where a represents the number of grids in the sintered silver layer, and b is a constant smaller than 1. Since N_{nucl} is normally much bigger than N_{prop}, it is obvious that the lifetime of an attachment with discrete sintered silver can be much longer than an attachment with continuous sintered silver. The sintered silver with grid-pattern was therefore considered as more thermomechanically reliable than the silver layer with only one continuous piece.

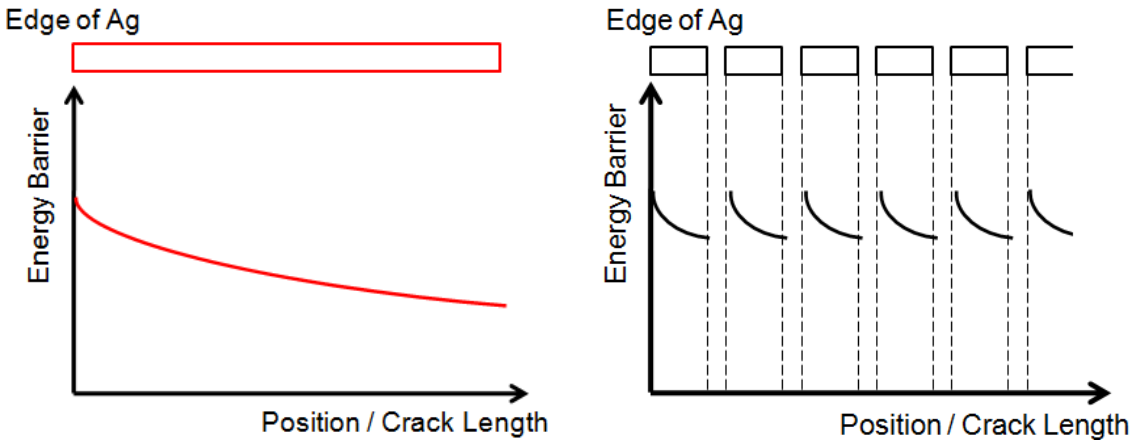


Figure 13.13. Hypothesized energy barriers to fail the attachment (a) with continuous sintered silver and (b) with discrete sintered silver.

4.4. Summary of the Effect of Substrate Roughness on the Die-attachment Shear Strength

Both with very promising properties to be able to use in high temperature electronics packaging, nanoscale silver paste and DBA substrate were used together for reliability test as well as characterizing their compatibility during temperature cycling test. As expected, die-shear strength of sintered silver on surface roughened DBA dropped significantly after temperature cycling. While comparing two testing methods, attach-before-cycling and attach-after-cycling, die shear strengths did not appear to be very different. It was suggested that the drop in die-shear strength was mainly due to the increasing surface roughness of the DBA substrate. The microstructural evolution of sintered silver had little influence on the drop in die-shear strength, if there was any.

With regard to the reliability of large-area sintered silver on DBA, promising microstructure showed that (1) the device-to-silver and silver-to-substrate interfaces remained intact even after cycling, no obvious horizontal cracks along the interfaces were observed; (3) sintered silver deformed with the roughened aluminum. Due to its porous structure and low elastic modulus, sintered silver was

supposed to be very compliant to thermomechanical stresses; and (4) some vertical cracks in the sintered silver layer were found after temperature cycling. From the cross-sectional SEM image, the vertical crack lines were found to be the 3D characteristics of the cycled silver layer. Finite element simulation suggested that the vertical crack lines were able to reduce the stress level in the semiconductor device, and in the mean time reduced the strain in the sintered silver layer. The sintered silver with grid-pattern was therefore considered as more thermomechanically reliable than the silver layer with only one continuous piece.

Chapter 5. SUMMARY AND CONCLUSIONS

With the working temperature of many applications approaching the limit of current packaging technologies, it is essential to develop technologies that are more advanced in terms of materials, structure, and manufacturability to fulfill the needs of systems with higher power density, higher temperature capability, and better reliability.

This study focuses on the development and evaluation of die-attach and substrate technology for high-temperature applications. For the die-attach material, nanoscale silver paste was developed as an alternative to solder alloys for better high-temperature capability, as well as better thermal, electrical, and mechanical performance. The second contribution of this study was the evaluation of direct bonded aluminum (DBA) substrate for high-temperature electronics packaging applications. Unlike the failure mode of the DBC substrate, no delamination of aluminum from ceramic base-plate was found for the DBA substrate, which made DBA a very promising substrate for high-temperature applications.

5.1. Development of low-temperature sintering of nanoscale silver paste for device attachment

A nanoscale silver paste that can be used as a lead-free die-attachment was developed as part of this work. It can be fired at temperatures below 300 ℃, and was capable of high-temperature operation. The joint that was formed after sintering contains sub-micrometer to micrometer-scale pores that were randomly distributed in the microstructure. This type of microstructure gave a very low elastic modulus of 9 GPa, which was substantially lower than those of bulk silver and high-temperature solder alloys while the CTE was comparable to that of bulk silver. Its electrical and thermal conductivities were around five times higher than

those of solder alloys. Typical die-shear strength of around 30 MPa can be obtained with a 300 ℃ or lower firing temperature and a relatively short peak temperature dwell time of 10 minutes. This can be increased further by a higher firing temperature and/or the application of a small amount of pressure. Temperature cycling results indicated that the nanoscale silver die-attach material had outstanding resistance to thermal cycling. This combination of properties made it a suitable candidate material for attaching SiC devices for elevated temperature operation.

For large-area device attachment, a modified heating profile was designed and used to sinter the nanoscale silver paste. Up to 5 MPa external pressure was applied during the sintering stage. Strong attachment of large chips to substrates with silver, gold, and copper metallization was also demonstrated. Analyses of the sintered joints by scanning acoustic imaging and electron microscopy showed that the attachment layer had a uniform microstructure consisting of micron-sized porosity to offer excellent reliability for high temperature applications.

5.2. Thermomechanical reliability of direct bonded aluminum (DBA)

Substrate reliability was one of the biggest problems in high-temperature electronics packaging. Unlike die-attach material, which focused on ease of application and working performance at high temperature, there was no standard substrate technology that claimed itself reliably working at high-temperature.

As an alternative to DBC, DBA substrate provided more compliant conducting layer and less stress accumulation at the metal-ceramic interface. In this study, the reliability of DBA substrate under the condition of large range thermal cycling (-55 ^{o}C to 250 ^{o}C) was studied. Due to the low elastic modulus of aluminum and less strain hardening of aluminum, thermomechanical stress induced at the Al-AlN interface was much less than that of DBC substrate, no delamination of the aluminum layer from the ceramic base-plate was observed for up to 1500 thermal

cycles.

However, the aluminum surface was found to be roughened after the cycling tests, which could be the biggest obstacle for DBA to be used in high-temperature electronics packaging applications. Based on microstructure characterization of temperature cycling DBA, significant recrystallization was observed. It was believed that, for aluminum with small grains, at high temperature, 250 ^{o}C, under tremendous thermomechanical stress, hillocks would form on the aluminum surface as a means to relieve the compressive stresses, especially at grain boundaries. It was also observed that by metalizing aluminum with Ni and Ag would help delaying the formation of hillocks, which can also be explained by the stress relieving theory. For some of the large size grains, as they were under recrystallization and recovery processes, they were firstly broke into many small grains, and then continue to undergo the formation of hillocks. For some other large grains that were suitably aligned to the applied stress, wrinkling would occur in those grains that contained shear planes which experience a maximum resolved shear stress greater than the critical resolved shear stress for plastic flow on that plane. Therefore in a temperature cycled DBA substrate, the typical pattern on the aluminum would be the combination of many small hillocks randomly distributed on the surface, and a few wrinkling patterns with mostly paralleled striations.

5.3. Effect of Substrate Roughness on the Die-attachment Shear Strength

Both with very promising properties to be able to use in high temperature electronics packaging, nanoscale silver paste and DBA substrate were used together for reliability test as well as characterizing their compatibility during temperature cycling test. As expected, die-shear strength of sintered silver on surface roughened DBA dropped significantly after temperature cycling. While

comparing two testing methods, attach-before-cycling and attach-after-cycling, die shear strengths do not appear to be very different. It is suggested that the drop in die-shear strength was mainly due to the increasing surface roughness of DBA. The microstructural evolution of sintered silver had little influence on the drop in die-shear strength, if there was any.

With regard to the reliability of large-area sintered silver on DBA, promising microstructure shows that (1) the device-to-silver and silver-to-substrate interfaces remain intact even after cycling, no obvious horizontal cracks along the interfaces are observed; (3) sintered silver deformed with the roughened aluminum. Due to its porous structure and low elastic modulus, sintered silver was supposed to be very compliant to thermomechanical stresses; and (4) some vertical cracks in the sintered silver layer were found after temperature cycling. From the cross-sectional SEM image, the vertical crack lines were found to be the 3D characteristics of the cycled silver layer. Finite element simulation suggested that the vertical crack lines were able to reduce the stress level in the semiconductor device, and in the mean time reduced the strain in the sintered silver layer. The sintered silver with grid-pattern was therefore considered as more thermomechanically reliable than the silver layer with only one continuous piece.

5.4. Original contributions

1. Developed an interconnect material, nanoscale silver paste, for large area semiconductor device with improved thermal, electrical and reliability performance;
2. Analyzed the effects of large temperature cycling range on the thermomechanical reliability of direct bonded aluminum (DBA) substrate. Identified the mechanisms that cause the aluminum surface to get roughened;

3. Analyzed the reliability of low-temperature sintered silver attachment on DBA substrate for high-temperature electronics packaging experimentally and numerically. Discovered the formation of vertical crack lines in the sintered silver layer during temperature cycling reliability test.

5.5. Publications and patents

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Patent:

Nanoscale Metal Paste for Interconnect and Method of Use

Guo-Quan Lu, Guangyin Lei, and Jesus N. Calata

US patent application No. 20090162557

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APPENDIX A: ELECTROPLATING OF SILVER PROCESS

For electroplating of Ag, sample material can be pre-metalized with Cu, Ni, or electroless Ag. For heavily oxidized surface, Cu or Ni in air for long time, short time etching in nitric acid (for Cu) or slight polish with sandpaper (for Cu & Ni) can be applied to remove the surface oxidization. Before electroplating, substrate should be cleaned using acetone, alcohol, and DI water, with ultrasound agitation for ~10 minutes. After the cleaning process, dry the sample with compressed air immediately to prevent the surface oxidation.

Electroplating of Ag is divided into two steps. First step is the activation of sample surface with “Silver Strike” plating bath. This plating bath contains high concentration of cyanide ions and low concentration of silver ions. By applying “high” current density between the sample and the anode (silver plate), silver ions will attack the sample surface, and form a very thin yet porous silver layer. This step has to be very short, up to 30 seconds, so that the porous silver structure would not be too thick to cause weak adhesion problem. For the second electroplating step, the plating bath contains higher concentration of silver ions. The plating current density is only half of that used in the strike process. The plating time is about 10 to 15 minutes.

Because not only the silver ions exist in the plating bath, but also the sodium, potassium, and especially hydrogen ions will adhere to the sample surface, driven by the electric current. If the silver concentration in the plating bath has dramatically changed, and non-proper current density is applied, large amount of hydrogen ions may accumulate on the sample surface and would have potential to deteriorate the plating quality. Therefore, after the plating process, sample will be slowly heated up to 300^{o}C, soaked for 30 minutes to evaporate all the hydrogen atoms in the plating film. Tape test will then be applied to check the

adhesion between the silver metallization and the substrate material. For direct plating of Ag on Cu surface, heating at 300^{o}C should be shortened within several minutes to prevent further diffusion of Cu atoms into Ag metallization. Because there is no diffusion barrier between Cu and Ag, Cu atoms will soon diffuse to the sample surface, and become oxidized at such high temperature.

All the chemicals used to prepare the "Silver strike" and "Silver plating" baths can be obtained from Alfa-Aesar (www.alfa.com).

1. Silver strike

Silver cyanide	6.6 g/L
Potassium cyanide	75 g/L
Potassium carbonate	15 g/L
Temperature	Room temperature
Current density	20 ~ 25 mA/cm^2
Duration	Up to 30 seconds
Anode	Silver plate

*In calculating the current used in the plating process, do not forget to count the whole area of the sample submerged in the plating bath.

2. Water wash

Swill in tap water followed by rinsing in DI water

3. Silver plating

Silver cyanide	36 g/L
Potassium cyanide (or NaCN)	60 g/L (45 g/L for NaCN)
Potassium carbonate (or Na_2CO_3)	45 g/L (37.5 g/L for Na_2CO_3)
Temperature	Room temperature
Current density	~10 mA/cm^2
Duration	15 minutes for 8.5 μm
Anode	Silver plate

After electroplating of silver, rinse the sample thoroughly with tap water and blow it dry with compressed air.

APPENDIX B: ELECTROPLATING OF NICKEL PROCESS

For electroplating of Ni, sample material can be pre-metalized with Cu. Short time etching in nitric acid is always applied to remove the surface oxidization. After etching, thoroughly rinse the sample with DI water and dry the surface with compressed air immediately to prevent the surface oxidation.

All the chemicals used to prepare the nickel plating bath can be obtained from Alfa-Aesar (www.alfa.com).

Plating bath (Watt type bath)

$NiSO_4$	300 g/L
$NiCl_2$	45 g/L
Boric acid	40 g/L
pH	2.5 ~ 4.0 (acidified with sulfuric acid)
Temperature range	50 ~ 60 ^oC
Current density	20 mA/cm^2
Duration	10 minutes for 4.5 µm
Anode	Nickel plate (mesh)

After electroplating of nickel, rinse the sample thoroughly with tap water and blow it dry with compressed air.

APPENDIX C: ELECTROLESS PLATING OF SILVER PROCESS

Electroless silver plating only works on samples pre-metalized with Cu. Short time etching in nitric acid is always applied to remove the surface oxidization. After etching, thoroughly rinse the sample with DI water and dry the surface with compressed air immediately to prevent the surface oxidation.

Electroless silver plating bath is obtained from Alfa-Aesar (www.alfa.com). After sample is cleaned, it will be submerged in the plating bath. No electrode and power supply is needed. Unlike the electrolytical plating processes, electroless plating process is initiated by a chemical reaction between Cu and Ag. During the plating process, the ambient temperature is kept between 75^{o}C to 85^{o}C. Because the reaction happens when Cu is exposed to Ag bath, it would stop when the Cu surface is fully covered with fresh Ag. The plating thickness is only several hundred nanometers, 300 ~ 400nm. The plating duration is usually 10 minutes.

After the plating process, rinse the sample thoroughly with tap water and blow it dry with compressed air.