

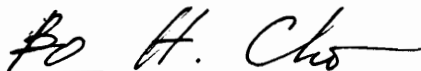
**MODELING AND ANALYSIS OF SPACECRAFT BATTERY CHARGER  
SYSTEMS**

by

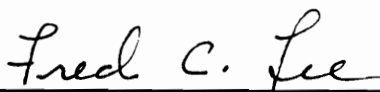
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Doctor of Philosophy  
in  
Electrical Engineering

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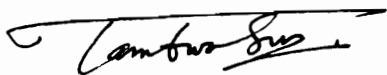
Bo H. Cho, Chairman



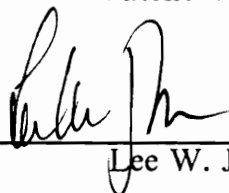
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April, 1991

Blacksburg, Virginia

# MODELING AND ANALYSIS OF SPACECRAFT BATTERY CHARGER SYSTEMS

by

Seong Joong Kim

Bo H. Cho, Chairman

Electrical Engineering

(ABSTRACT)

Large-signal analysis of various spacecraft power systems is performed to predict the bus dynamics in various modes of operation. The large-signal trajectories of the system's operating point are analyzed employing qualitative graphical representation. The analyses are verified through simulation using EASY5 software.

Small-signal dynamic characteristics of spacecraft battery charge converter systems are analyzed to facilitate the design of control loop for optimum performance and stability. Control-loop designs for the charge converters in bus voltage regulation mode, charge current regulation mode, and peak power tracking mode are discussed.

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I also acknowledge the supports provided by NASA GSFC and NSF.

With much love and gratitude, I thank my parents for their support and prayers.

Finally, I would like to thank my wife, Hyun-sook, for her care, understanding and love. I dedicate this dissertation to my wife, Hyun-sook, in token of my love and appreciation.

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# Chapter 1

## Introduction

### *1.1 Background*

A spacecraft power system provides the generation, storage, regulation, and distribution of electrical power required for all service demands on the spacecraft. Power for earth-orbiting satellites is usually generated by arrays of photovoltaic cells which convert solar energy to electrical power. The power generated by the solar array is stored and regulated by a combination of storage batteries and voltage regulators. The batteries are required to provide the power when the spacecraft is in the earth's shadow and the sun is eclipsed. They can also provide

peak power for demand beyond the capacity of the solar array for a short period of time. The solar array degrades due to high energy particles, and the battery efficiency degrades with charge/discharge cycling; these parameters limit the spacecraft mission life.

Typical spacecraft power systems consists of a solar array, an energy storage battery, and power processing electronics. Different configurations of the power processing electronics results in different power systems. Although their configurations vary depending on their orbits, power level, and applications, they can be broadly divided into two types: direct energy transfer (DET) systems and peak power tracking (PPT) systems [4,5,6].

In the DET system, solar array power is directly transferred to the load without the use of any series connected regulator or converter. However to regulate or limit the bus voltage, a shunt regulator or limiter is employed. The power conditioning equipment (such as the shunt regulator, battery charger and discharger) not only balances the power but also regulates the bus voltage. Because of weight and efficiency advantages over series pass linear regulators, switching regulators are widely used for battery chargers and dischargers as well as for load converters. There are many references [40 - 46] introducing topologies of the battery charger and discharger for specific spacecraft. Typically a buck converter is used for the battery charger, and a boost or boost derived converter is used for the battery discharger.

The PPT system uses a series switching converter (typically a PWM buck converter) between the solar array and distribution bus. The series converter locates the solar array's operating point at the peak power point by controlling the duty ratio. Various techniques are reported for peak power tracking schemes [37 - 39].

Whenever the spacecraft comes out of eclipse, the solar array is at a very low temperature, and generates maximum power. A spacecraft in a low earth orbit (LEO) not only goes through a large number of eclipses compared to a spacecraft in geosynchronous orbit (GEO), but also the ratio of eclipse period to orbit period is much higher. Because the interval that excess power is available is substantial in LEO, the the series regulator power loss is compensated, and a smaller solar array can be used. Therefore, many spacecraft in LEO utilize the PPT system. In GEO, the extra power that is produced by the cold solar array after eclipse is a much smaller percentage of the total energy profile. Therefore, the advantage that was observed in LEO is not present. In this case, the series regulator power losses are greater than the power gained by the cold array. Thus, the shunt regulator system (DET) is more efficient in use of solar array power in GEO because it has less overall power dissipation. Trade-off studies between DET and PPT systems have been conducted in [4,5,6].

## ***1.2 Objective and Outline***

A spacecraft power system requires reliability, long life, and high efficiency. As discussed in the previous section, design of a system's configuration, size of the solar array and capacity of the battery are largely dependent on the performance of the power conditioning equipment. Especially, an efficient and reliable battery charging system is most critical.

Solar arrays, as the primary power source for a spacecraft, have nonlinear output I-V characteristics. The operating point of the solar array is determined by such factors as the array's temperature, illumination level, and the load characteristics of the power conditioning equipment. There are several modes of operation, resulting from variations in illumination level and load demands. The operating mode of the charger varies widely according to the solar array output characteristic at a given load condition. Also, different power system configurations result in different modes of operation of the charger.

Because of the weight and efficiency advantages over series pass linear regulators, switching regulators are widely used in battery charger systems. Switching regulators are highly nonlinear, as are the output characteristics of the solar array. A nonlinear charger, when coupled with a nonlinear solar array source and nonlinear load, results in dynamics very different from those of conventional switching regulators in dc to dc power conversion applications. Moreover, the charger

regulator operates in the peculiar way that the input voltage is regulated. Since the charger operates from a very light load to full load condition it has both discontinuous and continuous inductor current modes of operation. Both modes of operation must be considered during controller design.

In the DET system employing the regulated bus configuration, the battery charger has two different modes of operation. When there is sufficient solar array current to supply the spacecraft loads, yet insufficient solar array current to charge the batteries at commanded rates, the spacecraft bus is regulated by controlling the charge current to the batteries in a method similar to a shunt regulator. This mode is called the charger's bus voltage regulation mode. When there is sufficient current from the solar array to charge the batteries at commanded rates, the charger regulates the battery charging current. This period is called the charge current regulation mode. The charger has two independent control loops for bus voltage regulation and charge current regulation. The operating mode, voltage or current regulation, is selected by a central mode controller. Dynamics of the charger and its terminal characteristics are quite different between the two modes of operation.

PPT systems employ a series switching regulator between the solar array and distribution bus. The series converter controls the solar array's operating point at the peak power point. The converter then regulates solar array output voltage

according to the reference voltage set by the tracker. The peak power tracker is activated only when the battery is not fully charged or when the load demand is greater than the solar array output. When peak power tracking is not used the series converter is used for a battery charge current controller. Dynamics also differ in the bus voltage regulation mode from the charge current regulation mode.

When the solar array feeds the load converters, multiple equilibrium operating points exist, but only one is desirable [20,21,22]. In [22], the stability conditions of the system operating points were derived analytically. The trajectories of the system operating point are determined according to the stability nature of the equilibrium points. When the power conditioning equipment, i.e. the battery charger, regulates the solar array output voltage, stability of the operating point and its trajectories are determined by the power conditioning equipment.

The objective of this research is to analyze the dynamic behaviors of various types of spacecraft power processing systems focusing on the battery charging system, and to provide design guidelines for the charge regulator for the optimum performance and stability of the system.

In Chapter 2, large-signal analysis for both DET and PPT systems is performed employing a graphical analysis method providing physical insight into the system. Steady-state operating points are identified with respect to the operating condi-



tions for various spacecraft power systems. An effective source line or load line including the power conditioning equipment are considered graphically. Stability of the operating points and their trajectories during the transition between sunlight and eclipse periods are analyzed. Analyses are verified by EASY5 simulation.

In Chapter 3 and 4, small-signal analyses of the DET charger system operating in bus voltage regulation mode and charge current regulation mode are performed. A buck switching converter for the charger is modeled for both CCM and DCM. Design strategies for the regulator are presented. The non-minimum phase nature of the system in the bus voltage regulation mode is analyzed.

In Chapter 5, small-signal modeling and analyses of the PPT charger system operating in the both peak power tracking mode and charge current regulation mode are performed. When the peak power tracking is active, the reference voltage of the regulator set by the tracker changes continuously as the illumination level of the solar array changes. Dynamics of the system due to the change in the reference voltage are modeled and analyzed.

Conclusions are presented in Chapter 6.

As systems increase in size, computer modeling becomes essential for study of the performance of power systems as a whole rather than the various subsystems in-

dividually. These computer models can be divided into two groups: the small-signal ac model, and the large-signal model. Small-signal models are linear or linearized models. They are used mainly for frequency domain analysis. The objective of small-signal models [18,19] is to ensure the stability of all feedback loops of various power conditioning equipment and to characterize the bus impedance. Large-signal models incorporate nonlinearities in the system and circuits (i.e., switches, saturation, protection, limiters, and other nonlinear functions). Large-signal models [8-17] are used for transient simulation to predict system behavior under different operating conditions: sunlight, eclipse and transition period.

At the Virginia Power Electronics Center, modeling and analysis of spacecraft power system has been done extensively for several years. Component models were developed and updated continuously using an existing dynamic system analysis software, EASY5. Since EASY5 uses modular concepts, each component of spacecraft power systems was modeled as a separate macro module. These component models were stored in a model library. It includes the solar array, different types of shunt regulators, batteries, several different topologies of charger and discharger, loads, switching converters, filters, and different types of controllers [26-29]. The model library was expanded to incorporate the ac bus spacecraft. With these models, different systems are configured collecting corresponding component models from the model library. EASY5 component models used in this research are provided in Appendix A. Appendix B presents EASY5 program lists of system models and their analysis programs.

## Chapter 2

# Large-Signal Analysis of Spacecraft Power Systems

### *2.1 Introduction*

Solar arrays, the primary power source for spacecraft, have highly nonlinear output I-V characteristics. The operating point of the solar array is determined by factors such as the array's temperature, illumination level, and the load characteristics of the power conditioning equipment.

There are several modes of operation, resulting from variations in illumination level and load demands. The nonlinear solar array source, coupled with nonlinear load characteristics, often has multiple equilibrium points, of which only one

is desired. An undesired oscillation or sudden voltage drop in the solar array's output may occur, depending on the system's operating conditions [21].

In this chapter, large-signal behaviors of various spacecraft power systems are analyzed with qualitative graphical representations of the trajectories of the system's operating point. The dc characteristics of the solar array, battery, various power conditioning equipment, and spacecraft loads are expressed as current-voltage (I-V) curves.

The operating point of the system is determined by finding the intersection (equilibrium point) of the source and load curves. This graphical analysis method is verified through simulations using the models described in [27 - 30].

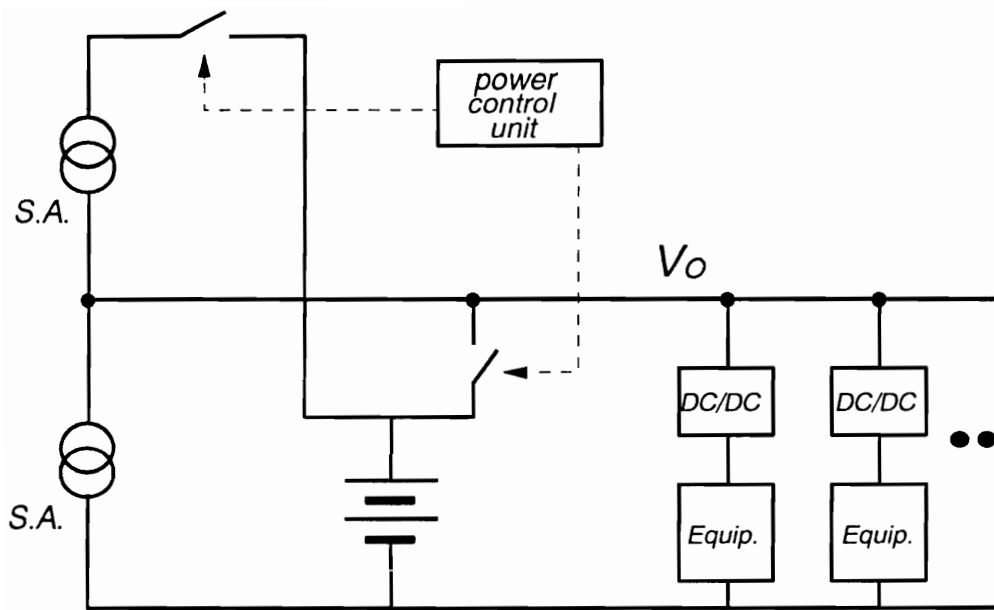
Dynamic behavior of the unregulated bus system and sunlight regulated bus system are reviewed in the Section 2.2 and 2.3. The battery lock-up phenomenon at the exit of eclipse for the sunlight regulated bus system is elaborated upon. In Section 2.3 the regulated bus system's modes of operation between eclipse and sunlight periods are discussed. The PPT system's large-signal behavior is presented in Section 2.4.

## 2.2 *Unregulated Bus Systems*

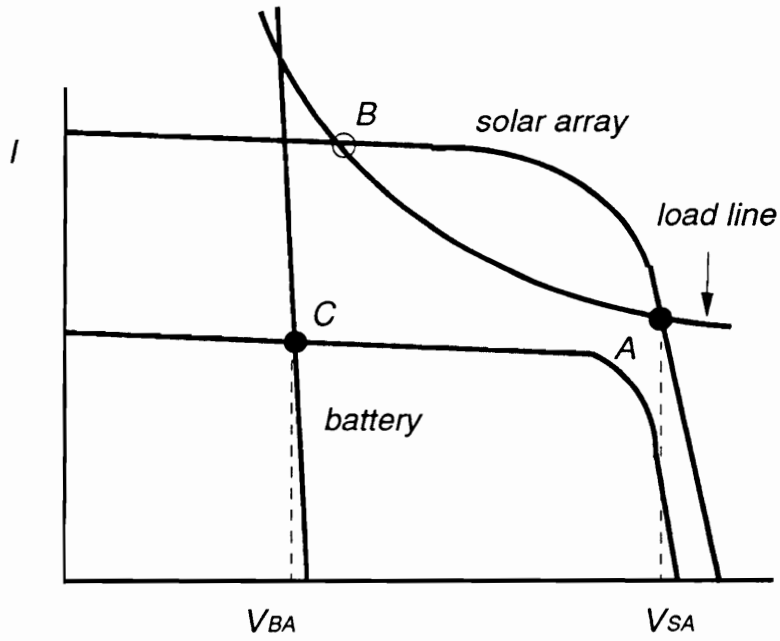
In the unregulated bus system, solar array and battery are directly connected to the bus, reducing the control electronics of the power system. A typical configuration is shown in Fig. 2.1. The solar array is divided into two parts. The main array is connected directly to the bus and feeds spacecraft payloads. A secondary array in series with the main array acts as a current source used to charge the battery after eclipses. Two switches commanded by the power control unit control the charge/discharge of the battery and the connections to the bus.

In this unregulated bus system, the bus voltage directly depends on the energy source characteristics. Figure 2.2 shows the solar array output and the equivalent load characteristics. A spacecraft power system usually has many load converters to feed the various pieces of equipment which requires regulated input voltages. Since the load converters regulate their output voltages, they can be treated as a constant-power load, assuming that the converters are lossless.

During the sunlight period, the operating point is determined by the intersection of the solar array source curve and the constant power load line. There are two equilibrium points, A and B. It is known that the operating point in the voltage source region of the solar array (Point A) is the stable equilibrium point, while the operating point in the current source region of the solar array (Point B) is an unstable equilibrium point. A detailed analytical proof is given in ref [21]. As the



*Figure 2.1. Block Diagram of Unregulated Bus System*

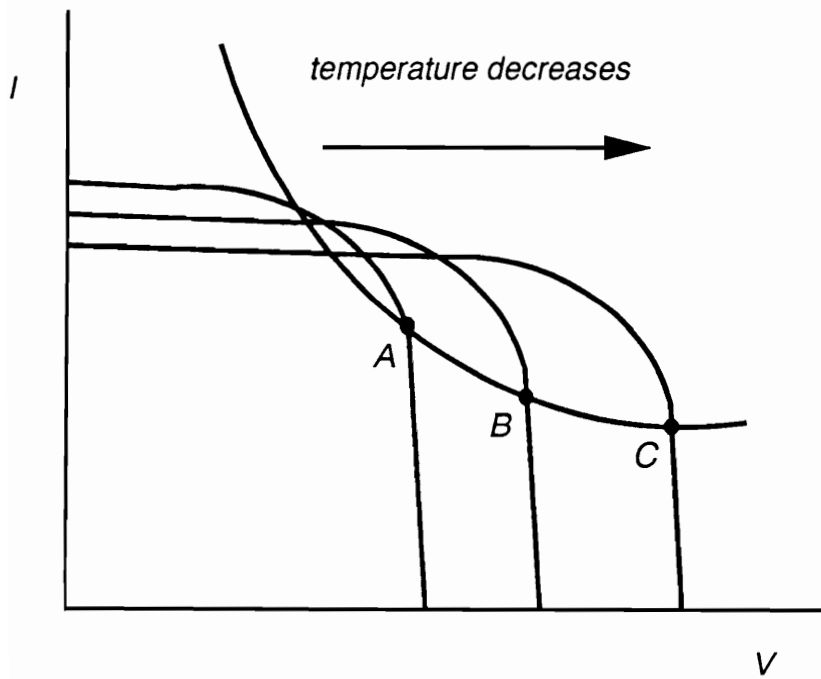


**Figure 2.2. Operating Points of Unregulated System**

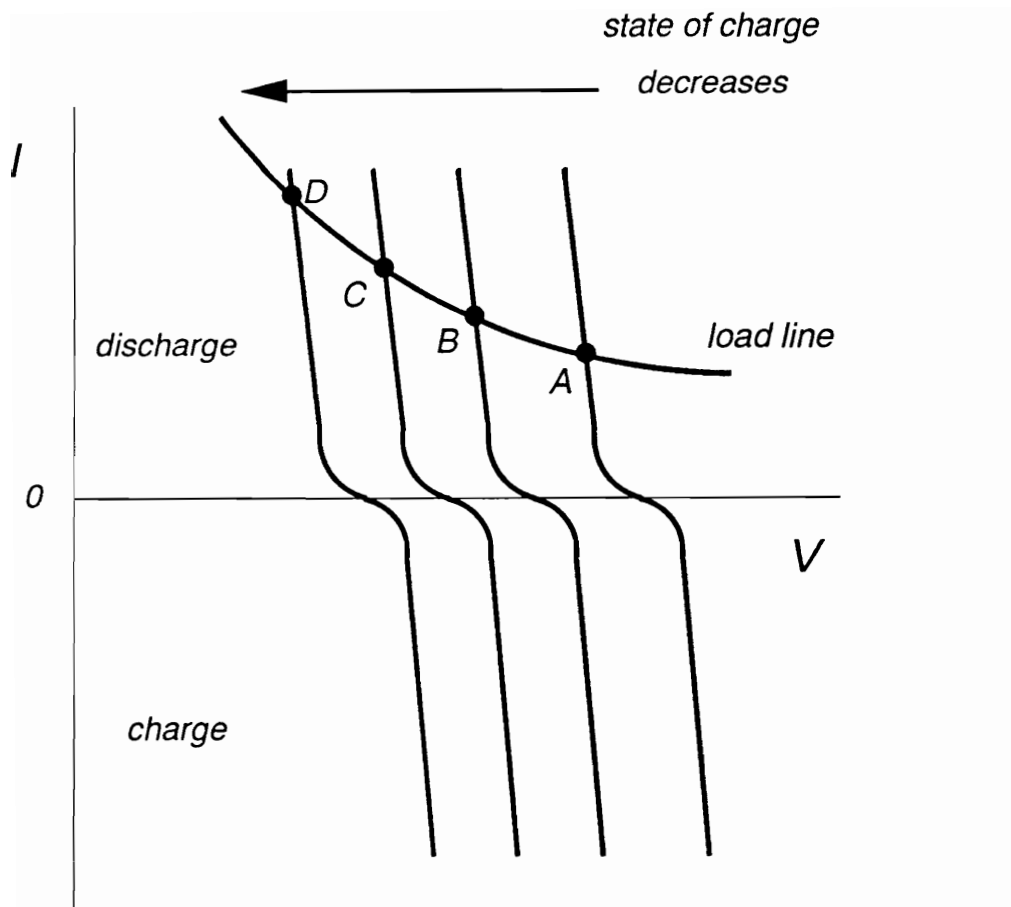
solar array output power decreases, the system's operating point moves to the intersection of the battery source line and the constant power load line, Point C.

As shown in Fig. 2.2, the bus voltage changes between the battery voltage and the solar array voltage. Also, the solar array output voltage and the battery voltage themselves vary widely. The solar array output voltage is sensitive to changes in temperature as shown in Fig. 2.3. For instance, when the spacecraft comes out of the eclipse period, the low temperature of the array produces a high voltage (Point C). As the temperature increases, the operating point moves to Point A. Battery characteristics also change according to the state of charge (SOC) of the battery as shown in Fig. 2.4. As the battery discharges, the operating point moves from A to D, and bus voltage drops. These characteristics of the solar array and battery result in a large variation of the bus voltage during the orbit period. For instance, the bus voltage changes from 20 V to 70 V for FLTSATCOM [25, 26]. Due to the wide variation of bus voltage, the overall efficiency of the unregulated bus system is low compared with the regulated bus configuration [25].





*Figure 2.3. Solar Array I-V Characteristics*



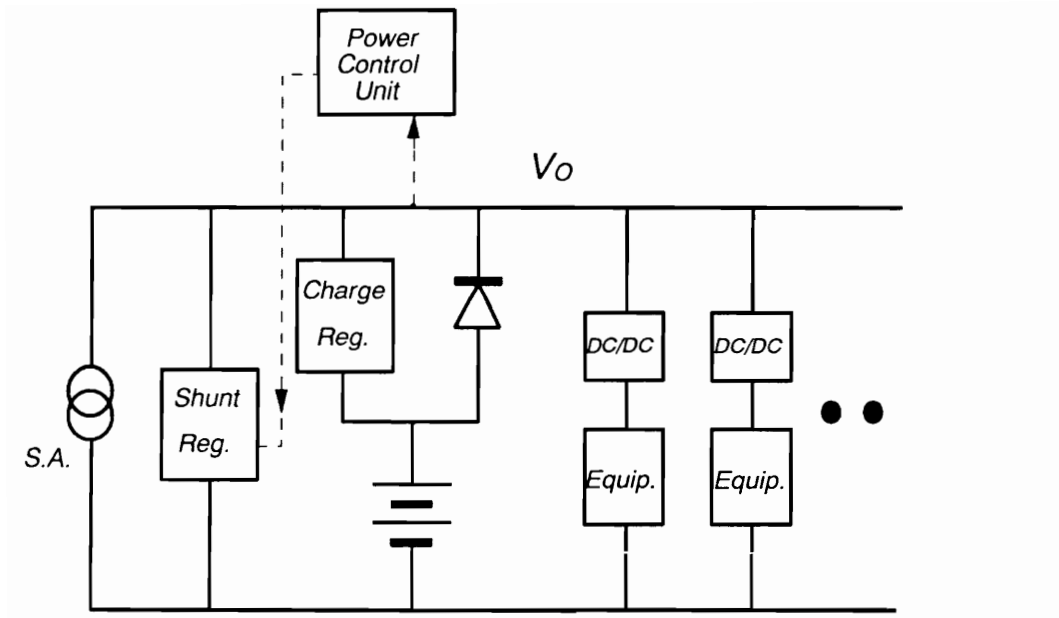
**Figure 2.4. Battery I-V Characteristics**

## ***2.3 Sunlight Regulated Bus System***

In the sunlight regulated bus system, voltage regulation is implemented during the sunlight period to reduce the large voltage variation on the bus. A typical configuration is shown in Fig. 2.5. The operating voltage of the solar array is fixed by a shunt regulator during the sunlight period. The solar array provides energy to the spacecraft loads and recharges the battery. The excess energy is radiated to space by the shunt regulator in order to maintain the bus voltage at a fixed value. A charge regulator is used to regulate charging current. During the eclipse period, however, the bus is directly connected to the battery. Thus bus voltage is no longer regulated.

During the eclipse period, or when peak power demands exceed the capacity of the solar array, the bus voltage drops and is clamped to the battery voltage by the forward diode. The system's mode of operation then is similar to the unregulated system.

Since the solar array degrades during the mission period, different solar array I-V curves exist at its beginning- and end-of-life. The bus regulation voltage should be selected near the peak power voltage at the end-of-life in order to obtain maximum available power at the end-of-mission. By doing so, the system can have an energy balance throughout the mission period. Thus the selected regulation voltage resides in the current source region of the solar array. Without a regulator the operating point in the current source region is unstable in the case



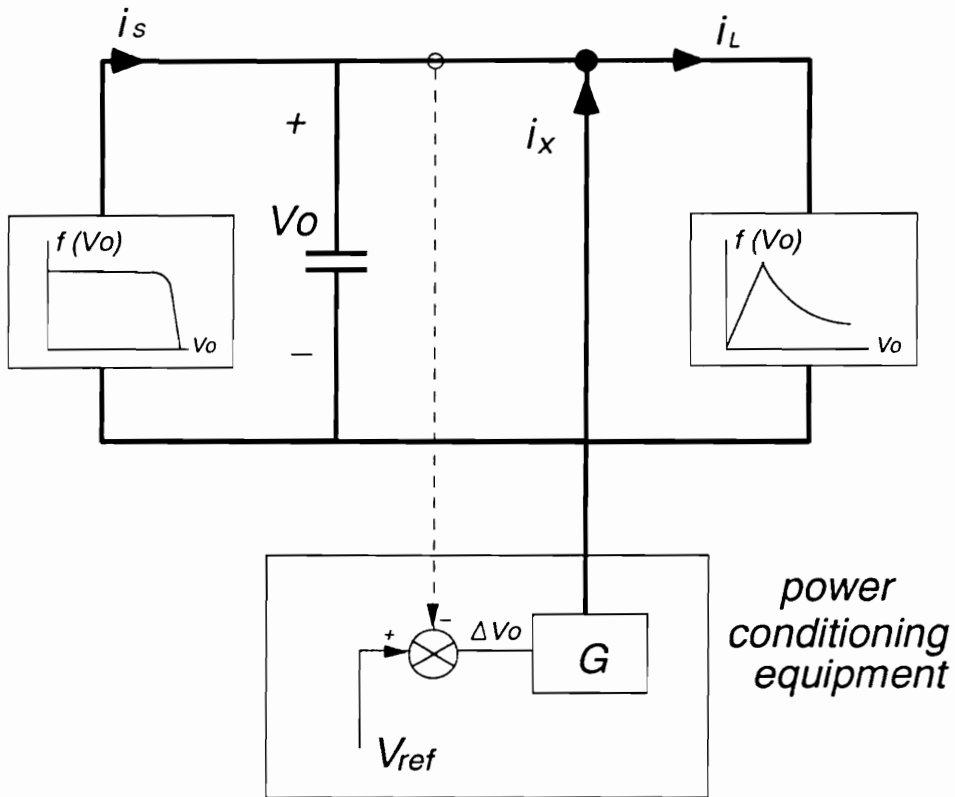
**Figure 2.5. Block Diagram of Sunlight Regulated System**

of a constant-power load, as discussed in the previous section. A qualitative graphical method is employed to analyze how the shunt regulator makes the system stable.

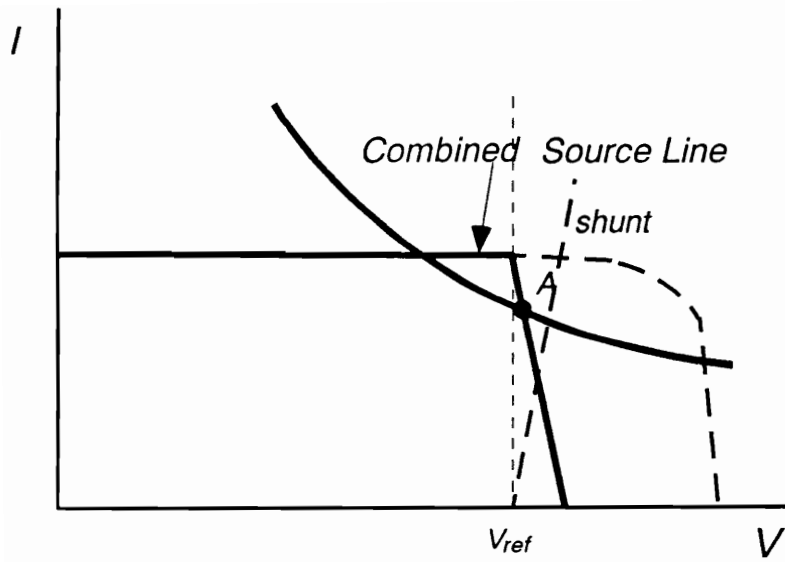
Figure 2.6 shows the block diagram of the system with the bus voltage regulator. The sensed bus voltage is compared with a reference voltage. The resulting error signal is amplified by the transadmittance of the shunt regulator  $G$ , to generate the shunt current  $i_x$  which controls the bus voltage. For large-signal analysis, the transadmittance of regulator can be treated as a transconductance. That is, the dynamics of the regulator itself are ignored for qualitative analysis of the system's dynamic behavior. In [21], the eigenvalues of the system are derived, and it is shown analytically how a power conditioning equipment (shunt regulator) stabilizes the system in the current source region. This can be explained graphically, providing physical insight to the system.

The transconductance of the shunt regulator can be combined with the solar array line, thus forming an effective source characteristic seen by the constant power load, as shown in Fig. 2.7(a). Physically, it means that with the shunt regulator the effective source becomes a stiff voltage source supplying the constant power load. Thus the operating (equilibrium) point resides on the shunt line (stiff voltage source) and system is stable.

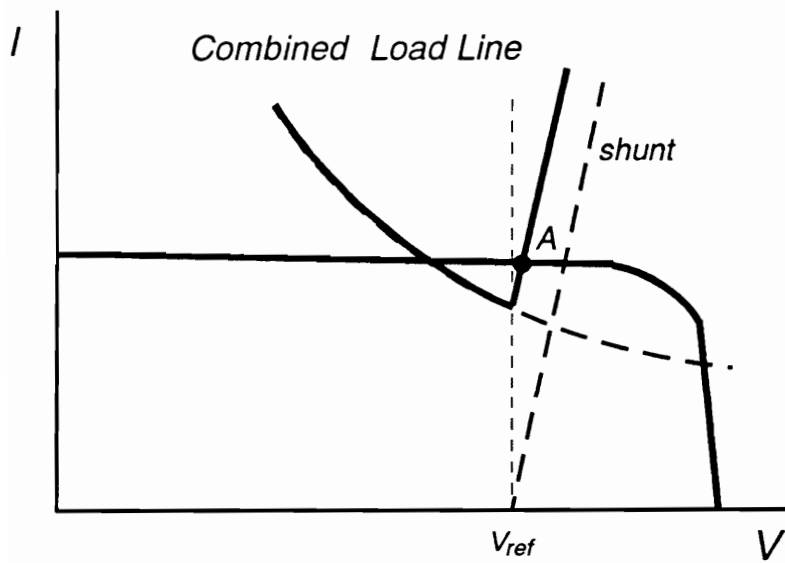
Another way to treat the system in the shunt mode is that the effective load characteristic seen by the solar array is constructed by combining the shunt reg-



**Figure 2.6. Functional Block Diagram of Bus Voltage Regulator**



(a)



(b)

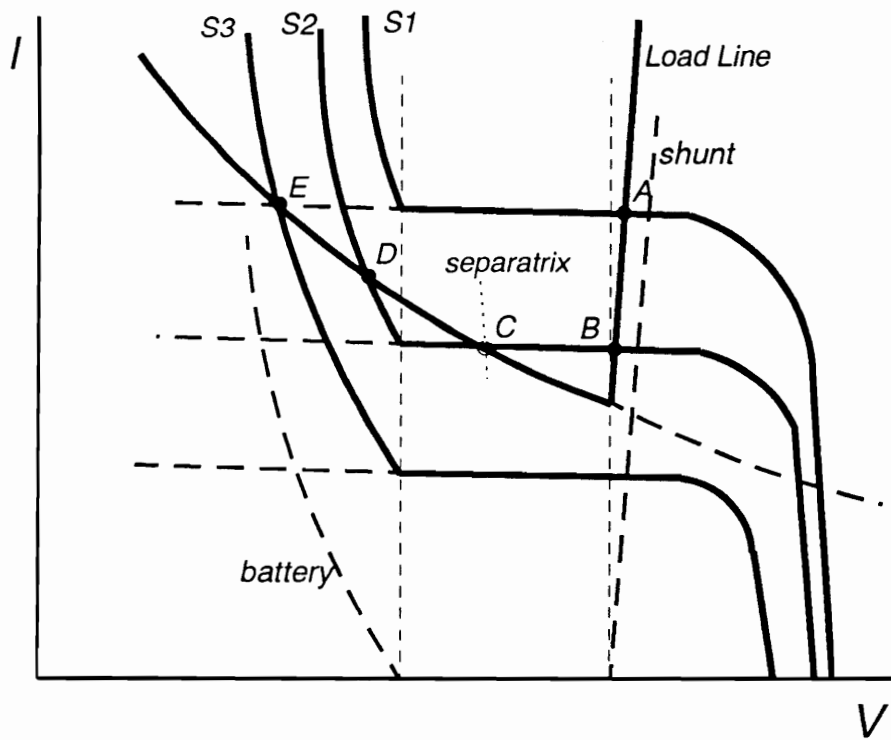
**Figure 2.7. Operating Point in Shunt Mode**  
 (a) seen by the load  
 (b) seen by the solar array

ulator with the constant power load line, as shown in Fig. 2.7(b). This translates physically into a constant current source (solar array) supplying a low resistance load. Therefore, the undesired dynamic loading effect will not occur and the system will be stable.

The large-signal behavior of the sunlight regulated bus system is shown in Fig. 2.8. It includes three (S1-S3) effective source characteristics and an effective load characteristic. Effective source lines are obtained by adding the solar array curve and battery characteristics. The load line is the sum of the I-V curves of the constant power load and the shunt regulator.

Curve S1 represents a source characteristic when the system operates in sunlight mode. There exists only one stable equilibrium point A generated by the shunt regulator. Curve S3 represents the system operating in the battery discharging mode, which has a stable equilibrium point E. Between Curves S1 and S3, there exists Curve S2 which has three equilibrium points B, C, and D. The Points B and D are stable operating points, but Point C is an unstable point. When an unstable equilibrium point resides between two stable points, there exists a separatrix (the line through Point C for curve S2) which separates the trajectories between the two stable equilibrium points. If the previous operating point stays on the right-hand side of the separatrix, the operating point remains at the shunt line (point B). And when the previous operating point stays on the left side of the separatrix, the operating point remains at the battery line (point E).



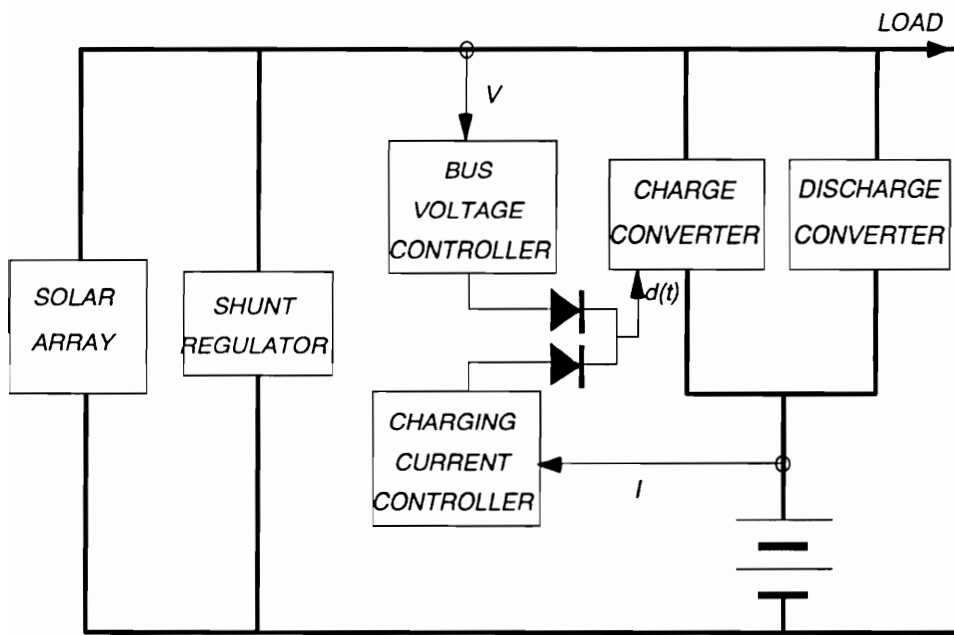


**Figure 2.8. Large-Signal Behavior of Sunlight Regulated System**

During the transition from eclipse to sunlight, although the solar array can provide enough power to the load, the operating point remains at the battery line (point D) since the operating point cannot cross the separatrix. This undesirable phenomenon is known as the battery lock-up [12]. Recovery from lock-up can be achieved either by reducing the load or by increasing the solar array power temporarily. Then the operating point moves into the shunt line (Curve S1) which has only one equilibrium point. When these are impossible, the only condition for recovery is oversizing of the solar array.

## ***2.4 DET Regulated Bus System***

The main difference between the regulated bus system and the sunlight regulated system is that the diode at the battery output is replaced by a battery discharge regulator which regulates the bus voltage during the eclipse period. Figure 2.9 shows the block diagram of the regulated-bus system, which includes the power conditioning equipment. In the regulated-bus system, the power conditioning equipment, such as the shunt regulator, battery charger and discharger, not only balance the power but also regulate the bus voltage. A bus voltage band scheme is used to activate each regulator within a specific range of bus voltage.



**Figure 2.9. Block Diagram of Regulated Bus System**

As far as the bus dynamics are concerned, the battery discharger has the same characteristics as the shunt regulator, except that the direction of the control current  $i_x$  in Fig. 2.6 is reversed. The discharger can also be regarded either as a load seen by the solar array or as a source seen by the load.

The battery charger is activated when the bus voltage is higher than the charger's reference voltage, and the battery is not fully charged. For the battery charger, there exist three different modes of operation: bus voltage regulating mode, charging current regulating mode, and trickle charge mode. Before the charging current reaches a preset charge current limit, the bus voltage is regulated by the charger. This mode is called the charger's bus voltage regulation mode. When the charger is in this mode, the function of the battery charger is the same as for the shunt regulator from the viewpoint of bus dynamics. During this mode, the battery charger takes the excess power from the solar array to regulate the bus voltage, as well as to charge the battery. Therefore, the same analysis is valid for the charge mode if the transconductance of the shunt and its reference voltage are replaced by those of the charger. When the charging current reaches a preset current limit and the solar array still produces excess power, the charging current is regulated at its limit value. This period is called the charger's charge current regulation mode. When the charger operates in this mode, the bus voltage is not regulated by the charger. The bus voltage then rises due to the excess solar array power, and the system settles in the shunt mode. In this mode the charger be-

haves as a constant current sink load to the solar array source, and dynamics of the bus are determined by the characteristics of the shunt regulator.

The system operating condition is subject to change due to constantly varying load power consumption and the solar array's power generation. A central control unit constantly monitors the bus voltage and activates the appropriate power conditioning equipment. The solar array system's modes of operation are analyzed as the solar array's output power changes.

#### **2.4.1 Sunlight to Eclipse Transition Analysis**

The equivalent load line seen by the solar array source can be constructed as shown in Fig. 2.10. Since the battery charger is not involved in this transition, the equivalent load line includes the constant power load, the battery discharger, and the shunt regulator.

Using Fig. 2.10, the system's mode of operation is described as follows: starting from the shunt mode of Curve S1 and the corresponding operating point A, the operating point travels along the shunt line until the solar array power decreases to Curve S2. During this interval, there exists only one equilibrium point in the system. As the solar array power further decreases from Curve S2, there exist three equilibrium points between Curve S2 and S4 (i.e., Curve S3). However,

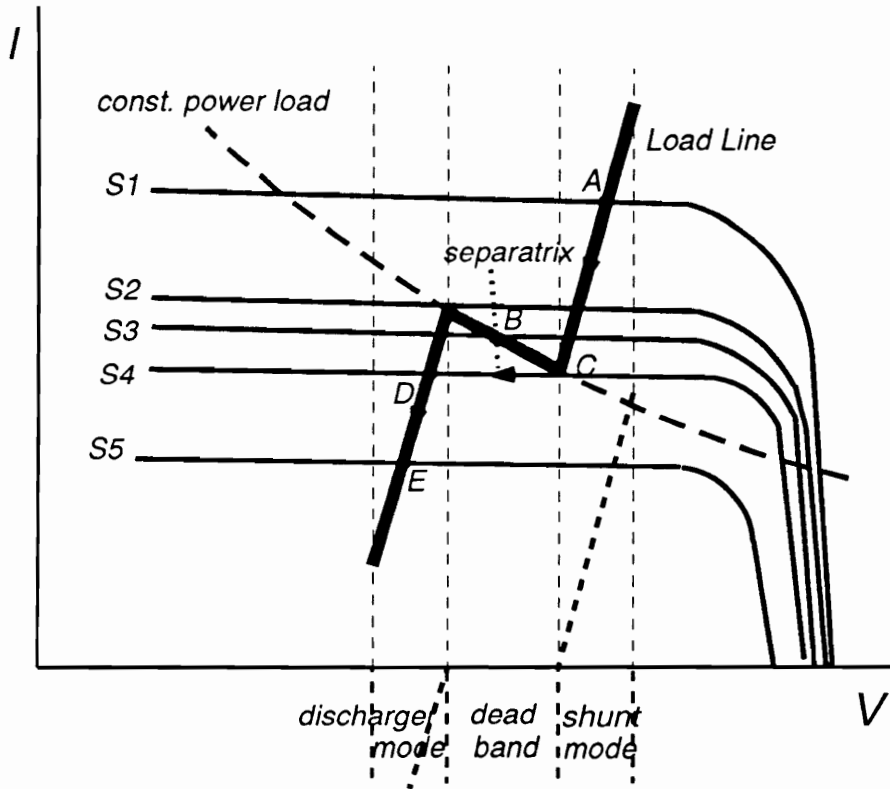


Figure 2.10. Graphical Analysis of Sunlight to Eclipse Transition

since the previous operating point at any instant during this interval remains on the right hand side of the separatrix (the line through Point B for Curve S3), the operating point remains on the shunt line until Point C. As soon as the solar array power decreases beyond Point C, the bus voltage drops through a deadband to Point D, which is the only equilibrium point and is stable. Thus the battery discharger is turned on at a finite load condition. A deadband is required between the shunt and battery-discharger reference voltage to avoid undesired overlapping operation. The transient behavior during the deadband mode depends on the size of the bus filter capacitor, the cable inductance, and the transconductance gain of the battery discharger.

For system simulations, the following models are used: solar arrays, batteries, a linear shunt regulator, a buck switching regulator with an input filter as a battery charger, a boost regulator with a secondary output filter as a battery discharger, and a constant power load. Each piece of power conditioning equipment has a compensation network for the error amplifier to ensure stability of the local regulators as well as of the system bus.

Figure 2.11 shows the result of simulation of this case. The illumination level of the solar arrays is set to be linearly time-varying from curve S1 (shunt active mode) to curve S5 (battery discharging mode). As the illumination level decreases, the solar array current decreases. The shunt regulator current then decreases to regulate the bus voltage. As soon as the shunt current reaches zero, the bus voltage drops rapidly. This period represents the deadband mode. When the

bus voltage reaches a preset value (118 V), the battery discharger turns on and regulates the bus voltage. The shunt regulator and battery discharger are designed to ensure small-signal stability for all operating conditions during this transition.

### 2.4.2 Eclipse to Sunlight Transition Analysis

Figure 2.12 shows the equivalent load line, including the battery charger, during the eclipse to sunlight mode. The trajectory of the system's operating point in this transition period is different from that of the sunlight to eclipse mode. Curve S5 and the corresponding operating point E again represent the system in the battery discharging mode. As the solar array output power increases until it reaches Curve S4, the operating point travels on the battery discharger line. Between S4 and S2, there exist three equilibrium points. However, since the initial condition for any given time during this interval resides on left-hand side of the separatrix, the operating point stays on the battery discharger line until Point D'. Thus the battery discharger turns off at its no-load condition. As soon as the solar array power increases beyond Point D', the bus voltage rises to Point F through the deadband between the battery discharger and charger line. Thus the charger turns on at the finite current. Between Point F and G, the bus voltage is regulated by the charger, and the shunt is still inactive. Point



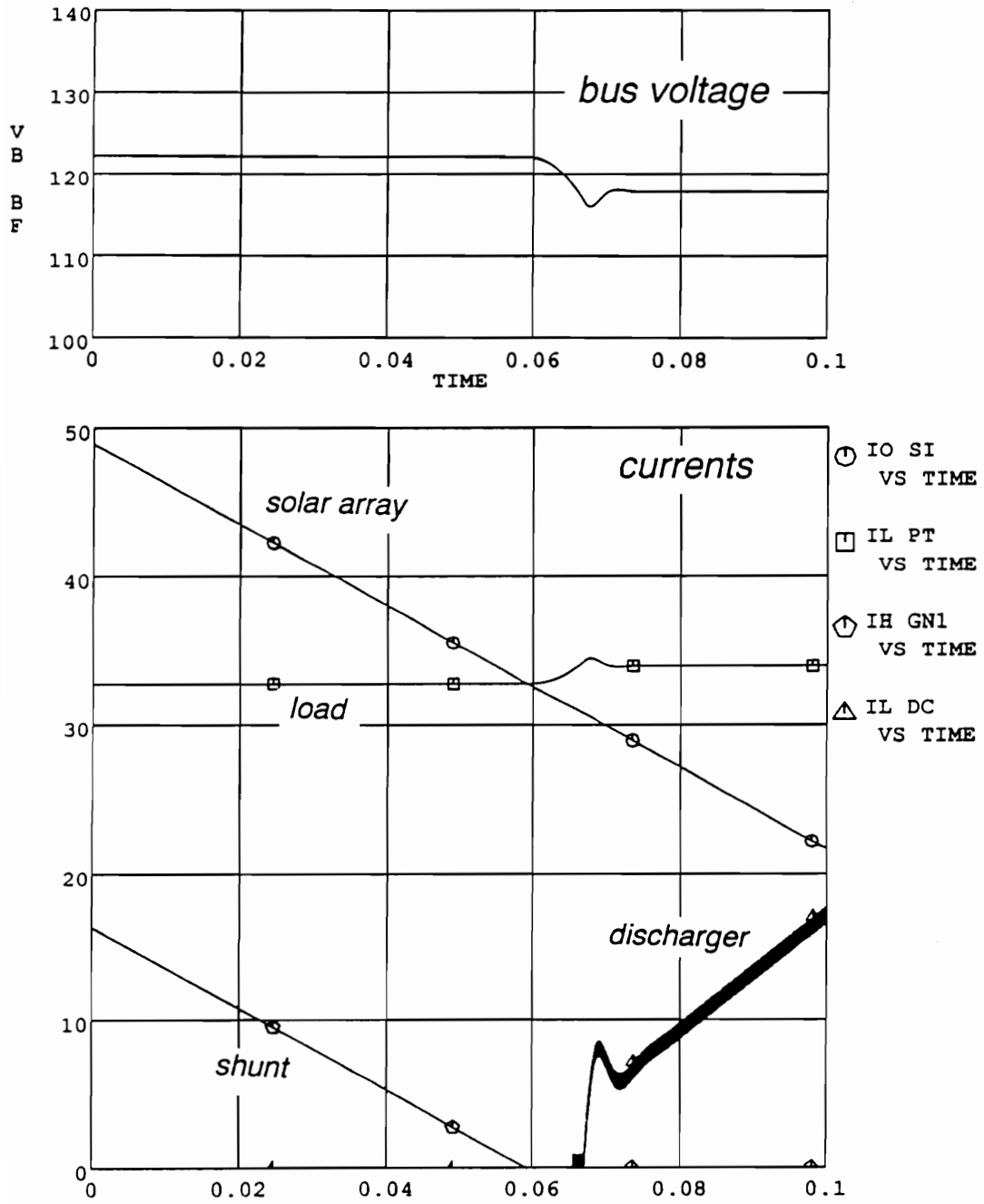


Figure 2.11. Simulation Results of Sunlight to Celipse Transition

G represents the charge current reaching its preset maximum current. As the solar array power further increases to Curve S1, the bus voltage rises to Point A through the deadband between the charger's voltage regulation and shunt modes. This deadband is needed to avoid turning on the shunt regulator before the charger reaches the maximum charging current.

During the charge current regulation mode, the charger can be treated as a constant current load to the system. Thus excessive power is absorbed by the constant battery-charging current and shunt current, and the bus voltage is regulated by the shunt regulator. When the battery is fully charged, the shunt takes most of the excessive power, except for the trickle charge current to the battery. The system's operating condition then returns to the shunt mode in Fig. 2.10, completing the cycle.

Figure 2.13 shows the simulation results of the transition from the eclipse to sunlight condition. As illumination increases, the solar array current increases. Then the discharger current decreases to regulate the bus voltage. As soon as the discharger current becomes zero, the bus voltage rises rapidly during a dead band mode. When the bus voltage reaches a preset value (120 V), the battery charger turns on and regulates the bus voltage. As the illumination is further increased, the charge current reaches a preset current limit (30 A) and is regulated at the limit value. Then, due to the excessive solar array power, the bus voltage rises until the shunt regulator is turned on. After the shunt regulator is activated, the bus voltage is regulated with a shunt reference voltage (122 V). The design of

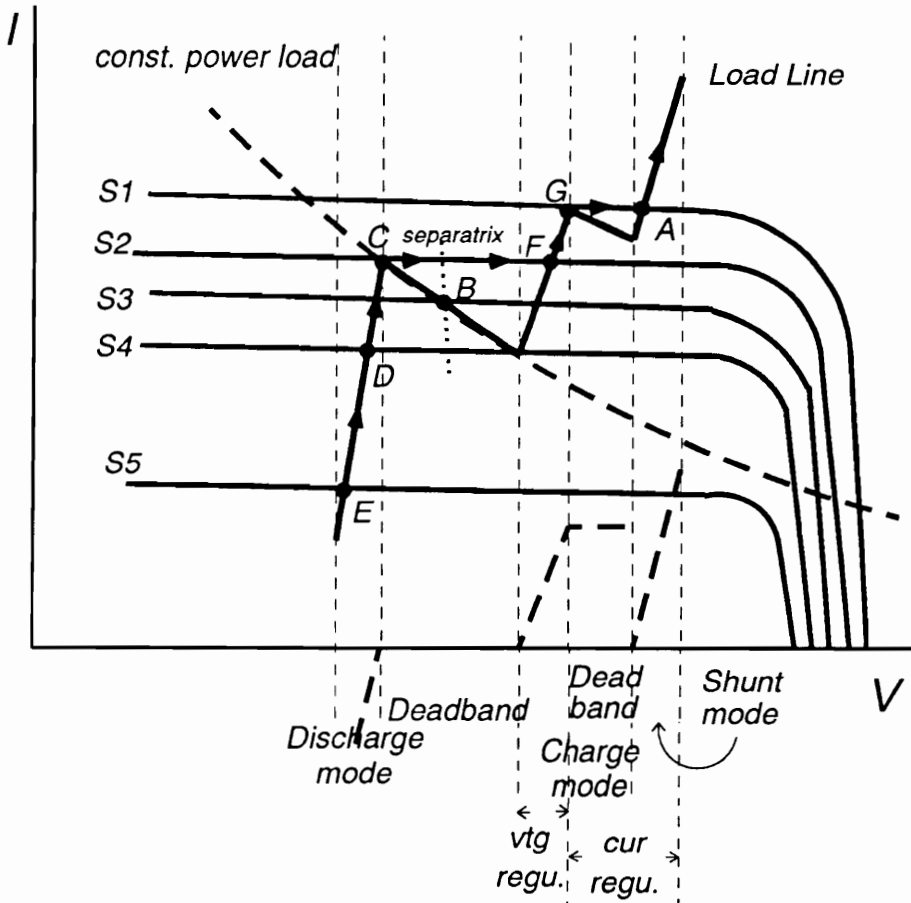


Figure 2.12. Graphical Analysis of Eclipse to Sunlight Transition

each regulator must not only ensure its stability, but also a fast response time so to avoid overlapping operation between the operating modes.

## 2.5 *Peak Power Tracking System*

The Peak power tracking (PPT) system uses a series switching regulator between the solar array and the spacecraft loads as shown in Fig. 2.14. The solar array's output voltage is regulated at its peak power point by the series converter (typically buck type). A peak power tracker continuously calculates the peak power point and sets a voltage reference to the regulator. The converter then regulates its input voltage according to the provided reference voltage by controlling the duty ratio.

Various techniques are employed for the peak power tracking algorithm [39 - 47]. One popular technique is to calculate  $\frac{dp}{dv}$  of the solar array from sensed voltage and current information using a microprocessor. As shown in Fig. 2.15, the  $\frac{dp}{dv}$  of the solar array is positive in the current source region and negative in the voltage source region. In order to track the peak power point, the reference

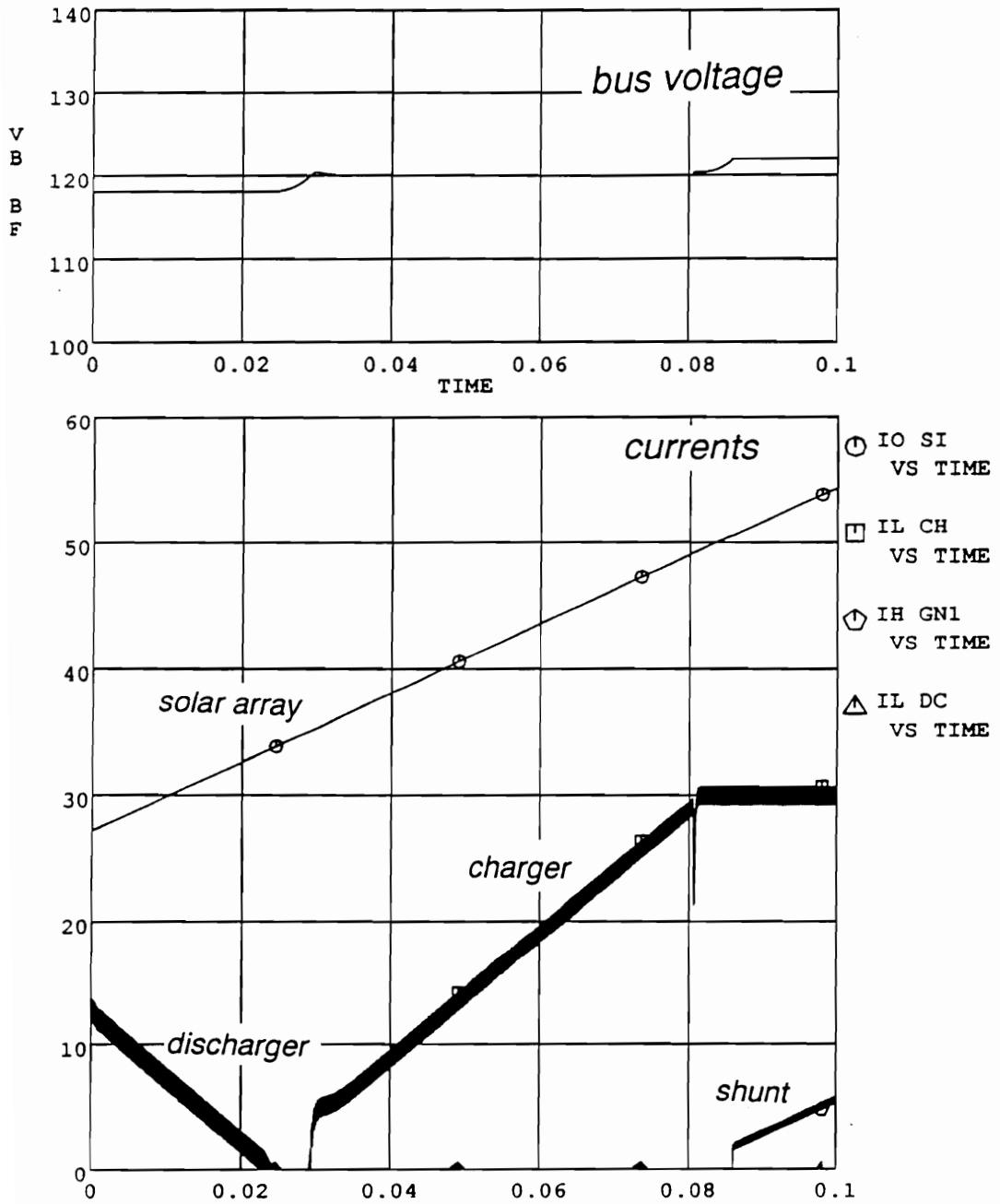
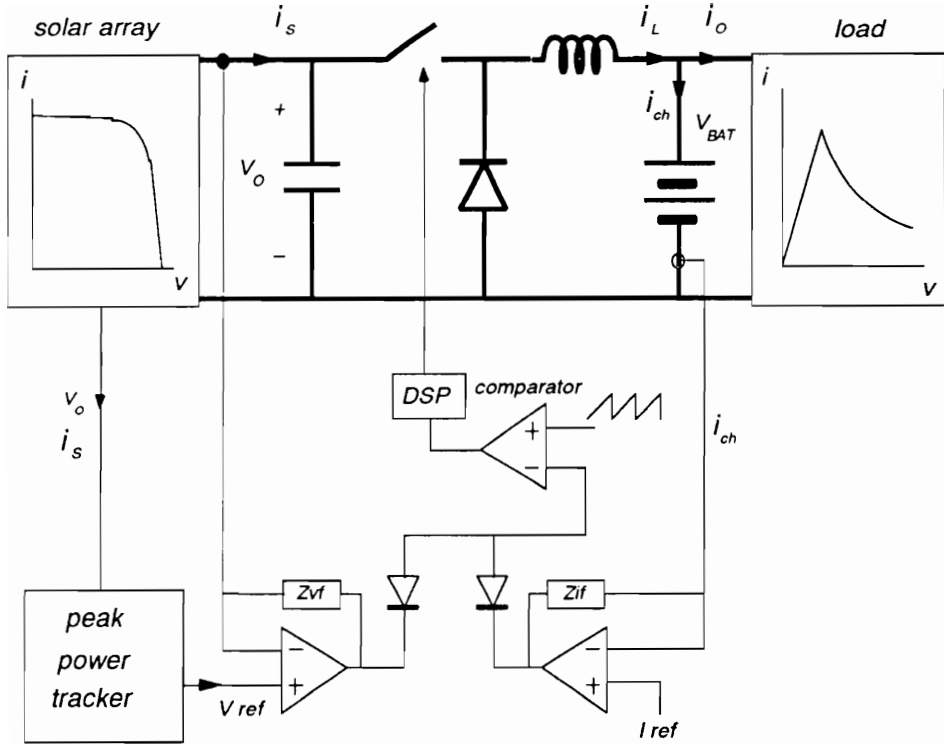


Figure 2.13. Simulation Result of Eclipse to Sunlight Transition



**Figure 2.14. Circuit Diagram of PPT System**

voltage to the converter is increased if  $\frac{dp}{dv}$  is positive, and if  $\frac{dp}{dv}$  is negative, reference voltage is reduced until  $\frac{dp}{dv}$  becomes zero.

The peak power tracker is activated after eclipse when the state of charge (SOC) of the battery is low, and it is disabled when the battery is fully charged. The peak power tracker is also activated when the load demand is greater than the solar array output. When not in operation, the converter is used as a battery charge current regulator.

Figure 2.16 shows the solar array's operating point in the PPT system. Curve C1 is a combined load line of battery and constant power load as seen by the solar array when the system operates in the peak power tracking mode. The solar array operating point is the peak power point, P. When the battery is fully charged, the peak power tracker is disabled. Then the converter is used for a current regulator (trickle charger). Curve C2 represents the load line as seen by the solar array during this mode. Three equilibrium points A, B, and C exist in C2. However, the solar array operating point moves from P to A, because the initial condition, P, was on the right-hand side of the separatrix.

PPT system is an inherently unregulated bus system and the distribution bus voltage is determined by the battery voltage. A voltage regulator may be added between the battery and load to achieve a regulated bus.

For the system simulation, the following models are used: solar array, battery, peak power tracker, buck switching regulator as a peak power tracking converter,

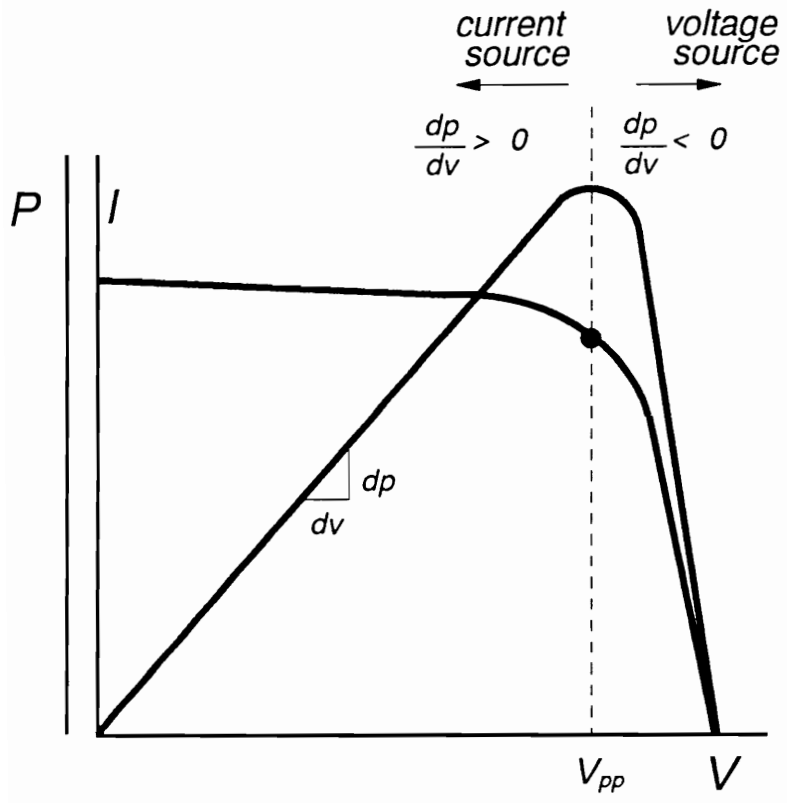
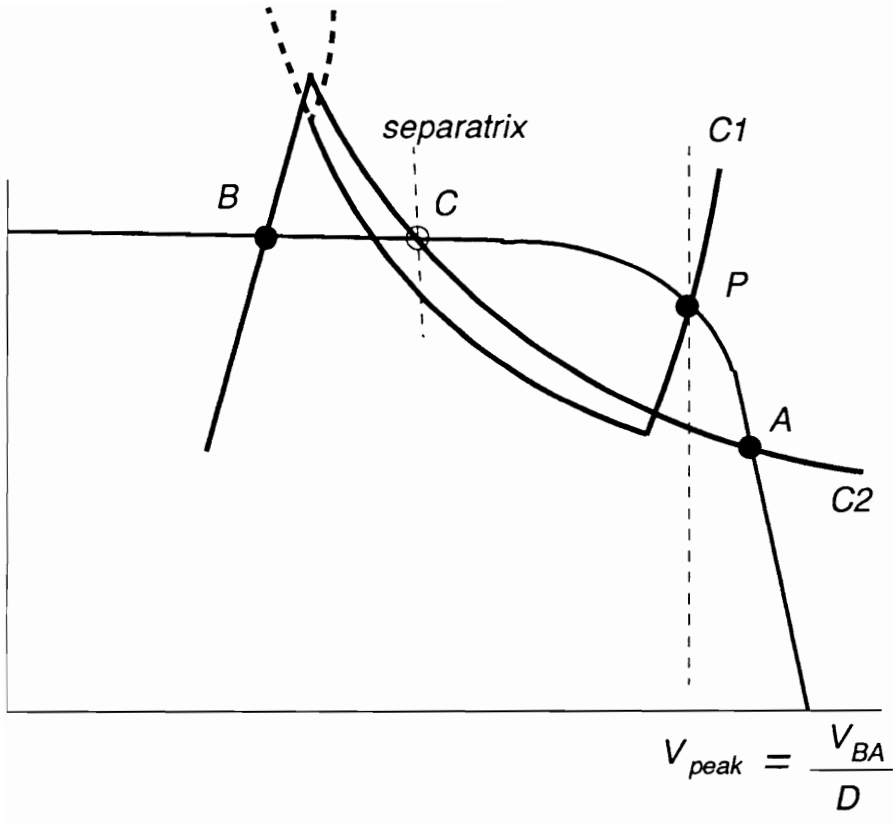


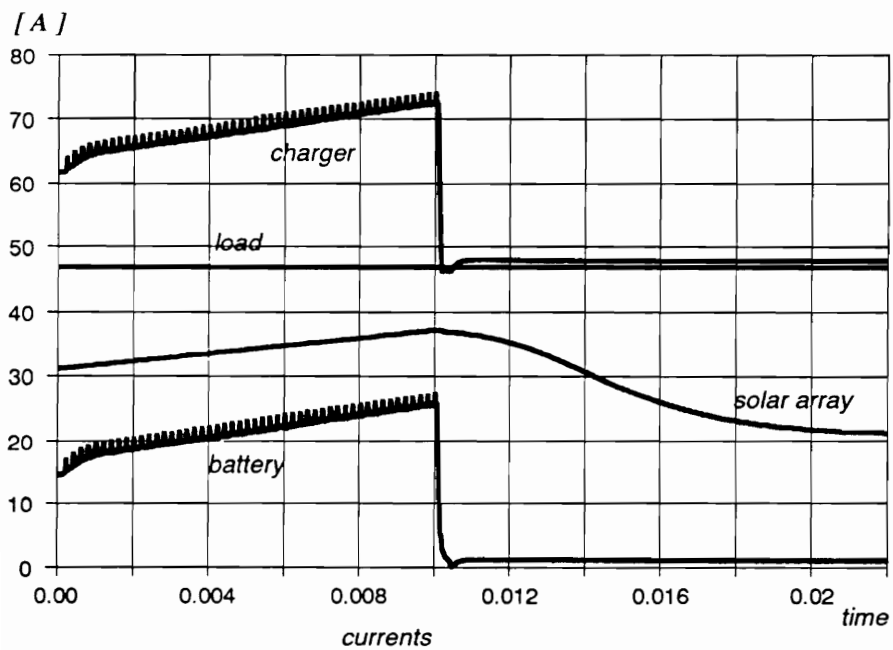
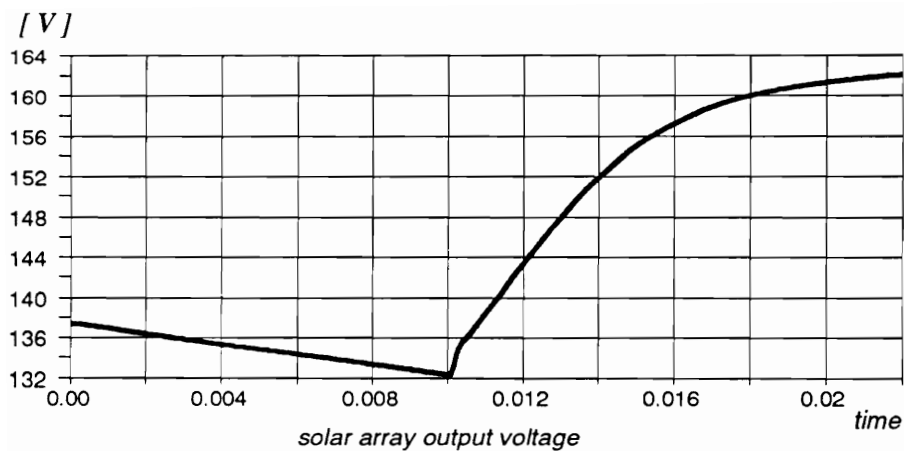
Figure 2.15. Solar Array Characteristics





**Figure 2.16. Operating Points in PPT System**

and constant power load. Figure 2.17 shows the simulation results of the transition from eclipse to sunlight condition. Initially, the solar array is operating in the PPT mode. As illumination increases, the solar array operating point follows the peak power point. The solar array current increases, and voltage decreases a little. Whenever the peak power tracker updates the reference voltage in a discrete fashion, current spikes appear in the inductor current of the converter. At 10 ms, the peak power tracker is disabled. The solar array output voltage increases rapidly and converges to the voltage source region (Point C2 in Fig. 2.16). The battery charge current is regulated at 3 A.



**Figure 2.17. Simulation of Eclipse to Sunlight Transition**

## 2.6 *Summary*

The Large-signal dynamics of the system's mode of operation for various spacecraft power system configurations are analyzed employing the qualitative graphical method. The effective source line and load line of the solar array power system are defined to analyze the stability of the system's operating point. The use of stability information on each equilibrium point and the separatrix clearly characterize the large-signal behavior of the system. The graphical method also provides physical insights to the large-signal dynamics of the system. The trajectory of the system's operating point during the transition from the sunlight to eclipse mode is different than that of the transition from the eclipse to sunlight mode.

Large-signal characteristics of the unregulated bus system and the sunlight regulated bus system have been reviewed. In the unregulated bus system, the bus is directly connected to the solar array and battery, and the bus voltage varies widely with variation of the output voltages of the solar array and battery. In the sunlight regulated bus system, during the period of the eclipse-to-sunlight mode, the battery lock-up situation occurs. The battery lock-up problem was discussed.

In the DET system, considering the degradation in the solar array power generation, the operating point of the solar array should stay in the current source region, which is the unstable region without power conditioning equipment. The

system can be stabilized in this region when a power conditioning regulator is employed. The regulator's transconductance can be treated as part of either the source or the load. The equivalent source characteristic seen by the constant power load and the equivalent load characteristic seen by the solar array output are characterized. With the regulators, the system can be viewed as a stiff voltage source with a constant power load or as a solar array current source with a stiff current sink.

For the PPT system, graphical analysis illustrates that after the peak power tracker is deactivated, the solar array's operating point moves to the stable equilibrium point in the voltage source region.

The system's modes of operation throughout an orbit cycle, including deadband modes, are simulated using developed component models. Appendix provides component and system models used in the simulations.

## **Chapter 3**

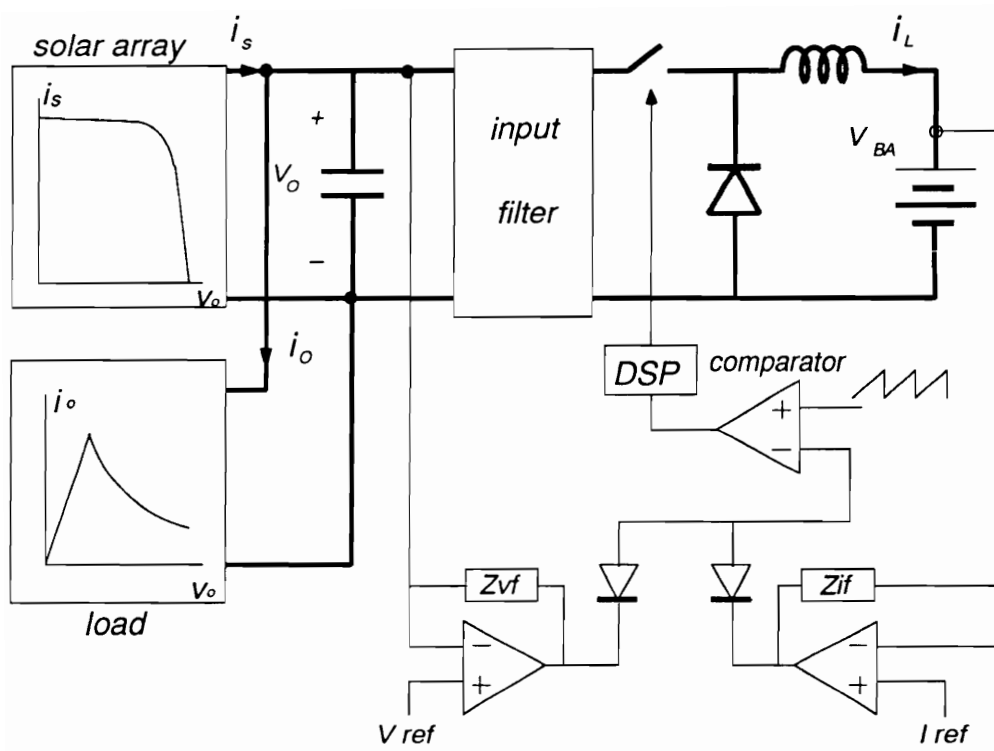
# **Small-Signal Analysis of the Charger in Bus-Voltage Regulation Mode**

### ***3.1 Introduction***

For the DET system employing the regulated bus configuration, when there is sufficient solar array current to supply the spacecraft loads, yet insufficient solar array current to charge the batteries at commanded rates, the spacecraft bus is regulated by controlling the charge current to the batteries in a method similar to a shunt regulator. This mode is called the charger's bus voltage regulation mode.

Because of advantages in weight and efficiency over series pass linear regulators, switching regulators are widely used in battery charger systems. Figure 3.1 shows a schematic of the battery charger subsystem which uses buck converter topology. The bus voltage,  $v_o$ , is regulated at the charger's preset reference voltage by control of the duty cycle. Thus the charger draws an appropriate current, which is the difference between the solar array output current and the load current at the bus voltage, to balance the power and thereby maintain the bus voltage regulation. In the charger system, the solar array is the power source supplying the charge current to the battery, thus power flows from the bus to the battery. However, as far as small-signal dynamics are concerned, it is important to realize that *the input variable is the battery voltage used as a fixed voltage source, and the output variable to be controlled is the bus voltage,  $v_o$* . The dynamics and design strategies of the charger are quite different from those of conventional switching regulators.

Switching regulators are highly nonlinear, as is the output characteristic of the solar array. A nonlinear charger, when coupled with a nonlinear solar array source and nonlinear load, results in a nonminimum phase system and its dynamics are quite different from those of conventional switching regulators. The small-signal dynamics of the charger thus depend on the equivalent dynamic impedance characteristics seen by the charger at the bus (output terminal). Furthermore, since the charger operates in both DCM and CCM, both modes of operation should be considered for the controller design. In this chapter, small-signal dynamic characteristics of battery charging system of the DET system in



**Figure 3.1. Circuit Diagram of the DET Charger System**



the bus voltage regulation mode of operation are modeled and analyzed to facilitate design of the control-loop for optimum performance and stability.

In Section 3.2, terminal characteristics of the charger are defined. The dc load and the linear equivalent dynamic ac load for the charger are derived by linearizing the nonlinear solar array output and the constant power load characteristics. The voltage-mode controlled (Section 3.3) and the current-mode controlled charger regulators are modeled and analyzed for both CCM and DCM. Design strategies for an optimum feedback compensator for the charger operating in both CCM and DCM are discussed. In Section 3.5, the nonminimum phase nature of the charger system is analyzed and problems associated with the conditionally stable system are investigated.

## ***3.2 Modeling of Terminal Characteristics***

Spacecraft power systems include many load converters which regulate their output voltages at different levels according to the requirements of the payloads. Assuming the load converters are lossless, the spacecraft load can be considered as a constant power load seen by the bus. During the bus voltage regulation

mode, the equivalent dynamic impedance is the parallel combination of the output impedance of the solar array and the input impedance of the constant power load at a given operating voltage.

As shown in Fig. 3.2, the solar array output and the load characteristics are represented by nonlinear functions. For such nonlinear I-V curves, the equivalent dc resistance and the dynamic ac resistance at a given operating point are quite different. Also, the dynamic ac resistance varies with the operating condition.

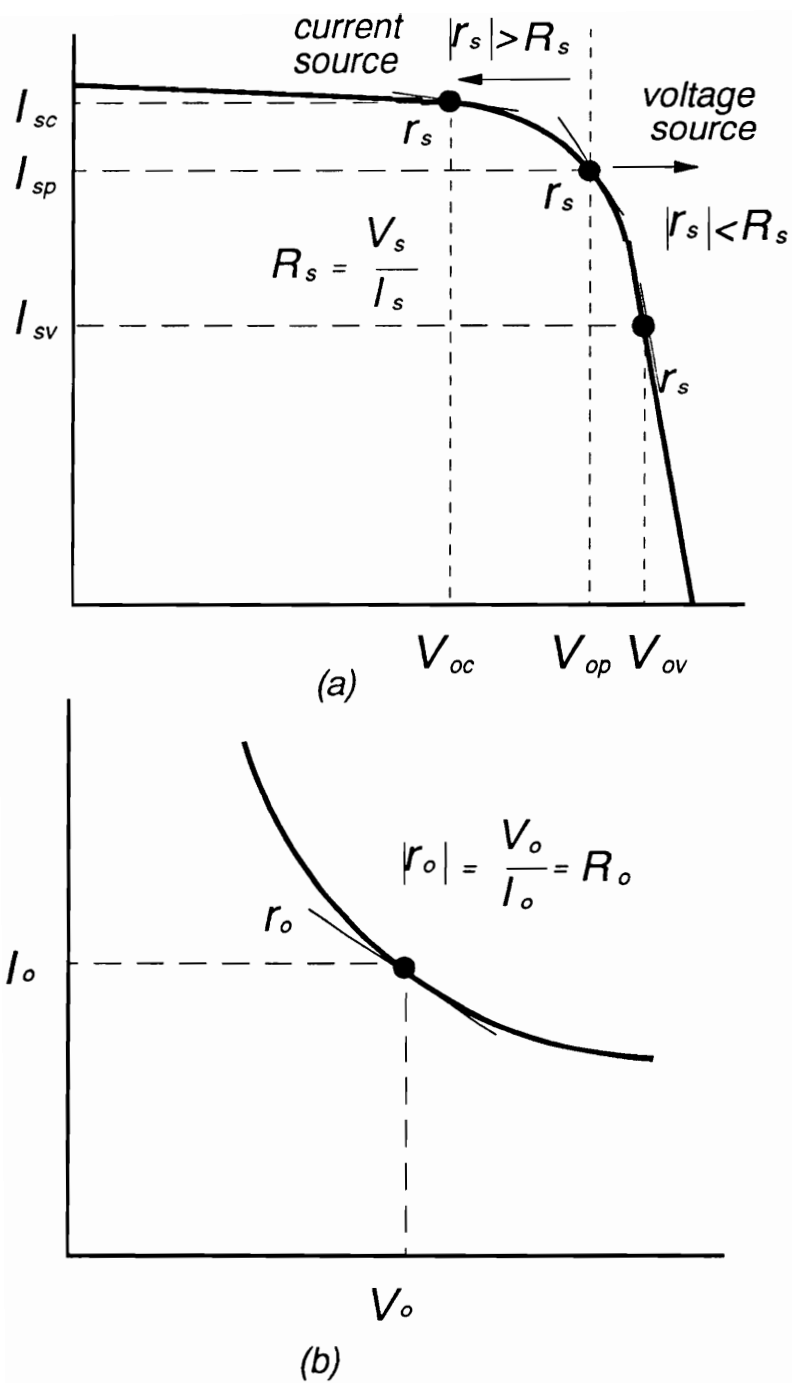
To derive the small-signal dynamic output impedance of the solar array, a nonlinear function representing the solar array output is linearized by taking the first order term of the Taylor series :

$$\begin{aligned} i_s &= f(v_o) \simeq f(V_o) + \frac{df(v_o)}{dv_o} \hat{v}_o \\ &= I_s + \frac{1}{r_s} \hat{v}_o \end{aligned} \quad (3.1)$$

where  $r_s$  is the dynamic resistance (tangential slope) of the solar array I-V curve at a given operating point  $(V_o, I_s)$ . Notice that the value of  $r_s$  is negative. The magnitude of  $r_s$  varies widely depending on the operating region of the solar array output. For the solar array, output power is:

$$p_s = i_s v_o \quad (3.2)$$

At the peak power point, the differential of the power becomes zero.



**Figure 3.2. Dynamic Resistance and DC Resistance**  
 (a) solar array  
 (b) constant power load

$$\begin{aligned}
dp &= \frac{\partial p_s}{\partial i_s} di_s + \frac{\partial p_s}{\partial v_o} dv_o \\
&= v_o di_s + i_s dv_o \Big|_{v_o = V_{op}, i_s = I_{sp}} = 0
\end{aligned} \tag{3.3}$$

From Eq. (3.3), dynamic resistance of a solar array at the peak power point becomes:

$$r_s = \frac{dv_o}{di_s} = -\frac{V_{op}}{I_{sp}} \equiv -R_{sp} \tag{3.4}$$

where  $R_{sp}$  is the dc resistance of the solar array at the peak power point. The relationship between dynamic resistance and dc resistance of the solar array, as shown in Fig. 3.2(a), is:

$$\begin{aligned}
|r_s| &> R_s \quad \text{in the current source region} \\
|r_s| &= R_s \quad \text{at the peak power point} \\
|r_s| &< R_s \quad \text{in the voltage source region}
\end{aligned} \tag{3.5}$$

Similarly, for the constant power load,

$$\begin{aligned}
i_o &= f(v_o) \simeq f(V_o) + \frac{df(v_o)}{dv_o} \hat{v}_o \\
&= I_o + \frac{1}{r_o} \hat{v}_o
\end{aligned} \tag{3.6}$$

where  $r_o$  is the dynamic resistance (tangential slope) of the constant power load at a given operating point. For the constant power load, the differential of power

is always zero. Thus the magnitude of the dynamic resistance of a constant power load is the same as the dc resistance at a given operating point, as shown in Fig. 3.2(b).

$$r_o = \frac{dv_o}{di_o} = -\frac{V_o}{I_o} \equiv -R_o \quad (3.7)$$

When the solar array feeds a constant power load, following relations are shown:

$$\begin{aligned} |r_s| &> |r_o| && \text{in the current source region} \\ |r_s| &= |r_o| && \text{at the peak power point} \\ |r_s| &< |r_o| && \text{the voltage source region} \end{aligned} \quad (3.8)$$

Since the solar array degrades during its lifetime, the load power level is set at the maximum available power of the solar array in its end-of-life. Thus in the DET system the regulation voltage is set near the maximum power point of the solar array's end-of-life I-V characteristic. Therefore, during the mission period the solar array's operating point resides in the current source region.

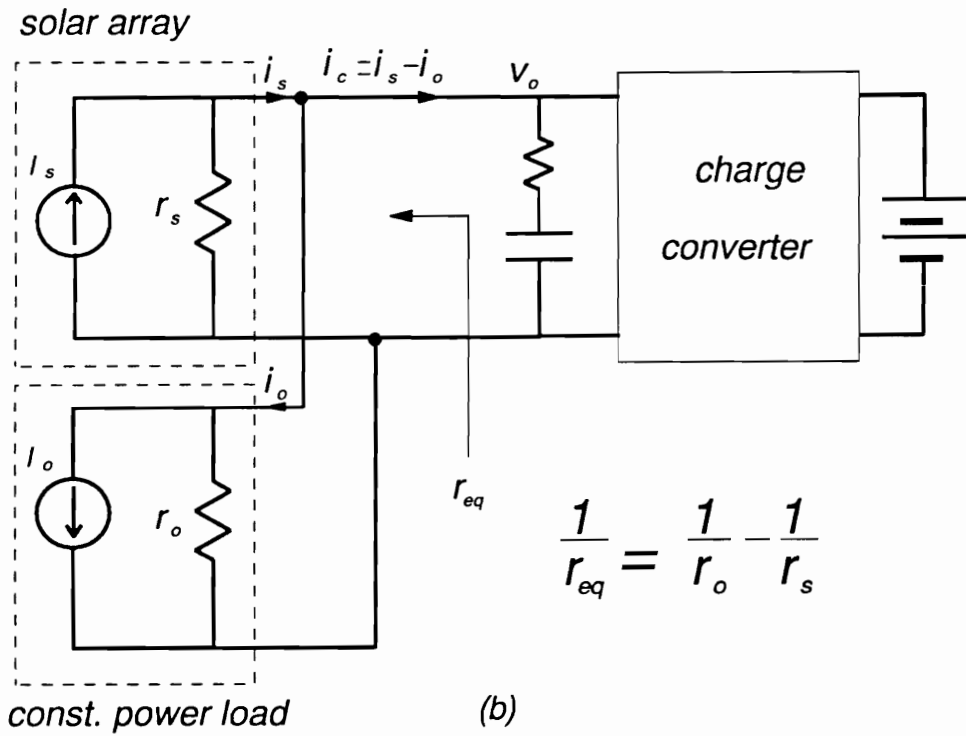
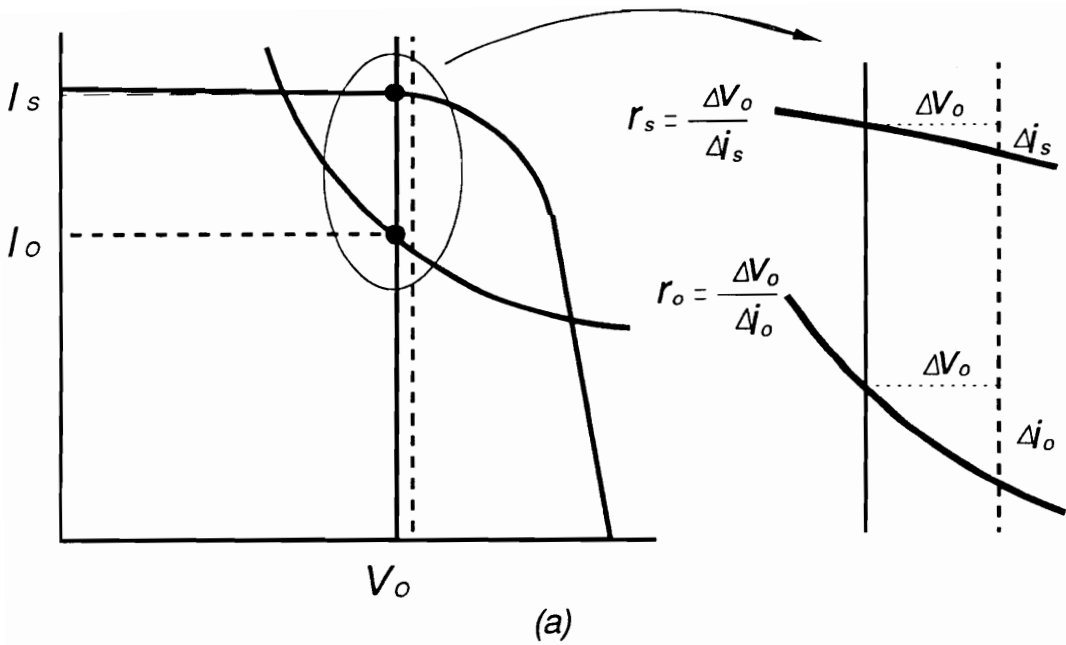
Dynamic resistances of the solar array and the constant power load in the current source region are shown in Fig. 3.3(a). Change in the bus voltage  $\Delta v_o$  in a positive direction results an increase in the input current to the charger  $\Delta i_c$ . This shows that the dynamic impedance seen by the charger,  $r_{eq} = \frac{\Delta v_o}{-\Delta i_c}$  should be negative. Notice that the negative sign comes from the direction of  $i_c$  defined in the figure. The dc load resistance seen by the charger is:

$$R_{dc} = \frac{V_o}{I_c} = \frac{V_o}{I_s - I_o} \quad (3.9)$$

The linearized terminal characteristic of the charger is shown in Fig. 3.3(b). The equivalent impedance,  $r_{eq}$ , seen by the charger is given by:

$$\frac{1}{r_{eq}} = \frac{-di_c}{dv_o} = \frac{d(i_o - i_s)}{dv_o} = \frac{1}{r_o} - \frac{1}{r_s} \quad (3.10)$$

Since the magnitude of  $r_s$  is greater than the magnitude of  $r_o$ , and both  $r_o$  and  $r_s$  are negative, the equivalent resistance,  $r_{eq}$ , becomes negative, and the magnitude of  $r_{eq}$  is greater than  $r_o$ . Notice from Eqs. (3.9) and (3.10) that the dc load and small-signal ac load are different.



**Figure 3.3. Equivalent Terminal Characteristics of the Charger**  
 (a) definition of dynamic resistance  
 (b) equivalent dynamic resistance

### 3.3 Modeling, Analysis and Design of the Charger with Voltage-Mode Control

#### 3.3.1 Continuous Conduction Mode

##### Power stage modeling

Figure 3.4 shows two switched networks of the buck type charge converter operating in continuous conduction mode. State variables  $x = [i_L \ v_C]^T$ , and input and output variables,  $v_{BA}$  and  $v_o$ , are defined. The state-space averaging technique [47] is employed to derive the small-signal linear model.

DC gains of the converter, assuming lossless operation, are given by:

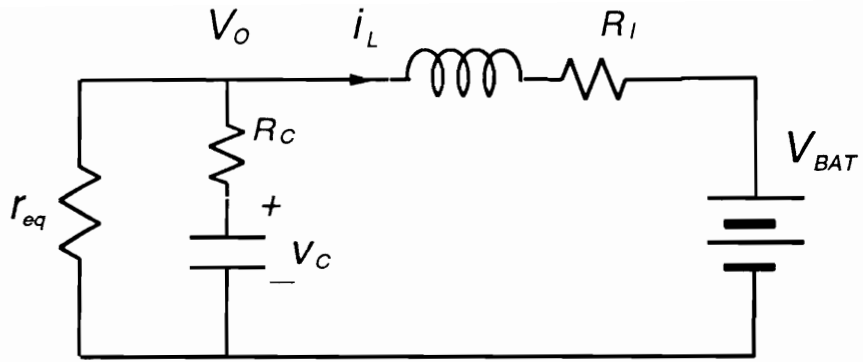
$$V_o = \frac{V_{BA}}{D} \quad (3.11)$$

$$I_L = \frac{(I_s - I_o)}{D} \quad (3.12)$$

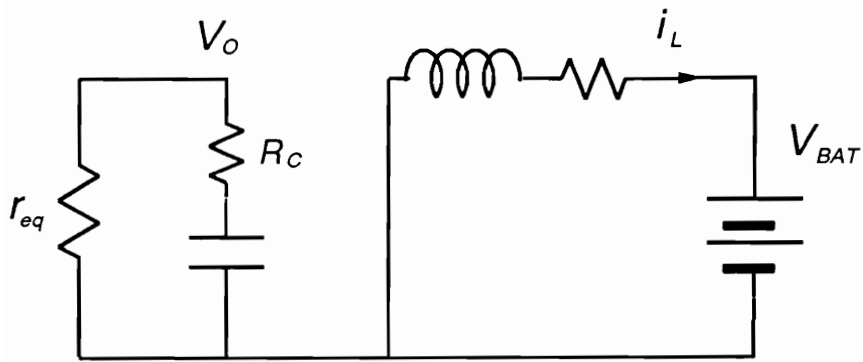
The control-to-bus voltage small-signal transfer function,  $F_{dv}$ , becomes:

$$F_{dv} = \frac{\hat{v}_o}{\hat{d}} = \frac{-\frac{V_{BA}}{D^2} (1 + s \frac{I_L L}{V_{BA}}) (1 + s R_c C)}{1 + s [(\frac{R_l}{D^2} + R_c) C + \frac{L}{D^2 r_{eq}}] + s^2 \frac{LC}{D^2}} \quad (3.13)$$





$dTs$



$d'Ts$

**Figure 3.4. Switched Equivalent Circuit of Charger**

where  $R_c$  and  $R_l$  represent ESR of the bus capacitor and the charge inductor, respectively.

Although the charger has a buck converter topology, its dynamic behavior is similar to that of a boost converter. This is because the two switched networks in Fig. 3.4 are identical to those of a boost converter except that the switch's on-time and off-time are interchanged. Thus it is expected that Eq. (3.13) be similar to the control-to-output transfer function of the boost converter. However, since power flows from the solar array to the battery, the steady-state dc inductor current direction is reversed from that of the boost converter. As shown in Eq. (3.13), the location of the zero is determined by the dc operating condition, not by the terminal ac resistance  $r_{eq}$ . Thus the  $F_{dv}$  of the charger has a moving left-half-plane (LHP) zero instead of the right-half-plane (RHP) zero of the boost converter. Another important aspect of Eq. (3.13) is that the dc gain of  $F_{dv}$  is negative for all operating regions of the solar array. This can be easily explained since an increase in the duty cycle results in a decrease in the bus voltage when the battery voltage is constant.

When the solar array operates in the voltage source region, both  $r_o$  and  $r_s$  are negative, and  $|r_o| > |r_s|$ . Thus  $r_{eq}$  is positive and the transfer function has a complex LHP pole pair. However, in the current source region of the solar array, since  $r_{eq}$  is negative, the s-term coefficient in the denominator can be negative (a complex RHP pole pair) at a very heavy load or when the parasitic terms,  $R_c$  and

$R_l$ , are small. Dynamics of the closed-loop system will be investigated in the following sections for this open-loop unstable case.

The control-to-charge current transfer function is:

$$\begin{aligned}
 F_{di} = \frac{\hat{i}_L}{\hat{d}} &= \frac{\frac{V_o}{L} (s + \frac{1}{C r_{eq}}) - \frac{D I_L}{LC}}{\frac{D^2}{LC} [1 + s\{(\frac{R_l}{D^2} + R_c)C + \frac{L}{D^2 r_{eq}}\} + s^2 \frac{LC}{D^2}]} \\
 &= \frac{I_k}{D^2} \frac{(1 + s \frac{V_o C}{I_k})}{1 + s\{(\frac{R_l}{D^2} + R_c)C + \frac{L}{D^2 r_{eq}}\} + s^2 \frac{LC}{D^2}}
 \end{aligned} \tag{3.14}$$

where

$$I_k = \frac{V_o}{r_{eq}} - D I_L \tag{3.15}$$

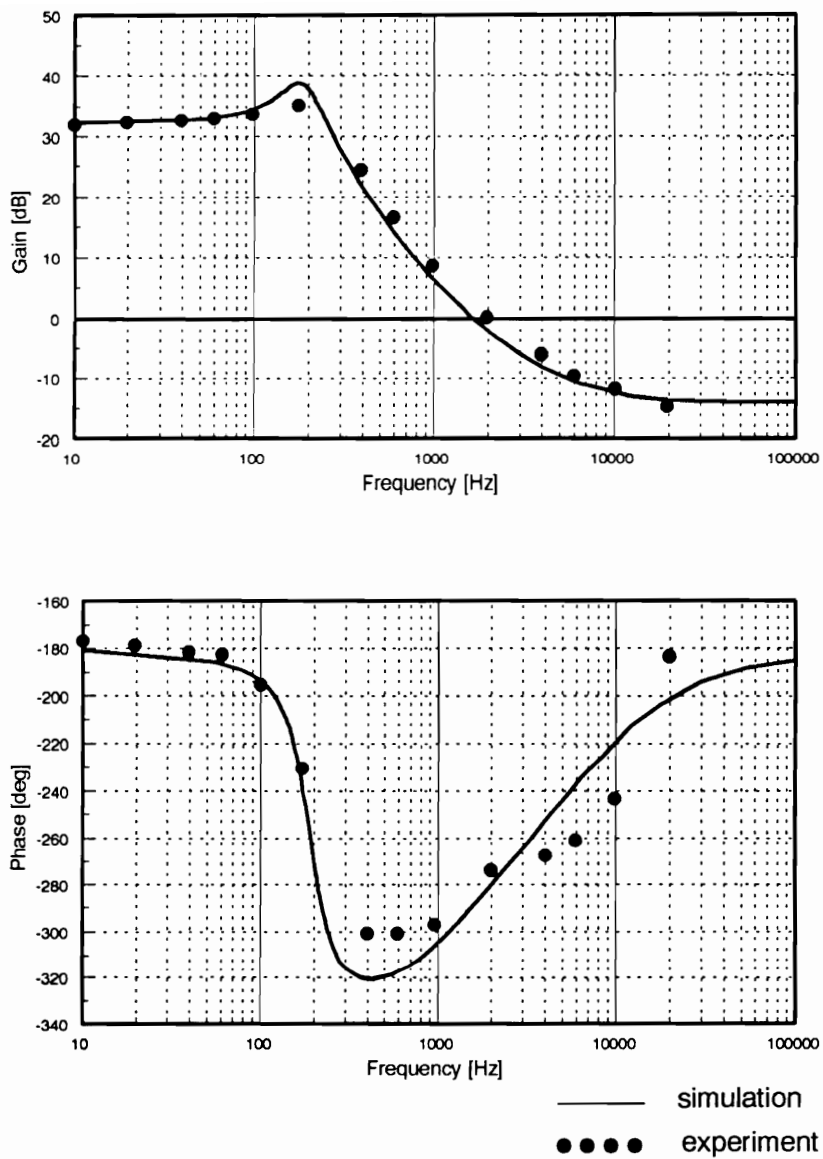
The dc gain and the location of zero are proportional to  $I_k$ , which is a function of both dc operating condition  $I_L$  and the dynamic resistance  $r_{eq}$ . When the solar array operates in the current source region where  $r_{eq}$  is negative,  $I_k$  is always negative. This results in a negative dc gain and a RHP zero, again this is quite different from the conventional converter system. The interpretation of Eq. (3.14) will be elaborated in the design of the current-mode control in Section 3.4.

## Experimental verification

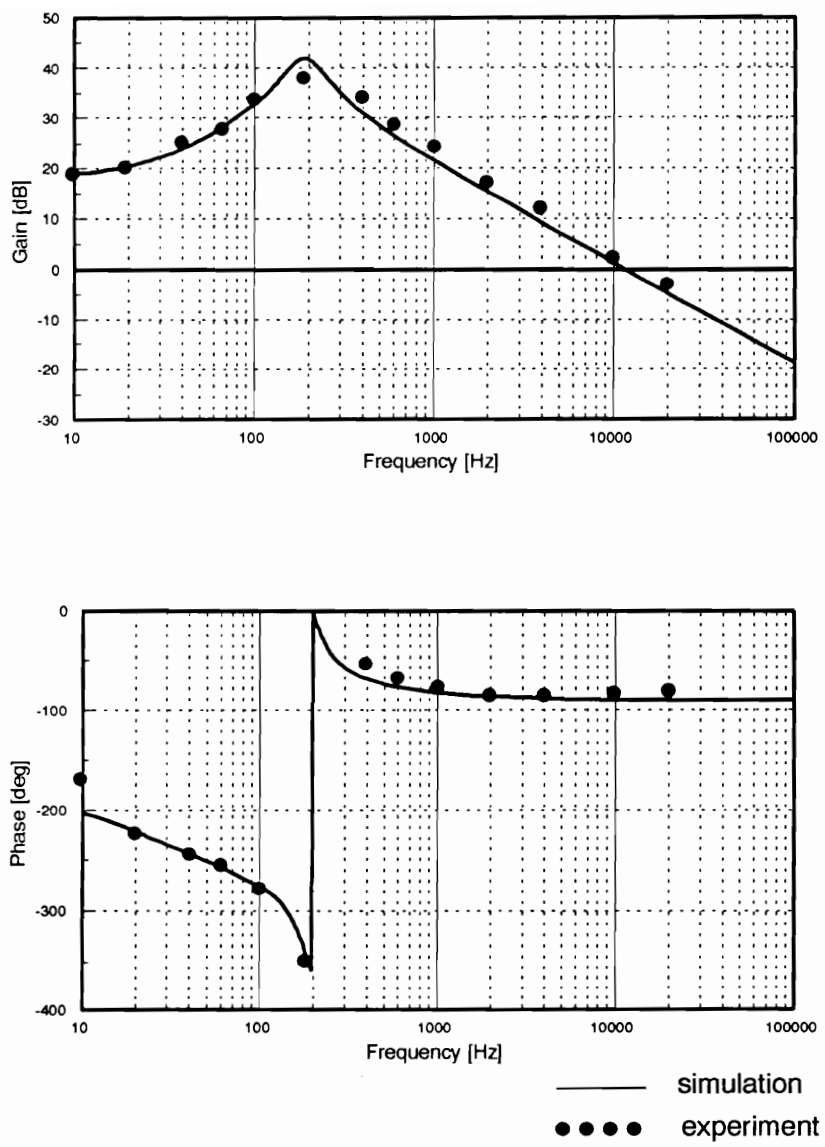
An experimental circuit was built to verify the results of the analysis. An active current source circuit with a controllable output resistance was designed to simulate the solar array output. The output resistance was set to match  $r_s$  in the current source region of the solar array. The solar array operating voltage was set at 13.6 V, and the corresponding output resistance was 50  $\Omega$ . An active load and a power supply were used to simulate a constant power load and the battery, respectively. The battery voltage was set at 5 V. The bus filter capacitance and the charger inductance were 500  $\mu\text{F}$  and 200  $\mu\text{H}$ . Figure 3.5 shows the control-to-bus voltage transfer function. These parameter values and parasitics result in a LHP complex pole pair. Notice that the phase at low frequency is -180 degree which confirms a negative dc gain characteristic. The high frequency phase is approaching -180 degree due to the two LHP zeroes and the LHP complex pole pair. The control-to-charge current transfer function during the voltage regulation mode is shown in Fig. 3.6. The low frequency phase is again -180 degree and a RHP zero causes the phase to drop to -450 degree at high frequencies. Experimental data agree well with the simulation results except for a slightly lower Q.

## Closed-loop Design Considerations in CCM

In order to design the voltage control loop, the loop gain is defined.



**Figure 3.5.** *Control-to-Bus Voltage Transfer Function*



**Figure 3.6. Control-to-Charge Current Transfer Function**

$$T_v = F_{dv} H_v F_m \quad (3.16)$$

$H_v$  and  $F_m$  represent the transfer functions of the compensator and PWM gain, respectively. Since  $F_{dv}$  has a negative dc gain, a *positive feedback compensation gain* is required to achieve overall negative feedback action. This can be realized by adding an inverter stage either in the error amplifier or in the PWM block. The following compensator consisting of an integrator, two poles, and two zeroes is required for the voltage-mode control.

$$H_v = \frac{\omega_m}{s} \frac{\left(1 + \frac{s}{\omega_{z1}}\right) \left(1 + \frac{s}{\omega_{z2}}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right) \left(1 + \frac{s}{\omega_{p2}}\right)} \quad (3.17)$$

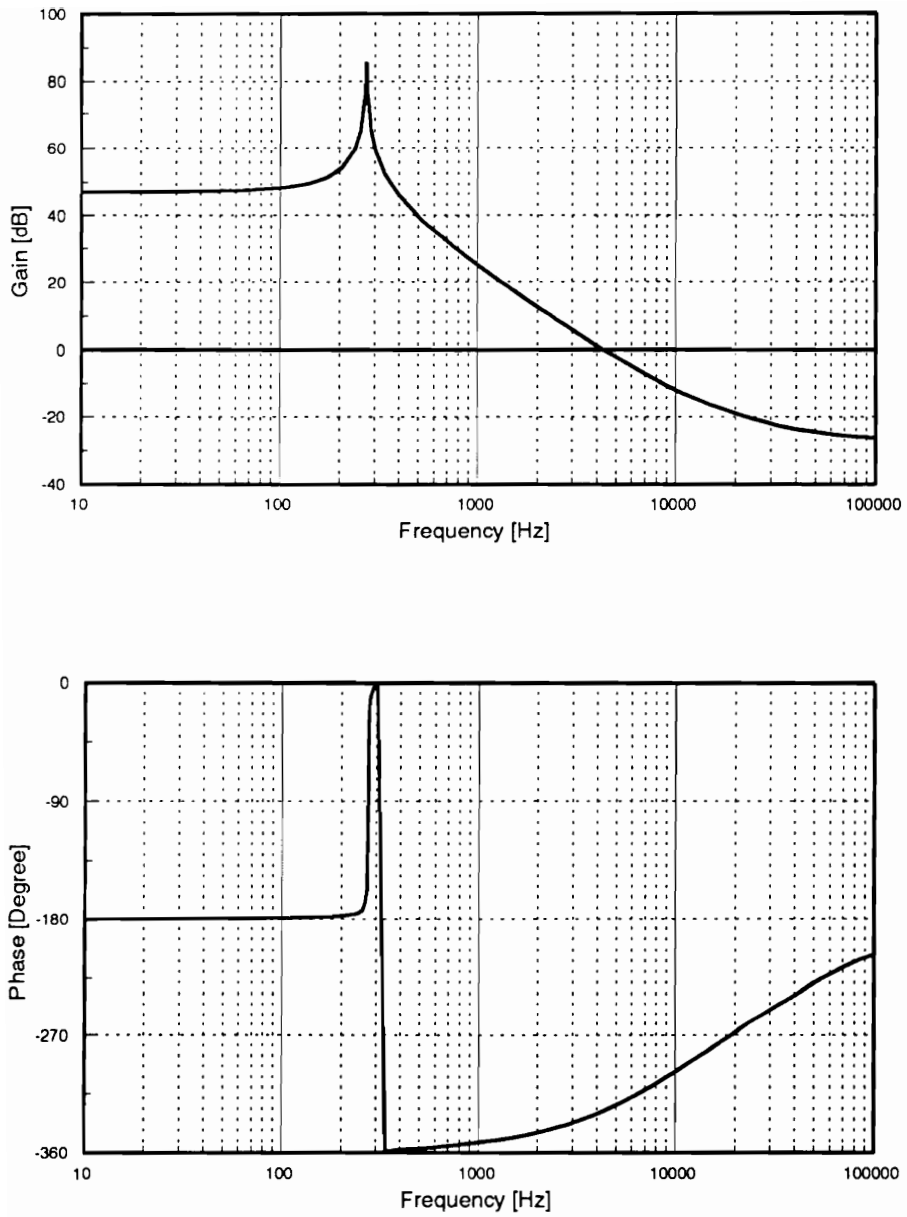
An integrator is needed for tight dc regulation. In order to compensate the excessive phase lag due to the integrator and a complex pole pair, two zeroes should be used. A low frequency zero is placed before the resonant frequency of the converter to avoid conditional stability. The second zero compensates the phase lag due to the complex pole pair. The first pole is placed to cancel the ESR zero or the LHP zero, whichever comes first. A high frequency pole is used to attenuate the switching ripple and high frequency noise in the feedback control circuit.

As described previously, the open-loop transfer functions can have a RHP complex pole pair when the parasitic terms are very small. Figure 3.7 shows the control-to-output voltage transfer function of this case. The sharp phase boost at the resonant frequency indicates the presence of a complex RHP pole pair. It

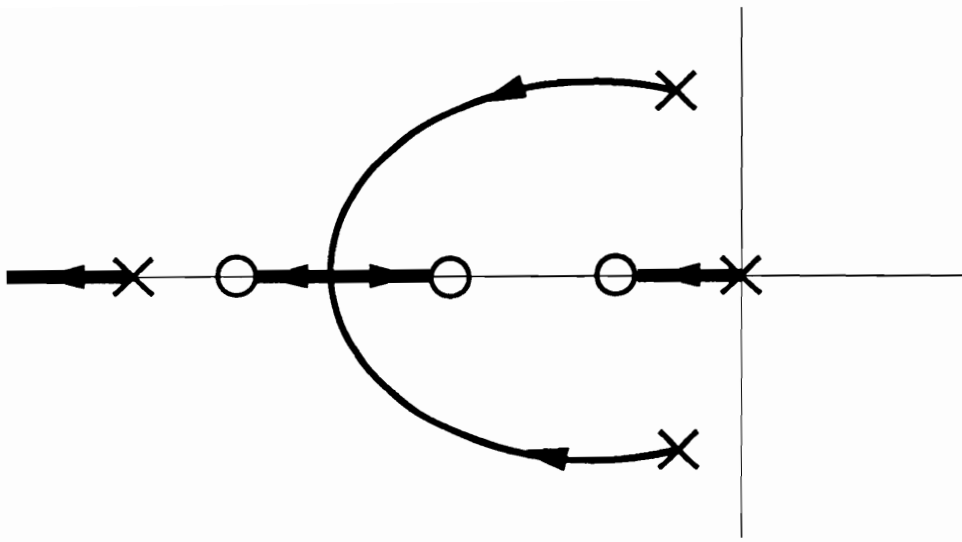
also shows the negative dc gain and very high Q characteristics. In order to investigate this open-loop unstable system, let's call this example Case 2, and the previous example which has a LHP pole pair Case 1. Figure 3.8 show root loci of the loop gains of the two cases. Two root loci show similar trajectories, and both cases have similar closed-loop eigenvalues for a given feedback gain. Case 2, however, can be unstable at very low gain.

When the loop-gain contains RHP poles, it is difficult to determine closed-loop stability from the Bode plot. In order to analyze the stability of a system using a loop gain with RHP poles, the Nyquist Criterion can be applied to its polar plot. Fig. 3.9 shows polar plots of the two cases. In Case 1, shown in Fig. 3.9(a), the loop gain does not have an open-loop RHP pole ( $N=0$ ) and it does not have counter-clockwise encirclement about the  $(-1, j0)$  point ( $N=0$ ). Since it does not have a closed-loop RHP pole ( $Z=P-N=0$ ), the system is stable. In Case 2, shown in Fig. 3.9(b), the loop gain has two open-loop RHP poles ( $P=2$ ) and two encirclements ( $N=2$ ). Thus, it does not have a closed-loop RHP pole ( $Z=P-N=0$ ) and the system is stable. The gain and phase margins used to measure relative stability are shown in Fig. 3.9(b). The system can be unstable if the gain is reduced below the gain margin, resulting in a conditionally stable system. The result for this nonminimum phase system is contrary to what is usually true for minimum phase systems in which system goes unstable for high gain, and is stable for low gain. The gain margin, defined in Fig. 3.9(b), represents how much the gain can be reduced to maintain stability.

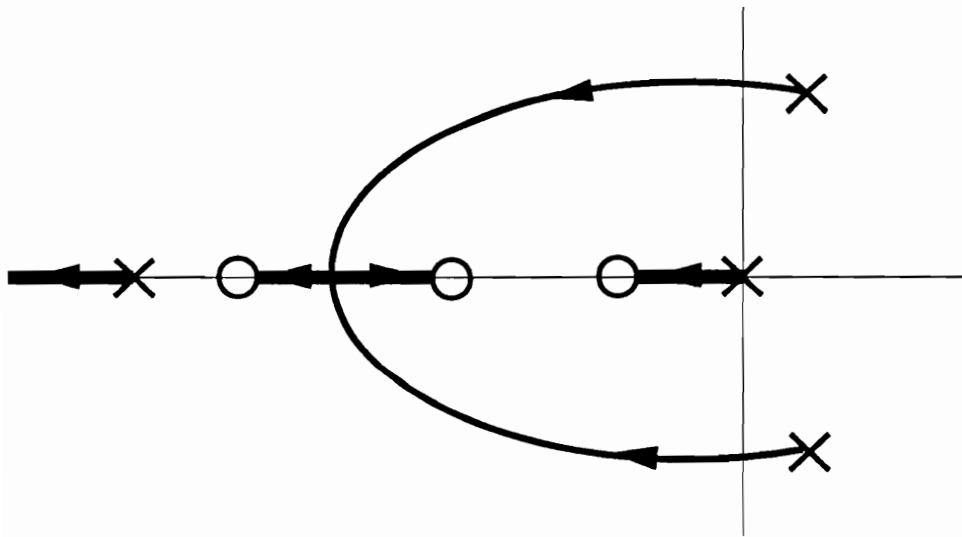




*Figure 3.7. Control-to-Output Transfer Function*



(a)

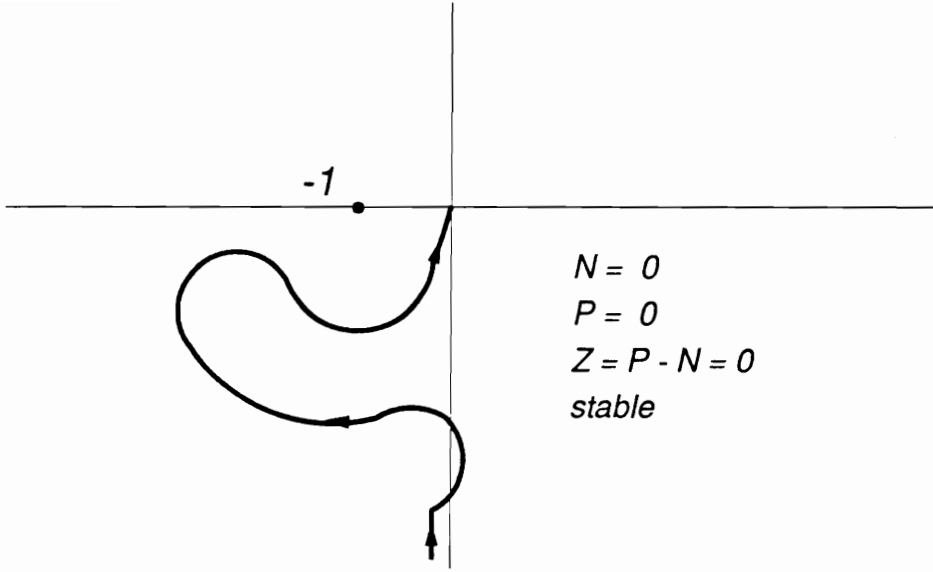


(b)

**Figure 3.8. Root Locus of Voltage-Mode Control**

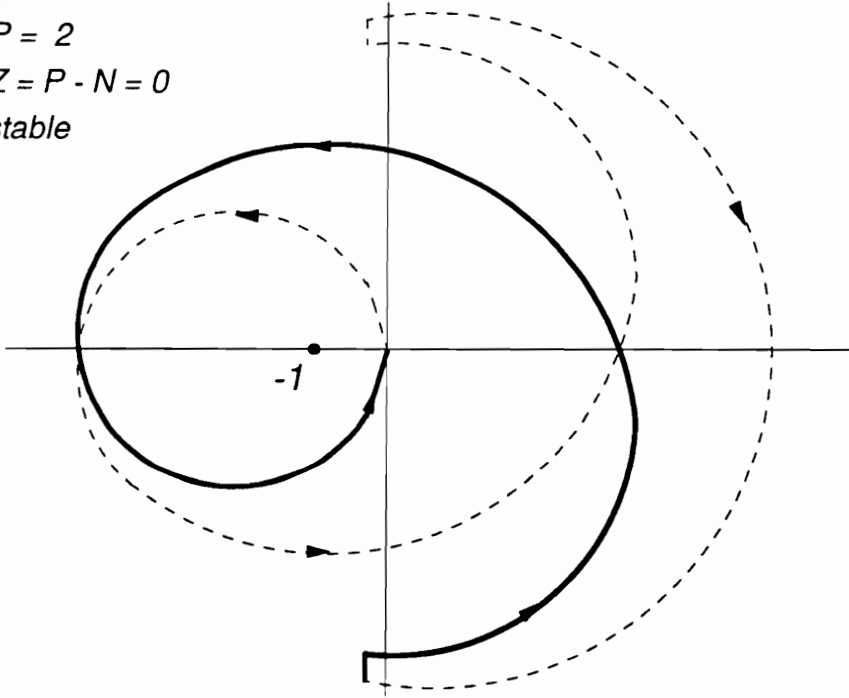
(a) Case 1

(b) Case 2



(a)

$N = 2$   
 $P = 2$   
 $Z = P - N = 0$   
*stable*



(b)

**Figure 3.9. Polar Plot of Loop-Gain in Voltage-Mode Control**

(a) Case 1

(b) Case 2

### 3.3.2 Discontinuous Conduction Mode

#### Power Stage Modeling

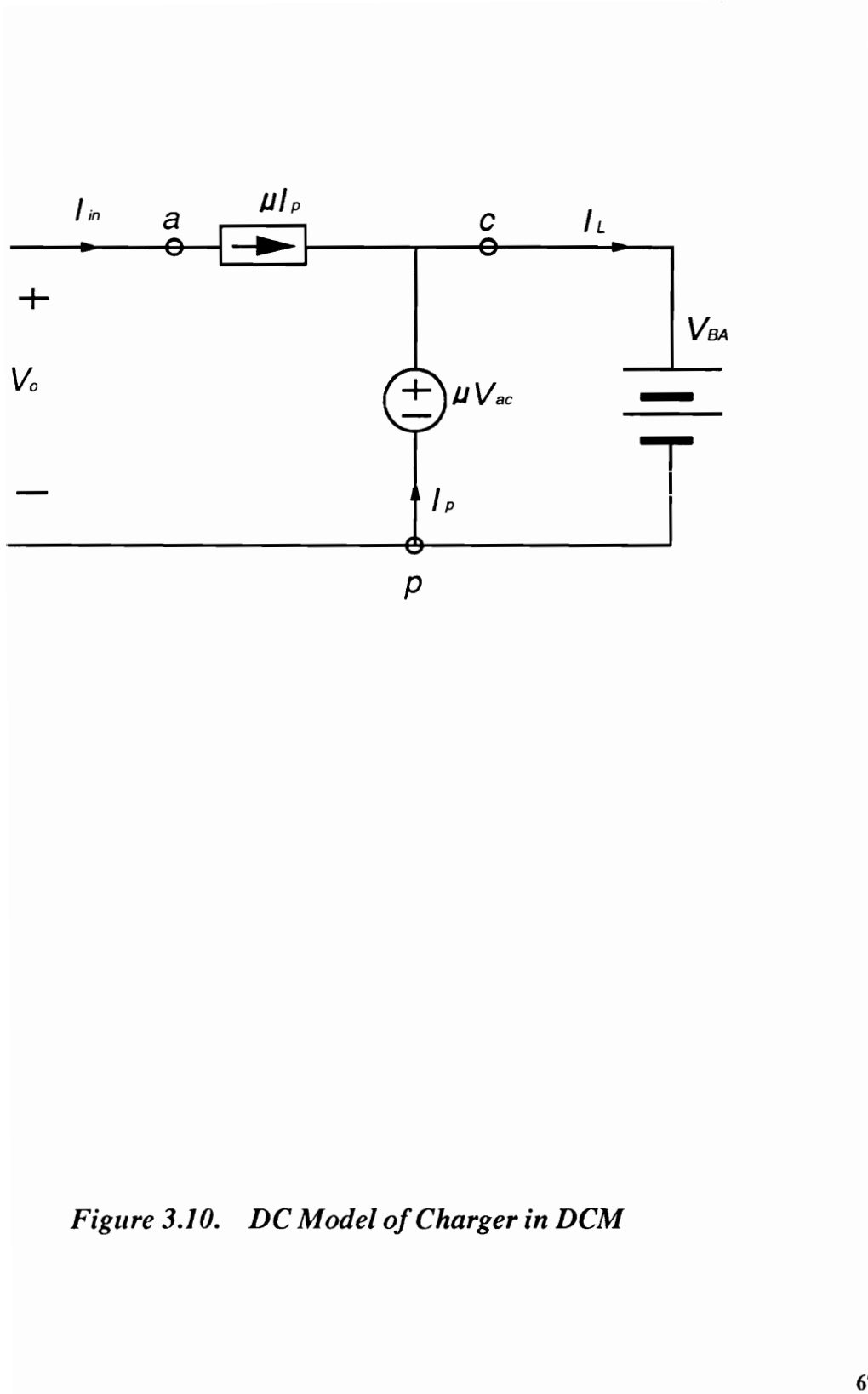
In the DET system, when the solar array's output power increases during the transition from eclipse to sunlight mode, the battery charger turns on at very light loads and operates for both discontinuous and continuous conduction modes. Since the dc and small-signal dynamic behaviors of the switching regulators for the two modes of operation are quite different, the discontinuous conduction mode (DCM) must be considered for the analysis and feedback controller design. The PWM switch model [49] is used for the DCM analysis.

Under dc conditions, the charger converter using the PWM switch model results in Fig. 3.10. From Fig. 3.10, we get

$$V_{BA} = \mu V_{ac} = \mu(V_o - V_{BA}) \quad (3.18)$$

which gives

$$M \equiv \frac{V_{BA}}{V_o} = \frac{1}{1 + \frac{1}{\mu}} \quad (3.19)$$



**Figure 3.10. DC Model of Charger in DCM**

The amplification factor  $\mu$  of the PWM switch model is:

$$\begin{aligned}\mu &= \frac{D^2}{2LF_s} \frac{V_{BA}}{I_{in}} = \frac{D^2}{2LF_s} \frac{V_O}{I_{in}} M \\ &= \frac{D^2}{2LF_s} RM = \frac{D^2 M}{K}\end{aligned}\quad (3.20)$$

where

$$R \equiv \frac{V_O}{I_{in}}, \quad K \equiv \frac{2LF_s}{R}$$

Notice that the definition of dc resistance  $R$  is different from that of a typical buck converter. Substitution of (3.20) in (3.19) gives

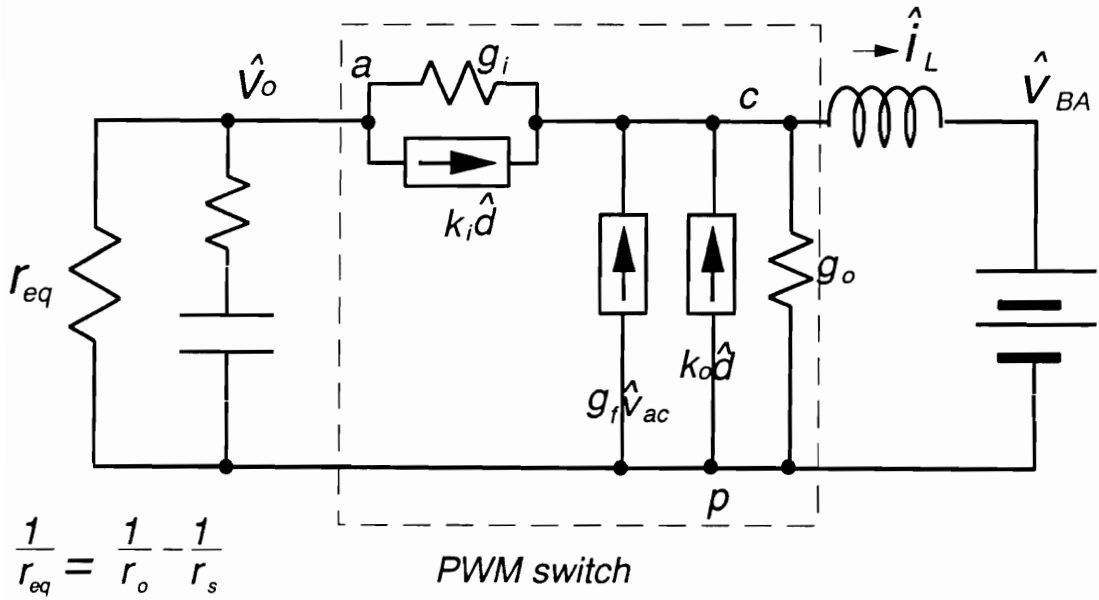
$$M = 1 - \frac{K}{D^2} \quad (3.21)$$

$$D = \sqrt{\frac{K}{1 - M}} \quad (3.22)$$

The critical value of  $K$  which determines the boundary between CCM and DCM is obtained from (3.21) by letting  $M = D$ .

$$K_{crit} = 1 - D \quad (3.23)$$

Figure 3.11 presents the charger's small-signal model employing the PWM switch model. From the Fig. 3.11 the control-to-output transfer function is derived. At nodes  $a$  and  $c$  of Fig. 3.11, KCL is applied.



**Figure 3.11. Small-Signal Model of Charger in DCM**

$$\frac{v_o}{r_{eq}} + \frac{v_o}{R_c + \frac{1}{C_s}} + (v_o - Ls i_L) g_i + k_i d = 0 \quad (3.24)$$

$$(v_o - Ls i_L) g_i + k_i d + g_f(v_o - Ls i_L) + k_o d - g_o Ls i_L - i_L = 0 \quad (3.25)$$

where

$$\begin{aligned} g_i &= \frac{I_a}{V_{ac}} = \frac{I_{in}}{V_O(1-M)} = \frac{1}{R(1-M)} \\ g_o &= \frac{I_p}{V_{cp}} = \frac{I_{in}(1/M - 1)}{MV_O} = \frac{1-M}{RM^2} \\ g_f &= 2 \frac{I_p}{V_{ac}} = \frac{2I_{in}(1/M - 1)}{V_O(1-M)} = \frac{2}{RM} \\ k_i &= \frac{2I_a}{D} = \frac{2I_{in}}{D} \\ k_o &= \frac{2I_p}{D} = \frac{2I_{in}(1-M)}{DM} \end{aligned} \quad (3.26)$$

From Eqs. (3.24) and (3.25), the control-to-output transfer function becomes:

$$\begin{aligned} \frac{\hat{v}_o}{\hat{d}} &= \frac{k_i(1 + G_s L s) - (k_i + k_o) g_i L s}{(g_i + g_f) g_i L s - (G_p + g_i)(1 + G_s L s)} \\ &\quad - k_i r_{eq} (1 + R_c s) \left\{ 1 + (G_s + g_i - \frac{k_o}{k_i} g_i) L s \right\} \\ &= \frac{\quad}{a + b s + c s^2} \end{aligned} \quad (3.27)$$



where

$$\begin{aligned}
 a &= 1 + g_i r_{eq} \\
 b &= (R_c + r_{eq})C + g_i r_{eq} R_c C + g_i r_{eq} L g_o + G_s L \\
 c &= g_i r_{eq} R_c L C g_o + (R_c + r_{eq})G_s L C
 \end{aligned} \tag{3.28}$$

$$\begin{aligned}
 G_p &\equiv \frac{1}{r_{eq}} + \frac{1}{1/Cs + R_c} \\
 G_s &\equiv g_i + g_f + g_o
 \end{aligned}$$

The denominator of Eq. (3.27) can be factored if  $|\frac{b}{a}| \gg |\frac{c}{a}|$ .

$$\begin{aligned}
 a + bs + cs^2 &= a(1 + \frac{b}{a}s + \frac{c}{a}s^2) \\
 &\simeq a(1 + \frac{b}{a}s)(1 + \frac{c}{a}s)
 \end{aligned}$$

Then, since  $|\frac{b}{a}| \gg |\frac{c}{a}|$  in Eq. (3.28), Eq. (3.27) can be simplified.

$$\frac{\hat{v}_o}{\hat{d}} \simeq G_d \frac{(1 + \frac{s}{\omega_z})(1 + sR_c C)}{(1 + \frac{s}{\omega_{p1}})(1 + \frac{s}{\omega_{p2}})} \tag{3.29}$$

where

$$\begin{aligned}
G_d &= - \frac{2V_o(1 - M)r_{eq}}{D\{R(1 - M) + r_{eq}\}} \simeq - \frac{2V_o}{DR} \{r_{eq} \parallel R(1 - M)\} \\
\omega_z &= \frac{RM^2(1 - M)}{L(1 - M + 2M^2)} \\
\omega_{p1} &= \frac{RM^2\{R(1 - M) + r_{eq}\}}{r_{eq}(1 - M)(R^2CM^2 + L) + RL} \simeq \frac{1}{C\{r_{eq} \parallel R(1 - M)\}} \\
\omega_{p2} &= \frac{r_{eq}(1 - M)(R^2CM^2 + L) + RL}{RLC r_{eq}} \simeq \frac{R(1 - M)}{L}
\end{aligned} \tag{3.30}$$

Since  $r_{eq} < 0$  and  $R \gg |r_{eq}|$ , the dc gain,  $G_d$ , becomes positive, and  $\omega_{p1}$  becomes negative, which is a RHP pole.

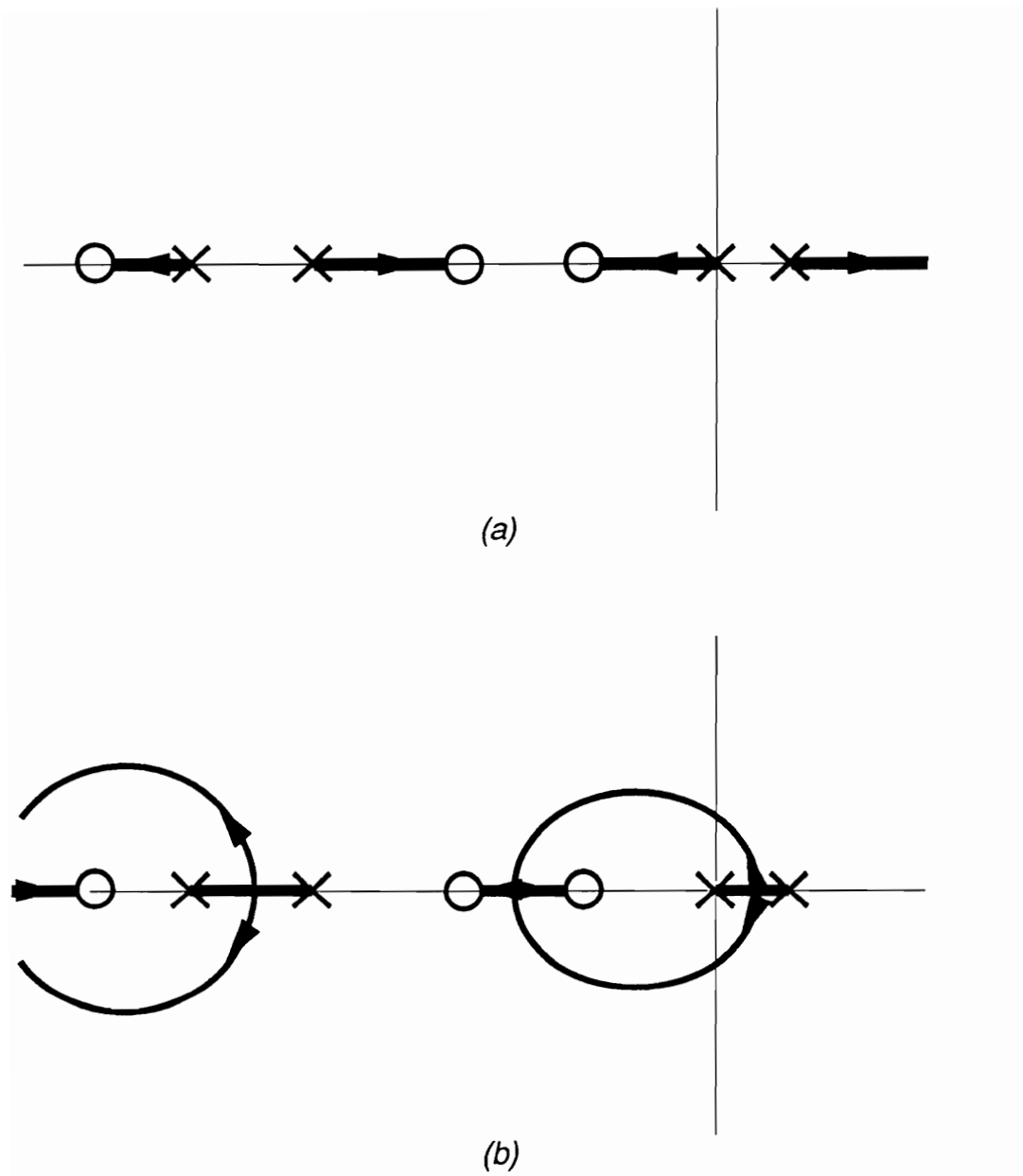
In [49], Vorperian shows that conventional switching converters in discontinuous mode have two separate real poles. The low frequency pole is same as the single pole given by state-space averaging [50]. The second pole  $f_{p2}$  occurs in the range  $f_{p2} \geq F_s / \pi$ . It was also shown that the RHP zero is present in the control-to-output transfer function of boost and buck-boost converter.

In Eq. (3.30), as the charge current increases, the dc gain  $G_d$  increases, and the RHP  $\omega_{p1}$  moves towards the origin. It is interesting to note that dc gain in DCM is positive, while it is negative in CCM. Thus extra care is needed in designing a compensator.

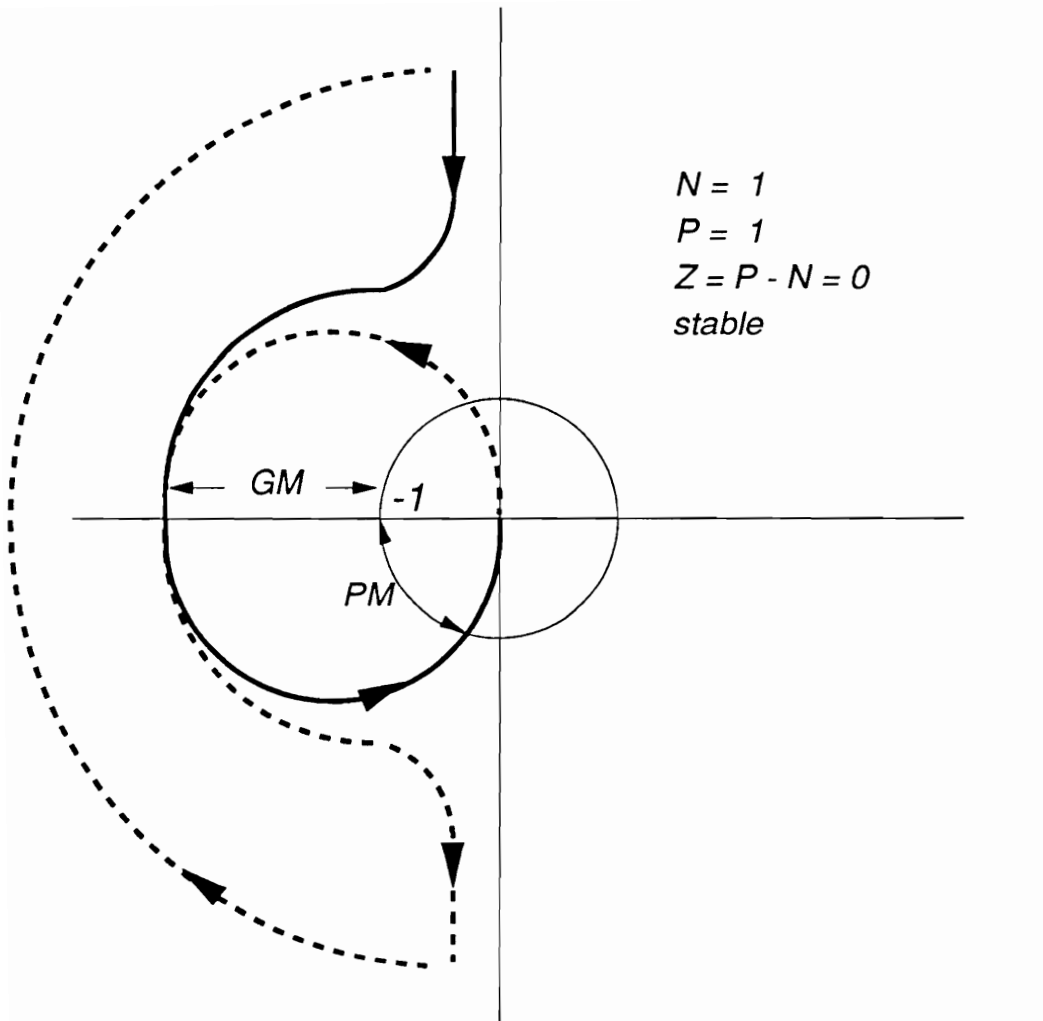
### Closed-loop Design Consideration in DCM

Figure 3.12 shows the root locus of the loop gain using the same type of compensator as for the CCM case. As discussed earlier, feedback control design for a nonminimum phase system, as in Eq. (3.29), is quite different from that of a minimum phase system. Figure 3.12(a) shows the root locus of a system with the compensator of negative gain, while Fig. 3.12(b) shows the case when positive gain is used. Figure 3.12(a) indicates that system is always unstable. Figure 3.12(b) shows a conditionally stable system which can be unstable for a low gain. Thus, it is necessary to use positive feedback gain although the control-to-bus voltage transfer function has a positive dc gain. Therefore the same feedback compensator can be used for both CCM and DCM operations.

Closed-loop stability is also analyzed using the Nyquist Criterion. Figure 3.13 illustrates the polar plot of the loop gain. Since the loop gain has one open-loop RHP pole, the polar plot of the loop gain must make one counter-clockwise encirclement if the system is to be stable. Figure 3.13 reveals that the loop gain encircles the  $(-1, j0)$  point once, so the system will be stable for a properly designed compensator with a positive dc gain.



**Figure 3.12. Root Locus of Loop-Gain in DCM**  
 (a) positive gain  
 (b) negative gain



**Figure 3.13.** Polar Plot of Loop-Gain in DCM

### 3.3.3 Closed-loop Control Design for the Charger in both CCM and DCM

As discussed in Section 3.3.1 and 3.3.2, dynamics of the charge converter in CCM and DCM are quite different. However, it is necessary to design a feedback compensator to optimize system performance in both CCM and DCM. Dynamics of the charger also change according to level of the charge current which varies widely. Thus, it is important to design a compensator for the worst case condition for the system stability. In order to identify the worst case, the operating range of the charge current should be determined first. In Chapter 2, it was shown that during the transition from eclipse to sunlight, the charger turns on at finite load. The minimum charge current can be determined approximately by

$$I_{in}|_{\min} \simeq \frac{V_{ch} - V_{dis}}{r_{eq}} \quad (3.31)$$

where  $V_{ch}$  and  $V_{dis}$  represent regulation voltages of the charger and discharger respectively. The upper limit of the charge current operating in DCM is determined from the boundary condition between CCM and DCM. The upper limit in CCM is given by the charge current limit.

Since the charger in CCM has a complex pole pair, it is necessary to stabilize it for CCM first. In CCM, from Eq. (3.13), the control-to-bus voltage transfer function  $F_{dv}$  is insensitive to the change of the battery voltage, which can be considered a fixed value during the bus voltage regulation mode. However, the zero in  $F_{dv}$  moves as a function of the dc charge current. As the charge current

increases, the LHP zero moves towards lower frequency which boosts the loop-gain phase at the crossover frequency. Therefore, when we design the loop gain in CCM, the stability should be ensured at the minimum charge current. On the other hand, as the zero moves towards lower frequency, the loop-gain crossover frequency increases. Thus the integrator gain should be adjusted not to exceed the crossover frequency limit at the maximum charge current.

In DCM, from Eq. (3.30), the dc gain of  $F_{dv}$  varies widely with respect to the charge current level. The lowest dc gain occurs at the minimum charge current and the loop-gain crossover occurs at a much lower frequency than in CCM. Thus the worst case bus performance occurs at the minimum load condition.

To illustrate the loop-gain design, the space platform system under study is used as an example. Its dc operating conditions are given by

Bus voltage  $V_o = 120$  V

Battery voltage  $V_{BA} = 65\text{--}85$  V

Solar array maximum power = 6,000 W

Load power = 1,800 W

Charge current limit = 23 A

The circuit parameters are

$L = 50 \mu\text{H}$ ,  $R_l = 50 \text{ m}\Omega$

$C = 2000 \mu\text{F}$ ,  $R_c = 50 \text{ m}\Omega$

Switching frequency = 90 kHz

The maximum loop-gain crossover frequency is set at 10 kHz and the worst case phase margin is set to 30 degree.

From Eq. (3.23), the boundary between the CCM and DCM is obtained such that  $I_{crit} = 3.3 A$ .

The operating conditions and the corresponding characteristics of the control-to-output transfer function  $F_{dv}$  for the four extreme conditions are summarized in Table 3.1. In order to design a feedback compensator for the extreme conditions in Table 3.1 to satisfy the loop-gain requirement, the design procedure is as follows. First, for the 10 kHz loop-gain crossover frequency, the gain of the compensator is limited from the case of  $I_{Lmax}$  in CCM. As shown in Fig. 3.12 and Table 3.1, the gain of the compensator should be maximized to compensate the low gain of  $F_{dv}$  in DCM in order to optimize the system performance. Due to the RHP pole in  $F_{dv}$  in DCM, the pole-zero placement should be designed for the case of  $I_{Lmin}$  in DCM. Thus, the design of an optimum compensator requires several iterations to satisfy the design goal.

The designed compensator parameters are:

$$H_v = \frac{900}{s} \frac{(1 + \frac{s}{1,260})(1 + \frac{s}{1,880})}{(1 + \frac{s}{10,000})(1 + \frac{s}{31,400})}$$



**Table 3.1 Control-to-Output Transfer Function Data  
in Voltage-Mode Control**

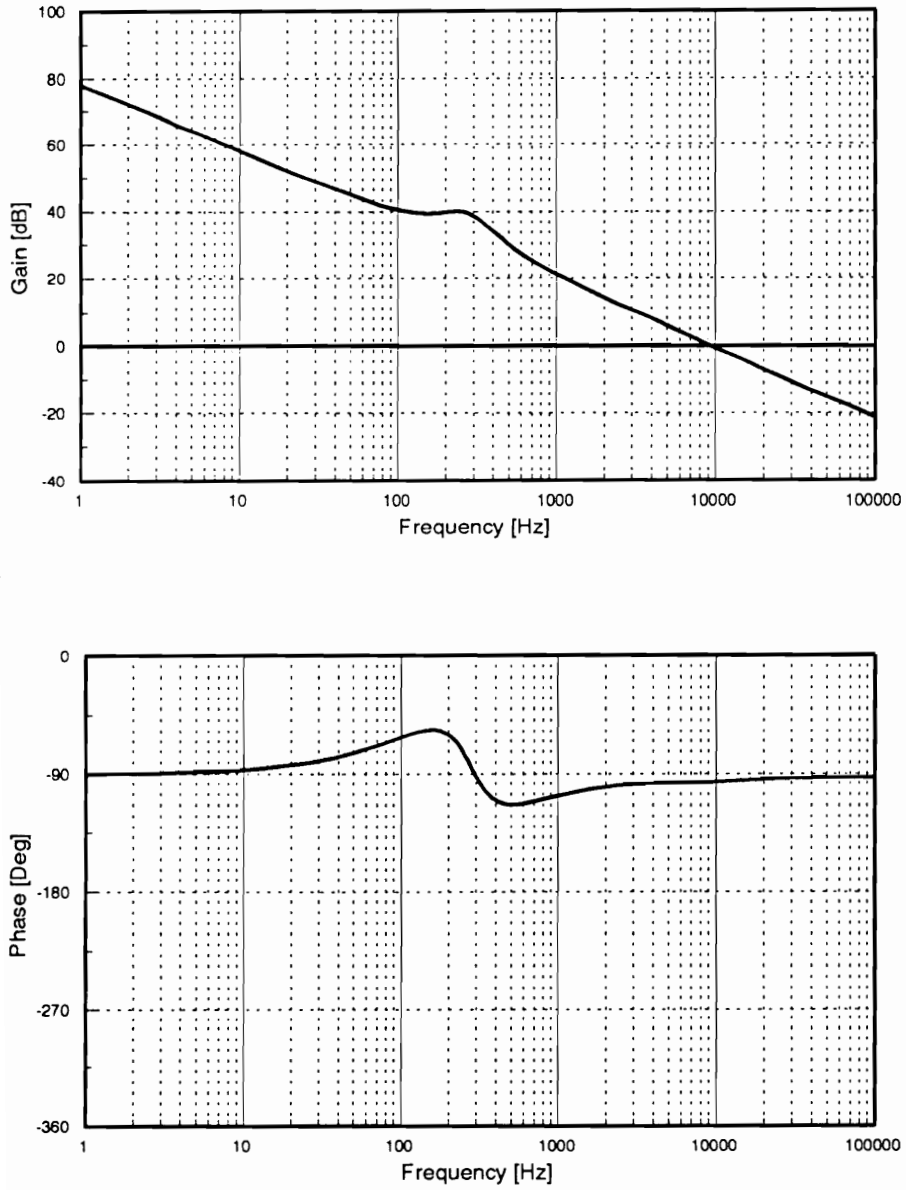
	DCM		CCM	
	$I_{Lmin} = 0.2 A$	$I_{Lmax} = 3.3 A$	$I_{Lmin} = 3.3 A$	$I_{Lmax} = 23 A$
$R_{dc}$	1,056 ohm	67 ohm	67 ohm	9.7 ohm
$r_{eq}$	- 8.8 ohm	- 8.8 ohm	- 8.8 ohm	- 8.8 ohm
$D$	0.13	0.54	0.54	0.54
$G_d$	16.8	83.2	- 226	-226
$W_{z1}$	10 e3	10 e3	10 e3	10 e3
$W_{z2}$	1.55 e6	397 e3	396 e3	58 e3
$W_b$			1705	1732
$Q$			1.4	1.4
$W_{p1}$	- 51.7	- 39.1		
$W_{p2}$	710 e3	183 e3		
$F_{dv} = G_d \frac{(1 + s/W_{z1})(1 + s/W_{z2})}{(1 + s/W_{p1})(1 + s/W_{p2})}$			$F_{dv} = G_d \frac{(1 + s/W_{z1})(1 + s/W_{z2})}{1 + s/QW_b + s^2/W_b^2}$	

Figures 3.14 through 3.21 show the loop gain and bus impedance characteristics for each case in Table 3.1.

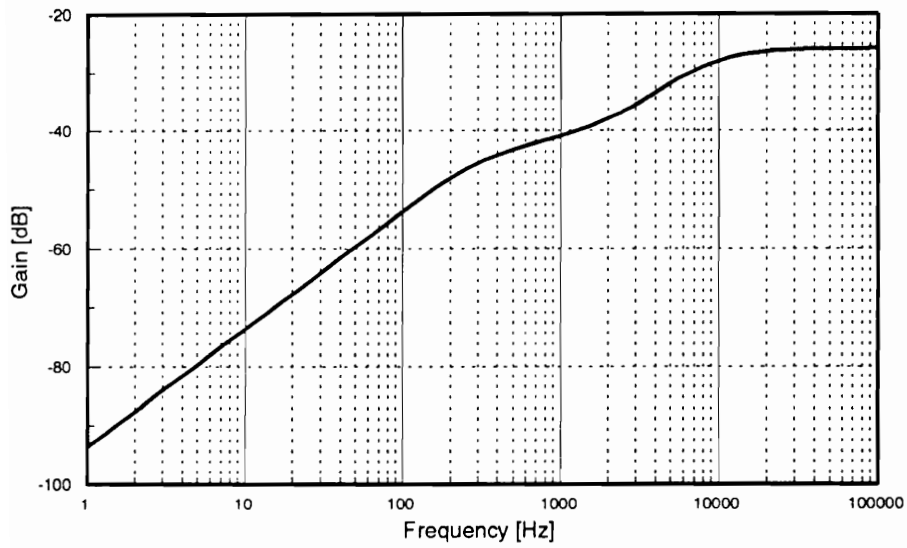
In DCM, as shown in Figs. 3.18 through 3.21, loop-gain bandwidths are much lower than the CCM cases and bus impedances become higher. The reduction of the dc gain of the control-to-output transfer function from CCM to DCM and the low frequency RHP pole give those poor performance in DCM. In order to satisfy the worst case 30 degree phase margin at the worst case (minimum current in DCM), the compensator zero was moved to a lower frequency and the integrator gain was reduced. This resulted in even higher bus impedance in DCM as well as poorer performance in CCM.

### ***3.4 Modeling, Analysis and Design of the Charger with Current-Mode Control***

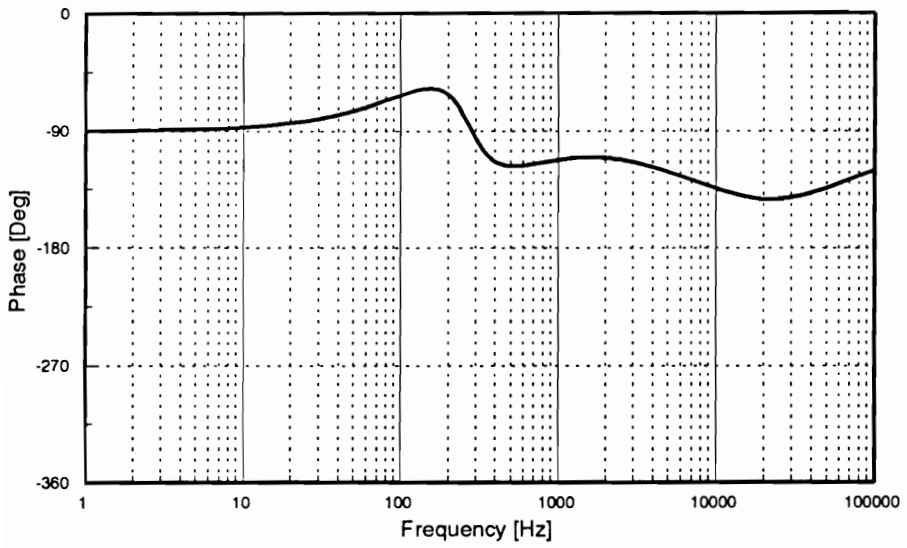
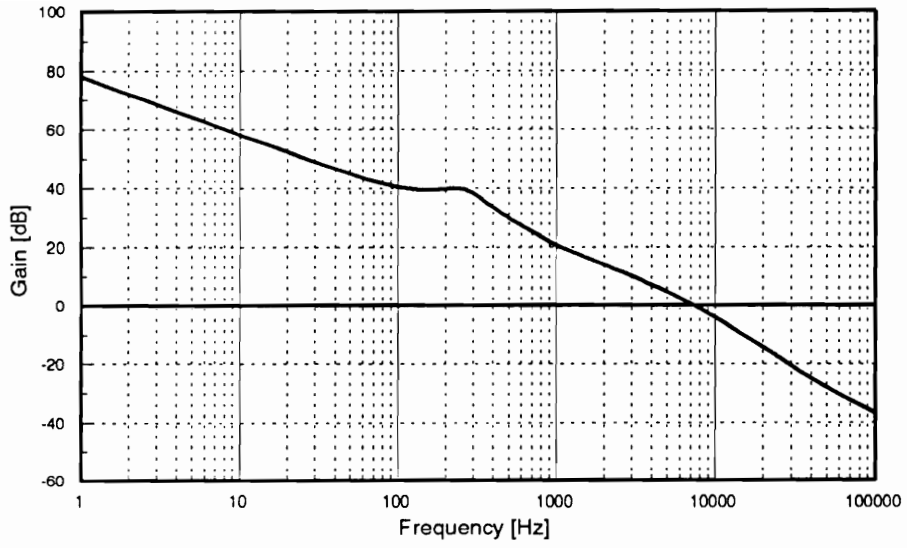
Due to its many advantages over voltage-mode control, current-mode control is widely used for switching regulators. Especially for a switching regulator with several parallel modules for a high power system, current-mode control should be used for current sharing among parallel modules. However, current-mode



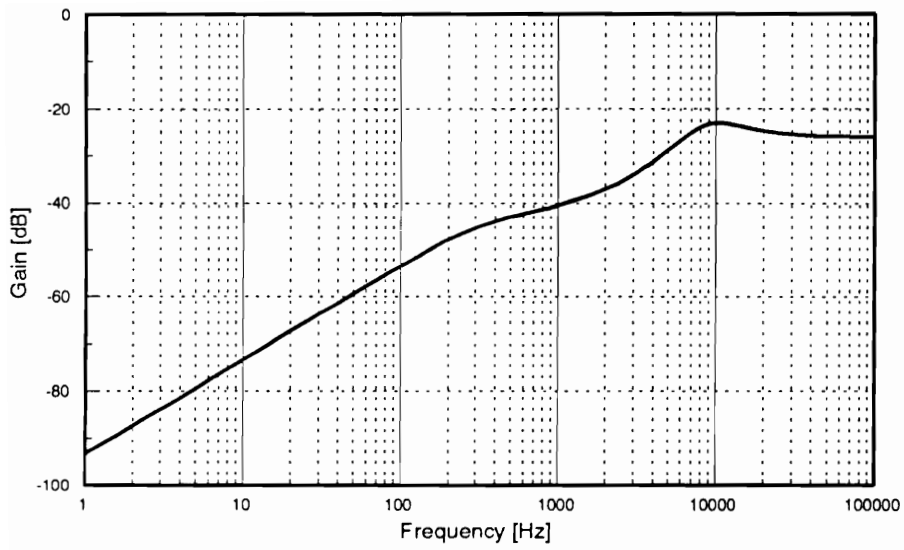
*Figure 3.14. Loop Gain in CCM, Maximum Current*



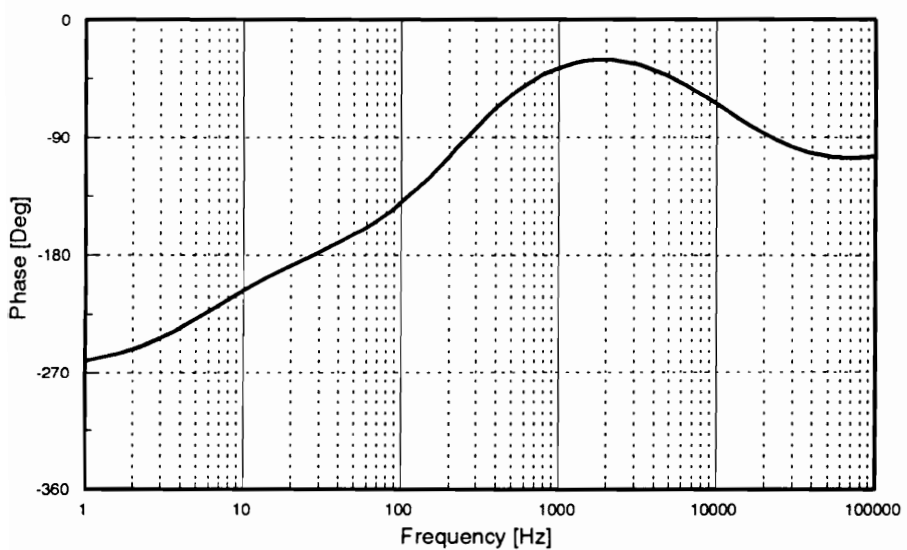
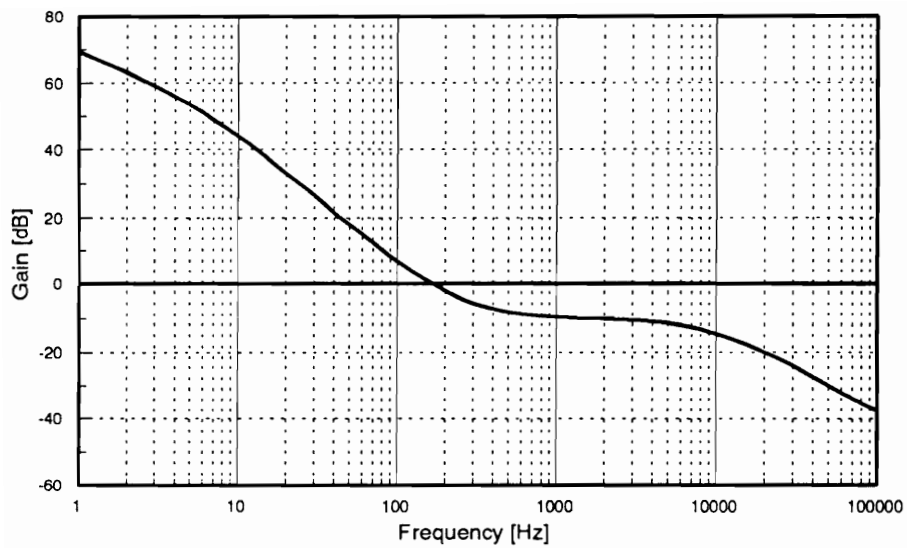
**Figure 3.15.** *Bus Impedance in CCM, Maximum Current*



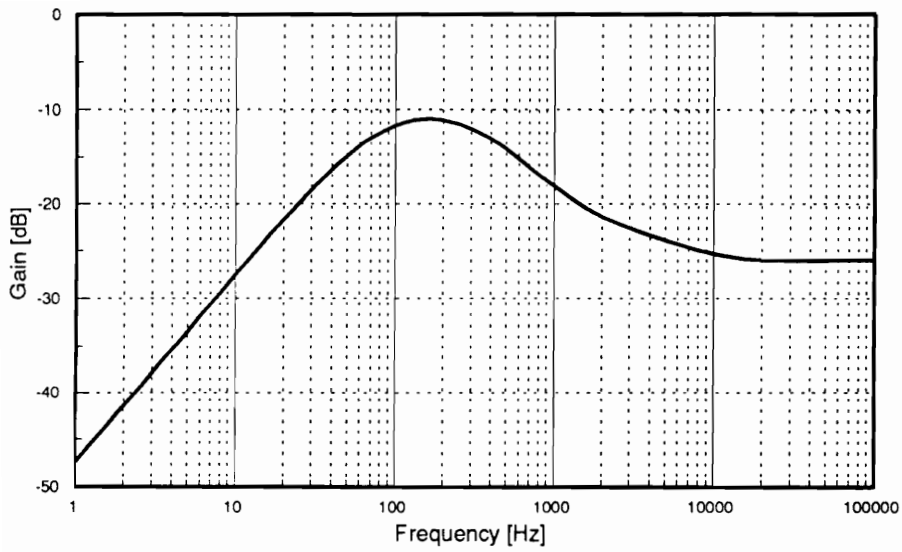
*Figure 3.16. Loop Gain in CCM, Minimum Current*



**Figure 3.17. Bus Impedance in CCM, Minimum Current**

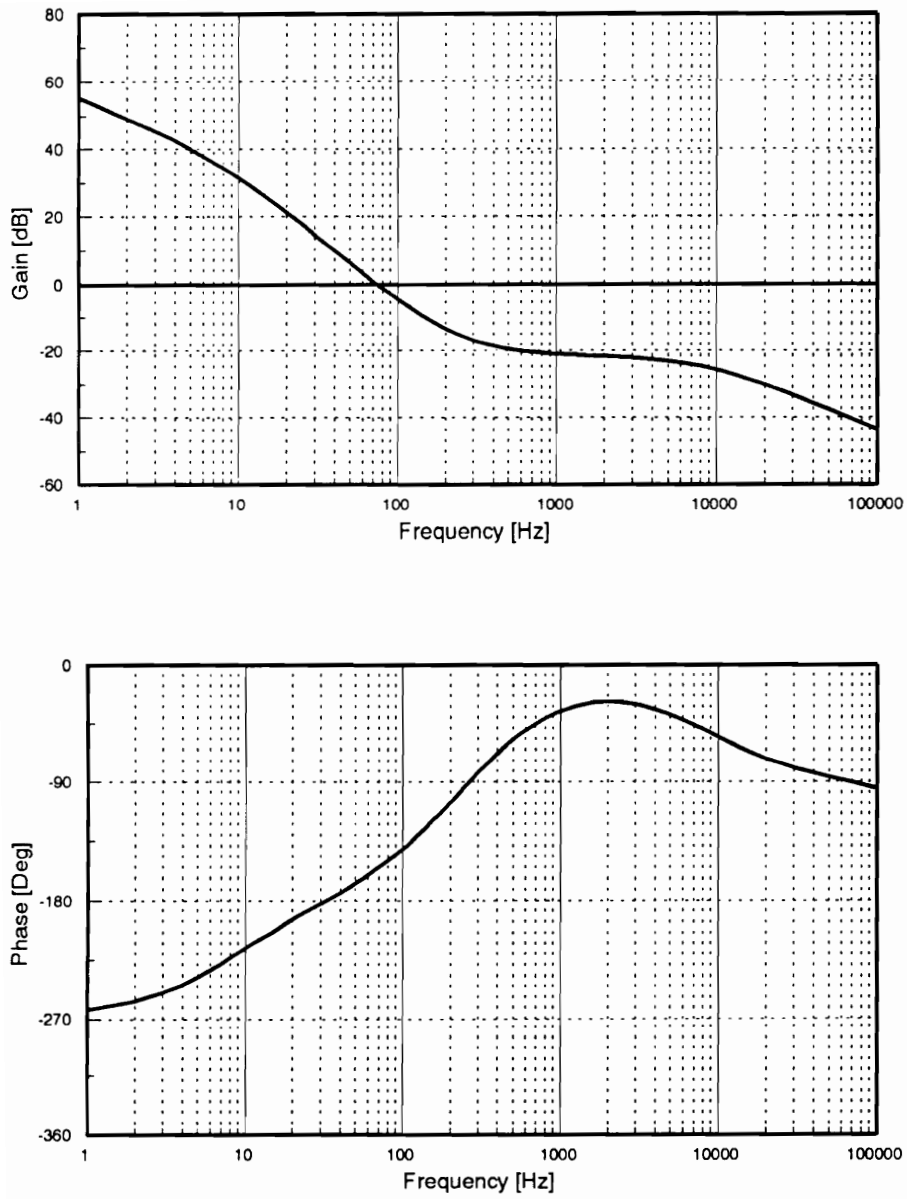


*Figure 3.18. Loop Gain in DCM, Maximum Current*

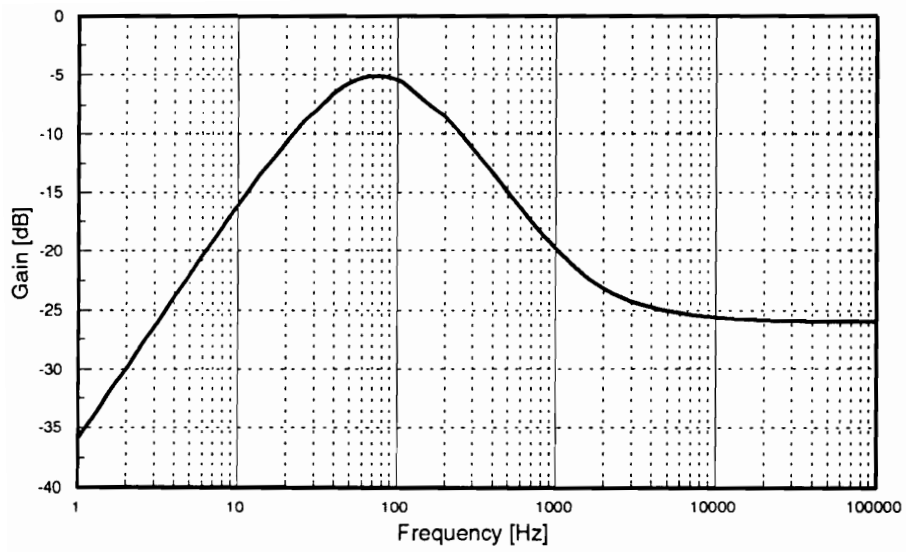


**Figure 3.19. Bus Impedance in DCM, Maximum Current**





*Figure 3.20. Loop Gain in DCM, Minimum Current*



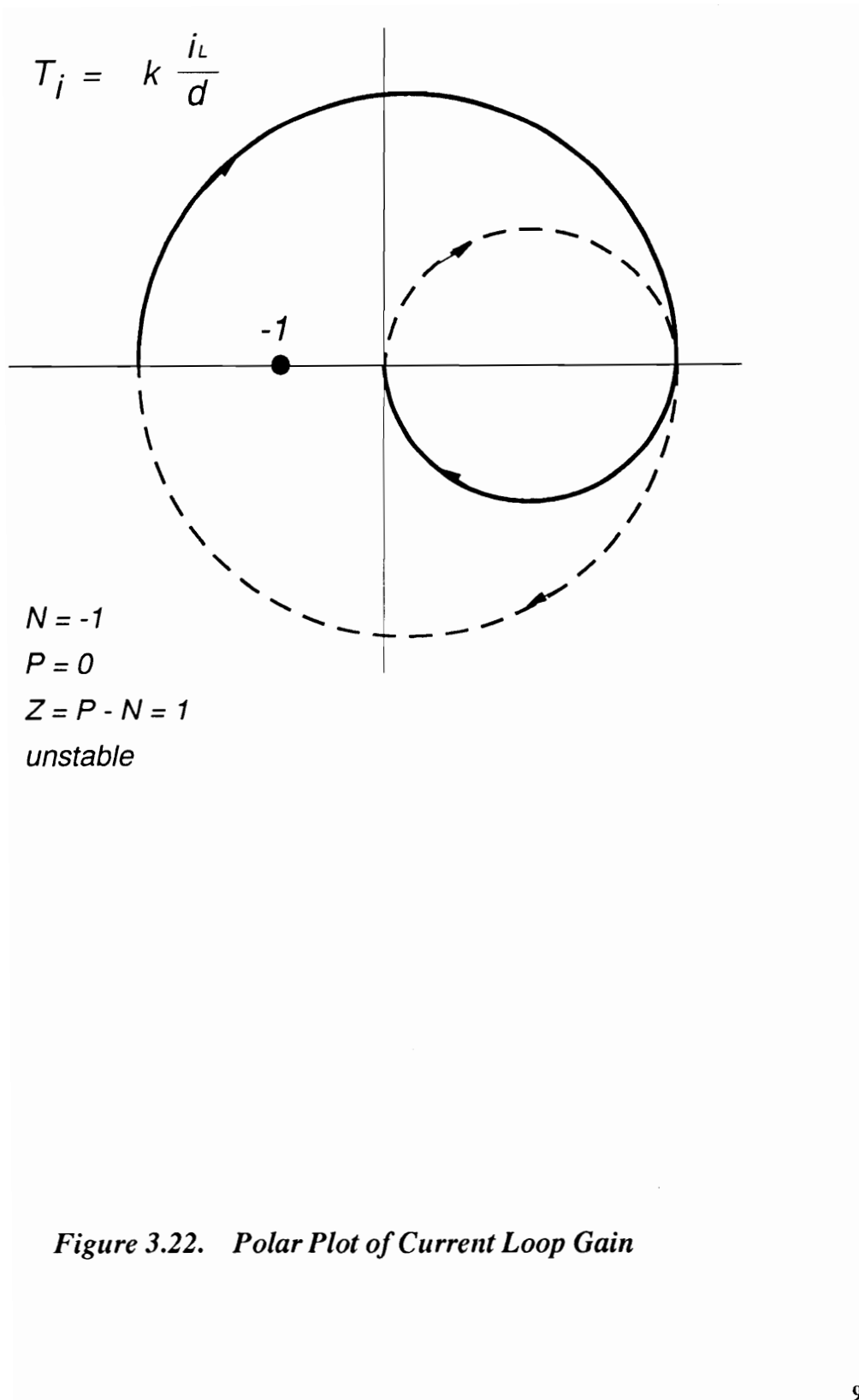
**Figure 3.21. Bus Impedance in DCM, Minimum Current**

control for a battery charger regulator also shows different dynamic characteristics from conventional switching regulators as in the case of the voltage-mode control. As shown in Eq. (3.13), the duty-cycle to inductor current transfer function has a negative dc gain and a right-half-plane (RHP) zero. This results in an unstable current loop-gain. Figure 3.22 shows the Nyquist plot of the current loop gain ignoring the high frequency complex pole pair due to the sampling effect of closing the current loop. As long as the dc gain is larger than unity, the number of encirclements becomes -1. Since the open loop transfer function does not have a RHP pole for the given circuit parameters, there exists one closed loop RHP pole. Thus the current loop becomes unstable. However, this may not necessarily imply that the current-mode control cannot be used for the battery charger. As in the case of the voltage-mode control, it is necessary to consider both CCM and DCM operation.

### **3.4.1 Continuous Conduction Mode**

#### Modeling of the Current-Mode Controlled Charger Operating in CCM

The recent modeling approach for switching regulators employing current-mode control [51] is implemented for the charger circuit as shown in Fig. 3.23. This uses the PWM switch model for the power stage, and sampling action and feedforward terms of the current loop are included in the model. From the power



stage of Fig. 3.23, transfer functions of the duty cycle-to-bus voltage and duty cycle-to-charge current are derived, and previous derivations of Eqs. (3.13) (3.14) are confirmed. The results are:

$$F_v = \frac{\hat{v}_o}{\hat{d}} = -\frac{V_o}{D} \frac{(1 + \frac{s}{\omega_v})(1 + sR_cC)}{\Delta(s)} \quad (3.32)$$

where

$$\begin{aligned} \omega_v &= \frac{V_{BA}}{I_L L} \\ \Delta(s) &= 1 + \frac{s}{Q_o \omega_o} + \frac{s^2}{\omega_o^2} \\ \omega_o &= \frac{D}{\sqrt{LC}}, \quad Q_o = \frac{1}{\omega_o (\frac{L}{D^2 r_{eq}} + CR_c)} \end{aligned} \quad (3.33)$$

The control-to-charge current transfer function is:

$$F_i = \frac{\hat{i}_L}{\hat{d}} = \frac{I_k}{D^2} \frac{(1 + s \frac{V_o C}{I_k})}{\Delta(s)} \quad (3.34)$$

where

$$\begin{aligned} I_k &= V_o \left( \frac{1}{r_o} - \frac{1}{r_s} \right) - (I_s - I_o) \\ &= \frac{V_o}{r_{eq}} - D I_L \end{aligned} \quad (3.35)$$

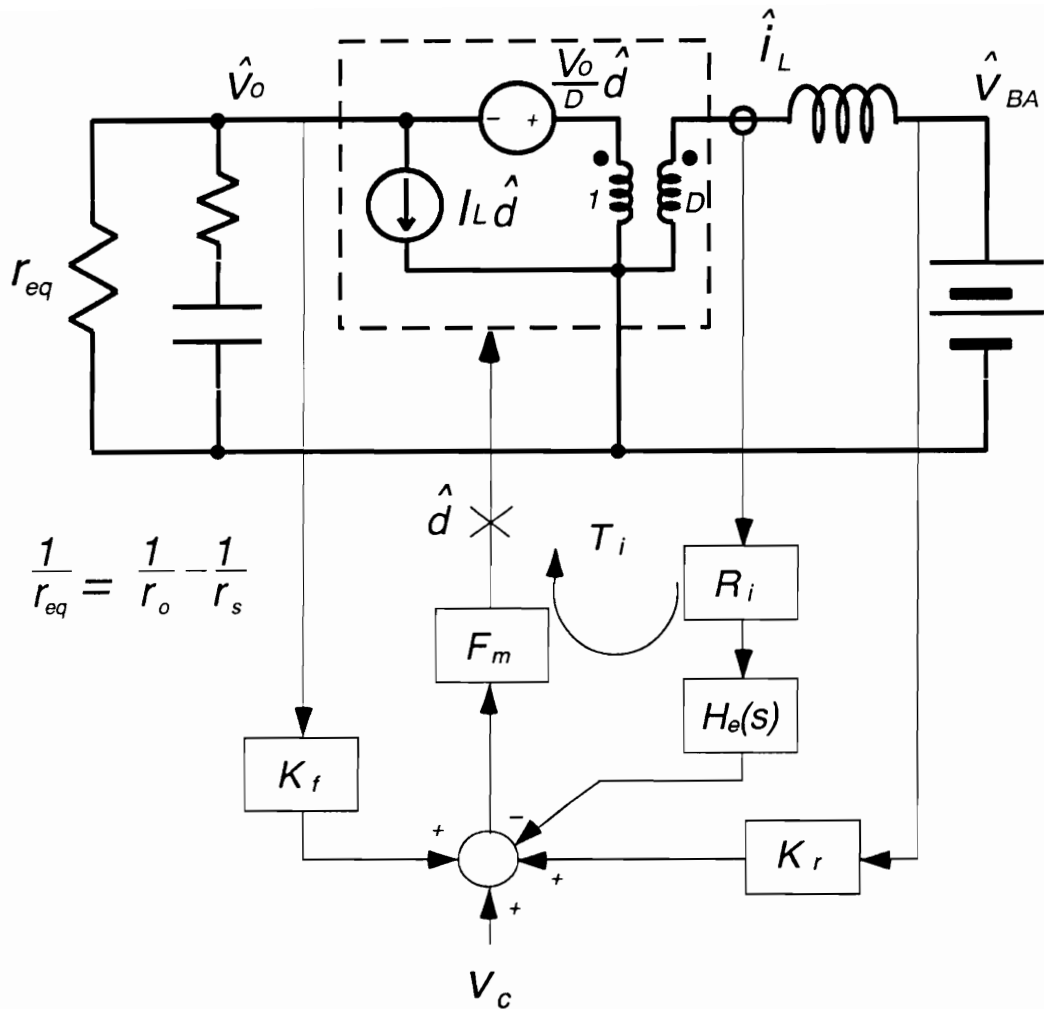


Figure 3.23. Small-Signal Model of Charger using Current Mode Control

From Fig. 3.23 the current loop gain,  $T_i$ , becomes:

$$\begin{aligned} T_i &= F_m F_i R_i H_e(s) \\ &= G_i \frac{(1 + \frac{s}{\omega_i}) H_e(s)}{\Delta(s)} \end{aligned} \quad (3.36)$$

where

$$\begin{aligned} G_i &\equiv \frac{I_k}{D^2} F_m R_i \\ \omega_i &\equiv \frac{I_k}{V_o C} \\ H_e(s) &= 1 + \frac{s}{Q_n \omega_n} + \frac{s^2}{\omega_n^2} \\ \omega_n &= \frac{\pi}{T_s}, \quad Q_n = -\frac{2}{\pi} \end{aligned} \quad (3.37)$$

Then the control-to-bus voltage transfer function with the current loop closed in Fig. 3.23 becomes:

$$\begin{aligned} \frac{\hat{v}_o}{\hat{v}_c} &= \frac{F_m F_v}{1 + T_i - F_v K_f F_m} \\ &= \frac{-F_m \frac{V_o}{D}}{1 + G_i + K_f F_m \frac{V_o}{D}} \frac{(1 + \frac{s}{\omega_v})(1 + sR_c C)}{(1 + as + bs^2 + cs^3)} \end{aligned} \quad (3.38)$$

where

$$\begin{aligned}
 a &= \frac{\frac{1}{Q_o\omega_o} + \frac{G_i}{Q_n\omega_n} + \frac{G_i}{\omega_i} + K_f F_m \frac{V_o}{D} \left(\frac{1}{\omega_v} + R_c C\right)}{1 + G_i + K_f F_m \frac{V_o}{D}} \\
 b &= \frac{\frac{1}{\omega_o^2} + G_i \left(\frac{1}{\omega_n^2} + \frac{1}{Q_n\omega_n\omega_i}\right) + K_f F_m \frac{V_o}{D} \frac{R_c C}{\omega_v}}{1 + G_i + K_f F_m \frac{V_o}{D}} \\
 c &= \frac{\frac{G_i}{\omega_n^2\omega_i}}{1 + G_i + K_f F_m \frac{V_{BA}}{D^2}}
 \end{aligned} \tag{3.39}$$

In Eq. (3.38), since  $|a| \gg |b|$  and  $|a| \gg |c|$  for practical conditions, the third order polynomial of the denominator can be factored.

$$1 + as + bs^2 + cs^3 \simeq (1 + as) \left(1 + \frac{b}{a}s + \frac{c}{a}s^2\right)$$

Then, Eq. (3.38) can be simplified.



$$\frac{\hat{v}_o}{\hat{v}_c} \equiv F_v \simeq G_x \frac{(1 + \frac{s}{\omega_v})(1 + sR_cC)}{(1 + \frac{s}{\omega_x})(1 + \frac{s}{\omega_n Q_p} + \frac{s^2}{\omega_n^2})} \quad (3.40)$$

where

$$G_x = \frac{-F_m \frac{V_o}{D}}{1 + G_i + K_f F_m \frac{V_o}{D}}$$

$$\omega_x = \frac{1 + G_i + K_f F_m \frac{V_o}{D}}{\frac{1}{Q_o \omega_o} + \frac{G_i}{Q_n \omega_n} + \frac{G_i}{\omega_i} + K_f F_m \frac{V_o}{D} (\frac{1}{\omega_v} + R_c C)}$$

$$K_f = -\frac{D T_s R_i}{L} (1 - \frac{D}{2}) \quad (3.41)$$

$$Q_p = \frac{1}{\pi (m_c D' - 0.5)}$$

$$\omega_n = \frac{\pi}{T_s}$$

The dc gain  $G_x$  becomes positive, because  $G_i$  and  $K_f$  are both negative and the magnitude of  $G_i$  is greater than one.

The denominator of  $\omega_x$  can be simplified since its second term and fourth term are much smaller than the other terms in the practical case.

$$\omega_x \simeq \frac{1 + G_i + K_f F_m \frac{V_o}{D}}{\frac{1}{Q_o \omega_o} + \frac{G_i}{\omega_i}} \quad (3.42)$$

If  $|G_i| \gg 1$ , Eq. (3.42) can be further simplified.

$$\omega_x \simeq \frac{G_i}{\frac{G_i}{\omega_i}} = \omega_i \quad (3.43)$$

This reveals that the dominant pole  $\omega_x$  can be approximated to the RHP zero of duty cycle-to-charge current transfer function in Eq. (3.34), and thus  $\omega_x$  becomes a RHP pole. As the charge current increases, the magnitude of  $G_i$  increases. It results in lower dc gain and a higher RHP pole in the control-to-output transfer function  $F_v$ .

The second order term in the denominator of Eq. (3.40) has a resonant frequency at a half of the switching frequency, and its damping is a function of the magnitude of the external ramp. Once the damping factor  $Q_p$  is adjusted by the external ramp to avoid peaking at the half of the switching frequency, the complex pole pair has little effect on system dynamics.

### 3.4.2 Discontinuous Conduction Mode

#### Modeling of the Current-Mode Controlled Charger Operating in DCM

When current-mode control is used for discontinuous conduction mode, the current feedback term is not needed in the small-signal model [51], as shown in Fig. 3.24. From Fig. 3.24 the control-to-output transfer function becomes:

$$\frac{\hat{v}_o}{\hat{v}_c} = \frac{F_m \frac{\hat{v}_o}{\hat{d}}}{1 - K_f F_m \frac{\hat{v}_o}{\hat{d}}} \quad (3.44)$$

The duty cycle-to-bus voltage transfer function in DCM was given by Eqs. (3.27) and (3.28) in the voltage-mode control section:

$$\frac{\hat{v}_o}{\hat{d}} \simeq G_d \frac{(1 + \frac{s}{\omega_z})(1 + sR_c C)}{(1 + \frac{s}{\omega_{p1}})(1 + \frac{s}{\omega_{p2}})} \quad (3.45)$$

where

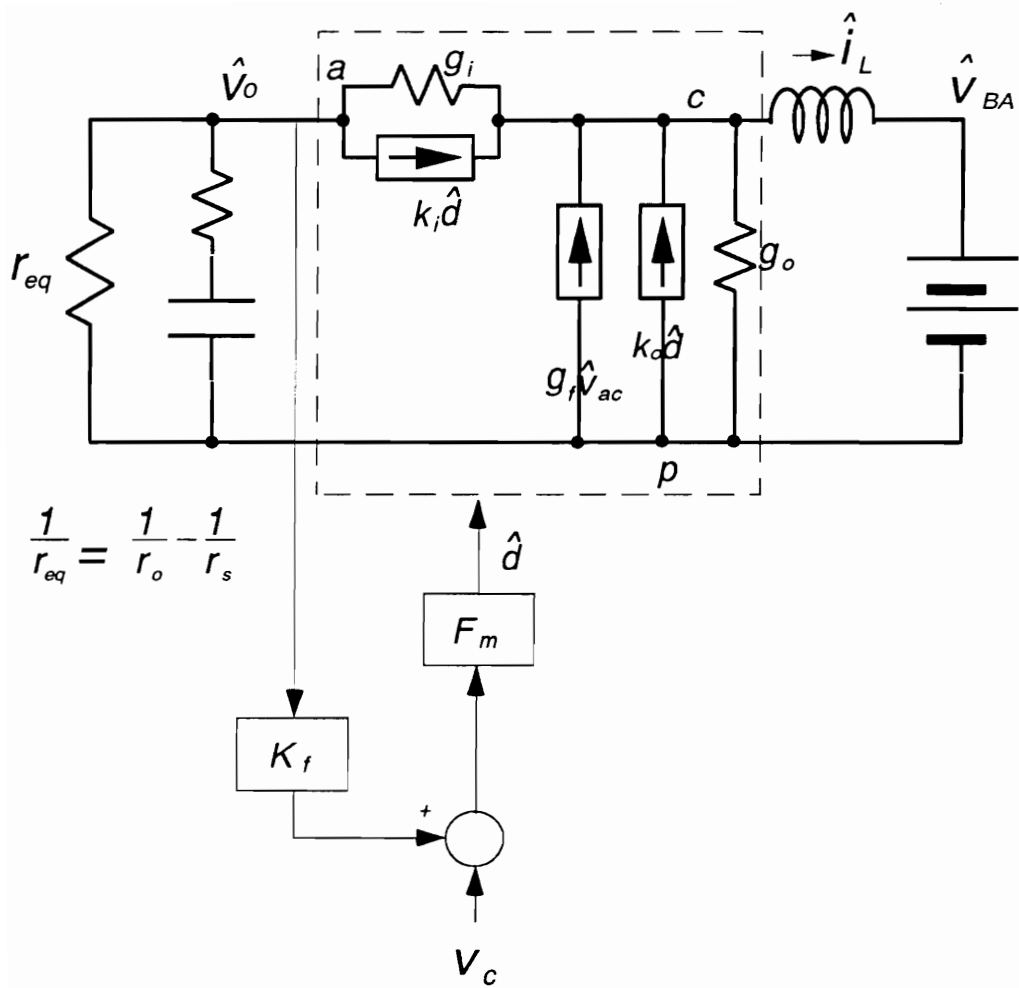


Figure 3.24. Small-Signal Model of Charger using CMC in DCM

$$\begin{aligned}
G_d &= - \frac{2V_O(1 - M)r_{eq}}{D\{R(1 - M) + r_{eq}\}} \\
\omega_z &= \frac{RM^2(1 - M)}{L(1 - M + 2M^2)} \\
\omega_{p1} &= \frac{RM^2\{R(1 - M) + r_{eq}\}}{r_{eq}(1 - M)(R^2CM^2 + L) + RL} \\
\omega_{p2} &= \frac{r_{eq}(1 - M)(R^2CM^2 + L) + RL}{RLCr_{eq}}
\end{aligned} \tag{3.46}$$

Substituting of Eq. (3.45) into (3.44), the DCM control-to-output transfer function with the current-loop closed becomes

$$\frac{\hat{v}_o}{\hat{v}_c} \equiv F_v \simeq F_m G_c \frac{(1 + \frac{s}{\omega_z})(1 + sR_cC)}{(1 + \frac{s}{\omega_{c1}})(1 + \frac{s}{\omega_{c2}})} \tag{3.47}$$

where

$$\begin{aligned}
G_c &= \frac{G_d}{1 - K_f F_m G_d} < G_d \\
|\omega_{c1}| &< |\omega_{p1}|
\end{aligned} \tag{3.48}$$

$G_d$  and  $\omega_{p1}$  represent the dc gain and the pole of the duty cycle-to-output voltage transfer function in DCM shown in Eq. (3.45). The dc gain  $G_c$  is positive and the low frequency pole  $\omega_{c1}$  is a RHP pole. Compared with the single loop case, dc

gain is lower and locations of poles are moved close to the origin. However, since the coefficient  $K_f$  is very small in practical cases, the difference is negligible. Thus current-mode control's control-to-output transfer function in DCM can be approximated to that of voltage-mode control.

### 3.4.3 Control-Loop Design of the Current-Mode Controlled Charge Regulator

As given in Eqs. (3.40) and (3.47), the control-to-output transfer functions for CCM and DCM have similar low frequency characteristics. They have positive dc gains and low frequency RHP poles. In CCM, as the charge current increases, the magnitude of the dc gain of  $F_v$  decreases, and the RHP pole moves towards higher frequency. However their effects in  $F_v$  cancel each other at higher frequencies.

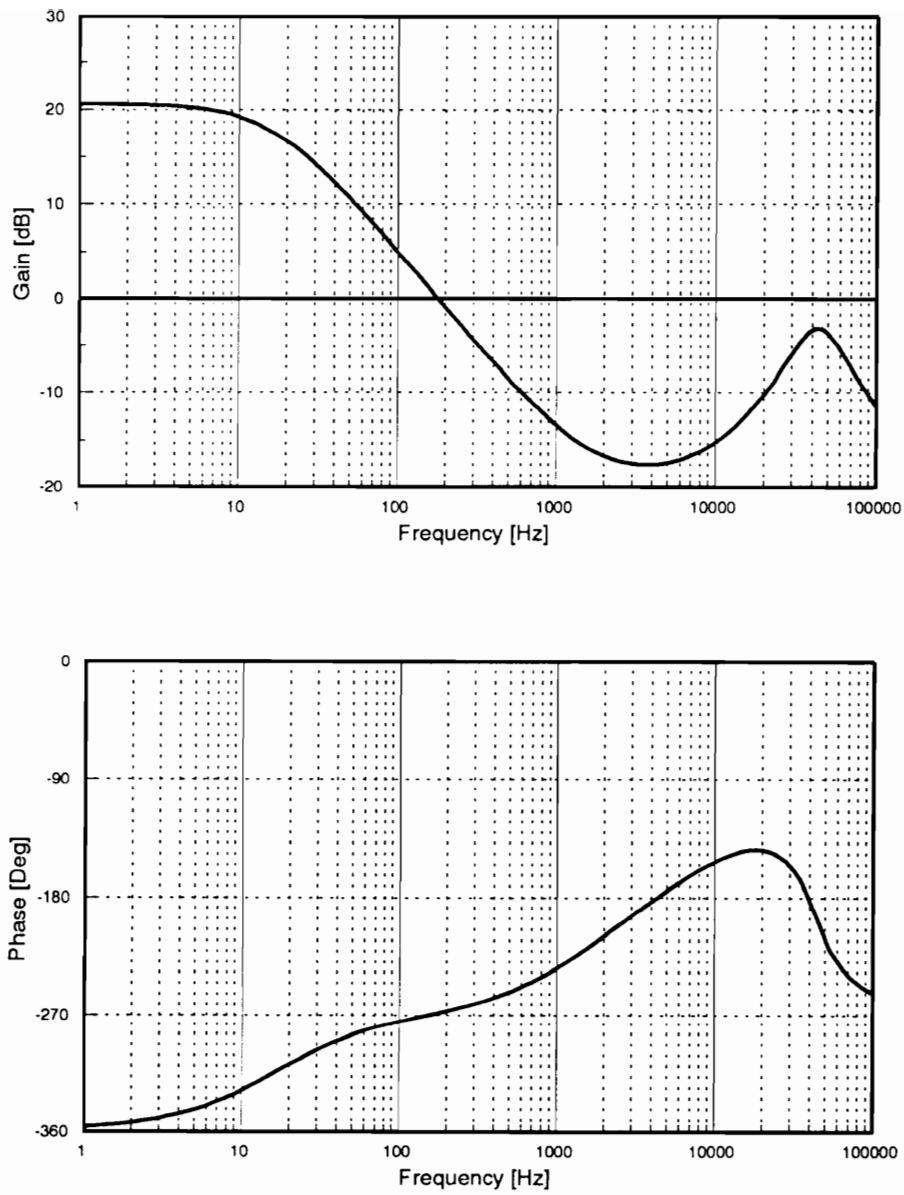
In CCM, the main variation in  $F_v$  comes from the moving zero as in the voltage-mode control. Thus loop gain should be designed at the maximum charge current as the worst case which limits the crossover frequency. Since  $F_v$  in DCM has the same characteristics as voltage-mode control, the loop gain should be designed at the minimum charge current in the DCM as the worst case where the minimum phase margin specification has to be satisfied.

The same power stage parameter values used in voltage-mode control are employed as an example. Figures 3.25 and 3.26 present the control-to-output transfer function with the current-loop closed at two extreme cases ( the maximum current in CCM and the minimum current in DCM). They show around 12 dB difference in dc gain, which is much smaller than the voltage-mode control case. The peaking in the high frequency of the CCM curve results from two zeros and a complex pole pair.

As in voltage-mode control, four extreme conditions for the given parameter values are summarized in Table 3.2.

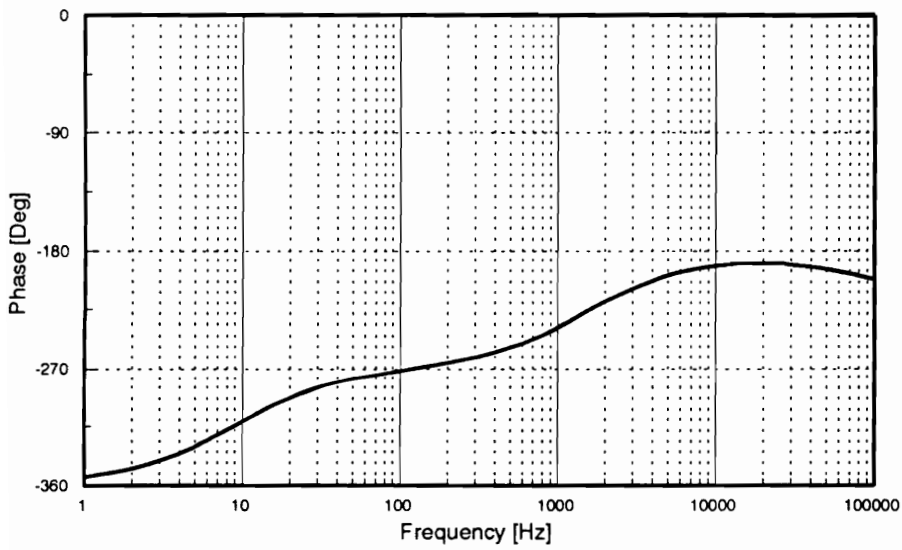
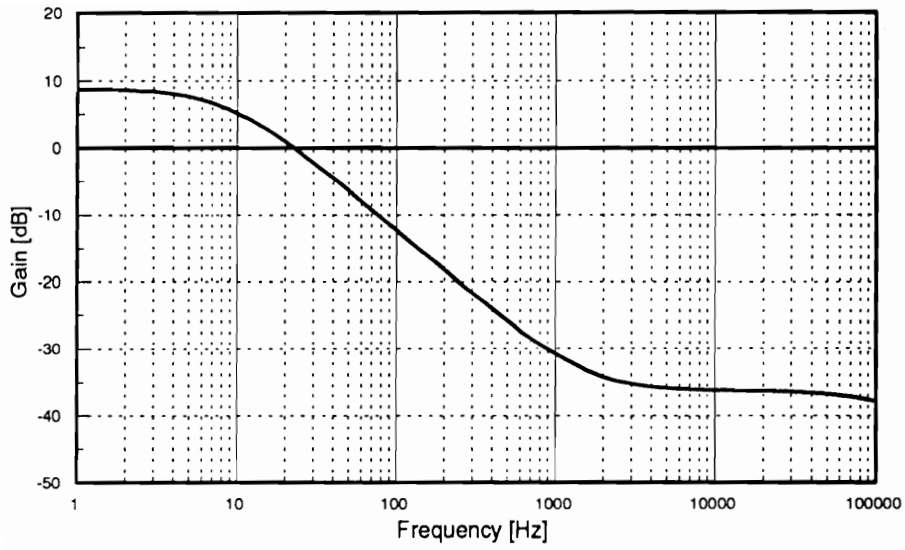
As discussed for the DCM case of voltage-mode control, even though the control-to-output transfer function  $F_v$  has a positive dc gain, a positive gain feedback compensator should be used to stabilize the system due to the nonminimum phase nature of the system.

A compensator which has an integrator, a pole and a zero is employed. The gain of the integrator is determined by the highest gain condition of  $G_x$  in Eq. (3.40) in CCM for the maximum possible loop-gain crossover frequency. The zero is placed to satisfy the 30 degree phase margin of the loop gain at the minimum charge current in DCM. A pole is set to cancel the esr zero or  $\omega_v$ , whichever comes first. The designed compensator parameters are:



**Figure 3.25. Control-to-Output Transfer Function of the CMC Charger in CCM Worst Case**





**Figure 3.26. Control-to-Output Transfer Function in DCM Worst Case**

**Table 3.2 Control-to-Output Transfer Function Data in Current-Mode Control**

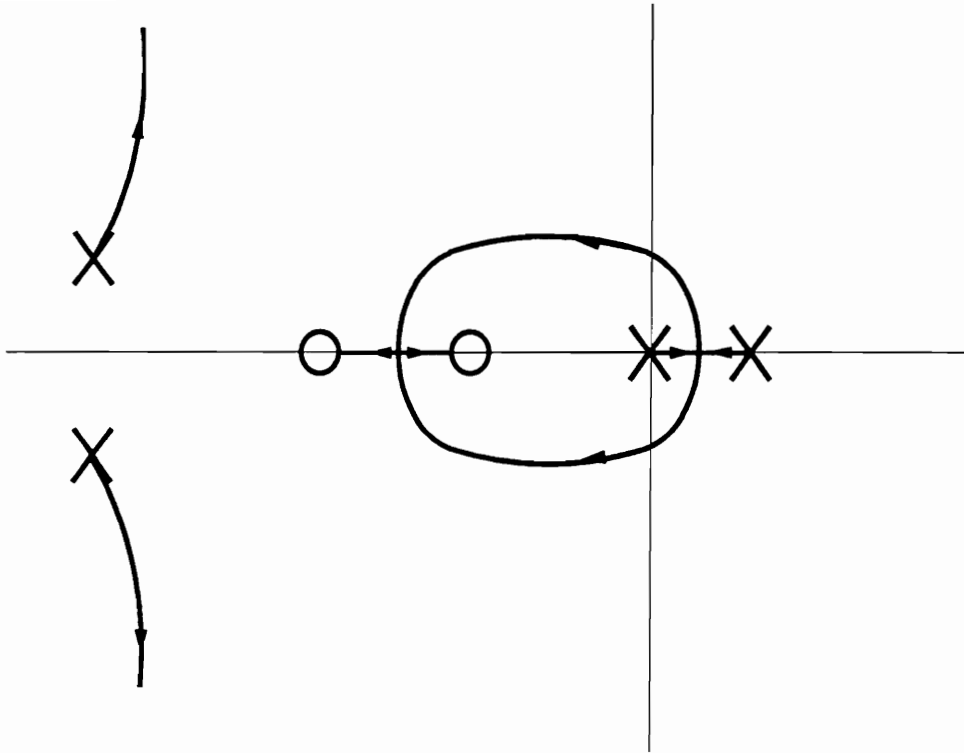
	DCM		CCM	
	$I_{Lmin} = 0.2 \text{ A}$	$I_{Lmax} = 3.3 \text{ A}$	$I_{Lmin} = 3.3 \text{ A}$	$I_{Lmax} = 23 \text{ A}$
$R_{dc}$	1,056 ohm	67 ohm	67 ohm	9.7 ohm
$r_{eq}$	- 8.8 ohm	- 8.8 ohm	- 8.8 ohm	- 8.8 ohm
$D$	0.13	0.54	0.54	0.54
$G_d$	3.1	12.7	17.5	10.4
$W_{z1}$	10 e3	10 e3	10 e3	10 e3
$W_{z2}$	1.55 e6	397 e3	396 e3	58 e3
$W_n$			275 e3	275 e3
$Q$			1.25	1.25
$W_{p1}$	- 55.5	- 50.9	- 61.9	- 108
$W_{p2}$	710 e3	183 e3		
$F_V = G_d \frac{(1 + s/W_{z1})(1 + s/W_{z2})}{(1 + s/W_{p1})(1 + s/W_{p2})}$			$G_d \frac{(1 + s/W_{z1})(1 + s/W_{z2})}{(1 + s/W_{p1})(1 + s/QW_n + s^2/W_n^2)}$	

$$H_v = \frac{70,000}{s} \frac{(1 + \frac{s}{4,100})}{(1 + \frac{s}{10,000})}$$

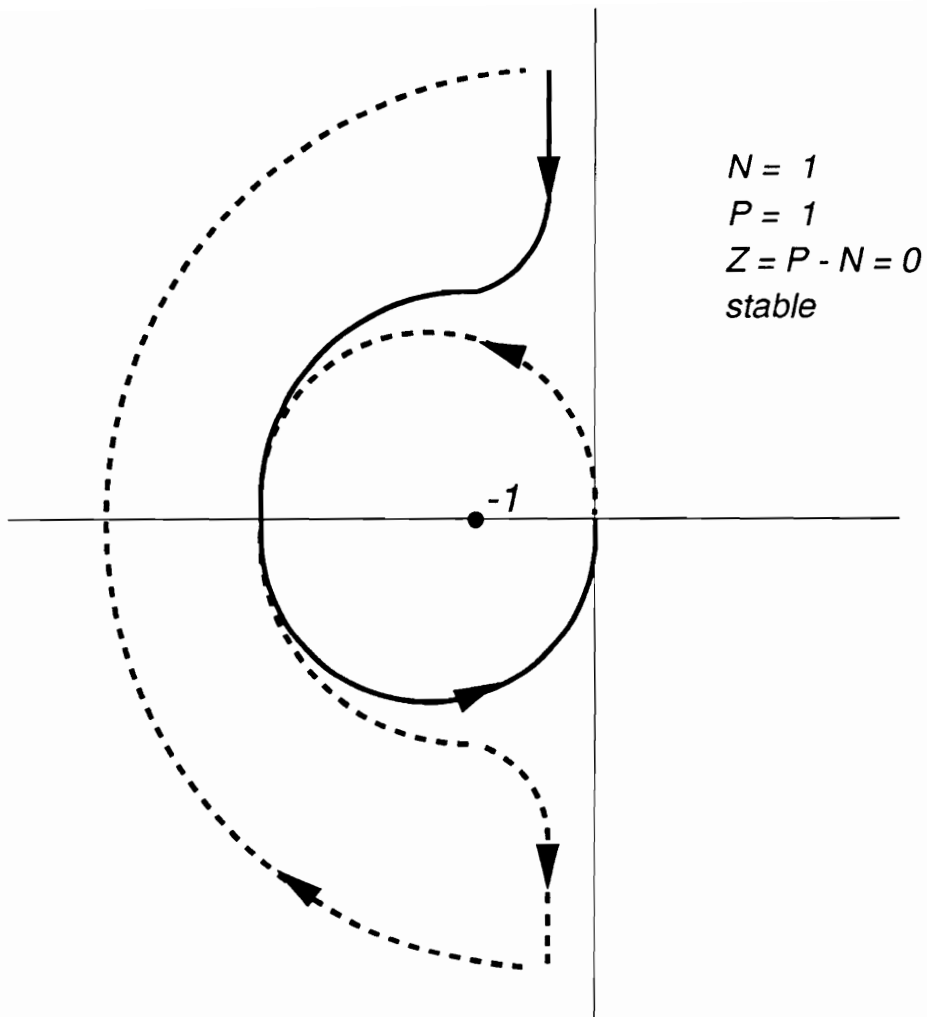
Figure 3.27 shows the root locus of the loop gain in CCM. Due to the RHP open-loop pole a conditionally stable system occurs. Closed-loop stability for the desired gain is examined by use of the Nyquist criterion using a polar plot of the loop gain shown in Fig. 3.28. The loop gain has one RHP pole, and the polar plot shows one encirclement. Thus the system is stable for a designed gain.

A Bode plot of the loop gain at the worst case in CCM is shown in Fig.3.29. It shows 48 dB gain margin and 90 degree phase margin. Figure 3.30 shows the closed-loop bus impedance at the worst case CCM.

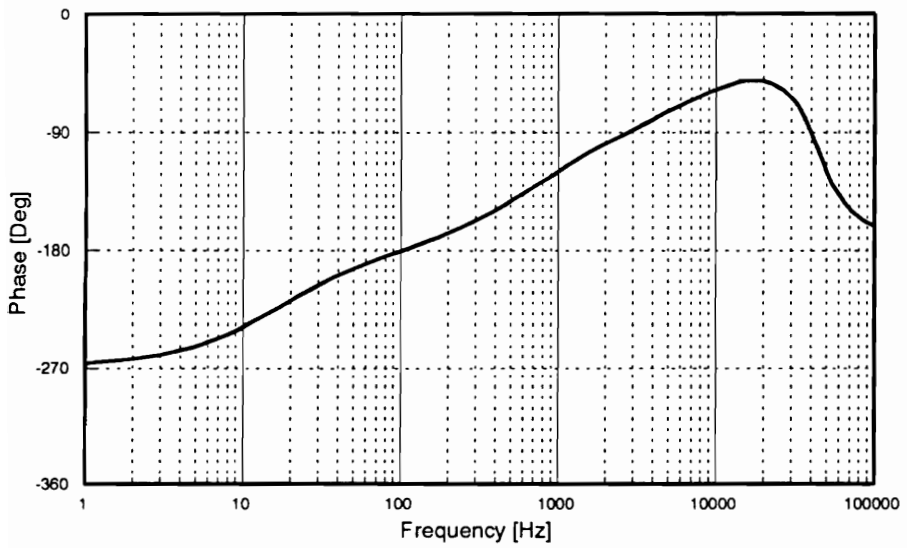
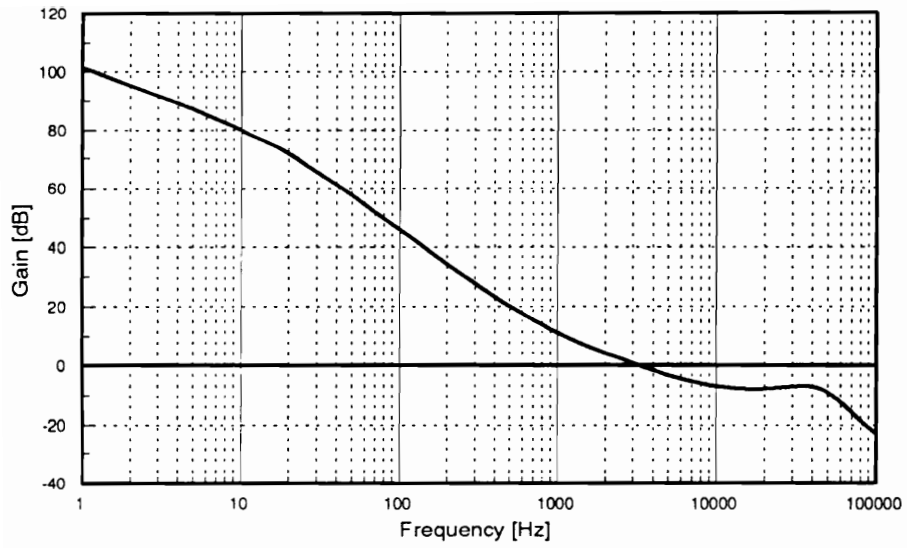
A loop gain characteristic at the worst case DCM using the same compensator of CCM is shown in Fig. 3.31. The dc gain of the loop gain was reduced about 10 dB from the CCM case. The bus impedance at the worst case DCM is presented in Fig. 3.32. The bus impedance remains low even in the DCM worst condition. Compared with the voltage-mode control case, current-mode control exhibits superior performance in DCM. This is because the low frequency characteristics in DCM and CCM are similar to each other and the difference in dc gain between the two extreme cases is much smaller than with voltage-mode control.



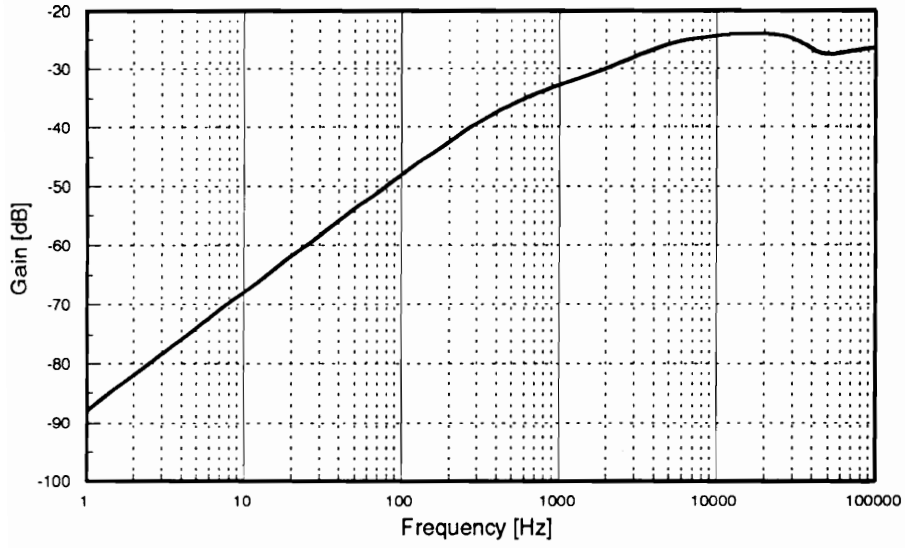
*Figure 3.27. Root Locus of Loop Gain in Current-Mode Control*



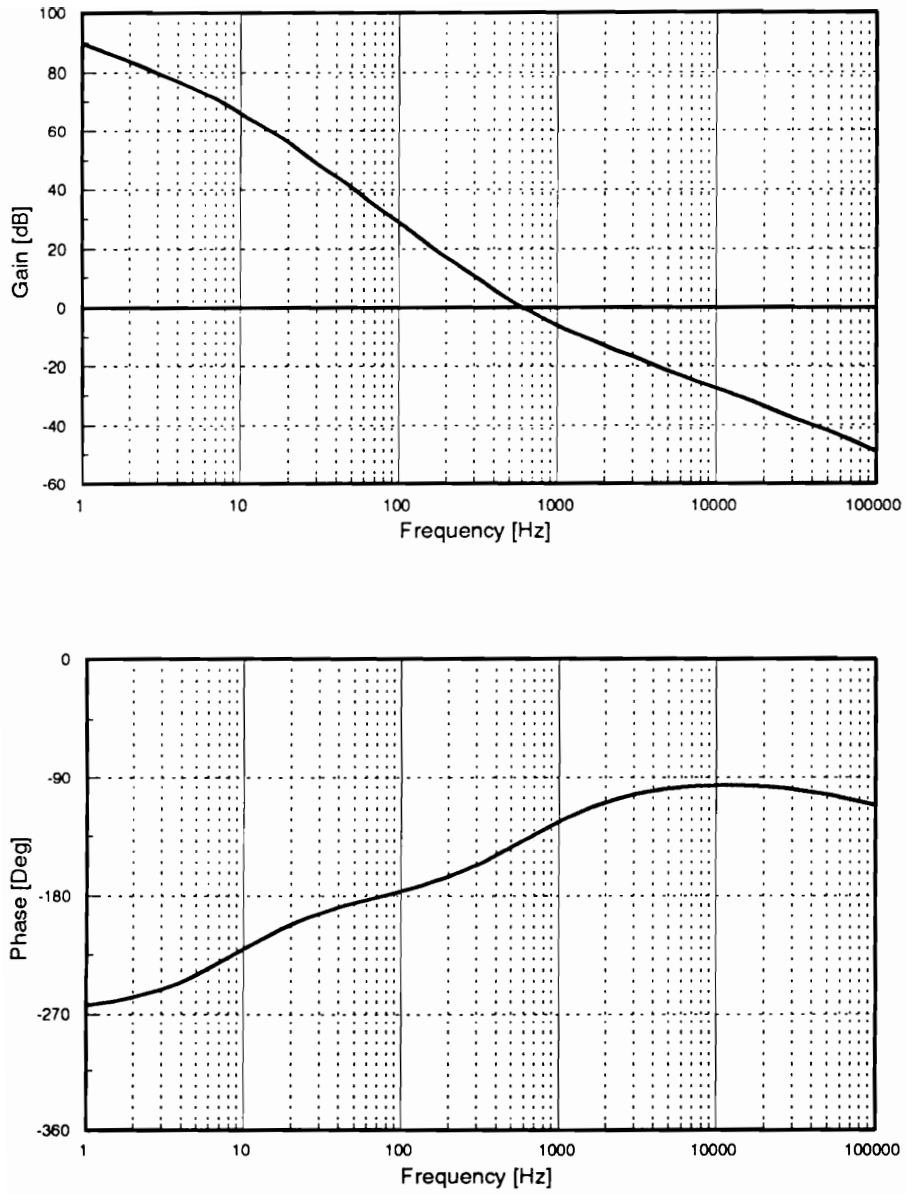
*Figure 3.28. Polar Plot of the Loop Gain of Current-Mode Control*



*Figure 3.29. Loop Gain at CCM Worst Case*

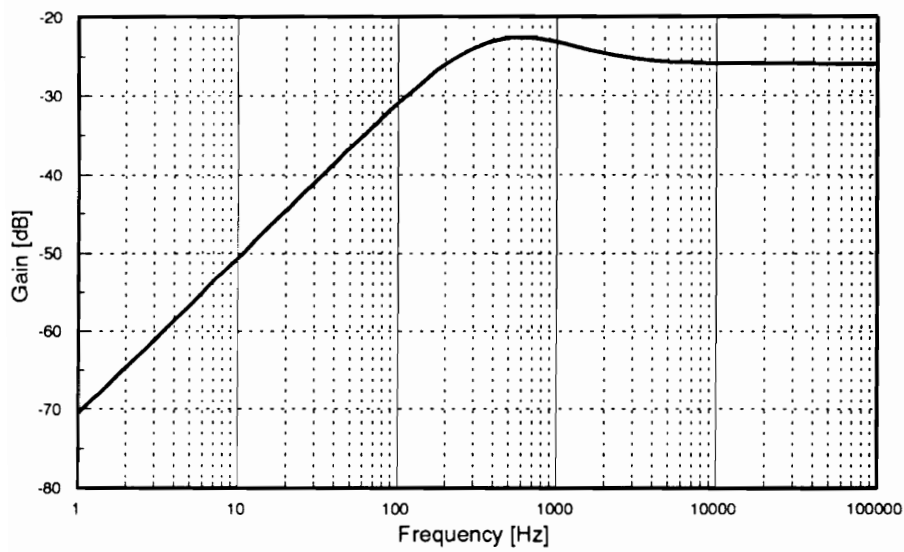


*Figure 3.30. Bus Impedance in CCM Worst Case*



*Figure 3.31. Loop Gain in DCM Worst Case*





**Figure 3.32. Bus Impedance in DCM Worst Case**

### ***3.5 Analysis of the Nonminimum Phase Charger System***

As discussed in previous sections, the charger system in the bus voltage regulation mode is conditionally stable in DCM with voltage-mode control as well as in both DCM and CCM with the current-mode control. If the feedback gain is reduced below the gain margin, the system becomes unstable. Also the system is unstable in the open-loop condition.

In the small-signal sense, one can always assure that the gain is high enough to ensure stability. However, in the large-signal sense, a low gain may occur during a transient. For instance, the error amplifier in the feedback compensator circuit may be saturated before start-up and it may take some time to bring the amplifier into the linear region. During this period, the regulator may go through the open-loop unstable condition. In order to investigate these problems, possible practical cases are set up and simulated.

First, to illustrate the conditional stability, simulations are performed using the large-signal model of the charger system. A simulation case is set up such that integrator gains are reduced by 60 dB at 2 msec for the chargers employing

voltage-mode control and current-mode control operating in CCM. Figure 3.33 shows the simulation results for both systems. Since the charger using voltage-mode control is stable in CCM even at very low gain, the bus voltage and charge current settle down as shown in Fig. 3.33(a). However, for the charger employing the current-mode control, system become unstable due to the lowered gain as shown in Fig. 3.33(b). Since the dominant eigenvalue locates near the origin, system goes unstable slowly.

Figure 3.34 shows the start-up transients for charger systems employing voltage-mode control and current-mode control. The feedback compensator gain was increased linearly from zero to the designed value from 0 to 2 msec. Initial conditions of charge current and all control variables are set to zero. Even though the charger passes through the unstable region, the controller begins regulating as soon as there is sufficient gain to stabilize the system. The charger employing current-mode control shows less overshoot and a faster settling time than the voltage-mode control charger.

The cases presented here, of course, are large-signal problems. However, the results show that there is no detrimental effect of the conditional stability.

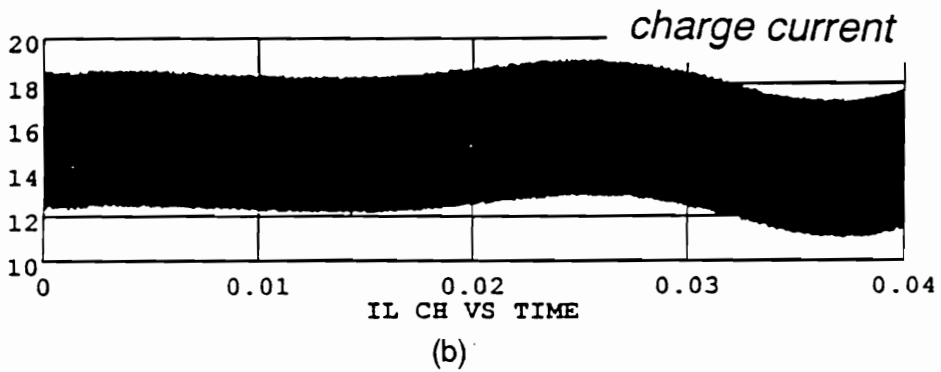
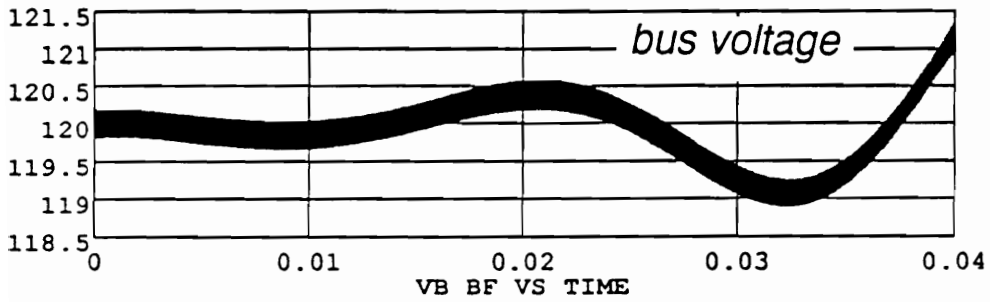
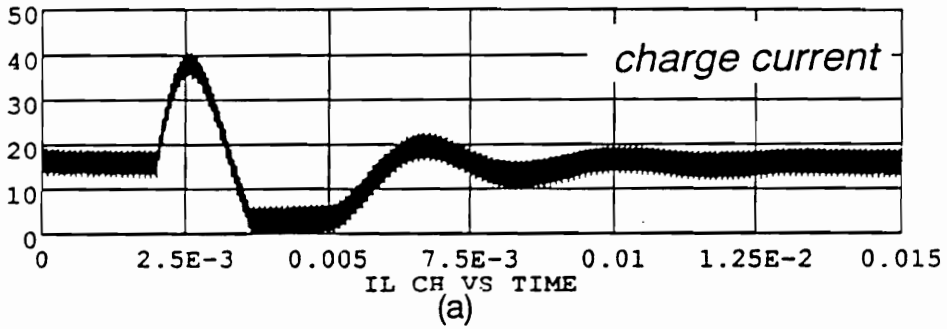
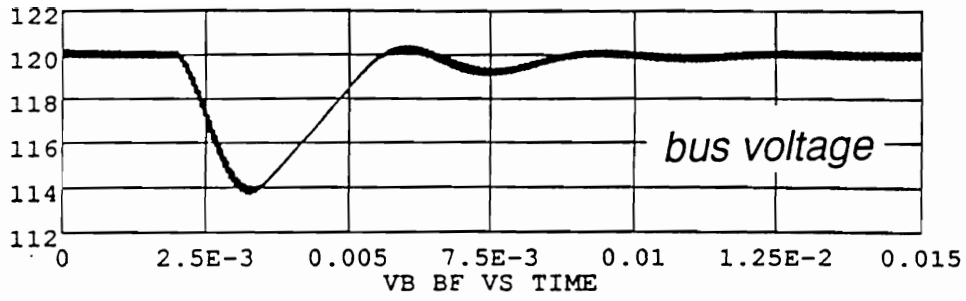
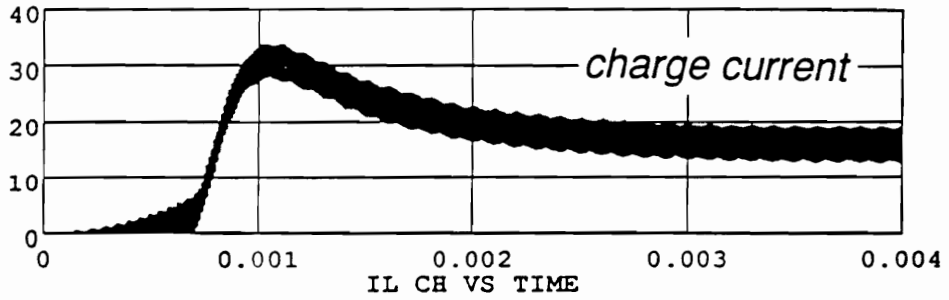
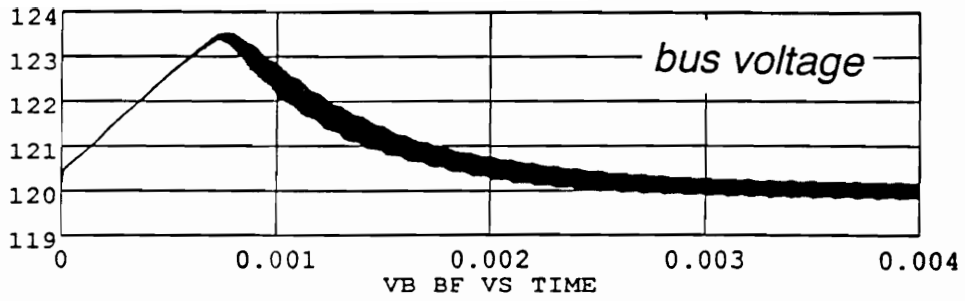


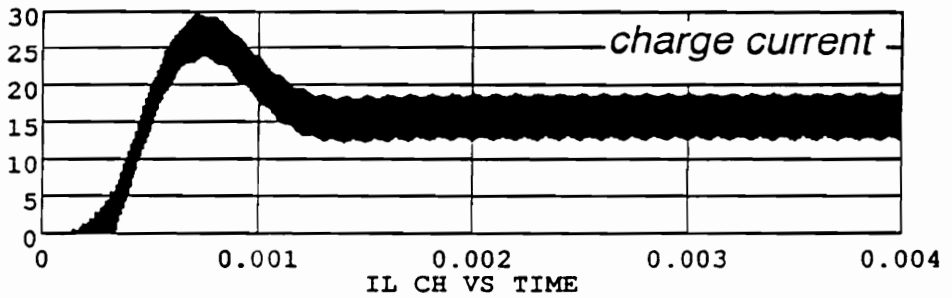
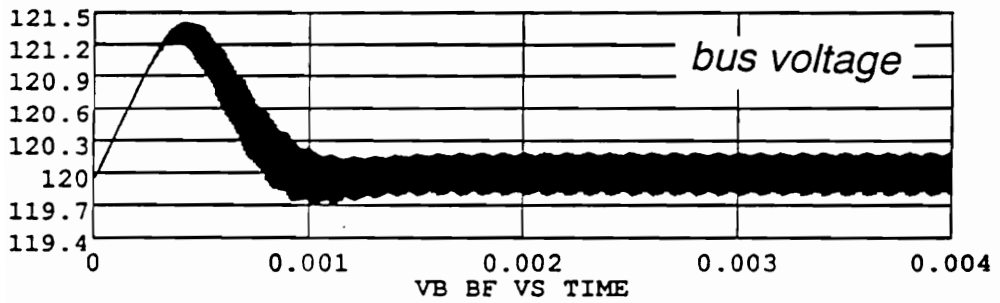
Figure 3.33. Transient Response for the Step Gain Change

(a) voltage-mode control

(b) current-mode control



(a)



(b)

**Figure 3.34. Transient Response for the Start-Up**

(a) voltage-mode control

(b) current-mode control

### 3.6 *Summary*

When the charger operates in the bus voltage regulation mode, the output terminal characteristic of the charger is quite different from those of conventional switching regulators. The equivalent load impedance is the parallel combination of the dynamic impedance of the solar array output and the constant power load. The equivalent impedance, therefore, is negative. Switching regulator in the battery charger system operates in the unique mode such that the input voltage is regulated. Even though a buck topology is used for the charger, its dynamic behavior is much like the boost converter except that the power flows in the reverse direction.

When the voltage-mode control is employed, the control-to-output voltage transfer function in CCM has a negative dc gain, two LHP zeroes and a complex pole pair. The complex pole pair resides in either LHP or RHP according to the circuit parameters. For regulation of the bus voltage, a positive compensator gain should be used to achieve overall negative feedback action. In DCM, the control-to-output transfer function has a positive dc gain and a low frequency RHP pole resulting in a nonminimum phase system. Even though it has a positive dc gain, a positive compensation gain is required. Thus, the same compensator used in CCM can be employed.

When the current-mode control is used, the control-to-output transfer function with the current-loop closed has a positive dc gain, a low frequency RHP pole and a high frequency complex pole pair in CCM. The control-to-output transfer function in DCM is approximately same with that of the voltage-mode control in DCM. A positive compensation gain is required to regulate the bus voltage in both CCM and DCM.

Since the charger operates both in CCM and DCM, the control loop should be designed for both modes. When voltage-mode control is used, it is difficult to achieve good performance in both modes due to the low frequency RHP pole and the large difference in dc gain between CCM and DCM. On the contrary, the current-mode control gives superior performance operated in both CCM and DCM. That is because the control-to-output transfer functions in the DCM and the CCM have similar low frequency characteristics.

In the bus voltage regulation mode, charger systems are unstable under open-loop condition and conditionally stable when the feedback loop is closed. However, as long as the gain margin is sufficient, it does not have any detrimental effects.

# Chapter 4

## Small-Signal Analysis of the Charger in Charge-Current Regulation Mode

### *4.1 Introduction*

As the charge current increases to the preset limit, the bus voltage regulation loop becomes disabled and the charge current regulation loop is activated. During the charge current regulation mode, a buck switching regulator provides a constant charge current to the battery at a selected rate. Several different charging rates may exist, depending upon the voltage/temperature (V/T) status



of the battery. Charge current is tapered back to trickle charge if the battery voltage and temperature rise above a preset V/T limit.

During this period, the bus voltage is regulated by the shunt regulator, and the bus voltage becomes a stiff voltage source to the charger. Thus the charger's input terminal dynamics, including the bus filter capacitor are absorbed by this voltage source. The duty cycle of the charger is therefore fixed by the bus voltage and the battery voltage.

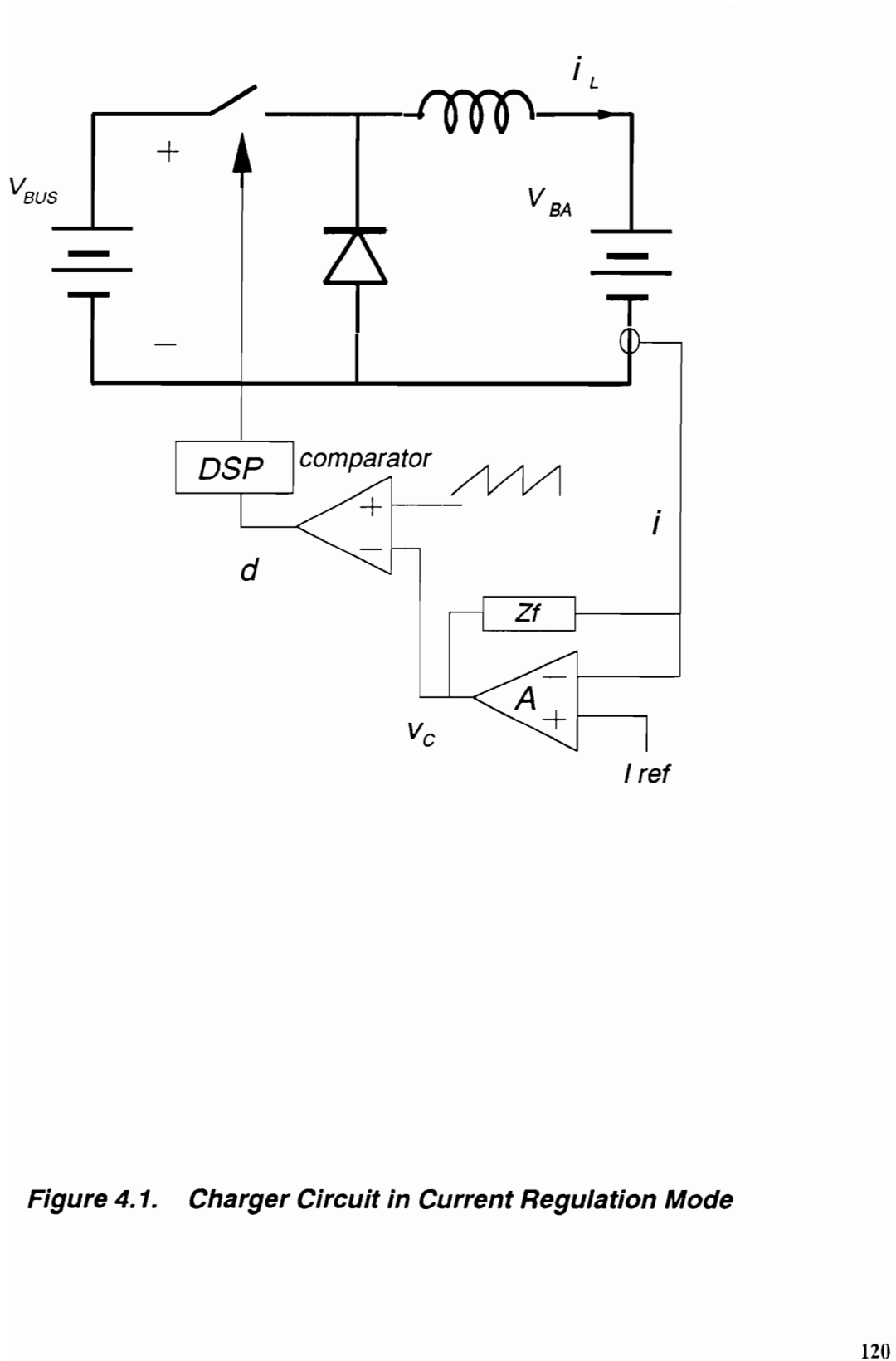
$$D = \frac{V_{BA}}{V_{Bus}} \quad (4.1)$$

As shown in Fig. 4.1, to regulate the charge current, a sensed charge current,  $i_L$ , is compared with a reference current. The difference is amplified by an error amplifier to generate a control voltage.

$$(i_L - I_{ref}) A = v_c \quad (4.2)$$

$$v_c F_m = d \quad (4.3)$$

where  $A$  is the error amplifier gain and  $F_m$  is the PWM gain. Since the duty cycle is a fixed constant value which is determined by the bus voltage and battery voltage, from Eq. (4.3), the control voltage  $v_c$  is also fixed according to the steady-state duty cycle regardless of  $I_{ref}$  value. Therefore, from Eq. (4.2), a large gain of  $A$  provides a small error in  $i_L - I_{ref}$ .



**Figure 4.1. Charger Circuit in Current Regulation Mode**

In order to maintain the fixed duty ratio, however, the charge current should be regulated. Unless charge current is regulated, the converter will be unstable because both input and output of the converter are stiff voltage sources.

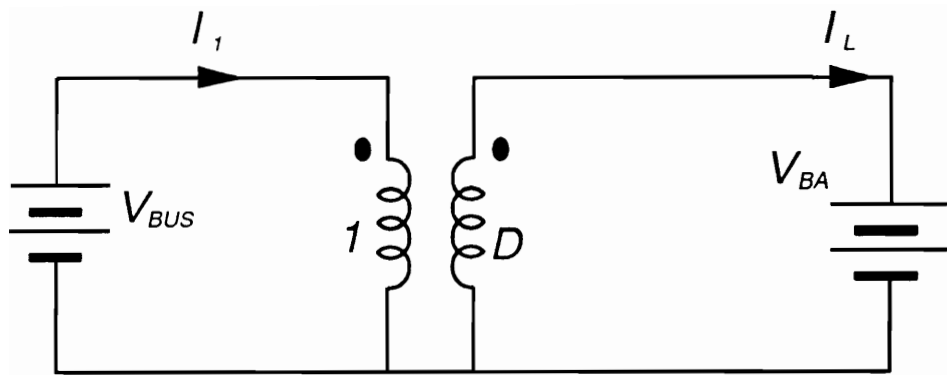
## 4.2 Continuous Conduction Mode

### 4.2.1 Small-Signal Analysis

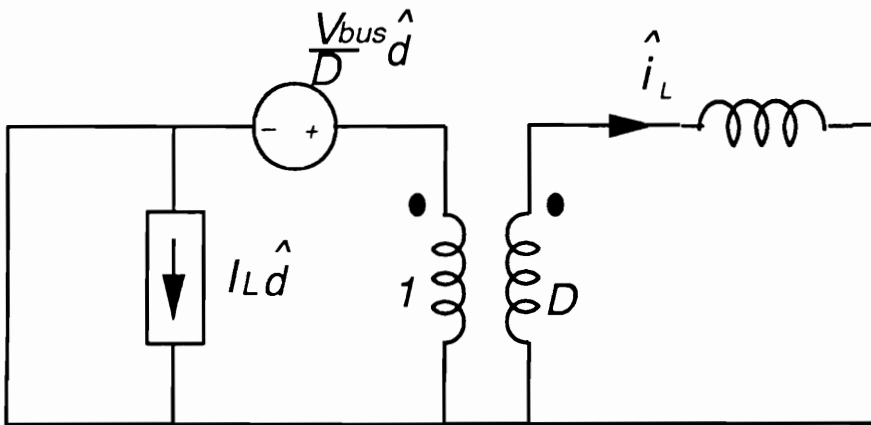
Figure 4.2 shows dc model and small-signal model of the charger in the current regulation mode. The PWM switch model is implemented. From the Fig. 4.2(a) the steady-state duty cycle is given by

$$D = \frac{V_{BA}}{V_{Bus}} = \frac{I_L}{I_{in}} \quad (4.4)$$

Small-signal model is generated by substituting the PWM switch model to the Fig. 4.1. Since the bus voltage and battery voltage are stiff voltage sources, it is assumed that both  $\hat{v}_{Bus}$  and  $\hat{v}_{BA}$  are zero. Then small-signal model shown in Fig. 4.2(b) is obtained. From the Fig. 4.2(b), we get



(a)



(b)

**Figure 4.2. Charger CCM Model in Current Regulation Mode**

(a) dc model

(b) small-signal model

$$\frac{V_{Bus}}{D} \hat{d} = L \frac{d\hat{i}_L}{dt} \quad (4.5)$$

From Eq. (4.5) the control-to-charge current transfer function is given by

$$G_d = \frac{\hat{i}_L}{\hat{d}} = \frac{V_{Bus}}{L s} \quad (4.6)$$

#### 4.2.2 Regulator Design

To design the closed-loop system, control loop-gain , T, is defined.

$$T = H_i F_m G_d = H_i F_m \frac{V_{Bus}}{L s} \quad (4.7)$$

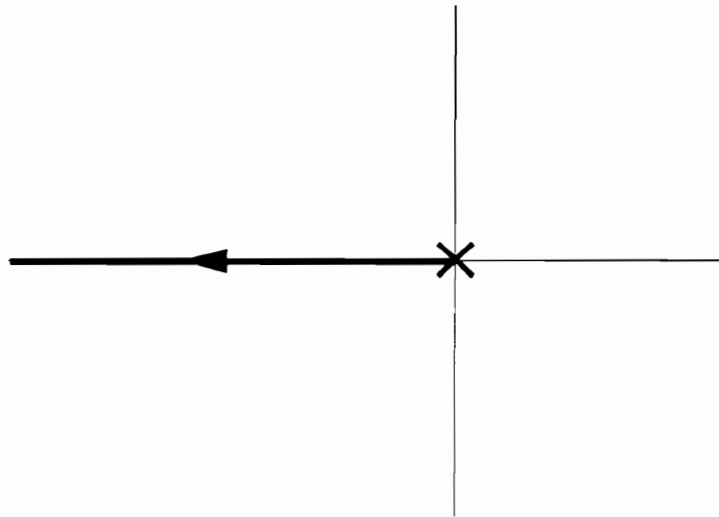
where  $H_i$  is a feedback compensator. Figure 4.3(a) shows root locus of the loop-gain when a simple feedback gain is used, and Fig. 4.3(b) presents root locus for integrator plus a zero compensator. The loop gain of Eq. (4.7) is stable for any constant gain of  $H_i$ , and the steady-state error for step change of the current reference can be zero. However, for a constant feedback gain, switching ripple of the inductor current is amplified and generates steady-state error during the PWM process. In order to eliminate the steady-state error, the inductor current should be averaged. The averaging can be achieved by using an integrator in the

compensator. When an integrator is used, the loop-gain has double poles at the origin providing no steady-state error for linear change as well as a step change of current reference. In addition to an integrator, a zero is necessary to achieve proper phase margin.

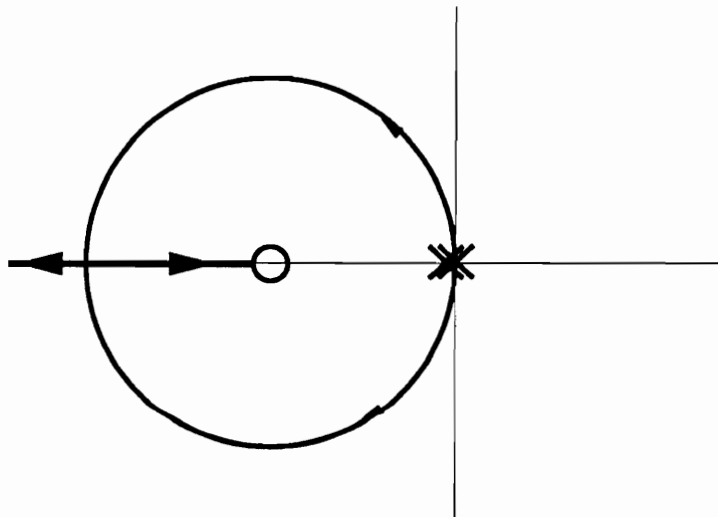
Figure 4.4 shows the simulation result of the step change of the current reference. In Fig. 4.4,  $I_{ref}$  is set to 30 A, then at 2 ms,  $I_{ref}$  is step changed to 20 A. Notice that the control voltage,  $v_c$ , is the same before and after the step change of the current reference, while the charge current is regulated at different value. Figure 4.5 presents the current regulation for a linear change of the current reference. The current reference is changed linearly from 30 A to 10 A. It shows that steady-state error does not exist.

### ***4.3 Discontinuous Conduction Mode***

Even though battery is fully charged, trickle charger is active to compensate the leakage in the battery. It charges the battery with a small current to maintain the battery in full state-of-charge. In this case, the charger operates in DCM.

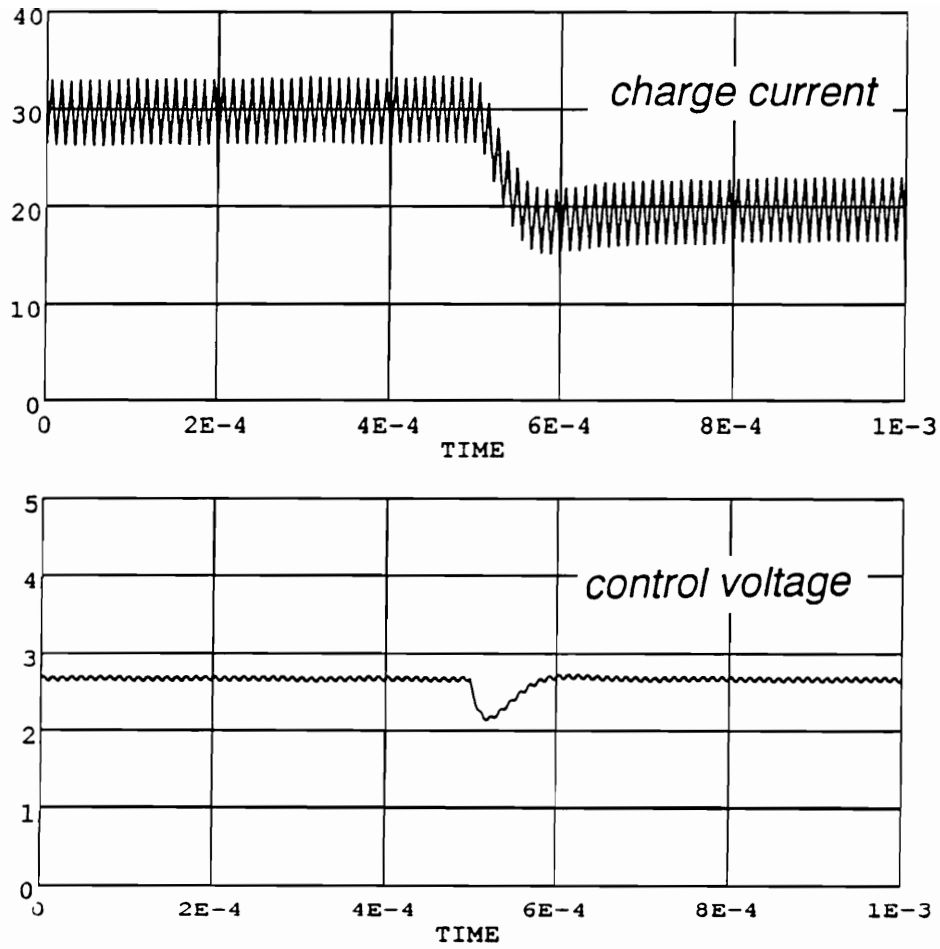


(a)



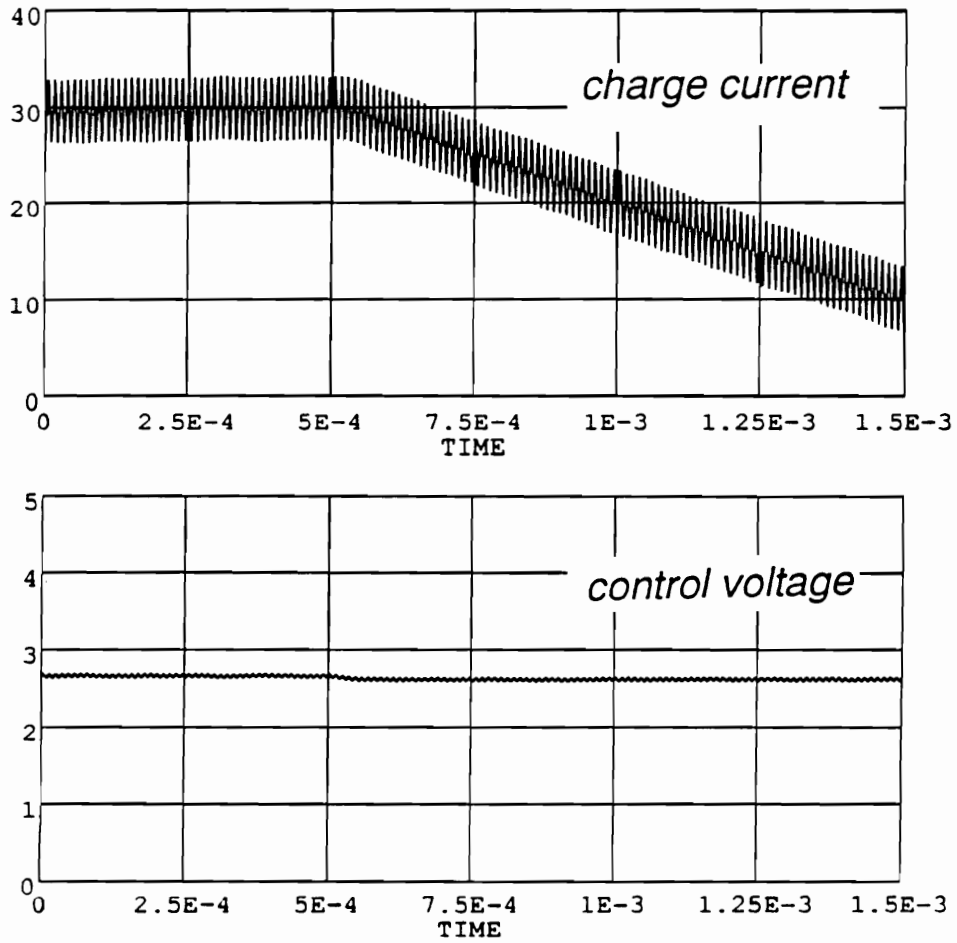
(b)

**Figure 4.3.** *Root Loci of Loop Gain in Current Regulation Mode*  
(a) *simple gain compensator*  
(b) *integrator plus zero compensator*



*Figure 4.4. Transient Response for Step Change in the Current Reference*





*Figure 4.5. Transient Response for Linear Change of the Current Reference*

### 4.3.1 DC Analysis

Under dc conditions, substitution of the PWM switch model results in Fig. 4.6.

From the Fig. 4.6, we get

$$I_L = I_{in} + I_p = \left(1 + \frac{1}{\mu}\right) I_{in} \quad (4.8)$$

$$V_{BA} = \mu V_{ac} = \mu(V_{Bus} - V_{BA}) \quad (4.9)$$

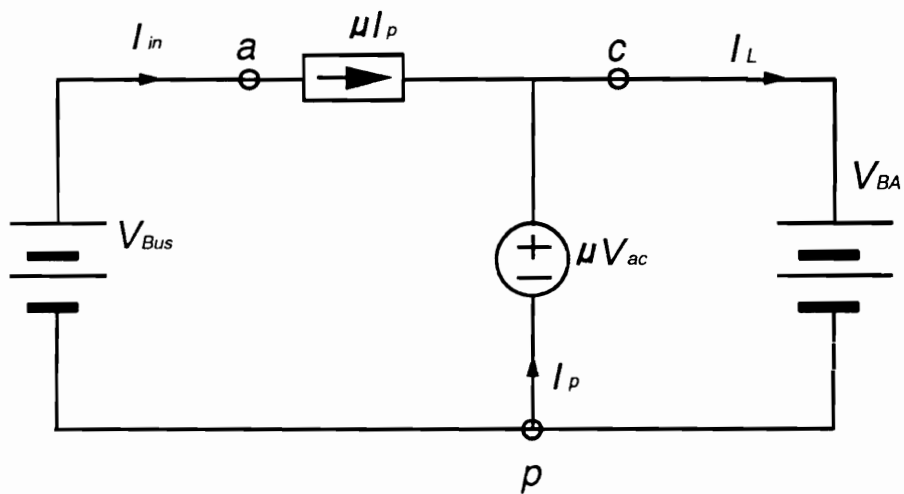
From Eqs. (4.8) and (4.9),

$$M \equiv \frac{I_{in}}{I_L} = \frac{V_{BA}}{V_{Bus}} = \frac{1}{1 + \frac{1}{\mu}} \quad (4.10)$$

The amplification factor  $\mu$  of the PWM switch model is:

$$\mu = \frac{D^2}{2LF_s} \frac{V_{cp}}{I_a} = \frac{D^2}{2LF_s} \frac{V_{BA}}{I_{in}} = \frac{D^2}{2LF_s} \frac{V_{Bus}}{I_L} \quad (4.11)$$

Substitution of (4.11) in (4.10) gives



**Figure 4.6.** DC Model of Charger in DCM

$$D = \sqrt{\left(\frac{1}{M} - 1\right) \frac{I_L}{2LF_s V_{Bus}}} \quad (4.12)$$

The critical value of charge current which determines the boundary between CCM and DCM is obtained from (4.12) by letting  $D = M$ .

$$I_L|_{crit} = \frac{M(1 - M) V_{Bus}}{2LF_s} = \frac{(1 - M) V_{BA}}{2LF_s} \quad (4.13)$$

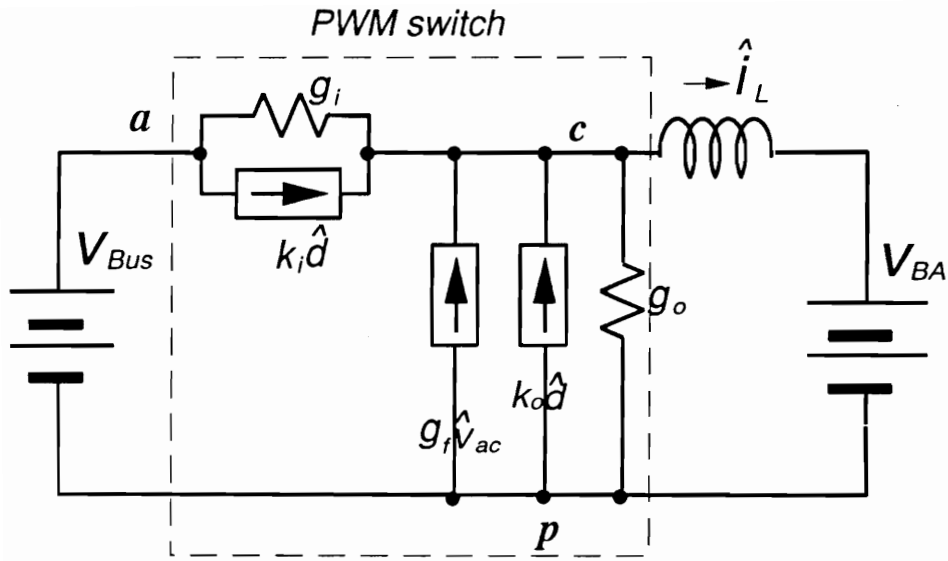
### 4.3.2 Small-signal Analysis

Figure 4.7(a) represents small-signal model of charger employing PWM switch model. Since  $\hat{v}_{Bus}$  and  $\hat{v}_{BA}$  are zero, Fig. 4.7(a) can be simplified to Fig. 4.7(b). From the Fig. 4.7(b), we get

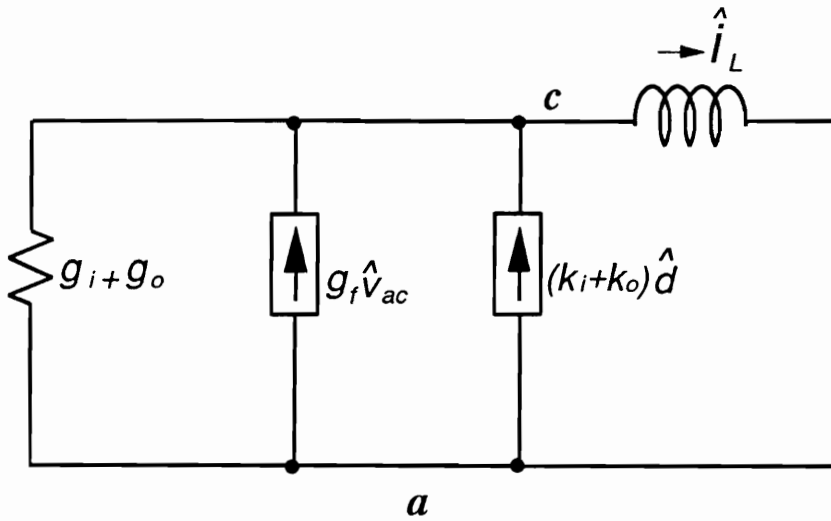
$$(g_f + g_i + g_o) \hat{v}_{ac} + (k_i + k_o) \hat{d} = \hat{i}_L \quad (4.14)$$

$$\hat{v}_{ac} = -L s \hat{i}_L \quad (4.15)$$

From Eqs. (4.11) and (4.12), the control-to-charge current transfer function is given by



(a)



(b)

**Figure 4.7. Small-Signal Model of Current Regulation in DCM**  
 (a) small-signal model using PWM switch  
 (b) simplified small-signal model

$$\frac{\hat{i}_L}{\hat{d}} = \frac{k_i + k_o}{1 + (g_i + g_o + g_f) L s} \quad (4.16)$$

where

$$\begin{aligned} k_i + k_o &= \frac{2}{D} (I_a + I_p) = \frac{2}{D} I_L \\ g_i + g_o + g_f &= \frac{I_a}{V_{ac}} + \frac{2I_p}{V_{ac}} + \frac{I_p}{V_{cp}} = \frac{I_L}{(1 - M) V_{BA}} \end{aligned} \quad (4.17)$$

Substituting Eq. (4.14) into (4.13), we get

$$\frac{\hat{i}_L}{\hat{d}} = \frac{2 I_L}{D} \frac{1}{1 + \frac{s}{\omega_p}} \quad (4.15)$$

where

$$\omega_p = \frac{(1 - M) V_{BA}}{I_L L} \quad (4.16)$$

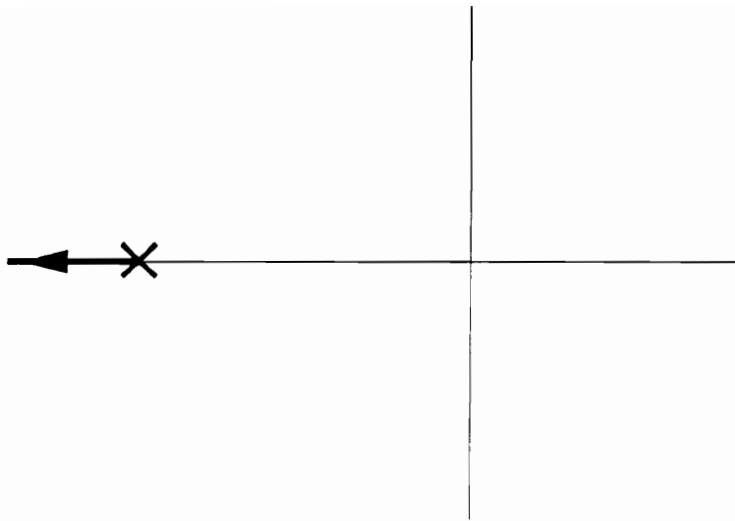
Once the current reference of the trickle charge is determined, the dc gain and location of pole  $\omega_p$  are fixed because the battery voltage is fixed. In practical case, the pole  $\omega_p$  locates at very high frequency (higher than the switching frequency). Thus the control-to-charge current transfer function can be considered as a constant which is the dc gain  $\frac{2 I_L}{D}$ . The root locus of the loop-gain for a simple gain is shown in Fig. 4.8(a), and Fig. 4.8(b) presents root locus for integrator plus zero compensator. When a simple gain feedback is used, very fast

response can be achieved, but steady-state error occurs. The integrator plus zero compensator gives no steady-state error, however, the response is slower.

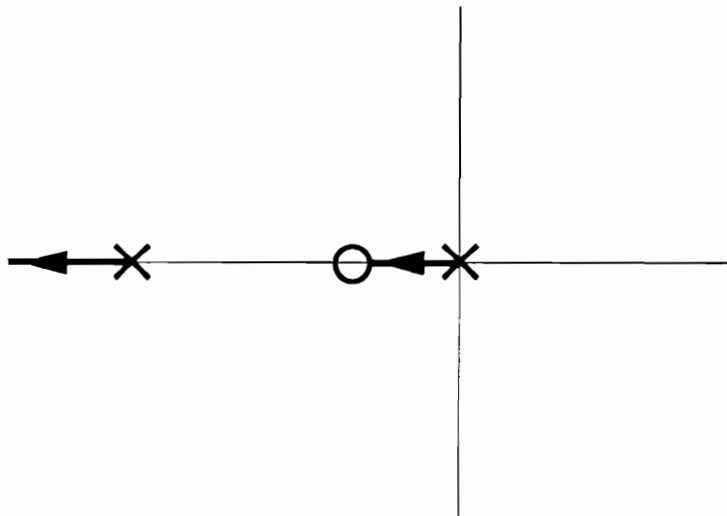
#### ***4.4 Summary***

When the system operates in the charge current regulation mode, the charger operates with a fixed duty cycle which is determined by the regulated bus voltage and the battery voltage. Since the bus voltage is a stiff voltage source, charger's input terminal dynamics, including the bus filter capacitor, are absorbed by the voltage source. Thus, the small-signal dynamics become the first order in both CCM and DCM. The charger in this mode is inherently open-loop unstable due to the stiff voltage sources at the both input and output terminals.

In CCM, the control-to-charge current transfer function has a pole at the origin, while it has a pole at high frequency in DCM. The control-to-charge transfer functions in CCM and DCM are not only first order but also their parameters are fixed. Thus it is not difficult to design the control-loop for operations in both CCM and DCM.



(a)



(b)

**Figure 4.8. Root Loci of Current Regulation Mode in DCM**  
(a) simple gain compensator  
(b) integrator plus zero compensator



In the compensator design, an integrator is necessary to reduce the switching ripple as well as the steady-state error in the charge current. In order to achieve proper phase margin, a zero is required.

# **Chapter 5**

## **Small-Signal Analysis of the Peak Power Tracking Converter**

### ***5.1 Introduction***

PPT systems use a series switching converter between the solar array and distribution bus. The series converter controls the solar array's operating point at the peak power point. The converter then regulates solar array voltage according to the reference voltage set by the tracker. The peak power tracker is activated only when the battery is not fully charged or the load demand is greater than the solar array output. When the peak power regulator is not in operation, the series

converter is used for a battery charge current controller. Since the converter dynamic is much faster than the tracker, only the converter dynamics are investigated here.

In this chapter, small-signal dynamic characteristics of battery charging subsystem of PPT systems in different modes of operation are analyzed to facilitate the design of the control-loop for optimum performance and stability.

The charge converter for the peak power tracking system operates either as a tracking converter or a current regulator. In Section 3.4, the converter's small-signal characteristics for both PPT mode and current regulation mode are derived. The differences in control-loop design between the PPT and the DET systems are described.

## ***5.2 Terminal Characteristics***

When the series regulator (buck converter) operates in peak power tracking mode, the solar array output voltage is regulated at its peak power point according to the reference voltage provided by the tracker. That is, the converter regulates its input voltage. It is similar to the bus-voltage regulation in DET charger

system. In the PPT system, however, as shown in Fig. 5.1, spacecraft payloads are directly connected to the battery. Thus the load dynamics do not affect the charger's control loop.

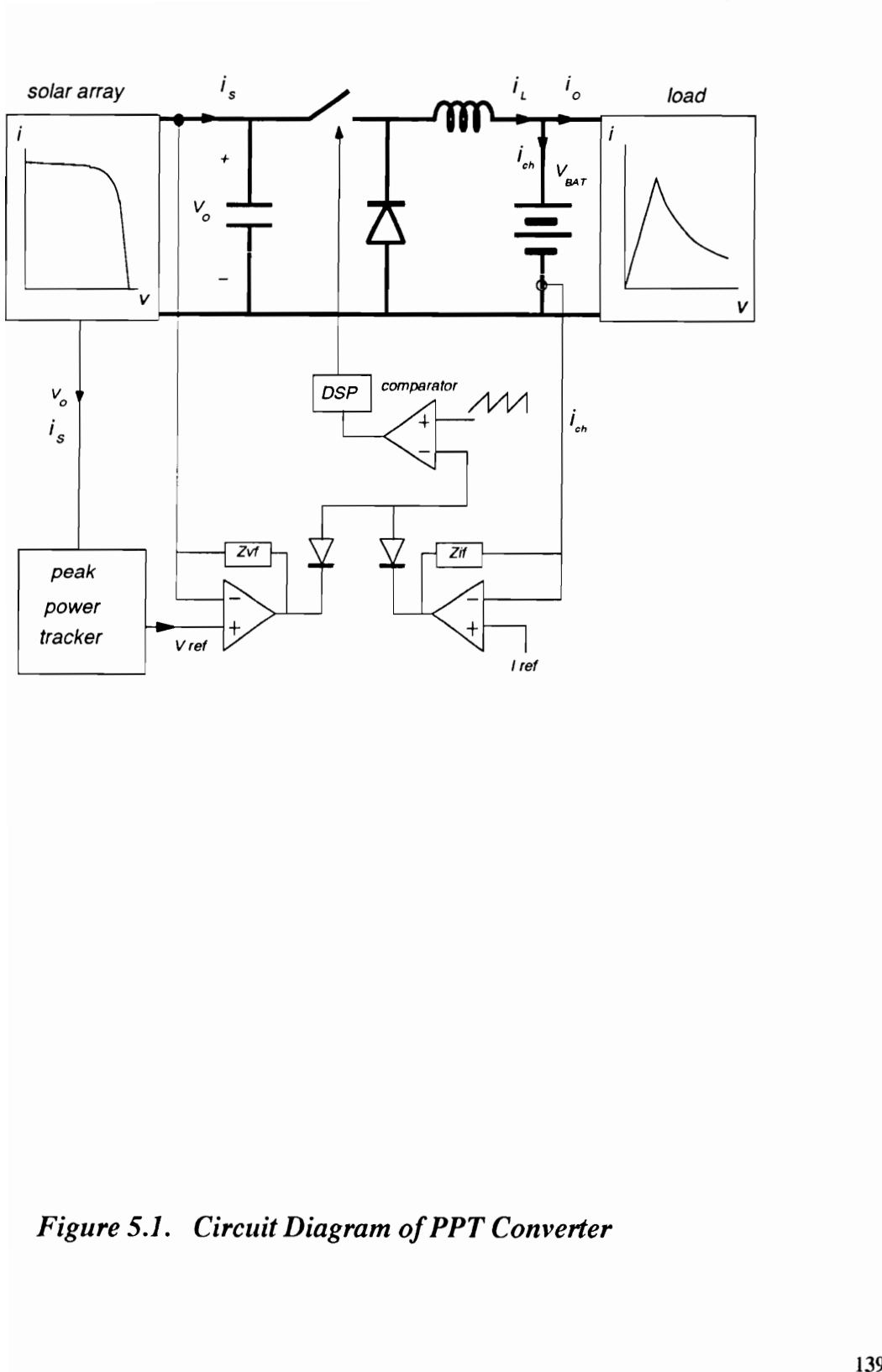
The dynamic impedance seen by the converter becomes the dynamic resistance of the solar array.

$$r_{eq} = -r_s \quad (5.1)$$

The negative sign comes from the direction of  $i_s$  defined in the Fig. 5.1. This is the same with the bus-voltage regulation of the DET system omitting  $r_o$ . Therefore,  $r_{eq}$  is positive in the PPT system. The dc resistance seen by the converter is defined by

$$R_{dc} \equiv \frac{V_o}{I_s} \quad (5.2)$$

When the regulator operates at the peak power point of the solar array,  $|R_{dc}| = |r_s|$ . Peak power tracking mode starts from the exit of the eclipse and continues until the battery is fully charged. When a fully charged condition is sensed, the system goes into the current regulation mode (trickle charge mode). During this mode the converter regulates the charge current into the battery. The solar array supplies the load current and the trickle charge current. As described in Chapter 2, the operating point of the solar array moves to the voltage source region in this mode, and  $|R_{dc}| > |r_s|$ . In DET system, the output voltage of the solar array becomes a stiff voltage source regulated by the shunt regulator during



**Figure 5.1. Circuit Diagram of PPT Converter**

the charge current regulation mode. In PPT system, however, output voltage of the solar array is determined by the load line seen by the solar array as shown in Fig. 2.16. The duty-ratio of the converter is determined by the ratio of the battery voltage to the solar array voltage.

### ***5.3 Small-Signal Analysis in Peak Power Tracking Mode***

The peak power tracker activates from no load (no solar array power) to full load (maximum solar array power). The converter thus operates in both DCM and CCM. Since the dc and small-signal dynamics for the two modes of operation are quite different, the analysis and feedback controller design must consider both CCM and DCM operations.

### 5.3.1 Continuous Conduction Mode

DC gains of the converter assuming lossless are given by

$$V_o = \frac{V_{BA}}{D} \quad (5.3)$$

$$I_L = \frac{I_s}{D} \quad (5.4)$$

Small-signal model is same as that of the DET system except the terminal equivalent load. The control-to-output voltage small-signal transfer function becomes:

$$F_{dv} = \frac{\hat{v}_o}{\hat{d}} = \frac{-\frac{V_{BA}}{D^2} \left(1 + s \frac{I_L L}{V_{BA}}\right) (1 + s R_c C)}{1 + s \left[ \left(\frac{R_l}{D^2} + R_c\right) C + \frac{L}{r_{eq} D^2} \right] + s^2 \frac{LC}{D^2}} \quad (5.5)$$

This transfer function is the same as the Eq. (3.12) of the DET system, omitting load related parameters,  $I_o$  and  $r_o$ . Since  $r_{eq}$  is positive,  $F_{dv}$  has complex LHP pole pair and negative dc gain. Compared with the DET case, the damping factor  $Q$  is increased since  $r_{eq}$  is positive. In the PPT converter, all of the power generated by the solar array passes through the converter, while a part of the power passes through the charge converter in the DET system. Thus the inductor current  $I_L$  of the converter is much larger than that of the DET charger. Therefore the moving zero in  $F_{dv}$  of the Eq. (5.5) can reside much lower frequency.

The control loop can be designed similar to the strategy used in the voltage-mode control of the DET charger system which was presented in Section 3.3. Since the  $F_{dv}$  has a negative dc gain, a positive feedback compensation gain is required to achieve overall negative feedback. Due to the LHP zero, it is not difficult to design a feedback loop compensator. The same type of the compensator of Eq. (3.17) used in the DET charger can be employed for optimum design.

### 5.3.2 Discontinuous Conduction Mode

DC equations are identical to the DET charger in Eqs. (3.18) - (3.23). The control-to-output voltage transfer function is also in the same form with the DET charger.

$$\frac{\hat{v}_o}{\hat{d}} \simeq G_d \frac{(1 + \frac{s}{\omega_z})(1 + sR_c C)}{(1 + \frac{s}{\omega_{p1}})(1 + \frac{s}{\omega_{p2}})} \quad (5.6)$$

where



$$\begin{aligned}
G_d &= - \frac{2V_O(1 - M)r_{eq}}{D\{R(1 - M) + r_{eq}\}} \\
\omega_z &= \frac{RM^2(1 - M)}{L(1 - M + 2M^2)} \\
\omega_{p1} &= \frac{RM^2\{R(1 - M) + r_{eq}\}}{r_{eq}(1 - M)(R^2CM^2 + L) + RL} \\
\omega_{p2} &= \frac{r_{eq}(1 - M)(R^2CM^2 + L) + RL}{RLC r_{eq}}
\end{aligned} \tag{5.7}$$

However, since  $r_{eq}$  is positive, the dc gain  $G_d$  is negative, and  $\omega_{p1}$  becomes a low frequency LHP pole. Thus the system is an open-loop stable system and does not have conditionally stable problem.

### 5.3.3 Control-Loop Design

Same strategies used in the loop-gain design in the voltage-mode control of the DET system are applied in the PPT system. As the illumination increases, the solar array current increases. The zero  $\omega_z$  moves toward lower frequency. This results in the higher loop-gain crossover frequency. Thus the integrator gain should be limited not to exceed the crossover frequency limit at the maximum

charge current. And at the minimum charge current in DCM, minimum stability margin should be satisfied.

However, as discussed in Chapter 3, when the voltage-mode control is used, it is difficult to achieve good performance for both CCM and DCM because of the low frequency pole and the smaller dc gain in DCM. Thus, it is preferable to operate only in CCM. In PPT system, this can be achieved simply by turning on the transistor switch of the converter continuously until the inductor current reaches the critical value which goes to CCM operation. The solar array operating point is fixed to the battery voltage. Once the inductor current exceeds the critical value, the peak power tracker is activated. By doing so, performance of the converter can be optimized within the CCM.

### Design Example

Solar array maximum power = 6570 W

Solar array current at maximum power = 43 A

Solar array voltage at maximum power = 153 V

Battery voltage  $V_{BA} = 65\text{--}85$  V

Load power = 1,800 W

The circuit parameters are

$L = 50 \mu\text{H}$ ,  $R_l = 50 \text{ m}\Omega$

$C = 2000 \mu\text{F}$ ,  $R_c = 50 \text{ m}\Omega$

Switching frequency = 90 kHz

The maximum loop-gain crossover frequency is set at 10 kHz and the worst case phase margin is set to 45 degree.

Solar array I-V curves under the different illumination level are generated using solar array dc model [28]. From the solar array data, range of the dc operating conditions are obtained.

peak power voltage = 148-153 V

duty ratio  $D = 0.44-0.56$

inductor current  $I_L = 3.3-76.8$  A

resonant frequency = 221-282 Hz

moving zero  $\omega_z = 2.7-59$  kHz

Loop gain of the two extreme cases is considered. At maximum inductor current, the crossover frequency should not exceed 10 kHz. At minimum current, 45 degree phase margin should be satisfied. The designed compensator is given by

$$H_v = \frac{2200}{s} \frac{(1 + \frac{s}{1,380})(1 + \frac{s}{11,300})}{(1 + \frac{s}{10,000})(1 + \frac{s}{62,800})}$$

The loop-gains and the output impedances of the converter in two extreme cases are shown in Figs. 5.2 - 5.5. Figures show the good performance in both extreme cases. At the maximum current, the loop-gain crossover frequency is 10 kHz. At the minimum current, the loop-gain bandwidth is reduced only a little, and the

phase margin is 45 degree. The bus impedances are low and their maximum values are the ESR of the output capacitors.

As the illumination changes, the peak power point also changes. Thus, it is necessary to define another performance parameter besides the audiosusceptibility and output impedance of the regulator. The regulator should behave well according to the continuously changing reference voltage. Dynamics of the regulator are modeled and analyzed as follows.

From the PPT converter circuit in Fig. 5.6(a),

$$\frac{v_o - v_{ref}}{Z_i} = \frac{v_{ref} - v_c}{Z_f} \quad (5.8)$$

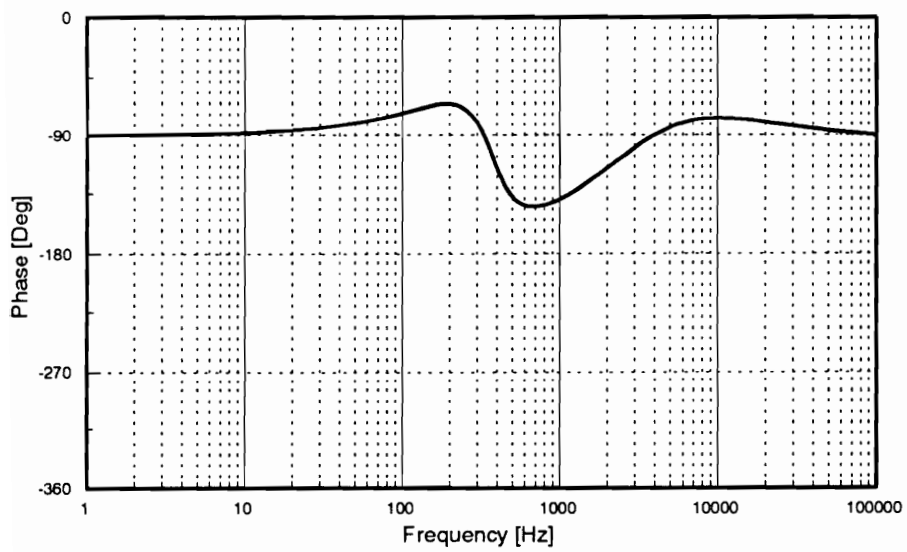
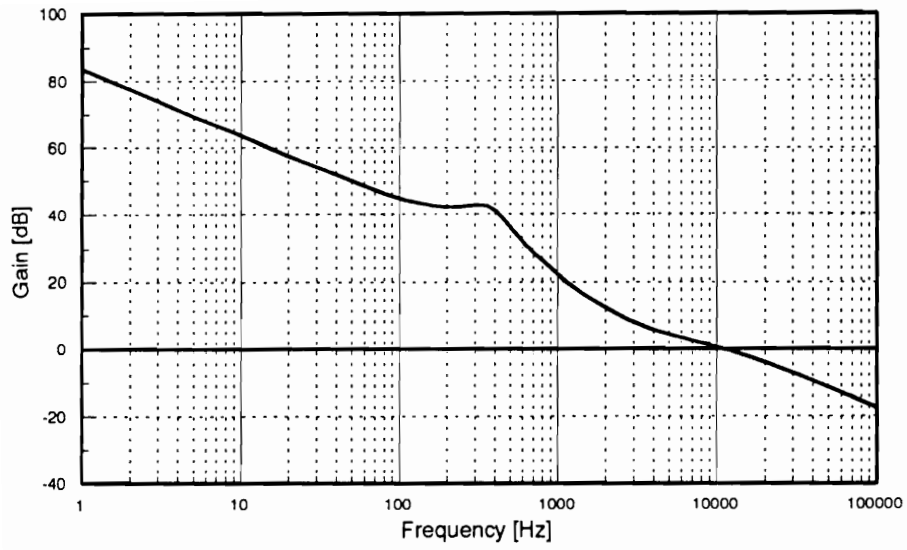
From Eq. (5.8), following transfer functions are obtained.

$$F_r \equiv \frac{\hat{v}_c}{\hat{v}_{ref}} = 1 + \frac{Z_f}{Z_i} \quad (5.9)$$

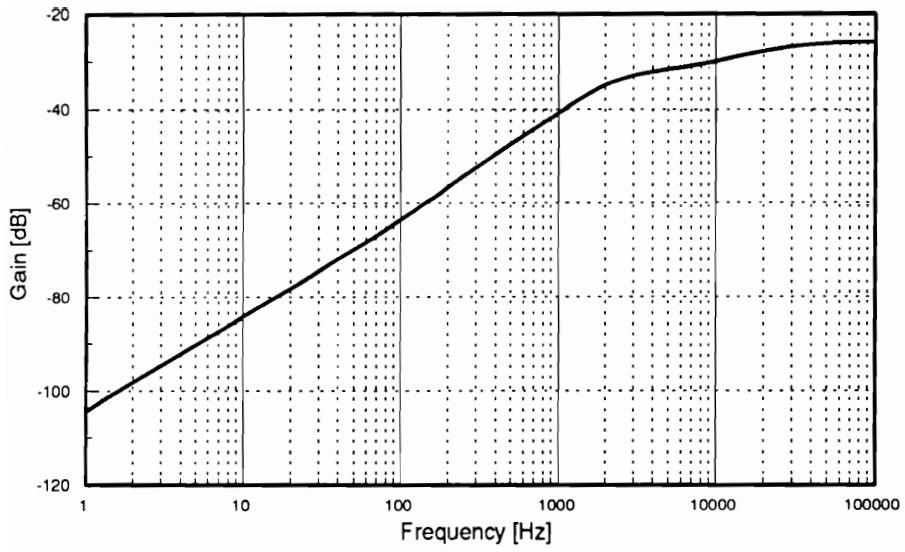
$$F_v \equiv \frac{\hat{v}_o}{\hat{v}_c} = - \frac{Z_f}{Z_i} \quad (5.10)$$

Then, from the small-signal block diagram in Fig. 5.6(b), the open-loop  $\hat{v}_{ref}$  to the solar array output voltage transfer function is

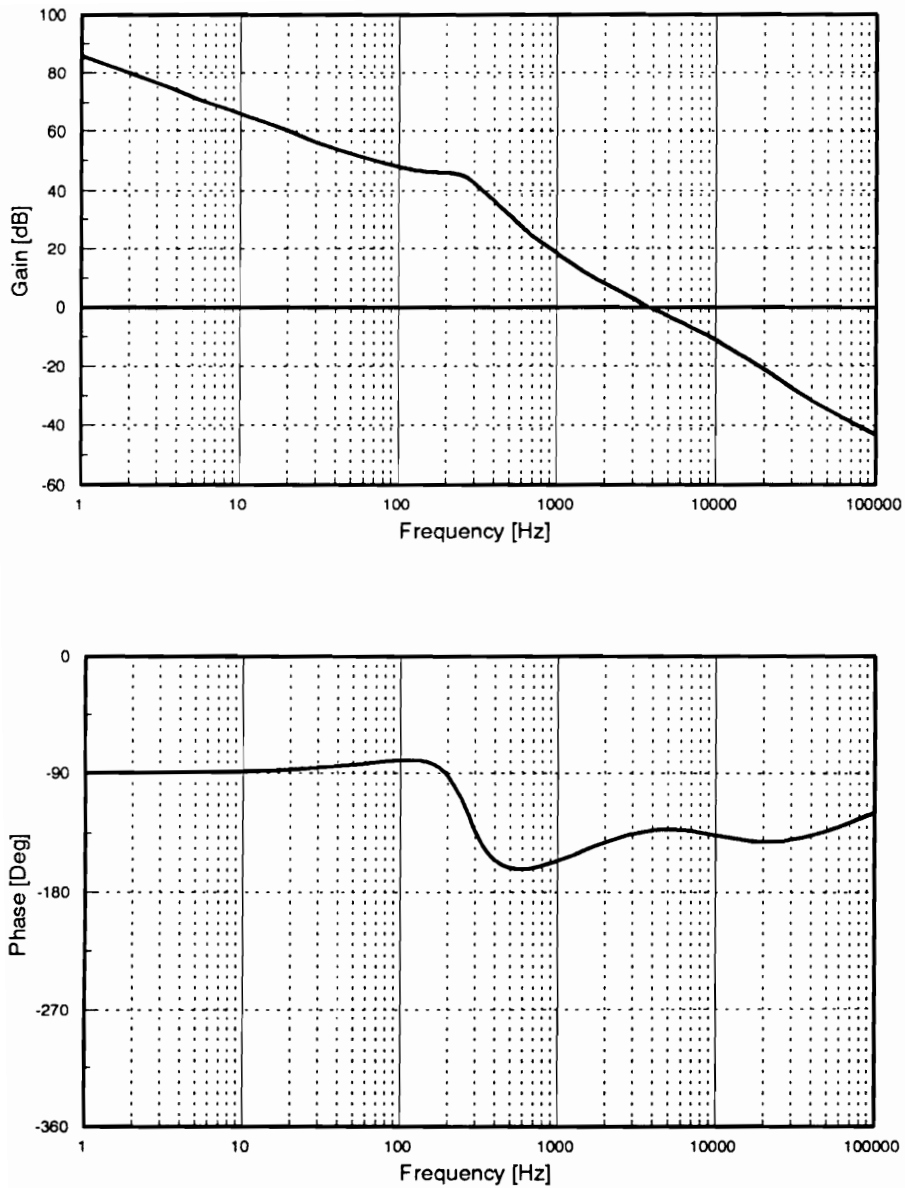
$$\frac{\hat{v}_o}{\hat{v}_{ref}} = F_r F_m G_d \quad (5.11)$$



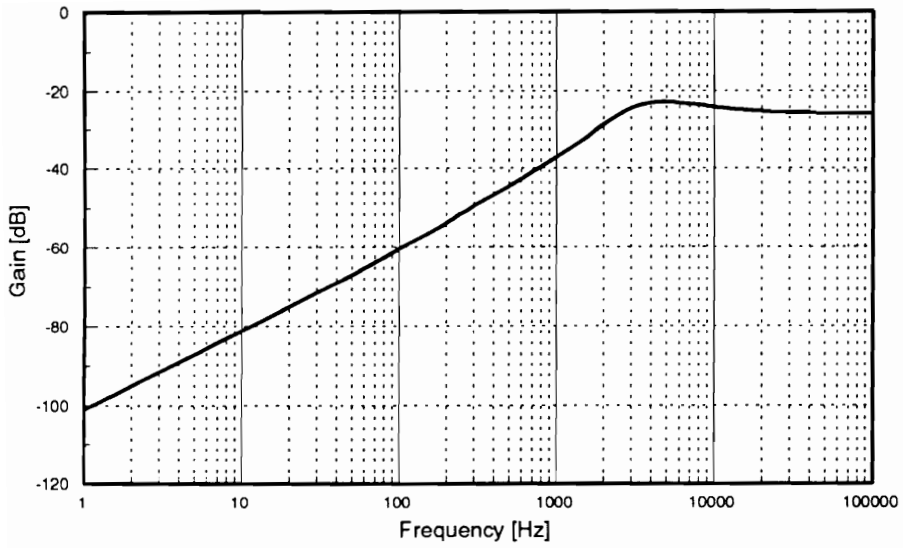
**Figure 5.2. Loop Gain of the PPT Converter at Maximum Current**



**Figure 5.3.** *Output Impedance of the PPT Converter at Maximum Current*

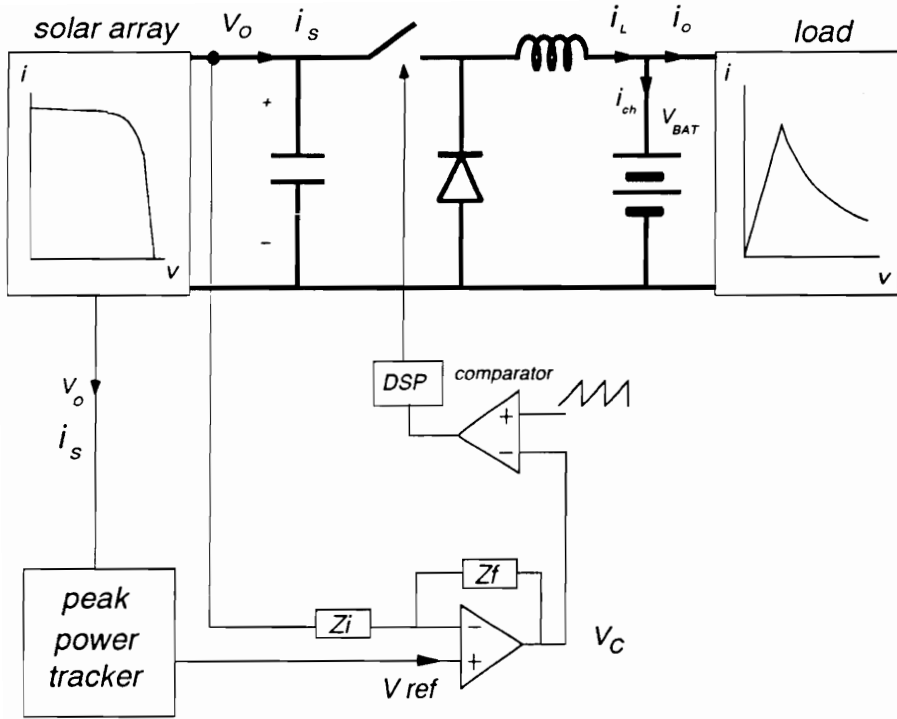


**Figure 5.4. Loop Gain of the PPT Converter at Minimum Current**

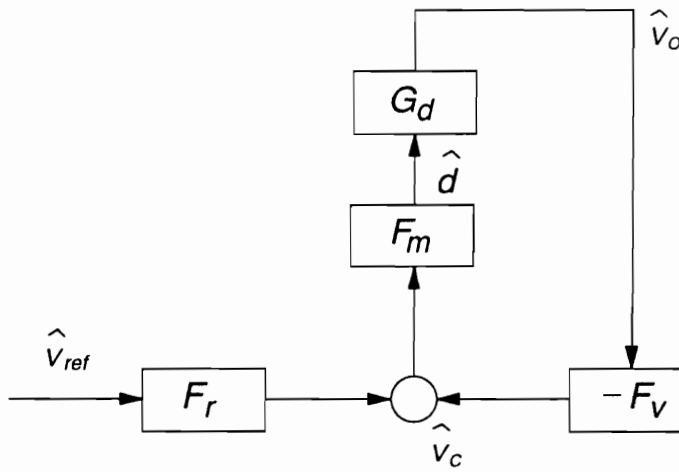


**Figure 5.5.** *Output Impedance of the PPT Converter at Minimum Current*





(a)



(b)

**Figure 5.6. PPT Converter in PPT Mode**

(a) Circuit Diagram

(b) Small-Signal Block Diagram

The closed-loop transfer function is given by

$$\frac{\hat{v}_o}{\hat{v}_{ref}} \Big|_{CL} = \frac{F_r F_m G_d}{1 + F_m G_d F_v} \quad (5.12)$$

At low frequency, it can be approximated by

$$\frac{\hat{v}_o}{\hat{v}_{ref}} \simeq \frac{F_r}{F_v} = \frac{1 + \frac{Z_f}{Z_i}}{\frac{Z_f}{Z_i}} = 1 + \frac{Z_i}{Z_f} \quad (5.13)$$

Figure 5.7 shows the transfer functions of Eq. (5.9) through (5.12). The closed-loop transfer function remains at 0 dB until the loop-gain crossover frequency, and it follows the open-loop transfer function beyond the crossover frequency. Thus, it is required that the frequency of the reference change should not exceed the crossover frequency. As long as the frequency of the reference change maintains below the crossover frequency, the steady-state error does not exist.

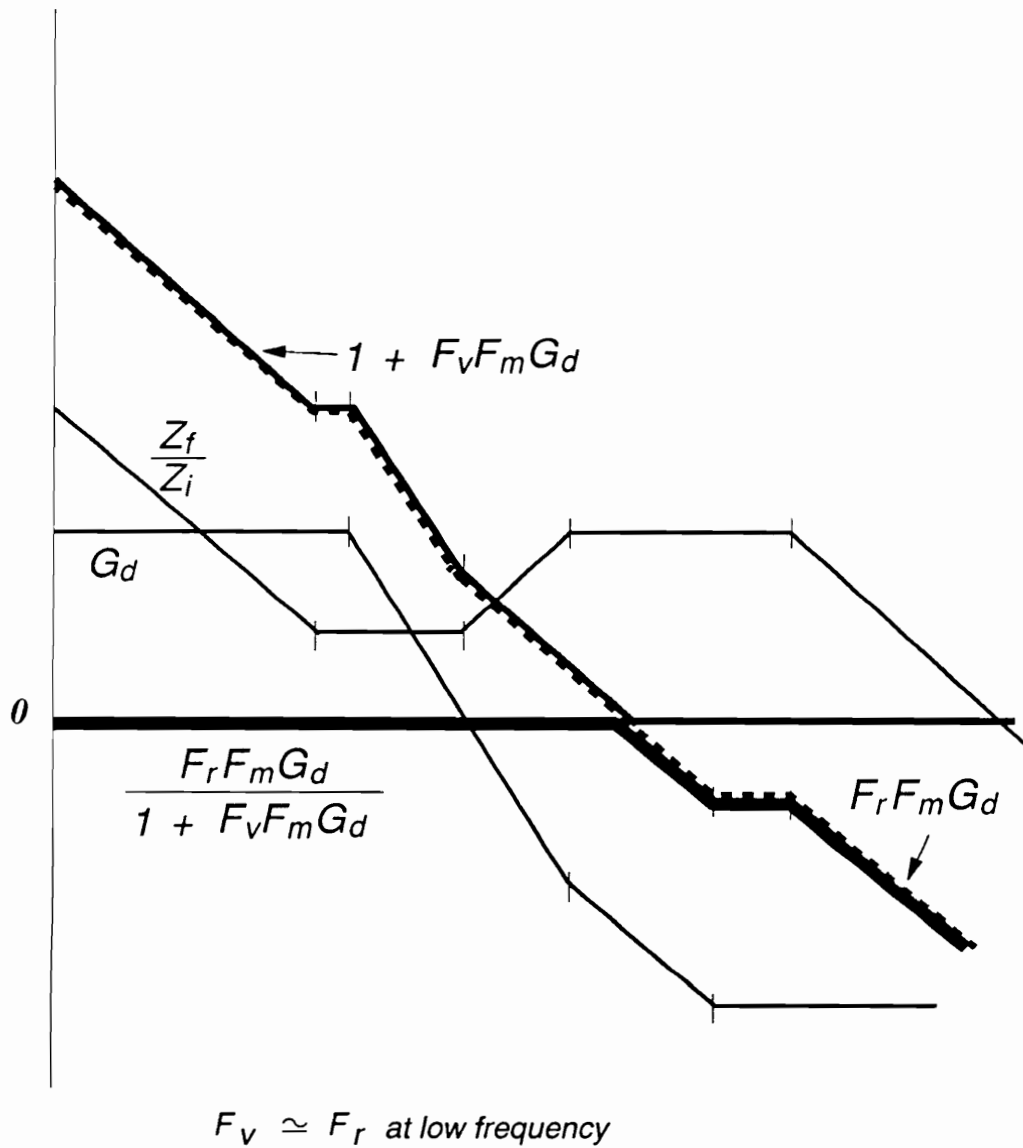


Figure 5.7. Reference Change to Output Transfer Function

## 5.4 Current Regulation Mode

When the peak power tracker is not in force, the converter is used as a trickle charge current regulator. In DET system, since the shunt regulator regulates the bus voltage, the input voltage of the converter could be considered as ideal source. In PPT system however input of the converter is the output voltage of the solar array. In Chapter 2, it was shown that the operating point of the solar array resided in the voltage source region in the current regulation mode of the PPT system. Thus dynamic behavior of the converter in current regulation mode is similar to that of the DET system except that bus filter capacitor comes into the dynamic. According to the current level of the trickle charge, it can operate either in CCM or DCM.

### 5.4.1 Continuous Conduction Mode

The control-to-charge current transfer function is given by

$$F_{di} = \frac{\hat{i}_L}{\hat{d}} = \frac{-\frac{V_{BA} + Dr_s I_s}{D^3 r_s} (1 + s/w_z)}{1 + s[(\frac{R_l}{D^2} + R_c)C - \frac{L}{r_s D^2}] + s^2 \frac{LC}{D^2}} \quad (5.14)$$

where

$$w_z = -\frac{V_{BA} + Dr_s I_s}{r_s V_{BA} C}$$

In Eq. (5.8), the dc gain and the location of zero are functions of a dc operating point of the solar array I-V curve, and they have common term  $V_{BA} + Dr_s I_s$ .

$$\begin{aligned} V_{BA} + Dr_s I_s &= V_{BA} + \frac{V_{BA}}{V_o} I_s r_s \\ &= V_{BA} \left( 1 + \frac{r_s}{R_s} \right) \end{aligned} \quad (5.15)$$

Since the operating point should be in the voltage source region during current regulation mode, from the relation between the dynamic resistance and dc resistance of Eq. (3.5), Eq. (5.15) becomes positive. The dc gain therefore becomes positive, and the zero is located in the LHP.

In the practical design, since the  $R_s \gg |r_s|$ , the zero  $\omega_z$  in Eq. (5.14) can be simplified by.

$$w_z = -\frac{V_{BA} + Dr_s I_s}{r_s V_{BA} C} \simeq -\frac{1}{r_s C} \quad (5.16)$$

Also dc gain  $G_i$  is simplified by

$$G_i = -\frac{V_{BA} + Dr_s I_s}{D^3 r_s} \simeq \frac{V_{BA}}{D^3 r_s} \quad (5.17)$$

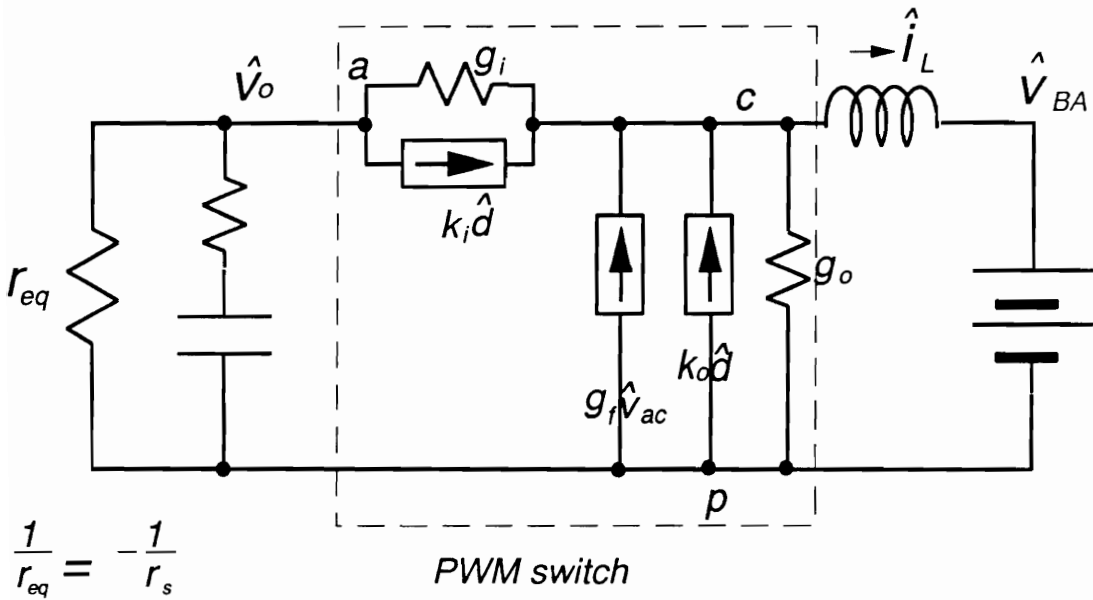
## 5.4.2 Discontinuous Conduction Mode

DC equations are identical to the results of the current regulation mode of the DET system. In the small-signal model, since  $\hat{v}_{Bus}$  is not zero, capacitor C should be included as shown in Fig. 5.8. This small-signal model in Fig. 5.8 is the same with the DCM small-signal model of bus voltage regulation mode of the DET system except that the equivalent dynamic resistance  $r_{eq}$  is changed from  $r_o \parallel (-r_s)$  to  $-r_s$ . The control-to-inductor current transfer function is derived from the Eqs. (3.24)-(3.25).

$$\frac{\hat{i}_L}{\hat{d}} \simeq G_i \frac{(1 + \frac{s}{\omega_z})}{(1 + \frac{s}{\omega_{p1}})(1 + \frac{s}{\omega_{p2}})} \quad (5.18)$$

where

$$\begin{aligned} G_i &= \frac{2I_s(1 - M)(R - r_{eq})}{DM\{R(1 - M) + r_{eq}\}} \\ \omega_z &= \frac{R - r_{eq}}{Rr_{eq}C} \\ \omega_{p1} &= \frac{RM^2\{R(1 - M) + r_{eq}\}}{r_{eq}(1 - M)(R^2CM^2 + L) + RL} \\ \omega_{p2} &= \frac{r_{eq}(1 - M)(R^2CM^2 + L) + RL}{RLCr_{eq}} \end{aligned} \quad (5.19)$$



**Figure 5.8. Small-Signal DCM Model of PPT Converter in Current Regulation Mode**

In practical case, since  $R \gg r_{eq}$ , the dc gain,  $G_i$ , becomes positive, and  $\omega_z$  becomes LHP zero.

### 5.4.3 Control-Loop Design

In CCM case, the control-to-current transfer function has a LHP complex pole pair and a zero. In the DCM, the complex pole pair of the CCM are split to a low frequency pole and a high frequency pole, and the zero is the same with the CCM case. Thus, for both CCM and DCM cases, a compensator with an integrator and a zero can be used.

In the current-regulation mode of the DET system, the current reference changes from the maximum value (current limit) to the minimum value (trickle charge). In the PPT system, however, the regulation of the charge current is required only in the trickle charge mode. It makes the control-loop design easier.



## 5.5 Summary

In the PPT mode, the dynamic impedance  $r_{eq}$  seen by the converter is the dynamic resistance of the solar array output, and it is positive. Since  $r_{eq}$  is positive, the system is open-loop stable and does not have the conditionally stable problem. The other small-signal characteristics are similar to those of the bus voltage regulation mode of the DET system. When the PPT converter employs the voltage-mode control, the performance in DCM could be poor as in the DET system. In the PPT system, however, the converter's operating range can be limited only in CCM to obtain good dynamic performance. This is achieved by turning on the transistor switch of the converter continuously until the inductor current reaches the critical value where the CCM starts. By doing so, the performance of the converter can be optimized within CCM.

Since the PPT converter regulates the output voltage of the solar array by the change of the reference voltage, the regulator should behave well for the continuous change of the reference. The closed-loop reference change-to-output voltage transfer function drops from 0 dB after the loop-gain crossover frequency. Thus, the frequency of the reference change is limited by the crossover frequency.

In the PPT system operating in the current regulation mode, the input voltage of the converter is the solar array output voltage. During this mode, the operating point of the solar array is in the voltage source region. Unlike in the DET system,

the input voltage is not a regulated stiff voltage source. Thus, the capacitor connected between the solar array output and the charger should be included in the regulator's model. The capacitor dynamics and the different terminal impedance characteristics in the PPT system make the design of the control-loop quite different from that in the DET system.

# Chapter 6

## Conclusions

The principal objective of this dissertation is the analysis of the dynamic behavior of the spacecraft power processing system that facilitates the design of the power conditioning equipment. The large-signal dynamics of the power conditioning equipment through an orbit period are analyzed employing qualitative graphical method. The use of stability information on each equilibrium point and the separatrix clearly characterize the large-signal behavior of the system. It was revealed that the trajectory of the system's operating point during the transition from the sunlight to eclipse mode is different than that of the transition from the eclipse to sunlight mode.

In the DET system, bus regulation voltage is set at the current source region of the solar array which is the unstable operating region without the power conditioning equipment. The system is stabilized in this region when a power conditioning regulator is employed. The regulator's transconductance can be treated as part of either the source or the load. The equivalent source characteristic seen by the constant power load and the equivalent load characteristic seen by the solar array output are characterized. With the regulators, the system can be viewed as a stiff voltage source with a constant power load or as a solar array current source with a stiff current sink load. In the PPT system, graphical analysis illustrates that after the peak power tracker is deactivated, the solar array's operating point moves into the stable equilibrium point in the voltage source region.

Small-signal characteristics of the spacecraft battery charger systems in various modes of operation are derived and analyzed. And their control-loop design guidelines are presented.

When the charger operates in the bus voltage regulation mode, the equivalent load impedance is negative. Switching regulator in the battery charger system operates in the unique mode such that the input voltage is regulated. Even though a buck topology is used for the charger, its dynamic behavior is much like the boost converter except that the power flows in the reverse direction.

When the voltage-mode control is employed, the control-to-output voltage transfer function in CCM has a negative dc gain, two LHP zeroes and a complex pole pair. For regulation of the bus voltage, a positive compensator gain should be used to achieve overall negative feedback action. In DCM, the control-to-output transfer function has a positive dc gain and a low frequency RHP pole resulting in a nonminimum phase system. Even though it has a positive dc gain, a positive compensation gain is required. Thus, the same compensator used in CCM can be employed.

When the current-mode control is used, the control-to-output transfer function with the current-loop closed has a positive dc gain, a low frequency RHP pole and a high frequency complex pole pair in CCM. The control-to-output transfer function in DCM is approximately same with that of the voltage-mode control in DCM. A positive compensation gain is required to regulate the bus voltage in both CCM and DCM.

Since the charger operates both in CCM and DCM, the control loop should be designed for both modes. When voltage-mode control is used, it is difficult to achieve good performance in both modes. On the contrary, the current-mode control gives superior performance operated in both CCM and DCM.

In the bus voltage regulation mode, charger systems are unstable under open-loop condition and conditionally stable when the feedback loop is closed. However, as long as the gain margin is sufficient, it does not have any detrimental effects.

When the system operates in the charge current regulation mode, the charger operates with a fixed duty cycle which is determined by the regulated bus voltage and the battery voltage. Since the bus voltage is a stiff voltage source, charger's input terminal dynamics, including the bus filter capacitor, are absorbed by the voltage source. Thus, the small-signal dynamics become the first order in both CCM and DCM. The charger in this mode is inherently open-loop unstable due to the stiff voltage sources at the both input and output terminals.

When the peak power tracking converter operates in the PPT mode, the dynamic impedance  $r_{eq}$  seen by the converter is the dynamic resistance of the solar array output, and it is positive. Since  $r_{eq}$  is positive, the system is open-loop stable and does not have the conditionally stable problem. The other small-signal characteristics are similar to those of the bus voltage regulation mode of the DET system.

Since the PPT converter regulates the output voltage of the solar array by the change of the reference voltage, the regulator should behave well for the continuous change of the reference. The closed-loop reference change-to-output voltage transfer function drops from 0 dB after the loop-gain crossover frequency. Thus, the frequency of the reference change is limited by the crossover frequency.

In the PPT system operating in the current regulation mode, the input voltage of the converter is the solar array output voltage. During this mode, the operating point of the solar array is in the voltage source region. Unlike in the DET system,

the input voltage is not a regulated stiff voltage source. Thus, the capacitor connected between the solar array output and the charger should be included in the regulator's model.

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# Appendix A

## EASY5 Macro Models

EASY5 component macro models used in this dissertation are provided.

- SI** solar array large-signal model
- SS** solar array small-signal model
- CH** power stage of the charger large-signal model
- CS** power stage of the charger small-signal model (state-space averaging)
- SW** power stage of the charger in CCM small-signal model (PWM switch)
- DM** power stage of the charger in DCM small-signal model (PWM switch)
- BF** bus filter capacitor
- PP** compensator (three poles and two zeros)
- PZ** compensator (two poles and two zeros)
- MP** compensator (two poles and one zero)
- CC** current feedback loop

- BA** battery model
- WM** PWM model large-signal
- PW** PWM model small-signal
- FM** PWM model small-signal for new current-mode control model
- PT** constant power load large-signal model
- SL** constant power load small-signal model
- PK** peak power tracker

## Solar Array (large-signal model)



### INPUTS

QUANTITY NAME	DESCRIPTION	UNITS
VX	voltage from bus capacitor	volts
LL	initial illumination level	
LLS	slope of the illumination change	
NP	number of parallel cells	
NP	number of serial cells	
IOI	initial guess for solar array current	amps

### OUTPUTS

QUANTITY NAME	DESCRIPTION	UNITS
IO	output current	amps
PO	output power	watts
FIL	illumination level	
SR	dc resistance	ohms
DR	dynamic resistance	ohms

```

MACRO FILE NAME = MACROS
DEFINE MACRO = SI
*****
** SOLAR ARRAY MODEL(CURRENT SOURCE) REVISED ON 10/22/89*****
*****

* = = = = = > IO

* = = = = = < VX

MACRO INPUTS = VX  LL  LLS  LS2
  TIL  LLM  LLX
  NP  NS  IOI
* IX = INPUT CURRENT
* LL = INITIAL ILLUMINATION LEVEL
* LLS, LS2 = SLOPE OF ILLUMINATION CHANGE
* TIL = TIME WHEN LLS CHANGES TO LS2
* LLM = MIN. VALUE OF ILLUMINATION LEVEL
* R,L,C, : CABLE IMPEDANCE
* NP = NO. OF PSIALLEL SIRAYS
* NS = NO. OF SERIAL CELLS
* IOI = INITIAL GUESS FOR CURRENT OUTPUT

MACRO OUTPUTS = IO  FIL
  PO  DUM  SDR
  IPR  SR  DR

* IO = SOLAR ARRAY OUTPUT CURRENT
* FIL = ILLUMINATION LEVEL ( 1 = FULL SUN )

MACRO CODE
MACRO STOP SORT
*** SOLAR CELL PARAMETERS ****
* RS = INTERNAL SERIES RESISTANCE
* RSH = INTERNAL SHUNT RESISTANCE
* XI0 = REVERSE SATURATION CURRENT
* TN = NOMINAL TEMPERATURE
* Q = ELECTRON CHSIGE
* XK = BOLTZMANN CONSTANT
* XIG = LIGHT-GENERATED CURRENT
* VOC = OPEN CIRCUIT VOLTAGE
  RS = .42
  RSH = 250.
  XIG = .14115
  XI0 = 4.1869E-11
  A = .969
  TN = 301.
  Q = 1.602E-19
  XK = 1.381E-23
  VOC = .5512
*  XKO = Q / ( XK * A * TN )
  XKO = 39.8
* ILLUMINATION CHANGE WITH LINESI SLOPE OF LLS,LS2
  IF ( TIME .GT. TILSI-- ) THEN
    FILSI-- = LLMSI-- + LS2SI-- * (TIME- TILSI--)
    IF ( FILSI-- .LE. LLMSI-- ) FILSI-- = LLMSI--

```

```

    IF ( FILSI-- .GE. 1.1 ) FILSI-- = 1.1
ELSE
    FILSI-- = LL SI-- + LLSSI-- * TIME
    IF ( FILSI-- .LE. LLMSI-- ) FILSI-- = LLMSI--
    IF ( FILSI-- .GE. LLXSI-- ) FILSI-- = LLXSI--
ENDIF
*****
* EFFECT OF ILLUMINATION CHANGE
  XIG = XIG * FILSI--
*
  C1 = ( 1. + RS / RSH )
  C2 = NP SI-- / ( NS SI-- * RSH )
  C3 = -NP SI-- * XIG
  A1 = XKO / NS SI--
  A2 = XKO * RS / NP SI--
*****
  IPRSI-- = IO SI--
  IF ( TIME .NE. 0. ) GOTO + + + 10
*
* INITIAL GUESS FOR SOLAR ARRAY OUTPUT VOLTAGE
  IO SI-- = IOISI--
*****
*** NEWTON ITERATION *****
*****
+ + + 10 CONTINUE
  XIOP = IO SI--
  FI = C1 * IO SI-- + C2 * VX SI-- + C3 + NP SI--
  & * XI0 * DEXP ( A1 * VX SI-- + A2 * IO SI-- )
  DFI = C1 + XKO * XI0 * RS * DEXP ( A1 * VX SI--
  & + A2 * IO SI-- )
  IO SI-- = IO SI-- - FI / DFI
  ZZ = ( IO SI-- - XIOP ) / IO SI--
  IF ( DABS ( ZZ ) .LE. 1.E-4 ) GOTO + + + 20
  GO TO + + + 10
*****
+ + + 20 CONTINUE
  PO SI-- = VX SI-- * IO SI--
  SR SI-- = VX SI-- / IO SI--
  DR SI-- = DABS(TINC/(IO SI-- - IPRSI--))
  VD = VX SI-- / NS SI-- + RS * IO SI-- / NP SI--
  SDRSI-- = 1. / ( NP SI-- * ( XI0 * XKO * DEXP ( XKO * VD ) - 1. / RSH ) )
MACRO DERIVATIVES, DUMSI-- = 1
MACRO RESUME SORT
END OF MACRO
*****
MODEL DESCRIPTION
LOCATION = 22, SI
END OF MODEL

```



## Solar Array (small-signal model)



### INPUTS

QUANTITY NAME	DESCRIPTION	UNITS
VO	voltage from bus capacitor	volts
CD	diffusion capacitance of one cell	farads
CT	transition capacitance of one cell	farads
RD	dynamic resistance	ohms
RS, RSH	parasitic resistances	ohms
NP	number of parallel cells	
NP	number of serial cells	

### OUTPUTS

QUANTITY NAME	DESCRIPTION	UNITS
IO	output current	amps
VC	internal capacitor voltage	volts



## Charger Power Stage (large-signal model)



### INPUTS

QUANTITY NAME	DESCRIPTION	UNITS
V1	input voltage	volts
I2	output current	amps
IQ	switching function from PWM	
TS	switching period	sec
L	inductance	henries

### OUTPUTS

QUANTITY NAME	DESCRIPTION	UNITS
IL	charge current	amps
I1	input current	amps

```

*****
** LARGE SIGNAL MODEL OF BUCK CHARGER
* 3/9/90
*****
MACRO FILE NAME = MACROS
DEFINE MACRO = CH
MACRO INPUTS =
    V1 L RL
    IQ VBA
* IQ ; SWITCHING FUNCTION
* IQ = 1 (SWITCH;ON)
* IQ = 0 (SWITCH;OFF)
* VBA ; INPUT VTG(FROM BATTERY LOAD)
MACRO OUTPUTS =
    IL I1
* IL ; INDUCTOR CURRENT(STATE)
* I1 ; SWITCH CURRENT
* VL ; TRANSFORMER VOLTAGE
MACRO CODE
MACRO STOP SORT
****
    IF(DABS(IQ CH--).LT.1.E-3)THEN
* SWITCH OFF
        IF(IL CH--.LE.0.)THEN
MACRO DERIVATIVE, IL CH-- = 0.
            I1 CH-- = 0.
        ELSE
**** SWTCH OFF & IL > 0
MACRO DERIVATIVE, IL CH-- = (-VBACH-- -IL CH--*RL CH--)/L CH--
*
            I1 CH-- = 0
            END IF
        ELSE
**** SWITCH ON ***
            I1 CH-- = IL CH--
MACRO DERIVATIVE, IL CH-- = ( V1 CH-- -VBACH-- -
*
            IL CH--*RL CH--)/L CH--

        END IF
*
        IF(IL CH--.LE.0.)IL CH-- = 0.
MACRO RESUME SORT
END OF MACRO
MODEL DESCRIPTION
LOCATION = 22, CH
END OF MODEL

```

## Charger Power Stage (small-signal model)



### INPUTS

QUANTITY NAME	DESCRIPTION	UNITS
V1	input voltage	volts
DH	duty cycle	
V2	output voltage	volts
VBS	bus voltage (dc)	volts
VBA	battery Voltage (dc)	volts
ILS	charge current (dc)	amps
L	inductance	henries

### OUTPUTS

QUANTITY NAME	DESCRIPTION	UNITS
IL	charge current	amps
I1	input current	amps

```

*****
* CHARGER POWER STAGE SMALL SIGNAL
**   using state-space averaging
* REVISED 3/14/90
MACRO FILE NAME = MACROS
DEFINE MACRO = CS
MACRO INPUTS = DH  V1  V2
          L  RL
          VBA  VBS  ILS
MACRO OUTPUTS = IL  I1  D
MACRO CODE
MACRO STOP SORT
*
  D CS-- = (VBACS-- + RL CS-- * ILSCS--)/VBSCS--
**** STATE EQUATIONS ****
MACRO DERIVATIVE, IL CS-- = ( D CS-- * V1 CS--
&          - V2 CS-- + VBSCS-- * DH CS-- - RL CS-- * IL CS--
&          )/L CS--
*****
  I1 CS-- = D CS-- * IL CS-- + ILSCS-- * DH CS--
*****
MACRO RESUME SORT
END OF MACRO
MODEL DESCRIPTION
LOCATION = 22,CS
END OF MODEL

```

## Charger Power Stage (small-signal model with PWM switch)



### INPUTS

QUANTITY NAME	DESCRIPTION	UNITS
V1	input voltage	volts
DH	duty cycle	
V2	output voltage	volts
VBS	bus voltage (dc)	volts
VBA	battery Voltage (dc)	volts
ILS	charge current (dc)	amps
L	inductance	henries

### OUTPUTS

QUANTITY NAME	DESCRIPTION	UNITS
IL	charge current	amps
Ii	input current	amps

```

*****
* CHARGER POWER STAGE SMALL SIGNAL
* using PWM switch model
* REVISED 2/11/91
DEFINE MACRO=SW
MACRO INPUTS= V1 V2 DH
L RL RE
VBA VBS ILS
MACRO OUTPUTS=IL I1 D DP
VD VCP
MACRO CODE
MACRO STOP SORT
*
D SW-- =(VBASW-- +RL SW--*ILSSW--)/VBSSW--
DP SW-- = 1.- D SW--
VD SW-- = VBSSW-- + ILSSW-- *(D SW-- -
& DP SW--) * RE SW--
**
I1 SW-- = D SW-- * IL SW-- + ILSSW-- * DH SW--
VCPSW-- = D SW-- * V1 SW-- - RE SW-- * D SW-- * DP SW-- * IL SW--
& + VD SW-- * DH SW--
**** STATE EQUATIONS*****
MACRO DERIVATIVE,IL SW-- =( VCPSW-- - V2 SW-- -IL SW--*RL SW--)/L SW--
*****
MACRO RESUME SORT
END OF MACRO
MODEL DESCRIPTION
LOCATION = 22,SW
END OF MODEL

```



## Charger Power Stage (DCM model with PWM switch)



### INPUTS

QUANTITY NAME	DESCRIPTION	UNITS
V1	input voltage	volts
DH	duty cycle	
V2	output voltage	volts
VBS	bus voltage (dc)	volts
VBA	battery Voltage (dc)	volts
ILS	charge current (dc)	amps
L	inductance	henries

### OUTPUTS

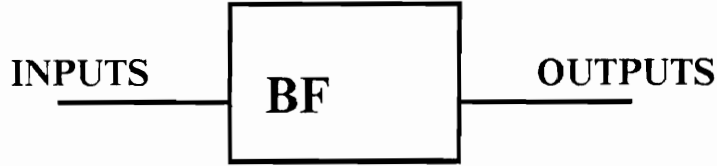
QUANTITY NAME	DESCRIPTION	UNITS
IL	charge current	amps
I1	input current	amps

```

*****
* CHARGER POWER STAGE SMALL SIGNAL
* DCM
* using PWM SWITCH model
* REVISED 12/16/90
DEFINE MACRO=DM
MACRO INPUTS= V1 V2 DH
      L      RL
      VBS IIS VBA DS
MACRO OUTPUTS=IL I1 M
      VAC VCP R
      GO GI GF
      KI KO
MACRO CODE
MACRO STOP SORT
*
      M DM-- = VBADM-- /VBSDM--
      R DM-- = VBSDM-- /IISDM--
**
      GI DM-- = 1./(R DM--*(1.-M DM--))
      GO DM-- = (1.-M DM--)/(R DM--*M DM--**2)
      GF DM-- = 2./(R DM--*M DM--)
      KI DM-- = 2.*IISDM--/DS DM--
      KO DM-- = 2.*IISDM--*(1.-M DM--)/(DS DM--*M DM--)
*****
      VCPDM-- = (1./(GO DM-- + GI DM-- + GF DM--))*
&      ((GI DM-- + GF DM--)*
&      V1 DM-- + (KI DM-- + KO DM--)*DH DM-- -IL DM--)
      VACDM-- = V1 DM-- - VCPDM--
      I1 DM-- = VACDM--*GI DM-- + KI DM--*DH DM--
**** STATE EQUATIONS*****
MACRO DERIVATIVE,IL DM-- = ((1./(GO DM-- + GI DM-- + GF DM--))*
&      ((GI DM-- + GF DM--)*
&      V1 DM-- + (KI DM-- + KO DM--)*DH DM--
&      -IL DM--)-IL DM--*RL DM--V2 DM--)/L DM--
*****
MACRO RESUME SORT
END OF MACRO
MODEL DESCRIPTION
LOCATION = 22,DM
END OF MODEL

```

## Bus Filter Capacitor



### INPUTS

QUANTITY NAME	DESCRIPTION	UNITS
I1	input current from solar array and load	amps
I2	output current from power stage	amps
RC	ESR of capacitor	ohms
CB	bus capacitance	farads
C	dummy capacitance	farads

### OUTPUTS

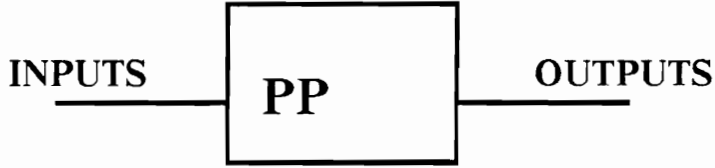
QUANTITY NAME	DESCRIPTION	UNITS
VB	bus voltage	volts
VC	dummy capacitor voltage	volts

```

MACRO FILE NAME = MACROS
* BUS FILTER CAPACITOR
*-----
DEFINE MACRO = BF
MACRO INPUTS
  I1  I2
  C   CB   RC
MACRO OUTPUTS
  VB  VC
MACRO CODE
MACRO STOP SORT
MACRO DERIVATIVE,VB BF-- = (I1 BF-- -(VB BF-- - VC BF--)/RC BF--
*                          - I2 BF-- )/CB BF--
MACRO DERIVATIVE,VC BF-- = (VB BF--VC BF--)/RC BF--/C BF--
*
MACRO RESUME SORT
END OF MACRO
MODEL DESCRIPTION
LOCATION = 44,BF
END OF MODEL
PRINT

```

**Compensator (3 poles, 2 zeroes)**



**INPUTS**

QUANTITY NAME	DESCRIPTION	UNITS
VO	power stage output voltage	volts
ER	reference voltage	volts
ER2	reference vtg after TC	volts
WZ1,WZ2	zero frequencies	rad/sec
WP	pole frequency	rad/sec
TC	time for ref vtg change	sec

**OUTPUTS**

QUANTITY NAME	DESCRIPTION	UNITS
VE	output voltage	volts
X1,X2,X3	intermediate state variable	
REF	reference voltage	volts

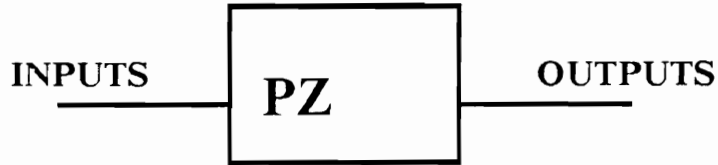
```

MACRO FILE NAME = MACROS
*****
*** COMPENSATOR(INTEGRATOR + 2 ZERO,2 POLE)
*****
DEFINE MACRO = PP SYMBOL = 200
MACRO INPUTS =
  WZ WP
  WM1 WM2
  K ER VO
  WZ2 WP2
  VEH VEL
  FLG T1 T2
*
* VO ;POWER STAGE OUTPUT VOLTAGE
* WZ ;ZERO FREQUENCY(2*PI*F)
* WP ;POLE FREQUENCY(2*PI*F)
* K ;OUTPUT VOLTAGE DIVIDING RATIO
* (IF VTG IVIDER NOT USED,K = 1)
* ER ;REFERENCE VOLTAGE
* WM1; GAIN BEFORE TC
* WM2; GAIN AFTER TC
* TC ; TIME FOR REF. VTG. CHANGE
* FLG; FLAG FOR ENABLE AND DISABLE
MACRO OUTPUTS = X1 X2 X3 VE
  REF WM
  ERR
* X1 ;DUMMY STATE
* VE ;OUTPUT VOLTAGE(TO PWM)
MACRO CODE
MACRO STOP SORT
*
  REFPP-- = ER PP--
  WM PP-- = WM1PP--
  IF(TIME.GE.T1 PP--.AND.TIME.LT.T2 PP--)WM PP-- = WM2PP--
  TC1 = 1/WZ PP--
  TC2 = 1/WP PP--
  ERRPP-- = K PP--*VO PP-- - REFPP--
  VE PP-- = (X3 PP-- + X2 PP--/WZ2PP--)*WP2PP--
MACRO DERIVATIVE,X1 PP-- = ERRPP-- - (X1 PP-- + ERRPP--*TC1)/TC2
MACRO DERIVATIVE,X2 PP-- = WM PP--*(X1 PP-- + ERRPP--*TC1)/TC2
MACRO DERIVATIVE,X3 PP-- = X2 PP-- - VE PP--
*
  IF(FLGPP--.LT.1.E-5)THEN
MACRO DERIVATIVE,X1 PP-- = 0.
MACRO DERIVATIVE,X2 PP-- = 0.
MACRO DERIVATIVE,X3 PP-- = 0.
  END IF
  IF (VE PP-- .GE.VEHPP--)VE PP-- = VEHPP--
  IF (VE PP-- .LE.VELPP--)VE PP-- = VELPP--

MACRO RESUME SORT
END OF MACRO
MODEL DESCRIPTION
LOCATION = 22,PP
END OF MODEL

```

### Compensator (2 poles, 2 zeroes)



### INPUTS

QUANTITY NAME	DESCRIPTION	UNITS
VO	power stage output voltage	volts
ER	reference voltage	volts
ER2	reference vtg after TC	volts
WZ1,WZ2	zero frequencies	rad/sec
WP	pole frequency	rad/sec
TC	time for ref vtg change	sec

### OUTPUTS

QUANTITY NAME	DESCRIPTION	UNITS
VE	output voltage	volts
X1,X2	intermediate state variable	
REF	reference voltage	volts

```

*****
*** COMPENSATOR(2 ZERO,2 POLE)
*****
MACRO FILE NAME = MACROS
DEFINE MACRO = PZ
MACRO INPUTS =
    WM  WZ1  WZ2  WP
    K   ER   VO
    FLG
*
* VO ;POWER STAGE OUTPUT VOLTAGE
* WZ1,WZ2 ;ZERO FREQUENCIES(2*PI*F)
* WP ;POLE FREQUENCY(2*PI*F)
* K ;OUTPUT VOLTAGE DIVIDING RATIO
*   (IF VTG IVIDER NOT USED,K = 1)
* ER ;REFERENCE VOLTAGE
*
MACRO OUTPUTS = X1  X2  VE
* X1,X2 ;DUMMY STATE
* VE ;OUTPUT VOLTAGE(TO PWM)
MACRO CODE
MACRO STOP SORT
*
    Z2 = WM PZ--*WP PZ--/WZ1PZ--/WZ2PZ--
    ERR = K PZ--*VO PZ-- - ER PZ--
    VE PZ-- = X2 PZ-- + Z2*ERR
MACRO DERIVATIVE,X1 PZ-- = ERR *WM PZ--*WP PZ--
MACRO DERIVATIVE,X2 PZ-- = X1 PZ-- + Z2*(WZ1PZ-- + WZ2PZ--)*ERR
    &    -WP PZ--*VE PZ--
*
    IF(FLGPZ--.LT.1.E-5)THEN
MACRO DERIVATIVE,X1 PZ-- = 0.
MACRO DERIVATIVE,X2 PZ-- = 0.
    END IF

MACRO RESUME SORT
END OF MACRO
MODEL DESCRIPTION
LOCATION = 22,PZ
END OF MODEL

```



### Compensator (2 poles, 1 zero)



### INPUTS

QUANTITY NAME	DESCRIPTION	UNITS
VO	power stage output voltage	volts
ER	reference voltage	volts
ER2	reference vtg after TC	volts
WZ	zero frequency	rad/sec
WP	pole frequency	rad/sec
TC	time for ref vtg change	sec

### OUTPUTS

QUANTITY NAME	DESCRIPTION	UNITS
VE	output voltage	volts
X1	dummy state variable	
REF	reference voltage	volts

```

MACRO FILE NAME = MACROS
*****
*** COMPENSATOR(1 ZERO,2 POLE)
*****
DEFINE MACRO = MP  SYMBOL = 200
MACRO INPUTS =
    WZ  WP
    WM1 WM2
    K   ER  VO
    TC1 TC2
    FLG
*
* VO ;POWER STAGE OUTPUT VOLTAGE
* WZ ;ZERO FREQUENCY(2*PI*F)
* WP ;POLE FREQUENCY(2*PI*F)
* K ;OUTPUT VOLTAGE DIVIDING RATIO
*   (IF VTG IVIDER NOT USED,K = 1)
* ER ;REFERENCE VOLTAGE
* WM1; GAIN BEFORE TC
* WM2; GAIN AFTER TC
* TC ; TIME FOR REF. VTG. CHANGE
* FLG; FLAG FOR ENABLE AND DISABLE
MACRO OUTPUTS = X1  VE  REF
                ERR  WM
* X1 ;DUMMY STATE
* VE ;OUTPUT VOLTAGE(TO PWM)
MACRO CODE
MACRO STOP SORT
*
    REFMP-- = ER MP--
    WM MP-- = WM1MP--
    IF(TIME.GE.TC1MP--.AND.TIME.LT.TC2MP--)WM MP-- = WM2MP--
    TC1 = 1/WZ MP--
    TC2 = 1/WP MP--
    ERRMP-- = K MP--*VO MP-- - REFMP--
MACRO DERIVATIVE,X1 MP-- = ERRMP-- - (X1 MP-- + ERRMP--*TC1)/TC2
MACRO DERIVATIVE,VE MP-- = WM MP--*(X1 MP-- + ERRMP--*TC1)/TC2
*
    IF(FLGMP--.LT.1.E-5)THEN
MACRO DERIVATIVE,X1 MP-- = 0.
MACRO DERIVATIVE,VE MP-- = 0.
    END IF
MACRO RESUME SORT
END OF MACRO
MODEL DESCRIPTION
LOCATION = 22,MP
END OF MODEL

```

### current feedback loop



### INPUTS

QUANTITY NAME	DESCRIPTION	UNITS
IL	inductor current	amps
NI	current transformer turn ratio	
NP	primary # of turn	henries
LP	primary inductance	

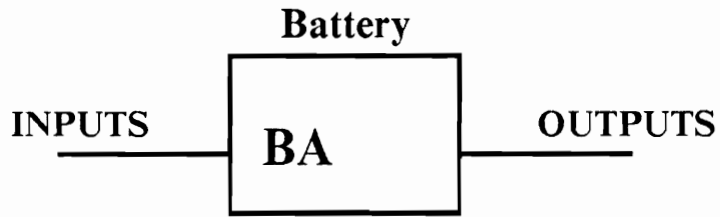
### OUTPUTS

QUANTITY NAME	DESCRIPTION	UNITS
VI	output control voltage	volts

```

*****
*** CURRENT LOOP (C I C) MODULE
*****
MACRO FILE NAME = MACROS
DEFINE MACRO = CC SYMBOL = 200
MACRO INPUTS =
    IL  NI  RW
    NP  LP
*
* IL ; INDUCTOR CURRENT(FROM POWER STAGE)
*   (FLUX IF BUCK/BOOST)
* NI ; CURRENT TRANSFORMER TURNS RATIO
* NP ; IF FLYBACK : POWER STAGE PRIMARY # OF TURNS
*   OTHERWISE NP = 1
* LP ; IF FLYBACK ; POWER TRANSFORMER PRIMARY INDUCTANCE
*   OTHERWISE LP = 1
*
MACRO OUTPUTS = VI
*
* VI ; CIC OUTPUT CONTROL VOLTAGE
*
MACRO CODE
MACRO STOP SORT
*
    VI CC-- = NP CC--/LP CC--*
    &    IL CC--*RW CC--/NI CC--
*
MACRO RESUME SORT
END OF MACRO
MODEL DESCRIPTION
LOCATION = 22,CC
END OF MODEL

```



### INPUTS

QUANTITY NAME	DESCRIPTION	UNITS
IB	current from charger	amps
TB	battery temperature	degrees
NC	number of serial cells	
IQC	control flag for battery status	

### OUTPUTS

QUANTITY NAME	DESCRIPTION	UNITS
VC1	battery voltage	volts
VC2	internal variable	volts
TB	battery temperature	degrees
NC	number of serial cells	
IQC	control flag for battery status	

```

MACRO FILE NAME = MACROS
DEFINE MACRO = BA
*****
** BATTERY MODEL *****
*****
*
*   <--I1                                 <-- IB
*   _____/\/\/\-----O
*   |          |          RS
*   |          |          |
*   | \D/  /D\  |          |
*   | --- -- |          |
*   | _____|  = = = = C1          VI
*   |          |          |
*   *I3 |          |          |
*   | --- -- |          |
*   | \D/  = = = C2  |          |
*   | / --- -- |          |
*   |          |          |
*   |          |          |-----O
*   |          |          |
*   |          |          |
*   = = = = = < IB
*   |
*   = = = = = > VC1
*
MACRO INPUTS = IB TB NC
                I0
* TB = BATTERY TEMPERATURE
* NC = NUMBER OF SERIAL CELLS
* I0 = PARAMETER VALUE FOR LEAKAGE CURRENT(I3)
*
MACRO OUTPUTS = VC1 VC2
                I1 I3
                MIN
* MIN = MINUTE
MACRO CODE
MACRO STOP SORT

VM = 1.348
RS = .0005
D1V0 = 0.025
D1I0 = 5.
D3V0 = 1.348
D1K2 = 0.8
D3K2 = 1.35
D1D3L = 1.5

MINBA-- = TIME / 60.

AA = 40.27 * D1V0 / D1D3L
FK1DEN = DEXP(AA) - 1.
DD = 1. - ( 519. / ( 459. + TB BA-- ) )
FK1NUM = DEXP ( 40.27 * D1K2 * DD )

```

```

FK1 = D1I0 * FK1NUM / FK1DEN
*
FK3 = 20900. / ( D1D3L * ( 459. + TB BA-- ) )
*
BA = 40.27 * D3V0 / D1D3L
FK2DEN = DEXP ( BA ) - 1.
FK2NUM = DEXP ( 40.27 * D3K2 * DD )
FK2 = I0 BA-- * FK2NUM / FK2DEN
*
PP = ( VC1BA-- / NC BA-- - VM ) ** 2
QQ = ( VC2BA-- / NC BA-- - VM ) ** 2
C1 = 80000. * DEXP ( -120. * PP ) + 5000.
C2 = 205.E4 * ( DEXP ( -400. * QQ ) ) + 5000.
C1 = C1 / NC BA--
C2 = C2 / NC BA--
*
*   AH BA-- = IBRBA-- * TIME / 3600.
*
I1 BA-- = 2. * FK1 * DSINH ( FK3 * ( VC1BA-- - VC2BA-- )
C      / NC BA-- )
I3 BA-- = FK2 * ( DEXP ( FK3 * VC2BA-- / NC BA-- ) - 1. )
MACRO DERIVATIVES, VC1BA-- = ( IB BA-- - I1 BA-- ) / C1
MACRO DERIVATIVES, VC2BA-- = ( I1 BA-- - I3 BA-- ) / C2
MACRO RESUME SORT
END OF MACRO
*****
MODEL DESCRIPTION
LOCATION = 22, BA
END OF MODEL
PRINT

```

## PWM (large-signal model)



### INPUTS

QUANTITY NAME	DESCRIPTION	UNITS
VE	error voltage	volts
VI	output from current loop	volts
IQ	switching function from PWM	
TI	switching period	sec
ER	reference voltage	volts
VP	amplitude of external ramp	volts

### OUTPUTS

QUANTITY NAME	DESCRIPTION	UNITS
VC	control voltage	volts
IQ	switching function	
VR	external ramp voltage	volts
D	duty cycle	



```

*****
** P.W.M (CONSTANT FREQUENCY)***
*****
MACRO FILE NAME = MACROS
DEFINE MACRO = WM
MACRO INPUTS =
    TI VP VQ ER
    CIC SCM
    VE VI
    VCX VCN ILX
    DMN DMX
*
* VE ; AMPLIFIED ERROR VTG(FROM COMPENSATOR)
* VI ; INPUT VOLTAGE FROM CURRENT FEEDBACK MODULE
* CIC; IF CIC, CIC = 1
*   OTHERWISE CIC = 0
* SCM; IF SCM, SCM = 1
*   OTHERWISE SCM = 0
* TI ; SWICHING INTERVAL
* VP ; AMPLITUDE OF EXTERNAL RAMP
*   ( IF EXT.RAMP NOT USED,VP = 0)
* VQ ; THRESHOLD VOLTAGE
* ER ; REFERNCE VOLTAGE OF OP.AMP
*
MACRO OUTPUTS =
    VR VC IQ TN
    VS D
*
* VR ; EXTERNAL RAMP VOLTAGE
* VC ; TOTAL CONTROL VOLTAGE
* IQ ; SWITCHING FUNCTION
*   (IF SWITCH = 0N, IQ = 1)
*   (IF SWITCH = OFF,IQ = 0)
*
MACRO CODE
MACRO STOP SORT
****
*** RAMP GENERATION
*
    IF(TIME.EQ.0.)THEN
        N WM-- = 0.
        NP WM-- = 0.
    END IF
    TN WM-- = (TIME + TI WM--)/TI WM--
    NP WM-- = N WM--
    N WM-- = IDINT(TN WM--)
    VR WM-- = VP WM--*(TN WM-- -N WM--)+ VQ WM--
****
    VC WM-- = -VE WM---CICWM--*VS WM---
    &   SCMWM--*VI WM--
* OP-AMP SATURATION
    IF(VC WM--.GT.VCXWM--)VC WM-- = VCXWM--
    IF(VC WM--.LT.VCNWM--)VC WM-- = VCNWM--
* COMPARATOR
    EPS = 1.E-5
    IF(IQ WM--.GT.EPS)THEN

```

```

VS WM-- = VI WM--
  IF(VR WM--.GT.VC WM--)THEN
    IQ WM-- = 0
  END IF
ELSE
  VS WM-- = 0.
END IF
IF(NP WM--.NE.N WM--)IQ WM-- = 1
*PROTECTION
D WM-- = TN WM---N WM--
IF(D.LT.DMNWM--)IQ WM-- = 1
IF(D.GT.DMXWM--)IQ WM-- = 0
IF(IL WM--.GT.ILXWM--)IQ WM-- = 0
*
MACRO RESUME SORT
END OF MACRO
MODEL DESCRIPTION
LOCATION= 22, WM
END OF MODEL

```

## PWM small-signal



### INPUTS

QUANTITY NAME	DESCRIPTION	UNITS
VE	input voltage	volts
VI	voltage from current loop	volts
FM	PWM gain	
VJ	injection voltage	volts
NN	coefficient for loop gain mesure	
MM	coefficient for loop gain mesure	

### OUTPUTS

QUANTITY NAME	DESCRIPTION	UNITS
DH	duty ratio	
HD	duty ratio (dummy)	

```

*****
**   PWM (SMALL SIGNAL) *****
*****
MACRO FILE NAME = MACROS
DEFINE MACRO = PW
MACRO INPUTS =
  VE  VI
  FM  NN  MM
  VJ  CV  CI  CC
  MACRO OUTPUTS =
  DH  HD
*VE ;INPUT VTG FROM COMPENSATOR MODULE
*VI ;INPUT VTG FROM CURRENT-LOOP MODULE
*FM ;PWM GAIN
*VJ ;INJECTION VOLTAGE
*DH ;DUTY RATIO
*HD ;DUTY RATIO(DUMMY)
*CC ;WHEN MESURING T2 CC = 1, OTHERWISE CC = 0
MACRO CODE
MACRO STOP SORT
*
  HD PW-- = -FM PW--*(CV PW--*VE PW-- +
  &      CI PW--*VI PW--)
  DH PW-- = NN PW--*HD PW-- + MM PW--*VJ PW--
  1      -FM PW--*CC PW--*VI PW--
*****
*
MACRO RESUME SORT
END OF MACRO
MODEL DESCRIPTION
LOCATION = 22, PW
END OF MODEL

```

## PWM model with new model for current-mode control



### INPUTS

QUANTITY NAME	DESCRIPTION	UNITS
VC	input voltage from compensator	volts
IL	charge current from current loop	amps
FM	PWM gain	
VJ	injection voltage	volts
NN	coefficient for loop gain mesure	
MM	coefficient for loop gain mesure	

### OUTPUTS

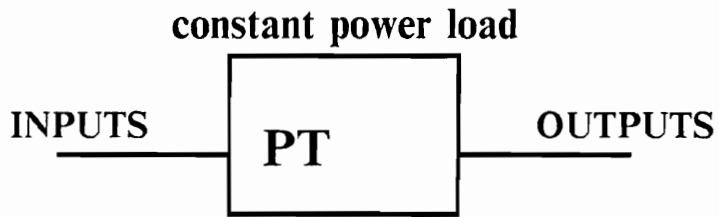
QUANTITY NAME	DESCRIPTION	UNITS
DH	duty ratio	
HD	duty ratio (dummy)	

```

*****
** CURRENT MODE CONTROL PWM (SMALL SIGNAL) *****
*****
MACRO FILE NAME = MACROS
DEFINE MACRO = FM
MACRO INPUTS =
  VG IL VO VC
  FM NN MM
  VJ
  KF KR RI TS
MACRO OUTPUTS =
  X1 X2
  DH HD
  U Y
*VC ;INPUT VTG FROM COMPENSATOR MODULE
*IL ;INPUT VTG FROM CURRENT-LOOP MODULE
*FM ;PWM GAIN
*VJ ;INJECTION VOLTAGE
*DH ;DUTY RATIO
*HD ;DUTY RATIO(DUMMY)
MACRO CODE
MACRO STOP SORT
*
  PI = 3.141592
  WN = PI /TS FM--
  Q = -2./PI
  U FM-- = IL FM-- * RI FM--
  Y FM-- = X2 FM-- + 1.E14 * U FM--/WN**2

  HD FM-- = FM FM--*(KF FM-- *VG FM-- + KR FM-- *VO FM--
  & -Y FM-- + VC FM--)
  DH FM-- = NN FM--*HD FM-- + MM FM--*VJ FM--
*****
MACRO DERIVATIVE,X1 FM-- = 1.E14 *U FM-- -1.E14 *Y FM--
MACRO DERIVATIVE,X2 FM-- = X1 FM-- + 1.E14*U FM--/(Q *WN)
  & - 1.E7 * Y FM--
*
MACRO RESUME SORT
END OF MACRO
MODEL DESCRIPTION
LOCATION = 22, FM
END OF MODEL

```



### INPUTS

QUANTITY NAME	DESCRIPTION	UNITS
VL	input voltage	volts
PW1,PW2	const power values	W
PC	PC = 1 for step load change, PC = 0 for linear change	
VR	minimum vtg to maintain const power	volts
SW	slope of time varying power	

### OUTPUTS

QUANTITY NAME	DESCRIPTION	UNITS
IL	load current	amps
PW	load power	W

```

*****
* CONSTANT POWER LOAD
*****
MACRO FILE NAME = MACROS
*****
DEFINE MACRO = PT
* LOAD MODEL
* INPUT IS BUS VOLTAGE (VL) AND POWER (PW) OUTPUT IS ILOAD
* OPTION1 ; A CONSTANT POWER DEVICE (VL*IL = PW)
* OPTION2 ; THE POWER IS LINEARLY VARIED
*
*
* VL ----->
*
* IL <-----
*
**** FOR CONSTANT POWER ; PC PT = 1.
**** FOR TIME VARYING POWER ; PC PT = 0.
*
MACRO INPUTS = VL  PW1  PW2  PC  PWO
              VR  TC  SW
MACRO OUTPUTS = IL
              PW  SL
MACRO CODE
MACRO STOP SORT

      IF(PC PT--.EQ.1.)GO TO + + +23
      PW PT-- = SW PT--*TIME + PWOPT--
      IL PT-- = PW PT-- / VL PT--
      GOTO + + +33
+ + +23 CONTINUE
      PW PT--=PW1PT--
      IF(TIME.GE.TC PT--)PW PT--=PW2PT--
      IL PT-- = PW PT-- / VL PT--
+ + +33 SL PT-- = PW PT-- /VR PT--/VR PT--
      IF (VL PT-- .LT. VR PT--) IL PT-- = SL PT--*VL PT--
      IF(IL PT-- .LT. 0.) IL PT-- = 0.
MACRO RESUME SORT
END OF MACRO
*****
*****
MODEL DESCRIPTION
LOCATION = 42, PT
END OF MODEL
PRINT

```



### constant power load



### INPUTS

QUANTITY NAME	DESCRIPTION	UNITS
VI	input voltage (small-signal)	volts
PW	const power values	W
VBS	bus voltage (dc value)	volts

### OUTPUTS

QUANTITY NAME	DESCRIPTION	UNITS
IO	load current (small-signal)	amps
ISS	load current (dc)	amps
R	resistance (dc)	ohms

```

*****
* CONSTANT POWER LOAD
* SMALL SIGNAL MODEL 3/14/90
*****
MACRO FILE NAME = MACROS
*****
DEFINE MACRO = SL
* LOAD MODEL
* INPUT IS BUS VOLTAGE (V1) AND POWER (PW) OUTPUT IS ILOAD
*
*
* V1 ---->
*
* IO <-----
*
*
MACRO INPUTS = V1  PW  VBS
MACRO OUTPUTS = IO  R  ISS
MACRO CODE
MACRO STOP SORT

    ISSL-- = PW SL--/ VBSSL--
    R SL-- = - VBSSL--/ISSL--
    IO SL-- = V1 SL-- / R SL--
MACRO RESUME SORT
END OF MACRO
*****
*****
MODEL DESCRILION
LOCATION=42, SL
END OF MODEL
PRINT

```

## Peak Power Tracker



### INPUTS

QUANTITY NAME	DESCRIPTION	UNITS
IO	input current from solar array	amps
PO	solar array power	watts
TI	switching period of converter	seconds
DRF	magnitude of reference change	volts
DPM	min. power to give the reference change	watts

### OUTPUTS

QUANTITY NAME	DESCRIPTION	UNITS
VRF	reference voltage to converter	volts
DPI	derivative of power w.r.t. current	

```

*****
*** PEAK POWER TRACKER
***      4/4/90
** CALCULATE DP/DI
*****
MACRO FILE NAME=MACROS
DEFINE MACRO=PK
MACRO INPUTS=
  IO  PO  TI
  DPM DRF  VRI
* DPM ; MIN DEL P
* DRF ; DEL REF
* VRI ; INITIAL V REF
MACRO OUTPUTS = VRF  DLI  DLP  DPI
                TN  NP  N
* DLI ; DEL I
* DLP ; DEL P
* DPI ; DEL P/ DEL I
MACRO CODE
MACRO STOP SORT
  IF(TIME.EQ.0.)THEN
    VRFPK-- = VRIPK--
    N PK-- = 0.
    NP PK-- = 0.
    END IF
**
  TN PK-- = (TIME + TI PK--)/TI PK--
  NP PK-- = N PK--
  N PK-- = IDINT(TN PK--)
*
  IF(NP PK--.NE.N PK--)THEN
**
    DLIPK-- = IO PK-- - IOP
    DLPPK-- = PO PK-- - POP
    IOP = IO PK--
    POP = PO PK--
    IF(DLIPK--.EQ.0.)GO TO + + + 77
    DPIPK-- = DLPPK-- / DLIPK--
*
    IF(DPIPK--.LT.0.)THEN
      IF(DABS(DLPPK--).GE.DPMPK--)THEN
        VRFPK-- = VRFPK-- + DRFPK--
        END IF
      ELSE
        IF(DABS(DLPPK--).GE.DPMPK--)THEN
          VRFPK-- = VRFPK-- - DRFPK--
          END IF
        END IF
    + + + 77 CONTINUE
    END IF
MACRO RESUME SORT
END OF MACRO
MODEL DESCRIPTION
LOCATION = 22,PK
END OF MODEL

```

## Appendix B

### EASY5 Program List

Simulations in this dissertation were performed employing EASY5 software. The system model generation programs (MOD files) and analysis programs (ANC files) are provided.

#### *B.1 Large-Signal Model of the Charger System employing Voltage-Mode Control*

```
***** [CHSL.MOD]
*****
**** CHARGER SYSTEM MODEL ****
** LARGE-SIGNAL MODEL    REVISED 3/12/91
****   FOR VOLTAGE-MODE CONTROL
*****
MACRO FILE NAME = MACROS
MODEL DESCRIPTION
***** SOLAR ARRAY *****
LOCATION = 1,SI,INPUTS = BF(VB = VX)
```

```

***** BUS FILTER CAPACITOR *****
LOCATION = 4,BF,INPUTS = SI(IO = I1),MC2(S,2 = I2)
***** CHARGER *****
*LOCATION = 12,FF,INPUTS = BC(I1 = I2),AR(VB = V1)
LOCATION = 13,CH, INPUTS = BF(VB = V1),BA(VC1 = VBA),WM(IQ = IQ)
LOCATION = 35,WM, INPUTS = PP(VE = VE)
LOCATION = 33,UP
LOCATION = 46,PP, INPUTS = BF(VB = VO),UP(S2 = WM1)
***** BATTERY *****
LOCATION = 57,BA, INPUTS = CH(IL = IB)
***** LOAD *****
LOCATION = 69,PT,INPUTS = BF(VB = VL)
*****
LOCATION = 79,MC2,INPUTS = CH(I1 = S,1),PT(IL = S,3)
END OF MODEL
PRINT

```

```

*****
****   [CHSL.ANC]
*CHRAGER VTG MODE 3/12/91
** SINGLE LOOP CONTROL
PARAMETER VALUES
LL SI = 0.87
LLSSI = 0.,LS2SI = 1000., TILSI = 1., LLMSI = 0.6
LLXSI=1
NP SI = 295, NS SI = 320
*****
NP SI=300, NS SI=360
*****
LL SI= 1
*LL SI= .6
*INITIAL GUESS
IOISI = 45.75
*IOISI=20
*****
CB BF = 100E-6,RC BF = 50E-3
C BF=1900E-6
INITIAL CONDITIONS
VB BF = 120,VC BF = 120
*****
*****INPUT FILTER
*INITIAL CONDITIONS
*V2 FF = 27.0, VC1FF = 27, I1 FF = 0
PARAMETER VALUES
*L1 FF = 10.E-6, C1 FF = 450E-6, RL1FF = 0.001
*C2 FF = 26E-6, RC1FF = 0.5
*** CHARGER POWER STAGE
PARAMETER VALUES
L CH= 200E-6
L CH= 50E-6
RL CH= 0.1
RL CH= .05
INITIAL CONDITIONS
IL CH= 15.8
IL CH= 0
*****
PARAMETER VALUES
*****
TI WM = 20E-6, VP WM= 4, VQ WM= 0
TI WM= 11.11111E-6
DMNWM= 0,DMXWM= 1.
*DMNWM = .544444,DMXWM = .544444
CICWM= 0,SCMWM= 0
VI WM= 0
*****
**VTG LOOP COMPENSATER
PARAMETER VALUES
*****
SLPUP= -1200E3
*SLPUP= -10E3
*SLPUP= -1E15
DLYUP= 2.E-3
DLYUP= 0

```

```

LIMUP = -2400
*LIMUP = -24
ER PP = 120, WP PP = 10E3
K PP = 1
VEHPP = 0, VELPP = -15
WM2PP = -10
WZ PP = 754
WP2PP = 31.4E3
WZ2PP = 1.88E3
FLGPP = 1
T1 PP = 12E-3, T2 PP = 1
WZ PP = 1630, WZ2PP = 5.85E3
WP2PP = 283E3
*****
** BATTERY **
TB BA = 50
NC BA = 90
I0 BA = 0.22
INITIAL CONDITIONS
VC1BA = 64, VC2BA = 64
*****
PARAMETER VALUES
C1 MC2 = 1, C2 MC2 = 1, C3 MC2 = 0, C4 MC2 = 0
S4 MC2 = 0
*****
PC PT = 1
VR PT = 10
PWOPT = 4000, SW PT = 200000
*****
PW1PT = 4000, PW2PT = 3600
*PW1PT = 1800, PW2PT = 1620
*PW2PT = 2500
TC PT = 23E-3
ONLINE PLOTS
INT MODE = 4
TMAX = 4E-3, TINC = 0.05E-6
PRATE = 1E3, OUTFRATE = 20
DISPLAY1
VB BF, IL CH, VC WM
DISPLAY2
VB BF, VC BF, VC WM, VE PP
SIMULATE
XIC-X
PARAMETER VALUES
*T1 PP = 2E-3, T2 PP = 3E-3
*TC PT = 11E-3, TMAX = 5.999E-3
TMAX = 15E-3
PRATE = 1E3, OUTFRATE = 40
OUTFRATE = 100
*SIMULATE
*****

```



## *B.2 Small-Signal Model of the Charger System employing Voltage-Mode Control*

```
*****
**** DET CHARGER SYSTEM MODEL ****
*** VTG REGULATION MODE
** SMALL-SIGNAL MODEL    REVISED 3/11/91
*   SINGLE LOOP CONTROL  [CCM.MOD]
*****
MACRO FILE NAME = MACROS
MODEL DESCRIPTION
***** SOLAR ARRAY *****
LOCATION = 1,SS, INPUTS = BF(VB = VO)
***** BUS FILTER CAPACITOR *****
LOCATION = 4,BF, INPUTS = SS(IO = I1),LM(I2 = I2)
***** CHARGER *****
*LOCATION = 12,FF,INPUTS = BC(I1 = I2),AR(VB = V1)
LOCATION = 13,CS, INPUTS = BF(VB = V1),BA(VC1 = V2),PW(DH = DH)
LOCATION = 35,PW, INPUTS = PP(VE = VE)
LOCATION = 46,PP,INPUTS = BF(VB = VO)
*LOCATION = 48,CC, INPUTS = CS(IL = IL)
***** BATTERY *****
LOCATION = 57,BA,INPUTS = CS(IL = IB)
***** LOAD *****
LOCATION = 69,SL,INPUTS = BF(VB = V1)
*****
LOCATION = 79,MC2,INPUTS = CS(I1 = S,1),SL(IO = S,3)
*****
LOCATION = 54,LM,INPUTS = MC2(S,2 = I1)
*****
END OF MODEL
PRINT
```

```

*****
*CHARGER SMALL-SIGNAL [CCM.ANC]
***** 3/11/91
***** SINGLE-LOOP CNTL
PARAMETER VALUES
RS SS = .05,RSHSS = 250,CD SS = .24E-6,CT SS = .063E-6
NP SS = 395, NS SS = 320
*****
NP SS = 300, NS SS = 360
*****
** CURRENT SOURCE REGION
RD SS = 87
*****
** VTG SOURCE REGION
*RD SS = 1
*****
CB BF = 1E-6,RC BF = 50E-3
C BF = 2000E-6
*****
*****INPUT FILTER
*L1 FF = 10.E-6, C1 FF = 450E-6, RL1FF = 0.001
*C2 FF = 26E-6, RC1FF = 0.5
*** CHARGER POWER STAGE
PARAMETER VALUES
L CS = 50E-6
VBACS = 65,VBSCS = 120
RL CS = .05
*** AT HEAVY LOAD
ILSCS = 23
*** AT LIGHT LOAD
ILSCS = 3.3
*****
**VTG LOOP COMPENSATER
ER PP = 0
K PP = 1
WZ PP = 1630
WP PP = 10E3
*****
WP2PP = 126E3
WZ2PP = 11.3E3
WM PP = -4800
FLGPP = 1
*****
WM PP = -900
WZ PP = 1260
WZ2PP = 1880
WP2PP = 31.4E3
*****
** BATTERY **
TB BA = 50
NC BA = 90
IO BA = 0.22
*****
C1 MC2 = 1, C2 MC2 = 1, C3 MC2 = 0,C4 MC2 = 0
S4 MC2 = 0
*****

```

```

PW SL = 1800
VBSSL = 120
*****
FM PW = .0
NN PW = 0, MM PW = 0, VJ PW = 0
CV PW = 0, CI PW = 0
CC PW = 0
VI PW = 0
*****
NN LM = 1,MM LM = 0,IILM = 2
*****
ONLINE PLOTS
*****
PRINT CONTROL = 3.005
TF MANUAL SCALE
FREQ MIN = 6.29
FREQ MAX = 6.28E5
*****
NO STATES
INT CONTROL = IL CS = 1
TF INPUT = DH PW, TF OUTPUT = IL CS
TITLE = IL / D
*TRANSFER FUNCTION
*****
TF INPUT = DH PW,TF OUTPUT = I1 CS
TITLE = I1/D
*TRANSFER FUNCTION
*****
TF INPUT = VB BF,TF OUTPUT = IL CS
TITLE = IL/VB
*TRANSFER FUNCTION
*****
TF INPUT = VB BF,TF OUTPUT = I1 CS
TITLE = I1/VB
*TRANSFER FUNCTION
*****
NO STATES
INT CONTROLS
VC SS = 1,VB BF = 1,VC BF = 1
PARAMETER VALUES
C1 MC2 = 0,C2 MC2 = 0
TF INPUT = S2 MC2,TF OUTPUT = VB BF
TITLE = SA IMP.
*TRANSFER FUNCTION
*****
PARAMETER VALUES
C1 MC2 = 0,C2 MC2 = 1
TF INPUT = S2 MC2,TF OUTPUT = VB BF
*TF INPUT = I1 CS
TITLE = SA IMP. + LOAD
*TRANSFER FUNCTION
PARAMETER VALUES
C1 MC2 = 1
INT CONTROLS
IL CS = 1
TF INPUT = S2 MC2,TF OUTPUT = VB BF

```

```

TITLE = OPEN LOOP Z
*TRANSFER FUNCTION
*****
PARAMETER VALUES
NN PW = 1,CV PW = 1,CI PW = 0
FM PW = .25
VJ PW = 3
ALL STATES
INT CONTROLS
VC SS = 0,VB BF = 0,VC BF = 0
TF INPUT = VB BF,TF OUTPUT = I1 CS
TITLE = Y
*TRANSFER FUNCTION
*****
PARAMETER VALUES
NN LM = 0, MM LM = -1
TITLE = LOOP GAIN 1
TF INPUT = I1LM, TF OUTPUT = S2 MC2
*TRANSFER FUNCTION
PARAMETER VALUES
NN LM = 1, MM LM = 0
*****
ALL STATES
TITLE = BUS IMPEDANCE
TF INPUT = S2 MC2,TF OUTPUT = VB BF
TRANSFER FUNCTION
*****
PARAMETER VALUES
NN LM = 0, MM LM = -1
TITLE = NEW LOOP GAIN
TF INPUT = I1LM, TF OUTPUT = S2 MC2
*TRANSFER FUNCTION
PARAMETER VALUES
NN LM = 1, MM LM = 0
*****
PARAMETER VALUES
NN PW = 0, MM PW = -1
VJ PW = 1,CI PW = 0
TITLE = LOOP GAIN
TF INPUT = VJ PW, TF OUTPUT = HD PW
TRANSFER FUNCTION
PARAMETER VALUES
CV PW = 0,CI PW = 1
TITLE = LOOP GAIN T1
TF INPUT = VJ PW, TF OUTPUT = HD PW
*TRANSFER FUNCTION
TITLE = LOOP GAIN T1
PARAMETER VALUES
CV PW = 1
TF INPUT = VJ PW, TF OUTPUT = HD PW
*TRANSFER FUNCTION
TITLE = LOOP GAIN T2
PARAMETER VALUES
CI PW = 0,CC PW = 1
TF INPUT = VJ PW, TF OUTPUT = HD PW
*TRANSFER FUNCTION

```

```

PARAMETER VALUES
NN PW = 1, MM PW = 0
VJ PW = 0, CI PW = 1, CC PW = 0
*****
PARAMETER VALUES
C2 MC2 = 1
TF INPUT = S2 MC2,TF OUTPUT = VB BF
TITLE = SA + PT
*TRANSFER FUNCTION
PARAMETER VALUES
C1 MC2 = 1
INT CONTROLS
IL CS = 1
TF INPUT = S2 MC2,TF OUTPUT = VB BF
TITLE = SA + PT + CS
*TRANSFER FUNCTION
INT CONTROLS
VC1BA = 1,VC2BA = 1
TF INPUT = S2 MC2,TF OUTPUT = VB BF
TITLE = SA + PT + CS + BA
*TRANSFER FUNCTION
NO STATES
INT CONTROLS
VC1BA = 1,VC2BA = 1
TF INPUT = IL CS,TF OUTPUT = VC1BA
TITLE = BATTERY IMP.
*TRANSFER FUNCTION
ALL STATES
PARAMETER VALUES
FM PW = 0,CV PW = 0,CI PW = 0
CC PW = 0
INT CONTROLS
X1 PP = 0,X2 PP = 0,X3 PP = 0
TF INPUT = DH PW,TF OUTPUT = VB BF
TITLE = VB/D
*TRANSFER FUNCTION
*****
TF INPUT = DH PW,TF OUTPUT = VC BF
TITLE = VC/D
*TRANSFER FUNCTION
*****
TF INPUT = DH PW,TF OUTPUT = IL CS
TITLE = IL/D
*TRANSFER FUNCTION
*****
NO STATES
INT CONTROLS
X1 PP = 1,X2 PP = 1,X3 PP = 1
TF INPUT = VB BF,TF OUTPUT = VE PP
TITLE = COMPENSATOR
*TRANSFER FUNCTION

```

```

*****
**** DET CHARGER SYSTEM MODEL ****
*** VTG REGULATION MODE closed-loop model
** SMALL-SIGNAL MODEL using PWM switch model
** REVISED 2/11/91 DCM
* [DCM.MOD]
*****
MODEL DESCRIPTION
***** SOLAR ARRAY *****
LOCATION = 1,SS, INPUTS = BF(VB = VO)
***** BUS FILTER CAPACITOR *****
LOCATION = 4,BF, INPUTS = SS(IO = I1),MC(S,2 = I2)
***** CHARGER *****
LOCATION = 13,DM, INPUTS = BF(VB = V1),BA(VC1 = V2),FD(DH = DH)
LOCATION = 35,FD, INPUTS = BF(VB = VG),LM(VC = VC)
LOCATION = 46,PP, INPUTS = BF(VB = VO)
***** BATTERY *****
LOCATION = 57,BA,INPUTS = DM(IL = IB)
***** LOAD *****
LOCATION = 69,SL,INPUTS = BF(VB = V1)
*****
LOCATION = 79,MC,INPUTS = DM(I1 = S,1),SL(IO = S,3)
*****
LOCATION = 54,LM,INPUTS = PP(VE = VI)
END OF MODEL
PRINT

```

```

*****
* CHARGER SMALL-SIGNAL [DCM.ANC]
* DCM
* USING PWM SWITCH MODEL
***** 2/11/91
PARAMETER VALUES
RS SS = .05, RSHSS = 250, CD SS = .24E-6, CT SS = .063E-6
NP SS = 395, NS SS = 320
*****
NP SS = 300, NS SS = 360
*****
** CURRENT SOURCE REGION
RD SS = 87
*****
** VTG SOURCE REGION
*RD SS = 1
*RD SS = 3.6
*****
CB BF = 1E-6, RC BF = 50E-3
C BF = 2000E-6
*****
*****INPUT FILTER
*L1 FF = 10.E-6, C1 FF = 450E-6, RL1FF = 0.001
*C2 FF = 26E-6, RC1FF = 0.5
*** CHARGER POWER STAGE
PARAMETER VALUES
L DM = 200E-6
L DM = 50E-6
RL DM = 0.05
VBADM = 65, VBSDM = 120
DS DM = .13
DS DM = .54
I1SDM = 0.1136
I1SDM = 1.78
*****
PW SL = 1800
VBSSL = 120
*****
*PW SL = 1E-3
*****
** BATTERY **
TB BA = 50
NC BA = 90
I0 BA = 0.22
*****
C1 MC = 1, C2 MC = 1, C3 MC = 0, C4 MC = 0
S4 MC = 0
*****
*****
* SINGLE LOOP
FM FD = .25
NN FD = 0, MM FD = 0
*****
*****
VJ FD = 1
*****

```

```

*FOR SINGLE LOOP
KF FD=0
*****
WM1PP= -2100
WM2PP= -218
WZ PP= 565, WZ2PP= 628E3
WP PP= 10E3,WP2PP= 31.4E3
K PP= 1, ER PP= 0
T1 PP= 1,T2 PP= 1,FLGPP= 1
*****
WZ PP= 1260
WP2PP= 50E3
WZ2PP= 1880
WM1PP= -900
*****
XX LM= 0,YY LM= 0
VJ LM= 1
*****
ONLINE PLOTS
*****
PRINT CONTROL= 3.005
TF MANUAL SCALE
FREQ MIN = 6.29
FREQ MAX = 6.28E5
*FREQ MIN = 10
*FREQ MAX = 1E6
*****
* OPEN LOOP TRANSFER FUNCTION *
*****
ALL STATES
INT CONTROL= IL DM= 1
VC SS= 1
VB BF= 1, VC BF= 1

TF INPUT= DH FD, TF OUTPUT= IL DM
TITLE= IL / D
*TRANSFER FUNCTION
TF INPUT= DH FD, TF OUTPUT= VB BF
TITLE= V / D
*TRANSFER FUNCTION
*****
TF INPUT= DH FD,TF OUTPUT= I1 DM
TITLE= I1/D
*TRANSFER FUNCTION
*****
TF INPUT= S2 MC,TF OUTPUT= VB BF
TITLE= OPEN LOOP Z
*TRANSFER FUNCTION
*****
* CURRENT LOOP GAIN *
*****
PARAMETER VALUES
MM FD= -1
*****
TF INPUT= VJ FD,TF OUTPUT= HD FD
TITLE= CURRENT LOOP GAIN TI

```



```

*TRANSFER FUNCTION
*****
* CONTROL TO OUTPUT *
*****
PARAMETER VALUES
MM FD=0,NN FD=1
*****
TF INPUT = VC LM,TF OUTPUT = VB BF
TITLE = VB / VC
*TRANSFER FUNCTION
*****
* CLOSED LOOP IMP. *
*****
PARAMETER VALUES
MM FD=0,NN FD=1
XX LM=1
*****
TF INPUT = S2 MC,TF OUTPUT = VB BF
TITLE = Z out
TRANSFER FUNCTION
*****
* LOO GAIN *
*****
PARAMETER VALUES
XX LM=0, YY LM=1
*****
TF INPUT = VJ LM,TF OUTPUT = VD LM
TITLE = LOOP GAIN
TRANSFER FUNCTION

```

### ***B.3 Large-Signal Model of the Charger System employing Current-Mode Control***

```
*****
**** CHARGER SYSTEM MODEL **** VTG CONTROL
** LARGE-SIGNAL MODEL REVISD 12/3/90
***** USING CURRENT-MODE CONTROL
*****
MACRO FILE NAME = MACROS
MODEL DESCRIPTION
***** SOLAR ARRAY *****
LOCATION = 1,SI,INPUTS = BF(VB = VX)
***** BUS FILTER CAPACITOR *****
LOCATION = 4,BF,INPUTS = SI(IO = I1),MC2(S,2 = I2)
***** CHARGER *****
*LOCATION = 12,FF,INPUTS = BC(I1 = I2),AR(VB = V1)
LOCATION = 13,CH, INPUTS = BF(VB = V1),BA(VC1 = VBA),WM(IQ = IQ)
LOCATION = 35,WM,INPUTS = MPV(VE = VE),CC(VI = VI)
LOCATION = 33,UP
LOCATION = 46,MPV,INPUTS = BF(VB = VO),UP(S2 = WM1)
LOCATION = 48,CC,INPUTS = CH(IL = IL)
***** BATTERY *****
LOCATION = 57,BA,INPUTS = CH(IL = IB)
***** LOAD *****
LOCATION = 69,PT,INPUTS = BF(VB = VL)
*****
LOCATION = 79,MC2,INPUTS = CH(I1 = S,1),PT(IL = S,3)
END OF MODEL
PRINT
```

```

*****
* CHRAGER VTG REGULATION MODE 12/3/90
* EMPLOYING CURRENT-MODE CONTROL [CHR.ANC]
*****
PARAMETER VALUES
LL SI = 0.87
LLSSI = 0.,LS2SI = 1000., TILSI = 1., LLMSI = 0.6
NP SI = 295, NS SI = 320
*****
NP SI= 300, NS SI= 360
*****
LL SI= 1
*INITIAL GUESS
IOISI = 45.75
*****
CB BF= 100E-6,RC BF= 50E-3
C BF= 1900E-6
INITIAL CONDITIONS
VB BF = 120,VC BF= 119.5
*****
*****INPUT FILTER
*INITIAL CONDITIONS
*V2 FF = 27.0, VC1FF = 27, I1 FF = 0
PARAMETER VALUES
*L1 FF = 10.E-6, C1 FF = 450E-6, RL1FF = 0.001
*C2 FF = 26E-6, RC1FF = 0.5
*** CHARGER POWER STAGE
PARAMETER VALUES
L CH= 50E-6
RL CH= 0.05
INITIAL CONDITIONS
IL CH= 0
*****
PARAMETER VALUES
*****
TI WM = 11.1111E-6, VP WM= 2., VQ WM= 0
DMNWM= 0.,DMXWM= 1
*ILXWM= 330
SCMWM= 0,CICWM= 1
*****
SLPUP= -35E6
*SLPUP= -1E12
DLYUP= 0
LIMUP= -70E3
**VTG LOOP COMPENSATER
PARAMETER VALUES
ER MPV= 120,WP MPV= 10E3
K MPV= 1
WZ MPV= 4100
VMXMPV= 10,VMNMPV= -10
*****
*WM1MPV= -80E3
*****
WM2MPV= -70
TC1MPV= 12E-3,TC2MPV= 113E-3
** CURRENT LOOP

```

```

NP CC = 1, LP CC = 1
RW CC = 10
*****
NI CC = 40
*****
** BATTERY **
TB BA = 50
NC BA = 90
IO BA = 0.22
INITIAL CONDITIONS
VC1BA = 64, VC2BA = 64
*****
PARAMETER VALUES
C1 MC2 = 1, C2 MC2 = 1, C3 MC2 = 0, C4 MC2 = 0
*****
PC PT = 1
VR PT = 105
PWOPT = 4000, SW PT = 200000
*****
PW1PT = 4000, PW2PT = 3600
*PW2PT = 2500
TC PT = 114E-3
ONLINE PLOTS
INT MODE = 4
TMAX = 4E-3, TINC = 0.05E-6
PRATE = 1E3, OTRATE = 20
DISPLAY1
VB BF, IL CH, VE MPV
DISPLAY2, VC WM, VE MPV, VI CC
SIMULATE
XIC-X
PARAMETER VALUES
*TC PT = 1E-3, TMAX = 1.999E-3
TMAX = 40E-3
PRATE = 1E3, OTRATE = 20
OTRATE = 200
*SIMULATE
*****

```

## ***B.4 Small-Signal Model of the Charger System employing Current-Mode Control***

```
*****
**** DET CHARGER SYSTEM MODEL ****
*** VTG REGULATION MODE CURRENT-MODE CONTROL
** SMALL-SIGNAL MODEL using PWM switch model
** REVISED 2/11/91
* [CMC.MOD]
*****
MODEL DESCRIPTION
***** SOLAR ARRAY *****
LOCATION = 1,SS, INPUTS = BF(VB = VO)
***** BUS FILTER CAPACITOR *****
LOCATION = 4,BF, INPUTS = SS(IO = I1),MC(S,2 = I2)
***** CHARGER *****
LOCATION = 13,SW, INPUTS = BF(VB = V1),BA(VC1 = V2),FM(DH = DH)
LOCATION = 35,FM, INPUTS = BA(VC1 = VO),SW(IL = IL),BF(VB = VG),LM(VC = VC)
LOCATION = 46,MP, INPUTS = BF(VB = VO)
***** BATTERY *****
LOCATION = 57,BA,INPUTS = SW(IL = IB)
***** LOAD *****
LOCATION = 69,SL,INPUTS = BF(VB = V1)
*****
LOCATION = 79,MC,INPUTS = SW(I1 = S,1),SL(IO = S,3)
*****
LOCATION = 54,LM,INPUTS = MP(VE = VI)
END OF MODEL
PRINT
```

```

*****
* CHARGER SMALL-SIGNAL [CMC.ANC]
** FOR CURRENT MODE CONTROL
* USING PWM SWITCH MODEL
***** 2/11/91
PARAMETER VALUES
RS SS = .05,RSHSS = 250,CD SS = .24E-6,CT SS = .063E-6
NP SS = 395, NS SS = 320
*****
NP SS = 300, NS SS = 360
*****
** CURRENT SOURCE REGION
RD SS = 87
*****
** VTG SOURCE REGION
*RD SS = 1
*RD SS = 3.6
*****
CB BF = 1E-6,RC BF = 50E-3
C BF = 2000E-6
*****
*****INPUT FILTER
*L1 FF = 10.E-6, C1 FF = 450E-6, RL1FF = 0.001
*C2 FF = 26E-6, RC1FF = 0.5
*** CHARGER POWER STAGE
PARAMETER VALUES
L SW = 50E-6
RL SW = 0.05
VBASW = 65,VBSSW = 120
*** AT HEAVY LOAD
ILSSW = 23
*** AT LIGHT LOAD
*ILSSW = 3.3
*****
RE SW = 0
*****
PW SL = 1800
VBSSL = 120
*****
*** RESISTIVE LOAD
*PW SL = -1800
*****
** BATTERY **
TB BA = 50
NC BA = 90
I0 BA = 0.22
*****
C1 MC = 1, C2 MC = 1, C3 MC = 0,C4 MC = 0
S4 MC = 0

*****
**** Q = 1 RAMP = 2 V
FM FM = 0.1978
** Q = 2
*FM FM = .228
*FM FM = .325

```

```

NN FM=0,MM FM=0
*****
** w/o ext ramp *****
*FM FM=0.333
*****
VJ FM= 1,TS FM= 11.111E-6
KF FM= -0.02195
KR FM= 0.0
RI FM= 0.25
*****
WM1MP= -340E3
WM1MP= -210E3
WM1MP= -70E3
WM2MP= -65E3
WZ MP= 18.8E3
WZ MP= 6.28E3
WZ MP= 4.2E3
WP MP= 10E3
K MP= 1, ER MP= 0
TC1MP= 1,TC2MP= 1,FLGMP= 1
*****
XX LM= 0,YY LM= 0
VJ LM= 1
*****
ONLINE PLOTS
*****
PRINT CONTROL= 3.005
TF MANUAL SCALE
FREQ MIN = 6.29
FREQ MAX = 6.28E5
*FREQ MIN = 10
*FREQ MAX = 1E6
*****
* OPEN LOOP TRANSFER FUNCTION *
*****
ALL STATES
INT CONTROL= IL SW = 1
VC SS= 1
VB BF = 1, VC BF = 1

TF INPUT = DH FM, TF OUTPUT = IL SW
TITLE = IL / D
*TRANSFER FUNCTION
TF INPUT = DH FM, TF OUTPUT = VB BF
TITLE = V / D
TRANSFER FUNCTION
*****
TF INPUT = DH FM,TF OUTPUT = I1 SW
TITLE = I1/D
*TRANSFER FUNCTION
*****
TF INPUT = S2 MC,TF OUTPUT = VB BF
TITLE = OPEN LOOP Z
*TRANSFER FUNCTION
*****
* CURRENT LOOP GAIN *

```

```

*****
PARAMETER VALUES
MM FM = -1
*****
TF INPUT = VJ FM, TF OUTPUT = HD FM
TITLE = CURRENT LOOP GAIN TI
*TRANSFER FUNCTION
*****
* CONTROL TO OUTPUT *
*****
PARAMETER VALUES
MM FM = 0, NN FM = 1
*****
TF INPUT = VC LM, TF OUTPUT = VB BF
TITLE = VB / VC
TRANSFER FUNCTION
*****
* CLOSED LOOP IMP. *
*****
PARAMETER VALUES
MM FM = 0, NN FM = 1
XX LM = 1
*****
TF INPUT = S2 MC, TF OUTPUT = VB BF
TITLE = Z out
TRANSFER FUNCTION
*****
* LOO GAIN *
*****
PARAMETER VALUES
XX LM = 0, YY LM = 1
*****
TF INPUT = VJ LM, TF OUTPUT = VE MP
TITLE = LOOP GAIN
TRANSFER FUNCTION
*****
NO STATES
INT CONTROLS
X1 MP = 1, VE MP = 1
TF INPUT = VB BF
TF OUTPUT = VE MP
TITLE = COMPENSATOR
*TRANSFER FUNCTION

```



```

*****
**** DET CHARGER SYSTEM MODEL ****
*** VTG REGULATION MODE CURRENT-MODE CONTROL
** SMALL-SIGNAL MODEL using PWM switch model
** REVISED 2/11/91 DCM
* [CMD.MOD]
*****
MODEL DESCRIPTION
***** SOLAR ARRAY *****
LOCATION = 1,SS, INPUTS = BF(VB = VO)
***** BUS FILTER CAPACITOR *****
LOCATION = 4,BF, INPUTS = SS(IO = I1),MC(S,2 = I2)
***** CHARGER *****
LOCATION = 13,DM, INPUTS = BF(VB = V1),BA(VC1 = V2),FD(DH = DH)
LOCATION = 35,FD, INPUTS = BF(VB = VG),LM(VC = VC)
LOCATION = 46,MP, INPUTS = BF(VB = VO)
***** BATTERY *****
LOCATION = 57,BA,INPUTS = DM(IL = IB)
***** LOAD *****
LOCATION = 69,SL,INPUTS = BF(VB = V1)
*****
LOCATION = 79,MC,INPUTS = DM(I1 = S,1),SL(IO = S,3)
*****
LOCATION = 54,LM,INPUTS = MP(VE = VI)
END OF MODEL
PRINT

```

```

*****
* CHARGER SMALL-SIGNAL [CMD.ANC]
* CURRENT-MODE CONTROL DCM
* USING PWM SWITCH MODEL
***** 2/11/91
PARAMETER VALUES
RS SS = .05,RSHSS = 250,CD SS = .24E-6,CT SS = .063E-6
NP SS = 395, NS SS = 320
*****
NP SS = 300, NS SS = 360
*****
** CURRENT SOURCE REGION
RD SS = 60
*****
** VTG SOURCE REGION
*RD SS = 1
*RD SS = 3.6
*****
CB BF = 1E-6,RC BF = 50E-3
C BF = 2000E-6
*****
*****INPUT FILTER
*L1 FF = 10.E-6, C1 FF = 450E-6, RL1FF = 0.001
*C2 FF = 26E-6, RC1FF = 0.5
*** CHARGER POWER STAGE
PARAMETER VALUES
L DM = 200E-6
RL DM = 0.05
VBADM = 65,VBSDM = 120
DS DM = .13
I1SDM = .1136
*****
DS DM = .54
I1SDM = 1.78
*****
PW SL = 1800
VBSSL = 120
*****
*PW SL = 1E-3
*****
** BATTERY **
TB BA = 50
NC BA = 90
I0 BA = 0.22
*****
C1 MC = 1, C2 MC = 1, C3 MC = 0,C4 MC = 0
S4 MC = 0
*****
FM FD = 0.1978
NN FD = 0,MM FD = 0
*****
** w/o ext ramp *****
*****
VJ FD = 1
KF FD = -0.02195
*****

```

```

WM1MP = -210E3
WM1MP = -95E3
WM1MP = -70E3
WM2MP = -60E3
WZ MP = 18.8E3
WZ MP = 6.28E3
WZ MP = 4.1E3
WP MP = 10E3
K MP = 1, ER MP = 0
TC1MP = 1, TC2MP = 1, FLGMP = 1
*****
XX LM = 0, YY LM = 0
VJ LM = 1
*****
ONLINE PLOTS
*****
PRINT CONTROL = 3.005
TF MANUAL SCALE
FREQ MIN = 6.29
FREQ MAX = 6.28E5
*FREQ MIN = 10
*FREQ MAX = 1E6
*****
* OPEN LOOP TRANSFER FUNCTION *
*****
ALL STATES
INT CONTROL = IL DM = 1
VC SS = 1
VB BF = 1, VC BF = 1

TF INPUT = DH FD, TF OUTPUT = IL DM
TITLE = IL / D
*TRANSFER FUNCTION
TF INPUT = DH FD, TF OUTPUT = VB BF
TITLE = V / D
TRANSFER FUNCTION
*****
TF INPUT = DH FD, TF OUTPUT = I1 DM
TITLE = I1/D
*TRANSFER FUNCTION
*****
TF INPUT = S2 MC, TF OUTPUT = VB BF
TITLE = OPEN LOOP Z
TRANSFER FUNCTION
*****
* CURRENT LOOP GAIN *
*****
PARAMETER VALUES
MM FD = -1
*****
TF INPUT = VJ FD, TF OUTPUT = HD FD
TITLE = CURRENT LOOP GAIN TI
*TRANSFER FUNCTION
*****
* CONTROL TO OUTPUT *
*****

```

```

PARAMETER VALUES
MM FD=0,NN FD= 1
*****
TF INPUT = VC LM,TF OUTPUT = VB BF
TITLE = VB / VC
TRANSFER FUNCTION
*****
* CLOSED LOOP IMP.          *
*****
PARAMETER VALUES
MM FD=0,NN FD= 1
XX LM= 1
*****
TF INPUT = S2 MC,TF OUTPUT = VB BF
TITLE = Z out
TRANSFER FUNCTION
*****
* LOO GAIN                  *
*****
PARAMETER VALUES
XX LM=0, YY LM= 1
*****
TF INPUT = VJ LM,TF OUTPUT = VD LM
TITLE = LOOP GAIN
TRANSFER FUNCTION

```

## *B.5 Large-Signal Model of the Charger System in Current Regulation Mode*

```
*****
**** DET CHARGER SYSTEM MODEL ****
** LARGE-SIGNAL MODEL
**   REVISED 3/3/90
**   FOR CHARGE CURRENT REGULATION
*****
MACRO FILE NAME = MACROS
MODEL DESCRIPTION
LOCATION = 13,PB,INPUTS = WM(IQ = IQ)
LOCATION = 23,GA,INPUTS = PB(IL = VO)
LOCATION = 33,WM,INPUTS = GA(VE = VE)
END OF MODEL
PRINT
```

```

*****
** DET CHARGER CURRENT CONTROL MODE ***
*** 3/4/90 [CUR.ANC]
*****
PARAMETER VALUES
*** CHARGER POWER STAGE
PARAMETER VALUES
L PB= 200E-6, C PB= 1500
VBAPB= 60,IG PB= 0
GA GA = .5,ER GA = 30,K GA = 1
*****
GA GA = 1
*****
ER2GA = 20,TC GA = 2E-3
INITIAL CONDITIONS
VC PB = 120
*****
PARAMETER VALUES
TI WM = 20E-6,VP WM = 5,VQ WM = -3.5
VCXWM = 15,VCNWM = -15,DMNWM = 0.01,DMXWM = .98
ONLINE PLOTS
INT MODE = 4
TMAX = 2E-3, TINC = 0.1E-6
PRATE = 1E3, OUTFRATE = 20
PARAMETER VALUES
*LLSSI = 0.1E3
DISPLAY1
IL PB,VE GA,VC WM
SI MANUAL SCALE
DISPLAY2
VR WM,XRANGE = 1.9E-3,1.999E-3
VC WM,XRANGE = 1.9E-3,1.999E-3
IL PB,XRANGE = 1.9E-3,1.999E-3
DISPLAY3(OVERPLOT)
VR WM
VC WM,XRANGE = 1.9E-3,1.999E-3
DISPLAY4
VR WM,XRANGE = 1.96E-3,2.12E-3
VC WM,XRANGE = 1.96E-3,2.12E-3
IL PB,XRANGE = 1.96E-3,2.12E-3
DISPLAY5(OVERPLOT)
VR WM
VC WM,XRANGE = 1.96E-3,2.12E-3
TMAX = 2.999E-3, TINC = 0.1E-6
PRATE = 50, OUTFRATE = 5
SIMULATE
XIC-X
PARAMETER VALUES
ER2MP = 66,TC MP = 3E-3
TMAX = 5E-3
*SIMULATE
*****

```

## B.6 Large-Signal Model of the DET system

```
*****
**** DET SPACECRAFT POWER SYSTEM MODEL ****
** LARGE-SIGNAL MODEL    REVISED 3/9/90
*****
MACRO FILE NAME = MACROS
MODEL DESCRIPTION
***** SOLAR ARRAY *****
LOCATION = 1,SI,INPUTS = BF(VB = VX)
***** BUS FILTER CAPACITOR *****
LOCATION = 4,BF,INPUTS = MC1(S,2 = I1),MC2(S,2 = I2)
***** CHARGER *****
LOCATION = 12,FF,INPUTS = CH(I1 = I2),BF(VB = V1)
LOCATION = 13,CH, INPUTS = FF(V2 = V1),BA(VC1 = VBA),WC(IQ = IQ)
LOCATION = 35,WC,INPUTS = PZ(VE = VE),MPC(VE = VI),CH(IL = IL),CU(IBC = IQC)
LOCATION = 46,PZ,INPUTS = BF(VB = VO),CU(IBC = FLG)
LOCATION = 48,MPC,INPUTS = CH(IL = VO),WC(FLG = FLG)
***** BATTERY *****
LOCATION = 57,BA,INPUTS = CH(IL = IB)
***** LOAD *****
LOCATION = 69,PT,INPUTS = BF(VB = VL)
***** SHUNT *****
LOCATION = 65,GN1,INPUTS = BF(VB = VB)
***** B/D *****
LOCATION = 47,DC,INPUTS = BF(VB = V2),BA(VC1 = V1),WY2(IQ = IQ)
LOCATION = 49,MPD,INPUTS = BF(VB = VO)
LOCATION = 58,CC2,INPUTS = DC(IL = IL)
LOCATION = 67,WY2,INPUTS = MPD(VE = VE),CC2(VI = VI),DC(IL = IL),CU(IBD = IQC)
***** CCU *****
LOCATION = 5, CU,INPUTS = BF(VB = VB),BA(VC1 = VBB)
*****
LOCATION = 77,MC1,INPUTS = SI(IO = S,1),DC(I2 = S,3)
LOCATION = 79,MC2,INPUTS = FF(I1 = S,1),PT(IL = S,3),GN1(IH = S,4)
END OF MODEL
PRINT
```

```

*****
* DET SYSTEM LARGE-SIGNAL MODEL
*           3/9/90
*           [DET.ANC]
*****
PARAMETER VALUES
LL SI = 0.6,LLXSI=1.1
LLSSI = 0.,LS2SI = 1000., TILSI = 51., LLMSI = 0.6
NP SI = 395, NS SI = 320
*INITIAL GUESS
IOISI = 32.7
CB BF = 1900E-6,RC BF = 50E-3
C BF = 100E-6
INITIAL CONDITIONS
VB BF = 118,VC BF = 118
PARAMETER VALUES
ER GN1= 122,GA GN1= 200
K GN1= 1,WP GN1= 5E4
*****INPUT FILTER
INITIAL CONDITIONS
V2 FF = 118, VC1FF = 118, I1 FF = 0
PARAMETER VALUES
L1 FF = 40.E-6, C1 FF = 450E-6, RL1FF = 0.001
C2 FF = 26E-6, RC1FF = 0.5
*** CHSIGER POWER STAGE
PARAMETER VALUES
L CH= 200E-6
RL CH=0.05
PARAMETER VALUES
TI WC = 20E-6, VP WC = 5, VQ WC = 0
VCXWC = 15, VCNWC = -15,DMNWC = 0.0,DMXWC = 1
VCXWC = 5E3,VCNWC = -5E3
ILMWC = 30
**VTG LOOP COMPENSATER
PARAMETER VALUES
ER PZ = 120,WP PZ = 314E3
WM PZ = -4959,K PZ = 1
WZ1PZ = 628
WZ2PZ = 6.28E3
** CURRENT LOOP COMPENSATOR
ER MPC = 30,WP MPC = 125.6E3
WM MPC = 4.2E3,K MPC = 1
WZ MPC = 6.28E3
VBXCU = 119.5, VBHCU = 80
VBNCU = 119
** BATTERY **
TB BA = 50
NC BA = 90
IO BA = 0.22
INITIAL CONDITIONS
VC1BA = 64, VC2BA = 64
VC DC = 118
I2 DC = 1.9,VE MPD = -2.2
***** B/D COMPONENTS *****
PARAMETER VALUES
L DC = 68E-6,RL DC = .01

```



```

LF DC = 1E-6,CF DC = 100E-6
RF DC = .052
* COMPENSATOR
K MPD = 1., ER MPD = 118
WM MPD = 1800,WP MPD = 7E3
WZ MPD = 900
**
NI CC2 = 400, RW CC2 = 35
NP CC2 = 1, LP CC2 = 1
** PWM
TI WY2 = 20E-6,VP WY2 = 3, VQ WY2 = .5
CICWY2 = 1, SCMWY2 = 0
VCXWY2 = 15, VCNWY2 = -15,ILXWY2 = 50
DMNWY2 = 0.1, DMXWY2 = 0.95
C1 MC1 = 1, C2 MC1 = 1, C3 MC1 = 0,C4 MC1 = 0
C1 MC2 = 1, C2 MC2 = 1, C3 MC2 = 1,C4 MC2 = 0
S4 MC1 = 0
*****
PC PT = 1
VR PT = 105
PWOPT = 4000,SW PT = 200000
PW1PT = 4000,PW2PT = 3000
TC PT = 120E-3
ONLINE PLOTS
INT MODE = 4
TMAX = 4E-3, TINC = 0.1E-6
PRATE = 1E3, OUTFRATE = 20
DISPLAY1
VB BF,IL CH,IH GN1,I2 DC
DISPLAY2,VB BF,VC DC,IL DC,VC WY2
SIMULATE
XIC-X
PARAMETER VALUES
LLSSI = 0.005E3
IOISI = 32.66
DISPLAY1
IO SI,VB BF,IL CH,FILSI
SI MANUAL SCALE
DISPLAY3(OVERPLOT)
IO SI,I1 FF,IH GN1,I2 DC,XRANGE = 3.3E-3,3.6E-3
DISPLAY4,VB BF,FILSI,IL CH,XRANGE = 3.3E-3,3.6E-3
DISPLAY2(OVERPLOT)
I2 DC,IH GN1,I1 FF,IL PT
DISPLAY5
VC1FF,I1 FF,IL BC,IB BB
TMAX = 100E-3, TINC = 0.1E-6
PRATE = 1E3, OUTFRATE = 1000
SIMULATE

```

## ***B.7 Large-Signal Model of the PPT system***

```
*****
**** PPT SPACECRAFT POWER SYSTEM MODEL ****
** LARGE-SIGNAL MODEL
**   REVISED 4/4/90 USING [PK]
*****
MACRO FILE NAME = MACROS
MODEL DESCRIPTION
*****
***** SOLAR ARRAY *****
LOCATION = 1,SI,INPUTS = BF(VB = VX)
***** BUS FILTER CAPACITOR *****
LOCATION = 4,BF,INPUTS = SI(IO = I1),FF(I1 = I2)
***** PEAK POWER TRACKER *****
LOCATION = 15,PK,INPUTS = SI(IO = IO),SI(PO = PO)
***** CHARGER *****
LOCATION = 12,FF,INPUTS = CH(I1 = I2),BF(VB = V1)
LOCATION = 13,CH, INPUTS = FF(V2 = V1),BA(VC1 = VBA),WC(IQ = IQ)
LOCATION = 35,WC,INPUTS = PZ(VE = VE),MPC(VE = VI),MC2(S,2 = IL)
LOCATION = 46,PZ,INPUTS = BF(VB = VO),PK(VRF = ER)
LOCATION = 48,MPC,INPUTS = MC2(S,2 = VO),WC(FLG = FLG)
***** BATTERY *****
LOCATION = 57,BA,INPUTS = MC2(S,2 = IB)
***** LOAD *****
LOCATION = 69,PT,INPUTS = BA(VC2 = VL)
*****
LOCATION = 79,MC2,INPUTS = CH(IL = S,1),PT(IL = S,3)
END OF MODEL
PRINT
```

```

*****
** PEAK POWER TRACKING SYSTEM
**           [PKT.ANC]
*** 4/3/90
PARAMETER VALUES
LL SI = 0.6
LLSSI = 0.,LS2SI = 1000., TILSI = 4E-3, LLMSI = 0.6
NP SI = 295, NS SI = 320
NP SI = 395
*INITIAL GUESS
IOISI = 26.55
LLXSI=1
LLSSI=0.
*****
CB BF = 1900E-6,RC BF = 50E-3
C BF = 100E-6
INITIAL CONDITIONS
VB BF = 136,VC BF = 136
*****
PARAMETER VALUES
VRIPK = 137.4
TI PK = .5E-3
DPMPK = 100,DRFPK = .1
*****
*****INPUT FILTER
INITIAL CONDITIONS
V2 FF = 136, VC1FF = 136, I1 FF = 31
IL CH = 45
PARAMETER VALUES
L1 FF = 40.E-6, C1 FF = 450E-6, RL1FF = 0.001
C2 FF = 26E-6, RC1FF = 0.5
*** CHSIGER POWER STAGE
PARAMETER VALUES
L CH = 200E-6
RL CH = 0.05
*****
PARAMETER VALUES
*****
TI WC = 20E-6, VP WC = 5, VQ WC = 0
VCXWC = 15, VCNWC = -15,DMNWC = 0.1,DMXWC = 0.9
VCXWC = 5E3,VCNWC = -5E3
ILMWC = 30
*****
**VTG LOOP COMPENSATER
PARAMETER VALUES
WP PZ = 314E3
WM PZ = -4959,K PZ = 1
WZ1PZ = 628
WZ2PZ = 6.28E3
WM PZ = -4000
** CURRENT LOOP COMPENSATOR
ER MPC = 3,WP MPC = 125.6E3
WM MPC = 4.2E3,K MPC = 1
WZ MPC = 6.28E3
*****
** BATTERY **

```

```

TB BA = 50
NC BA = 90
IO BA = 0.22
INITIAL CONDITIONS
VC1BA = 64, VC2BA = 64
PARAMETER VALUES
C1 MC2= 1, C2 MC2= -1, C3 MC2= 0,C4 MC2= 0
*****
PC PT = 1
VR PT = 50
PWOPT = 3000, SW PT = 200000
PW1PT = 3000, PW2PT = 3000
*PW1PT = 1000
TC PT = 120
ONLINE PLOTS
INT MODE = 4
DISPLAY1
VB BF, IO SI
*, PO SI
DISPLAY2
IO SI, IL CH, IL PT, S2 MC2
*DISPLAY3
*VRFPK, DLIPK, DLPPK, DPIP K
*DISPLAY4
*(VE PZ, VC WC, VB BF, PO SI
*SI MANUAL SCALE
*DISPLAY5
*VR WC, XRANGE = 7.75E-3, 7.999E-3
*VC WC, XRANGE = 7.75E-3, 7.999E-3
*VRFPK, XRANGE = 7.75E-3, 7.999E-3
*IL CH, XRANGE = 7.75E-3, 7.999E-3
TMAX = 29.999E-3, TINC = 0.1E-6
TMAX = 2E-3
PRATE = 500, OUTFRATE = 200
*SIMULATE
*XIC-X
PARAMETER VALUES
LLSSI = 0.0005E3
DPMPK = 10
*IOISI = 31.1, VRIPK = 137.4
DISPLAY2(OVERPLOT)
IO SI, IL PT, IL CH, S2 MC2
TMAX = 200E-3, TINC = 0.1E-6
PRATE = 2E3, OUTFRATE = 1000
*TMAX = 10E-3, OUTFRATE = 40
SIMULATE

```

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## Vita

Seong Joong Kim was born in Seoul, Korea on October 12, 1953. He received the B.S. and M.S. degree both in electrical engineering from Seoul National University, in 1976 and 1978, respectively. From 1978 to 1983, he worked in Agency for Defense Development of Korea as a research engineer. His experiences include hybrid simulation for missile and remotely piloted vehicle.

He began studying at Virginia Polytechnic Institute and State University in the fall of 1983, and received M.S. degree in Electrical Engineering in 1986, concentrating on the modeling and analysis of switching regulators. Since 1986, he has been graduate research assistant of the Virginia Power Electronic Center (VPEC). He is actively involved in power electronics research in the areas of spacecraft power systems, computer-aided design and analysis of switching regulators.

He and Hyun-sook Sohn were married in 1980 and they have two daughters, Soo-kyung and Ji-yoon.

A handwritten signature in black ink that reads "Seong J Kim". The signature is written in a cursive, flowing style.