NOVEL CONCEPTS IN HIGH-FREQUENCY RESONANT POWER PROCESSING

by

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APPROVED:

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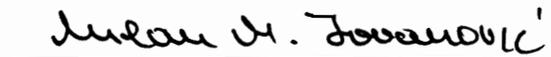
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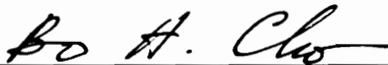
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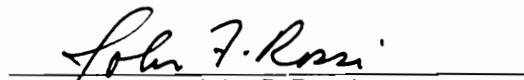
John F. Rossi

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(ABSTRACT)

Two new power conversion techniques, the constant-frequency zero-voltage-switching multi-resonant-converter (CF ZVS-MRC) technique and the zero-voltage-switching technique that uses the magnetizing inductance of the power transformer as a resonant element (ZVS (L_M)) are proposed, analyzed. and evaluated for high-frequency applications. In addition, a novel design optimization approach for resonant type converters is introduced.

Complete dc analysis of CF forward and half-bridge (HB) ZVS-MRCs are given, and the dc voltage-conversion-ratio characteristics for each of these two converters are derived. Graphic design procedures that maximize the efficiency and minimize current and voltage stresses are established. The design guidelines are verified on a 50 W CF forward ZVS-MRC operating with a switching frequency above 2 MHz, and on a 100 W HB ZVS-MRc operating with a switching frequency of 750 kHz.

The ZVS (L_M) technique is developed to eliminate the need for a large, inefficient external resonant inductor in ZVS resonant converters. This new family of isolated converters can operate with zero-voltage-switching of the primary active switches only (quasi-resonant (QR) operation) or with soft-switching of all semiconductor devices (multi-resonant (MR) operation). Furthermore. variable and constant frequency operation of all topologies in this new family of dc/dc converters are possible.

A complete dc analysis of the HB ZVS-MRC (L_M) is given, and the dc voltage-conversion-ratio characteristics are derived. Design guidelines are defined using the same graphic method

employed in the design of CF ZVS-MRCs. Constant frequency implementation of the HB ZVS-MRC (L_M) using controllable saturable inductors is also proposed.

Finally, a novel approach to evaluate and design resonant converters based on the minimization of reactive power is developed.

To my grandmother, Marta Calleros de Azmitia, and

the memory of my grandfather, Enrique Azmitia Toriello.

Acknowledgements

I would like to express my sincere appreciation to both, Professor Fred C. Lee and Dr. Milan M. Jovanović, for their patience, guidance, and support during my doctoral studies. Much of this work would not have been possible without their encouragement and belief in me.

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1. INTRODUCTION

The advancement of Very Large Scale Integration (VLSI) technology continues to reduce the size and increase the speed of information processing systems. At the same time, power demands of the VLSI systems continue to increase due to higher densities of data processing systems. However, the size reduction of power supplies has not kept the same pace. This trend has prompted the research and development of efficient electric power conditioners having high power densities and fast transient response operating with conversion frequencies in the megahertz range.

Generally, when the conversion frequency of conventional Pulse-Width-Modulated (PWM) supplies nears 1 MHz, the switching loss becomes excessive due to the presence of a high current and a high voltage during turn-on and turn-off phase of the power switch. Circuit parasitics, such as transformer leakage inductance, semiconductor junction capacitances, and rectifier reverse recovery are among the major factors that hinder the operation of "hard switched" PWM converters at higher switching frequencies.

Recent developments in high-frequency power conversion have shown an increased utilization of parasitic components. Several innovative techniques have been proposed to operate the active switch with zero-voltage turn-on or zero-current turn-off in order to minimize switching losses, stresses, and noises. Generally, these techniques can be classified in two groups: **resonant techniques** and **pulse-width-modulated** (PWM) techniques with **zero-voltage-switching** (ZVS) or **zero-current-switching** (ZCS) [A1-A27], [B1-B36]. The ZVS concept has also been extended to include both active and passive switches [C1-C20], [D1-D15]. The resulting multi-resonant converters (MRCs) and class-E converters with resonant rectifiers utilize the transformer leakage inductance and transistor and rectifier junction capacitances to form a multi-component resonant network to obtain ZVS of all semiconductor components.

Two major **disadvantages** of resonant type converters are **variable frequency** operation and increased **current and/or voltage stresses** of all semiconductor components. Normally, ZVS converters require constant off-time variable frequency control, while ZCS converters require constant on-time variable frequency control. For converters operating with a wide input voltage and load range, the frequency range is also broad. As result, an optimum design of the magnetic components (inductors and transformers) and EMI and output filters is difficult to achieve. In addition, the bandwidth of a closed-loop control is compromised since it is determined by the minimum switching frequency. It would be desirable to operate the converters at a constant frequency to derive a greater benefit from high-frequency operation.

Several **constant-frequency** (CF) resonant converters operating under zero-voltage or zero-current switching have been proposed [E1-E31]. A class-E converter operating at approximately 1.5 MHz was described in [E2]. The class-E approach was later modified to attain even higher switching frequencies [C6,C7]. Buck and flyback CF PWM converters which use zero-voltage-resonant transition are described in [E13], while a ZVS full-bridge (FB) PWM converter

using phase shift control is discussed in [E7,E13]. The clamp-mode series-resonant converter is introduced in [E8], and the buck zero-current-switched quasi-resonant converters (ZCS-QRCs) operating at constant frequency are discussed in [E9]. The constant frequency implementation of resonant converters simplifies the design of the magnetic components and reduces the switching interference spectrum to a single frequency.

An additional disadvantage of the ZVS quasi-resonant (QR) and multi-resonant (MR) family of converters is that they require a **relatively large resonant inductor** to achieve ZVS over a wide load range. The resonant inductor is subjected to high resonant currents and voltages which have detrimental effects on the overall efficiency and size of ZVS-QRCs and ZVS-MRCs. In isolated ZVS-QRC and ZVS-MRC topologies, the resonant inductor is connected in series with the primary winding of the power transformer [B19-B39],[D1-D15]. However, the magnetizing inductance cannot be used as a resonant element in these topologies. For example, in the half-bridge ZVS-QRC, the primary windings of the transformer is shorted during the resonant stage due to the simultaneous conduction of output rectifiers. This makes it impossible to use the magnetizing inductance as a resonant element to achieve ZVS [D8]. To use the magnetizing inductance as the resonant inductor, it is necessary to open the secondary side of the transformer during the resonant interval instead of shorting it. With the secondary of the transformer open, the magnetizing inductance appears in series with the capacitance of the primary switches, thus forming the necessary resonant circuit needed for ZVS [F1-F3].

Recent developments have shown several converters operating with ZVS by utilizing the magnetizing inductance to discharge the switch capacitances [E18,F1-F7]. A ZVS forward converter utilizing the magnetizing inductance of the power transformer as a resonant ele-

ment is described in [E18,F3,F7]. Similar utilization of the magnetizing inductance as a resonant component for the full-bridge (FB) and half-bridge (HB) topologies is described in [F3-F5]].

This work introduces two new families of ZVS converters: the **CF ZVS-MR family** and the **family of isolated ZVS converters which uses the magnetizing inductance of the power transformer as a resonant element.** A systematic approach to generating these two new families is discussed in detail. Furthermore, the operation of the forward and HB topologies are analyzed by neglecting all major losses in the converters. Design procedures for these two topologies are determined from the idealized analysis. The advantages and disadvantages of these new families of converters are discussed relative to other soft switching resonant techniques.

The **family of ZVS-MRC operating at constant frequency** is generated by replacing the passive switch in the multi-resonant switch with an active switch [E1,E5,E6,E20,E24]. Several experimental CF ZVS-MRC circuits have been reported so far [E1,E5,E6,E20]. The CF buck converter is described in [E1,E5], the HB converter in [E5,E20], and the Cuk converter in [E6]. An introductory, generalized analysis of CF ZVS-MRCs is presented in [B35]. The analysis was developed primarily for nonisolated topologies, but it can be applied to isolated topologies if the magnetizing current of the transformer is neglected. However, the analysis is not directly applicable to the CF forward ZVS-MRC since the magnetizing current plays an important role in its operation [D3,D7,D12]. Also, the analysis cannot be directly applied to off-line (bridge-type and push-pull) ZVS-MRCs due to the inherent clamping of the resonant-voltage waveform of the primary switches [D6,D8-D10]. In this work the complete analysis of the CF forward and HB ZVS-MRCs is presented.

The **family of ZVS converters which utilizes the magnetizing inductance of the power transformer** is generated by operating isolated PWM converters with constant off-time variable on-time control (variable switching frequency) and allowing for the resonance between the magnetizing inductance and the capacitance in parallel with the power switch(es). In order to insure the resonance of the magnetizing inductance during the complete resonant transition, a mechanism that opens the secondary windings of the power transformer during this interval is needed. The magnetizing inductance then becomes a resonant element, forming a resonant network with the capacitances across each of the power switches. Depending on the mechanism used to open the secondary winding of the power transformer during the resonant interval, this family of converters can also operate with constant switching frequency. This concept is further extended to obtain soft turn-off of the output rectifiers,resulting in operation similar to that of ZVS-MRCs. Like the ZVS-MRCs, all of the major circuit parasitics are absorbed by the resonant network.

1.1 Objectives of the Research

The need for high-frequency, high-density, low cost, reliable, and expendable modular power supplies compatible with logic cards has motivated the following studies:

a) Development of CF ZVS-MRCs:

- Comprehensive analysis of the CF forward and HB ZVS-MR topologies.

- Definition of a systematic and complete design procedure for the CF ZVS-MRCs.

- Assessment of merits and limitations of CF ZVS-MRCs high-frequency operation.

b) Development of isolated ZVS (L_M) converters:

- Development of a new family of ZVS converters which uses the magnetizing inductance of the power transformer as a resonant element.

- Comprehensive analysis of the ZVS forward and HB topologies.

- Definition of a systematic and complete design procedure for the HB ZVS converter that uses the magnetizing inductance as a resonant element.

- Assessment of merits and limitations of ZVS converters that use the magnetizing inductance as a resonant element suitable for high-frequency power conversion.

c) Assessment of various resonant power processing techniques:

- Development of an analysis of circulating power to asses the efficiency of different power processing techniques.

- Comparison of the new families of ZVS converters with existing ZVS and ZCS resonant converters.

- Definition of design guidelines to minimize the circulating power flowing through resonant converters (maximize power stage efficiency).

1.2 Methods of Approach

By neglecting the higher order effects, the operation of isolated ZVS converters can be modeled as a sequence of equivalent circuits, each corresponding to a specific switching interval during a switching cycle. State equations and the boundary condition of each stage can be determined and matched to describe the steady-state behavior and to derive the dc voltage-conversion-ratio characteristics.

From the dc characteristics, given a switching frequency or switching frequency range of operation, design procedures for ZVS converters which assume minimum stress on the semiconductor switches and maximum efficiency of the power stage are proposed. Also, design techniques for isolated driver stages are described for both families of converters. A mag-amp type control is proposed for constant frequency implementation of ZVS-MRCs (L_M).

Using an energy transfer analysis, ZVS topologies are evaluated. The region of their most suitable application is determined taking into account the maximum conversion frequency, input voltage range, load range, circulating energy, relative efficiency, and expected power density.

1.3 Major Results

For the two high-frequency techniques considered in this work, the major results can be summarized as follows:

CF ZVS-MRCs:

(1) The family of ZVS-MRCs operating at a constant switching frequency was proposed.

(2) Simple rules for generating CF ZVS-MRCs from corresponding PWM converters were defined.

(3) A comprehensive dc analysis of the forward and HB CF ZVS-MRCs was performed.

(4) DC voltage-conversion-ratio characteristics were calculated.

(5) Design procedures for the CF forward and HB ZVS-MR topologies, which used the computed dc characteristics, were defined.

(6) The designs were verified experimentally by building a 50 W CF forward ZVS-MRC operating at a switching frequency above 1 MHz and a 100 W CF HB ZVS-MRC switching at approximately 700 KHz.

ZVS (L_M) converters:

(1) A new family of ZVS converters that uses the magnetizing inductance as a resonant component was proposed (ZVS (L_M). The converters can operate with variable or constant switching frequency.

(2) Rules for generating this new family of converters from their PWM counterparts were defined.

(3) The ZVS (L_M) technique was expanded to allow for soft switching operation of the rectifier circuit (ZVS-MRC (L_M)).

(4) A dc analysis of the HB ZVS-MRC (L_M) was performed.

(5) DC voltage-conversion-ratio characteristics for the HB ZVS-MRC (L_M) were calculated.

(6) A design procedure for the HB topology that maximizes power stage efficiency was given. The procedure was verified experimentally by the construction of a 100 W converter operating with a minimum switching frequency of 250 kHz.

(8) Constant frequency operation of the HB ZVS-MRC (L_M) was verified experimentally.

Assessment of resonant techniques:

(1) A reactive power analysis to asses different power processing techniques was developed.

(2) Characteristics measuring the reactive power processed by different resonant techniques were determined for the bridge-type topologies.

(3) A number of resonant converters were optimized based on reactive power minimization.

1.4 Outline of Dissertation

This dissertation is divided into three major parts. The first part of the dissertation, Chapters 2 and 3 discuss CF ZVS-MRCs. The principle of operation of CF ZVS-MRCs is presented in

Chapter 2 and a complete dc analysis of the forward and HB topologies are discussed in Chapter 3.

Chapters 4 and 5 introduce the new family of converters that use the magnetizing inductance of the transformer as a resonant element. Chapter 4 discusses the principle of operation of this new family of converters. A detail dc analysis of the HB topology ZVS-MRC (L_M) is presented in Chapter 5.

In Chapter 6, the analysis of reactive power in a number of resonant converter is presented. The analysis is used to define design procedures that maximize the efficiency of the converters.

Finally, conclusions and suggestions for future work are given in Chapter 7.

2. CONSTANT FREQUENCY ZVS-MRCs

2.1 Introduction

This chapter presents the basic principle of operation of the constant frequency (CF) zero-voltage-switched (ZVS) multi-resonant (MR) family of converters. The operation of the conventional buck ZVS-MRC is presented to show how ZVS-MRCs can be operated under constant frequency. Like the conventional ZVS-MRCs, the CF ZVS-MRCs operate with zero voltage switching of all semiconductor devices, power switches and rectifier diodes [E1,E5,E6,E20].

The new family of CF ZVS-MRCs is generated using a systematic approach based on the CF zero-voltage multi-resonant switch concept. The CF ZVS-MRC implementation of the six basic topologies (buck, boost, buck-boost, zeta, sepic, and cuk) are discussed in this chapter. In

addition, implementation of the basic isolated topologies is also shown and topological variations for the forward and the HB converters are discussed in detail.

2.2 Principle of Operation of the Buck ZVS-MRC

The conventional buck ZVS-MRC is shown in Fig. 2.1. The resonant components in this converter are the capacitances across the active switch, C_S, the capacitance in parallel with the secondary windings of the power transformer, C_D, and the resonant inductor, L. To simplify the discussion of the operation of the buck ZVS-MRC and how its operation results in variable frequency control, it will be assumed that the load and output filter can be replaced by a constant current source and that the semiconductor devices are ideal (switching and conduction losses are neglected). The operation of the buck ZVS-MRC can be characterized by the sequence of the topological stages the converter follows during one switching cycle. The different topological stages result from the possible on/off state of the two semiconductor switches (switch S_1 and rectifier diode D). The waveforms corresponding to the operation of this converter are shown by the solid lines of Fig. 2.2. In addition, the topological sequence the buck ZVS-MRC goes through one switching cycle is shown in Fig. 2.3.

Following the topological sequence shown in Fig. 2.3, prior to time T_O, switch S_1 is on and the resonant inductor current increases in a resonant fashion since capacitance C_D resonates with L. At time T_O, switch S_1 is turned off and the voltage across this switch increases in a resonant manner due to the interaction of capacitances C_S and C_D with the resonant inductor.
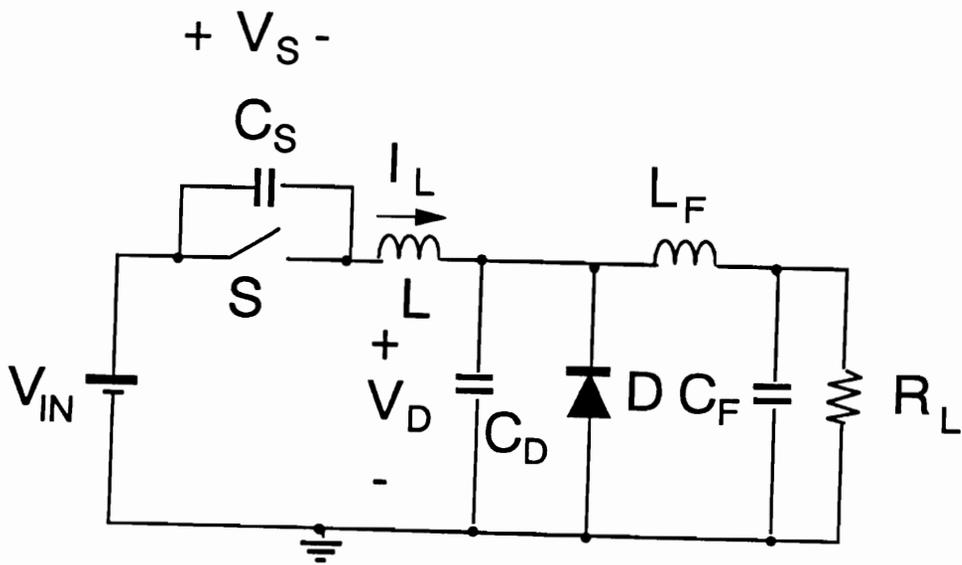
Figure 2.1. Buck zero-voltage-switched (ZVS) multi-resonant-converter (MRC).
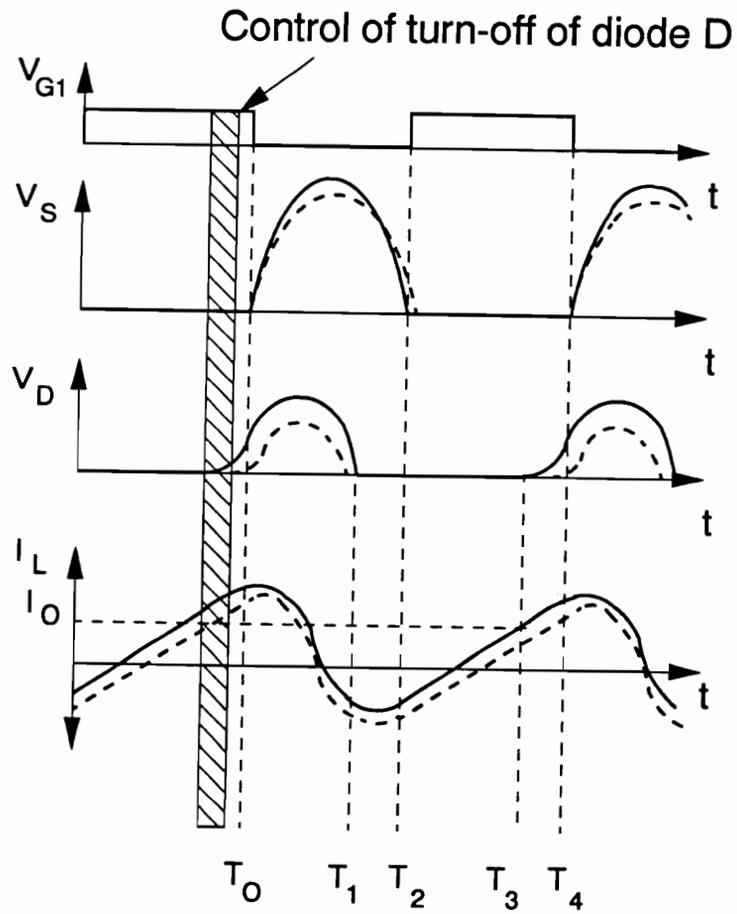
Figure 2.2. Typical waveforms of the buck ZVS-MRC (solid lines) and the constant frequency implementation of the buck ZVS-MRC (dotted lines). From top to bottom: gate-source voltage of switch S_1, V_{G1}, drain-source voltage of switch S_1, V_S, capacitor voltage, V_D, and resonant inductor current, I_L.
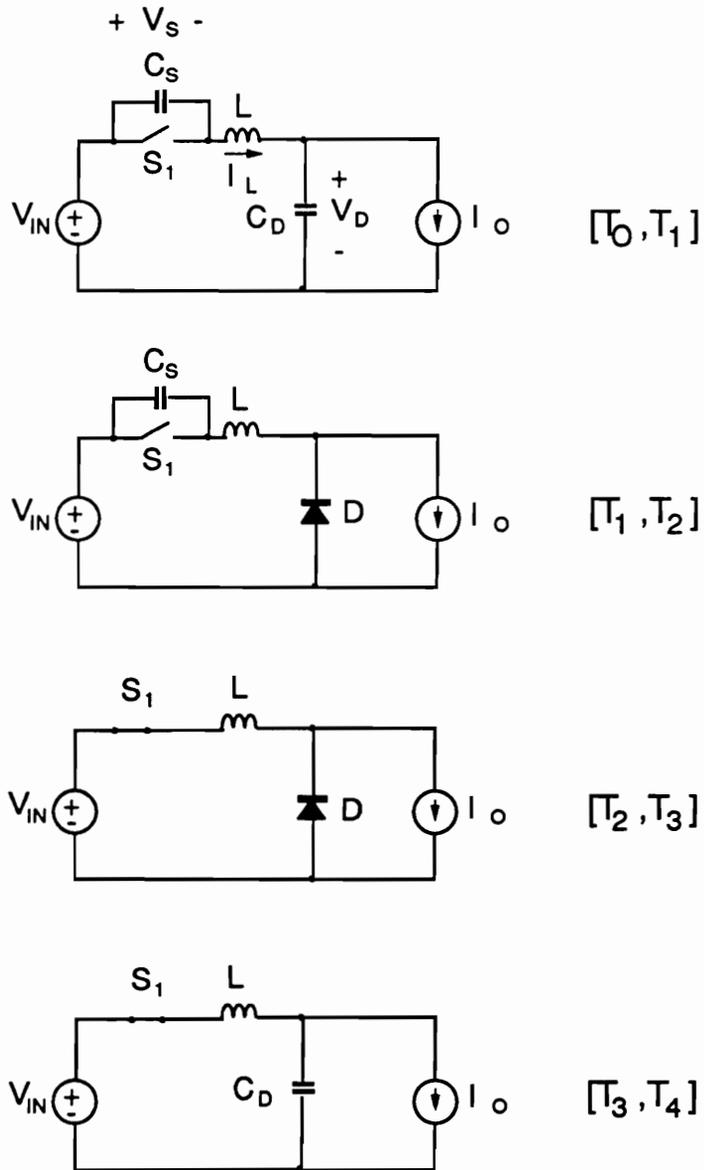
Figure 2.3. Topological stage sequence for the buck ZVS-MRC.

At time T_1, the voltage across the rectifier diode becomes forward biased. During the time interval $T_1 - T_2$, the resonant inductor resonates with capacitance C_S in a manner that forces the voltage across this capacitance to return to zero at time T_2. Since the resonant inductor current is less than zero at time T_2, the antiparallel diode of switch S_1 will conduct. Zero voltage turn-on of switch S_1 is possible during the interval between time T_2 and the time the resonant inductor current becomes positive (conduction interval of the antiparallel diode of switch S_1). From time $T_2 - T_3$, switch S_1 and diode D conduct, and the resonant inductor current increases linearly. At time T_3, the value of the resonant inductor current increases to the value of the load current turning the freewheeling diode off. As the resonant inductor current continues to increase above the value of the load current, the difference between the resonant inductor and load currents charges capacitor C_D, giving rise to the fourth topological stage. In this last topological stage, $T_3 - T_4$, switch S_1 is conducting and the resonant inductor resonates with capacitance C_D. This stage ends when switch S_1 is turned off initiating a new switching cycle. From the operation of this converter it can be concluded that power is transferred during the first and last topological stages and the second and third stages correspond to the freewheeling stages. The turn-off time of the freewheeling diode is determined from the converter operation. Therefore, there is no way of controlling the duration of the power transferring stages (time duration determined by the natural operation of the converter), and variable frequency control is needed to regulate the output terminal of this converter and all other ZVS-MRCs.

From the basic operation of the buck ZVS-MRC, it can be inferred that constant frequency operation of this converter is possible if the time at which the last stage begins can be controlled; i.e., controlling the duration of the power transferring stages. In the conventional buck ZVS-MRC the last stage begins when the resonant inductor current increases to the value of

the load current and diode D is commutated off naturally. It is possible to control the time at which the freewheeling stage ends by replacing diode D by a second active switch, S_2, resulting in operation of the converter as depicted by the dotted lines of Fig. 2.2. When the resonant inductor current increases to the value of the load current, switch S_2 does not turn off and the difference between the resonant inductor and load currents is returned to the source. By adding switch S_2 across the input of the output filter, the duration time during which power is transferred to the load can be easily controlled using CF operation. The idea of controlling ZVS-MRCs under constant switching frequency can be generalized for all topologies by introducing the concept of the CF MR switch.

2.3 CF Zero-Voltage Multi-Resonant Switch

The ZVS-QRC and ZVS-MRC families have been derived from the PWM converter family by replacing the PWM switch with the quasi-resonant (QR) switch and multi-resonant (MR) switch shown in Fig. 2.4(a) and 2.4(b), respectively [B25,B26]. In a similar manner, by replacing the PWM switch with the CF multi-resonant switch in Fig. 2.4(c), the family of CF ZVS-MRC is generated [E5].

It should be noted that both the quasi-resonant switch and multi-resonant switch use a combination of active and passive switches. As a result, no direct control of the power flow through the passive switch is possible. The power delivered from the source to the load is determined by the duration of the on-time (i.e., the duration for which the source is connected
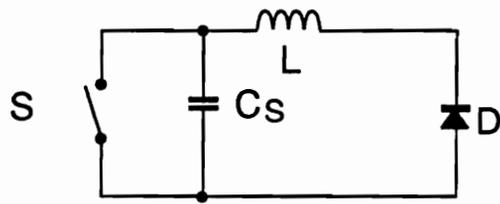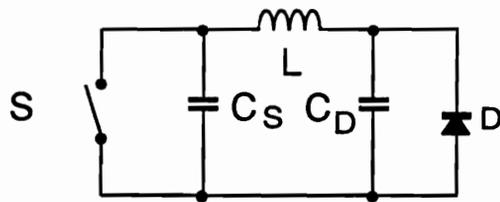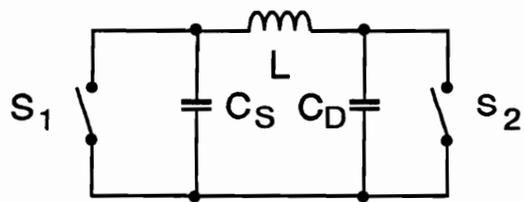
Figure 2.4.   Resonant switches:
(a) zero-voltage QR switch,
(b) zero-voltage MR switch, and
(c) zero-voltage CF MR switch.

to the output). To control the output power flow in ZVS-QRCs, it is necessary to vary the switching frequency by varying the on-time while the off-time is maintained constant (constant off-time control).

The single active switch, S, in ZVS-QRCs and ZVS-MRCs controls the power flow from the source to the load, but there is no way of returning any excess energy back to the source. The loss of control of the power flow from the load to the source is related to the loss of freedom that results from operating with ZVS. By operating with soft switching, the time at which the rectifier diode (passive switch) turns on/off is determined by the zero-voltage condition which depends on the operation of the converter and cannot be arbitrarily set. In order to regain the lost degree of freedom, the passive switch can be replaced by a second active switch as shown in Fig. 2.4(c). The second active switch is used to control the flow of energy from the load to the source. Constant-frequency operation is now possible, since any excess energy that is transferred to the rectifier circuit can be returned to the load by simply modulating the pulse width of the on-time of the second active switch. Switch S_1 is operated with CF and constant duty cycle, where the off time is determined by the ZVS condition.

The CF buck ZVS-MRC is obtained by replacing the PWM switch in the buck PWM converter with the CF MR switch as shown in Fig. 2.5. In other words, simply replace the freewheeling diode by an active switch as suggested in the first section of this chapter. The detailed analysis of the operation of the CF buck ZVS-MRC shows how a second active switch can be used to control ZVS-MRCs at a constant switching frequency. It is important to notice that in ZVS converters the active switches are generally replaced by MOSFET switches. MOSFETs are selected as the active device because a voltage unidirectional switch is needed for ZVS. To switch under zero voltage conditions, the antiparallel diode of switch S_1 and S_2 naturally conducts prior to turn-on, clamping the switch voltage to zero. Therefore, when the switch

finally turns on, the voltage supported by the switch is zero, resulting in lossless turn-on. Throughout this work it will be understood that when referring to a switch that operates with ZVS, the physical switch will have an antiparallel diode, either an inherent antiparallel diode such as MOSFET devices, or an externally added antiparallel diode.

2.4 Operation of CF Buck ZVS-MRC

For ease of explanation, it is assumed that the inductance of the output filter is large and in steady-state the output filter can be approximated by a constant current source with a value equal to the load current, and that all semiconductor devices are ideal. The different topological stages of the CF buck ZVS-MRC are shown in Fig. 2.6 and the typical waveforms of the operation of this converter are shown in Fig. 2.7. The operation of the CF buck ZVS-MRC can be summarized in the following manner:

Stage A $[T_O, T_1]$, Fig. 2.6(a)

Previous to time T_O, switch S_1 and S_2 are on and the inductor current increases linearly while the load current freewheels through switch S_2. Stage A begins when switch S_1 is turned off and the current that was flowing through the switch is diverted into the resonant capacitor C_S. Switch S_2 remains off and the voltage across switch S_1 increases in a resonant manner as capacitances C_D and C_S resonate with inductance L. This stage ends when the voltage
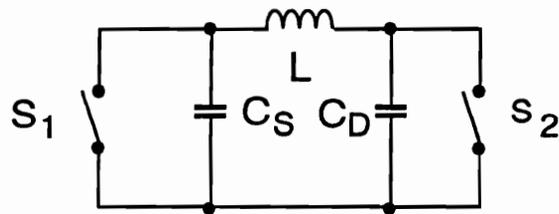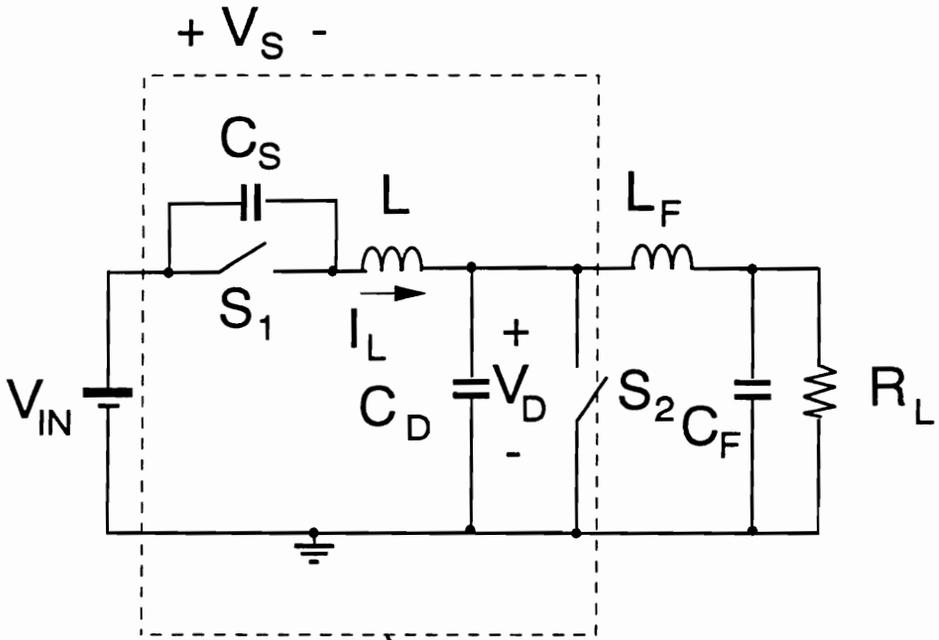
Figure 2.5. Constant Frequency (CF) buck zero-voltage-switched (ZVS) multi-resonant-converter (MRC). Dotted region shows the CF MR switch.
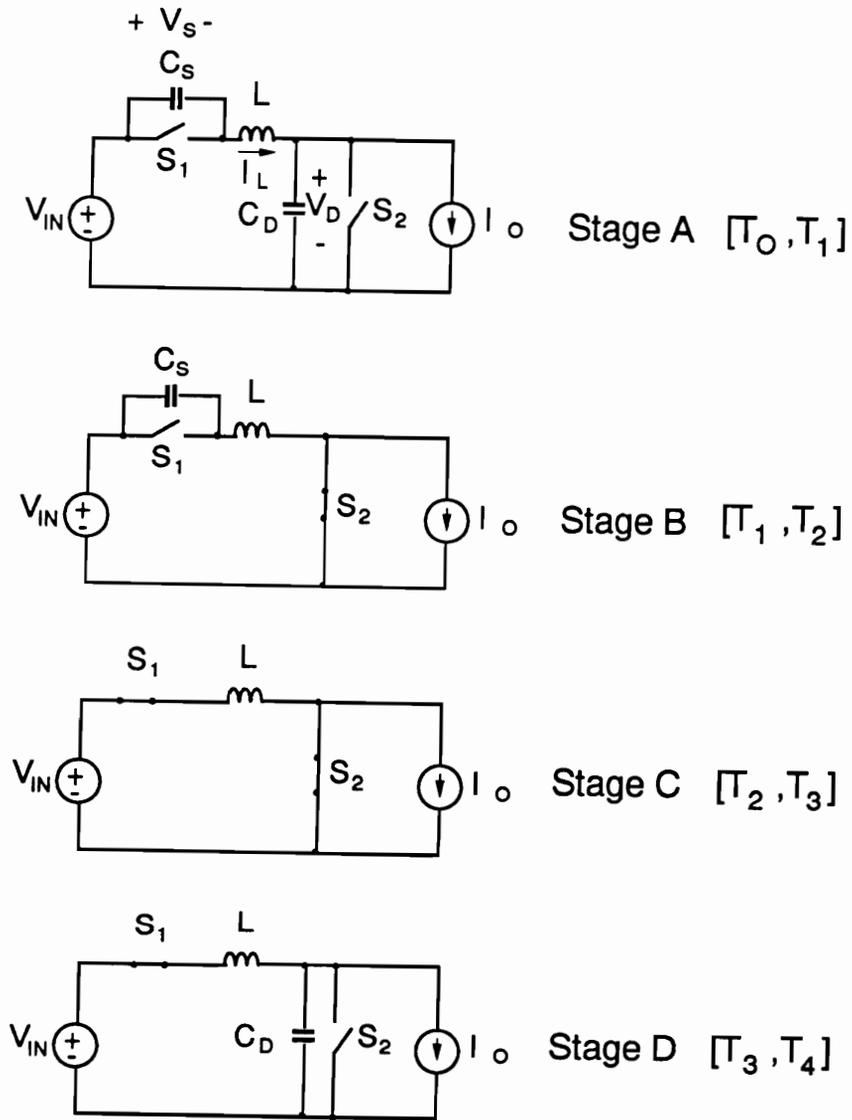
Figure 2.6.   Topological stage sequence of the CF buck ZVS-MRC.

Switch S₂ conducts

Switch S $_2$ conducts

V_{G2}

V_{G1}

V_S

V_D

I_L

I_O

T_0 T_1 T_2 T_3 T_4

t

Antiparallel diode
of switch S $_2$ conducts
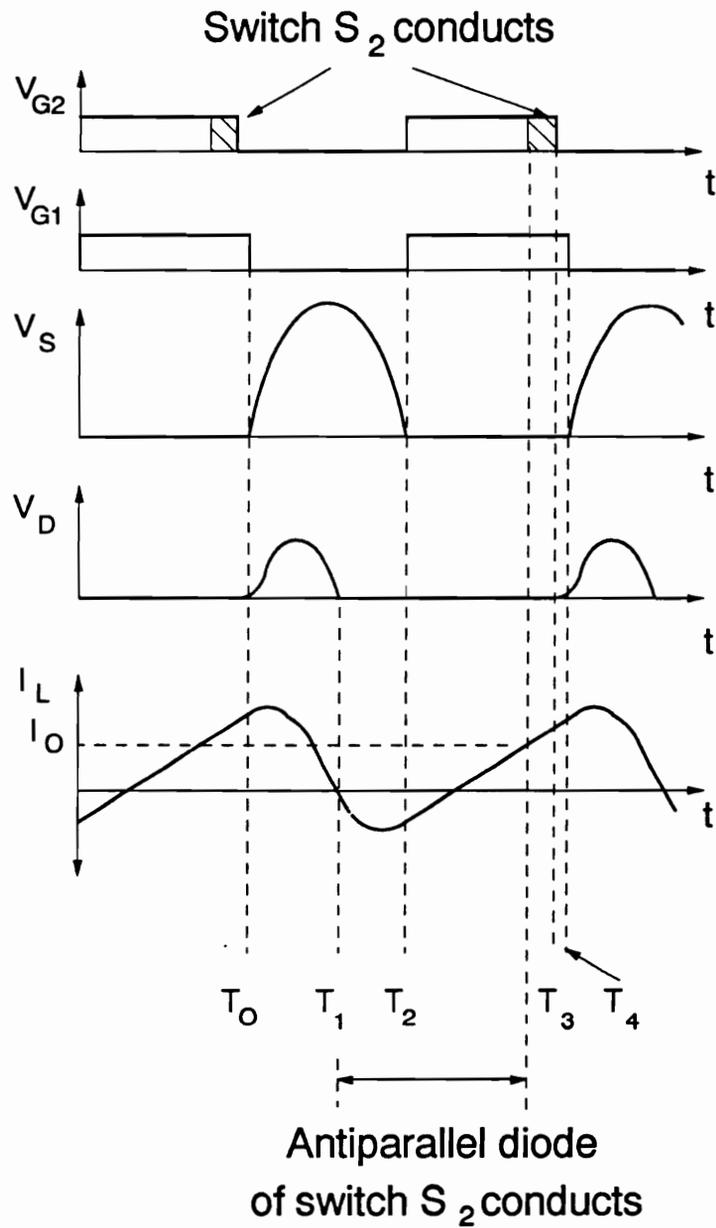
Figure 2.7.   Typical waveforms of the CF buck ZVS-MRC, from top to bottom: gate-source voltage
of switch S_2, V_{G2}, gate-source voltage of switch S_1, V_{G1}, drain-source voltage of switch
S_1,V_S, capacitor voltage V_D, and resonant inductor current I_L.

across switch S_2, V_D, discharges to zero at time T_1. Since current I_L is less than the load current at time T_1, switch S_2 naturally turns on as its antiparallel diode conducts.

Stage B [T_1, T_2], Fig. 2.6(b)

At time T_1, switch S_2 is on and capacitance C_S resonates with resonant inductor L. During this stage no energy is transferred to the load. This stage ends when the voltage across switch S_1 resonates back to zero at time T_2. Since the resonant inductor current is less than zero at time T_2, the antiparallel diode of switch S_1 will conduct. Switch S_1 can be turned on under zero voltage as long as its antiparallel diode is conducting.

Stage C [T_2, T_3], Fig. 2.6(c)

In this stage current through inductor L increases in a linear manner. Switch S_2 is on and no power is transferred to the load during this stage. During this stage the current through inductor L increases above the load current and switch S_2 will conduct (the current is commutated from the antiparallel diode of switch S_2 to switch S_2). Stage C ends when switch S_2 is turned off at time T_3

Stage B [T_3, T_4], Fig. 2.6(d)

Switch S_1 is on and switch S_2 is off. Capacitance C_D charges in a resonant manner through inductor L. Since switch S_2 is off during this stage, power is transferred to the load. This stage ends at time T_4 when switch S_1 is turned off and a new switching cycle begins.

Since power is transferred to the load only during the off-time of switch S_2, the output voltage of this converter can easily be regulated by controlling the on-time of this switch without having to vary the switching frequency. This second active switch is referred to as the constant-frequency (CF) switch. Using this technique, soft switching of all semiconductor devices is achieved at a constant switching frequency.

Due to the multiple resonance present in CF MRCs, normal operation of these converters results in more than one mode of operation where each mode corresponds to a different topological stage sequence. The complete dc analysis of the CF buck ZVS-MRC is presented in [E1] (operation of the CF buck ZVS-MRC results in four different modes).

2.5 Basic Constant-Frequency Multi-Resonant Topologies

The family of CF ZVS-MRCs is obtained by replacing the PWM switch in corresponding PWM converters with the CF MR switch discussed in Section 2.2. Alternatively, the CF ZVS-MR family of converters can also be generated from conventional PWM converters using the following rules:

(1) replace the rectifier diode with an active switch

(antiparallel diode is needed for operation with ZVS),

(2) place capacitance C_S in parallel with switch S_1,

(3) place capacitance C_D in parallel with switch S_2, and

(4) insert resonant inductor L in the loop containing switch S_1 and S_2.

The six basic CF ZVS-MRC topologies (buck, boost, buck-boost, zeta, sepic, and cuk) are shown in Fig. 2.8. The principle of operation of the basic topologies is similar to the one described for the buck topology. Zero-voltage-switching for S_1 and S_2 is achieved by allowing the resonance of the capacitors in parallel with the switches and the resonant inductor L. Switch S_1 is operated with constant switching frequency and constant duty cycle where the off time of the switching signal is determined by the ZVS condition of the switch. Switch S_2 controls the amount of power processed by the resonant network to be delivered to the load. Excess energy is returned to the source thorough switch S_2.

The parasitic capacitance of switches S_1 and S_2 are absorbed by the resonant capacitances C_S and C_D. Generally, capacitances C_S and C_D are placed directly across the corresponding power switch. However, there are many possible locations in the circuit for these resonant capacitances that would result in CF ZVS-MR operation. The different possible locations for C_S, C_D, and L can be identified by application of the capacitor and inductor shift rules [G6]. The shifting of the resonant components will result in different bias applied to the given resonant component, but it will not affect the basic operation of the circuit.

For high-frequency operation, the resonant capacitors should be placed directly across the active switches to prevent circuit lead inductances from introducing an additional reactance that can interact with the other resonant components. Any inductance between the junction capacitance and C_S and C_D will result in undesirable oscillations. If the frequency of operation is sufficiently high, no external capacitances are needed and the junction capacitances of the power switches can be used as the resonant capacitances C_S and C_D.
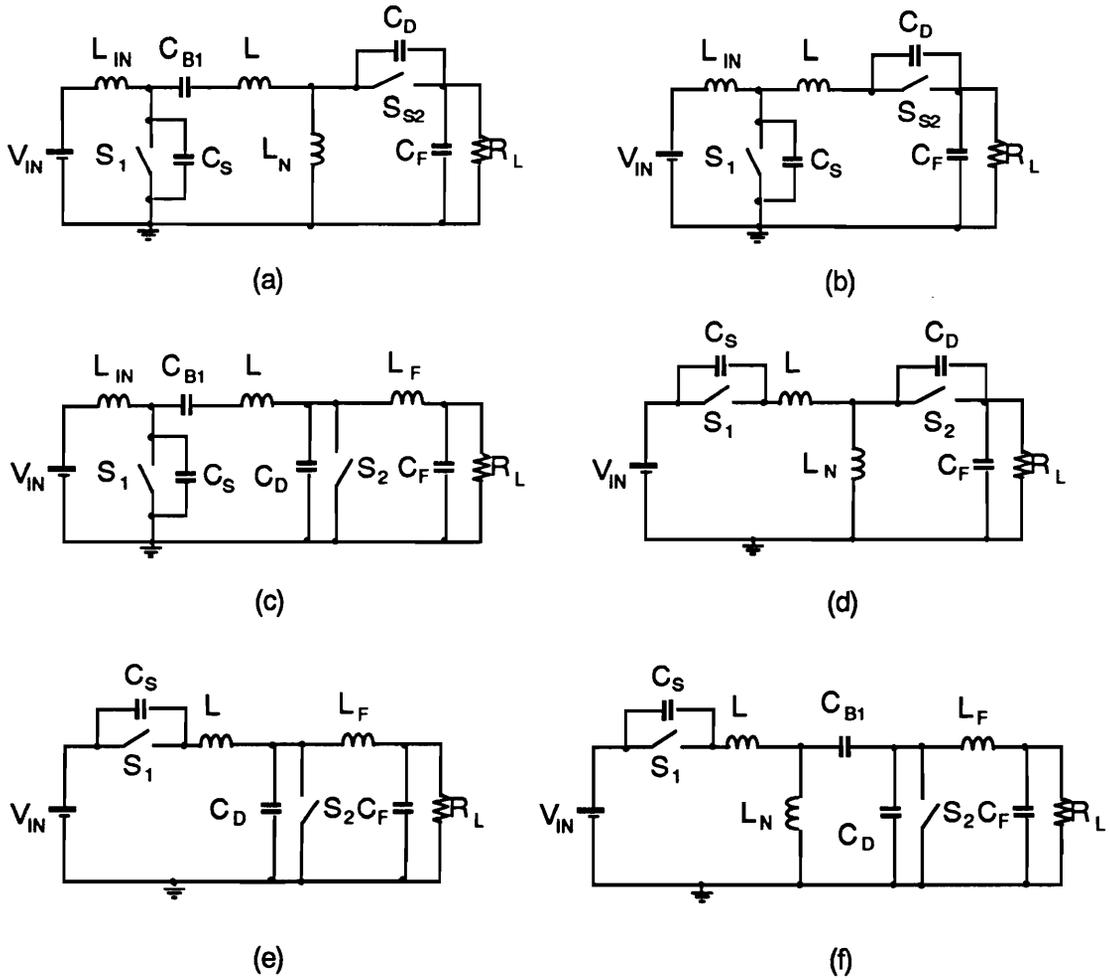
Figure 2.8. Basic CF ZVS-MRC topologies: (a) sepic, (b) boost, (c) cuk, (d) buck-boost, (e) buck, and (f) zeta. S_2 is the constant frequency switch.
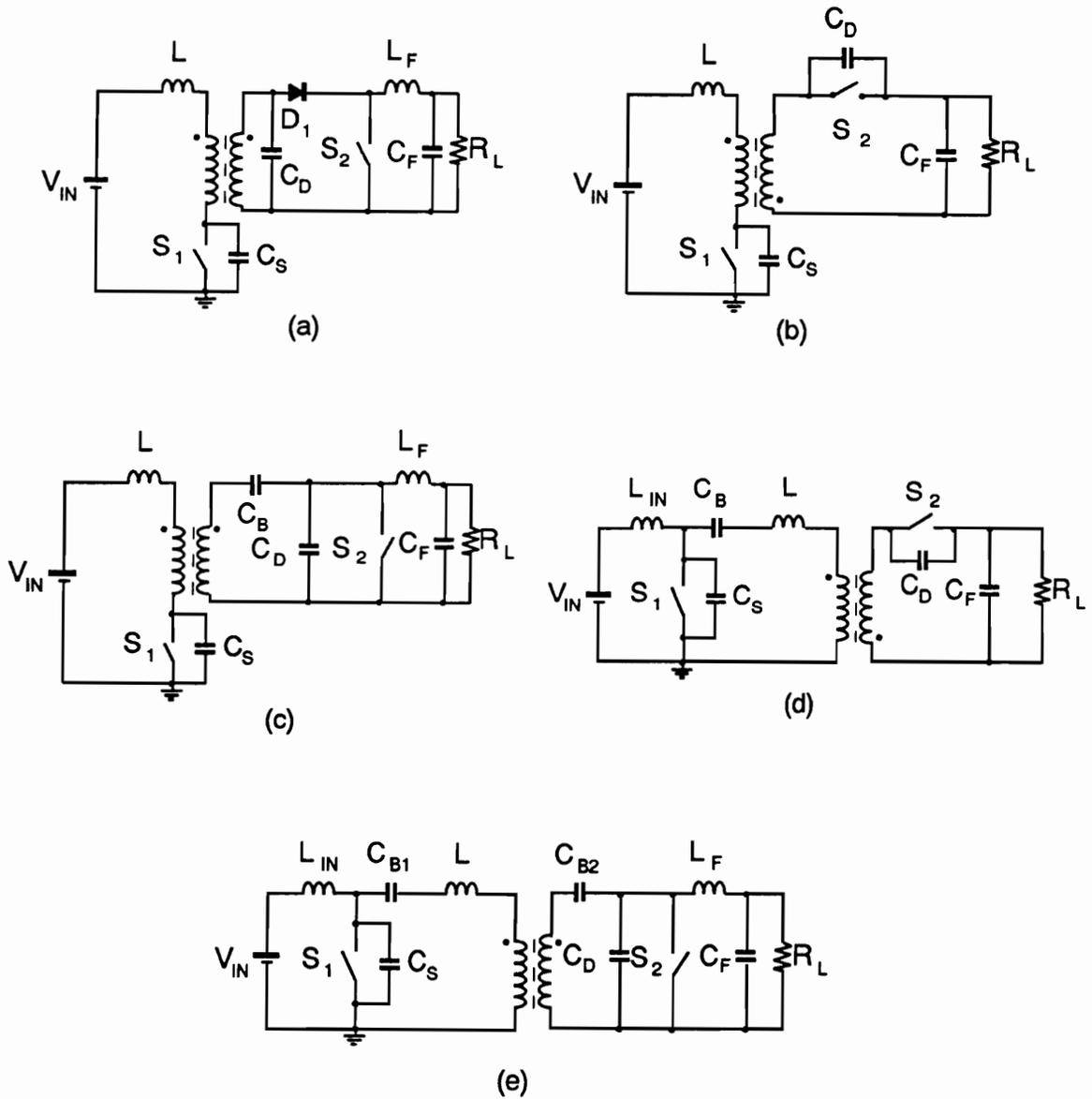
Figure 2.9. Basic single-ended isolated CF ZVS-MRC topologies: (a) forward, (b) flyback, (c) zeta, (d) sepic, and (e) cuk. S_2 is the constant frequency switch.

In most power conversion applications, a power transformer is used in dc/dc converter circuits to provide electrical isolation and/or the desired conversion ratio. Generally, the leakage inductance of the power transformer, especially in off-line applications, can disrupt the normal operation of dc/dc converters. CF MR converters absorb the effect of the leakage inductance of the transformer without disrupting the operation of the converter. The six basic isolated topologies are shown in Fig. 2.9. The resonant capacitance C_D is shown in the secondary circuit, directly in parallel with switch S_2. Placing capacitance C_D on the secondary allows the leakage inductance of the transformer to form part of the resonant inductor L.

Capacitance C_D can also be placed across the primary windings of the power transformer. The advantage of placing the resonant capacitance C_D on the primary side is that the high frequency current associated with this capacitance will not circulate through the power transformer, thereby reducing transformer winding losses. The effect of the leakage inductance can not be accounted for in the operation of the converter if capacitance C_D is placed across the primary winding of the transformer. At high switching frequencies, this arrangement will result in unwanted ringing between the leakage inductance and the junction capacitance of switch S_2 and the forward diode D_1 in the forward topology. This ringing increases conduction losses in the rectifier circuit and could possibly result in an unstable operation similar to that of ZVS-QRCs [B17,D1,D8,D12].

Operation of CF ZVS-MRCs results in conduction of the antiparallel diode of the CF switch for an extended period of time. If a MOSFET switch is used for the CF switch, the poor characteristics of the inherent antiparallel diode in all MOSFET switches will result in high conduction losses. Conduction losses due to the conduction of the anitparallel diode of the CF switch can be reduced by placing an external low forward voltage drop diode (Schottky diode) in parallel with the MOSFET switch. A second alternative is to advance the turn-on time of the CF switch

and operate the MOSFET switch as a synchronous rectifier [D12]. That is, force the current to flow through the MOSFET rather than the antiparallel diode. Synchronous rectifiers are MOSFET devices with improved third quadrant characteristics. These devices are manufactured to operate as controlled rectifiers and their third quadrant voltage vs. current characteristics are much better than their first quadrant characteristics. The idea of synchronous rectification can be used successfully in CF ZVS-MRCs to reduce conduction losses of the CF switch by using a device that has good first and third quadrant voltage vs. current characteristics (low $R_{DS}(ON)$). Using synchronous rectification in CF ZVS-MRCs does not result in additional control. This will become more clear as the control requirements for the CF forward and HB ZVS-MRCs are discussed in the next chapter.

The operation of nonisolated CF ZVS-MRCs can be directly extended to the single-ended, isolated topologies, as long as the magnetizing current of the transformer is neglected. Therefore, the analysis is not directly applicable to the CF forward ZVS-MRC since the magnetizing current plays an important role in its operation [D7]. Also, the analysis cannot be directly applied to off-line (bridge-type, push-pull) ZVS-MRCs due to the inherent clamping of the resonant voltage waveform of the primary switches [B22,D8].

Figure 2.10 shows different implementations of the CF forward ZVS-MRC. CF operation of this converter is possible by regaining control of the turn-off time of the freewheeling diode. Direct control of the turn-off time of this device is achieved by replacing it by an active switch as shown in Fig. 2.10(a). Control of the turn-off time of the freewheeling diode is also possible by controlling the turn-on time of the forward diode D_1. Control of the turn off time of the forward diode is achieved by replacing this diode with an active switch as shown in Fig. 2.10(b).
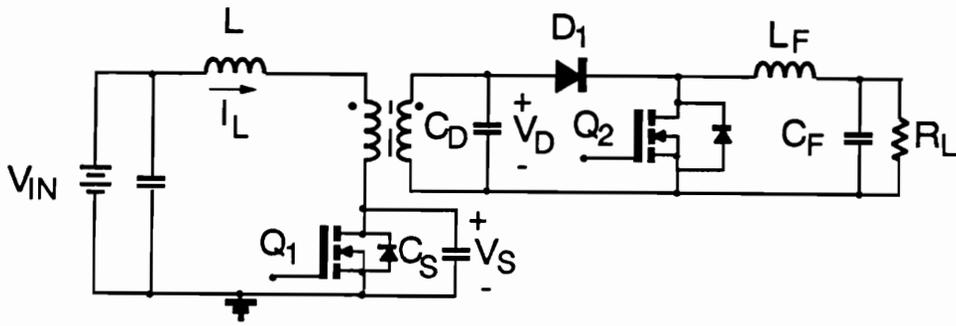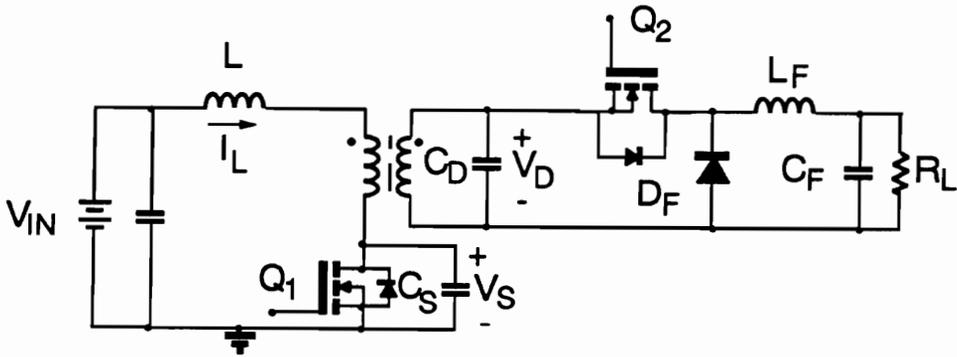
Figure 2.10. Different implementations of the CF forward ZVS-MRC:
(a) Constant frequency switch Q_2 in place of freewheeling diode D_F;
(b) Constant frequency switch Q_2 in place of forward diode D_1.
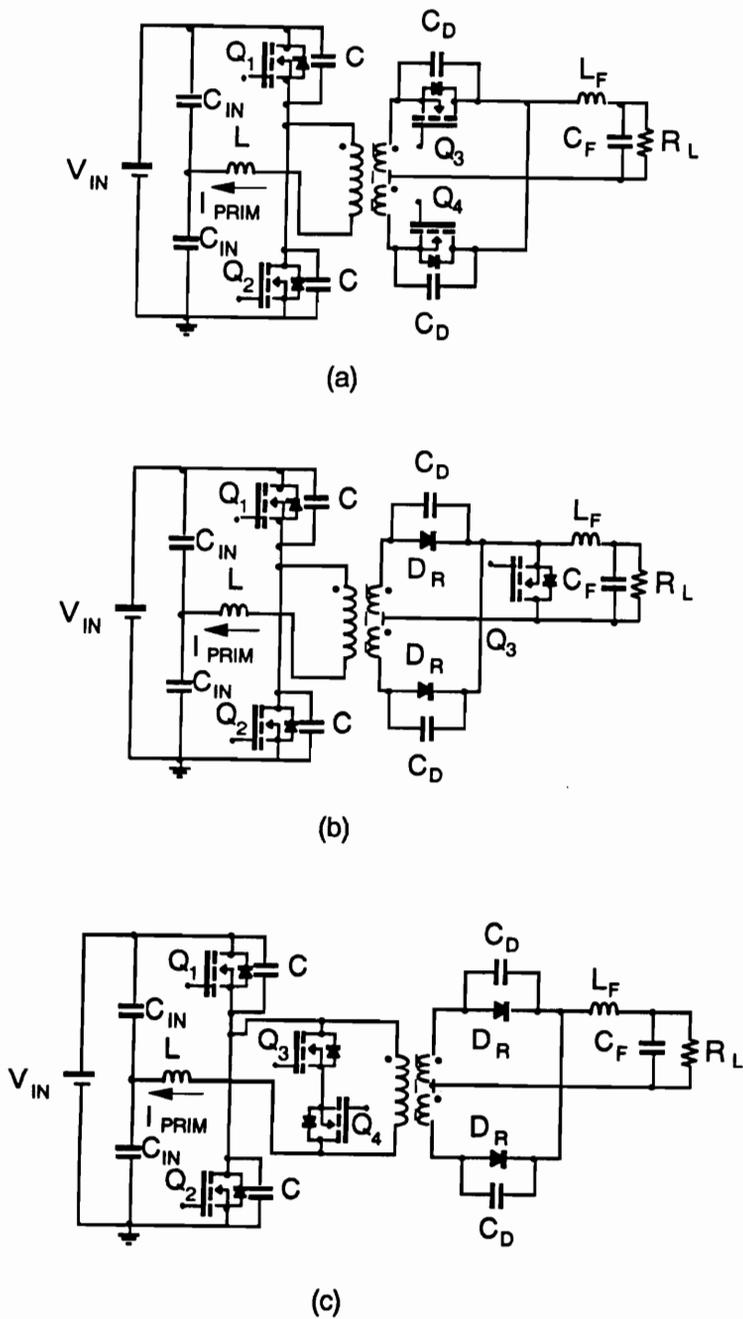
Figure 2.11. Different implementations of the CF HB ZVS-MRC.
(a) Two active switches (constant frequency switches) replacing the rectifier diodes;
(b) One active switch placed across the input of the output filter;
(c) A bidirectional switch across the primary windings of the transformer.

The first implementation of this converter, shown in Fig. 2.10(a), is preferred because no isolated driver is needed for switch S_2 (CF switch).

Figure 2.11 shows different implementations of the CF HB ZVS-MRC. Like the conventional HB ZVS-MRC, the load current freewheels through the shorted secondary windings of the power transformer during the freewheeling stage of the CF HB ZVS-MRC [D6,D8,E20]. Since the secondary windings of the transformer are shorted during this stage, the CF HB ZVS-MRC can be implemented by adding only one extra switch (across the output filter) as shown in Fig. 2.11(b) and still operate with ZVS. Furthermore, CF switch Q_3 can be shifted to the primary side of the power transformer as shown in Fig. 2.11(c). This implementation requires a true bidirectional switch. By placing the CF switch on the primary side, the conduction losses in this switch and the power transformer are reduced considerably. A complete dc analysis of the CF forward and the HB ZVS-MRC will be presented in Chapter 3.

A detailed analysis of the CF cuk ZVS-MRC has been presented in [E6].

2.6 Experimental CF Buck ZVS-MRC

To demonstrate the high-frequency operation of CF multi-resonant converter, a CF buck ZVS-MRC was implemented. The circuit diagram of the experimental converter is shown in Fig. 2.12. The converter uses a simple control scheme to regulate the output voltage. The
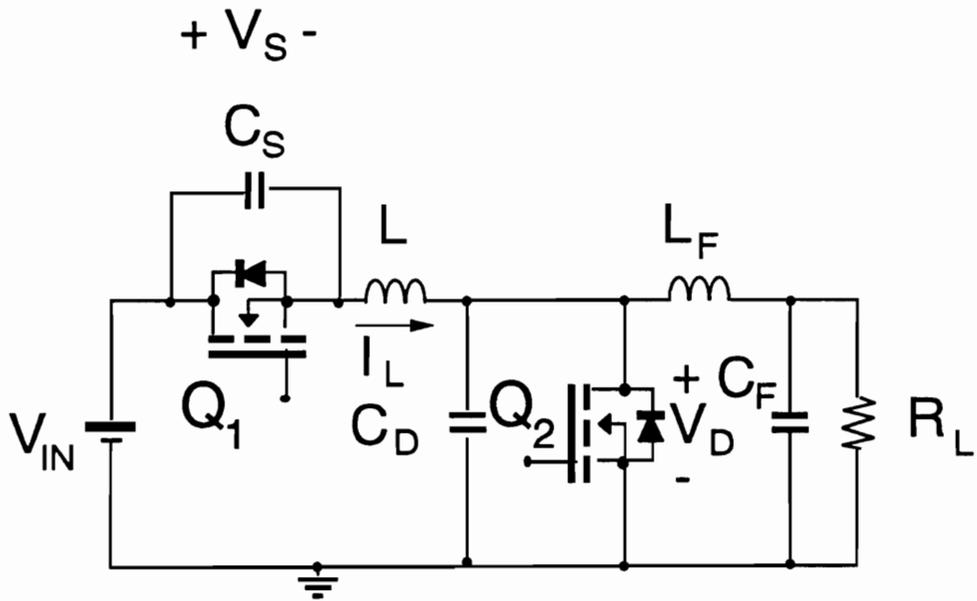
Q_1 and Q_2 - IRFZ40

V_{IN} = 15.5 V

V_O = 7.5 V

P_O = 30 W

Figure 2.12. Experimental CF buck ZVS-MRC. A MOSFET switch is used for the constant frequency switch Q_2.

Table 2.1. Efficiency of experimental CF buck ZVS-MRC for different load currents

V_{IN} [V]	I_{IN} [A]	V_O [V]	I_O [A]	η [%]
15.5	2.55	7.52	4.07	77.4
15.5	2.30	7.65	3.50	75.2
15.5	2.00	7.55	3.00	73.1
15.5	1.80	7.39	2.50	66.2
15.5	1.70	7.46	2.00	56.6
15.5	1.50	7.56	1.50	48.9
15.5	1.20	7.52	1.00	40.4
15.5	0.70	7.67	0.00	0.00

Q1 drive

MONOSTABLE #1
Td control

Q_

OSCILLATOR
Toff control

Flip-Flop

O
CK   RD

Q

CL

MONOSTABLE #2
Ton control

Q_

Q2 drive

T_s

T_{off}

T_d

T_{on}
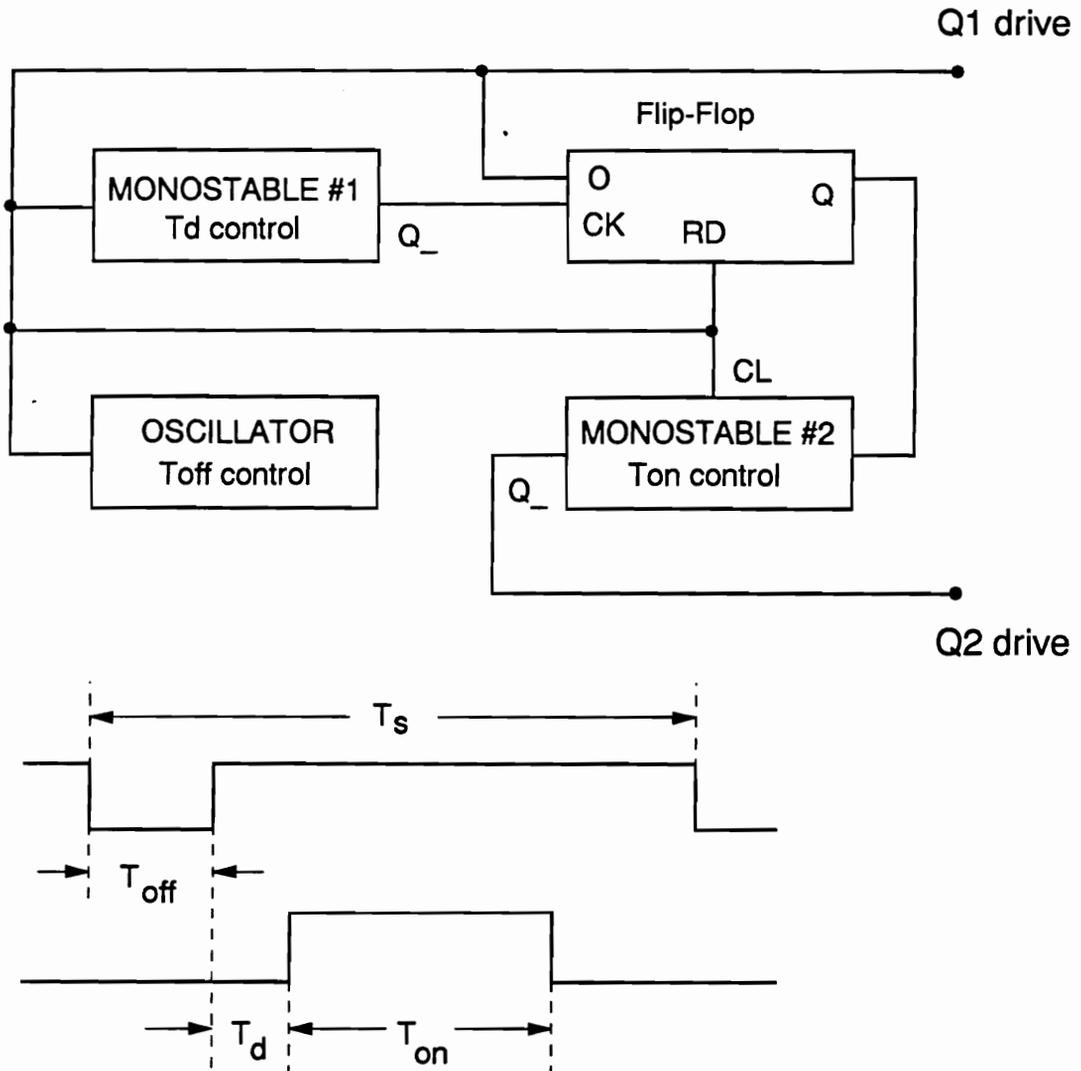
Figure 2.13. Conceptual diagram of gate drive for CF buck ZVS-MRC. Active switch Q_1 oscillates at constant frequency and constant duty cycle. The constant frequency switch Q_2 is pulse-width-modulated.
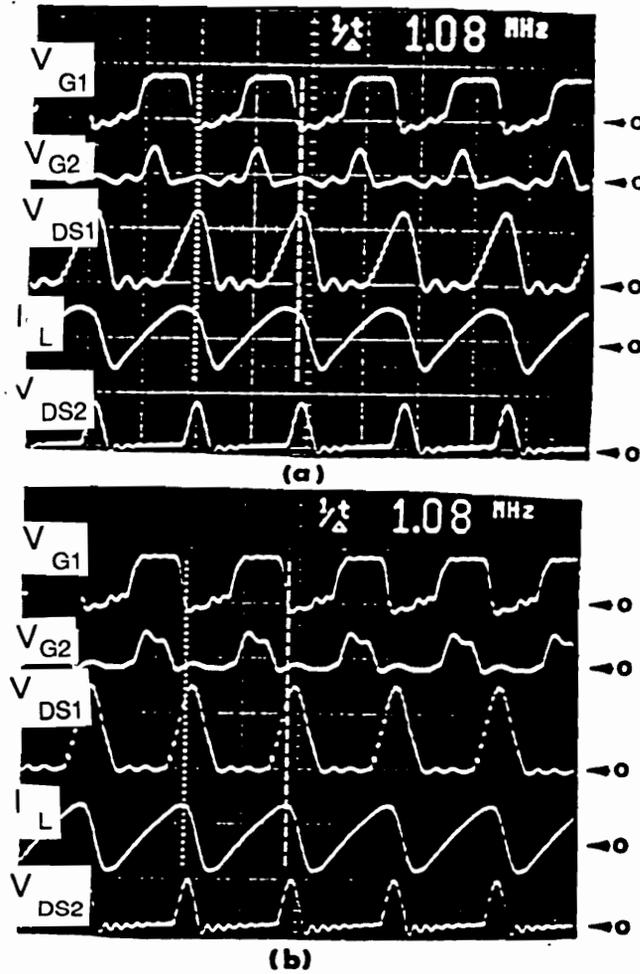
Figure 2.14. Oscillograms of experimental CF buck ZVS-MRC for different loads:
(a) full load (7.5 V/ 4 A);
(b) no load (7.5 V/ 0 A).
Shown from top to bottom, are the following waveforms: gate-to-source voltages of Q_1 (V_{G1}) and Q_2 (V_{G2}), voltage across switch Q_1 (V_{DS1}), resonant inductor current (I_L), and voltage across switch Q_2 (V_{DS2}). Input voltage $V_{IN} = 15\ Vdc$.

driving signal of the CF switch can be generated from the driving signal of the primary switch Q_1 as shown in Fig. 2.13. The converter is controlled by varying the duration of T_{ON} of the driving signal for Q_2.

The converter was designed to deliver 30 W at an input voltage of 15 V and output voltage of 7.5 V. The converter was operated at a switching frequency of 1.08 MHz. The following components were used for the power stage:

S_1, S_2	- IRFZ40;
C_S	- 15 nF NPO chip ceramic;
C_D	- 50 nF NPO chip ceramic;
L	- 500 nH;
L_F	- 1 μH; and
C_F	- 22 μH.

Figure 2.14 shows the ocsillograms of the experimental buck converter for full load and light load operation. The waveforms are very clean with essentially no parasitic oscillations. The converter regulates the output voltage from full load (4 A) to no load (0 A) at a constant switching frequency. The measured power stage efficiency for different load conditions is given in the last column of Table 2.1. MOSFET voltage stress does not vary considerably as the load is varied from full load to no load.

2.7 Summary

A new family of CF ZVS-MRCs has been presented. The CF ZVS-MR family of converters can be generated by replacing the PWM switch by the CF MR switch in the typical PWM converters. The CF ZVS-MRCs are suitable for high-frequency operation due to their ability to absorb all of the major parasitic components into the resonant network. All semiconductor devices operate under ZVS conditions at a constant switching frequency resulting in a substantial reduction of switching losses.

3. ANALYSIS OF CF FORWARD AND HALF-BRIDGE ZVS-MRCs

3.1 Introduction

The PWM forward and half-bridge (HB) converters are two of the most popular topologies used in applications that require isolation. The forward topology is most effective in the 50 W - 200 W range. The single-ended, single switch forward converter is a very cost effective topology due to its low part count. The forward converter is one of the most attractive topologies of the new family of CF ZVS-MRCs. Its operation, analysis, and characteristics are similar to those of the conventional forward ZVS-MRC. However, the effect of the magnetizing inductance of the power transformer, which makes the operation of the CF forward ZVS-MRC quite different from that of the CF buck ZVS-MRC, cannot be ignored.

The voltage stress of the active switch in single-ended ZVS converters is generally several times the input voltage [B33,D1-D15]. On the other hand, the bridge-type topologies clamp the voltage across the primary active switches to the value of the input voltage. Therefore, in similar applications, single-ended topologies require the use of switches with higher break-down voltage. These devices have higher on-resistance relative to the devices used in HB and push-pull topologies. As a result, the HB converter will operate with lower turn-on loss. Consequently, the ZVS HB converter is very attractive for off-line applications where the switching loss is of importance. Also, due to the two quadrant operation of the HB topology, the transformer of this converter operates with reduced flux density when compared with the one used for the forward or flyback converters having similar cross-sectional core areas.

Flux reset in the power transformer is not a concern in CF forward and HB ZVS-MRCs. In the forward topology, transformer core reset is provided by the resonant capacitance C_D that ap-pears across the secondary winding of the transformer [D7,D12]. In the HB topology, trans-former core reset results from the two-quadrant operation.

Finally, due to the higher conversion frequency, the HB converter requires a smaller output filter. For the same peak-to-peak output voltage ripple, the filter corner frequency of the HB topology is twice that of the forward and flyback topologies.

This chapter presents complete dc analysis of the CF forward and HB ZVS-MRCs. It also dis-cusses design trade-offs and outlines design procedure for both the forward and HB topologies. Finally, experimental results for a 50 W CF forward ZVS-MRC and a 100 W, off-line, CF HB ZVS-MRC are presented.

3.2 CF Forward ZVS-MRC

Figure 3.1 shows the conventional forward and the CF forward ZVS-MRCs. The constant fre-
quency implementation of the forward ZVS-MRC is derived by simply replacing the free-
wheeling diode in the forward ZVS-MRC by transistor Q_2 as shown in Fig. 3.1(b). Capacitance
C_S is the resonant capacitance across transistor Q_1 and it includes the output capacitance of
this switch. Capacitance C_D is the resonant capacitance across the secondary windings of the
power transformer, and it incorporates the parasitic capacitance of both, rectifier D_1 and CF
switch Q_2. L is the resonant inductor and it absorbs the leakage inductance of the power
transformer.

3.2.1 DC Analysis

To simplify the analysis it is assumed that:

a)   the output filter inductance is sufficiently large and can be approximated by a current
     source with a value equal to the output current, I_O;

b)   the voltage drop across the conducting semiconductor switches (MOSFETs and diodes)
     is negligible;

c)   the switching times of the semiconductor switches are zero; and
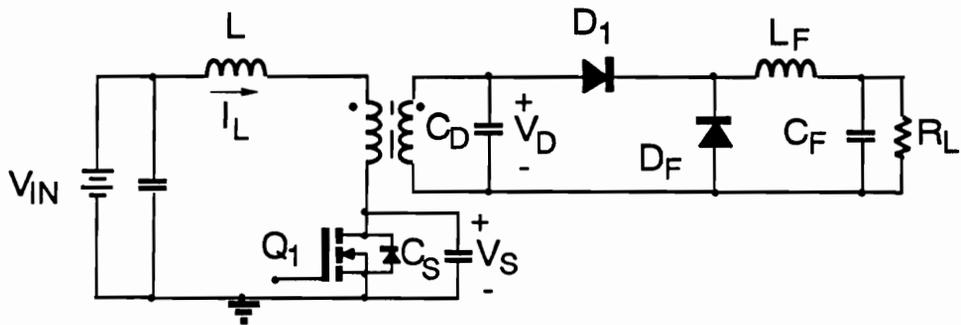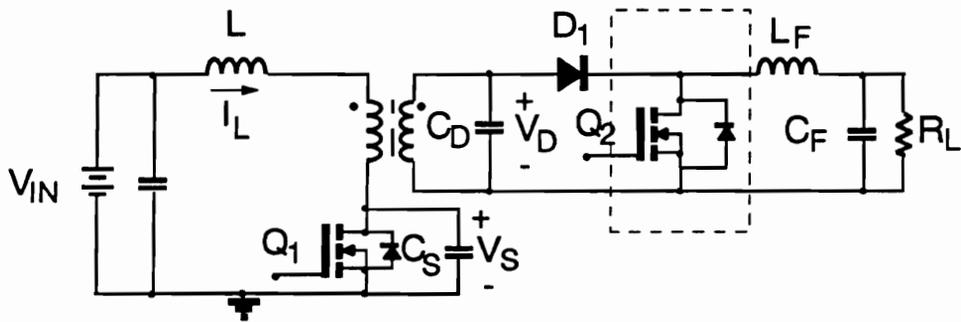
Figure 3.1. (a) Forward ZVS-MRC (b) CF forward ZVS-MRC.

3. ANALYSIS OF CF FORWARD AND HALF-BRIDGE ZVS-MRCs

d) the magnetizing inductance of the power transformer is large and can be represented by an equivalent current source, I_M, whose magnitude depends on the operating condition but is constant over one switching cycle.

To further simplify the analysis, the load current, I_O, and the resonant capacitance, C_D, are reflected to the primary side of the transformer. In addition, diode D_1 and transistor Q_2 are replaced by a single-pole double-throw switch. The equivalent model of the simplified converter is shown in Fig. 3.2.

During one switching cycle, the converter goes through a sequence of five of the six possible topological stages shown in Fig. 3.3. The CF forward ZVS-MRC can operate in four different modes, each representing a different sequence of topological stages. Modes II.A and II.B occur for heavy load currents, whereas Modes I.A and I.B occur for light output currents.

3.2.1.1 Mode I of Operation

The sequence of the topological stages in Mode I.A is A-B-C-A-E. Figure 3.4 shows the key waveforms of the CF forward ZVS-MRC in this mode of operation.

Stage A [T_0, T_1], Fig. 3.3(a)

During this stage transistor Q_1 and diode D_1 are conducting and transistor Q_2 is off. Voltage V_D across C_D is positive and capacitance C_D and inductor L resonate until the voltage across
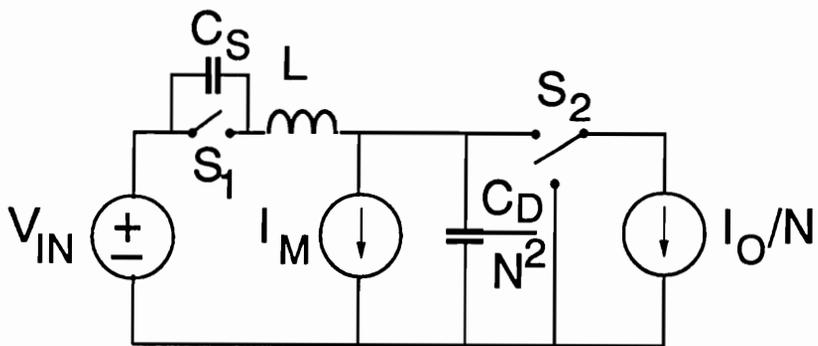
Figure 3.2. Equivalent model of the CF forward ZVS-MRC.
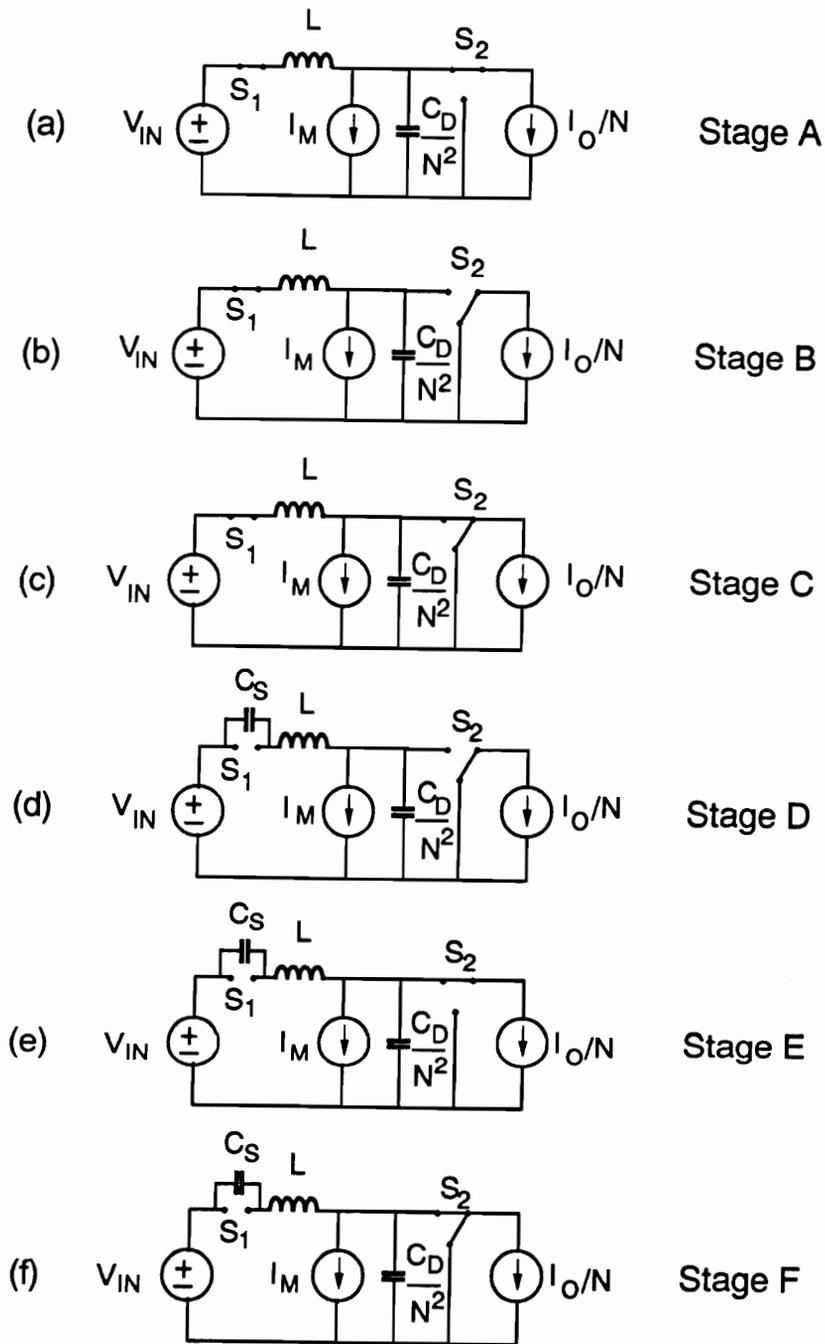
Figure 3.3. Topological stages of the CF forward ZVS-MRC: (a) Stage A, (b) Stage B, (c) Stage C, (d) Stage D, (e) Stage E, and (f) Stage F.
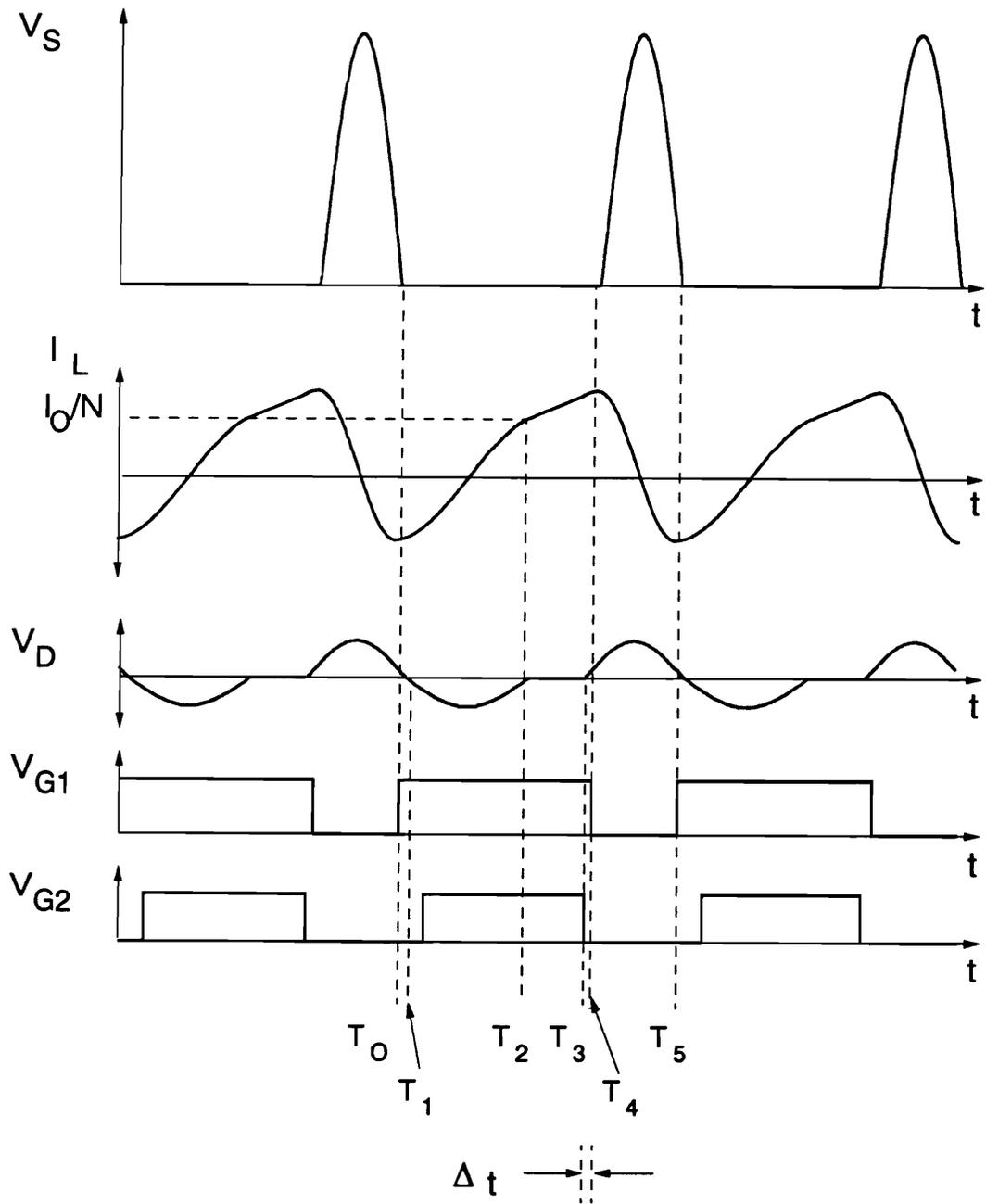
Figure 3.4. Ideal waveforms of the CF forward ZVS-MRC operating in Mode I.A, from top to bottom: drain-source voltage of switch Q_1, V_S, resonant inductor current I_L, capacitor voltage V_D, gate-source voltage V_{G1}, and gate-source voltage V_{G2}. Δt is defined as the time between the turn-off of switch Q_1 and the constant frequency switch Q_2.

Q_2 reaches zero at time T_1 and its antiparallel diode starts conducting. At the same time diode D_1 turns off.

Stage B $[T_1, T_2]$, Fig.3.3(b)

Since the antiparallel diode of Q_2 is conducting. capacitance C_D continues to resonate with L. This stage ends at time T_2 when voltage V_D increases to zero and diode D_1 turns on. To achieve lossless turn-on, Q_2 should be turned on during this stage.

Stage C $[T_2, T_3]$, Fig. 3.3(c)

In this stage D_1 and Q_2 conduct. As a result. voltage V_D is clamped to zero and the voltage across resonant inductor L is V_{IN}. The resonant inductor current increases linearly until Q_2 is turned off at time T_3.

Stage A $[T_3, T_4]$, Fig. 3.3(a)

Diode D_1 remains on and capacitance C_D and inductance L start to resonate. Voltage V_D increases in a resonant manner. This stage ends at time T_4, when Q_1 is turned off.

Stage E $[T_4, T_5]$, Fig. 3.3(e)

Diode D_1 remains on, so capacitances C_D and C_S and inductance L resonate. This stage ends at time T_5, when voltage V_S returns to zero through a resonant oscillation. Transistor Q_1 should be subsequently turned on to achieve lossless turn-on. The next cycle is then initiated.

From the preceding explanation it can be seen that the resonance of capacitance C_D is interrupted for only a short interval, $T_3 - T_2$. Switch Q_1 remains on during this interval and the resonant inductor current increases linearly.

In Mode I.B of operation the conduction time of the CF switch extends past the time at which switch Q_1 is turned off, resulting in lower dc voltage-conversion-ratios. The low dc voltage-conversion-ratios are due to the large period of the switching cycle during which the CF switch shorts the input terminals of the output filter.

3.2.1.2 Mode II of Operation

In Mode I of operation the capacitor voltage V_D is positive at the turn-off time of switch Q_1. In Mode II of operation the capacitor voltage V_D is negative at the turn-off time switch Q_1. For negative capacitor voltage V_D, the forward diode D_1 is off and the load current freewheels through the antiparallel diode of switch Q_2. Again, in Mode II.B of operation, the turn-off time of the constant frequency switch occurs after turn-off time of switch Q_1.

Figures 3.5 to 3.7 show the waveforms for Modes I.B, II.A, and II.B, respectively. The sequence of topological sequences for the different modes of operation are summarized in Table 3.1. A detailed description of the different modes of operation for CF forward ZVS-MRC are given in Appendix A.
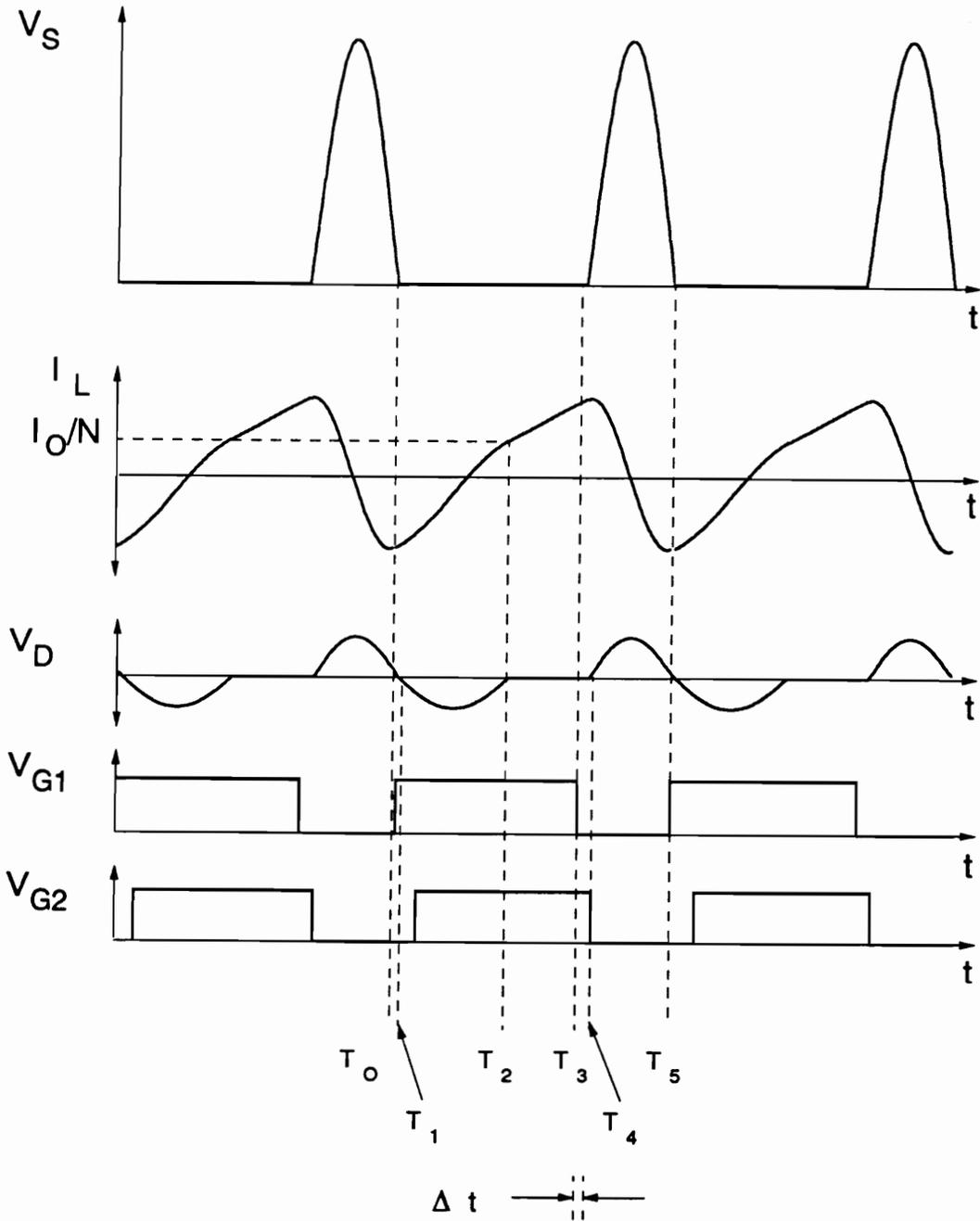
Figure 3.5. Ideal waveforms of the CF forward ZVS-MRC operating in Mode I.B, from top to bottom: drain-source voltage of switch Q_1, V_S, resonant inductor current I_L, capacitor voltage V_D, gate-source voltage V_{G1}, and gate-source voltage V_{G2}. Δt is defined as the time between the turn-off of switch Q_1 and the constant frequency switch Q_2.
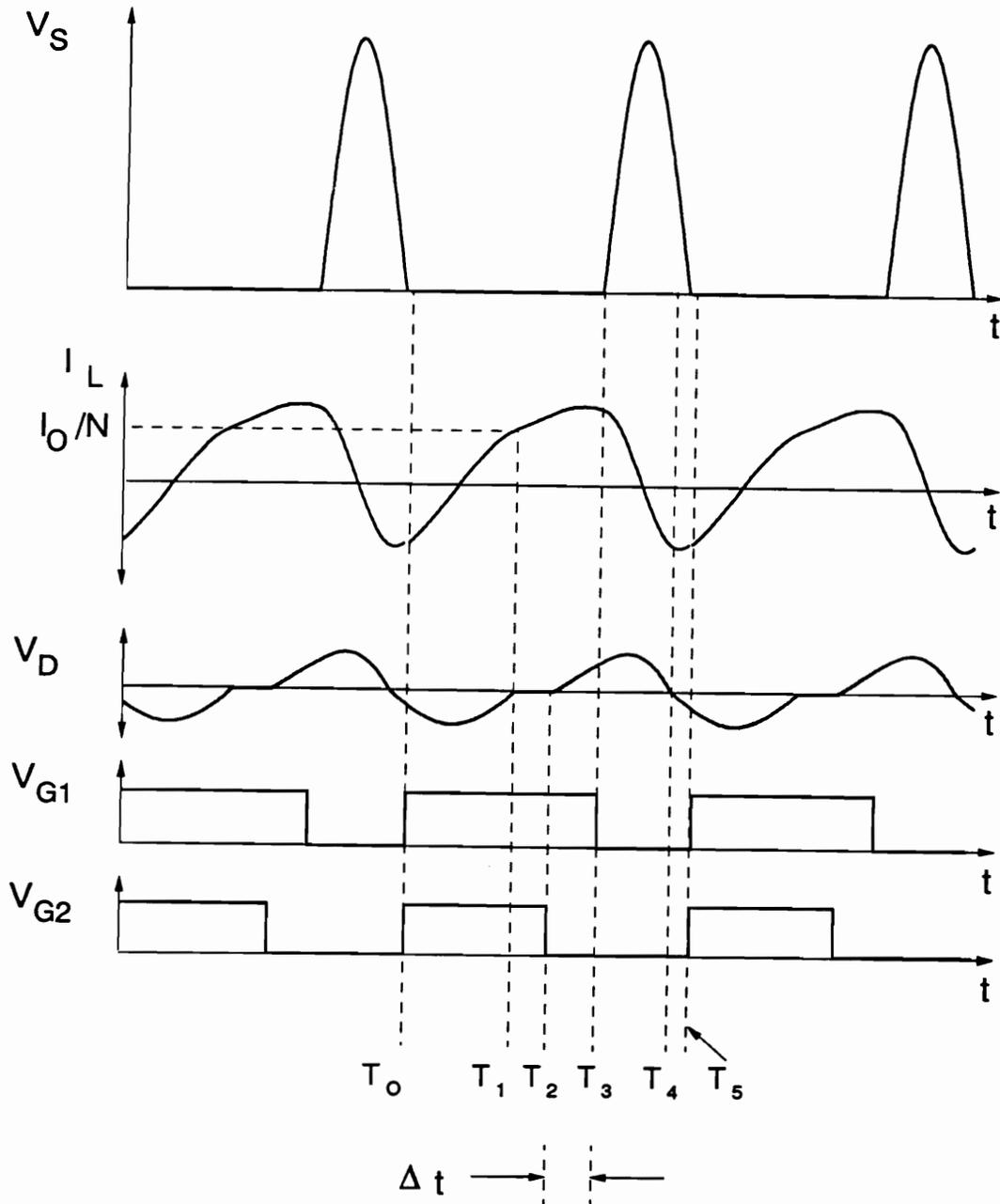
Figure 3.6. Ideal waveforms of the CF forward ZVS-MRC operating in Mode II.A, from top to bottom: drain-source voltage of switch Q_1, V_S, resonant inductor current I_L, capacitor voltage V_D, gate-source voltage V_{G1}, and gate-source voltage V_{G2}. Δt is defined as the time between the turn-off of switch Q_1 and the constant frequency switch Q_2.
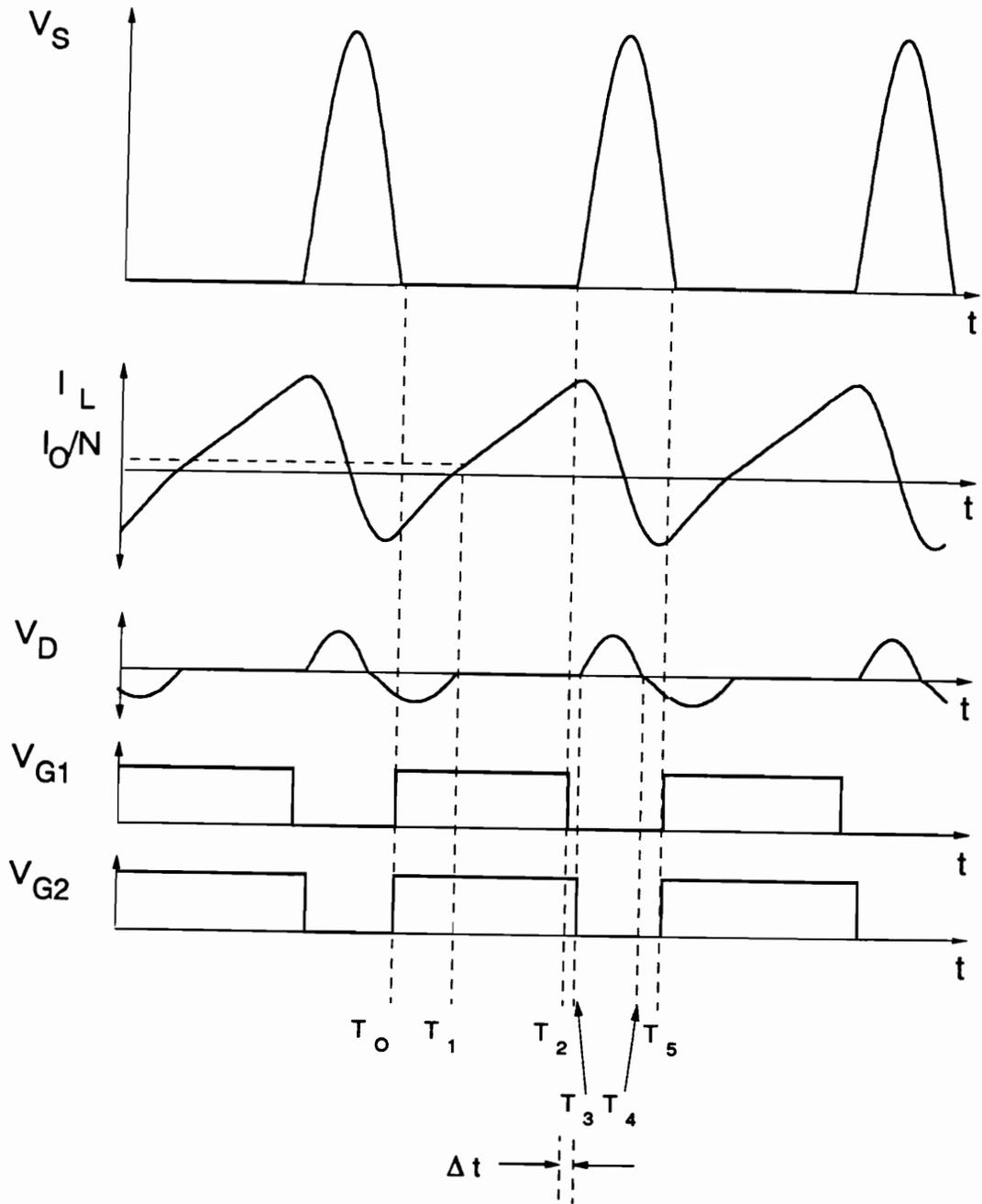
Figure 3.7. Ideal waveforms of the CF forward ZVS-MRC operating in Mode II.B, from top to bottom: drain-source voltage of switch Q_1, V_S, resonant inductor current I_L, capacitor voltage V_D, gate-source voltage V_{G1}, and gate-source voltage V_{G2}. Δt is defined as the time between the turn-off of switch Q_1 and the constant frequency switch Q_2.

Table 3.1. Modes of operation of the CF forward ZVS-MRC

MODE	STAGE SEQUENCE
I.A	A - B - C - A - E
I.B	A - B - C - F - E
II.A	B - C - A - E - D
II.B	B - C - F - E - D

3.2.2 DC Voltage-Conversion-Ratio

Due to the continuous resonance of the different resonant components, a closed form solution of the operation of the CF forward ZVS-MRC is not attainable. The dc voltage conversion ratio curves are obtained by using a numerical algorithm to solve the differential equations for each stage of the sequence for all five modes of operation. The equations describing the different topological stages are given in Appendix A. Figures 3.8 and 3.9 show the typical dc voltage-conversion-ratio characteristics of the CF forward ZVS-MRC as a function of δ. δ is defined as the time between the turn-off of the CF switch Q_2 and the turn-off of primary switch Q_1 (Δt in Fig. 3.4) normalized with respect to $1/f_O$, where $f_O = 1/2\pi\sqrt{LC_S}$ is the resonant frequency. The characteristics are given for different normalized switching frequencies, f_s/f_O, and different effective resonant capacitance ratio, $C_N = C_D/(C_S N^2)$, where N is the turns ratio of the trans-former. The running parameter in Figs. 3.8 and 3.9 is the normalized output current, $I_{ON} = Z_O I_O/N V_{IN}$, where $Z_O = \sqrt{L/C_S}$ is the characteristic impedance of the power stage.

Figure 3.8 also indicates the regions on dc voltage-conversion-ratio curves where the different modes of operation appear. Modes I.A and II.A occur for positive δ while modes I.B and II.B occur only for negative values of δ. For large normalized load currents and large values of δ, the dc voltage conversion curves will result in regions of positive slope. This behavior is similar to the one observed in conventional ZVS-MRCs for switching frequencies that are much smaller than the resonant frequency. In order to avoid instabilities, positive slope re-gions of the dc voltage conversion ratio characteristics should be avoided. Appendix A pro-vides a complete set of characteristics, $C_N = 2, 3, 5,$ and 7, and $f_S/f_O = 0.55, 0.6, 0.65, 0.7,$ and 0.8 for design purposes.
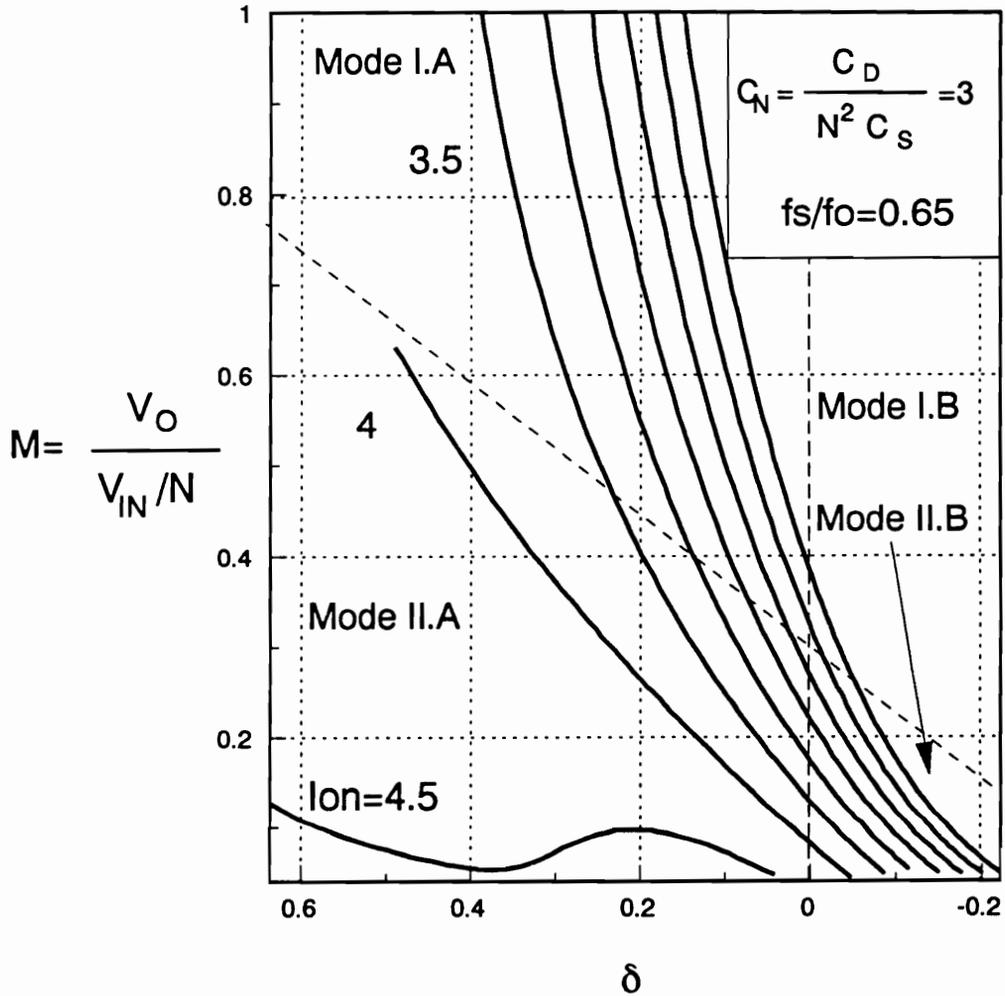
Figure 3.8. DC voltage conversion ratio curves of the CF forward ZVS-MRC indicating the region in which the different modes of operation occur; $C_N = C_D/(CN^2)$, $I_{ON} = I_O Z_O/V_{IN}$, $Z_O = \sqrt{L/C}$, and $f_O = 1/2\pi\sqrt{LC}$.
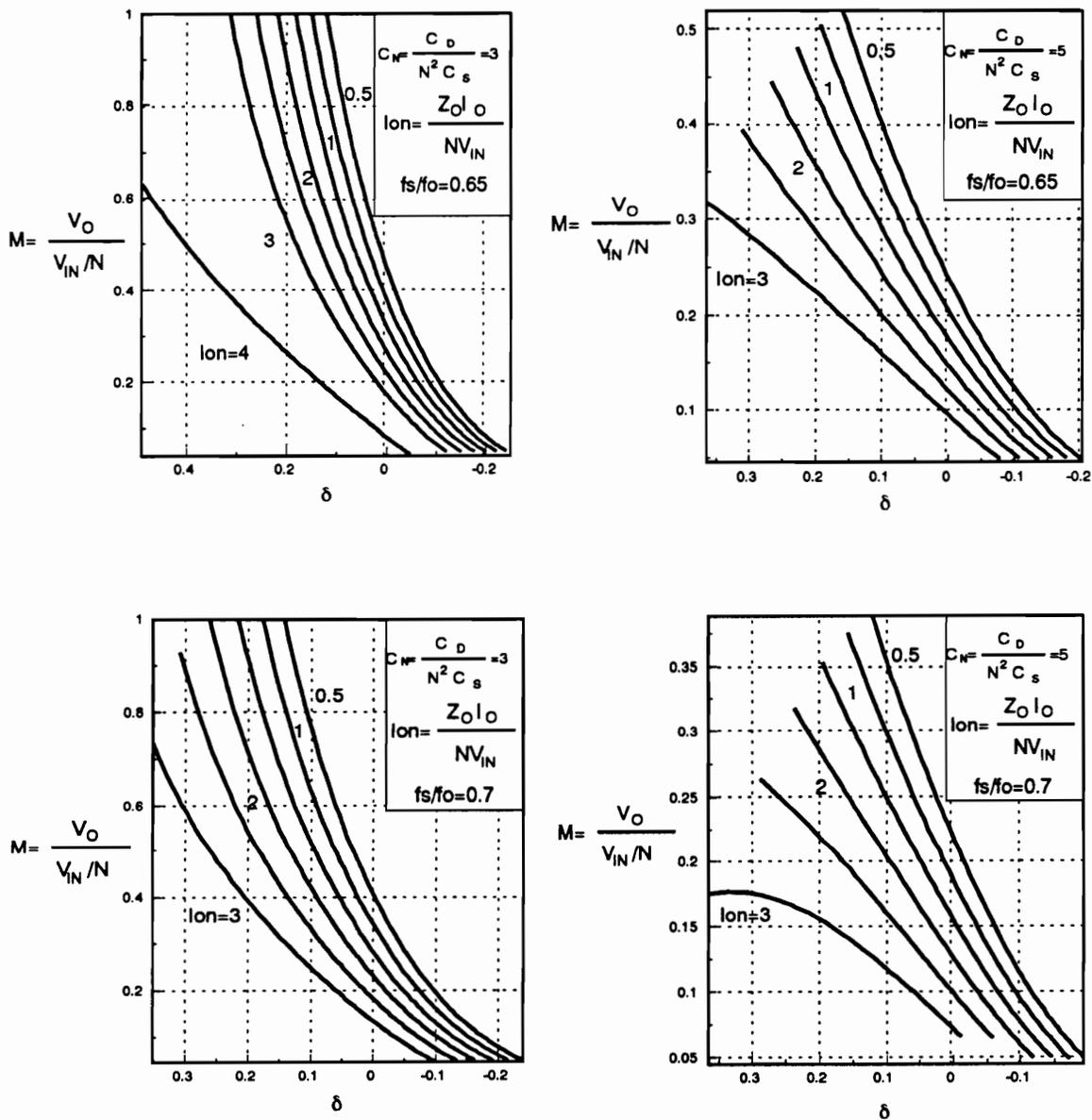
Figure 3.9. DC voltage conversion ratio curves of the CF forward ZVS-MRC for different values of C_N and f_s/f_O; $C_N = C_D/(CN^2)$, $I_{ON} = I_O Z_O/V_{IN}$, $Z_O = \sqrt{L/C}$, and $f_O = 1/2\pi\sqrt{LC}$.

3.3 CF HB ZVS-MRC

The circuit diagram of the conventional and CF HB ZVS-MRCs are shown in Fig. 3.10. The CF HB ZVS-MRC is obtained by replacing the output rectifiers in the HB ZVS-MRC with transistors Q_3 and Q_4 as shown in Fig. 3.10(b). Resonant capacitors C_1 and C_2 represent the output capacitance of the primary transistors, Q_1 and Q_2. Resonant inductor L can either be a separate inductor or the leakage inductance of the transformer. Since the junction capacitance of the CF switches is not sufficiently large to obtain the desired resonance, capacitors C_3 and C_4 are usually externally-added capacitors.

3.3.1 DC Analysis

To simplify the analysis, in addition to the assumptions made for the forward converter, it is assumed that Q_1 and Q_2 and switches Q_3 and Q_4 are identical so that $C_1 = C_2 = C_S$ and $C_3 = C_4 = C_D$. Since the magnetizing current is not important for the operation of the HB converter, it is ignored.

It was found that during one switching cycle the converter enters a sequence of five topological stages out of the seven possible shown in Fig. 3.11. It was also found that the CF HB ZVS-MRC can operate in six modes. Mode I.A occurs at high load currents and high dc voltage conversion ratios whereas modes II.A, II.B, and II.C occur at lighter load currents and
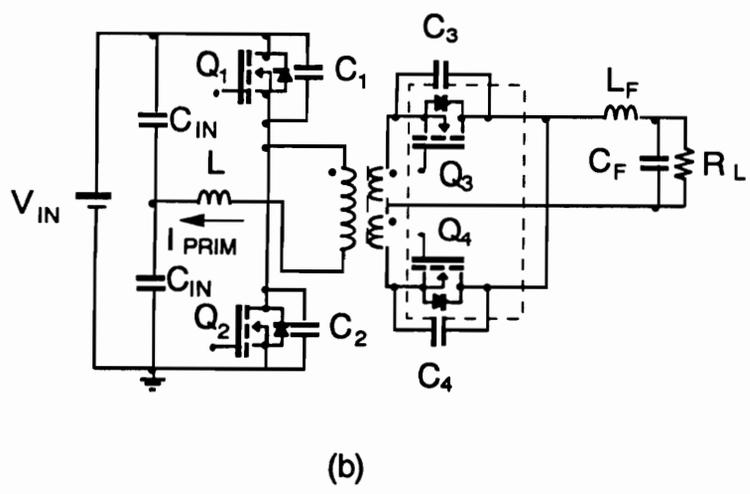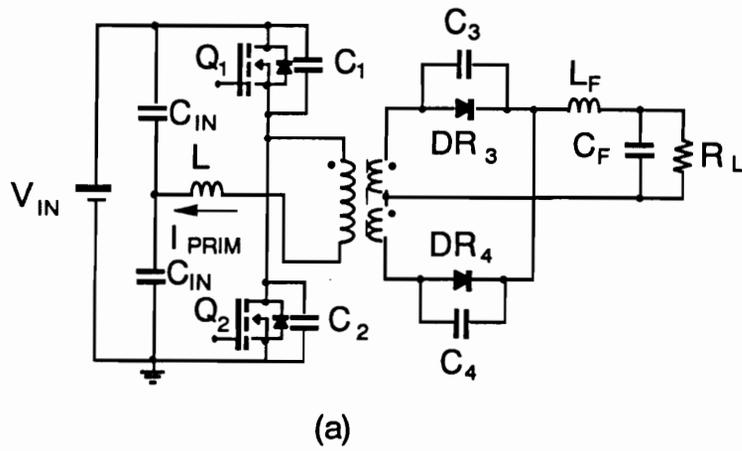
Figure 3.10. (a) Half-bridge ZVS-MRC (b) CF half-bridge ZVS-MRC.

high dc voltage-conversion-ratios. Modes I.B and I.C occur for low dc voltage conversion ratios.

3.3.1.1 Mode I of Operation

Figure 3.12 shows the key waveforms of the CF HB ZVS-MRC during Mode I.A of operation. The sequence of the topological stages in this mode is A-B-C-CF-D.

Stage A [T_0, T_1]. Fig. 3.11(a)

At time T_O, Q_1 is turned off. Since the antiparallel diode of Q_3 is reverse-biased, capacitances C_1, C_2, and C_4 resonate with inductance L. During this stage capacitance C_1 is being charged in a resonant manner and C_2 is being discharged. The stage terminates at time T_1 when voltage across capacitor C_2 becomes zero (at the same time voltage across C_1 is V_{IN}). Subsequently, switch Q_2 and the constant frequency switch Q_3 should be turned on to achieve soft switching.

Stage B [T_1, T_2], Fig. 3.11(b)

In this stage C_4 continues to resonate with L. Due to a negative voltage across L, the primary current decreases and C_4 continues to discharge. The stage terminates at time T_2 when the capacitor voltage across C_4 becomes zero and the antiparallel diode of Q_4 turns on.
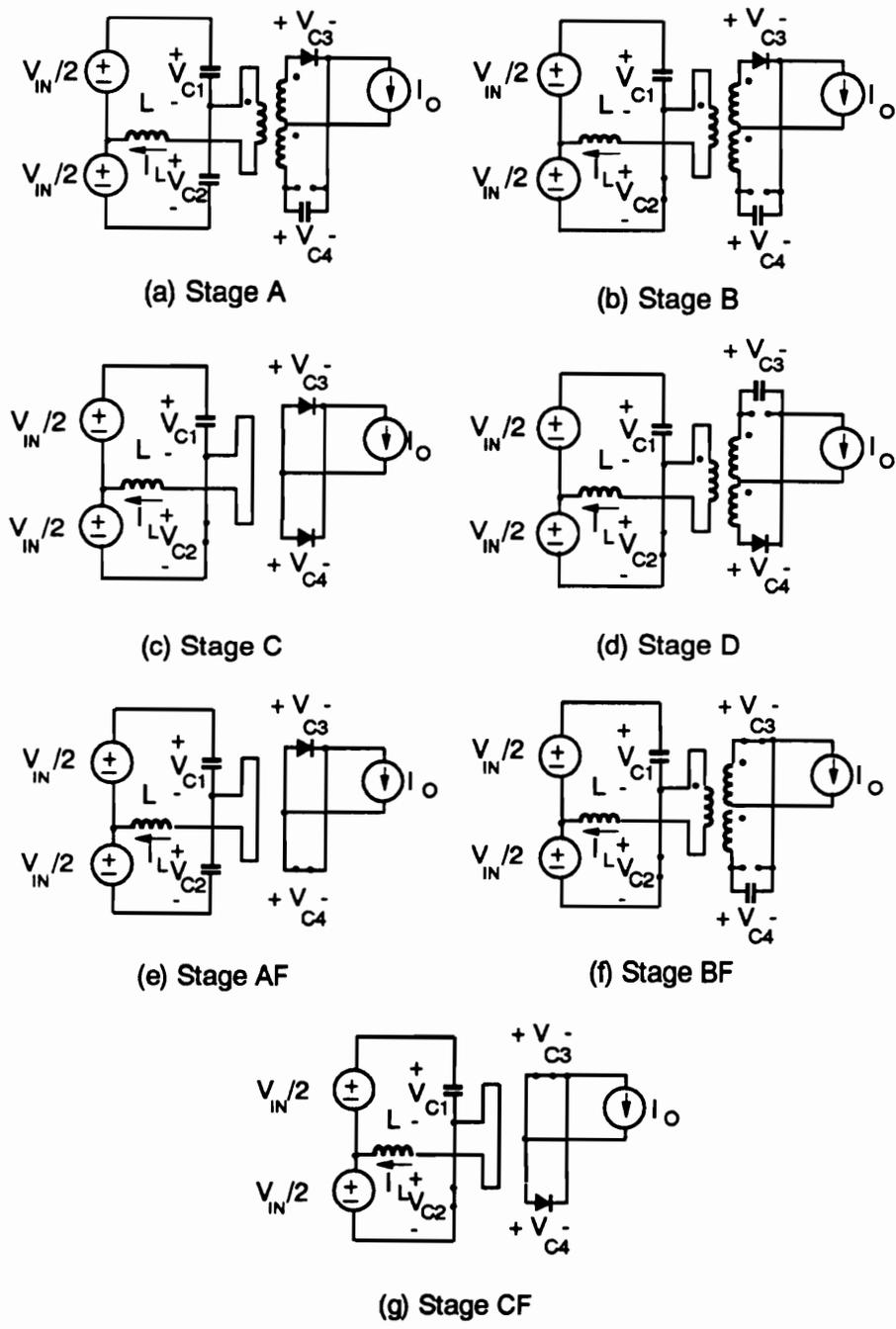
Figure 3.11. Topological stages of the CF HB ZVS-MRC: (a) Stage A, (b) Stage B, (c) Stage C, (d) Stage D, (e) Stage AF, (f) Stage BF, and (g) Stage CF.
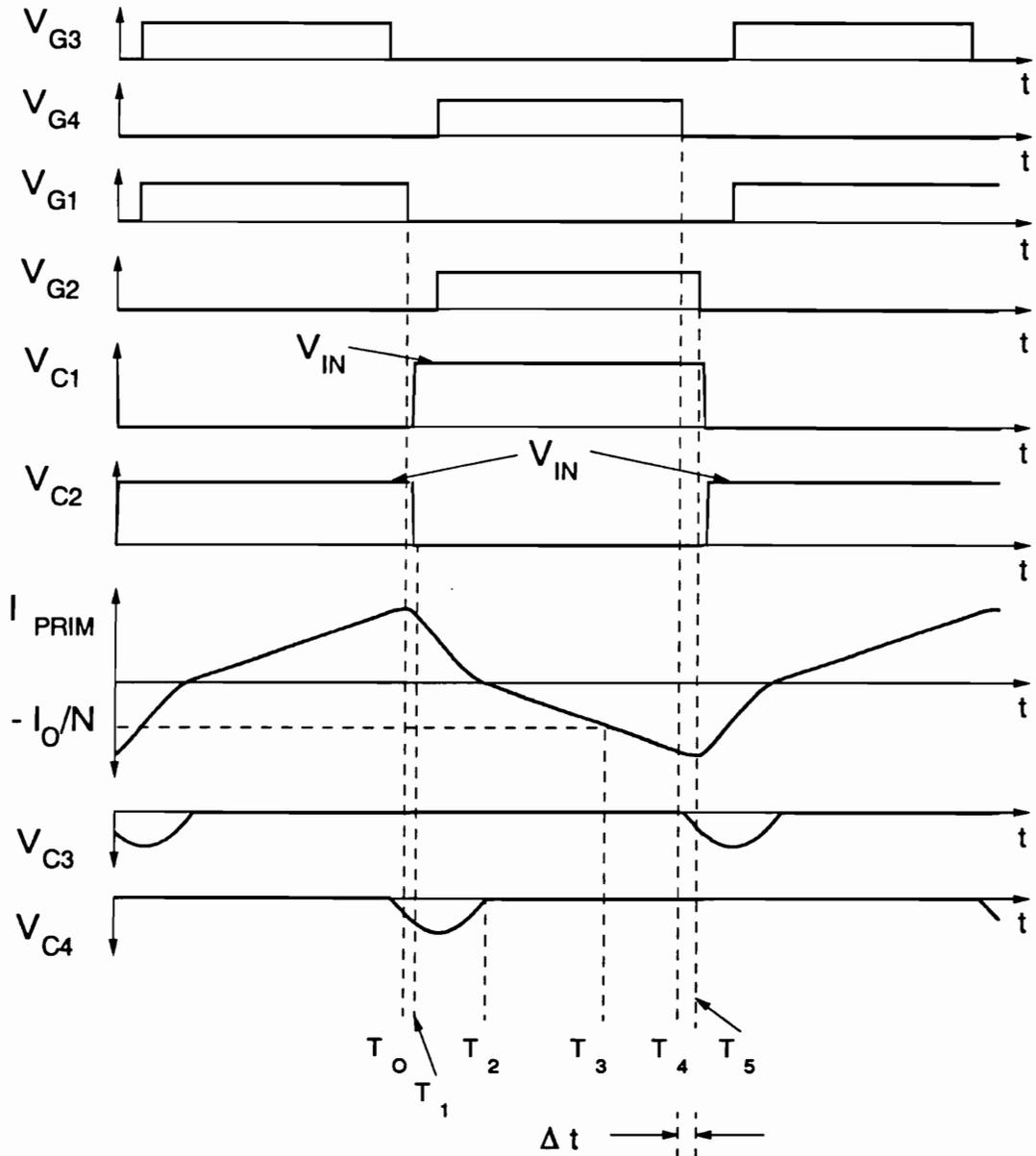
Figure 3.12. Ideal waveforms of the CF HB ZVS-MRC operating in Mode I.A, from top to bottom: gate-source voltage V_{G3}, gate-source voltage V_{G4}, gate-source voltage V_{G1}, gate-source voltage V_{G2}, drain-source voltage of switch Q_1, V_{C1}, drain-source voltage of switch Q_2, V_{C2}, primary current I_{PRIM}, capacitor voltage V_{C3}, and capacitor voltage V_{C4}. Δt is defined as the time elapsed between the turn-off of the primary switch, Q_1 or Q_2, and the corresponding constant frequency switch.

Stage C [T_2, T_3], Fig. 3.11(c)

In this stage the antiparallel diodes of Q_3 and Q_4 conduct so that the secondary windings of the transformer are shorted. As a result, the primary voltage across the transformer is zero and a negative voltage is applied to L. The primary current decreases with a constant rate. This stage terminates at time T_3 when the primary current becomes $-I_O/N$ and the antiparallel diode of Q_3 ceases to conduct.

Stage CF [T_3, T_4], Fig. 3.11(g)

During this stage transistor Q_3 conducts. The primary voltage of the transformer is zero and the current through the resonant inductor continues to decrease at a constant rate. This stage terminates when switch Q_3 is turned off at time T_4.

Stage D [T_4, T_5], Fig. 3.11 (d)

At time T_4, C_3 starts resonating with inductance L. This stage ends when transistor Q_2 is turned off and a new conversion cycle is initiated.

In Mode I.A of operation the time at which capacitance C_3 resonates with inductance L is delayed until switch Q_3 is turned off (as long as switch Q_3 is on the voltage across C_3 is shorted).

In Mode I.B and I.C the conduction time of switches Q_3 and Q_4 (the CF switches) is extended past the time during which the switching transition of switches Q_1 and Q_2 occurs. Therefore,

the voltage across the input of the output filter remains shorted for a longer period of the switching cycle resulting in low dc voltage-conversion-ratios.

3.3.1.3 Mode II of Operation

In this mode of operation the current through the resonant inductor is between $I_O/N < I_L < -I_O/N$ at the time the secondary side resonant capacitor discharges resulting in the absence of the natural freewheeling stage (Stage C). Mode II is characterized by increased circulating currents in the rectifier circuit and the secondary windings of the transformer.

In Modes II.B and II.C, the CF switches are allowed to conduct a longer period of time and they are not turned off until after the primary switches (switches Q_1 or Q_2) have been turned off. Figures 3.13 to 3.15 show the typical converter waveforms for the CF HB ZVS-MRC operating in Modes I.C, II.A, and II.C, respectively. Table 3.2 summarizes the five-stage sequences of the modes of operation for the CF HB ZVS-MRC. A detailed description of the six modes of operation of the CF HB ZVS-MRC are given in Appendix B.

3.3.2 DC Voltage-Conversion-Ratio

For reasons similar to the ones discussed for the forward topology, the dc voltage conversion ratio curves for the HB topology are obtained by using a numerical algorithm to solve the differential equations for each stage of the sequence representing the eight modes of opera-
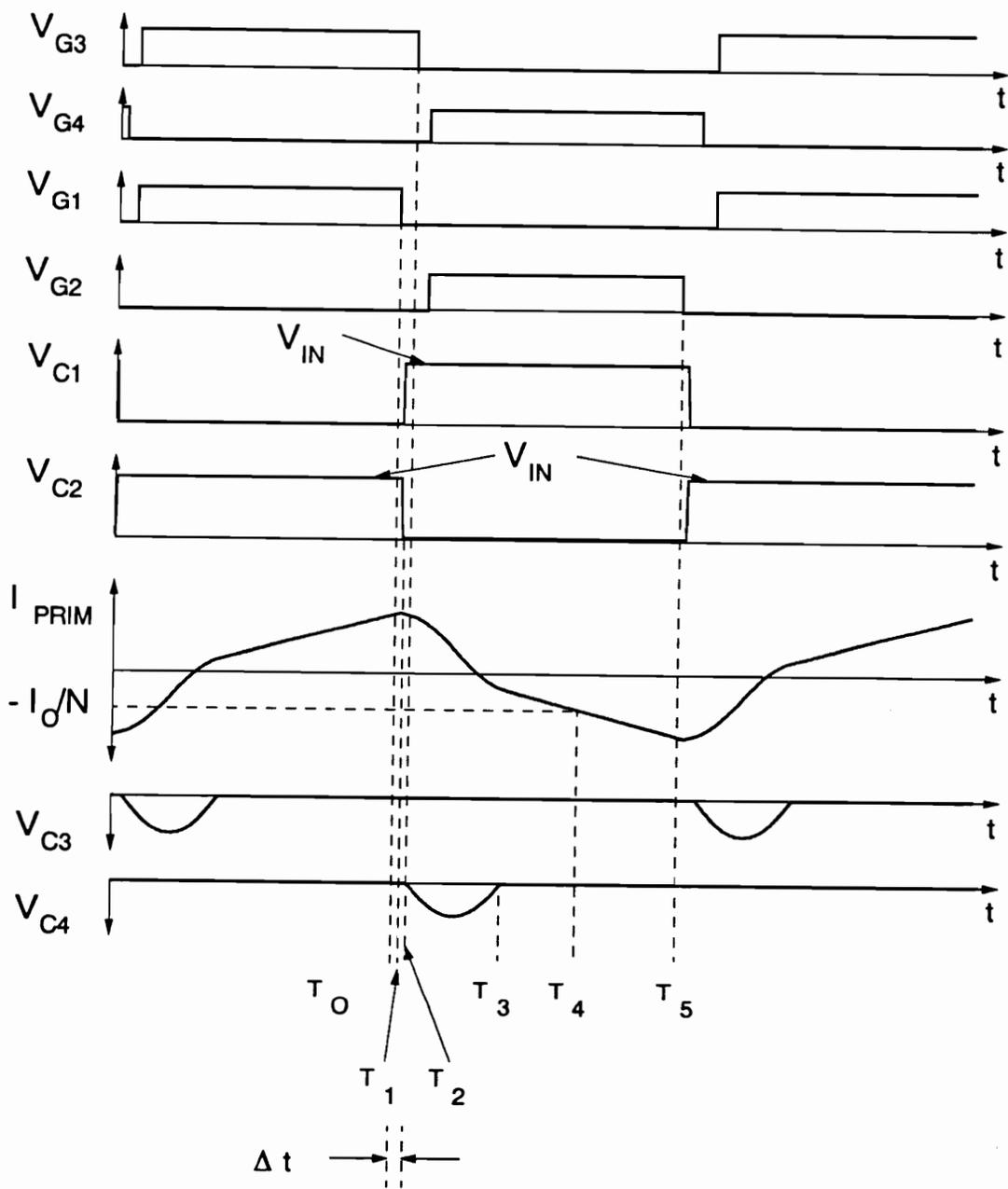
Figure 3.13. Ideal waveforms of the CF HB ZVS-MRC operating in Mode I.C, from top to bottom: gate-source voltage V_{G3}, gate-source voltage V_{G4}, gate-source voltage V_{G1}, gate-source voltage V_{G2}, drain-source voltage of switch Q_1, V_{C1}, drain-source voltage of switch Q_2, V_{C2}, primary current I_{PRIM}, capacitor voltage V_{C3}, and capacitor voltage V_{C4}. Δt is defined as the time elapsed between the turn-off of the primary switch, Q_1 or Q_2, and the corresponding constant frequency switch.
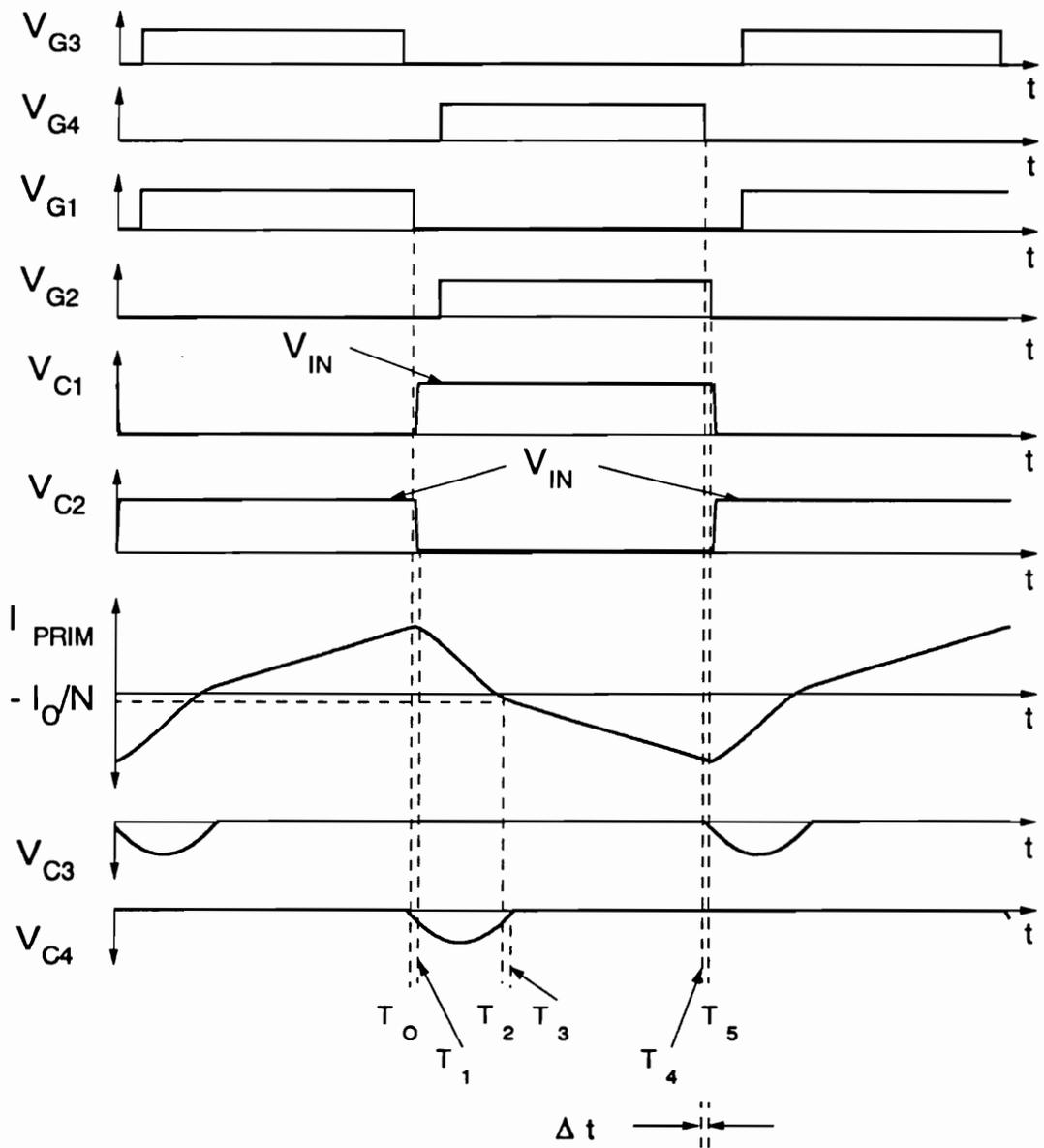
Figure 3.14. Ideal waveforms of the CF HB ZVS-MRC operating in Mode II.A, from top to bottom: gate-source voltage V_{G3}, gate-source voltage V_{G4}, gate-source voltage V_{G1}, gate-source voltage V_{G2}, drain-source voltage of switch Q_1, V_{C1}, drain-source voltage of switch Q_2, V_{C2}, primary current I_{PRIM}, capacitor voltage V_{C3}, and capacitor voltage V_{C4}. Δt is defined as the time elapsed between the turn-off of the primary switch, Q_1 or Q_2, and the corresponding constant frequency switch.
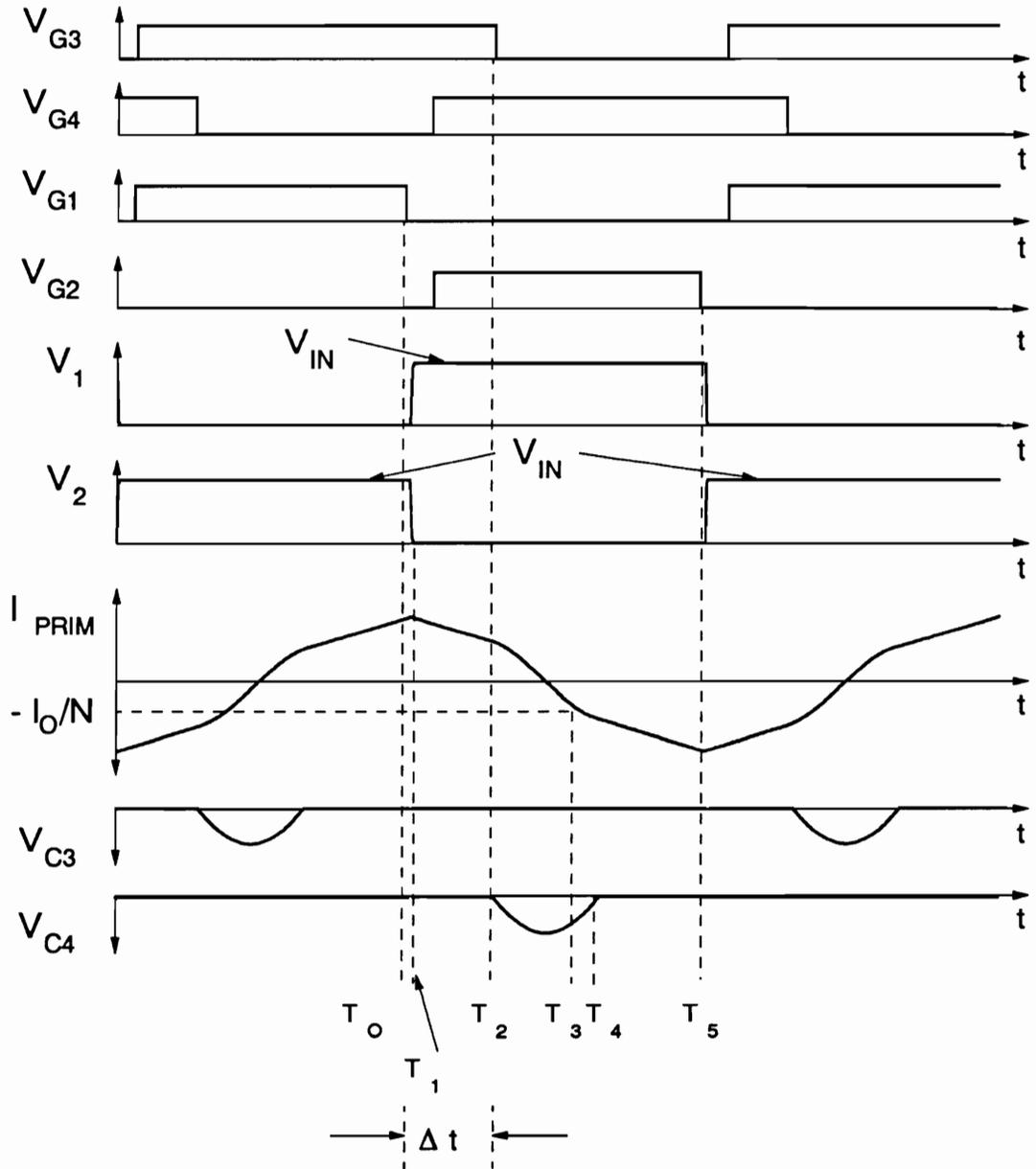
Figure 3.15. Ideal waveforms of the CF HB ZVS-MRC operating in Mode II.C, from top to bottom: gate-source voltage V_{G3}, gate-source voltage V_{G4}, gate-source voltage V_{G1}, gate-source voltage V_{G2}, drain-source voltage of switch Q_1, V_{C1}, drain-source voltage of switch Q_2, V_{C2}, primary current I_{PRIM}, capacitor voltage V_{C3}, and capacitor voltage V_{C4}. Δt is defined as the time elapsed between the turn-off of the primary switch, Q_1 or Q_2, and the corresponding constant frequency switch.

Table 3.2. Modes of operation of the CF HB ZVS-MRC.

MODE	STAGE SEQUENCE
I.A	A - B - C - CF - D
I.B	A - B - C - CF - AF
I.C	AF - CF - B - C - CF
II.A	A - B - BF - CF - D
II.B	A - B - BF - CF - AF
II.C	AF - CF - B - BF - CF

tion. The equations for the topological stages describing the operation of the HB topology are given in Appendix B. Figures 3.16 and 3.17 show the typical dc voltage-conversion-ratio characteristics of the CF HB ZVS-MRC as a function of δ. δ is defined as the time between the turn-off of the CF switch Q_3 or Q_4, and the turn-off of the primary switch Q_1 or Q_2, respectively, (Δt in Fig. 3.11) normalized with respect to $1/f_O$, where the resonant frequency is $f_O = 1/2\pi\sqrt{LC}$. The characteristics are given for different normalized conversion frequencies, f_{con}/f_0, and for different values of $C_N = 2C_D/(CN^2)$, where $f_{con} = 2f_S$ is the conversion frequency, f_S is the switching frequency, and N is the turns ratio of the transformer. The running parameter in Figs. 3.16 and 3.17 is the normalized output current, $I_{ON} = 2Z_O I_O/NV_{IN}$ where $Z_O = \sqrt{L/2C}$ is the characteristic impedance.

Figure 3.16 also shows the regions in the dc voltage-conversion-ratio characteristics where the different modes of operation for the CF HB ZVS-MRC occur. Mode I occurs for heavy load operation and Mode II occurs for lighter load conditions. Modes I.A and II.A occur for positive values of δ and modes I.B, I.C, II.B, and II.C occur for negative values of δ.

A complete set of design characteristics, $C_N = 2, 5, 10$, and 20; and $f_{CON}/f_O = 0.2, 0.25, 0.3$, and 0.35, are given in Appendix B.
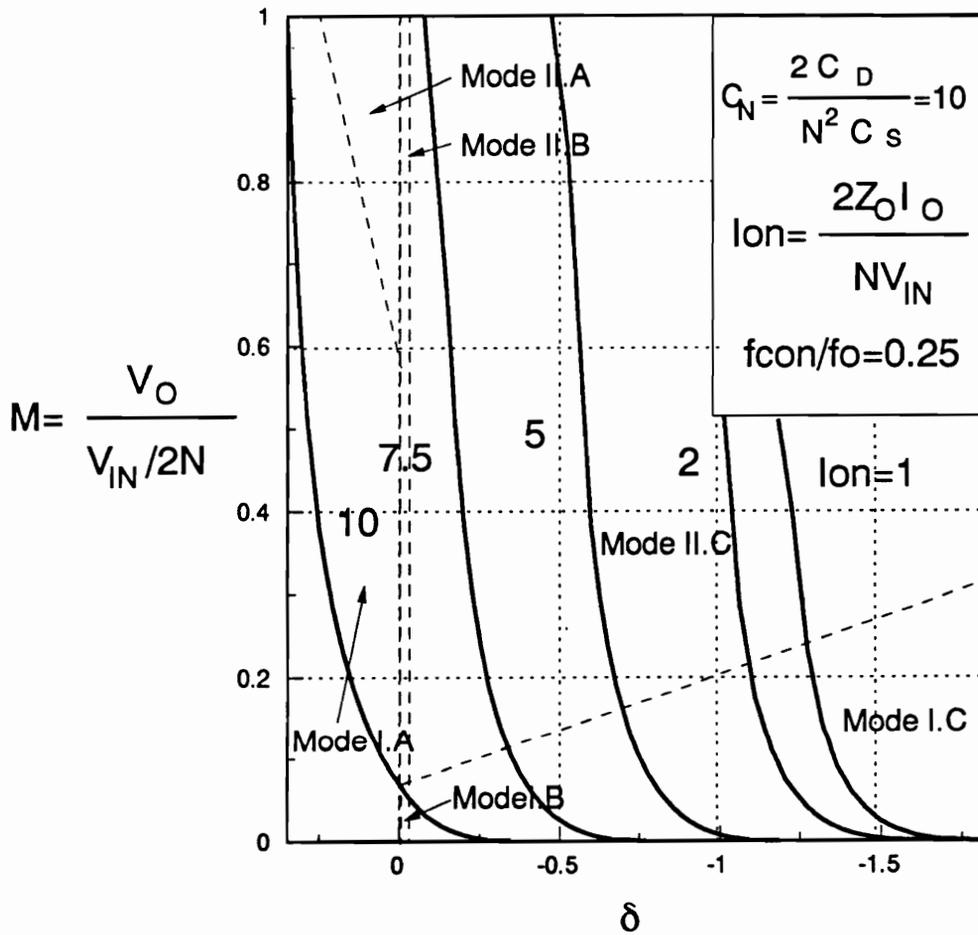
Figure 3.16. DC voltage conversion ratio curve of the CF HB ZVS-MRC showing the regions where the different modes of operation occur; $C_N = 2C_D/(CN^2)$, $I_{ON} = 2I_OZ_O/(V_{IN}N)$, $Z_O = \sqrt{L/2C}$, and $f_O = 1/2\pi\sqrt{2LC}$.
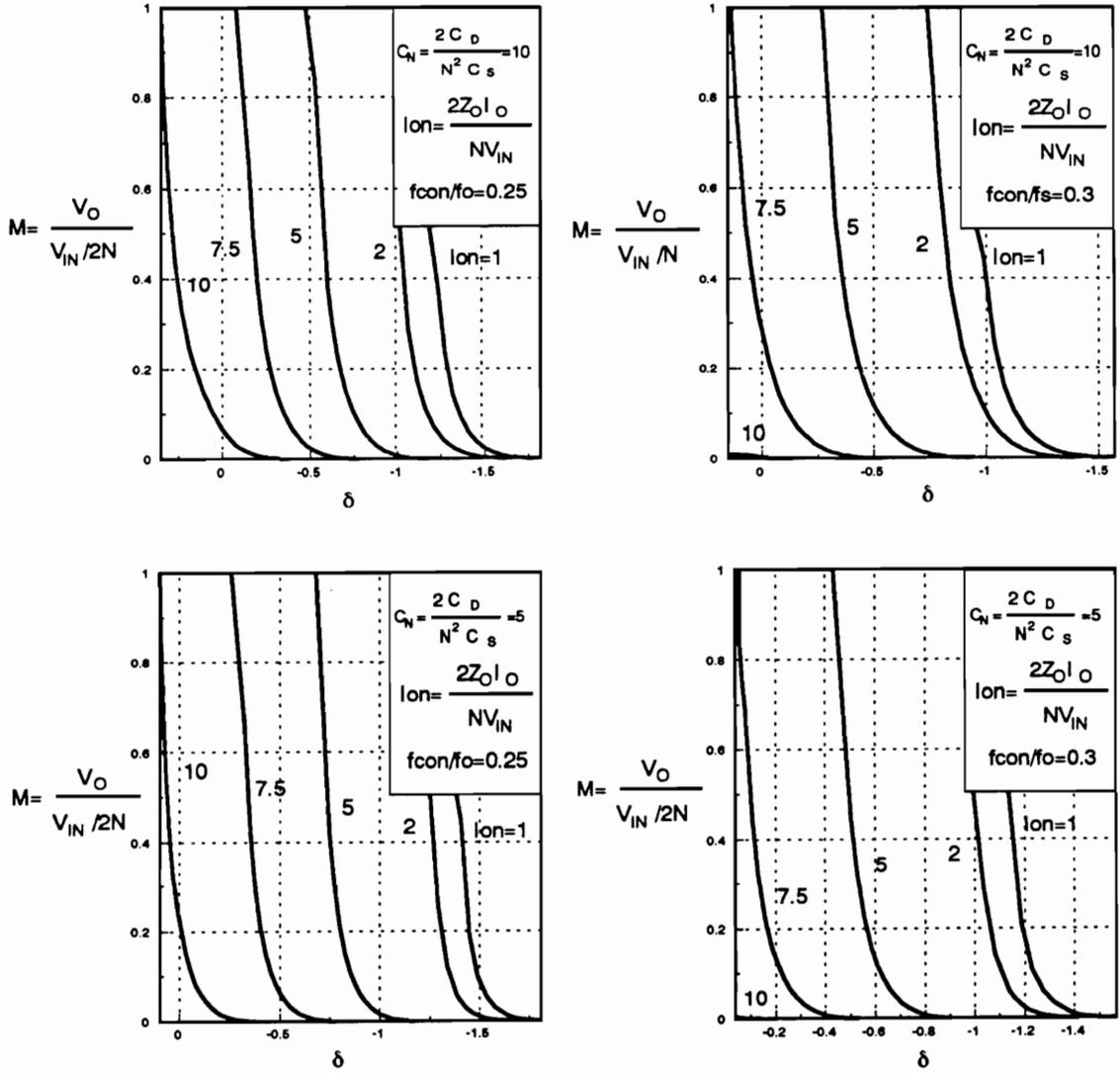
Figure 3.17. DC voltage conversion ratio curves of the CF HB ZVS-MRC for different values of C_N and f_{con}/f_o; $C_N = 2C_D/(CN^2)$, $I_{ON} = 2I_oZ_o/(V_{IN}N)$, $Z_o = \sqrt{L/2C}$, and $f_o = 1/2\pi\sqrt{2LC}$.

3.4 Design Guidelines

In order to determine design guidelines for CF ZVS-MRCs, it is necessary to determine the maximum peak-to-peak currents and voltages for both the active switches and the rectifier diodes. Since CF ZVS-MRCs can be designed for different values of f_s/f_O (f_{con}/f_O for the HB topology) and C_N which results in different device stresses, design trade-offs need to be considered. No analytical expressions for the current and voltage stresses on the different converter components exist for any topology of this new family of converters. Therefore, current and voltage stresses are determined from the numerical solution of the operation of the converters.

To evaluate the effect of the different design parameters on the performance of CF ZVS-MRCs, different design examples for both the forward and HB topologies are considered. A stress analysis of the different design examples provides design trade-offs and guidelines. The designs of the CF forward and HB ZVS-MRC are based on the numerically calculated dc voltage-conversion-ratio characteristics and require the following design specifications:

- input voltage range, $V_{IN}^{max} - V_{IN}^{min}$;
- output voltage, V_O;
- load range, $I_O^{min} - I_O^{max}$; and
- switching frequency, f_s.

The first step in designing the converter is to determine the transformer turns ratio N, C_N, and f_s/f_O (f_{CON}/f_O for the HB topology) using a set of dc characteristics plotted for different C_N and f_s/f_O (f_{CON}/f_O). In order to design an efficient converter, both conduction and magnetic core

losses have to be minimized. In CF ZVS-MRCs, minimizing conduction losses is not a trivial task because of the nonlinear behavior characteristic of these converters and the large amounts of circulating energy resulting from CF and soft switching operation. Normally, to minimize conduction losses on the primary side (primary switch and power transformer), the turns ratio of the transformer is maximized. This requires that the converter be designed for the highest dc voltage conversion ratio. A high turns ratio would suggest low currents flowing in the primary side and consequently minimum conduction losses. But for CF ZVS-MRCs, this is generally not the case.

The magnetic core losses in the resonant inductor and transformer are directly related to the voltage swing across them. This voltage swing also has a nonlinear dependence on C_N and f_S/f_O (f_{CON}/f_O). Furthermore, the voltage swing across L and the transformer in these converters is three to six times the input voltage. This results in considerable core losses that cannot be ignored. In addition, in some single-ended topologies like the flyback, zeta, and forward converters, the transformer operates with an inherent dc bias. This dc bias generally also results in increased core losses. For example, for Q_1 material, a dc bias can increase the core to several times the core loss resulting from an ac excitation [D12,G8].

As the above discussion suggests, the effect of the design parameters (N, C_N, f_S/f_O (f_{CON}/f_O), and Z_O) are interrelated, thus complicating the design of CF ZVS-MRCs. To evaluate the effect of these parameters, the CF forward and HB are designed using different combinations of N, I_{ON}, C_N, and f_S/f_O (f_{CON}/f_O). Stress analyses are then performed to determine design trade-offs and guidelines.

3.4.1 Design Trade-offs for CF Forward ZVS-MRC

Design trade-offs of the forward topology are based on the following design specifications:

- input voltage range, $V_{IN}^{max} - V_{IN}^{min} = 45 - 55$ V;
- output voltage, $V_O = 5$ V;
- load range, $I_O^{min} - I_O^{max} = 2$- 10 A; and
- switching frequency, $f_s = 2$ MHz.

These design specifications represent design parameters for a VLSI application. Figure 3.18 shows the dc voltage-conversion-ratio characteristics of the CF forward ZVS-MRC for $C_N = 5$ and 3, and $f_s/f_O = 0.65$ and 0.7. From the dc voltage conversion ratio characteristics it can be seen that for $C_N = 5$ and $f_s/f_O = 0.7$ a transformer turns ratio less than or equal to one which will translate into high conduction losses. Due to high conduction losses it is obvious that such a characteristic should be avoided when designing a CF ZVS-MRC. From the dc characteristics it can also be seen that a fourth design parameter needs to be determined, i.e., the maximum normalized load current, $I_{ON}^{max} = (I_O^{max} Z_O)/V_{IN}^{min}$. To investigate the effect of N, C_N, f_s/f_O, and I_{ON}^{max} on the converter performance, seven different design examples are considered:

Design # 1: N = 5, $I_{ON}^{max} = 4$, $C_N = 3$, and $f_s/f_O = 0.65$,

Design # 2: N = 8, $I_{ON}^{max} = 3$, $C_N = 3$, and $f_s/f_O = 0.65$,

Design # 3: N = 3, $I_{ON}^{max} = 4$, $C_N = 3$, and $f_s/f_O = 0.65$,

Design # 4: N = 5, $I_{ON}^{max} = 3$, $C_N = 3$, and $f_s/f_O = 0.65$,

Design # 5: N = 2, $I_{ON}^{max} = 3$, $C_N = 5$, and $f_s/f_O = 0.65$,
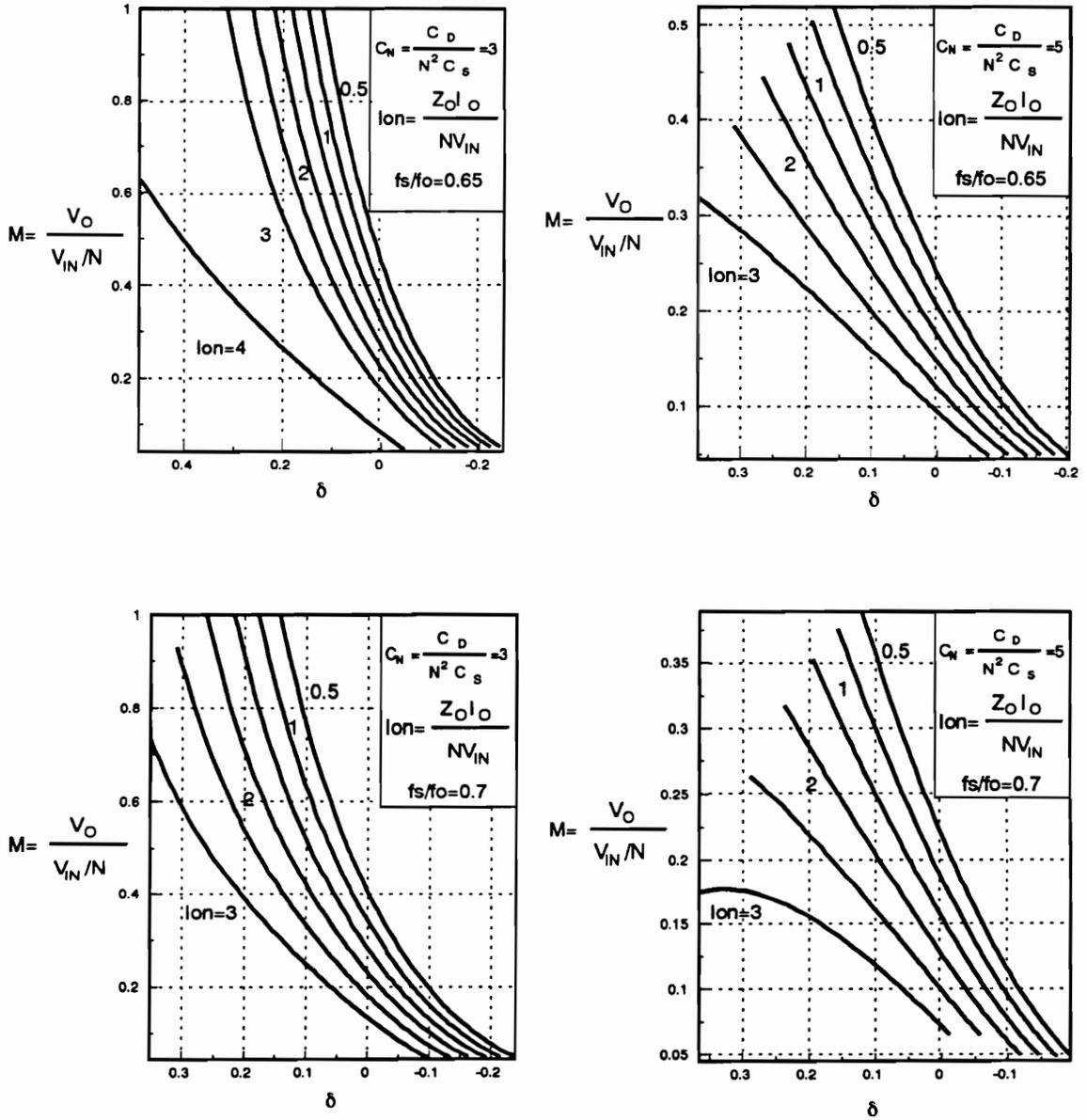
Figure 3.18. DC voltage conversion ratio curve of the CF forward ZVS-MRC for $C_N = 3$ and 5, and $f_S/f_O = 0.65$ and 0.7; $C_N = 2C_D/(CN^2)$, $I_{ON} = 2I_O Z_O/(V_{IN}N)$, $Z_O = \sqrt{L/2C}$, and $f_O = 1/\sqrt{2LC}$.

Design # 6: $N = 2$, $I_{ON}^{max} = 3$, $C_N = 3$, and $f_S/f_O = 0.7$, and

Design # 7: $N = 2$, $I_{ON}^{max} = 4$, $C_N = 3$, and $f_S/f_O = 0.65$.

Figures 3.19 and 3.20 show the operating ranges and stresses for the first four designs which study the effect of selecting different transformer turns ratios and I_{ON}^{max} (Z_O is determined from I_{ON}) values on the current and voltage stresses while C_N and f_S/f_O are kept constant. Since the procedure is identical in each case, only Design #1 is described in detail.

Figure 3.19 shows the dc voltage conversion ratio characteristic for $C_N = 3$ and $f_S/f_O = 0.65$. For a given C_N and f_S/f_O, the minimum conduction time of the CF switch occurs at full load (I_{ON}^{max}) and low line (M_{max}) (point A in Fig. 3.19), whereas the maximum conduction time of this switch occurs at light load ($I_{ON}^{min} = I_{ON}^{max} V_{IN}^{min} I_O^{min}/(V_{IN}^{max} I_O^{max})$) and high line ($M_{min} = M_{max} V_{IN}^{min}/V_{IN}^{max}$) (point C in Fig. 3.19). Points B (high-line and full-load) and D (low-line and light-load) are the two remaining points needed to completely define the operating region on the dc voltage-conversion-ratio curves. Point B is determined by M^{min} and $I_{ON} = (I_{ON}^{max} V_{IN}^{min})/V_{IN}^{max}$. Similarly, point D is determined by M^{max} and $I_{ON} = I_{ON}^{max} I_O^{min}/I_O^{max}$. By selecting M_{max} and I_{ON}^{max}, the operating point at full load and low line is defined. For the first design, the maximum value of the normalized load current was, by arbitrary choice, selected as 4.0. As a result, the operating range extends over the shaded area shown in Fig. 3.19. Every point on the dc voltage-conversion-ratio curves (M, f_S/f_O, and I_{ON}) has a one-to-one correspondence with the points in the current/voltage characteristics. Therefore, any operating region defined in the dc voltage-conversion-ratio curves can be transposed into any of the other characteristics from which the current and voltage stresses associated with a given region of operation can be determined.
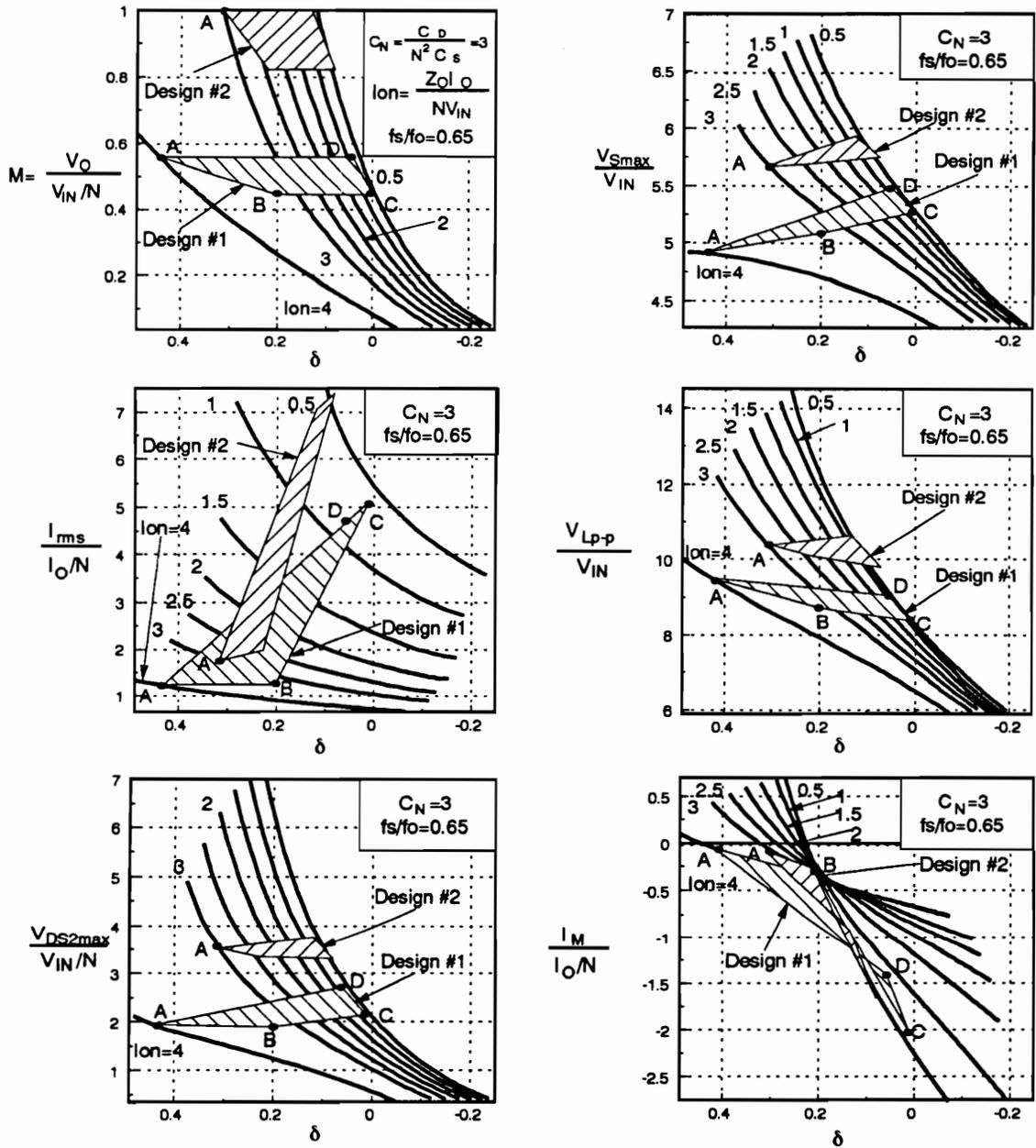
Figure 3.19. Design examples #1 and #2 for the CF forward ZVS-MRC; $C_N = 3$ and $f_S/f_O = 0.65$ showing: maximum normalized primary switch voltage stress V_S^{max}/V_{IN}, primary rms current $I_{PRIM}^{rms}/(I_O/N)$, peak-to-peak normalized resonant inductor voltage V_L^{p-p}/V_{IN}. maximum normalized constant frequency switch voltage stress V_{DS2}^{max}/V_{IN}, and normalized magnetizing current $I_M/(I_O/N)$.

Figures 3.19 - 3.23 show normalized characteristics of the maximum transistor Q_1 voltage, V_S^{max}, peak-to-peak resonant inductor voltage, V_L^{p-p}, transistor Q_2 voltage, V_{DS2}^{max}, resonant inductor rms current, I_{PRIM}^{rms}, and the magnetizing current, I_M. The voltage characteristics are normalized with respect to the input voltage V_{IN}. The current characteristics are normalized with respect to the ratio of I_O/N.

Since the characteristics are normalized, it is difficult to predict the region in which the minimum voltage and current stresses will occur for a given design. The voltage and current stresses can be determined from the shown characteristics by denormalizing the voltages and currents at each corner of the operating region. The resulting currents and voltages for the first four designs are summarized in Table 3.3. The following design trade-offs are inferred:

1) Comparison of designs #1 and #4 suggests that increasing I_{ON}^{max} and holding all other parameters constant (designing for higher Z_O) decreases all voltage and current stresses.

2) Comparison of designs #1 and #3 and designs #2 and #4 suggests that moving down in a line of constant I_{ON} results in decreased voltage stresses but increased current stresses.

3) Finally, comparison of designs #1 and #2 suggests that designing for a higher M_{max} and a lower I_{ON} does not result in lower conduction losses.

For a given C_N and f_S/f_O, the converter should be designed so that full load and low line operation occurs for the minimum conduction time of the CF switch, i.e., design for maximum
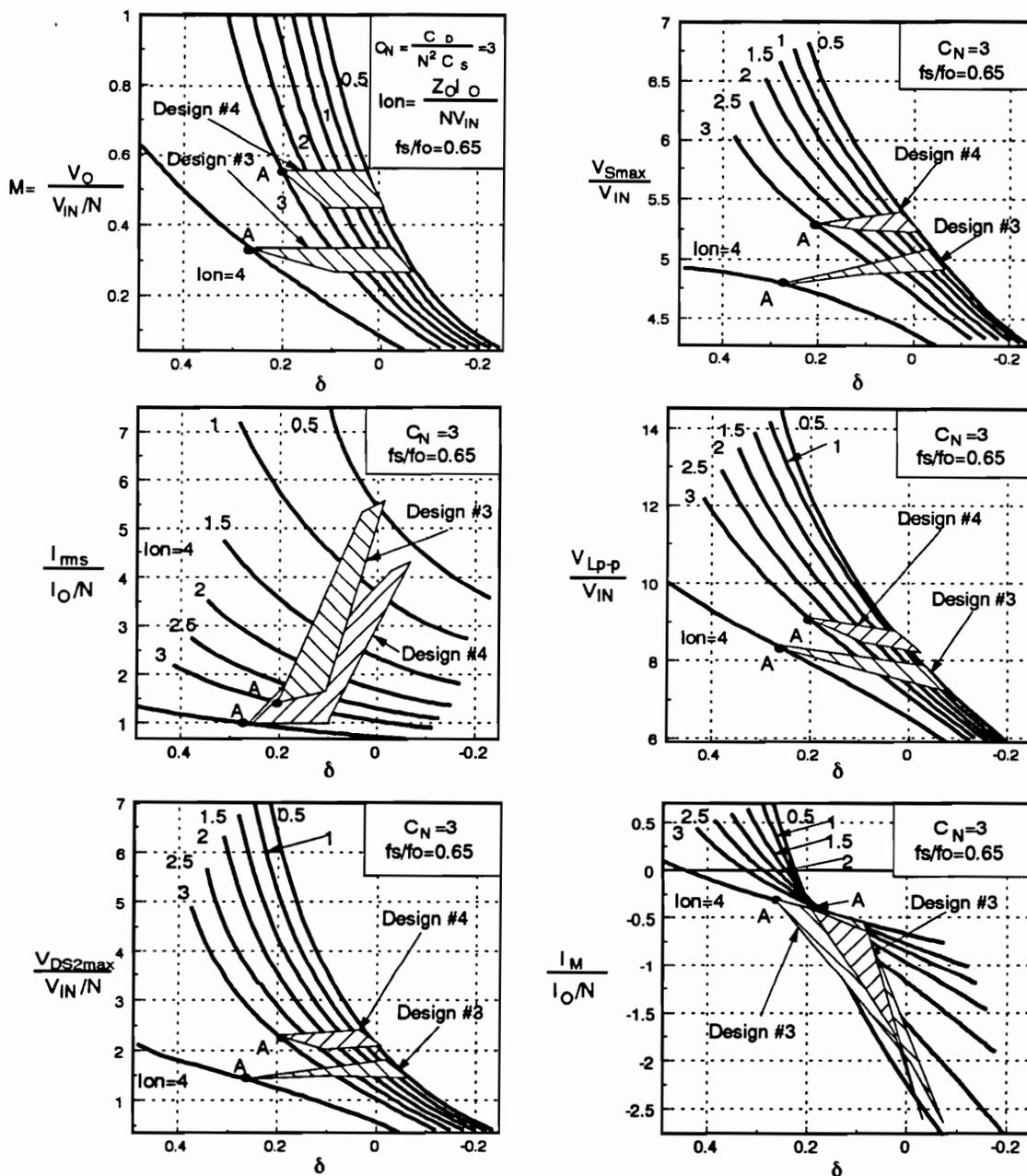
Figure 3.20. Design examples #3 and #4 for the CF forward ZVS-MRC; $C_N = 3$ and $f_S/f_O = 0.65$ showing: maximum normalized primary switch voltage stress V_S^{max}/V_{IN}, primary rms current $I_{PRIM}^{rms}/(I_O/N)$ peak-to-peak normalized resonant inductor voltage V_L^{-P}/V_{IN}. maximum normalized constant frequency switch voltage stress V_{DS2}^{max}/V_{IN}, and normalized magnetizing current $I_M/(I_O/N)$.

Table 3.3. Summary of design examples #1, #2, #3, and #4 for the CF forward ZVS-MRC

		Design #1	Desing #2	Design #3	Design #4
V_S^{max}	HL	280	313	267	289
(V)	LL	220	257	215	237
V_L^{p-p}	HL	481	555	429	462
(V)	LL	425	466	369	406
V_{DS2}^{max}	HL	20.9	20.5	23.0	22.0
(V)	LL	17.6	17.5	22.5	20.2
I_{PRIM}^{rms}	HL	2.6	2.2	3.4	3.2
(A)	LL	2.5	2.0	3.3	2.8
I_M	HL	-0.60	-0.33	-2.00	-1.30
(A)	LL	-0.16	-0.11	-1.00	-0.80

HL - High-Line (55 V)
LL - Low-Line (45 V)
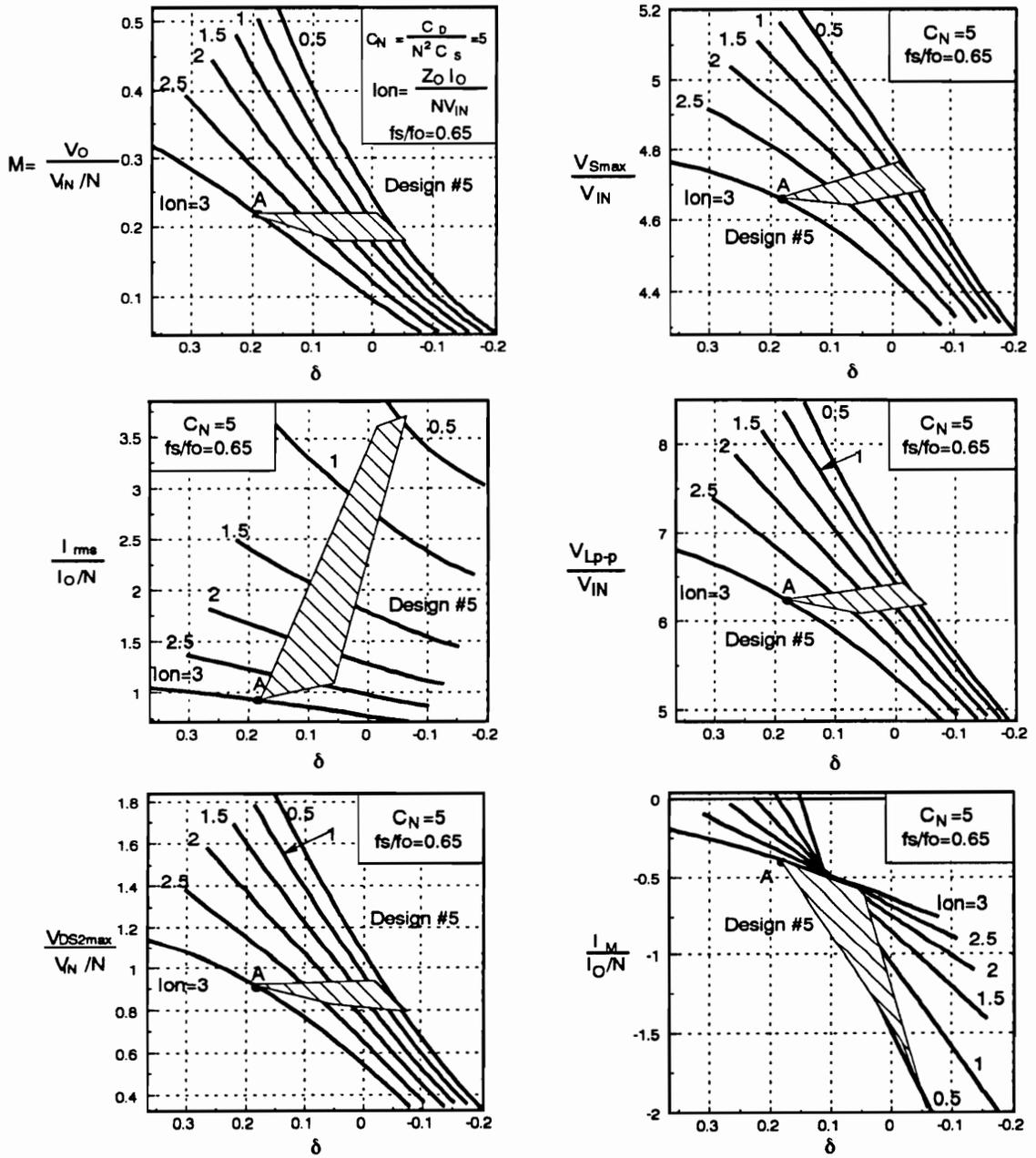
Figure 3.21. Design example #5 for the CF forward ZVS-MRC; $C_N = 5$ and $f_S/f_O = 0.65$ showing: maximum normalized primary switch voltage stress V_S^{max}/V_{IN}, primary rms current $I_{PRIM}^{rms}/(I_O/N)$, peak-to-peak normalized resonant inductor voltage V_L^{p-p}/V_{IN}. maximum normalized constant frequency switch voltage stress V_{DS2}^{max}/V_{IN}, and normalized magnetizing current $I_M/(I_O/N)$.
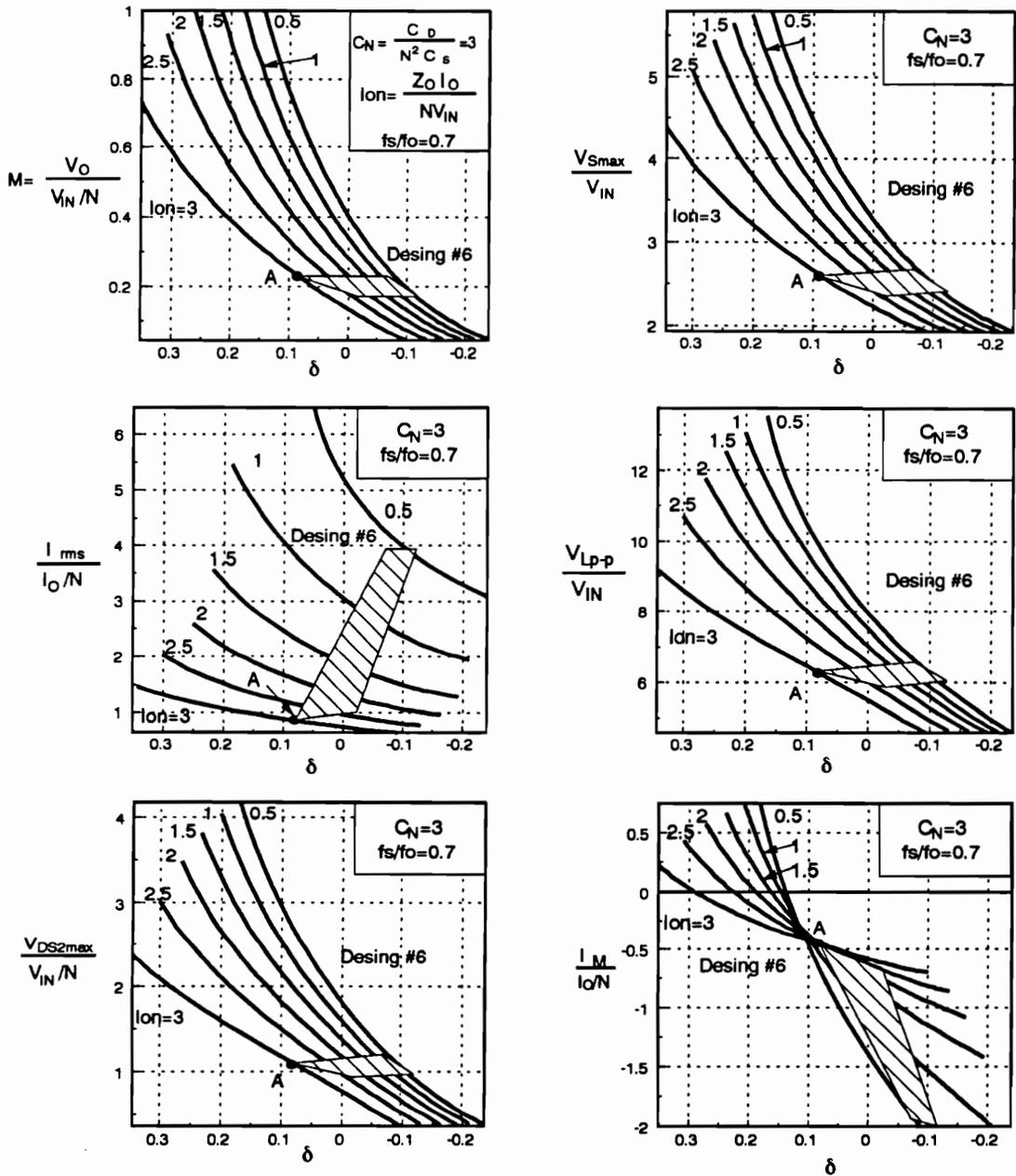
Figure 3.22. Design example #6 for the CF forward ZVS-MRC; $C_N = 3$ and $f_S/f_O = 0.7$ showing: maximum normalized primary switch voltage stress V_S^{max}/V_{IN}, primary rms current $I_{PRIM}^{rms}/(I_O/N)$, peak-to-peak normalized resonant inductor voltage V_L^{p-p}/V_{IN}. maximum normalized constant frequency switch voltage stress V_{DS2}^{max}/V_{IN}, and normalized magnetizing current $I_M/(I_O/N)$.
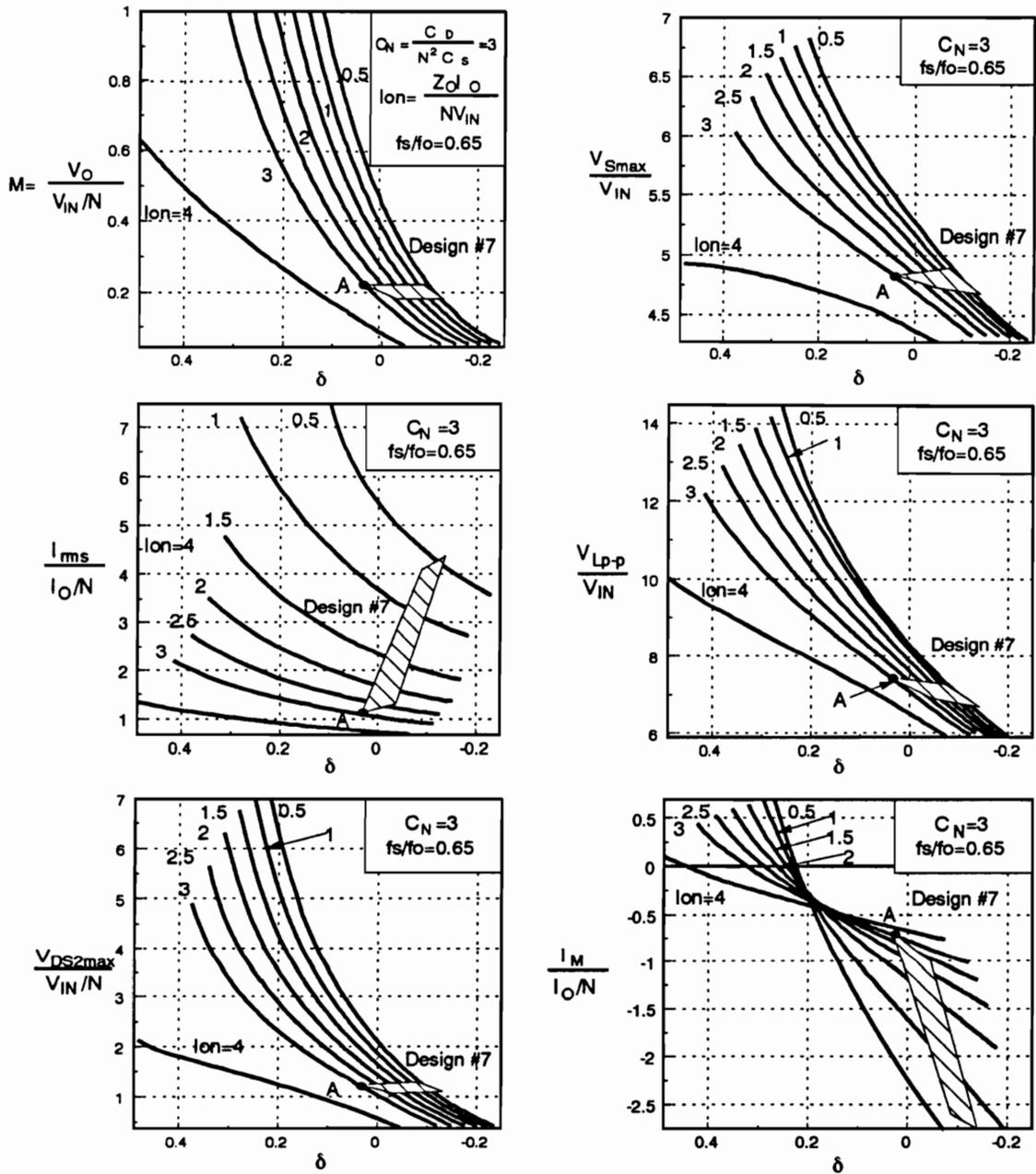
Figure 3.23. Design example #7 for the CF forward ZVS-MRC; $C_N = 5$ and $f_S/f_O = 0.55$ showing: maximum normalized primary switch voltage stress V_S^{max}/V_{IN}, primary rms current $I_{PRIM}^{rms}/(I_O/N)$, peak-to-peak normalized resonant inductor voltage V_L^{p-p}/V_{IN}, maximum normalized constant frequency switch voltage stress V_{DS2}^{max}/V_{IN}, and normalized magnetizing current $I_M/(I_O/N)$.

M_{max} in the highest I_{ON} curve that does not result in unstable operation. It is obvious from the transformer power transfer characteristics that this I_{ON} line results in the lowest amounts of circulating energy.

In order to determine the effect of selecting different values of C_N and f_S/f_O, three more design examples were considered. Figures 3.21 - 3.23 show the operating regions and stress analysis for these three designs. The current and voltage stresses resulting from these design examples are summarized in Table 3.4. Thus, it can be concluded that increasing C_N and f_S/f_O increases both current and voltage stresses. The minimum practical value of f_S/f_O is determined by the minimum frequency of operation (stable operation) of the conventional forward ZVS-MRC designed for the same value of C_N. As the conduction time of the constant frequency switch decreases to zero, the operation of the CF forward ZVS-MRC parallels that of the conventional forward ZVS-MRC.

One very important result derived from the dc analysis is the determination of the characteristics of the normalized dc magnetizing current, $I_{MN} = I_M/(I_O/N)$. Zero dc bias operation is important, as suggested before, because the core loss for some materials is very dependent on the dc bias. For the conventional forward ZVS-MRC it can be seen that for $M = 0.5$, I_{MN} is approximately zero regardless of the load (switching frequency changes with the load resistance). Furthermore, for $M > 0.5$, I_{MN} is positive, while for $M < 0.5$ it is negative. For M different than 0.5, the magnitude of I_{MN} increases when the load current increases. This behavior of the magnetizing current in the conventional forward ZVS-MRC can be explained as follows:

$$I_{MN} = I_{IN} - DI_O = I_O(M - D) \tag{3.1}$$

Table 3.4. Summary of design examples #5, #6, and #7 for the CF forward ZVS-MRC

		Design #5	Desing #6	Design #7
V_S^{max}	HL	244	129	260
(V)	LL	209	117	216
V_L^{p-p}	HL	335	324	382
(V)	LL	281	283	332
V_{DS2}^{max}	HL	22.6	26.1	29.7
(V)	LL	20.4	24.7	28.1
I_{PRIM}^{rms}	HL	5.5	4.9	6.0
(A)	LL	4.6	4.2	5.5
I_M	HL	-3.0	-3.5	-5.0
(A)	LL	-2.0	-2.2	-3.6

HL - High-Line (55 V)
LL - Low-Line (45 V)

where I_O is the dc output current and D is defined as the conduction time of the forward diode relative to the switching period. It can be seen that the magnetizing current becomes zero when M = D. This condition holds for M = 0.5. since D is approximately 0.5 for the conventional forward ZVS-MRC. However, D is not necessarily equal to 0.5 for the CF forward ZVS-MRC since the control of the conduction time of the rectifier devices is what allows for CF operation. In the CF forward ZVS-MRC $I_{MN} \simeq 0$ occurs only for light conduction times of the CF switch. Consequently, the region where I_{MN} is zero is limited to maximum values of δ and dc voltage-conversion-ratios between 0.65 and 0.45. This suggests that for partial to light load operation, the magnetizing current in the CF forward ZVS-MRC will be strongly biased negatively.

Finally, one last trade-off that should be considered in all single-ended topologies is that of the voltage stress across switch Q_1. From the different design examples it can be observed that for these design specifications it is very difficult to design a CF forward ZVS-MRC with a primary switch voltage stress, V_S^{max}, lower than 200 V. If this stress is limited below 200 V a device rated for 200 V can be used, otherwise, a 400 V device is needed. Generally a 200 V device has a much lower $R_{DS(ON)}$, approximately half of that of a 400 V device. Therefore, using a 200 V device could considerably reduce the conduction losses. As the design examples suggest, reducing the voltage stresses usually increases conduction losses. This means that for single ended topologies, like the forward converter, the designer has to decide if lowering the primary voltage stress so that a lower $R_{DS(ON)}$ device can be used will decrease the overall conduction losses. No general rule can be given in this case, since the answer is very case dependent due to the discrete nature of the device ratings.

3.4.2 Design Procedure for CF Forward ZVS-MRC

A design procedure can be established for the CF forward ZVS-MRC based on the trade-offs described in the previous section. Four rules should be followed while designing the CF forward ZVS-MRC:

1) A dc voltage-conversion-ratio characteristic curve that allows for the converter to be designed for $I_M = 0$ under full load conditions should be selected.

2) The power stage characteristic impedance Z_O should be maximized; i.e., the low-line full-load operating condition should be designed to fall in the maximum I_{ON} curve that does not result in unstable operation.

3) The value of C_N and f_S/f_O should be selected to be as low as possible to minimize conduction losses due to circulating energy.

4) The turns ratio of the transformer should be selected so that nominal line and full-load operating condition result in $I_M = 0$ (reduces core losses resulting from the dc bias at nominal-line and full-load operating condition).

Once C_N, f_s/f_O, M_{max}, and I_{ON}^{max} have been selected, the turns ratio of the transformer is calculated from:

$$N = \frac{V_{IN}^{nom} M_{@(I_M = 0)}}{V_O} \tag{3.2}$$

where V_{IN}^{nom} is the nominal input voltage. From the definition for C_N, f_O, and I_{ON}^{max}, it follows that:

$$L = \frac{N I_{ON}^{max} V_{IN}^{min}}{2\pi f_O I_O^{max}} \tag{3.3}$$

$$C_S = \frac{I_O^{max}}{2\pi f_O N I_{ON}^{max} V_{IN}^{min}} \tag{3.4}$$

and

$$C_D = C_S C_N^{min} \tag{3.5}$$

The voltage ratings of the semiconductor devices can be easily determined from the complete set of given characteristics. For simplicity, the peak current through the primary switch can be estimated using the following expression:

$$I_{Q1}^{pk} < \frac{V_{IN}^{max}}{2Lf_S} \tag{3.6}$$

where the maximum current through the CF switch is:

$$I_{Q2}^{pk} < N I_{Q1}^{pk} \tag{3.7}$$

Finally, the input and output filters are designed following rules similar to those for PWM converters.

3.4.3 Design Trade-offs for CF HB ZVS-MRC

There are two main differences between the design of push-pull topologies like the HB converter and the design of the CF forward ZVS-MRC. First, the transformer in push-pull topologies operates with no dc bias. Second, the voltage stress across the primary switches is clamped to the value of the input voltage. Not having to consider these two issues simplifies the design of the HB converter and all other push-pull topologies.

Design trade-offs of the HB topology are based on the following design specifications:

- input voltage range, $V_{IN}^{max} - V_{IN}^{min} = 270\text{-}330$ V;
- output voltage, $V_O = 5$ V;
- load range, $I_O^{min} - I_O^{max} = 0 \text{ - } 20$ A; and
- switching frequency, $f_s = 750$ kHz.

Figure 3.24 shows the dc characteristics of the CF HB ZVS-MRC for $C_N = 10$ and 5, and $f_{con}/f_O = 0.3$ and 0.25. To investigate the effect of N, C_N, f_{con}/f_O, and I_{ON}^{max} on the converter performance, eight different design examples are considered:

Design # 1: $N = 13$, $I_{ON}^{max} = 10$, $C_N = 5$, and $f_{con}/f_O = 0.25$,

Design # 2: $N = 27$, $I_{ON}^{max} = 10$, $C_N = 5$, and $f_{con}/f_O = 0.25$,
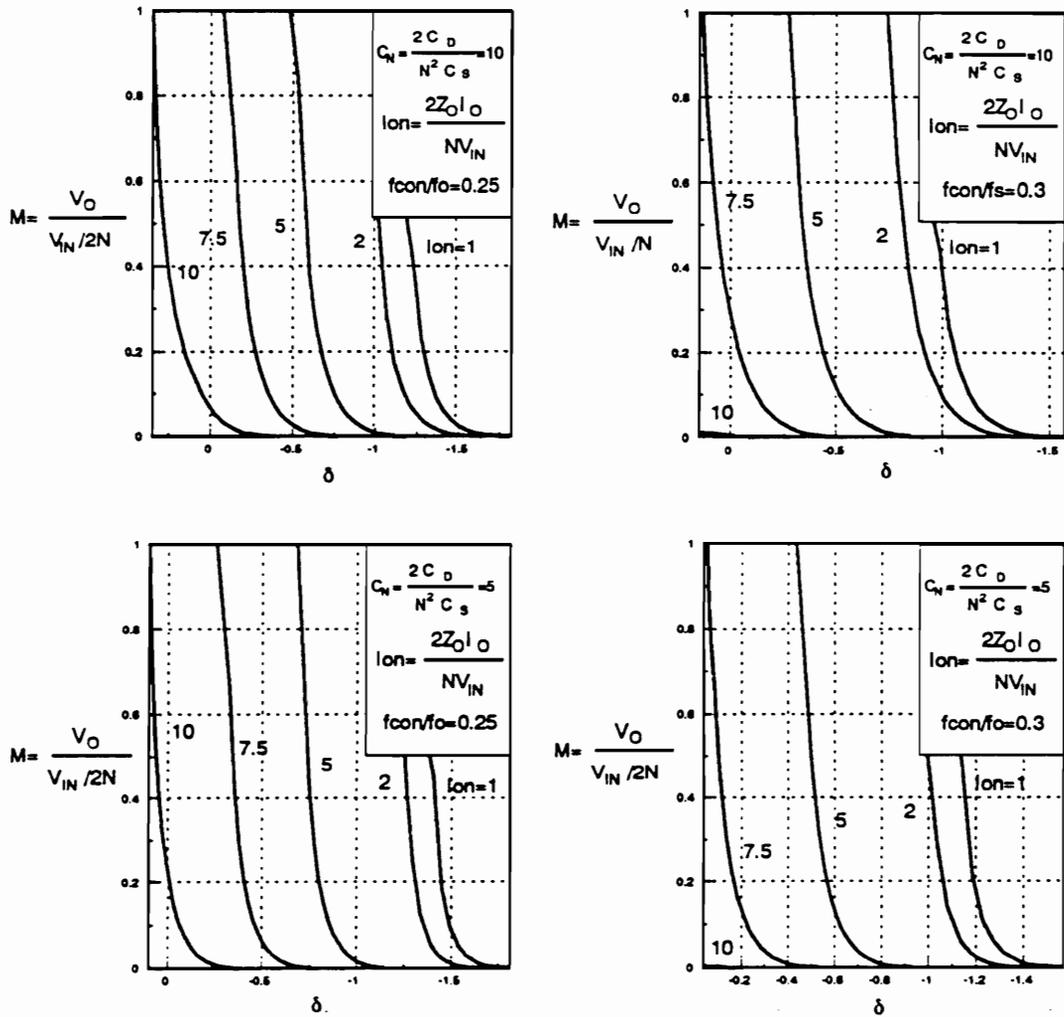
Figure 3.24. DC voltage conversion ratio curve of the CF forward ZVS-MRC for $C_N = 10$ and 5, and $f_s/f_O = 0.3$ and 0.25; $C_N = 2C_D/(CN_2)$, $I_{ON} = 2I_OZ_O/(V_{IN}N)$, $Z_O = \sqrt{L/2C}$, and $f_O = 1/2\pi\sqrt{2LC}$.

Design # 3: $N = 5$, $I_{ON}^{max} = 10$, $C_N = 5$, and $f_{con}/f_O = 0.25$,

Design # 4: $N = 13$, $I_{ON}^{max} = 7.5$, $C_N = 5$, and $f_{con}/f_O = 0.25$,

Design # 5: $N = 13$, $I_{ON}^{max} = 10$, $C_N = 10$, and $f_{con}/f_O = 0.25$,

Design # 6: $N = 13$, $I_{ON}^{max} = 7.5$, $C_N = 5$, and $f_{con}/f_O = 0.3$, and

Design # 7: $N = 13$, $I_{ON}^{max} = 7.5$, $C_N = 10$, and $f_{con}/f_O = 0.3$.

Figures 3.25 - 3.29 show normalized characteristics of the peak-to-peak resonant inductor voltage, V_L^{p-p}/V_{IN}, peak-to-peak primary transformer voltage, V_{PRIM}^{p-p}/V_{IN}, and the primary rms current, $I_{PRIM}^{rms}/(I_O/N)$.   The voltage characteristics are normalized with respect to the input voltage, V_{IN}. The current characteristics are normalized with respect to the load current reflected into the primary side, I_O/N.

Figures 3.25 - 3.27 show the operating ranges and stresses for the first four designs. Again, the first four designs study the effect of selecting different transformer turns ratios N and I_{ON}^{max} on the current and voltage stresses while C_N and f_{con}/f_O remain constant. Table 3.5 summarizes the voltage and current stresses resulting from designs #1 - #4. From the results shown in these tables, the following design trade-offs are observed:

1) Comparison of designs #1 and #4 suggests that increasing I_{ON}^{max} with all other parameters held constant decreases all voltage and current stresses.

2) Comparison of designs #1, #2, and #3 suggests that moving down in a line of constant I_{ON} results in decreased voltage stresses but increased current stresses.
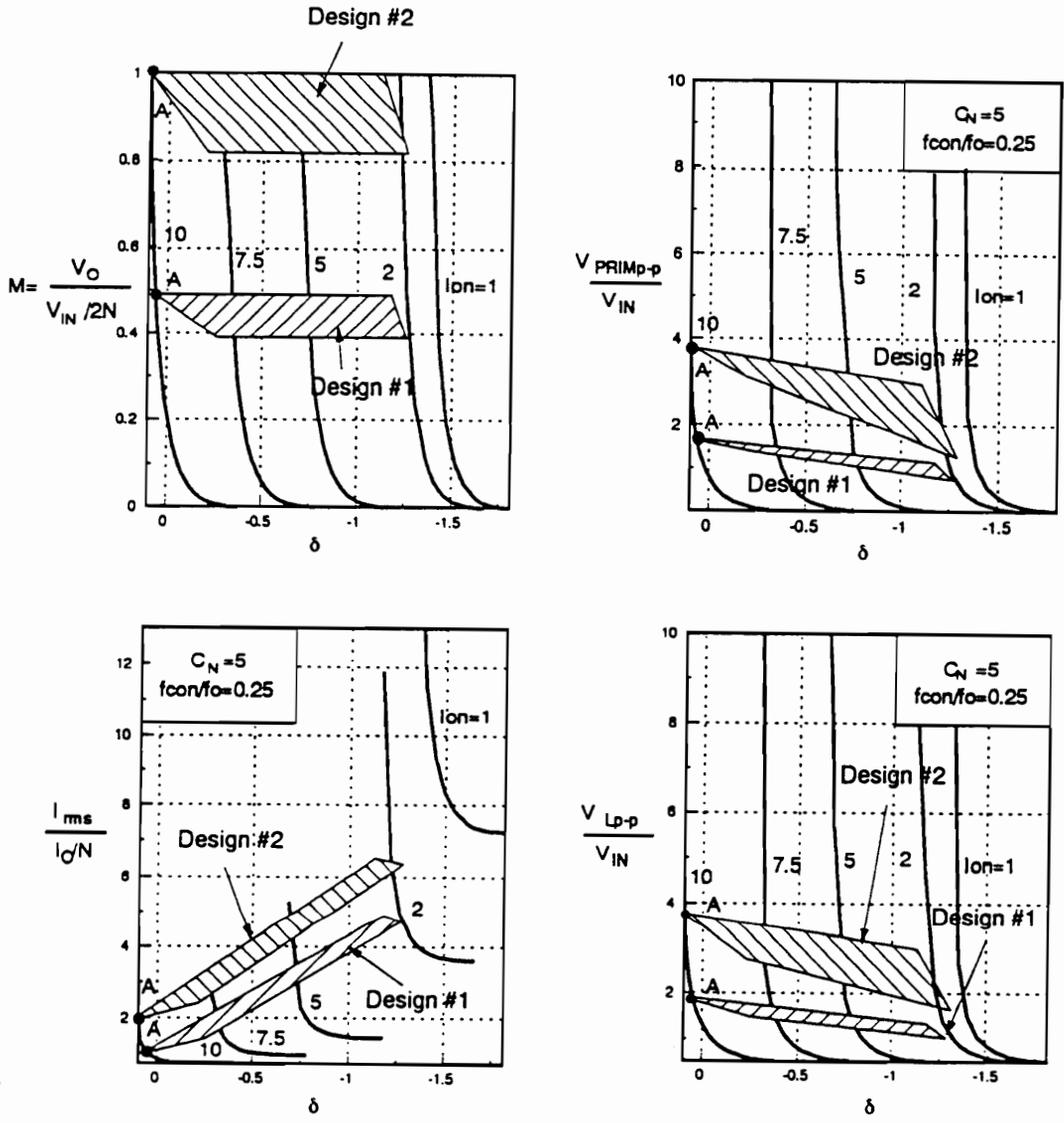
Figure 3.25. Design examples #1 and #2 for the CF HB ZVS-MRC; $C_N = 5$ and $f_S/f_O = 0.25$ showing: dc voltage conversion ratio $V_O/(V_{IN}/2N)$, peak-to-peak normalized primary transformer voltage V_{PRIM}^{p-p}/V_{IN}, primary rms current $I_{PRIM}^{rms}/(I_O/N)$, and peak-to-peak normalized resonant inductor voltage V_L^{p-p}/V_{IN}.
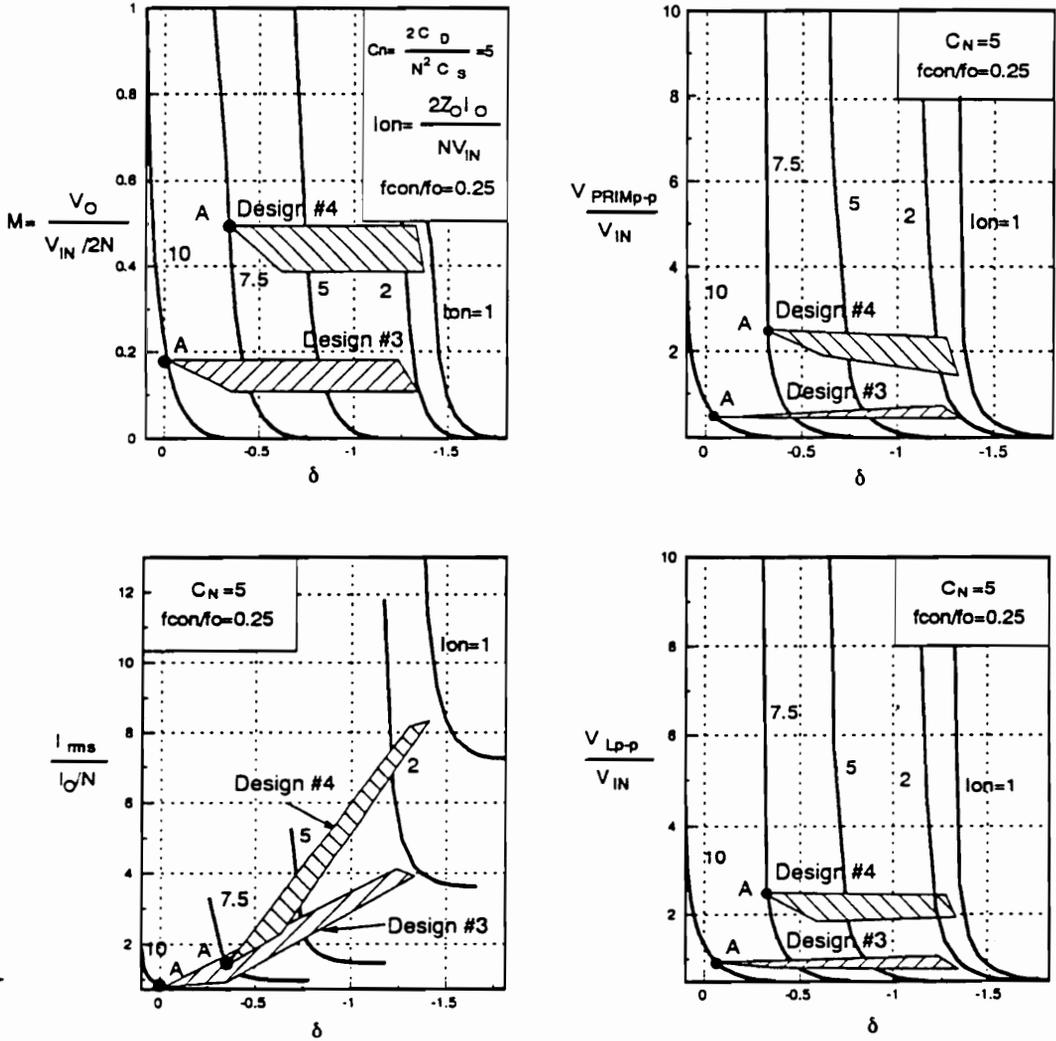
Figure 3.26. Design examples #3 and #4 for the CF HB ZVS-MRC; $C_N = 5$ and $f_S/f_O = 0.25$ showing: dc voltage conversion ratio $V_O/(V_{IN}/2N)$, peak-to-peak normalized primary transformer voltage V_{PRIM}^{p-p}/V_{IN}, primary rms current $I_{PRIM}^{rms}/(I_O/N)$, and peak-to-peak normalized resonant inductor voltage V_L^{p-p}/V_{IN}.

Table 3.5. Summary of design examples #1, #2, #3, and #4 for the CF HB ZVS-MRC.

		Design #1	Desing #2	Design #3	Design #4
V_{PRIM}^{p-p}	HL	396	1053	165	627
(V)	LL	540	115	162	675
V_L^{p-p}	HL	544.5	1023	303	643
(V)	LL	634.5	796.5	257	675
I_{PRIM}^{rms}	HL	1.85	1.74	3.88	3.23
(A)	LL	1.62	1.48	3.8	2.23

HL - High-Line (330 V)
LL - Low-Line (270 V)
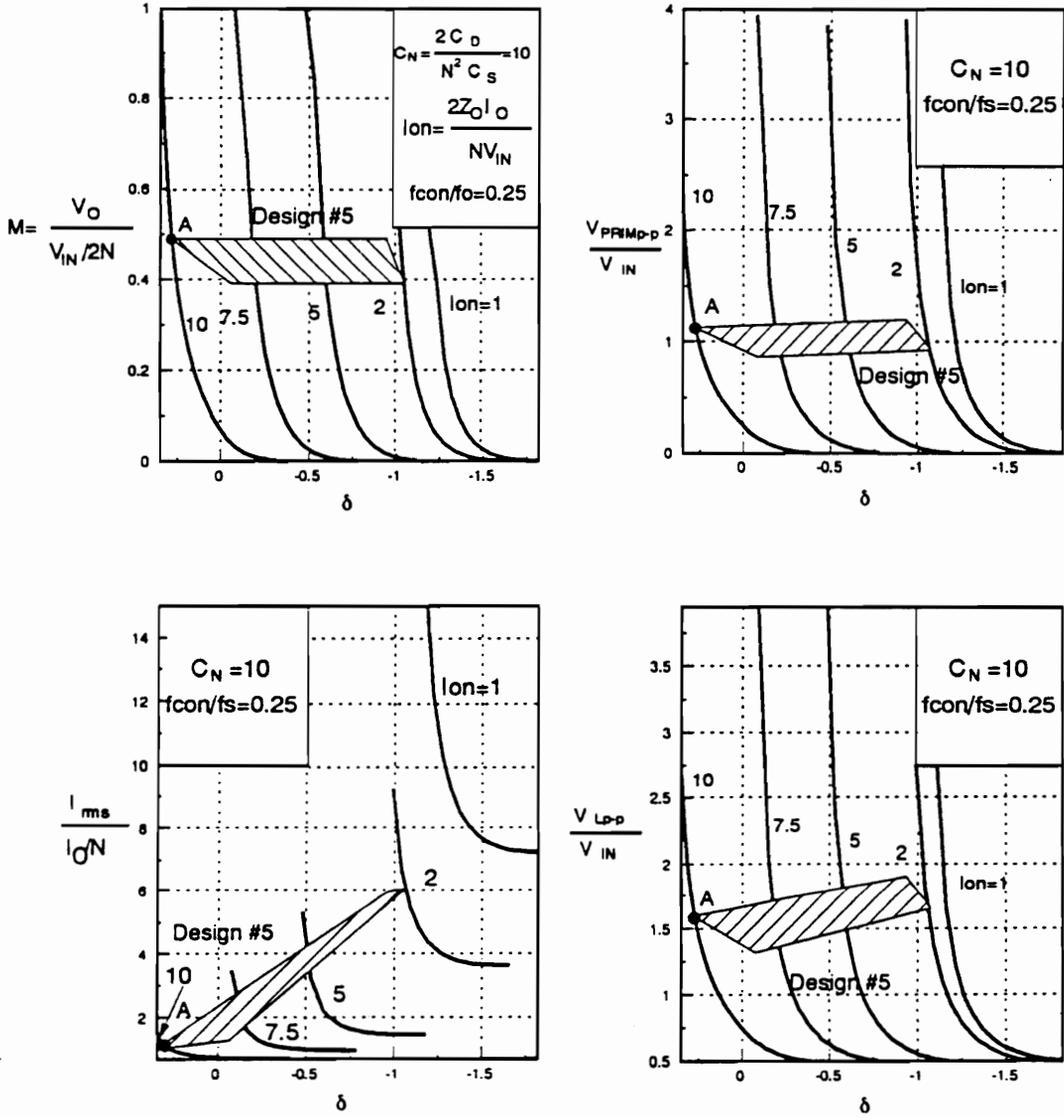
Figure 3.27. Design example #5 for the CF HB ZVS-MRC; $C_N = 10$ and $f_S/f_O = 0.25$: showing: dc voltage conversion ratio $V_O/(V_{IN}/2N)$, peak-to-peak normalized primary transformer voltage $V\beta_{\bar{R}\bar{I}\bar{M}}/V_{IN}$, primary rms current $I_{PRIM}^{rms}/(I_O/N)$, and peak-to-peak normalized resonant inductor voltage V_L^{p-p}/V_{IN}.
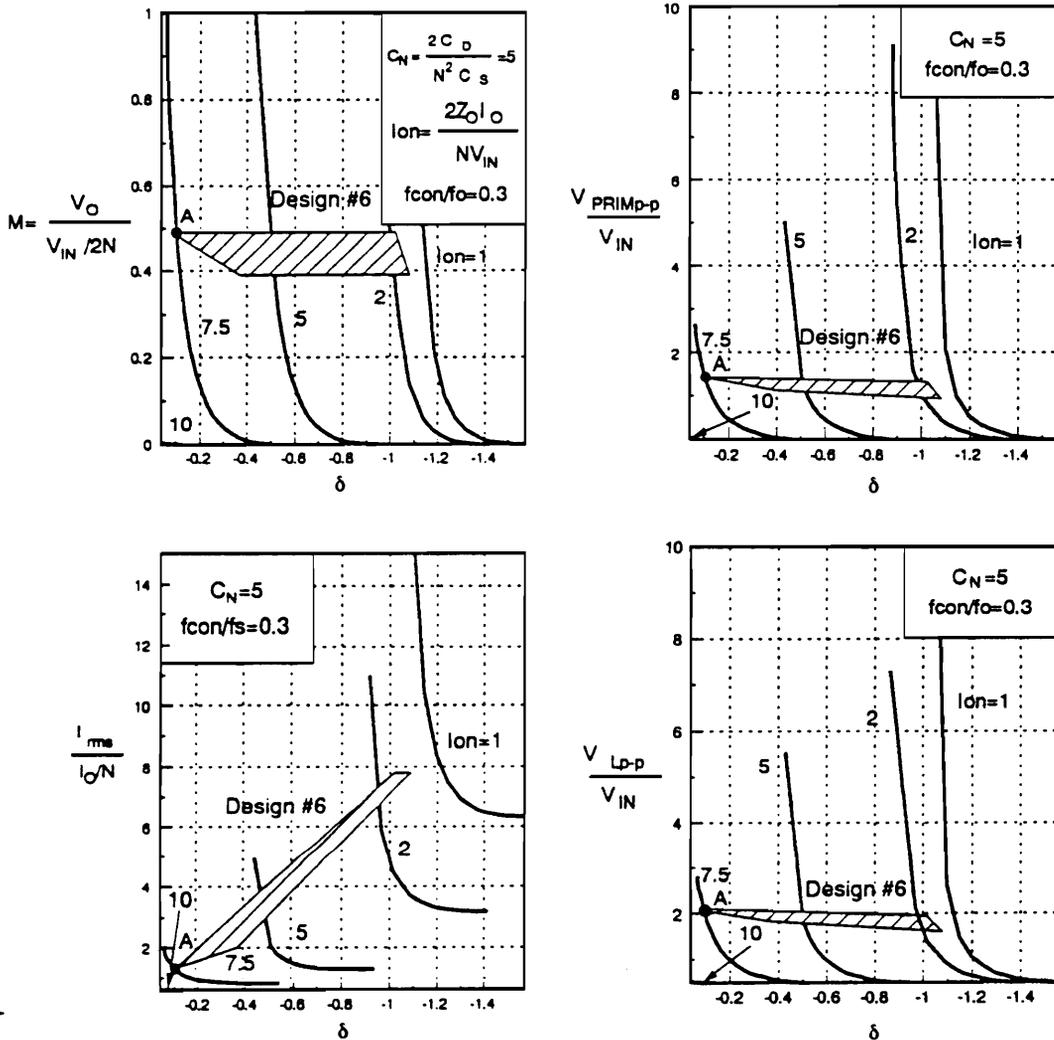
Figure 3.28. Design example #6 for the CF HB ZVS-MRC; $C_N = 5$ and $f_s/f_0 = 0.3$ showing: dc voltage conversion ratio $V_O/(V_{IN}/2N)$, peak-to-peak normalized primary transformer voltage V_{PRIM}^{p-p}/V_{IN}, primary rms current $I_{PRIM}^{rms}/(I_O/N)$, and peak-to-peak normalized resonant inductor voltage V_L^{p-p}/V_{IN}.

Figure 3.29. Design example #7 for the CF HB ZVS-MRC; $C_N = 10$ and $f_S/f_O = 0.3$ showing: dc voltage conversion ratio $V_O/(V_{IN}/2N)$, peak-to-peak normalized primary transformer voltage V_{PRIM}^{p-p}/V_{IN}, primary rms current $I_{PRIM}^{rms}/(I_O/N)$, and peak-to-peak normalized resonant inductor voltage V_L^{p-p}/V_{IN}.

The effect of the design parameters I_{ON}^{max} and N on the value of the current and voltages is similar to the one displayed by the CF forward ZVS-MRC. The difference lies in that the dc voltage conversion ratio characteristics for the HB topology are much steeper than those of the forward topology. Although the dc voltage conversion ratio characteristics of the HB topology are very steep, the normalized primary rms current characteristics remain relatively flat for high values of I_{ON}. This means that as the converter design is changed and higher values of M are selected, the value of the primary rms current will decrease but at a much slower rate than the increase in M. As can be seen from the results of designs #1 and #2, the value of the maximum primary rms current at full load decreases from 1.84 in Design #1 to 1.74 in Design #2. However, the value of the turns ratio increases from 13 in Design #1 to 27 in Design #2. This means that the winding resistance resulting from Design #2 is more than twice the one for Design #1. Therefore, Design #1 will more likely result in decreased overall conduction losses.

The effect of selecting different C_N and f_{con}/f_O is studied in designs #5, #6, and #7 and is shown in Figs. 3.27 - 3.29. The results from these designs are summarized in Table 3.6. As can be seen from Table 3.6, the effect of C_N and f_{con}/f_O in the design of the HB is similar to the one observed for the forward converter, i.e., increasing C_N and f_{con}/f_O increases the voltage and current stresses.

Since the maximum voltage of the primary switches in the CF half-bridge ZVS-MRC is limited to the maximum input voltage (V_{IN}^{max}), the voltage stress of the switches is independent of the load current.

Table 3.6. Summary of design examples #5, #6, and #7 for the CF HB ZVS-MRC.

		Design #5	Desing #6	Design #7
V_{PRIM}^{p-p}	HL	247.5	726	247.5
(V)	LL	371.3	576	297
V_L^{p-p}	HL	412.5	990	429
(V)	LL	438.8	540	405
I_{PRIM}^{rms}	HL	2.24	2.92	3.0
(A)	LL	1.84	1.88	2.03

HL - High-Line (330 V)
LL - Low-Line (270 V)

3.4.4 Design Procedure for CF HB ZVS-MRC

From the design trade-off study, the following rules should be used in designing a CF HB ZVS-MRC:

1) The value of C_N and f_{con}/f_O should be selected to be as low as possible to minimize conduction losses due to circulating energy.

2) The characteristic impedance of the power stage Z_O should be maximized; i.e., select the full-load low-line operating condition to fall in the maximum I_{ON} curve that does not result in unstable operation.

3) The converter should be designed for $M \simeq 0.5$ in order to minimize conduction losses in the primary circuit.

Once C_N, f_{con}/f_O, M_{max}, and I_{ON}^{max} have been selected, the turns ratio of the transformer and resonant component values are calculated from:

$$N = \frac{V_{IN}^{min} 2M_{max}}{V_O} \tag{3.8}$$

$$C_D = \frac{1}{2} N^2 C_N C \tag{3.9}$$

and

$$L = \frac{C_S}{2} \left[\frac{N I_{ON}^{max} V_{IN}^{min}}{I_O^{max}} \right]^2 \qquad (3.10)$$

Switches Q_1 and Q_2 with small on-resistance are necessary to keep the conduction losses low, whereas smaller output capacitances of the switches are desirable to reduce the primary peak (and rms) currents. Thus, the value of C_S is the value of the output capacitance of either Q_1 or Q_2.

The peak current through the primary switches can be estimated using the following expression:

$$I_{PRIM}^{pk} < \frac{V_{IN}^{max}}{4 L f_s} \qquad (3.11)$$

The peak current through the CF switches is:

$$I_{CF}^{pk} < N I_{PRIM}^{pk} \qquad (3.12)$$

and the maximum voltage stress on the CF switches is:

$$V_{CF}^{max} = \frac{V_{IN}^{max}}{N} \qquad (3.13)$$

3.5 Experimental Results

Using the design guidelines suggested in the previous section, a 50 W CF forward ZVS-MRC and two 100 W CF HB ZVS-MRCs were built.

3.5.1 Experimental Results for CF Forward ZVS-MRC

3.5.1.1 Power Stage

A 50 W, CF forward ZVS-MRC with a 5 V output was designed for an input voltage range from 45 V to 55 V. The converter operates from full load (10 A) to no load (0 A) at a switching frequency of 1.9 MHz. The components of the power stage are the following:

Q_1 - IRF740 (International Rectifier);

Q_2 - IRFZ44 (International Rectifier);

TR   - core: custom made E core (material Q_1);

     primary: 6 turns of 150/44 Litz wire;

     secondary: 2 turns 5 mils copper foil;

     primary leakage inductance: 390 nH;

L - inductance: 2 μH;

     core: Micrometals iron powder core T44-6;

     winding: 22 turns of 150/44 Litz wire;

D_1 - Semetex SXS300W45M;

C_S - 270 pF + 2 x 480 pF mica;

C_D - 7 x 6.8 nF, NPO chip ceramic;

L_F - inductance: 1 μH;

     core: TDK RM5Z52B (material H_{7C4});

     winding: 4 turns magnet wire AWG# 16;

     gap: 5 mm; and
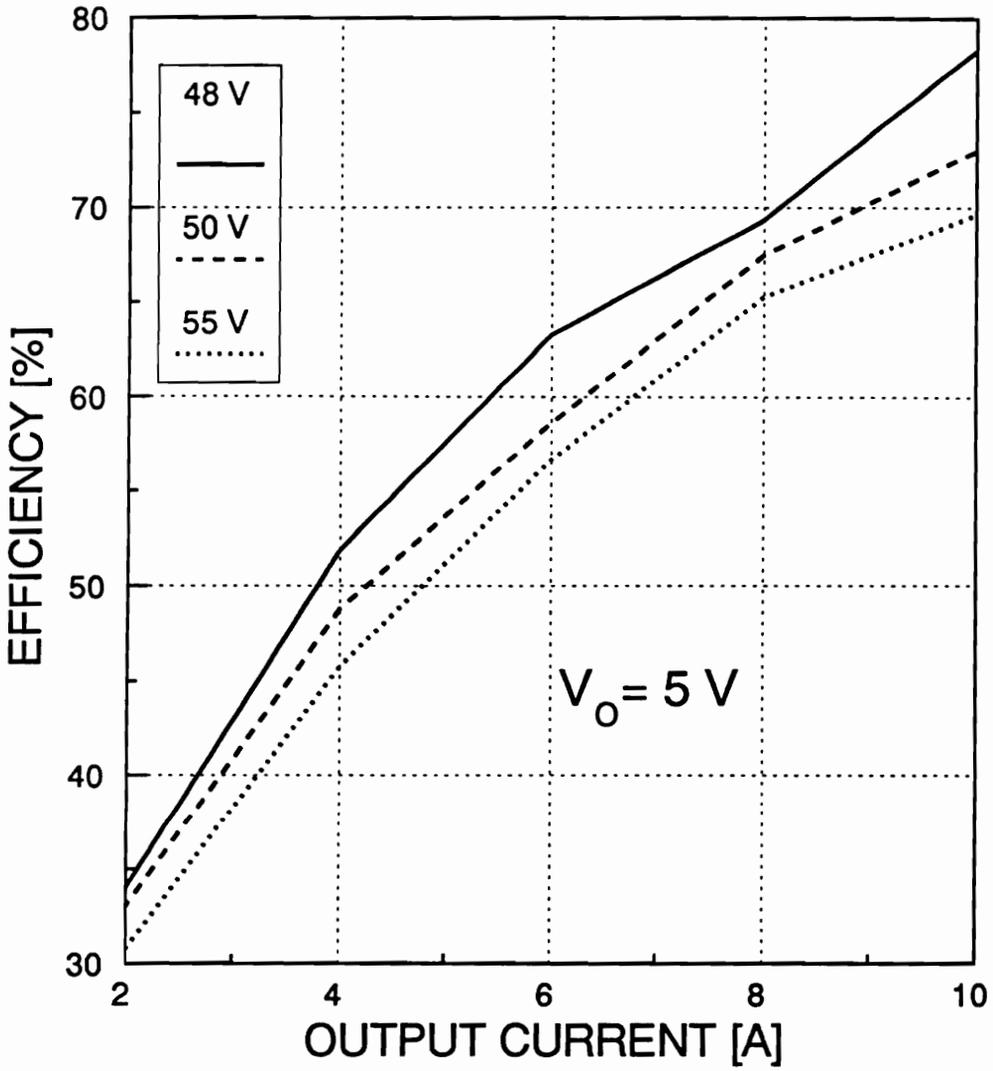
Figure 3.30.   Measured efficiency of the CF forward ZVS-MRC as a function of the load current for different line conditions.
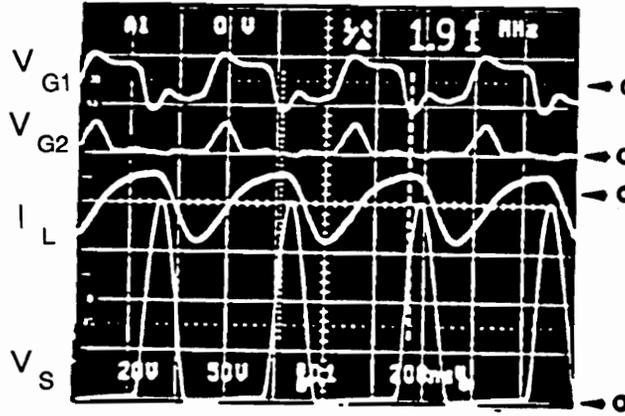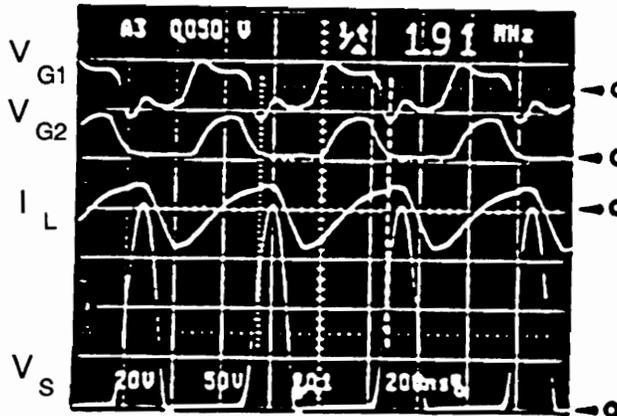
Figure 3.31. Waveforms of the CF forward ZVS-MRC for different load conditions:
(a) full load (10 A) and low line (45 V);
(b) no load (0 A) and low line (45 V).
showing from top to bottom; primary switch gate drive (V_{G1}), CF switch gate drive (V_{G2}), resonant inductor current (I_L), and primary switch drain-source voltage (V_S).
Scales: 20 V/div.; 20 V/div.; 3 A/div.; 50 V/div.; 200 ns/div..
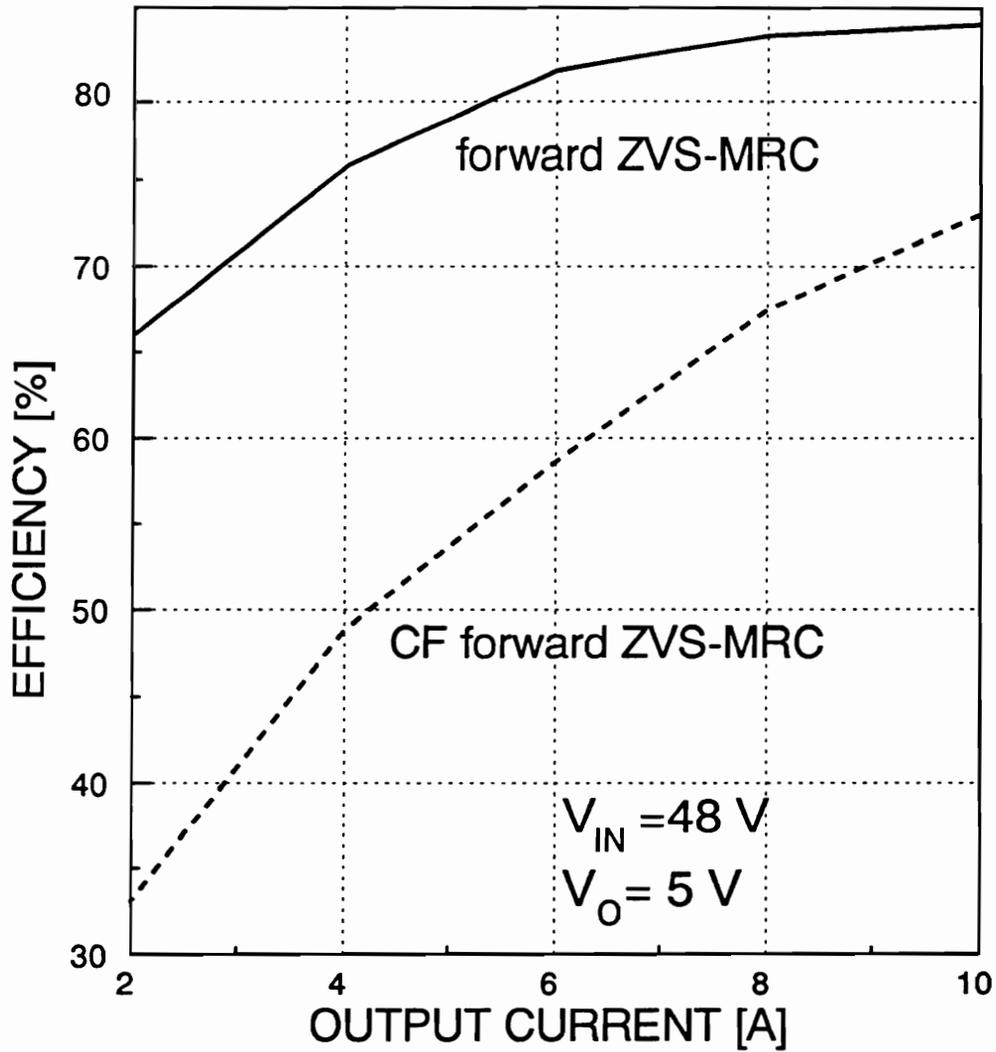
Figure 3.32. Measured efficiency of the forward ZVS-MRC and CF forward ZVS-MRC for different load currents and an input voltage of 48 V.

C_F - 4 x 3 μF NPO chip ceramic.

Figure 3.30 shows the measured efficiency of the power stage as a function of the load current for different input voltages. A maximum efficiency of 78.3% was obtained for the power stage at full load and low line. The maximum efficiency occurs for the minimum conduction period of the CF switch. Figure 3.31 shows the oscillograms of key waveforms at low line for full load and no load operation. Figure 3.32 compares the efficiency of a variable frequency forward ZVS-MRC built for the same specifications and using the same components and that of the CF forward ZVS-MRC for different load currents and an input voltage of 48 V. Figure 3.32 shows that the increased circulating energy resulting from constant frequency operation of ZVS-MRC heavily penalizes the performance of CF ZVS-MRCs.

3.5.1.2 Control/Timing Requirements for the CF Switch

The gate-source signal for the primary switch Q_1 of the CF forward ZVS-MRC oscillates at a constant switching frequency and a constant duty cycle. The off-time of this switch is determined from the resonance of the primary switch voltage. No feedback control is needed for the primary switch Q_1. The turn-on time of the constant frequency switch Q_2 cannot be synchronized with the turn-on time of the primary switch, if soft switching of Q_2 is desired, because in Mode I of operation the voltage across capacitor voltage V_D is positive (forward diode D_1 is conducting) at the time the primary switch turns on. Soft switching of Q_2 can be maintained for all operating conditions by introducing a delay between the turn-on time of this switch relative to the turn-on time of Q_1. Once the capacitor voltage V_D becomes negative, the antiparallel diode of switch Q_2 will conduct and soft switching of this switch can be achieved.
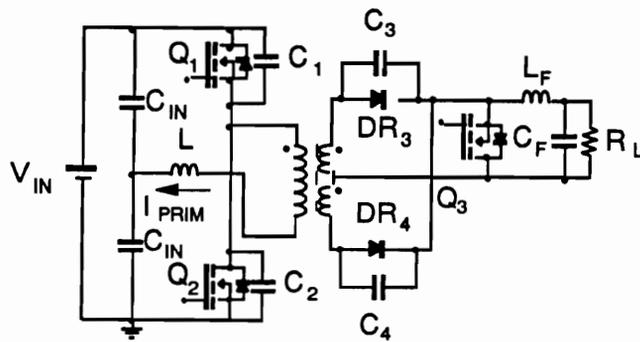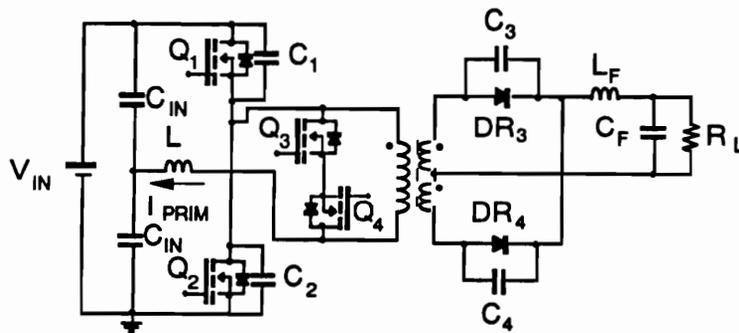
Figure 3.33. Experimental CF HB ZVS-MRCs
(a) One constant frequency switch across the input terminals of the output filter;
(b) constant frequency switch across the primary transformer winding.

In general, the delay between the two switches is very short and can be easily adjusted once the hardware is completed. A similar control scheme as the one shown for the CF buck ZVS-MRC (Fig. 2.13) can be used for the CF forward ZVS-MRC. Positive feedback control is needed to control the conduction time of the constant frequency switch since an increase in the conduction time of this switch results in a decrease of the output voltage.

3.5.2 Experimental Results for CF HB ZVS-MRC

3.5.2.1 Power Stage

The CF HB ZVS-MRCs shown in Fig. 3.33(a) and Fig. 3.33(b) were designed for an input voltage range from 270 V to 330 V. The converters operate with a switching frequency of 700 kHz and are capable of regulating the 5 V output from no load to full load (20 A). The experimental power stage components of the circuit implementation shown in Fig. 3.33(a) are:

Q_1, Q_2 - IRF740 (International Rectifiers);

Q_3 - IRFZ44 (International Rectifiers);

C_1, C_2 - output capacitance of IRF740;

TR   - core: TDK LP 32/13 (material H_{7C4});

            primary: 16 turns of 150/44 Litz wire;

            secondary: 1 turn of 5 strand of 150/44 Litz wire;

            primary leakage inductance: 16 μH;

L - leakage inductance of power transformer;
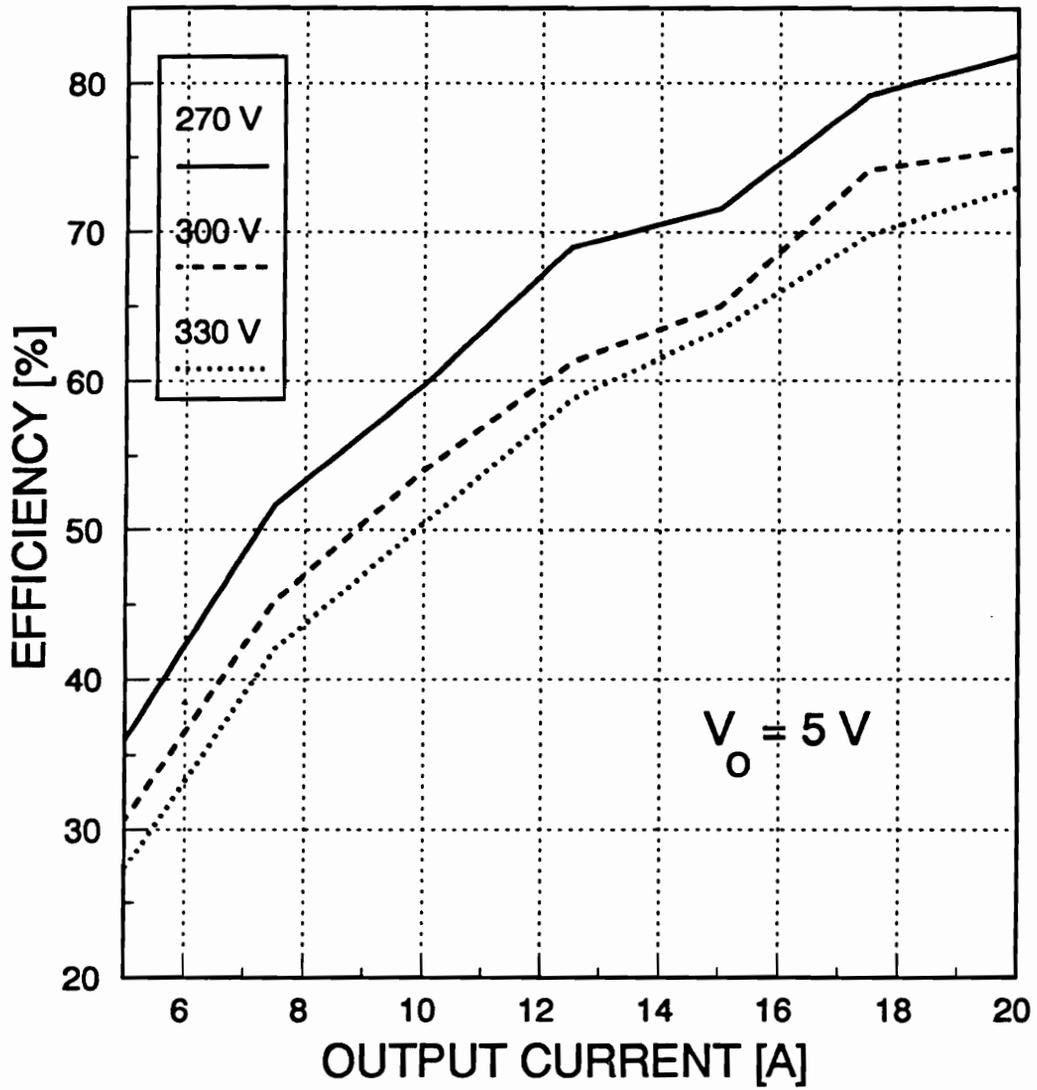
Figure 3.34. Measured efficiency of the CF HB ZVS-MRC shown in Fig. 3.33(a) as a function of the load current for different line conditions.
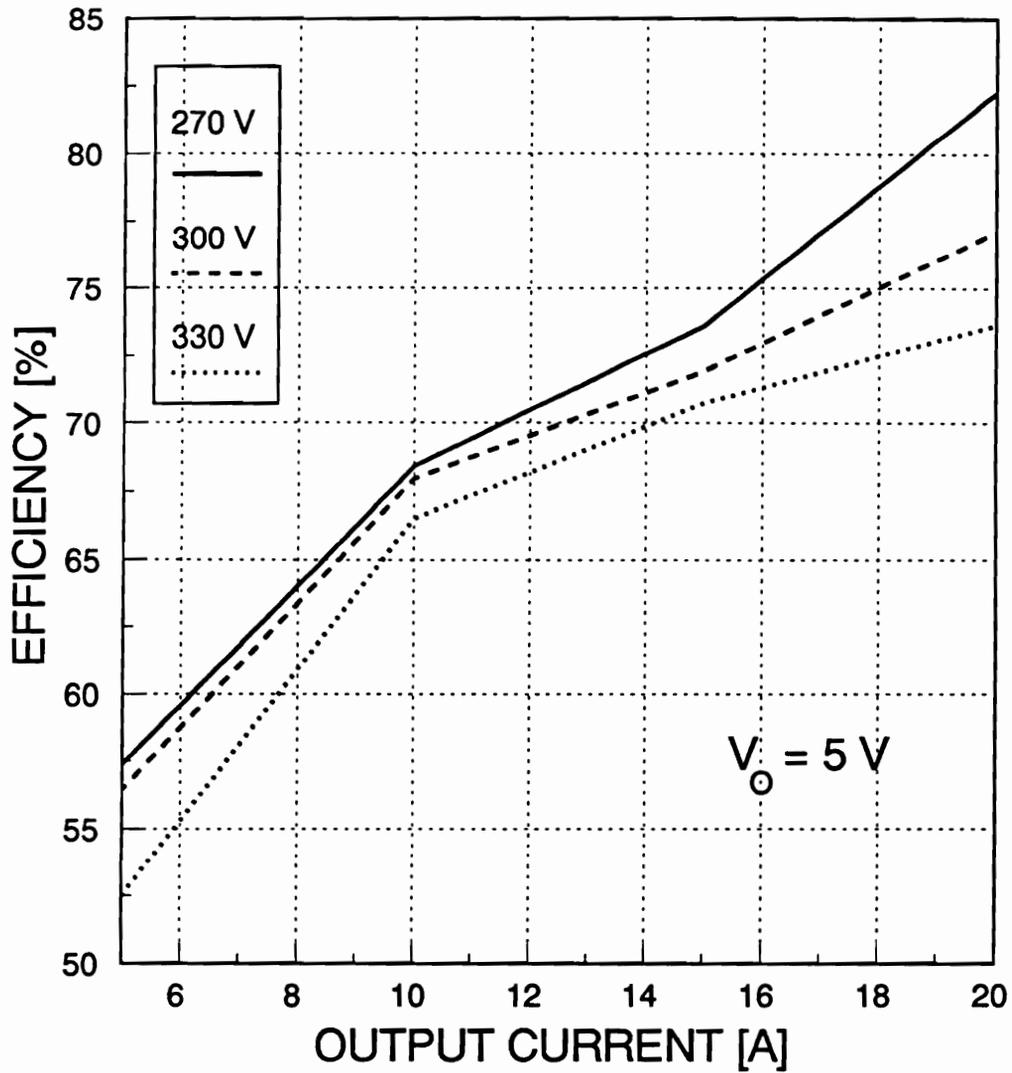
Figure 3.35. Measured efficiency of the CF HB ZVS-MRC shown in Fig. 3.33(b) as a function of the load current for different line conditions.
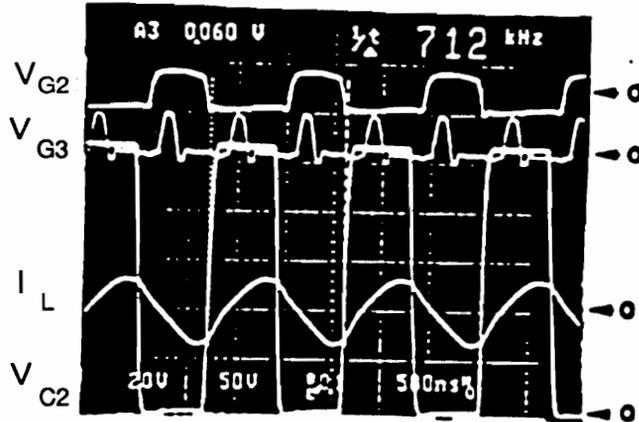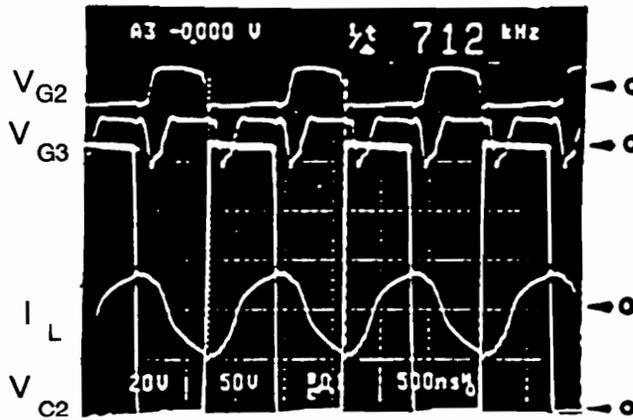
Figure 3.36. Waveforms of the CF HB ZVS-MRC, with the CF switch in the secondary side for different load conditions:
(a) full load (20 A) and low line (270 V);
(b) no load (0 A) and low line (270 V).
showing from top to bottom; Q_2 gate drive (V_{G2}), Q_3 gate drive (V_{G3}), resonant inductor current (I_L), and drain-source voltage of Q_2 (V_{C2}).
Scales: 20 V/div.; 20 V/div.; 3 A/div.; 50 V/div.; 500 ns/div..

D_{R3}, D_{R4} - 60CNQ045 (International Rectifier);

C_3, C_4 - 4 x 6.8 nF NPO chip ceramic;

L_F - inductance: 1 μH;

  core: TDK RM6Z12 (material H_{7C4});

  winding: 4 turns magnet wire AGW# 16;

  gap: 5 mm.; and

C_F - 5 x 3.3 μF NPO ceramic chip.

For the experimental power stage shown in Fig. 3.33(b), the following components are used:

$Q_1 - Q_4$ - IRF740 (International Rectifier);

C_1, C_2 - output capacitance of IRF740;

TR - core: TDK LP 22/13 (material H_{7C4});

  primary: 10 turns of 150/44 Litz wire;

  secondary: 1 turn of 5 strand of 150/44 Litz wire;

  primary leakage inductance: 400 nH;

L - inductance: 16 μH;

  core: TDK LP 22/13 (material H_{7C4}:

  winding: 20 turns of 150/44 Litz wire;

  gap: 7mm;

D_{R3}, D_{R4} - 60CNQ045 (International Rectifier);

C_3, C_4 - 4 x 6.8 nF NPO chip ceramic;

L_F - inductance: 1 μH;

  core: TDK RM6Z12 (material H_{7C4});

  winding: 4 turns magnet wire AGW# 16;

gap: 5 mm.; and

C_F - 5 x 3.3 μF NPO ceramic chip.

Figure 3.34 shows the measured efficiency of the experimental power stage of Fig. 3.33(a) as a function of the output current, whereas Fig. 3.35 shows the measured efficiency of the experimental power stage of Fig. 3.33(b) as a function of the output current. The maximum efficiency for both designs occurs at low line and full load. Placing the CF switch in the primary side reduces the conduction losses associated with the CF switch, and results in higher efficiencies over the whole load and input voltage range. A significant decrease in efficiency at light loads results from increased conduction losses and the loss of zero-voltage turn-on of the CF switch. Figure 3.36 shows oscillograms for the CF HB ZVS-MRC shown in Fig. 3.33(a) operating at low line and full load, and low line and no load.

3.5.2.1 Control/Timing Requirements for the CF Switches

The gate drive signal for the CF switches for the CF HB with two active switches in the rectifier circuit (Fig. 3.10(b)) can be synchronized with the gate drive signal of the primary switches. That is, the turn-on time of the constant frequency switches coincides with that of the corresponding primary switch. This is possible because in the HB topology the switching frequency is half of the filter frequency and all switches will only conduct for half a cycle. For example, when the primary current (resonant inductor current) is positive at the start of a switching cycle (time T_O in Fig. 3.12), the antiparallel diode of switch Q_3 conducts and the load is being supplied from the primary. At time T_2 (Fig. 3.12), the load current freewheels through the shorted secondary transformer windings, i.e., the antiparallel diode of switches Q_3 and Q_4
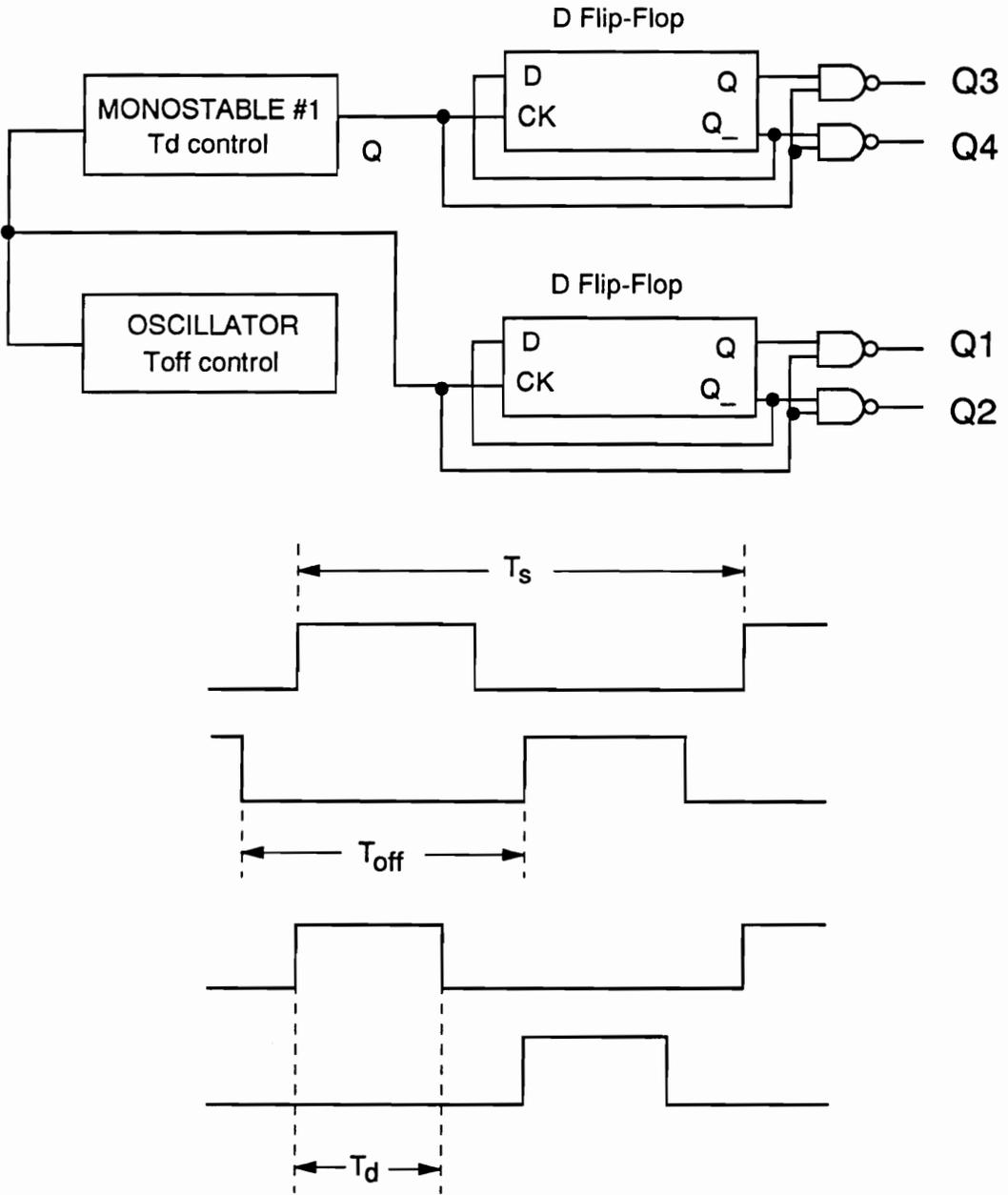
Figure 3.37. Block diagram of the control scheme for the CF HB ZVS-MRC of Fig. 33.3(b).
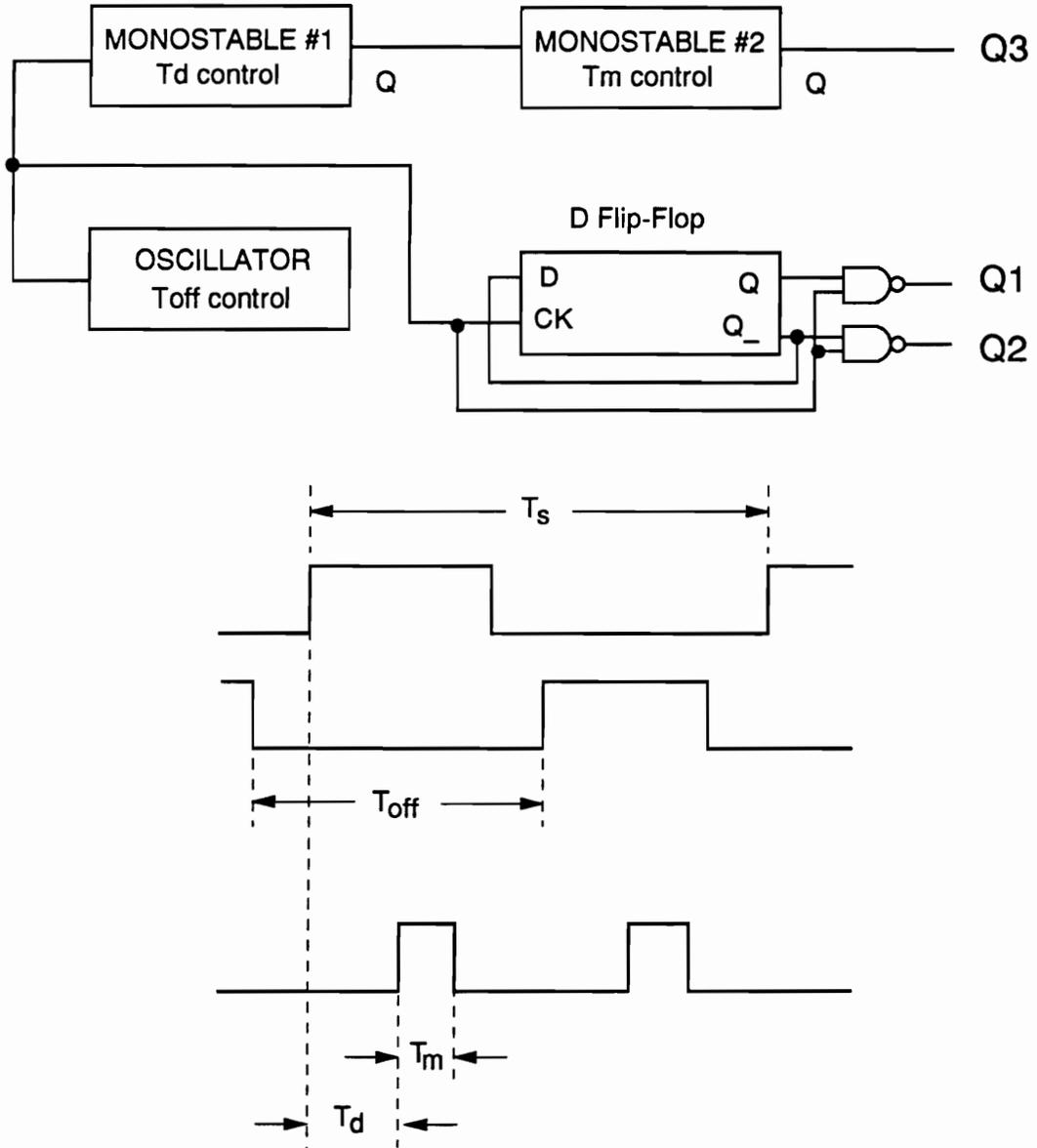
Figure 3.38. Block diagram of the control scheme for the CF HB ZVS-MRC of Fig. 33.3(a).

conduct. At time T_3 (Fig. 3.12) the primary current has decreased to $- I_O/N$ and CF switch Q_3 will start conducting. From this discussion, it can be seen that switch Q_3 can be turned on at T_O without changing the operation of the converter because it's antiparallel diode will conduct during the time interval $T_3 - T_O$. Switch Q_3 turns-on under zero voltage (ZVS). Thus, the turn-on time of switch Q_3 is synchronized with the turn-on time of switch Q_1 and the turn-on time of switch Q_4 is synchronized with the turn-on time of switch Q_2.

As for all CF ZVS-MRCs, the primary switches require no feedback control. Positive feedback control is needed for the consonant frequency switches. This means that as the conduction time of switch Q_3 and Q_4 increases, the output voltage will decrease as the line and load remain constant.

The same control scheme can be used for the constant frequency implementation of the HB topology using a bidirectional switch in parallel with the primary windings of the power transformer (Fig. 3.33(b)). A true bidirectional switch can be implemented using two MOSFETS as shown in Fig. 3.33(b). Each MOSFET used in the bidirectional switch switches at the same speed as the principal switches (switches Q_1 and Q_2). Thus, the turn-on time of switch Q_3 is synchronized with the the turn-on time of switch Q_1, and Q_4 is synchronized with Q_1. The practical implementation of this control scheme is shown in Fig.3.37.

The control scheme of the constant frequency switch for the implementation of the CF HB converter using one active switch in the secondary circuit (Fig. 3.33(a)) is not as simple as the one described above. The turn-on time of switch Q_3 has to be adjusted so that it occurs during the freewheeling stage. During the freewheeling stage, the voltage across the input terminals of the output filter is zero and Q_3 can be turned on under zero voltage. The duration and the time of the freewheeling stage, relative to the switching transition of the primary switches

(beginning of the switching cycle), varies as a function of load and line conditions. Therefore, if the turn-on time of the constant frequency switch Q_3 is adjusted for soft switching under heavy load conditions, it is very likely that zero voltage turn-on will be lost at light load conditions. Switch Q_3 switches at twice the switching frequency and its turn-on time does not coincide with the turn-on of either of the primary switches. Therefore, a delay has to be introduced between the turn-on time of switch Q_3 and the turn-on of switches Q_1 and Q_2. The control for the implementation of the CF HB ZVS-MRC using one CF switch at the input of the output fileter is shown in Fig.3.38.

3.6 Summary

A complete dc analysis and design of the CF forward and HB MR converters is presented. Design trade-offs are presented for both of these topologies. Design guidelines for the CF forward and HB ZVS-MRCs based on the design trade-off studies are listed. The design of the forward topology is different from the other converters in this new family of converters because the magnetizing current plays an important role in the operation of the converter. The design of the HB topology also differs from the other converters in this family of ZVS-MRCs, since the primary switches are clamped to the input voltage, interrupting the resonance of the primary switch capacitance and the resonant inductor. An alternative design method based on the analysis of reactive energy flowing through the converter will be discussed in Chapter 6. This alternative method minimizes the transformer size while maximizing the efficiency of the converter. Performance of an experimental 50 W forward converter and two 100 W, off-

line, HB converters are also shown. A significant improvement of the performance of the CF ZVS-MRC is expected from the development of MOSFETs with very low on-resistance (synchronous rectifiers).

4. NEW FAMILY OF ZVS ISOLATED CONVERTERS

USING THE MAGNETIZING INDUCTANCE

4.1 Introduction

Circuit parasitics, such as transformer leakage inductance, semiconductor junction capacitances, and rectifier reverse recovery are among the major factors hindering operation of "hard switched" PWM converters at high switching frequencies. Recent developments in high-frequency power conversion have shown an increased utilization of parasitic components. Several innovative techniques have been proposed to operate the active switch with zero-voltage turn-on in order to minimize switching losses, stresses, and noises. Generally, these techniques can be classified in two groups: resonant techniques and pulse-width-modulated (PWM) techniques with zero-voltage switching (ZVS) [B1-B36] and [C1-C20]. The ZVS concept has also been extended to include both active and passive switches [D1-D15].

In order to obtain ZVS of all semiconductor components, the resulting multi-resonant converters (MRCs) [D1] and class-E converters with resonant rectifiers [C2] utilize the transformer leakage inductance and transistor and rectifier junction capacitances to form a multi-component resonant network. The constant frequency implementation of the ZVS-MR family of converters was discussed in the first three chapters.

A major disadvantage of the resonant type converters is they require a relatively large resonant inductor to achieve ZVS over a wide load range, in particular the zero-voltage-switched (ZVS) quasi-resonant (QR) and multi-resonant (MR) family of converters, for both variable and constant frequency operation. The resonant inductor is subjected to high resonant currents and voltages, which have a detrimental effect on the overall efficiency and size of ZVS-QRCs, ZVS-MRCs, and CF ZVS-MRCs.

In isolated ZVS-QRC and ZVS-MRC topologies, the resonant inductor is connected in series with the primary winding of the power transformer as shown in Fig. 4.1 for the half-bridge (HB) ZVS-QRC [B22]. However, the magnetizing inductance cannot be used as a resonant element because the primary of the transformer is shorted during the resonant stage, due to the simultaneous conduction of output rectifiers DR_1 and DR_2 as shown in Fig. 4.2(b) [B22]. Figure 4.2 shows the topological stage sequence found in one half-cycle of normal operation of the HB ZCS-QRC. To use the magnetizing inductance as the resonant inductor, it is necessary to open the secondary side of the transformer during the resonant interval instead of shorting it. With the secondary of the transformer open, the magnetizing inductance appears in series with the capacitances of the primary switches, thus forming a resonant circuit.

In this chapter, a method of generating a new family of isolated ZVS converters which utilize the magnetizing inductance as a resonant element and eliminates the need for an external
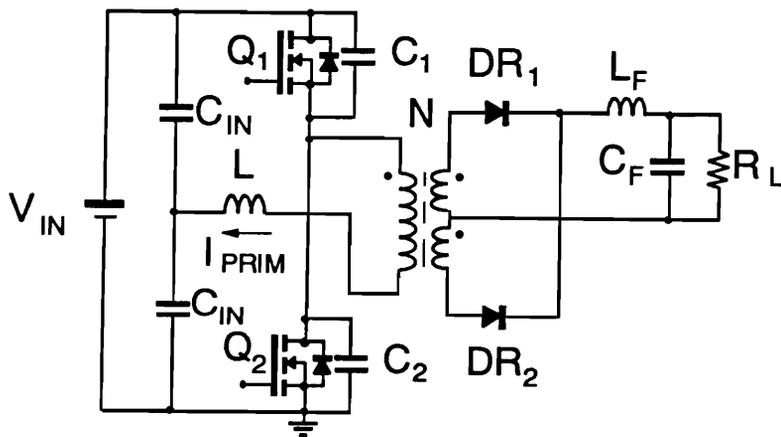
Figure 4.1. The HB ZVS-QRC.
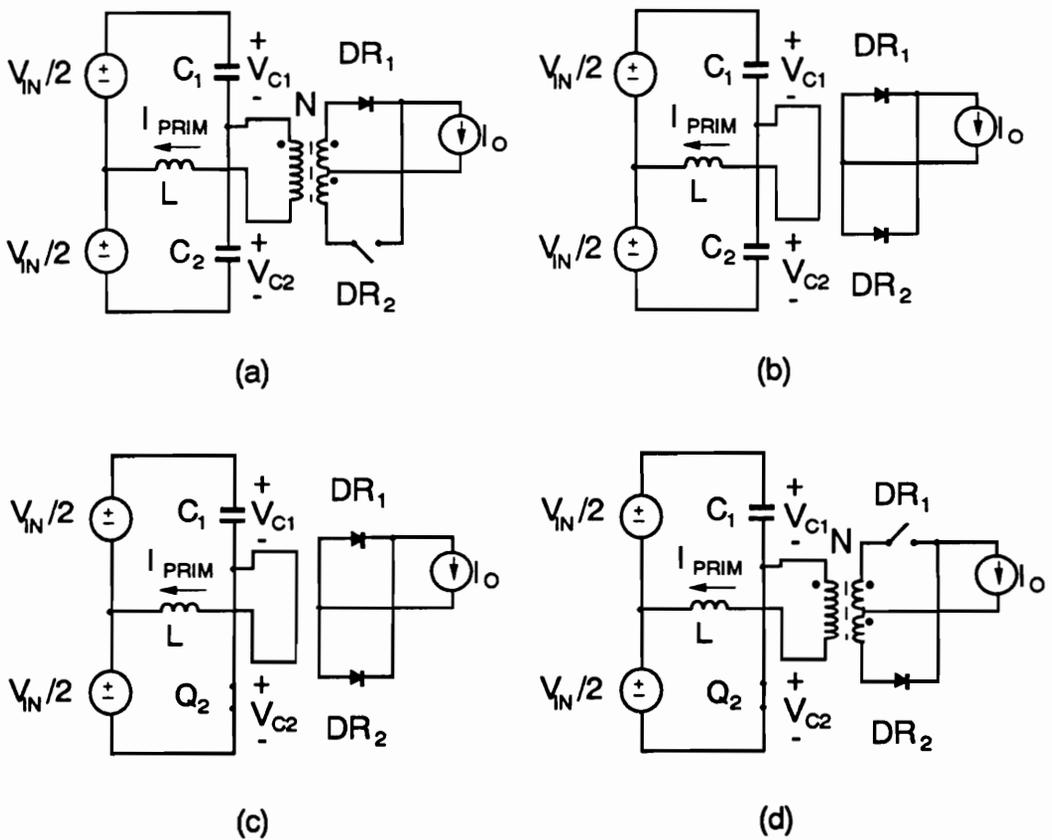
Figure 4.2. Topological stages of HB ZVS-QRC: (a) capacitor charging; (b) resonant; (c) inductor discharging; and (d) constant current stage.

resonant inductor is described. This new concept is first shown for the HB topology. The bridge-type topologies result in PWM-type current and waveforms which result in reduced conduction losses relative to resonant converters. Operation of the forward and flyback topologies is also discussed to provide some insight as to how the operation of single-ended topologies differ from HB and push-pull converters. Finally, the concept is further extended to obtain soft turn-off of the output rectifiers.

4.2 Concept and Development

Generally, soft turn-on in ZVS converters is achieved by turning on the switch while its anti-parallel diode is conducting. The antiparallel diode is forced into conduction by resonating the output capacitance of the switch with an inductor connected in series with the transformer [1]. For example, in the HB converter of Fig. 4.1, resonance between L, C_1, and C_2 is used to obtain ZVS of Q_1 and Q_2. The operation and detailed analysis of the circuit is given in [B22]. In this chapter, only a brief description of ZVS mechanism is presented. In other resonant, QRC, and MRC topologies, the ZVS principle is similar to that of the described HB converter.

4.2.1 Zero-Voltage-Switching Principle in HB ZVS-QRC
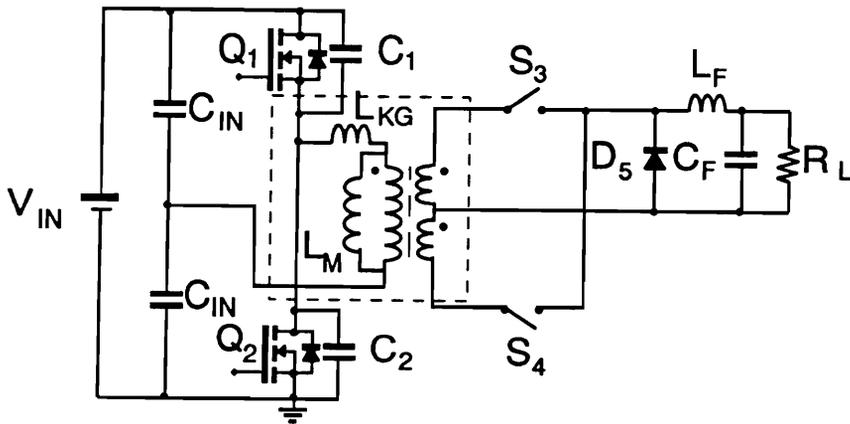
Figure 4.3. The HB ZVS-QRC (L_M) converter Rectifier diodes are replaced by active switches to open the secondary transformer windings during the switching transition and enable the magnetizing inductance to charge and discharge the primary switch capacitances in a resonant manner.
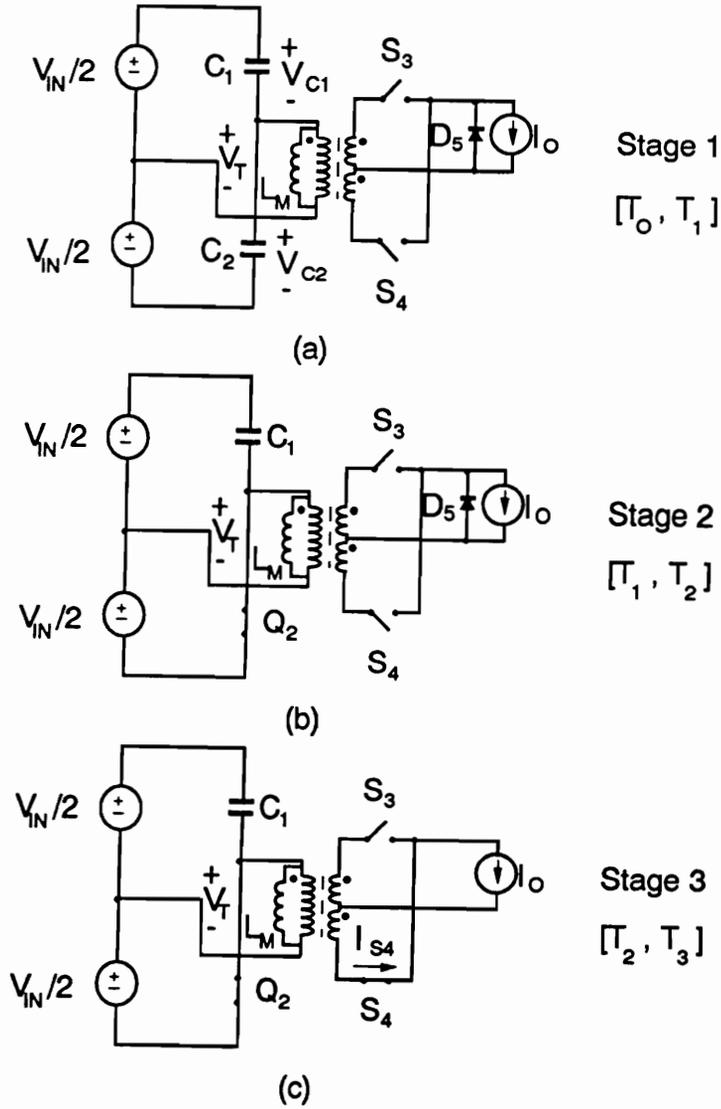
Figure 4.4. Topological stages of the HB ZVS-QRC (L_M): (a) Stage 1; (b) Stage 2; and (c) Stage 3.
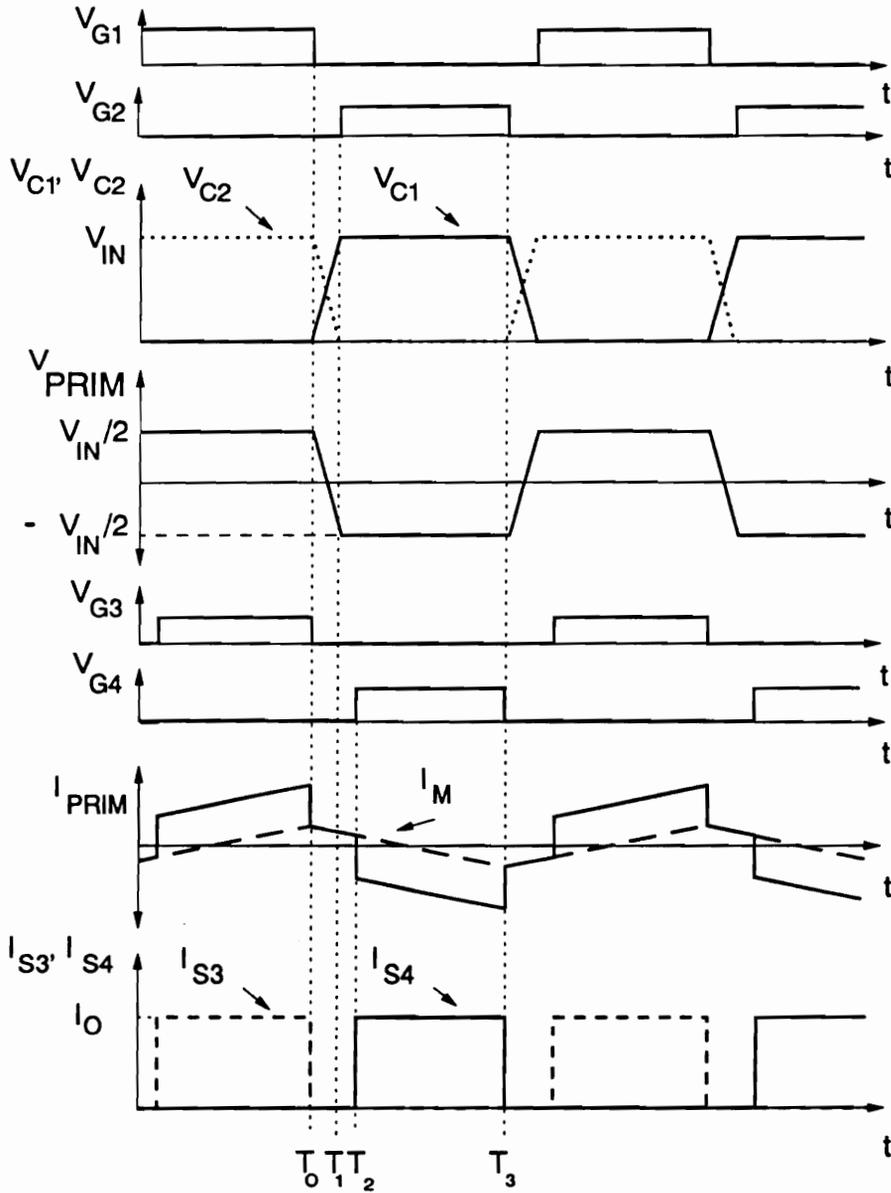
Figure 4.5. Ideal waveforms of the HB ZVS-QRC (L_M), from top to bottom: gate-source voltage of switch Q_1, V_{G1}, gate-source voltage of switch Q_2, V_{G2}, drain-source voltage of switches Q_1 and Q_2, V_{C1} and V_{C2}, primary transformer voltage V_{PRIM}, gate-source voltage of switch S_3, V_{G3}, gate-source voltage of switch S_4, V_{G4}, primary current I_{PRIM}, and secondary switch currents I_{S3} and I_{S4}. I_M represents the magnetizing transformer current.

Prior to the turn off of switch Q_1 in the HB converter of Fig. 4.1, constant output current I_O is flowing through the upper secondary. At the same time, primary current I_O/N flows through switch Q_1, the primary winding, and inductor L. Due to the conduction of Q_1, the voltage across C_1 is zero, and the full supply voltage V_{IN} appears across C_2. When Q_1 is turned-off, primary current I_O/N is diverted from Q_1 to C_1 and C_2. The equivalent circuit of the converter immediately after the switch is turned off is shown in Fig. 4.2(a). Since the primary current during this stage remains constant (I_O/N), there is no voltage drop across inductor L, and voltages across C_1 and C_2 change linearly. Voltage V_{C1} increases from zero to V_{IN}, while voltage V_{C2} decreases from V_{IN} to zero at the same rate. When voltages across C_1 and C_2 reach $V_{IN}/2$, i.e., $V_{C1} = V_{C2} = V_{IN}/2$, the primary voltage across the transformer becomes zero. Further change of voltages V_{C1} and V_{C2} tend to make the primary voltage of the transformer negative, which forces rectifier DR_2 to turn on. When DR_2 starts conducting, the secondary windings of the transformer are shorted since DR_1 still conducts. As a result, the primary voltage across the transformer is zero as shown in Fig. 4.2(b). Inductance L and capacitances C_1 and C_2 (effectively connected in parallel) form a resonant circuit and the voltages across C_1 and C_2 continue to change (C_1 to charge and C_2 to discharge) in a resonant fashion. When voltage V_{C2} reaches zero, antiparallel diode D_2 starts conducting, clamping the voltage across Q_2 to zero. If Q_2 is turned on while D_2 is conducting, ZVS of Q_2 is achieved.

As can be seen, during the resonant stage, which creates the conditions for ZVS, the transformer is shorted by simultaneous conduction of the output rectifiers. As a result, the magnetizing inductance of the transformer, which is in series with L, is taken out of the circuit. To use the magnetizing inductance as a resonant element and eliminate the need for an external resonant inductor, it is necessary to modify the circuit in Fig. 4.1 so that the magnetizing inductance is not shorted during the resonant stage.

4.2.2 Zero-Voltage-Switching using the Magnetizing Inductance

Figure 4.3 shows the conceptual implementation of a HB ZVS which utilizes the magnetizing inductance as a resonant element (HB ZVS-QRC (L_M)). In order to prevent the voltage across the magnetizing inductance of the power transformer from being shorted during the switching transition, the rectifiers are replaced by switches S_3 and S_4. In addition, to ensure a current path when both secondary switches are turned-off, a freewheeling diode D_5 is connected across the input of the output filter. The added switches, S_3 and S_4, delay the energy transfer from the primary circuit to the secondary circuit until the magnetizing inductance discharges the output capacitance of the switch to be turned on and forces its antiparallel diode into conduction. During a switching cycle this converter enters a sequence of three topological stages. Figure 4.4 shows the topological stages and Fig. 4.5 the ideal waveforms of the converter. The waveforms are obtained assuming that the forward voltage drop of all semiconductor devices, the leakage inductance of the power transformer, and the parasitic capacitance of the rectifier diodes are negligible. Also, the output filter and the load are replaced by an ideal current source by assuming that the inductance of the output filter is large enough so that the filter inductor current is constant during a switching period.

Prior to the turn off of transistor Q_1 in the circuit of Fig. 4.3, secondary-side switch S_3 is on, and switch S_4 is off. As result, the entire constant load current flows through the upper secondary, as in the case of the converter in Fig. 4.1. At $t = T_0$, switches Q_1 and S_3 are turned off, and the magnetizing current is diverted from Q_1 into C_1 and C_2. At the same time, the load current is commutated to the freewheeling diode. Figure 4.4(a) shows the equivalent circuit of the converter immediately after Q_1 and S_3 are turned off. This topological stage is referred to as Stage 1. With the output current freewheeling, the primary current consists only of the

magnetizing current. This magnetizing current charges C_1 and discharges C_2 at the same rate. It should be noted that charging of C_1 and discharging of C_2 occurs in a resonant fashion, since L_M, C_1, and C_2 form a resonant circuit. However, L_M is normally very large, and a relatively constant magnetizing current during the duration of Stage 1 produces linear voltage changes across C_1 and C_2. Stage 1 ends at $t = T_1$, when the voltage across switch Q_2 decreases to zero, and the antiparallel diode of Q_2 starts conducting. To achieve ZVS, the gate drive to switch Q_2 should be applied while its antiparallel diode is conducting. During Stage 2, shown in Fig. 4.4(b), switch S_3 and S_4 remain off, and no power is transferred to the load. The primary current is the magnetizing current of the power transformer and the load current continues to freewheel through diode D_5. This stage ends at $t = T_2$, when switch S_4 is turned on, and the converter enters Stage 3. During Stage 3, Fig. 4.4(c), the load current is commutated from the freewheeling diode to the lower secondary. As a result, during this stage power is transferred to the load. The primary current is the sum of the magnetizing current of the transformer and the load current reflected to the primary. This stage ends at $t = T_3$ when switches Q_2 and S_4 are turned off, marking the beginning of a new conversion cycle.

Since power is delivered to the load only during Stage 3, the output voltage can be regulated at a constant switching frequency by varying the duration of this stage; controlling the time of Stage 2. Note that the duration of Stage 1 can not be controlled, since approximately constant blocking time $T_1 - T_O$ is needed to create conditions for ZVS of the primary switches. This time interval is dependent upon the magnetizing current, magnetizing inductance, and the junction capacitance of switches Q_1 and Q_2. The maximum output voltage is obtained when the duration of Stage 2 is zero, i.e., when $T_2 = T_1$. If the duration of Stage 2 is fixed, i.e., $T_2 - T_1 = $ constant, the output voltage can be regulated by varying the switching frequency.

To simplify the variable-frequency control, the duration of Stage 2 can be made zero $(T_2 = T_1)$ in practice.

With variable-frequency control, Q_1 and Q_2 operate with variable on-time control, while switches S_3 and S_4 are delayed by a constant time interval $(T_1 - T_0)$. Figure 4.6 shows the dc voltage-conversion-ratio characteristics as a function of the normalized conversion frequency $(f_s/2f_O)$ where $\omega_O = 2\pi f_O = 1/\sqrt{2CL_M}$, $C = C_1 = C_2$ is the resonant capacitance across the primary switches, and L_M is the magnetizing inductance of the transformer. Under constant frequency control, switch Q_1 and Q_2 operate with constant frequency and constant duty cycle, while switches S_3 and S_4 are leading-edge PWM. The dc voltage-conversion-ratio characteristics for constant-frequency control can be approximated by $M = D \simeq (T_2 - T_1)/(T_3 - T_1)$, assuming the duration of Stage 1, $T_1 - T_0$, is small. The dc voltage-conversion-ratio for both variable frequency and constant frequency operation are load independent.

This concept can be extended to other isolated topologies as shown in Fig. 4.7. For single ended topologies, the resonance of the output capacitance of the primary switch and the magnetizing inductance of the power transformer take place for half of a resonant cycle. Figure 4.8 shows the ideal waveforms for the forward topology of Fig. 4.7(a). The stage sequence for normal operation of the forward converter is shown in Fig. 4.9. In this topology, when power transfer is interrupted by a forced turn-off of switch Q_1, the output capacitance of the switch starts resonating with the magnetizing inductance of the transformer, Stage 1 $[T_0, T_1]$. As a result, the voltage V_{C1} in Fig. 4.8 first increases, goes through a maximum, and finally reaches zero at $t = T_1$. At $t = T_1$, the antiparallel diode of Q_1 starts conducting the primary current and V_{C1} remains at zero. ZVS is achieved by turning on Q_1 when the antiparallel diode is conducting. The additional active switch S_2 replacing the forward diode is necessary

to insure that the turn-on of the forward diode D_1 (Fig. 2.9(a)) will not prevent the zero voltage turn-on of switch S_1.

In Stage 2 [T_1, T_2], the voltage across the magnetizing inductance is equal to the input voltage resulting in a magnetizing current that increases at a constant rate. The load current continues to freewheel. Stage 3 [T_2, T_3] begins when switch S_2 is turned on, thus turning off the freewheeling diode; power is transferred to the load from the source. This last stage ends when switch S_1 is turned off at time T_3 initiating a new switching cycle.

It should be noted that the flyback and sepic topologies do not need an extra active switch to resonate the magnetizing inductance of the power transformer during the resonant interval, since the magnetizing inductance is free to resonate during the off-interval of the power switch. In addition, the resonance of the resonant capacitor voltage across the power switch is clamped by the output voltage. The ideal waveforms for the flyback topology are shown in Fig. 4.10. The topological stage sequence for this converter is shown in Fig. 4.11.

The operation of the flyback converter is the following: in Stage 1 [T_O, T_1], switch S_1 conducts and the magnetizing current increases at a constant rate. At time T_1, switch S_1 is turned off, Stage 2, and the magnetizing current charges capacitance C_1 in parallel with S_1. Capacitance C_1 will continue to charge until the voltage across this capacitance is equal to $V_O/N + V_{IN}$, where N is the turns ratio of the transformer. At the same time, the magnetizing inductance gets clamped to $- V_O/N$. In Stage 3 [T_2, T_3], the magnetizing current decreases at a constant rate since the magnetizing inductance remains clamped to $- V_O/N$. This stage ends when the magnetizing current decreases to zero and diode D_2 turns off. In Stage 4 [T_3, T_4], the magnetizing inductance resonates with capacitance C_1. If V_O/N is greater than the input volt-
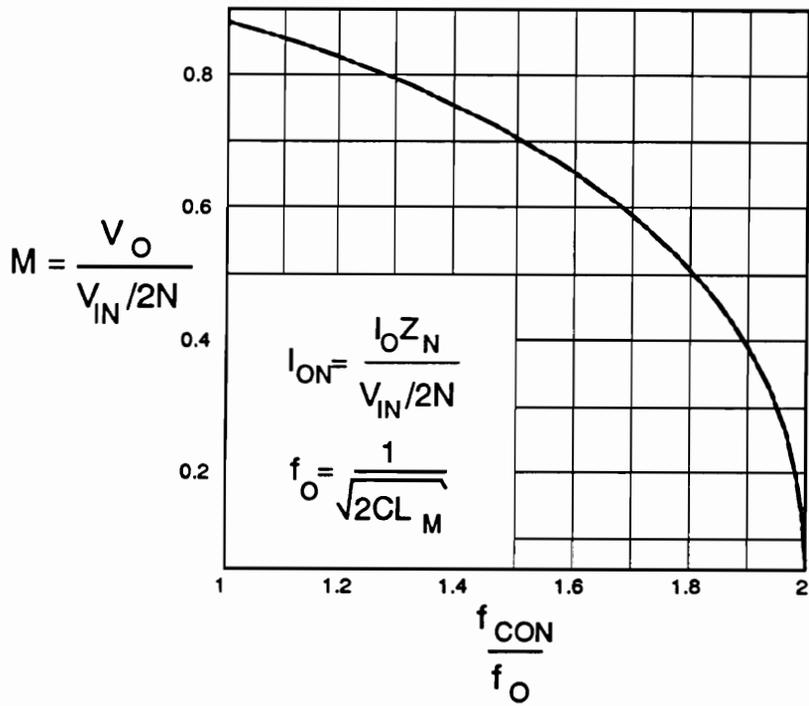
Figure 4.6. DC voltage-conversion-ratio characteristics of the HB ZVS-QRC (L_M) as a function of the normalized conversion frequency. $I_{ON} = 2I_O Z_O/(V_{IN}N)$, $Z_O = \sqrt{L_M/2C}$, and $f_O = 1/2\pi\sqrt{2CL_M}$.
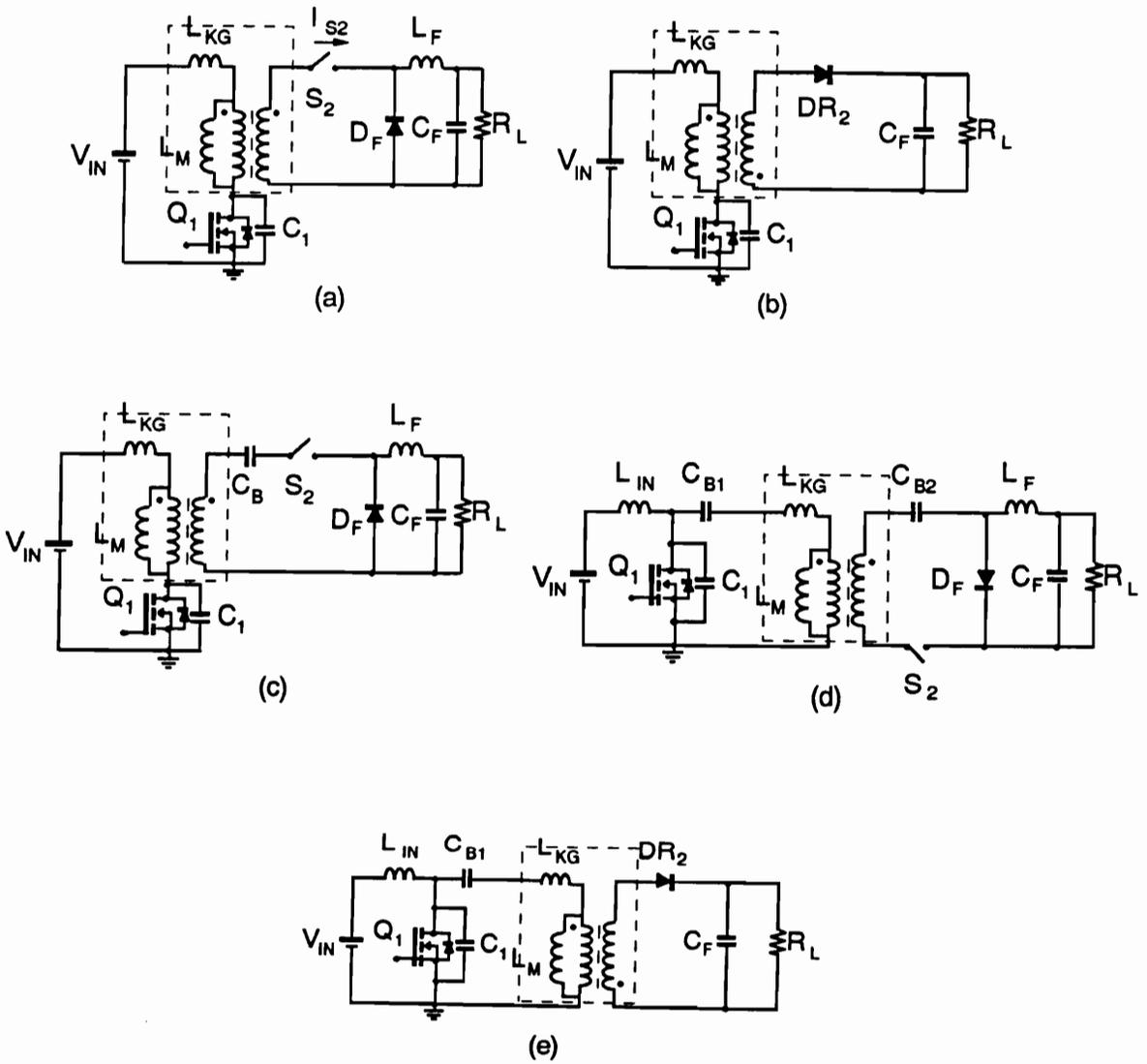
Figure 4.7. Basic isolated ZVS-QRC (L_M) topologies: (a) forward; (b) flyback; (c) zeta; (d) cuk; (e) sepic.
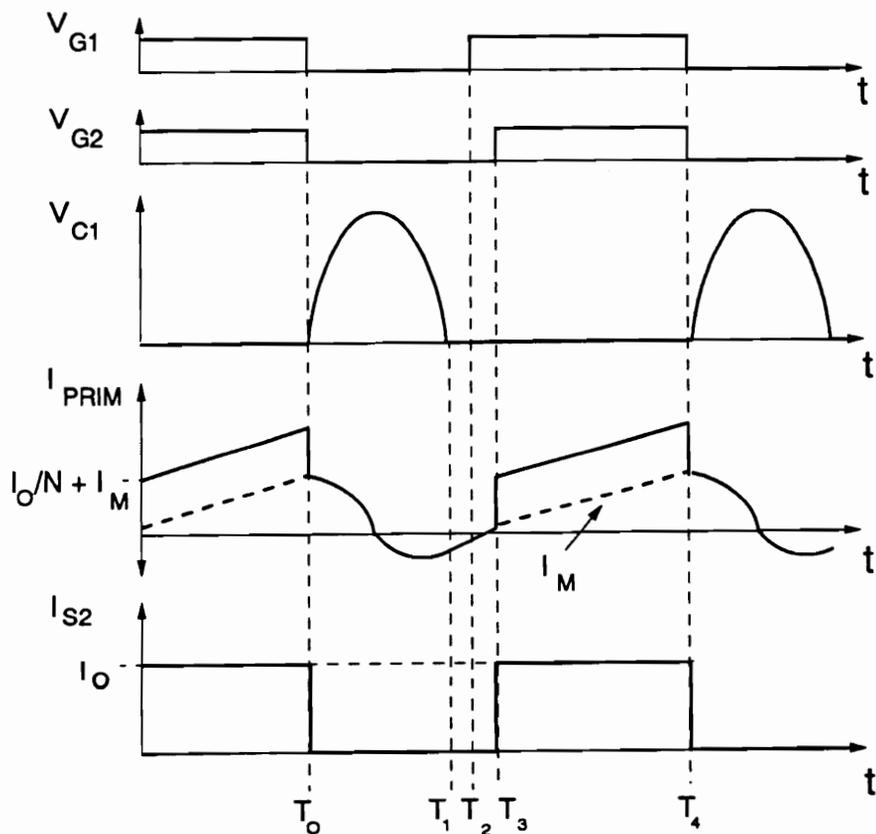
Figure 4.8. Ideal waveforms of the forward ZVS-QRC (L_M), from top to bottom: gate-source voltage of switch S_1, V_{G1}, gate-source voltage of switch S_2, V_{G2}, drain-source voltage of switch S_1, V_{DS1}, primary current I_{PRIM}, and current through secondary switch S_2. I_M and I_O represents the magnetizing and output load currents respectively.
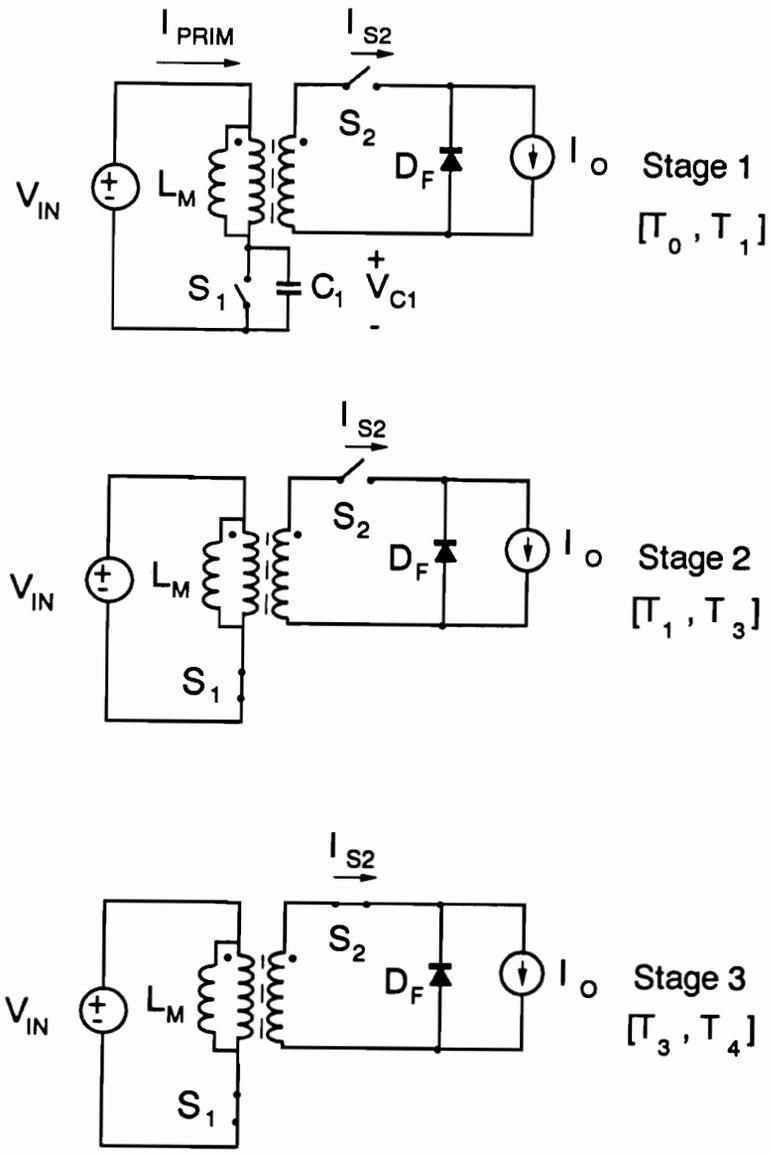
Figure 4.9. Topological stages of the forward ZVS-QRC (L_M).

age, then capacitance C_1 will naturally discharge to zero before switch S_1 is turned on. Although not given here, this can be easily shown by writing the differential equation describing Stage 4. If output voltages where $V_O/N < V_{IN}$ are desired, diode D_2 needs to be replaced by an active switch. By replacing diode D_2 with an active switch, the current through this second switch can be forced to conduct in the reverse direction, storing additional energy in the magnetizing inductance that can be used to switch Q_1 under zero-voltage conditions. The flyback as shown in Fig. 4.9 operates with a variable switching frequency.

If constant frequency operation is desirable for the flyback converter, diode D_2 needs to be replaced by a second active switch. By adding the second active switch, the conduction time of the rectifier switch (previously diode D_2) can be controlled. Another characteristic of the flyback and sepic topologies that should be mentioned is that because the magnetizing inductance is used as a resonant element, no resetting scheme is needed. This is the case for all single-ended topologies of this new family of converters.

4.2.3 Implementation

The switch that opens the secondary winding(s) of the power transformer during the resonant interval can be implemented in different ways. Figure 4.12 shows the implementation with a series combination of a saturable reactor and a rectifier diode [F2]. The saturable reactor provides the necessary blocking time to ensure that the resonant interval has ended before allowing the rectifier diode to conduct. Figure 4.13 (b) shows the HB topology implemented by replacing the secondary switches with the switch described in Fig. 4.11. Other isolated
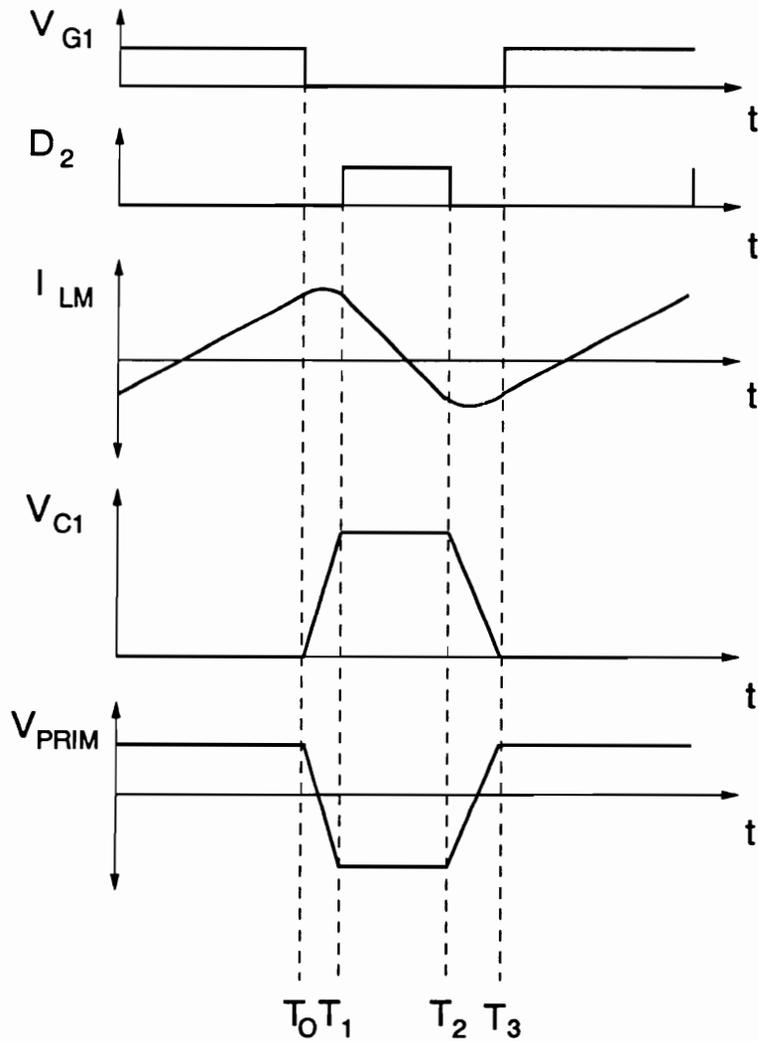
Figure 4.10. Ideal waveforms of the flyback ZVS-QRC (L_M), from top to bottom: gate-source voltage of switch S_1, on-time of rectifier diode D_2, magnetizing current I_{LM}, drain-source voltage of switch S_1, V_S, and primary transformer voltage V_{PRIM}.
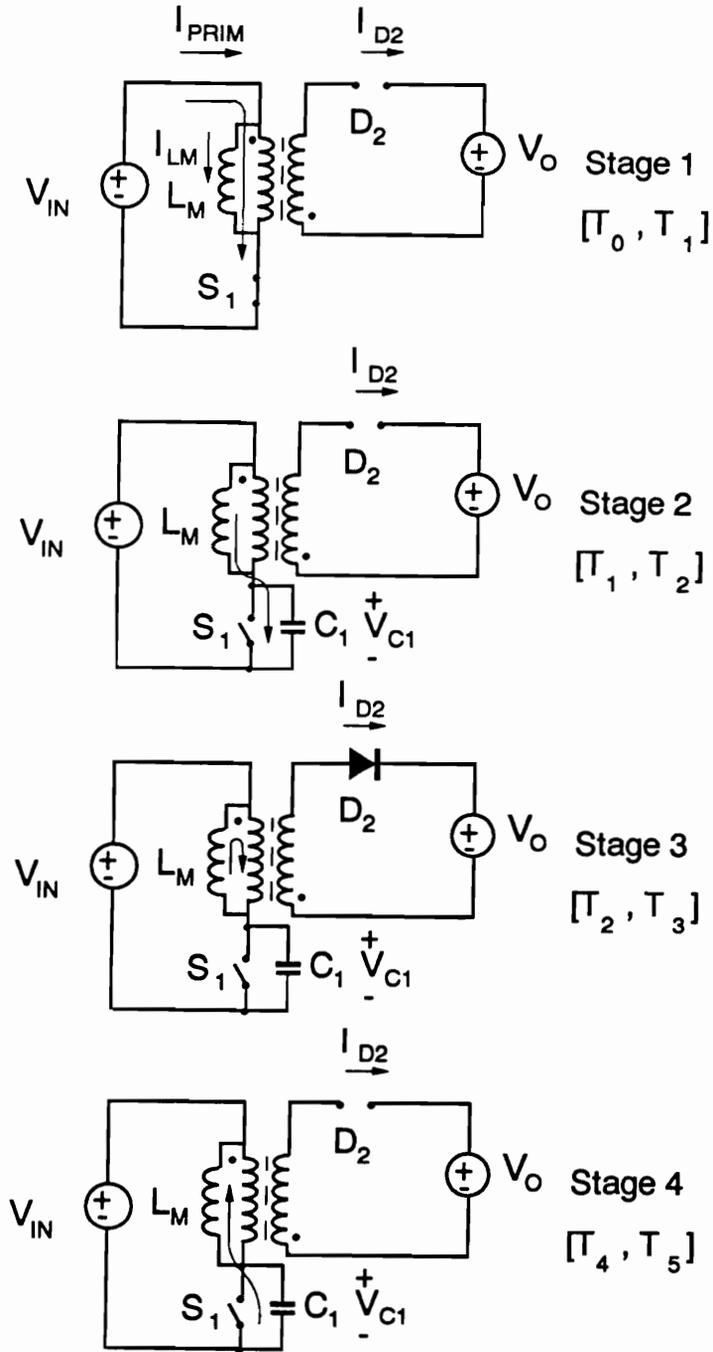
Figure 4.11.   Topological stages of the flyback ZVS-QRC (L_M).

topologies can be easily generated following the same procedure. It should be noted that the circuit in Fig. 4.13 requires variable frequency control because the saturable inductor blocking time is fixed.

Constant frequency operation of ZVS-QRC (L_M) requires an additional active switch in the rectifier circuit. The active switch in the primary side of the power stage is operated with constant switching frequency and constant duty cycle (off time is determined by ZVS condition) and the output voltage is regulated by PWM of the active switch in the secondary side. Therefore, constant frequency operation results in secondary side control. Secondary side control can easily be used in multiple output applications where all outputs have to be tightly regulated; i.e., the second active switch in the rectifier circuit is used as a postregulator. Furthermore, since ZVS of the primary switch(es) only depends on the interaction of the output capacitance of this switch(es) and the magnetizing inductance of the transformer, a common front end can be designed independently from the postregulated rectifier circuits. The front end can be designed for a maximum power rating exceeding that of the total output power, allowing for system expansion in the future.

4.2.4 Soft-Switching Rectifier Circuit

The output rectifiers of the converters shown in Figs. 4.7 and 4.13 turn off with an abrupt reverse voltage, resulting in parasitic ringings of the junction capacitance of the rectifier and the secondary side transformer leakage and lead inductances. To avoid the parasitic ringings, it is necessary to resonate the rectifier voltage in a controlled fashion as, for example, it is done
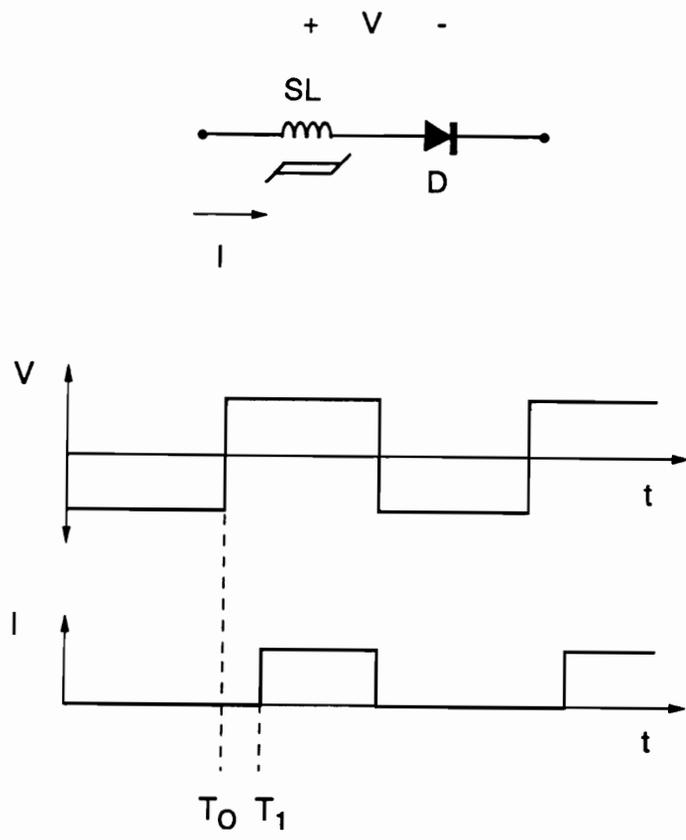
Figure 4.12. Magnetic switch: series combination of a saturable inductor and a rectifier diode.
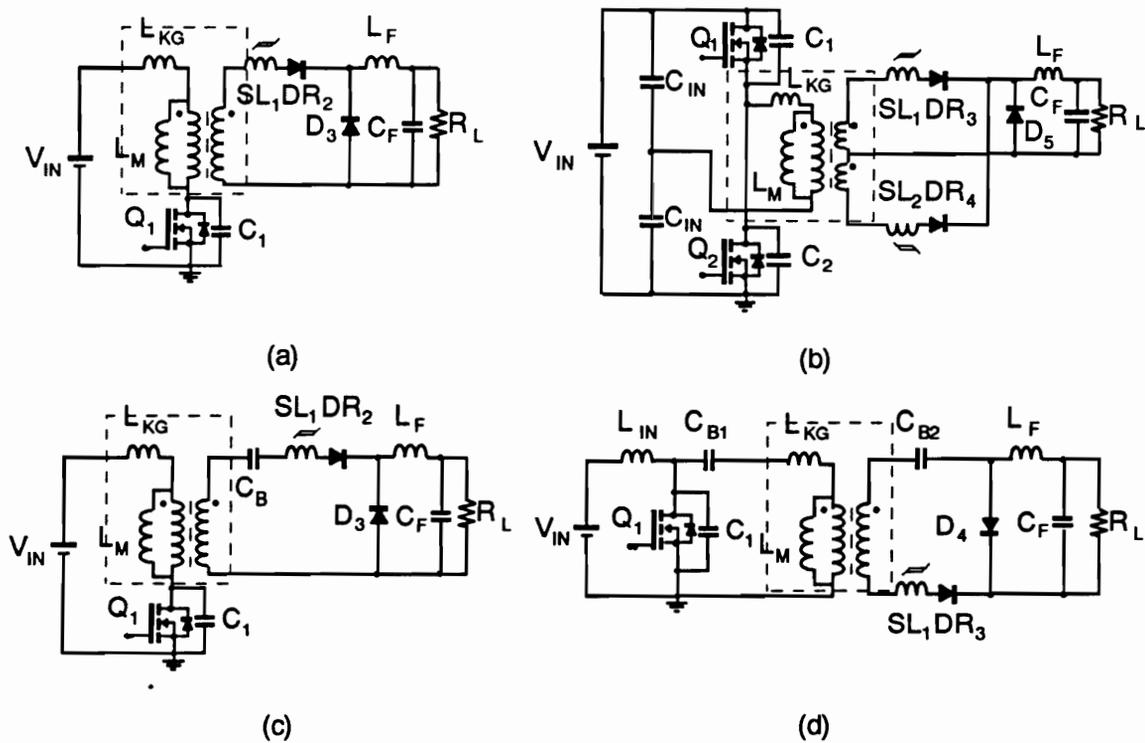
Figure 4.13. Implementation of the ZVS-QRC (L_M) using saturable inductors: (a) forward, (b) half-bridge, (c) zeta, and (d) cuk.

in ZVS-MRCs [D1,D2]. The rectifier-voltage resonance can be controlled by adding a linear inductor across the saturable inductor as shown in Fig. 4.14. The saturable inductor provides the needed blocking time (open circuit) to allow the magnetizing inductance to achieve ZVS of the primary side switches. The linear inductor provides a path for the parasitic capacitance of the nonconducting rectifier to charge and discharge in a controlled fashion. The linear inductor can be designed to carry a small fraction of the total load current, thereby minimizing the circulating energy in these converters. All semiconductor devices, with the exception of the freewheeling diode, switch at zero voltage. The basic variable frequency ZVS isolated topologies with soft switching in all semiconductor devices implemented with saturable inductors (ZVS-MRC (L_M)) are shown in Fig. 4.15. Constant frequency operation of these converters is possible by controlling the blocking time of the saturable inductor(s). The implementation of the HB ZVS-MRC (L_M) operating with a constant switching frequency will be discussed in the following chapter.

4.5 Summary

A new family of isolated ZVS converters which utilize the magnetizing inductance of the power transformer to achieve zero voltage turn-on of the primary switches has been presented. By employing saturable inductors, the concept was extended so that soft switching of the output rectifiers is obtained with a minimum circulating energy flowing through the converter. The proposed converters can operate with a variable or constant switching frequency. A complete dc analysis, design guidelines, and experimental results for the HB converter are presented
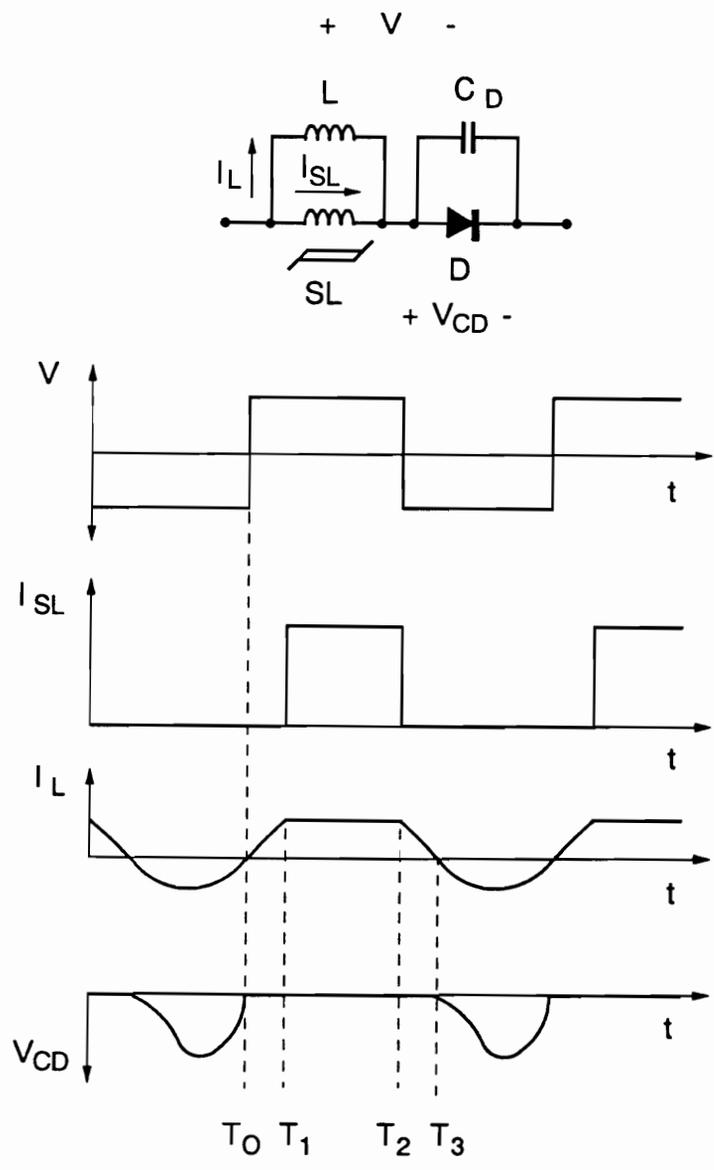
Figure 4.14. The soft-switched magnetic switch.
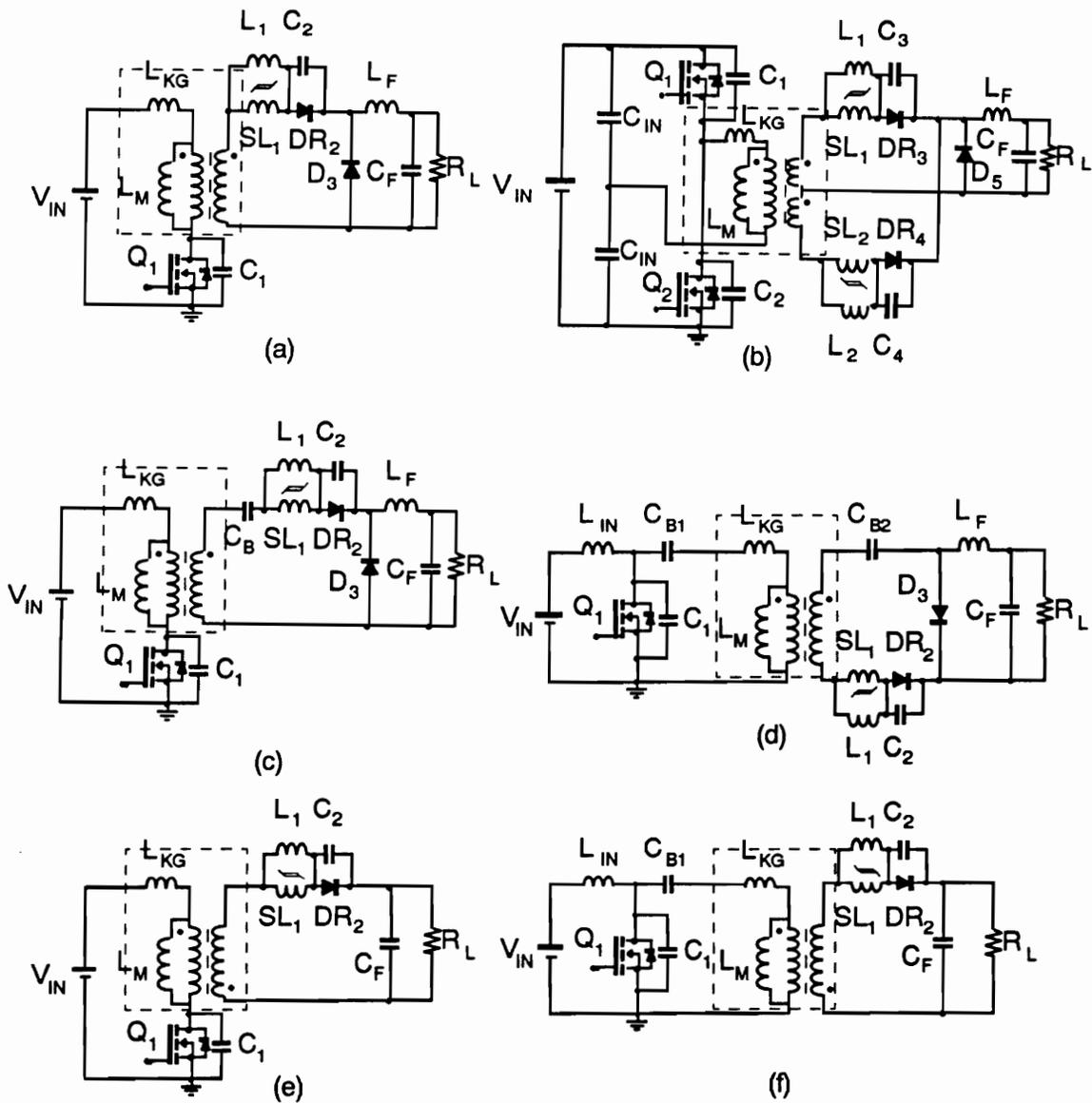
Figure 4.15. Soft switching implementation of the rectifier circuit in ZVS (L_M) converters: (a) forward, (b) half-bridge, (c) zeta, (d) cuk, (e) flyback, and (f) sepic.

in the next chapter. In the following chapter, a detailed analysis of the operation of the HB topology (Fig. 4.14(b)) is presented.

5. DC ANALYSIS AND IMPLEMENTATION

OF THE HB ZVS-MRC (L_M)

5.1 Introduction

A new family of converters that uses the magnetizing inductance as a resonant element was introduced in the previous chapter. By using the magnetizing inductance as a resonant component the need for using an external resonant inductor to achieve ZVS is eliminated. The bridge-type topologies of this new family of ZVS converters exhibit a very desirable property. These converters clamp the resonant voltage across the primary switches, resulting in a very short resonant interval. Since the resonant interval in these converters is only a small fraction of the total switching cycle, the current and voltage waveforms are squarewave shaped like those of PWM converters. PWM-type waveforms are very desirable since they result in low conduction losses and minimize circulating energy.

Chapter 4 discussed how the parallel combination of a linear and saturable inductor is used to obtain soft switching of the rectifier circuit for this new family of converters. Using saturable inductors to implement the soft switching rectifier circuit helps keep the circulating energy flowing through the converter at a minimum. This means that for the HB topology, the current and voltage waveforms are mostly squarewave shaped and there is not much energy circulating through the converter. In this chapter, the dc analysis of the HB ZVS-MRC (L_M) is studied in detail. First, only variable frequency operation is considered in the analysis. Like most resonant topologies, this converter is found to operate in more than one mode. The dc voltage conversion ratio and stress analysis characteristics obtained from the dc analysis are used in design trade-off studies. The trade-off study is used to define design guidelines for the HB ZVS-MRC (L_M).

The last section of this chapter studies the implementation of the HB ZVS-MRC (L_M) using controllable saturable inductors. By controlling the blocking time of the saturable inductors, the soft-switched HB can operate at a constant switching frequency. Finally, experimental results for a 100 W HB ZVS-MRC (L_M) operating with variable and constant switching frequency are presented.

5.2 Operation of the HB ZVS-MRC (L_M)

The ZVS-MRC L_M is shown in Fig. 5.1. The primary switches Q_1 and Q_2 of this converter are turned on under zero voltage and the rectifier diodes DR_3 and DR_4 are turned on under soft
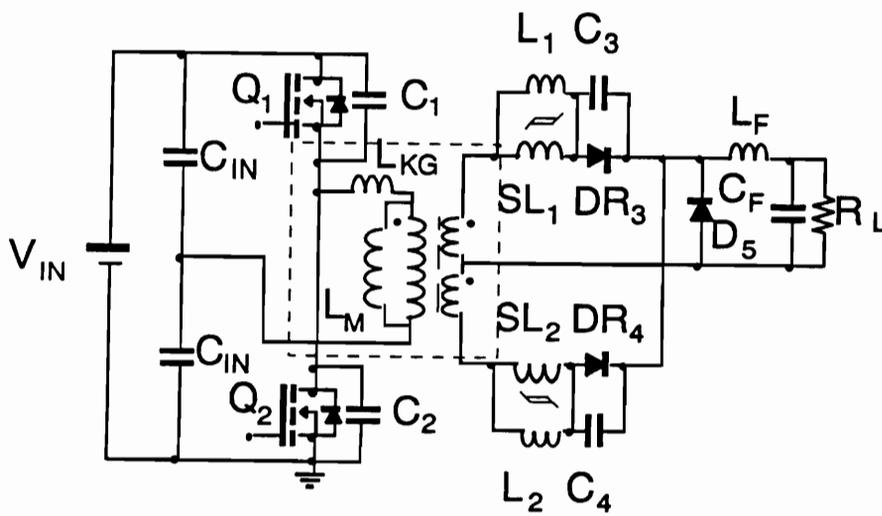
Figure 5.1.   The HB ZVS-MRC (L_M).

switching conditions. ZVS of the primary switches is achieved by allowing capacitances C_1 and C_2 to resonate with the magnetizing inductance during the switching transition. This switching transition is very short due to the voltage clamping of the primary switches that is characteristic of all bridge-type topologies. Soft switching of the rectifier diodes is achieved by allowing capacitance C_3 and C_4 to charge and discharge in a controlled fashion through the linear inductor in parallel with the saturable inductor and in series with the rectifier diodes. The linear inductors carry only a small fraction of the total current when the rectifier diodes are forward biased. Most of the load current flows through the saturable inductors. Like a typical HB converter, when rectifier DR_3 is forward biased, rectifier DR_4 is reversed biased and vice versa. As can be seen from the previous discussion, capacitances C_1, C_2, C_3, and C_4 are resonant capacitances, and L_1, L_2, and L_M are the resonant inductors of the converter.

5.2.1 DC Analysis

To simplify the analysis of the HB ZVS-MRC (L_M), it is assumed that:

a) the output filter inductance is sufficiently large so that it can be approximated by a current source with a value equal to the output current, I_O;

b) the voltage drops across the conducting semiconductor switches (MOSFETs and diodes) are negligible;

c) the switching times of the semiconductor switches are zero;

d) transformer leakage inductance is negligible;

e) $C = C_1 = C_2$; $C_D = C_3 = C_4$; and $L = L_1 = L_2$;

f) the saturable inductors, SL_1 and SL_2, are identical;

g) the slope of the saturable inductance SL_1 and SL_2 is defined by the ratio L/SL (ratio of the linear inductance to saturable inductance); and

h) the current through the linear inductor L at the time the corresponding saturable inductor saturates is I_{SAT} as shown in Fig. 5.2(b).

The representation of the saturable inductor is shown in Fig. 5.2(a). The inductors block all current when not saturated. Once saturated, it behaves like an inductor with very low inductance.

During a switching cycle, the converter enters a sequence of seven or eight topological stages during heavy load and light load operation, respectively. Each sequence of topological stages represents a different mode of operation. Figure 5.3 shows the different possible topological stages.

The operation of the HB ZVS-MRC (L_M) is classified into four major modes of operation. The first three modes occur for heavy load conditions, while the fourth mode is found at light load operation. Since light-load operation is not important for the design of the converter, it will not be discussed in detail.
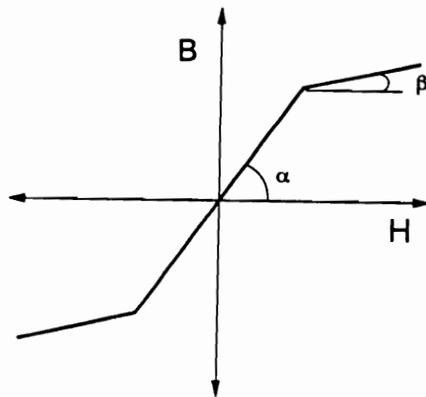
β = Slope in Saturated Region

α = Slope in Linear Region

$$L/SL = \frac{\alpha}{\beta}$$

(a)
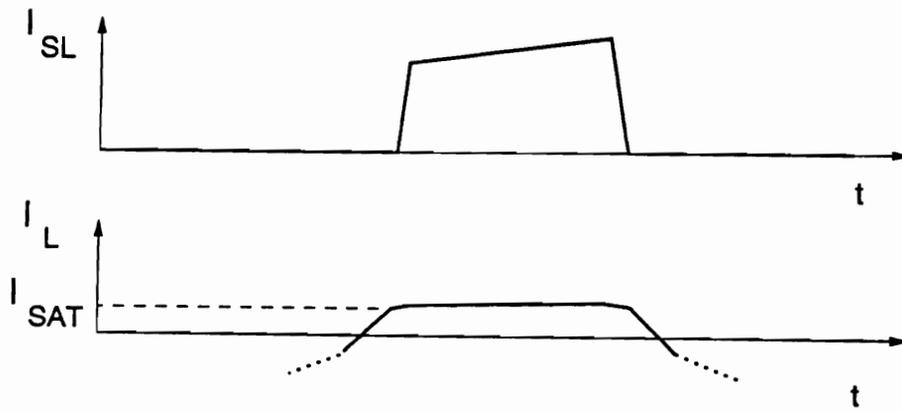
(b)

Figure 5.2. (a) Representation of the saturable inductor for dc analysis; (b) Current through the linear and saturable inductor with SL saturated.
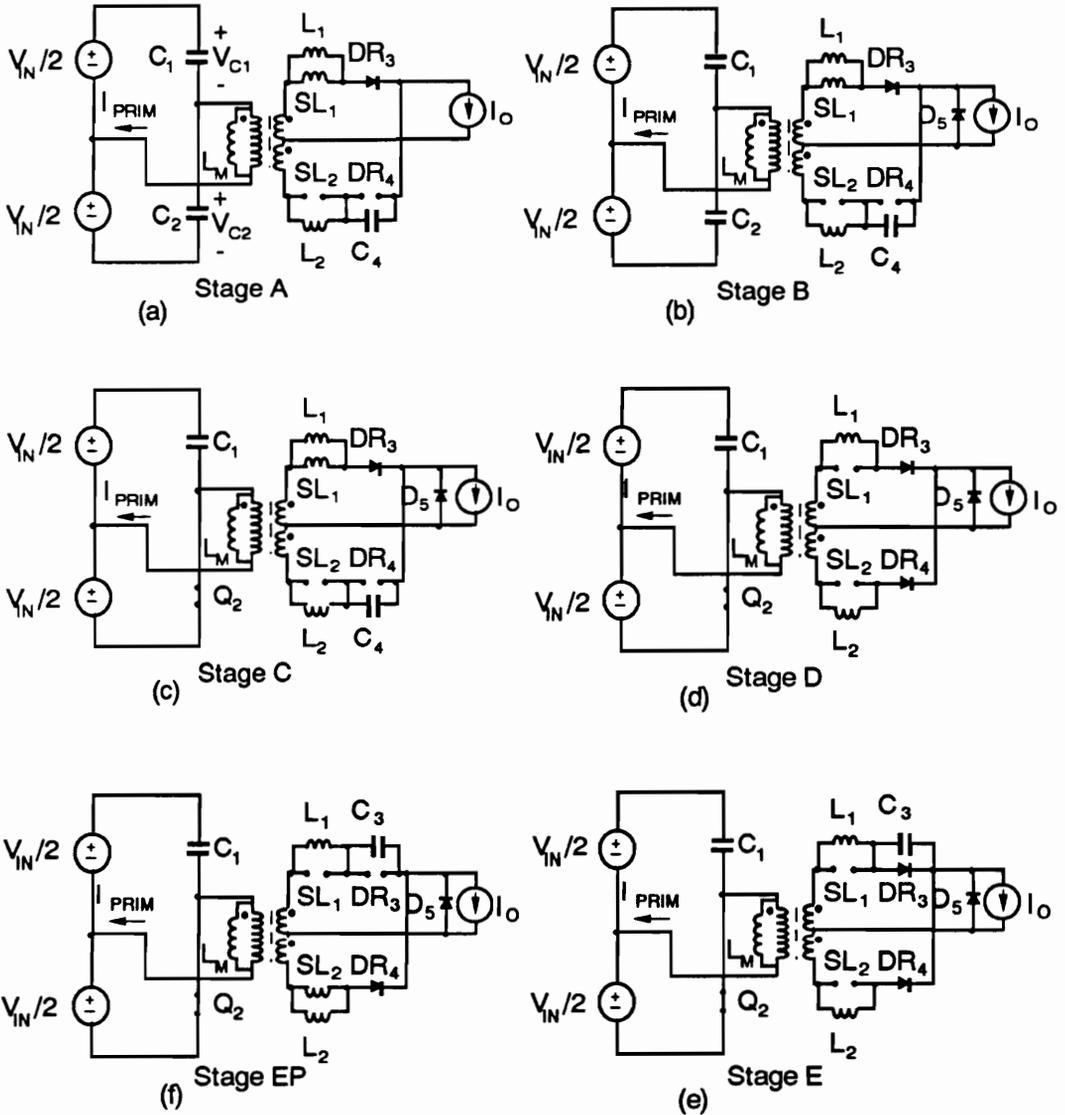
Figure 5.3a. Topological stage of the HB ZVS-MRC (L_M):
(a) Stage A, (b) Stage B, (c) Stage C, (d) Stage D, (e) Stage E, and (f) Stage EP.
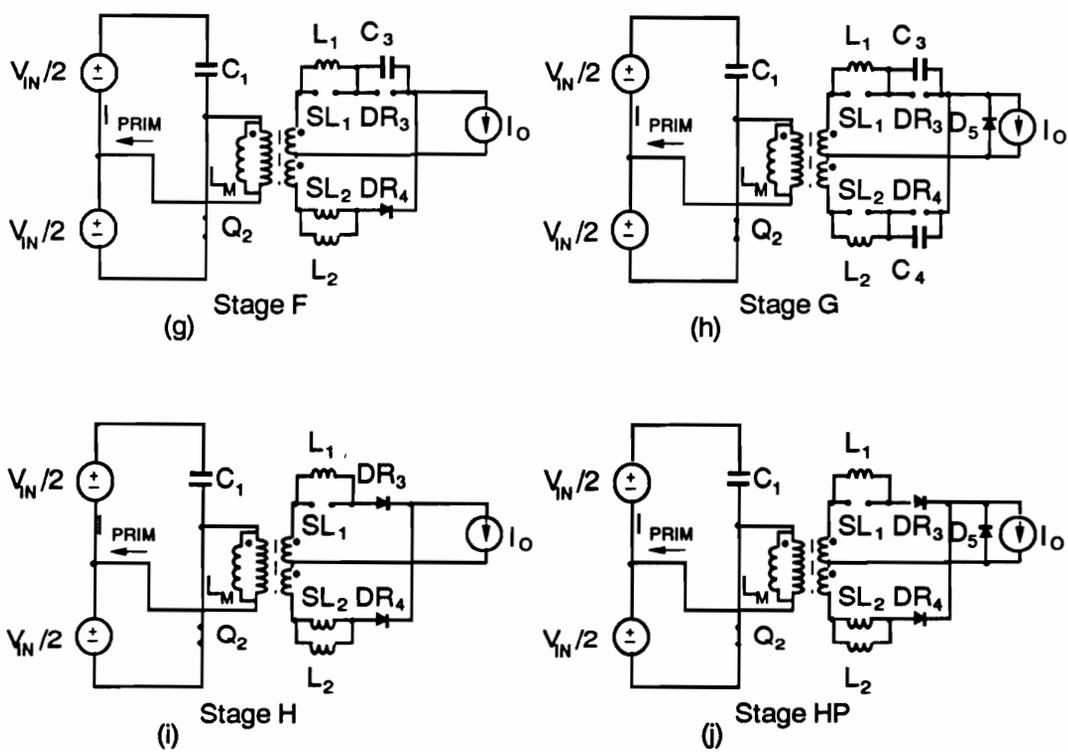
Figure 5.3b. Topological stage of the HB ZVS-MRC (L_M):
(g) Stage F, (h) Stage G, (i) Stage H, and (j) Stage HP.
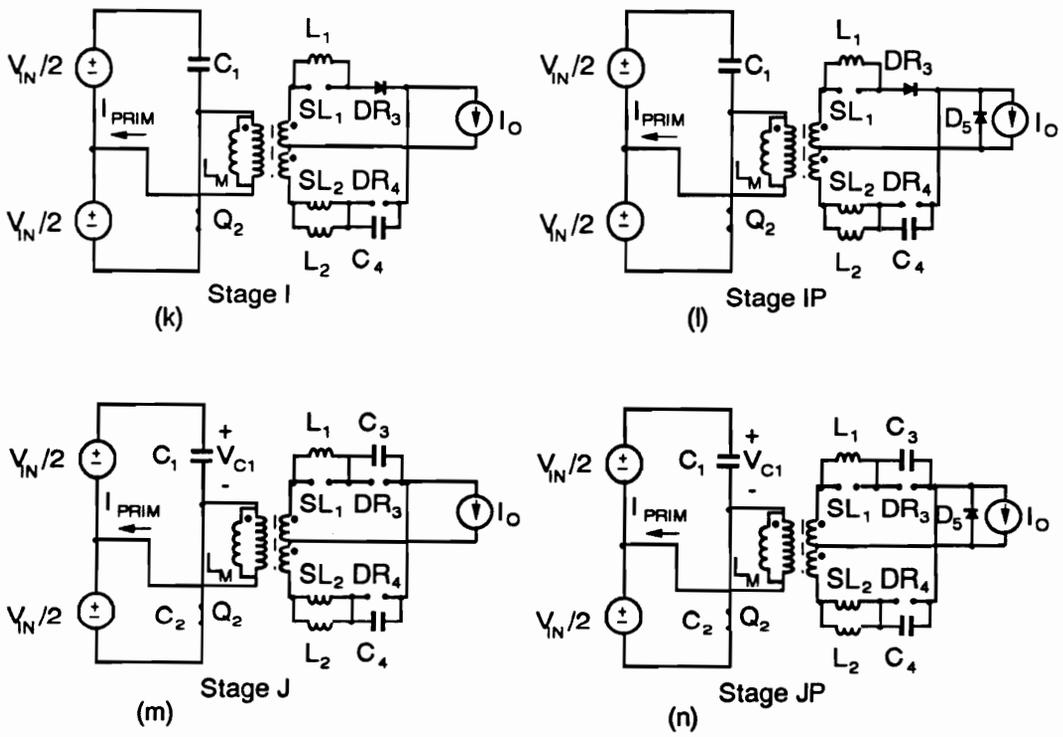
Figure 5.3c. Topological stage of the HB ZVS-MRC (L_M):
(k) Stage I, (l) Stage IP, (m) Stage J, and (n) Stage JP.

5.2.1.1 Mode I of Operation

The sequence of topological stages for Mode I.A is A-B-C-D-HP-H-F. Figure 5.4 shows the key waveforms of the soft switched HB operating on this mode. Figure 5.4b shows an expanded view of the switching transition.

Prior to the turn-off of switch Q_1, load current I_O flows through the upper secondary and the primary current flows through Q_1. Voltage across C_1, V_{C1}, is zero, and voltage across C_2, V_{C2}, is equal to the supply voltage V_{IN}. Inductor SL_1 is saturated, whereas inductor SL_2 is unsaturated.

Stage A [T_0, T_1], Fig. 5.3(a)

At $t = T_O$, Q_1 is turned off, and the primary current is diverted into C_1 and C_2. Capacitance C_1 starts charging while C_2 starts discharging at the same rate. Inductor SL_1 remains saturated, and rectifier DR_3 continues to conduct. In this stage, inductor SL_2 is blocking and capacitance C_4 resonates with inductor L_2. The stage ends at time T_1 when primary voltage becomes zero, i.e., $V_{C1}(T_1) = V_{C2}(T_1) = V_{IN}/2$.

Stage B [T_1, T_2], Fig. 5.3(b)

In Stage B, capacitances C_1 and C_2 start to resonate with the magnetizing inductance of the power transformer and the negative primary voltage begins to reset SL_1. The current through SL_1 decreases quickly as the saturable reactor becomes unsaturated. Capacitance C_1 continues to charge, and C_2 continues to discharge. At the beginning of Stage B most of the load current is diverted to the freewheeling diode. However, rectifier DR_3 continues to conduct
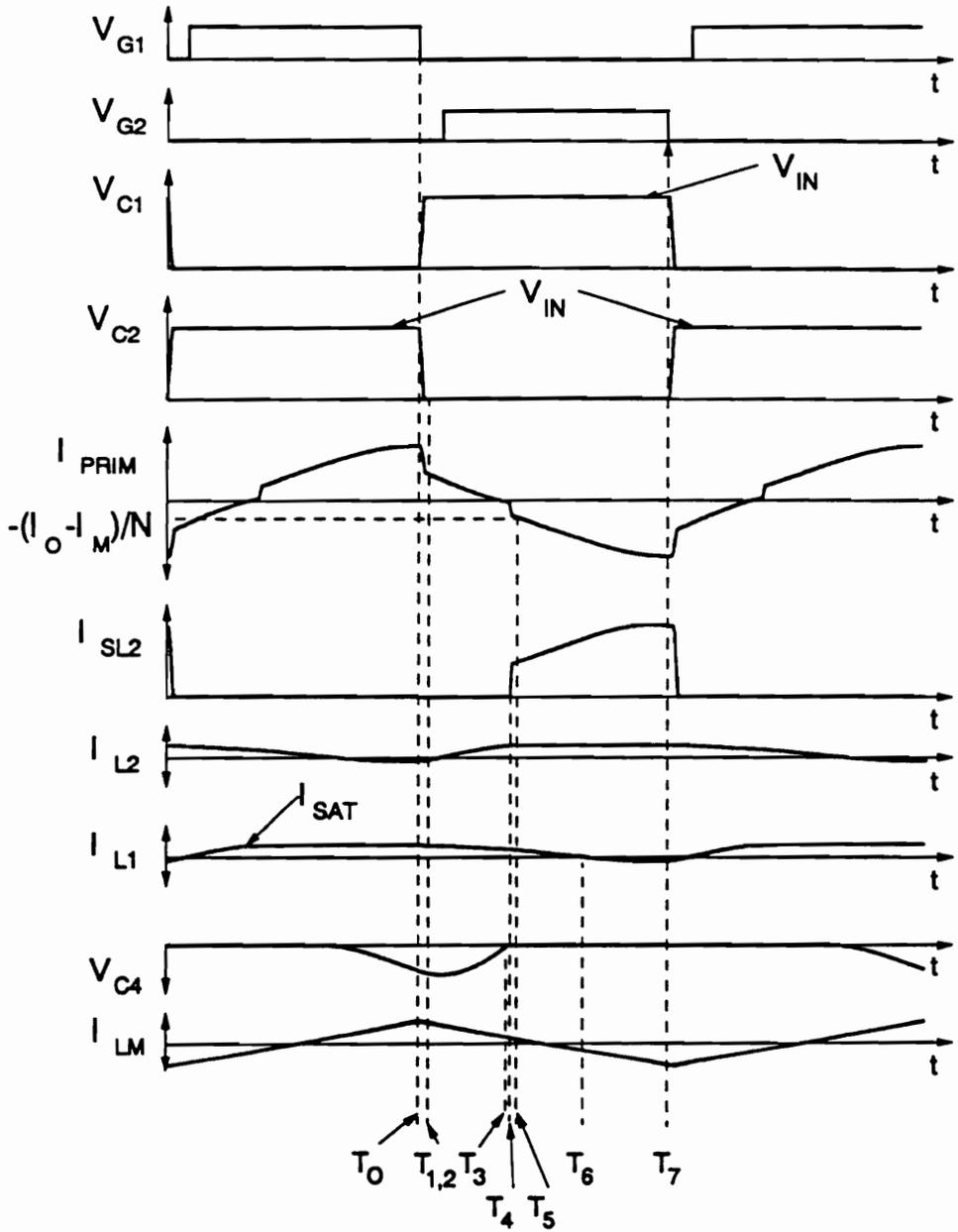
Figure 5.4a. Ideal waveforms of the HB ZVS-MRC (L_M) operating in Mode I.A, from top to bottom: gate-source voltage V_{G1}, gate-source voltage V_{G2}, switch Q_1 voltage V_{C1}, switch Q_2 voltage V_{C2}, primary current I_{PRIM}, saturable inductor current I_{SL2}, linear inductor current I_{L2}, linear inductor current I_{L1}, and rectifier capacitor voltage V_{C4}.
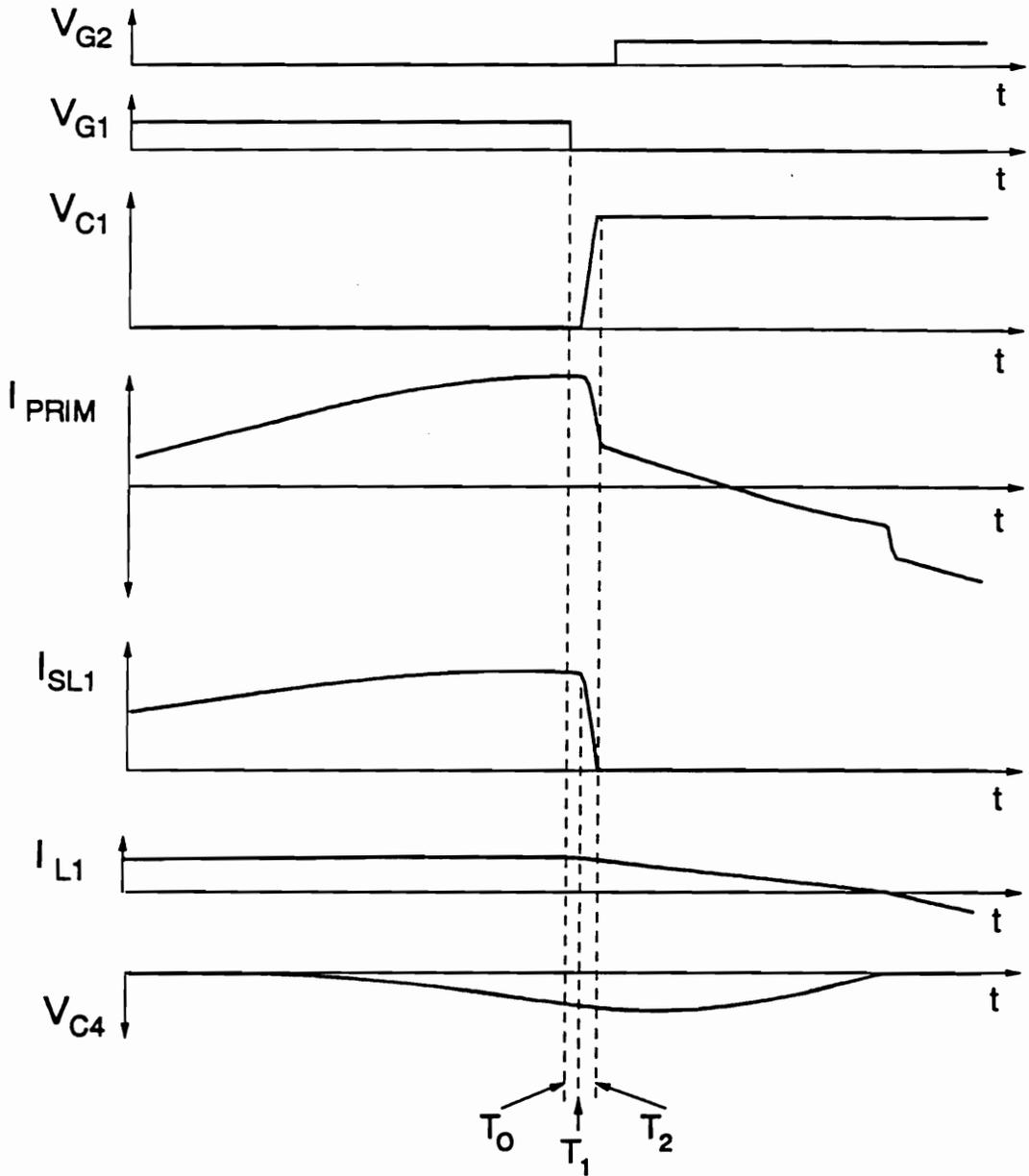
Figure 5.4b. Ideal waveforms of the HB ZVS-MRC (L_M) operating in Mode I.A; switching transition $[T_0 - T_2]$, from top to bottom: gate-source voltage V_{G1}, gate-source voltage V_{G2}, switch Q_1 voltage V_{C1}, switch Q_2 voltage V_{C2}, primary current I_{PRIM}, saturable inductor current I_{SL2}, linear inductor current I_{L2}, linear inductor current I_{L1}, and rectifier capacitor voltage V_{C4}.

since a small, positive, current (5-10 % of the load current) flows through inductor L_1. The current through L_1 decreases to zero due to the negative voltage across the upper secondary. At the same time, inductor L_2 and capacitor C_4 continue to resonate. This stage ends at time T_2 when the voltage across capacitor C_2 becomes zero, and the antiparallel diode of Q_2 starts conducting. Switch Q_2 should be turned on while its antiparallel diode is conducting to achieve ZVS.

Stage C [T_2, T_3], Fig. 5.3(c)

During Stage C, inductor L_1 continues to discharge, inductor L_2 and capacitor C_4 continue to resonate, and saturable inductor SL_1 continues to reset. During this stage, the current through SL_1 decreases to zero. Since the the negative voltage across the upper secondary is constant $(-V_{IN}/N)$, current through L_1 decreases linearly. Also, the freewheeling diode continues to conduct. This stage ends at time T_3 when the voltage across capacitor C_4 completely discharges and rectifier DR_4 turns on.

Stage D [T_3, T_4], Fig. 5.3(d)

In Stage D, both saturable inductors are blocking. Current through L_1 continues to decrease and current through inductor L_2 increases linearly. The freewheeling diode continues to carry most of the load current. This stage ends at time T_4 when inductor SL_2 saturates.

Stage HP [T_4, T_5], Fig. 5.3(d)

In Stage HP, the current through the saturable inductor SL_2 increases rapidly since this inductor is saturated. The freewheeling diode continues to conduct until the current through

SL_2 is large enough to supply the load. The current through L_1 continues to increase and the current through L_2 to decrease in a linear manner. Stage HP ends when the sum of the current through L_1, L_2, and SL_2 equals the load current there by turning the freewheeling diode off.

Stage H [T_5, T_6], Fig. 5.3(d)

In this stage, the load current is supplied by saturable inductor SL_2. The current through L_1 continues to linearly decrease and the current through L_2 and SL_2 to increase also in a linear manner. This stage ends at time T_6 when the current through L_1 decreases to zero and diode DR_3 turns off.

Stage F [T_6, T_7], Fig. 5.3(f)

In Stage F, inductor SL_1 continues to block and capacitor C_3 begins resonating with inductor L_1. Inductor SL_2 remains saturated and most of the load current flows through SL_2. This stage ends when switch Q_2 is turned off, initiating a new conversion cycle.

5.2.1.2 Mode II of Operation

In Mode II of operation the current through the linear inductor L_1 decreases to zero, turning off rectifier diode DR_3 before capacitor C_4 completely discharges to zero. The change in polarity of the current through L_1 initiates the resonance between this inductance and rectifier capacitance C_3. In this mode, rectifier capacitances C_3 and C_4 will both resonate with the lin-

ear inductors at the same time. Mode II results in higher dc voltage-conversion-ratios relative to Mode I.

5.2.1.3 Mode III of Operation

In Mode III of operation, SL_2 saturates before capacitor C_4 discharges completely (Mode I of operation) or the current through linear inductor L_1 reverses its polarity (Mode II of operation). This mode maximizes the time duration of the power transferring stages, resulting in higher dc voltage-conversion ratios relative to the two previous modes of operation.

Figures 5.4 to 5.15 show the typical waveforms of the HB ZVS-MRC (L_M) for the different modes of operation. Table 5.1 summarizes the topological sequences for the different modes of operation. The topological stages _P where _ is a letter from E to J, represent the converter during the time in which saturable inductor SL_2 is saturated, but its current has not increased to the necessary value so as to turn off the freewheeling diode. These stages represent the switching transition of the magnetic switch.

5.2.1.4 Light Load Operation

For heavy to medium load operation, the saturable reactors SL_1 and SL_2 supply most of the load current, while the linear inductors, L_1 and L_2, carry 10 to 20% of the total load current. Heavy load currents result in increased delay between the time the saturable reactor begins
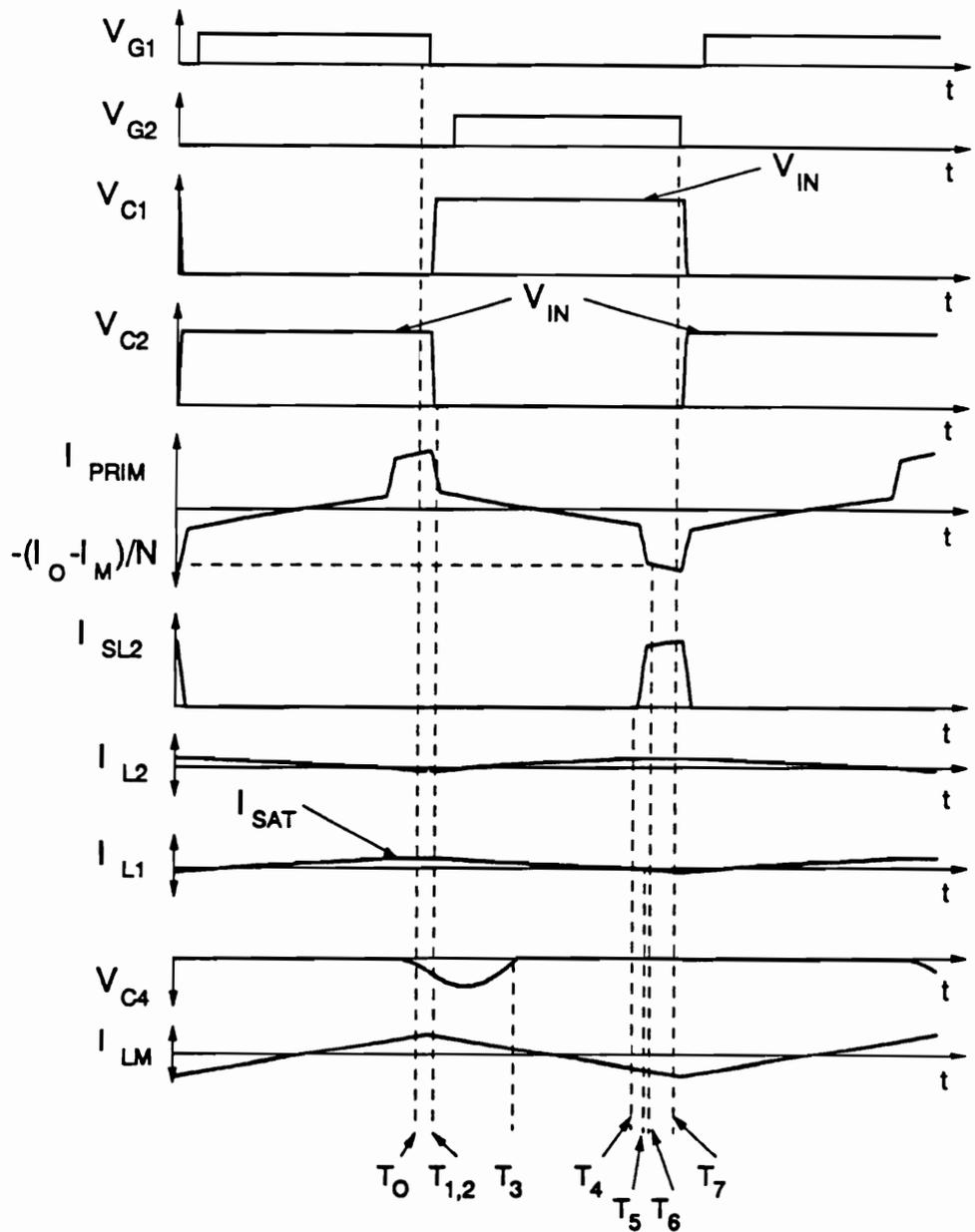
Figure 5.5. Ideal waveforms of the HB ZVS-MRC (L_M) operating in Mode I.B, from top to bottom: gate-source voltage V_{G1}, gate-source voltage V_{G2}, switch Q_1 voltage V_{C1}, switch Q_2 voltage V_{C2}, primary current I_{PRIM}, saturable inductor current I_{SL2}, linear inductor current I_{L2}, linear inductor current I_{L1}, and rectifier capacitor voltage V_{C4}.
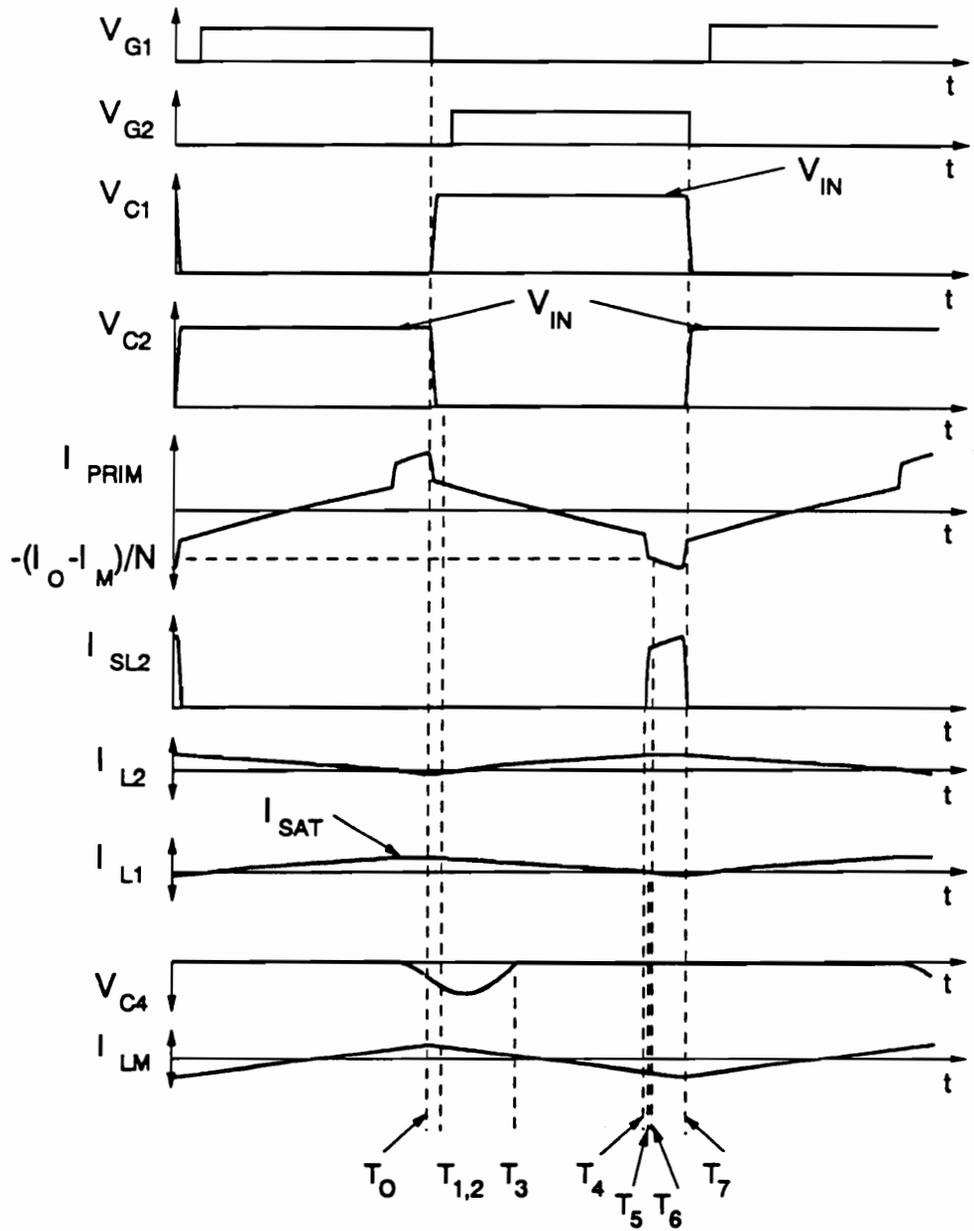
Figure 5.6. Ideal waveforms of the HB ZVS-MRC (L_M) operating in Mode I.C, from top to bottom: gate-source voltage V_{G1}, gate-source voltage V_{G2}, switch Q_1 voltage V_{C1}, switch Q_2 voltage V_{C2}, primary current I_{PRIM}, saturable inductor current I_{SL2}, linear inductor current I_{L2}, linear inductor current I_{L1}, and rectifier capacitor voltage V_{C4}.
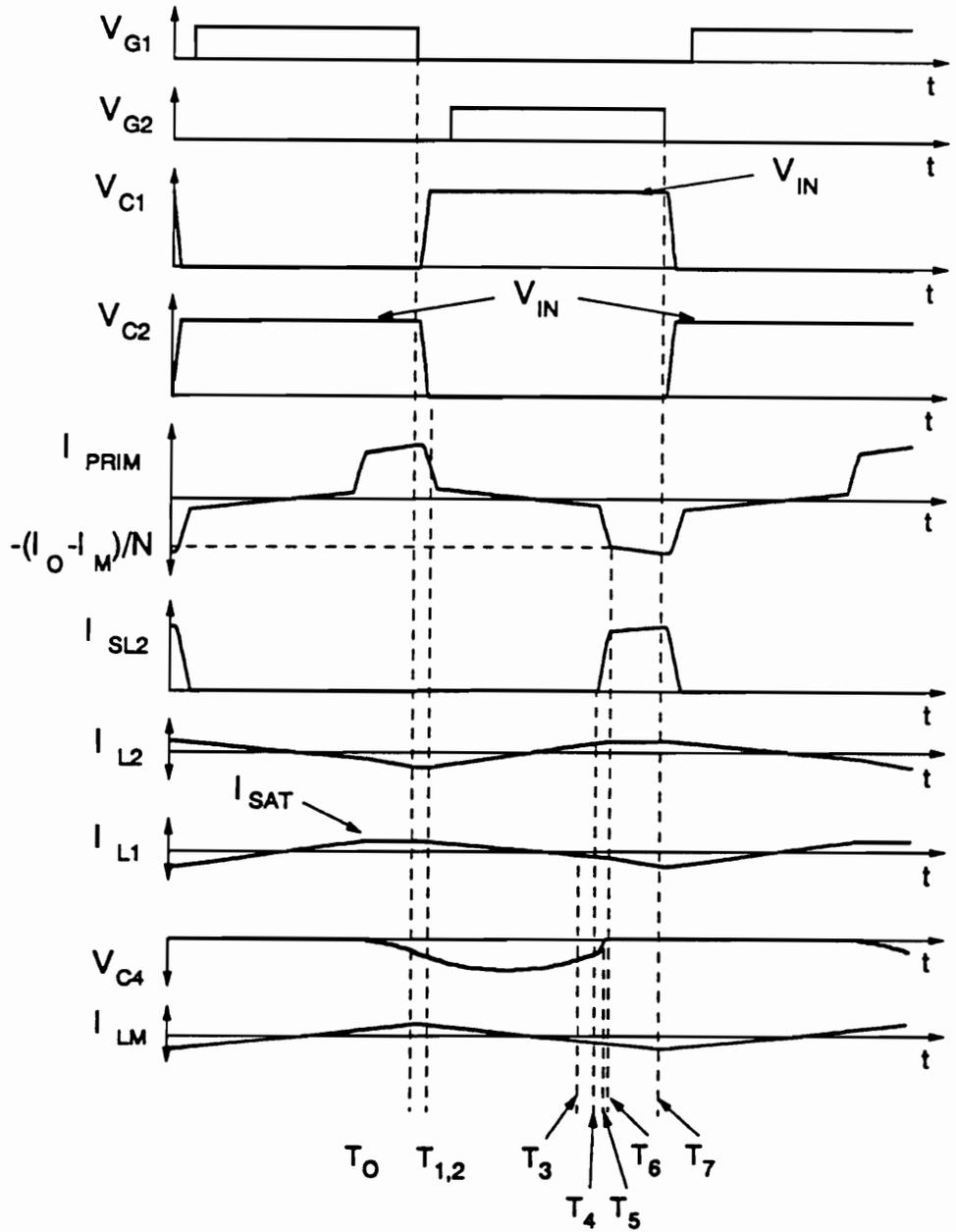
Figure 5.7. Ideal waveforms of the HB ZVS-MRC (L_M) operating in Mode II.A, from top to bottom: gate-source voltage V_{G1}, gate-source voltage V_{G2}, switch Q_1 voltage V_{C1}, switch Q_2 voltage V_{C2}, primary current I_{PRIM}, saturable inductor current I_{SL2}, linear inductor current I_{L2}, linear inductor current I_{L1}, and rectifier capacitor voltage V_{C4}.
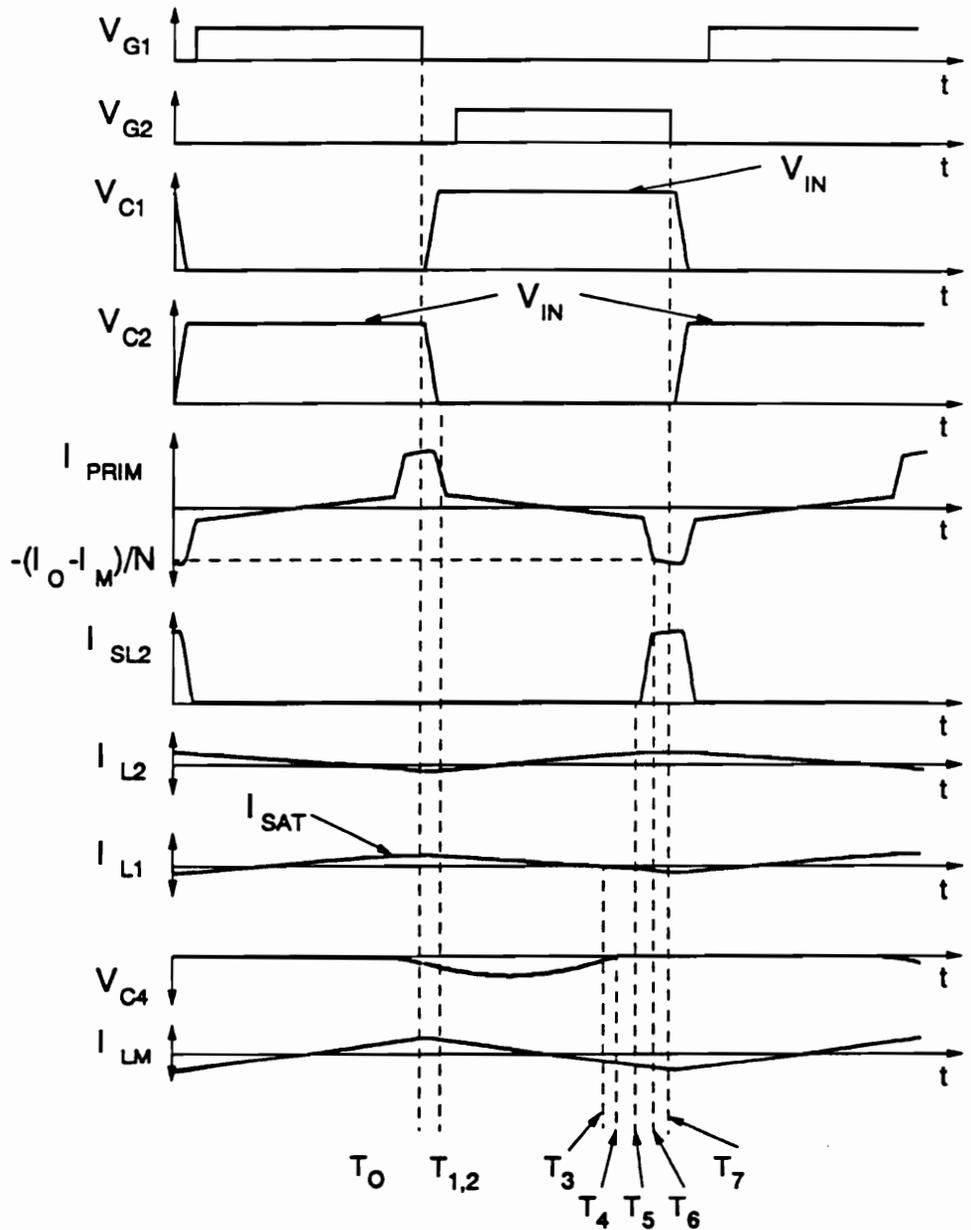
Figure 5.8. Ideal waveforms of the HB ZVS-MRC (L_M) operating in Mode II.B, from top to bottom: gate-source voltage V_{G1}, gate-source voltage V_{G2}, switch Q_1 voltage V_{C1}, switch Q_2 voltage V_{C2}, primary current I_{PRIM}, saturable inductor current I_{SL2}, linear inductor current I_{L2}, linear inductor current I_{L1}, and rectifier capacitor voltage V_{C4}.
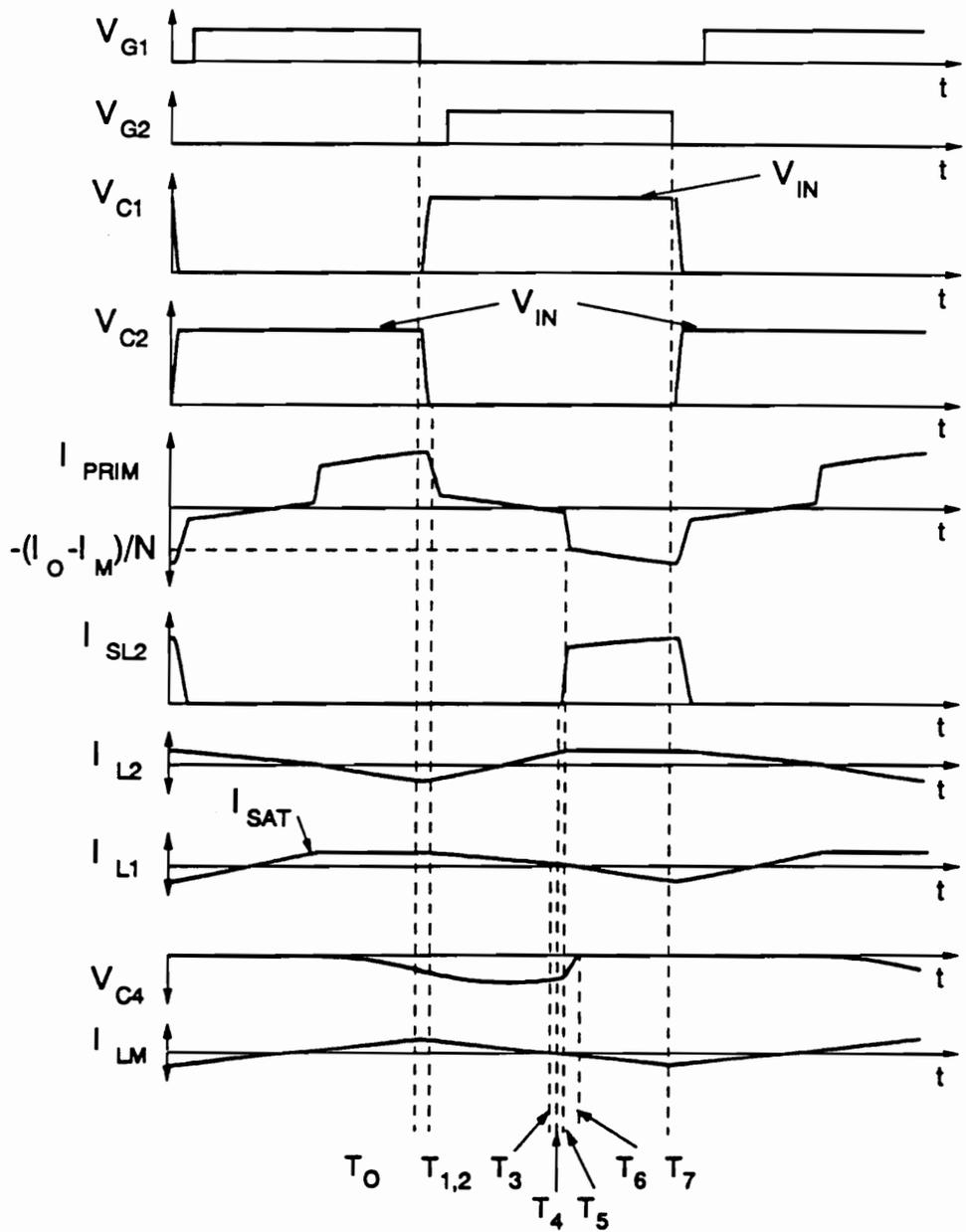
Figure 5.9. Ideal waveforms of the HB ZVS-MRC (L_M) operating in Mode II.C, from top to bottom: gate-source voltage V_{G1}, gate-source voltage V_{G2}, switch Q_1 voltage V_{C1}, switch Q_2 voltage V_{C2}, primary current I_{PRIM}, saturable inductor current I_{SL2}, linear inductor current I_{L2}, linear inductor current I_{L1}, and rectifier capacitor voltage V_{C4}.
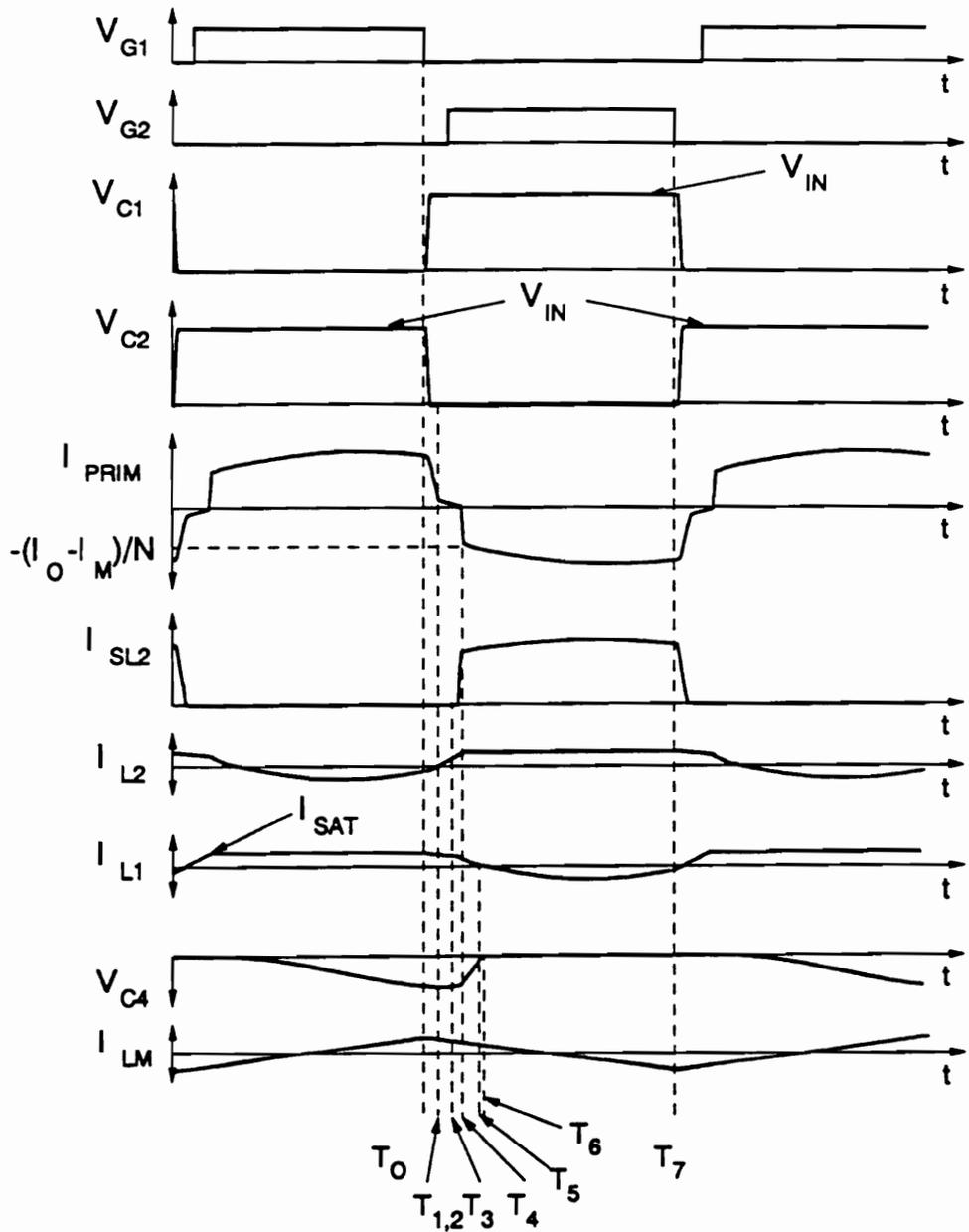
Figure 5.10.   Ideal waveforms of the HB ZVS-MRC (L_M) operating in Mode III.A, from top to bottom: gate-source voltage V_{G1}, gate-source voltage V_{G2}, switch Q_1 voltage V_{C1}, switch Q_2 voltage V_{C2}, primary current I_{PRIM}, saturable inductor current I_{SL2}, linear inductor current I_{L2}, linear inductor current I_{L1}, and rectifier capacitor voltage V_{C4}.
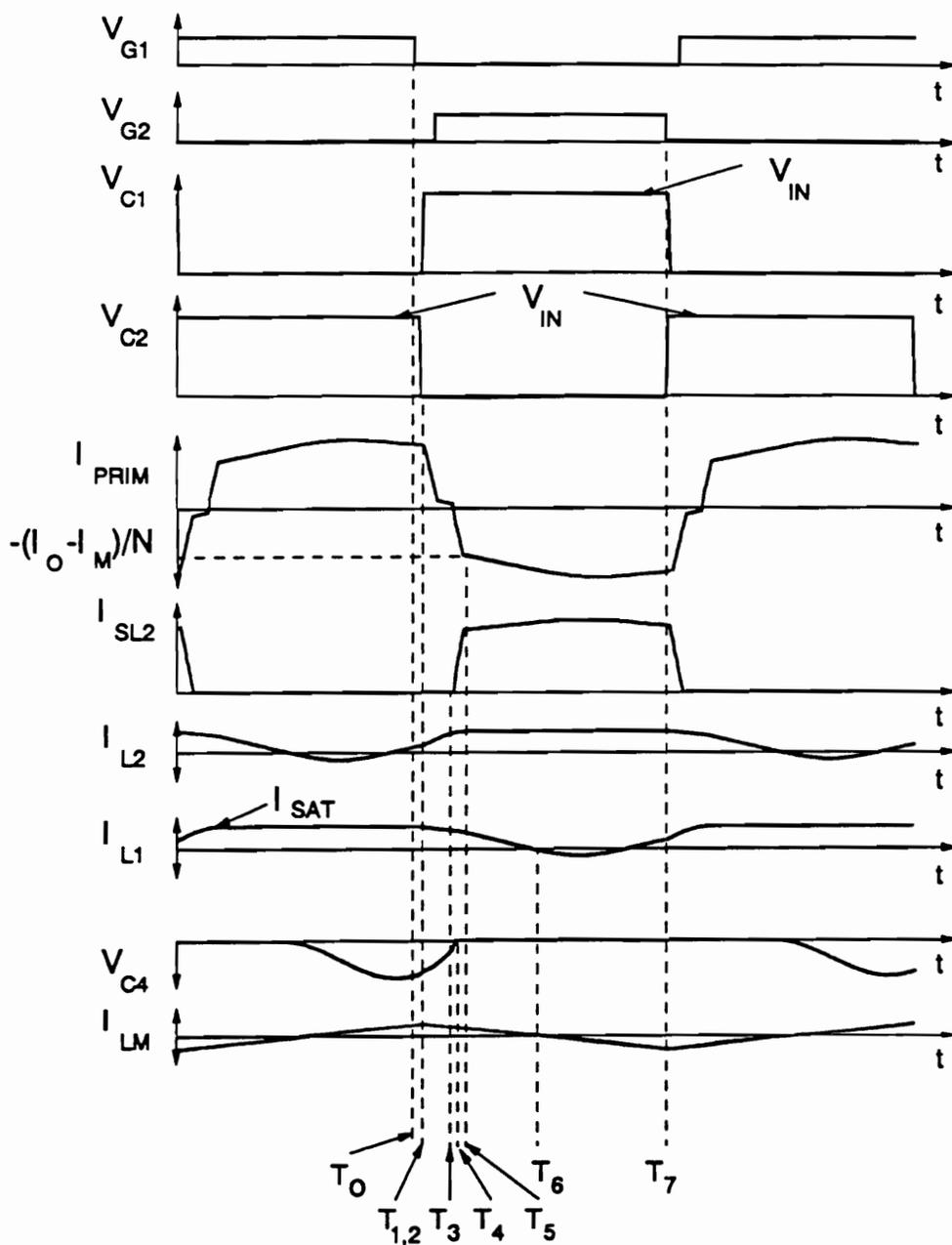
Figure 5.11. Ideal waveforms of the HB ZVS-MRC (L_M) operating in Mode III.B, from top to bottom:
gate-source voltage V_{G1}, gate-source voltage V_{G2}, switch Q_1 voltage V_{C1}, switch Q_2
voltage V_{C2}, primary current I_{PRIM}, saturable inductor current I_{SL2}, linear inductor
current I_{L2}, linear inductor current I_{L1}, and rectifier capacitor voltage V_{C4}.
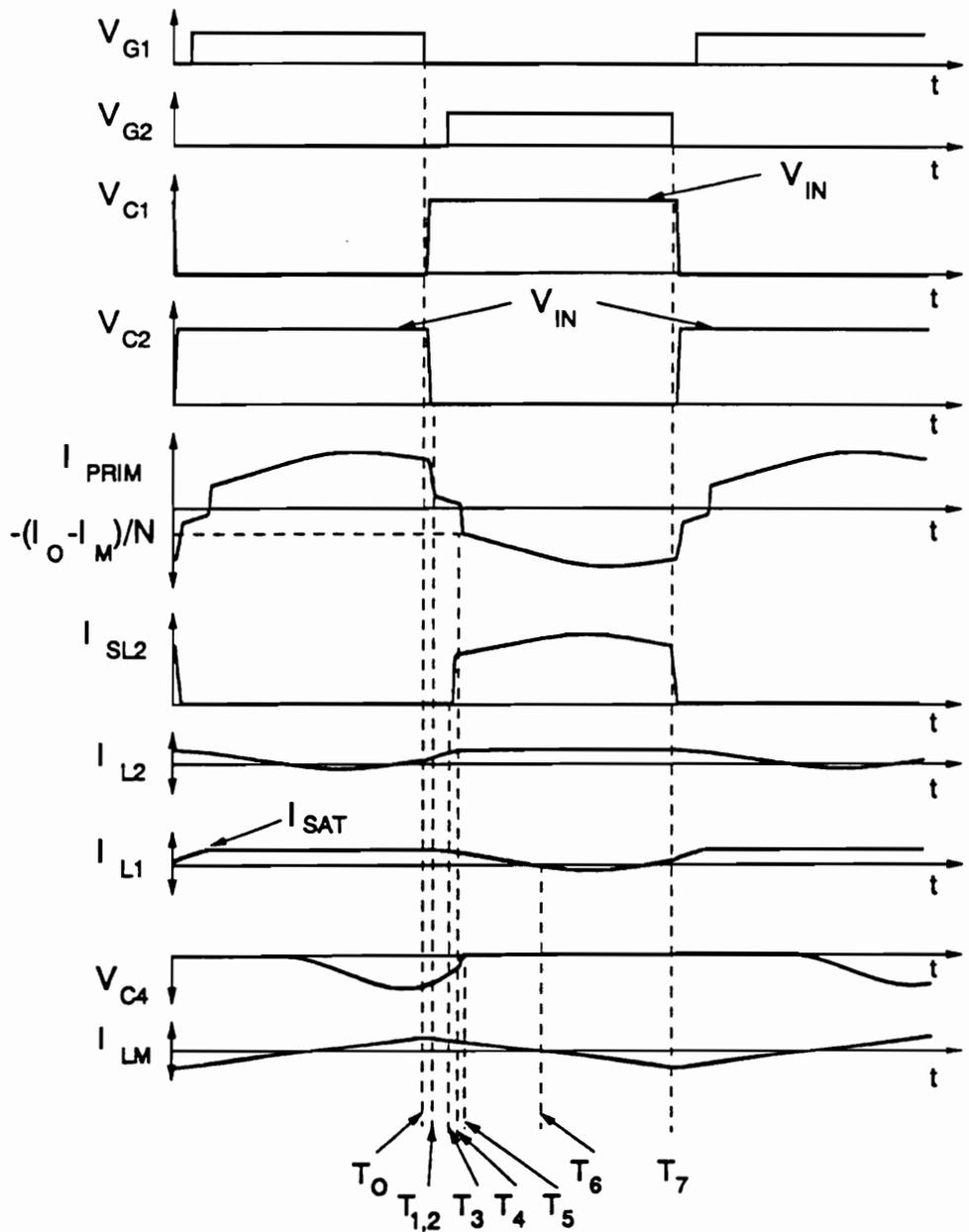
Figure 5.12. Ideal waveforms of the HB ZVS-MRC (L_M) operating in Mode III.C, from top to bottom: gate-source voltage V_{G1}, gate-source voltage V_{G2}, switch Q_1 voltage V_{C1}, switch Q_2 voltage V_{C2}, primary current I_{PRIM}, saturable inductor current I_{SL2}, linear inductor current I_{L2}, linear inductor current I_{L1}, and rectifier capacitor voltage V_{C4}.
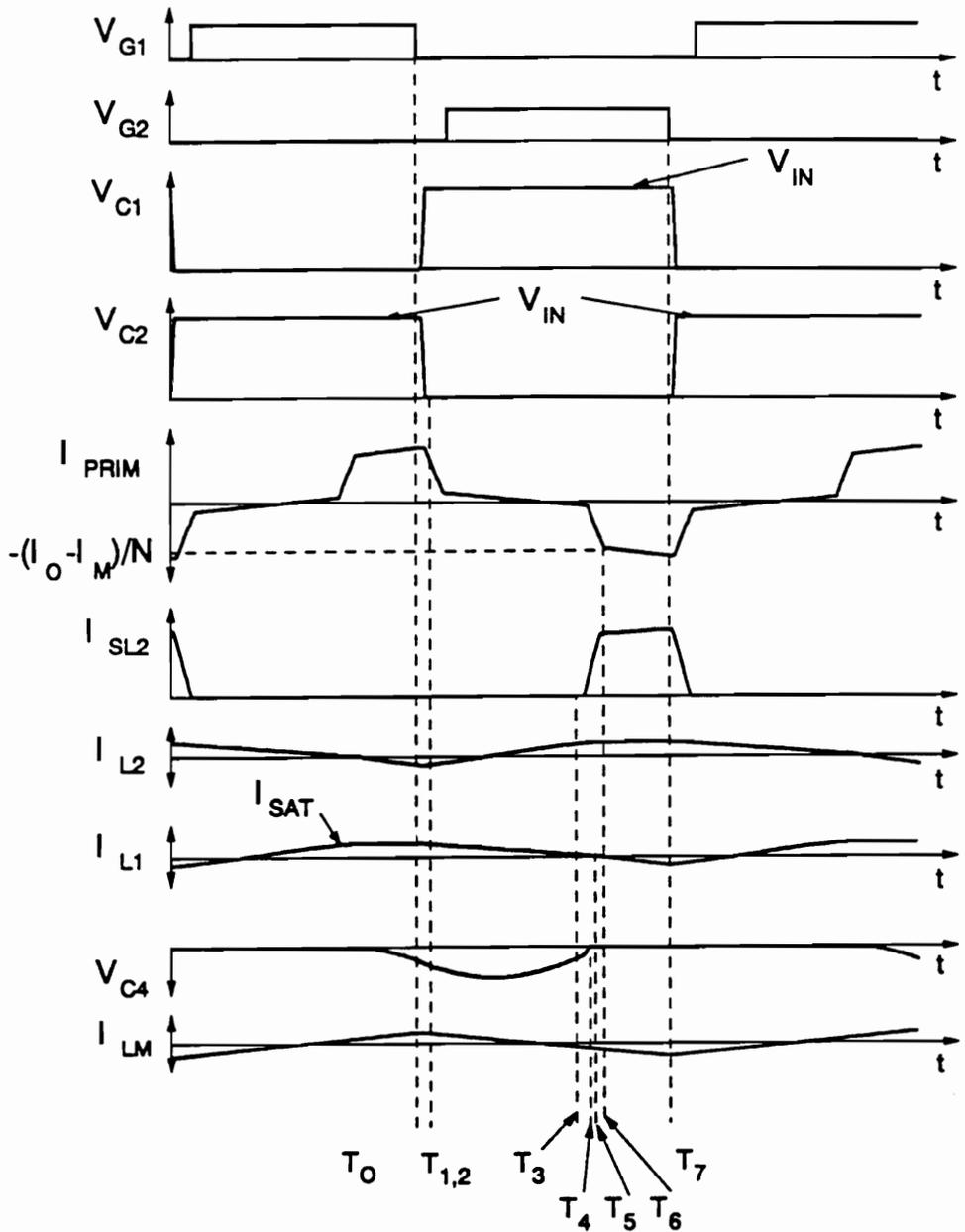
Figure 5.13. Ideal waveforms of the HB ZVS-MRC (L_M) operating in Mode III.D, from top to bottom: gate-source voltage V_{G1}, gate-source voltage V_{G2}, switch Q_1 voltage V_{C1}, switch Q_2 voltage V_{C2}, primary current I_{PRIM}, saturable inductor current I_{SL2}, linear inductor current I_{L2}, linear inductor current I_{L1}, and rectifier capacitor voltage V_{C4}.
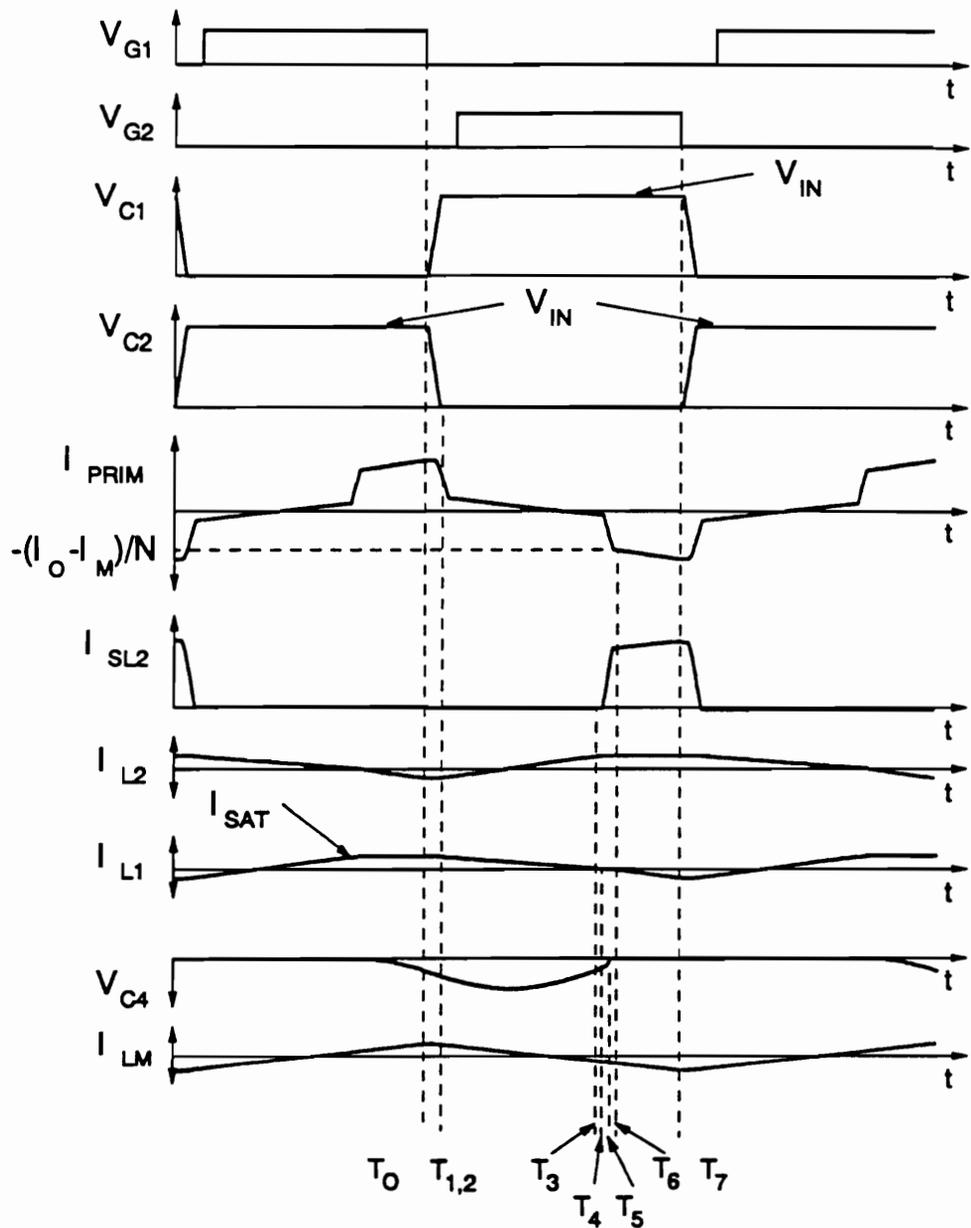
Figure 5.14. Ideal waveforms of the HB ZVS-MRC (L_M) operating in Mode III.E, from top to bottom: gate-source voltage V_{G1}, gate-source voltage V_{G2}, switch Q_1 voltage V_{C1}, switch Q_2 voltage V_{C2}, primary current I_{PRIM}, saturable inductor current I_{SL2}, linear inductor current I_{L2}, linear inductor current I_{L1}, and rectifier capacitor voltage V_{C4}.
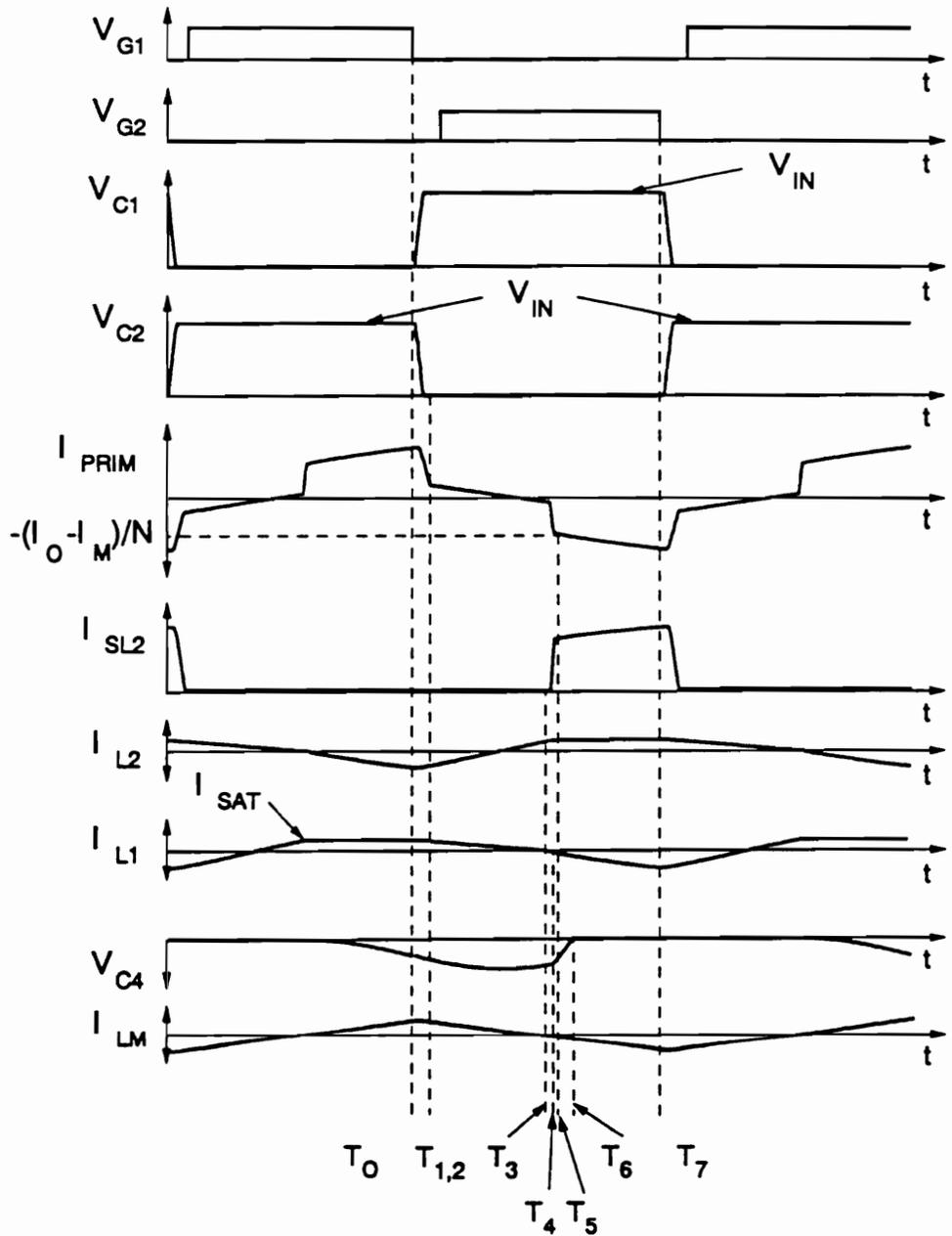
Figure 5.15. Ideal waveforms of the HB ZVS-MRC (L_M) operating in Mode III.F, from top to bottom: gate-source voltage V_{G1}, gate-source voltage V_{G2}, switch Q_1 voltage V_{C1}, switch Q_2 voltage V_{C2}, primary current I_{PRIM}, saturable inductor current I_{SL2}, linear inductor current I_{L2}, linear inductor current I_{L1}, and rectifier capacitor voltage V_{C4}.

Table 5.1. Modes of operation of the HB ZVS-MRC (L_M).

MODE	STAGE SEQUENCE
I.A	A - B - C - D - HP - H - F
I.B	A - B - C - D - HP - EP - F
I.C	A - B - C - D - E - EP - F
II.A	A - B - C - G - JP - EP - F
II.B	A - B - C - G - E - EP - F
II.C	A - B - C - G - JP - J - F
III.A	A - B - C - IP - I - H - F
III.B	A - B - C - IP - HP - H - F
III.C	A - B - C - IP - I - J - F
III.D	A - B - C - IP - HP - EP - F
III.E	A - B - C - IP - JP - EP - F
III.F	A - B - C - IP - JP - J - F
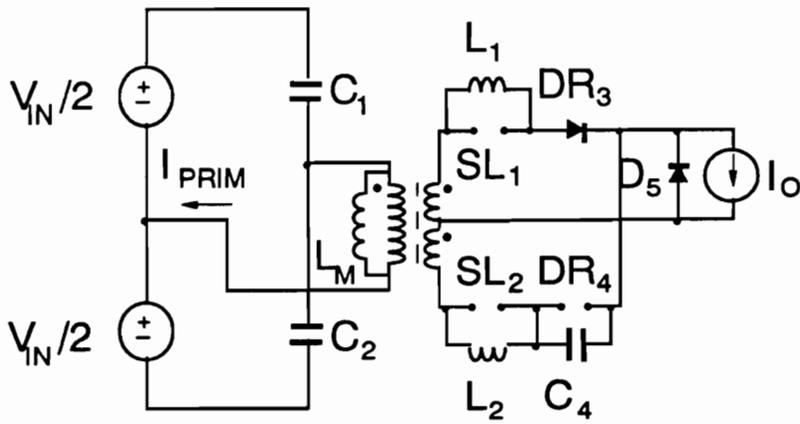
Figure 5.16.   Topological Stage BP.   Saturable inductors SL_1 and SL_2 are in the unsaturated state.

to unsaturate and the time it blocks all current (saturable inductors were modeled to have a finite inductance when saturated and infinite inductance when unsaturated). The corresponding saturable inductor, saturable inductor SL_1 for the half cycle described by the topological sequences in the preceding discussion, will not start resetting until the voltage across the transformer windings changes polarity. The transformer voltage will changes from positive to negative at the start of topological Stage B. Topological stages A and B model the switching transition of the primary switches and correspond to a small fraction of the total switching period. Therefore, for heavy loads, the delay time necessary for the saturable cores to come out of saturation is longer than the duration of the switching transition (time duration of topological stages A and B) as is modeled in the topological sequences describing modes I, II, and III. At lighter loads, the time it takes the saturable inductor to come out of saturation decreases and the current through this inductor will decrease to zero before the switching transition is over. Therefore, to model light load operation, an added topological stage is needed to represent the latter duration of Stage B when saturable inductor SL_1 is no longer saturated. This stage is shown in Fig. 5.16 as topological Stage BP. During light load operation, the switching transition is represented by the topological sequence of Stage A, Stage B, and Stage BP.

For even lighter load operation most of the load will no longer be supplied by the saturable inductors. In the extreme case, no load operation, the saturable inductors will never saturate and all of the load current will be supplied by the linear inductors L_1 and L_2. Light load to no load operation was not modelled since they are not necessary for the design of the converter. A detail analysis of this converter is given in Appendix C. The primary switches in this converter turn on under zero voltage due to the resonance of the primary-switch capacitance and the magnetizing inductance. Similarly, the rectifiers turn on softly (zero-voltage turn-on) due

to the controlled resonance of the rectifier capacitance and the linear inductors on the secondary side of the transformer. Since in normal operation the saturable inductors are not forced to sweep the complete B-H loop, the converter can operate at a relatively high frequency. A constant off-time, variable frequency control is required to regulate the output voltage. However, if controlled saturable inductors are used instead, constant frequency operation of the primary switches is possible by using post regulation. constant frequency operation will be discussed in the sections that follow.

As can be seen from Figs. 5.4 to 5.15, currents and voltages in the primary circuit are quasi-squarewave. The amplitude of the voltage waveform is clamped to V_{IN} as in the corresponding PWM converter. The amplitude of the primary current waveform shows a light resonance and is slightly higher than in PWM converters. These PWM-like waveshapes are very desirable since they result in lower conduction losses and stresses.

Single-ended topologies will do not have these desirable characteristics since the voltage across the primary switch will resonante to several times the input voltage. However, due to the precense of the saturable inductor, the current stressess will be much reduced compared to those in ZVS-MRCs.

5.3 DC Voltage-Conversion-Ratio

The dc voltage-conversion-ratio curves are obtained by solving the differential equations for each stage of the sequence representing the different modes of operation. The solution of the

differential equations for the different stages used to represent the operation of this converter are given in Appendix C. A set of dc voltage-conversion-ratio characteristics are shown in Figs. 5.17 and 5.18. The characteristics are plotted as a function of normalized conversion frequency, $f_{con} = f_S/2f_O$, for different normalized output currents, $I_{ON} = Z_N I_O/N V_{IN}$. The characteristics are plotted for different values of the design parameters: $C_N = 2C_D/(N^2 C)$, the ratio of the capacitance across the rectifiers reflected to the primary $(4C_D/N^2)$ and the resonant capacitance across the primary switches (2C); $L_N = 4L_M/(N^2 L)$, the ratio of the magnetizing inductance L_M and the resonant inductors across the rectifiers reflected to the primary $(N^2 L/4)$; $I_{SLN} = I_{SAT}/(I_O/N)$, the normalized current of the linear inductor during the interval the saturable inductor is saturated; and L/SL, the ratio between the secondary linear inductance and the inductance of the saturable reactor when saturated. The resonant frequency is defined as $\omega_O = 2\pi f_O = 1/\sqrt{2CL_M}$ and the characteristic impedance as $Z_N = \sqrt{L_M/2C}$. V_{IN} is the input voltage and N is the turns ratio of the transformer.

The selected value of L/SL only changes the spacing between the different curves of constant I_{ON} in the dc voltage-conversion-ratio curves. As the value of L/SL increases the distance between the curves decreases. The decreased frequency dependence resulting from line and load variations for $0.2 < M < 0.7$ is due to the presence of the saturable inductors.

Figure 5.18 also shows the regions of the dc voltage conversion curves corresponding to different modes of operation. In Mode III, the saturable inductor SL_2 saturates before capacitor C_4 completely discharges to zero, maximizing the duration of the power transferring stages. Mode III of operation results in the highest power stage dc gain. In Mode II, linear inductor L_1 decreases to zero before either SL_2 saturates or C_4 completely discharges resulting in the simultaneous resonance of capacitances C_4 and C_3. Mode II of operation results in lower dc gains than those found in Mode III of operation. In Mode I of operation, rectifier capacitance
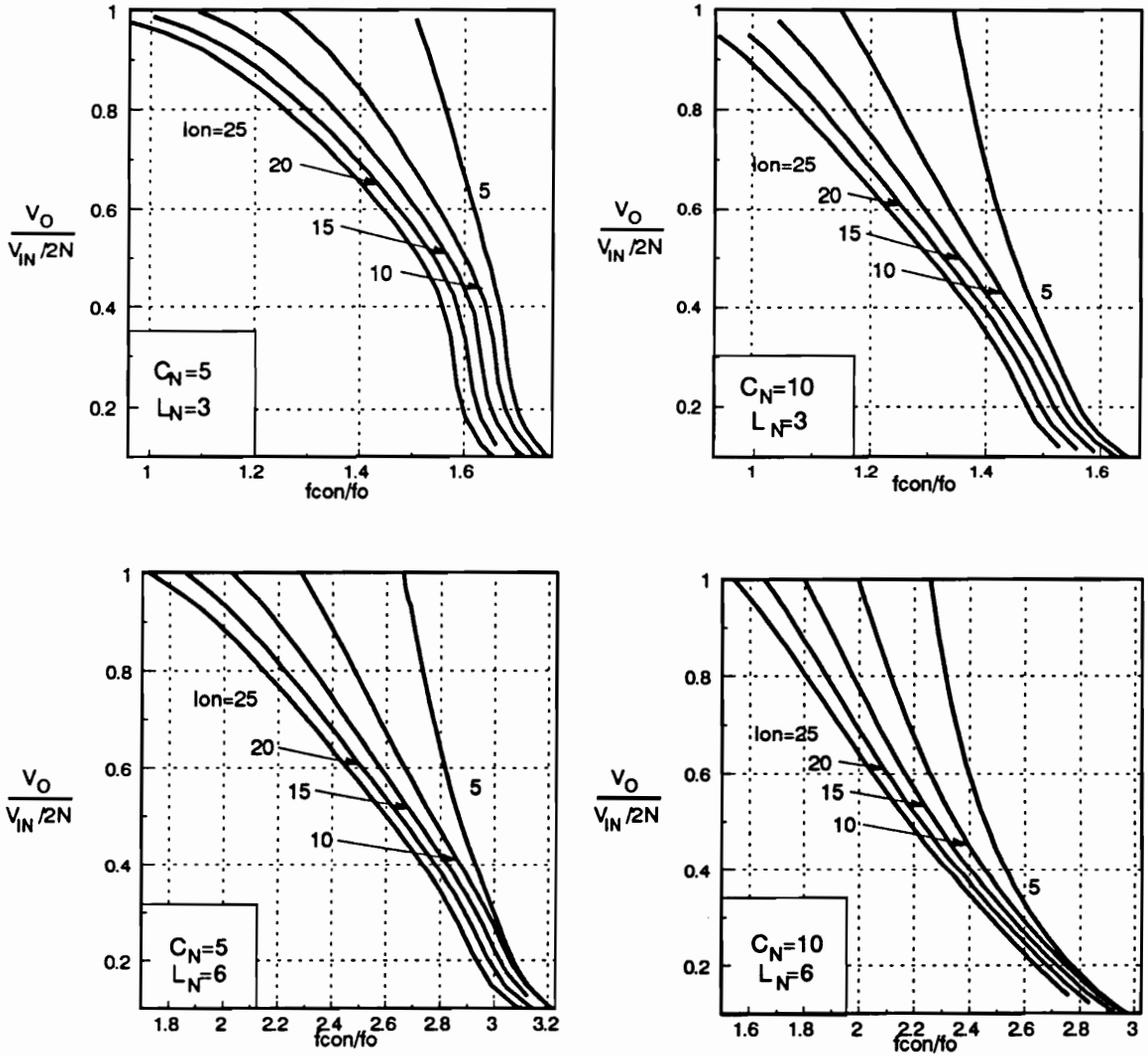
Figure 5.17. DC voltage-conversion-ratio characteristics as a function of the normalized switching frequency for different values of C_N and L_N. All characteristics are plotted for $I_{SLN}=1$ __and__ $L/SL=100$; $C_N = 2C_D/(CN^2)$, $L_N = 4L_M/(LN^2)$, $I_{SLN} = I_{SAT}/(I_O/N)$, $Z_O = \sqrt{L_M/2C}$, $I_O = 2I_OZ_O/(V_{IN}N)$, and $f_O = 1/2\pi\sqrt{2CL_M}$.
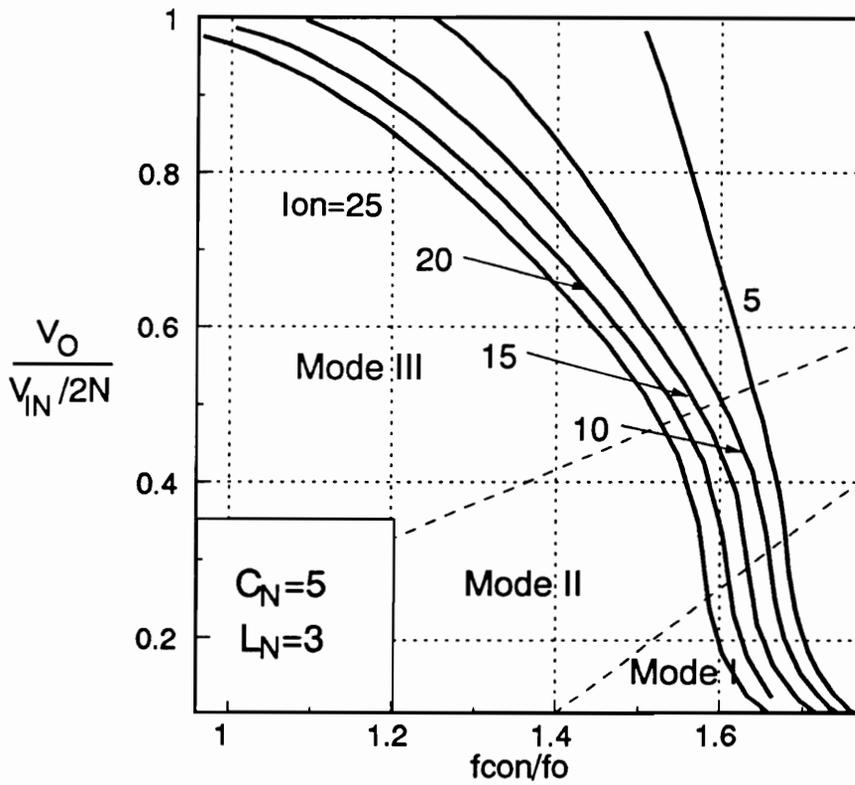
Figure 5.18. DC voltage-conversion-ratio characteristics showing the regions where the different modes of operation occur: $C_N = 5$, $L_N = 3$, $I_{SLN} = 100$, and $L/SL = 100$.

C_4 completely discharges to zero turning rectifier diode DR_4 on before saturable inductor SL_2 saturates or the current through linear inductor L_1 changes polarity. For light to no load operation, all or a high percentage of the load current flows thorough the linear inductors. This mode of operation is not shown since it is not necessary for design purposes.

A complete set of design characteristics, $C_N = 5$ and 10 and, $L_N = 1$, 3, and 6 are given in Appendix C.

5.4 Design Guidelines

5.4.1 Design Trade-off Study

To determine design guidelines for the HB ZVS-MRC (L_M), it is necessary to determine how rms currents and peak-to-peak voltages for the magnetic components and the rectifier diodes vary as a function of the design parameters. Since this converter can be designed for different C_N, L_N, I_{SLN}, L/SL, Z_O, and transformer turns ratio N, a design trade-off study needs to be considered. No analytical expression for the current and voltage stresses on the different components exist for the HB ZVS-MRC (L_M). Therefore, current and voltage stresses are determined from the numerical solution of the operation of the converter used to determine the dc voltage-conversion curves.

To evaluate the effect of the different design parameters on the performance of this converter, different design examples are considered. Comparing current and voltage stresses for the different design examples provides design guidelines. The design of the HB ZVS-MRC (L_M) is based on the dc voltage-conversion-ratio characteristics curves and the following design specifications:

- input voltage range, V_{IN}^{max} - V_{IN}^{min};
- output voltage, V_O;
- load range, I_O^{max} - I_O^{min}; and
- minimum switching frequency, f_S^{min}.

The first step in designing the converter is to determine the transformer turns ratio N, C_N, L_N, and Z_O using a set of dc voltage-conversion-ratio curves.

For a design that maximizes efficiency, peak resonant currents and the circulating energy flowing through the converter must be minimized. Circulating energy is directly dependent on the values of C_N and L_N. In addition, C_N and L_N determine the frequency range of the converter for the given input voltage, output voltage, and load current specifications. I_{SLN} determines the blocking time of the saturable inductors. A smaller I_{SLN} corresponds to a shorter blocking time. For variable-frequency control, it is desirable to minimize the blocking time by making it slightly greater than the duration of the switching transition. By allowing the saturable inductors to saturate as fast a possible, i.e., minimum I_{SLN}, the duration of the stages during which power is transferred to the load is maximized for a given C_N, L_N, and Z_O; i.e., minimizes the loss in duty cycle as seen by the rectifier circuit. Similarly, maximizing the ratio L/SL decreases the load dependence by decreasing the time it takes the saturable inductors to come out of saturation (as for a ideal operation).

The effect of the design parameters (N, C_N, L_N, Z_O, I_{SLN}, and L/SL) are interrelated, thus complicating the design of the HB ZVS-MRC (L_M). From the above discussion, the effects of I_{SLN} and L/SL are well understood. I_{SLN} should be minimized and L/SL should be maximized for a given inductor design. This minimizes conduction losses in the primary side (higher transformer turns ratio) and the frequency range (lower load dependence). The effects due to the remaining design parameters on the design of the HB ZVS-MRC (L_M) are not obvious. To evaluate the effect of the transformer turns ratio N, C_N, L_N, and Z_O, the soft switched HB is designed using different combinations of these parameters and a current and voltage stress analysis is performed to determine design trade-offs and guidelines.

Design trade-offs of this converter are based on the following design specifications:

- input voltage range, V_{IN}^{max} - V_{IN}^{min} = 40 - 60 V;

- output voltage, V_O = 5 V;

- load range, I_O^{max} - I_O^{min} = 5 - 20 A; and

- minimum switching frequency, f_S^{min}. = 250 kHz.

Figures 5.18 - 5.21 show the dc characteristics of the HB ZVS-MRC (L_M) for C_N = 5 and 10, and L_N = 3 and 6. All characteristics are plotted for L/SL = 100 and $I_{SLN} = I_{SAT}/(I_O/N)$ = 1. I_{SLN} = 1 corresponds to a maximum current through the linear inductors of 10 - 15 % of the total load current if the converter is designed for an I_{ON} >15. Six different design examples are considered in the design trade-off study:

Design #1: N = 3, I_{ON}^{max} = 25, C_N = 5, and L_N = 6;
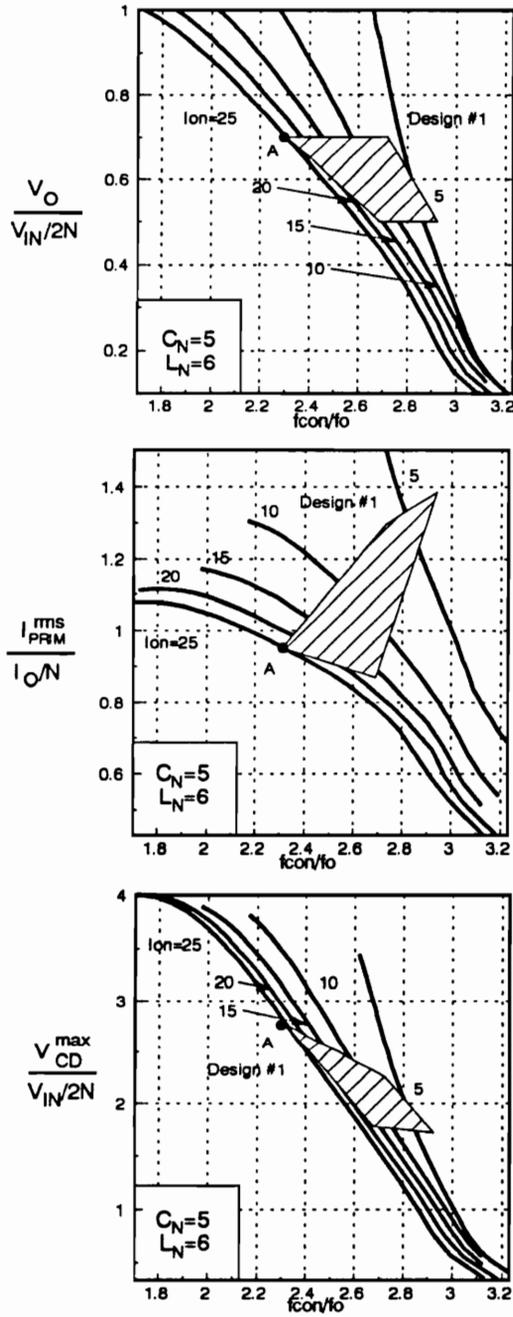
Figure 5.19. Design example #1 for the HB ZVS-MRC L_M; $C_N = 5$, $L_N = 6$, $I_{SLN} = 1$, and L/SL = 100 showing: dc voltage conversion ratio ($V_O/(V_{IN}/2N)$), normalized primary rms current ($I_{PRIM}^{rms}/(I_O/N)$), and maximum normalized rectifier diode voltage stress ($V_{CD}^{max}/(V_{IN}/2N)$).
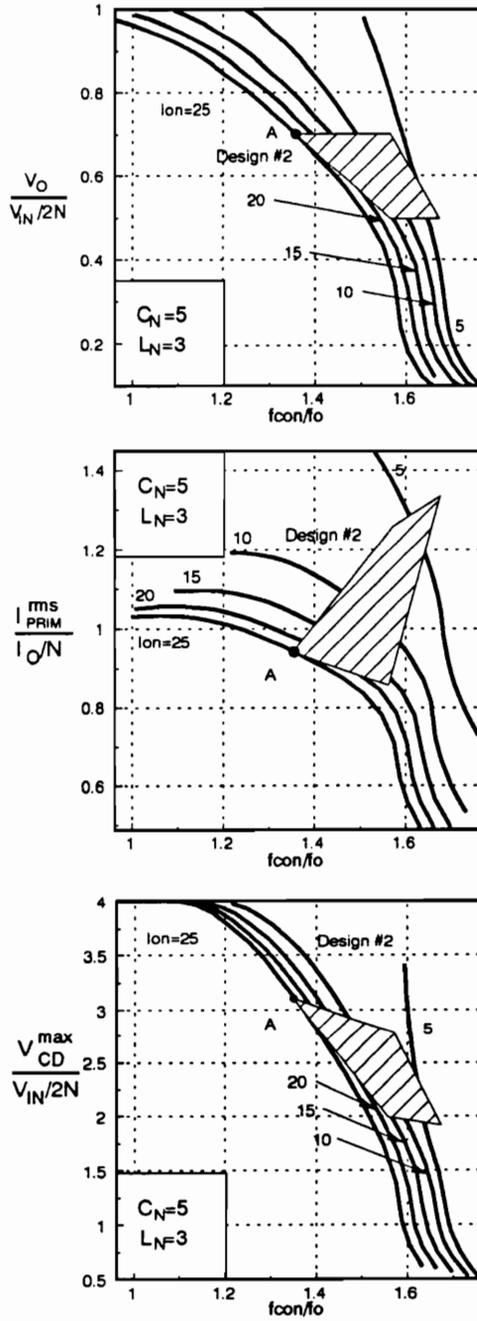
Figure 5.20. Design example #2 for the HB ZVS-MRC L_M; $C_N = 5$, $L_N = 3$, $I_{SLN} = 1$, and $L/SL = 100$ showing: dc voltage conversion ratio $(V_O/(V_{IN}/2N))$, normalized primary rms current $(I_{PRIM}^{rms}/(I_O/N))$, and maximum normalized rectifier diode voltage stress $(V_{CD}^{max}/(V_{IN}/2N))$.
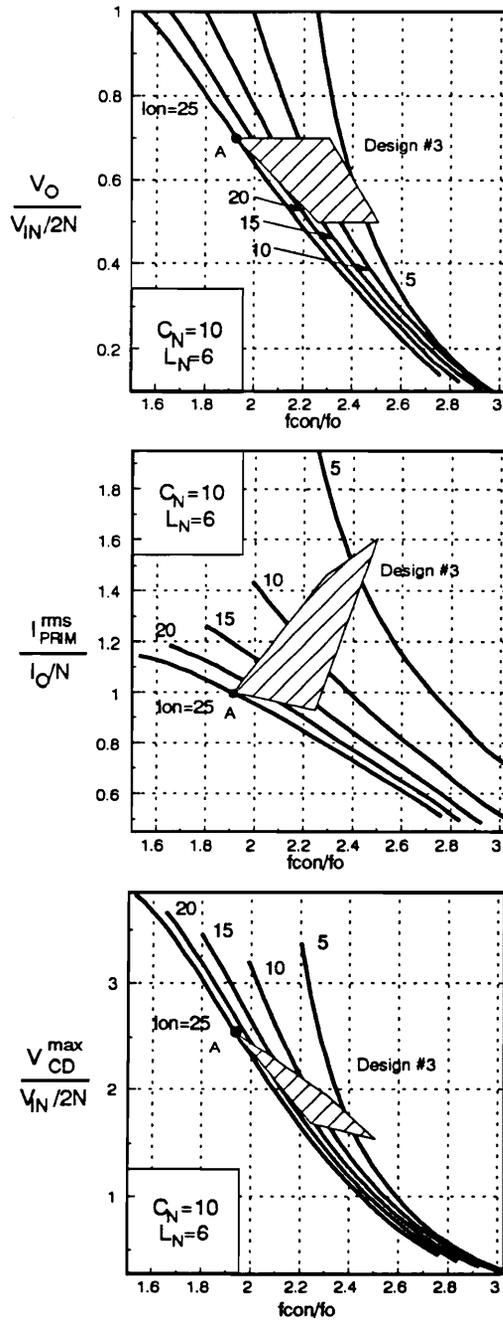
Figure 5.21. Design example #3 for the HB ZVS-MRC L_M; $C_N = 10$, $L_N = 6$, $I_{SLN} = 1$, and L/SL = 100 showing: dc voltage conversion ratio ($V_O/(V_{IN}/2N)$), normalized primary rms current ($I_{PRIM}^{rms}/(I_O/N)$), and maximum normalized rectifier diode voltage stress ($V_{CD}^{max}/(V_{IN}/2N)$).
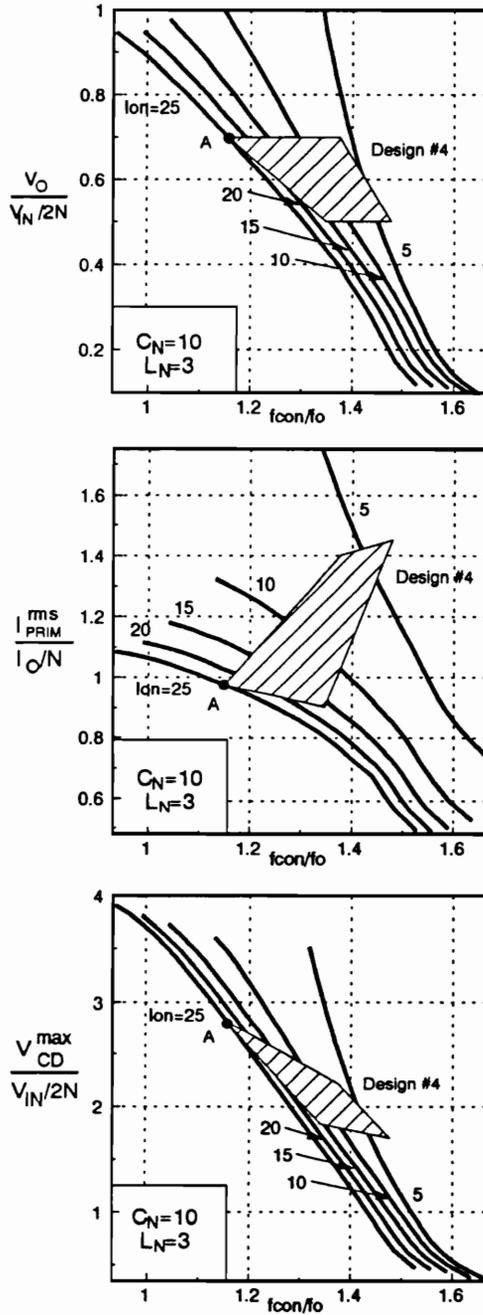
Figure 5.22. Design example #4 for the HB ZVS-MRC L_M; $C_N = 10$, $L_N = 3$, $I_{SLN} = 1$, and L/SL = 100 showing: dc voltage conversion ratio ($V_O/(V_{IN}/2N)$), normalized primary rms current ($I_{PRIM}^{rms}/(I_O/N)$), and maximum normalized rectifier diode voltage stress ($V_{CD}^{max}/(V_{IN}/2N)$).

Design #2: $N = 3$, $I_{ON}^{max} = 25$, $C_N = 5$, and $L_N = 3$;

Design #3: $N = 3$, $I_{ON}^{max} = 25$, $C_N = 10$, and $L_N = 6$;

Design #4: $N = 3$, $I_{ON}^{max} = 25$, $C_N = 10$, and $L_N = 3$;

Design #5: $N = 4$, $I_{ON}^{max} = 25$, $C_N = 5$, and $L_N = 6$; and

Design #6: $N = 3$, $I_{ON}^{max} = 20$, $C_N = 5$, and $L_N = 6$.

Figures 5.19 - 5.22 show the operating regions and device stresses for the first four designs which study the effect of selecting different values of C_N and L_N while the remaining design parameters are kept constant. Defining the region of operation follows similar guidelines as the ones shown for the CF ZVS-MRCs. This characteristics show the dc voltage-conversion-ratio curves, the normalized rms primary current, and the maximum voltage stress across the rectifier diodes normalized with respect to the input voltage. Voltage stress characteristics are not needed for the remaining components since the HB operation results in clamping of the primary switch voltage stresses to the value of the input voltage. Furthermore, since the magnetizing inductance of the the transformer is the resonant inductor, the primary transformer voltage consists of a square waveform with a maximum of $V_{IN}/2$ and a minimum of $- V_{IN}/2$. Figure 5.19 shows the operating region corresponding for Design #1. As for most variable frequency ZVS topologies, the minimum switching frequency is determined by the full-load and low-line conditions (point A in Fig. 5.19). Full-load and high-line operation is shown as point B in Fig. 5.19 and points C and D represent high-line and light-load and low-line and light-load conditions, respectively.

Since the characteristics are normalized, it is difficult to predict the regions that would result in minimum primary rms current (minimum conduction losses) and the regions of minimum rectifier diode voltage stress, V_{CD}^{max}. To understand the effect of C_N and L_N, Table 5.2 summa-

rizes the calculated rms primary currents and maximum rectifier diode voltage stress for high-line and low-line, and full-load operation for the first four designs. From the results in Table 5.2, the following design trade-off is inferred: comparing Design #1 with Designs #2 and #3 suggests that increasing the ratio L_N or C_N increases the value of the rms primary current but decreases the maximum voltage stress seen by the rectifier diodes.

In order to study the effect of selecting different transformer turns ratios N (selecting M_{max}) and different power stage characteristic impedances Z_O (selecting I_{ON}), two more design examples were considered. Figure 5.23 shows the operating region and stress analysis corresponding to these two designs. The resulting currents and voltages stresses of these designs are summarized in Table 5.3 and suggest the following conclusions:

1) Designing for a higher transformer turns ratio (selecting a higher M_{max}) decreases the primary rms current without increasing the maximum rectifier voltage stress considerably (2 V maximum difference).

2) Designing for a lower power stage characteristic impedance Z_O results in increased primary rms current and increased maximum rectifier voltage stress.

Table 5.2. Summary of design examples #1, #2, #3, and #4 of the HB ZVS-MRC (L_M).

		Design #1	Desing #2	Design #3	Design #4
V_{CD}^{max}	HL	17.5	20	16.5	17.5
(V)	LL	18.33	21.33	17.2	18.66
I_{PRIM}^{rms}	HL	5.9	5.77	6.17	6.13
(A)	LL	6.35	6.33	6.53	6.46

HL - High-Line (60 V)
LL - Low-Line (40 V)

Table 5.3. Summary of design examples #5 and #6 of the HB ZVS-MRC (L_M).

		Design #5	Desing #6
V_{CD}^{max}	HL	18.7	18.5
(V)	LL	20	18.66
I_{PRIM}^{rms}	HL	4.87	6.133
(A)	LL	5.4	6.533

HL - High-Line (60 V)
LL - Low-Line (40 V)
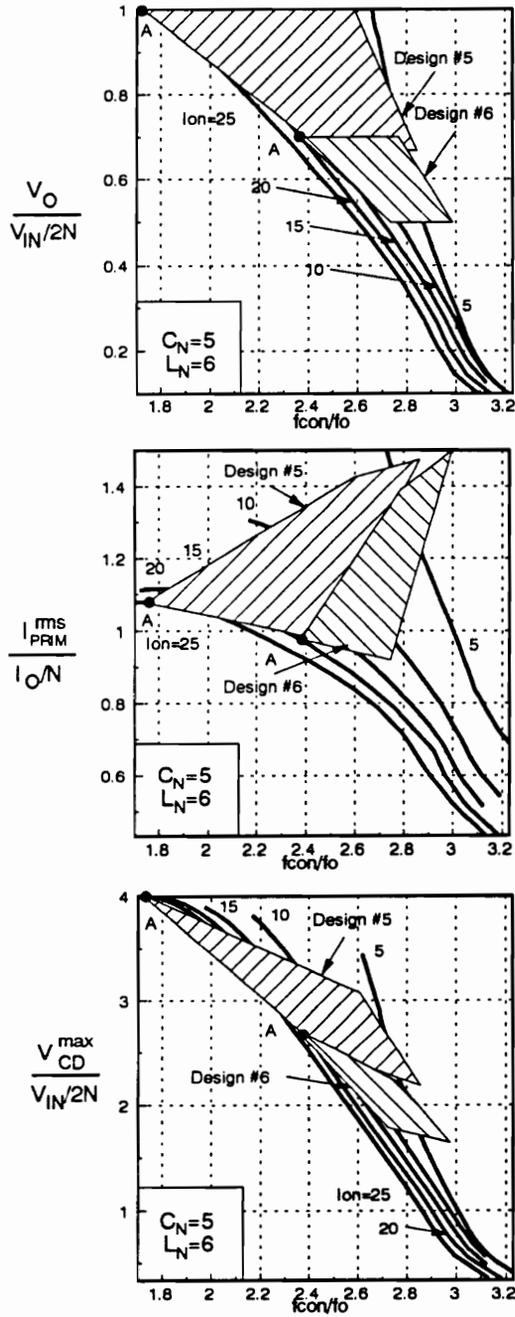
Figure 5.23. Design examples #5 and #6 for the HB ZVS-MRC L_M; $C_N = 5$, $L_N = 6$, $I_{SLN} = 1$, and $L/SL = 100$ showing: dc voltage conversion ratio $(V_O/(V_{IN}/2N))$, normalized primary rms current $(I_{PRIM}^{rms}/(I_O/N))$, and maximum normalized rectifier diode voltage stress $(V_{CD}^{max}/(V_{IN}/2N))$.

5.4.2 Design Procedure for the HB ZVS-MRC (L_M)

From the design trade-off study, the following rules should be used in designing the HB ZVS-MRC (L_M) if conduction losses need to be minimized:

1) The value of the capacitance ratio C_N and inductor ratio L_N should be minimized.

2) The characteristic impedance of the converter should be maximized (design so that full-load and low-line condition falls in the maximum I_{ON} curve).

3) The turns ratio of the transformer should be maximized (design for the maximum M_{max} possible).

Once C_N, L_N, M_{max}, and I_{ON}^{max} have been selected, the turns ratio is calculated from the following expressions:

$$N = \frac{V_{IN}^{min} 2M_{max}}{V_O} \tag{5.1}$$

The values of C_1 and C_2 represent the output capacitances of the switches. Once the switches are selected based on their current and voltage ratings and on-resistance as is done in corresponding PWM converters, the value for $C = C_1 = C_2$ is known. To minimize the ripple of the primary current, i.e., minimize the stresses and losses in the switches and primary winding, it is desirable to maximize L_M. L_M determines the resonant frequency along with capacitance

C. Therefore, the design frequency range and the selected capacitance C impose the upper limit on L_M for a given C_N, L_N, L/SL, and I_{SLN}. Once L_M is determined, the remaining resonant components can be determined from the following expressions:

$$C = \frac{1}{2} N^2 C_N c \qquad (5.2)$$

and

$$L = \frac{4L_M}{N^2 L_N} \qquad (5.3)$$

The presence of the leakage inductance of the power transformer does not affect the operation of the converter since it is in series with the relatively large linear inductors on the secondary side. The reset of the saturable inductors with variable frequency control is done by the resonance between linear inductor L and capacitance C_D which determines the volt-second product across saturable inductor. The primary switches Q_1 and Q_2 operate with variable frequency constant off-time control like conventional ZVS-MRCs.

5.5 Experimental Results for Variable Frequency Operation

A 100 W HB ZVS converter was designed for an input voltage range of 40 V to 60 V, an output voltage of 5 V, and a load-current range of 0 A to 20 A. The experimental power stage components are:

Q_1, Q_2 -IRF540 (International Rectifiers);

C_1, C_2 -output capacitance of IRF540,

        559 pF [8];

TR   -core: TDK EPC-19-Z (material H_{7C4});

        primary: 5 X 3 turns of 150/42 Litz

        wire;

        secondary: 2 turn of 5 mil. copper

        foil;

        primary leakage inductance: 60 nH;

        magnetizing inductance: 25 μH;

DR_3, DR_4 -60CNQ045 (International Rectifier);

C_3, C_4 -2 x 0.5 nF ceramic cap.;

L_F -inductance: 1 μH;

        core: TDK RM6Z12 (material H_{7C4});

        winding: 4 turns magnet wire

        AGW# 16;

        gap: 5 mm.;

C_F -5 x 3.3 μF NPO ceramic chip cap.;

where TR stand for the power transformer. The combination of linear and saturable inductors (L_1/SL_1 and L_2/SL_2) is implemented on a single core by winding four turns of Litz wire 150/44 on an amorphous Toshiba core (MB10 X 7 X 4.5). The reset of the saturable inductor is determined by the operation of the converter and depends on the value of the resonant components and load and line conditions. As long as the residual flux of the core is comparable to B_{SAT} (material with high squareness factor), the flux swing in the core will be limited to the top portion of the first and second quadrant of the B-H loop as shown in Fig. 5.24

Figure 5.25 shows the measured efficiency of the converter as a function of the load current for different input voltages. The converter has a maximum efficiency of 86.3 % at low line and full load. The efficiency decreases to 83.1 % at high line and full load. The switching frequency range is between 250 kHz to 1 MHz. Figure 5.26 shows typical oscillograms of key waveforms of the HB converter for full load (20 A) and no load (0 A) operation. The measured efficiency of a conventional HB ZVS-MRC designed for the same specifications is shown in Fig. 5.27. The HB ZVS-MRC has a maximum efficiency of 85 % at low line and full load operation and the efficiency of the converter decreases to 80.2 % at high line and full load operation. The experimental HB ZVS-MRC operated with a minimum switching frequency of 250 kHz and a maximum switching frequency of 1.6 MHz. Comparing the efficiencies shown in Figures 5.26 and 5.27 suggests that the performance of the HB ZVS-MRC (L_M) is less sensitive to variations in line and load conditions. The decreased sensitivity is due to decreased circulating energy flowing between the primary and secondary circuits. Figure 5.28 shows a photograph of the HB ZVS-MRC (L_M) and HB ZVS-MRC power stages. The reduced circulating energy in the HB ZVS-MRC (L_M) results in a size reduction of the power transformer. The TDK EPC-27-Z core (H_{7C4} material) is used for the transformer in the HB ZVS-MRC shown in Fig. 5.28(b). A com-
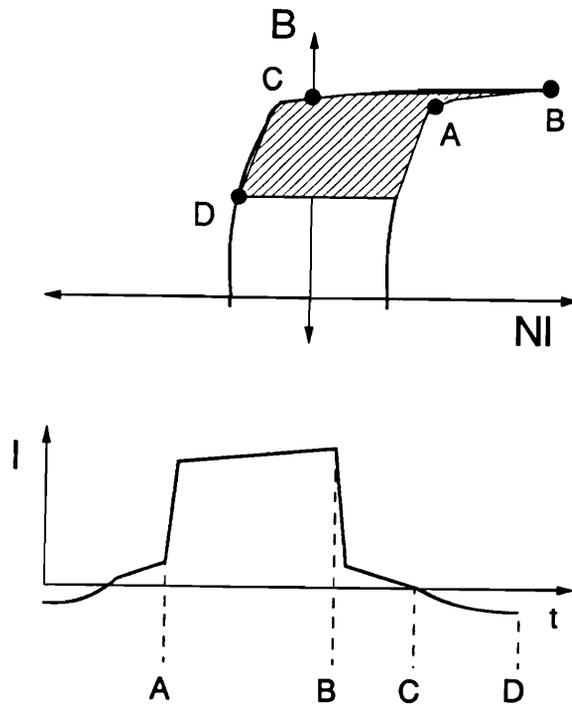
Figure 5.24. Flux swing experienced by the saturable inductors in the variable frequency HB ZVS-MRC (L_M).
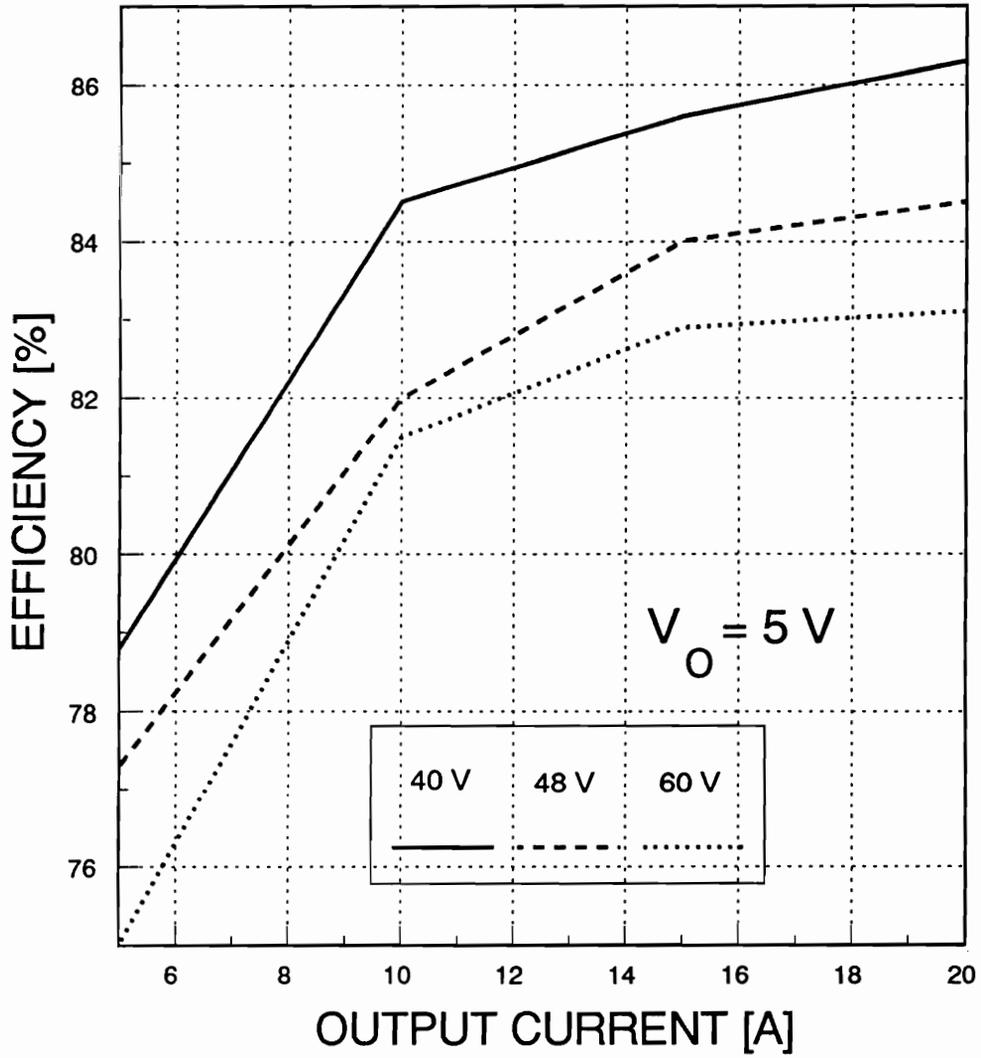
Figure 5.25. HB ZVS-MRC (L_M) efficiency as a function of load current for different input voltages of the converter operating with variable frequency.
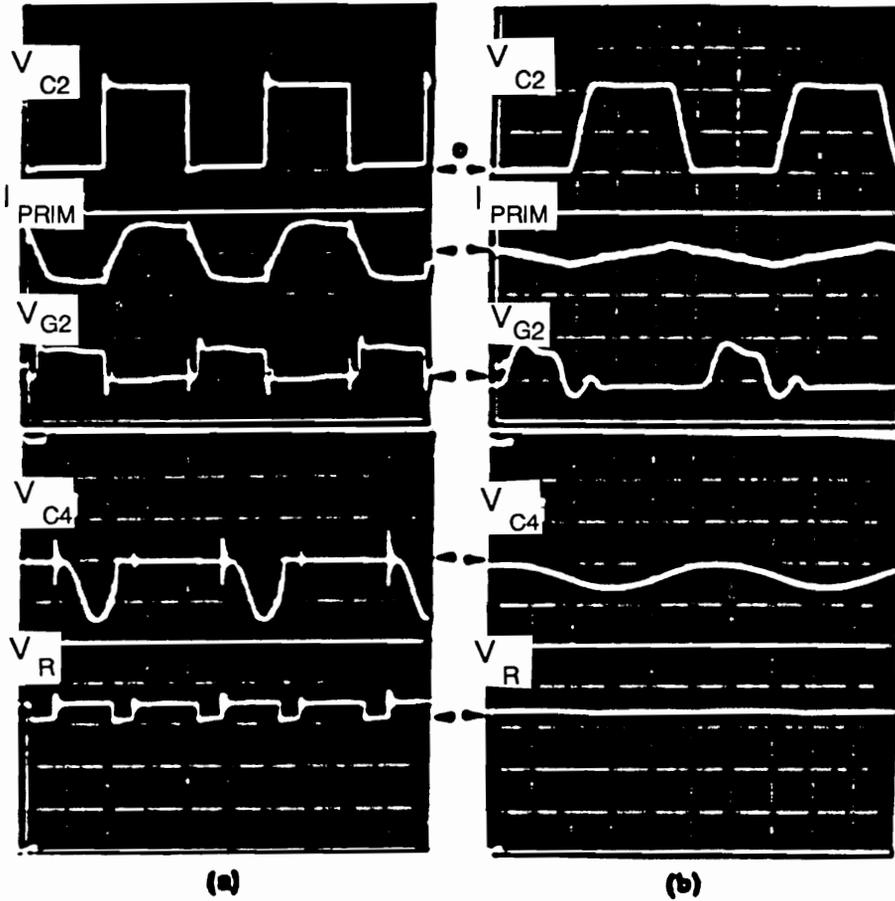
Figure 5.26. Oscillograms of the experimental variable frequency HB ZVS-MRC (L_M):
(a) full load (20 A) and low line (40 V), $f_S = 250$ kHz;
(b) no load (0 A) and low line (40 V), $f_S = 1$ MHz.
Shown from top to bottom: drain-to-source of Q_2 (V_{C2}, 20 V/div.); primary current, 10 A/div. for (a) and 1 A/div. for (b); gate-to-source of Q_2 (V_{G2}, 20 V/div.); voltage across C_4, 20 V/div.; rectified voltage, 20 V/div..
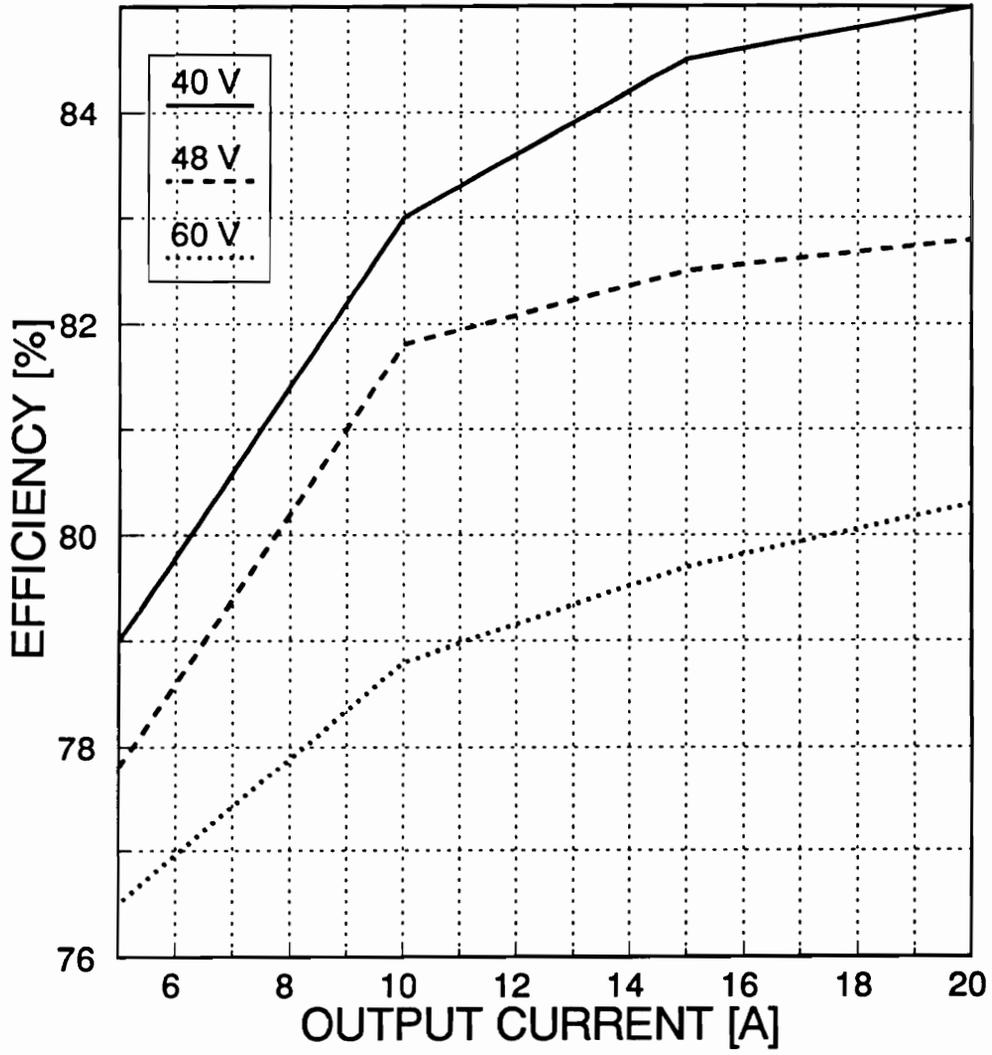
Figure 5.27. HB ZVS-MRC efficiency as a function of load current for different input voltages.
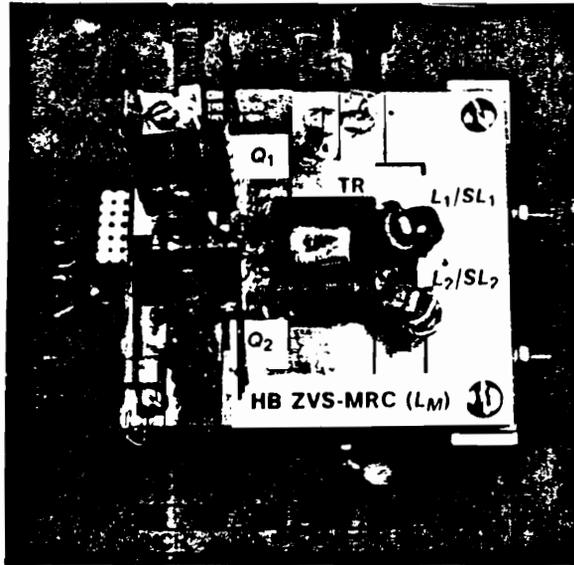
(a)
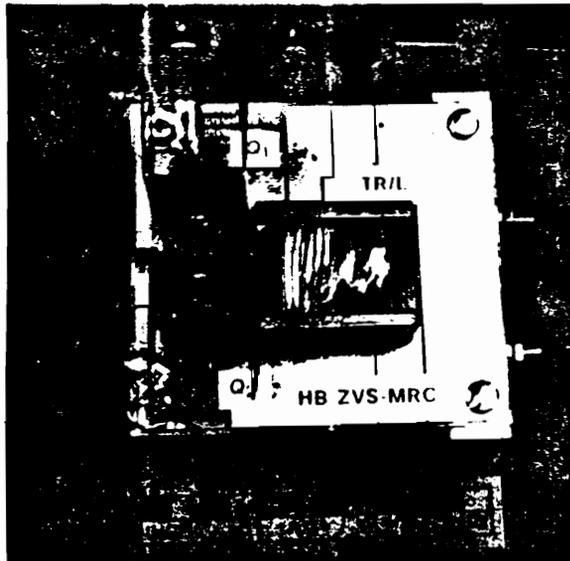
(b)

Figure 5.28. (a) HB ZVS-MRC (L_M) power stage; (b) HB ZVS-MRC power stage.

parison of the difference in the transformer size resulting from these two power processing techniques is shown in Fig. 5.29.

5.6 Constant Frequency Implementation

As discussed previously, the proposed family converters can operate at a constant switching frequency if controllable saturable inductors are used. Figure 5.30 shows the implementation of the controllable saturable inductor using an E core [G5,G6]. For ferrite core materials, the blocking time, given a set of windings, is controlled by biasing the core further or closer to saturation with a dc control current. The current through the control winding sets up a dc bias in the core. Depending on the value of the dc bias, the blocking time of the saturable inductor varies. Increasing the control current increases the dc bias on leg l_3 (leg that saturates) of the controlled saturable inductor as shown in Fig. 5.30. As the dc bias in leg l_3 increases, the blocking time of the saturable inductor decreases, resulting in increased output voltage. Similarly, if the value of the control current deceases, the blocking time of the saturable inductor increases, resulting in a lower output voltage. The maximum blocking time occurs for a zero control current corresponding to no dc bias.

The maximum blocking time of the saturable inductor occurs at high line and no load conditions. The minimum blocking time corresponds to operation at low line and full load. This means that the saturable inductor has to be designed so that it is able to block the secondary
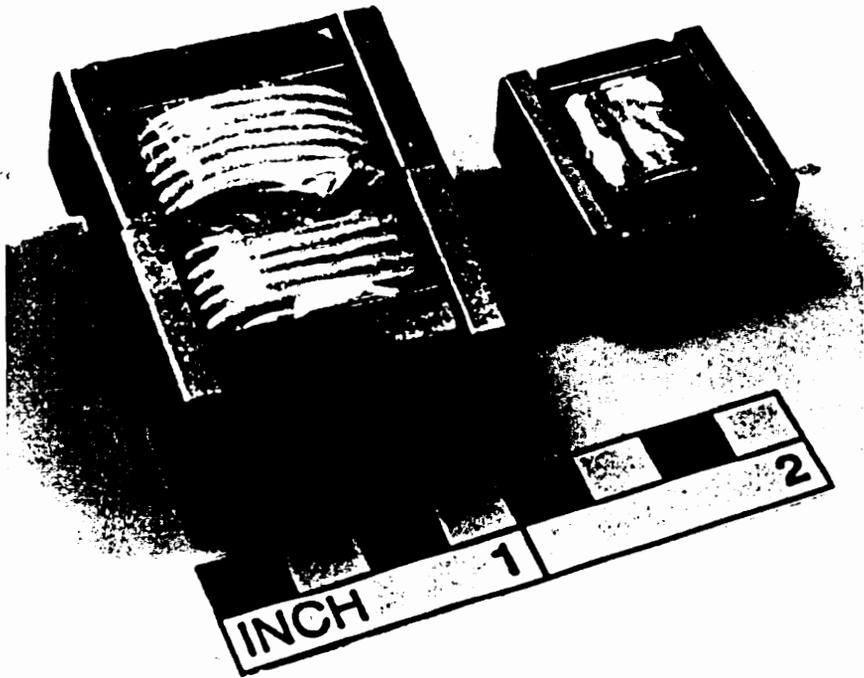
Figure 5.29.   Power stage power transformer from left to right: HB ZVS-MRC and HB ZVS-MRC
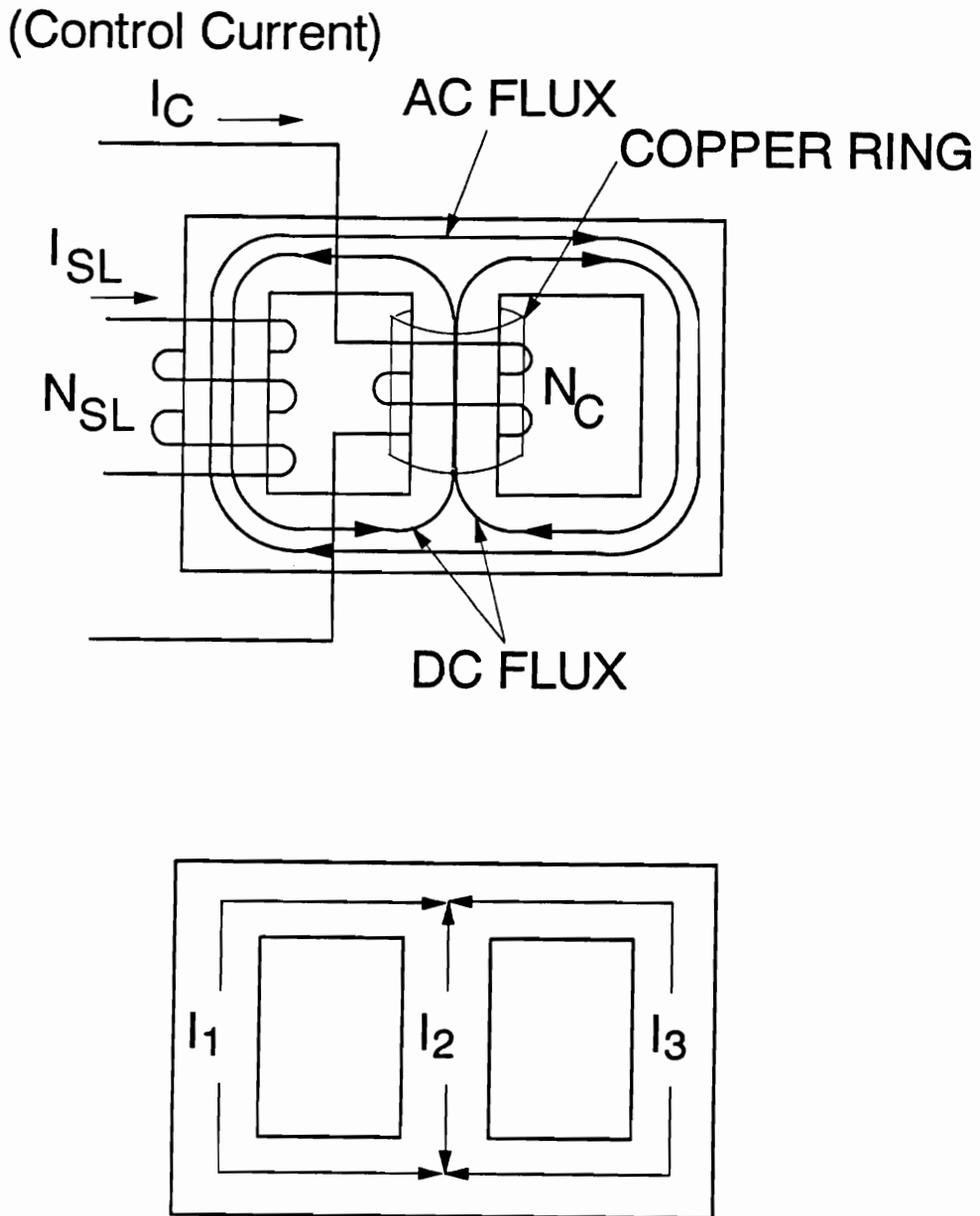
Figure 5.30. Implementation of a controllable saturable inductor using a EI ferrite core. N_C is the control winding and N_{SL} is the power winding were most of the load current flows when the inductor saturates.
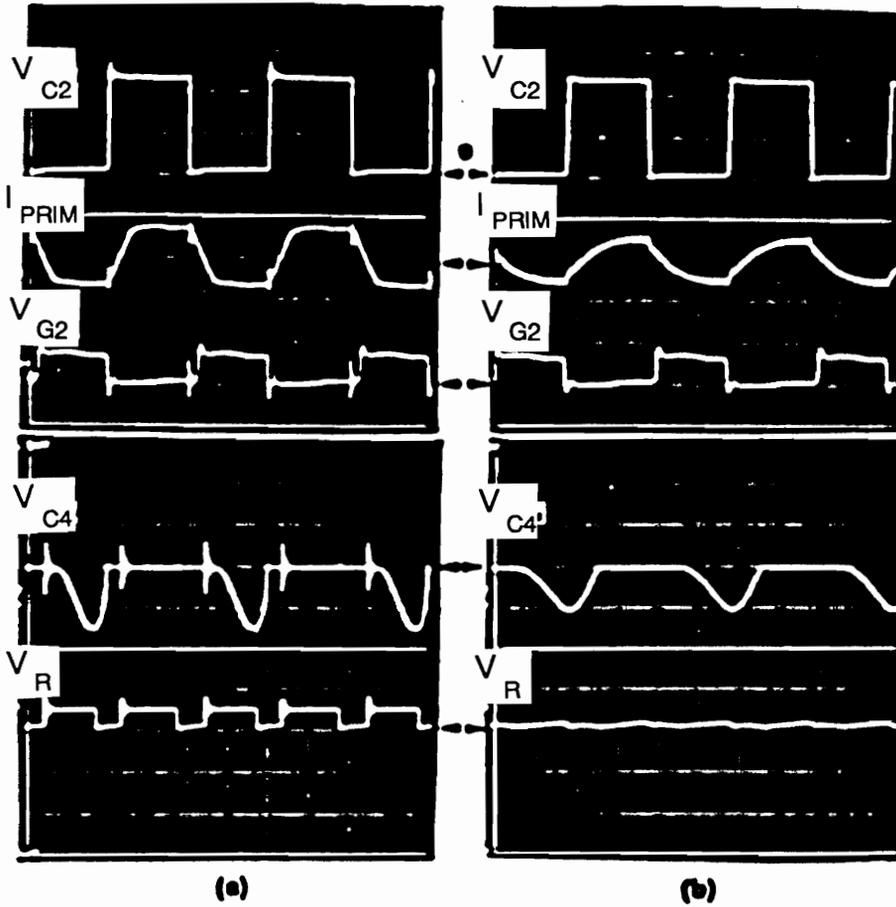
Figure 5.31. Oscillograms of the experimental constant frequency HB ZVS converter:
(a) full load (20 A) and low line (40 V), $I_{DC} = 330$ mA;
(b) no load (0.6 A) and low line (40 V), $I_{DC} = 0$ A.
Shown from top to bottom: drain-to-source of Q_2 (V_{C2}, 20 V/div.); primary current, 10
A/div. for a) and 1 A/div. for b); gate-to-source of Q_2 (V_{G2}, 20 V/div.); voltage across
C_4, 20 V/div.; rectified voltage, 20 V/div..

transformer voltage for half a switching cycle at zero dc bias. The value of the linear inductor and the no load condition determine the size of the saturable inductor $(V_{IN}/(2Nf_{con}) \simeq N_{SL}^2 A_C B_{SAT} 0.95)$, where A_C is the corssectional area of the core and a factor of 0.95 is used to insure the no load condition applies. Furthermore, in order to maximize the transformer turns ratio, the saturable inductor has to be designed so that the duration of the free-wheeling stages at low line and full load are minimized, i.e., proper selection of the maximum dc bias.

With this secondary-side mag-amp control, the converter is well suited for multiple output applications.

Figure 5.31 shows typical oscillograms for the key waveforms of the soft switching HB operating at a constant switching frequency of 250 kHz. An EPC-13-Z core from TDK, material H_{7C4} is used as the controllable saturable inductor. The principal winding consists of six turns of Litz wire 150/42, and the control winding consists of 50 turns of magnet wire AWG #34. In addition, 8.9 nF external capacitance was added across the rectifiers. The converter regulates the output for line ranges from 45 V to 55 V and for load ranges from full load to 0.6 A at low line, and from full load to 6 A at high line.

5.7 Summary

A new family of isolated ZVS converters which utilizes the magnetizing inductance of the power transformer to achieve zero voltage turn-on of the primary switches has been pre-

sented. By employing saturable inductors, the concept is extended so that soft switching of the output rectifiers is obtained with a minimum circulating energy flowing through the converter. The proposed converters can operate with a variable or constant switching frequency. A complete dc analysis, design guidelines, and experimental results for the half-bridge converter were presented.

6. ANALYSIS OF REACTIVE POWER IN
RESONANT CONVERTER

6.1. Introduction

Generally, higher conversion frequencies bring size reduction of power transformer and filter components and increase the overall power density. In particular, the size of the transformer is determined by the maximum volt-second product applied to the primary winding and the currents flowing through the primary and secondary windings. The maximum volt-second product determines the maximum flux density and dictates the selection of the primary turns and cross-sectional area of the core. At the same time, the currents in the primary and secondary windings, along with their respective number of turns, determine the window area of the core. By increasing the conversion frequency, the volt-second product decreases, making it possible to reduce the number of primary turns and/or to select a core with a smaller

cross-sectional area. The minimum number of primary turns is practically limited by the required turns ratio for a one-turn secondary. Beyond this, any decrease of volt-second product due to a higher conversion frequency can be achieved by a reduction in the cross-sectional area of the core. However, this trend occurs only in a limited frequency range because the core and copper (winding) losses also increase as the frequency increases, thus reducing the efficiency of the transformer. As a result, operating a transformer above a certain frequency no longer results in a size reduction, but on the contrary, requires a larger core to handle the increased core and copper losses. This frequency strongly depends on the magnetic material. Depending on the application, the frequency range of 200 kHz to 1 MHz seems to be optimal for most high-frequency magnetic materials used today.

Generally, the transformer current and voltage in isolated PWM converters are square-wave and without a noticeable phase-shift, as represented in Fig. 6.1. As a result, only real power is processed through the power transformer, and virtually no circulating energy (reactive power) is generated during the power processing. However, as switching frequencies increase into the megahertz range, PWM converters suffer from excessive switching losses. To reduce switching losses and make high-frequency operation possible, a number of resonant and soft-switching converters have been proposed [A1-A31], [B1-B36], [C1-C20], [D1-D15], [E1-E31], [F1-F7], including the converters in the first five chapters of this work. These converters utilize controlled resonances of reactive parasitics and/or externally added resonant components to achieve zero-current or zero-voltage switching of the power switches and/or rectifiers. Generally, due to continuous resonances, resonant converters have sinusoidal-type currents and/or voltages. In addition, in the majority of resonant converters, the primary current and voltage of the transformer exhibit a significant phase shift that results in a substantial reactive (circulating) power flow as shown in Fig. 6.2. Although the resonant con-
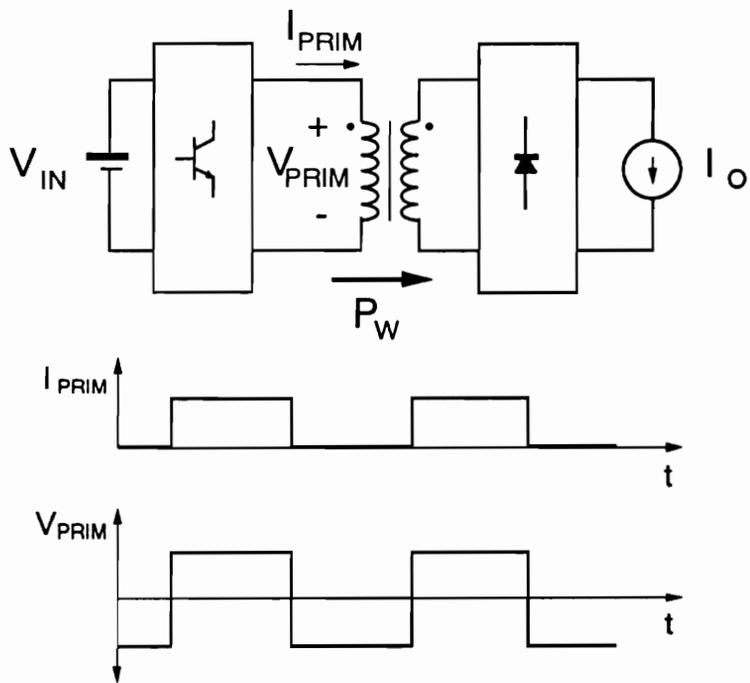
Figure 6.1.   Power flow in PWM dc/dc converters.
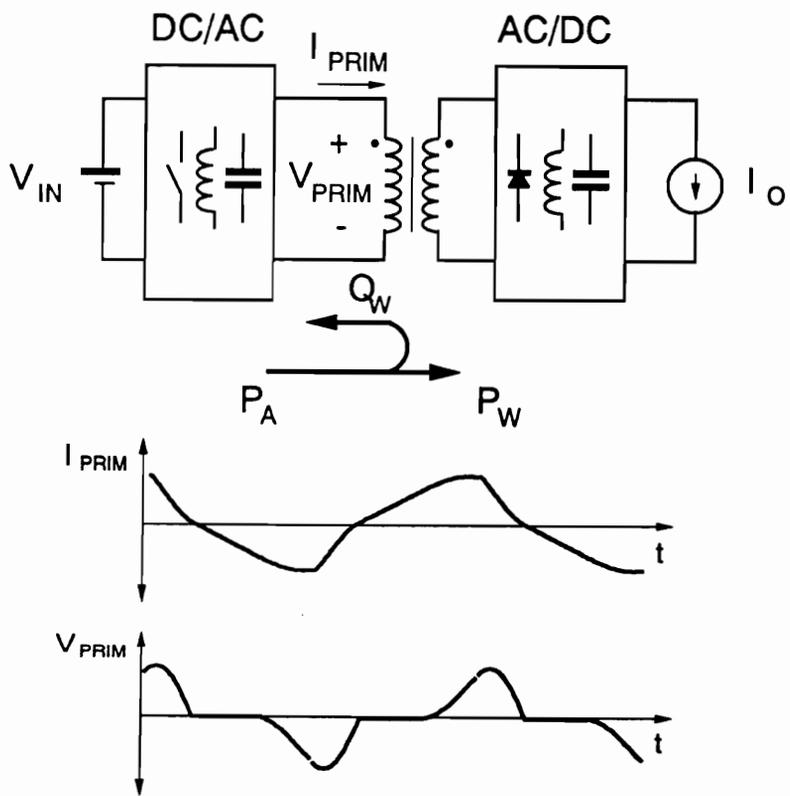
Figure 6.2. Power flow in resonant-type dc/dc converters.

verters with in-phase primary current and voltage do not circulate power, they still suffer from increased current and voltage stresses compared to their PWM counterparts. In soft-switching converters, resonances occur only during short switching transitions so that their currents and voltages are closer to square-type waveforms of PWM converters.

To achieve soft-switching for a wide range of operating line and load conditions, resonant-type converters usually need to be designed with a large amount of circulating energy (reactive power) [D1-D15]. As a result, the amount of power processed by the transformer in a resonant-type converter is usually significantly greater than that of a similar PWM converter with the same rated output power. Therefore, the size of the power transformer in high-frequency resonant-type converters is not necessarily smaller than the size of the power transformer of the corresponding PWM converter operating at a lower switching frequency. In addition, to process the increased amount of power, resonant converters require switches with higher voltage and/or current ratings. This has a detrimental effect on the overall efficiency of the power stage due to increased conduction losses, especially when a power FET is used.

In this chapter, a new methodology is presented to measure the effectiveness of power conversion. It is based on the analysis of the reactive power processed by the power transformer as an indicator of the amount of circulating energy in the resonant network. In addition, the current stresses of the power switches are derived for a number of resonant converter topologies. The results of the analysis are used to define design guidelines which minimize circulating energy. The analyzed converter topologies include: the half-bridge zero-current-switching quasi- resonant-converter (HB ZCS-QRC) [D4], the half-bridge zero-voltage-switched multi-resonant-converter (HB ZVS-MRC) [D6], the constant frequency half-bridge zero-voltage-switched multi-resonant-converter (CF HB ZVS-MRC), the HB ZVS that uses the

magnetizing inductance as a resonant element (HB ZVS-MRC (L_M), and the full-bridge series-parallel-resonant-converter (FB SPRC) [A25-A31]. Although only bridge-type topologies are presented, the analysis and conclusions can be easily extended to any other topology.

6.2. Analysis of Real and Reactive Power

Due to the presence of reactive components, the power processed by the power transformer of a resonant converter consists of real (P_W) and reactive (Q_W) power. To calculate P_W and Q_W, it is necessary to determine the primary voltage and primary current waveforms. For the five converters considered in this paper, the primary voltage and current waveforms are determined analytically using the approach described in [A25-A31], [B14], [D4-D7], [E20], and [F3]. In this approach, the operation of a converter during a single conversion cycle is divided into several topological stages corresponding to different states of the switching devices (MOSFETs and rectifiers). Equivalent circuits for each topological stage are solved analytically, assuming that the capacitor voltages and inductor currents are continuous at the boundaries of two consecutive topological stages. However, due to the nonlinear nature of these converters and the larger number of modes of operations (sequences of topological stages) usually encountered in resonant-type converters, a numerical algorithm is necessary to obtain the desired waveforms. Recently, this approach has been successfully used to obtain the dc characteristics of a number of quasi- and multi-resonant converters [A31], [B14], [D6], [E20], and [F3]. In this work, the described approach is extended to calculate the real,

reactive, and apparent power flowing through the power transformer and current stresses of the switches of the discussed converters.

Since the currents and voltages of the analyzed converters are not true sinusoids, the contributions of higher voltage and current harmonics to P_W and Q_W have to be taken into account. By applying a Fourier decomposition to the primary voltage and current waveforms, the accurate calculation of real, reactive, and apparent power, P_A, processed by the transformer can be obtained. The Fourier representation of the primary transformer voltage and current is given by:

$$V_{PRIM}(t) = \sum_{1}^{n} V_{PRIMn} \sin(n\omega_0 t) \tag{6.1}$$

and

$$I_{PRIM}(t) = \sum_{0}^{n} I_{PRIMn} \sin(n\omega_0 t + \phi_n) \tag{6.2}$$

where V_{PRIMn} and I_{PRIMn} represent the nth harmonic of the primary transformer voltage and current, respectively, and ϕ_n is the phase shift between the primary transformer voltage and current waveforms. From the Fourier representation of these signals, the real power, reactive power, and apparent power can be obtained from the following expressions:

$$P_W = \sum_{1}^{n} \frac{V_{PRIMn} I_{PRIMn}}{2} \cos(\phi_n) \tag{6.3}$$

$$P_A = V_{PRIM}^{rms} \, I_{PRIM}^{rms} \tag{6.4}$$

where $V_{PRIM}^{rms} = \left(\sum_1^n V_{PRIMn}^2/2\right)^{1/2}$ and $I_{PRIM}^{rms} = \left(\sum_0^n I_{PRIMn}^2/2\right)^{1/2}$ are the primary rms voltage, and current and P_W and P_A are the real and apparent power, respectively. Thus, the reactive power processed by the transformer is

$$Q_W = \sqrt{P_A^2 - P_W^2} \tag{6.5}$$

Finally, the effectiveness of the transformer in transferring power can be defined as the ratio of the apparent power and real power, i.e.,

$$\gamma = \frac{1}{pf} = \frac{P_A}{P_W} \tag{6.6}$$

For the best transformer utilization, and consequently, minimum transformer size, γ should be equal to one. In this case, the transformer processes only real power, since it operates with unity power factor ($pf = 1$).

The Fourier decomposition is also used to calculate the true rms value of the primary current (I_{PRIM}^{rms}). This current not only determines the copper loss in the primary winding, but also determines the current stresses and losses of the primary switches. Generally, for HB and FB type converters, the rms current of the primary switch is

$$I_{SW}^{rms} = \frac{I_{PRIM}^{rms}}{\sqrt{2}} \tag{6.7}$$

The relationship between peak switch current I_{SW}^{PK} and I_{PRIM}^{rms} depends on the shape of the primary current waveform. However, the upper boundary of I_{SW}^{PK} is

$$I_{SW}^{PK} \leq \sqrt{2}\, I_{PRIM}^{rms(\,max)} \tag{6.8}$$

where the equal sign is used for distortion-free sinusoidal waveforms. For converters with quasi-sinusoidal waveforms, such as those of Fig. 6.3(a), 6.3(c), 6.3(d), and 6.3(e), the peak switch current is close to the limit given in Eq. (6.8). On the other hand, for converters with predominantly square-wave shape of the primary current, such as in the converter of Fig. 6.3(b), the peak switch current is closer to the rms primary current, i.e., $I_{SW}^{PK} \simeq I_{PRIM}^{rms}$.

Figures 6.4 through 6.8 show the dc conversion ratio M, the power transfer effectiveness of the transformer γ, and the normalized primary rms current (I_{PRIMN}^{rms}) characteristics for the five converters (Fig. 6.3). It should be noted that the SPRC characteristics in Fig. 6.8 were obtained by taking into account the primary switch capacitance [A31]. The characteristics are all plotted as a function of f_{con}/f_O (x-axis) for different normalized load currents I_{ON} with the exception of the characteristics of the SPRC, which are given for different values of the normalized load resistance Q. For every operating point on the dc characteristics (M, f_{con}/f_O, I_{ON}), the ratio of the apparent power to the real power processed by the transformer can be determined by reading the γ value for the corresponding f_{con}/f_O. The normalized rms primary current can be determined in a similar manner. For example, the dc operating point defined in a gain characteristic can be mapped into the γ and I_{PRIM}^{rms} characteristics, as shown in Fig. 6.4. Conversely, any point in the γ or I_{PRIM}^{rms} characteristics can be mapped into the two remaining characteristics. The relationship between the real and reactive power as a function of γ is

$$Q_W = P_W \tan(\cos^{-1}(1/\gamma)) \qquad\qquad (6.9)$$

6.3. Discussion

As can be seen from Figs. 6.4 - 6.8, the HB ZCS-QRC and the HB ZVS-MRC (L_M) have relatively small $\gamma = P_A/P_W$ (close to unity). As a result, these two converters circulate very small amounts of power between the primary and the secondary circuits. The HB ZCS-QRC has the best overall power-transfer effectiveness among the analyzed converters. As seen from Fig. 6.4, its worst-case power transfer effectiveness, which occurs at full load, is $\gamma = 1.18$, and it is independent of frequency. In this converter, power is transferred from the primary to the secondary only during the on-time period of a switching cycle. Most of the power processed by the transformer is delivered to the load because the primary current and primary transformer voltage are in phase (Fig. 6.3(a)). The presence of small amounts of reactive power $(\gamma \neq 1)$ results mainly from harmonic distortion of the primary voltage waveform. Due to the resonance of the switch current that is used to create conditions for lossless turn-off, the rms primary current in the HB ZCS-QRC is higher than that in the PWM HB circuit, as shown in Fig. 6.4(c). Thus, the conduction losses in the transformer and the semiconductor switches are increased compared to the HB PWM converter.

Besides the HB ZCS-QRC, the HB ZVS-MRC (L_M) does not suffer from excessive circulating power during heavy load operation. As can be seen from Fig. 6.5, for conversion frequencies
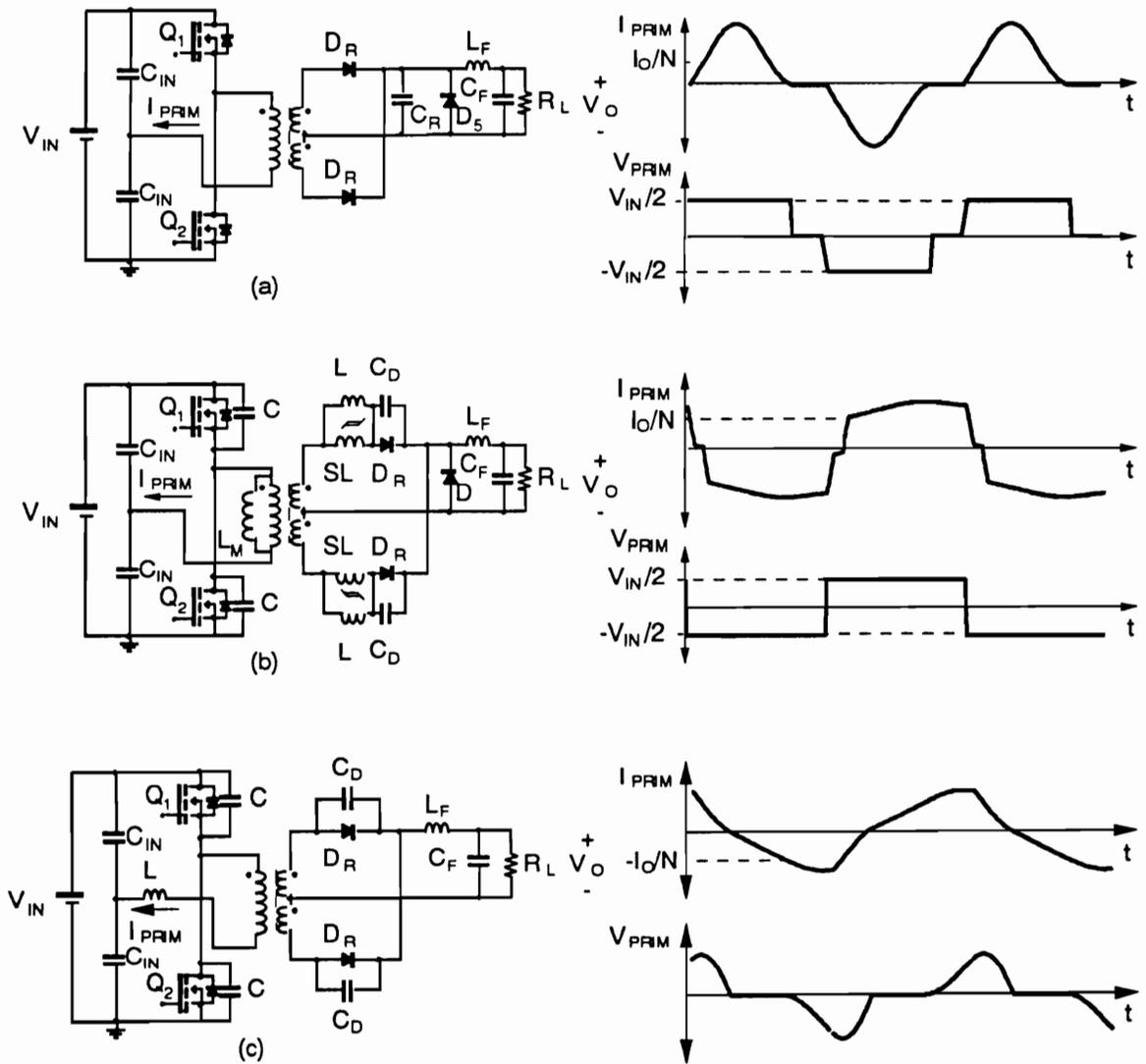
Figure 6.3a.   Circuit diagrams and primary transformer voltage and current waveforms for differ-
ent resonant converters: (a) HB ZCS-QRC, (b) HB ZVS-MRC (L_M), and (c) HB
ZVS-MRC

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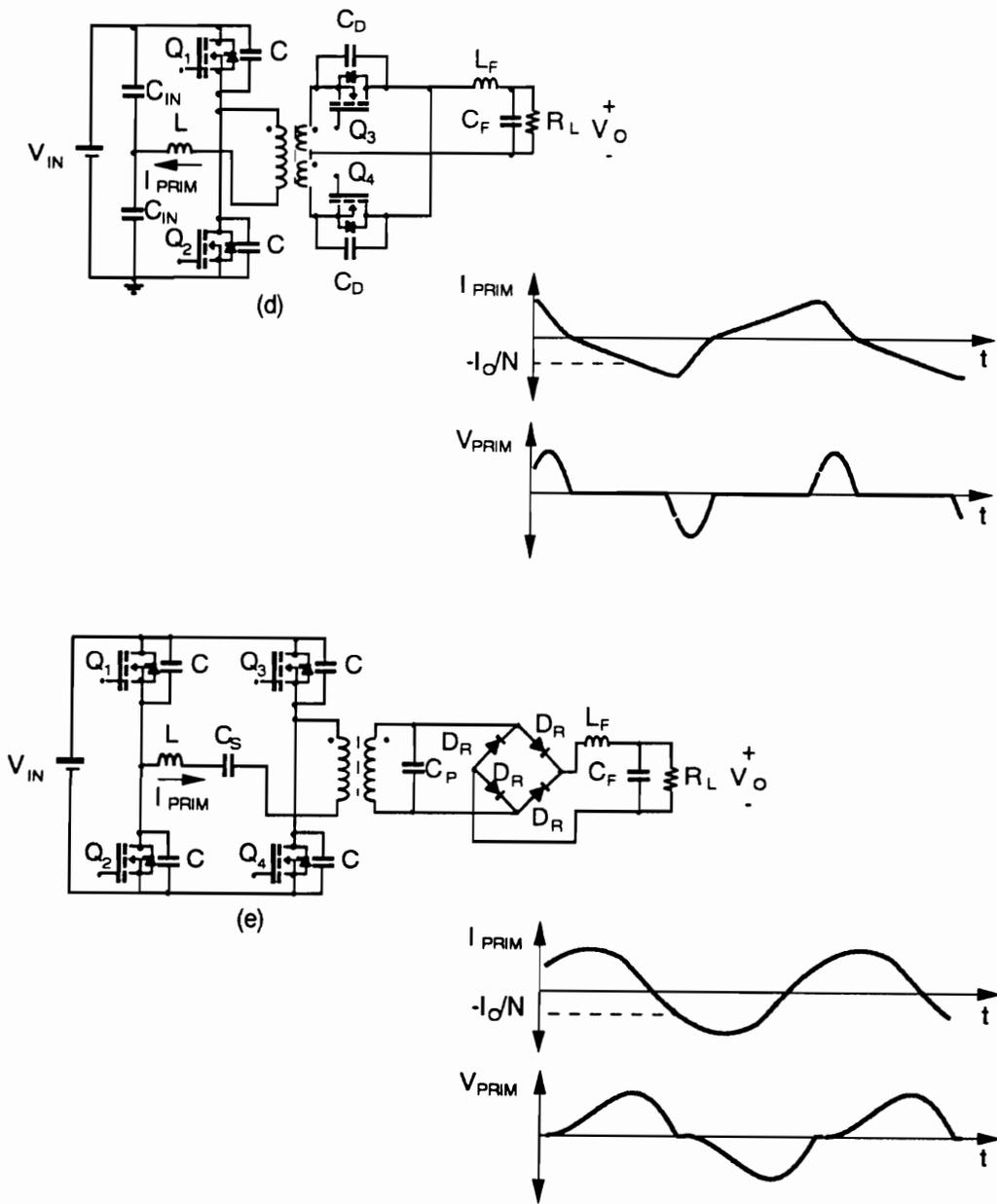
Figure 6.3b. Circuit diagrams and primary transformer voltage and current waveforms for different resonant converters continue: (d) CF HB ZVS-MRC, and (e) FB SPRC.
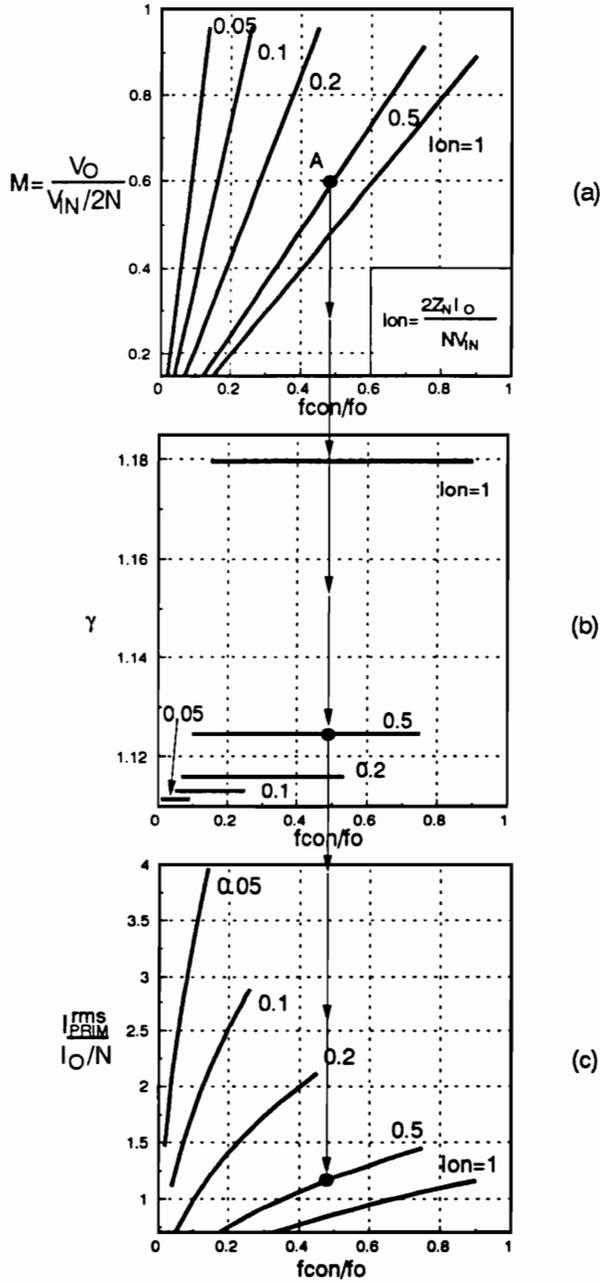
Figure 6.4. HB ZCS-QRC: (a) dc voltage conversion ratio, (b) transformer power transfer effectiveness, (c) normalized primary rms current. characteristics. $I_{ON} = 2I_OZ_O/V_{IN}N$, $Z_O = \sqrt{L/2C_R}$, and $f_O = 1/\sqrt{2C_RL}$; L is the leakage inductance of transformer.
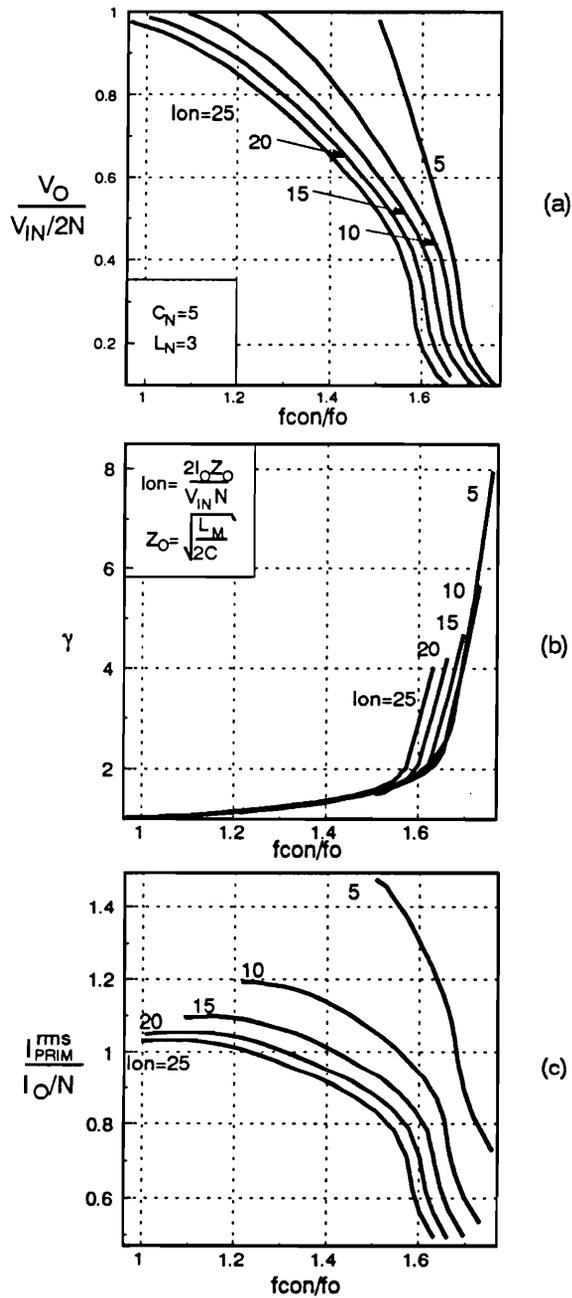
Figure 6.5. HB ZVS-MRC L_M: (a) dc voltage conversion ratio, (b) transformer power transfer effectiveness, (c) normalized primary rms current. Characteristics are for $C_N = 10$, $L_N = 3$, and $= 2$ where $C_N = 2C_D/CN^2$, $L_N = 4L_M/LN^2$ and $I_{ON} = 2I_OZ_O/V_{IN}N$, $Z_O = \sqrt{L_M/2C}$, and $f_O = 1/\sqrt{2CL_M}$. I_{SLN} is the current through the linear inductor when the corresponding saturable inductor satrurates.
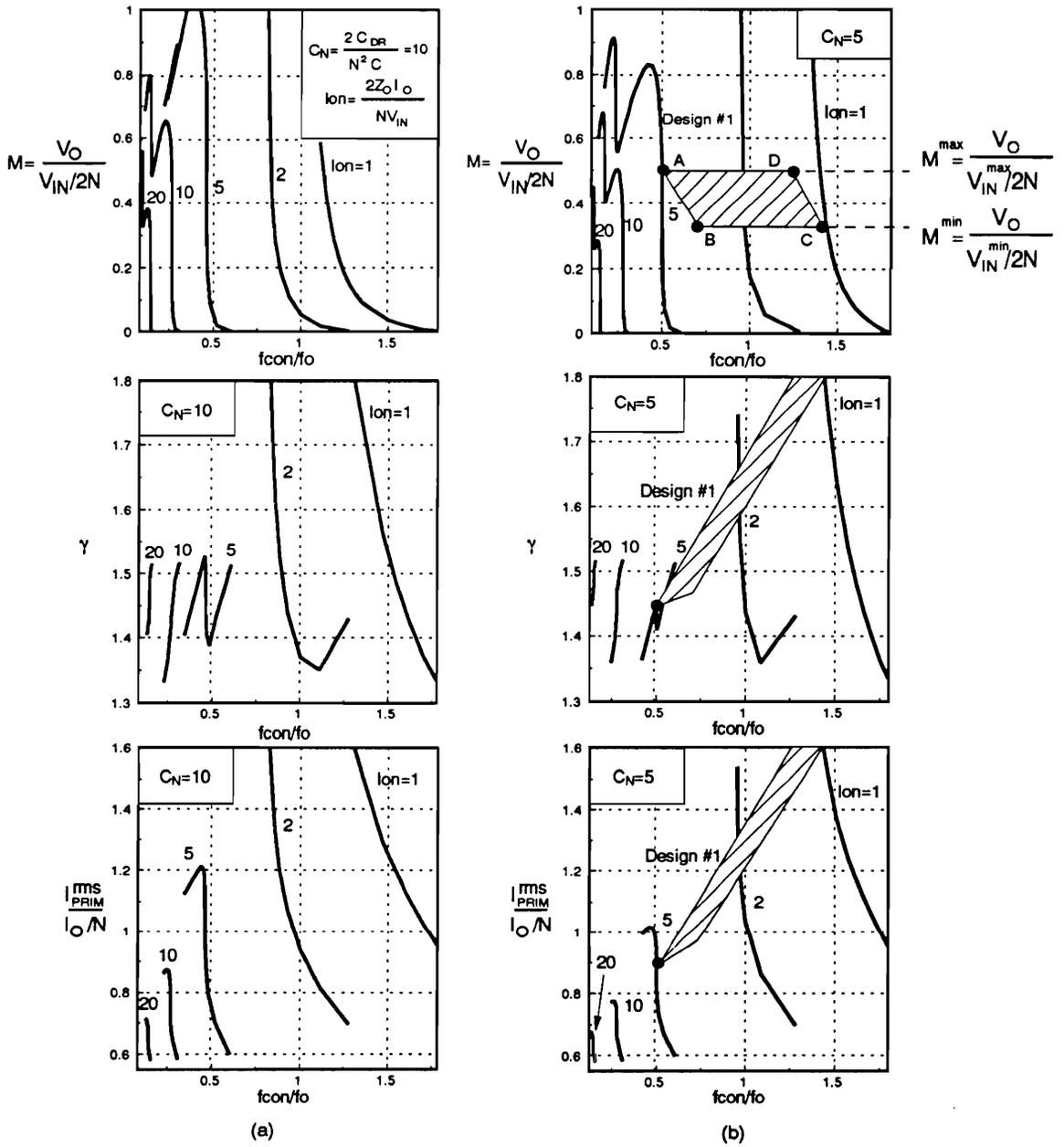
Figure 6.6. HB ZVS-MRC dc voltage conversion ratio, transformer power transfer effectiveness, and normalized primary rms current characteristics for a) $C_N = 10$, and b) $C_N = 5$ where $C_N = 2C_D/CN^2$, $I_{ON} = 2I_0Z_0/V_{IN}N$, $Z_0 = \sqrt{L/2C}$, and $f_0 = 1/\sqrt{2CL}$. Operating point A corresponds to low-line and full-load conditions.
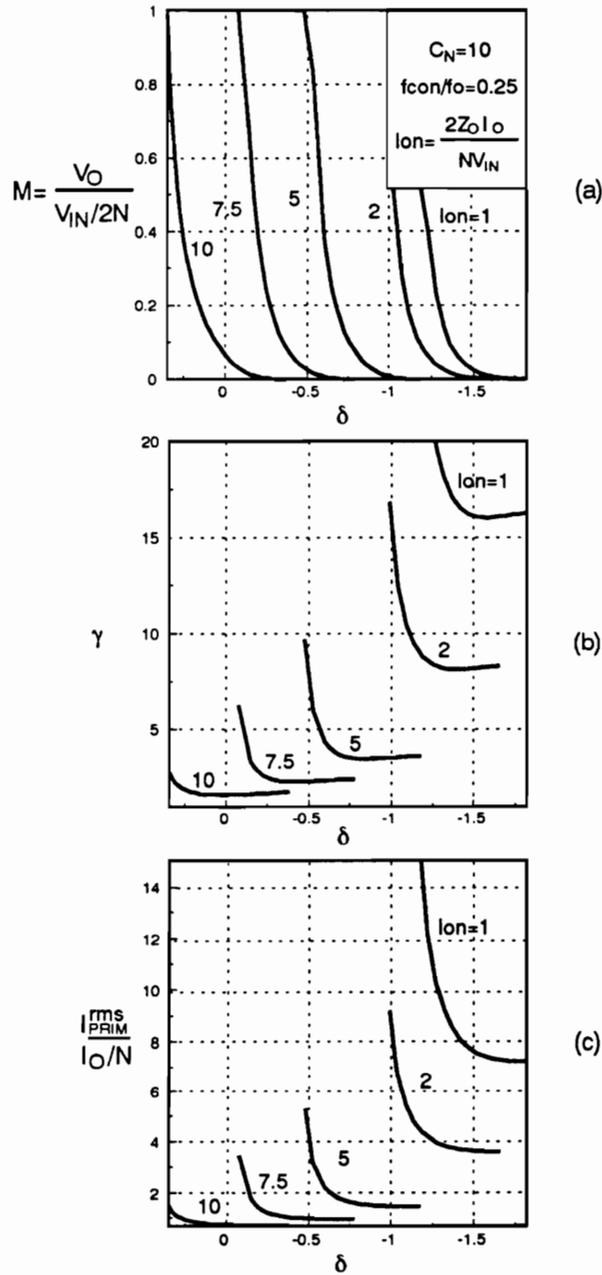
Figure 6.7. CF HB ZVS-MRC: (a) dc voltage conversion ratio, (b) transformer power transfer effectiveness, (c) normalized primary rms current. Characteristics are for $C_N = 10$ and $f_{con}/f_O = 0.250$. δ is defined as the normalized time duration (with respect to $1/f_O$) between the turn-off time of the secondary side switches (constant-frequency switches) and the primary switches, and $f_O = 1/\sqrt{2CL}$, $Z_O = \sqrt{L/2C}$, and $I_{ON} = 2I_O Z_O/V_{IN}N$.
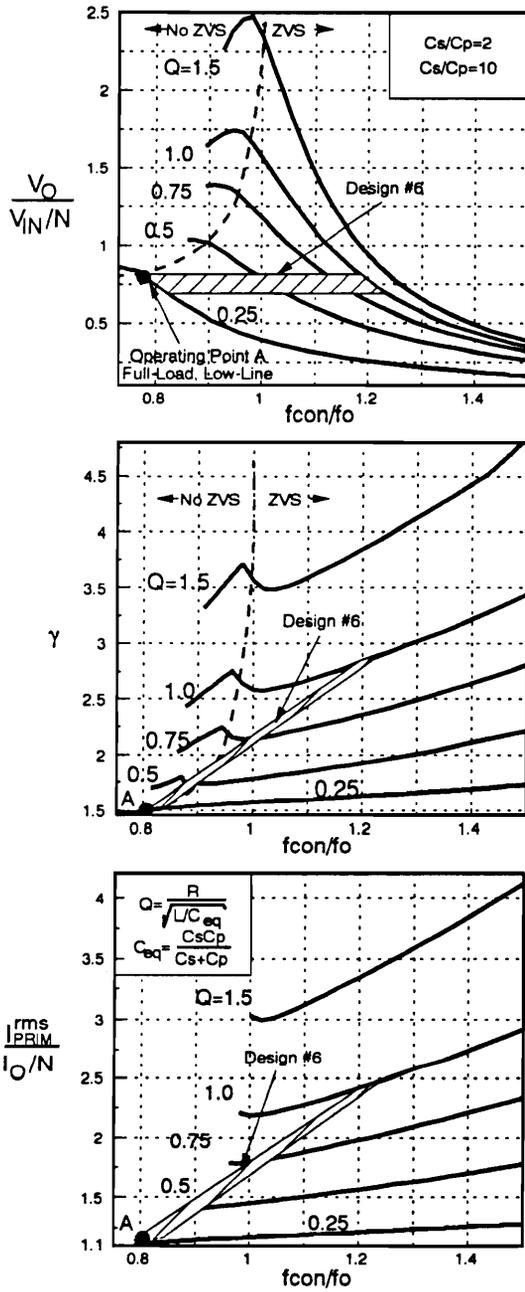
Figure 6.8a. FB SPRC dc voltage conversion ratio, transformer power transfer effectiveness, and normalized primary rms current characteristics for $C_S/C = 10$ and $C_S/C_P = 2$. Operating point A corresponds to low-line and full-load conditions. $Q = R/Z_0$, $I_{ON} = I_0 Z_0/V_{IN}N$, $Z_0 = \sqrt{L/C_{eq}}$, $f_0 = 1/\sqrt{LC_{eq}}$, and $C_{eq} = C_S C_P/(C_S + C_P)$.

Figure 6.8b. FB SPRC dc voltage conversion ratio, transformer power transfer effectiveness, and normalized primary rms current characteristics for $C_S/C = 10$ and $C_S/C_P = 1$. Operating point A corresponds to low-line and full-load conditions. $Q = R/Z_0$, $I_{ON} = I_0 Z_0/V_{IN}N$, $Z_0 = \sqrt{L/C_{eq}}$, $f_0 = 1/\sqrt{LC_{eq}}$, and $C_{eq} = C_S C_P/(C_S + C_P)$.

Figure 6.8c. FB SPRC dc voltage conversion ratio, transformer power transfer effectiveness, and normalized primary rms current characteristics for $C_S/C = 10$ and $C_S/C_P = 0.5$. Operating point A corresponds to low-line and full-load conditions. $Q = R/Z_O$, $I_{ON} = I_O Z_O/V_{IN}N$, $Z_O = \sqrt{L/C_{eq}}$, $f_O = 1/\sqrt{LC_{eq}}$, and $C_{eq} = C_S C_P/(C_S + C_P)$.

below 1.5 of the resonant frequency, γ is independent of load. , In addition, for dc voltage-conversion-ratios close to one and for $f_{con}/f_O < 1.3$, $\gamma \leq 1.2$. Therefore, a properly designed converter, which at heavy loads operates with $f_{con}/f_O < 1.3$, does not circulate a significant amount of power. The good power transfer effectiveness is due to a very short resonant interval in comparison to the switching period, and the absence of any resonance between reactive elements on different sides of the transformer. That is, the energy stored in the magnetizing inductance at the beginning of every switching transition is used to operate the active switches under ZVS, while the linear inductors located on the secondary side are used for charging and discharging the capacitance in parallel with the rectifier diodes in a controlled fashion. In addition, this converter has square-type primary current and switch current waveforms, as shown in the previous chapter, so that their rms values are only slightly higher than those in the PWM HB circuit, Fig. 6.5(c). As a result, the soft-switching of the semiconductor components is achieved without significantly increasing their conduction losses. The added components on the secondary side (SL, L, and C_D) have a minimal effect on the efficiency and the size of the converter, since the saturable reactor SL and linear inductor L can be integrated on a single surface-mount type ferrite core [F3].

The HB ZVS-MRC (Fig. 6.6), the CF HB ZVS-MRC (Fig. 6.7), and the FB SPRC (Fig. 6.8) circulate relatively large amounts of power. For these converters, the circulating power is a strong function of the load (I_{ON}) and line (M) conditions, as well as of the values of the reactive components. For example, in the multi-resonant converter (Fig. 6.3(c)), a higher ratio of rectifier capacitance C_D to the switch capacitance C, i.e., $C_N = 2C_D/(N^2C)$, results in increased circulating power when dc operating points with the same I_{ON} and M are compared. This effect is more noticeable at lighter loads (i.e., $I_{ON} = 2$, 1, ...), as can be seen by comparing γ in Figs. 6.6(a) and 6.6(b). Similarly, a higher ratio of the series to parallel capacitances C_S/C_P

in the SPRC results in smaller circulating power as can be seen by comparing γ in Figs. 8(a), 8(b), and 8(c). For these two converters, dc operating conditions with minimum circulating energy (minimum γ) occur for heavy loads ($I_{ON} = 5, 10, \ldots$, in Fig. 6.6, and $Q = 0.25, 0.5, \ldots$ in Fig. 6.8). Even when a dc operating point with minimum circulating energy is selected, the apparent power processed in the transformer of the HB ZVS-MRC and SPRC is approximately 1.4 times the real (output) power. This corresponds to circulating power comparable to the output power, since for $P_W = Q_W$, $\gamma = P_A/P_W = \sqrt{1 + (Q_W/P_W)^2} = \sqrt{2}$. Therefore, the power transformer for the best possible design in the ZVS-MRC and SPRC handles roughly twice the power of the transformer in the corresponding PWM circuit. In addition, the converters with increased circulating power (i.e., ZVS-MRCs, CF ZVS-MRCs, and the SPRC) also suffer from increased primary rms currents. The rms primary current shows the same trend with respect to load and line conditions as does γ. As a result, to accommodate larger power and rms currents, the size of the transformer in these converters has to be larger than the size of the transformer in the corresponding PWM converter operating at a similar frequency. In addition, these converters require primary switches with higher current ratings to handle the increased rms currents. Table 6.1 shows typical utilization factors of the primary switches for all of the analyzed converters operating with minimum circulating energy. The utilization factor is defined as the ratio of the output power divided by the number of switches to the product of the peak voltage and current seen by these switches.

The largest amount of circulating power and its strongest dependence on load and line conditions are found in the CF HB ZVS-MRC, Fig. 6.7(c). In applications with wide input-voltage and/or load range, this converter exhibits very poor efficiency at medium and light loads. As a result, its potential applications are limited to those with narrow input-voltage and load variations, such as the ones encountered in the systems with power-factor corrector.

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Table 6.1. Switch utilization factors for analyzed bridge converters.

Topology	Switch U.F.
PWM	$\simeq 0.25$
ZCS-QRC	$\simeq 0.10$
ZVS-MRC (L_M)	$\simeq 0.21$
ZVS-MRC	$\simeq 0.15$
CF ZVS-MRC	$\simeq 0.12$
SPRC	$\simeq 0.15$

6.4. Design Optimazation Based on Mininization of Reactive Power

Since the HB ZCS-QRC and the HB ZVS-MRC (L_M) do not circulate significant amounts of power, their design optimization procedures are relatively simple and are based on criteria other than the minimization of the reactive power as described in detail in [B14] for the HB ZCS-QRC and in Chapter 5 for the HB ZVS-MRC (L_M). On the other hand, for the HB ZVS-MRC, CF HB ZVS-MRC, and the SPRC, design optimization guidelines that maximize their overall efficiencies can be defined based on the minimization of the reactive power. As discussed in the previous section, the rms primary current (as well as the secondary currents) exhibits the same trend as the reactive power, i.e., regions of operation with smaller reactive power also have smaller rms primary currents. Consequently, the minimization of the reactive power also results in the minimization of the conduction losses and therefore maximizes the overall efficiency. Due to the limited number of applications in which the CF ZVS-MRC can be used, design examples for this converter are not considered in this paper.

In this section, several design examples for the HB ZVS-MRC and SPRC, which use the characteristics presented in Figs. 6.6, 6.8, and 6.9 to identify the regions of operation with minimum circulating energy are presented. The boundaries of the region of operation are determined from the line and load specifications. For example, point A in Fig. 6.6(b) represents low-line

(V_{IN}^{min}), full-load (I_O^{max}) operating point, while point B corresponds to the high-line (V_{IN}^{max}), full-load (I_O^{max}) operating point. Similarly, points C and D in Fig. 6.6(b) correspond to the high-line (V_{IN}^{max}), light-load (I_O^{min}) and low-line (V_{IN}^{min}), light-load (I_O^{min}) operating points, respectively. Low line operating points A and D lie on the $M^{max} = V_O/(V_{IN}^{min}/2N)$ line, while high-line (V_{IN}^{max}) operating points B and C lie on the $M_{min} = V_O/(V_{IN}^{max}/2N)$ line. These four points completely define the operating region for the given design specifications.

For example, the HB ZVS-MRC can be designed to operate in the region shown in Fig. 6.6(a). From the γ characteristics (Fig. 6.6(b)), it can be seen that Design #1 does not minimize the circulating power. The amount of circulating power can be minimized by selecting the operating regions, as shown in Fig. 6.9(a). Regions of minimum circulating energy are selected by specifying the low-line full-load operating points (point A) at minimum γ on the selected I_{ON} curves. Design #2 and Design #3 circulate the same amounts of power under full-load and low-line conditions ($\gamma \simeq 1.4$) which is less than in Design #1 ($\gamma \simeq 1.45$). However, Design #3 requires a transformer with a substantially lower turns ratio than Design #2 because the region of operation corresponding to Design #3 (Fig. 6.9(a)) lies in the region of the dc characteristics with lower gain ($M^{max} = 0.45$) than in the case of Design #2 ($M^{max} = 0.87$). The turns ratio of the transformer in Design #3 is approximately one-half of that in Design #2 (0.45/0.87 $\simeq 0.5$). Therefore, Design #2 has lower conduction losses on the primary side and maximum overall efficiency under heavy load conditions. In addition, Design #2 will operate with a narrower switching frequency range. It should be noted that by selecting the full-load, low-line operating point on a curve with $I_{ON} \leq 2$ (point A in Design #4 in Fig. 6.9(a)), the turns ratio of the transformer can be slightly increased in comparison with Design #2. However, the circulating power in this design would be larger since γ increases dramatically at lower values of I_{ON}.
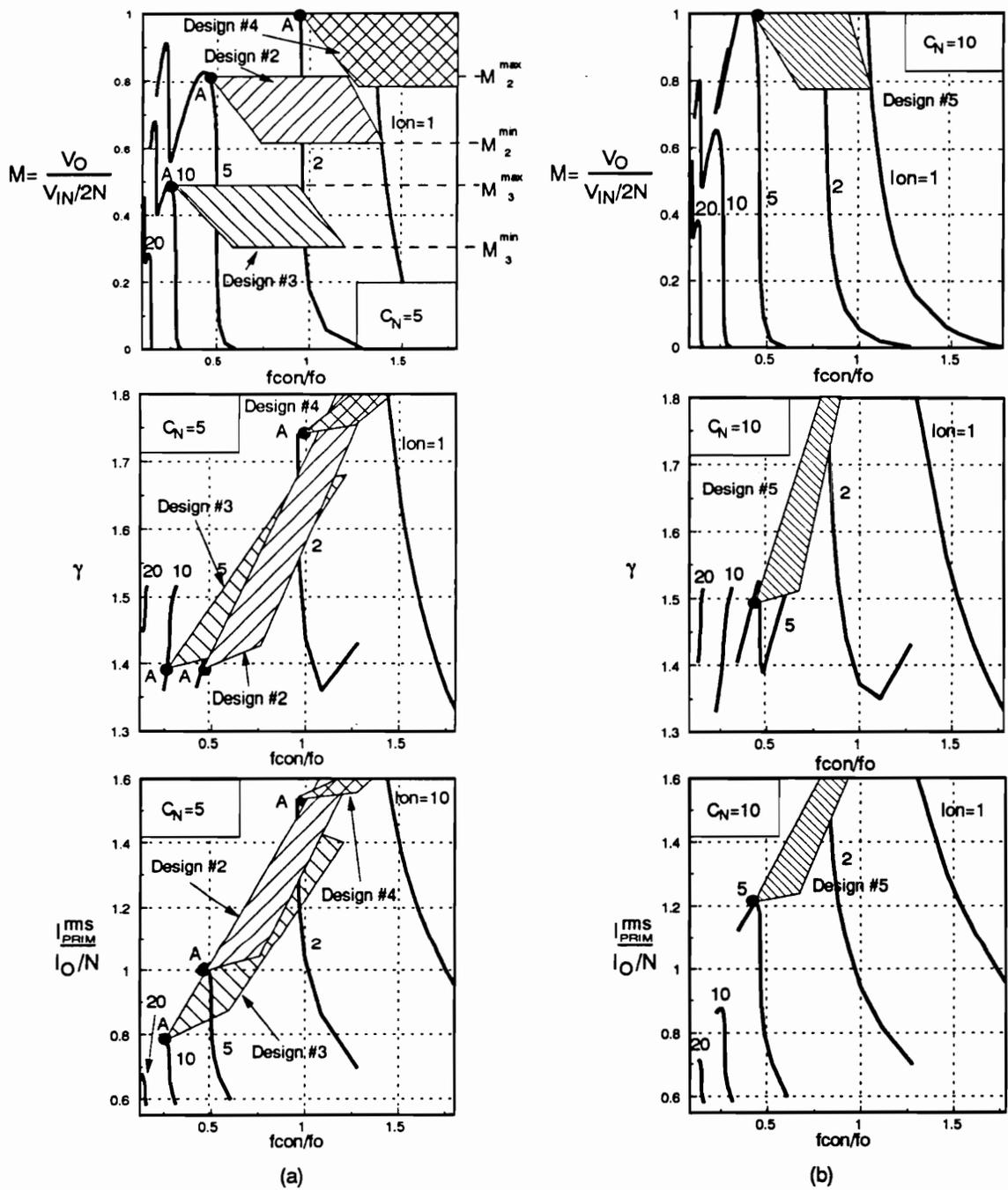
Figure 6.9. Design optimization of HB ZVS-MRC based on minimum reactive power: (a) Designs #2, #3, and #4 and (b) Design #9. Operating point A corresponds to low-line and full-load conditions.

A higher transformer turns ratio for the same I_{ON}^{max} can be obtained by selecting a characteristic with higher C_N, for example Design #5 in Fig. 6.9(b). This design clearly results in higher reactive power compared to Design #2. To compare conduction losses (I_{PRIM}^{rms}) of Design #5 relative to Design #2, it is necessary to determine the relative turns ratio of the transformers since the rms primary current is given in the normalized form. The turns ratio of the transformer in Design #5 has a larger number of turns because the low-line, full-load operating point (point A in Fig. 6.9(a)) is selected at a higher dc gain ($M_{\#5}^{max} \simeq 1$) compared to Design #2 ($M_{\#2}^{max} \simeq 0.8$). In fact, the number of turns of the transformer ($N_{\#5}$) in Design #5 is $N_{\#5} = M_{\#5}^{max}/M_{\#2}^{max} \simeq 1.25 N_{\#2}$. Therefore, the maximum rms primary current for Design #5 (operating point A) is $I_{PRIM\#5}^{rms} = 1.2 I_O^{max}/1.25 N_{\#2} = 0.96 I_O^{max}/N_{\#2} \simeq I_{PRIM\#2}^{rms}$, i.e., approximately equal to the rms primary current for Design #2. Since Design #2 circulates less power, it is more efficient than Design #5.

From the γ characteristics of the SPRC shown in Fig. 6.6 for different ratios of series to parallel capacitances C_S/C_P, it can be seen that the circulating power is a strong function of C_S/C_P for high values of Q, i.e., $Q > 0.75$. The circulating power decreases as the ratio of these capacitances increases. For example, for $Q = 1$ and in the vicinity of the resonant frequency ($f_{con}/f_O \simeq 0.9$ - 1.0), γ is approximately 4 for $C_S/C_P = 0.5$ (Fig. 6.8(a)), approximately 3 for $C_S/C_P = 1$ (Fig. 6.8(b)), and 2.5 for $C_S/C_P = 2$ (Fig. 6.8(c)). However, for lower values of Q (i.e., $Q < 0.75$), the amount of circulating power is almost independent of C_S/C_P. For $Q = 0.25$, for example, γ is in the range of 1.5 to 1.75, regardless of the C_S/C_P ratio.

The rms primary current shows a similar trend as the circulating power with respect to the C_S/C_P ratio. Generally, higher values of C_S/C_P result in smaller rms primary currents. This trend continues for lower Q values. For example, normalized rms primary currents for $Q = 0.25$ and around the resonant frequency are approximately 1.75, 1.3, and 1.1 for $C_S/C_P = 0.5$,

1, and 2 respectively. To minimize the circulating power in the SPRC, it is necessary that the low-line, full-load operating point (point A on the dc characteristics in Fig. 6.8) be placed at the maximum gain $(M = V_O/(V_{IN}/N))$ on the lowest Q curve. The operating regions in Figs. 6.8(a), 6.8(b), and 6.8(c), labeled Designs #6, #7, and #8, indicate the regions with the minimum circulating energy.

From Figs. 6.8(a), 6.8(b), and 6.8(c), it can be seen that Designs #6 and #7 have smaller circulating energy ($\gamma \simeq 1.5$ for operating point A) compared to Design #8 ($\gamma \simeq 1.75$). Due to the higher dc gain, Designs #7 and #8 have a higher transformer turns ratio ($M^{max} \simeq 1$ for operating point A) compared to Design #6 ($M^{max} \simeq 0.8$). The turns ratio of the transformer in Design #6 is approximately 20% smaller than the turns ratio for Designs #7 and #8, i.e., $N_{\#6} \simeq 0.8 N_{\#7,\#8}$. As a result, the rms primary current for Design #6 is larger than the rms primary current for Design #7. Namely, from Fig. 6.6(a), $I^{max}_{PRIM\#6} = 1.1 I^{max}_O / N_{\#6} = 1.1 I^{max}_O / 0.8 N_{\#7,\#8} \simeq 1.45 I^{max}_O / N_{\#7}$. Since for Design #8 (Fig. 6.8(c)), $I^{rms}_{PRIM\#8} \simeq 1.5$, the rms primary currents for Designs #6 and #8 are almost the same. Since Design #7 circulates the least amount of power and has the smallest rms primary current, it is expected to yield the best efficiency.

It should be noted that if operating point A is selected at a higher Q, as for example $Q = 0.5$ for Design #9 in Fig. 6.9(b), the circulating energy is increased compared to Design #7 which lies in the $Q = 0.25$ curve. At the same time, the rms primary currents are approximately equal, even though a higher transformer turns ratio for Design #9 can be used since the dc gain is higher $(M_{max} \simeq 1.25)$ than in Design #7 $(M_{max} \simeq 1)$. From Fig. 6.8(b) $I^{rms}_{PRIM\#9} \simeq 1.6 I^{max}_O / N_{\#9} = 1.6 I^{max}_O / 1.25 N_{\#7} = 1.28 I^{max}_O / N_{\#7}$, while $I^{rms}_{PRIM\#7} \simeq 1.25 I^{max}_O / N_{\#7}$. Therefore, Design #9 is less efficient than Design #7. However, Design #9 does operate with a narrower frequency range. Therefore, higher Qs ($Q > 0.25$; i.e., not minimum γ) should be

considered only when there is a frequency range constraint. This result agrees with the design guidelines for the SPRC provided in [A18]. The characteristics in Fig. 6.8 can also be used to evaluate this trade-off if the switching-frequency range is a design variable.

As can be seen from the above design examples, even when the HB ZVS-MRC and SPRC are designed for minimum γ, the reactive power circulating through the converters is comparable with the power delivered to the load. As a result, the transformer in these converters usually has to be designed to process more than twice the output power. Therefore, the expected transformer size reduction from high-frequency operation of resonant converters in most cases cannot be realized. This is especially true if the converters need to operate with a wide input-voltage range.

Generally, the poor power-transfer characteristics of resonant converters are associated with a large phase-shift between the primary voltage and current of the transformer . Good sinusoidal waveforms with minimum distortion are not necessary to achieve efficient power transfer through the transformer ($\gamma \simeq 1$). For example, ZCS-QRCs have good transformer power-transfer characteristics since these signals are in phase, even though their primary transformer voltage and current are not sinusoids.

The power transfer characteristics of the transformer in ZVS resonant converters can be improved considerably ($\gamma \simeq 1$) by placing the secondary-side resonant capacitances on the primary side. This dramatically reduces the amount of reactive power that needs to be handled by the transformer, but results in the loss of soft switching on the rectifiers. However, the primary-side resonance does not reduce the reactive power circulating on the primary circuit that has to be handled by the primary switches and resonant components. It also precludes

the absorption of the transformer leakage inductance into the resonant network, causing parasitic ringings and losses on the secondary side.

6.5. Summary

The analysis of reactive (circulating) power and rms currents in a number of resonant converters is presented. The results of the analysis show that the HB ZCS-QRC and the soft-switched HB ZVS-MRC (L_M) circulate relatively small amounts of power. However, the circulating power in HB ZVS-MRC, CF HB ZVS-MRC, and SPRC is found to be considerably larger. The analysis is used to generate sets of characteristics for each converter that can be used in their design optimization based on the minimization of the circulating power. In addition, several design examples are presented for HB ZVS-MRC and SPRC. The described analysis and procedure can be easily extended to any other resonant or soft-switched topology.

7. CONCLUSION

This dissertation introduced two new zero-voltage-switched power conversion technologies; the constant-frequency (CF) zero-voltage-switched (ZVS) multi-resonant (MR) technology and the zero-voltage-switched technology that utilizes the magnetizing inductance of the power transformer as a resonant element (ZVS (L_M)). The CF ZVS-MR family of converters is an extension of ZVS-MRCs modified so that constant frequency operation is possible. Multi-resonant operation at constant switching frequency was achieved by replacing the rectifier diode(s) by an active switch.

The second ZVS technique makes use of the magnetizing inductance of the power transformer as a resonant component. The operation of these converters is modified so that during the switching transition the magnetizing inductance is free to resonate. By adding a second active switch in the rectifier circuit, the time during which the secondary winding(s) is connected to the load can be controlled. Therefore, during the switching transition the magnetizing

inductance is disconnected from the load and allowed to resonate with the resonant capacitances so that soft switching operation of the primary switch(es) is achieved.

Any PWM topology can be transformed into its CF multi-resonant counterpart by replacing the active/passive semiconductor devices with the CF multi-resonant switch network. To operate CF ZVS-MRCs in the low megahertz switching frequencies, external resonant components have to be added since the intrinsic parasitic reactances of the power stage are not sufficient. The dc analysis of the forward and HB topologies has been described in detail. A numerical algorithm was used to solve the transcendental equations describing the operation of these two topologies. Based on the dc analysis, a design trade-off study was performed, resulting in a set of design guidelines for each of these two topologies. It was found that to optimize the efficiency of CF ZVS-MRCs, the ratio of resonant capacitances, C_N, and the frequency of operation should be minimized. On the other hand, the value of the characteristic impedance has to be maximized to minimize conduction losses. The value of the turns ratio of the transformer is selected so that the transformer core losses due to the inherent dc bias, characteristic of single-ended topologies, is minimized. Finally, because of the added active switch in the secondary side, CF ZVS-MRCs have secondary side control, resulting in simple control schemes.

Unlike the PWM forward, the CF forward ZVS-MRC does not require an additional transformer resetting circuit. Transformer reset was achieved from the interaction of the magnetizing inductance and the secondary side resonant capacitor, C_D. Like most single-ended ZVS topologies, the primary transistor voltage will resonate to a maximum value of several times the input voltage, resulting in a design trade off between the maximum voltage rating and device $R_{DS}(on)$ when selecting the device for this switch.

7. CONCLUSION

The design of the CF HB ZVS-MRC follow guidelines similar to the one given for the CF forward ZVS-MRC but because of the clamping of the primary switch voltage and the zero dc biased operation of the transformer, the design of the HB topology is more straightforward.

The concept of using the magnetizing inductance of the transformer as a resonant component was first considered as it relates to zero voltage turn-on of the primary power switches. The switches used to insure that the magnetizing inductance was free to resonate during the switching transition can be implemented using either semiconductor or magnetic switches. IGBTs and SCRs can be used as the secondary side switches. Similarly, the series combination of a diode and a saturable inductor can also be used. Variable or constant frequency operation of these converters is possible. For constant frequency operation, the secondary side switches result in secondary side control.

Soft turn-on of the rectifier diodes was obtained by adding the parallel combination of a saturable and linear inductor in series with the rectifier diodes (ZVS-MRC (L_M)). The linear inductor was used to charge and discharge the junction capacitance of the rectifiers in a controlled fashion. The saturable inductor carried most of the load current and clamped the resonance of the linear inductors to minimize the circulating energy needed for soft switching. The parallel combination of saturable and linear inductor can be implemented in practice with a single amorphous core.

The bridge-type topologies of this family of converters operate with quasi-square type currents and voltages much like the ones of their PWM counterparts, resulting in low conduction losses. A dc analysis was presented for the HB ZVS-MRC (L_M). The dc analysis was performed using a nonlinear algorithm that solved the transcendental equations describing the operation of this converter. Based on the dc analysis, a design trade-off study was performed

resulting in a set of design guidelines for the soft-switched HB converter. It is found that to optimize the efficiency, the ratio of resonant components, C_N and L_N, need to be minimized to minimize the circulating energy flowing through the converter. The value of the current at the time the saturable reactor saturates, I_{SAT} (the saturation current for the integrated version of linear/saturable inductor) and the ratio between the slope of the linear and saturable inductances, L/SL, should be minimized to reduce the frequency range. This also contributes to minimize the circulating energy flowing through the converter.

Constant frequency implementation of the HB ZVS-MRC (L_M) was implemented by replacing the saturable inductors with controllable saturable inductors. The blocking time of the saturable reactor was controlled by changing the dc bias on the core. A controllable saturable inductor fabricated from an EI ferrite core was used. The control winding was placed on the center leg while the saturable inductor winding was placed on one of the outside legs. The ac flux resulting from the saturable inductor winding, which could disturb the control, was isolated to the outside path of the core by adding a single turn copper ring in the center leg. This copper ring prevented any ac flux from entering the center leg. The dc bias established by the control winding allowed one of the outside legs to easily saturate.

In the final chapter a comprehensive analysis of the reactive power (circulating power) in several resonant converters was presented. The ratio of reactive power to real power transferred through the power transformer was used to asses the effectiveness of the different power conversion techniques. Ideally, power processing techniques should result in zero reactive power, i.e., transferr only real power. The studied converter topologies include: HB zero-current-switched (ZCS) quasi-resonant-converter (QRC), HB zero-voltage-switched (ZVS) multi-resonant-converter (MRC), the HB zero-voltage-switched (ZVS) multi-resonant-converter (MRC) (L_M), and the HB series-parallel-resonant-converter (SPRC). From the studied

topologies, the HB ZCS-QRC and the HB ZVS-MRC (L_M) generated the least amount of reactive power. On the other hand, CF ZVS-MRCs generated a large amount of reactive power. In most cases, the reactive power transferred in these converters was greater than the real power transferred, resulting in an increased size of the power transformer. Since the reactive power processed by CF ZVS-MRCs does not decrease considerably as the output load decreases, the performance of these converters is very sensitive to the changes in load, i.e., the efficiency decreases rapidly as the output load decreases. For similar reasons, the performance of this family of converters is also very sensitive to line variations. The study suggests that CF ZVS-MRCs are not suitable for applications that require a large input voltage range or high performance at fractional loads.

High-frequency power conversion provides numerous research opportunities, resulting in new and better power conversion techniques. The following research areas are of considerable interest for future work.

- **Phase shift control of ZVS-MRCs.** Due to large circulating energy, the CF ZVS-MR family of converters discussed in this dissertation has limited applications. A second alternative to achieving constant frequency operation of ZVS-MRCs is phase shift control. Phase shift control has been successfully implemented for PWM and resonant topologies. Phase shift control of a class-E dc-dc converter was presented in [C14], but for practical reasons, a one transformer topology would be more desirable.

- **Evaluation of the merits of single-ended topologies of the new family of converters using the magnetizing inductance.** Many low power applications (below 100 W) require single-ended topologies because of their low part count. The implementation of single-ended

topologies was shown, but the complete analysis of these converters was not presented. The forward and flyback topologies may be found to have merits in high-frequency applications.

- **Integration of magnetic structures in the soft switched HB.** The implementation of the soft switched HB results in three different magnetic structures. These magnetic structures are small, but it would be very desirable to integrate the saturable inductors and transformer into a single core.

- **Soft-switching techniques with PWM type control and waveforms.** Square-type currents and voltages result in low conduction losses. Furthermore, constant frequency control simplifies the design of the filter and magnetic components. Topologies that achieve soft-switching while still maintaining square-type currents and voltages and operate at a constant switching frequency would be very desirable.

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Appendix A. Analysis CF Forward ZVS-MRC

Figure A.1 shows the circuit diagram for CF forward ZVS-MRCs. Capacitance C_S is the resonant capacitance across transistor Q_1 and it includes the output capacitance of this switch. Capacitance C_D is the resonant capacitance across the secondary windings of the power transformer, and it incorporates the parasitic capacitance of both rectifier D_1 and CF switch Q_2. L is the resonant inductor and it absorbs the leakage inductance of the power transformer.
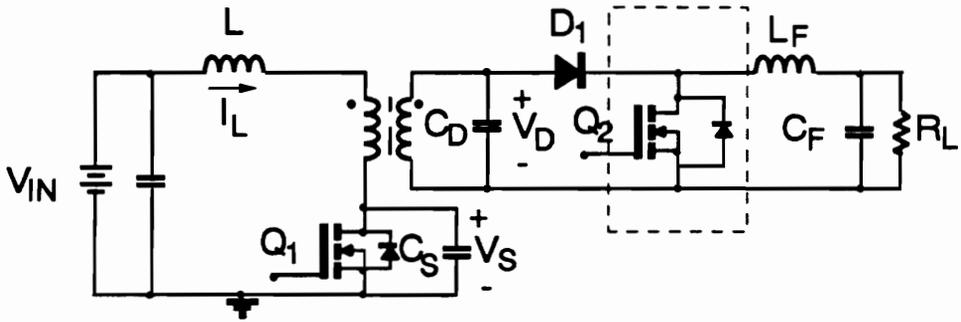
Figure A.1. The CF forward ZVS-MRC.

A.1 DC Analysis

To simplify the analysis it is assumed that:

a) the output filter inductance is sufficiently large and can be approximated by a current source with a value equal to the output current, I_O;

b) the voltage drop across the conducting semiconductor switches (MOSFETs and diodes) is negligible;

c) the switching times of the semiconductor switches are zero; and

d) the magnetizing inductance of the power transformer is large and can be represented by an equivalent current source, I_M, whose magnitude depends on the operating condition but is constant over one switching cycle.

To further simplify the analysis, the load current, I_O, and the resonant capacitance, C_D, are reflected to the primary side of the transformer. In addition, diode D_1 and transistor Q_2 are replaced by a single-pole double-throw switch. The equivalent model of the simplified converter is shown in Fig. A.2.

During one switching cycle, the converter goes through a sequence of five of the six possible topological stages shown in Fig. A.3. The CF forward ZVS-MRC can operate in four different modes, each representing a different sequence of topological stages. Modes II.A and II.B occur for heavy load currents, whereas Modes I.A and I.B occur for light output currents.
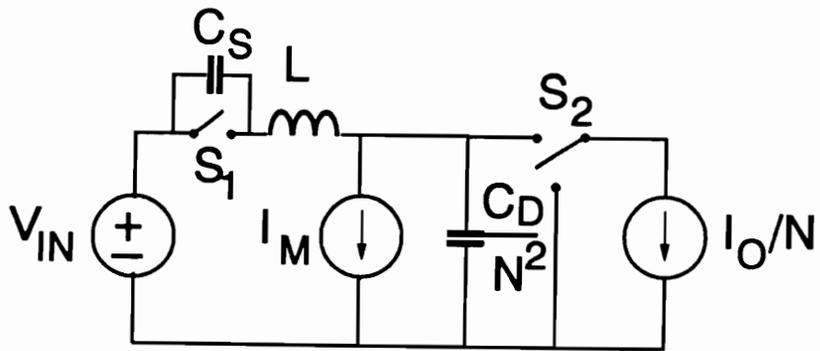
Figure A.2. Equivalent model of the CF forward ZVS-MRC.
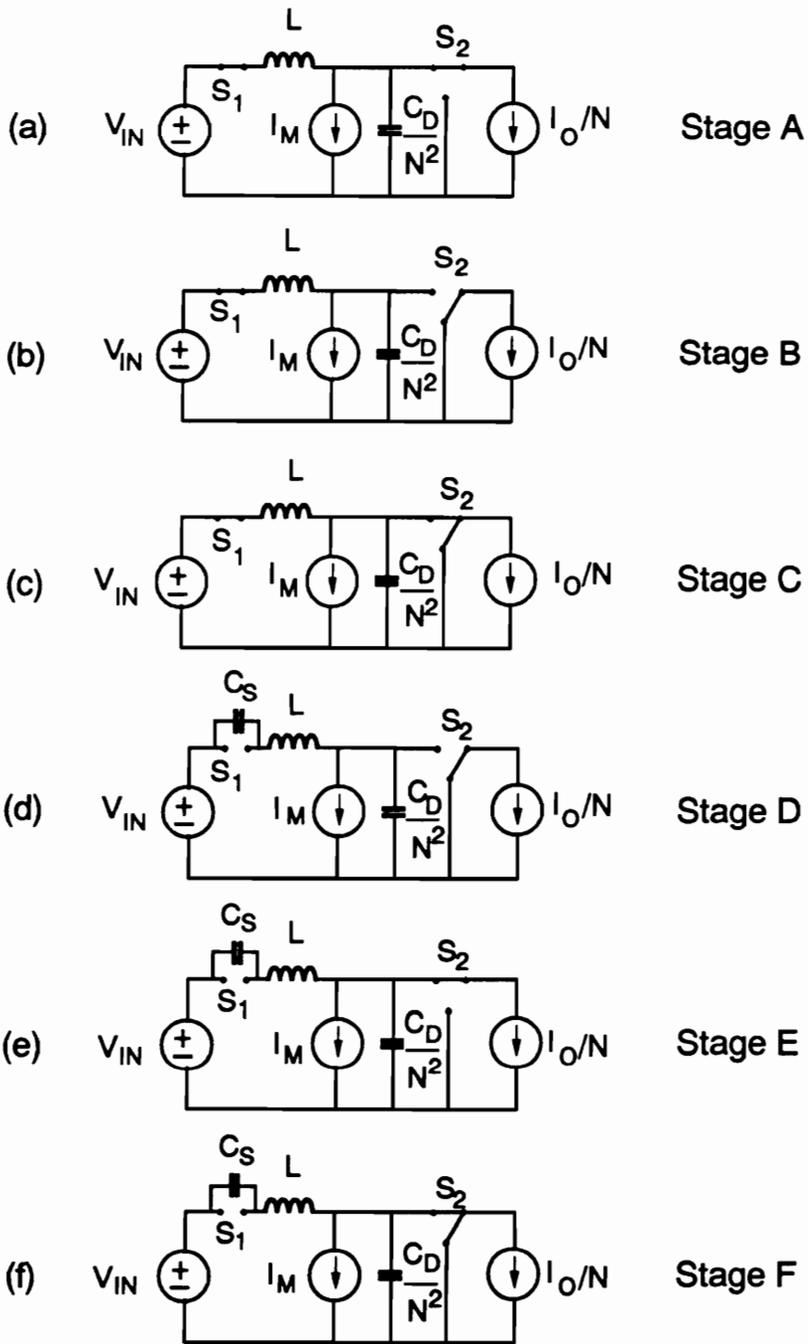
Figure A.3. Topological stages of the CF forward ZVS-MRC: (a) Stage A, (b) Stage B, (c) Stage C, (d) Stage D, (e) Stage E, and (f) Stage F.

A.2.1.1 Mode I of Operation

Mode I.A

The sequence of the topological stages in Mode I.A is A-B-C-A-E. Figure A.4 shows the key waveforms of the CF forward ZVS-MRC in this mode of operation.

Stage A $[T_O, T_1]$, Fig. A.3(a)

During this stage transistor Q_1 and diode D_1 are conducting and transistor Q_2 is off. Voltage V_D across C_D is positive and capacitance C_D and inductor L resonate until the voltage across Q_2 reaches zero at time T_1 and its antiparallel diode starts conducting. At the same time diode D_1 turns off.

Stage B $[T_1, T_2]$, Fig.A.3(b)

Since the antiparallel diode of Q_2 is conducting, capacitance C_D continues to resonate with L. This stage ends at time T_2 when voltage V_D increases to zero and diode D_1 turns on. To achieve lossless turn-on, Q_2 should be turned on during this stage.

Stage C $[T_2, T_3]$, Fig. A.3(c)

Figure A.4. Ideal waveforms of the CF forward ZVS-MRC operating in Mode I.A, from top to bottom: drain-source voltage of switch Q_1, V_S, resonant inductor current I_L, capacitor voltage V_D, gate-source voltage V_{G1}, and gate-source voltage V_{G2}. Δt is defined as the time between the turn-off of switch Q_1 and the constant frequency switch Q_2.

In this stage D_1 and Q_2 conduct. As a result, voltage V_D is clamped to zero and the voltage across resonant inductor L is V_{IN}. The resonant inductor current increases linearly until Q_2 is turned off at time T_3.

Stage A [T_3, T_4], Fig. A.3(a)

Diode D_1 remains on and capacitance C_D and inductance L start to resonate. Voltage V_D increases in a resonant manner. This stage ends at time T_4, when Q_1 is turned off.

Stage E [T_4, T_5], Fig. A.3(e)

Diode D_1 remains on, so capacitances C_D and C_S and inductance L resonate. This stage ends at time T_5, when voltage V_S returns to zero through a resonant oscillation. Transistor Q_1 should be subsequently turned on to achieve lossless turn-on. The next cycle is then initiated.

From the preceeding explanation, it can be seen that the resonance of capacitance C_D is interrupted for only a short interval, $T_3 - T_2$. Switch Q_1 remains on during this interval and the resonant inductor current increases linearly.

Mode I.B

The sequence of the topological stages in Mode I.B is A-B-C-F-E. Figure A.5 shows the key waveforms of the CF forward ZVS-MRC in this mode of operation.

Stage A [T_O, T_1], Fig. A.3(a)
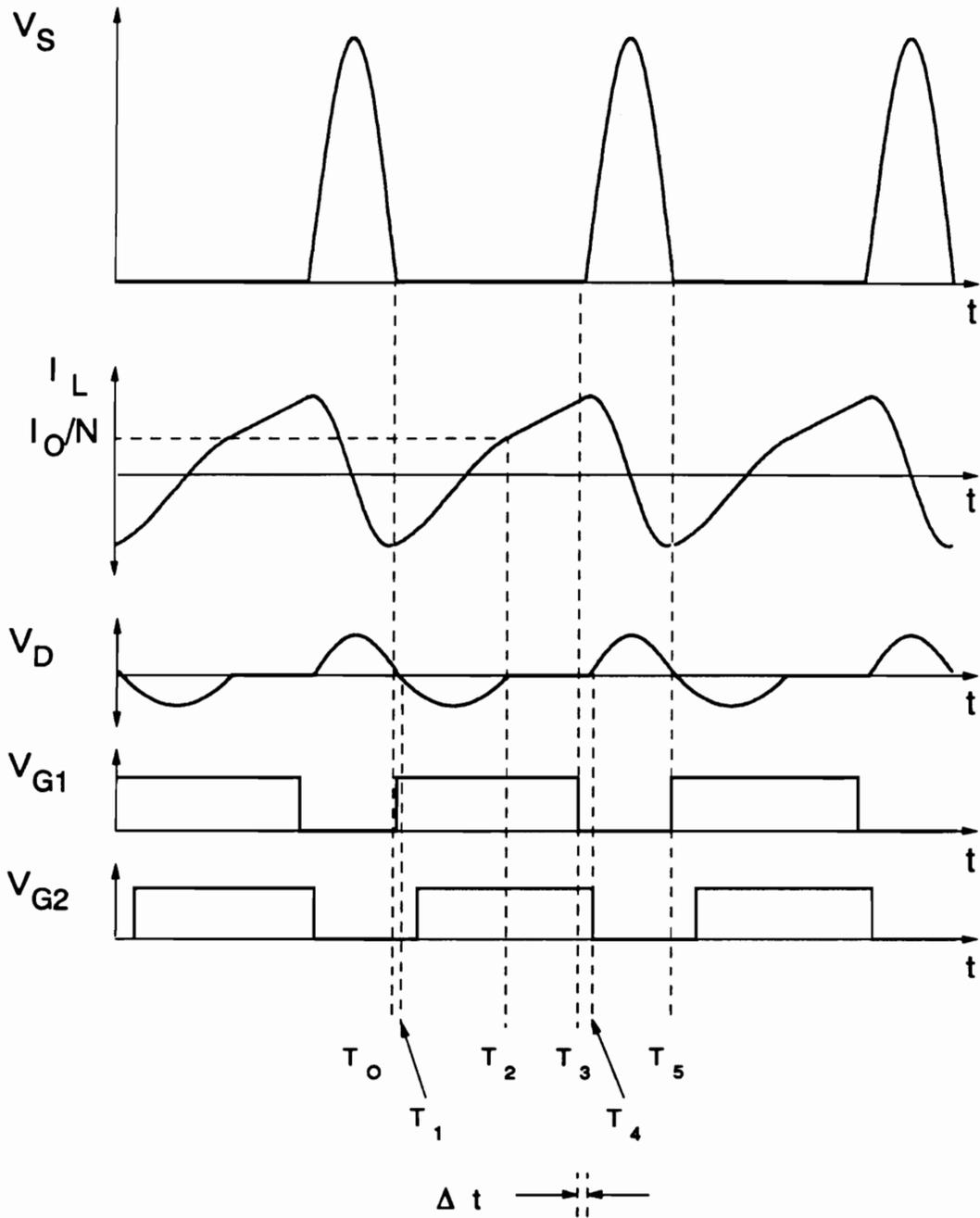
Figure A.5. Ideal waveforms of the CF forward ZVS-MRC operating in Mode I.B, from top to bottom: drain-source voltage of switch Q_1, V_S, resonant inductor current I_L, capacitor voltage V_D, gate-source voltage V_{G1}, and gate-source voltage V_{G2}. Δt is defined as the time between the turn-off of switch Q_1 and the constant frequency switch Q_2.

During this stage transistor Q_1 and diode D_1 are conducting and transistor Q_2 is off. Voltage V_D across C_D is positive, and capacitance C_D and inductor L resonate until the voltage across Q_2 reaches zero at time T_1 and the antiparallel diode of Q_2 starts conducting. At the same time, diode D_1 turns off.

Stage B [T_1, T_2], Fig. A.3(b)

Since the antiparallel diode of Q_2 is conducting, capacitance C_D continues to resonate with L. This stage ends at time T_2 when voltage V_D increases to zero, turning on diode D_1. To achieve lossless turn-on, Q_2 should be turned on during this stage.

Stage C [T_2, T_3], Fig. A.3(c)

In this stage D_1 and Q_2 conduct. As a result, voltage V_D is clamped at zero and the voltage across resonant inductor L is V_{IN}. This stage ends at time T_3 when switch Q_1 is turned off.

Stage F [T_3, T_4], Fig. A.3(f)

Diode D_1 remains on, switch Q_1 is off, and capacitance C_S and inductance L start to resonate. Voltage V_S increases and the resonant inductor current increases in a resonant manner until switch Q_2 is turned off at time T_4.

Stage E [T_4, T_5], Fig. A.3(e)

Diode D_1 is on, so capacitances C_S and C_D and inductance L resonate. This stage ends at time T_5 when voltage V_S returns to zero through a resonant oscillation. Transistor Q_1 should be subsequently turned on to achieve lossless turn-on. The next cycle is then initiated.

This mode of operation is very similar to Mode I.A, the difference being that in Mode I.B the resonance of capacitance C_D is interrupted for a longer time, resulting in switch Q_2 being turned off after switch Q_1 is turned off.

A.2.1.2 Mode II of Operation

In Mode I of operation capacitor voltage V_D is positive at the turn-off time of switch Q_1. In Mode II of operation capacitor voltage V_D is negative at the turn-off time of switch Q_1. As long as capacitor voltage V_D is negative, the forward diode D_1 is off and the load current freewheels through the antiparallel diode of switch Q_2.

Mode II.A

The sequence of the topological stages in Mode II.A is B-C-A-E-D. Figure A.6 shows the key waveforms of the CF forward ZVS-MRC in this mode of operation.

Stage B [T_O, T_1], Fig. A.3(b)
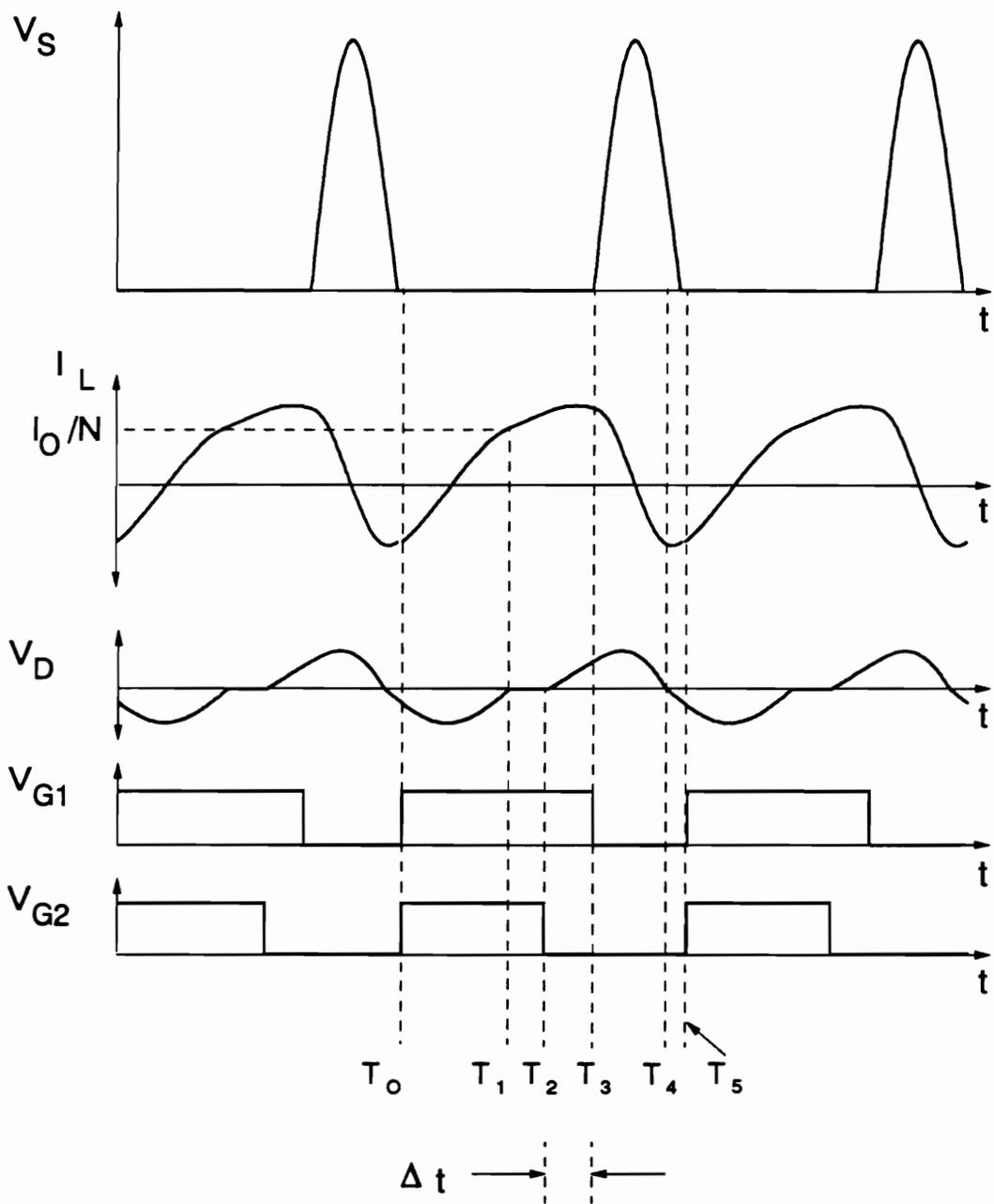
Figure A.6. Ideal waveforms of the CF forward ZVS-MRC operating in Mode II.A, from top to bottom: drain-source voltage of switch Q_1, V_S, resonant inductor current I_L, capacitor voltage V_D, gate-source voltage V_{G1}, and gate-source voltage V_{G2}. Δt is defined as the time between the turn-off of switch Q_1 and the constant frequency switch Q_2.

Since the antiparallel diode of Q_2 is conducting, capacitance C_D resonates with L. This stage ends at time T_1 when voltage V_D increases to zero, turning on diode D_1. To eliminate the turn-on loss, Q_2 should be turned on during this stage.

Stage C [T_1, T_2], Fig. A.3(c)

In this stage D_1 and Q_2 conduct. As a result, voltage V_D is clamped at zero and the voltage across resonant inductor L is V_{IN}. The resonant inductor current increases linearly until Q_2 is turned off at time T_2.

Stage A [T_2, T_3], Fig. A.3(a)

Diode D_1 remains on and capacitance C_D and inductance L start to resonate. Voltage V_D increases in a resonant manner. This stage ends at time T_3, when Q_1 is turned off.

Stage E [T_3, T_4], Fig. A.3(d)

Diode D_1 remains on and capacitances C_S and C_D resonate with inductance L. This stage ends at time T_4, when voltage V_D decreases to zero through a resonant oscillation and forward diode D_1 turns off.

Stage D [T_4, T_5], Fig. A.3(e)

During this stage the antiparallel diode of switch Q_2 conducts and diode D_1 is off. Voltage V_D across C_D is negative and capacitance C_S and C_D resonate with inductor L until the voltage

across Q_1 reaches zero at time T_5 and the antiparallel diode of Q_1 starts conducting. Q_1 should be subsequently turned on to achieve lossless turn-on. The next cycle is then initiated.

Mode II.B

The sequence of the topological stages in Mode II.B is B-C-F-D-E. Figure A.7 shows the key waveforms of the CF forward ZVS-MRC in this mode of operation.

Stage B [T_0, T_1], Fig. A.3(b)

Since the antiparallel diode of Q_2 is conducting, capacitance C_D resonates with L. This stage ends at time T_1 when voltage V_D increases to zero, turning on diode D_1. To achieve lossless turn-on, Q_2 should be turned on during this stage.

Stage C [T_1, T_2], Fig. A.3(c)

In this stage D_1 and Q_2 conduct. As a result, voltage V_D is clamped to zero and the voltage across resonant inductor L is V_{IN}. The resonant inductor current increases linearly until Q_1 is turned off at time T_2.

Stage F [T_2, T_3], Fig. A.3(f)

Diode D_1 and switch Q_2 remain on and voltage V_D remains clamped to zero. Voltage V_S increases in a resonant manner. This stage ends at time T_4, when Q_2 is turned off.
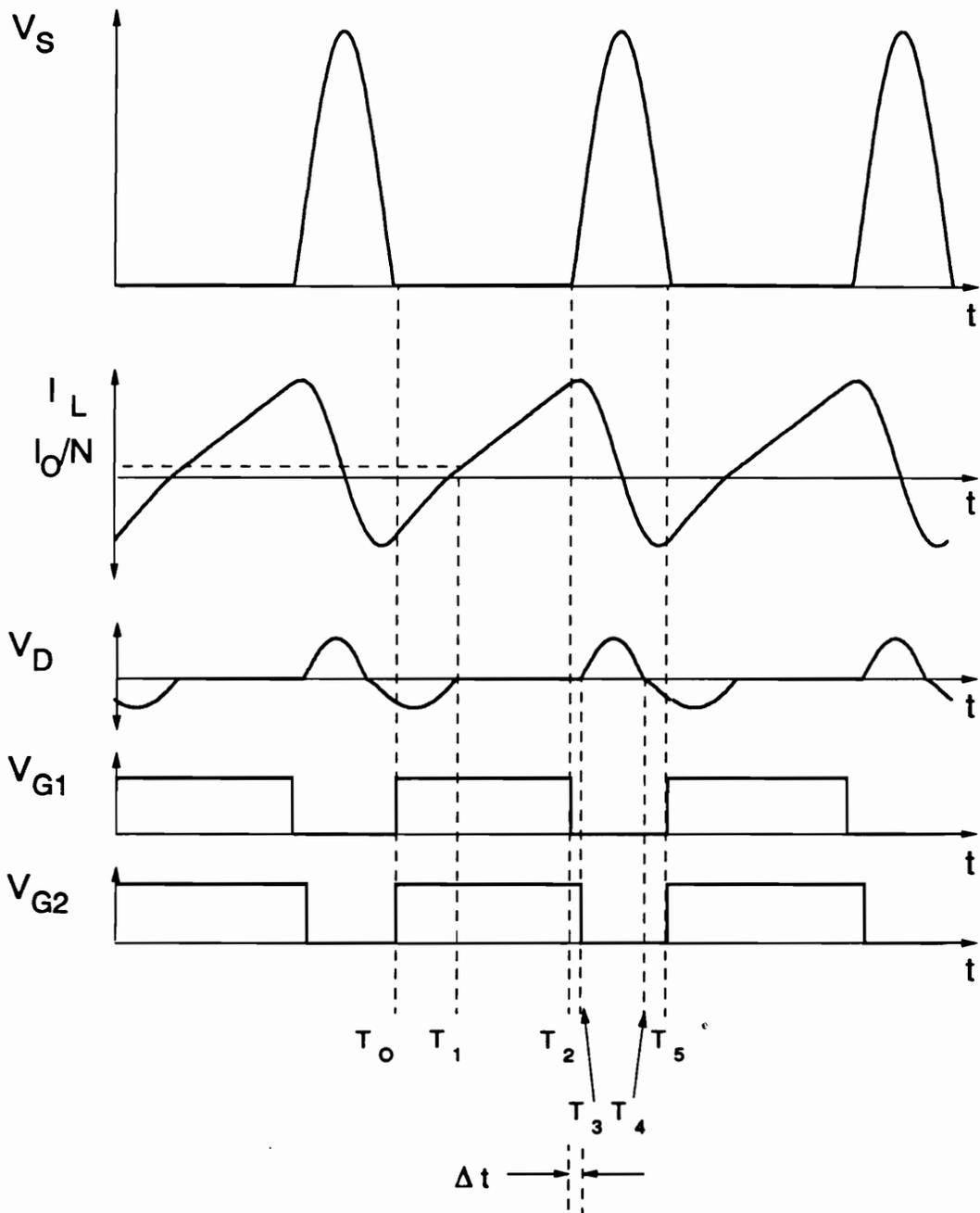
Figure A.7. Ideal waveforms of the CF forward ZVS-MRC operating in Mode II.B, from top to bottom: drain-source voltage of switch Q_1, V_S, resonant inductor current I_L, capacitor voltage V_D, gate-source voltage V_{G1}, and gate-source voltage V_{G2}. Δt is defined as the time between the turn-off of switch Q_1 and the constant frequency switch Q_2.

Stage E [T_3, T_4], Fig. A.3(e)

Diode D_1 remains on and capacitances C_S and C_D and inductance L resonate. Capacitor voltage V_D increases in a resonant manner. This stage ends at time T_5 when voltage V_D resonates back to zero turning diode D_1 off and forcing the antiparallel diode of switch Q_2 on. Transistor Q_2 should be subsequently turned on to achieve soft switching.

Stage D [T_4, T_5], Fig. A.3(d)

During this stage voltage V_D across C_D is negative and the antiparallel diode of switch Q_2 conducts. Capacitances C_D and C_S resonate with the resonant inductor L. This stage ends at time time T_5 when the voltage across switch Q_1 resonates back to zero. Switch Q_1 should be turned on soon after to achieve lossless turn-on, initiating a new switching cycle.

The difference between Mode II.A and Mode II.B is similar to the one described between modes I.A and I.B; in Mode II.B switch Q_2 is turned off after switch Q_1 is already off.

The sequence of the four modes of operation are summarized in Table A.1.

Table A.1. Modes of operation of the CF forward ZVS-MRC.

MODE	STAGE SEQUENCE
I.A	A - B - C - A - E
I.B	A - B - C - F - E
II.A	B - C - A - E - D
II.B	B - C - F - E - D

A.2 DC Voltage-Conversion-Ratio

Figures A.8a - A.15a show the typical dc voltage-conversion-ratio characteristics of the CF forward ZVS-MRC as a function of δ. δ is defined as the time between the turn-off of the CF switch Q_2 and the turn-off of primary switch Q_1 (Δt in Fig. A.4) normalized with respect to $1/f_O$, where $f_O = 1/2\pi\sqrt{LC_S}$ is the resonant frequency. The characteristics are given for different normalized switching frequencies f_S/f_O and different effective resonant capacitance ratio $C_N = C_D/(C_S N^2)$, where N is the turns ratio of the transformer. The running parameter in Figs. A.8a - A.15c is the normalized output current $I_{ON} = Z_O I_O/N V_{IN}$, where $Z_O = \sqrt{L/C_S}$ is the characteristic impedance of the power stage.

A complete set of design characteristics is given for $C_N = 2, 3, 5$, and 7, and $f_S/f_O = 0.55, 0.6, 0.65$, and 0.8 (Figs. A.8a - A.15c). Characteristics for all possible combinations are not given since not all possible combinations result in practical design curves. For example, low capacitance ratios ($C_N = 2$) and low switching frequencies ($f_S/f_O < 0.8$) will result in large conduction times of the CF switch (high conduction losses) for all values of I_{ON}. Therefore, this characteristics will not provide an efficient design. Similarly, high capacitance ratios ($C_N = 7$) and high switching frequencies ($f_S/f_O > 0.6$) result in dc voltage conversion ratio characteristics with M < 0.3. Again, this characteristics will not result in a practical design.

A.3 DC Analysis of the Topological Stages

The following section contains the mathematical derivations pertaining to the different topological stages resulting from the forward ZVS-MRC operating at a constant switching frequency. Analytical expressions for the initial conditions, circuit equations, their solutions, and durations of the topological stages for the ideal CF forward ZVS-MRC are presented.

STAGE A [T_{A0}, T_{A1}] (Fig. A.16)

Initial Conditions:

$$v_S(T_{A0}) = 0 \qquad (A.1.a)$$

$$v_D(T_{A0}) = V_D^A \qquad (A.1.b)$$

$$i_L(T_{A0}) = I_L^A \qquad (A.1.c)$$

Equations:

$$L\frac{di_L(t)}{dt} + v_D(t) = V_{IN} \qquad (A.2.a)$$

$$i_L(t) - C_D\frac{dv_D(t)}{dt} = I_O + I_M \qquad (A.2.b)$$
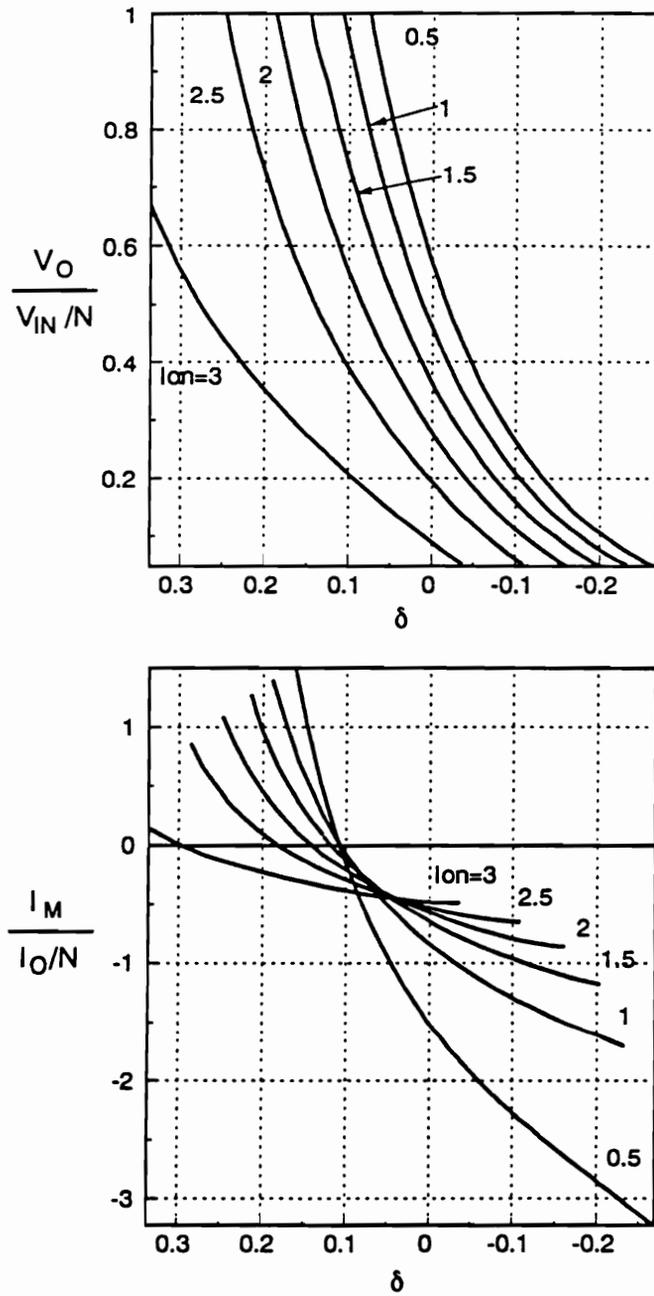
Figure A.8a. DC voltage conversion ratio and V_S^{max}/V_{IN} curves of the CF forward ZVS-MRC for $C_N = 2$ and $f_S/f_O = 0.80$. $C_N = C_D/(CN^2)$, $I_{ON} = I_O Z_O/V_{IN}$, $Z_O = \sqrt{L/C}$, and $f_O = 1/2\pi\sqrt{LC}$.
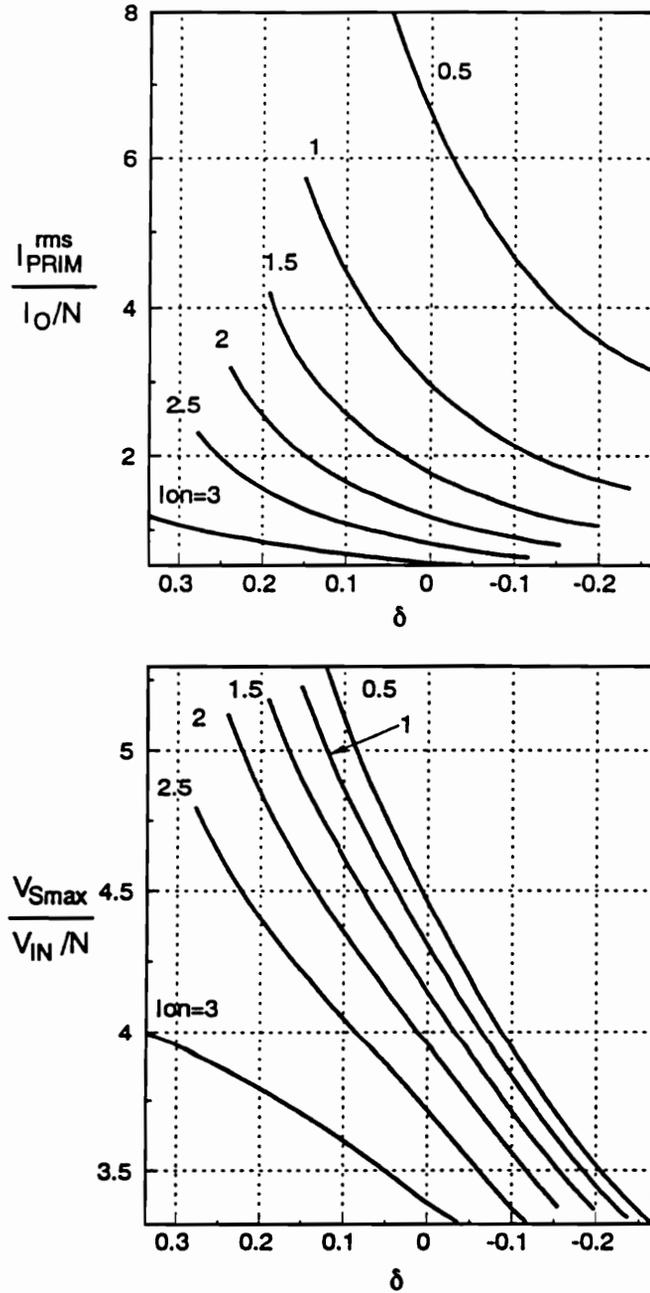
Figure A.8b. Normalized primary rms current and V_L^{p-p}/V_{IN} characteristics of the CF forward ZVS-MRC $C_N = 2$ and $f_S/f_O = 0.80$. $C_N = C_D/(CN^2)$, $I_{ON} = I_O Z_O/V_{IN}$, $Z_O = \sqrt{L/C}$, and $f_O = 1/2\pi\sqrt{LC}$.
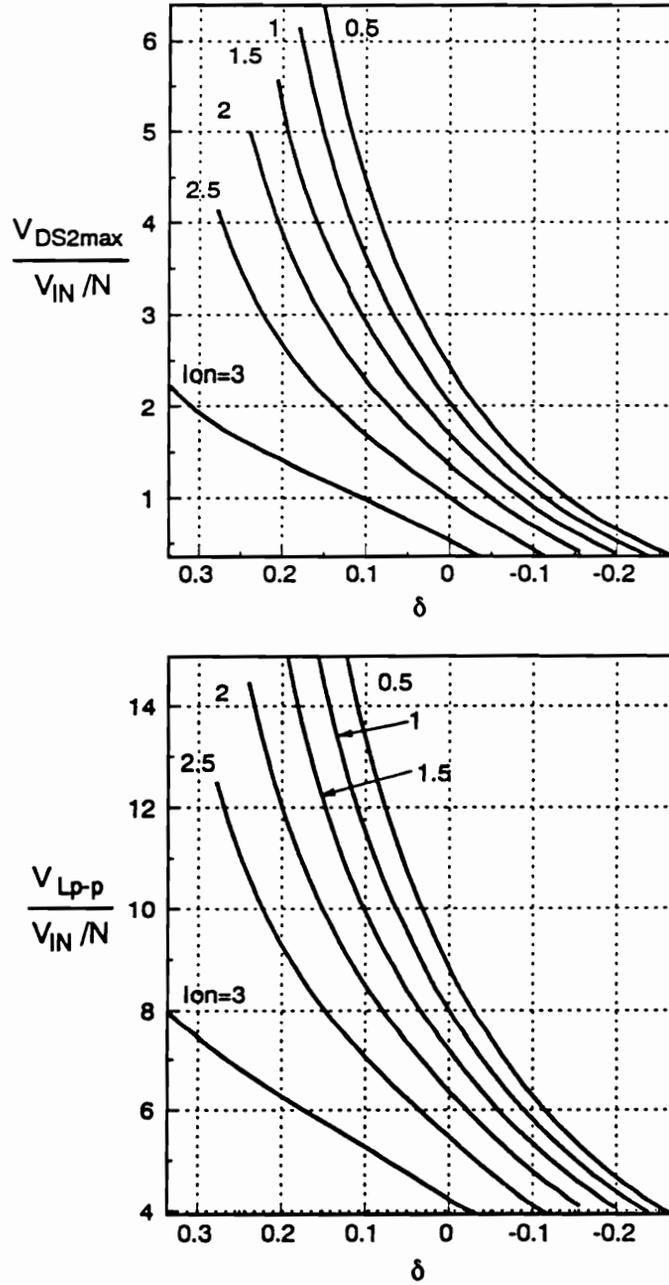
Figure A.8c. V_{DS2}^{max}/V_{IN} and $I_M/(I_O/N)$ characteristics of the CF forward ZVS-MRC $C_N = 2$ and f_S/f_O = 0.80. $C_N = C_D/(CN^2)$, $I_{ON} = I_O Z_O/V_{IN}$, $Z_O = \sqrt{L/C}$, and $f_O = 1/2\pi\sqrt{LC}$.
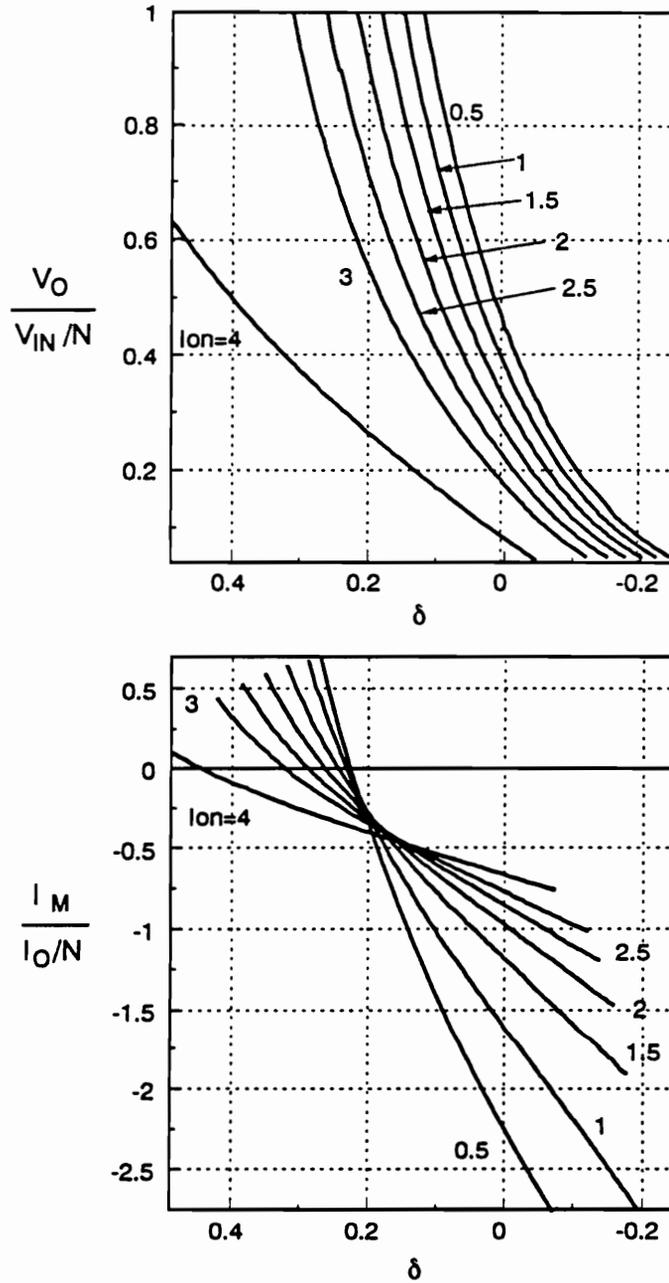
Figure A.9a. DC voltage conversion ratio and V_S^{max}/V_{IN} curves of the CF forward ZVS-MRC for $C_N = 3$ and $f_S/f_O = 0.65$. $C_N = C_D/(CN^2)$, $I_{ON} = I_O Z_O/V_{IN}$, $Z_O = \sqrt{L/C}$, and $f_O = 1/2\pi\sqrt{LC}$.
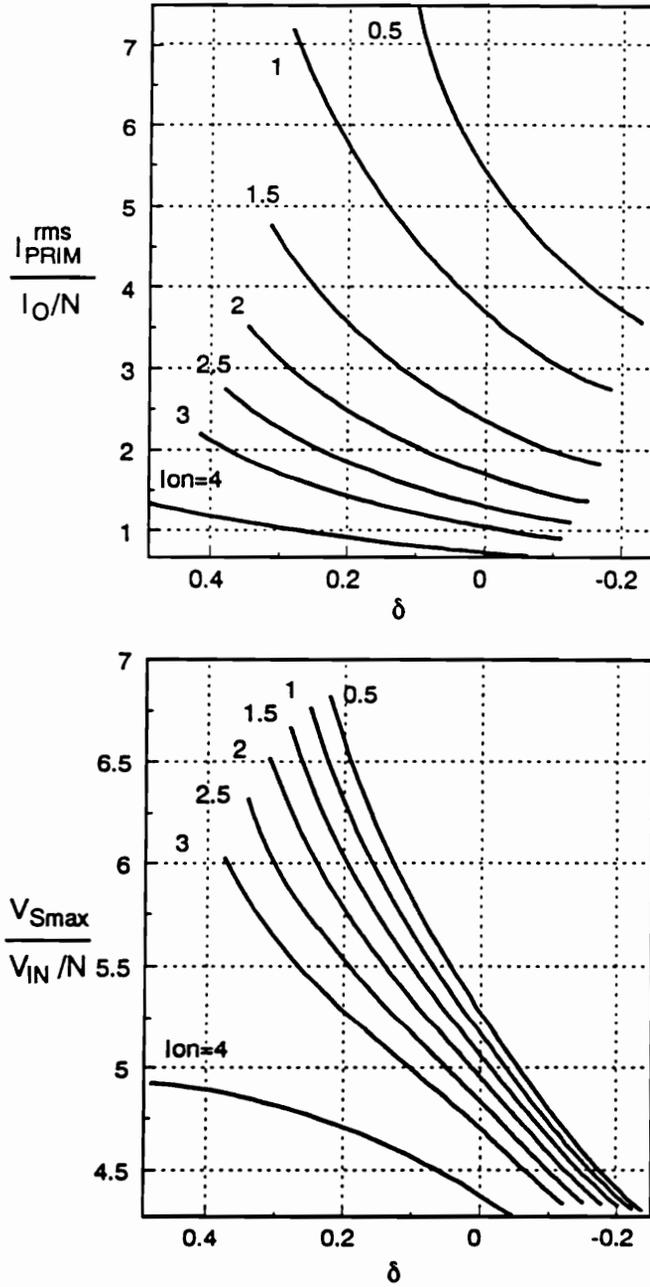
Figure A.9b. Normalized primary rms current and V_L^{p-p}/V_{IN} characteristics of the CF forward ZVS-MRC C_N = 3 and f_s/f_O = 0.65. $C_N = C_D/(CN^2)$, $I_{ON} = I_O Z_O/V_{IN}$, $Z_O = \sqrt{L/C}$, and $f_O = 1/2\pi\sqrt{LC}$.
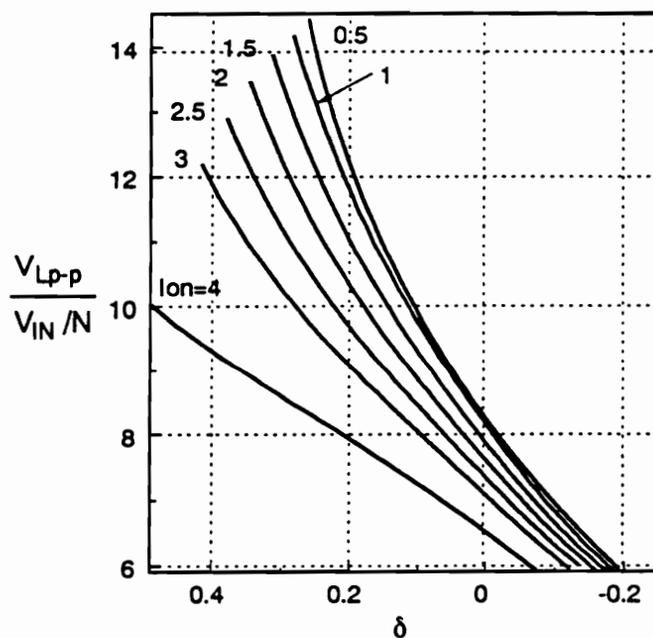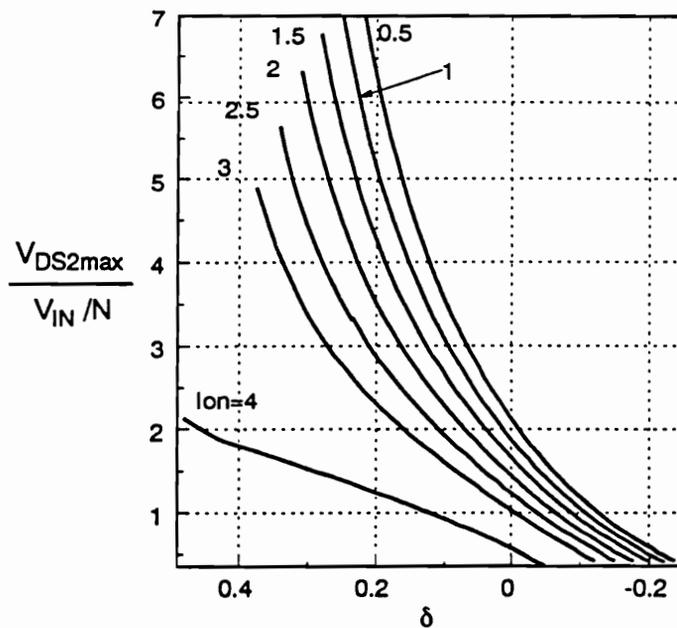
Figure A.9c. V_{DS2}^{max}/V_{IN} and $I_M/(I_O/N)$ characteristics of the CF forward ZVS-MRC $C_N = 3$ and f_S/f_O = 0.65. $C_N = C_D/(CN^2)$, $I_{ON} = I_O Z_O/V_{IN}$, $Z_O = \sqrt{L/C}$, and $f_O = 1/2\pi\sqrt{LC}$.
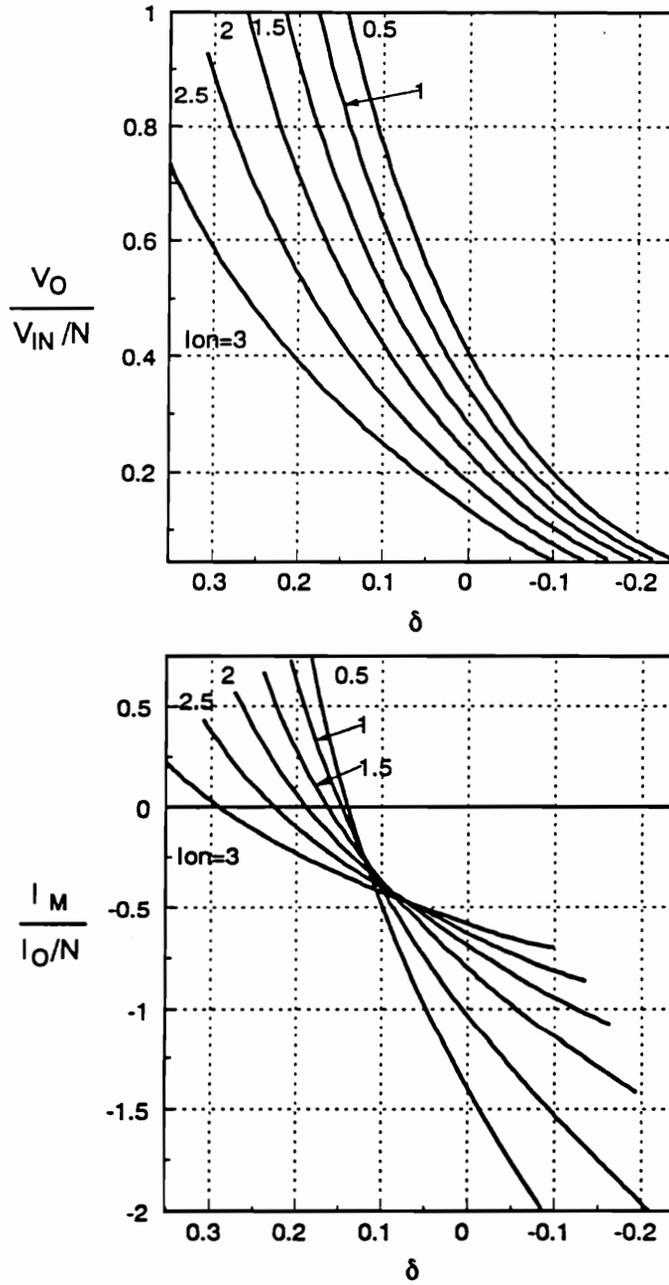
Figure A.10a. DC voltage conversion ratio and V_S^{max}/V_{IN} curves of the CF forward ZVS-MRC for $C_N = 3$ and $f_S/f_O = 0.70$. $C_N = C_D/(CN^2)$, $I_{ON} = I_O Z_O/V_{IN}$, $Z_O = \sqrt{L/C}$, and $f_O = 1/2\pi\sqrt{LC}$.
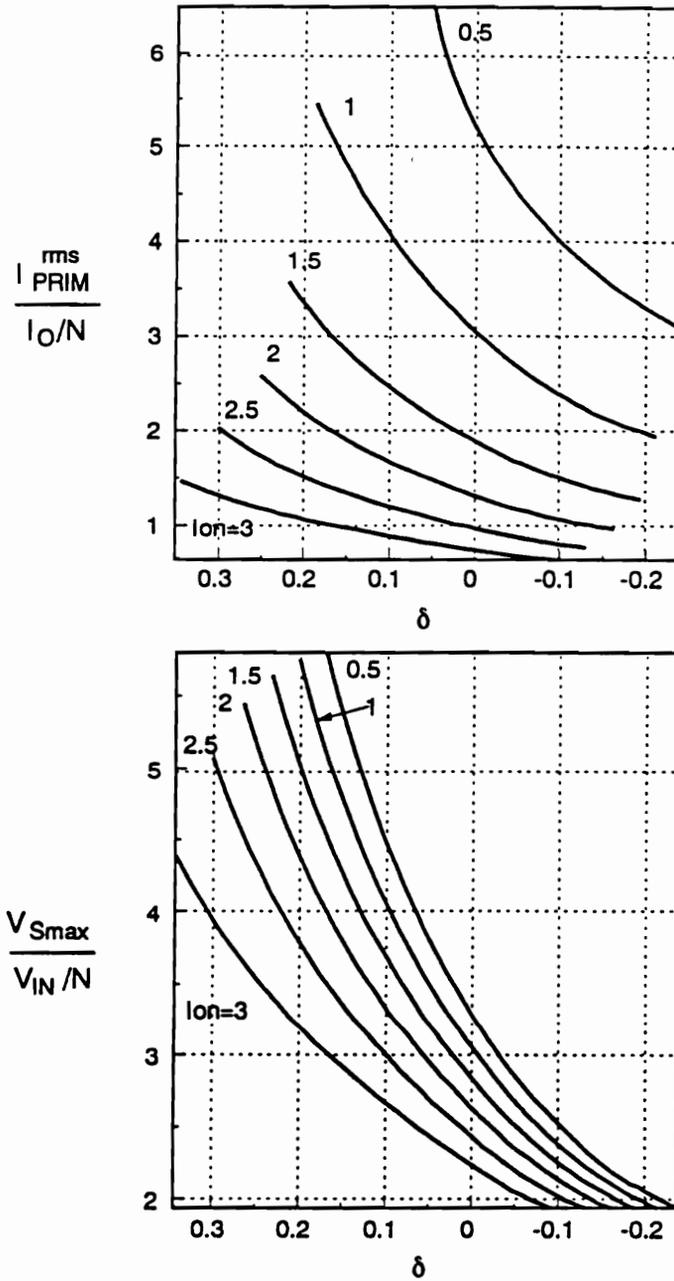
Figure A.10b. Normalized primary rms current and V_L^{p-p}/V_{IN} characteristics of the CF forward ZVS-MRC $C_N = 3$ and $f_S/f_O = 0.70$. $C_N = C_D/(CN^2)$, $I_{ON} = I_O Z_O/V_{IN}$, $Z_O = \sqrt{L/C}$, and $f_O = 1/2\pi\sqrt{LC}$.
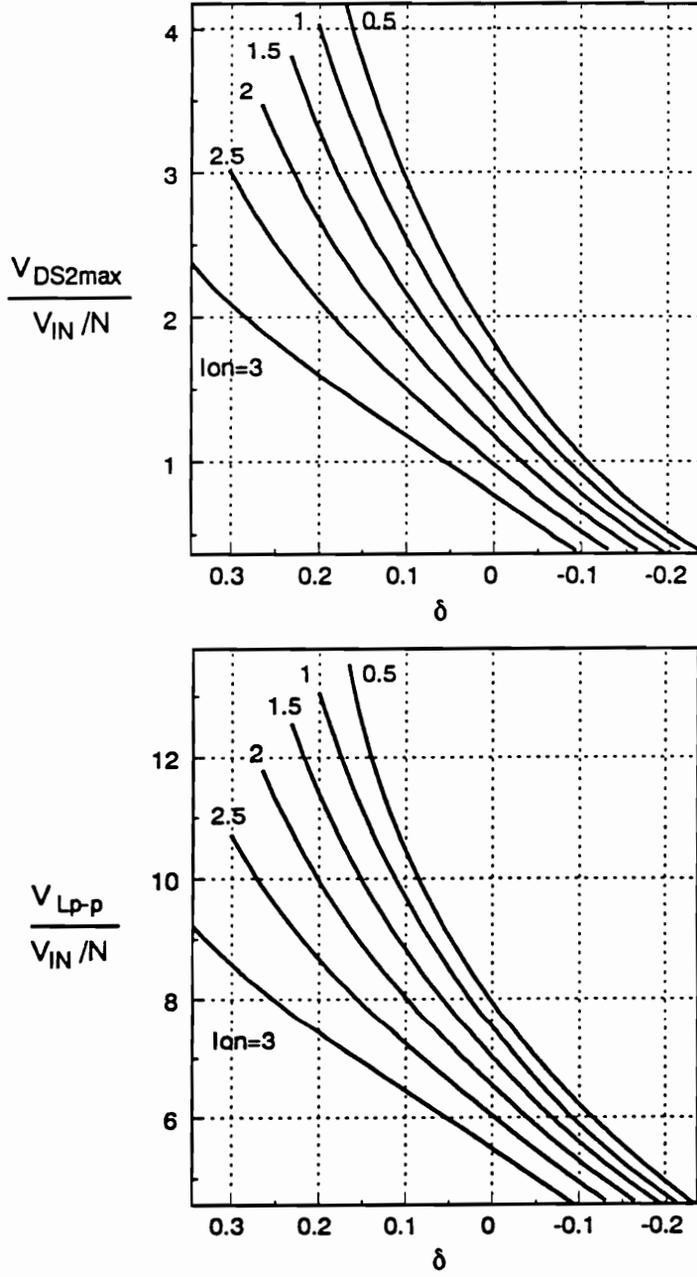
Figure A.10c. V_{DS2}^{max}/V_{IN} and $I_M/(I_O/N)$ characteristics of the CF forward ZVS-MRC $C_N = 3$ and $f_S/f_O = 0.70$. $C_N = C_D/(CN^2)$, $I_{ON} = I_O Z_O/V_{IN}$, $Z_O = \sqrt{L/C}$, and $f_O = 1/2\pi\sqrt{LC}$.
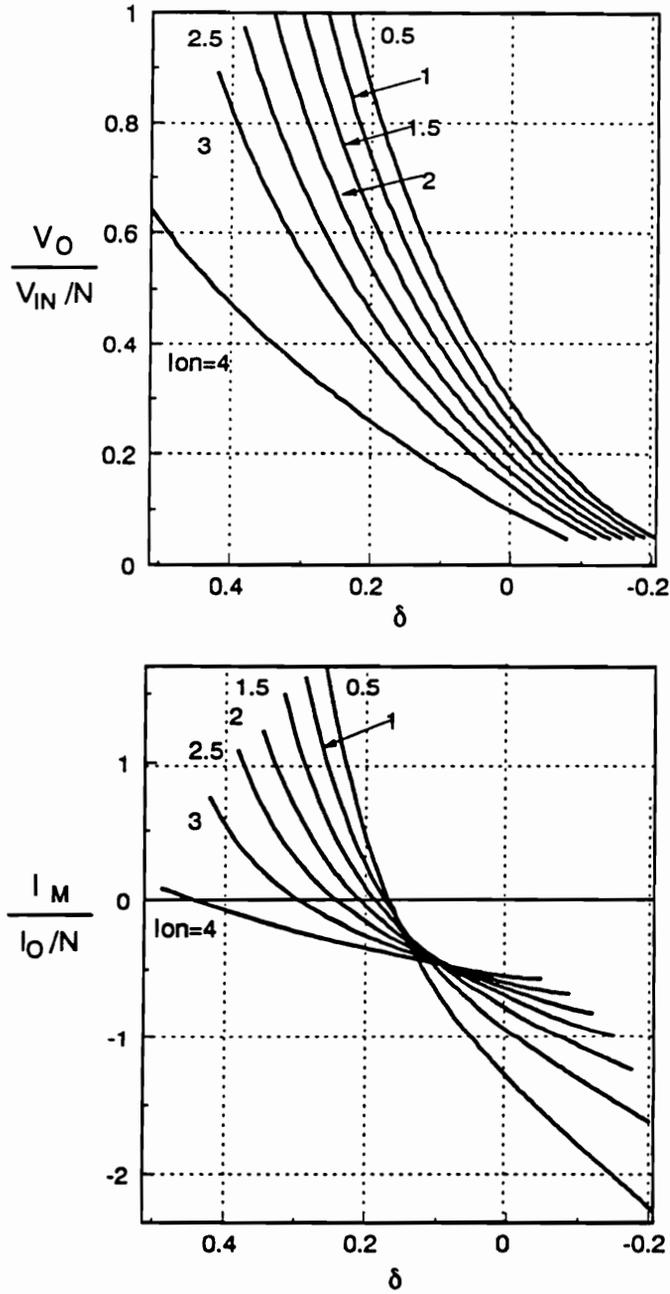
Figure A.11a. DC voltage conversion ratio and V_S^{max}/V_{IN} curves of the CF forward ZVS-MRC for $C_N = 5$ and $f_S/f_O = 0.55$. $C_N = C_D/(CN^2)$, $I_{ON} = I_O Z_O/V_{IN}$, $Z_O = \sqrt{L/C}$, and $f_O = 1/2\pi\sqrt{LC}$.
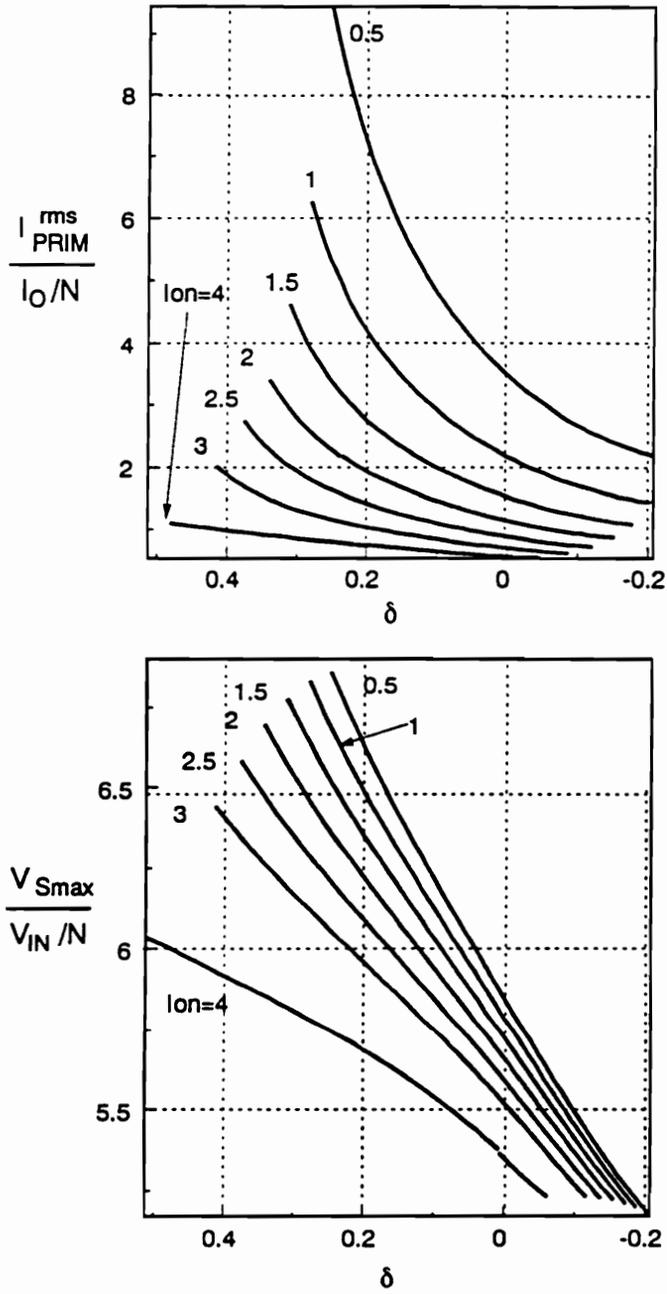
Figure A.11b. Normalized primary rms current and V_L^{p-p}/V_{IN} characteristics of the CF forward ZVS-MRC C_N = 5 and f_S/f_O = 0.55. $C_N = C_D/(CN^2)$, $I_{ON} = I_OZ_O/V_{IN}$, $Z_O = \sqrt{L/C}$, and $f_O = 1/2\pi\sqrt{LC}$.
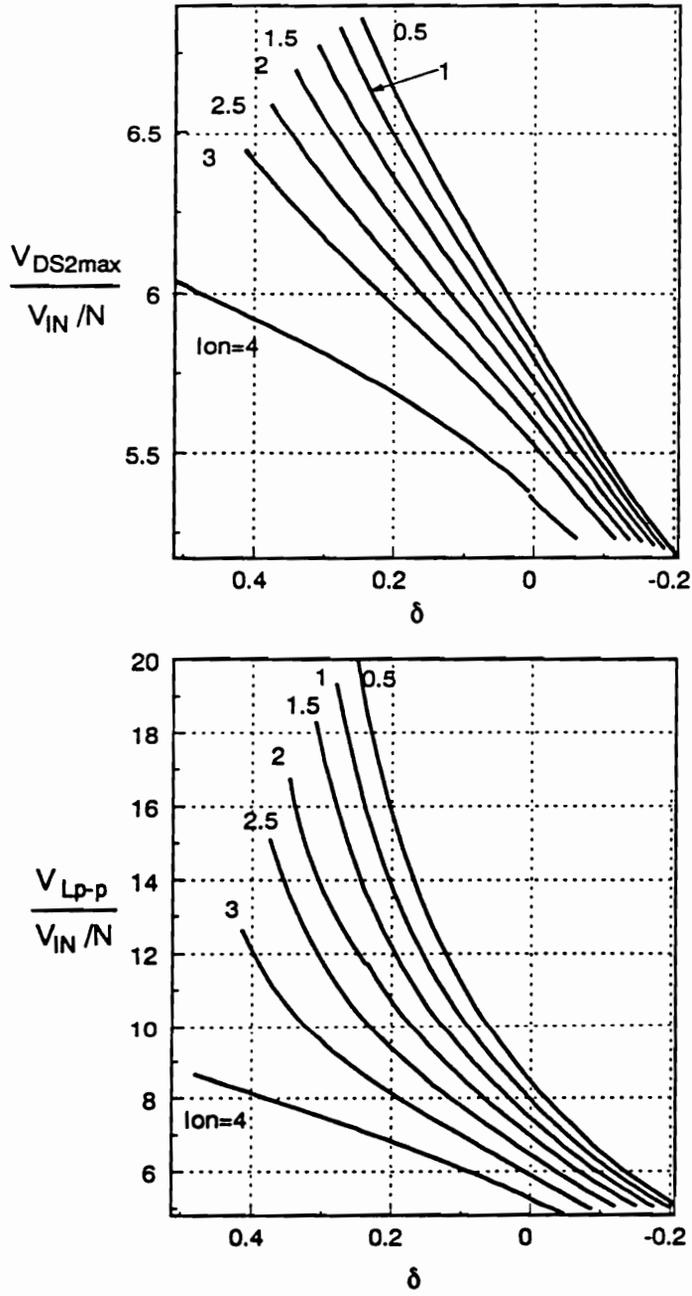
Figure A.11c. V_{DS2}^{max}/V_{IN} and $I_M/(I_O/N)$ characteristics of the CF forward ZVS-MRC $C_N = 5$ and $f_S/f_O = 0.55$. $C_N = C_D/(CN^2)$, $I_{ON} = I_O Z_O/V_{IN}$, $Z_O = \sqrt{L/C}$, and $f_O = 1/2\pi\sqrt{LC}$.
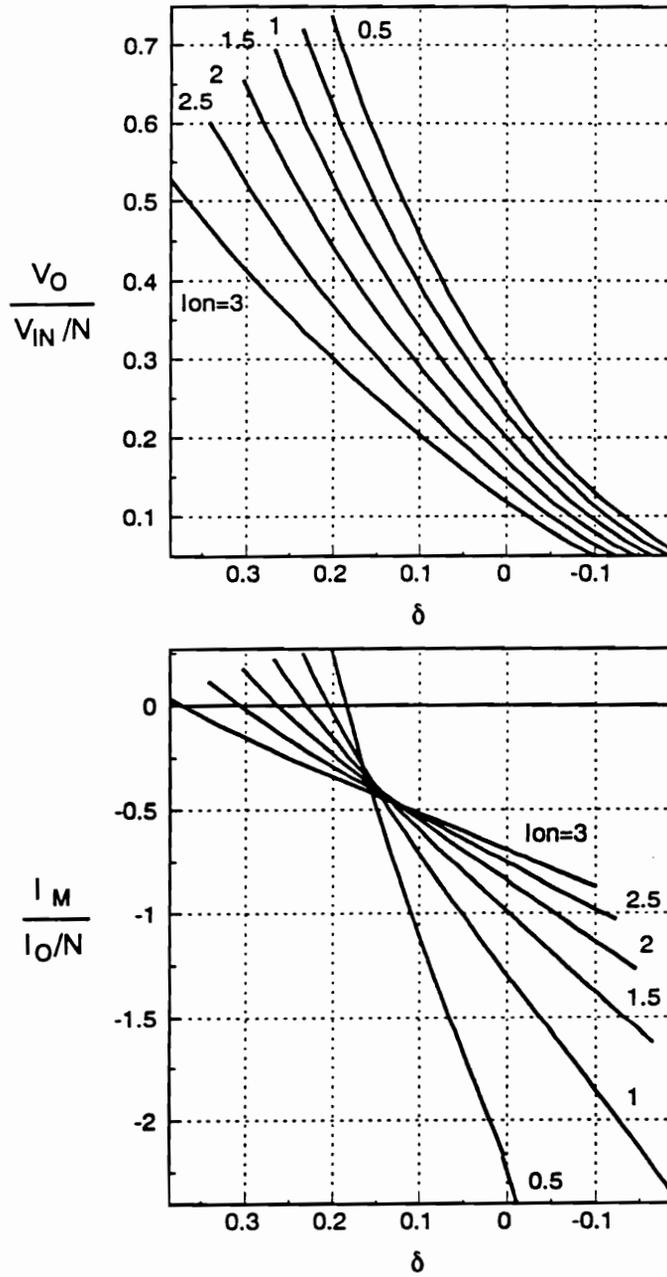
Figure A.12a. DC voltage conversion ratio and V_S^{max}/V_{IN} curves of the CF forward ZVS-MRC for $C_N = 5$ and $f_S/f_O = 0.60$. $C_N = C_D/(CN^2)$, $I_{ON} = I_O Z_O/V_{IN}$, $Z_O = \sqrt{L/C}$, and $f_O = 1/2\pi\sqrt{LC}$.
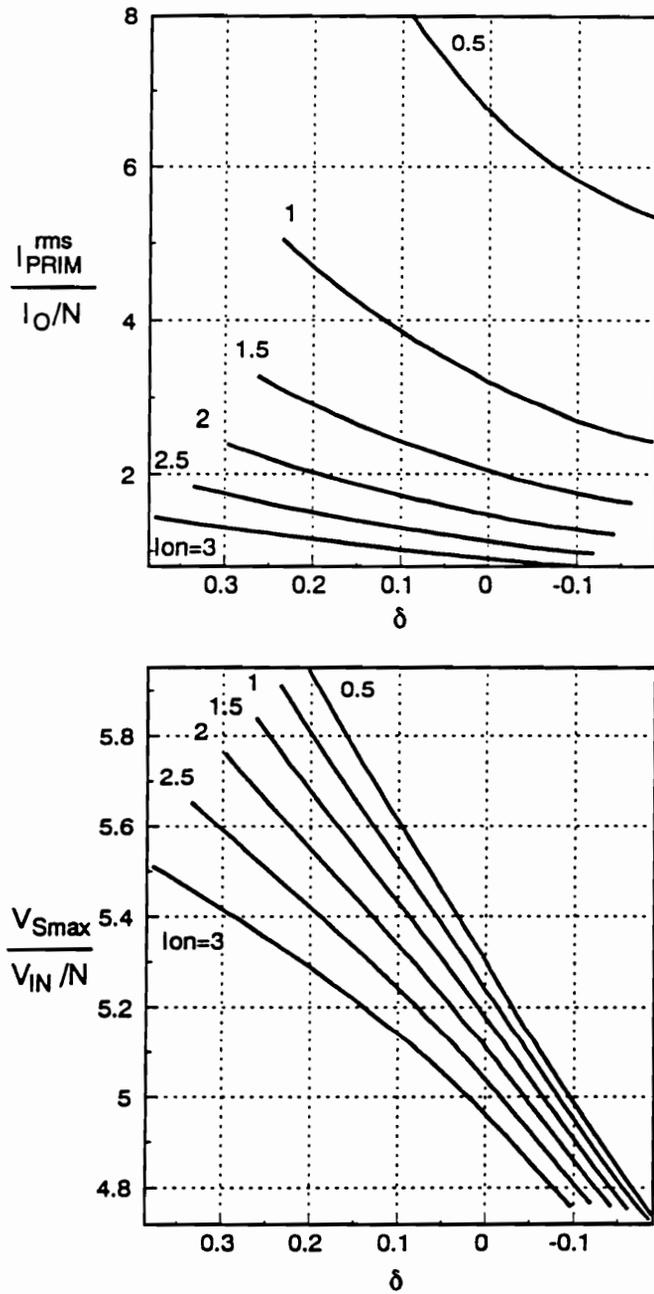
Figure A.12b. Normalized primary rms current and V_L^{p-p}/V_{IN} characteristics of the CF forward ZVS-MRC $C_N = 5$ and $f_S/f_O = 0.60$. $C_N = C_D/(CN^2)$, $I_{ON} = I_O Z_O/V_{IN}$, $Z_O = \sqrt{L/C}$, and $f_O = 1/2\pi\sqrt{LC}$.
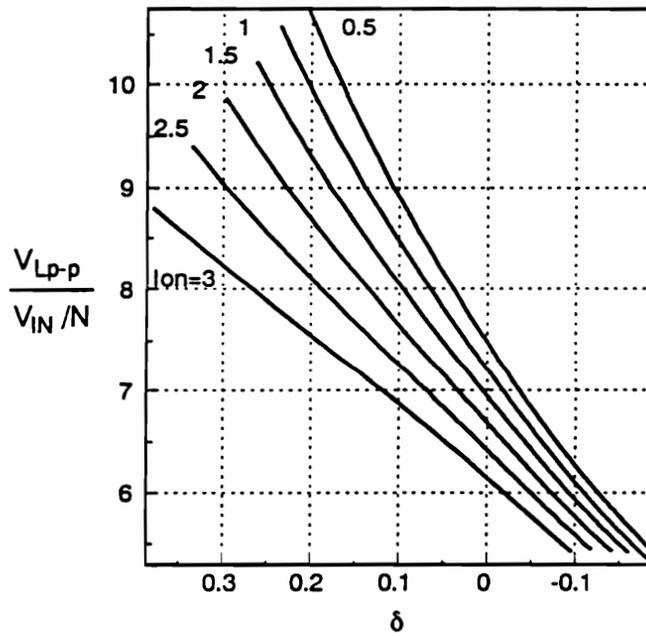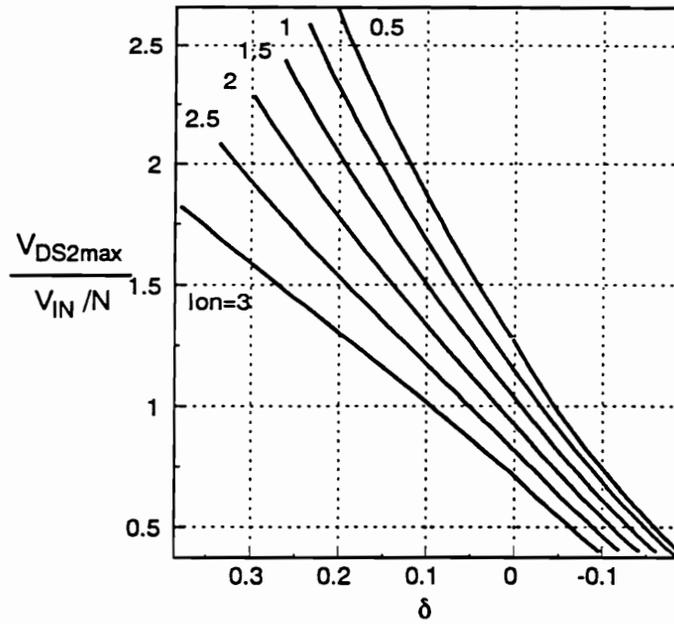
Figure A.12c. V_{DS2}^{max}/V_{IN} and $I_M/(I_O/N)$ characteristics of the CF forward ZVS-MRC $C_N = 5$ and $f_S/f_O = 0.60$. $C_N = C_D/(CN^2)$, $I_{ON} = I_O Z_O/V_{IN}$, $Z_O = \sqrt{L/C}$, and $f_O = 1/2\pi\sqrt{LC}$.
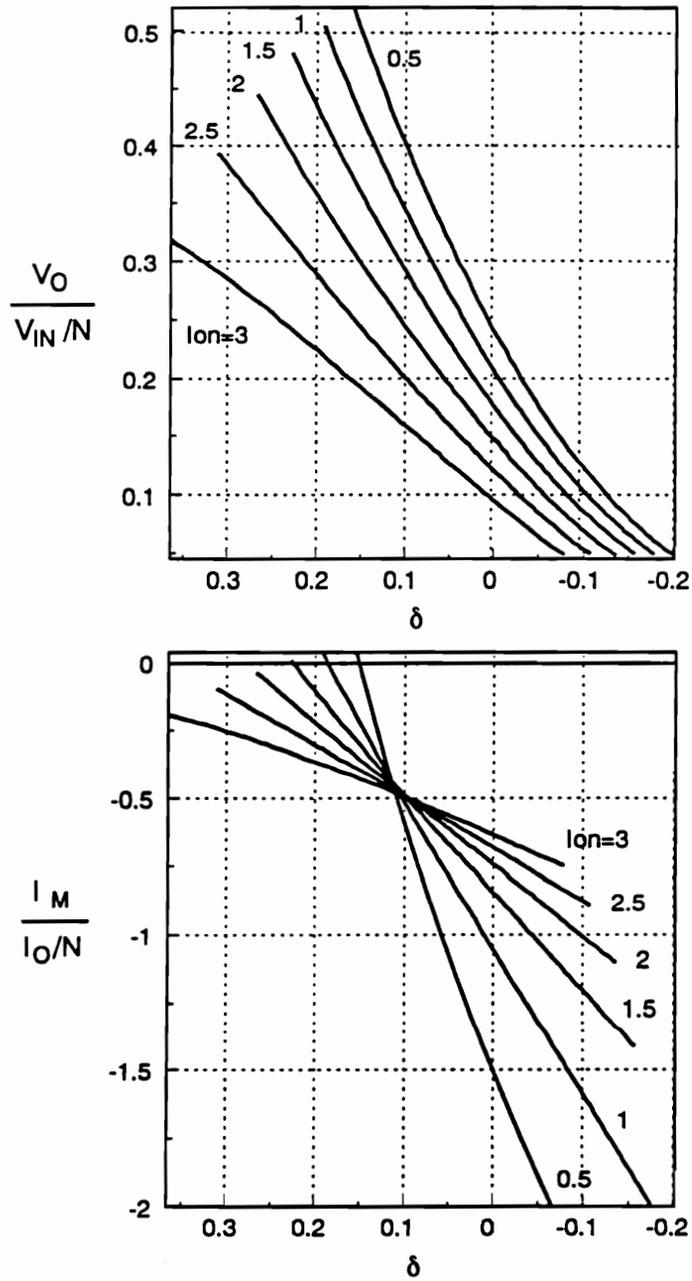
Figure A.13a. DC voltage conversion ratio and V_S^{max}/V_{IN} curves of the CF forward ZVS-MRC for $C_N = 5$ and $f_S/f_O = 0.65$. $C_N = C_D/(CN^2)$, $I_{ON} = I_O Z_O/V_{IN}$, $Z_O = \sqrt{L/C}$, and $f_O = 1/2\pi\sqrt{LC}$.
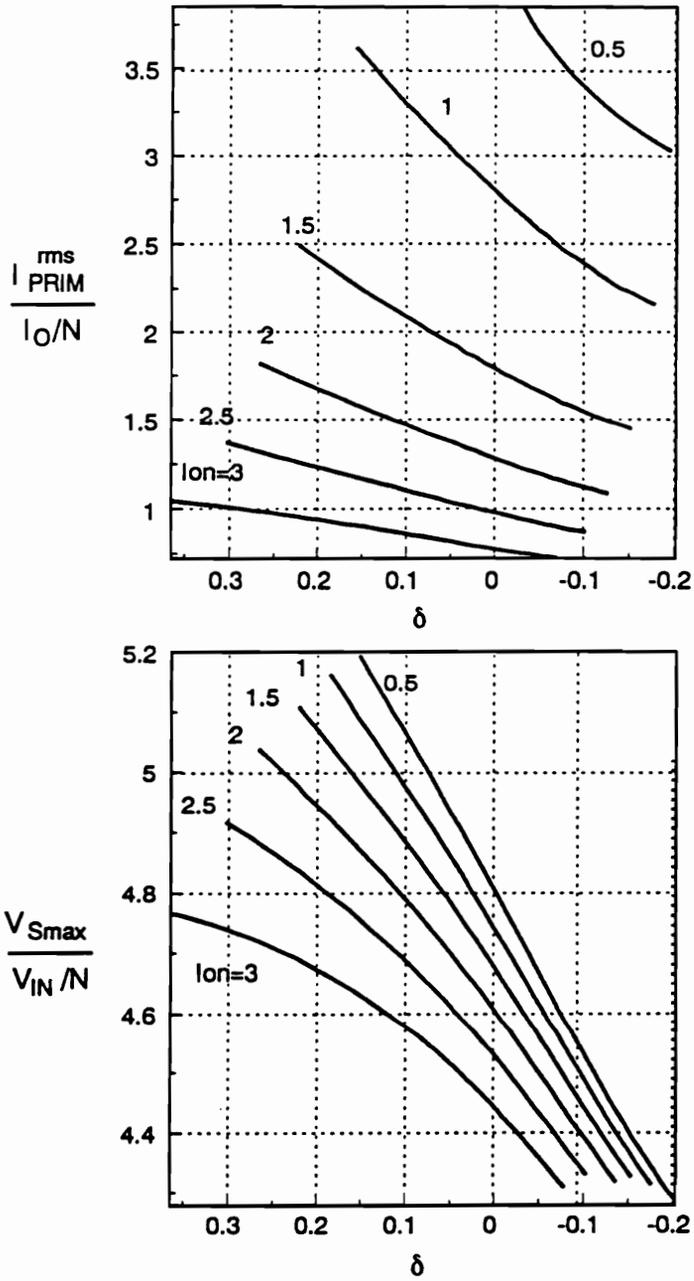
Figure A.13b. Normalized primary rms current and V_L^{p-p}/V_{IN} characteristics of the CF forward ZVS-MRC C_N = 5 and f_S/f_O = 0.65. $C_N = C_D/(CN^2)$, $I_{ON} = I_O Z_O/V_{IN}$, $Z_O = \sqrt{L/C}$, and $f_O = 1/2\pi\sqrt{LC}$.
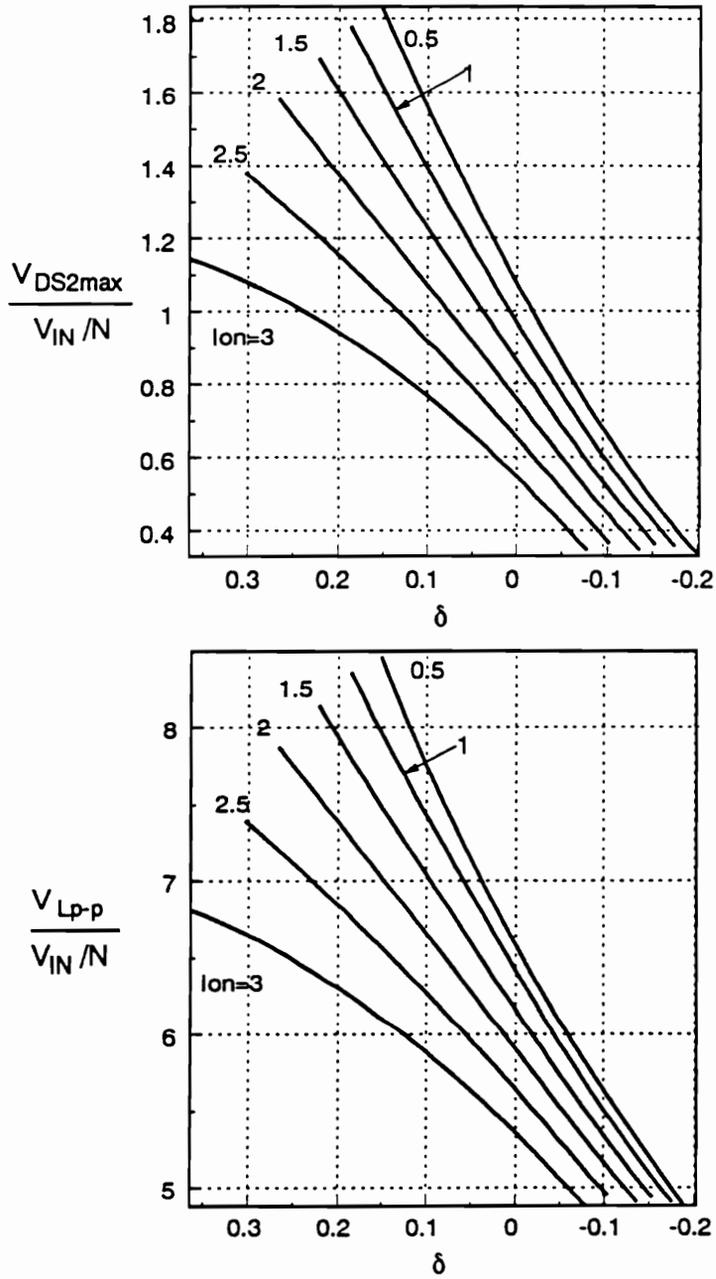
Figure A.13c. V_{DS2}^{max}/V_{IN} and $I_M/(I_O/N)$ characteristics of the CF forward ZVS-MRC $C_N = 5$ and $f_S/f_O = 0.65$. $C_N = C_D/(CN^2)$, $I_{ON} = I_O Z_O/V_{IN}$, $Z_O = \sqrt{L/C}$, and $f_O = 1/2\pi\sqrt{LC}$.
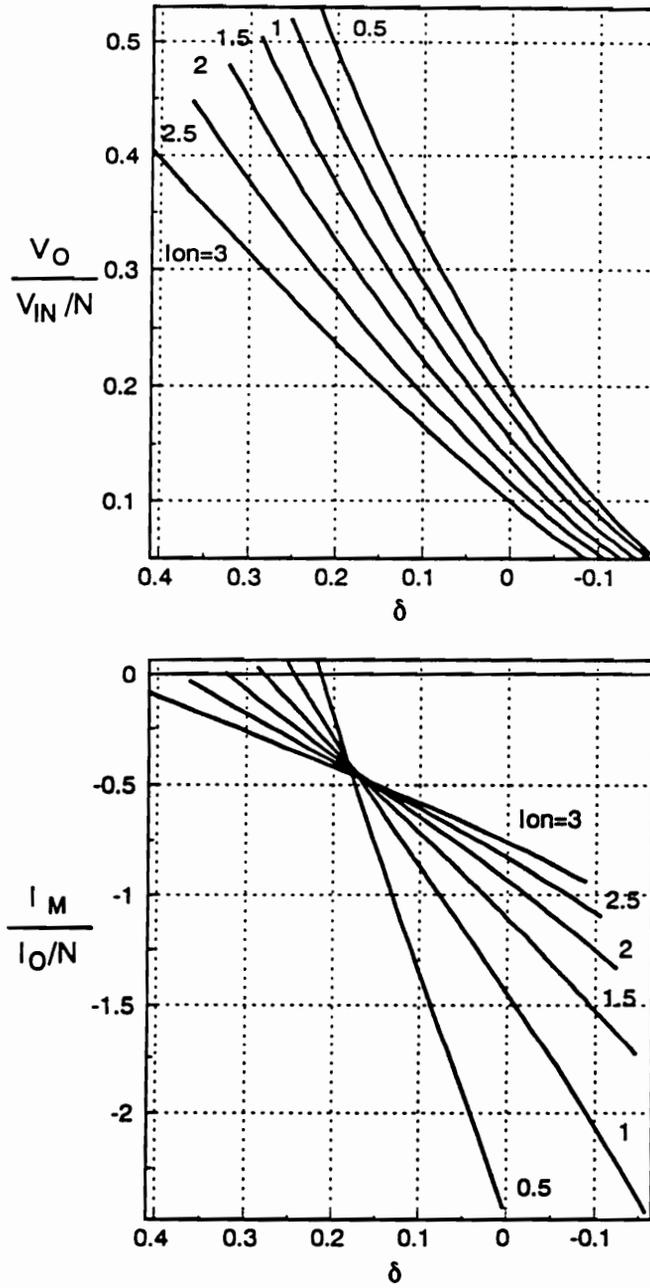
Figure A.14a. DC voltage conversion ratio and V_S^{max}/V_{IN} curves of the CF forward ZVS-MRC for $C_N = 7$ and $f_S/f_O = 0.55$. $C_N = C_D/(CN^2)$, $I_{ON} = I_OZ_O/V_{IN}$, $Z_O = \sqrt{L/C}$, and $f_O = 1/2\pi\sqrt{LC}$.
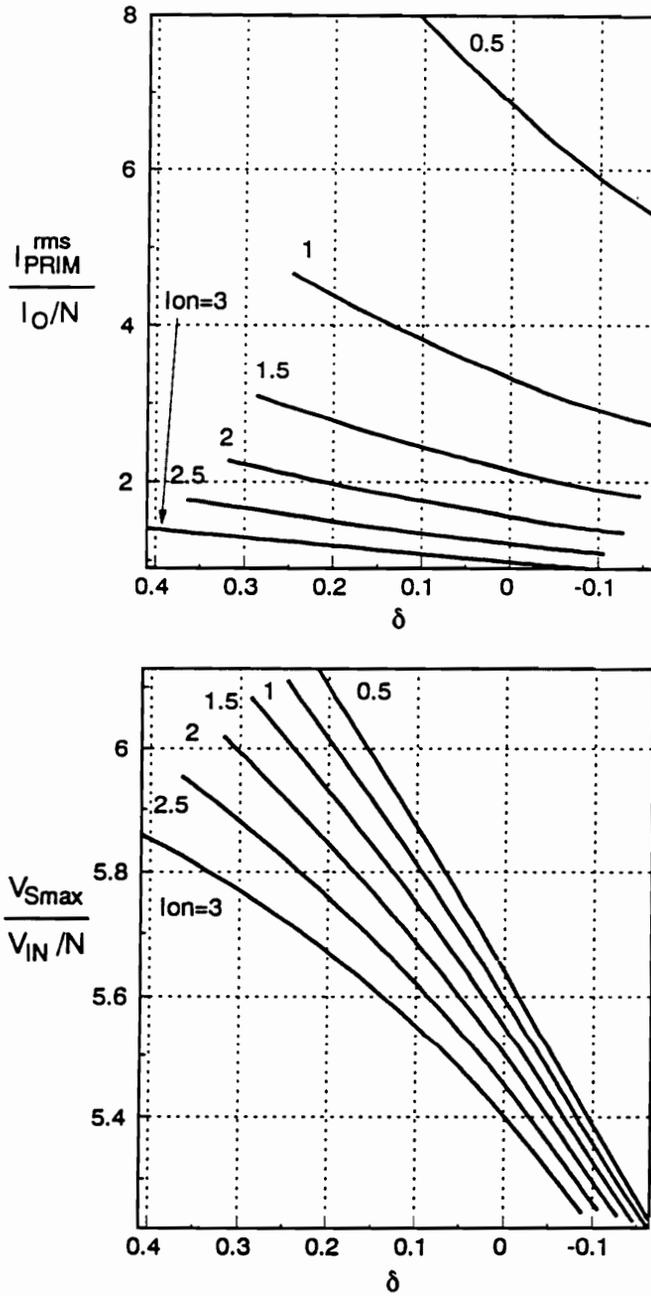
Figure A.14b. Normalized primary rms current and V_L^{p-p}/V_{IN} characteristics of the CF forward ZVS-MRC $C_N = 7$ and $f_S/f_O = 0.55$. $C_N = C_D/(CN^2)$, $I_{ON} = I_O Z_O/V_{IN}$, $Z_O = \sqrt{L/C}$, and $f_O = 1/2\pi\sqrt{LC}$.
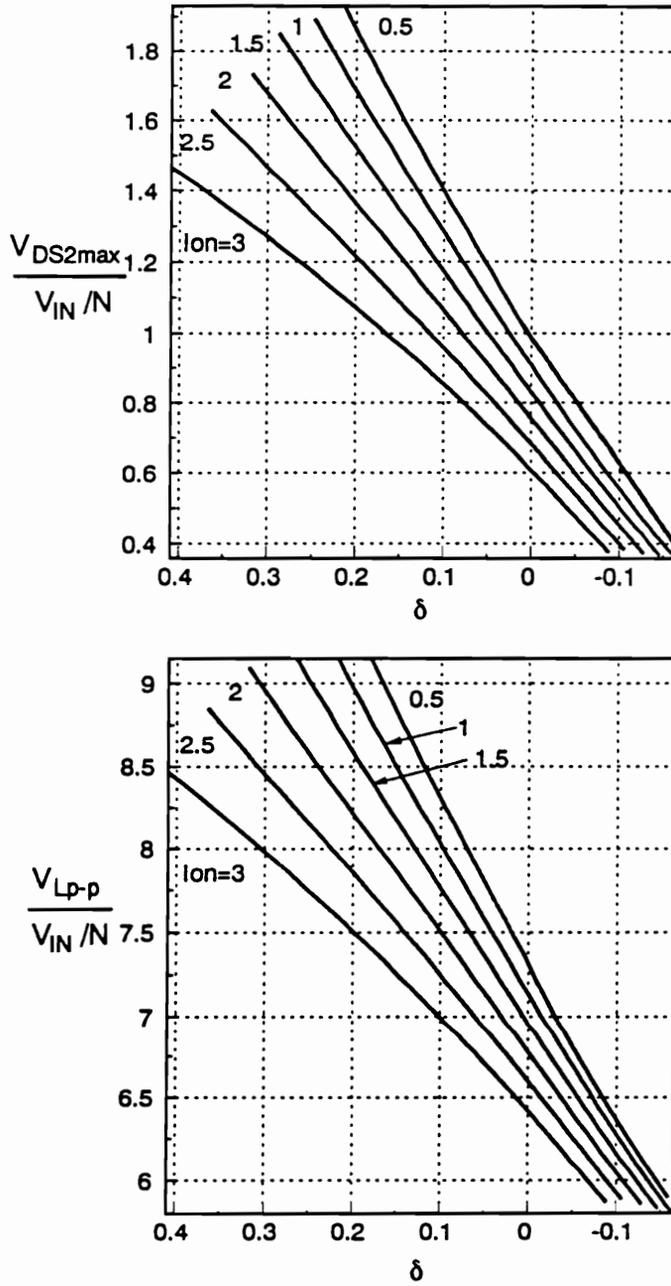
Figure A.14c. V_{DS2}^{max}/V_{IN} and $I_M/(I_O/N)$ characteristics of the CF forward ZVS-MRC $C_N = 7$ and $f_S/f_O = 0.55$. $C_N = C_D/(CN^2)$, $I_{ON} = I_O Z_O/V_{IN}$, $Z_O = \sqrt{L/C}$, and $f_O = 1/2\pi\sqrt{LC}$.
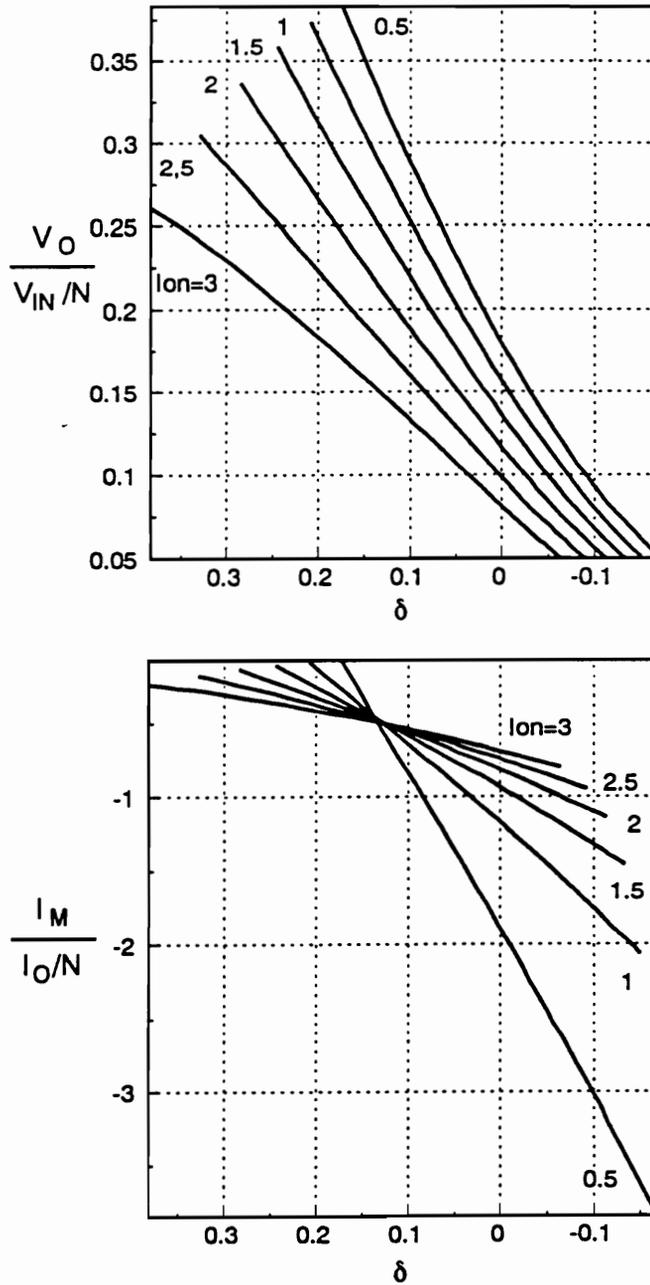
Figure A.15a. DC voltage conversion ratio and V_S^{max}/V_{IN} curves of the CF forward ZVS-MRC for $C_N = 7$ and $f_S/f_0 = 0.60$. $C_N = C_D/(CN^2)$, $I_{ON} = I_0 Z_0/V_{IN}$, $Z_0 = \sqrt{L/C}$, and $f_0 = 1/2\pi\sqrt{LC}$.
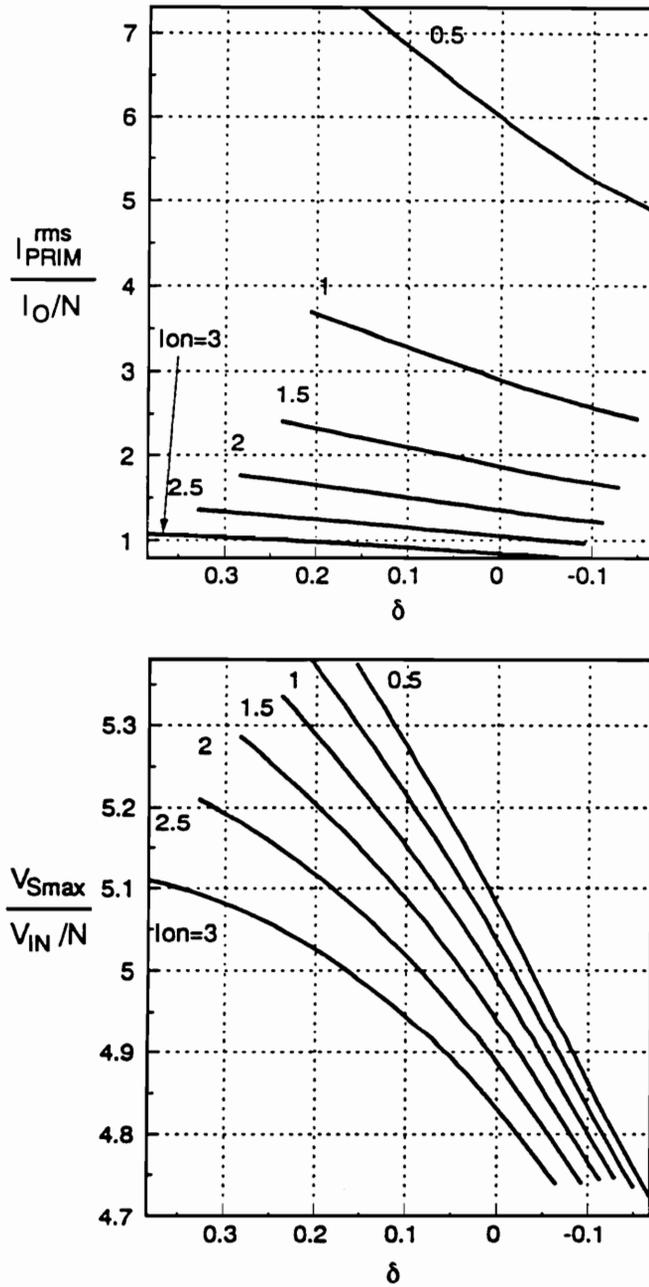
Figure A.15b. Normalized primary rms current and V_L^{p-p}/V_{IN} characteristics of the CF forward ZVS-MRC. $C_N = 7$ and $f_S/f_0 = 0.60$. $C_N = C_D/(CN^2)$, $I_{ON} = I_0 Z_0/V_{IN}$, $Z_0 = \sqrt{L/C}$, and $f_0 = 1/2\pi\sqrt{LC}$.

Figure A.15c. V_{DS2}^{max}/V_{IN} and $I_M/(I_O/N)$ characteristics of the CF forward ZVS-MRC $C_N = 7$ and $f_S/f_O = 0.60$. $C_N = C_D/(CN^2)$, $I_{ON} = I_O Z_O/V_{IN}$, $Z_O = \sqrt{L/C}$, and $f_O = 1/2\pi\sqrt{LC}$.
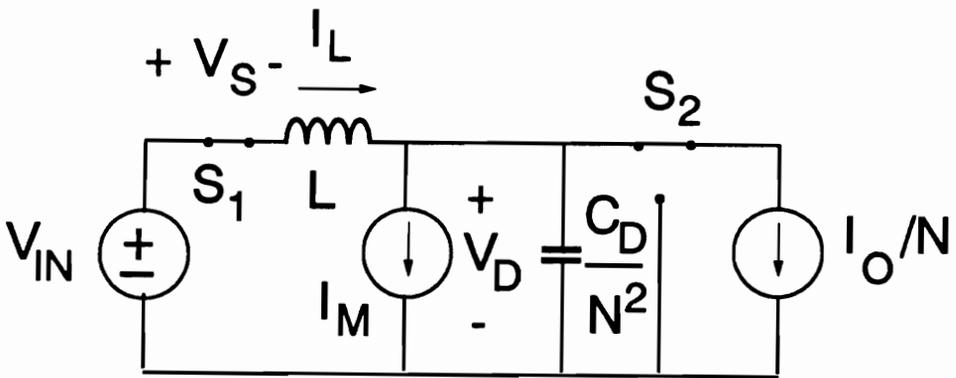
Figure A.16. Topological Stage A of ideal CF forward ZVS-MRC.

From Eqs. (A.1.a) - (A.2.b), it follows that:

$$\frac{d^2 v_D(t)}{dt^2} + \frac{N^2}{LC_D} v_D(t) = \frac{N^2}{LC_D} V_{IN} \qquad (A.3.a)$$

where the following parameters are defined as:

$$\omega_O = \frac{1}{\sqrt{LC_S}} \qquad (A.3.b)$$

$$C_N = \frac{C_D}{C_S N^2} \qquad (A.3.c)$$

$$Z_O = \sqrt{\frac{L}{C_S}} \qquad (A.3.d)$$

$$Z_D = \sqrt{\frac{L}{C_D/N^2}} \qquad (A.3.e)$$

and

$$K = \sqrt{\frac{C_S N^2}{C_D}} \qquad (A.3.f)$$

It should be noted that $C_D/(N)^2$ represents the capacitance of the CF switch and the free-wheeling diode reflected into the primary. Therefore, C_N is the ratio between the total reflected secondary side capacitance and the primary switch capacitance C_S.

Solution:

$$v_D^A = a_A \cos \omega_O Kt + b_A \sin \omega_O Kt + V_{IN} \qquad (A.4.a)$$

$$i_L^A = b_A \omega_O K \frac{C_D}{N^2} \cos \omega_O Kt - a_A \omega_O K \frac{C_D}{N^2} \sin \omega_O Kt + I_O + I_M \qquad (A.4.b)$$

where

$$a_A = V_D^A - V_{IN} \qquad (A.5.a)$$

$$b_A = Z_D(I_L^A - I_O - I_M) \qquad (A.5.b)$$

Initial conditions I_L^A and V_D^A are determined from Stages C (Eq. (A.17)) and E (Eqs. (A.29a) and (A.29.b)) which preceede Stage A.

Voltages are normalized with respect to V_{IN}, currents with respect to I_O/N, and time with respect to $1/f_O$ ($f_O = \omega_O/2\pi$); Eqs. (A.4.a) and (A.4.b) then respectively become:

$$v_D^{AN} = (V_D^{AN} - 1) \cos 2\pi Kt_N + K[I_L^{AN} - I_{MN} - 1]I_{ON} \sin 2\pi Kt_N + 1 \qquad (A.6.a)$$

$$i_L^{AN} = 1 + I_{MN} + [I_L^{AN} - I_{MN} - 1] \cos 2\pi Kt_N - \frac{[V_D^{AN} - 1]}{KI_{ON}} \sin 2\pi Kt_N \qquad (A.6.b)$$

Stage Duration $T_A = T_{A1} - T_{AO}$

The stage duration T_A is determined from the following condition if the next stage is Stage B:

$$v_D(T_A) = 0 \qquad\qquad (A.7)$$

but if the next stage is Stage E, then stage duration T_A is determined from the turn-off of the primary switch capacitance. In both cases, it is necessary to solve a transcendental equation to determine the stage duration.

STAGE B $[T_{BO}, T_{B1}]$ (Fig. A.17)

Initial Conditions:

$$v_S(T_{BO}) = 0 \qquad\qquad (A.8.a)$$

$$v_D(T_{BO}) = V_D^B \qquad\qquad (A.8.b)$$

$$i_L(T_{BO}) = I_L^B \qquad\qquad (A.8.c)$$

Equations:
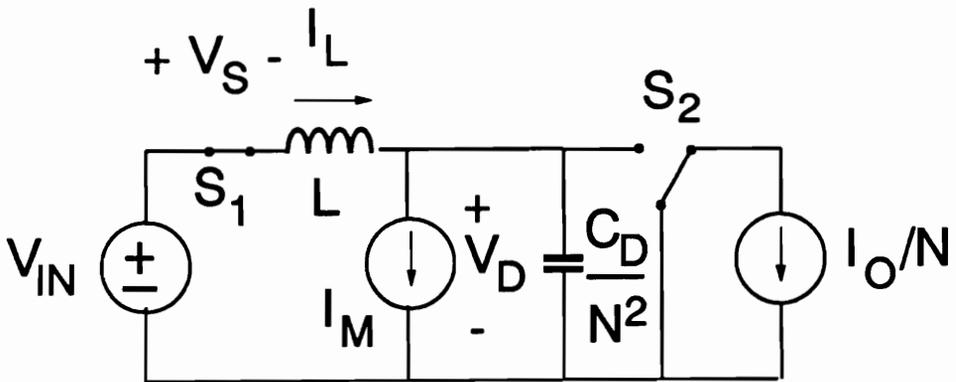
Figure A.17. Topological Stage B of ideal CF forward ZVS-MRC.

$$L \frac{di_L(t)}{dt} + v_D(t) = V_{IN} \qquad (A.9.a)$$

$$i_L(t) - C_D \frac{dv_D(t)}{dt} = I_O \qquad (A.9.b)$$

From Eqs. (A.9.a) and (A.9.b), it follows that:

$$\frac{d^2 v_D(t)}{dt^2} + \frac{N^2}{LC_D} v_D(t) = \frac{N^2}{LC_D} V_{IN} \qquad (A.10.a)$$

Solution:

$$v_D^B = a_B \cos \omega_O Kt + b_B \sin \omega_O Kt + V_{IN} \qquad (A.11.a)$$

$$i_L^B = b_B \omega_O K \frac{C_D}{N^2} \cos \omega_O Kt - a_B \omega_O K \frac{C_D}{N^2} \sin \omega_O Kt + I_M \qquad (A.11.b)$$

where

$$a_B = V_D^B - V_{IN} \qquad (A.12.a)$$

$$b_B = Z_D(I_L^B - I_M) \qquad (A.12.b)$$

or in the normalized form:

$$v_D^{BN} = (V_D^{BN} - 1) \cos 2\pi K t_N + K[I_L^{BN} - I_{MN}]I_{ON} \sin 2\pi K t_N + 1 \qquad (A.13.a)$$

$$i_L^{BN} = I_{MN} + [I_L^{BN} - I_{MN}] \cos 2\pi K t_N - \frac{[V_D^{BN} - 1]}{K I_{ON}} \sin 2\pi K t_N \qquad (A.13.b)$$

Stage Duration $T_B = T_{B1} - T_{BO}$

The stage duration T_B is determined from the following condition:

$$v_D(T_B) = 0 \qquad (A.14)$$

STAGE C [T_{CO}, T_{C1}] (Fig. A.18)

Initial Conditions:

$$v_S(T_{CO}) = 0 \qquad (A.15.a)$$

$$v_D(T_{CO}) = 0 \qquad (A.15.b)$$

$$i_L(T_{CO}) = I_L^C \qquad (A.15.c)$$

Equations:
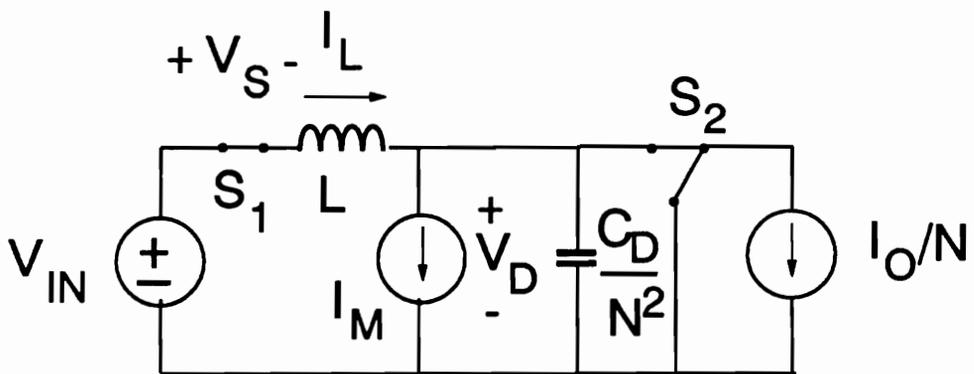
Figure A.18. Topological Stage C of ideal CF forward ZVS-MRC.

$$L \frac{di_L(t)}{dt} = V_{IN} \tag{A.16}$$

Solution:

$$i_L^C = I_L^C + \frac{V_{IN}}{L} t \tag{A.17}$$

or in the normalized form:

$$i_L^{CN} = I_L^{CN} + 2\pi t_N \tag{A.18}$$

Stage Duration $T_C = T_{C1} - T_{CO}$

The stage duration T_C is determined from the turn-off of the CF switch Q_2.

STAGE D [T_{DO}, T_{D1}] (Fig. A.19)

Initial Conditions:

$$v_S(T_{DO}) = V_S^D \tag{A.19.a}$$
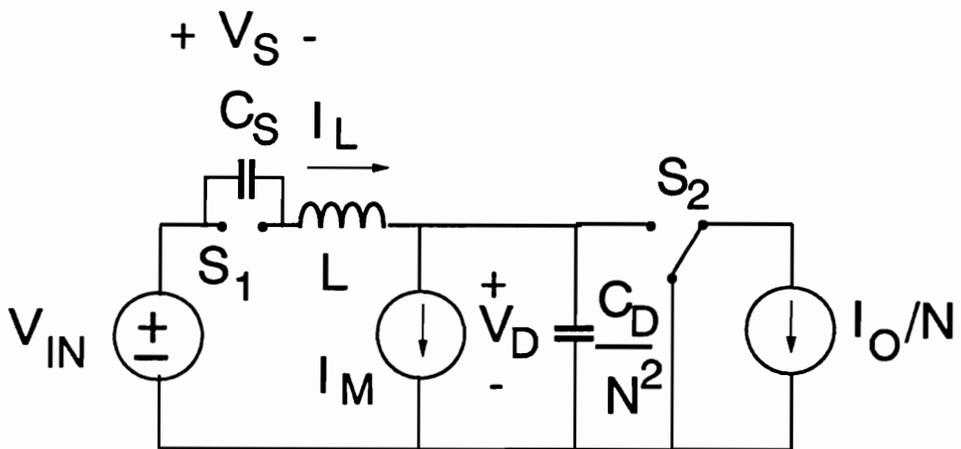
Figure A.19. Topological Stage D of ideal CF forward ZVS-MRC.

$$v_D(T_{DO}) = V_D^D \qquad (A.19.b)$$

$$i_L(T_{DO}) = I_L^D \qquad (A.19.c)$$

Equations:

$$L\frac{di_L(t)}{dt} + v_D(t) + v_S(t) = V_{IN} \qquad (A.20.a)$$

$$i_L(t) - C_D\frac{dv_D(t)}{dt} = I_O + I_M \qquad (A.20.b)$$

$$i_L(t) = i_{CD}(t) = C_D\frac{dv_S(t)}{dt} \qquad (A.20.c)$$

From Eqs. (A.20.a) - (A.20.c), it follows that:

$$\frac{d^3v_S(t)}{dt^3} + K_2\omega_O^2\,\frac{dv_S(t)}{dt} = \frac{I_O + I_M}{C_D/N^2}\,\omega_O^2 \qquad (A.21.a)$$

where

$$K_2 = \frac{1 + C_N}{C_N} \qquad (A.21.b)$$

Solution:

$$v_D^D = V_{IN} + C_N^{-1} a_D \cos \omega_O K_2^{1/2} t + C_N^{-1} b_D \sin \omega_O K_2^{1/2} t - c_D - d_D t \qquad (A.22.a)$$

$$i_L^D = b_D C_S \omega_O K_2^{1/2} \cos \omega_2 K_2^{1/2} t - a_D C_S \omega_O K_2^{1/2} \sin \omega_2 K_2^{1/2} t + d_D C_S \qquad (A.22.b)$$

$$v_S^D = a_D \cos \omega_O K_2^{1/2} t + b_D \sin \omega_O K_2^{1/2} t + c_D + d_D t \qquad (A.22.c)$$

where

$$a_D = \frac{V_D^D - V_{IN} + V_S^D}{K_2} \qquad (A.23.a)$$

$$b_D = \frac{i_L^D - \dfrac{I_O + I_M}{1 + C_N}}{K_2^{1/2} \omega_O} \qquad (A.23.b)$$

$$c_D = V_S^D - \frac{V_D^D - V_{IN} + V_S^D}{K_2} \qquad (A.23.c)$$

$$d_D = \frac{I_O + I_M}{1 + C_N} \qquad (A.23.d)$$

or in the normalized form:

$$v_D^{DN} = (1 + \frac{V_D^{DN} - 1}{1 + C_N}) \cos 2\pi K_2^{1/2} t_N + (i_L^{DN} I_{ON} - \frac{I_{ON}(1 + I_{MN})}{1 + C_N}) \sin 2\pi K_2^{1/2} t_N$$

$$+ \frac{C_N}{1 + C_N} (V_D^{DN} - 1) + \frac{I_{ON}(1 + I_{MN})2\pi t_N}{1 + C_N} \qquad (A.24.a)$$

$$i_L^{DN} = [I_L^{DN} - \frac{1 + I_{MN}}{1 + C_N}] \cos 2\pi K_2^{1/2} t_N + \frac{[V_D^{DN} - 1]}{I_{ON}K_2^{1/2}} \sin 2\pi K_2^{1/2} t_N$$

$$+ \frac{I_{ON}(1 + I_{MN})}{1 + C_N} \qquad (A.24.b)$$

$$v_S^{DN} = \frac{V_D^{DN} - 1}{K_2} (\cos 2\pi K_2^{1/2} t_N - 1) + \frac{[I_L^{DN} I_{ON} - \frac{I_{ON}(1 + I_{MN})}{1 + C_N}]}{C_N K_2^{1/2}} \sin 2\pi K_2^{1/2} t_N$$

$$+ \frac{I_{ON}(1 + I_{MN})2\pi t_N}{1 + C_N} \qquad (A.24.c)$$

Stage Duration $T_D = T_{D1} - T_{DO}$

The stage duration T_D is determined from the following condition if the stage following is Stage B:

$$v_S(T_D) = 0 \qquad (A.25.a)$$

and by

$$v_D(T_D) = 0 \qquad (A.25.b)$$

if the following stage is Stage E.

STAGE E [T_{EO}, T_{E1}] (Fig. A.20)

Initial Conditions:

$$v_S(T_{EO}) = V_{S1}^E \qquad (A.26.a)$$

$$v_D(T_{EO}) = V_D^E \qquad (A.26.b)$$

$$i_L(T_{EO}) = I_L^E \qquad (A.26.c)$$

Equations:

$$L\frac{di_L(t)}{dt} + v_D(t) + v_S(t) = V_{IN} \qquad (A.27.a)$$

$$i_L(t) - C_D\frac{dv_D(t)}{dt} = I_M \qquad (A.27.b)$$

$$i_L(t) = i_{CD}(t) = C_D\frac{dv_S(t)}{dt} \qquad (A.27.c)$$

From Eqs. (A.27.a) - (A.27.c), it follows that:
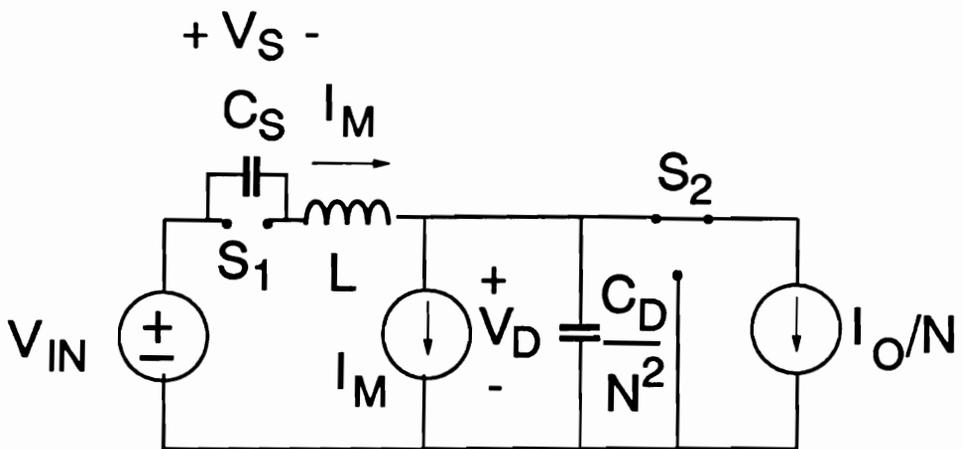
Figure A.20.   Topological Stage E of ideal CF forward ZVS-MRC.

$$\frac{d^3 v_S(t)}{dt^3} + K_2 \omega_O^2 \frac{dv_S(t)}{dt} = \frac{I_M}{C_D/N^2} \omega_O^2 \qquad (A.28)$$

Solution:

$$v_D^E = V_{IN} + C_N^{-1} a_E \cos \omega_O K_2^{1/2} t + C_N^{-1} b_E \sin \omega_O K_2^{1/2} t - c_E - d_E t \qquad (A.29.a)$$

$$i_L^E = b_E C_S \omega_O K_2^{1/2} \cos \omega_2 K_2^{1/2} t - a_E C_S \omega_O K_2^{1/2} \sin \omega_2 K_2^{1/2} t + d_E C_S \qquad (A.29.b)$$

$$v_S^E = a_E \cos \omega_O K_2^{1/2} t + b_E \sin \omega_O K_2^{1/2} t + c_E + d_E t \qquad (A.29.c)$$

where

$$a_E = \frac{V_D^E - V_{IN} + V_S^E}{K_2} \qquad (A.30.a)$$

$$b_E = \frac{i_L^E - \dfrac{I_M}{1 + C_N}}{K_2^{1/2} \omega_O} \qquad (A.30.b)$$

$$c_E = V_S^E - \frac{V_D^E - V_{IN} + V_S^E}{K_2} \qquad (A.30.c)$$

$$d_E = \frac{I_M}{1 + C_N} \qquad (A.30.d)$$

or in the normalized form:

$$v_D^{EN} = (1 + \frac{V_D^{EN} - 1}{1 + C_N}) \cos 2\pi K_2^{1/2} t_N + (I_L^{EN} - \frac{I_{MN}}{1 + C_N}) I_{ON} \sin 2\pi K_2^{1/2} t_N$$

$$+ \frac{C_N(V_D^{EN} - 1)}{1 + C_N} + \frac{I_{ON}I_{MN}2\pi t_N}{1 + C_N} \qquad (A.31.a)$$

$$i_L^{EN} = [I_L^{EN} - \frac{I_{MN}}{1 + C_N}] \cos 2\pi K_2^{1/2} t_N + \frac{[V_D^{EN} - 1]}{I_{ON}K_2^{1/2}} \sin 2\pi K_2^{1/2} t_N$$

$$+ \frac{I_{MN}}{1 + C_N} \qquad (A.31.b)$$

$$v_S^{EN} = \frac{(V_D^{EN} - 1)}{K_2} (\cos 2\pi K_2^{1/2} t_N - 1) + \frac{I_{ON}[I_L^{EN} - \frac{I_{MN}}{1 + C_N}]}{C_N K_2^{1/2}} \sin 2\pi K_2^{1/2} t_N$$

$$+ \frac{I_{ON}I_{MN}2\pi t_N}{1 + C_N} \qquad (A.31.c)$$

Stage Duration $T_E = T_{E1} - T_{EO}$

The stage duration T_E is determined from the following condition if the stage following is Stage A:

$$v_S(T_F) = 0 \qquad (A.32.a)$$

and by

$$v_D(T_E) = 0 \qquad (A.32.b)$$

if the following stage is Stage D.

STAGE F [T_{FO}, T_{F1}] (Fig. A.21)

Initial Conditions:

$$v_S(T_{FO}) = V_S^F \qquad (A.33.a)$$

$$v_D(T_{FO}) = 0 \qquad (A.33.b)$$

$$i_L(T_{FO}) = I_L^F \qquad (A.33.c)$$

Equations:

$$L\frac{di_L(t)}{dt} + v_S(t) = V_{IN} \qquad (A.34.a)$$

$$i_L(t) = i_{CS}(t) = C_S\frac{dv_S(t)}{dt} \qquad (A.34.b)$$

From Eqs. (A.34.a) and (A.34.b), it follows that:
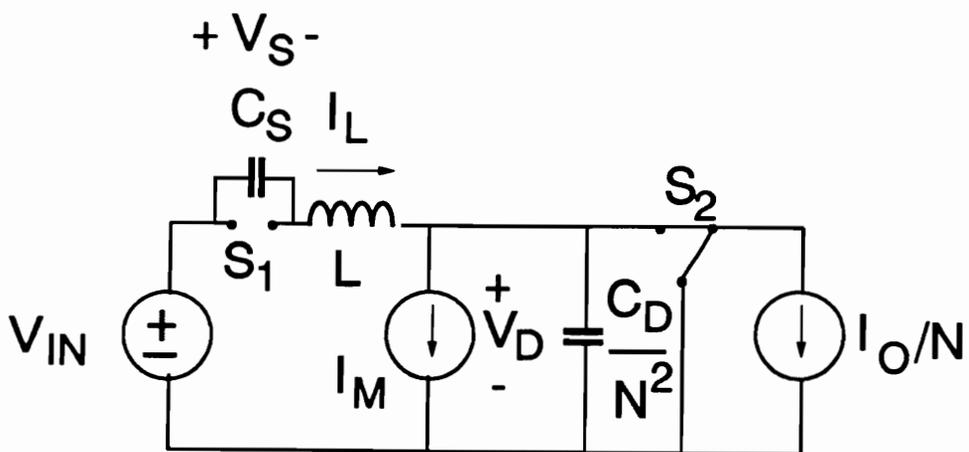
Figure A.21.   Topological Stage F of ideal CF forward ZVS-MRC.

$$\frac{d^2 v_S(t)}{dt^2} + \omega_O^2 v_S(t) = \omega_O^2 V_{IN} \qquad (A.35)$$

Solution:

$$v_S^F = a_F \cos \omega_O t + b_F \sin \omega_O t + V_{IN} \qquad (A.36.a)$$

$$i_L^F = b_F Z_O^{-1} \cos \omega_O t - a_F Z_O^{-1} \sin \omega_O t \qquad (A.36.b)$$

where

$$a_F = V_S^F - V_{IN} \qquad (A.37.a)$$

$$b_F = I_L^F Z_O \qquad (A.37.b)$$

or in the normalized form:

$$v_S^{FN} = 1 - \cos 2\pi t_N + I_L^{FN} I_{ON} \sin 2\pi t_N \qquad (A.38.a)$$

$$i_L^{FN} = I_L^{FN} \cos 2\pi t_N + \frac{\sin 2\pi t_N}{I_{ON}} \qquad (A.38.b)$$

Stage Duration $T_F = T_{F1} - T_{FO}$

The stage duration T_F is determined by the turn-off time of the CF switch Q_2.

A.4 Calculating the DC Voltage-Conversion-Ratio

To find the dc voltage-conversion-ratio of the CF forward ZVS-MRC, the secondary transformer voltage has to be integrated during the intervals for which the forward diode D_1 conducts relative to the switching period. For the CF forward ZVS-MRC, only topological Stages A and D transfer power to the load. Therefore, by finding the average secondary transformer voltage during the duration of these stages, the output voltage can be calculated in the following manner:

$$V_O = f_O[\sum_0^{n_1}\int_0^{T_A} v_D^A dt + \sum_0^{n_2}\int_0^{T_D} v_D^D dt] \qquad (A.39)$$

where n_1 and n_2 are the number of times Stage A and Stage D occur during one switching cycle, respectively. The dc voltage-conversion-ratio can be calculated simply by normalizing Eq. (A.39) with respect to the source voltage V_{IN}/N:

$$M = \sum_0^{n_1} \int_0^{T_{AN}} v_D^{AN} dt_N + \sum_0^{n_2} \int_0^{T_{DN}} v_D^{DN} dt_N \tag{A.40}$$

The normalized average transformer voltage for these two stages is given by the following expressions:

$$\int_0^{T_{AN}} v_D^{AN} dt_N = \frac{(V_D^{AN} - 1) \sin 2\pi K T_{AN}}{2\pi K} + I_{ON}(I_L^{AN} - 1 - I_{MN}) \frac{(1 - \cos 2\pi K T_{AN})}{2\pi K}$$

$$+ T_{AN} \tag{A.41.a}$$

$$\int_0^{T_{DN}} v_D^{DN} dt_N = \frac{V_D^{DN} \sin 2\pi K_2^{1/2} T_{DN}}{2\pi K_2^{1/2}} + I_{ON}(\frac{I_L^{DN} - 1 - I_{MN}}{C_N} + \frac{1 + I_{MN}}{1 + C_N}) \frac{(1 - \cos 2\pi K_2^{1/2} T_{DN})}{2\pi K_2^{1/2}}$$

$$+ (1 - V_S^{DN} + C_N V_D^{DN}) \frac{(T_{DN} - \sin 2\pi K_2^{1/2} T_{DN})}{(2\pi K_2^{1/2})(1 + C_N)} - \frac{\pi I_{ON}(1 + I_{MN}) T_{DN}^2}{1 + C_N} \tag{A.41.b}$$

A FORTRAN program is used to calculate the dc voltage-conversion-ratio curves. ·

Appendix B. Analysis CF HB ZVS-MRC

The circuit diagram of the CF HB ZVS-MRCs is shown in Fig. B.1. The CF HB ZVS-MRC is obtained by replacing the output rectifiers in the HB ZVS-MRC with transistors Q_3 and Q_4. Resonant capacitors C_1 and C_2 represent the output capacitance of the primary transistors, Q_1 and Q_2. Resonant inductor L can either be a separate inductor or the leakage inductance of the transformer. Since the junction capacitance of the CF switches is not sufficiently large to obtain the desired resonance, capacitors C_3 and C_4 are usually externally-added capacitors.

B.1 DC Analysis

To simplify the analysis, in addition to the assumptions made for the forward converter, it is assumed that Q_1 and Q_2 and switches Q_3 and Q_4 are identical, so that $C_1 = C_2 = C_S$ and
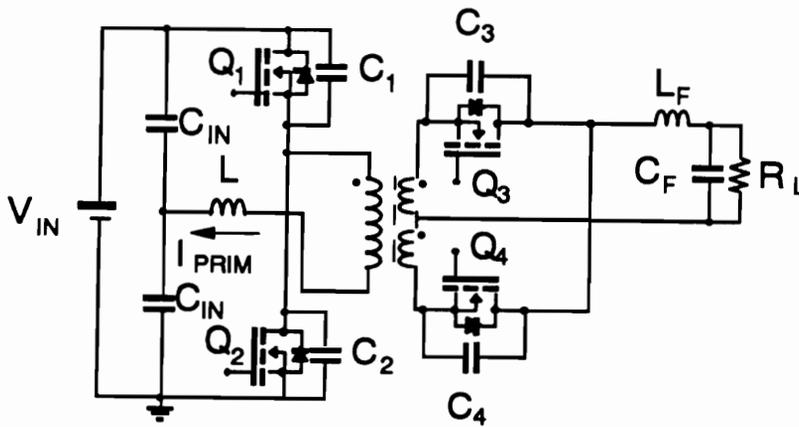
Figure B.1. The CF HB ZVS-MRC.

$C_3 = C_4 = C_D$. Since the magnetizing current is not important for the operation of the half-bridge converter, it is ignored.

It was found that during one switching cycle the converter enters a sequence of five topological stages out of the seven possible shown in Fig. B.2. It was also found that the CF HB ZVS-MRC can operate in six modes. Mode I.A occurs at high load currents and high dc voltage conversion ratios, whereas modes II.A, II.B, and II.C occur at light load currents and high dc voltage conversion ratios. Modes I.B and I.C occur for low dc voltage conversion ratios and high conduction periods of the CF switches.

B.1.1 Mode I of Operation

Mode I.A

Figure B.3 shows the key waveforms of the CF HB ZVS-MRC during Mode I.A of operation. The sequence of the topological stages in this mode is A-B-C-CF-D.

Stage A $[T_O, T_1]$, Fig. B.2(a)

At time T_O, Q_1 is turned off. Since the antiparallel diode of Q_3 is reverse-biased, capacitances C_1, C_2, and C_4 resonate with inductance L. During this stage capacitance C_1 is being charged in a resonant manner and C_2 is being discharged. The stage terminates at time T_1 when voltage across capacitor C_2 becomes zero (at the same time voltage across C_1 is V_{IN}). Sub-

(a) Stage A

(b) Stage B

(c) Stage C

(d) Stage D

(e) Stage AF
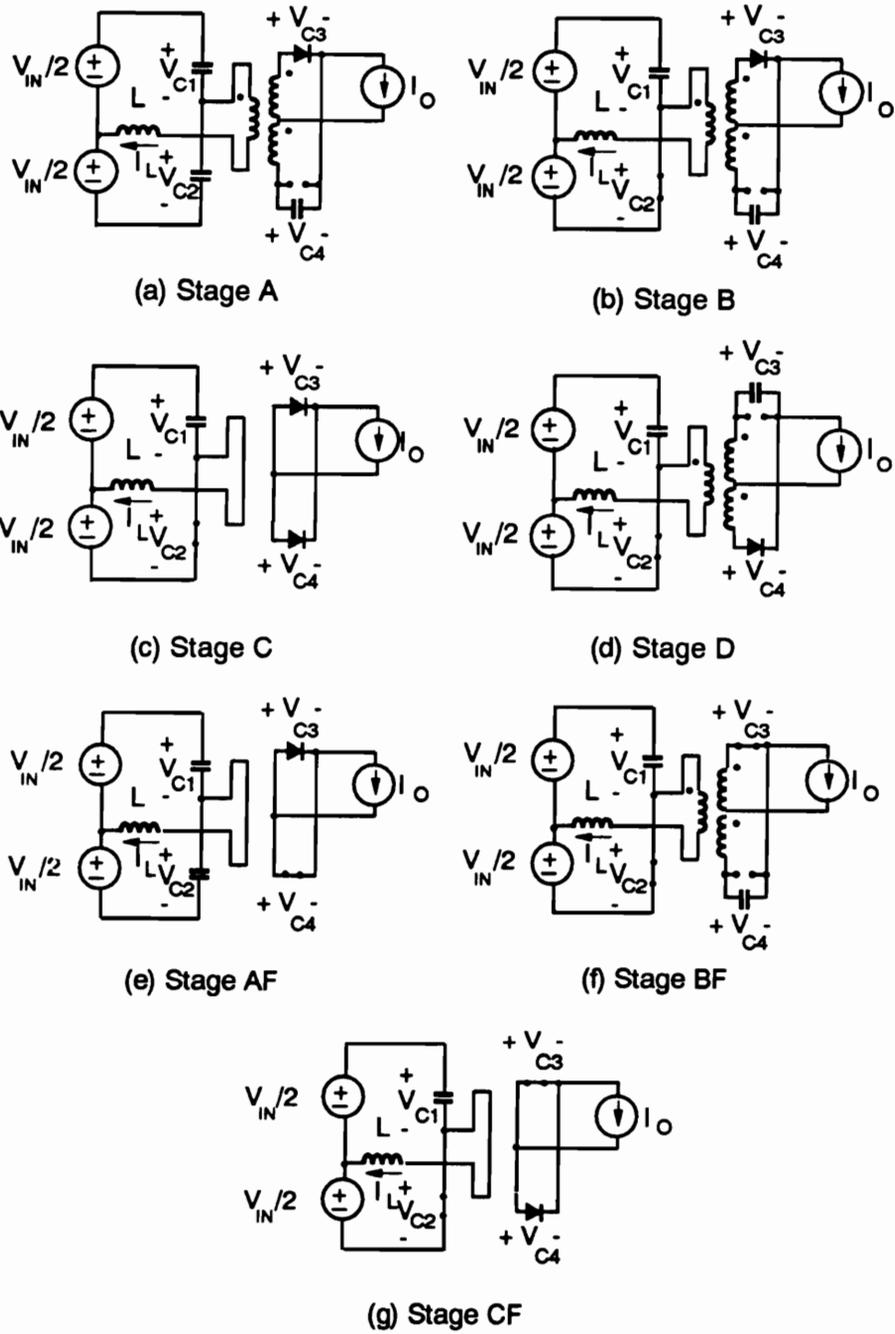
(f) Stage BF

(g) Stage CF

Figure B.2. Topological stages of the CF HB ZVS-MRC: (a) Stage A, (b) Stage B, (c) Stage C, (d) Stage D, (e) Stage AF, (f) Stage BF, and (g) Stage CF.
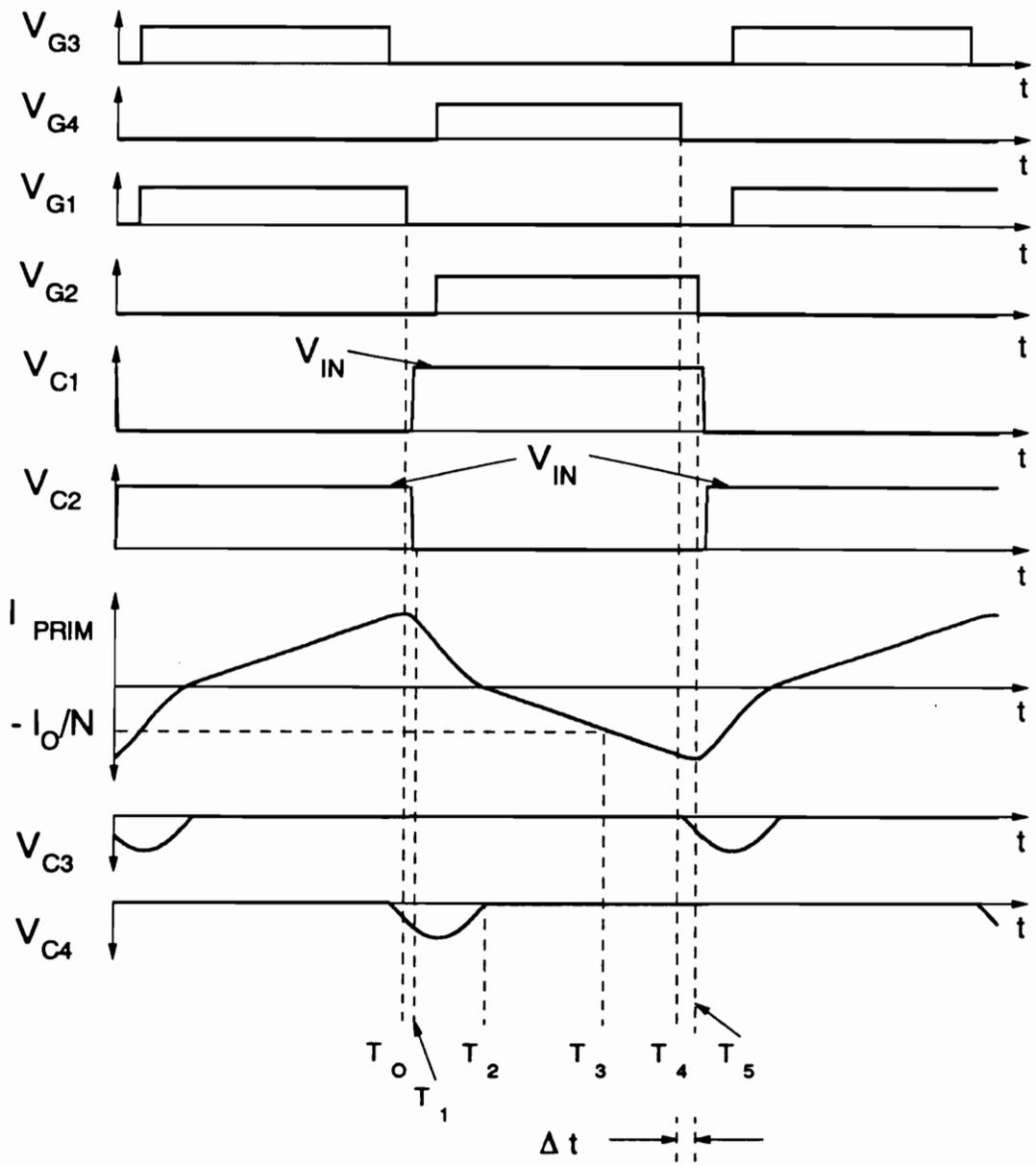
Figure B.3. Ideal waveforms of the CF HB ZVS-MRC operating in Mode I.A, from top to bottom: gate-source voltage V_{G3}, gate-source voltage V_{G4}, gate-source voltage V_{G1}, gate-source voltage V_{G2}, drain-source voltage of switch Q_1, V_{C1}, drain-source voltage of switch Q_2, V_{C2}, primary current I_{PRIM}, capacitor voltage V_{C3}, and capacitor voltage V_{C4}. Δt is defined as the time elapsed between the turn-off of the primary switch, Q_1 or Q_2, and the corresponding constant frequency switch.

sequently, switch Q_2 and the constant frequency switch Q_3 should be turned on to achieve soft switching.

Stage B [T_1, T_2], Fig. B.2(b)

In this stage C_4 continues to resonate with L. Due to a negative voltage across L, the primary current decreases and C_4 continues to discharge. The stage terminates at time T_2 when the capacitor voltage across C_4 becomes zero and the antiparallel diode of Q_4 turns on.

Stage C [T_2, T_3], Fig. B.2(c)

In this stage the antiparallel diodes of Q_3 and Q_4 conduct so that the secondary windings of the transformer are shorted. As a result, the primary voltage across the transformer is zero and a negative voltage is applied to L. The primary current decreases with a constant rate. This stage terminates at time T_3 when the primary current becomes $-I_O/N$ and the antiparallel diode of Q_3 ceases to conduct.

Stage CF [T_3, T_4], Fig. B.2(g)

During this stage transistor Q_3 conducts. The primary voltage of the transformer is zero and the current through the resonant inductor continues to decrease at a constant rate. This stage terminates when switch Q_3 is turned off at time T_4.

Stage D [T_4, T_5], Fig. B.2(d)

At time T_4, C_3 starts resonating with inductance L. This stage ends when transistor Q_2 is turned off and a new conversion cycle is initiated.

In Mode I.A of operation the time at which capacitance C_3 resonates with inductance L is delayed until switch Q_3 is turned off (as long as switch Q_3 is on the voltage across C_3 is shorted).

Mode I.B

The sequence of topological stages in this mode of operation is A-B-C-CF-AF.

Stage A [T_O, T_1], Fig. B.2(a)

At time T_O, Q_4 is turned off. The antiparallel diode of Q_3 is reverse-biased and capacitances C_1, C_2, and C_4 resonate with inductance L. During this stage capacitance C_1 is being charged in a resonant manner and C_2 is being discharged. The stage terminates at time T_1, when voltage across capacitor C_2 becomes zero (at the same time voltage across C_1 is V_{IN}). Subsequently, Q_2 and Q_3 should be switched on to achieve lossless turn-on.

Stage B [T_1, T_2], Fig. B.2(b)

In this stage C_4 continues to resonate with L. Due to a negative voltage across L, the primary current decreases and C_4 continues to discharge. The stage terminates at time T_2, when the capacitor voltage across C_4 becomes zero and the antiparallel diode of Q_4 turns on.

Stage C [T_2, T_3], Fig. B.2(c)

In this stage the antiparallel diodes of Q_3 and Q_4 conduct so that the secondary windings of the transformer are shorted. As a result, the primary voltage across the transformer is zero and a negative voltage is applied to L. The primary current decreases with a constant rate. The stage terminates at time T_3 when the primary current becomes $-I_O/N$ and the antiparallel diode of Q_3 ceases to conduct.

Stage CF [T_3, T_4], Fig. B.2(g)

During this stage transistor Q_3 conducts. The primary voltage of the transformer is zero and the current through the resonant inductor continues to decrease at a constant rate. This stage terminates when switch Q_1 is turned off at time T_4.

Stage AF [T_4, T_5], Fig. B.2(e)

In this stage switch Q_3 is on and the antiparallel diode of switch Q_4 is conducting resulting in a zero primary transformer voltage. Capacitances C_1 and C_2 resonate with inductance L. Capacitance C_1 is being charged in a resonant manner and capacitance C_2 is being discharged at the same rate. This stage ends at time time T_5 when switch Q_3 is turned off.

In Mode I.B of operation switch Q_3 is turned off a short interval after switch Q_2 is turned off and before switch Q_1 is turned on under zero voltage.

Mode I.C

Figure B.4 shows the key waveforms of the CF HB ZVS-MRC during Mode I.C of operation. The sequence of the topological stages in this mode is AF-CF-B-C-CF.

Stage AF [T_O, T_1], Fig. B.2(e)

At time T_O, switch Q_1 is turned off. Switch Q_4 and the antiparallel diode of switch Q_3 remains on clamping the primary transformer voltage to zero, and capacitance C_1 and C_2 resonate with L. Capacitance C_1 is charged in a resonant manner and capacitance C_2 discharges at the same rate during this stage. This stage ends when the voltage across capacitance C_2 decreases to zero through a resonant oscillation. At the same time the voltage across capacitance C_1 reaches the supply voltage and remains clamped to this value. Subsequently, switch Q_2 should be turned under soft switching conditions.

Stage CF [T_1, T_2], Fig. B.2(g)

During this stage switches Q_2, Q_4 and the antiparallel diode of switch Q_3 are on and the load current freewheels through the shorted secondary winding of the transformer. The voltage across the resonant inductor is negative and the current through this inductor decreases at a constant rate. This stage ends at time time T_2 when switch Q_4 is turned off.

Stage B [T_2, T_3], Fig. B.2(b)

In this stage switch Q_2 and the antiparallel diode of switch Q_3 conduct. Due to the negative voltage across inductance L, the primary current decreases and capacitance C_4 is first
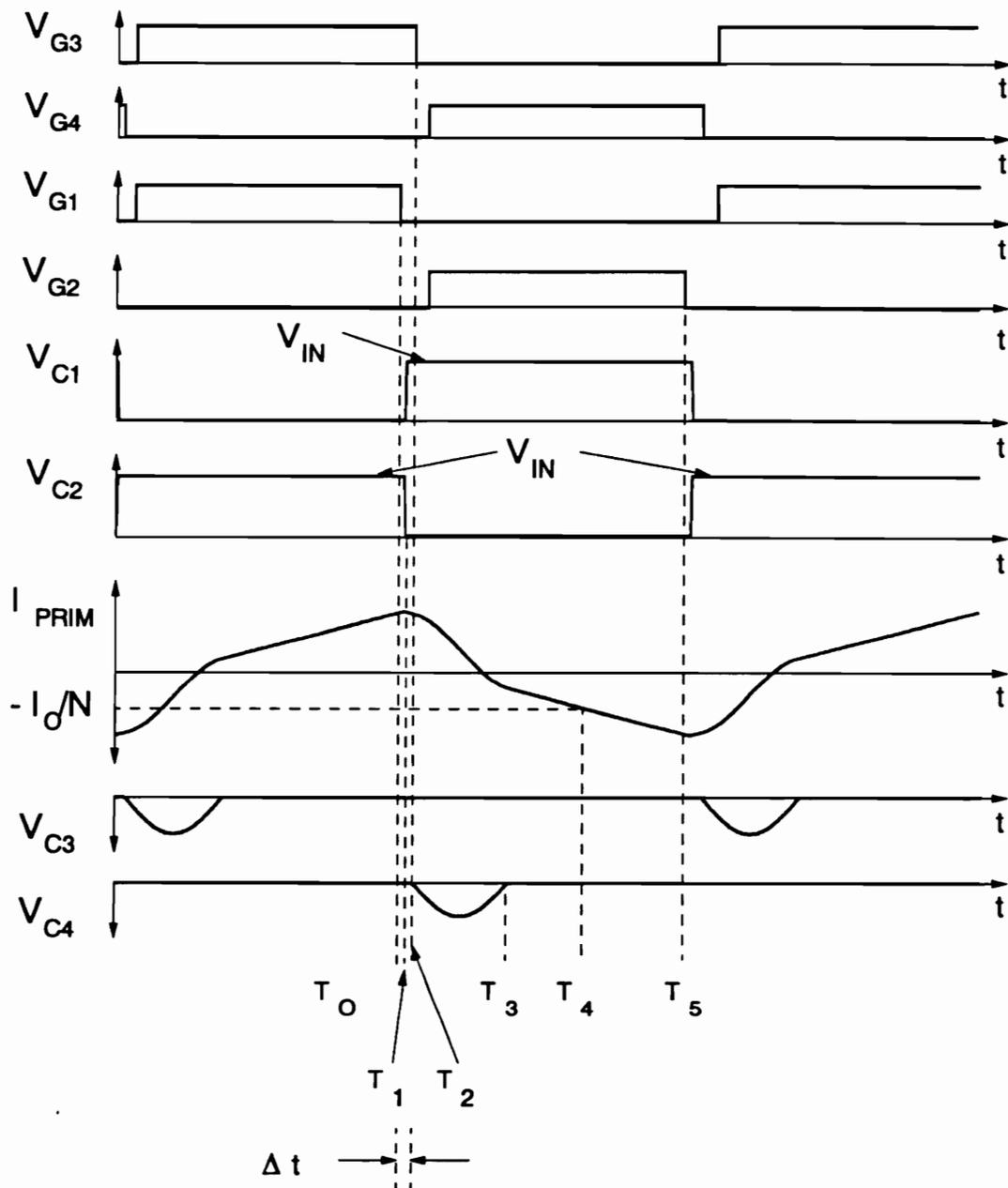
Figure B.4. Ideal waveforms of the CF HB ZVS-MRC operating in Mode I.C, from top to bottom: gate-source voltage V_{G3}, gate-source voltage V_{G4}, gate-source voltage V_{G1}, gate-source voltage V_{G2}, drain-source voltage of switch Q_1, V_{C1}, drain-source voltage of switch Q_2, V_{C2}, primary current I_{PRIM}, capacitor voltage V_{C3}, and capacitor voltage V_{C4}. Δt is defined as the time elapsed between the turn-off of the primary switch, Q_1 or Q_2, and the corresponding constant frequency switch.

charged and subsequently discharged in a resonant manner. This stage ends when the capacitor voltage across C_4 becomes zero and the antiparallel diode of switch Q_4 turns on.

Stage C [T_3, T_4], Fig. B.2(c)

In this stage the antiparallel diodes of Q_3 and Q_4 conduct so that the secondary windings of the transformer are shorted. As a result, the primary voltage across the transformer is zero and a negative voltage is applied to L. The primary current decreases at a constant rate. The stage terminates at time T_4, when the primary current becomes $-I_O/N$ and the antiparallel diode of Q_3 ceases to conduct.

Stage CF [T_4, T_5], Fig. B.2(g)

During this stage transistor Q_3 and the antiprallel diode of switch Q_4 conduct. The primary voltage of the transformer is zero and the current through the resonant inductor continues to decrease at a constant rate. This stage ends when transistor Q_2 is turned off and a new conversion cycle is initiated at time T_5.

In Mode I.C switch Q_3 remains on for a longer time than in the two previous modes and is turned off after the switching transition of the primary switches. The resonance of the secondary side capacitances is interrupted for most of the switching cycle, resulting in low output voltages.

B.1.2 Mode II of Operation

In this mode of operation the current through the resonant inductor is betweem $I_O/N < I_L < -I_O/N$ at the time the secondary side resonant capacitor discharges, resulting in the absence of the natural freewheeling stage (Stage C). Mode II is characterized by increased circulating currents in the rectifier circuit and the secondary windings of the transformer.

Mode II.A

Figure B.5 shows the key waveforms of the CF HB ZVS-MRC during Mode II.A of operation. The sequence of the topological stages in this mode is A-B-BF-CF-D.

Stage A $[T_O, T_1]$, Fig. B.2(a)

At time T_O, Q_1 is turned off. Since the antiparallel diode of Q_3 is reverse-biased, capacitances C_1, C_2, and C_4 resonate with inductance L. During this stage capacitance C_1 is being charged in a resonant manner and C_2 is being discharged. The stage terminates at time T_1, when voltage across capacitor C_2 becomes zero (at the same time voltage across C_1 is V_{IN}). Subsequently, Q_2 and Q_3 should be turned on to eliminate the turn-on loss.

Stage B $[T_1, T_2]$, Fig. B.2(b)

In this stage C_4 continues to resonate with L. Due to a negative voltage across L, the primary current decreases and C_4 continues to discharge. The stage terminates at time T_2, when the
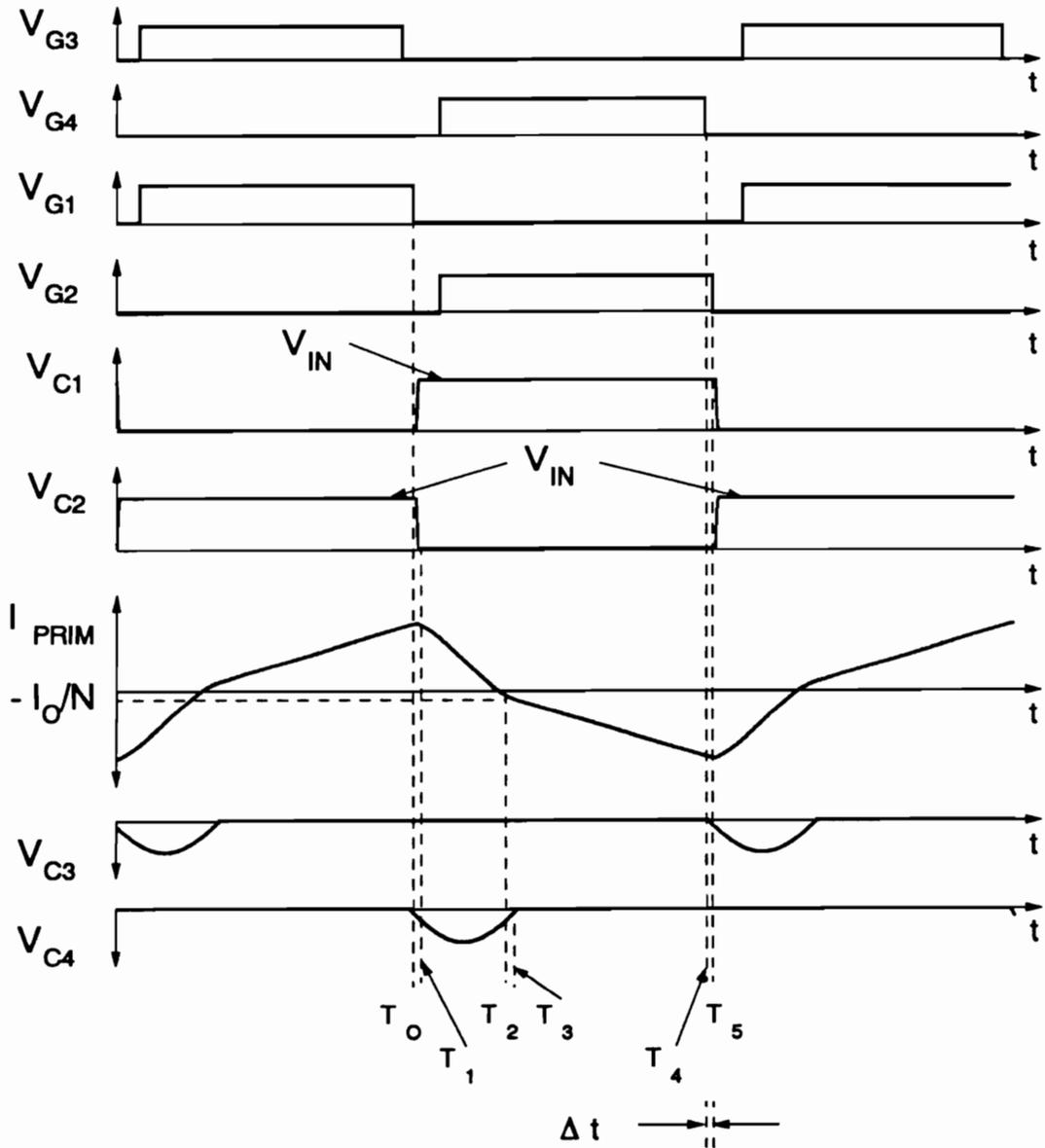
Figure B.5. Ideal waveforms of the CF HB ZVS-MRC operating in Mode II.A, from top to bottom: gate-source voltage V_{G3}, gate-source voltage V_{G4}, gate-source voltage V_{G1}, gate-source voltage V_{G2}, drain-source voltage of switch Q_1, V_{C1}, drain-source voltage of switch Q_2, V_{C2}, primary current I_{PRIM}, capacitor voltage V_{C3}, and capacitor voltage V_{C4}. Δt is defined as the time elapsed between the turn-off of the primary switch, Q_1 or Q_2, and the corresponding constant frequency switch.

current through the resonant inductor decreases to $-I_{ON}/N$, the antiparallel diode of switch Q_3 ceases to conduct, and switch Q_3 conducts.

Stage BF [T_2, T_3], Fig. B.2(f)

In this stage switch Q_2 and Q_3 are on and capacitance C_4 continues to resonate with inductance L. This stage ends at time T_3 when the voltage across capacitance C_4 decreases to zero through a resonant oscillation and the antiparallel diode of switch Q_4 starts to conduct.

Stage CF [T_3, T_4], Fig. B.2(g)

In stage CF transistor Q_3 and the anitparallel diode of Q_4 conduct. The primary voltage of the transformer is zero (secondary windings of the transformer are shorted) and the current through the resonant inductor continues to decrease at a constant rate. This stage terminates when switch Q_3 is turned off at time T_4.

Stage D [T_4, T_5], Fig. B.2(d)

At time T_4, C_3 starts to resonate with inductance L. This stage ends when transistor Q_2 is turned off and a new conversion cycle is initiated.

Mode II.B

In modes II.B and II.C, the CF switches are allowed to conduct a longer period of time and they are not turned off until after the primary switches (switches Q_1 or Q_2) have been turned off. The sequence of the topological stages in Mode II.B is A-B-BF-CF-AF.

Stage A $[T_O, T_1]$, Fig. B.2(a)

At time T_O, Q_4 is turned off. Since the antiparallel diode of Q_3 is reverse-biased, capacitances C_1, C_2, and C_4 resonate with inductance L. During this stage capacitance C_1 is being charged in a resonant manner and C_2 is being discharged. The stage terminates at time T_1 when voltage across capacitor C_2 becomes zero (at the same time voltage across C_1 is V_{IN}). Subsequently, Q_2 and Q_3 should be switched on to achieve lossless turn-on.

Stage B $[T_1, T_2]$, Fig. B.2(b)

In this stage C_4 continues to resonate with L. Due to a negative voltage across L, the primary current decreases and C_4 continues to discharge. The stage terminates at time T_2, when the current through the resonant inductor decreases to $-I_{ON}/N$ and switch Q_3 conducts as its antiparallel diode turn off.

Stage BF $[T_2, T_3]$, Fig. B.2(f)

In this stage switch Q_2 and Q_3 are on and capacitance C_4 continues to resonate with inductance L. This stage ends at time T_3 when the voltage across capacitance C_4 decreases to zero through a resonant oscillation and the antiparallel diode of switch Q_4 starts to conduct.

Stage CF [T_3, T_4], Fig. B.2(g)

During this stage transistor Q_3 and the anitparallel diode of Q_4 conduct. The primary voltage of the transformer is zero (secondary windings of the transformer are shorted) and the current through the resonant inductor continues to decrease at a constant rate. This stage terminates when switch Q_2 is turned off at time T_4.

Stage AF [T_4, T_5], Fig. B.2(e)

At time T_4, capacitances C_1 and C_2 start to resonate with inductance L. During Stage AF Q_3 remains on and the antiparallel diode of switch Q_4 continues to conduct (transformer secondary winding remain shorted). Capacitance C_1 charges in a resonant manner and capacitance C_2 discharges at the same rate. Stage AF ends when switch Q_3 is turned off.

Mode II.C

In Mode II.B switch Q_3 is turned off after switch Q_2 is turned off and before switch Q_1 is turned on under zero voltage. In Mode II.C, however, switch Q_3 is turned off after the switching transition for switches Q_1 and Q_2 has occurred. The sequence of the topological stages in Mode II.C is AF-CF-B-BF-CF. Figure B.6 shows the key waveforms of the CF HB ZVS-MRC operating in Mode II.C.

Stage AF [T_O, T_1], Fig. B.2(e)

At time T_O, Q_1 is turned off. The antiparallel diode of Q_3 is forward-biased and the antiparallel diode of switch Q_4 conducts. During this stage capacitances C_1 and C_2 resonate with
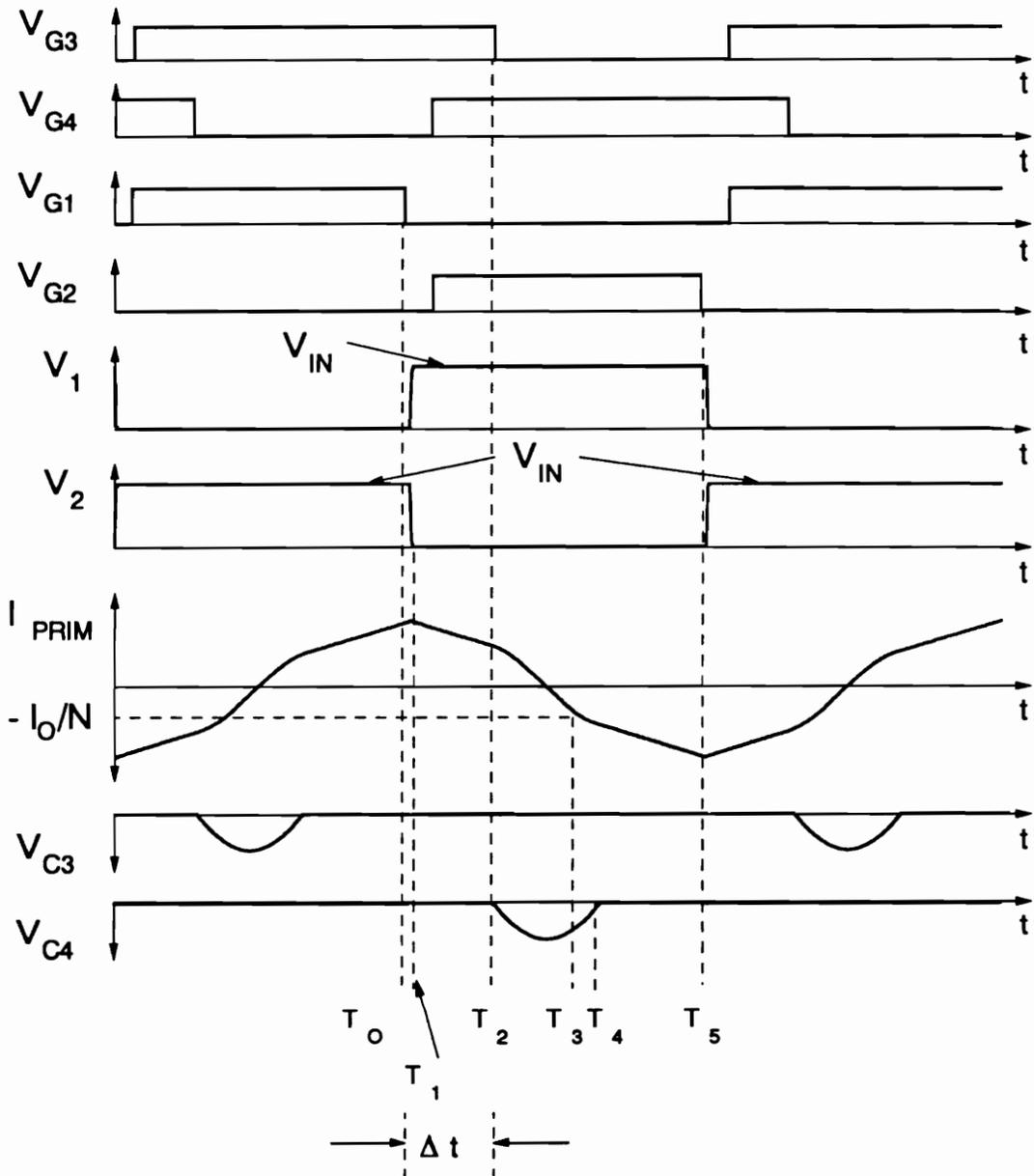
Figure B.6. Ideal waveforms of the CF HB ZVS-MRC operating in Mode II.C, from top to bottom: gate-source voltage V_{G3}, gate-source voltage V_{G4}, gate-source voltage V_{G1}, gate-source voltage V_{G2}, drain-source voltage of switch Q_1, V_{C1}, drain-source voltage of switch Q_2, V_{C2}, primary current I_{PRIM}, capacitor voltage V_{C3}, and capacitor voltage V_{C4}. Δt is defined as the time elapsed between the turn-off of the primary switch, Q_1 or Q_2, and the corresponding constant frequency switch.

inductance L. The secondary windings of power transformer are shorted and capacitance C_1 is charged in a resonant manner and C_2 is discharged at the same rate. The stage terminates at $t = T_1$ when voltage across capacitor C_2 becomes zero (at the same time voltage across C_1 is V_{IN}). Subsequently, Q_2 and Q_3, should be turned on to eliminate the switching loss.

Stage CF [T_1, T_2], Fig. B.2(g)

During this stage Q_4 remains on and the antiparallel diode of switch Q_3 continues to conduct. The secondary windings of the transformer remain shorted and the current through the resonant inductor decreases at a constant rate. This stage ends when switch Q_4 is turned off.

Stage B [T_2, T_3], Fig. B.2(b)

In this stage C_4 starts to resonate with L. Due to a negative voltage across L, the primary current decreases and C_4 charges in a resonant manner. The stage terminates at time T_2, when the current through the resonant inductor decreases to $- I_{ON}/N$. Also, the antiparallel diode of switch Q_3 ceases to conduct and switch Q_3 begins to conducts.

Stage BF [T_3, T_4], Fig. B.2(f)

In this stage switch Q_2 and Q_3 are on and capacitance C_4 continues to resonate with inductance L. This stage ends at time T_4 when the voltage across capacitance C_4 decreases to zero through a resonant oscillation and the antiparallel diode of switch Q_4 starts to conduct.

, Stage CF [T_4, T_5], Fig. B.2(g)

In Stage CF transistor Q_3 and the anitparallel diode of Q_4 conduct. The primary voltage of the transformer is zero (secondary windings of the transformer are shorted) and the current through the resonant inductor continues to decrease at a constant rate. This stage terminates when switch Q_2 is turned off at time T_5.

Table B.1 summarizes the five-stage sequences of all the modes of operation modeled for the CF HB ZVS-MRC.

B.2 DC Voltage-Conversion-Ratio

Figures B.7a - B.14a shows the typical dc voltage-conversion-ratio characteristics of the CF HB ZVS-MRC as a function of δ. δ is defined as the time between the turn-off of the CF switch Q_3 or Q_4, and the turn-off of the primary switch Q_1 or Q_2, respectively (Δt in Fig. 3.11) normalized with respect to $1/f_O$, where the resonant frequency is $f_O = 1/2\pi\sqrt{LC}$. The characteristics are given for different normalized conversion frequencies, f_{con}/f_0, and for different values of $C_N = 2C_D/(CN^2)$, where $f_{con} = 2f_S$ is the conversion frequency, f_S is the switching frequency, and N is the turns ratio of the transformer. Figures B.7a - B.14b are plotted for different values of the normalized output current. $I_{ON} = 2Z_O I_O/NV_{IN}$ where $Z_O = \sqrt{L/2C}$ is the characteristic impedance.

Table B.1. Modes of operation of the CF HB ZVS-MRC.

MODE	STAGE SEQUENCE
I.A	A - B - C - CF - D
I.B	A - B - C - CF - AF
I.C	AF - CF - B - C - CF
II.A	A - B - BF - CF - D
II.B	A - B - BF - CF - AF
II.C	AF - CF - B - BF - CF

A complete set of design characteristics is given for $C_N = 2, 5, 10,$ and 20, and $f_{CON}/f_O = 0.2,$ 0.25, 0.3, and 0.35 (Figs. B.7a - B.14b). Characteristics for all possible combinations are not given since not all possible combinations result in practical design curves. For example, low capacitance ratios ($C_N = 2$) and low switching frequencies ($f_{CON}/f_O < 0.35$) will result in operation where the CF switches conduct for an extended period of time regardless of the load current, resulting in high conduction losses. Similarly high capacitance ratio ($C_N = 20$) and very low switching frequencies ($f_{CON}/f_O < 0.2$) will also result in design where the CF switches conduct for an extended period of time. Again this will result in an inefficient design.

B.3 DC Analysis of the Topological Stages

Analytical expressions for the initial conditions, circuit equations, their solutions, and durations of the topological stages reffer to the ideal CF HB ZVS-MRC.

STAGE A [T_{AO}, T_{A1}] (Fig. B.15)

Initial Conditions:

$$v_{C1}(T_{AO}) = V_{C1}^A \qquad\qquad (B.1.a)$$

$$v_{C2}(T_{AO}) = V_{C2}^A \qquad\qquad (B.1.b)$$

$$i_{PRIM}(T_{AO}) = I_{PRIM}^A \qquad\qquad (B.1.c)$$
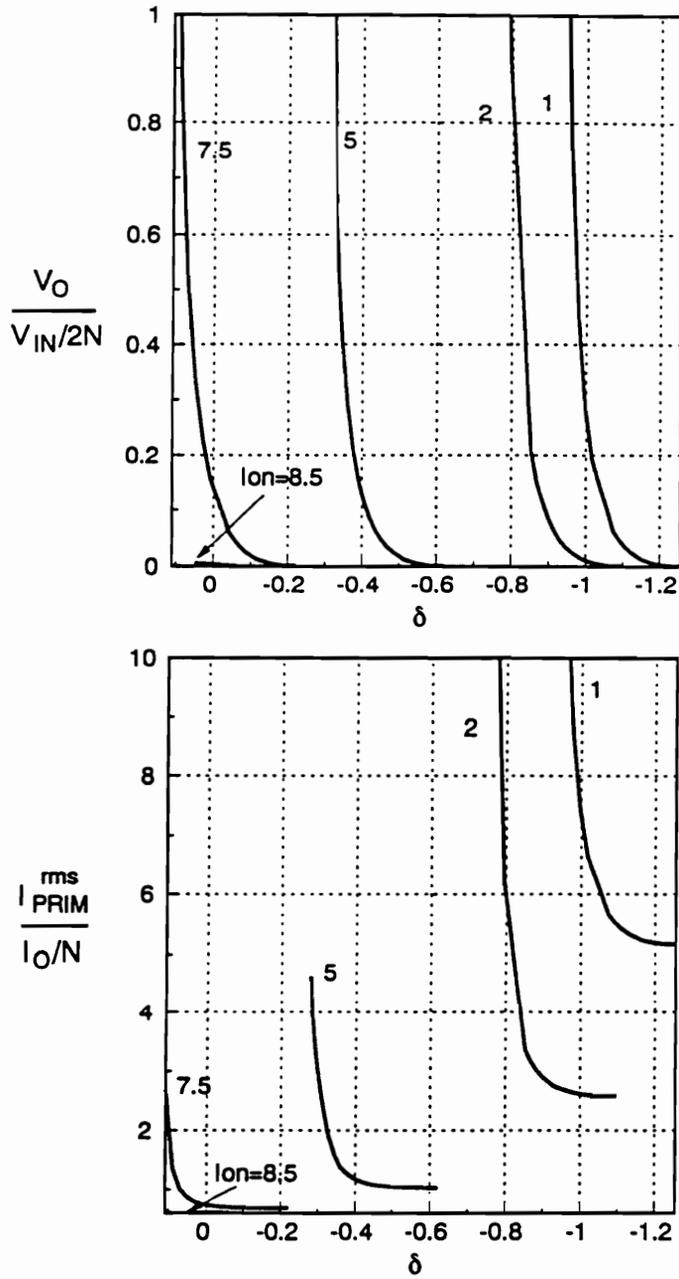
Figure B.7a. DC voltage conversion ratio curve of the CF HB ZVS-MRC for $C_N = 2$ and f_{CON}/f_O = 0.35. $C_N = 2C_D/(CN^2)$, $I_{ON} = 2I_OZ_O/(V_{IN}N)$, $Z_O = \sqrt{L/2C}$, and $f_O = 1/2\pi\sqrt{2LC}$.
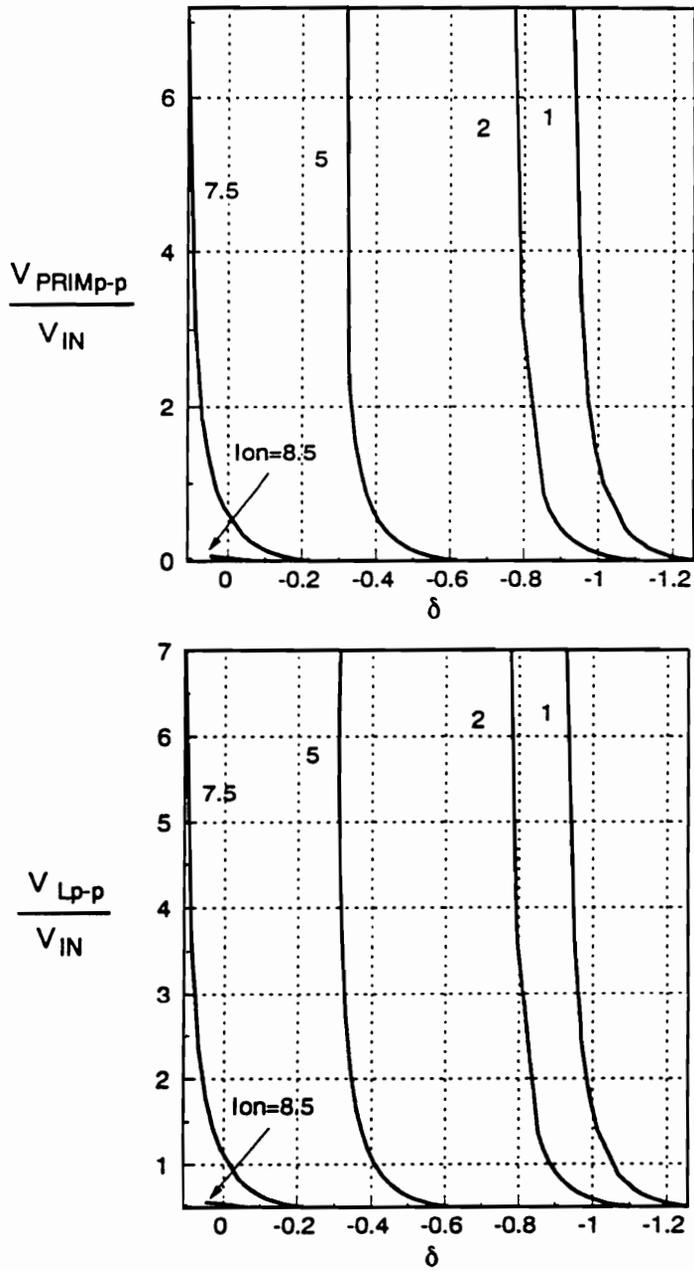
Figure B.7b. Normalized primary rms current and V_L^{p-p} characteristics of the CF HB ZVS-MRC for $C_N = 2$ and $f_{CON}/f_O = 0.35$. $C_N = 2C_D/(CN^2)$, $I_{ON} = 2I_O Z_O/(V_{IN}N)$, $Z_O = \sqrt{L/2C}$, and $f_O = 1/2\pi\sqrt{2LC}$.
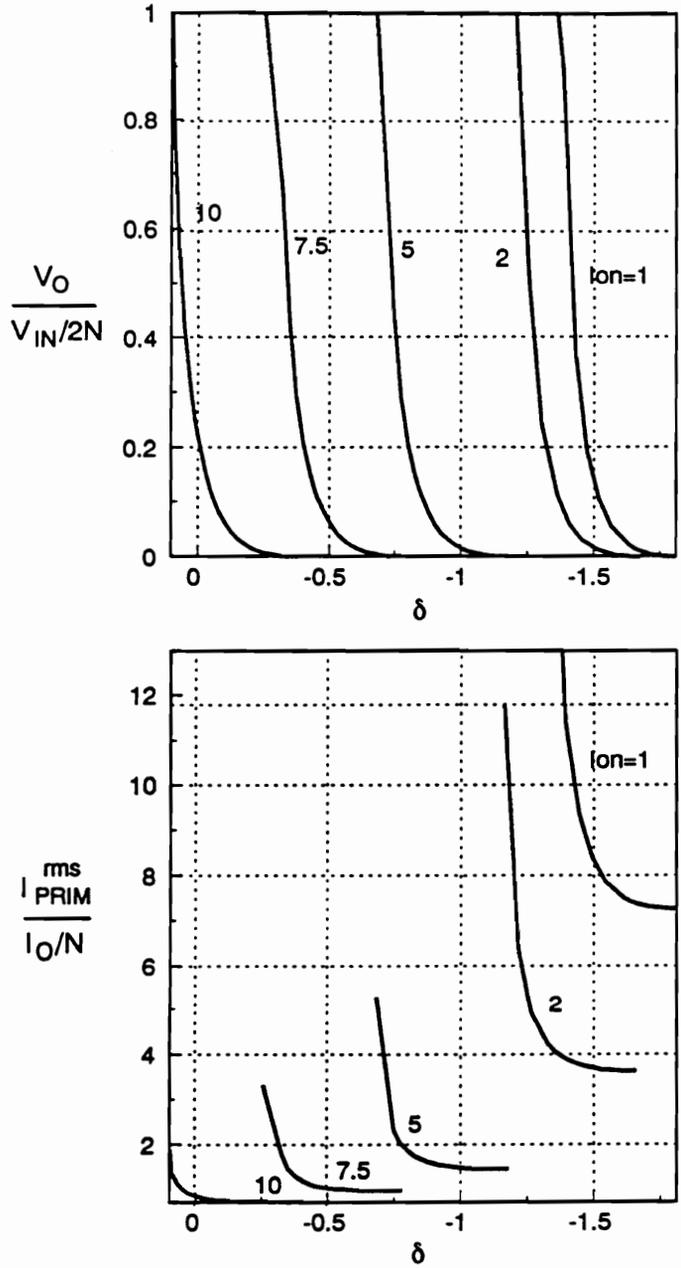
Figure B.8a.   DC voltage conversion ratio curve of the CF HB ZVS-MRC for $C_N = 5$ and f_{CON}/f_O
              = 0.25. $C_N = 2C_D/(CN^2)$, $I_{ON} = 2I_OZ_O/(V_{IN}N)$, $Z_O = \sqrt{L/2C}$, and
              $f_O = 1/2\pi\sqrt{2LC}$.
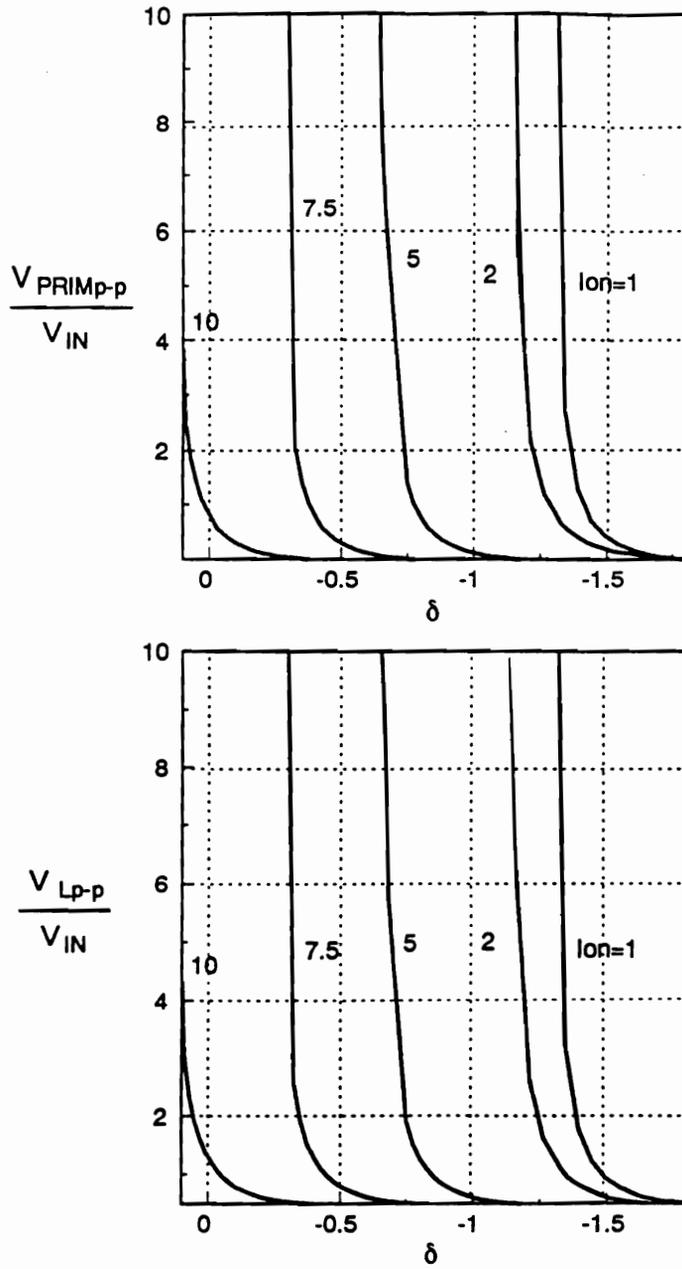
Figure B.8b. Normalized primary rms current and V_L^{p-p} characteristics of the CF HB ZVS-MRC for $C_N = 5$ and $f_{CON}/f_O = 0.25$. $C_N = 2C_D/(CN^2)$, $I_{ON} = 2I_OZ_O/(V_{IN}N)$, $Z_O = \sqrt{L/2C}$, and $f_O = 1/2\pi\sqrt{2LC}$.
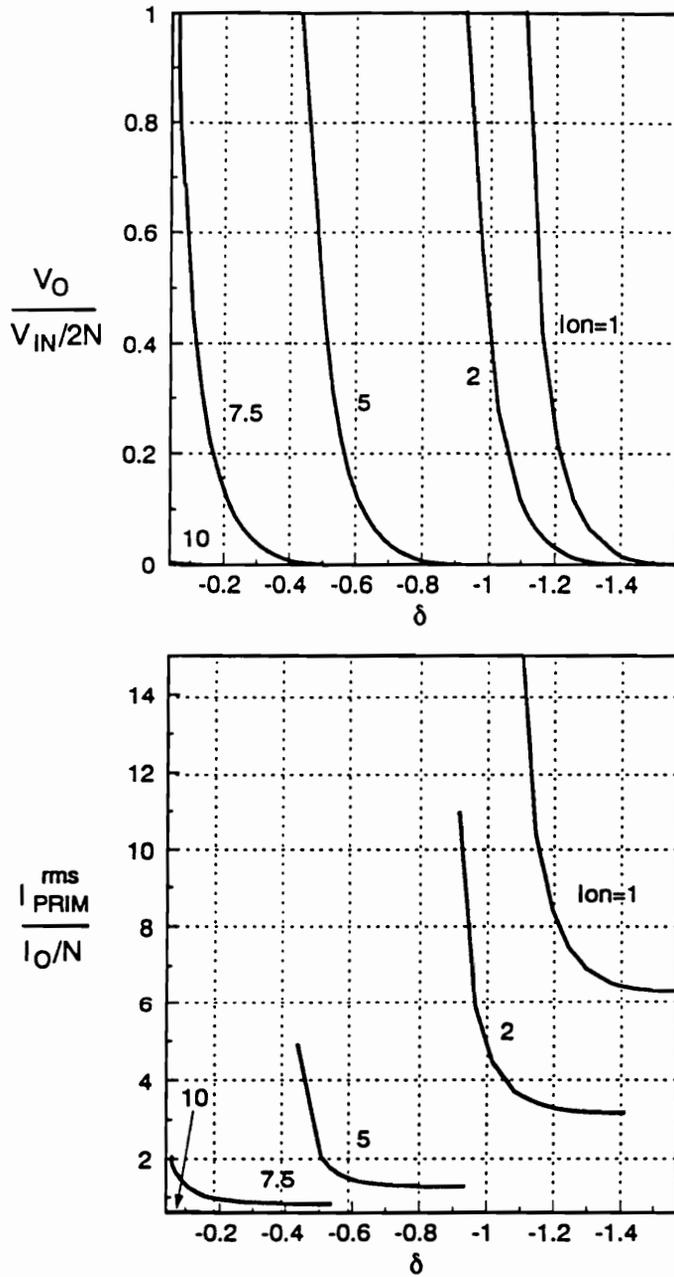
Figure B.9a. DC voltage conversion ratio curve of the CF HB ZVS-MRC for $C_N = 5$ and f_{CON}/f_O = 0.30. $C_N = 2C_D/(CN^2)$, $I_{ON} = 2I_O Z_O/(V_{IN}N)$, $Z_O = \sqrt{L/2C}$, and $f_O = 1/2\pi\sqrt{2LC}$.

Figure B.9b. Normalized primary rms current and V_L^{p-p} characteristics of the CF HB ZVS-MRC for $C_N = 5$ and $f_{CON}/f_0 = 0.30$. $C_N = 2C_D/(CN^2)$, $I_{ON} = 2I_0Z_0/(V_{IN}N)$, $Z_0 = \sqrt{L/2C}$, and $f_0 = 1/2\pi\sqrt{2LC}$.
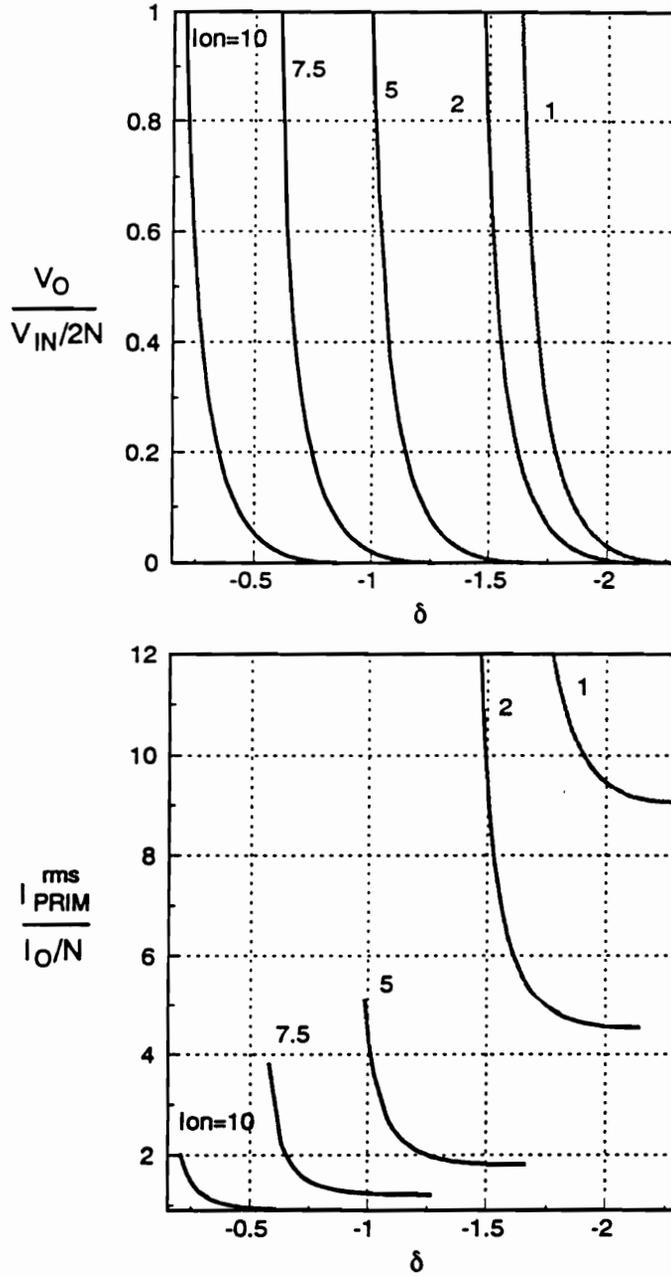
Figure B.10a. DC voltage conversion ratio curve of the CF HB ZVS-MRC for $C_N = 10$ and $f_{CON}/f_O = \underline{0.20}$. $C_N = 2C_D/(CN^2)$, $I_{ON} = 2I_OZ_O/(V_{IN}N)$, $Z_O = \sqrt{L/2C}$, and $f_O = 1/2\pi\sqrt{2LC}$.
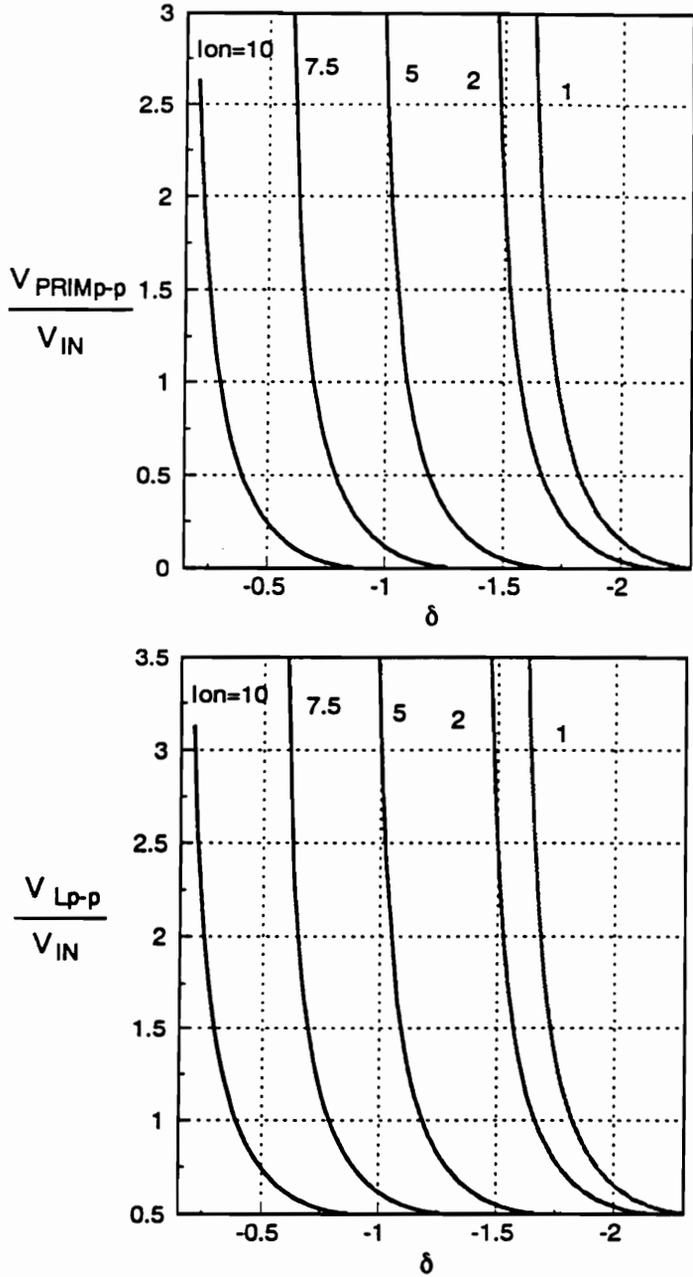
Figure B.10b. Normalized primary rms current and V_L^{p-p} characteristics of the CF HB ZVS-MRC for $C_N = 10$ and $f_{CON}/f_O = 0.20$. $C_N = 2C_D/(CN^2)$, $I_{ON} = 2I_OZ_O/(V_{IN}N)$, $Z_O = \sqrt{L/2C}$, and $f_O = 1/2\pi\sqrt{2LC}$.
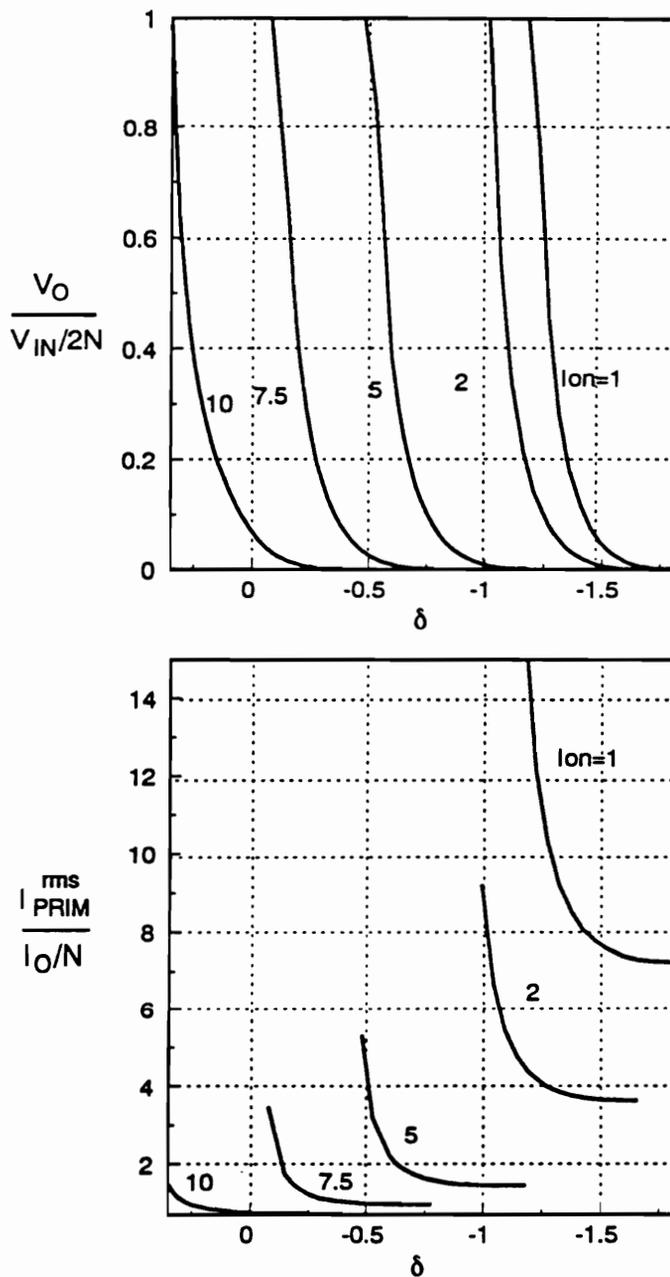
Figure B.11a. DC voltage conversion ratio curve of the CF HB ZVS-MRC for $C_N = 10$ and $f_{CON}/f_O = 0.25$. $C_N = 2C_D/(CN^2)$, $I_{ON} = 2I_O Z_O/(V_{IN}N)$, $Z_O = \sqrt{L/2C}$, and $f_O = 1/2\pi\sqrt{2LC}$.
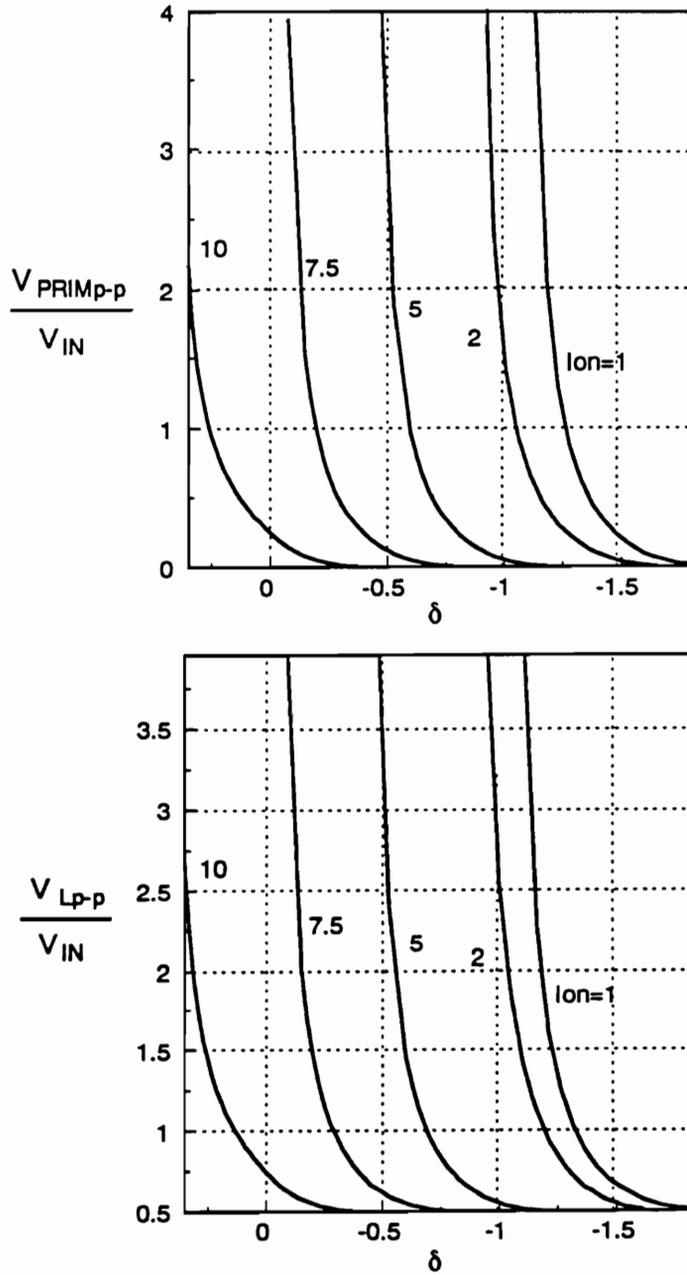
Figure B.11b. Normalized primary rms current and V_L^{p-p} characteristics of the CF HB ZVS-MRC for $C_N = 10$ and $f_{CON}/f_O = 0.25$. $C_N = 2C_D/(CN^2)$, $I_{ON} = 2I_OZ_O/(V_{IN}N)$, $Z_O = \sqrt{L/2C}$, and $f_O = 1/2\pi\sqrt{2LC}$.
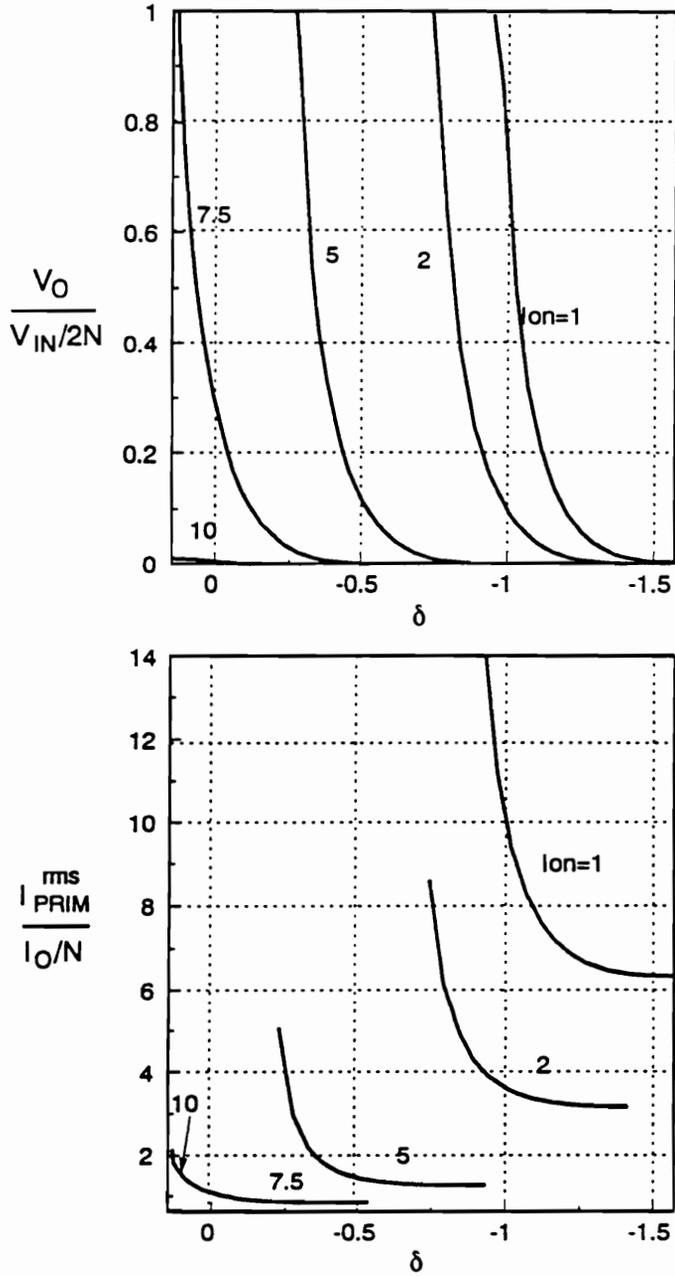
Figure B.12a. DC voltage conversion ratio curve of the CF HB ZVS-MRC for $C_N = 10$ and $f_{CON}/f_O = 0.30$. $C_N = 2C_D/(CN^2)$, $I_{ON} = 2I_O Z_O/(V_{IN}N)$, $Z_O = \sqrt{L/2C}$, and $f_O = 1/2\pi\sqrt{2LC}$.

Figure B.12b. Normalized primary rms current and V_L^{p-p} characteristics of the CF HB ZVS-MRC for $C_N = 10$ and $f_{CON}/f_O = 0.30$. $C_N = 2C_D/(CN^2)$, $I_{ON} = 2I_O Z_O/(V_{IN}N)$, $Z_O = \sqrt{L/2C}$, and $f_O = 1/2\pi\sqrt{2LC}$.

Figure B.13a. DC voltage conversion ratio curve of the CF HB ZVS-MRC for $C_N = 20$ and $f_{CON}/f_O = 0.25$. $C_N = 2C_D/(CN^2)$, $I_{ON} = 2I_OZ_O/(V_{IN}N)$, $Z_O = \sqrt{L/2C}$, and $f_O = 1/2\pi\sqrt{2LC}$.
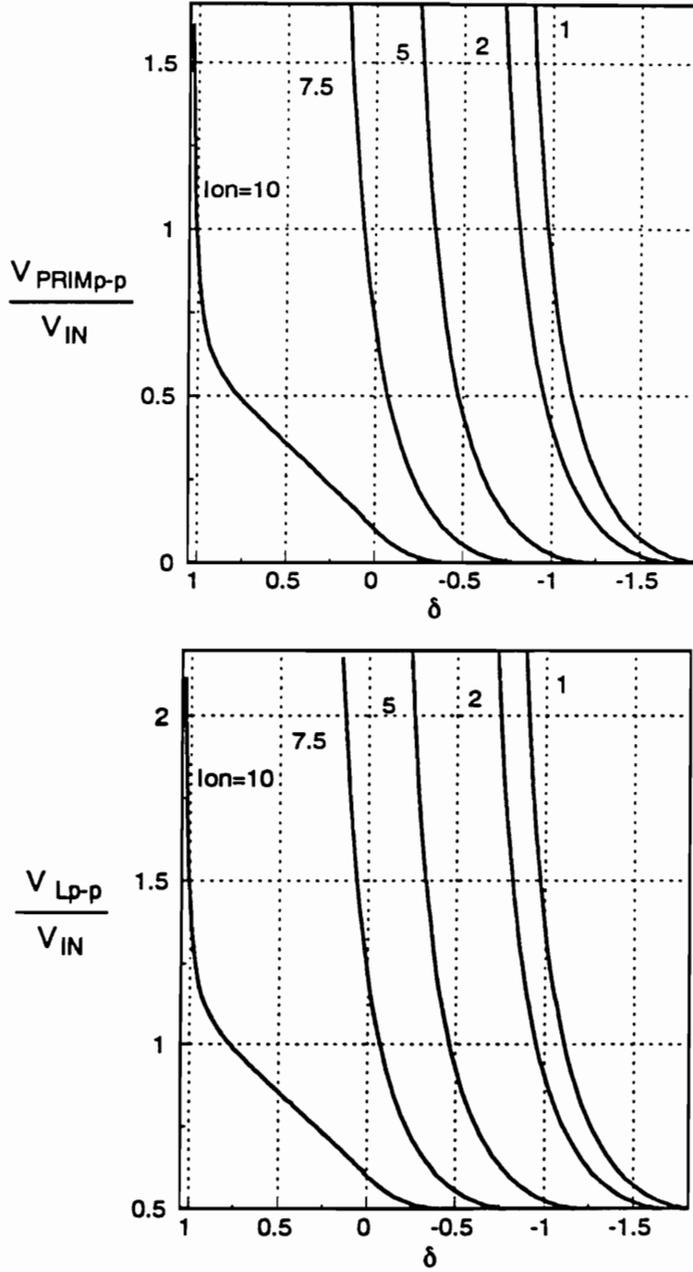
Figure B.13b. Normalized primary rms current and V_L^{p-p} characteristics of the CF HB ZVS-MRC for $C_N = 20$ and $f_{CON}/f_O = 0.25$. $C_N = 2C_D/(CN^2)$, $I_{ON} = 2I_O Z_O/(V_{IN}N)$, $Z_O = \sqrt{L/2C}$, and $f_O = 1/2\pi\sqrt{2LC}$.
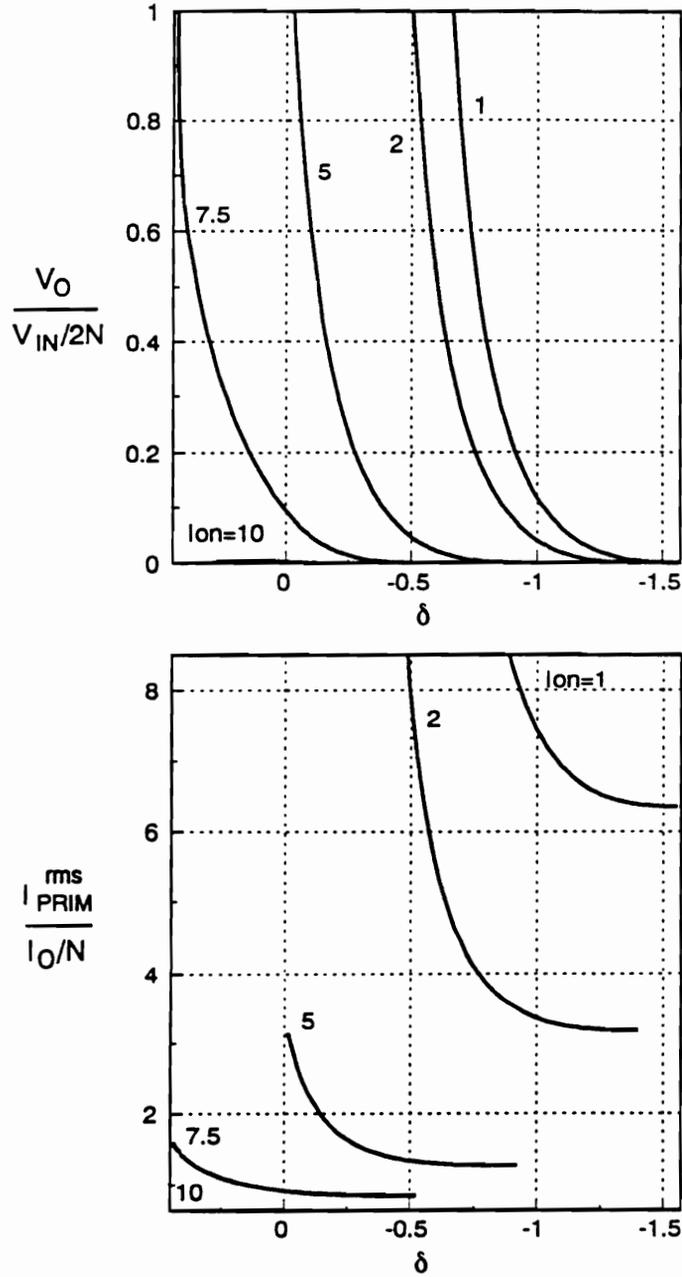
Figure B.14a.   DC voltage conversion ratio curve of the CF HB ZVS-MRC for $C_N = 20$ and $f_{CON}/f_O = \underline{0.30}$. $C_N = 2C_D/(CN^2)$, $I_{ON} = 2I_O Z_O/(V_{IN}N)$, $Z_O = \sqrt{L/2C}$,   and $f_O = 1/2\pi\sqrt{2LC}$.

Figure B.14b. Normalized primary rms current and V_L^{p-p} characteristics of the CF HB ZVS-MRC for $C_N = 20$ and $f_{CON}/f_O = 0.30$. $C_N = 2C_D/(CN^2)$, $I_{ON} = 2I_O Z_O/(V_{IN}N)$, $Z_O = \sqrt{L/2C}$, and $f_O = 1/2\pi\sqrt{2LC}$.

$$I_L = I_{PRIM}$$
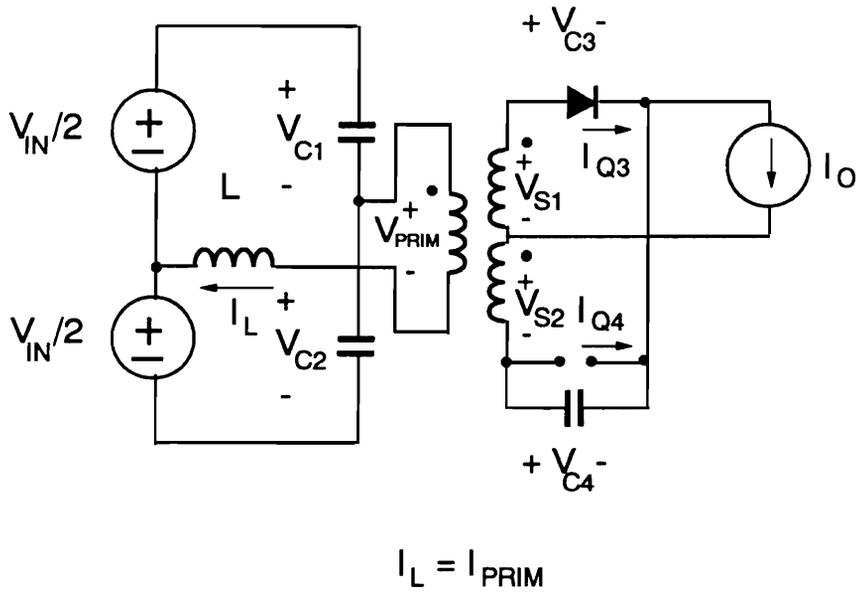
Figure B.15.   Topological Stage A of ideal CF HB ZVS-MRC.

$$v_{PRIM}(T_{AO}) = V_{PRIM}^{A} \qquad (B.1.d)$$

$$i_{Q3}(T_{AO}) = I_{Q3}^{A} \qquad (B.1.e)$$

$$i_{Q4}(T_{AO}) = I_{Q4}^{A} \qquad (B.1.f)$$

$$v_{Q3}(T_{AO}) = 0 \qquad (B.1.g)$$

$$v_{Q4}(T_{AO}) = V_{Q4}^{A} \qquad (B.1.h)$$

Equations:

$$v_{C1}(t) + v_{PRIM}(t) + L \frac{di_{PRIM}(t)}{dt} = \frac{V_{IN}}{2} \qquad (B.2.a)$$

$$i_{PRIM}(t) = C_1 \frac{dv_{C1}(t)}{dt} - C_2 \frac{dv_{C2}(t)}{dt} = 2C \frac{dv_{C1}(t)}{dt} \qquad (B.2.b)$$

$$i_{PRIM}(t) = \frac{1}{N} \left[i_{Q3}(t) - i_{Q4}(t) \right] \qquad (B.2.c)$$

$$i_{Q3}(t) + i_{Q4}(t) = I_O \qquad (B.2.d)$$

$$v_{S1}(t) + v_{S2}(t) = - v_{Q4}(t) \qquad (B.2.e)$$

$$i_{Q4}(t) = C_4 \frac{dv_{Q4}(t)}{dt} \qquad (B.2.f)$$

$$v_{S1}(t) = v_{S2}(t) = \frac{v_{PRIM}(t)}{N} \qquad (B.2.g)$$

From Eqs. (B.1.a) - (B.2.g), it follows that:

$$\frac{d^3 v_{C1}(t)}{dt^3} + \omega_O^2 K^2 \frac{dv_{C1}(t)}{dt} = \frac{NI_O}{8LCC_D} \qquad (B.3.a)$$

where

$$\omega_O = \frac{1}{\sqrt{2LC}} \qquad (B.3.b)$$

$$K = \sqrt{\frac{1}{C_N} + 1} \qquad (B.3.c)$$

$$C_N = \frac{2C_D}{N^2 C} \qquad (B.3.d)$$

It should be noted that $C_D/(N/2)^2$ represents the reflected capacitance of the CF switches reflected into the primary. This capacitance is seen in series with switch capacitances C_1 and C_2. which are effectively connected in parallel. Therefore, C_N can be regarded as a ratio of the reflected CF switch capacitance into the primary and total primary switch capacitance, $C_1 + C_2 = 2C$.

Solution:

$$v_{C1}^A = b_A(\cos \omega_O Kt - 1) + a_A \sin \omega_O Kt + \frac{NI_O}{4C_D K^2} t \tag{B.4.a}$$

$$i_{PRIM}^A = \frac{-b_A K}{Z_O} \sin \omega_O Kt + \frac{a_A K}{Z_O} \cos \omega_O Kt + \frac{NI_O C}{2C_D K^2} \tag{B.4.b}$$

$$v_{PRIM}^A = \frac{V_{IN}}{2} + b_A - (1 - K^2)b_A \cos \omega_O Kt - (1 - K^2)a_A \sin \omega_O Kt - \frac{NI_O}{4C_D K^2} t \tag{B.4.c}$$

where

$$a_A = \frac{Z_O}{K} [I_{PRIM}^A - \frac{I_O}{N(1 + C_N)}] \tag{B.5.a}$$

$$b_A = \frac{1}{K^2} [V_{PRIM}^A - \frac{V_{IN}}{2} + V_{C1}^A] \tag{B.5.b}$$

Initial conditions I_{PRIM}^A and V_{PRIM}^A are determined from the stage preceding Stage A. For Modes I.A and II.A, it is Stage D (Eqs. (B.26.a) and (B.26.b)) with negative signs at $t = T_D$). For Modes I.B and II.B, it is Stage AF (Eqs. (B.34.a) and (B.34.b)) with a negative sign at time $t = T_{AF}$).

Normalizing voltages with respect to $V_{IN}/2$, current with respect to I_O/N, and time with respect to $1/f_O$, Eqs. (B.4.a) - (B.4.c) become:

$$v_{C1}^{AN} = b_{AN}(\cos 2\pi K t_N - 1) + \frac{I_{ON}}{2K}\left[I_{PRIM}^{AN} - \frac{1}{1+C_N}\right]\sin 2\pi K t_N + \frac{\pi I_{ON}}{K^2 C_N}t_N \qquad (B.6.a)$$

$$i_{PRIM}^{AN} = -\frac{2K b_{AN}}{I_{ON}}\sin 2\pi K t_N + \left[I_{PRIM}^{AN} - \frac{1}{1+C_N}\right]\cos 2\pi K t_N + \frac{1}{K^2 C_N} \qquad (B.6.b)$$

$$v_{PRIM}^{AN} = \frac{1}{2} + b_{AN} - (1-K^2)b_{AN}\cos 2\pi K t_N - (1-K^2)\frac{I_{ON}}{2K}\left[I_{PRIM}^{AN} - \frac{1}{1+C_N}\right]\sin 2\pi K t_N$$

$$-\frac{\pi I_{ON}}{K^2 C_N}t_N \qquad (B.6.c)$$

where

$$I_{ON} = \frac{2Z_O I_O}{N V_{IN}} \qquad (B.7.a)$$

$$b_{AN} = \frac{1}{K^2}(V_{PRIM}^{AN} - 0.5 + V_{C1}^{AN}) \qquad (B.7.b)$$

Stage Duration $T_A = T_{A1} - T_{AO}$

Stage duration T_A is determined from:

$$v_{C1}(T_A) = V_{IN} \qquad (B.8.a)$$

To solve for T_A, it is necessary to solve a transcendental equation to get the stage duration.

STAGE B [T_{BO}, T_{B1}] (Fig. B.16)

Initial Conditions:

$$v_{C1}(T_{BO}) = V_{IN} \qquad (B.9.a)$$

$$v_{C2}(T_{BO}) = 0 \qquad (B.9.b)$$

$$i_{PRIM}(T_{BO}) = I_{PRIM}^{B} \qquad (B.9.c)$$

$$v_{PRIM}(T_{BO}) = V_{PRIM}^{B} \qquad (B.9.d)$$

$$i_{Q3}(T_{BO}) = I_{Q3}^{B} \qquad (B.9.e)$$

$$i_{Q4}(T_{BO}) = I_{Q4}^{B} \qquad (B.9.f)$$

$$v_{Q3}(T_{BO}) = 0 \qquad (B.9.g)$$

$$v_{Q4}(T_{BO}) = V_{Q4}^{B} \qquad (B.9.h)$$

Equations:

$$v_{PRIM}(t) + L\frac{diPRIM(t)}{dt} = -\frac{V_{IN}}{2} \qquad (B.10.a)$$

$$I_L = I_{PRIM}$$
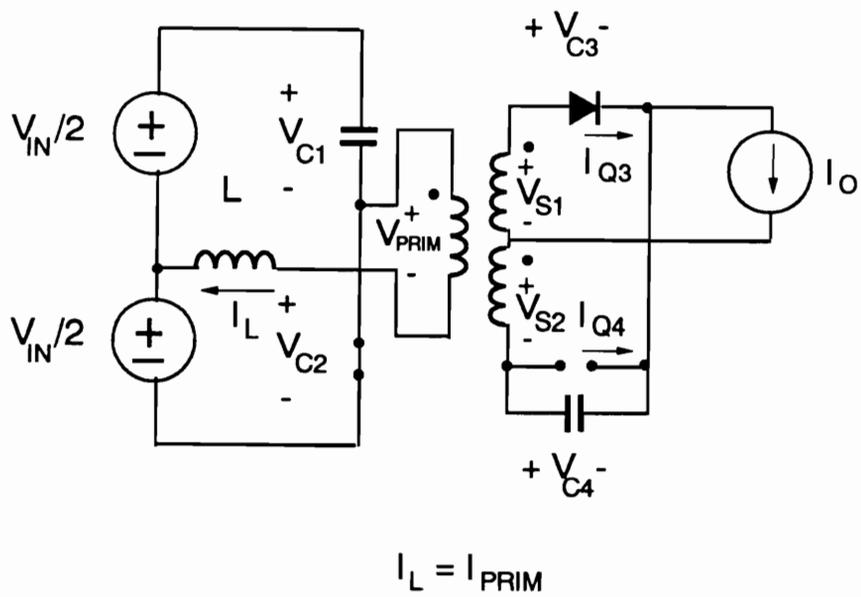
Figure B.16.   Topological Stage B of ideal CF HB ZVS-MRC.

$$i_{PRIM}(t) = \frac{1}{N}\left[i_{Q3}(t) - i_{Q4}(t)\right] \tag{B.10.b}$$

$$i_{Q3}(t) + i_{Q4}(t) = I_O \tag{B.10.c}$$

$$v_{S1}(t) + v_{S2}(t) = -v_{Q4}(t) \tag{B.10.d}$$

$$i_{Q4}(t) = C_D \cdot \frac{dv_{Q4}(t)}{dt} \tag{B.10.e}$$

$$v_{S1}(t) = v_{S2}(t) = \frac{v_{PRIM}(t)}{N} \tag{B.10.f}$$

From Eqs. (B.10.a) - (B.10.f), it follows that:

$$\frac{d^2 v_{PRIM}(t)}{dt^2} + \omega_O^2 C_N^{-1} v_{PRIM}(t) = -\frac{N^2 V_{IN}}{8LC_D} = -\frac{V_{IN}\omega_O^2}{2C_N} \tag{B.11}$$

Solution:

$$v_{PRIM}^B = a_B \cos \omega_O C_N^{-1/2} t - b_B \sin \omega_O C_N^{-1/2} t - \frac{V_{IN}}{2} \tag{B.11.a}$$

$$i_{PRIM}^B = \frac{I_O}{N} + \frac{C_N^{1/2}}{Z_O} (b_B \cos \omega_O C_N^{-1/2} t - a_B \sin \omega_O C_N^{-1/2} t) \tag{B.11.b}$$

where $Z_O = \sqrt{L/2C}$ is the characteristic impedance and

$$a_B = V_{PRIM}^B + \frac{V_{IN}}{2} \qquad (B.12.a)$$

$$b_B = \frac{Z_O}{C_N^{1/2}} \left[I_{PRIM}^B - \frac{I_O}{N} \right] \qquad (B.12.b)$$

or in the normalized form:

$$v_{PRIM}^{BN} = a_{BN} \cos 2\pi C_N^{-1/2} t_N + b_{BN} \sin 2\pi C_N^{-1/2} t_N - \frac{1}{2} \qquad (B.13.a)$$

$$i_{PRIM}^{BN} = 1 + \frac{2C_N^{1/2}}{I_{ON}} (b_{BN} \cos 2\pi C_N^{-1/2} t_N - a_{BN} \sin 2\pi C_N^{-1/2} t_N) \qquad (B.13.b)$$

where

$$a_{BN} = V_{PRIM}^{BN} + \frac{1}{2} \qquad (B.14.a)$$

$$b_{BN} = \frac{I_{ON}}{2C_N^{1/2}} (I_{PRIM}^{BN} - 1) \qquad (B.14.b)$$

Stage Duration $T_B = T_{B1} - T_{BO}$:

$$v_{PRIM}^B(T_B) = 0, \qquad (B.15.a)$$

or

$$i^{B}_{PRIM}(T_B) = -I_O/N. \qquad (B.15.b)$$

STAGE C [T_{CO}, T_{C1}] (Fig. B.17)

Initial Conditions:

$$v_{C1}(T_{CO}) = V_{IN} \qquad (B.16.a)$$

$$V_{C2}(T_{CO}) = 0 \qquad (B.16.b)$$

$$i_{PRIM}(T_{CO}) = I^{C}_{PRIM} \qquad (B.16.c)$$

$$v_{PRIM}(T_{CO}) = 0 \qquad (B.16.d)$$

$$i_{Q3}(T_{CO}) = I^{C}_{Q3} \qquad (B.16.e)$$

$$i_{Q4}(T_{CO}) = I^{C}_{Q4} \qquad (B.16.f)$$

$$v_{Q3}(T_{CO}) = 0 \qquad (B.16.g)$$

$$v_{Q4}(T_{CO}) = 0 \qquad (B.16.h)$$

Equations:

$$I_L = I_{PRIM}$$
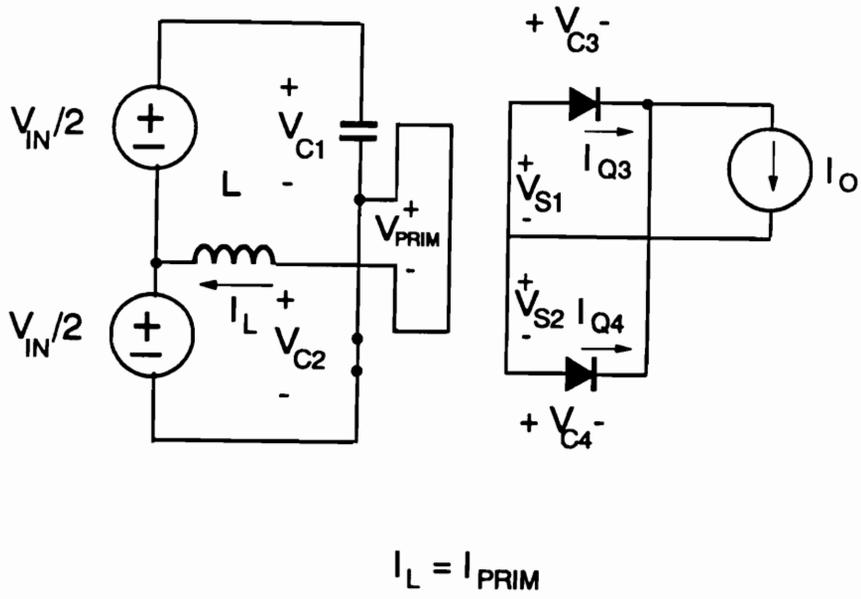
Figure B.17. Topological Stage C of ideal CF HB ZVS-MRC.

$$L \frac{di_{PRIM}(t)}{dt} + \frac{V_{IN}}{2} = 0 \qquad (B.17)$$

Solution:

$$i_{PRIM}^{c} = I_{PRIM}^{c} - \frac{V_{IN}}{2L} t \qquad (B.18)$$

or in the normalized form:

$$i_{PRIM}^{CN} = I_{PRIM}^{CN} - \frac{2\pi}{I_{ON}} t_{N} \qquad (B.19)$$

Stage Duration $T_C = T_{C1} - T_{CO}$:

$$i_{PRIM}^{c}(T_C) = -\frac{I_O}{N} \qquad (B.20)$$

and, from Eq. (B.18), it follows that:

$$T_C = \frac{2L}{V_{IN}} \left[I_{PRIM}^{c} + \frac{I_O}{N} \right] \qquad (B.21)$$

or in the normalized form from Eq. (B.19), it follows that:

$$T_{CN} = \frac{I_{ON}}{2\pi} (I_{PRIM}^{CN} + 1)$$

(B.22)

STAGE D [T_{DO}, T_{D1}] (Fig. B.18)

Initial Conditions:

$$v_{C1}(T_{DO}) = V_{IN}$$

(B.23.a)

$$v_{C2}(T_{DO}) = 0$$

(B.23.b)

$$i_{PRIM}(T_{DO}) = I_{PRIM}^{D}$$

(B.23.c)

$$v_{PRIM}(T_{DO}) = V_{PRIM}^{D}$$

(B.23.d)

$$i_{Q3}(T_{DO}) = I_{Q3}^{D}$$

(B.23.e)

$$i_{Q4}(T_{DO}) = I_{Q4}^{D}$$

(B.23.f)

$$v_{Q3}(T_{DO}) = V_{Q3}^{D}$$

(B.23.g)

$$v_{Q4}(T_{DO}) = 0$$

(B.23.h)

Equations:
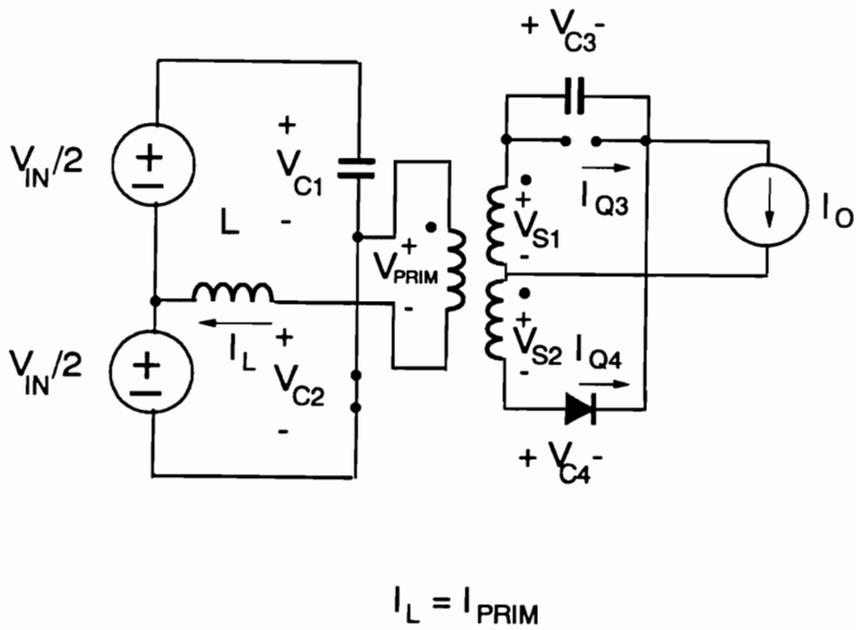
Figure B.18. Topological Stage D of ideal CF HB ZVS-MRC.

$$I_L = I_{PRIM}$$

$$v_{PRIM}(t) + L\,\frac{di_{PRIM}(t)}{dt} = -\frac{V_{IN}}{2} \qquad (B.24.a)$$

$$i_{PRIM}(t) = \frac{1}{N}\,[i_{Q3}(t) - i_{Q4}(t)] \qquad (B.24.b)$$

$$i_{Q3}(t) + i_{Q4}(t) = I_O \qquad (B.24.c)$$

$$v_{PRIM}(t) = \frac{Nv_{Q3}(t)}{2} \qquad (B.24.d)$$

$$i_{Q3}(t) = C_D\,\frac{dv_{Q3}(t)}{dt} \qquad (B.24.e)$$

From Eqs. (B.24.a) - (B.24.e), it follows that:

$$\frac{d^2 v_{PRIM}(t)}{dt^2} + \omega_O^2 C_N^{-1} v_{PRIM}(t) = -\frac{1}{2}\,\omega_O^2 C_N^{-1} V_{IN} \qquad (B.25)$$

Solution:

$$v_{PRIM}^D = a_D \cos \omega_O C_N^{-1/2} t + b_D \sin \omega_O C_N^{-1/2} t - \frac{V_{IN}}{2} \qquad (B.26.a)$$

$$i_{PRIM}^D = -\frac{I_O}{N} + \frac{C_N^{1/2}}{Z_O}\,(b_D \cos \omega_O C_N^{-1/2} t + a_D \sin \omega_O C_N^{-1/2} t) \qquad (B.26.b)$$

where

$$a_D = V_{PRIM}^D + \frac{V_{IN}}{2} \tag{B.27.a}$$

$$b_D = \frac{Z_O}{NC_N^{1/2}} \left[i_{PRIM}^D + \frac{I_O}{N} \right] \tag{B.27.b}$$

or in the normalized form:

$$v_{PRIM}^{DN} = a_{DN} \cos 2\pi C_N^{-1/2} t_N + b_{DN} \sin 2\pi C_N^{-1/2} t_N - \frac{1}{2} \tag{B.28.a}$$

$$i_{PRIM}^{DN} = -1 + \frac{2C_N^{1/2}}{I_{ON}} (b_{DN} \cos 2\pi C_N^{-1/2} t_N - a_{DN} \sin 2\pi C_N^{-1/2} t_N) \tag{B.28.b}$$

where

$$a_{DN} = V_{PRIM}^{DN} + \frac{1}{2} \tag{B.29.a}$$

$$b_{DN} = \frac{I_{ON}}{2C_N^{1/2}} (I_{PRIM}^{DN} + 1) \tag{B.29.b}$$

Stage Duration $T_D = T_{D1} - T_{DO}$

Time duration for this stage is determined by the turn-off of the primary switches. For the half cycle being analyzed, T_d is determined by the turn-off of switch Q_2.

STAGE AF [T_{AFO}, T_{AF1}] (Fig. B.19)

Initial Conditions:

$$v_{C1}(T_{AFO}) = 0 \qquad (B.30.a)$$

$$v_{C2}(T_{AFO}) = V_{IN} \qquad (B.30.b)$$

$$i_{PRIM}(T_{AFO}) = I_{PRIM}^{AF} \qquad (B.30.c)$$

$$V_{PRIM}(T_{AFO}) = 0 \qquad (B.30.d)$$

$$i_{Q3}(T_{AFO}) = I_{Q3}^{AF} \qquad (B.30.e)$$

$$i_{Q4}(T_{AFO}) = I_{Q4}^{AF} \qquad (B.30.f)$$

$$v_{Q3}(T_{AFO}) = 0 \qquad (B.30.g)$$

$$v_{Q4}(T_{AFO}) = 0 \qquad (B.30.h)$$

Equations:
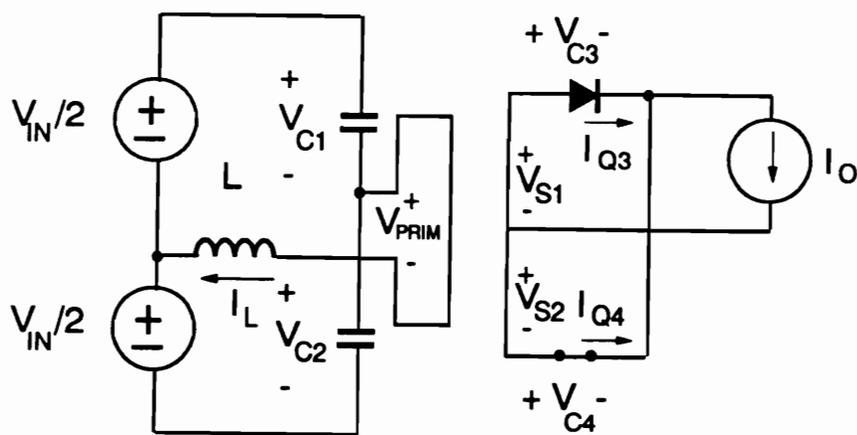
$$I_L = I_{PRIM}$$

Figure B.19.   Topological Stage AF of ideal CF HB ZVS-MRC.

$$v_{C1}(t) + L\,\frac{di_{PRIM}(t)}{dt} = \frac{V_{IN}}{2} \qquad\qquad (B.31.a)$$

$$i_{PRIM}(t) = C_1\,\frac{dv_{C1}(t)}{dt} - C_2\,\frac{dv_{C2}(t)}{dt} = 2C\,\frac{dv_{C1}(t)}{dt} \qquad\qquad (B.31.b)$$

$$i_{PRIM}(t) = \frac{1}{N}\,[i_{Q3}(t) - i_{Q4}(t)] \qquad\qquad (B.31.c)$$

$$i_{Q3}(t) + i_{Q4}(t) = I_O \qquad\qquad (B.31.d)$$

$$v_{S1}(t) = v_{S2}(t) = 0 \qquad\qquad (B.31.e)$$

From Eqs. (B.30.a) - (B.31.e), it follows that:

$$\frac{d^2 v_{C1}(t)}{dt^2} + \omega_O^2\,\frac{dv_{C1}(t)}{dt} = \frac{\omega_O^2 V_{IN}}{2} \qquad\qquad (B.32)$$

Solution:

$$v_{C1}^{AF} = \frac{1}{2}\,[a_{AF}\cos\omega_O t + b_{AF}\sin\omega_O t + V_{IN}] \qquad\qquad (B.33.a)$$

$$i_{PRIM}^{AF} = \frac{1}{2Z_O}\,[b_{AF}\cos\omega_O t - a_{AF}\sin\omega_O t] \qquad\qquad (B.33.b)$$

where

$$a_{AF} = 2(V_{C1}^{AF} - 0.5) \tag{B.34.a}$$

$$b_{AF} = 2I_{PRIM}^{AF}Z_O \tag{B.34.b}$$

or in the normalized form:

$$v_{C1}^{AFN} = \frac{1}{2}\left[1 + a_{AFN}\cos 2\pi t_N + b_{AFN}\sin 2\pi t_N\right] \tag{B.35.a}$$

$$i_{PRIM}^{AFN} = I_{PRIM}^{AFN}\cos 2\pi t_N - \frac{a_{FN}}{I_{ON}}\sin 2\pi t_N \tag{B.35.b}$$

where

$$a_{AFN} = 2(V_{C1}^{AFN} - 0.5) \tag{B.36.a}$$

$$b_{AFN} = I_{PRIM}^{AFN}I_{ON} \tag{B.36.b}$$

Stage Duration $T_{AF} = T_{AF1} - T_{AFO}$

For all modes containing stage AF, the duration of this stage is determined by the turn-off of the CF switch. For the half cycle being analyzed it corresponds to the turn-off of CF switch Q_3.

STAGE BF [T_{BFO}, T_{BF1}] (Fig. B.20)

$$I_L = I_{PRIM}$$
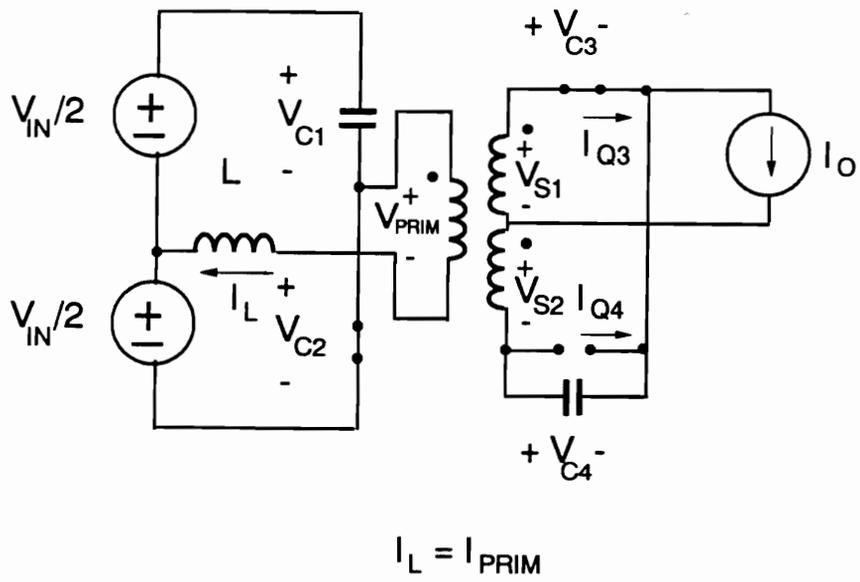
Figure B.20. Topological Stage BF of ideal CF HB ZVS-MRC.

Initial Conditions:

$$v_{C1}(T_{BFO}) = V_{IN} \qquad (B.37.a)$$

$$v_{C2}(T_{BFO}) = 0 \qquad (B.37.b)$$

$$i_{PRIM}(T_{BFO}) = -\frac{I_O}{N}\,just(u2)BF \qquad (B.37.c)$$

$$v_{PRIM}(T_{BFO}) = V_{PRIM}^{BF} \qquad (B.37.d)$$

$$i_{Q3}(T_{BFO}) = I_{Q3}^{BF} \qquad (B.37.e)$$

$$i_{Q4}(T_{BFO}) = I_{Q4}^{BF} \qquad (B.37.f)$$

$$v_{Q3}(T_{BFO}) = 0 \qquad (B.37.g)$$

$$v_{Q4}(T_{BFO}) = V_{Q4}^{BF} \qquad (B.37.h)$$

Equations:

$$v_{PRIM}(t) + L\,\frac{di_{PRIM}(t)}{dt} = -\frac{V_{IN}}{2} \qquad (B.38.a)$$

$$i_{PRIM}(t) = \frac{1}{N}\left[i_{Q3}(t) - i_{Q4}(t)\right] \qquad (B.38.b)$$

$$i_{Q3}(t) + i_{Q4}(t) = I_O \qquad (B.38.c)$$

$$v_{S1}(t) + v_{S2}(t) = -v_{Q4}(t) \qquad (B.38.d)$$

$$i_{Q4}(t) = C_D \frac{dv_{Q4}(t)}{dt} \qquad (B.38.e)$$

$$v_{S1}(t) = v_{S2}(t) = \frac{v_{PRIM}(t)}{N} \qquad (B.38.f)$$

From Eqs. (B.37.a) - (B.38.f), it follows that:

$$\frac{d^2 v_{PRIM}(t)}{dt^2} + \omega_O^2 C_N^{-1} v_{PRIM}(t) = -\frac{N^2 V_{IN}}{8LC_D} = -\frac{V_{IN}\omega_O^2}{2C_N} \qquad (B.39)$$

Solution:

$$v_{PRIM}^{BF} = a_{BF} \cos \omega_O C_N^{-1/2} t - b_{BF} \sin \omega_O C_N^{-1/2} t - \frac{V_{IN}}{2} \qquad (B.40.a)$$

$$i_{PRIM}^{BF} = \frac{I_O}{N} + \frac{C_N^{1/2}}{Z_O}(b_{BF} \cos \omega_O C_N^{-1/2} t - a_{BF} \sin \omega_O C_N^{-1/2} t) \qquad (B.40.b)$$

where

$$a_{BF} = V_{PRIM}^{BF} + \frac{V_{IN}}{2} \tag{B.41.a}$$

$$b_{BF} = \frac{Z_O}{C_N^{1/2}} \left[\, - \frac{2I_O}{N} \, \right] \tag{B.41.b}$$

or in the normalized form:

$$v_{PRIM}^{BFN} = a_{BFN} \cos 2\pi C_N^{-1/2} t_N + b_{BFN} \sin 2\pi C_N^{-1/2} t_N - \frac{1}{2} \tag{B.42.a}$$

$$i_{PRIM}^{BFN} = 1 + \frac{2C_N^{1/2}}{I_{ON}} (b_{BFN} \cos 2\pi C_N^{-1/2} t_N - a_{BFN} \sin 2\pi C_N^{-1/2} t_N) \tag{B.42.b}$$

where

$$a_{BFN} = V_{PRIM}^{BFN} + \frac{1}{2} \tag{B.43.a}$$

$$b_{BFN} = \frac{I_{ON}}{C_N^{1/2}} \tag{B.43.b}$$

Stage Duration $T_{BF} = T_{BF1} - T_{BFO}$:

$$v_{PRIM}^{BF}(T_{Bf}) = 0 \tag{B.44}$$

STAGE CF [T_{CFO}, T_{CF1}] (Fig. B.21)

Initial Conditions:

$$v_{C1}(T_{CFO}) = V_{IN} \tag{B.45.a}$$

$$v_{C2}(T_{CFO}) = 0 \tag{B.45.b}$$

$$i_{PRIM}(T_{CFO}) = I_{PRIM}^{CF} \tag{B.45.c}$$

$$v_{PRIM}(T_{CFO}) = 0 \tag{B.45.d}$$

$$i_{Q3}(T_{CFO}) = I_{Q3}^{CF} \tag{B.45.e}$$

$$i_{Q4}(T_{CFO}) = I_{Q4}^{CF} \tag{B.45.f}$$

$$v_{Q3}(T_{CFO}) = 0 \tag{B.45.g}$$

$$v_{Q4}(T_{CFO}) = 0 \tag{B.45.h}$$

Equations:

$$L \frac{di_{PRIM}(t)}{dt} + \frac{V_{IN}}{2} = 0 \tag{B.46}$$

Solution:

$$I_L = I_{PRIM}$$
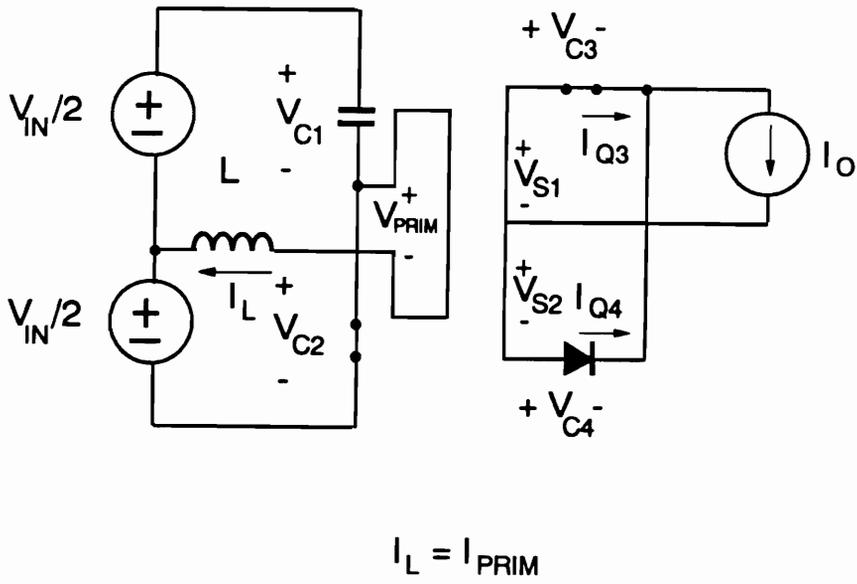
Figure B.21. Topological Stage CF of ideal CF HB ZVS-MRC.

$$i_{PRIM}^{CF} = I_{PRIM}^{CF} - \frac{V_{IN}}{2L}\,t \qquad\qquad (B.47)$$

or in the normalized form:

$$i_{PRIM}^{CFN} = I_{PRIM}^{CFN} - \frac{2\pi}{I_{ON}}\,t_N \qquad\qquad (B.48)$$

Stage Duration $T_{CF} = T_{C1} - T_{CO}$

The duration of this stage is determined by the turn-off of the CF switch when the converter operates in either Mode I.A or Mode II.A. The CF switch can be either switch Q_3 or Q_4 depending on whether this topological stage occurs before or after Stage C. If Stage CF occurs before Stage C, T_{CF} will be determined by the turn-off of switch Q_4; and if Stage CF occurs after Stage C, T_{CF} is determined by the turn-off of switch Q_3. For Modes I.B, I.C, II.B, and II.C the time duration T_{CF} is determined by the turn-off of the primary switches Q_1 and Q_2 (operation for negative δ).

B.4 Calculating the DC Voltage-Conversion-Ratio
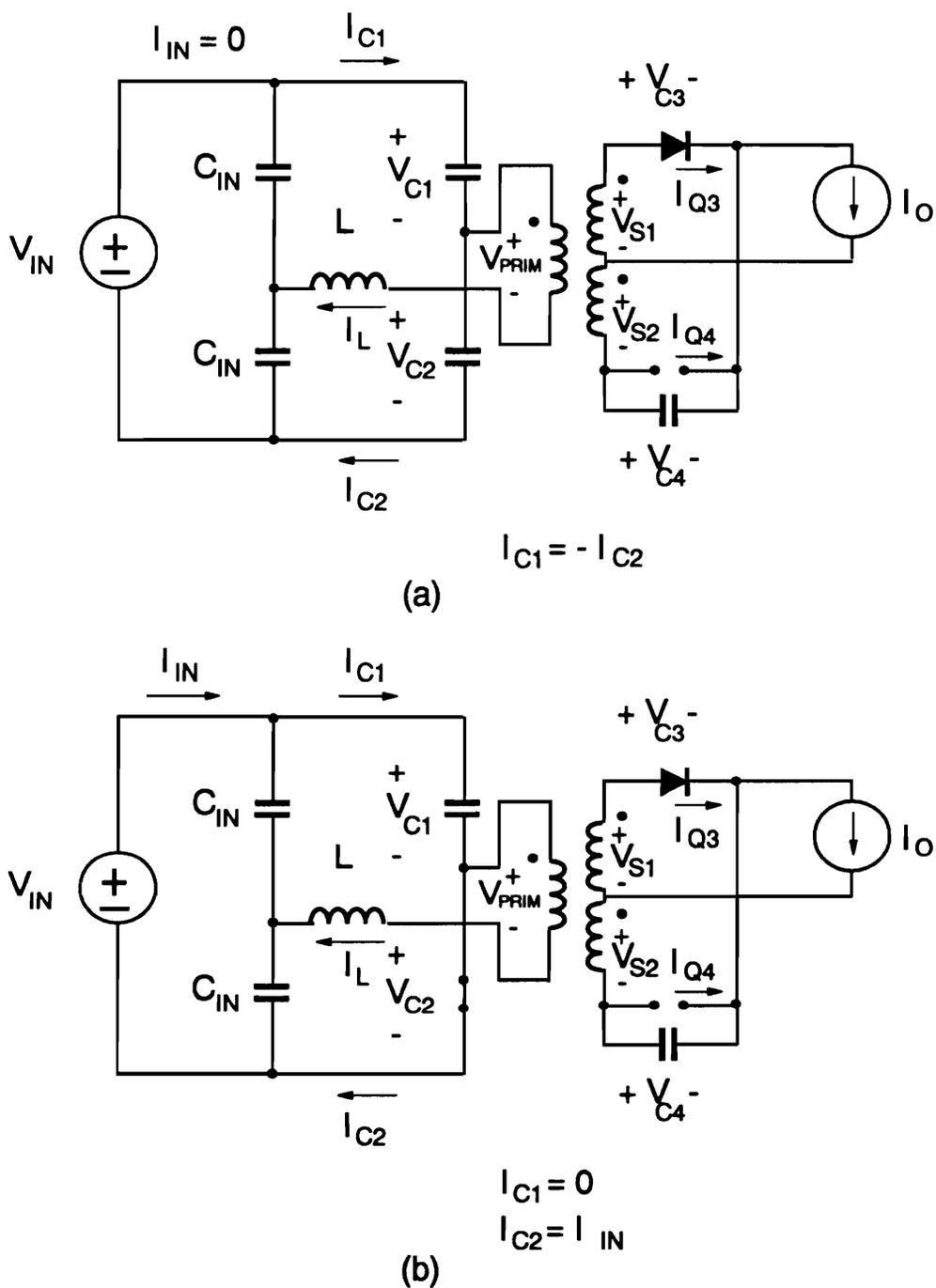
Figure B.22. Circuit representation of the primary of the HB during:
(a) switching transition;
(b) non-switching operation.

As shown in [D8], in the HB ZVS-MRC the source delivers power only during stages when the primary switch capacitors do not carry current. This conclusion is also valid for the CF HB ZVS-MRC. Therefore, in a CF HB ZVS-MRC, the power is delivered in all stages except Stages A, AF, and E.

The equivalent circuit of the primary side of the converter during the inductor-discharging stages is shown in Fig. B.22. In the circuit configuration of Fig. B.22(b) there is no change in the voltage across the resonant capacitors ($V_{C1} = V_{IN}$, $V_{C1} = 0$); there is no current flowing through these capacitors either. Thus, from Fig. B.22(b), it follows that:

$$i_{SS}(t) = -\frac{i_{PRIM}(t)}{2} \qquad (B.49)$$

Therefore, the input energy during one conversion cycle (T_{CON}) is given by

$$E_{inp} = \frac{1}{2} \int_0^{T_{CON}} V_{IN} i_{PRIM}(t) dt \qquad (B.50)$$

whereas, the output energy during a conversion cycle is

$$E_{out} = V_O I_O T_{CON} \qquad (B.51)$$

Expression for the dc voltage-conversion-ratio is obtained by first substituting the expressions for the primary currents in Stage B (Eq. B.11.b), Stage C (Eq. B.18), Stage D (Eq. B.26.b), Stage BF (Eq. B.43.b), and Stage CF (Eq. B.48), into equation B.53 and integrating it. The rsulting expression is then equated to equation B.54. In the normalized form, the following relation is then obtained:

$$\frac{V_O}{V_{IN}/(2N)} = 1 - f_{con}[T_{AN} + T_{A\Gamma N} + 2T_{BN} + 2T_{BFN} + T_{CF1N} + T_{CF2N}$$

$$+ (i_{PRIM}^{CN} + 1)\frac{T_{CN}}{2} + (i_{PRIM}^{CF1N} + i_{PRIM}^{DN})\frac{T_{CF1N}}{2} + (i_{PRIM}^{CF2N} + i_{PRIM}^{BFN})\frac{T_{CF2N}}{2}$$

$$+ \frac{C_N}{\pi I_{ON}}[b_{BN}\sin 2\pi C_N^{-1/2}(T_{BN} + T_{BFN}) - a_{BN}(1 - \cos 2\pi C_N^{-1/2}(T_{BN} + T_{BFN}))]$$

$$+ \frac{C_N}{\pi I_{ON}}(b_{DN}\sin 2\pi C_N^{-1/2}T_{DN} - a_{DN}(1 - \cos 2\pi C_N^{-1/2}T_{DN}))] \qquad (B.52)$$

To calculate the dc voltage-conversion-ratio, it is necessary to find the duration of the different topological stages. Since it requires solving transcendental equations, the voltage-conversion-ratio can only be computed using a numerical procedure. A FORTRAN program was used to calculate the dc voltage-conversion-ratio.

Appendix C. Analysis of HB ZVS-MRC (L_M)

The circuit diagram of the HB ZVS-MRC (L_M) is shown in Fig. C.1. Capacitances C_1, C_2, C_3, and C_4 are resonant capacitances, and L_1, L_2. and L_M are the resonant inductors of the converter. Since the junction capacitance of the rectifier diodes is not sufficiently large to obtain the desired resonance, capacitors C_3 and C_4 are usually externally added capacitors.

C.1 DC Analysis

To simplify the analysis of the HB ZVS-MRC (L_M). it is assumed that:

a) the output filter inductance is sufficiently large so that it can be approximated by a current source with a value equal to the output current, I_O;
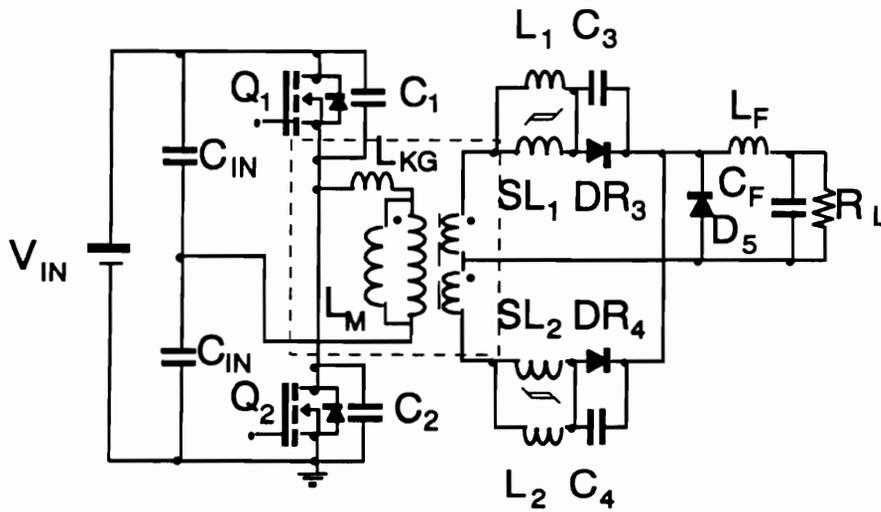
Figure C.1.   Soft switched half-bridge (HB ZVS-MRC (L_M)).

b) the voltage drops across the conducting semiconductor switches (MOSFETs and diodes) are negligible;

c) the switching times of the semiconductor switches are zero;

d) transformer leakage inductance is negligible;

e) $C = C_1 = C_2$; $C_D = C_3 = C_4$; and $L = L_1 = L_2$:

f) the saturable inductors, SL_1 and SL_2, are identical;

g) the slope of the saturable inductance SL_1 and SL_2 is defined by the ratio L/SL (ratio of the linear inductance to saturable inductance); and

h) the current through the linear inductor L at the time the corresponding saturable inductor saturates is I_{SAT} as shown in Fig. C.2(b).

The representation of the saturable inductor is shown in Fig. C.2(a). The reactors block all current when not saturated. Once saturated, it behaves like an inductor with very low inductance.

During a switching cycle, the converter enters a sequence of seven or eight topological stages during heavy load and light load operation, respectively. Again, each sequence of topological stages represents a different mode of operation. Figure C.3 shows the different possible topological stages.

The operation of the soft switched HB converter can be classified into four major modes of operation. The first three modes occur for heavy load operation, while the fourth mode is characteristic of light load operation. Light load operation is not considered essential to the design of the converter and will not be discussed in detail.
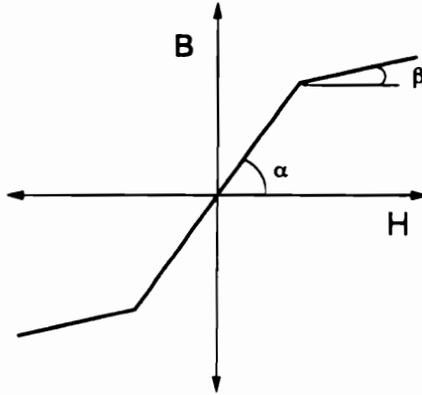
$$\beta = \text{Slope in Saturated Region}$$

$$\alpha = \text{Slope in Linear Region}$$

$$\text{L/SL} = \frac{\alpha}{\beta}$$

(a)
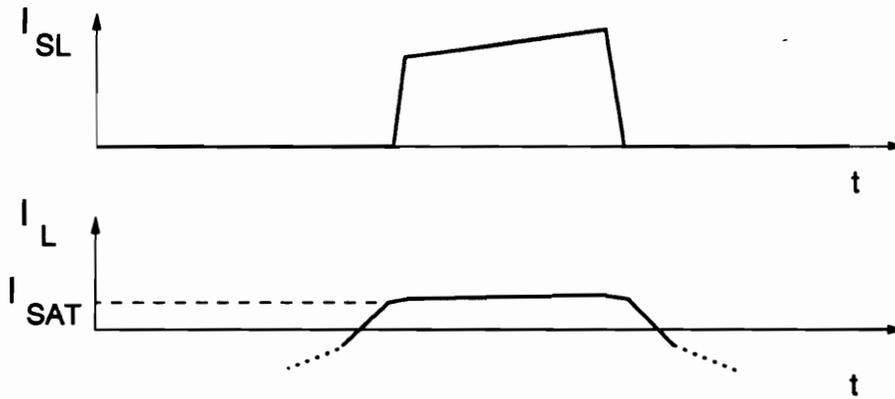
(b)

Figure C.2. (a) Representation of the saturable inductor for dc analysis; (b) Current through the linear and saturable inductor with SL saturated.
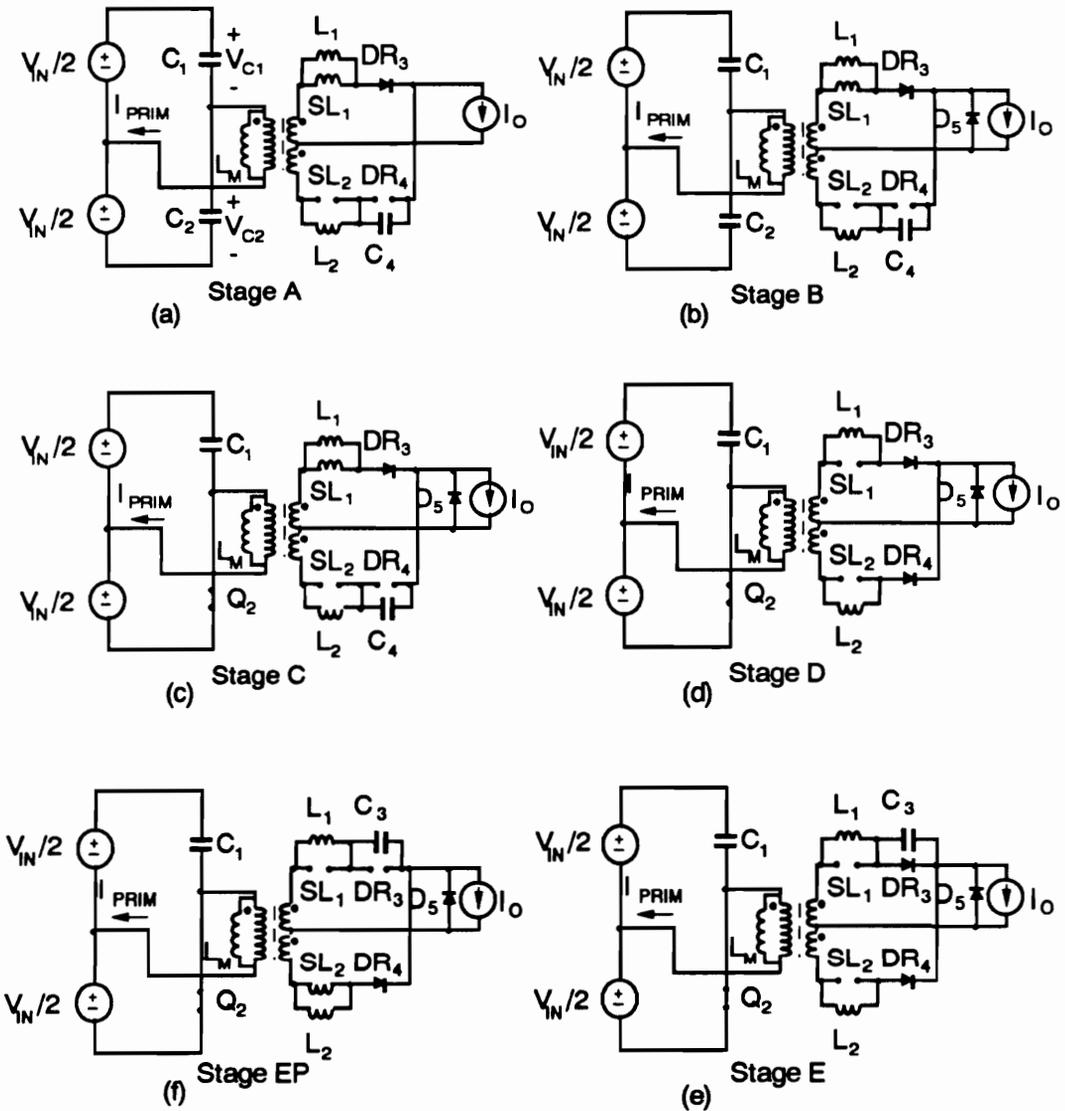
Figure C.3a. Topological stage of the HB ZVS-MRC (L_M):
(a) Stage A, (b) Stage B, (c) Stage C, (d) Stage D, (e) Stage E, and (f) Stage EP.
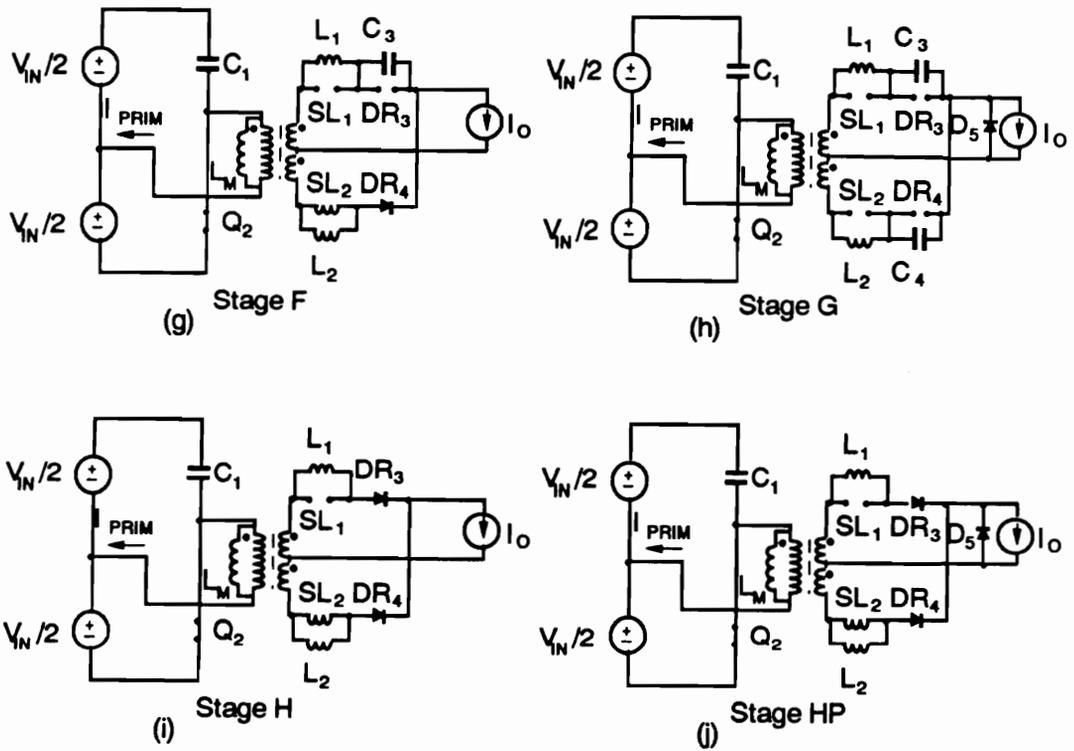
Figure C.3b. Topological stage of the HB ZVS-MRC (L_M):
(g) Stage F, (h) Stage G, (i) Stage H, and (j) Stage HP.
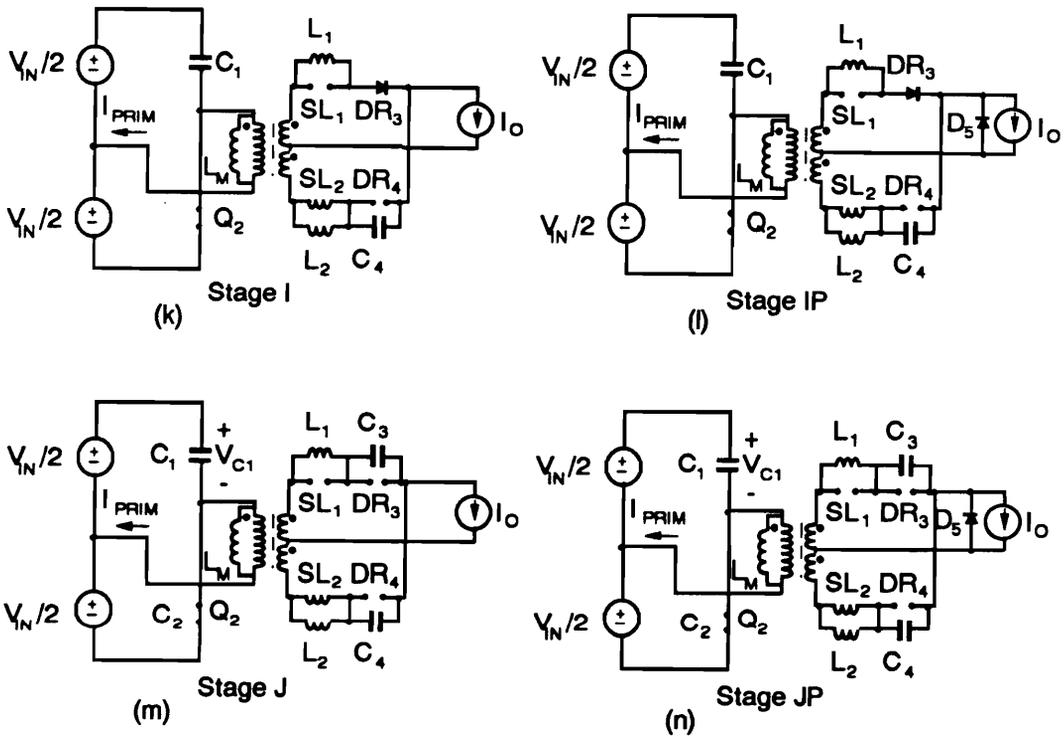
Figure C.3c. Topological stage of the HB ZVS-MRC (L_M):
(k) Stage I, (l) Stage IP, (m) Stage J, and (n) Stage JP.

C.1.1 Mode I of Operation

Mode I.A

The sequence of topological stages for Mode I.A is A-B-C-D-HP-H-F. Figure C.4 shows the key waveforms of the soft switched HB operating on this mode.

Prior to the turn-off of switch Q_1, load current I_O flows through the upper secondary and the primary current flows through Q_1. Voltage across C_1, V_{C1}, is zero, and voltage across C_2, V_{C2}, is equal to the supply voltage V_{IN}. Inductor SL_1 is saturated, whereas inductor SL_2 is unsaturated.

Stage A [T_O, T_1], Fig. C.3(a)

At $t = T_O$, Q_1 is turned off, and the primary current is diverted into C_1 and C_2. Capacitance C_1 starts charging while, C_2 starts discharging at the same rate. Inductor SL_1 remains saturated, and rectifier DR_3 continues to conduct. In this stage, inductor SL_2 is blocking and capacitance C_4 resonates with inductor L_2. The stage ends at time T_1 when primary voltage becomes zero, i.e.. $V_{C1}(T_1) = V_{C2}(T_1) = V_{IN}/2$.

Stage B [T_1, T_2], Fig. C.3(b)

In Stage B, capacitances C_1 and C_2 start to resonate with the magnetizing inductance of the power transformer and the negative primary voltage begins to reset SL_1. The current through SL_1 decreases quickly as the saturable reactor becomes unsaturated. Capacitance C_1 con-

Figure C.4a. Ideal waveforms of the HB ZVS-MRC (L_M) operating in Mode I.A, from top to bottom: gate-source voltage V_{G1}, gate-source voltage V_{G2}, switch Q_1 voltage V_{C1}, switch Q_2 voltage V_{C2}, primary current I_{PRIM}, saturable inductor current I_{SL2}, linear inductor current I_{L2}, linear inductor current I_{L1}, and rectifier capacitor voltage V_{C4}.
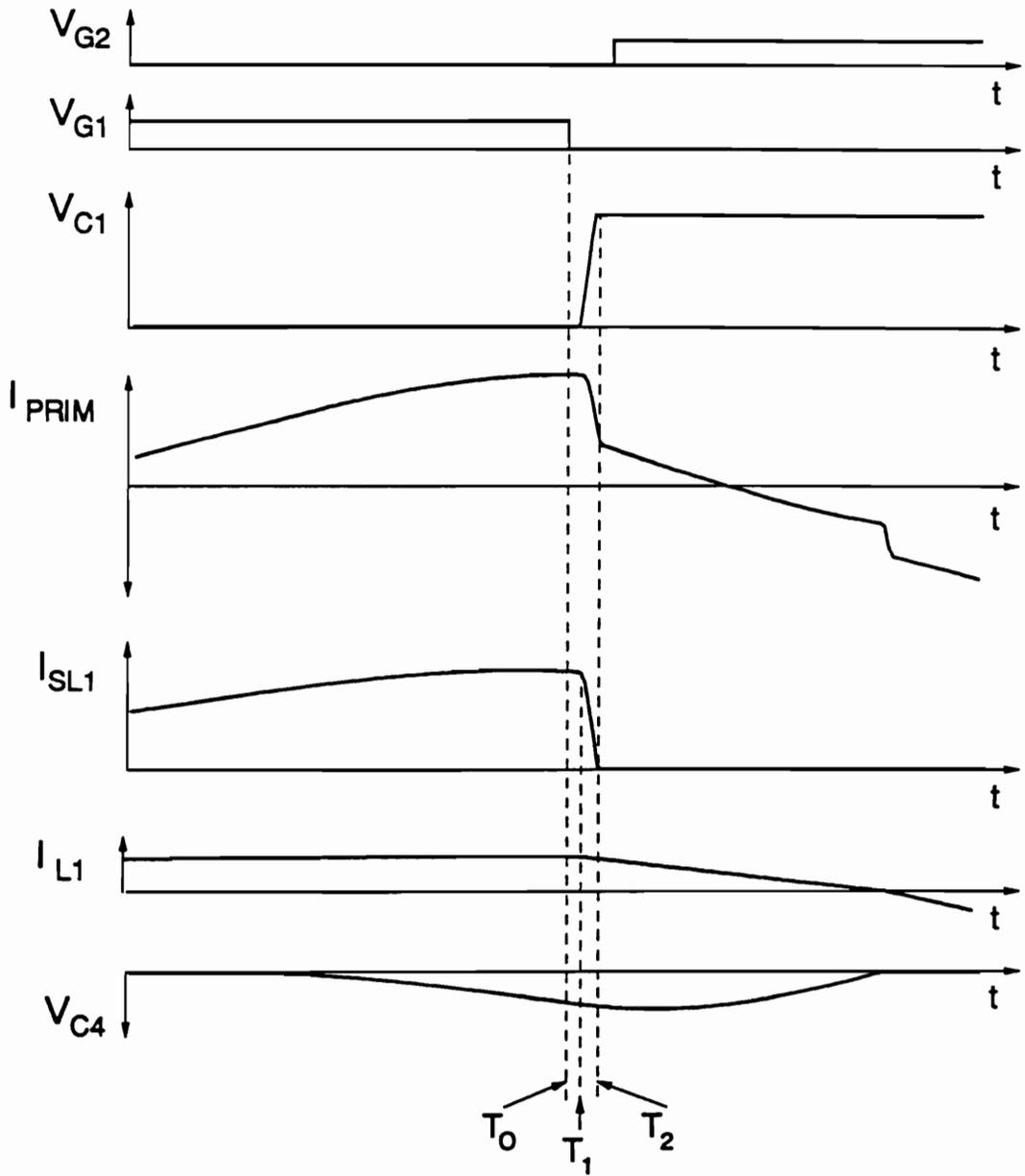
Figure C.4b. Ideal waveforms of the HB ZVS-MRC (L_M) operating in Mode I.A; switching transitionn [$T_O - T_2$], from top to bottom: gate-source voltage V_{G1}, gate-source voltage V_{G2}, switch Q_1 voltage V_{C1}, switch Q_2 voltage V_{C2}, primary current I_{PRIM}, saturable inductor current I_{SL2}, linear inductor current I_{L2}, linear inductor current I_{L1}, and rectifier capacitor voltage V_{C4}.

tinues to charge, and C_2 continues to discharge. At the beginning of Stage B most of the load current is diverted to the freewheeling diode. However, rectifier DR_3 continues to conduct since a small, positive current (5-10 % of the load current) flows through inductor L_1. The current through L_1 decreases to zero due to the negative voltage across the upper secondary. At the same time, inductor L_2 and capacitor C_4 continue to resonate. This stage ends at time T_2 when the voltage across capacitor C_2 becomes zero, and the antiparallel diode of Q_2 starts conducting. Switch Q_2 should be turned on while its antiparallel diode is conducting to achieve ZVS.

Stage C [T_2, T_3], Fig. C.3(c)

During Stage C, inductor L_1 continues to discharge, inductor L_2 and capacitor C_4 continue to resonate, and saturable inductor SL_1 continues to reset. During this stage, the current through SL_1 decreases to zero. Since the the negative voltage across the upper secondary is constant ($- V_{IN}/N$), current through L_1 decreases linearly. Also, the freewheeling diode continues to conduct. This stage ends at time T_3 when the voltage across capacitor C_4 resonates to zero and rectifier DR_4 turns on.

Stage D [T_3, T_4], Fig. C.3(d)

In Stage D, both saturable inductors are blocking. Current through L_1 continues to decrease and current through inductor L_2 increases linearly. The freewheeling diode continues to carry most of the load current. This stage ends at time T_4 when inductor SL_2 saturates.

Stage HP [T_4, T_5], Fig. C.3(d)

In Stage HP, the current through the saturable inductor SL_2 increases rapidly since this inductor is saturated. The freewheeling diode continues to conduct until the current through SL_2 is large enough to supply the load. The current through L_1 continues to increase and the current through L_2 to decrease in a linear manner. Stage HP ends when the sum of the current through L_1, L_2, and SL_2 equals the load current there by turning the freewheeling diode off.

Stage H [T_5, T_6], Fig. C.3(d)

In this stage, the load current is supplied by saturable inductor SL_2. The current through L_1 continues to linearly decrease and the current through L_2 and SL_2 increases also in a linear manner. This stage ends at time T_6 when the current through L_1 decreases to zero and diode DR_3 turns off.

Stage F [T_6, T_7], Fig. C.3(f)

In Stage F, inductor SL_1 continues to block, and capacitor C_3 begins resonating with inductor L_1. Inductor SL_2 remains saturated and most of the load current flows through SL_2. This stage ends when switch Q_2 is turned off. initiating a new conversion cycle.

Mode I.B

The sequence of topological stages for Mode I.B is A-B-C-D-HP-EP-F. Figure C.5 shows the key waveforms of the soft switched HB operating on this mode.
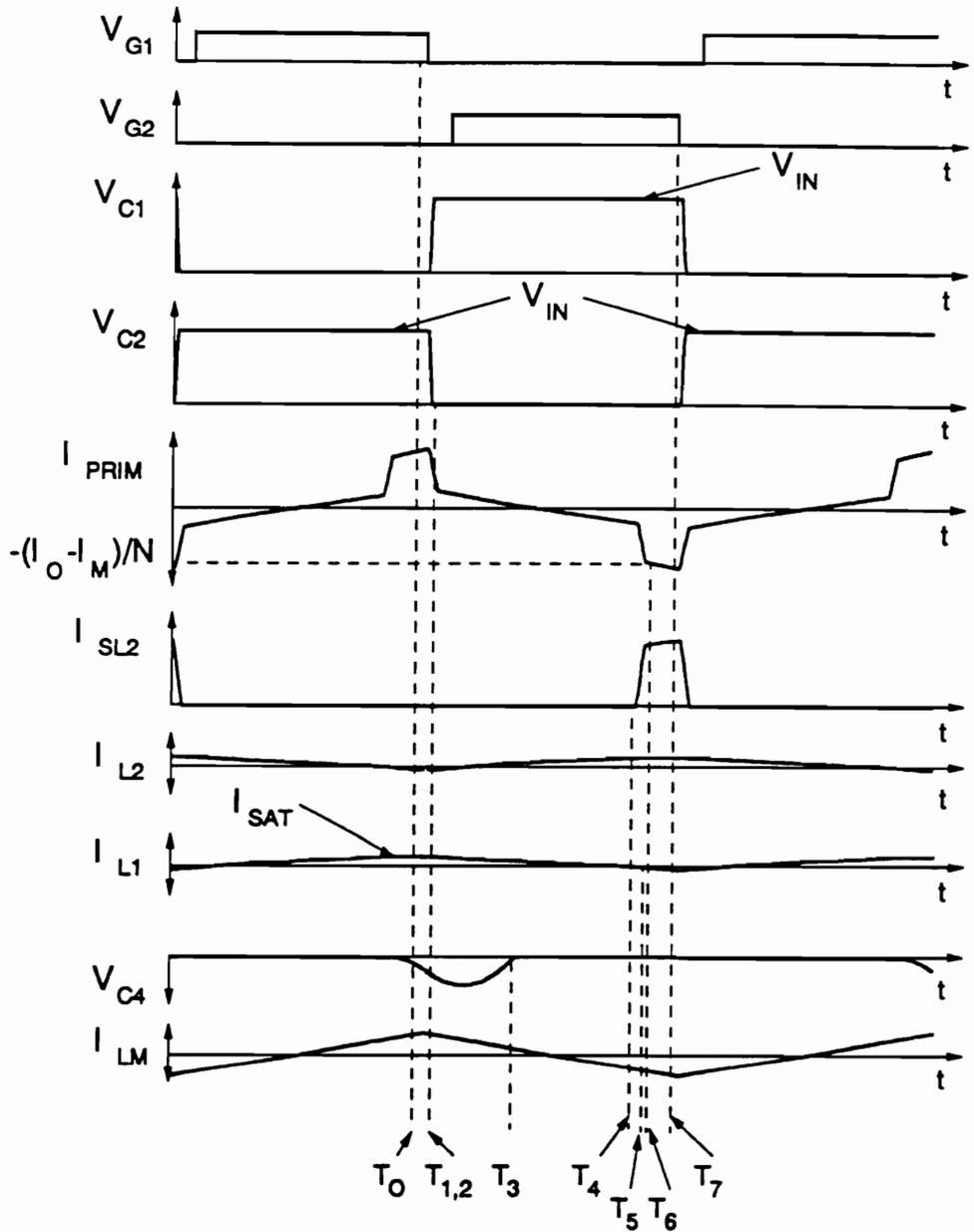
Figure C.5. Ideal waveforms of the HB ZVS-MRC (L_M) operating in Mode I.B, from top to bottom: gate-source voltage V_{G1}, gate-source voltage V_{G2}, switch Q_1 voltage V_{C1}, switch Q_2 voltage V_{C2}, primary current I_{PRIM}, saturable inductor current I_{SL2}, linear inductor current I_{L2}, linear inductor current I_{L1}, and rectifier capacitor voltage V_{C4}.

Prior to the turn-off of switch Q_1, load current I_O flows through the upper secondary and the primary current flows through Q_1. Voltage across C_1, V_{C1}, is zero, and voltage across C_2, V_{C2}, is equal to the supply voltage V_{IN}. Inductor SL_1 is saturated, whereas inductor SL_2 is unsaturated.

Stage A [T_O, T_1], Fig. C.3(a)

At $t = T_O$, Q_1 is turned off, and the primary current is diverted into C_1 and C_2. Capacitance C_1 starts charging and C_2 starts discharging at the same rate. Inductor SL_1 remains saturated, and rectifier DR_3 continues to conduct. In this stage, inductor SL_2 continues to block and capacitance C_4 resonates with inductor L_2. The stage ends at time T_1 when primary voltage becomes zero, i.e., $V_{C1}(T_1) = V_{C2}(T_1) = V_{IN}/2$.

Stage B [T_1, T_2], Fig. C.3(b)

In Stage B, capacitances C_1 and C_2 start to resonate with the magnetizing inductance of the power transformer since the negative primary voltage resets SL_1. The current through SL_1 decreases quickly as the saturable reactor becomes unsaturated. Capacitance C_1 continues to charge, and C_2 continues to discharge. At the beginning of Stage B, most of the load current is diverted to the freewheeling diode. The current through L_1 decreases to zero due to the negative voltage across the upper secondary. At the same time, inductor L_2 and capacitor C_4 continue to resonate. This stage ends at time T_2 when the voltage across capacitor C_2 becomes zero, and the antiparallel diode of Q_2 starts conducting. Switch Q_2 should be turned on while its antiparallel diode is conducting to achieve lossless switching.

Stage C [T_2, T_3], Fig. C.3(c)

During Stage C, inductor L_1 continues to discharge, inductor L_2 and capacitor C_4 continue to resonate, and saturable inductor SL_1 continues to reset. During this stage, the current through SL_1 decreases to zero. Since the the negative voltage across the upper secondary is constant $(-V_{IN}/N)$, current through L_1 decreases linearly. Also, the freewheeling diode continues to conduct. This stage ends at time T_3 when the voltage across capacitor C_4 completely discharges and rectifier DR_4 turns on.

Stage D $[T_3, T_4]$, Fig. C.3(d)

In Stage D, both saturable inductors are unsaturated and the current through L_1 continues to linearly decrease and at the same time the current through inductor L_2 increases linearly. The freewheeling diode continues to carry most of the load current. This stage ends at time T_4 when inductor SL_2 saturates.

Stage HP $[T_4, T_5]$, Fig. C.3(j)

In Stage HP, the current through the saturable inductor SL_2 increases rapidly since SL_2 is saturated, but this current is still not large enough to supply the load, therfore, the freewheeling diode continues to conduct. The current through L_1 continues to increase and the current through L_2 decreases linearly. This stage ends at time T_5 when the current L_1 decreases to zero and diode DR_3 turns off.

Stage EP $[T_5, T_6]$, Fig. C.3(f)

In stage EP, inductor SL_1 continues to reset and capacitor C_3 is charged in a resonant manner through inductor L_1. Inductor SL_2 remains saturated and the freewheeling diode continues to conduct. Stage EP ends when the sum of the current through L_1, L_2, and SL_2 increase to the value of the load current, thereby turning the freewheeling diode off.

Stage F [T_6, T_7], Fig. C.3(g)

In Stage F, inductor SL_1 remains unsaturated and capacitor C_3 continues to resonate with inductor L_1. Inductor SL_2 remains saturated, and most of the load current flows through SL_2. This stage ends when switch Q_2 is turned off, initiating a new conversion cycle.

Mode I.C

The sequence of topological stages for Mode I.C is A-B-C-D-E-EP-F. Figure C.6 shows the key waveforms of the soft switched HB operating on this mode.

Prior to the turn-off of switch Q_1, load current I_O flows through the upper secondary and the primary current flows through Q_1. Voltage across C_1, V_{C1}, is zero, and voltage across C_2, V_{C2}, is equal to the supply voltage V_{IN}. Inductor SL_1 is saturated, whereas inductor SL_2 is unsaturated.

Stage A [T_O, T_1], Fig. C.3(a)

At $t = T_O$, Q_1 is turned off, and the primary current is diverted into C_1 and C_2. Capacitance C_1 starts charging while C_2 starts discharging at the same rate. Inductor SL_1 remains saturated, and rectifier DR_3 continues to conduct. In this stage, inductor SL_2 blocks all current and

Figure C.6. Ideal waveforms of the HB ZVS-MRC (L_M) operating in Mode I.C, from top to bottom: gate-source voltage V_{G1}, gate-source voltage V_{G2}, switch Q_1 voltage V_{C1}, switch Q_2 voltage V_{C2}, primary current I_{PRIM}, saturable inductor current I_{SL2}, linear inductor current I_{L2}, linear inductor current I_{L1}, and rectifier capacitor voltage V_{C4}.

capacitance C_4 resonates with inductor L_2. The stage ends at time T_1 when primary voltage becomes zero, i.e., $V_{C1}(T_1) = V_{C2}(T_1) = V_{IN}/2$.

Stage B [T_1, T_2], Fig. C.3(b)

In Stage B, capacitances C_1 and C_2 start to resonate with the magnetizing inductance of the power transformer since the negative primary voltage resets SL_1. The current through SL_1 decreases quickly as the saturable reactor becomes unsaturated. Capacitance C_1 continues to charge and C_2 continues to discharge. Most of the load current is diverted into the free-wheeling diode. The current through L_1 decreases to zero and inductor L_2 and capacitor C_4 continue to resonate. This stage ends at time T_2 when the voltage across capacitor C_2 becomes zero, and the antiparallel diode of Q_2 starts conducting. Switch Q_2 should be turned on while its antiparallel diode is conducting to achieve ZVS.

Stage C [T_2, T_3], Fig. C.3(c)

During Stage C, inductor L_1 continues to discharge, inductor L_2 and capacitor C_4 continue to resonate, and saturable inductor SL_1 is resetting. During this stage, the current through SL_1 decreases to zero. Since the the negative voltage across the upper secondary is constant ($-V_{IN}/N$), current through L_1 decreases linearly. Also, the freewheeling diode continues to conduct. This stage ends at time T_3 when the voltage across capacitor C_4 completely discharges and rectifier DR_4 turns on.

Stage D [T_3, T_4], Fig. C.3(d)

In Stage D, both saturable inductors are unsaturated, and current through L_1 continues to linearly decrease. At the same time the current through inductor L_2 increases linearly. The freewheeling diode continues to carry most of the load current. This stage ends at time T_4 when the current through L_1 decreases to zero turning diode DR_3 off.

Stage E [T_4, T_5], Fig. C.3(e)

In Stage E, inductor SL_1 continues to reset and capacitor C_3 resonates with inductor L_1. Inductor SL_2 is saturated and the current through SL_2 and L_2 increases linearly. This stage ends at time T_6 when the current through L_2 increases to I_{SAT} and SL_2 saturates.

Stage EP [T_5, T_6], Fig. C.3(f)

In stage EP, inductor SL_1 continues to reset and capacitor C_3 begins to resonate with inductor L_1. Inductor SL_2 remains saturated and the freewheeling diode continues to conduct. Stage EP ends when the sum of the current through L_1, L_2, and SL_2 increases to the value of the load current at which point the freewheeling diode is turned off.

Stage F [T_6, T_7], Fig. C.3(g)

In Stage F, inductor SL_1 is unsaturated and capacitor C_3 resonates with inductor L_1. Inductor SL_2 remains saturated, and most of the load current flows through SL_2. This stage ends when switch Q_2 is turned off, initiating a new conversion cycle.

C.1.2 Mode II of Operation

In Mode II of operation the current through the linear inductor L_1 decreases to zero, turning off rectifier diode DR_3 before capacitor C_4 completely discharges to zero. The change in polarity of the current through L_1 initiates the resonance between this inductance and rectifier capacitance C_3. In this mode. rectifier capacitances C_3 and C_4 will both resonate with the linear inductors at the same time. Mode II results in higher dc-voltage-conversion-ratios compared to Mode I.

Mode II.A

The sequence of topological stages for Mode II.A is A-B-C-G-JP-EP-F. Figure C.7 shows the key waveforms of this converter operating on this mode.

Prior to the turn-off of switch Q_1, load current I_O flows through the upper secondary and the primary current flows through Q_1. Voltage across C_1 , V_{C1}, is zero, and voltage across C_2, V_{C2}, is equal to the supply voltage V_{IN}. Inductor SL_1 is saturated, whereas inductor SL_2 is unsaturated.

Stage A [T_O, T_1], Fig. C.3(a)

At $t = T_O$, Q_1 is turned off, and the primary current is diverted into C_1 and C_2. Capacitance C_1 starts charging and C_2 starts discharging at the same rate. Inductor SL_1 remains saturated, and rectifier DR_3 continues to conduct. In this stage, inductor SL_2 is continues to reset and

Figure C.7. Ideal waveforms of the HB ZVS-MRC (L_M) operating in Mode II.A, from top to bottom: gate-source voltage V_{G1}, gate-source voltage V_{G2}, switch Q_1 voltage V_{C1}, switch Q_2 voltage V_{C2}, primary current I_{PRIM}, saturable inductor current I_{SL2}, linear inductor current I_{L2}, linear inductor current I_{L1}, and rectifier capacitor voltage V_{C4}.

capacitance C_4 resonates with inductor L_2. The stage ends at time T_1 when primary voltage becomes zero, i.e., $V_{C1}(T_1) = V_{C2}(T_1) = V_{IN}/2$.

Stage B [T_1, T_2], Fig. C.3(b)

In Stage B, capacitances C_1 and C_2 start to resonate with the magnetizing inductance of the power transformer since the negative primary voltage resets SL_1. The current through SL_1 decreases quickly as the saturable reactor unsaturates. Capacitance C_1 continues to charge, and C_2 continues to discharge. Most of the load current flows through the freewheeling diode. The current through L_1 decreases to zero due to the negative voltage across the upper secondary. At the same time, inductor L_2 and capacitor C_4 continue to resonate. This stage ends at time T_2 when the voltage across capacitor C_2 becomes zero and the antiparallel diode of Q_2 starts conducting. Switch Q_2 should be turned on while its antiparallel diode is conducting to achieve ZVS.

Stage C [T_2, T_3], Fig. C.3(c)

During Stage C, inductor L_1 continues to discharge, inductor L_2 and capacitor C_4 continue to resonate, and saturable inductor SL_1 continues to reset. During this stage, the current through SL_1 decreases to zero. Since the the negative voltage across the upper secondary is constant ($-V_{IN}/N$), current through L_1 decreases linearly. Also, the freewheeling diode continues to conduct. This stage ends at time T_3 when the current flowing through linear inductor L_1 decreases linearly to zero turning diode DR_3 off.

Stage G [T_3, T_4], Fig. C.3(h)

In Stage G, inductor L_2 resonates with capacitance C_4 and inductor L_1 resonates with capacitance C_3. The freewheeling diode continues to conduct during the duration of this stage. Stage G ends at time T_4 when the current through linear inductor L_2 increases to the value of I_{SAT} and saturable inductor SL_2 saturates.

Stage JP $[T_4, T_5]$, Fig. C.3(n)

In this stage, inductor L_1 continues to resonate with the capacitance in parallel with rectifier diode DR_3, C_3, and saturable inductor SL_2 and linear inductor L_2 resonate with rectifier capacitance C_4. The current through SL_2 and L_2 increase but now in a resonant manner. The freewheeling diode continues to conduct for the duration of this stage. Stage JP ends at time T_5 when capacitor C_4 discharges to zero,turning diode DR_4 on.

Stage EP $[T_5, T_6]$, Fig. C.3(f)

In this stage, the freewheeling diode continues to conduct and inductor current I_{L1} continues to decrease in a resonant manner as capacitance C_3 is charged in a controlled fashion. The current through L_2 and SL_2 increases in a linear manner, but the current through the saturable reactor increases at a much faster rate. Stage J ends when the sum of the currents through L_1, L_2, and SL_2 increases to the value of the load current, turning the freewheeling diode off.

Stage F $[T_6, T_7]$, Fig. C.3(g)

In Stage F, capacitor C_3 continues resonating with inductor L_1. Inductor SL_2 remains saturated, and most of the load current flows through this inductor. The current through linear

inductor L_2 does not vary considerably ($I_{L2} \simeq I_{SAT}$) as long as SL_2 remains saturated. This stage ends when switch Q_2 is turned off, and a new conversion cycle is initiated.

Mode II.B

The sequence of topological stages for Mode II.B is A-B-C-G-E-EP-F. Figure C.8 shows the key waveforms of the soft switched HB operating on this mode.

Prior to the turn-off of switch Q_1, load current I_O flows through the upper secondary and the primary current flows through Q_1. Voltage across C_1 , V_{C1}, is zero, and voltage across C_2, V_{C2}, is equal to the supply voltage V_{IN}. Inductor SL_1 is saturated, whereas inductor SL_2 is unsaturated.

Stage A [T_O, T_1], Fig. C.3(a)

At $t = T_O$, Q_1 is turned off, and the primary current is diverted into C_1 and C_2. Capacitance C_1 starts charging, while C_2 starts discharging at the same rate. Inductor SL_1 remains saturated, and rectifier DR_3 continues to conduct. In this stage, inductor SL_2 is unsaturated and capacitance C_4 resonates with inductor L_2. The stage ends at time T_1 when primary voltage becomes zero, i.e., $V_{C1}(T_1) = V_{C2}(T_1) = V_{IN}/2$.

Stage B [T_1, T_2], Fig. C.3(b)

In Stage B, capacitances C_1 and C_2 start to resonate with the magnetizing inductance of the power transformer since the negative primary voltage resets SL_1. The current through SL_1 decreases quickly as the saturable reactor becomes unsaturated. Capacitance C_1 continues

Figure C.8. Ideal waveforms of the HB ZVS-MRC (L_M) operating in Mode II.B, from top to bottom: gate-source voltage V_{G1}, gate-source voltage V_{G2}, switch Q_1 voltage V_{C1}, switch Q_2 voltage V_{C2}, primary current I_{PRIM}, saturable inductor current I_{SL2}, linear inductor current I_{L2}, linear inductor current I_{L1}, and rectifier capacitor voltage V_{C4}.

to charge, and C_2 continues to discharge. Most of the load current is diverted into the free-wheeling diode. The current through L_1 decreases to zero, at the same time, inductor L_2 and capacitor C_4 continue to resonate. This stage ends at time T_2 when the voltage across capacitor C_2 becomes zero and the antiparallel diode of Q_2 starts conducting. Switch Q_2 should be turned on while its antiparallel diode is conducting to achieve ZVS.

Stage C [T_2, T_3], Fig. C.3(c)

During Stage C, inductor L_1 continues to discharge, inductor L_2 and capacitor C_4 continue to resonate, and saturable inductor SL_1 is resetting. During this stage, the current through SL_1 decreases to zero and this inductor will remain unsaturated for the remaining of the switching cycle. Since the the negative voltage across the upper secondary is constant ($- V_{IN}/N$), current through L_1 decreases linearly. Also, the freewheeling diode continues to conduct. This stage ends at time T_3 when the current through L_1 changes from positive to negative and rectifier diode DR_3 ceases to conduct.

Stage G [T_3, T_4], Fig. C.3(h)

In Stage G, both saturable inductors are unsaturated and current through L_2 increases and current through L_1 decreases in a resonant manner. Capacitance C_3 charges in a controlled manner through linear inductor L_1 and capacitance C_4 discharges through L_2. The free-wheeling diode continues to carry most of the load current. This stage ends at time T_4 when the voltage across rectifier capacitance C_4 resonates back to zero, turning rectifier DR_4 on.

Stage E [T_4, T_5], Fig. C.3(e)

In Stage E, inductor SL_1 continues to reset and capacitor C_3 resonates with inductor L_1. Inducfor SL_2 is unsaturated and the current through L_2 increases linearly. This stage ends at time T_6 when the the current through L_2 increases to the value of I_{SAT} and saturable inductor SL_2 saturates.

Stage EP [T_5, T_6], Fig. C.3(f)

In stage EP, inductor SL_1 continues to reset and capacitor C_3 resonates with inductor L_1. Inductor SL_2 is saturated and the freewheeling diode continues to conduct. The current through SL_2 and L_2 increase in a linear manner. Stage EP ends when the sum of the current through L_1, L_2, and SL_2 increases to the value of the load current, turning the freewheeling diode off.

Stage F [T_6, T_7], Fig. C.3(g)

In Stage F, inductor SL_1 continues to reset and capacitor C_3 resonates with inductor L_1. Inductor SL_2 remains saturated, and most of the load current flows through SL_2. This stage ends when switch Q_2 is turned off, initiating a new conversion cycle.

Mode II.C

The sequence of topological stages for Mode II.C is A-B-C-G-JP-J-F. Figure C.9 shows the key waveforms of this converter operating on this mode.

Prior to the turn-off of switch Q_1, load current I_O flows through the upper secondary and the primary current flows through Q_1. Voltage across C_1, V_{C1}, is zero, and voltage across C_2,
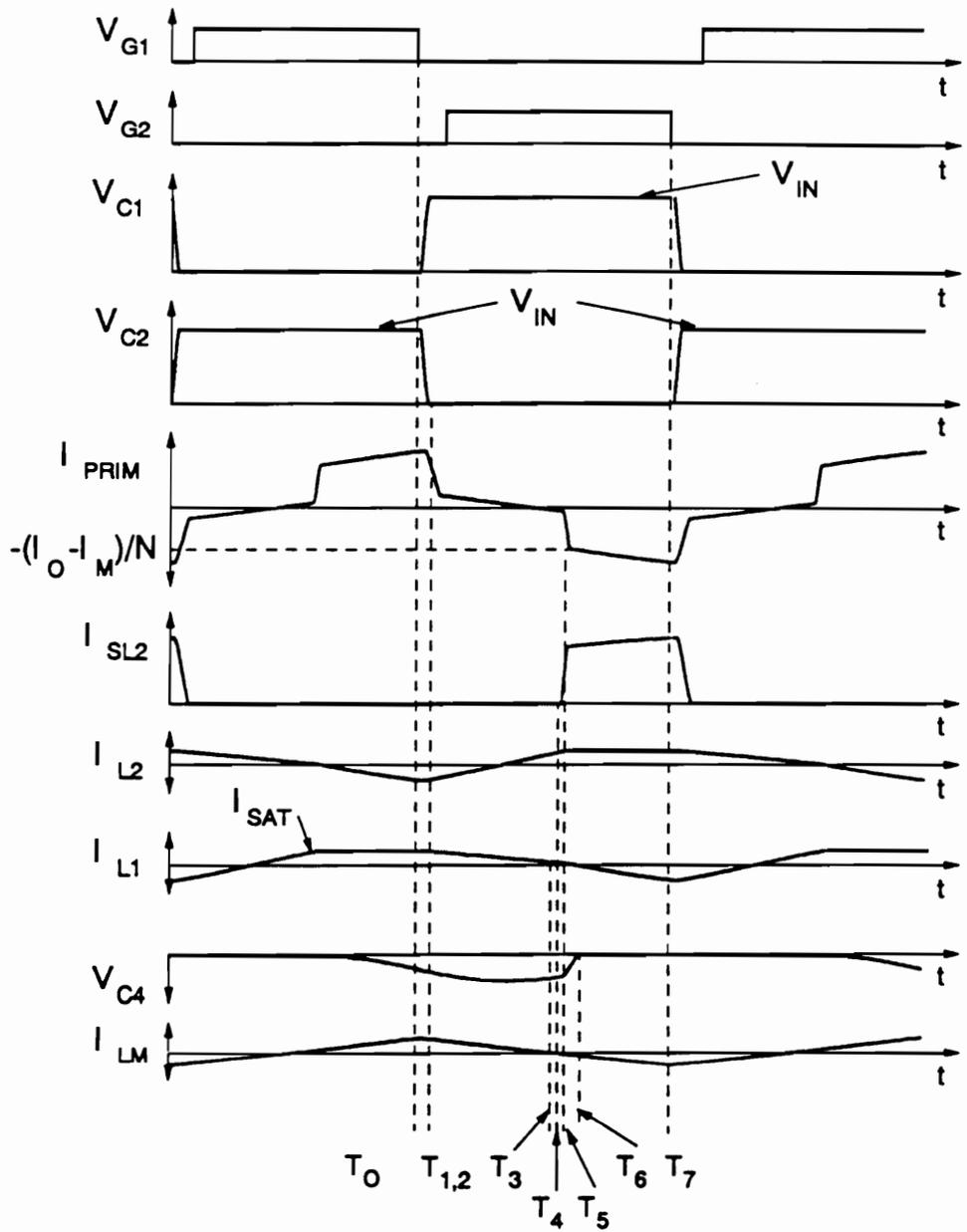
Figure C.9. Ideal waveforms of the HB ZVS-MRC (L_M) operating in Mode II.C, from top to bottom: gate-source voltage V_{G1}, gate-source voltage V_{G2}, switch Q_1 voltage V_{C1}, switch Q_2 voltage V_{C2}, primary current I_{PRIM}, saturable inductor current I_{SL2}, linear inductor current I_{L2}, linear inductor current I_{L1}, and rectifier capacitor voltage V_{C4}.

V_{C2}, is equal to the supply voltage V_{IN}. Inductor SL_1 is saturated, whereas inductor SL_2 is unsaturated.

Stage A [T_0, T_1], Fig. C.3(a)

At $t = T_0$, Q_1 is turned off, and the primary current is diverted into C_1 and C_2. Capacitance C_1 starts charging, while C_2 starts discharging at the same rate. Inductor SL_1 remains saturated, and rectifier DR_3 continues to conduct. In this stage, inductor SL_2 is unsaturated and capacitance C_4 resonates with inductor L_2. The stage ends at time T_1 when primary voltage becomes zero, i.e., $V_{C1}(T_1) = V_{C2}(T_1) = V_{IN}/2$.

Stage B [T_1, T_2], Fig. C.3(b)

In Stage B, capacitances C_1 and C_2 start to resonate with the magnetizing inductance of the power transformer since the negative primary voltage resets SL_1. The current through SL_1 decreases quickly as the saturable reactor becomes unsaturated. Capacitance C_1 continues to charge, and C_2 continues to discharge. Most of the load current flows through the freewheeling diode and the current through L_1 decreases to zero due to the negative voltage across the upper secondary. At the same time, inductor L_2 and capacitor C_4 continue to resonate. This stage ends at time T_2 when the voltage across capacitor C_2 becomes zero and the antiparallel diode of Q_2 starts conducting. Switch Q_2 should be turned on while its antiparallel diode is conducting to operate with ZVS.

Stage C [T_2, T_3], Fig. C.3(c)

During Stage C, inductor L_1 continues to discharge, inductor L_2 and capacitor C_4 continue to form a resonant network, and saturable inductor SL_1 continues to reset. During this stage, the current through SL_1 decreases to zero and this saturable reactor will block all current for the remaining of the switching cycle. Since the the negative voltage across the upper secondary is constant $(-V_{IN}/N)$, current through L_1 decreases linearly. Also, the freewheeling diode continues to conduct. This stage ends at time T_3 when the current flowing through linear inductor L_1 decreases to zero, turning diode DR_3 off.

Stage G [T_3, T_4], Fig. C.3(h)

In Stage G, inductor L_2 resonates with capacitance C_4 and inductor L_1 resonates with capacitance C_3. The freewheeling diode continues to conduct during the duration of this stage. Stage G ends at time T_4 when the current through linear inductor L_2 increases to the value of I_{SAT} and saturable inductor SL_2 saturates.

Stage JP [T_4, T_5], Fig. C.3(n)

In this stage, inductor L_1 continues to resonate with the capacitance in parallel with rectifier diode DR_3, C_3, and saturable inductor SL_2 and linear inductor L_2 resonate with rectifier capacitance C_4. The current through SL_2 and L_2 increases in a resonant manner, and the freewheeling diode continues to conduct for the duration of this stage. Stage JP ends at time T_5 when the sum of the current through SL_2, L_2, and L_1 increases to the value of the load current turning the freewheeling diode off.

Stage J [T_5, T_6], Fig. C.3(m)

In this stage, the freewheeling diode is off and inductor current I_{L1} decreases in a resonant manner as capacitance C_3 is charged in a controlled fashion. Saturable inductor SL_2 is saturated and supplies most of the load current. Rectifier capacitance C_4 continues to discharge in a resonant manner as it interacts with SL_2, L_2, L_1, and C_3. The load current is mostly supplied by the lower rectifier circuit. Stage J ends when rectifier capacitance C_4 discharges to zero and rectifier diode DR_4 turns on.

Stage F $[T_6, T_7]$, Fig. C.3(g)

In Stage F, capacitor C_3 continues resonating with inductor L_1. Inductor SL_2 remains saturated and most of the load current flows through SL_2. The current through linear inductor L_2 does not vary considerably $(I_{L2} \simeq I_{SAT})$ as long as SL_2 remains saturated. This stage ends when switch Q_2 is turned off, and a new conversion cycle is initiated.

C.1.3 Mode III of Operation

In Mode III of operation SL_2 saturates before capacitor C_4 discharges completely (Mode I of operation) or the current through linear inductor L_1 reverses its polarity (Mode II of operation). This mode maximizes the time duration of the power transferring stages, resulting in higher dc voltage-conversion ratios compared to the two previous modes of operation.

Mode III.A
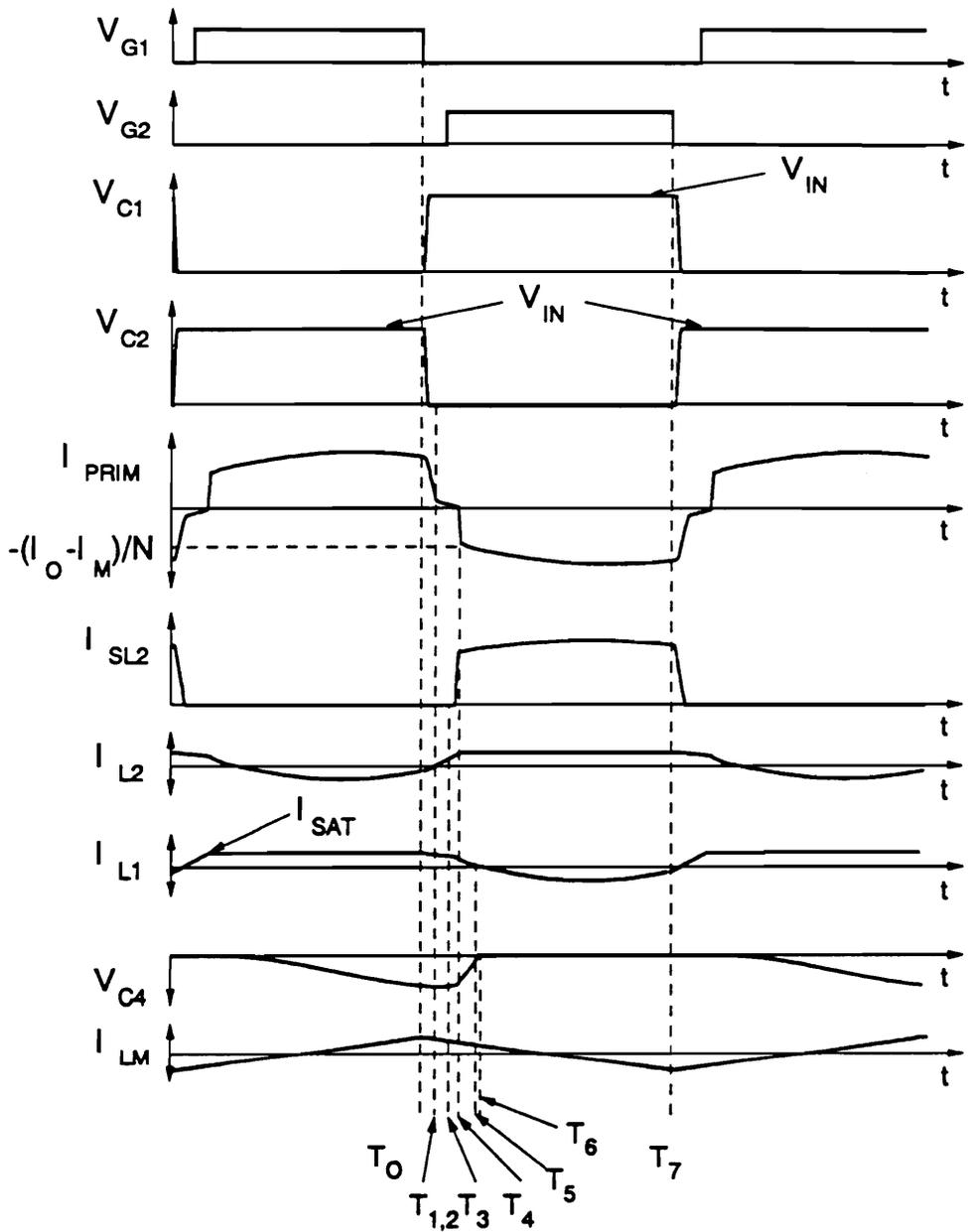
Figure C.10. Ideal waveforms of the HB ZVS-MRC (L_M) operating in Mode III.A, from top to bottom: gate-source voltage V_{G1}, gate-source voltage V_{G2}, switch Q_1 voltage V_{C1}, switch Q_2 voltage V_{C2}, primary current I_{PRIM}, saturable inductor current I_{SL2}, linear inductor current I_{L2}, linear inductor current I_{L1}, and rectifier capacitor voltage V_{C4}.

The sequence of topological stages for Mode III.A is A-B-C-IP-I-H-F. Figure C.10 shows the key waveforms of the HB ZVS-MRC (L_M) operating on this mode.

Prior to the turn-off of switch Q_1, load current I_O flows through the upper secondary and the primary current flows through Q_1. Voltage across C_1, V_{C1}, is zero, and voltage across C_2, V_{C2}, is equal to the supply voltage V_{IN}. Inductor SL_1 is saturated, whereas inductor SL_2 is unsaturated.

Stage A $[T_O, T_1]$, Fig. C.3(a)

At $t = T_O$, Q_1 is turned off, and the primary current is diverted into C_1 and C_2. Capacitance C_1 starts charging, while C_2 starts discharging at the same rate. Inductor SL_1 remains saturated, and rectifier DR_3 continues to conduct. In this stage, inductor SL_2 is unsaturated and capacitance C_4 resonates with inductor L_2. The stage ends at time T_1 when primary voltage becomes zero.

Stage B $[T_1, T_2]$, Fig. C.3(b)

In Stage B, capacitances C_1 and C_2 start to resonate with the magnetizing inductance of the power transformer since the negative primary voltage resets SL_1. The current through SL_1 decreases quickly as the saturable reactor unsaturates. Capacitance C_1 continues to charge, and C_2 continues to discharge. At the beginning of Stage B most of the load current is diverted to the freewheeling diode. The current through L_1 decreases to zero and inductor L_2 and capacitor C_4 continue to resonate. This stage ends at time T_2 when the voltage across capacitor C_2 becomes zero, and the antiparallel diode of Q_2 starts conducting. Switch Q_2

should be turned on soon after while its antiparallel diode is conducting to achieve lossless switching.

Stage C [T_2, T_3], Fig. C.3(c)

During Stage C, inductor L_1 continues to discharge, inductor L_2 and capacitor C_4 continue to resonate, and saturable inductor SL_1 continues to reset. During this stage, the current through SL_1 decreases to zero. Since the the negative voltage across the upper secondary is constant ($-V_{IN}/N$), current through L_1 decreases linearly. Also, the freewheeling diode continues to conduct. This stage ends at time T_3 when saturable inductor SL_2 saturates.

Stage IP [T_3, T_4], Fig. C.3(l)

In Stage IP, inductor L_2 and saturable inductor SL_2 resonate with capacitance C_4. Inductor L_1 continues to decrease linearly and the freewheeling diode conducts. Stage IP ends at time T_4 when the sum of the current flowing through L_1, L_2, and SL_2 increases to the value of the load current and the freewheeling diode ceases to conduct.

Stage I [T_4, T_5], Fig. C.3(k)

In this stage, inductors L_1, L_2, and SL_2 resonate with capacitance C_4. SL_2 supplies most of the load current and the freewheeling diode is off. At time T_5 the voltage across capacitor C_4 completely discharges and rectifier DR_4 is turned on.

Stage H [T_5, T_6], Fig. C.3(i)

In this stage, the load current is supplied by the lower rectifier circuit. The current through L_1 continues to decrease and the current through L_2 and SL_2 increases in a linear manner. This stage ends at time T_6 when the current through L_1 decreases to zero and diode DR_3 turns off.

Stage F [T_6, T_7], Fig. C.3(g)

In Stage F, inductor SL_1 continues to reset and capacitor C_3 begins resonating with inductor L_1. Inductor SL_2 remains saturated, and most of the load current flows through SL_2. This stage ends when switch Q_2 is turned off, beginning a new conversion cycle.

Mode III.B

The sequence of topological stages for Mode III.B is A-B-C-IP-HP-H-F. Figure C.11 shows the key waveforms of this converter operating on this mode.

Prior to the turn-off of switch Q_1, load current I_O flows through the upper secondary and the primary current flows through Q_1. Voltage across C_1 , V_{C1}, is zero, and voltage across C_2, V_{C2}, is equal to the supply voltage V_{IN}. Inductor SL_1 is saturated, whereas inductor SL_2 is unsaturated.

Stage A [T_O, T_1], Fig. C.3(a)

At $t = T_O$, Q_1 is turned off, and the primary current is diverted into C_1 and C_2. Capacitance C_1 starts charging, while C_2 starts discharging at the same rate. Inductor SL_1 remains saturated, and rectifier DR_3 continues to conduct. In this stage, inductor SL_2 is unsaturated and

Figure C.11. Ideal waveforms of the HB ZVS-MRC (L_M) operating in Mode III.B, from top to bottom: gate-source voltage V_{G1}, gate-source voltage V_{G2}, switch Q_1 voltage V_{C1}, switch Q_2 voltage V_{C2}, primary current I_{PRIM}, saturable inductor current I_{SL2}, linear inductor current I_{L2}, linear inductor current I_{L1}, and rectifier capacitor voltage V_{C4}.

capacitance C_4 resonates with inductor L_2. The stage ends at time T_1 when primary voltage becomes zero, i.e., $V_{C1}(T_1) = V_{C2}(T_1) = V_{IN}/2$.

Stage B $[T_1, T_2]$, Fig. C.3(b)

In Stage B, capacitances C_1 and C_2 start to resonate with the magnetizing inductance of the power transformer since the negative primary voltage resets SL_1. The current through SL_1 decreases quickly as the saturable reactor becomes unsaturated. Capacitance C_1 continues to charge, and C_2 continues to discharge. Most of the load current flows through the freewheeling diode. The current through L_1 decreases to zero due to a negative voltage across the upper secondary. At the same time, inductor L_2 and capacitor C_4 continue to resonate. This stage ends at time T_2 when the voltage across capacitor C_2 becomes zero and the antiparallel diode of Q_2 starts conducting. Switch Q_2 should be turned on while its antiparallel diode is conducting to achieve ZVS.

Stage C $[T_2, T_3]$, Fig. C.3(c)

During Stage C, inductor L_1 continues to discharge, inductor L_2 and capacitor C_4 continue to resonate, and saturable inductor SL_1 continues to reset. During this stage, the current through SL_1 decreases to zero. Since the the negative voltage across the upper secondary is constant $(- V_{IN}/N)$, current through L_1 decreases linearly. Also, the freewheeling diode continues to conduct. This stage ends at time T_3 when saturable inductor SL_2 saturates.

Stage IP $[T_3, T_4]$, Fig. C.3(I)

In Stage IP, inductor L_2 and saturable inductor SL_2 resonate with capacitance C_4. Inductor L_1 continue to decrease linearly and the freewheeling diode conducts. Stage IP ends at time T_4 when capacitor C_4 has completely discharged and diode DR_4 turns on.

Stage HP [T_4, T_5], Fig. C.3(j)

In this stage, inductor current $i_{L1}(t)$ continues to decrease and the current through L_2 and SL_2 increases linearly. Stage HP ends when the sum of the current flowing through L_1, L_2, and SL_2 increases to the value of the load current.

Stage H [T_5, T_6], Fig. C.3(i)

In this stage, the load current is supplied by the lower rectifier circuit. The current through L_1 continues to decrease and the current through L_2 and SL_2 increases in a linear manner. This stage ends at time T_6 when the current through L_1 decreases to zero and diode DR_3 turns off.

Stage F [T_6, T_7], Fig. C.3(g)

In Stage F, inductor SL_1 remains unsaturated and capacitor C_3 begins resonating with inductor L_1. Inductor SL_2 remains saturated and most of the load current flows through SL_2. This stage ends when switch Q_2 is turned off, and a new conversion cycle is initiated.

Mode III.C

Figure C.12. Ideal waveforms of the HB ZVS-MRC (L_M) operating in Mode III.C, from top to bottom: gate-source voltage V_{G1}, gate-source voltage V_{G2}, switch Q_1 voltage V_{C1}, switch Q_2 voltage V_{C2}, primary current I_{PRIM}, saturable inductor current I_{SL2}, linear inductor current I_{L2}, linear inductor current I_{L1}, and rectifier capacitor voltage V_{C4}.

The sequence of topological stages for Mode III.C is A-B-C-IP-I-J-F. Figure C.12 shows the key waveforms of this converter operating on this mode.

Prior to the turn-off of switch Q_1, load current I_O flows through the upper secondary and the primary current flows through Q_1. Voltage across C_1, V_{C1}, is zero, and voltage across C_2, V_{C2}, is equal to the supply voltage V_{IN}. Inductor SL_1 is saturated, whereas inductor SL_2 is unsaturated.

Stage A [T_O, T_1], Fig. C.3(a)

At $t = T_O$, Q_1 is turned off, and the primary current is diverted into C_1 and C_2. Capacitance C_1 starts charging, while C_2 starts discharging at the same rate. Inductor SL_1 remains saturated, and rectifier DR_3 continues to conduct. In this stage, inductor SL_2 is unsaturated and capacitance C_4 resonates with inductor L_2. The stage ends at time T_1 when primary voltage becomes zero, i.e., $V_{C1}(T_1) = V_{C2}(T_1) = V_{IN}/2$.

Stage B [T_1, T_2], Fig. C.3(b)

In Stage B, capacitances C_1 and C_2 start to resonate with the magnetizing inductance of the power transformer since the negative primary voltage resets SL_1. The current through SL_1 decreases quickly as the saturable reactor becomes unsaturated. Capacitance C_1 continues to charge, and C_2 continues to discharge. Most of the load current flows through the free-wheeling diode. The current through L_1 decreases to zero due to a negative voltage across the upper secondary. At the same time, inductor L_2 and capacitor C_4 continue to resonate. This stage ends at time T_2 when the voltage across capacitor C_2 becomes zero and the anti-

parallel diode of Q_2 starts conducting. Switch Q_2 should be turned on while its antiparallel diode is conducting to achieve ZVS.

Stage C [T_2, T_3], Fig. C.3(c)

During Stage C, inductor L_1 continues to discharge, inductor L_2 and capacitor C_4 continue to resonate, and saturable inductor SL_1 continues to reset. During this stage, the current through SL_1 decreases to zero and since the the negative voltage across the upper secondary is constant ($-V_{IN}/N$). current through L_1 decreases linearly. Also, the freewheeling diode continues to conduct. This stage ends at time T_3 when the current through L_2 increases to the value of I_{SAT} and saturable inductor SL_2 saturates.

Stage IP [T_3, T_4], Fig. C.3(I)

In Stage IP, inductor L_2 and SL_2 resonates with capacitance C_4. Inductor L_1 continues to decrease linearly and the freewheeling diode continues to conduct. Stage IP ends at time T_4 when the sum of the current flowing through L_1. L_2. and SL_2 increases to the value of the load current.

Stage I [T_4, T_5], Fig. C.3(k)

In this stage, inductor current $i_{L1}(t)$ continues to linearly decrease and the current through L_2 and SL_2 increases in a resonant manner. The freewheeling diode is off and the load current is supplied by the lower rectifier circuit. This stage ends at time T_5 when the current through L_1 decreases to zero turning diode DR_3 off.

Stage J [T_5, T_6], Fig. C.3(m)

In this stage, the load current is supplied by the lower rectifier circuit. The current through L_1 decreases and the current through L_2 and SL_2 increases in a resonant manner (interaction with C_3 and C_4). This stage ends at time T_6 when the voltage across C_4 resonates back to zero turning diode DR_4 on.

Stage F [T_6, T_7], Fig. C.3(g)

In Stage F, inductor SL_1 is unsaturated and capacitor C_3 begins resonating with inductor L_1. Inductor SL_2 remains saturated, and most of the load current flows through this inductor. This stage ends when switch Q_2 is turned off, and a new conversion cycle is initiated.

Mode III.D

The sequence of topological stages for Mode III.D is A-B-C-IP-HP-EP-F. Figure C.13 shows the key waveforms of this converter operating on this mode.

Prior to the turn-off of switch Q_1, load current I_O flows through the upper secondary and the primary current flows through Q_1. Voltage across C_1, V_{C1}, is zero, and voltage across C_2, V_{C2}, is equal to the supply voltage V_{IN}. Inductor SL_1 is saturated, whereas inductor SL_2 is unsaturated.

Stage A [T_O, T_1], Fig. C.3(a)
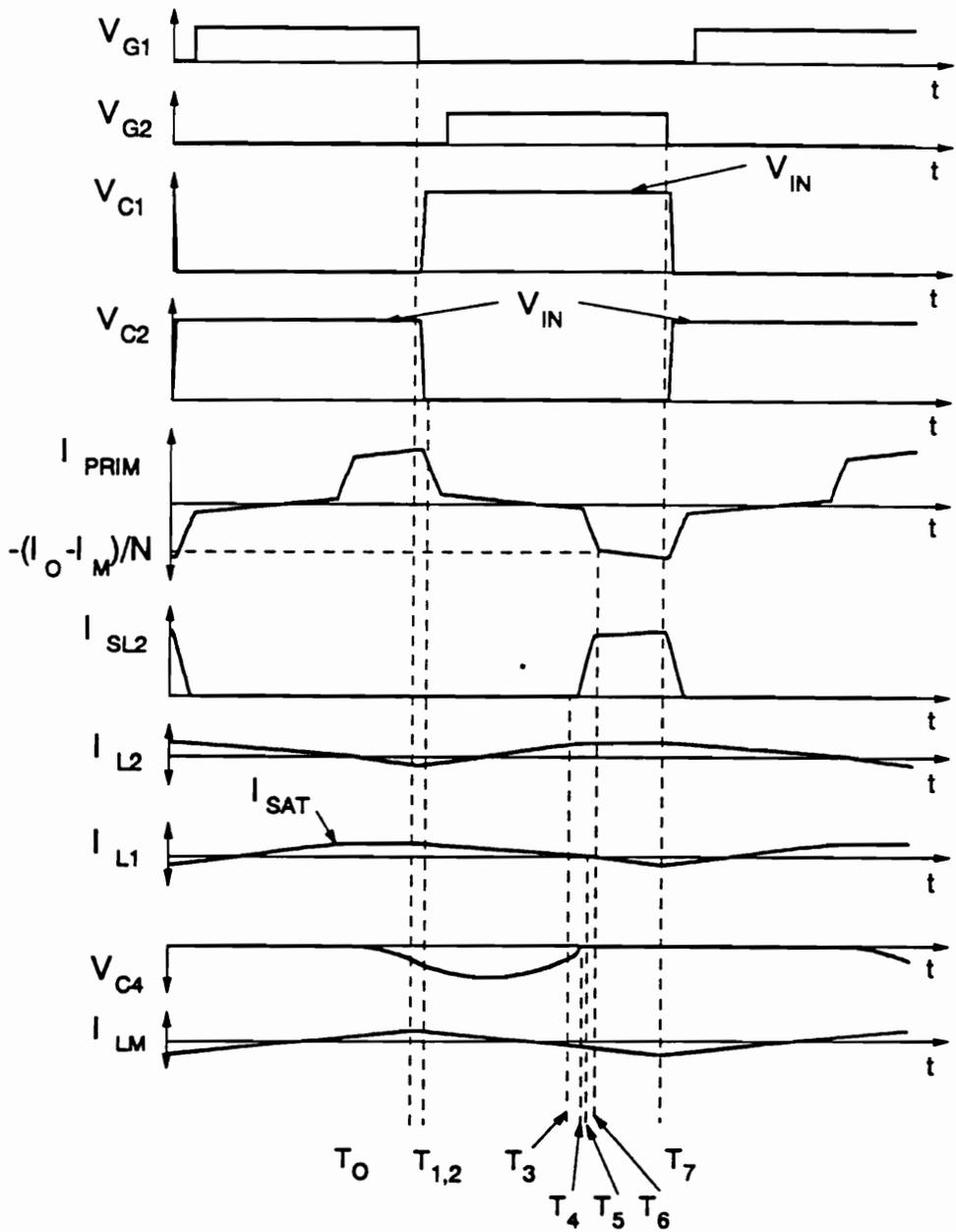
**Figure C.13.** Ideal waveforms of the HB ZVS-MRC (L_M) operating in Mode III.D, from top to bottom: gate-source voltage V_{G1}, gate-source voltage V_{G2}, switch Q_1 voltage V_{C1}, switch Q_2 voltage V_{C2}, primary current I_{PRIM}, saturable inductor current I_{SL2}, linear inductor current I_{L2}, linear inductor current I_{L1}, and rectifier capacitor voltage V_{C4}.

At $t = T_O$, Q_1 is turned off, and the primary current is diverted into C_1 and C_2. Capacitance C_1 starts charging, while C_2 starts discharging at the same rate. Inductor SL_1 remains saturated, and rectifier DR_3 continues to conduct. In this stage, inductor SL_2 is unsaturated and capacitance C_4 resonates with inductor L_2. The stage ends at time T_1 when primary voltage becomes zero, i.e., $V_{C1}(T_1) = V_{C2}(T_1) = V_{IN}/2$.

Stage B $[T_1, T_2]$, Fig. C.3(b)

In Stage B, capacitances C_1 and C_2 start to resonate with the magnetizing inductance of the power transformer since the negative primary voltage resets SL_1. The current through SL_1 decreases quickly as the saturable reactor becomes unsaturated. Capacitance C_1 continues to charge, and C_2 continues to discharge. Most of the load current flows through the freewheeling diode. The current through L_1 decreases to zero due to the negative voltage across the upper secondary. At the same time, inductor L_2 and capacitor C_4 continue to resonate. This stage ends at time T_2 when the voltage across capacitor C_2 becomes zero and the antiparallel diode of Q_2 starts conducting. Switch Q_2 should be turned on while its antiparallel diode is conducting to achieve ZVS.

Stage C $[T_2, T_3]$, Fig. C.3(c)

During Stage C, inductor L_1 continues to discharge, inductor L_2 and capacitor C_4 continue to resonate, and saturable inductor SL_1 continues to reset. During this stage, the current through SL_1 decreases to zero. Since the the negative voltage across the upper secondary is constant $(-V_{IN}/N)$, current through L_1 decreases linearly. Also, the freewheeling diode continues to conduct. This stage ends at time T_3 when saturable inductor SL_2 saturates.

Stage IP [T_3, T_4], Fig. C.3(I)

In Stage IP, inductor L_2 and saturable inductor SL_2 resonate with capacitance C_4. Inductor L_1 continues to decrease linearly and the freewheeling diode continues to conducts. Stage IP ends at time T_4 when capacitor C_4 completely discharged and diode DR_4 turns on.

Stage HP [T_4, T_5], Fig. C.3(j)

In this stage, inductor current $i_{L1}(t)$ continues to decrease and the current through L_2 and SL_2 increases linearly. Stage HP ends when the current through linear inductor L_1 decreases to zero, turning rectifier diode DR_3 off and starting the resonance of the rectifier capacitance C_3 and inductor L_1.

Stage EP [T_5, T_6], Fig. C.3(f)

In this stage, the freewheeling diode continues to conduct and inductor L_1 resonates with capacitance C_3. Saturable inductor SL_2 is saturated. The current through SL_2 and the linear inductor L_2 increases in a linear manner, but the current through the saturable reactor increases at a much faster rate. This stage ends when the sum of the currents flowing through both linear inductors and saturable inductor SL_2 increases to the value of the load current turning the freewheeling diode off.

Stage F [T_6, T_7], Fig. C.3(g)

In Stage F, capacitor C_3 continues resonating with inductor L_1. Inductor SL_2 remains saturated, and most of the load current flows through SL_2. The current through linear inductor L_2

does not vary considerably ($I_{L2} \simeq I_{SAT}$) as long as SL_2 remains saturated. This stage ends when switch Q_2 is turned off, and a new conversion cycle is initiated.

Mode III.E

The sequence of topological stages for Mode III.E is A-B-C-IP-JP-EP-F. Figure C.14 shows the key waveforms of this converter operating on this mode.

Prior to the turn-off of switch Q_1, load current I_O flows through the upper secondary and the primary current flows through Q_1. Voltage across C_1, V_{C1}, is zero, and voltage across C_2, V_{C2}, is equal to the supply voltage V_{IN}. Inductor SL_1 is saturated, whereas inductor SL_2 is unsaturated.

Stage A [T_O, T_1], Fig. C.3(a)

At $t = T_O$, Q_1 is turned off, and the primary current is diverted into C_1 and C_2. Capacitance C_1 starts charging and C_2 starts discharging at the same rate. Inductor SL_1 remains saturated, and rectifier DR_3 continues to conduct. In this stage, inductor SL_2 is resetting and capacitance C_4 resonates with inductor L_2. The stage ends at time T_1 when primary voltage becomes zero, i.e., $V_{C1}(T_1) = V_{C2}(T_1) = V_{IN}/2$.

Stage B [T_1, T_2], Fig. C.3(b)

In Stage B, capacitances C_1 and C_2 start to resonate with the magnetizing inductance of the power transformer since the negative primary voltage resets SL_1. The current through SL_1 decreases quickly as the saturable reactor becomes unsaturated. Capacitance C_1 continues
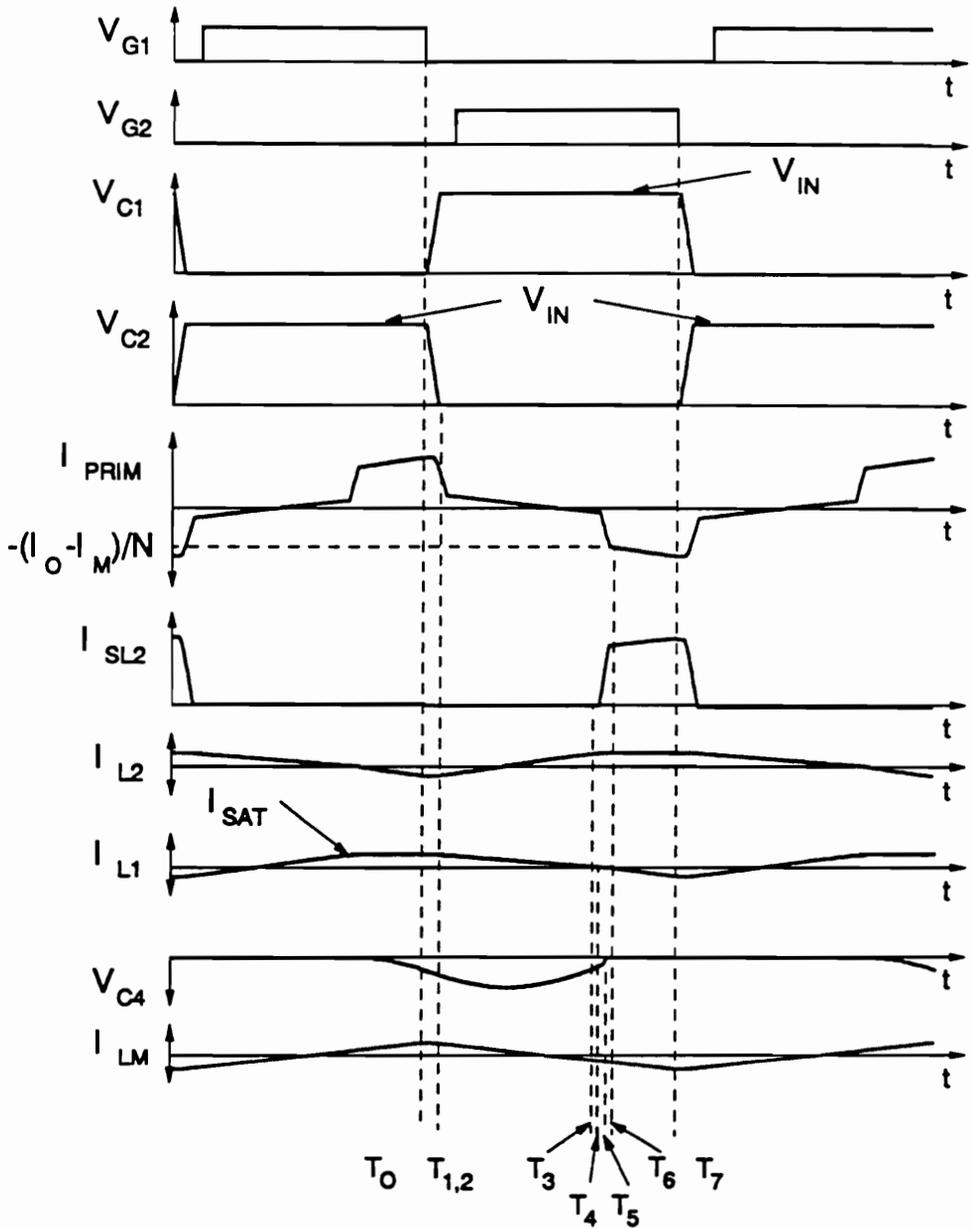
Figure C.14. Ideal waveforms of the HB ZVS-MRC (L_M) operating in Mode III.E, from top to bottom: gate-source voltage V_{G1}, gate-source voltage V_{G2}, switch Q_1 voltage V_{C1}, switch Q_2 voltage V_{C2}, primary current I_{PRIM}, saturable inductor current I_{SL2}, linear inductor current I_{L2}, linear inductor current I_{L1}, and rectifier capacitor voltage V_{C4}.

to charge, and C_2 continues to discharge. Most of the load current flows through the free-wheeling diode. The current through L_1 decreases to zero due to the negative voltage across the upper secondary. At the same time, inductor L_2 and capacitor C_4 continue to resonate. This stage ends at time T_2 when the voltage across capacitor C_2 becomes zero and the anti-parallel diode of Q_2 starts conducting. Switch Q_2 should be turned on while its antiparallel diode is conducting to achieve ZVS.

Stage C [T_2, T_3], Fig. C.3(c)

During Stage C, inductor L_1 continues to discharge, inductor L_2 and capacitor C_4 continue to resonate, and saturable inductor SL_1 continues to reset. During this stage, the current through SL_1 decreases to zero and since the the negative voltage across the upper secondary is constant ($-V_{IN}/N$), current through L_1 decreases linearly. Also, the freewheeling diode continues to conduct. This stage ends at time T_3 when the current through L_2 increases to the value of I_{SAT} and saturable inductor SL_2 saturates.

Stage IP [T_3, T_4], Fig. C.3(l)

In Stage IP, inductor L_2 and saturable inductor SL_2 resonate with capacitance C_4. Inductor L_1 continue to decrease linearly and the freewheeling diode conducts. Stage IP ends at time T_4 when the current through linear inductor L_1 linearly decreases to zero, turning rectifier diode DR_3 off.

Stage JP [T_4, T_5], Fig. C.3(n)

In this stage, inductor L_1 starts resonating with the capacitance in parallel with rectifier diode DR_3, C_3. Saturable inductor SL_2 and linear inductor L_2 continue to resonate with rectifier capacitance C_4. The current through SL_2 and L_2 increases in a resonant manner. The free-wheeling diode continues to conduct for the duration of this stage. Stage JP ends at time T_5 when voltage across capacitor C_4 resonates back to zero, turning rectifier diode DR_4 on.

Stage EP [T_5, T_6], Fig. C.3(f)

In this stage, the freewheeling diode continues to conduct and inductor L_1 resonates with capacitance C_3. Saturable inductor SL_2 is saturated and the current through SL_2 and the linear inductor L_2 increases in a linear manner, but the current through the saturable reactor increases at a much faster rate. This stage ends when the sum of the currents flowing through both linear inductors and saturable inductor SL_2 increases to the value of the load current turning the freewheeling diode off.

Stage F [T_6, T_7], Fig. C.3(g)

In Stage F, capacitor C_3 continues resonating with inductor L_1. Inductor SL_2 remains saturated, and most of the load current flows through SL_2. This stage ends when switch Q_2 is turned off, and a new conversion cycle is initiated.

Mode III.F

The sequence of topological stages for Mode III.F is A-B-C-IP-JP-J-F. Figure C.15 shows the key waveforms of this converter operating on this mode.
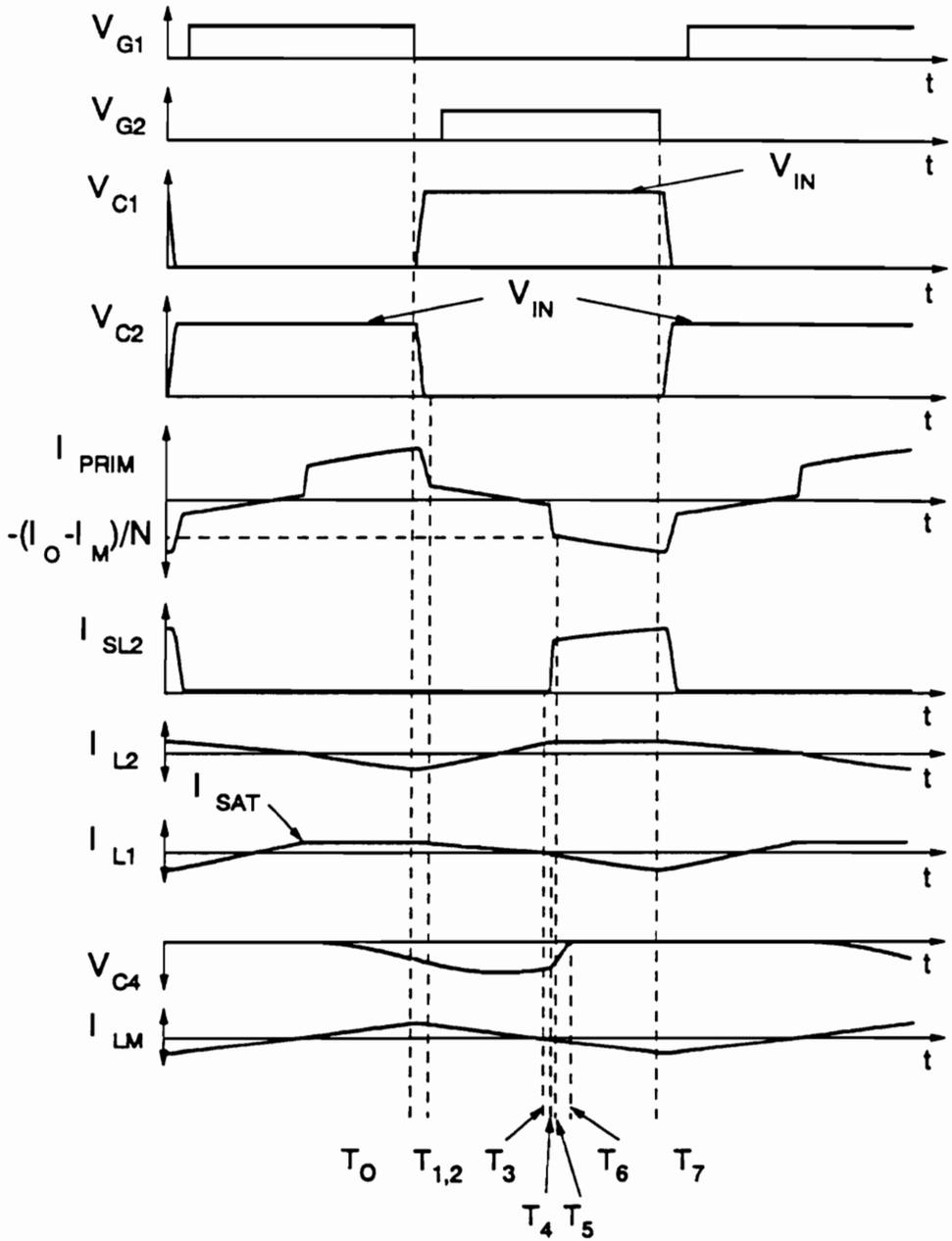
Figure C.15. Ideal waveforms of the HB ZVS-MRC (L_M) operating in Mode III.F, from top to bottom: gate-source voltage V_{G1}, gate-source voltage V_{G2}, switch Q_1 voltage V_{C1}, switch Q_2 voltage V_{C2}, primary current I_{PRIM}, saturable inductor current I_{SL2}, linear inductor current I_{L2}, linear inductor current I_{L1}, and rectifier capacitor voltage V_{C4}.

Prior to the turn-off of switch Q_1, load current I_O flows through the upper secondary and the primary current flows through Q_1. Voltage across C_1, V_{C1}, is zero, and voltage across C_2, V_{C2}, is equal to the supply voltage V_{IN}. Inductor SL_1 is saturated, whereas inductor SL_2 is unsaturated.

Stage A $[T_O, T_1]$, Fig. C.3(a)

At $t = T_O$, Q_1 is turned off, and the primary current is diverted into C_1 and C_2. Capacitance C_1 starts charging and C_2 starts discharging at the same rate. Inductor SL_1 remains saturated, and rectifier DR_3 continues to conduct. In this stage, inductor SL_2 is unsaturated and capacitance C_4 resonates with inductor L_2. The stage ends at time T_1 when primary voltage becomes zero, i.e., $V_{C1}(T_1) = V_{C2}(T_1) = V_{IN}/2$.

Stage B $[T_1, T_2]$, Fig. C.3(b)

In Stage B, capacitances C_1 and C_2 start to resonate with the magnetizing inductance of the power transformer since the negative primary voltage resets SL_1. The current through SL_1 decreases quickly as the saturable reactor becomes unsaturated. Capacitance C_1 continues to charge, and C_2 continues to discharge. Most of the load current flows through the free-wheeling diode. The current through L_1 decreases to zero due to the negative voltage across the upper secondary. At the same time, inductor L_2 and capacitor C_4 continue to resonate. This stage ends at time T_2 when the voltage across capacitor C_2 becomes zero and the anti-parallel diode of Q_2 starts conducting. Switch Q_2 should be turned on while its antiparallel diode is conducting to achieve ZVS.

Stage C $[T_2, T_3]$, Fig. C.3(c)

During Stage C, inductor L_1 continues to discharge, inductor L_2 and capacitor C_4 continue to resonate, and saturable inductor SL_1 continues to reset. During this stage, the current through SL_1 decreases to zero. Since the the negative voltage across the upper secondary is constant $(-V_{IN}/N)$, current through L_1 decreases linearly. Also, the freewheeling diode continues to conduct. This stage ends at time T_3 when saturable inductor SL_2 saturates.

Stage IP [T_3, T_4], Fig. C.3(l)

In Stage IP, inductor L_2 and saturable inductor SL_2 resonate with capacitance C_4. Inductor L_1 continues to decrease linearly and the freewheeling diode conducts. Stage IP ends at time T_4 when the current through linear inductor L_1 linearly decreases to zero, turning rectifier diode DR_3 off.

Stage JP [T_4, T_5], Fig. C.3(n)

In this stage, inductor L_1 starts resonating with the capacitance in parallel with rectifier diode DR_3, C_3. Saturable inductor SL_2 and linear inductor L_2 continue to resonate with rectifier capacitance C_4. The current through SL_2 and L_2 increases in a resonant manner. The freewheeling diode continues to conduct for the duration of this stage. Stage JP ends at time T_5 when the sum of the current through SL_2. L_2. and L_1 increases to the value of the load current, turning the freewheeling diode off.

Stage J [T_5, T_6], Fig. C.3(m)

In this stage, the freewheeling diode is off and inductor current I_{L1} decreases in a resonant manner as capacitance C_3 is charged in a controlled fashion. Saturable inductor SL_2 is saturated and supplies most of the load current. Rectifier capacitance C_4 continues to discharge in a resonant manner as it interacts with SL_2, L_2, L_1, and C_3. Stage J ends when rectifier capacitance C_4 discharges to zero and rectifier diode DR_4 turns on.

Stage F $[T_6, T_7]$, Fig. C.3(g)

In Stage F, capacitor C_3 continues resonating with inductor L_1. Inductor SL_2 remains saturated, and most of the load current flows through SL_2. The current through linear inductor L_2 does not vary considerably $(I_{L2} \simeq I_{SAT})$ since SL_2 is saturated. This stage ends when switch Q_2 is turned off, and a new conversion cycle is initiated.

C.3.2 Light Load Operation

For heavy to medium load operation the saturable reactors SL_1 and SL_2 supply most of the load current, while the linear inductors, L_1 and L_2, carry 20 to 10% of the total load current. Heavy load currents result in increased delay between the time the saturable reactor begins to unsaturate and the time it blocks all current (saturable inductors were modeled to have a finite inductance when saturated and infinite inductance when unsaturated). The corresponding saturable inductor, saturable inductor SL_1 for the half cycle described by the topological sequences in the preceding discussion, will not start resetting until the voltage across the transformer windings changes polarity. The transformer voltage will changes from

positive to negative at the start of topological Stage B. Topological stages A and B model the switching transition of the primary switches and correspond to a small fraction of the total switching period. Therefore, for heavy loads, the delay time necessary for the saturable cores to come out of saturation is longer than the duration of the switching transition (time duration of topological stages A and B) as is modeled in the topological sequences describing modes I, II, and III. At lighter loads, the time it takes the saturable inductor to come out of saturation decreases and the current through this inductor will decrease to zero before the switching transition is over. Therefore, to model light load operation, an added topological stage is needed to represent the latter duration of Stage B when saturable inductor SL_1 is no longer saturated. This stage is shown in Fig. C.16 as topological Stage BP. During light load operation, the switching transition is represented by the topological sequence of Stage A. Stage B. and Stage BP.

For even lighter load operation, most of the load will no longer be supplied by the saturable inductors. In the extreme case, no load operation, the saturable inductors will never saturate and all of the load current will be supplied by the linear inductors L_1 and L_2. Light load to no load operation was not modelled since they are not necessary for the design of the converter. The primary switches in this converter turn on under zero voltage due to the resonance of the primary-switch capacitance and the magnetizing inductance. Similarly, the rectifiers turn on softly (zero-voltage turn-on) due to the controlled resonance of the rectifier capacitance and the linear inductors on the secondary side of the transformer. Since in normal operation the saturable inductors are not forced to sweep the complete B-H loop, the converter can operate at a relatively high frequency. A constant off-time, variable frequency control is required to regulate the output voltage.
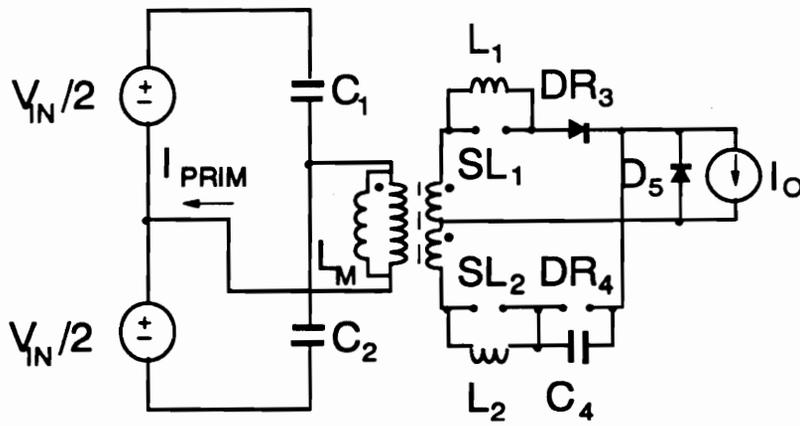
Figure C.16. Topological Stage BP. Saturable inductors SL_1 and SL_2 are in the unsaturated state.

Table C.1. Modes of operation of the HB ZVS-MRC (L_M).

MODE	STAGE SEQUENCE
I.A	A - B - C - D - HP - H - F
I.B	A - B - C - D - HP - EP - F
I.C	A - B - C - D - E - EP - F
II.A	A - B - C - G - JP - EP - F
II.B	A - B - C - G - E - EP - F
II.C	A - B - C - G - JP - J - F
III.A	A - B - C - IP - I - H - F
III.B	A - B - C - IP - HP - H - F
III.C	A - B - C - IP - I - J - F
III.D	A - B - C - IP - HP - EP - F
III.E	A - B - C - IP - JP - EP - F
III.F	A - B - C - IP - JP - J - F

C.2 DC Voltage-Conversion-Ratio

A set of dc voltage-conversion-ratio characteristics is shown in Figs. C.17a - C.22a. The characteristics are plotted as a function of normalized conversion frequency, $f_{con} = f_S/2f_O$ for different normalized output currents, $I_{ON} = Z_N I_O/NV_{IN}$. The characteristics are plotted for different values of the design parameters: $C_N = 2C_D/(N^2C)$, the ratio of the capacitance across the rectifiers reflected to the primary $(4C_D/N^2)$ and the resonant capacitance across the primary switches $(2C)$; $L_N = 4L_M/(N^2L)$, the ratio of the magnetizing inductance L_M and the resonant inductors across the rectifiers reflected to the primary $(N^2L/4)$; $I_{SLN} = I_{SAT}/(I_O/N)$, the normalized current of the linear inductor during the interval the saturable inductor is saturated; and L/SL, the ratio between the secondary linear inductance and the inductance of the saturable reactor when saturated. The resonant frequency is defined as $\omega_O = 2\pi f_O = 1/\sqrt{2CL_M}$ and the characteristic impedance as $Z_N = \sqrt{L_M/2C}$. V_{IN} is the input voltage and N is the turns ratio of the transformer.

A complete set of design characteristics are given for $C_N = 5$ and 10, and $L_N = 1, 3,$ and 6 (Figs. C.17a - C.22b). All characteristics are plotted for $I_{SAT}/I_O = 1$ and for the ratio $L / SL = 100$.

C.3 DC Analysis of Topological Stages

Analytical expressions for the initial conditions, circuit equations, their solutions, and durations of the topological stages refers to the ideal HB ZVS-MRC (L_M) shown in Fig. C.1:

C.3.1 Heavy Load Operation

STAGE A [T_{AO}, T_{A1}] (Fig. C.23)

Initial Conditions:

$$v_{C1}(T_{AO}) = 0 \qquad\qquad (C.1.a)$$

$$v_{C2}(T_{AO}) = V_{IN} \qquad\qquad (C.1.b)$$
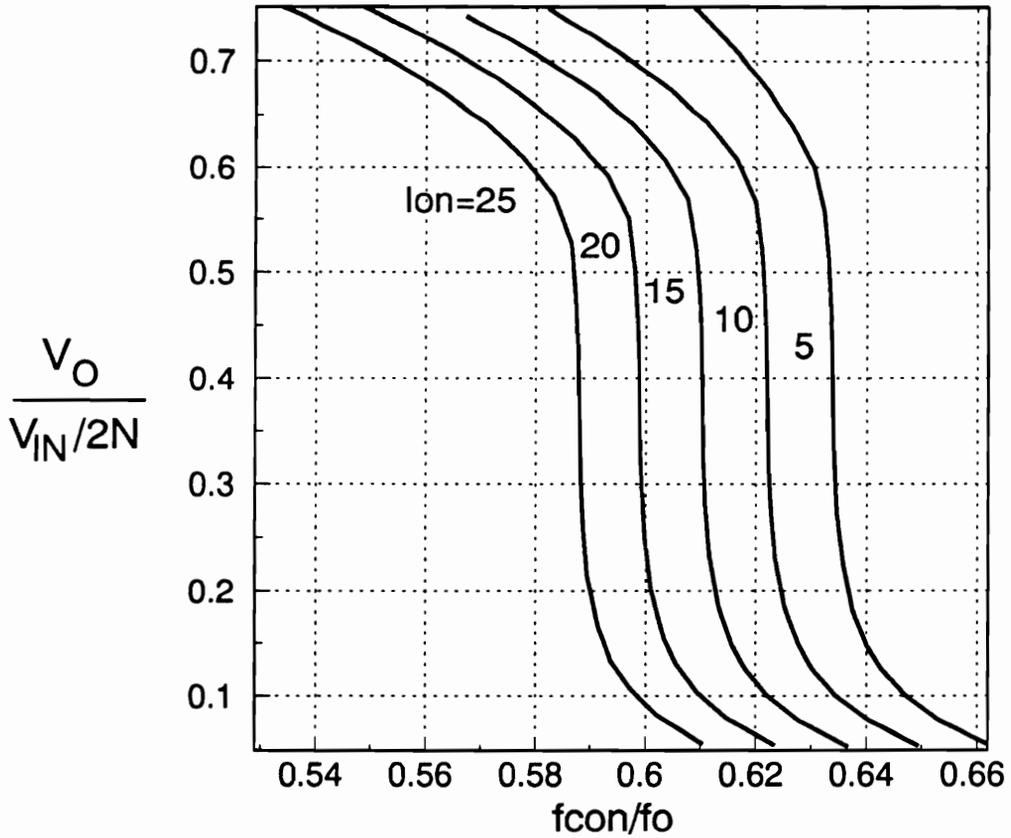
Figure C.17a. DC voltage-conversion-ratio characteristics as a function of the normalized switching frequency for $C_N = 5$ and $L_N = 1$. The characteristics are plotted for $I_{SLN} = 1$ and $L/SL = 100$; $C_N = 2C_D/(CN^2)$, $L_N = 4L_M/(LN^2)$, $I_{SLN} = I_{SAT}/(I_O/N)$, $Z_O = \sqrt{L_M/2C}$, $I_O = 2I_O Z_O/(V_{IN}N)$, and $f_O = 1/2\pi\sqrt{2CL_M}$.
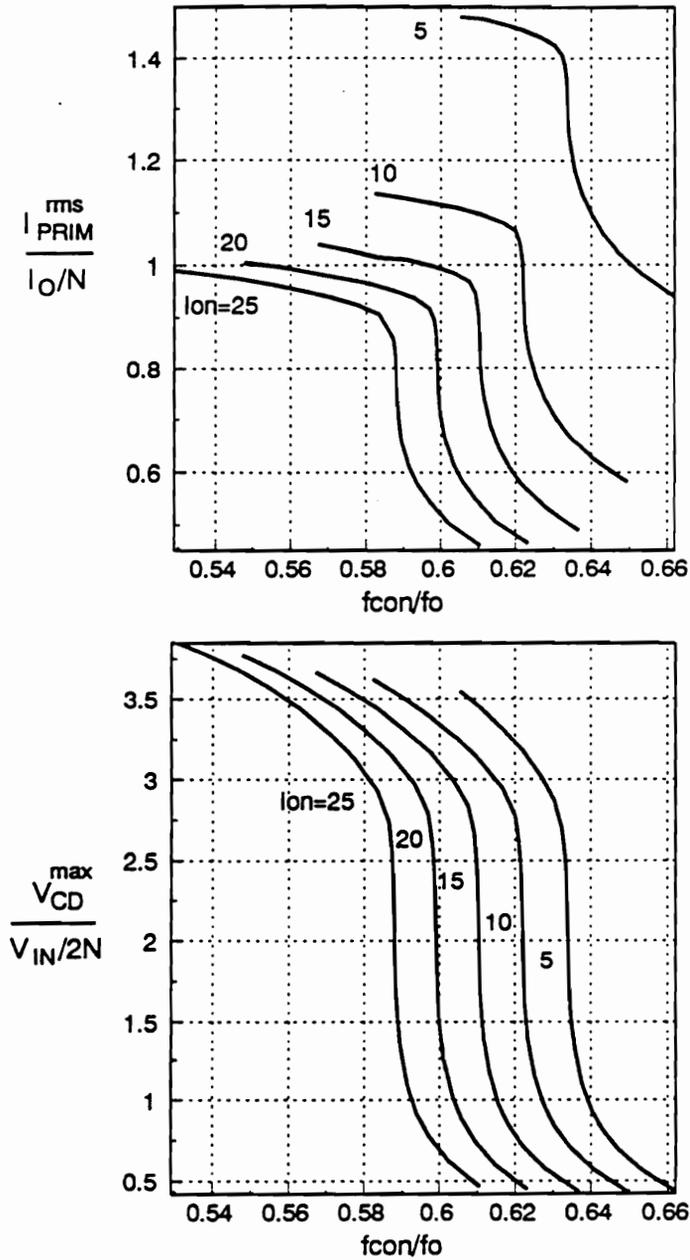
Figure C.17b. Normalized primary rms current and maximum rectifier voltage characteristics for $C_N = 5$ and $L_N = 1$ as a function of the normalized switching frequency. The characteristics are plotted for $I_{SLN} = 1$ and $L/SL = 100$; $C_N = 2C_D/(CN^2)$, $L_N = 4L_M/(LN^2)$, $I_{SLN} = I_{SAT}/(I_O/N)$, $Z_O = \sqrt{L_M/2C}$, $I_O = 2I_O Z_O/(V_{IN} N)$, and $f_O = 1/2\pi\sqrt{2CL_M}$.
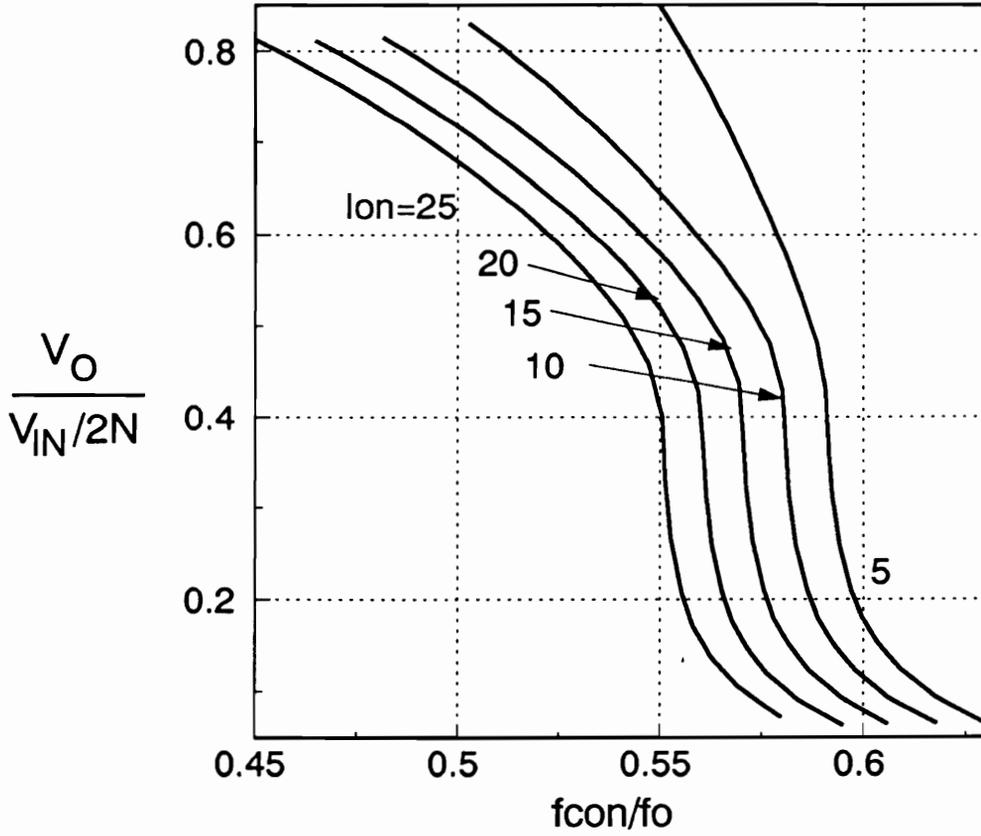
Figure C.18a. DC voltage-conversion-ratio characteristics as a function of the normalized switching frequency for $C_N = 10$ and $L_N = 1$. The characteristics are plotted for $I_{SLN} = 1$ and $L/SL = 100$; $C_N = 2C_D/(CN^2)$, $L_N = 4L_M/(LN^2)$, $I_{SLN} = I_{SAT}/(I_O/N)$, $Z_O = \sqrt{L_M/2C}$, $I_O = 2I_O Z_O/(V_{IN}N)$, and $f_O = 1/2\pi\sqrt{2CL_M}$.
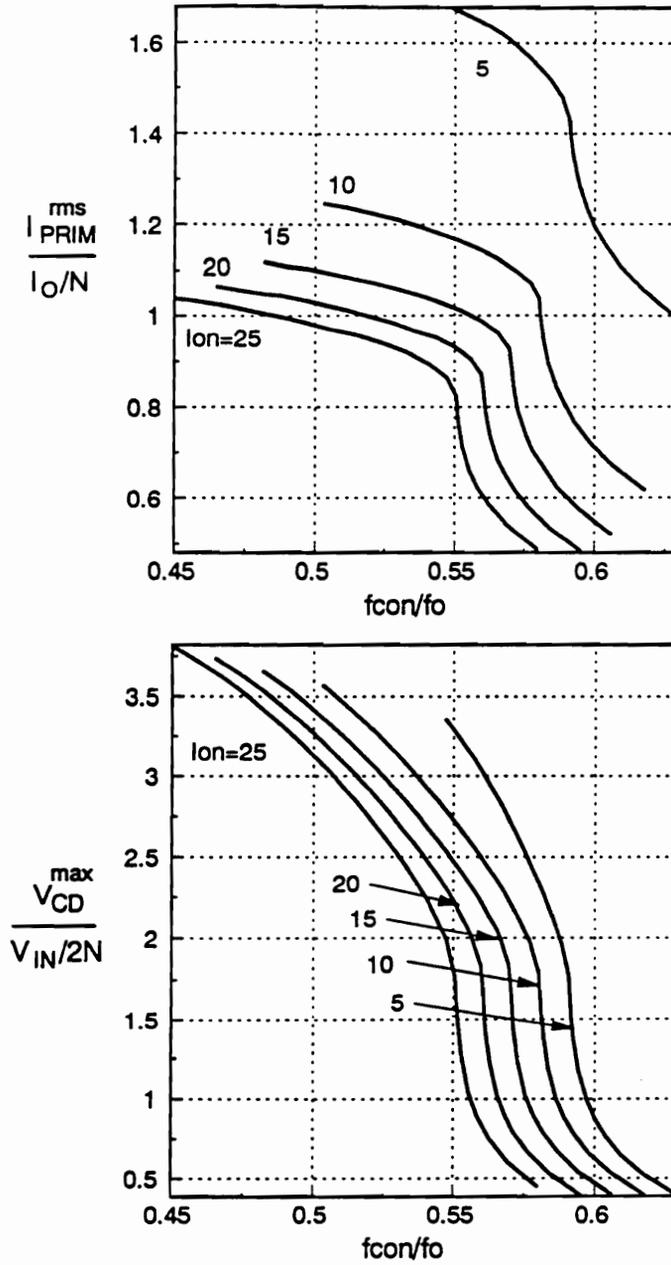
Figure C.18b. Normalized primary rms current and maximum rectifier voltage characteristics for $C_N = 10$ and $L_N = 1$ as a function of the normalized switching frequency. The characteristics are plotted for $I_{SLN} = 1$ and $L/SL = 100$; $C_N = 2C_D/(CN^2)$, $L_N = 4L_M/(LN^2)$, $I_{SLN} = I_{SAT}/(I_O/N)$, $Z_O = \sqrt{L_M/2C}$, $I_O = 2I_O Z_O/(V_{IN} N)$, and $f_O = 1/2\pi\sqrt{2CL_M}$.
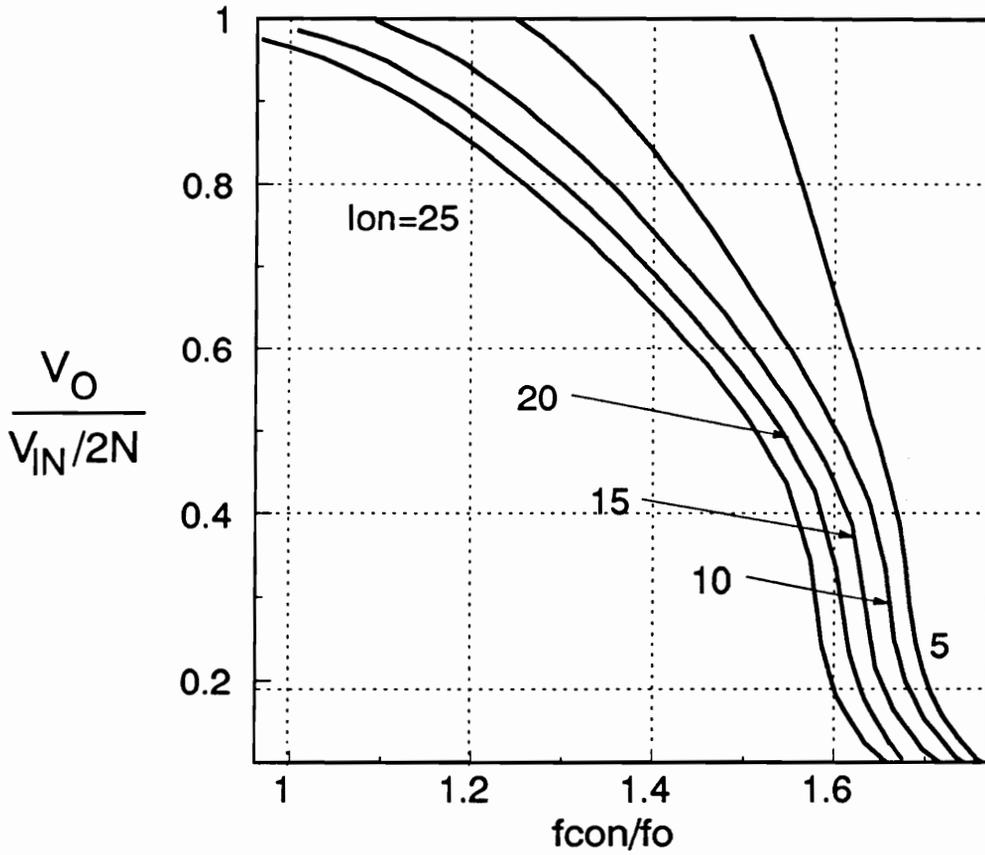
Figure C.19a. DC voltage-conversion-ratio characteristics as a function of the normalized switching frequency for $C_N = 5$ and $L_N = 3$. The characteristics are plotted for $I_{SLN} = 1$ and $L/SL = 100$; $C_N = 2C_D/(CN^2)$, $L_N = 4L_M/(LN^2)$, $I_{SLN} = I_{SAT}/(I_O/N)$, $Z_O = \sqrt{L_M/2C}$, $I_O = 2I_O Z_O/(V_{IN}N)$, and $f_O = 1/2\pi\sqrt{2CL_M}$.
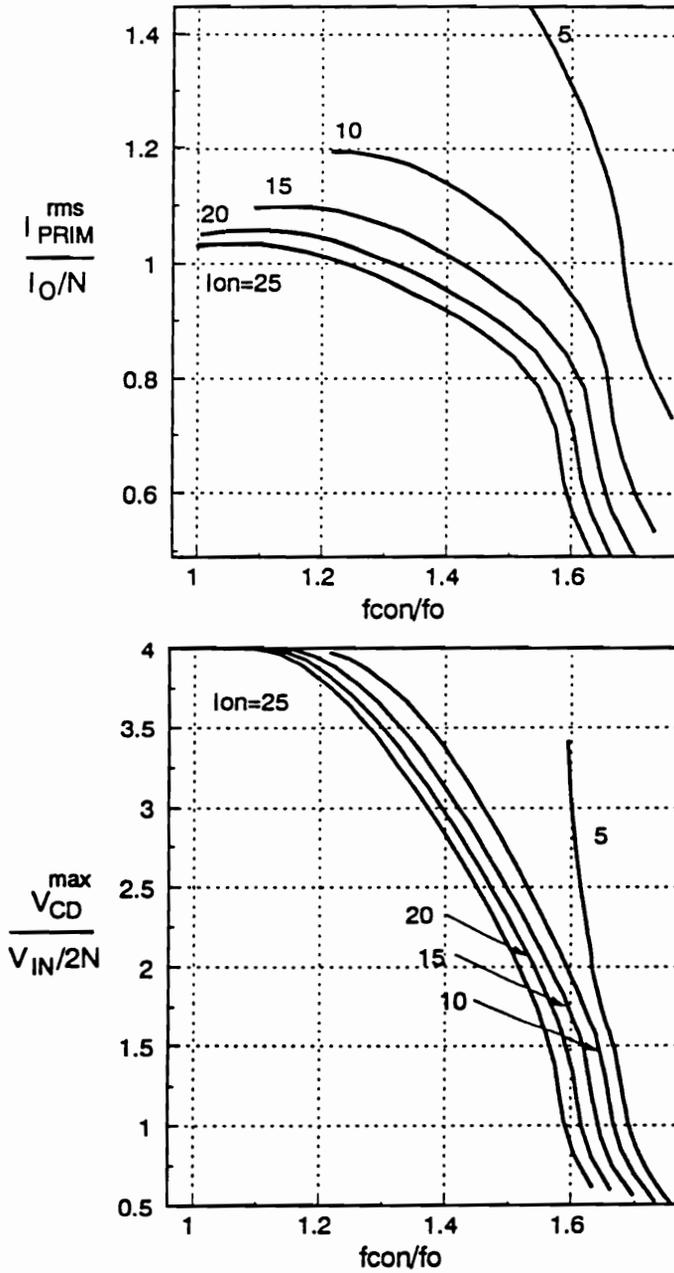
Figure C.19b. Normalized primary rms current and maximum rectifier voltage characteristics for $C_N = 5$ and $L_N = 3$ as a function of the normalized switching frequency. The characteristics are plotted for $I_{SLN} = 1$ and $L/SL = 100$; $C_N = 2C_D/(CN^2)$, $L_N = 4L_M/(LN^2)$, $I_{SLN} = I_{SAT}/(I_O/N)$, $Z_O = \sqrt{L_M/2C}$, $I_O = 2I_O Z_O/(V_{IN}N)$, and $f_O = 1/2\pi\sqrt{2CL_M}$.
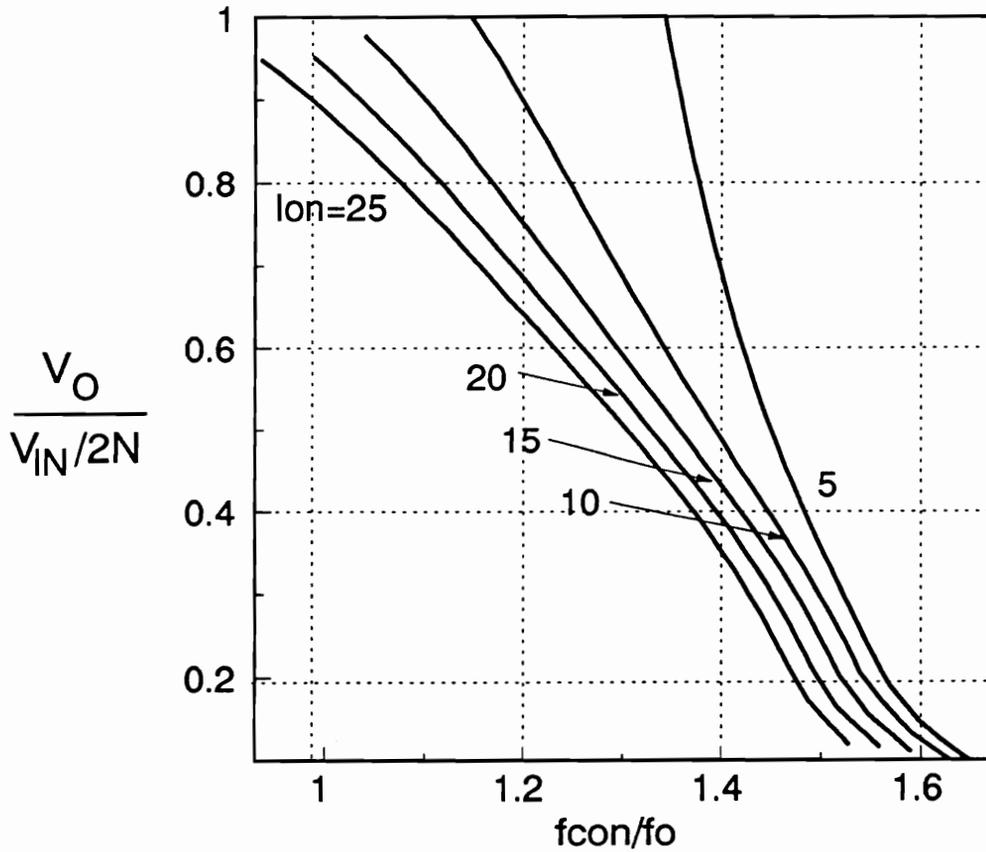
Figure C.20a. DC voltage-conversion-ratio characteristics as a function of the normalized switching frequency for $C_N = 10$ and $L_N = 3$. The characteristics are plotted for $I_{SLN} = 1$ and $L/SL = 100$; $C_N = 2C_D/(CN^2)$, $L_N = 4L_M/(LN^2)$, $I_{SLN} = I_{SAT}/(I_O/N)$, $Z_O = \sqrt{L_M/2C}$, $I_O = 2I_O Z_O/(V_{IN}N)$, and $f_O = 1/2\pi\sqrt{2CL_M}$.
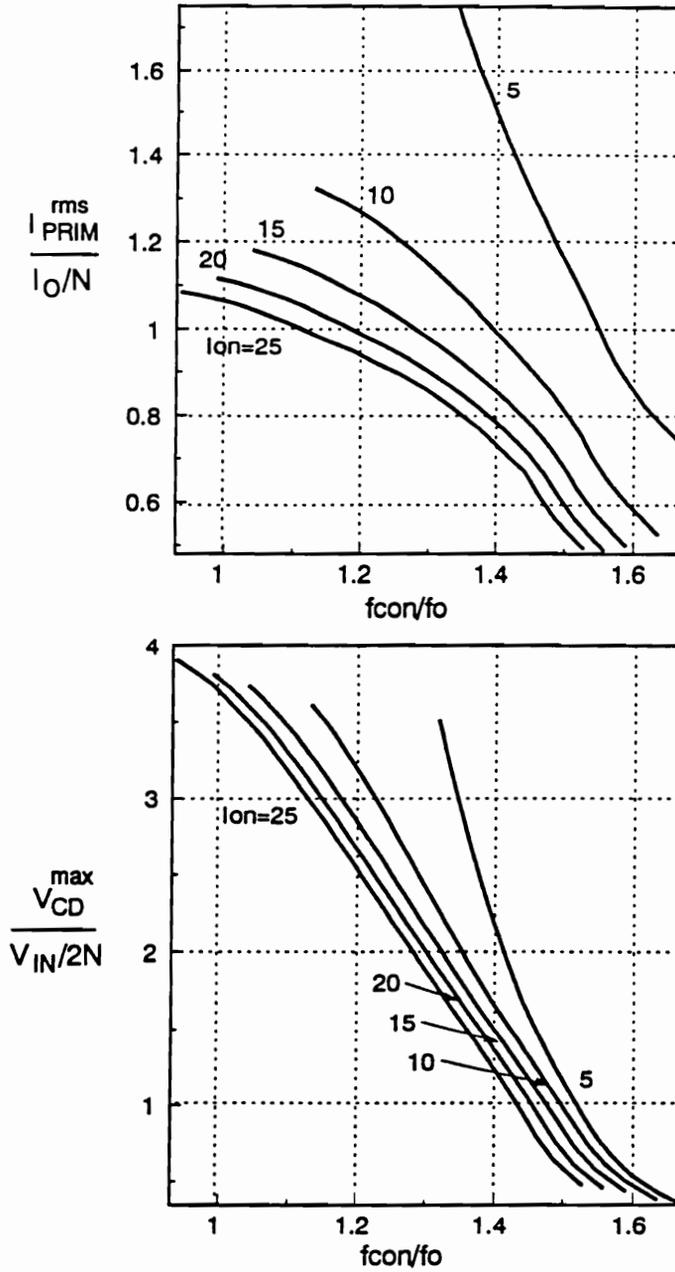
Figure C.20b. Normalized primary rms current and maximum rectifier voltage characteristics for $C_N = 10$ and $L_N = 3$ as a function of the normalized switching frequency. The characteristics are plotted for $I_{SLN} = 1$ and $L/SL = 100$; $C_N = 2C_D/(CN^2)$, $L_N = 4L_M/(LN^2)$, $I_{SLN} = I_{SAT}/(I_O/N)$, $Z_O = \sqrt{L_M/2C}$, $I_O = 2I_OZ_O/(V_{IN}N)$, and $f_O = 1/2\pi\sqrt{2CL_M}$.
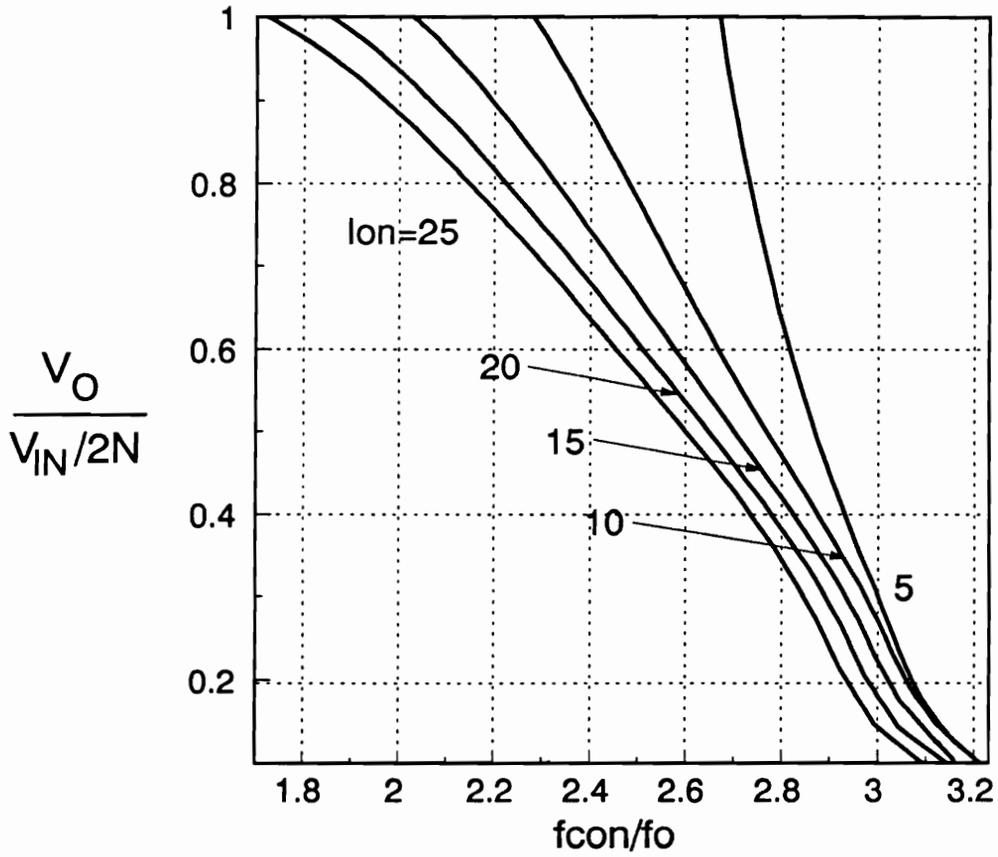
Figure C.21a.   DC voltage-conversion-ratio characteristics as a function of the normalized switch-
ing frequency for $C_N = 5$ and $L_N = 6$. The characteristics are plotted for $I_{SLN} = 1$ and
$L/SL = 100$; $C_N = 2C_D/(CN^2)$, $L_N = 4L_M/(LN^2)$, $I_{SLN} = I_{SAT}/(I_O/N)$, $Z_O = \sqrt{L_M/2C}$,
$I_O = 2I_OZ_O/(V_{IN}N)$, and $f_O = 1/2\pi\sqrt{2CL_M}$.
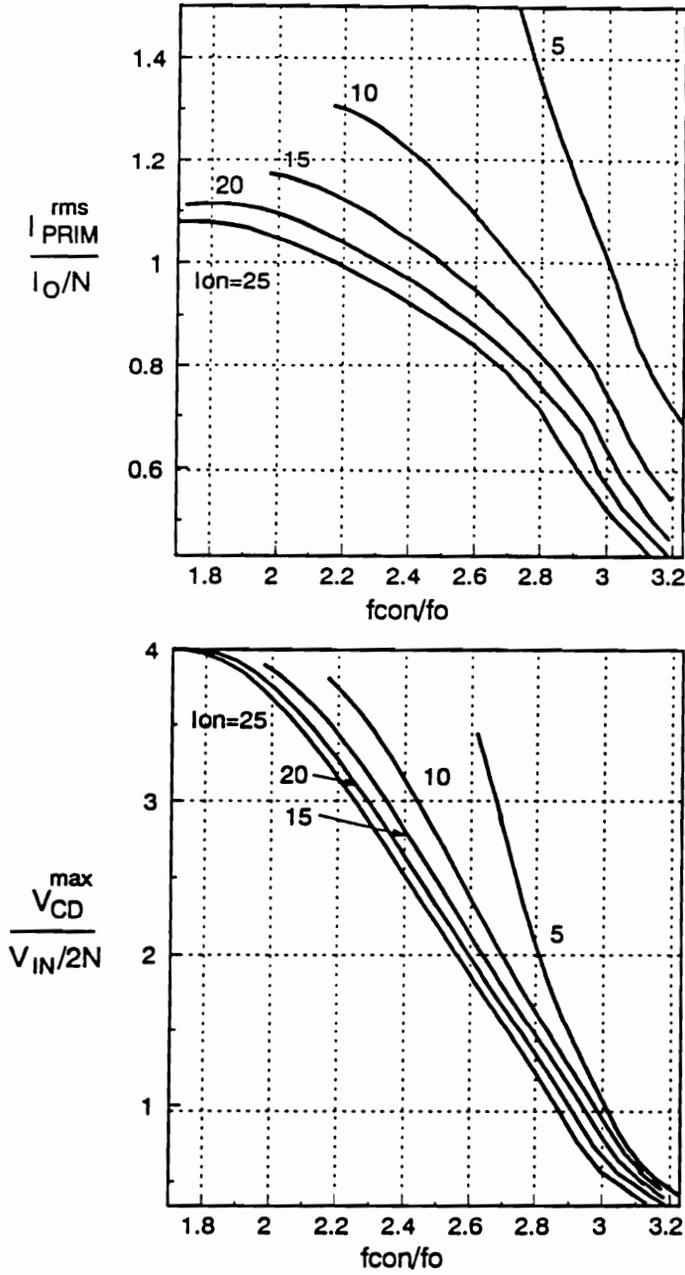
Figure C.21b. Normalized primary rms current and maximum rectifier voltage characteristics for $C_N=5$ and $L_N=6$ as a function of the normalized switching frequency. The characteristics are plotted for $I_{SLN} = 1$ and $L/SL = 100$; $C_N = 2C_D/(CN^2)$, $L_N = 4L_M/(LN^2)$, $I_{SLN} = I_{SAT}/(I_O/N)$, $Z_O = \sqrt{L_M/2C}$, $I_O = 2I_O Z_O/(V_{IN}N)$, and $f_O = 1/2\pi\sqrt{2CL_M}$.
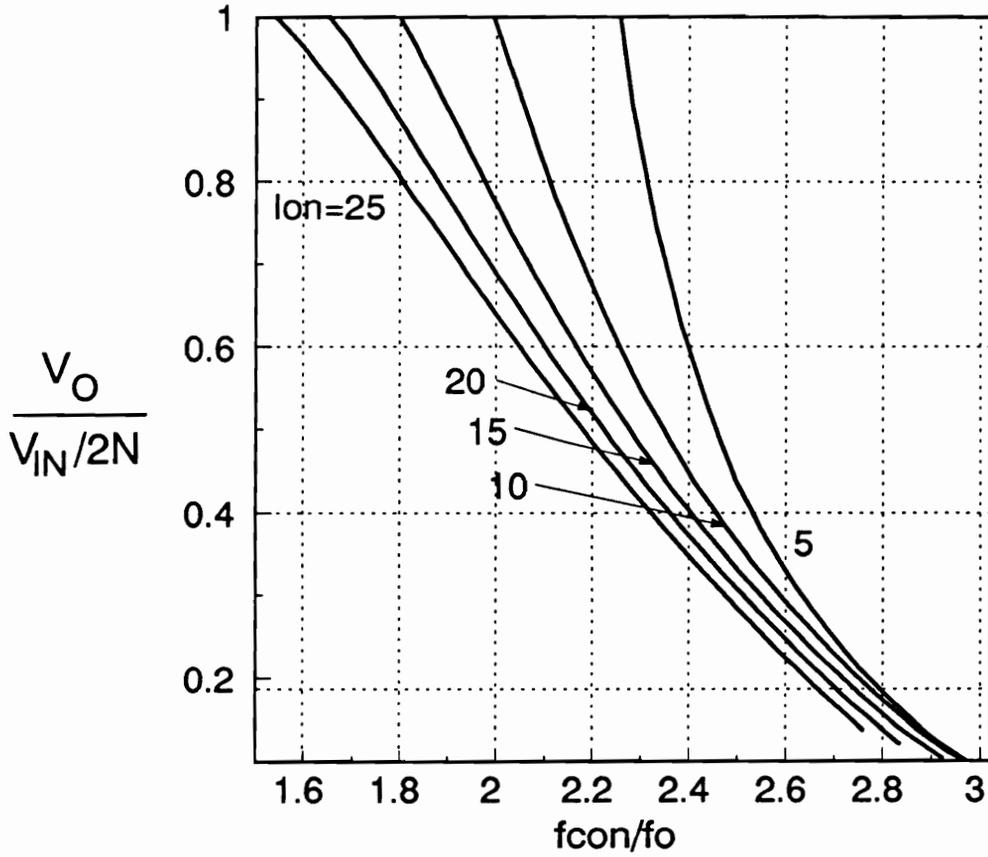
Figure C.22a. DC voltage-conversion-ratio characteristics as a function of the normalized switching frequency for $C_N = 10$ and $L_N = 6$. The characteristics are plotted for $I_{SLN} = 1$ and $L/SL = 100$; $C_N = 2C_D/(CN^2)$, $L_N = 4L_M/(LN^2)$, $I_{SLN} = I_{SAT}/(I_O/N)$, $Z_O = \sqrt{L_M/2C}$, $I_O = 2I_O Z_O/(V_{IN}N)$, and $f_O = 1/2\pi\sqrt{2CL_M}$.
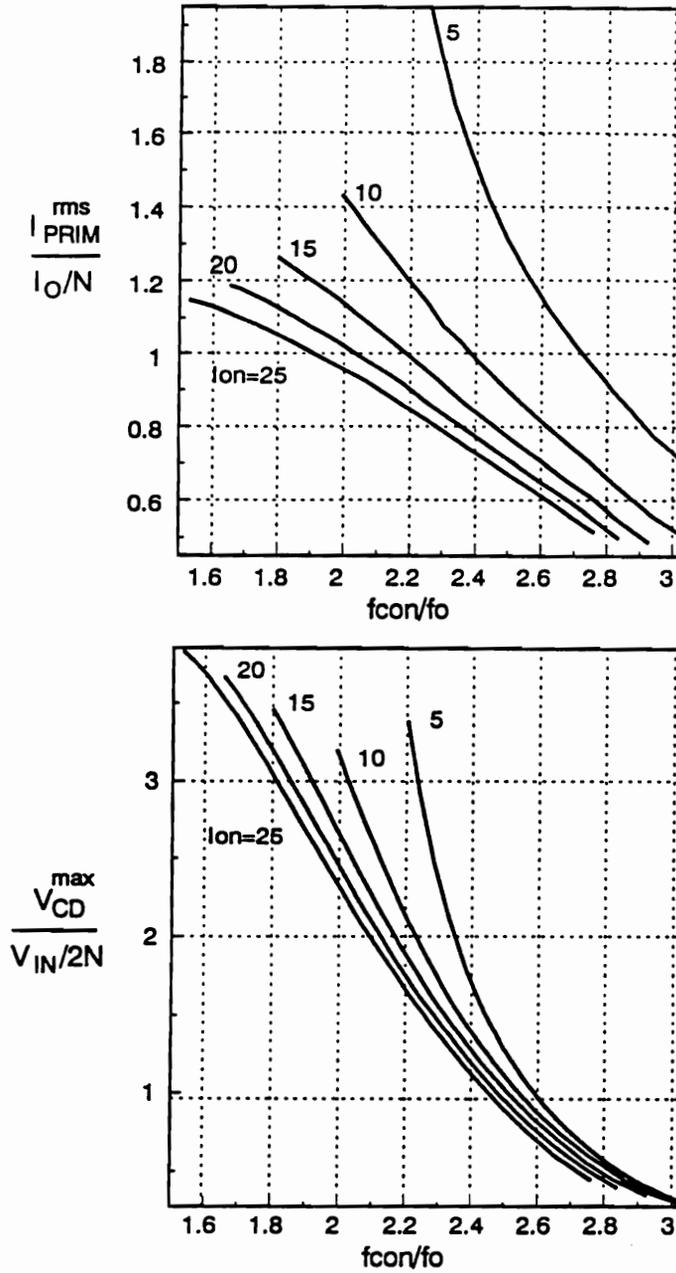
Figure C.22b. Normalized primary rms current and maximum rectifier voltage characteristics for $C_N = 10$ and $L_N = 6$ as a function of the normalized switching frequency. The characteristics are plotted for $I_{SLN} = 1$ and L/SL $= 100$; $C_N = 2C_D/(CN^2)$, $L_N = 4L_M/(LN^2)$, $I_{SLN} = I_{SAT}/(I_O/N)$, $Z_O = \sqrt{L_M/2C}$, $I_O = 2I_O Z_O/(V_{IN}N)$, and $f_O = 1/2\pi\sqrt{2CL_M}$.
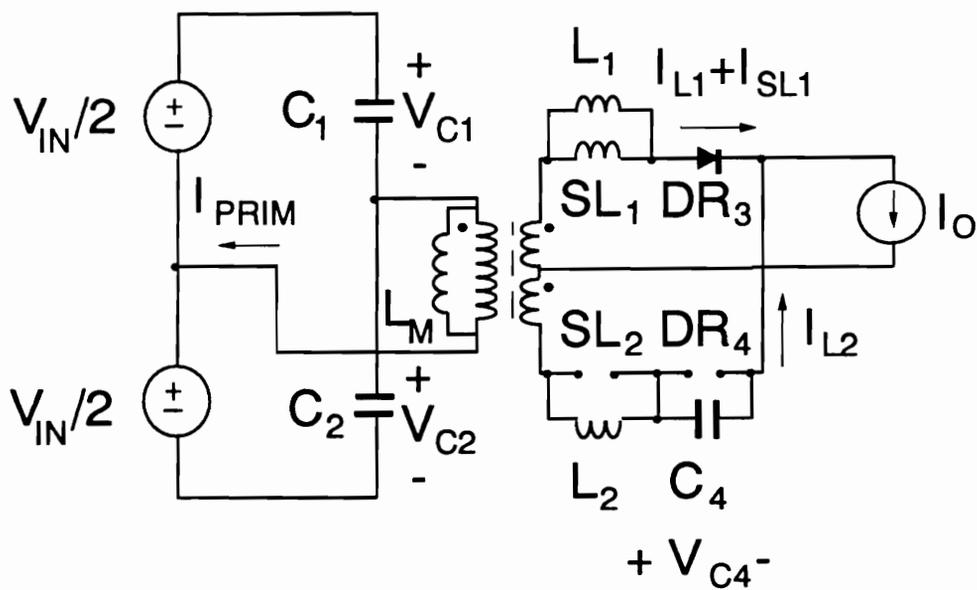
Figure C.23.   Topological Stage A of ideal HB ZVS-MRC (L_M).

$$i_{PRIM}(T_{AO}) = I_{PRIM}^{A} \qquad (C.1.c)$$

$$i_{LM}(T_{AO}) = I_{LM}^{A} \qquad (C.1.d)$$

$$v_{C3}(T_{AO}) = 0 \qquad (C.1.e)$$

$$v_{C4}(T_{AO}) = V_{C4}^{A} \qquad (C.1.f)$$

$$i_{L1}(T_{AO}) = I_{L1}^{A} \qquad (C.1.g)$$

$$i_{L2}(T_{AO}) = I_{L2}^{A} \qquad (C.1.h)$$

$$i_{SL1}(T_{AO}) = I_{SL1}^{A} \qquad (C.1.i)$$

$$i_{SL2}(T_{AO}) = 0 \qquad (C.1.j)$$

Equations:

$$v_{C1}(t) + v_{C2}(t) = V_{IN} \qquad (C.2.a)$$

$$C \frac{dv_{C1}(t)}{dt} = C \frac{dv_{C2}(t)}{dt} + i_{LM}(t) + i_{PRIM}(t) \qquad (C.2.b)$$

$$i_{PRIM}(t) = \frac{1}{N} [i_{L1}(t) + i_{SL1}(t) - i_{L2}(t)] \qquad (C.2.c)$$

$$v_{L1}(t) = v_{SL1}(t) = L \frac{di_{L1}(t)}{dt} = SL \frac{di_{SL1}(t)}{dt} \qquad (C.2.d)$$

$$i_{L1}(t) + i_{SL1}(t) + i_{L2}(t) = I_O \tag{C.2.e}$$

$$i_{L2}(t) = i_{C4}(t) = C_D \frac{dv_{C4}(t)}{dt} \tag{C.2.f}$$

$$\frac{V_{IN}(t)}{2} = v_{C1}(t) + L_M \frac{di_{LM}(t)}{dt} \tag{C.2.g}$$

$$\frac{V_{IN}}{2} = L \frac{di_{L1}(t)}{dt} - v_{C4}(t) - L \frac{di_{L2}(t)}{dt} \tag{C.2.h}$$

From Eqs. (C.1.a) - (C.2.h), it follows that:

$$\frac{d^4 v_{C4}(t)}{dt^4} + \frac{d^2 v_{C4}(t)}{dt^2} \left[\frac{K_1 L_N}{C_N} + 1 + K_1 L_N \right] \omega_O^2 + \frac{dv_{C4}(t)}{dt} \frac{K_1 L_N}{C_N} \omega_O^4 = 0 \tag{C.3.a}$$

where

$$\omega_O = \frac{1}{\sqrt{2L_M C}} \tag{C.3.b}$$

$$K_1 = \frac{1 + \dfrac{L}{SL}}{2 + \dfrac{L}{SL}} \tag{C.3.c}$$

$$C_N = \frac{2C_D}{N^2 C} \tag{C.3.d}$$

$$L_N = \frac{4L_M}{N^2 L} \qquad (C.3.e)$$

$$Z_O = \sqrt{\frac{L_M}{2C}} \qquad (C.3.f)$$

$$a_1 = (K_1 \frac{L_N}{C_N} + 1 + K_1 L_N)\omega_O^2 \qquad (C.3.g)$$

$$a_2 = \frac{K_1 L_N}{C_N}\omega_O^4 \qquad (C.3.h)$$

The roots of Eq. (C.3.a) are:

$$\mp j\gamma = \mp \sqrt{\frac{-a_1 - \sqrt{a_1^2 - 4a_2}}{2}} \qquad (C.3.i)$$

$$\mp j\beta = \mp \sqrt{\frac{-a_1 + \sqrt{a_1^2 - 4a_2}}{2}} \qquad (C.3.j)$$

It should be noted that $C_D/(N/2)^2$ represents the reflected capacitance of the rectifier into the primary where $C_D = C_3 = C_4$. This reflected capacitance is seen in series with switch capacitances C_1 and C_2, which are effectively connected in parallel. Therefore, C_N can be regarded as a ratio of the reflected rectifier capacitances into the primary and total primary switch capacitance, $C_1 + C_2 = 2C$. Similarly, $L(N/2)^2$ represents the reflected secondary resonant inductors into the primary. L_N is the ratio of the magnetizing inductance L_M and the reflected resonant inductors $L(N/2)^2$.

Solution:

$$v_{C4}^A = a_A \cos \gamma t + b_A \sin \gamma t + c_A \cos \beta t + d_A \sin \beta t \tag{C.4.a}$$

$$i_{L2}^A = C_D[b_A\gamma \cos \gamma t - a_A\gamma \sin \gamma t + d_A\beta \cos \beta t - c_A\beta \sin \beta t] \tag{C.4.b}$$

$$i_{LM}^A = CN[b_A\gamma \cos \gamma t - a_A\gamma \sin \gamma t + d_A\beta \cos \beta t - c_A\beta \sin \beta t - K_2K_1[b_A\gamma^3 \cos \gamma t$$

$$- a_A\gamma^3 \sin \gamma + d_A\beta^3 \cos \beta t - c_A\beta^3 \sin \beta t]] - \frac{1}{N}[I_O - 2i_{L2}(t)] \tag{C.4.c}$$

$$v_{C1}^A = \frac{V_{IN}}{2} + \frac{1}{2}[a_A N \cos \gamma t + b_A N \sin \gamma t + c_A N \cos \beta t + d_A N \sin \beta t$$

$$- K_2K_1N[a_A\gamma^2 \cos \gamma t + b_A\gamma^2 \sin \gamma t + c_A\beta^2 \cos \beta t + d_A\beta^2 \sin \beta t]] \tag{C.4.d}$$

$$i_{L1}^A = \frac{C_D}{1 + \dfrac{L}{SL}}[b_A\gamma(\cos \gamma t - 1) - a_A\gamma \sin \gamma t + d_A\beta(\cos \beta t - 1) - c_A\beta \sin \beta t] + I_{L1}^A \tag{C.4.e}$$

$$i_{SL2}^A = I_O - i_{L1}^A - i_{L2}^A \tag{C.4.f}$$

where

$$d_A = \frac{I_{LM}^A + \dfrac{I_O}{N} - I_{L2}^A(1 - K_2\gamma^2)\dfrac{NC}{C_D} - I_{L2}^A\dfrac{2}{N}}{NC\beta K_2[\gamma^2 - \beta^2]} \tag{C.5.a}$$

$$b_A = \frac{I_{L2}^A - C_D\beta d_A}{\gamma C_D} \tag{C.5.b}$$

$$c_A = \frac{2(\frac{V_{IN}}{2} - V_{C1}^A) + N V_{C4}^A (1 - K_2 \gamma^2)}{N K_2 (\beta^2 - \gamma^2)} \qquad (C.5.c)$$

$$a_A = V_{C4}^A - c_A \qquad (C.5.d)$$

$$K_2 = \frac{C_N}{L_N \omega_O^2} \qquad \cdot \qquad (C.5.e)$$

Initial conditions I_{L1}^A, I_{L2}^A, V_{C4}^A, I_{LM}^A, and V_{C1}^A are determined from the stage preceding Stage A. Normalizing voltages with respect to $V_{IN}/2$, current with respect to I_O/N, and time with respect to $1/f_O$, Eqs. (C.4.a) - (C.4.d) become:

$$v_{C4}^{AN} = a_{AN} \cos \gamma_N t_N + b_N \sin \gamma_N t_N + c_{AN} \cos \beta_N t_N + d_N \sin \beta_N t_N \qquad (C.6.a)$$

$$i_{L2}^{AN} = \frac{C_N}{4 I_{ON}} [b_{AN} \gamma_S \cos \gamma_N t_N - a_{AN} \gamma_S \sin \gamma_N t_N + d_{AN} \beta_S \cos \beta_N t_N - c_{AN} \beta_S \sin \beta_N t_N] \qquad (C.6.b)$$

$$v_{C1}^{AN} = 1 + [a_{AN} \cos \gamma_N t_N + b_{AN} \sin \gamma_N t_N + c_{AN} \cos \beta_N t_N + d_{AN} \sin \beta_N t_N$$

$$- \frac{C_N}{L_N} K_1 [a_{AN} \gamma_S^2 \cos \gamma_N t_N + b_{AN} \gamma_S^2 \sin \gamma_N t_N + c_{AN} \beta_S^2 \cos \beta_N t_N + d_{AN} \beta_S^2 \sin \beta_N t_N]] \qquad (C.6.c)$$

$$i_{LM}^{AN} = [b_{AN} \gamma_S^2 \cos \gamma_N t_N - a_{AN} \gamma_S^2 \sin \gamma_N t_N + d_{AN} \beta_S^2 \cos \beta_N t_N - c_{AN} \beta_S^2 \sin \beta_N t_N$$

$$- \frac{C_N}{L_N} K_1 [b_{AN} \gamma_S^3 \cos \gamma_N t_N - a_{AN} \gamma_S^3 \sin \gamma_N t_N + d_{AN} \beta_S^3 \cos \beta_N t_N \qquad (C.6.d)$$

$$- c_{AN} \beta_S^3 \sin \beta_N t_N]]/I_{ON} - 1 + 2 I_{L2}^{AN}$$

$$i_{L1}^{AN} = \frac{C_N}{4I_{ON}(1 + \frac{L}{SL})} [b_{AN}\gamma_S(\cos \gamma_N t_N - 1) - a_{AN}\gamma_S \sin \gamma_N t_N$$

$$+ d_{AN}\beta_S(\cos \beta_N t_N - 1) - c_{AN}\beta_S \sin \beta_N t_N] + i_{L1}^{AN} \qquad (C.6.e)$$

$$i_{SL2}^{AN} = 1 - I_{L1}^{AN} - I_{L2}^{AN} \qquad (C.6.e)$$

where

$$I_{ON} = \frac{2Z_O I_O}{N V_{IN}} \qquad (C.7.a)$$

$$\gamma_N = \frac{\gamma}{f_O} \qquad (C.7.b)$$

$$\gamma_S = \frac{\gamma}{\omega_O} \qquad (C.7.c)$$

$$\beta_N = \frac{\beta}{f_O} \qquad (C.7.d)$$

$$\beta_S = \frac{\beta}{\omega_O} \qquad (C.7.e)$$

$$d_{AN} = \frac{2I_{ON}[I_{LM}^{AN} + 1 - \frac{2I_{L2}^{AN}}{C_N}(1 - \frac{C_N}{L_N}\gamma_S^2) - 2I_{L2}^{AN}]}{\frac{C_N}{L_N}\beta_S(\gamma_S^2 - \beta_S^2)} \qquad (C.7.f)$$

$$b_{AN} = \frac{4I_{L2}^{AN} I_{ON}}{\gamma_S C_N} - \frac{\beta_S}{\gamma_S} d_{AN} \qquad (C.7.g)$$

$$c_{AN} = \frac{2(1 - V_{C1}^{AN}) + V_{C4}^{AN}(1 - \frac{C_N}{L_N} \gamma_S^2)}{\frac{C_N}{L_N}(\beta_S^2 - \gamma_S^2)} \qquad (C.7.h)$$

$$a_{AN} = V_{C4}^{AN} - c_{AN} \qquad (C.7.i)$$

Stage Duration $T_A = T_{A1} - T_{AO}$

Stage duration T_A is determined from the condition:

$$v_{C1}(T_A) = \frac{V_{IN}}{2} . \qquad (C.8)$$

To solve for T_A, it is necessary to solve a transcendental equation.

STAGE B [T_{BO}, T_{B1}] (Fig. C.24)

Initial Conditions:
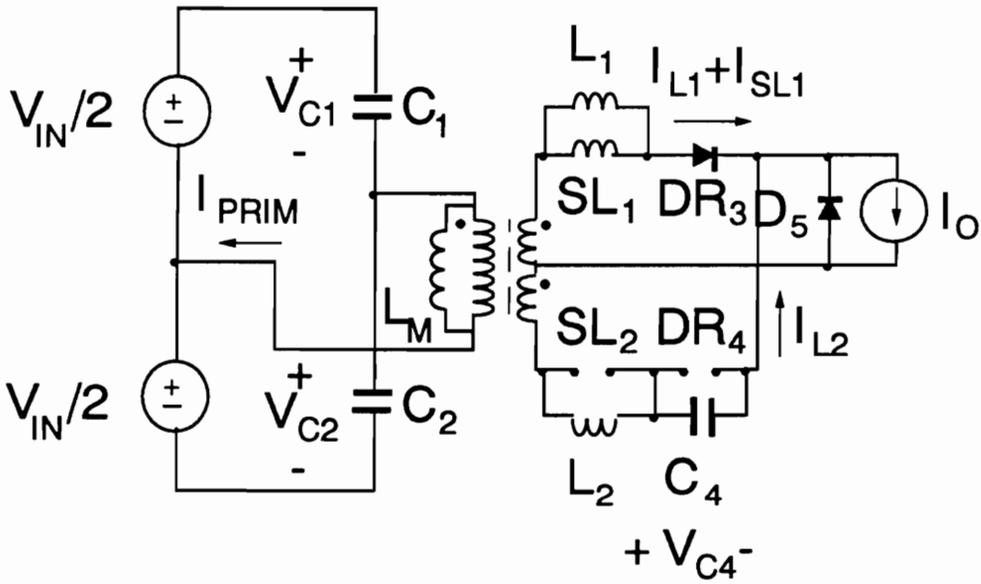
$$v_{C1}(T_{BO}) = \frac{V_{IN}}{2} \qquad (C.9.a)$$

Figure C.24. Topological Stage B of ideal HB ZVS-MRC (L_M)

$$v_{C2}(T_{BO}) = \frac{V_{IN}}{2} \qquad\qquad (C.9.b)$$

$$i_{PRIM}(T_{BO}) = I_{PRIM}^{B} \qquad\qquad (C.9.c)$$

$$i_{LM}(T_{BO}) = I_{LM}^{B} \qquad\qquad (C.9.d)$$

$$v_{C3}(T_{BO}) = 0 \qquad\qquad (C.9.e)$$

$$v_{C4}(T_{BO}) = V_{C4}^{B} \qquad\qquad (C.9.f)$$

$$i_{L1}(T_{BO}) = I_{L1}^{B} \qquad\qquad (C.9.g)$$

$$i_{L2}(T_{BO}) = I_{L2}^{B} \qquad\qquad (C.9.h)$$

$$i_{SL1}(T_{BO}) = I_{SL1}^{B} \qquad\qquad (C.9.i)$$

$$i_{SL2}(T_{BO}) = 0 \qquad\qquad (C.9.j)$$

Equations:

$$v_{C1}(t) + v_{C2}(t) = V_{IN} \qquad\qquad (C.10.a)$$

$$C\frac{dv_{C1}(t)}{dt} = C\frac{dv_{C2}(t)}{dt} + i_{LM}(t) + i_{PRIM}(t) \qquad\qquad (C.10.b)$$

$$i_{PRIM}(t) = \frac{1}{N}\left[i_{L1}(t) + i_{SL1}(t) - i_{L2}(t)\right] \qquad\qquad (C.10.c)$$

$$\frac{V_{IN}}{2N} = v_{L1}(t) = v_{SL1}(t) = L\,\frac{di_{L1}(t)}{dt} = SL\,\frac{di_{SL1}(t)}{dt} \qquad (C.10.d)$$

$$i_{L1}(t) + i_{SL1}(t) + i_{L2}(t) = 0 \qquad (C.10.e)$$

$$i_{L2}(t) = i_{C4}(t) = C_D\,\frac{dv_{C4}(t)}{dt} \qquad (C.10.f)$$

$$\frac{V_{IN}}{2N} = v_{C4}(t) + L\,\frac{di_{L2}(t)}{dt} \qquad (C.10.g)$$

$$\frac{V_{IN}(t)}{2} = v_{C1}(t) + L_M\,\frac{di_{LM}(t)}{dt} \qquad (C.10.h)$$

From Eqs. (C.9.a) - (C.10.h), it follows that:

$$\frac{d^4 v_{C4}(t)}{dt^4} + \frac{d^2 v_{C4}(t)}{dt^2}\,[\,\frac{L_N}{C_N} + K_3\,]\omega_O^2 + \frac{dv_{C4}(t)}{dt}\,[\,\frac{L_N}{C_N}K_3 - \frac{L_N^2}{4C_N}\,]\omega_O^4 = 0 \qquad (C.11.a)$$

where

$$K_3 = 1 + \frac{L_N}{2}\,(1 + \frac{L}{2SL}\,) \qquad (C.11.b)$$

$$a_1 = (\,\frac{L_N}{C_N} + K_3)\omega_O^2 \qquad (C.11.c)$$

$$a_2 = \frac{L_N}{C_N}\,[K_3 - \frac{L_N}{4}\,]\omega_O^4 \qquad (C.11.d)$$

The roots of Eq. (C.11.a) are:

$$\mp j\gamma = \mp \sqrt{\frac{-a_1 - \sqrt{a_1^2 - 4a_2}}{2}} \tag{C.11.e}$$

$$\mp j\beta = \mp \sqrt{\frac{-a_1 + \sqrt{a_1^2 - 4a_2}}{2}} \tag{C.11.f}$$

Solution:

$$v_{C4}^B = a_B \cos \gamma t + b_B \sin \gamma t + c_B \cos \beta t + d_B \sin \beta t \tag{C.12.a}$$

$$i_{L2}^B = C_D[b_B\gamma \cos \gamma t - a_B\gamma \sin \gamma t + d_B\beta \cos \beta t - c_B\beta \sin \beta t] \tag{C.12.b}$$

$$i_{LM}^B = \frac{N}{L_M} \left[\frac{b_B}{\gamma} \cos \gamma t - \frac{a_B}{\gamma} \sin \gamma t + \frac{d_B}{\beta} \cos \beta t - \frac{c_B}{\beta} \sin \beta t + K_2[a_B\gamma \sin \gamma t \right.$$

$$\left. - b_B\gamma \cos \gamma t + c_B\beta \sin \beta t - d_B\beta \cos \beta t]\right] + e_B \tag{C.12.c}$$

$$v_{C1}^B = \frac{V_{IN}}{2} + N[a_B \cos \gamma t + b_B \sin \gamma t + c_B \cos \beta t + d_B \sin \beta t - K_2[a_B\gamma^2 \cos \gamma t$$

$$+ b_B\gamma^2 \sin \gamma t + c_B\beta^2 \cos \beta t + d_B\beta^2 \sin \beta t]] \tag{C.12.d}$$

$$i_{L1}^B = \frac{1}{L_1} \left[\frac{b_B}{\gamma} \cos \gamma t - \frac{a_B}{\gamma} \sin \gamma t + \frac{d_B}{\beta} \cos \beta t - \frac{c_B}{\beta} \sin \beta t + K_2[a_B\gamma \sin \gamma t \right.$$

$$\left. - b_B\gamma \cos \gamma t + c_B\beta \sin \beta t - d_B\beta \cos \beta t]\right] + f_B \tag{C.12.e}$$

$$i_{SL1}^{B} = \frac{1}{SL} \left[\frac{b_B}{\gamma} \cos \gamma t - \frac{a_B}{\gamma} \sin \gamma t + \frac{d_B}{\beta} \cos \beta t - \frac{c_B}{\beta} \sin \beta t + K_2[a_B\gamma \sin \gamma t \right.$$

$$\left. - b_B\gamma \cos \gamma t + c_B\beta \sin \beta t - d_B\beta \cos \beta t] \right] + g_B \qquad (C.12.f)$$

where

$$d_B = \frac{I_{LM}^{B} + \frac{I_{L1}^{B}}{N} + \frac{I_{SL1}^{B}}{N} - I_{L2}^{B}[(1 - K_2\gamma^2)\frac{2CN}{C_D} + \frac{1}{N}]}{2CN\beta K_2(\gamma^2 - \beta^2)} \qquad (C.13.a)$$

$$b_B = \frac{I_{L2}^{B} - C_D\beta d_B}{\gamma C_D} \qquad (C.13.b)$$

$$c_B = \frac{\frac{(\frac{V_{IN}}{2} - V_{C1}^{B})}{N} + V_{C4}^{B}(1 - K_2\gamma^2)}{K_2(\beta^2 - \gamma^2)} \qquad (C.13.c)$$

$$a_B = V_{C4}^{B} - c_B \qquad (C.13.d)$$

$$f_B = I_{L1}^{B} - \frac{1}{L} \left[\frac{b_B}{\gamma} + \frac{d_B}{\beta} - K_2(\gamma b_B - \beta d_B) \right] \qquad (C.13.e)$$

$$e_B = I_{LM}^{B} - \frac{NL}{L_M} [I_{L1}^{B} - f_B] \qquad (C.13.f)$$

$$g_B = I_{SL1}^{B} - \frac{1}{SL} \left[\frac{b_B}{\gamma} + \frac{d_B}{\beta} - K_2(\gamma b_B - \beta d_B) \right] \qquad (C.13.g)$$

or in the normalized form:

$$v_{C4}^{BN} = a_{BN} \cos \gamma_N t_N + b_{BN} \sin \gamma_N t_N + c_{BN} \cos \beta_N t_N + d_{BN} \sin \beta_N t_N \qquad (C.14.a)$$

$$i_{L2}^{BN} = \frac{C_N}{4I_{ON}} [b_{BN}\gamma_S \cos \gamma_N t_N - a_{BN}\gamma_S \sin \gamma_N t_N + d_{BN}\beta_S \cos \beta_N t_N - c_{BN}\beta_S \sin \beta_N t_N] \quad (C.14.b)$$

$$v_{C1}^{BN} = 1 + [a_{BN} \cos \gamma_N t_N + b_{BN} \sin \gamma_N t_N + c_{BN} \cos \beta_N t_N + d_{BN} \sin \beta_N t_N$$

$$- \frac{C_N}{L_N} [a_{BN}\gamma_S^2 \cos \gamma_N t_N + b_{BN}\gamma_S^2 \sin \gamma_N t_N + c_{BN}\beta_S^2 \cos \beta_N t_N + d_{BN}\beta_S^2 \sin \beta_N t_N]] \quad (C.14.c)$$

$$i_{LM}^{BN} = [b_{BN}\gamma_S \cos \gamma_N t_N - a_{BN}\gamma_S \sin \gamma_N t_N + d_{BN}\beta_S \cos \beta_N t_N - c_{BN}\beta_S \sin \beta_N t_N$$

$$- \frac{C_N}{L_N} [b_{BN}\gamma_S^3 \cos \gamma_N t_N - a_{BN}\gamma_S^3 + d_{BN}\beta_S^3 \cos \beta_N t_N - c_{BN}\beta_S^3 \sin \beta_N t_N]]/I_{ON} \qquad (C.14.d)$$

$$- i_{L1}^{BN} - i_{SL1}^{BN} + i_{L2}^{BN}$$

$$i_{L1}^{BN} = \frac{L_N}{4I_{ON}} [\frac{b_{BN}}{\gamma_S} \cos \gamma_N t_N - \frac{a_{BN}}{\gamma_S} \sin \gamma_N t_N + \frac{d_{BN}}{\beta_S} \cos \beta_N t_N - \frac{c_{BN}}{\gamma_S} \sin \beta_N t_N$$

$$+ \frac{C_N}{L_N} [a_{BN}\gamma_S \sin \gamma_N t_N - b_{BN}\gamma_S \cos \gamma_N t_N + c_{BN}\beta_S \sin \beta_N t_N \qquad (C.14.e)$$

$$- d_{BN}\beta_S \cos \beta_N t_N]] + f_{BN}$$

$$i_{SL1}^{BN} = \frac{LL_N}{4I_{ON}SL} [\frac{b_{BN}}{\gamma_S} \cos \gamma_N t_N - \frac{a_{BN}}{\gamma_S} \sin \gamma_N t_N + \frac{d_{BN}}{\beta_S} \cos \beta_N t_N - \frac{c_{BN}}{\gamma_S} \sin \beta_N t_N$$

$$+ \frac{C_N}{L_N} [a_{BN}\gamma_S \sin \gamma_N t_N - b_{BN}\gamma_S \cos \gamma_N t_N + c_{BN}\beta_S \sin \beta_N t_N \qquad (C.14.f)$$

$$- d_{BN}\beta_S \cos \beta_N t_N]] + g_{BN}$$

where

$$\gamma_N = \frac{\gamma}{f_O} \qquad (C.15.a)$$

$$\gamma_S = \frac{\gamma}{\omega_O} \qquad (C.15.b)$$

$$\beta_N = \frac{\beta}{f_O} \qquad (C.15.c)$$

$$\beta_S = \frac{\beta}{\omega_O} \qquad (C.15.d)$$

$$d_{BN} = \frac{I_{ON}[I_{LM}^{BN} + I_{L1}^{BN} + I_{SL1}^{BN} - I_{L2}^{BN}(\frac{4}{C_N}[1 - \frac{C_N}{L_N}\gamma_S^2] + 1)]}{\frac{C_N}{L_N}\beta_S[\gamma_S^2 - \beta_S^2]} \qquad (C.15.e)$$

$$b_{BN} = \frac{4I_{L2}^{BN} I_{ON}}{\gamma_S C_N} - \frac{\beta_S}{\gamma_S} d_{BN} \qquad (C.15.f)$$

$$c_{BN} = \frac{V_{C1}^{BN} - 1 + V_{C4}^{BN}[1 - \frac{C_N}{L_N}\gamma_S^2]}{\frac{C_N}{L_N}(\beta_S^2 - \gamma_S^2)} \qquad (C.15.g)$$

$$a_{BN} = V_{C4}^{BN} - c_{BN} \qquad (C.15.h)$$

$$f_{BN} = I_{L1}^{BN} - I_{L2}^{BN} \frac{L_N(1 - \frac{C_N}{L_N} \gamma_S^2)}{C_N \gamma_S^2} - \frac{d_{BN} L_N}{4 \beta_S} \left[1 - \frac{C_N}{L_N} \beta_S^2 - \left(\frac{\beta_S}{\gamma_S} \right)^2 \left(1 - \frac{C_N}{L_N} \gamma_S^2 \right) \right] \qquad (C.15.i)$$

$$g_{BN} = I_{SL1}^{BN} - \frac{LL_N}{4SL} \left[b_{BN} \frac{(1 - \frac{C_N}{L_N} \gamma_S^2)}{\gamma_S} + d_{BN} \frac{(1 - \frac{C_N}{L_N} \beta_S^2)}{\beta_S} \right] \qquad (C.15.j)$$

$$e_{BN} = I_{LM}^{BN} - 4L_N [I_{L1}^{BN} - f_{BN}] \qquad (C.15.k)$$

Stage Duration $T_B = T_{B1} - T_{BO}$

Stage duration T_B is determined from the condition:

$$v_{C1}(T_B) = V_{IN} \qquad (C.16.a)$$

or

$$i_{SL1}(T_B) = 0. \qquad (C.16.b)$$

STAGE C $[T_{CO}, T_{C1}]$ (Fig. C.25)

Initial Conditions:
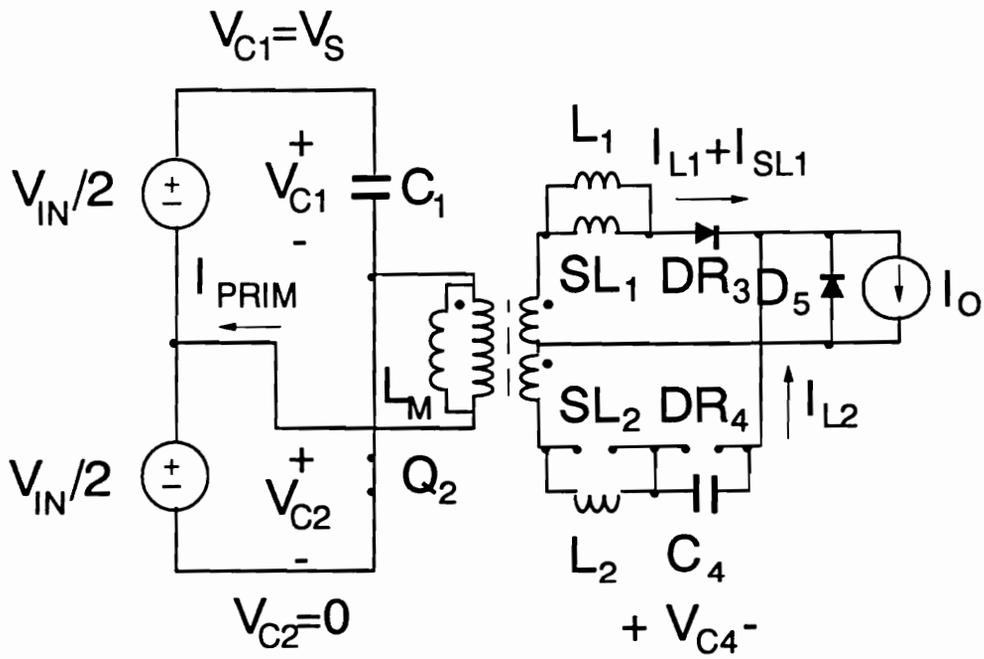
Figure C.25. Topological Stage C of ideal HB ZVS-MRC (L_M).

$$v_{C1}(T_{CO}) = V_{IN} \qquad (C.17.a)$$

$$v_{C2}(T_{CO}) = 0 \qquad (C.17.b)$$

$$i_{PRIM}(T_{CO}) = I_{PRIM}^{C} \qquad (C.17.c)$$

$$i_{LM}(T_{CO}) = I_{LM}^{C} \qquad (C.17.d)$$

$$v_{C3}(T_{CO}) = 0 \qquad (C.17.e)$$

$$v_{C4}(T_{CO}) = V_{C4}^{C} \qquad (C.17.f)$$

$$i_{L1}(T_{CO}) = I_{L1}^{C} \qquad (C.17.g)$$

$$i_{L2}(T_{CO}) = I_{L2}^{C} \qquad (C.17.h)$$

$$i_{SL1}(T_{CO}) = I_{SL1}^{C} \qquad (C.17.i)$$

$$i_{SL2}(T_{CO}) = 0 \qquad (C.17.j)$$

Equations:

$$v_{PRIM}(t) = -\frac{V_{IN}}{2} \qquad (C.18.a)$$

$$\frac{v_{PRIM}(t)}{N} = L\frac{di_{L1}(t)}{dt} \qquad (C.18.b)$$

$$\frac{V_{IN}}{2N} = v_{C4}(t) + L\frac{di_{L2}(t)}{dt} \qquad (C.18.c)$$

$$i_{L2}(t) = i_{C4}(t) = C_D\frac{dv_{C4}(t)}{dt} \qquad (C.18.d)$$

$$-\frac{V_{IN}}{2} = L_M\frac{di_{LM}(t)}{dt} \qquad (C.18.e)$$

From Eqs. (C.17.a) - (C.18.e), it follows that:

$$\frac{d^2 v_{C4}(t)}{dt^2} + v_{C4}(t)\omega_D^2 = \frac{V_{IN}\omega_D^2}{2N} \qquad (C.19.a)$$

where

$$\omega_D = \frac{1}{\sqrt{LC_D}} \qquad (C.19.b)$$

Solution:

$$v_{C4}^C = a_C \cos \omega_D t + b_C \sin \omega_D t + \frac{V_{IN}}{2N} \qquad (C.20.a)$$

$$i_{L2}^C = C_D\omega_D[b_C \cos \omega_D t - a_C \sin \omega_D t] \qquad (C.20.b)$$

$$i_{L1}^{C} = -\frac{V_{IN}}{2NL} t + I_{L1}^{C} \qquad (C.20.c)$$

$$i_{LM}^{C} = -\frac{V_{IN}}{2L_M} t + I_{LM}^{C} \qquad (C.20.d)$$

where

$$a_C = V_{C4}^{C} - \frac{V_{IN}}{2} \qquad (C.21.a)$$

$$b_C = \frac{I_{L2}^{C}}{\omega_D C_D} \qquad (C.21.b)$$

or in the normalized form:

$$v_{C4}^{CN} = a_{CN} \cos \xi t_N + b_{CN} \sin \xi t_N + 1 \qquad (C.22.a)$$

$$i_{L2}^{CN} = -\frac{1}{I_{ON}} \sqrt{\frac{C_N L_N}{16}} \left[a_{CN} \cos \xi t_N - b_{CN} \sin \xi t_N \right] \qquad (C.22.b)$$

$$i_{L1}^{CN} = -\frac{L_N \pi t_N}{2 I_{ON}} + I_{L1}^{CN} \qquad (C.22.c)$$

$$i_{LM}^{CN} = -\frac{2\pi t_N}{I_{ON}} + I_{LM}^{CN} \qquad (C.22.d)$$

where

$$a_{CN} = V_{C4}^{CN} - 1 \qquad (C.23.a)$$

$$b_{CN} = I_{L2}^{CN} I_{ON} \sqrt{\frac{16}{L_N C_N}} \qquad (C.23.b)$$

$$\xi = 2\pi \sqrt{\frac{L_N}{C_N}} \qquad (C.23.c)$$

Stage Duration $T_C = T_{C1} - T_{CO}$

Stage duration T_C is determined from the conditions:

$$i_{L1}(T_C) = 0 \qquad (C.24.a)$$

or

$$i_{L2}(T_C) = I_{SAT}. \qquad (C.24.b)$$

I_{SAT} is the current of the linear inductor at the time the saturable inductor saturates.

STAGE D $[T_{DO}, T_{D1}]$ (Fig. C.26)

Initial Conditions:
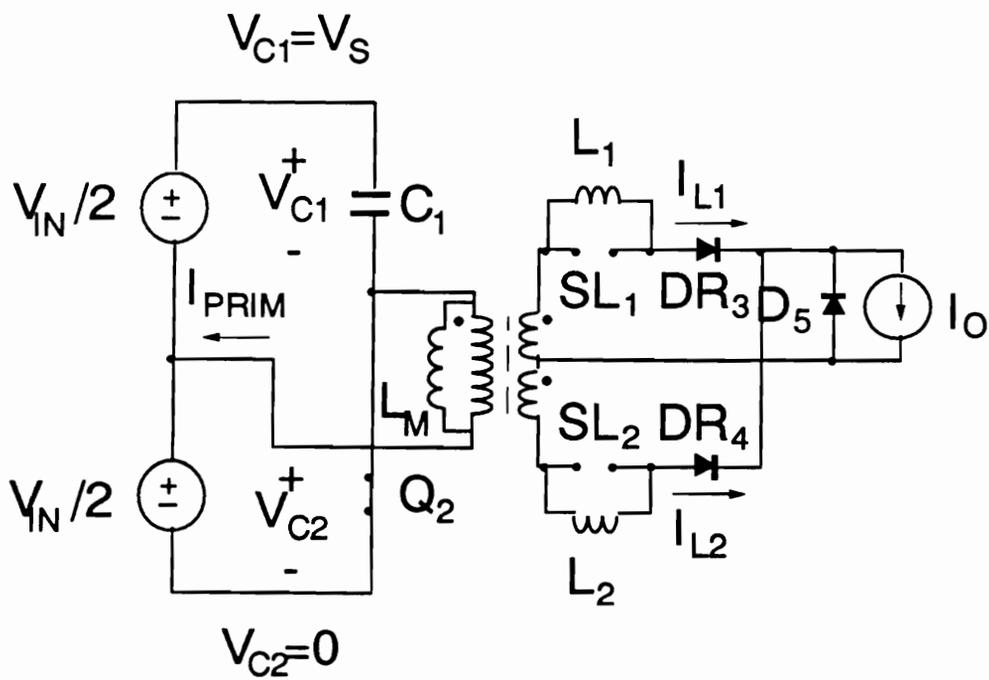
Figure C.26. Topological Stage D of ideal HB ZVS-MRC (L_M).

$$v_{C1}(T_{DO}) = V_{IN} \qquad\qquad (C.25.a)$$

$$v_{C2}(T_{DO}) = 0 \qquad\qquad (C.25.b)$$

$$i_{PRIM}(T_{DO}) = I_{PRIM}^D \qquad\qquad (C.25.c)$$

$$i_{LM}(T_{DO}) = I_{LM}^D \qquad\qquad (C.25.d)$$

$$v_{C3}(T_{DO}) = 0 \qquad\qquad (C.25.e)$$

$$v_{C4}(T_{DO}) = 0 \qquad\qquad (C.25.f)$$

$$i_{L1}(T_{DO}) = I_{L1}^D \qquad\qquad (C.25.g)$$

$$i_{L2}(T_{DO}) = I_{L2}^D \qquad\qquad (C.25.h)$$

$$i_{SL1}(T_{DO}) = 0 \qquad\qquad (C.25.i)$$

$$i_{SL2}(T_{DO}) = 0 \qquad\qquad (C.25.j)$$

Equations:

$$v_{PRIM}(t) = -\frac{V_{IN}}{2} \qquad\qquad (C.26.a)$$

$$\frac{V_{IN}}{2N} = -L\,\frac{di_{L1}(t)}{dt} \qquad\qquad (C.26.b)$$

$$\frac{V_{IN}}{2N} = L \frac{di_{L2}(t)}{dt} \qquad (C.26.c)$$

$$-\frac{V_{IN}}{2} = L_M \frac{di_{LM}(t)}{dt} \qquad (C.26.d)$$

Solution:

$$i_{L1}^D = -\frac{V_{IN}}{2NL} t + I_{L1}^D \qquad (C.27.a)$$

$$i_{L2}^D = \frac{V_{IN}}{2NL} t + I_{L2}^D \qquad (C.27.b)$$

$$i_{LM}^D = -\frac{V_{IN}}{2L_M} t + I_{LM}^D \qquad (C.27.c)$$

or in the normalized form:

$$i_{L1}^{DN} = -\frac{L_N \pi t_N}{2I_{ON}} + I_{L1}^{DN} \qquad (C.28.a)$$

$$i_{L2}^{DN} = \frac{L_N \pi t_N}{2I_{ON}} + I_{L2}^{DN} \qquad (C.28.b)$$

$$i_{LM}^{DN} = -\frac{2\pi t_N}{I_{ON}} + I_{LM}^{DN} \qquad (C.28.c)$$

Stage Duration $T_D = T_{D1} - T_{DO}$

Stage duration T_C is determined from the conditions:

$$i_{L1}(T_D) = 0; \quad T_D = \frac{I_{L1}^D 2NL}{V_{IN}} \qquad (C.29.a)$$

or

$$i_{L2}(T_D) = I_{SAT}; \quad T_D = \frac{(I_{SAT} - I_{L2}^D)2NL}{V_{IN}} . \qquad (C.29.b)$$

STAGE E $[T_{EO}, T_{E1}]$ (Fig. C.27)

Initial Conditions:

$$v_{C1}(T_{EO}) = V_{IN} \qquad (C.30.a)$$

$$v_{C2}(T_{EO}) = 0 \qquad (C.30.b)$$

$$i_{PRIM}(T_{EO}) = I_{PRIM}^E \qquad (C.30.c)$$

$$i_{LM}(T_{EO}) = I_{LM}^E \qquad (C.30.d)$$
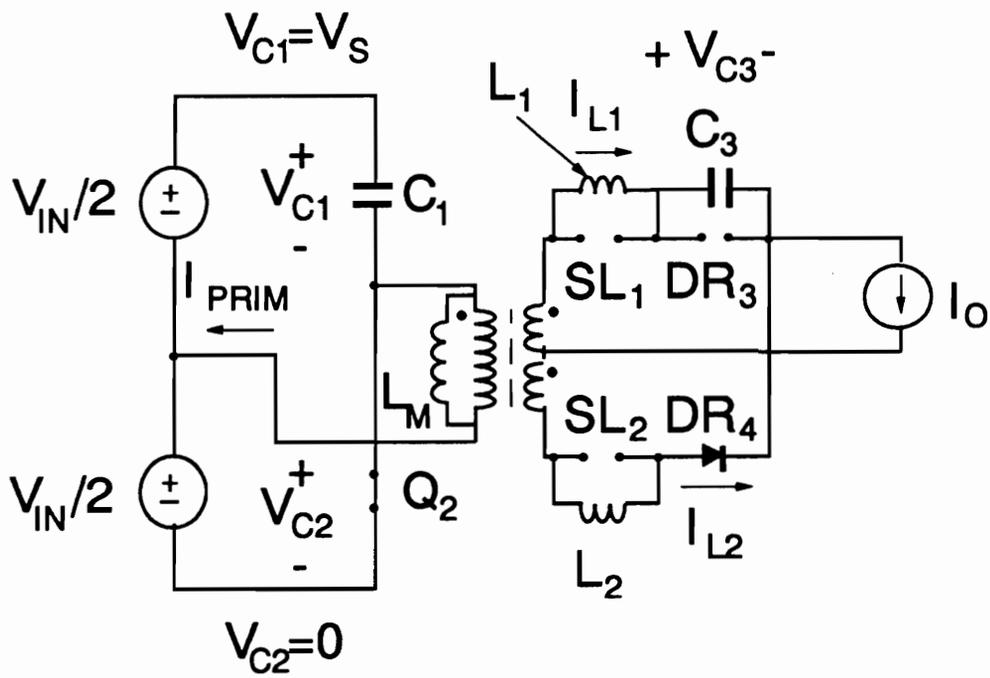
Figure C.27. Topological Stage E of ideal HB ZVS-MRC (L_M).

$$v_{C3}(T_{EO}) = V_{C3}^{E} \qquad (C.30.e)$$

$$v_{C4}(T_{EO}) = 0 \qquad (C.30.f)$$

$$i_{L1}(T_{EO}) = I_{L1}^{E} \qquad (C.30.g)$$

$$i_{L2}(T_{EO}) = I_{L2}^{E} \qquad (C.30.h)$$

$$i_{SL1}(T_{EO}) = 0 \qquad (C.30.i)$$

$$i_{SL2}(T_{EO}) = I_{SL2}^{E} \qquad (C.30.j)$$

Equations:

$$v_{PRIM}(t) = -\frac{V_{IN}}{2} \qquad (C.31.a)$$

$$\frac{v_{PRIM}(t)}{N} = -\frac{V_{IN}}{2N} = L\frac{di_{L}1(t)}{dt} + v_{C3}(t) \qquad (C.31.b)$$

$$\frac{V_{IN}}{2N} = v_{L2}(t) = L\frac{di_{L2}(t)}{dt} \qquad (C.31.c)$$

$$i_{L1}(t) = i_{C3}(t) = C_{D}\frac{dv_{C3}(t)}{dt} \qquad (C.31.d)$$

$$-\frac{V_{IN}}{2} = L_{M}\frac{di_{LM}(t)}{dt} \qquad (C.31.e)$$

From Eqs. (C.30.a) - (C.31.e), it follows that:

$$\frac{d^2 v_{C3}(t)}{dt^2} + v_{C3}(t)\omega_D^2 = \frac{V_{IN}\omega_D^2}{2N}$$

(C.32)

Solution:

$$v_{C3}^E = a_E \cos \omega_D t + b_E \sin \omega_D t + \frac{V_{IN}}{2N}$$

(C.33.a)

$$i_{L1}^E = C_D \omega_D [b_E \cos \omega_D t - a_E \sin \omega_D t]$$

(C.33.b)

$$i_{L2}^E = \frac{V_{IN}}{2NL} t + I_{L2}^E$$

(C.33.c)

$$i_{LM}^E = -\frac{V_{IN}}{2L_M} t + I_{LM}^E$$

(C.33.d)

where

$$a_E = V_{C3}^E - \frac{V_{IN}}{2}$$

(C.33.a)

$$b_E = -\frac{I_{L1}^E}{\omega_D C_D}$$

(C.33.b)

or in the normalized form:

$$v_{C3}^{EN} = a_{EN} \cos \xi t_N + b_{EN} \sin \xi t_N + 1 \qquad (C.34.a)$$

$$i_{L1}^{EN} = -\frac{1}{I_{ON}} \sqrt{\frac{C_N L_N}{16}} \left[a_{EN} \cos \xi t_N - b_{EN} \sin \xi t_N \right] \qquad (C.34.b)$$

$$i_{L2}^{EN} = \frac{L_N \pi t_N}{2 I_{ON}} + I_{L2}^{EN} \qquad (C.34.c)$$

$$i_{LM}^{EN} = -\frac{2\pi t_N}{I_{ON}} + I_{LM}^{EN} \qquad (C.34.d)$$

where

$$a_{EN} = V_{C3}^{EN} - 1 \qquad (C.35.a)$$

$$b_{EN} = I_{L1}^{EN} I_{ON} \sqrt{\frac{16}{L_N C_N}} \qquad (C.35.b)$$

Stage Duration $T_E = T_{E1} - T_{EO}$

Stage duration T_E is determined from the conditions:

$$i_{L1}(T_E) + i_{L2}(T_E) = I_O \qquad (C.36.a)$$

or

$$i_{L2}(T_E) = I_{SAT}. \tag{C.36.b}$$

STAGE EP $[T_{EPO},\ T_{EP1}]$ (Fig. C.28)

Initial Conditions:

$$v_{C1}(T_{EPO}) = V_{IN} \tag{C.37.a}$$

$$v_{C2}(T_{EPO}) = 0 \tag{C.37.b}$$

$$i_{PRIM}(T_{EPO}) = I_{PRIM}^{EP} \tag{C.37.c}$$

$$i_{LM}(T_{EPO}) = I_{LM}^{EP} \tag{C.37.d}$$

$$v_{C3}(T_{EPO}) = V_{C3}^{EP} \tag{C.37.e}$$

$$v_{C4}(T_{EPO}) = 0 \tag{C.37.f}$$

$$i_{L1}(T_{EPO}) = I_{L1}^{EP} \tag{C.37.g}$$

$$i_{L2}(T_{EPO}) = I_{L2}^{EP} \tag{C.37.h}$$

$$i_{SL1}(T_{EPO}) = 0 \tag{C.37.i}$$

$$i_{SL2}(T_{EPO}) = I_{SL2}^{EP} \tag{C.37.j}$$
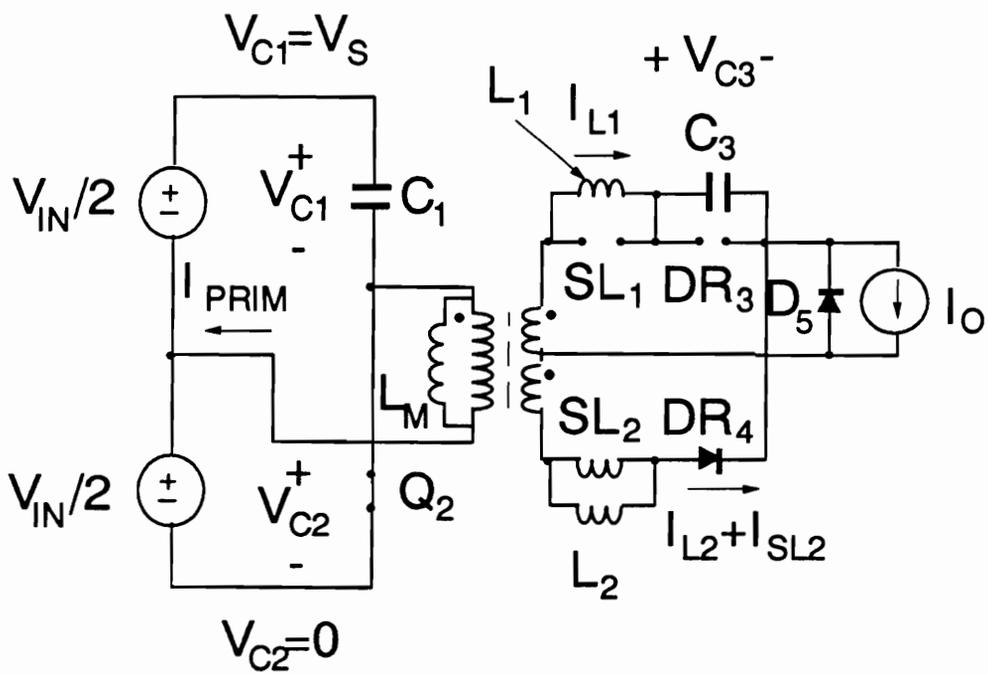
Figure C.28. Topological Stage EP of ideal HB ZVS-MRC (L_M).

Equations:

$$v_{PRIM}(t) = -\frac{V_{IN}}{2} \tag{C.38.a}$$

$$\frac{v_{PRIM}(t)}{N} = -\frac{V_{IN}}{2N} = L\frac{di_L1(t)}{dt} + v_{C3}(t) \tag{C.38.b}$$

$$\frac{V_{IN}}{2N} = v_{L2}(t) = v_{SL2}(t) = L\frac{di_{L2}(t)}{dt} = SL\frac{di_{SL2}(t)}{dt} \tag{C.38.c}$$

$$i_{L1}(t) = i_{C3}(t) = C_D\frac{dv_{C3}(t)}{dt} \tag{C.38.d}$$

$$-\frac{V_{IN}}{2} = L_M\frac{di_{LM}(t)}{dt} \tag{C.38.e}$$

From Eqs. (C.37.a) - (C.38.e), it follows that:

$$\frac{d^2v_{C3}(t)}{dt^2} + v_{C3}(t)\omega_D^2 = \frac{V_{IN}\omega_D^2}{2N} \tag{C.39}$$

Solution:

$$v_{C3}^{EP} = a_{EP}\cos\omega_D t + b_{EP}\sin\omega_D t + \frac{V_{IN}}{2N} \tag{C.40.a}$$

$$i_{L1}^{EP} = C_D \omega_D [b_{EP} \cos \omega_D t - a_{EP} \sin \omega_D t] \qquad (C.40.b)$$

$$i_{L2}^{EP} = \frac{V_{IN}}{2NL} t + I_{L2}^{EP} \qquad (C.40.c)$$

$$i_{SL2}^{EP} = \frac{V_{IN}}{2NSL} t + I_{SL2}^{EP} \qquad (C.40.d)$$

$$i_{LM}^{EP} = -\frac{V_{IN}}{2L_M} t + I_{LM}^{EP} \qquad (C.40.e)$$

where

$$a_{EP} = V_{C3}^{EP} - \frac{V_{IN}}{2} \qquad (C.41.a)$$

$$b_{EP} = \frac{I_{L1}^{EP}}{\omega_D C_D} \qquad (C.41.b)$$

or in the normalized form:

$$v_{C3}^{EPN} = a_{EPN} \cos \xi t_N + b_{EPN} \sin \xi t_N + 1 \qquad (C.42.a)$$

$$i_{L1}^{EPN} = -\frac{1}{I_{ON}} \sqrt{\frac{C_N L_N}{16}} [a_{EPN} \cos \xi t_N - b_{EPN} \sin \xi t_N] \qquad (C.42.b)$$

$$i_{L2}^{EPN} = \frac{L_N \pi t_N}{2 I_{ON}} + I_{L2}^{EPN} \qquad (C.42.c)$$

$$i_{SL2}^{EPN} = \frac{SL}{L} \frac{L_N \pi t_N}{2 I_{ON}} + I_{L2}^{EPN} \qquad (C.42.d)$$

$$i_{LM}^{EPN} = -\frac{2\pi t_N}{I_{ON}} + I_{LM}^{EPN} \qquad (C.42.e)$$

where

$$a_{EPN} = V_{C3}^{EPN} - 1 \qquad (C.43.a)$$

$$b_{EPN} = I_{L1}^{EPN} I_{ON} \sqrt{\frac{16}{L_N C_N}} \qquad (C.43.b)$$

Stage Duration $T_{EP} = T_{EP1} - T_{EPO}$

Stage duration T_E is determined from the condition:

$$i_{SL2}(T_{EP}) + i_{L2}(T_{EP}) + i_{L1}(T_{EP}) = I_O \qquad (C.44)$$

STAGE F [T_{FO}, T_{F1}] (Fig. C.29)

Initial Conditions:

$$v_{C1}(T_{FO}) = V_{IN} \qquad (C.45.a)$$
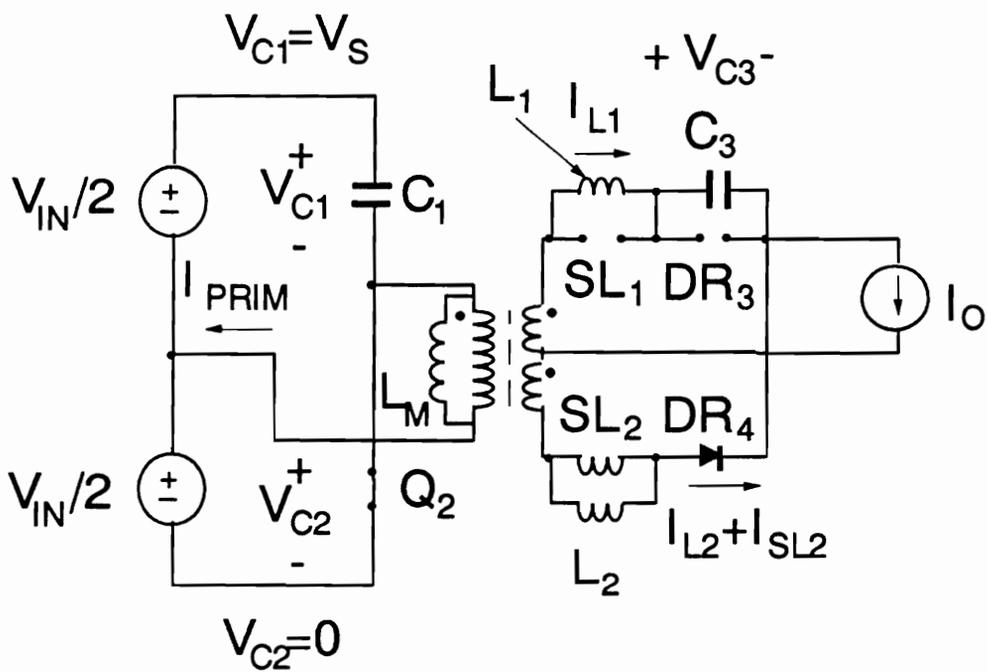
Figure C.29. Topological Stage F of ideal HB ZVS-MRC (L_M).

$$v_{C2}(T_{FO}) = 0 \qquad\qquad (C.45.b)$$

$$i_{PRIM}(T_{FO}) = I_{PRIM}^{F} \qquad\qquad (C.45.c)$$

$$i_{LM}(T_{FO}) = I_{LM}^{F} \qquad\qquad (C.45.d)$$

$$v_{C3}(T_{FO}) = V_{C3}^{F} \qquad\qquad (C.45.e)$$

$$v_{C4}(T_{FO}) = 0 \qquad\qquad (C.45.f)$$

$$i_{L1}(T_{FO}) = I_{L1}^{F} \qquad\qquad (C.45.g)$$

$$i_{L2}(T_{FO}) = I_{L2}^{F} \qquad\qquad (C.45.h)$$

$$i_{SL1}(T_{FO}) = 0 \qquad\qquad (C.45.i)$$

$$i_{SL2}(T_{FO}) = I_{SL2}^{F} \qquad\qquad (C.45.j)$$

Equations:

$$v_{PRIM}(t) = -\frac{V_{IN}}{2} \qquad\qquad (C.46.a)$$

$$\frac{2v_{PRIM}(t)}{N} = -\frac{V_{IN}}{N} = L\frac{di_{L}1(t)}{dt} + v_{C3}(t) - L\frac{di_{L2}(t)}{dt} \qquad\qquad (C.46.b)$$

$$\frac{V_{IN}}{2N} = v_{L2}(t) = v_{SL2}(t) = L\frac{di_{L2}(t)}{dt} = SL\frac{di_{SL2}(t)}{dt} \qquad\qquad (C.46.c)$$

$$i_{L1}(t) = i_{C3}(t) = C_D \frac{dv_{C3}(t)}{dt} \tag{C.46.d}$$

$$-\frac{V_{IN}}{2} = L_M \frac{di_{LM}(t)}{dt} \tag{C.46.e}$$

From Eqs. (C.45.a) - (C.46.e), it follows that:

$$\frac{d^2v_{C3}(t)}{dt^2} + v_{C3}(t)\omega_D^2 K_1 = \frac{V_{IN}\omega_D^2 K}{2N} \tag{C.47}$$

Solution:

$$v_{C3}^F = a_F \cos K_1^{1/2}\omega_D t + b_F \sin K_1^{1/2}\omega_D t + \frac{V_{IN}}{2N} \tag{C.48.a}$$

$$i_{L1}^F = C_D\omega_D K_1^{1/2}[b_F \cos K_1^{1/2}\omega_D t - a_F \sin K_1^{1/2}\omega_D t] \tag{C.48.b}$$

$$i_{L2}^F = \frac{1}{L\omega_D K_1^{1/2}(2 + \frac{L}{SL})} (a_F \sin \omega_D K_1^{1/2}t - b_F(\cos \omega_D K_1^{1/2}t - 1)) + c_F \tag{C.48.c}$$

$$i_{SL2}^F = I_O - i_{L1}^F - i_{L2}^F \tag{C.48.d}$$

$$i_{LM}^F = -\frac{V_{IN}}{2L_M}t + I_{LM}^F \tag{C.48.e}$$

where

$$a_F = V_{C3}^F - \frac{V_{IN}}{2} \qquad (C.49.a)$$

$$b_F = \frac{I_{L1}^F K_1^{-1/2}}{\omega_D C_D} \qquad (C.49.b)$$

$$c_F = I_{L2}^F \qquad (C.49.c)$$

or in the normalized form:

$$v_{C3}^{FN} = a_{FN} \cos \xi K_1^{1/2} t_N + b_{FN} \sin \xi K_1^{1/2} t_N + 1 \qquad (C.50.a)$$

$$i_{L1}^{FN} = -\frac{1}{I_{ON}} \sqrt{\frac{C_N L_N K_1}{16}} [a_{FN} \cos \xi K_1^{1/2} t_N - b_{FN} \sin K_1^{1/2} \xi t_N] \qquad (C.50.b)$$

$$i_{L2}^{FN} = \frac{1}{I_{ON}} \sqrt{\frac{C_N L_N}{16(2 + \dfrac{L}{SL})(1 + \dfrac{L}{SL})}} [a_{FN} \sin \xi K_1^{1/2} t_N$$

$$- b_{FN}(\cos \xi K_1^{1/2} t_N - 1)] + c_{FN} \qquad (C.50.c)$$

$$i_{SL2}^{FN} = 1 - i_{L1}^{FN} - i_{L2}^{FN} \qquad (C.50.d)$$

$$i_{LM}^{FN} = -\frac{2\pi t_N}{I_{ON}} + I_{LM}^{FN} \qquad (C.42.e)$$

where

$$a_{FN} = V_{C3}^{FN} - 1 \tag{C.51.a}$$

$$b_{FN} = I_{L1}^{FN} I_{ON} \sqrt{\frac{16}{L_N C_N K_1}} \tag{C.51.b}$$

$$c_{FN} = I_{L2}^{FN} \tag{C.51.c}$$

Stage Duration $T_F = T_{F1} - T_{FO}$

Stage duration T_F is determined by the turn-off of switch Q_2 initiating a new conversion cycle.

STAGE G $[T_{GO}, T_{G1}]$ (Fig. C.30)

Initial Conditions:

$$v_{C1}(T_{GO}) = V_{IN} \tag{C.52.a}$$

$$v_{C2}(T_{GO}) = 0 \tag{C.52.b}$$

$$i_{PRIM}(T_{GO}) = I_{PRIM}^{G} \tag{C.52.c}$$

$$i_{LM}(T_{GO}) = I_{LM}^{G} \tag{C.52.d}$$
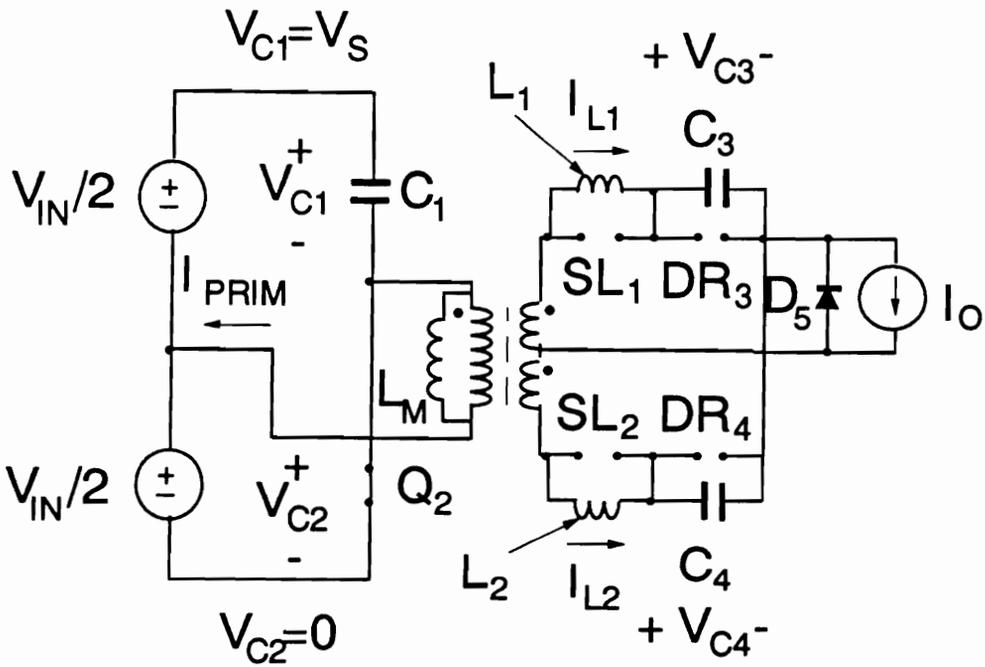
Figure C.30.   Topological Stage G of ideal HB ZVS-MRC (L_M).

$$v_{C3}(T_{GO}) = V_{C3}^{G} \qquad\qquad (C.52.e)$$

$$v_{C4}(T_{GO}) = V_{C4}^{G} \qquad\qquad (C.52.f)$$

$$i_{L1}(T_{GO}) = I_{L1}^{G} \qquad\qquad (C.52.g)$$

$$i_{L2}(T_{GO}) = I_{L2}^{G} \qquad\qquad (C.52.h)$$

$$i_{SL1}(T_{GO}) = 0 \qquad\qquad (C.52.i)$$

$$i_{SL2}(T_{GO}) = 0 \qquad\qquad (C.52.j)$$

Equations:

$$v_{PRIM}(t) = -\frac{V_{IN}}{2} \qquad\qquad (C.53.a)$$

$$\frac{v_{PRIM}(t)}{N} = -\frac{V_{IN}}{2N} = L\frac{di_{L1}(t)}{dt} + v_{C3}(t) \qquad\qquad (C.53.b)$$

$$\frac{V_{IN}}{2N} = L\frac{di_{L2}(t)}{dt} + v_{C4}(t) \qquad\qquad (C.53.c)$$

$$i_{L1}(t) = i_{C3}(t) = C_D\frac{dv_{C3}(t)}{dt} \qquad\qquad (C.53.d)$$

$$i_{L2}(t) = i_{C4}(t) = C_D\frac{dv_{C4}(t)}{dt} \qquad\qquad (C.53.e)$$

$$-\frac{V_{IN}}{2} = L_M \frac{di_{LM}(t)}{dt} \qquad (C.53.f)$$

From Eqs. (C.52.a) - (C.53.f), it follows that:

$$\frac{d^2 v_{C3}(t)}{dt^2} + v_{C3}(t)\omega_D^2 = \frac{V_{IN}\omega_D^2}{2N} \qquad (C.54.a)$$

$$\frac{d^2 v_{C4}(t)}{dt^2} + v_{C4}(t)\omega_D^2 = -\frac{V_{IN}\omega_D^2}{2N} \qquad (C.54.b)$$

Solution:

$$v_{C3}^G = a_G \cos \omega_D t + b_G \sin \omega_D t + \frac{V_{IN}}{2N} \qquad (C.55.a)$$

$$i_{L1}^G = C_D \omega_D [b_G \cos \omega_D t - a_G \sin \omega_D t] \qquad (C.55.b)$$

$$v_{C4}^G = c_G \cos \omega_D t + d_G \sin \omega_D t - \frac{V_{IN}}{2N} \qquad (C.55.c)$$

$$i_{L2}^G = C_D \omega_D [d_G \cos \omega_D t - c_G \sin \omega_D t] \qquad (C.55.d)$$

$$i_{LM}^G = -\frac{V_{IN}}{2L_M} t + I_{LM}^G \qquad (C.55.e)$$

where

$$a_G = V_{C3}^G - \frac{V_{IN}}{2} \qquad (C.56.a)$$

$$b_G = \frac{I_{L1}^G}{\omega_D C_D} \qquad (C.56.b)$$

$$c_G = V_{C4}^G + \frac{V_{IN}}{2} \qquad (C.56.c)$$

$$d_G = \frac{I_{L2}^G}{\omega_D C_D} \qquad (C.56.d)$$

or in the normalized form:

$$v_{C3}^{GN} = a_{GN} \cos \xi t_N + b_{GN} \sin \xi t_N + 1 \qquad (C.57.a)$$

$$i_{L1}^{GN} = -\frac{1}{I_{ON}} \sqrt{\frac{C_N L_N}{16}} \, [a_{GN} \cos \xi t_N - b_{GN} \sin \xi t_N] \qquad (C.57.b)$$

$$v_{C4}^{GN} = c_{GN} \cos \xi t_N + d_{GN} \sin \xi t_N - 1 \qquad (C.57.c)$$

$$i_{L2}^{GN} = -\frac{1}{I_{ON}} \sqrt{\frac{C_N L_N}{16}} \, [c_{GN} \cos \xi t_N - d_{GN} \sin \xi t_N] \qquad (C.57.d)$$

$$i_{LM}^{GN} = -\frac{2\pi t_N}{I_{ON}} + I_{LM}^{GN} \qquad (C.57.e)$$

where

$$a_{GN} = V_{C3}^{GN} - 1 \qquad\qquad (C.58.a)$$

$$b_{GN} = I_{L1}^{GN} I_{ON} \sqrt{\frac{16}{L_N C_N}} \qquad\qquad (C.58.b)$$

$$c_{GN} = V_{C4}^{GN} + 1 \qquad\qquad (C.58.c)$$

$$d_{GN} = I_{L2}^{GN} I_{ON} \sqrt{\frac{16}{L_N C_N}} \qquad\qquad (C.58.d)$$

Stage Duration $T_G = T_{G1} - T_{GO}$

Stage duration T_G is determined from the conditions:

$$i_{L1}(T_G) + i_{L2}(T_G) = I_O \qquad\qquad (C.59.a)$$

$$i_{L2}(T_G) = I_{SAT}, \qquad\qquad (C.59.b)$$

or

$$v_{C4}(T_G) = 0. \qquad\qquad (C.59.c)$$

STAGE H [T_{HO}, T_{H1}] (Fig. C.31)
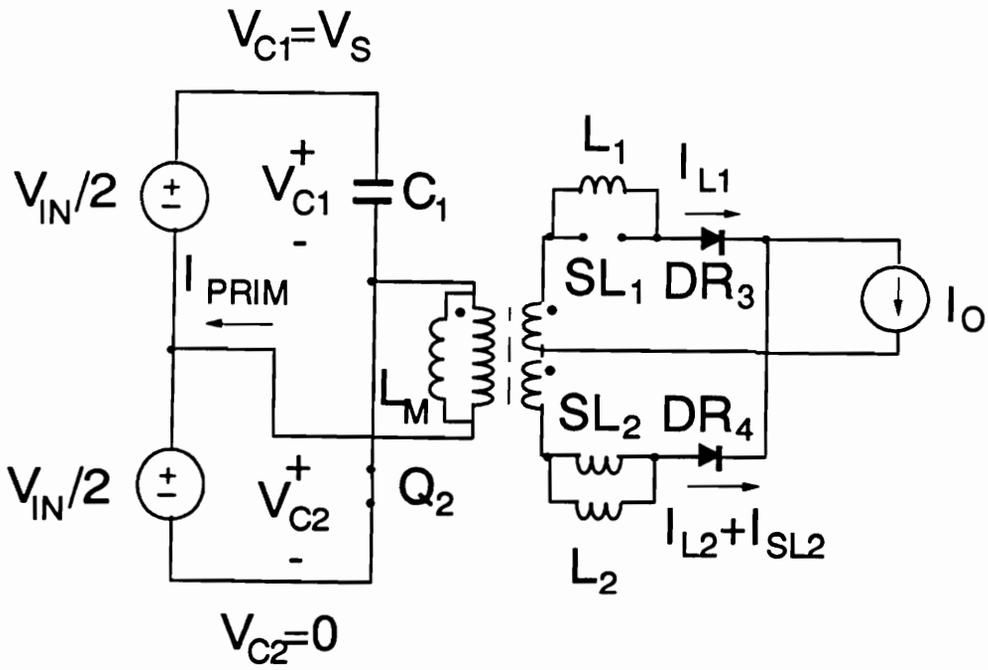
Figure C.31. Topological Stage H of ideal HB ZVS-MRC (L_M).

Initial Conditions:

$$v_{C1}(T_{HO}) = V_{IN} \qquad (C.60.a)$$

$$v_{C2}(T_{HO}) = 0 \qquad (C.60.b)$$

$$i_{PRIM}(T_{HO}) = I_{PRIM}^{H} \qquad (C.60.c)$$

$$i_{LM}(T_{HO}) = I_{LM}^{H} \qquad (C.60.d)$$

$$v_{C3}(T_{HO}) = 0 \qquad (C.60.e)$$

$$v_{C4}(T_{HO}) = 0 \qquad (C.60.f)$$

$$i_{L1}(T_{HO}) = I_{L1}^{H} \qquad (C.60.g)$$

$$i_{L2}(T_{HO}) = I_{L2}^{H} \qquad (C.60.h)$$

$$i_{SL1}(T_{HO}) = 0 \qquad (C.60.i)$$

$$i_{SL2}(T_{HO}) = I_{SL2}^{H} \qquad (C.60.j)$$

Equations:

$$v_{PRIM}(t) = -\frac{V_{IN}}{2} \qquad (C.61.a)$$

$$\frac{2v_{PRIM}(t)}{N} = -\frac{V_{IN}}{N} = L\frac{di_{L1}(t)}{dt} - L\frac{di_{L2}(t)}{dt} \qquad (C.61.b)$$

$$v_{L2}(t) = v_{SL2}(t) = L\frac{di_{L2}(t)}{dt} = SL\frac{di_{SL2}(t)}{dt} \qquad (C.61.c)$$

$$i_{L1}(t) + i_{L2}(t) + i_{SL2}(t) = I_O \qquad (C.61.d)$$

$$-\frac{V_{IN}}{2} = L_M\frac{di_{LM}(t)}{dt} \qquad (C.61.e)$$

Solution:

$$i_{L1}^H = -\frac{V_{IN}}{NL}\frac{(1 + \dfrac{L}{SL})}{(2 + \dfrac{L}{SL})}t + I_{L1}^H \qquad (C.62.a)$$

$$i_{L2}^H = \frac{V_{IN}}{NL}\frac{1}{(2 + \dfrac{L}{SL})}t + I_{L2}^H \qquad (C.62.b)$$

$$i_{SL2}^H = \frac{V_{IN}}{NSL}\frac{1}{(1 + \dfrac{L}{SL})}t + I_{SL2}^H \qquad (C.62.c)$$

$$i_{LM}^H = -\frac{V_{IN}}{2L_M}t + I_{LM}^H \qquad (C.62.d)$$

or in the normalized form:

$$i_{L1}^{HN} = -\frac{L_N \pi t_N}{I_{ON}} \frac{(1 + \frac{L}{SL})}{(2 + \frac{L}{SL})} + I_{L1}^{HN} \qquad (C.63.a)$$

$$i_{L2}^{HN} = \frac{L_N \pi t_N}{I_{ON}} \frac{1}{(1 + \frac{L}{SL})} + I_{L2}^{DN} \qquad (C.63.b)$$

$$i_{SL2}^{HN} = \frac{SL}{L(1 + \frac{L}{SL})} \frac{L_N \pi t_N}{I_{ON}} + I_{L2}^{HN} \qquad (C.63.c)$$

$$i_{LM}^{HN} = -\frac{2\pi t_N}{I_{ON}} + I_{LM}^{HN} \qquad (C.63.d)$$

Stage Duration $T_H = T_{H1} - T_{HO}$

Stage duration T_H is determined from the condition:

$$i_{L1}(T_H) = 0; \quad T_H = \frac{I_{L1}^{H} NL}{V_{IN}} . \qquad (C.64)$$

STAGE HP $[T_{HPO}, T_{HP1}]$ (Fig. C.32)

Initial Conditions:
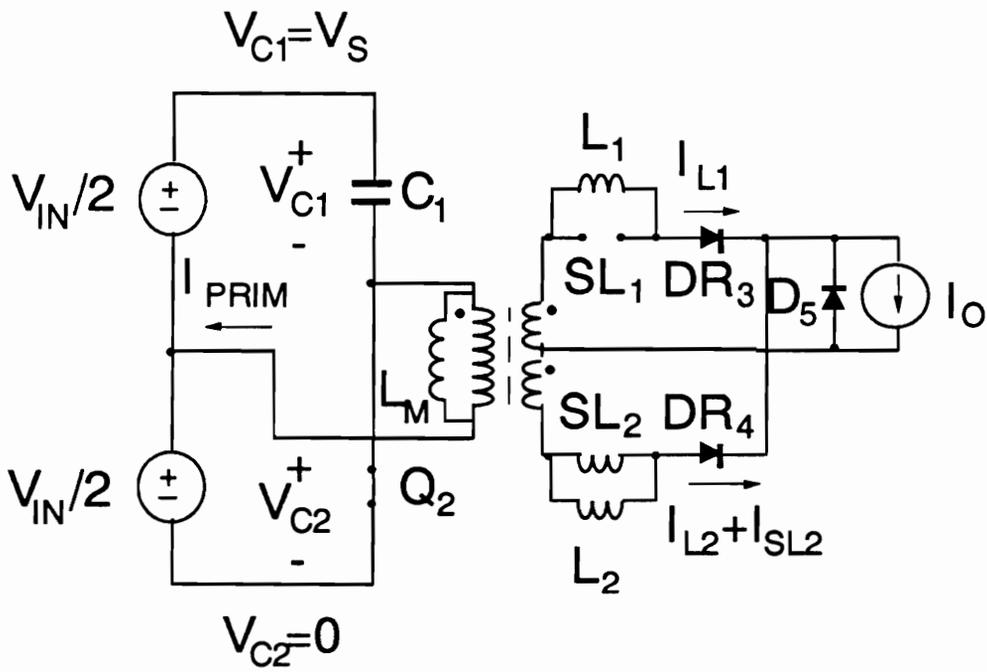
Figure C.32.   Topological Stage HP of ideal HB ZVS-MRC (L_M).

$$v_{C1}(T_{HPO}) = V_{IN} \qquad\qquad (C.65.a)$$

$$v_{C2}(T_{HPO}) = 0 \qquad\qquad (C.65.b)$$

$$i_{PRIM}(T_{HPO}) = I_{PRIM}^{HP} \qquad\qquad (C.65.c)$$

$$i_{LM}(T_{HPO}) = I_{LM}^{HP} \qquad\qquad (C.65.d)$$

$$v_{C3}(T_{HPO}) = 0 \qquad\qquad (C.65.e)$$

$$v_{C4}(T_{HPO}) = 0 \qquad\qquad (C.65.f)$$

$$i_{L1}(T_{HPO}) = I_{L1}^{HP} \qquad\qquad (C.65.g)$$

$$i_{L2}(T_{HPO}) = I_{L2}^{HP} \qquad\qquad (C.65.h)$$

$$i_{SL1}(T_{HPO}) = 0 \qquad\qquad (C.65.i)$$

$$i_{SL2}(T_{HPO}) = I_{SL2}^{HP} \qquad\qquad (C.65.j)$$

Equations:

$$v_{PRIM}(t) = -\frac{V_{IN}}{2} \qquad\qquad (C.66.a)$$

$$\frac{v_{PRIM}(t)}{N} = -\frac{V_{IN}}{2N} = L\frac{di_{L1}(t)}{dt} \qquad\qquad (C.66.b)$$

$$\frac{v_{PRIM}(t)}{N} = \frac{V_{IN}}{2N} = L\,\frac{di_{L2}(t)}{dt} \tag{C.66.c}$$

$$v_{L2}(t) = v_{SL2}(t) = L\,\frac{di_{L2}(t)}{dt} = SL\,\frac{di_{SL2}(t)}{dt} \tag{C.66.d}$$

$$-\frac{V_{IN}}{2} = L_M\,\frac{di_{LM}(t)}{dt} \tag{C.66.e}$$

Solution:

$$i_{L1}^{HP} = -\frac{V_{IN}}{2NL}\,t + I_{L1}^{HP} \tag{C.67.a}$$

$$i_{L2}^{HP} = \frac{V_{IN}}{2NL}\,t + I_{L2}^{HP} \tag{C.67.b}$$

$$i_{SL2}^{HP} = \frac{V_{IN}}{2NSL}\,t + I_{SL2}^{HP} \tag{C.67.c}$$

$$i_{LM}^{HP} = -\frac{V_{IN}}{2L_M}\,t + I_{LM}^{HP} \tag{C.67.d}$$

or in the normalized form:

$$i_{L1}^{HPN} = -\frac{L_N \pi t_N}{2I_{ON}} + I_{L1}^{HPN} \tag{C.68.a}$$

$$i_{L2}^{HPN} = \frac{L_N \pi t_N}{2I_{ON}} + I_{L2}^{HPN} \qquad (C.68.b)$$

$$i_{SL2}^{HPN} = \frac{SL}{L} \frac{L_N \pi t_N}{2I_{ON}} + I_{SL2}^{HPN} \qquad (C.68.c)$$

$$i_{LM}^{HPN} = -\frac{2\pi t_N}{I_{ON}} + I_{LM}^{HPN} \qquad (C.68.d)$$

Stage Duration $T_{HP} = T_{HP1} - T_{HPO}$

Stage duration T_{HP} is determined from the conditions:

$$i_{L1}(T_{HP}) = 0; \quad T_D = \frac{I_{L1}^{HP} 2NL}{V_{IN}} \qquad (C.69.a)$$

or

$$i_{L2}(T_{HP}) + i_{L1}(T_{HP}) + i_{SL2}(T_{HP}) = I_O. \qquad (C.69.b)$$

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# STAGE I [T_{IO}, T_{I1}] (Fig. C.33)

Initial Conditions:
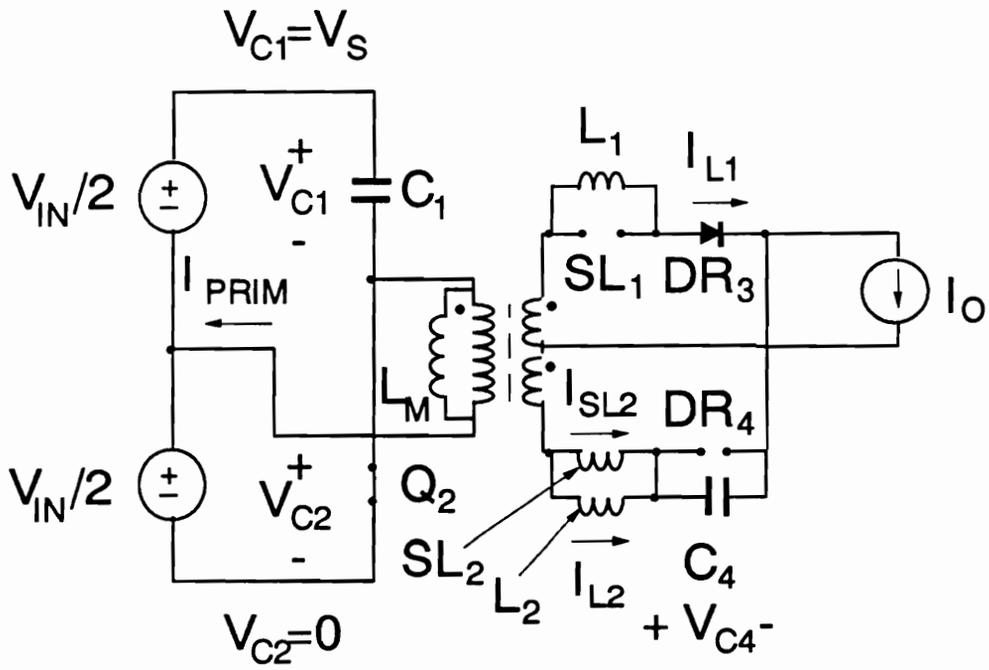
Figure C.33. Topological Stage I of ideal HB ZVS-MRC (L_M).

$$v_{C1}(T_{IO}) = V_{IN} \qquad (C.70.a)$$

$$v_{C2}(T_{IO}) = 0 \qquad (C.70.b)$$

$$i_{PRIM}(T_{IO}) = I^{I}_{PRIM} \qquad (C.70.c)$$

$$i_{LM}(T_{IO}) = I^{I}_{LM} \qquad (C.70.d)$$

$$v_{C3}(T_{IO}) = 0 \qquad (C.70.e)$$

$$v_{C4}(T_{IO}) = V^{I}_{C4} \qquad (C.70.f)$$

$$i_{L1}(T_{IO}) = I^{I}_{L1} \qquad (C.70.g)$$

$$i_{L2}(T_{IO}) = I^{I}_{L2} \qquad (C.70.h)$$

$$i_{SL1}(T_{IO}) = 0 \qquad (C.70.i)$$

$$i_{SL2}(T_{IO}) = I^{I}_{SL2} \qquad (C.70.j)$$

Equations:

$$v_{PRIM}(t) = -\frac{V_{IN}}{2} \qquad (C.71.a)$$

$$\frac{V_{IN}}{N} = L\frac{di_{L1}(t)}{dt} - v_{C4}(t) - L\frac{di_{L2}(t)}{dt} \qquad (C.71.b)$$

$$i_{L1}(t) + i_{L2}(t) + i_{SL2}(t) = I_O \qquad (C.71.c)$$

$$i_{L2}(t) + i_{SL2}(t) = i_{C4}(t) = C_D \frac{dv_{C4}(t)}{dt} \qquad (C.71.d)$$

$$-\frac{V_{IN}}{2} = L_M \frac{di_{LM}(t)}{dt} \qquad (C.71.e)$$

From Eqs. (C.70.a) - (C.71.e), it follows that:

$$\frac{d^2 v_{C4}(t)}{dt^2} + v_{C4}(t) K_1 \omega_D^2 = \frac{V_{IN} K_1 \omega_D^2}{N} \qquad (C.72)$$

Solution:

$$v_{C4}^I = a_I \cos \omega_D K_1^{1/2} t + b_I \sin \omega_D K_1^{1/2} t + \frac{V_{IN}}{N} \qquad (C.73.a)$$

$$i_{SL2}^I = \frac{L}{SL} \frac{C_D \omega_D K_1^{1/2}}{1 + \frac{L}{SL}} [b_I \cos \omega_D K_1^{1/2} t - a_I \sin \omega_D K_1^{1/2} t] + c_I \qquad (C.73.b)$$

$$i_{L2}^I = C_D \omega_D K_1^{1/2} [b_I \cos \omega_D K_1^{1/2} t - a_I \sin \omega_D K_1^{1/2} t] - I_{SL2}^I \qquad (C.73.c)$$

$$i_{LM}^I = -\frac{V_{IN}}{2L_M} t + I_{LM}^I \qquad (C.73.d)$$

where

$$a_I = v_{C4}^I - \frac{V_{IN}}{N} \tag{C.74.a}$$

$$b_I = \frac{I_{L2}^I + I_{SL2}^I}{\omega_D C_D K_1^{1/2}} \tag{C.74.b}$$

$$c_I = I_{L2}^I - \frac{\dfrac{L}{SL}}{1 + \dfrac{L}{SL}} (I_{L2}^I + I_{SL2}^I) \tag{C.74.c}$$

or in the normalized form:

$$v_{C4}^{IN} = a_{IN} \cos \xi K_1^{1/2} t_N + b_{IN} \sin \xi K_1^{1/2} t_N + 2 \tag{C.75.a}$$

$$i_{SL2}^{IN} = \frac{\dfrac{L}{SL}}{(1 + \dfrac{L}{SL})I_{ON}} \sqrt{\frac{L_N C_N}{16} K_1} \, [b_{IN} \cos K_1^{1/2} \xi t_N - a_{IN} \sin K_1^{1/2} \xi t_N] + c_{IN} \tag{C.75.b}$$

$$i_{L2}^{IN} = \frac{1}{I_{ON}} \sqrt{\frac{L_N C_N}{16} K_1} \, [b_{IN} \cos K_1^{1/2} \xi t_N - a_{IN} \sin K_1^{1/2} \xi t_N] - i_{SL2}^{IN} \tag{C.75.c}$$

$$i_{LM}^{IN} = -\frac{2\pi t_N}{I_{ON}} + I_{LM}^{IN} \tag{C.75.d}$$

where

$$a_{IN} = V_{C4}^{IN} - 2 \tag{C.76.a}$$

$$b_{IN} = (I_{L2}^{IN} + I_{SL2}^{IN})I_{ON}\sqrt{\frac{16}{L_N C_N K_1}} \qquad (C.76.b)$$

$$c_{IN} = I_{SL2}^{IN} - \frac{\dfrac{L}{SL}}{1 + \dfrac{L}{SL}}(I_{L2}^{IN} + I_{SL2}^{IN}) \qquad (C.76.c)$$

Stage Duration $T_I = T_{I1} - T_{IO}$

Stage duration T_I is determined from the conditions:

$$i_{L1}(T_I) = 0 \qquad (C.77.a)$$

or

$$v_{C4}(T_I) = 0. \qquad (C.77.b)$$

STAGE IP $[T_{IPO}, T_{IP1}]$ (Fig. C.34)

Initial Conditions:

$$v_{C1}(T_{IPO}) = V_{IN} \qquad (C.78.a)$$
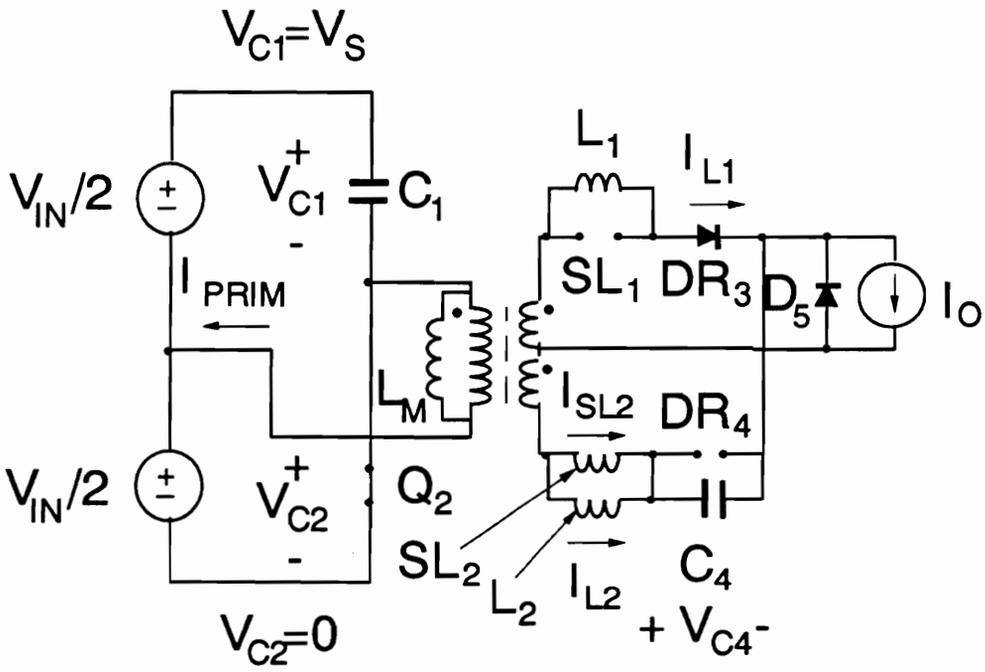
$$v_{C2}(T_{IPO}) = 0 \qquad (C.78.b)$$

Figure C.34. Topological Stage IP of ideal HB ZVS-MRC (L_M).

$$i_{PRIM}(T_{IPO}) = I_{PRIM}^{IP} \qquad (C.78.c)$$

$$i_{LM}(T_{IPO}) = I_{LM}^{IP} \qquad (C.78.d)$$

$$v_{C3}(T_{IPO}) = 0 \qquad (C.78.e)$$

$$v_{C4}(T_{IPO}) = V_{C4}^{IP} \qquad (C.78.f)$$

$$i_{L1}(T_{IPO}) = I_{L1}^{IP} \qquad (C.78.g)$$

$$i_{L2}(T_{IPO}) = I_{L2}^{IP} \qquad (C.78.h)$$

$$i_{SL1}(T_{IPO}) = 0 \qquad (C.78.i)$$

$$i_{SL2}(T_{IPO}) = I_{SL2}^{IP} \qquad (C.78.j)$$

Equations:

$$v_{PRIM}(t) = -\frac{V_{IN}}{2} \qquad (C.79.a)$$

$$\frac{V_{IN}}{2N} = L\frac{di_{L2}(t)}{dt} + v_{C4}(t) \qquad (C.79.b)$$

$$\frac{V_{IN}}{2N} = -L\frac{di_{L1}(t)}{dt} \qquad (C.79.c)$$

$$i_{L2}(t) + i_{SL2}(t) = i_{C4}(t) = C_D\frac{dv_{C4}(t)}{dt} \qquad (C.79.d)$$

$$-\frac{V_{IN}}{2} = L_M \frac{di_{LM}(t)}{dt} \qquad (C.79.e)$$

From Eqs. (C.78.a) - (C.79.e), it follows that:

$$\frac{d^2v_{C4}(t)}{dt^2} + v_{C4}(t)K_4^2\omega_D^2 = \frac{V_{IN}K_4^2\omega_D^2}{2N} \qquad (C.80.a)$$

$$K_4 = \sqrt{1 + \frac{L}{SL}} \qquad (C.80.b)$$

Solution:

$$v_{C4}^{IP} = a_{IP}\cos\omega_D K_4 t + b_{IP}\sin\omega_D K_4 t + \frac{V_{IN}}{2N} \qquad (C.81.a)$$

$$i_{SL2}^{IP} = \frac{L}{SL}C_D\omega_D K_4^{-1}[b_{IP}\cos\omega_D K_4 t - a_{IP}\sin\omega_D K_4 t] + c_{IP} \qquad (C.81.b)$$

$$i_{L2}^{IP} = C_D\omega_D K_4[b_{IP}\cos\omega_D K_4 t - a_{IP}\sin\omega_D K_4 t] - i_{SL2}^{IP} \qquad (C.81.c)$$

$$i_{LM}^{IP} = -\frac{V_{IN}}{2L_M}t + I_{LM}^{IP} \qquad (C.81.d)$$

where

$$a_{IP} = V_{C4}^{IP} - \frac{V_{IN}}{2N} \qquad (C.82.a)$$

$$b_{IP} = \frac{I_{L2}^{IP} + I_{SL2}^{IP}}{\omega_D C_D K_4} \qquad (C.82.b)$$

$$c_{IP} = I_{L2}^{IP} - \frac{\dfrac{L}{SL}}{1 + \dfrac{L}{SL}} (I_{L2}^{IP} + I_{SL2}^{IP}) \qquad (C.82.c)$$

or in the normalized form:

$$v_{C4}^{IPN} = a_{IPN} \cos \xi K_4 t_N + b_{IPN} \sin \xi K_4 t_N + 1 \qquad (C.83.a)$$

$$i_{SL2}^{IPN} = \frac{\dfrac{L}{SL}}{I_{ON}(1 + \dfrac{L}{SL})} \sqrt{\frac{L_N C_N}{16(1 + \dfrac{L}{SL})}} [b_{IPN} \cos K_4 \xi t_N - a_{IPN} \sin K_4 \xi t_N] + c_{IPN} \quad (C.83.b)$$

$$i_{L2}^{IPN} = \frac{1}{I_{ON}} \sqrt{\frac{L_N C_N}{16(1 + \dfrac{L}{SL})}} [b_{IPN} \cos K_4 \xi t_N - a_{IPN} \sin K_4 \xi t_N] - i_{SL2}^{IPN} \qquad (C.83.c)$$

$$i_{LM}^{IPN} = - \frac{2\pi t_N}{I_{ON}} + I_{LM}^{IPN} \qquad (C.83.d)$$

where

$$a_{IPN} = V_{C4}^{IPN} - 1 \qquad (C.84.a)$$

$$b_{IPN} = \frac{(I_{L2}^{IPN} + I_{SL2}^{IPN}) I_{ON}}{K_4} \sqrt{\frac{16}{L_N C_N}} \qquad (C.84.b)$$

$$c_{IPN} = I_{SL2}^{IPN} - \frac{\dfrac{L}{SL}}{1 + \dfrac{L}{SL}}(I_{L2}^{IPN} + I_{SL2}^{IPN}) \qquad (C.84.c)$$

Stage Duration $T_{IP} = T_{IP1} - T_{IPO}$

Stage duration T_{IP} is determined from the conditions:

$$i_{L1}(T_{IP}) = 0 \qquad (C.85.a)$$

$$v_{C4}(T_{IP}) = 0 \qquad (C.85.b)$$

or

$$i_{L1}(T_{IP}) + i_{L2}(T_{IP}) + I_{SL2}(T_{IP}) = I_O \qquad (C.85.c)$$

STAGE J $[T_{JO}, T_{J1}]$ (Fig. C.35)

Initial Conditions:

$$v_{C1}(T_{JO}) = V_{IN} \qquad (C.86.a)$$

$$v_{C2}(T_{JO}) = 0 \qquad (C.86.b)$$
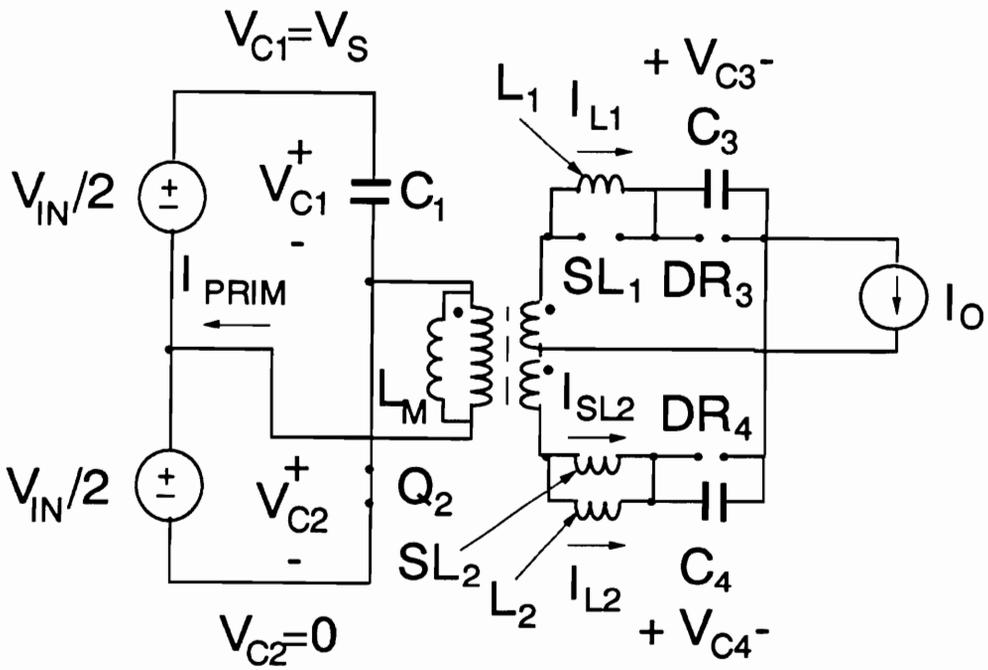
Figure C.35. Topological Stage J of ideal HB ZVS-MRC (L_M).

$$i_{PRIM}(T_{JO}) = I^J_{PRIM} \qquad (C.86.c)$$

$$i_{LM}(T_{JO}) = I^J_{LM} \qquad (C.86.d)$$

$$v_{C3}(T_{JO}) = V^J_{C3} \qquad (C.86.e)$$

$$v_{C4}(T_{JO}) = V^J_{C4} \qquad (C.86.f)$$

$$i_{L1}(T_{JO}) = I^J_{L1} \qquad (C.86.g)$$

$$i_{L2}(T_{JO}) = I^J_{L2} \qquad (C.86.h)$$

$$i_{SL1}(T_{JO}) = 0 \qquad (C.86.i)$$

$$i_{SL2}(T_{JO}) = I^J_{SL2} \qquad (C.86.j)$$

Equations:

$$v_{PRIM}(t) = -\frac{V_{IN}}{2} \qquad (C.87.a)$$

$$\frac{2v_{PRIM}(t)}{N} = -\frac{V_{IN}}{N} = L\frac{di_{L1}(t)}{dt} + v_{C3}(t) - v_{C4}(t) - L\frac{di_{L2}(t)}{dt} \qquad (C.87.b)$$

$$i_{L1}(t) + i_{L2}(t)i_{SL2}(t) = I_O \qquad (C.87.c)$$

$$i_{L2}(t) + i_{SL2}(t) = i_{C4}(t) = C_D\frac{dv_{C4}(t)}{dt} \qquad (C.87.d)$$

$$i_{L1}(t) = i_{C3}(t) = C_D \frac{dv_{C3}(t)}{dt} \tag{C.87.e}$$

$$-\frac{V_{IN}}{2} = L_M \frac{di_{LM}(t)}{dt} \tag{C.87.f}$$

From Eqs. (C.86.a) - (C.87.f), it follows that:

$$\frac{d^4 v_{C4}(t)}{dt^4} + v_{C4}(t) \frac{2(1 + \frac{L}{SL})}{LC_D(2 + \frac{L}{SL})} = 0 \tag{C.88.a}$$

$$\omega_J = \sqrt{\frac{2(1 + \frac{L}{SL})}{LC_D(2 + \frac{L}{SL})}} \tag{C.88.b}$$

Solution:

$$v_{C4}^J = a_J \cos \omega_J t + b_J \sin \omega_J t + c_J t + d_j \tag{C.89.a}$$

$$i_{L2}^J = \frac{C_D}{(1 + \frac{L}{SL})} [b_J \omega_J(\cos \omega_J t - 1) - a_J \omega_j \sin \omega_J t] + I_{L2}^J \tag{C.89.b}$$

$$v_{C3}^J = -a_J \cos \omega_J t - b_J \cos \omega_J t + c_J t + d_J - \frac{V_{IN}}{N} \tag{C.89.c}$$

$$i_{L1}^J = C_D[a_J \omega_J \sin \omega_J t - b_J \omega_J \cos \omega_J t + c_J] \tag{C.89.d}$$

$$i_{SL2}^J = I_O - i_{L2}^J - i_{L1}^J \qquad (C.89.e)$$

$$i_{LM}^J = -\frac{V_{IN}}{2L_M}t + I_{LM}^J \qquad (C.89.f)$$

where

$$d_J = \frac{V_{C3}^J + V_{C4}^J + \dfrac{V_{IN}}{N}}{2} \qquad (C.90.a)$$

$$a_J = V_{C4}^J - d_J \qquad (C.90.b)$$

$$c_J = \frac{I_{L1}^J + I_{L2}^J + I_{SL2}^J}{2C_D} \qquad (C.90.c)$$

$$b_J = \frac{I_{L2}^J + I_{SL2}^J}{\omega_J C_D} - \frac{c_J}{\omega_J} \qquad (C.90.d)$$

or in the normalized form:

$$v_{C4}^{JN} = a_{JN}\cos\delta t_N + b_{JN}\sin\delta t_N + \frac{i_{L1}^J + i_{L2}^J + i_{SL2}^J}{C_N}\frac{8\pi t_N}{I_{ON}} + d_{JN} \qquad (C.91.a)$$

$$i_{L2}^{JN} = \frac{C_N K_5}{4 I_{ON}\left(1 + \dfrac{L}{SL}\right)}\left[b_{JN}(\cos\delta t_N - 1) - a_{JN}\sin\delta t_N\right] + I_{L2}^{JN} \qquad (C.91.b)$$

$$v_{C3}^{JN} = -a_{JN} \cos \delta t_N - b_{JN} \sin \delta t_N + \frac{i_{L1}^{J} + i_{L2}^{J} + i_{SL2}^{J}}{C_N} \frac{8\pi t_N}{i_{ON}} + d_{JN} - 2 \qquad (C.91.c)$$

$$i_{L1}^{JN} = \frac{K_5 C_N}{4 i_{ON}} [a_{JN} \sin \delta t_N - b_{JN} \cos \delta t_N] + \frac{i_{L1}^{JN} + i_{L2}^{JN} + i_{SL2}^{JN}}{2} \qquad (C.91.d)$$

$$i_{SL2}^{JN} = 1 - i_{L1}^{JN} - i_{L2}^{JN} - i_{SL2}^{JN} \qquad (C.91.e)$$

$$i_{LM}^{JN} = -\frac{2\pi t_N}{i_{ON}} + i_{LM}^{JN} \qquad (C.91.f)$$

where

$$d_{JN} = V_{C3}^{JN} + V_{C4}^{JN} + 1 \qquad (C.92.a)$$

$$a_{JN} = V_{C4}^{JN} - d_{JN} \qquad (C.92.b)$$

$$b_{JN} = \frac{2 i_{ON}}{C_N K_5} [i_{L2}^{JN} + i_{SL2}^{JN} - i_{L1}^{JN}] \qquad (C.92.c)$$

$$\delta = 2\pi K_5 \qquad (C.92.d)$$

$$K_4 = \sqrt{\frac{2 L_N (1 + \frac{L}{SL})}{C_N (2 + \frac{L}{SL})}} \qquad (C.92.e)$$

Stage Duration $T_J = T_{J1} - T_{JO}$

Stage duration T_J is determined from the condition:

$$v_{C4}(T_J) = 0 \qquad (C.93)$$

STAGE JP [T_{JPO}, T_{JP1}] (Fig. C.36)

Initial Conditions:

$$v_{C1}(T_{JPO}) = V_{IN} \qquad (C.94.a)$$

$$v_{C2}(T_{JPO}) = 0 \qquad (C.94.b)$$

$$i_{PRIM}(T_{JPO}) = I_{PRIM}^{JP} \qquad (C.94.c)$$

$$i_{LM}(T_{JPO}) = I_{LM}^{JP} \qquad (C.94.d)$$

$$v_{C3}(T_{JPO}) = V_{C3}^{JP} \qquad (C.94.e)$$

$$v_{C4}(T_{JPO}) = V_{C4}^{JP} \qquad (C.94.f)$$

$$i_{L1}(T_{JPO}) = I_{L1}^{JP} \qquad (C.94.g)$$

$$i_{L2}(T_{JPO}) = I_{L2}^{JP} \qquad (C.94.h)$$

$$i_{SL1}(T_{JPO}) = 0 \qquad (C.94.i)$$
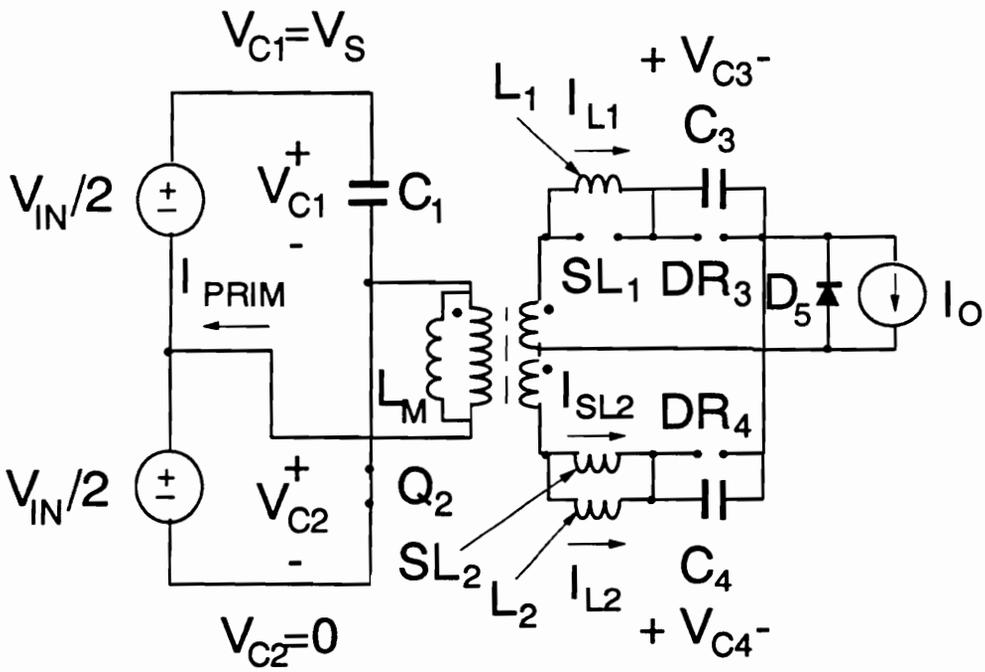
Figure C.36.   Topological Stage JP of ideal HB ZVS-MRC (L_M).

$$i_{SL2}(T_{JPO}) = I_{SL2}^{JP}$$ (C.94.j)

Equations:

$$v_{PRIM}(t) = -\frac{V_{IN}}{2}$$ (C.95.a)

$$\frac{v_{PRIM}(t)}{N} = -\frac{V_{IN}}{2N} = L\frac{di_{L1}(t)}{dt} + v_{C3}(t)$$ (C.95.b)

$$\frac{v_{PRIM}(t)}{N} = -\frac{V_{IN}}{2N} = -v_{C4}(t) - L\frac{di_{L2}(t)}{dt}$$ (C.95.c)

$$i_{L2}(t) + i_{SL2}(t) = i_{C4}(t) = C_D\frac{dv_{C4}(t)}{dt}$$ (C.95.d)

$$i_{L1}(t) = i_{C3}(t) = C_D\frac{dv_{C3}(t)}{dt}$$ (C.95.e)

$$-\frac{V_{IN}}{2} = L_M\frac{di_{LM}(t)}{dt}$$ (C.95.f)

From Eqs. (C.94.a) - (C.95.f), it follows that:

$$\frac{d^2v_{C4}(t)}{dt^2} + v_{C4}(t)\frac{1 + \dfrac{L}{SL}}{LC_D} = \frac{V_{IN}}{2}$$ (C.96.a)

$$\frac{d^2 v_{C3}(t)}{dt^2} + v_{C3}(t)\frac{1}{LC_D} = -\frac{V_{IN}}{2} \qquad (C.96.b)$$

$$\omega_{JPa} = \sqrt{\frac{1 + \dfrac{L}{SL}}{-\dfrac{}{LC_D}}} \qquad (C.96.c)$$

$$\omega_D = \frac{1}{\sqrt{LC_D}} \qquad (C.96.d)$$

Solution:

$$v_{C4}^{JP} = a_{JP}\cos\omega_{JP}t + b_{JP}\sin\omega_{JP}t + \frac{V_{IN}}{2} \qquad (C.97.a)$$

$$i_{L2}^{JP} = \frac{C_D}{(1 + \dfrac{L}{SL})}[b_{JP}\omega_{JP}(\cos\omega_{JP}t - 1) - a_{JP}\omega_{JP}\sin\omega_{JP}t] + i_{L2}^{JP} \qquad (C.97.b)$$

$$v_{C3}^{JP} = c_{JP}\cos\omega_D t - d_{JP}\cos\omega_D t + -\frac{V_{IN}}{2} \qquad (C.97.c)$$

$$i_{L1}^{JP} = C_D[c_J\omega_D\sin\omega_D t - d_J\omega_D\cos\omega_D t] \qquad (C.97.d)$$

$$i_{SL2}^{JP} = \frac{C_D\dfrac{L}{SL}}{(1 + \dfrac{L}{SL})}[b_{JP}\omega_{JP}(\cos\omega_{JP}t - 1) - a_{JP}\omega_{JP}\sin\omega_{JP}t] + i_{SL2}^{JP} \qquad (C.97.e)$$

$$i_{LM}^{JP} = -\frac{V_{IN}}{2L_M}t + i_{LM}^{JP} \qquad (C.97.f)$$

where

$$a_{JP} = V_{C4}^{JP} - 1 \qquad (C.98.a)$$

$$b_{JP} = \frac{I_{L2}^{JP} + I_{SL2}^{JP}}{C_{D^{(1)}JP}} \qquad (C.98.b)$$

$$c_J = V_{C3}^{JP} + 1 \qquad (C.98.c)$$

$$d_J = \frac{I_{L1}^{JP}}{C_{D^{(1)}D}} \qquad (C.98.d)$$

or in the normalized form:

$$v_{C4}^{JPN} = a_{JN} \cos vt_N + b_{JN} \sin vt_N + 1 \qquad (C.99a)$$

$$i_{L2}^{JN} = \frac{1}{I_{ON}} \sqrt{\frac{C_N L_N}{8(1 + \frac{L}{SL})}} [b_{JPN} \cos vt_N - a_{JPN} \sin vt_N] + i_{L2}^{JPN} - \frac{I_{L2}^{JPN} + I_{SL2}^{JPN}}{1 + \frac{L}{SL}} \qquad (C.99.b)$$

$$v_{C3}^{JPN} = -a_{JN} \cos vt_N - b_{JN} \sin vt_N - 1 \qquad (C.99.c)$$

$$i_{L1}^{JPN} = -\frac{1}{I_{ON}} \sqrt{\frac{C_N L_N}{16}} [c_{JPN} \cos vt_N - d_{JPN} \sin vt_N] \qquad (C.99.d)$$

$$i_{SL2}^{JPN} = \frac{1}{I_{ON}} \sqrt{\frac{C_N L_N (1 + \frac{L}{SL})}{8}} [b_{JPN} \cos vt_N - a_{JPN} \sin vt_N] - i_{L2}^{JPN} \qquad (C.99.e)$$

$$i_{LM}^{JPN} = -\frac{2\pi t_N}{I_{ON}} + i_{LM}^{JPN} \qquad (C.99.f)$$

where

$$a_{JPN} = V_{C4}^{JPN} - 1 \qquad (C.100.a)$$

$$b_{JN} = [I_{L2}^{JPN} + I_{SL2}^{JPN}] \sqrt{\frac{8}{C_N L_N (1 + \frac{L}{SL})}} \qquad (C.100.b)$$

$$c_{JN} = V_{C3}^{JPN} - 1 \qquad (C.100.c)$$

$$d_{JPN} = I_{L1}^{JPN} I_{ON} \sqrt{\frac{16}{C_N L_N}} \qquad (C.100.d)$$

$$v = 2\pi \sqrt{\frac{L_N(1 + \frac{L}{SL})}{C_N}} \qquad (C.100.e)$$

Stage Duration $T_{JP} = T_{JP1} - T_{JPO}$

Stage duration T_J is determined from the conditions:

$$v_{C4}(T_{JP}) = 0 \qquad (C.101)$$

or

$$i_{L2}(T_{JP}) + i_{SL2}(T_{JP}) + i_{L1}(T_{JP}) = I_O \qquad (101.b)$$

C.1.4 Light Load Operation

The following topological stages occur only for light load operation so that the load is comparable to the value of the current through the secondary linear inductors prior to the saturation of the saturable inductor. For very light loads, the saturable inductor will never saturate and all of the load current is supplied by the secondary linear inductors.

STAGE BP [T_{BPO}, T_{BP1}] (Fig. C.37)

Initial Conditions:

$$v_{C1}(T_{BPO}) = V_{C1}^{BP} \qquad (C.102.a)$$

$$v_{C2}(T_{BPO}) = V_{C2}^{BP} \qquad (C.102.b)$$

$$i_{PRIM}(T_{BPO}) = I_{PRIM}^{BP} \qquad (C.102.c)$$

$$i_{LM}(T_{BPO}) = I_{LM}^{BP} \qquad (C.102.d)$$

$$v_{C3}(T_{BPO}) = 0 \qquad (C.102.e)$$

$$v_{C4}(T_{BPO}) = V_{C4}^{BP} \qquad (C.102.f)$$

$$i_{L1}(T_{BPO}) = I_{L1}^{BP} \qquad (C.102.g)$$
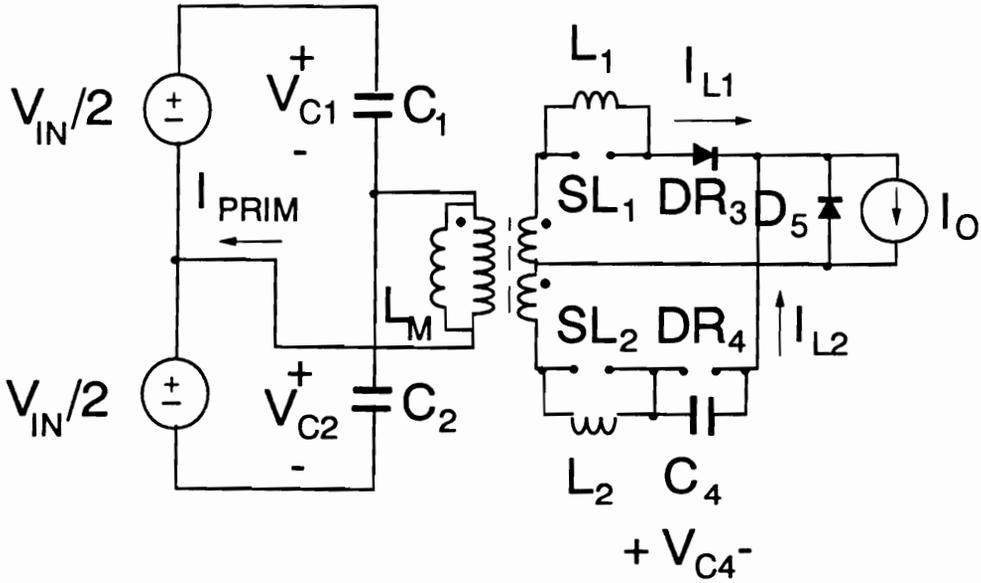
Figure C.37. Topological Stage BP of ideal HB ZVS-MRC (L_M).

$$i_{L2}(T_{BPO}) = I_{L2}^{BP} \tag{C.102.h}$$

$$i_{SL1}(T_{BPO}) = 0 \tag{C.102.i}$$

$$i_{SL2}(T_{BPO}) = 0 \tag{C.102.j}$$

Equations:

$$v_{C1}(t) + v_{C2}(t) = V_{IN} \tag{C.103.a}$$

$$C \frac{dv_{C1}(t)}{dt} = C \frac{dv_{C2}(t)}{dt} + i_{LM}(t) + i_{PRIM}(t) \tag{C.103.b}$$

$$i_{PRIM}(t) = \frac{1}{N} [i_{L1}(t) - i_{L2}(t)] \tag{C.103.c}$$

$$i_{L2}(t) = i_{C4}(t) = C_D \frac{dv_{C4}(t)}{dt} \tag{C.103.d}$$

$$\frac{V_{IN}}{2N} = v_{C4}(t) + L \frac{di_{L2}(t)}{dt} \tag{C.103.e}$$

$$\frac{V_{IN}(t)}{2} = v_{C1}(t) + L_M \frac{di_{LM}(t)}{dt} \tag{C.103.f}$$

$$\frac{v_{PRIM}(t)}{N} = L \frac{di_{L1}(t)}{dt} \tag{C.103.g}$$

From Eqs. (C.102.a) - (C.103.g), it follows that:

$$\frac{d^4 v_{C4}(t)}{dt^4} + \frac{d^2 v_{C4}(t)}{dt^2} \left[\frac{L_N}{C_N} + K_6 \right] \omega_O^2 + \frac{dv_{C4}(t)}{dt} \left[\frac{L_N}{C_N} K_5 - \frac{L_N^2}{4C_N} \right] \omega_O^4 = 0 \qquad (C.104.a)$$

where

$$K_6 = 1 + \frac{L_N}{2} \qquad (C.104.b)$$

$$a_1 = \left(\frac{L_N}{C_N} + K_6 \right) \omega_O^2 \qquad (C.104.c)$$

$$a_2 = \frac{L_N}{C_N} \left[K_6 - \frac{L_N}{4} \right] \omega_O^4 \qquad (C.104.d)$$

The roots of Eq. (C.96.a) are:

$$\mp j\gamma = \mp \sqrt{\frac{-a_1 - \sqrt{a_1^2 - 4a_2}}{2}} \qquad (C.104.e)$$

$$\mp j\beta = \mp \sqrt{\frac{-a_1 + \sqrt{a_1^2 - 4a_2}}{2}} \qquad (C.104.f)$$

Solution:

$$v_{C4}^{BP} = a_{BP} \cos \gamma t + b_{BP} \sin \gamma t + c_{BP} \cos \beta t + d_{BP} \sin \beta t \qquad (C.105.a)$$

$$i_{L2}^{BP} = C_D [b_{BP}\gamma \cos \gamma t - a_{BP}\gamma \sin \gamma t + d_{BP}\beta \cos \beta t - c_{BP}\beta \sin \beta t] \qquad (C.105.b)$$

$$i_{LM}^{BP} = \frac{N}{L_M} \left[\frac{b_{BP}}{\gamma} \cos \gamma t - \frac{a_{BP}}{\gamma} \sin \gamma t + \frac{d_{BP}}{\beta} \cos \beta t - \frac{c_{BP}}{\beta} \sin \beta t \right.$$

$$\left. + K_2[a_{BP}\gamma \sin \gamma t - b_{BP}\gamma \cos \gamma t + c_{BP}\beta \sin \beta t - d_{BP}\beta \cos \beta t]] + e_{BP} \right. \qquad (C.105.c)$$

$$v_{C1}^{BP} = \frac{V_{IN}}{2} + N[a_{BP} \cos \gamma t + b_{BP} \sin \gamma t + c_{BP} \cos \beta t + d_{BP} \sin \beta t$$

$$- K_2[a_{BP}\gamma^2 \cos \gamma t + b_{BP}\gamma^2 \sin \gamma t + c_{BP}\beta^2 \cos \beta t + d_{BP}\beta^2 \sin \beta t]] \qquad (C.105.d)$$

$$i_{L1}^{BP} = \frac{1}{L_1} \left[\frac{b_{BP}}{\gamma} \cos \gamma t - \frac{a_{BP}}{\gamma} \sin \gamma t + \frac{d_{BP}}{\beta} \cos \beta t - \frac{c_{BP}}{\beta} \sin \beta t \right.$$

$$\left. + K_2[a_{BP}\gamma \sin \gamma t - b_{BP}\gamma \cos \gamma t + c_{BP}\beta \sin \beta t - d_{BP}\beta \cos \beta t]] + f_{BP} \right. \qquad (C.105.e)$$

$$i_{SL1}^{BP} = \frac{1}{L_{SL1}} \left[\frac{b_{BP}}{\gamma} \cos \gamma t - \frac{a_{BP}}{\gamma} \sin \gamma t + \frac{d_{BP}}{\beta} \cos \beta t - \frac{c_{BP}}{\beta} \sin \beta t \right.$$

$$\left. + K_2[a_{BP}\gamma \sin \gamma t - b_{BP}\gamma \cos \gamma t + c_{BP}\beta \sin \beta t - d_{BP}\beta \cos \beta t]] + g_{BP} \right. \qquad (C.105.f)$$

where

$$d_{BP} = \frac{i_{LM}^{BP} + \frac{i_{L1}^{BP}}{N} - i_{L2}^{BP}\left[(1 - K_2\gamma^2)\frac{2CN}{C_D} + \frac{1}{N}\right]}{2CN\beta K_2(\gamma^2 - \beta^2)} \qquad (C.108.a)$$

$$b_{BP} = \frac{i_{L2}^{BP} - C_D\beta_S d_{BP}}{\gamma_S C_D} \qquad (C.108.b)$$

$$c_{BP} = \frac{\dfrac{(\dfrac{V_{IN}}{2} - V_{C1}^{BP})}{N} + V_{C4}^{BP}(1 - K_2\gamma^2)}{K_2(\beta^2 - \gamma^2)} \qquad (C.108.c)$$

$$a_{BP} = V_{C4}^{BP} - c_{BP} \qquad (C.108.d)$$

$$f_{BP} = I_{L1}^{BP} - \frac{1}{L}\left[\frac{b_{BP}}{\gamma} + \frac{d_{BP}}{\beta} - K_2(\gamma b_{BP} - \beta d_{BP})\right] \qquad (C.108.e)$$

$$e_{BP} = I_{LM}^{BP} - \frac{NL}{L_M}\left[I_{L1}^{BP} - f_{BP}\right] \qquad (C.108.f)$$

$$g_{BP} = I_{SL1}^{BP} - \frac{1}{SL}\left[\frac{b_{BP}}{\gamma} + \frac{d_{BP}}{\beta} - K_2(\gamma b_{BP} - \beta d_{BP})\right] \qquad (C.108.g)$$

or in the normalized form:

$$v_{C4}^{BPN} = a_{BPN}\cos\gamma_N t_N + b_{BPN}\sin\gamma_N t_N + c_{BPN}\cos\beta_N t_N + d_{BPN}\sin\beta_N t_N \qquad (C.109.a)$$

$$i_{L2}^{BPN} = \frac{C_N}{4I_{ON}}\left[b_{BPN}\gamma_S\cos\gamma_N t_N - a_{BPN}\gamma_S\sin\gamma_N t_N\right.$$

$$\left. + d_{BPN}\beta_S\cos\beta_N t_N - c_{BPN}\beta_S\sin\beta_N t_N\right] \qquad (C.109.b)$$

$$v_{C1}^{BPN} = 1 + \left[a_{BPN}\cos\gamma_N t_N + b_{BPN}\sin\gamma_N t_N + c_{BPN}\cos\beta_N t_N + d_{BPN}\sin\beta_N t_N\right.$$

$$\left. - \frac{C_N}{L_N}\left[a_{BPN}\gamma_S^2\cos\gamma_N t_N + b_{BPN}\gamma_S^2\sin\gamma_N t_N\right.\right. \qquad (C.109.c)$$

$$+ c_{BPN}\beta_S^2 \cos \beta_N t_N + d_{BPN}\beta_S^2 \sin \beta_N t_N]]$$

$$i_{LM}^{BPN} = [b_{BPN}\gamma_S \cos \gamma_N t_N - a_{BPN}\gamma_S \sin \gamma_N t_N + d_{BPN}\beta_S \cos \beta_N t_N - c_{BPN}\beta_S \sin \beta_N t_N$$

$$- \frac{C_N}{L_N} [b_{BPN}\gamma_S^3 \cos \gamma_N t_N - a_{BPN}\gamma_S^3 + d_{BPN}\beta_S^3 \cos \beta_N t_N \qquad (C.109.d)$$

$$- c_{BPN}\beta_S^3 \sin \beta_N t_N]]/I_{ON} - i_{L1}^{BPN} + i_{L2}^{BPN}$$

$$i_{L1}^{BPN} = \frac{L_N}{4 I_{ON}} [\frac{b_{BPN}}{\gamma_S} \cos \gamma_N t_N - \frac{a_{BPN}}{\gamma_S} \sin \gamma_N t_N + \frac{d_{BPN}}{\beta_S} \cos \beta_N t_N - \frac{c_{BPN}}{\gamma_S} \sin \beta_N t_N$$

$$+ \frac{C_N}{L_N} [a_{BPN}\gamma_S \sin \gamma_N t_N - b_{BPN}\gamma_S \cos \gamma_N t_N \qquad (C.109.e)$$

$$+ c_{BPN}\beta_S \sin \beta_N t_N - d_{BPN}\beta_S \cos \beta_N t_N]] + f_{BPN}$$

$$i_{SL1}^{BPN} = \frac{L L_N}{4 I_{ON} SL} [\frac{b_{BPN}}{\gamma_S} \cos \gamma_N t_N - \frac{a_{BPN}}{\gamma_S} \sin \gamma_N t_N + \frac{d_{BPN}}{\beta_S} \cos \beta_N t_N - \frac{c_{BPN}}{\gamma_S} \sin \beta_N t_N$$

$$+ \frac{C_N}{L_N} [a_{BPN}\gamma_S \sin \gamma_N t_N - b_{BPN}\gamma_S \cos \gamma_N t_N \qquad (C.109.f)$$

$$+ c_{BPN}\beta_S \sin \beta_N t_N - d_{BPN}\beta_S \cos \beta_N t_N]] + g_{BPN}$$

where

$$\gamma_N = \frac{\gamma}{f_O} \qquad (C.110.a)$$

$$\gamma_S = \frac{\gamma}{\omega_O} \qquad (C.110.b)$$

$$\beta_N = \frac{\beta}{f_O} \qquad (C.110.c)$$

$$\beta_S = \frac{\beta}{\omega_O} \qquad (C.110.d)$$

$$d_{BPN} = \frac{I_{ON}[I_{LM}^{BPN} + I_{L1}^{BPN} - I_{L2}^{BPN}(\frac{4}{C_N}[1 - \frac{C_N}{L_N}\gamma_S^2] + 1)]}{\frac{C_N}{L_N}\beta_S[\gamma_2^2 - \beta_S^2]} \qquad (C.110.e)$$

$$b_{BPN} = \frac{4I_{L2}^{BPN}I_{ON}}{\gamma_S C_N} - \frac{\beta_S}{\gamma_S} d_{BPN} \qquad (C.110.f)$$

$$c_{BPN} = \frac{V_{C1}^{BPN} - 1 + V_{C4}^{BPN}[1 - \frac{C_N}{L_N}\gamma_S^2]}{\frac{C_N}{L_N}(\beta_S^2 - \gamma_S^2)} \qquad (C.110.g)$$

$$a_{BPN} = V_{C4}^{BPN} - c_{BPN} \qquad (C.110.h)$$

$$f_{BPN} = I_{L1}^{BPN} - I_{L2}^{BPN} \frac{L_N(1 - \frac{C_N}{L_N}\gamma_S^2)}{C_N \gamma_S^2} - \frac{d_{BPN}L_N}{4\beta_S}[1 - \frac{C_N}{L_N}\beta_S^2 - (\frac{\beta_S}{\gamma_S})^2(1 - \frac{C_N}{L_N}\gamma_S^2)] \quad (C.110.i)$$

$$g_{BPN} = I_{SL1}^{BN} - \frac{LL_N}{4SL}[b_{BPN}\frac{(1 - \frac{C_N}{L_N}\gamma_S^2)}{\gamma_S} + d_{BN}\frac{(1 - \frac{C_N}{L_N}\beta_S^2)}{\beta_S}] \qquad (C.110.j)$$

$$e_{BPN} = I_{LM}^{BPN} - 4L_N[I_{L1}^{BPN} - f_{BPN}] \qquad (C.110.k)$$

Stage Duration $T_{BP} = T_{BP1} - T_{BPO}$

Stage duration T_{BP} is determined from the condition:

$$v_{C1}(T_{BP}) = V_{IN} \tag{C.111}$$

C.4 DC Voltage-Conversion-Ratio

The dc voltage-conversion-ratio of the soft switched HB is obtained by integrating the rectified voltage, that is, the voltage that appears at the input terminals of the output filter. For full load operation, the converter delivers power to the load only during Stages A, F, H, and I. For light load operation, the converter delivers power also during Stages J, K, L, and M. Therefore, by finding the average rectified voltage during the duration of these stages, the output voltage can be calculated:

$$V_O = f_{con} \Big[\int_0^{T_A} v_R^A dt + \int_0^{T_F} v_R^F dt + \int_0^{T_H} v_R^H dt$$

$$+ \int_0^{T_I} v_R^I dt + \int_0^{T_J} v_R^J dt] \tag{C.112}$$

where v_R^i is the rectified time domain voltage that appears at the input of the output filter during Stage i. The dc voltage-conversion-ratio can be calculated by normalizing Eq. (C.112) with respect to $V_{IN}/2N$:

$$\frac{V_O}{V_{IN}/2N} = M = [\int_0^{T_{AN}} v_R^{AN} dt_N + \int_0^{T_{FN}} v_R^{FN} dt_N + \int_0^{T_{HN}} v_R^{HN} dt_N$$

$$\int_0^{T_{IN}} v_R^{IN} dt_N + \int_0^{T_{JN}} v_R^{JN} dt_N] \tag{C.113}$$

The normalized average rectified voltage for these stages is given by the following expressions:

$$\int_0^{T_{AN}} v_R^{AN} dt_N = \frac{1}{2} [\frac{b_{AN}}{\gamma_N} (\cos \gamma_N T_{AN} - 1) - \frac{a_{AN}}{\gamma_N} \sin \gamma_N T_{AN} + \frac{d_{AN}}{\beta_N} (\cos \beta_N T_{AN} - 1)$$

$$- \frac{c_{AN}}{\beta_N} \sin \beta_N T_{AN} + \frac{C_N}{L_N 2\pi} K_1 [a_{AN} \gamma_S \sin \gamma_N T_{AN} - b_{AN} \gamma_S (\cos \gamma_N T_{AN} - 1)$$

$$+ c_{AN} \beta_S \sin \beta_N T_{AN} - d_{AN} \beta_S (\cos \beta_N T_{AN} - 1)]] - \frac{2I_{ON}}{\pi L_N} (I_{L1}^{BN} - I_{L1}^{AN}) \tag{C.114.a}$$

$$\int_0^{T_{FN}} v_R^{FN} dt_N = T_{FN} - \frac{1}{(2 + \frac{L}{SL})\xi K_1^{1/2}} [a_{FN} \sin \xi K_1^{1/2} T_{FN} -$$

$$b_{FN}(\cos \xi K_1^{1/2} T_{FN} - 1)] \qquad (C.114.b)$$

$$\int_0^{T_{HN}} v_R^{HN} dt_N = (K - 1)T_{HN} \qquad (C.114.c)$$

$$\int_0^{T_{IN}} v_R^{IN} dt_N = -T_{IN} - \frac{K_1}{\xi K_1^{1/2}} [a_{IN} \sin \xi K_1^{1/2} T_{IN} + b_{IN}(\cos \xi K_1^{1/2} T_{IN} - 1)] \qquad (C.114.d)$$

$$\int_0^{T_{JN}} v_R^{JN} dt_N = T_{JN} - \frac{C_N K_5}{2\pi L_N} [a_{JN} \sin \delta t_N - b_{JN}(\cos \delta t_N - 1)] - d_{JN} T_{JN} -$$

$$(I_{L2}^{JN} + I_{SL2}^{JN} - I_{L1}^{JN}) \frac{T_{JN}^2}{2} + \frac{a_{JN}}{K_5} \sin \delta t_N - \frac{b_{JN}}{K_5} (\cos \delta t_N - 1) \qquad (C.114.e)$$

The dc voltage-conversion-ratio is calculated by solving the trancendental equations for every stage to determine their time duration. The voltage-conversion-ratio can only be computed using a nonlinear algorithm. A FORTRAN program is used to calculate the dc voltage-conversion-ratio curves for this converter.

Vita

The author was born in Guatemala City, Guatemala. He received his B.S. degree from North Carolina State University in both Electrical and Mechanical Engineering in 1986. He received his M.S. degree in Electrical Engineering also from North Carolina State University in 1988.

Since starting his doctoral studies at Virginia Polytechnic Institute and State University he has worked on various research projects in the area of power electronics. His research interests include modeling, testing, and design of high-frequency dc-to-dc converters.

The author is a member of the Phi Kappa Phi honor society and the IEEE Power Electronics Society.