ZERO-VOLTAGE SWITCHED RESONANT AND PWM CONVERTERS: DESIGN-ORIENTED ANALYSIS AND PERFORMANCE EVALUATION

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(ABSTRACT)

The relative performance evaluation of the different alternatives of bridge topologies with zero-voltage switching is presented. A design-oriented analysis is developed to optimize implementation of the converters in terms of efficiency. Efficiency optimization requires minimizing the circulating currents which are directly proportional to the reactive energy required by the resonant tank. The comparison of the different converters is based on the reactive energy required for ZVS. The study considers resonant converters with conventional variable frequency control and with phase-shift control, and the zero-voltage-switched full-bridge PWM converter (ZVS-FB-PWM). Also, a systematic procedure to determine all possible resonant converters with two or three reactive elements is presented, and the design-oriented analysis used to classify them according to their properties.

The analysis for the resonant converters uses the fundamental approximation which is verified by comparison with the existing exact analysis for the series resonant converter (SRC), the parallel resonant converter (PRC) and the LCC resonant converter (LCC-RC). Comparison of design examples shows a superior performance for the LCC-RC, and less circulating current for the conventional variable-frequency resonant converters than for the

phase-shifted control version. Experimental verification is provided for the phase-shifted resonant converters.

The effect of switch capacitance on the zero-voltage switching (ZVS) of resonant converters is studied for the SRC, PRC and LCC-RC. The effect of switch capacitance is more pronounced for low Q designs. Consequently, it is of primary importance for the LCC-RC whose optimal design requires low Q values. The results have been verified experimentally in an LCC-RC prototype.

A complete analysis and design procedure are provided for the new ZVS-FB-PWM converter, including a new active clamp circuit that completely eliminates the ringing in the rectifiers. The design procedure and design considerations have been verified with three experimental prototypes.

The comparison of the resonant converters with the ZVS-FB-PWM converter based on the reactive power required for ZVS, shows that the ZVS-FB-PWM converter is a superior alternative to resonant converters. The ZVS-FB-PWM converter always has less circulating current than the resonant converters when it is designed for a limited ZVS range.

To my parents Josep

and Mª del Carme

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1. Introduction

1.1 Background and Motivation

The increasing demand for power processors with higher power density has led to a progressive increase of the switching frequencies. Operation at higher frequencies results in a considerable size reduction for transformers and filters. However, losses associated with high-frequency operation have to be kept as low as possible to achieve efficient power conversion. At high frequencies, switching losses become very high, making many conventional circuits impractical, or at least partially limiting the size reduction and resulting in poor efficiencies.

The main factors that contribute to the high-frequency switching losses are:

- Semiconductor devices used as switches in power processors have non-zero turn-on and turn-off times, and as a result, during switching transitions between on-state and

off-state, the devices can be conducting significant current while there is a large voltage applied across them. This current and voltage overlap results in a large amount of energy being dissipated in the switching device. At high frequencies the energy lost in the overlap becomes the largest part of the total losses in the switches.

- Due to the high dv/dt and di/dt required at high frequencies, voltage and current oscillations are induced in parasitic capacitances and inductances during the switching transitions. These oscillations result in higher peak current and voltage in the switches, increasing the losses due to the voltage and current overlap, and requiring switching devices with higher voltage and current ratings. Also, these oscillations generate EMI that can couple other parts of the converter, or even surrounding electronic equipment.

- Every time a device is turned on while there is voltage applied across it, the energy stored in the parasitic capacitance across the devices is dissipated in the switch. This power loss in the switches increases proportionally to the frequency and to the square of the switches' off-voltage.

Soft-switching techniques have been developed to reduce switching losses, allowing efficient power conversion even for frequencies in the megahertz range for low powers, and hundreds of kilohertz for multikilowatt powers. Soft-switching for the power devices can be achieved either with zero-current switching (ZCS) or with zero-voltage switching (ZVS). Zero-current switching consists of turning off the switches when there is no current circulating through them. ZCS is also called natural commutation. Zero-voltage

switching consists of turning on the switches when there is no voltage applied across them.

Common to all approaches to soft-switching is the use of reactive elements, present in the circuit as parasitics, or purposely added. The reactive elements shape the currents and voltages to achieve ZVS or ZCS.

According to the principle of operation, soft-switching converters can be grouped in three families: resonant converters, quasi-resonant and multi-resonant converters, and PWM converters with resonant transitions.

The basic resonant converter structure consists of a square wave inverter, a reactive network, a rectifier stage, and an output filter. The inverter applies a square wave of voltage or current to the reactive network, also called the resonant tank. In the voltage inverter case, the resonant tank is designed so that it presents high impedance to the high-frequency harmonics of the square waves at the output of the inverter stage, avoiding sharp edges in the current waveforms drawn from the inverter. In the current inverter case, the resonant tank is designed so that the voltage at the output of the inverter has soft transitions.

Due to the reactive nature of the resonant tank, the load of the inverter stage can have a leading or lagging power factor. In the voltage inverter case, a load with a leading power factor forces the current through the switching device to be zero before it is turned off, resulting in ZCS. A lagging power factor load forces the antiparallel diode of each switch to be conducting when the device is turned on, resulting in ZVS. The reactive

power factor implies that a certain amount of energy is returned to the source each switching cycle. This excess of energy delivered to the resonant tank is always required to achieve soft-switching. The design has to be such that the increased conduction losses due to the circulating energy do not outweigh the savings in switching losses. The consideration of the reactive power that circulates between the resonant tank and the inverter stage is critical in the design. The work presented here provides a design-oriented analysis that can be applied to all resonant converters, and that provides a general way to determine the reactive power for each resonant converter.

An additional advantage of resonant converters is that the sinusoidal nature of currents or voltages also provides soft transitions (ZVS or ZCS) for the rectifier stage, reducing switching losses and oscillations on the rectifier diodes.

The topologies used for the inverter stage are half-bridge [A-3, A-4, A-8], full-bridge [A-5, A-8], push-pull [A-8, A-46] or single ended, also called class-E [E-1, E-4]. This work deals mostly with bridge topologies. Two main reasons support this choice. The first is that bridge topologies are used for medium and high power levels at which parasitics can become significant even at frequencies of several kilohertz, requiring a converter topology able to operate efficiently even in the presence of parasitic reactances, and consequently, this has been the typical application of resonant converters. The second reason is that the bridge inverter naturally limits peak current or voltage in the switching devices, resulting in reduced stresses on them compared with single-ended topologies [A-8, F-9].

Resonant converters were first introduced to make possible the use of switches without controllable turn-off capability (*i.e.* thyristors) to interrupt dc voltage or current [A-1, A-2]. Hence, the first resonant converters were used for zero-current switching. ZCS also proved to be beneficial for circuits using BJT's, because it reduces the turn-off delay associated with bipolar devices. However, zero-voltage switching is more advantageous for high-frequency operation. The maximum frequency for zero-current switching is limited by the turn-on losses associated with the discharge of the output capacitance of the switches. This loss is proportional to the value of the output capacitance and switching frequency of the devices and is dependent quadratically on the switch voltage prior to turn-on.

Zero-voltage switching eliminates the losses associated with the discharge of their output capacitance, and allows the use of external capacitors across the switches as lossless snubbers [A-8, A-24, A-28, A-29]. Also, for bridge topologies, ZVS avoids increased turn-on losses due to the reverse recovery current in the diodes in parallel with the switches [A-8, C-19, C-20].

Consequently, ZVS operation offers considerable advantages when compared to ZCS: Slow diodes can be used, making it possible for MOSFET's to use their internal body diode reducing the number of components. Also, with the addition of capacitors as lossless snubbers the turn-off losses can be drastically reduced, resulting in a converter with negligible switching losses [A-25]. The work presented here is devoted to ZVS operation for bridge topologies.

Conventional resonant converters use an inductor in series with a capacitor as a resonant tank. Two basic configurations are possible for the load connection: For the parallel resonant converter (PRC) the rectifier-load stage is placed in parallel with the resonant tank capacitor, and for the series resonant converter (SRC) the rectifier-load stage is placed in series with the LC tank [A-4, A-8]. Studies of the performance and design of these two resonant converters include dc-characteristics [A-3 to 5, A-8, A-13, A-16 to 17], small-signal analysis [A-7, A-9, A-11, A-52], and design optimization [A-19, A-21, A-25, A-28, A-39]. A few studies consider the effect of resonant components with losses [A-12, A-32].

At high frequencies parasitic reactances in the circuit cannot be neglected, and if the parasitics cannot be considered part of the LC series resonant tank, the converters' characteristics are significantly modified. Analysis of several new topologies with more than two resonant elements that-can not be reduced to a series LC has shown that in some cases the resulting converter may have desirable features for some applications [B-4, B-5]. This has motivated the analysis of many possible resonant tank topologies with three or more elements [B-14, B-23].

The best known topology with three resonant elements consists of a series LC branch in series with a capacitor in parallel with the rectifier/load stage [B-2 to B-5, B-6 to B-13, B-15 to B-23, B-28]. The resulting converter is called a series-parallel resonant converter because it combines features of the SRC and PRC. Another common name for the converter is LCC resonant converter. The LCC resonant converter improves the partial load efficiency compared to the PRC and provides better regulation than the SRC

for line-load variations [B-4]. Also, the series resonant capacitor provides dc blocking that is required when using a transformer for isolation. The LCC resonant converter will be used to compare three-element resonant converters with the conventional two-element resonant converters (SRC and PRC).

A large number of new topologies are possible using more than two resonant elements. Some have been analyzed, but a more comprehensive and systematic analysis is required to assess their potential advantages. This work presents a set of rules for an exhaustive search of possible topologies, and a design-oriented analysis that permits evaluation of trade-offs involved in each topology for ZVS operation. The generality of the analysis allows a comparative evaluation of the topologies found.

The ZVS operation requires the voltage across the devices to be zero when the device is turned on. Since for an efficient design the amount of energy available for ZVS is minimized, the parasitic output capacitance of the devices becomes a critical parameter to considered in order to ensure ZVS. The output capacitance of the switches cannot be considered part of the resonant tank because it is only active during each of the switching transitions. Consequently, their effect has to be analyzed separately. In this work it will be shown that this capacitance reduces the load and voltage range for which ZVS can be achieved, and alters the characteristics of the converter [H-1 to H-4, H-6].

The control of resonant converters typically requires variable-frequency operation [A-2, A-15, A-18, A-22, A-23, A-34, A-41]. For wide input-voltage range and load range, the frequency range can be large. The magnetic components have to be

designed to operate over the whole frequency range, making their optimization difficult. Also, the bandwidth of the closed-loop control, determined by the minimum switching frequency, is compromised. Several control techniques allow operation at fixed frequency [C-1, C-3, C-4, C-7, C-11]. All of them consist of applying a quasi-square wave of variable duty cycle to the tank, and using this duty cycle to regulate the output. When using a quasi-square wave of variable duty cycle, ZVS or ZCS may not be retained for the whole input voltage range or load range [C-11, C-18]. Some topologies result in a more efficient design while retaining soft-switching over all load and line variations. A systematic study is needed to determine which resonant tank configuration would provide the most desirable properties. The same procedure used for the conventional resonant converters is applied in this work to constant frequency resonant converters. This permits the comparison of the performance of constant-frequency resonant converters with two and three elements with their variable frequency counterparts.

Quasi-resonant and multi-resonant converters are derived from pulse-width-modulated (PWM) topologies by adding reactive elements to shape the current and voltage in the switches [F-1, F-2]. Power regulation is still achieved by varying the ratio between on and off-time of the switches. However, variable frequency is required in most cases for regulation. Typically, ZCS converters are controlled using fixed on-time for the switches, and ZVS converters using fixed off-time [F-3, F-9, F-10]. Variable frequency control results in problems similar to the ones mentioned for resonant converters.

Several families of quasi-resonant and multi-resonant converters with fixed frequency operation have been developed [F-17]. The fixed frequency is achieved at the

cost of increased complexity of the circuit. The resulting topologies have efficiencies and sizes similar to their variable frequency counterparts, but their main advantage is in better control characteristics and easier suppression of EMI.

ZVS for quasi-resonant and multi-resonant converters has been implemented in single-ended converters and bridge topologies as well. The major disadvantage of single-ended topologies is that the peak voltage across the switches is much larger than for their PWM counterparts. In bridge topologies the peak voltage in the switches is clamped by the input voltage supply and that makes bridge topologies more attractive. A comprehensive study of topologies and design procedures can be found in Refs. [F-1 to F-21].

A different approach to obtaining ZVS is given by the PWM converters with resonant transitions. The main difference between this approach and the resonant approaches is that the ZVS is achieved with a resonance during the switching transition that does not play any significant part in the energy transfer.

Recently these techniques have gained considerable interest because they combine the good features of PWM converters: fixed-frequency operation and trapezoidal shape voltages and currents. The ZVS is achieved by discharging the capacitance in parallel with the switches by means of the parasitic inductance present in the circuit. Early works report the ZVS features inherent to bridge topologies operated with phase-shift control [G-1 to G-3] without mention of the proper design to fully utilize the ZVS capability. The design equations and optimization procedure for the power stage is

presented in this work; the results obtained have been published in Refs. [G-17, G-22, G-24].

The most popular converter is the zero-voltage-switched full-bridge PWM (ZVS-FB-PWM) converter [G-6, G-9, G-10, G-17, G-18]. This circuit uses a full-bridge topology with phase-shift control for the switches in the bridge and does not require any additional resonant components. The parasitic leakage inductance of the transformer at the output of the bridge introduces a phase-lag between the current supplied by the bridge and the square wave voltage forcing the diodes in the bridge to conduct before any switch is turned on, in a way similar to how ZVS is achieved for resonant converters in bridge topologies. However, the loss of ZVS with partial loads is gradual, and therefore less detrimental to the performance than in the case of the phase-shifted resonant converters [G-22].

The application of this technique has been extended to other topologies such as the two-switch forward [G-19] and push-pull [G-28], and also for dc-dc transformers without output voltage regulation [G-4, G-20, G-36].

The need for optimized control of the phase-shifted ZVS-FB-PWM converter has motivated the development of small-signal models [G-21, G-26]. The feasibility of current mode control has been proved [G-13, G-17, G-24] and even commercial IC's are already available for their control [G-25]. Other control techniques are also possible like one that uses asymmetrical control of a half-bridge topology [G-19].

The leakage inductance used to achieve ZVS can be replaced in some cases by a saturable reactor in series with the transformer; which reduces the energy storage needed in the inductance in series with the transformer for extended ZVS range and reduces the severity of the oscillations in the rectifier [G-32]. However, the high-frequency losses in saturable reactors for the magnetic materials available limit its application to low power and medium switching frequencies.

Also, several works propose the use of the magnetizing inductance to achieve ZVS. This is made possible by disconnecting the secondary during the switching transitions, either by switches [G-28] or saturable reactors [G-15, G-31]. The saturable reactors have the limitations mentioned in the previous paragraph, while the use of additional switches is not always desirable for high-frequency high-power applications.

A major problem for high power and high-voltage applications is that when a large ZVS range is required the relatively large leakage inductance of the power transformer rings with the rectifiers' capacitance. This causes large oscillations in the secondary voltage that are difficult to snubber. To reduce the amplitude of the ringing, several possible clamp circuits for the secondary have been proposed [G-11, G-17]. In this work a new active clamp circuit that completely eliminates the ringing in the rectifier is presented. The results of the analysis of the active clamp and hardware implementation have been published [G-24].

Other alternatives that add external reactive elements or circuits not in series with the main power path to obtain ZVS are outside the scope of this work. For reference purposes, since they are in the same area of interest, the main alternatives are:

- To add a resonant-pole. The energy to discharge the output capacitance of the devices is provided by the current circulating through the resonant pole branch during the switching transitions. The resulting converter waveforms are very similar to the ones obtained for resonant converters [G-5, G-7, G-8, G-29, G-33].

- To use an auxiliary network with an active switch that is active during the on-off transitions and the off-time of the main switch [G-35]. The purpose of the auxiliary network is to force the antiparallel diode of the main switch to conduct before the switch is turned on, and to recover the energy stored in the switch's output capacitance. ZVS is achieved at the cost of increased complexity of the circuit and the added losses of the auxiliary circuitry. It is an attractive option for some single-ended topologies [G-35, G-37].

1.2 Objectives of the Research

The need for high-density, reliable and efficient dc to dc converters for the medium to high-power range has motivated the study of ZVS techniques for bridge

topologies. The many options available make their selection for a particular application extremely difficult.

This work's main objective is to provide design procedures to minimize the circulating currents, because circulating currents result in increased conduction losses and larger transformer size. Since the circulating currents are directly proportional to the reactive energy required by the resonant tank, a comparison of designs is based on the reactive energy required for ZVS.

The design-oriented analysis provides the reactive power required for ZVS by each of the converters studied. Since the same analysis approach is used for the conventional resonant converters with variable-frequency control and resonant converters with fixed frequency control (phase-shift), the two cases can be easily compared to assess their relative merits and limitations.

The analysis of resonant converters neglects the reactive parasitics not included in the resonant tank. However, for ZVS the switch capacitance is of primary importance, and because it only affects the operation during the switches' transitions, cannot be included in the resonant tank. The use of low Q designs and external capacitors as lossless snubbers modifies the ZVS limits and characteristics of resonant converters. Conventional two-element resonant converters in general use designs with $Q>1$, but new resonant converters with three elements (like the LCC resonant converters) require operation with low Q values resulting in a more pronounced effect of the switch capacitance. This effect

is studied for the SRC, PRC and LCC converters, showing the effect for each case. Design rules taking this effect into account are provided.

The new ZVS-FB-PWM converter is studied as a superior alternative to resonant converters in most cases. A complete analysis and design procedure are provided, including a new active clamp circuit that eliminates the ringing in the rectifiers.

The generality of the design-oriented approach used for resonant converters allows a comparison of the resonant converter with the ZVS-FB-PWM converter.

The detailed objectives for each of the converter types studied are:

- For **resonant converter** topologies with **variable-frequency control**:
  - Development of an analysis procedure for assessment of merits and limitations of resonant topologies that can be applied to all resonant converters.
  - To define a systematic design procedure for resonant converters based on the required reactive power.
  - To determine a systematic procedure to derive all possible topologies of resonant converters with two and three reactive elements in the resonant tank.
  - Comparison of the LCC topology with three resonant elements to the SRC and PRC.
  - Analysis of the effect of switch capacitance in the converters' performance.
- For **resonant converters** with **constant-frequency** control techniques:
  - Assessment of merits and limitations of constant-frequency control techniques.

- Comprehensive design-oriented analysis of phase-shift-controlled (clamped mode) series and parallel resonant converters.
- Design-oriented analysis of phase-shift-controlled LCC resonant converter.
- Comparison of phase-shifted series an parallel resonant converters with the phase-shifted LCC resonant converter.

- For the **zero-voltage-switched full-bridge PWM** (ZVS-FB-PWM) converter:
  - Comprehensive analysis of phase-shifted ZVS-FB-PWM converters.
  - Determination of the design procedure for ZVS-FB-PWM converters.
  - Evaluation of performance of practical implementation of ZVS-FB-PWM converters. The effects of parasitics and circuit variations.
  - Development of an active clamp to eliminate the rectifier ringing: Analysis and design procedure.
  - Comparison of ZVS-PWM techniques with resonant techniques.

1.3 Major Results

The major results of the research can be summarized as follows:

1. The development of a design-oriented analysis of **resonant converters** for assessment of merits and limitations of possible topologies has produced:
    - An analysis technique with general application to resonant converters with an arbitrary resonant network.
    - Validation of the analysis technique compared to the exact analysis.
    - Definition of rules to generate all new possible resonant networks with two and three reactive elements, and their classification according to general properties.
    - Assessment of ZVS implementation feasibility.
    - To determine how to relate the normalized results to actual stresses in the switches and the resonant elements, and use of the reactive power analysis to optimize the converters for minimum circulating currents.
    - Comparison of SRC and PRC with LCC resonant converter designs to show that the LCC resonant converter has superior performance in terms of circulating currents and frequency range required for control.
2. The study of the ZVS implementation with **resonant converters** operated at **constant frequency** has produced:

- A simplified analysis technique to determine characteristics of phase-shift-controlled resonant converters.
- Comparison of the results with the exact analysis for the SRC and PRC with phase-shift control.
- Design optimization in terms of reactive power.
- Assessment of ZVS capabilities of different resonant networks with more than two reactive elements.
- Comparison of PS-SRC and PS-PRC in terms of ZVS capabilities.
- Experimental verification of the comparison of PS-SRC and PS-PRC.
- Comparison of PS-SRC and PS-PRC with a converter with three reactive elements, PS-LCC, in terms of ZVS capabilities, and circulating currents.
- The comparison of phase-shifted resonant converters with their variable frequency-control counterparts to show that the phase-shift-control designs result in larger reactive powers.

3. Analysis of resonant converters including the **effect of parasitics** on the ZVS. Generalization to multi-element resonant converters.
    - Analysis of the effect of switch capacitances in the ZVS performance of SRC, PRC, and LCC resonant converters.
    - Extension of the conclusions to other possible resonant networks.
    - Experimental verification for the LCC resonant converter.
4. The comprehensive analysis of the **ZVS-FB-PWM converter** has produced:

- Design-oriented analysis of the ZVS-FB-PWM converter.
- Determination of ZVS capabilities with input voltage range and load variation.
- Determination of a systematic design procedure.
- A modified converter with the addition of a secondary voltage clamp. Analysis and design procedure.
- Optimization of the design in terms of reactive power.
- Experimental verification of the design procedure, and practical considerations required for two prototypes used as examples.

5. Evaluation of performances of ZVS-FB-PWM converters and comparison to the resonant converter alternatives has produced:

- The ZVS-FB-PWM converter results in superior performance than the resonant converters when it is designed for a limited ZVS range.

Part of the results obtained have been published in Refs. [C-18, C-19, C-20, C-31, G-20, G-24, G-25, G-27].

2. Design-Oriented Analysis of Resonant Converters

2.1 Introduction

This chapter consists of three major parts. The first part presents the definition of resonant converters and a simplified analysis that uses the fundamentals of currents and voltages in the converters. The analysis is used on all the topologies of resonant converters with two elements to determine their basic properties.

The second part presents a systematic search of possible resonant converters with three reactive elements using the definition provided at the beginning of the chapter. The simplified analysis is used to determine the transfer functions for all possible topologies, and to evaluate their main properties. Their properties are related to the well-known conventional resonant converters, series resonant converter (SRC), and parallel resonant converter (PRC). The LCC resonant converter is selected for comparison in design with the SRC and PRC because of its special characteristics.

Finally, in the third part the design considerations for resonant converters are addressed. The resonant tanks provide soft switching for the devices in the inverter bridge and the rectifier. However, the reactive nature of the resonant tank results in a certain amount of reactive power that circulates between the converter and the input source. Using the simplified analysis presented in this chapter, the current stresses in the devices in the bridge, and the reactive power delivered to the converter can be determined normalized with respect to the output power. This allows the evaluation of the increase in current stress with respect to PWM converters, and also the comparison of different resonant converters. A comparison of designs for the SRC, PRC and LCC resonant converter summarizes the comparison.

2.2 Resonant Converter Structure

A great number of publications about resonant converters are available in the literature. However, no clear definition of what a resonant converter is has been reported. Among the descriptions available, we have:

- In a very early publication by Schwarz [A-2], he refers to resonant converters as: *"Converter philosophy for controlled transfer and transformation of electric energy through internal series resonant circuits,"* with, *"control of the continuously oscillating high Q series resonant circuit"*, where, *"the converter's output circuit extracts cyclically and in a controlled fashion energy from this oscillating circuit to satisfy the load."*

- Also, Steigerwald [A-10], refers to them as: *"Transistor dc-dc converters which employ a resonant circuit."* And, describing the circuit he adds, *"The resonant circuit is driven with square waves of current or voltage , and by adjusting the frequency around the resonant point, the voltage on the resonant components can be adjusted to any practical voltage level."*

- Also a very general, more functional description by Oruganti [A-14], calls a resonant converter, *"A power converter that uses the circuit resonance to commutate a power device, with the objectives of reducing the switching losses and stresses of the power devices so that higher efficiencies and higher power conversion frequencies can be obtained."*

- Probably the more accurate description of what is known as resonant converters is given by Severns [B-22]. He describes a resonant converter as a power processor that fits the two following statements:

  1.- *"The power transfer from input to output is primarily via the fundamental component of the switching frequency. The harmonics of the source and load contribute little to the power transfer. (i.e. Resonant tank acts as either a bandpass or lowpass filter, isolating the input and output at harmonics of the switching frequency)."*

  2.- *"The waveforms of the voltage or current response of the tank to the excitation of the source and the load is piecewise sinusoidal."*

Using this last definition, the general structure of a dc to dc resonant converter is depicted in Fig. 2.1. An input voltage or current source connected to an inverter through the input filter. The inverter provides a square voltage or current that excites the resonant network, which may contain a transformer. Following the resonant network a rectifier is placed, which provides a unidirectional voltage or current. Finally, after passing through the output filter, dc voltage or current is obtained for the load.

The combination input source and filter, and output filter and load, can be considered ideal sources for a properly designed filter. The selection of the resonant network affects the performance of the converter mainly in the following:

- power transfer characteristics,
- how soft-switching is achieved for the devices in the inverter and rectifier,
- the stresses for the devices,

In the next section, a frequency domain analysis for design purposes is presented. This will provide a very general way to determine the power transfer characteristics for different resonant tanks, and also determine the effect on the devices of the inverter and the rectifier.

The design oriented analysis also provides a general way to determine for which operating conditions zero-current switching (ZCS) or zero-voltage switching (ZVS) for the power devices can be achieved, and the reactive power delivered to the resonant network.

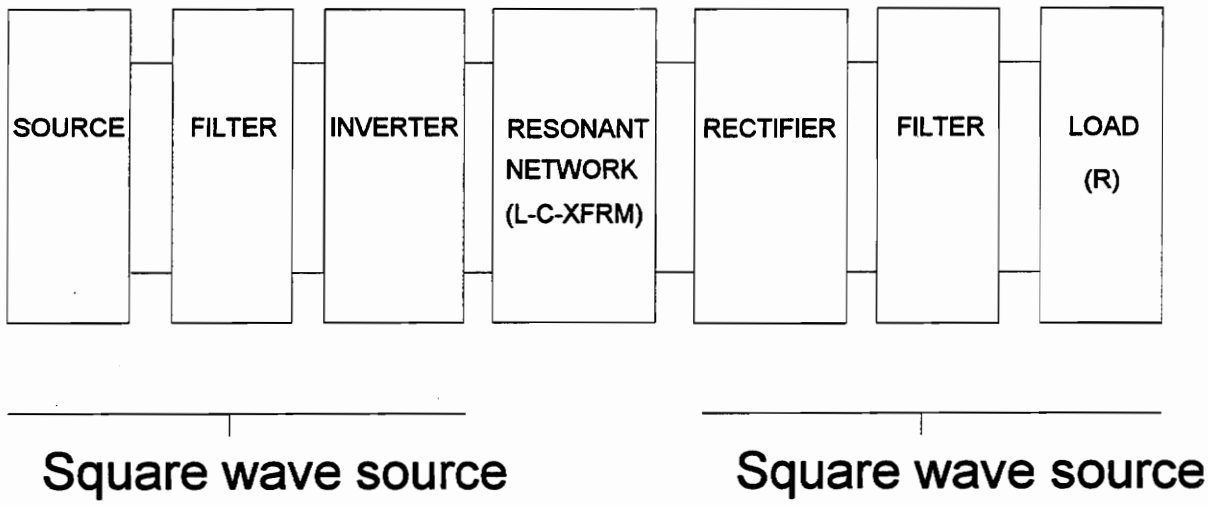


Figure 2.1: Resonant converter structure

2.3 Frequency-Domain Analysis

The frequency domain analysis is based on the fact that the energy transfer is done at the fundamental of the switching frequency. The resonant tank is designed to eliminate the high-frequency harmonics. Consequently, the design for the resonant converters can be done considering only the fundamental of the waveforms involved in the process. The results obtained with this analysis are compared with the results of the exact analysis for some resonant converters, when available. Also, secondary effects that affect the design and that require a more detailed analysis are presented separately.

The first step in this analysis is to define the inverter excitation and load of the resonant tank in terms of the switching frequency fundamental. Figure 2.2 presents the combination of the input source filter and inverter which provides the resonant tank input excitation.

Using Fourier series decomposition the voltage or current excitation can be expressed as:

$$v_{in} = \frac{4}{\pi} \cdot V_{in} \cdot \sum_{n=1,3...}^{\infty} \frac{\sin(n \cdot \omega_{sw} \cdot t)}{n}, \tag{2.1}$$

$$i_{in} = \frac{4}{\pi} \cdot I_{in} \cdot \sum_{n=1,3...}^{\infty} \frac{\sin(n \cdot \omega_{sw} \cdot t)}{n}, \tag{2.2}$$

where V_{in} and I_{in} are the dc input voltage and current, respectively.

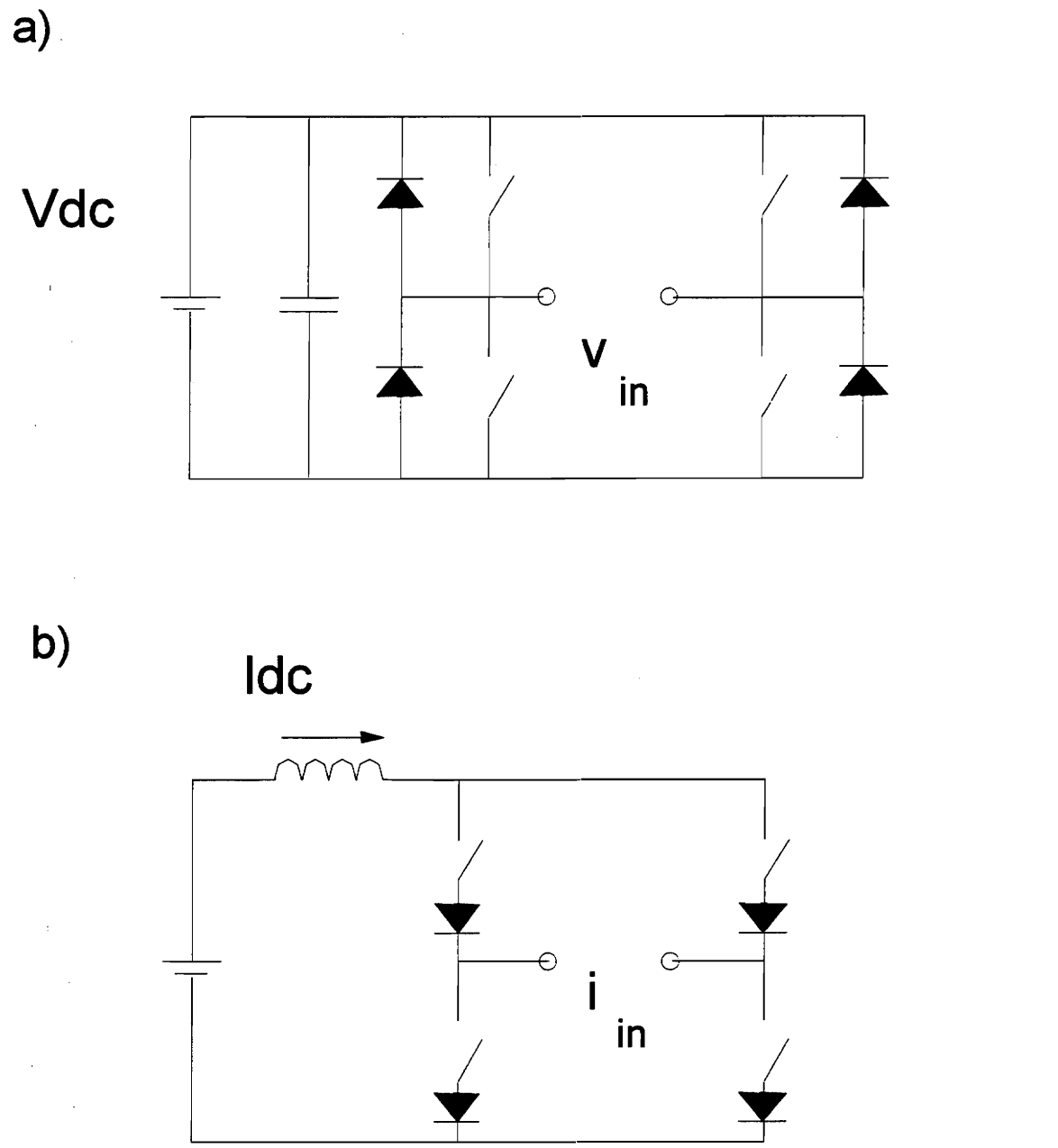


Figure 2.2: **Resonant tank excitation: a) voltage excitation circuit, b) current excitation circuit.**

The load of the resonant network is a rectifier with a capacitive or inductive filter. This results in a square wave of current or voltage applied to the tank. An inductive filter results in a current square wave associated to a sinusoidal voltage in the tank, and a capacitive filter results in a square voltage associated to a sinusoidal current in the tank. Since this square wave is applied to the tank by the rectifier, the current and voltage are always in phase. Using the fact that the energy transfer is done at the fundamental frequency of the switching frequency, this load can be represented by a resistor, R_{ac} ,that corresponds to the ratio of the fundamental components of the voltage and the current at the input of the rectifier. The rectifier load side of the converter is depicted in Fig. 2.3.

For the capacitive filter case (Fig. 2.3a), the fundamental of the voltage and the current at the input of the rectifier are

$$v_{ac} = \frac{4}{\pi} \cdot V_{out} \cdot \sin(\omega_{sw} \cdot t) \text{ for a voltage inverter, and} \qquad (2.3)$$

$$i_{ac} = \frac{\pi}{2} \cdot I_{out} \cdot \sin(\omega_{sw} \cdot t) \text{ for a current inverter} \qquad (2.4)$$

where V_{out} and I_{out} are the dc output voltage and current, respectively. Consequently the equivalent resistance is

$$R_{ac} = \frac{V_{ac}}{I_{ac}} = \frac{8}{\pi^2} \cdot R_{out}\,, \qquad (2.5)$$

where R_{out} is the actual dc load resistance of the converter.

Proceeding analogously for the inductive filter case, we have:

$$v_{ac} = \frac{\pi}{2} \cdot V_{out} \cdot \sin(\omega_{sw} \cdot t), \qquad (2.5)$$

$$i_{ac} = \frac{4}{\pi} \cdot I_{out} \cdot \sin(\omega_{sw} \cdot t) \text{ , and} \tag{2.6}$$

$$R_{ac} = \frac{V_{ac}}{I_{ac}} = \frac{\pi^2}{8} \cdot R_{out} \text{ .} \tag{2.7}$$

The voltage or current gain of the dc to dc converter corresponds to the gain of the resonant network multiplied by a constant. Four cases have to be considered:

- Voltage inverter, and capacitive filter after the rectifier:

$$M_V = \frac{V_{out}}{V_{in}} = \frac{v_{ac}}{v_{in}} \tag{2.8}$$

- Current inverter, and inductive filter after the rectifier:

$$M_i = \frac{I_{out}}{I_{in}} = \frac{i_{ac}}{i_{in}} \tag{2.9}$$

- Voltage inverter, and inductive filter after the rectifier:

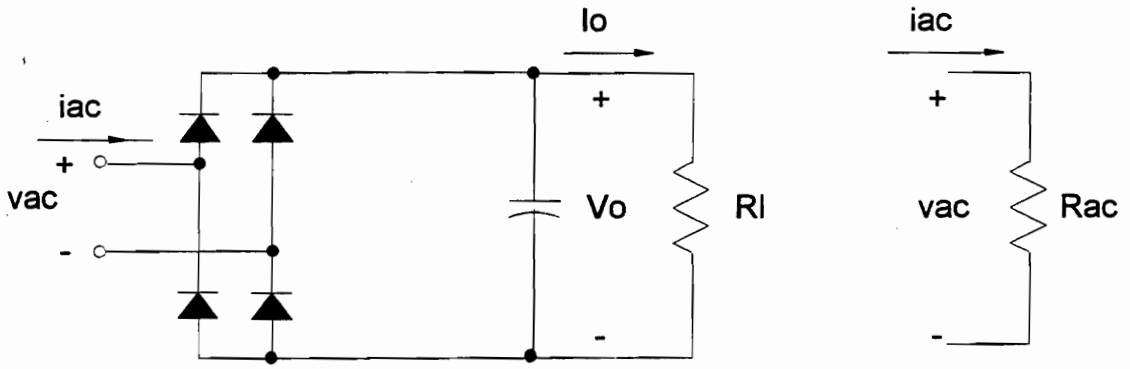
$$M_V = \frac{V_{out}}{V_{in}} = \frac{8}{\pi^2} \cdot \frac{v_{ac}}{v_{in}} \tag{2.10}$$

- Current inverter, and capacitive filter after the rectifier:

$$M_i = \frac{I_{out}}{I_{in}} = \frac{8}{\pi^2} \cdot \frac{i_{ac}}{i_{in}} \tag{2.11}$$

The currents and voltages in the converter can be calculated using the fundamental component of the input source, the corresponding equivalent resistor, and the impedances of the resonant network at the switching frequency.

a)



b)

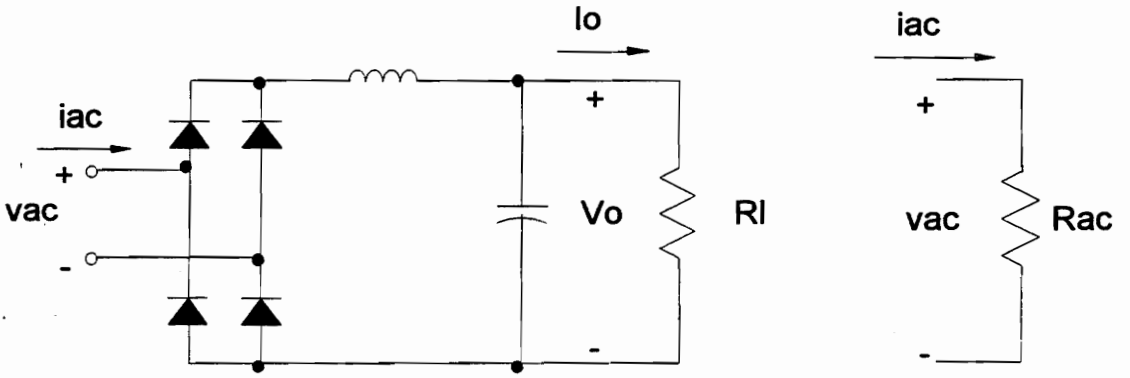


Figure 2.3: Resonant tank load: a) rectifier with capacitive filter, b) rectifier with inductive filter.

2.4 Soft Switching with Resonant Converters

Rectifier

Soft switching consists on avoiding voltage and current overlap during the on-off transitions on the devices, and a finite-slope increase of the voltage or current after the transition. In the rectifier, the transition for the diodes is done at the zero crossing of the ac voltage or current applied from the tank varying sinusoidally. Consequently, the switching losses and ringing are considerably reduced with respect to the PWM converters case. However, parasitics, such as diode capacitance, and leakage inductance of the transformer, together with reverse recovery currents, can still result in switching losses and ringing because the current or the voltage increase sharply.

The ability of resonant converters to minimize the effects of the parasitics on the rectifier stage depends on how effectively a topology can incorporate the parasitics into the resonant network. The diodes' capacitance can be incorporated either into the output filter in the capacitive filter case, or into a capacitor of the resonant network in parallel with the diodes. The transformer leakage inductance has to be part of an inductance of the resonant network. This issue will be addressed when presenting the possible resonant network topologies.

Inverter

Since the inverter transitions are externally controlled, soft switching depends on the relative signs of current and voltage at the on-off transition. The equivalent circuit seen from the inverter output is shown in Fig. 2.4. Due to the reactive nature of the resonant tank, the load of the inverter stage, Z_{in} , at the switching frequency, can have a leading or lagging power factor.

In the voltage inverter case, the switches can block current in one direction. In the voltage inverter case, a load with leading power factor forces the current through the switching device to be zero before it is turned off, providing ZCS. A lagging power factor load forces the antiparallel diode of each switch to be conducting when the device is turned on, resulting on ZVS. Figure 2.5 and 2.6 show the typical waveforms for these two cases, when a voltage inverter is used.

Also in the current inverter case a lagging power factor results in ZCS operation, and a leading power factor results in ZVS operation. However, ZVS in general cannot be achieved for the switches. The MOSFET switches require a series blocking diode because they do not have reverse blocking capability, and the series diode prevents the output capacitance of the switch from discharging before the MOSFET is turned on.

The inverters in Figs. 2.5 and 2.6 are implemented with MOSFET's. In the ZCS case the MOSFETs require fast antiparallel diodes, because the diodes are hard switched. The turn-on of each MOSFET turns off the diode in parallel with the other switch in the same leg. Since the diodes are turned off with high dv/dt and di/dt, they go through a severe reverse recovery process. To avoid shorting the input source because of the slow

recovery of the MOSFET's body diode, an additional external diode is placed in series to block the body diode and a fast external antiparallel diode is used.

The ZVS or ZCS operating regions can be determined by calculating the value of the phase of the impedance seen by the inverter. The fundamental approximation method just described provides a simple way to perform this calculation. In addition to that, as will be shown for several converters, the method is very accurate around the transition of the tank impedance from capacitive to inductive. A case for which circuit parasitics have to be considered is presented in Chapter 4. The analysis in Chapter 4 shows the effect of significant switch capacitance on the ZVS range.

The reactive power factor implies that a certain amount of energy is returned to the source each switching cycle. This excess energy delivered to the resonant tank is always required to achieve soft-switching. The design has to be such that the increased conduction losses due to the circulating energy do not overcome the savings in switching losses. The reactive energy required for a particular design depends on the resonant network employed. This is going to be the basis of comparing different resonant networks in the following chapters.

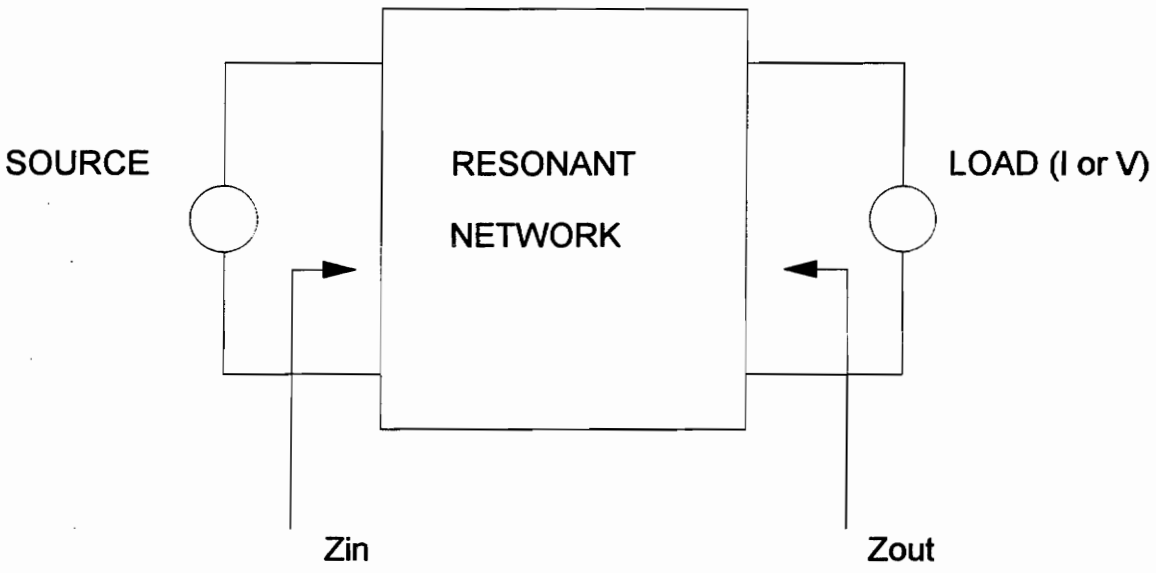


Figure 2.4: Equivalent load of the inverter stage.

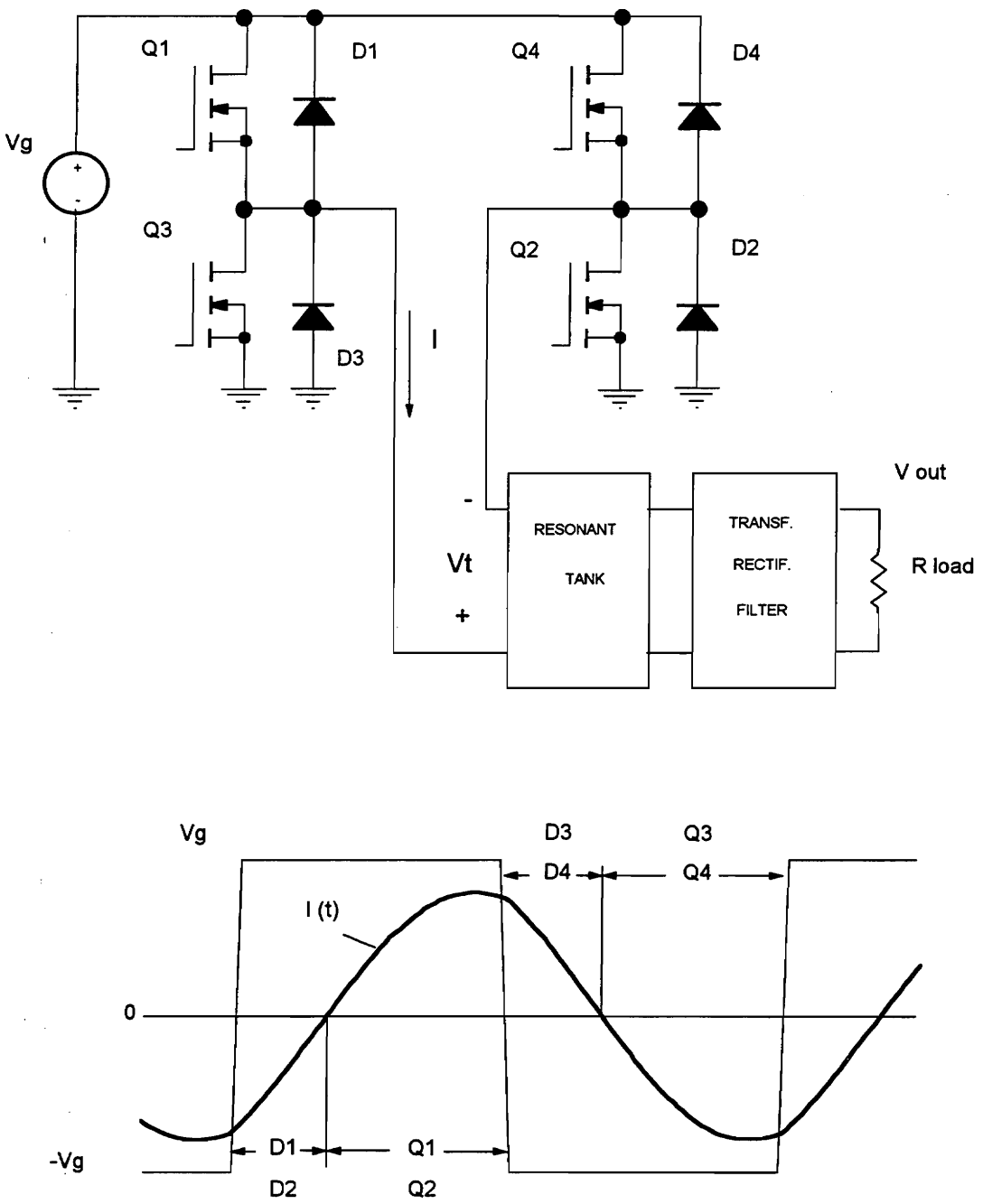


Figure 2.5: ZVS operation of a resonant converter.

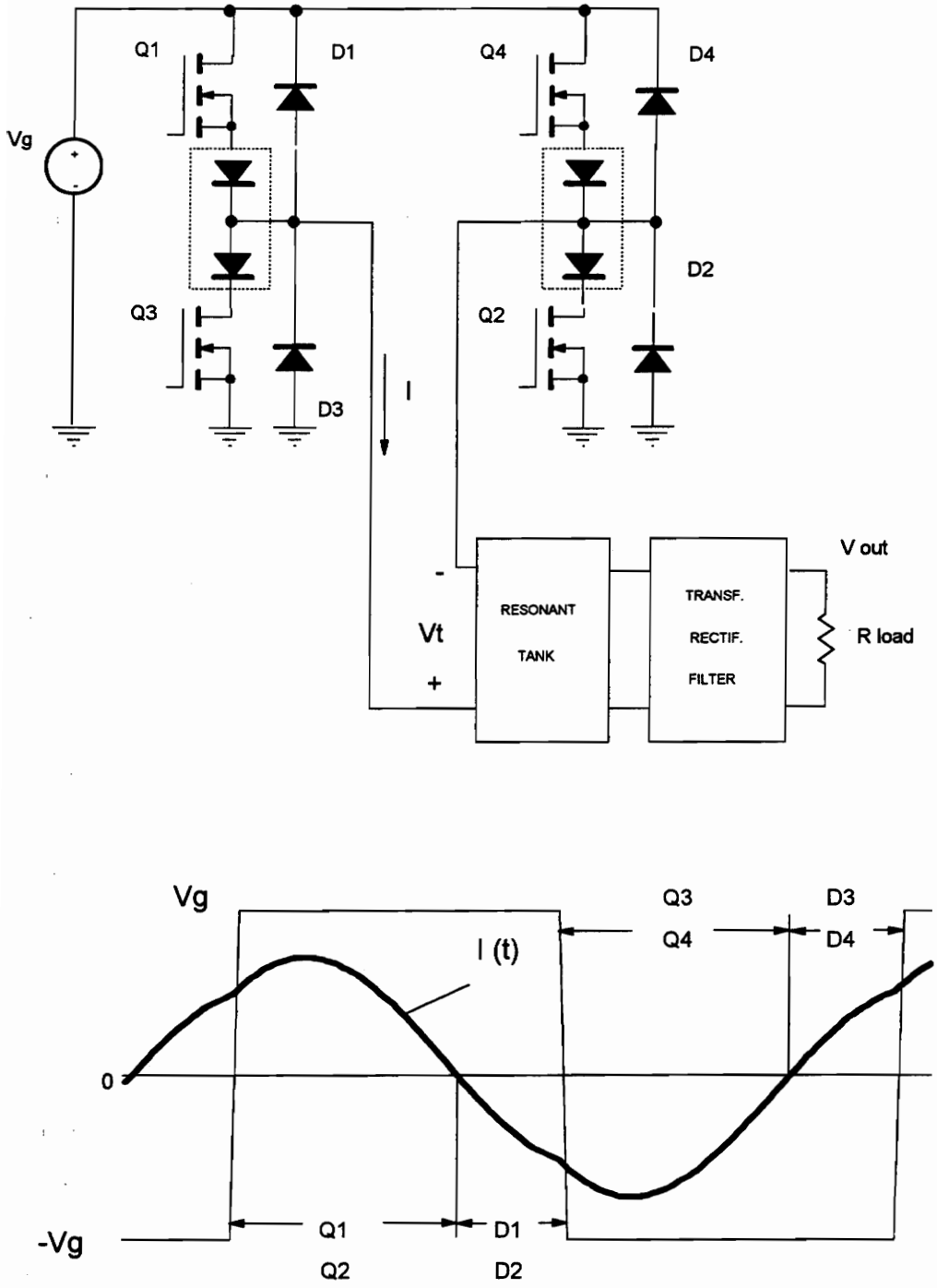


Figure 2.6: ZCS operation of a resonant converter.

2.5 Resonant Converters with Two Reactive Elements

Conventional resonant converters have a resonant network consisting of an inductor and a capacitor. In this section all possible configurations for two element resonant converters will be presented. The definition of resonant converter is going to be used to determine the possible networks. Also the transfer function of each network is provided.

2.5.1 Possible Topologies

The inverter stage acts as a square waveform ac source connected to the resonant network. In the following it will be considered an input ac source (voltage or current) for the resonant network. Using the definitions provided at the beginning of the chapter, in order to operate as a resonant converter the circuit topologies have to comply with the following rules:

- Voltage sources or capacitor loops are not allowed.
- Current sources or inductor cut-sets are not allowed.
- The resonant network has to filter the high-frequency harmonics of the input source.

- The resonant network has to filter the high-frequency harmonics from the load rectifier side.

Also, some components are redundant, namely,

- An inductor in parallel with the input voltage source does not alter the power conversion.
- A capacitor in series with the input voltage source does not alter the power conversion.

Following the former rules, the possible topologies for two-elements resonant converters are depicted in Fig. 2.7. The converters in the left column of Fig. 2.7 are the well-known Series Resonant Converter (SRC) and Parallel Resonant Converter (PRC), the ones in the right column are their duals.

Figure 2.8 shows the possible topologies that do not result in a resonant converter. All three topologies shown in Fig. 2.8 do not filter the high frequency harmonics, and consequently, the sharp edges in the current or the voltage in the rectifier would be seen at the inverter, and vice versa.

The current gain function for the dual SRC and dual PRC are the same as the voltage gain function for the SRC and the PRC.

The two bottom converters in Fig. 2.7 have the same circuit diagram. However, they are different because the output source corresponding to the rectifier-load side of the converter is not an independent source.

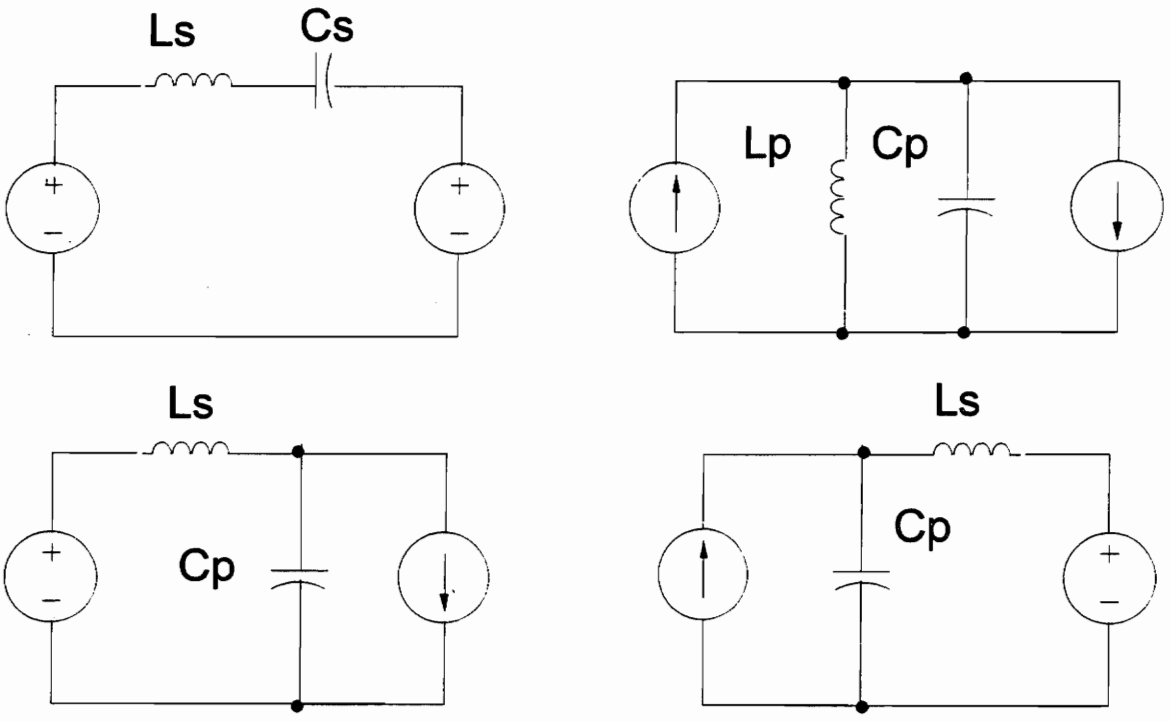


Figure 2.7: Possible resonant networks with two reactive elements.

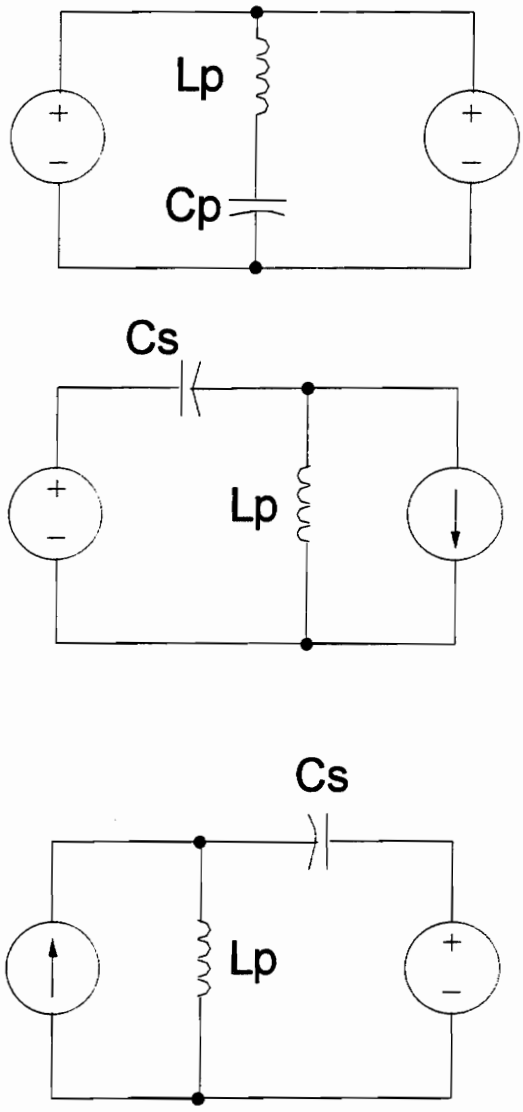


Figure 2.8: Resonant networks with two reactive elements that do not correspond to a resonant converter.

2.6 Design Characteristics for Two-Element Resonant Converters

This section presents a design-oriented analysis of the SRC, and PRC. The objective is not to provide a new analysis method of these resonant converters, but to provide a clear idea of the trade-offs involved in the design of the two converters. This provides a sound way to compare their performance and assess their suitability for different applications.

The design-oriented characteristics presents the stresses in the converter devices and shows their relation to the reactive power involved in the power processing. The soft switching for resonant converters always involves reactive power delivered by the source. This reactive power results in increased conduction losses and larger reactive components. The two converters analyzed have different reactive power requirements to provide soft-switching over the whole operating range. Their relative performance is going to be presented with the help of a design example at the end of the chapter.

The fundamental approximation analysis has the advantage of allowing one to determine the characteristics of the converter as close-form equations. The close form characteristics equations can be easily manipulated to present the characteristics in the best suitable form for the design choices.

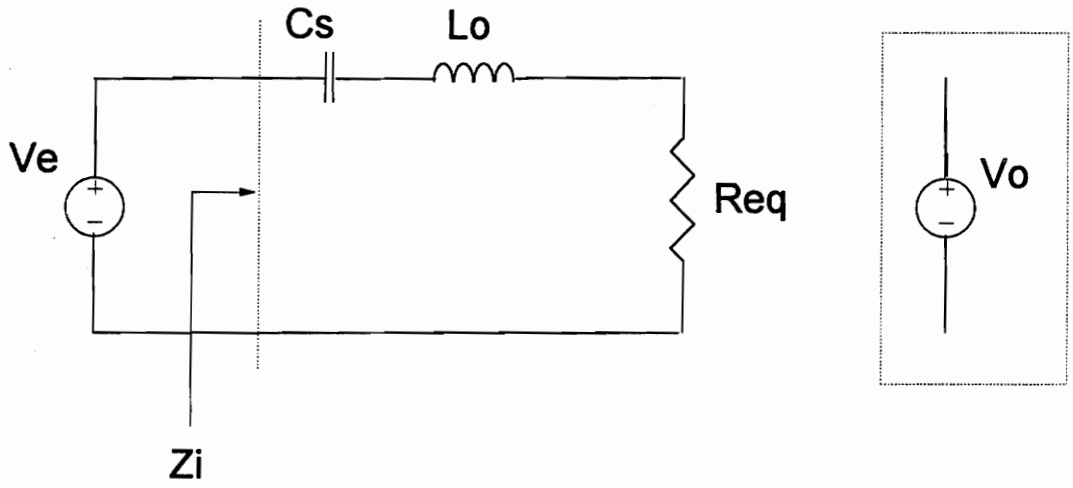


Figure 2.9: Series resonant converter model.

The cumbersome exact method requires extensive computation, and in general the design is based in normalized characteristics that do not provide a clear understanding of the actual values of the voltages and currents until they are denormalized according to the design parameters selected.

2.6.1 Series Resonant Converter

The series resonant converter model is presented in Figure 2.9. The input voltage source to the resonant tank, V_e, is an ac source corresponding to the fundamental of the voltage at the output of the inverter stage. The dependent voltage source corresponding to the rectifier is replaced by a resistor as described in the former section. Using the method of analysis described in the previous section, the voltage gain for the SRC is

$$M_v(\omega_n, Q_s) = \frac{j \cdot \omega_n}{\frac{\pi^2}{8} \cdot Q_s \cdot \left(1 - \omega_n^2\right) + j \cdot \omega_n}, \tag{2.12}$$

normalizing the frequency and impedances with

$$\omega_o = \frac{1}{\sqrt{L_s \cdot C_s}} \quad \text{and} \quad Z_o = \sqrt{\frac{L_s}{C_s}}, \tag{2.13}$$

and defining

$$Q_s = \frac{Z_o}{R_{load}}. \tag{2.14}$$

The results of this analysis are compared with the exact analysis presented in [A-4]. Figure 2.10 presents the voltage gain with respect to the frequency for the exact solution and the fundamental approximation method.

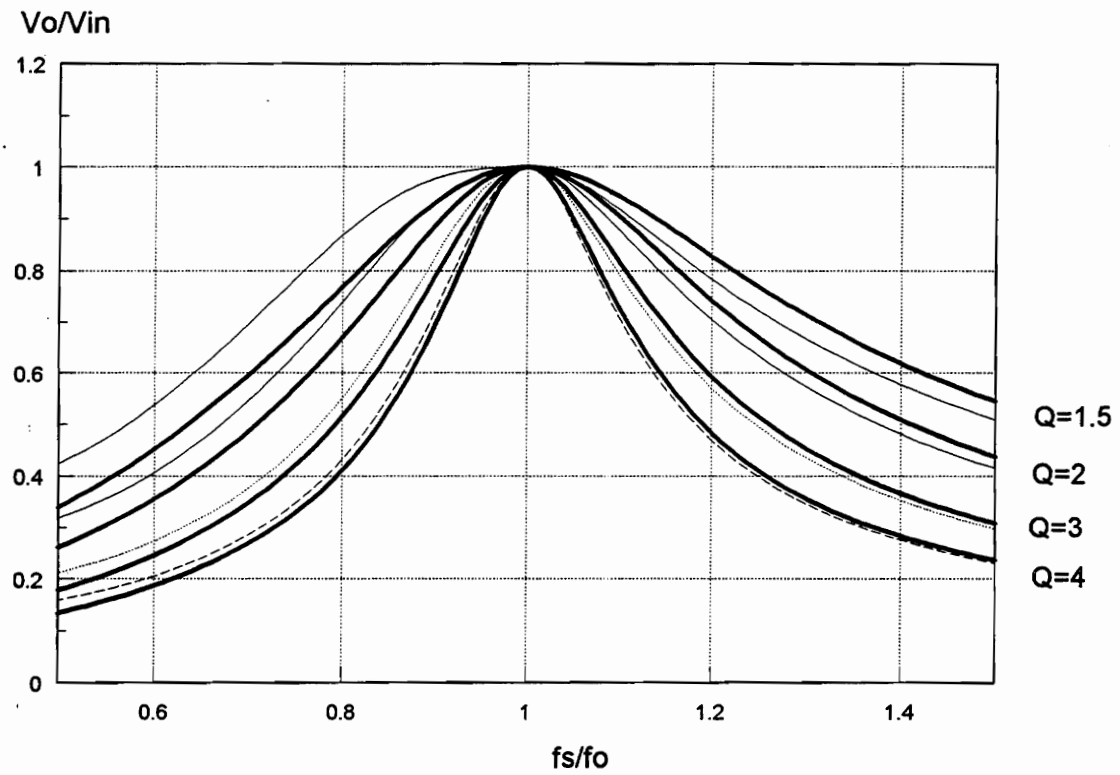


Figure 2.10: Comparison of voltage gain of the SRC obtained with the exact solution (thin lines) with the fundamental approximation analysis result (thick lines).

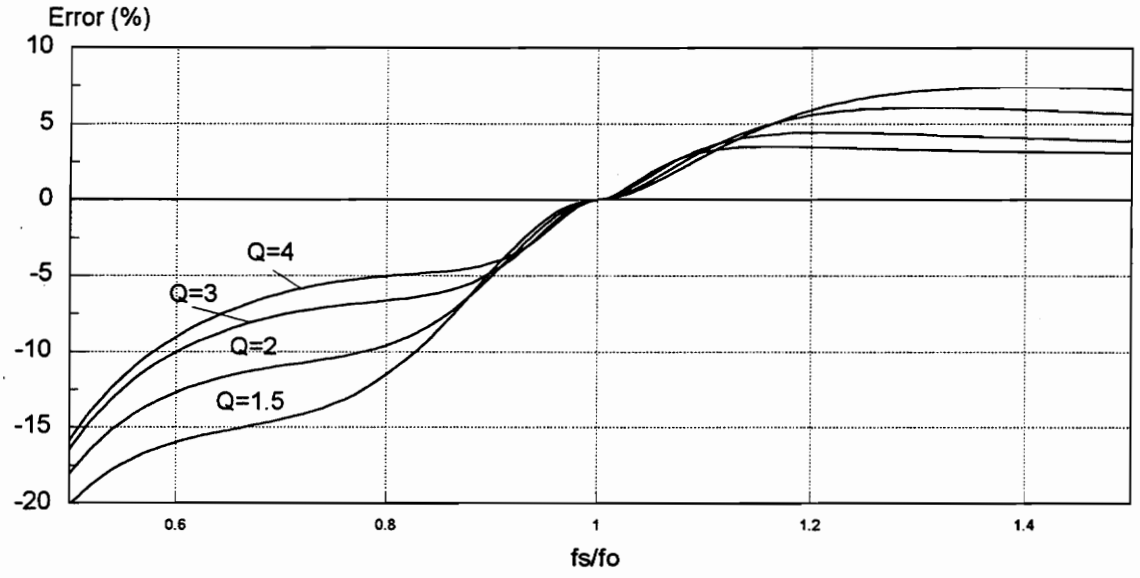


Figure 2.11: Error between the exact analysis and the fundamental approximation analysis for the SRC voltage gain.

Figure 2.11 presents the error with respect to the frequency for different loads. The error is minimal for frequencies of interest around the resonant frequency. Also, the approximated method is more accurate for large Q values. The error is smaller at frequencies above resonance because the high frequency harmonics get more attenuation from the resonant tank characteristics.

The SRC converter behaves as a bandpass filter, with the passband centered at the resonant frequency. The gain in the bandpass is equal to one, independently of the load. The high frequency slope is -20 dB/dec.. This corresponds to the frequency response of a second-order system with a real zero at the origin and a pair of complex conjugate poles at the resonant frequency.

The input impedance to the resonant tank, Z_i , determines the soft-switching characteristics of the SRC. Using the fundamental approximation method, the normalized input impedance to the tank is,

$$Z_i(\omega_n, Q_s) = \frac{\left(1-\omega_n^2\right) + j\cdot\frac{8}{\pi^2}\frac{1}{Q_s^2}\cdot\omega_n}{j\cdot\omega_n} \quad . \tag{2.15}$$

Figure 2.12 shows the plot of the phase of the input impedance. It can be seen that the impedance changes from inductive to capacitive at the resonant frequency, independently of the load. This shows that the converter operates with zero-voltage switching above the resonant frequency, and with zero-current switching below the resonant frequency. If the switches have a significant capacitance compared to the resonant capacitors, operation slightly above resonance is required to achieve ZVS. A

complete analysis of the effect of the switches capacitance on the ZVS limit can be found in Chapter 4.

The rms value of the normalized input current to the tank can be expressed as a function of the normalized input impedance to the tank as

$$I_{in}^{n}(\omega_n, Q_s) = \frac{2\cdot\sqrt{2}}{\pi}\cdot\frac{1}{Z_i(\omega_n, Q_s)} \tag{2.16}$$

Using Eq. (2.12) and Eq. (2.16), the normalized input current to the tank for constant gain can be calculated. Figure 2.13 shows the normalized input current to the tank with respect to the frequency showing the constant gain current. The characteristics show that the current for constant gain changes almost proportionally to the load. This is a good characteristic of the SRC that results in good partial load efficiencies. Also, the characteristics show that a large frequency range is required to keep the voltage gain constant over a load variation.

However, all the characteristics are normalized with respect to parameters that have to be chosen for each specific design. The rms value of the actual input current to the tank can be expressed as

$$I_{in} = I_{in}^{n}\cdot\frac{V_{in}}{Z_o} = I_{in}^{n}\cdot\frac{V_{in}}{n^2\cdot R_{load}}\cdot\frac{n^2\cdot R_{load}}{Z_o} = \frac{V_{in}}{R_{load}}\cdot\frac{I_{in}^{n}}{n^2\cdot Q_s}, \tag{2.17}$$

where n corresponds to the transformer turns ratio required for the design. The transformer turns ratio can be determined from,

$$n = M_v(\omega_n, Q_s)\cdot\frac{V_{in}}{V_{out}}. \tag{2.18}$$

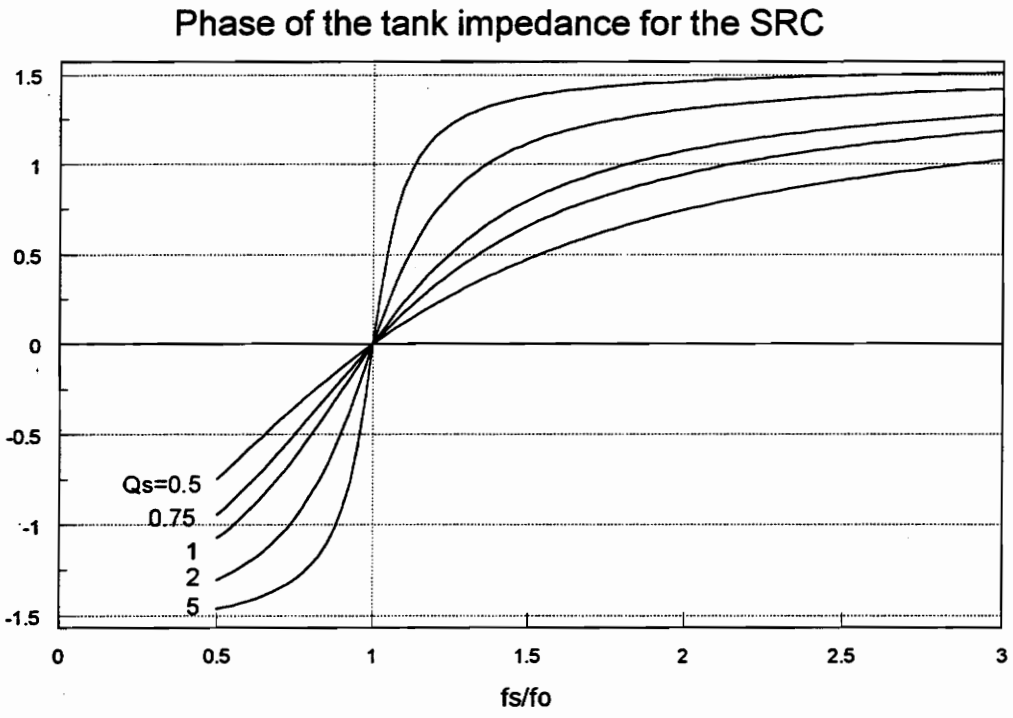


Figure 2.12: Phase of the input impedance to the resonant tank for different loads as a function of frequency.

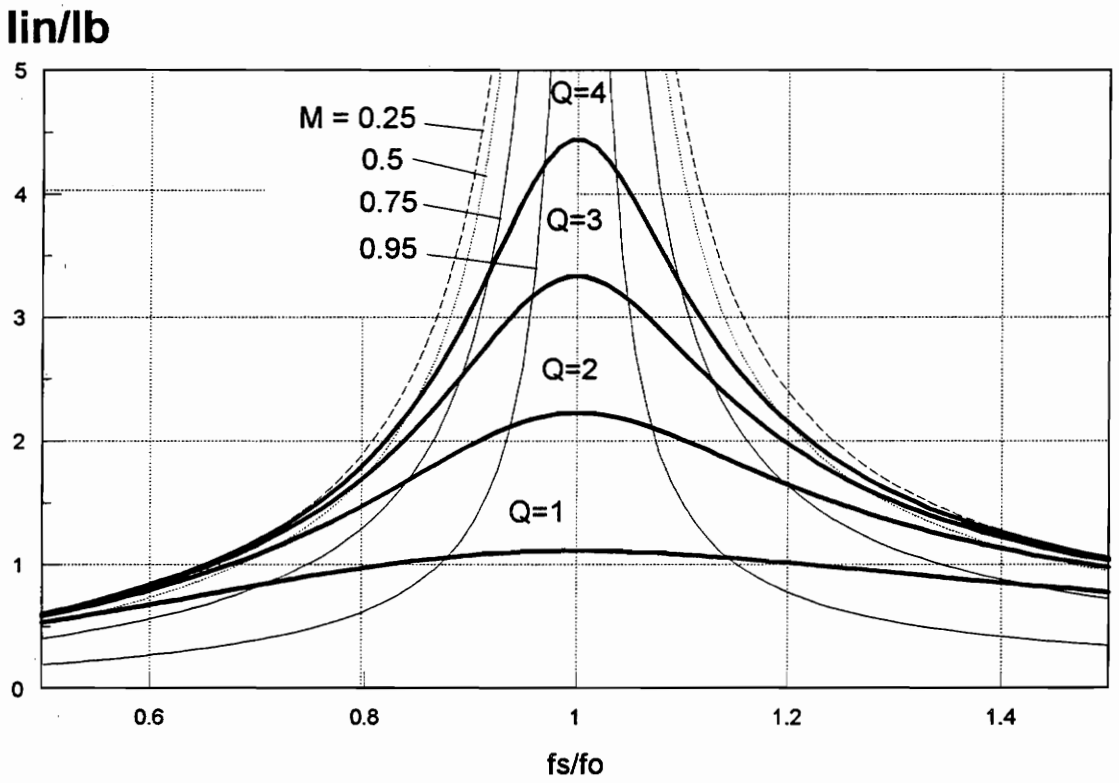


Figure 2.13: Normalized input current to the resonant tank for different loads and constant gain current as a function of frequency.

Putting this in Eq. (2.17),

$$I_{in}(\omega_n, Q_s) = \frac{V_{out}^2}{R_{load} \cdot V_{in}} \cdot \frac{I_{in}^n(\omega_n, Q_s)}{M_v^2(\omega_n, Q_s) \cdot Q_s} \quad . \tag{2.19}$$

The first term of Eq. (2.19) is the output power divided by the input voltage, which corresponds to the minimum current required to provide the output power required from an input-output power balance point of view.

Figure 2.14 shows the plot of the term

$$f(\omega_n, Q_s) = \frac{I_{in}^n(\omega_n, Q_s)}{M_v^2(\omega_n, Q_s) \cdot Q_s} \quad . \tag{2.20}$$

The minimum current through the resonant tank for the SRC occurs at the resonant frequency, and consequently the switching frequency for the design has to be chosen as close to resonance as possible.

Also, from Fig. 2.14 it can be seen that the current required in the tank can be several times the minimum current. This is one of the main problems associated with resonant converters when compared to PWM converters. For PWM converters the rms input current that has to be provided by the inverter is approximately only the output power divided by the input voltage and times the square root of the duty cycle.

The extra current required by the SRC compared to a PWM converter is due to the reactive power that has to be delivered by the inverter. The reactive power to be provided by the inverter can be represented by the power factor of the loaded resonant tank. For the SRC the power factor seen by the inverter is

$$PF_{SRC}(\omega_n, Q_s) = \frac{P_{out}}{S} = \frac{2 \cdot \sqrt{2}}{\pi} M_V(\omega_n, Q_s) \ , \qquad (2.21)$$

where S corresponds to the product of the rms values of the current and the voltage at the input of the resonant tank.

Figure 2.15 shows the power factor at the input of the resonant tank. The graph shows that the power factor is largest at the resonant frequency, and consequently a design operating close to this frequency requires the minimum amount of reactive power.

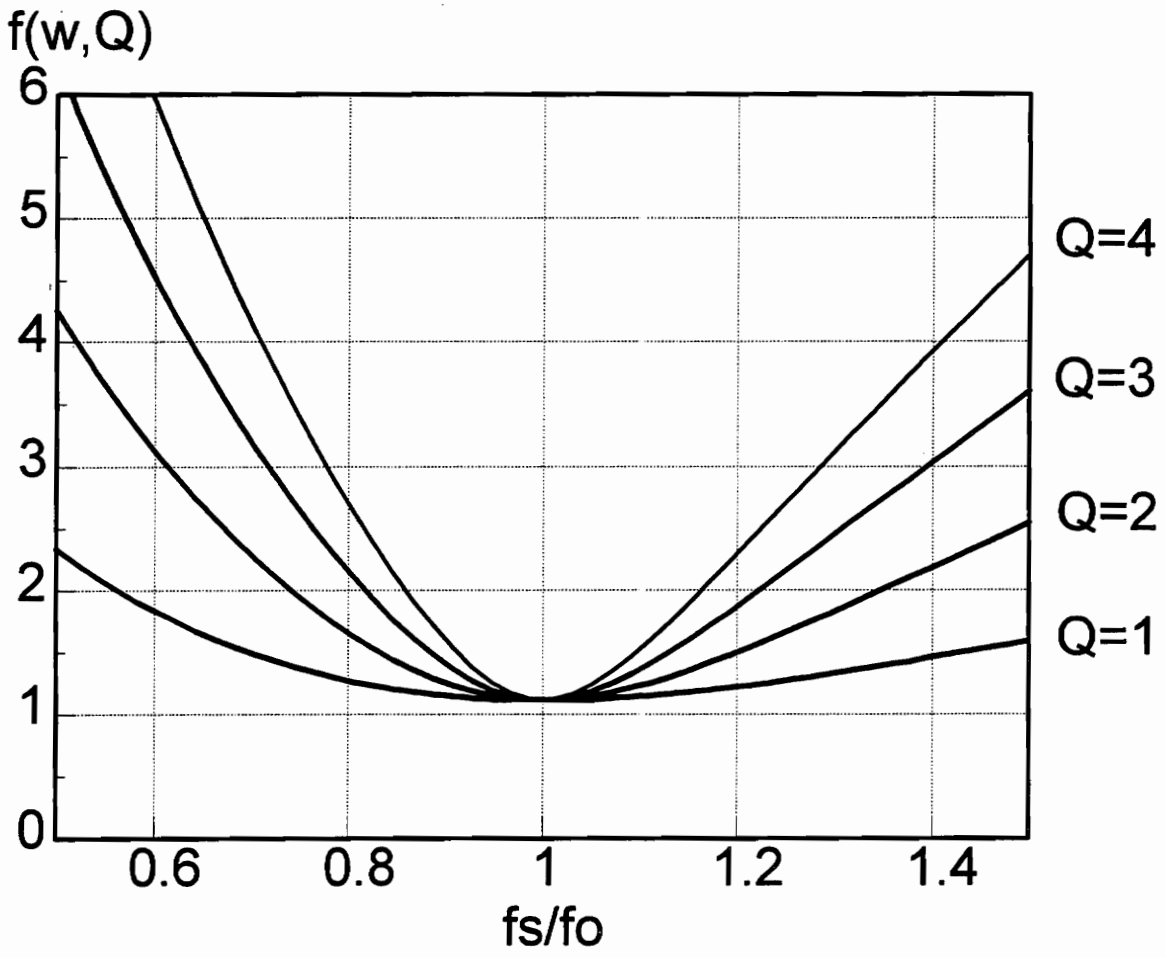


Figure 2.14: Input current to the resonant tank normalized with respect to the output power for different loads as a function of frequency.

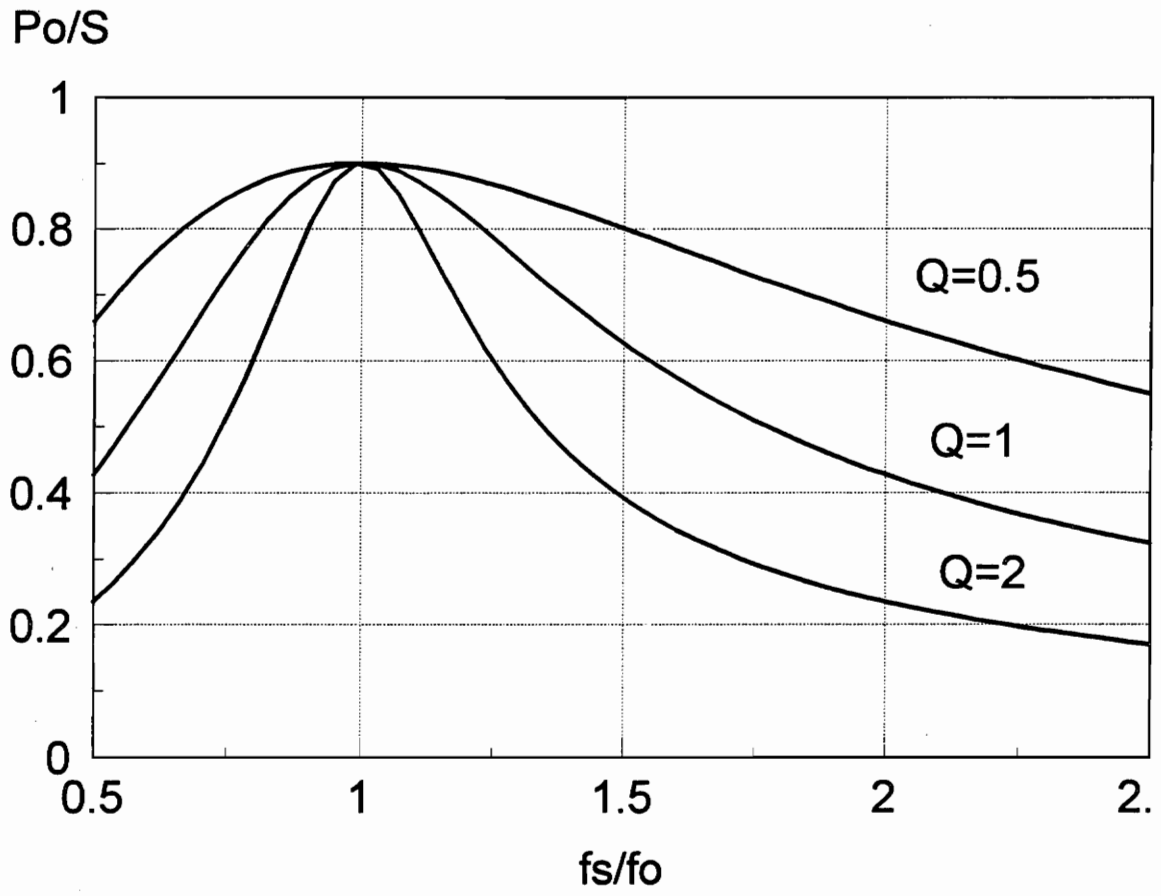


Figure 2.15: Power factor at the input of the resonant tank for different loads as a function of frequency.

2.6.2 Parallel Resonant Converter

The parallel resonant converter model is presented in Figure 2.16. The input voltage source to the resonant tank, V_e, is an ac source corresponding to the fundamental of the voltage at the output of the inverter stage. The dependent voltage source corresponding to the rectifier is replaced by a resistor as described the previous section. Using the method of analysis described in the previous section, the voltage gain for the PRC is,

$$M_v(\omega_n, Q_p) = \frac{Q_p}{\frac{\pi^2}{8} \cdot Q_p \cdot \left(1 - \omega_n^2\right) + j \cdot \omega_n}, \tag{2.22}$$

normalizing the frequency and impedances with,

$$\omega_o = \frac{1}{\sqrt{L_s \cdot C_p}} \quad \text{and} \quad Z_o = \sqrt{\frac{L_s}{C_p}}, \tag{2.23}$$

and defining

$$Q_p = \frac{R_{load}}{Z_o}. \tag{2.24}$$

The results of this analysis are compared with the exact analysis presented in Ref. [A-7]. Figure 2.17 presents the voltage gain with respect to frequency for the exact solution and the fundamental approximation method. Figure 2.18 presents the error with respect to the frequency for different loads. The error is minimal around the resonant frequency, and remains small for large values of Q and at high frequencies.

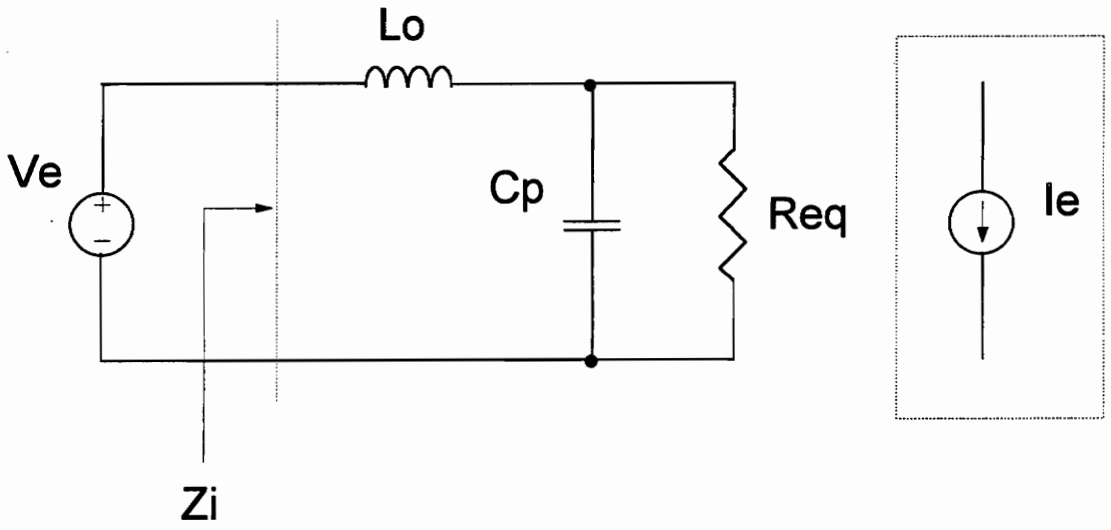


Figure 2.16: Parallel resonant converter model.

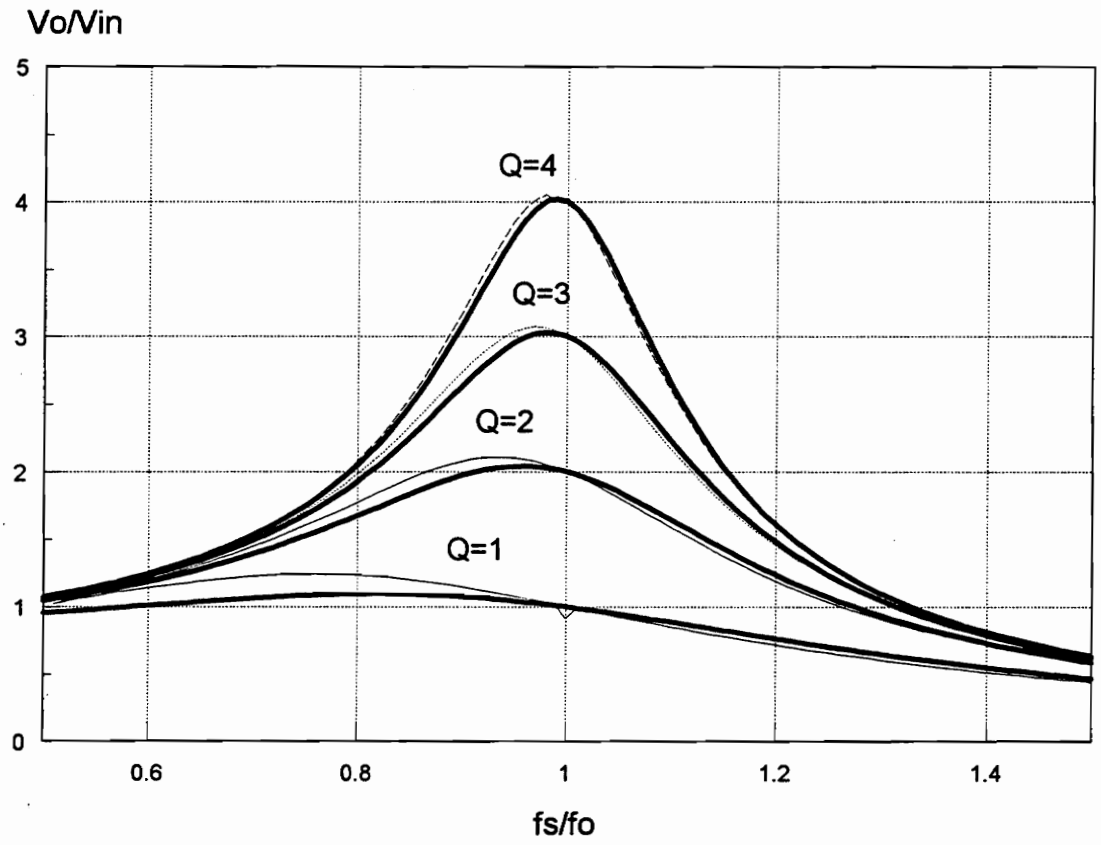


Figure 2.17: Comparison of voltage gain of the PRC obtained with the exact solution (thin lines) with the fundamental approximation analysis result (thick lines).

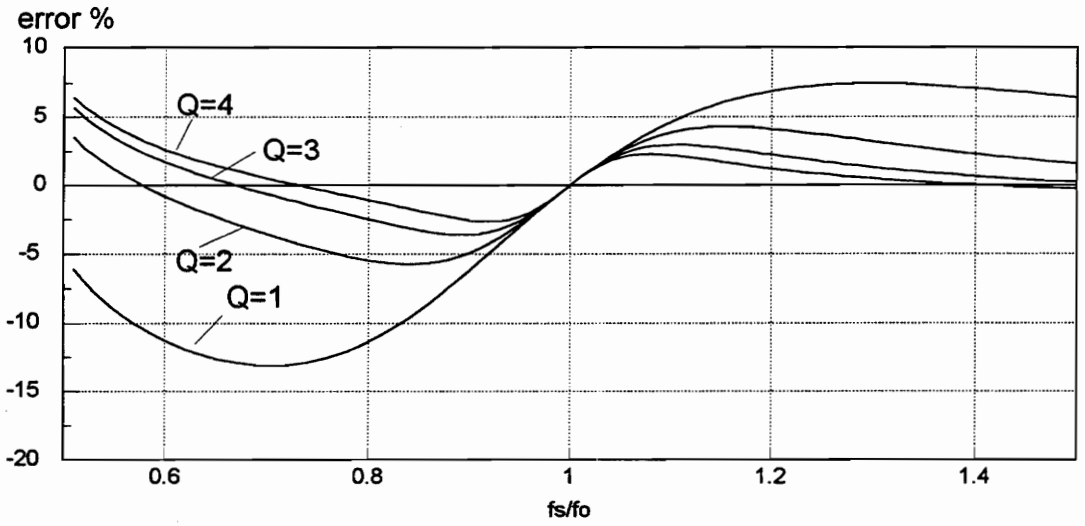


Figure 2.18: Error between the exact analysis and the fundamental approximation analysis for the PRC voltage gain.

The PRC behaves as a lowpass filter with the corner frequency at the resonant frequency. Since the gain function has a pair of complex conjugate poles the amplitude of the gain at the corner frequency depends on the load. The region of the characteristic with practical use is actually the region where the gain is load dependent, around the corner frequency, because it is where the reactive power is minimal. The high frequency slope is -40 dB/dec..

The input impedance to the resonant tank, Z_i, determines the soft switching characteristics of the PRC. Using the fundamental approximation method, the normalized input impedance to the tank is

$$Z_i(\omega_n, Q_s) = \frac{\left(1-\omega_n^2\right)\cdot\frac{\pi^2}{8}\cdot Q_p + j\cdot\omega_n}{1+j\cdot\omega_n\cdot\frac{\pi^2}{8}\cdot Q_p} \quad . \tag{2.25}$$

Figure 2.19 shows the plot of the phase of the input impedance. It can be seen that the impedance changes from inductive to capacitive at a frequency dependent on the load. The frequency limit between ZVS operation and ZCS operation corresponds to the peak of the voltage gain. The peak gain frequency is

$$\omega_n = \sqrt{1-\frac{1}{Q_p^2}} \tag{2.26}$$

The parasitic switch capacitance modifies the frequency of operation required to achieve ZVS. A complete analysis of the effect of the switches capacitance on the ZVS limit can be found in Chapter 4.

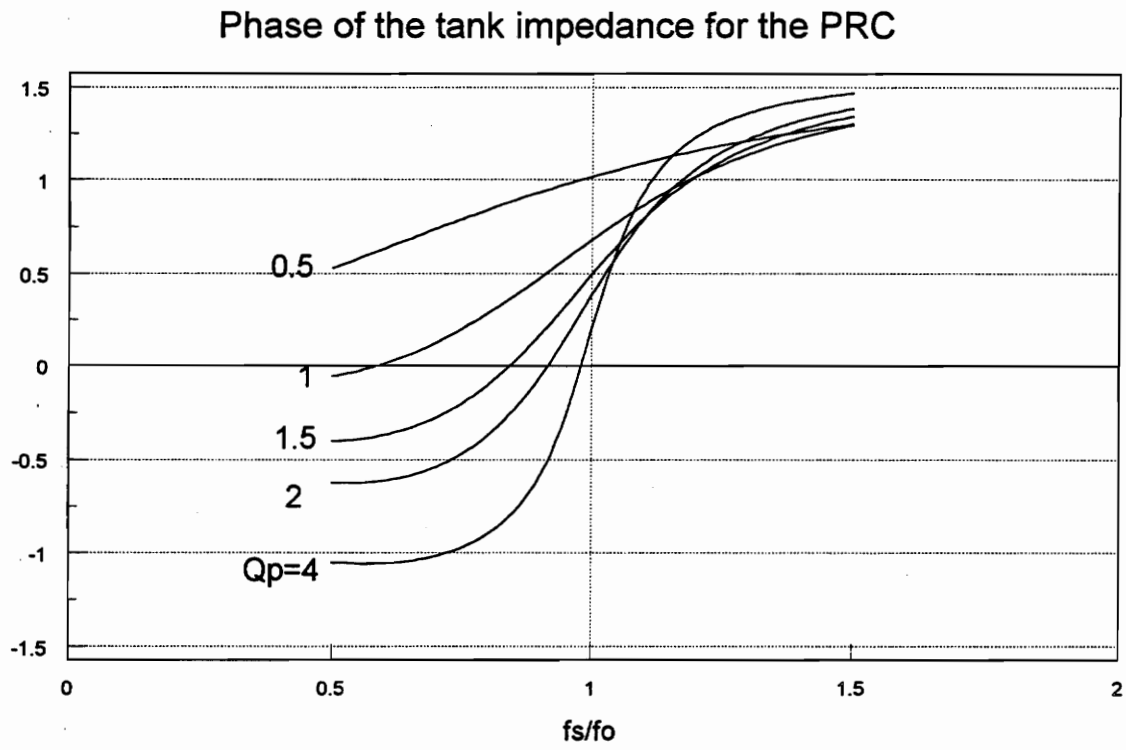


Figure 2.19: Phase of the input impedance to the resonant tank for different loads as a function of frequency.

The rms value of the normalized input current of the tank can be expressed as a function of the normalized input impedance to the tank as,

$$I_{in}^{n}(\omega_n, Q_p) = \frac{2 \cdot \sqrt{2}}{\pi} \cdot \frac{1}{Z_i(\omega_n, Q_p)} \tag{2.27}$$

Using Eq. (2.22) and Eq. (2.27), the normalized input current to the tank for constant gain can be calculated. Figure 2.20 shows the normalized input current to the tank with respect to the frequency showing the constant gain current. The characteristics show that the current for constant gain remains almost constant when the load changes. Also, the characteristics show that a smaller frequency range than in the SRC case is required to keep the voltage gain constant over a load range variation.

The rms value of the actual input current to the tank can be expressed as,

$$I_{in}(\omega_n, Q_p) = \frac{V_{out}^2}{R_{load} \cdot V_{in}} \cdot \frac{I_{in}^{n}(\omega_n, Q_p) \cdot Q_p}{M_v^2(\omega_n, Q_p)} \tag{2.28}$$

Figure 2.21 shows the plot of the term

$$f(\omega_n, Q_p) = \frac{I_{in}^{n}(\omega_n, Q_p)}{M_v^2(\omega_n, Q_p) \cdot Q_p} \tag{2.29}$$

The minimum current through the resonant tank for the PRC corresponds to the frequency at which the maximum gain occurs for each Q. Consequently, the minimum switching frequency should be chosen as close as possible to the peak voltage gain.

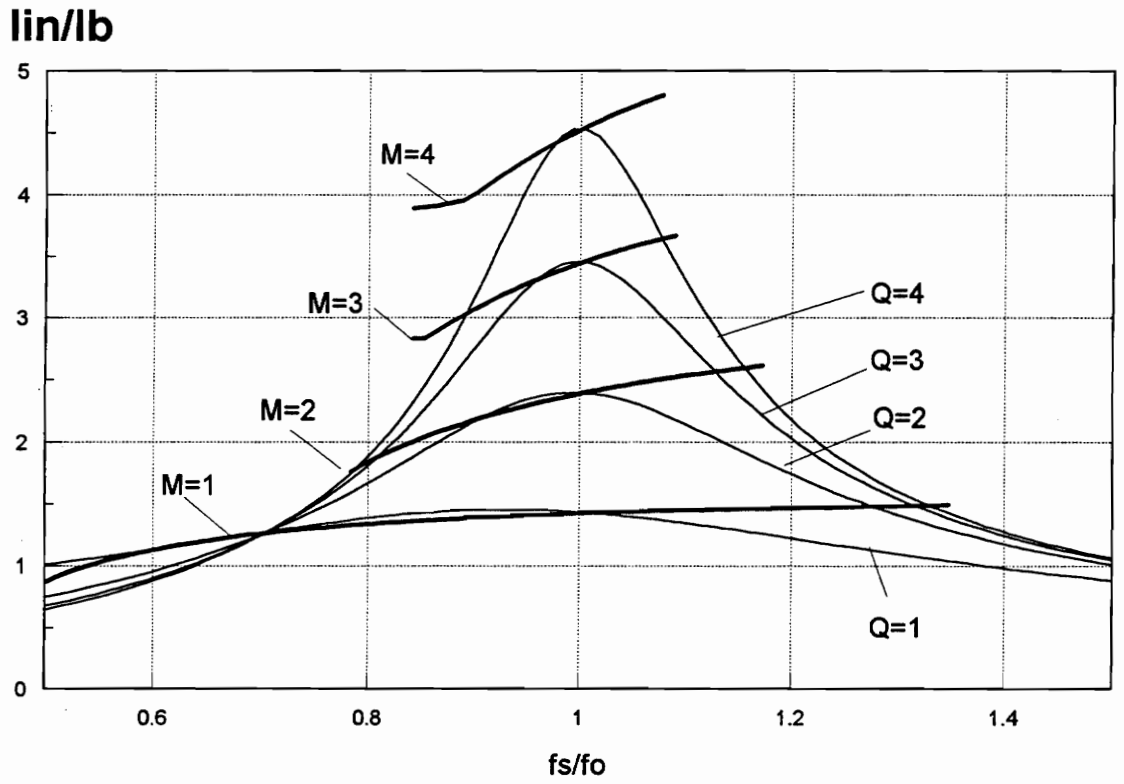


Figure 2.20: Normalized input current to the resonant tank for different loads and constant gain current as a function of frequency.

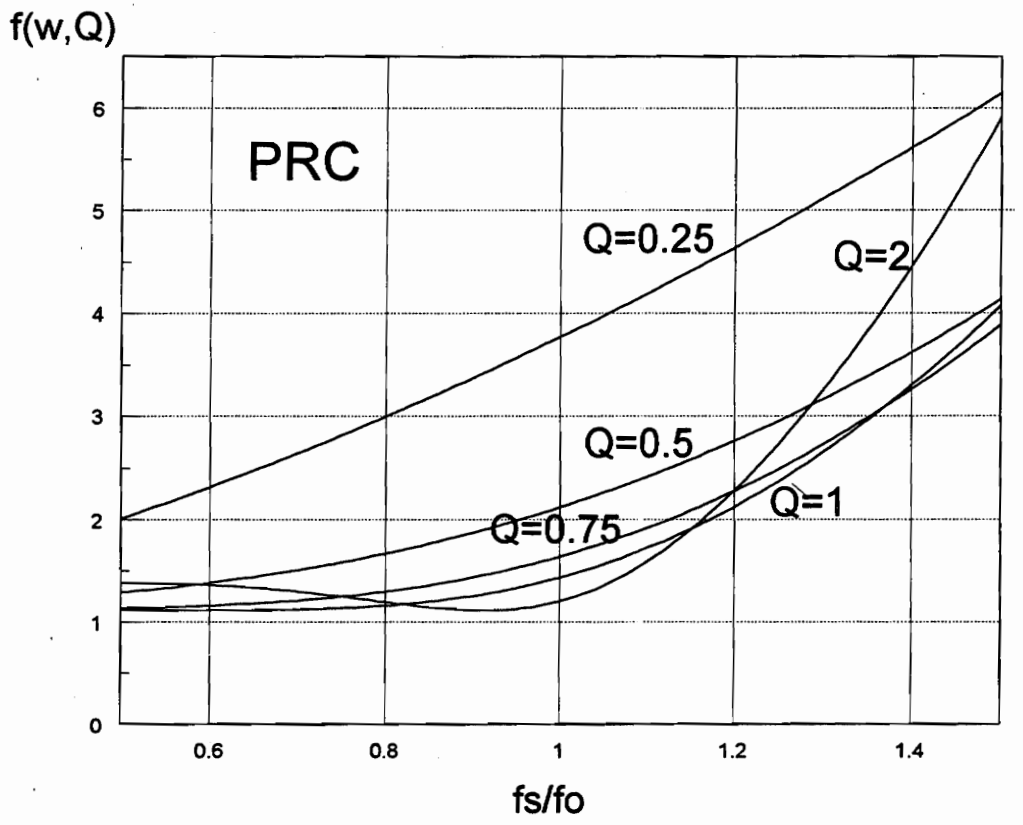


Figure 2.21: Input current to the resonant tank normalized with respect to output power for different loads as a function of frequency.

The behavior with respect to the load, Q, shows that for Q values lower than 1 the input current increases. The minimum values of Q should be selected equal to one or larger. However, the lower the Q value is, the larger is the frequency range required for regulation. The frequency range required increases dramatically for values of Q equal to one and lower.

An important difference with respect to the SRC is that the input current to the resonant tank is always larger for ZVS operation than for ZCS operation. This is because the reactive power required by the tank is larger for ZVS operation. ZVS requires operation above resonance, and for those frequencies the impedance of the capacitor in parallel with the load has lower impedance, and consequently, the circulating current is larger at higher frequencies.

Figure 2.21 shows that the current required in the tank can be several times the minimum current. The reactive power to be provided by the inverter can be represented by the power factor of the loaded resonant tank. For the PRC the power factor seen by the inverter is,

$$PF_{PRC}(\omega_n, Q_p) = \frac{P_{out}}{S} = \frac{\pi}{2\cdot\sqrt{2}} M_v(\omega_n, Q_p) \cdot \frac{1}{1 + j\cdot\omega_n \cdot \frac{\pi^2}{8}\cdot Q_p} \qquad (2.30)$$

where S corresponds to the product of the rms values of the current and the voltage at the input of the resonant tank.

Figure 2.22 shows the power factor at the input of the resonant tank. The reactive power required for the tank is lower below the peak voltage gain frequency, and is minimal for Q=1.

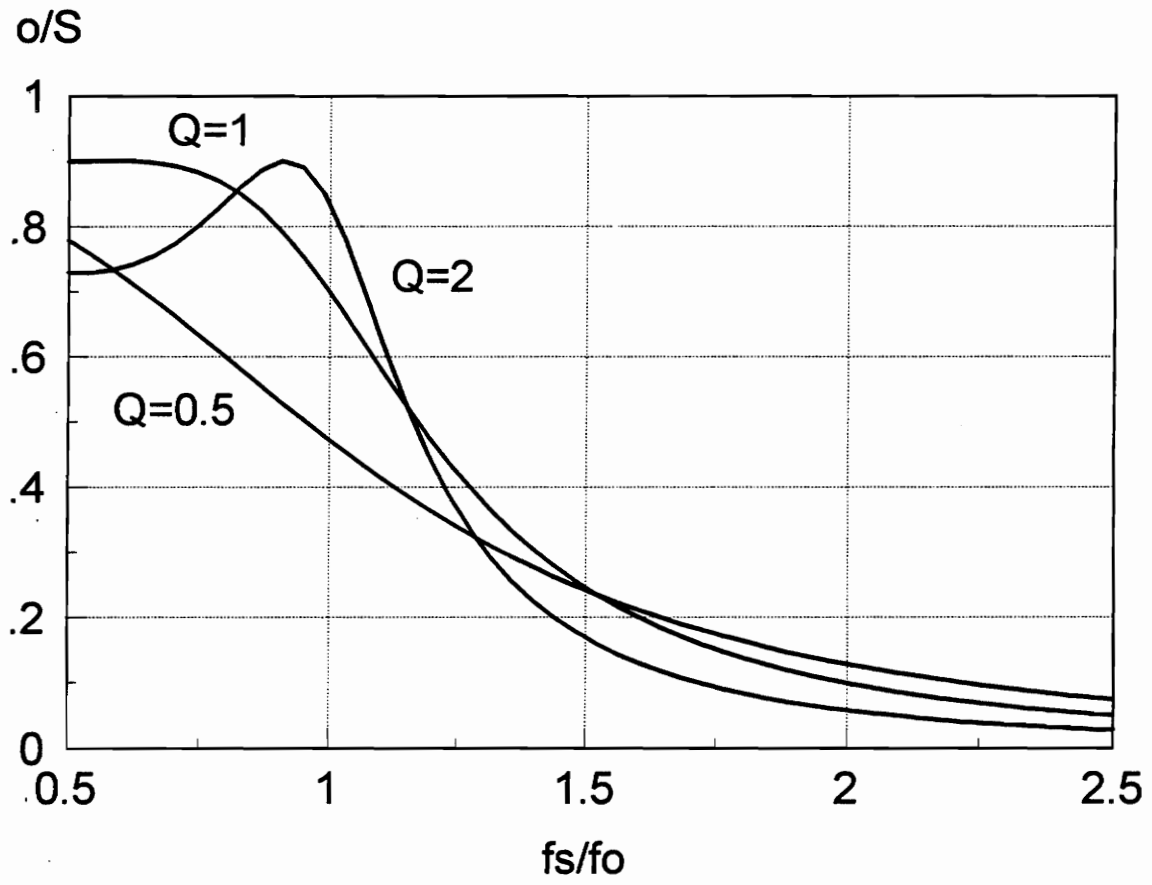


Figure 2.22: Power factor at the input of the resonant tank for different loads as a function of frequency.

2.7 Resonant Converters with Three Reactive Elements

Since power regulation and soft switching for resonant converters can be achieved with only two reactive elements, the addition of more resonant components may seem initially undesirable. However, in some cases the additional reactive elements are already present in the circuit as parasitics, with capacitance or inductance values comparable to the resonant elements, changing the resonant converter characteristics. Also, in some cases the additional elements are added to modify the characteristics of the converters in a desirable way, without significantly increasing the size and cost of the converter, giving the designer an added choice to achieve the desired conversion characteristics. This has motivated the exhaustive search of topologies with three resonant elements, in order to determine their properties.

The number of possible topologies with three resonant components is considerably larger than the number with two elements, requiring a more systematic way to determine all the possibilities. In the next section an exhaustive search of the possible three element networks is presented. Also, the diversity of voltage and current gains for all the topologies found are given in a table.

2.7.1 Possible Topologies with Three Elements

The three reactive elements can be arranged in two possible modes, either forming a T network or a Π network. Figure 2.23 shows the two possibilities with a table

showing the possible placement of the reactances. The placement of a reactance is marked on the table as X, a short is marked as S, and an infinite inductance or open circuit is marked as O. The possibility of an open circuit in the B position is excluded for the Π-network case because it disconnects the input and the output. Also, the case of a short in the b position for the T-networks is excluded for the same reason.

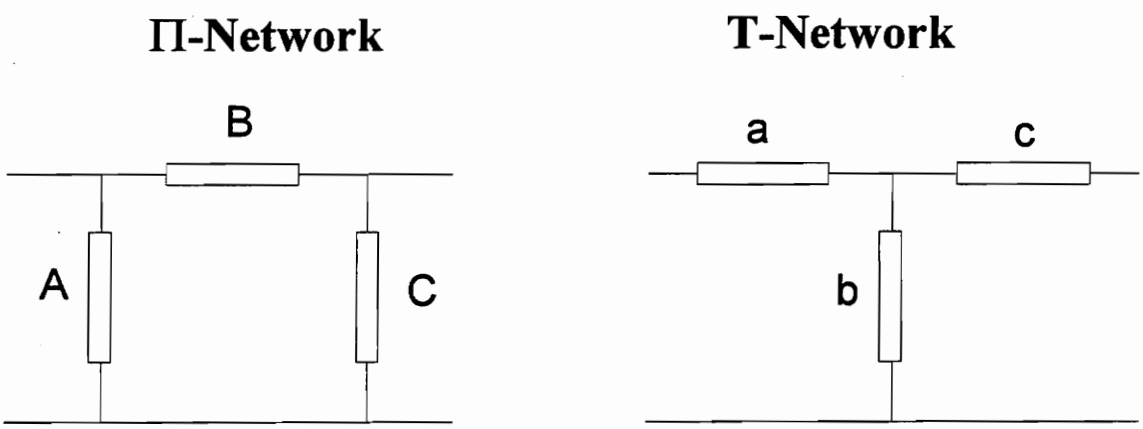
Networks T1 and Π1 are only a wire connection and do not contain reactive elements; consequently, they are discarded. The rest correspond to only five different possibilities,

- Series Network: Cases Π3, T2, T5, and T6 correspond to having a series-parallel combination of the three elements in series between input source and the load.

- Parallel Network: Cases Π2, Π5, Π6, and T3 correspond to having a series-parallel combination of the three elements in parallel with the input source and the load.

- Series-Parallel Networks: Cases Π4, Π7, T4, and T7 correspond to having a reactive network or element in series between input and load, and a reactive network or element in parallel with the input source or the load.

- Π-Network: Case Π8 corresponds to having three single reactive elements in a Π-network arrangement.



Π	A	B	C
1	O	S	O
2	O	S	X
3	O	X	O
4	O	X	X
5	X	S	O
6	X	S	X
7	X	X	O
8	X	X	X

T	a	b	c
1	S	O	S
2	S	O	X
3	S	X	S
4	S	X	X
5	X	O	S
6	X	O	X
7	X	X	S
8	X	X	X

Figure 2.23: Possible resonant networks with three reactive elements.

- T-Network: Case T8 corresponds to having three single reactive elements in a T-network arrangement.

Tables 2.1 and 2.2 show all the possibilities, indicating the source type at input and output to have a resonant converter. A description of the rule not fulfilled by the networks which do not result in a resonant converter is also indicated in the table.

The number of possible topologies is 26. These topologies can be grouped in terms of input-output supplies in three groups:

- Converters with input voltage and output voltage, or input current and output current, that are symmetrical, *i.e.* interchanging input and output sides results in the same converter. Figure 2.24 shows the four topologies that fit this description. The converters in the left column are the duals of the converters in the right column.

- Converters with input voltage and output voltage, or input current and output current, that are not symmetrical. Two different converters are obtained for each of the resonant networks of these type, depending on which side is considered input. Figure 2.25 shows the resulting converters. The converters in the left column are the duals of the converters in the right column.

- Converters with input voltage and output current, or vice versa. For each of the corresponding resonant networks two converters are possible depending on which side is considered input. Figure 2.26 shows the resulting converters. Also, the converters in the left column are the duals of the converters in the right column.

Table 2.1: Possible Three-Elements Topologies I

Network type	Position			Input	Output	Comments
	A	B	C			
Series Network		L+(C//L)		Voltage	Voltage	
Π3, T2, T5, T6		L//(C+L)		Voltage	Voltage	
		C+(C//L)				Not low pass filter
		C//(L+C)				Not low pass filter
Parallel Network		L+(C//L)				Not low pass filter
Π2, Π5, Π6, T3		L//(C+L)				Not low pass filter
		C+(C//L)		Current	Current	
		C//(L+C)		Current	Current	
Series-Parallel		L	C//L	Voltage	Current	
Network		L	C+L	Voltage	Voltage	
Π4, Π7, T4, T7		C	C//L	Current	Current	
		C	C+L			Not low pass filter
	C//L	L		Current	Voltage	
	C+L	L		Voltage	Voltage	
	C//L	C		Current	Current	
	C+L	C				Not low pass filter
	L	C//L				Not low pass filter
	L	C+L		Voltage	Voltage	
	C	C//L		Current	Current	
	C	C+L		Current	Voltage	
		C//L	L			Not low pass filter
		C+L	L	Voltage	Voltage	
		C//L	C	Current	Current	
		C+L	C	Voltage	Current	

Table 2.2: Possible Three-Elements Topologies II

Network type	Position			Input	Output	Comments
	A	B	C			
Π-Network	L	L	L			Not low pass filter
Π8	L	L	C	Voltage	Current	
	L	C	L			Not low pass filter
	L	C	C	Current	Current	
	C	L	L	Current	Voltage	
	C	L	C	Current	Current	
	C	C	L	Current	Current	
	C	C	C			Not low pass filter
T-Network	L	L	L			Not low pass filter
T8	L	L	C	Voltage	Voltage	
	L	C	L	Voltage	Voltage	
	L	C	C	Voltage	Current	
	C	L	L	Voltage	Voltage	
	C	L	C			Not low pass filter
	C	C	L	Current	Voltage	
	C	C	C			Not low pass filter

Table 2.3 presents the gain for each of the converters. Table 2.4 shows the values of the constants used in the equations in Table 2.3 for each converter, using the notation of Figs. 2.24 to 2.26, and the following definitions:

For converters with 2 C and 1 L:

$$\omega_o = \frac{1}{\sqrt{L \cdot C_{eq}}}, \tag{2.31}$$

$$Z_o = \sqrt{\frac{L}{C_{eq}}}, \tag{2.32}$$

$$C_{eq} = \frac{C_1 \cdot C_2}{C_1 + C_2}, \tag{2.33}$$

$$C_n = \frac{C_1}{C_2}, \tag{2.34}$$

$$K_o^C = 1 + C_n, \tag{2.35}$$

$$K_1^C = \frac{1 + C_n}{C_n}. \tag{2.36}$$

For converters with 2 L and 1 C:

$$\omega_o = \frac{1}{\sqrt{L_{eq} \cdot C}}, \tag{2.37}$$

$$Z_o = \sqrt{\frac{L_{eq}}{C}}, \tag{2.38}$$

$$L_{eq} = \frac{L_1 \cdot L_2}{L_1 + L_2}, \tag{2.39}$$

$$L_n = \frac{L_1}{L_2}, \tag{2.40}$$

$$K_0^L = 1 + L_n \,, \tag{2.41}$$

$$K_1^L = \frac{1+L_n}{L_n} \,, \tag{2.42}$$

and normalizing the load

$$Q_S = \frac{Z_o}{R_{eq}} \,, \text{ or} \tag{2.43}$$

$$Q_p = \frac{R_{eq}}{Z_o} \,. \tag{2.44}$$

Table 2.5 summarizes the main properties of the three-elements topologies. According to the frequency of the gain, the converters can be grouped into two main categories:

- Bandpass filter characteristic. They have a load independent gain at the middle of the pass-band. The SRC is the corresponding two-element resonant converter with bandpass characteristics.

- Lowpass filter characteristic. They have a low frequency gain of one. The PRC is the corresponding two-element resonant converter with lowpass characteristics.

However, the association with SRC or PRC characteristics have to be taken into consideration also if there is overshoot in the voltage gain for high-Q loads, as is the case for the PRC. The peaking in the characteristics for high-Q values, as in the case of the PRC for frequencies around ω_0, determines the characteristics of the converter. The high frequency roll-off slope determines the high frequency harmonics contents of the output,

and is consequently a more important magnitude for inverter applications when a sinusoidal output is required.

Figures 2.27 and 2.28 show the gain characteristics for the converters with "SRC-type" voltage gain, all of them with a high frequency roll-off frequency of -20 dB/dec.. Figures 2.29 to 2.31 show the converters with "PRC-type" voltage gain, all of them show peaking dependent on the load (Q).

An interesting case is the LCC converter, designated in the list as 7d(r). This converter has a bandpass characteristic and a -40 dB/dec. roll-off slope at high frequencies. It also has a load-independent gain at the bandpass frequency (resonance of the LC series), but it has peaking in the voltage gain like the PRC.

In the next sections the performance and design characteristics of the LCC are addressed, and they will be used in the comparison with SRC, and PRC designs at the end of the chapter. The effects of the peaking in the characteristics and the bandpass behavior are analyzed in terms of device stresses and reactive power. This analysis will help to match the characteristics of the three-elements resonant converters presented with a specific desired performance.

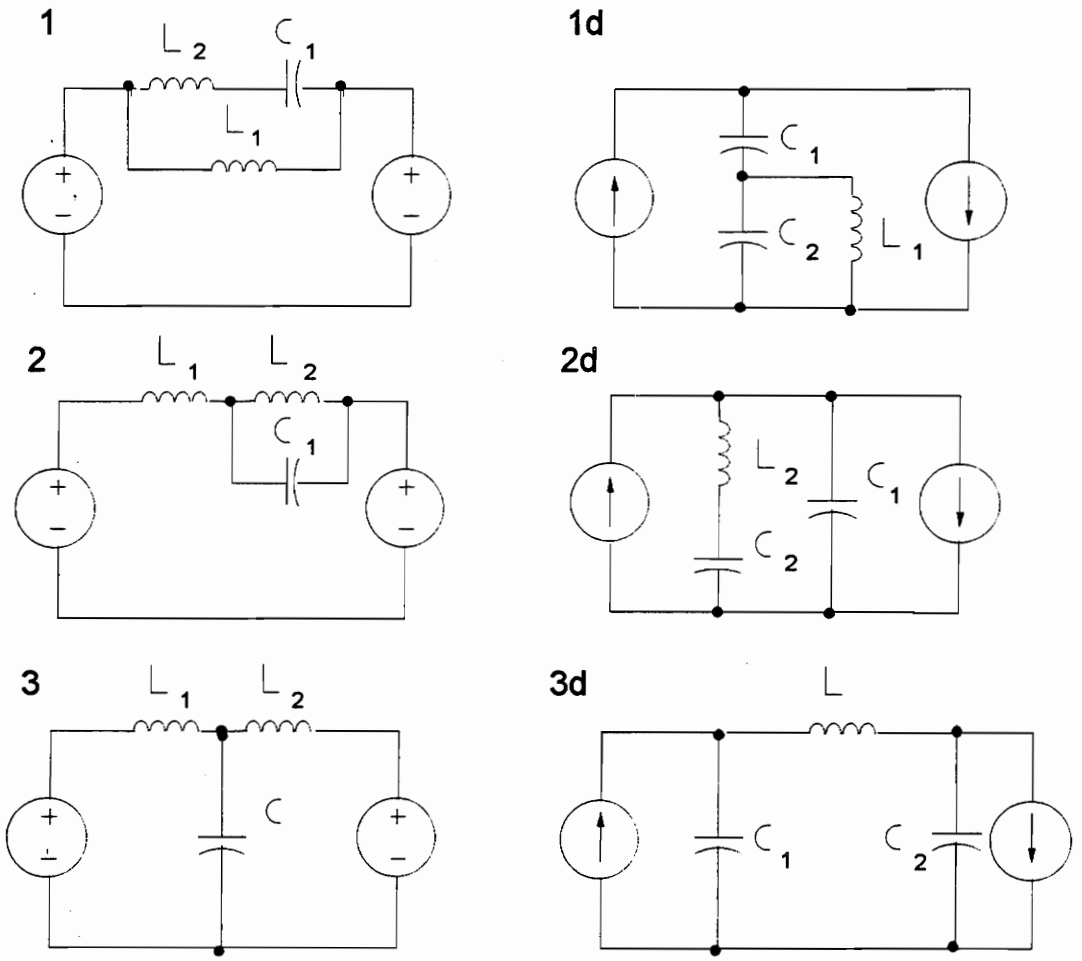


Figure 2.24: Topologies with in/out symmetry.

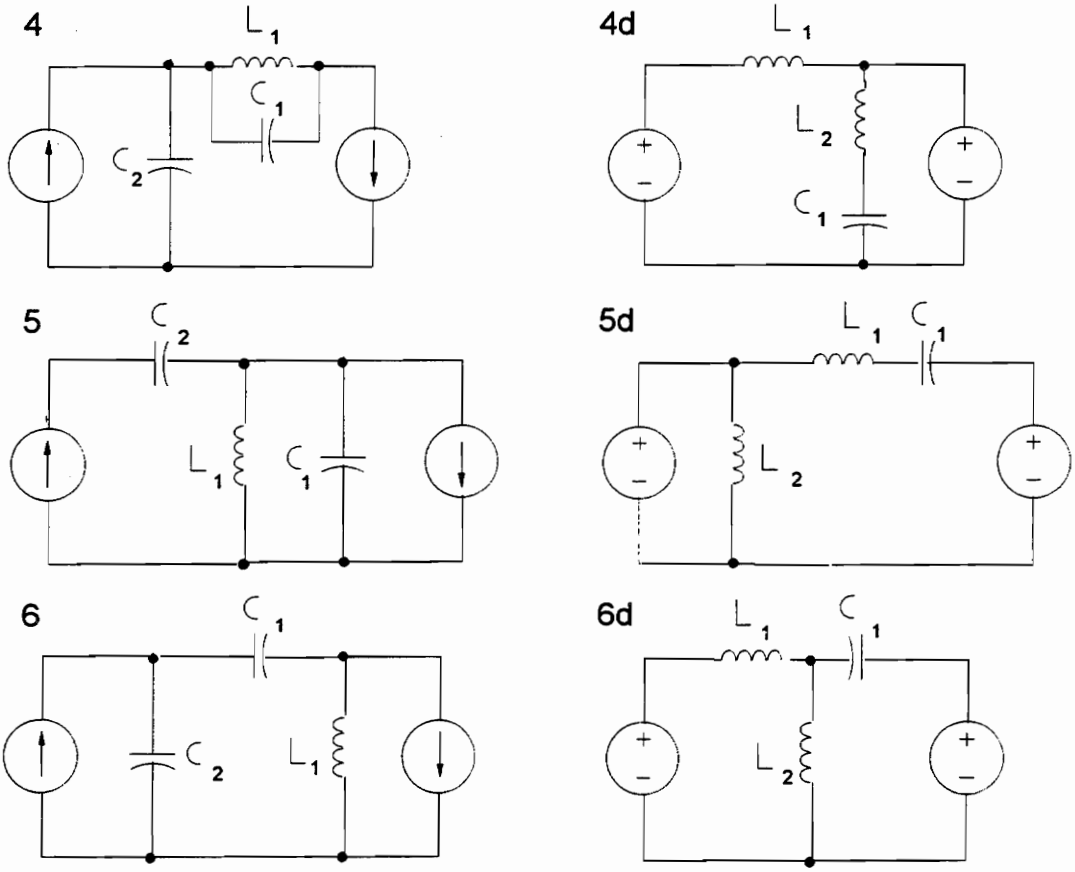


Figure 2.25: Topologies without in/out symmetry.

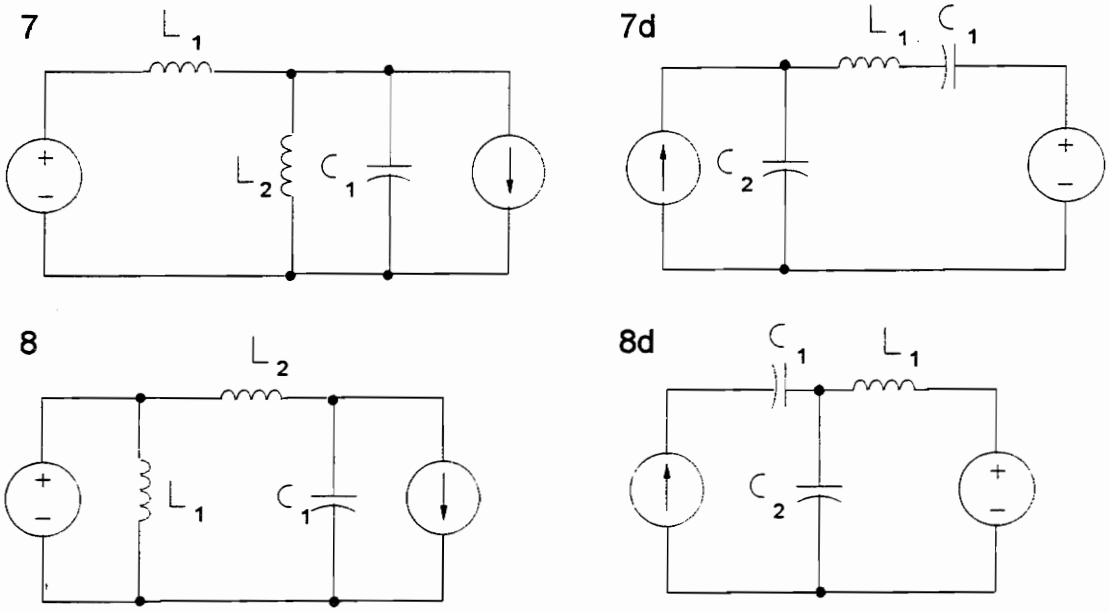


Figure 2.26: Topologies with different input and output sources.

Table 2.3: Gain Functions of Three-Elements Resonant Converters I

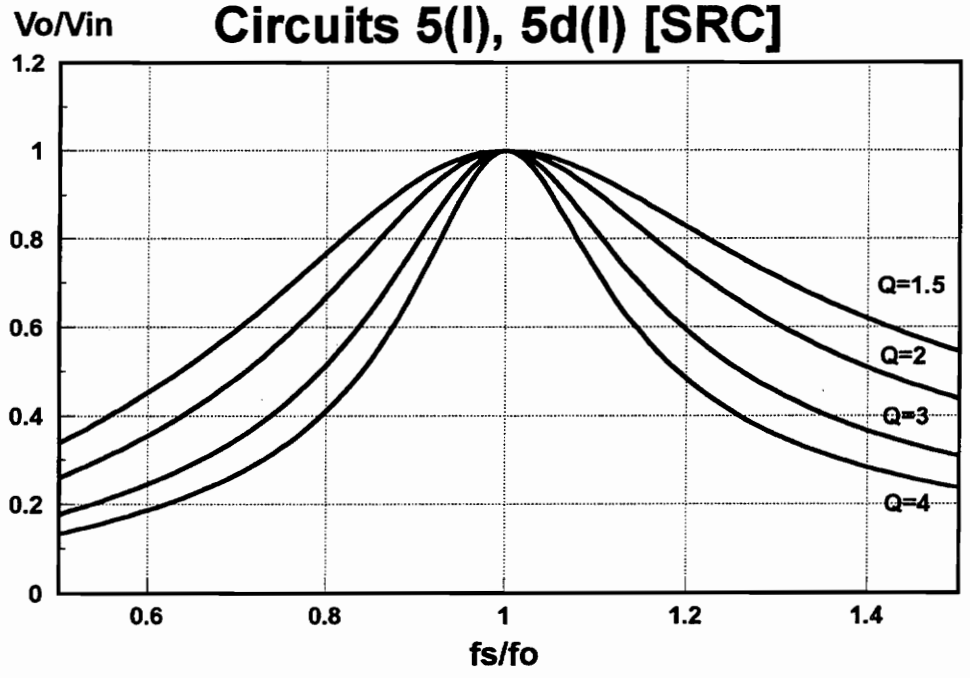
Circuits	Gain	Zeros
1, 1d, 2, 2d, 4, 4d(l)	$\frac{\left(1-\omega_n^2\cdot K_n\right)}{\left(1-\omega_n^2\cdot K_{d1}\right)-j\omega_n\cdot Q\cdot K_{d2}\cdot\left(1-\omega_n^2\cdot K_{d3}\right)}$	$\omega_z=\frac{1}{\sqrt{K_n}}$ $\omega_z=\infty$
3, 3d	$\frac{1}{\left(1-\omega_n^2\cdot K_{d1}\right)+j\omega_n\cdot Q\cdot K_{d2}\cdot\left(1-\omega_n^2\right)}$	$\omega_z=\infty$
4(r), 4d(r)	$\frac{Q}{Q+j\omega_n\cdot K_{d2}}$	$\omega_z=\infty$
5, 5d(l) (SRC)	$\frac{\omega_n}{\omega_n-j\cdot Q\cdot\left(1-\omega_n^2\right)}$	$\omega_z=0$ $\omega_z=\infty$
6, 6d(l)	$\frac{\omega_n^2\cdot K_n}{\omega_n^2\cdot K_{d1}-j\omega_n\cdot Q\cdot\left(1-\omega_n^2\right)}$	$\omega_z=0$ $\omega_z=\infty$
7, 7d(l)	$\frac{Q}{Q\cdot K_{d1}\cdot\left(1-\omega_n^2\right)+j\omega_n\cdot K_{d2}}$	$\omega_z=\infty$
5, 5d(r), 6, 6d(r) (LCC)	$\frac{-\omega_n^2\cdot K_n}{\left(1-\omega_n^2\cdot K_{d1}\right)+j\omega_n\cdot Q\cdot K_{d2}\cdot\left(1-\omega_n^2\cdot K_{d3}\right)}$	$\omega_z=0$ $\omega_z=\infty$
7, 7d(r), 8, 8d(r)	$\frac{j\omega_n\cdot Q\cdot Kn}{\left(1-\omega_n^2\cdot K_{d1}\right)+j\omega_n\cdot Q\cdot K_{d2}\cdot\left(1-\omega_n^2\cdot K_{d3}\right)}$	$\omega_z=0$ $\omega_z=\infty$
8, 8d(l) (PRC)	$\frac{Q}{j\omega_n+Q\cdot\left(1-\omega_n^2\right)}$	$\omega_z=\infty$

Table 2.4: Definition of the Constants Used in Table 2.3

Circuits	Gain type	Q	K_n	K_{d1}	K_{d2}	K_{d3}
1	M_v	Q_s	$K_0^L \cdot K_1^L$	$K_0^L \cdot K_1^L$	K_0^L	K_1^L
1d	M_i	Q_p	$K_0^C \cdot K_1^C$	$K_0^C \cdot K_1^C$	K_0^C	K_1^C
2	M_v	Q_s	K_1^L	K_1^L	$K_0^L \cdot K_1^L$	1
2d	M_i	Q_p	K_1^C	K_1^C	$K_0^C \cdot K_1^C$	1
3	M_v	Q_s	---	K_0^L	$K_0^L \cdot K_1^L$	---
3d	M_i	Q_p	---	K_0^C	$K_0^C \cdot K_1^C$	---
4(l)	M_i	Q_p	K_1^C	$K_0^C \cdot K_1^C$	---	K_1^C
4d(l)	M_v	Q_s	K_1^L	$K_0^L \cdot K_1^L$	---	K_1^L
4(r)	M_i	Q_s	---	---	K_1^C	---
4d(r)	M_v	Q_p	---	---	K_1^L	---
5(l)	M_i	Q_p	---	---	---	---
5d(l)	M_v	Q_s	---	---	---	---
5(r)	M_i	Q_p	K_0^C	$K_0^C \cdot K_1^C$	K_0^C	K_1^C
5d(r)	M_v	Q_s	K_0^L	$K_0^L \cdot K_1^L$	K_0^L	K_1^L
6(l)	M_i	Q_p	K_1^C	$K_0^C \cdot K_1^C$	K_0^C	---
6d(l)	M_v	Q_s	K_1^L	$K_0^L \cdot K_1^L$	K_0^L	---
6(r)	M_i	Q_p	K_1^C	K_1^C	1	1
6d(r)	M_v	Q_s	K_1^L	K_1^L	1	1
7(l)	M_v	Q_p	---	K_0^L	K_0^L	K_1^L
7d(l)	M_i	Q_s	---	K_0^C	K_0^C	K_1^C
7(r)	M_i	Q_s	K_1^L	K_1^L	$K_0^L \cdot K_1^L$	1
7d(r)	M_v	Q_p	K_1^C	K_1^C	$K_0^C \cdot K_1^C$	1
8(r)	M_i	Q_s	1	$K_0^L \cdot K_1^L$	K_0^L	K_1^L
8d(r)	M_v	Q_p	1	$K_0^C \cdot K_1^C$	K_0^C	K_1^C
8(l)	M_v	Q_p	---	---	---	---
8d(l)	M_i	Q_s	---	---	---	---

Table 2.5: Characteristics of Three Elements Resonant Converters II

Circuits	Load Independent Gain	Filter Characteristics
1, 1d, 2, 2d, 4, 4d(l)	$M=1$ at $\omega_n=\frac{1}{\sqrt{K_n}}$ $M=1$ at $\omega_n=0$	band pass, high-frequency gain slope -20 dB/dec.
3, 3d	$M=\frac{1}{1-K_{d1}}$ at $\omega_n=1$ $M=1$ at $\omega_n=0$	low pass, high-frequency gain slope -60 dB/dec.
4, 4d(r)	$M=1$ at $\omega_n=0$	low pass, high-frequency gain slope -20 dB/dec.
5, 5d(l) (SRC)	$M=1$ at $\omega_n=1$	band pass, high-frequency gain slope -20 dB/dec.
6, 6d(l)	$M=\frac{1}{K_{d1}}$ at $\omega_n=1$	band pass, high-frequency gain slope -20 dB/dec.
7, 7d(l) (LCC)	$M=\frac{1}{K_{d2}}$ at $\omega_n=0$	low pass, high-frequency gain slope -40 dB/dec.
5, 5d(r), 6, 6d(r)	$M=\frac{K_n}{K_{d1}-K_{d3}}$ at $\omega_n=\frac{1}{\sqrt{K_{d3}}}$	band pass, high-frequency gain slope -20 dB/dec.
7, 7d(r), 8, 8d(r)	$M=\frac{K_n\cdot K_{d1}}{K_{d2}\cdot(1-K_{d3})}$ at $\omega_n=\frac{1}{\sqrt{K_{d1}}}$	band pass, high-frequency gain slope -40 dB/dec.
8, 8d(l) (PRC)	$M=1$ at $\omega_n=0$	low pass, high-frequency gain slope -40 dB/dec.



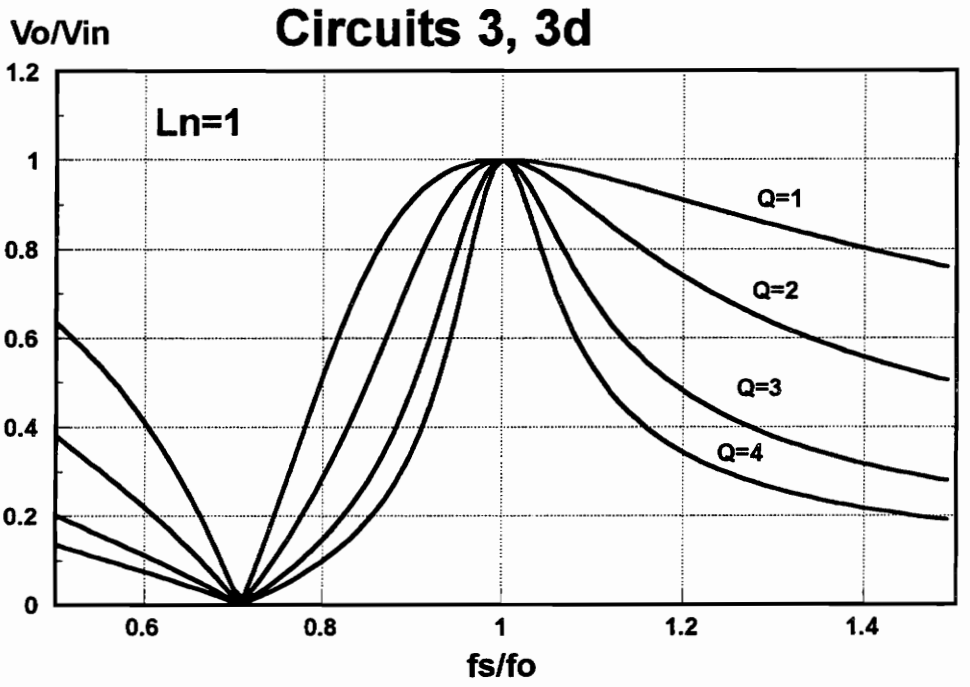


Figure 2.27: Gain of topologies similar to the SRC (1).

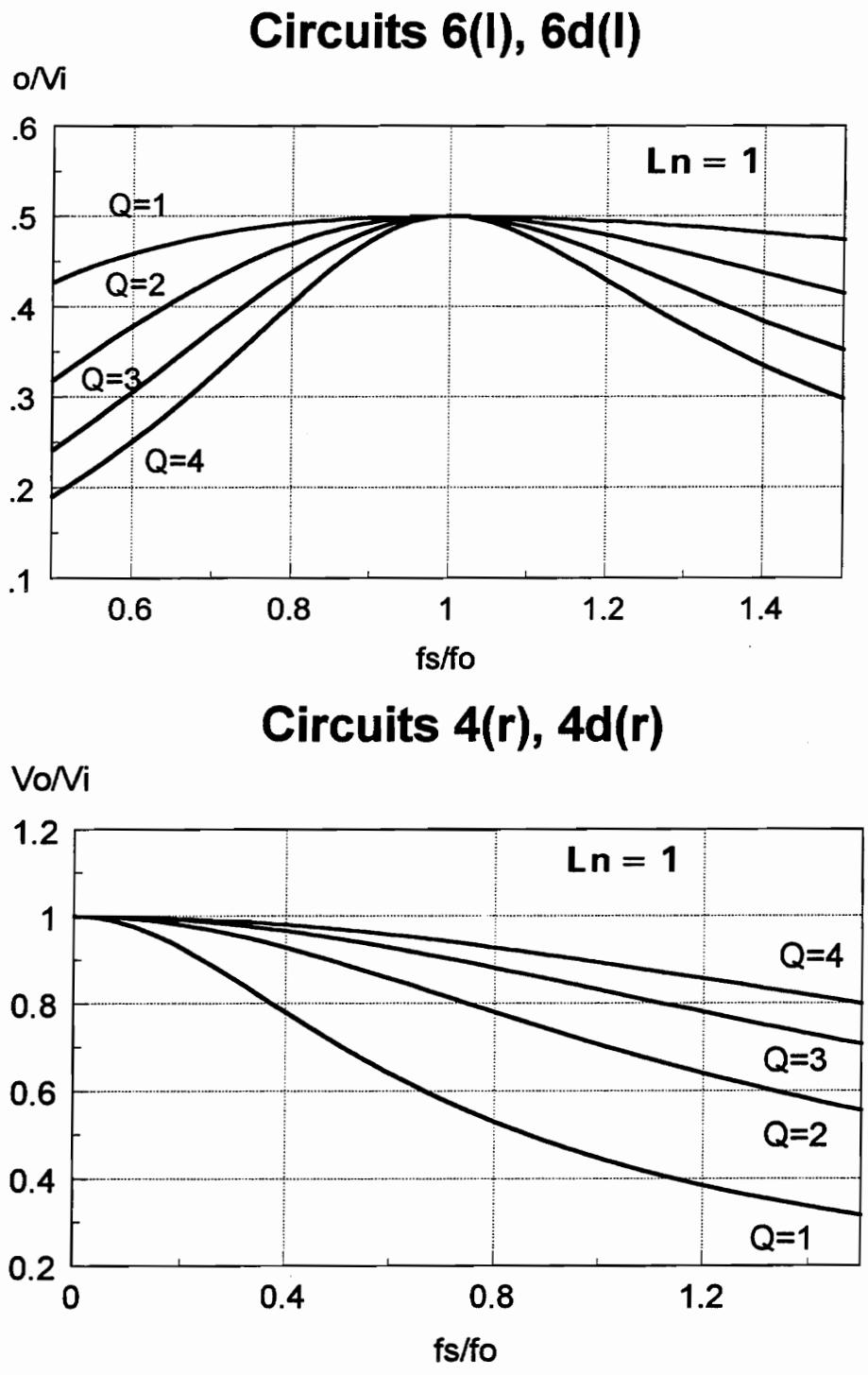


Figure 2.28: Gain of topologies similar to the SRC (2).

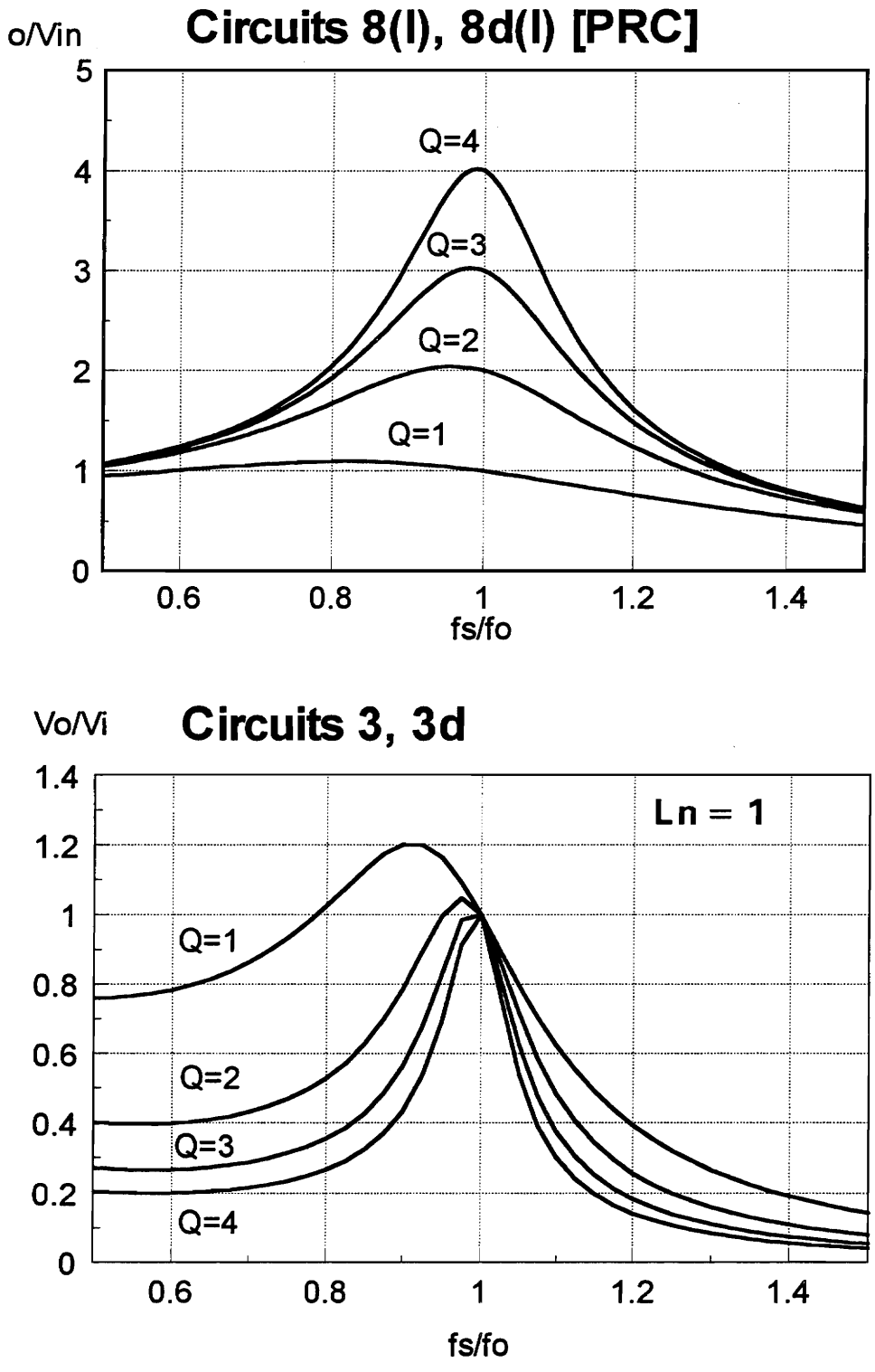


Figure 2.29: Gain of topologies similar to the PRC (1).

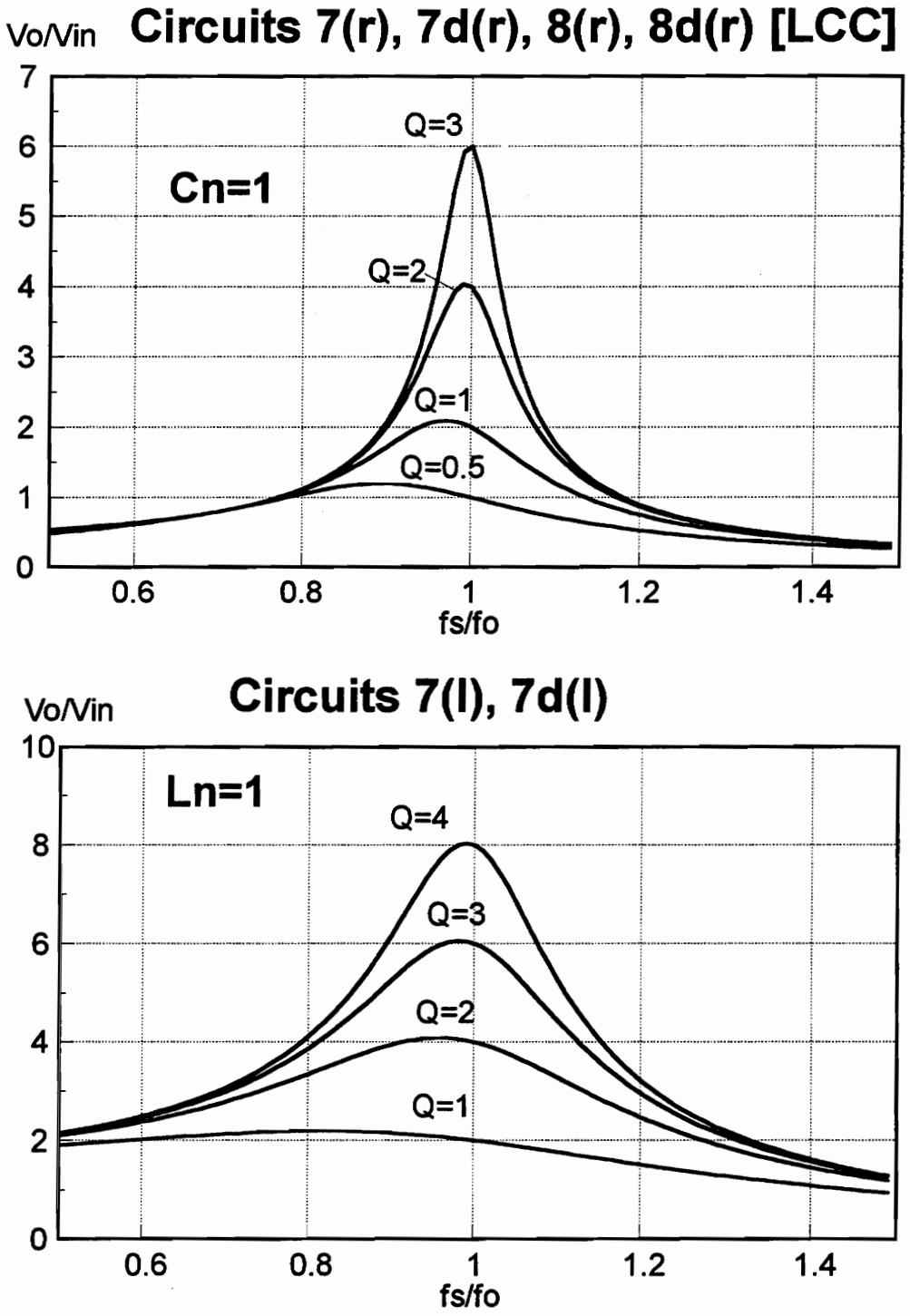


Figure 2.30: Gain of topologies similar to the PRC (2).

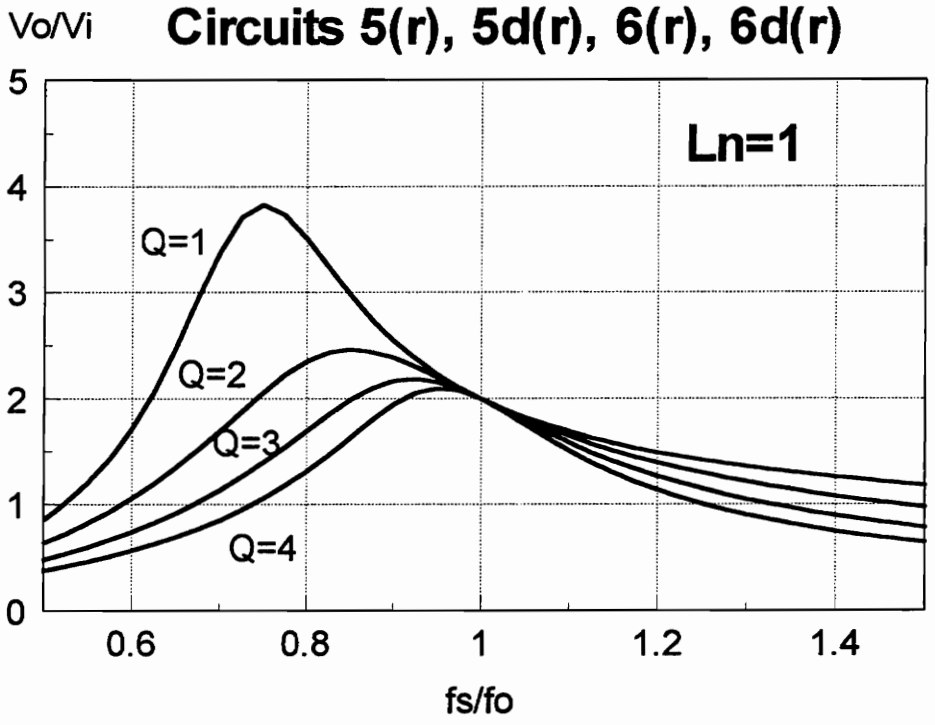


Figure 2.31: Gain of topologies similar to the PRC (3).

2.7.2 LCC Resonant Converter

The LCC resonant converter model is presented in Figure 2.32. The input voltage source to the resonant tank, V_e, is an ac source corresponding to the fundamental of the voltage at the output of the inverter stage. The dependent voltage source corresponding to the rectifier is replaced by a resistor as described in previous sections. Using the method of analysis described in the previous section, the voltage gain for the LCC is

$$M_v(\omega_n, Q_p, C_n) = \frac{j\cdot\omega_n\cdot Q_p\cdot\left(1+\frac{1}{C_n}\right)}{1-\omega_n^2\cdot\left(1+\frac{1}{C_n}\right)+j\cdot\omega_n\cdot\frac{\pi^2}{8}\cdot Q_p\cdot\frac{(1+C_n)^2}{C_n}\cdot\left(1-\omega_n^2\right)}, \quad (2.45)$$

normalizing the frequency and impedances with

$$\omega_o = \frac{1}{\sqrt{L_s\cdot C_{eq}}} \quad \text{and} \quad Z_o = \sqrt{\frac{L_s}{C_{eq}}}, \quad (2.46)$$

and defining

$$Q_p = \frac{R_{load}}{Z_o}, \quad C_{eq} = \frac{C_s\cdot C_p}{C_s+C_p}, \text{ and } \quad C_n = \frac{C_p}{C_s}. \quad (2.47)$$

Figure 2.33 shows the voltage gain of the LCC resonant converter for C_n equal to 1, comparing the approximate analysis and the exact solution. Figures 2.34, and 2.35 show the voltage gain of the LCC resonant converter for C_n equal to 2, and 0.5, respectively. It can be seen that the converter has load-independent gain at the frequency that corresponds to the resonance of the inductor with the series capacitor.

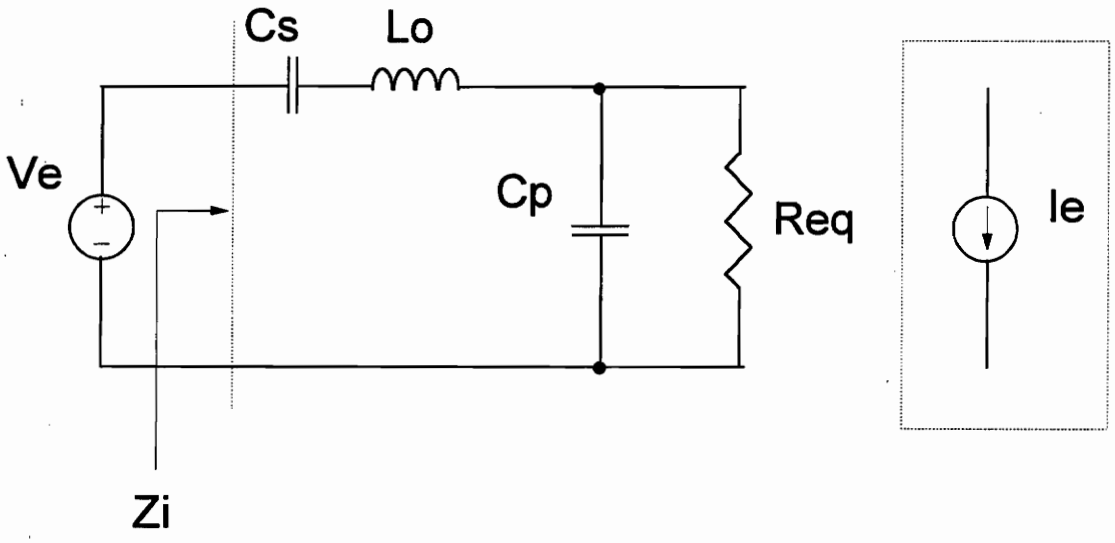


Figure 2.32: LCC resonant converter model.

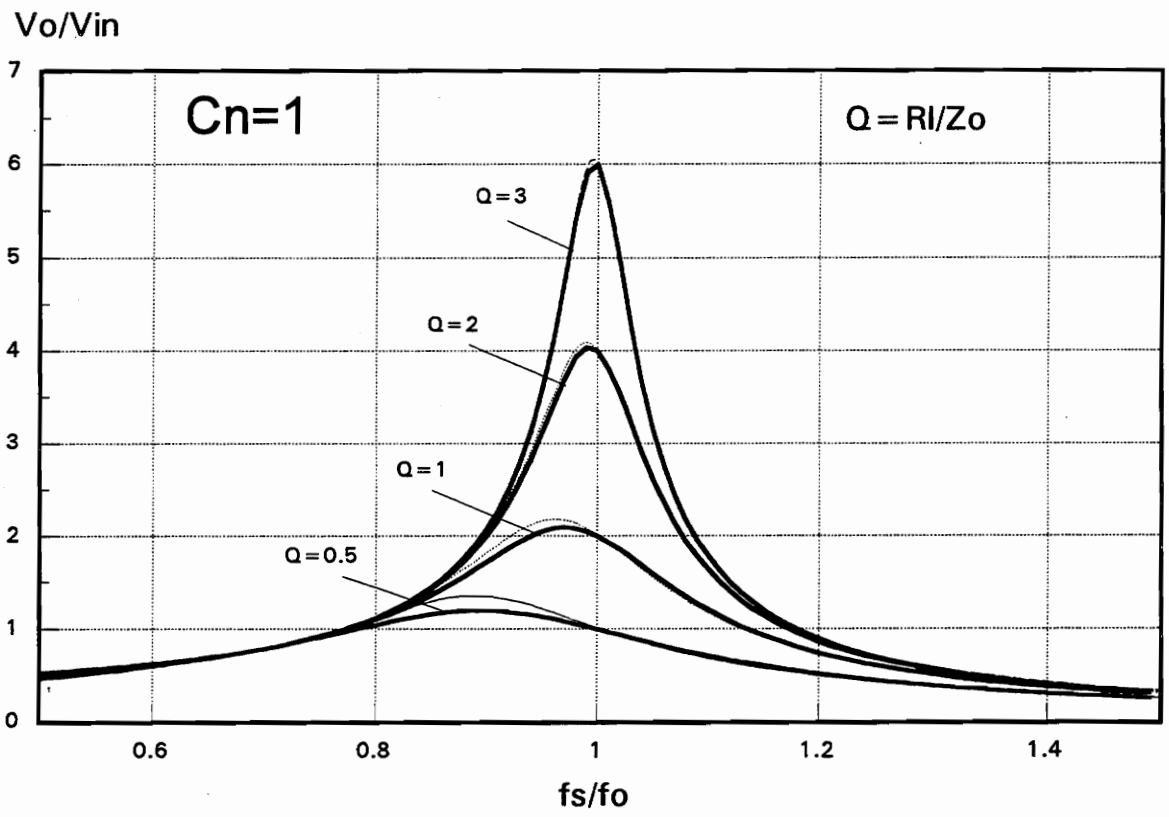


Figure 2.33: Voltage gain of the LCC-RC obtained for C_n= 1. Exact solution thin lines, and approximate solution thick lines.

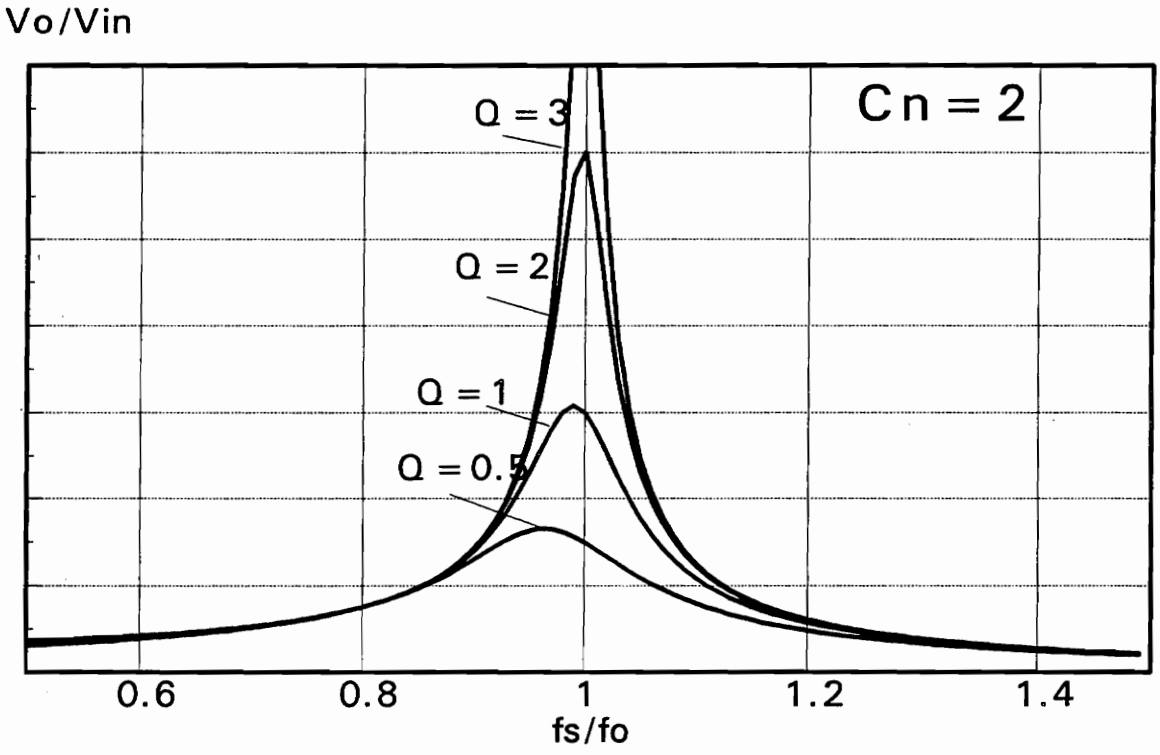


Figure 2.34: Voltage gain of the LCC-RC obtained for $C_n = 2$.

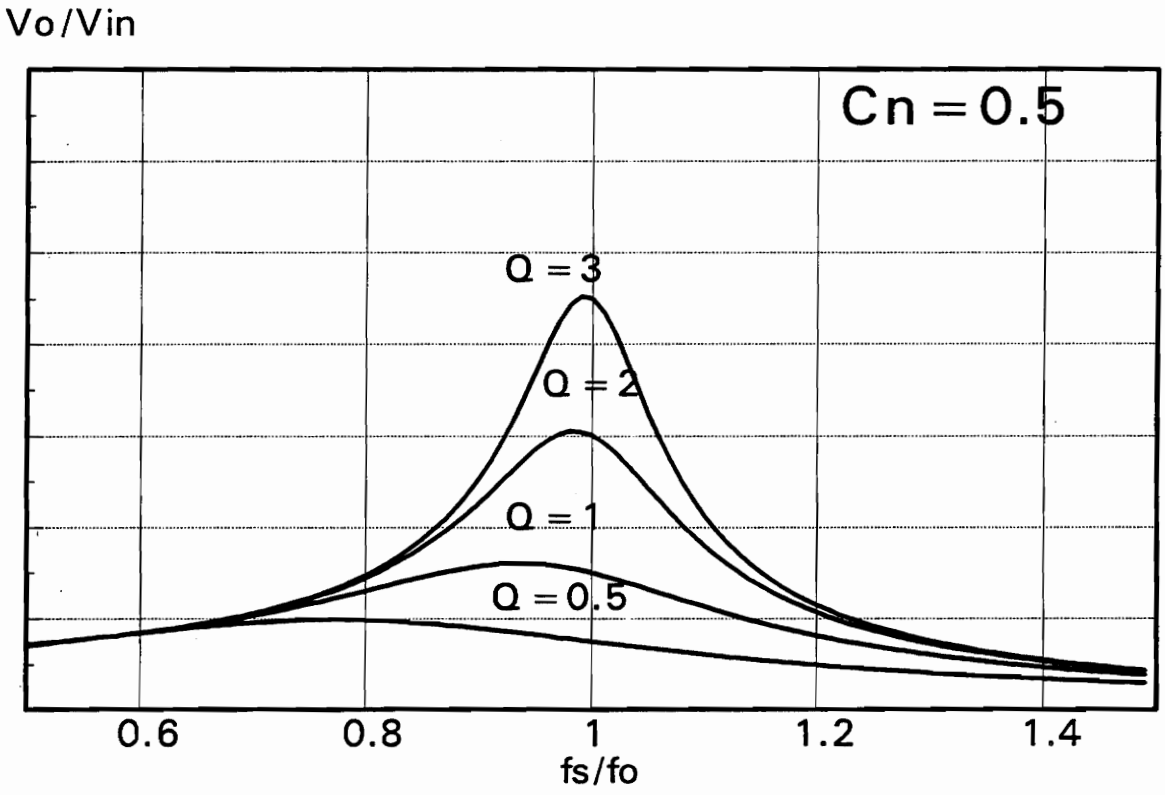


Figure 2.35: Voltage gain of the LCC-RC obtained for $C_n = 1/2$.

The peak voltage gain for the LCC resonant converter is $Q_p \cdot (1+C_n)$ instead of Q_p, as was the case for the PRC.

The characteristics of the converter approach those of the SRC as C_n tends to zero. The dominant behavior in the characteristics is similar to the PRC case for large values of C_n. Consequently, the converter behaves with a combination of properties of the SRC and the PRC, and may be closer to one or the other depending on the value of C_n. This capability allows a larger reduction of the circulating current for ZVS operation than for the PRC, but still retaining the step-up capabilities of the PRC.

The input impedance to the resonant tank, Z_i, determines the soft-switching characteristics of the LCC resonant converter. Using the fundamental approximation method, the normalized input impedance to the tank is

$$Z_i(\omega_n, Q_s) = \frac{1-\omega_n^2 \cdot \left(1+\frac{1}{C_n}\right) + j \cdot \omega_n \cdot \frac{\pi^2}{8} \cdot Q_p \cdot \frac{(1+C_n)^2}{C_n} \cdot \left(1-\omega_n^2\right)}{-\omega_n^2 \cdot \frac{\pi^2}{8} \cdot Q_p \cdot \frac{(1+C_n)^2}{C_n} + j \cdot \omega_n \cdot \left(1+\frac{1}{C_n}\right)} \quad (2.48)$$

Figure 2.36 shows the plot of the phase of the input impedance for Cn equal to 1, 2, and 0.5. It can be seen that the impedance changes from inductive to capacitive at a frequency dependent on the load, as was the case for the PRC. However, the load dependence is smaller than for the PRC. The converter operates with zero-voltage switching for frequencies above the peak of the voltage gain. The effect of the switch capacitance on the ZVS limit can be found in Chapter 4.

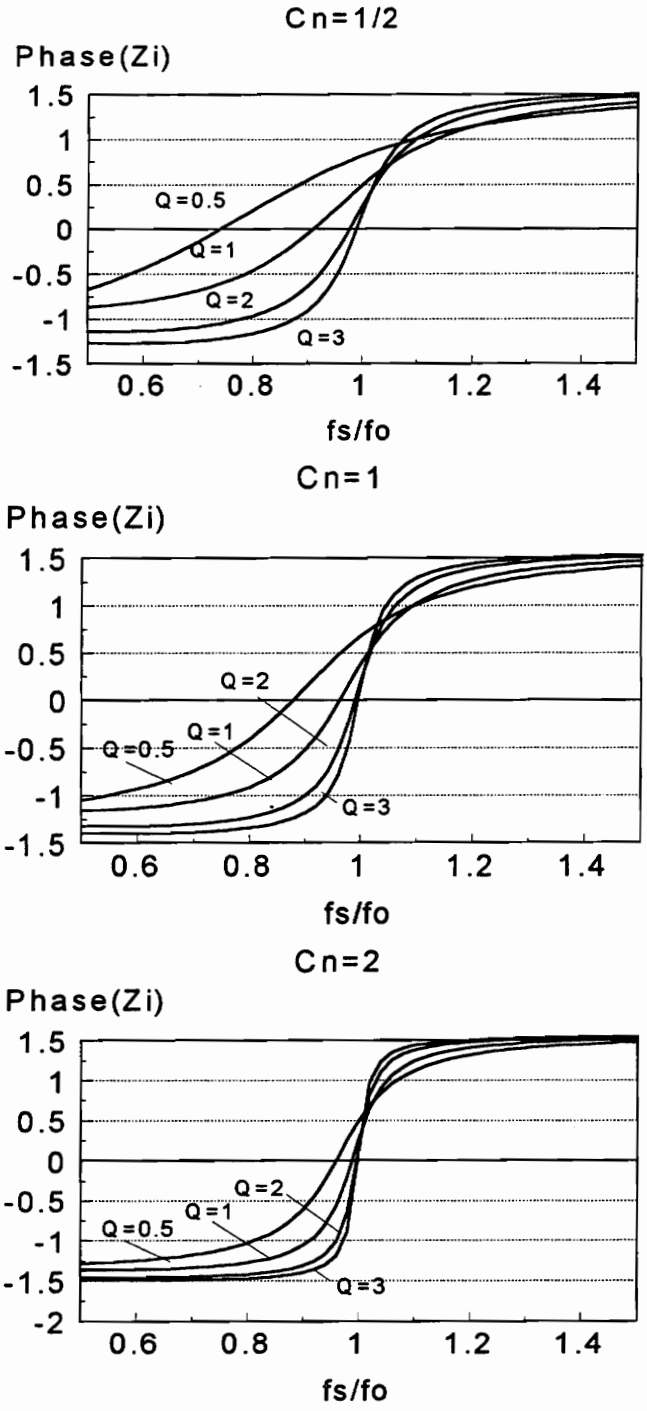


Figure 2.36: Phase of the input impedance to the resonant tank for different loads as a function of frequency.

The rms value of the normalized input current to the tank can be expressed as a function of the normalized input impedance to the tank as,

$$I_{in}^{n}(\omega_n, Q_p, C_n) = \frac{\pi}{2\cdot\sqrt{2}} \cdot \frac{1}{Z_i(\omega_n, Q_p, C_n)} \tag{2.49}$$

Using Eq. (2.44) and Eq. (2.49), the normalized input current to the tank for constant gain can be calculated. Figure 2.37 shows the normalized input current to the tank with respect to frequency showing the constant gain current. The characteristics show that the current for constant gain remains almost constant when the load changes for large voltage gains, as is the case for the PRC. However, for low voltage gains the current decreases slightly when the load decreases. The current decreases further at low voltage gains and smaller values of C_n as the converter approaches SRC behavior. Also, the characteristics show that the frequency range to keep the voltage gain constant over a load variation is larger than for the PRC.

The rms value of the actual input current to the tank can be expressed as,

$$I_{in}(\omega_n, Q_p, C_n) = \frac{V_{out}^2}{R_{load}\cdot V_{in}} \cdot \frac{I_{in}^{n}(\omega_n, Q_p, C_n)\cdot Q_p}{M_v^2(\omega_n, Q_p, C\ )} \tag{2.50}$$

Figures 2.38-2.40 show the plot of the term,

$$f(\omega_n, Q_p, C_n) = \frac{I_{in}^{n}(\omega_n, Q_p, C_n)}{M_v^2(\omega_n, Q_p, C_n)\cdot Q_p} \tag{2.51}$$

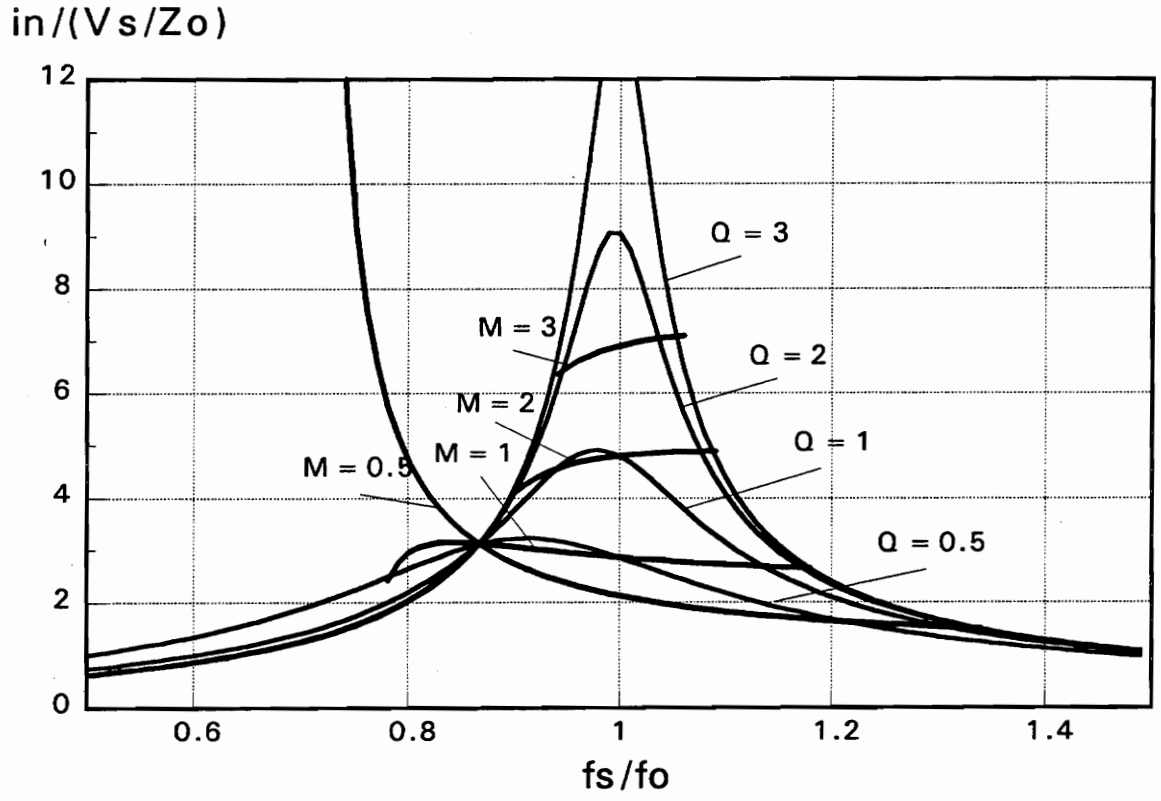


Figure 2.37: Normalized input current to the resonant tank for different loads and constant gain current as a function of frequency.

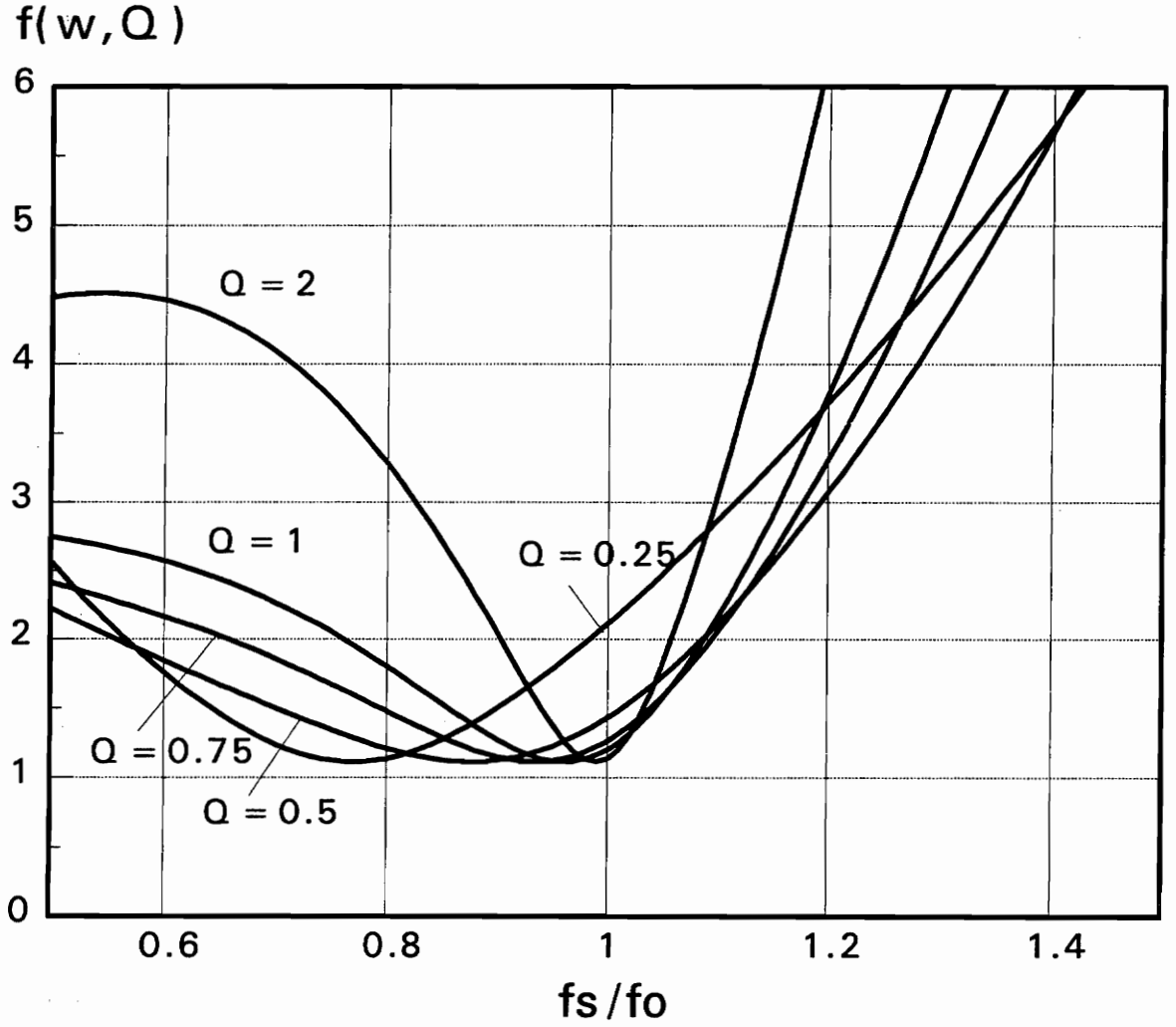


Figure 2.38: Input current to the resonant tank normalized with respect to the output power for different loads as a function of frequency, for Cn=1.

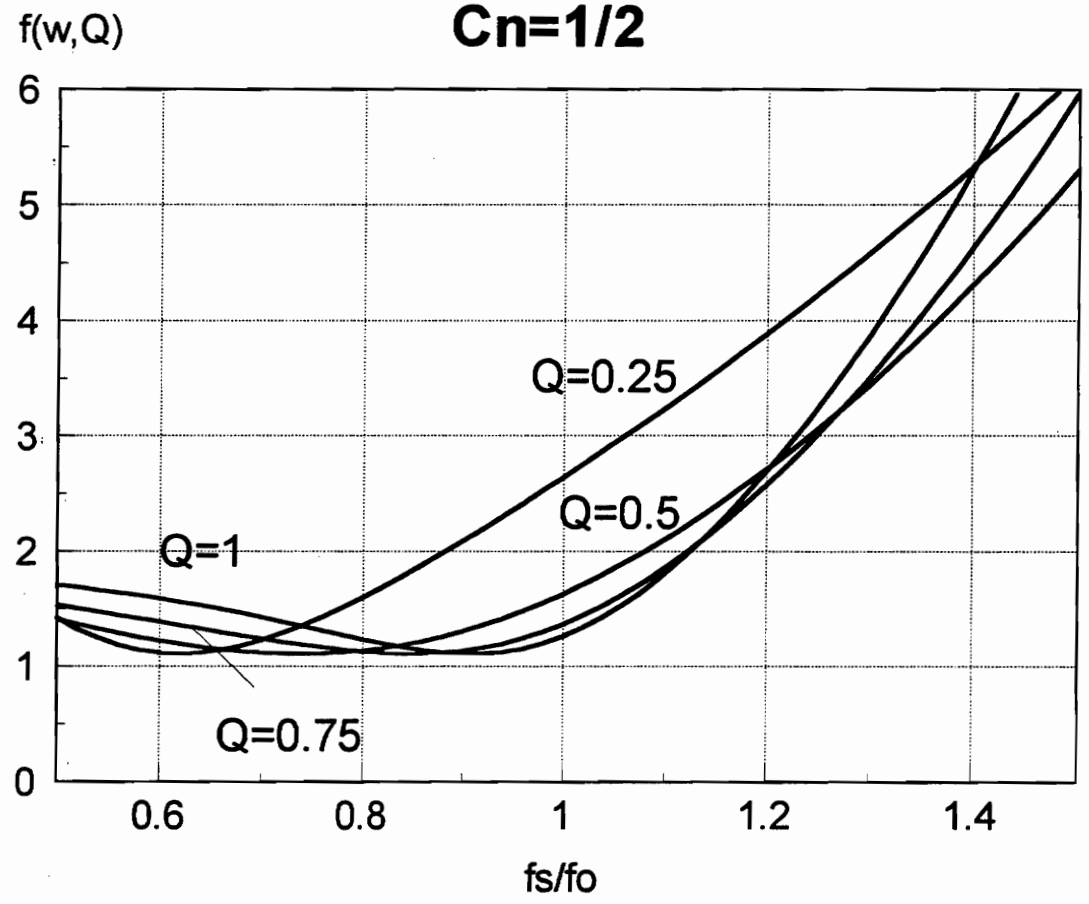


Figure 2.39: Input current to the resonant tank normalized with respect to the output power for different loads as a function of frequency, for Cn=1/2.

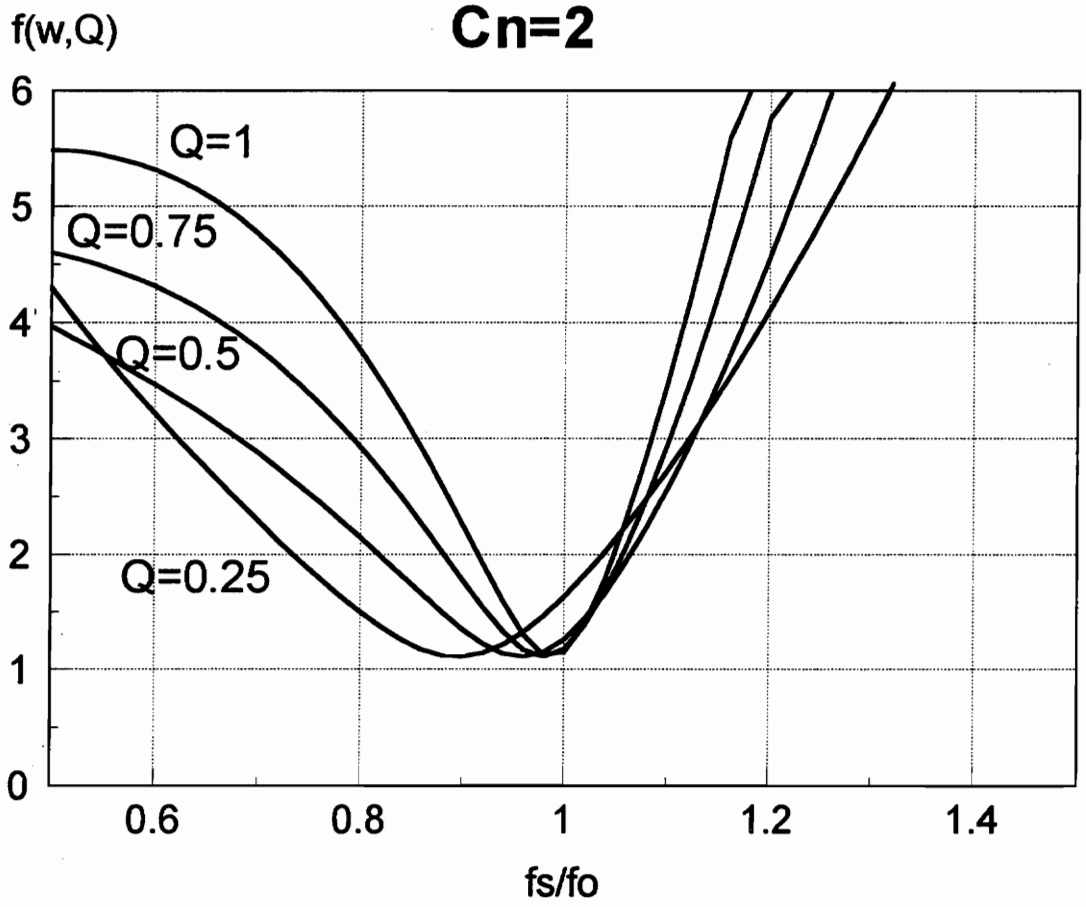


Figure 2.40: Input current to the resonant tank normalized with respect to the output power for different loads as a function of frequency, for Cn=2.

The discussion for the PRC can be repeated here, with the difference that the current increases for different Q values according to C_n. Also the behavior between SRC and PRC can be seen in the fact that the slope of the curves for high frequencies decreases, and the current values at low frequencies are higher than for the PRC.

Also, from Figs. 2.38-2.40 it can be seen that the current required in the tank, can be several times the minimum current. The reactive power to be provided by the inverter can be represented by the power factor of the loaded resonant tank. For the LCC converter the power factor seen by the inverter is,

$$PF_{LCC}(\omega_n, Q_p, C_n) = \frac{P_{out}}{S} = \frac{\pi}{2\cdot\sqrt{2}} M_v(\omega_n, Q_p, C_n) \cdot \frac{1}{1+j\cdot\omega_n\cdot(1+C_n)\cdot\frac{\pi^2}{8}\cdot Q_p} \quad (2.52)$$

where S corresponds to the product of the rms values of the current and the voltage at the input of the resonant tank.

Figures 2.41-2.43 show the power factor at the input of the resonant tank for several values of C_n. It is clear that the curves are closer to the ones for the SRC for low C_n values, and closer to the PRC for large C_n values.

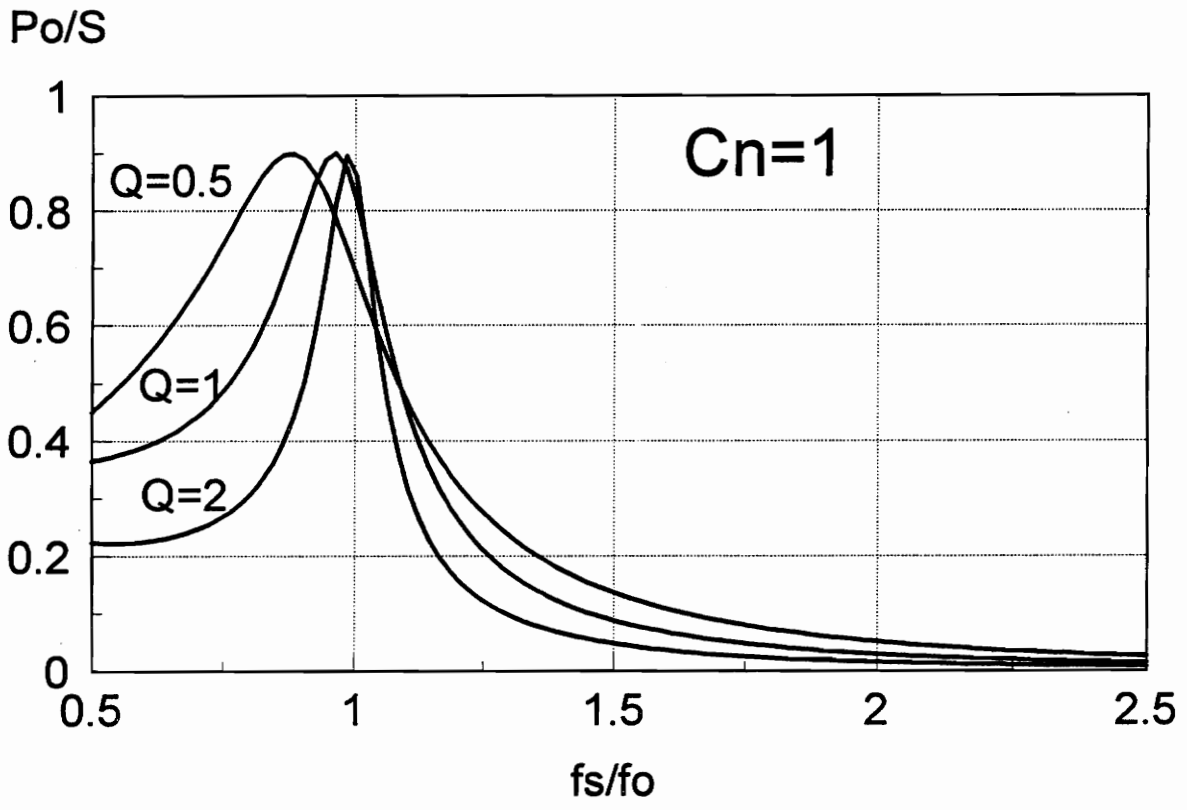


Figure 2.41: Power factor at the input of the resonant tank for different loads as a function of frequency for C_n=1.

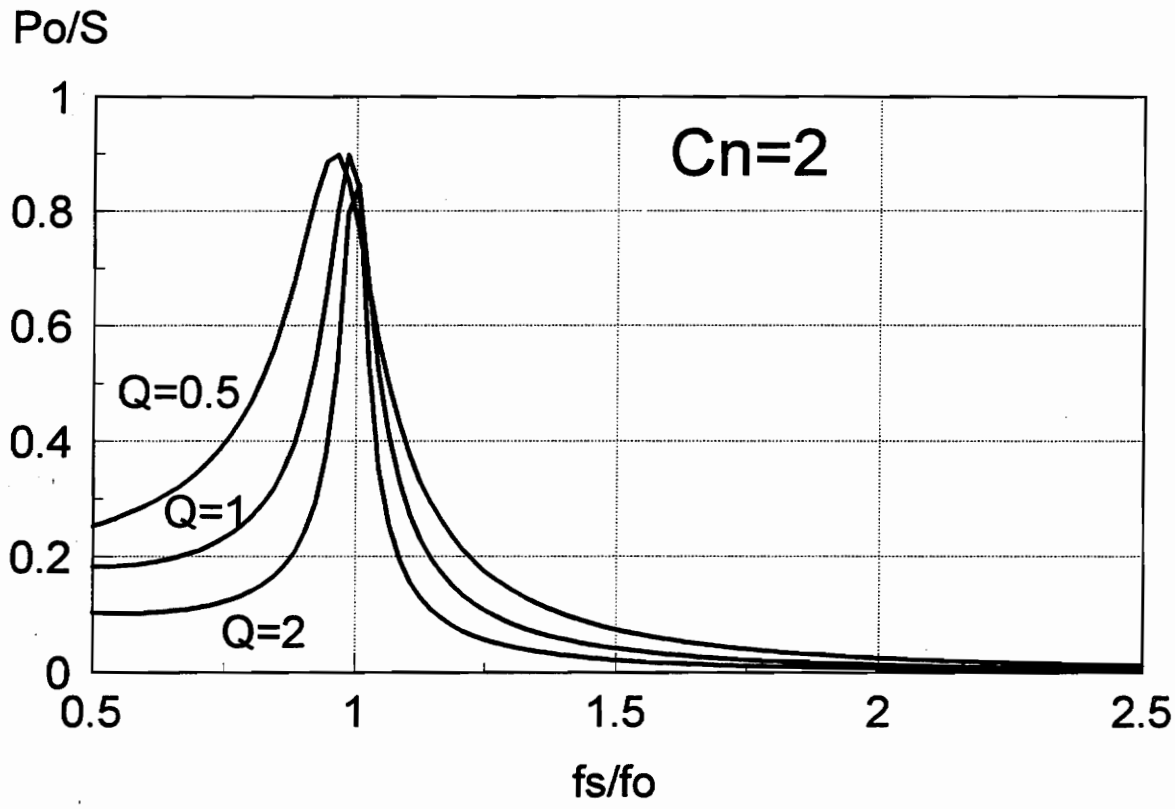


Figure 2.42: Power factor at the input of the resonant tank for different loads as a function of frequency for C_n=2.

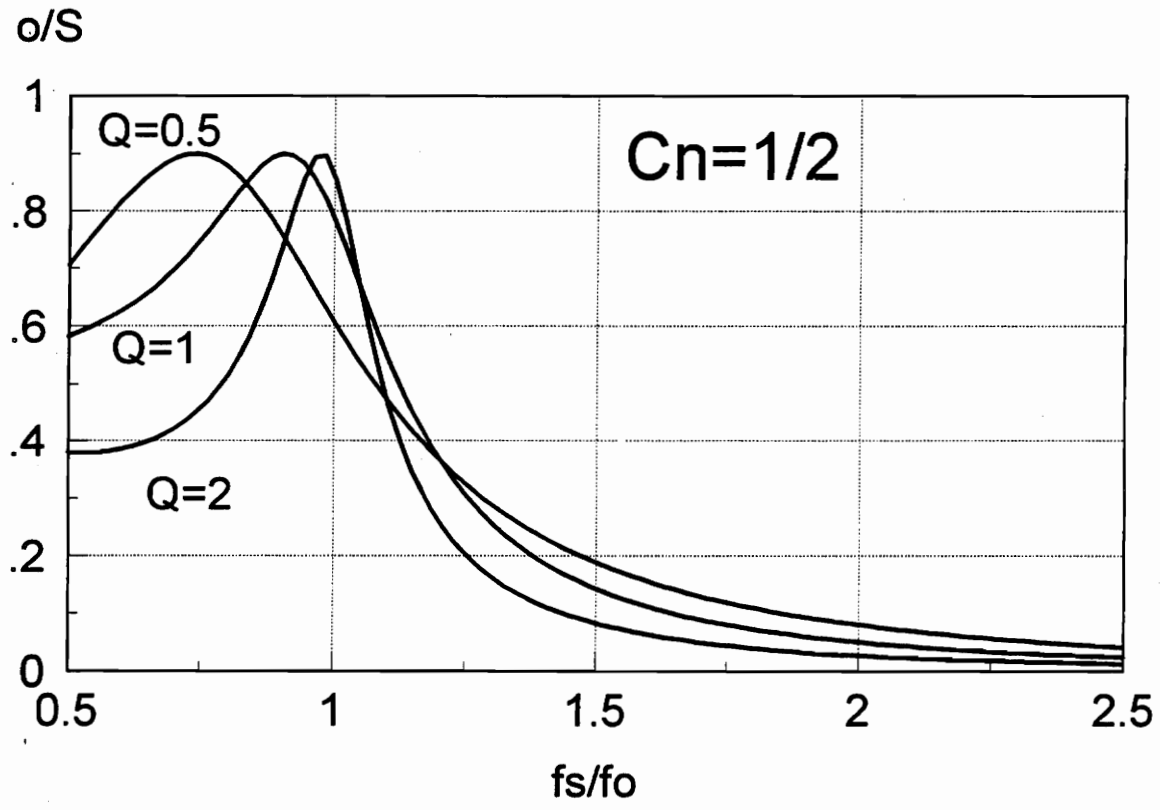


Figure 2.43: Power factor at the input of the resonant tank for different loads as a function of frequency for C_n=1/2.

2.8 Comparison of Resonant Converters and Conclusions

To compare the SRC, PRC, and LCC, three converters are designed for the following specs.:

- Input voltage range from 200 V to 300 V,
- Output voltage 5 V,
- Output Power range from 100 W to 10 W,
- Minimum switching frequency 500 kHz.

The converters are designed for ZVS operation. As has been described in section 2.3, ZVS operation eliminates the need for series blocking diodes and fast antiparallel diodes, resulting in a more efficient converter. The trade-offs described in the previous section have been considered for the converters as follows:

SRC

The Q value at full load has to be selected as high as possible to reduce the frequency range that is going to be needed for output voltage regulation. However, very high Q values make the circuit very sensitive to the tolerance of the resonant components, and also the resonant capacitor voltage increases with Q. At resonance the peak capacitor voltage is largest and would reach a value of Q times the input voltage. The Q value selected for full load is 5, and hence at 10% load the minimum Q is 0.5.

Zero-voltage switching requires operation above resonant frequency. The operating frequency is selected as close to resonance as possible to minimize the circulating currents in the resonant tank and some margin has to be allowed for the tolerance of the components. The operating frequency selected is 1.05 times the resonant frequency.

With the value of switching frequency and Q the rest of the parameters can be calculated.

PRC

The value of Q at full load has to be selected above one to reduce the currents in the tank, but large values result in reduced frequency range for the control. However, the inductor current increases very fast for higher values of Q. Therefore the value selected for full load is 2, and hence at 10% load the Q value is 20.

The switching frequency has to be selected as close to the peak voltage gain for the Q selected for ZVS operation, and to minimize circulating currents. The operating area in Fig. 2.45 shows that a smaller Q would not improve the reactive power required for this design at full load.

With the value of switching frequency and Q the rest of the parameters can be calculated.

LCC

The considerations for this converter are fairly similar to the ones for the PRC, with the exception that a series-to-parallel capacitor ratio has to be selected. Three designs are presented for the LCC: C_n=1, C_n=2, and C_n=0.5. Smaller capacitor ratios result in a larger frequency range required for the control, and larger ratios result in increased currents at full load high-line, as is the case for the PRC.

With the value of switching frequency, capacitor ratio, and Q the rest of the parameters can be calculated.

Table 2.6 presents the parameters selected for the six designs.

The currents' range, and peak capacitor voltages are given in Table 2.7 for the SRC and PRC designs, and in Table 2.8 for the three LCC converter designs. Figures 2.44-2.48 show the operating region of the six designs, and the power factor associated with each region. The following are the main general conclusions about the designs for the three converters.

- **Switching frequency range:** The SRC results in the larger frequency range, showing the difficulties faced in the design of this converter when large load and input voltage range are required. The LCC results in a larger frequency range than the PRC.

- **Resonant inductor current:** This current can be predicted from the power factor characteristics. The minimum current at full load corresponds to the LCC converter, which allows the design with the highest power factor. However, the current for the

LCC at full load high-line is larger than for the SRC for C_n equal to 0.5 and 2, which has the same current at high line and at low line. The PRC results in the larger currents, and this currents remain constant over the whole load range.

- **Capacitor voltage:** The largest voltage across the resonant capacitor corresponds to the SRC, which value could be reduced at the cost of reducing the power factor for the converter. The smallest values of voltage correspond to the LCC (C_n=0.5), because it can operate with a transformer turns ratio lower than the PRC.

For the three LCC resonant converter designs, the lowest current variation over the input voltage variation corresponds to a capacitance ratio of one. The lowest capacitance ratio (0.5) results in a larger frequency range. The highest capacitor ratio has the smallest frequency range required. However, the series capacitor voltage becomes extremely high. Capacitance ratios close to one result in a superior performance, i.e. lower currents and frequency range over line and load variations.

Among the three different resonant converters, the LCC converter results in the superior performance, because it can combine advantages of SRC and PRC. The efficiency at light load is worse than for the SRC. However, it results in lower currents and voltages than the PRC, at the cost of increasing the frequency range for regulation compared to the PRC. The frequency range required for the LCC design is still much smaller than the one required for the SRC.

However, the three converters have to operate with a power factor at the input of the resonant tank smaller than the one required for a PWM converter, which is

practically unity. Consequently, the voltage and current stresses for the resonant converters are always larger than for PWM converters. The main motivations for their use are the presence of large parasitic capacitance and/or inductance in the circuit that require a topology that can use them without energy loss, and the significant reduction in switching losses by ZVS or ZCS operation for high switching frequencies.

Several alternatives attempting to combine resonant switching and PWM operation are presented in the next chapters.

Table 2.6: Parameters Selected for the Three Designs

Converter	SRC	PRC	LCC	LCC	LCC
C_p/C_s	----	---	0.5	1	2
min. ω_n	1.05	1.05	0.95	1.0	1.0
max. ω_n	2.7	1.29	1.29	1.14	1.13
Q full load	5	2	0.75	1	0.5
Q min. load	0.5	20	7.5	10	5
L_o (in μH)	490	229	240	509	573
C_s (in nF)	0.23	----	1.14	0.4	0.27
C_p (in nF)	----	0.49	0.57	0.4	80.53
Trans. turns ratio	34.3	74	60	80	60

Table 2.7: Frequency Range, Current Stress, and Voltage Stress for SRC and PRC Designs

Converter	Load level	Parameter	High Line	Low Line
SRC	Full load	ω_n	1.123	1.05
		I_L	0.648	0.648
		V_{CPK}	1198	1282
	10 % load	ω_n	2.7	1.6
		I_L	0.065	0.065
		V_{CPK}	49.8	84
PRC	Full load	ω_n	1.2	1.05
		I_L	0.76	0.675
		V_{CPK}	581.8	581.8
	10 % load	ω_n	1.29	1.2
		I_L	0.77	0.72
		V_{CPK}	581.8	581.8

Table 2.8: Frequency Range, Current Stress, and Voltage Stress for the Three Design of the LCC Resonant Converter

C_p/C_s	Load level	Parameter	High Line	Low Line
C_n =0.5	Full load	ω_n	1.13	0.95
		I_L	0.68	0.61
		$V_{CPK\ (series)}$	227.4	240.7
		$V_{CPK\ (parallel)}$	383	383
	10 % load	ω_n	1.29	1.17
		I_L	0.66	0.61
		$V_{CPK\ (series)}$	192	192
		$V_{CPK\ (parallel)}$	383	383
C_n =1	Full load	ω_n	1.082	1.0
		I_L	0.64	0.6
		$V_{CPK\ (series)}$	671	677.96
		$V_{CPK\ (parallel)}$	628.3	628.3
	10 % load	ω_n	1.14	1.1
		I_L	0.63	0.61
		$V_{CPK\ (series)}$	628.8	628.6
		$V_{CPK\ (parallel)}$	581.8	581.8
C_n =2	Full load	ω_n	1.06	0.95
		I_L	0.66	0.63
		$V_{CPK\ (series)}$	1057	1071
		$V_{CPK\ (parallel)}$	471.7	471.3
	10 % load	ω_n	1.13	1.09
		I_L	0.62	0.6
		$V_{CPK\ (series)}$	943.7	943.7
		$V_{CPK\ (parallel)}$	471.3	471.3

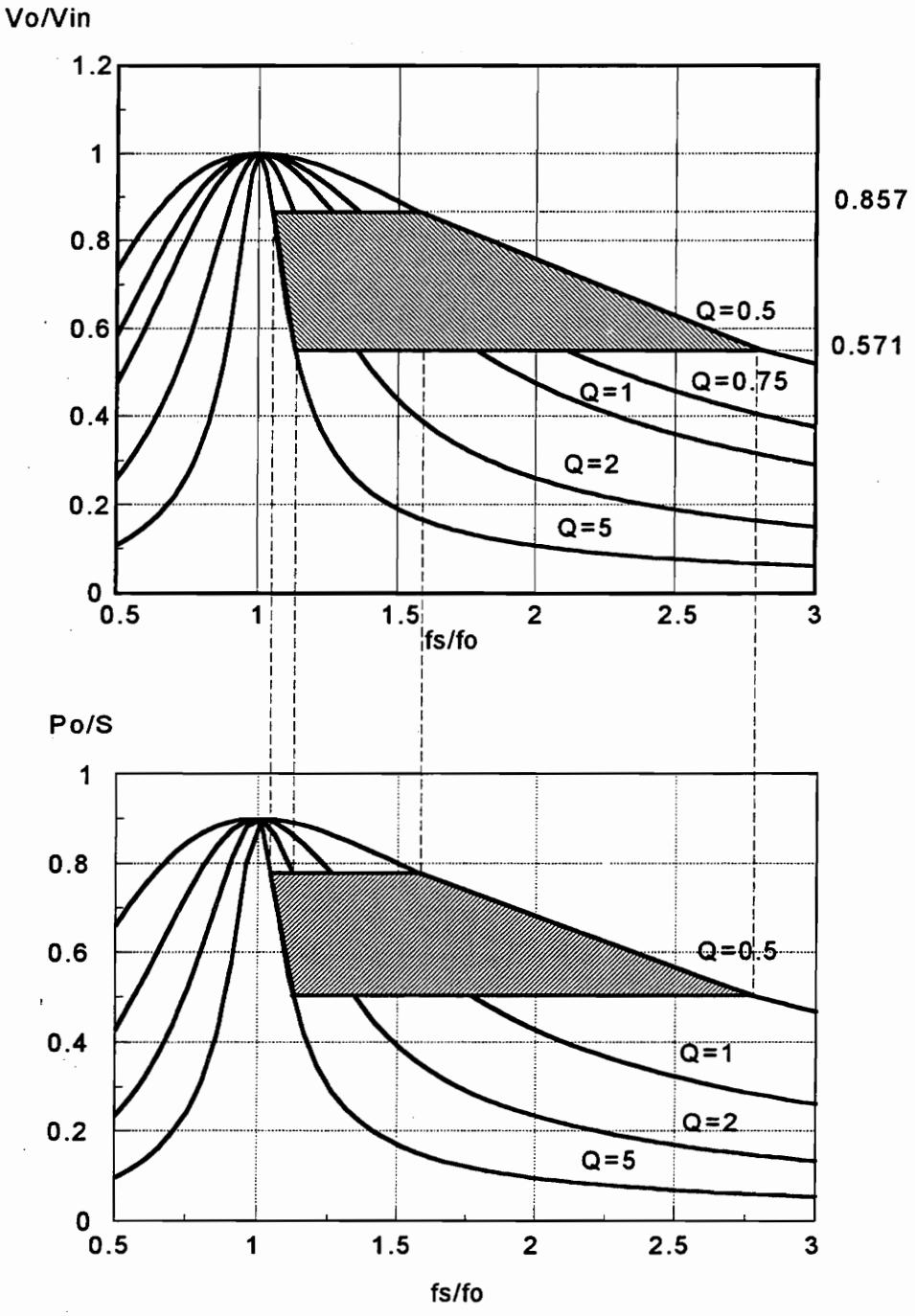


Figure 2.44: Series resonant converter design.

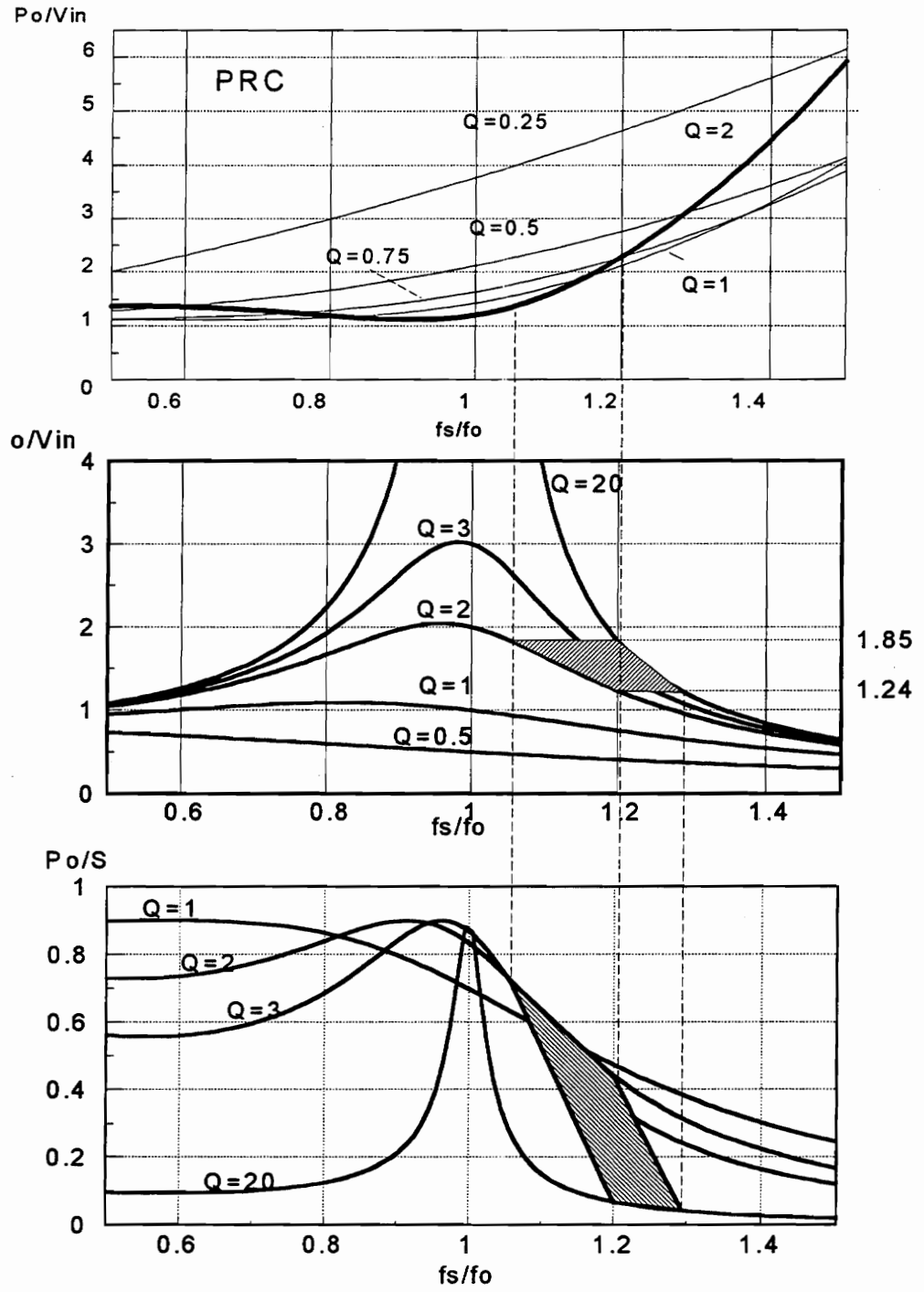


Figure 2.45: Parallel resonant converter design.

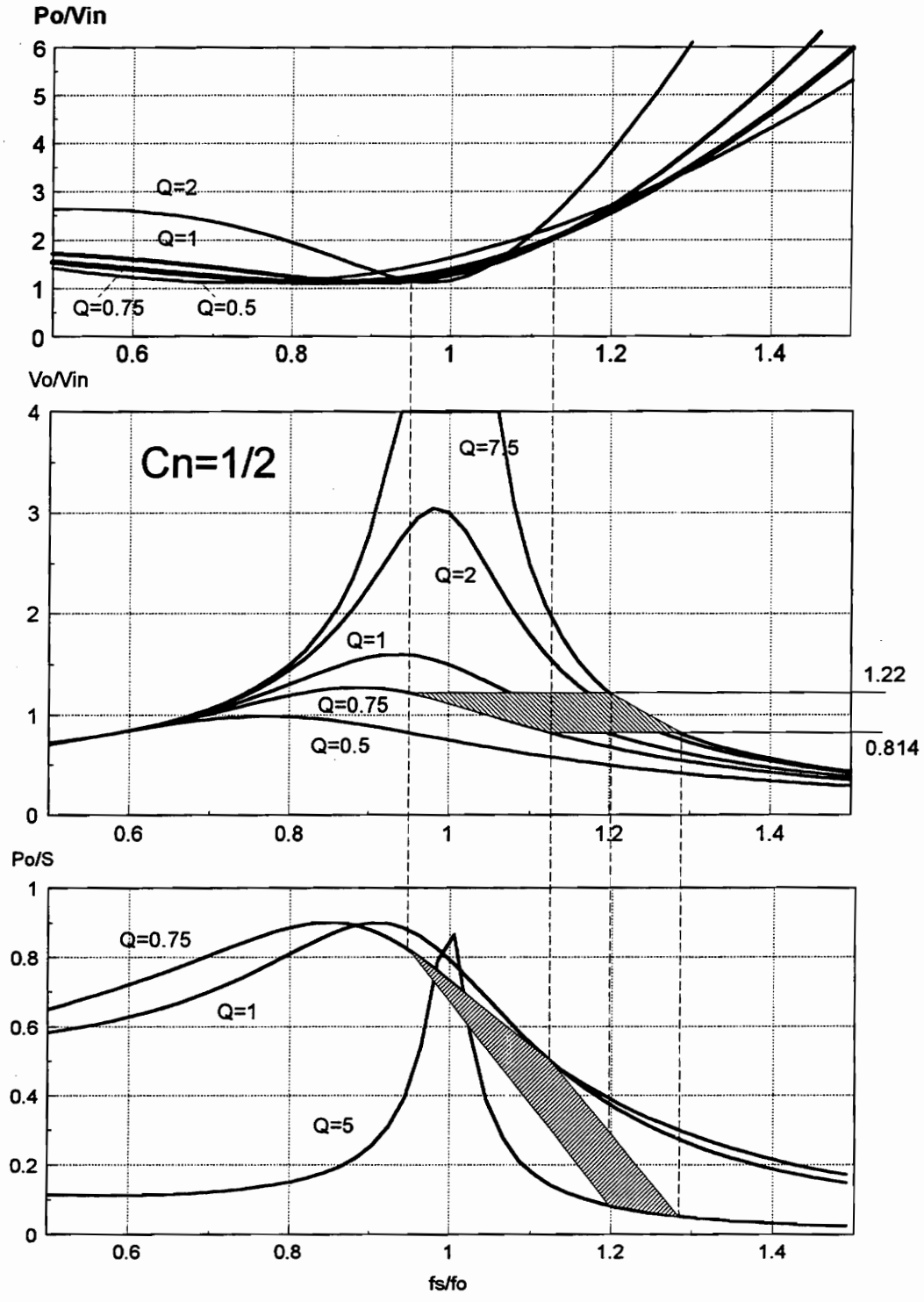


Figure 2.46: LCC resonant converter design with C_n =0.5.

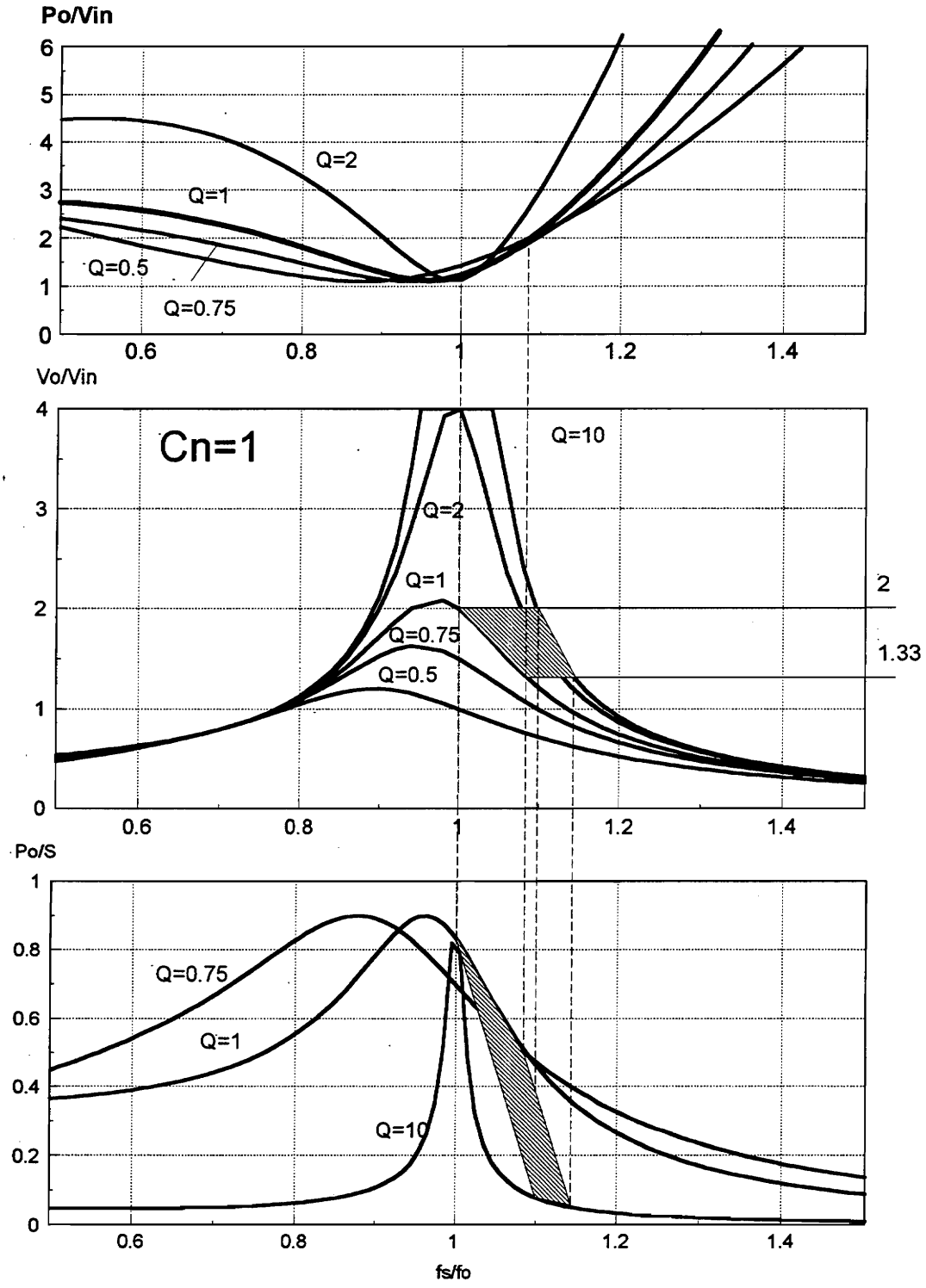


Figure 2.47: LCC resonant converter design with C_n =1.

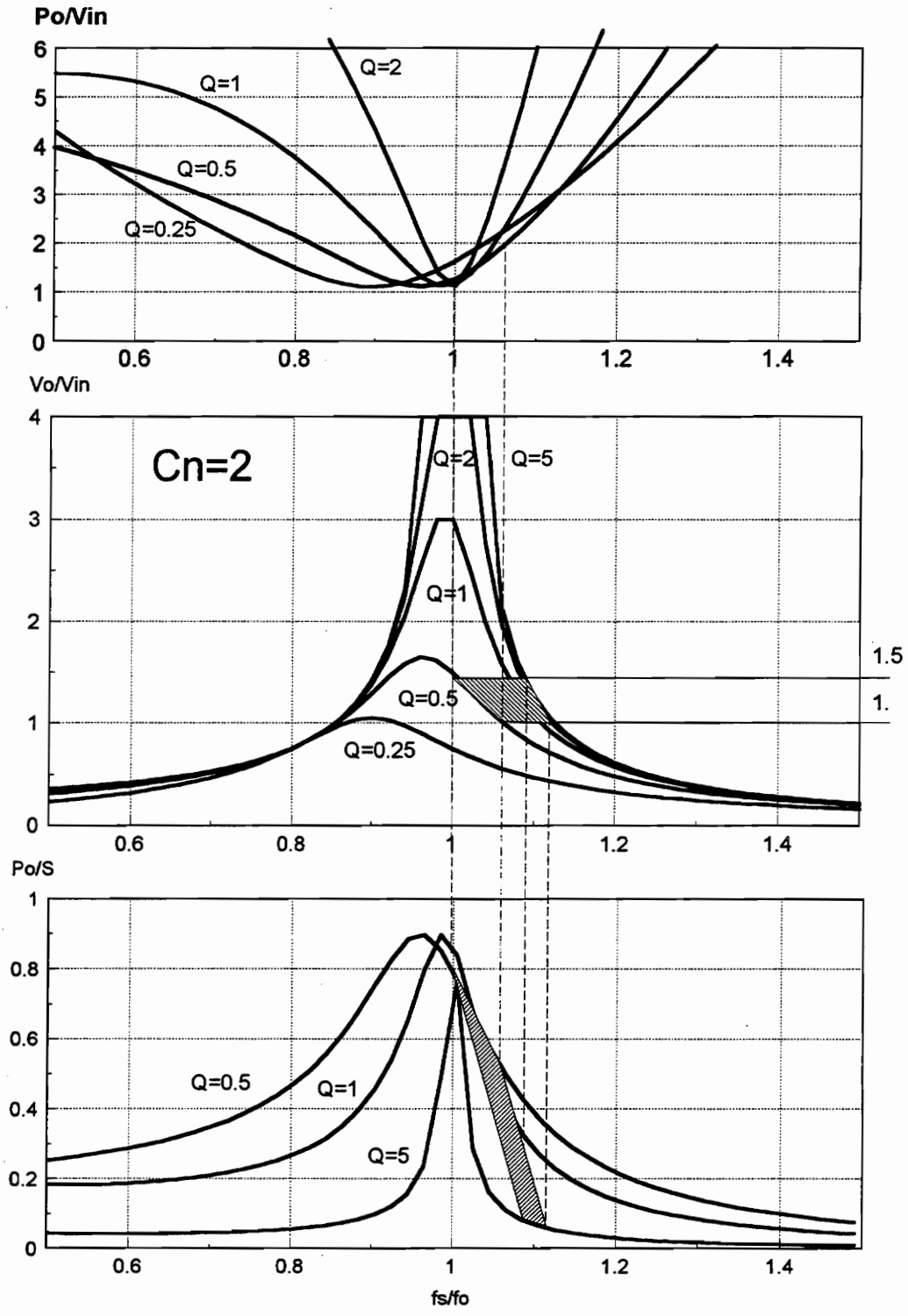


Figure 2.48: LCC resonant converter design with C_n =2.

3. Design and Performance Evaluation of Resonant Converters with Phase-Shift Control

3.1 Introduction

Control of conventional resonant converters requires variable frequency operation. Consequently, even if the converter has been designed for minimal reactive power at one extreme of the line range for full-load conditions, the converter has to operate with high reactive power at the other extreme of the line range for full-load. The only way to adjust the voltage gain for conventional resonant converters is varying the switching frequency to change the reactance of the tank, and hence changing the amount of reactive power required from the source inverter. The large reactive power results in large currents through the devices, and poor efficiency. Also, the magnetics have to be designed for the frequency range required for control over the load and input voltage variations, not taking full advantage of the highest frequency required at full load to optimize their volume and weight.

Phase-shift control allows operation at fixed frequency. This is achieved by applying a quasi-square wave of variable duty cycle to the resonant tank, instead of a square wave, as is the case for conventional resonant converters. The regulation in this case can be accomplished by varying the duty cycle of the voltage or current applied to the resonant tank.

Phase-shift control of resonant converters provides the advantage of operating at a fixed frequency, while retaining most of the desired features of conventional converters. The variation of reactive power over the line and load ranges is smaller than for conventional resonant converters, because with the constant frequency of operation the reactance of the resonant tank does not change from low-line to high-line conditions, resulting in less increase of reactive power over the input voltage variation. Also, the switching frequency can be optimized to result in minimum input current to the resonant tank for the required load. However, as it will be shown, to keep ZVS the designs using phase-shift control require higher reactive power than the ones using frequency control. The phase-shift control has circulating current during the time the input voltage to the tank is kept at zero.

In the previous chapter it was shown for which frequencies SRC, PRC, and LCC operate with zero-voltage switching (ZVS) and zero-current switching (ZCS). For reasons stated in the previous chapter, ZVS results in superior performance for converters employing MOSFET's; consequently this chapter addresses the ZVS operation of phase shifted resonant converters (PS-RC).

Conventional series and parallel resonant converters operate with zero voltage for the active devices when the switching frequency is above the resonant frequency for the SRC, and above the frequency corresponding to the peak voltage gain for the PRC and LCC. Since the conventional operation corresponds to phase-shift operation with unity duty cycle, phase-shift operation with large duty cycles also provides zero-voltage switching for the same frequencies as the conventional resonant converters. However, this

property is not retained when the duty cycle of the input voltage to the tank is reduced. The results are different for the SRC and PRC (and LCC). While the SRC cannot retain ZVS from full load to no load, it is possible to design the PRC and LCC to retain ZVS from full-load to no-load. The ZVS conditions and the design trade-offs involved in each case are analyzed in this chapter.

The fundamental approximation analysis presented for the conventional resonant converters in the previous chapter is also used for the phase-shifted resonant converters, and its accuracy compared with the available exact analysis.

Finally, the designs for a PS-SRC, PS-PRC, and PS-LCC converter are compared to assess the relative performance of the three converters, and experimental results are provided.

3.2 Fixed-Frequency Operation of Resonant Converters

Phase-shift operation of resonant converters uses a full-bridge resonant converter topology (Fig. 3.1). However, the operation and control of this circuit is different from conventional resonant converters. In each leg of the bridge, the switches are on and off in a complementary manner (180° out of phase), and the duty cycle for each switch is 50%. A phase shift is introduced between the gate drive signals for the two legs of the bridge to regulate the converter.

Regulation is accomplished by regulating either the time that each of the two diagonally-opposite switches conduct simultaneously, or duty cycle D, which is the complement of the phase shift time, (1-D). Zero phase shift corresponds to a maximum duty cycle. During the time when only one of the switches in each diagonal is on, the voltage across the resonant tank is clamped to zero. Then, the voltage applied to the tank is a quasi-square with positive and negative parts which can be regulated in a PWM manner (Fig. 3.2).

The converters are regulated by the PWM technique. The operation for a large duty cycle (i.e. tank voltage close to the square wave) is basically that of a conventional resonant converter. However, when the pulse width of the square wave is reduced, different resonant tanks behave differently.

Zero-voltage switching requires the zero crossing of the input current to the resonant tank to be lagging the leading edge of the voltage applied to the tank. Hence, zero phase for the impedance at the input of the tank is no longer the zero-voltage limit condition. The phase lag introduced by the tank's reactance has to be larger than half the phase shift.

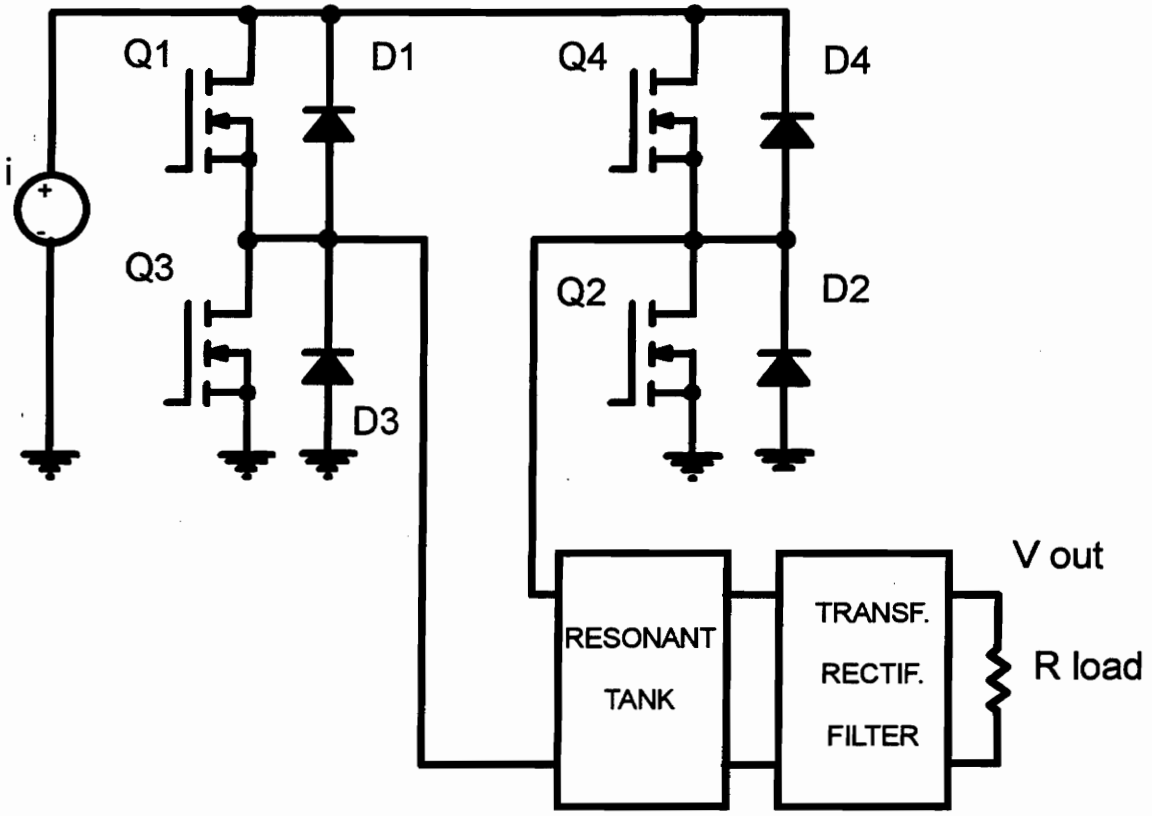


Figure 3.1: Phase-shifted resonant converter circuits topology.

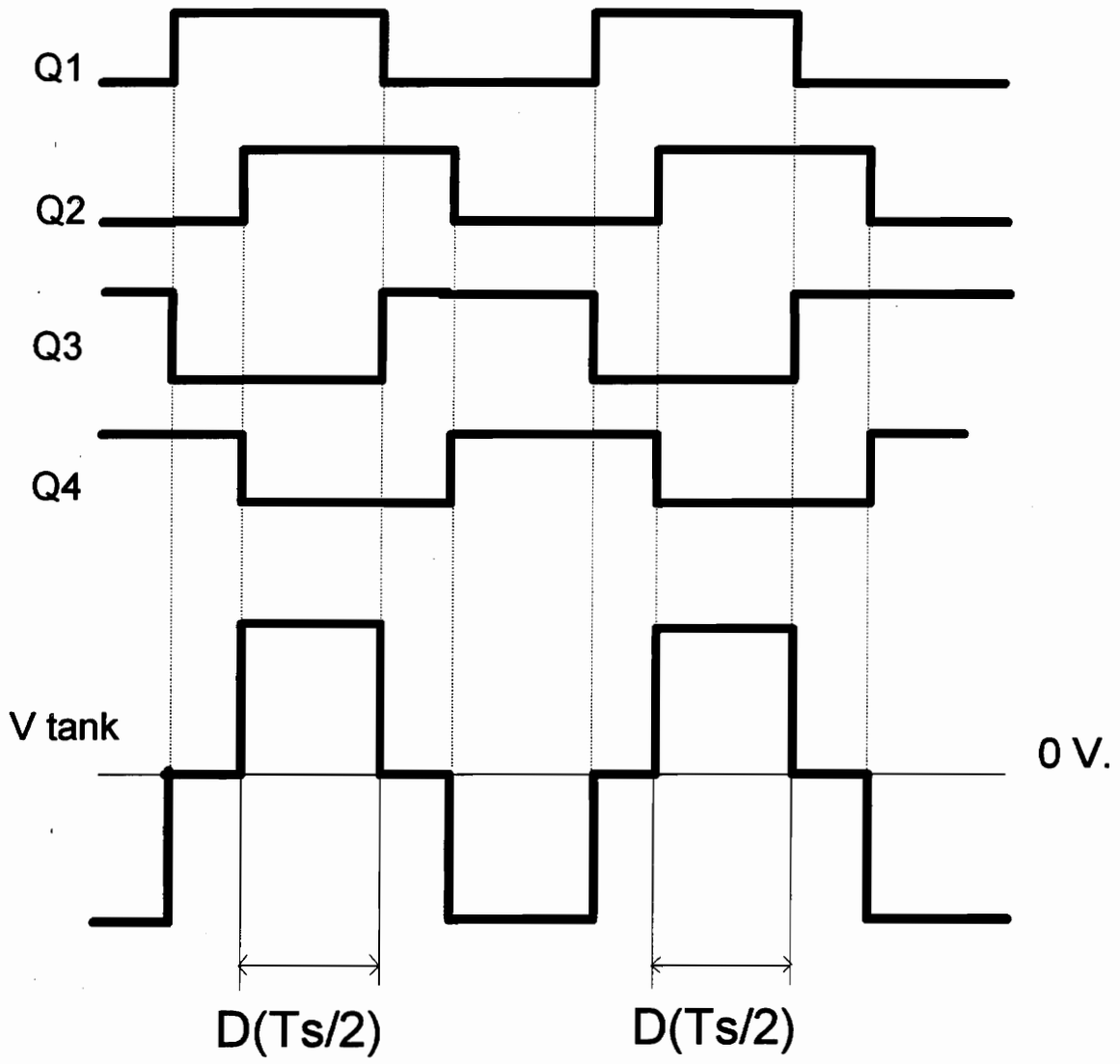


Figure 3.2: Switching waveforms and tank voltage.

3.3 Frequency-Domain Analysis of Phase-Shifted Resonant Converters

The simplified analysis presented in the previous chapter can also be applied to the phase-shift-controlled resonant converters. The inverter stage provides a quasi-square wave at the input of the tank, which can be expressed in Fourier series form as

$$v_{ac} = \frac{4}{\pi} \cdot \sum_{n=1,3..}^{\infty} \sin\left(n \cdot \frac{\pi}{2}\right) \cdot \sin\left(n \cdot \frac{\pi}{2} \cdot D\right) \cdot \frac{\sin(n \cdot \omega_s \cdot t)}{n} \tag{3.1}$$

Using only the fundamental component of the input to the tank, the gain of the converters corresponds to the gain of the resonant converter at the switching frequency selected times the factor that determines the fundamental of the input to the resonant tank as a function of the duty cycle:

$$M_{PS}(D, \omega_n, Q) = \sin\left(\frac{\pi}{2} \cdot D\right) \cdot M_{conv.}(\omega_n, Q), \tag{3.2}$$

where M_{ps} is the gain of the phase-shift-controlled resonant converter whose resonant tank has a frequency-dependent gain $M_{conv.}$. Figure 3.3 shows the relation between the two gains.

The phase-shift control modifies the input rms values of current and voltage to the tank and the output power as well. The power factor of the inverter stage load for the phase-shifted resonant converters can be calculated with the power factor of its

conventional converter counterpart at the switching frequency of operation selected for the phase-shift version times a factor function of the duty cycle. The relation between both can be expressed as:

$$P.F._{PS} = \frac{\sin\left(\frac{\pi}{2} \cdot D\right)}{\sqrt{D}} \cdot P.F._{conv.} \tag{3.3}$$

Figure 3.4 shows this factor. It is noteworthy to mention that the power factor is actually improved for duty cycles slightly lower than one. This can be attributed to a smaller amount of power returned to the source than in the square wave case.

3.4 Phase-Shifted Series Resonant Converter

The load current in a series resonant converter is the tank current, rectified and filtered. When the load current is reduced, so is the circulating current in the tank. At a certain point, the circulating current is not enough to keep the zero-voltage switching, and two of the switches are turned on with voltage [C-11,C-19,C-20].

The operation with zero-voltage switching is depicted in Fig. 3.5. The sequence of conduction for the devices is Q1-Q2, D3-Q2, D3-D4, Q3-Q4, D1-Q4, D1-D2. Every device starts conducting immediately after the diode in parallel with it conducts, so it turns on with virtually no voltage applied across it. However, when the pulse width decreases (Fig. 3.6), the conducting sequence is Q1-Q2, D3-Q2, Q3-D2, Q3-Q4, D1-Q4, Q1-D4. In this case, Q2 and Q4 are turned on with voltage, and conducting the reverse recovery current of diodes D4 and D2, respectively.

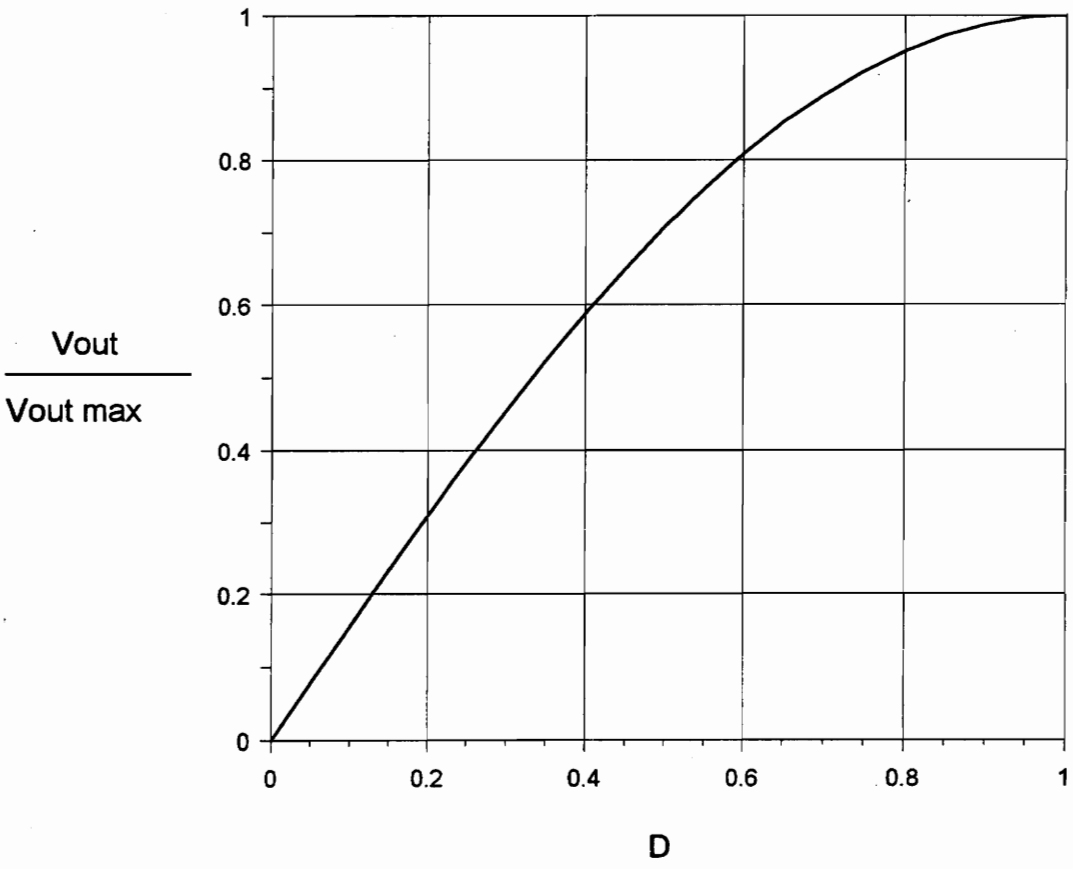


Figure 3.3: Ratio of the voltage gain with phase-shift control to the voltage gain with conventional resonant with respect to the duty cycle.

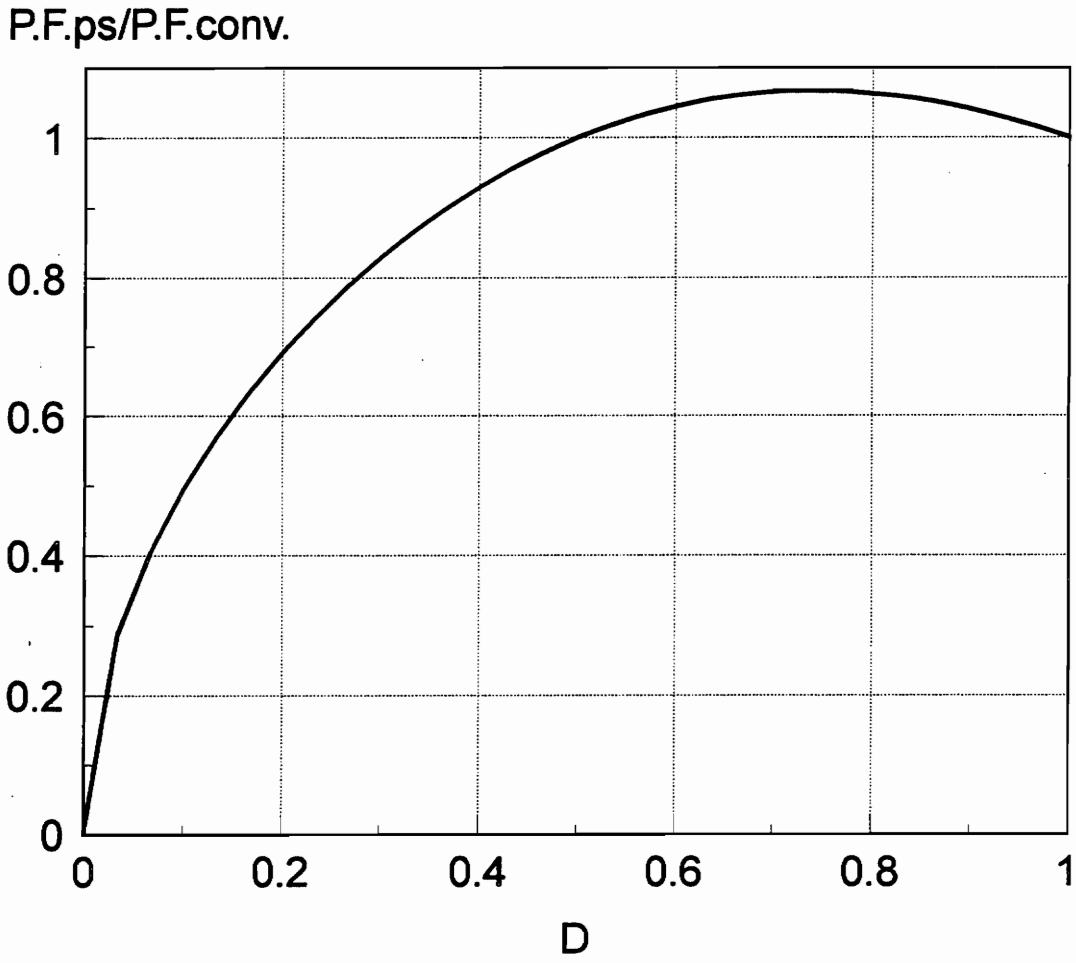


Figure 3.4: Ratio of the power factor with phase-shift control to the power factor with conventional resonant, with respect to the duty cycle.

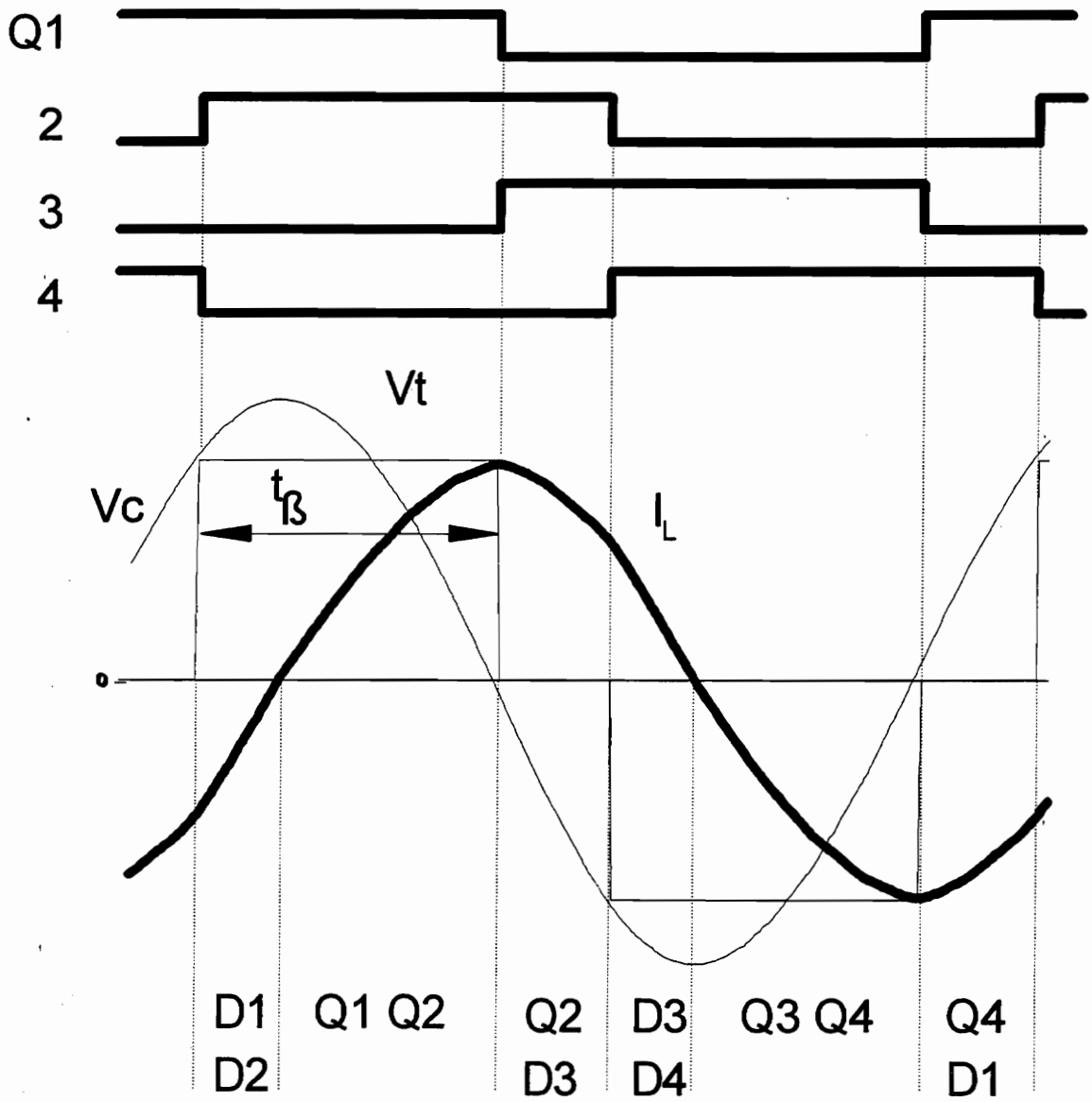


Figure 3.5: Tank voltage and current in the tank with zero-voltage switching.

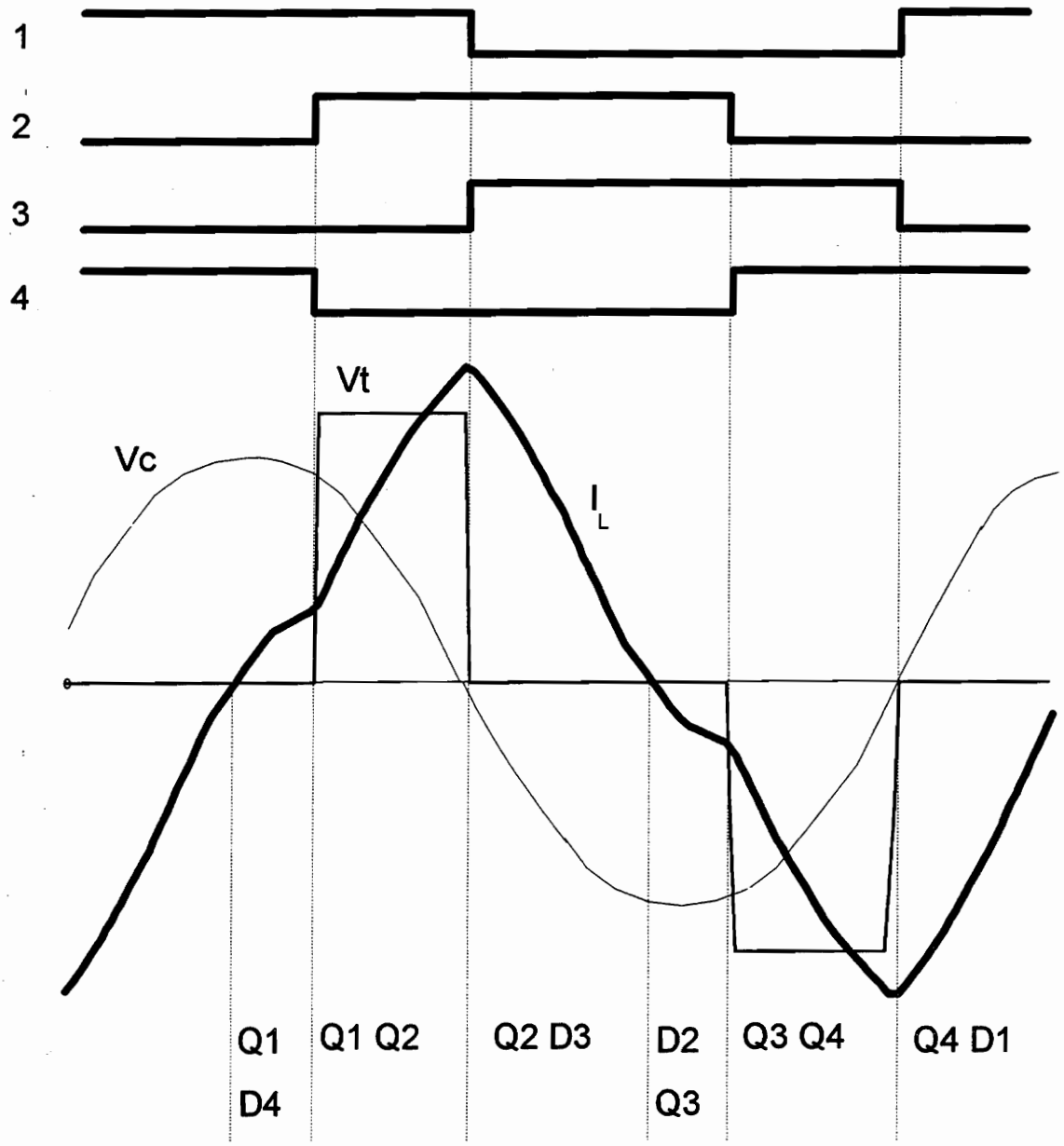


Figure 3.6: Tank voltage and current in the tank without zero-voltage switching.

However, they turn off naturally when the current through them becomes zero, and then the antiparallel diode of the other switch in the same bridge leg starts conducting.

The voltage gain of the phase-shift controlled series resonant converter can be calculated using Eqs. (3.3) and (2.12) as,

$$M_v(D,\omega_n,Q_s) = \frac{j\cdot\omega_n}{\frac{\pi^2}{8}\cdot Q_s\cdot\left(1-\omega_n^2\right)+j\cdot\omega_n}\cdot\sin\left(\frac{\pi}{2}\cdot D\right). \tag{3.4}$$

The zero-voltage-switching limit condition can be determined from the phase of the tank impedance and the duty cycle by:

$$\frac{\pi}{2}\cdot D \le \arg(Z_{in}) \tag{3.5}$$

where Z_{in} has been defined in Eq. (2.15) for the SRC.

The characteristics are normalized with the same parameters as the conventional resonant converters.

Figures 3.7 and 3.8 show the dc voltage gain when operating at switching frequencies 1.1 and 1.2 times the resonant frequency, respectively, indicating the region where the converter operates with ZVS. Figures 3.7 and 3.8 also show the results using the exact analysis [C-11]. The maximum voltage-gain error corresponds to the unity duty cycle, and this is the error in determining the voltage gain of the conventional SRC at the selected frequency (i.e. 1.1 and 1.2 times the resonant frequency in this case). The error becomes smaller for smaller duty cycles, and the voltage gain follows exactly the same pattern.

However, a significant error is observed in the prediction of the ZVS range. The approximated analysis shows that ZVS is lost at a higher duty cycle than it is at the one predicted by the exact analysis. The error becomes smaller for frequencies closer to the resonant frequency. In terms of general performance, both analyses show that the PS-SRC cannot operate from full load to no load with ZVS.

Using Eqs. (3.4), and (2.21). The power factor can be expressed as,

$$PF_{PS-SRC}(D,\omega_n,Q_p)=\frac{P_{out}}{S}=\frac{2\cdot\sqrt{2}}{\pi}M_v(\omega_n,Q_p)\cdot\frac{\sin\left(\frac{\pi}{2}\right)}{\sqrt{D}}. \quad (3.6)$$

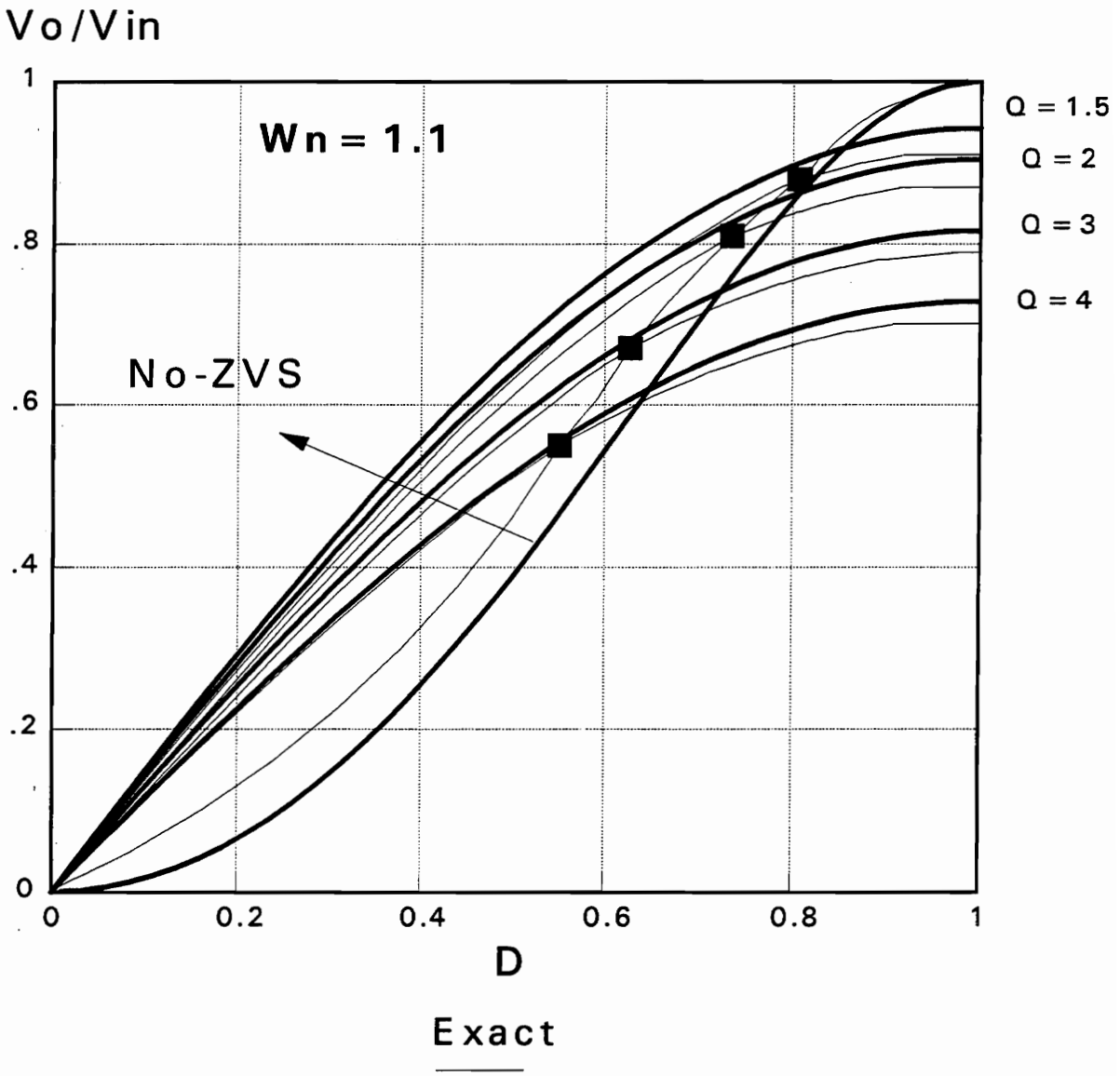


Figure 3.7: **DC voltage gain for the PS-series resonant converter for a switching frequency 1.1 times the resonant frequency, comparing exact analysis (thin lines) with fundamental approximation (thick lines).**

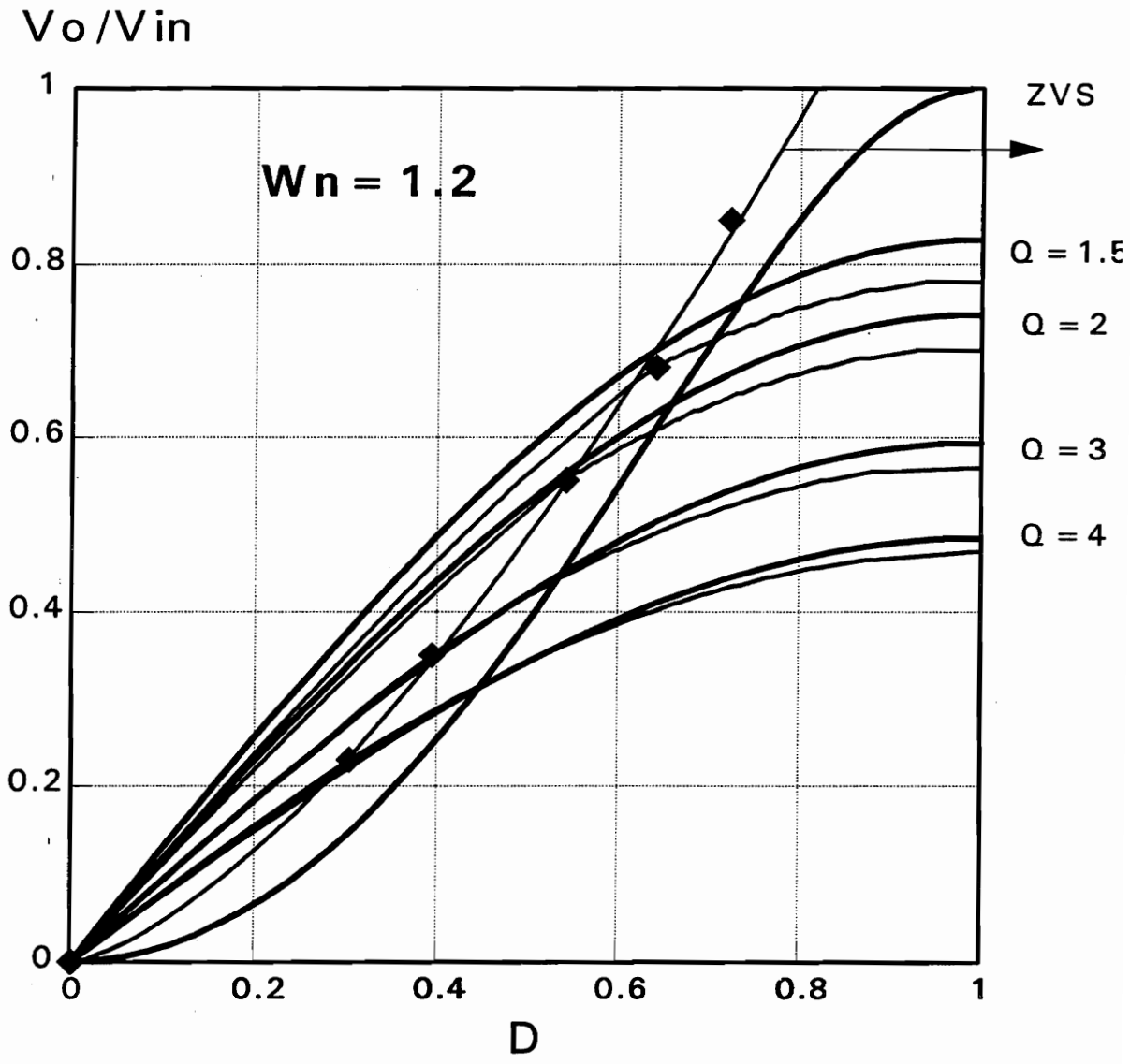


Figure 3.8: **DC voltage gain for the PS-series resonant converter for a switching frequency 1.2 times the resonant frequency, comparing exact analysis (thin lines) with fundamental approximation (thick lines).**

3.5 Phase-Shifted Parallel Resonant Converter

As for conventional resonant converters, the variation in load current does not strongly affect the circulating current through the tank. The consequence is that as the load current decreases and the pulse width becomes small, the converter can still retain zero-voltage switching for the active devices [C-18, C-20].

Figure 3.9 shows the typical operation waveforms for the phase-shifted parallel resonant converter. The sequence of operation is the same as for the series resonant when operating with zero-voltage switching (Q1-Q2, D3-Q2, D3-D4, Q3-Q4, D1-Q4, D1-Q2).

The voltage gain for the phase shifted PRC, using Eqs. (2.22) and (3.2), is,

$$M_v(\omega_n, Q_p) = \frac{Q_p}{\frac{\pi^2}{8}\cdot Q_p \cdot \left(1-\omega_n^2\right)+j\cdot\omega_n}\cdot \sin\left(\frac{\pi}{2}\cdot D\right) \tag{3.6}$$

The normalized dc voltage gain is presented in Figures 3.10 and 3.11, comparing exact and fundamental approximation analysis at frequencies 1.1 and 1.2 times the resonant frequency, respectively. The voltage-gain error has a maximum at unity duty cycle corresponding to that of the conventional PRC at this frequency.

The ZVS condition for the PS-PRC is the same as that one for the PS-SRC (Eq. (3.5)), except for using the input impedance defined for the PRC in Eq. (2.25). The approximate analysis error observed for the ZVS area is significant, as it was for the PS-

SRC. Also, the error is smaller for frequencies closer to the resonant frequency than at other frequencies.

The small region near the origin (closed dotted line) corresponds to the conditions where two of the switches lose zero-voltage switching. This small region only exists for operating frequencies ω_n=1.2 or lower. The phase-shifted parallel resonant converter can always be designed to operate from full load to no load with zero-voltage switching. It is necessary only to keep a circulating current through the tank almost constant at any load. This last fact is responsible for low partial-load efficiency, but it is less harmful for the reliable operation of the circuit than the loss of zero-voltage switching, as can be seen in the experimental results.

Using Eqs. (3.3), and (2.30). The power factor can be expressed as,

$$PF_{PS-PRC}(D,\omega_n,Q_p)=\frac{P_{out}}{S}=\frac{\pi}{2\cdot\sqrt{2}}M_v(\omega_n,Q_p)\cdot\frac{1}{1+j\cdot\omega_n\cdot\frac{\pi^2}{8}\cdot Q_p}\cdot\frac{\sin\left(\frac{\pi}{2}\right)}{\sqrt{D}}. \quad (3.7)$$

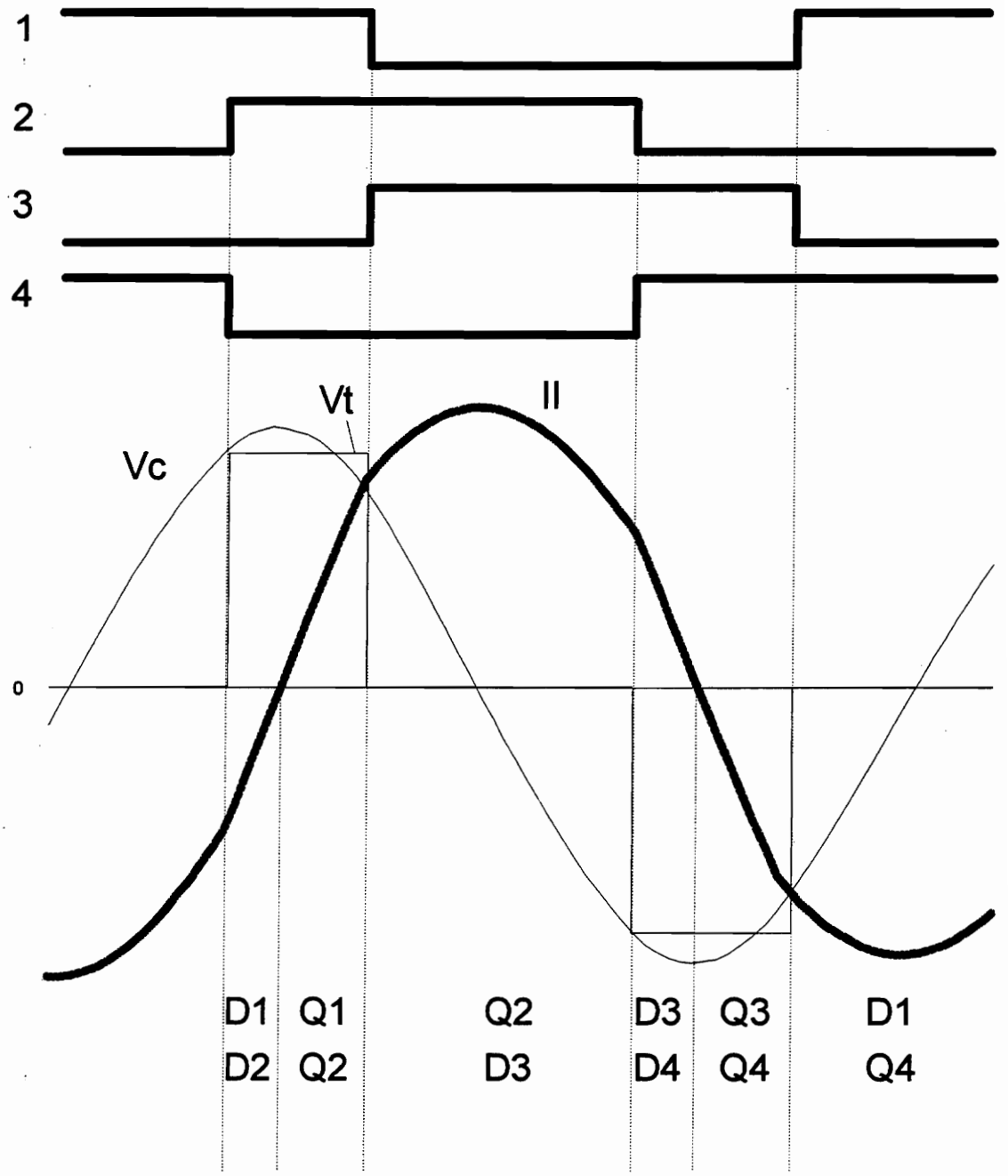


Figure 3.9: **Tank voltage and inductor current for the PS-parallel resonant converter.**

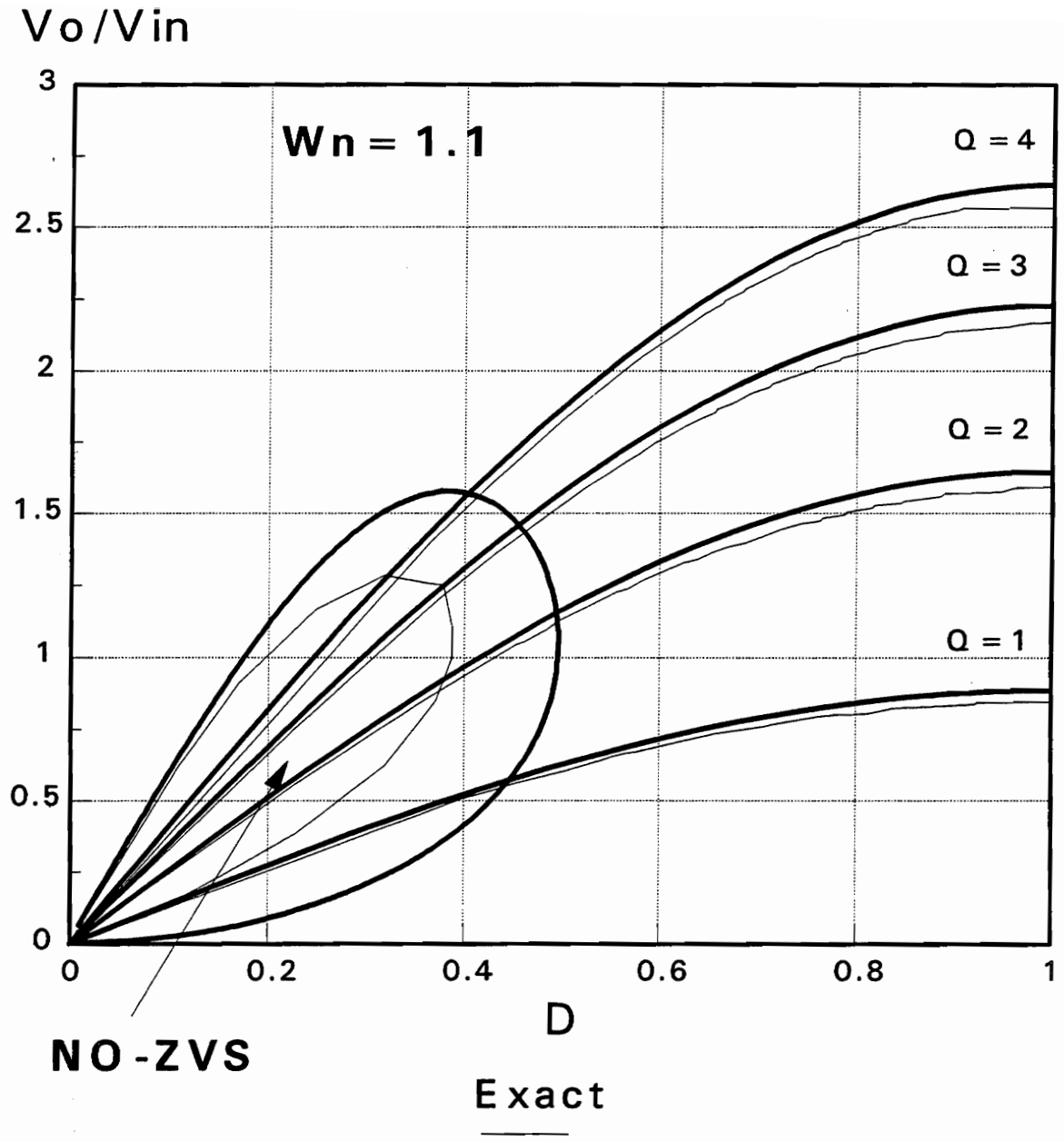


Figure 3.10: DC voltage gain for the PS-PRC at 1.1 times the resonant frequency, comparing exact analysis (thin lines) with fundamental approximation (thick lines).

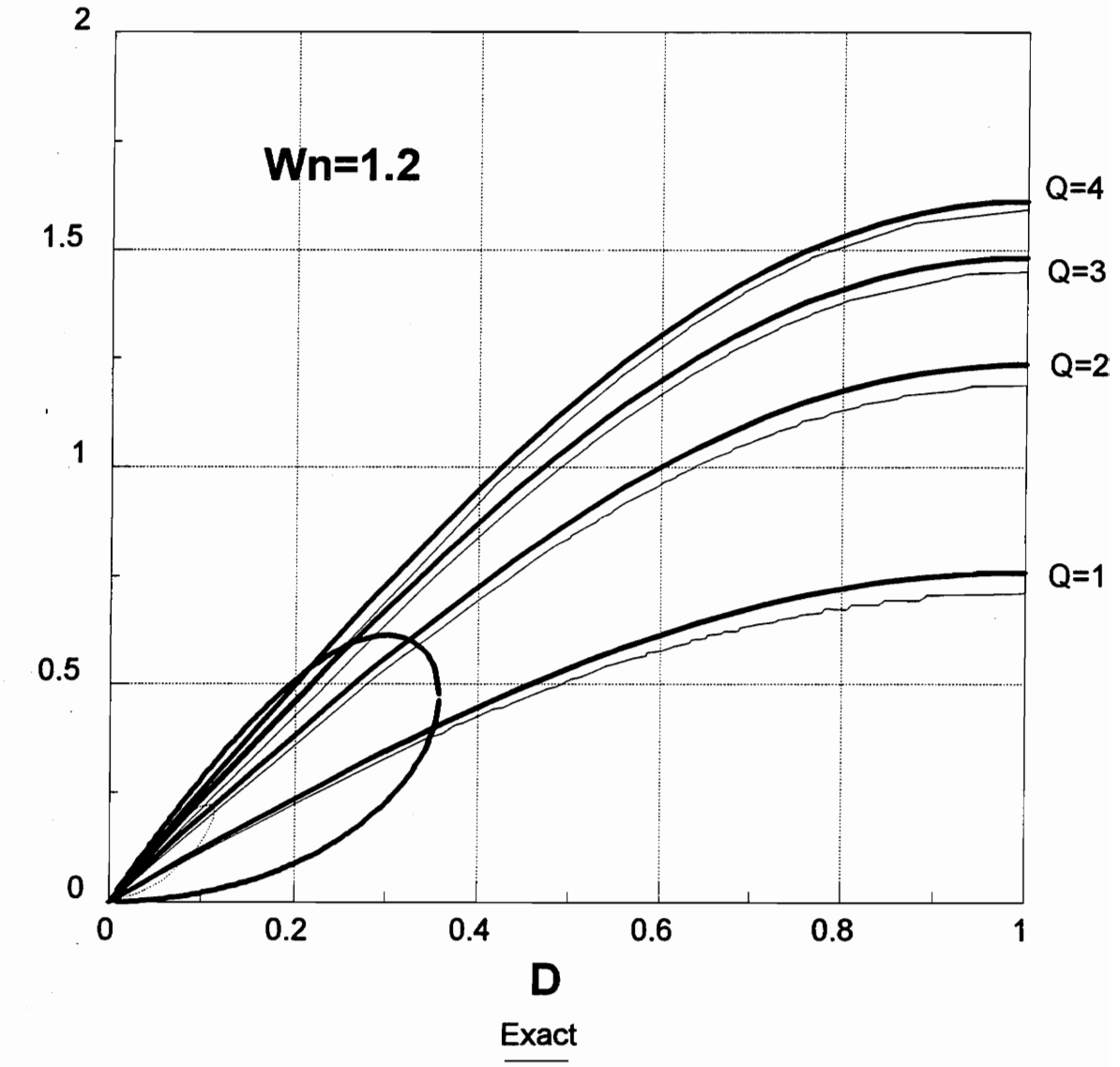


Figure 3.11: DC voltage gain for the PS-PRC at 1.2 times the resonant frequency, comparing exact analysis (thin lines) with fundamental approximation (thick lines).

3.6 Phase-Shifted LCC Resonant Converter

As for the PS-PRC, the variation in load current does not strongly affect the circulating current through the tank. The consequence is that as the load current decreases and the pulse width becomes small, the converter can still retain zero-voltage switching for the active devices [C-18, C-20].

The typical operation waveforms for the phase-shifted LCC resonant converter are the same as those corresponding to the PS-PRC and PS-SRC. The sequence of operation is the same as for the series resonant when operating with zero-voltage switching (Q1-Q2, D3-Q2, D3-D4, Q3-Q4, D1-Q4, D1-Q2).

The voltage gain for the phase shifted LCC, using Eqs. (2.45) and (3.2), is

$$M_v(\omega_n, Q_p, C_n) = \frac{j\cdot\omega_n\cdot Q_p\cdot\left(1+\frac{1}{C_n}\right)}{1-\omega_n^2\cdot\left(1+\frac{1}{C_n}\right)+j\cdot\omega_n\cdot\frac{\pi^2}{8}\cdot Q_p\cdot\frac{(1+C_n)^2}{C_n}\cdot\left(1-\omega_n^2\right)}\cdot\sin\left(\frac{\pi}{2}\cdot D\right) \tag{3.8}$$

The voltage gain versus the duty cycle for different loads is presented for different capacitance ratios in Figs. 3.12-3.15 for frequencies 1.2, 1.1 and 1.0 times the resonant frequency.

The ZVS condition for the PS-LCC is the same as that for the PS-SRC and PS-PRC (Eq. (3.5)), but using for input impedance the input impedance of the LCC-RC defined in Eq. (2.48).

For frequencies larger than the resonant frequency the small region close to the origin (closed dotted line), corresponds to the conditions where two of the switches lose zero-voltage switching.for frequencies larger than the resonant frequency. This region is smaller than for the PS-PRC at the same frequency because the LCC resonant converter achieves ZVS at frequencies lower than the resonant frequency for higher Q's than the PRC. The voltage gain courves at the resonant frequency show a ZVS range similar the one for the PS-SRC. The voltage gain courves show the intermediate behavior between the SRC and PRC. However, the PS-LCC resonant converter can be designed to operate from full load to no load with zero-voltage switching is a proper frequency is chosen, while the PS-SRC can never work with ZVS from full load to no load.

Using Eqs. (3.3) and (2.52), the power factor can be expressed as

$$PF_{PS-LCC}(D,\omega_n,Q_p,C_n)=\frac{P_{out}}{S}=\frac{\pi}{2\cdot\sqrt{2}}M_v(\omega_n,Q_p,C_n)\cdot\frac{1}{1+j\cdot\omega_n\cdot\frac{\pi^2}{8}\cdot Q_p}\cdot\frac{\sin\left(\frac{\pi}{2}\right)}{\sqrt{D}} \tag{3.9}$$

The performance of the PS-LCC is expected to correspond to a combination of the properties of the PS-SRC and PS-PRC, and this will be shown in the design examples at the end of this chapter.

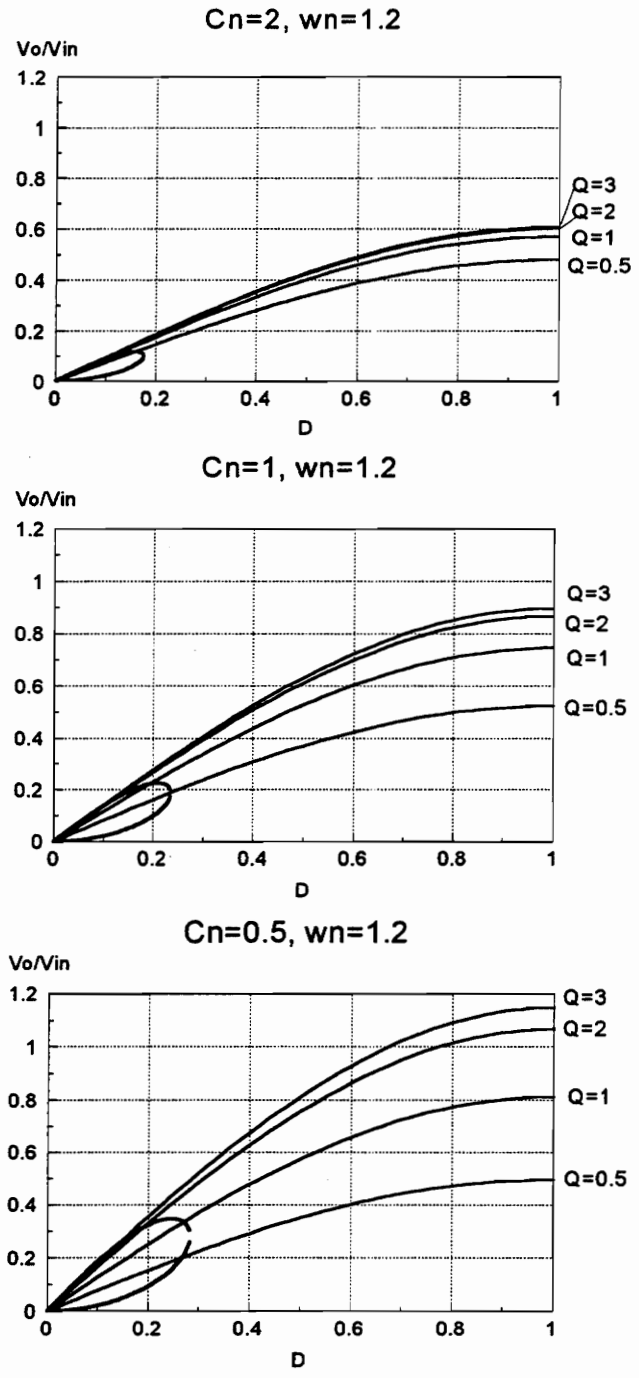


Figure 3.12: DC voltage gain for the PS-LCC resonant converter for a switching frequency 1.2 times the resonant frequency, for C_n = 2, 1, and 0.5, respectively.

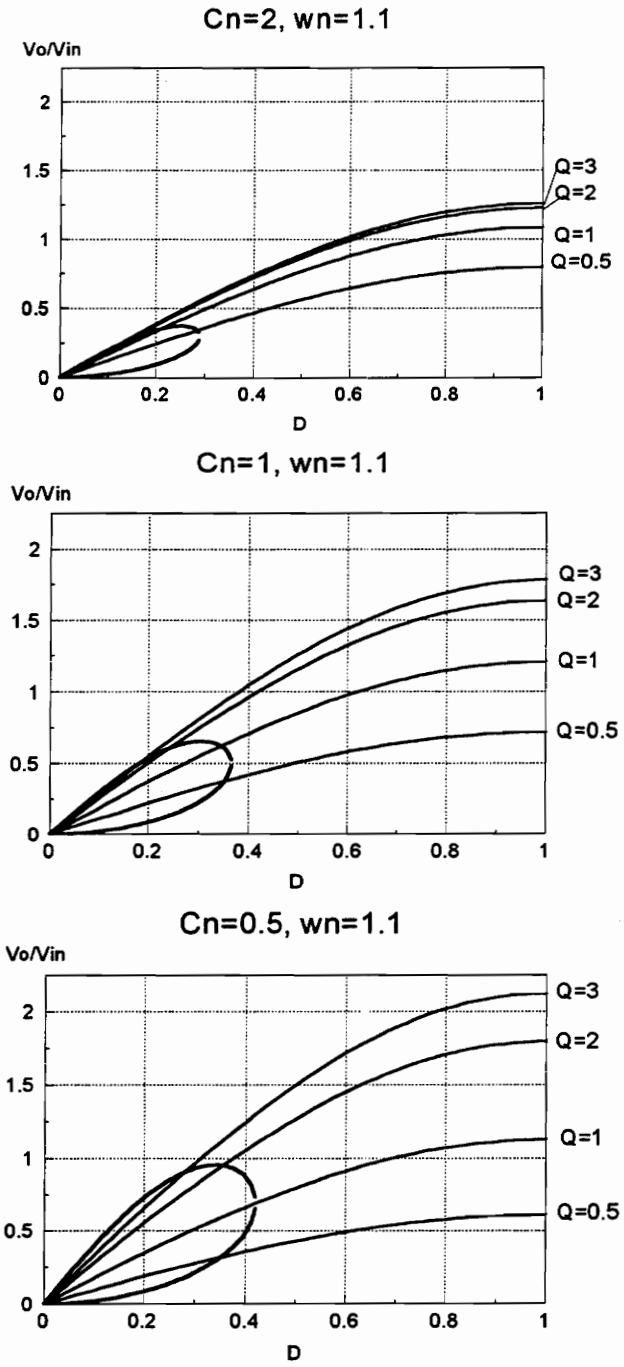


Figure 3.13: DC voltage gain for the PS-LCC resonant converter for a switching frequency 1.1 times the resonant frequency, for C_n = 2, 1, and 0.5, respectively.

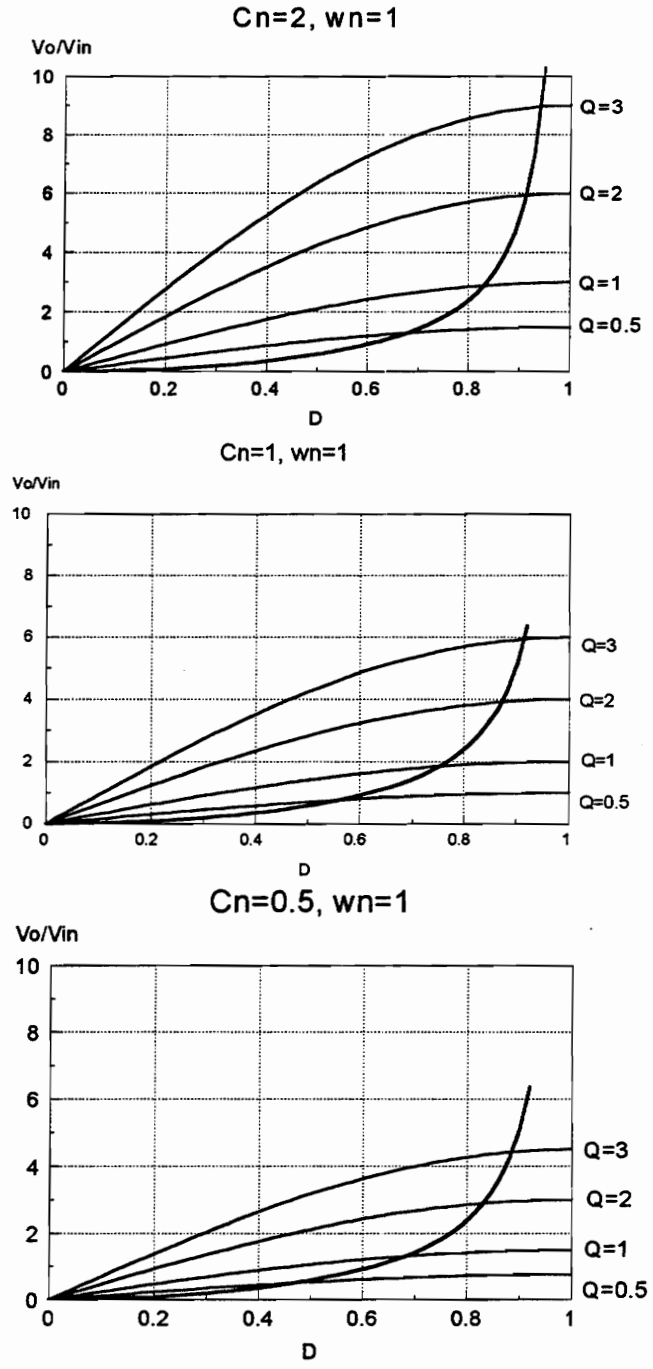


Figure 3.14: DC voltage gain for the PS-LCC resonant converter for a switching frequency equal to the resonant frequency, for C_n = 2, 1, and 0.5, respectively.

3.7 Comparison of Phase-Shifted SRC and PRC

3.7.1 Design Objectives

In order to compare the phase-shifted parallel and series resonant converters, two prototypes have been designed with the following specifications:

Input voltage range 200 to 300 V.

Output voltage 5 V.

Output power 100 W.

Switching frequency 500 kHz range.

The comparison of the two designs shows the difference in load range with zero voltage. The implementation of the designs as breadboard prototypes verifies the conclusions of the analysis and permits a comparison of the loss breakdown.

3.7.2 Design of a Series Resonant Converter

The operation with zero-voltage turn-on for the active switches also provides natural turn-off for the diodes. Then there is no need to use fast-recovery diodes and the internal diodes of the MOSFET's can be used. The power stage is shown in Fig. 3.15.

In order to avoid losing zero-voltage switching, the value of Q at full load has to be as high as possible, and the converter has to operate sufficiently above the resonant frequency. However, large values of Q result in large circulating currents (low power factor), as has been shown for the conventional SRC, and, to also avoid large circulating currents the switching frequency has to be close to the resonant frequency.

A feasible switching frequency to provide enough ZVS margin and to avoid excessive circulating currents was found to be ω_n=1.2. The Q at maximum load was chosen to be 3.5. Figure 3.16 shows the operating region for the voltage gain, and the power factor of the resonant tank.

The maximum duty cycle obtainable with the control logic circuit used is 0.8. The Q selected for full load is the smallest Q that provides the desired voltage gain for the maximum duty cycle. The voltage gain 0.5 was selected because it is the value at which maximum power can be transferred to the load, according to previous studies of the series resonant converter [A-14]. The minimum voltage gain (for high-input voltage) is 0.35. The minimum value of duty cycle for which ZVS is achieved at full load is 0.4 for low line, and 0.5 for high line. These ZVS limits correspond to a minimum load of 86 W at high line and 60 W at low line.

Then, the transformer turns ratio is calculated by

$$n = \frac{M_{max} \cdot V_{in,min}}{V_{out} + V_{diode}} = 18 \text{ turns} .$$

The other circuit parameters are calculated by

$$Z_o = Q_{max} \cdot R_{out} \cdot n^2 = 306\ \Omega \text{ and } f_s = 1.2 \cdot f_o = 557 \text{ kHz}$$

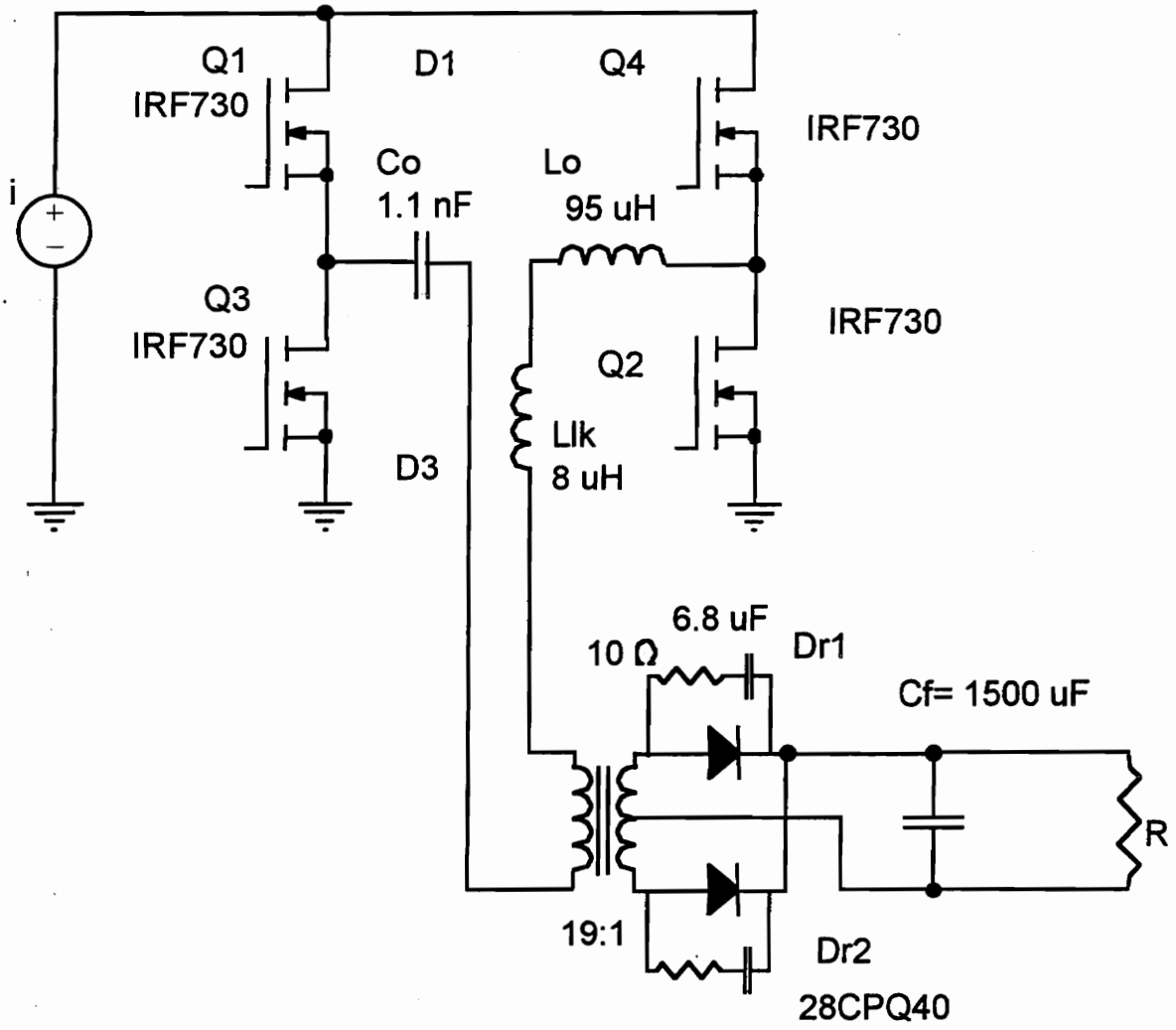


Figure 3.15: Circuit for the PS-SRC above resonant frequency.

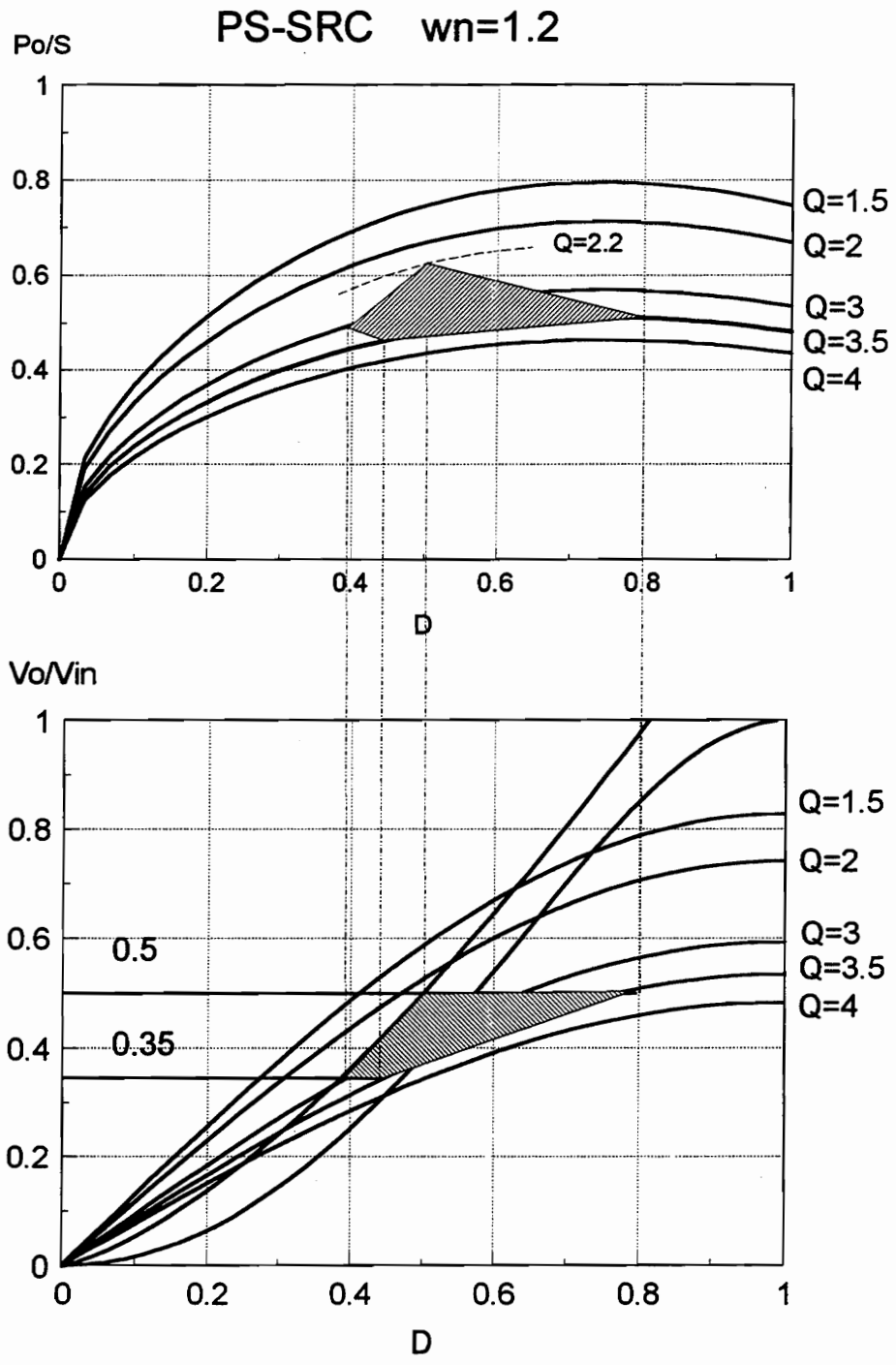


Figure 3.16: Operating region for the PS-SRC design.

Figure 3.16 shows the power factor of the operating region. The power factor is less than 0.5, so the currents at the input of the resonant tank are larger than the values obtained in chapter 2 for conventional resonant converters. The main reason for the low power factor is the high frequency of operation selected (1.2 f_0).

3.7.3 Design of a Parallel Resonant Converter

As a basis for comparison, the power stage uses the same active components (MOSFETs and diodes) used for the PS-SRC. The switching frequency is also selected the same as for the PS-SRC case ($1.2 \cdot f_0$). However, the PS-PRC can be designed to operate from full load to no load with zero-voltage switching. The zero-voltage switching allows the use of the internal diodes of the MOSFETs. The circuit used is presented in Fig. 3.17.

The minimum Q is chosen to be 1.67 which gives a gain of M=1 for D=0.8. The corresponding values at high line are M=0.66 and D=0.44. Then, the transformer turns ratio is calculated by

$$n = \frac{M_{max} \cdot V_{in,min}}{V_{out} + V_{diode}} = 36 \text{ turns} .$$

The other circuit parameters are calculated by

$$Z_0 = \frac{R_{out} \cdot n^2}{Q_{min}} = 202\ \Omega \text{ and } f_s = 1.2 \cdot f_0 = 557 \text{ kHz}$$

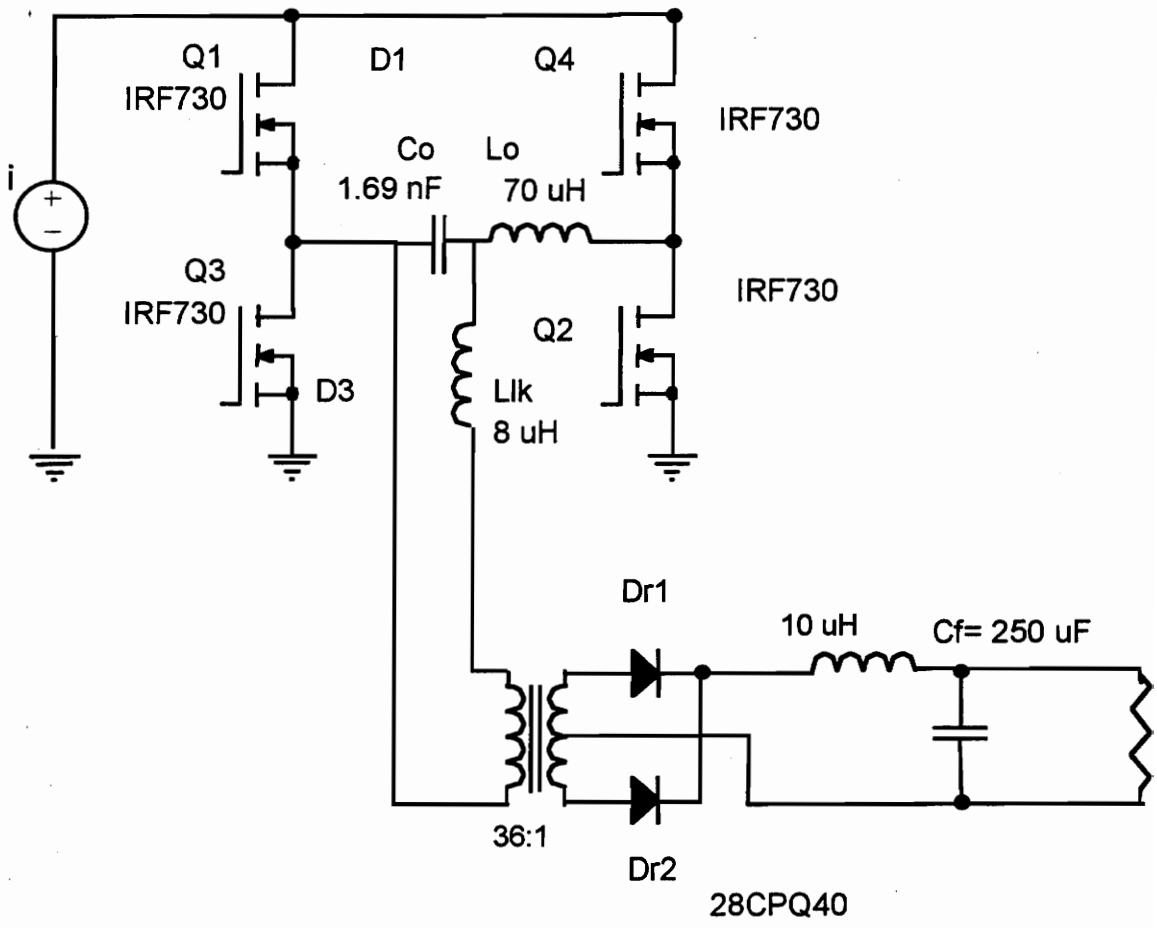


Figure 3.17: Circuit for the PS-PRC design.

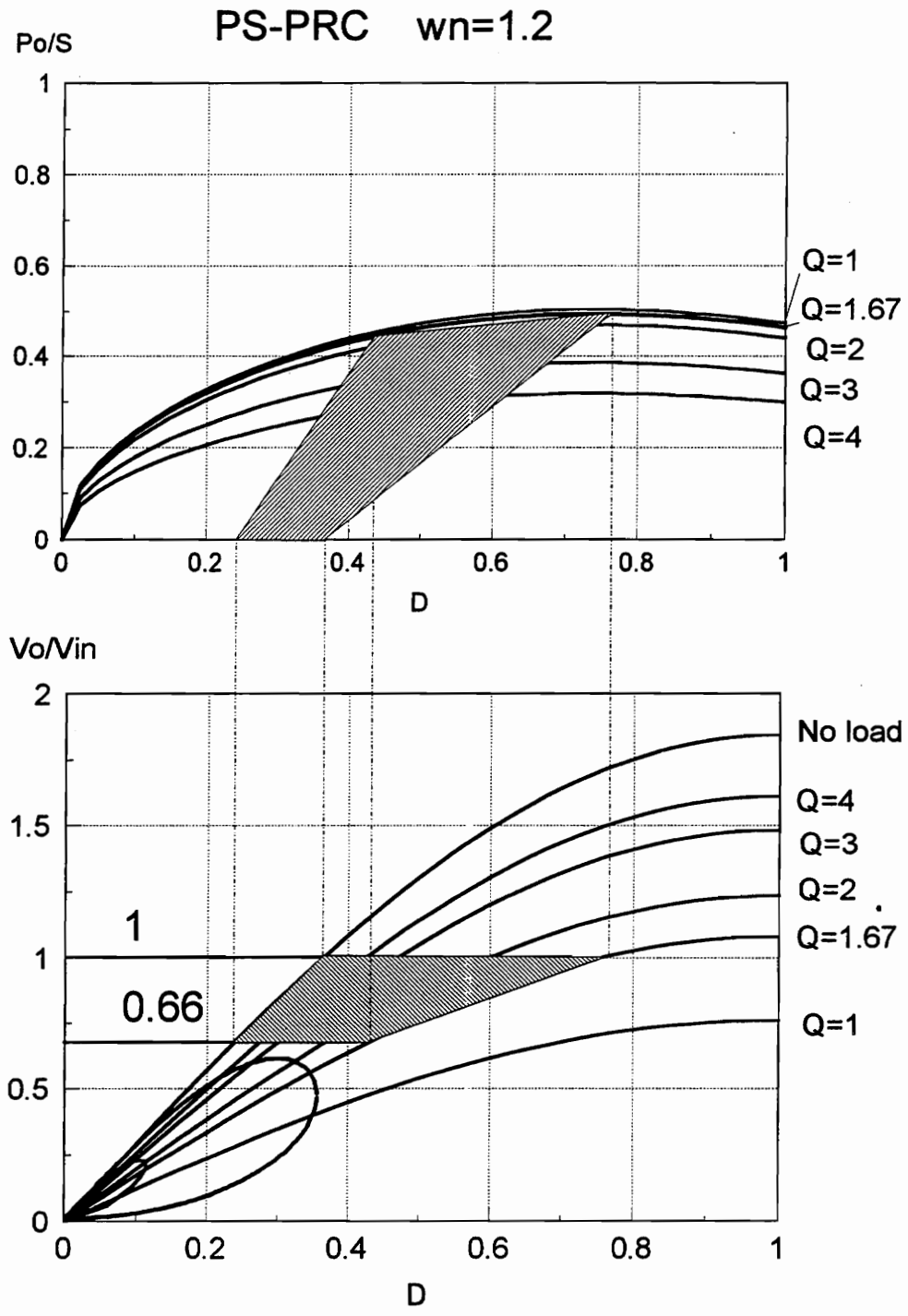


Figure 3.18: Operating region for the PS-parallel resonant converter design.

The operating region is shown in Fig. 3.18. The maximum power factor for this design is close to that of the PS-SRC design. Consequently, the currents at the input of the resonant tank are very similar to those for the PS-SRC. However, for this design ZVS is achieved from full load to no load. A more advantageous design is possible for the PS-PRC. An optimized design and comparison with the PS-LCC converter are provided in the next section.

3.7.4 Experimental Results

The experimental circuits were built using the values calculated in Sects. 3.7.2 and 3.7.3. The duty cycle required was found to be larger than expected according to the ideal model characteristics. The tank and switching loss have a damping effect, which requires larger current and larger duty cycles.

The maximum load current for the PS-SRC for low line with the maximum duty cycle was found to be 18 A. Also, for high line (300 V) and 18 A output current, the PS-SRC loses zero-voltage switching. This can be seen with the decrease of the efficiency due to the switching losses (Fig. 3.19).

Figure 3.19 shows the efficiency versus load current for both converters at low and high line, respectively. It can be seen that efficiency deteriorates dramatically when the zero-voltage switching is lost for the PS-SRC, although the current through the tank is decreasing. This is due to the reverse recovery of the internal diodes of the MOSFET's when the zero-voltage switching is lost. The efficiency reduction observed for the PS-PRC is due to the large circulating current at partial loads.

The efficiency of the circuit was measured for the operation between full load and the minimum load, which corresponds to the area below the boundary of zero-voltage switching for the PS-SRC, provided that the switching loss was below the maximum power dissipation allowed in the devices.

The efficiency of the PS-PRC decreases rapidly at partial loads because the tank current remains practically constant. As can be seen in the operating region the power factor for the PS-PRC goes to zero at no load, and consequently it has much larger currents at low loads than the PS-SRC.

Figures 3.20 shows the waveforms for the PS-SRC at full load for high and low line. Figure 3.21 shows the waveforms for the PS-PRC at full load for high and low line conditions, and Fig. 3.22 shows the waveforms at no load for the PS-PRC. The waveforms show the ZVS operation in all cases.

The maximum efficiency obtainable in both cases is almost the same, but the performance of the PS-PRC is superior for two reasons:

- The PS-PRC can achieve ZVS from full load to no load, and
- PS-PRC is more efficient at high line than the PS-SRC, since for the PS-PRC, the input current to the tank changes less over the line variations.

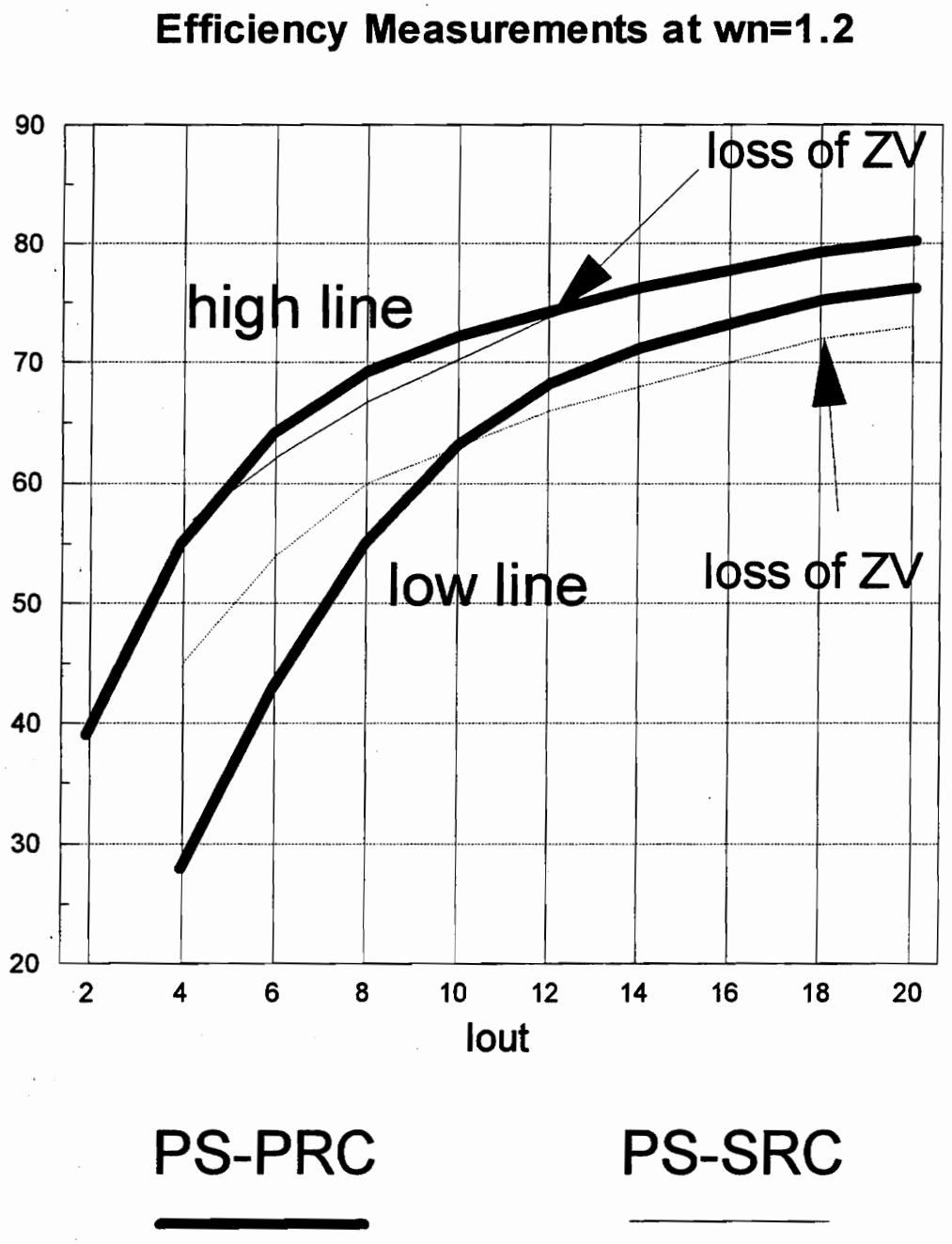
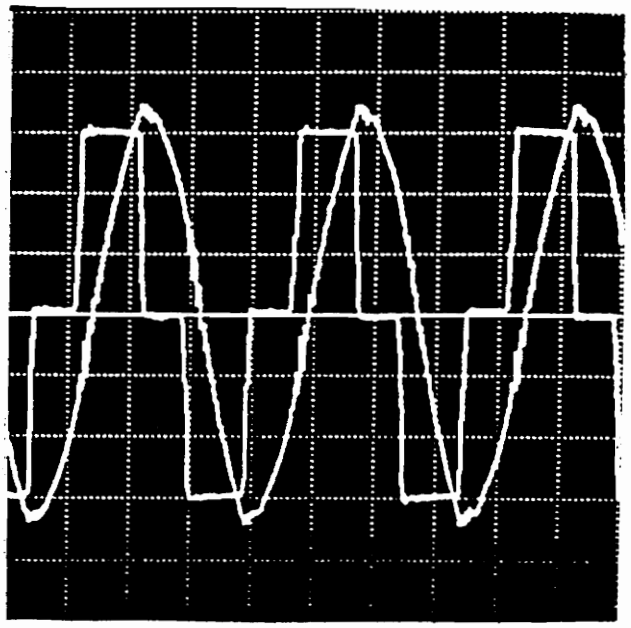


Figure 3.19: Measured efficiency for the PS-PRC (thick lines) and for the PS-SRC (thin lines), for high-line and low line-cases.

Full load, High Line



Full load, Low line

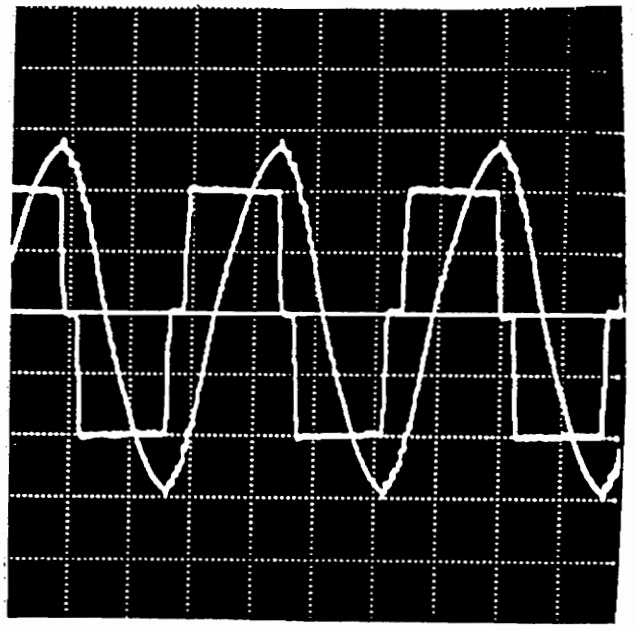
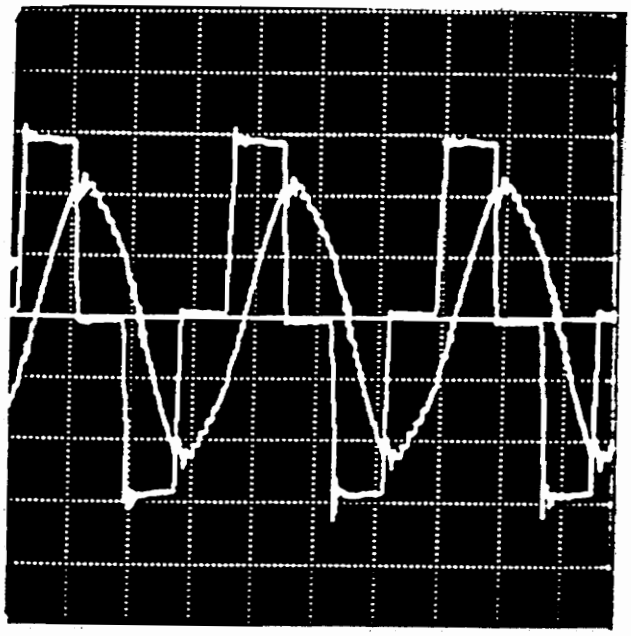


Figure 3.20: Tank voltage and inductor current for the PS-SRC. (Scales: voltage 100 V/div., current 0.5 A/div., time 500 nsec./div.).

Full load, High Line



Full load, Low line

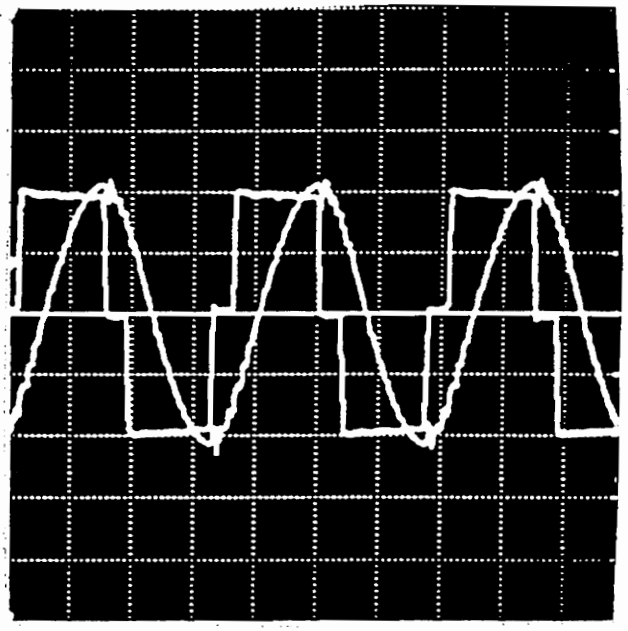


Figure 3.21: Tank voltage and inductor current for the PS-PRC. (Scales: voltage 100 V/div., current 1 A/div., time 500 nsec./div.).

No load

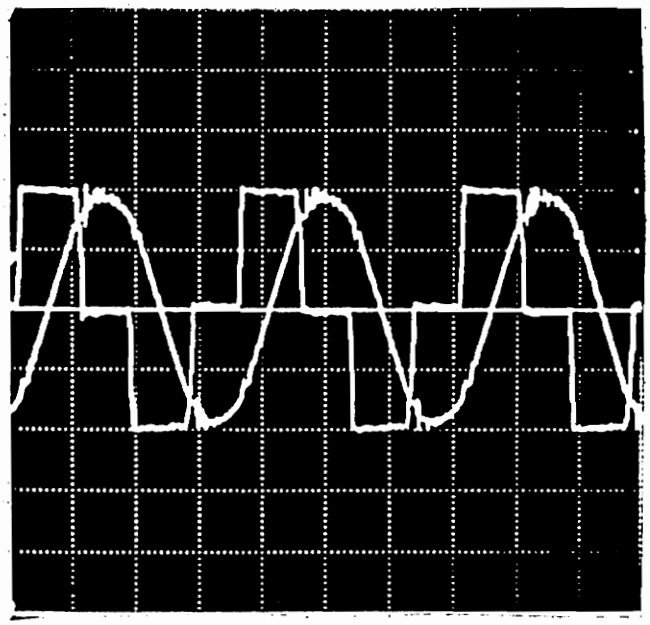


Figure 3.22: Tank voltage and inductor current for the PS-PRC at low line, no load condition. (Scales: voltage 100 V/div., current 0.5 A/div., time 500 nsec./div.).

3.8 Comparison of PS-PRC and PS-LCC Resonant Converter

The performances of the PS-PRC and PS-LCC resonant converters are compared using several designs for the same specifications used in the previous section. The PS-SRC is not considered here because is has been determined that it has worse performance than the PS-PRC in terms of efficiency, and also the PS-SRC cannot achieve ZVS from no load to full load, while the PS-PRC and PS-LCC can.

Using the voltage gain for the PS-LCC shown in Figs. 3.12 and 3.13 and the voltage gain for the PS-PRC shown in Figs. 3.10 and 3.11, for $\omega_n = 1.1$ and $\omega_n = 1.2$, respectively. Several designs are considered for the PS-PRC and PS-LCC with $C_n = 2$, 1, and 0.5. The converters have been designed to operate with ZVS from full load to no load, and for a maximum duty cycle of 0.9. The minimum gain to achieve full-load range ZVS is used in each case, because it results in the minimum Q. The lowest Q for the frequencies considered corresponds to the minimum input current to the resonant tank.

Figures 3.23, 3.25, 3.27, and 3.29 show the inductor current, the voltage gain and the power factor as a function of the frequency, indicating the values corresponding to the frequencies selected for the phase-shifted designs. These figures show the maximum power factor achievable for each design, and the input current to the tank normalized with respect to P_{out}/V_{in}. Figures 3.24, 3.26, 3.28, and 3.30 show the voltage gain operating

operating regions foe each design with respect to the duty cycle, these figures illustrate the selection of Q for ZVS operation over the whole load and input voltage range, and the required duty cycle variation. Table 3.1 summarizes the designs parameters.

The values of input current to the resonant tank are calculated with Eqs. (2.28), and (2.50) for the PS-PRC and PS-LCC, respectively.

The performance of the PS-PRC is better than that of the PS-LCC. This is because the PS-PRC requires less reactive power at full load than the PS-LCC to retain ZVS over the whole range of operation. The best design for the PS-PRC has a power factor of 0.58, while the best design for the PS-LCC has a power factor of 0.55

The duty-cycle variation at full load for the designs presented is from 0.9 at low line to 0.458 at high line. The variation of power factor from low line to high line can be calculated using Eqs. (3.7) and (3.9) as,

$$P.F_{\cdot low-line} = P.F_{\cdot high-line} \cdot \frac{\sin\left(\frac{\pi}{2} \cdot D_{high-line}\right)}{\sin\left(\frac{\pi}{2} \cdot D_{low-line}\right)} \cdot \sqrt{\frac{D_{low-line}}{D_{high-line}}}, \qquad (3.10)$$

resulting in a variation of 1.07.

The designs result in input currents to the tank higher than for the conventional resonant converters design presented in Figs. 2.45-2.48. This is because the choice of Q to achieve ZVS over the whole line range forces the converter to require more reactive power. This results in input currents larger than those of the conventional resonant converter.

Table 3.1: Designs for the PS-PRC and PS-LCC Resonant Converter

Converter			ω_n=1.1	ω_n=1.2
PS-PRC	Min. Voltage gain		1.6	0.65
	Min. Q (full load)		3.4	1.4
	N_p/N_s		96	39
	Input current	low line	1.79	2.13
	$\div(P_{out}/V_{in})$	high line	2.68	3.2
	Power factor	low line	0.58	0.5
	at full load	high line	0.56	0.46
PS-LCC	Min. Voltage gain		1	0.4
C_n =0.5	Min. Q (full load)		1.5	0.64
	N_p/N_s		60	24
	Input current	low line	1.93	2.62
	$\div(P_{out}/V_{in})$	high line	2.89	3.93
	Power factor	low line	0.55	0.40
	at full load	high line	0.51	0.38
PS-LCC	Min. Voltage gain		0.65	0.25
C_n =1	Min. Q (full load)		0.741	0.327
	N_p/N_s		39	15
	Input current	low line	2.1	3.34
	$\div(P_{out}/V_{in})$	high line	3.12	5.01
	Power factor	low line	0.51	0.32
	at full load	high line	0.48	0.3
PS-LCC	Min.Voltage gain		0.4	0.15
C_n =2	Min. Q (full load)		0.34	0.15
	N_p/N_s		24	9
	Input current	low line	2.57	4.89
	$\div(P_{out}/V_{in})$	high line	3.85	7.34
	Power factor	low line	0.41	0.22
	at full load	high line	0.38	0.2

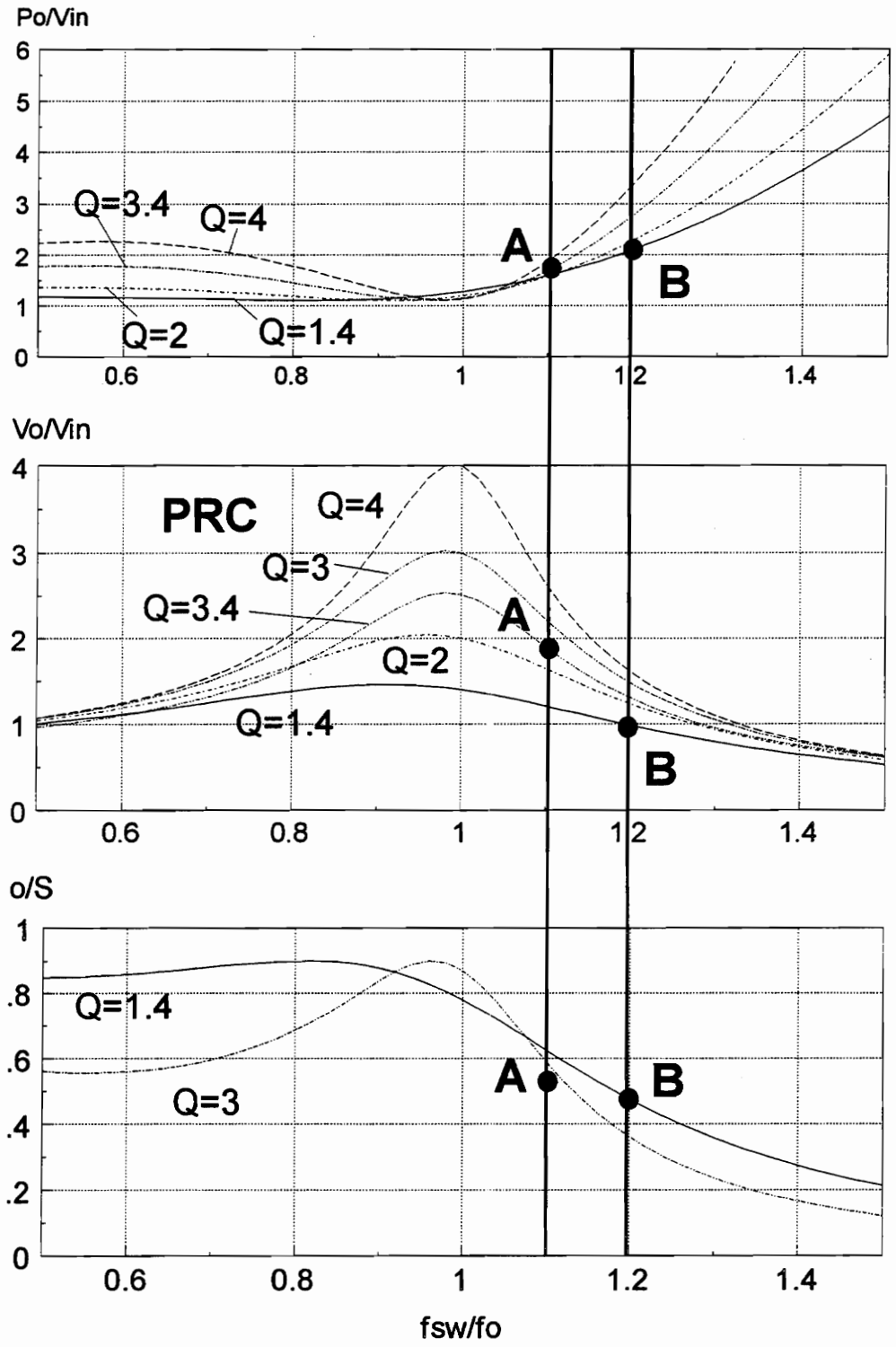
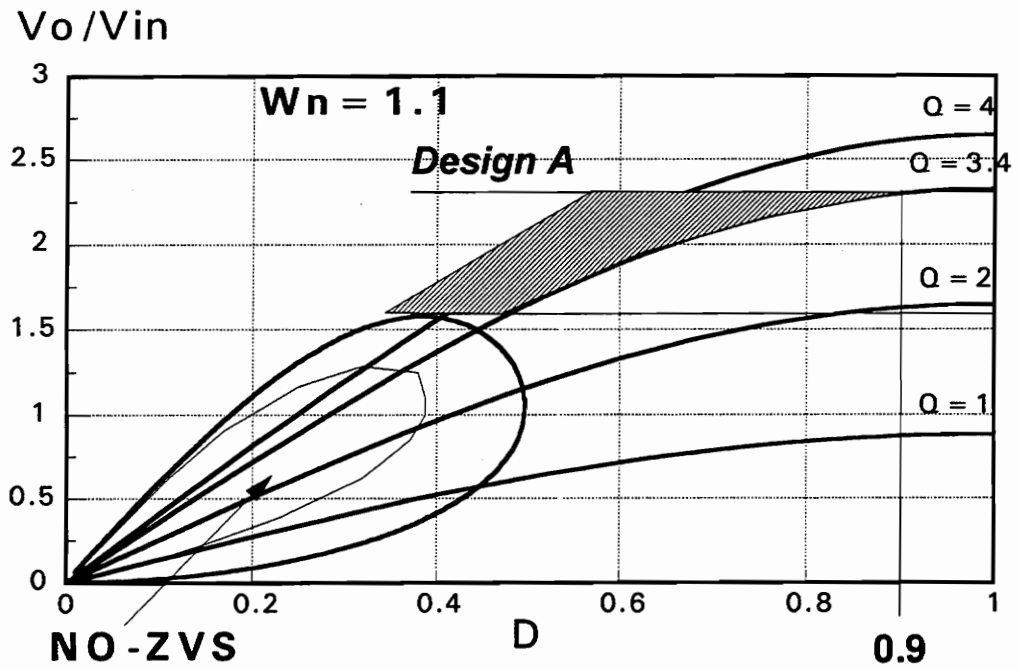


Figure 3.23: Designs for the PS-PRC, frequencies of operation selected.



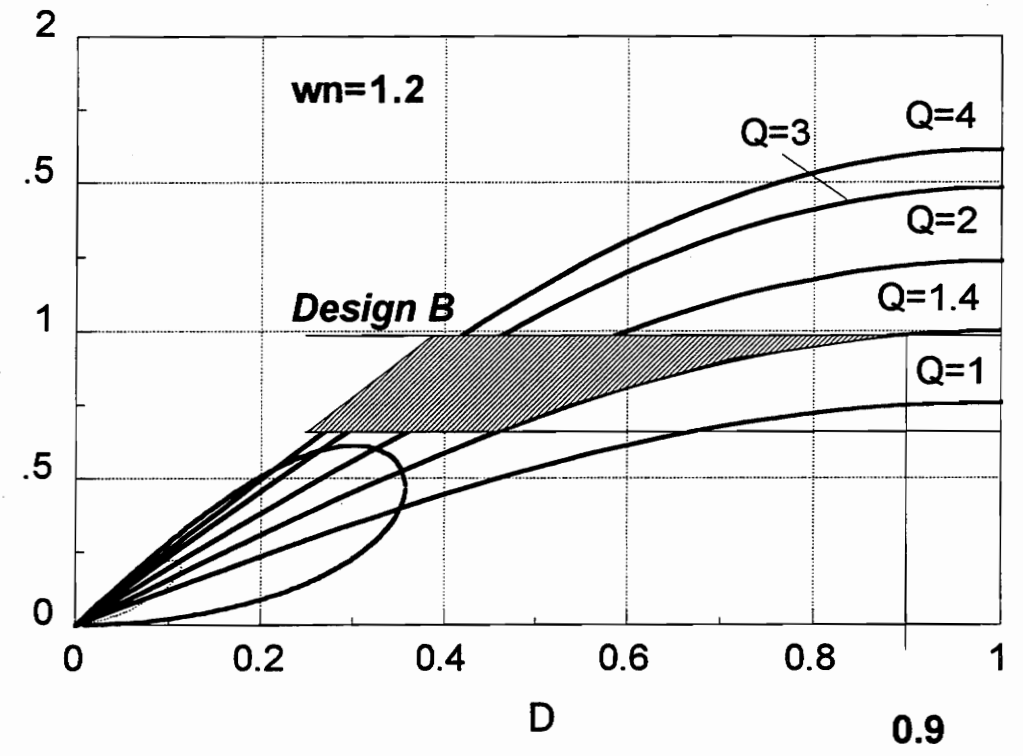


Figure 3.24: Designs for the PS-PRC, operating regions.

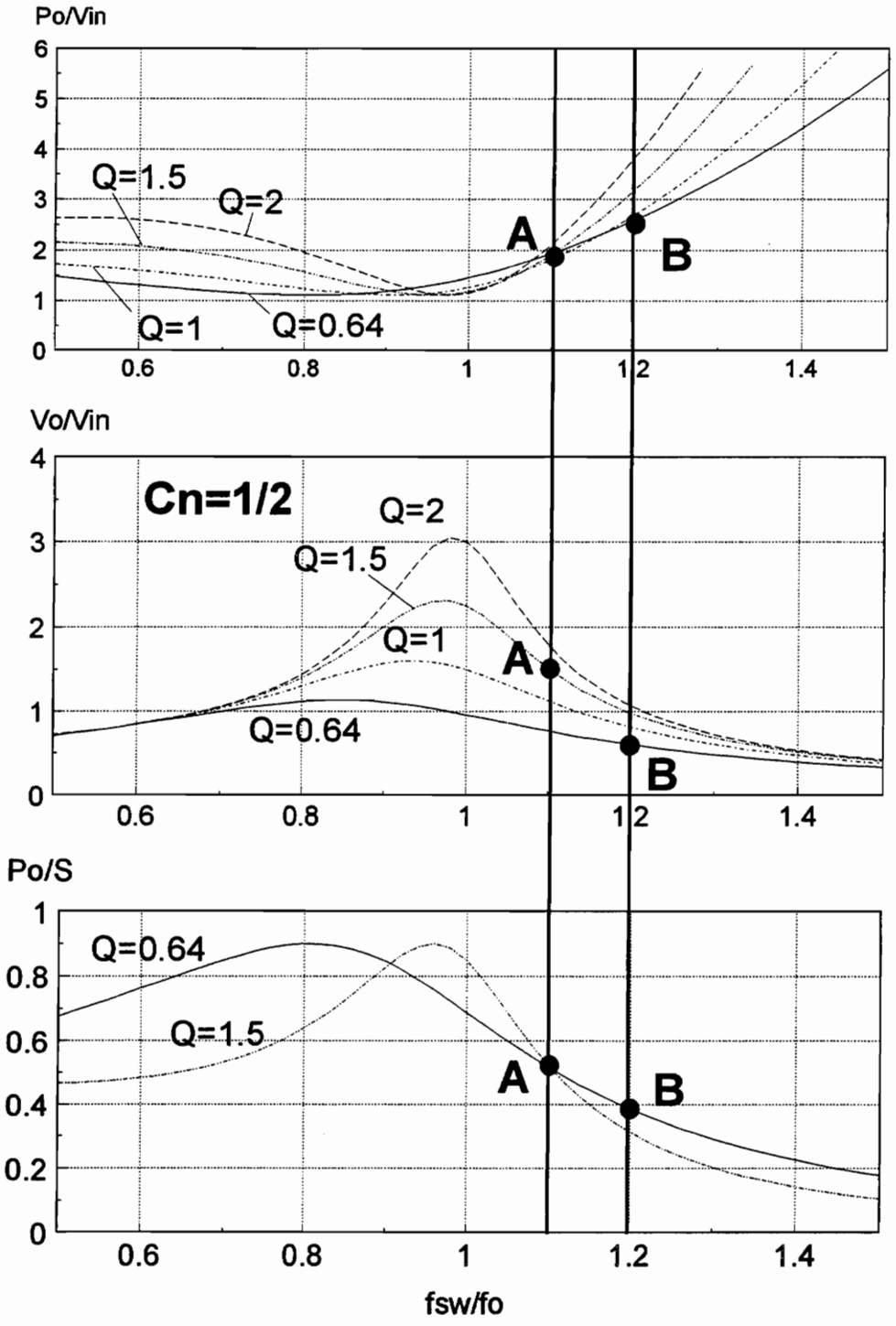


Figure 3.25: PS-LCC resonant converter designs with C_n=0.5, frequencies of operation selected.

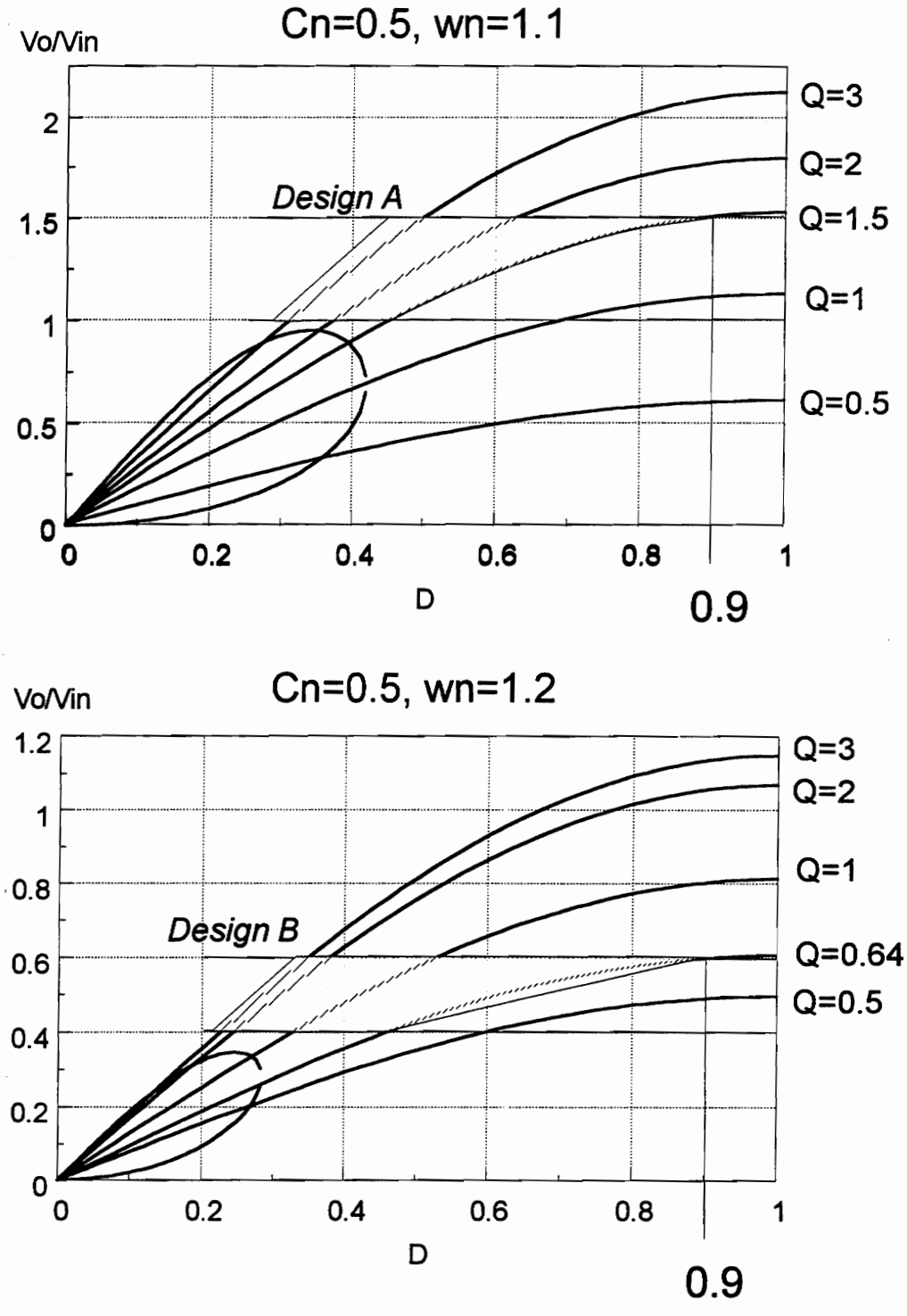


Figure 3.26: PS-LCC resonant converter designs with C_n=0.5, operating regions.

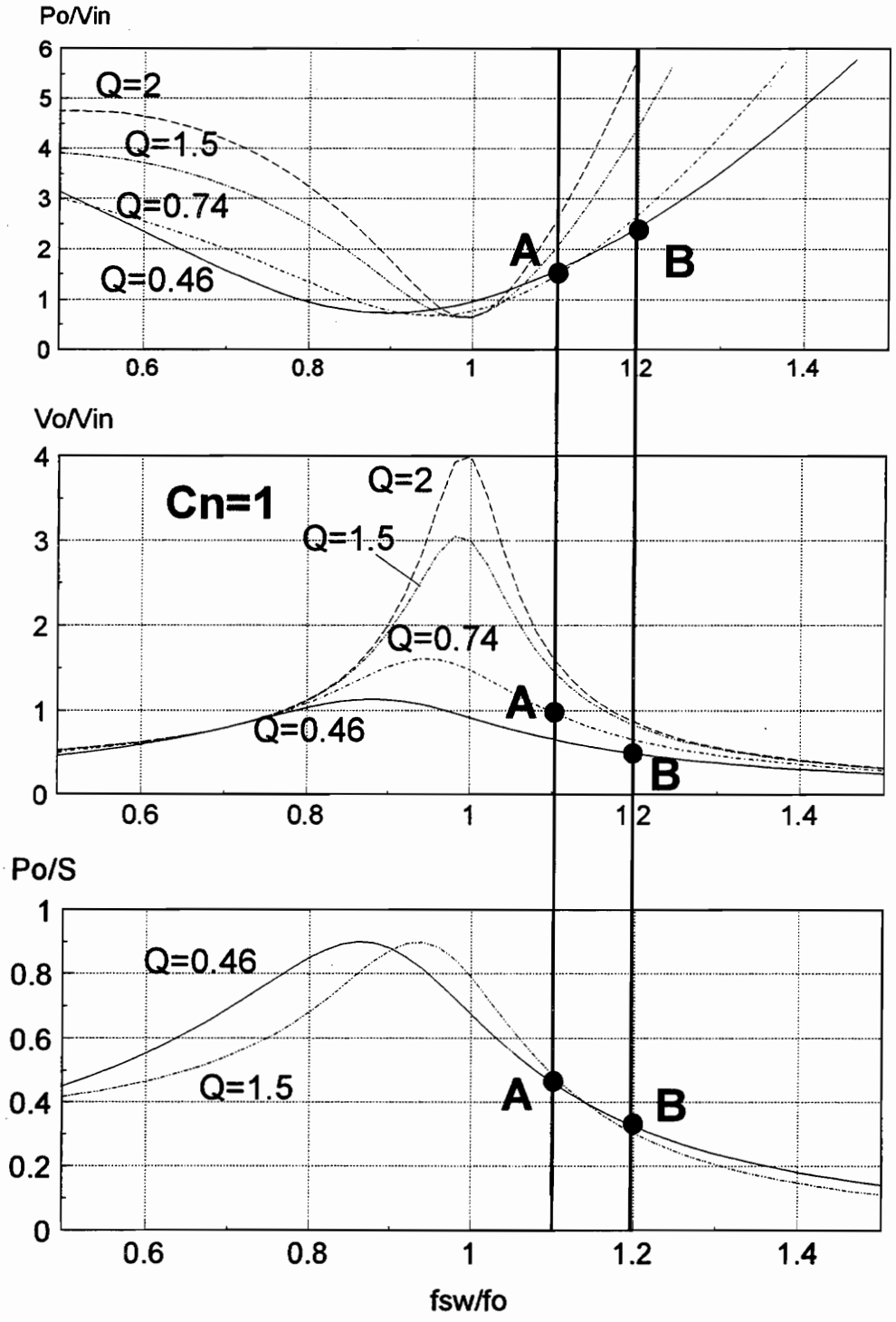


Figure 3.27: PS-LCC resonant converter designs with C_n=1 , frequencies of operation selected.

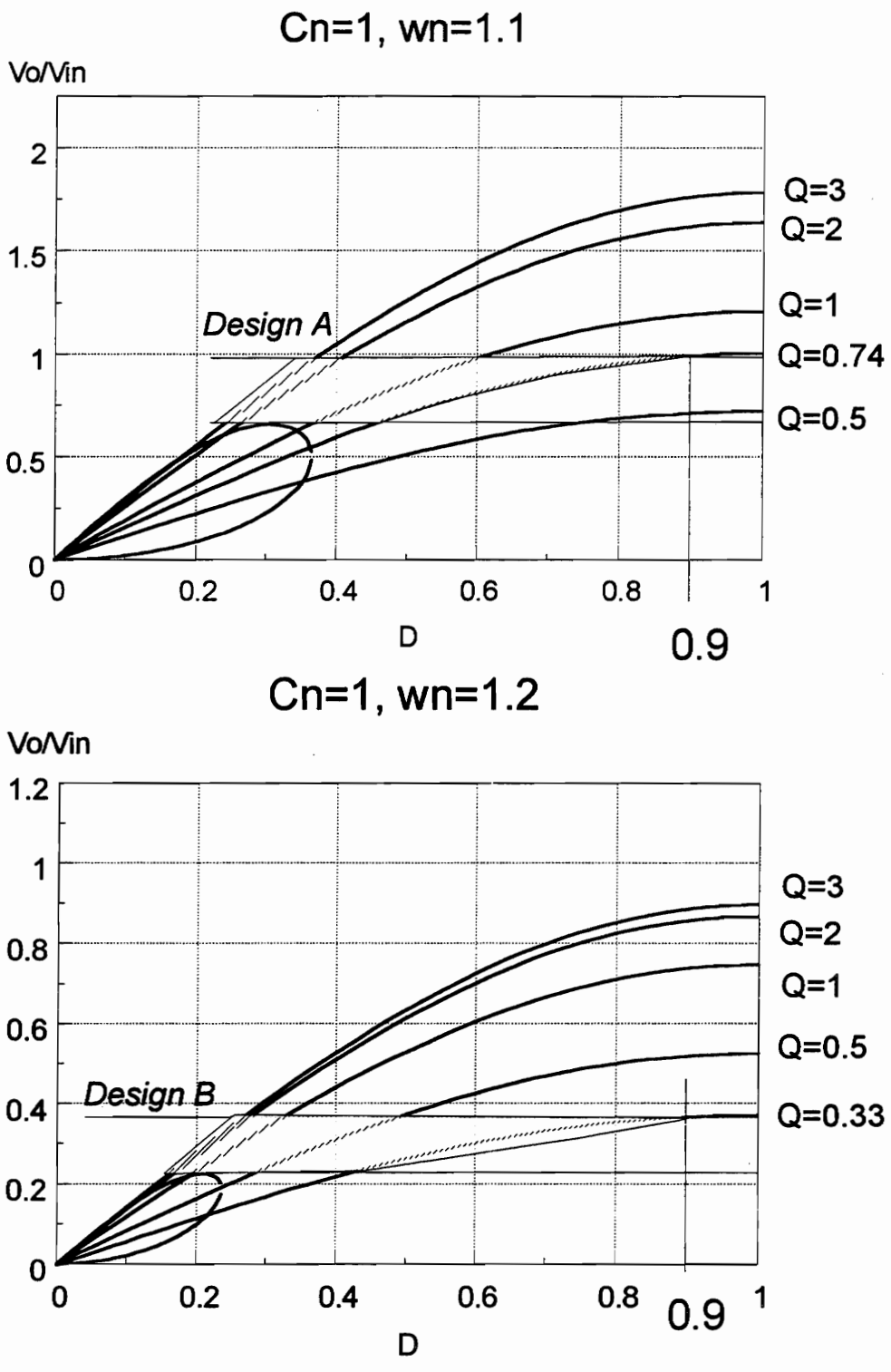


Figure 3.28: PS-LCC resonant converter designs with C_n=1, operating regions.

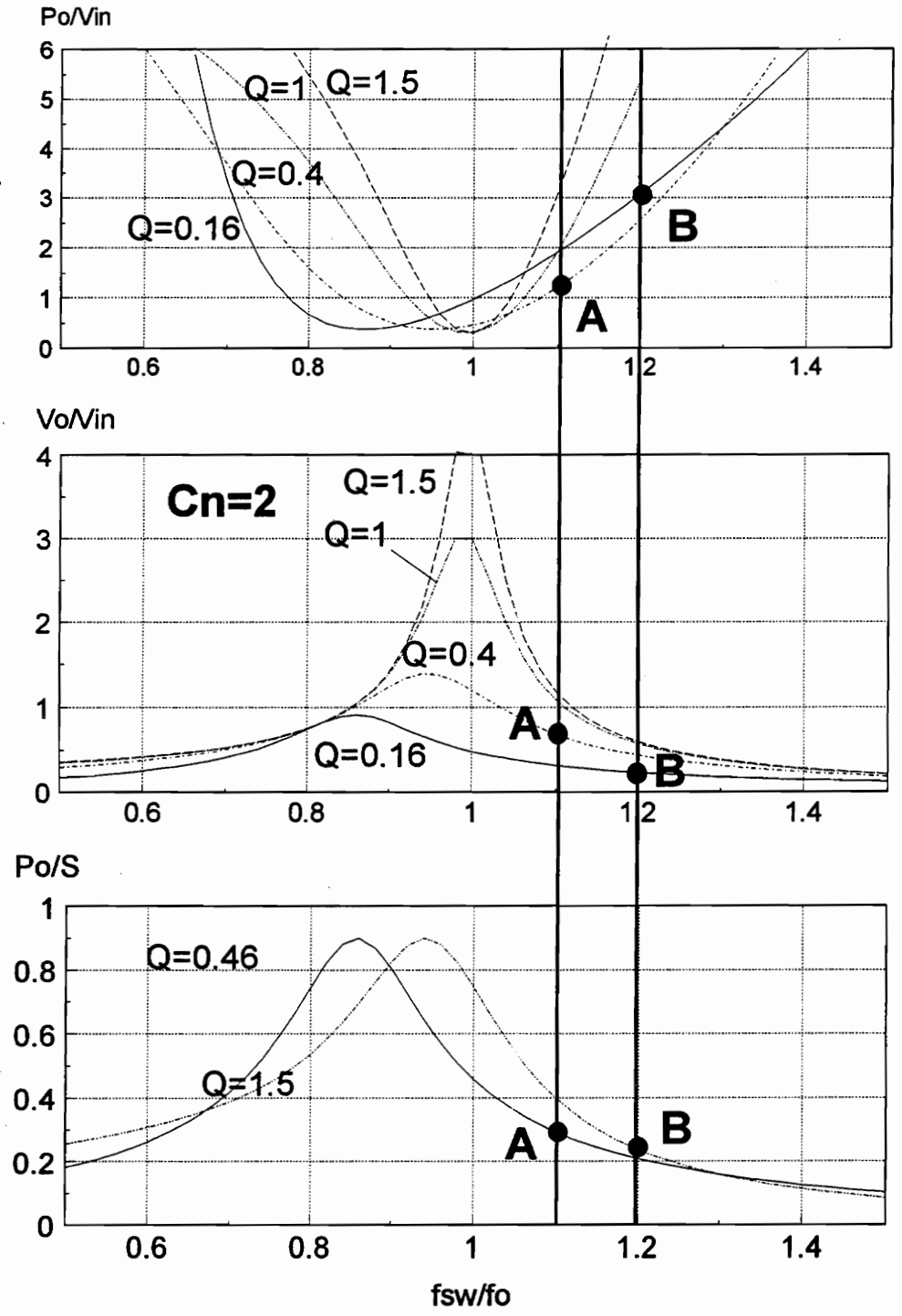


Figure 3.29: PS-LCC resonant converter designs with C_n=2, frequencies of operation selected.

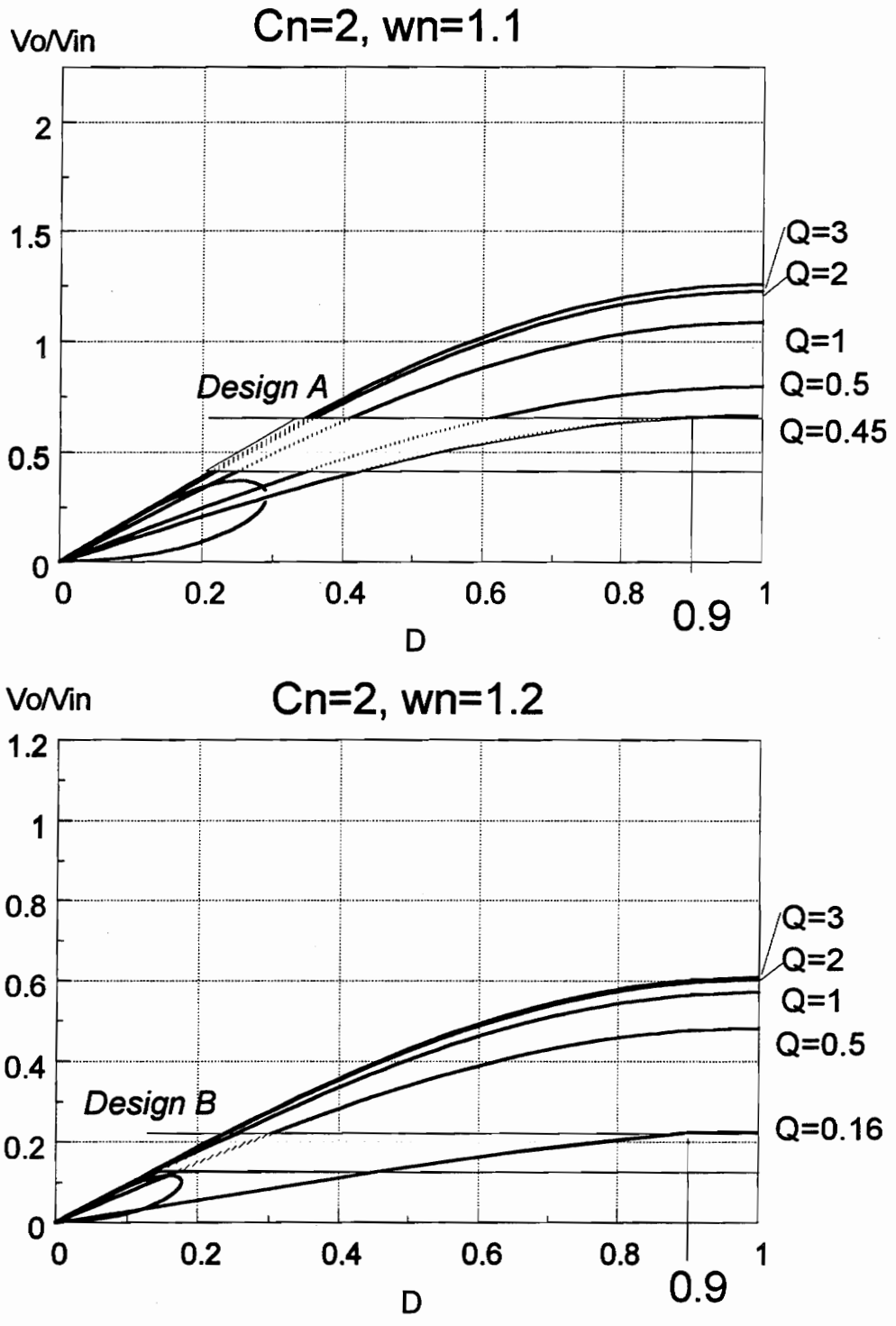


Figure 3.30: PS-LCC resonant converter designs with C_n =2, operating regions.

4. Effect of Switch Output Capacitance on Zero-Voltage Switching of Resonant Converters

4.1 Significance of Switch Capacitance for Zero-Voltage Switching

Generally, bridge-type resonant converters can operate with ZVS without increased voltage stress on the devices. However, ZVS topologies still suffer from higher switch currents as compared to their pulse-width-modulated (PWM) counterparts. To minimize the conduction loss, large MOSFET devices with inherently large output capacitances are usually employed. In addition, lossless capacitive snubbers are often used across the devices to reduce their turn-off losses and minimize undesirable ringing due to parasitic inductances. As a result, the effective capacitance across the devices can be relatively large, which significantly affects the operation of the converter.

In analyses of resonant converters that assume ideal switches, ZVS operation is predicted to occur whenever the switching frequency is above the resonant frequency of the tank. However, it has been found that if the capacitance of the devices is sufficiently large, ZVS cannot be achieved above resonant frequency because the energy in the resonant inductor is not sufficient to discharge the output capacitance of the devices. This is especially true for resonant converters designed to operate with a low Q-factor of the resonant tank at full load. For example, this is always the case in a properly designed LCC resonant converter (LCC-RC), also called series parallel resonant converter (SPRC) [B-3, B-7].

Therefore, the effect of switch capacitance on ZVS operation and voltage conversion characteristics is of prime importance for a proper design of resonant converters operating with low Q-factor.

The analysis presented in this paper predicts the operating conditions of resonant converters at which ZVS is obtained as a function of the capacitance of the switches, allowing the designer to make the right choice of switching devices and capacitive snubbers. The inclusion of switch capacitance adds complexity to the analysis. Extra resonant components have to be added (switch capacitance), and two more topological stages, corresponding to the switching transitions, have to be considered. Also, a numerical algorithm has to be employed to generate the dc characteristics and to determine operating regions with ZVS.

The analysis to be presented is experimentally verified on a LCC-RC.

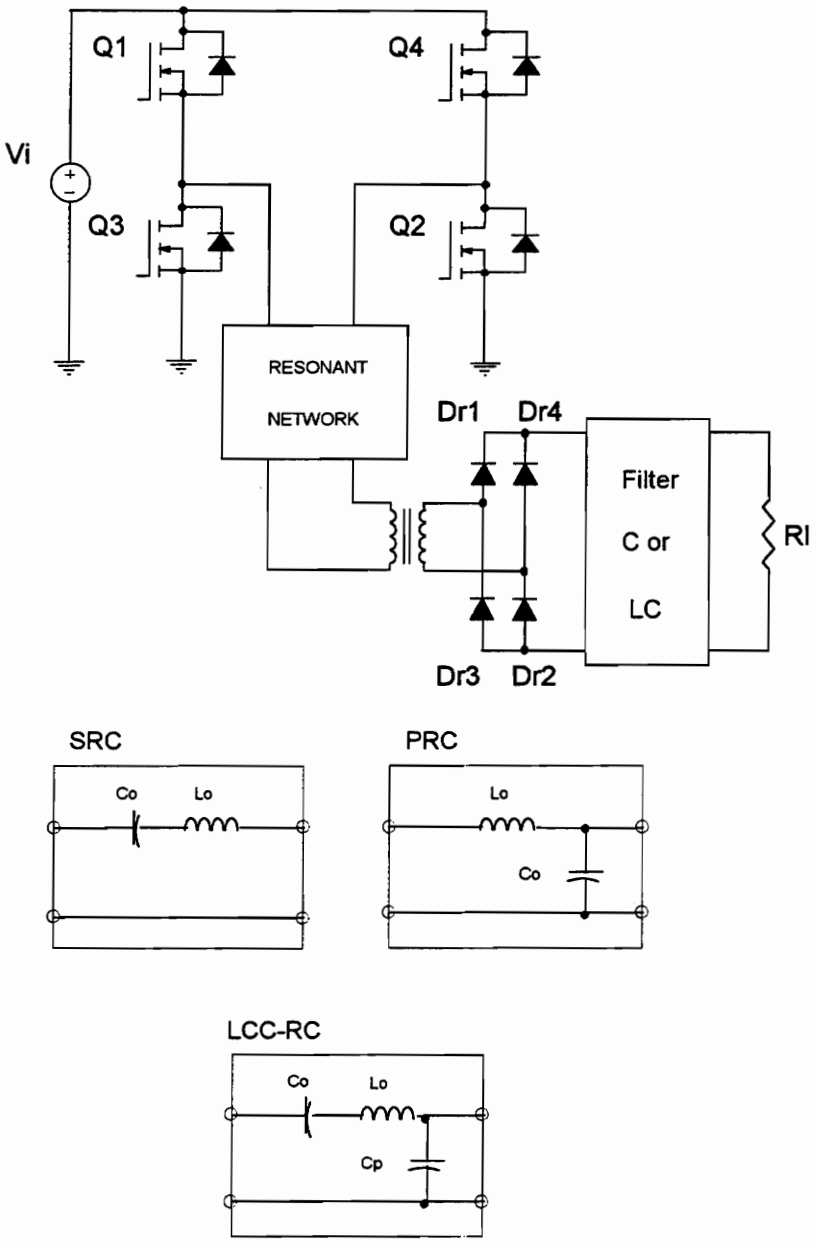


Figure 4.1: Resonant converter.

4.2 Analysis Including Switch Capacitance

Resonant converters have been analyzed previously by means of the conventional approach, without taking the effect of switch capacitance into consideration. Several methods of analysis are available for resonant converters [A-9, A-11, A-14, D-1 B-4]. The approach used for the dc analysis presented in this paper is the time-domain analysis [A-9, A-11]. This approach requires determining the sequence of topological stages of the converter, formulating the differential equations in each case, and solving them by matching the initial conditions at the beginning and the end of the period. This method is very general and can be applied to any resonant converter. The main difficulty is that the solution of the differential equations in most cases can be only solved numerically.

In this paper, the effect of the switch capacitance is analyzed for the SRC, PRC, and LCC-RC. Figure 4.1 shows the general schematic for a resonant converter. The filter stage is an LC filter for the PRC and LCC-RC, and only a C for the SRC. The analysis including the switch capacitance results in two additional topological stages corresponding to the switching transitions. In these two stages the switches' capacitances are modeled as a capacitor C_{sw}. For a full-bridge topology, C_{sw} corresponds to the total capacitance across one of the switches, including the output capacitance of the MOSFET's, C_{oss}, plus any external capacitor added as a lossless snubber. The capacitances across Q1 and Q2 are in parallel, and their equivalent capacitance is in series with the equivalent capacitances across Q3 and Q4 which are in parallel.

In the analysis, C_{sw} is assumed to be a linear capacitance. This assumption is only valid if snubber capacitors much larger than C_{oss} are added across the switches. Otherwise, if only the switch capacitance is present, the value of the linear capacitance C_{sw} is chosen so that it stores the same charge as the actual nonlinear C_{oss} of the switches at the operating voltage:

$$C_{sw} = 2 \cdot C_{oss}^{(at, V_{in})}$$

The differential equations are solved using a numerical algorithm. The equations are normalized with respect to the following normalization factors:

- resonant frequency

$$\omega_o = \frac{1}{\sqrt{L_o \cdot C_o}},$$

where C_o corresponds to C_s for the SRC, to C_p for the PRC, and $C_s \cdot C_p / (C_s + C_p)$ for the LCC-RC.

- current and voltage normalization factors,

$$I_b = \frac{V_{in}}{Z_o} \quad \text{and} \quad V_b = V_{in}$$

where $Z_o = \sqrt{L_o / C_o}$.

The switch capacitance is expressed as

$$C_{sn} = \frac{C_s}{C_{sw}}$$

for the SRC and LCC, and as

$$C_{sn} = \frac{C_p}{C_{sw}}$$

for the PRC.

4.2.1 Analysis of the SRC Including Switch Capacitance.

Figure 4.2 shows the equivalent circuit representation used in the analysis; V_e takes the values shown in the table in Fig. 4.2, according to the devices that are conducting. Between switching intervals the circuit for mode I is used for the analysis, while the circuit for mode II is used for the converter operation during the switching transitions. Figure 4.3 shows the typical waveforms for the SRC, indicating the topological modes corresponding to each interval of the switching period.

The equations describing current and voltages in topological mode I are:

$$v_c^n = \left(v_c^{onI} - V_e^n\right)\cdot\cos(\omega_o t) + i_L^{onI}\cdot\sin(\omega_o t) + V_e^n) \tag{4.1}$$

$$i_L^n = \left(-v_c^{onI} + V_e^n\right)\cdot\sin(\omega_o t) + i_L^{onI}\cdot\cos(\omega_o t) \tag{4.2}$$

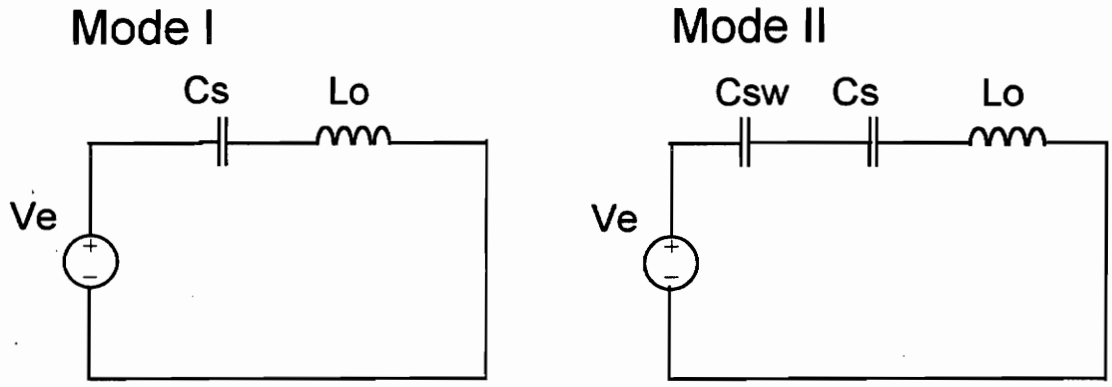
The equations corresponding to mode II are:

$$v_c^n = \frac{1}{1+C_{sn}}\cdot\left(C_{sn}v_c^{onII} - v_{sw}^{onII} + V_e^n\right) + \frac{1}{1+C_{sn}}\cdot\left(v_c^{onII} + v_{sw}^{onII} - V_e^n\right)\cdot\cos\left(\omega_o t\sqrt{1+C_{sn}}\right) +$$

$$+\frac{1}{\sqrt{1+C_{sn}}}\cdot i_L^{onII}\cdot\sin\left(w_o t\sqrt{1+C_{sn}}\right) \tag{4.3}$$

$$v_{sw}^n = \frac{C_{sn}}{1+C_{sn}}\cdot\left(-v_c^{onII} + \frac{v_{sw}^{onII}}{C_{sn}} + V_e^n\right) + \frac{C_{sn}}{1+C_{sn}}\cdot\left(v_c^{onII} + v_{sw}^{onII} - V_e^n\right)\cdot\cos\left(\omega_o t\sqrt{1+C_{sn}}\right) +$$

$$+\frac{C_{sn}}{\sqrt{1+C_{sn}}}\cdot i_L^{onII}\cdot\sin\left(\omega_o t\sqrt{1+C_{sn}}\right) \tag{4.4}$$



Topological mode	Conducting on Prim.	Conducting on Sec.	V_e
I	Q1-Q2	Dr3-Dr4	$+V_i+V_{out}$
I	Q1-Q2	Dr1-Dr2	$+V_i-V_{out}$
II	none	Dr1-Dr2	$+V_i-V_{out}$
I	Q3-Q4	Dr1-Dr2	$-V_i-V_{out}$
I	Q3-Q4	Dr3-Dr4	$-V_i+V_{out}$
II	none	Dr3-Dr4	$-V_i+V_{out}$

Figure 4.2: SRC topological modes.

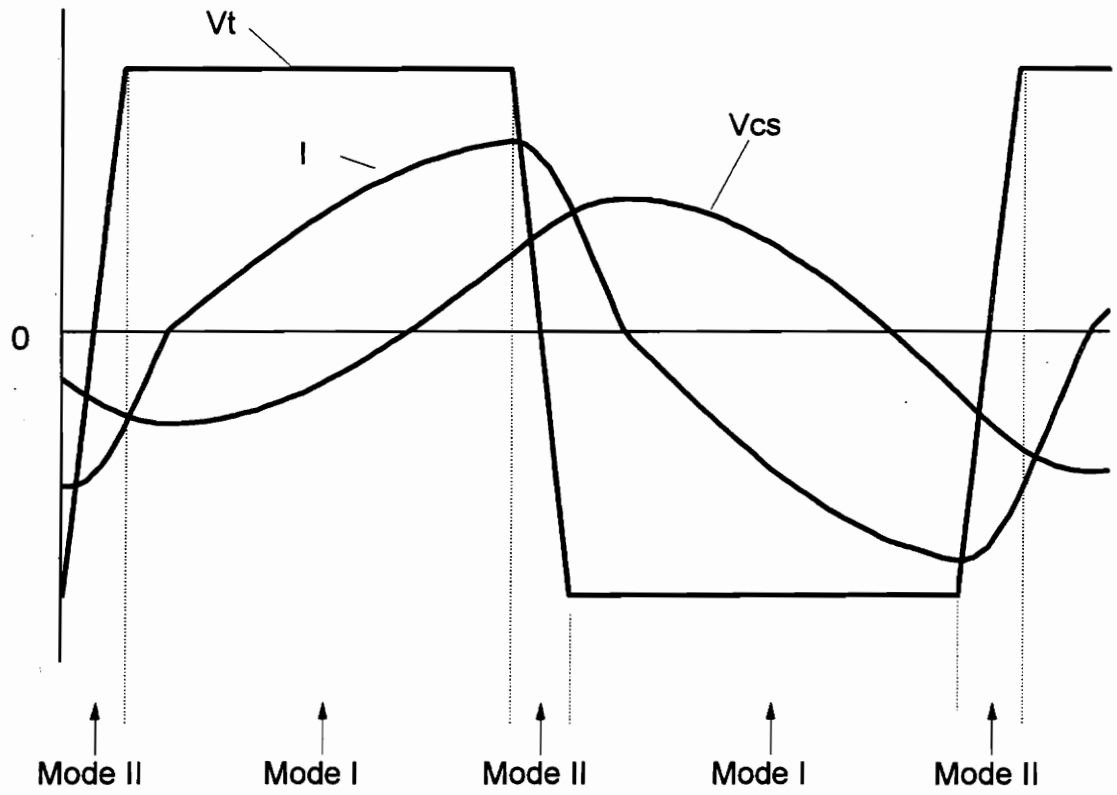


Figure 4.3: SRC typical waveforms, indicating the topological modes, for operation above resonant frequency.

$$i_L^n = \frac{1}{\sqrt{1+C_{sn}}} \cdot \left(-v_c^{onII} - v_{sw}^{onII} + V_e^n\right) \cdot \sin\left(\omega_o t\sqrt{1+C_{sn}}\right) + i_L^{onII} \cdot \cos\left(\omega_o t\sqrt{1+C_{sn}}\right) \qquad (4.5)$$

where v_c^n and i_L^n, are the normalized capacitor voltage and inductor current; v_c^{onI}, v_c^{onII}, i_L^{onI}, and i_L^{onII}, are the initial values for the voltage and current at the beginning of the interval corresponding to each mode.

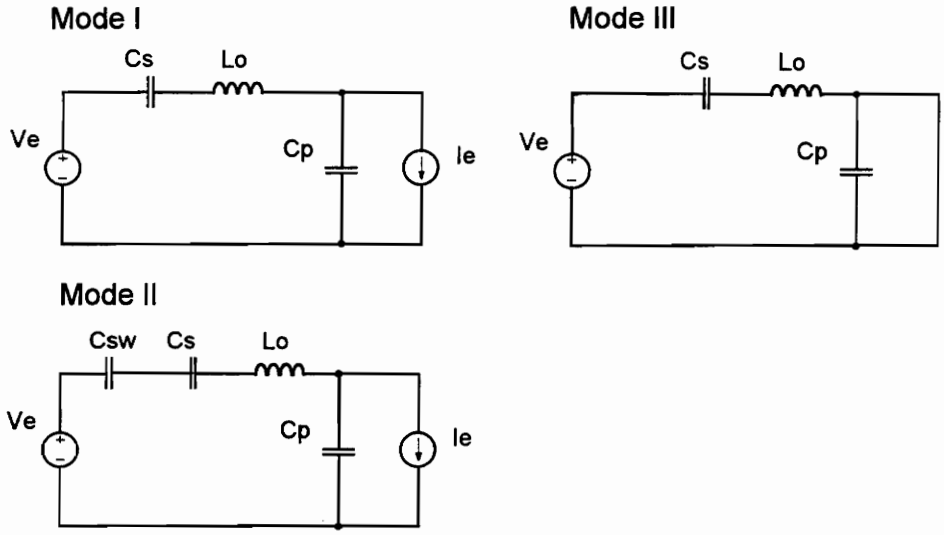
4.2.2 Analysis of the PRC and LCC-RC Including Switch Capacitance.

Figure 4.4 shows the equivalent circuit representation used in the analysis; V_e and I_e take the values shown in the table in Fig. 4.4, according to the devices that are conducting. Between switching intervals the circuit for mode I is used for the analysis, while the circuit for mode II is used for the converter operation during the switching transitions. The circuit for mode III corresponds to the discontinuous capacitor voltage operation. Figure 4.5 shows the typical waveforms for the PRC and LCC-RC, indicating the topological modes corresponding to each interval of the switching period. The only difference in this case is that for the PRC, C_S is not considered, or is assumed large enough so that it does not affect the converter operation.

The equations describing topological mode I for the PRC are:

$$v_c^n = \left(v_c^{onI} - V_e^n\right) \cdot \cos(\omega_o t) + \left(i_L^{onI} - I_e^n\right) \cdot \sin(\omega_o t) + V_e^n \qquad (4.6)$$

$$i_L^n = \left(-v_c^{onI} + V_e^n\right) \cdot \sin(\omega_o t) + i_L^{onI} \cdot \cos(\omega_o t) + I_e^n \cdot (1 - \cos(\omega_o t)) \qquad (4.7)$$



Topological mode	Conducting on Prim.	Conducting on Sec.	V_e	I_e
I	Q1-Q2	Dr3-Dr4	$+V_i$	$-I_{out}$
I	Q1-Q2	Dr1-Dr2	$+V_i$	$+I_{out}$
II	none	Dr1-Dr2	$+V_i$	$+I_{out}$
III	Q1-Q2	all	$+V_i$	short
I	Q3-Q4	Dr1-Dr2	$-V_i$	$+I_{out}$
I	Q3-Q4	Dr3-Dr4	$-V_i$	$-I_{out}$
II	Q3-Q4	Dr3-Dr4	$-V_i$	$-I_{out}$
III	Q3-Q4	all	$-V_i$	short

Figure 4.4: PRC and LCC-RC topological modes.

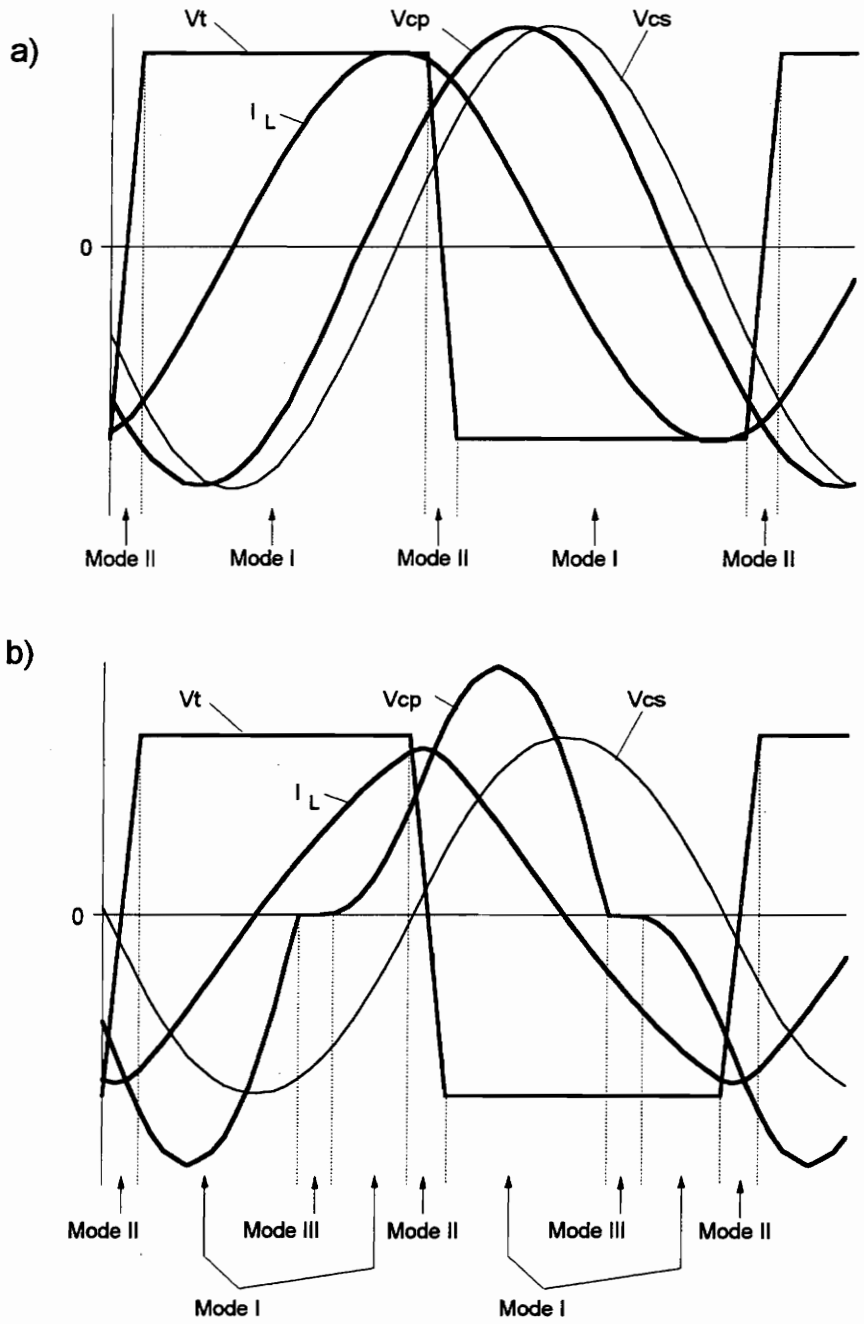


Figure 4.5: **LCC-RC typical waveforms, indicating the topological modes, for operation with: a) continuous capacitor voltage, and b) discontinuous capacitor voltage.**

The equations corresponding to mode II are:

$$v_c^n = v_c^{onII} + \frac{V_e^n - v_c^{onII}}{1+C_{sn}} \cdot \left(1 - \cos\left(\omega_o t\sqrt{1+C_{sn}}\right)\right) + \frac{1}{\sqrt{1+C_{sn}}} \cdot i_L^{onII} \cdot \sin\left(\omega_o t\sqrt{1+C_{sn}}\right) -$$

$$- \frac{I_e^n}{(1+C_{sn})\sqrt{1+C_{sn}}} \cdot \left[C_{sn}\omega_o t\sqrt{1+C_{sn}} + \sin\left(\omega_o t\sqrt{1+C_{sn}}\right)\right], \quad (4.8)$$

$$v_{sw}^n = \frac{1}{2} \cdot \frac{C_{sn}}{1+C_{sn}} \cdot \left(V_e^n - v_c^{onII}\right) \cdot \left[1 - \cos\left(\omega_o t\sqrt{1+C_{sn}}\right)\right] + \frac{C_{sn}}{\sqrt{1+C_{sn}}} \cdot i_L^{onII} \cdot \sin\left(\omega_o t\sqrt{1+C_{sn}}\right) +$$

$$+ \frac{I_e^n}{1+C_{sn}} \cdot \left[C_{sn}\omega_o t - \frac{C_{sn}}{\sqrt{1+C_{sn}}} \cdot \sin\left(\omega_o t\sqrt{1+C_{sn}}\right)\right], \quad (4.9)$$

$$i_L^n = \frac{V_e^n - v_c^{on}}{\sqrt{1+C_{sn}}} \cdot \sin\left(\omega_o t\sqrt{1+C_{sn}}\right) + i_L^{on} \cdot \cos\left(\omega_o t\sqrt{1+C_{sn}}\right) + \frac{I_e^n}{1+C_{sn}} \cdot \left[1 - \cos\left(\omega_o t\sqrt{1+C_{sn}}\right)\right] \quad (4.10)$$

where v_c^n, and i_L^n, are the normalized parallel capacitor voltage and normalized inductor current, respectively. The values v_c^{onI}, v_c^{onII}, i_L^{onI} and i_L^{onII}, are the corresponding initial values at the beginning of topological modes I and II.

The equations for topological mode III are:

$$v_c^n = 0\,, \quad (4.11)$$

$$i_L^n = i_L^{onIII} + V_e^n \cdot \omega_o t\,, \quad (4.12)$$

where i_L^{onIII}, is the inductor current at the beginning of topological mode III.

For the LCC-RC the equations can be expressed as a function of the ratio of the series and the parallel capacitors, defined as

$$C_n = \frac{C_s}{C_p},$$

and using for V_e and I_e the values shown in the table of Fig. 4.4.

The equations describing topological mode I for the LCC are:

$$v_{cs}^n = \left[\cos(\omega_o t) + \frac{C_n}{1+C_n}\cdot(1-\cos(\omega_o t))\right]\cdot v_{cs}^{onl} - \frac{C_n}{1+C_n}\cdot(1-\cos(\omega_o t))\cdot v_{cp}^{onl} +$$

$$+\frac{1}{1+C_n}\cdot i_L^{onl}\cdot\sin(\omega_o t) + \frac{1}{1+C_n}\cdot(1-\cos(\omega_o t))\cdot V_e^n + \frac{C_n}{(1+C_n)^2}\cdot[\omega_o t - \sin(\omega_o t)]\cdot I_e^n \tag{4.13}$$

$$v_{cp}^n = \left[\cos(\omega_o t) + \frac{1}{1+C_n}\cdot(1-\cos(\omega_o t))\right]\cdot v_{cp}^{onl} - \frac{C_n}{1+C_n}\cdot(1-\cos(\omega_o t))\cdot v_{cs}^{onl} +$$

$$+\frac{1}{1+C_n}\cdot i_L^{onl}\cdot\sin(\omega_o t) + \frac{1}{1+C_n}\cdot(1-\cos(\omega_o t))\cdot V_e^n -$$

$$-\left[\frac{C_n}{1+C_n}\cdot\sin(\omega_o t) + \frac{C_n}{(1+C_n)^2}\cdot[\omega_o t - \sin(\omega_o t)]\right]\cdot I_e^n \tag{4.14}$$

$$i_L^n = -v_{cs}^{onl}\cdot\sin(\omega_o t) - v_{cp}^{onl}\cdot\sin(\omega_o t) + i_L^{onl}\cdot\cos(\omega_o t) +$$

$$+V_e^n\cdot\sin(\omega_o t) + \frac{1}{1+C_n}\cdot(1-\cos(\omega_o t))\cdot I_e^n \tag{4.15}$$

where v_{cs}^n, v_{cp}^n, and i_L^n, correspond to the normalized voltage for the series and parallel capacitors and normalized inductor current, respectively. The values v_{cs}^{onl}, v_{cp}^{onl}, and i_L^{onl} are the corresponding initial values at the beginning of topological mode I.

The equations for topological mode II are obtained from the equations for mode I by replacing C_S with $C_S + C_{SW}$. After substitution and simplification,

$$v_{cs}^n = AAN \cdot \cos\alpha_t + BAN \cdot \sin\alpha_t + CAN + 2\pi \cdot \frac{C_n}{1+C_n} \cdot \frac{1}{1+C_n+C_{sn}} \cdot t_n \cdot I_e^n , \qquad (4.16)$$

$$v_{sw}^n = \frac{1}{2} \cdot \frac{C_p}{C_{sw}} \cdot \left[AAN \cdot \cos\alpha_t + BAN \cdot \sin\alpha_t - v_{cs}^{onII} + 2 \cdot \pi \cdot \frac{C_n}{1+C_n} \cdot \frac{1}{1+C_n+C_{sn}} \cdot t_n \cdot I_e^n\right] + v_{sw}^{on} - 1 (4.$$

$$v_{cp}^n = C_n \cdot \left(v_{cs}^{nII} - v_{cs}^{nII}\right) - 2 \cdot \pi \cdot \frac{C_n}{1+C_n} \cdot t_n \cdot I_e^n, \text{ and} \qquad (4.18)$$

$$i_L^n = \sqrt{(1+C_n) \cdot (1+C_n+C_{sw})} \cdot (BAN \cdot \cos\alpha_t - AAN \cdot \sin\alpha_t) + \frac{C_n}{1+C_n+C_{sn}} \cdot I_e^n , \qquad (4.19)$$

where

$$\alpha_t = \sqrt{1+\frac{C_{sn}}{1+C_n}} \cdot \omega_o \cdot t, \; t_n = \frac{t}{T_{sw}},$$

$$AAN = \frac{v_{cs}^{onII} + v_{cp}^{onII} + 2 \cdot v_{sw}^{onII} - 1}{1+C_n+C_{sn}},$$

$$BAN = \frac{i_L^{on}}{\sqrt{(1+C_n) \cdot (1+C_n+C_{sn})}},$$

$$CAN = 1 + v_{cp}^{on} - 2 \cdot v_{sw}^{on} + AAN \cdot (C_n + C_{sn}),$$

and T_{SW} is the switching period.

The equations for topological mode III are:

$$v_{cs}^n = V_E^n + \left(v_{cs}^{onIII} - V_E^n\right) \cdot \cos\alpha_d + \sqrt{\frac{1}{1+C_n}} \cdot i_L^{onIII} \cdot \sin\alpha_d, \qquad (4.20)$$

$$v_{cp}^{n} = 0, \tag{4.21}$$

$$i_{L}^{n} = \sqrt{\frac{1}{1+C_n}} \cdot \left(v_{cs}^{onIII} - V_{E}^{n}\right) \cdot \sin\alpha_d + i_{L}^{onIII} \cdot \cos\alpha_d, \tag{4.22}$$

where $\alpha_d = \left(\sqrt{1/(1+C_n)}\right) \cdot \omega_o \cdot t$.

The equations for the three topological modes can be solved numerically for each set of operating conditions. The dc conversion characteristics are obtained by integrating the parallel capacitor voltage v_{cp}^{n}.

4.3 Effects of Switch Capacitance

Resonant converters operate with zero-voltage switching (ZVS) if the switches are turned on after their output capacitance is completely discharged. This requires the inductor current to be exactly zero at the instant of switching, after discharging the switches' output capacitance, or to have current flowing through the anti-parallel diodes of the MOSFET's that are about to be turned on.

4.3.1 Effects of C_{sw} on the SRC

For ideal switches, C_{oss}=0 and with no external snubber capacitors, the ZVS is achieved at any frequency above the frequency that corresponds to the peak of the voltage gain for given Q ($Q = Z_o/R_{load}$). Figure 4.6 shows the dc voltage gain characteristics of the SRC with ideal switches.

Figures 4.7a and 4.7b show the voltage gain characteristics for different switch capacitance values. Also the region where the converter operates with zero voltage

switching for the switches in the bridge is shown in each case. Two major effects can be noticed:

- The voltage gain decreases when C_{sw} increases, and this is more pronounced for low Q values.
- The ZVS can only be achieved at frequencies higher than the resonant frequencies. The frequency has to be higher when C_{sw} increases, and it changes more for the low Q values. No ZVS operation is possible for the lower Q's; for instance no ZVS operation is possible for Q<0.75 for C_{sw}/C_s=0.2.

4.3.2 Effects of C_{sw} on the PRC

For ideal switches, C_{oss}=0 and with no external snubber capacitors, the ZVS is achieved at any frequency above the frequency that corresponds to the peak of the voltage gain for given Q ($Q = R_{load}/Z_o$). Figure 4.8 shows the dc voltage gain characteristics of the PRC with ideal switches.

Figure 4.9 shows the dc characteristics for different values of switch capacitance, with the ZVS limit for ideal switches and the new one. It can be seen that the voltage gain is almost unchanged when including the switch capacitance. However, the ZVS limit is pushed to higher frequencies. Since the dc characteristics are not changed, all ZVS limits can be shown on the same graph. Figure 4.10 shows different ZVS limits corresponding to several C_{sw}.

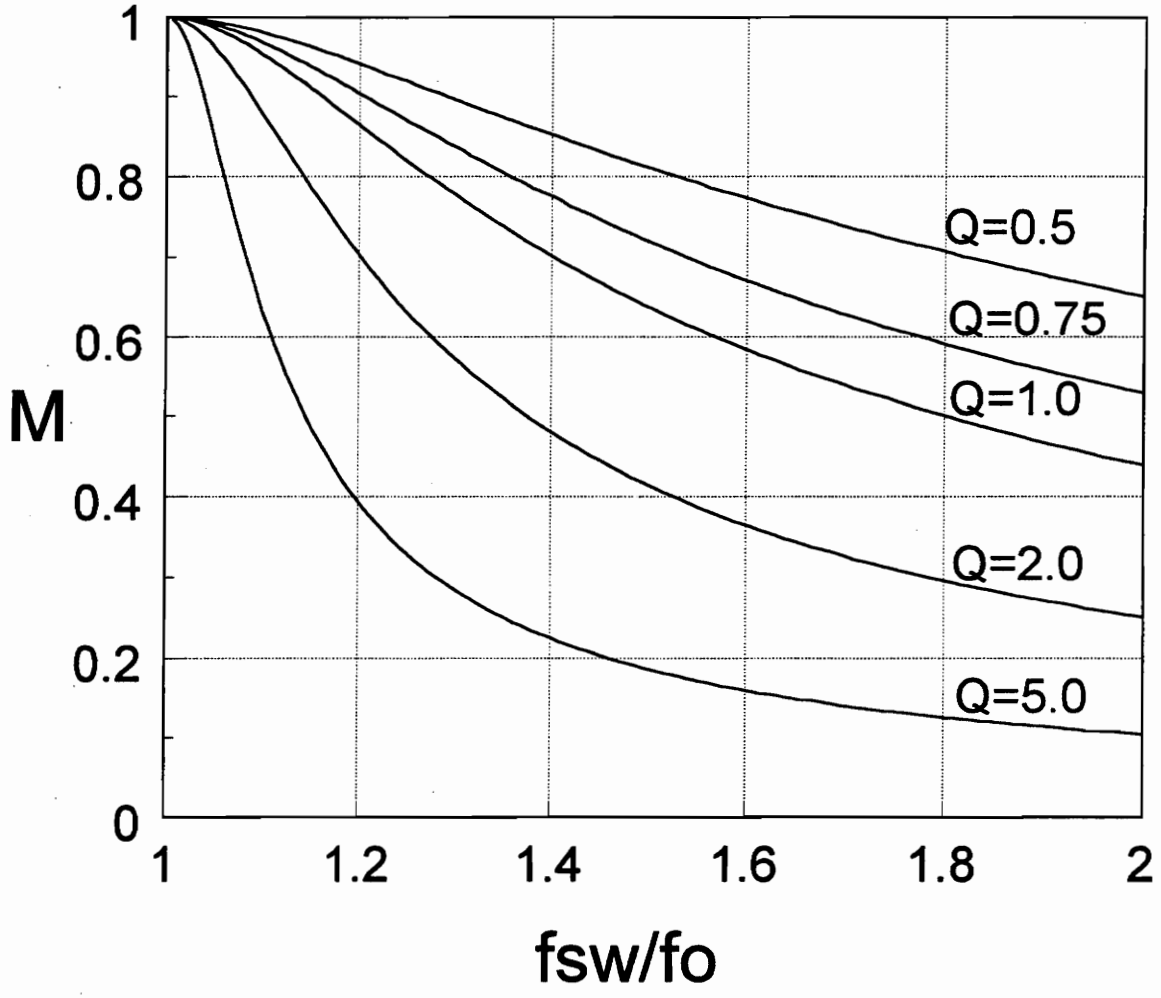


Figure 4.6: Dc characteristics for the SRC with ideal switches. ZVS operation for all frequencies above the resonant frequency, $(f_{sw}/f_o)>1$.

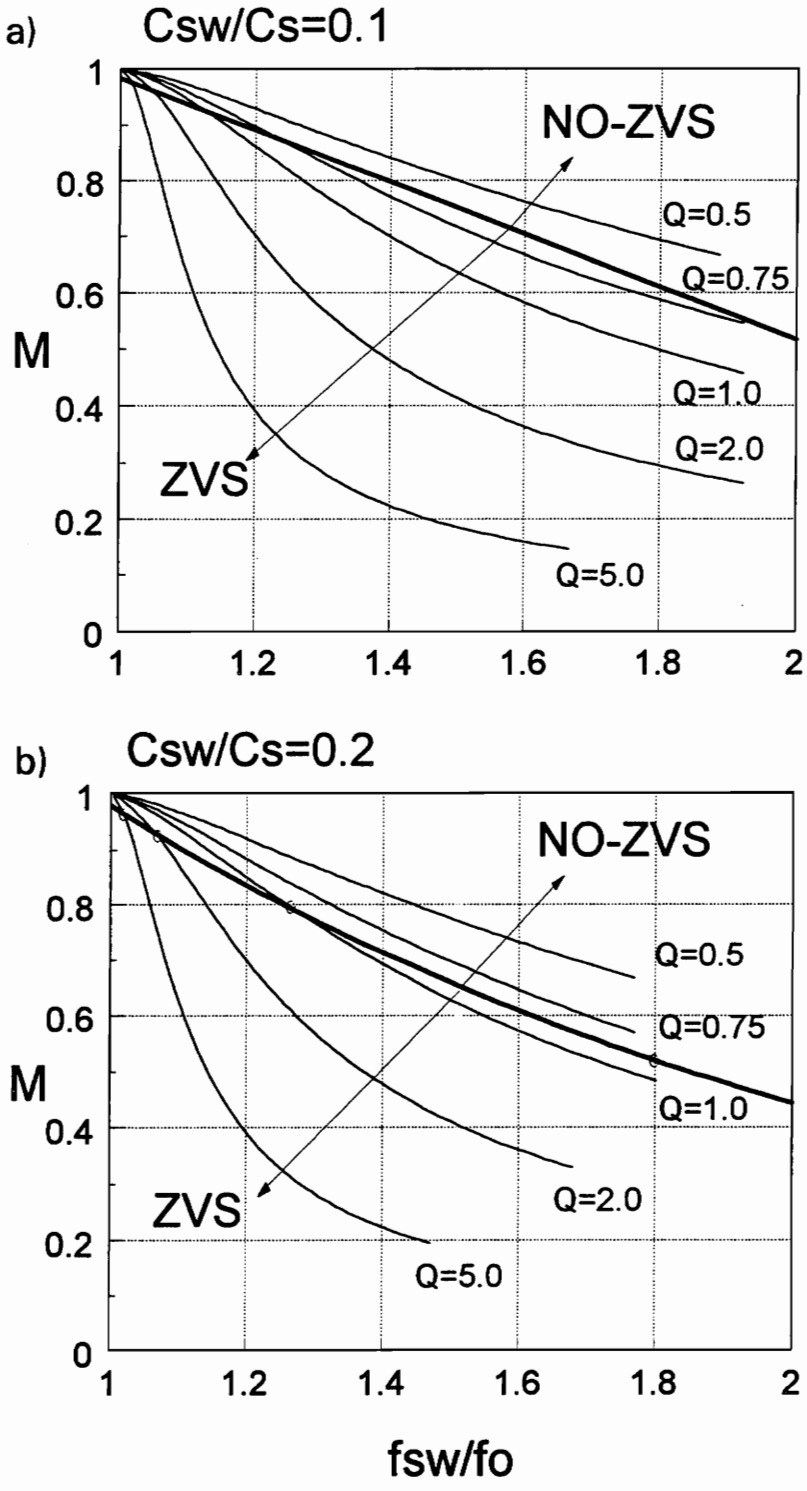


Figure 4.7: Dc characteristics of SRC, for different values of C_{sw}.

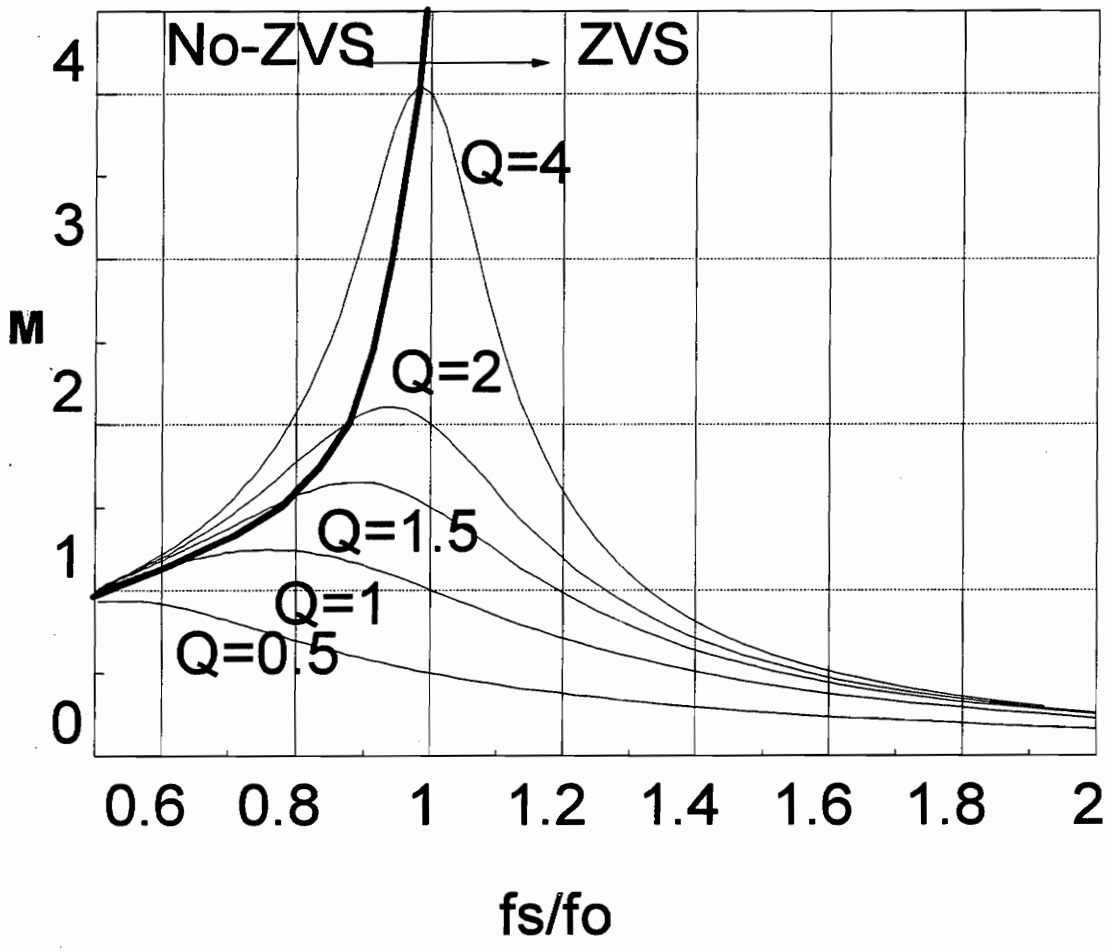


Figure 4.8: Dc characteristics for the PRC with ideal switches.

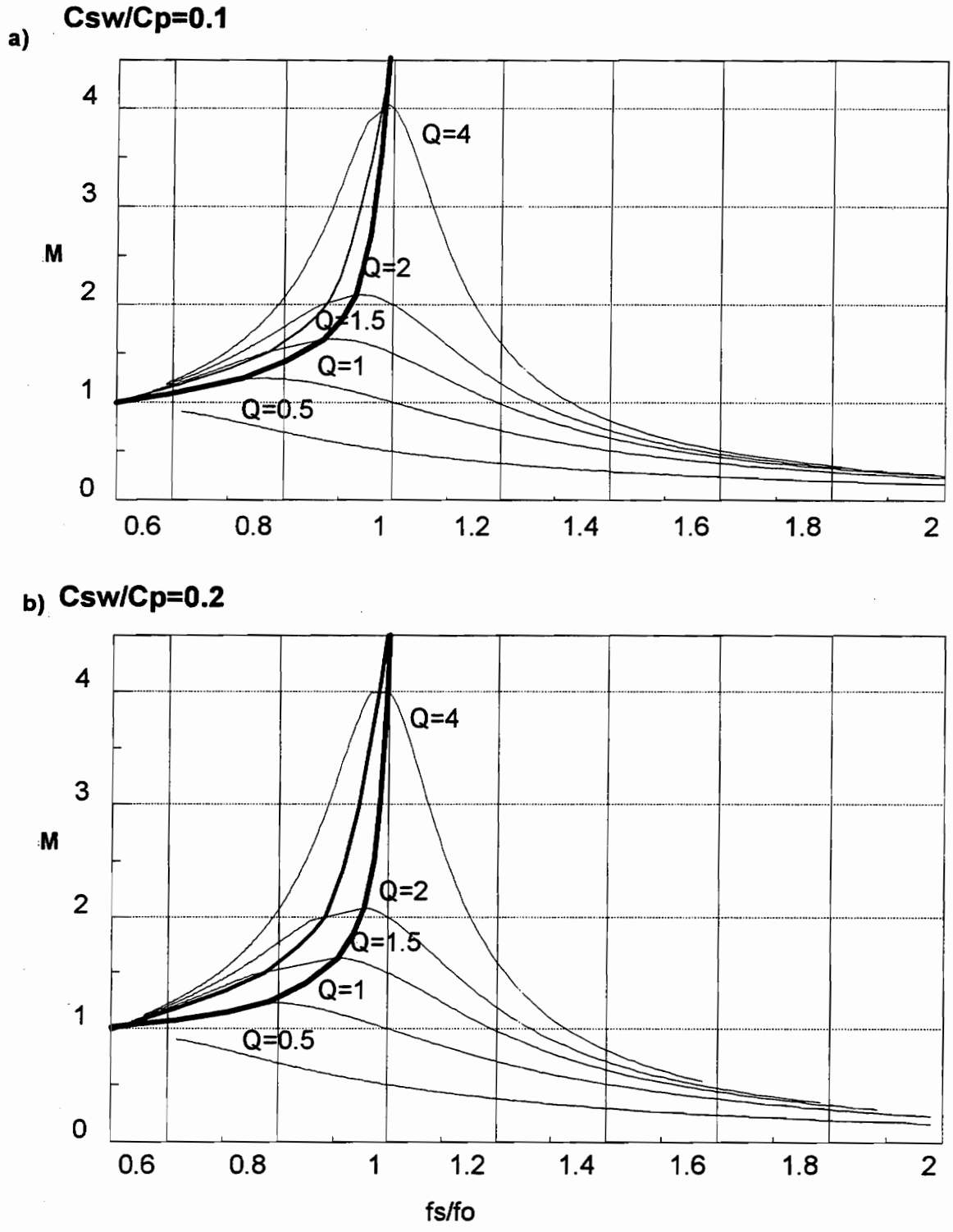


Figure 4.9: Dc characteristics of PRC, for different values of C_{sw}.

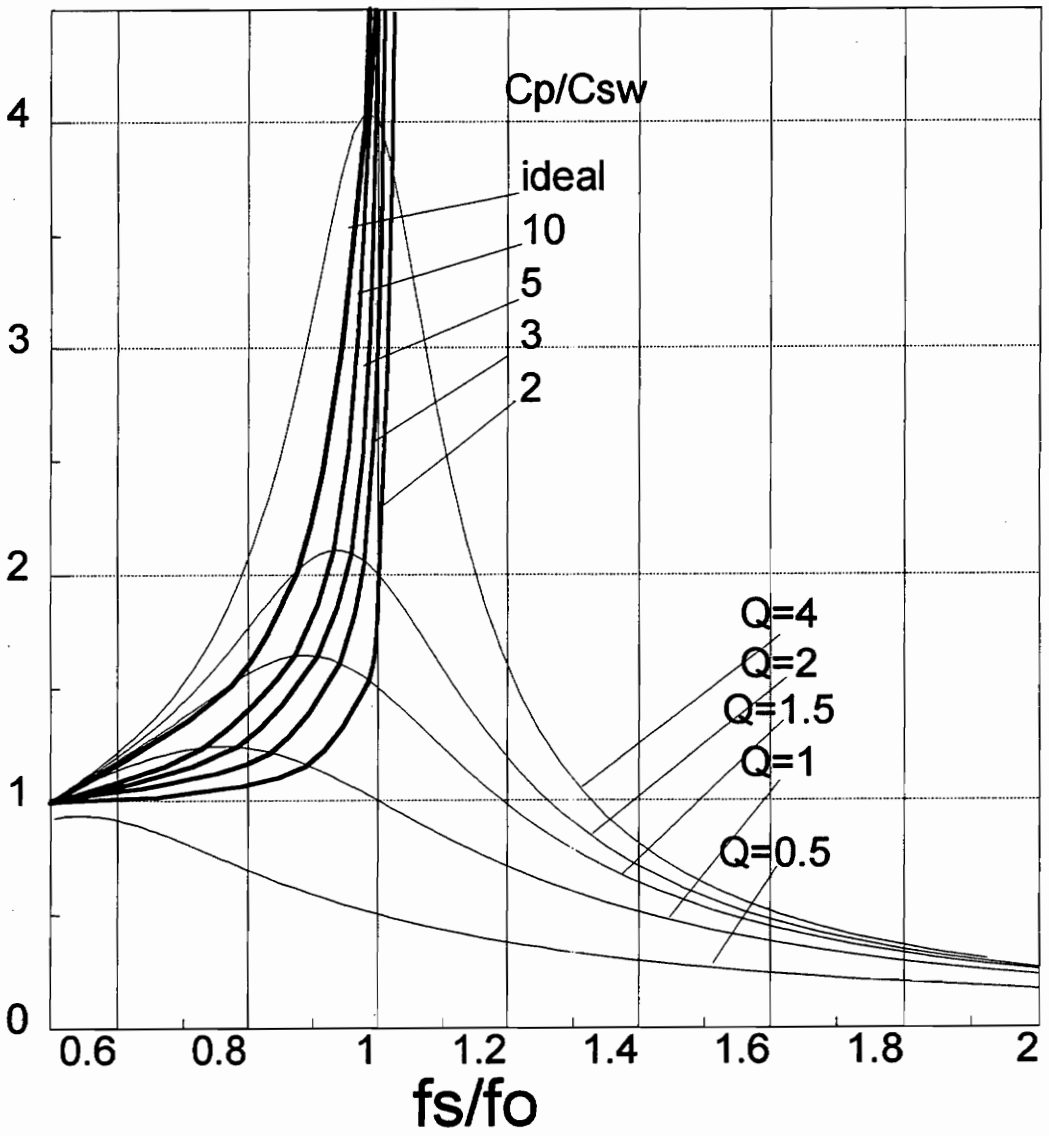


Figure 4.10: Dc characteristics of an ideal PRC, for different values of C_{sw}.

4.3.3 Effects of C_{sw} on the LCC-RC

For ideal switches, C_{oss}=0, and with no external snubber capacitors, the ZVS is achieved at any frequency above the frequency that corresponds to the peak of the voltage gain for a given Q ($Q = R_{load}/Z_o$), as is the case for the PRC. Figure 4.11 shows the dc voltage gain characteristics of the LCC-RC with ideal switches for C_n=1 with the ZVS regions indicated.

The next subsections discuss the effect of switch capacitance on the dc characteristics of the LCC-RC for different values of C_n and C_{sn}.

A) Effects of C_{sw} at Constant C_s/C_p

Figures 4.12(a)-(c) show the dc gain characteristics of the LCC-RC for different ratios of series capacitance C_s to switch capacitance C_{sw}, i.e., for C_{sn} equal to 10, 4, and 1, respectively. Also the regions with ZVS operation are indicated in each graph. As can be seen, the ZVS range shrinks for larger switch capacitance because the ZVS boundary moves towards higher frequencies (away from frequencies for which the voltage gain is maximal for a particular Q). In addition, larger switch capacitances reduce the voltage gain, particularly the peak voltage gains for lower values of Q. Consequently, a wider frequency range is required to regulate the output voltage of the converter against line and load variations. For very large C_{sw}, as for example in Fig. 4.12(c), ZVS is also lost at high frequency, especially for lower values of Q. In fact, in Fig. 4.12(c) no ZVS operation is achievable for $Q \leq 0.25$.

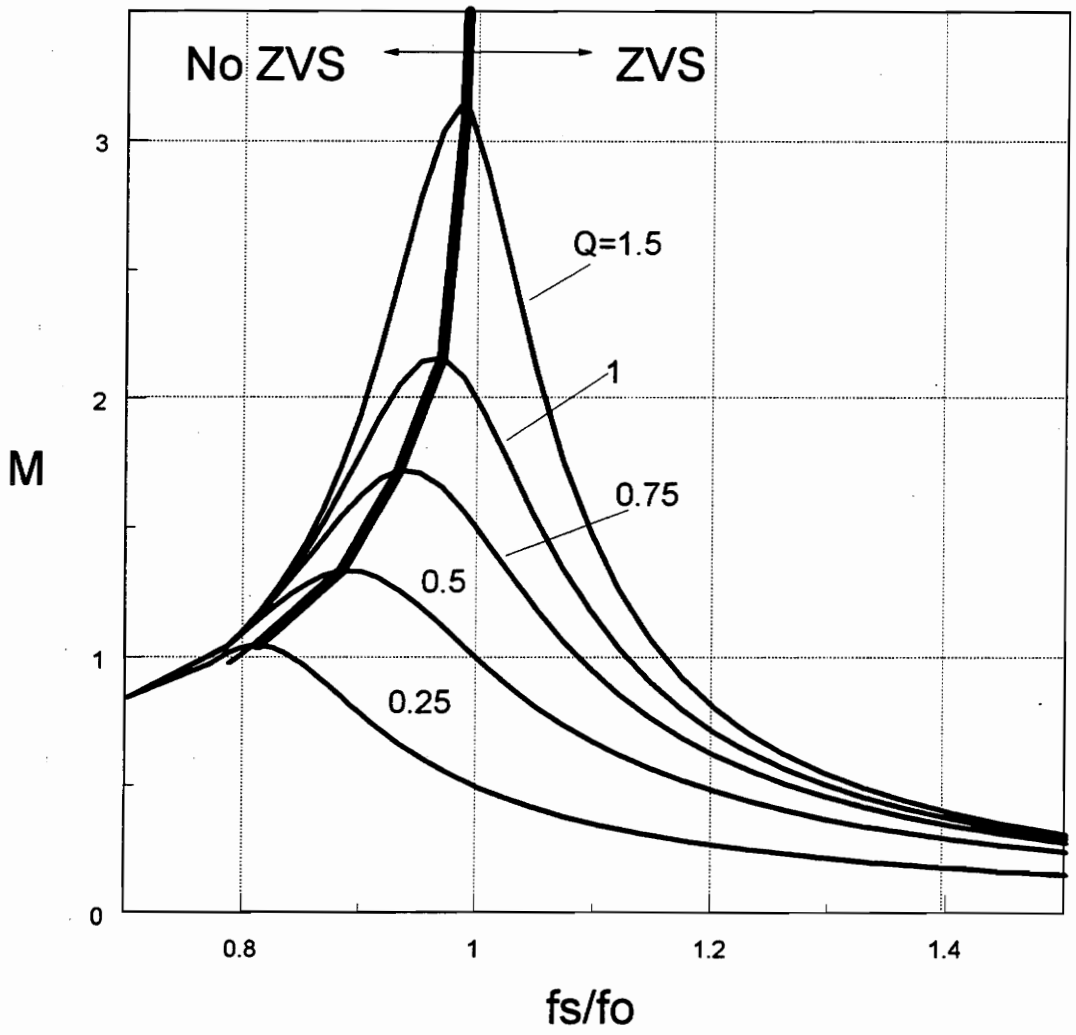


Figure 4.11: Dc characteristics of an ideal SPRC

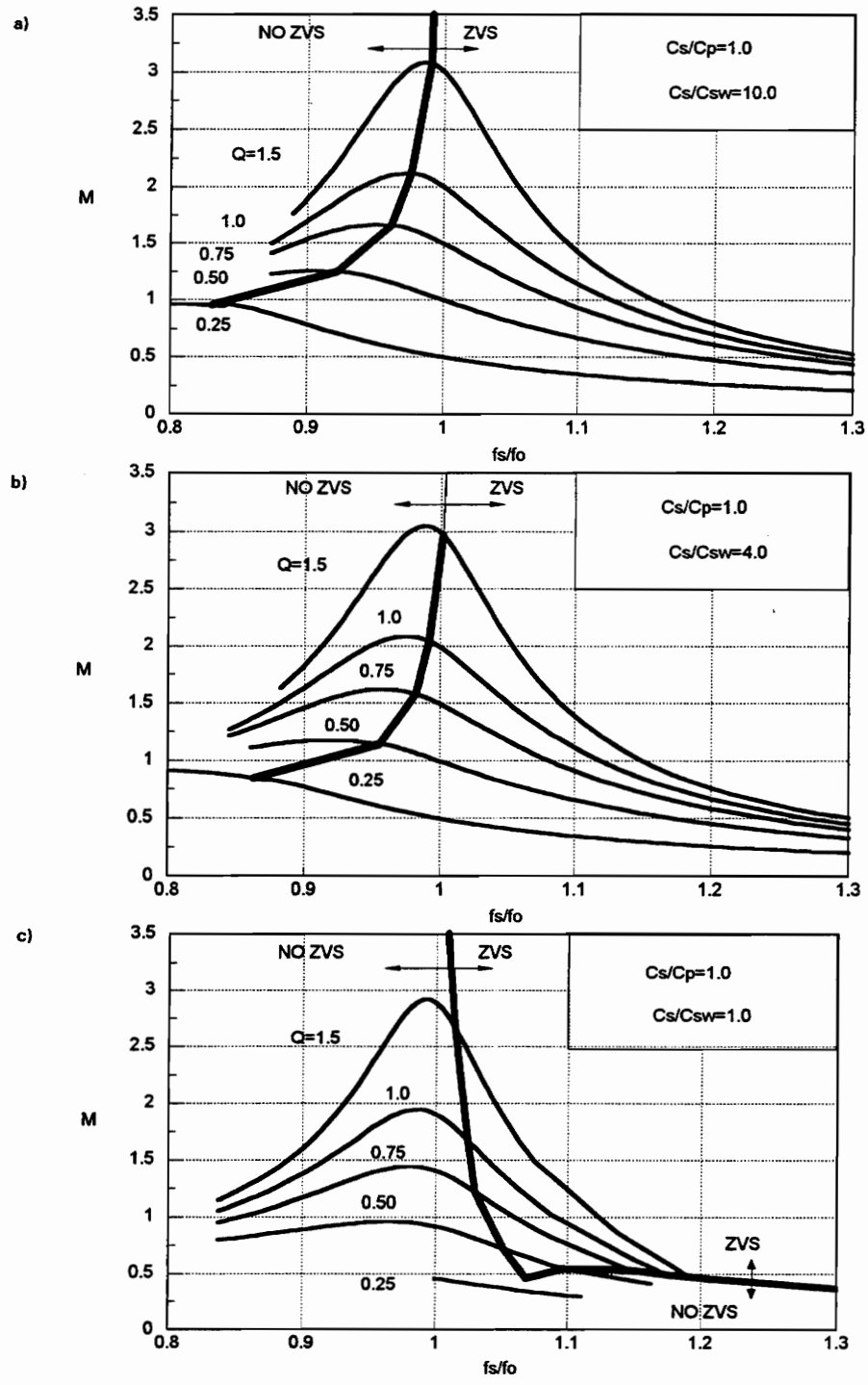


Figure 4.12: Dc characteristics of SPRC for $C_n=C_s/C_p=1$ and: a) $C_{sn}=C_s/C_{sw}=10$, b) $C_{sn}=4$, and c) $C_{sn}=1$.

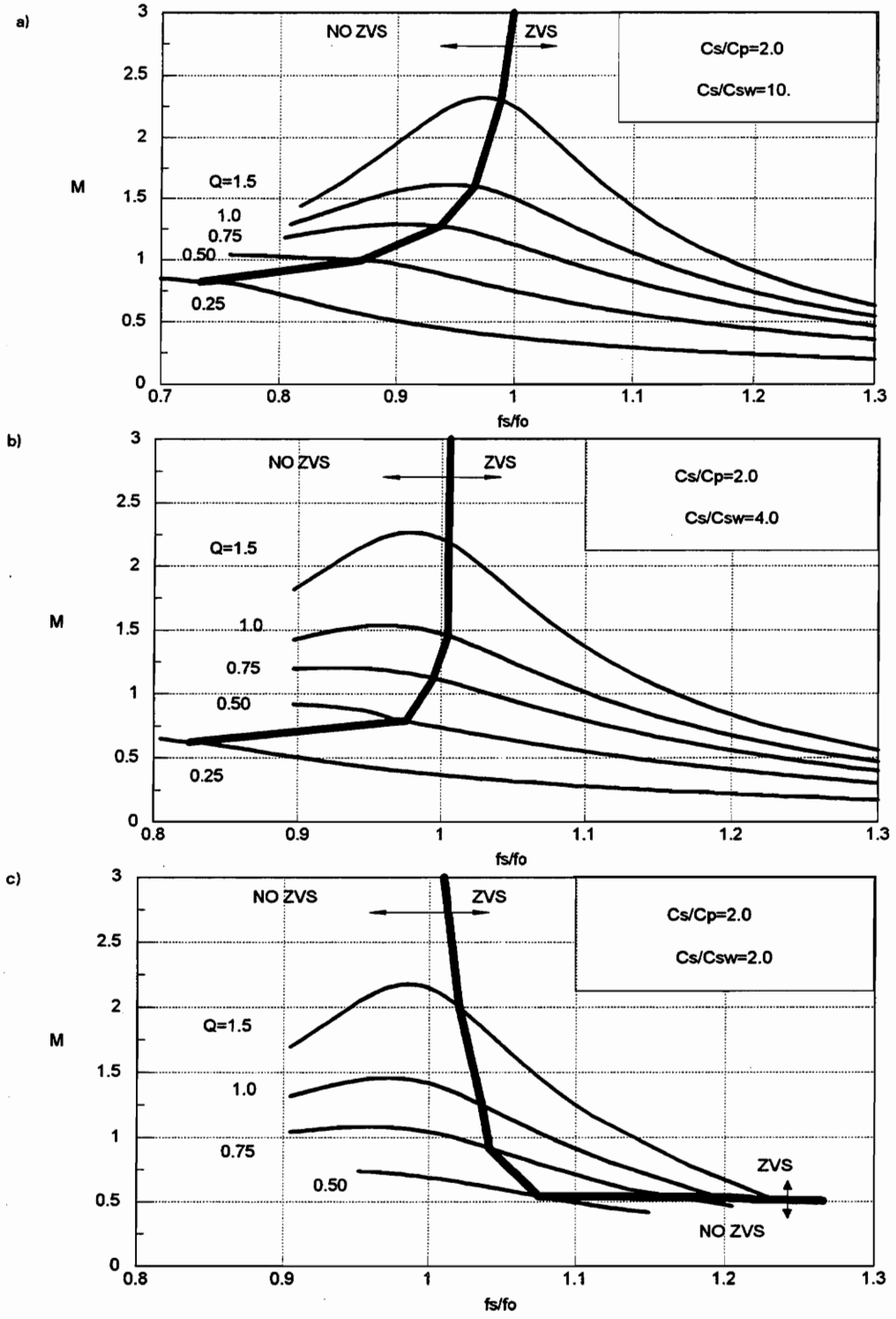


Figure 4.13: Dc characteristics of SPRC for C_n=2 and: a) C_{sn}=10, b) C_{sn}=4, and c) C_{sn}=2.

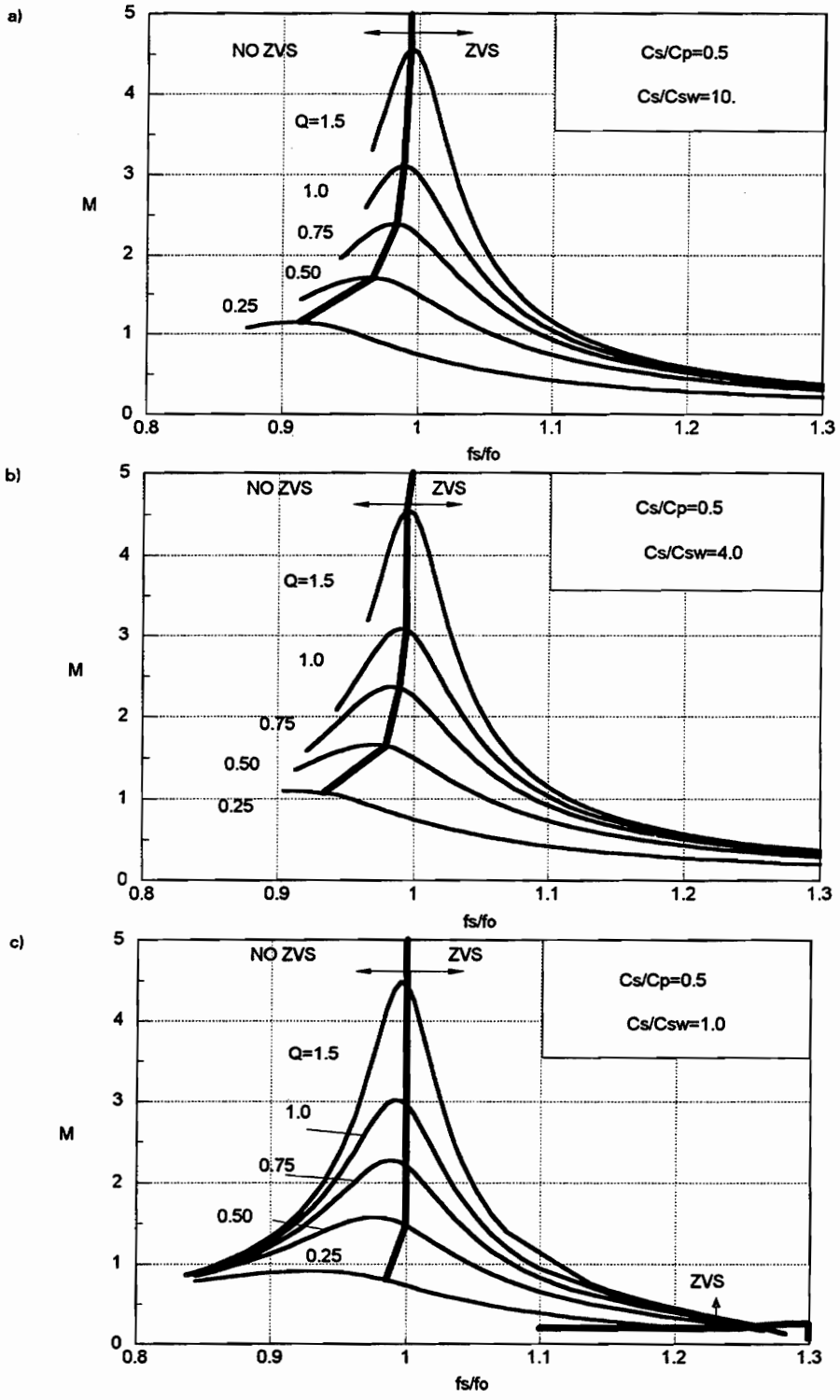


Figure 4.14: Dc characteristics of SPRC for C_n=0.5 and: C_{sn}=10, b) C_{sn}=4, and c) C_{sn}=1.

B) Effects of C_{sw} for different $C_n = C_s / C_p$

To analyze the effect of C_{sw} for different values of C_n, Figs. 4.13 and 4.14 show sets of dc characteristics for $C_n = 0.5$ and $C_n = 2$, respectively. As can be seen by comparing Figs. 4.12, 4.13, and 4.14, the effect of switch capacitance is more pronounced for larger values of C_n (larger values of C_s), i.e., when the converter behaves more as a series-resonant converter (SRC). On the other hand, larger values of C_p that make the converter behave more as a parallel-resonant converter (PRC) diminish the effects of switch capacitance. In both cases, however, the ZVS range decreases and the peak dc voltage gain reduces as the switch capacitance is increased. For example, for $C_n = 2$ and $C_{sn} = 2$ (Fig. 4.13(c)), ZVS is completely lost for $Q<0.5$, while for $C_n = 1$ and $C_{sn} = 1$ (Fig. 4.12(c)), ZVS is lost for $Q<0.25$.

For larger values of C_n (larger C_s, smaller C_n)the LCC-RC behaves like an SRC, and for lower values of C_n (smaller C_s, larger C_p) like a PRC. The effect of the switch capacitance is perfectly consistent with this property of the LCC-RC. For the same C_{sw} ZVS requires operation at higher frequency for the LCC-RC with large C_n values. Also the sensitivity of the voltage gain characteristics to C_{sw} is higher for large C_n, as it is for the SRC.

4.4 Experimental Verifications

To verify the analysis, a prototype LCC-RC has been designed with the following specifications:

- input voltage range from 40 to 60 V,
- output voltage 10 V,
- output power 50 W, and
- minimum switching frequency 900 kHz.

The converter was designed following the guidelines described in chapter 2. According to the guidelines, the optimal design of a LCC-RC requires that the full-load, low-line operating point is selected with a low Q ($Q \leq 0.5$) and for $C_n \approx 1$. For the experimental converter, $C_n = 1$ is selected, and the full-load, low-line operating point is placed on the $Q = 0.5$ curve. The required turns ratio of the transformer for this selection of the operating point is $n = N_p/N_s = 4$, and the resulting resonant components are: C_s = 4.7 nF, C_p = 73 nF (secondary side), and L = 9.2 μH.

To examine the effect of switch capacitance, two devices with significantly different values of C_{oss} were used for the primary switches. Figure 4.15, shows the operating region of the converter when IRFP240 devices (R_{DSon} = 0.18 Ω, C_{oss} = 350 pF at 25 V) are used. Note that for the dc characteristics in Fig. 4.15, C_{sn} = 10, which is close to the value of the ratio for the series resonant capacitor (C_s = 4.7 nF and the output capacitance of IRFP240 (C_{oss} = 350 pF). As can be seen from Fig. 4.15, the operating point A (V_{in} = 48 V) is within the ZVS region. Figure 4.16 that shows the oscillograms of the gate-drive signal, drain-to-source, and current for one of the switches of the experimental circuit with the IRFP240 devices confirms this result.

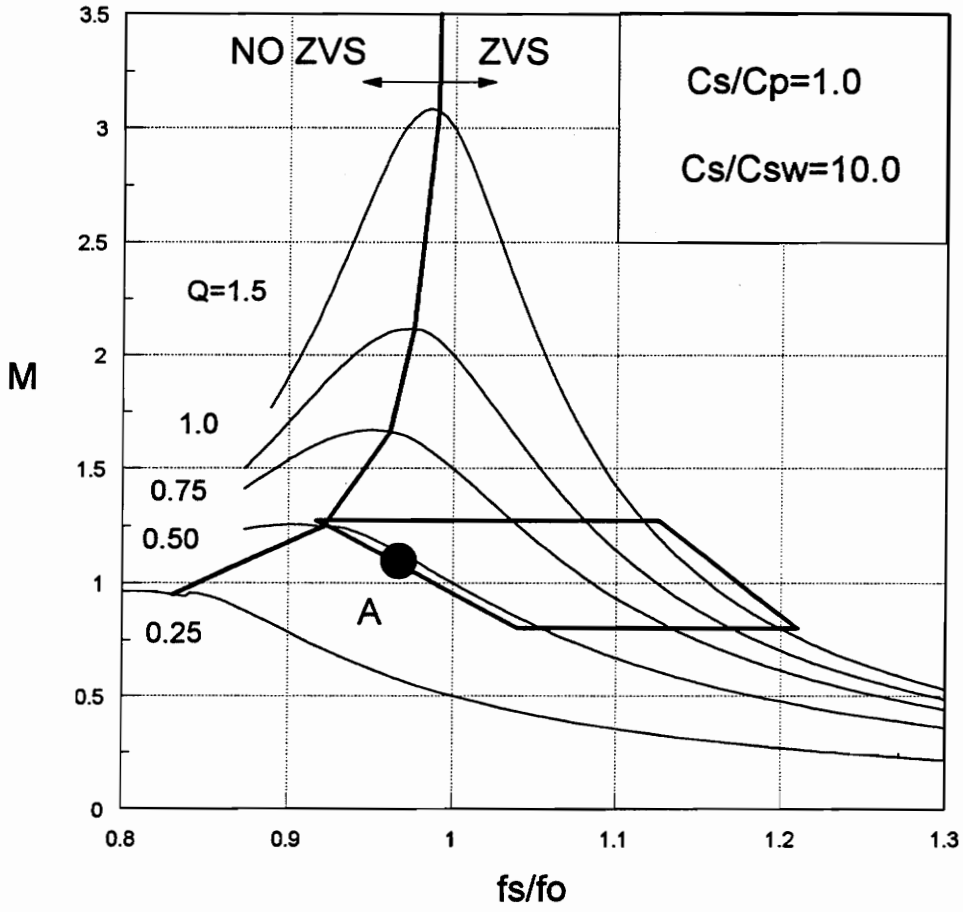


Figure 4.15: Dc characteristics for C_{sn}=10.

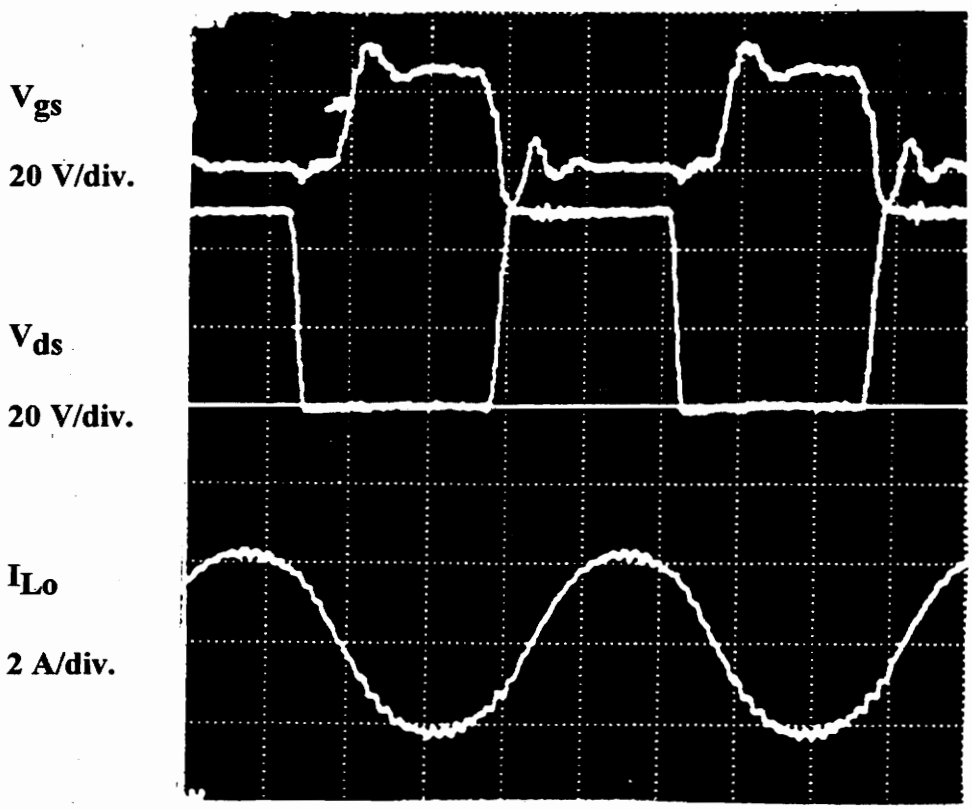


Figure 4.16: Voltage and current waveforms of switch Q1, with ZVS operation.

Figure 4.17 shows the operating region of the converter when IRFP150 devices (R_{DSon} = 0.055 Ω, C_{oss} = 1 nF at 25 V) are used. For the dc characteristics in Fig. 4.10, C_{sn} = 4 corresponds to the C_{sn} of the experimental converter with the IRFP150's. The operating point for V_{in} = 48 V (point B in Fig. 4.10) in this design is in the region where ZVS is lost. The oscillogram in Fig. 4.18 verifies this finding. As can be seen, the voltage across the device peaks before reaching the input voltage, and consequently, the antiparallel diode is not turned on before the device starts conducting. The loss of ZVS results in increased switching losses and increased voltage ringing across the devices.

4.5 Summary and Conclusions

An analysis of the resonant converters (SRC, PRC and LCC-RC) operating above resonant frequency that includes the effects of the capacitance of the primary switches is presented. It was shown that switch capacitance has significant effects on the dc voltage-conversion ratio characteristics and the zero-voltage-switching range of the converter.

The SRC is the most sensitive of the three, with significant changes in the ZVS range and voltage gain. The PRC is the least sensitive, with negligible changes in voltage, but still changes in the ZVS range.

For all three converters the effects are especially pronounced for lower values of the Q-factor of the resonant tank and higher ratios of the series to parallel resonant capacitors. Since the optimal design of the LCC-RC requires operation at lower values of Q, the results of the analysis are extremely useful in design optimization of the LCC-RC in

the presence of a significant capacitance across the primary switches, either because of a large output capacitance in the devices or an intentionally added capacitance of lossless capacitive snubbers.

The analysis is verified experimentally on a 50 W, 900 kHz LCC-RC converter.

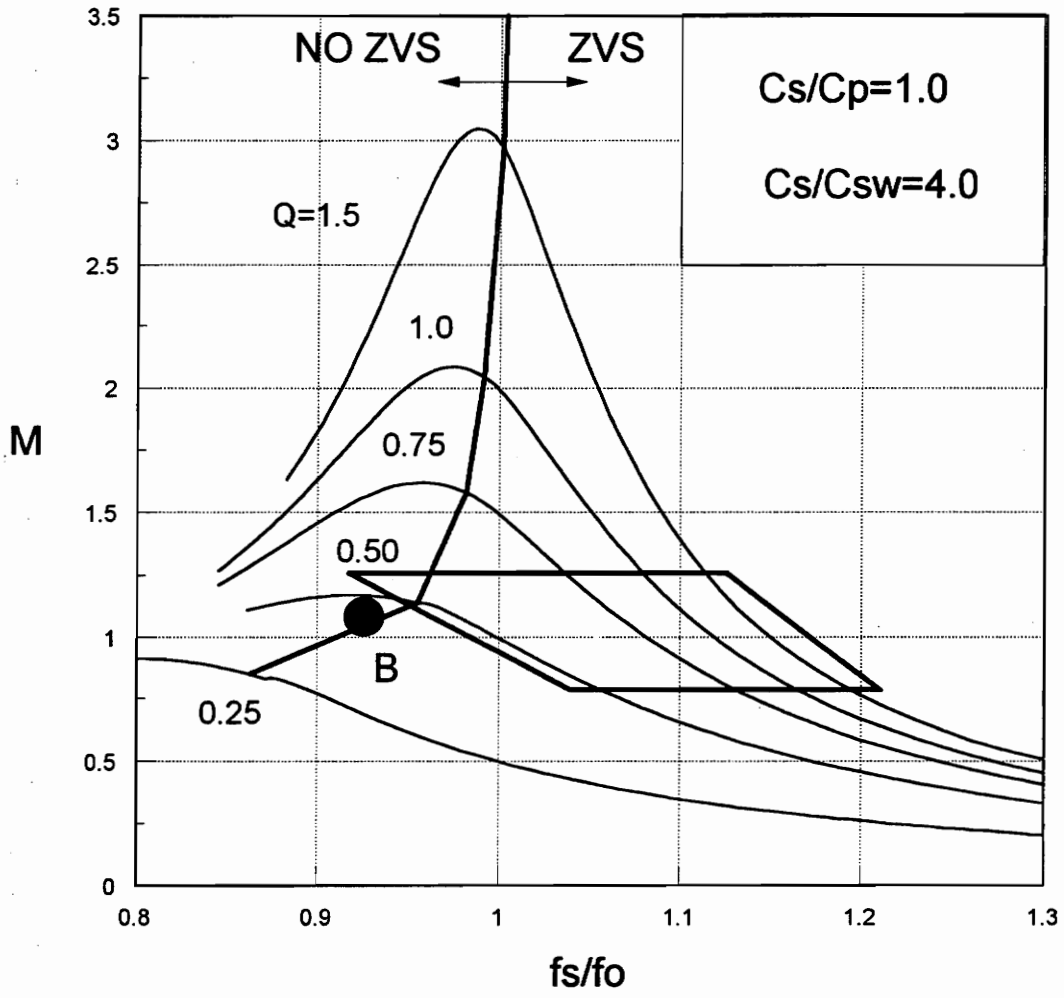


Figure 4.17: Dc characteristics for C_{sn} = 4.

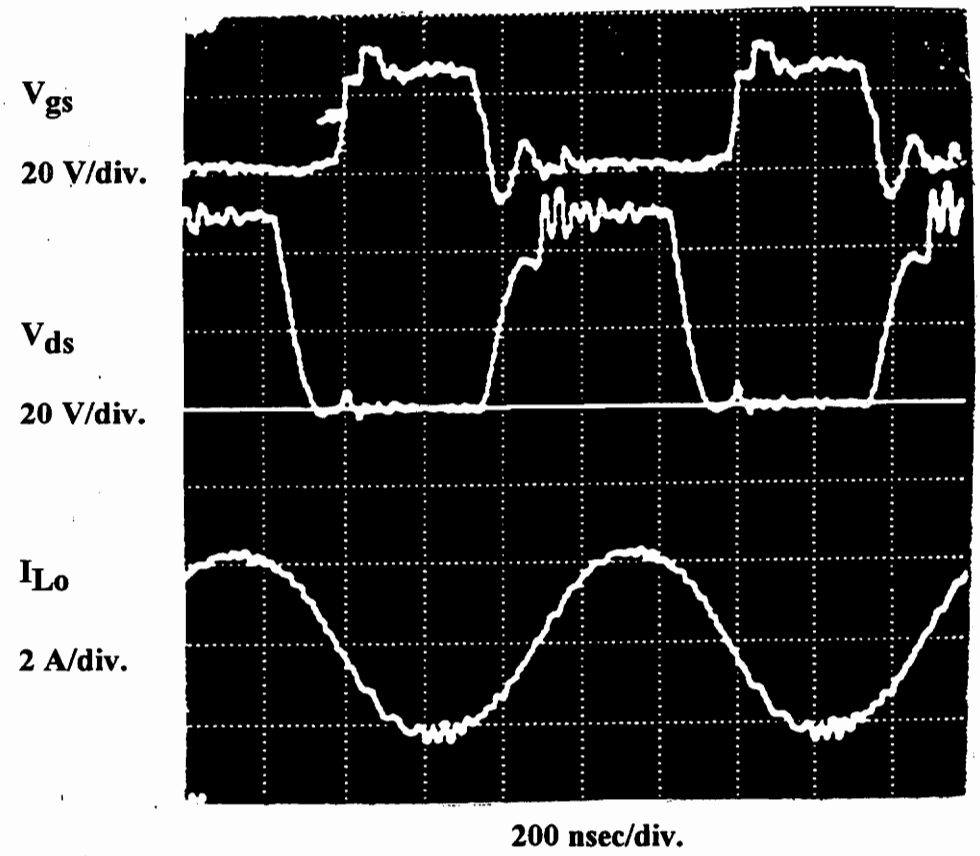


Figure 4.18: Voltage and current of switch Q1, without ZVS operation.

5. Phase-Shifted Full-Bridge PWM Converter with Active Clamp

5.1 Introduction

The research and application of zero-voltage switching (ZVS) for the class of PWM converters is gaining increasing attention, as this converter family combines the simplicity of PWM converters with the soft-switching characteristics of resonant converters. The member of this family that is most widely used, especially in high-power and high-voltage applications, is the ZVS full-bridge (FB) PWM converter [G-6, G-11, G-17]. This converter is controlled by the phase-shifted PWM technique which enables the use of all parasitic elements in the bridge to provide ZVS conditions for the active switches.

When conventional PWM converters are operated at high frequencies, the circuit parasitics have detrimental effects on the converter performance. Switching losses are

especially pronounced in high-power high-voltage applications. Snubbers are required, thus adding significant losses in high-frequency operation. In the conventional full-bridge PWM converter, the diagonally opposite switches (Q1 and Q2, or Q3 and Q4) are turned on and off simultaneously, as shown in Fig. 5.1. When all four switches are turned off the load current freewheels through the rectifiers, and the energy stored in the leakage inductance of the power transformer causes severe ringing with FET junction capacitances.

To minimize the parasitic ringing, the gate signals for Q2 and Q4 are delayed (phase-shifted) with respect to those of Q1 and Q3, so that the primary of the transformer is either connected to the input voltage or shorted. The leakage inductance current is never interrupted, thus solving the problem of the parasitic ringing associated with the conventional full-bridge PWM converter. Furthermore, the energy stored in the leakage inductance can be used to discharge the energy stored in the FET junction capacitances to achieve ZVS conditions for all four switches in the primary side. The converter requires no additional resonant components; Fig. 5.2 shows the topology of the converter and the gate drive signals required.

The current stress for the bridge is larger than for the conventionally operated PWM full-bridge, but it provides low-loss switching and reduced ringing amplitude in the primary switches, together with a less restricted design of the power stage transformer, which may have a significant leakage inductance without detrimental effects on the converter performance.

Summarizing the main features of the ZVS-FB-PWM converter [G-17] are:

- PWM control at a fixed frequency.
- ZVS for the active switches with much reduced switching stress, switching losses and EMI.
- A minimal number of components.
- The internal diodes of the MOSFET's can be used since fast recovery diodes are not required in the bridge.
- The leakage inductance in the transformer is used to provide the ZVS.

These advantages, however, are accompanied by the following disadvantages with respect to a conventional FB-PWM converter:

- The rms currents in the bridge are increased due to the presence of circulating current components.
- The effective-duty-cycle range is reduced as the leakage inductance of the transformer increases in order to attain ZVS.

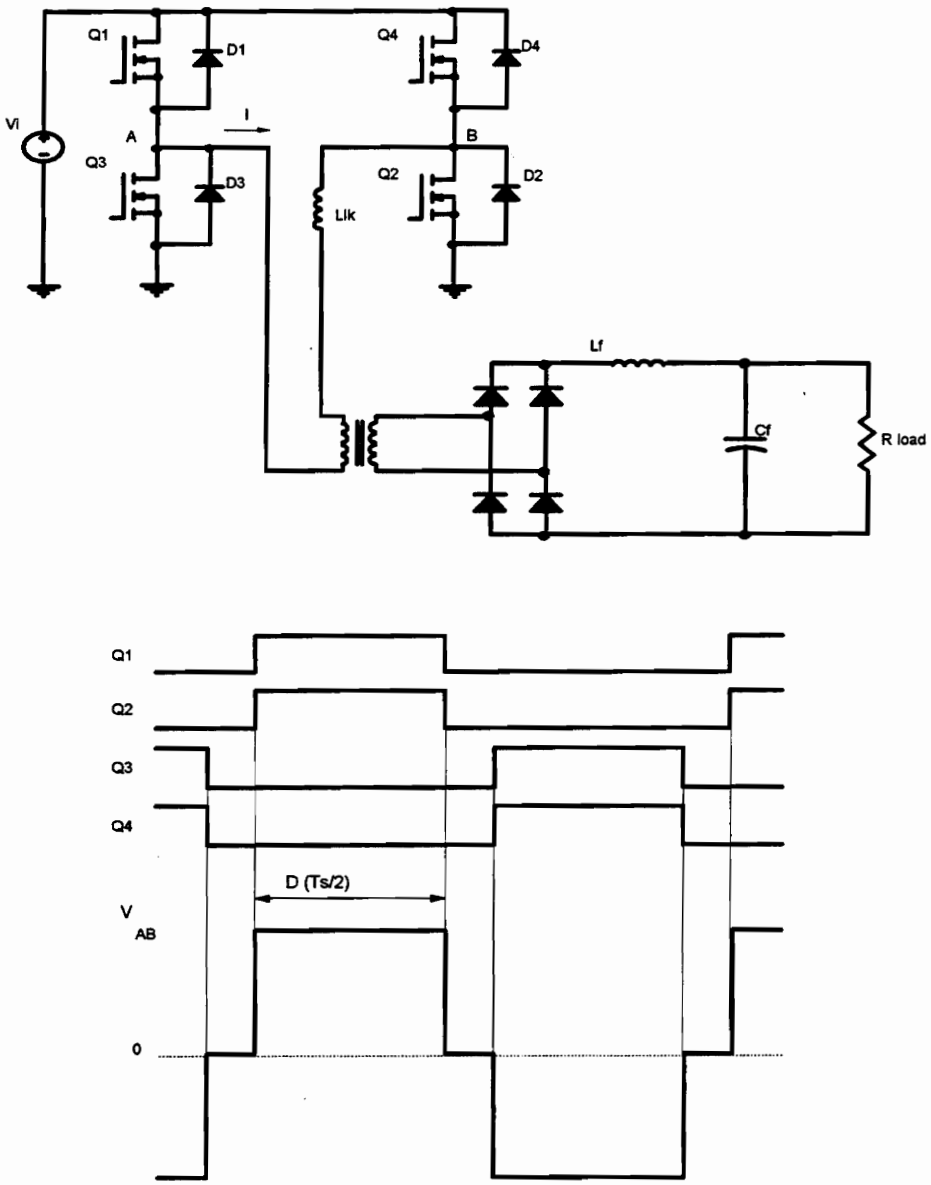


Figure 5.1: Conventional full-bridge PWM converter topology.

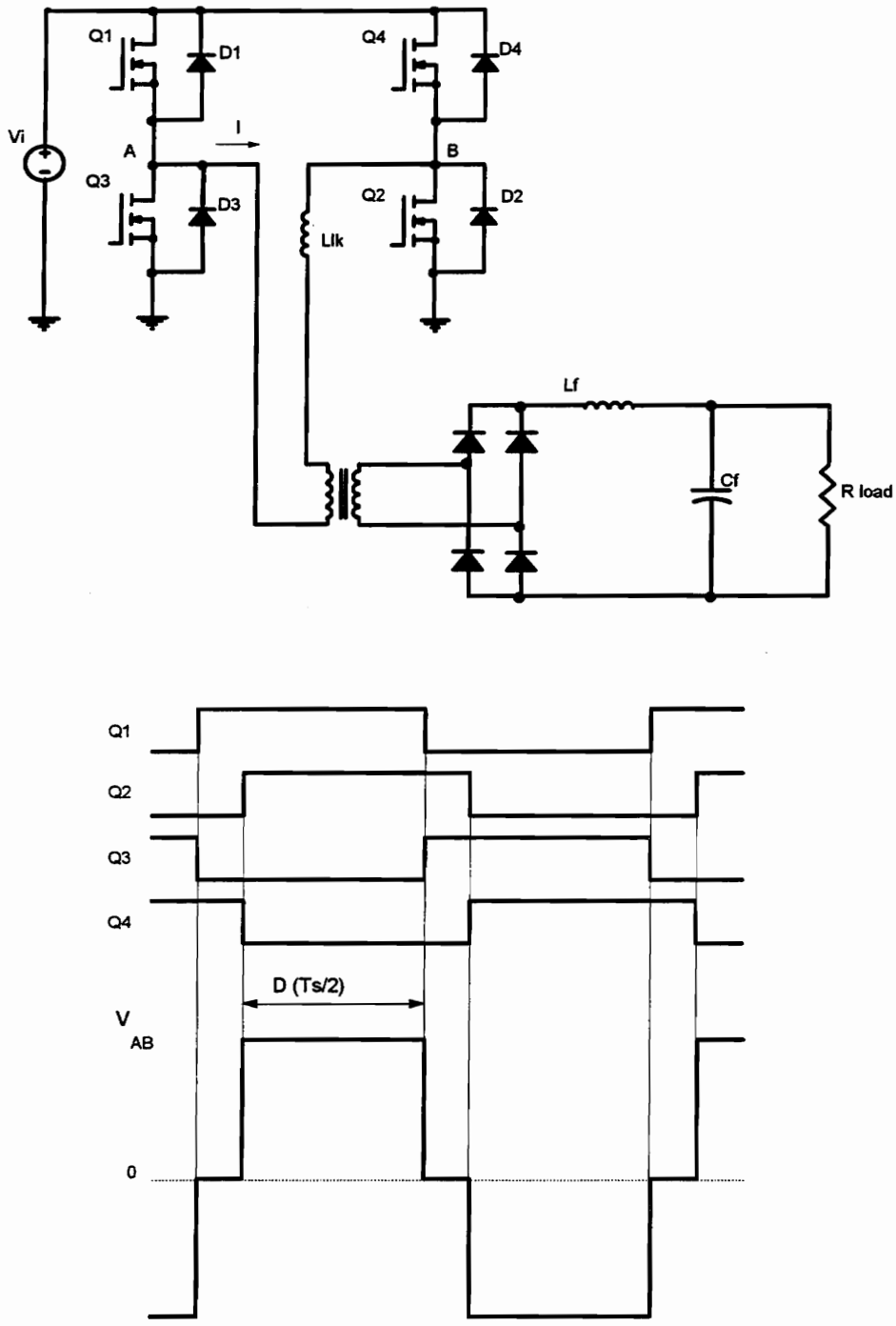


Figure 5.2: Full bridge ZVS PWM converter topology.

5.2 Operation Principle

Figure 5.3 shows the waveforms of the primary voltage and current and the secondary voltage, highlighting their main characteristics. The converter operation for a half cycle is described as follows:

t_1 to t_2: In the primary, Q4 and D1 are conducting. In the secondary Dc and Dd are conducting. The primary current follows the output filter current.

t_2^-: Switch Q4 turns off, and the current through the primary of the transformer charges the output capacitance of Q4 and discharges the output capacitance of Q2, turning on the diode D2.

t_2: Diode D2 starts conducting, Q2 can be turned on with virtually no voltage applied (only the forward drop of the parallel diode), (Fig. 5.3.1).

t_2 to t_3: The primary current circulates through diodes D1 and D2. The secondary of the transformer is shorted by the diodes of the rectifier stage. (Fig. 5.3.2.).

t_3 to t_4 The primary current circulates through Q1 and Q2. The secondary of the transformer is shorted. (Fig. 5.3.2.).

t_4 to t_5: The voltage in the secondary of the transformer starts increasing, and the leakage inductance of the transformer starts resonating with the diodes' capacitance. (Fig. 5.3.3.).

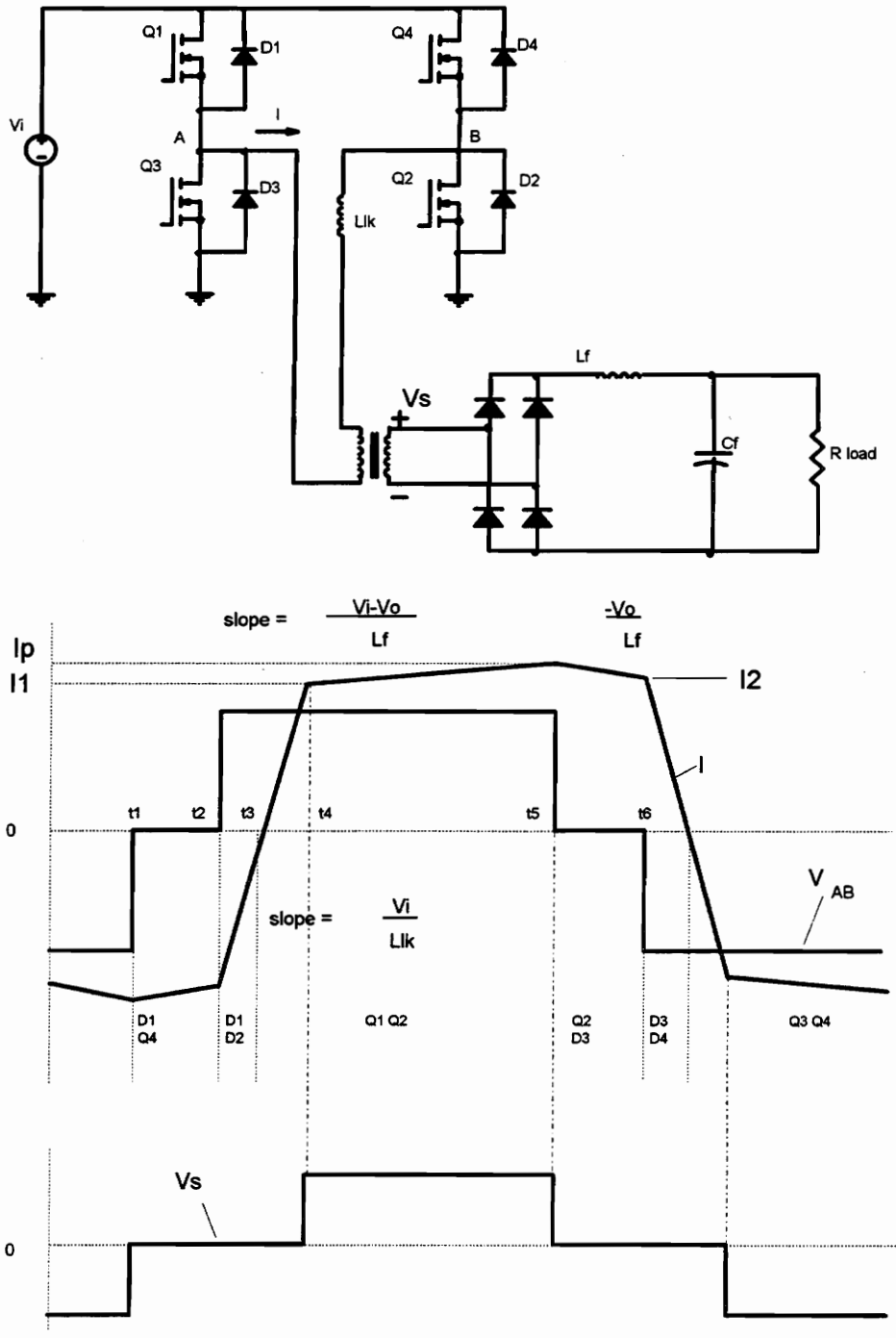


Figure 5.3: Circuit topology, primary current and voltage, and secondary voltage.

t_5^-: Switch Q1 turns off and the current through the primary discharges the output capacitance of Q3 and charges the output capacitance of Q1. When Q1 turns off, the current through the primary of the transformer is the output current reflected to the primary. The energy of the output filter inductor is used to achieve ZVS, and therefore ZVS is easily attained for switches Q1 and Q3.(Fig. 5.3.4)

t_5: Diode D3 is turned on. After D3 starts conducting, Q3 can be turned on with no voltage applied across it (Fig. 5.3.5).

In summary, the switching conditions for the switches are:

- Q2 and Q4 turn on with ZV when the energy stored in the leakage inductance is enough to discharge their output capacitances.
- Q1 and Q3 turn on with ZV over a range that is always larger than that of Q2 and Q4, because the energy in the output filter inductor is used to discharge the switches' capacitance.

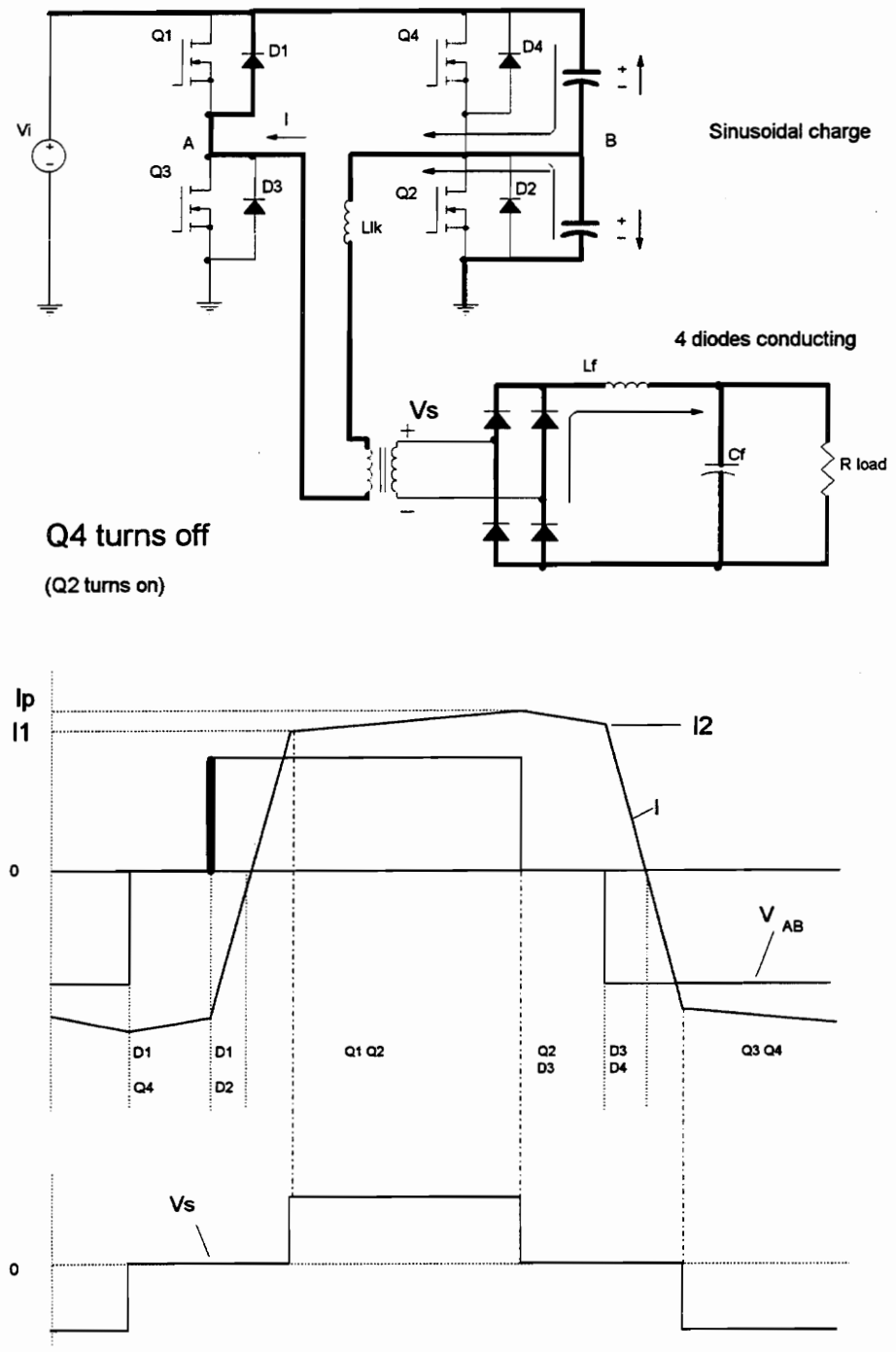


Figure 5.3.1: Current path when Q4 is turned off.

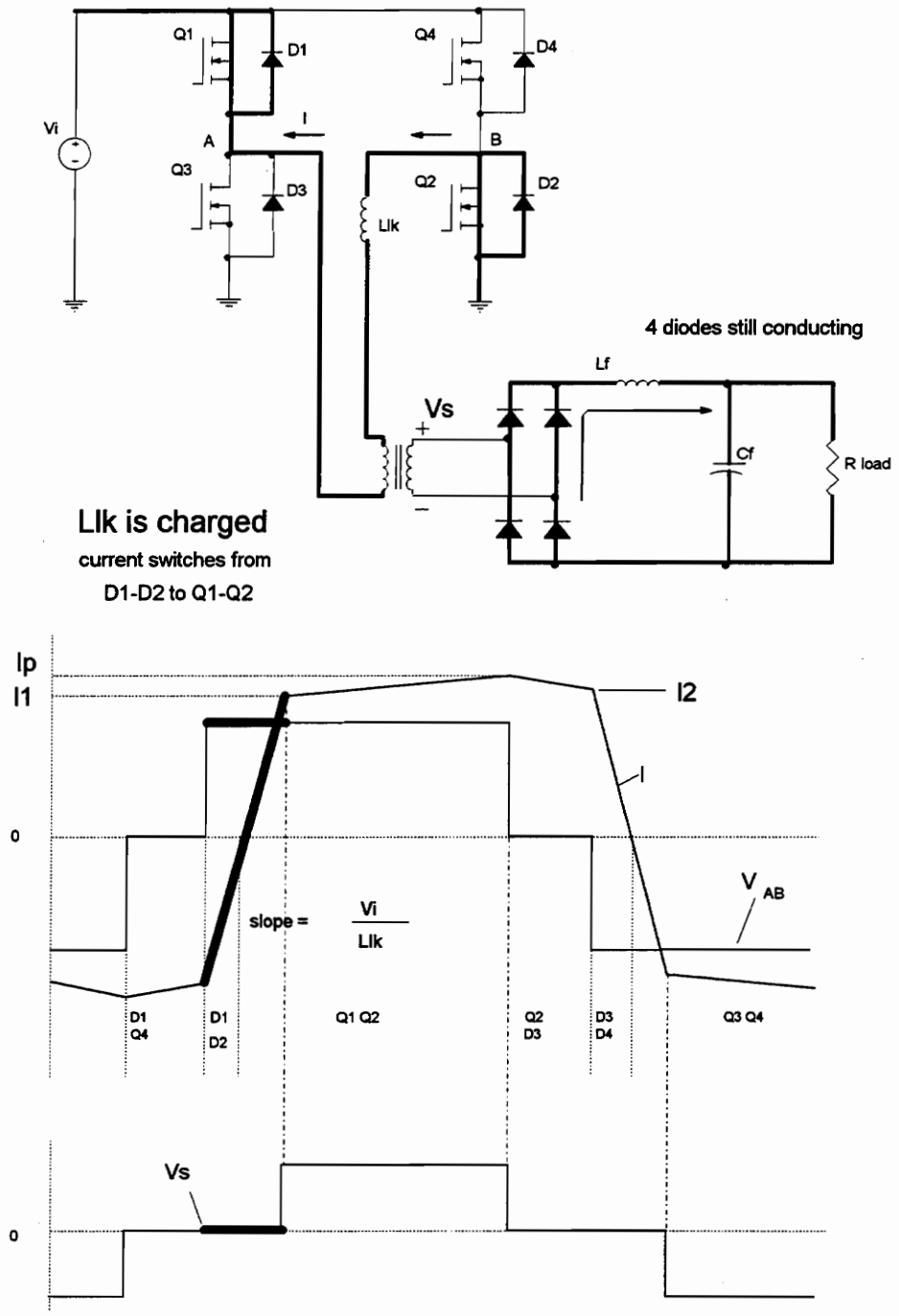


Figure 5.3.2: Current path when D1 is conducting.

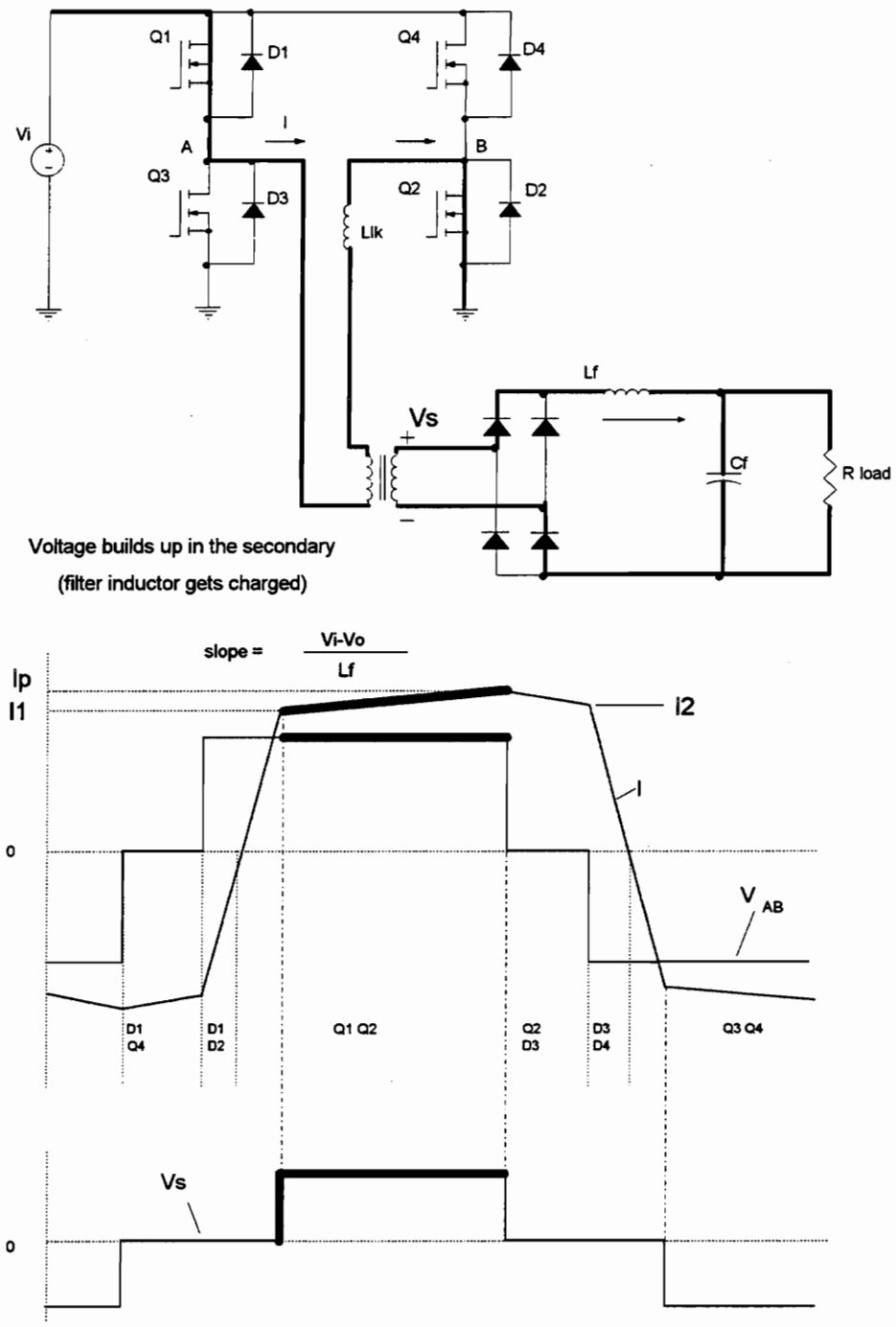


Figure 5.3.3: Current path when Q1 and Q2 are conducting.

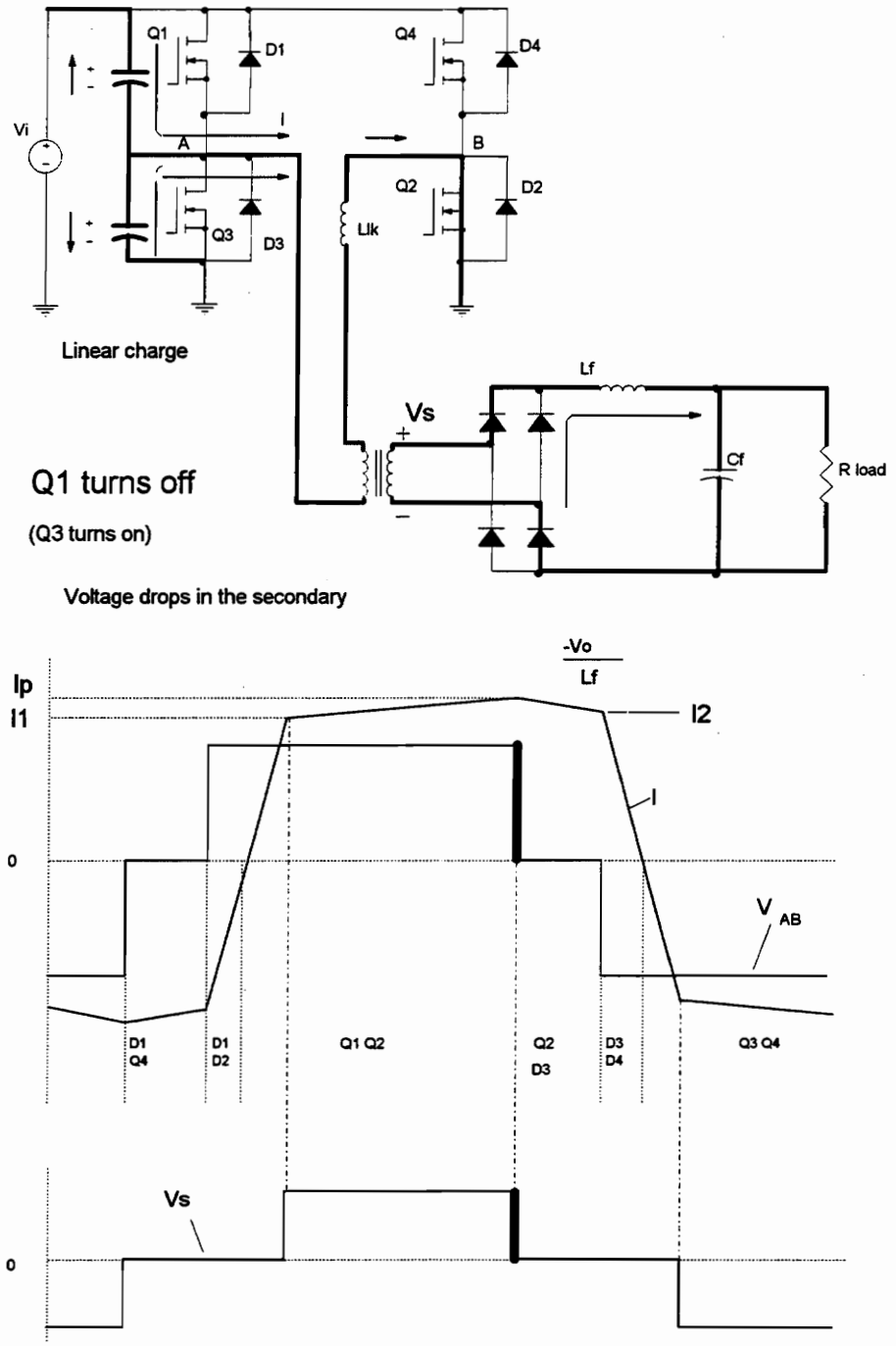


Figure 5.3.4: Current path when Q1 is turned off.

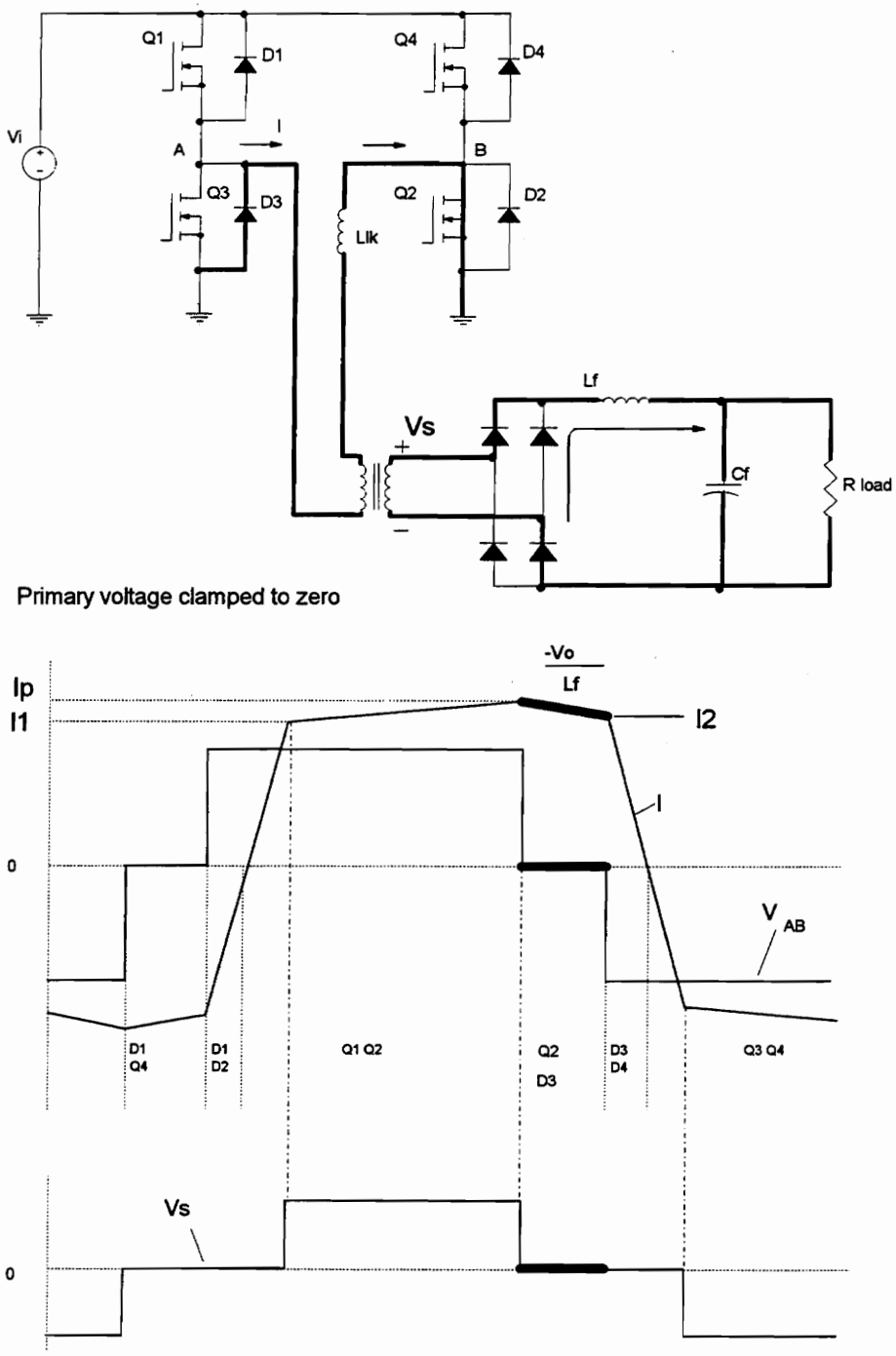


Figure 5.3.5: Current path when Q2 and D3 are conducting.

5.3 Converter Analysis

5.3.1 Conditions for Zero-Voltage Switching

The FB-ZVS-PWM converter provides ZVS for all four switches in the bridge. However, the mechanism by which ZVS is achieved is different for both legs of the bridge.

For transistors Q2 and Q4, the ZVS is provided by the resonance between the leakage inductance, L_{lk}, and the output capacitance of the switch. Figure 4.4 shows the waveform of the current through D2-Q2 and the rising edge of the transformer primary voltage waveform for different operating conditions.

Before Q2 is turned off, the current in the primary is flowing through the diode D3 and transistor Q2. The primary voltage is clamped to zero, and the value of the of the primary current is equal to the reflected filter-inductor current. When Q2 turns off, the current through the primary reduces rapidly. This causes the filter-inductor current to start freewheeling through the rectifiers. The energy stored in the primary leakage inductance turns on diode D4. In order to turn on D4, the output capacitance of Q4 has to be discharged first and the output capacitance of Q2 charged up to the input voltage. The energy available for charging the output capacitances of Q4 and Q2 is the energy stored in L_{lk} when Q2 is turned off. The transformer winding capacitance across the primary winding also has to be charged in the process. To accomplish this, the following inequality has to be met:

$$E = \frac{1}{2} \cdot L_{lk} \cdot I_2^2 \geq \frac{4}{3} \cdot C_{MOS} \cdot V_{in}^2 + \frac{1}{2} \cdot C_{tr} \cdot V_{in}^2 \qquad (5.1)$$

where I_2 is the current through the primary when Q2 turns off, V_{in} is the input voltage, L_{lk} is the transformer leakage inductance, C_{MOS} is the output capacitance of the switch at V_{in}, and C_{tr} is the transformer winding capacitance. The term $\frac{4}{3} \cdot C_{MOS} \cdot V_{in}^2$ corresponds to two times the energy stored in the nonlinear drain-to-source capacitor, whose capacitance is inversely proportional to the square root of the voltage.

The resonance between L_{lk}, C_{MOS}, and C_{tr} provides a sinusoidal voltage across the capacitances that reaches a maximum at one fourth of the resonant frequency period. The dead time between Q2 and Q4 has to be set at $\delta\tau_{max}$ to ensure that there is sufficient time to charge/discharge the capacitances. The dead time required to ensure ZVS with the maximum possible load range can be determined by the following equation:

$$\delta\tau_{max} = \frac{T}{4} = \frac{\pi}{2} \cdot \sqrt{L_{lk} \cdot C} \tag{5.2}$$

where $C = C_{MOS} + C_{tr}$.

Figure 5.4 presents the voltage across the transistor Q2 at turn-off. In the first voltage waveform, the energy in L_{lk} is equal to the energy required to charge the capacitances. In the second voltage waveform, the energy in L_{lk} is larger than the energy required to charge the capacitors. The switch output capacitance is charged in less than $\delta\tau_{max}$, and the voltage is clamped to the input voltage. In the last voltage waveform, the energy in L_{lk} is not enough to charge the output capacitances, and ZVS is lost after the dead time, $\delta\tau_{max}$; Q4 (or Q2) is turned on; and the voltage increases immediately to V_{in}.

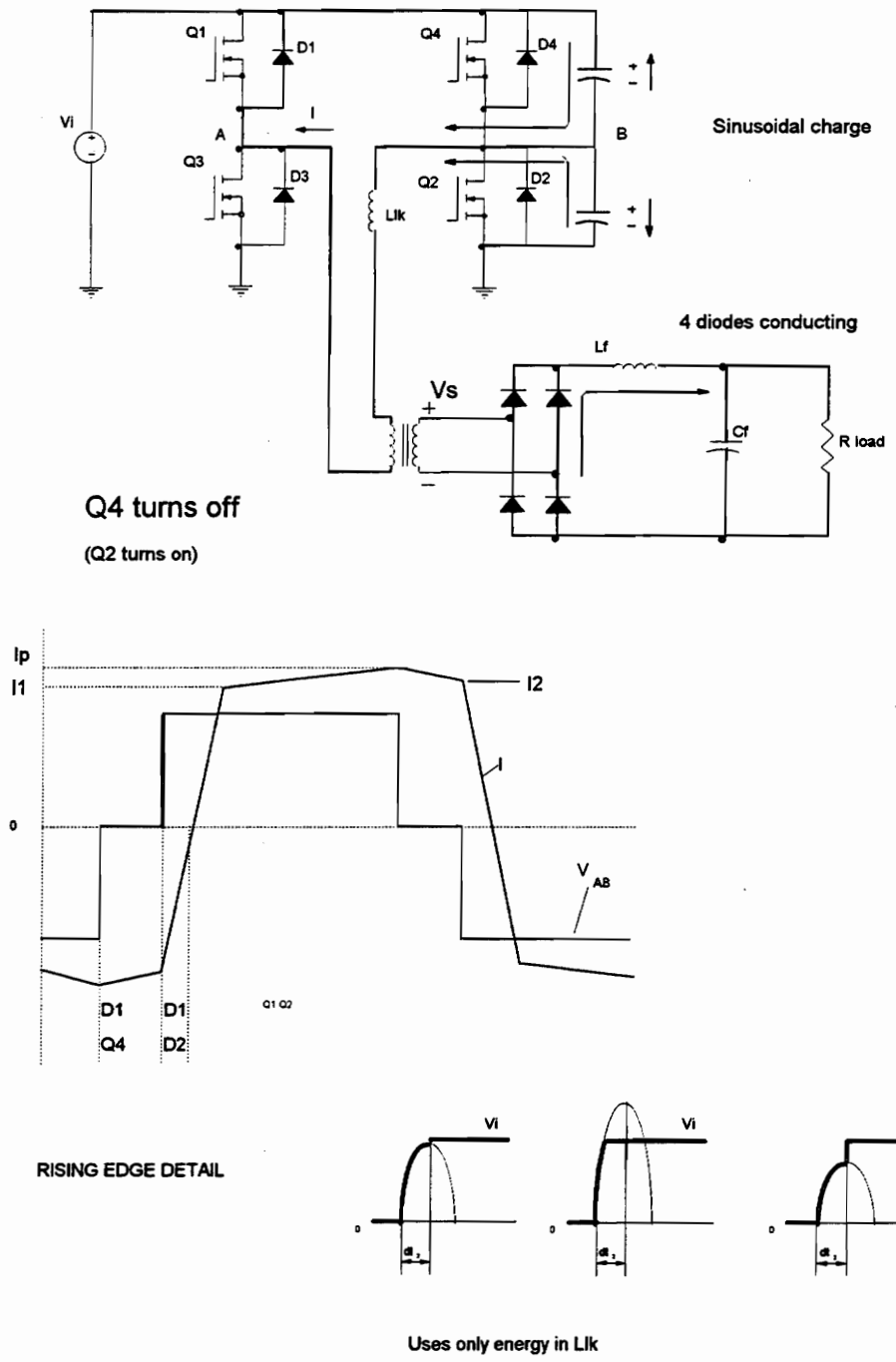


Figure 5.4: Current through switch Q2 and voltage rising edge for different load conditions.

Whether ZVS can be achieved for Q2 and Q4 is dependent on the load level of the converter. For light loads, the current through L_{lk}, when Q2 or Q4 are turned off, may not be enough to turn on the antiparallel diode.

For switches Q1 and Q3, ZVS is provided by a different mechanism. Before Q1 is turned off, the current in the primary is reaching its peak value. The primary current is the filter inductor current reflected to the primary. When Q1 is turned off, the energy available to charge the output capacitance of Q1 and discharge the output capacitance of Q3 is the energy stored in L_{lk} and the energy in the output filter inductor. This energy in the output filter inductor is available because the filter inductor current does not freewheel through the rectifier until the voltage across the secondary has fallen to zero.

Since the energy in the filter inductor is large compared to the energy stored in the capacitances in the primary, the charging of the switches can be approximated by a linear charging with a constant current. Consequently, the dead time $\delta\tau_1$, required between the turn-off of Q1 and the turn-on of Q3 can be determined from the equation

$$\delta\tau_1 \cdot I_p = 4 \cdot C_{MOS} \cdot V_{in} , \tag{5.3}$$

where the term $4 \cdot C_{MOS} V_{in}$, corresponds to twice the charge stored in the nonlinear output capacitance of the MOSFET, and I_p is the peak current in the output filter inductor reflected to the primary. The dead time can be calculated for the minimum I_p chosen to achieve ZVS. If load current is further reduced, the ZVS property can not be maintained. Figure 5.5 presents the current through D1-Q1 and the detail waveform during the linear charge interval of the output capacitances of the switches.

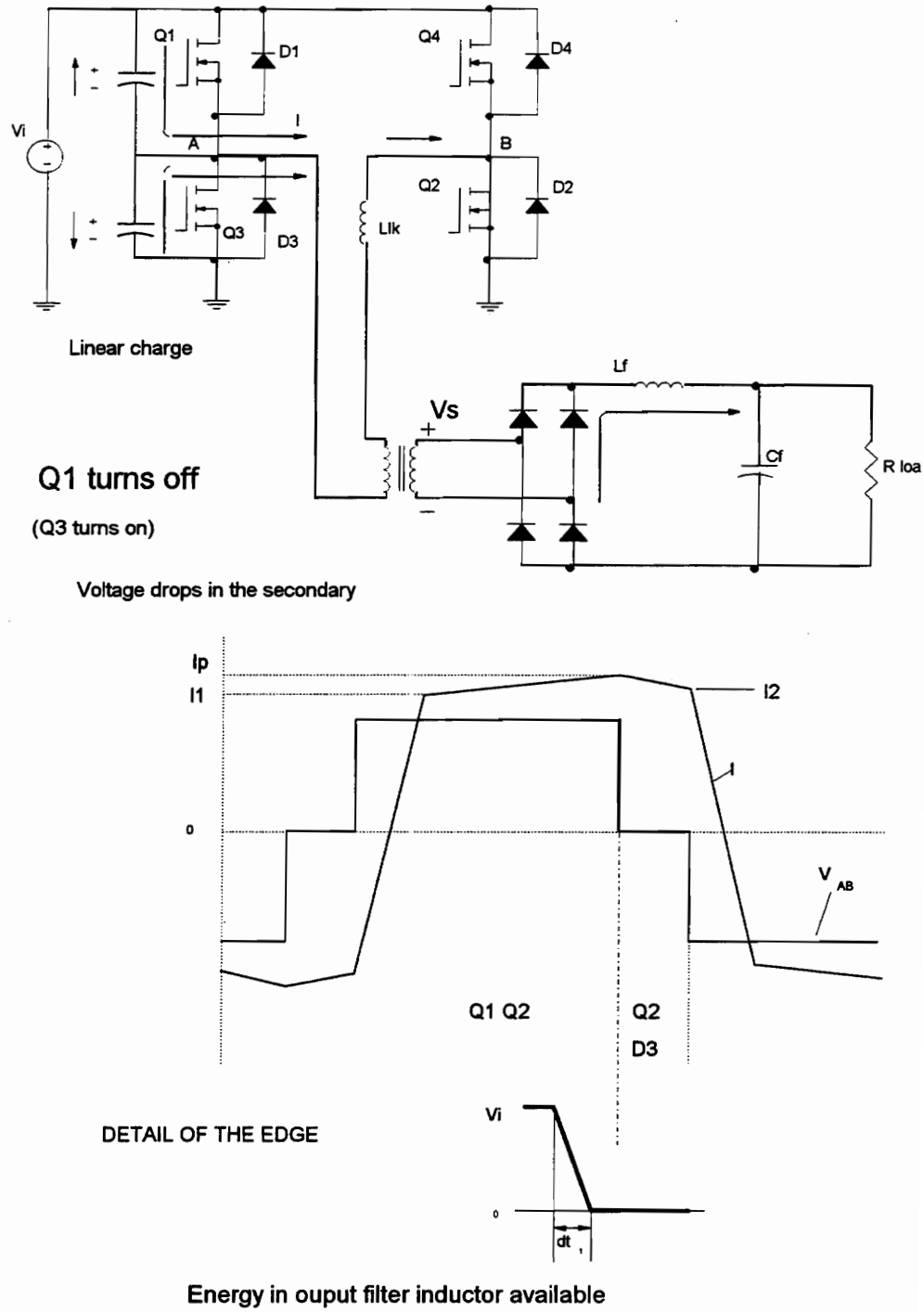


Figure 5.5: Current through switch Q2 and voltage rising edge.

5.3.2 Critical Current for Zero-Voltage Switching

The ZVS for Q1 and Q3 can be achieved even at light loads because D1 and D3 can always be turned on by the energy stored in the output filter inductance. However, ZVS for Q2 and Q4 can only be achieved for a load current above the critical value, I_{crit}. Using Eq. (5.1),

$$I_{crit} = \sqrt{\frac{2}{L_{lk}} \cdot \left(\frac{4}{3} \cdot C_{MOS} \cdot V_{in}^2 + \frac{1}{2} \cdot C_{tr} \cdot V_{in}^2 \right)} \quad . \tag{5.4}$$

The available current through L_{lk} at t_2 can be calculated by

$$I_2 = \frac{N_s}{N_p} \cdot \left(I_{load} + \frac{\Delta I}{2} - \frac{V_{out}}{L_{lk} + L_f} \cdot (1-D) \cdot \frac{T}{2} \right) \tag{5.5}$$

where L_f is the filter inductance, V_{out} is the output voltage, D is the duty cycle in the primary, T is the switching period, I_{load} is the average output filter current, ΔI is the current ripple of the output filter inductor, and N_p and N_s are the number of turns in the primary and secondary of the transformer, respectively.

Finally, ZVS is achieved for a load current so that $I_2 > I_{crit}$, which can be expressed as:

$$I_{load} \geq \frac{N_p}{N_s} \cdot I_{crit} - \frac{\Delta I}{2} + \frac{V_{out}}{L_{lk} + L_f} \cdot (1-D) \cdot \frac{T}{2} \tag{5.6}$$

The magnetizing current can only be used to achieve ZVS when the load current reflected to the primary is lower than the magnetizing current (*i.e.:* at light loads). For such light loads the energy available to charge/discharge the output capacitances of the

switches Q2 and Q4 at times t_2 and t_6, respectively, is the energy stored in the leakage inductance plus the energy stored in the magnetizing inductance of the transformer. This is because the magnetizing current can not circulate through the secondary of the transformer during intervals t_1 to t_2 and t_5 to t_6, due to the low output inductor filter currents freewheeling through the rectifier. The use of the magnetizing current has been fully described in [G-9]. The primary leakage inductance and output capacitance of the devices are used to achieve ZVS, as has been described in Section 5.3.1. The transformer does not need to be designed to minimize its leakage inductance as would be necessary for a conventional PWM converter. However, the parasitic capacitances of the windings have an adverse effect. They need to be discharged at the same time that the output capacitances of the devices are discharged. This increases the total energy required to implement ZVS of the primary switches, as presented in Eqs. (5.1) and (5.3), resulting in a larger minimum critical current required to achieve ZVS. Therefore, the transformer design has to aim to reduce the winding parasitic capacitance.

5.3.3 DC Voltage Conversion Ratio.

ZVS is achieved over a greater load range if a larger L_{lk} is used. However, the finite slopes in the rising and falling edges of the primary current cause the effective duty cycle available in the transformer secondary to reduce; therefore there is a reduction of the converter voltage gain. Consequently, the converter gain is dependent on the leakage inductance, the frequency of operation, and the load.

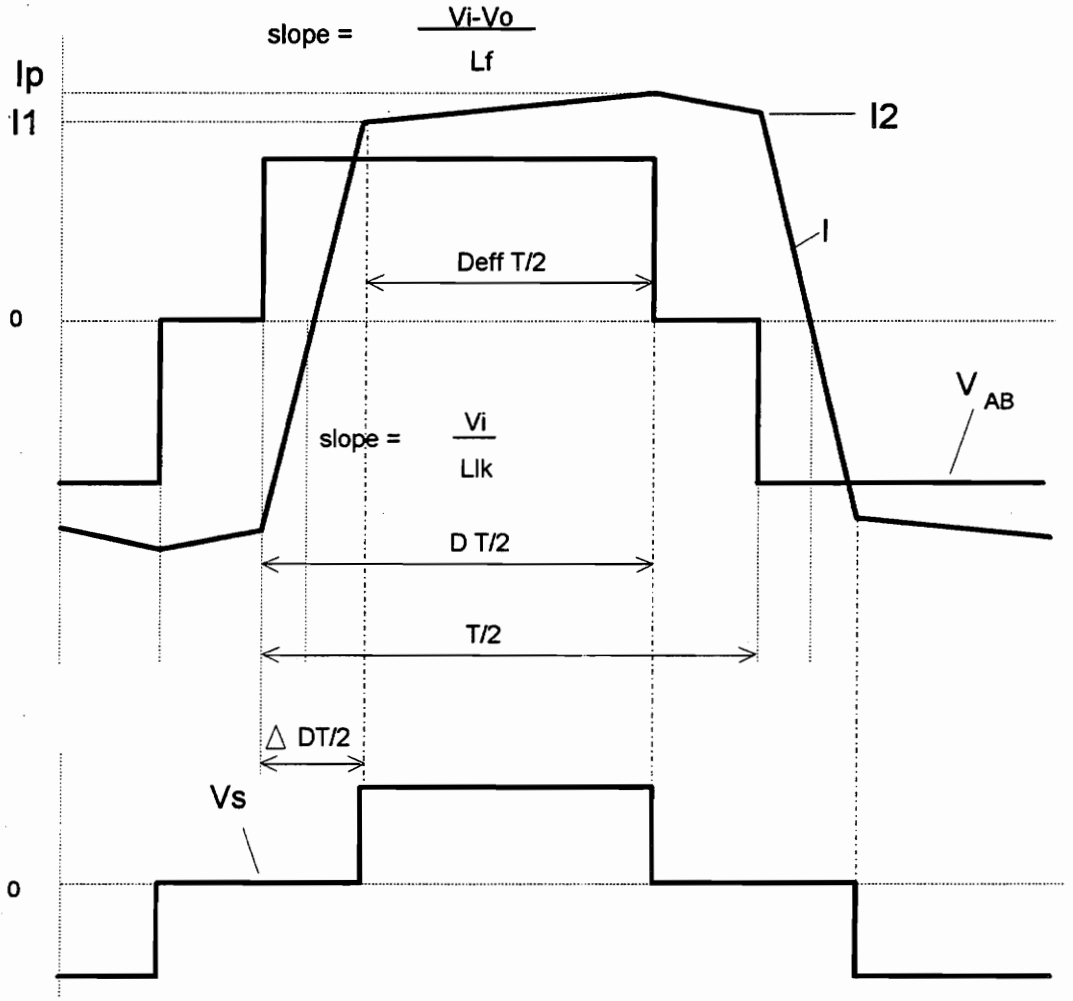


Figure 5.6: Primary and secondary voltage and current waveforms.

Figure 5.6 shows transformer primary current waveform with the expressions for the different slopes during each switching time interval.

The voltage gain of the ZVS-PWM converter can be expressed as:

$$\frac{V_{out}}{V_{in}} = \frac{N_s}{N_p} \cdot D_{eff} , \tag{5.7}$$

where N_p and N_s are the number of turns in the primary and secondary of the transformer, respectively, and D_{eff} is the duty cycle of the secondary voltage.

The primary duty cycle can be expressed as:

$$D = D_{eff} + \Delta D , \tag{5.8}$$

where ΔD is the loss of duty cycle due to the finite slope of the rising and falling edges of the primary current. Using the variables defined in Fig. 5.4, ΔD can be expressed as:

$$\Delta D = \frac{I_1 + I_2}{\frac{V_{in}}{L_{lk}} \cdot \frac{T}{2}} \tag{5.9}$$

and

$$\Delta D = \frac{\frac{N_s}{N_p}}{\frac{V_{in}}{L_{lk}} \cdot \frac{T}{2}} \cdot \left(2 \cdot I_{load} - \frac{V_{out}}{L_f} \cdot (1-D) \cdot \frac{T}{2} \right) . \tag{5.10}$$

Putting Eq. (5.10) into (5.8) and using Eq. (5.7), the following expression is obtained:

$$D = \frac{1 + \frac{4 \cdot L_{lk} \cdot f_s}{R'} - \frac{L_{lk}}{L'_f}}{\frac{1}{D_{eff}} - \frac{L_{lk}}{L'_f}}, \tag{5.11}$$

where $R' = R_{load} (N_p / N_s)^2$ and $L'_f = L_f (N_p / N_s)^2$ are the load resistance and the filter inductor reflected to the primary, respectively.

When the term containing (1 - D) in Eq. (5.10) is small compared to 2 I_{load}, Eq. (5.11) can be simplified to:

$$D = D_{eff} \cdot \left(1 + 4 \cdot \frac{L_{lk}}{R'} \cdot f_s\right). \tag{5.12}$$

For a given output power, input/output voltage ratio, and maximum duty cycle, the transformer turns ratio, switching frequency, and leakage inductance have to be chosen to satisfy

$$1 \geq D_{max} \geq \frac{N_p}{N_s} \cdot \frac{V_{out}}{V_{in}} \cdot \left(1 + 4 \cdot \frac{L_{lk}}{R'} \cdot f_s\right). \tag{5.13}$$

Figure 5.7 shows the voltage gain D_{eff} for several loads, and the following converter characteristics:

- transformer turns ratio $N_p/N_s=1$
- switching frequency 100 kHz
- $L_{lk}=52$ µH
- Full load resistance $R'= 64.8\ \Omega$ ($P_{out}= 2$ kW, $V_{out}= 360$ V)

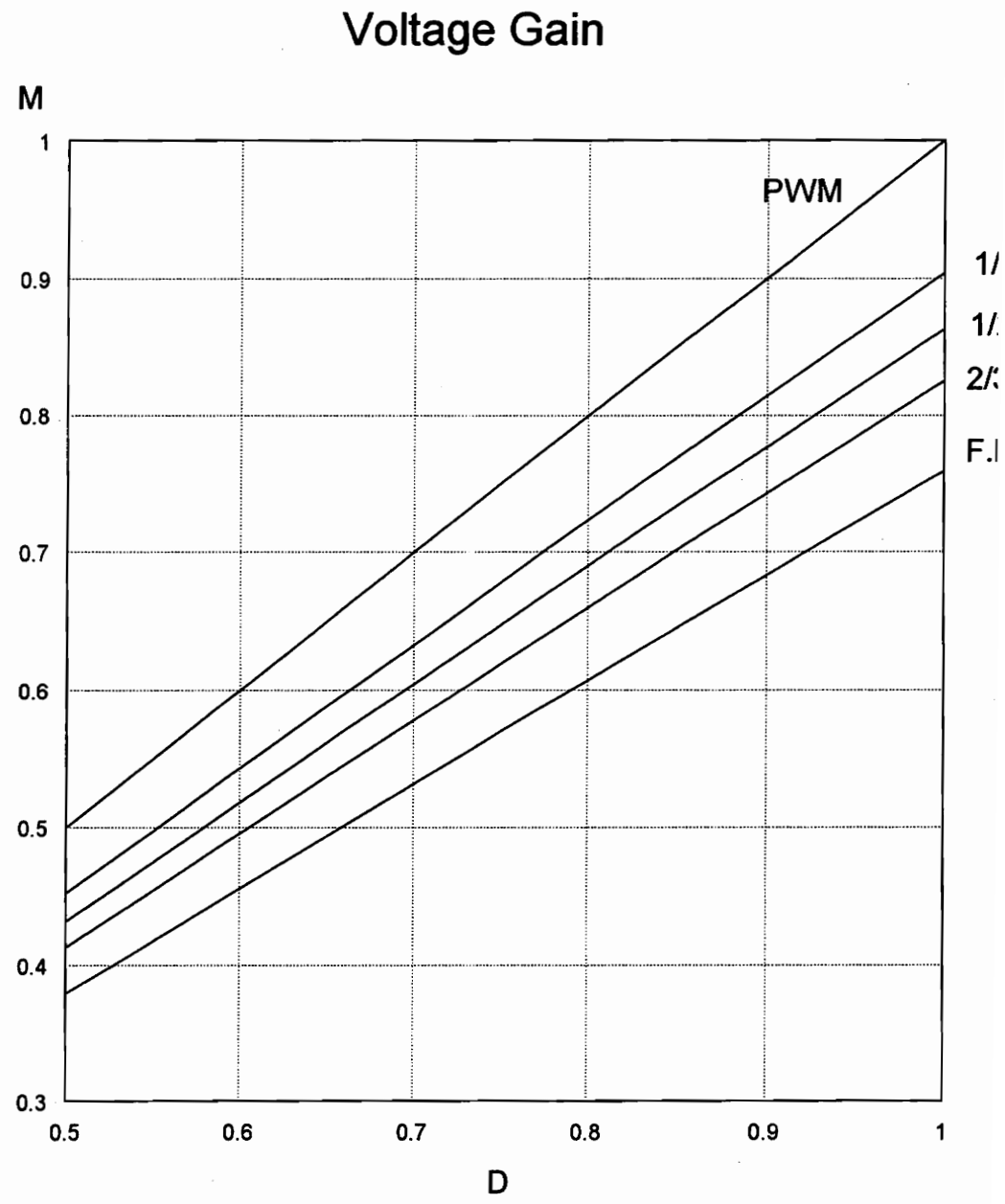


Figure 5.7: ZVS-FB-PWM Voltage gain for several load conditions.

5.4 Active Clamp for the Rectifier Stage

5.4.1 Transitions on the Rectifier Stage

The ringing across the output rectifier is the result of resonant oscillation among the leakage inductance of the transformer, the windings capacitance, and the rectifier diodes' capacitances. This ringing appears across the rectifier when the voltage in the transformer secondary rises. When the voltage is applied to the secondary, one of the rectifier diodes is reverse biased, and the leakage of the transformer rings with the diode's capacitance and transformer winding capacitances. For Shottky diodes, the peak voltage of the oscillation would be two times the voltage across the secondary, because they behave as an ideal capacitor when reverse biased. However, for pn-junction diodes, the reverse recovery current significantly increases the peak voltage.

The ringing has to be snubbed, but the use of an RC snubber in parallel with the rectifier would introduce large losses. The ringing frequency is:

$$f_{mg} = \frac{1}{2 \cdot \pi \cdot \frac{N_p}{N_s} \cdot \sqrt{L_{lk} \cdot C}} \tag{5.14}$$

Due to the large values of L_{lk}, the ringing frequency is usually less than 10 times the switching frequency. This makes the use of an RC snubber in the secondary impractical [G-24]. The problem is particularly severe in high-voltage, high-power applications, where the reverse recovery time of the rectifiers is excessive because Shottky diodes cannot be used.

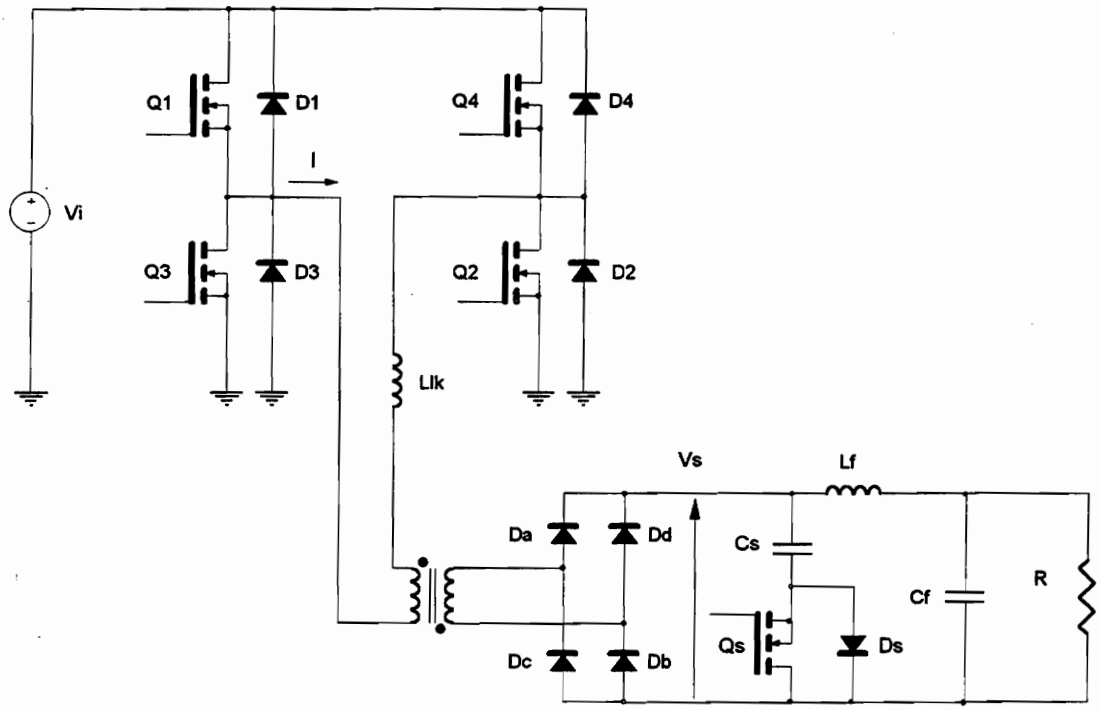


Figure 5.8: ZVS-FB-PWM converter with the secondary clamp.

Several solutions to this problem have been suggested. The simplest one [G-11] is to use a passive clamp circuit across the rectifiers. The clamp circuit limits the peak voltage in the secondary, but does nothing to damp or prevent the ringing. The excessive ringing causes EMI and control problems. The power dissipation of the clamp circuit also makes it impractical for use in high-voltage, high-power applications above several hundred volts and several kilowatts.

Another method is to use a low-leakage power transformer with a separate inductor in the primary, and to clamp the voltage in the primary circuit [G-16]. This approach has two drawbacks. One is the requirement for an extra inductor, which increases the size and reduces the efficiency of the converter. The other is the high-frequency ringing between the parasitic capacitance of the rectifiers and the leakage inductance, which requires the use of a dissipative snubber in the secondary.

The use of the active clamp circuit presented in this section completely eliminates voltage overshoot and ringing in a nondissipative manner. These attributes make the active clamp particularly useful in high voltage, high-power applications.

5.4.2 Circuit Operation

The proposed converter is shown in Fig. 5.8. When the secondary voltage is high, the active snubber (Q_S, D_S, C_S) connects a large capacitor in parallel with the rectifiers. The resonant frequency of the clamp capacitor and leakage inductance has to be small compared to the switching frequency, *i.e.* $2\pi \cdot \sqrt{n^2 \cdot L_{lk} \cdot C_S} >> T_S$, where T_S, is the

switching period. Consequently, the rectifier voltage is clamped to the steady state value of the clamp capacitor, and there is no overshoot in the secondary.

In steady-state operation, the average current through the clamp capacitor is zero. The energy from the leakage inductance of the transformer charges the snubber capacitor through the clamp diode. The capacitor returns energy to the output through the MOSFET.

The bridge is operated with phase-shift control in the same manner as in the conventional ZVS-FB-PWM converter [G-24]. Figure 5.9 shows the typical waveforms for the converter with the clamp circuit, the current through the clamp capacitor, and the driver signal for the clamp MOSFET. The converter operation for a half cycle is described as follows:

t_1 to t_2: In the primary, Q4 and D1 are conducting. In the secondary Dc and Dd are conducting. The primary current follows the output filter current.

t_2^-: Switch Q4 turns off, and the current through the primary of the transformer charges the output capacitance of Q4 and discharges the output capacitance of Q2, turning on diode D2.

t_2: Diode D2 starts conducting, Q2 can be turned on with virtually no voltage applied (only the forward drop of the parallel diode).

t_2 to t_3: The primary current circulates through diodes D1 and D2. The secondary of the transformer is shorted by diodes Da to Dd.

t_3 to t_4 The primary current circulates through Q1 and Q2. The secondary of the transformer is shorted.

t_4: The primary current reaches the reflected filter inductor current.

t_4 to t_5: The voltage in the secondary of the transformer starts increasing, and the leakage inductance of the transformer starts resonating with the diodes' capacitance.

t_5: The secondary voltage, V_S, reaches the clamp capacitor, and the clamp diode starts conducting. The secondary is clamped to the capacitor voltage.

t_5 to t_6: The current through the clamp capacitor decreases until it reverses sign at t_6. At this time the clamp's MOSFET has to already be turned on.

t_6: The clamp current naturally commutates from D_S to Q_S. For this reason D_S does not need to be a fast diode, and the body diode of Q_S is used.

t_6 to t_7: The current flows through the MOSFET Q_S until Q_1 is turned off. The clamp's MOSFET has to be turned off when the secondary voltage starts decreasing.

t_7: When the voltage in the secondary starts decreasing, the primary current is smaller than the reflected filter inductor current. Therefore, the output filter inductor current starts free-wheeling through the rectifier. The secondary is shorted.

The current in the leakage inductance charges the output capacitance of Q_1 and discharges the capacitance of Q_3; and diode D_3 is subsequently turned on.

t_7 to t_8: The primary current remains constant (assuming that the switches have zero resistance and the diodes have zero voltage drop). The secondary is still shorted.

t_8: The primary current reaches the reflected output filter inductor current. Rectifier diodes D_c and D_d stop conducting.

The most important changes in the converter operation due to the introduction of the clamp are:

- There is no ringing in the secondary voltage, reducing the voltage stress in the rectifiers, and eliminating snubber losses.
- The transformer secondary current is the sum of the output filter inductor current and the current trough the clamp capacitor.
- The peak primary current is reduced because the current through the snubber capacitor is negative when the output filter inductor current reaches its peak.
- ZVS for Q_1 and Q_3 is achieved in exactly the same manner as for Q_2 and Q_4. The output filter inductor does not intervene in the process.

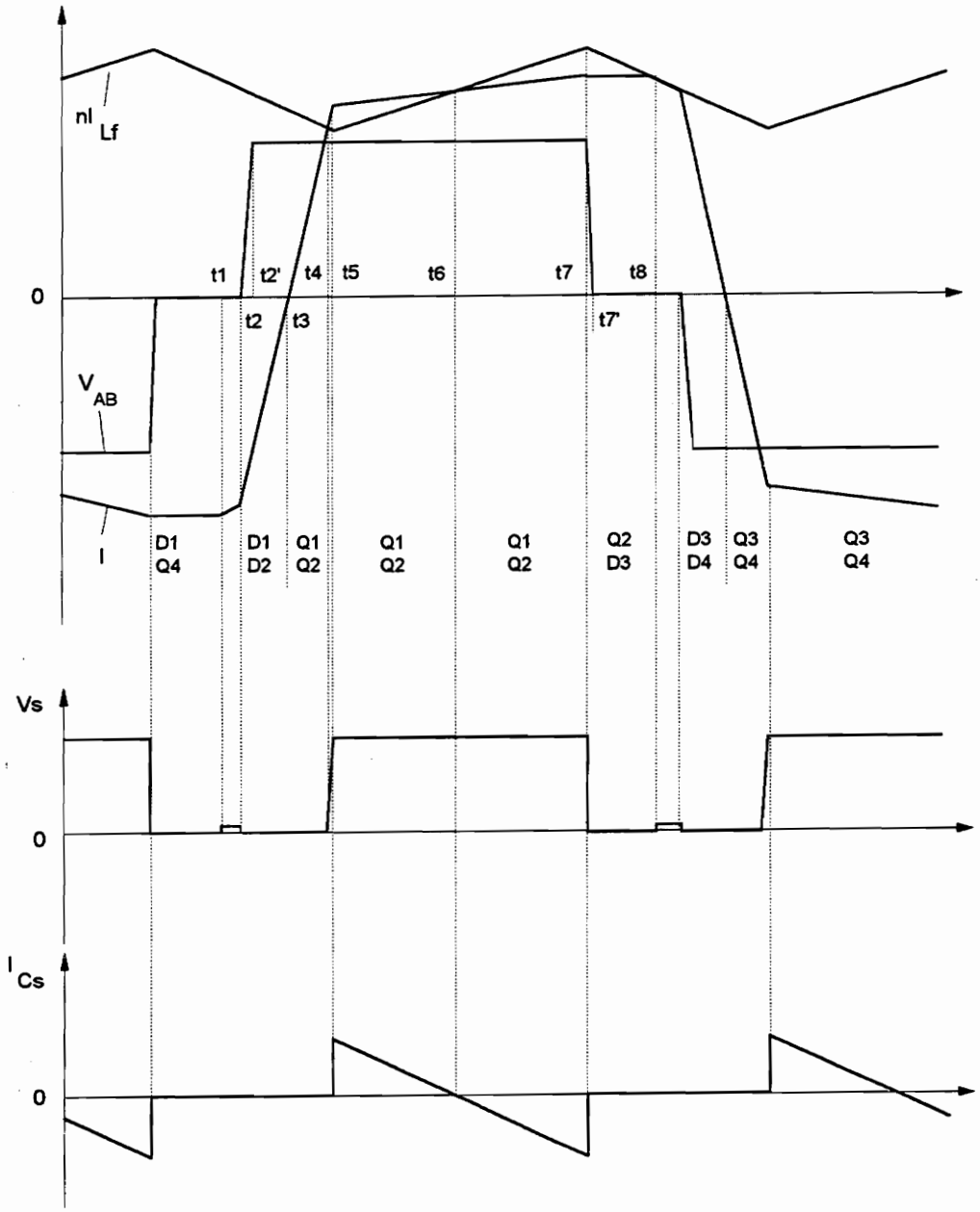


Figure 5.9: Typical waveforms for the ZVS-FB-PWM converter with the secondary clamp.

5.4.3 Active Clamp Analysis and Characteristics

Assuming that the clamp capacitor is chosen sufficiently large, the voltage in the secondary is a square wave with a peak value equal to the voltage across the clamp capacitor. Consequently, the output voltage, V_{out}, is determined by the duty cycle of the secondary voltage , V_{cs}, by:

$$V_{out} = D_{eff} \cdot V_{cs}. \tag{5.15}$$

The analysis of the ZVS-FB-PWM presented in section 5.3.3 shows how to calculate the primary duty cycle, D, knowing the circuit parameters. That part of the analysis is also valid for this circuit. The goal of the analysis presented here is to determine the snubber capacitor voltage.

During the interval t_5 to t_7, the slope of the transformer secondary current, S_{ls}, is determined by:

$$S_{ls} = \frac{n \cdot V_{in} - V_{cs}}{n^2 \cdot L_{lk}} \tag{5.16}$$

where V_{in} is the input voltage, n is the transformer turns ratio ($n = N_s/N_p$), V_{cs} is the steady-state voltage of the clamp capacitor, and L_{lk} is the leakage inductance of the transformer. The current through the snubber capacitor is the difference between the secondary current and the filter inductor current. The slope of the snubber capacitor current is:

$$S_{lcs} = \frac{n \cdot V_{in} - V_{cs}}{n^2 \cdot L_{lk}} - \frac{V_{cs} - V_{out}}{L_f} \tag{5.17}$$

where V_{out} is the output voltage, and L_f is the value of the output filter inductor.

The difference between transformer secondary current and the filter inductor current at time t_5 corresponds to the resonance between L_{lk} and the rectifiers' capacitance when the voltage reaches V_{cs}, plus the reverse recovery current through the rectifiers that are turned off. Assuming that the rectifiers' capacitance is constant, this current difference, Δi_{sec}, can be calculated as [G-24]:

$$\Delta i_{sec} = \frac{V_{in} \cdot n}{\sqrt{\frac{L_{lk}}{C_{sec}}}} \cdot \cos\left[\sin^{-1}\left(\frac{V_{cs} - n \cdot V_{in}}{n \cdot V_{in}}\right)\right] + 2 \cdot |i_{rr}| \tag{5.18}$$

where C_{sec} is the sum of rectifiers' and transformer winding capacitances, and i_{rr} is the peak reverse current through one rectifier diode due to reverse recovery.

Since the average current through the clamp capacitor is zero in steady state, the following implicit expression for the snubber capacitor voltage is obtained:

$$\left(\frac{V_{cs} - V_{out}}{L_f} + \frac{V_{cs} - n \cdot V_{in}}{n^2 \cdot L_{lk}}\right) \cdot \frac{V_{out} \cdot T_s}{4 \cdot V_{cs}} = \frac{V_{in} \cdot n}{\sqrt{\frac{L_{lk}}{C_{sec}}}} \cdot \cos\left[\sin^{-1}\left(\frac{V_{cs} - n \cdot V_{in}}{n \cdot V_{in}}\right)\right] + 2 \cdot |i_{rr}|, \tag{5.19}$$

where T_s is the switching period.

Using Eq.(5.7), Eq.(5.19) can be written as a function of the effective duty cycle:

$$\left[V_{cs}\left(\frac{1 - D_{eff}}{L_f} + \frac{1}{n^2 \cdot L_{lk}}\right) - \frac{V_{in}}{n \cdot L_{lk}}\right] \cdot \frac{D_{eff} \cdot T_s}{4} = \frac{n \cdot V_{in}}{\sqrt{\frac{L_{lk}}{C_{sec}}}} \cdot \cos\left[\sin^{-1}\left(\frac{V_{cs}}{n \cdot V_{in}} - 1\right)\right] + 2 \cdot |i_{rr}|. \tag{5.20}$$

To illustrate the variation of V_{cs} with respect to D_{eff}, V_{cs} is compared with the steady state secondary voltage in the ideal case, $C_{sec}=0$, $i_{rr}=0$. In this ideal case, Eq. (5.20) gives:

$$V_{cs}^{o} = n \cdot V_{in} \cdot \frac{L_f}{L_f + (1 - D_{eff}) \cdot n^2 \cdot L_{lk}} \tag{5.21}$$

Figure 5.10 shows the ratio V_{cs}/V^{o}_{cs}, as a function of D_{eff} for different values of L_{lk}, and for the following circuit parameters:

- $|i_{rr}| = 0.6$ A
- $L_f = 300$ μH
- $C_{sec} = 130$ pF
- $n = 1$
- $V_{in} = 600$ V
- $T_s = 10$ μsec

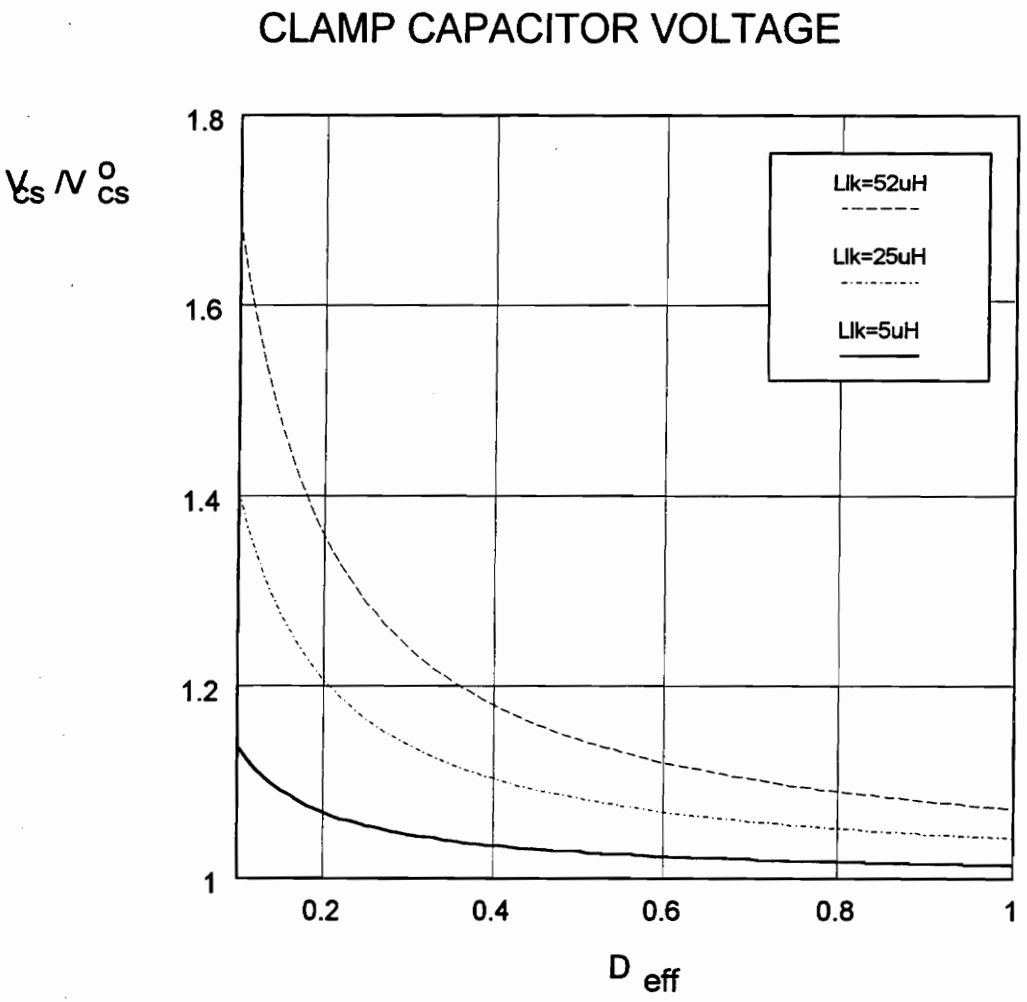


Figure 5.10: Ratio V_{cs}/V^{0}_{cs} vs. secondary duty cycle for L_{lk}=5 μH, 25 μH, and 50 μH.

The graph in Fig. 5.10 shows several things that influence the design of the converter with the snubber. First, the steady state secondary voltage with the snubber is always higher than the secondary voltage for the ideal case; the secondary voltage increases with an increase of L_{lk} and/or C_{sec}. Secondly, there is a sharp increase in V_{cs} as D_{eff} is small (less than 0.2). This operation should be avoided because of the increased voltage stress on the rectifier diodes.

Figure 5.10 is not shown for values of duty cycle smaller than 0.05 because these duty cycles correspond to a time shorter than the time required for the secondary voltage to rise (*i.e.* D_{eff}=0.05, or $D_{eff}T_r$=0.25 μsec). For these small duty cycles Eq.(5.20) is not valid. The rising time of the secondary voltage can be calculated from knowing the leakage inductance and the total capacitance in the secondary:

$$t_{rise} = \frac{\pi}{2} \cdot \sqrt{L_{lk} \cdot C_{sec}}, \tag{5.22}$$

where t_{rise} corresponds to the time required for the secondary to reach $n \cdot V_{in}$.

5.5 Design Trade-offs

As has been shown in the previous chapter, this converter cannot maintain ZVS from full load to no load. The selection of the ZVS range as part of the design requires considering the trade-offs involved in the choice. This chapter addresses the trade-offs involved in the selection of switching frequency and leakage inductance. The experimental results obtained in two prototypes are presented and used to verify the analysis and the design procedure.

The zero-voltage switching range of the ZVS-FB-PWM can be arbitrarily extended by increasing the value of the primary inductance, adding an external inductor if necessary. However, larger values of primary inductance result in a larger loss of duty cycle as shown in Eq. (5.10). Consequently, for a larger ZVS range the conduction losses in the primary will increase, not only because of longer transition times for the current, but also because a lower transformer turns ratio would have to be selected (Eq. 5.7).

The addition of the active clamp to the converter influences the choices for the ZVS range. The current through the clamp capacitor depends on the leakage inductance value, and the reverse recovery current of the rectifier's diodes. Consequently, the selection of the inductance in series with the transformer affects the clamp current in two ways:

- The peak current through the clamp depends on the characteristic impedance of the resonant circuit formed by the effective inductance in series with the transformer reflected to the secondary and the diodes' capacitance. Hence, the

clamp current due to the resonance increases when the inductance is reduced (Eq. (5.18)).

- Also the slope of the current is inversely proportional to the inductance in series with the transformer. The current slope determines the di/dt seen by the rectifier's diodes, and the reverse recovery current, i_{rr}, increases with the di/dt seen by the diodes.

As has been presented in Chapter 2, zero-voltage switching for resonant converters depends on the phase shift between the current and the voltage in the loaded resonant tank. The control action required to regulate the output voltage when the load changes can be to vary the frequency or the duty cycle applied to the resonant tank. Both control actions change the phase shift between the current and voltage in the tank. Consequently, for resonant converters load changes and the corresponding control action result in an abrupt loss of zero-voltage switching once the ZVS limit is passed. A good feature of the converter is that the loss of ZVS at partial loads is gradual. ZVS is lost because the energy in the primary inductance is not enough to discharge the output capacitance of the switches. Consequently, the voltage at which the switches are turned on increases from zero at the ZVS limit, up to the full input voltage, if the primary current is zero. However, the primary current minimum value is the magnetizing frequency. When the load current reflected to the primary is comparable to the magnetizing current, the energy in the magnetizing inductance is used to discharge the output capacitance of the devices.

The gradual loss of zero-voltage switching for the phase-shifted full-bridge PWM converter allows for practical designs with limited zero-voltage switching range. If the zero-voltage switching is lost at partial loads, since the conduction losses in the devices are already reduced and the switching losses increase gradually, the thermal dissipation limit is not exceeded.

Also, several trade-offs are involved in the selection of the switching frequency. ZVS allows operation at high frequencies without increased switching losses. However, for the same ZVS range, higher frequencies result in a larger loss of duty cycle. And since the ZVS range is always limited, an upper frequency limit exists for the case when ZVS loss cannot be tolerated, even at very light loads, because switching losses can exceed the thermal dissipation for the devices.

These trade-offs are explored in the following sections for specific design, with its hardware implementation of that design is presented in the last section of this chapter.

5.5.1 Analysis of Conduction Losses

The ZVS-FB-PWM converter provides ZVS for the devices, but it has larger rms currents in the primary than the conventional FB-PWM converter. It is of primary interest to quantify the conduction losses and to compare them with the conventional design.

The conduction losses due to the channel resistance of the switches can be calculated by

$$P_Q = R_{on} \cdot I_{rms}^2, \tag{5.23}$$

where R_{on} is the channel resistance of the switch, and I_{rms} is the rms current through the switch. The conduction losses for the switches are:

- Q2 or Q4

$$P_{Q_{2,4}} = R_{on} \cdot \left[\left(\frac{I_1}{\sqrt{3}} \right)^2 \cdot \frac{\Delta D}{2} + \left(I_{out}^2 + \frac{\Delta I_1^2}{3} \right) \cdot D_{eff} + \left(I_{cav}^2 + \frac{\Delta I_2^2}{3} \right) \cdot (1-D) \right] \quad (5.24)$$

- Q1 or Q3

$$P_{Q_{1,3}} = R_{on} \cdot \left[\left(\frac{I_1}{\sqrt{3}} \right)^2 \cdot \frac{\Delta D}{2} + \left(I_{out}^2 + \frac{\Delta I_1^2}{3} \right) \cdot D_{eff} \right], \quad (5.25)$$

where, using the variables defined in Fig. 5.6, $\Delta I_1 = \frac{I_p - I_1}{2}$, $\Delta I_2 = \frac{I_p - I_2}{2}$, $I_{cav} = \frac{I_p + I_2}{2}$, and $I_{out} = \frac{I_p + I_1}{2}$.

For a conventional PWM converter, $\Delta D \cong 0$, and there is no conduction during the interval $(1\text{-}D)\cdot T_2$. The conduction loss for each of the switches is:

$$P_{Q_{PWM}} = R_{on} \cdot \left(I_{out}^2 + \frac{\Delta I_1^2}{3} \right) \cdot D_{eff}, \quad (5.26)$$

where the variables used are defined in Fig. 5.6.

The conduction losses on the bridge diodes are:

$$P_D = V_{diode} \cdot I_{av}, \quad (5.27)$$

where V_{diode} is the forward voltage drop on the diodes, and I_{av} is the average current through the diodes. The conduction loss of the diodes can be written as:

• D2 or D4

$$P_{D_{2,4}} = \left(\frac{I_2}{2}\right) \cdot V_f \cdot \frac{\Delta D}{2} \tag{5.28}$$

• D1 or D3

$$P_{D_{1,3}} = V_f \cdot \left(I_{out} \cdot (1-D) + \frac{I_2}{2} \cdot \frac{\Delta D}{2}\right) \tag{5.29}$$

These losses are negligible for a conventional FB-PWM converter.

The conduction losses in the rectifier are the same for a conventional PWM and a ZVS-PWM:

• Rectifier

$$P_{rect} = 4 \cdot \left(\frac{I_{out}}{2}\right) \cdot V_f \tag{5.30}$$

assuming a FB rectifier is used.

From the loss expressions, it can be deduced that the ZVS-PWM converter has larger conduction losses than the conventional PWM bridge, particularly when using a small duty cycle and a large L_{lk} that imply a large (1 - D) and a large ΔD, respectively. The main advantage for the ZVS-PWM in terms of efficiency is the much-reduced switching losses and the elimination of the need for snubber circuits across the bridge switches. In the next chapter the bridge currents for the ZVS-PWM converter are compared to the currents in conventional PWM converters and resonant converters.

5.6 Design Procedure

5.6.1 Zero-Voltage Switching Range Selection

Once the capacitance of the switches in the bridge is known, the minimum ZVS range corresponds to the minimum leakage inductance possible for the transformer. Increasing the ZVS range results in larger currents in the primary. Consequently, in terms of conduction losses smaller ZVS ranges are desirable. However, a practical design requires other considerations:

- When ZVS is lost, large dv/dt is present in the voltage across the switches, resulting not only in switching losses, but also in noise generation that requires additional filtering at the input. Also the noise generated can cause problems by being coupled to other parts of the system through heatsink capacitance or radiation. The effect of the noise and its relative detrimental effects depend on the input voltage and power level of the converter, requiring a case by case design decision.

- The reverse recovery current and the voltage ringing across the rectifier depend on the value of the inductance in series with the transformer. Large inductances reduce the ringing frequency and the peak current associated with the ringing. While the reduction in peak current is desirable, the low frequency ringing is undesirable because it increases the losses in the snubbers used across the rectifiers. However, when using the active clamp described in the previous chapter, larger inductances reduce the current in the clamp, resulting in reduced

currents reflected to the primary and keeping the advantages of low di/dt values for the current waveforms.

Adjustment of the ZVS range can be achieved to a limited extend with the design of the transformer for the required leakage inductance. However, the optimization of the transformer does not leave flexibility in adjusting its leakage inductance. A large leakage inductance results in general in larger transformers or in poor efficiency. Consequently, the preferred way to adjust the ZVS range is with an external inductor in series with the transformer.

The selection of the inductance in series with the transformer is based on two main effects on the converter operation:

- The rms currents through the secondary clamp.
- The ZVS operation range.

At a given voltage level the value of the current through the clamp depends on the slope of the transformer current during the secondary voltage rise, the equivalent capacitance of the rectifier diodes, and the clamp voltage level. Expressions for the clamp voltage were presented in the analysis in the previous chapter. The clamp voltage depends on input voltage, secondary voltage duty cycle, D_{eff}, inductance in series with the transformer, output filter inductance, and the diodes' capacitance and reverse-recovery effect.

Since the effect of the inductance depends on the characteristics of the diodes, the optimal selection of inductance requires testing with the actual hardware components to be used. To illustrate the effect of the inductance value on the clamp current and the converter waveforms, several values of inductance were tested in prototype with the following characteristics:

- Input voltage 325 V to 400 V
- Output voltage 360 V
- Transformer turns ratio $N_p/N_s = 0.75$
- Transformer leakage inductance $L_{lk} = 0.8\ \mu H$
- Output power 8 kW

The complete circuit diagram with the values for the is shown in Fig. 5.12.

Figure 5.11 shows primary current and voltage, rectifier voltage, and clamp current for three possible external inductors:

- $L_{ext} = 0$, $L_{tot} = L_{lk} + L_{ext} = 0.8\ \mu H$
- $L_{ext} = 3.8\ \mu H$, $L_{tot} = L_{lk} + L_{ext} = 4.6\ \mu H$
- $L_{ext} = 1.5\ \mu H$, $L_{tot} = L_{lk} + L_{ext} = 2.3\ \mu H$

Without an external inductor, the current through the clamp is excessively large. This not only increases the losses in the clamp switch but also modifies notably the primary current. On the other hand, the improvement by more than doubling the external inductor ($L_{ext} = 3.8\ \mu H$) is small, and since the ac current through this inductor is very

large, the smallest possible value of inductance is desired. The inductor selected was L_{ext} = 1.5 μH.

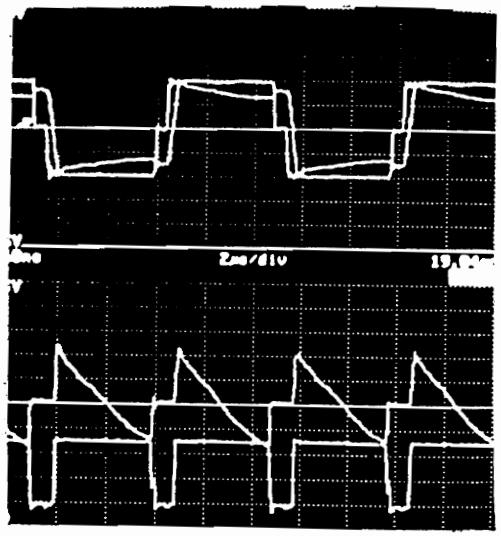
With the selected value of external inductance, the loss of duty cycle during the current change of sign in the primary is:

- at high line (400 V) ΔD = **0.07**
- at low line (320 V) D = **0.08**

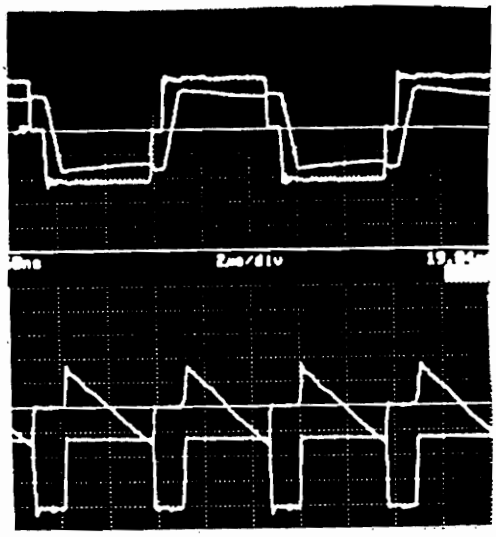
With the selected external inductor the load level at which ZVS begins to be partially lost was calculated to be 35% of the full rated load for the high-line case. The complete circuit used for this test is presented in section 5.7.2.

No ext. inductor

L_{ext}= 3.8 μH



L_{ext}= 1.5 μH



Scales: Voltage: 50 V/div.
Primary Current: 5 A/div.
Clamp Current: 1 A/div.
Time: 2 μsec/div.

Figure 5.11: External Inductor Testing Results: In each picture, top waveforms are primary current and voltage, and bottom waveforms are the clamp current and the voltage across the rectifier.

5.6.2 Clamp Design Considerations

The active clamp circuit eliminates the ringing on the voltage across the rectifiers. The voltage across the rectifiers is kept almost constant during the time the secondary voltage is high. To achieve this, the clamp capacitor has to be large enough to allow a very small voltage change when the excess energy in L_{lk} is discharged in it. It was found experimentally that good results were obtained for a resonant frequency of L_{lk} and the clamp capacitor three times smaller than the switching frequency. Hence, the clamp capacitor value can be calculated from

$$C_c = \frac{1}{L_{lk} \cdot n^2} \cdot \left(\frac{5}{4 \cdot \pi \cdot f_s} \right)^2 . \tag{5.31}$$

5.6.3 Design Procedure

The equations presented in the analysis and the design trade-offs presented in this chapter are used to design the ZVS-FB-PWM converter. The interdependence of the several choices requires an iterative procedure that is outlined in this section.

Specifications needed to start the design are V_{in}, V_{out}, P_{out}, and maximum current ripple allowed at the output filter, Δi_{out} .The design procedure can be performed in the following steps.

1. Choose D_{max}. D_{max} should be chosen as large as possible to maximize N_p/N_s and subsequently reduce the conduction losses in the primary (Eqs. 5.23-5.25). D_{max} is, however, limited by the duty cycle range allowed by the PWM controller.

2. Choose V_{sec}. V_{sec} should be chosen as low as possible to reduce the voltage stress of the rectifiers, and to maximize N_p/N_s. However, reducing V_{sec}, *i.e.* increasing N_p/N_s, reduces the primary current and consequently increases the value of L_{lk} required to achieve a desired ZVS range. For this reason the initial choice of V_{sec} is somewhat arbitrary, and the final value is obtained after several iterations o steps 2-5.

   V_{sec} has to satisfy:

$$V_{sec} \geq \frac{V_{out}}{D_{max}} \tag{5.32}$$

   and

$$\frac{N_p}{N_s} = \frac{V_{in}}{V_{sec}} . \tag{5.33}$$

   The initial choice of V_{sec} should be somewhat higher than V_{out}/D_{max}. Once V_{sec} is chosen, it is straightforward to calculate N_p/N_s, D_{eff} from Eq. (5.7) and ΔD from Eq. (5.10).

3. Choose the ZVS range, *i.e.* the load current, $I_{min,ZVS}$, at which ZVS is lost. To achieve the desired ZVS range, an inductance in series with the transformer has to be selected. However, since the loss of duty cycle is already fixed, the leakage inductance can not be chosen independently of the frequency.

   The ZVS range depends on the current available at the switching of Q2 and Q4. This current can be determined knowing the current ripple, and the loss of duty cycle at the load for which ZVS is lost. However, since the leakage inductance, output filter

inductance, and switching frequency are still not determined, an iteration process of steps 3-5 is required to determine the final values.

To start the iteration $I_2=I_{min,ZVS}$ is assumed, and after going through steps 4 and 5 I_2 is recalculated from Eq. 5.5. The process is repeated until changes in I_2 are negligible.

4. Calculate L_{lk} from Eq. 5.4 as,

$$L_{lk} = \frac{2}{I_2^2}\left(\frac{4}{3}\cdot C_{mos}\cdot V_{in}^2 + \frac{1}{2}\cdot C_{tr}\cdot V_{in}^2\right) \tag{5.34}$$

To perform this calculation, it is necessary to choose the devices for the bridge, and estimate the parasitic capacitance of the transformer. In order to make the selection, an estimate of the rms current trough the primary of the transformer and the bridge can be obtained from the following normalized equation

$$I_{prim}=\left(\frac{P_{out}}{V_{out}}\right)\cdot\frac{Q+\frac{2}{\pi}\cdot f_n}{D\cdot Q}\cdot\sqrt{1-\frac{2}{3}\cdot D\left(1-\frac{Q}{Q+\frac{2}{\pi}\cdot f_n}\right)}\,. \tag{5.35}$$

Assuming

$$\frac{N_p}{N_s} = \frac{V_{in}^{min}}{V_{out}}\cdot D_{eff}^{min} \tag{5.36}$$

and using Eq. 5.12, the effective duty cycle can be expressed as

$$D_{eff} = \frac{D}{1+\frac{2}{\pi}\cdot\frac{f_n}{Q}} \tag{5.37}$$

with Q defined as

$$Q = \frac{n^2 \cdot R_{out}}{Z_o}, \tag{5.38}$$

where $Z_o = \sqrt{L_{lk}/C_{eq}}$ is obtained from the leakage inductance and the equivalent capacitance seen from the primary, defined as

$$C_{eq} = \frac{8}{3} \cdot C_{mos} + C_{tr}. \tag{5.39}$$

The definition of Q is linked to the ZVS condition expressed in Eq. 5.6. After normalizing and some manipulation it can be rewritten as

$$D_{eff} \geq Q. \tag{5.40}$$

The normalized switching frequency, f_n, is defined as

$$f_n = f_{sw} \cdot \left(2\pi \cdot \sqrt{L_{lk} \cdot C_{eq}}\right). \tag{5.41}$$

The value of f_n can be estimated from the time that the voltage transition across the switches takes. The transition time should be short compared to the switching period, and consequently the value of f_n is in general smaller than 0.1. This value for f_n does not significantly affect the primary current.

Figure 5.12 shows the values of $I_p \cdot (V_{in}/P_{out})$ for f_n=0.1 and different values of Q. Knowing the ZVS range, the effective duty cycle, and the converter input-output specs., the current through the switches and the transformer primary can be estimated, and used to select the switches and allow a transformer design to calculate the capacitance that affects the ZVS.

5. Calculate the switching frequency from Eq. 5.4 by

$$f_{sw} = \frac{n^2 \cdot R_{load}}{4 \cdot L_{lk}} \cdot \left(\frac{D_{max}}{D_{eff}} - 1 \right). \tag{5.42}$$

The filter inductance can be calculated from

$$L_f = D_{eff} \cdot \frac{V_{in} - V_{out}}{\Delta i} \cdot \frac{1}{2 \cdot f_s}. \tag{5.43}$$

The duty cycle at the ZVS limit can be calculated using Eq. 5.11, and the new value of I_2 is determined from

$$I_2 = I_{zvs,min} + \frac{\Delta i}{2} - \frac{V_{out}}{L_{lk} + L_f} \cdot (1 - D_{ZVS}) \cdot \frac{1}{2 \cdot f_{sw}}, \tag{5.44}$$

and return to step 3 to recalculate.

After completing these steps, the initial design is obtained. This design, however, may not be satisfactory from the point of view of circuit realization. The following cases may occur:

- Switching frequency too low (high): In this case it is possible to go to step 4 and reduce (increase) the ZVS range or return to step 2 and increase (decrease) V_{sec} .

- L_{lk} too high (low): In this case it is possible to go to step 4 and reduce (increase) the ZVS range or to return to step 2 and increase (decrease) V_{sec} .

5.6.4 Design Example

To illustrate the design procedure, a ZVS-FB-PWM converter is designed with the following specifications:

- input voltage, $V_{in} = 600$ V,
- output voltage, $V_{out} = 360$ V,
- output power, $P_{out} = 2000$ W ($I_{out} = 5.56$ A),
- current ripple $\Delta i_{out} = 2.3$ A.

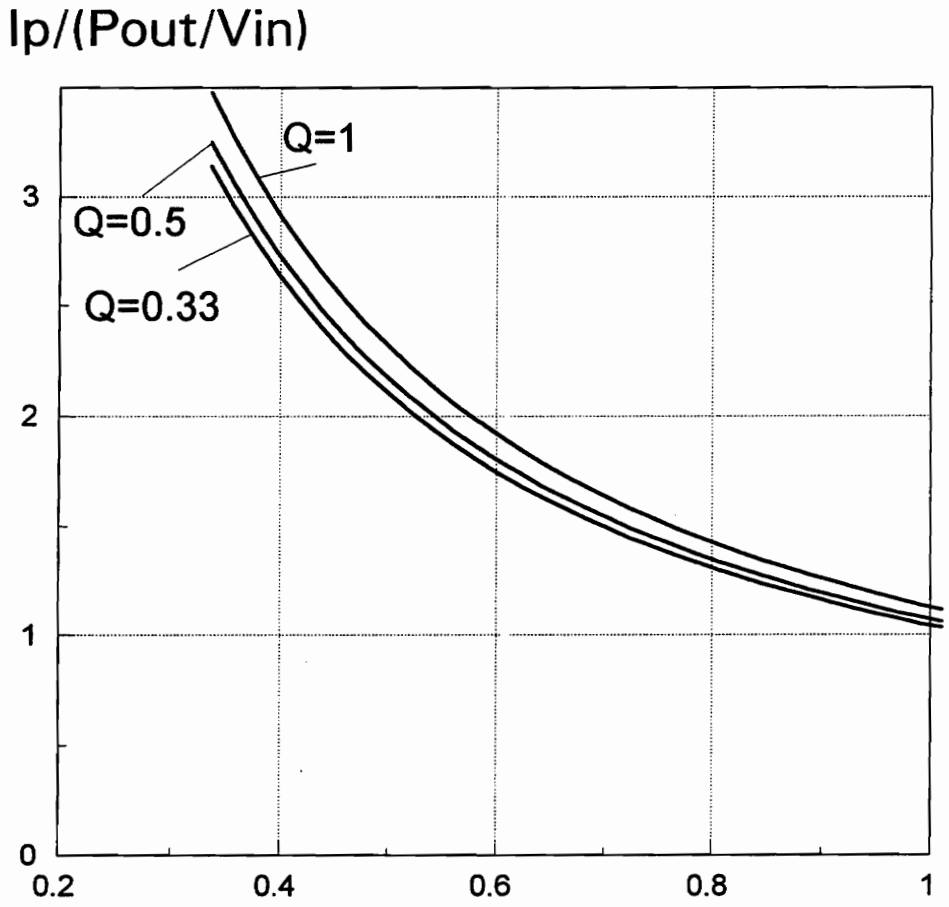


Figure 5.12: Current through the transformer primary normalized with respect to $I_p \cdot (V_{in}/P_{out})$ for different values of Q vs. duty cycle.

Using the design procedure, the following were chosen:

1. The maximum duty cycle was selected to be $D_{max} = 0.8$,

2. The maximum secondary voltage was selected to be V_{sec} = 600 V, hence the transformer turns ratio is n = 1,

3. The ZVS range is chosen to be from full-load to 50% load; this implies a minimum load current for ZVS of 2.78 A. Consequently, the initial value for I_2 is 2.78 A.

4. To determine the switches' and the transformer capacitances the current is estimated based in Fig. 5.12. The switches selected IRFPE50 have C_{mos} = 82 pF. The transformer with n = 1 and the current determined is assumed to have C_{tr} = 100 pF. Hence, the inductance required calculated with Eq. 5.34 is L_{lk} = 14.8 μH.

5. Using Eqs. 5.42 to 5.44, the following values were obtained,

$$f_{sw} = 368.5 \text{ kHz}, L_f = 105 \text{ μH, and } D_{ZVS} = 0.67.$$

These values give a value of I_2 = 2.1 A. Recalculating from step 3 with the values obtained, f_{sw} = 212 kHz, Llk = 26 μH.

After going through the design steps several more times, the following results were obtained:

$$Llk = 52 \text{ μH}, f_{sw} = 95 \text{ kHz}, L_f = 314 \text{ μH, and } D_{ZVS} = 0.79.$$

This converter was built and the results are presented in the next section.

5.7 Experimental Results

5.7.1 Circuit Without External Inductance

The circuit designed in section 5.6.4 was constructed using a transformer with a core EE-55/55/21 of H7C4 material from TDK, and $N_p = N_s = 26$ turns. The transformer was built with a proper winding arrangement to have a leakage inductance of Llk = 52 μ H.

To clamp the ringing across the rectifier stage, the active clamp proposed in section 5.4 was implemented. Also a conventional dissipative clamp was implemented for comparison purposes. Figures 5.13 and 5.14 show the circuits with the dissipative clamp, and the active clamp, respectively.

Figure 5.15 shows the current and voltage in the primary (top waveforms) and the voltage across the secondary rectifier for the dissipative clamp implementation at full load. The absence of ringing in the voltage waveform shows the ZVS operation. The ringing in the primary current is related to the secondary voltage ringing. The secondary voltage ringing is clamped to 850 V. The ringing is clamped for the first two cycles. The damping in the ringing path is very small. The ringing frequency (3.2 MHz) is low compared to the switching frequency. If an RC snubber was used, the snubber losses would be very high.

When the load current is decreased below 2.7 A, ZVS is lost, as wanted. Figure 5.16 shows the waveforms for a load current of 2.1 A. The waveforms correspond to the predictions of the analysis. The voltage in the primary increases sinusoidally until L_{lk} has been fully discharged, then the switch is turned on with 200 V between the drain and source.

The waveforms of the circuit using the active clamp are shown in Fig. 5.17 compared with the ones with a dissipative clamp. The ringing is completely eliminated.

Figure 5.18 shows the converter waveforms at a power level of 1 kW. The current through the clamp capacitor has not changed significantly. This supports the assumptions made to derive the clamp capacitor value. The slope of the current when reverse voltage is applied to the diodes is limited by the leakage inductance. Consequently the reverse recovery current, i_{rr} is relatively small and does not vary significantly with the load.

Figure 5.19 shows the measured values of the clamp capacitor voltage as a function of D_{eff}, compared with the analysis prediction. The rectifier parameters used in the calculation are: diodes' capacitance C_{sec} = 130 pF, and reverse recovery current $|i_{rr}|$ = 0.6 A.

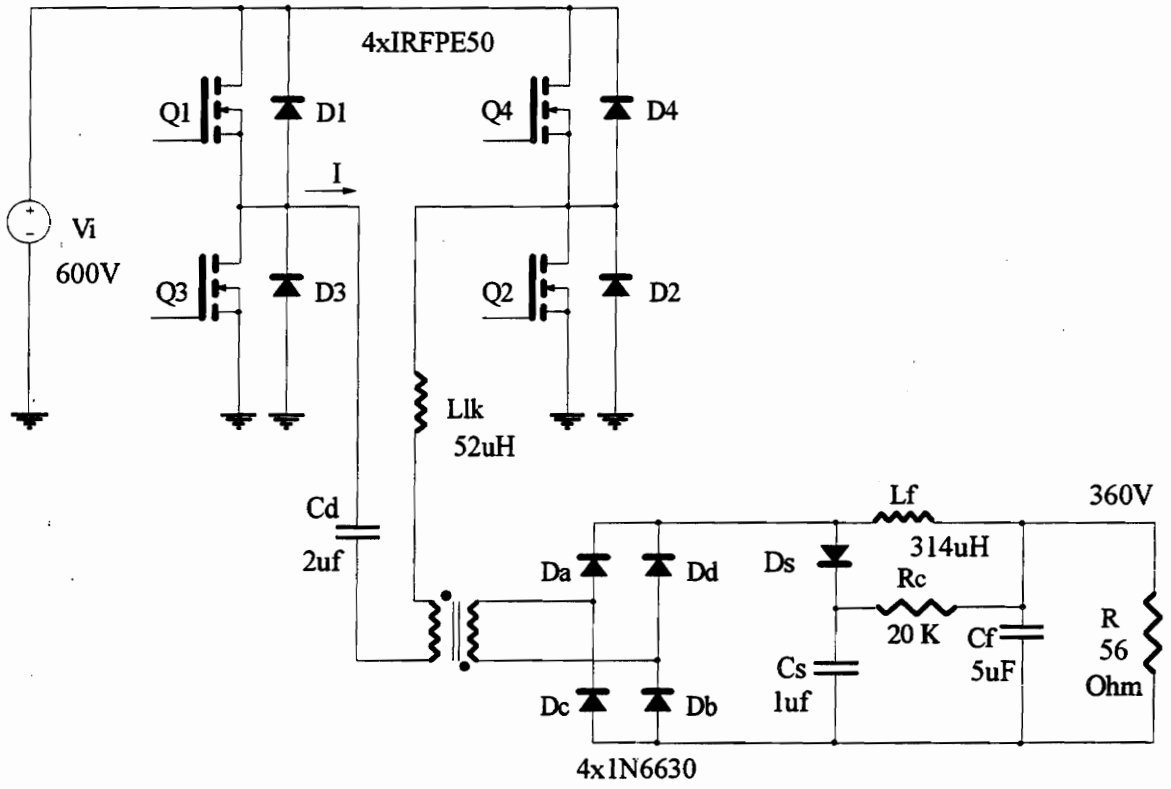


Figure 5.13: 2 kW ZVS-FB-PWM converter with a dissipative clamp.

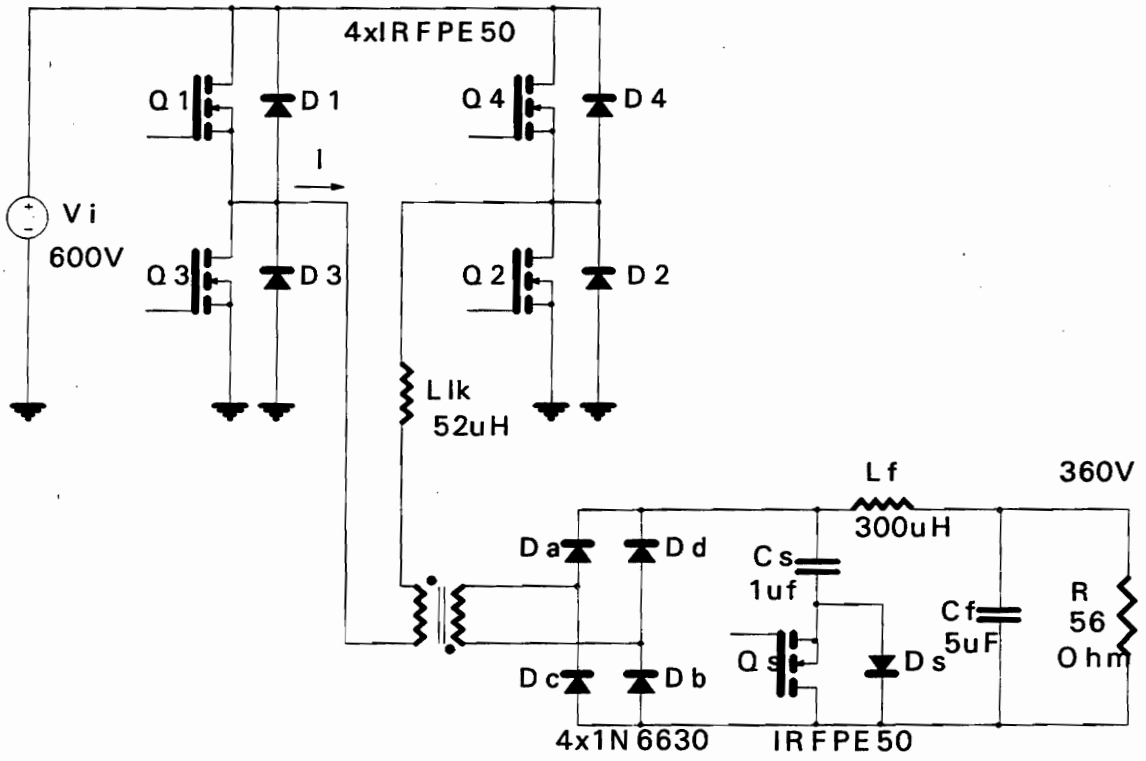


Figure 5.14: 2 kW ZVS-FB-PWM converter with the active clamp.

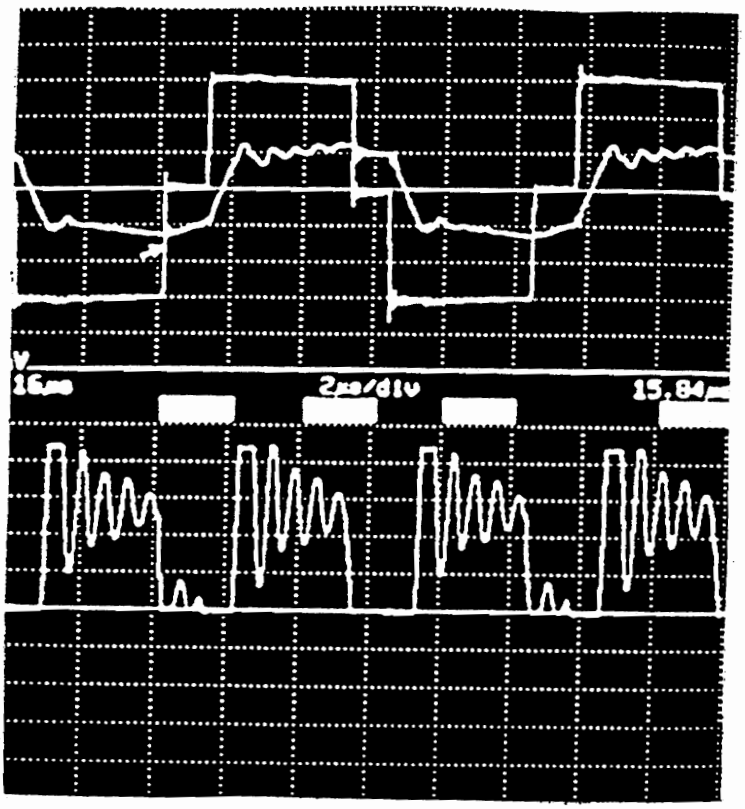
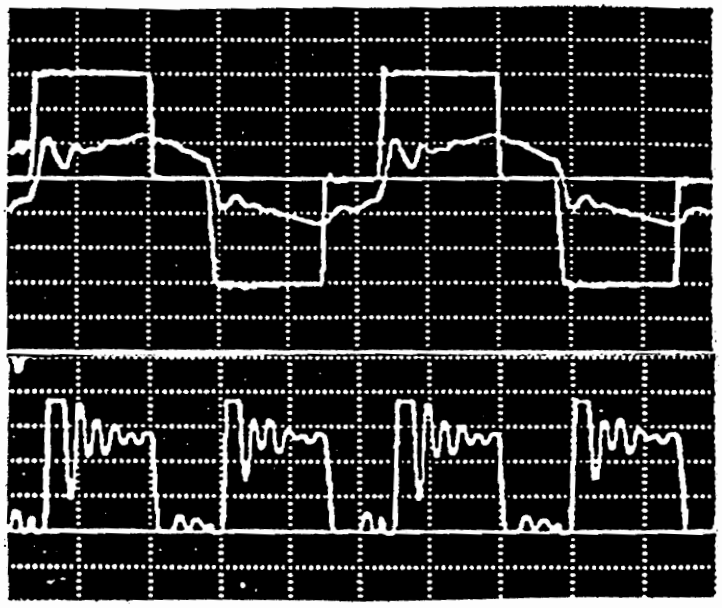


Figure 5.15: Waveforms at 2 kW with a dissipative clamp.

a)



b)

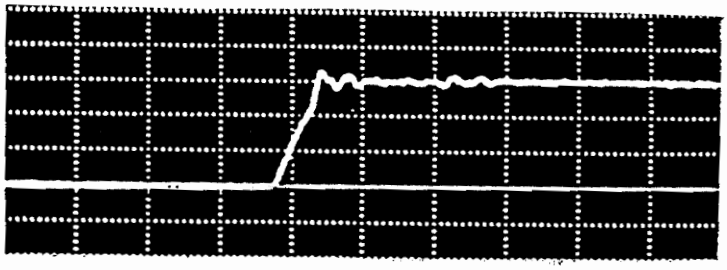


Figure 5.16: **a) Voltage and current in the primary (top waveforms) and voltage across the rectifier (lower waveform) for 2.1 A load current, b) detail of the rising edge (no-ZVS). (Scales: Voltage: 200 V/div., current: 2 A/div., time: 2 μsec/div.).**

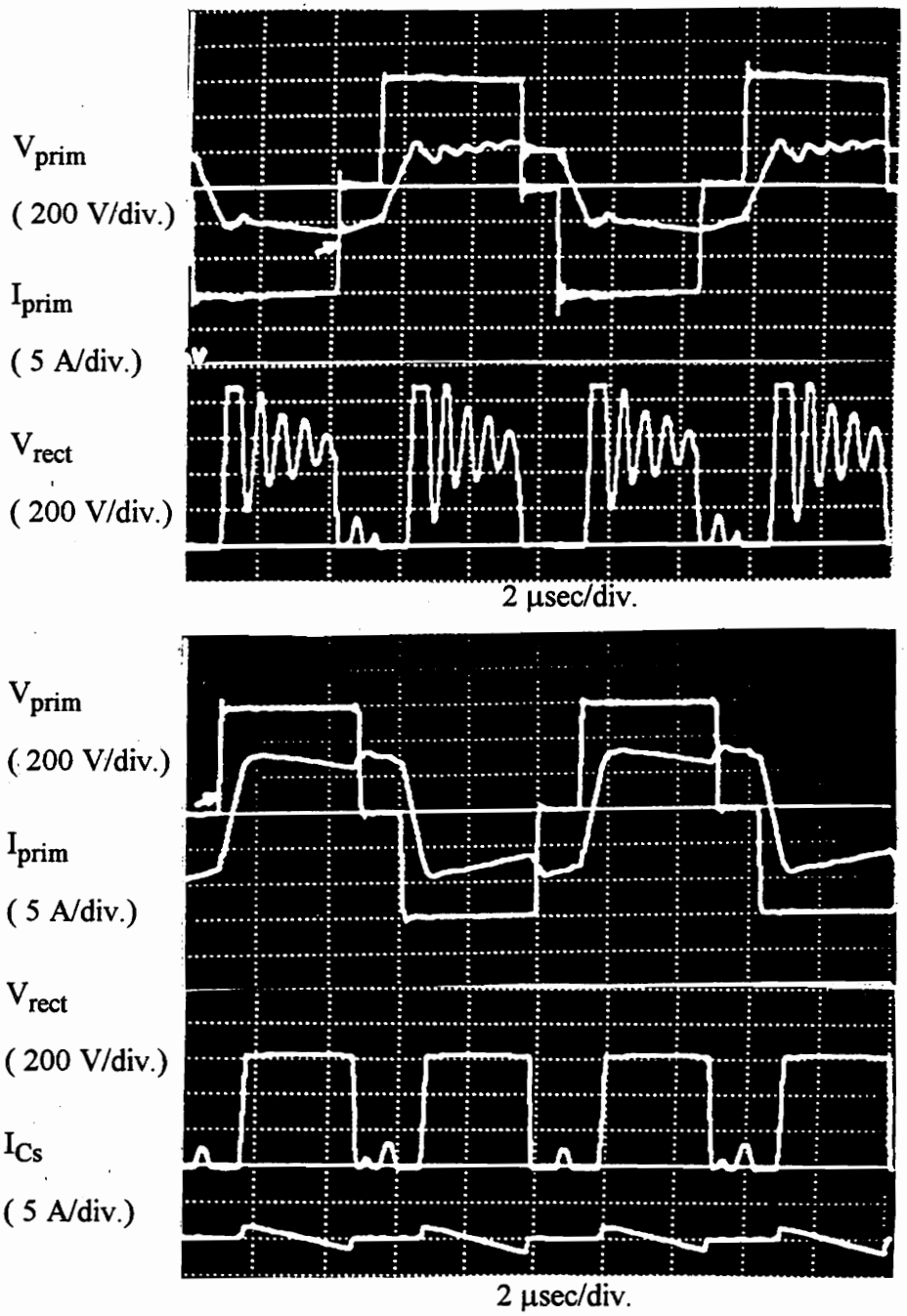


Figure 5.17: Waveforms at 2 kW with an active clamp (bottom), and with a dissipative clamp (top).

5.7.2 Circuit with External Inductance

Another circuit was constructed to verify the generality of the analysis and the clamp performance for a higher power converter. Also the circuit design required additional design considerations to achieve thermal stability for the transformer.

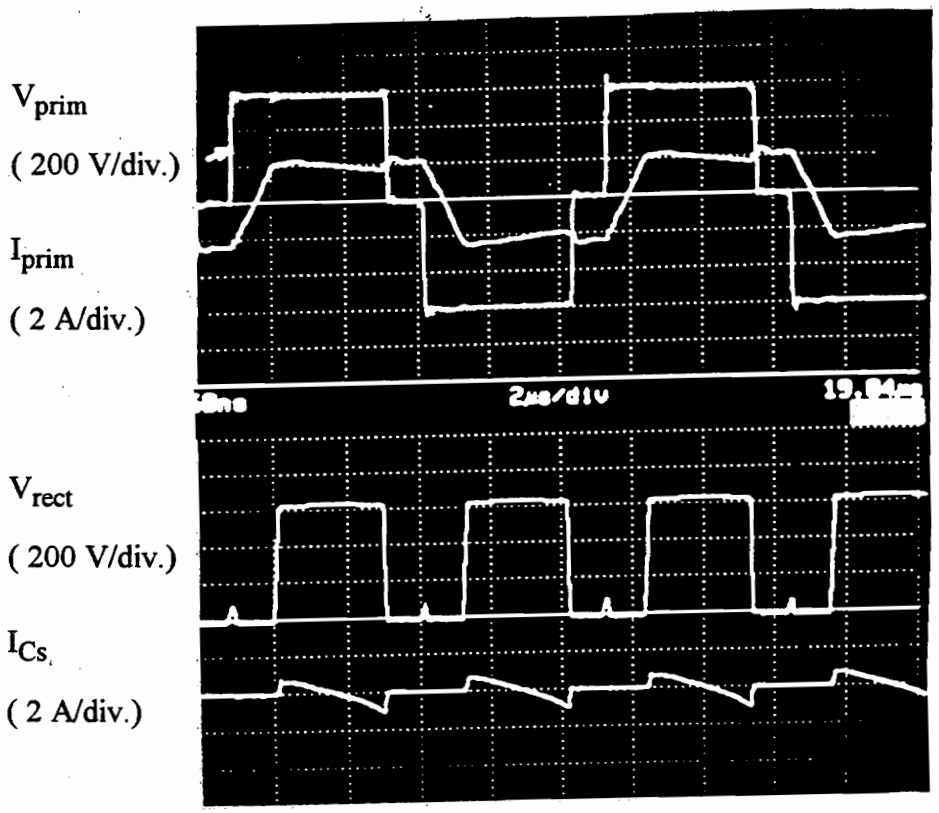
The specifications for the converter are:

- input voltage, V_{in} = 325 V to 400 V,
- output voltage, V_{out} = 360 V,
- output power, P_{out} = 8000 W (I_{out} = 22.22 A),
- current ripple Δi_{out} = ±4 A

Following the design procedure the converter parameters are:

- maximum duty cycle, D_{max} = 0.8 V,
- effective duty cycle, D_{Fe} = 0.6 V,
- secondary voltage with clamp, V_{sec} = 750 V,
- VS range from full load to 30 % load,
- leakage inductance required L_{lk} = 4 μH
- output filter inductance L_f = 90 μH

However, its implementation operation proved that the design of the transformer with the required leakage inductance was not practical and an external inductance was added to provide the required inductance for ZVS. The following summarizes the considerations for the transformer design.



2 μsec/div.

Figure 5.18: Waveforms at 1 kW with the active clamp.

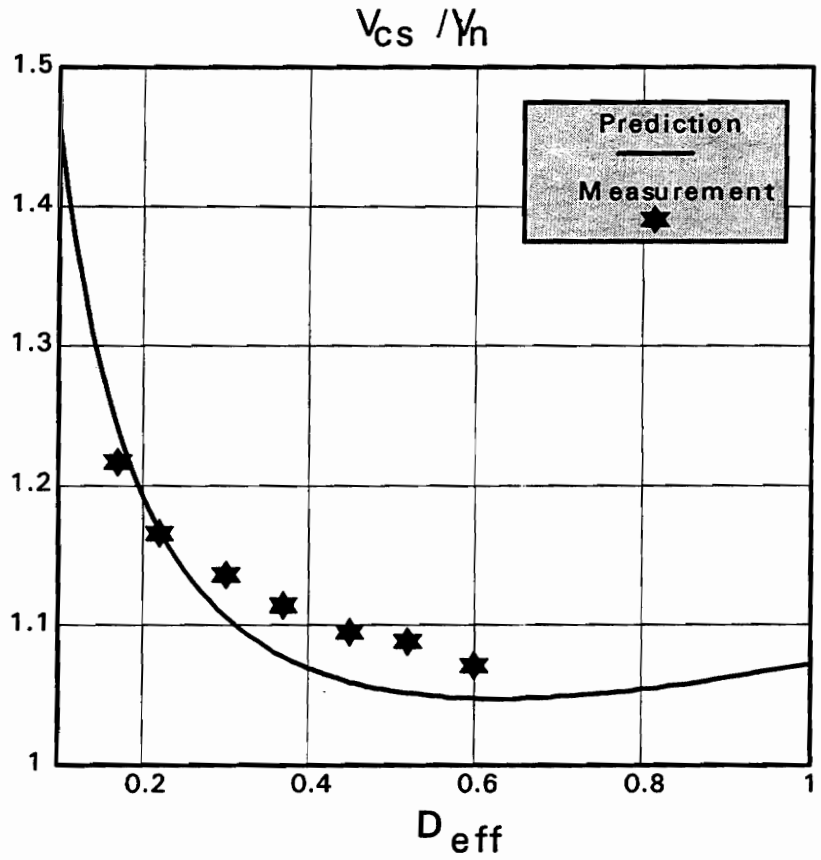


Figure 5.19: Comparison of calculated and measured active clamp voltage with respect to effective duty cycle.

Transformer design considerations

Large currents in the transformer generate large magnetic fields in the windings. These fields affect the current distribution in the windings and consequently, are a major factor in determining copper losses in the transformer. The field distribution and hence the eddy current losses in the windings depend heavily on the winding geometry. It was found that some specific arrangements of the windings reduce the peak magnetic fields, reducing dramatically the copper losses by allowing a better utilization of the available copper section of the windings.

The transformer design required experimental comparison of several alternatives to obtain a satisfactory solution. The required transformer turns ratio n = 1.8 is accomplished with $N_p = 9$ turns and $N_s = 16$ turns.

Figures 5.20 and 5.21 show the different winding distributions tested for the EC90 and EIC90 cores of PC40 material from TDK. The wire used for the windings is Litz wire 1100/40.

a) The first alternative tested (Fig. 5.20a) uses an EIC core with the following winding distribution:

   - secondary with 16 turns of Litz wire in three consecutive layers, and

   - primary 9 turns of two parallel wires in three consecutive layers. This transformer has a leakage inductance of 4 μH. However, the copper losses are too high. The steady-state winding temperature at 6 kW exceeds 100 °C.

b) The second alternative was tested using an EC90 core (Fig. 5.20b). The larger size of the core allowed single-layer primary and secondary windings. The leakage inductance was smaller than for the previous case, but was still acceptable for the converter.

This alternative does not modify appreciably the magnetic fields in the windings, but it provides more surface for the removal of the heat from the windings. Unfortunately, the heat removal by natural convection was not sufficient to decrease the temperature in the windings to safe levels.

c) A third alternative was tested using the EIC90 core with the same number of turns as the two former transformers, but alternating the layers of the primary and secondary windings (Fig. 5.21a). This transformer had a leakage inductance of 2 μH. This is too small for ZVS operation of the converter, and an external inductor was used to provide the additional inductance required. The copper losses were reduced approximately by a factor of two. However, the temperature in the hottest part of the windings was still too high for safe operation.

d) Finally a transformer using an EC90 core and interleaving was built using two layers of 16 turns in parallel for the secondary and two layers of nine turns each in parallel for the primary, and alternating primary and secondary layers (Fig. 5.21b). The transformer operates with a maximum temperature of 80 °C at full-load. The leakage inductance of the transformer is less than 1 μH, and consequently an external inductor of 3 μH is required for the desired ZVS range.

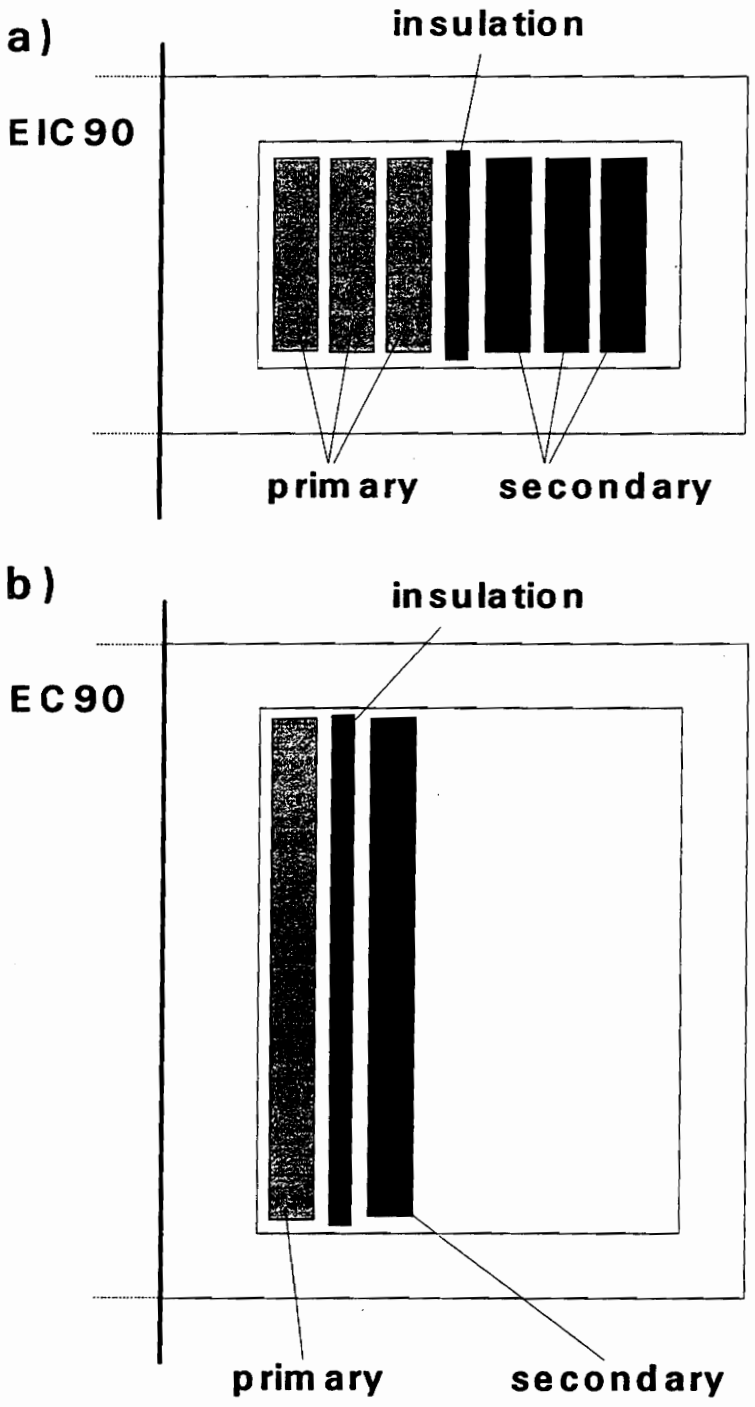


Figure 5.20: Transformer structure for cases a and b.

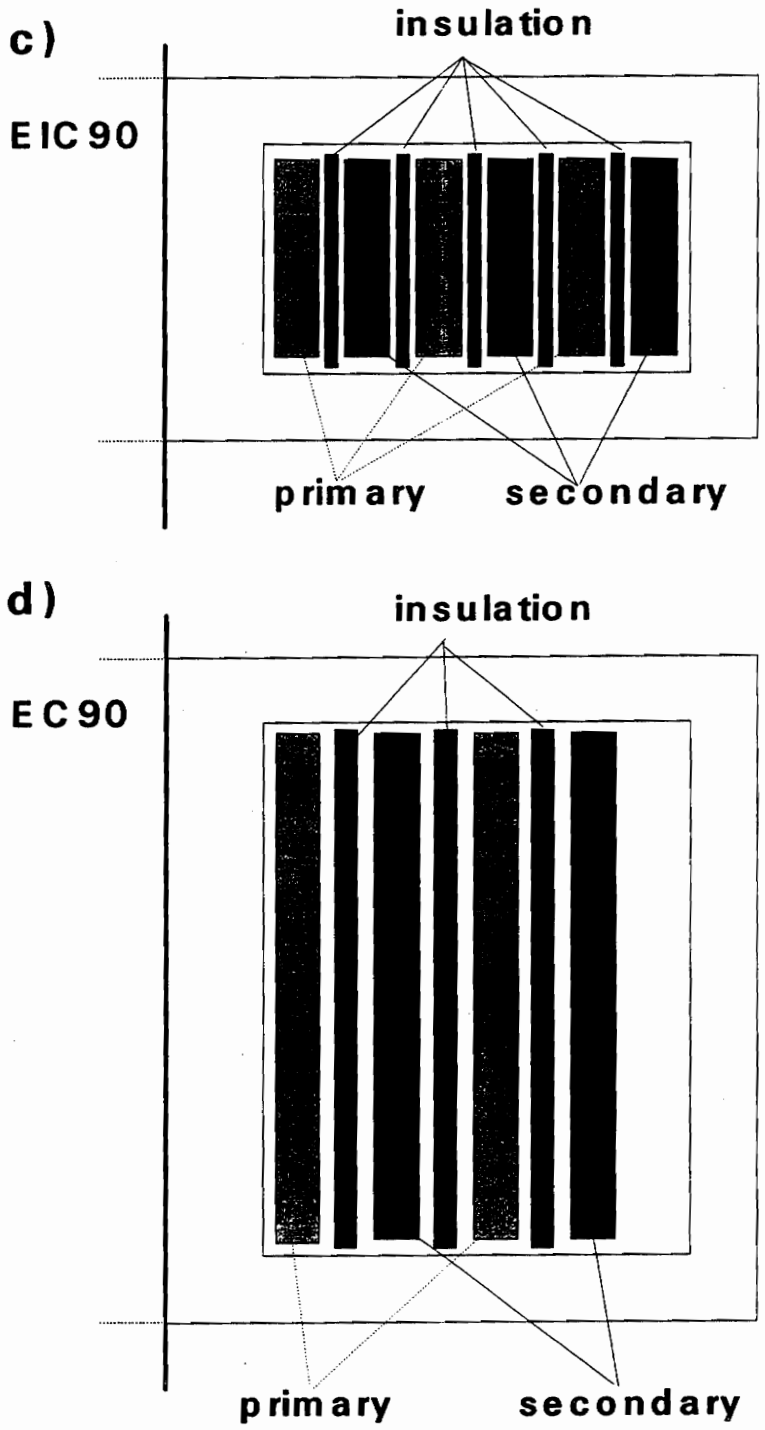


Figure 5.21: Transformer structure for cases c and d.

The interleaving significantly reduces the copper resistance because it reduces the peak magnetic field in the windings, reducing the proximity effect and providing a more even distribution of currents in the windings. However, the effective copper section used is much smaller than the real copper section. The copper section had to be selected to keep the copper losses at a reasonable level for thermal stability.

Figure 5.22 shows the converter schematic with the parts selected for the converter. The waveforms show good agreement with the expected results from the analysis of the circuit with the active clamp. Figure 5.23 shows the converter waveforms at full load. The voltage across the secondary shows absolutely no ringing. The negative slope of the primary current shows that the secondary voltage is clamped at the voltage of C_{clamp}, higher than $n \cdot V_{in}$. In this case the voltage was selected to be 750 V.

Figure 5.24 shows the waveforms for 2 kW output power. The ZVS is lost, but there is no ringing across the primary voltage, and all the waveforms are very clean. The current trough the clamp has only decreased to a peak value of 5 A compared to 7 A at full load. This verifies the validity of the analysis using the reverse recovery current for the diodes at full load, which is the worst case, with minimum error for design purposes.

Figure 5.25 shows the waveforms for 1 kW output power when discontinuous current in the output filter is reached. No deterioration in the performance is observed at this power level.

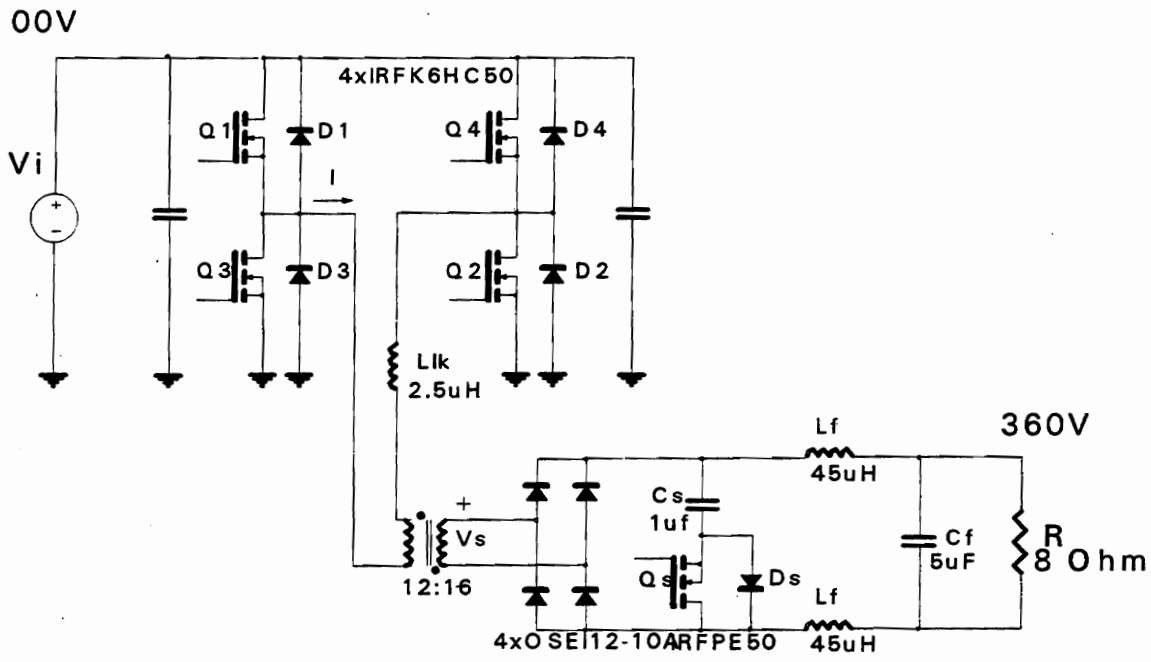
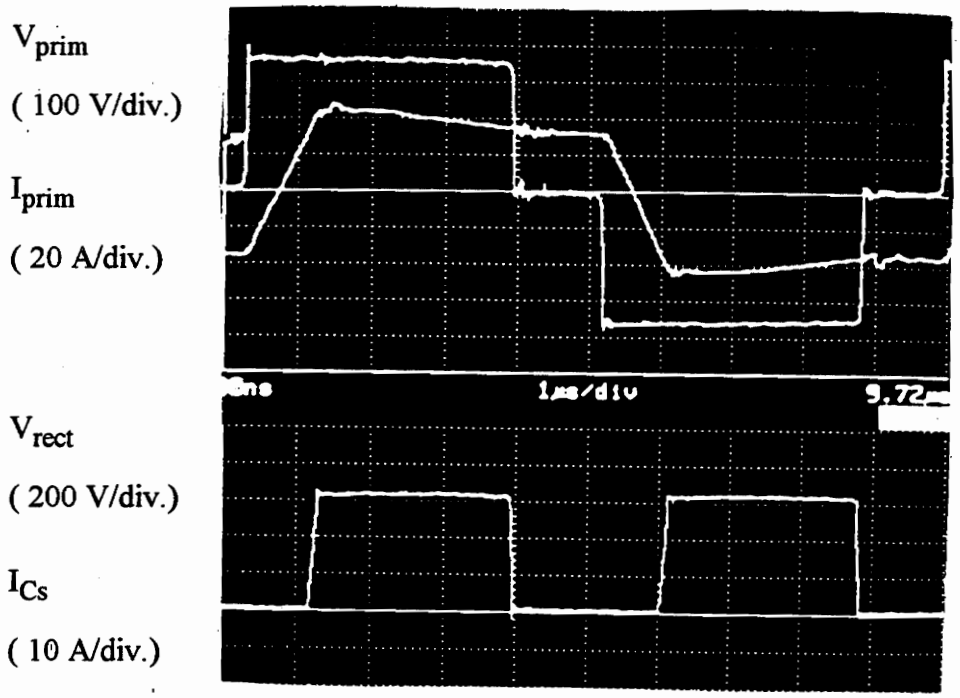


Figure 5.22: 8 kW converter schematic with an active clamp.



1 μsec/div.

Figure 5.23: Waveforms at 8 kW with an active clamp.

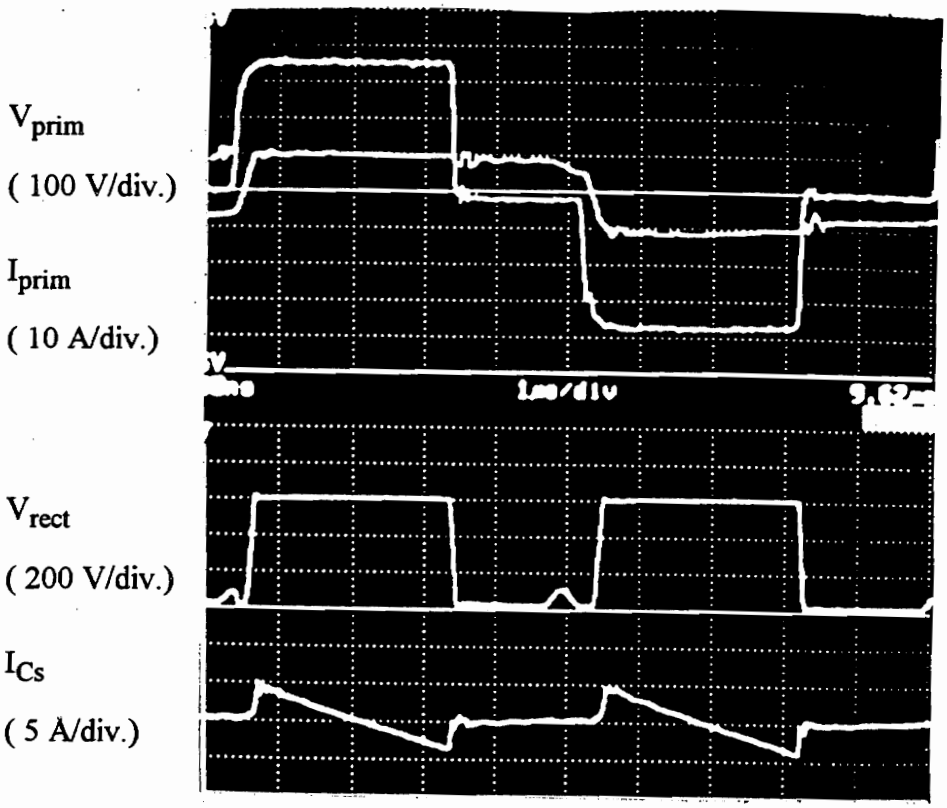


Figure 5.24: Waveforms at 2 kW with an active clamp.

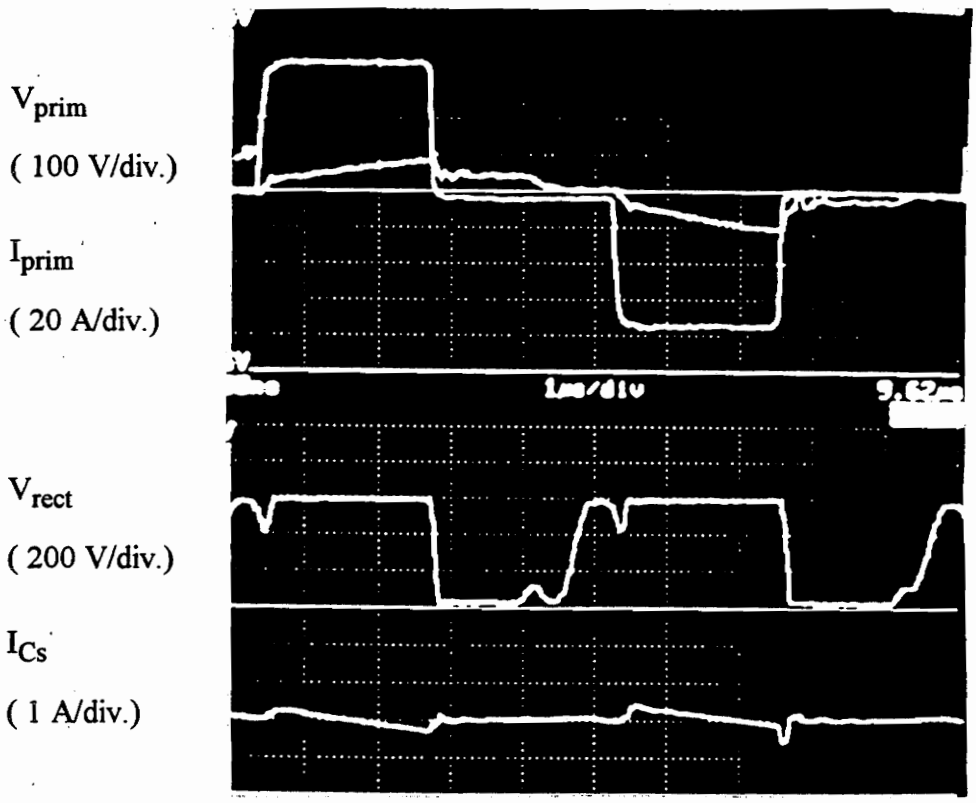


Figure 5.25: Waveforms at 1 kW with active clamp, in discontinuous operation mode.

Efficiency measurements

Figure 5.26 shows the measurements of efficiency *vs.* load. The efficiency remains almost constant until after the ZVS is lost and the switching losses start to increase. The increase of switching losses is followed by a further drop in efficiency due to the low output power.

Table 5.1 presents the loss breakdown at full load and at 25% load (after losing ZVS). The conduction losses on the bridge switches, rectifier diodes, and clamp switch were calculated using the rms values of the measured waveforms. The transformer core losses were calculated, and the copper losses estimated from the temperature increase measured. The output filter inductor losses were calculated: the core losses were calculated using the design parameters and the copper losses were found using the ac and dc resistances measured from the inductor used. The difference between the measured losses and analysis is assumed to be due to the switching losses in the bridge devices.

The switching losses at full load are practically zero, because of the ZVS operation. The switches are turned on with zero voltage, consequently, with no turn-on losses. The fast turn-off of the switches together with a large value of output capacitance minimizes the current-voltage overlap during turn-off. The switching losses are negligible until ZVS is lost. The operation without ZVS does not cause any problem, because when the ZVS is lost, the total power loss in the bridge devices is much lower than at full load.

The main losses are due to the channel resistance of the MOSFETs and the conduction losses in the rectifier. The transformer losses are kept low by the design because the transformer is cooled only by natural convection.

The clamp losses are smaller than for the dissipative clamp used in the 2 kW version. However, the impact of these losses in the converter efficiency is minimal because of their small relative value in both cases. The main achievement in using the active clamp circuit is to completely eliminate any ringing in the secondary without any extra losses.

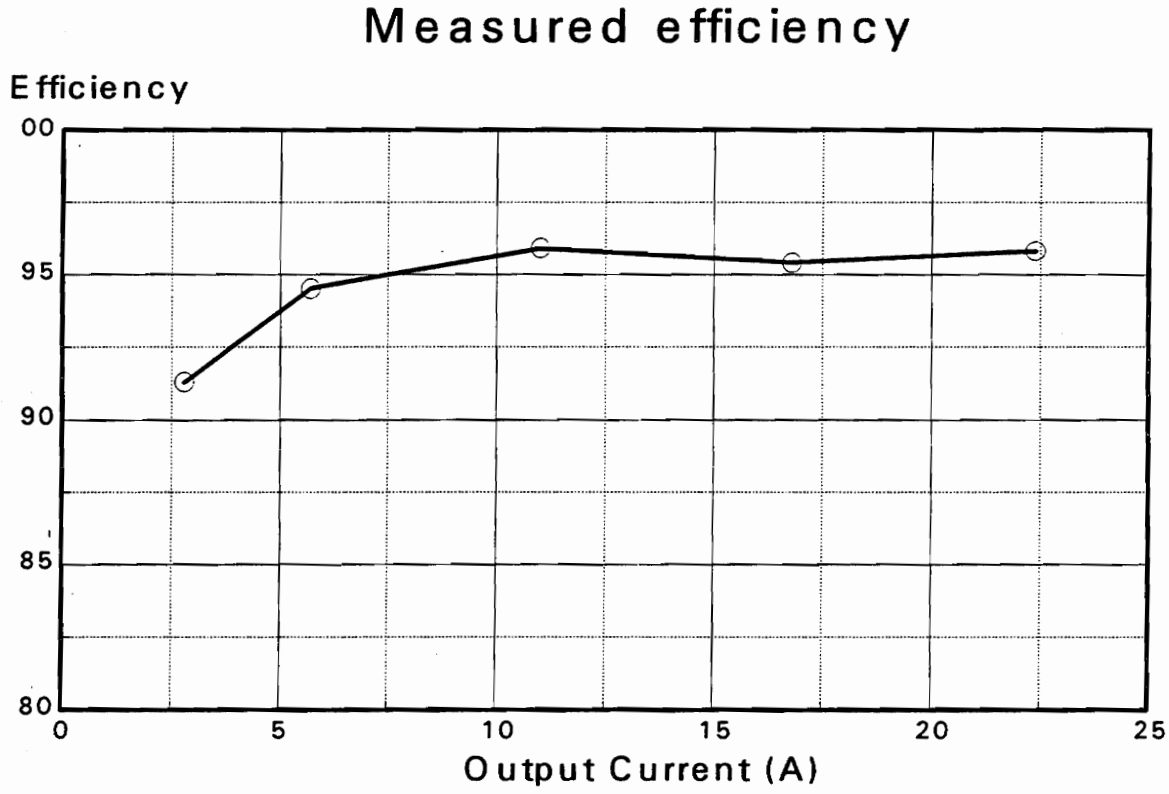


Figure 5.26: Efficiency measurements versus load for the 8 kW ZVS-FB-PWM converter with an active clamp.

Table 5.1: Loss Breakdown for the 8 kW ZVS-FB-PWM Converter.

switching frequency	100 kHz		100 kHz	
input voltage	355 V		355 V	
output voltage	360 V		360 V	
output power	8 kW		2 kW	
efficiency	95.8 %		95 %	
switches' cond.	175.2 W	50.5 %	26.0 W	24.7 %
transformer	41.2 W	11.9 %	31.9 W	30.4 %
external inductor	11.2 W	3.2 %	5.3 W	5.0 %
filter inductor	17.9 W	5.2 %	5.9 W	5.6 %
rectifier	94.5 W	27.2 %	24.5 W	23.3 %
switching	0.0 W	0.0 %	7.5 W	7.1 %
clamp	7.2 W	2.1 %	4.3 W	4.1 %
Total losses	347.2 W	100.0 %	105.0 W	100.0 %

5.8 Comparison of ZVS-FB-PWM with Resonant Converters

To compare the ZVS-FB-PWM converter with the resonant converters, a converter has been designed for the same specs as the resonant converters in chapter 2:

- Output power 100 W,
- Output Voltage 5 V,
- Input Voltage from 200 V to 300 V,
- Switching frequency 500 kHz.

Three designs are have ZVS from full load to 100%, 75%, 50%, and 25% load, respectively. Table 5.2 presents the main parameters for the four designs.

The expression for the primary current has been given in Eq. (5.13). The power factor of the primary of the ZVS-FB-PWM converter is

$$PF_{ZVS-FB} = \frac{D}{1+4\cdot\frac{L_{lk}}{R_{load}}\cdot f_{sw}} \cdot \frac{1}{\sqrt{D\left(1-\frac{2}{3}\cdot D\cdot\left(1-\frac{1}{1+4\cdot\frac{L_{lk}}{R_{load}}\cdot f_{sw}}\right)\right)}}, \qquad (5.45)$$

Figure 5.27 shows the operating region for the design with ZVS only at full load. The top graph of Figure 5.27 shows the primary current normalized with respect to the output power divided by the input voltage, and the bottom graph shows the operating region power factor. Lower power factors correspond to higher primary currents.

Figures 5.28 and 5.29 present the operating region power factor for the four designs. The power factor is reduced for designs with a wider ZVS range.

For comparison purposes Figures 5.30 reproduces the operating region power factor for the designs for the SRC and PRC obtained in Chapter 2, and Figure 5.31 reproduces the operating region power factor for the LCC-RC designs.

The ZVS-FB-PWM results in less circulating current than the resonant converters' designs, except for the cases with ZVS at high line from full load to 50% load and 25 % load, respectively. The SRC results in better power factor than the ZVS-FB-PWM with ZVS range larger than form full load to 50 %. Large ZVS range result in more loss of duty cycle, and consequently in larger circulating currents. The circulating currents can be kept lower than for the resonant converters slecting the ZVS range apropiately..

Table 5.2:Designs for the ZVS-FB-PWM Converters

		Design 1	Design 2	Design 3	Design 4
$L_{lk,}$ (μH)		7	11.75	22	39
N_p / N_s		34	33	30	20
ZVS	high line	100	75	50	25
	low line	74	56	37	18
D (full load)	high line	0.6	0.6	0.6	0.6
	low line	0.9	0.9	0.9	0.9
ΔD (full load)	high line	0.027	0.047	0.098	0.26
	low line	0.041	0.071	0.147	0.39
D (10 % load)	high line	0.57	0.56	0.51	0.36
	low line	0.85	0.83	0.77	0.54
I_{prim} (rms)	high line	0.58	0.60	0.65	0.91
	low line	0.58	0.59	0.63	0.86

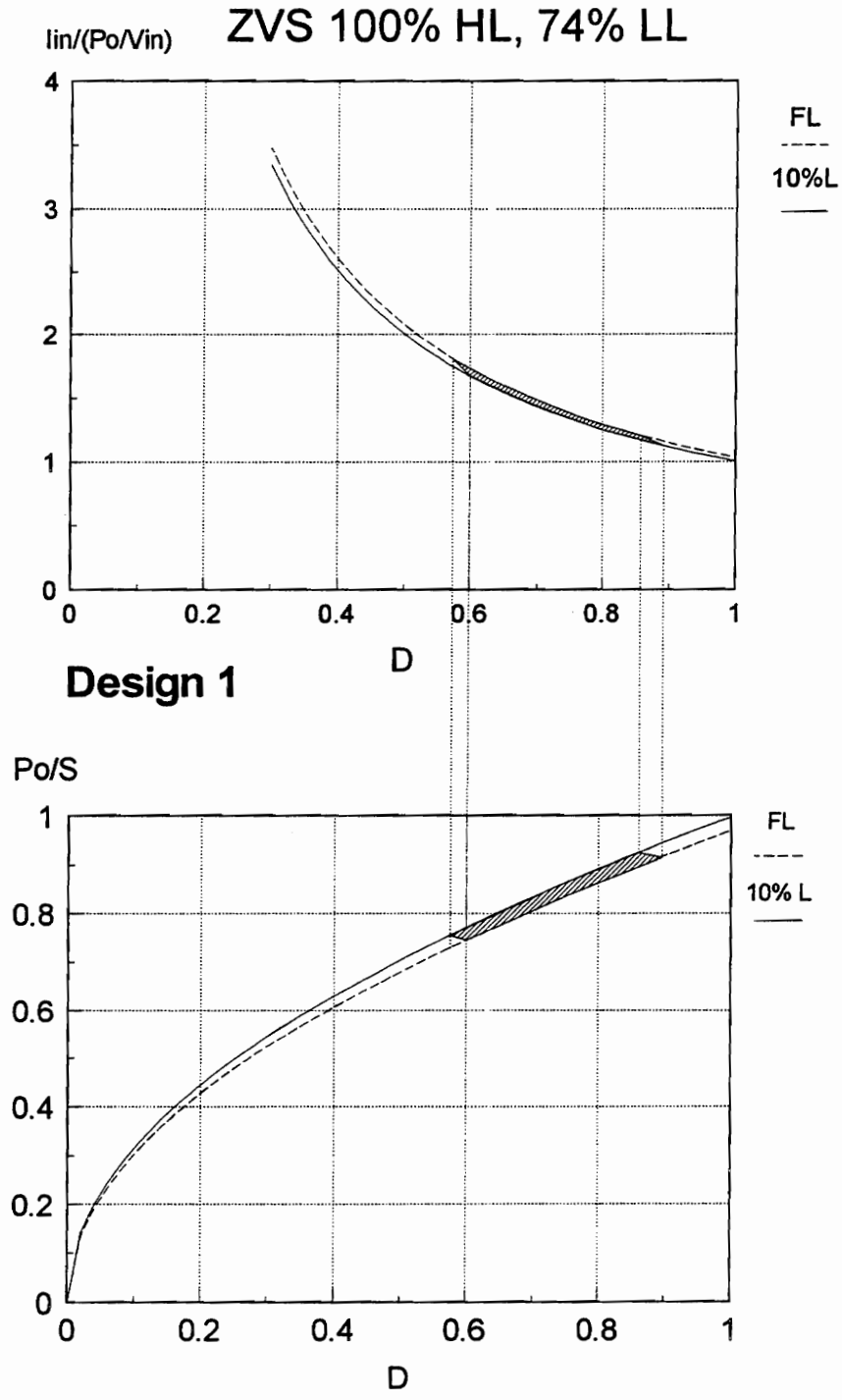


Figure 5.27: Power factor corresponding to the operating region of the ZVS-FB-PWM converter design ZVS only at full load.

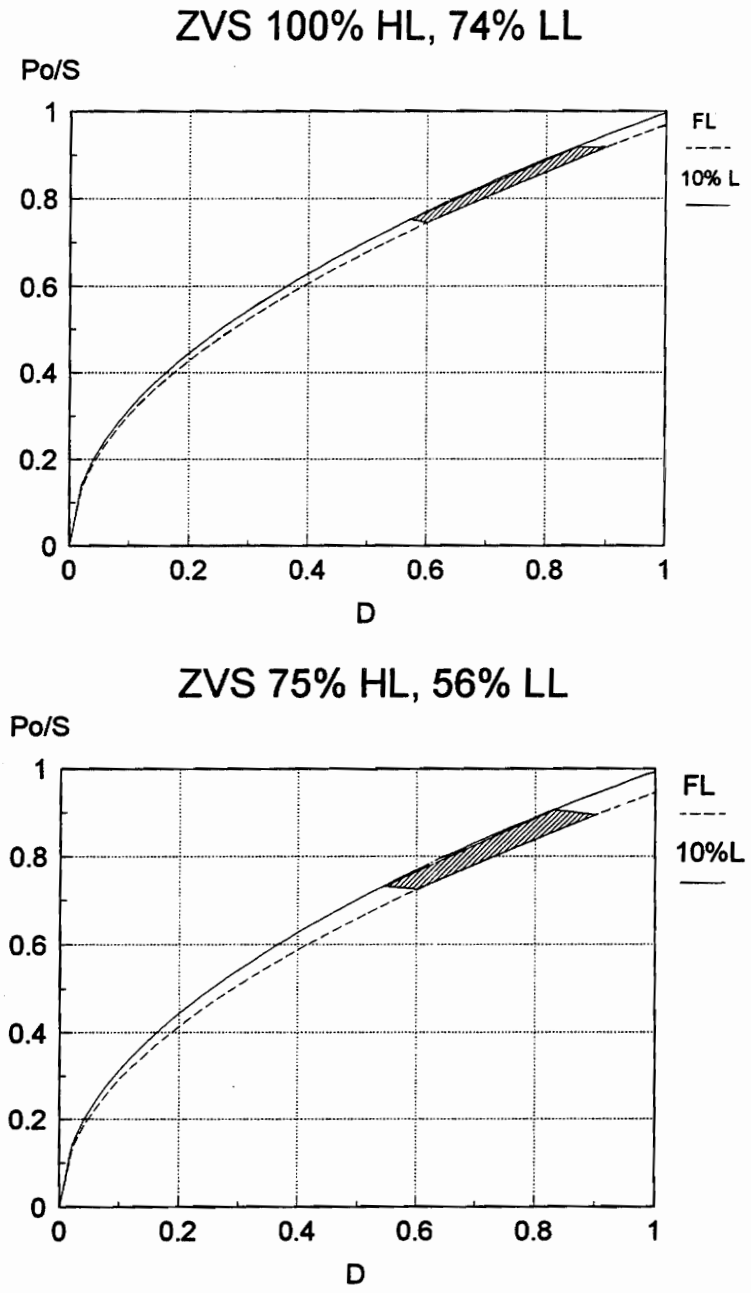


Figure 5.28: Power factor corresponding to the operating region of the ZVS-FB-PWM converter designs with 100% and 75% ZVS range.

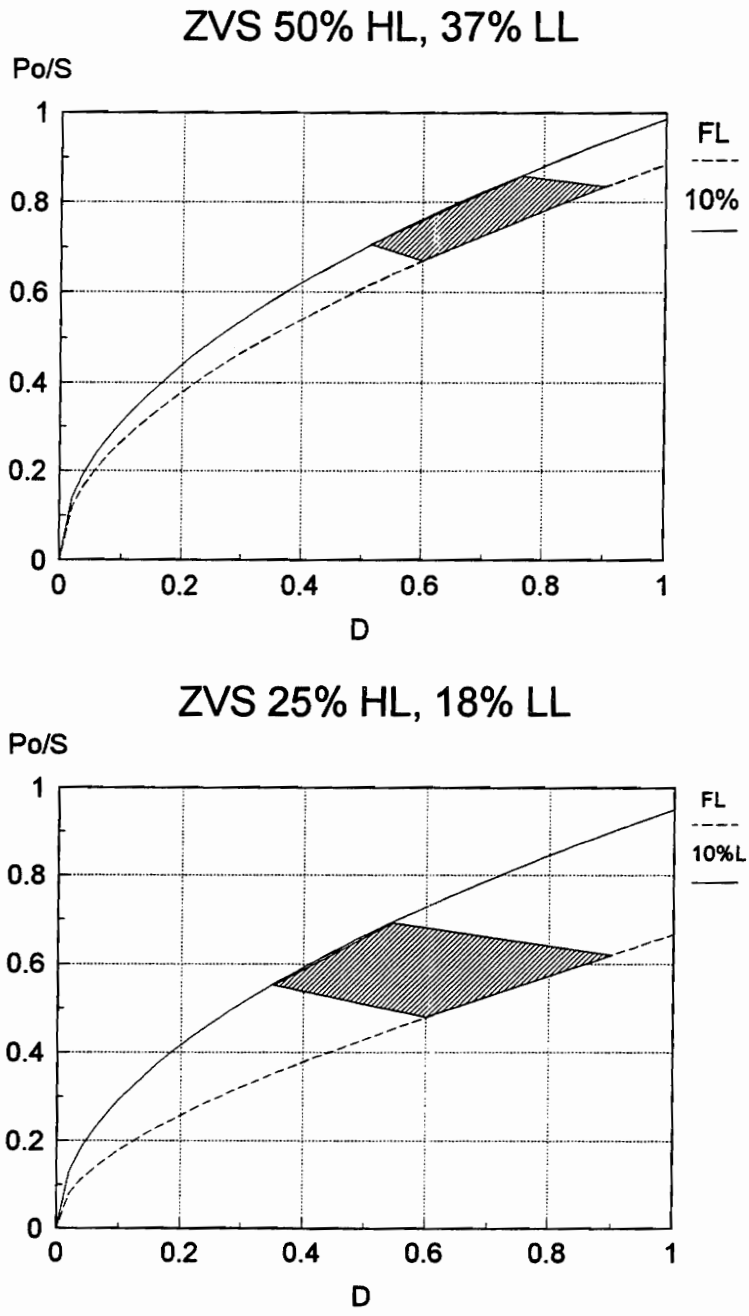


Figure 5.29: Power factor corresponding to the operating region of the ZVS-FB-PWM converter designs with 50% and 25% ZVS range.

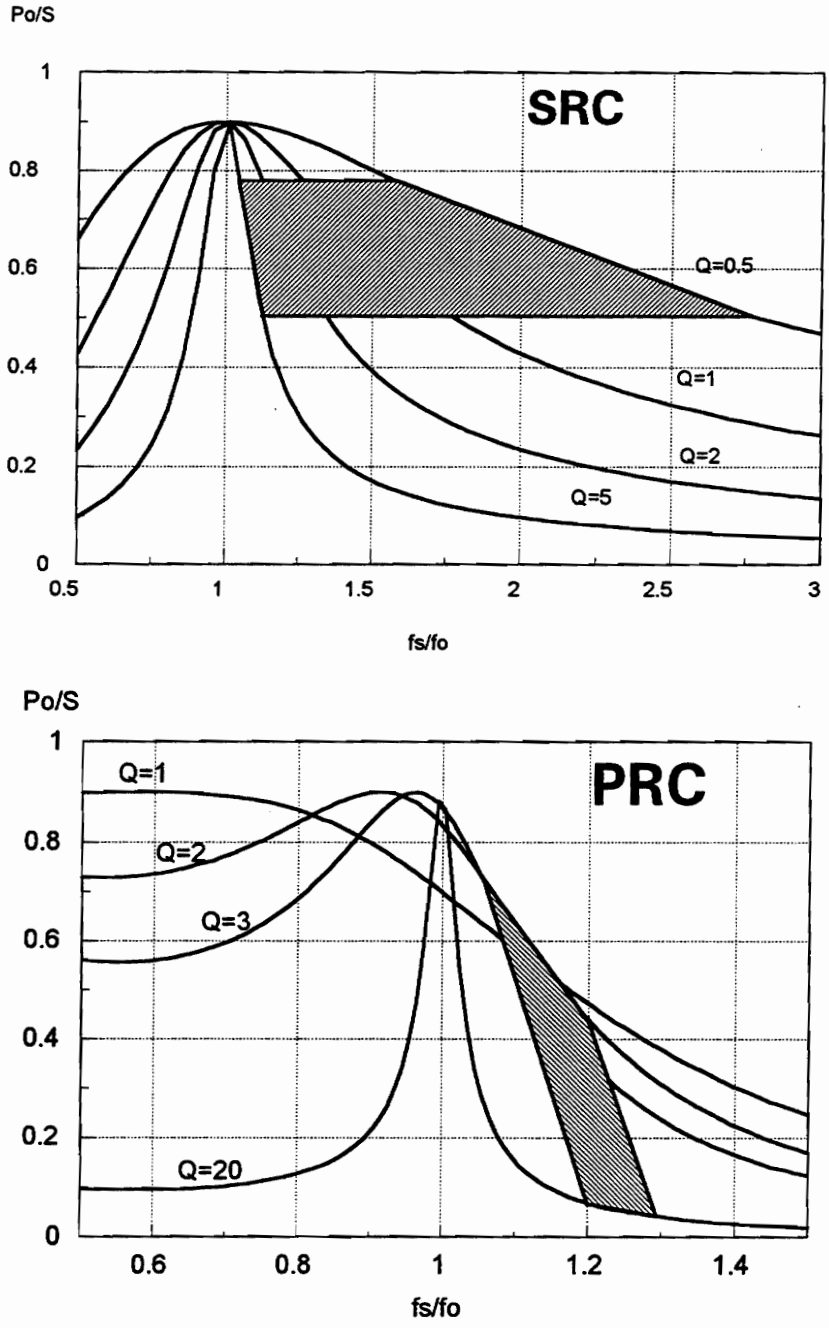


Figure 5.30: Power factor corresponding to the operating region of the SRC and PRC designs, respectively.

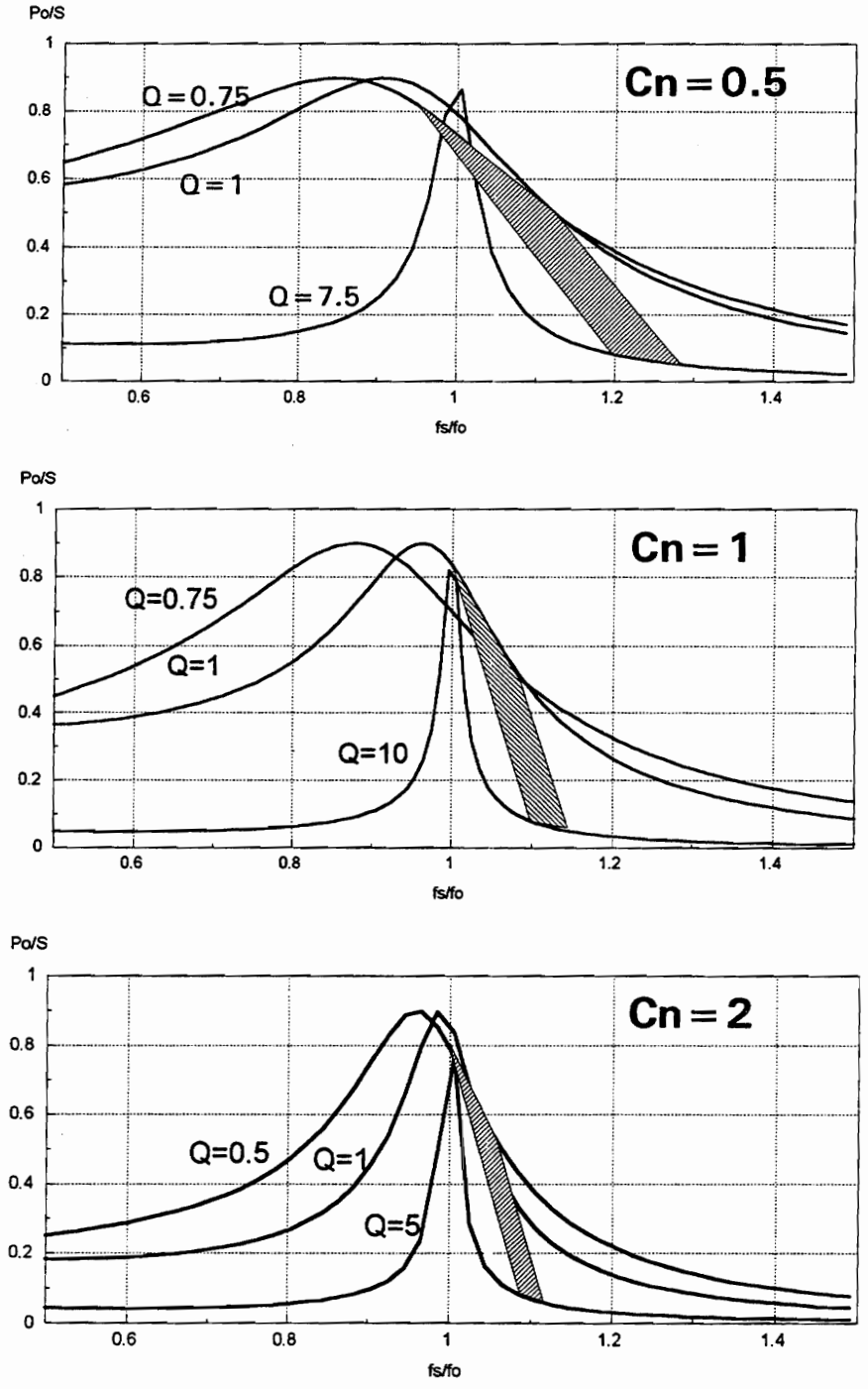


Figure 5.31: Power factor corresponding to the operating region of the LCC designs for C_n=0.5, 1, and 2, respectively.

6. Conclusions and Future Work

This dissertation presents a comparative evaluation of different zero-voltage-switching (ZVS) bridge converters, and a comprehensive analysis of several alternatives, providing a design procedure to optimize the efficiency.

A design-oriented analysis for resonant converters is developed. This analysis uses the fundamental of the voltages and currents in the converter. The results obtained have been verified and compared with those of the exact analysis, available for the SRC, the PRC, and the LCC-RC.

The simplified analysis gives an expression for the input current to the resonant tank normalized with respect to the output power divided by the input voltage. This normalization provides a clear representation of how the selection of parameters affects the currents in the resonant tank and the inverter bridge, and thus facilitating the selection of parameters to minimize the currents for an optimally efficient design. Also, the reactive power required at the resonant tank can be calculated using the simplified analysis approach. The reactive power required by the tank is a good measure of the current in the bridge and can be used as the basis for comparison of the different converters considered.

A systematic procedure to obtain all possible resonant converters with two or three reactive elements in the resonant tank is provided. All the possible topologies have been presented, and the analysis has been used to determine their basic properties.

The possible resonant converters with two reactive elements are the SRC, the PRC, and their duals. The determination of the gain characteristics for the three-element resonant converters shows that they can be grouped into two major categories according to the similarity of their gain characteristics with the SRC and the PRC. The similarity of the behavior of the LCC-RC to an SRC or to a PRC varies according to the parameters selected in its design.

To compare the SRC and PRC with the LCC-RC, a design example has been used. The comparison of the designs for the SRC and PRC and several designs of the LCC-RC for different capacitor ratios show that the LCC-RC is a superior alternative. The selection of a capacitor ratio for the LCC-RC allows a design that requires less reactive power than the PRC over the whole load and line range, while requiring a smaller frequency range than the SRC, and requiring no more reactive power than the SRC at full load.

The analysis has been extended to the constant-frequency phase-shifted resonant converters. The results obtained have been verified comparing them with the exact analysis available for the PS-SRC and the PS-PRC.

Designs of the PS-SRC and the PS-PRC have been built to compare their characteristics. The PS-SRC cannot be designed to operate from full load to no load with ZVS. However, the efficiencies obtained at full load are very similar for both.

A comparison of the PS-PRC and the PS-LCC is based on the design procedure defined by the simplified analysis. The designs for both options minimize the reactive

power required for the tank in order to optimize the efficiency, and allow operation with ZVS from full load to no load. The results show that better efficiency is expected for the PS-LCC, because choosing a capacitance ratio, C_n=0.5, less reactive power is required to achieve ZVS over the whole load and line ranges.

The designs show that the efficiency of the phase-shifted resonant converter is lower than for its conventional counterparts because in order to achieve ZVS over the whole line and load range a design with higher reactive power is required.

The effect of the switch capacitance on the ZVS is critical particularly when designs with low Q are used. Since the designs that result in less reactive power being required by the resonant tank for the PS-LCC have Q values lower than one, it is of great interest to analyze this effect. The analysis requires a numerical procedure to solve the circuit's differential equations since the fundamental approximation cannot be used in this case.

The effect of the output capacitance of the switch is more pronounced for the SRC, resulting in a higher frequency of operation required to achieve ZVS, and even making it impossible to achieve ZVS below a certain value of Q. The increase in frequency and Q values results in a higher reactive power required by the resonant tank, and consequently, a reduction in efficiency. The effect is minimal for the PRC, for which only very large values of the switch capacitance significantly change the ZVS limit frequency for the Q's of interest, and there is no appreciable loss of voltage gain. The effect on the LCC-RC is somewhere in between the effect on the SRC and on the PRC, according to the capacitance ratio selected. For a lower capacitance ratio ($C_n=C_p/C_s$), the converter 's

characteristics approach those of an SRC and the effect is more pronounced, while for large capacitance ratios the effect is less pronounced, as it is for the PRC.

The results are presented such that the information is easily usable for design purposes. The results have been verified experimentally with a hardware prototype of an LCC-RC.

An alternative with efficiency superior to that of the resonant converters is the ZVS-FB-PWM converter. This converter achieves ZVS by allowing the leakage inductance of the transformer to resonate with the output capacitance of the devices of the bridge using phase-shift control. This new converter has recently become very commonly used, and a new complete analysis is presented together with the its design procedure.

The main feature of the ZVS-FB-PWM is its PWM control with the low rms currents, characteristic of PWM converters. ZVS cannot be achieved from full load to no load for the leading leg of the bridge. However, unlike resonant converters, the ZVS loss is gradual, decreasing proportionally to the energy available in the leakage inductance, and operation at light loads without ZVS is practical.

The analysis and design procedure have been verified in two prototypes with 2 kW and 8 kW output power respectively, resulting in efficiencies higher than 95% at full load.

A major problem for the ZVS-FB-PWM for relatively large output voltages is the ringing across the rectifier. Since the leakage inductance is used to achieve ZVS for the bridge inverter, it is designed to be larger than that of a conventional PWM converter, or

even with an external inductor added if necessary. This results in a low-frequency ringing across the rectifiers that results in very large losses if a conventional dissipative snubber is used. A new active clamp circuit is presented that completely eliminates the ringing across the rectifiers in a nondissipative manner.

The new active clamp circuit analysis is provided and the design procedure is verified with a hardware implementation for a 2 kW and an 8 kW prototype.

Finally, the primary current and the reactive power required at the output of the inverter bridge are calculated to allow a comparison with the resonant converters. The current in the bridge increases when increasing the ZVS range for the design, which requires more reactive power by the primary. A design with the same specifications used for the comparison with the resonant converters shows that the ZVS-FB-PWM results in lower currents and reactive power than the resonant converters, if the ZVS range is selected to be from full load to a load above 50% at high input line.

Many areas are of interest for future research in the areas of resonant converters and the ZVS-FB-PWM. Among them, the following have considerable potential interest:

In the area of soft-switched FB-PWM converters:

- Further improvements in the ZVS-FB-PWM converter, like the use of the energy in the magnetizing inductance to achieve ZVS over a wider load and line range with less increase in circulating current, and the use of saturable inductors to reduce the amount of energy stored to achieve ZVS, and reduce

the ringing across the rectifiers. The pursuit of this line can lead to new ZVS-FB-PWM converters with better characteristics for specific applications.

- Study of zero-current switching techniques for PWM-controlled bridge topologies for cases when input current is required, or slow turn-off devices are used.

In the area of resonant converters:

- Detailed study of three-element resonant converters for applications in which the parasitics can be part of the resonant tank. Such cases can include induction-heating applications where the load is highly inductive, high-voltage converters for which the capacitance and leakage inductance of the transformer are comparable to the values of the resonant tank, components or applications in which the magnetizing inductance of the transformer is small and has to be considered part of the resonant tank.

- Evaluation of possible advantages in topologies with more than three reactive elements in the resonant tank for specific applications.

- Improvements for the fixed-frequency resonant converters. Specific topologies with more than two reactive elements can result in better performance than the SRC, PRC or LCC-RC topologies with the choice of the right parameters.

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