Effects of Ion Processing and Substrate Variables on Electrical Characteristics of GaAs

by

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(ABSTRACT)

The main objective of this study was to determine fundamental information related to ion-beam-induced damage to gallium arsenide (GaAs). The study covers experimental results concerning defect creation in GaAs versus parameters such as implantation energy, nature of GaAs substrate, crystalline orientation, and annealing. Transport and deep level transient spectroscopy (DLTS) results are presented for 50 keV Si-implanted and RTA (rapid thermal annealing) GaAs with (100) and (211) substrate orientations. Several electron traps are identified and their possible origins discussed. It is observed that (211) GaAs, after Si-implantation and RTA, has higher residual damage than (100) oriented GaAs. The electrical properties of active GaAs on Cr-doped and undoped GaAs substrates are compared. The DLTS response of active layers on Cr-doped GaAs is significantly different from those on undoped GaAs. A viable explanation that accounts for this difference is presented. The effects of furnace annealing on electrical properties of 50 keV, 4 x 10^{13} cm^{-2} Si-implanted GaAs are addressed. A correlation between the structural recovery and electrical activation is established.

The effects of 2 and 6 MeV Si implantation followed by RTA on the electrical characteristics of GaAs are investigated in detail. MeV Si-implantation and RTA generates active buried layers in GaAs. The buried layer quality is found to be at least comparable to a similarly processed keV Si-implanted active GaAs layer. The deep traps in MeV-implanted GaAs are identified and explained in terms of their probable origins. The deep level behavior of MeV Si-implanted and RTA GaAs is distinctly different from keV Si-implanted and RTA GaAs. This difference is largely due to the dynamic annealing occurring during MeV implantation.

MESFETs formed on MBE-grown $Al_{.35}Ga_{.65}As$ and low temperature MBE-grown GaAs buffer layers have shown peculiar characteristics (improved transconductance, sharper carrier profile,

variability in threshold voltage, significant backgating, etc.). The effects of $Al_{.35}Ga_{.65}As$ buffers and low temperature GaAs buffers on the electrical properties of the overlying active GaAs are investigated. Transport, DLTS, and SIMS (Secondary Ion Mass Spectroscopy) measurements are employed to explain the abnormalities in buffered MESFETs. Deep states and impurities are identified in buffers; they appear to migrate toward the channel-buffer interface during processing. The defects originating from the buffer are correlated to the performance of MESFETs formed on them.

The effects of ion processing parameters, substrate chemistry, buffer layers, and annealing on the electrical characteristics of active GaAs layers are identified. An understanding of these effects is extremely critical to obtain reproducible devices with desirable characteristics.

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List of Abbreviations and Acronyms

C-V : Capacitance-Voltage

DLTS : Deep Level Transient Spectroscopy

EPD : Etch Pit Density

EPR : Electron Paramagnetic Resonance

FA : Furnace Annealing

HB : Horizontal Bridgman

IRTA : Infra-red rapid thermal annealing

I-V : Current-Voltage

LEC : Liquid Encapsulated Czochralski

LPE : Liquid Phase Epitaxy

LT : Low Temperature

MeV : Mega electron volt

MBE : Molecular Beam Epitaxy

MESFET : Metal Semiconductor Field Effect Transistor

MOCVD : Metal-Organic Chemical Vapor Deposition

RBS : Rutherford Back Scattering

rf : radio frequency

RTA : Rapid Thermal Annealing

RTP : Rapid Thermal Processing

SAINT : Self Aligned Implantation for n^+ layer Technology

SI : Semi-insulating

SIMS : Secondary Ion Mass Spectroscopy

SL : Superlattice

TEM : Transmission Electron Microscopy

VPE : Vapor Phase Epitaxy

XRC : X-ray Rocking Curve

XRD : X-ray Diffraction

XTEM : Cross-sectional Transmission Electron Microscopy

CHAPTER 1. INTRODUCTION

1.1 Why GaAs ?

The advantages of GaAs as a material for optoelectronic devices and high speed ICs may be explained by comparing its properties with those of Si, the single most important material for the present day semiconductor devices and ICs. Table 1 shows that the electron mobility in GaAs is a factor of six greater than that in Si. Due to its large band gap it is possible to grow bulk GaAs in semi-insulating form with a resistivity greater than $1x10^6$ ohm-cm. These advantages make GaAs devices operate several times faster than Si devices, enable higher frequency operation (several GHz), and allowing for the fabrication of monolithic integrated circuits (digital and analog) with good device isolation and less parasitic components. The direct band structure enables GaAs to be used for the fabrication of optoelectronic devices (lasers, LED, etc.) and in making of heterojunction lasers with an epitaxially compatible material (e.g. AlAs).

1.2 Disadvantages

On the negative side, GaAs dissociates at temperatures above ~ 600 °C due to the high vapor pressure of arsenic. This complicates high temperature processing of GaAs because of the loss of surface As. To prevent As out-diffusion, GaAs surfaces need to be "capped" with a dielectric layer (such as SiO_2, Si_3N_4) or by using a high vapor pressure As atmosphere. Thermal instabilities and the lack of dopants with high diffusion constants have rendered thermal diffusion technology inadequate for GaAs. Unlike Si, GaAs has the disadvantage of not having a suitable native oxide. Even a deposited oxide or dielectric layer on GaAs results in a very high surface state density which makes MOS based devices unsuitable on GaAs. Therefore GaAs technology has developed based on MESFET (metal semiconductor field effect transistor) devices.

Table 1.1. Comparison of some basic material properties of GaAs and Si [144].

Property	GaAs	Si	Importance
energy gap (eV)	1.4	1.1	optical properties
intrinsic carrier concentration (cm^{-3})	$2x10^6$	$1x10^{10}$	semi-insulating
intrinsic resistivity (Ω-cm)	$4x10^8$	$4x10^5$	high isolation
electron mobility (cm^2/V-sec for $N = 10^{17}$ cm^{-3})	6000	1000	high speed
thermal conductivity (W/cm-°C)	0.5	1.4	high circuit density
vapor pressure at 1000 °C (torr)	1	10^{-8}	high temperature processing

1.3 Background

Ion implantation is used in the fabrication of a wide variety of GaAs microwave, digital, electrooptic devices and integrated circuits. Si implantation into bulk grown semi-insulating GaAs is performed to create a shallow n-type conductive layer. A thermal annealing which follows the implantation process is a requisite step to reduce ion damage and to cause implant activation. Recently, rapid thermal annealing (RTA) has emerged as a viable technique for dopant activation in ion implanted semiconductors [3]. Unlike the more conventional furnace annealing method, in which the sample is heated (usually with a cap or under an arsenic overpressure environment) at temperatures of ~ 800-900 °C for ~ 20-30 minutes, during RTA the sample undergoes a rapid temperature cycling (with or without cap) at approximately 850-900 °C for ~ 3-30 seconds.

The performance of a GaAs based device is a critical function of the electronic , structural, and chemical properties of the GaAs material. These properties are strongly influenced by both the processing variables (e.g. ion implantation, epitaxial growth, annealing parameters, etc.) and the quality of the starting GaAs substrates. In this research, the two important processes that were investigated are Si^+-implantation (into different kinds of GaAs substrates and buffer layers) and thermal annealing. Ion implantation and annealing have emerged as the principal technologies for the production of GaAs integrated circuits. Direct ion implantation into GaAs substrates provides several advantages such as simplicity, greater controllability and reproducibility in fabrication of GaAs integrated circuits. An implantation technology yielding uniform and reproducible doping characteristics across each individual substrate and from substrate to substrate is highly desirable for GaAs IC processing.

Defects generated by ion implantation present a variety of problems to be overcome in device fabrication. For the implanted dopants to dominate the carrier transport, defects must be largely removed and impurities must be largely located in appropriate lattice sites. This is achieved through high temperature annealing which causes activation but also has its own associated problems. It is therefore imperative to detect and characterize the deep levels in ion-implanted and annealed GaAs.

The study of defects in GaAs is very important since most of the electronic properties of GaAs, and consequently the performance of the device, depend ultimately on the nature and the concentration of defects present in the material. The most important defects from the technological point of view are those that are created as a result of various thermal and mechanical stresses involved in device processing. These defects are formed from the native defects, impurities, and/or complexes involving both. The characteristics of such defects must be determined and understood since they play a crucial role in limiting the high speed and noise performance of the devices subsequently formed.

This dissertation is organized into the following chapters: Theoretical Concepts (Chapter 2), Literature Review (Chapter 3), Experimental Techniques (Chapter 4), Results and Discussion (Chapter 5), and Summary and Conclusions (Chapter 6). The experimental results presented in Chapter 5 pertain to samples with widely different processing histories. A listing of several topics that are addressed in the different sections of the chapter is provided below :

Table 1.2. Topics addressed in Chapter 5.

Topics	Section number
Substrate Variables	5.1
(100) and (211) oriented GaAs	5.1.1
Undoped and Cr-doped GaAs	5.1.1
Low temperature GaAs buffer	5.1.3
$Al_{.35}Ga_{.65}As$ buffer	5.1.4
High energy (MeV) Si-implanted GaAs	5.2
Annealing and electrical activation	5.3

1.4 Research Objectives

Relatively little is known about the effects of the various processing steps on the nature and

density of deep level traps in the active layer and at the active-buffer interface of GaAs. There is a need to better understand the relationship between the substrate type, implant damage, electrical activation and damage removal. The variables investigated in this research are : ion energy, undoped or Cr doped GaAs substrates, substrate orientation, buffer layers (low temperature GaAs, AlGaAs), RTA, furnace annealing, and proximity annealing. The ways in which these variables affect deep levels, dopant distribution, and transport characteristics need to be better understood and controlled. There is growing experimental evidence indicating that defects and inhomogeneity in GaAs substrates severely limit the uniformity and performance of finished devices. A good part of this research is dedicated towards understanding the characteristics of active n-GaAs formed on low temperature GaAs or $Al_{.35}Ga_{.65}As$ buffers. The uniqueness of the active layers lies in the fact that they are MBE-grown GaAs (at normal temperature) and subsequently ion implanted and annealed to generate n-type activity. As will be seen in Chapter 3, almost all the reported results are on MBE grown n-layer on various buffer layers and practically no data exists on the characteristics of MBE-grown, ion-implanted, and annealed GaAs.

There is almost a complete lack of understanding of the deep level and transport properties in (211) oriented GaAs, although the (211) orientation has been reported to yield better device performance than the more conventional (100) oriented GaAs [130]. In view of this it is extremely important to assess the merits and demerits of the two orientations involved with regard to their electrical characteristics.

As discussed in Chapter 3, the low temperature MBE grown GaAs buffer has gained considerable interest due to its high resistivity, which allows it to provide excellent device isolation. Although, the electrical and structural characteristics of such layers have been investigated in detail, the effects of such a layer on an overlying implanted and annealed GaAs layer are not well understood. There exist numerous problems on the applicability of low temperature MBE grown GaAs as a buffer layer for MESFETs, the solution of which must be sought in understanding the electrical characteristics at the buffer-active layer interface.

High energy (MeV) implantation into GaAs offers a number of attractive advantages in creating buried active layers. Most of the work on high energy implantation in GaAs has been confined to the study of structural and transport characteristics of the buried layer. There is a near-complete lack of data on details of the deep level characteristics of MeV Si-implanted GaAs. A part of this research is aimed towards establishing the identity of electrically active defects in MeV Si-implanted and RTA annealed GaAs. The electrical characteristics of the MeV implanted active layer are compared with those formed by keV implantation. The damage and annealing mechanisms in keV and MeV implanted GaAs are addressed.

Based on the above discussion, the present work has multiple objectives, and are listed in the order in which they appear in Chapter 5. Those objectives are :

1. To compare (100) and (211) GaAs substrates electrically, to better understand the orientation effects on device behavior.
2. To study the effects of substrate stoichiometry (Cr-doped and undoped) on the electrical properties of Si-implanted and RTA-annealed GaAs.
3. To understand the role of an MBE-grown $Al_{.35}Ga_{.65}As$ buffer layer and low temperature (LT) MBE-grown GaAs buffer layer on the electrical behavior of Si-implanted active layers. To obtain a correlation between FET performance (with or without a buffer) and the characteristics of the corresponding active layer.
4. To gain a better understanding of the electrical properties of high energy (MeV) Si-implanted and RTA-annealed GaAs.
5. To establish a correlation between electrical activation and damage recovery in 50 keV Si-implanted GaAs:Cr by isochronal (20 mins.) proximity annealing; to address the electrical behavior of disordered and anneal-induced ordered GaAs.

The theoretical considerations and the experimental techniques used to meet the above objectives, and the findings of this research, are discussed in the subsequent chapters.

CHAPTER 2. THEORETICAL CONSIDERATIONS

2.1 Metal-GaAs Interface

One of the early theories explaining the barrier at a metal-semiconductor interface is due to the model proposed by Schottky [145]. According to this model, the metal-semiconductor barrier height (Φ_b) is a function of the metal work function (Φ_m) and the electron affinity of semiconductor (χ_s),

$$\Phi_b = \Phi_m - \chi_s \qquad (2.1)$$

However in GaAs, due to the localized surface states with energies within the band gap, Φ_b is not a function of Φ_m. These states are associated with surface potential fluctuations caused by the crystal lattice imperfections at the surface. A high density of surface states (~10^{13} cm^{-2} or higher) can accommodate the contact potential difference between the metal and GaAs, thereby pinning the Fermi level at the GaAs surface (Fig. 2.1a). The pinning of the Fermi level results from the submonolayer coverage of different metals or oxygen (mostly as contaminants) and the level being virtually independent of the nature of the contamination. The high surface state density of GaAs "pins" the Fermi level roughly at 0.8 eV below the conduction band minimum [146].

The Schottky barrier gate is one of the most important elements in many GaAs devices. When a metal is placed on n-GaAs, the difference in Fermi level (more accurately between the surface and the bulk) results in the formation of a depletion region in GaAs. For all practical purposes, a Schottky diode can be treated analogous to an one-sided abrupt p^+-n junction with the space charge layer on the n-GaAs side (Fig. 2.1b). On assuming a sharp boundary at the edge of the depletion region, the relationship between the depth of the depletion region (W) and the applied bias (V), for the case of uniform doping (N_D) can be expressed as [147]

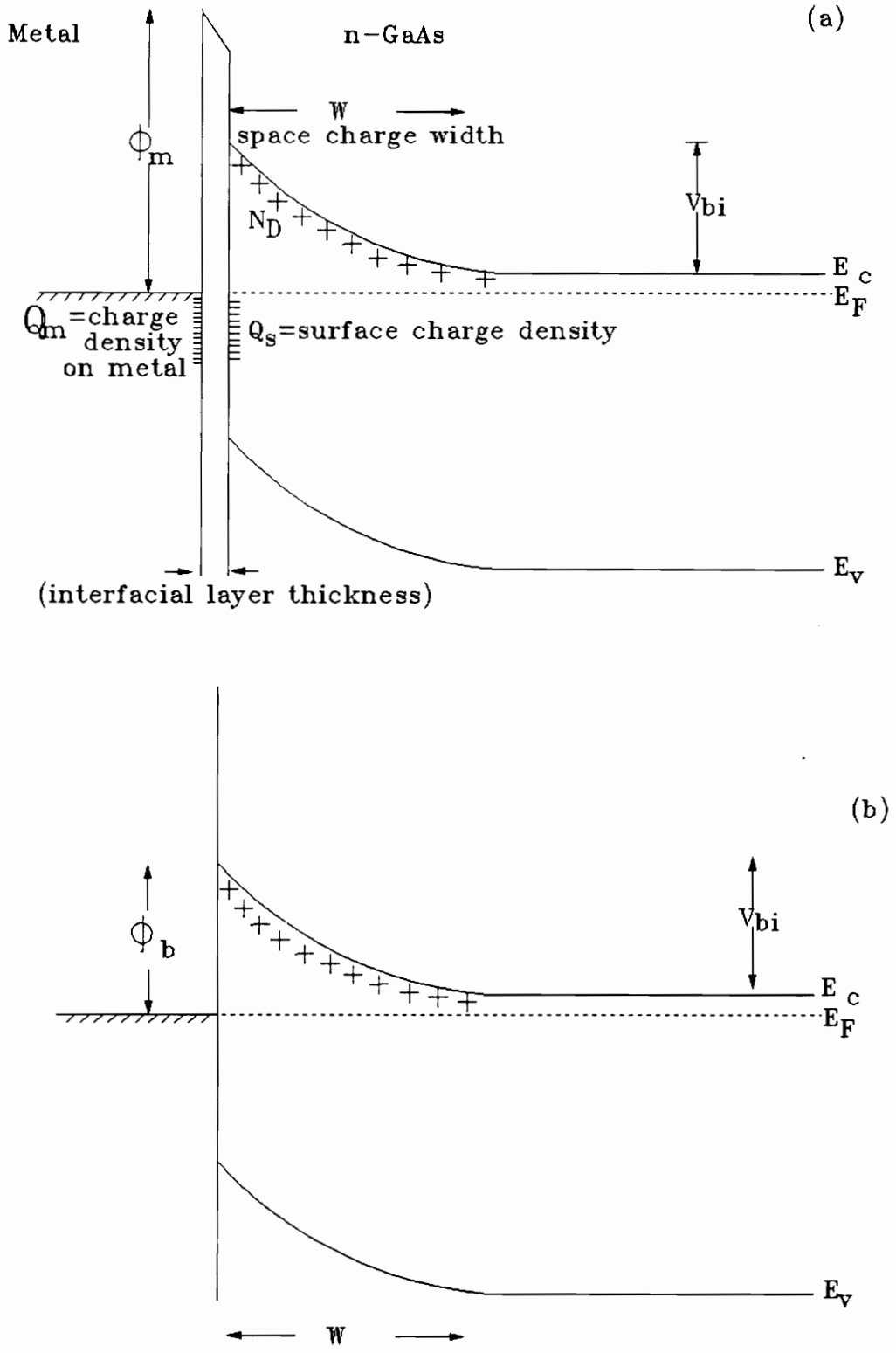


Fig. 2.1 Energy band diagram for a) Schottky barrier with surface states and b) ideal Schottky barrier (from Ref. [151]).

$$W^2 = \frac{2\epsilon}{qN_D}\left(V_{bi} - V - \frac{kT}{q}\right) \qquad (2.2)$$

where ϵ is the semiconductor permittivity, k is the Boltzmann constant, T is the temperature, q is the electronic charge, and V_{bi} is the built-in potential (approximately 0.8 V for GaAs) required to support the depletion layer. In the case of a non uniform doping profile ($N_D(x)$), the relationship is of the form

$$V_{bi} - V = \frac{q}{\epsilon}\int_0^W xN_D(x)\,dx \qquad (2.3)$$

2.1.1 Depletion Region

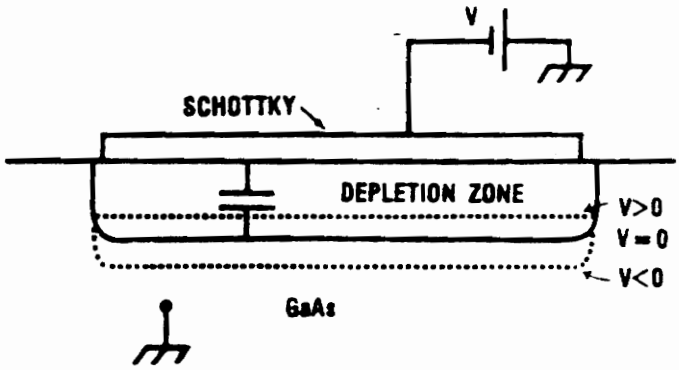
The depletion region, acting as a parallel plate capacitor of thickness W (see Fig. 2.2a), has a depletion layer capacitance (C), expressed as

$$C = \frac{dQ}{dV} = \frac{\epsilon A}{W} \qquad (2.4)$$

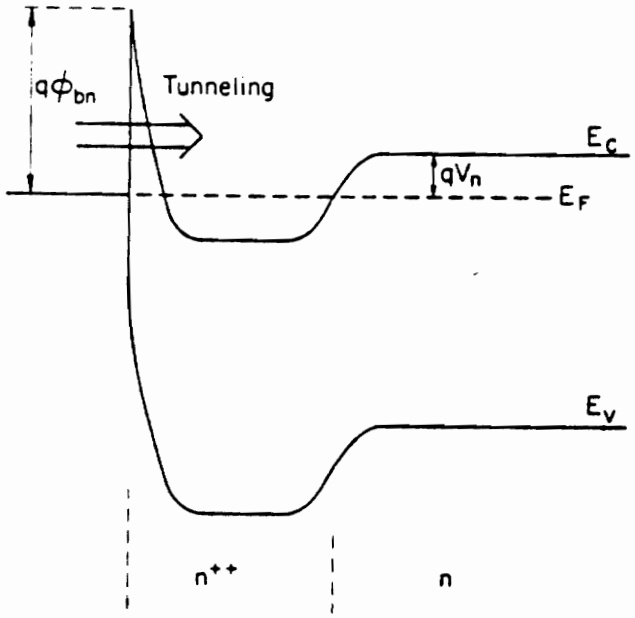
where A is the Schottky diode area or the contact area. It is evident from equations (2.2) and (2.3) that the depletion layer width (W) is bias dependent i.e. W increases with increasing reverse bias until the breakdown voltage is reached, beyond which W cannot be extended further. Using equations (2.3) and (2.4), one can arrive at a relationship relevant for deducing the dopant profile in semiconductors and is given by

$$N_D(x) = \frac{2}{q\epsilon A^2}\frac{-1}{d[1/C^2]/dV} = \frac{C^3}{q\epsilon A^2}\left(\frac{dC}{dV}\right)^{-1} \qquad (2.5)$$

The above result is also true for the case of uniform doping density. Equation (2.5) is widely used in the determination of the dopant concentration distribution by the C-V (Capacitance-Voltage) method. The C-V measurements, for this purpose, are performed at high enough frequency (usually 1 MHz) so that the effects of deep levels in the dopant profile are eliminated. At high measurement



a)



b)

Fig. 2.2 a) Depletion region under a Schottky contact behaving as a parallel plate capacitor and b) Energy band diagram for tunnel type ohmic contact (from Ref. [183] and [151], respectively).

frequencies the electron emission or capture processes from deep levels are slow to respond to the measurement signal.

Resolution in doping profile determination using the C-V method is limited to a distance on the order of the Debye length [148]. The Debye length is due to the electron screening effects and represents a departure from the abrupt boundary at the bottom of the depletion region. The Debye length is given by

$$L_D^2 = \frac{kT\epsilon}{q^2 N_D} \qquad (2.6)$$

For $N_D \sim 10^{17}$ cm^{-3}, the Debye length is on the order of 0.02 μm. The C-V procedure has a minimum and maximum depth between which the method is valid for dopant profiling. The minimum depth is approximately decided by the depletion layer width formed due to the built-in voltage (~ 0.8 V) across the Schottky barrier. Although a forward bias can shrink the depletion region to a minor extent, the forward leakage current, at such bias, prohibits any valid capacitance measurements. On the other extreme, the maximum depth of probing by the C-V technique is limited by the reverse breakdown voltage of the Schottky diode.

The above analysis (C-V) is based on the tacit assumption that the capacitance is the only element in the measuring circuit. Almost all capacitance meters and profiling instruments measure capacitance by applying a small rf voltage (much smaller than the dc bias that determines the diode capacitance) while monitoring the imaginary component of the resulting rf current i.e.

$$I = \frac{V}{Z} = V(i\omega C) \qquad (2.7)$$

In presence of series resistance (R_s), which always exists between the Schottky barrier and the ohmic contact of a diode, the current is modified to

$$I = \frac{V}{R_s + (i\omega C)^{-1}} = V\left(\frac{R\omega^2 C^2}{1+(\omega R_s C)^2} + \frac{i\omega C}{1+(\omega R_s C)^2}\right) \qquad (2.8)$$

Since the capacitance bridge measures only the out-of-phase component of the current, the measured capacitance C_m is related to the actual capacitance (C) by

$$C_m = \frac{C}{1+(\omega RC)^2} \qquad (2.9)$$

It is obvious from (2.9) that if the series resistance value is high then the measured capacitance and consequently the doping concentration values will be erroneous. In principle, these errors can be corrected if the phase angle of the rf measurement signal is also monitored during the measurement [149].

Many times, for the purpose of characterizing a Schottky barrier, the presence of an ohmic contact is not mandatory. Two Schottky diodes in a back-to-back configuration, with appropriate modification in formulae, may be used instead. If one of the diode's area is significantly bigger than the other, then the bigger diode may be treated as ohmic. In the back-to-back geometry, the two diodes are in series and the effective capacitance (C) at zero bias is given by

$$\frac{1}{C} = \frac{1}{C_d} + \frac{1}{C_D} = \frac{d}{\epsilon A_d} + \frac{d}{\epsilon A_D} \qquad (2.10)$$

where A_d, A_D are the area of small and big diodes, respectively, and C_d and C_D are their corresponding capacitances. On reverse biasing the smaller diode, all the voltage drop will occur across the depletion region of the smaller diode but the bigger diode, for practical purposes, will be under zero bias condition. On knowing the effective capacitance at zero bias and the areas of each diode, the individual capacitances of the diodes (small and big) under bias can be determined from the effective capacitance value at that bias. The back-to-back Schottky geometry can be utilized in dopant profile (C-V) and DLTS (to be discussed later) measurements.

2.2 Current Transport

The dominant current transport mechanism across a Schottky barrier is due to thermionic emission [150]. The thermionic emission current originates from the electrons having sufficient energy

to surmount the metal-semiconductor contact barrier. The current-voltage (I-V) relationship of a Schottky diode is expressed by the thermionic emission model as

$$I = I_0(\exp[\frac{qV}{nkT}] - 1) \qquad (2.11)$$

where T is the diode temperature; k, the Boltzmann constant; n, the ideality factor representing departure from ideal Schottky junction (n=1); and I_0 is the reverse saturation current which is related to the Schottky barrier height Φ_b as

$$I_0 = AA^{**}T^2\exp(-\frac{q\Phi_b}{kT}) \qquad (2.12)$$

where A is the diode area; A^{**} is the effective Richardson constant which is dependent on the effective electron mass and for GaAs, A^{**} is 120 A/(cm K)^2 [147]. The value of A^{**}, compared to T, has a relatively insignificant effect on Φ_b, since it appears outside the exponential term in (2.12). For example, a 100 % error in A^{**} will cause an increase of only about 0.018 eV in Φ_b. The reverse saturation current (I_0) and the ideality factor (n) are the two most important Schottky diode parameters which give a measure of the diode quality. The diode barrier height can be obtained by performing I-V measurements over a temperature range and making use of equations (2.11) and (2.12).

2.2.1 Ohmic Contacts

By definition, good ohmic contacts have small resistances and inject (or extract) only a few minority carriers. The I-V characteristics of such contacts should be linear and stable over time and temperature. The ohmic contact resistances at the source and drain of a FET contribute to parasitic resistance and are therefore very important to FET performance. It is not possible to make metal contacts on GaAs without forming a dipole layer [151]. Therefore , ohmic contacts with Φ_b=0 cannot be made on low doped GaAs by simply choosing a metal with an appropriate work function. Whenever a metal contact is put on moderately or low doped GaAs, the junction is rectifying. To

fabricate ohmic contacts on GaAs, the general procedure is to dope a thin layer of GaAs underneath the contact to as high level as possible. This results in a narrow depletion region and consequently, a thin electron barrier as shown in Fig. 2.2b. At sufficiently high doping levels, the surface barrier becomes thin enough to allow transport to occur by tunnelling (or field emission). As the doping level in a semiconductor increases, the width of the potential barrier decreases and therefore, the tunnelling probability increases. The current density (J) for field emission can be approximately expressed as

$$J \sim \exp\left[-\frac{q\phi_b}{E_{00}}\right] \qquad , \text{ where } \quad E_{00} \approx \frac{gh}{4\pi}\sqrt{\frac{N_D}{\epsilon m^*}} ,$$

h is Plank's constant and m^* is the electron effective mass.

Most often ohmic contacts on n-GaAs are realized through alloyed contact of Au (88%)-Ge(12%) with a Ni or Pt overlayer. Ge occupies Ga lattice sites on ohmic annealing and results in the formation of a n^+ region underneath the contact. A figure of merit for ohmic contacts is the specific contact resistance (r_c) defined as

$$r_c = \left[\frac{\partial V}{\partial I}\right]_{V=0} \qquad (2.13)$$

An optimum value of r_c during device processing is ~ 10^{-6} Ω-cm^{-2}.

2.3 Schottky Barriers with Traps

In the treatment of Schottky barriers in section 2.1, the presence of traps in the semiconductor has been neglected. Bleicher and Lange have treated the time and bias dependence of Schottky barrier capacitance in the presence of deep level traps [152]. Consider a Schottky barrier formed on a n-type semiconductor having a shallow donor density N_D, and a deep donor, located at E_C-E_T, with concentration N_T. Assume a reverse bias, V_R, is applied to the diode and the resulting band diagram together with the charge distribution is shown in Fig. 2.3. The electrons are depleted in the region $0 \le x \le W$, where W is the width of the space charge region. In the depletion or the space

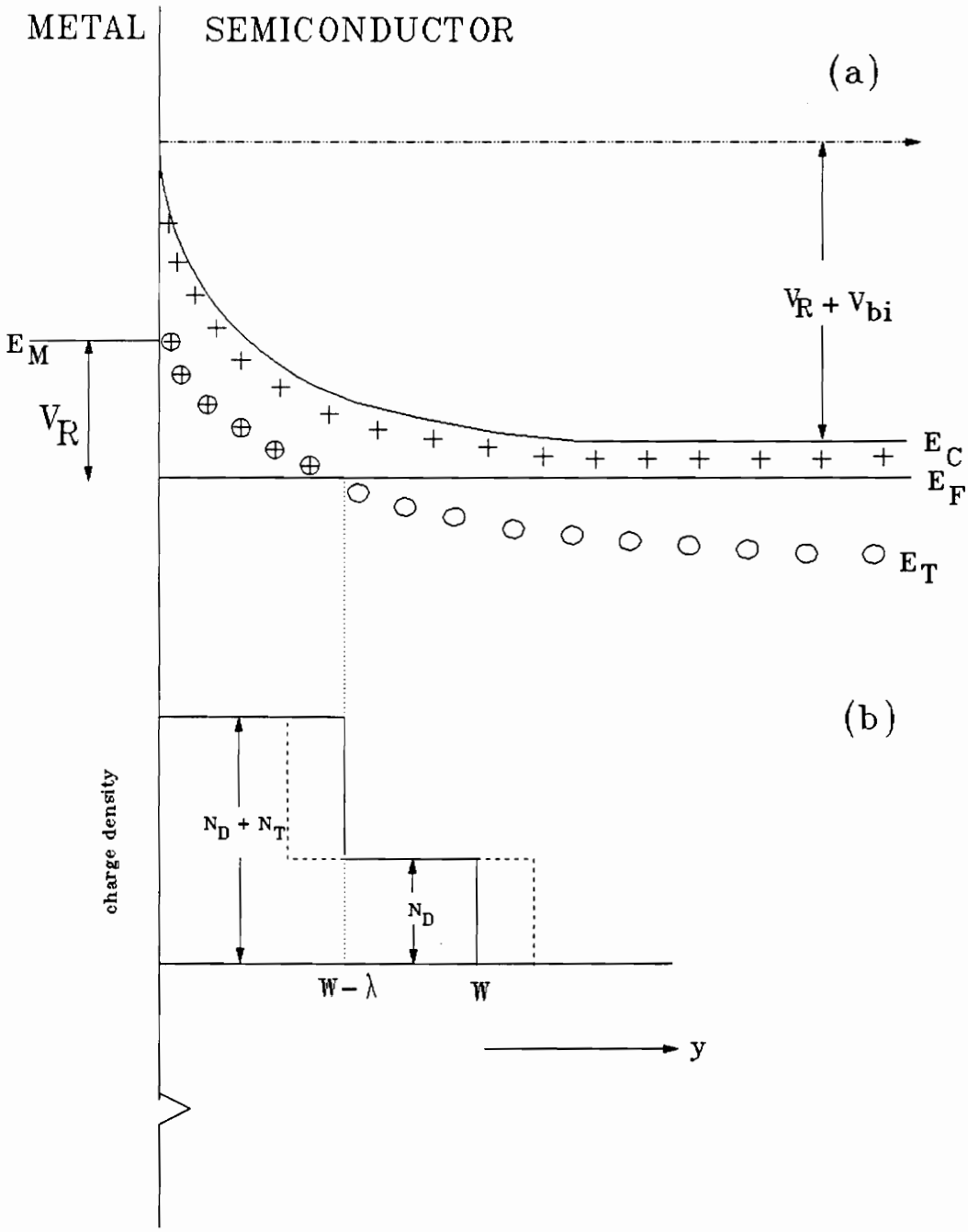


Fig. 2.3 a) Energy band diagram of a Schottky diode with a deep donor level under a quiescent reverse bias and b) Corresponding charge distribution under equilibrium (solid line) and under non equilibrium i.e. immediately after a bias pulse (dashed line) conditions (from Ref. [173]).

charge region, the electronic states at the deep level are empty in the region $0 \le x \le W-\lambda$, where $W-\lambda$ is the plane where the deep level crosses the bulk Fermi level, E_F. For a non-uniformly doped material $N_D(x)$, λ is given by

$$E_F - E_T = \frac{q^2}{\epsilon} \int_{W-\lambda}^{W} N_D(x) \, [x - (W-\lambda)] \, dx \qquad (2.14)$$

where q is the electronic charge and x is the distance from the surface. For $N_D(x)$ being constant as in a uniformly doped material, the above equation yields

$$\lambda = \left[\frac{2\epsilon (E_F - E_T)}{q^2 N_D} \right]^{\frac{1}{2}} \qquad (2.15)$$

and double integration of Poisson's equation over the depletion region yields [173]

$$V_R + V_{bi} = \frac{q}{\epsilon} \left[\int_0^{W-\lambda} N_T(x) \, . x dx + \int_0^{W} N_D(x) \, . x dx \right]$$

where V_{bi} is the built-in potential, V_R is the applied reverse bias and for $N_D(x) = N_D$ and $N_T(x) = N_T$, the above relationship may be expressed as

$$V_R + V_{bi} = \frac{q}{2\epsilon} \left[(N_D + N_T) W^2 + N_T (\lambda^2 - 2W\lambda) \right] \qquad (2.16)$$

The capacitance of a Schottky diode, in the presence of a uniform trap density (N_T) and a shallow donor density (N_D), can be obtained by combining equations (2.2), (2.4), and (2.16) and is expressed as

$$C = \sqrt{\left[\frac{N_T A \epsilon q \lambda}{2\epsilon V - q\lambda^2 N_T} \right]^2 + \frac{(N_D + N_T) q \epsilon^2 A^2}{2\epsilon V - q\lambda^2 N_T}} - \frac{N_T A q \epsilon \lambda}{2\epsilon V - q\lambda^2 N_T} \qquad (2.17)$$

where $V = V_{bi} + V_R$. Equation (2.17) is a generalized expression for a Schottky diode capacitance and is not limited to any special value of frequency, bias or trap density. As a special case, when the measurement signal frequency is very high such that the traps do not contribute to the capacitance, then the above relationship may be expressed as

$$C = \sqrt{\frac{qA^2 \epsilon N_D}{2(V_{bi}+V_R)}} \qquad (2.18)$$

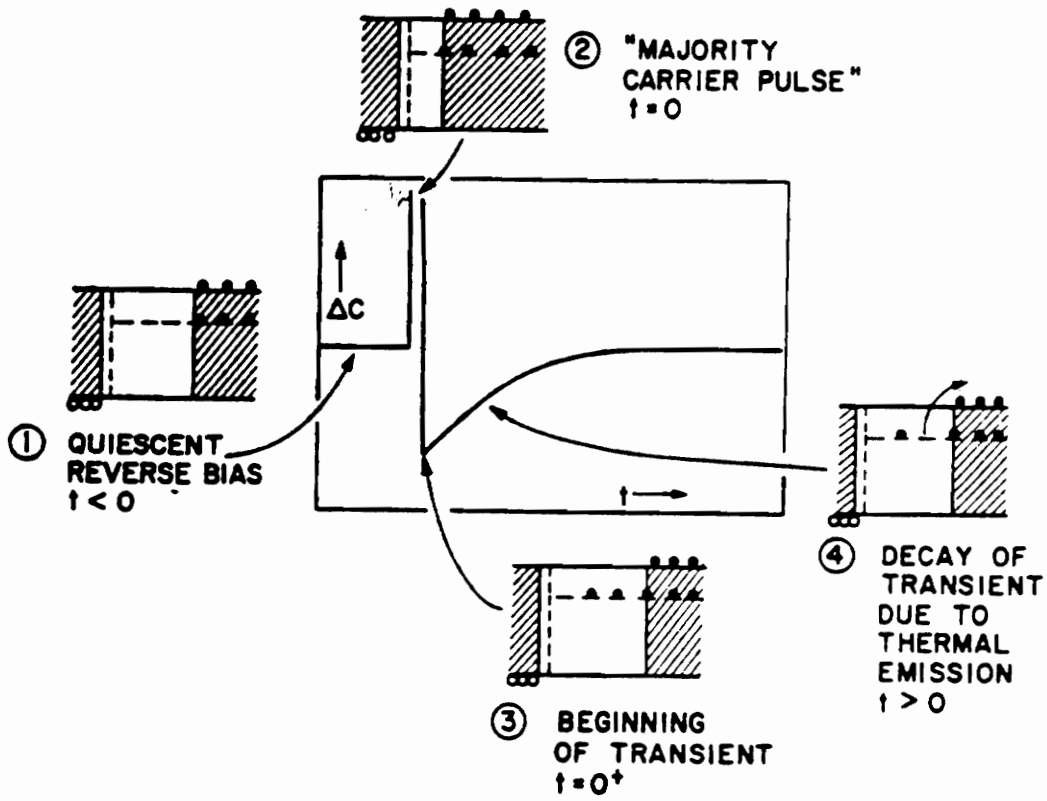
which can also be obtained by using equations (2.2) and (2.4).

2.4 Principle of DLTS

DLTS (Deep Level Transient Spectroscopy) is a widely used technique to detect and characterize defects in semiconductors [153]. The basic idea underlying DLTS operation is the assumption that once a trap level is filled, for example by a voltage pulse of specific duration, the trap level occupancy will decay exponentially immediately after the end of the pulse period. An exponential decay function is assumed because of the dominance of the thermal emission rate of free carriers (e_n) over the capture rate (c_n) i.e. $e_n >> c_n$. The capture and emission processes associated with a majority carrier trap and the corresponding changes in the diode capacitance with time are schematically shown in Fig. 2.4.

Majority and minority carrier traps in the depletion region of a reverse biased Schottky barrier on n-GaAs can be filled by a bias or optical pulse of a fixed duration, respectively. The pulse bias contracts the depletion layer, making free charge carriers available for recombination processes. The time available for these processes is just the pulse period, while the spatial location in which the recombination can take place is the region through which the depletion layer is moved by the pulse. In the optically pulsed DLTS technique, the traps are filled by a pulse of sub-band gap light [156].

The activation energy and thermal capture cross-section of various traps are determined from



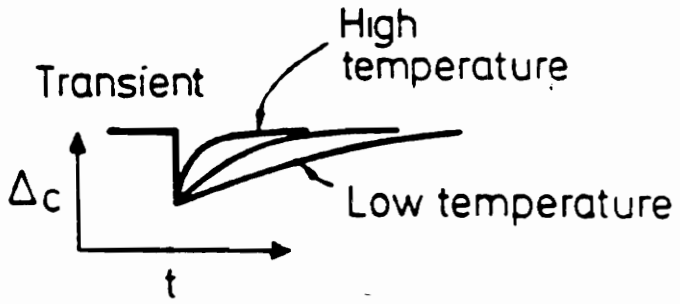


Fig. 2.4 Electron capture and emission processes due to a majority carrier pulse and the corresponding changes in depletion layer capacitance with time (from Ref. [153]).

the measured thermal carrier emission rates at several fixed temperatures. Using the principle of detailed balance, emission rates for hole traps (e_p) vary with temperature according to

$$e_p = \gamma_p T^2 \sigma_p \exp(-E_a/kT) \qquad (2.19)$$

where σ_p is the hole capture cross-section (assumed to be temperature independent), E_a is the hole trap activation energy ($E_a = E_T - E_V$), T is the temperature, k is the Boltzmann constant, and γ_p is a constant containing all temperature independent factors, being 1.7 x 10^{21} $cm^{-2}s^{-1}K^{-2}$ for GaAs. For electron traps, emission rates (e_n) vary as

$$e_n = \gamma_n T^2 \sigma_n \exp(-E_a/kT) \qquad (2.20)$$

where σ_n is the electron capture cross-section (assumed temperature independent), E_a is the electron trap activation energy ($E_a = E_C - E_T$), and γ_n is 2.28 x 10^{20} $cm^{-2}s^{-1}K^{-2}$ for GaAs. On removal of the bias pulse, the traps empty out exponentially as a function of time and can be expressed as

$$N_T(t) = N_T(0) \exp(e_n/kT) \qquad (2.21)$$

where $N_T(t)$ is the concentration of ionized traps at time t, after the pulse removal, with emission rate e_n at temperature T, and $N_T(0)$ is the total trap concentration in the depletion region that was filled by the pulse bias. For hole traps, the same equation holds with the appropriate changes in the subscripts. If the trap concentration N_T (=$N_T(0)$ assumed) is much less than the shallow dopant density (N_D), then the junction capacitance, after the removal of the bias pulse, will vary with time according to

$$C(t) = C_0\{1 + \frac{N_T}{2N_D}[1 - \exp(-e_n t)]\} \qquad (2.22)$$

where C_0 is the steady state capacitance of the diode at a particular reverse bias.

Peaks occur in the DLTS spectrum when the emission rate of carriers from the trap corresponds to the "rate window" set by the chosen delay times t_1 and t_2. At the peak temperature, the emission rate of the trap is given by the value of the rate window and can be obtained using the following relationship

$$e_n = [\ln(\frac{t_1}{t_2})]\,[t_1 - t_2]^{-1} \qquad (2.23)$$

By plotting spectra of different rate windows and monitoring the peak positions i.e. knowing how the emission rate of a trap level will vary with temperature, the activation energy and capture cross section, which together determine the signature for each trap, can be determined. A standard means of characterizing the trap energy level is often to construct a plot of ln (e_n/T^2) vs 1/T, determine its slope and make use of equations of equations (2.19) or (2.20), depending upon the nature of the trap. The trap capture cross-section σ_n can be inferred from the intercept value on the $\ln(e_n/T^2)$ axis. A simpler and approximate method is to assume the prefactor in equation (2.18) to be 10^{12} sec^{-1} (for electron traps) and solving for the activation energy (E_a) by knowing the DLTS peak temperature at a predetermined rate window [32]. Since E_a depends logarithmically on the prefactor, the resulting value of E_a will be within ± 10 % of the true value.

The DLTS signal, $\Delta C(t)$, corresponding to the sampling time t_1 and t_2 is given by

$$\Delta C(t) = C(t_1) - C(t_2) = \epsilon A\{[\frac{1}{W(t_1)}] - [\frac{1}{W(t_2)}]\} \qquad (2.24)$$

where ϵ is the semiconductor permittivity, A the diode or junction area, and $W(t_1)$ and $W(t_2)$ are the depletion widths at delay times t_1 and t_2 (or box-car integrator times), used to define the rate window. The sign of the DLTS peak indicates whether the deep level is a majority or a minority carrier trap; its position on temperature axis determines the energy level and the magnitude of the transient (or the peak height) is proportional to the trap concentration. The presence of a minority carrier trap

can be detected using either a p-n junction device (making minority carrier injection possible) or by using an optical pulse to cause changes in trap population. Combining equations (2.22) and (2.24), the intensity of the DLTS signal $\Delta C(t)$, which is also dependent on rate window, can be related to the trap concentration N_T as

$$N_T = \frac{2\Delta C(t)}{C_0} \frac{N_D}{[\exp(-e_n t_1) - \exp(-e_n t_2)]} \qquad (2.25)$$

2.4.1 Limitations

Parameters extracted from DLTS measurements are based on the assumption of exponential capacitance transients. A number of mechanisms can result in non-exponential transients: electric-field dependent emission rate of trapped charge, trap density being comparable to the net shallow dopant density, multi-exponential decay due to several trap levels with similar emission rate, and non-abrupt junctions, where the free carrier tail extending from the quasi-neutral region into the space charge region can give rise to capture [158, 159].

The trap emission rates may depend on the electric field which varies through the depletion region and results in a continuous distribution of time constants. Lang and Henry have found that the emission rates of traps near the metallurgical junction is higher (because of higher field) than those near the edge of the depletion region [154]. Li and Wang have proposed a new reverse-bias pulsed deep level transient spectroscopy (RDLTS) technique to investigate the electric field effect of carrier emission from deep level centers [157]. A double correlation DLTS (DDLTS) technique, an extension of Lang's DLTS, has been proposed to be effective in smearing out the field dependence of emission rate of traps in the space charge region [155].

Several authors have analyzed the non-exponential capacitance transients arising out of high trap densities [163-165]. The only guarantee for an exponential transient is small trap density i.e. the ratio $N_T/N_D < 0.1$. Many times a non-exponential behavior results when more than one defect level

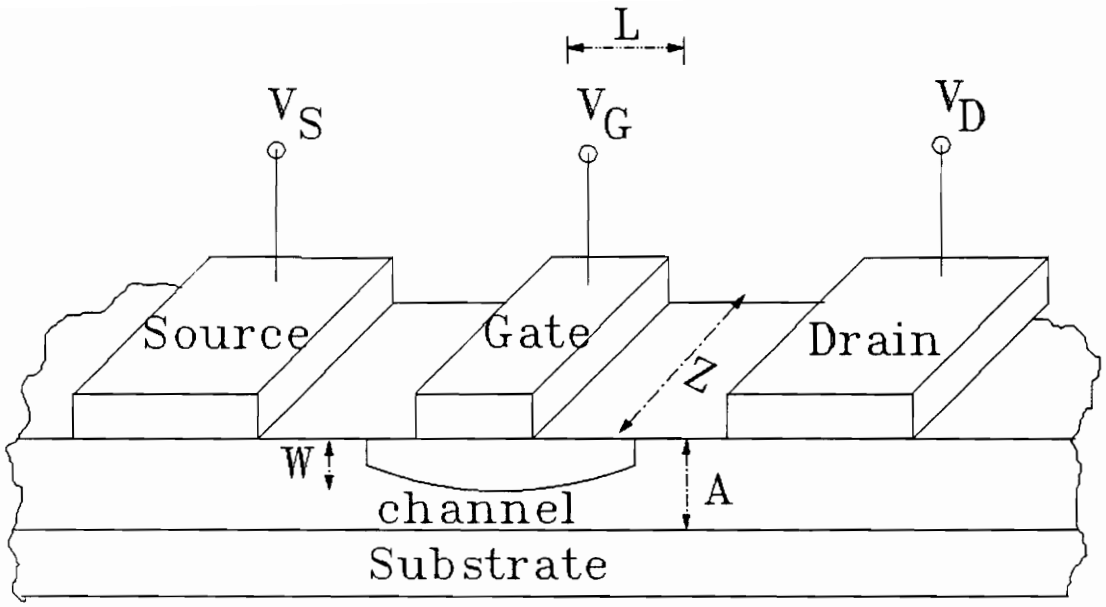
(probably closely spaced) contributes to the transient [160]. Each defect has its own emission rate with its characteristic transient. For closely spaced trap states, the DLTS signal has a shoulder or hump, or even a single broadened peak. In these cases the evaluation of the trap parameters becomes very involved [161]. The difficulty associated with these non-exponential transients may be possibly overcome by adopting the constant capacitance technique to obtain the exponential transients of the voltage change required to preserve a constant depletion layer width and hence a constant capacitance [166, 167].

The effect of diode leakage current on DLTS measurements has been investigated, and it has been shown that leakage current causes carrier capture which competes with the thermal emission to change the trap occupancy [162]. If the leakage current is not corrected, it can lead to misinterpretation of DLTS results. The DLTS results can also be severely affected by a high diode dissipation factor [168]. A high diode series resistance i.e. a high dissipation factor (close to unity) will strongly reduce the DLTS signal and in the extreme case may even reverse its sign [168]. If this happens, then the validity of the DLTS results are questionable.

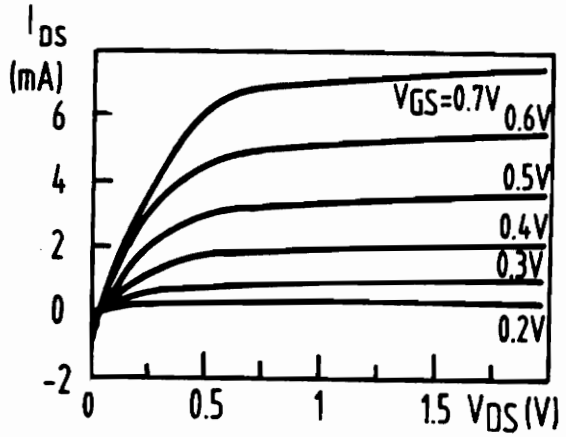
2.5 GaAs MESFET

The MESFET (MEtal Semiconductor Field Effect Transistor) forms the basis for the GaAs monolithic circuit technologies. This section will cover the generic description of MESFET, and the definition of some of the MESFET parameters that are discussed in the later chapters. The GaAs MESFET uses the depletion layer under the gate electrode to modify the depth of an n-channel and thereby affecting the drain to source current (I_{DS}) in the device. A schematic cross section of a MESFET is shown in Fig. 2.5a. Usually the source of the FET is made the common or the ground terminal and a positive potential is applied at the drain terminal.

The steady state current I_{DS} depends on the gate voltage (V_{GS}) and the voltage V_{DS}, applied to the drain. A typical dc characteristic of a MESFET is shown in Fig. 2.5b, where I_{DS} is plotted against V_{DS} at different gate biases (V_{GS}). It is evident from the figure that there are two regions of



a)



b)

Fig. 2.5 a) Cross-sectional schematic of a MESFET and b) a typical I-V characteristics of a MESFET.

operations of a MESFET. At low drain voltages, the channel current increases linearly with the drain bias and is called the linear region of operation, where the electron velocity is $v_d = \mu E$, E being the electric field and μ the mobility (see Fig. 2.6(i)). At a certain value of drain voltage, V_{DSAT}, the electric field in the channel reaches a threshold electric field at which the electron velocity reaches the maximum (v_s). Beyond this threshold field the mobility saturates and so does the velocity (v_s) (see Fig. 2.6(i)). Therefore, at drain voltages above V_{DS}, the channel current remains constant. This is called the saturation region of the I-V characteristics. The MESFET devices mostly operate in the saturation region where the electron mobility ($\mu = \mu_s$) is independent of the electric field.

The steady state I_{DS}-V_{DS}-V_{GS} characteristics for a uniformly doped channel have been derived by Schokley [169]. For a non uniform doping profile $N_D(y)$ (distribution of dopant concentration in the direction normal to the channel) the channel current is expressed as [170]

$$I_{DS} = qv_d Z \int_W^A N_D(y)\, dy \qquad (2.26)$$

where Z is the gate width, A, the channel thickness, W, the depletion layer width, and v_d the electron drift velocity. For the linear region of operation, $v_d = \mu V_{DS}/L$, where L is the gate length, and in the saturation region of FET $v_d = v_s$. The depletion layer width (W) is related to the gate voltage (V_{GS}) in the following way

$$V_{bi} - V_{GS} = \left(\frac{q}{\epsilon}\right) \int_0^W N_D(y)\, y dy \qquad (2.27)$$

If the gate bias is such that it extends the depletion layer completely across the channel thickness then the electron flow in the channel is pinched off and the channel current I_{DS} vanishes. The pinch-off voltage (V_p) across a fully depleted n-layer is given by

The threshold voltage (V_T) is defined as the applied gate bias at which the depletion layer just pinches off the channel. The threshold voltage and pinch off voltage differ by the built-in potential and has

$$V_p = \frac{q}{\epsilon}\int_0^{\infty} N_D(y)\, y dy \qquad (2.28)$$

the relationship

$$V_T = V_{bi} - V_p \qquad (2.29)$$

MESFETs with positive threshold voltage are normally off and they operate in the enhancement mode, requiring positive V_{GS} ($>V_T$) to make the channel conducting (ON). The transistors with negative threshold voltage operate in the depletion mode requiring a negative V_{GS} ($<V_T$) to make the channel non-conducting (OFF).

A very important characteristic of a FET is the transconductance (g_m) defined as

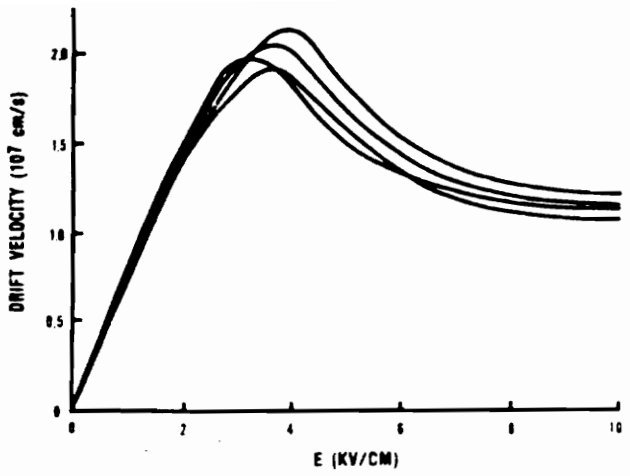
$$g_m = \left[\frac{\partial I_{DS}}{\partial V_{GS}}\right]_{V_{DS}-const} = \frac{\epsilon v_d Z}{W} \qquad (2.30)$$

where the symbols have their usual meaning. The measured transconductance (g_{me}) is dependent on the parasitic source resistance (R_s) and is related to the intrinsic transconductance (g_m as in (2.30)) by

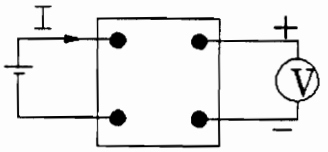
$$g_{me} = \frac{g_m}{1+g_m R_s} \qquad (2.31)$$

It is obvious that the source resistance (R_s) can drastically reduce the gain of the device. The output conductance of a FET (g_{ds}) for $V_{DS} \geq V_{DSAT}$ is defined as

$$g_{ds} = \left[\frac{\partial I_{DS}}{\partial V_{DS}}\right]_{V_{GS}-const} \qquad (2.32)$$

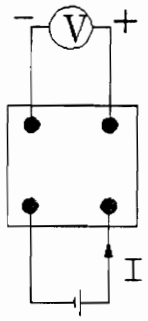


i)



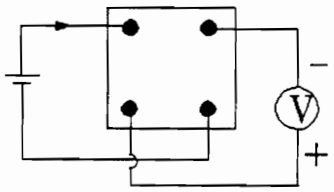
Cable Layout 1

(a)



Cable Layout 2

(b)



Cable Layout 3

(c)

ii)

Fig. 2.6 i) Electron drift velocity in GaAs as function of electric field at 300 K [189] and ii) sample connections for a van der Pauw measurement [190].

The output conductance affects the maximum available gain of a FET, and ideally should be zero. Another important parameter of a FET is the cut-off frequency (f_T), the frequency at which the current gain of the intrinsic FET is unity (i.e $|i_G| = |i_D|$), and is expressed as

$$f_T = \frac{1}{2\pi\tau} = \frac{g_m}{2\pi C_{gs}} = \frac{v_s}{2\pi L} \qquad (2.33)$$

where C_{gs} is the gate-source capacitance and τ is the transit time for electrons at their saturated velocity to move across the gate length. It is evident that for high frequency operation, the MESFET should have a high cut-off frequency. The noise performance of a FET may be quantified by the noise figure (NF), which is a function of frequency, FET bias voltage, and impedance matching. The noise figure is defined by

$$NF = \frac{(signal\ /\ noise)_{input}}{(signal\ /\ noise)_{output}}$$

The above mentioned FET parameters will be appropriately discussed in the subsequent chapters. The correlation between the materials characteristics and the FET parameters will be addressed at length.

2.6 Transport Characteristics

Hall-effect measurement techniques enable the determination of carrier mobilities and concentrations in semiconductors. Under some circumstances, especially in the case of an ion-implanted layer or thin films, it is not convenient to use a bar shaped sample needed for the Hall measurement. The van der Pauw technique, which requires four arbitrary contacts located anywhere on the periphery of a uniformly thick sample of arbitrary shape, offers an appropriate solution [171]. For the van der Pauw method to be valid, the ohmic contact size should be very small and located very close to the sample periphery. The sample must also be singly connected i.e. there should not be any isolated holes. It is necessary in this technique to measure across different pairs of contacts

to correct for the geometry and therefore interchanging the current and voltage leads for various configurations as shown in Fig. 2.6(ii). The sample resistivity (ρ_{av}) is expressed as

$$\rho_{av} = \frac{\pi t}{\ln 2} \left(\frac{R_a + R_b}{2}\right) f\left(\frac{R_a}{R_b}\right) \qquad (2.34)$$

where R_a (= (V1-V2)/I) is the resistance in position (a) of Fig. 2.6(ii), R_b is defined in the same way for position (b), t is the sample thickness (for implanted sample it is the implant layer thickness), and f (R_a/R_b) is a function dependent on the ratio of R_a and R_b [171]. The average Hall mobility can be determined by measuring the change of the resistance, with or without a magnetic field, in position (c) and is given by

$$\mu_{av} = 10^8 \left(\frac{\Delta R_c t}{B \rho_{av}}\right) \qquad (2.35)$$

where B is the value of the magnetic field in gauss applied perpendicular to the sample. The average carrier concentration (n_{av}) is then calculated using the following relationship

$$n_{av} = \frac{r_H}{q \rho_{av} \mu_{av}} \approx \frac{1}{q \rho_{av} \mu_{av}} \quad (for \ \ r_H = 1) \qquad (2.36)$$

where q is the electronic charge and r_H is the Hall factor and is the ratio of the Hall mobility to the drift mobility . The value of r_H depends on scattering mechanisms and impurity concentration and for practical purposes, its value is close to unity for electrons.

2.6.1 Transport Profile

The interpretation of the Hall effect measurement becomes difficult in the case of implanted samples since in such samples both the mobility and the carrier concentration vary with depth. Hall effect measurements on implanted samples would yield weighted averages of the resistivity, mobility, and carrier concentration, by using equations (2.34), (2.35), and (2.36), respectively. In the case of Hall measurements on implanted samples, it is necessary that the current passing through the sample

be confined to the implanted layer.

Assuming the Hall factor (r_H) to be unity and neglecting all contact resistances, the depth dependent Hall mobility, $\mu(y)$, is related to the average Hall mobility (μ_{av}) given by

$$\mu_{av} = \frac{\int_{\lambda_d}^{A} \sigma(y)\,\mu(y)\,dy}{\int_{\lambda_d}^{A} \sigma(y)\,dy} \qquad (2.37)$$

where A is the thickness of the conducting (active) layer, $\sigma(y)$ is the conductivity at location y, and λ_d is the surface depletion depth and is represented by the characteristic Debye length as given by equation (2.6). Similarly, the relationship between the apparent carrier concentration (n_{av}) and the depth dependent carrier concentration, n(y), is expressed as

$$n_{av} = \frac{1}{A}\frac{\left[\int_{\lambda_d}^{A} n(y)\,\mu(y)\,dy\right]^2}{\int_{\lambda_d}^{A} \mu(y)^2 n(y)\,dy} \qquad (2.38)$$

Both μ_{av} and n_{av} are the values obtained through the Hall-effect by considering the sample to be homogeneous.

The experimental procedure of depth profiling consists of sequentially removing thin layers of the implanted section and re-measuring resistivity and mobility by using equations (2.34) and (2.35). This cycle is repeated until most of the implanted layer has been removed. The most direct chemical method of removing successive layers in GaAs is to etch the sample for a fixed interval of time. An oxidizing etchant of 1:1:100 (by vol) of concentrated H_2SO_4 : 30% H_2O_2 : H_2O give a GaAs etch rate of approximately 600 Å min^{-1} [73,74]. The resistivity (ρ_n) and mobility (μ_n) values of the sample at the n^{th} layer can be determined by knowing the average resistivities and average mobilities

after two successive layer removals and by using the following relationships [172]

$$\rho_n = \frac{\Delta d}{\frac{d_{n+1}}{\rho_{n+1(avg)}} - \frac{d_n}{\rho_{n(avg)}}} \qquad (2.39)$$

and

$$\mu_n = \frac{\frac{\mu_{n+1(avg)} d_{n+1}}{\rho_{n+1(avg)}} - \frac{\mu_{n(avg)} d_n}{\rho_{n(avg)}}}{\frac{d_{n+1}}{\rho_{n+1(avg)}} - \frac{d_{n(avg)}}{\rho_{n(avg)}}} \qquad (2.40)$$

where $\rho_{n(avg)}$ and $\mu_{n(avg)}$ are the average resistivity and mobility after the removal of the n^{th} layer, respectively, and Δd ($= d_{n+1} - d_n$) is the thickness of the layer etched away. The carrier concentration (n_n) in the n^{th} layer may be evaluated as

$$n_n = \frac{1}{q\rho_n\mu_n} \qquad (2.41)$$

In concluding this chapter it is appropriate to emphasize that the theoretical concepts and background material discussed so far form the basis of deriving almost all the results of this research, presented and discussed in Chapter 5.

CHAPTER 3. LITERATURE REVIEW

This chapter deals with a review of the vast amount of research conducted on GaAs so far; more specifically, the review is focused on the effects of ion implantation, annealing, substrate and buffer layers on electrical properties of GaAs. The gist of the research results on defect characteristics of GaAs, both process and substrate induced, will be presented. Since almost all of the current research involves ion implantation and annealing processes on either semi-insulating (SI) or molecular beam epitaxy (MBE) grown GaAs, a major thrust will be on reviewing the available literature concerning these materials. The chapter is divided into different sections. First the various issues on GaAs substrate material are discussed. This is followed by a review of the available literature on ion implantation and annealing studies. The reported results on defects in GaAs and their impact on device performance are discussed next, followed by a review on the studies of high energy (MeV) implantation into GaAs. The chapter is concluded by reviewing the published results on the characteristics of MBE GaAs layer and buffer layers (low temperature MBE GaAs and AlGaAs) and their effects on device behavior.

3.1 Substrate

The quality of GaAs substrates very often limits the quality of the implanted layer subsequently formed with it. It is a technological problem to produce GaAs wafers with identical electrical properties on a routine production basis due to their severe sensitivity to the background impurities introduced during growth. Often the background defects and impurities in the substrate mask the defects that are induced due to ion implantation and subsequent processes. To obtain desirable doping properties of the ion-implanted and annealed GaAs, the substrate should conform to the following requirements :

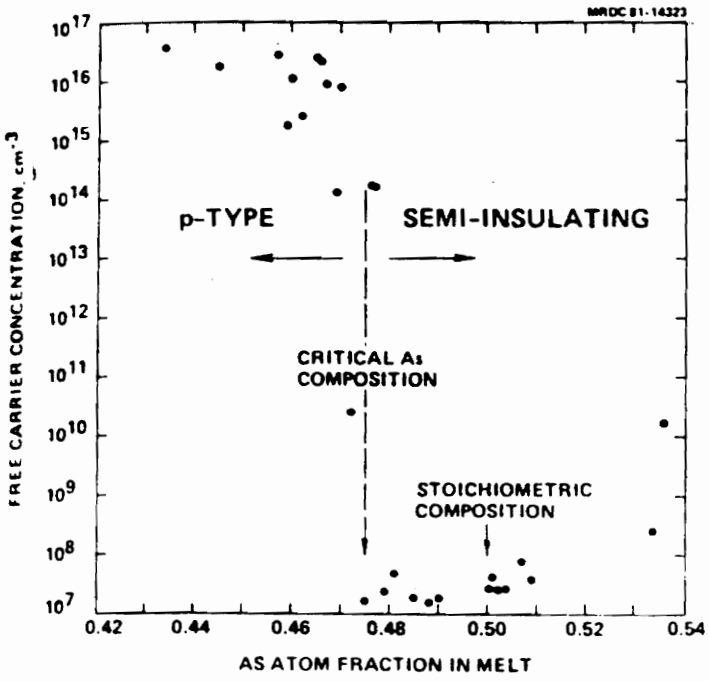
1. High resistivity and thermally stable to permit fabrication of planar, isolated active regions

without etching ($\rho > 10^7$ Ω-cm).

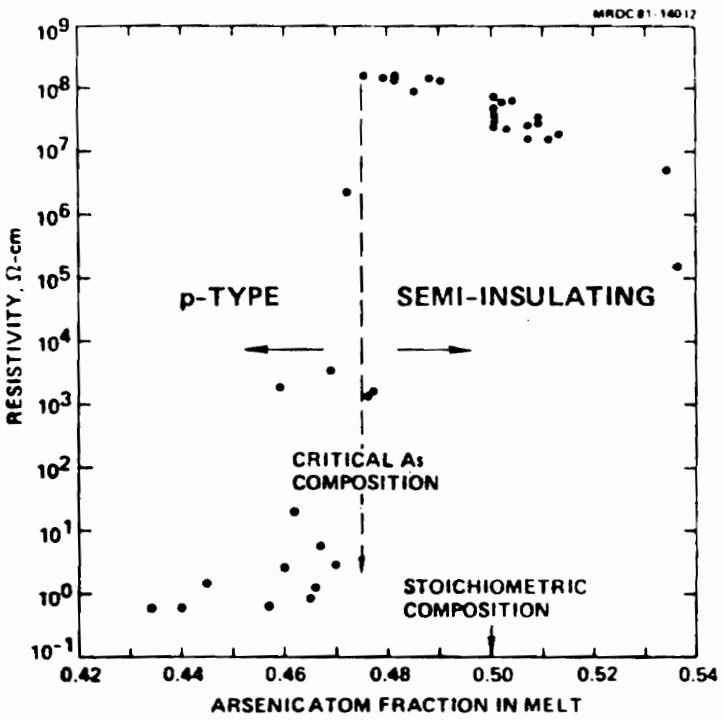
2. Low background doping with respect to shallow donor and acceptor impurities.
3. Free from crystalline defects such as stacking faults, inclusions, precipitates, twins, and low angle grain boundaries. Substrates with dislocation densities $< 10^5$ cm^{-2} are acceptable for implantation and device fabrication.
4. Large and regular size wafer shapes for permitting high device yield.

Melt composition is a key parameter in the crystal growth of GaAs as it strongly affects the concentration of deep levels and consequently the semi-insulating nature of GaAs substrates. Fornari *et al.* [59] have reported that with increasing Ga/As ratio in the melt, the concentration of electron traps EL2, EL5, and EL6 decreases as do the concentrations of defects such as V_{Ga} and As_{Ga}. The free carrier concentration in undoped LEC (liquid encapsulated Czochralski) GaAs is controlled by the balance between EL2 deep donors and carbon shallow acceptors [62]. Semi-insulating GaAs can be grown only from melts above a critical As composition as shown in Fig. 3.1a. All methods of LEC growth of GaAs favor As-rich growth and therefore the basic defects entering the complexes responsible for most of the deep levels in GaAs are either the Ga-vacancy (V_{Ga}) or the As-interstitial (As_i) or both.

The GaAs crystals grown from an As-rich melt exhibit higher electron mobility than those grown under Ga-rich conditions [58]. However, crystals grown under Ga rich condition are p-type with lower resistivity (refer to Fig. 3.1b) and fewer dislocations. Such dislocation reduction is explained in terms of reduction of point defects (As-interstitial), which are known to enhance expansion of microloops and form microprecipitates along dislocations [58]. The p-type conductivity in LEC GaAs grown from Ga-rich melt is believed to be due to an acceptor-like antisite Ga_{As} defect [59]. EL2 plays a dominant role in the compensation mechanism of undoped LEC grown GaAs [77]. It has been shown that the shallow acceptors (mostly due to C from the pyrolytic boron nitride crucible) and shallow donors (mostly due to Si pick-up from the quartz crucible) are compensated by the deep donor EL2 and the deep acceptor related to Cr, respectively [75]. Lagowski *et al.* have



a)



b)

Fig. 3.1 **Effect of melt stoichiometry of LEC GaAs on** a) free carrier concentration and b) electrical resistivity [62].

attributed EL2 to antisite defect (As_{Ga}) formed during post-growth cooling as per the following reaction [78] :

$$As_{Ga}^{x} + V_{Ga}^{-} = As_{Ga}^{++} + V_{As}^{+} + 4e^{-}$$

where As_{Ga}^{x} is neutral As on a Ga site, V_{Ga}^{-} is an ionized Ga vacancy, As_{Ga}^{++} is the ionized antisite defect, e^{-} the electron, and V_{As}^{+} is an ionized As vacancy. In contrast to the behavior of EL2 in the undoped SI GaAs, the EL2 concentration in the doped crystals is suppressed at a high free electron concentration of about $1x10^{17}$ cm^{-3} and above [79]. The radial distribution of EL2 in an undoped LEC GaAs wafer follows a W-shaped pattern but the profile becomes M shaped in crystals doped above the threshold concentration.

The excess EL2 in LEC grown undoped GaAs over shallow acceptors (carbon) pins the Fermi level to the middle of the band gap resulting in a semi-insulating material. In HB (Horizontal Bridgman) grown GaAs, an excess of background shallow donors over shallow acceptors is usually present, so that the deep acceptor Cr is normally added to pin the Fermi level to mid-gap for obtaining SI material. Yeo *et al.* have made a detailed comparison of low dose Si implants into undoped LEC and Bridgman grown Cr-doped GaAs substrates [76]. They report an activation efficiency of 90%, after annealing, for both substrates, however, mobilities are much better and electrically active layers much deeper in the undoped than the Cr-doped substrates. Similar observations have also been reported by Hickmott [83].

3.2 Ion Implantation

Ion implantation is the most attractive technique for the formation of small dimension channels or contact regions for integrated circuit applications. This is especially the case for GaAs where the diffusion-technology is practically non-existent. There are no impurities for GaAs, with the possible exception of Zn, that have the desired diffusion coefficient to cause significant diffusion of

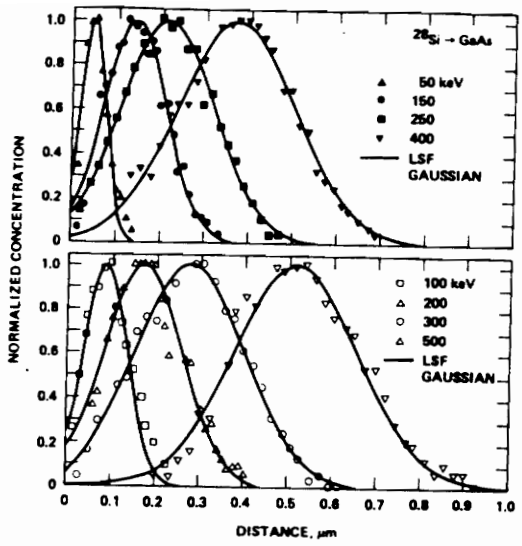
dopants at feasible processing temperatures. Therefore, implantation is a more suitable technology for GaAs based devices. Ion implantation in GaAs can introduce dopants, that are not easily diffused, at relatively low temperatures, with a fairly good control on dopant concentration and its distribution. A direct ion implantation technology, yielding uniform and reproducible doping characteristics across each substrate is highly desired for GaAs IC processing.

When incident ions impinge on the target, the majority penetrate some distance and slow down by the random interaction with the nuclei and electrons of the target. The depth of penetration is a function of ion energy, mass, and the atomic number of both ion and target atoms. Predictions on the depth distribution of the implanted atoms (N(x)) are possible for amorphous targets and is given by the LSS theory as [20] :

$$N(x) = N_0 \exp[-(x-R_p)^2 / 2\Delta R_p^2] \qquad (3.1)$$

where N_0 is the implant dose, R_p, the projected range and ΔR_p, the standard deviation signifying the spread in the profile. Fig. 3.2a [23] shows a typical Si depth distribution in GaAs, as measured by SIMS, for various energies of implantation. The profiles are normalized to the maximum of the solid lines which are Gaussian, fitted to the data by least square methods. R_p and ΔR_p computed from the fitted data are shown in Fig. 3.2b as a function of ion energy. The theoretical values of R_p and ΔR_p computed from the LSS theory are also shown in the figure (solid lines). Over the ion energy shown, the agreement between the LSS theory and the experimental Gaussian fit is within 10% for R_p and within 20% for ΔR_p [23]. Extensive tables of average projected range and its standard deviation for ions implanted into GaAs for device applications are well documented [21].

In crystalline targets however, the implanted atom distribution is dependent on the substrate orientation during implantation. If the incident ion-beam is within a critical angle to a major crystal axis, the ions will be steered down in the open direction of the lattice, consequently the implant depth will be far greater than that predicted by the LSS theory for amorphous targets. This phenomenon is known as ion channeling and causes irreproducibility in dopant profiles and consequently the



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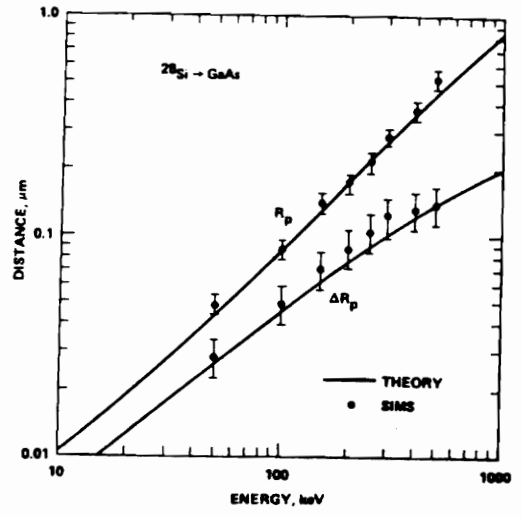

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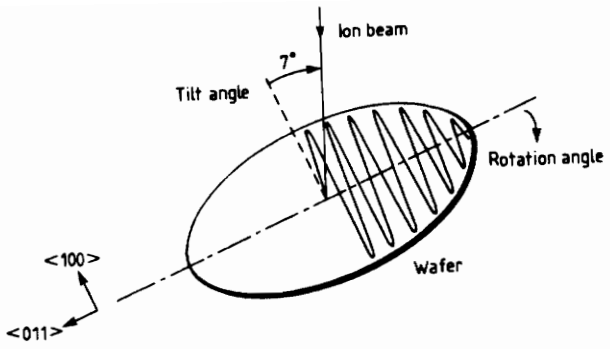
Fig. 3.2 Si implantaion into GaAs at various ion energies a) Si atomic profiles by SIMS and Gaussian curves least-square fitted to the data and b) projected range statistics (R_p and ΔR_p) (from Ref. [23]).

electrical properties. To minimize ion channeling, the crystal is usually misaligned (typically 7° away from the ion beam) during implantation and made to appear like an amorphous target to the ion-beam (Fig. 3.3a). Tabatabaie-Alavi and Smith have modeled Si-implantation profiles for a wide range of ion energies and doses together with the effect of a 500 Å thick SiN implantation cap [112]. They observed that at energies below 125 keV, the through-nitride implants have less straggle than the direct implants and at energies above 150 keV, the profiles with and without the use of SiN implant-cap are very similar.

3.2.1 Ion Implantation Damage

During implantation, target atoms are displaced from their lattice position due to collisions with incident ions. If the total damage energy integrated over all displacements exceeds a critical value, the region turns amorphous [114]. For a sufficiently energetic ion beam, cascades of displacements, and hence zones of amorphization may result as is schematically depicted in Fig. 3.3b [22,141]. In the case of high ion doses these amorphous zones may overlap and cause substantial crystal disorder. When ion energy is below the critical value of specific damage energy, displaced atoms result in simple and complex point defects which may cluster to form dislocation loops [114].

Ion implantation into GaAs leads to the formation of As and Ga vacancies in regions up to the projected range and excess atoms beyond this. Defects resulting from damage production usually compensate the electrical activity of the implanted ions. Predominantly electron traps are formed in irradiated and implanted GaAs [18]. The amount of ion damage to GaAs is a function of the mass, energy, and dose of implanting ions and also the substrate temperature. These parameters also determine if the damage consists of isolated defect clusters or amorphous layers (buried or continuous) [19]. Although Si implantation into Cr-doped and undoped LEC GaAs is Gaussian, the donor concentration after annealing is nearly constant over much of the ion-range; however, there is a transition region at the end of the implanted ion-range, where the dopant concentration drops appreciably and the properties of the semi-insulating substrate dictate the electrical behavior of the



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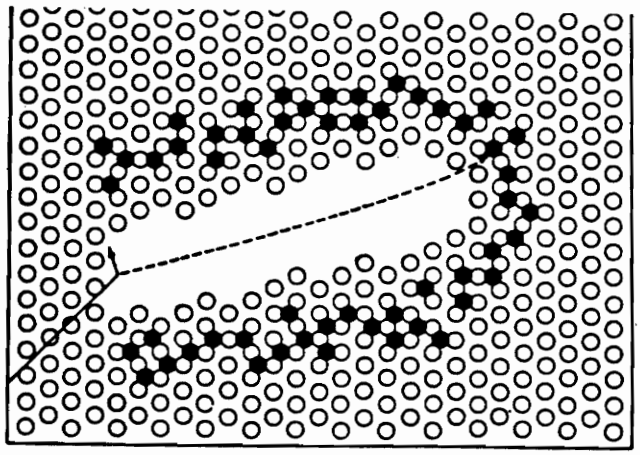


b)

Fig. 3.3 Schematic illustrations of a) ion beam angular tilt to avoid channelling [140] and b) ion-induced damage to crystal lattice [141].

channel [83].

3.3 Annealing

Ion implantation is an attractive technique to introduce dopants in GaAs but results in severe damage to the crystal lattice. Thermal annealing is necessary to reduce ion-damage and cause electrical activation i.e. to provide energy to the implanted ions to move to the appropriate substitutional sites in the crystal lattice. Implantation annealing of GaAs is much more complicated than Si and the problems with the dopant distribution and the loss of As from the wafer surface are well documented [15-17]. At typical annealing temperatures of 800-900 °C , GaAs decomposes due to its congruent evaporation at ~ 630 °C. The surface integrity of GaAs, during annealing, is very critical for device performance. The problem of surface dissociation is overcome by one of the following methods :

1. by annealing in an atmosphere with sufficiently high As partial pressure;
2. by annealing using a dielectric (SiO_2, Si_3N_4 etc.) protective layer on the surface;
3. by using GaAs wafers, as protective caps, in mechanical contact with the sample surface (proximity annealing);
4. by annealing for a time insufficient for significant As loss, rapid thermal annealing (RTA).

In capped annealing, the quality of the encapsulant and its thermal stability influence significantly the yield and reproducibility of the implanted and annealed active GaAs layers. Impurities in the capping layer, strain at the interface, pin-hole porosity, extent of diffusion of Ga into the dielectric cap etc. eventually affect the characteristics of the active layer.

Recrystallization of the amorphous layer in semiconductors occurs by solid state epitaxy (SPE). Regrowth of the amorphous layer in (100) GaAs leaves behind a large amount of disorder as observed by Raman spectroscopy and RBS measurements [19]. TEM results reported by Sadana [19] suggest that the disorder consists primarily of bundles of stacking faults and micro-twins. The annealing of the dislocation loops is determined by their size and concentration, both of which depend critically on implantation parameters the and substrate conditions [114]. The loops, as observed by

TEM, are interstitial in nature [115]. The dislocations provide sites for segregation and trapping of dopants and impurities because of which carrier concentration and mobility are suspected to be degraded. During annealing primary loops coalesce to form larger loops by climb and glide processes, which for a longer anneal time may be lost to the surface depending on the proximity of the defect to surface.

Shigetomi and Matsumori have reported on the optical and electrical properties of 200 keV Si-implanted GaAs, annealed at various temperatures [117]. Their optical absorption data, shown in Fig. 3.4a, indicate that at 400 °C epitaxial reordering of the ion-induced disordered amorphous layer is almost complete but a 800 °C annealing is required for perfect recrystallization. Electrical conduction in the disordered GaAs layer is governed by the hopping-conduction assisted by the localized states. A typical effect of the annealing temperature on the carrier activation and mobility in Si-implanted GaAs at different ion doses is shown in Fig. 3.4b [118].

During annealing a variety of antisite defect complexes of As_{Ga} and Ga_{As} are likely to form and may redistribute and cause compensation effects. It is believed that the dopant-point defect interaction controls the level of electrical activity of GaAs after annealing [14]. Unfortunately, there is evidence that both Cr [109] and EL2 [110] out-diffuse near the surface at temperatures characteristic of the post-implant annealing. The out-diffusion of these deep centers is extremely undesirable as they would strongly modify the free-carrier profile and can cause an adverse effect on device performance. In fact, the deep level movements in SI GaAs during annealing may cause the appearance of a spurious type conversion (n or p), near the surface of the wafer. Makram-Ebeid, *et al.* [110] have shown that the out-diffusion of EL2 to the surface is related to the loss of As, probably assisted by vacancies. The out-diffusion behavior of EL2 is a strong function of the annealing and the capping conditions.

3.3.1 Furnace Annealing

The problems associated with FA are the redistribution of implanted ions, the compensating

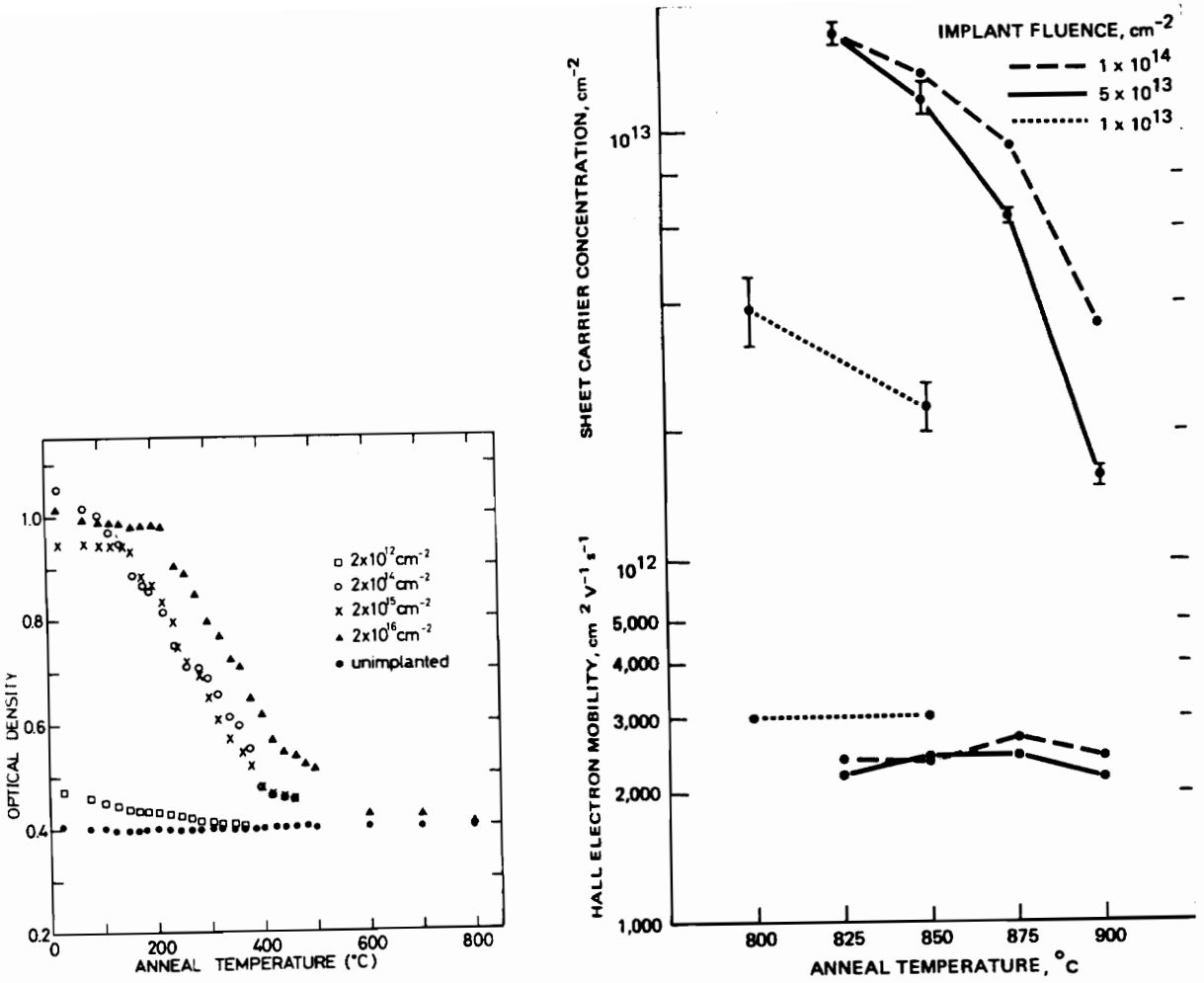


Fig. 3.4. Effects of furnace annealing temperature on Si implanted GaAs on a) optical absorption of photon energy at 1.36 eV (from Ref.[117]) and b) sheet carrier concentration and mobility (from Ref. [118]).

Cr, and EL2 centers [28-29,39-41]. This redistribution results in the lack of controllability and uniformity in device characteristics. Fang *et al.* have investigated the traps in Si-implanted and annealed HB grown GaAs [61]. They indicated that Si-implanted GaAs activated at 825 °C and above contains the same trap species as those in bulk n-GaAs before and after anneal. A comparison between Si-implanted GaAs samples activated by RTA and FA at 850 °C revealed that most of the electron trap densities are smaller in the GaAs sample with FA than in the sample annealed with RTA. The trap levels EL5 (0.37 eV) and EL9 (0.21 eV) appear to have a common connection with EL2 and are speculated to be defect complexes associated with As_{Ga} [61]. Traps EL3 (0.60 eV), EL4 (0.48 eV) and EL2 are likely to show metastable or bistable behavior, and may be responsible for the low frequency noise and hysteresis in the drain current-voltage characteristics of MESFET devices.

In a separate study on the deep level parameters in Si-implanted and furnace annealed GaAs, numerous electron and hole traps were detected using electrical and optical DLTS, and the results are summarized in Table 3.1. Two prominent trapping centers in Si-implanted and furnace annealed (800-850 °C) GaAs are reported : a 0.52 eV electron trap and a 0.15 eV hole trap [64,143]. The presence of the electron trap at E_c-0.53 eV has also been observed by Sriram and Das in a similarly processed GaAs MESFET [65].

Rhee and Bhattacharya have detected deep levels in SI Cr-doped GaAs before and after Si-implantation and furnace annealing [38]. Electron and hole traps with activation energies of 0.52 ± 0.01 eV and 0.15 ± 0.01 eV, respectively, were consistently observed. These traps are attributed to the implantation and annealing processes. The Cr centers resulted in hole emissions with an activation energy of 0.85 ± 0.01 eV.

3.3.2 Rapid Thermal Annealing

Rapid thermal annealing (RTA), also known as Rapid thermal processing (RTP), is suggested as a promising technique for minimizing the dopant and the compensating center redistribution and for achieving high electrical activation of the implanted ions [39]. RTA at 600 °C is effective in

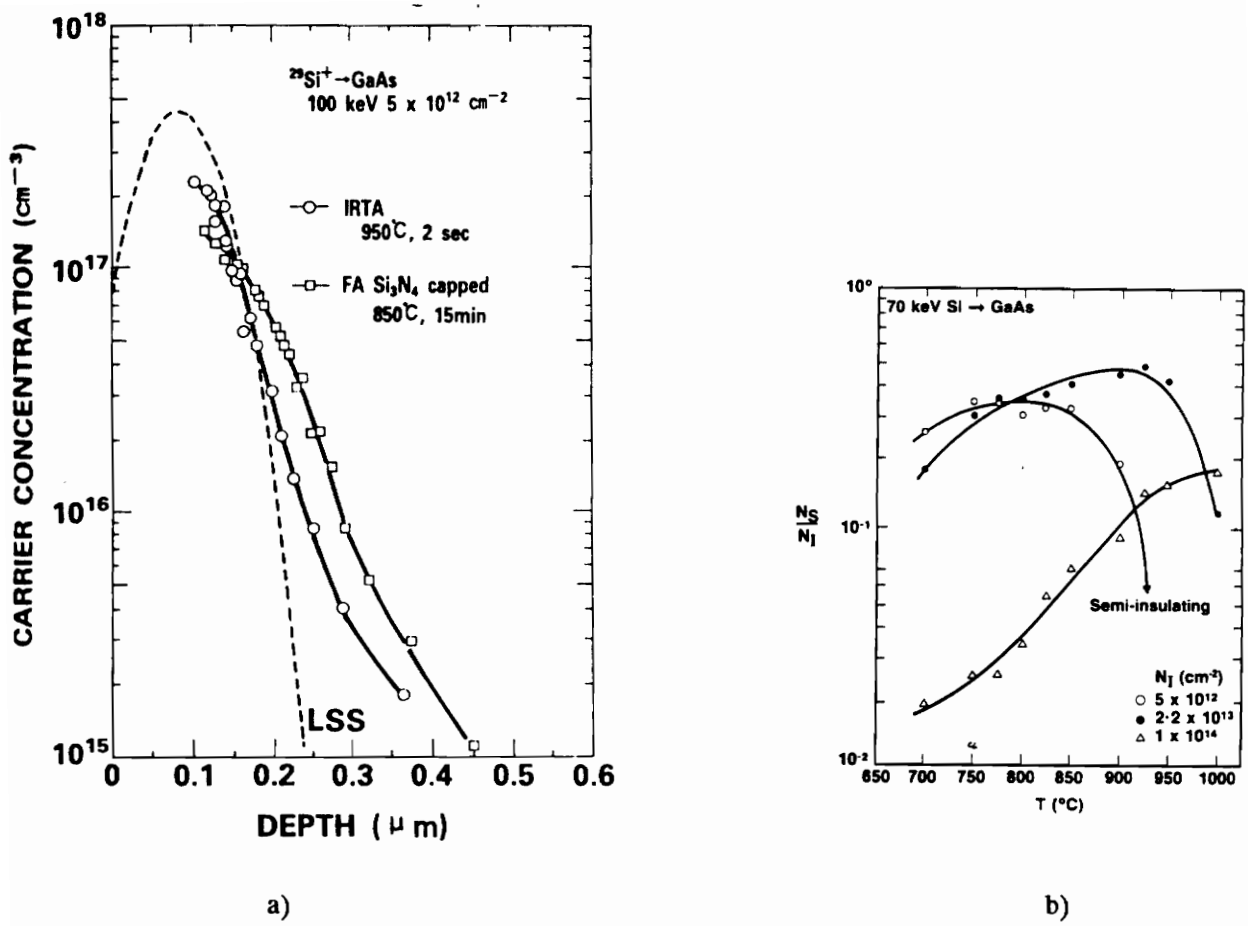
Table 3.1. Commonly observed traps in Si-implanted GaAs and their characteristics [143].

Trap Type	Trap Label	Activation Energy (ΔE_T) 1) (eV)	Capture Cross-Section 2) σ_∞ (cm^{-2})	Usual Occurrence	Possible Identity
Hole traps	A	0.21	1.3×10^{13}	In samples with existing substrate damage	lattice damage
	B	0.27	7.0×10^{-12}	Detected in samples undergoing prolonged post-implant anneal	may be related to Ga vacancies
	C	0.25	6.0×10^{-15}		
	D	0.47	9.6×10^{-10}		
	E	0.43	5.0×10^{-15}	All samples	copper impurity
	F	0.65	1.9×10^{-12}	Most samples	unknown
	G	0.72	2.4×10^{-12}	All samples	native defect
	I	1.10	1.1×10^{-8}	Most samples	unknown
Electron traps	H	0.57	1.4×10^{-15}	All samples	implantation damage
	J	0.82	2.0×10^{-14}	Most samples	EL2, related to Ga vacancy

1) Denotes average value over all samples measured.
2) Determined from the emission rate prefactor.

removing the implantation-induced damage but higher temperatures (600-900 °C) are necessary to anneal out the extended defects [119]. Kohzu and coworkers have applied infrared thermal annealing (IRTA) to activate 100 keV Si-implanted GaAs [42]. The carrier profiles by IRTA are much steeper than those by furnace annealing (FA) and are shown Fig. 3.5a. MESFET characteristics with an active layer formed by IRTA and furnace annealing under Si_3N_4 cap are compared in Table 3.2 and their drain current characteristics are shown in Fig. 3.6. The FETs formed on the active layers made by IRTA showed 30-40 % higher transconductance and lower pinch-off than the FETs made using FA [42]. Tandon *et al.* in the activation analysis of Si-implanted GaAs have noticed that high temperature RTA results in improved activation of high-dose implants but low temperatures are favorable for low-dose implants, as shown in Fig. 3.5b [80]. To understand the electrical activation of implanted dopants, the original electronic properties of the compensated SI GaAs, and changes upon annealing, should be known.

Katayama, *et al.* [30] have studied the effects of RTA on the electron traps in Si-doped LEC GaAs. RTA introduced electron traps ED1 (E_c-0.26 eV), ED2 (E_c-0.49 eV), and ED3 (E_c-0.55 eV) in the GaAs sample. At the same time the traps EL3 (E_c-0.61 eV), EL5 (E_c-0.40 eV), and EL6 (E_c-0.35 eV) that were present in the as-grown sample were not observed after RTP [30]. The RTP related traps are attributed to the production of As interstitial and As vacancies due to large thermal stress induced by the rapid heating in RTP. The EL2 density remains unchanged after RTP and is in contrast with the results reported for furnace processing [29]. This difference in behavior is due to the short-time processing of RTP which prevents out-diffusion of EL2. Although the depth profile of EL2 was flat after RTP, its spatial variation was quite pronounced, being two orders of magnitude higher towards the edge than towards the center of the sample [36]. This is attributed to the thermal stress induced during RTP. The spatial variations of EL2 in MBE GaAs due to FA and RTP are shown in Fig. 3.7a. Kohzu *et al.* have shown that n-type GaAs activated by RTA (100 keV, $5x10^{12}$ cm^{-2} dose) has a higher peak carrier concentration and a steeper carrier concentration profile than the FA GaAs sample [42].



a) b)

Fig. 3.5 a) Comparison of carrier concentration profiles (by C-V) in 100 keV Si-implanted and annealed [42] and b) effects of RTA annealing temperatures on the activation ratio of 70 keV Si-implanted GaAs at various ion doses [80].

Table 3.2. Comparison of GaAs MESFET (1 μm x 300 μm) characteristics on active layers formed by RTA and FA methods

Characteristics	Conditions	RTA	FA
Drain saturation current (mA)	V_{DS} = 3V, V_{GS} = 0V	64.0	64.5
Transconductance (mS)	V_{DS} = 3V, V_{GS} = 0V	34.0	24.0
Pinch-off voltage (V)	V_{DS} = 3V, I_{DS} = 100μA	2.7	3.6
Gate leakage current (nA)	V_{DS} = 0V, V_{GS} = -1V	27.0	26.0
Gate breakdown voltage (V)	V_{DS} = 0V, I_{DS} = 10 μA	10-12	14-18

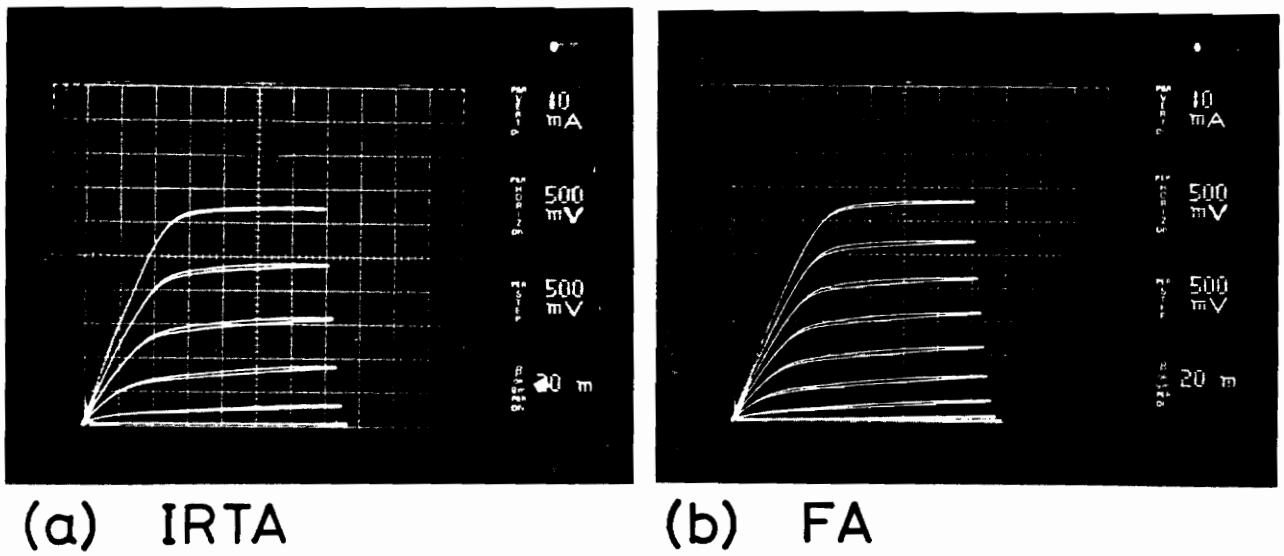
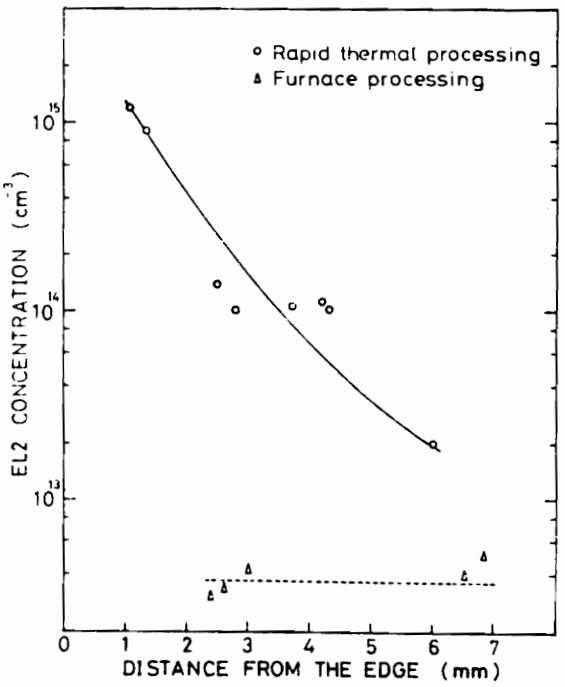


Fig. 3.6 I-V characteristics of GaAs MESFETs a) on IRTA annealed layer and b) on furnace annealed layer [42].



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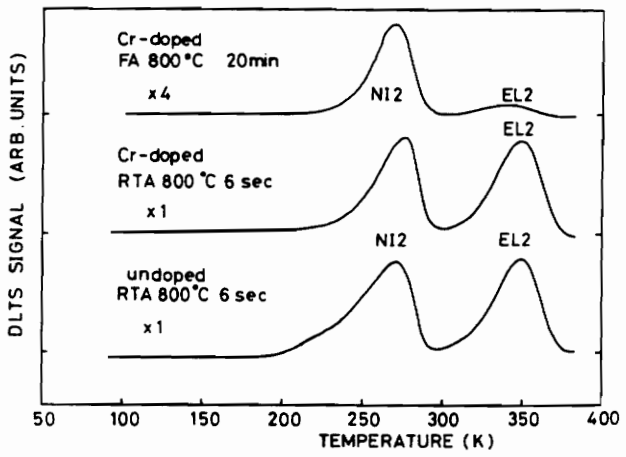


b)

Fig. 3.7 a) Spatial distribution of EL2 in MBE-GaAs due to RTP (800 °C/6 s) and furnace annealing (800 °C/15 min.) [36] and b) DLTS spectra of 250 keV Si-implanted and RTA or furnace annealed GaAs [2].

Dhar and coworkers have investigated the nature and distribution of deep levels in Si-implanted and RTA annealed GaAs [63]. They observed a dominant electron trap, also seen in the furnace annealed samples, at E_c-0.57 eV. The origin of the trap is associated with the implantation damage, possibly related to V_{Ga}. Interestingly, they obtained lower trap densities in RTA samples, compared to that in the equivalent furnace-annealed samples. Kuzuhara and Nozaki have detected the electron traps due to RTA on Si-doped LEC and HB grown GaAs using DLTS [116]. They report an RTA-induced electron trap level at E_c-0.20 eV, possibly because of the rapid heating involved in the RTA process.

Kitagawa and coworkers [2] have investigated the deep levels in Si-implanted (250 keV, $2x10^{13}$ cm^{-2} dose) and RTA undoped and Cr-doped LEC SI GaAs. They report the occurrence of EL4 (E_c-0.55 eV) and EL2 (E_c-0.78 eV) in both types of substrates (undoped and Cr-doped) after RTA at 850 °C and above (refer to Fig. 3.7b). The EL4 level is proposed to be created by the association of defects in the original substrate and the implantation-induced damage during the high temperature annealing. The low concentration of EL2 in the spectrum of the furnace-annealed sample is due to the out-diffusion of EL2 into the SiO_2 encapsulant, during annealing.

3.4 Orientation Effects

Banerjee *et al.* have reported an unusual implanted carrier profile in (211) oriented GaAs [130]. They compared MESFETs formed on Si-implanted and RTA annealed (100) and (211) GaAs surfaces and the results are presented in Table 3.3. The (211) GaAs MESFET has a higher transconductance, a lower noise figure, a higher cut-off frequency and gain than a typical MESFET on (100) GaAs. The improved device performance of (211) GaAs over the conventional orientation of (100) GaAs is attributed to the unique carrier-profile in (211), where the carrier density rises near the surface, remains flat for the most part of the implanted region and falls off rapidly near the tail of the profile. In a separate study, however, Feng *et al.* could not confirm the existence of the unique carrier profile in (211) GaAs [131].

Table 3.3. Comparison of MESFET Parameters on (100) and (211) GaAs [130].

Orientation	NF (dB) at 12 GHz	Gain (dB) at 12 Ghz	f_T (GHz)	g_m (extrinsic) (mS/mm)	g_m (intrinsic) (mS/mm)
(100)	1.50	10.5	31.0	200	263
(211)	0.95	10.0	40.8	280	339
(211)	1.03	11.1	40.1	280	344

Not many studies have been conducted on evaluating the properties of active layers formed on (211) oriented GaAs substrates. Bhattacharya and coworkers have used RBS and TEM to investigate the annealing characteristics of 60 keV Si-implanted (1×10^{15} cm^{-2}) (100) and (211) GaAs surfaces [132]. They observed that the solid state epitaxial regrowth begins at 250 °C, for both orientations, but the damage recovery rate is much slower in (211) GaAs. After annealing at 900 °C for 30 mins. with Si_3N_4 cap, the crystal quality of (100) GaAs recovered to its virgin state but (211) GaAs still had residual damage. The higher resistance to damage annealing in (211) compared to (100) is attributed to the higher rate of development of dislocation tangles and loops in (211) [132].

3.5 Material Defects

Lattice defects in GaAs can be broadly classified as [1] :

i) point defects, such as vacancies, interstitial, and antisite defects

ii) microdefects, such as interstitial and vacancy loops, small inclusions and precipitates

iii) extended defects, such as dislocations and stacking faults.

A large variety of simple intrinsic defects may exist in GaAs: vacancies in each sublattice V_{Ga}, V_{As}, interstitial Ga_i and As_i, with at least two possible sites for each ; antisites defects As_{Ga} and Ga_{As}. Each of these defects can have more than one charge state and can have several configurations by forming pairs or complexes between them, thus creating more than one trap state or level in the band gap. The trap density in ion-implanted GaAs can vary over a wide range of values. The quality of SI GaAs, implantation and annealing parameters, type of annealing, all affect the trap concentration in the final device [25-26]. A good review of the deep-level defects in III-V semiconductors is given by Mircea and Bois [101].

One major deep level in LEC GaAs is the well-studied EL2 with activation energies between E_c-0.78 eV and E_c-0.83 eV [43-45]. This level has also been reported in VPE (vapor phase epitaxy) and MOCVD (organo metallic chemical vapor deposition) layers of GaAs [45-48]. The experimental results have shown the evidence of assigning this level to V_{Ga}-related defect. Li and Wang have

developed a possible model for the mechanism of EL2 formation and assigned the origin of EL2 to the simple antisite As_{Ga} defect with the assumption that the complexes of higher order involving As_{Ga} are not formed [49]. From their model, the antisite defect As_{Ga} can be predicted to form favorably in ion-implanted and annealed GaAs sample. The antisite defect, As_{Ga}, is a double donor giving rise to the midgap trap, EL2, with its characteristics photo-quenching effects [50]. The common electron and hole traps present in the bulk and epitaxial GaAs are very well documented and are shown in Tables 3.4 and 3.5 for electron and hole traps, respectively [34,57].

Jervis and co-workers have investigated the effects of ion-implantation and annealing of LPE (liquid phase epitaxy) GaAs and indicated that the deep level concentrations in them are primarily the characteristics of the material before implantation [55]. They have also observed that the Si implantation through a Si_3N_4 cap significantly increases the deep level concentration by providing pathways for the contaminants to reach the active layer.

3.5.1 Effects on Material and Device Properties

The deep levels can perturb the characteristics of MESFETs by means of exchange of the carriers with either the conduction band or the valence band; depending upon the nature of the trap and its position in the band gap. Ponce and coworkers [1] observed a positive correlation, as shown in Fig. 3.8, between etch pit density (EPD), mobility and transconductance (g_m) of a MESFET formed by 200 keV Si-implantation into LEC GaAs. All three parameters have high values near the edge and center of the wafer. This correlation is attributed to the interactions among microscopic imperfections as a result of processing. A similar relationship between FET characteristics, substrate mobility, and dislocation density has been reported by Wang and Bujatti [13]. They suggest that the dislocations are indirectly related to device performance through an improvement in mobility because of segregation of unwanted imperfections. Pearton *et al.* [14] have, however, mentioned that the presence of dislocations alone is not important in influencing the electrical properties of the active GaAs layer. They observed that although the loop density is significantly reduced due to RTA, a significant

Table 3.4. Electron trap parameters in bulk and epitaxial GaAs [34].

Label (Fig. 1)	Reference and alternative labels	Activation energy E_{na}, eV	Emission section σ_{na}, cm^2	Observations	Possible comparisons
ET1	(14)	0·85	$6{\cdot}5\times10^{-13}$	Bulk material	
ET2	(14)	0·3	$2{\cdot}5\times10^{-15}$	Bulk material	
ES1	(13)	0·83	$1{\cdot}0\times10^{-13}$	Bulk material	
EF1	(15)	0·72	$7{\cdot}7\times10^{-15}$	Cr doped bulk mat.	
EI1	(20)	0·43	$7{\cdot}3\times10^{-16}$	V.P.E. mat.	
EI2	(20)	0·19	$1{\cdot}1\times10^{-14}$	V.P.E. mat.	
EI3	(20)	0·18	$2{\cdot}2\times10^{-14}$	V.P.E. mat.	
EB1	(16)	0·86	$3{\cdot}5\times10^{-14}$	Cr doped L.P.E. mat.	
EB2	(16)	0·83	$2{\cdot}2\times10^{-13}$	As grown V.P.E. mat.	
EB3	(12) (E5)	0·90	$3{\cdot}0\times10^{-11}$	Electron irradiated mat.	
EB4	(12) (E4)	0·71	$8{\cdot}3\times10^{-13}$	Electron irradiated mat.	
EB5	(17) (M4)	0·48	$2{\cdot}6\times10^{-13}$	As grown M.B.E. mat.	
EB6	(12) (E3)	0·41	$2{\cdot}6\times10^{-13}$	Electron irradiated mat.	
EB7	(17) (M3)	0·30	$1{\cdot}7\times10^{-14}$	As grown M.B.E. mat.	
EB8	(17) (M1)	0·19	$1{\cdot}5\times10^{-14}$	As grown M.B.E. mat.	
FB9	(12) (E2)	0·18	Imprecise	Electron irradiated mat.	
EB10	(12) (E1)	0·12	Imprecise	Electron irradiated mat.	
EL1		0·78	$1{\cdot}0\times10^{-14}$	Cr doped bulk mat.	
EL2	(10) (A)	0·825	$(0{\cdot}8\text{–}1{\cdot}7)\times10^{-13}$	V.P.E. material	EL2 = ET1 = ES1 = EB2
EL3	(10) (B)	0·575	$(0{\cdot}8\text{–}1{\cdot}7)\times10^{-13}$	V.P.E. material	
EL4		0·51	$1{\cdot}0\times10^{-12}$	As grown M.B.E. mat.	EL4 = EB5
EL5	(10) (C)	0·42	$(0{\cdot}5\text{–}2{\cdot}0)\times10^{-13}$	V.P.E. mat.	EL5 = EB6(?)
EL6		0·35	$1{\cdot}5\times10^{-13}$	Bulk material	EL6 = ET2
EL7		0·30	$7{\cdot}2\times10^{-15}$	As grown M.B.E. mat.	EL7 = EB7; EL7 = EL6(?)
EL8	(18) (D)	0·275	$7{\cdot}7\times10^{-15}$	V.P.E. mat.	
EL9	(18) (E)	0·225	$6{\cdot}8\times10^{-15}$	V.P.E. mat.	
EL10		0·17	$1{\cdot}8\times10^{-15}$	As grown M.B.E. mat.	EL10 = EB8
EL11	(18) (F)	0·17	$3{\cdot}0\times10^{-16}$	V.P.E. mat.	EL11 = ET3 = EL10(?)
EL12	(18) (A′)	0·78	$4{\cdot}9\times10^{-12}$	V.P.E. mat.	EL12 = EB4(?)
EL14		0·215	$5{\cdot}2\times10^{-16}$	Bulk material	
EL15		0·15	$5{\cdot}7\times10^{-13}$	Electron irradiated mat.	EL15 = EB9
EL16		0·37	$4{\cdot}0\times10^{-18}$	V.P.E. mat.	

Table 3.5 Hole trap parameters in bulk and epitaxial GaAs [57].

Label (Fig. 1)	Reference and alternative labels	Activation energy E_{pa} (eV)	Emission section σ_{pa} m^{-2}	Type of sample	Excitation mode	Chemical origin	Possible comparisons
HT1	(8)	0·44	$1·2 \times 10^{-14}$	V.P.E.			
HS1	(9)	0·58	$2·0 \times 10^{-19}$	L.P.E.			
HS2	(9)	0·64	$4·1 \times 10^{-16}$	L.P.E.			
HS3	(9)	0·44	$4·8 \times 10^{-18}$	L.P.E.			
HB1	(4)	0·78	$5·2 \times 10^{-16}$	Cr-doped l.p.e.		Cr	
HB2	(4) (B)	0·71	$1·2 \times 10^{-14}$	As-grown l.p.e.			
HB3	(4)	0·52	$3·4 \times 10^{-16}$	Fe-doped l.p.e.		Fe	
HB4	(4)	0·44	$3·4 \times 10^{-14}$	Cu-doped l.p.e.		Cu	
HB5	(4) (A)	0·40	$2·2 \times 10^{-13}$	As-grown l.p.e.			
HB6	(7) (H1)	0·29	$2·0 \times 10^{-14}$	Electron irradiated l.p.e.			
HL1	(3)	0·94	$3·7 \times 10^{-14}$	Cr-doped v.p.e.	Electrical and optical	Cr	HL1 = HB1 = HS1
HL2	(3)	0·73	$1·9 \times 10^{-14}$	As-grown l.p.e.	Electrical and optical		HL2 = HB2 = HS2
HL3	(10)	0·59	$3·0 \times 10^{-15}$	Fe-diffused v.p.e.	Electrical	Fe	HL3 ≃ HL8
HL4	(3)	0·42	$3·0 \times 10^{-15}$	Cu-diffused v.p.e.	Electrical and optical	Cu	HL4 = HB4 = HT1
HL5	(3)	0·41	$9·0 \times 10^{-14}$	As-grown l.p.e.	Electrical and optical		HL5 = HB5
HL6	(10)	0·32	$5·6 \times 10^{-14}$	V.P.E. with p^+ layer	Electrical		
HL7	(10)	0·35	$6·4 \times 10^{-15}$	As-grown m.b.e.	Electrical		HL7 = HB6 ?
HL8	(10)	0·52	$3·5 \times 10^{-16}$	As-grown m.b.e.	Electrical		HL8 = HB3
HL9	(10)	0·69	$1·1 \times 10^{-13}$	As-grown v.p.e.	Optical		
HL10	(10)	0·83	$1·7 \times 10^{-13}$	As-grown v.p.e.	Electrical and optical		
HL11	(10)	0·35	$1·4 \times 10^{-15}$	Melt grown	Optical		HL11 = HL5 ?
HL12	(10)	0·27	$1·3 \times 10^{-14}$	Zn-contaminated l.p.e.	Electrical		

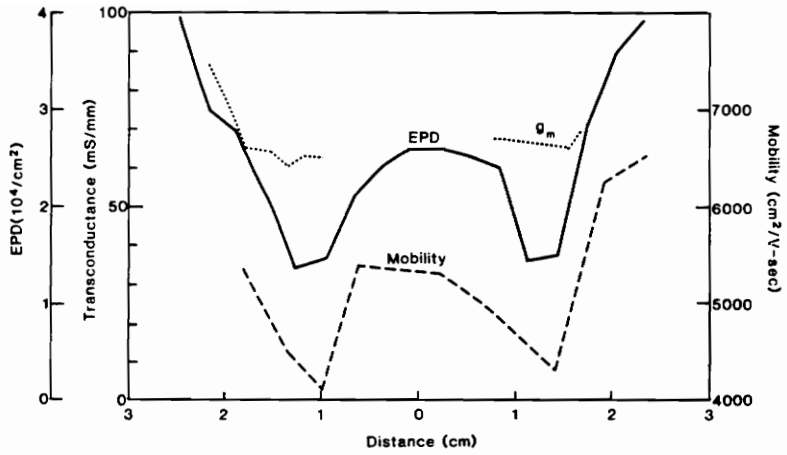


Fig. 3.8 Radial distribution of dislocation density, mobility, and transconductance across a GaAs wafer [1].

quantity of these extended defects still remained. These remaining loops did not appear to affect the electrical activation or the carrier mobility in the active layer, the mobility being comparable to that of the bulk.

A lot of work has been dedicated towards the relationship between substrate defects and FET performance [3-5]. The direct effects of dislocation on the electrical properties of the active layers and on the performance of MESFETs formed by ion implantation and annealing have been reported [3-5,72]. The threshold voltage (V_{th}) shifts to more negative values as the dislocation density increases. Most of the previous work has emphasized the correlation between the dislocations and the various device properties, especially the pinch-off voltage [6-9] and the saturation current [10-12]. In view of the correlation of the device threshold voltage (V_{th}) and the transconductance (g_m) with dislocation, Pearton, *et al.* [14] predicted that the electrical properties of devices and/or active layers are decided by the impurity cloud gathered to, and surrounding the dislocation core, rather than by the intrinsic properties of the extended defect itself. During RTA, there is less chance of impurity collecting near the dislocation, and this may possibly account for the occasional observations of the higher activations for the RTA compared to the furnace annealed GaAs, even though the residual damage is higher in the former. Along this line, Sadana [19] also reports that the structural defects visible by TEM in furnace annealed GaAs are apparently not the most important factor in determining the electrical activity of the implanted region.

Golio and Trew have presented a modelling technique for determining the carrier concentration (n(x)), the low-field mobility ($\mu(x)$), and the saturation velocity ($v_m(x)$) profiles for a known depth distribution of trap density ($N_T(x)$) and shallow-level donor concentration ($N_D(x)$) [24]. They subsequently fed these parameters into a device model to predict the dc characteristics and small-signal S parameters of ion-implanted MESFETs. The carrier and the mobility profiles for 70 keV Si-implanted GaAs with peak doping density of $2x10^{17}$ cm^{-3} are shown in Figs. 3.9a and 3.9b, respectively, for different trap density values. It is noted that the trapping states in GaAs have a significant effect on both the free carrier concentration and the transport properties of the implanted

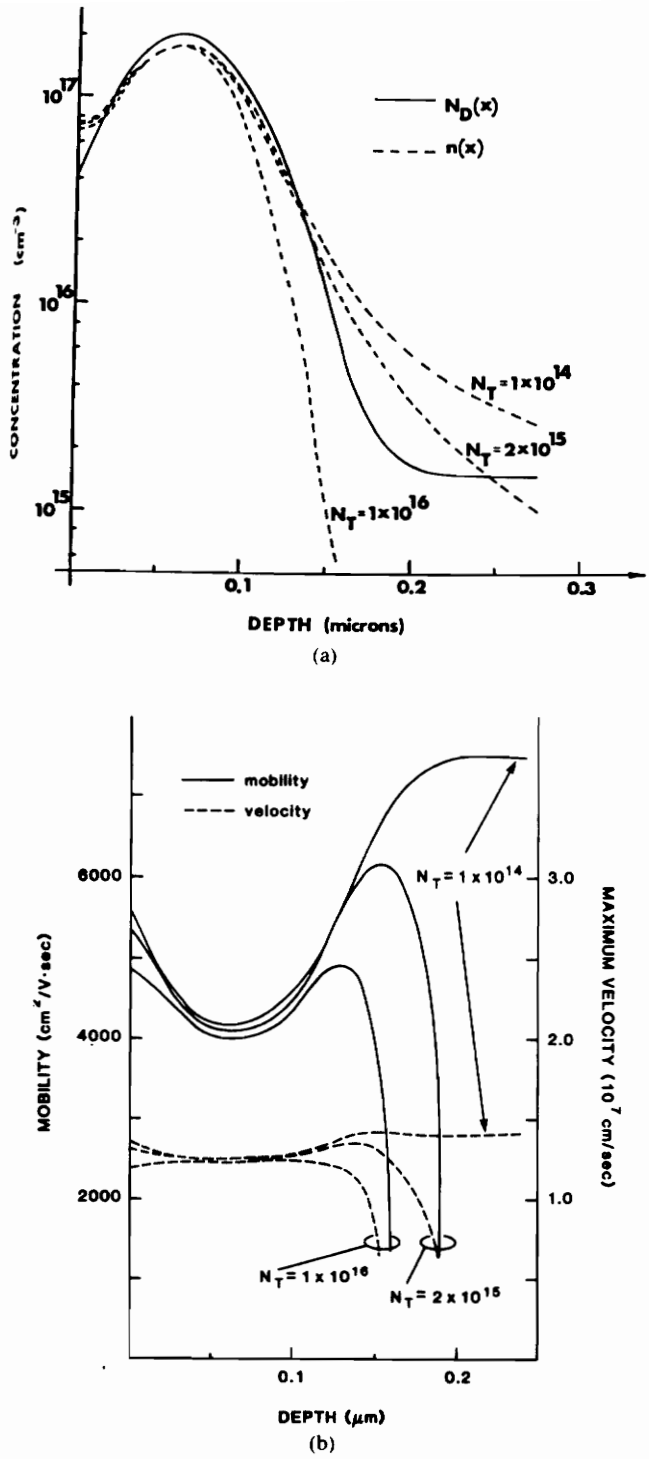


Fig. 3.9 Simulated effects of trap concentration in 75 keV Si-implanted GaAs a) carrier concentration (solid curves) and trap concentration (dashed curves) profiles and b) mobility and velocity profiles for the samples in a) [24].

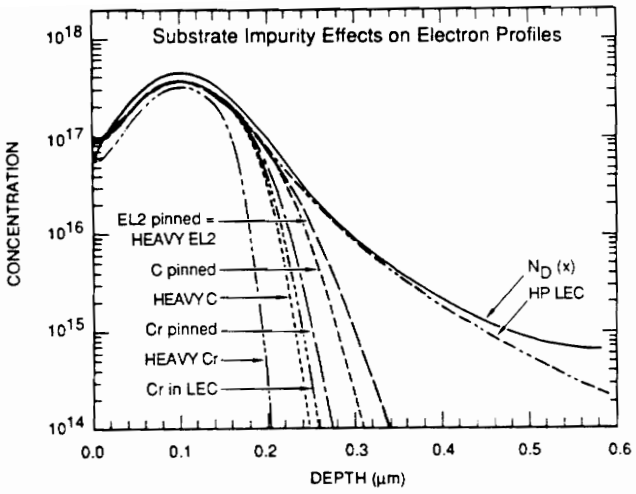
Table 3.6 75 keV Si-implanted MESFET circuit element values for peak concentration = $2x10^{17}$ cm^{-3}, V_{DS} = 3 V, V_{GS} = 0 V, L = 1 μm, Z = 300 μn [24].

Element	Deep level concentration (cm^{-3})		
	$1x10^{14}$	$2x10^{15}$	$1x10^{16}$
g_m (mho)	48.4	45.6	41.5
C_{gs} (pF)	0.419	0.417	0.399
R_{dr} (kΩ)	1.22	1.20	1.35
R_i (Ω)	3.337	3.423	3.680
τ (psec)	8.00	8.15	8.41
f_{max} (GHz)	66.1	64.5	61.8

g_m : transconductance
τ : gate delay
f_{max} : maximum frequency of oscillation
R_i : input resistance
R_{dr} : output resistance
C_{gs} : gate-source capacitance

active layer. The MESFET equivalent parameters for three different deep level densities are shown in Table 3.6. The deep level concentration has the most impact on the MESFET transconductance and the gate delay time, which decreases and increases, respectively, as the trap concentration increases [24]. The gain-bandwidth product (f_T) and the maximum frequency of oscillation (f_{max}) are affected by N_T, decreasing steadily at high values of N_T. There exists a critical trap concentration, depending upon the implantation energy and dose, beyond which a severe degradation in the device performance is predicted [24]. The deep electron traps in the active layer of MESFETs are also known to have deleterious effects on the noise figure (NF) of the device. The fluctuation in the occupancy of deep traps in the device causes generation noise. The excess in the minimum noise figure scales directly with the trap density [120].

The effects of substrate impurities on the ion implanted channel of a GaAs MESFET are very well investigated by Anholt and Sigmon [102]. They indicated that background impurities of shallow and deep acceptors in GaAs play an important role in determining the shape of the implanted carrier profile and on the uniformities in threshold voltage of MESFETs formed on them. In order to obtain an implant profile with a steeply falling tail, it is suggested that a high concentration of deep or shallow acceptors in the substrate is required. The modeled results are shown in Fig. 3.10a, where the strong impact of shallow (carbon) and deep (chromium) acceptors on the electron profiles is evident. With deep or shallow acceptors on the substrate side, an electron energy barrier is formed between the substrate and the active layer. The height of the barrier increases with the acceptor concentration, resulting in a greater carrier depletion on the active side and thus a narrowing of the carrier profile in the active layer. Anholt and Sigmon also indicated the importance of a buried p-layer to generate a sharply falling electron profile in the overlying active layer [102]. This approach would also help in improving the threshold voltage uniformity (more applicable to digital FETs) because of the lower influence of the fluctuating acceptor impurities in the substrate. The use of a buried p-layer in the fabrication of a SAINT (self aligned implantation for n^+ layer technology) has been demonstrated by Yamasaki and coworkers [105], and they obtained very high speed performance



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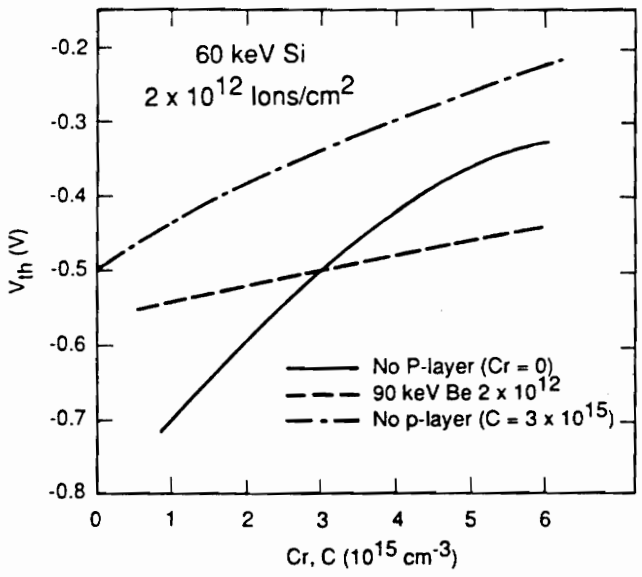


b)

Fig. 3.10 Modeled effects of substrate impurities on a) Si-implanted carrier profile in GaAs and b) MESFET threshold voltage [102].

FET (minimum delay time of 9.9 ps/gate), with a better threshold voltage control and with suppression of the substrate current in these devices. Unlike dislocation, which has a local effect on MESFET threshold voltage, the impurities affect the device characteristics almost uniformly across the entire wafer [103]. The dependence of the MESFET threshold voltage on the acceptor concentration is found to be significant; an increased shallow or deep acceptor concentration results in higher threshold (more positive) voltage and is shown in Fig. 3.10b [102]. Similar observations have been reported by Baumgartner and Löhnert in which they correlated the bulk resistivity of a SI GaAs substrate to the residual acceptor concentration and eventually to the threshold voltage of MESFETs [113].

The reduction in carrier mobility in an active GaAs layer occurs not only due to the scattering effects of the ionized dopants but also due to other possible scattering mechanisms involving defects and imperfections, either present in the original substrate or induced by the fabrication process [27]. Deep levels in the channel region or at the channel-substrate interface region of FETs can give rise to various undesirable effects such as variation of g_m with frequency, adverse noise performance, sensitivity to light, looping or hysteresis in the drain current-voltage characteristics, low output resistance, low source-drain breakdown voltage, low power gain at rf, and backgating/sidegating.

Although all of the above mentioned effects contribute to the anomalies in MESFETs, the problem of backgating or sidegating is most significant for both analog and digital integrated circuits as it will result in the unwanted interaction between closely spaced devices, consequently putting limits on the achievable circuit packing density. Backgating and sidegating refer to the reduction in drain-source current in a FET as a result of a bias applied to the substrate and to a nominally isolated-side electrode (or device), respectively [85,86]. The sidegating effects has also been observed for dc, rf, and digital bias conditions [87]. Alternatively, sidegating can be defined as a crosstalk between FET and an adjacent isolated device, while backgating is the crosstalk between the FET and the substrate electrode. Kocot and Stolte, in their backgating model, held deep traps at the channel-substrate interface, either EL2 or Cr center, responsible for this effect [86]. Some success in reducing this effect

has been achieved by incorporating a high resistivity undoped AlGaAs or AlGaAs/GaAs superlattice buffer layer between the active layer and the SI GaAs substrate [89] or by using a p-type implant under an n-type active GaAs layer [90]. The published results on the effects of the buffer layers will be discussed in section 3.8.

Lee, *et al.* have reported a correlation between the current conduction in the substrate and the backgating effects [100]. The onset bias for the backgating effect reportedly coincides with the trap-fill-limited voltage (the applied bias at which the injected carriers fill up the deep traps in the substrate) for substrate conduction [100]. Several researchers have suggested that the effective thickness of the channel is modulated by the extension of the depletion region from the substrate interface into the active n-layer, due to traps near the interface [52,53]. Itoh and Yanai, in their investigation of the interface effects on GaAs MESFETs, have shown that the major cause of drift in drain current and rf parameters in GaAs MESFETs is the interface effects and not the surface effects, since drift was also observed in the surface-passivated devices [54].

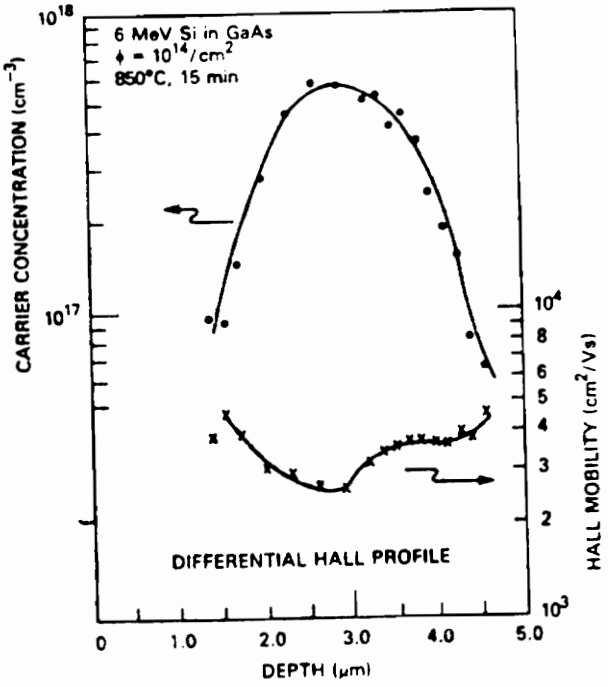
3.6 High Energy Implantation

High energy (MeV) implantation is of interest in the fabrication of microwave monolithic integrated circuits and the special device structures which require deep conductive layers (e.g. mixer diode, varactor diode, PIN diode etc.). By the use of selective ion implantation deep and shallow conductive layer devices can be integrated in a monolithic format. The surface properties of GaAs are very process sensitive and are difficult to control. Accordingly, GaAs device performances are dependent on the surface conditions. MeV implantation results in increased depth of ion penetration which may potentially be useful in forming devices away from the surface with higher yield. The literature available on MeV implantation of GaAs is scarce. Recently Krownne and Thompson have successfully employed MeV ion implantation in the fabrication of a slow wave phase shifter designed for performing in the millimeter wave range [121]. They report that the ion-implanted phase shifter devices showed comparable electrical performance to the epitaxial devices. Feasible use of MeV

implantation in the construction of a millimeter-wave mixer diode has been demonstrated [122].

A buried active layer is formed after MeV implantation and annealing of GaAs [123-125]. A typical electrical profile (free-carrier density and mobility) for a 6 MeV Si-implanted and furnace annealed (850 °C /15 min.) GaAs sample is shown in Fig. 3.11a. The buried n-layer is located at a depth of 2 μm from the surface for the case of 6 MeV Si implantation. It has been indicated that for an implant concentration of 5×10^{17} cm^{-3} or less, 850 °C furnace annealing is quite adequate but for a higher implant concentration, the RTA method yields superior results [124]. The Hall mobility of the carriers in the buried layer compares well to the reported value of the drift mobility at a particular impurity concentration. SIMS and electrolytic C-V measurements performed on 1, 2, 4 and 6 MeV Si-implanted GaAs showed practically no dopant redistribution, both for the case of furnace annealing (800 °C, 15 min.) and RTA (1000 °C, 10 sec) methods [126]. Higher n-type activation has been reported when Si is co-implanted with sulphur [125]. Sulphur occupies As sites and thus minimizes the possibility of Si taking up As sites and causing self-compensation.

The electrical and structural changes in GaAs as a result of Cl^{3+} (6.2 or 8.3 MeV) and O^{3+} (6.2 MeV) implantation have been reported [127]. The RBS and XTEM results indicate that MeV ion-implantation, both Cl^{3+} and O^{3+}, resulted in a buried amorphized crystal structure for ion doses above 1×10^{15} cm^{-2}. Although annealing can restore crystallinity to the amorphized region, many of the crystal defects still remained after the heat treatment [127]. The structural effect of MeV Si-implanted GaAs and its annealing behavior have been reported by Chen and coworkers [128,129]. They report that MeV Si-implantation of GaAs at room temperature results in a very small amount of lattice disorder. There is a possibility that the dislocations may be disordered but no amorphous regions are otherwise created. This is contrary to the finding of Bardin *et al.* [127]. It has been suggested that during MeV implantation of GaAs, an extensive in-situ self-annealing takes place with the formation of both perfect and partial interstitial-type dislocation loops [128, 129]. These loops appear to form by the merging of the excess interstitial generated as a result of the implantation. Upon annealing at 500 °C and beyond, the surface region became increasingly defect free with



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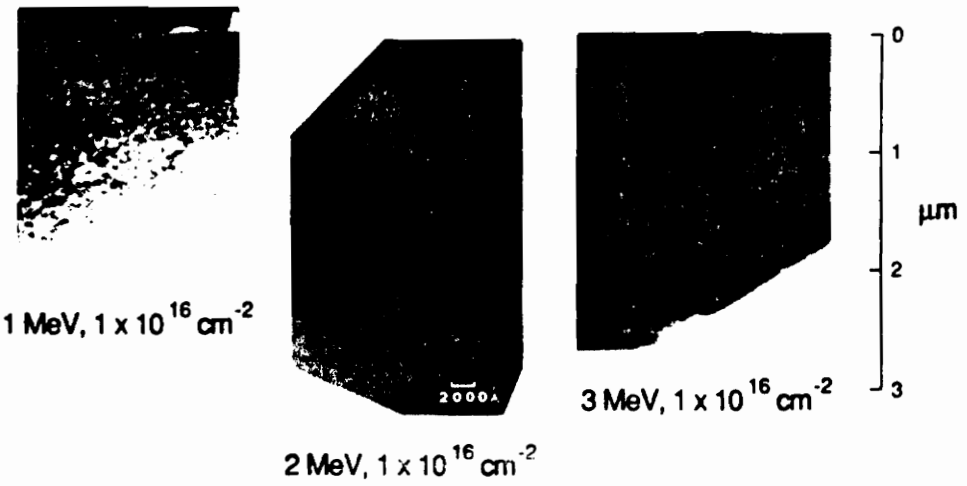


b)

Fig. 3.11 a) Carrier concentration and mobility profiles in 6 MeV Si implanted and furnace annealed GaAs [124] and b) XTEM microstructures of 1, 2, and 3 MeV Si-implanted GaAs [128].

dislocations increasing in size and decreasing in density. The annealing-out of the defects at the near-surface region is partly due to the fact that the dislocation loops, during annealing, grow and climb to the surface, with the surface acting as annihilation sink for the loops [129]. A typical XTEM microstructure for 1, 2, and 3 MeV Si-implanted (1 x 10^{16} cm^{-2}) and RTA (800 °C, 30 sec) GaAs is shown in Fig. 3.11b. It is evident from the figure that a buried residual defect band of loops remains even after high temperature annealing and with an increase in implant energy, the band of defects is located farther away from the surface.

3.7 MBE Epitaxial Layer

The first study of deep levels in n-GaAs grown by MBE was reported by Lang *et al.* [32] and they observed nine different electron traps labelled M0....M8. Most of the observed traps are ascribed to the chemical contaminants incorporated during growth. Lang *et al.* [32] concluded that these traps are characteristics of the growth process and their occurrence is very much influenced by the growth conditions. The trap parameters of few "M" levels are provided in Table 3.4 [34]. Blood and Harris have shown that the concentrations of the "M" levels in MBE GaAs is weakly dependent on As:Ga flux ratio but decrease rapidly with increasing growth temperature [33]. Tables 3.7 and 3.8 summarize the effects of MBE growth temperature on electron and hole trap concentrations in GaAs, respectively [60]. Typically substrate temperature during growth varies between 550 - 650 °C. Neave, *et al.* have obtained a correlation between the arsenic species and the trap concentrations [35]. With all other growth parameters remaining constant, a substantially lower trap concentration is detected in MBE GaAs layers grown with dimeric arsenic (As_2) than with tetrameric arsenic (As_4) species. This fact is also supported by Künzel *et al.* [106]. Skromme *et al.* have characterized high purity Si-doped MBE GaAs (total trap concentration ~ $3x10^{13}$ cm^{-3}) using different purity As sources. They concluded that to achieve high purity layers, improvement in the vacuum system is not only sufficient but a highest purity of As source with lowest concentration of residual impurities is also necessary [107]. They have indicated that the As source contributes to C contamination and this possibly explains why the

Table 3.7. Summary of electron traps in MBE-GaAs grown at different temperatures [60].

Layer	Substrate* temperature, °C	Trap density, cm^{-3} EB8 M1	EB7 M3	EB5 M4	EB3	EB6	EL3	Detection limit
A1	550			1×10^{12}				5×10^{11}
A2	550	1×10^{13}						1×10^{12}
A3	550	1×10^{13}	1×10^{12}	1×10^{13}				1×10^{12}
B1	520	5×10^{14}						1×10^{13}
B2	490	3×10^{14}	7×10^{13}	4×10^{14}				1×10^{13}
B3	460		1×10^{15}		4×10^{16}			1×10^{14}
B4	430		2×10^{15}	$3 \times 10^{}$	5×10^{15}			1×10^{14}
B5	320				1×10^{16}	3×10^{14}	3×10^{15}	2×10^{14}
B6	300				6×10^{15}	4×10^{14}	6×10^{15}	2×10^{14}

* All traps with unmarked densities were found to be below the detection limit

Table 3.8. Summary of hole traps in MBE-GaAs grown at different temperatures [60].

Layer	Substrate temperature, °C	Trap density, cm^{-3} HL9	HB4 (copper)	HB1 (chromium)	Cr(A) (chromium)	HB6	Detection limit
A1	550	6×10^{13}		8×10^{12}	X	X	2×10^{12}
A2	550	1×10^{13}	1×10^{13}	1×10^{12}	1×10^{12}		2×10^{11}
A3	550	8×10^{13}		5×10^{13}	6×10^{13}		1×10^{12}
B1	520	2×10^{14}	3×10^{14}				1×10^{13}
B2	490						2×10^{13}
B3	460	1×10^{15}	3×10^{15}			2×10^{15}	2×10^{13}
B4	430	4×10^{15}	3×10^{15}			2×10^{15}	5×10^{14}

X: data in the temperature range of this trap not taken

undoped MBE GaAs is slightly p-type ($p \sim 10^{14}$ cm^{-3}) [108].

EL2, which is not present in the as-grown MBE n-GaAs, can be created by high temperature annealing [31,36,37,56]. Also the concentration of electron traps in the as-grown MBE n-GaAs is substantially reduced by high temperature annealing (around 700 °C) [31,56]. The effects of annealing (capless or Si_3N_4-capped) on the deep level spectra of MBE n-GaAs are shown in Fig. 3.12 [56].

Metze and Calawa have studied the effects of growth rates on low temperature MBE-grown and Si-doped GaAs [95]. They could obtain a good n-type GaAs film at substrate temperatures as low as 380 °C by reducing the growth rate to ~ 0.02 μm/hr from the conventional growth rate of ~ 1 μm/hr. They believe that at temperatures below 500 °C, the variable acceptor concentration, which presumably causes compensation in Si-doped GaAs, increases with a decrease in the growth temperature at a constant growth rate (R) . So with a decrease in the substrate temperature, R has to be correspondingly decreased in order to obtain reasonable n-type behavior. The acceptor defects are identified as defects resulting from the insufficient time for the adsorbed As and Ga atoms to reach to their appropriate lattice sites [95]. Beyond a 500 °C growth temperature, the acceptor defect concentration is negligible compared to the Si donor concentration, and therefore an n-type layer with good electrical properties is realized.

Palmateer, *et al.* have reported on the dependence of the properties of MBE GaAs layers grown at 565 °C on a heat-treated and non heat-treated Cr-doped GaAs substrates [70]. No electron traps of concentration greater than $1x10^{12}$ cm^{-3} were detected when the pressure ratio of the As_4 and Ga beam fluxes during growth was 6:1. In the case of the non-heat-treated substrate, significant build-up of Mn and Si, originating from the substrate, at the substrate-epilayer interface has been reported [70]. Biswas, *et al.* have investigated the regrowth of Si-doped MBE GaAs on an epitaxial GaAs substrate (at 610 °C, at a growth rate of 0.8 μm/hr with As/Ga flux ratio of 18:1) with the regrowth surface being exposed to several realistic device processing steps [111]. They indicate the presence of a perturbed carrier profile at the substrate regrown-layer interface and identified several deep electron and hole traps at the interface region. The origin of the perturbed carrier profile is

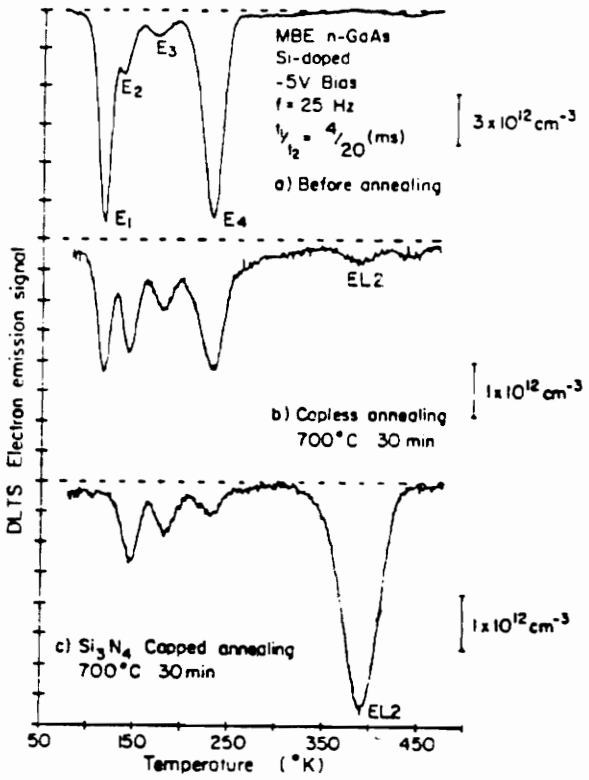


Fig. 3.12 DLTS spectra of electron traps in Si-doped MBE GaAs, a) unannealed, b) capless annealed (700 °C/30 min), and c) Si_3N_4 capped and annealed (700 °C/30 min) [56].

attributed to the disordered region created at the interface during regrowth.

3.8 Buffer Layer

To reduce anomalies and improve rf performance of a FET, the insertion of a buffer layer between the channel and the substrate has been proposed [51]. However, the buffer layer is not always effective in eliminating the anomalies and therefore the interfacial problems in GaAs MESFETs still remain even with the buffer layer. This problem is serious for performance stability of not only GaAs MESFET, but also other GaAs planar devices such as Gunn effect devices, monolithically integrated circuits, etc.. A number of significant problems facing GaAs IC development has been attributed to the SI GaAs substrate or to the buffer layer underlying the active layer [52]. Itoh and Yanai have studied the instability in drain current in GaAs MESFETs with buffer layer and indicated that the instability is due to the hole traps or deep acceptors, which exist both at the channel-buffer and the buffer-substrate interfaces[84]. From the viewpoint of stability performance, the interface effects in GaAs planar devices are phenomenon in which the effective thickness of the channel is modulated by the extension of the depletion layer from the interface into the active n-channel, due to traps or impurities located at the interface. A small fluctuation in the effective channel thickness causes drastic changes in the drain current and some of the equivalent circuit and high frequency parameters of a GaAs MESFET [54]. It has been reported that the deep level impurities and defect centers, which are typically observed in the active and buffer layers, most often originate from the GaAs substrate [70].

The phenomenon of backgating is caused by the relatively large capacitance at the substrate-active channel interface due to negative charge accumulation on deep traps in the interface region. Closely compensated substrates or buffer layers have less backgating effects than those with large excess deep traps which are unoccupied in the bulk [86]. To reduce backgating, the buffer layer should provide an increase in bulk resistivity. The microwave performance of GaAs MESFETs is known to be limited by undesirable material properties resulting in high parasitic output conductance

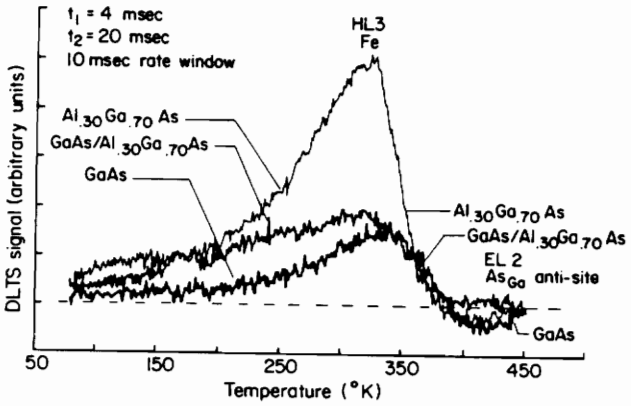
due to the space charge limited buffer-substrate current [66]. In addition, there is a premature saturation of the output power and increased noise figures as a result of the substrate traps [67-69].

Schaff and Eastman report a superior performance of a MBE-grown GaAs FET on a superlattice (270 Å $Al_{0.45}Ga_{0.55}As$/ 30 Å GaAs, 100 periods) buffer compared to FETs on GaAs and AlGaAs buffers [71]. The DLTS measurements of FETs grown on three different buffers (GaAs, AlGaAs, and superlattice) are shown in Fig. 3.13a. The deep level concentration is considerably reduced by using the superlattice buffer layer. The corresponding backgating performance of FETs on these three buffers is shown in Fig. 3.13b. The GaAs and superlattice buffered devices showed minimal light sensitivity and little backgating effect. The severe light sensitivity in the AlGaAs buffer sample is likely to be linked to the higher deep level concentrations found in them. It has been observed that growth interruption during MBE can cause compensating centers to develop near the interface [82]. As a result, carrier depletion in the growing n-GaAs near the interface occurs, and is believed to be due to the out-diffusion of negatively charged centers into the GaAs overlayer during subsequent processing.

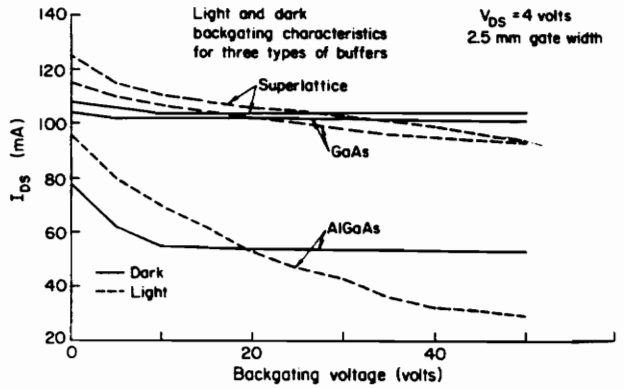
3.8.1 Low Temperature GaAs Buffer

Crystal defects during low temperature (LT) MBE growth of GaAs are produced because of the adsorbed Ga and As atoms, which fail to diffuse to the appropriate lattice sites before being incorporated into the growing film. Low temperature MBE growth is associated with high deep level concentrations mostly related to high densities of Ga-vacancy complexes. The low growth temperature (temperature below the conventional 550-650 °C substrate temperature) introduces a high concentration of compensating point-defects in the buffer. The high concentration of these traps at low growth temperatures makes it simple to grow a semi-insulating layer. However, the application of such layers as high-resistance buffer layers for GaAs MESFETs is not straightforward.

Smith, *et al.* were the first to develop this new buffer at substrate temperatures of 150-300 °C using Ga and As_4 beam fluxes under As stable condition at a growth rate of 1 μm/hr [88].



a)



b)

Fig. 3.13 Effect of FET buffer layers on a) DLTS spectra of active layers and b) backgating characteristics [71].

They report that the new LT GaAs buffer is highly resistive, optically inactive, and crystalline. The MESFET fabricated on the active layer grown on this buffer showed improved output resistance and breakdown voltages, but most important of all is the elimination of backgating and light sensitivity. The results are shown in Fig. 3.14a and 3.14b, where the backgating performance of MESFETs formed by implantation or by growth on different buffer layers is compared. The dc and rf characteristics of the MESFETs with LT GaAs buffers are comparable to the MESFETs fabricated by other conventional means [88]. In a separate publication, the same group has presented a detailed study on the sidegating effects of LT GaAs buffer layers in analog MESFET circuits (at rf) and also in digital circuits [98]. They were successful in reducing the rf signal coupling between devices made on a LT (200 °C) GaAs buffer compared to devices formed using a conventional buffer layer (undoped MBE GaAs grown at 580 °C). The device characteristics in the later structure were strongly modified by a sidegate bias [98]. As for the digital circuit using the LT buffer, the voltage levels of logic states were not affected by the duty cycle of the pulse trains or by the magnitude of the voltage transition of the logic state on an adjacent device. This is in contrast to the digital circuit fabricated using the conventional buffer. It therefore appears that the LT buffer can provide excellent device isolation and immunity to sidegating effects that are very often encountered in digital, analog, and monolithic microwave integrated circuits. Improved backgating characteristics with a LT GaAs buffer compared to an AlGaAs buffer have been reported by Delaney *et al.*, where they successfully fabricated a high performance MESFET using a LT GaAs buffer layer [99].

Melloch, Miller, and Das have investigated the effects of incorporating a LT (220 - 300°C) MBE GaAs buffer on the characteristics of a modulation-doped two dimensional electron gas [96]. No deleterious effects on the carrier density and the mobility of the electron gas were observed as a result of the insertion of the buffer layer. Instead a very high electron mobility of ~ $2x10^6$ cm^2/V-sec at 4.2 K at an electron density of $5x10^{11}$ cm^{-2} was realized. Lin, *et al.*, however, have discussed the anomalies in MODFETs using a LT GaAs buffer layer [97]. Although the dc and the sidegating performance of the FETs using a LT (300 °C) GaAs buffer were encouraging, the buffered MODFETs

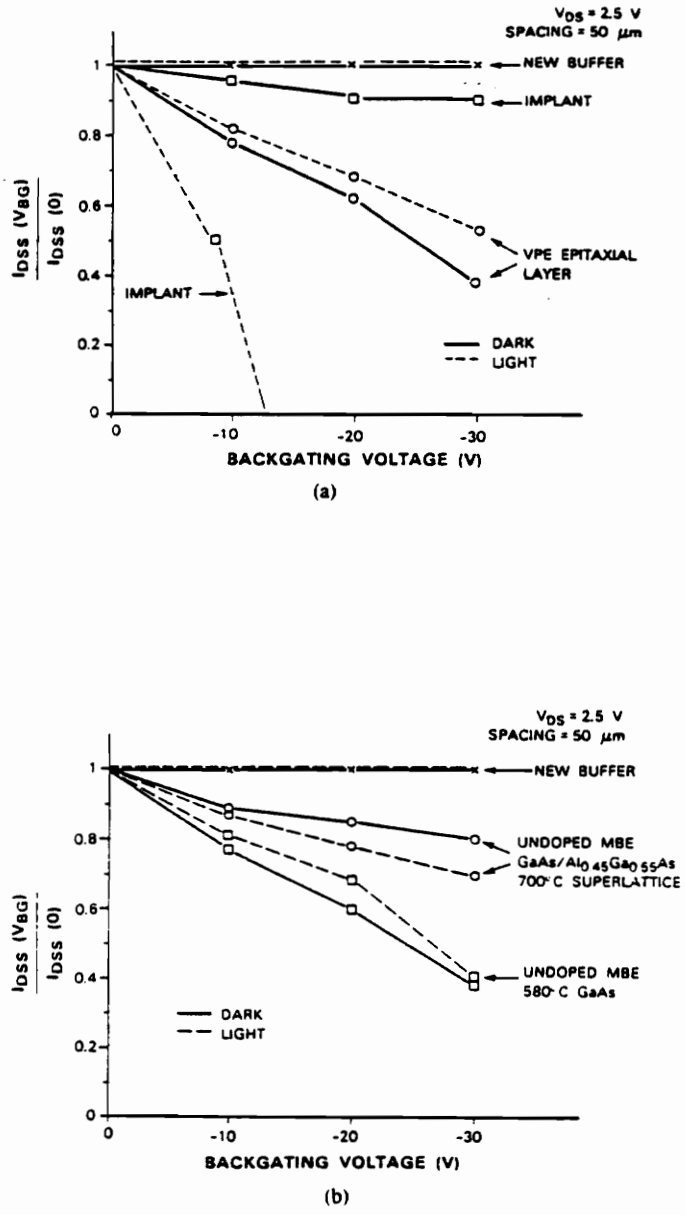


Fig. 3.14 Backgating characteristics of MESFETs using a) MBE active GaAs on LT GaAs buffer, VPE epitaxial, and implanted active layers, and b) MBE active GaAs on LT GaAs buffer, normal temperature MBE GaAs, and undoped superlattice buffer layers [88].

in a logic circuit exhibited slow turn-on transients and long propagation delays. These detrimental effects are probably caused by Ga vacancies diffusing into the top-epi during the epi-growth [97].

Kaminska, *et al.*, using TEM, XRD (X-ray diffraction), and EPR (electron paramagnetic resonance) techniques, report on the structural properties of MBE-GaAs grown at temperatures between 200-300 °C with a growth rate of 1 μm/hr [81]. Their results suggest that LT MBE-GaAs has a high degree of crystal perfection but with increased lattice parameter compared to the layers grown at normal MBE temperatures (550-650 °C). The layer grown at 200 °C showed the largest increase in the lattice parameter and also the highest concentration of arsenic antisite defects. Both the lattice parameter and the antisite defects were, however, reduced after a post growth annealing at 600 °C. The deep level concentration in a LT GaAs layer increases monotonically as the substrate temperature is reduced. At a growth temperature of 200 °C, the layer exhibits virtually no photoluminescence and has a resistivity substantially greater than that of SI GaAs [91]. These unique properties are attributed to an arsenic excess of ~ 1 atomic %. The LT GaAs buffer layer resistivity increases with decreasing growth temperature but below 200 °C, the layer thickness is limited by the material becoming polycrystalline [88]. The dislocation density in a LT GaAs buffer has been reported to be comparable to that of a GaAs epitaxial layer grown at normal substrate temperatures [91]. The large arsenic-rich deviation stoichiometry (~ 1-1.5 at. %) for a LT MBE GaAs layer has also been confirmed in a separate study [92]. Hall effect and EPR measurements on a LT GaAs buffer have shown the presence of an acceptor level at ~ 0.3 eV above the valence band, and is attributed to gallium vacancy. Wie, *et al.* have reported the XRC (X-ray rocking curve), RBS, and van der Pauw results on the MBE GaAs layers grown at 200 °C, 250 °C, and 305 °C [93]. The expansion in lattice parameter for the 200 °C grown layer was 0.15 %, which decreased with increasing growth temperature. The lattice parameter recovers on annealing at about 350-450 °C. This is related to the annealing of most of the defects, probably As interstitial, which are responsible for the lattice dilation.

The defect type and concentration in a LT GaAs layer may be similar to those in the high dose neutron-irradiated GaAs samples [94]. The main difference is that the neutron-irradiated GaAs

has stoichiometric point defects while a LT MBE-GaAs layer is As rich and contains As_i and As_{Ga} as dominant defects. The total defect concentration estimated from the lattice parameter measurements was very similar to the excess arsenic concentration in the sample and therefore the defects in LT MBE-GaAs involve As [94]. The temperature dependent conductivity data on LT MBE-GaAs indicate that the conduction mechanism involves hopping conduction through a defect band. Very recently, Tadayon, *et al.* have reported on the successful growth of a MBE GaAs layer at substrate temperature as low as 120 °C and at a growth rate of 0.1 μm/hr [104]. They have confirmed its high quality through Raman, 4 K photoluminescence, and TEM measurements.

3.8.2 $Al_xGa_{1-x}As$ Buffer Layer

The effects of using an $Al_xGa_{1-x}As$ buffer layer in MESFET fabrication have not been as extensively investigated as the effects of a low temperature GaAs buffer layer. The use of $Al_xGa_{1-x}As$ buffer layers in GaAs microwave power MESFETs to increase the device output resistance has been proposed by Eastman and his group [133]. It is known that an electron has a lower mobility and a lower saturation velocity in $Al_xGa_{1-x}As$ than in GaAs, and so the incorporation of $Al_xGa_{1-x}As$ as buffer layer is expected to increase the output resistance of a MESFET.

Morkoc and coworkers have investigated the $Al_xGa_{1-x}As$/GaAs interface properties grown by MBE at different substrate temperatures [134]. On the single period modulation doped $Al_xGa_{1-x}As$/ GaAs structures, they concluded that when the GaAs layer is grown over $Al_xGa_{1-x}As$, the mobilities of the two dimensional electron gas were much lower than when $Al_xG_{1-x}As$ is grown on top of GaAs. Moreover, the mobility in the former showed a strong dependence on the substrate temperature. The inferior mobility in GaAs/$Al_xGa_{1-x}As$ structures is attributed to the interface roughness caused by the binary growing on top of a "rough" ternary and may also be due to the impurity build-up at the hetero-interface because of the Al source. The defects in MBE-grown $Al_xGa_{1-x}As$ are strongly dependent on the growth temperature, growth rate, alloy composition, and the group V/III beam flux ratio, the results of which are very well documented [136-139].

Wang, *et al.* have succeeded in growing high quality $Al_xGa_{1-x}As$ buffer layers by MBE, and the GaAs MESFETs subsequently formed showed superior characteristics [135]. They fabricated MBE-grown n-GaAs on an $Al_xGa_{1-x}As$ ($x \sim 0.4$) buffer and at room temperature could obtain an electron mobility of ~ 4400 $cm^2/V\text{-sec}$ at a carrier density of ~ 1.1×10^{17} cm^{-3} in the channel. At a growth temperature of 550 °C of the buffer layer, they could not grow a n-type MBE GaAs layer on top because of the free carrier depletion arising from the out-diffusion of Ga vacancies, originating from the buffer. However, when the growth temperature was raised to 640-700 °C, the surface morphology of the buffer was smooth and a good n-type MBE-GaAs overlayer could be routinely obtained [135]. An $Al_{0.4}Ga_{0.6}As$ buffer layer grown at 700 °C was found to be highly resistive. The output resistance and the cut-off frequency of a MESFET on an $Al_{0.4}Ga_{0.6}As$ buffer were found to be 2000 ohm-mm and 45 GHz, respectively. There was no degradation of other device characteristics due to the use of $Al_{0.4}Ga_{0.6}As$ buffer.

CHAPTER 4. EXPERIMENTAL TECHNIQUES

This chapter details the sample processing history, contact formation techniques and the measurement system employed as a part this research. The information on the as-received wafers is provided first. The samples are divided into several groups, based on the objectives of the study. The order in which they are presented is the same as that of the results discussed in the next chapter. Following sample description, methods used to process and form contacts on GaAs will be discussed. Problems encountered during characterization, either due to sample preparation or wafer quality, will also be addressed. Lastly, the electrical characterization techniques of GaAs and a description on the measurement set up will be provided.

4.1 Wafer Description

The as-received wafers with their key process information and suppliers are classified in following categories:

A. <u>(100) and (211) undoped GaAs</u>

- Substrate material : (100) and (211) LEC GaAs
- ^{29}Si implantation energy/ dose : 50 keV/ 1.7 x 10^{13} cm^{-2}
- Implantation temperature/ cap : room temperature/ none
- Rotation angle during implantation★ : 0°, 45°
- Annealing mode : RTA
- Annealing temperature/ time : 850 °C/ 30 sec.
- Annealing cap : Si_3N_4
- Source : Texas Instruments

★ Rotation angle is the angle by which the major flat is rotated with respect to the horizontal plane of the beam.

B. (100) and (211) Cr doped GaAs

- Substrate material : (100) and (211) LEC GaAs:Cr
- Si^{29} implantation energy/ dose : 50 keV/ 1.7 x 10^{13} cm^{-2}
- Implantation temperature/ cap : room temperature/ none
- Rotation angle : 45° for (100), 0° and 45° for (211)
- Annealing mode : RTA
- Annealing temperature/ time : 850 °C/ 30 sec.
- Annealing cap : Si_3N_4
- Source : Texas Instruments

C.

(i) Fat FET* on control wafer (no-buffer)

- Starting substrate : (100) LEC undoped GaAs
- Si^{29} implantation energy/ dose : 150 keV/ 3.5 x 10^{12} cm^{-2}
- Implantation temperature/ cap : room temperature/ SiON
- Annealing mode : furnace
- Annealing temperature/ time : 827 °C/ 20 min.
- Annealing cap/ ambient : SiON/ 95% N_2 + 5%H_2
- SiON cap removal : in 50% diluted HF
- Self aligned TiWN gate (length by width) : 19.5 μm by 1712 μm

(ii) Fat FET* on low temperature (LT) GaAs buffer

- Starting substrate : (100) LEC undoped GaAs
- LT (250 °C) MBE GaAs buffer : 1.0 μm thick
- Normal temperature (580 °C) MBE undoped GaAs layer: 0.3 μm thick

- As to Ga flux ratio/ growth rate : 20:1/ 1 μm per hr.
- Si^{29} implantation energy/ dose : 150 keV/ 4 x 10^{12} cm^{-2}
- Implantation temperature/ cap : room temperature/ 850 Å SiON
- Annealing mode : furnace
- Annealing temperature/ time : 827 °C/ 20 min.
- Annealing cap/ ambient : 2000 Å SiON/ 90% N_2 + 10% H_2
- Self aligned TiWN gate (length by width) : 19.5 μm by 1712 μm

★ Fat FETs are large area FETs with gate lengths typically from 15 μm to 250 μm as compared to ≤ 1 μm in most FETs. Capacitance DLTS is limited in the case of small gate area FET devices, which have only very small capacitances and therefore the DLTS signal is hard to resolve and is often lost in the noise. To overcome this problem, capacitance DLTS on FETs are usually performed on fat FETs for better resolution. Refer to Fig. 5.13 (Chapter 5) for cross sectional schematics. In both (i) and (ii), gates were defined prior to implant activation. The fat FETs were fabricated and packaged at ITT, Roanoke.

D.

(i) Control wafer (no buffer)*

- Starting substrate : (100) SI LEC GaAs
- Si^{29} implantation energy/ dose : 150 keV/ 4 x 10^{12} cm^{-2}
- Implantation temperature/ cap : room temperature/ 850 Å SiON
- Annealing mode/ ambient : furnace/ 90% N_2 + 5% H_2
- Annealing temperature/ time : 827 °C/ 25 min.
- Annealing cap : 2000 Å SiON
- Source : ITT, Roanoke

(ii) $Al_{.35}Ga_{.65}As$ buffered wafers*

- Starting substrate : (100) LEC SI GaAs
- MBE grown undoped GaAs : 1000 Å thick
- 25 Å/25 Å period GaAs/AlAs MBE superlattice : 10 periods
- MBE grown (at 710 °C) undoped $Al_{.35}Ga_{.65}As$: 5000 Å thick
- As to Ga flux ratio for $Al_{.35}Ga_{.65}As$ growth/ growth rate : 10:1/ 1μm per hr.
- MBE grown (at 580 °C) undoped GaAs : 3000 Å thick
- As to Ga flux ratio for GaAs growth/ growth rate : 20:1/ 1 μm per hr.
- Si^{29} implantation energy/dose : 150 keV/ 4 x 10^{12} cm^{-2}
- Implantation temperature/cap : room temperature/850 Å SiON
- Annealing mode/ambient : furnace/ 90% N_2 + 5% H_2
- Annealing temperature/time : 827 °C/ 25 min.
- Annealing cap : 2000 Å SiON
- Interrupted growth between AlGaAs buffer and top epi GaAs layers
- Source : ITT, Roanoke

* Refer to Fig. 5.23 for cross sectional schematics. Four identically processed $Al_{.35}Ga_{.65}As$ buffered GaAs samples, on which fat FETs showed variable characteristics (discussed in Chapter 5), were investigated.

E. High energy MeV implanted GaAs

Sample	Si^{29+} energy (MeV)	implant dose (cm^{-2})	RTA (°C)/ 10 sec.
N1	2	1 x 10^{13}	850
N2	2	1 x 10^{13}	900
N3	2	1 x 10^{13}	950
N4	2	1 x 10^{13}	1000
N5	2	1 x 10^{13}	1050

Sample	Si^{29+} energy (MeV)	implant dose (cm^{-2})	RTA (°C)/ 10 sec.
N6	6	5×10^{12}	1000
N7	6	1×10^{13}	1000
N8	6	1×10^{14}	950
N9	6	1×10^{14}	1000
N0	11/10 MeV S/Si	1.5×10^{14} each.	1000

The as-received sample had ohmic contacts. Ohmic contacts for the 2 MeV samples were on a van der Pauw clover leaf geometry; but on the 6 MeV samples, they were placed at the four corners. The samples were obtained from Naval Research Laboratory, Washington D.C..

F. Electrical Activation

- Starting substrate : (100) and (211) GaAs:Cr
- Si^{29} implantation energy/ dose : 50 keV/ 4×10^{13} cm^{-2}
- Rotation angle : 45°
- Annealing mode : furnace (proximity using GaAs wafers as caps)
- Annealing temperature : no anneal, 200, 400, 525, 775, 850, and 1000 °C
- Annealing time/ ambient : 20 min./ 95% N_2 + 5% H_2

The as-implanted samples were received from Texas Instruments and proximity anneals were performed at VPI&SU.

4.2 Wafer Processing

Except for fat FETs (C), the as-received wafers were subjected to various cleaning steps. This was meant to remove organic and inorganic contaminants, including native oxides, from wafer surfaces. The surface cleaning of wafers is of paramount importance in forming contacts, both ohmic and

Schottky, with desirable and reproducible characteristics. Therefore, much time was spent in establishing sample cleaning procedures. At the beginning of the cleaning process, smaller pieces of 1cm x 1cm (approx.) sized samples were cut from the as-received wafers. The scribed samples were subjected to the following cleaning sequence :

(i) 5 min. in boiling trichloroethylene

(ii) 5 min. in warm acetone

(ii) 5 min. in methanol

(iv) rinse in de-ionized (DI) water

(v) 10 min. in 1:1 HCl:H_2O (by vol.)

(vi) rinse in DI water

(vii) blow dry with nitrogen

Subsequent to the above cleaning, the samples were promptly processed for contact metallization to facilitate electrical measurements.

4.3 Contact Formation

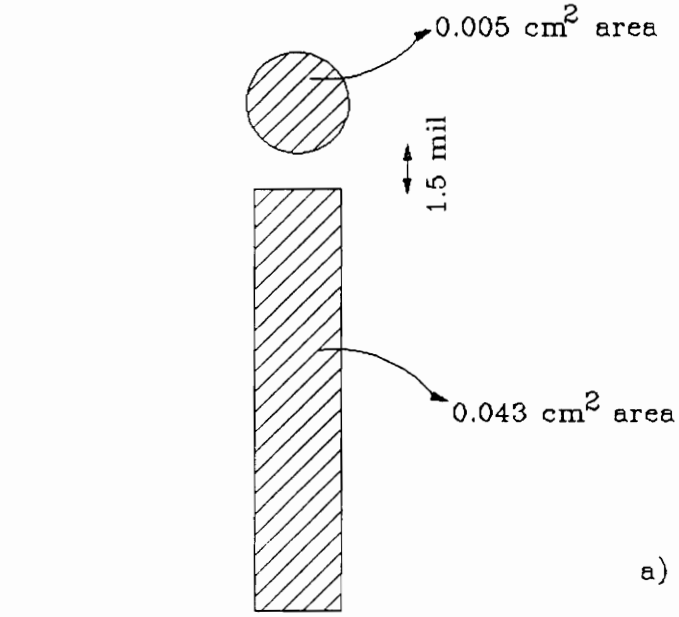
Two basic contacts, Schottky and ohmic, were formed on chemically cleaned GaAs surfaces. Transport or van der Pauw measurements require four ohmic contacts on a sample surface. The ohmic contacts were 1/32" in dia., and to minimize measurement related error, they were positioned as close as possible to the sample periphery [171]. DLTS measurements require a Schottky diode structure, consisting of both ohmic and Schottky contacts. There were initial difficulties in conducting DLTS measurements on Si implanted and annealed GaAs samples. This was due to poor Schottky diode characteristics which resulted in non-reproducible and non-reliable DLTS results. Invariably the DLTS spectra were noisy and devoid of any meaningful signal. With the exception of Schottky diodes on samples from group E and fat FETs from group C, this behavior was consistently observed in diodes formed on samples belonging to the A, B, D, and F families. What follows next are the sources for the difficulties in DLTS measurements and the methods adopted to circumvent them.

Problems: Schottky diodes formed on samples from categories A, B, D, and F had high series resistance and consequently high dissipation factor D (0.6-0.8). This value of dissipation rendered DLTS measurements on these diodes meaningless. For a reliable DLTS result, the condition of D << 1 should be satisfied. High values of series resistances in these diodes are attributed to shallow active layer thickness (up to ~ 0.2 μm) and wide separations between ohmic and Schottky contacts.

The closest separation between Schottky and ohmic dots that was possible using metal masks and alignment holes in the existing evaporation jig was ~ 2 mm. A similar spacing between the contacts of Schottky diodes on MeV implanted GaAs (group E) and Si doped LEC GaAs did not yield high dissipation values. The dissipation factors on such diodes varied between 0.1-0.15 and consequently the DLTS results on them are valid. A lower D value of these diodes is a result of a thicker active layer; 16 mils for the doped GaAs and several microns for the MeV implanted GaAs.

Solution: In order to perform valid DLTS measurements on samples from categories A, B, D, and F, efforts were made to reduce the effects of series resistance. After various experimentation and within the scope of existing facilities, the best course was to perform DLTS measurements on Schottky barriers with a back-to-back configuration on these samples. The configuration involves a series connection of small and large area Schottky contacts with the smaller contact dominating the effective capacitance, more so when the contact is reverse biased (refer to equation 2.10). Since current across a Schottky barrier scales as the contact area, the bigger contact owing to its larger area is ohmic-like. Using this geometry, the separation between two Schottky contacts could be reduced to 1.5 mil (see Fig. 4.1a). An aluminum mask was made incorporating this contact pattern. The back-to-back configuration not only simplifies processing (only one metallization) but most important of all, reduces the contact separation. The new pattern resulted in D values between 0.1-0.25. This is a significant improvement over the D values obtained with a diode configuration.

During DLTS measurements, the space charge under the smaller Schottky contact is modulated by pulse and bias sequence and therefore the DLTS results pertain to that region of the



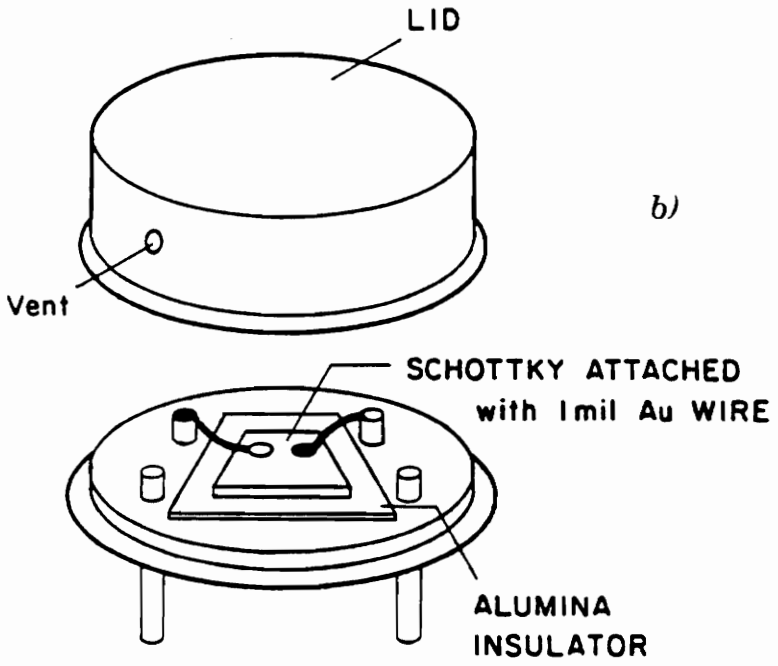


Fig. 4.1 a) A typical back-to-back Schottky geometry and b) packaged diode in a TO-8 header.

space charge. The space charge under the bigger Schottky contact is unaffected when the reverse biased smaller Schottky is momentarily pulsed to zero bias during DLTS, and therefore does not contribute to the capacitance transient. The DLTS results, discussed in Chapter 5, of GaAs samples belonging to groups A, B, and E were obtained via a back-to-back Schottky configuration. For samples from group F, the D values were still high (0.6-0.7) even with the new geometry. DLTS results on such samples lack validity and are therefore not included. For samples from group E, DLTS results were derived using Schottky diodes. For the fat FETs, the D values between gate(G) and source(S) contacts were low (refer to Table 5.6, Chapter 5) and hence DLTS measurements between G-S on such samples are reliable. Thus the DLTS results reported in Chapter 5 are obtained using either Schottky diodes or the two Schottkies back-to-back configuration, depending upon the severity of the effects of series resistance.

Contacting Techniques: The chemically cleaned GaAs samples, depending upon the type of measurements, were either subjected to ohmic or Schottky metallization on the active side. Ohmic dots were defined using a metal mask by evaporating Au:Ge (88% Au-12% Ge) alloy from a tungsten boat. An 1800 Å thick Au:Ge layer was deposited per run, followed by a 600 Å thick layer of Ni to form the annealing cap. Ohmicity to the Au:Ge/Ni dots were induced by annealing the samples at 440 °C for 2 min. under a flow of forming gas (95% N_2 + 5% H_2).

Al Schottky contacts of 1500 Å thickness were deposited by thermal evaporation through a metal mask. Both Schottky and ohmic evaporations were performed in a Denton-503 evaporator. The system is equipped with mechanical and diffusion pumps; and also a liquid nitrogen cold trap to prevent back streaming of diffusion pump oil and other hydrocarbons into the high vacuum chamber. A Varian quartz crystal thickness monitor, model Kronos QM-311 and a rotating shutter were used in conjunction to control the thicknesses of evaporated films. The vacuum prior to every evaporation was ~ 2×10^{-6} torr. Extreme precautions were taken to keep the evaporator and the sample processing arena clean so as to avoid external contaminants from effecting the contact integrity. Following

evaporation, the samples were withdrawn by venting the chamber using dry nitrogen.

Packaging: The GaAs samples with appropriate ohmic and Schottky contacts on them were packaged in a TO-8 header for electrical measurements. Both DLTS and van der Pauw samples were mounted on alumina substrates into a TO-8 package using a Si base thermally conductive grease. The purpose of the alumina substrate is to act as an insulator and insure against a common ground through the sample back. Electrical contacts between sample and header were achieved using 1 mil thick Au wire and attaching it by means of an Epo-Tek H20E electrically conductive epoxy. The epoxy was thermally cured, in nitrogen, at 150 °C for 5 min.. A schematic of a mounted diode on a TO-8 header is shown in Fig. 4.1b. The resulting packaged device was ready for electrical characterization.

4.4 Electrical Characterization System

Owing to the nature of electrical measurements and a large number of samples involved in the research, it is almost mandatory to use an automated test station for electrical analysis. Such a station would not only simplify data acquisition and data processing but would also help minimizing irreproducibility due to measurement errors. This set up was designed and implemented by Cole and Johnson and a detailed description of hardware and software aspects of the system is provided in references [174] and [175]. The system was given the name MEDUSA (Materials and Electronic Device and Unified System Analyzer). Since almost all the experimental data for this research was acquired using MEDUSA, it is imperative to discuss some of the key features of the system.

MEDUSA employs an IBM PC-AT which is interfaced with various measurement instruments via an IEEE 488 bus. The hardware layout of the system is shown in Fig. 4.2. The system can perform experiments belonging to different experimental groups such as capacitance and conductance against time (C-t, G-t), against voltage (C-V, C-G), current versus voltage (I-V), van der Pauw measurements, and four-point resistivity over a range of temperature (T = 10 K - 600 K). The measurements on packaged samples were carried out in a closed cycle, He cooled, CTI model 22

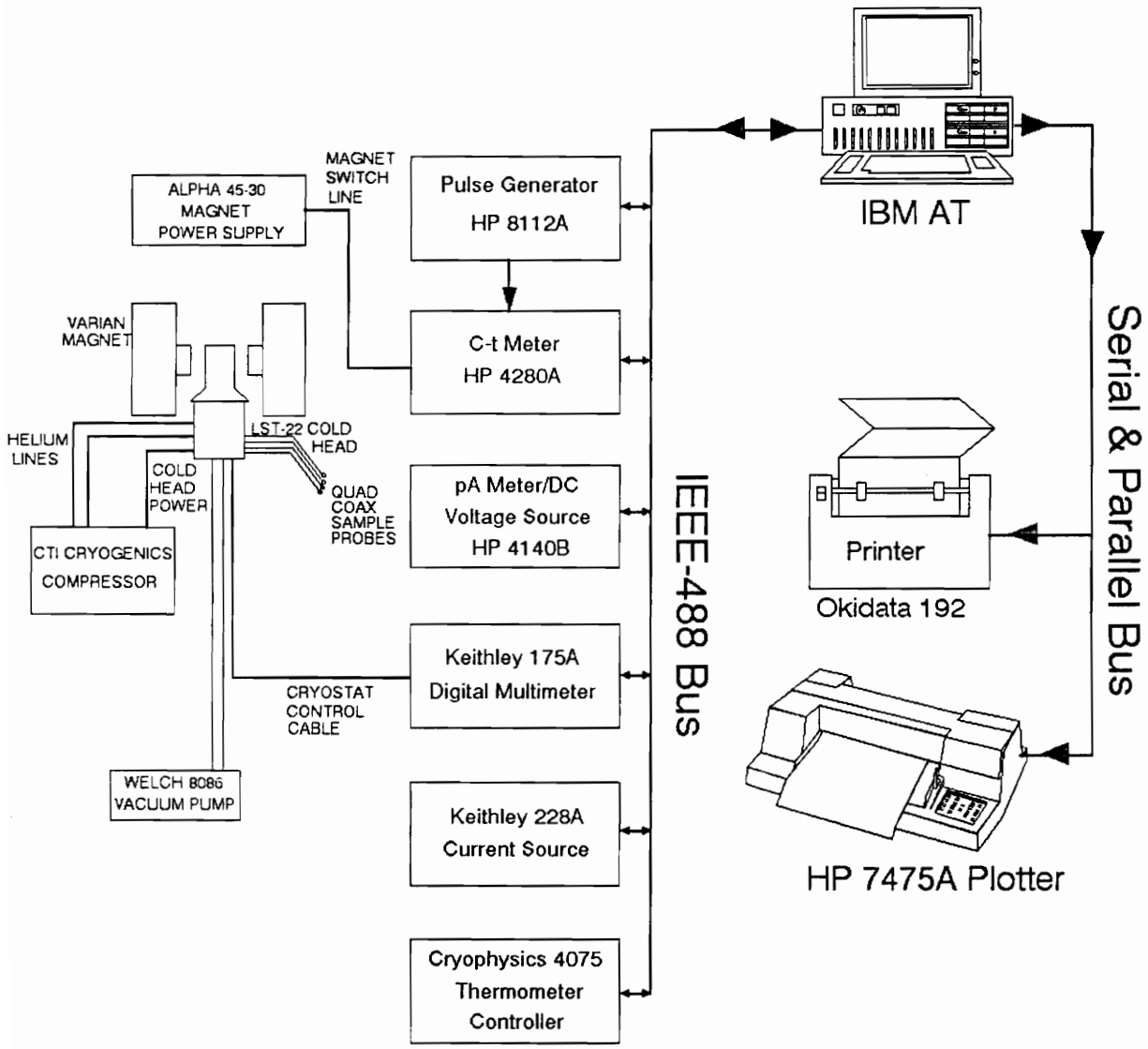


Fig. 4.2 Hardware layout of MEDUSA [175].

cryostat. The temperature in the cryostat was varied by means of a CTI compressor and a Cryophysics Inc., model 4075 temperature controller with a temperature control of ± 0.2 K. During a temperature scan, the computer sets and controls the temperature through the temperature controller via IEEE-488 bus.

MEDUSA software contains four main modules; a controlling batch file (MEDUSA.BAT), a parameter selection routine (PARAMETER), an experimental measurement routine (RUNIT), and a graphics routine for data processing and plotting (GRAPHICS). A comprehensive description of the MEDUSA software can be found in reference [175]. The software is written in Better Basic and is very user-friendly. The flow diagram of MEDUSA batch file that links to various program modules is depicted in Fig. 4.3. The parameter routine allows the user to choose experiments and set parameters for the experiments chosen. The RUNIT routine does the actual measurements on selected experiments and acquires data. The graphics routine processes the raw data and plots appropriate graphs through HP 7475 A plotter. There are twenty eight different graphs that are derivable from the graphics routine.

MEDUSA provides a wide scope for electrical analysis and a significant portion of its experimental menu was used in generating data for this research. The electrical measurements performed in this study and instruments used for specific tasks are listed in Table 4.1.

4.5 Electrical Measurements

The GaAs samples with appropriate contacts (Schottky, ohmic or both) and mounted on TO-8 headers were positioned in the cryostat, one at a time, for electrical characterization. A brief overview of various electrical measurements, performed in this research, are discussed in this section.

4.5.1 Current-Voltage Measurements

Current-Voltage (I-V) characteristics of Schottky barrier diodes were determined using a HP 4140 B pA Meter/DC Voltage Source. The instrument has a current measurement range of $1x10^{-15}$ -

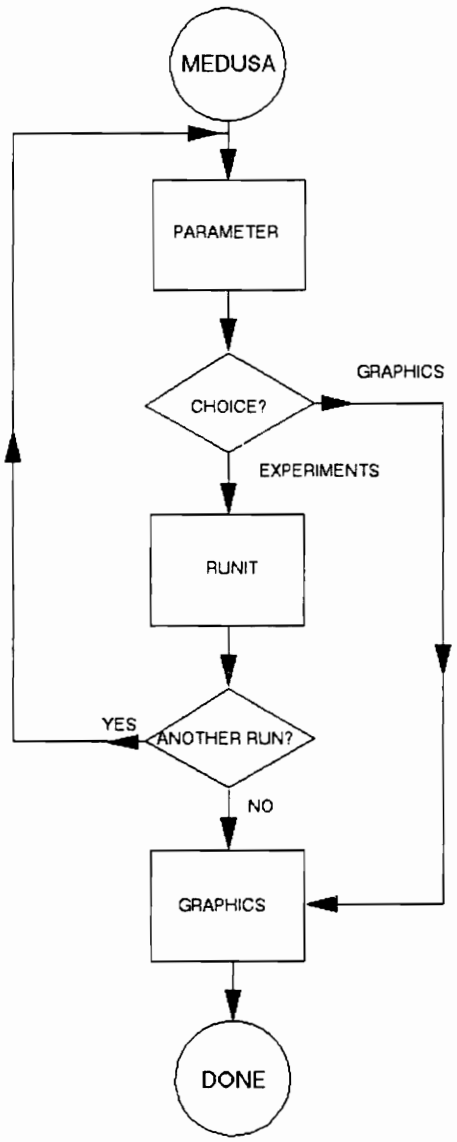


Fig. 4.3 Flow diagram of MEDUSA batch program [175].

Table 4.1. Electrical measurements and their associated instruments in MEDUSA.

Measurements	Instruments
DLTS	HP 4280 (C-t/C-V meter) HP 8112 A pulse generator
C-T, G-T, C-G-V	HP 4280 (C-t/C-V meter)
I-V	HP 4140 pA meter
van der Pauw	HP 4140 pA meter Kiethley 195 A multimeter Varian electro-magnet

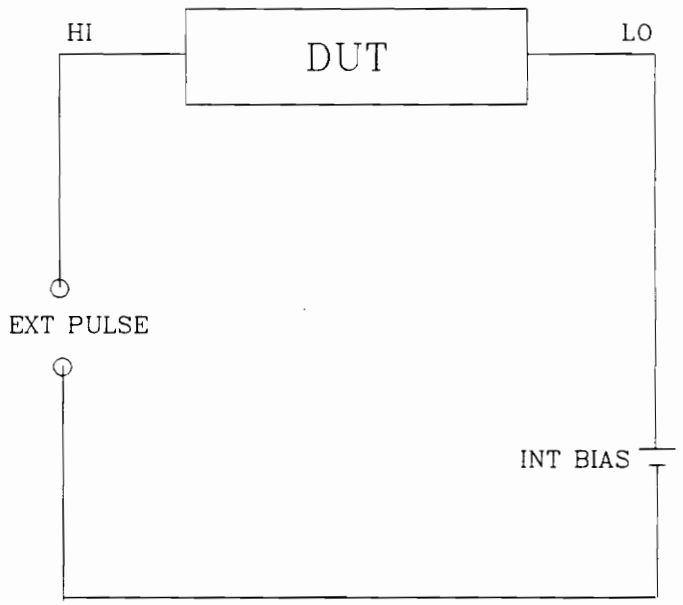


Fig. 4.4 Connection mode for the C-meter, pulse generator, and the diode (DUT) during a DLTS measurement.

$1.999x10^{-2}$ amps with a basic accuracy of 0.5%. The voltage source of the instrument can provide bias between -100 to + 100 V to the device under test (DUT) with a voltage resolution of 0.01 V. The parameters for I-V measurements were fed into the system controller (IBM-PC AT) and the experimental run, data acquisition, and data storage were all accomplished by the computer through the IEEE 488 bus. The parameters, for example, start bias, stop bias, and step bias along with the delay time between measurements and the initial hold period were specified prior to an I-V run. The experimental data and their associated parameter values were all stored in an user-defined output file name. For the temperature scan, the start, the stop, and the step temperature parameters were selected prior to the start of the experimental run. The sample first cooled down to the specified minimum temperature of the scan and subsequent to the completion of one I-V measurement cycle at that temperature, the sample temperature was raised by the specified step temperature and the complete I-V measurement cycle was once again performed. The entire process was computer controlled and it lasted till the I-V measurement was completed at the maximum temperature.

4.5.2 Capacitance and Conductance Measurements (C-G-V, C-G-T, DLTS)

The Schottky barrier capacitance of the samples was measured using a Hewlett Packard 4280A 1MHz C-Meter/C-V Plotter, which can measure capacitance (C) and conductance (G) of a DUT as a function of the constant dc bias, the swept dc bias, or the time after the application of a bias pulse. The maximum C and G values that can be measured using 4280A are 1.9 nF and 12 mS, respectively. The basic measurement accuracy is 0.1% and the measurement resolution of the instrument is 1 fF on the most sensitive range. The 4280A C-V meter has a built-in dc source which can output 0 to ± 100 V with a voltage resolution of 0.01 V. The test signal for C and G measurements was 1 MHz 30 mV rms sine wave.

The C-V measurements primary utility is in the determination of the doping profile. G-V measurements although do not directly result in the derivation of any desirable parameters, the measurement is useful in obtaining a diode's D value. In case the G values are high, appropriate

corrections become mandatory in the corresponding C values, or else the deduced doping profile will be erroneous. To monitor the diode's quality factor during C-V or C-T measurements, the corresponding G-V or G-T measurements, with identical parameters, were always performed. The measurement procedures were similar to those described for I-V, where the parameters such as start bias, stop bias, step bias, hold time, and measurement delay times were fed into the computer at the beginning of the experimental run. The temperature dependence of C and G (C-T, and G-T) were done by specifying the appropriate biases and temperatures (start, stop, and step) and then letting the computer control the entire measurement process.

The concept of the DLTS measurement is to record the capacitance transient at each selected temperature and to store the sequentially acquired transient data for subsequent analysis. The HP 4280 A C-meter was used to measure the capacitance transients and by using an external pulse generator (HP 8112 A) in conjunction with HP 4280 A, transients as short as 10 μsec could be measured. The connection mode between the C-meter, the pulse generator ,and the DUT during C-t measurements is shown in Fig. 4.4. The experimental parameters during DLTS were defined by the following program input values :

(i) reverse bias (start, stop, and step)

(ii) pulse bias (high, low, and step, (-7 to +7 V))

(iii) step delay time (≥ 10 μsec)

(iv) pulse bias width (initial, final, and step (≥ 10 μsec))

(v) number of capacitance readings as a function of time

During a DLTS measurement, the HP 8112 A outputs bias pulses with a typical transition of 5 nsec for leading and trailing edges. The HP 4280 A provides a TTL level signal at the start of a C-t mode measurement to the pulse generator. The duration of the signal being equal to the pulse bias width, chosen as a parameter. This signal is used to synchronize the pulse biases from HP 8112 A with the measurement.

On completion of recording the capacitance transients over the temperature range (typically

100 - 400 K), MEDUSA then enters into the GRAPHICS routine for data analysis. In this routine two different delay times (t_1 and t_2) are selected (i.e. fixing the rate window) and the difference in capacitance values at these two time instants is plotted as a function of temperature. The resulting plot is a DLTS spectrum with a rate window specified by t_1 and t_2. The sensitivity of the DLTS system is 10^{-3} ,i.e. any traps with concentrations less than 10^{-3} times the doping density cannot be detected.

4.5.3 van der Pauw Measurements

The packaged samples with four corner ohmic contacts were characterized for transport properties using the van der Pauw technique. For this purpose, current, between one pair of contacts, was supplied from HP 4140 B pA meter/DC voltage source and the voltage drop across the other pair (V) was recorded using Model 195 A Kiethley Digital Multimeter. The Model 195 A has a resolution of 100 nV in the most sensitive range (20 mV). The current value (I) was specified as a parameter and the HP 4140 B voltage source would keep incrementing its bias (usually by .01 V) until the current level either became equal to or just exceeded the value of the set parameter. The actual current (I) and the measured voltage (by 195 A multimeter) were recorded for one configuration, shown in Fig. 2.6., and the procedure was repeated for other configurations as well. The value of the magnetic field applied perpendicular to the sample in configuration (c) (see Fig. 2.6) was set at 3400 Gauss. The magnetic strength of the electromagnet could be varied by adjusting the magnet power supply to proper current. The experimental data in (I-V) pairs were then processed in the Graphics routine to derive resistivity, mobility, and carrier concentration values.

For profile measurements, the samples were etched in 1 : 1 : 100 conc. H_2SO_4 : 30 % H_2O_2 : H_2O solution , usually for 10 secs. (or more depending upon the layer thickness to be removed) and remeasured by van der Pauw method to determine the transport characteristics. The etch and measure procedure was repeated until all the active layer thickness was etched away. Knowing the average values of carrier concentration, mobility, and resistivity after each successive etch, their depth dependent characteristics were obtained by using equations (2.39) to (2.41) (Chapter 2).

CHAPTER 5. RESULTS AND DISCUSSION

The experimental results addressing the research objectives are presented in this chapter. First, the effects of substrate variables and buffer layers on the electrical properties of GaAs are discussed. The results related to the effects of implant parameters, electrical activation, and damage recovery are discussed next. Wherever possible, attempts have been made to compare the results of this research with those reported in the literature.

5.1 Substrate Variables

Ion implantation of dopants into semi-insulating (SI) GaAs and subsequent annealing is a widely used technique to form conducting channels in MESFETs. The defects induced into the channel and the substrate as a result of implantation and/or annealing can have detrimental effects on the performance of FETs and other similar devices. These defects depend strongly on the processing methods and the type of the starting substrate. It is therefore very important to understand the defect characteristics and their relation to processing parameters and substrate variables. Understanding of this behavior is imperative to produce devices with optimum performance. This section will focus on the effects of substrate variables on the electrical characteristics of ion-implanted and annealed GaAs layers. It is known that substrate stoichiometry and preexisting flaws can influence the presence and annealing out of implantation related defects. The substrates compared in this section are (100) and (211) oriented undoped and Cr-doped liquid encapsulated Czochralski (LEC) SI GaAs. This study compares the effects of substrate orientation, (100) and (211), and substrate type (undoped or Cr-doped LEC) on the electrical properties of ion implanted active layers. Following the conclusion of this comparison, the effects of buffer layers (low temperature GaAs and $Al_{.35}Ga_{.65}As$) on the electrical characteristics of ion-implanted GaAs channels will be addressed in detail.

5.1.1 (100) vs. (211) undoped LEC GaAs

For Si-implanted GaAs MESFETs, (100) is the traditional substrate orientation. Recently it has been reported by Banerjee *et al.* [130] that MESFETs on (211) substrates have higher transconductance and lower noise figures. This behavior is attributed to the unique carrier concentration profile for (211) surface, as compared to (100). The occurrence of a non-Gaussian carrier concentration profile in (211) with a natural n^+ surface region has been reported [130].

In this section results on (100) and (211) GaAs are compared. The processing conditions of the samples were discussed in Chapter 4 under category A. Both sample sets have received identical Si-implantation (50 keV at 1.7 x 10^{13} cm^{-2}) and RTA annealing. Transport (van der Pauw) and deep level transient measurements (DLTS) were performed to discern the differences in electrical behavior of (100) and (211) GaAs surfaces.

5.1.1a Transport Characteristics

Carrier concentration and Hall-mobility profiles for (100) and (211) orientations are shown in Figs. 5.1a and 5.1b, respectively. The carrier profile is somewhat steeper near the implant tail for (211) than for (100). It is interesting to note that the flat profile in (211) between 200 Å and 1000 Å, as reported in [130], is not evident in this sample. Instead, the carrier profile of (100) is flatter than (211).

The temperature dependence of Hall parameters (i.e. resistivity, mobility, and carrier concentration) in (100) and (211) GaAs are shown in Figs. 5.2, 5.3, and 5.4, respectively. These results refer to samples that were RTA annealed at 850 °C for 30 seconds. The Hall parameters behave in the expected way against temperature but (100) GaAs show higher mobility and lower resistivity than (211) GaAs at all measurement temperatures. The lower conductivity in (211) is also confirmed through photoconductivity measurements done on identical samples [176]. The differences in mobility and resistivity in the two orientations are attributed to higher damage density in (211)

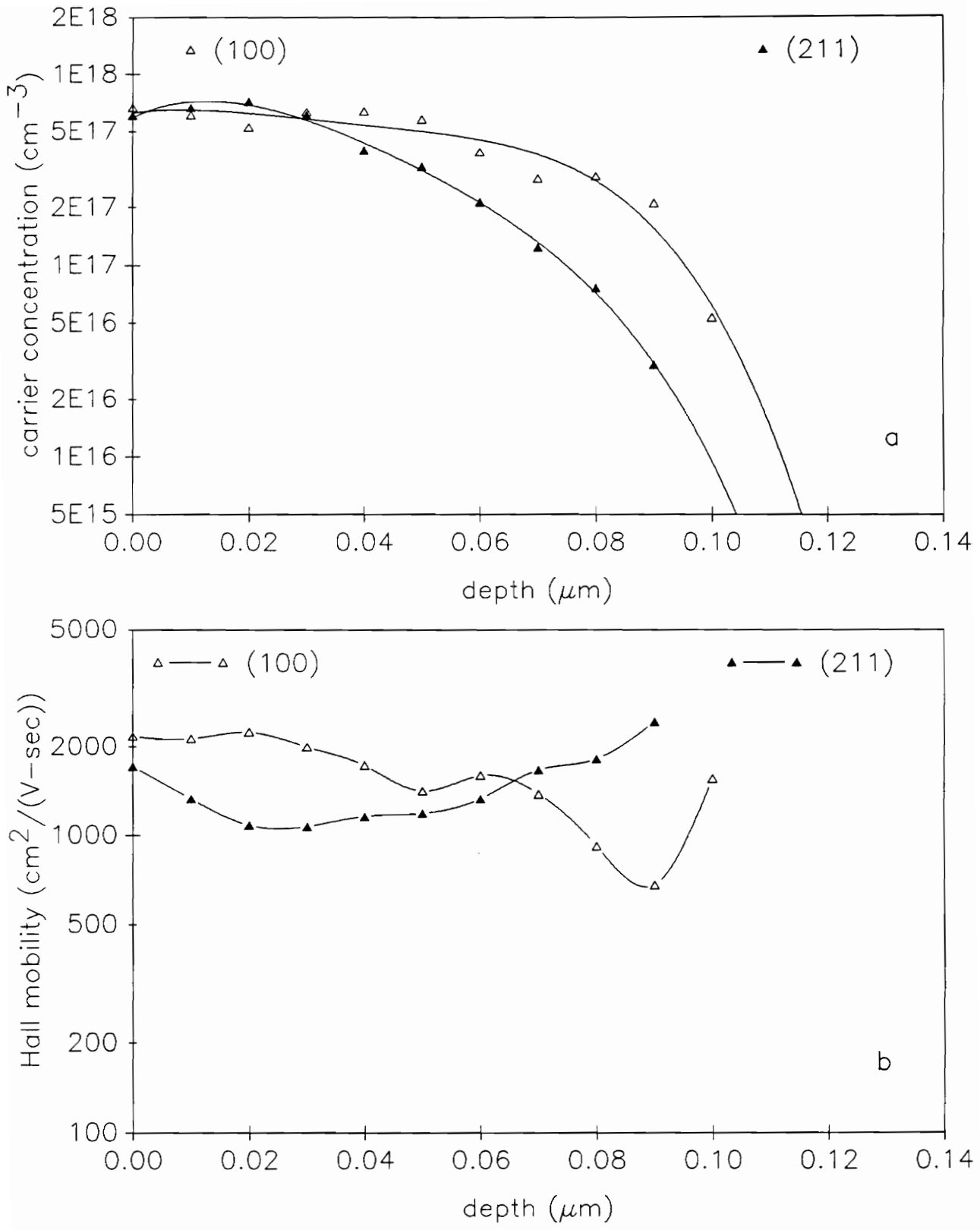


Fig. 5.1 Transport characteristics of 50 keV Si-implanted and 850 °C RTA (100) and (211) GaAs : a) carrier concentration profiles and b) mobility profiles.

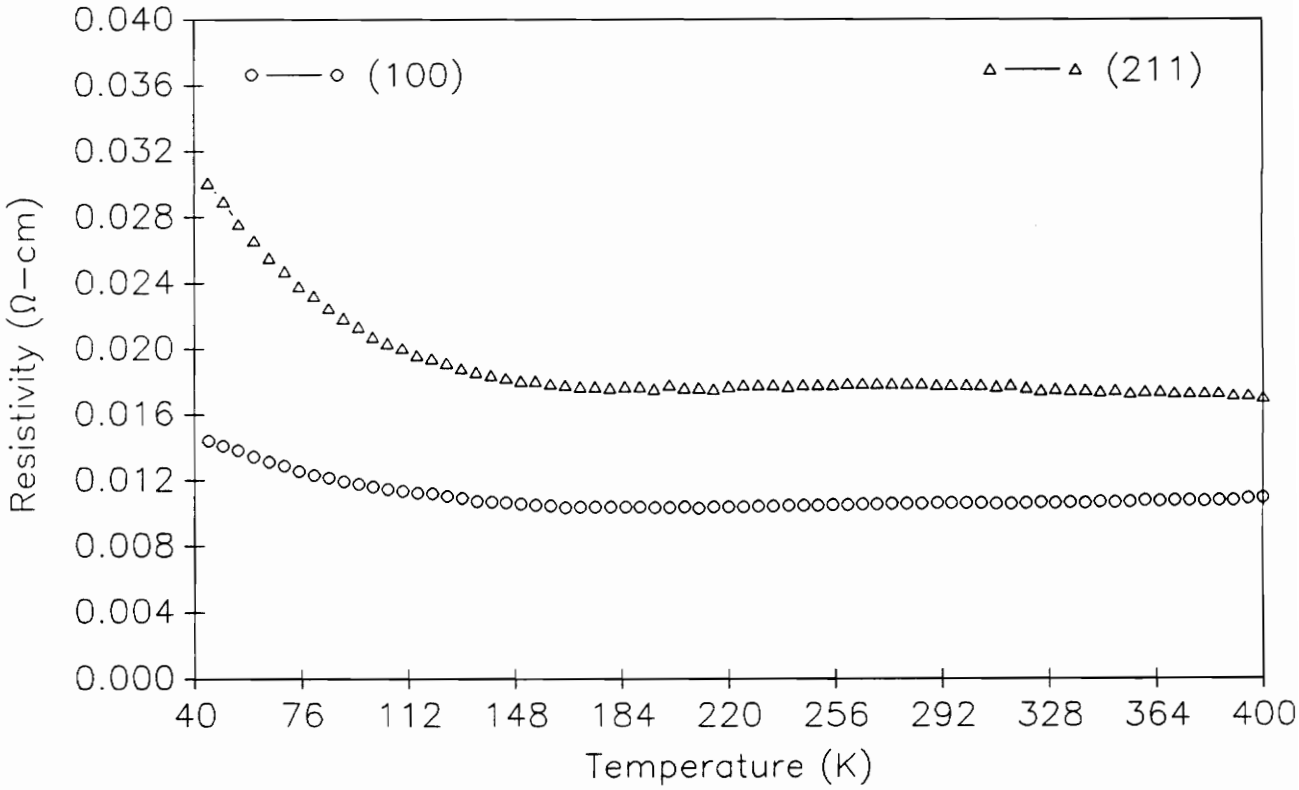


Fig. 5.2 Temperature dependence of resistivity of 50 keV Si-implanted and 850 °C RTA (100) and (211) GaAs.

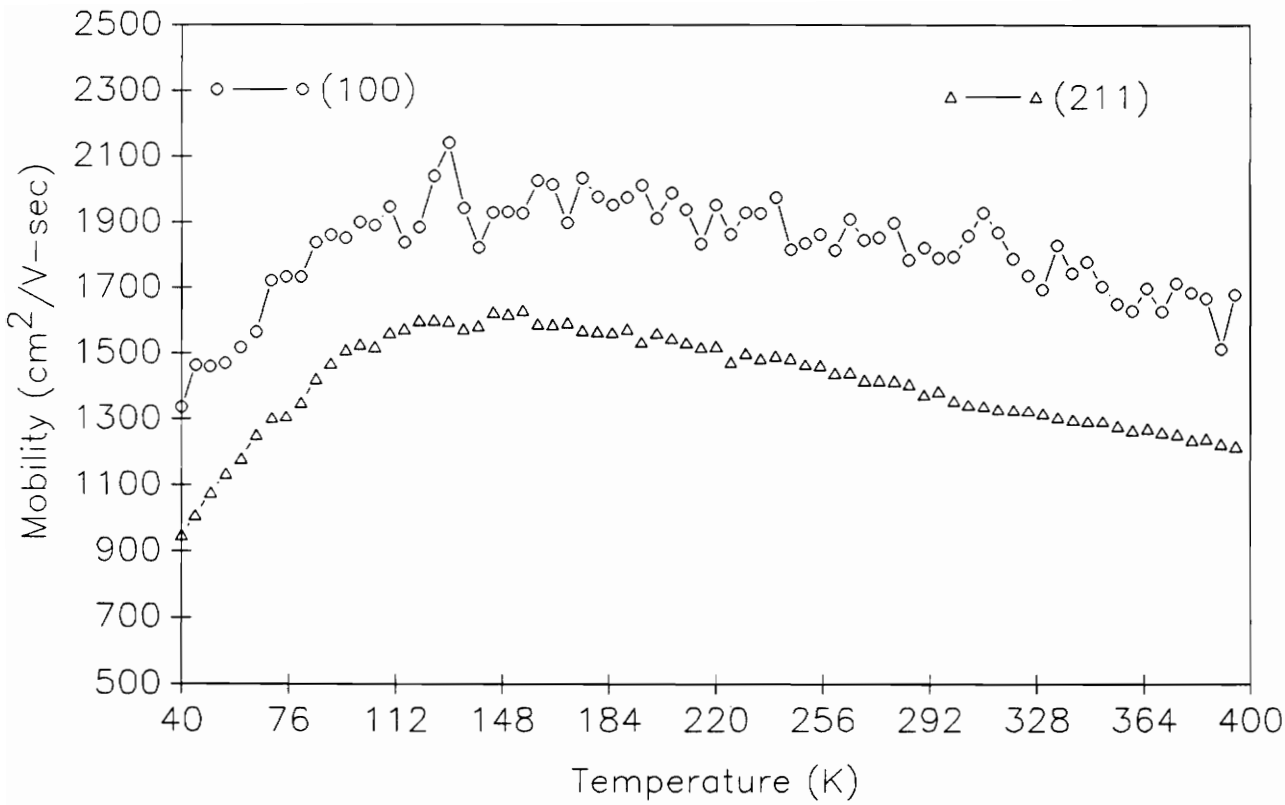


Fig. 5.3 Temperature dependence of Hall mobility of 50 keV Si-implanted and 850 °C RTA (100) and (211) GaAs.

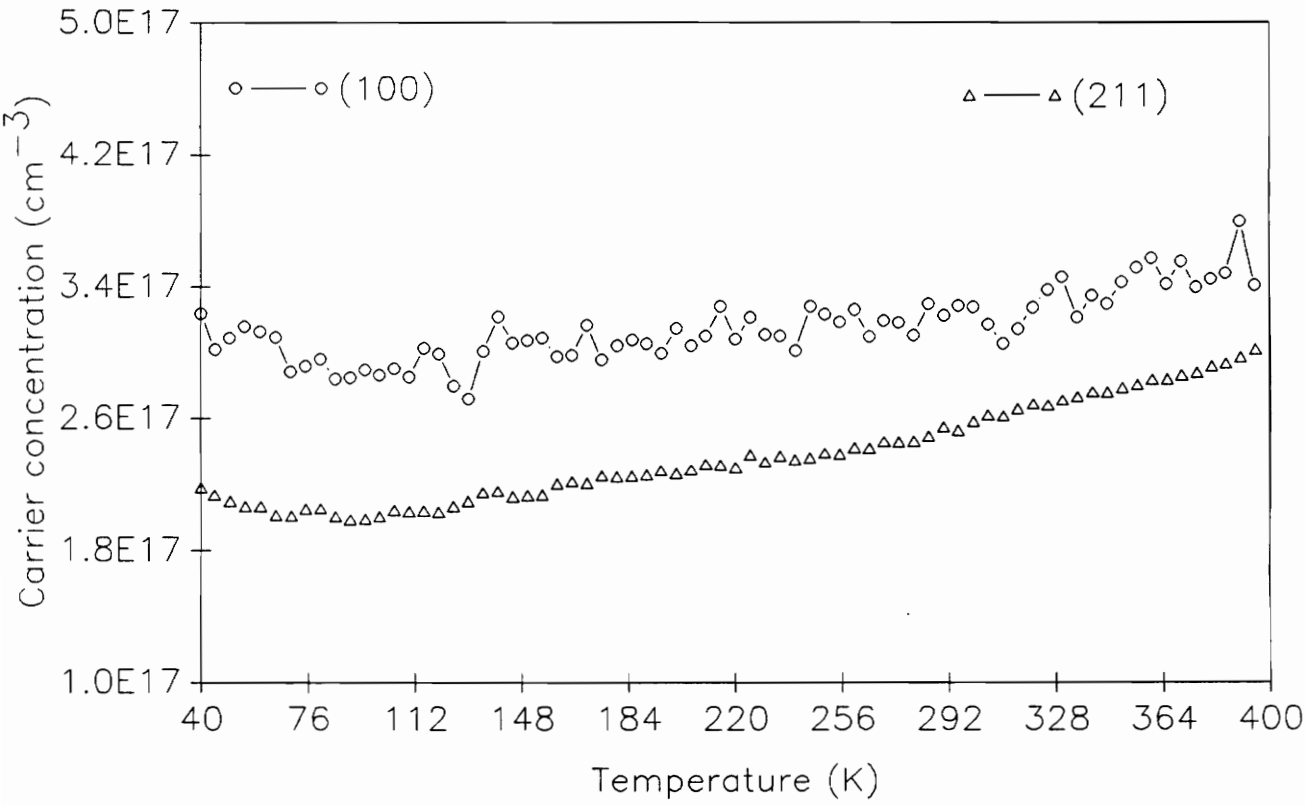


Fig. 5.4 Temperature dependence of carrier concentration of 50 keV Si-implanted and 850 °C RTA (100) and (211) GaAs.

GaAs than in (100) GaAs [132]. Bhattacharya *et al.* [132] have reported that the damage recovery of (211) crystals is slower and the microtwins in them are more stable than in (100). In their study, Si-implanted (211) GaAs annealed under a Si_3N_4 cap had residual damage. This was contrary to the behavior of (100) GaAs, which showed RBS channeling spectra comparable to a virgin crystal. Optical measurements (Raman and UV) also revealed higher near-surface damage in (211) than in (100) GaAs [131].

To summarize the transport measurements, the effective mobility and conductivity of the active layer is lower for (211) than for (100) GaAs. This is consistent with a higher residual damage in (211) than in (100). The carrier profile in (211) GaAs does not agree with the unusual profile reported in reference [130].

5.1.1b Deep Level Characteristics

Electron traps in Si-implanted and RTA annealed (100) and (211) GaAs were characterized by using DLTS. The effects of rotation angle during implantation on deep level properties of (211) GaAs were also investigated. In this section the deep level characteristics of active layers on the following GaAs substrates will be considered:

1. (100) orientation, rotation angle=45°
2. (211) orientation, rotation angle=45°
3. (211) orientation, rotation angle=0°

The deep level parameters (namely the trap activation energy ΔE (E_C-E_T), the capture cross-section σ_n, and trap concentration N_T) are derived from capacitance transient measurements at several temperatures. The measurement parameters are adjusted so that a large reverse bias is avoided. A large reverse bias would generate large reverse current (due to field emission) causing a

large ohmic drop in the neutral material which would make the capacitance measurements prone to error. The DLTS results presented here are representative of the several samples characterized.

It is well known that stoichiometry of the original substrate can influence the defect characteristics of the active layers subsequently formed. A typical DLTS spectrum of a Si doped (100) LEC GaAs is shown in Fig. 5.5. The measurement parameters used in this run are also included in the figure. There is one major electron trap with an activation energy of E_c-0.78 eV. The trap density N_T and capture cross section σ_- were found to be 7.6 x 10^{15} cm^{-3} and 2.95 x 10^{-14} cm^{-2}, respectively. The characteristics of this trap are similar to the well known EL2 center. This center is prevalent in LEC grown GaAs under As rich conditions. The origin of EL2 is believed to be related to antisite (As_{Ga} i.e. As on Ga site), defects [182]. Although the processing conditions of (100) and (211) GaAs samples to be investigated in this section are markedly different from that of Si-doped LEC GaAs, it may be noted that the defect spectrum in Fig. 5.5 is a typical representation of the deep level features in a GaAs substrate prior to any ion processing or thermal treatment. This spectrum may serve as a basis for comparison with the DLTS spectra obtained for samples after ion implantation and annealing.

Fig. 5.6. is the defect spectrum of a 50 keV Si-implanted (100) GaAs activated by RTA at 850 °C for 30 seconds. The experimental parameters used during DLTS measurements are also provided in the figure. The spectrum contains multiple emission peaks, one of which is EL2. Some of the defect peaks are not easily resolved, but contribute to the broad profile of the spectrum. The appearance of a broad DLTS signal is believed to be associated with complex defects rather than a well defined point defect. The two dominant electron traps, labelled A and B, in Fig. 5.6 are located at E_c-0.70 eV and E_c-0.83 eV from the conduction band. The characteristics of several electron traps in Fig. 5.6 are presented in Table 5.1, and possible similarities to the well documented trap levels are also listed. This comparison is helpful in relating the trap identity to their possible origins.

The trap level at E_c-0.83 eV corresponds to the emission signal from EL2. The creation of

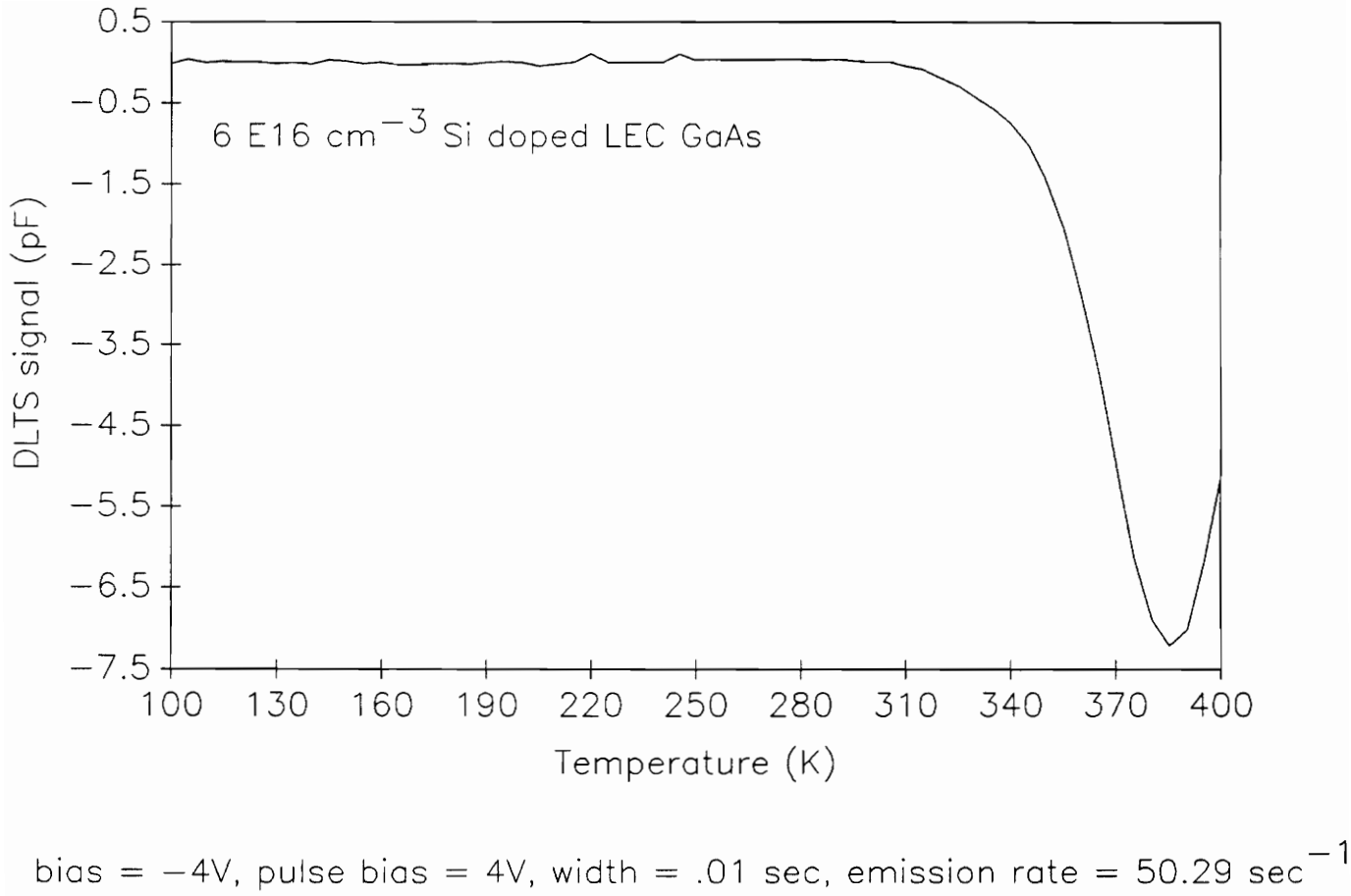


Fig. 5.5 DLTS spectrum of a Si doped (100) LEC-GaAs.

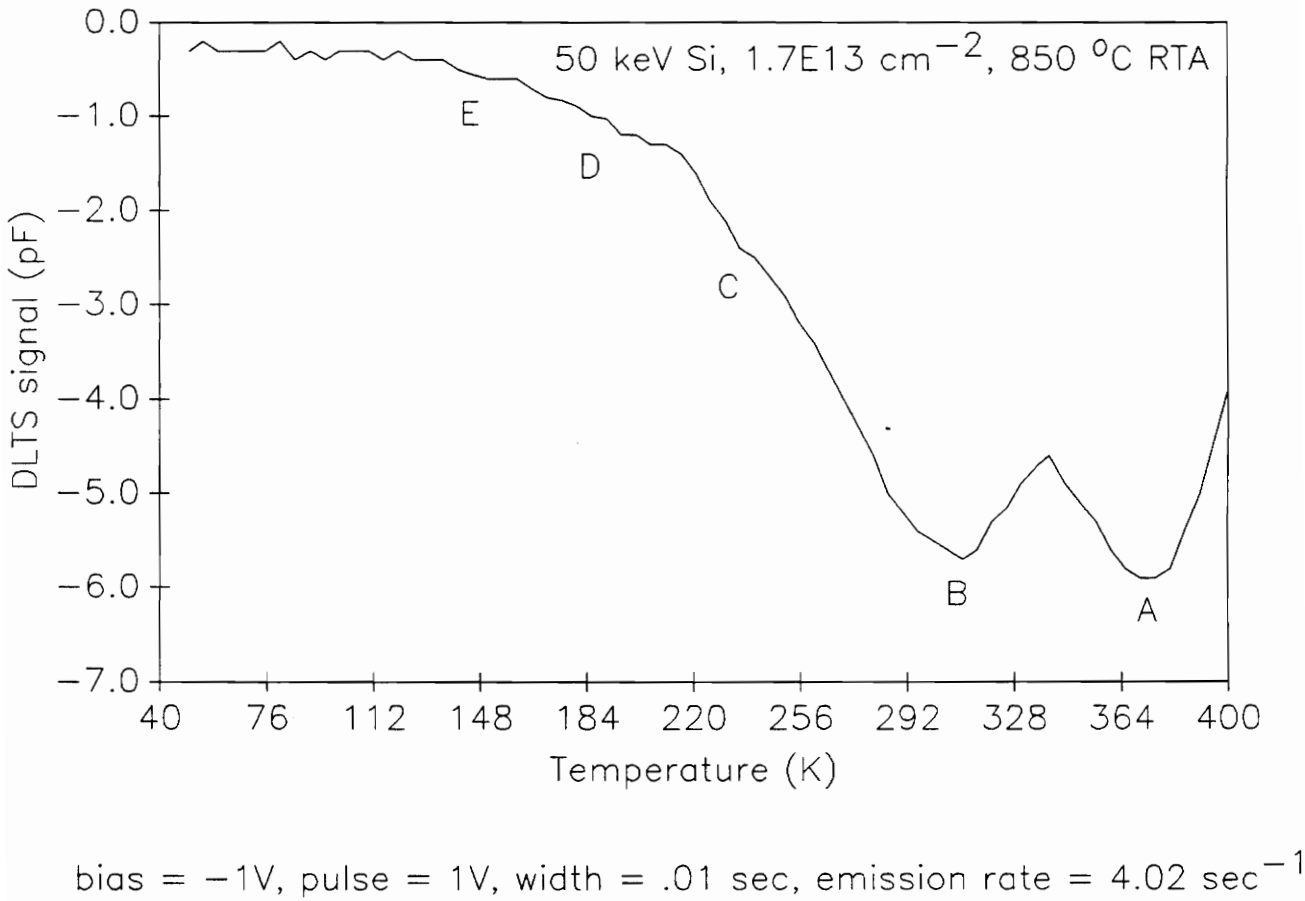


Fig. 5.6 DLTS spectrum of a Si-implanted and RTA annealed (100) GaAs (labels A-E are defined in text).

Table 5.1. Trap parameters of Si-implanted and RTA annealed (100) GaAs.

Depth	Label	E_C-E_T (eV)	N_T/N_D	Possible designation
0.14 μm	A	0.83	.055	EL2
	B	0.71	.054	EB4
	C	0.53	.022	EL4
	D	0.42	.0094	EL5
	E	0.33	.0052	EL6
			$\Sigma N_T/N_D = 0.145$	
0.153 μm	A	0.80	.047	EL2
	B	0.72	.055	EB4
	C	0.51	.018	EL4
	D	0.42	.010	EL5
	E	0.34	.005	EL6
			$\Sigma N_T/N_D = 0.135$	

an EL2 center by ion implantation has been reported in literature [49,177]. The observed EL2 level in the (100) GaAs sample may quite likely be the sum of the concentrations of EL2 caused by Si implantation and RTA and those existing in the original substrate. Ion implantation introduces both Ga and As vacancies as well as more complex dislocation networks. If EL2 is an As_{Ga} defect, then the following are possible reaction mechanisms involved in the formation of EL2 [49] :

$$As_{As} + V_{Ga} \rightleftharpoons As_{Ga} + V_{As} \qquad \text{and/or} \qquad As_i + V_{Ga} \rightleftharpoons As_{Ga}$$

where V_{Ga} is a Ga vacancy, As_i is an As interstitial, and As_{As} is As on As lattice site. It has been reported that the As_{Ga} defect or EL2 has an activation energy between E_c-0.78 eV and E_c-0.83 eV [43-45,101]. The implanted Si atoms preferably reside at Ga sites in competition with As_i. However, due to the implantation process, there are abundant Ga vacancies resulting from stoichiometry deviation. It is very likely that these Ga vacancies participate in the formation of As_{Ga} during subsequent activation annealing. Therefore it appears that the EL2 center, apart from being in the original substrate, is also closely associated with the implantation and annealing process.

The other dominant peak B is at E_c-0.70 eV and is similar to EB4 (0.71 eV) observed in electron and proton irradiated GaAs [14-16]. A similar defect center in high concentration has been reported in Si-implanted and furnace annealed GaAs:Cr [55]. This center appears to be a result of a residual defect after implantation and annealing, and its stability is apparently independent of the type of annealing (furnace or RTA). Wang *et al.* have attributed this level to impurity-vacancy complexes [181].

Remaining trap levels C, D, and E are approximately located at energy positions 0.53, 0.42, and 0.33 eV from the conduction band, respectively, and are analogous to EL4 (0.52 eV), EL5 (0.42 eV), and EL6 (0.33 eV) centers, respectively [179]. The EL4 level is a radiation-induced center since a similar defect (to be shown later) has also been observed in 4 keV Ar^+ bombarded GaAs. The occurrence of this center has been reported by Kitagawa *et al.* [2] in a similarly processed GaAs sample. Rhee, Bhattacharya, and Koyama observed the same trap in Si-implanted and furnace-

annealed active layers on Cr-doped GaAs substrates [38]. They consider this level to be an ion-induced defect state. A similar opinion about the origin of the 0.52 eV electron trap has been expressed by several researchers in separately published reports [65,178]. Li *et al.* observed this state at 0.52 eV in a proton-irradiated LPE n-GaAs, and has assigned this defect to complexes involving V_{Ga} and V_{As} [49].

The trap level D (EL5) appearing in relatively smaller concentrations has also been detected in Si-implanted and annealed GaAs [49,63,179]. A 60 keV Ar^+ irradiated GaAs after annealing at 500-600 °C has the identical defect [180]. The origin of EL5 in ion-processed and annealed GaAs is not well established but is believed to be associated with complexes involving Ga vacancies and donor atoms [49].

At this point it is worthwhile to mention that, unlike Si, the number of probable defect complexes in a compound semiconductor increases remarkably, and precise defect identification, if at all possible, becomes very involved. The trap labelled E at 0.33 eV has been detected in bulk GaAs before [34]. Wang *et al.* [181] have found this defect, in small concentration, in Se implanted and annealed GaAs. The origin of this center is not fully understood but there are reports of its relationship with a single Ga vacancy [33].

The DLTS measurement conducted on the same (100) GaAs at 2V reverse bias (probe depth ~ 0.15 μm) revealed no new trap levels other than those observed at 1V. The only noticeable change was the reduction in peak intensities of the A (0.84 eV) and B (0.70 eV) levels. The trap parameters deduced for this region of space charge are also presented in Table 5.1. A rough estimate of total relative trap concentration ($\Sigma N_T/N_D$) at probed depths is about 0.13 - 0.15.

The DLTS response of a 50 keV Si-implanted and RTA (850 °C for 30 sec.) annealed (211) GaAs is shown in Fig. 5.7. Although the measurement parameters are identical to those used for (100), the spectrum for (211) appears broader. The appearance of a broad DLTS signal is indicative of the fact that the traps are closely spaced in energy and are somewhat distributive in nature. There

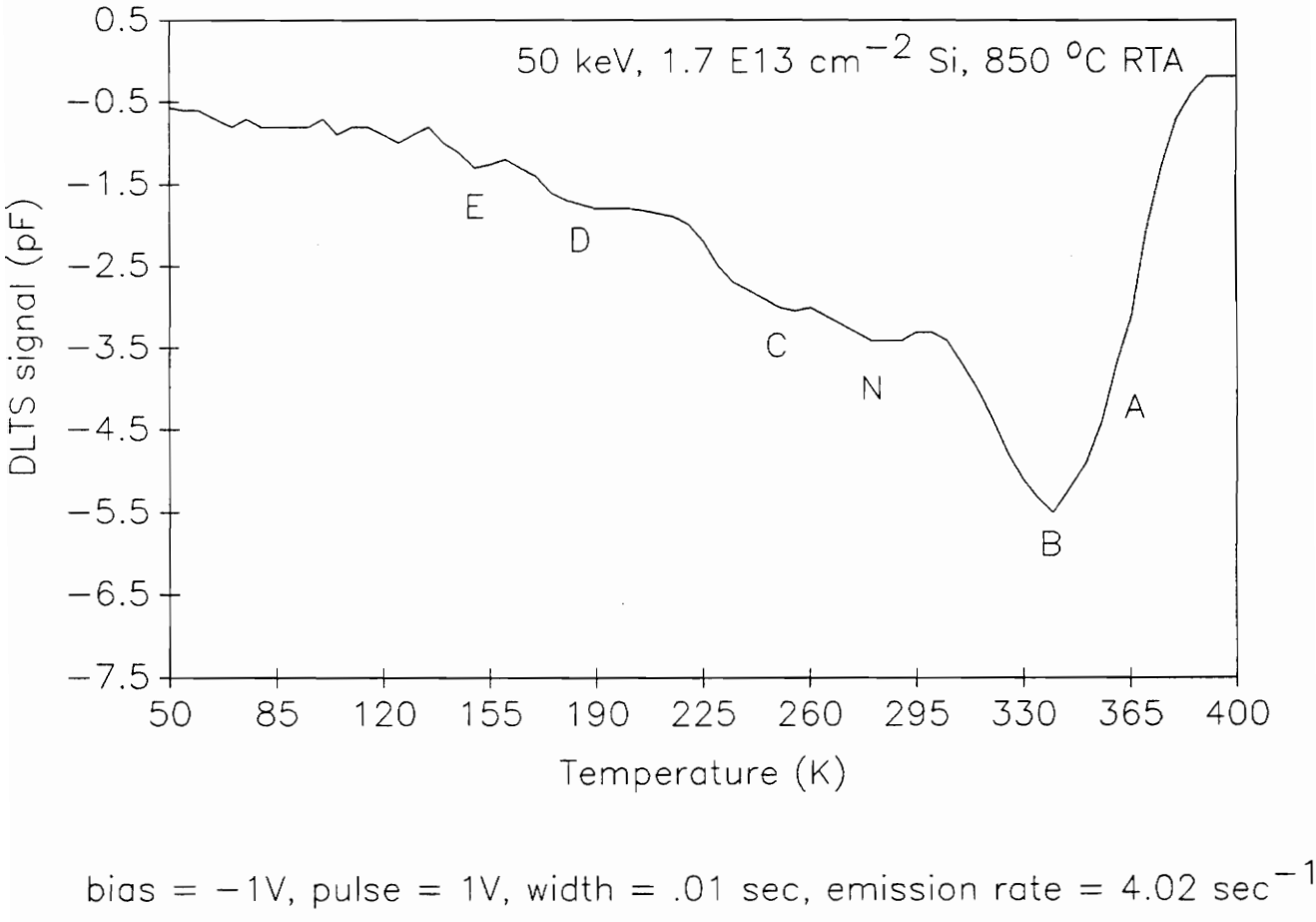


Fig. 5.7 DLTS spectrum of a Si-implanted and RTA annealed (211)-45° GaAs (labels A-E are defined in text).

Table 5.2. Trap parameters of Si-implanted and RTA annealed (211)-45° GaAs.

Depth	Label	E_C-E_T (eV)	N_T/N_D	Possible designation
0.14 μm	A	0.83	.030	EL2
	B	0.77	.052	EB4 (?)
	N	0.63	.032	?
	C	0.56	.028	EL4
	D	0.42	.016	EL5
	E	0.33	.011	EL6
			$\Sigma N_T/N_D = 0.169$	
0.16 μm	A	0.81	.046	EL2
	B	0.76	.040	EB4 (?)
	N	0.65	.037	?
	C	0.55	.038	EL4
	D	0.47	.040	EL5 (?)
	E	0.34	.014	EL6
			$\Sigma N_T/N_D = 0.215$	

are several trap levels noticeable in the spectrum with varying signal intensities. The spectrum probes to a depth of ~ 0.14 μm from the surface. The trap characteristics and their comparison with better known deep levels (see Table 3.4) are listed in Table 5.2. Comparing Table 5.2 with Table 5.1, it appears that the sum total concentration of deep levels is higher in (211) than in (100) GaAs orientation.

The most prominent level (B) in Fig. 5.7 is located at E_c-0.76 eV. This is similar to EB4 observed in (100) but with a slightly lower emission rate. The other trap levels in (211) are approximately at E_c-0.34 (EL6), E_c-0.42 (EL5), E_c-0.56 (EL4), and E_c-0.83 (EL2). Similar trap states were also observed in the (100) spectrum. The trap level, N, at E_c-0.63 eV is a new center and was not seen in (100). Except for the substrate orientation, the (100) and (211) samples had identical implantation and annealing procedures. The new 0.63 eV center in (211) therefore appears to be influenced solely by the substrate orientation. A DLTS experiment conducted at a higher reverse bias (3V) on (211) showed no additional electron traps other than those identified at 1V, and similar to the results with 1V, the DLTS signal continues to remain broad. The depth of the space charge region at 3V reverse bias is approximately 0.16 μm. The trap characteristics corresponding to this probe depth are also summarized in Table 5.2.

It is important to discuss the significance of a higher total relative trap concentration in (211) than in (100), both being 50 keV Si-implanted and 850 °C RTA-annealed. The higher relative trap concentration is consistent with the fact that the residual damage, as discussed before, is greater in (211) than in (100). The higher density of deep levels in (211) GaAs may also account for the lower mobility observed on such substrates (refer to section 5.1.1a).

The DLTS results discussed so far for (100) and (211) substrates were for the case where the angular rotation during implantation was maintained at 45°. The DLTS results presented next are for the (211) substrate whose rotation angle during implantation was kept at 0°. The other implantation and annealing parameters remain the same as in the previous two samples. The DLTS

spectrum of this sample is shown in Fig. 5.8. The spectrum indicates the presence of six electron trap levels: A (0.80 eV), B (0.75 eV), N (0.63 eV), C (0.51 eV), D (0.42 eV), and E (0.33 eV). Some of the identified levels appear as shoulder to the broad spectrum and therefore, their energy positions are approximate. The details of the trap characteristics and their possible correlation to better known electron levels are presented in Table 5.3. The spectral features of Fig. 5.8 are very similar to Fig. 5.7, with a prominent peak B, being EB4, located at E_c-0.75 eV.

There is no noticeable difference in the trap levels deduced for (211) substrates with 0° and 45° angular rotation. The total relative trap concentrations at probing depth of 0.14 μm are nearly the same in both cases. At a depth of 0.16 μm, however, the relative trap concentration is somewhat higher for (211) with 45° rotation angle. The higher relative defect concentration for 45° rotation at greater depths may be due to a more diffused nature of implant damage. Based on the trap parameters obtained for (211) with different angular rotation (refer to Tables 5.2 and 5.3), it may be inferred that the angular rotation (0° and 45°) during ion implantation has no appreciable effect on the deep level behaviors of the active layers formed on them.

One interesting observation emerges on comparing Tables 5.1, 5.2, 5.3, and 5.5 : the sum total relative electron trap concentration obtained, is higher in undoped GaAs than in Cr-doped GaAs substrates, and is true for both (100) and (211) orientations. It is important to mention that the channel thickness is approximately 0.15-0.16 μm as result of 50 keV Si implantation and RTA annealing. The space charge width at zero bias is about 0.12-0.13 μm deep and is therefore very close to the channel-substrate interface. The DLTS results discussed so far pertained to the region of probe between 0.12 and 0.16 μm from the sample surface. This implies that the deep levels obtained through DLTS are characteristic of the region more towards the tail of the implant profile. The transport measurements indicate that the active layer is ~ 0.12-0.13 μm thick. The difference in thicknesses estimated from transport and capacitance measurements is due to the surface depletion layer, which was not accounted for in the transport measurements.

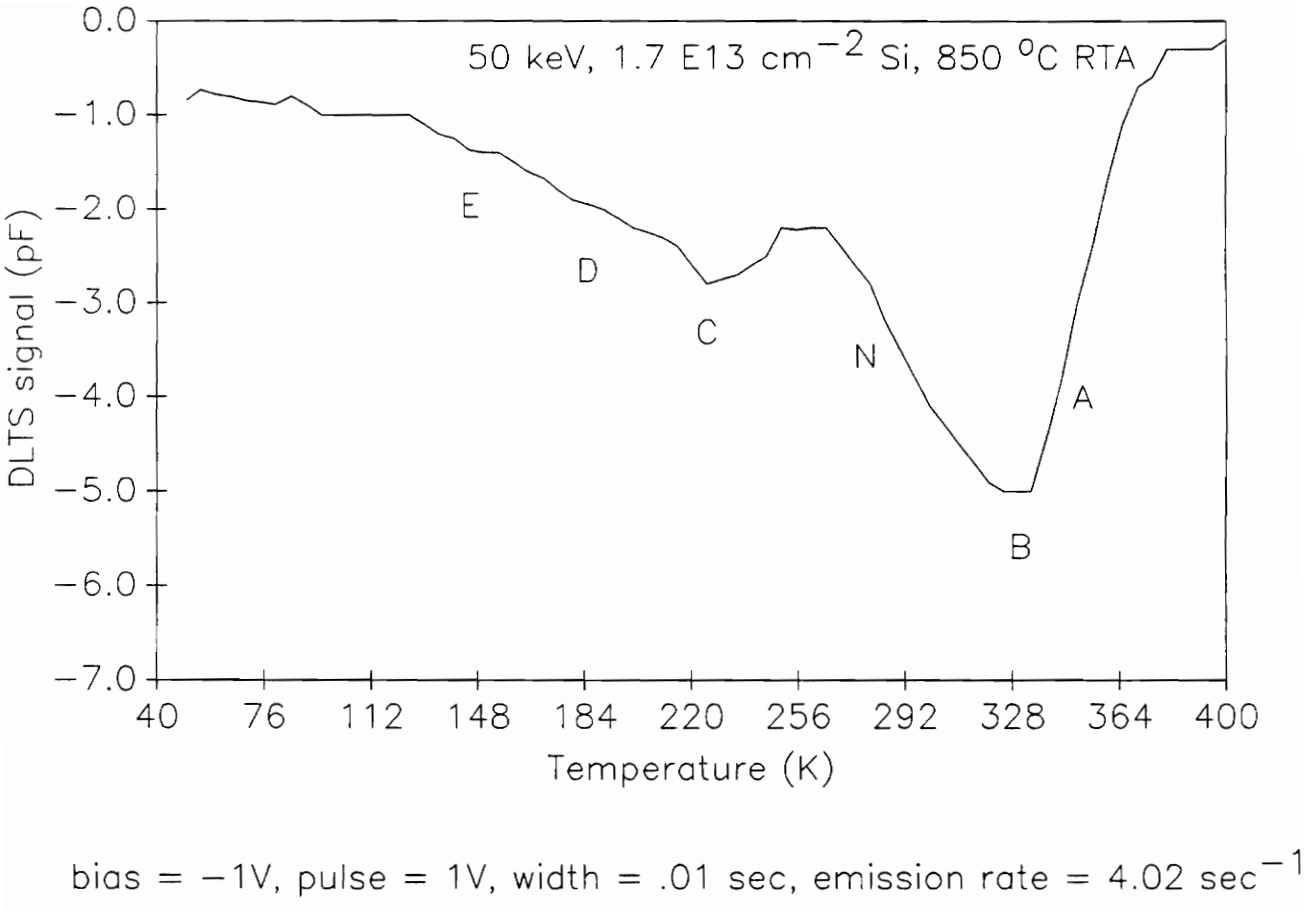


Fig. 5.8 DLTS spectrum of a Si-implanted and RTA annealed (211)-0° GaAs (trap labels are defined in text).

Table 5.3. Trap parameters of Si-implanted and RTA annealed (211)-0° GaAs.

Depth	Label	E_C-E_T (eV)	N_T/N_D	Possible designation
0.14 μm	A	0.80	.028	EL2
	B	0.75	.048	EB4 (?)
	N	0.63	.027	?
	C	0.51	.027	EL4
	D	0.42	.020	EL5
	E	0.33	.013	EL6
			$\Sigma N_T/N_D = 0.163$	
0.16 μm	A	0.82	.030	EL2
	B	0.73	.033	EB4 (?)
	N	0.66	.030	?
	C	0.51	.030	EL4
	D	0.42	.025	EL5 (?)
	E	0.37	.017	EL6
			$\Sigma N_T/N_D = 0.165$	

To summarize, the deep level properties of a 50 keV Si-implanted and RTA-annealed active layer on (100) and (211) GaAs substrates are similar, except (211) has an additional deep level (0.63-0.65 eV) and the sum total of relative trap densities is higher in (211) than in (100). Within the scope of the measurement technique used, there was no apparent effect of 0° and 45° rotation angle during implantation on the deep level characteristics of (211) GaAs substrates.

5.2.1 (100) vs. (211) LEC GaAs:Cr

This section deals with the electrical properties of 50 keV Si-implanted and RTA (850 °C/30 sec.) activated (100) and (211) GaAs. Except for the substrate being Cr doped, the samples discussed in this section are processed identically like the samples in 5.1.1. The sample process description is provided under category B in Chapter 4. The effects of substrate orientation (100) and (211) on transport and deep level behavior of Cr-doped GaAs will be discussed next.

5.1.2a Transport Characteristics

Although no detailed transport profiling was done on these samples, the average room temperature measurements yielded the parameters presented in Table 5.4.

Table 5.4. Room temperature Hall parameters

substrate	sheet resistance ρ_s ($\Omega/\square$)	mobility $cm^2/V\text{-}sec$	sheet concentration $n_s(cm^{-2})$
(100)	231	2430	$1.11x10^{13}$
(211)	366	1662	$1.02x10^{13}$

Since the active layer thicknesses on these samples are not precisely known (profiling was not

performed), the values of sheet resistance and sheet carrier concentration are listed instead. It is evident from Table 5.4 that (211) has lower mobility and higher resistivity than (100) on GaAs:Cr substrate. The results are consistent with the findings in section 5.1.1a on the undoped GaAs substrate. It may be concluded that, compared to the (100) GaAs, the (211) GaAs has inferior transport parameters, and this is independent of the original substrate being undoped or Cr doped. The observed differences in transport parameters are almost exclusively influenced by substrate orientation.

5.1.2b Deep Level Characteristics

DLTS measurements were performed on Si-implanted and RTA-annealed (100) and (211) GaAs:Cr using Schottky barriers in back-to-back geometry. Fig. 5.9 is a representative DLTS spectrum for the (100) GaAs:Cr sample. The spectrum was recorded at 1V reverse bias (i.e. at 0.13 μm away from the surface). Unlike the spectrum for a similarly processed (100) undoped GaAs (refer to Fig. 5.6), the spectrum in Fig. 5.9 is sharp and has one dominant peak, C, located at E_c-0.56 eV. This trap is similar to EL4 but with a slightly modified emission rate. The details of the trap characteristics for the sample are presented in Table 5.5.

The occurrence of traps at E_c-0.55 eV has been reported for a 250 keV Si-implanted and 800 °C RTA-annealed (100) GaAs [2]. It has been proposed that this level is created by the association of the defects in the original substrate and the defects due to implantation at high annealing temperatures (≥ 800 °C). The same level has been consistently observed by Dhar *et al.* in both furnace and RTA annealed GaAs [63]. They have reported that this level followed the dislocation profile in the sample and is due to implant damage, possibly associated with Ga vacancy. To consolidate this argument on the origin of level C in Fig. 5.9, DLTS spectra for an MBE grown n-GaAs, before and after 4 keV Ar^+ bombardment, are shown in Fig. 5.10. The results provide strong evidence that ion processing generated two electron trap levels (one at E_c-0.31 eV (EL6) and the

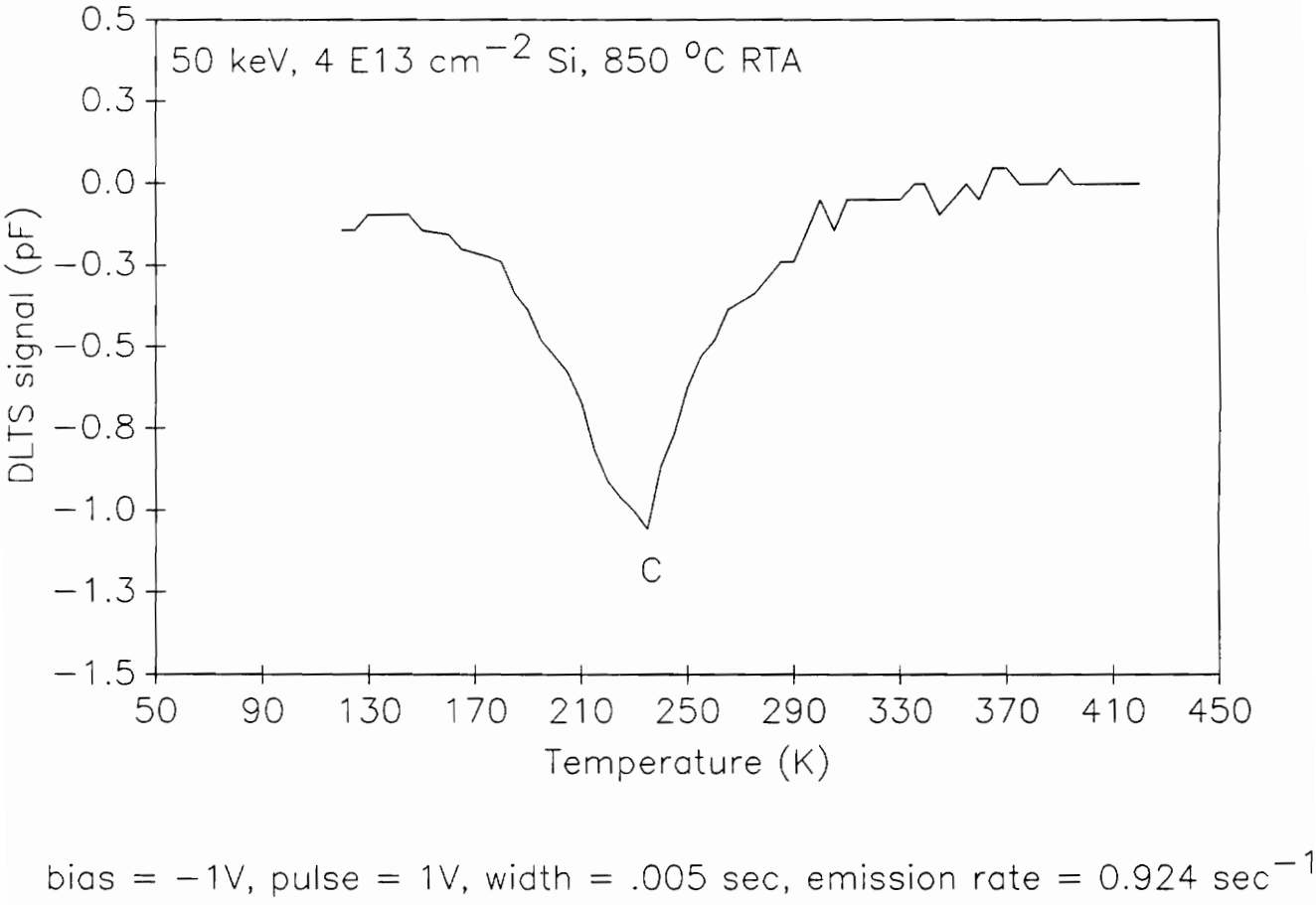


Fig. 5.9 DLTS spectrum of a Si-implanted and RTA annealed (100) GaAs:Cr (label C is defined in text).

Table 5.5. Trap parameters of Si-implanted and RTA annealed GaAs:Cr.

Substrate	Depth (μm)	Label	E_C-E_T (eV)	N_T/N_D	Possible designation
(100)-45°	0.132	C	0.56	.006	EL4
	0.140	C	0.56	.010	EL4
(211)-45°	0.140	C	0.55	.010	EL4
	0.145	C	0.55	.043	EL4
(211)-0°	0.140	C	0.54	.030	EL4
	0.145	C	0.54	.050	EL4

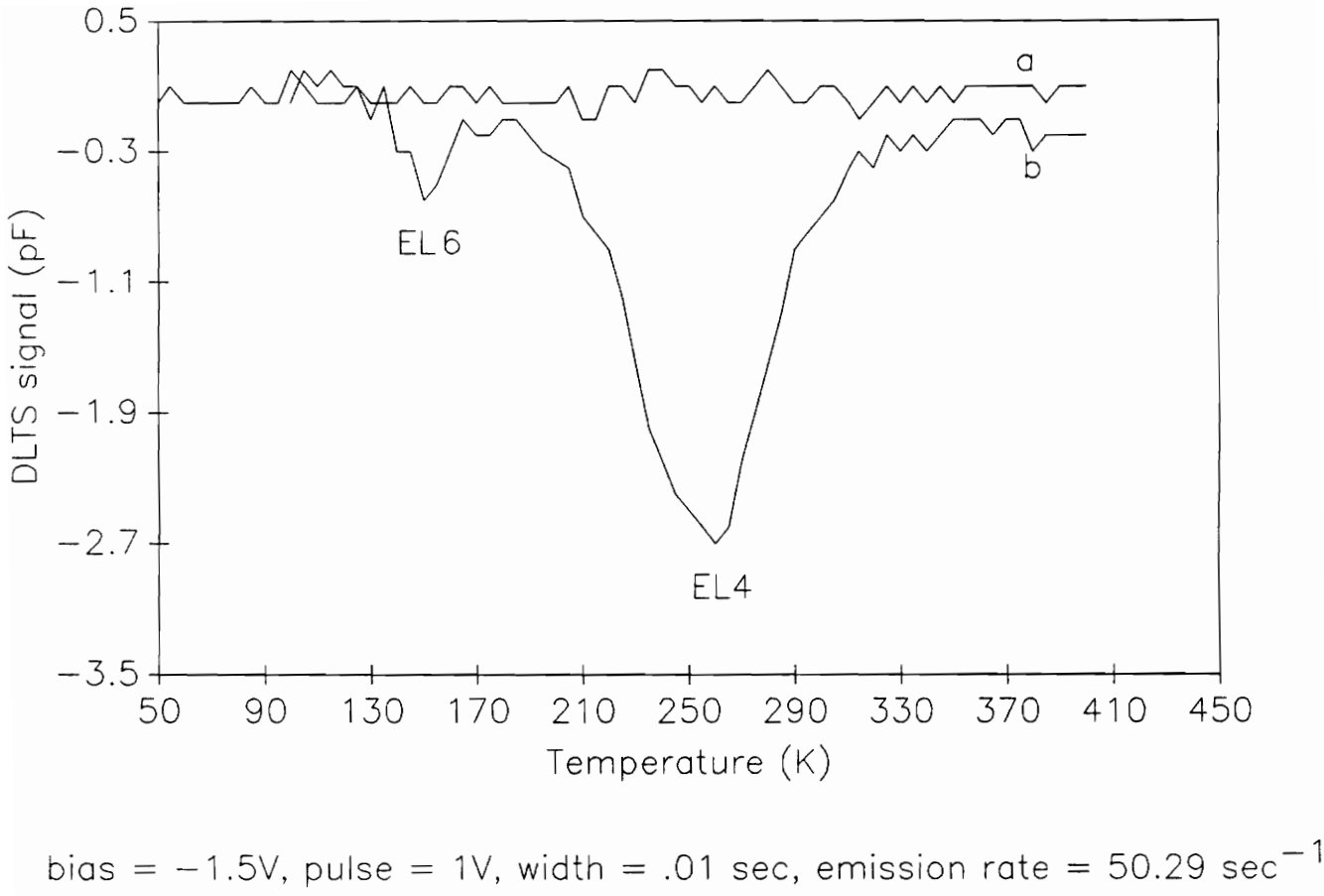


Fig. 5.10 DLTS spectra of MBE n-GaAs : a) before and b) after 4 keV Ar^+ bombardment.

other at E_c-0.52 eV (EL4)) in an otherwise defect free virgin sample (trap density below the detection limit of 10^{-3} times the doping density). The level EL4 detected in both 50 keV Si-implanted (100) GaAs:Cr and 4 keV Ar^+ etched MBE GaAs have similar characteristics and are believed to be due to ion damage. These results are in very good agreement with published reports [2,63].

The DLTS outputs for (211) substrates with 45° and 0° rotation angle during Si implantation are shown in Figs. 5.11 and 5.12, respectively. The DLTS measurement parameters are the same in both cases. The spectra, shown in Figs. 5.11 and 5.12, are very similar to the (100) spectrum. The DLTS signals in them continue to be dominated by emission from the EL4 (0.54-0.55 eV) center. The trap parameters for both (211) samples at two different reverse biases are included in Table 5.5. It appears that the sum total of relative trap concentrations in (211) is higher than in (100), and is consistent with the findings on undoped LEC GaAs substrates as discussed before (section 5.1.1b). Accordingly, it may be concluded that a higher total relative trap density in (211), compared to (100), is independent of the original GaAs substrate being undoped or Cr-doped.

There is no evidence of trap states other than EL4 in the (100) and (211) Cr-doped GaAs samples after 50 keV Si implantation and RTA (refer to Figs. 5.9, 5.11, and 5.12). This is in direct contrast with the DLTS results on (100) and (211) undoped substrates, where multiple trap levels were identified (refer to section 5.1.1b). In addition, the electron trap level unique to (211) GaAs, at 0.63-0.65 eV, was also not detected in the (211) Cr-doped GaAs. This difference of deep level behavior between two types of substrates are believed to be related to the substrate chemistry.

It is reasonable to expect native defects such as EL2 to appear in the DLTS spectra of the samples under consideration. The absence of EL2 and other electron levels in GaAs:Cr substrates may be attributed to one or both of the following :

(1) The emission from EL2 and from other electron levels with low densities may be masked by the emission from hole traps with large densities in the same temperature range.

(2) Cr competing with As for vacant Ga site and thus making EL2 (As_{Ga}) concentration below

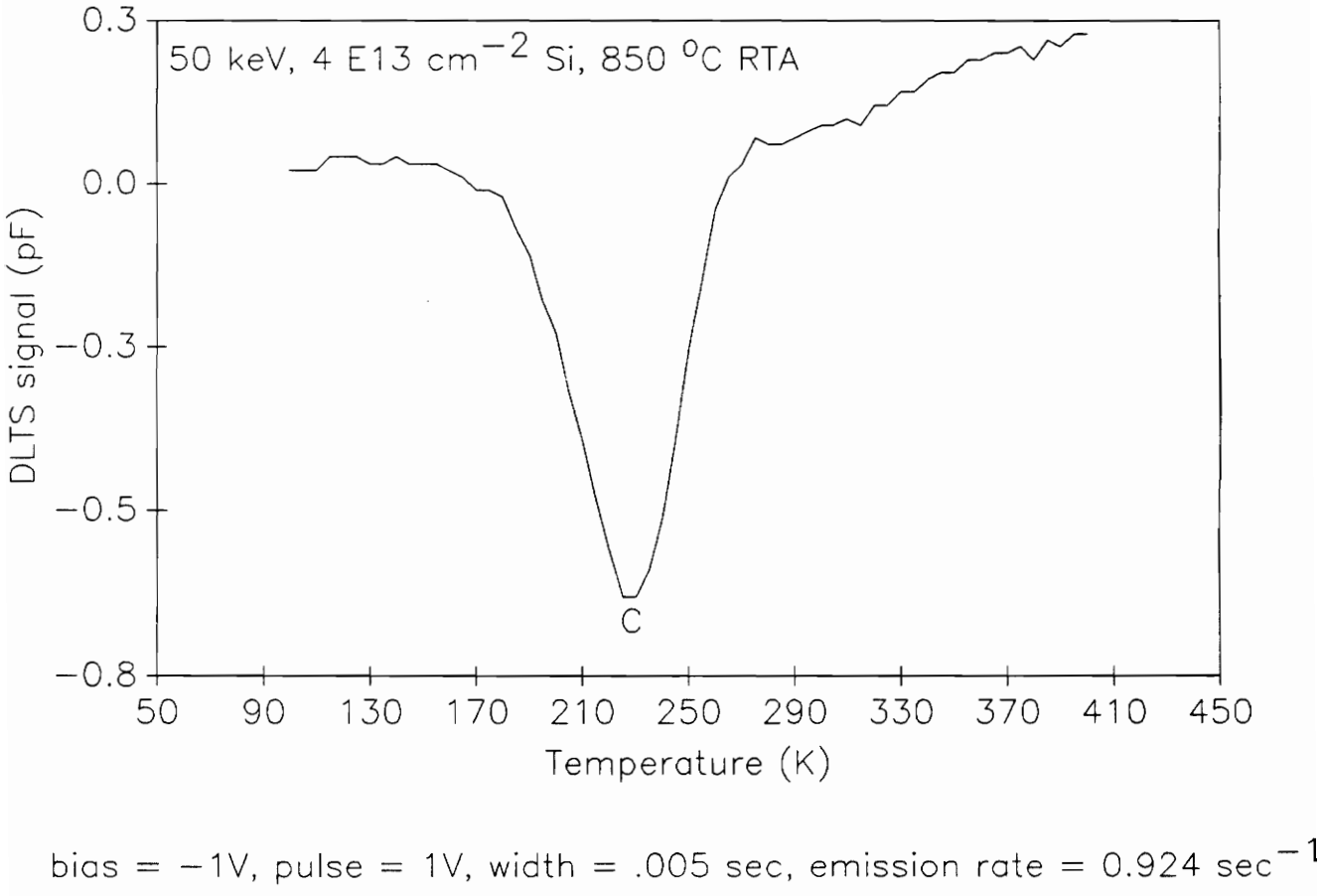


Fig. 5.11 DLTS spectrum of a Si-implanted and RTA annealed (211)-45° GaAs:Cr (label C is defined in text).

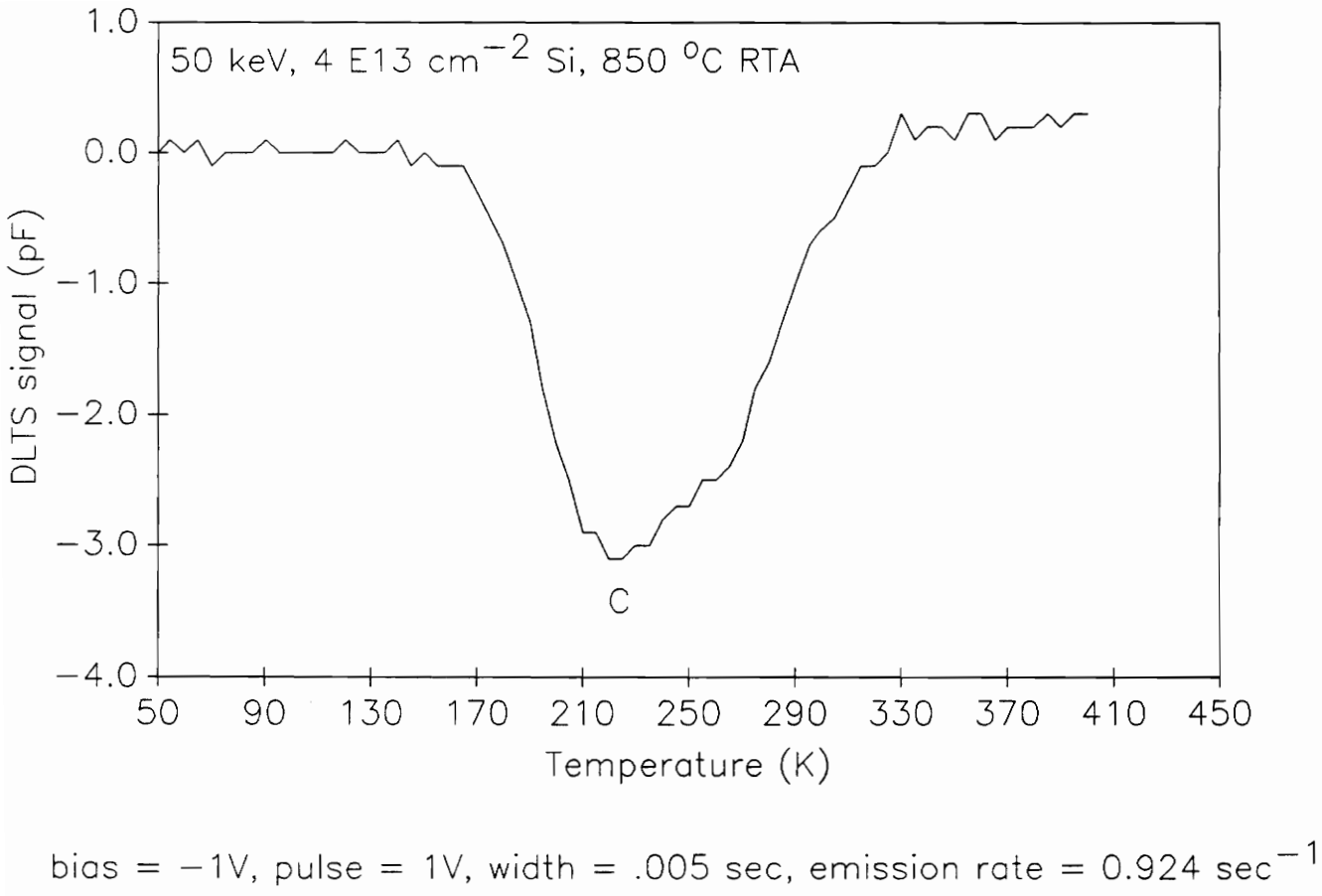


Fig. 5.12 DLTS spectrum of a Si-implanted and RTA annealed (211)-0° GaAs:Cr (label C is defined in text).

the detection limit of the measurement.

The absence of EL2 in Si-implanted GaAs has been reported by Fang *et al.* [61]. Its absence is attributed to the crystal stoichiometry of the starting SI substrate.

In summary, the level EL4 in Si-implanted and RTA-annealed (100) and (211) GaAs:Cr has been identified. Like in undoped GaAs substrates, the (211) orientation contains a higher relative trap density than (100) oriented GaAs:Cr. It is apparent that the type of starting SI substrate has a marked influence on the DLTS character of the active channels formed. Many of the electron traps that were identified in (100) and (211) undoped substrates were not evident in the Cr-doped substrates of either orientation.

5.1.3 Low Temperature GaAs Buffer

Recently the performance of a GaAs MESFET was shown to be substantially improved by using a low temperature (LT) MBE grown GaAs buffer layers [88]. The new buffer layer has gained considerable interest for MESFET fabrication due to its high resistivity and possibility for excellent device isolation. In this section, the electrical characteristics of Si-implanted GaAs active layer formed on a LT GaAs buffer and on a SI substrate are compared. The processing history for both samples (with and without LT GaAs buffer) is described in category C in Chapter 4. The schematic representation of the cross-sections of the LT buffer and no buffer (control) samples are shown in Fig. 5.13.

The implantation on these samples was done through a silicon-oxy-nitride (SiON) cap and the post-implant annealing was done in a furnace at 827 °C for 20 minutes under arsine atmosphere. Electrical measurements were made on fat FETs formed on these wafers. The fat FETs had self-aligned TiW nitride (TiWN) gates of 19.5 μm long and 1712 μm wide. The diode and the DLTS measurements were performed between the gate and the source contacts of fat FETs.

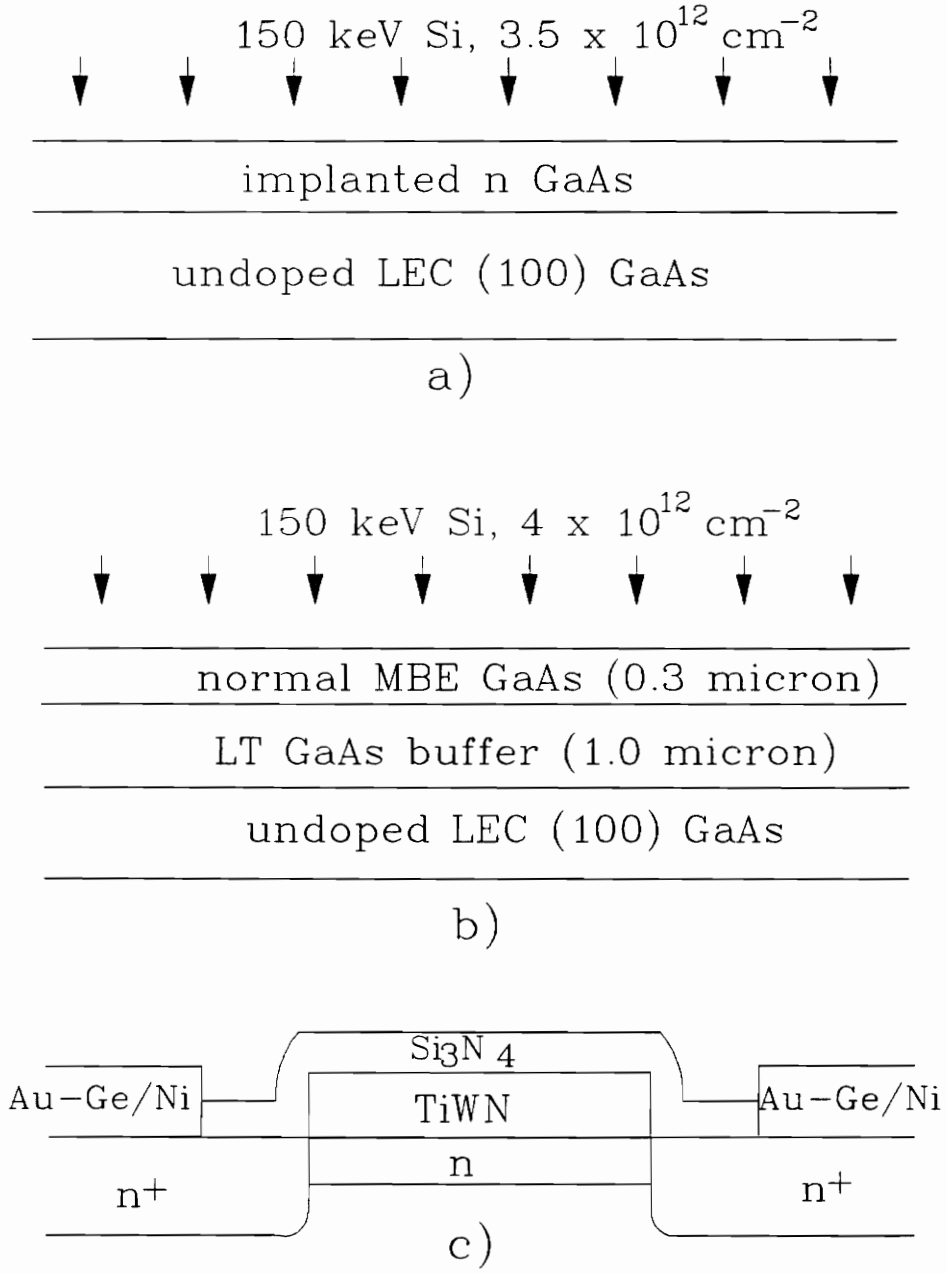


Fig. 5.13 Schematic cross sections of : a) control wafer, b) LT GaAs buffer wafer, c) fat FET structure.

5.1.3a Diode Measurements

The activation energy (Richardson) plots for the Schottky barriers on no-buffer and LT GaAs buffer samples are shown in Figs. 5.14a and 5.14b, respectively. The plots appear identical and the respective barrier heights (Φ_b), obtained from their slopes are listed in Table 5.6. Also included in the table are the ideality factor (n), reverse saturation current (I_0), zero bias gate capacitance (C_{gs}), zero bias parallel conductance (G), and the phase angle (θ).

Table 5.6. Diode parameters for no-buffer (I) and LT GaAs buffer (II) samples.

sample	Φ_b (eV)	Cgs (pF)	G (mS)	θ	n	I_0 (amps)	V_{BD} (V)
I	0.93	45.57	.024	-85.23	1.17	5.6×10^{-11}	3.5
II	0.92	46.07	.025	-85.0	1.13	5.1×10^{-11}	5.0

It is evident from Table 5.6 that the parameters of Schottky diodes formed on the active layers with and without LT GaAs buffer are very similar. C-V (Capacitance-Voltage) measurements performed on these diodes reveal a dopant profile more abrupt and sharp for the diode with LT buffer than for the diode formed on a directly implanted channel. The characteristic dopant profiles for samples with no-buffer and with LT GaAs buffer are presented in Fig. 5.15. The cause for this striking difference in the dopant profiles will be addressed later through DLTS measurements.

The MESFET characteristics with and without the LT GaAs buffer are compared in Table 5.7 (refer to page 132). The MESFET performance on a Mg-implanted p-GaAs buffer layer, also included in the table, is surprisingly similar to the FET on the LT GaAs buffer layer [183]. Fig. 5.15 and Table 5.7 clearly indicate that FETs formed on a channel with a sharper carrier profile exhibit reduced magnitude of threshold voltage (V_{th}), higher transconductance (g_m), and lower drain current (I_{dss}) than FETs with a more diffused profile. Although there have been reports of significant

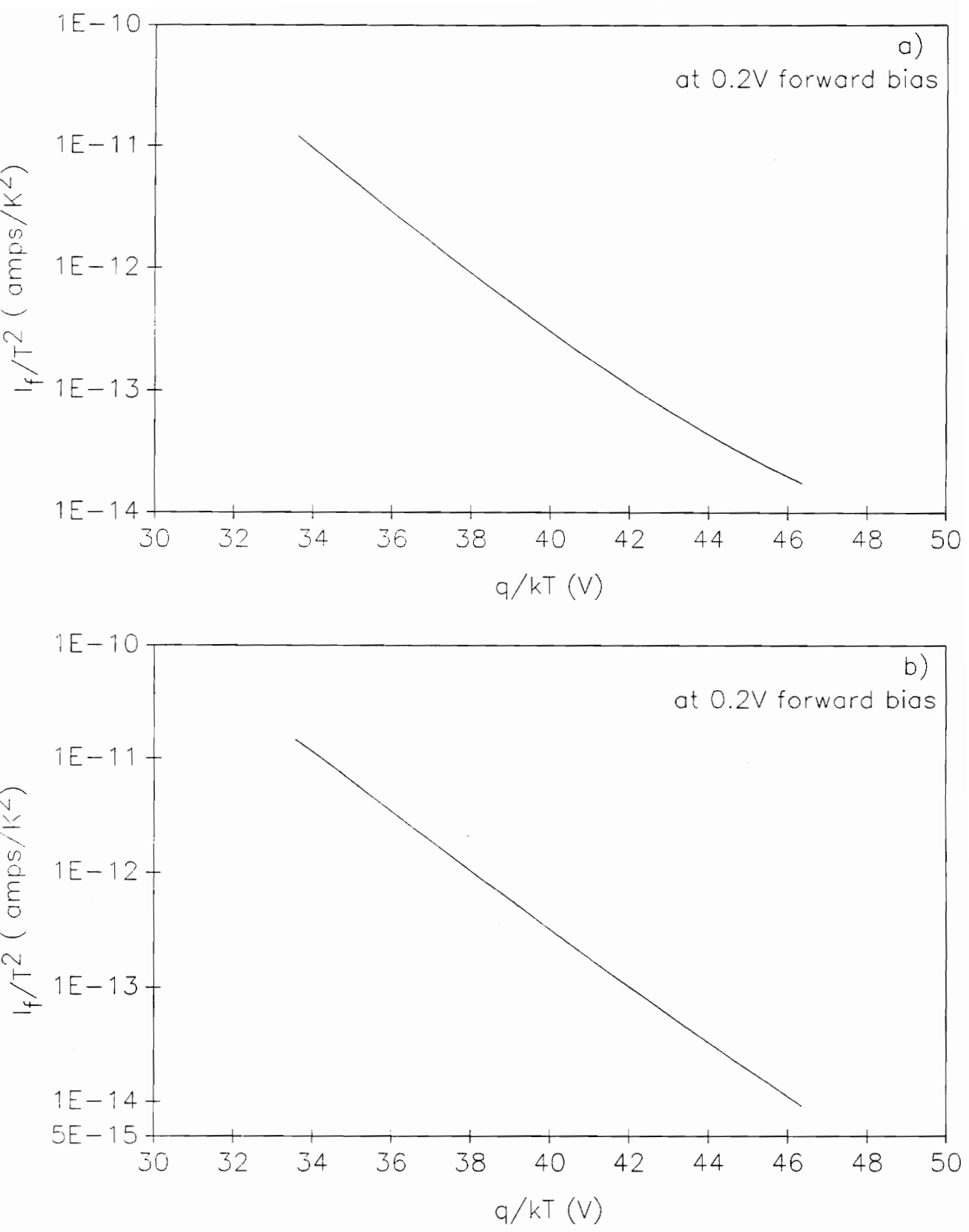


Fig. 5.14 Richardson plots for diodes on a) no-buffer and b) LT GaAs buffer samples.

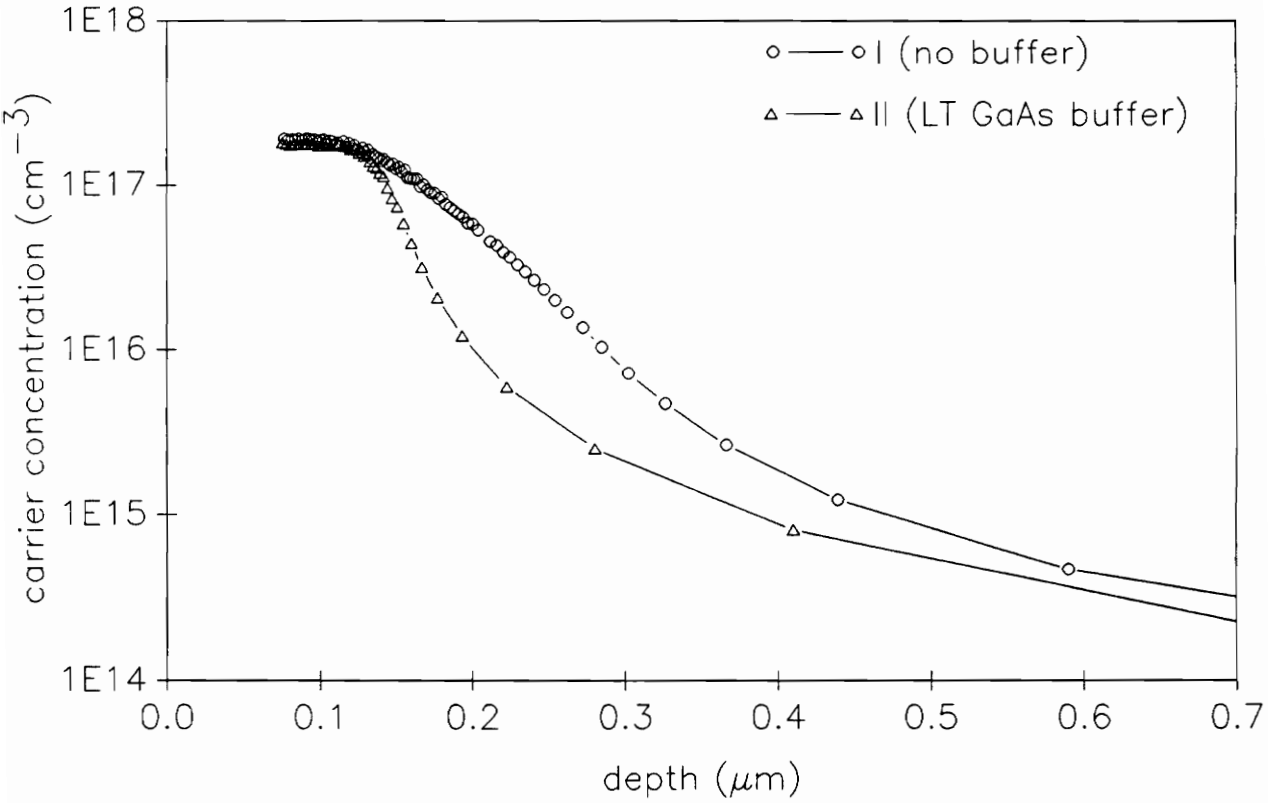


Fig. 5.15 Dopant profiles of fat FET channels on no-buffer and LT GaAs buffer samples.

improvement in the backgating (and/or sidegating) behavior of FETs on LT GaAs buffer [88,98] , the FET sample on LT GaAs buffer examined in this research has behaved otherwise [183]. In their sidegating model, Kocot and Stolte [86], emphasized the need of a buffer layer with a low density of traps to minimize the effects backgating. On the other extreme, they proposed the need of a buffer layer with high trap density for realizing good device isolation. Therefore it is difficult for a single substrate or an epitaxial buffer to provide isolation and minimize backgating (or sidegating) concurrently. In this context, a LT GaAs buffer appears to be a potential solution [88,98]. The following section will focus on the defect characteristics of the channel on a LT GaAs buffer layer. Although the FET performance on such a buffer is desirable (high g_m, reduced V_{th}), they exhibited significant backgating effects, the reasons for which will be discussed.

5.1.3b DLTS Measurements

Capacitance DLTS experiments were conducted on sample type I (no buffer) and II (LT GaAs buffer) at regions of varying depths from the surface. The DLTS spectra of sample I at different regions in the channel are shown in Fig. 5.16. It is interesting to note that the spectra are flat (except for the noise) at different probe depths. This means that the traps in the sample are either absent or their concentrations are below the detection limit (10^{-3} of the net carrier concentration) of the DLTS system. Similar observations hold for sample II (LT GaAs buffer) at depths of ~ 0.10 and 0.15 μm from the surface (see Fig. 5.17). Except for the instrumental noise, the DLTS spectra in Figs. 5.16 and 5.17 are featureless.

The absence of any detectable electron trap in the channel regions of both the samples is very surprising. This is in direct contrast with the results obtained for 50 keV Si-implanted and RTA GaAs where various electron traps were detected (refer to section 5.1.1b). Although the implantation and annealing parameters for the fat FETs are widely different from those used in 5.1.1b, it is quite reasonable to expect EL2 (an established trap level in undoped LEC GaAs) to appear in the DLTS

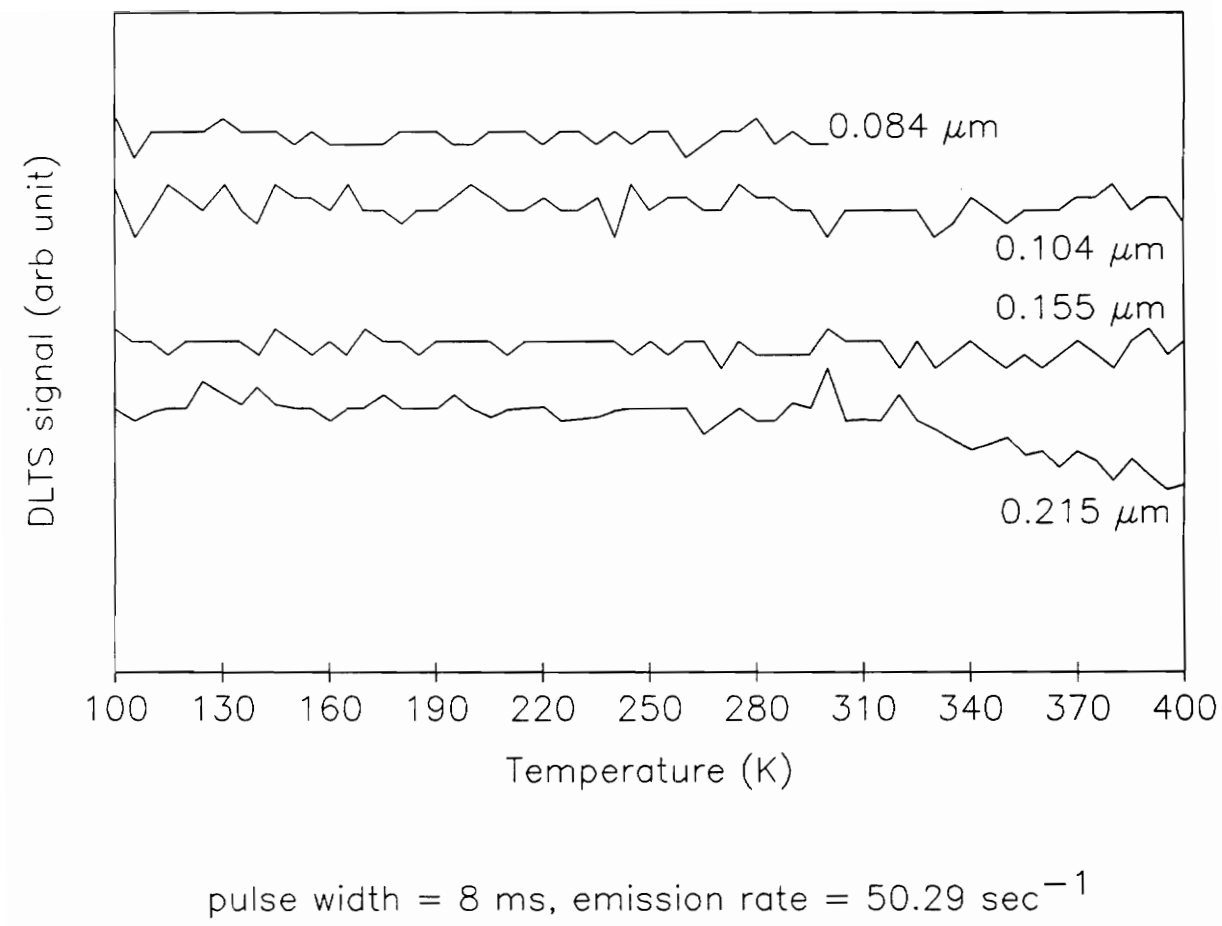


Fig. 5.16 DLTS spectra of sample I (no buffer) at indicated depths.

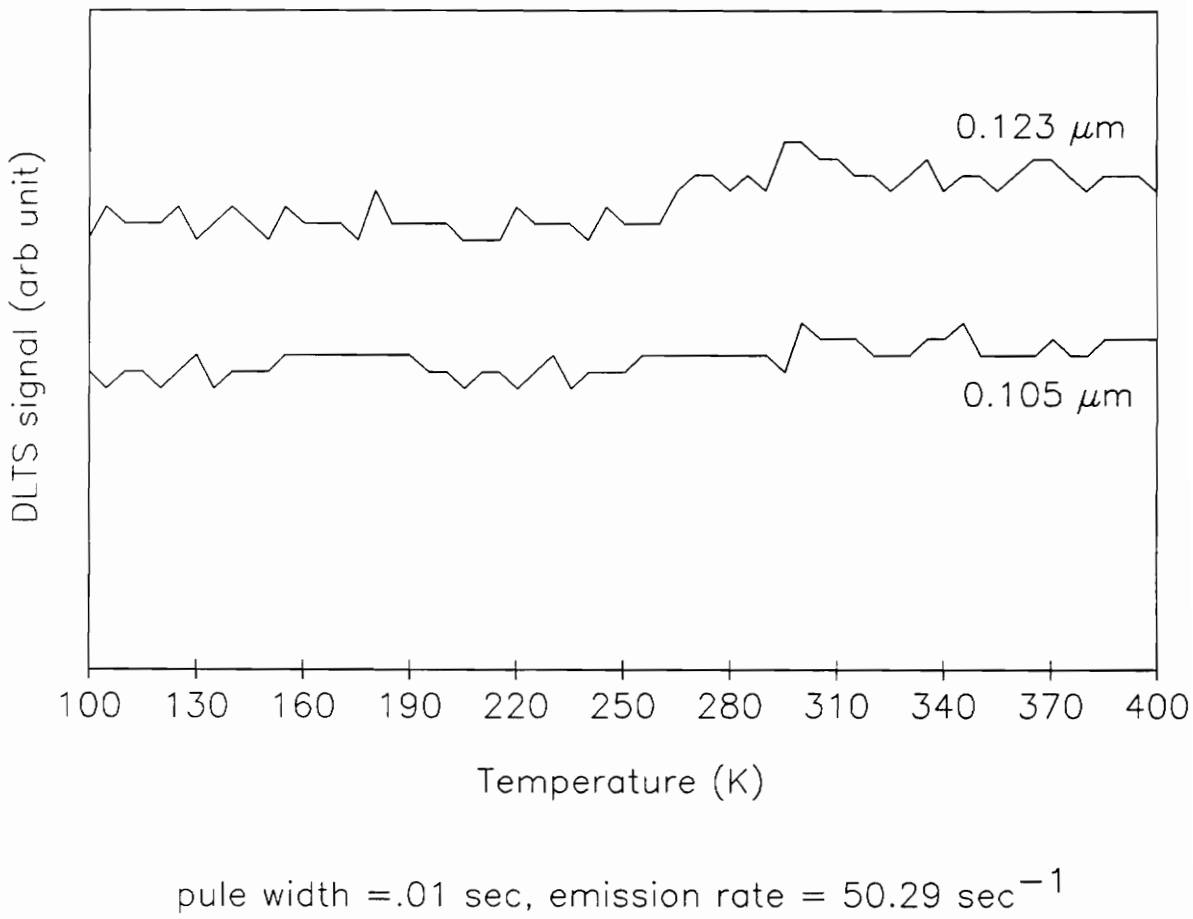


Fig. 5.17 DLTS spectra of sample II (LT GaAs buffer) at indicated depths.

spectra. The total absence of any detectable traps in the channel regions of both fat FETs (I and II) may be explained in terms of one of the following possibilities (or their combination) :

i) Post-implant furnace annealing at 827 °C for 20 minutes is sufficient to diminish all trap levels to a concentration below the detection limit.

ii) Implantation through a 850 Å SiON nitride cap results in significantly less damage, which is healed during the subsequent annealing process. There are similar reports on Si-implanted GaAs through a 1500-2000 Å thick silox (SiO_2) encapsulating layer with subsequent furnace annealing [64,143]. The reported DLTS spectra showed no evidence of any electron trapping states. No account for the absence of traps has been provided, but the use of silox encapsulant during implantation has been proposed to be effective in significantly reducing trap concentrations [64,143].

iii) Out-diffusion of defects into the gate metal (TiWN) during furnace annealing. The fabrication sequence of fat FETs is such that the gate metallization is completed before the post-implant heat treatment. During annealing, the gate metal covers the region of the active layer directly under it, while the remaining portion of the wafer surface is capped with SiON film. It is known that EL2 out-diffuses into the annealing cap during heat treatment [2,110]. The loss of EL2 is more in furnace-annealed than in RTA-annealed samples because of longer annealing time in the former, and hence more out-diffusion [2]. This loss is related to the decrease in excess As concentration near the surface, i.e. As out-diffuses into the annealing cap. The diffusion behavior of other electron trap levels during annealing has not been considered as extensively as EL2.

The above discussion attempts to present a possible scenario that can help understand the total absence of electron traps in the channels of fat FETs (I and II). A more concrete reason explaining the occurrence of flat DLTS spectra will emerge in section 5.1.4b, where by means of

detailed comparison, one of the above mentioned possibilities will be seen as adequate in explaining the observed behavior.

It is important to emphasize that the channel in sample II (LT GaAs buffer) was formed by Si implantation into a normal MBE grown epi-layer (see Fig. 5.13). It is therefore appropriate to expect some of the well known MBE related trap levels [32] in the spectra of Fig. 5.17. EL2, though not a characteristic defect in as-grown MBE GaAs, can be created by annealing [36]. All these facts support the expectation on the occurrence of electron traps in sample II. So far, the DLTS results simply suggest that the implantation and annealing methods employed in sample II are such that the MBE related trap levels are reduced to a level below the detection limit of the apparatus.

The DLTS experiments were performed on samples I and II at deeper regions to further define the deep level character of these samples. The DLTS results for sample I (no-buffer) remain unchanged even at depths close to the active layer-substrate interface. The results of sample I remain unaltered when an identical sample with four fat FET gate fingers in parallel was measured for DLTS. The motive for using this configuration (four parallel gates) was to increase the total gate capacitance C and thereby improve the DLTS resolution (trap density scales as $\Delta C/C$).

The most dramatic change in DLTS results is seen in the LT GaAs buffered sample (II) when the probe depth approached ~ 0.15 μm. Positive DLTS peaks begin appearing, and the spectrum exhibits four distinct hole emission peaks (labelled A-D) at a depth of 0.39 μm. These spectra are shown in Fig. 5.18. The DLTS signal amplitudes become stronger with probing depth and, at 0.39 μm depth, the region of probe is well into the LT GaAs buffer. At this location , the appearance of strong DLTS peaks indicates the presence of defects at significant concentrations. The temperature dependence of the thermal emission rates for the four defect peaks is shown in Fig. 5.19. The corresponding trap parameters are tabulated in Table 5.8. Contrary to these results, positive peaks were systematically absent in sample I (no-buffer) at all probe depths. The appearance of hole-like traps near pinch-off bias in sample II (see Fig. 5.18) suggests the possibility of hole emission from

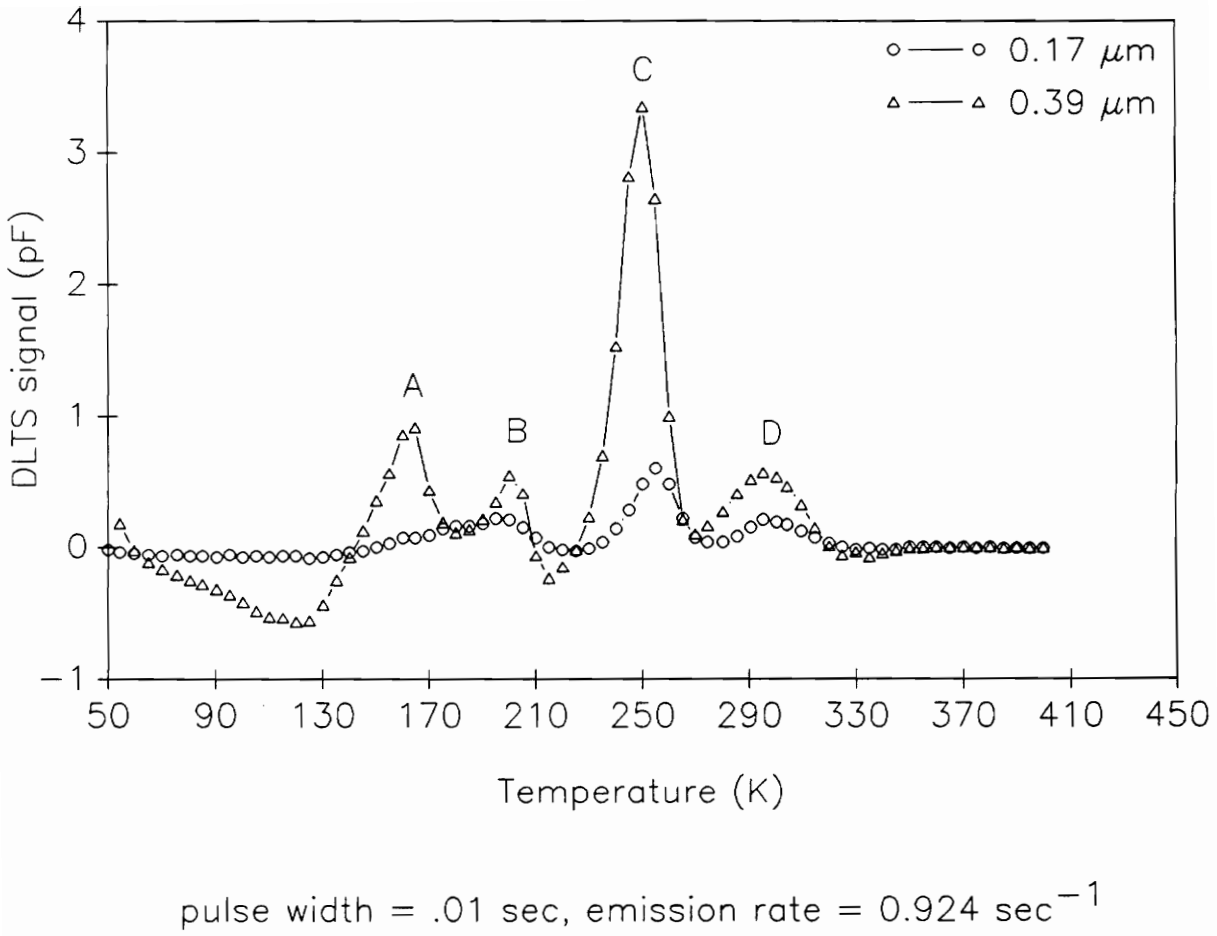


Fig. 5.18 DLTS spectra of LT GaAs buffer sample (II) at indicated depths (labels A-D are defined in Table 5.8).

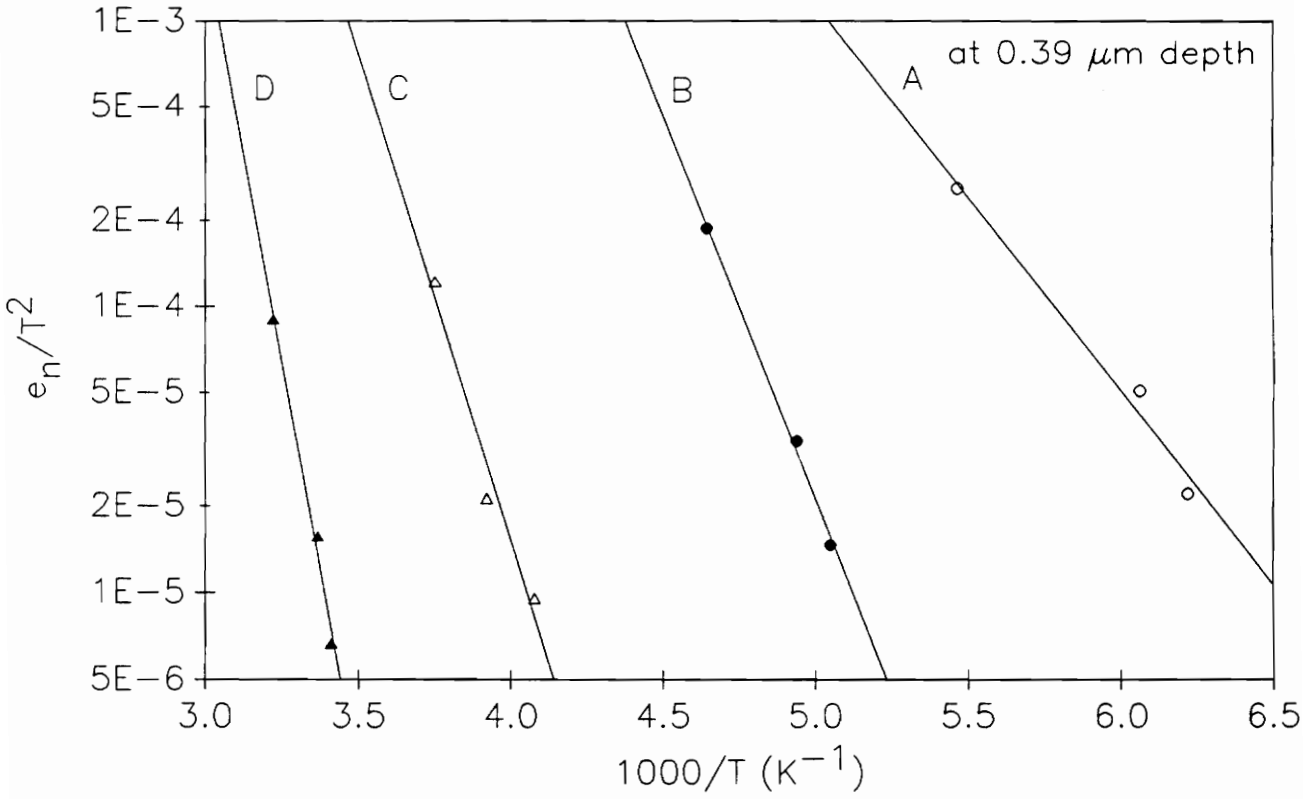


Fig. 5.19 Temperature dependence of thermal emission rates of hole traps (A-D) in sample with LT GaAs buffer (II).

Table 5.7. Effect of LT GaAs buffer on MESFET dc parameters [183].

Sample	I_{dss} (mA/mm)	g_m at (mS/mm) at ½ I_{dss}	V_{th} (V)
150 keV Si^{29} into LEC GaAs	415	100	-5.48
150 keV Si^{29} into GaAs on LT GaAs buffer	296	123	-2.69
150 keV Si^{29} + 250 keV Mg^{24} into LEC GaAs	305	136	-2.67

Table 5.8. Trap characteristics of sample with LT GaAs buffer (II) at 0.39 μm depth.

Label*	$E_T - E_V$ (eV)	σ (cm^{-2})
A	0.27	3.8×10^{-18}
B	0.53	3.2×10^{-13}
C	0.68	4.1×10^{-13}
D	1.15	2.6×10^{-7}

* The trap labels (A-D) correspond to the DLTS peaks observed in Fig. 5.18.

acceptor type defects at the active layer-buffer interface.

At first sight, the above results appear anomalous. This is because injection of minority carriers does not occur in an electrical DLTS measurement employing a Schottky barrier, and therefore it is not possible to detect hole traps in an n-GaAs using this technique. The origin of these hole peaks in sample II will now be discussed in detail.

As suggested in reference [168], a high diode series resistance may reverse the sign of an apparent capacitance transient owing to the error incorporated in the capacitance reading, with the error being more severe when the diode dissipation factor D is close to or larger than unity. In the case of the LT GaAs buffer sample (II), the D value under DLTS measurement conditions (V_r=2V, f=1 MHz) was found to be 0.27, and is significantly lower than the D=1 value for reversing the DLTS signal. It is therefore certain that the positive DLTS peaks in Fig. 5.18 are not a manifestation of the series resistance effects.

Houng *et al.* have also detected hole traps in n-GaAs FETs by electrical DLTS [184]. Similar to the DLTS spectra in Fig. 5.18, they too observed hole trapping effects only when the space charge edge approached the channel-substrate (GaAs:Cr) interface. In their study the hole levels were located at 0.58 eV and 0.81 eV above the valence band edge. The appearance of the positive DLTS peaks is attributed to the image effect of the majority carrier traps located at the substrate side and acting through the interface space charge region.

Among the traps listed in Table 5.8, the level A (0.27 eV) is comparable to an acceptor level at 0.30 eV, obtained by Hall effect and thermally stimulated EPR measurements on MBE grown LT GaAs buffer layers [92]. The defect is ascribed to a Ga vacancy, a major defect source detected in LT GaAs buffers. The traps B, C, and D are believed to be the characteristics of the LT GaAs buffer under study, and are reported for the first time. The level D is similar in characteristics to the hole level at E_V+1.10 eV, and has been observed earlier in a Si-implanted and furnace annealed GaAs [63].

Crystal defects are produced during low temperature growth of MBE GaAs buffers. At low

growth temperatures, adsorbed Ga and As atoms fail to diffuse to proper lattice sites before being incorporated into the lattice. These defects during subsequent high temperature processing diffuse upward towards the epi-buffer interface. It is suspected that these defects and impurities in the LT GaAs buffer are responsible for the hole levels detected in DLTS. Although these defects originate from the LT GaAs buffer, their migration into top epi layer is somewhat localized near the epi-buffer interface. This was evidenced in DLTS (Fig. 5.18) where positive peaks were observed only when the probe region approached the interface. Further clarification on the origin of the hole levels will be presented by a model described in the next section.

5.1.3c Model

The hole trapping phenomena in the fat FET on LT GaAs buffer can be explained by means of a second space charge region, near the interface, in addition to the primary space charge region under the Schottky barrier gate. To simplify the model two assumptions are made :

i) The back or the inactive portion of the top epi-layer is a part of the LT GaAs buffer layer and the simplified structure schematic with depletion layer widths is shown in Fig. 5.20a. This is a reasonable assumption since the pinch-off in sample II occurs at ~ 0.25 μm while the epi-layer is 0.30 μm thick.

ii) The buffer-substrate junction is neglected in the model. It is assumed that the junction has small capacitance owing to insignificant charge build-up.

The energy band diagram of the active-buffer layer interface with an acceptor type deep level (E_{AA}) on the buffer side is shown in Fig. 5.20b. It is assumed that beyond channel depth d ($x>d$), the only charge is due to ionized deep acceptors at E_{AA} with concentration N_T. The acceptor states are negatively ionized (empty of holes) for $d<x<x_1$ and neutral (filled with holes) for $x>x_1$, where x_1 is

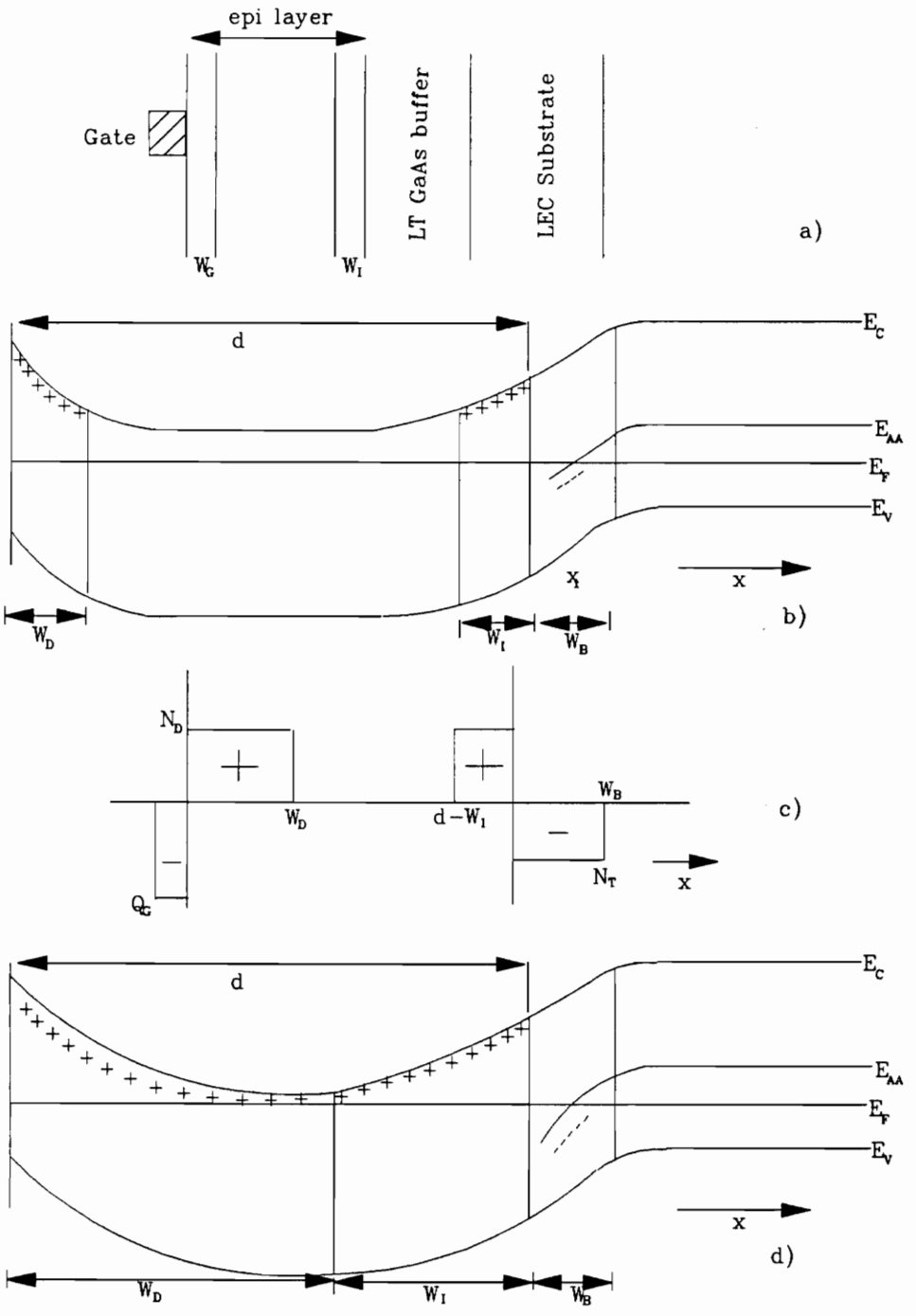


Fig. 5.20 Band diagram and space charge model for LT GaAs buffer sample (II) : a) schematic structure with depletion layer widths, b) band diagram at zero bias, c) space charge distribution at zero bias, and d) band diagram near pinch-off condition.

the point of intersection of the acceptor state E_{AA} with the Fermi level E_F. The active-buffer layer interface behaves as an ordinary p-n junction formed by deep acceptors (buffer side) and shallow donors (active side). The space charge distribution in the simplified structure (under the condition of zero bias) is shown in Fig. 5.20c. When the reverse bias on the Schottky gate approaches pinch-off, the second space charge region due to defect states in the buffer can affect the gate capacitance. The band diagram under the pinch-off condition is represented by Fig. 5.20d.

By treating the active buffer layer interface as a p-n junction, the space charge region penetration (W_I) into the active side is given by

$$W_I = \left[\frac{2\epsilon_s N_T^- V_{bi}}{qN_D (N_T^- + N_D)} \right] \qquad (5.1)$$

where N_T^- is the ionized acceptor density in the space charge region, ϵ_s is the semiconductor permittivity, q is the electronic charge, N_D is the shallow donor concentration, and V_{bi} is the built-in potential of the interface junction. It has been shown by Houng and Pearson [184] that near pinch-off condition, there is a drastic reduction of free carrier concentration (n_0) from the value close to N_D (shallow donor concentration). This is due to the interface space charge affecting the electrostatic potential. Under such a situation, the space charge neutrality condition is not valid and the Schottky barrier capacitance is more appropriately expressed as [184] :

$$C = \epsilon_s A \left[W_G + \left(\frac{\epsilon_s kT}{2q^2 N_D^2 L_D} \right) (N_D - n_0) \exp\left(\frac{-d - W_G - W_I}{L_D} \right) \right]^{-1} \qquad (5.2)$$

where L_D is the Debye length given by

$$L_D = \sqrt{\frac{\epsilon_s kT}{q^2 N_D}} \qquad (5.3)$$

Equation (5.2) indicates that near pinch-off ($W_G \rightarrow d\text{-}W_I$) , capacitance C decreases with increase in W_I.

When hole traps are present in the buffer depletion region, the emptied hole traps are filled with holes as the gate bias is made more positive (pulsing period in DLTS). This is because of the acceptor level (E_{AA}) going above the Fermi level (E_F) during the pulse period. Once the bias pulse is removed (i.e. the gate bias is made more negative), the filled hole traps begin emitting holes with time constant τ_p and the net ionized acceptor concentration (N_T^-) varies with time t as:

$$N_T^-(t) = N_T^-(\infty) - N_T(0)\ \exp\left(\frac{-t}{\tau_p}\right) \qquad (5.4)$$

where $N_T(0)$ is the concentration of filled traps immediately after the filling pulse and $N_T^-(\infty)$ is the ionized trap density in steady state. It is evident from equation (5.4) that N_T^- increases with time after the removal of the bias pulse, as does W_I according to equation (5.1). The increase in W_I is reflected in the decrease of the diode capacitance with time, a characteristic feature of a hole emission process. This is the reason for the occurrence of hole traps in sample II, when the steady state biasing during DLTS was close to pinch-off. It is now confirmed through the model that the minority traps in the DLTS spectra of Fig. 5.18 are due to deep acceptors residing in the buffer side and close to the interface. It has been reported that the measured time constants of these hole traps from DLTS are the true values but the trap concentrations determined this way are somewhat overestimated [184].

The above discussion satisfactorily explains the occurrence of positive DLTS peaks in the LT GaAs buffer sample (II) near pinch-off and beyond. The complete absence of any peaks in no-buffer sample (I), even near the channel substrate interface, suggests that the nature of the interface formed in either case is significantly different. The detection of hole levels at the channel-buffer interface in sample II is consistent with the steeply falling dopant profile (refer to Fig. 5.15) and reduced threshold voltage (V_{th}) observed in such FETs. Background acceptor impurities (deep or shallow) in the substrate are known to be effective in cutting off the implant channeling tails of donor atoms [102].

The resulting profile is sharper and has a strong impact on the MESFET threshold voltage. Under such a situation, negative charges accumulate on the substrate side and corresponding positive charges are built on the back side of the channel near the interface. The width of the interface space charge region is dependent upon the acceptor density in the substrate. The higher the acceptor density, the larger will be the penetration of the space charge into the channel and, consequently, the electron profile is steeper and the pinch-off quicker.

A 1MHz steady state capacitance and parallel conductance of fat FET on LT GaAs buffer (biased to 0.39 μm) show a unique behavior with temperature variation. Capacitance and conductance both exhibit distinct features as a function of temperature (C-T, G-T) and are shown in Figs. 5.21 and 5.22, respectively. This behavior was only seen when the gate is biased near pinch-off or beyond. For fat FET with a directly implanted channel on a SI substrate (sample I), such temperature dependence of capacitance and conductance are absent even at gate biases near the channel-substrate interface. The features in the C-T and G-T plots of sample II are attributed to acceptor type defects originating from the LT GaAs buffer and are consistent with the findings of the DLTS study.

To summarize, the channel formed on a LT GaAs buffer has an abrupt carrier profile which strongly influences the MESFET characteristics. Four different kinds of hole traps in the LT buffer layer were identified. These traps apparently migrate into the top epi layer during subsequent processing. The presence of hole traps in the buffer has a direct effect on the shape of the carrier profile in the overlying GaAs. A model is presented to account for the appearance of hole traps in the DLTS of an n-GaAs MESFET with a LT GaAs buffer. Although the hole trap characteristics in the LT GaAs buffer sample have been identified, their structural nature still remains largely unknown. Without detailed knowledge of the structural characteristics, it is very difficult to assign precise origins to these electrical defects.

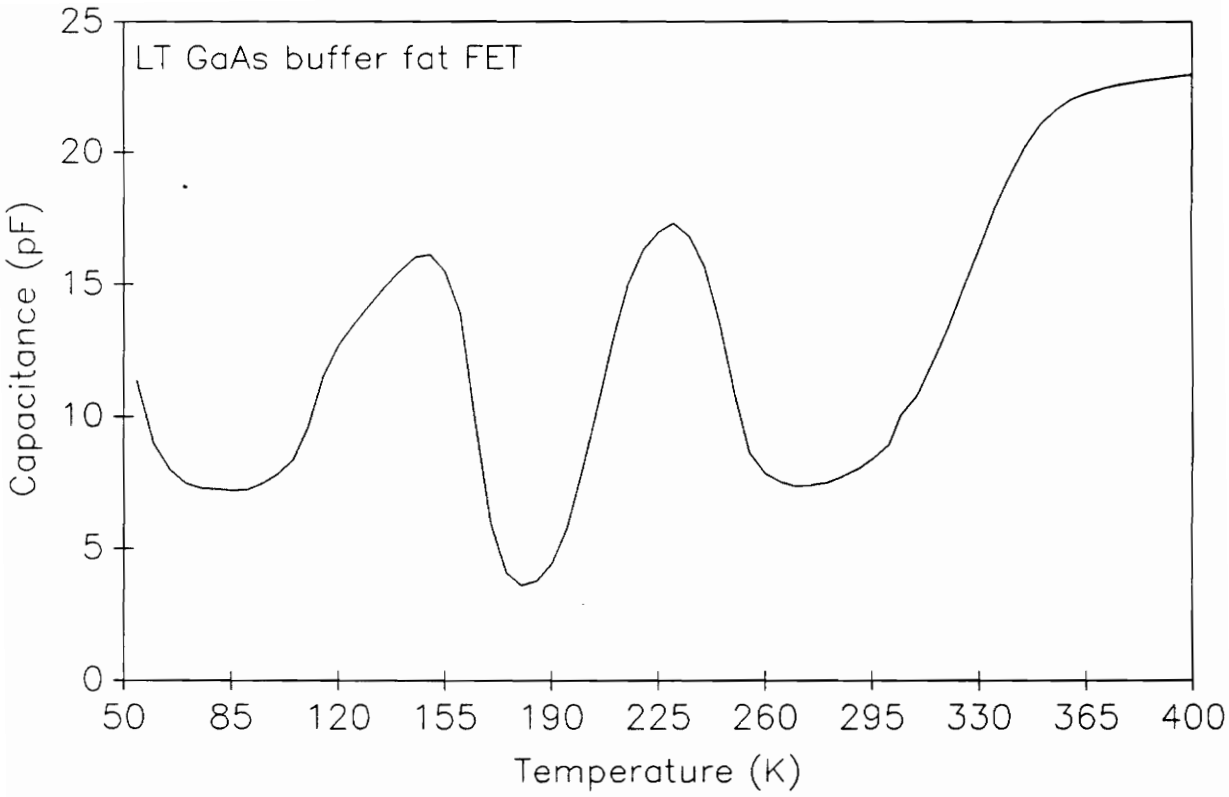


Fig. 5.21 Temperature dependence of capacitance of sample II at -2V gate bias (frequency = 1MHz).

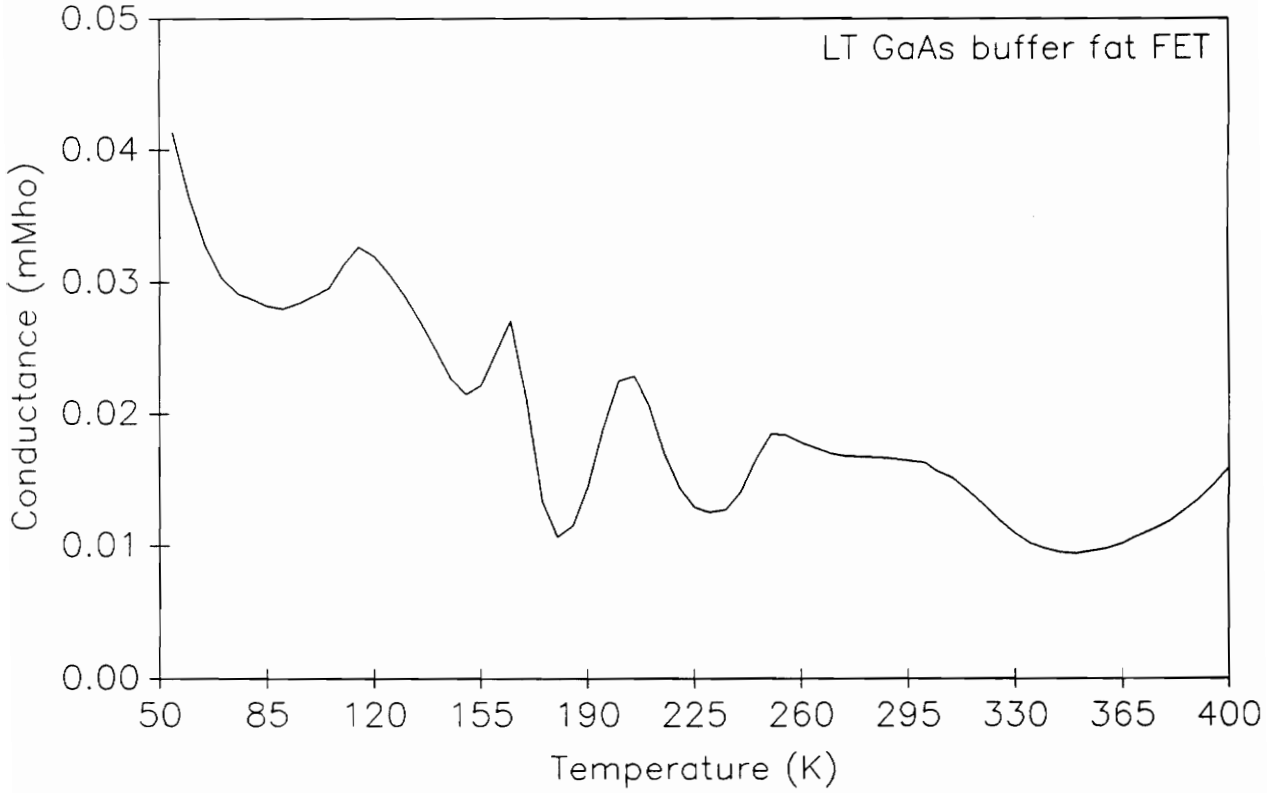
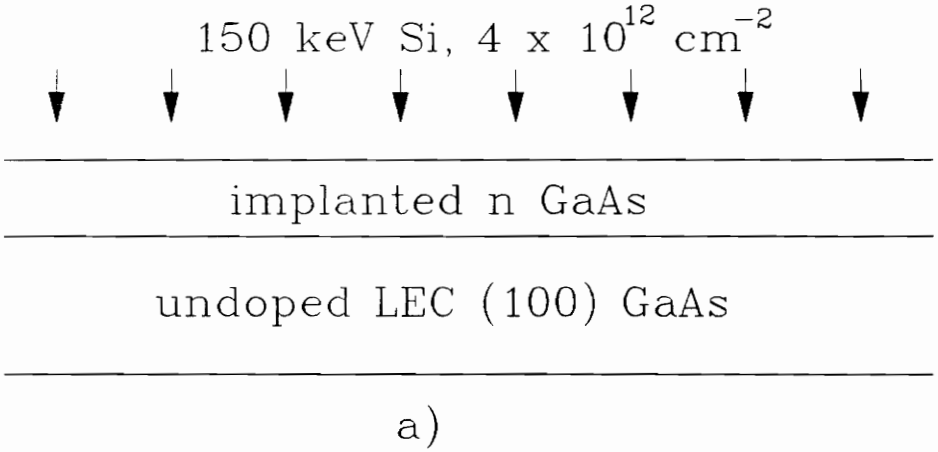


Fig. 5.22 Temperature dependence of conductance of sample II at -2V gate bias (frequency = 1MHz).

5.1.4 $Al_{.35}Ga_{.65}As$ Buffer

Following the study on LT GaAs buffers, studies related to the effects of MBE grown $Al_{.35}Ga_{.65}As$ buffer layer on the electrical characteristics of the overlying GaAs channel are reported in this section. Detailed results on transport and deep level properties of Si-implanted channel with and without a $Al_{.35}Ga_{.65}As$ buffer layer are presented. Sample processing conditions are described under category D in Chapter 4. In all samples, Si implantation was done through a 2000 Å thick SiON encapsulating layer. Schematics of the structures for buffer and no buffer sample are shown in Fig. 5.23.

The motivation behind this work is the observed variation in FET threshold voltage (V_{th}) for devices fabricated from implantation into MBE grown GaAs layers over an $Al_{.35}Ga_{.65}As$ buffer. Nominally identical wafers processed in a similar fashion have resulted in V_{th} variation from -2.4 to -5.5 V [185]. From carrier profile measurements on fat FETs, this behavior is believed to be more strongly linked with the tail of the implant at the upper GaAs/$Al_{.35}Ga_{.65}As$ interface than to the activation nearer the surface of GaAs, well away from the interface. Measurements on MESFETs with $Al_{.35}Ga_{.65}As$ buffer have shown significantly reduced V_{th}, lower I_{dss}, higher g_m, larger breakdown, and better linearity of transfer characteristics than the corresponding MESFETs without any buffer layer [185]. The best of the wafers on $Al_{.35}Ga_{.65}As$ has shown excellent rf power performances. Unfortunately, deleterious effects have also been reported in MESFET with an $Al_{.35}Ga_{.65}As$ buffer [185]. These include strong sidegating, parasitic rf conduction paths, and evidence of electrical activities within or at the lower interface of $Al_{.35}Ga_{.65}As$ buffer. The difficulty in delineating the effects of the buffer layer arises from the fact that it is virtually impossible to generate a channel (implanted or epitaxial) on a buffer with the buffer not experiencing any of the subsequent processing steps. Therefore in an attempt to study electrical activity and variability of characteristics in $Al_{.35}Ga_{.65}As$ buffers, the as-grown layers were tested for voltage dependence of 1MHz capacitance using a Hg probe. The results of four $Al_{.35}Ga_{.65}As$ wafers processed identically are presented in Table 5.9 [185].



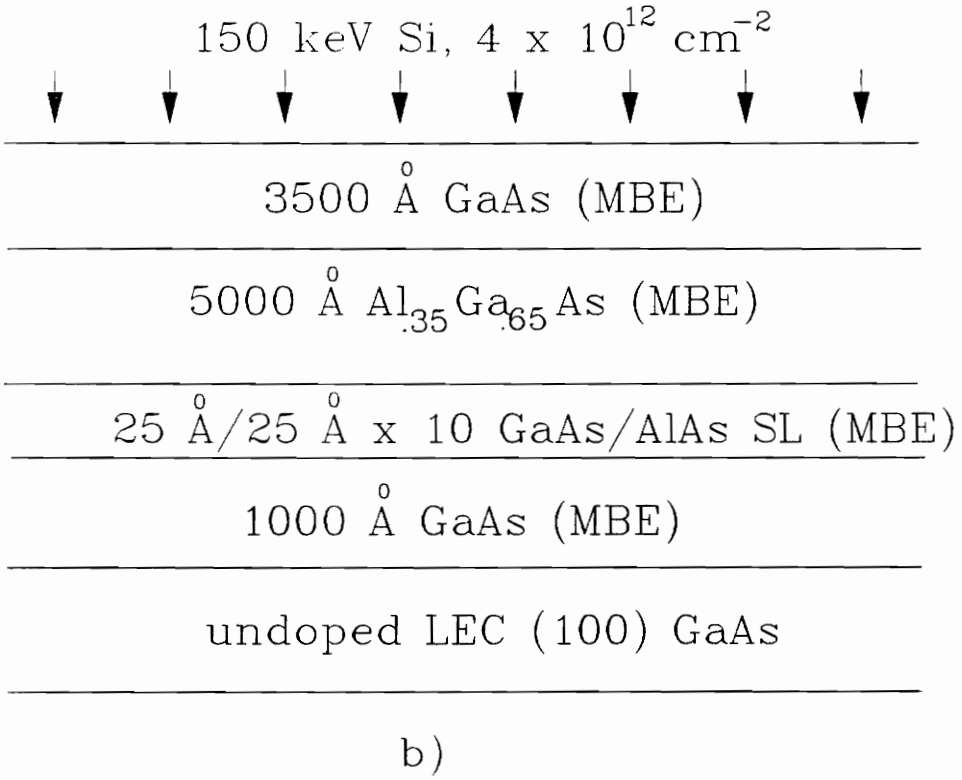


Fig. 5.23 Schematic cross sections of a) control and b) $Al_{.35}Ga_{.65}As$ buffer samples.

Table 5.9. Hg probe capacitance (C) of as-grown AlGaAs buffer at two biases [185].

Sample	Material	C (pF) at 0V	C (pF) at 18V
A	SI LEC GaAs	-	-
B	$Al_{.35}Ga_{.65}As$ buffer	0.28	0.25
C	$Al_{.35}Ga_{.65}As$ buffer	0.40	0.28
D	$Al_{.35}Ga_{.65}As$ buffer	0.86	0.50
E	$Al_{.35}Ga_{.65}As$ buffer	1.85	0.55

Samples B and C show little voltage dependence of capacitance, D shows a moderate dependence, and E shows a strong dependence. The control sample A with no buffer (i.e. a SI substrate) exhibited voltage invariant capacitance. In subsequent measurements, the samples with activated channels will be referred to by the same labels as the buffer or the substrate on which they are formed.

5.1.4a Transport Characteristics

Average transport parameters at room temperature are derived from the van der Pauw technique and are shown in Table 5.10.

Table 5.10. Room temperature Hall parameters

sample	sheet resistance ρ_s ($\Omega/\square$)	mobility ($cm^2/V\text{-}sec$)	sheet carrier concentration $n_s(cm^{-2})$	% Activation
A	487	4215	3.03×10^{12}	76
B	650	3727	2.56×10^{12}	64
C	634	3898	2.53×10^{12}	63
D	577	3937	2.74×10^{12}	69
E	598	3627	2.87×10^{12}	72

Comparing Tables 5.9 and 5.10, no correlation exists between the active layer sheet resistance and the voltage dependence of the Hg probe capacitance of the corresponding as-grown $Al_{.35}Ga_{.65}As$ buffer layers.

The temperature dependence of Hall mobility (μ) of the above samples is shown in Fig. 5.24.

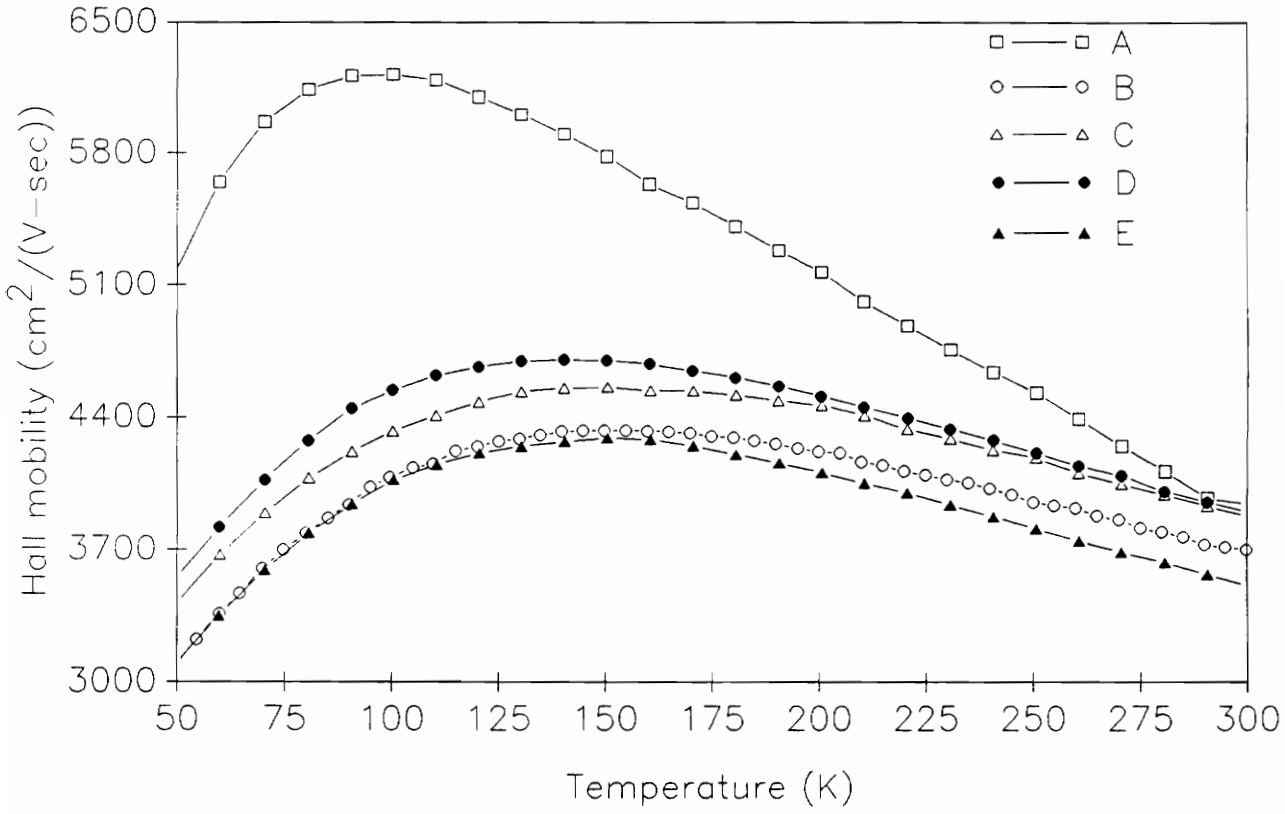


Fig. 5.24 Temperature dependence of Hall mobility of control and $Al_{.35}Ga_{.65}As$ buffer samples.

At low temperatures, the mobilities in the active layers on an $Al_{.35}Ga_{.65}As$ buffer are considerably lower than the no-buffer sample. At near room temperature, however, the mobility values are relatively close (see Fig. 5.24). The peak mobility in the no-buffer sample (A) is 6468 $cm^2/(V\text{-sec})$ and occurs at 100 K. The $Al_{.35}Ga_{.65}As$ buffered samples (B-E) have peak mobilities between 4300-4700 $cm^2/(V\text{-sec})$ at temperatures between 140 - 150 K. Not only is the peak mobility higher in A (by 1.38 to 1.50 times), the impurity scattering limited mobility regime in it dominates over a shorter temperature range than in the $Al_{.35}Ga_{.65}As$ buffer samples. The Hall mobility in A varies as $T^{0.56}$ at low temperatures (impurity scattering limited) and as $T^{-0.61}$ at higher temperatures (lattice scattering limited). The samples with an $Al_{.35}Ga_{.65}As$ buffer have $\mu \sim T^{0.49}$ and $\mu \sim T^{-0.33}$ at low and high temperature regimes, respectively. This difference in mobility behavior between the control and the $Al_{.35}Ga_{.65}As$ buffer samples is attributed to impurities or defects originating from the buffer layer and diffusing into the overlying GaAs layer. No direct correlation exists between the mobility characteristics and the voltage dependent capacitance behavior of the corresponding as-grown buffers.

The variation of sheet carrier concentration (n_s) of the samples in the temperature range 50 - 300 K is shown in Fig. 5.25. It is clear that samples C, D, and E have an anomalous rise in n_s at temperatures below about 190 K. The best of the $Al_{.35}Ga_{.65}As$ buffer samples (i.e. B, which had the least voltage dependent capacitance on the as-grown buffer) has this rise in n_s to a significantly lesser extent and at much lower temperature (below 70 K) than the remaining buffer samples. The control sample A shows the expected variation of n_s with temperature. The anomalous rise in sheet carrier concentration with decreasing temperature is probably due to the conduction in the impurity band [186]. A similar effect has also been reported in ion implanted and annealed VPE GaAs, where the effect has been assigned to a change in the scattering factor value which otherwise is assumed to be unity [178].

The room temperature Hall concentration and mobility profiles in samples A, B, and D are shown in Figs. 5.26, 5.27, and 5.28, respectively. Two striking differences are evident in these figures.

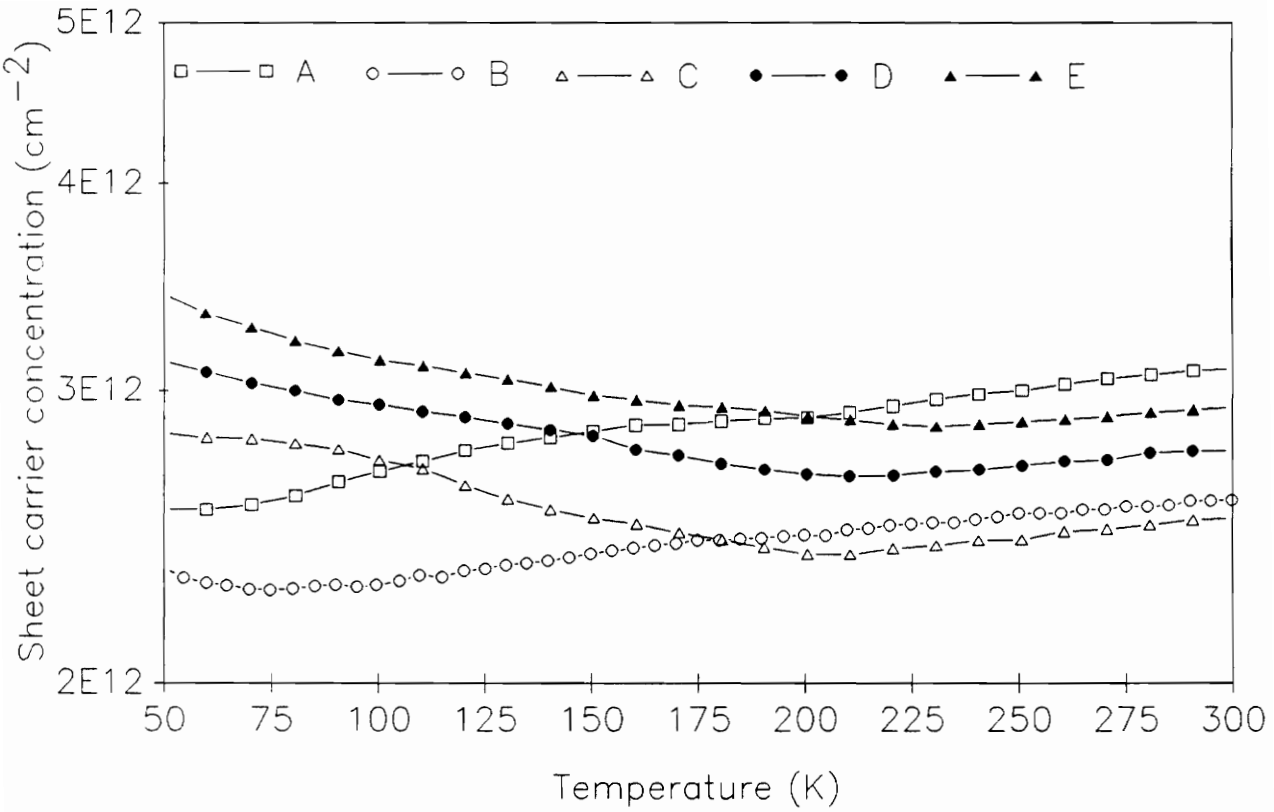


Fig. 5.25 Temperature dependence of sheet carrier concentration of control and $Al_{.35}Ga_{.65}As$ buffer samples.

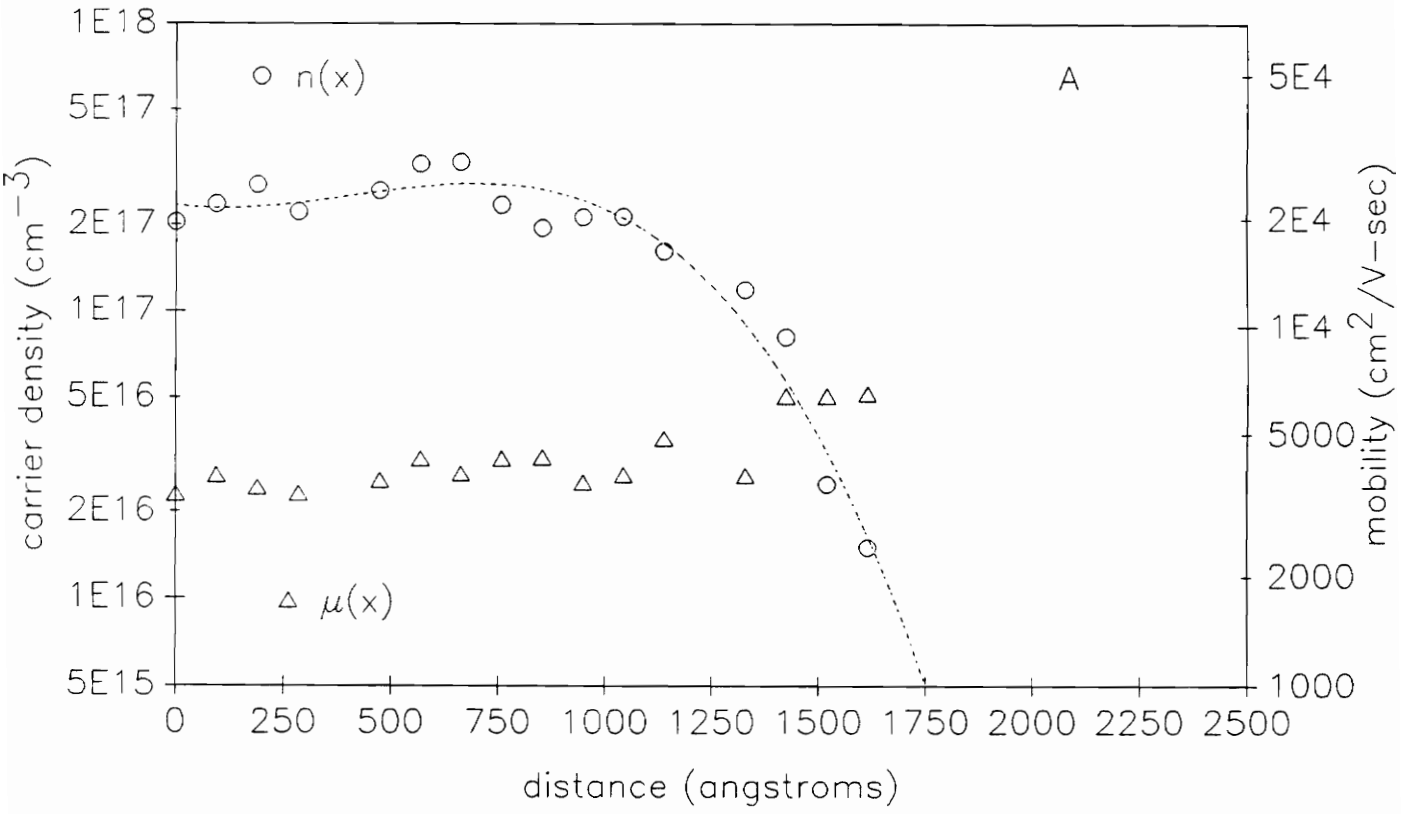


Fig. 5.26 Carrier concentration and Hall mobility profiles versus distance for sample A (no-buffer).

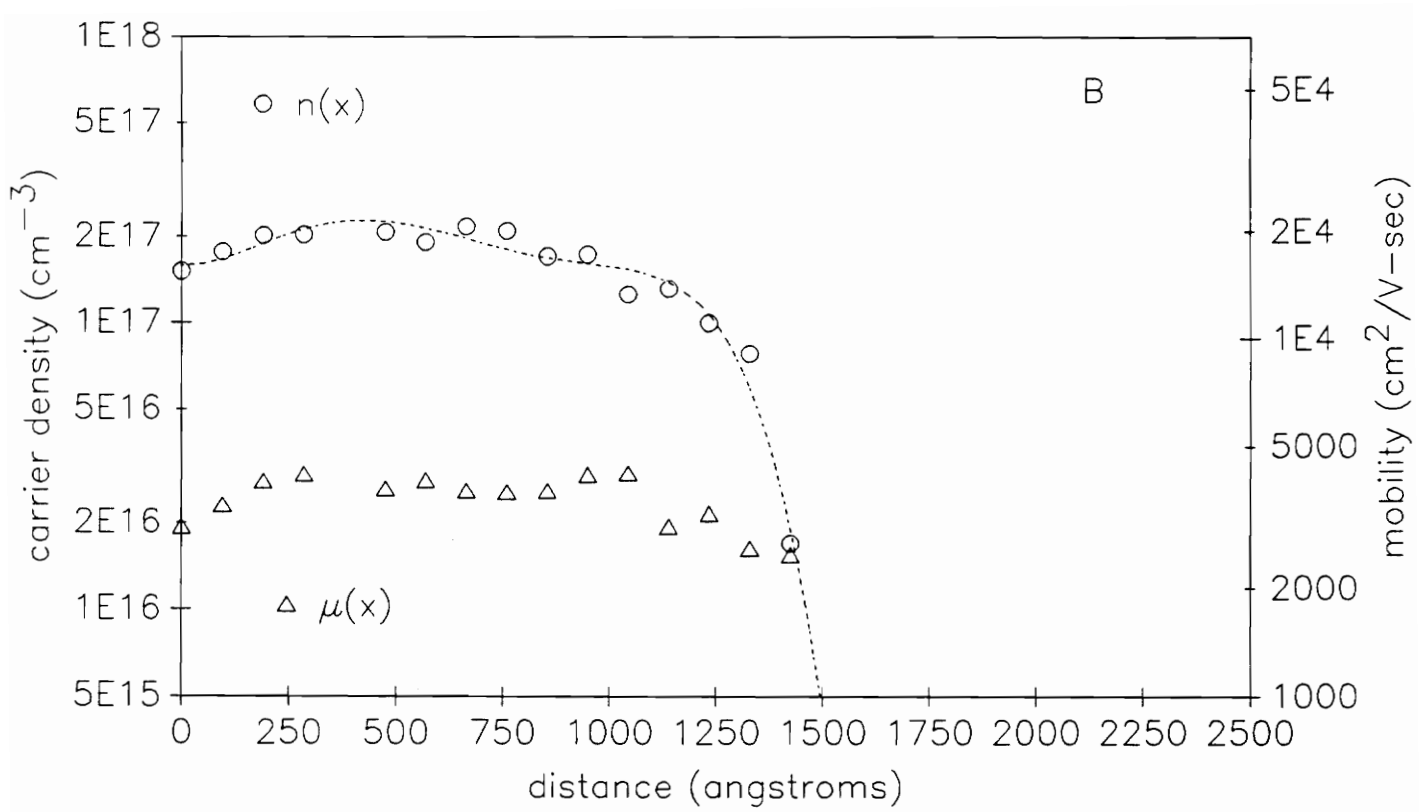


Fig. 5.27 Carrier concentration and Hall mobility profiles versus distance for sample B (with $Al_{.35}Ga_{.65}As$ buffer).

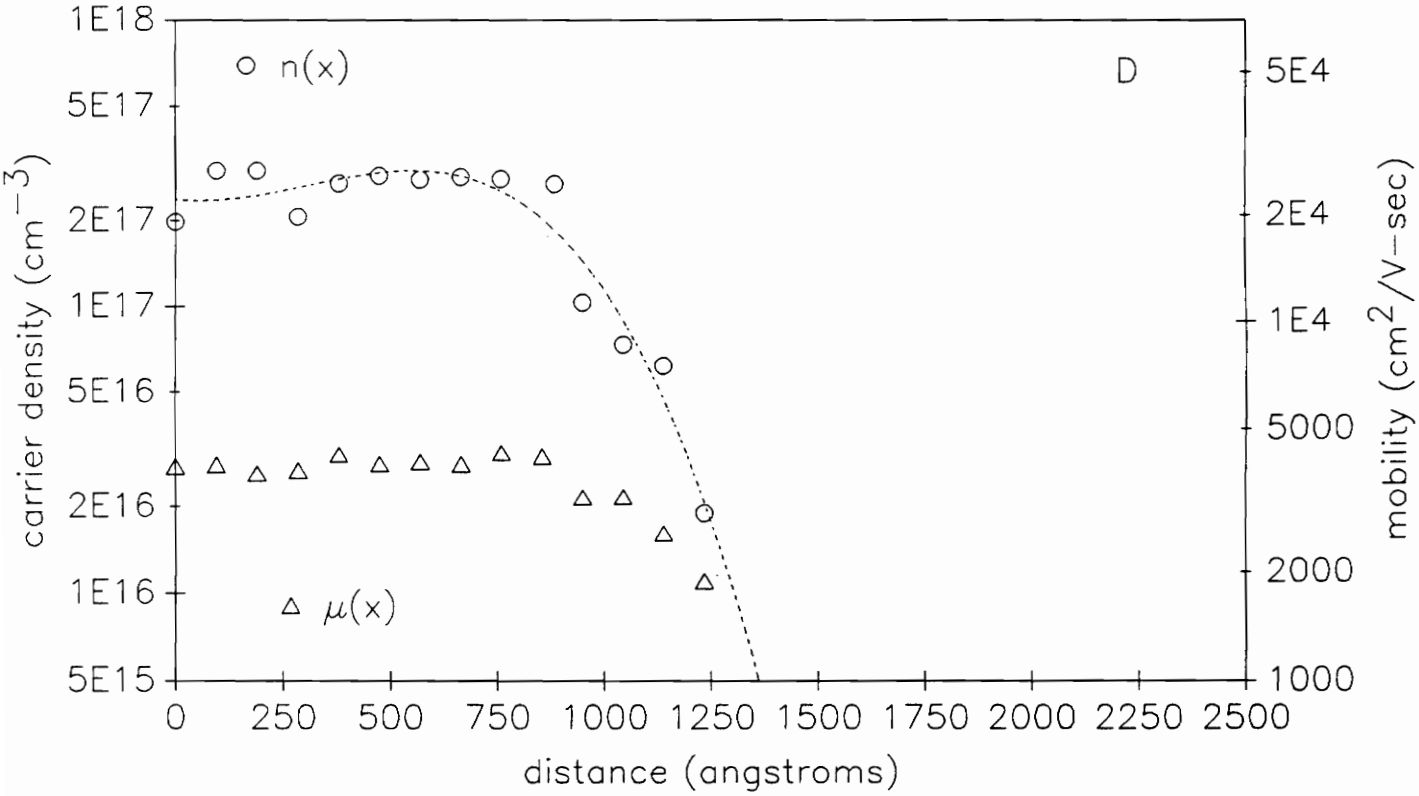


Fig. 5.28 Carrier concentration and Hall mobility profiles versus distance for sample D (with $Al_{.35}Ga_{.65}As$ buffer).

First, the samples with the $Al_{.35}Ga_{.65}As$ buffer (B and D) have sharper carrier profiles than the no buffer case (sample A), with profile being the sharpest in sample D. Second, mobility in the control sample A increases through the active-substrate interface, while in samples B and D it decreases across the interface between the active layer and the buffer. The interface mobility in sample A increases by about 52 % over the average mobility in the active layer. On the contrary, mobility across the interface decreases (by about 33% for sample B and 52% for sample D) from the effective mobility of the active layer. It is interesting to note that the percent decrease in mobility at the interface is apparently linked to the voltage dependence of Hg probe capacitance of as-grown $Al_{.35}Ga_{.65}As$ layers (refer to Table 5.9). The decrease in interface mobility is less for the sample whose Hg probe capacitance of the as-grown buffer showed weak voltage dependence (e.g. sample B). Sample D has a higher mobility reduction and so is its modest dependence of the buffer layer capacitance on voltage. These results reiterate the presence of defects and impurities in the $Al_{.35}Ga_{.65}As$ buffer and in the inactive region of the overlying GaAs. As a result, deep or shallow levels (depending upon the impurity type) are created and are believed to be responsible for the interface-mobility reduction and also for the abrupt carrier profiles in the channels of the buffer samples. The Hall profiles of the control sample reflect the cleanliness of the interface between the active channel and the SI substrate and that the interface is relatively defect free. This fact was further confirmed by the I-V (Current-Voltage) characteristics of the samples between two ohmic contacts after the top active layer was chemically etched away. The I-V characteristics, measured on a Tektronix-575 curve tracer, of the buffer samples (B and D) exhibited significant looping (hysteresis) while in the control sample the looping was almost negligible.

5.1.4b Deep Level Characteristics

Electron traps in the active layers of samples A, B, C, and E were characterized by using deep level transient spectroscopy. A typical DLTS spectrum of the control sample A is shown in Fig. 5.29.

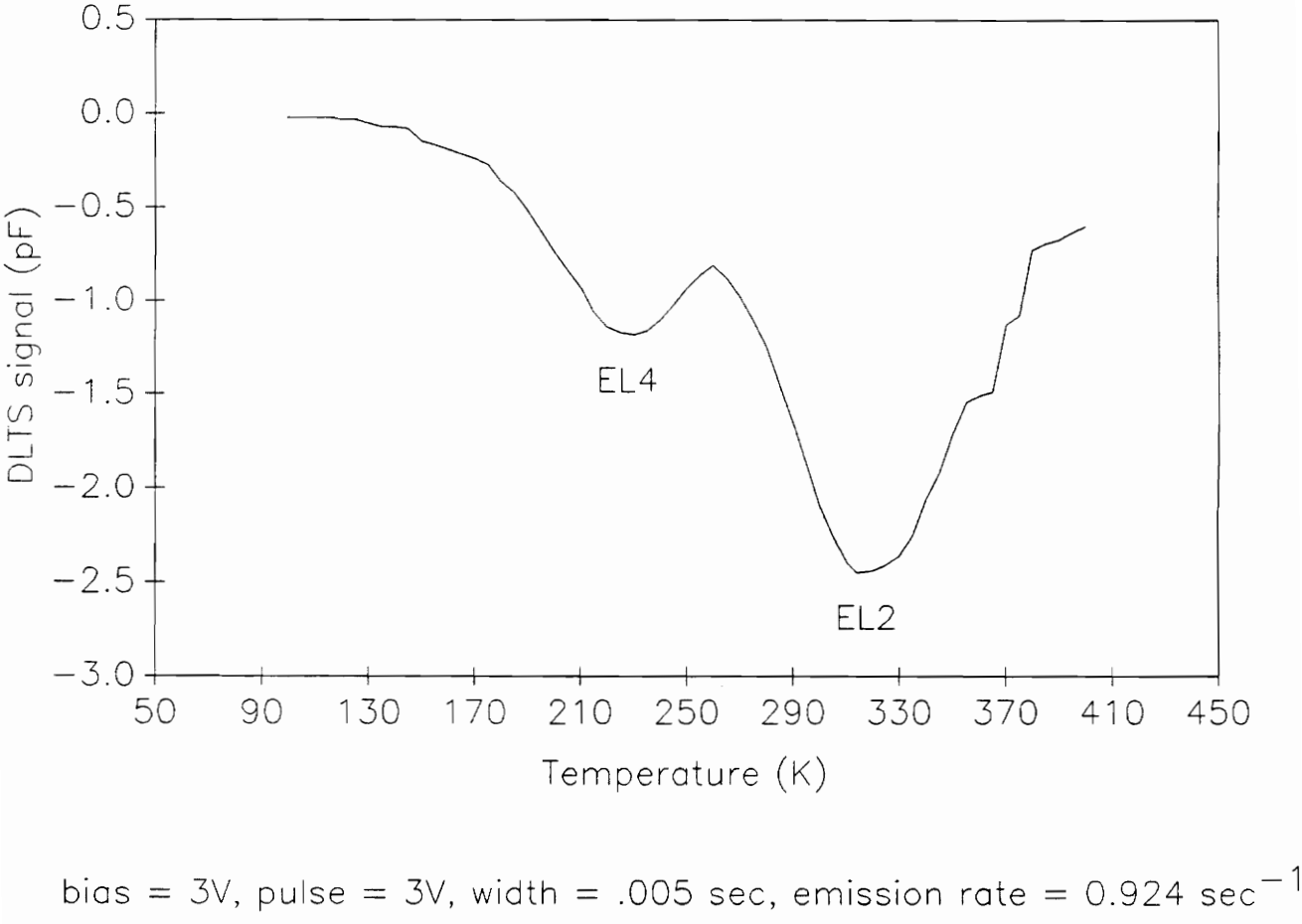


Fig. 5.29 DLTS spectrum of control sample A (150 keV Si-implanted and 827 °C furnace annealed SI GaAs).

There are two electron traps levels and they correspond to traps residing at depths between 0.16 and 0.25 μm from the sample surface. This implies that the region probed in DLTS is in most part the implant tail of the active layer (refer to Fig. 5.26). The details of the trap characteristics are presented in Table 5.11. The spectrum in Fig. 5.29 reveals a trap level at E_c-0.54 eV and is similar to EL4, a level already identified in 50 keV Si-implanted and RTA activated LEC GaAs (refer to section 5.1.1b). This level, as mentioned earlier, is due to implantation damage residual after annealing. Interestingly, this level was detected in both 150 keV Si-implanted and furnace annealed and 50 keV Si implanted and rapid thermal annealed GaAs samples. These results indicate that EL4 is independent of the type of annealing method. Also energy as low as 4 keV Ar^+ (and no annealing) generated this defect. Therefore EL4 defect levels in these samples are characteristics of the ion processing damage.

Also present in the spectrum of sample A is a level at E_c-0.75 eV, and is comparable to EL2. This level may originate from the substrate, or may be due to the damage or due to the effects of both. Substrate contribution to this defect center is very reasonable to expect, at least partially, since EL2 is the main source of compensation in all undoped LEC GaAs substrates.

It is now appropriate to refer back to section 5.1.3b where an identically processed no buffer fat FET (sample I) revealed no features in DLTS for regions probed in the channel and near the interface. The DLTS results of control fat FET (sample I) and of sample A are astonishingly different (refer to Figs. 5.16 and 5.29) in spite of both having identical starting substrates and identical implantation and annealing parameters. The only differences in processing occurred during annealing; for fat FET, a SiON encapsulant was on top of the already defined TiWN gate, while sample A had an SiON encapsulant in direct contact with the whole region of the wafer. Since all other processing conditions remain unaltered, the contrasting deep level spectrum is attributable to the effects of TiWN gate during annealing. In the fat FET, the regions investigated in DLTS were directly underneath the TiWN gate while the probed region in sample A was under the SiON cap during annealing. The DLTS results suggest that during annealing the diffusion characteristics of defects in GaAs are

significantly different under a TiWN and a SiON layer. Based on the DLTS results and relating them back to the processing conditions, it is proposed that during furnace annealing for 20 mins. at 827 °C, the defects responsible for EL2 and EL4 strongly out-diffuse into the TiWN gate. Since two trap states levels were identified in sample A, such an out-diffusion behavior, if any, is not so strong under a SiON capping layer. Therefore, the reason for flat DLTS spectra of fat FET samples discussed in section 5.1.3b is due to out-diffusion of electron traps, definitely EL2 and EL4, into the TiWN gate during furnace annealing.

The deep level spectra of samples with $Al_{.35}Ga_{.65}As$ buffer, i.e. samples B, C, and E, are shown in Figs. 5.30, 5.31, and 5.32, respectively. The corresponding trap parameters are listed in Table 5.11. In all the buffer samples there are two main electron levels; one near EL4 (E_c-0.52 eV) and the other being close to EL2 (E_c-0.75 eV). As in sample A, the DLTS measurements on buffer samples also probed regions partly in the implant tail and the remaining part in the GaAs epi immediately beneath the channel. The only difference between the DLTS results of no-buffer (control) and $Al_{.35}Ga_{.65}As$ buffer samples being the relative peak intensities of the two identified levels. EL2 is a dominant trap level in the control sample but EL4 is a dominant center in the buffer samples B, C, and E. The reason for this difference in the deep level characteristics of the two sample types is not well understood. It can be speculated however, that the diffusion of defects from the $Al_{.35}Ga_{.65}As$ buffer towards the overlying GaAs channel during activation annealing has an impact in partially compensating or annihilating EL2. Another possible reason may be the defects existing in the top part of the sample i.e. the channel region of the substrate, prior to implantation. For sample A, the starting substrate is SI LEC GaAs and hence there is significant concentration of EL2. For samples B, C, and E, the implantation were made into MBE grown GaAs epi-layers, where EL2 is normally absent. The appearance of EL2 in samples B, C, and E is, in all likelihood, associated with the implantation and annealing process. Also conspicuous in the results is the absence of well known MBE growth related trap levels i.e. M1 (0.18 eV), M2 (0.27 eV), M3 (0.30 eV), M4 (0.50 eV) in GaAs

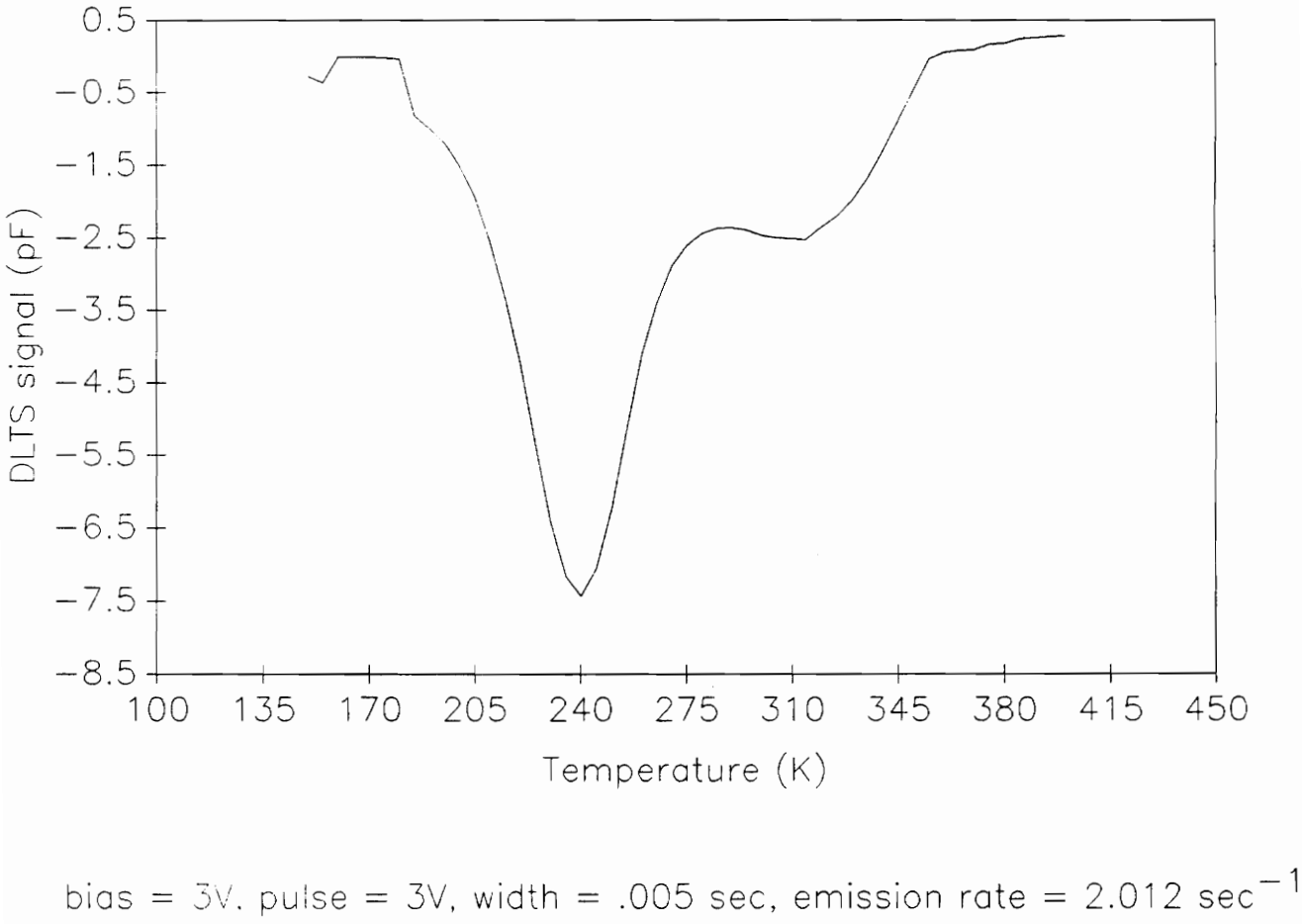


Fig. 5.30 DLTS spectrum of sample B (150 keV Si-implanted and 827 °C furnace annealed MBE GaAs grown on $Al_{.35}Ga_{.65}As$ buffer).

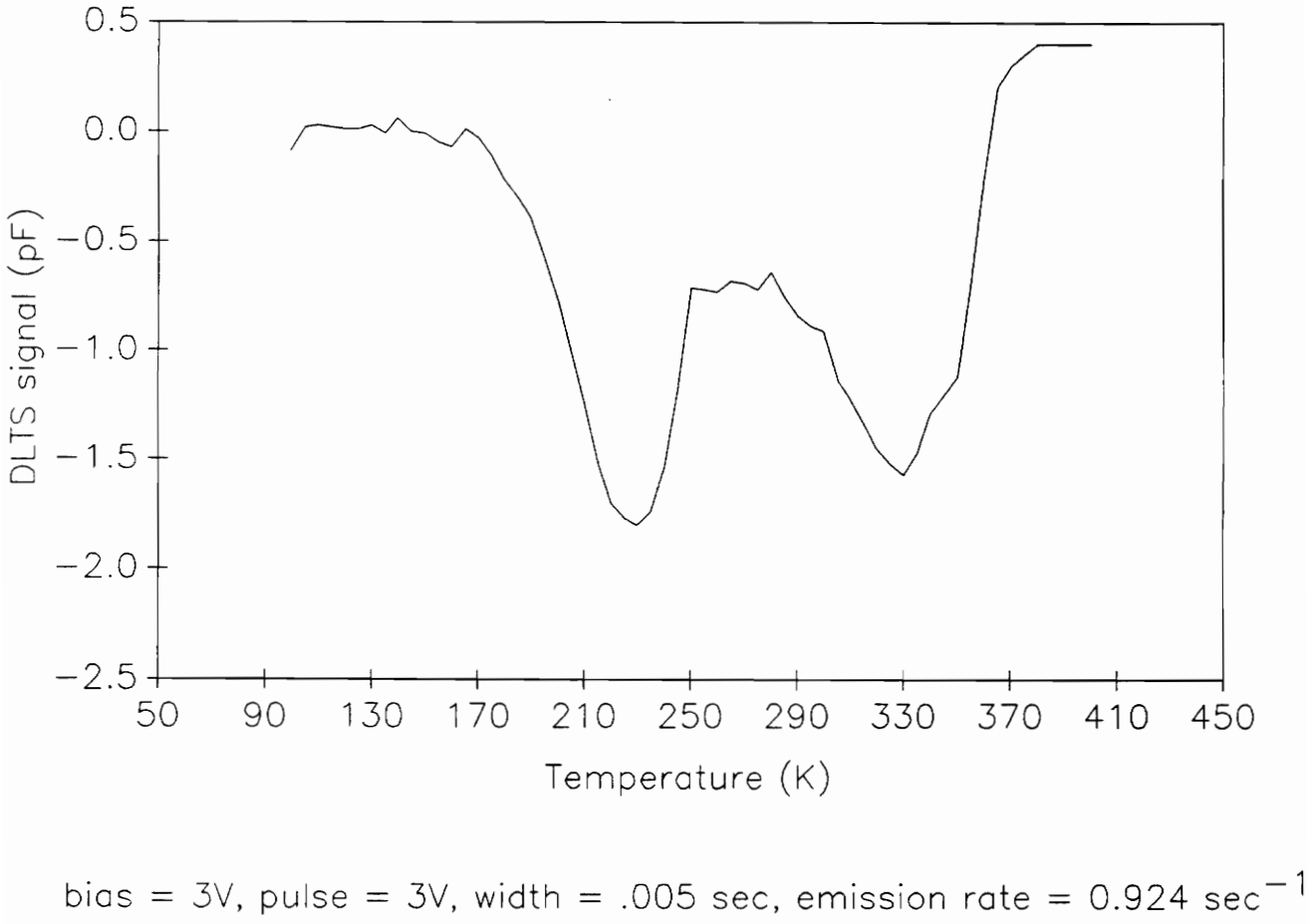


Fig. 5.31 DLTS spectrum of sample C (150 keV Si-implanted and 827 °C furnace annealed MBE GaAs grown on $Al_{.35}Ga_{.65}As$ buffer).

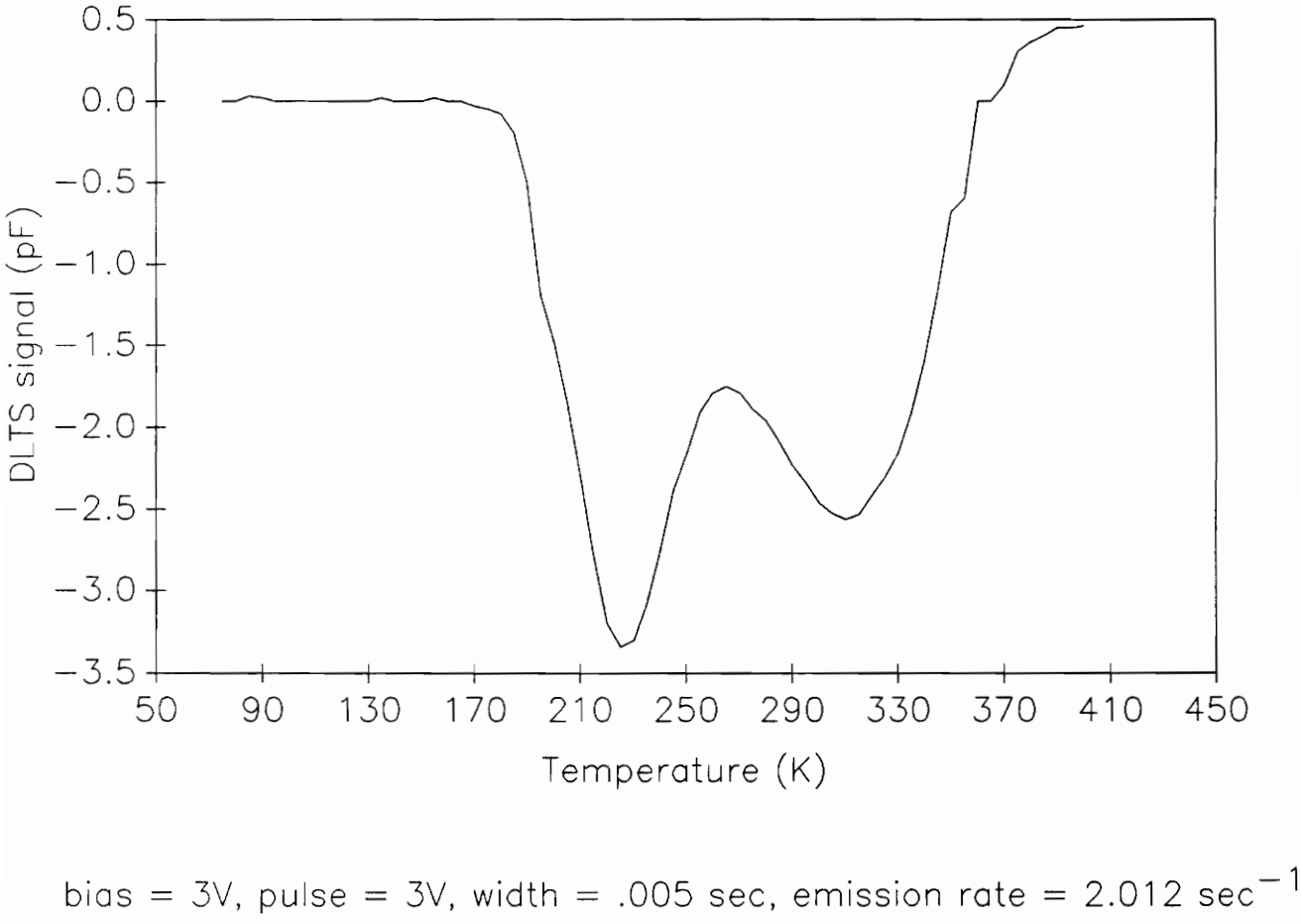


Fig. 5.32 DLTS spectrum of sample D (150 keV Si-implanted and 827 °C furnace annealed MBE GaAs grown on $Al_{.35}Ga_{.65}As$ buffer).

Table 5.11. Trap parameters of Si-implanted channels on no-buffer and $Al_{35}Ga_{65}As$ buffer layers.

sample	E_C-E_T (eV)	N_T/N_D	Possible designation
A	0.55	.022	EL4
	0.76	.045	EL2
B	0.55	.097	EL4
	0.73	.032	EL2 or EL12
C	0.54	.027	EL4
	0.77	.023	EL2
D	0.53	.045	EL4
	0.72	.035	EL2 or EL12

[32]. However, there has been a report by Xin *et al.* [37] that the concentration of traps in MBE GaAs can be significantly reduced either by capless or Si_3N_4 capped heat-treatment. Therefore, on the basis of the above discussion, the following comments are noteworthy :

1. Higher EL2 concentration in sample A than in samples B, C, and E can be explained via the contribution due to EL2 originally existing in the substrate. This additive contribution from the substrate to the total EL2 concentration is missing in the buffer samples.
2. The implantation and annealing process are such that the MBE related traps in GaAs become obscured (below the sensitivity limit of the measurement) in samples B, C, and E.
3. EL2 seen in samples B, C, and E is very likely generated as result of implantation and furnace annealing.

The DLTS measurements performed at other depths in the buffered samples showed no additional trap levels. There was no clear correlation between the relative trap concentration and the depth position from the sample surface. The space charge edge could not be driven into the buffer layer because of the channel breakdown. It is apparent that the DLTS results on channels of samples A, B, C, and E do not offer any significant understanding to the cause for variability of V_{th} of FETs on $Al_{.35}Ga_{.65}As$ buffer. The results however answer other additional questions; namely the reason for flat DLTS spectra for no buffer fat FET (sample I), if EL2 can be created by implantation and annealing, and the cause for the suppression of MBE related traps in the spectra of $Al_{.35}Ga_{.65}As$ buffer and LT GaAs buffer samples. In an attempt to clarify the unanswered questions on the characteristics of $Al_{.35}Ga_{.65}As$ buffer FETs and the role of buffer layer, SIMS (Secondary Ion Mass Spectroscopy) measurements were performed on these samples and are described in the next section.

5.1.4c SIMS Analysis

SIMS (Secondary Ion Mass Spectroscopy) characterization was performed in a Perkin Elmer

PHI model 3500 SIMS 011 spectrometer. SIMS measurements on no-buffer (A) and $Al_{.35}Ga_{.65}As$ buffer samples (C and E) were done using a 4 keV Ar^+ beam at beam current of 4 μA and at an incident angle of 45°. The elemental profiles of Mn, Mg, Si, Cr, Cu, and C in sample A have shown very low signal counts and their concentration levels were buried in the background noise. These impurities were probed up to a depth of 0.5 μm from the sample surface. SIMS profiles of various impurities in samples C and E are shown in Figs. 5.33 and 5.34, respectively. Some of the notable results from the SIMS study are as follows:

1. $Al_{.35}Ga_{.65}As$ buffer layers have significant concentrations of Mn and there is an evidence of Mn diffusing into the top GaAs layer from the buffer. There is some uncertainty in the SIMS signal from Mn because of its atomic mass being equivalent to KO^+. But, owing to the nature of the samples, presence of Mn is more likely than the species bearing KO^+.
2. Sample E has appreciable concentrations of Mg and Cr, both in buffer and active layers. Sample C has an approximately similar concentration of Mg but an almost negligible concentration of Cr.
3. There are significant amounts of Si in the $Al_{.35}Ga_{.65}As$ buffer of sample E and also in the buffer of sample C, but to a lesser extent.
4. The control sample A had Mn, Mg, Si, and Cr concentrations below the instrument's detection limit (< 10 atomic counts per sec.).

The rise in signal counts of Mn and Si from the GaAs layer into the buffer layer across the interface indicates that these impurities are associated with the $Al_{.35}Ga_{.65}As$ buffer and are characteristics of the actual process conditions present during buffer growth. It is interesting to note that sample E, which exhibited maximum voltage dependent capacitance of the as-grown buffer, has higher concentrations of Si and Mn among the two buffer samples investigated. It is believed that these impurities are the cause for the voltage dependent capacitance behavior of the as-grown buffer.

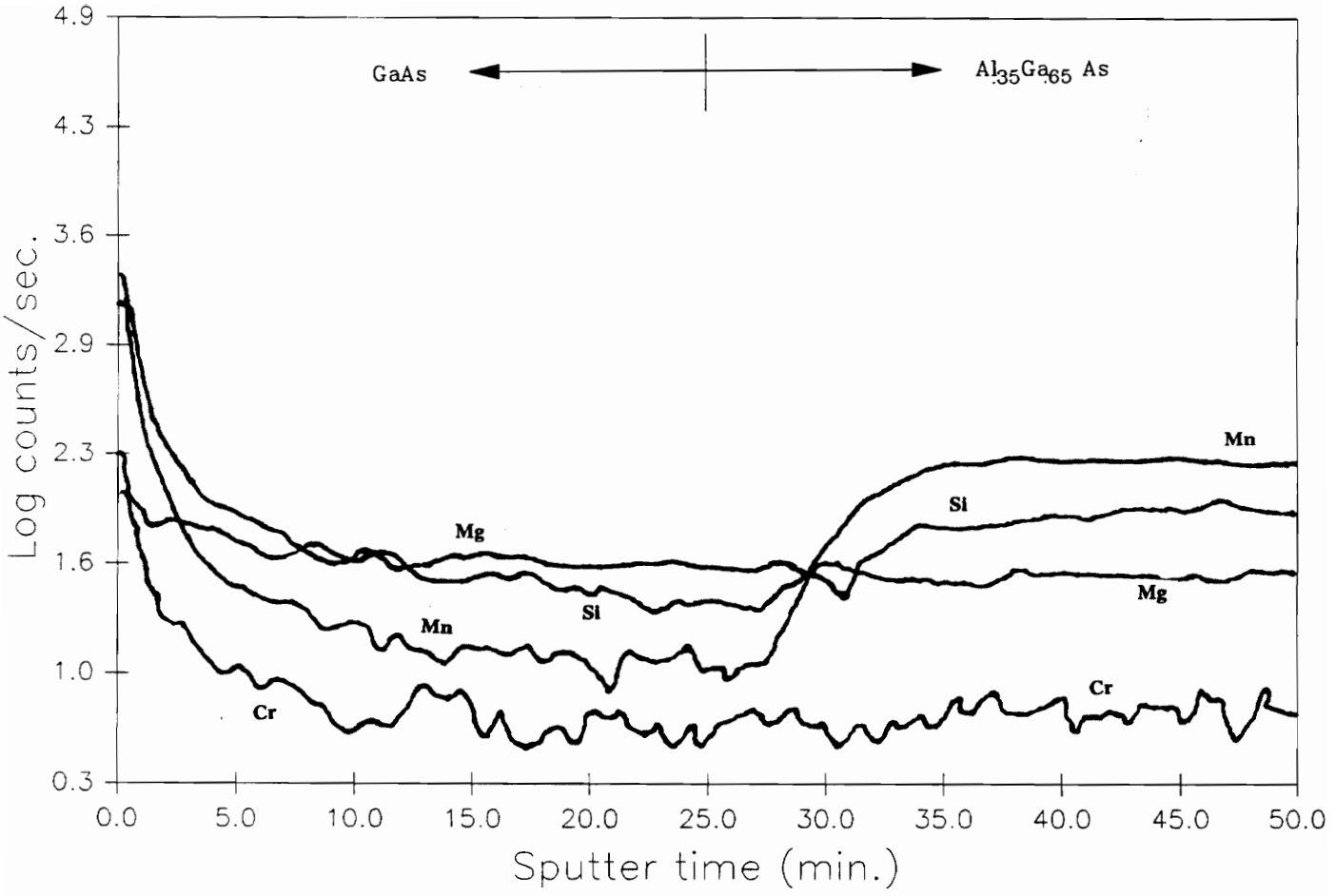


Fig. 5.33 SIMS profiling of impurities in sample C (150 keV Si-implanted and 827 °C furnace annealed MBE GaAs grown on $Al_{.35}Ga_{.65}As$ buffer).

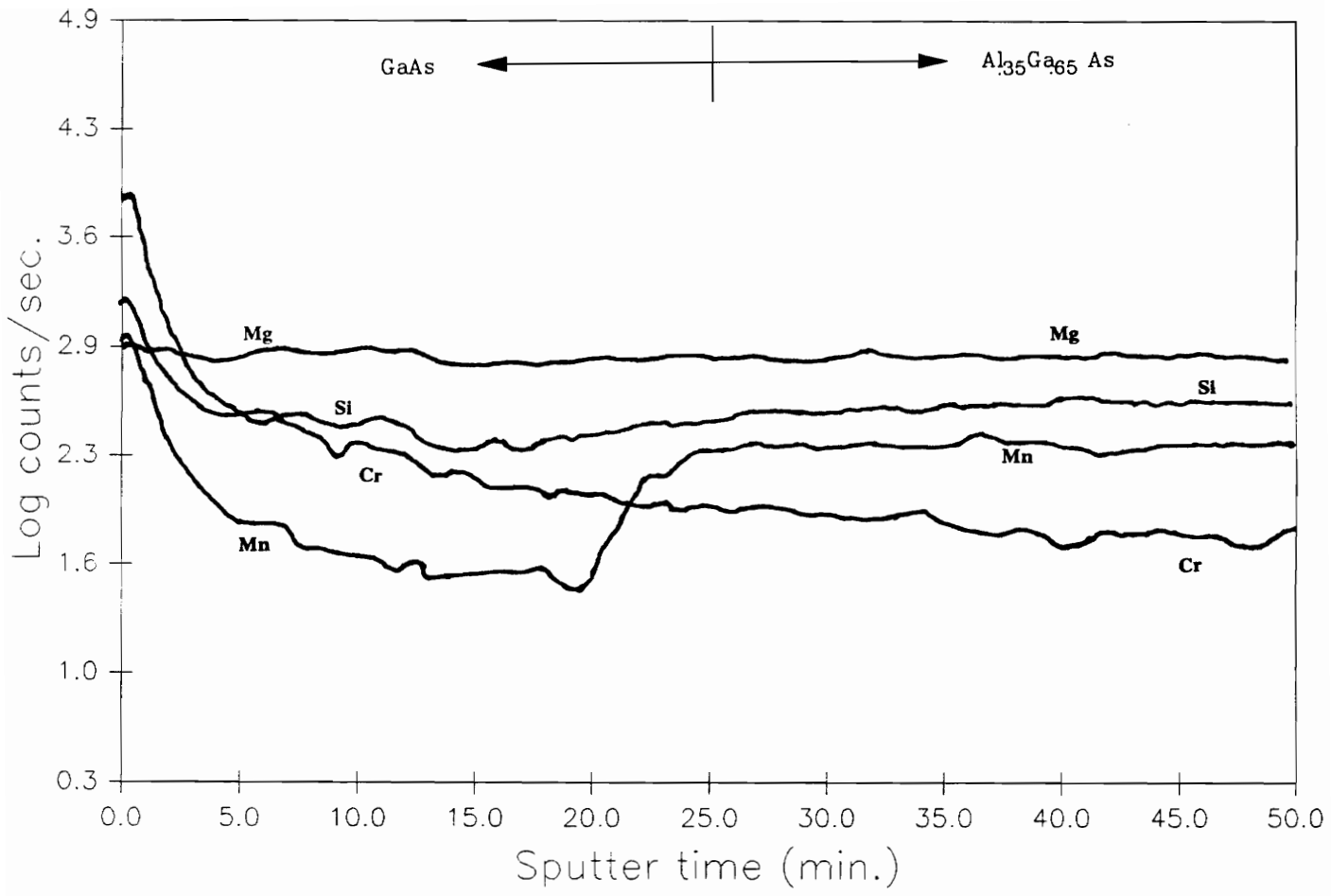


Fig. 5.34 SIMS profiling of impurities in sample E (150 keV Si-implanted and 827 °C furnace annealed MBE GaAs grown on $Al_{.35}Ga_{.65}As$ buffer).

The higher the concentration of these impurities, the greater the voltage dependence of capacitance. Although there is lack of direct correlation between the SIMS results and the peculiarities of FETs on $Al_{.35}Ga_{.65}As$ buffers, the impurities identified in the $Al_{.35}Ga_{.65}As$ buffer appear to affect the FET characteristics in certain ways. The origin of the observed non-uniformities of V_{th} on FETs with $Al_{.35}Ga_{.65}As$ buffer must be due to the impurities in buffer layers, their interaction with implant damage, and their distribution behavior upon thermal treatment. The high concentration of impurities in the buffer are consistent with the decrease in Hall mobility across the interface, as discussed before. The presence of these impurities in the buffer layers also provides an explanation for the unexpected rise in carrier concentration with decreasing temperature as observed in the buffered samples. These impurities form a band of states which provide pathways for conduction and hence the rise in carrier density at low temperatures.

To sum up, the impurities identified in $Al_{.35}Ga_{.65}As$ buffer can help explain the differences in interface mobility behavior in the no-buffer and the buffered samples. These impurities most likely interact with the implantation induced defects and during subsequent annealing form defect complexes. The observed peculiarities of FETs with $Al_{.35}Ga_{.65}As$ buffer i.e. higher g_m, reduced V_{th} can be explained by means of a sharper carrier profile in the channels which in turn may be potentially explained by means of these defect complexes and impurities. There is evidence that immediately underneath the active layer of samples C and E, the concentration of Mg is higher than that of Si. This results in a p-type region below the n-GaAs channel which reduces the effective channel thickness and thus making the carrier profile more abrupt. From the results of majority carrier DLTS on buffer samples, no clear correlation could be obtained between the identified trap parameters and the corresponding FET characteristics. The variation in threshold voltage for FETs on $Al_{.35}Ga_{.65}As$ is likely to be linked with the impurities that are incorporated in the buffer during growth. Although the buffer wafers were identically processed, the impurity contents in them, as measured via SIMS, differed appreciably.

5.2 High Energy MeV Implantation

Megavolt ion implantation, as discussed in Chapter 3, has recently become very attractive in attaining increased level of device integration in a monolithic format [125]. MeV implanted GaAs has a buried active layer , the depth of which is a function of implantation parameters [124,126]. The buried layer quality is extremely critical for the device structures formed on it. The buried channel structure is a promising way to overcome surface related problems in GaAs devices. The key issue in MeV implantation of GaAs is to address the effects of high energy implantation and annealing on the characteristics of near surface and buried layers. Additionally it is also important to understand the fundamental difference in properties of keV and MeV implanted GaAs. In the following sections, a detailed picture on transport and deep level properties of high energy (MeV) Si-implanted and RTA annealed (100) GaAs is presented. The sample history i.e. implantation and annealing parameters, are listed under category E in Chapter 4. All samples were directly MeV implanted into LEC SI GaAs and subsequently RTA activated for 10 sec..

5.2.1 Transport Characteristics

Average Hall mobility and carrier concentration as a function of temperature are shown in Figs. 5.35 and 5.36 for samples N4 (2 MeV 1e13 cm^{-2} Si, 1000 °C RTA) and N9 (6 MeV 1e14 cm^{-2} 1000 °C RTA), respectively. The impurity scattering is evident below 110 K for N4 and 130 K for N9. At higher temperatures, the mobilities are governed by lattice scattering. Because of its lower dose, N4 has higher mobility than N9. The average peak mobilities are 7923 and 3701 cm^2/V-sec for N4 and N9, respectively. The temperature dependence of Hall mobility of two samples is as expected. The variation of carrier concentrations with temperature are slightly different for N4 and N9; being invariant in the former and variant in the latter with a small positive gradient. The rise in carrier density of N9 from 1.02 x 10^{17} cm^{-3} at 70 K to 1.22 x 10^{17} cm^{-3} at 350 K, to a first approximation, is related to a high density of defects in the sample. In addition to higher dose, lower mobility of N9

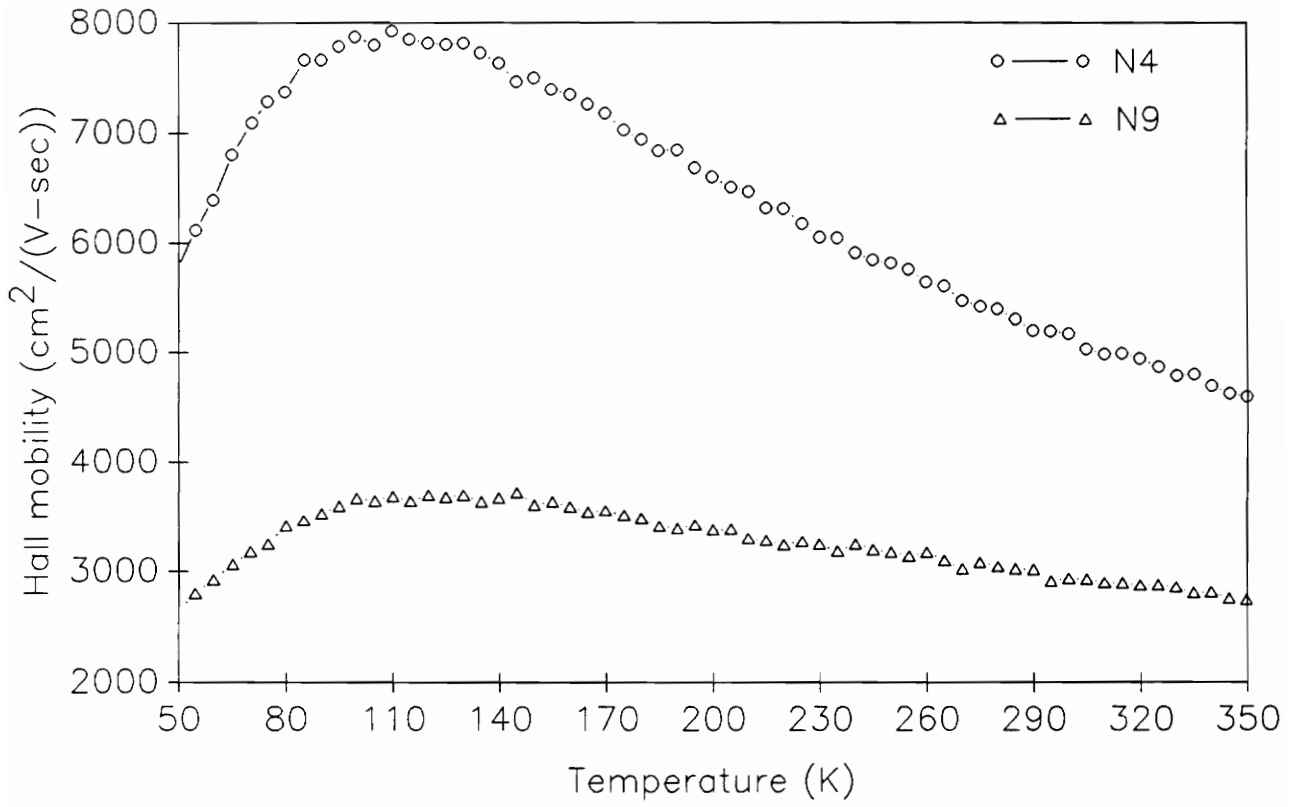


Fig. 5.35 Temperature dependence of average Hall mobility of samples N4 (2 MeV, 1x10^{13} cm^{-2} Si, and 1000 °C RTA) and N9 (6 MeV, 1x10^{14} cm^{-2} Si, and 1000 °C RTA).

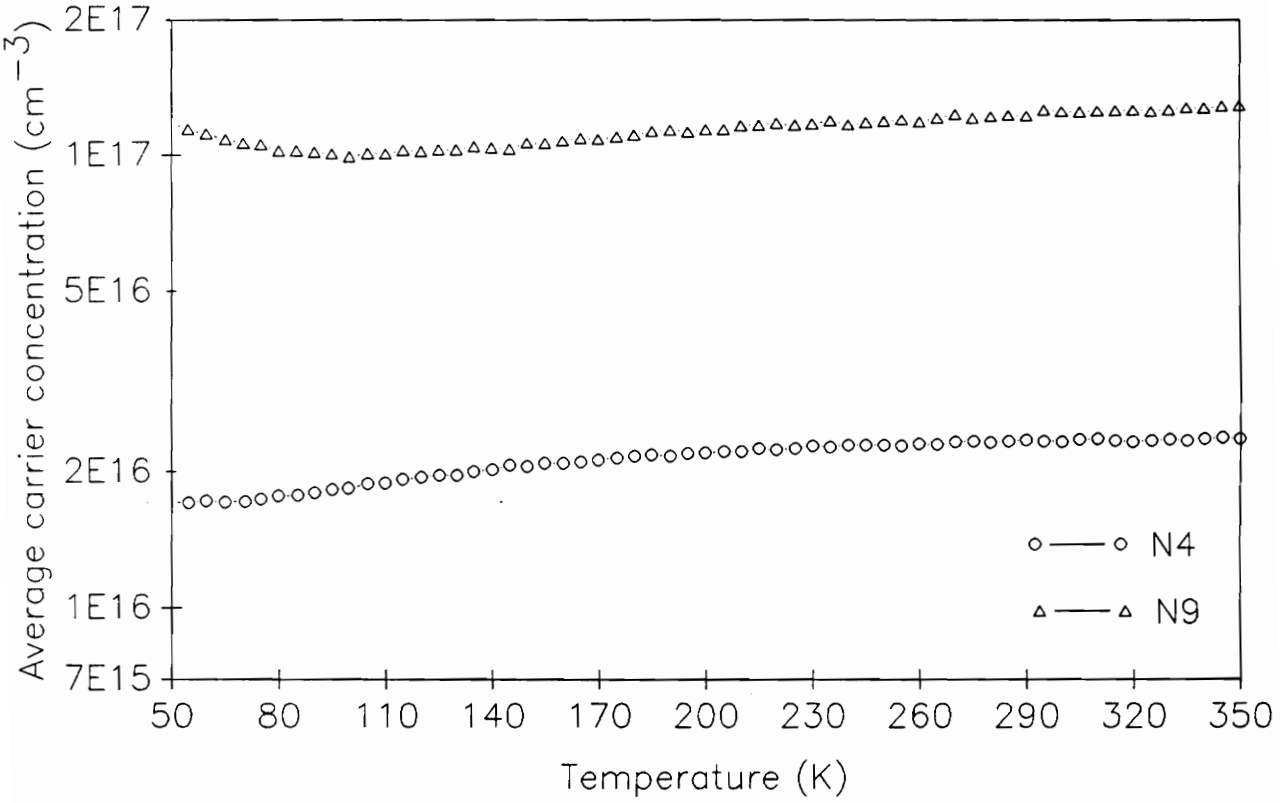


Fig. 5.36 Temperature dependence of carrier concentration of samples N4 (2 MeV, 1x10^{13} cm^{-2} Si, and 1000 °C RTA) and N9 (6 MeV, 1x10^{14} cm^{-2} Si, and 1000 °C RTA).

may also be enhanced by the presence of these defects.

Room temperature carrier concentration profiles of N4 and N9 are presented in Figs. 5.37a and 5.37b, respectively. For the 2 MeV case, the active layer begins at 1 μm and extends up to 3.36 μm deep. The peak concentration of 6.3 x 10^{16} cm^{-3} occurs at a depth of 2.16 μm. In the 6 MeV sample, the buried layer lies between 1.75 and 4.87 μm from the surface. The peak carrier density in this case is 4.8 x 10^{17} cm^{-3} at a depth of 3.8 μm. TRIM-86 [126] calculations for 2 and 6 MeV Si-implanted GaAs have shown that the respective projected ranges (R_p) are 1.41 and 3.04 μm away from the surface. Obviously the experimental profiles of samples N4 and N9 are broader than that predicted by TRIM. This broadening of the Si profiles may be due to channeling and/or radiation enhanced diffusion. Radiation enhanced diffusion is a result of rise in substrate temperature during implantation [128]. The profiles in Fig. 5.37 confirm the presence of buried active layers due to MeV implantation; the depth of which increases with ion energy.

Figs. 5.38a and 5.38b represent Hall mobility profiles and Figs. 5.39a and 5.39b show the resistivity profiles of samples N4 and N9, respectively. At peak carrier density, Hall mobilities are 5420 and 2379 cm^2/V-sec for N4 and N9, respectively. The depths of lowest resistivity correspond to the peak position of their respective carrier profiles. The van der Pauw measurements revealed that the buried layer transport properties of MeV implanted GaAs are at least comparable, if not better, to a similarly processed keV energy Si implanted GaAs (refer to Figs. 5.1 and 5.26).

5.2.2 Deep Level Characteristics

DLTS measurements were performed on 2 and 6 MeV Si-implanted and RTA annealed samples in order to gain an understanding of their deep level properties. Different depths of the implanted buried layers were accessed through a combination of chemical etching (in 1:1:100 by volume of conc. H_2SO_4:30 % H_2O_2:H_2O) and reverse biasing. Typical DLTS spectra for samples N1, N2. N3, and N5 are shown in Figs. 5.40, 5.41, 5.42, and 5.43, respectively. The experimental

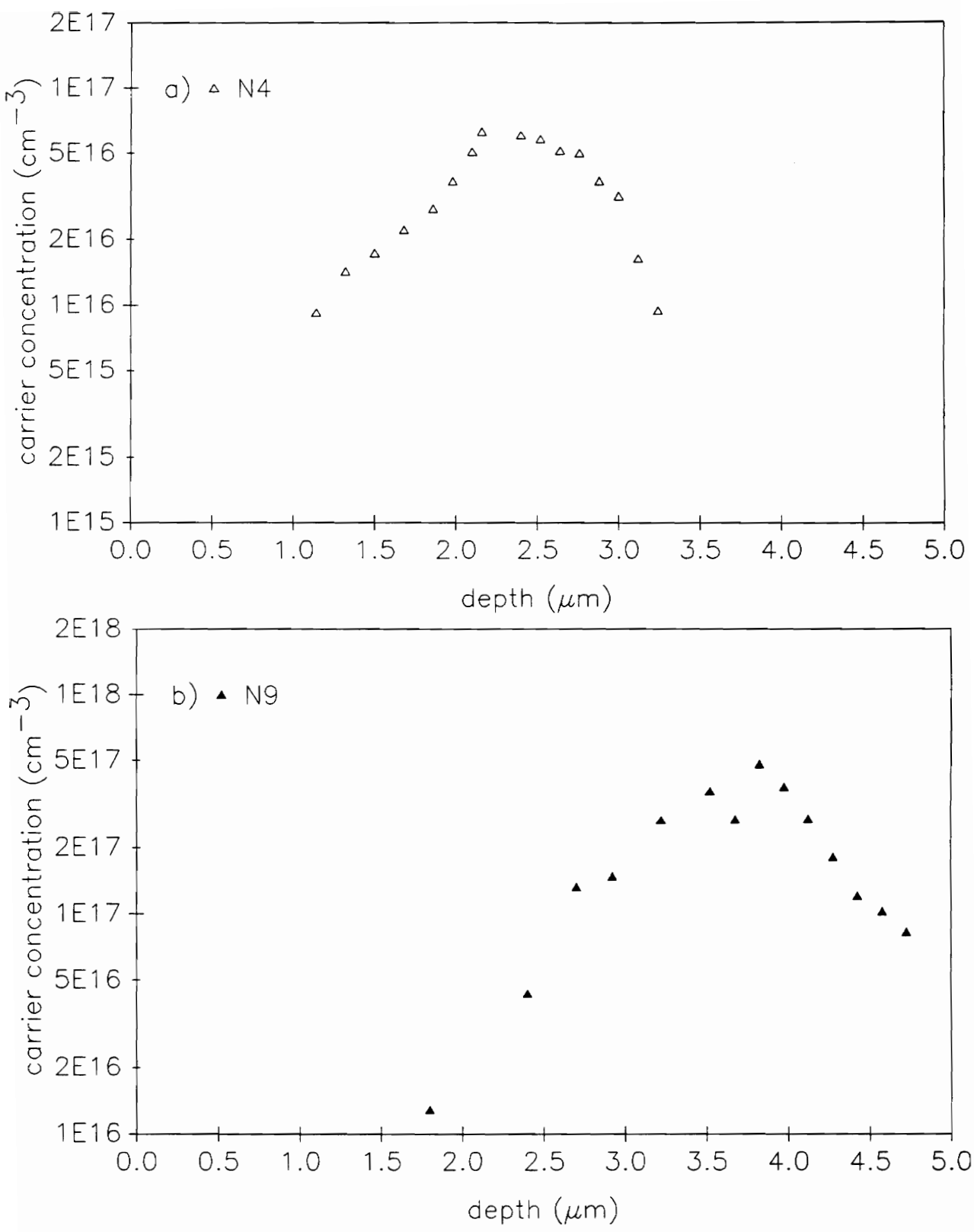


Fig. 5.37 Room temperature carrier concentration profiles of samples: a) N4 (2 MeV, $1x10^{13}$ cm^{-2} Si, and 1000 °C RTA) and b) N9 (6 MeV, $1x10^{14}$ cm^{-2} Si, and 1000 °C RTA).

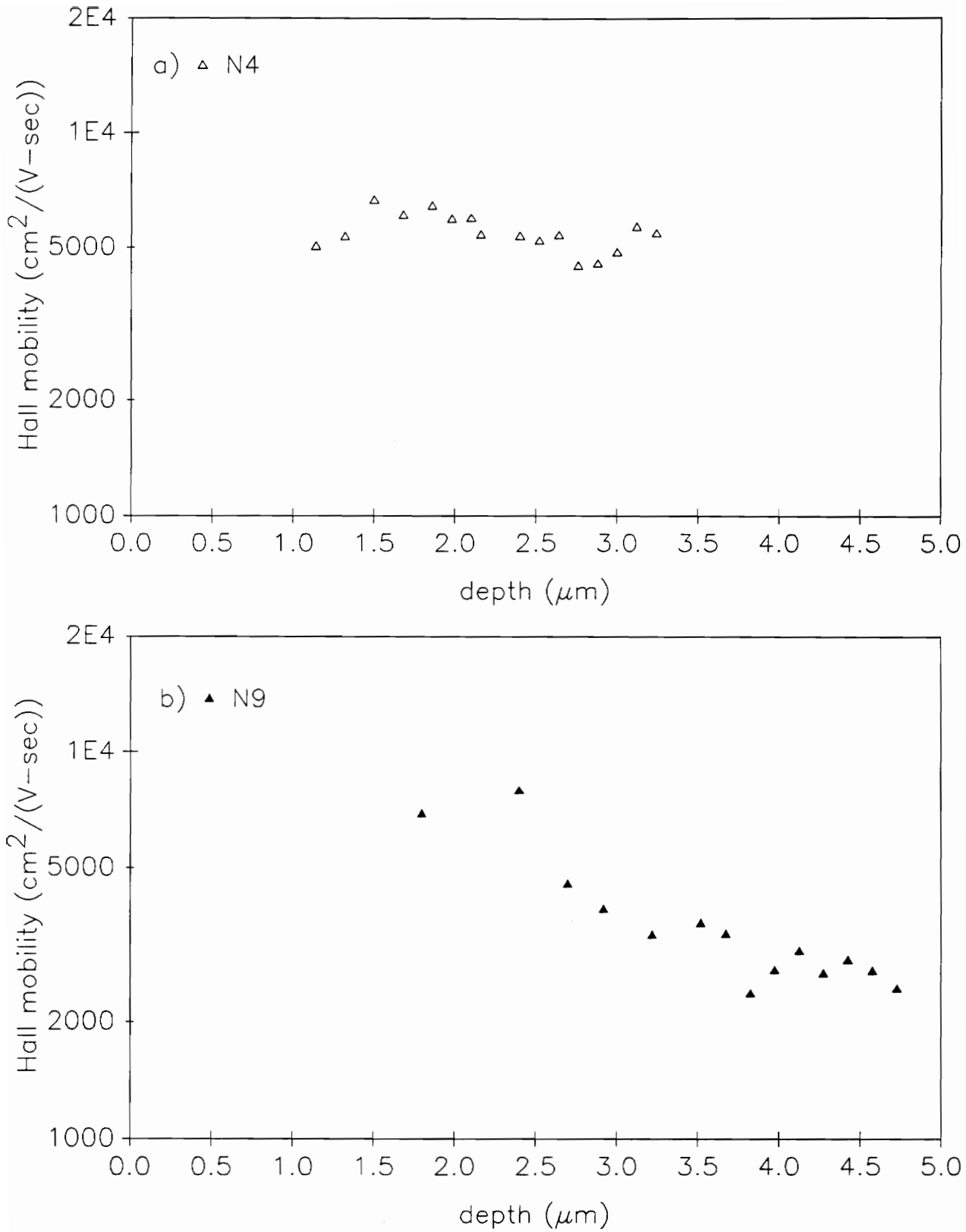


Fig. 5.38 Room temperature Hall mobility profiles of samples: a) N4 (2 MeV, $1x10^{13}$ cm^{-2} Si, and 1000 °C RTA) and b) N9 (6 MeV, $1x10^{14}$ cm^{-2} Si, and 1000 °C RTA).

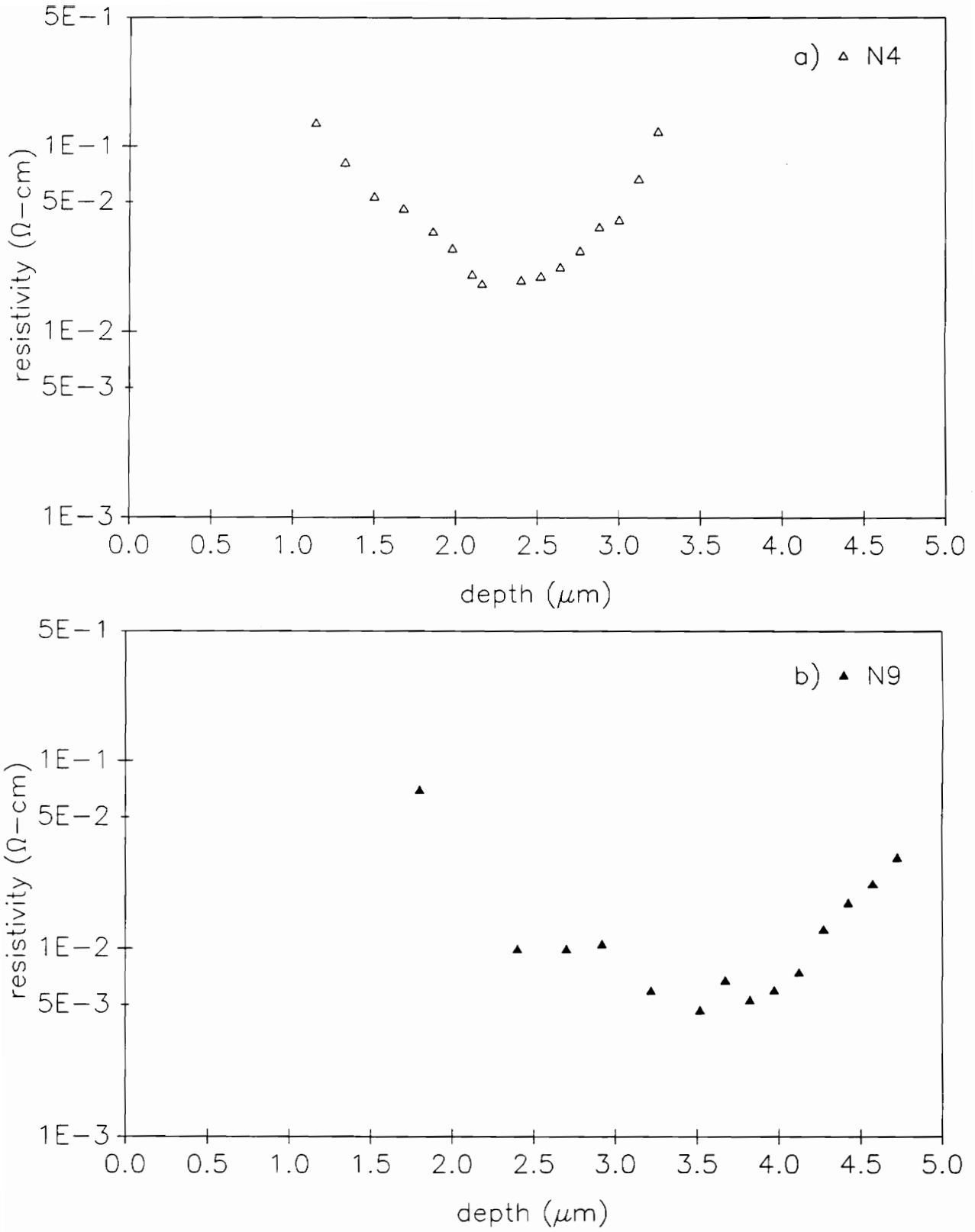


Fig. 5.39 Room temperature resistivity profiles of samples: a) N4 (2 MeV, $1x10^{13}$ cm^{-2} Si, and 1000 °C RTA) and b) N9 (6 MeV, $1x10^{14}$ cm^{-2} Si, and 1000 °C RTA).

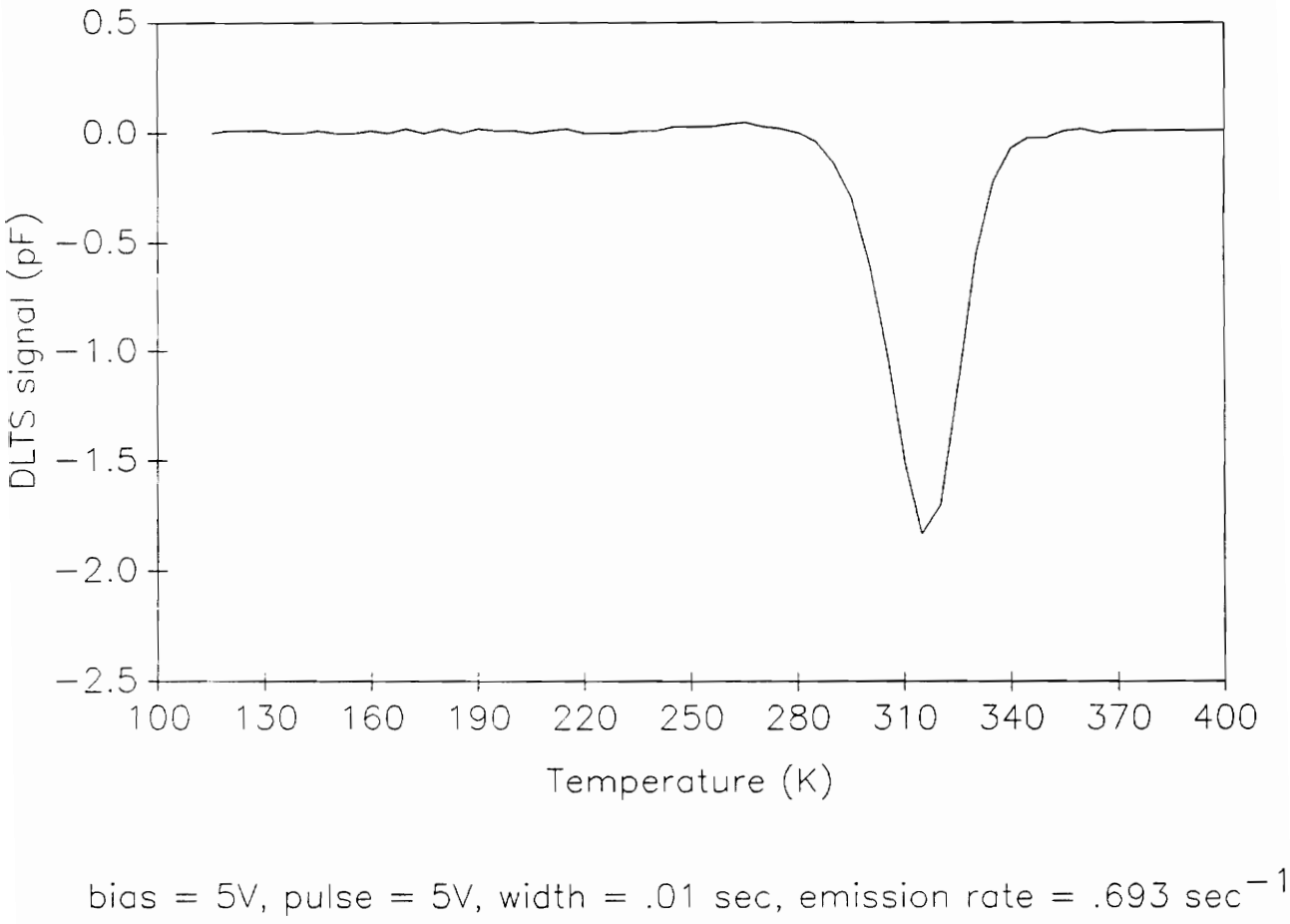


Fig. 5.40 DLTS spectrum of sample N1 (2 MeV, 1e13 cm^{-2} Si, and 850 °C RTA).

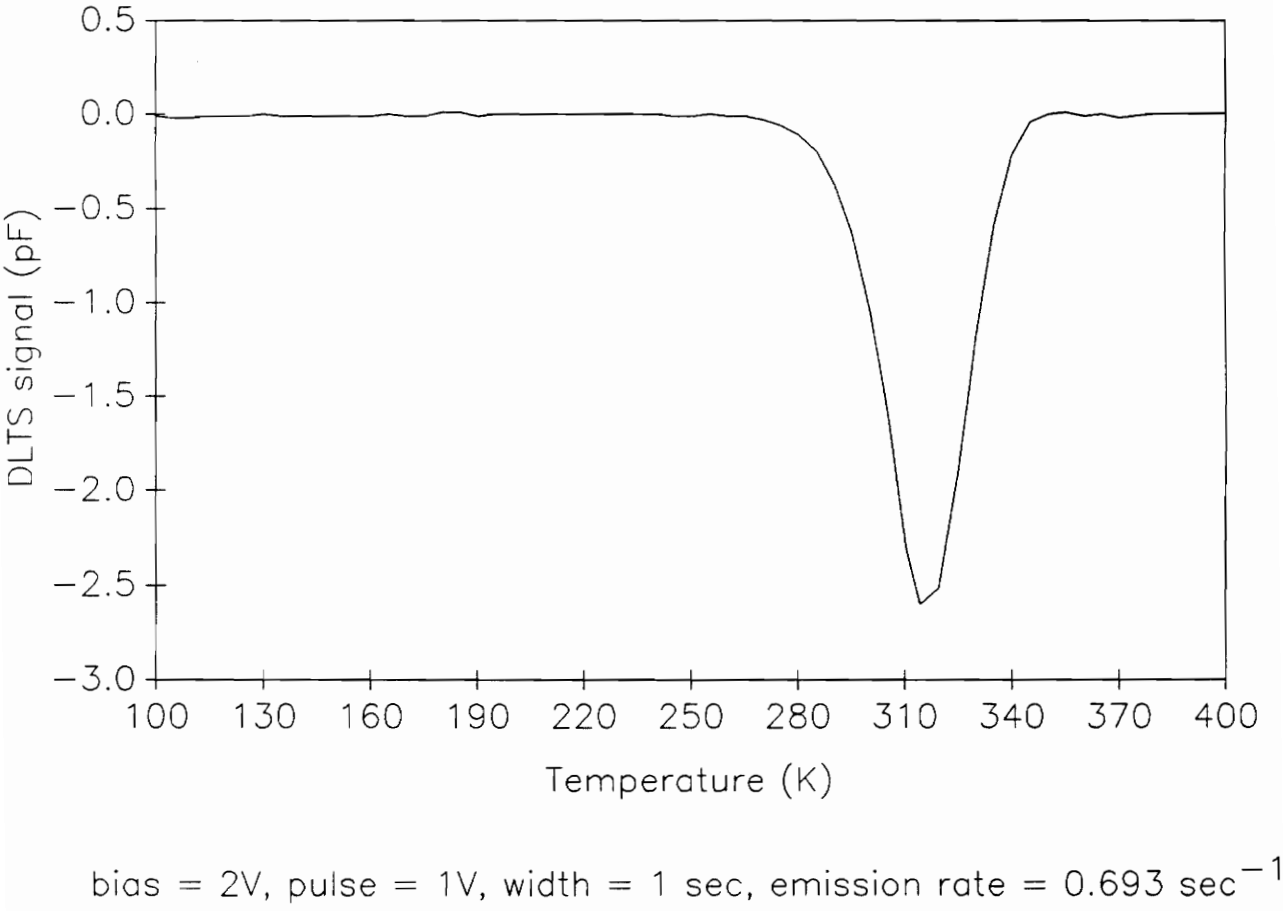


Fig. 5.41 DLTS spectrum of sample N2 (2 MeV, 1e13 cm^{-2} Si, and 900 °C RTA).

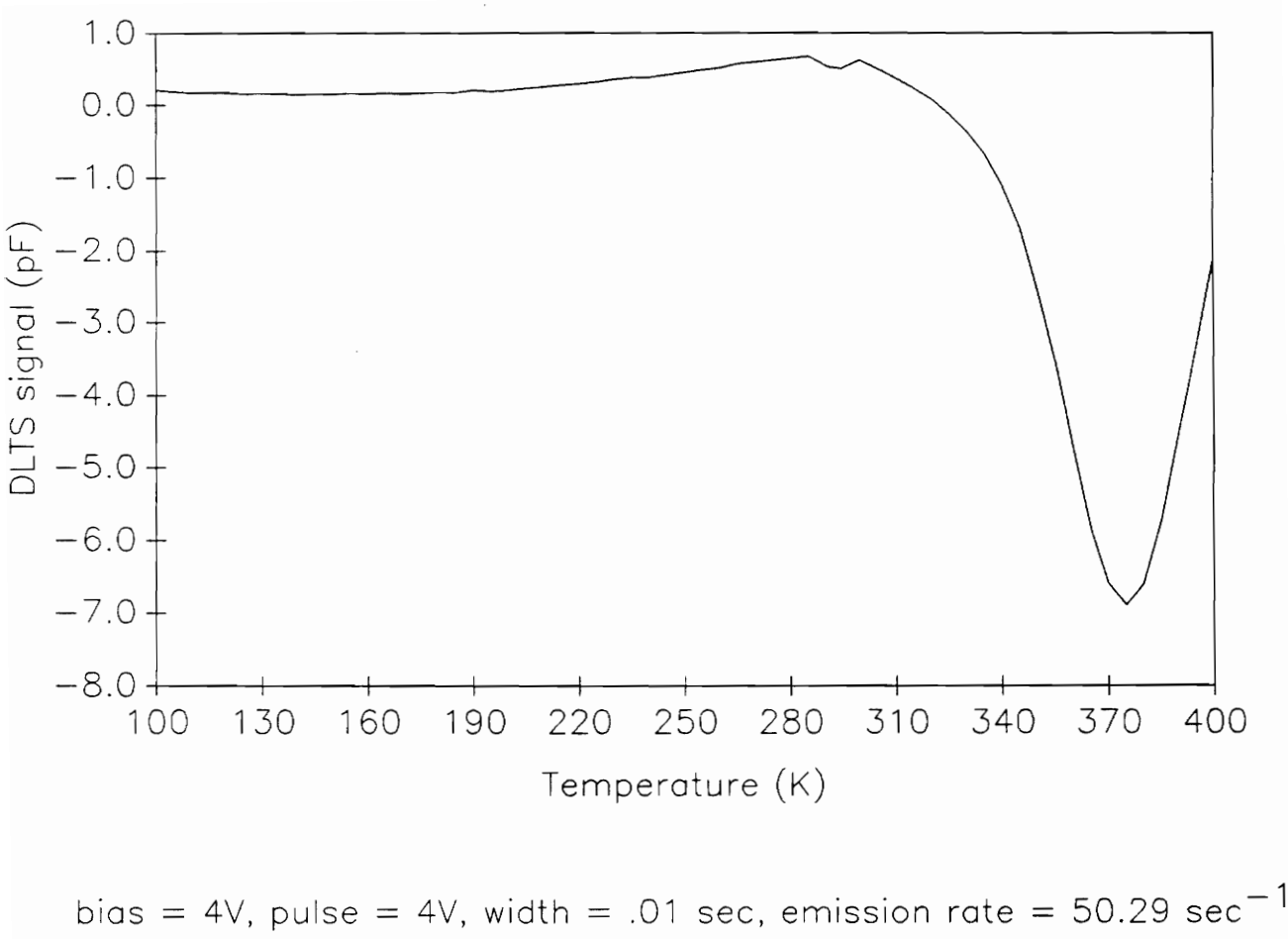


Fig. 5.42 DLTS spectrum of sample N3 (2 MeV, 1e13 cm^{-2} Si, and 950 °C RTA).

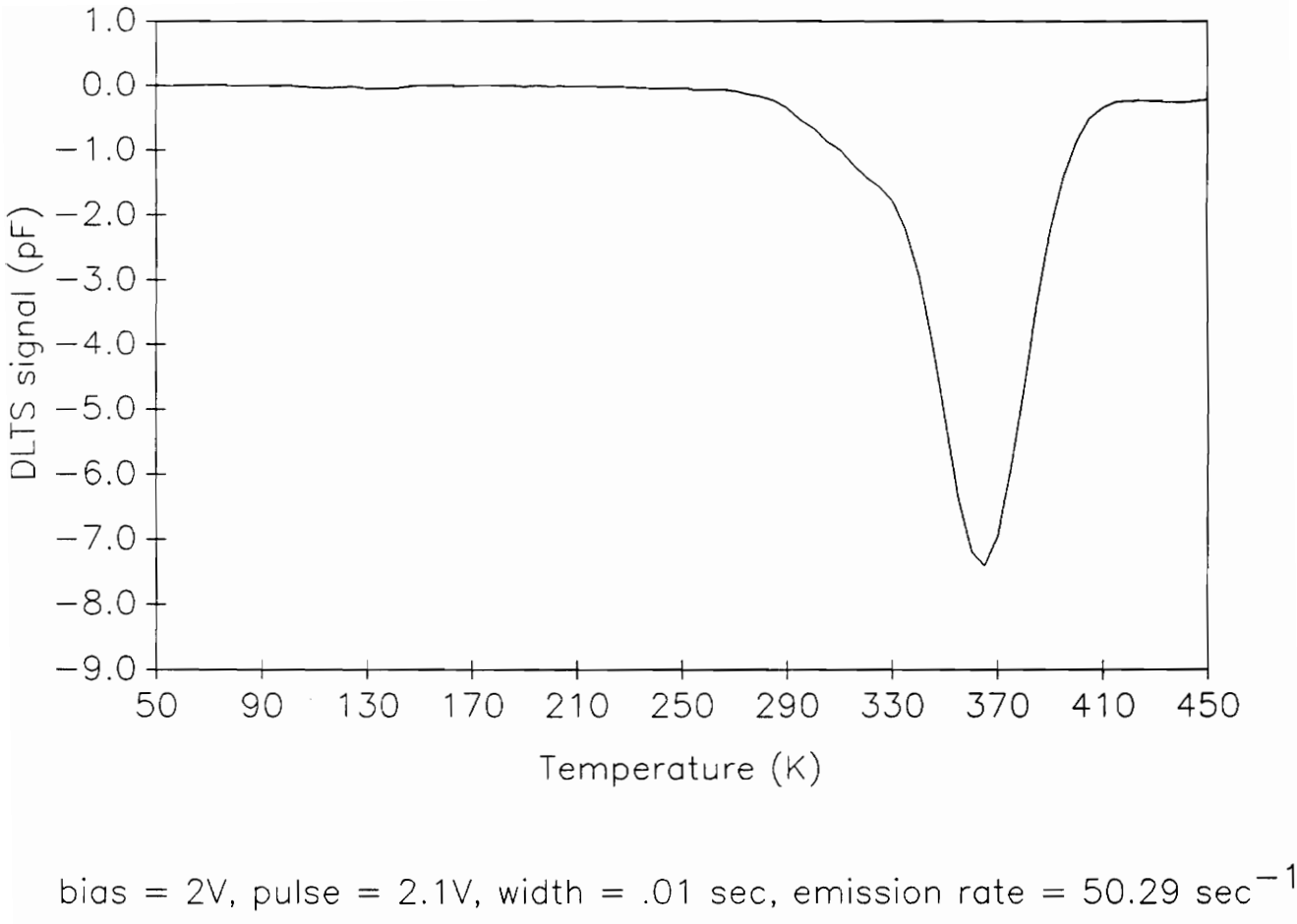


Fig. 5.43 DLTS spectrum of sample N5 (2 MeV, 1e13 cm^{-2} Si, and 1050 °C RTA).

parameters used during DLTS experiments are included in these figures.

There is a similarity between the DLTS spectra of 2 MeV samples. Figs. 5.40-5.43, all exhibit one, well defined trap peak due to EL2. The trap characteristics of 2 MeV samples (N1, N2, N3, and N5) are presented in Table 5.12, where σ refers to the electron capture cross section of the traps. There is no evidence of any level, other than EL2, at regions of different depths in the buried layers (refer to Table 5.12). The relative trap concentrations (N_T/N_D) in these samples are significantly high and varied between 0.1 - 0.29. A large N_T/N_D ratio results in a strong modification of emission transients. The only guarantee for an exponential transient from a charged defect center is when $N_T/N_D < 0.1$ [164]. Clearly this condition is violated in the 2 MeV samples investigated, and thus the trap densities estimated in Table 5.12 should be considered as approximate. There is no positive correlation between the RTA temperatures (850, 900, 950, and 1000 °C) and the relative trap densities. The relative trap density for the 950 °C annealed sample (N3) was found to be the lowest. Over all there is not much difference in the deep level qualities of the buried layers of N1, N2, N3, and N5. All contain a single trap level, belonging to the EL2 family, in high relative concentration.

The presence of a singular trap level is further confirmed by thermally scanned capacitance (C-T) measurements at a bias corresponding to the steady state reverse bias used during the DLTS measurements. During a thermal scan a step in the capacitance is observed when a trap goes from being completely filled to completely empty. This step in the capacitance is discernible if the trap concentration is comparable to the effective doping density. The energy of the trap level may be estimated from the capacitance step as :

$$E_C - E_T = \Delta E = 30.7kT_{step} \qquad (5.5)$$

where 30.7 has been linearly interpolated from Lang [187], and T_{step} is the temperature at the midpoint of capacitance transition. A typical C-T plot of sample N2 at 5V reverse bias is shown in Fig. 5.44. Using equation (5.5) , ΔE was found to be 0.76 eV and is very close to the value obtained by DLTS. The step in Fig. 5.44 is due to emission from EL2 center. C-T measurements performed

Table 5.12. Characteristics of deep levels in the 2 MeV samples.

sample#	depth (μm)	ΔE (eV)	N_T/N_D	σ (cm^2)
N1	0.83	0.80	.205	$3.2x10^{-13}$
N2	1.33	0.77	.116	$7.1x10^{-14}$
	1.36	0.76	.170	$7.4x10^{-14}$
	1.37	0.77	.243	$6.9x10^{-14}$
	1.40	0.77	.287	$5.0x10^{-14}$
	1.42	0.77	.282	$5.1x10^{-14}$
N3	1.60	0.75	.092	$3.3x10^{-14}$
	1.62	0.75	.098	$3.3x10^{-14}$
	1.64	0.77	.151	$5.2x10^{-14}$
	1.67	0.77	.172	$5.2x10^{-14}$
	1.69	0.77	.158	$5.2x10^{-14}$
N5	1.69	0.76	.210	$7.7x10^{-14}$
	2.57	0.77	.084	$3.3x10^{-14}$

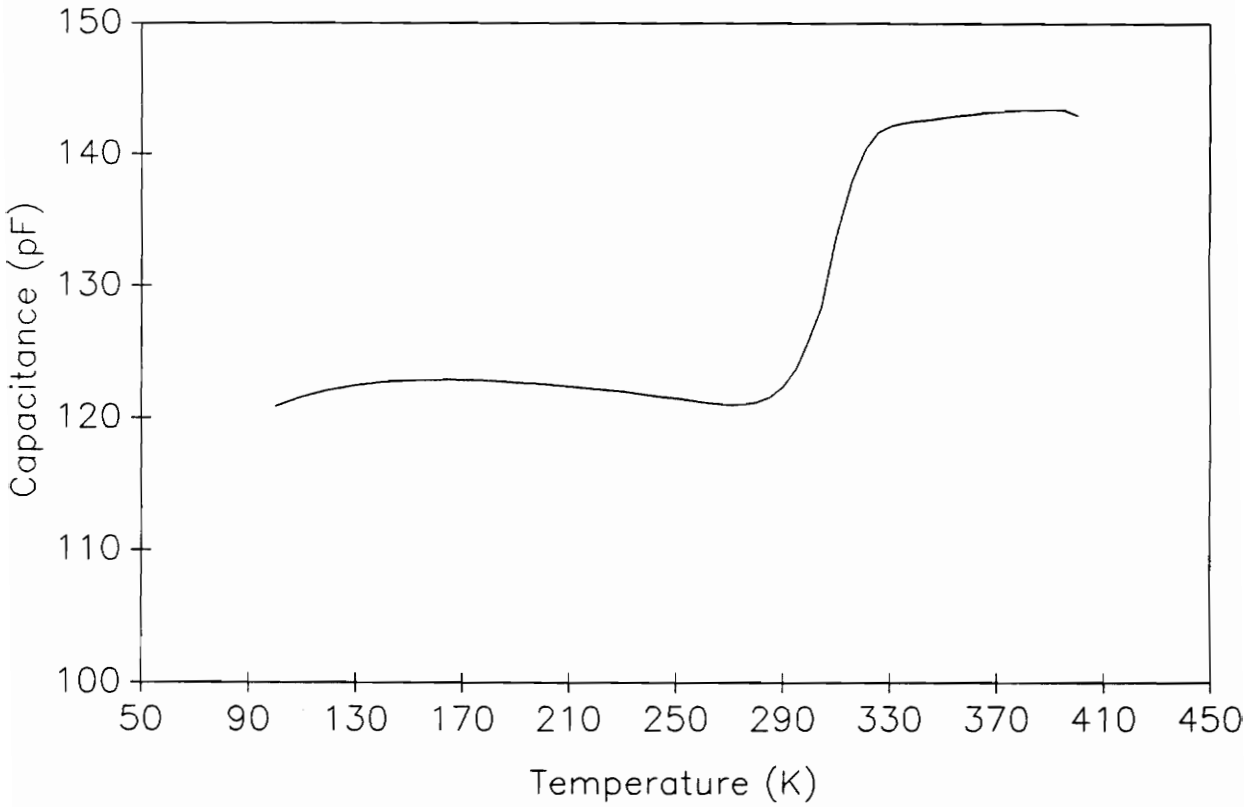


Fig. 5.44 **Temperature dependence of capacitance of sample N2 at reverse bias of 5V** (frequency = 1MHz).

on samples N1, N3, and N5 yielded similar results.

A DLTS spectrum of sample N5, taken at a deeper region in the buried layer (2.57 μm from the surface), is presented in Fig. 5.45. In this case, 2.2 μm of GaAs was chemically etched away from the surface. The spectrum, like before, exhibits a single trap level due to EL2. The only difference in the spectra of Figs. 5.43 and 5.45 is the relative trap densities, which are considerably reduced at a deeper region (near the implant tail) of the buried layer. The N_T/N_D ratio decreased from 0.210 to 0.084 with probe depth changing from 1.69 μm to 2.57 μm from the sample surface (refer to Table 5.12).

Representative DLTS spectra of 6 MeV Si-implanted and RTA GaAs (i.e. N6, N7, and N8) are shown in Figs. 5.46, 5.47, and 5.48, respectively. The trap parameters for these samples are provided in Table 5.13. Like the 2 MeV samples, the DLTS spectra of 6 MeV samples are dominated by EL2 alone. This holds even at deeper probe depths (refer to Table 5.13). The trap activation energy for 6 MeV samples varied between 0.76 - 0.81 eV and their signature closely resembles one of the member of EL2 family. Interestingly, the relative trap densities estimated by DLTS are also high in 6 MeV Si-implanted and RTA-annealed GaAs . For reasons described earlier, the values of N_T/N_D in Table 5.13 are rough estimates. The relative densities of EL2 in samples N6, N7, and N8 varied between 0.09-0.43, and appeared to be higher than those obtained in 2 MeV samples. Samples N6 and N7 had the same processing conditions except N6 had implant dose lower than that used for N7. It is evident that in the range of implant dose investigated, the relative trap density is somewhat higher for samples with higher ion dose.

A typical C-T characteristic of sample N8 at a reverse bias of 5V is shown in Fig. 5.49. The step in the capacitance transition once again confirms the presence of EL2 in high concentration. The samples N6 and N7 showed similar C-T behavior.

To investigate the tail of the implant profile, DLTS measurements were taken for sample N6 at depths of 4.87 and 5.05 μm from the surface. This was achieved by chemically etching away a 4.75

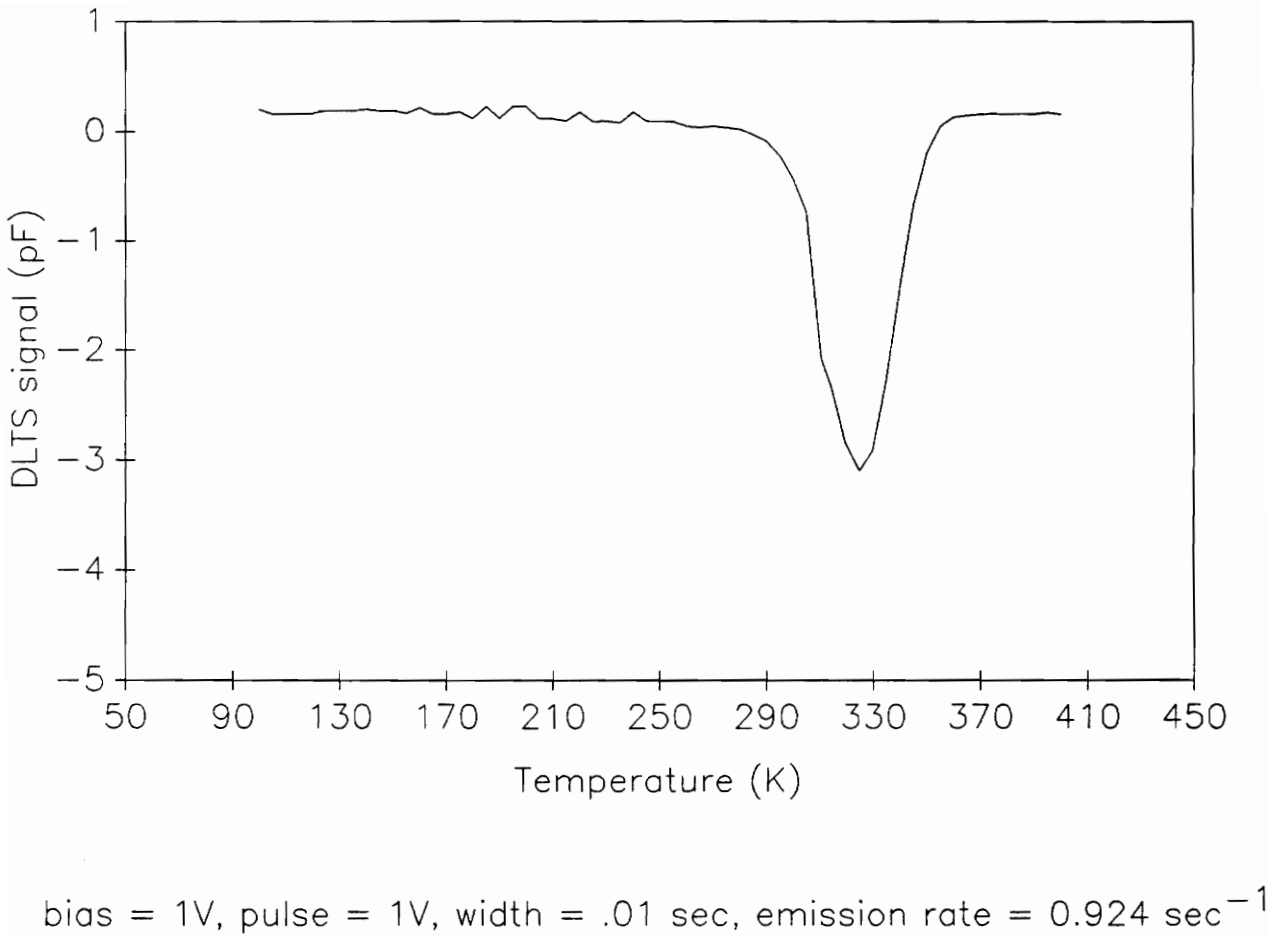


Fig. 5.45 DLTS spectrum of sample N5 near the tail of the implant profile (2 MeV, 1x10^{13} cm^{-2} Si, and 1050 °C RTA).

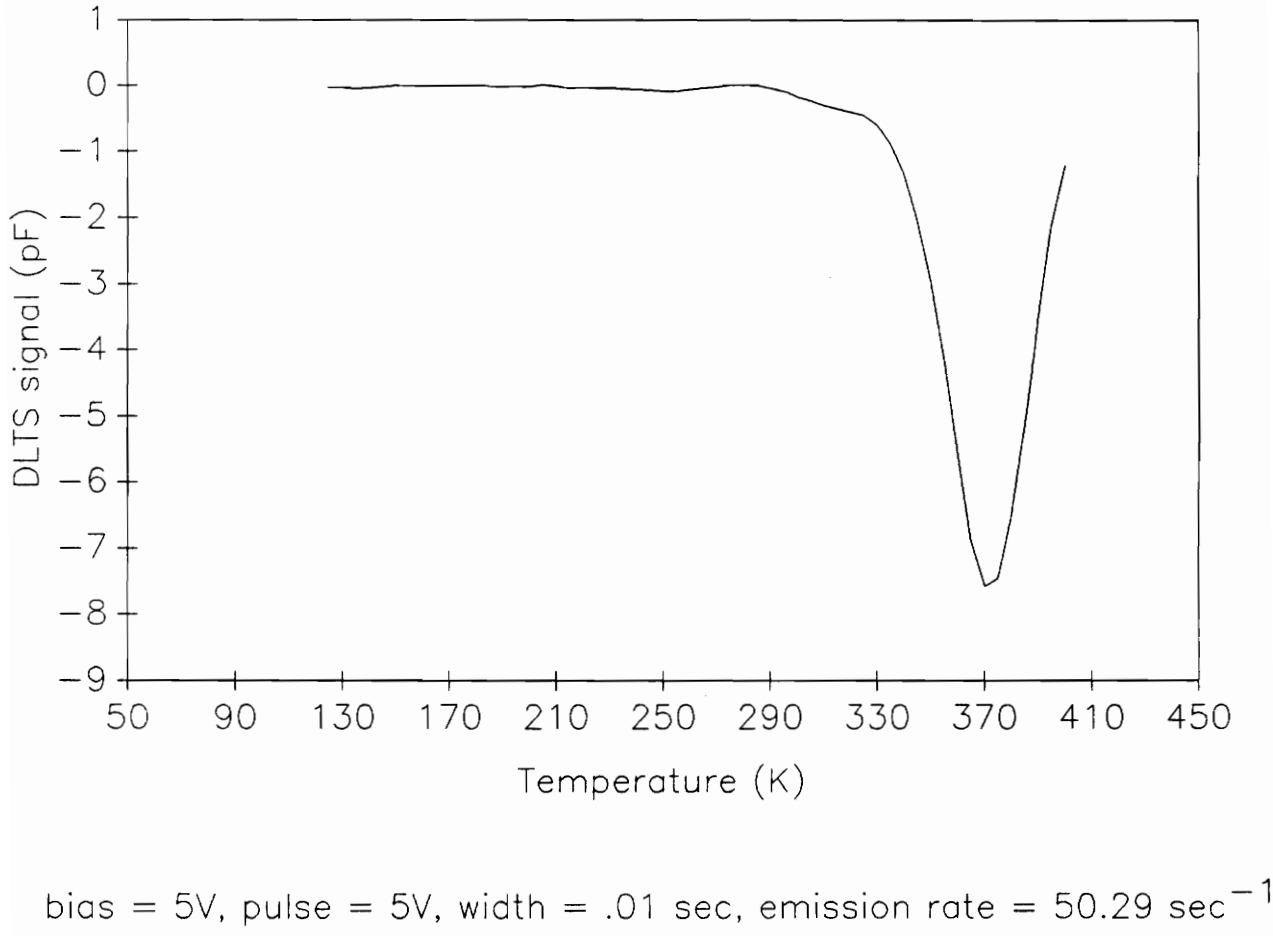


Fig. 5.46 DLTS spectrum of sample N6 (6 MeV, 5e12 cm^{-2} Si, and 1000 °C RTA).

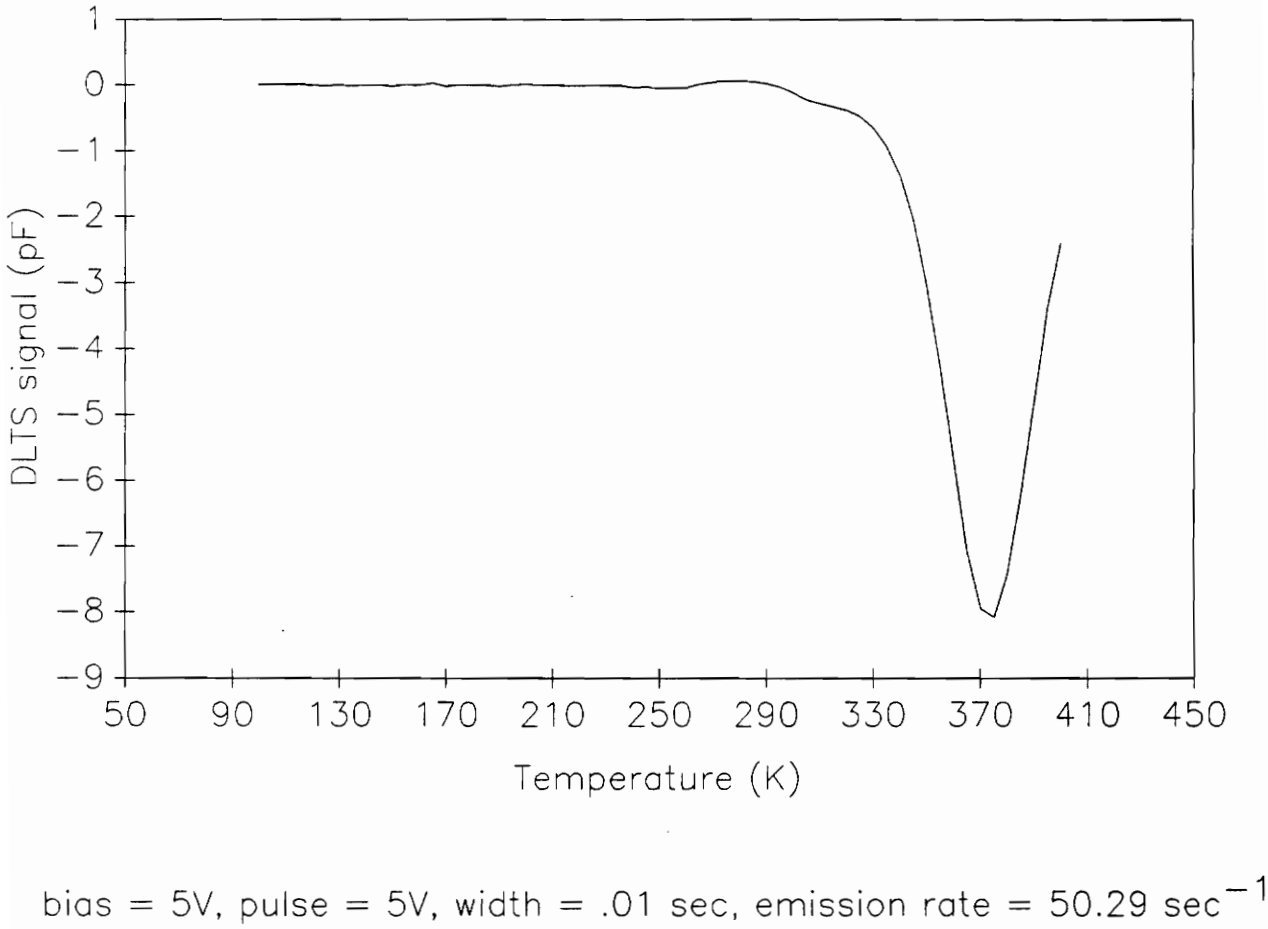


Fig. 5.47 DLTS spectrum of sample N7 (6 MeV, 1e13 cm^{-2} Si, and 1000 °C RTA).

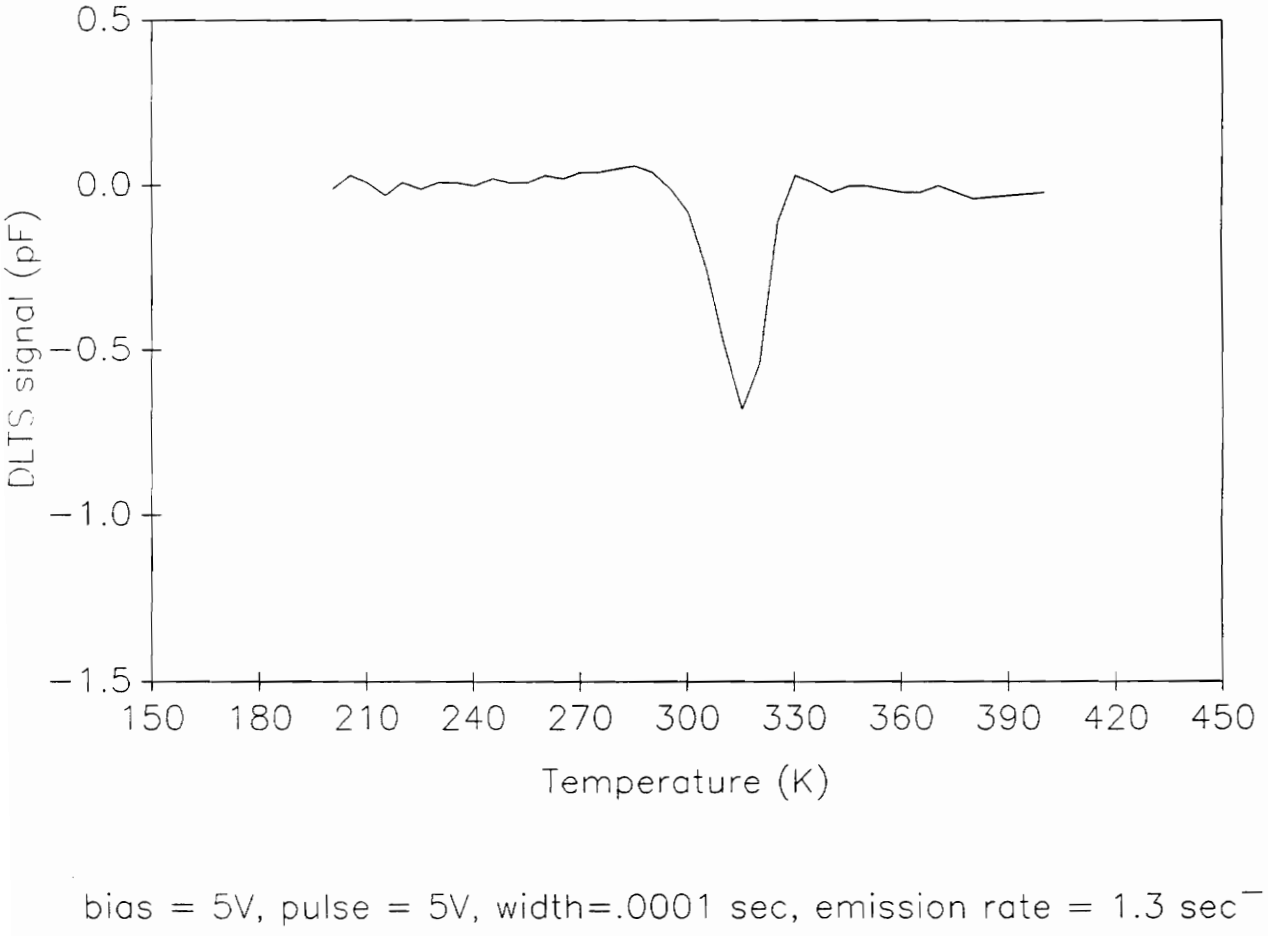


Fig. 5.48 DLTS spectrum of sample N8 (6 MeV, 1e14 cm^{-2} Si, and 950 °C RTA).

Table 5.13. Characteristics of deep levels in 6 MeV Si-implanted and 10/11 MeV Si/S co-implanted GaAs samples.

sample#	depth (μm)	ΔE (eV)	N_T/N_D	σ (cm^{-2})
N0	0.13	0.81	.091	$1.7x10^{-13}$
N6	2.65	0.76	.322	$4.0x10^{-14}$
	2.70	0.76	.374	$4.3x10^{-14}$
	2.76	0.76	.351	$4.3x10^{-14}$
	2.99	0.76	.328	$4.3x10^{-14}$
	4.87	0.79	.086	$6.9x10^{-14}$
	5.05	0.79	.086	$6.9x10^{-14}$
N7	2.46	0.77	.381	$2.5x10^{-14}$
	2.51	0.77	.387	$2.5x10^{-14}$
	2.53	0.77	.433	$2.5x10^{-14}$
N8	1.05	0.81	.143	$8.9x10^{-13}$

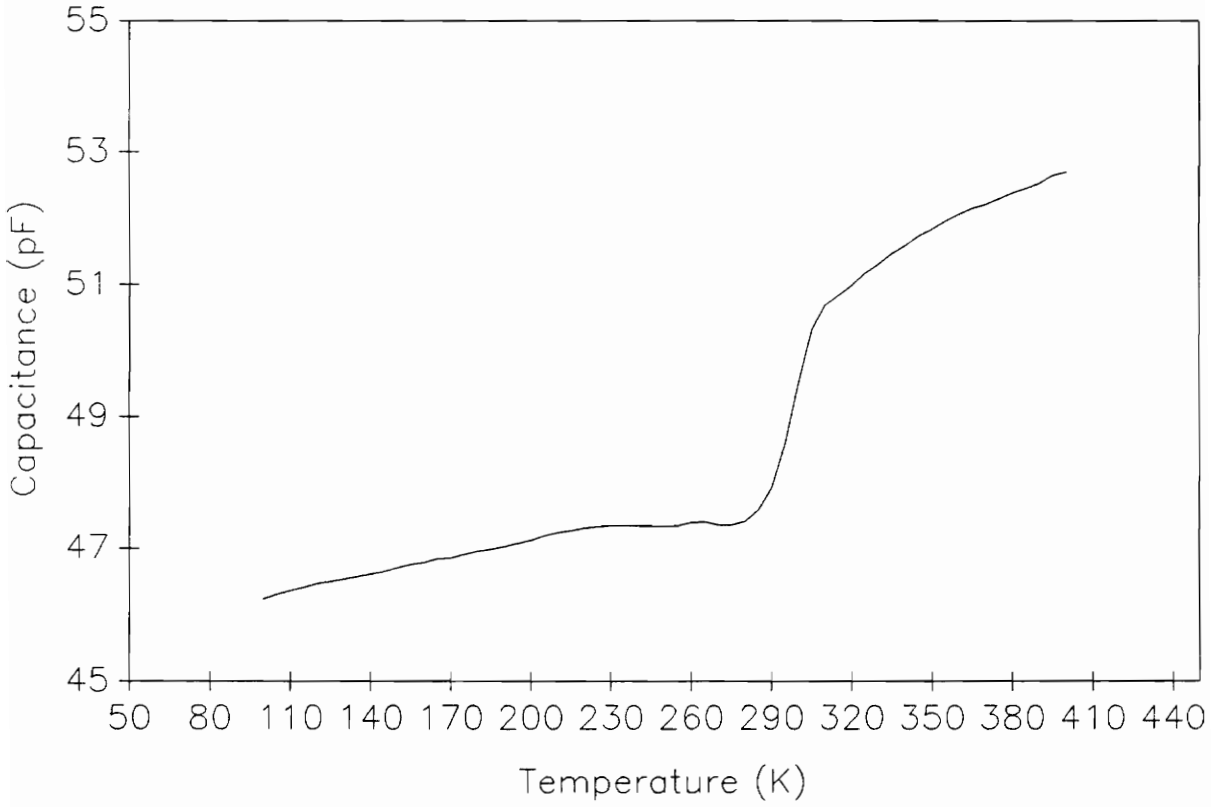


Fig. 5.49 Temperature dependence of capacitance of sample N8 at a reverse bias of 5V (frequency = 1MHz).

μm thick GaAs layer from the top. The DLTS spectrum of N6 corresponding to a depth of 4.87 μm is shown in Fig. 5.50. No additional trap levels, other than EL2, are revealed. Once again the striking difference between this spectrum and the one taken at a shallower region of the buried layer (Fig. 5.46) is the relative trap concentration, which reduced from 0.322 at a depth of 2.65 μm to 0.086 at 4.87 μm. Fig. 5.51 shows the variation of relative EL2 density with depth in the buried layer of samples N5 and N6.

As a continuation of this study, sample N0, with a dual implantation of 11 MeV S and 10 MeV Si, was investigated for traps using DLTS. A typical DLTS spectrum of N0 at 2V reverse bias is presented in Fig. 5.52. The spectral features remain unaltered when compared with the spectra of 2 and 6 MeV Si-implanted GaAs. EL2 continues to be the sole trap level, and other levels are either absent or in a concentrations that are below the detection limit of the measurement. It is not possible to assign a depth parameter to the EL2 level in N0 since the as-received sample had chemical etching and FET type surface implantation subsequent to MeV implantation and annealing; the details of which are not known precisely. The intention of including the DLTS results of N0 is to merely elucidate if any other trap levels, other than EL2, appear because of change in MeV implantation energy. The trap parameters for N0 are also provided in Table 5.13.

The key result of DLTS measurements is the presence of a single trap level, EL2, in MeV Si-implanted and RTA annealed GaAs in the investigated ranges of fluence and annealing temperatures. There are some notable dissimilarities between the DLTS results of keV and MeV Si- implanted and RTA GaAs. 50 keV Si-implanted and RTA-activated GaAs contained multiple trap levels (refer to Fig. 5.6 and Table 5.1). The level EL4 (0.52 eV), which was identified as an implantation- induced level in 50 keV Si-implanted and RTA GaAs, is surprisingly missing in MeV implanted GaAs samples. The level EL4 was also detected in 150 keV Si-implanted and furnace annealed GaAs (see Fig. 5.29). The contrasting DLTS results of MeV and keV Si-implanted GaAs suggest the possibility of a different nature of damage and annealing mechanisms.

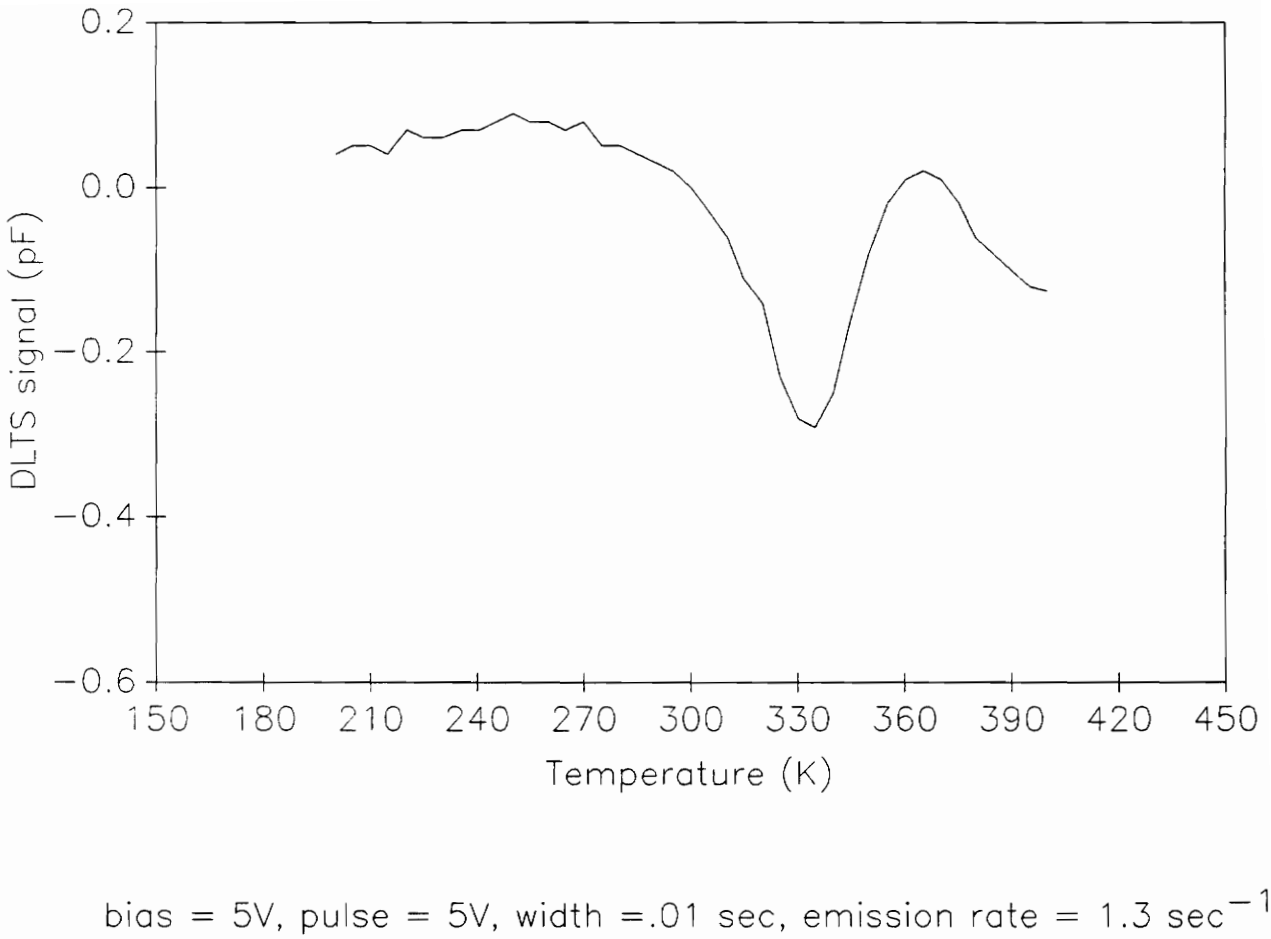


Fig. 5.50 DLTS spectrum of sample N6 near the tail of the implant profile (6 MeV, $5x10^{12}$ cm^{-2} Si, and 1000 °C RTA).

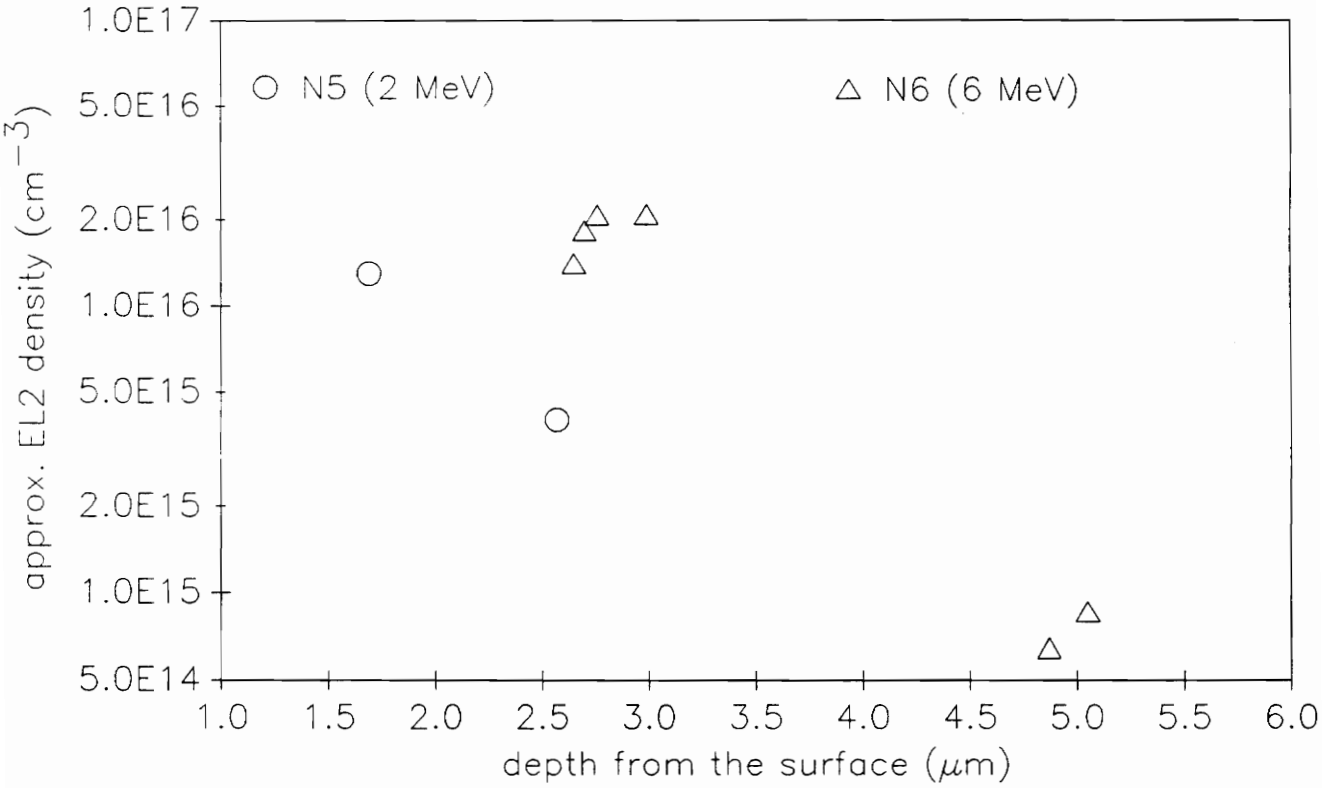


Fig. 5.51 **Variation of relative EL2 concentration at different depths in buried layers of samples N5** (2 MeV, $1x10^{13}$ cm^{-2} Si, and 1050 °C RTA) and **N6** (6 MeV, $5x10^{12}$ cm^{-2} Si, and 1000 °C RTA).

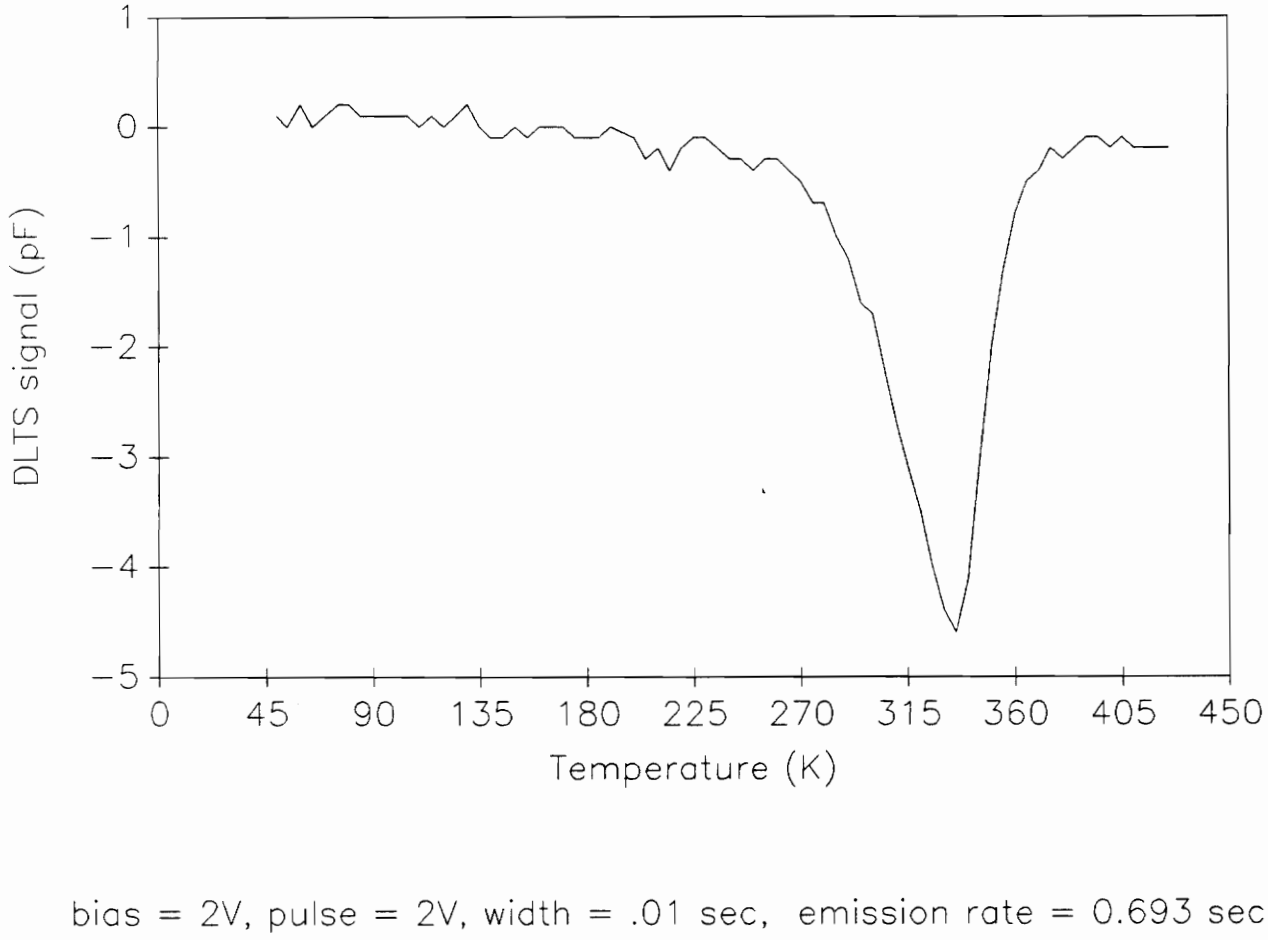


Fig. 5.52 DLTS spectrum of sample N0 (11 MeV S/ 10 MeV Si co-implanted at 1.5×10^{14} cm^{-2} ion dose each and 1000 °C RTA).

The absence of trap levels in MeV implanted GaAs that were otherwise observed after keV implantation possibly indicates the occurrence of a significant in-situ self-annealing of MeV implantation damage during room temperature implantation. Although the detailed nature of MeV implantation induced defects is not fully established, an intense dynamic annealing during MeV Si implantation of GaAs has been reported by Chen *et al.* [128]. They have examined lattice disorder due to 1-3 MeV Si implantation in GaAs using RBS and TEM techniques. The RBS channeling spectra of virgin and room temperature Si-implanted GaAs with different MeV energies are shown in Fig. 5.53a. The key findings of their investigation are as follows:

(i) Even at a dose of 10^{16} cm^{-2} of 1-3 MeV Si, only a small amount of lattice disorder remains. Lattice disorder saturates roughly at 10^{15} cm^{-2} dose i.e. a steady state is reached between the rate of lattice disorder and in-situ annealing.

(ii) Without adequate cooling of the substrate, it is difficult to amorphize GaAs by MeV Si implantation. This is due to in-situ self-annealing during implantation, where mobility of point defects and their long range migration play an important role in determining the annealing behavior of defects. During this in-situ annealing, perfect and partial dislocation loops are formed, as identified in high resolution TEM [129].

(iii) Annealing at 900 °C for 10 sec restores the crystallinity of the near-surface region of the implanted GaAs. Deeper down, a band of residual dislocation remains as is evidenced by a steep rise in back scattering yield [see Fig. 5.53b].

It has been reported by Chen *et al.* [129] that in a 1 MeV Si-implanted GaAs, the maximum of the buried residual band defect correlates with the peak of the Si implant profile. The nature of residual defects after MeV implantation is different in the near-surface and in the buried layer. In the near-surface region, the defect density is low. Most of the defects are discrete point-defect complexes and small interstitial dislocation loops, both of which are easily annealed out. Away from

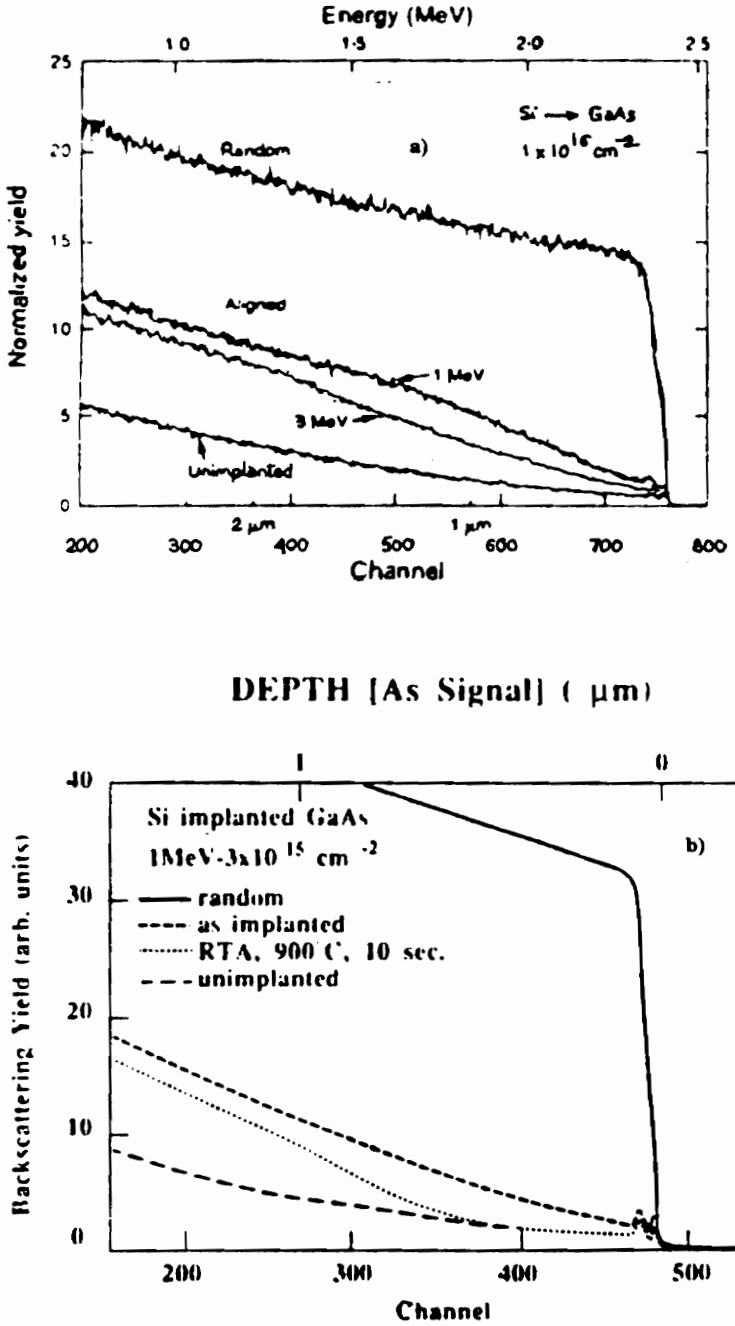


Fig. 5.53 RBS channeling spectra of GaAs after a) MeV Si implantation and b) 1 MeV Si implantation and 900 °C RTA (taken from ref. [128]).

the surface, in the buried layer, there is a high concentration of loops. Upon annealing they combine and become stable, resulting in a buried residual defect band of loops, whose density decreases and size increases with increasing annealing temperature.

On the basis of above discussions, there appears to be a correlation between the electrical DLTS and the reported structural findings (RBS, XTEM) on MeV Si-implanted GaAs. The EL2 level observed in samples 2 MeV Si, 6 MeV Si, and 10/11 MeV Si/S implanted GaAs is a result of the combination of EL2 existing in the original substrate and those induced by implantation and RTA. It is known that ion implantation in GaAs creates EL2 centers [49,177]. This is again confirmed in samples N5 and N6 (refer to Fig. 5.51), where the EL2 concentration is reduced approximately by an order of magnitude from the region near the buried layer peak to depths near the tail of the implant profile. It is therefore proposed that the EL2 in the buried layer of MeV Si-implanted and RTA GaAs are mostly due to secondary defects generated by ion implantation which during annealing segregate and agglomerate into a high density buried band of dislocations. The high relative trap densities in the MeV implanted buried layer agree well with the presence of high density dislocations in the region. It is also proposed that the observed broadening of the carrier concentration profiles in N4 and N9 as compared to TRIMs prediction is likely to be due to radiation enhanced diffusion caused by the dynamic annealing process during implantation.

In conclusion, the deep level characteristics of MeV Si-implanted and RTA GaAs are significantly different from those of an identically processed keV Si-implanted GaAs. The MeV Si-implanted samples contain one dominant electron trap at 0.75-0.80 eV in high concentration and its origin can be correlated with dislocation bands in the active layer. EL2 is mainly localized in the buried layer of MeV Si-implanted GaAs and its concentration reduces drastically towards the tail of the implant profile.

5.3 Electrical Activation and Annealing

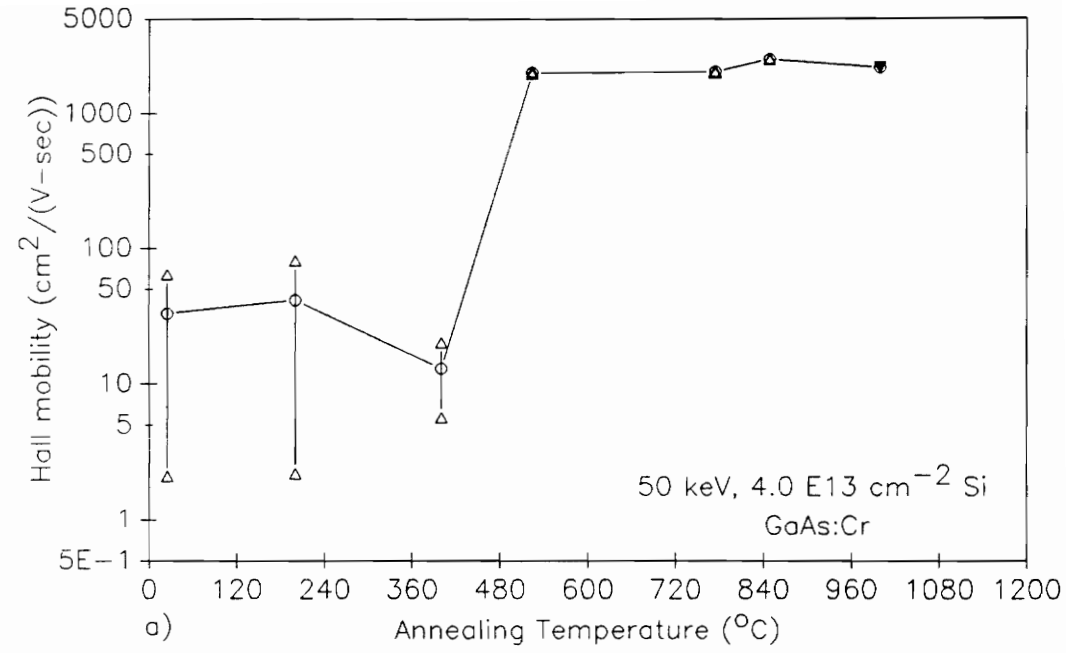
Electrical activation of ion implanted GaAs layers depends critically on the annealing conditions. Important annealing parameters are the annealing type (furnace or RTA), temperature, duration, and annealing ambient. The effects of low and high temperature isochronal furnace annealing (20 minutes) on the electrical characteristics of 50 keV Si (at 4 x 10^{13} cm^{-2} dose) implanted (100) GaAs:Cr will be addressed in detail in this section. The annealing parameters used in this study were described under category F in Chapter 4. A proximity annealing method [188] was employed, where the GaAs samples were sandwiched between GaAs wafers on top and bottom. The annealing was performed in a tube furnace under an atmosphere of forming gas (95% N_2 + 5% H_2). Wherever appropriate, correlation between the structural recovery and electrical activation of Si-implanted GaAs will be presented.

5.3.1 Transport Characteristics

The effect of annealing on Hall-mobility is shown in Fig. 5.54a. The error bars shown on the curve are the limits of accuracy estimated at different anneal temperatures. The uncertainties in the mobility values of the as-implanted and low temperature annealed (< 525 °C) samples are high because of their low values. These samples have structural disorder, comprised of interstitial, vacancies, dislocations and their complexes, that are responsible for reduced mobility. The mobility takes a sharp rise after annealing at 525°C. This is consistent with the Raman measurements, shown in Fig. 5.55, on these samples [194]. The Raman spectra at different annealing temperatures, suggest that most of the ion implantation damage is removed and structural recovery is achieved by 525 °C annealing.

In a semiconductor, dc conductivity σ_0 can be expressed as

$$\sigma_0 = q(n\mu_n + p\mu_p) + \sigma_{hopping} \qquad (5.6)$$



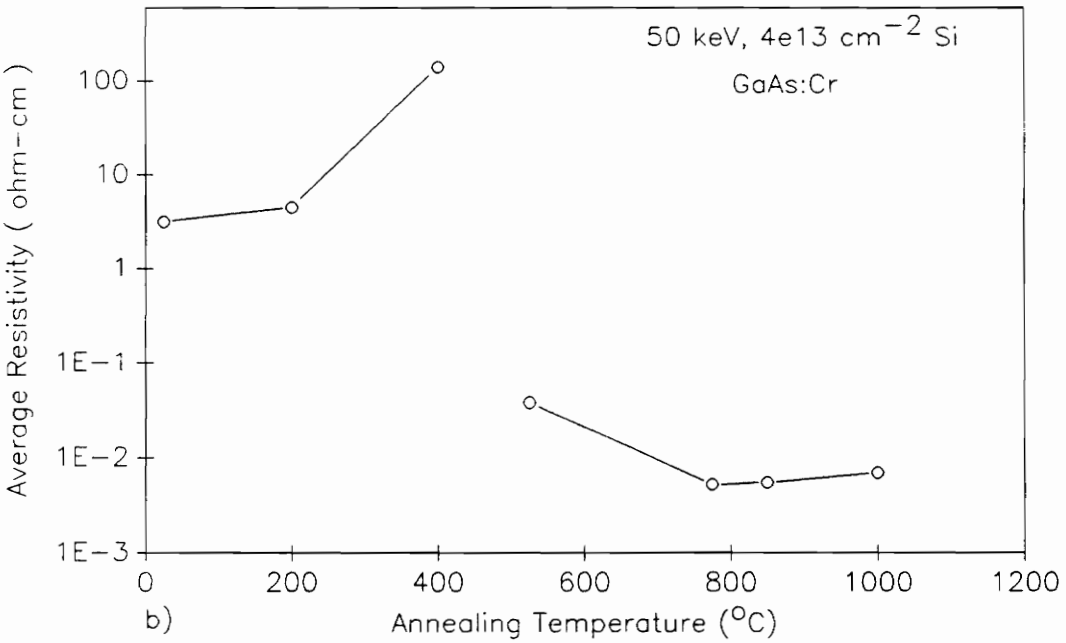


Fig. 5.54 Effect of proximity annealing temperature on: a) Hall mobility and b) sheet resistivity of 50 keV, $4x10^{13}$ cm^{-2} Si-implanted GaAs:Cr.

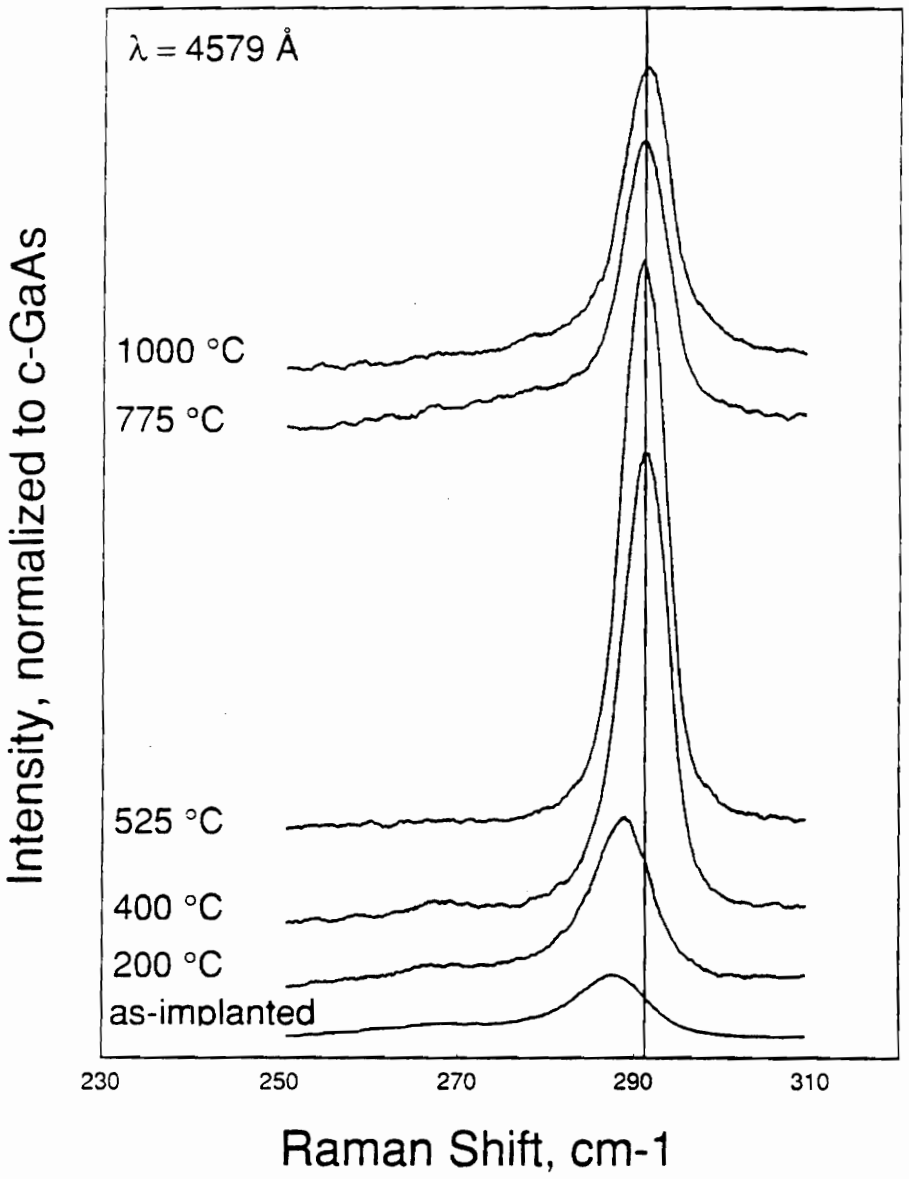


Fig. 5.55 Raman spectra of 50 keV Si-implanted GaAs:Cr after various proximity annealing temperatures [194].

where n and p are electron and hole concentrations, μ_n and μ_p are the electron and hole mobility, respectively and $\sigma_{hopping}$ is an additional conductivity term due to hopping conduction. The dc conduction mechanism in as-implanted SI GaAs is based on hopping and is similar to that in disordered or amorphous semiconductors, as proposed by Mott *et al.* [191]. The dependence of resistivity on temperature for an as-implanted sample is shown in Fig. 5.56a. In this case, the process of thermally activated hopping of carriers is dominant. At temperatures above 185 K, the resistivity is governed by phonon-assisted hopping and follows the relation:

$$\rho = \rho_0 \exp\left[\frac{W}{kT}\right] \tag{5.7}$$

where W is the hopping energy and ρ_0 is the resistivity extrapolated to infinite temperature. The observed value of W in the as-implanted case is 0.091 eV. Kato *et al.* measured an energy of 0.087 eV for a completely disordered GaAs:Cr material [192].

For temperatures below 185 K, there are fewer phonons, and the resistivity values of the as-implanted sample better follow the relation

$$\rho = C \exp\left[\frac{B}{T^{1/4}}\right] \tag{5.8}$$

where C is a constant and is a function of hopping energy and the average distance between the localized states. In this low temperature range, the mechanism of carrier transport is by variable-range hopping. After annealing at 525 °C, there is a weaker dependence of resistivity on temperature (Fig. 5.56b). The temperature effect became progressively weaker in samples annealed at higher temperatures.

The change in resistivity with annealing is shown in Fig. 5.54b. A reasonably good ohmic contact could be obtained using pressure probes (Pt-Rh) on samples as-implanted or those implanted and annealed up to 400 °C. The resistivity initially rises up to around 400 °C annealing. This rise is attributed to anneal induced reduction in defect states which would otherwise participate in hopping

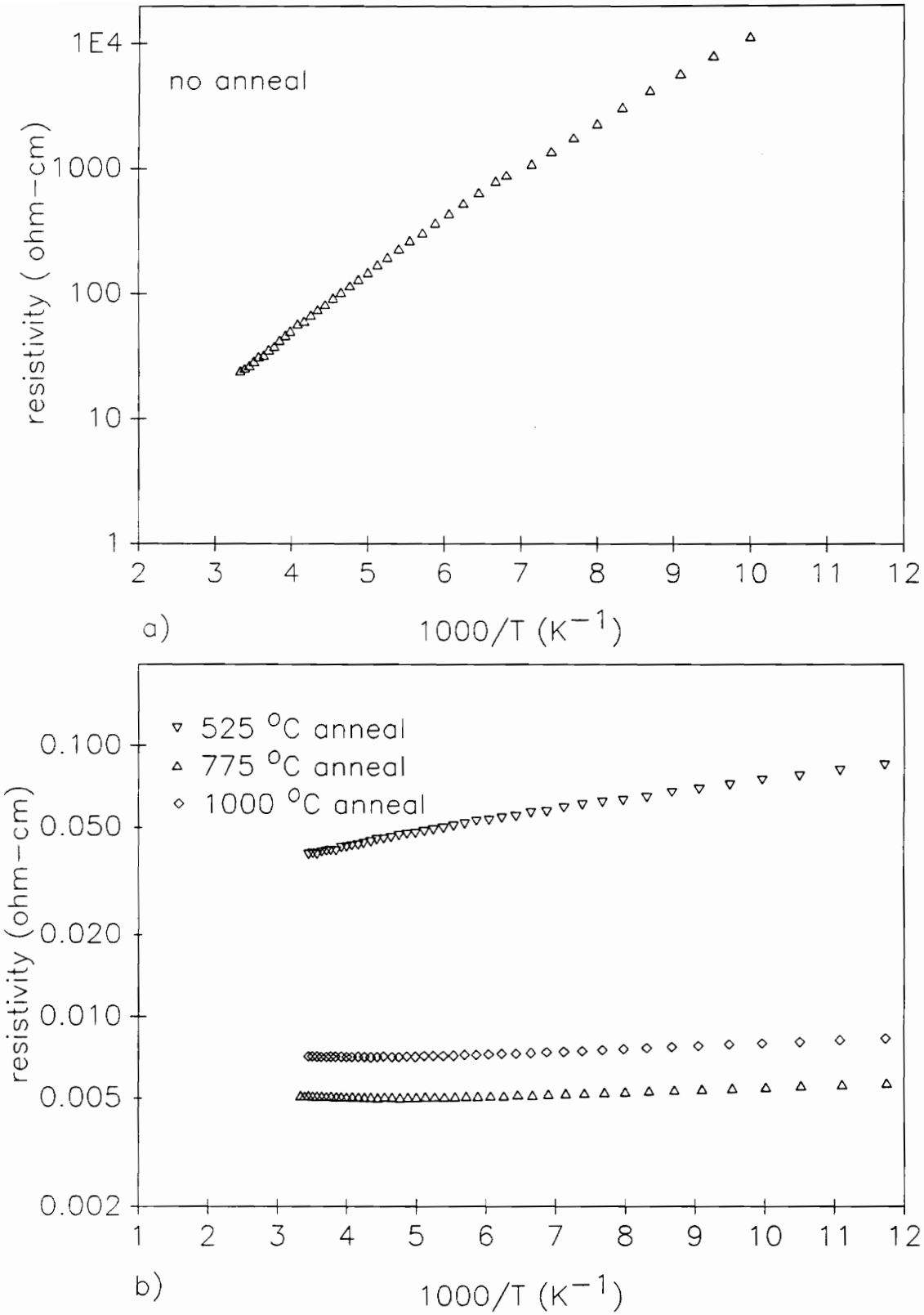


Fig. 5.56 Temperature dependence of resistivity of 50 keV Si-implanted GaAs:Cr after various annealing treatments : a) no anneal and b) annealed at indicated temperatures.

conduction. The low-temperature annealing up to 400 °C causes lattice restoration to the original state and is effective in annealing out the hopping states. The effect of low-temperature annealing on the resistivity of an ion-implanted GaAs sample can be expressed as [192]

$$\log(\frac{\rho_T}{\rho_{RT}}) \propto t \exp[\frac{E_g}{kT}]$$

where ρ_T is the resistivity after annealing at temperature T, ρ_{RT} is the as-implanted resistivity, t is the annealing time, and E_a is the activation energy for recrystallization of disordered GaAs, which in this case was found to be 0.38 eV. This value of E_a is comparable to 0.35 eV, reported by Kato *et al.* for N^+ and S^+ implanted GaAs [192].

At 525 °C annealing temperature, the drop in resistivity is significant, beyond which the change is less rapid, eventually saturating at higher annealing temperatures. The step-like behavior of mobility and resistivity at 525°C indicates the commencement of a different type of conduction process, and that the hopping mechanism become nearly insignificant. Such changes in conduction mechanisms are conceivable once structural recrystallization is nearly achieved.

Dopant activation begins to occur at around 525 °C. The maximum activation is achieved between 775 and 850 °C. A small decline in electrical activation was found for anneals between 850 and 1000 °C. This decline may be due to amphoteric Si occupying As sites at such annealing temperatures, thereby increasing the compensation ratio. The transport properties obtained from van der Pauw measurements for samples annealed at different temperatures are listed in Table 5.14. The temperature dependence of Hall mobility and carrier concentration of samples with three different annealing temperatures are shown in Figs. 5.57a and 5.57b, respectively. The mobility and Hall carrier concentration behave as expected against temperature. The sample with 525 °C anneal has a more pronounced impurity scattering regime, controlling Hall mobility at low temperatures, than the 775 and 1000 °C annealed samples (refer Fig. 5.57a). Also, the carrier concentration of the 525 °C sample is somewhat temperature dependent, but the temperature effect on carrier density of the 775 and

Table 5.14. Average transport parameters of 50 keV Si-implanted and proximity annealed GaAs:Cr.

annealing temperature (°C)	resistivity (ohm-cm)	mobility $cm^2/V\text{-}sec$	carrier density (cm^{-3})
as implanted	21.21	33 ± 31	?
200	4.49	42 ± 39	?
400	140.36	13 ± 7	?
525	0.0384	1997 ± 46	8.1×10^{16}
775	0.0052	2017 ± 26	5.9×10^{17}
850	0.0055	2523 ± 22	4.5×10^{17}
1000	0.0070	2163 ± 20	4.1×10^{17}

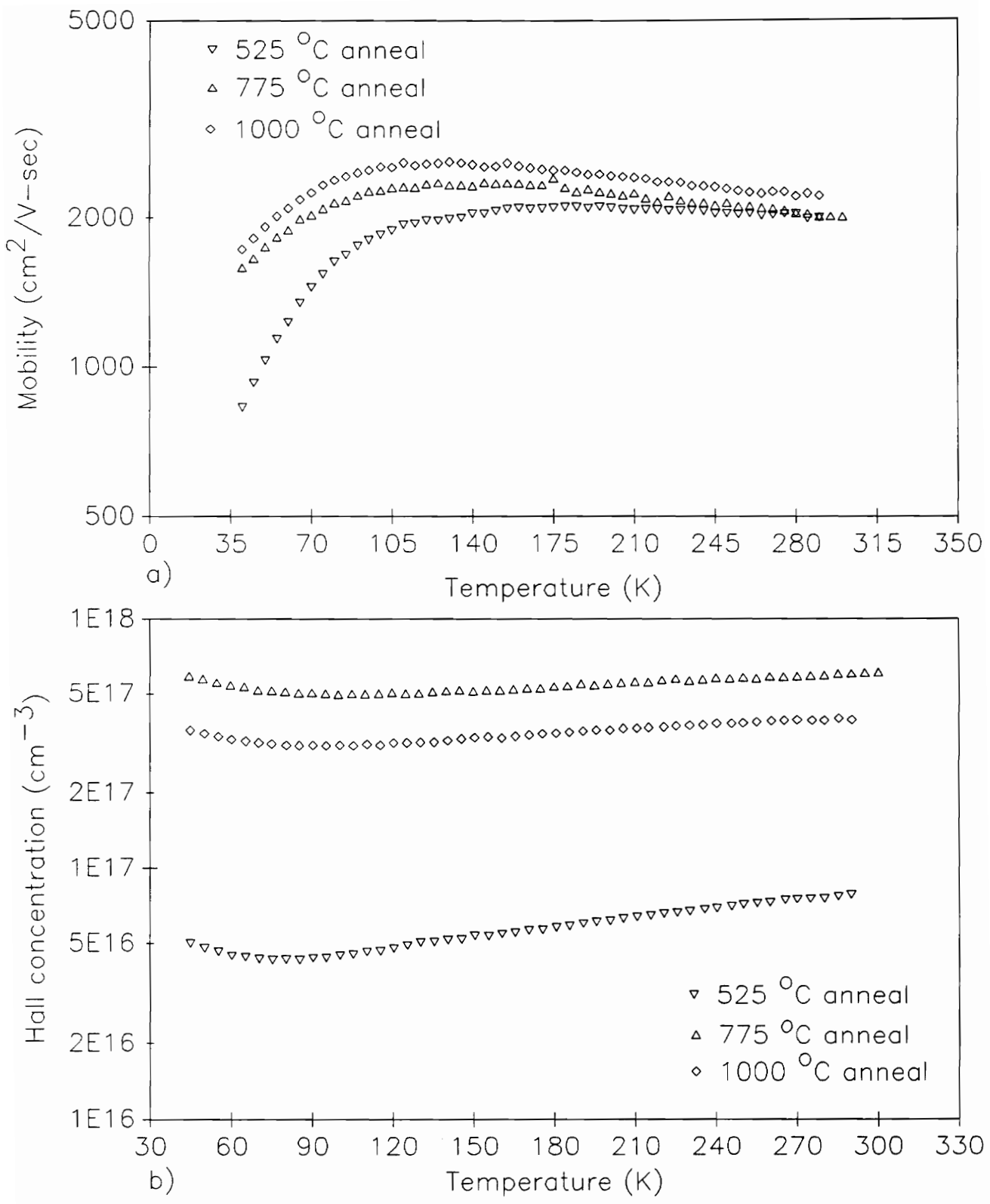


Fig. 5.57 Temperature dependence of a) Hall mobility and b) carrier concentration of 50 keV Si-implanted and proximity annealed GaAs:Cr at indicated temperatures.

1000 °C annealed samples is almost insignificant. From the temperature dependence of carrier activation, the Si activation energy of 0.56 eV is obtained. Cummings, *et al.* obtained a value of 0.51 eV for 100 keV Si (1e15 cm^{-2}) implanted GaAs and annealed under As-H_2 environment [193]. The results of this study indicate that, although 525°C annealing is sufficient to heal 50 keV Si (4e13 cm^{-2}) implantation damage structurally, a higher annealing temperature (775-850°C) is necessary to achieve meaningful electrical activation.

CHAPTER 6. CONCLUSIONS

The GaAs samples investigated in this research were of a widely varying nature and, depending upon the material and processing history, the associated research details were multifarious. The entire work was divided into several independent investigations and questions related to the various research objectives were addressed accordingly. The effects of ion processing parameters and substrate and buffer layer variables on the electrical characteristics of GaAs were studied and analyzed. Several interesting and useful results have emerged from this work and are summarized in the following sections.

6.1 Orientation Effects

The key results on the comparative study of Si-implanted and RTA activated (100) and (211) GaAs are listed below :

1. Electron mobility and sheet resistance of 50 keV Si-implanted and RTA-activated GaAs are higher on (211) than on (100) orientation. This is true for both undoped and Cr-doped GaAs substrates. The non-Gaussian carrier profile in (211) GaAs (reported in [130]) could not be confirmed. Under identical processing conditions, the active layer thickness on (211) GaAs was found to be consistently smaller than on (100) GaAs.

2. Several deep levels such as EL2, EB4, EL4, EL5, and EL6 were identified in 50 keV Si-implanted and 850 °C RTA-activated (100) and (211) oriented GaAs. (211) GaAs exhibited an additional electron trap level at 0.63-0.65 eV; this is believed to be an effect of the substrate orientation. No new levels were revealed, for either orientation, when the probe depths were varied across the active layer thickness.

3. The origin of EL4 in Si-implanted and RTA-annealed GaAs has been attributed to implantation-induced damage. The source of other trap levels could not be determined but may be either due to the starting substrate, the implantation and annealing processes, or a

combination of both.

4. The traps are more distributive in nature in (211) than in (100) GaAs. Total relative trap density is apparently higher in (211) than in (100) GaAs. This is because of higher residual implantation damage in the former and is true even if the starting substrates were Cr-doped. A lower electron mobility in (211) GaAs compared to (100) GaAs correlates well with the higher relative trap concentrations found for (211) GaAs.

In summary, Si-implanted and RTA activated (100) GaAs sample exhibits better transport characteristics and has lower electron trap concentrations than an identically processed (211) GaAs. Based on these results, a superior performance of devices formed on (100) GaAs compared to (211) GaAs may be predicted.

6.2 Substrate Stoichiometry

Substrate chemistry has a significant impact on the DLTS spectra of Si-implanted and annealed GaAs. With the exception of EL4, electron traps that were present in (100) and (211) Si-implanted and RTA GaAs (undoped substrates) were apparently missing in identically processed Cr-doped GaAs substrates of either orientation. It is very likely that the substrate impurities interact with the defects and result in the formation of neutral complexes (i.e trap annihilation). The DLTS results indicate that the total relative electron trap concentration is lower for active layers formed on Cr-doped GaAs than on undoped GaAs substrates. The lower trap concentrations may eventually lead to a better performance of devices formed on Cr-doped GaAs substrates. The results of this study suggest that the RTA method is adequate for causing implant activation, and the combination of a Cr-doped substrate and RTA annealing are probably responsible for a lower electron trap concentration in Si-implanted and activated layer on Cr-doped GaAs compared to undoped GaAs substrates.

6.3 Buffer Layer

Two types of MBE buffer layers (LT GaAs and $Al_{.35}Ga_{.65}As$) were investigated and their roles in influencing the characteristics of the overlying implanted n-GaAs layers were studied. The comparison of characteristics was made with the active layers formed directly on LEC grown undoped SI GaAs substrates.

6.3.1. LT MBE GaAs Buffer Layer

The Schottky diode parameters of implanted n-GaAs with or without LT GaAs buffers were very similar except for the breakdown voltage which was higher for the diode with a LT GaAs buffer. The implanted carrier profile of GaAs on a LT GaAs buffer was sharper than in the GaAs with no buffer. The sharp carrier profile causes higher transconductance, lower drain current, and earlier pinch-off in FETs with the LT GaAs buffer than in FETs formed directly on SI GaAs.

The channel regions of FETs with and without LT GaAs buffers were devoid of any detectable traps. This absence is attributed to the out-diffusion of electron traps (definitely EL2 and EL4) into a TiWN gate during furnace annealing (827 °C for 27 min.). It has been observed that the trap diffusion behavior in GaAs is strongly dependent on the annealing methods and the nature of the capping layer. Four different hole trap levels were identified at the interface between the LT GaAs buffer and the overlying GaAs epi-layer. The appearance of hole trap peaks in electrical DLTS on an n-GaAs Schottky barrier was explained by means of an interface model due to a second space charge. The unique carrier profile of an implanted channel on a LT GaAs buffer is due to these hole traps originating from the buffer side and diffusing into the top epi-layer during subsequent processing. The sharp carrier concentration profile is responsible for many of the improved FET's performance parameters (i.e. higher g_m, lower threshold voltage etc.). The acceptor type defects in the LT GaAs buffer layer most likely contribute significantly to the phenomena of backgating observed in MESFETs with the LT GaAs buffer. Although the defects in the LT GaAs buffer are acceptor-like, their precise structural nature is unknown.

In summary, the defects in the LT GaAs buffer layers are advantageous since they result in a steeply falling carrier concentration profile, but are disadvantageous because of providing pathways for cross-talk (backgating/sidegating).

6.3.2 MBE $Al_{.35}Ga_{.65}As$ Buffer Layer

The carrier concentration profile of implanted n-GaAs on an $Al_{.35}Ga_{.65}As$ buffer (analogous to the LT GaAs buffer case) was more abrupt than the implanted n-GaAs with no buffer. The Hall mobility decreased across the interface of the implanted channel and the epi-GaAs on the $Al_{.35}Ga_{.65}As$ buffer. This is in contrast to the increased mobility across the interface between the implanted GaAs and the undoped LEC GaAs substrate (no buffer). The low temperature Hall-mobility in an implanted n-GaAs with no buffer was significantly higher than the corresponding mobility in implanted GaAs on $Al_{.35}Ga_{.65}As$ buffers. These results indicate that the interface between the active GaAs and the SI GaAs is relatively defect-free; this is not the case with the interface between the active GaAs and the epi-GaAs on $Al_{.35}Ga_{.65}As$ buffers.

Trap levels EL2 and EL4 were identified in the implanted channels on both no-buffer and $Al_{.35}Ga_{.65}As$ buffer samples. In the case of buffered samples, Si-implantation was made into an MBE-grown epi-layer. The results of this study indicate that Si implantation and furnace annealing can generate EL2 in MBE-grown GaAs. In addition, the MBE growth related traps (M1-M4) in GaAs are suppressed as a result of the subsequent implantation and annealing processes.

The SIMS measurements have identified Si, Mn, and Mg as impurities in the as-grown MBE $Al_{.35}Ga_{.65}As$ buffer layers. These impurities are the source of voltage dependent capacitance behavior of the as-grown buffer wafers. A high concentration of these impurities in the buffer is consistent with the decrease in interface Hall mobility in such samples. The non-uniformity in the threshold voltage of FETs on $Al_{.35}Ga_{.65}As$ buffer is related to the variation in impurities in the buffer layers. The source of these impurities is presumed to be related to the buffer layer growth and it is expected that a control over the impurities in the buffer layers is necessary to achieve uniformity in FETs

threshold voltage (on $Al_{.35}Ga_{.65}As$ buffer). Since FETs with $Al_{.35}Ga_{.65}As$ buffers have shown significant backgating, it is suspected that these impurities are in some way responsible for the effect. The nature of defect states or deep levels (caused by impurities or interaction between the impurities and crystal defects) in the buffer layers could not be determined because of the limitation of the DLTS technique to diode leakage current and breakdown.

There was no positive correlation between the peculiarities of FETs on $Al_{.35}Ga_{.65}As$ buffers and the electron trap characteristics of their active layers. Transport and SIMS measurements provide explanation for the higher transconductance and earlier pinch-off (due primarily to a steep implant tail) of FETs on such buffers as compared to the FET on a directly-implanted SI GaAs (i.e. no buffer). The MBE-grown undoped $Al_{.35}Ga_{.65}As$ buffer layers do have potential usage in the fabrication of GaAs MESFETs provided the impurities and the growth parameters are successfully controlled.

6.4 High Energy Implantation

MeV Si implantation and annealing of GaAs resulted in the formation of a buried active layer, the depth of which increased with increasing in ion energy. The experimental carrier concentration profiles in 2 and 6 MeV Si-implanted GaAs were broader than that predicted by TRIM calculations; this difference is attributed to the enhanced diffusion of implanted ions during MeV radiation. The transport characteristics of MeV Si-implanted buried layers are comparable to the active layer formed similarly by a keV energy Si implantation into GaAs.

Both 2 MeV as well as 6 MeV Si-implanted and RTA GaAs showed only EL2. Other trap levels were either absent or below the detection limit of the DLTS apparatus (~ 10^{-3} times the doping density). The concentrations of EL2 in these samples were significantly high (0.1-0.4 times the doping density). For the 6 MeV case, the relative EL2 density increased when the ion-dose increased from $5x10^{12}$ to $1x10^{13}$ cm^{-2}. In both 2 and 6 MeV Si-implanted GaAs, the EL2 trap was present throughout the buried active layer but its concentration towards the tail of the implant profile was reduced approximately by an order of magnitude. This result indicates that the level EL2 can be created by

MeV Si-implantation and RTA in LEC-grown GaAs.

10 MeV Si and 11 MeV S co-implanted and RTA GaAs also exhibited one dominant trap in relatively high concentration (~ 0.1), due to EL2. It appears that Si ion energies in the MeV range do not drastically affect the deep level characteristics of GaAs; all ion energies resulted in one trap level (EL2) with a high relative trap concentration. This is noticeably different from the deep level characteristics of similarly processed keV Si-implanted GaAs where multiple trap levels were identified. The difference in deep level characteristics of MeV and keV Si-implanted GaAs is explained in terms of dynamic annealing occurring during MeV Si-implantation of GaAs. The origin of the MeV Si implantation induced EL2 level in GaAs is related to the buried defect band of dislocations that remain in the buried layer even after RTA.

6.5 Electrical Activation

A proximity furnace annealing (low and high temperatures) method was employed to investigate the activation behavior of 50 keV, $4x10^{13}$ cm^{-2} Si implanted Cr-doped GaAs substrates. The key result is that the electrical activation of such samples begins at about 525 °C; an annealing temperature in the range 775 - 850 °C is required to achieve desirable activation. The structural recovery of the implanted layers precedes electrical activation and is almost complete by 525 °C.

6.6 Remarks

The results of this research have clearly demonstrated the importance of processing parameters (ion implantation, annealing, and capping) and substrate variables (stoichiometry, orientation, and buffer layers) in determining the electrical properties of Si-implanted active GaAs layers. The defect levels and the transport properties of Si-implanted GaAs layers were found to be process and substrate dependent. The quality of such active layers is extremely important in determining the performance of the devices eventually formed. The results of this study provide evidence that (100) oriented Cr-doped GaAs is a good starting substrate for Si-implantation and

subsequent RTA. The use of LT MBE GaAs or the MBE $Al_{.35}Ga_{.65}As$ buffer layers in device fabrication gives promising results provided the defects and impurities in them are better controlled. High energy (MeV) Si implantation is definitely an attractive technology for device fabrication. Apart from the ability to produce buried structures, this process yields active layers with favorable electrical properties. In addition, MeV implantation into GaAs can potentially delineate surface related defects, which is always a problem area in devices formed on GaAs surfaces. In general, the results of this work emphasize the need to control meticulously both the process parameters and the substrate properties to achieve desirable characteristics of GaAs based devices and integrated circuits.

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