ANALYSIS AND DESIGN OF MULTIPLE-OUTPUT FORWARD CONVERTER WITH WEIGHTED VOLTAGE CONTROL

by

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(ABSTRACT)

This work presents the modeling and analyses of multiple-output forward converters with weighted voltage control. Based upon the analyses, the systematic design methodologies and design tools are provided.

A power stage dc model including all the major parasitics, which are detrimental to the output voltages, is derived. A nonlinear programming based design tool is developed to search for the weighting factors. Five methods of stacking secondaries to improve cross-regulation are presented, and the improvement of cross-regulation is quantified.

A small-signal model of the multiple-output converters with coupled output filter inductors and weighted voltage control is established. The small-signal characteristics are studied, and the model shows that the system behavior is very sensitive to the coupling coefficient, which has been reported, but never been quantified. The pole-zero interlaced condition is derived. A current-mode control small-signal model is also presented, which can predict all the observed phenomena of current-mode control. Compensator design is discussed for different types of power stage transfer functions for both voltage-mode and current-mode control.

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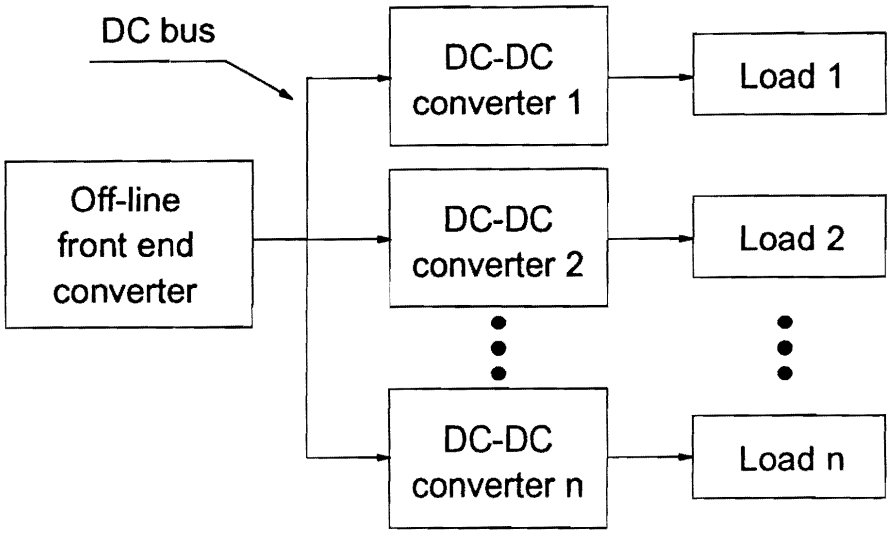
1. Introduction

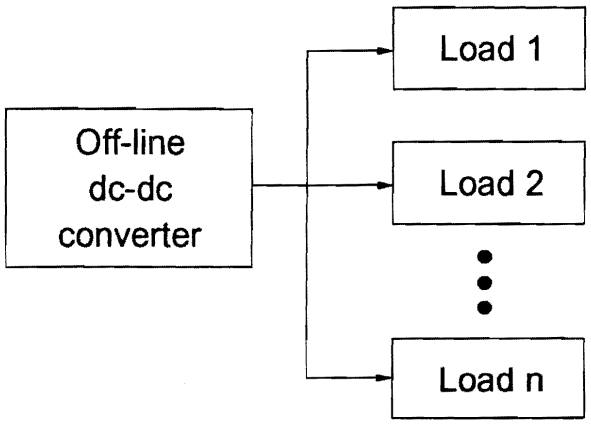
1.1 Background

For many applications, multiple-output power systems are required to deliver several isolated and regulated voltages to different loads. There are two main ways to achieve multiple outputs. One is to use a multiple-output converter (MOC) [A1 - A16], and the other is to use distributed power system (DPS) [B1-B11]. A MOC is basically a one-stage, centralized power system, while a DPS is characterized by distributing the power processing functions among a number of power converters. The basic structures of the two types of power processing are shown in Fig. 1.1.

In a DPS (either dc or ac DPS) power processing takes place in many places, which gives the DPS many advantages, such as better thermal management, increased reliability, standardized modular system, non-interrupting maintenance, and reduced size [B11]. Nevertheless, the overall system is more complex and the cost is higher, which makes DPS



(a) Distributed power system (DPS).



(b) Multiple-output converter.

Fig. 1.1. Comparison of a distributed power system and a multiple-output converter. *In the distributed power system, an off-line front-end converter provides a dc bus. A number of dc-dc converters are mounted on board, and each converter delivers the required voltage and power to its load. As for the multiple output converter, on the other hand, there is only one power processing unit, i.e., the off-line dc-dc converter, which provides all the power to different loads.*

more suitable for high power or special occasions, such as military and aerospace applications. In a MOC, on the other hand, the multiple-outputs are obtained by coupling several windings on the same transformer core. Compared with the DPS, the major advantages of using the MOC are simplicity and lower cost, which makes MOCs more suitable for commercial electronic equipment.

For a MOC, the major problem encountered in applications is how to regulate the outputs with only one power processing unit. A widely-used method of regulating a MOC is **cross-regulation**. [C1-C17] In this scheme, the only control is provided by the primary active switches, which are modulated by the feedback signal. Depending on the implementation of the feedback, this scheme can be further divided into two categories: single feedback control and weighted voltage control. The conventional approach toward regulating the multiple outputs is to sense only one output, while the unsensed outputs are cross-regulated, which may vary over a large range. In the weighted voltage control, on the other hand, several outputs are sensed and fed back to modulate the primary switches. As a result, all the sensed outputs are regulated. Although this scheme does not eliminate the output errors, it redistributes the regulation error according to the "weight" assigned to each output. If properly designed, all the outputs can be maintained within the design specifications.

To improve the regulation of a cross-regulated MOC, **secondary stacking** [C3,C16] and **coupled output filter inductors** (also referred to as **integrated magnetics**) [I1-I22] can be employed, either individually or collectively, depending on the requirements of the system. Stacking secondary sides is mainly utilized to improve dc

cross-regulation [C3,C16], whereas coupled output filter inductors are mainly utilized to improve transient response to step load or line change [I1,I3,I6,I17]. In addition to improving dynamic response, the integrated magnetic components also have the capability of so-called ripple steering [I4,I5,I8,I11,I12].

For the applications where the output voltages have to be tightly regulated, extra power processing devices can be added to the secondary sides, and this is the so-called **post regulation** [D1-D22]. There are a number of often-used methods, and three of them are stated as follows.

The simplest method is to use a **linear regulator** in the power channel, where the output voltage is to be tightly regulated, but excluded from the feedback signal [D1-D3]. In this regulation scheme, the secondary voltage to be post-regulated is deliberately set higher than it really needs to be. A linear regulator is then inserted between the secondary and the output, providing a regulated output voltage. Since the post-regulator operates in the linear region of the semiconductor device, there is a relatively large voltage drop, and this large voltage drop will cause excessive power loss, especially when the load current is large. Therefore, linear regulators are basically limited to low power and low current applications.

The second post-regulation method is to use a **saturable reactor** (also referred to as **magamp**) to post-process the power again [D4-D15]. As the main switch in the primary starts conducting, essentially the voltage across the secondary winding is blocked by the saturable reactor, since the core is working in the linear region, and the corresponding inductance is very large. After the core is saturated, the saturable reactor

exhibits little impedance, and the secondary voltage is transferred to the output. By controlling the reset time of the saturable core, the voltage block time can be adjusted, thereby controlling the output. This regulation scheme dominates the high current applications. But the power stage becomes more complex, and extra control circuitry is needed to provide the necessary regulation.

The third post-regulation scheme is to use a **synchronous switch post regulator** which emerged in late 70's [D16-D18]. As the rapid development and improvement of semiconductor devices make synchronous rectifiers more popular, this technique attracts more attention in multiple-output power supplies [D19-D21]. For the applications with the load current between 2 A and 20 A, it is a very attractive alternative to other regulation schemes, such as saturable reactors. In addition, it can eliminate the "dummy load" for no load operation. The main drawback of this technique is that the extra driving circuitry is needed, which complicates the control circuit. The extra switching operation may result in a noisier system.

In addition to the cross-regulation and post-regulation, there is another effective but less used regulation method. From the above discussion, it can be seen that imperfect regulation in MOC is mainly due to the fact that only one control variable, which is the duty cycle, d, is utilized to regulate more than one output. If the number of the outputs is limited to two, **pulse-width modulation (PWM)** and **frequency modulation (FM)** can be used simultaneously to achieve perfect regulation for both outputs [E1-E10]. For this control scheme, one output has to operate in a continuous conduction mode (CCM) and the other one in a discontinuous conduction mode (DCM). The voltage of the output with

CCM operation is controlled only by PWM, while the voltage of the output with DCM operation is controlled by both PWM and FM. Therefore, both outputs can be tightly regulated to the desired values. Variable frequency control prevents this regulation method from wide application. Besides, its application is strictly limited to the converters with two outputs.

Figure 1.2 summarizes all the aforementioned regulation schemes. In view of efficiency, complexity, and cost, the cross-regulation is usually the first design choice. Yet, many important issues pertaining to the design of cross-regulated MOCs have not been solved; these issues are identified as follows:

- the effects of the parasitics in the circuit, such as the leakage inductances of the transformer and the voltage drops of the rectifier diodes, on the output voltages,
- selection of the weighting factors to meet the desired regulation specifications,
- methods of improving cross-regulation,
- small-signal model for MOCs with weighted voltage control and coupled inductors,
- compensator design for MOCs with weighted voltage control and coupled inductors,
- current model control for MOCs with weighted voltage control and coupled inductors.

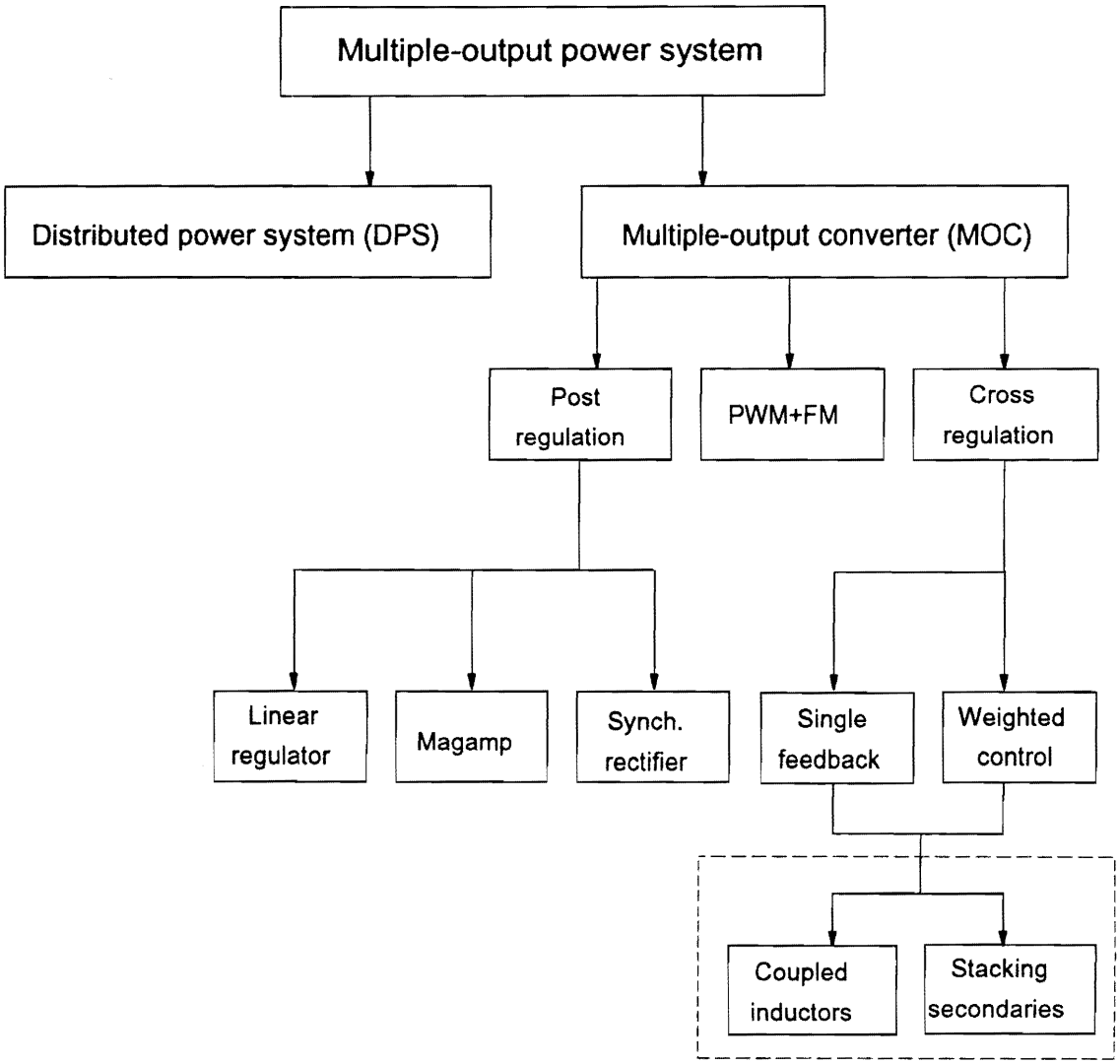


Fig. 1.2. Classification of multiple-output power systems. *The use of coupled inductors and stacking secondaries is optional. They can be used either individually or collectively, depending on the application.*

1.2 Objective

The objective of this work is to perform a comprehensive study of multiple-output converters with weighted voltage control, and based upon that to provide systematic design methodologies.

1.2.1 DC Analysis and Design

To reveal the relations between the output voltages and the parasitics and to facilitate design, an analytical dc model is derived [C14], and based on that a design method for the weighting factors is presented. The design of the weighting factors uses a nonlinear programming technique and is coded into a program. The presented design tool can automatically search for the feasible solution for the weighting factors, and the solution is the "best" in the sense that the total error between the output voltages and the nominal voltages is minimal.

As an effective way to improve cross-regulation, stacking secondary sides is often used in a MOC. An analytical model is established, and the improvement of cross-regulation is quantified [C15]. The analysis reveals the mechanism of improving cross-regulation, and the results are incorporated into the design tool.

Since the transformer leakage inductances affect the dc output voltages, a transformer model which characterizes the leakage phenomenon is also derived, which can be used to predict the output voltages more accurately, although numerically.

1.2.2 Small-Signal Analysis and Design

Another important aspect of MOCs is the compensator design in the control loop. A good design should guarantee the system stable under all the operating conditions, and at the same time provide fast response and small over/under shoot during transients. There are not many published papers devoted to this issue. Most of the work from a handful of published papers focused on the stability analysis, dealing with little of the design issue [F7-F11]. Only one paper discussed some design issues [F10], but some of the conclusions presented in the paper are misleading due to some derivation errors and improper interpretations of the analytical results.

In the light of the need to understand the small-signal behavior, a small-signal model for multiple-output forward converters is developed to predict the effects of the weighting factors and coupled output filter inductors on the small-signal characteristics [F11]. The model is derived by using PWM switch model [F5], and the experimental and model predictions agree well. Based on the model, the methodology of compensator design is presented.

Current mode control is often used in MOCs, but there are very few papers discussing this issue [G11]. A new small-signal model for MOCs with current mode control is developed. The model includes the coupled output filter inductors, which is very useful information but has never been reported so far. The model can correctly predict some unique characteristics for current model control, such as subharmonic oscillation when the duty cycle approaches 50%. The compensator design for MOCs with current mode control is also proposed.

1.3 Dissertation Outline

In Chapter 2, the dc analysis is performed, and based upon that, the design procedure is proposed. A nonlinear optimization-based design tool is developed to help find the optimal weighting factors.

Chapter 3 discusses stacking of the secondaries, revealing how stacking can improve dc cross-regulation. Various stacking methods are presented, analyzed, and compared. The results are incorporated into the design tool.

Chapter 4 is focused on small-signal analysis and design of multiple-output converters. First, a unified small-signal model is developed, which covers the converters

with coupled inductors and weighted-voltage control. The model explains why the multiple-output converters tend to be unstable if the control loop is closed at a relatively high frequency. Based on the analysis, some design issues are discussed.

In Chapter 5, a small-signal model for the multiple-output converters with current-mode control is developed. The current-mode cell for the multiple-output converters is identified. The feedforward and feedback gains are derived, which characterize the dependence of the sensed current on the variation of input and output voltages, and are quite different from those of a single-output converter.

Major conclusions are presented in Chapter 6. The design tools which perform the dc and small-signal analyses and designs are provided in Appendices A and B.

A new model for multiple-winding transformers, which characterizes the leakage phenomenon of transformers, is provided in Appendix C. The unique feature of the model is that each parameter has a distinctive physical meaning and corresponds to a part of the leakage flux. For high frequency applications where the leakage effects on the output voltages are dominant, this model can be used to predict cross-regulation characteristics.

2. DC Analysis and Design of Weighted Voltage Control for Multiple-Output Converters

2.1 Introduction

The most commonly-used method of regulating multiple-output converters is to sense one output while cross-regulating the remaining outputs. This regulation scheme provides tight regulation for the sensed output. The cross-regulated outputs, however, may severely deviate from the desired values, especially during transients such as a step load change. The transient characteristics of the cross-regulated outputs can be improved dramatically by coupling the output filter inductors. While this approach improves the dynamic behavior of the cross-regulated outputs, it does not improve their dc cross-regulation characteristics significantly, except when one power channel is operating at a discontinuous conduction mode (DCM).

Simultaneous improvements of the transient and dc performances of the cross-

regulated outputs can be obtained by sensing and regulating two or more outputs simultaneously, as illustrated in Fig. 2.1, which is herein referred to as *weighted voltage control* (WVC). Instead of controlling only one output, a number of outputs are sensed, and the weighted sum of the output voltages is fed back to modulate the duty cycle, d. Compared with the conventional single-output-sensing feedback control, the WVC redistributes the dc regulation error among the sensed outputs. If the weighting factors and the compensator are properly designed, the dc cross-regulation and dynamic characteristics of the sensed outputs can be significantly improved.

Although the weighted control has been widely used on many power supply designs, there are no systematic analysis and design procedure for this control method, and most designs are performed on the trial-and-error basis. The effort of this chapter is to develop an analytical model, and based upon that provide design insight for multiple-output forward converters employing the weighted voltage control. More specifically, the focus is on the determination of the weighting factors in order to meet the desired dc regulation specifications.

First, a power stage model, including the effects of all the major parasitics, is derived, revealing the critical parameters which affect the dc regulation. Then the closed-loop dc regulation is calculated, thereby relating the output voltages to the weighting factors. From the design specifications, the feasible range of the weighting factors $\{K_i\}$ is identified. For the converters with dual output, the identification of the feasible range for the weighting factors can be performed graphically on K_1-K_2 plane. When dealing with more than two outputs, it is difficult to visualize the feasible range over 3-D (or even

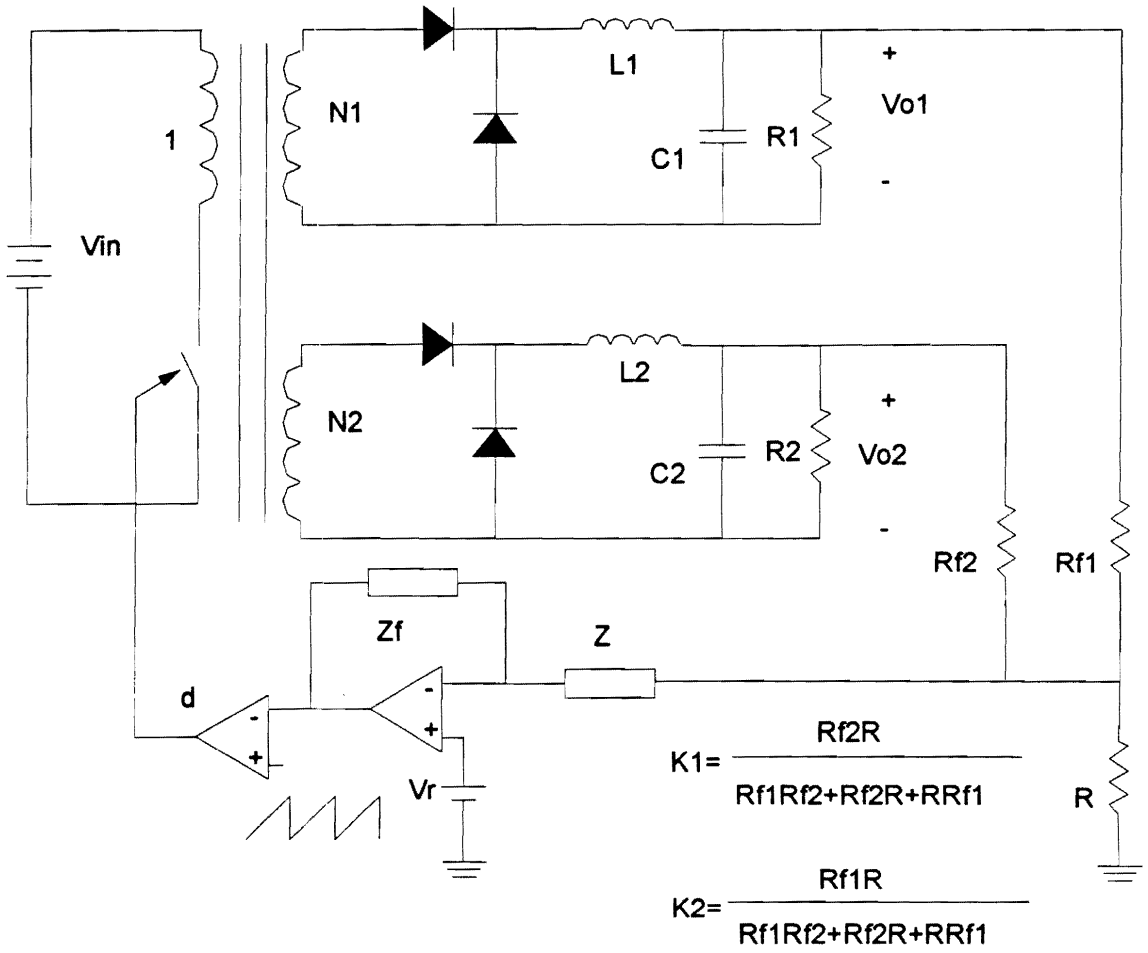


Fig. 2.1. A dual-output forward converter with weighted voltage control. Multifeedback provides more design freedom. By changing the ratio of the weighting factors, K_1 and K_2, the output voltages can be adjusted. The reset circuitry is not shown here.

higher order) space. Therefore, the process of identification of the feasible range for $\{K_i\}$ has to be automated. A design tool is provided which is based on the nonlinear programming technique. Since the objective function used is the weighted sum of the squared differences between the calculated and specified output voltages, the weighting factors are to be chosen automatically in the middle of the feasible range for the weighting factors, if there is any. Besides, the design tool can solve the design problem with any number of outputs.

The proposed design procedures are applied to two-output and three-output converters respectively. The calculations are experimentally verified.

2.2 DC Model of the Power Stage

Generally, the quality of cross-regulation depends on a number of the circuit parasitics. The major parasitics are the forward voltage drops of the rectifier diodes, the leakage inductances of the transformer, and the winding resistances of the transformer and the output filter inductors. In this section, the effects of these major parasitics on dc output voltages are investigated, and the analytical expressions for dc output voltages are derived.

2.2.1 Modeling of Major Components

The output circuit (drain-to-source) of the MOSFET is modeled as an ideal switch in series with a resistor whose value is equal to the on-resistance R_{ds} of the MOSFET. The parasitic output capacitance of the MOSFET is modeled by a capacitor C_{ds} placed in parallel with the ideal switch and the resistor, as shown in Fig. 2.2.(a).

The diodes can be modeled as an ideal diode in series with a voltage source and a resistor, as shown in Fig. 2.2.(b). Then the voltage across the diode can be expressed as:

$$V_D = V_d + I_D R_d, \tag{2.1}$$

where V_d is the offset voltage, which represents the invariant part of the forward voltage drop of the diode, and R_d is the on-resistance of the diode, which represents the varying part of the forward voltage drop of the diode.

Since the output filter inductors essentially carry dc currents, they can be modeled as an ideal inductor in series with a dc resistor, as shown in Fig. 2.2.(c).

The transformer is modeled as an ideal transformer plus its parasitics. The parasitics which are particularly critical to cross-regulation are the winding resistances and the leakage inductances. Using the structure in which the transformer primary winding is sandwiched between the secondary windings allows the leakage inductances to be lumped on the secondary sides and the magnetizing inductance to be located on the primary side [H6, H7]. The voltage drop across each winding is characterized by a lumped resistance

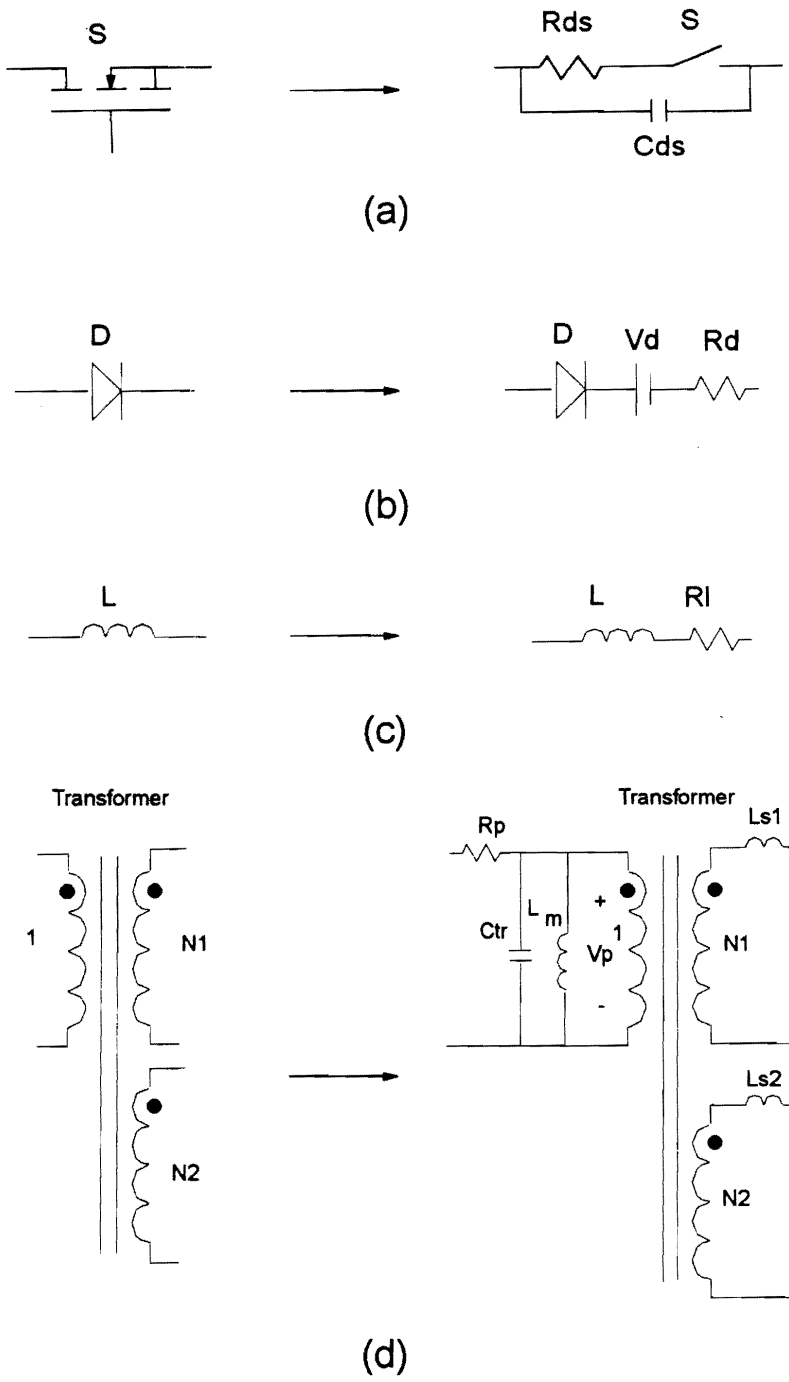


Fig. 2.2. ***Modeling of the major components.*** *The power stage components can be represented by their ideal counterparts and parasitics: (a) active switch; (b)diode; (c) inductor; (d) transformer.*

placed in the corresponding winding. Since the core loss does not have much effect on cross regulation, the core loss is neglected in the transformer model, as shown in Fig. 2.2.(d).

Replacing each component with its corresponding model, a simplified power stage circuit model is obtained, as shown in Fig. 2.3. Based on this circuit model, the analytical expressions for the output voltages can be obtained.

2.2.2 Derivation of the DC Output Voltage

The basic idea of calculating the output voltages is to decouple the primary side from the secondary sides. The primary and secondary sides are treated separately. Then the voltage at the input of each output filter inductor is averaged to obtain the corresponding output voltage.

2.2.2.1 Analysis of the Primary Side

During the on-state of the active switch, the current flowing through the MOSFET and the primary winding consists of two parts: the reflected load currents and the magnetizing current. For a properly designed transformer, the magnetizing current is small compared with the reflected load currents, so it can be assumed to be zero. As a result, the voltage across the primary winding is the line voltage V_{in} reduced by the

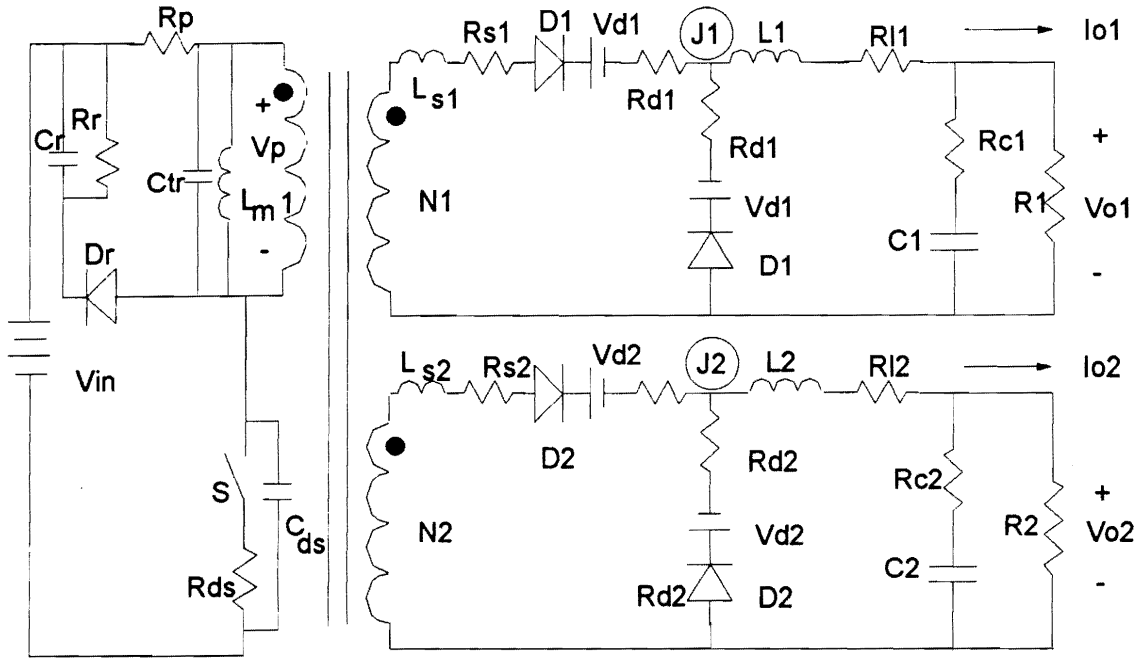


Fig. 2.3. ***The power stage dc model with each component substituted with its corresponding circuit model.*** *DC regulation characteristics are mainly decided by the parasitics inside the circuit. Their effects can be quantified analytically.*

voltage drops across the primary winding resistance and the channel resistance of the active switch. The value of the primary voltage is

$$V_p = V_{in} - I_p R_{on} - \Delta V_{pcu}, \tag{2.2}$$

where

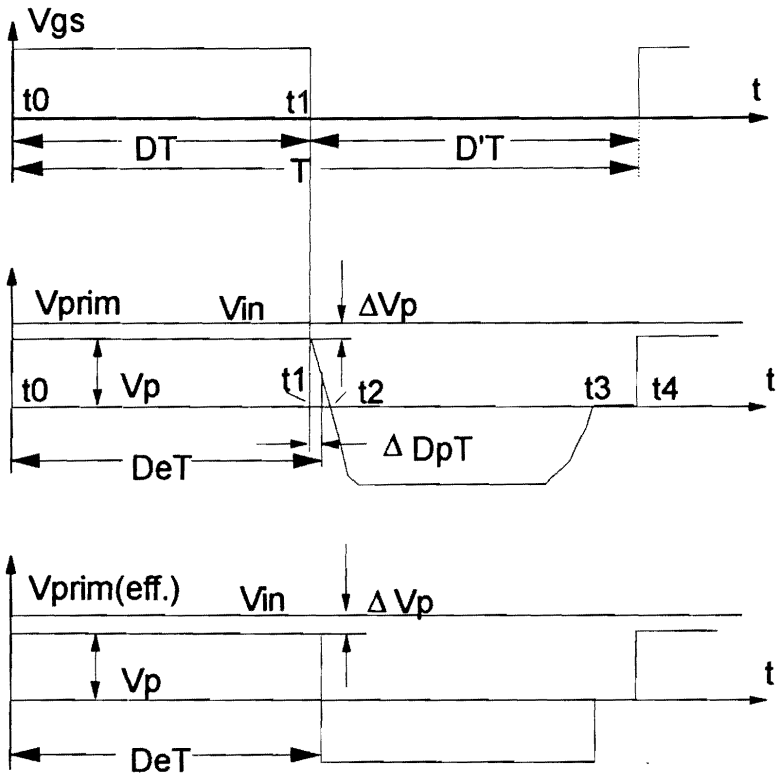
V_{in} - line voltage,

R_{on} - on-resistance of the switch,

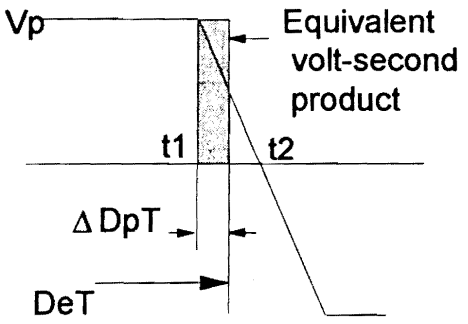
I_p - magnitude of the current in the primary, $I_p = N_1 I_{o1} + N_2 I_{o2}$,

ΔV_{pcu} - voltage drop across the primary winding. If the radius (or half of the thickness) of the winding is less than the skin depth, ΔV_{pcu} can be approximated as $I_p R_{pdc}$; otherwise, the calculation involves harmonic decomposition.

As the active switch is turned off, the reversal of the transformer voltage takes a finite time Δt_p to charge the parasitic capacitance C_{ds}, which is a nonlinear function of the drain-to-source voltage, and any other capacitance connected to the drain of the MOSFET (*e.g.*, the capacitance of the transformer and the reset circuitry, *etc.*). As a result, the voltage across the primary winding of the transformer does not drop to zero till t_2 (Fig. 2.4). This charging process causes an effective duty cycle extension ΔD_p. Generally, the rigorous calculation of the duty cycle extension is extremely involving. However, the analysis can be simplified by assuming a large magnetizing inductance of the transformer so that the primary current can be modeled as a constant current source with the value



(a) The primary waveforms.



(b) Magnification of Vprim waveform during t1-t2.

Fig. 2.4. ***The primary voltage in one switching period.*** *Due to the parasitic capacitances in the circuit, a positive voltage is still applied across the primary of the transformer even when the gate drive signal is removed. This duty cycle extension can be quantified by equivalent volt-second product.*

equal to the sum of the reflected output currents. In this case, the time needed to charge the parasitic capacitances is

$$\Delta t_p = t_2 - t_1 = \frac{C_t V_{in} + 10 C_o \sqrt{V_{in}}}{I_p}, \tag{2.3}$$

and the corresponding duty cycle extension can be calculated based on the equivalent volt-second product, Fig. 2.4(b),

$$\Delta D_p = \frac{\Delta t_p}{2T_s} = \frac{C_t V_{in} + 10 C_o \sqrt{V_{in}}}{2 I_p} f_s. \tag{2.4}$$

where

C_t - total capacitance of the transformer and the reset circuitry,

C_o - junction capacitance of the MOSFET when V_{ds}=25 V,

f_s - switching frequency,

T_s - switching period, $T_s = 1/f_s$.

Therefore, the voltages across the transformer windings have an effective duty cycle

$$D_e = D + \Delta D_p. \tag{2.5}$$

2.2.2.2 Analysis of the Secondary Sides

Every secondary of the transformer can be modeled by a voltage source with the magnitude equal to the reflected primary voltage, or $V_s = NV_p$, with an effective duty cycle

D_e. To simplify analysis, the current through the output filter inductor is assumed to be constant, equal to the load current. Since the load current flows through either diode D_A or diode D_B, which are usually of the same type, the voltage source and the resistance of the diodes D_A and D_B can be shifted to the branch in series with the output filter. Figure 2.5 shows the simplified secondary subcircuit diagram and waveforms in one complete switching cycle. When the active switch in the primary is turned on at $t=t_o$, voltage is induced immediately on the secondary windings. During time interval t_o - t_1, D_B is still conducting, and the current is commutating from D_B to D_A (Fig. 2.5(a)). As long as D_B is conducting, the voltage at node J, V_J, is equal to zero. During t_1- t_2, D_B is cut off and D_A carries all the load current (Fig. 2.5(b)). During t_2 - t_3, the switch is turned off, and the voltage V_J becomes zero again, since the load current is commutating from D_A to D_B (Fig. 2.5(c)). During t_3 -t_4, only D_B is conducting, and V_J is zero (Fig. 2.5(d)). In a complete switching cycle, V_J is a square wave with a duty cycle loss caused by the leakage inductance. The duty-cycle loss at node J is

$$\Delta D_s = \frac{L_s}{V_s} f_s I_o, \tag{2.6}$$

where

V_s - secondary voltage, L_s - leakage inductance, I_o - load current.

The voltage drop caused by the secondary winding resistance, ΔV_{scu}, can be calculated using the same approach as the one described for the primary winding.

The total voltage drop across the diodes equals:

$$V_D = V_d + I_o R_d. \tag{2.7}$$

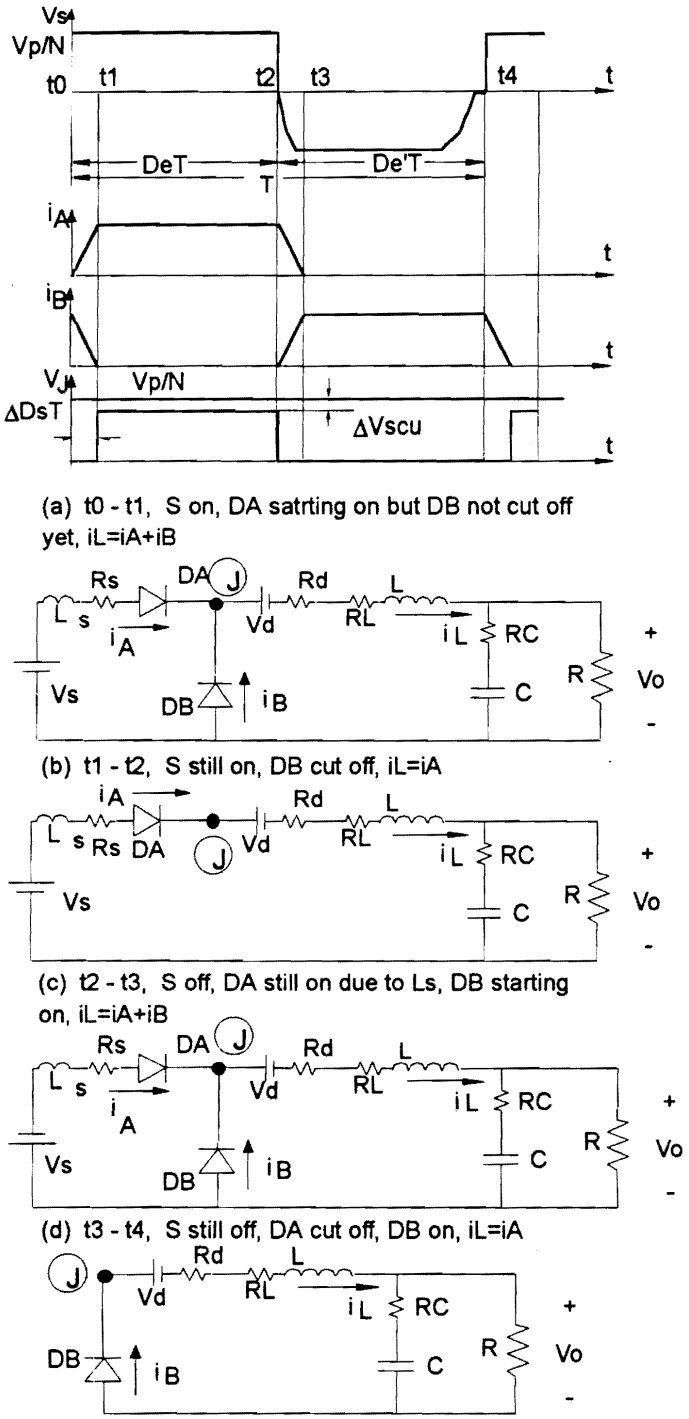


Fig. 2.5. ***The secondary waveforms and corresponding subcircuit diagram in one switching period.*** *The inductive parasitics cause a duty cycle loss, whereas the resistive parasitics cause voltage drop.*

2.2.2.3 Output Voltages

The output voltage V_o can be calculated by averaging V_J, which is a square wave with the magnitude equal to the secondary voltage minus the voltage drop across the secondary winding and the duty cycle D_e-ΔD_s, over a switching period:

$$V_o = (D_e - \Delta D_s)(V_s - \Delta D_{scu}) - V_D - I_o R_L. \tag{2.8}$$

By neglecting the second order term, the output voltage in Eq. (2.8) can be written as:

$$V_o = D_e V_A - V_B, \tag{2.9}$$

where

$$V_A = V_s - \Delta V_{scu} = NV_p - \Delta V_{scu}, \tag{2.10}$$

$$V_B = V_d + I_o(f_s L_s + R_d + R_L) = V_d + I_o Z_B, \tag{2.11}$$

where

$$Z_B = f_s L_s + R_d + R_L. \tag{2.12}$$

V_A quantifies the effects of input voltage, the transformer turns ratio, winding resistance, and the on-resistance of the active switch on the output voltage. V_B quantifies the voltage variation induced by the leakage inductance of the transformer, the resistances of the rectifier diodes and the output filter inductor. As can be seen from Fig. 2.6, the output voltage level depends mainly on V_A, while the voltage variation range depends

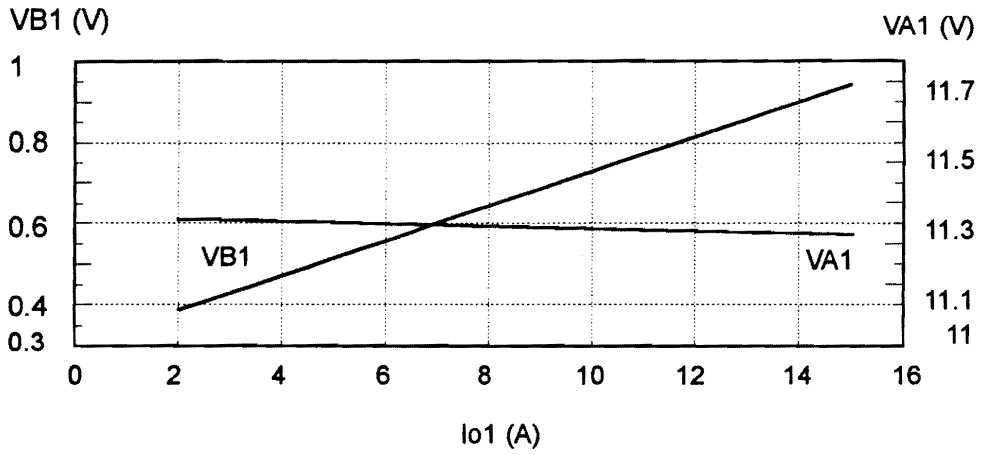


*Fig. 2.6. **Dependence of V_A and V_B on load current I_{o1}.** V_A shows if the secondary is correctly centered and V_B indicates voltage variation range.*

mainly on V_B. These two quantities, therefore, provide useful information for design. Improper centering can be improved by adjusting V_A, whereas large voltage variation can be improved by refining the term V_B.

The quality of cross-regulation is determined by the combined effect of the forward voltage drop of the rectifier diodes, the inductor winding resistors, and the leakage inductances. To improve the cross regulation, it is important to decrease the total value of the internal impedance, rather than the value of the individual parasitic parameter.

2.3 Selection of Weighting Factors

For a multiple-output dc-dc converter with weighted control, each output is not only related to the circuit parameters, but also to the weighting factors, $\{K_i\}$. The purpose of this section is to establish relations between the output voltages and the weighting factors for a dual-output converter, as shown in Fig. 2.1.

As derived in the last section, the output voltages can be expressed as:

$$V_{o1} = D_e V_{A1} - V_{B1}, \tag{2.13}$$

and

$$V_{o2} = D_e V_{A2} - V_{B2}, \tag{2.14}$$

where $\{V_{Ai}\}$ and $\{V_{Bi}\}$ are defined in Eqs. (2.10) and (2.11) for outputs 1 and 2, respectively.

In the steady state, the feedback renders the sum of the weighted output voltages equal to the reference voltage (Fig. 2.7), *i.e.*,

$$V_r = K_1(D_e V_{A1} - V_{B1}) + K_2(D_e V_{A2} - V_{B2}). \tag{2.15}$$

Solving Eq. (2.15) for D_e

$$D_e = \frac{V_r + K_1 V_{B1} + K_2 V_{B2}}{K_1 V_{A1} + K_2 V_{A2}}, \tag{2.16}$$

and substituting D_e into Eqs. (2.13) and (2.14) yields the closed-loop output voltages:

$$V_{o1} = \frac{V_r + K_1 V_{B1} + K_2 V_{B2}}{K_1 V_{A1} + K_2 V_{A2}} V_{A1} - V_{B1}, \tag{2.17}$$

and

$$V_{o2} = \frac{V_r + K_1 V_{B1} + K_2 V_{B2}}{K_1 V_{A1} + K_2 V_{A2}} V_{A2} - V_{B2}. \tag{2.18}$$

For a given power stage (given L_s, R_L, V_d, R_d, *etc.*,) the output voltages calculated from Eqs. (2.17) and (2.18) are only functions of input voltage, load currents and weighting factors, *i.e.*,

$$V_{oi} = f(I_{o1}, I_{o2}, V_{in}, K_1, K_2), \qquad i = 1, 2. \tag{2.19}$$

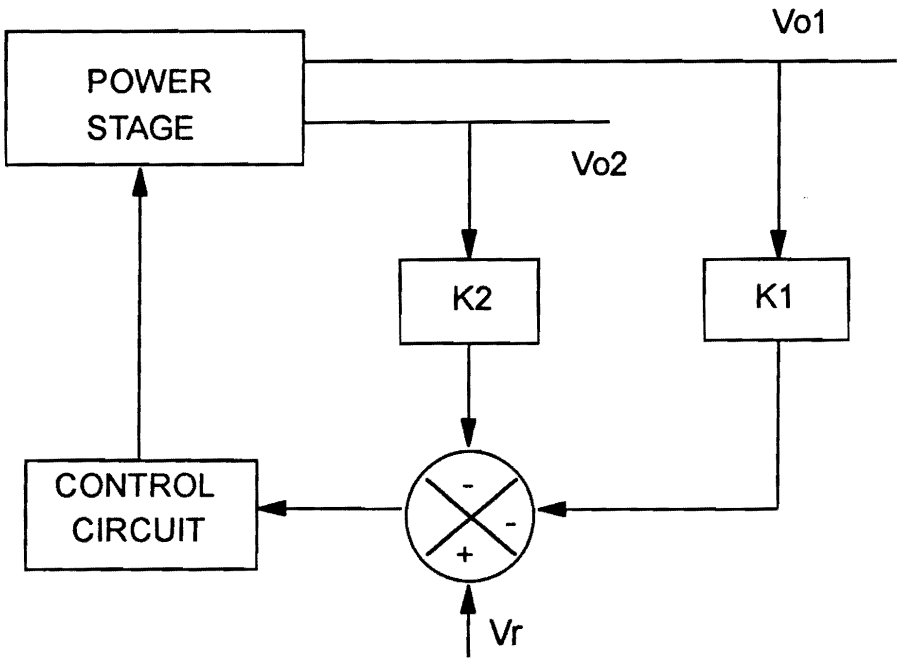


Fig. 2.7. Feedback control block diagram. *The weighted sum of the output voltages V_{o1} and V_{o2} is forced to be equal to the reference voltage, V_r. This relation relates the output voltages, V_{o1} and V_{o2}, to the weighting factors, K_1 and K_2.*

The output voltages reach their extremes at low line when one output is at the full load and the other at light load, *i.e.*,

$$V_{o1}^{max} = f_1(I_{o1}^{min}, I_{o2}^{max}, V_{in}^{min}, K_1, K_2), \tag{2.20}$$

$$V_{o2}^{min} = f_2(I_{o1}^{min}, I_{o2}^{max}, V_{in}^{min}, K_1, K_2), \tag{2.21}$$

and

$$V_{o1}^{min} = f_1(I_{o1}^{max}, I_{o2}^{min}, V_{in}^{min}, K_1, K_2), \tag{2.22}$$

$$V_{o2}^{max} = f_2(I_{o1}^{max}, I_{o2}^{min}, V_{in}^{min}, K_1, K_2). \tag{2.23}$$

The design objective is to keep the output voltages within the dc specifications for any load and line conditions,

$$V_{o1}^{min} \geq V_{o1(spec)}^{min}, \tag{2.24}$$

$$V_{o1}^{max} \leq V_{o1(spec)}^{max}, \tag{2.25}$$

$$V_{o2}^{min} \geq V_{o2(spec)}^{min}, \tag{2.26}$$

$$V_{o2}^{max} \leq V_{o2(spec)}^{max}. \tag{2.27}$$

Depending on the design specifications, Eqs. (2.24) - (2.27) define different regions of feasible values of K_1 and K_2. The following scenarios are discussed.

1) Inequalities (2.24) - (2.27), with K_1 and K_2 axes together, specify a closed region in the first quadrant, Fig. 2.8(a). It is noticed that the feasible region is bounded by the K_1 and

K_2 axes. Even if one of the weighting factors assumes the value of zero, the dc regulation specifications can still be met. Therefore, the cross-regulation through single feedback can be viewed as a special case of weighted control. Usually, this is the case for loose regulation specifications.

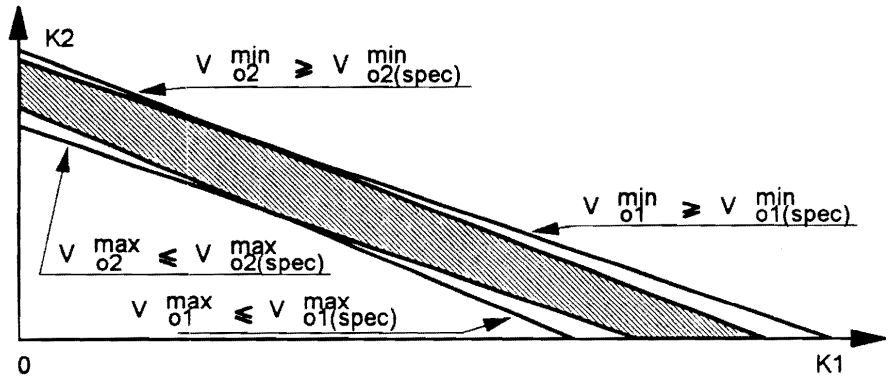
2) Inequalities (2.24) - (2.27) specify a closed region in the first quadrant as shown in Fig. 2.8(b). This corresponds to tighter regulation specifications. The single feedback control can never meet the regulation requirements.

3) Inequalities (2.24) - (2.27) do not specify a common region in the first quadrant as shown in Fig. 2.8(c). This situation implies that the design specifications are too tight for the given power stage circuit parameters, or the power stage design is inadequate to meet the regulation requirements. No matter what values of the weighting factors are selected, the regulation specifications cannot be met. Under this scenario, the design specifications must be relaxed, or else the power stage must be redesigned to accommodate the specifications.

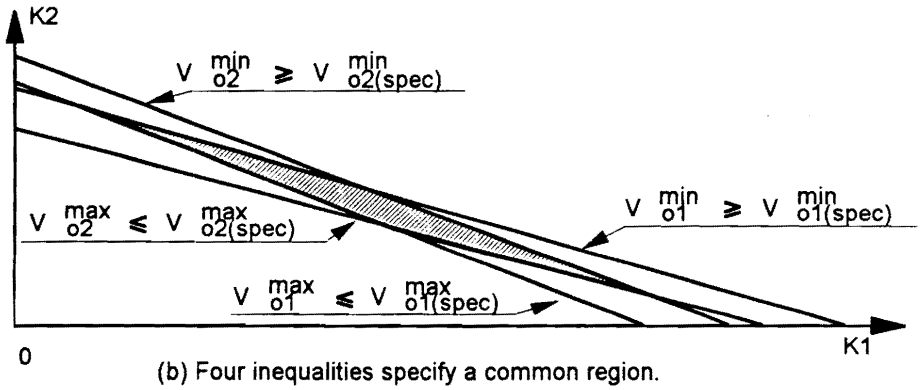
Once the weighting factors $\{K_i\}$ are selected, the parameters of the voltage divider network in Fig. 2.1 can be easily calculated. Assuming that R has been chosen, R_{f1} and R_{f2} are

$$R_{f1} = \frac{1-(K_1+K_2)}{K_1} R, \tag{2.28}$$

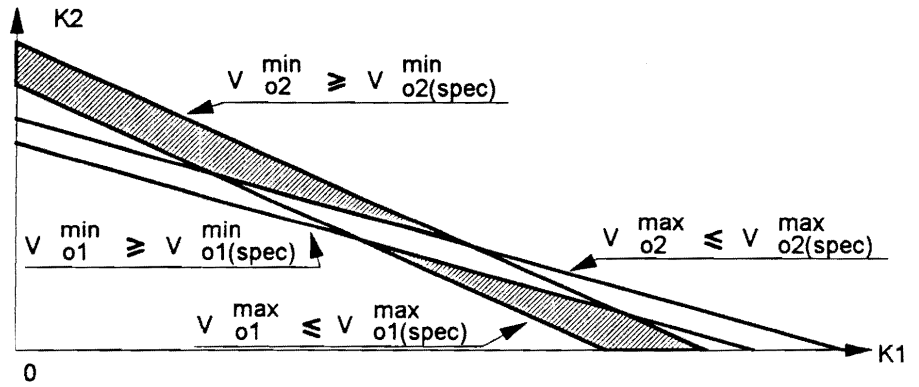
$$R_{f2} = \frac{1-(K_1+K_2)}{K_2} R. \tag{2.29}$$



(a) Four inequalities with K1 and K2 axes specify a common region.



(b) Four inequalities specify a common region.



(c) There is no common region. Relax the design specifications or redesign the power stage.

Fig. 2.8. Three different cases for the weighting factors $\{K_i\}$. As the dc regulations are more tightly specified, the feasible region for the weighting factors, K_1 and K_2, becomes smaller. To a certain point, there no longer exists a common region for K_1 and K_2.

2.4 Design Illustration

The design of a multiple-output dc-dc converter with weighted control is an iterative process, as shown in Fig. 2.9. The whole process starts from the power stage design which can follow the standard design procedure [K3]. After the power stage parameters are decided, the output voltages are calculated, and Eqs. (2.24) - (2.27) are used to determine if there exists a feasible region for the weighting factors. If no feasible region is found, the power stage has to be redesigned. If still no feasible region is found after a number (which is predetermined) of iterations, the design specifications will have to be relaxed. Then the same process can be carried on again for the new specifications. If the feasible region is finally found, a set of weighting factors $\{K_i\}$ is selected. The design could stop here. However, it is suggested that a large signal simulation is performed with the designed parameters using some circuit simulator, such as PSpice or Saber. If the simulation confirms that the design specifications are met, the design is finished. Otherwise, more iterations will be needed.

To demonstrate the described dc analysis and the proposed method of determining weighting factor, a dual-output forward converter was designed with the following dc specifications:

- input line voltage V_{in}, $120\ V$ - $190\ V$,
- 5 V output: $4.8V \le V_{o1} \le 5.2V$, $2A \le I_{o1} \le 15A$,
- 12 V output: $11.5V \le V_{o2} \le 12.7V$, $0.5A \le I_{o2} \le 3A$.

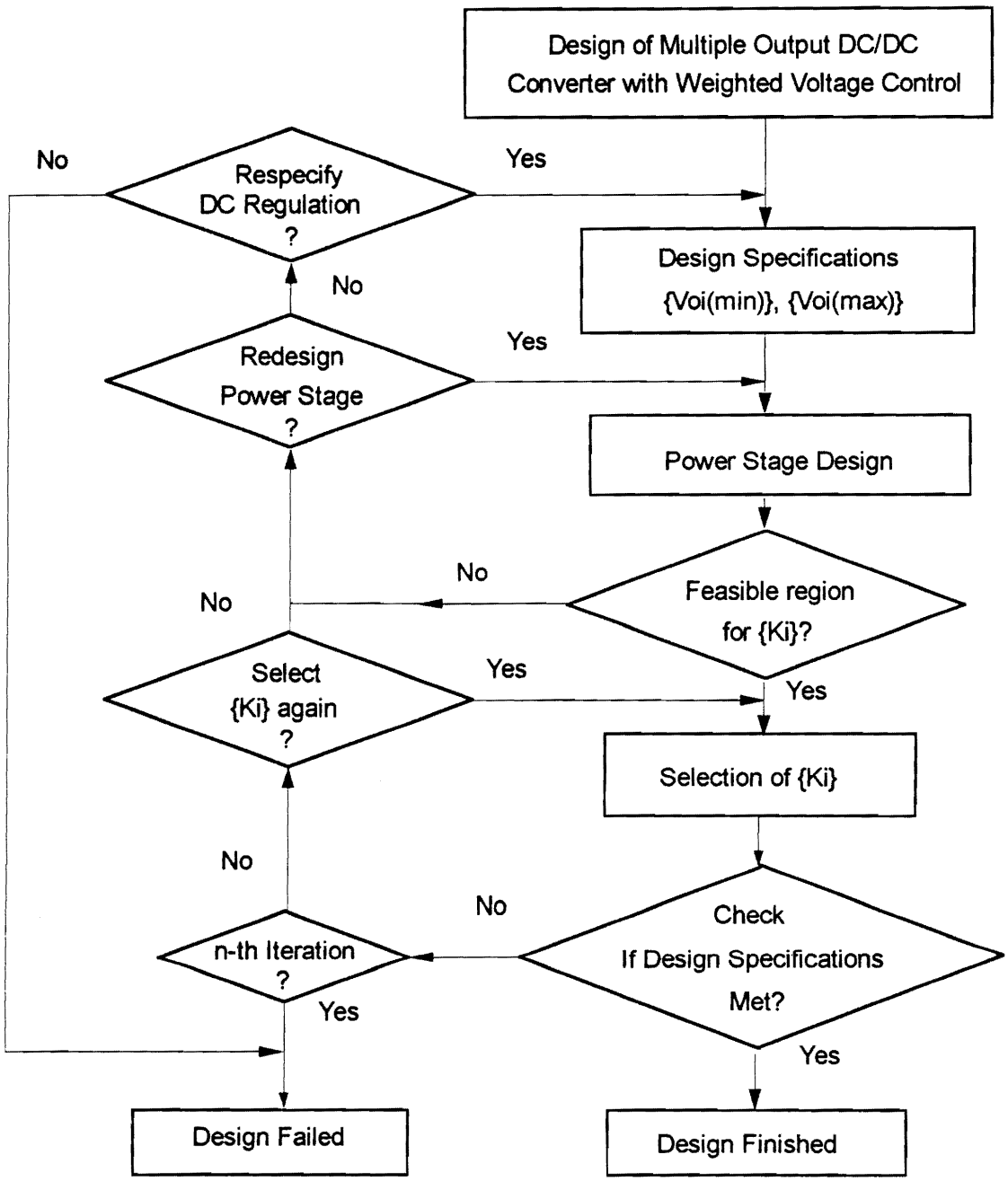


Fig. 2.9. The design procedure for a multiple-output converter with weighted voltage control. *The design is an iterative process. It should be realized that if the dc regulation specifications are too tight, there may exist no feasible solutions for the weighting factors.*

Following the well-established design procedure for the forward converter power stage, the experimental forward converter operating at 100 kHz was built with the following components: active switch S, IRFPE50; 5-V output rectifier diodes D_{A1} and D_{B1}, IR62CNQ030; 12-V output rectifier diodes D_{A2} and D_{B2}, IR30CNQ045. The transformer is made of TDK EEC28LZ core with 28 turns 3xAWG27 as the primary winding, 3 turns 0.12x12 mm copper foil as 5-V secondary winding, and 7 turns 6xAWG27 wire as the 12-V secondary winding. The circuit diagram is shown in Fig. 2.10, and the values of the parameters are listed in Table 2.1

By substituting the power stage parameters listed in Table 2.1 into Eqs. (2.24) - (2.27), the following inequalities are obtained:

$$5.2K_1 + 12.34K_2 \geq 2.515, \tag{2.30}$$

$$4.8K_1 + 13.248K_2 \leq 2.515, \tag{2.31}$$

$$4.566K_1 + 12.7K_2 \geq 2.515. \tag{2.32}$$

$$4.838K_1 + 11.5K_2 \leq 2.515. \tag{2.33}$$

Plotting the boundary lines defined by Eqs. (2.30) - (2.33) in Fig. 2.11, it can be seen that they do not define a common region. This means that either the power stage is not properly designed or the design specifications are too tight. Assuming the design specifications are not allowed to be relaxed, then the only way to find feasible weighting factors $\{K_i\}$ is to redesign the power stage.

Typically, the improper design of the power stage results from two aspects: (1) the

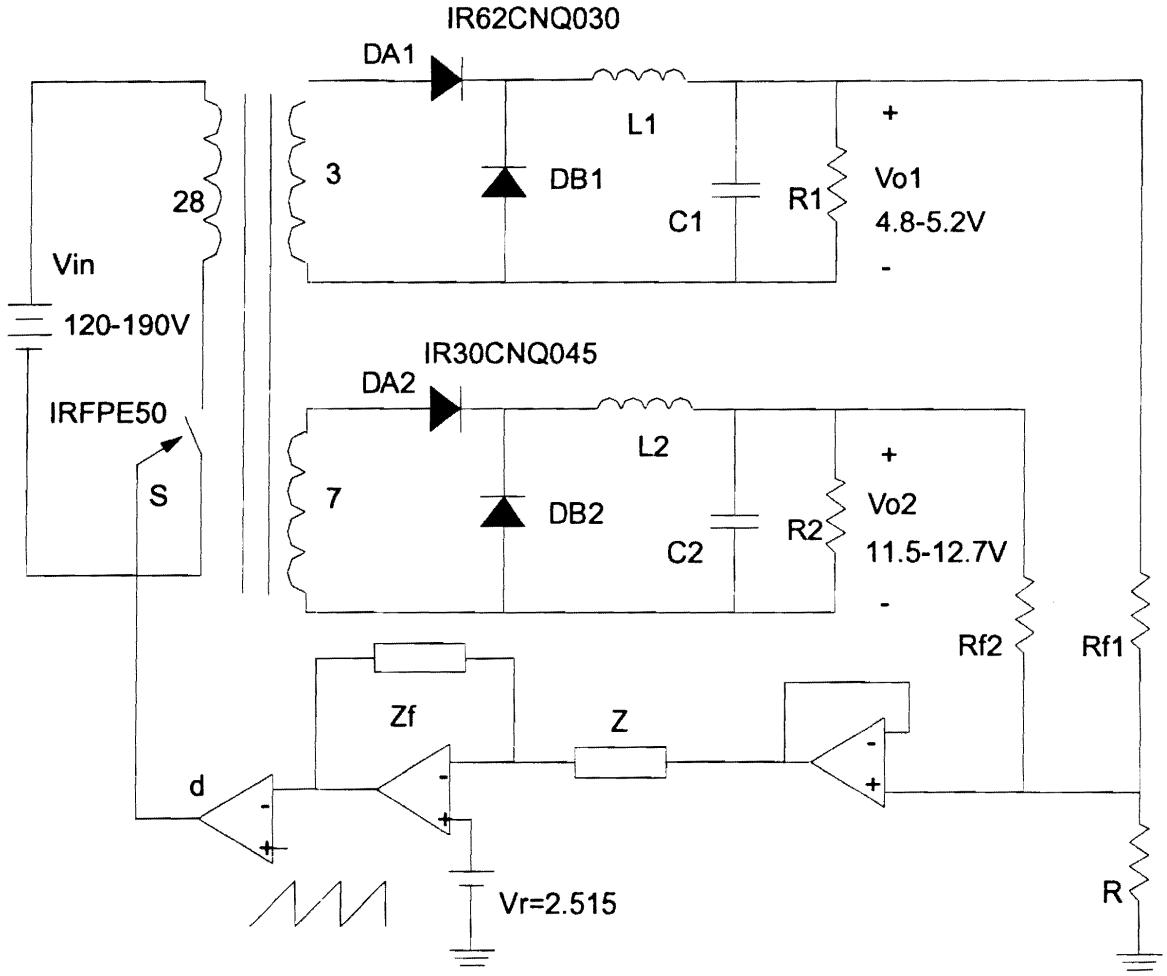


Fig. 2.10. Circuit diagram of the experimental dual-output converter. The rectifier diodes in each power channel are in the same package, which results in the identical characteristics for the diodes.

Table 2.1 The list of the circuit parameters.

R_{ds} (Ω)	1.4	C_{ds} (pF)	350
V_{d1} (V)	0.301	R_{d1} (Ω)	0.008
V_{d2} (V)	0.402	R_{d2} (Ω)	0.015
L_1 (μH)	72	R_{L1} (Ω)	0.023
L_2 (μH)	424	R_{L2} (Ω)	0.076
L_{s1} (nH)	77.1	L_{s2} (nH)	153
R_{pdc} (Ω)	0.079	R_{s1dc} (Ω)	0.002
R_{s2dc} (Ω)	0.011	V_r (V)	2.515

secondary sides are not properly centered; (2) the internal impedances are too large and they cause excessive internal voltage drops. It is important to pinpoint the cause before starting to redesign the power stage.

In Fig. 2.11, Eqs. (2.30) - (2.32) (3 of the 4 inequalities in Eqs.(2.24) - (2.27)) define a common region for $\{K_i\}$ marked as (1), which makes the 5-V output meet the design specifications. Similarly, Eqs. (2.31) - (2.33) define another region for $\{K_i\}$, which makes the 12 V output meet the design specifications. Let us assume that the 5-V power channel is more critical and its design is not going to be changed. If a set of $\{K_i\}$ is chosen such that the 5-V output just meets the regulation requirement while the 12-V output has the minimum regulation error, then the cross section of Eqs. (2.31) and (2.32), which is point A as shown in Fig. 2.11, defines such $\{K_i\}$, where K_1=0.237 and K_2=0.104. Using this set of $\{K_i\}$, the calculated V_{o1} just falls into the design specifications, whereas the calculated V_{o2} falls outside the design specifications. Figure 2.12 shows the variation of the output voltages. One can easily identify if improper centering or large internal impedance causes unsatisfactory dc regulation. For this specific design, it is obvious what the problem is -- the improper voltage centering. The difference between the maximum and minimum output voltages is within the specified values. The 12-V output needs to be downshifted.

There are several possible ways to center the secondary voltages. In this work, an autotransformer with a turns ratio of 40/41 is inserted between the secondary winding and the rectifiers in 12-V output as shown in Fig. 2.13, thereby changing the effective turns ratio of 12 V output from 0.156 to 0.152. Applying Eqs. (2.24) - (2.27) again, after this

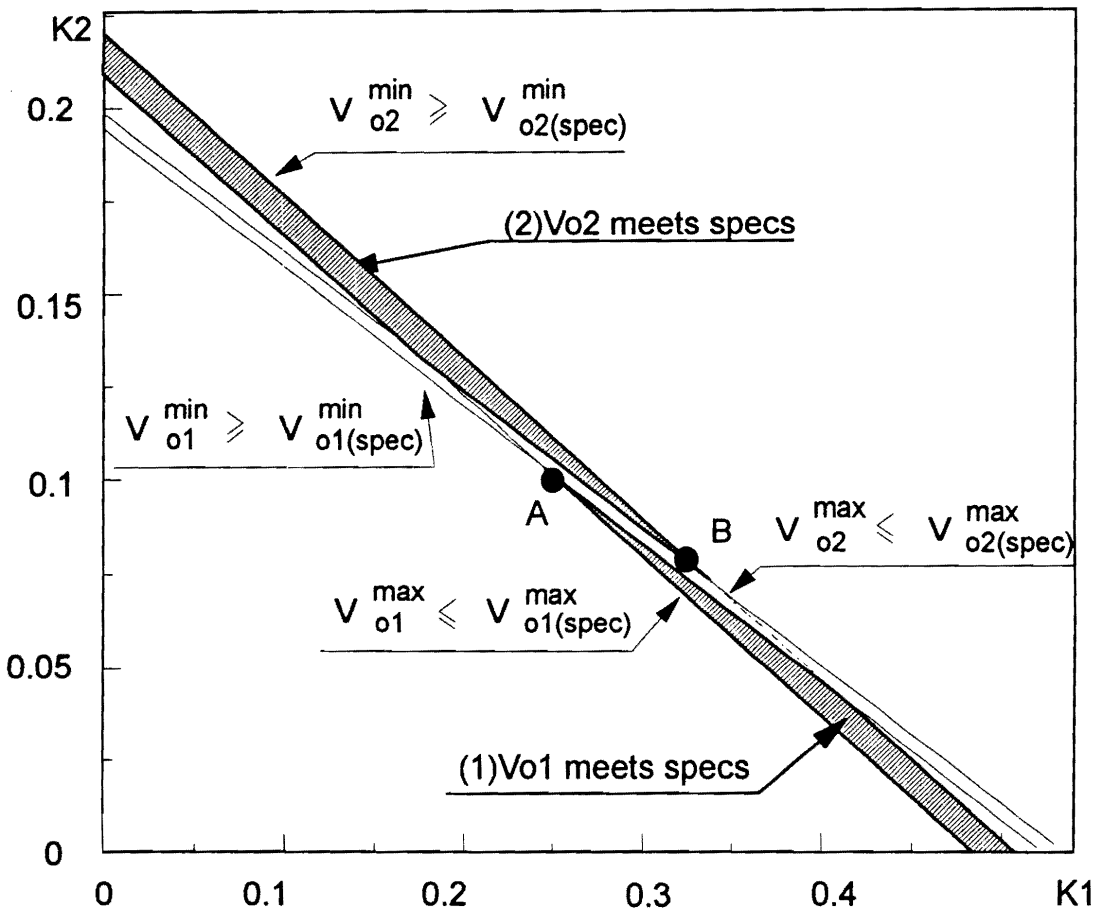
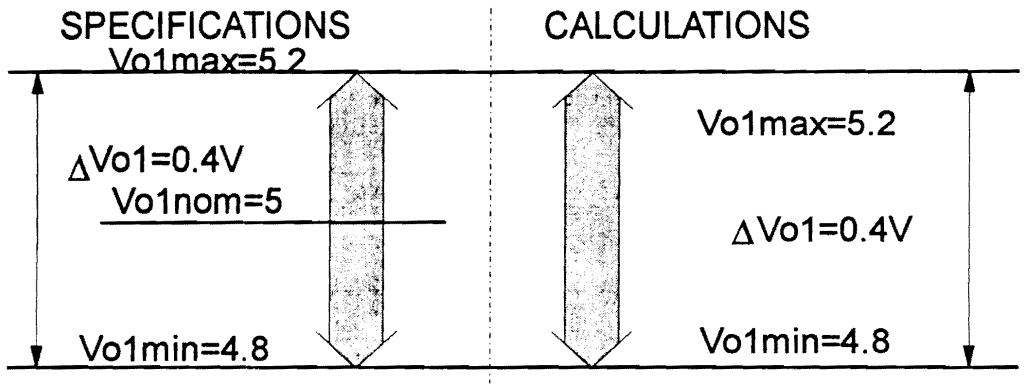
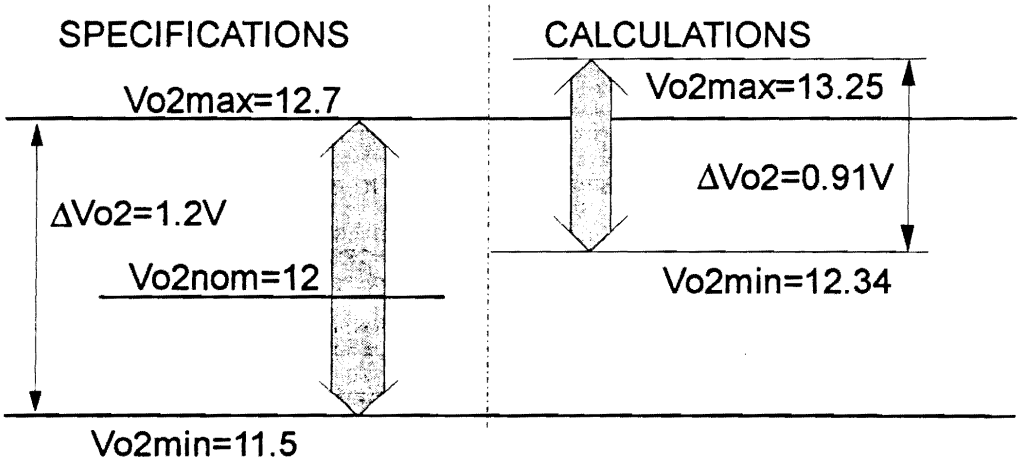


*Fig. 2.11. **The first design attempt.** Four inequalities do not specify a common region in K_1 - K_2 plane. It is necessary either to redesign the power stage, or to respecify the dc regulation.*



(a) Voltage variation diagram for Vo1



(b) Voltage variation diagram for Vo2

Fig. 2.12. Voltage variation diagram. *The variations of both outputs are within the design specifications, but the 12 V output is off the center.*

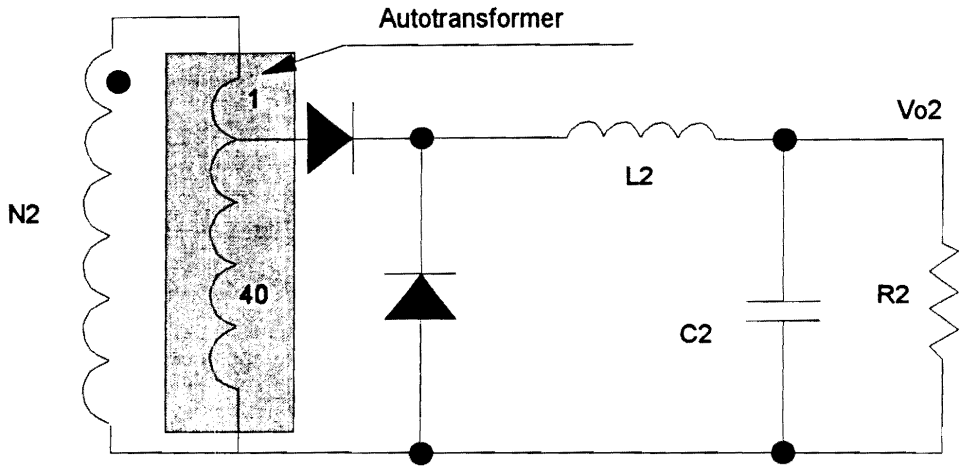


Fig. 2.13. 12-V secondary with an autotransformer. The autotransformer behaves like a lossless voltage divider.

modification, another set of inequalities are obtained:

$$5.2K_1 + 11.73K_2 \geq 2.515, \tag{2.34}$$

$$4.8K_1 + 12.59K_2 \leq 2.515, \tag{2.35}$$

$$4.848K_1 + 12.7K_2 \geq 2.515, \tag{2.36}$$

$$5.233K_1 + 11.5K_2 \leq 2.515. \tag{2.37}$$

These four inequalities do specify a common region in the first quadrant, as shown in Fig. 2.14.

Theoretically speaking, any set of the weighting factors $\{K_i\}$ chosen from the inside of the shadowed area in Fig. 2.14 should meet the design regulation specifications. If the $\{K_i\}$ are chosen near the edges of the area, however, the output voltages may be easily out of the specifications, because there are other secondary factors not included in the model, such as the effects of the output current ripples on the output voltages. Besides, the component values may deviate from the nominal ones somehow, which may be caused, for instance, by the variation of temperature. Therefore, it is preferable to choose $\{K_i\}$ in the middle of the area to provide certain design margin. In this design, the weighting factors are chosen at point P, which gives K_1=0.278 and K_2=0.093, the ratio of K_1/K_2=3. If R is chosen as 1 kΩ, the feedback network is calculated as R_{f1}=2.263 kΩ and R_{f2}= 6.763 kΩ. With these values, each output should meet its regulation specifications. Figure. 2.15 shows the measured and calculated output voltages, and there is a good agreement between the two. Both outputs are within the specifications.

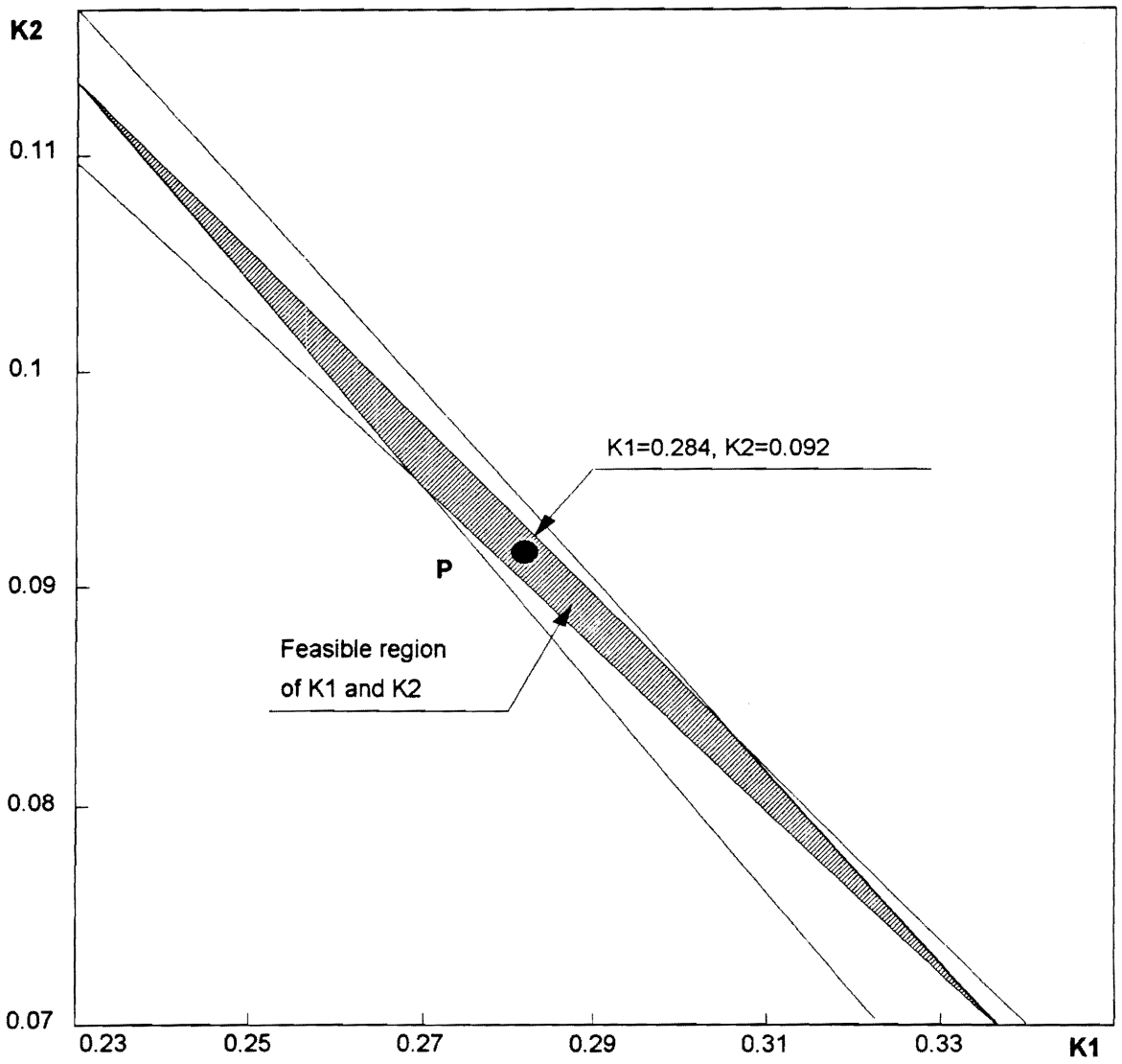


Fig. 2.14. The feasible region for the weighting factors $\{K_i\}$. After an autotransformer is used, the secondary voltage of the 12 V output is downshift. As a result, a feasible region for the weighting factors is found.

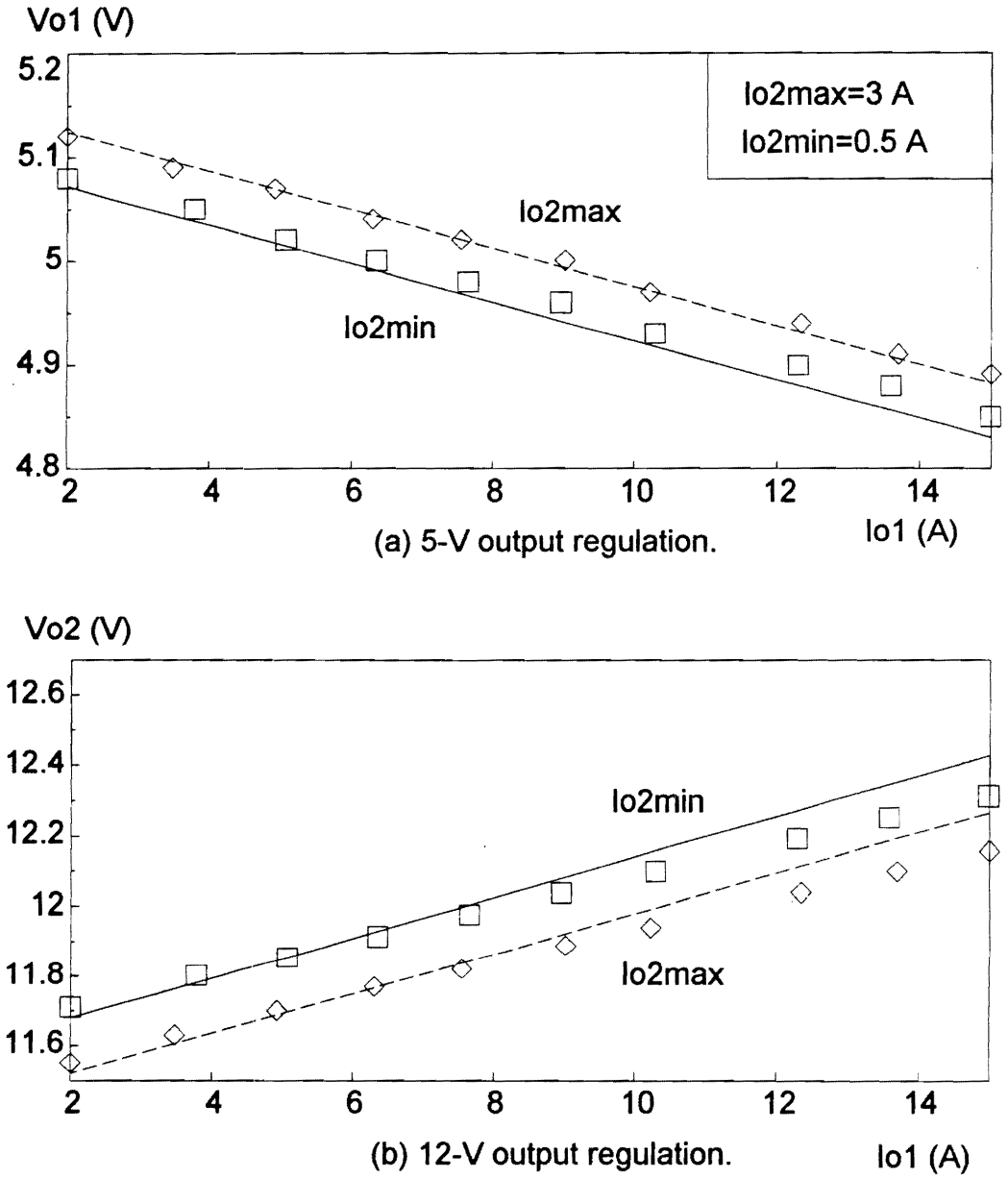


Fig. 2.15. The calculation and measurement of the output voltages. *The worst dc regulations occur at extreme operation conditions, i.e., the light and heavy load combinations.*

2.5 Generalization of the Design Method

The method for designing weighted-voltage control for multiple output converters as presented in Sec. 2.4 is conceptually simple and straightforward, providing good design insight. However, it is limited to the converters with two outputs, since 3-D pictures are usually difficult to visualize. The calculation is cumbersome, and the process is not automated; thus, it is hard to achieve optimum design. In this section, the design method is generalized based on nonlinear programming technique. Since the design is a process of searching for the minimum of a pre-defined objective function under the constraints specified by the design specifications, the final result is "optimal" among all possible solutions. As a result, an optimization design tool is developed, which can be easily applied to the converters with any number of outputs. The program is written using Matlab which has built-in optimization routine and good graphics capability.

2.5.1 Basic Concept of Nonlinear Programming

The general mathematical programming problem can be stated as

$$\text{minimize} \qquad f(x) \tag{2.38}$$

$$\text{subject to} \qquad h_i(x) = 0, \quad i = 1, 2, \ldots, m \tag{2.39}$$

$$g_j(x) \le 0, \quad j = 1, 2, \ldots, r \tag{2.40}$$

$$x \in S$$

where

$f(x)$ - objective function,

x - an n-dimensional vector of design parameters,

$h_i(x)$ - equality constraints,

$g_j(x)$ - inequality constraints,

S - a subset of n-dimensional space.

Traditionally, the constrained nonlinear programming problems are translated into a basic unconstrained problem by using a penalty function for constraints. In this way, the constrained problem is solved by using a sequence of parameterized unconstrained optimizations, which in the limit converge to the constrained problem. The augmented Lagrangian method is one of the popular algorithms and has been used for optimum design in power electronics [J1 - J3]. However, these methods are now considered relatively inefficient and have been replaced by other methods, such as Sequential Quadratic Programming (SQP) method [J4]. Later on the SQP method will be used to help solve the multiple-output converter design problem.

2.5.2 Formation of the Problem

This section demonstrates how to formulate the optimization problem through a dual-output converter.

In Section 2.2, the output voltages are expressed analytically, in terms of the power stage parameters, as:

$$V_{o1} = \frac{V_r + K_1 V_{B1} + K_2 V_{B2}}{K_1 V_{A1} + K_2 V_{A2}} V_{A1} - V_{B1}, \tag{2.41}$$

and

$$V_{o2} = \frac{V_r + K_1 V_{B1} + K_2 V_{B2}}{K_1 V_{A1} + K_2 V_{A2}} V_{A2} - V_{B2}, \tag{2.42}$$

where V_{Ai} and V_{Bi} are given in Eqs. (2.10 - 2.11). Once the power stage is designed, the output voltage variations are only the functions of the weighting factors. The design goal is to find the proper weighting factors such that the output voltages are within the design specifications. There can be numerous solutions for the feasible weighting factors. Our design should not only guarantee the output voltages inside the design specifications, but also minimize the variation of the output voltages. Let us construct an object function, which is the weighted sum of the squared errors between each output and its nominal value:

$$F(K_1,K_2)=\sum_{i=1}^{2}W_i(V_{oi(spec)}^{nom}-V_{oi}^{min})^2+\sum_{i=1}^{2}W_i(V_{oi(spec)}^{nom}-V_{oi}^{max})^2, \tag{2.43}$$

where W_i's are the weights assigned to the outputs according to their "importance". If one of the outputs is more important than the other, the corresponding error term in the objective function can be more heavily weighted. If V_{o1} is considered more critical than V_{o2}, for example, W_1 can be larger than W_2. If there is no priority between the outputs, all the error terms in the objective function can be equally weighted, and W_i's can take the same value, *e.g.*, $W_1 = W_2 = 1$.

The design constraints can be stated as the requirement that the output voltages should be within the design specifications, *i.e.*,

$$V_{o1}^{min} \geq V_{o1(spec)}^{min}, \tag{2.44}$$

$$V_{o1}^{max} \leq V_{o1(spec)}^{max}, \tag{2.45}$$

$$V_{o2}^{min} \geq V_{o2(spec)}^{min}, \tag{2.46}$$

$$V_{o2}^{max} \leq V_{o2(spec)}^{max}. \tag{2.47}$$

In addition, the feedback signal, which is the sum of the weighted output voltages, should be equal to the reference voltage, or

$$V_r = \sum_{i=1}^{2}K_iV_{oi}. \tag{2.48}$$

Now the multiple-output converter design problem is converted to an optimization

problem. The constructed objective function will force the output voltages to be centered around the nominal output voltages. The constraints tend to confine the output voltage variations inside the design specifications. It should be noted that if the output voltage specifications are very tight, the optimization process may not find feasible solution for the weighting factors $\{K_i\}$. In this case, the power stage has to be redesigned, or dc regulation specifications have to be relaxed.

2.5.3 Optimization Design Tool

The advantages of using the optimization tool are that the selection of the weighting factors can be automated, and the process can be easily extended to the converter with any number of outputs. The whole process is coded into a program which is based on Matlab. Figure 2.16 shows the flow chart of the program. The source code is in Appendix A.

The basic function of the program is to search for the feasible weighting factors $\{K_i\}$. This search process is based on the power stage parameters and the load ranges and output cross-regulation specifications. If a feasible solution for $\{K_i\}$ is found, the design is finished, and the result is optimal in the sense that the differences between the output voltages and the nominal values are minimal. In reality, however, it is rarely the case that the first-round design can meet the design specifications. Very often, it may not find a feasible solution for $\{K_i\}$ after invoking QSP routine. Therefore, the program provides an option to modify the power stage design. In addition to the power stage parameters obtained from the preliminary

design, the lower boundaries of these parameters are also part of the inputs to the program. The parameter boundaries are usually dominated by other design considerations, such as cost and availability. For instance, the 5-V secondary rectifier diodes can use either IR62CNQ030 or IR20CTQ035. The voltage ratings for both diodes are adequate to meet the whole line and load range variations. From cross-regulation point of view, the IR62CNQ030 is more favorable, since its ac resistance, which characterizes the variant part of the forward voltage drop of the diode, is only 0.008 Ω, while the IR20CTQ035 has a resistance of 0.022 Ω. As for the cost, however, the IR20CTQ035 is more desirable, since its price is approximately a quarter of that of IR62CNQ030. The similar trade-off can be made for other components. If a designed component is not allowed to change, then the lower boundary for the component parameter can be simply set equal to the preliminary design. The program will automatically sweep the value of each parameter till a feasible solution for $\{K_i\}$ is found. Once the searching process is completed, the final results, including the weighting factors and the modified power stage parameters, are stored in an output file. The dc cross-regulation characteristics are also plotted for all the outputs. The design example given in Section 2.4 is used here again to demonstrate the optimization design tool.

Substituting all the circuit parameters given in Table 2.1 into the program, the program calculates the coefficient of the output voltages. The calculated results are used to form the objective function and the constraints. By invoking the SQP routine provided by Matlab, the weighting factors are obtained as follows:

$$K_1 = 0.279, \quad K_2 = 0.093. \tag{2.49}$$

The corresponding objective function is

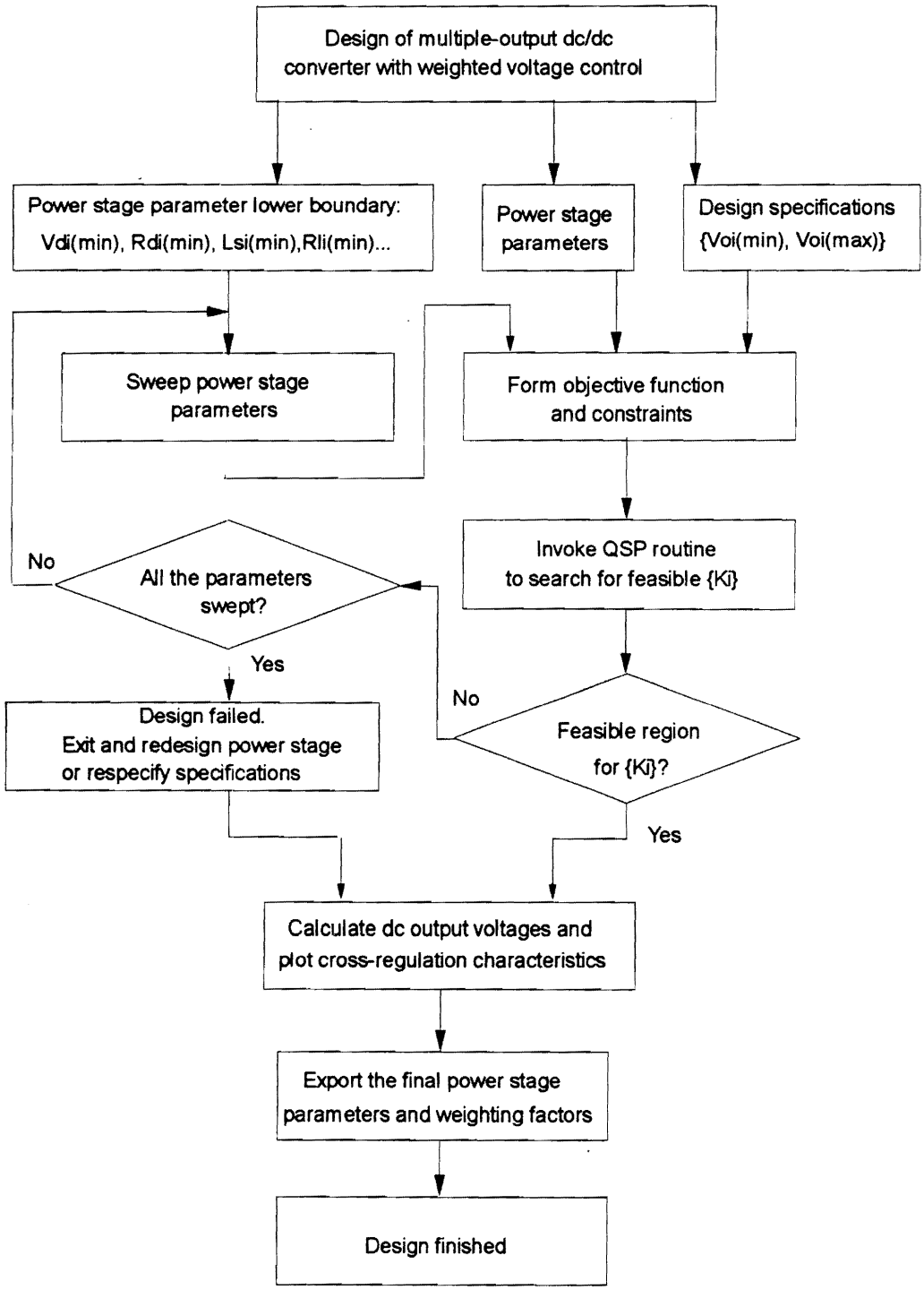


Fig. 2.16. Flow chart of the optimization-based design tool. *The design tool performs (1) searching for feasible $\{K_i\}$, (2) sweeping the power stage parameters, and (3) calculating cross-regulation characteristics.*

$$F=0.4512 \tag{2.50}$$

Compared with the results given in Sec. 2.4:

$$K_1 = 0.284, \quad K_2 = 0.092, \tag{2.51}$$

the objective function has a value of

$$F=0.4567. \tag{2.52}$$

The good matching between the two results is due to the fact that the weighting factors were already selected from the middle of the feasible region, which should be close to the optimized values obtained from the design tool.

This example shows that with the optimization design tool, it is possible to force the output voltages around their nominal values, and the overall voltage excursions will be minimized.

Another example given here is a triple-output converter. The design and regulation specifications are

- input line voltage V_{in}, $120\ V$ - $190\ V$,
- 3.3 V output: $3.1V \le V_{o1} \le 3.5V$, $2A \le I_{o1} \le 12A$,
- 5 V output: $4.7V \le V_{o2} \le 5.3V$, $2A \le I_{o1} \le 12A$,
- 12 V output: $11.5V \le V_{o3} \le 12.7V$, $0.5A \le I_{o3} \le 3A$.

The power stage parameters, as summarized in Table 2.4, are used as the input to

Table 2.4 Circuit parameters of the triple-output converter.

R_{ds} (Ω)	1.4	C_{ds} (pF)	250
V_{d1} (V)	0.301	R_{d1} (Ω)	0.008
V_{d2} (V)	0.301	R_{d2} (Ω)	0.008
V_{d3} (V)	0.402	R_{d3} (Ω)	0.015
L_1 (μH)	31.96	R_{L1} (Ω)	0.0093
L_2 (μH)	71.7	R_{L2} (Ω)	0.023
L_3 (μH)	423.7	R_{L3} (Ω)	0.0769
L_{s1} (nH)	52.9	L_{s2} (nH)	77.13
L_{s3} (nH)	153	R_{pdc} (Ω)	0.079
R_{s1dc} (Ω)	0.002	R_{s2dc} (Ω)	0.0025
R_{s3dc} (Ω)	0.011		

the design tool. After executing the program, the weighting factors are found as:

$$K_1 = 0.122, \quad K_2 = 0.167, \quad K_3 = 0.106. \tag{2.53}$$

For the 3-output converter, the worst regulations occur when one output is operating at light (or heavy) load, while the other two outputs are operating at heavy (or light) loads. The experimental results and calculations are given in Fig.2.17.

For general nonlinear programming problems, the optimization results can be very sensitive to the initial guess for the variables $[x_1, x_2, \ldots x_n]^T$ when there exists more than one local minimum. Since there is no guarantee that the obtained solution is the global minimum, different initial values have to be tested. Fortunately, for the cross-regulation problem studied here, the objective function defined in Eq. (2.43) is well behaved. It can be seen from the mesh surface plot of the objective function in Fig. 2.18, that the objective function has only one minimum, which is of course the global minimum. One does not have to go through many iterations. A good starting point can be decided by assuming that all the outputs are equally weighted, *i.e.*,

$$K_1 V_{o1} = K_2 V_{o2} = \cdots = K_n V_{on} = \frac{V_r}{n}. \tag{2.54}$$

Different initial values were tested for the above two problems, and they all yielded the same results.

Actually, Fig. 2.18 also demonstrates how the optimization process works. If a set initial value of $\{K_i\}$ is chosen at point A, which is obviously away from the solution, the value of the corresponding objective function is large. The optimization routine will move

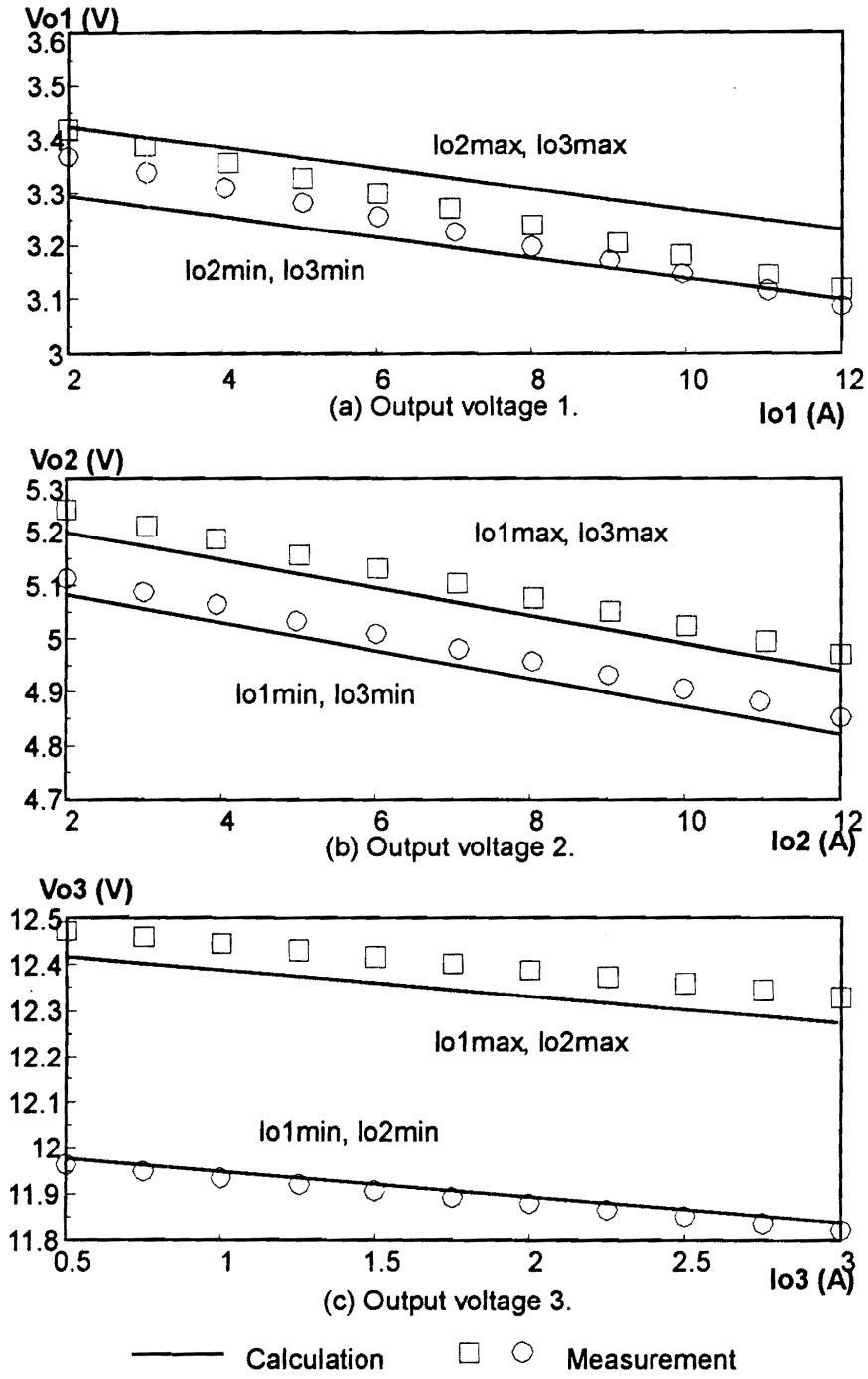


Fig. 2.17. The calculation and measurement of the output voltages for the 3-output converter. *The worst regulations occur when one output is operating at one extreme, i.e., light load (or heavy load), whereas the other outputs are operating at another extreme, i.e., heavy load (or light load).*

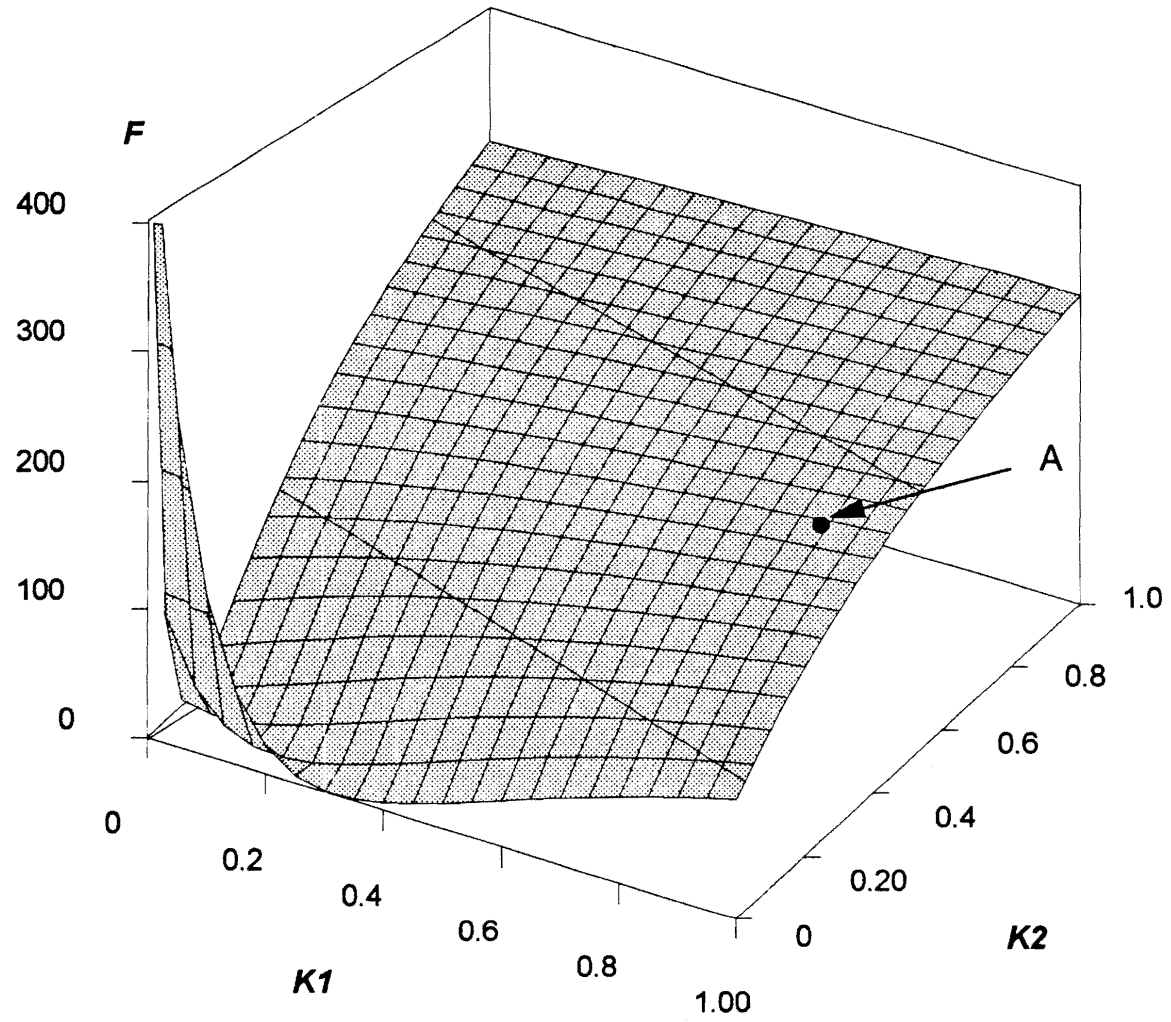


Fig. 2.18. 3-D mesh surface plot of the objective function. *The objective function is well behaved as the weighting factors $\{K_i\}$ vary. There is no local minimum, and hence the optimum solution, if there is one, is the global minimum.*

$\{K_i\}$ towards the "valley". On the way to the valley, the value of the objective function is becoming smaller and smaller, till the weighting factors $\{K_i\}$ are moved to the bottom of the 3-D surface, where the optimal weighting factors $\{K_i\}$ are obtained.

In the design tool, the leakage inductances of the transformer is lumped on the secondaries. Using this model, the secondaries are decoupled from each other. Nevertheless, this model does not account for the interactions among the secondaries. If the effects of the leakage inductances are comparable with those of other parasitics, this model may not be adequate to describe the effects of the leakage inductances. Therefore, a better model is needed to describe the characteristics of the transformer. In Appendix C, a new multiple-winding transformer model is presented. This model features that the each model parameter is corresponding to a magnetic flux, and has specific physical meaning. The model takes more complex form, and therefore is hard to use for analytical derivation. Nevertheless, the model can be used for numerical simulation to verify the design results.

2.6 Summary

A dc model incorporating all major parasitics is derived for a forward dc-dc converter with multiple outputs. The model reveals that dc regulation depends, to a large extent, on the internal impedance which is the sum of the equivalent resistance of the rectifier diodes, the winding resistance of the output filter inductor, and the product of the

leakage inductance and the switching frequency in each output. In addition, the winding resistances of the transformer, the parasitic output capacitance, and the on-resistance of the active switch also affect the dc output voltage. The parasitics affect the output voltages in different ways. The resistances cause internal voltage drops, while the parasitic capacitance and the leakage inductance cause some modification of the effective duty cycle on the secondary side of the transformer. To improve the dc regulation, it is important to decrease the internal impedance for each output. In addition to the internal impedances, correct centering is also crucial for achieving good regulation.

The closed-loop output voltages are decided by the weighting factors in addition to the power stage parameters. By applying the dc regulation specifications, a set of inequalities is obtained, which specify the region for $\{K_i\}$. For some cases, it is possible to find a set $\{K_i\}$, which will achieve the desired dc regulation for all outputs. For other cases, the required regulation may not be met by simply choosing $\{K_i\}$. Either relaxation of the design specifications or redesign of the power stage may have to be required.

A nonlinear-programming based optimization design tool is developed for designing multiple-output converters with weighted voltage control. The objective function is defined as the weighted sum of the squared errors between each output voltage and its nominal value, with the dc cross-regulation specifications as the constraints. The obtained weighting factors $\{K_i\}$ are optimal in the sense that the output voltages have minimal errors. Since the so-defined objective function is well behaved, the solution is not sensitive to the initial condition, an often-encountered problem when nonlinear programming is used. The feasible solution for the weighting factors $\{K_i\}$, if there is one, should be the global minimum.

3. Improvement of DC Cross-Regulation by Stacking Secondaries

3.1 Introduction

As discussed in the last chapter, inability to meet dc regulation results from two sources: improper centering and internal voltage drops due to the secondary parasitic inductances and resistances. The centering problem can be solved by using an autotransformer or a fractional number of turns [H4]. Due to using weighted voltage control (WVC), the dc regulations vary according to the values of the weighting factors. Nevertheless, WVC does not reduce the total error. In essence, WVC only redistributes the error among the outputs rather than reducing voltage variation range. Any improvement of dc regulation for one output occurs at the cost of the other outputs. The deviation of each output from its desired value depends on how much it is weighted in the

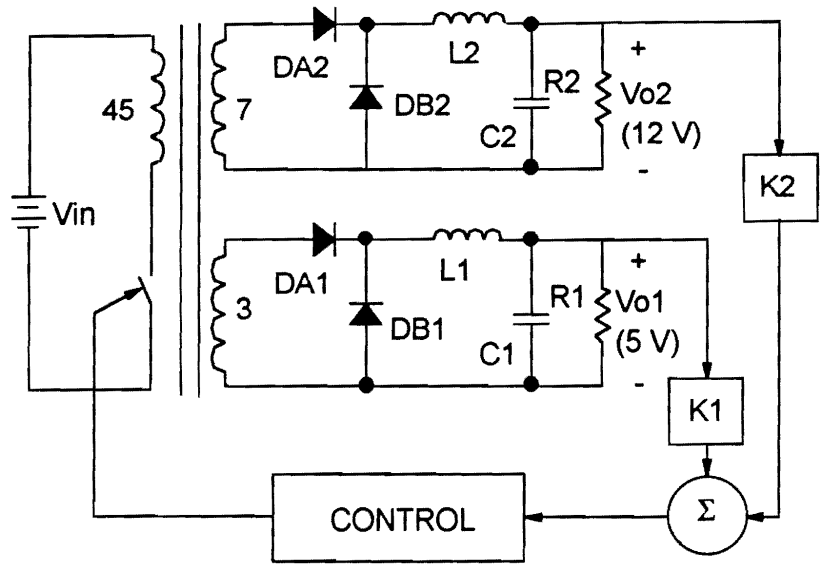
feedback signal. Since there is little coupling between the outputs, there is virtually no tracking between the outputs, as either of the load currents varies. As a result, the output voltages vary over a wide range. Stacking secondaries, Fig. 3.1, can effectively reduce the voltage variation range and help to correctly center the secondary voltages [C3].

In this chapter, various stacking schemes are analyzed, and their dc cross-regulation improvements are quantified. The analytical expressions of the output voltages for the stacking schemes are derived, incorporating major parasitics, such as leakage inductances, forward voltage drops of the rectifier diodes, and the winding resistances of the transformer and the output filter inductors. The advantages and disadvantages of each stacking scheme in terms of quality of dc cross-regulation, current stress, and internal power losses are evaluated, helping to achieve the optimum design.

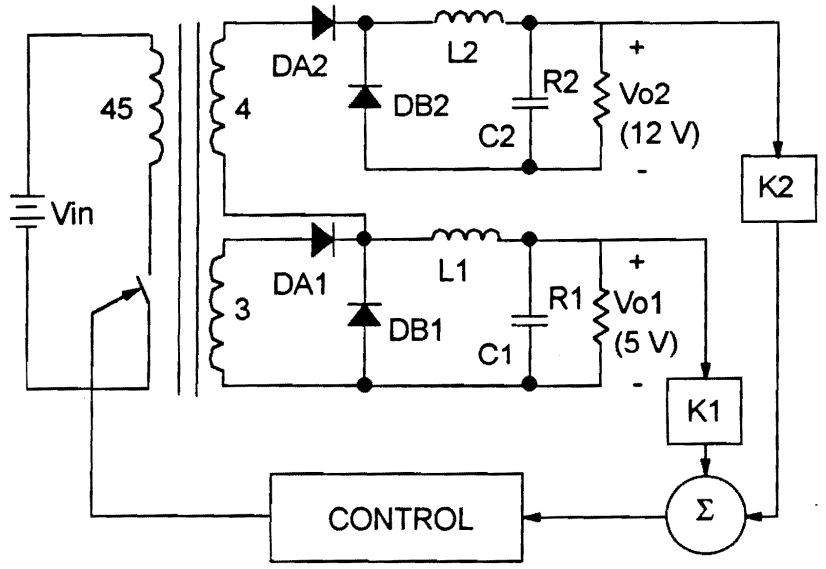
3.2 Analysis of the Multiple-Output Converter with Stacked Secondaries

In this section, the dual-output converter given in Section 2.4 is used as an example to illustrate the effectiveness of stacking secondaries in improving dc cross-regulation. The effects of stacking secondaries are quantified analytically.

Figure 3.1 shows the circuit of the multiple-output converter with and without



(a)



(b)

Fig. 3.1. ***Two power stage configurations:*** *(a) non-stacked secondaries; (b) stacked secondaries. By stacking the secondaries of the power channels, a cross-talk is introduced between the power channels, and they can track each other better as any load varies.*

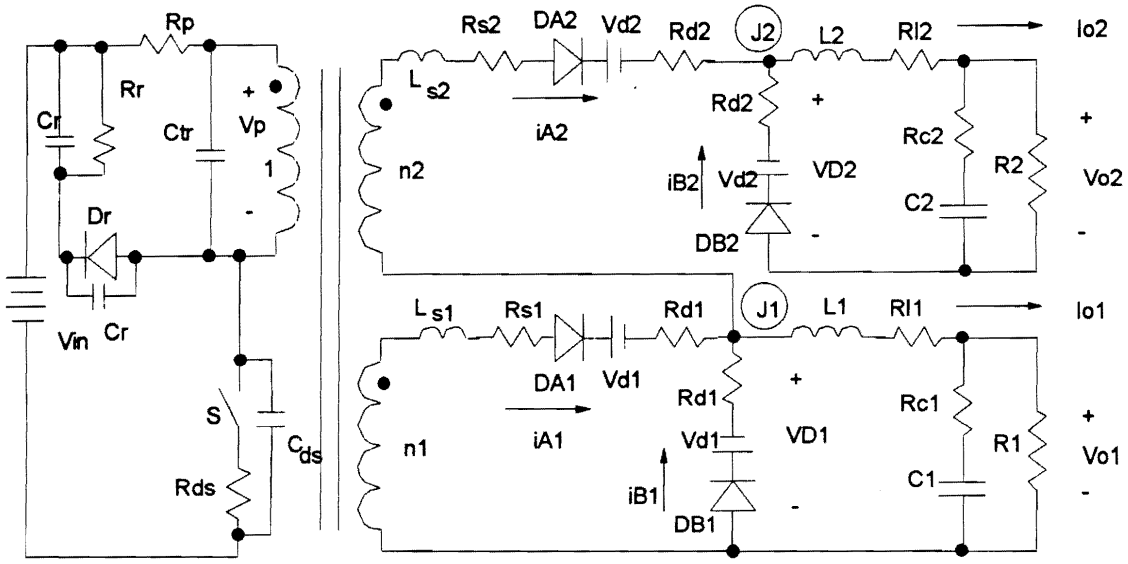


Fig. 3.2. Equivalent circuit model of the multiple-output converter with stacked secondaries. *Compared with the circuit model given in Fig. 2.2, it can be seen that the only difference is that the 12-V output current also flows through the 5-V output transformer winding and the forward diode* D_{A1}.

stacked secondaries. The power stage dc model, shown in Fig.3.2, is obtained by substituting each component with its corresponding circuit model as done in Section 2.2. The same major parasitics are included in the following analysis.

The primary side of the circuit is treated in the same way as in Section 2.2. The major parasitic affecting the primary circuit is the junction capacitance of the active switch, which yields an effective duty cycle extension, as given in Eqs. (2.4) and (2.5). As for the secondary circuits, the same parasitics affect the circuit operation differently, compared with the analysis performed in Section 2.2. The detailed analysis follows.

Every secondary of the transformer can be modeled by a voltage source with magnitude equal to the reflected primary voltage and effective duty cycle, D_e. To simplify the analysis, the current flowing through each inductor is assumed to be constant. The waveforms over a complete switching period are shown in Fig. 3.3. The procedure to derive the output voltages is to find the voltages across the freewheeling diodes (D_{B1} and D_{B2}), V_{J1} and V_{J2}. The output voltages are then obtained by averaging V_{J1} and V_{J2} over a switching period.

As the active switch is turned on, the voltages across the freewheeling diodes, V_{J1} and V_{J2}, cannot change instantaneously due to the leakage inductances L_{s1} and L_{s2}. The effective duty cycle losses are

$$\Delta D_1 = \frac{I_{o1} + I_{o2}}{V_{s1}} L_{s1} f_s, \tag{3.1}$$

and

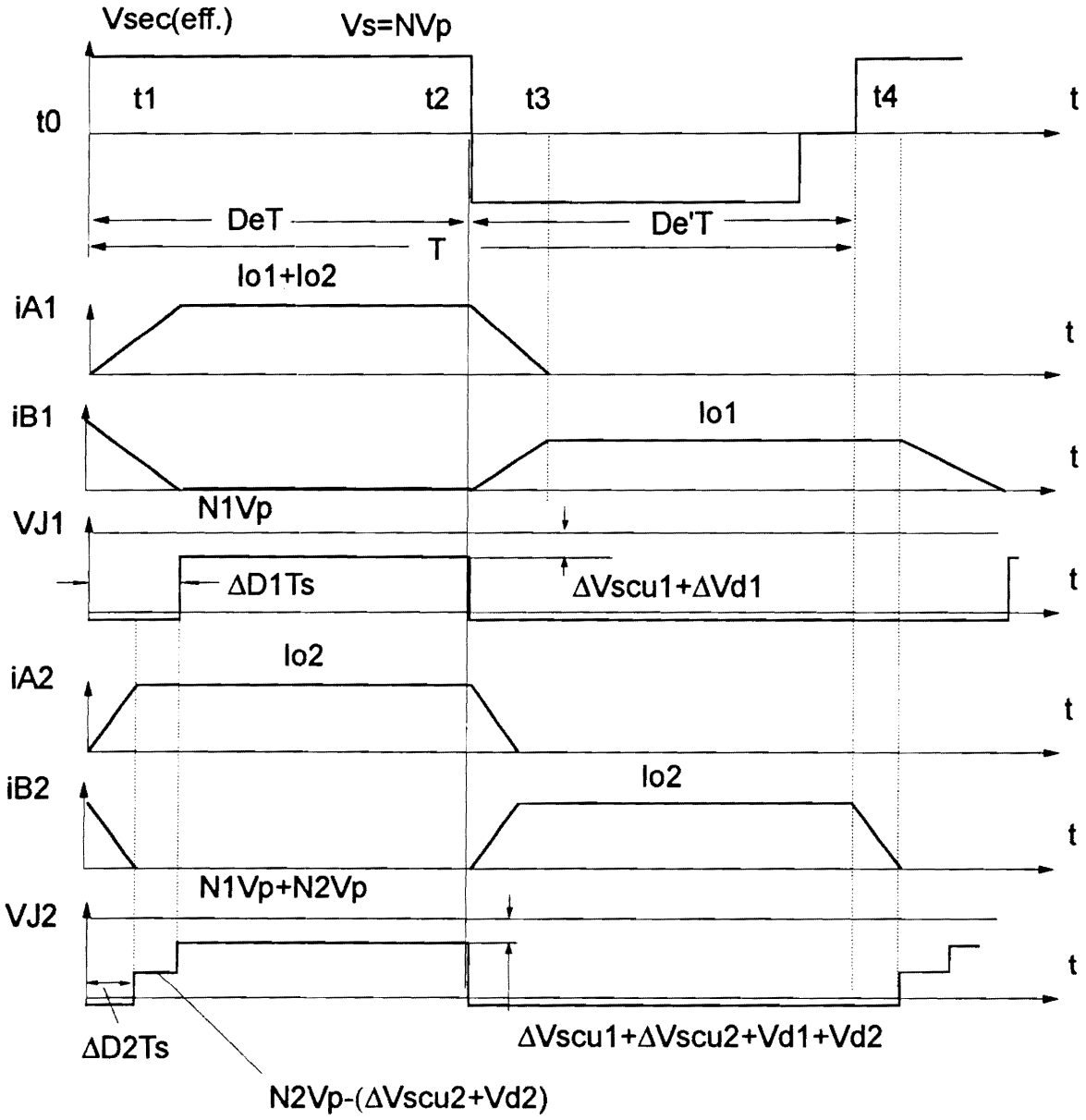


*Fig. 3.3. **Waveforms in a complete switching period for stacked secondaries.** Compared with the non-stacked secondaries in Section 2.2, it can be seen that the 12 V channel V_{J2} is changed.*

$$\Delta D_2 = \frac{I_{o2}}{V_{s2}} L_{s2} f_s. \tag{3.2}$$

After the leakage inductances are charged to their corresponding load currents, V_{J1} and V_{J2} become

$$V_{J1}=V_{s1}-(I_{o1}+I_{o2})(R_{s1}+R_{d1})-V_{d1}, \tag{3.3}$$

and

$$V_{J2}=V_{s1}+V_{s2}-(I_{o1}+I_{o2})(R_{s1}+R_{d1})-V_{d1}-V_{d2}-I_{o2}(R_{s2}+R_{d2}). \tag{3.4}$$

Averaging voltages V_{J1} and V_{J2} yields the output voltages:

$$\begin{aligned} V_{o1} = {} & [V_{s1} - (I_{o1} + I_{o2})(R_{s1} + R_{d1}) - V_{d1}](D_e - \Delta D_1) \\ & - (V_{d1} + I_{o1} R_{d1})(1 - D_e + \Delta D_1) - R_{L1} I_{o1}, \end{aligned} \tag{3.5}$$

and

$$\begin{aligned} V_{o2} = {} & [V_{s2} - V_{d1} - V_{d2} - I_{o1} R_{d1} - I_{o2}(R_{s2} + R_{d2})](\Delta D_1 - \Delta D_2) \\ & + [V_{s1} + V_{s2} - V_{d1} - V_{d2} - (I_{o1} + I_{o2})(R_{s1} + R_{d1}) - I_{o2}(R_{s2} \\ & + R_{d2})](D_e - \Delta D_1) - (V_{d2} + I_{o2} R_{d2})(1 - D_e + \Delta D_2) - I_{o2} R_{L2}. \end{aligned} \tag{3.6}$$

By neglecting the 2nd order terms, the output voltages become

$$\begin{aligned} V_{o1} \approx {} & [V_{s1} - (I_{o1} R_{s1} + I_{o2}(R_{s1} + R_{d1})] D_e \\ & - [V_{d1} + I_{o1}(L_{s1} f_s + R_{d1} + R_{L1}) + I_{o2} L_{s1} f_s], \end{aligned} \tag{3.7}$$

or

$$V_{o1} \approx V_{s1}D_e - V_{d1} - I_{o1}Z_{11} - I_{o2}Z_{12}, \tag{3.8}$$

and

$$\begin{aligned} V_{o2} \approx & [V_{s1} + V_{s2} - V_{d1} - I_{o1}(R_{s1} + R_{d1}) - I_{o2}(R_{s1} + R_{d1} + R_{s2})]D_e \\ & - \{V_{d2} + I_{o1}L_{s1}f_s + I_{o2}[(L_{s1} + L_{s2})f_s + R_{d2} + R_{L2}]\}, \end{aligned} \tag{3.9}$$

or

$$V_{o2} \approx (V_{s1} + V_{s2})D_e - (V_{d1}D_e + V_{d2}) - I_{o1}Z_{21} - I_{o2}Z_{22}, \tag{3.10}$$

where the internal impedances are defined as:

$$Z_{11} = L_{s1}f_s + R_{s1}D_e + R_{d1} + R_{L1}, \tag{3.11}$$

$$Z_{12} = (R_{s1} + R_{d1})D_e + L_{s1}f_s, \tag{3.12}$$

$$Z_{21} = L_{s1}f_s + (R_{s1} + R_{d1})D_e, \text{ and} \tag{3.13}$$

$$Z_{22} = (L_{s1} + L_{s2})f_s + (R_{s1} + R_{d1} + R_{s2})D_e + R_{d2} + R_{L2}. \tag{3.14}$$

Each output voltage is dependent not only on its load current but also on the load current of the other output. This is different from the non-stacked case, where the output voltages are

$$V_{o1} = V_{s1}D_e - V_{d1} - I_{o1}(L_{s1}f_s + R_{s1}D_e + R_{d1} + R_{L1}), \tag{3.15}$$

and

$$V_{o2} = V_{s2}D_e - V_{d2} - I_{o2}(L_{s2}f_s + R_{s2}D_e + R_2 + R_{L2}). \quad (3.16)$$

For the non-stacked case, as shown in Fig. 3.1(a), there is no coupling between the outputs. If one load current increases and its output voltage drops, the feedback control will cause the duty cycle to increase. As a result, the voltage of another output will also increase, even though its load current is kept constant. On the other hand, stacking the secondaries, as shown in Fig. 3.1(b), introduces coupling between the outputs. Whenever a load current variation occurs at any output, it results in a voltage change at that output, and another output voltage changes in the same direction. Now a duty cycle change produced by the feedback control loop adjusts all the output voltages in the same direction, thereby producing smaller overall excursion of both outputs in steady state. This internal voltage compensation mechanism makes the outputs track each other. The ability of tracking between the output voltages depends on transimpedances Z_{12} and Z_{21}. The larger the transimpedances, the better the tracking between the output voltages. Figure 3.4 shows the internal voltage compensation mechanism.

Stacking secondaries not only introduces an internal voltage compensation, resulting in better voltage tracking, but it also has the function of voltage centering. By applying stacking scheme, a constant voltage drop (the constant part of the rectifier diodes, V_d) is introduced, and the stacked output voltage can be downshifted. It can be seen that all the stacking schemes presented later on introduce certain amount of constant voltage drop for the stacked output except for direct stacking of the transformer secondary windings.

Besides improving cross-regulation, stacking of secondaries makes it possible for the transformer to use fewer turns for the higher voltage output. When the 12-V

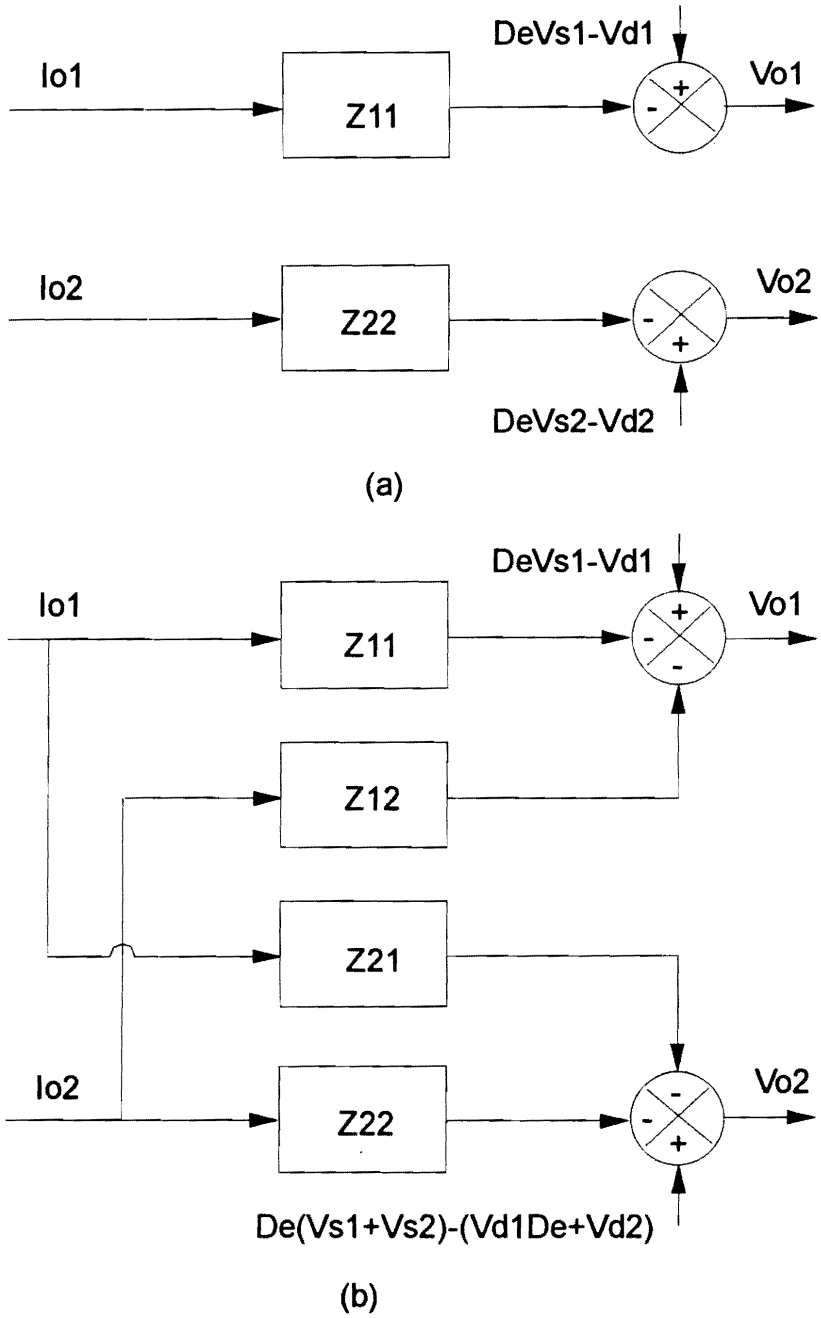


Fig. 3.4. ***Illustration of internal voltage compensation mechanism:*** *(a) non-stacked secondaries; (b) stacked secondaries. By stacking the secondaries, the output voltages can track each other as any load changes.*

secondary is stacked on the 5-V secondary, for instance, the 12-V secondary can use 4 turns instead of 7 turns before stacking. Fewer turns directly translate into less leakage inductance, and therefore the adverse effects of leakage inductance are reduced. Furthermore, fewer turns make it possible to use copper foil, and to avoid using expensive Litz wire for high- frequency applications.

The dc cross-regulation is calculated for the converter with stacked secondaries as shown in Fig. 3.5. The improvement of cross regulation is obvious.

Improvement of dc regulation for stacked secondaries is not without penalty. As can be seen from Fig. 3.1, the load current for 12-V output goes through the 5-V secondary winding and the forward rectifier diode, D_{A1}, in addition to the 12-V secondary winding and the forward rectifier diode, D_{A2}, during on-time. The power losses are obviously increased. So is the current stress on D_{A1}. These can be analytically calculated.

The primary power losses can be approximated as:

$$P_p=(N_1I_{o1}+N_2I_{o2})^2(R_{ds}+R_p)D_e, \tag{3.17}$$

where the turns ratios are

$$N_1=\frac{N_{s1}}{N_p}, N_2=\frac{N_{s2}}{N_p}. \tag{3.18}$$

The secondary losses before stacking are

$$P_1 = I_{o1}V_{d1} + I_{o1}^2(R_{L1} + R_{d1} + R_{s1}D_e), \tag{3.19}$$

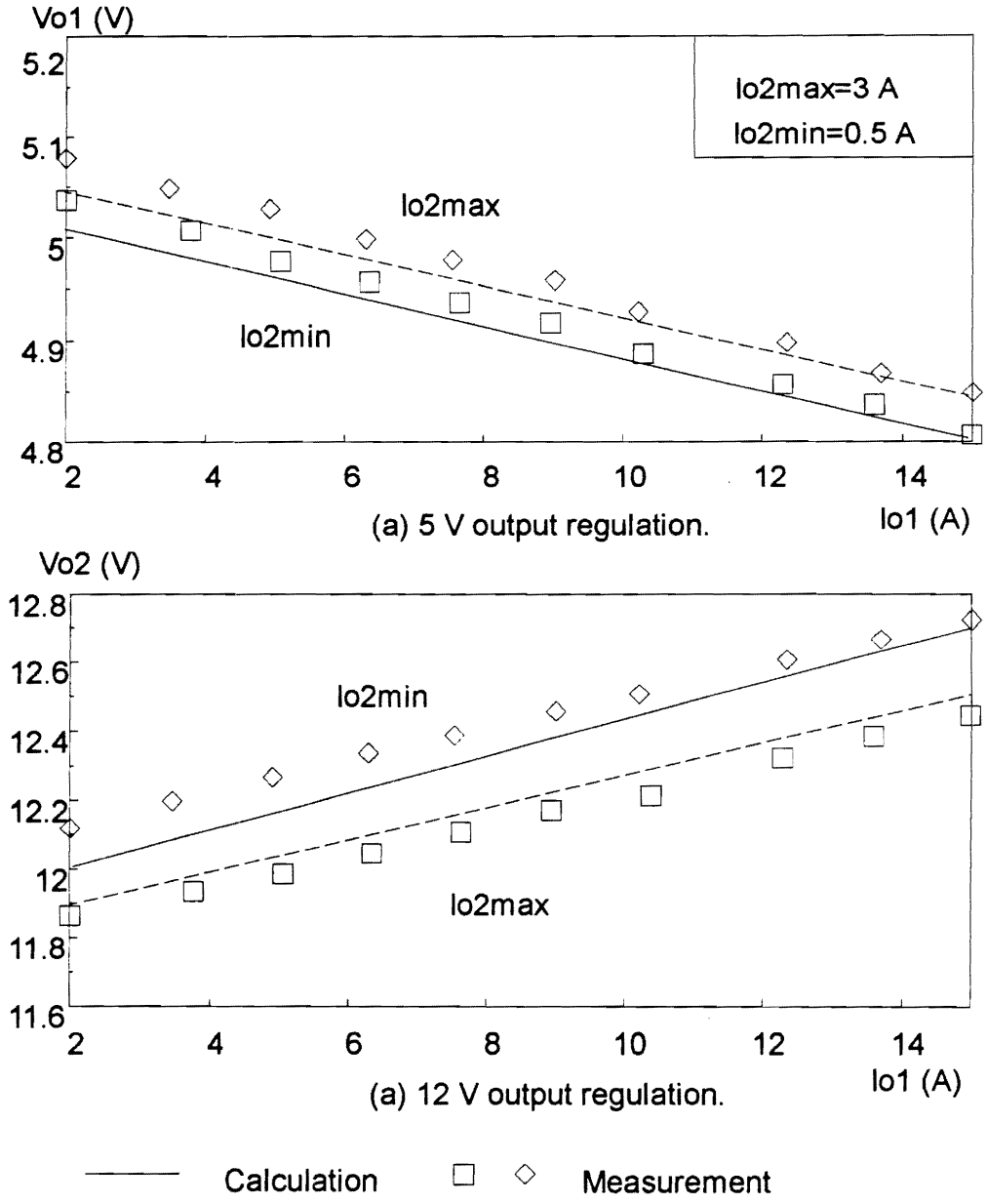


Fig. 3.5. Output voltages with stacked secondaries and WVC: *(a) 5-V output, and (b) 12-V output. By stacking 12-V secondary on 5-V secondary, the dc regulation specifications can be met without using autotransformer on 12-V secondary.*

and

$$P_2 = I_{o2}V_{d2} + I_{o2}^2(R_{L2} + R_{d2} + R_{s2}D_e). \tag{3.20}$$

After stacking the secondary of V_{o2} on the secondary of V_{o1}, the secondary losses become

$$\begin{aligned} P_1 = {} & I_{o1}V_{d1} + I_{o1}^2(R_{L1} + R_{d1} + R_{s1}D_e) && \leftarrow \textit{same as non-stacking} \\ & + I_{o2}V_{d1}D_e + (2I_{o1}I_{o2} + I_{o1}^2)(R_{d1} + R_{s1})D_e && \leftarrow \textit{increased part} \end{aligned} \tag{3.21}$$

and

$$P_2 = I_{o2}V_{d2} + I_{o2}^2(R_{L2} + R_{d2} + R_{s2}D_e). \tag{3.22}$$

Compared with Eq. (3.20), it can be seen that the expression for P_2 is the same as that before stacking, but the winding resistance, R_{s2}, is smaller. Therefore, the power loss for V_{o2} is decreased. The power losses in V_{o1} output, however, are increased by:

$$\Delta P_1 = I_{o2}V_{d1} + (2I_{o1}I_{o2} + I_{o1}^2)(R_{d1} + R_{s1})D_e. \tag{3.23}$$

If I_{o2} is small compared with I_{o1} (usually the case), the increased power losses are insignificant. The current stress of D_{A1} is increased from I_{o1} to $I_{o1}+I_{o2}$. Again, if the load current of V_{o2} is small, the current stress is increased only by a small amount.

3.3 *Various Methods of Stacking*

In the above discussion, the 12-V secondary winding is stacked at the input of the output filter of the 5-V output. However, stacking can be realized in different ways. The various stacking schemes are summarized, analyzed, and compared below.

(A) Stacking the secondary windings only (Fig. 3.6(a)).

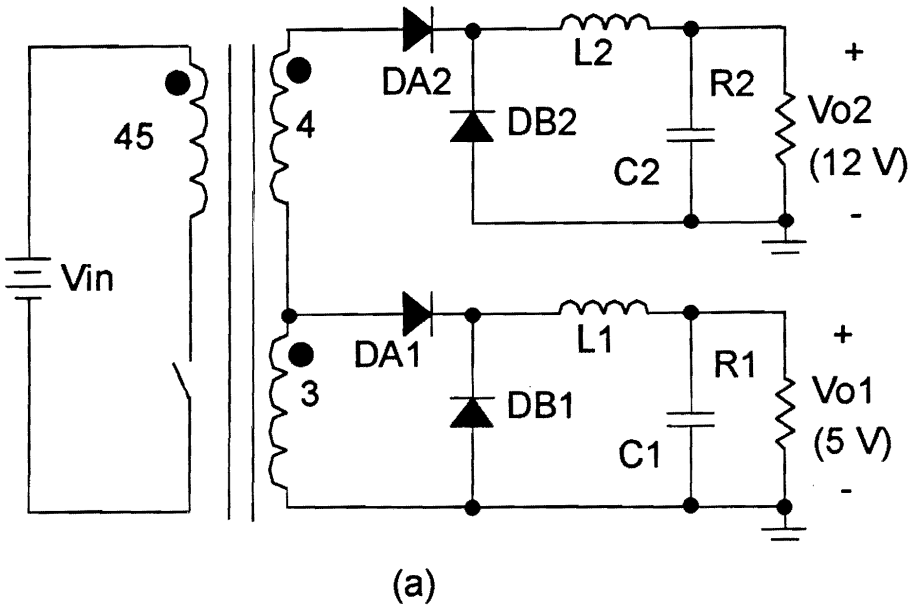
The coupling between two outputs is established only through the transformer. The transimpedances and the losses are the smallest among all the schemes. The major benefit is that the 12-V output secondary winding can use fewer turns, which results in smaller leakage inductances. The current stress for each rectifier diode is unchanged compared with the non-stacked case.

(B) Stacking the secondary freewheeling diodes (Fig. 3.6(b)).

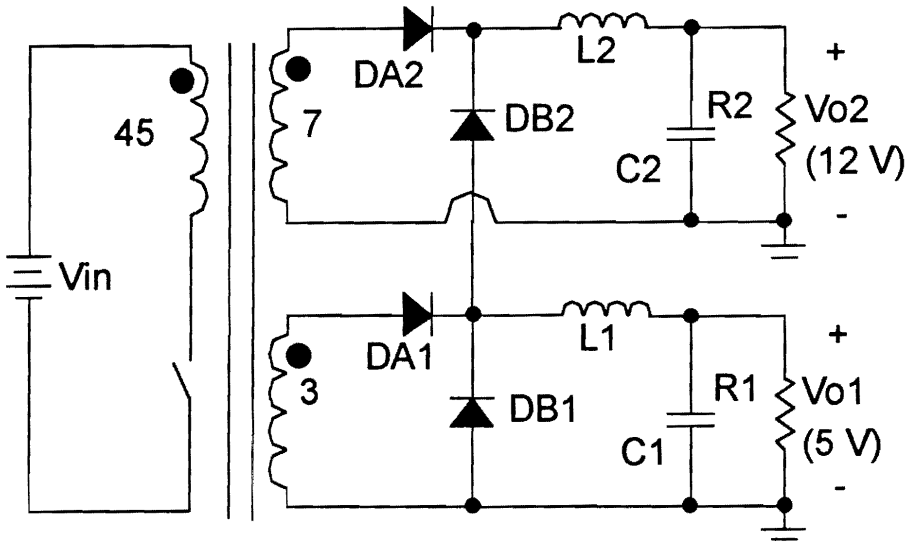
Internal voltage compensation occurs during turn-off of the active switch. The transformer is the same as that of non-stacked case, *i.e.*, the 12-V secondary winding is 7 turns. The losses are smaller compared with (A). The current stress of D_{B1} is increased to $I_{o1}+I_{o2}$.

(C) Stacking the secondary windings and the freewheeling diodes (Fig. 3.7(a)).

This is the combination of schemes (A) and (B). Internal voltage compensation occurs during both turn-on and -off intervals. The transimpedances and power losses are

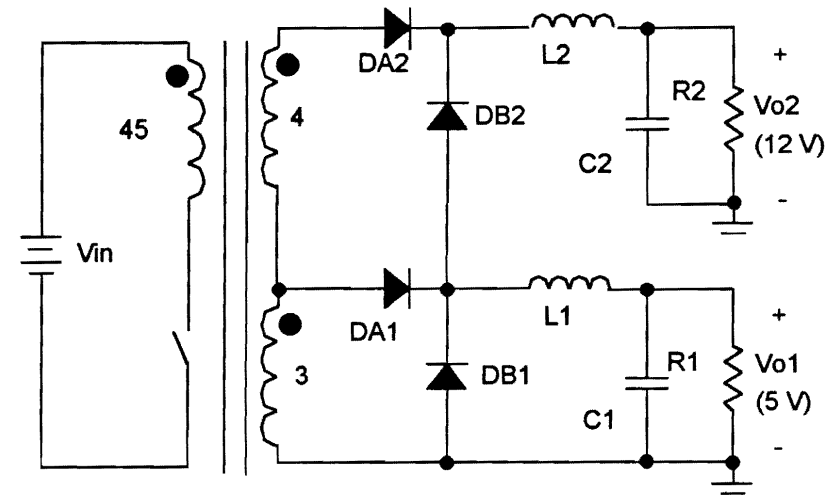


(a)

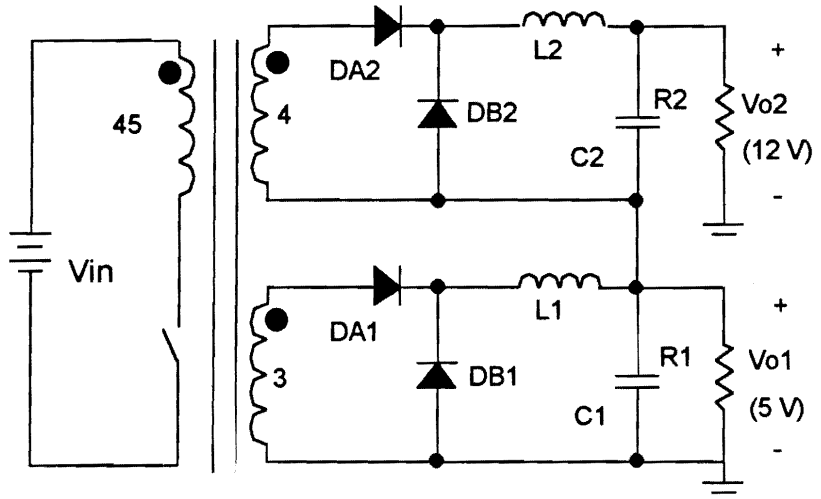


(b)

Fig. 3.6. Variations of the stacking scheme (I): *(a) stacking the secondary windings of the transformer; (b) stacking the freewheeling diodes.*



(a)



(b)

Fig. 3.7. Variation of the stacking scheme (II): *(a) stacking the secondary windings of the transformer and freewheeling diodes; (b) stacking the outputs.*

moderate among all the stacking schemes. The current stress of D_{B1} is $I_{o1}+I_{o2}$.

(D) Stacking at the input of the output filter (Fig. 3.1(b)).

This scheme has been fully analyzed in the last section, and it is listed here again to facilitate comparison. Internal voltage compensation occurs during turn-on of the active switch. The transimpedances and the increased losses are similar to those of (B).

(E) Stacking at the output of V_{o1} (Fig. 3.7(b)).

This scheme provides the best output voltage tracking, since the transimpedances are the largest. The power losses, nevertheless, are also the highest. The current stresses for both D_{A1} and D_{B1} are increased from I_{o1} to $I_{o1}+I_{o2}$.

The analytical expressions of output voltages for all the discussed stacking schemes can take the form given in Eqs. (3.7) and (3.9). These expressions, together with the condition that the feedback signal be equal to the reference voltage, facilitate control design. The output voltages, however, can also be expressed in terms of the impedances, as shown in Eqs. (3.8) and (3.10). The impedance form makes it easier to compare the voltage tracking ability, voltage offset amount, and power losses for various stacking schemes. The output voltages with impedance form can be generally expressed as:

$$V_{o1} = V_{s1}D_e - V_{d1} - I_{o1}Z_{11} - I_{o2}Z_{12}, \tag{3.24}$$

$$V_{o2} = (V_{s1} + V_{s2})D_e - V_{d2} - I_{o1}Z_{21} - I_{o2}Z_{22} - V_{off}. \tag{3.25}$$

Table 3.1 summarizes the expressions for the constant offset voltage, V_{off}, and the

Table 3.1 Analytical Expressions of the Internal Impedances and the Off-Set Voltage for V_{o2}

Type	Z_{11}	Z_{12}	Z_{21}	Z_{22}	V_{off}
(a)	$R_{s1}D_e + L_{s1}f_s + R_{d1} + R_{L1}$	$R_{s1}D_e + L_{s1}f_s$	$R_{s1}D_e + L_{s1}f_s$	$(R_{s1} + R_{s2})D_e + R_{d2} + R_{L2} + (L_{s1} + L_{s2})f_s$	0
(b)	$R_{s1}D_e + L_{s1}f_s + R_{d1} + R_{L1}$	$R_{d1}(1 - D_e)$	$R_{d1}(1 - D_e)$	$R_{d1}(1 - D_e) + R_{d2} + L_{s2}f_s + R_{L2}$	$(1 - D_e)V_{d1}$
(c)	$R_{s1}D_e + L_{s1}f_s + R_{d1} + R_{L1}$	$(R_{s1} + R_{L1})D_e + R_{d1}(1 - D_e) + L_{s1}f_s$	$R_{s1}D_e + (1 - D_e)R_{d1} + L_{s1}f_s$	$(R_{s1} + R_{s2})D_e + (1 - D_e)R_{d1} + R_{d2} + R_{L2}(L_{s1} + L_{s2})f_s$	$(1 - D_e)V_{d1}$
(d)	$R_{s1}D_e + L_{s1}f_s + R_{d1} + R_{L1}$	$(R_{s1} + R_{d1})D_e + L_{s1}f_s$	$(R_{s1} + R_{d1})D_e + L_{s1}f_s$	$(R_{s1} + R_{d1} + R_{s2})D_e + R_{d2} + R_{L2} + (L_{s1} + L_{s2})f_s$	$V_{d1}D_e$
(e)	$R_{s1}D_e + L_{s1}f_s + R_{d1} + R_{L1}$	$R_{s1}D_e + R_{d1} + L_{s1}f_s + R_{L1}$	$R_{s1}D_e + L_{s1}f_s + R_{d1} + R_{L1}$	$(R_{s1} + R_{s2})D_e + (L_{s1} + L_{s2})f_s + R_{d1} + R_{d2} + R_{L1} + R_{L2}$	V_{d1}

impedances, Z_{ij}. Stacking at the output, as in scheme (E), gives the highest transimpedances, since the 12-V output current flows through all the 5-V secondary components. Therefore, voltage tracking between the outputs is the best among the five schemes. Stacking the secondary windings, as in scheme (A), yields the smallest transimpedance and the worst voltage tracking. Stacking freewheeling diodes, as in scheme (B), stacking the secondary windings and the freewheeling diodes simultaneously, as in scheme (C), and stacking at the input of the output filter, as in scheme (D), give intermediate transimpedances and voltage tracking ability. In terms of efficiency, the results are exactly opposite. Scheme (E) has maximum power loss, and scheme (A) has minimum power losses. The power losses and voltage tracking for schemes (B), (C) and (D) depend on duty cycle. If the duty cycle is greater than 50%, scheme (D) gives better voltage tracking and larger power loss. If the duty cycle is smaller than 50%, schemes (B) and (C) yield better voltage tracking and larger power losses. Table 3.2 shows the comparison of power losses for different stacking schemes.

Table 3.2. Comparison of Power Losses for Various Schemes.

(Total power loss before stacking: $P=16.41\ W$)

Scheme	(A)	(B)	(C)	(D)	(E)
$P_S\ (W)$	16.46	17.54	17.9	17.74	20.44
$\Delta P/P\ (\%)$	0.3	6.9	9	8.1	24.6

3.4 Summary

Stacking of secondaries is a simple but effective method of improving dc cross-regulation for multiple-output converters without severely sacrificing efficiency. By stacking the secondaries, coupling between the power channels is introduced, and the outputs can track each other as any load current changes. The voltage tracking ability depends on the transimpedances. Large transimpedances yield good voltage tracking but poor efficiency. There is a trade-off between dc cross-regulation and efficiency. Stacking secondary windings gives the smallest transimpedances, and therefore the voltage tracking is the poorest. As the stacking point moves further away from the secondary winding, the transimpedances are increased, which results in better voltage tracking. Stacking at the output gives the highest transimpedances, the best voltage tracking, but the worst efficiency.

4. Small-Signal Analysis and Design for Multiple-Output Converters

4.1 Introduction

Generally, the small-signal properties of a multiple-output converter with WVC and/or coupled inductors are quite different from those of a single-output converter or a multiple-output converter with only one regulated output. The differences are primarily caused by interaction among the outputs of the converter, resulting in higher order of the small-signal transfer functions. Furthermore, when WVC is used simultaneously with the coupled output-filter inductors, the positions of poles and zeros of the small-signal transfer functions are significantly altered compared with the non-coupled case. Some published papers have noticed the sensitivity of the loop gain to the coupled inductors [F9, F10, I16], but did not give the explanations of how the coupled inductors affect the system characteristics. There is little information available for design engineers when performing

loop compensation. The purpose of this chapter is to provide a small-signal model and a compensator design methodology for the multiple-output forward converter.

First, a small-signal model for a multiple-output forward converter with weighted voltage control is derived. The model is derived by assuming the most general case for arbitrary number of outputs with coupled output-filter inductors, Fig. 4.1. The effects of the weighting factors and the coupled inductors on the small-signal behavior are investigated. In addition, the small-signal characteristics, such as audio susceptibilities, output impedances, and output transimpedances of the multiple-output converter with weighted voltage control and coupled output-filter inductors are studied. Based on the analysis, the design issues for loop compensation are discussed. The small-signal model and the design procedure are verified on an experimental two-output forward converter.

4.2 Small-Signal Modeling

The small-signal model is obtained by applying PWM-switch modeling techniques [F5]. In this technique, the nonlinear PWM switches of a converter are replaced with a simple linear small-signal circuit. Figure 4.2 shows the small-signal equivalent circuit of a multiple-output converter with coupled inductors obtained by replacing the active and passive switches with the PWM switch small-signal model. To simplify the analysis, the

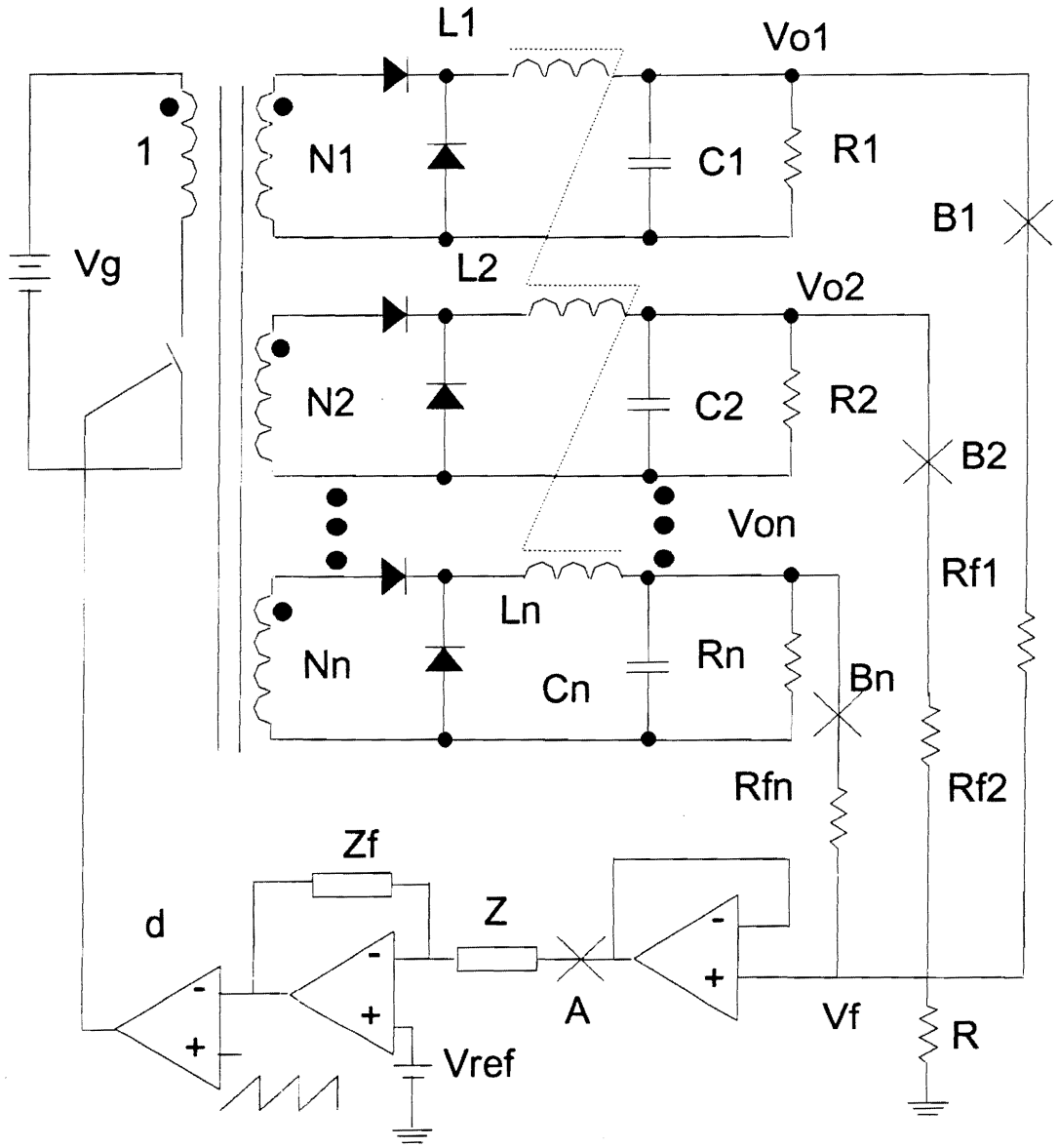


Fig. 4.1 A multiple-output forward converter with WVC and coupled output filter inductors. The weighted control and coupled inductors complicate the small-signal behavior of the converter.

following assumptions are made:

1) The switches (including passive and active switches) have zero junction capacitances and infinite off-resistances. The small-signal on-resistances of the switches are lumped together with the winding resistances of the output filter inductors.

2) The transformer is ideal, *i.e.*, the magnetizing inductance is infinite, and the leakage inductances are zero. The core loss is negligible.

3) The output filter inductors do not have any core losses.

It should be emphasized that these assumptions are justified only for small-signal analysis because the circuit parasitics have negligible effect on the ac characteristics. However, the same parasitics have significant effects on the dc characteristics and cannot be neglected in the dc analysis as discussed in Chapter 2.

The small signal model is derived for the operation in continuous conduction mode (CCM). The state space variables are defined as the inductor currents and capacitor voltages:

$$X = [i_{L1} \quad i_{L2} \quad \cdots \quad i_{Ln} \quad v_{c1} \quad v_{c2} \quad \cdots \quad v_{cn}]^T_{2n\times 1}, \tag{4.1}$$

the input variables are the input voltage, load currents and duty cycle:

$$U = [v_{in} \quad d \quad i_{o1} \quad i_{o2} \quad \cdots \quad i_{on}]^T_{(n+2)\times 1}, \tag{4.2}$$

and the output variables are the output voltages:

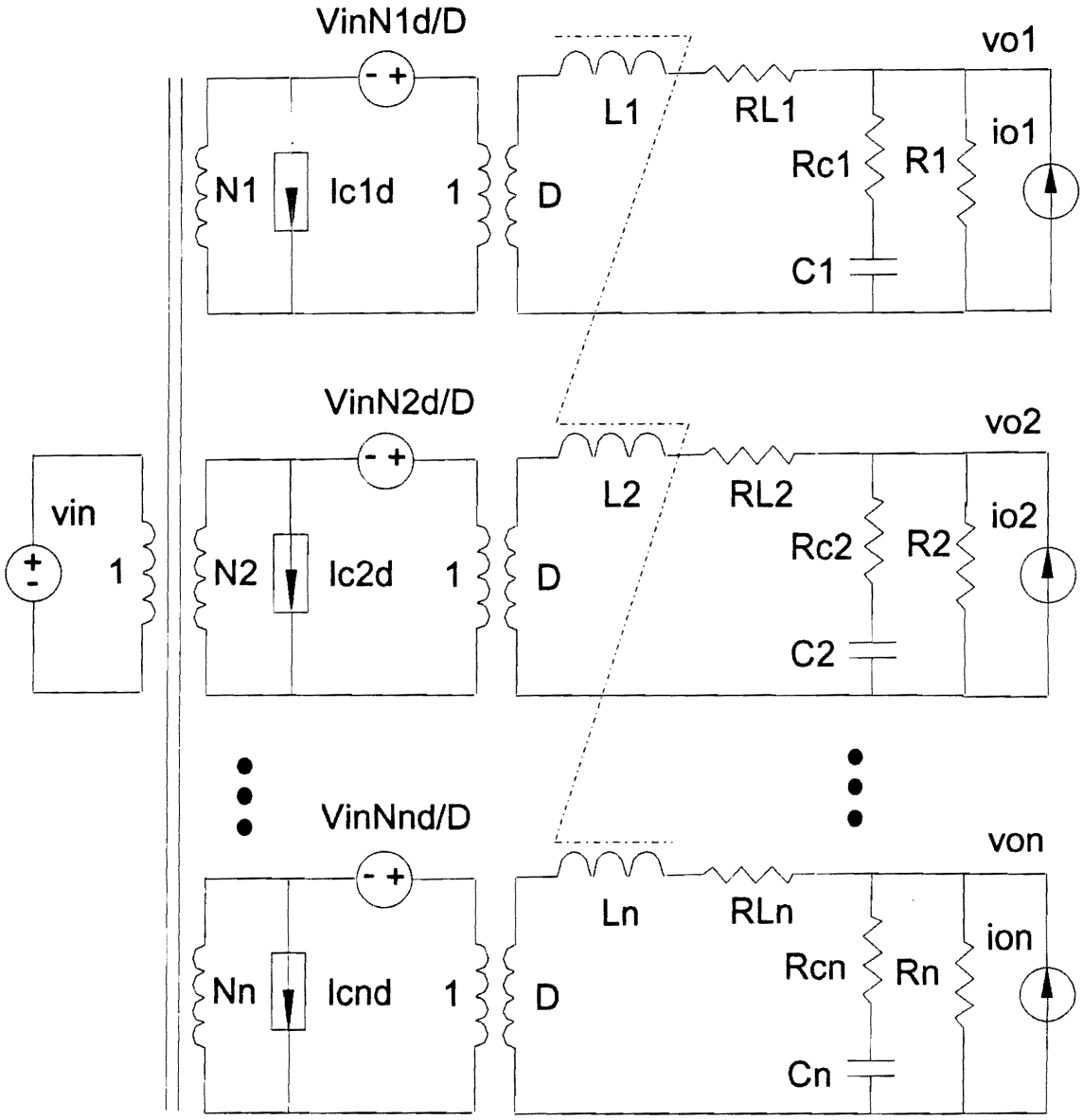


*Fig. 4.2. **Small-signal circuit model obtained by using PWM switch model.** By assuming ideal transformer, the secondary power channels can be separated from each other, and 3-terminal PWM switch model can be applied.*

$$Y = [v_{o1} \quad v_{o2} \quad \cdots \quad v_{on}]^T_{n\times 1}. \tag{4.3}$$

The resulting state equations are

$$\dot{X} = AX + BU, \tag{4.4}$$

$$Y = CX + DU, \tag{4.5}$$

where

$$A = \begin{bmatrix} -M^{-1}P \\ S \end{bmatrix}_{2n\times 2n}, \tag{4.6}$$

$$B = \begin{bmatrix} M^{-1}R \\ T \end{bmatrix}_{2n\times(n+2)}, \tag{4.7}$$

$$C = \begin{bmatrix} R_{p1} & 0 & \cdots & 0 & R_{q1} & 0 & \cdots & 0 \\ 0 & R_{p2} & \cdots & 0 & 0 & R_{q2} & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & R_{pn} & 0 & 0 & \cdots & R_{qn} \end{bmatrix}_{n\times 2n}, \tag{4.8}$$

$$D = \begin{bmatrix} 0 & 0 & R_{p1} & 0 & \cdots & 0 \\ 0 & 0 & 0 & R_{p2} & \cdots & 0 \\ \vdots & \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & 0 & \cdots & R_{pn} \end{bmatrix}_{n\times(n+2)}. \tag{4.9}$$

M is the inductance matrix which is defined as:

$$M = \begin{bmatrix} M_{11} & M_{12} & \cdots & M_{1n} \\ M_{21} & M_{22} & \cdots & M_{2n} \\ \vdots & \vdots & \ddots & \vdots \\ M_{n1} & M_{n2} & \cdots & M_{nn} \end{bmatrix}_{n\times n}, \tag{4.10}$$

$$P = \begin{bmatrix} R_{t1} & 0 & \cdots & 0 & R_{q1} & 0 & \cdots & 0 \\ 0 & R_{t2} & \cdots & 0 & 0 & R_{q2} & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & R_{tn} & 0 & 0 & \cdots & Rqn \end{bmatrix}_{n\times 2n}, \tag{4.11}$$

$$R = \begin{bmatrix} N_1 V_{in} & N_1 D & -R_{p1} & 0 & \cdots & 0 \\ N_2 V_{in} & N_2 D & 0 & -R_{p2} & \cdots & 0 \\ \vdots & \vdots & \vdots & \vdots & \ddots & \vdots \\ N_n V_{in} & N_n D & 0 & 0 & \cdots & -R_{pn} \end{bmatrix}_{n\times(n+2)}, \tag{4.12}$$

$$S = \begin{bmatrix} \frac{R_1}{\tau_1} & 0 & \cdots & 0 & -\frac{1}{\tau_1} & 0 & \cdots & 0 \\ 0 & \frac{R_2}{\tau_2} & \cdots & 0 & 0 & -\frac{1}{\tau_2} & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & \frac{R_n}{\tau_n} & 0 & 0 & \cdots & -\frac{1}{\tau_n} \end{bmatrix}_{n\times 2n}, \tag{4.13}$$

$$T=\begin{bmatrix} 0 & 0 & \frac{R_1}{\tau_1} & 0 & \cdots & 0 \\ 0 & 0 & 0 & \frac{R_2}{\tau_2} & \cdots & 0 \\ \vdots & \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & 0 & \cdots & \frac{R_n}{\tau_n} \end{bmatrix}_{n\times(n+2)}, \tag{4.14}$$

where the elements of the coefficient matrices are defined as:

$$M_{ij}=k_{ij}\sqrt{L_iL_j},\ i\neq j,\quad M_{ii}=L_i, \tag{4.15}$$

$$R_{pi}=R_i//R_{ci},\quad R_{qi}=\frac{R_i}{R_i+R_{ci}},$$

$$R_{ti}=R_{Li}+R_i//R_{ci},\quad \tau_i=(R_i+R_{ci})C_i,\quad (i,j=1,\ldots n),$$

and k_{ij} is the coupling coefficient between the i-th and j-th output filter inductors, R_i the load resistor, R_{Li} the sum of the on-resistance of the rectifier diode and the output filter inductor, C_i the filter capacitor, R_{ci} the equivalent series resistor (ESR) of the capacitor, and N_i the transformer turns ratio.

Equations (4.1) through (4.15) are general expressions which describe the small-signal behavior of a forward converter with n outputs in time domain. The system characteristics in the frequency domain, where design and measurements are usually performed, are easily obtained by taking Laplace transform of the state equations.

4.3 Effects of Weighted Control and Coupled Inductors

In this section, the individual as well as combined effects of the weighting factors and coupling coefficients of the output filter inductors on small-signal transfer function are investigated. First, the effects of the weighting factors are studied by assuming no coupling between the output filter inductors. Then the effects of the coupling coefficients in the absence of WVC are studied. Finally, the combined effects of the weighting factors and coupling coefficients are discussed. To avoid lengthy expressions without losing generality, the following analysis is performed on a forward converter with two outputs.

4.3.1 Effects of Weighting Factors

To investigate the effects of weighting factors alone, it is assumed that the coupling coefficients are zero, *i.e.*, $k_{ij}=0,\ i,j=1,2,\ i\neq j$, in the small-signal model derived in the previous section. For WVC, according to Fig. 4.1, the feedback signal, v_f, is derived from the weighted sum of the output voltages, *i.e.*,

$$v_f = K_1 v_{o1} + K_2 v_{o2}. \tag{4.16}$$

where K_1 and K_2 are the weighting factors which can be calculated from the weighting network resistors:

$$K_1 = \frac{R_{f2}R}{R_{f1}R_{f2} + R_{f1}R + R_{f2}R}, K_2 = \frac{R_{f1}R}{R_{f1}R_{f2} + R_{f1}R + R_{f2}R}. \tag{4.17}$$

In the following analyses, two quantities are often encountered, *i.e.*, duty cycle-to-output transfer function and duty cycle-to-feedback transfer function. Here "feedback" refers to the weighted sum of the output voltages which is used as feedback signal. "Output" refers to the output voltage of each power channel.

From Eqs. (4.1) - (4.16), the duty cycle-to-feedback transfer function is derived as:

$$G_{vd}(s) = \frac{v_f}{d} = \frac{K_1 N_1 V_{in}(1 + \frac{s}{s_{z1}})}{(1 + \frac{s}{\omega_{o1}Q_1} + \frac{s^2}{\omega_{o1}^2})} + \frac{K_2 N_2 V_{in}(1 + \frac{s}{s_{z2}})}{(1 + \frac{s}{\omega_{o2}Q_2} + \frac{s^2}{\omega_{o2}^2})}, \tag{4.18}$$

where ω_{oi} is the resonant frequency of each output filter, Q_i the damping coefficient, and s_{zi} the ESR zero. They are given by:

$$\omega_{oi} = \frac{1}{\sqrt{L_i C_i}} \sqrt{\frac{1 + R_{Li}/R_i}{1 + R_{Ci}/R_i}} \approx \frac{1}{\sqrt{L_i C_i}}, \tag{4.19}$$

$$Q_i = \frac{1}{\omega_{oi}} \frac{1}{L_i/(R_{Li} + R_i) + C_i(R_{ci} + R_{Li}//R_i)}, \tag{4.20}$$

$$s_{zi} = 1/(R_{ci}C_i), \quad i = 1, 2. \tag{4.21}$$

To study the effect of the weighting factors on the small-signal characteristics, Eq.

(4.18) is factorized into pole-zero product form:

$$G_{vd}(s)=V_{in}\frac{K_1N_1(1+\frac{s}{s_{z1}})(1+\frac{s}{\omega_{o2}Q_2}+\frac{s^2}{\omega_{o2}^2})+K_2N_2(1+\frac{s}{s_{z2}})(1+\frac{s}{\omega_{o1}Q_1}+\frac{s^2}{\omega_{o1}^2})}{(1+\frac{s}{\omega_{o1}Q_1}+\frac{s^2}{\omega_{o1}^2})(1+\frac{s}{\omega_{o2}Q_2}+\frac{s^2}{\omega_{o2}^2})}. \quad (4.22)$$

The numerator is

$$Num=V_{in}\left[K_1N_1(1+\frac{s}{s_{z1}})(1+\frac{s}{\omega_{o2}Q_2}+\frac{s^2}{\omega_{o2}^2})+K_2N_2(1+\frac{s}{s_{z2}})(1+\frac{s}{\omega_{o1}Q_1}+\frac{s^2}{\omega_{o1}^2})\right]. \quad (4.23)$$

Usually, the frequencies of the ESR zeros are much higher than the resonant frequencies of the low pass filters, or $|\omega_{oi}|<<s_{zi}$, $i=1, 2$. At low frequency, *i.e.*, $|s|<<s_{zi}$, $i=1, 2$, Eq. (4.23) can be approximated as:

$$Num\approx V_{in}\left[K_1N_1(1+\frac{s}{\omega_{o2}Q_2}+\frac{s^2}{\omega_{o2}^2})+K_2N_2(1+\frac{s}{\omega_{o1}Q_1}+\frac{s^2}{\omega_{o1}^2})\right], \quad (4.24)$$

or

$$Num\approx V_{in}K_B(1+\frac{s}{\omega_zQ_z}+\frac{s^2}{\omega_z^2}), \quad (4.25)$$

where

$$K_B=K_1N_1+K_2N_2, \quad (4.26)$$

$$\frac{1}{\omega_z^2} = \frac{1}{K_1N_1 + K_2N_2}\left(\frac{K_2N_2}{\omega_{o1}^2} + \frac{K_1N_1}{\omega_{o2}^2}\right), \tag{4.27}$$

$$\frac{1}{\omega_z Q_z} = \frac{1}{K_1N_1 + K_2N_2}\left(\frac{K_2N_2}{\omega_{o1}Q_1} + \frac{K_1N_1}{\omega_{o2}Q_2}\right). \tag{4.28}$$

Since the numerator is of the 3rd order, it can be written in the form of:

$$Num \approx V_{in}K_B\left(1 + \frac{s}{s_z}\right)\left(1 + \frac{s}{\omega_z Q_z} + \frac{s^2}{\omega_z^2}\right). \tag{4.29}$$

Letting Eq. (4.29) equal Eq. (4.23) and comparing the coefficients of s terms on both sides, the following relation is obtained:

$$\frac{1}{s_z} \approx \frac{1}{K_1N_1 + K_2N_2}\left(\frac{K_1N_1}{s_{z1}} + \frac{K_2N_2}{s_{z2}}\right). \tag{4.30}$$

Finally, the duty cycle-to-feedback transfer function is rewritten into the pole-zero form:

$$G_{vd}(s) = V_{in}\frac{K_B\left(1 + \frac{s}{s_z}\right)\left(1 + \frac{s}{\omega_z Q_z} + \frac{s^2}{\omega_z^2}\right)}{\left(1 + \frac{s}{\omega_{o1}Q_1} + \frac{s^2}{\omega_{o1}^2}\right)\left(1 + \frac{s}{\omega_{o2}Q_2} + \frac{s^2}{\omega_{o2}^2}\right)}, \tag{4.31}$$

where

$$K_B = K_1N_1 + K_2N_2, \tag{4.32}$$

$$\frac{1}{s_z} \approx \frac{1}{K_1N_1 + K_2N_2}\left(\frac{K_1N_1}{s_{z1}} + \frac{K_2N_2}{s_{z2}}\right), \tag{4.33}$$

$$\frac{1}{\omega_z^2} \approx \frac{1}{K_1N_1 + K_2N_2}\left(\frac{K_2N_2}{\omega_{o1}^2} + \frac{K_1N_1}{\omega_{o2}^2}\right). \tag{4.34}$$

As can be seen from Eq. (4.31), unlike the two-output converter with single-output feedback control where the transfer function is of the 2nd order, the transfer function of the same converter with WVC becomes the 4th order. Figure 4.3 shows the Bode plot of the duty cycle-to-feedback transfer function (v_f/d) using the ratio of the weighting factors, $u(=K_1/K_2)$, as running parameter. According to Eq. (4.31), the transfer function has two pairs of complex poles, one pair of complex zeros, and a real zero (equivalent ESR zero). From Eq. (4.19), resonant frequencies ω_{o1} and ω_{o2} of the complex poles do not depend on the weighting factors. However, the resonant frequency of complex zero, ω_z, and the real zero, s_z, are the functions of weighting factors K_1 and K_2, as can be seen from Eqs. (4.33) and (4.34). Therefore, as the ratio of the weighting factors varies, the positions of the poles are fixed, and the positions of the zeros are changing. Assuming $\omega_{o1} \le \omega_{o2}$, it can be seen from Eq. (4.34) that

$$\frac{1}{\omega_z^2} = \frac{1}{K_1N_1 + K_2N_2}\left(\frac{K_2N_2}{\omega_{o1}^2} + \frac{K_1N_1}{\omega_{o2}^2}\right) \le \frac{1}{K_1N_1 + K_2N_2}\left(\frac{K_2N_2}{\omega_{o1}^2} + \frac{K_1N_1}{\omega_{o1}^2}\right) = \frac{1}{\omega_{o1}^2}, \tag{4.35}$$

and

$$\frac{1}{\omega_z^2} = \frac{1}{K_1N_1 + K_2N_2}\left(\frac{K_2N_2}{\omega_{o1}^2} + \frac{K_1N_1}{\omega_{o2}^2}\right) \ge \frac{1}{K_1N_1 + K_2N_2}\left(\frac{K_2N_2}{\omega_{o2}^2} + \frac{K_1N_1}{\omega_{o2}^2}\right) = \frac{1}{\omega_{o2}^2}. \tag{4.36}$$

Equations (4.35) and (4.36) show that no matter how the zeros move, the poles and

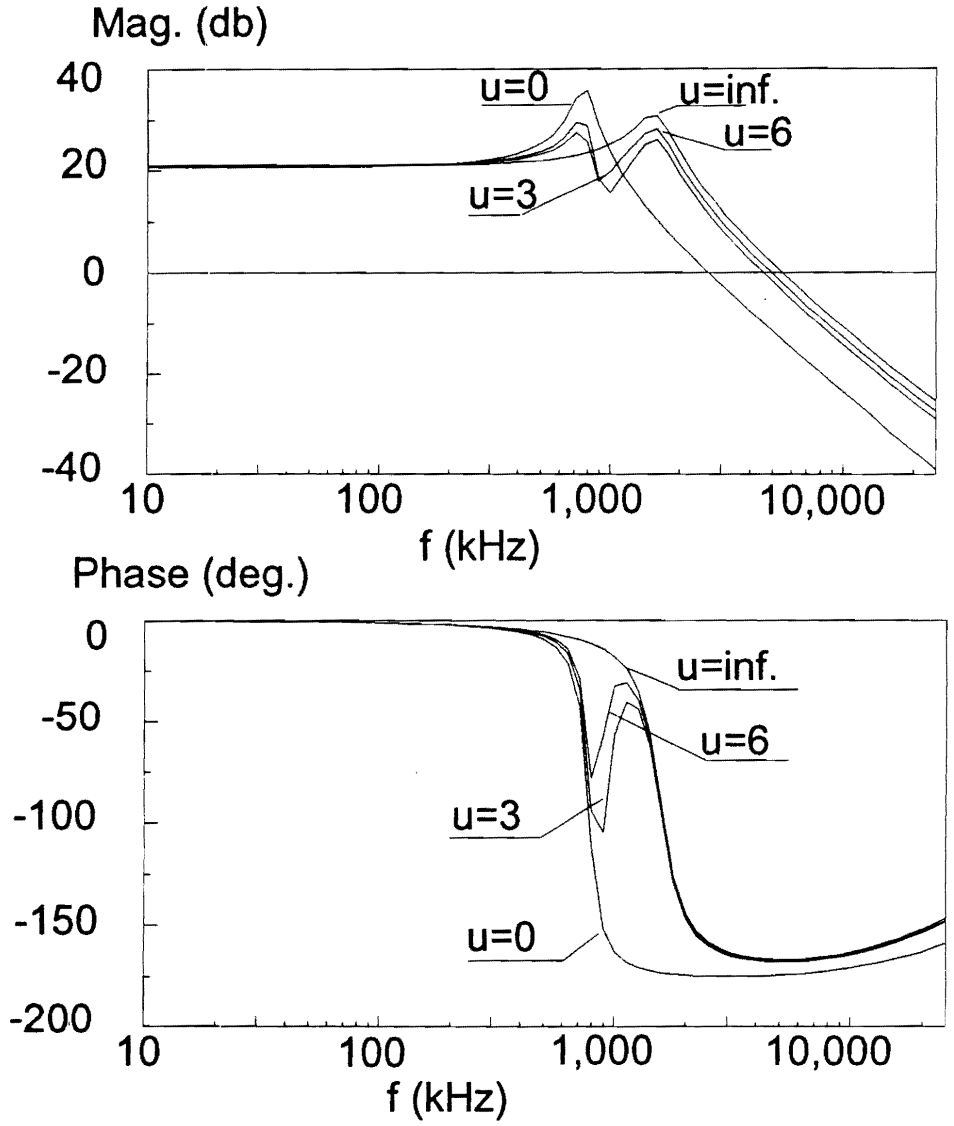


Fig. 4.3. Bode plot of duty cycle-to-feedback (v_f /d) transfer function of a multiple-output converter with WVC. The ratio of the weighting factors is the running parameter.

zeros are always interlaced, *i.e.*,

$$\omega_{o1} \le \omega_z \le \omega_{o2}. \tag{4.37}$$

The interlaced pole-zero distribution makes the system behavior at both low and high frequencies similar to that of a 2nd order system. In the middle frequency range, however, the frequency characteristics exhibit multiple peaks.

If the extreme case is assumed, *i.e.*, $u = 0\ (or\ \infty)$, the transfer function is reduced to a 2nd order system. Therefore, the single feedback control scheme is a special case of the weighted voltage control. Actually, the duty cycle-to-output transfer function is bounded by these two extreme cases.

4.3.2 Effects of Coupled Inductors

The duty cycle-to-output transfer functions of the two-output converter with coupled inductors but without WVC is derived as follows:

$$G_{vd1} = \frac{\begin{array}{l} V_{in}(1+R_{C1}C_1 s)\{N_1[1+(R_{C2}C_2+\frac{L_2}{R_2}+R_{L2}C_2)s+L_2C_2s^2] \\ \quad -N_2[\frac{M_{12}}{R_2}s+C_2M_{12}s^2]\} \end{array}}{\begin{array}{l} [1+(R_{C1}C_1+\frac{L_1}{R_1}+R_{L1}C_1)s+L_1C_1s^2][1+(R_{C2}C_2+\frac{L_2}{R_2}+R_{L2}C_2)s+L_2C_2s^2] \\ \quad -[\frac{M_{12}}{R_1}s+C_1M_{12}s^2][\frac{M_{12}}{R_2}s+C_2M_{12}s^2] \end{array}} \cdot \tag{4.38}$$

Exchanging the subscripts 1 (or 2) to 2 (or 1), the duty cycle-to-output 2 transfer function, G_{vd2}, can be obtained. Obviously, if there is no coupling between the output inductors L_1 and L_2, *i.e.*, the coupling coefficient $k=k_{12}=0$, the transfer function reduces to that of the single output converter, which is a 2nd order system.

Figure 4.4 shows the duty cycle-to-output transfer functions for both outputs, where the coupling coefficient k is the running parameter. Generally, the transfer functions are of the 4th order, with two pairs of complex poles, a pair of complex zeros, and a real zero. The resonant frequencies of both poles and zeros depend on the value of the coupling coefficient. Unlike the case of WVC without coupled inductors, where the poles and zeros are always interlaced, here the duty cycle-to-output transfer function for one output has an interlaced pole-zero distribution (Fig. 4.4(a)), whereas another has a non-interlaced pole-zero distribution (Fig. 4.4(b)). As a result, for the conventional single-output feedback control, the loop compensation depends on the choice of the sensed output. It is more desirable to feedback the output whose duty cycle-to-output transfer function has interlaced poles and zeros. It is observed that the power channel with higher resonant frequency of the output filter has interlaced complex poles and zeros. From compensation design point of view, therefore, this output should be sensed to implement the feedback regulation if single feedback control scheme is used.

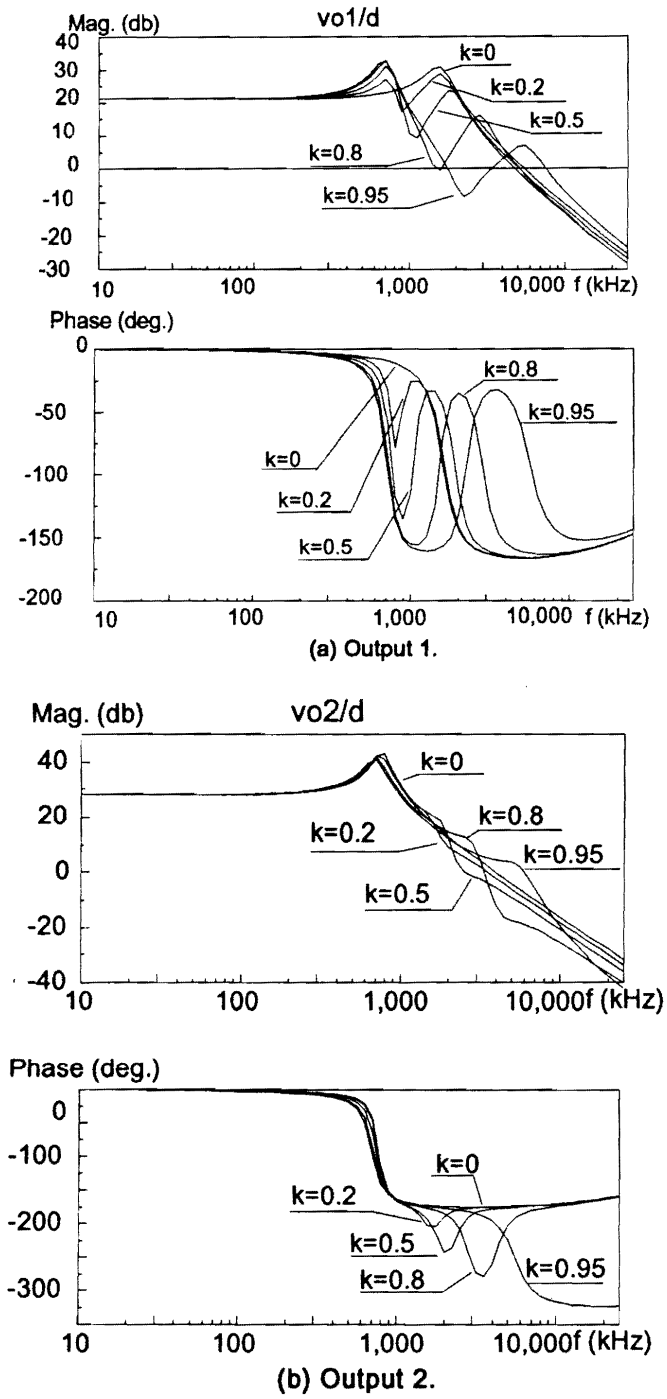


*Fig. 4.4 **Bode plots of duty cycle-to-output transfer function of the dual-output forward converter with coupled inductors.** (a) output 1; (b) output 2. The coupling coefficient is the running parameter.*

4.3.3 Combined Effects of WVC and Coupled Inductors

When WVC and coupled inductors are employed simultaneously, the duty cycle-to-feedback transfer function is obtained by summing two weighted outputs:

$$\frac{v_f}{d} = K_1 G_{vd1} + K_2 G_{vd2}. \tag{4.39}$$

where G_{vd1} and G_{vd2} are defined by Eq. (4.38).

Figure 4.5 shows the Bode plot of the duty cycle-to-feedback transfer function. For different ratio of the weighting factors and different coupling coefficient, the system behavior can change drastically, from the 2nd order system to the 4th order system, from an interlaced pole-zero distribution to a non-interlaced distribution.

Figure 4.6 shows the pole-zero distribution for different values of the coupling coefficient and the ratio of the weighting factors, where the resonant frequencies of the output filter are not close to each other. As can be seen, the locations of the complex zeros are dependent on both the ratio of the weighting factors and the coupling coefficient, whereas the locations of the complex poles are only affected by coupling coefficient. Furthermore, the low frequency poles have a smaller variation and the high frequency poles have a larger variation as the coupling coefficient varies. The physical cause of this phenomenon is explained in the following section.

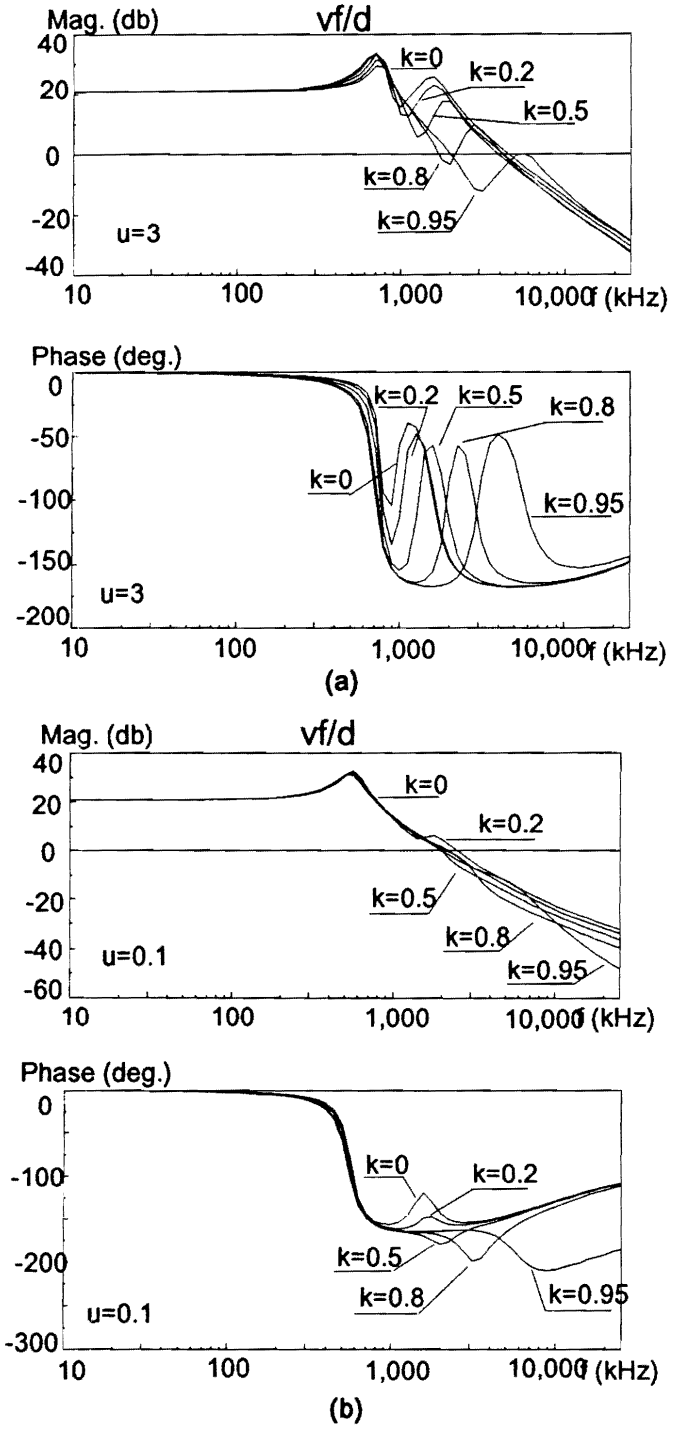


Fig. 4.5. Bode plots of duty cycle-to-feedback (v_f /d) transfer function of the dual-output converter with WVC and coupled inductors for different weighting factors. (a) $u=K_1/K_2=3$; (b) $u=K_1/K_2=0.1$.

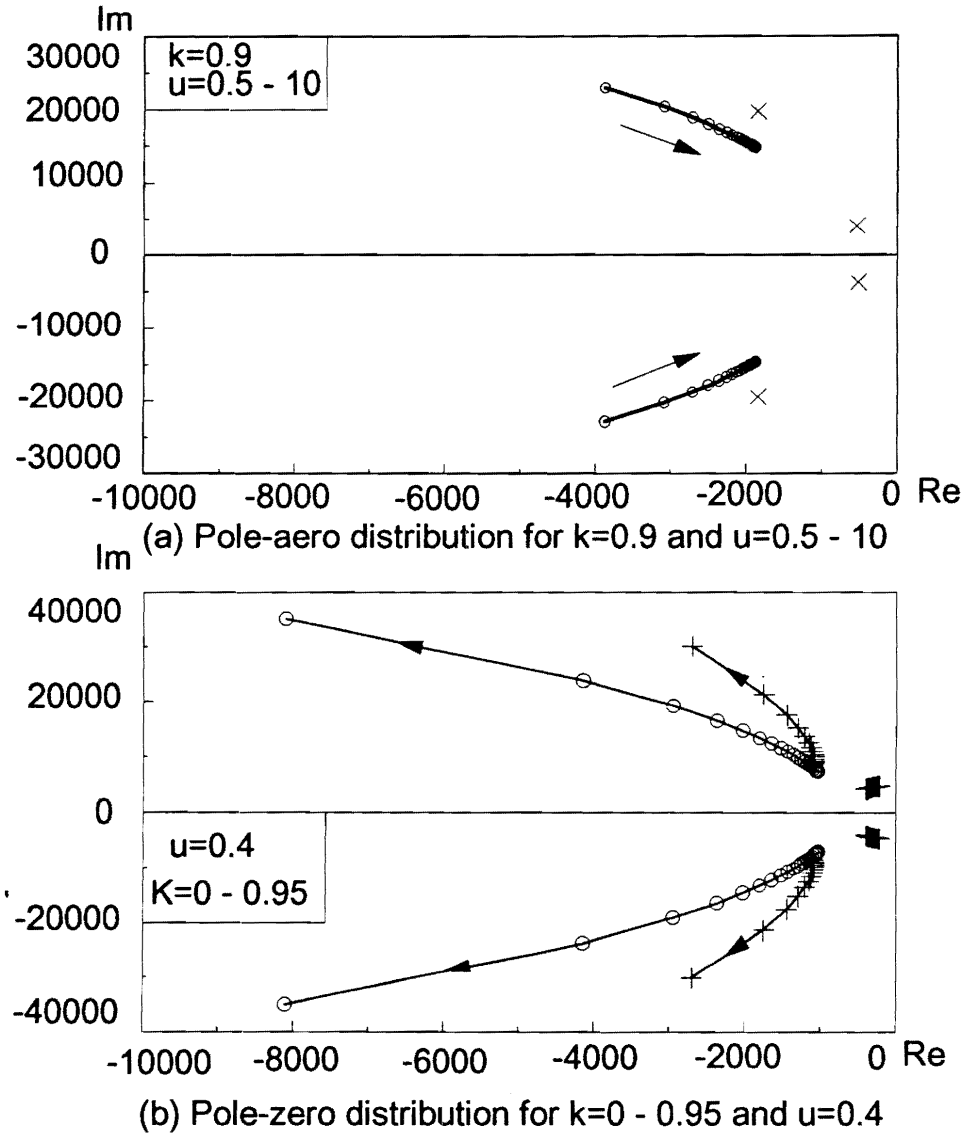


*Fig. 4.6. **Pole-zero distribution of a MOC with WVC and coupled inductors for different values of the weighting factors and the coupling coefficient.** The equivalent real zero locates far beyond the left boundary, and is not shown here. (a) k=0.9, u=0.5 - 10; (b) k=0 - 0.95, u=0.4.*

4.3.4 Physical Explanation of Variation of the Complex Poles and Zeros

Figure 4.6 shows that the complex poles and zeros are the functions of the coupling coefficient, k. This phenomenon can be predicted by using Eq. (4.39), but no physical explanation is given to accompany the equation. In this section, the physical reason why the complex poles and zeros are varied as the coupling coefficient changes is explained.

Figure 4.7 shows the equivalent small-signal model of the multiple-output converter obtained by replacing the coupled inductors with its circuit model. The coupled inductors, which are characterized by the self-inductances, mutual inductance and coupling coefficient in Sections 4.3.1 - 4.3.3, are now modeled in terms of mutual inductance M_c, leakage inductances L_{ci}, and voltage transfer ratio n_{12}. To simplify the analysis, the ESR's of the output filter capacitors are neglected. All the circuit parameters are referred to the V_{o1} secondary side, and the referred parameter values are

$$v_{o2}' = n_{12} v_{o2}, \tag{4.40}$$

$$R_2' = n_{12}^2 R_2, \tag{4.41}$$

$$L_{c2}' = n_{12}^2 L_{c2}, \tag{4.42}$$

$$C_2' = \frac{C_2}{n_{12}^2}, \tag{4.43}$$

where n_{12} is the voltage ratio from the V_{o2} channel to V_{o1} channel, or if the leakage

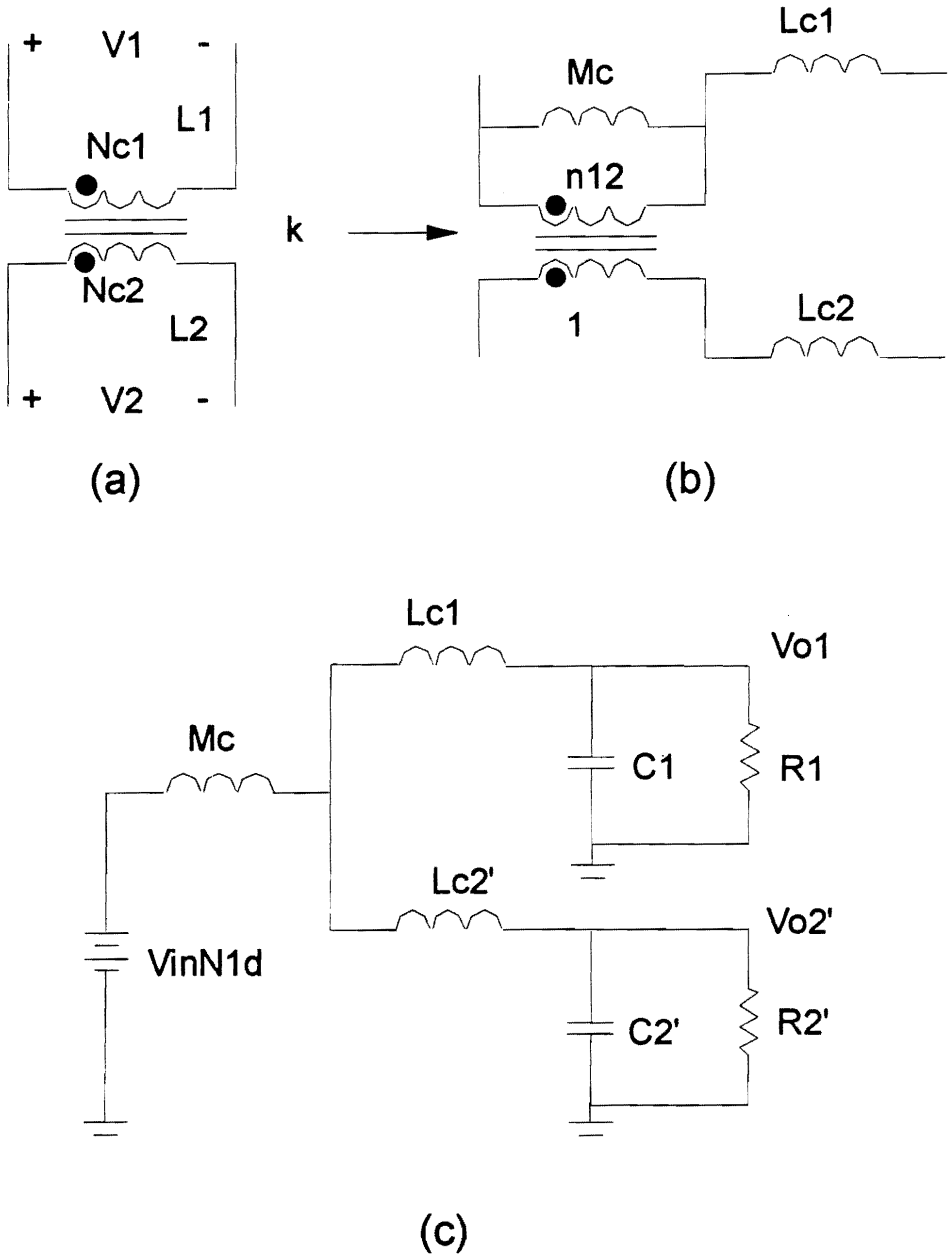


Fig. 4.7 Physical explanation of the variation of the complex poles and zeros by replacing the coupled inductors with its equivalent circuit model: (a) coupled inductors; (b) circuit model of the coupled inductors; (c) equivalent small-signal model with all the circuit parameters referred to V_{o1} secondary side.

inductances are very small, the voltage ratio is simply the turns ratio of the coupled inductors.

From Fig. 4.7, the following equations can be obtained:

$$(1+\frac{L_{c1}}{R_1}s+L_{c1}C_1s^2+\frac{M_c}{R_1}s+M_cC_1s^2)v_{o1}+(\frac{M_c}{n_{12}R_2}s+\frac{M_cC_2}{n_{12}}s^2)v_{o2}=V_{in}N_1d, \tag{4.44}$$

$$(\frac{M_c}{R_1}s+M_cC_1s^2)v_{o1}+(1+\frac{L_{c2}}{R_2}s+L_{c2}C_2s^2+\frac{M_c}{n_{12}^2R_2}s+\frac{M_cC_2}{n_{12}^2}s^2)n_{12}v_{o2}=V_{in}N_1d. \tag{4.45}$$

The duty cycle-to-output transfer functions can be solved as:

$$\frac{v_{o1}}{d}=\frac{Num1}{Den}, \quad and \quad \frac{v_{o2}}{d}=\frac{Num2}{Den}, \tag{4.46}$$

where the numerators and denominator are

$$Num1=V_{in}N_1(1+\frac{L_{c2}}{R_2}s+L_{c2}C_2s^2), \tag{4.47}$$

$$Num2=\frac{V_{in}N_1}{n_{12}}(1+\frac{L_{c1}}{R_1}s+L_{c1}C_1s^2), \tag{4.48}$$

$$\begin{aligned} Den &= \left[1+\frac{M_c+L_{c1}}{R_1}s+(M_c+L_{c1})C_1s^2\right]\left[1+\frac{M_c+n_{12}^2L_{c2}}{n_{12}^2R_2}s+\frac{(M_c+n_{12}^2L_{c2})C_2}{n_{12}^2}s^2\right] \\ &= -\left[\frac{M_c}{R_1}s+M_cC_1s^2\right]\left[\frac{M_c}{n_{12}^2R_2}s+\frac{M_cC_2}{n_{12}^2}s^2\right]. \end{aligned} \tag{4.49}$$

Equations (4.47) and (4.48) show that the complex zeros of the duty cycle-to-output transfer functions are decided by the leakage inductances of the coupled inductors. The leakage inductances are in turn dependent on the coupling coefficient. The larger the coupling coefficient, the smaller the leakage inductances. This explains why the complex zeros move to high frequency as the coupling coefficient increases. As for the complex poles, the situation is more complicated, but some interesting results can still be extracted if certain assumptions are made.

The denominator is a 4th order polynomial. To investigate the variation of the complex poles, the coefficient of s^4 term is shown as follows:

$$s^4: \quad \left[L_{c1}L_{c2} + \frac{M_c L_{c1}}{n_{12}^2} + M_c L_{c2} \right] C_1 C_2. \tag{4.50}$$

First assuming the output filter inductors are loosely coupled, *i.e.*,

$$L_{c1} >> M_c, \qquad and \qquad L_{c2} >> M_c, \tag{4.51}$$

Eq. (4.50) can be approximated as:

$$s^4: \quad L_{c1}L_{c2}C_1C_2, \tag{4.52}$$

and the resonant frequencies of the complex poles are

$$\omega_{pt1} = \frac{1}{\sqrt{L_{c1}C_1}} \qquad and \qquad \omega_{pt2} = \frac{1}{\sqrt{L_{c2}C_2}}, \tag{4.53}$$

which are similar to the case when there is no coupling between the output filter inductors

as discussed in Sec. 4.3.1.

Now assuming the output filter inductors are tightly coupled, *i.e.*,

$$M_c >> L_{c1}, \quad and \quad M_c >> L_{c2}, \tag{4.54}$$

Eq. (4.50) can be approximated as:

$$s^4: \quad M_c(L_{c1} + n_{12}^2 L_{c2}) \frac{C_1 C_2}{n_{12}^2}. \tag{4.55}$$

The duty cycle-to-output transfer functions have two pairs of complex poles. One pair can be viewed as the resonance of the mutual inductance, which is approximately equal to the magnetizing inductance in this case, and the parallel combination of the output filter capacitors, while the other pair can be viewed as the resonance of the total leakage inductance and the series combination of the output filter capacitors:

$$\omega_{pt1} = \frac{1}{\sqrt{M_c(C_1 + \frac{C_2}{n_{12}^2})}}, \tag{4.56}$$

$$\omega_{pt2} = \frac{1}{\sqrt{(L_{c1} + n_{12}^2 L_{c2}) \frac{C_1 C_2}{n_{12}^2 C_1 + C_2}}}. \tag{4.57}$$

Equations (4.56) and (4.57) clearly explain why one pair of complex poles stay relatively fixed and another pair of complex poles move to high frequency as the coupling

coefficient is increased as shown in Fig. 4.6. Since the mutual inductance is much larger than the leakage inductances, it can be considered approximately equal to the magnetizing inductance, which changes little under the condition given in Eq. (4.54). Therefore, the corresponding resonant frequency, ω_{pt1}, does not change much. ω_{pt2} depends on the total leakage inductance, which is, in turn, very strongly dependent on the coupling between the output filter inductors. A large coupling coefficient, k, will yield small leakage inductance, resulting in high ω_{pt2}.

4.4 Prediction of Audio Susceptibilities and Output Impedances

In addition to the duty cycle-to-feedback transfer function, audio susceptibilities and output impedances are also important quantities for a dc-dc converter. Audio susceptibilities describe the rejection of the line disturbance, whereas the output impedances describe the rejection of the load disturbances, just like a single-output converter. One unique feature of multiple-output converters is that any output voltage is dependent not only on its own load current, which is characterized by the output impedance, but also on the other load current, which is characterized by transimpedance. In this section, the audio susceptibility and the output impedances, including

transimpedances, are derived and experimentally verified.

The circuit parameters used to generate all the audio susceptibilities, output impedances, output transimpedances, and loop gain are given in Table 4.3.

4.4.1 Open-loop Audio Susceptibilities and Output Impedances

The small-signal circuit model demonstrated in Fig. 4.2 fully describes the small-signal behavior. By using the circuit simulators, such as PSpice and Saber, all the small-signal transfer functions can be obtained. When discussing audio susceptibilities and output impedances, however, it is more convenient to represent the system using a block diagram. Besides, the block diagram is more suitable when using system simulators, such as Easy 5 and Matlab. Figure 4.8 shows the small-signal block diagram of a dual-output converter with weighted voltage control and coupled inductors. Each open-loop transfer function is defined and derived as follows.

The duty cycle-to-output transfer functions have been derived in Sec. 4.2, and are given here again for completeness:

$$G_{vdi} \equiv \frac{v_{oi}}{d} = \frac{Num(G_{vdi})}{Den}, \qquad i = 1, 2. \tag{4.58}$$

The audio susceptibilities, or line-to-output transfer functions:

$$G_{vi} \equiv \frac{v_{oi}}{v_{in}} = \frac{Num(G_{vi})}{Den}, \qquad i = 1, 2. \tag{4.59}$$

The output impedance transfer functions:

$$Z_{oi} \equiv \frac{v_{oi}}{i_{oi}} = \frac{Num(Z_{oi})}{Den}, \qquad i = 1, 2. \tag{4.60}$$

The output transimpedance transfer functions:

$$Z_{oij} \equiv \frac{v_{oi}}{i_{oj}} = \frac{Num(Z_{oij})}{Den}, \qquad i, j = 1, 2, \qquad i \neq j. \tag{4.61}$$

The denominator of each transfer function is the characteristic equation of the system, which is therefore invariant. The transfer functions differ from each other by numerators. The analytical expressions of the denominators and the numerators are summarized in Table 4.1. Figure 4.9 shows the open-loop audio susceptibility transfer functions. Figure 4.10 shows the open-loop output impedance transfer functions. Figure 4.11 shows the open-loop output transimpedance transfer functions. It is interesting to notice that the expressions of the output transimpedances $Z_{o12}(s)$ and $Z_{o21}(s)$ are identical, *i.e.*,

$$Z_{oij} \equiv Z_{oji}, \qquad i, j = 1, 2, \qquad i \neq j. \tag{4.62}$$

This can be explained by examining the relationship between the two outputs from the small-signal circuit model in Fig. 4.2. Since the power stage transformer can be approximated as an ideal transformer, all power channels are virtually decoupled from

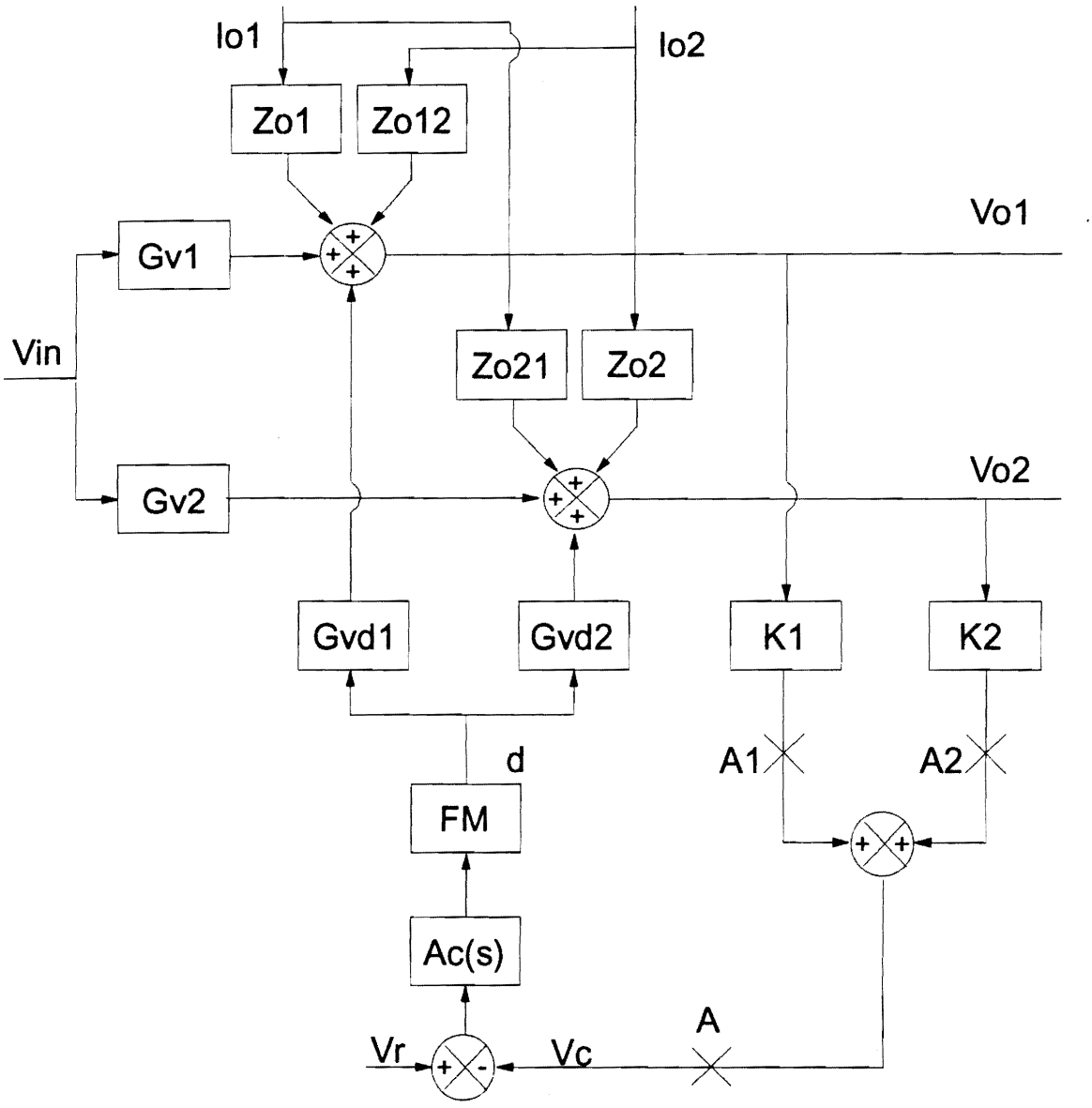


Fig. 4.8. Small-signal block diagram. *The analytical expression of each transfer function in the block diagram is given in Table 4.1. The closed-loop transfer functions, such as closed-loop audios and output impedances can be easily derived.*

Table 4.1. Analytical expressions of the open-loop transfer functions.

Den	$[1+(R_{C1}C_1+\frac{L_1}{R_1}+R_{L1}C_1)s+L_1C_1s^2][1+(R_{C2}C_2+\frac{L_2}{R_2}+R_{L2}C_2)s+L_2C_2s^2]-[\frac{M_{12}}{R_1}s+C_1M_{12}s^2][\frac{M_{12}}{R_2}s+C_2M_{12}s^2]$
Num(G_{vd1})	$V_{in}(1+R_{C1}C_1s)\{N_1[1+(R_{C2}C_2+\frac{L_2}{R_2}+R_{L2}C_2)s+L_2C_2s^2]-N_2[\frac{M_{12}}{R_2}s+C_2M_{12}s^2]\}$
Num(G_{vd2})	$V_{in}(1+R_{C2}C_2s)\{N_2[1+(R_{C1}C_1+\frac{L_1}{R_1}+R_{L1}C_1)s+L_1C_1s^2]-N_1[\frac{M_{12}}{R_1}s+C_1M_{12}s^2]\}$
Num(G_{v1})	$D(1+R_{C1}C_1s)\{N_1[1+(R_{C2}C_2+\frac{L_2}{R_2}+R_{L2}C_2)s+L_2C_2s^2]-N_2[\frac{M_{12}}{R_2}s+C_2M_{12}s^2]\}$
Num(G_{v2})	$D(1+R_{C2}C_2s)\{N_2[1+(R_{C1}C_1+\frac{L_1}{R_1}+R_{L1}C_1)s+L_1C_1s^2]-N_1[\frac{M_{12}}{R_1}s+C_1M_{12}s^2]\}$
Num(Z_{o1})	$(1+R_{C1}C_1s)\{[1+(R_{C2}C_2+\frac{L_2}{R_2}+R_{L2}C_2)s+L_2C_2s^2](sL_1+R_{L1})-\frac{s^2M_{12}^2}{R_2}[1+R_2C_2s]\}$
Num(Z_{o2})	$(1+R_{C2}C_2s)\{[1+(R_{C1}C_1+\frac{L_1}{R_1}+R_{L1}C_1)s+L_1C_1s^2](sL_2+R_{L2})-\frac{s^2M_{12}^2}{R_1}[1+R_1C_1s]\}$
Num(Z_{o12})	$sM_{12}(1+R_{C1}C_1s)(1+R_{C2}C_2s)$
Num(Z_{o21})	$sM_{12}(1+R_{C1}C_1s)(1+R_{C2}C_2s)$

each other. The only physical link between the power channels is through the mutual inductance of the coupled output filter inductors, $M_{12}=M_{21}=M$, which is the same, no matter in which power channel. As a result, the transimpedances are also identical, or the output transimpedances are reciprocal. The experimental results also confirm the theoretical derivation.

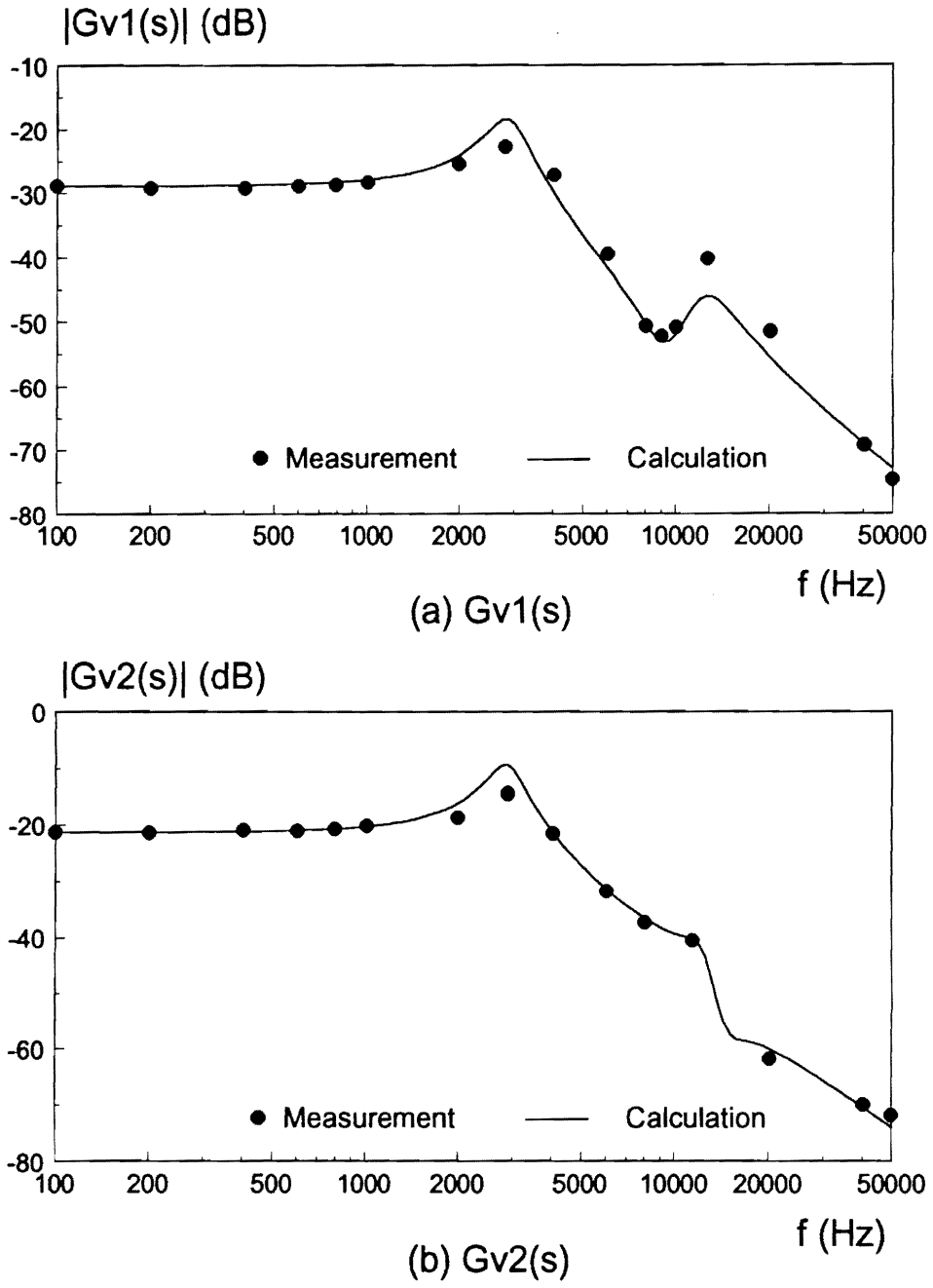


Fig. 4.9. Open-loop audio susceptibilities. *(a) Open-loop audio from the input to output 1. (b) Open-loop audio from the input to output 2. The open-loop audio susceptibilities are essentially the same as the open-loop duty cycle-to-output transfer functions except for the constant gains.*

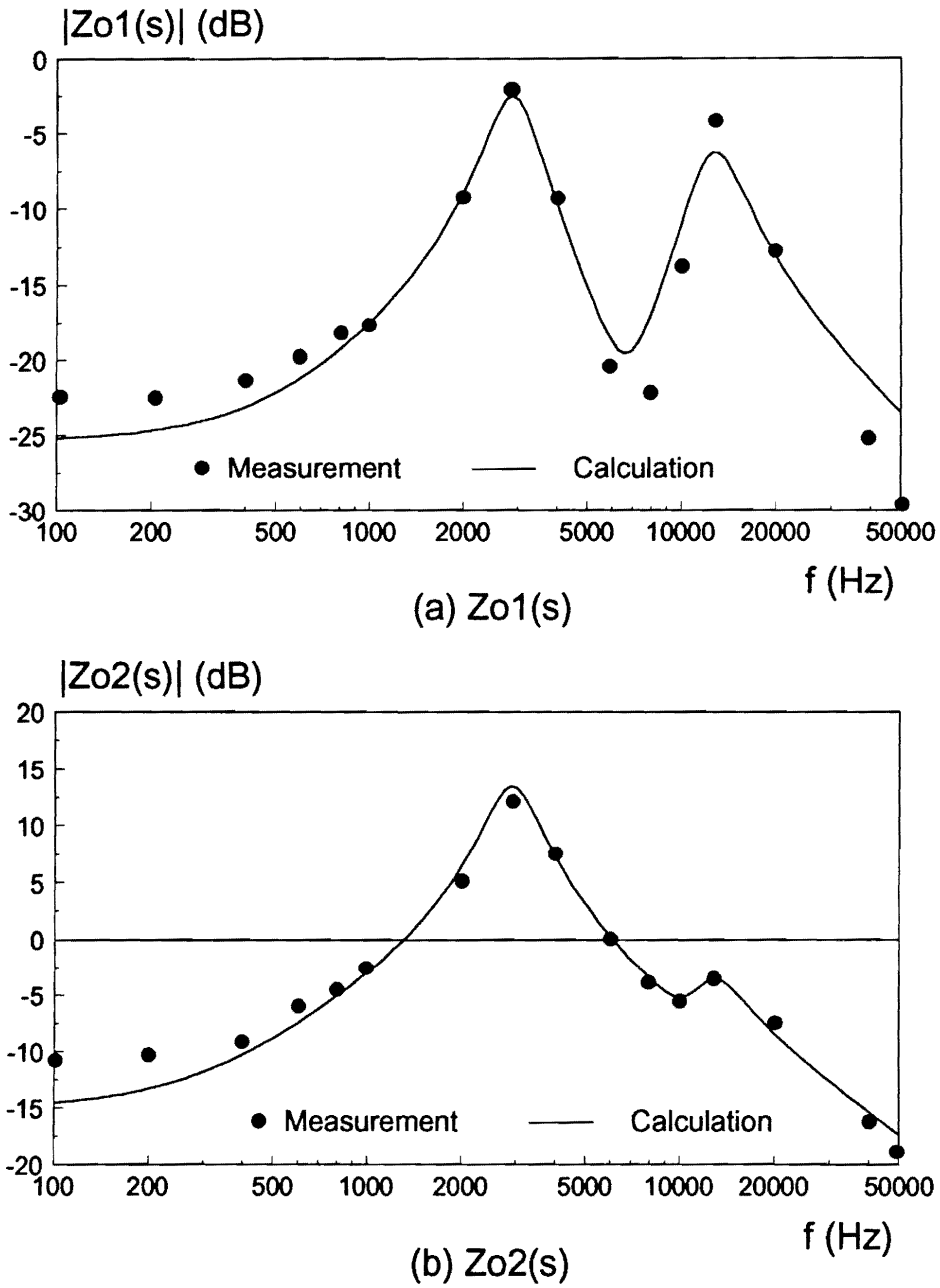


Fig. 4.10. Open-loop output impedances. *(a) Output impedance of output 1. (b) Output impedance of output 2. Due to coupling between the output inductors, the output impedances exhibit multiple peaks which occur at the resonant frequencies of the system complex poles.*

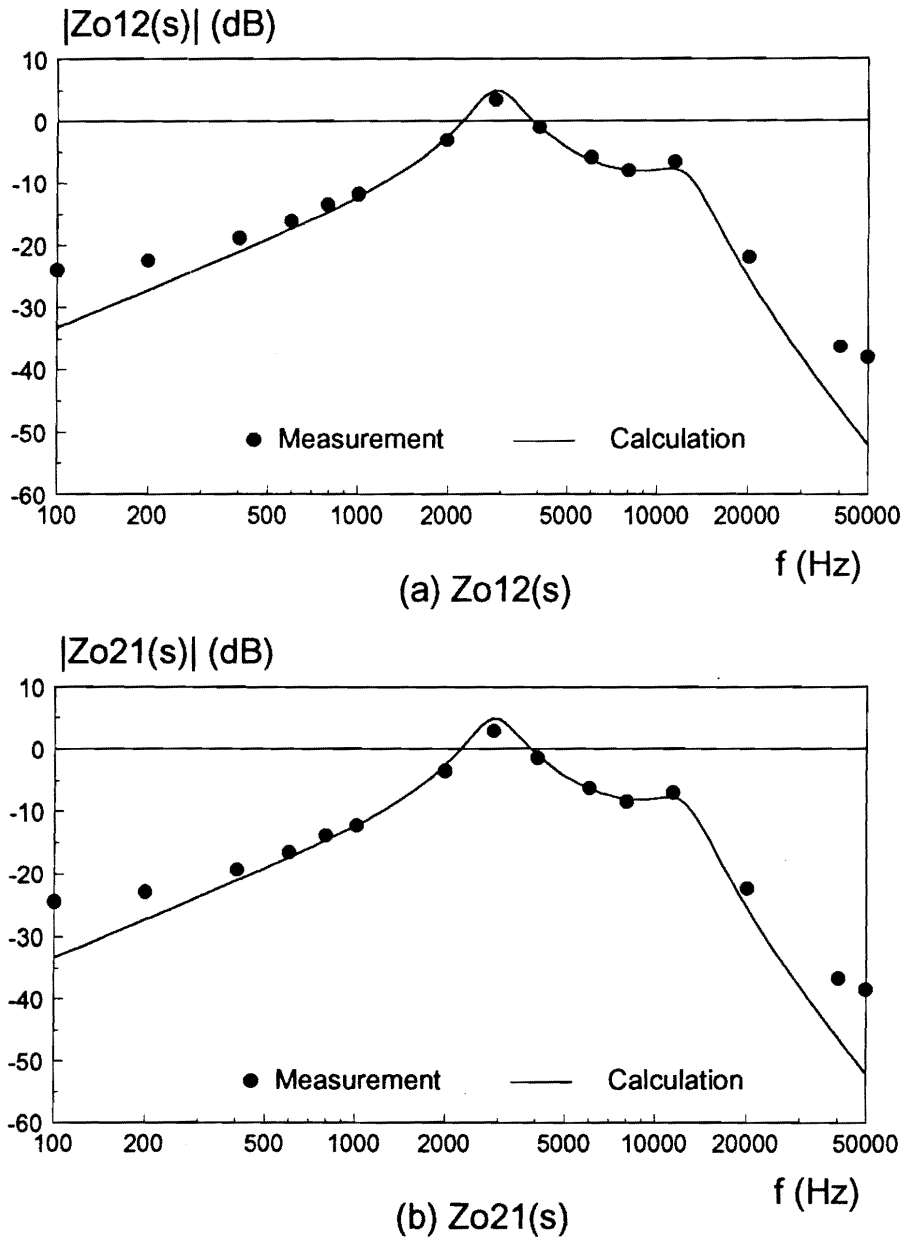


Fig. 4.11. Open-loop output transimpedances. *(a) Output transimpedance $Z_{o12}(s)$. (b) Output transimpedance $Z_{o21}(s)$. The output transimpedances are unique for the multiple-output converters. They characterize the dependence of the output voltages on the other load current. It is interesting to notice that $Z_{o12}(s)$ and $Z_{o21}(s)$ are reciprocal.*

4.4.2 Closed-Loop Audio Susceptibilities and Output Impedances

For a dc-dc converter, more important is the closed-loop small-signal behavior, which also affects the compensator design. When discussing closed-loop small-signal transfer functions, the loop gain is always used, which is defined by breaking the loop at point A in Fig. 4.8:

$$T = A_c F_m (K_1 G_{vd1} + K_2 G_{vd2}). \tag{4.63}$$

The so-defined loop gain can provide stability information and is convenient to use when performing compensator design. Since the product of each weighting factor, the duty cycle-to-output transfer function, the modulator gain, and the compensator transfer function often appear in the expressions of the closed-loop audio susceptibility and output impedance transfer functions, two additional loop gains are defined:

$$T_1 = A_c F_m K_1 G_{vd1}, \tag{4.64}$$

and

$$T_2 = A_c F_m K_2 G_{vd2}. \tag{4.65}$$

T_1 and T_2 happen to take the same form as the loop gain of the single output converter. It should be noticed that, however, each loop gain, T_1 or T_2, does not provide adequate stability information.

The analytical expression for each closed-loop transfer function is derived and

summarized in Table 4.2.

It can be seen that both the denominators and numerators of the analytical expressions of the closed-loop audio susceptibilities and output impedances include the compensator $A_c(s)$. This may lead to the incorrect conclusion that the wide bandwidth, which usually asks for high loop gain, does not improve dynamic regulation. In the following, the output impedance $Z_{o1}(s)$ is used to demonstrate how the high loop gain improves the dynamic characteristics.

The closed-loop output impedance $Z_{o1(CL)}(s)$ is derived as:

$$Z_{o1(CL)} = \frac{Z_{o1}(1+T_2) - \frac{K_2}{K_1} T_1 Z_{o21}}{1+T} \tag{4.66}$$

Assuming $|T_1|>>1$ and $|T_2|>>1$, $Z_{o1(CL)}(s)$ can be simplified as:

$$Z_{o1(CL)} \approx \frac{Z_{o1}T_2 - \frac{K_2}{K_1} T_1 Z_{o21}}{T} = \frac{K_2(G_{vd2}Z_{o1} - G_{vd1}Z_{o21})}{K_1 G_{vd1} + K_2 G_{vd2}} \tag{4.67}$$

The numerator of the closed-loop output impedance is the difference between the two terms. The first term $G_{vd2}Z_{o1}$ is caused by the output impedance of the V_{o1} power channel and $G_{vd1}Z_{o21}$ is caused by the output transimpedance between two power channels, which is due to the coupled inductors. Their difference results in the reduction of the output impedance. Physically, this can be explained by referring to the small-signal block diagram as given in Fig. 4.8. The current disturbance at $i_{o1}(s)$ is injected into the system through two paths: one through the output impedance $Z_{o1}(s)$, and the other through the output transimpedance $Z_{o21}(s)$. The effect of weighted voltage control tends

Table 4.2. Analytical expressions of the closed-loop transfer functions.

Audio Susceptibility 1	$G_{v1(CL)}$	$\frac{G_{v1}T_2 - \frac{K_2}{K_1}T_1G_{v2}}{1+T}$
Audio Susceptibility 2	$G_{v2(CL)}$	$\frac{G_{v2}T_1 - \frac{K_1}{K_2}T_2G_{v1}}{1+T}$
Output Impedance 1	$Z_{o1(CL)}$	$\frac{Z_{o1}(1+T_2) - \frac{K_2}{K_1}T_1Z_{o21}}{1+T}$
Output Impedance 2	$Z_{o1(CL)}$	$\frac{Z_{o2}(1+T_1) - \frac{K_1}{K_2}T_2Z_{o12}}{1+T}$
Transimpedance from i_{o2} to v_{o1}	$Z_{o12(CL)}$	$\frac{Z_{o12}(1+T_2) - \frac{K_2}{K_1}T_1Z_{o2}}{1+T}$
Transimpedance from i_{o1} to v_{o2}	$Z_{o21(CL)}$	$\frac{Z_{o21}(1+T_1) - \frac{K_1}{K_2}T_2Z_{o1}}{1+T}$
Loop Gain 1	T_1	$A_cF_mK_1G_{vd1}$
Loop Gain 2	T_2	$A_cF_mK_2G_{vd2}$
Total Loop Gain	T	$A_cF_m(K_1G_{vd1}+K_2G_{vd2})$

to cancel these two disturbances in the system. As a result, the output impedance is decreased by using coupled inductors and weighted-voltage control simultaneously.

It should be pointed out that if the coupled inductors are not employed, the second term including the output transimpedance will disappear, and consequently the reduction of the closed-loop output impedance will be far less effective. An interesting result is obtained by assuming there is no coupling between the output filter inductors, *i.e.*, $Z_{o21}=0$. The closed-loop output impedance becomes

$$Z_{o1(CL)}=Z_{o1}\frac{(1+T_2)}{1+T}\approx Z_{o1}\frac{K_2G_{vd2}}{K_1G_{vd1}+K_2G_{vd2}}=Z_{o1}\frac{1}{1+\dfrac{K_1G_{vd1}}{K_2G_{vd2}}} \tag{4.68}$$

To facilitate discussion, the closed-loop output impedance for the other power channel is also provided:

$$Z_{o2(CL)}=Z_{o2}\frac{(1+T_1)}{1+T}\approx Z_{o2}\frac{K_1G_{vd1}}{K_1G_{vd1}+K_2G_{vd2}}=Z_{o2}\frac{1}{1+\dfrac{K_2G_{vd2}}{K_1G_{vd1}}} \tag{4.69}$$

It can be seen that the closed-loop output impedances are mainly decided by the ratio of the weighting factors. Let us assume that the two power channels are identical and the outputs are equally weighted, then the closed-loop output impedance will be one half of the open-loop output impedances, or *6 dB* reduction in the closed-loop output impedances will take place. It can be concluded that reduction of the output impedance by using weighted voltage control is very limited. In addition, it is impossible to reduce the output impedances in both power channels. The reduction of the output impedance in one power channel is at the cost of increasing the output impedance in the other power

channel. On the other hand, if the coupled inductors are used, the closed-loop output impedance is dependent not only on the open-loop output impedance Z_{o1} but also on the open-loop transimpedance Z_{o21} (Eq. (4.69)). These two terms appear in the numerator of the closed-loop output impedance with opposite signs, which results in reduced output impedance. This shows one of the advantages of using coupled inductors.

Now assuming $|T_1|<<1$ and $|T_2|<<1$, then $Z_{o1(CL)}(s)$ can be simplified as:

$$Z_{o1(CL)} \approx Z_{o1}. \tag{4.70}$$

The closed-loop output impedance is basically the same as the open-loop output impedance; therefore, only under this circumstance the feedback does not have effect on load regulation.

Compared with single-output converter, where the closed-loop output impedance is directly surpressed by the high loop gain, the reduction of the closed-loop output impedance for the dual-output converter is not directly decided by the loop gain, but rather by the difference between $G_{vd2}Z_{o1}$ and $G_{vd1}Z_{o21}$, Eq. (4.69). This improvement of the output impedance, nevertheless, is under the condition $|T_1|>>1$ and $|T_2|>>1$. This condition means that the loop gain should be high over the frequency range of interest. If the loop gain is too low, the closed-loop output impedance will simply take the value of the open-loop output impedance.

There is another case worth noticing: that is, when the loop gain is comparable to unity, which occurs in the vicinity of the cross-over frequency of the loop gain, the closed-loop output impedance has to be decided from Eq. (4.66). Depending on the values of the

open-loop duty cycle-to-output transfer functions, output impedances, and output transimpedances, the closed-loop output impedance can be greater or smaller than its open-loop counterpart. Since the situation is far more complicated than the previous two, it is hard to draw a general conclusion, and therefore this situation should be avoided by closing the loop at a high frequency. Later on, an example will be given to demonstrate a case in which the closed-loop output impedance is greater than the open-loop output impedance.

Figure 4.12 shows the closed-loop output impedances for the same converter with the same operation conditions. The compensator consists of an integrator plus two poles and two zeros:

$$A_{c1}(s) = \frac{K_I}{s} \frac{(s+s_{zc1})(s+s_{zc2})}{(s+s_{pc1})(s+s_{pc2})} \tag{4.71}$$

The design of the compensator will be elaborated on in the next section. The closed-loop output impedances, compared with their open-loop counterparts, are reduced. Unlike in the case of its single-output counterpart, where the output impedance can be nulled at dc by using an integrator in the loop gain, the output impedances of the dual output converter always have finite values at dc, even when an integrator is applied in the compensator.

The same argument can be applied to the output transimpedances and audio susceptibilities, and the same results can be obtained. It is interesting to notice that the closed-loop audio susceptibilities, as shown in Fig. 4.13, can be nulled at dc, since the

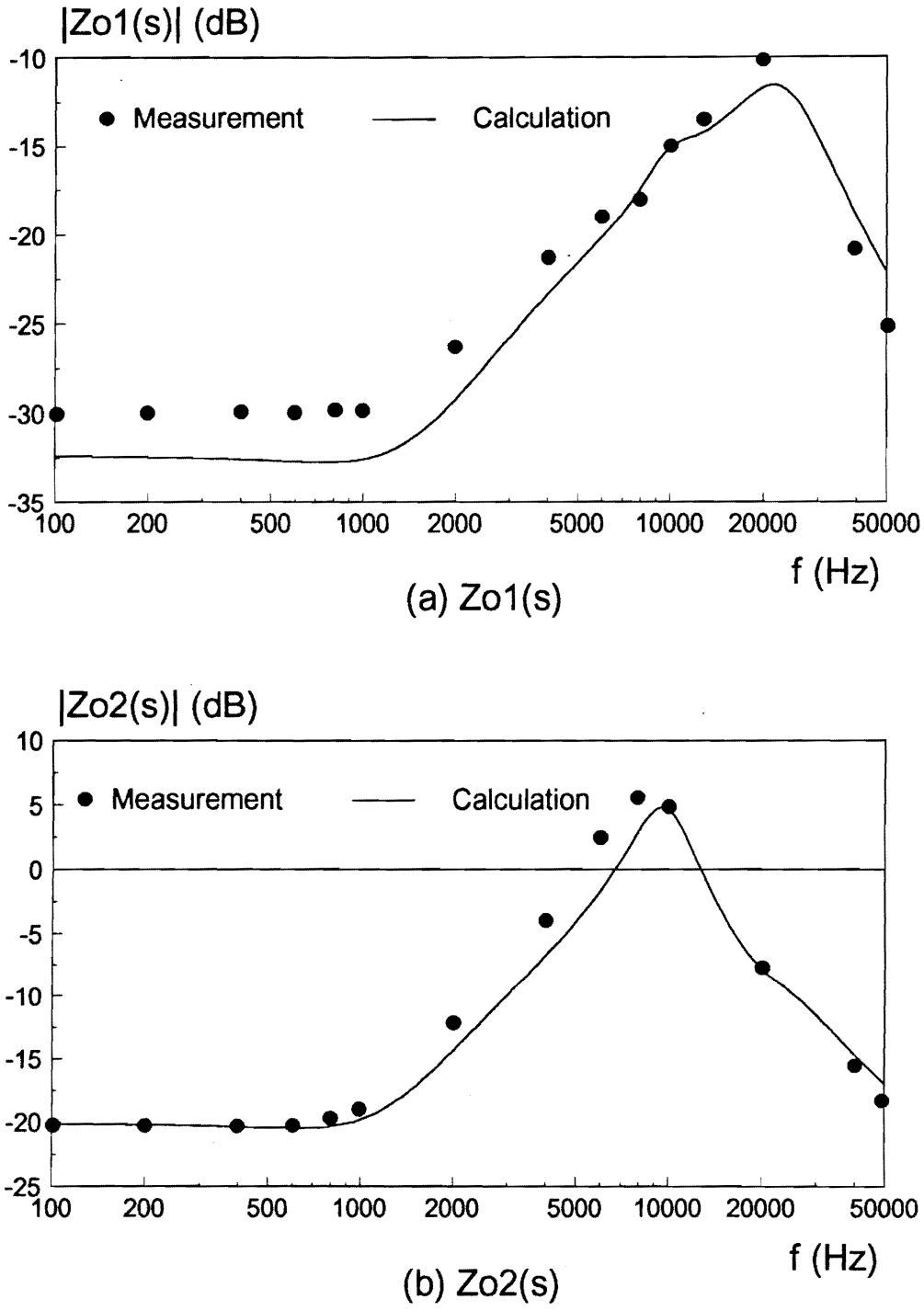


Fig. 4.12. Closed-loop output impedances. *The closed-loop output impedances are reduced by designing the compensator properly. Unlike the single output converter, the closed-loop output impedances have finite values at dc.*

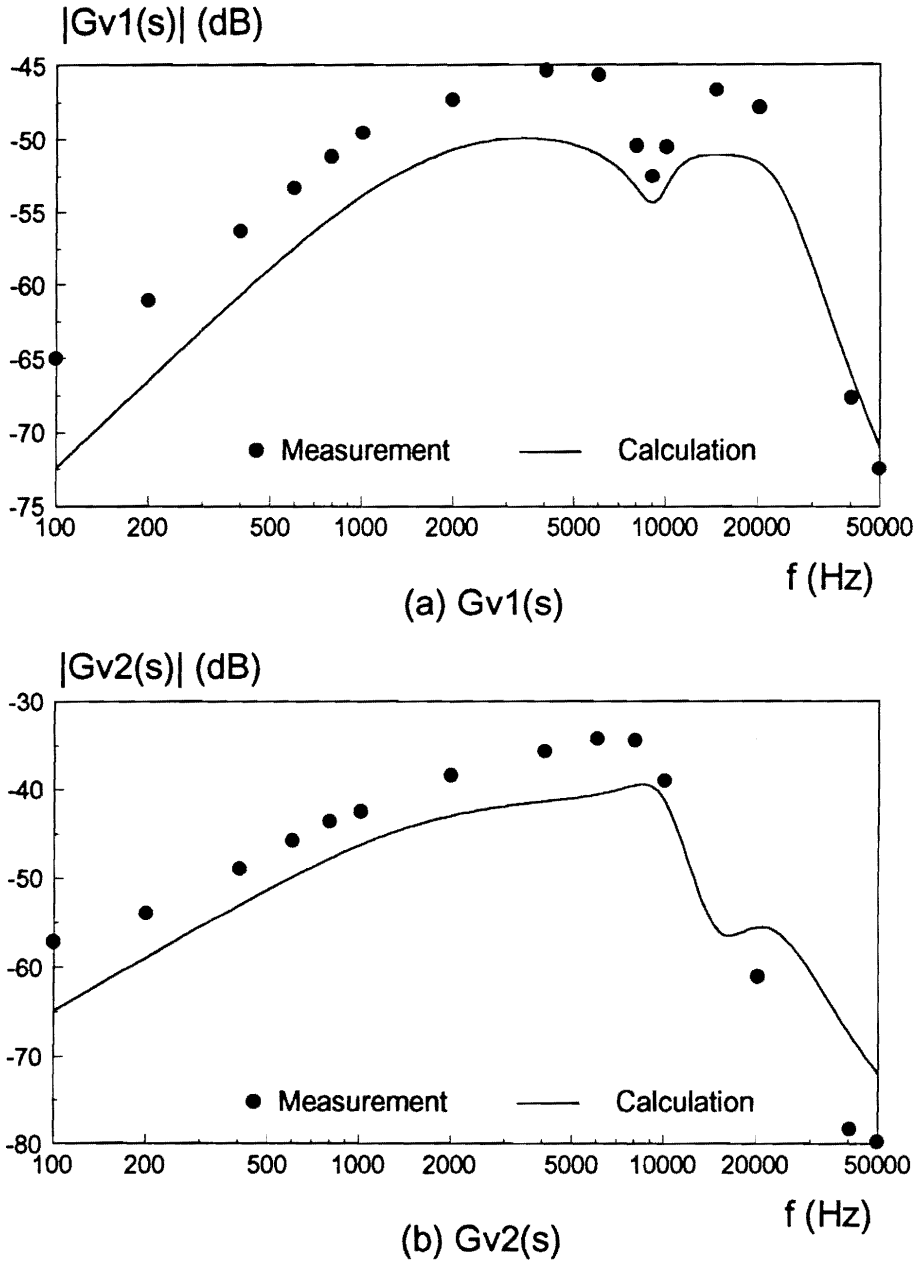


Fig. 4.13. Closed-loop audio susceptibilities. *Reduction of the audio susceptibilities is more significant compared with the closed-loop output impedances. This explains why the dual-output converter is more robust against the line disturbance than against the load disturbances.*

numerator of each audio susceptibility is the difference of two terms, *i.e.*,

$$G_{v1(CL)} = \frac{G_{v1}T_2 - \frac{K_2}{K_1}T_1 G_{v2}}{1+T} = \frac{K_2(DN_1N_2V_{in} - DN_1N_2V_{in})}{(K_1N_1 + K_2N_2)V_{in}} = 0, \qquad (4.72)$$

which is consistent with the fact that the dual-output converter is very robust to the line voltage disturbance. Again, the drastic reduction of the closed-loop audio susceptibility is not the direct effect of high loop gain, but rather the effect of weighted-voltage control. Referring to the small-signal block diagram as given in Fig. 4.8, it can be observed that the perturbance from the line voltage, v_{in}, is also injected into the system through two paths: one through the open-loop audio susceptibility of power channel one, $G_{v1}(s)$, and the other through the open-loop audio susceptibility of power channel two, $G_{v2}(s)$. The net effects tend to cancel each other. As a result, the closed-loop audio susceptibility is drastically decreased. The conclusion made here is diferent from what is reported in [F10], where the reduction of the closed-loop audio susceptibility has been attributed to the high loop gain of the compensator. Actually, only one audio propagation path was accounted for in [F10].

From the above analyses, it can be concluded that the compensator should be designed so that the cross-over frequency be as high as possible and the loop gain be high over the frequency range of interest to improve the line and load regulations, provided that the compensated system has enough stability margin.

To support the above conclusions, another compensator with an integrator only is applied:

$$A_{c2}(s) = \frac{K_I}{s}. \tag{4.73}$$

The loop gains for both cases are plotted in Fig. 4.14. It can be seen that using an integrator results in a much lower cross-over frequency and a much lower loop gain compared with using the compensator with two zeros and three poles, Eq. (4.71). Figure 4.15 shows the open-loop output impedance and closed-loop output impedances employing both types of compensators. The comparison clearly shows that the higher loop gain results in a smaller output impedance. For the lower loop gain, which corresponds to a lower cross-over frequency, the closed-loop output impedances have even higher peaking than the open-loop output impedances. This is because the value of the loop gain around the resonant frequency of the first pair of power stage complex poles is close to unity, but the phase delay is close to -180°. The magnitude of the denominator in Eq. (4.66) is very small, resulting in higher closed-loop output impedances. Figure 4.16 shows the large signal simulation of the output responses to a step load current change for two different types of compensators. Again, the comparison is favorable to the compensator which yields higher cross-over frequency and higher loop gain.

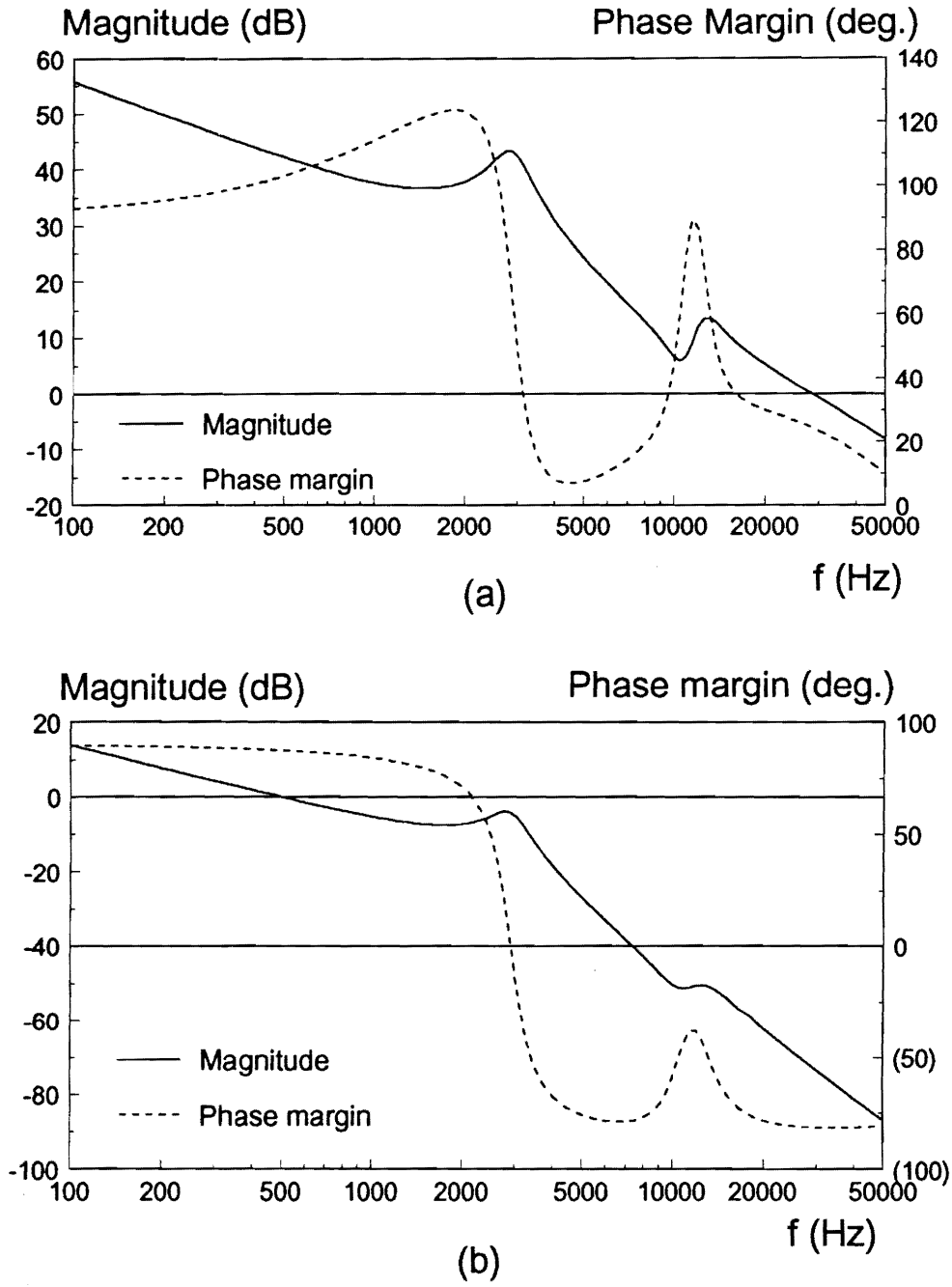


Fig. 4.14. Loop gain using different compensators. *The compensator of an integrator plus 2 poles and 2 zeros (a) results in a higher crossover and a higher loop gain than the compensator of an integrator (b).*

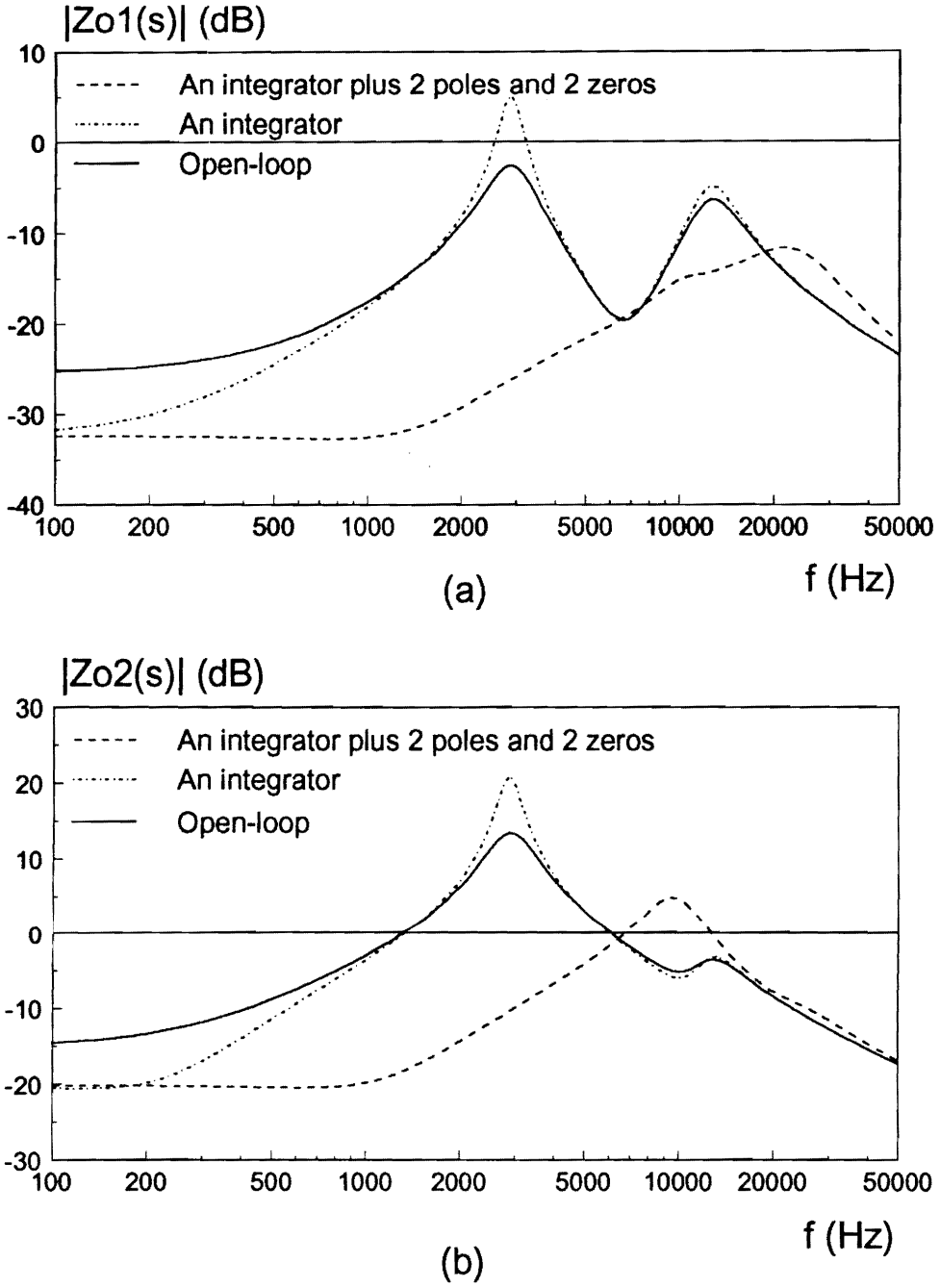
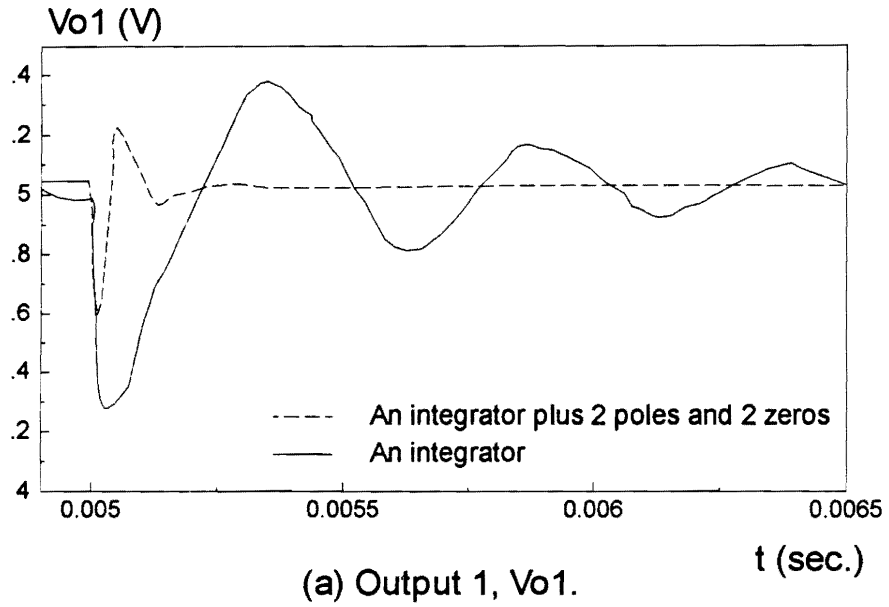
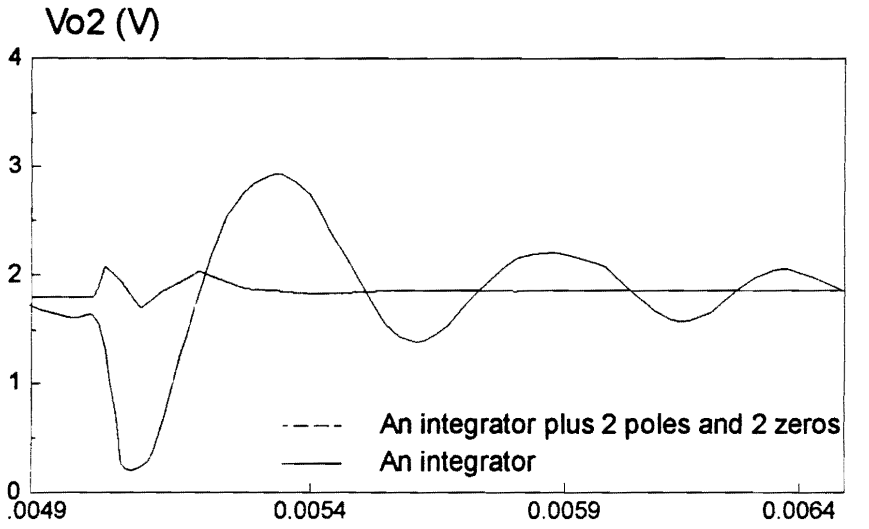


Fig. 4.15. Comparison of output impedances using different compensators. *Three curves shown here are open-loop output impedances and closed-loop output impedances with different types of compensator. (a) Output 1; (b) Output 2.*



(a) Output 1, Vo1.



(b) Output 2, Vo2.

Fig. 4.16. Transient responses to a step load change at output 1. *The higher loop gain yields smaller output impedances, and consequently faster response with smaller over/under shoots.*

4.5 Design Considerations

It can be seen from the above analyses that it is desirable to have high cross-over frequency and high loop gain to improve dynamic responses, provided that the system has enough stability margin. The compensator design is based on the system duty cycle-to-output (-feedback) transfer functions which can take different form for different circuit parameters. From the discussion of Sec. 4.3, the duty cycle-to-output (-feedback) transfer functions fall into two categories: (1) those with interlaced complex poles and zeros, and (2) those with non-interlaced poles and zeros. The converter with WVC belongs only to category (1). For the converter with coupled inductors only, one duty cycle-to-output transfer function falls into (1), and the other transfer function falls into (2). As for the converter with both WVC and coupled inductor, the transfer function can be of either type, depending on the converter parameters, coupling coefficient, and weighting factors. In this section, the compensator designs for different cases are discussed.

4.5.1 Compensator Design for the Pole-Zero Interlaced System

For a converter whose duty cycle-to-feedback transfer function has interlaced complex poles and zeros, the system behavior at both low and high frequencies is similar to that of the single output converter. The major difference is in the middle frequency

range, where the characteristics show multiple peaks, as can be seen in Figs. 4.3, 4.4(a) and 4.5(a). No matter how the poles and zeros move, the phase never exceeds -180°. As a result, the commonly used compensator with an integrator plus two poles and two zeros:

$$A_c(s) = \frac{K_I}{s} \frac{(s+s_{zc1})(s+s_{zc2})}{(s+s_{pc1})(s+s_{pc2})} \tag{4.74}$$

can be employed. First, the loop gain crossover frequency, f_c, is set according to the resonant frequencies of the duty cycle-to-output (-feedback) transfer function, and the given switching frequency, f_s. From the analyses in the last section, it is possible to improve the closed-loop dynamic characteristics with high loop gain. If the loop gain is very low, closed-loop control will not improve the dynamic characteristics. If the loop gain is comparable to unity, the closed-loop dynamic performance could be worse than the open-loop dynamic performance. Since the peakings of open-loop audio susceptibilities and the output impedances occur at the resonant frequencies of the complex poles, the close-over frequency, f_c, shall be chosen higher than these resonant frequencies. However, the cross-over frequency cannot be pushed up arbitrarily. It is also limited by the switching frequency. It is suggested that the cross-over frequency be set so as not to exceed $f_c = f_s/5 - f_s/3$.

The design criterion for the compensator poles and zeros is to make sure that the closed-loop system has high loop gain before the cross-over frequency while maintaining enough stability margin. One compensator pole is placed to cancel the equivalent ESR zero. The other one is placed at approximately one half of the switching frequency to attenuate the switching noise in the modulator. The amplitude of the loop gain and

stability margin are determined by the placement of the compensator zeros. To achieve a high loop gain at the low frequency range, a pole is placed at the origin. The first compensator zero is placed slightly below the low frequency complex pole $s_{zc1} \leq \omega_{pt1}$. The position of the second compensator zero determines loop gain over the mid-frequency range and stability margin. There can be several possible placements of the second zero: (1) $\omega_{pt1} < s_{zc2} < \omega_{zt1}$; (2) $\omega_{zt1} < s_{zc2} < \omega_{pt2}$; (3) $\omega_{pt2} < s_{zc2} < \omega_c$. These three methods are to be investigated .

The asymptotes of the duty cycle-to-feedback transfer function, compensator, and loop gain for all three different designs are sketched in Fig. 4.17 - Fig. 4.19. To make a fair comparison, the crossover frequency is the same.

It can be seen that the third design, i.e., placing the second compensator zero, s_{zc2}, after the second pair of complex poles of the duty cycle-to-feedback transfer function, ω_{pt2}, yields the highest overall loop gain for the same crossover frequency. Therefore, it is suggested that

$$\omega_{pt2} \leq s_{zc2} \leq \omega_c. \tag{4.75}$$

Furthermore, the second compensator zero, s_{zc2}, should be placed close to the second pair of the complex poles of the duty cycle-to-feedback transfer function to ensure enough phase margin.

A potential problem for this design is that if the first pair of complex poles, ω_{pt1}, and the complex zeros, ω_{zt}, are widely separated, the phase can approach -180°.

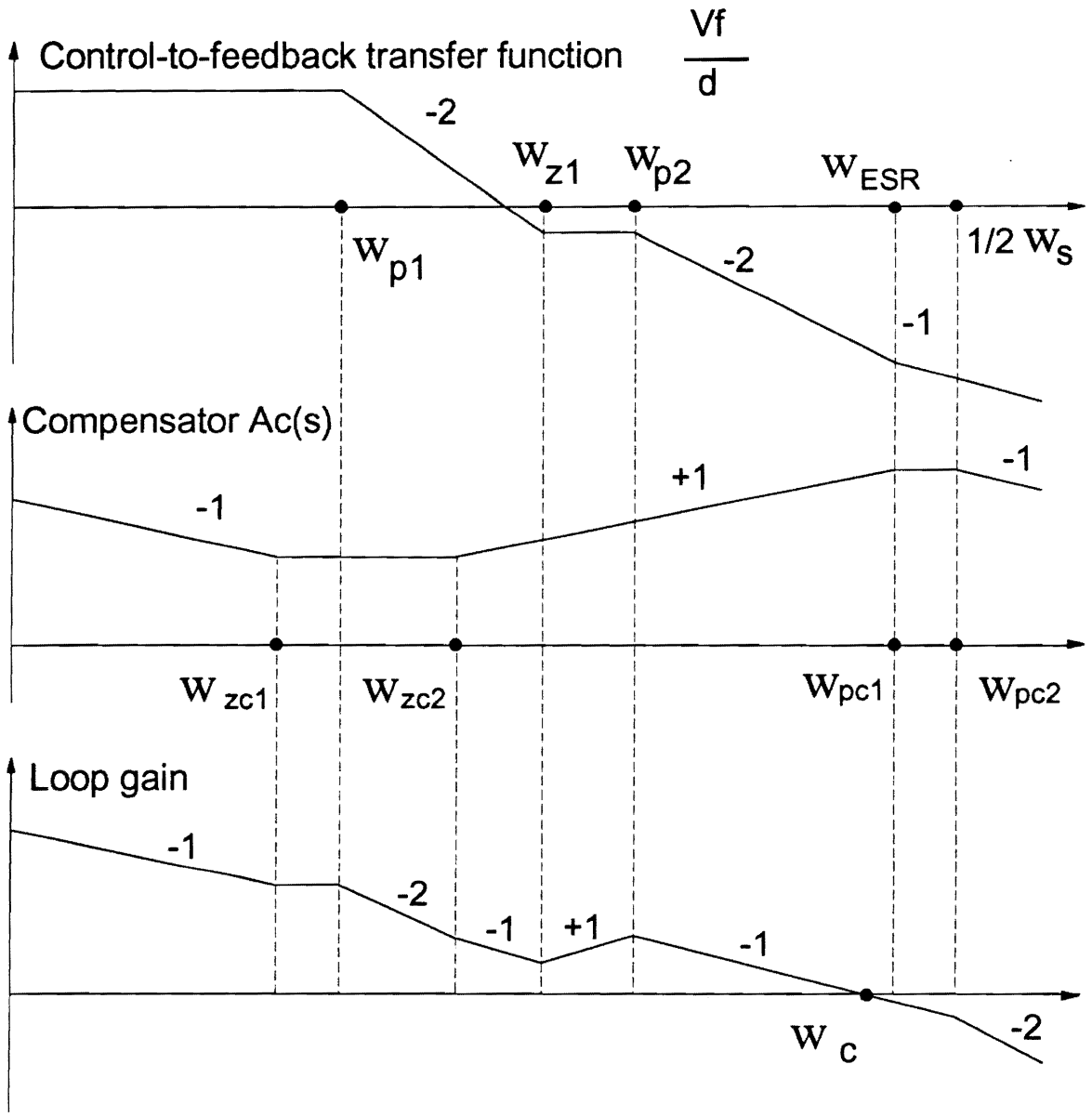


Fig. 4.17. Compensator design for the system with interlaced complex poles and zeros (1). The second compensator zero is placed between the first complex poles and the complex zeros, or $\omega_{pt1} < s_{zc2} < \omega_{zt1}$.

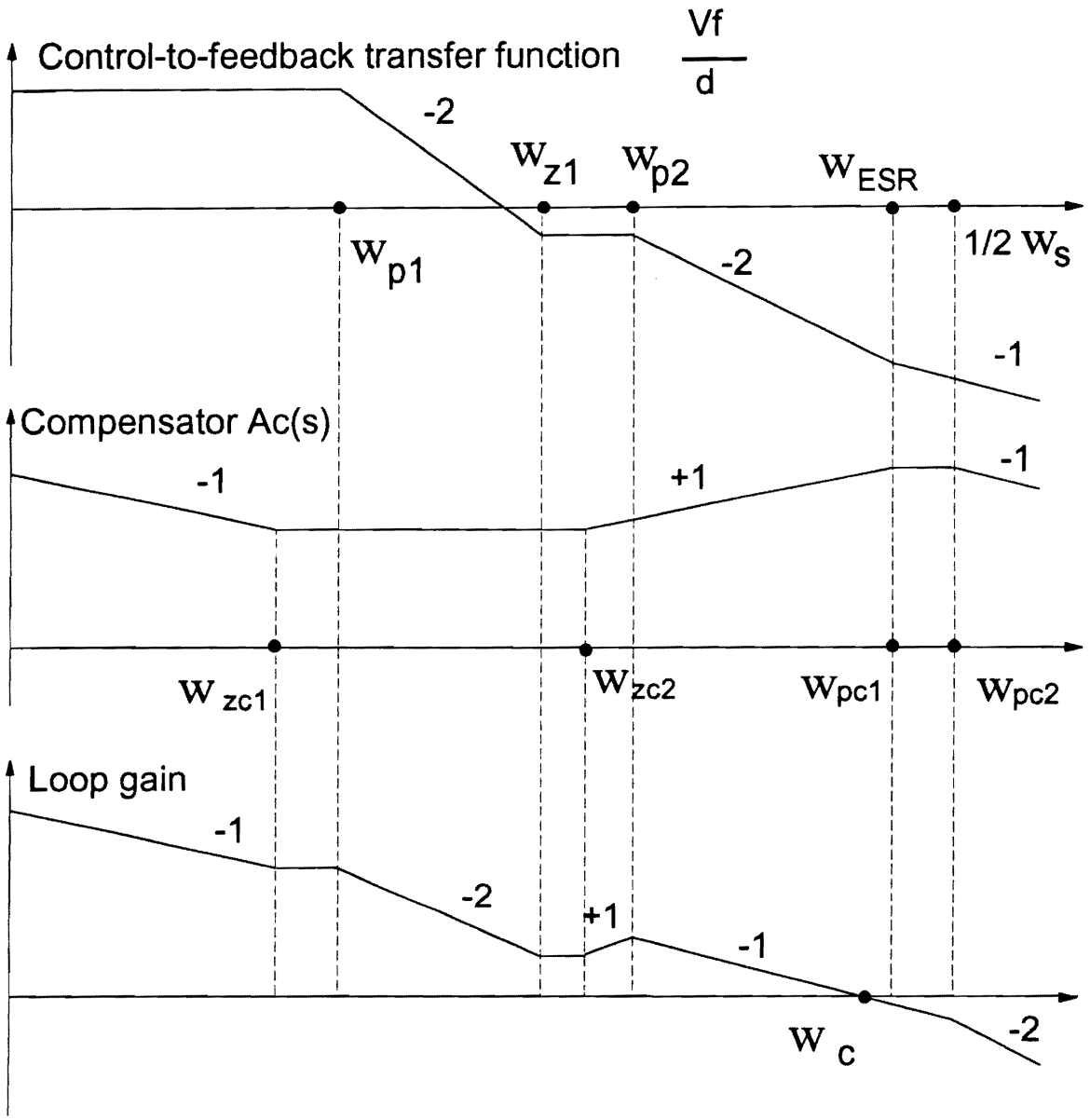


Fig. 4.18. Compensator design for the system with interlaced complex poles and zeros (2). The second compensator zero is placed between the complex zeros and the second pair of complex poles, or $\omega_{zt1} < s_{zc2} < \omega_{pt2}$.

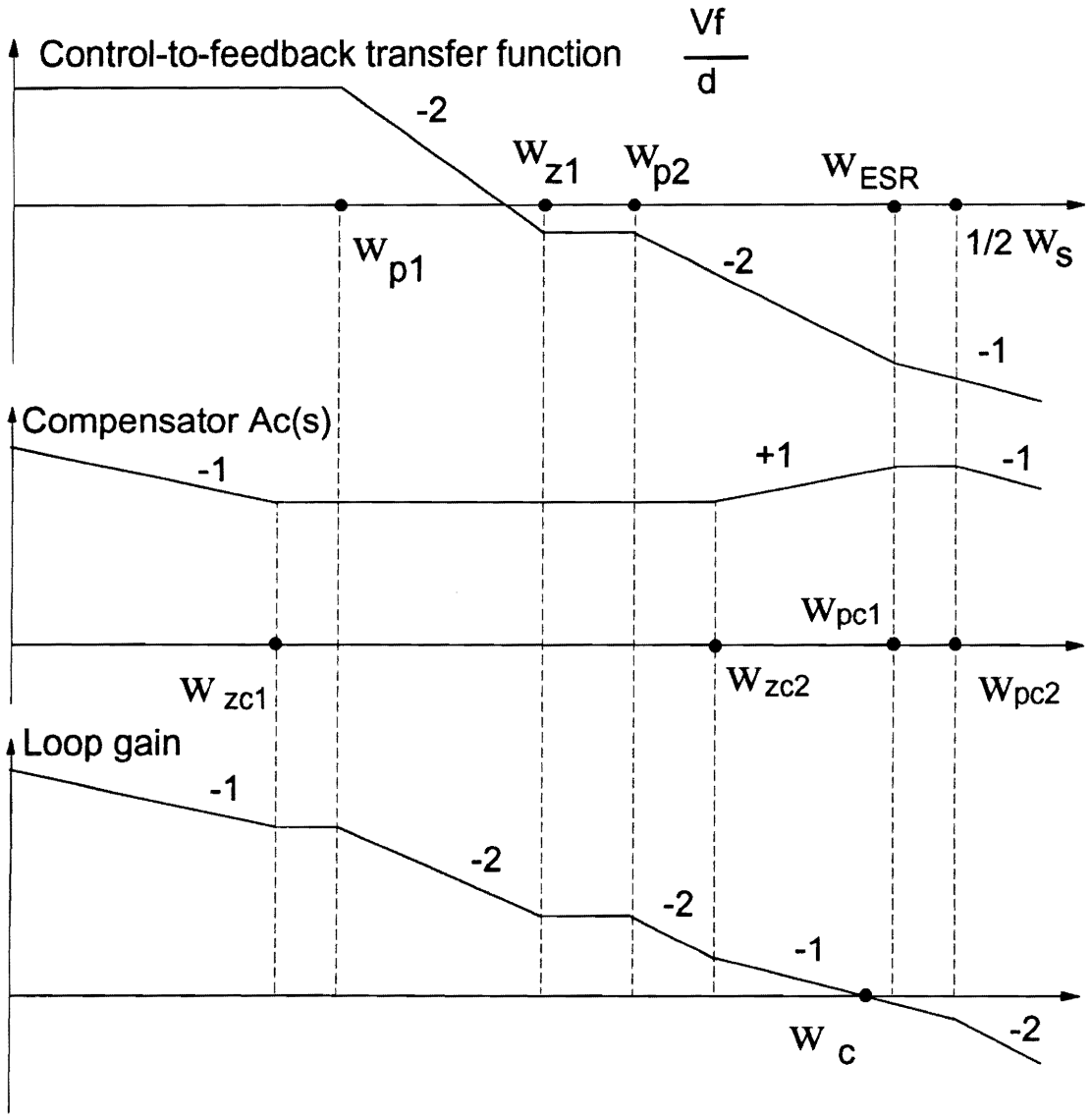


Fig. 4.19. Compensator design for the system with interlaced complex poles and zeros (3). The second compensator zero is placed after the second pair of the complex poles, or $\omega_{pt2} < s_{zc2} < \omega_c$.

Although this occurs at low frequency ($<\omega_{zl}$), and the corresponding loop gain is usually very high and will not cause stability problem even at low line for normal operation, it may cause oscillation during start-up if the control circuitry is not properly designed.

If the second pair of the complex poles, ω_{pt2}, is located very close to or even higher than the selected crossover frequency, ω_c, the second compensator zero should be placed between the first pair of the complex poles, ω_{pt1}, and the complex poles, ω_{zt}, to ensure that the system has enough stability margin.

4.5.2 Compensator Design for the Pole-Zero Non-Interlaced System

For a converter whose transfer function has non-interlaced poles and zeros, the phase delay can exceed -180° because of two pairs of consecutive complex poles, as shown in Figs. 4.4(b) and 4.5(b). If the second pair of complex poles is followed immediately by a pair of complex zeros, excessive phase delay will not occur. Therefore, the previously discussed 2-zero-3-pole compensator can still be used. However, if the second pair of complex poles and the complex zeros are widely separated and the phase delay exceeds -270°, the system crossover frequency has to be chosen below the resonant frequency of the first pair of complex poles. In this case, a single integrator with a relatively low gain is suitable for the compensator, Fig. 4.20. Apparently, the closed-loop performances of the converter with noninterlaced poles and zeros are inferior to those of

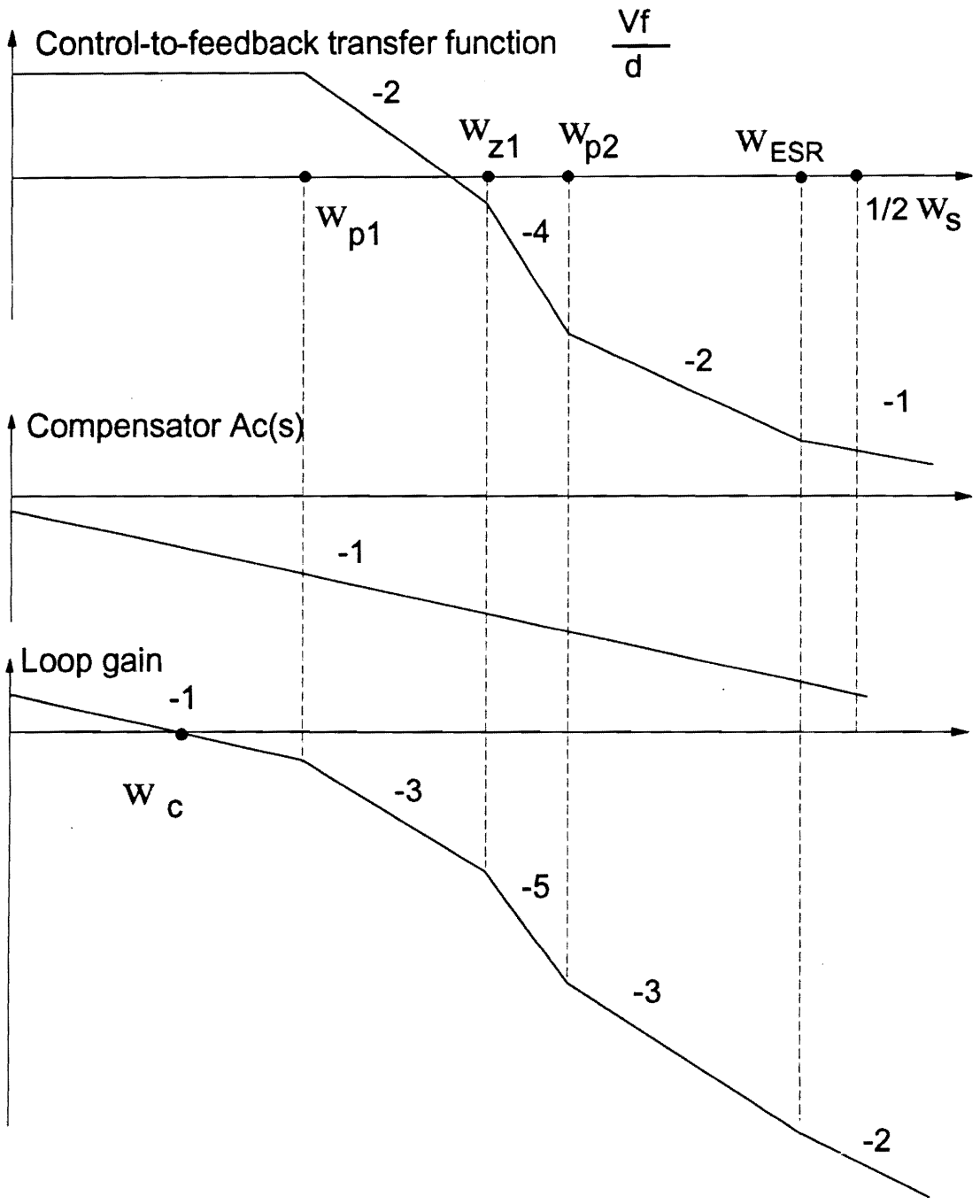


Fig. 4.20. Compensator design for the system with non-interlaced complex poles and zeros. *Since the non-interlaced complex poles and zeros are widely separated, the phase drops drastically at a relatively low frequency. Therefore, the control loop has to be closed at low frequency.*

the converter with interlaced poles and zeros as discussed in the last section. Therefore, this situation should be avoided by all means.

4.5.3 Power Stage Design Considerations

From the above discussion, it is obvious that a system with interlaced complex poles and zeros is more desirable than a system with non-interlaced poles and zeros. Since the positions of the poles and zeros of the power stage duty cycle-to-feedback transfer function are dependent on the coupling coefficient and the weighting factors, the degree of coupling can be adjusted so that the duty cycle-to-feedback transfer function may have interlaced poles and zeros.

If the resonant frequencies of the two output filters are separated, the low-frequency complex poles are relatively fixed. Then the system transfer function can be approximately written into the pole-zero form:

$$G_{vd}(s) = \frac{V_{in}K_B(1+\frac{s}{s_{zt}})(1+\frac{s}{\omega_{zt}Q_{zt}}+\frac{s^2}{\omega_{zt}^2})}{(1+\frac{s}{\omega_{pt1}Q_{pt1}}+\frac{s^2}{\omega_{pt1}^2})(1+\frac{s}{\omega_{pt2}Q_{pt2}}+\frac{s^2}{\omega_{pt2}^2})}, \tag{4.76}$$

where

$$K_B = K_1N_1 + K_2N_2, \tag{4.77}$$

and the poles and zeros are approximated as:

$$s_{zt} \approx \frac{K_1N_1 + K_2N_2}{K_1N_1R_{c1}C_1 + K_2N_2R_{c2}C_2}, \tag{4.78}$$

$$\omega_{zt}^2 \approx \frac{K_1N_1 + K_2N_2}{(1-k)(K_1N_1L_2C_2 + K_2N_2L_1C_1)}, \tag{4.79}$$

$$\omega_{pt1}^2 \approx \frac{1}{L_1(C_1 + \frac{C_2}{n_{12}^2})}, \tag{4.80}$$

$$\omega_{pt2}^2 \approx \frac{1}{(1-k^2)L_2(\frac{C_1C_2}{C_1 + C_2/n_{12}^2})}. \tag{4.81}$$

Equations (4.79) - (4.81) give the approximated expressions for the resonant frequencies of the complex poles and zeros. To make the complex poles and zeros interlace means

$$\omega_{pt1}^2 \le \omega_{zt}^2 \le \omega_{pt2}^2. \tag{4.82}$$

The left side of the inequality is always met; to meet right side of the inequality, there must be

$$\frac{K_1N_1 + K_2N_2}{(1-k)(K_1N_1L_2C_2 + K_2N_2L_1C_1)} \le \frac{1}{(1-k^2)L_2(\frac{C_1C_2}{C_1 + C_2/n_{12}^2})}, \tag{4.83}$$

or the coupling coefficient should meet:

$$k \le \frac{K_1N_1L_2C_2 + K_2N_2L_1C_1}{(K_1N_1 + K_2N_2)L_2(\frac{C_1C_2}{C_1 + C_2/n_{12}^2})} - 1. \tag{4.84}$$

Figure (4.21) shows the right side of Eq. (4.84) as a function of the ratio of the

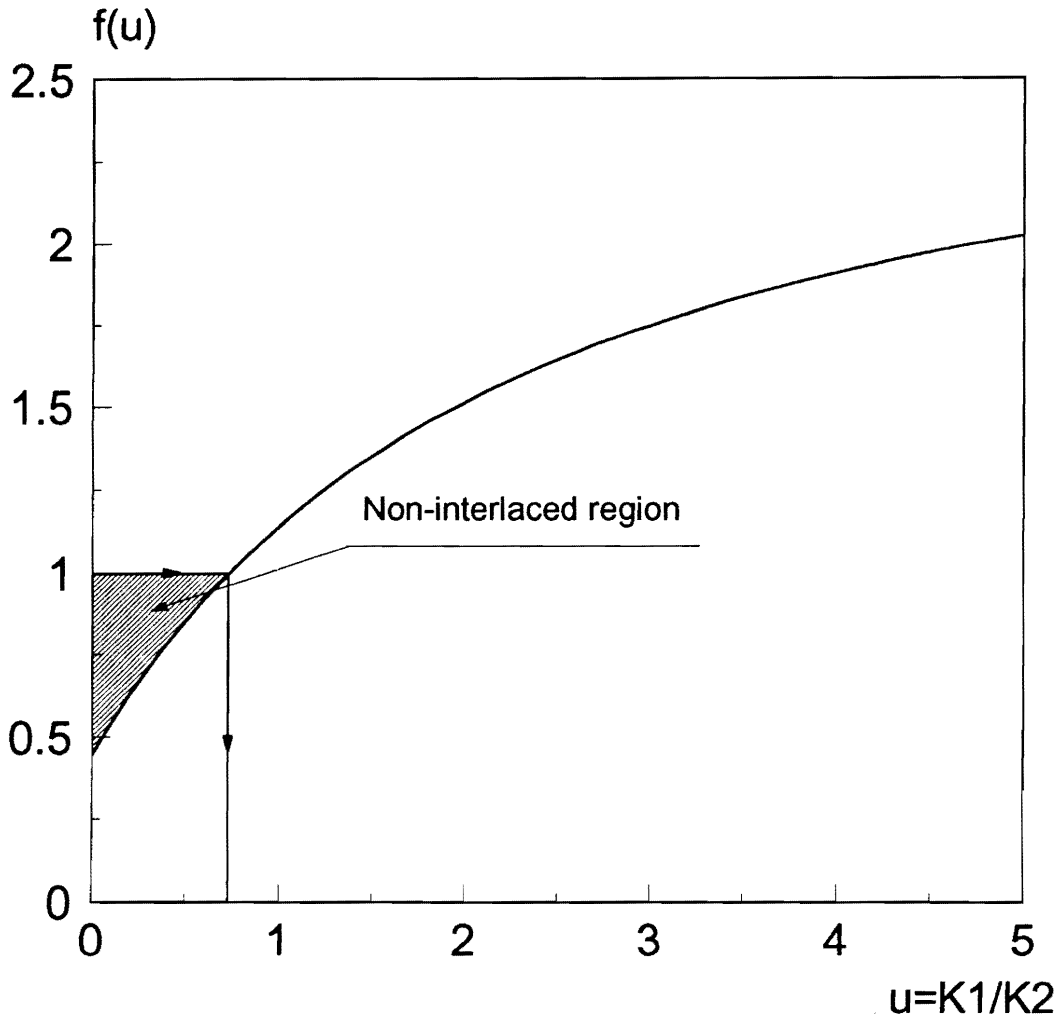


Fig. 4.21. Design criterion for coupling coefficient, k, to ensure a pole-zero interlaced system. *The vertical axis f(u) is actually the right side of Eq. (4.84), which should be greater than the coupling coefficient, k. It is noticed that the coupling coefficient is in the range: 0<k<1. Once f(u)>1, k can take any value and the system still has interlaced poles and zeros.*

weighting factors, $u=K_1/K_2$. it can be seen that a large coupling coefficient tends to yield a noninterlaced pole-zero distribution for the given weighting factors, and the system tends to have less stability margin for the same compensator design, which agrees with the finding reported in [F9]. It is noticed that once the right side of Eq. (4.84) exceeds 1, the coupling coefficient, k, no longer affects relative positions of the poles and zeros since k is physically bounded in the range (0,1). Actually, if the coupling coefficient is chosen outside the shadowed area, the final duty cycle-to-output transfer function will have interlaced complex poles and zeros.

4.6 Design Example

In this section, the design of a dual-output forward converter is illustrated. The design specifications of the converter are:

- input line voltage V_{in}, $120\ V$ - $190\ V$,
- 5 V output: $4.8V \le V_{o1} \le 5.2V$, $2A \le I_{o1} \le 15A$, and
- 12 V output: $11.5V \le V_{o2} \le 12.7V$, $0.5A \le I_{o2} \le 3A$.

The experimental dual-output forward converter operating at 100 kHz was built with its circuit parameters as shown in Table 4.3.

To meet dc regulation specification, the ratio of the weighting factors is chosen as

Table 4.3. List of the Circuit Parameters.

N_1	0.107	N_2	0.25
L_1 (μH)	17.8	R_{L1} (Ω)	0.037
L_2 (μH)	96.6	R_{L2} (Ω)	0.12
C_1 (μF)	50	R_{c1}(Ω)	0.0087
C_2 (μF)	24	R_{c2}(Ω)	0.0087
R_{1min} (Ω)	0.333	R_{2min} (Ω)	4
R_{1max} (Ω)	2.5	R_{2max} (Ω)	24
K_1	0.278	K_2	0.093
k	0.89	n_{12}	0.479

$u=K_1/K_2=3$, which yields $K_1=0.284$, $K_2=0.092$.

The turns ratio of the coupled inductors is equal to the ratio of the output voltages [I16]. The coupling between the output inductors is designed $k=0.89$.

Figure 4.22 shows the duty cycle-to-output transfer functions for the designed converter. The duty cycle-to-output 1 transfer function has interlaced complex poles and zeros, and the duty cycle-to-output 2 transfer function has non-interlaced complex poles and zeros. The duty cycle-to-feedback transfer function, which is the combination of the two, has interlaced complex poles and zeros as shown in Fig. 4.23.

Using Eqs. (4.79) - (4.81) derived in the last section, the values of the resonant frequencies of the poles and zeros are calculated as:

$$s_{zt} \approx 1.775 \times 10^6 \quad rad/s, \quad or \quad f_{zt} \approx 283 \quad kHz, \tag{4.85}$$

$$\omega_{zt} \approx 67430 \quad rad/s, \quad or \quad f_{zt} \approx 10732 \quad Hz, \tag{4.86}$$

$$\omega_{pt1} \approx 19061 \quad rad/s, \quad or \quad f_{pt1} \approx 3034 \quad Hz, \tag{4.87}$$

$$\omega_{pt2} \approx 74077 \quad rad/s, \quad or \quad f_{pt2} \approx 11790 \quad Hz. \tag{4.88}$$

Checking against Fig. 4.23, it can be seen that there is a good agreement among the PSpice simulations, measurements, and approximated expressions Eqs. (4.86) - (4.88).

Since the complex poles and zeros are interlaced, the compensator with an integrator plus two poles and two zeros as given in Eq. 4.71 is employed. The crossover

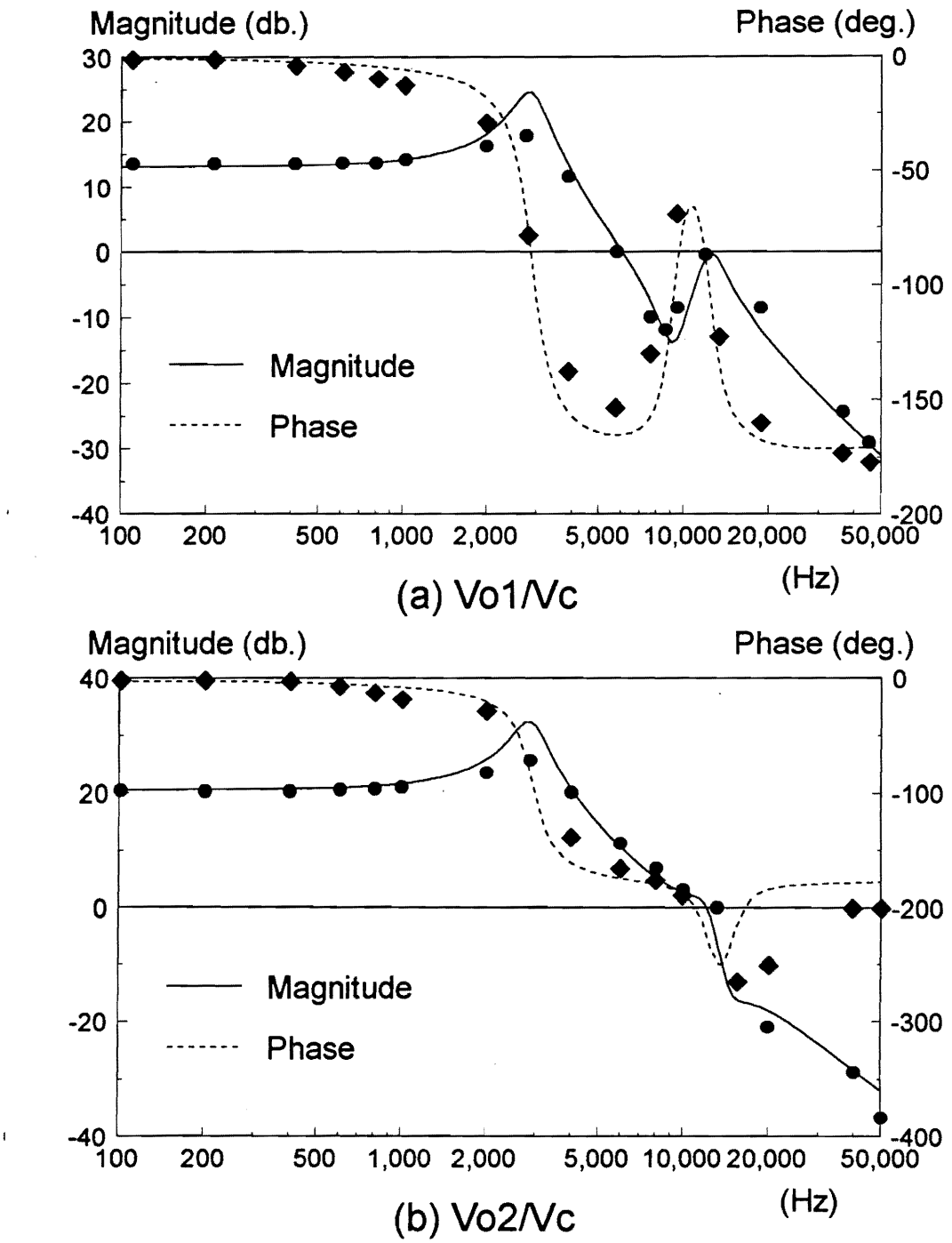


Fig. 4.22. Duty cycle-to-output transfer functions for the design example. *(a) 5-V output. The transfer function has interlaced complex poles and zeros. (b) 12-V output. The transfer function has non-interlaced complex poles and zeros. The dots are the measurement.*

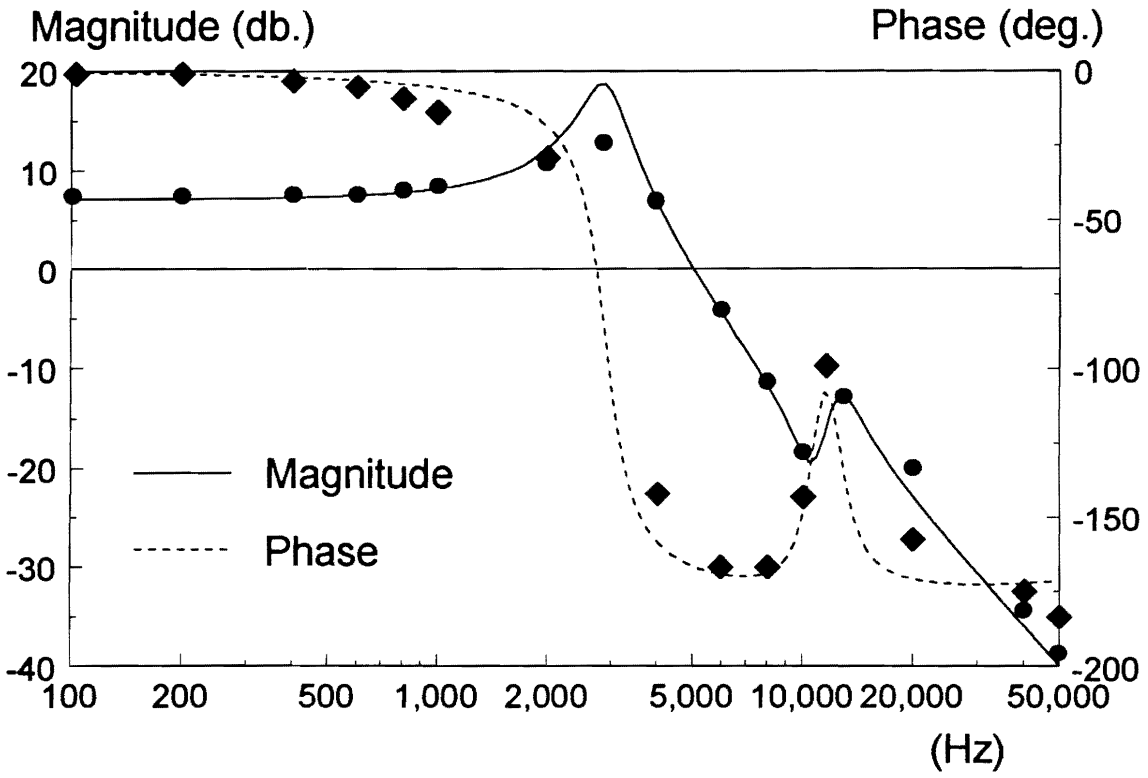


*Fig. 4.23. **Duty cycle-to-feedback transfer function for the design example.** The weighting factors are K1=0.284, K2=0.092. It is noticed that the 12-V duty cycle-to-output transfer function has non-interlaced complex poles and zeros. The combined transfer function has interlaced complex poles and zeros.*

frequency is chosen at 30 kHz. The first pole is placed at half of the switching frequency:

$$s_{pc1} = 314159.3 \quad rad/s, \quad or \quad f_{pc1} = 50 \quad kHz. \tag{4.89}$$

The second pole is placed below the equivalent ESR zero:

$$s_{pc2} = 628318 \quad rad/s, \quad or \quad f_{pc2} = 100 \quad kHz. \tag{4.90}$$

The first zero is placed below the first pair of the complex poles:

$$s_{zc1} = 12566 \quad rad/s, \quad or \quad f_{zc1} = 2000 \quad Hz. \tag{4.91}$$

The second zero is placed right after the second pair of the complex poles:

$$s_{zc2} = 94248 \quad rad/s, \quad or \quad f_{zc1} = 15000 \quad Hz. \tag{4.92}$$

The integrator gain is

$$K_I = 150000. \tag{4.93}$$

Figure 4.24 shows the system loop gain measured at the feedback path after the summing junction point A, as shown in Fig. 4.8. The system has a phase margin of 32°. The calculations agree well with the measurements up to half of the switching frequency.

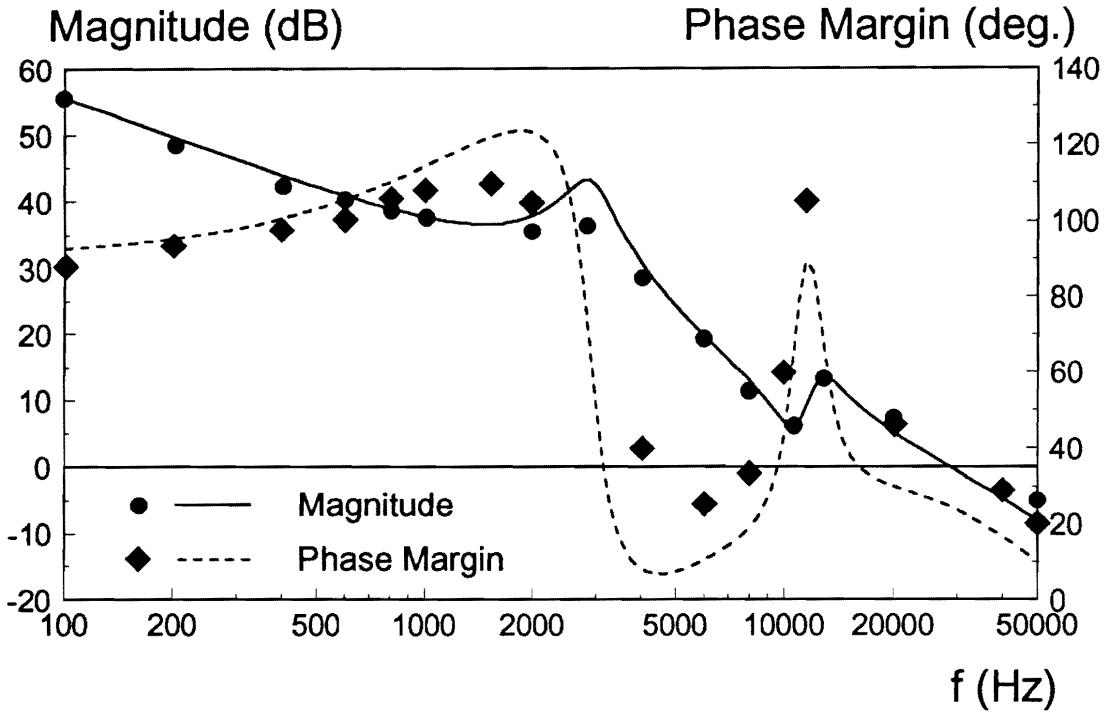


*Fig. 4.24. **Loop gain of the dual-output forward converter with WVC.** The operation condition is high line. As the line voltage decreases, the gain will be lower. If the loop gain is not high enough, the magnitude may intersect 0 dB line more than once due to the complex zeros in the duty cycle-to-feedback transfer function, especially during start-up. Therefore, it is necessary to check the stability margin at the lowest line voltage for which the feedback controller starts to regulate the output voltages.*

4.7 Summary

A small-signal model for a multiple-output forward converter with weighted voltage control and coupled inductors is derived. The converter duty cycle-to-feedback transfer function is of the $2n^{th}$ order. For different values of the weighting factors and the coupling coefficient of the output filter inductors, the system small-signal behaviors can vary drastically. The relative positions of the complex poles and zeros of the duty cycle-to-feedback transfer function are of particular interest for the compensator design. The distribution of the complex poles and zeros can exhibit different patterns, interlaced or non-interlaced complex poles and zeros, depending on the system parameters. The coupling coefficient affects the positions of both complex poles and zeros, whereas the weighting factors affect only the positions of the complex zeros. The system with interlaced poles and zeros is capable of achieving high loop gain and tends to yield better dynamic performances. The analytical model indicates that by adjusting the values of the weighting factors and the coupling coefficient of the output inductors according to Eq. (4.84), the interlaced pole-zero pattern can be obtained.

For a system with interlaced complex poles and zeros, a design employing the compensator with 2 zeros and 3 poles can be used to yield satisfactory performances and stability margin. For a system with non-interlaced complex poles and zeros, an integrator with a relatively low gain has to be used to provide a loop crossover prior to the first double pole, in order to provide adequate stability margin. Since the crossover of the loop

gain is significantly reduced, and consequently inferior dynamic performances occur, compared with the design for the pole-zero interlaced case, this situation should be avoided. Equation (4.84) provides the criterion for a pole-zero interlaced system.

The dynamic performances for a multiple-output converter are characterized by the audio susceptibilities and output impedances just like its single-output counterpart. The unique quantities for the multiple-output converter are the output transimpedances which describe the output voltage variation caused by the other load current. The analytical expressions for the open- and closed-loop audio susceptibilities, the output impedances, and the output transimpedances contain the compensator transfer function, $A_c(s)$, in both numerators and denominators, which could mislead one to conclude that the high loop gain does not improve dynamic performances. Actually, the high loop gain does improve the closed-loop performances, just like the single-output converter. The mechanism of decreasing the audio susceptibilities, output impedances, and output transimpedances, however, is different. Unlike the single-output converter, in which the high loop gain knocks down the audio and the output impedance directly, the decreasing of the audios and output impedances is achieved by cancellation of two numerator terms through which the disturbances are injected into the system. Since the numerators of the audio susceptibilities and the output impedances are the differences between the two terms, it is possible to null the audio susceptibilities and output impedances at a specific frequency.

5. Modeling and Analysis of Current-Mode Control for Multiple-Output Converters

5.1 Introduction

On many occasions, current-mode control is used in conjunction with weighted voltage control and coupled inductors in a MOC. In spite of wide application of current-mode control in MOCs, the small-signal characteristics of current-mode control for the MOCs are not well understood. The published work on current-mode control for MOCs is limited to dc regulation analysis [G11]. There is no small-signal model available for analysis and design when current-mode control is applied. Therefore, some important issues, such as how the system behaves once current-mode control is applied and if the nice features of current-mode control for single-output converters are still preserved, remain without an answer. The purpose of this chapter is to perform a small-signal analysis and provide design insight for the application of current-mode control to MOCs.

First, a small-signal model for MOCs with current-mode control is established. The model includes the effects of weighted control and coupled inductors, which distinguish MOCs from their single-output counterparts. The model is able to predict some unique characteristics of current-mode control, such as subharmonic oscillation and removal of power stage pole to high frequency. Based on the model, the effects of weighting factors and coupling coefficients are investigated. The derived small-signal model is experimentally verified and the design considerations are discussed.

5.2 Small-Signal Model for Current-Mode Control

Figure 5.1 shows a multiple-output forward converter with current-mode control. According to its function, the circuit can be decomposed into three parts: (1) the power stage, which is the same as the voltage-mode control; (2) the current-mode control stage, which includes the information of the sensed currents, the feedforward and feedback gains; and (3) the compensator stage, which is required for both voltage- and current-mode control but is different for voltage- and current-mode control. This section is focused on part (2) - derivation of the current-mode control. The small-signal characteristics and design issues are discussed in next two sections.

To provide design insight, the analysis is performed for a dual-output forward

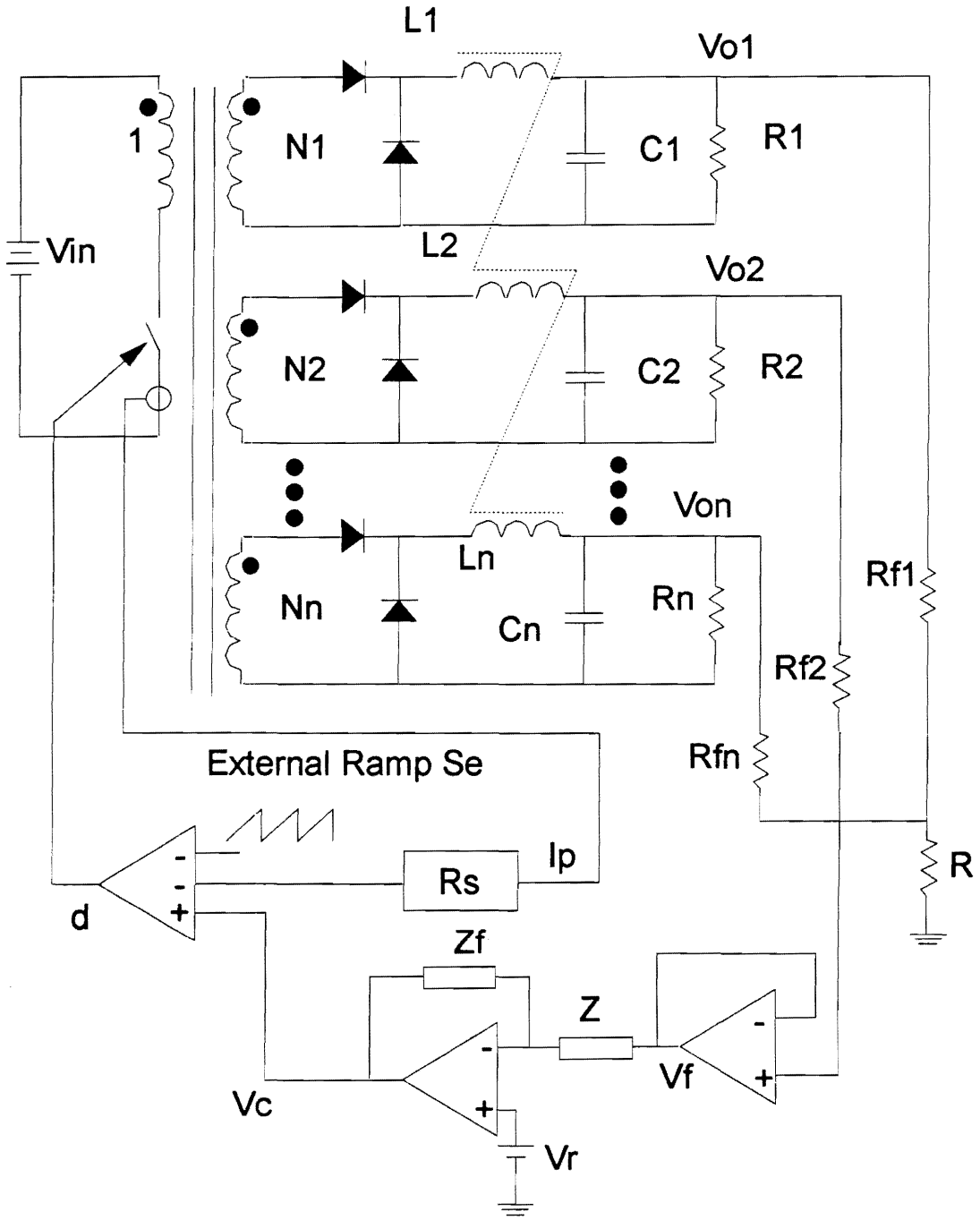


Fig. 5.1. A multiple-output forward converter with current-mode control. Usually, the primary current, which contains the information of all the load currents, is sensed to implement the current mode control.

converter. The basic concept can be easily extended to other topologies with an arbitrary number of outputs.

5.2.1 Modulation and Sampling Gains

The power stage small-signal model is the same for both voltage- and current-mode control. The power stage small-signal model is obtained by using PWM switch modeling techniques, as was done in Chapter 4, which can be directly used for the converter with current-mode control. The circuit model is provided in Fig. 4.2, and small-signal block diagram is shown in Fig. 4.8.

The duty cycle, d, for control of the converter is typically generated with a control voltage and a reference ramp clocked at the desired switching frequency. For single output converter, the current waveform, in conjunction with an external ramp, provides the ramp of the modulator. The modulator gain of the circuit, F_m, is [G2]

$$F_m = \frac{1}{(S_n + S_e)T_s}, \tag{5.1}$$

where T_s is the switching period, S_n is the on-time slope of the current-sense waveform, and S_e is the external ramp which provides design flexibility and stabilizes the current feedback loop [G1-G5]. For a MOC, since the feedback signal is derived from the primary side, it contains the information about both inductor currents. The on- and off-

time slopes of the primary current can be derived from the generic current-mode cell for MOC, as shown in Fig. 5.2 [G7]. For a multiple-output forward converter, the on-time slope, S_{np}, and off-time slope, S_{fp}, of the sensed current are

$$S_{np} = R_s(N_1 S_{n1} + N_2 S_{n2}), \tag{5.2}$$

or

$$S_{np} = R_s \frac{(N_1 L_2 - N_2 M)V_{on1} + (N_2 L_1 - N_1 M)V_{on2}}{L_1 L_2 - M^2}, \tag{5.3}$$

and

$$S_{fp} = R_s(N_1 S_{f1} + N_2 S_{f2}), \tag{5.4}$$

or

$$S_{fp} = R_s \frac{(N_1 L_2 - N_2 M)V_{off1} + (N_2 L_1 - N_1 M)V_{off2}}{L_1 L_2 - M^2}, \tag{5.5}$$

where V_{oni} and V_{offi} are the on- and off-time voltages across the output filter inductors, S_{ni} and S_{fi} are the on- and off-time slopes of the currents through the output filter inductors, and L_1 and L_2, respectively, and are given by:

$$S_{ni} = \frac{(N_i L_j - N_j M)V_{oni}}{L_1 L_2 - M^2}, \qquad i, j = 1, 2, \quad i \neq j, \tag{5.6}$$

and

$$S_{fi} = \frac{(N_i L_j - N_j M)V_{offi}}{L_1 L_2 - M^2}, \qquad i, j = 1, 2, \quad i \neq j. \tag{5.7}$$

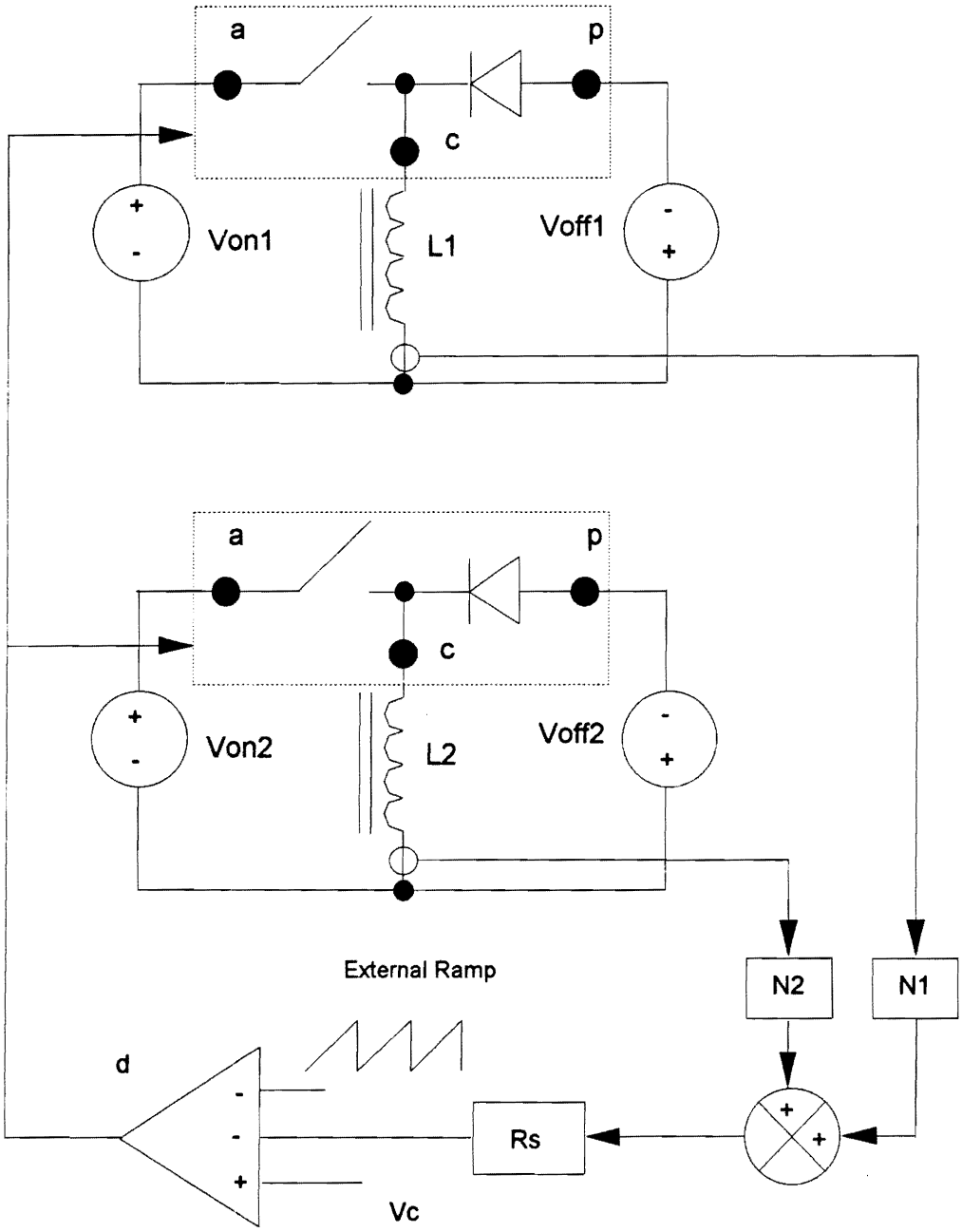


Fig. 5.2. Generic current-mode cell for MOC. *Since the generic current-mode cell is invariant for different topologies, it can also be used for other converters with current-mode control. Notice that the inductors are coupled on the same core.*

Equations (5.3) and (5.5) include the effects of the coupled inductors which are unique to MOCs. Substituting Eq. (5.3) into Eq. (5.1) gives the expression of the modulator gain.

Since current-mode control exhibits characteristics which can only be explained with discrete model [G2], the constant frequency current-mode control converter can be considered a sample-and-hold system with the sampling instant occurring at the intersection of the current signal and the reference voltage. The transfer function of the sampling-and-hold can be approximated by a 2nd-order system [G7]:

$$H_e(s) \approx 1 + \frac{s}{\omega_n Q_z} + \frac{s^2}{\omega_n^2} \tag{5.8}$$

where: $Q_z = -\frac{2}{\pi}$ and $\omega_n = \frac{\pi}{T_s}$.

5.2.2 Feedback and Feedforward Gains

The average inductor currents of the circuit are related to the instantaneous current through the current slopes which are affected by input and output voltages. The feedforward gains from the input voltage and the feedback gains from the output voltages are used to model this dependence. Though the feedforward and feedback gains can be derived from Fig. 5.1, their expressions depend on the specific topology. Therefore, they have to be derived for each circuit. The generic current-mode cell for MOCs shown in Fig. 5.2 is invariant for different topologies, since the dependence of the inductor current

is not directly associated with the input and output voltages, but rather with the on- and off-time voltages across the inductor. The on- and off-time voltages across the inductor are merely the linear combinations of the input and output voltages. The derived feedforward and feedback gains in terms of the on- and off-time voltages, therefore, are universal and can be easily converted in terms of the line and output voltages. The small-signal model of the current cell for the MOC is shown in Fig. 5.3.

Referring to the generic current-mode cell in Fig. 5.2, the relations between the duty cycle, d, and the on- and off-time voltages across the inductors can be derived as:

$$d = \frac{v_{off1}}{v_{on1} + v_{off1}} = \frac{v_{off2}}{v_{on2} + v_{off2}}, \tag{5.9}$$

and

$$d' = \frac{v_{on1}}{v_{on1} + v_{off1}} = \frac{v_{on2}}{v_{on2} + v_{off2}}. \tag{5.10}$$

The steady-state waveforms pertinent to the derivation are given in Fig. 5.4. The basic process is to establish the relationship between the inductor currents and the feedforward gains from the steady-state waveforms. Then the same quantities are derived directly from the small-signal circuit. Finally, the feedforward gains can be solved from these equations.

The average value of the sum of inductor currents referred to the primary is

$$R_s \langle i_{tp} \rangle = v_c - dT_s S_e \frac{S_{fp} d' T_s}{2}. \tag{5.11}$$

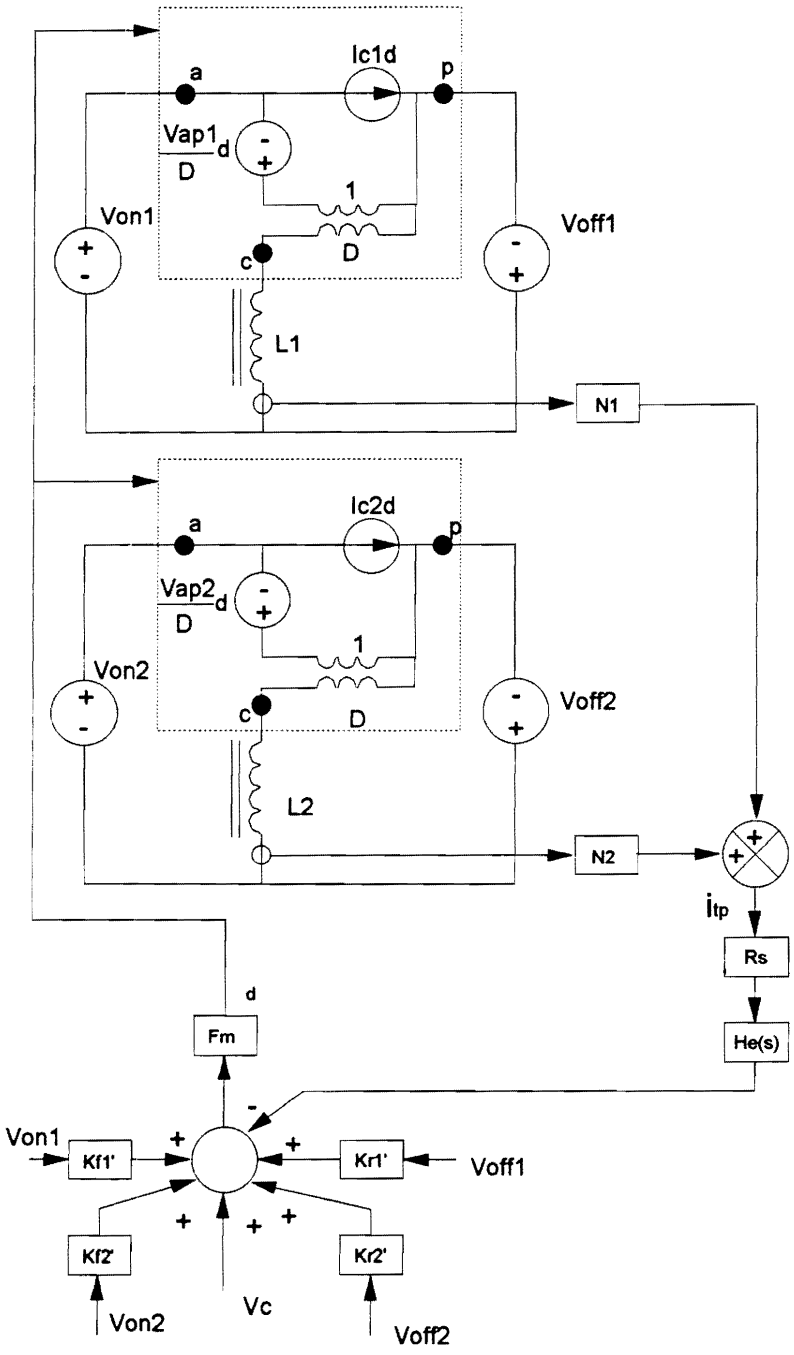


Fig. 5.3. Small-signal model for the generic current cell. *Generally, there are n on-time voltages and n off-time voltages, where n is the number of the outputs. For a forward converter, each on-time voltage is the difference between the secondary voltage and the corresponding output voltage, whereas each off-time voltage is the corresponding output voltage.*

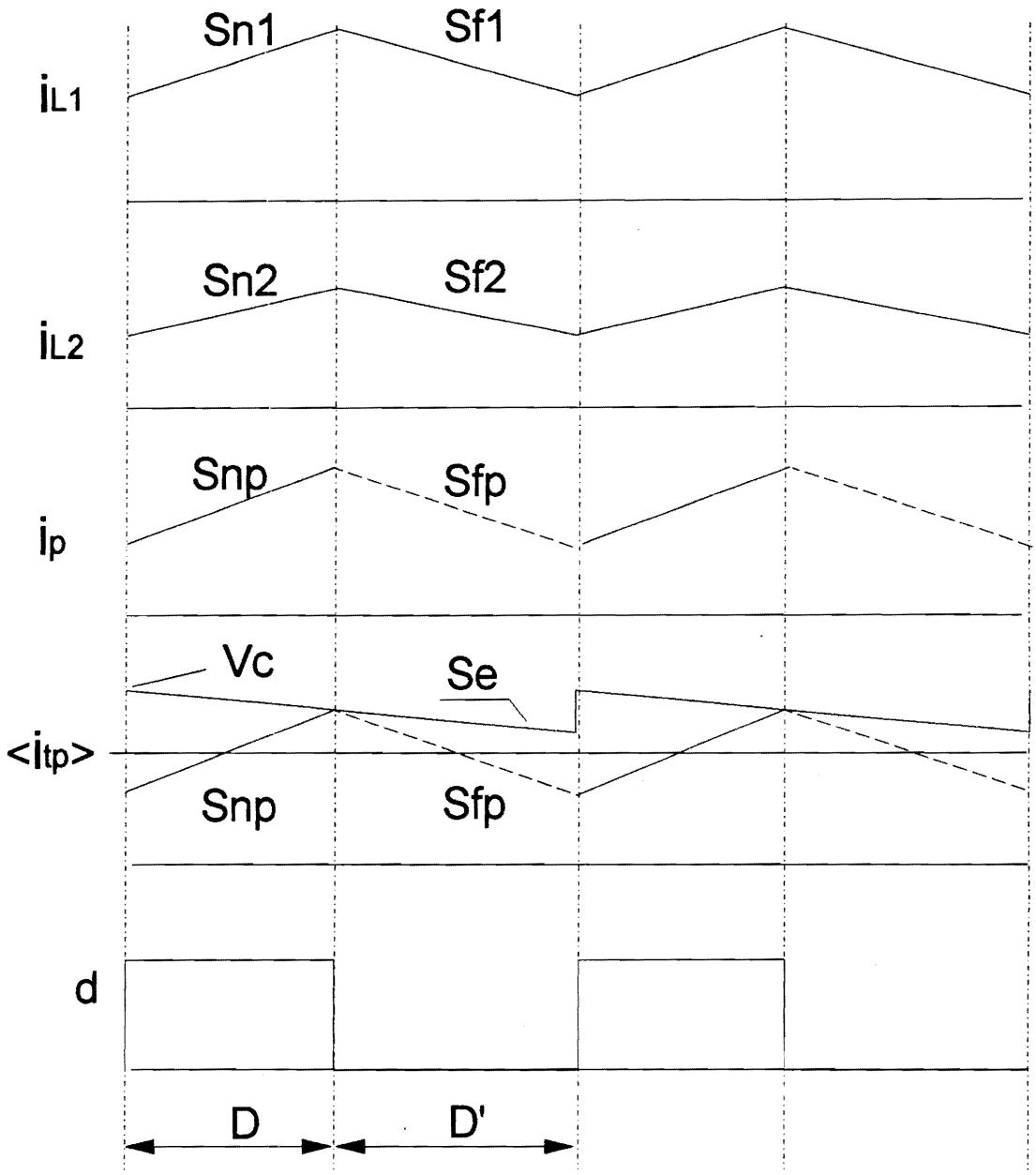


Fig. 5.4. Steady-state waveforms for current-mode control. *The variables are defined as: i_{Li} - inductor current; i_p - primary current; i_{tp} - sum of the inductor currents referred to the primary; S_{ni} (S_{fi}) - on-time (off-time) inductor current slope; S_{np} (S_{fp}) - on-time (off-time) slope of the sum of the inductor currents referred to the primary; S_e - external ramp slope; v_c - control voltage.*

Substitution of Eqs. (5.9) and (5.10) into Eq. (5.11) yields:

$$R_s < i_{tp} >= v_c - \frac{S_e T_s v_{off1}}{v_{on1} + v_{off1}} - \frac{S_{fp} T_s}{2} \frac{v_{on1}}{(v_{on1} + v_{off1})}. \tag{5.12}$$

Perturbing the average current with respect to the on-time voltage v_{on1} gives:

$$\frac{R_s < i_{tp} >}{v_{on1}} = \frac{D T_s S_e}{V_{ap1}} - \frac{D^2 T_s S_{fp}}{2 V_{off1}} \tag{5.13}$$

The same quantity can be obtained from Fig. 5.3 by perturbing v_{on1} and assuming v_{on2}, v_{off1}, and v_{off2} to be zero (Fig. 5.5). It is noticed that the inductors are shorted under dc condition. Then the following two equations are obtained:

$$d = F_m (K'_{f1} v_{on1} - < i_{tp} > R_s), \tag{5.14}$$

$$v_{on1} + \frac{V_{ap1}}{D} d = 0. \tag{5.15}$$

Solving these two equations for the ratio of the sensed current and the on-time voltage v_{on1} yields:

$$\frac{R_s < i_{tp} >}{v_{on1}} = \frac{D}{V_{ap1} F_m} + K'_{f1}, \tag{5.16}$$

Let Eq. (5.13) be equal to Eq. (5.16):

$$\frac{D T_s S_e}{V_{ap1}} - \frac{D^2 T_s S_{fp}}{2 V_{off1}} = \frac{D}{V_{ap1} F_m} + K'_{f1}. \tag{5.17}$$

The feedforward gain K'_{f1} is solved as:

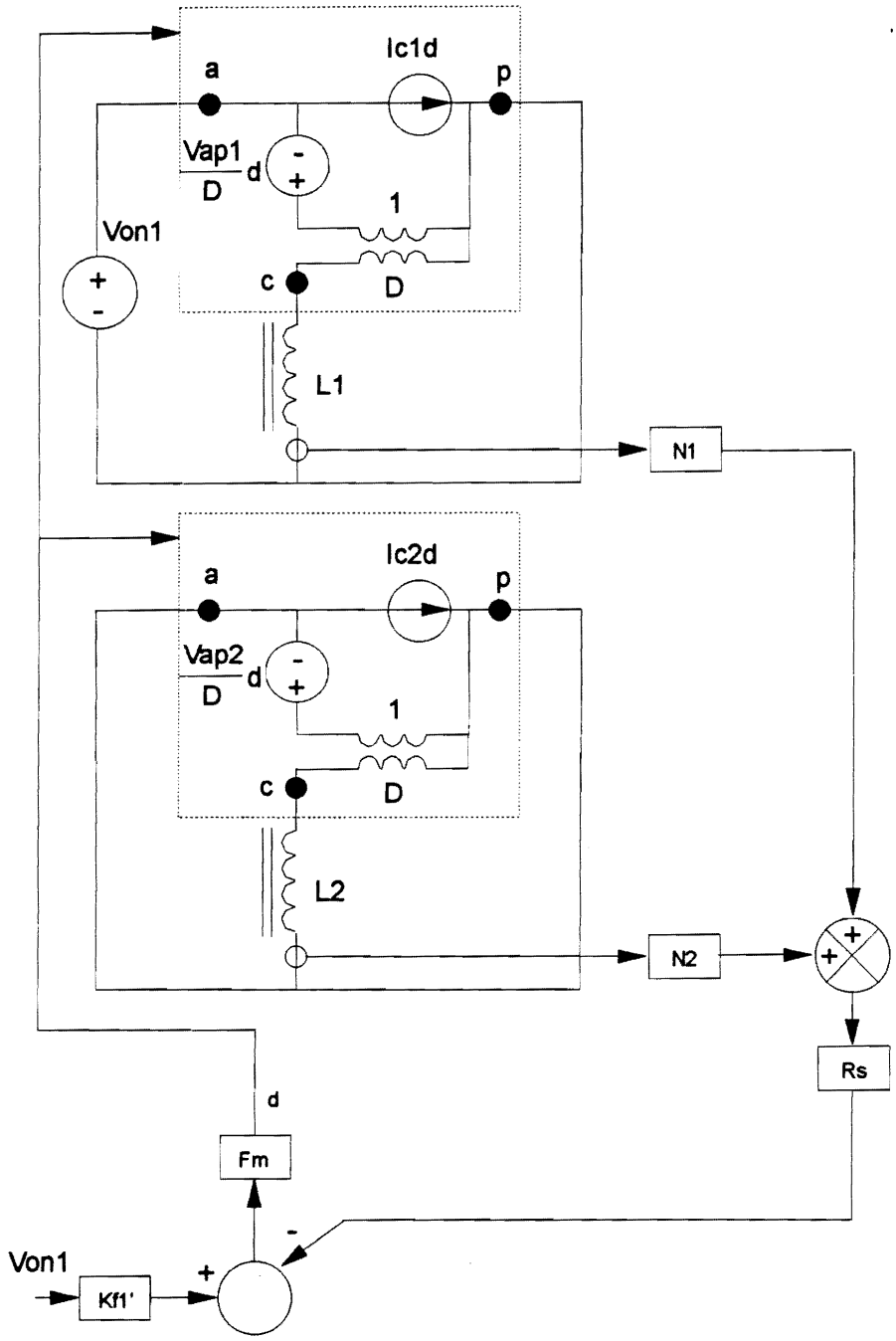


Fig. 5.5. Small-signal model for the generic current cell with fixed v_{on2}, v_{off1}, and v_{off2}. Under dc condition, the sampling-and-hold gain $H_e(s)$ is simply unity.

$$K_{f1}' = -\frac{D^2 T_s}{V_{off1}}\left(S_{np} + \frac{S_{fp}}{2}\right) \tag{5.18}$$

Now the feedback gain from the off-time voltage, v_{off1}, to the control is derived. The average value of the total inductor currents is perturbed again, but this time with respect to the off-time voltage, v_{off1}:

$$\frac{R_s < i_{tp} >}{v_{off1}} = -\frac{D' T_s}{V_{ap1}}\left(S_e + \frac{S_{np}}{2}\right) \tag{5.19}$$

The same quantity can be derived from Fig. 5.3 by perturbing v_{off1} and assuming v_{on1}, v_{on2}, and v_{off2} to be zero as shown in Fig. 5.6. Again, the inductors are shorted under dc condition. Then the following two equations are obtained:

$$d = F_m\left(K_{r1}' v_{off1} - < i_{tp} > R_s\right), \tag{5.20}$$

$$D' v_{off1} = V_{ap1} d. \tag{5.21}$$

Solving these two equations for the ratio of the sensed current and the off-time voltage v_{off1} yields:

$$\frac{R_s < i_{tp} >}{v_{off1}} = K_{r1}' \frac{D'}{V_{ap1} F_m} \tag{5.22}$$

Let Eq. (5.19) be equal to Eq. (5.22):

$$-\frac{D' T_s}{V_{ap1}}\left(S_e + \frac{S_{np}}{2}\right) = K_{r1}' - \frac{D'}{V_{ap1} F_m} \tag{5.23}$$

The feedback gain K_{r1}' is solved as:

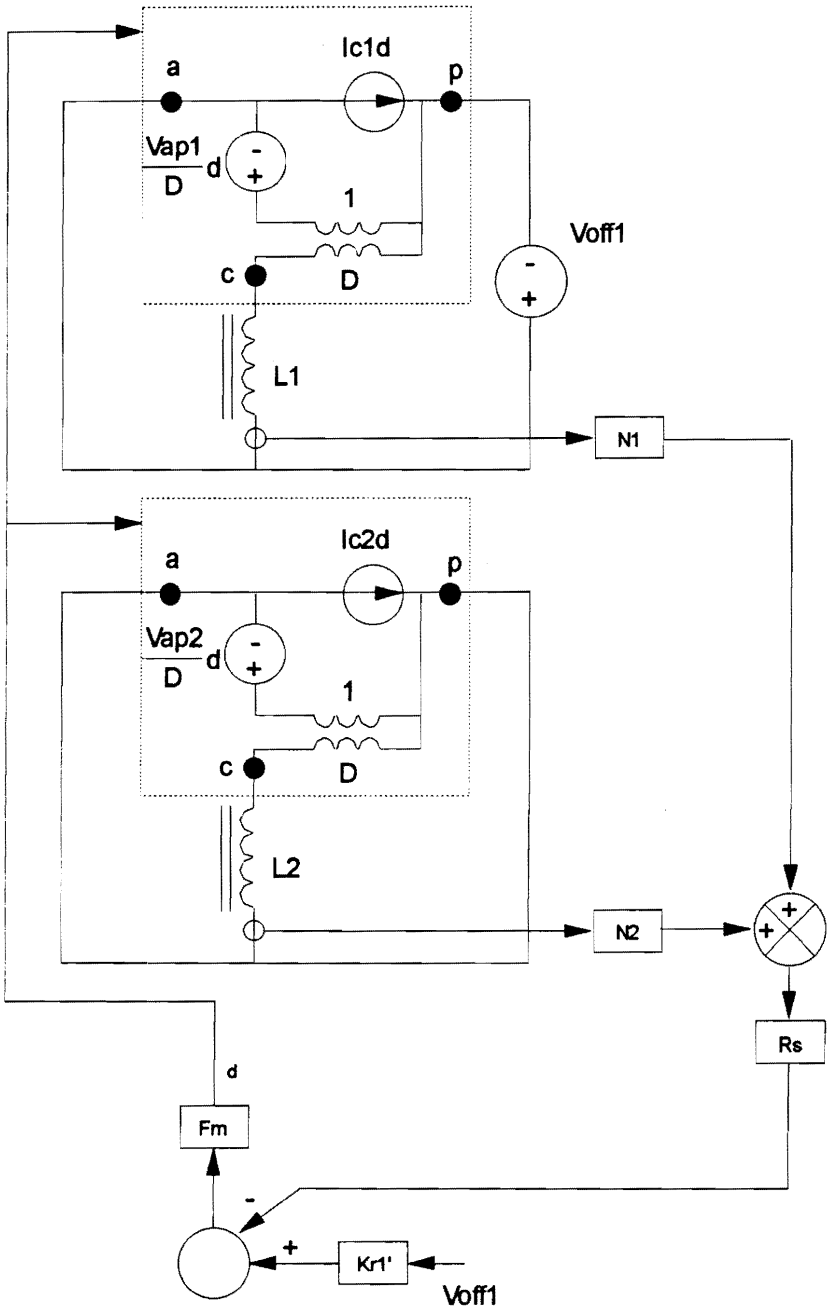


Fig. 5.6. Small-signal model for the generic current cell with fixed v_{on1}, v_{on2}, and v_{off2}. Again, the sampling-and-hold gain $H_e(s)$ is simply unity under dc condition.

$$K_{r1}^{'} = \frac{D^{'2} T_s S_{np}}{2V_{on1}}. \tag{5.24}$$

Similarly, the feedforward and feedback gains $K_{f2}^{'}$ and $K_{r2}^{'}$ are derived as:

$$K_{f2}^{'} = -\frac{D^2 T_s}{V_{off2}}(S_{np} + \frac{S_{fp}}{2}) \tag{5.25}$$

and

$$K_{r2}^{'} = \frac{D^{'2} T_s S_{np}}{2V_{on2}}. \tag{5.26}$$

The above-derived feedforward and feedback gains $K_{fi}^{'}$ and $K_{ri}^{'}$ are universal and not restricted to a specific topology. For a forward converter, the on- and off-time voltages are

$$V_{oni} = V_{in} N_i - V_{Di} - V_{oi}, \qquad i = 1, 2, \tag{5.27}$$

$$V_{offi} = V_{oi} + V_{Di}, \qquad i = 1, 2, \tag{5.28}$$

where V_{Di}'s are the voltage drops caused by the rectifier diodes.

A feedforward path from the input voltage is provided by the feedforward gain $K_{fi}^{'}$ only. The feedback from the output voltage is provided by both $K_{fi}^{'}$ and $K_{ri}^{'}$. The feedforward and feedback gains for the forward converter are therefore calculated as:

$$K_{fi} = K_{fi}^{'}, \qquad i = 1, 2, \tag{5.29}$$

and the feedback gains are

$$K_{ri} = K_{ri}^{'} - K_{fi}^{'}, \qquad i = 1, 2. \tag{5.30}$$

or

$$K_{ri} = \frac{DT_s}{2V_{offi}}[(1+D)S_{np} + DS_{fp}], \qquad i = 1, 2. \tag{5.31}$$

Since the inputs for two power channels are derived from the same input voltage, it is more meaningful to express the feedforward gain directly from the input voltage to the duty cycle:

$$K_f = \frac{d}{v_g} = N_1 K_{f1}^{'} + N_2 K_{f2}^{'}, \tag{5.32}$$

or

$$K_f = -D^2 T_s (S_{np} + \frac{S_{fp}}{2})(\frac{N_1}{V_{off1}} + \frac{N_2}{V_{off2}}). \tag{5.33}$$

The derivation of feedforward and feedback gains K_f, K_{r1}, and K_{r2} completes the small-signal model for the MOC with current-mode control, as shown in Fig. 5.7.

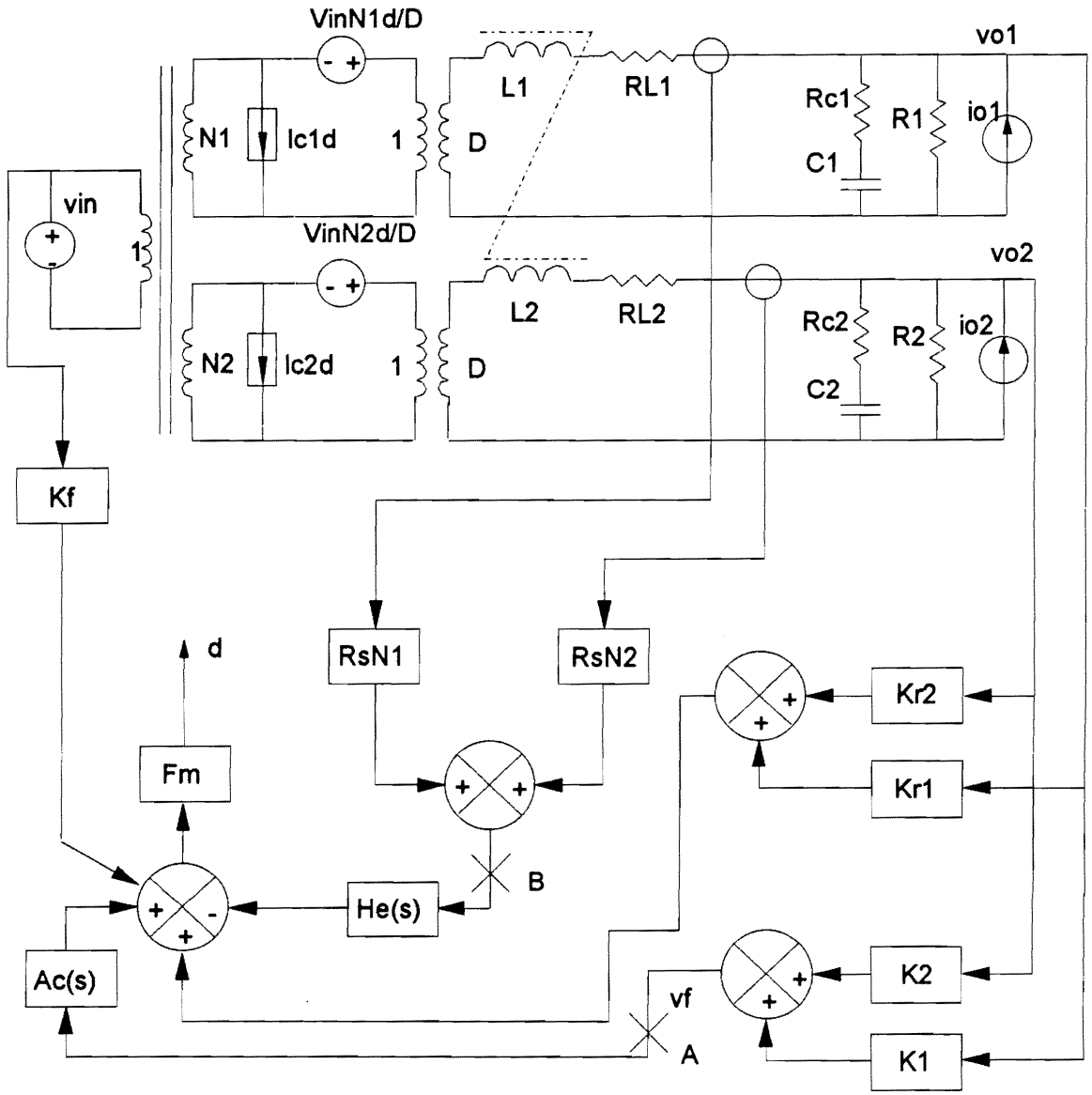


*Fig. 5.7. **Complete small-signal model for the MOC with current-mode control.** The feedforward gain represents the effect of the perturbation of the line voltage on the duty cycle. The feedback gains represent the effect of the perturbation of the output voltages on the duty cycle.*

5.3 Small-Signal Characteristics

The small-signal characteristics of the MOC with current-mode control can be investigated by using the model derived above. The small-signal model shown in Fig. 5.7 was coded into a PSpice program, which was used to generate all of the transfer functions discussed in the following part of the chapter.

5.3.1 Current Loop Gain

Current loop gain, defined by breaking the current loop at point B in Fig. 5.8 with voltage loop open, provides stability information for current-mode control. It is well known that for a single output converter, when the duty cycle of a converter operating under current-mode control exceeds 50%, the inductor current can oscillate until a limit cycle is reached (the phenomenon also referred to as "subharmonic oscillation"). For a MOC, the subharmonic oscillation can also happen once the duty cycle exceeds 50%. The derived small-signal model can accurately predict this phenomenon. Figure 5.9 shows the current loop gain for the operation with duty cycle, $d=0.50$, without external ramp S_e. The gain of the current loop gain touches *0 dB* at half switching frequency and the corresponding phase is -180°, which means the phase margin is 0°. If the duty cycle is increased further, instability can occur.

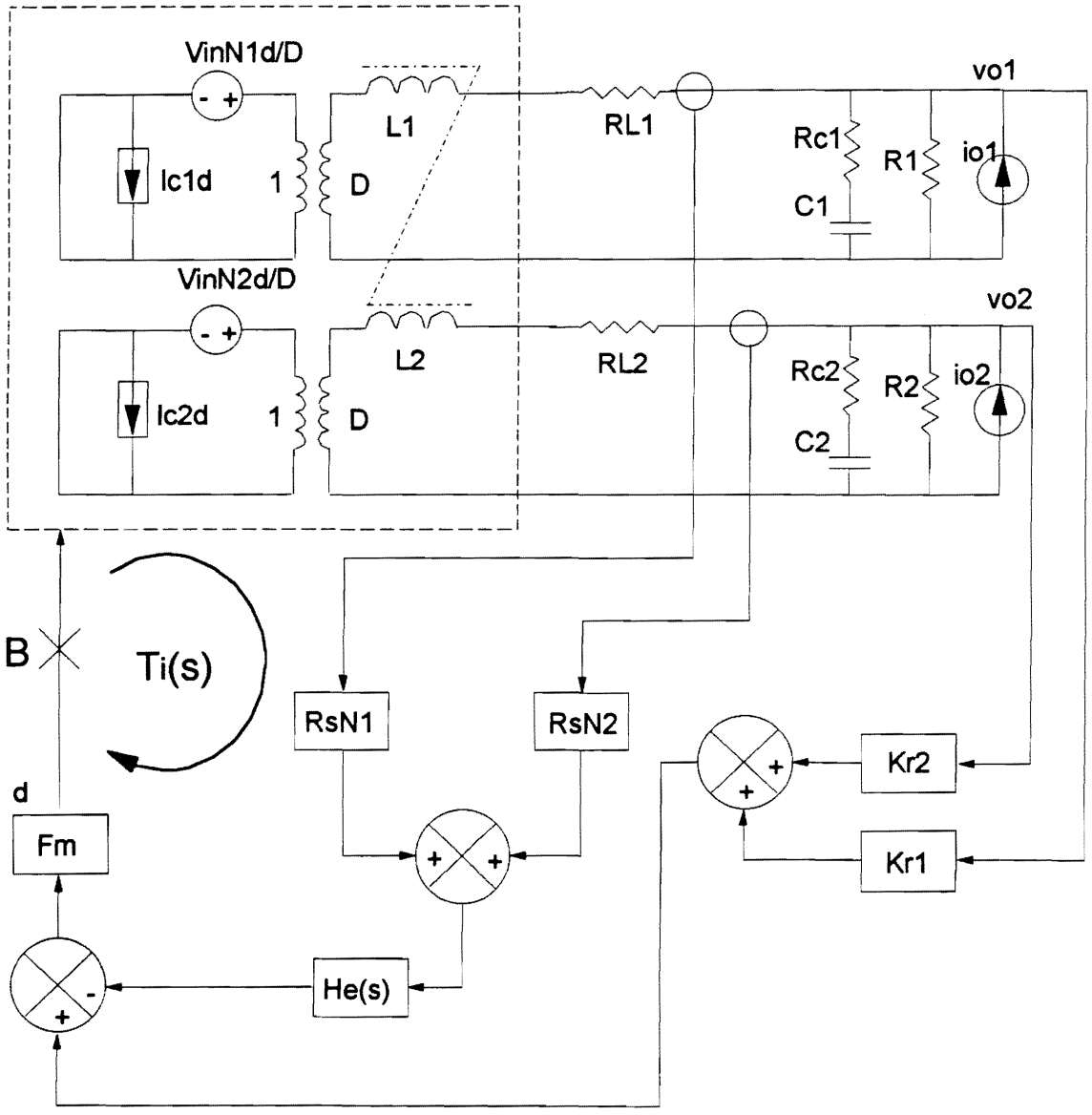


Fig. 5.8. Current-loop gain definition. *The current loop gain is defined by breaking the feedback loop at point B. Since the input voltage is fixed when the current loop gain is calculated, the feedforward gain, K_f, does not show up in the small-signal model.*

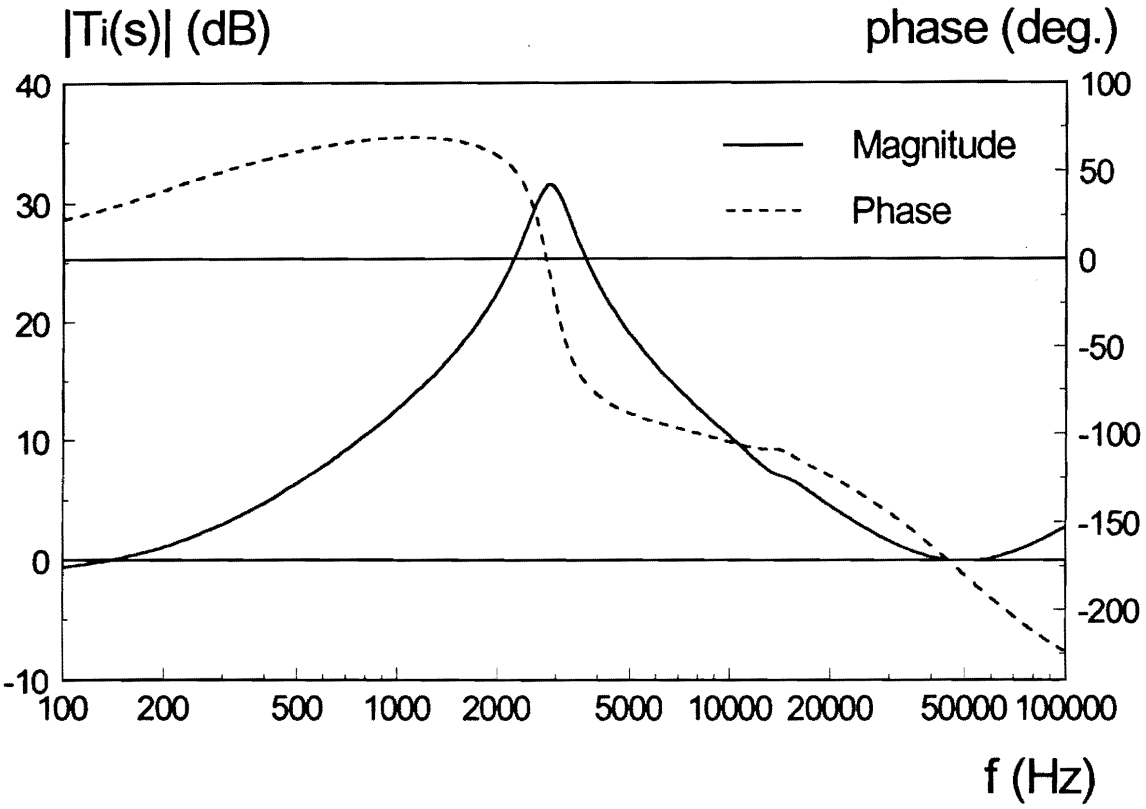


Fig. 5.9. Current-loop gain. *The loop gain clearly shows that when duty cycle is close to 50%, the current loop gain has little phase margin. If duty cycle is increased further, subharmonic oscillation can occur.*

The same conclusion can also be drawn by checking the discrete-time equation of the sensed current, which is given by:

$$i_p(k+1) = -\alpha i_p(k), \tag{5.34}$$

where k is the sampling instant and α is governed by:

$$\alpha = \frac{S_{fp} - S_e}{S_{np} + S_e}. \tag{5.35}$$

If there is no external ramp, then the coefficient α is

$$\alpha = \frac{S_{fp}}{S_{np}} = \frac{(N_1 L_2 - N_2 M)V_{off1} + (N_2 L_1 - N_1 M)V_{off2}}{(N_1 L_2 - N_2 M)V_{on1} + (N_2 L_1 - N_1 M)V_{on2}}. \tag{5.36}$$

Neglecting the parasitics in the circuit, Eq. (5.36) becomes

$$\alpha = \frac{D}{1-D} \tag{5.37}$$

If the duty cycle is larger than 0.5, α is greater than one, which means that any perturbation on the current will result in growing oscillation, and the system becomes unstable. It can be seen from the above analysis that coupling of the output filter inductors does not change the condition under which the subharmonic oscillation occurs.

5.3.2 Duty Cycle-to-Output Transfer Functions

To study the small-signal characteristics of the MOC with current-model control, the converter discussed in Chapter 4 is used here again to generate various transfer functions. The operation conditions are V_{in}=150.2 V, V_{o1}=5.1 V, I_{o1}=2.25 A, V_{o2}=11.68 V, I_{o2}=0.73 A, and D=0.34.

The duty cycle-to-output transfer function for each power channel is defined as the ratio of the corresponding output voltage, v_{oi}, and the control signal, v_c, with current loop closed. Figure 5.10 shows the measurements and calculations of the duty cycle-to-output transfer functions, and they agree well. It can be seen that the nice feature of current-mode control is still preserved for MOCs. By applying current-mode control, the low frequency double pole becomes a single pole, which is the same as in the case of single-output converter with current-mode control, followed by a complex zero-pole pair, which is unique to MOCs. At high frequency, the sampling-and-hold effect can be observed. As in the situation when only voltage-mode control is applied, the relative positions of the poles and zeros (here the low frequency single pole and a pair of complex poles and a pair of complex zeros for current-mode control) are crucial for compensator design considerations. For the duty cycle-to-output 1 transfer function in Fig. 5.10 (a), a pair of complex zeros are interlaced with the low frequency single pole and a pair of complex poles. As for the duty cycle-to-output 2 transfer function in Fig. 5.10 (b), however, a pair of complex poles locate between the low frequency single pole and a pair of complex zeros. As a result, the phase drops drastically (almost to -250°) before being brought up

by the complex zeros. If the single feedback control scheme is used, it is preferable to feedback the output which has interlaced poles and zeros to realize closed-loop control.

Figure 5.11 shows the duty cycle-to-feedback transfer function, based on which the compensator design is performed. The complex zeros, low frequency single pole, and the high frequency complex poles can be either interlaced or noninterlaced depending upon the values of the weighting factors and coupling coefficient. Similarly to the system discussed in Chapter 4, the pole-zero noninterlaced system has a large phase delay at low frequency; thus it is difficult to achieve high gain and wide bandwidth. To ensure good performance of the converter, it is desirable to have the pole-zero interlaced system.

Compared with the duty cycle-to-output and -feedback transfer functions with voltage-mode control only, as shown in Figs. 4.20 and 4.20, it can be seen that current-mode control does remove one of the low frequency complex double poles to high frequency, which results in a single pole at low frequency, but it does not change the relative positions of the poles and zeros. This means that the pole-zero interlacing relation as suggested in Eq. 4.85 can still be used to design a pole-zero interlaced system even when current-mode control is used.

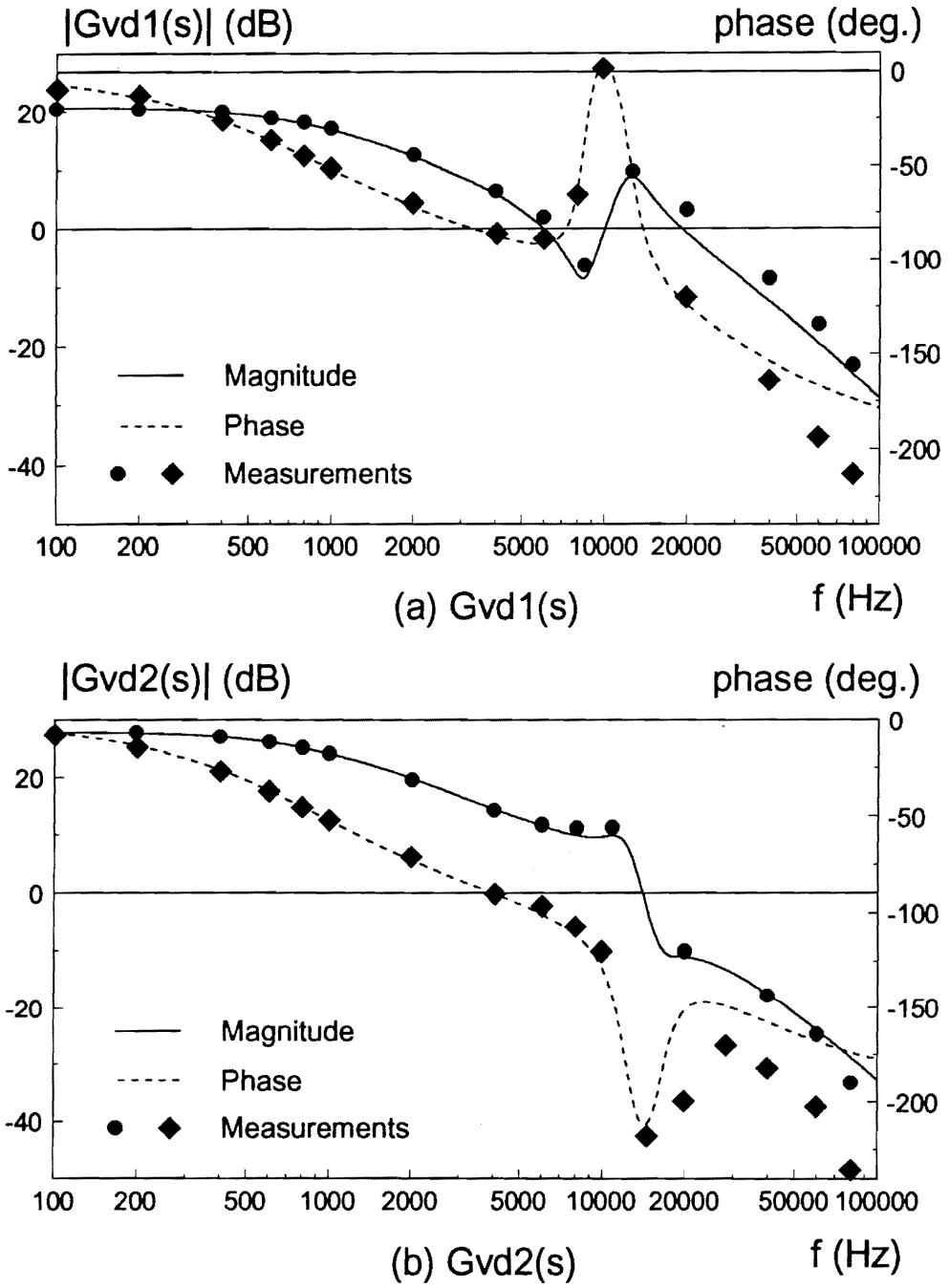


Fig. 5.10. Duty cycle-to-output transfer functions with current-loop closed. *At low frequency, the system has one single pole, one pair of complex poles and one pair of complex zeros. Duty cycle-to-output 1 transfer function shown in (a) has interlaced poles and zeros, while duty cycle-to-output 2 transfer function shown in (b) has non-interlaced poles and zeros.*

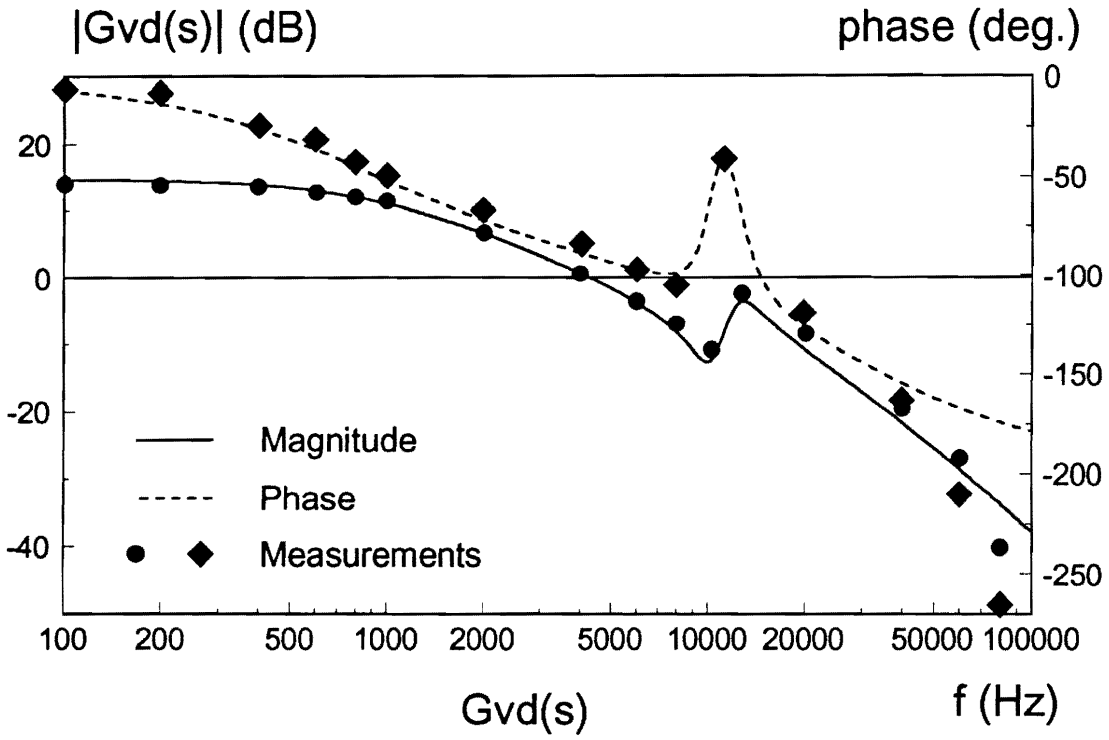


Fig. 5.11. Duty cycle-to-feedback transfer function with current-loop closed. *For MOC with weighted-voltage control, the nice feature of current-mode control is still preserved, i.e., the low frequency behaves like a single pole system. Compared with using voltage-mode control only, the compensator design can be simplified. The predictions and measurements agree very well up to half switching frequency.*

5.3.3 Audio Susceptibilities and Output Impedances

From the derived small-signal model, audio susceptibilities and output impedances (including output transimpedances) can also be calculated.

Figure 5.12 shows the audio susceptibilities with current loop closed. Comparison with the open-loop audio susceptibilities without current-mode control as shown in Fig. 4.11 shows that the audio susceptibilities for both power channels are decreased. From the small-signal model for the MOC with current-mode control in Fig. 5.7, it can be seen that the perturbation from the line voltage affects the power stage transfer functions in two ways. One is through the power stage small-signal model; the other one is through the feedforward gain, K_f, which is negative. The series connection of the controlled sources with the line voltage makes it possible to eliminate the effects of the line perturbation under certain conditions. Although complete null of audio susceptibilities is not practical due to their sensitivity to the current ramp slops [G7,G8], current-mode control can still reduce the effects of the line perturbation on the outputs.

Figure 5.13 shows the output impedances with current loop closed. Compared with the output impedances with voltage-mode control only as shown in Fig. 4.9, it can be seen that the output impedances are severely altered, especially at low frequencies. When using voltage-mode control, the open-loop output impedances are basically the resistances of the output filter inductors at the low frequency. Once current-mode control is applied, the low-frequency impedances are increased drastically, because current-mode control makes

the output filter inductors behave like current sources. If the compensator for the total feedback voltage, which is the weighted sum of the output voltages, is properly designed, the final output impedances can be attenuated to low values. The compensator design will be discussed in the next section.

The output transimpedances are shown in Fig. 5.14. Similarly, the transimpedances are drastically increased at the low frequency compared with their counterparts when only voltage-mode control is used. Both predictions and measurements show that the two output transimpedances are exactly the same, which means that current-mode control does not change the reciprocity of the output transimpedances.

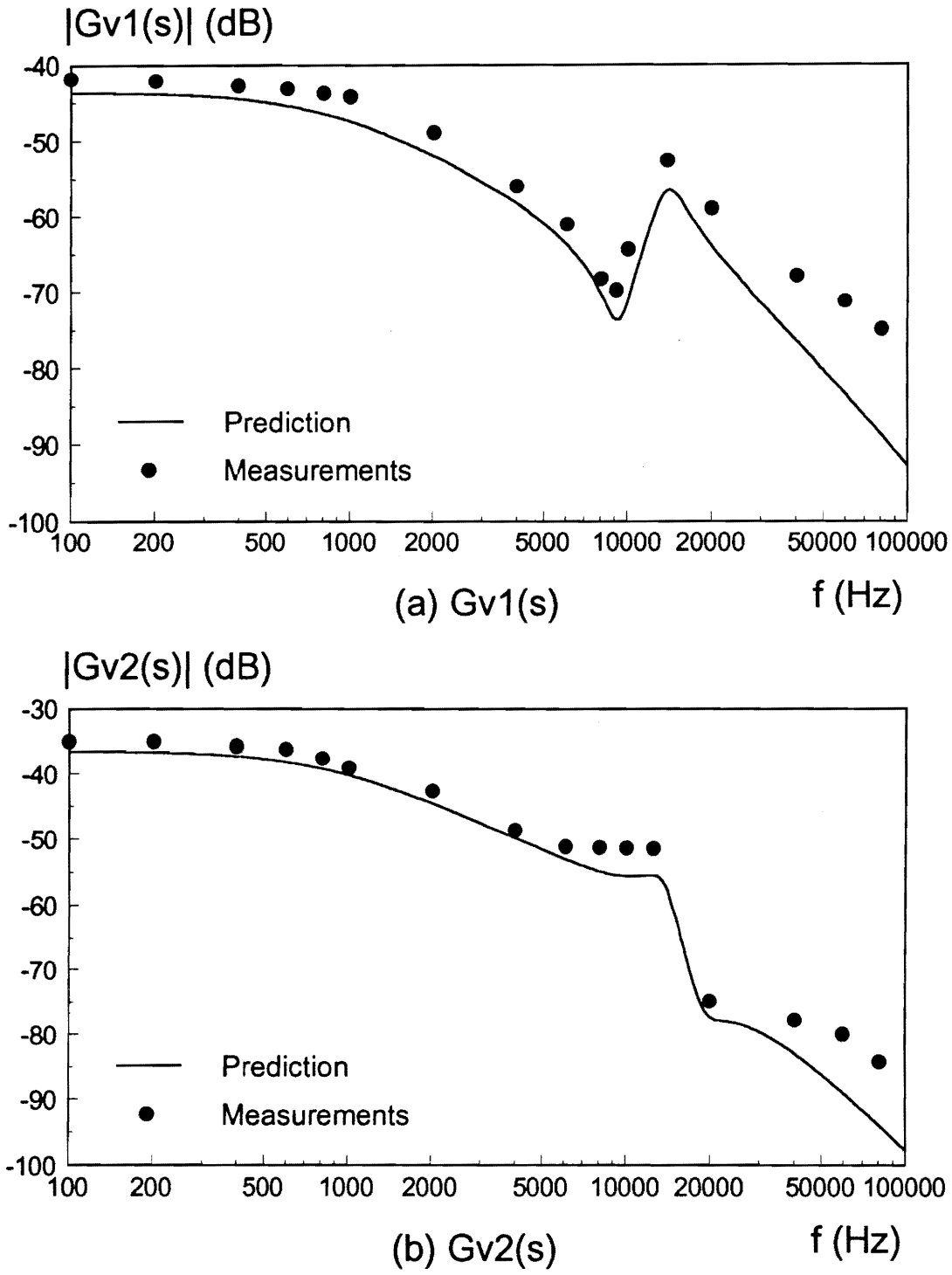


Fig. 5.12. Open-loop audio susceptibilities with current-loop closed. *The audio susceptibilities are reduced compared with the open-loop audio susceptibilities without current-mode control.*

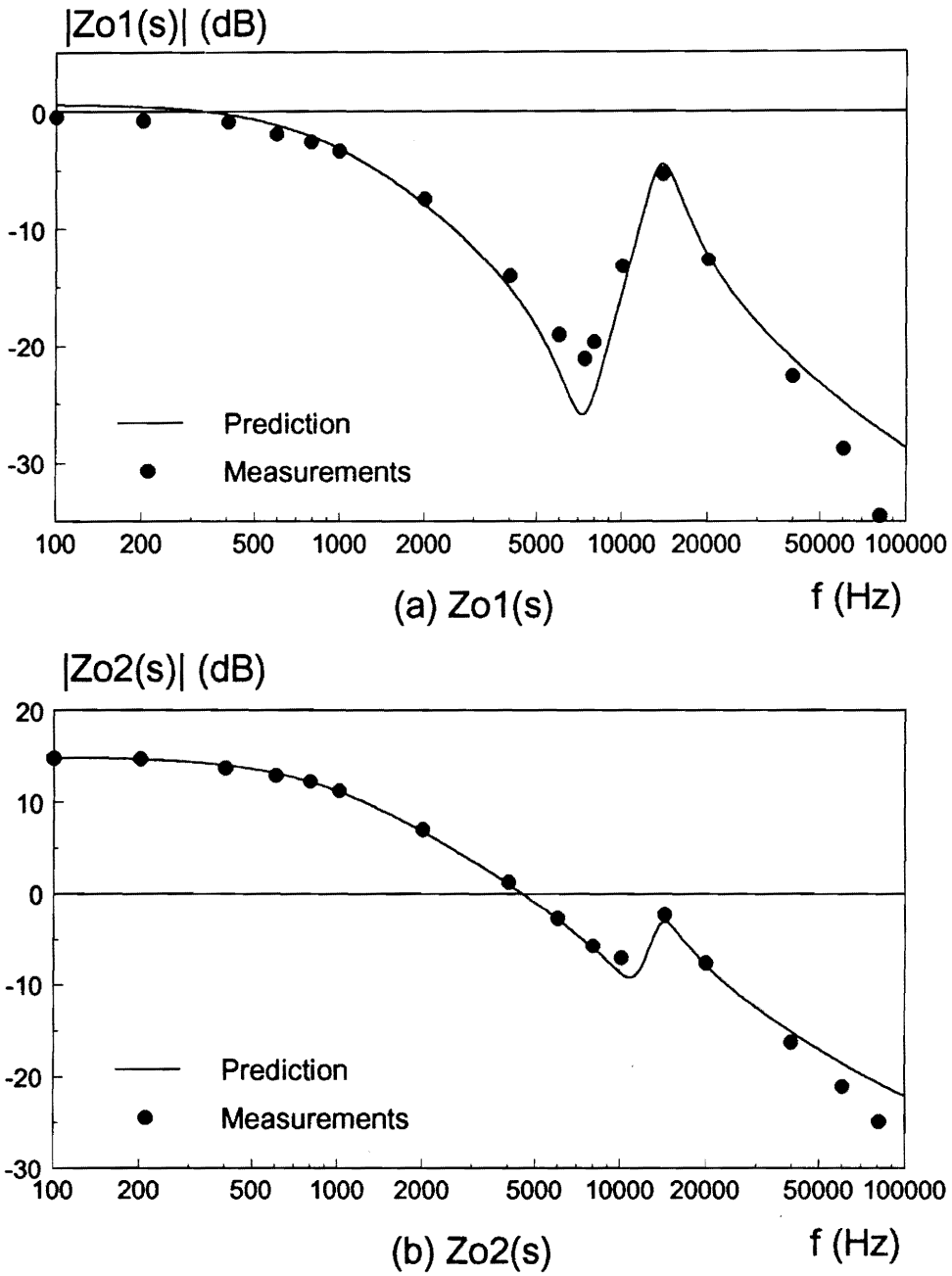


Fig. 5.13. Open-loop output impedances with current loop closed. *The open-loop output impedances are increased, especially at low frequencies compared with those whithout current-mode control. Current-mode control makes the output filter inductors behave like current sources.*

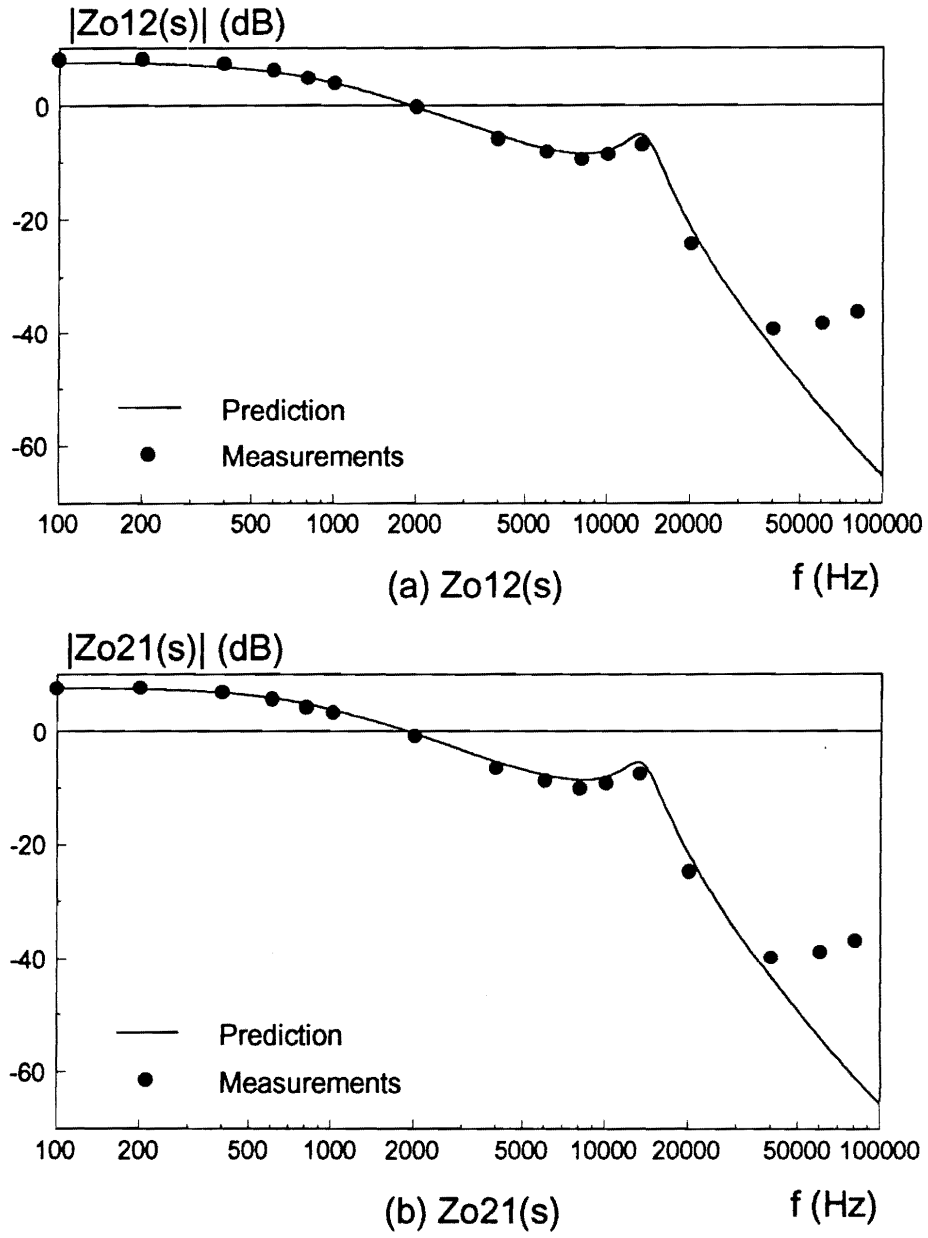


Fig. 5.14. Open-loop output transimpedances with current loop closed. *The two output transimpedances are exactly the same. Current-mode control does not change the reciprocal nature of the output transimpedances.*

5.4 Design Considerations

For MOCs with current-mode control, the duty cycle-to-output (or feedback) transfer functions at low frequencies are of 3rd order, one single pole plus a pair of complex poles and a pair of complex zeros. The sampling gain is approximated as a second order system with the resonant frequency at half switching frequency. In the compensator design, the distribution of the poles and zeros directly affects the selection of the compensator. For the pole-zero interlaced system, the compensator can assume the form of one integrator plus one pole and one zero. Furthermore, the compensator pole is placed at the ESR zero, and the compensator zero is placed in the vicinity of the first single pole. The resulting system will have a relatively large stability margin and good performance. For pole-zero widely separated and noninterlaced system, the loop must be closed at a relatively low frequency to insure enough stability margin; therefore, an integrator is the candidate for the compensator.

Figure 5.15 shows the prediction and measurement of the loop gain with current-mode control for the same converter as the one used in Chapter 4. Again, the agreement between the two is good. The primary switch current is sensed with a 1:100 current sensing transformer and a 910 Ω resistor. The feedforward gain from the input voltage is K_f=*-0.00341*. The feedback gains from the outputs are K_{r1}=*-0.027* and K_{r2}=*-0.015*. Since the duty cycle-to-feedback transfer function, shown in Fig. 5.11, has interlaced poles and zeros, a compensator with an integrator plus one pole and one zero is employed:

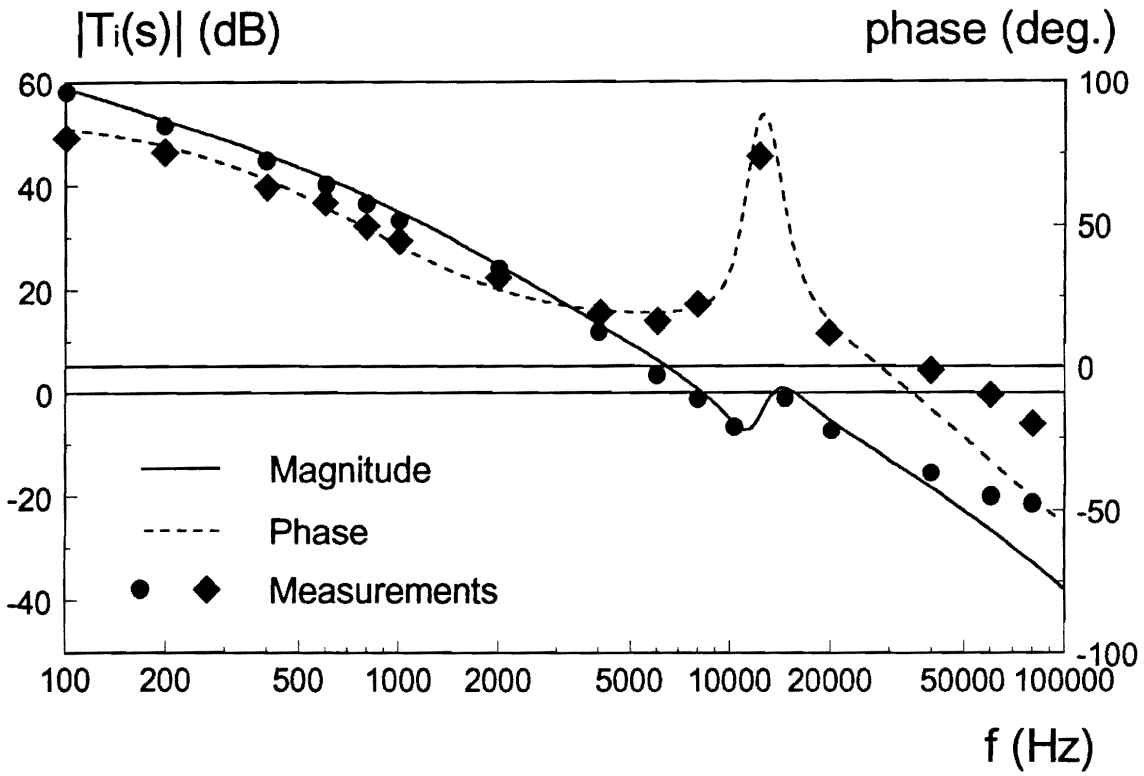


Fig. 5.15. Loop gain with current-loop closed. *For current-mode control, the problem of multiple-crossing of the 0 dB line also exists due to the multiple peaks of the power stage transfer functions. Fortunately, the phase delay in this vicinity is not significant, and therefore it will not cause stability problem.*

$$A_c(s)=\frac{K_I\ (1+s/s_z)}{s\ (1+s/s_p)}, \tag{5.38}$$

where the integrator gain $K_I=99920\ rad/s.$, the compensator zero $s_z=62858\ rad/s.$, and the compensator pole $z_p=502810\ rad/s.$.

It is well known that the current loop may run into subharmonic oscillation if the resonance caused by the sampling-and-hold effect at half switching frequency is not properly damped. Usually, an external ramp is added to the sensed current to provide the necessary damping. For the MOCs, the feedback current is sensed on the primary side, which also includes the magnetizing current, as shown in Fig. 5.16. During one switching cycle, the slope of the magnetizing current is constant with a value of

$$S_{mag}=\frac{V_{in}}{L_m}, \tag{5.39}$$

where V_{in} is the input line voltage, and L_m is the magnetizing inductance.

Although the magnitude of the magnetizing current is usually much smaller than that of the sum of the reflected output filter inductor currents, the slope of the magnetizing current can be comparable to that of the reflected load currents. Under this circumstance, the slope of the magnetizing current behaves like an external ramp which helps damp the oscillation. Therefore, for a forward converter with current-mode control, the slope compensation is inherent. In the example, the slope of the sum of the reflected output filter inductor currents is

$$S_{np}=0.0609\times 10^6\quad A/sec., \tag{5.40}$$

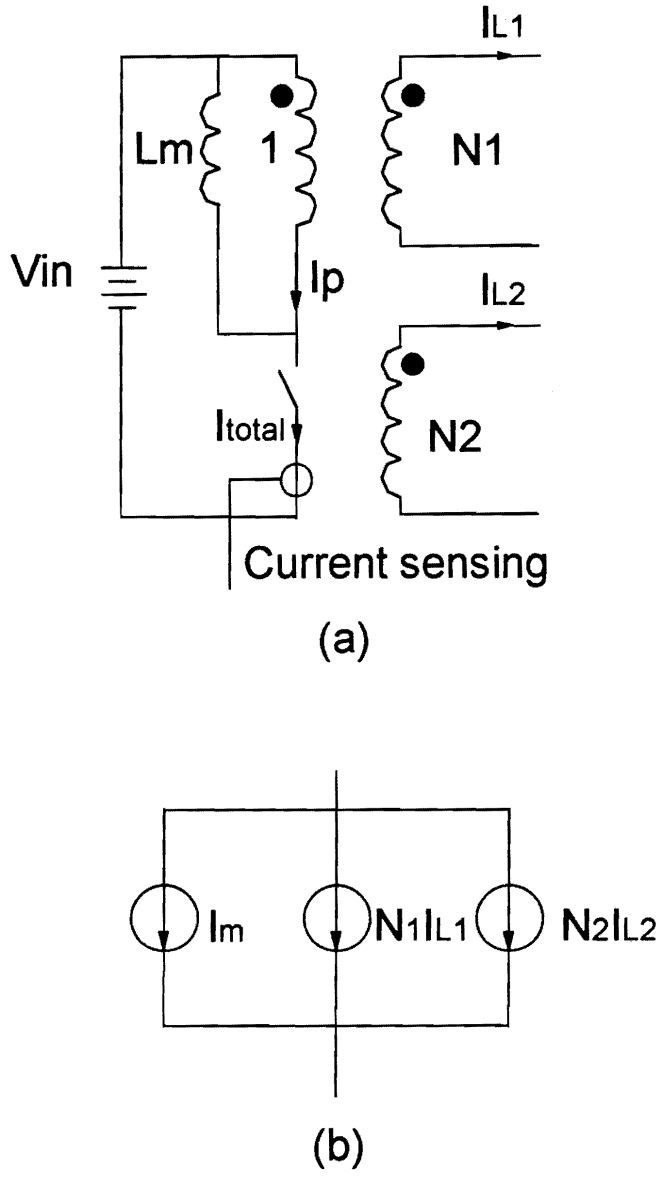


Fig. 5.16. Real sensed current. *For a forward converter, the switch current is usually sensed, which also includes the magnetizing current. During turn-on time, the magnetizing current has a constant slope with the value of the input voltage divided by the magnetizing inductance. The existence of the magnetizing current in the sensed current provides an inherent slope compensation to stabilize the current loop.*

and the slope of the magnetizing current is

$$S_{mag} = 0.075 \times 10^6 \quad A/sec.. \tag{5.41}$$

The prediction and measurement show that the magnetizing current slope here is adequate to damp the half switching frequency resonance, and the system has about 30° phase margin.

If the slope compensation provided by the magnetizing current is not enough, an external ramp, S_e, has to be added. Because of the complexity of the system, it is very difficult to express the Q factor of the resonance at half switching frequency analytically. Therefore, it may take several attempts of trial and error to find the proper external ramp. With the help of simulation program, such as PSpice, the process will not be exhaustive.

5.5 Summary

In this chapter, a small-signal model for current-mode control is derived. The derivation is based on the generic current cell which is universal regardless of the specific topology dealt with. The effects of the perturbations of the input and output voltages on the feedback current are characterized by the feedforward gain, K_f, and feedback gains,

K_{r1} and K_{r2}.

The derived small-signal model can accurately predict some unique characteristics for current mode control such as subharmonic oscillation. Like a single output converter, the low frequency double poles of the power stage transfer function for a MOC with current mode control are split into two single poles, which make the power stage transfer function behave like a single pole system at low frequency. The extra pole-zero pair of the MOC, however, still exhibits multiple peaks. Fortunately, the multiple crossings caused by the multiple peaks on the loop gain will not cause stability problem due to the phase cancellation of the complex poles and zeros.

When designing the compensator for a MOC, the relative positions of the power stage duty cycle-to-feedback transfer function with current loop closed are important in determining the type of the compensator. For a pole-zero interlaced system, an integrator plus one pole and one zero is a good candidate. For pole-zero non-interlaced system, an integrator has to be used to ensure stability of the system, but nonetheless this situation is undesirable. Since the pole-zero interlacing relationship, as given in Chapter 4, is not changed by introducing current-mode control, it can be employed to design a pole-zero interlaced system.

Introducing current-mode control can decrease the audio susceptibilities. As for the output impedances, however, introducing current-mode control causes the output impedances and output transimpedances to increase, since the inductor currents behave like current sources.

For the MOC, once the duty cycle approaches 50%, the current loop exhibits instability just as its single-output counterpart. An external ramp is therefore needed to damp the oscillation occuring at half switching frequency. Since the feedback current is sensed on the primary, which also has the magnetizing current, an external slope compensation is inherent. This will help prevent the system from oscillation.

6. Conclusions

A dc model for the power stage of a multiple-output forward converter is derived, which includes all the major parasitics detrimental to output voltages. The model reveals that the parasitics affect the output voltages differently: the parasitic capacitances of the active switch and the transformer cause a duty cycle extension; the leakage inductances cause a duty cycle loss; and the resistive parasitics cause an internal voltage drop. Since cross-regulation is affected by the internal impedance, which is the sum of the resistances of the rectifier diode, the transformer winding resistance, and the inductor winding resistance, and the product of the switching frequency and the leakage inductance in each power channel, it is important to lower the values of the internal impedances.

In essence, the weighted voltage control redistributes the regulation errors among the sensed outputs by assigning each output a different "weight" in the feedback signal. A nonlinear programming technique-based methodology is developed to choose the feasible weighting factors automatically. The proposed objective function is the weighted sum of squared errors between the nominal and extreme output voltages. The so-defined

objective function can "force" the output voltages to be around their nominal values. The whole design process is coded into a program using Matlab which can be easily used by design engineers.

To improve the cross-regulation of all the outputs, the secondary sides of the power stage can be stacked together. By stacking secondaries, a cross talk is introduced among the outputs, and any load change causes all the outputs to change in the same direction. As a result, the adjustment of the duty cycle will compensate the voltage variation in the same direction. The analysis shows that as the stacking point is moved further away from the transformer, better regulation is obtained, but the power loss increases.

A small-signal model is developed, which includes coupled output filter inductors and weighted voltage control. The small-signal characteristics are found to be very sensitive to the coupling between the output filter inductors, which has been reported before but has never been quantified. The derived small-signal model can accurately predict how a small variation of the coupling coefficient can cause a drastic change of the positions of poles and zeros of the power stage transfer functions. From the standpoint of compensator design, it is desirable to have pole-zero interlaced duty cycle-to-feedback transfer function. The pole-zero interlaced condition is derived as shown in Eq. (4.80), and can be used as a design criterion.

Since the relative positions of the complex poles and zeros in the duty cycle-to-feedback transfer function can exhibit an interlaced or a noninterlaced pattern, the compensator design should also take a different form accordingly. For the pole-zero interlaced system, the compensator can take the configuration of an integrator plus two

poles and two zeros, which can yield a higher loop gain, and consequently a good dynamic response. For the pole-zero noninterlaced and widely-separated system, an integrator has to be used as the compensator. The resulted system will yield lower loop gain and inferior dynamic responses compared with the pole-zero interlaced system, and therefore should be avoided if possible.

A small-signal model for the current-mode control is developed which includes all the effects of the input and output voltage perturbations on the sensed current signal. Some unique features, such as the subharmonic oscillation as the duty cycle approaches 50%, can be predicted by the new model. Once current-mode control is applied, the low frequency complex poles of the power stage duty cycle-to-output (-feedback) transfer functions are split into a low frequency single pole and a high frequency single pole. The complex pole-zero pair at higher frequencies remain unchanged. As in case of the MOC with voltage-mode control only, the relative positions of the poles and zeros are critical for compensator design. The derived model indicates that the application of current-mode control does not change interlacing of poles and zeros. The pole-zero interlaced condition derived for voltage-model control can still be used as the design criterion.

Since the primary switch current is sensed to implement current-mode control, the magnetizing current, which is constant during on time, is also included as part of the sensed current signal. The magnetizing current behaves like an external ramp, and therefore, the current slope compensation is inherent for a MOC.

This dissertation presents a comprehensive study of weighted voltage control for multiple-output forward converters. As for the application of the analysis and design

methodologies provided in the dissertation to other topologies, more work needs to be done. The following topics are of considerable research interest for future work:

- detailed dc analyses of multiple-output flyback and current-fed push-pull (or Weinberg) converters. Flyback converters have the advantages of low part count and low cost, and are very widely used for multiple-output applications. Although some analyses have been done for flyback MOCs [C1, C2, C4, and C11], there is a need to incorporate these results into the design procedure for weighted-voltage control. A current-fed push-pull converter is also very popular, especially for the aerospace applications. Since the filter inductor is located on the primary side, the secondary impedances are smaller than those of a forward converter. It possesses the advantages of both forward and flyback converters from the point of view of cross regulation and voltage conversion. A comparison among these three topologies is needed to find the optimal topology for multiple-output applications.

- small-signal modeling and analyses for flyback and current-fed push-pull converters. Since flyback and current-fed push-pull converters have right half plane zeros, it is usually difficult to achieve high loop gain and wide bandwidth. For multiple outputs, the small-signal behavior will be even more complicated. The small-signal models are to be developed to facilitate compensator design.

- current-mode control for flyback and current-fed push-pull converters with multiple outputs. Small-signal model for current-mode control is necessary to provide design insight when current-mode control is applied.

- incorporation of the new transformer model, as derived in Appendix C, into the design tool. Since the new transformer model takes more complex form, the design equations used in Chapter 2 will also be more complex. Incorporation of this new model into the optimization design tool can yield design which accounts for all the effects of the leakage inductances.

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Appendix A. Programs for Calculation of the Weighting Factors

The programs listed below are used to search for the feasible weighting factors for multiple-output forward converters with weighted voltage control. The programs are written with Matlab, and are executable *.m files. In the programs where marked "###" the user should provide the values for the corresponding parameters.

The design equations are derived in Chapter 2 of this thesis. The flow chart of the program is also given in Chapter 2.

The programs need Matlab basic functions and optimization tool box. They can be run either on a Sun workstation or PC.

A.1 Dual-Output Converters

```
% Dual.m -- Invoking optimization routine to calculate weighting factors K1 and K2.
%          The objective function and constraints are stored in dual_a.m.
%          The dual_b.m is used to plot the output regulation.
%          The dual_c.m is used to plot the 3-D mesh for the objective function.
%          The final results are stored in dual_out.dat.

clear

% Define the global variable
global Fs Ts Dn Vinnom Vinmin Vinmax Vr Vin
global Vo1noms Vo1mins Vo1maxs Vo2noms Vo2mins Vo2maxs
global Io1min Io1max Io2min Io2max DI1 DI2
global Rpdc Rds Co Np Ns1 Ns2
global Vd1 Rd1 Rl1 Rs1dc Ls1 Vd2 Rd2 Rl2 Rs2dc Ls2
global N1 N2 N1auto N2auto
global NON_FEAS f NI W1 W2
global STACK Nss1 Nss2 STACK_OK

% Optimization objective function weighting
% If Vo1 is more important, let W1>W2, e.g., W1=10, W2=1.
% If Vo1 and Vo2 are of the same importance, let W1=W2=1.
W1=###;
W2=###;

% Design specifications

Fs=###;          % Switching frequency
Ts=1/Fs;         % Switching period

% Input voltage range
Vinnom=###;      % Nominal input line voltage
Vinmin=###;      % Minimum input line voltage
Vinmax=###;      % Maximum input line voltage

% The design is performed at the nominal line
Vin=###;

% Reference voltage
Vr=###;
```

```
% Specified output voltage range
Vo1noms=###;
Vo1mins=###;
Vo1maxs=###;
Vo2noms=###;
Vo2mins=###;
Vo2maxs=###;

% Load range
Io1min=###;
Io1max=###;
Io2min=###;
Io2max=###;

% Step size of the load current
NI=10;
DI1=(Io1max-Io1min)/NI;
DI2=(Io2max-Io2min)/NI;

% Primary circuit parameters

Rpdc=###;
Rds=###;
Co=###;

% Transformer turns
Np=###;
Ns1=###;
Ns2=###;

% Transformer turns ratio
N1=Ns1/Np;      % N1-N2 can use measured values.
N2=Ns2/Np;

% If the autotransformers are used on the secondaries, provide values for N1auto and N2auto. Otherwise
set them equal to 1.
N1auto=###;
N2auto=###;

% Real transformer turns ratios are
N1=N1*N1auto;
N2=N2*N2auto;

% Vo1 secondary circuit parameters
Vd1=###;
Rd1=###;
Rl1=###;
Rs1dc=###;
Ls1=###;
```

```
% Lower limit of Vo1 secondary circuit parameters
% If the circuit parameters are not allowed to change, simply set them equal to the original values, e.g.,
Vd1min=Vd1.
Vd1min=###;
Rd1min=###;
Rl1min=###;
Rs1dcmin=###;
Ls1min=###;

% Number of division of the secondary circuit parameters
%  between the given and minimum values, e.g., NP=4.
NP=###;

% Increment of Vo1 secondary circuit parameters
DVd1=(Vd1-Vd1min)/NP;
DRl1=(Rl1-Rl1min)/NP;
DLs1=(Ls1-Ls1min)/NP;
DRd1=(Rd1-Rd1min)/NP;
DRs1dc=(Rs1dc-Rs1dcmin)/NP;
DLs1=(Ls1-Ls1min)/NP;

% Vo2 secondary circuit parameters
Vd2=###;
Rd2=###;
Rl2=###;
Rs2dc=###;
Ls2=###;

% Lower limit of Vo2 secondary circuit parameters
% If the circuit parameters are not allowed to change, simply set them equal to the original values, e.g.,
Vd2min=###;
Vd2min=###;
Rd2min=###;
Rl2min=###;
Rs2dcmin=###;
Ls2min=###;

% Increment of Vo2 secondary circuit parameters
DVd2=(Vd2-Vd2min)/NP;
DRl2=(Rl2-Rl2min)/NP;
DLs2=(Ls2-Ls2min)/NP;
DRd2=(Rd2-Rd2min)/NP;
DRs2dc=(Rs2dc-Rs2dcmin)/NP;
DLs2=(Ls2-Ls2min)/NP;

% Making a starting guess at the solution
x= [###, ###];

% Open the output file
fid =fopen('dual_out.dat', 'w');
```

```
fprintf(fid, 'The initial circuit parameters are \n')
fprintf(fid,'\n');

% The initial Vo1 secondary power stage
fprintf(fid, 'Vd1= %g \n', Vd1);
fprintf(fid, 'Rd1= %g \n', Rd1);
fprintf(fid, 'Rl1= %g \n', Rl1);
fprintf(fid, 'Rs1dc= %g \n', Rs1dc);
fprintf(fid, 'Ls1= %g \n', Ls1);
fprintf(fid,'\n');

% The initial Vo2 secondary power stage
fprintf(fid, 'Vd2= %g \n', Vd2);
fprintf(fid, 'Rd2= %g \n', Rd2);
fprintf(fid, 'Rl2= %g \n', Rl2);
fprintf(fid, 'Rs2dc= %g \n', Rs2dc);
fprintf(fid, 'Ls2= %g \n', Ls2);
fprintf(fid,'\n');

% The initial weighting factors are
fprintf(fid, 'The initial guess of the weighting factors are \n')
fprintf(fid, 'K1= %g \n', x(1));
fprintf(fid, 'K2= %g \n', x(2));
fprintf(fid,'\n\n\n');

% Optimization convergence control variable.
options(2)=1e-4;
options(3)=1e-4;
options(4)=1e-4;
options(13)=1;      % indicate that there is one equality constraint
%options(14)=500;
options(17)=0.01;

% Invoke the optimization routine.
x=constr('dual_a',x,options)

% Store the value of the objective function
fobj=f;

% Check if the feasible solution is found.  If not, stacking the secondaries.
% dual_d.m formulates the objective function for stacked secondaries.
% STACK=0 means stacking routine has not been invoked.
% STACK=1 means stacking routine has been invoked once, etc.
STACK=0;
if NON_FEAS==1
        x=constr('dual_d',x,options)
        if NON_FEAS==0; % means feasible solution found
                STACK=1; %means feasible solution found for stacking
                fprintf(fid, 'Feasible solution found by stacking. \n\n');
        end
end
```

```
% Check if the feasible solution is found.
% If not, the circuit parameters will be swept over the given range
%    till the feasible solution is found.

while NON_FEAS == 1
        pcounter=0;

        % Sweep the circuit parameters on Vo1 secondary

                % Sweep the diode forward voltage drop
                for i=1:NP
                        if DVd1 == 0, break, end
                        Vd1=Vd1-DVd1;
                        % Invoke the optimization routine.
                        x=constr('dual_a',x,options)
                        if NON_FEAS == 0, break, end
                        if f > fobj
                          Vd1=Vd1+DVd1;
                          if i==1
                          fprintf(fid, 'Suggestion: change Vd1 in opposite direction. \n\n')
                          end
                         break
                        else
                                fobj=f;
                        end
                end
                        if NON_FEAS == 0, break, end

                % Sweep the output filter inductor resistance
                for i=1:NP
                        if DRl1 == 0, break, end
                        Rl1=Rl1-DRl1;
                        % Invoke the optimization routine.
                        x=constr('dual_a',x,options)
                        if NON_FEAS == 0, break, end
                end
                        if NON_FEAS == 0, break, end

                % Sweep the leakage inductance of the transformer
                for i=1:NP
                        if DLs1 == 0, break, end
                        Ls1=Ls1-DLs1;
                        % Invoke the optimization routine.
                        x=constr('dual_a',x,options)
                        if NON_FEAS == 0, break, end
                end
                        if NON_FEAS == 0, break, end

                % Sweep the diode small signal resistance
                for i=1:NP
```

```
            if DRd1 == 0, break, end
            Rd1=Rd1-DRd1;
            % Invoke the optimization routine.
            x=constr('dual_a',x,options)
            if NON_FEAS == 0, break, end
end
            if NON_FEAS == 0, break, end

% Sweep the secondary winding resistance
for i=1:NP
            if DRs1dc == 0, break, end
            Rs1dc=Rs1dc-DRs1dc;
            % Invoke the optimization routine.
            x=constr('dual_a',x,options)
            if NON_FEAS == 0, break, end
end
            if NON_FEAS == 0, break, end

% Sweep the circuit parameters on Vo2 secondary

% Sweep the diode forward voltage drop
for i=1:NP
            if DVd2 == 0, break, end
            Vd2=Vd2-DVd2;
            % Invoke the optimization routine.
            x=constr('dual_a',x,options)
            if NON_FEAS == 0, break, end
             if f > fobj
             Vd2=Vd2+DVd2;
              if i==1
              fprintf(fid, 'Suggestion: change Vd2 in opposite direction. \n\n')
              end
                    break
             else
                    fobj=f
             end
end
            if NON_FEAS == 0, break, end

% Sweep the output filter inductor resistance
for i=1:NP
            if DRl2 == 0, break, end
            Rl2=Rl2-DRl2;
            % Invoke the optimization routine.
            x=constr('dual_a',x,options)
            if NON_FEAS == 0, break, end
end
            if NON_FEAS == 0, break, end

% Sweep the leakage inductance of the transformer
for i=1:NP
```

```
                    if DLs2 == 0, break, end
                    Ls2=Ls2-DLs2;
                    % Invoke the optimization routine.
                    x=constr('dual_a',x,options)
                    if NON_FEAS == 0,break,end
                end
                    if NON_FEAS == 0,break,end

                % Sweep the diode small signal resistance
                for i=1:NP
                    if DRd2 == 0, break, end
                    Rd2=Rd2-DRd2;
                    % Invoke the optimization routine.
                    x=constr('dual_a',x,options)
                    if NON_FEAS == 0, break, end
                end
                    if NON_FEAS == 0, break, end

                % Sweep the secondary winding resistance
                for i=1:NP
                    if DRs2dc == 0, break, end
                    Rs2dc=Rs2dc-DRs2dc;
                    % Invoke the optimization routine.
                    x=constr('dual_a',x,options)
                    if NON_FEAS == 0, break, end
                end
                    if NON_FEAS == 0, break, end

        pcounter=pcounter+1;
        if pcounter == 1, break, end
end

if NON_FEAS == 0
disp('Good job! Feasible solution found. Ho! Ho!! Ho!!!')
fprintf(fid, 'Feasible solution found. \n\n');
end

if NON_FEAS == 1
disp('Sorry. No feasible solution found.')
fprintf(fid, 'No feasible solution found. \n\n')
fprintf(fid, 'Redesign power stage or respecify the regulation.  \n\n');
end

% Store the final design of the power stage

fprintf(fid, 'The final circuit parameters are \n\n')

% The autotransformer turns ratio
fprintf(fid, 'The autotransformer turns ratio \n')
fprintf(fid, 'N1auto= %g \n', N1auto);
fprintf(fid, 'N2auto= %g \n', N2auto);
```

```
fprintf(fid,'\n');

% The Vo1 secondary power stage
fprintf(fid, 'The Vo1 secondary power stage \n')
fprintf(fid, 'Vd1= %g \n', Vd1);
fprintf(fid, 'Rd1= %g \n', Rd1);
fprintf(fid, 'Rl1= %g \n', Rl1);
fprintf(fid, 'Rs1dc= %g \n', Rs1dc);
fprintf(fid, 'Ls1= %g \n', Ls1);
fprintf(fid,'\n');

% The Vo2 secondary power stage
fprintf(fid, 'The Vo2 secondary power stage \n')
fprintf(fid, 'Vd2= %g \n', Vd2);
fprintf(fid, 'Rd2= %g \n', Rd2);
fprintf(fid, 'Rl2= %g \n', Rl2);
fprintf(fid, 'Rs2dc= %g \n', Rs2dc);
fprintf(fid, 'Ls2= %g \n', Ls2);
fprintf(fid,'\n');

% The weighting factors are
fprintf(fid, 'The weighting factors are \n')
fprintf(fid, 'K1= %g \n', x(1));
fprintf(fid, 'K2= %g \n', x(2));
fprintf(fid,'\n');

% The parameters of the weighting network
% Assume R=1k
Rf=1;
Rf1=Rf*(1-x(1)-x(2))/x(1);
Rf2=Rf*(1-x(1)-x(2))/x(2);
fprintf(fid, 'The parameters of the weighting network are \n')
fprintf(fid, 'Rf= %g \n', Rf);
fprintf(fid, 'Rf1= %g \n', Rf1);
fprintf(fid, 'Rf2= %g \n', Rf2);

fclose(fid)

% If plotting dc regulation for given weighting factors only, use following.
% Otherwise comment the following line with "%".
x=[### ###]

% Invoking dual_b.m to plot the regulation characteristics.
dual_b(x)

% Invoking dual_c.m to plot the 3-D mesh of the objective function.
% This is optional.  If the user does not want it, he/she can comment the next line with "%".
dual_c(x)
```

****

% dual_a.m – calculate the function and constraint for dual.m
% The converter has two outputs, and each output is allowed to change over a certain range.

```
function [f,g] =dual_a(x)

% Define the global variable
global Fs Ts Dn Vinnom Vinmin Vinmax Vr Vin
global Vo1noms Vo1mins Vo1maxs Vo2noms Vo2mins Vo2maxs
global Io1min Io1max Io2min Io2max DI1 DI2
global Rpdc Rds Co Np Ns1 Ns2
global Vd1 Rd1 Rl1 Rs1dc Ls1 Vd2 Rd2 Rl2 Rs2dc Ls2
global N1 N2 N1auto N2auto
global NON_FEAS f NI W1 W2

% Combination a - Vo1max=Vo1(Io1min, Io2max)

Io1=Io1min;
Io2=Io2max;

%  Primary side
Ip=N1*Io1+N2*Io2;
Vp=Vin-Ip*(Rpdc+Rds);
Dldp=Fs*Co*Vp/Ip;
Dn=Dn+Dldp;

% Vo1 secondary side
Vs1=N1*Vp;
Delt1=Ls1*Io1/Vs1;
VA1a=Vs1-(Io1*Rs1dc);
VB1a=Vd1+Io1*(Fs*Ls1+Rd1+Rl1);

% Vo2 secondary side
Vs2=N2*Vp;
Delt2=Ls2*Io2/Vs2;
VA2a=Vs2-(Io2*Rs2dc);
VB2a=Vd2+Io2*(Fs*Ls2+Rd2+Rl2);

% Effective duty cycle De
Dea=(Vr+x(1)*VB1a+x(2)*VB2a)/(x(1)*VA1a+x(2)*VA2a);

% The maximum output voltage Vo1max
Vo1max=Dea*VA1a-VB1a;

% The minimum output voltage Vo2min
Vo2min=Dea*VA2a-VB2a;

% Combination b - Vo1min=Vo1(Io1max, Io2min)
```

```
Io1=Io1max;
Io2=Io2min;

% Primary side
Ip=N1*Io1+N2*Io2;
Vp=Vin-Ip*(Rpdc+Rds);
Dldp=Fs*Co*Vp/Ip;
Dn=Dn+Dldp;

% Vo1 secondary side
Vs1=N1*Vp;
Delt1=Ls1*Io1/Vs1;
VA1b=Vs1-(Io1*Rs1dc);
VB1b=Vd1+Io1*(Fs*Ls1+Rd1+Rl1);

% Vo2 secondary side
Vs2=N2*Vp;
Delt2=Ls2*Io2/Vs2;
VA2b=Vs2-(Io2*Rs2dc);
VB2b=Vd2+Io2*(Fs*Ls2+Rd2+Rl2);

% Effective duty cycle De
Deb=(Vr+x(1)*VB1b+x(2)*VB2b)/(x(1)*VA1b+x(2)*VA2b);

% The minimum output voltage Vo1min
Vo1min=Deb*VA1b-VB1b;

% The maximum output voltage Vo2max
Vo2max=Deb*VA2b-VB2b;

% Objective function
f=(Vo1max-Vo1noms)^2+(Vo1min-Vo1noms)^2+(Vo2max-Vo2noms)^2+(Vo2min-Vo2noms)^2;

% g(1) - Equality constraint constraints
g(1)=Vo1noms*x(1)+Vo2noms*x(2)-Vr;

% g(2) - g(7) -- inequality (g(i)<=0)
g(2)=Vo1mins-Vo1min;
g(3)=Vo1max-Vo1maxs;
g(4)=Vo2mins-Vo2min;
g(5)=Vo2max-Vo2maxs;

% g(6) - g(7) -- guarantee the weighting factors =>0
g(6)=-x(1);
g(7)=-x(2);
□
```

```
**********************************************************
```

```
% dual_b.m -- calculate and plot the output voltages for dual.m after optimization
% The converter has two outputs, and each output is allowed
%       to change over a certain range.

function dual_b(x)

% Define the global variable
global Fs Ts Dn Vinnom Vinmin Vinmax Vr Vin
global Vo1noms Vo1mins Vo1maxs Vo2noms Vo2mins Vo2maxs
global Io1min Io1max Io2min Io2max DI1 DI2
global Rpdc Rds Co Np Ns1 Ns2
global Vd1 Rd1 Rl1 Rs1dc Ls1 Vd2 Rd2 Rl2 Rs2dc Ls2
global N1 N2 N1auto N2auto
global NON_FEAS f NI W1 W2
global STACK Nss1 Nss2 STACK_OK

K1=x(1);
K2=x(2);

% There are 2 combinations of load currents to consider.  Each combination represents an extreme
%       operation condition, which corresponds to either a minimum or maximum voltage.

% If stacking yields a feasible solution, i.e., STACK=1, use stacked scheme to calculate the outputs.
%       Otherwise, calculate the outputs with non-stacked scheme.

if STACK==1

        % Combination a - Vo1max=Vo1(Io1min, Io2max)

        Io1=Io1min:DI1:Io1max;
        Io2=Io2max;

        %  Primary side
        Ip=Nss1*(Io1+Io2)+Nss2*Io2;
        Vp=Vin-Ip*(Rpdc+Rds);

        % Vo1 secondary side
        Vs1=Nss1*Vp;
        VA1a=Vs1-(Io1*Rs1dc+Io2*(Rs1dc+Rd1));
        VB1a=Vd1+Io1*(Fs*Ls1+Rd1+Rl1)+Io2*Ls1*Fs;

        % Vo2 secondary side
        Vs2=Nss2*Vp;
        VA2a=Vs1+Vs2-Vd1-Io1*(Rs1dc+Rd1)-Io2*(Rs1dc+Rd1+Rs2dc);
        VB2a=Vd2+Io1*Ls1*Fs+Io2*(Fs*(Ls2+Ls1)+Rd2+Rl2);

        % Effective duty cycle De
```

```
        Dea=(Vr+K1*VB1a+K2*VB2a)./(K1*VA1a+K2*VA2a);

        % The maximum output voltage Vo1max
        Vo1max=Dea.*VA1a-VB1a;

        % The minimum output voltage Vo2min
        Vo2min=Dea.*VA2a-VB2a;

        % Combination b - Vo1min=Vo1(Io1max, Io2min)

        Io1=Io1min:DI1:Io1max;
        Io2=Io2min;

        %  Primary side
        Ip=Nss1*(Io1+Io2)+Nss2*Io2;
        Vp=Vin-Ip*(Rpdc+Rds);

        % Vo1 secondary side
        Vs1=Nss1*Vp;
        VA1b=Vs1-(Io1*Rs1dc+Io2*(Rs1dc+Rd1));
        VB1b=Vd1+Io1*(Fs*Ls1+Rd1+Rl1)+Io2*Ls1*Fs;

        % Vo2 secondary side
        Vs2=Nss2*Vp;
        VA2b=Vs1+Vs2-Vd1-Io1*(Rs1dc+Rd1)-Io2*(Rs1dc+Rd1+Rs2dc);
        VB2b=Vd2+Io1*Ls1*Fs+Io2*(Fs*(Ls2+Ls1)+Rd2+Rl2);

        % Effective duty cycle De
        Deb=(Vr+K1*VB1b+K2*VB2b)./(K1*VA1b+K2*VA2b);

        % The minimum output voltage Vo1min
        Vo1min=Deb.*VA1b-VB1b;

        % The maximum output voltage Vo2max
        Vo2max=Deb.*VA2b-VB2b;

end

% If stacking does not yield feasible solution, i.e., STACK=0, use following.

if STACK==0

        % Combination a - Vo1max=Vo1(Io1min, Io2max)

        Io1=Io1min:DI1:Io1max;
        Io2=Io2max;

        %  Primary side
        Ip=N1*Io1+N2*Io2;
        Vp=Vin-Ip*(Rpdc+Rds);
```

```
% Vo1 secondary side
Vs1=N1*Vp;
VA1a=Vs1-(Io1*Rs1dc);
VB1a=Vd1+Io1*(Fs*Ls1+Rd1+Rl1);

% Vo2 secondary side
Vs2=N2*Vp;
VA2a=Vs2-(Io2*Rs2dc);
VB2a=Vd2+Io2*(Fs*Ls2+Rd2+Rl2);

% Effective duty cycle De
Dea=(Vr+K1*VB1a+K2*VB2a)./(K1*VA1a+K2*VA2a);

% The maximum output voltage Vo1max
Vo1max=Dea.*VA1a-VB1a;

% The minimum output voltage Vo2min
Vo2min=Dea.*VA2a-VB2a;

        % Combination b - Vo1min=Vo1(Io1max, Io2min)

Io1=Io1min:DI1:Io1max;
Io2=Io2min;

%  Primary side
Ip=N1*Io1+N2*Io2;
Vp=Vin-Ip*(Rpdc+Rds);
Dldp=Fs*Co*Vp/Ip;
Dn=Dn+Dldp;

% Vo1 secondary side
Vs1=N1*Vp;
Delt1=Ls1*Io1./Vs1;
VA1b=Vs1-(Io1*Rs1dc);
VB1b=Vd1+Io1*(Fs*Ls1+Rd1+Rl1);

% Vo2 secondary side
Vs2=N2*Vp;
Delt2=Ls2*Io2./Vs2;
VA2b=Vs2-(Io2*Rs2dc);
VB2b=Vd2+Io2*(Fs*Ls2+Rd2+Rl2);

% Effective duty cycle De
Deb=(Vr+K1*VB1b+K2*VB2b)./(K1*VA1b+K2*VA2b);

% The minimum output voltage Vo1min
Vo1min=Deb.*VA1b-VB1b;

% The maximum output voltage Vo2max
Vo2max=Deb.*VA2b-VB2b;
```

```
end

% Plot output 1
Io1=Io1min:DI1:Io1max;
figure(1);
subplot(2,1,1);
plot(Io1, Vo1min,'r-',Io1, Vo1max, 'g--')
title('Output 1')
xlabel('Io1(A)')
ylabel('Vo1(V)')
gtext('Io2min')
gtext('Io2max')

% Plot output 2
%Io2=Io2min:DI2:Io2max;
%figure(2);
subplot(2,1,2);
plot(Io1, Vo2min,'r-',Io1, Vo2max, 'g--')
title('Output 2')
xlabel('Io1(A)')
ylabel('Vo2(V)')
gtext('Io2min')
gtext('Io2max')

% Print output to the file output9.dat
y=[Io1' Vo1min' Vo1max' Io1' Vo2min' Vo2max']';
fid=fopen('output9.dat', 'w');
fprintf(fid, 'Io1(A) Vo1min(V) Vo1max(V) Io1(A) Vo2min(V) Vo2max(V) \n')
fprintf(fid, '%5.2f %9.4f %9.4f %6.2f %9.4f %9.4f \n', y)
fclose(fid)
```

****

% dual_c.m – calculate the 3-D graph of the objective function for delta9.m

```
% The converter has 2 outputs, and correspondingly 2 weighting factors K1, K2.

function dual_c(x)

format long

% Define the global variable
global Fs Ts Dn Vinnom Vinmin Vinmax Vr Vin
global Vo1noms Vo1mins Vo1maxs Vo2noms Vo2mins Vo2maxs
global Io1min Io1max Io2min Io2max DI1 DI2
global Rpdc Rds Co Np Ns1 Ns2
global Vd1 Rd1 Rl1 Rs1dc Ls1 Vd2 Rd2 Rl2 Rs2dc Ls2
global N1 N2 N1auto N2auto
```

```
global NON_FEAS f NI W1 W2 K1 K2

% Variation of the weighting factors K1 and K2
NK=20;
K1MAX=1;
K1MIN=0.075;
DK1=(K1MAX-K1MIN)/NK;
K2MAX=1;
K2MIN=0.075;
DK2=(K2MAX-K2MIN)/NK
K1=K1MIN:DK1:K1MAX;
K2=K2MIN:DK2:K2MAX;
[X,Y]=meshgrid(K1,K2);
%pause

% Combination a - Vo1max=Vo1(Io1min, Io2max)

Io1=Io1min
Io2=Io2max;

%  Primary side
Ip=N1*Io1+N2*Io2;
Vp=Vin-Ip*(Rpdc+Rds);
%Dldp=Fs*Co*Vp/Ip;
%Dn=Dn+Dldp;

% Vo1 secondary side
Vs1=N1*Vp;
%Delt1=Ls1*Io1/Vs1;
VA1a=Vs1-(Io1*Rs1dc);
VB1a=Vd1+Io1*(Fs*Ls1+Rd1+Rl1);

% Vo2 secondary side
Vs2=N2*Vp;
%Delt2=Ls2*Io2/Vs2;
VA2a=Vs2-(Io2*Rs2dc);
VB2a=Vd2+Io2*(Fs*Ls2+Rd2+Rl2);

% Effective duty cycle De
Dea=(Vr+X*VB1a+Y*VB2a)./(X*VA1a+Y*VA2a);

% The maximum output voltage Vo1max
Vo1max=Dea*VA1a-VB1a;

% The minimum output voltage Vo2min
Vo2min=Dea*VA2a-VB2a;

% Combination b - Vo1min=Vo1(Io1max, Io2min)

Io1=Io1max;
Io2=Io2min;
```

```
% Primary side
Ip=N1*Io1+N2*Io2;
Vp=Vin-Ip*(Rpdc+Rds);
Dldp=Fs*Co*Vp/Ip;
Dn=Dn+Dldp;

% Vo1 secondary side
Vs1=N1*Vp;
Delt1=Ls1*Io1/Vs1;
VA1b=Vs1-(Io1*Rs1dc);
VB1b=Vd1+Io1*(Fs*Ls1+Rd1+Rl1);

% Vo2 secondary side
Vs2=N2*Vp;
Delt2=Ls2*Io2/Vs2;
VA2b=Vs2-(Io2*Rs2dc);
VB2b=Vd2+Io2*(Fs*Ls2+Rd2+Rl2);

% Effective duty cycle De
Deb=(Vr+X*VB1b+Y*VB2b)./(X*VA1b+Y*VA2b);

% The minimum output voltage Vo1min
Vo1min=Deb*VA1b-VB1b;

% The maximum output voltage Vo2max
Vo2max=Deb*VA2b-VB2b;

% Objective function
f=(Vo1max-Vo1noms).^2+(Vo1min-Vo1noms).^2+(Vo2max-Vo2noms).^2+(Vo2min-Vo2noms).^2;

% Save the data to the file objfunc.asc
mat=[K2' f];
mat1=[0 K1; mat];
save objfunc.asc mat1 -ascii -tabs

% Plot mesh
figure(2);
%subplot(1,2,1)
mesh(K1,K2,f)
xlabel('K1')
ylabel('K2')
zlabel('f - objective funcion')
grid on

% Plot contour
figure(3);
%subplot(1,2,2);
contour(K1,K2,f,20)
xlabel('K1')
ylabel('K2')
```

A.2 Triple-Output Converters

```
% triple.m – Invoking optimization routine to calculate weighting factors k1,k2, and k3.
% The objective function and constraints are stored in triple_a.m.
% The triple_b.m is used to plot the output regulation.
% The final results are stored in triple_out.dat

% Define the global variable
global Fs Ts Dn Vinnom Vinmin Vinmax Vin Vr
global Vo1noms Vo1mins Vo1maxs Vo2noms Vo2mins Vo2maxs Vo3noms Vo3mins Vo3maxs
global Io1min Io1max Io2min Io2max Io3min Io3max DI1 DI2 DI3
global Rpdc Rds Co Np Ns1 Ns2 Ns3
global Vd1 Rd1 Rl1 Rs1dc Ls1 Vd2 Rd2 Rl2 Rs2dc Ls2 Vd3 Rd3 Rl3 Ls3 Rs3dc
global N1 N2 N3 N1auto N2auto N3auto
global NON_FEAS f NI W1 W2 W3

% Optimization objective function weighting
% If Vo1 is more important than Vo2, and Vo2 more important than Vo3, let W1>W2>W3, e.g.,
%   W1=3, W2=2, W3=1. If Vo1, Vo2 and Vo3 are of the same importance, let W1=W2=W3=1.
W1=1;
W2=1;
W3=1;

% Design specifications

Fs=###;          % Switching frequency
Ts=1/Fs;         % Switching period

% Input voltage range
Vinnom=###;      % Nominal input line voltage
Vinmin=###;      % Minimum input line voltage
Vinmax=###;      % Maximum input line voltage

% The design is performed at the nominal line
Vin=Vinnom;

% Reference voltage
Vr=###;

% Specified output voltage range
Vo1noms=###;
Vo1mins=###;
Vo1maxs=###;
Vo2noms=###;
Vo2mins=###;
Vo2maxs=###;
```

```
Vo3noms=###;
Vo3mins=###;
Vo3maxs=###;

% Load range
Io1min=###;
Io1max=###;
Io2min=###;
Io2max=###;
Io3min=###;
Io3max=###;

% Step size of the load current
NI=10;
DI1=(Io1max-Io1min)/NI;
DI2=(Io2max-Io2min)/NI;
DI3=(Io3max-Io3min)/NI;

% Primary circuit parameters

Rpdc=###;
Rds=###;
Co=###;

% Transformer turns
Np=###;
Ns1=###;
Ns2=###;
Ns3=###;

% Transformer turns ratio
N1=Ns1/Np;      % N1-N3 can use measured values.
N2=Ns2/Np;
N3=Ns3/Np;

% If the autotransformers are used on the secondaries, or,
N1auto=###;
N2auto=###;
N3auto=###;

% then the real transformer turns ratios are
N1=N1*N1auto;
N2=N2*N2auto;
N3=N3*N3auto;

% Vo1 secondary circuit parameters
Vd1=###;
Rd1=###;
Rl1=###;
Rs1dc=###;
Ls1=###;
```

```
% Number of division of the secondary circuit parameters between the given and minimum values
NP=4;

% Lower limit of Vo1 secondary circuit parameters
% If the circuit parameters are not allowed to change, simply set them
%       equal to the original values, e.g., Vd1min=Vd1.
Vd1min=###;
Rd1min=###;
Rl1min=###;
Rs1dcmin=###;
Ls1min=###;

% Number of division of the secondary circuit parameters between the given and minimum values
NP=4;

% Increment of Vo1 secondary circuit parameters
DVd1=(Vd1-Vd1min)/NP;
DRl1=(Rl1-Rl1min)/NP;
DLs1=(Ls1-Ls1min)/NP;
DRd1=(Rd1-Rd1min)/NP;
DRs1dc=(Rs1dc-Rs1dcmin)/NP;
DLs1=(Ls1-Ls1min)/NP;

% Vo2 secondary circuit parameters
Vd2=###;
Rd2=###;
Rl2=###;
Rs2dc=###;
Ls2=###;

% Lower limit of Vo2 secondary circuit parameters
% If the circuit parameters are not allowed to change, simply set them equal to the original values.
Vd2min=###;
Rd2min=###;
Rl2min=###;
Rs2dcmin=###;
Ls2min=###;

% Increment of Vo2 secondary circuit parameters
DVd2=(Vd2-Vd2min)/NP;
DRl2=(Rl2-Rl2min)/NP;
DLs2=(Ls2-Ls2min)/NP;
DRd2=(Rd2-Rd2min)/NP;
DRs2dc=(Rs2dc-Rs2dcmin)/NP;
DLs2=(Ls2-Ls2min)/NP;

% Vo3 secondary circuit parameters
Vd3=###;
Rd3=###;
Rl3=###;
```

```
Rs3dc=###;
Ls3=###;

% Lower limit of Vo3 secondary circuit parameters
% If the circuit parameters are not allowed to change, simply set them equal to the original values.
Vd3min=###;
Rd3min=###;
Rl3min=###;
Rs3dcmin=###;
Ls3min=###;

% Increment of Vo3 secondary circuit parameters
DVd3=(Vd3-Vd3min)/NP;
DRl3=(Rl3-Rl3min)/NP;
DLs3=(Ls3-Ls3min)/NP;
DRd3=(Rd3-Rd3min)/NP;
DRs3dc=(Rs3dc-Rs3dcmin)/NP;
DLs3=(Ls3-Ls3min)/NP;

% Making a starting guess at the solution.
x= [###, ###, ###]

% Open the output file
fid =fopen('triple_out.dat', 'w');

fprintf(fid, 'The initial circuit parameters are \n');
fprintf(fid,'\n');

% The initial Vo1 secondary power stage
fprintf(fid, 'Vd1= %g \n', Vd1);
fprintf(fid, 'Rd1= %g \n', Rd1);
fprintf(fid, 'Rl1= %g \n', Rl1);
fprintf(fid, 'Rs1dc= %g \n', Rs1dc);
fprintf(fid, 'Ls1= %g \n', Ls1);
fprintf(fid,'\n');

% The initial Vo2 secondary power stage
fprintf(fid, 'Vd2= %g \n', Vd2);
fprintf(fid, 'Rd2= %g \n', Rd2);
fprintf(fid, 'Rl2= %g \n', Rl2);
fprintf(fid, 'Rs2dc= %g \n', Rs2dc);
fprintf(fid, 'Ls2= %g \n', Ls2);
fprintf(fid,'\n');

% The initial Vo3 secondary power stage
fprintf(fid, 'Vd3= %g \n', Vd3);
fprintf(fid, 'Rd3= %g \n', Rd3);
fprintf(fid, 'Rl3= %g \n', Rl3);
fprintf(fid, 'Rs3dc= %g \n', Rs3dc);
fprintf(fid, 'Ls3= %g \n', Ls3);
fprintf(fid,'\n');
```

```
% The initial weighting factors are
fprintf(fid, 'The weighting factors are \n')
fprintf(fid, 'K1= %g \n', x(1));
fprintf(fid, 'K2= %g \n', x(2));
fprintf(fid, 'K3= %g \n', x(3));
fprintf(fid,'\n\n\n');

% Optimization convergence control variable.
options(2)=1e-4;
options(3)=1e-4;
options(4)=1e-4;
options(13)=1;      % indicate that there is one equality constraint
%options(14)=500;
options(17)=0.01;

% Invoke the optimization routine.
x=constr('triple_a',x,options)

% Store the value of the objective function
fobj=f

% Check if the feasible solution is found.
% If not, the circuit parameters will be swept over the given range
% till the feasible solution is found.

while NON_FEAS == 1
        pcounter=0;

        % Sweep the circuit parameters on Vo1 secondary

                % Sweep the diode forward voltage drop
                for i=1:NP
                        if DVd1 == 0, break, end
                        Vd1=Vd1-DVd1
                        % Invoke the optimization routine.
                        x=constr('triple_a',x,options)
                        if NON_FEAS == 0, break, end
                        if f > fobj
                          Vd1=Vd1+DVd1
                          if i==1
                          fprintf(fid, 'Suggestion: change Vd1 in opposite direction. \n\n')
                          end
                         break
                        else
                                fobj=f
                        end
                end
                        if NON_FEAS == 0, break, end

                % Sweep the output filter inductor resistance
```

```
for i=1:NP
        if DRl1 == 0, break, end
        Rl1=Rl1-DRl1
        % Invoke the optimization routine.
        x=constr('triple_a',x,options)
        if NON_FEAS == 0, break, end
end
        if NON_FEAS == 0, break, end

% Sweep the leakage inductance of the transformer
for i=1:NP
        if DLs1 == 0, break, end
        Ls1=Ls1-DLs1
        % Invoke the optimization routine.
        x=constr('triple_a',x,options)
        if NON_FEAS == 0, break, end
end
        if NON_FEAS == 0, break, end

% Sweep the diode small signal resistance
for i=1:NP
        if DRd1 == 0, break, end
        Rd1=Rd1-DRd1
        % Invoke the optimization routine.
        x=constr('triple_a',x,options)
        if NON_FEAS == 0, break, end
end
        if NON_FEAS == 0, break, end

% Sweep the secondary winding resistance
for i=1:NP
        if DRs1dc == 0, break, end
        Rs1dc=Rs1dc-DRs1dc
        % Invoke the optimization routine.
        x=constr('triple_a',x,options)
        if NON_FEAS == 0, break, end
end
        if NON_FEAS == 0, break, end

% Sweep the circuit parameters on Vo2 secondary

        % Sweep the diode forward voltage drop
        for i=1:NP
                if DVd2 == 0, break, end
                Vd2=Vd2-DVd2
                % Invoke the optimization routine.
                x=constr('triple_a',x,options)
                if NON_FEAS == 0, break, end
                 if f > fobj
                 Vd2=Vd2+DVd2
                  if i==1
```

```
                fprintf(fid, 'Suggestion: change Vd2 in opposite direction. \n\n')
                end
                        break
                else
                        fobj=f
                end
        end
                if NON_FEAS == 0, break, end

        % Sweep the output filter inductor resistance
        for i=1:NP
                if DRl2 == 0, break, end
                Rl2=Rl2-DRl2
                % Invoke the optimization routine.
                x=constr('triple_a',x,options)
                if NON_FEAS == 0, break, end
        end
                if NON_FEAS == 0, break, end

        % Sweep the leakage inductance of the transformer
        for i=1:NP
                if DLs2 == 0, break, end
                Ls2=Ls2-DLs2
                % Invoke the optimization routine.
                x=constr('triple_a',x,options)
                if NON_FEAS == 0, break, end
        end
                if NON_FEAS == 0, break, end

        % Sweep the diode small signal resistance
        for i=1:NP
                if DRd2 == 0, break, end
                Rd2=Rd2-DRd2
                % Invoke the optimization routine.
                x=constr('triple_a',x,options)
                if NON_FEAS == 0, break, end
        end
                if NON_FEAS == 0, break, end

        % Sweep the secondary winding resistance
        for i=1:NP
                if DRs2dc == 0, break, end
                Rs2dc=Rs2dc-DRs2dc
                % Invoke the optimization routine.
                x=constr('triple_a',x,options)
                if NON_FEAS == 0, break, end
        end
                if NON_FEAS == 0, break, end

% Sweep the circuit parameters on Vo3 secondary
```

```
% Sweep the diode forward voltage drop
for i=1:NP
        if DVd3 == 0, break, end
        Vd3=Vd3-DVd3
        % Invoke the optimization routine.
        x=constr('triple_a',x,options)
        if NON_FEAS == 0, break, end
         if f > fobj
         Vd3=Vd3+DVd3
          if i==1
          fprintf(fid, 'Suggestion: change Vd3 in opposite direction. \n\n')
          end
                break
         else
                fobj=f
         end

end
        if NON_FEAS == 0, break, end

% Sweep the output filter inductor resistance
for i=1:NP
        if DRl3 == 0, break, end
        Rl3=Rl3-DRl3
        % Invoke the optimization routine.
        x=constr('triple_a',x,options)
        if NON_FEAS == 0, break, end
end
        if NON_FEAS == 0, break, end

% Sweep the leakage inductance of the transformer
for i=1:NP
        if DLs3 == 0, break, end
        Ls3=Ls3-DLs3
        % Invoke the optimization routine.
        x=constr('triple_a',x,options)
        if NON_FEAS == 0, break, end
end
        if NON_FEAS == 0, break, end

% Sweep the diode small signal resistance
for i=1:NP
        if DRd3 == 0, break, end
        Rd3=Rd3-DRd3
        % Invoke the optimization routine.
        x=constr('triple_a',x,options)
        if NON_FEAS == 0, break, end
end
        if NON_FEAS == 0, break, end

% Sweep the secondary winding resistance
```

```
                for i=1:NP
                        if DRs3dc == 0, break, end
                        Rs3dc=Rs3dc-DRs3dc
                        % Invoke the optimization routine.
                        x=constr('triple_a',x,options)
                        if NON_FEAS == 0, break, end
                end
                        if NON_FEAS == 0, break, end

        pcounter=pcounter+1
        if pcounter == 1, break, end
end

if NON_FEAS == 0
disp('Good job, man. Feasible solution found.')
fprintf(fid, 'Feasible solution found. \n\n');
end

if NON_FEAS == 1
disp('Sorry, man. No feasible solution found.')
fprintf(fid, 'No feasible solution found. \n\n')
fprintf(fid, 'Redesign power stage or respecify the regulation.  \n\n');
end

% Store the final design of the power stage
fprintf(fid, 'The final circuit parameters are \n\n')

% The autotransformer turns ratio
fprintf(fid, 'The autotransformer turns ratio \n')
fprintf(fid, 'N1auto= %g \n', N1auto);
fprintf(fid, 'N2auto= %g \n', N2auto);
fprintf(fid, 'N3auto= %g \n', N3auto);
fprintf(fid,'\n');

% The Vo1 secondary power stage
fprintf(fid, 'Vd1= %g \n', Vd1);
fprintf(fid, 'Rd1= %g \n', Rd1);
fprintf(fid, 'Rl1= %g \n', Rl1);
fprintf(fid, 'Rs1dc= %g \n', Rs1dc);
fprintf(fid, 'Ls1= %g \n', Ls1);
fprintf(fid,'\n');

% The Vo2 secondary power stage
fprintf(fid, 'Vd2= %g \n', Vd2);
fprintf(fid, 'Rd2= %g \n', Rd2);
fprintf(fid, 'Rl2= %g \n', Rl2);
fprintf(fid, 'Rs2dc= %g \n', Rs2dc);
fprintf(fid, 'Ls2= %g \n', Ls2);
fprintf(fid,'\n');

% The Vo3 secondary power stage
```

```
fprintf(fid, 'Vd3= %g \n', Vd3);
fprintf(fid, 'Rd3= %g \n', Rd3);
fprintf(fid, 'Rl3= %g \n', Rl3);
fprintf(fid, 'Rs3dc= %g \n', Rs3dc);
fprintf(fid, 'Ls3= %g \n', Ls3);
fprintf(fid,'\n');

% The weighting factors are
fprintf(fid, 'The weighting factors are \n')
fprintf(fid, 'K1= %g \n', x(1));
fprintf(fid, 'K2= %g \n', x(2));
fprintf(fid, 'K3= %g \n', x(3));
fprintf(fid,'\n');

% The parameters of the weighting network
% Assume R=1k
Rf=1;
Rf1=Rf*(1-x(1)-x(2)-x(3))/x(1);
Rf2=Rf*(1-x(1)-x(2)-x(3))/x(2);
Rf3=Rf*(1-x(1)-x(2)-x(3))/x(3);
fprintf(fid, 'The parameters of the weighting network are \n')
fprintf(fid, 'Rf= %g \n', Rf);
fprintf(fid, 'Rf1= %g \n', Rf1);
fprintf(fid, 'Rf2= %g \n', Rf2);
fprintf(fid, 'Rf3= %g \n', Rf3);
fclose(fid)

% Invoking triple_b.m to plot the regulation characteristics.
% If only dc regulation is of interest, use the following x.  Otherwise, comment it.
%x=[0.1256 0.1788 0.1054]
triple_b(x)
```

****

% triple_a.m -- calculate the function and constraint for delta8.m

```
% The converter has three outputs, and each output is allowed
%  to change over a certain range.


function [f,g] =triple_a(x)

% Define the global variable
global Fs Ts Dn Vinnom Vinmin Vinmax Vin Vr
global Vo1noms Vo1mins Vo1maxs Vo2noms Vo2mins Vo2maxs Vo3noms Vo3mins Vo3maxs
global Io1min Io1max Io2min Io2max Io3min Io3max DI1 DI2 DI3
global Rpdc Rds Co Np Ns1 Ns2 Ns3
global Vd1 Rd1 Rl1 Rs1dc Ls1 Vd2 Rd2 Rl2 Rs2dc Ls2 Vd3 Rd3 Rl3 Ls3 Rs3dc
```

```
global N1 N2 N3 N1auto N2auto N3auto
global NON_FEAS f NI W1 W2 W3

% There are 6 combinations of load currents to consider. Each combination represents an extreme
operation condition, which corresponds to either a minimum or maximum voltage.

% Combination a - Vo1max=Vo1(Io1min, Io2max, Io3max)

Io1=Io1min;
Io2=Io2max;
Io3=Io3max;

% Primary side
Ip=N1*Io1+N2*Io2+N3*Io3;
Vp=Vin-Ip*(Rpdc+Rds);
Dldp=Fs*Co*Vp/Ip;
Dn=Dn+Dldp;

% Vo1 secondary side
Vs1=N1*Vp;
Delt1=Ls1*Io1/Vs1;
VA1a=Vs1-(Io1*Rs1dc);
VB1a=Vd1+Io1*(Fs*Ls1+Rd1+Rl1);

% Vo2 secondary side
Vs2=N2*Vp;
Delt2=Ls2*Io2/Vs2;
VA2a=Vs2-(Io2*Rs2dc);
VB2a=Vd2+Io2*(Fs*Ls2+Rd2+Rl2);

% Vo3 secondary side
Vs3=N3*Vp;
Delt3=Ls3*Io3/Vs3;
VA3a=Vs3-(Io3*Rs3dc);
VB3a=Vd3+Io3*(Fs*Ls3+Rd3+Rl3);

% Effective duty cycle De
Dea=(Vr+x(1)*VB1a+x(2)*VB2a+x(3)*VB3a)/(x(1)*VA1a+x(2)*VA2a+x(3)*VA3a);

% The maximum output voltage Vo1max
Vo1max=Dea*VA1a-VB1a;

% Combination b - Vo1min=Vo1(Io1max, Io2min, Io3min)

Io1=Io1max;
Io2=Io2min;
Io3=Io3min;

% Primary side
Ip=N1*Io1+N2*Io2+N3*Io3;
Vp=Vin-Ip*(Rpdc+Rds);
```

```
Dldp=Fs*Co*Vp/Ip;
Dn=Dn+Dldp;

% Vo1 secondary side
Vs1=N1*Vp;
Delt1=Ls1*Io1/Vs1;
VA1b=Vs1-(Io1*Rs1dc);
VB1b=Vd1+Io1*(Fs*Ls1+Rd1+Rl1);

% Vo2 secondary side
Vs2=N2*Vp;
Delt2=Ls2*Io2/Vs2;
VA2b=Vs2-(Io2*Rs2dc);
VB2b=Vd2+Io2*(Fs*Ls2+Rd2+Rl2);

% Vo3 secondary side
Vs3=N3*Vp;
Delt3=Ls3*Io3/Vs3;
VA3b=Vs3-(Io3*Rs3dc);
VB3b=Vd3+Io3*(Fs*Ls3+Rd3+Rl3);

% Effective duty cycle De
Deb=(Vr+x(1)*VB1b+x(2)*VB2b+x(3)*VB3b)/(x(1)*VA1b+x(2)*VA2b+x(3)*VA3b);

% The minimum output voltage Vo1min
Vo1min=Deb*VA1b-VB1b;

% Combination c - Vo2max=Vo2(Io1max, Io2min, Io3max)

Io1=Io1max;
Io2=Io2min;
Io3=Io3max;

%  Primary side
Ip=N1*Io1+N2*Io2+N3*Io3;
Vp=Vin-Ip*(Rpdc+Rds);
Dldp=Fs*Co*Vp/Ip;
Dn=Dn+Dldp;

% Vo1 secondary side
Vs1=N1*Vp;
Delt1=Ls1*Io1/Vs1;
VA1c=Vs1-(Io1*Rs1dc);
VB1c=Vd1+Io1*(Fs*Ls1+Rd1+Rl1);

% Vo2 secondary side
Vs2=N2*Vp;
Delt2=Ls2*Io2/Vs2;
VA2c=Vs2-(Io2*Rs2dc);
VB2c=Vd2+Io2*(Fs*Ls2+Rd2+Rl2);
```

```
% Vo3 secondary side
Vs3=N3*Vp;
Delt3=Ls3*Io3/Vs3;
VA3c=Vs3-(Io3*Rs3dc);
VB3c=Vd3+Io3*(Fs*Ls3+Rd3+Rl3);

% Effective duty cycle De
Dec=(Vr+x(1)*VB1c+x(2)*VB2c+x(3)*VB3c)/(x(1)*VA1c+x(2)*VA2c+x(3)*VA3c);

% The maximum output voltage Vo2max
Vo2max=Dec*VA2c-VB2c;

% Combination d - Vo2min=Vo2(Io1min, Io2max, Io3min)

Io1=Io1min;
Io2=Io2max;
Io3=Io3min;

%  Primary side
Ip=N1*Io1+N2*Io2+N3*Io3;
Vp=Vin-Ip*(Rpdc+Rds);
Dldp=Fs*Co*Vp/Ip;
Dn=Dn+Dldp;

% Vo1 secondary side
Vs1=N1*Vp;
Delt1=Ls1*Io1/Vs1;
VA1d=Vs1-(Io1*Rs1dc);
VB1d=Vd1+Io1*(Fs*Ls1+Rd1+Rl1);

% Vo2 secondary side
Vs2=N2*Vp;
Delt2=Ls2*Io2/Vs2;
VA2d=Vs2-(Io2*Rs2dc);
VB2d=Vd2+Io2*(Fs*Ls2+Rd2+Rl2);

% Vo3 secondary side
Vs3=N3*Vp;
Delt3=Ls3*Io3/Vs3;
VA3d=Vs3-(Io3*Rs3dc);
VB3d=Vd3+Io3*(Fs*Ls3+Rd3+Rl3);

% Effective duty cycle De
Ded=(Vr+x(1)*VB1d+x(2)*VB2d+x(3)*VB3d)/(x(1)*VA1d+x(2)*VA2d+x(3)*VA3d);

% The minimum output voltage Vo2min
Vo2min=Ded*VA2d-VB2d;

% Combination e - Vo3max=Vo3(Io1max, Io2max, Io3min)

Io1=Io1max;
```

```
Io2=Io2max;
Io3=Io3min;

% Primary side
Ip=N1*Io1+N2*Io2+N3*Io3;
Vp=Vin-Ip*(Rpdc+Rds);
Dldp=Fs*Co*Vp/Ip;
Dn=Dn+Dldp;

% Vo1 secondary side
Vs1=N1*Vp;
Delt1=Ls1*Io1/Vs1;
VA1e=Vs1-(Io1*Rs1dc);
VB1e=Vd1+Io1*(Fs*Ls1+Rd1+Rl1);

% Vo2 secondary side
Vs2=N2*Vp;
Delt2=Ls2*Io2/Vs2;
VA2e=Vs2-(Io2*Rs2dc);
VB2e=Vd2+Io2*(Fs*Ls2+Rd2+Rl2);

% Vo3 secondary side
Vs3=N3*Vp;
Delt3=Ls3*Io3/Vs3;
VA3e=Vs3-(Io3*Rs3dc);
VB3e=Vd3+Io3*(Fs*Ls3+Rd3+Rl3);

% Effective duty cycle De
Dee=(Vr+x(1)*VB1e+x(2)*VB2e+x(3)*VB3e)/(x(1)*VA1e+x(2)*VA2e+x(3)*VA3e);

% The maximum output voltage Vo3max
Vo3max=Dee*VA3e-VB3e;

% Combination f - Vo3min=Vo3(Io1min, Io2min, Io3max)

Io1=Io1min;
Io2=Io2min;
Io3=Io3max;

% Primary side
Ip=N1*Io1+N2*Io2+N3*Io3;
Vp=Vin-Ip*(Rpdc+Rds);
Dldp=Fs*Co*Vp/Ip;
Dn=Dn+Dldp;

% Vo1 secondary side
Vs1=N1*Vp;
Delt1=Ls1*Io1/Vs1;
VA1f=Vs1-(Io1*Rs1dc);
VB1f=Vd1+Io1*(Fs*Ls1+Rd1+Rl1);
```

```
% Vo2 secondary side
Vs2=N2*Vp;
Delt2=Ls2*Io2/Vs2;
VA2f=Vs2-(Io2*Rs2dc);
VB2f=Vd2+Io2*(Fs*Ls2+Rd2+Rl2);

% Vo3 secondary side
Vs3=N3*Vp;
Delt3=Ls3*Io3/Vs3;
VA3f=Vs3-(Io3*Rs3dc);
VB3f=Vd3+Io3*(Fs*Ls3+Rd3+Rl3);

% Effective duty cycle De
Def=(Vr+x(1)*VB1f+x(2)*VB2f+x(3)*VB3f)/(x(1)*VA1f+x(2)*VA2f+x(3)*VA3f);

% The minimum output voltage Vo3min
Vo3min=Def*VA3f-VB3f;

% Objective function
f=W1*((Vo1max-Vo1noms)^2+(Vo1min-Vo1noms)^2)+W2*((Vo2max-Vo2noms)^2+(Vo2min-
Vo2noms)^2)+W3*((Vo3max-Vo3noms)^2+(Vo3min-Vo3noms)^2);

% g(1) - Equality constraint constraints
g(1)=Vo1noms*x(1)+Vo2noms*x(2)+Vo3noms*x(3)-Vr;

% g(2) - g(7) -- inequality (g(i)<=0)
g(2)=Vo1mins-Vo1min;
g(3)=Vo1max-Vo1maxs;
g(4)=Vo2mins-Vo2min;
g(5)=Vo2max-Vo2maxs;
g(6)=Vo3mins-Vo3min;
g(7)=Vo3max-Vo3maxs;

% g(8) - g(10) -- guarantee the weighting factors =>0
g(8)=-x(1);
g(9)=-x(2);
g(10)=-x(3);
```

****

% triple_b.m -- calculate the output voltages for delta8.m after optimization

```
% The converter has three outputs, and each output is allowed
%  to change over a certain range.
% The results are plotted.

function triple_b(x)
```

```
% Define the global variable
global Fs Ts Dn Vinnom Vinmin Vinmax Vin Vr
global Vo1noms Vo1mins Vo1maxs Vo2noms Vo2mins Vo2maxs Vo3noms Vo3mins Vo3maxs
global Io1min Io1max Io2min Io2max Io3min Io3max DI1 DI2 DI3
global Rpdc Rds Co Np Ns1 Ns2 Ns3
global Vd1 Rd1 Rl1 Rs1dc Ls1 Vd2 Rd2 Rl2 Rs2dc Ls2 Vd3 Rd3 Rl3 Ls3 Rs3dc
global N1 N2 N3 N1auto N2auto N3auto
global NON_FEAS f NI

K1=x(1);
K2=x(2);
K3=x(3);

% There are 6 combinations of load currents to consider. Each combination represents an extreme
operation condition, which corresponds to either a minimum or maximum voltage.

% Combination a - Vo1max=Vo1(Io1min, Io2max, Io3max)

Io1=Io1min:DI1:Io1max;
Io2=Io2max;
Io3=Io3max;

% Primary side
Ip=N1*Io1+N2*Io2+N3*Io3;
Vp=Vin-Ip*(Rpdc+Rds);
Dldp=Fs*Co*Vp/Ip;
Dn=Dn+Dldp;

% Vo1 secondary side
Vs1=N1*Vp;
Delt1=Ls1*Io1./Vs1;
VA1a=Vs1-(Io1*Rs1dc);
VB1a=Vd1+Io1*(Fs*Ls1+Rd1+Rl1);

% Vo2 secondary side
Vs2=N2*Vp;
Delt2=Ls2*Io2./Vs2;
VA2a=Vs2-(Io2*Rs2dc);
VB2a=Vd2+Io2*(Fs*Ls2+Rd2+Rl2);

% Vo3 secondary side
Vs3=N3*Vp;
Delt3=Ls3*Io3./Vs3;
VA3a=Vs3-(Io3*Rs3dc);
VB3a=Vd3+Io3*(Fs*Ls3+Rd3+Rl3);

% Effective duty cycle De
Dea=(Vr+K1*VB1a+K2*VB2a+K3*VB3a)./(K1*VA1a+K2*VA2a+K3*VA3a);

% The maximum output voltage Vo1max
Vo1max=Dea.*VA1a-VB1a;
```

```
% Combination b - Vo1min=Vo1(Io1max, Io2min, Io3min)

Io1=Io1min:DI1:Io1max;
Io2=Io2min;
Io3=Io3min;

% Primary side
Ip=N1*Io1+N2*Io2+N3*Io3;
Vp=Vin-Ip*(Rpdc+Rds);
Dldp=Fs*Co*Vp/Ip;
Dn=Dn+Dldp;

% Vo1 secondary side
Vs1=N1*Vp;
Delt1=Ls1*Io1./Vs1;
VA1b=Vs1-(Io1*Rs1dc);
VB1b=Vd1+Io1*(Fs*Ls1+Rd1+Rl1);

% Vo2 secondary side
Vs2=N2*Vp;
Delt2=Ls2*Io2./Vs2;
VA2b=Vs2-(Io2*Rs2dc);
VB2b=Vd2+Io2*(Fs*Ls2+Rd2+Rl2);

% Vo3 secondary side
Vs3=N3*Vp;
Delt3=Ls3*Io3./Vs3;
VA3b=Vs3-(Io3*Rs3dc);
VB3b=Vd3+Io3*(Fs*Ls3+Rd3+Rl3);

% Effective duty cycle De
Deb=(Vr+K1*VB1b+K2*VB2b+K3*VB3b)./(K1*VA1b+K2*VA2b+K3*VA3b);

% The minimum output voltage Vo1min
Vo1min=Deb.*VA1b-VB1b;

% Combination c - Vo2max=Vo2(Io1max, Io2min, Io3max)

Io1=Io1max;
Io2=Io2min:DI2:Io2max;
Io3=Io3max;

% Primary side
Ip=N1*Io1+N2*Io2+N3*Io3;
Vp=Vin-Ip*(Rpdc+Rds);
Dldp=Fs*Co*Vp/Ip;
Dn=Dn+Dldp;

% Vo1 secondary side
Vs1=N1*Vp;
```

```
Delt1=Ls1*Io1./Vs1;
VA1c=Vs1-(Io1*Rs1dc);
VB1c=Vd1+Io1*(Fs*Ls1+Rd1+Rl1);

% Vo2 secondary side
Vs2=N2*Vp;
Delt2=Ls2*Io2./Vs2;
VA2c=Vs2-(Io2*Rs2dc);
VB2c=Vd2+Io2*(Fs*Ls2+Rd2+Rl2);

% Vo3 secondary side
Vs3=N3*Vp;
Delt3=Ls3*Io3./Vs3;
VA3c=Vs3-(Io3*Rs3dc);
VB3c=Vd3+Io3*(Fs*Ls3+Rd3+Rl3);

% Effective duty cycle De
Dec=(Vr+K1*VB1c+K2*VB2c+K3*VB3c)./(K1*VA1c+K2*VA2c+K3*VA3c);

% The maximum output voltage Vo2max
Vo2max=Dec.*VA2c-VB2c;

% Combination d - Vo2min=Vo2(Io1min, Io2max, Io3min)

Io1=Io1min;
Io2=Io2min:DI2:Io2max;
Io3=Io3min;

%  Primary side
Ip=N1*Io1+N2*Io2+N3*Io3;
Vp=Vin-Ip*(Rpdc+Rds);
Dldp=Fs*Co*Vp/Ip;
Dn=Dn+Dldp;

% Vo1 secondary side
Vs1=N1*Vp;
Delt1=Ls1*Io1./Vs1;
VA1d=Vs1-(Io1*Rs1dc);
VB1d=Vd1+Io1*(Fs*Ls1+Rd1+Rl1);

% Vo2 secondary side
Vs2=N2*Vp;
Delt2=Ls2*Io2./Vs2;
VA2d=Vs2-(Io2*Rs2dc);
VB2d=Vd2+Io2*(Fs*Ls2+Rd2+Rl2);

% Vo3 secondary side
Vs3=N3*Vp;
Delt3=Ls3*Io3./Vs3;
VA3d=Vs3-(Io3*Rs3dc);
VB3d=Vd3+Io3*(Fs*Ls3+Rd3+Rl3);
```

```
% Effective duty cycle De
Ded=(Vr+K1*VB1d+K2*VB2d+K3*VB3d)./(K1*VA1d+K2*VA2d+K3*VA3d);

% The minimum output voltage Vo2min
Vo2min=Ded.*VA2d-VB2d;

% Combination e - Vo3max=Vo3(Io1max, Io2max, Io3min)

Io1=Io1max;
Io2=Io2max;
Io3=Io3min:DI3:Io3max;

%  Primary side
Ip=N1*Io1+N2*Io2+N3*Io3;
Vp=Vin-Ip*(Rpdc+Rds);
Dldp=Fs*Co*Vp/Ip;
Dn=Dn+Dldp;

% Vo1 secondary side
Vs1=N1*Vp;
Delt1=Ls1*Io1./Vs1;
VA1e=Vs1-(Io1*Rs1dc);
VB1e=Vd1+Io1*(Fs*Ls1+Rd1+Rl1);

% Vo2 secondary side
Vs2=N2*Vp;
Delt2=Ls2*Io2./Vs2;
VA2e=Vs2-(Io2*Rs2dc);
VB2e=Vd2+Io2*(Fs*Ls2+Rd2+Rl2);

% Vo3 secondary side
Vs3=N3*Vp;
Delt3=Ls3*Io3./Vs3;
VA3e=Vs3-(Io3*Rs3dc);
VB3e=Vd3+Io3*(Fs*Ls3+Rd3+Rl3);

% Effective duty cycle De
Dee=(Vr+K1*VB1e+K2*VB2e+K3*VB3e)./(K1*VA1e+K2*VA2e+K3*VA3e);

% The maximum output voltage Vo3max
Vo3max=Dee.*VA3e-VB3e;

% Combination f - Vo3min=Vo3(Io1min, Io2min, Io3max)

Io1=Io1min;
Io2=Io2min;
Io3=Io3min:DI3:Io3max;

%  Primary side
Ip=N1*Io1+N2*Io2+N3*Io3;
```

```
Vp=Vin-Ip*(Rpdc+Rds);
Dldp=Fs*Co*Vp/Ip;
Dn=Dn+Dldp;

% Vo1 secondary side
Vs1=N1*Vp;
Delt1=Ls1*Io1./Vs1;
VA1f=Vs1-(Io1*Rs1dc);
VB1f=Vd1+Io1*(Fs*Ls1+Rd1+Rl1);

% Vo2 secondary side
Vs2=N2*Vp;
Delt2=Ls2*Io2./Vs2;
VA2f=Vs2-(Io2*Rs2dc);
VB2f=Vd2+Io2*(Fs*Ls2+Rd2+Rl2);

% Vo3 secondary side
Vs3=N3*Vp;
Delt3=Ls3*Io3./Vs3;
VA3f=Vs3-(Io3*Rs3dc);
VB3f=Vd3+Io3*(Fs*Ls3+Rd3+Rl3);

% Effective duty cycle De
Def=(Vr+K1*VB1f+K2*VB2f+K3*VB3f)./(K1*VA1f+K2*VA2f+K3*VA3f);

% The minimum output voltage Vo3min
Vo3min=Def.*VA3f-VB3f;

% Print output 1 to the file output1.dat
Io1=Io1min:DI1:Io1max;
%y=[Io1' Vo1min' Vo1max'];
%fid=fopen('output1.dat', 'w');
%fprintf(fid, 'Io1(A) Vo1min(V) Vo1max(V) \n')
%fprintf(fid, '%5.2f %9.4f %9.4f \n', y)
%fclose(fid)

% Plot output 1
figure(1);
subplot (3,1,1)
plot(Io1, Vo1min,'r-',Io1, Vo1max, 'g--')
title('Output 1')
xlabel('Io1(A)')
ylabel('Vo1(V)')
gtext('Io2min, Io3min')
gtext('Io2max, Io3max')

% Print output 2 to the file output2.dat
Io2=Io2min:DI2:Io2max;
%y=[Io2' Vo2min' Vo2max'];
%fid=fopen('output2.dat', 'w');
%fprintf(fid, 'Io2(A) Vo2min(V) Vo2max(V) \n')
```

```
%fprintf(fid, '%5.2f %9.4f %9.4f \n', y)
%fclose(fid)

% Plot output 2
Io2=Io2min:DI2:Io2max;
%figure(2);
subplot (3,1,2)
plot(Io2, Vo2min,'r-',Io2, Vo2max, 'g--')
title('Output 2')
xlabel('Io2(A)')
ylabel('Vo2(V)')
gtext('Io1min, Io3min')
gtext('Io1max, Io3max')

% Print output 3 to the file output3.dat
Io3=Io3min:DI3:Io3max;
%y=[Io3' Vo3min' Vo3max'];
%fid=fopen('output3.dat', 'w');
%fprintf(fid, 'Io3(A) Vo3min(V) Vo3max(V) \n')
%fprintf(fid, '%5.2f %9.4f %9.4f \n', y)
%fclose(fid)

% Plot output 3
Io3=Io3min:DI3:Io3max;
%figure(3);
subplot (3,1,3)
plot(Io3, Vo3min,'r-',Io3, Vo3max, 'g--')
title('Output 3')
xlabel('Io3(A)')
ylabel('Vo3(V)')
gtext('Io1min, Io2min')
gtext('Io1max, Io2max')

% Print output to the file output.dat
y=[Io1' Vo1min' Vo1max' Io2' Vo2min' Vo2max' Io3' Vo3min' Vo3max'];
fid=fopen('output.dat', 'w');
fprintf(fid, 'Io1(A) Vo1min(V) Vo1max(V) Io2(A) Vo2min(V) Vo2max(V) Io3(A) Vo3min(V)
Vo3max(V) \n')
fprintf(fid, '%5.2f %9.4f %9.4f %6.2f %9.4f %9.4f %6.2f %9.4f %9.4f \n', y)
fclose(fid)
```

Appendix B. PSpice Programs for Small-Signal Analysis

Two small-signal PSpice simulation programs are provided. Appendix B.1 is used to simulate the small-signal characteristics, including control-to-output (-feedback) transfer functions, open- and closed-loop audio susceptibilities, open- and closed-loop output impedances, open- and closed-loop output transimpedances, and loop gain for a dual-output forward converter with voltage-mode control only. Appendix B.2 has the same functions, but is used for the dual-output forward converter with current-mode control. The values of the circuit parameters, which are marked by "###" in the programs, are to be provided by the user.

The equations used in Appendix B.1 are derived in Chapter 4, and those in Appendix B.2 are derived in Chapter 5.

The programs can be used on evaluation version of PSpice on PCs.

Appendix B.1 Voltage-Mode Control

```
VMC.CIR
*THE PROGRAM PERFORMS SMALL SIGNAL ANALYSIS.
*BY DIFFERENT SETTINGS, LOOP GAIN, OUTPUT IMPEDANCE, AND AUDIO CAN BE
CALCULATED.

* PRIMARY SIDE
VG    1     0     AC    1     0; UNLESS CALCULATING AUDIO, OTHERWISE SET 0
VT1   1     2     DC    0
FP1   2     0     VTS1  ###
FP2   2     0     VTS2  ###

**********************************************************************

*5V OUTPUT POWER STAGE

ES1   11    0     1     0     ###
VTS1   11    12      DC     0

* GC1 AND EC1 ARE CONTROLLED BY EITHER V(108) (WHEN PERFORMING
*          CLOSED-LOOP ANALYSIS)
*   OR V(109) ( WHEN PERFORMING OPEN-LOOP ANALYSIS). GC1 HAS A GAIN
*         OF THE LOAD CURRENT, AND EC1 HAS A GAIN VinN1/D.
GC1    12     0      109    0     ###
EC1    13     12      109    0      ###

FD1    13     0      VS1          ###
ED1    14     0      13     0     ###
VS1    14     15      DC     0
L1     15    16     ###
RL1    16    17      ###
C1     17    18     ###
RC1    18     0      ###
R1     17     0     ###
```

```
*IPT1   0    17      AC     1      0 ; USED FOR Z1out(s) AND Z21(s)

**********************************************************************

*12V OUTPUT POWER STAGE

ES2    21     0      1      0      ###
VTS2   21     22      DC     0

* GC2 AND EC2 ARE CONTROLLED BY EITHER V(108) (WHEN PERFORMING
*          CLOSED-LOOP ANALYSIS)
*   OR V(109) ( WHEN PERFORMING OPEN-LOOP ANALYSIS). GC2 HAS A GAIN
*          OF THE LOAD CURRENT, AND EC2 HAS A GAIN VinN2/D.

GC2    22     0      109    0          ###
EC2    23     22      109    0      ###

FD2    23     0      VS2    ###
ED2    24     0      23     0      ###
VS2    24     25      DC     0
L2     25     26     ###
RL2    26     27      ###
C2     27     28     ###
RC2    28     0      ###
R2     27     0     ###
*IPT2   0    27      AC     1      0 ; USED FOR Z2out(s) AND Z12(s)

**********************************************************************

*COUPLED OUTPUT INDUCTOR
k12    L1     L2     ###

**********************************************************************

*FEEDBACK VOLTAGE
* u=3
EF1    101    102          17        0      ###; K1
EF2    102     0 27     0      ###; K2

*FEEDBACK NETWORK
RA1      101    104        ###
CA2    101    103    ###
RA3    103    104    ###
RA2    104    105    ###
CA1    105    107    ###
CA3    104    107    ###

*OP-AMP
RAI    104     0 1E10
RAO     106    107    1
EA     106     0    0      104     1E8
```

```
RAUX2 107       0       1E10

*DUTY CYCLE
*EDUTY  109    0     107    0     ### ;FOR Zin, Zout AND AUDIO
VDUTY  109    0     AC    ###     0 ;USED FOR LOOP GAIN
RAUX1  109    0     1

*CONTROL CARD
.AC    DEC    50     100     50E3
.PRINT  AC VDB(107) VP(107)
.PROBE
.END
```

Appendix B.2 Current-Mode Control

***CMC.cir - Dual-output forward converter withcurrent mode control.**

```
*POWER CHANNEL 1
ES1   1 0 160 0                ###
VT1   1 2 DC=0
L1    2 3                     ###
RL1   3 4 ###
RC1   4 5 ###
C1    5 0 ###
R1    4 0 ###

*POWER CHANNEL 2
ES2   11 0 160 0               ###
VT2   11 12 DC=0
L2    12 13                   ###
RL2   13 14 ###
RC2   14 15 ###
C2    15 0 ###
R2    14 0 ###

*COUPLING COEFFICIENT
k L1 L2                       ###

*CURRENT SENSING AND CONTROL
F1    0 110 VT1                ###
F2    0 110 VT2                ###
RI    110 0 ###    ; Sensing resistor

*TRANSFER FUNCTION OF THE SAMPLING GAIN
*CH=LH=LH2=TS/PI
GH1   0 120 110 0 1
```

```
RH   120 121 -1.57
CH   121 122                3.1831E-06
LH   122 0                  3.1831E-06
RCH  121 122 1E12
GH2  0 130 120 0 1
LH2  130 0                  3.1831E-06

*FEEDFORWARD FROM THE OUTPUTS
ER1  140 141 4 0            ###
ER2  141 0 14 0             ###
RER 140 0 1

*SUMMING FUNCTION
ESUM1 150 151 140 0 1
ESUM2  152 151 130 0 1
VC 152 0 AC 1
RSUM 150 0 1

*MULTIPLY BY MODULATION GAIN
EFM  160 0 150 0            ###
RFM  160 0 1

* SUMMING OF THE OUTPUT VOLTAGES
EWV1 170 171 4 0            ### ;K1
EWV2 171 0 14 0             ### : K2
RW 170 0 1

* COMPENSATOR
EC      190  0 170 0 1
RA1     190 192 ###
CA2     190 191 ###
RA3     191 192 ###
CA3     192 194 ###

*OP-AMP
RIA     192  0 1E10
EA       0 193 192 0 1E8
ROA     193 194 1
RAUX    194  0 1E10

.AC  dec  100  100  100000
.PRINT AC VDB(194) VP(194)
*.PRINT AC VDB(4) VP(4) VDB(14) VP(14)
.PROBE
.end
```

Appendix C. A New Model for Multiple-Winding Transformers

C.1 Introduction

When performing dc analysis and design in Chapter 2, the transformer leakage inductances are lumped on the secondaries. For the three-winding transformer with side-by-side winding structure, this model is adequate to characterize the leakage phenomenon. As for the four-winding transformer, which is used for the three-output converter, the model is over simplified since it only accounted for the leakage between the primary and each secondary. The leakage effects between each pair of secondary windings were not accounted for. For the applications where the leakage impedance, which is the product of the leakage inductance and switching frequency, is much smaller than the sum of the resistances of the rectifier diode and the output filter inductor in the same power channel, lumping the leakage inductances on the secondaries is a good approximation. By doing so, the analysis is simplified and at the same time the major leakage effects are accounted

for. However for the applications where the leakage impedances are comparable to the other parasitic resistances in the circuit, which usually occurs in high switching-frequency applications, a better model is needed.

This appendix presents a new model for multiple-winding transformer for the applications where precise modeling of leakage inductances is critical to the design. The new model takes into account of the geometry of the magnetic structure while providing a unified expression. Each parameter in the model has its physical meaning, and can be numerically determined for certain type of structures. The combinations of certain parameters can be analytically calculated and measured. Although the resulted model is difficult to use for analysis purpose, it can be used in conjunction with circuit simulators, such as PSpice or Saber, to provide more accurate simulation results.

C.2 Derivation of the New Transformer Model

Figure C.1 shows a three-winding transformer. Each winding carries a current with a voltage applied across its terminals. The interaction of the currents and voltages results in a magnetic field. The magnetic flux in the field can be decomposed into: (1) main flux, Φ_m, which links all the windings; (2) self-leakage inductances, Φ_1, Φ_2, and Φ_3, and each of them links each winding itself; and mutual leakage inductances, Φ_{12}, Φ_{13}, and Φ_{23}, and

each of them links two of the three windings as their subscripts denoted. The voltage across each winding can be expressed, in terms of the magnetic fluxes, as:

$$v_1 = N_1 \frac{d}{dt}(\Phi_m + \Phi_1 + \Phi_{12} + \Phi_{13}), \tag{C.1}$$

$$v_2 = N_2 \frac{d}{dt}(\Phi_m + \Phi_2 + \Phi_{12} + \Phi_{23}), \tag{C.2}$$

$$v_3 = N_3 \frac{d}{dt}(\Phi_m + \Phi_{13} + \Phi_{23} + \Phi_3), \tag{C.3}$$

where the magnetic fluxes are the functions of the excitation currents as expressed as following:

$$\Phi_1 = P_1 N_1 i_1, \tag{C.4}$$

$$\Phi_2 = P_2 N_2 i_2, \tag{C.5}$$

$$\Phi_3 = P_3 N_3 i_3, \tag{C.6}$$

$$\Phi_{12} = P_{12}(N_1 i_1 + N_2 i_2), \tag{C.7}$$

$$\Phi_{23} = P_{23}(N_2 i_2 + N_3 i_3), \tag{C.8}$$

$$\Phi_{13} = P_{13}(N_3 i_1 + N_1 i_1), \tag{C.9}$$

where P_i's and P_{ij}'s are the permeance of the magnetic paths of Φ_i and Φ_{ij}.

The main flux is confined inside the core and can be described:

$$\Phi_m = B A_c, \tag{C.10}$$

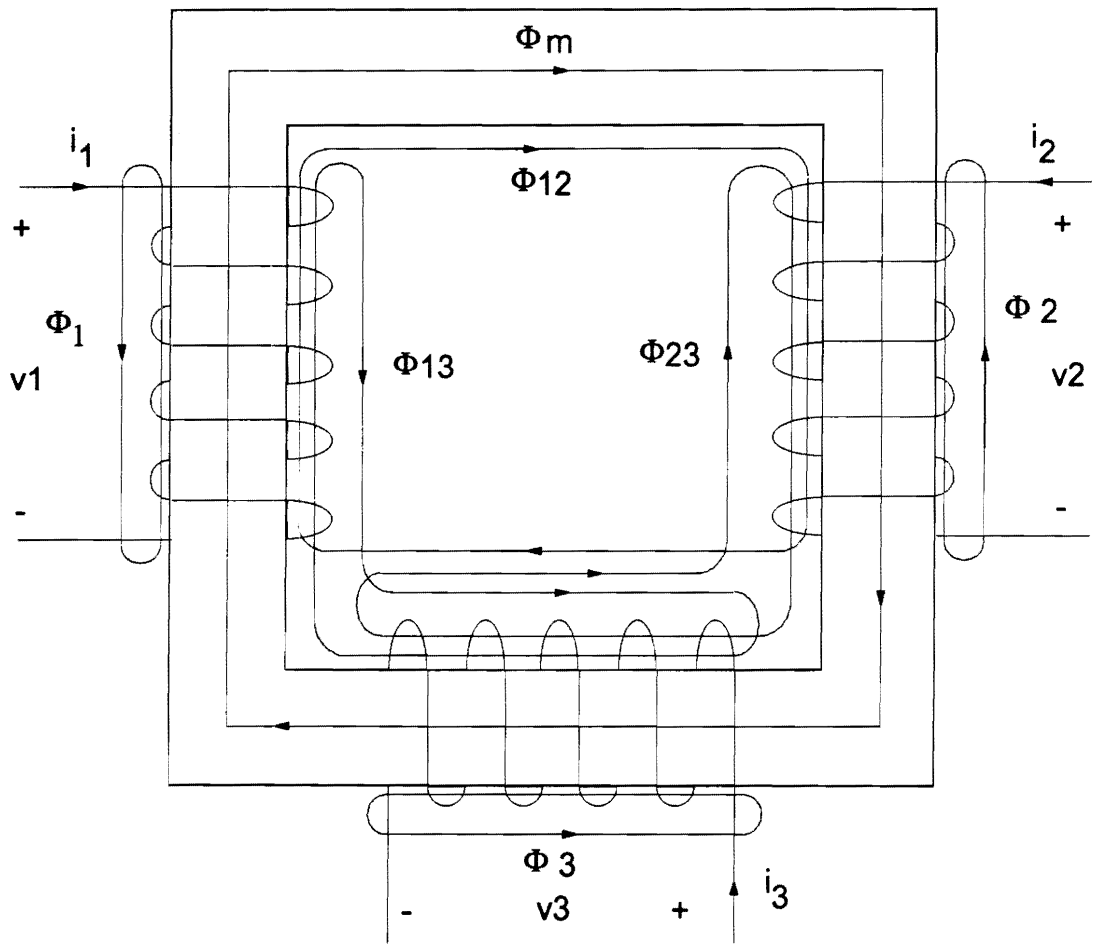


Fig. C.1. A three-winding transformer. The magnetic flux can be decomposed into the main flux, which links all the windings and is mainly confined inside the core, and leakage fluxes, which link only one or two of three windings.

$$Hl_m = N_1 i_1 + N_2 i_2, \tag{C.11}$$

$$B = \mu H, \tag{C.12}$$

then

$$\Phi_m = P_m (N_1 i_1 + N_2 i_2 + N_3 i_3), \tag{C.13}$$

where P_m is the permeance of the path of the main flux Φ_m.

The Eqs. (C.1) - (C.3) can be written in the form of:

$$v_1 = N_1 \frac{d}{dt}[P_m(N_1 i_1 + N_2 i_2 + N_3 i_3) + P_1 N_1 i_1 + P_{12}(N_1 i_1 + N_2 i_2) + P_{13}(N_1 i_1 + N_3 i_3)]$$

$$= N_1^2 (P_m + P_1 + P_{12} + P_{13}) \frac{di_1}{dt} + N_1 N_2 (P_m + P_{12}) \frac{di_2}{dt} + N_1 N_3 (P_m + P_{13}) \frac{di_3}{dt}, \tag{C.14}$$

$$v_2 = N_2 \frac{d}{dt}[P_m(N_1 i_1 + N_2 i_2 + N_3 i_3) + P_2 N_2 i_2 + P_{12}(N_1 i_1 + N_2 i_2) + P_{23}(N_2 i_2 + N_3 i_3)]$$

$$= N_1 N_2 (P_m + P_{12}) \frac{di_1}{dt} + N_1^2 (P_m + P_2 + P_{12} + P_{23}) \frac{di_2}{dt} + N_2 N_3 (P_m + P_{23}) \frac{di_3}{dt}, \tag{C.15}$$

$$v_3 = N_3 \frac{d}{dt}[P_m(N_1 i_1 + N_2 i_2 + N_3 i_3) + P_3 N_3 i_3 + P_{13}(N_1 i_1 + N_3 i_3) + P_{23}(N_2 i_2 + N_3 i_3)]$$

$$= N_1 N_3 (P_m + P_{13}) \frac{di_1}{dt} + N_2 N_3 (P_m + P_{23}) \frac{di_2}{dt} + N_3^2 (P_m + P_3 + P_{13} + P_{23}) \frac{di_3}{dt} \tag{C.16}$$

Referring all the voltages and currents to winding 1, *i.e.*,

$$v_2 = \frac{N_2}{N_1} v_{2-1}, \tag{C.17}$$

$$i_2 = \frac{N_1}{N_2} i_{2-1}, \tag{C.18}$$

$$v_3 = \frac{N_3}{N_1} v_{3-1}, \tag{C.19}$$

$$i_3 = \frac{N_1}{N_3} i_{3-1}, \tag{C.20}$$

and substituting the above relations into Eqs. (C.14) - (C.16) then the following expressions can be obtained:

$$v_1 = N_1^2(P_m + P_1 + P_{12} + P_{13})\frac{di_1}{dt} + N_1^2(P_m + P_{12})\frac{di_{2-1}}{dt} + N_1^2(P_m + P_{13})\frac{di_{3-1}}{dt}$$

$$= M_o^1\frac{di_1}{dt} + L_{l1}^1\frac{di_1}{dt} + L_{l12}^1\frac{di_1}{dt} + L_{l13}^1\frac{di_1}{dt} + M_o^1\frac{di_{2-1}}{dt} + L_{l12}^1\frac{di_{2-1}}{dt} + M_o^1\frac{di_{3-1}}{dt} + L_{l13}^1\frac{di_{3-1}}{dt}, \tag{C.21}$$

$$v_{2-1} = N_1^2(P_m + P_{12})\frac{di_1}{dt} + N_1^2(P_m + P_2 + P_{12} + P_{23})\frac{di_{2-1}}{dt} + N_1^2(P_m + P_{23})\frac{di_{3-1}}{dt}$$

$$= M_o^1\frac{di_1}{dt} + L_{l12}^1\frac{di_1}{dt} + M_o^1\frac{di_{2-1}}{dt} + L_{l2}^1\frac{di_{2-1}}{dt} + L_{l12}^1\frac{di_{2-1}}{dt} + L_{l23}^1\frac{di_{2-1}}{dt} + M_o^1\frac{di_{3-1}}{dt} + L_{l23}^1\frac{di_{3-1}}{dt}, \tag{C.22}$$

$$v_{3-1} = N_1^2(P_m + P_{13})\frac{di_1}{dt} + N_1^2(P_m + P_{23})\frac{di_{2-1}}{dt} + N_1^2(P_m + P_3 + P_{13} + P_{23})\frac{di_{3-1}}{dt}$$

$$= M_o^1\frac{di_1}{dt} + L_{l13}^1\frac{di_1}{dt} + M_o^1\frac{di_{2-1}}{dt} + L_{l23}^1\frac{di_{2-1}}{dt} + M_o^1\frac{di_{3-1}}{dt} + L_{l3}^1\frac{di_{3-1}}{dt} + L_{l13}^1\frac{di_{3-1}}{dt} + L_{l23}^1\frac{di_{3-1}}{dt}, \tag{C.23}$$

where L_{ij}^1 's are the leakage inductances referred to winding 1, which are defined :

$$L_{l1}^1 = N_1^2 P_1, \tag{C.24}$$

$$L_{l12}^1 = N_1^2 P_{12}, \tag{C.25}$$

$$L_{l13}^1 = N_1^2 P_{13}, \tag{C.26}$$

$$L_{l2}^1 = N_1^2 P_2, \tag{C.27}$$

$$L_{l23}^{1}=N_1^2 P_{23}, \tag{C.28}$$

$$L_{l3}^{1}=N_1^2 P_3, \tag{C.29}$$

v_{i-1} and i_{i-1} are the voltage and the current of i-th winding reflected to winding 1, and M_o^1 is the magnetizing inductance referred to winding 1, which is

$$M_o^1=N_1^2 P_m, \tag{C.30}$$

Using the mathematical expressions given in Eqs. (C.21) - (C.23), an equivalent circuit model can be constructed as shown in Fig. C.2(a). Placing ideal transformers between the interfaces of winding 1, windings 2 and 3 results in the final model, as shown in Fig. C.2(b).

In Fig. C.2, the leakage inductances associated with each winding is defined as:

$$L_{lij}^{k}=\frac{N_k^2}{N_1^2}L_{lij}^{1}. \tag{C.31}$$

The referred currents are

$$i_{i-j}=\frac{N_i}{N_j}i_i. \tag{C.32}$$

In the new model, the magnetizing inductance, M_o represents the main flux which links all the windings. The leakage inductances are represented by $L_{li}'s$ and $L_{lij}'s$. Each parameter in the model can be calculated for the winding with a regular structure, which happens to be true in most practical applications. In the following section, the calculation of the leakage inductances is demonstrated.

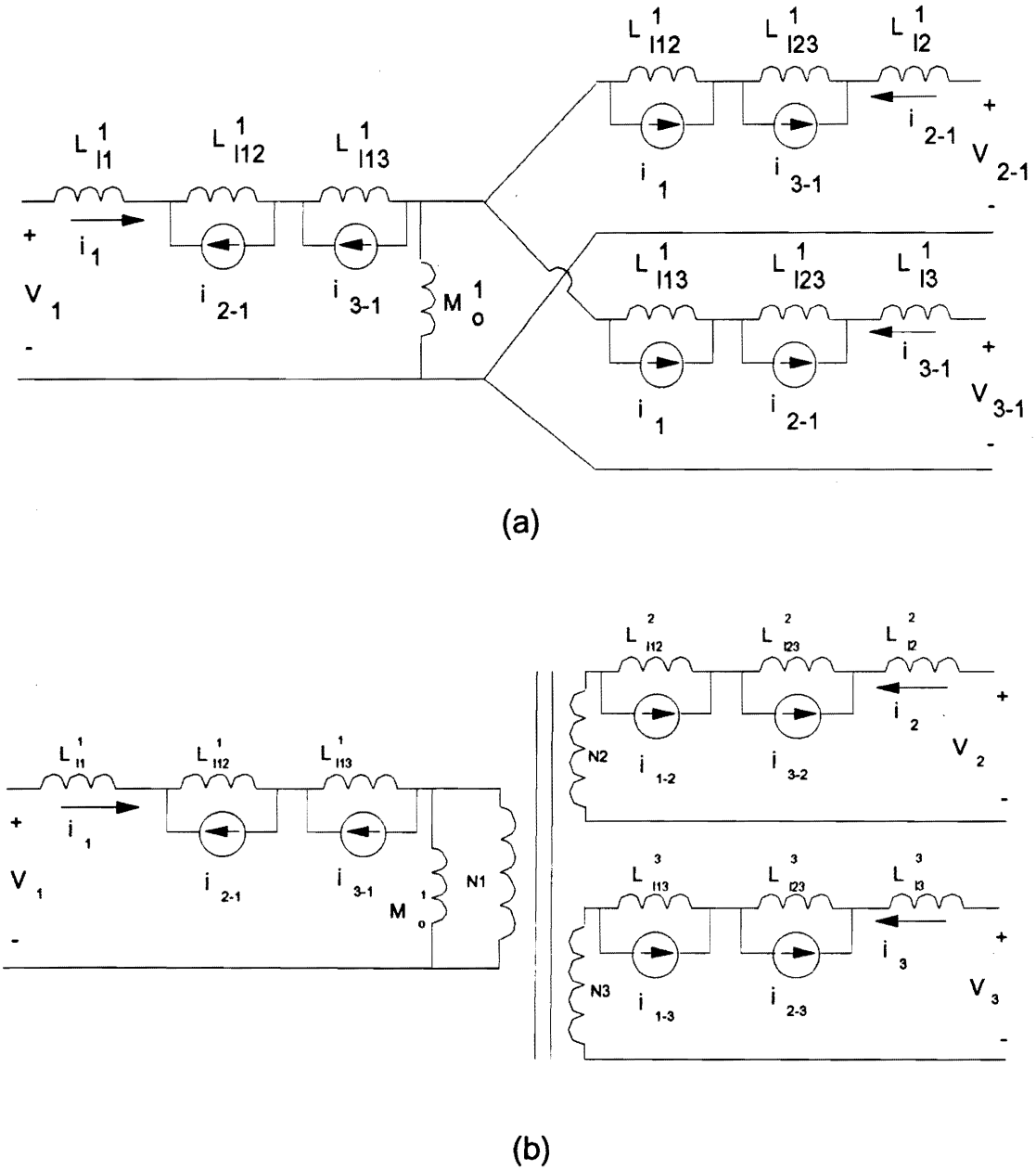


Fig. C.2. The derived transformer model. (a) All the voltages and currents are reflected to winding 1. (b) The final form of the transformer.

C.3 Calculation of the Parameters in the New Model

There is not a general way to calculate the values of the parameters in the new transformer model. The leakage inductances in the new transformer model must be decided according to the specific magnetic structure. When it comes to calculation of the parameters, the most important part involves the separation of the leakage flux which links different windings. Unfortunately, the separation of the leakage flux is extremely difficult if not impossible. In the following, a hybrid method of determining the leakage inductances is presented. The suggested method is based on numerical analysis which is performed using finite element method (Ansoft Maxwell Solver). The process is demonstrated through a three-winding transformer and a four-winding transformer both with side-by-side structure.

Figure C.3 shows the separation of the flux for the three-winding transformer. Qualitatively, the flux in windings 1, 2 and 3 can be viewed as the flux which only links itself, and the corresponding inductance is the self leakage inductance. The flux inside the gap between windings 1 and 2 can be viewed as the one which links windings 2 and 3, and the flux inside the gap between windings 2 and 3 can be viewed as the one which links windings 1 and 2. For this particular structure, any flux which links windings 1 and 3 must also link winding 2, which is part of the main flux according to the definition of the main flux. Therefore, there is no Φ_{13} in Fig. C.4. This separation gives a very rough picture

for flux distribution, which cannot serve the purpose of calculating leakage inductances. Actually, any attempt to separate the leakage flux rigorously is impossible. But with the help of this rough flux distribution, the values of leakage inductances can be determined numerically.

As well known, the voltages and currents of a multiple-winding transformer are related by the self- and mutual-inductances:

$$\begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix} = \begin{bmatrix} L_{11} & M_{12} & M_{13} \\ M_{21} & L_{22} & M_{23} \\ M_{31} & M_{32} & L_{33} \end{bmatrix} \frac{d}{dt} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix}. \tag{C.33}$$

Calculation of the leakage inductances starts from calculating the self- and mutual-inductances. Ansoft Maxwell solver can perform this calculation.

The self- and mutual-inductances are related to the magnetizing inductance and leakage inductances by following equations:

$$L_{11} = M_o^1 + L_{l1}^1 + L_{l12}^1 + L_{l13}^1, \tag{C.34}$$

$$L_{22} = \frac{N_2}{N_1}(M_o^1 + L_{l2}^1 + L_{l12}^1 + L_{l23}^1), \tag{C.35}$$

$$L_{33} = \frac{N_3^2}{N_1^2}(M_o^1 + L_{l3}^1 + L_{l13}^1 + L_{l23}^1), \tag{C.36}$$

$$M_{12} = M_{21} = \frac{N_2}{N_1}(M_o^1 + L_{l12}^1), \tag{C.37}$$

$$M_{13} = M_{31} = \frac{N_3}{N_1}(M_o^1 + L_{l13}^1), \tag{C.38}$$

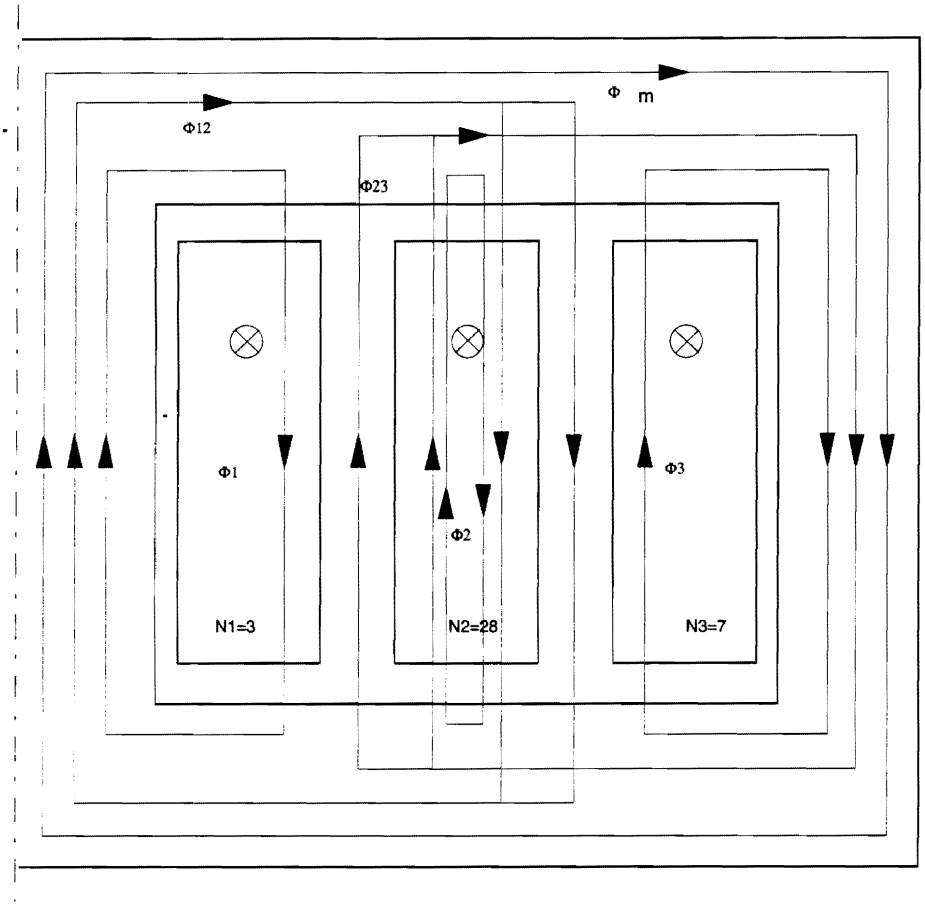


Fig. C.3. Magnetic flux diagram. *Conceptually, the magnetic flux can be decomposed into: (1) main flux, Φ_m; (2) self-leakage inductances, Φ_1, Φ_2, and Φ_3; and mutual leakage inductances, Φ_{12}, Φ_{13}, and Φ_{23}.*

$$M_{23} = M_{32} = \frac{N_2 N_3}{N_1^2}(M_o^1 + L_{l23}^1). \tag{C.39}$$

For the three-winding transformer discussed here:

$$L_{l13}=0, \tag{C.40}$$

then the magnetizing inductance and leakage inductances are

$$M_o^1 = \frac{N_3}{N_1} M_{31}, \tag{C.41}$$

$$L_{l1}^1 = L_{11} - \frac{N_1}{N_2} M_{12}, \tag{C.42}$$

$$L_{l3}^1 = \frac{N_1^2}{N_3^2} L_{33} - \frac{N_1^2}{N_2 N_3} M_{32}, \tag{C.43}$$

$$L_{l23}^1 = \frac{N_1}{N_2} M_{23} - \frac{N_1}{N_3} M_{13}, \tag{C.44}$$

$$L_{l12}^1 = \frac{N_1}{N_2} M_{12} - \frac{N_1}{N_3} M_{13}, \tag{C.45}$$

$$L_{l2}^1 = \frac{N_1}{N_2} L_{22} - \frac{N_1^2}{N_2 N_3} M_{23} - L_{l12}^1. \tag{C.46}$$

Now the inductance matrix (Table C.1) obtained from finite element simulation is used to calculate the magnetizing and leakage inductances, Table C.2.

Table C.1. Inductance Values Obtained from Finite Element Simulation.

$L_{11}(\mu H)$	$L_{22}(\mu H)$	$L_{33}(\mu H)$	$M_{12}(\mu H)$	$M_{13}(\mu H)$	$M_{23}(\mu H)$
20.1936697	1760.70586	110.154802	188.3968187	47.08423917	440.103511

Table C.2. Calculated Magnetic and Leakage Inductances.

$M_o{}^1(\mu H)$	$L_{l1}{}^1(nH)$	$L_{l2}{}^1(nH)$	$L_{l3}{}^1(nH)$	$L_{l12}{}^1(nH)$	$L_{l23}{}^1(nH)$
20.179	8.296	0	23.68	6.414	29.875

Generally speaking, the new transformer model has $n(n+1)/2$ leakage inductances, where n is the number of the windings. For a specific magnetic structure, however, the number of the parameters can be less. In the three-winding transformer with side-by-side arrangement, there are only five parameters instead of six. In this structure, winding 2 is sandwiched by windings 1 and 3, and therefore any flux which links winding 2 must link either winding1 or winding This means there is no L_{l2}. In addition, any flux which links windings 1 and 3, must also link winding 2. According to the definition of each flux component, this is the main flux. So there is no leakage flux which links windings 1 and 3, M_{l13}. The model of three-winding transformer with side-by-side structure is shown in Fig. C.4.

Since leakage inductances can only be accurately measured by performing short circuit test, it is impossible to measure the model parameters individually. Nonetheless, it is possible to measure certain combination of the leakage inductances. Table C.3 shows the measurement and calculation results.

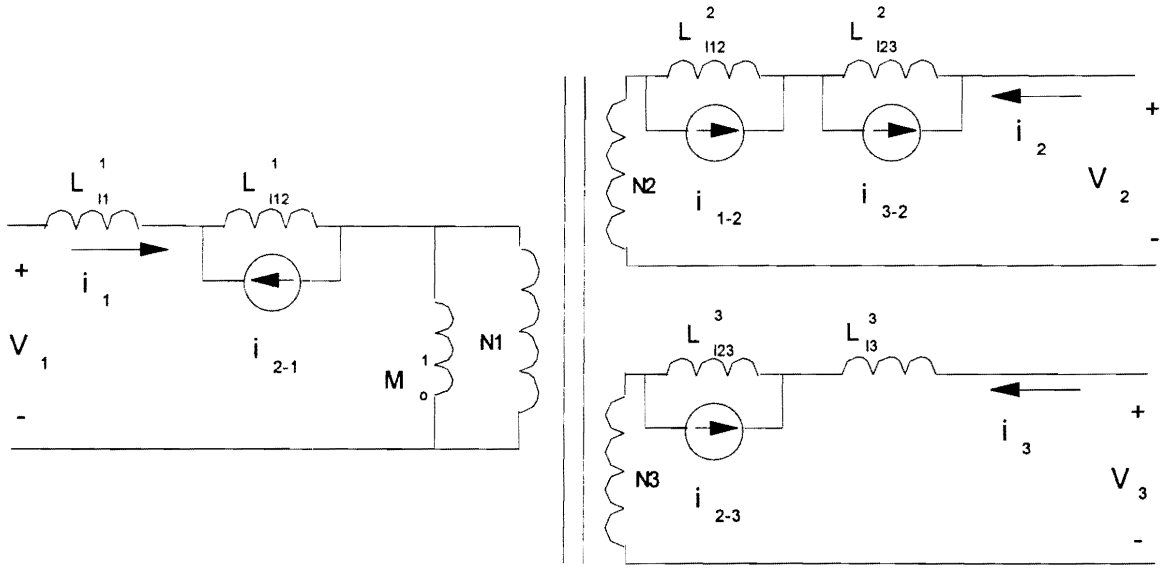


Fig. C.4. Three-winding transformer with side-by-side winding structure. *For this specific structure, some leakage inductance terms do not exist; therefore, the final model has fewer parameters than the general model does.*

Table C.3. Measurement and Calculation of the Combination of the Leakage Inductances.

	L_{1s2} (nH)	L_{1s3} (nH)	L_{2s3} (μH)
Calculation	38.171	68.265	3.161
Measurement	42.67	81.76	3.22

Note: L_{isj} stands for the inductance, either measured or calculated, at i winding with j winding shorted.

It can be seen that the calculated results are fairly close to the experimental results. The discrepancies are mainly due to the difference between the physical and modeled geometries, such as the terminations. Besides, the modeling tool is a 2-D solver, but the real problem is in nature a 3-D problem, which also accounted for the calculation errors.

Figure C.5 shows the geometrical structure of a four-winding transformer. The model for a four-winding transformer with side-by-side structure is shown in Fig. C.6. It can be seen that the real model takes much simpler form than the general model.

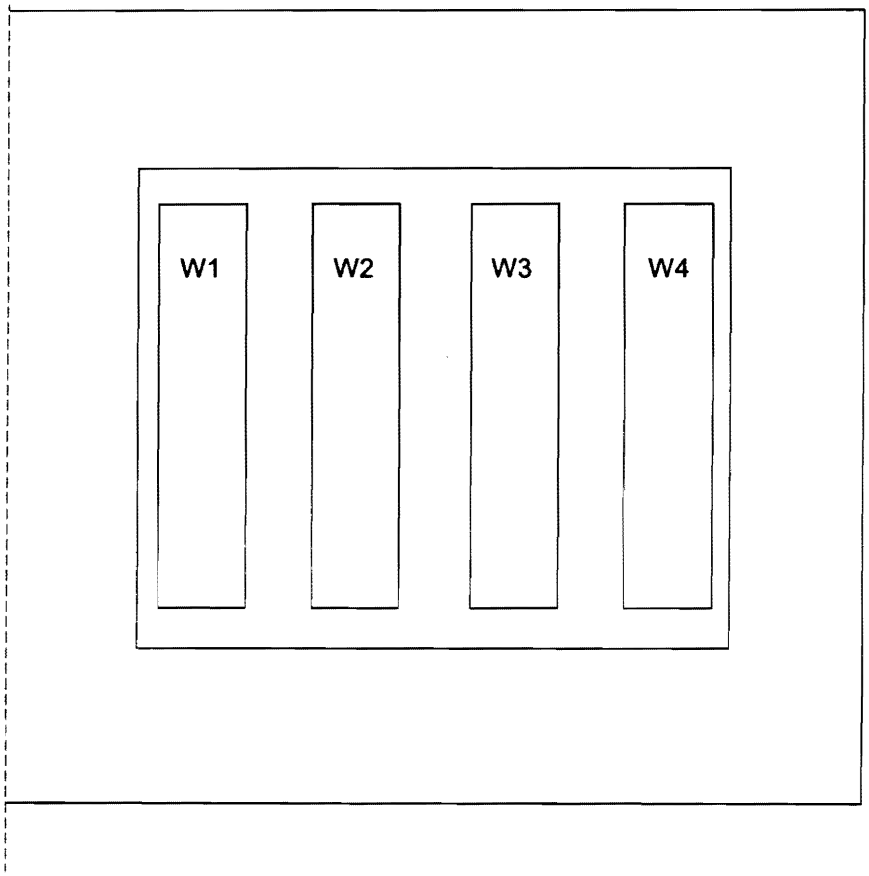


Fig. C.5. A four-winding transformer with side-by-side winding structure.

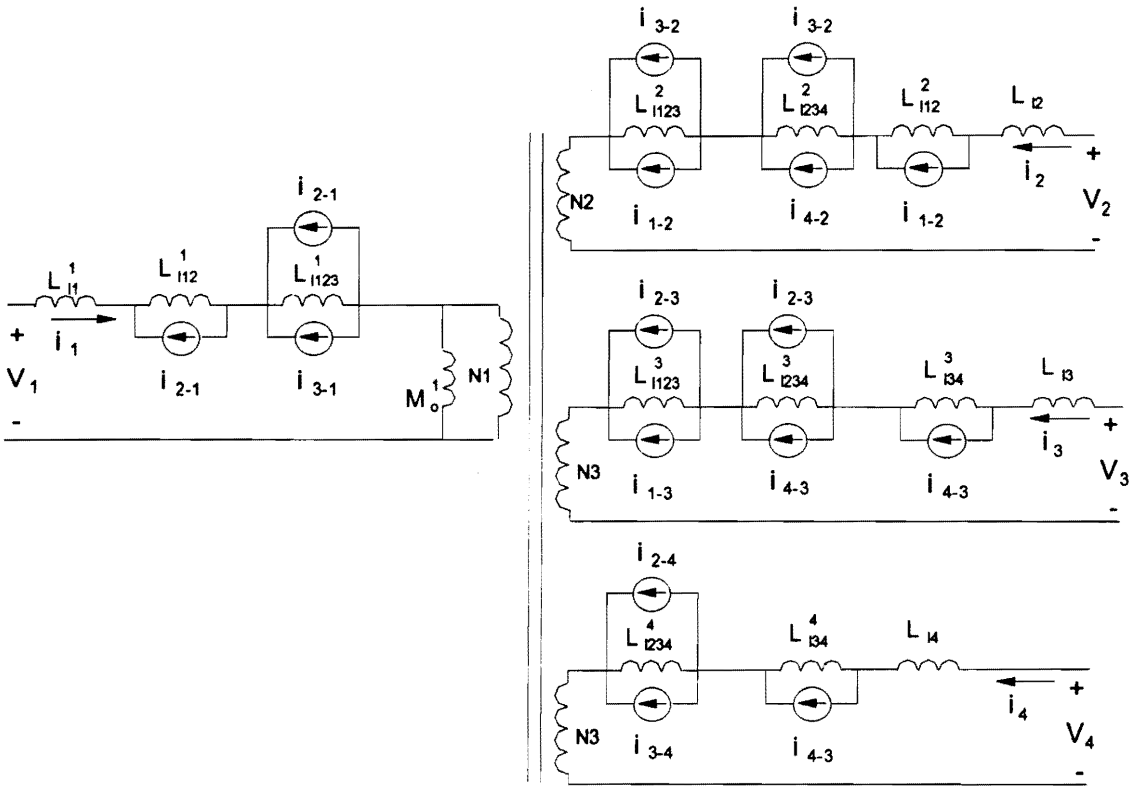


Fig. C.6. The final model for a four-winding transformer with side-by-side winding structure. *Due to the specific geometry, many components in the general model no longer exist. As a result, the model is simplified and more manageable.*

C.4 Conversion of the New Transformer Model into Other Form

The new transformer can be easily written in other forms. It is demonstrated here how to convert the 3-winding transformer model into a π–model which was originally presented in [H1], and the derivation was provided in [H8]. It can be seen that the π–model of the three-winding transformer is only a special case of the new model.

According to the new model, the port voltages for the transformer can be expressed:

$$v_1=(M_o^1+L_{l1}^1+L_{l12}^1+L_{l13}^1)\frac{di_1}{dt}+(M_o^1+L_{l12}^1)\frac{N_2\,di_2}{N_1\,dt}+(M_o^1+L_{l13}^1)\frac{N_3\,di_3}{N_1\,dt}, \tag{C.47}$$

$$v_2=(M_o^1+L_{l12}^1)\frac{N_2\,di_1}{N_1\,dt}+(M_o^1+L_{l2}^1+L_{l12}^1+L_{l23}^1)\frac{N_2^2\,di_2}{N_1^2\,dt}+(M_o^1+L_{l23}^1)\frac{N_2N_3\,di_3}{N_1^2\,dt}, \tag{C.48}$$

$$v_3=(M_o^1+L_{l13}^1)\frac{N_3\,di_1}{N_1\,dt}+(M_o^1+L_{l23}^1)\frac{N_2N_3\,di_2}{N_1^2\,dt}+(M_o^1+L_{l3}^1+L_{l13}^1+L_{l23}^1)\frac{N_3^2\,di_3}{N_1^2\,dt}. \tag{C.49}$$

As mentioned before, a three-winding transformer can be put into standard coupled-inductor form:

$$v_1=L_{11}\frac{di_1}{dt}+M_{12}\frac{di_2}{dt}+M_{13}\frac{di_3}{dt}, \tag{C.50}$$

$$v_2=M_{12}\frac{di_1}{dt}+L_{22}\frac{di_2}{dt}+M_{23}\frac{di_3}{dt}, \tag{C.51}$$

$$v_3=M_{13}\frac{di_1}{dt}+M_{23}\frac{di_2}{dt}+L_{33}\frac{di_3}{dt}, \tag{C.52}$$

where the self and mutual inductances can be expressed by the parameters in the model:

$$L_{11}=M_o^1+L_{l1}^1+L_{l12}^1+L_{l13}^1, \tag{C.53}$$

$$L_{22}=\frac{N_2^2}{N_1^2}(M_o^1+L_{l2}^1+L_{l12}^1+L_{l23}^1), \tag{C.54}$$

$$L_{33}=\frac{N_3^2}{N_1^2}(M_o^1+L_{l3}^1+L_{l13}^1+L_{l23}^1), \tag{C.55}$$

$$M_{12}=\frac{N_2}{N_1}(M_o^1+L_{l12}^1), \tag{C.56}$$

$$M_{13}=\frac{N_3}{N_1}(M_o^1+L_{l13}^1), \tag{C.57}$$

$$M_{23}=\frac{N_2N_3}{N_1^2}(M_o^1+L_{l23}^1), \tag{C.58}$$

Using these values, the parameters in the corresponding π-model can be calculated:

$$L_1=L_{11}-\frac{M_{12}M_{13}}{M_{23}}=(M_o^1+L_{l1}^1+L_{l12}^1+L_{l13}^1)-\frac{\frac{N_2}{N_1}(M_o^1+L_{l12}^1)\frac{N_3}{N_1}(M_o^1+L_{l13}^1)}{\frac{N_2N_3}{N_1^2}(M_o^1+L_{l23}^1)}$$

$$=\frac{M_o^1 L_{l1}^1+M_o^1 L_{l23}^1+L_{l1}^1 L_{l23}^1+L_{l12}^1 L_{l23}^1+L_{l13}^1 L_{l23}^1-L_{l12}^1 L_{l13}^1}{M_o^1+L_{l23}^1}\approx L_{l1}^1+L_{l23}^1, \qquad \text{(C.59)}$$

$$L_2=L_{22}-\frac{M_{12}M_{23}}{M_{13}}=\frac{N_2^2}{N_1^2}(M_o^1+L_{l1}^1+L_{l12}^1+L_{l13}^1)-\frac{\frac{N_2}{N_1}(M_o^1+L_{l12}^1)\frac{N_2N_3}{N_1^2}(M_o^1+L_{l23}^1)}{\frac{N_3}{N_1}(M_o^1+L_{l13}^1)}$$

$$=\frac{N_2^2}{N_1^2}\frac{M_o^1 L_{l2}^1+M_o^1 L_{l13}^1+L_{l2}^1 L_{l13}^1+L_{l12}^1 L_{l13}^1+L_{l23}^1 L_{l13}^1-L_{l12}^1 L_{l23}^1}{M_o^1+L_{l13}^1}\approx\frac{N_2^2}{N_1^2}(L_{l2}^1+L_{l13}^1), \quad \text{(C.60)}$$

$$L_3=L_{33}-\frac{M_{23}M_{13}}{M_{12}}=\frac{N_3^2}{N_1^2}(M_o^1+L_{l1}^1+L_{l12}^1+L_{l13}^1)-\frac{\frac{N_2N_3}{N_1^2}(M_o^1+L_{l23}^1)\frac{N_3}{N_1}(M_o^1+L_{l13}^1)}{\frac{N_2}{N_1}(M_o^1+L_{l12}^1)}$$

$$=\frac{N_3^2}{N_1^2}\frac{M_o^1 L_{l3}^1+M_o^1 L_{l12}^1+L_{l23}^1 L_{l12}^1+L_{l12}^1 L_{l13}^1+L_{l23}^1 L_{l12}^1-L_{l23}^1 L_{l13}^1}{M_o^1+L_{l12}^1}\approx\frac{N_3^2}{N_1^2}(L_{l3}^1+L_{l12}^1), \quad \text{(C.61)}$$

$$M=\frac{M_{12}M_{13}}{M_{23}}=\frac{\frac{N_2}{N_1}(M_o^1+L_{l12}^1)\frac{N_3}{N_1}(M_o^1+L_{l13}^1)}{\frac{N_2N_3}{N_1^2}(M_o^1+L_{l23}^1)}\approx M_o, \qquad \text{(C.62)}$$

$$A=\frac{M_{23}}{M_{13}}=\frac{\frac{N_2N_3}{N_1^2}(M_o^1+L_{l23}^1)}{\frac{N_3}{N_1}(M_o^1+L_{l13}^1)}\approx\frac{N_2}{N_1}, \qquad \text{(C.63)}$$

$$B=\frac{M_{23}}{M_{12}}=\frac{N_3}{N_1}\frac{\frac{N_2N_3}{N_1^2}(M_o^1+L_{l23}^1)}{\frac{N_2}{N_1}(M_o^1+L_{l12}^1)}\approx\frac{N_3}{N_1}. \tag{C.64}$$

The equivalent circuit is shown in Fig. C.7. Again if the windings are arranged in some regular way, each parameter can be estimated by either analytical or numerical calculation.

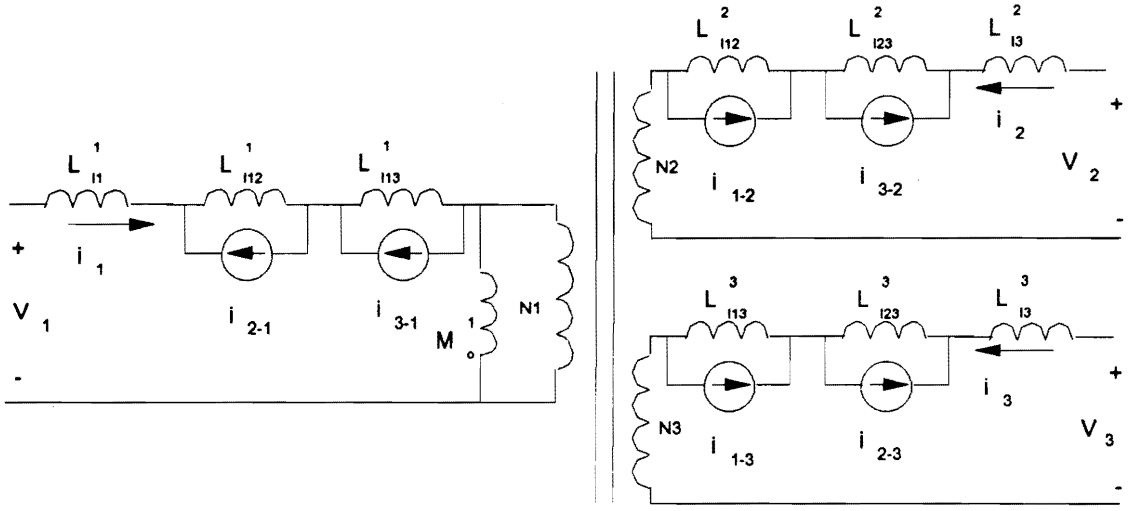
If a three-winding transformer structure has a specific magnetic structure, e.g., the windings are arranged side by side, the physical model presented in [H7] can be formulated, The following shows this physical model can also be obtained from the new transformer model. Substituting these parameters into Eqs. (C.59) - (C.61), the three leakage inductances are

$$L_1\approx L_{l1}^1+L_{l23}^1, \tag{C.65}$$

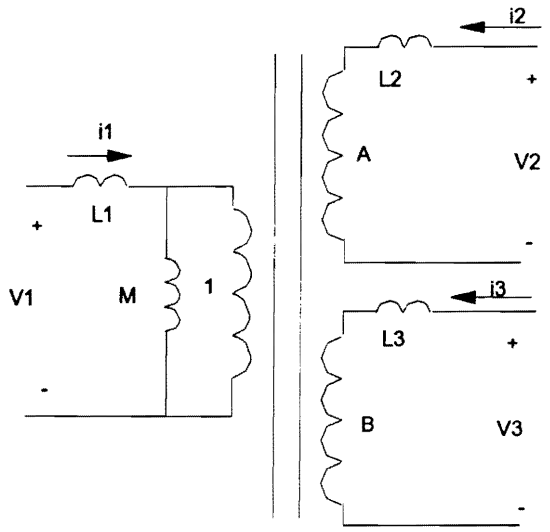
$$L_2\approx\frac{N_2^2}{N_1^2}(L_{l2}^1+L_{l13}^1)=0, \tag{C.66}$$

$$L_3\approx\frac{N_3^2}{N_1^2}(L_{l3}^1+L_{l12}^1). \tag{C.67}$$

Constructing a circuit model corresponding to (C.65) - (C.67), it is same as the one given in [H6].



(a)



(b)

Fig. C.7. Conversion of the new model to the π-model for a three-winding transformer. The π-model is actually a special case of the new model when the number of the windings is three.

C.5 Summary

A new model for multiple-winding transformers is presented. The model takes very general form regardless of geometry and magnetic property. The calculation of the model parameters has to be performed for specific magnetic structure with the help of numerical simulation tool -- finite element method. Each parameter in the model corresponds to a flux in the transformer. The calculated and measured results are fairly close, and the discrepancies are mainly due to the difference between the physical and modeled structures.

The problem related to the new model is that it is relatively complicated and difficult to use when performing analytical calculation. However, it can be useful for circuit simulation.

Vita

The author was born in Dalian, China. He received the B.S. and M.S. degrees in mechanical engineering from Shanghai Jiaotong University, in 1982 and 1984, respectively. he was then employed as an instructor in the mechanical engineering department at the same university from 1984 to 1987. In 1987, he joined Virginia Power Electronics Center (VPEC) of Virginia Polytechnic Institute and State University as a research assistant. He received the M.S.E.E. degree in 1991. His research interests include dc-dc converters, converter modeling and control, computer aided design, magnetics, hybrid and surface mount technology.