SOFT-SWITCHING TECHNIQUES FOR HIGH-POWER PWM CONVERTERS

by

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(ABSTRACT)

Soft-switching techniques can significantly reduce the switching loss and switching stresses of the power semiconductor devices in a power converter. This work presents several soft-switching topologies for high power PWM converters. These new topologies achieve soft-switching functions with minimum increase of device voltage/current stresses and converter circulating energy, and thus have advantages over conventional techniques in efficiency, power density, reliability, and cost of power converters.

The improved zero-current transition (ZCT) converters achieve zero-current switching at both turn-on and turn-off for all main switches and auxiliary switches. These converters significantly reduce the switching loss and stress of the power semiconductor devices, while have a voltage/current stress and circulating energy similar to a PWM converter's. The analysis, design, and experimental verification are presented.

The three-phase zero-voltage transition (ZVT) boost rectifiers/voltage source inverters are developed with simple auxiliary circuits. Unlike most existing three-phase soft-switching techniques, these new topologies achieve soft-switching functions without overcharging the resonant inductors, and realize the benefits of soft-switching operation with minimum extra main switch turn-offs and fixed auxiliary circuit control timing. The operation principles of the developed techniques are experimentally verified, and their efficiency performances are evaluated with experiments and computer simulation.

The three-phase ZVT buck rectifier topologies developed in this work achieves zero-voltage turn-on for all main switches with an optimum modulation schemes and simple auxiliary circuits. The auxiliary circuits, which are connected directly to each main switch, can also absorb the parasitic resonance of the bridge arms, and keep the voltage stress of the power devices at the minimum. The analysis and simulation results are presented to verify the converter operation.

New ZVT dc-link schemes for three-phase ac-dc-ac converters are investigated. With coordinated control of the ac-dc converter and the dc-ac converter, a set of simple auxiliary circuit can provide soft-switching function for all switches in both the ac-dc converter and the dc-ac converter. The power loss in the auxiliary circuit is also significantly lower than existing dc-link soft-switching schemes. Simulation with experimentally obtained device switching loss data proves that significant efficiency improvement can be achieved with the new ZVT dc-link techniques.

New ZVT and ZCT techniques for three-level converters are also developed. The auxiliary circuits are not in the main power path, and allow the converters to be controlled with optimum PWM schemes. Analysis and simulation results are presented to demonstrate the operation principles and advantages of soft switching in three-level converters.

To my wife and son

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TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

1 INTRODUCTION

1.1 BACKGROUND

Modern power supplies are required to provide high-quality power to their loads, and have a small physical size and weight. The switching frequency of a PWM power converter has profound effect on the converter power density and its electrical performances, because it practically determines the values of its reactive components, and limits the maximum bandwidth of the control loops (and thus the system dynamic performance). High-frequency operation of power converters is highly desired in many applications. However, the high-switching-frequency operation of a PWM converter is retarded by the high switching losses of power devices, and the high switching stresses caused by circuit parasitics (stray inductance, junction capacitance, etc.). The switching loss and stress problem is more pronounced in high power converters due to the poor switching characteristics and large physical size of high power semiconductor devices. Soft-switching techniques shape the switch voltage or current to zero before the switching action of power switches, thus avoiding the concurrent high voltage and high current in the switching transition. The benefits of soft switching can be summarized as:

- Low switching losses due to small overlap of the switch voltage and current;
- Low di/dt and dv/dt, and thus low voltage spike and EMI (electromagnetic interference) emissions;
- High reliability due to the favorable switching condition;
- Possible cost reduction due to the reduced voltage and current ratings of power semiconductor devices, and smaller values of reactive components.

Soft switching is an effective means to solve or alleviate switching losses and stress problems. Various soft-switching techniques have been developed in recent years, and are summarized in the following part of this section.

1.1.1 SOFT-SWITCHING TECHNIQUES IN DC-DC CONVERTERS

Soft-switching techniques in dc-dc converters have evolved from resonant converters (RC), quasi-resonant converters (QRC), multi-resonant converters (MRC), and soft-switched PWM converters to soft-transition PWM converters, including zero-voltage transition (ZVT) and zero-current transition (ZCT) techniques [A27]-[A37]. These soft-switching techniques can be classified into two categories: zero-voltage switching (ZVS), including ZVS RC, ZVS QRC, ZVS MRC and ZVT, and zero-current switching (ZCS), including ZCS RC, ZCS QRC, and ZCT. ZVS reduces or even eliminates the turn-on losses by shaping the switch voltage to zero prior to its turn-on, while ZCS reduces the turn-off loss by shaping the current of a switch to zero prior to its turn-off. RCs, QRCs and MRCs utilize reactive components, including parasitic elements in the practical circuit, to achieve soft-switching power conversion in a resonant fashion, and usually do not require extra active switches. On the other hand, ZVT and ZCT use additional auxiliary switches to control the resonance between the reactive components, and affect the converter operation only during the turn-on or turn-off switching transition. Although RCs, QRCs, and MRCs seem simple topologically, they suffer from high voltage/current stress and circulating energy compared to their PWM counterparts, and are used mainly in low power applications.

In medium to high power converters, ZVT and ZCT are more preferable than other soft switching schemes, because they achieve soft switching with minimum switch voltage/current stresses and minimum converter circulating energy, and incorporate the widely accepted PWM control. The switches used for high power applications are mainly minority carrier devices, such as IGBTs, MCTs and GTOs. The major switching loss in these devices is usually the switch turn-off loss, which can be reduced by zero-current turn-off. However, the turn-on loss (including diode reverse recovery loss) is also significant, especially in high voltage devices. An optimum soft-switching scheme for a specific converter can only be determined by the switch devices used. Generally, a

successful soft switching scheme for high power applications should have minimum voltage stress for all switches, significantly reduced turn-off loss, and very small diode reverse recovery. The soft switching of auxiliary switches is also desired in very-high-power applications. The ZVT topology in [A32] eliminates the switch turn-on loss and diode reverse recovery. However, both the main switch and the auxiliary switch are turned off with high current, which limits its application in high power applications. The topology presented in [A41] operates in a similar manner as the ZVT in [A32], has a capacitor snubber to reduce the auxiliary switch turn-off loss. Coupled inductors are adopted in [A33] [A34] to reduce the turn-off current of the auxiliary switch to the magnetizing current of the coupled inductor, which is much smaller than the main inductor current. However, the design of the coupled inductor is complex, and accurate and operating-condition-dependent control timing in the soft-switching transients is required to achieve zero-voltage turn-on. In all these ZVT topologies, the turn-off loss of the main switch is not tackled directly. Although snubber capacitors can be used to reduce switch turn-off loss, the effect of a snubber sized for high frequency operation is usually marginal for high power devices [A1] [A13]. The ZCT topology in [A35] reduces the main switch turn-off loss significantly, but does not reduce the turn-on loss and diode reverse recovery. In addition, it requires the auxiliary switch to be turned off with high current. Therefore, the existing ZCT technique is not suitable for high-power applications either.

1.1.2 SOFT-SWITCHING TECHNIQUES IN THREE-PHASE CONVERTERS

Three-phase PWM converters are the high-power topology most widely used in practice. According to power conversion requirements, three-phase converters are categorized as inverters (dc-ac converters), rectifiers (ac-dc converters) and cycloconverters (ac-ac converters). Cycloconverters are rarely used nowadays except in some extremely high power applications, and are not included in this work. Inverters are

widely used in motor drives, uninterruptible power supplies, and many other applications. Power factor correction (PFC) converters, i.e. rectifiers with active input current control, are replacing conventional diode or thyristor rectifiers in many applications due to the forthcoming stringent power quality regulation. Up to now, most research effort in the field of three-phase converters has been focused on inverters. However, high-switching-frequency operation is usually more important in PFC converters than in inverters, because PFC converters need to achieve high-quality current control with small reactive components, which are not important factors in most inverter applications. Soft-switching techniques, which are important to inverters in reducing current (torque) ripple and acoustic noise, and improving control performance through the use of high switching frequencies, are more critical in rectifier applications.

Three-phase voltage source converters, including voltage source inverters and boost rectifiers, are widely used nowadays. In unidirectional power flow and low power end applications, discontinuous current mode (DCM) single-switch PFC schemes are usually used [B1]-[B4]. The soft-switching techniques in dc-dc converter can be easily adopted in these rectifiers [B5]. Due to the DCM operation of the converters, the active switch has a very small turn-on loss, but is subject to high turn-off loss. [B6] incorporated the ZCT scheme in [A35] to reduce the switch turn-off loss, achieving high converter efficiency. [B7] proposes a method to combine three single-phase PFC converters into a three-phase boost rectifier, in which soft-switching techniques in dc-dc converters, such as ZVT and ZCT, can also be directly used. In higher power levels, full-bridge type topologies, which are used in inverters also, are usually used due to their better current quality and higher efficiency. Most soft switching techniques in bridge type converters are shared by both inverters and rectifiers, and can be classified into two categories: dc-link commutation schemes [B8]-[B23] and ac side commutation schemes [B24]-[B31]. The dc-link commutation schemes have an inductor or switch in the dc link to separate the bridge switches from the stiff dc-link voltage source, and incorporate a resonant circuit across the dc link to shape the voltage of all bridge switches to zero at the same

time. The resonant dc link (RDCL) converter proposed in [B9] operates similarly to the ZVS QRC techniques used in dc-dc converters. With a resonant inductor in the dc link, and resonant capacitors across all bridge switches, the dc-link voltage is made to resonate at high frequencies to create zero-voltage conditions regularly, and the bridge switches are switched only during the zero link voltage period. Discrete pulse modulation (DPM) schemes, such as Σ-Δ modulation, are used to synthesize the output voltages without hindering the soft-switching operation [B35]. One of major disadvantages of the RDCL technique is the high voltage stress of the main switches: each main switch is required to block up to 2.5 times the dc source voltage. In addition, the DPM control, which is more complex than the conventional PWM control, requires a dc-link resonant frequency 8~10 times higher than the switching frequency in a PWM converter for a comparable spectral performance [B34] [B37] [B38], which is usually impractical. The actively clamped version of RDCL reduces the switch voltage stress to around 1.5 times dc source voltage by a clamp circuit. However, a large amount of energy is circulated in the clamp circuit, and DPM control is still required. Some techniques are tried to provide PWM control to RDCL [B39]. However, the PWM range is severely limited, and the switching loss is increased significantly. Many other resonant link topologies are also proposed in recent years. Some are reviewed in [B34], and demonstrate no significant improvement over hard-switching converters.

Several other dc-link commutation topologies avoid the high voltage stress and DPM control by putting the resonant components out of the main power path, in order to enable PWM control. The parallel resonant dc link (PRDCL) [B13] reduces the voltage stress and circulating energy in RDCL by using a dc-link switch. The resonant circuit, paralleled across the inverter bridge, is actuated only when soft-switching action is required to create zero-voltage turn-on condition for the main bridge switches. However, the auxiliary circuit is complex: four additional switches, one in the dc link and three in the resonant circuit, are required in this topology. These auxiliary switches are turned off with high current, and one of them has a high voltage stress. Another PRDCL scheme in

[B14] simplifies the resonant circuit slightly by eliminating one auxiliary switch. The quasi-resonant dc link (QRDCL) converter in [B15] requires only two auxiliary switches, and one of the auxiliary switches is turned on and off with zero current. However, the control timing for the auxiliary circuit is complex and difficult to adjust for a wide load range. The ZVT and ZCT dc-link commutation techniques proposed first in [B16] adopt the ZVT and ZCT concepts to the dc link, and simplify the auxiliary switch control requirement. [B17] proposes to incorporate the control of the dc-link switch into the PWM scheme, so that the total switching losses can be minimized. The simple topology proposed in [B19] uses a snubber capacitor to reduce the auxiliary switch turn-off loss, but the dc-link switch turn-off loss and auxiliary circuit conduction loss are increased due to the overcharged and bi-directional resonant inductor current. Coupled-inductors are used in [B21] [B22] to reduce the auxiliary switch turn-off current. PWM control, usually with certain modifications to the conventional schemes [B17] [B41], is used in these soft-switching topologies, so the device voltage stress and converter circulating energy are comparable to their hard-switching PWM counterparts. One distinctive feature of these dc-link PWM soft-switching schemes is that fewer auxiliary switches than the main switches are required. However, the dc-link switch has to conduct the main inverter current, and is turned off with high current in every switching cycle; its conduction loss and switching loss are even much higher than a main switch's. As a result, the implementation of the auxiliary circuit is quite complex, and efficiency improvement of soft switching is curtailed significantly by the power loss of the dc-link switch. One exception is the ZVT boost rectifiers proposed in [B8], where the dc-link switch is changed into a diode, and thus has a much lower power loss. The dc-link diode also provides short-through protection for the main switches, and enhances the converter reliability. However, negative dc-link current is blocked by the dc-link diode, making bi-directional power flow impossible. These dc-link commutation schemes are attractive in relatively low power applications.

In higher power level, it is generally desired to place the auxiliary circuit out of the main power path to reduce its power loss. Then the soft-switching circuit can be put at the ac side of the main bridge. Each main switch can have a functionally independent auxiliary circuit to provide soft switching condition [B26] [B28]. Although the number of auxiliary switches in ac side commutation schemes is increased compared to the dc-link commutation schemes, each auxiliary switch has a much lower power loss and is turned off with zero or small current, and consequently has a simpler and lower-cost implementation. The auxiliary resonant commutated pole (ARCP) inverter [B26] [B27] achieves zero-voltage turn-on for all main switches without significant modification to the modulation schemes. A distinctive feature of ARCP is that the auxiliary switches block only half the dc-link voltage, and are turned off with zero current, therefore having a very low power loss. The ZVT topology in [B28] applies the ZVT technique in [A33] directly to each main switch in a configuration similar to the soft-switching scheme in [B22]. The conduction loss and turn-off loss of the auxiliary switches are smaller than those occurring with the basic ZVT topology proposed in [A32]. However, the switch turn-off loss in these two topologies is only indirectly tackled by snubber capacitors, which are not very effective in high-power, high-frequency operations. Besides, high snubber capacitance also causes high voltage/current distortion due to the "zero current clamp" effect, and reduces the dc-link voltage utilization due to the increased dwell time [E33] [E34]. It is realized that the turn-off loss of switches is a more severe problem than the turn-on loss in many high power applications, and a ZCS topology was proposed in [B43] to solve the switch turn-off loss and diode reverse recovery problems, but it has several shortcomings:

- Two auxiliary switches are placed in the dc link, and are turned off with high current, therefore causing high conduction loss and turn-off loss;
- A resonant inductor of considerable inductance is in series with each main switch, and therefore causes high power loss and excessively high voltage stress if zero-current switching is not achieved for any reason;

- The turn-offs of all switches are synchronized, which generally requires more switching action than is necessary with the optimum PWM strategy.

In medium power applications, one of the major drawbacks shared by the above ac-side commutation schemes is that six auxiliary switches are required, and their control timing changes with phase currents. As a result, the converter implementation and control are complex and not cost-effective. A three-phase ZVT topology is proposed in [B29] to simplify these topologies. If the turn-on instants of all main switches is synchronized, only one auxiliary switch is required to provide soft-switching function for all six main switches, so the topology becomes much simpler. This simplified ZVT topology is controlled with a modified SVM scheme [B42]. The drawback is that the total turn-off currents of the main switches are much increased, and the auxiliary switch has a high conduction loss. The so-called resonant snubber based soft-switching inverter (RS^3) [B30] [B31] achieves a similar performance but requires at least three auxiliary switches.

Compared with voltage source converters, the soft switching of current source converters (including current source inverters, buck and buck-boost rectifiers) has not been well studied. The resonant link approach [D1]-[D5] has serious drawbacks similar to those of RDCL in [B9] [B10]. Recently, several soft-switching topologies for PWM current source inverters/buck rectifiers were investigated in [D6]-[D10] [D13]. However, these topologies have the following shortcomings:

- The soft-switching circuits are connected to the dc-link, and cannot absorb the parasitic inductance energy in the bridge arms. This might be acceptable for very high power applications where GTOs are used as main switches. However, in lower power applications, each bridge arm is usually implemented as a uni-directional voltage device, such as IGBTs, MOSFETs or MCTs, and a diode in series, then the energy of the switch junction capacitance, plus snubber capacitance if any, is trapped by the diode, and the resonance between the junction capacitance and stray inductance in the bridge arms causes high voltage spike and power dissipation to the switch [D13].

- The soft-switching circuits usually have a resonant tank (a capacitor and an inductor), require complex control timing, and produce higher than minimum voltage/current stress. Especially, the switch voltage stress depends on the soft-switching timing in some of these topologies, making them difficult to use.

The ZVS single-stage buck rectifier in [D11] [D12] utilizes the same soft-switching technique as the ZVS full-bridge dc-dc converters, and provides zero-voltage turn-on for all main switches without additional components. However, twelve main switches are required, and the converter offers no cost and efficiency improvement over a conventional two-stage approach, i.e. a boost rectifier plus a full-bridge dc-dc converter, since all switches in the single-stage approach have to be designed according to both the peak voltage stress at high line and the peak current stress at low line. Besides, the conduction loss of the primary switches is increased due to the increased circulating current.

1.1.3 SOFT-SWITCHING TECHNIQUES IN MULTI-LEVEL CONVERTERS

The popularity of multi-level power conversion is ever-increasing in high-power applications, because it can reduce the switching loss of power switches and the current ripple of the bulk inductors, and enhance the voltage sharing of series switches. Various three-phase and dc-dc multi-level topologies are proposed in [C1]-[C6] [C16] [C17], and various control aspects are investigated in [C8] [C14]. Soft switching also plays a very important role in multi-level converters. [C17]-[C19] proposed several soft-switching topologies for multi-level dc-dc converters. A ZVT three-level three-phase boost rectifier is proposed in [B44]. However, the auxiliary switch in this topology needs to block full output voltage, which is twice the voltage requirement of the main switches. Also, all three phase currents are switched in every switching cycle, causing more than the optimum switch turn-off loss. [C20] introduces the ZVS concept similar to in [B23] into three-level inverters. However, two additional switches placed in the main power path

have high power loss. [C21] proposes a soft-switching topology similar to the ARCP, but the auxiliary switches are required to block higher voltage than the main switches. Besides, the switch turn-off loss is not directly tackled in these ZVS schemes.

1.1.4 CONTROL AND SMALL-SIGNAL MODELING OF THREE-PHASE CONVERTERS

In addition to power stage topology study, another important aspect of power converter is the control and modeling of power stage, which is related to this work, especially in the three-phase converters, but not directly covered in this dissertation. Most modeling techniques in dc-dc converters are based on the state-space averaging technique [E10], while a PWM switch model practically equivalent to the state-space averaging technique is proposed in [E11]. The effect of switch nonlinearities, such as storage modulation and switch saturation voltage, is also modeled in [E11] [E12]. The effect of the soft-switching (ZVT) operation is modeled using the circuit averaging technique, for dc-dc converters in [E13], and for three-phase ZVT boost rectifiers in [E14].

The modeling and control of three-phase converters are included in three categories: modulation, power stage modeling, and controller design. Various modulation schemes are presented in [E1]-[E6] [E37]. [E7]-[E9] compare the performances of some modulation schemes. [E15] introduces a method to model switches in three-phase converters as ideal transformers, and then apply the d-q transformation to each part of the converters. [E16] directly applies the d-q transformation to the system equations of three-phase converters, and derives the converter models in the d-q coordinates. [E17] [E29] introduce d-q coordinates modeling of three-phase buck rectifiers. Different control schemes are discussed in [E19] [E20] [E23]-[E31]. Most modeling techniques in three-phase converters are based on the d-q transformation, and the resulting d-q model of a three-phase converter consists of two coupled channels: d channel and q channel, each having a structure similar to a dc-dc converter. Due to the cross coupling of these two

channels, the control design of three-phase converters is more or less a trial-and-error process. [E38] proposes to model a three-phase converter at its "averaged" operating point, and the three-phase converter model developed shows the same dynamics as the d-channel in the d-q model, but has the simple structure of a dc-dc converter. Another control issue is the interaction of subsystems in a complex power converter system. The interaction of dc-dc converter systems has been studied in [E31] [E36], and its basic concept can be extended to three-phase power converters. The interaction analysis of the dc-link interface can directly adopt the dc-dc converter techniques in [E31]. However, the interaction analysis of the three-phase interface, such as between an EMI input filter and a three-phase PWM rectifier, is much more complex. This problem is addressed briefly in [E29] for buck rectifiers, and is analyzed in [E37] for general converters with a simple converter model. The effects of some power device nonlinearities on three-phase converters are discussed in [E34] [E35].

1.2 PRESENT WORK

The primary objective of this work is to study soft-switching schemes for different power converter topologies in high-power applications. Due to the difference in operation requirements and power semiconductor characteristics, no single soft-switching scheme is suitable for all applications. This dissertation proposes and verifies several new high-power soft-switching topologies for dc-dc and three-phase power converters. These topologies improve the existing soft-switching techniques in the following aspects:

(a). PWM control of the converter is still kept. At the same switching frequency, PWM control can achieve a better control performance than any other control schemes. With PWM control, the switch voltage/current stress and circulating energy in a soft-switching converter are also minimized.

(b). All auxiliary circuit components are not in the main power path, and have low power loss.

(c). The modification to optimum PWM schemes is minimized, and the resonant inductor overcharging is eliminated in three-phase converters, so the extra main switch turn-off and its related power losses are also minimized.

(d). The soft-switching functions are achieved with simple auxiliary circuit control timing. The control timing of the auxiliary circuit is fixed for all operating conditions, so extra current/voltage sensing is not required, and the soft-switching operation is more reliable.

Several new ZCT schemes are proposed to provide zero-current turn-on and turn-off for all switches, including the auxiliary switches, in a PWM converter, so the switching loss and stress of the switches can be significantly reduced. Experimental results prove that the switching loss and voltage spike of high power IGBT modules can be reduced by more than 80% with the improved ZCT technique. The proposed schemes are suitable for very high power applications, where the switching loss and stress need to be kept at minimum.

Several simplified ZVT schemes for three-phase PWM converters are proposed. The switch turn-on instants in three phases are synchronized by PWM schemes, so that the switches and diodes in a three-phase converter can be divided into a top group and a bottom group. The ZVT principle is then applied to each group of the switches and diodes, instead of to each switch/diode pair. As a result, the auxiliary circuit can be simplified, while still achieving soft turn-on for all main switches. Different implementations of the soft-switching circuits for three-phase boost rectifiers/voltage source inverters, buck rectifiers, and buck-boost rectifiers are investigated. The operation principle and efficiency improvement of the proposed ZVT soft-switching schemes are verified by experimental and simulation results.

New soft-switching dc-link scheme is also investigated for three-phase ac-dc-ac PWM converter systems. By coordinating the control of the ac-dc converter with the dc-ac converter, a simple dc-link auxiliary circuit can provide soft-switching function for all switches in both the rectifier and the inverter. The power loss of the auxiliary circuit is much lower than in other dc-link soft-switching schemes, which further increases the efficiency improvement and reduces the cost of the auxiliary circuit.

A new multi-level two-quadrant boost chopper structure is explored for superconductive magnetic energy storage (SMES) and motor drive applications, which demonstrates a significant performance improvement over a two-level chopper with the same power stage parameters on switching loss, current ripple, and voltage sharing. Soft-switching schemes for three-phase three-level PWM inverters are developed with the concept of ZVT and ZCT cells. Simplified ZVT topologies for three-phase three-level PWM rectifiers are also investigated with switch turn-on synchronized SVM schemes.

1.3 DISSERTATION OUTLINE

This dissertation is arranged as follows:

Chapter 2 describes improved zero-current transition techniques for high-power applications. With modified control timing and topologies, the proposed ZCT techniques achieve soft turn-on and turn-off for all switches without increasing the switch voltage stress and hindering PWM control. An MCT converter and an IGBT test circuit are tested, and demonstrate a significant switching loss and switching stress reduction, and efficiency improvement.

Chapter 3 investigates simplified zero-voltage transition circuits for three-phase voltage source inverters and boost rectifiers. Space vector modulation schemes are arranged to synchronize the active switch turn-on in each switching cycle, so that simple auxiliary circuits can be used to provide soft-switching turn-on for all main switches. Experimental results verify the operation principle of the ZVT schemes, and demonstrate significant efficiency improvement. Two test configurations are simulated to evaluate the performance of the proposed ZVT circuits and compare the efficiencies of different hard-switching and soft-switching topologies under the same operating conditions. One is for 230 V ac, 450 V dc applications, and the other for 460 V ac, 900 V dc applications. Simple power loss models for the main power devices with experimentally obtained switching loss data are used in the switching model simulation. 1~2% efficiency improvement over the hard-switching operation is obtained in the simulation for the proposed ZVT schemes, which means around 30% converter power loss reduction, and possibly considerable cost reduction with a proper design.

Chapter 4 presents several three-phase ZVT buck and buck-boost rectifiers. Similarly to in the ZVT VSI and boost rectifiers, the switch turn-on instants are synchronized in the three phases through the current SVM scheme, so only two auxiliary switches are required to achieve zero-voltage turn-on for all six main switches. The

operation and efficiency improvement of the soft-switching techniques are verified with simulation.

Chapter 5 investigates new soft-switching schemes for three-phase ac-dc-ac PWM power conversion systems. The soft-switching mechanism is applied to the dc link, which is common to the ac-dc converter (the rectifier) and the dc-ac converter (the inverter), so that a set of auxiliary circuit can be used to provide soft-switching functions to all switches. The power loss of the auxiliary circuit is also much lower than with other existing dc-link soft-switching schemes.

Chapter 6 presents novel techniques of multi-level power conversion. A new multi-level structure for two-quadrant boost choppers is proposed, and its PWM control scheme and small-signal model are developed. ZVT and ZCT techniques for the two-quadrant choppers are also discussed. PWM cells for three-phase three-level inverters are identified with careful examination of SVM schemes, and ZCT cell and ZVT cell concepts are used to derive soft-switching topologies for three-level inverters. Similarly to the technique used in Chapter 3, SVM schemes are arranged to synchronize switch turn-on in three-phase three-level boost rectifiers, and simple auxiliary circuits are developed to provide zero-voltage turn-on for main switches.

Conclusions of this work and suggestions for future work are given in Chapter 7.

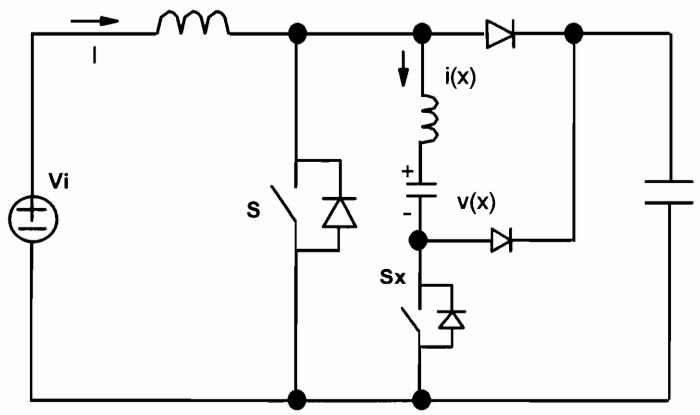
2 IMPROVED ZERO-CURRENT TRANSITION CONVERTERS FOR HIGH-POWER APPLICATIONS

2.1 INTRODUCTION

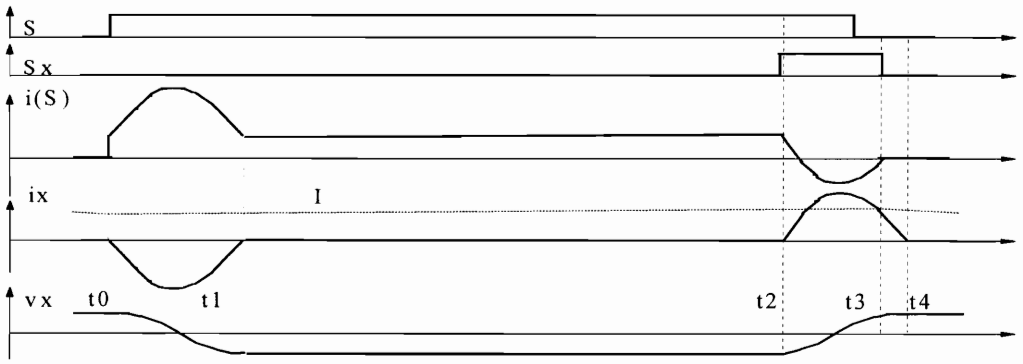
Power semiconductor switches in high power applications are subject to high switching stresses and switching losses. To alleviate these problems, significant derating of device voltage and current ratings and elaborate passive snubbers are usually used, and the switching frequency is limited to low-frequency ranges. Generally, a snubber circuit reduces the switching loss and switching stresses of the switches, but increases the total power loss in the converter. In recent years, various soft-switching techniques have been proposed to alleviate the switching loss and stress problems without resorting to bulky and lossy passive snubbers. The effects of soft switching on power devices are investigated in [A16]-[A25], which indicate significant performance improvements as well as cost, size, and weight reduction. A successful soft-switching scheme for high-power applications should reduce the switching losses, diode reverse recovery, and switching stress for all main and auxiliary switches without increasing the device voltage rating, because the device voltage margin is usually small, and the thermal management is very difficult. Most resonant converters, quasi-resonant converters, and multi-resonant converters are not suitable for high power applications due to the much increased voltage and current stresses. The recently developed zero-voltage transition (ZVT) [A32]-[A34], [A41] and zero-current transition (ZCT) [A35] PWM techniques incorporate the soft-switching functions into PWM converters, so that the switching losses can be reduced with minimum voltage/current stresses and circulating energy. The ZCT technique significantly reduces the switch turn-off loss by forcing the switch current to zero prior to its turn-off. A ZCT boost converter proposed in [A35] is shown in Fig. 2.1(a), where the

auxiliary circuit is shown within the dotted frame. The key waveforms of the circuit operation are shown in Fig. 2.1(b). As can be seen from Fig. 2.1(b), the current of the main switch is reduced to zero prior to its turn-off, so the switch turn-off loss is significantly reduced. However, the turn-on of the main switch is not affected by the auxiliary circuit, and severe diode reverse recovery causes high turn-on loss in the main switch. Moreover, the auxiliary switch turn-off current (at the moment t_3) is the same as the inductor current I, i.e. the same as the main switch turn-off current in the hard-switched converter. Therefore, this scheme can achieve efficiency improvement only if Sx has a much lower turn-off loss than S (such as in the low-power and low-voltage applications, where MOSFETs with low turn-off loss can be used to implement the auxiliary switch). Additionally, power switch devices used in high-power applications, usually IGBTs, MCTs, and GTOs, have limited turn-off capability, so the auxiliary switch would often be of a similar size and cost as the main switch to turn off the required current. This ZCT scheme is not suitable for high-power applications. The current commutation techniques for SCR converters [A38] [A39] are not suitable for gate turn-off devices either, because they do not solve the diode reverse recovery problem, have high power loss in the auxiliary circuit, and some of them increase switch voltage stress or require switches to block negative voltage.

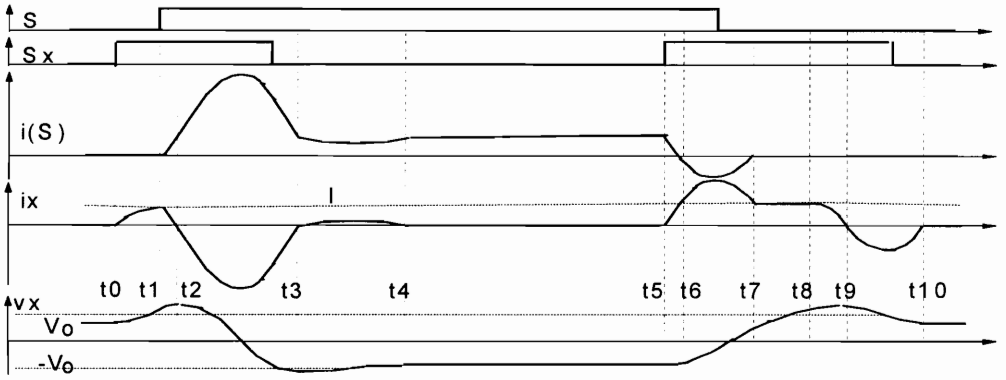
In this chapter, several new ZCT schemes are proposed to improve the ZCT technique in discussed in [A35]. With modified control and topology, all the main switches and the auxiliary switches are switched on and off under the zero-current condition, so the switching losses and stresses are reduced significantly. The zero-current switching of the auxiliary switches also allows the use of low-power rating device and low-conduction-loss devices, such as MCTs and IGBTs, in the auxiliary circuit. The soft switching schemes are discussed with the boost converter as an example, and are extended to other topologies through the concept of soft-switched PWM cells, since all PWM converters can be viewed as special connections of PWM cells.



(a) Topology proposed in [A35].



(b) Operational waveforms proposed in [A35].



(c) Waveforms with Proposed Modified Control.

Figure 2.1 **Existing ZCT PWM boost converter.** The main switch turn-on and auxiliary switch turn-off are in hard switching in (b). With a modified control, all switches can be switched under zero current, as shown in (c). However, the resonant current peak is much increased.

2.2 IMPROVED ZERO-CURRENT-TRANSITION BOOST CONVERTER

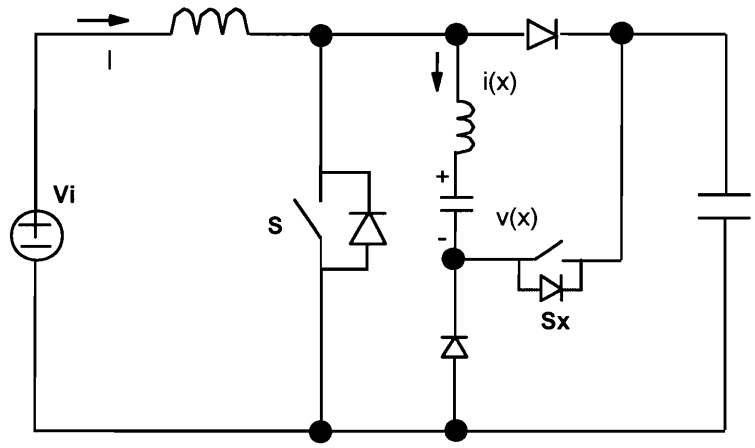
Up to now, all soft-switching PWM techniques reduce either the turn-on loss, or the turn-off loss of switches. ZVT techniques reduce or even eliminate the switch turn-on loss, and are attractive for devices with dominating turn-on loss, such as power MOSFETs. ZCT techniques reduce switch turn-off loss, and are more suitable for devices with dominating turn-off loss, such as GTOs. However, for the most widely used IGBTs, the distribution of the switching losses between turn-on and turn-off is device-dependent. Generally, turn-off loss is the dominating switching loss for low-voltage IGBTs. For high-voltage IGBTs, the switching loss distribution is more complex, and the turn-on loss is also significant due to the severe diode reverse recovery. Therefore, it would be of a great merit to develop a soft-switching scheme which could reduce both turn-on and turn-off losses, and thus could be effectively applied to different devices. This is especially important for very high power applications, where switching stress and loss are particularly annoying. The control of the ZCT topology shown in Fig. 2.1(a) can be modified to achieve this goal. The main switch turn-on current can be reduced to zero by the ZCT circuit, if the auxiliary switch is turned on before the main switch. Also, with a longer conduction time, the auxiliary switch current can be reduced to zero due to the resonance between Lx and Cx, so the auxiliary switch can be turned off under the zero-current condition also. Fig. 2.1(c) shows the key waveforms with this modified control. As can been seen, both the main switch and the auxiliary switch are turned on and off with zero current, so the switching losses of both switches can be reduced significantly. However, the current peak in the auxiliary circuit is very high, and causes high power loss. The current peak can be reduced by modifying the auxiliary circuit. The proposed new ZCT scheme is shown in Fig. 2.2(a). The modified auxiliary circuit, shown within the dotted frame, consists of resonant inductor Lx, resonant capacitor Cx, auxiliary switch Sx together with its anti-parallel diode Dx, and clamp diode Dc. This topology is similar to the one shown in Fig. 2.1(a), with a major difference only in the arrangement of the

auxiliary switch and clamp diode. However, as will be made clear later, the auxiliary circuit current peak of this topology is reduced, and the timing of the auxiliary switch is also much easier.

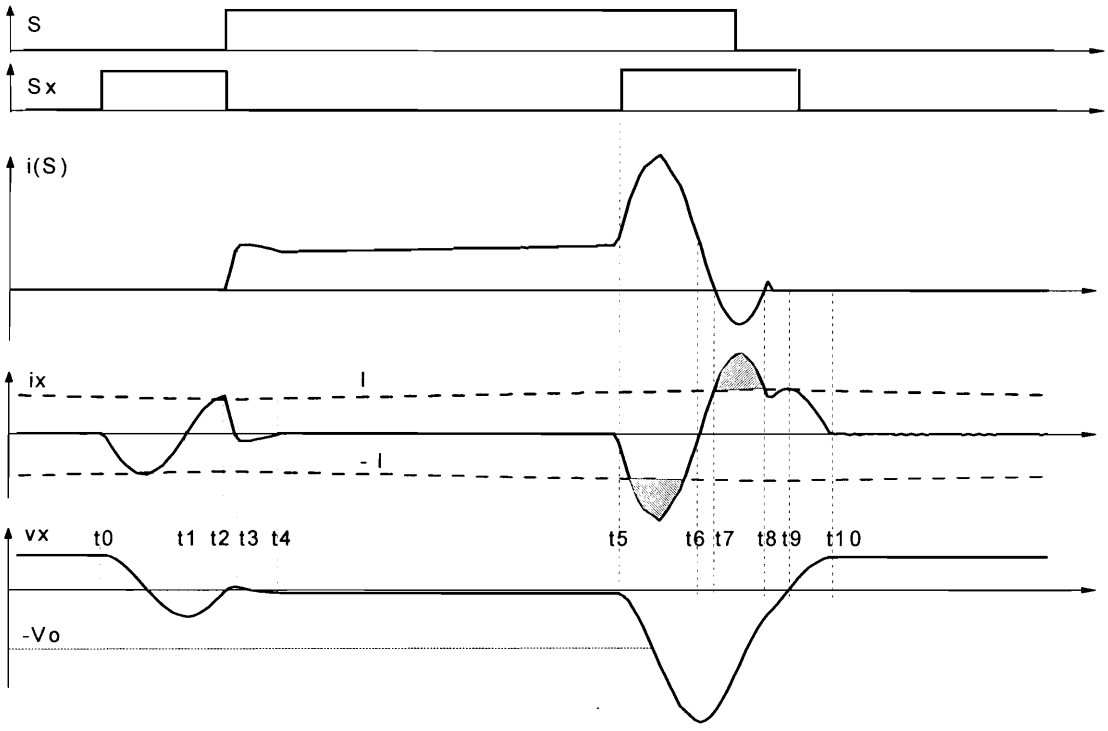
The operation of this converter is similar to its PWM counterpart's. The only difference is in the switch turn-on and turn-off transients, during which the auxiliary circuit is actuated to provide soft-switching conditions for the main switch S. The simulated waveforms during one switching period are shown in Fig. 2.2(b). During one switching period, the circuit goes through nine different stages, which are listed as (a) through (i) below, corresponding to the subtopologies in Fig. 2.3. The circuit parasitics, such as semiconductor junction capacitance and stray inductance, are included in the simulation but ignored in the following description. The operation description starts with switch turn-on transition. Before the main switch's turn-on, the inductor current I is conducted by the main diode, the auxiliary current i_x is zero, and v_x is a constant positive value. In the whole commutation process, the output voltage Vo and inductor current I are assumed to be constant, due to the large capacitance and inductance involved.

(a) Turn-On Transition I [t0, t2] At t0, Sx is turned on, starting the turn-on transition. The auxiliary resonant tank, consisting of Lx and Cx, begins to resonate. The auxiliary current ix resonates from zero to peak, and then decreases towards zero. When ix reaches zero at t1, the auxiliary circuit continues resonating, since the resonant capacitor voltage v_x is negative. Then, ix reverses its direction, and is conducted by Dx, the parallel diode of Sx. Afer this, Sx can be turned off under a zero-current and zero-voltage condition, with a much reduced power loss. As ix increases in positive value, the current of the main diode is diverted into the auxiliary circuit.

(b) Turn-On Transition II [t2, t3] When ix reaches its positive peak at t2, the current in the main diode is reduced to zero. Then S is turned on under the zero-current condition at t2. The turn-on loss is reduced significantly, since the diode reverse recovery is basically eliminated, and the current rise rate of the switch after turn-on is limited by



(a) Topology.



(b) Operational waveforms.

Figure 2.2 **An improved ZCT PWM converter**. The auxiliary switch and auxiliary diode interchange their positions in Fig. 2.1(a). All switches are switched with zero current at both switch turn-on and turn-off, and the resonant current peak is lower than in Fig. 3.1(c).

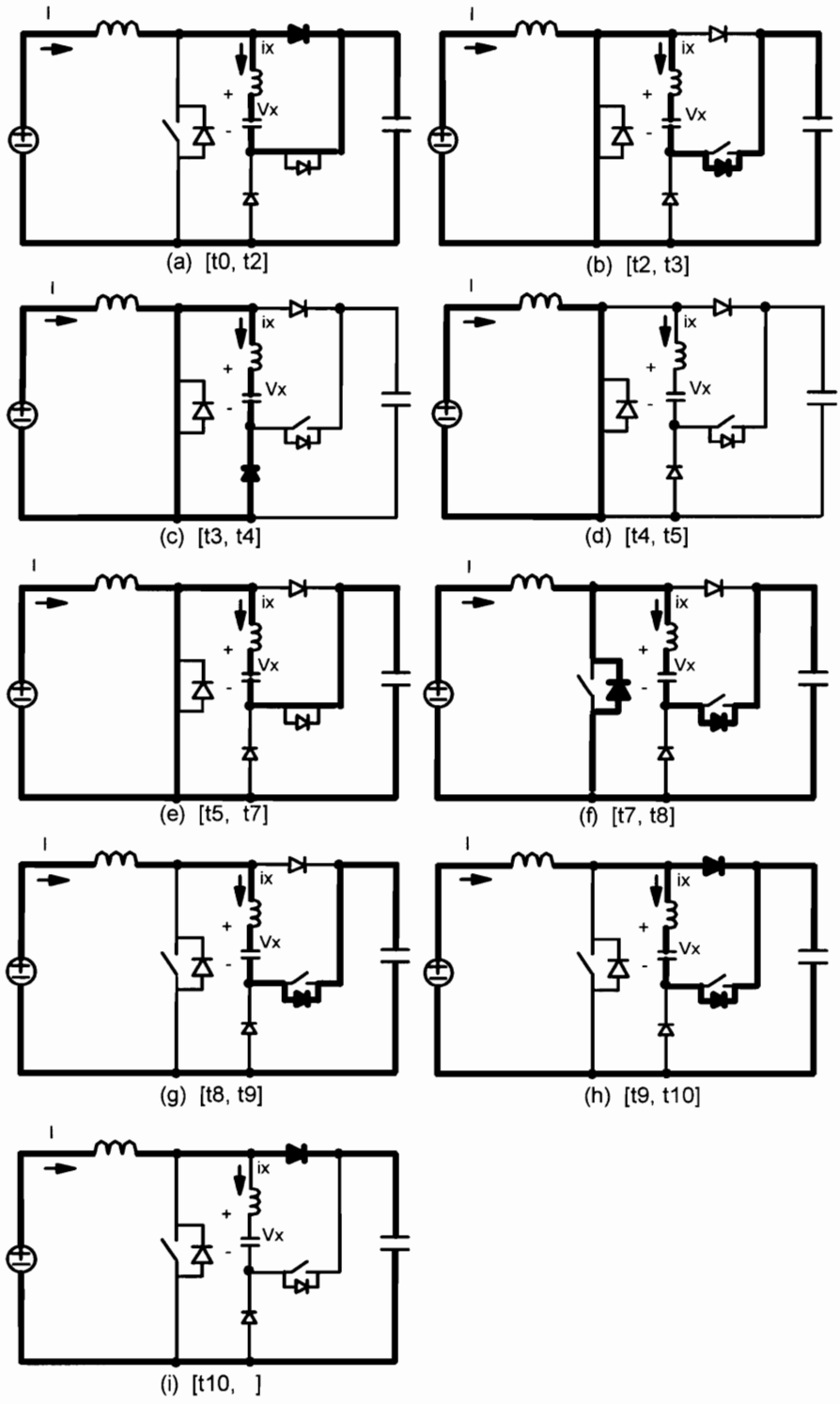


Figure 2.3 Operating stages in the soft-switching commutation.

the resonant inductor. After t2, ix decreases rapidly towards zero, since now output voltage V_o is included in the resonant path.

(c) Turn-On Transition III [t3, t4] At t3, ix returns to zero, and Dx is turned off naturally. Since the resonant capacitor voltage v_x is still positive, the auxiliary circuit continues resonating through the clamp diode Dc.

(d) Switch-On Stage [t4, t5] When i_x returns to zero again at t4, Dc is turned off naturally. The auxiliary circuit stops resonating, and is disconnected from the main circuit functionally. The converter resumes its PWM operation. The duration of this stage is determined by the PWM control.

(e) Turn-Off Transition I [t5, t7] Before the main switch is turned off, Sx is turned on at t5. The resonant tank starts to resonate again. The resonant path includes Lx, Cx, and output voltage V_o. Current i_x is negative, with its magnitude increasing from zero to peak, and then decreasing. When i_x returns to zero at t6, Sx is turned off under the zero-current condition. Since the resonant capacitor voltage v_x is less than $-V_o$ at t6, the auxiliary circuit continues resonating after t6, the positive i_x is conducted by Dx, and the current of the main switch is diverted out into the auxiliary circuit. Since Dx clamps the voltage of Sx at practically zero, the turn-off loss of Sx is largely eliminated.

(f) Turn-Off Transition II [t7, t8] At t7, i_x reaches I, and the main switch current is reduced to zero, so S is turned off under a zero-current condition. As i_x keeps increasing after t7, the surplus current will flow through the antiparallel diode of S, and clamp the voltage across S at zero. The gate signal of S can be removed, without causing much turn-off loss.

(g) Turn-Off Transition III [t8, t9] At t8, i_x falls to I, and the parallel diode of S stops conducting. Since the main diode is still reverse-biased, the main inductor current can only flow through the resonant tank, charging the resonant capacitor linearly.

(h) Turn-Off Transition IV [t9, t10] At t9, v_x is discharged to zero, and the main diode starts to conduct. The resonant tank begins to resonate again. As i_x resonates towards zero, the current in the main diode increases gradually.

(i) Diode On Stage [t10,) When i_x returns to zero at t10, the auxiliary circuit stops resonating, and is disconnected from the main circuit functionally. The inductor current is conducted by the main diode, and the converter resumes its PWM operation. The duration of this stage is determined by the PWM control.

Ideally, the peak of i_x during the turn-on transition at t2 is the same as the input current I at t9 if the resonant circuit has no power loss. Any power loss in the resonant path will reduce the attainable resonant current peak at t2. However, I is actually smaller at t2 than at t9, considering the current ripple due to finite boost inductance. Therefore, the zero-current turn-on of the main switch is still achievable in a practical circuit. After the turn-on, the current increase rate is controlled by the resonant inductor, and this fact helps to reduce the switch turn-on loss further.

Another point to notice is that the auxiliary switch is always turned on and off with zero current, and thus has very low switching loss and stress. This fact allows devices with much lower current rating than the main switch to be used in the auxiliary circuit.

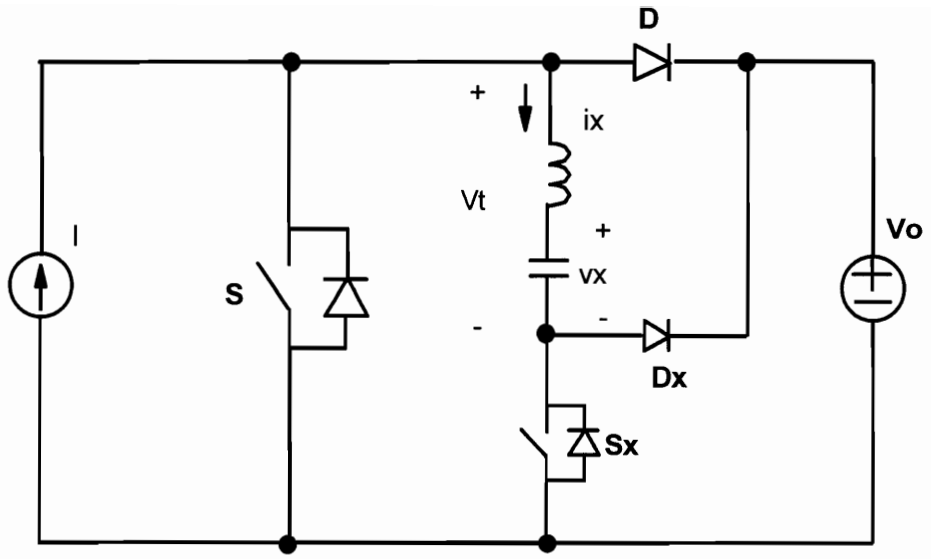
2.3 STATE-PLANE ANALYSIS OF ZCT OPERATION

The operation of the ZCT topology involves an LC resonant tank, and needs a detailed analysis. Since the current of the boost inductor, I, and the voltage of the output capacitor, V_o, can be assumed constant during the short period when the auxiliary circuit is active, the high-frequency equivalent circuits of Fig. 2.1(a) and Fig. 2.2(a) are shown in Figs. 2.4(a) and (b), respectively. The resonant inductor current i_x and the resonant capacitor voltage v_x are chosen as state variables. Assuming all the components to be ideal, the governing differential equations for the resonant tank are:

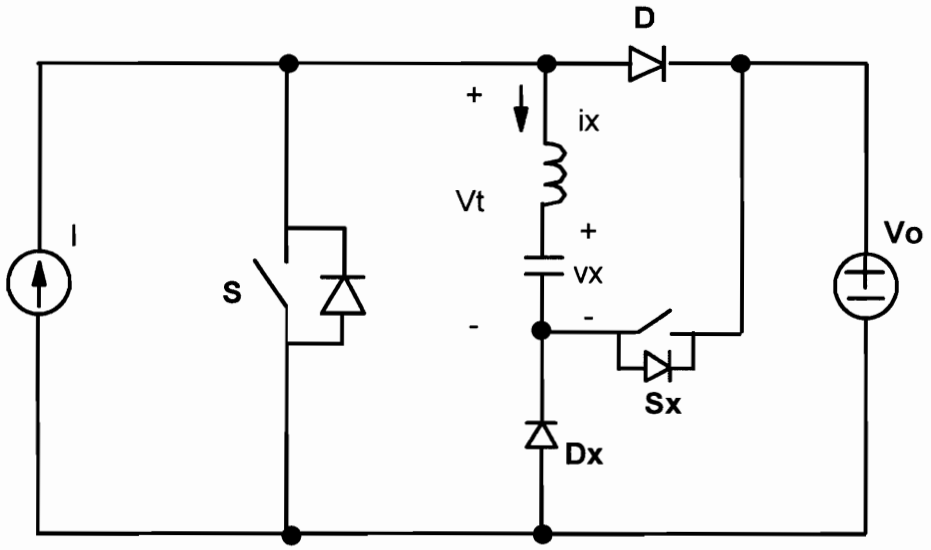
$$\begin{aligned} \frac{di_x}{dt} &= -\frac{1}{Lx}v_x + \frac{1}{Lx}V_t \\ \frac{dv_x}{dt} &= \frac{1}{Cx}i_x \end{aligned}, \qquad (2.1)$$

where V_t is the voltage across the resonant tank, and serves as the excitation to the resonant tank. V_t changes with the different operating stages of the power stage. For the operating stages shown in Fig. 2.3, in the intervals of [t0, t2], [t3, t4], and [t9, t10], $V_t = 0$; in the intervals of [t2, t3], [t5, t7], [t7, t8], $V_t = -V_o$. In the intervals when the resonant tank is in series with the input current source, i_x is no longer a state variable, and the second equation in (2.1) alone determines the circuit behavior. In the intervals of [t4, t5] and after t10 until the switch turn-on in the next switching cycle, the resonant tank is functionally disconnected from the rest of the circuit, and $i_x = 0$. In the interval of [t8, t9], $i_x = I$. In a period of $[t_k, t_{k+1}]$ in which V_t is constant and the LC tank is active, with the initial condition of $v_x(t_k) = V_{xk}$ and $i_x(t_k) = I_{xk}$, the solution to the above equations are:

$$\begin{aligned} v_x(t) &= Z_o I_{xk} \sin(\omega_o(t-t_k)) + (V_{xk} - V_t)\cos(\omega_o(t-t_k)) + V_t \\ i_x(t) &= I_{xk}\cos(\omega_o(t-t_k)) - \frac{V_{xk} - V_t}{Z_o}\sin(\omega_o(t-t_k)) \end{aligned}. \qquad (2.2)$$



(a). For Fig. 2.1(a)

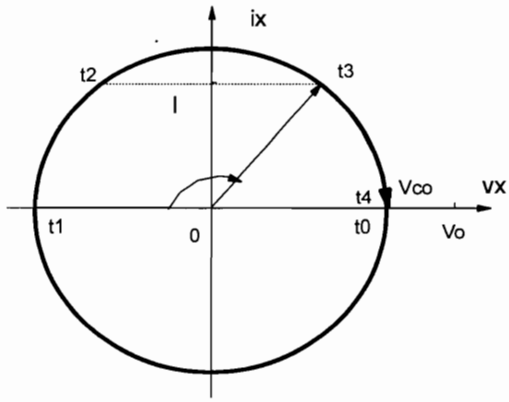


(b). For Fig. 2.2(a)

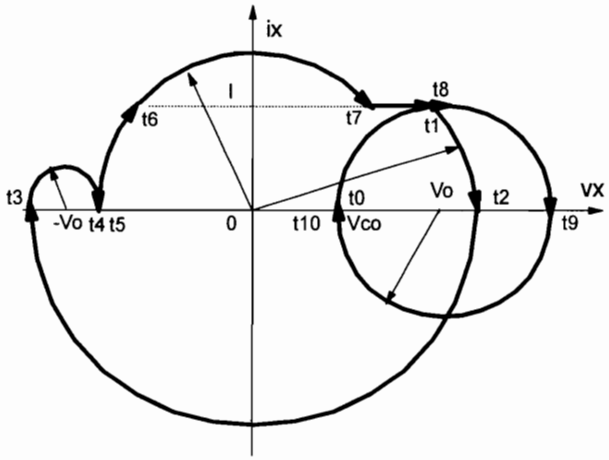
Figure 2.4 **High-frequency equivalent circuits of ZCT boost converters.** The input inductor can be treated as a current source, and the output capacitor can be treated as a voltage source in the soft-switching transition.

The above solution can be used to draw the state-plane trajectories of the ZCT circuit in i_x - v_x plane, which are more convenient to illustrate the circuit operation than waveforms [A27]. The state plane trajectories for the ZCT schemes discussed before are shown in Fig. 2.5, which clearly illustrates the functional differences among the three ZCT schemes. The time instants (t0, t1, t2, ...) in Figs. 2.5(a), 2.5(b) and 2.5(c) correspond to the time instants shown in Figs. 2.1(b), 2.1(c) and 2.2(b). The main switch or the main diode current is determined by $I - i_x$. The current is conducted by the parallel diode of the main switch when $I - i_x$ is negative. During the resonance, the state plane trajectory is part of a circle, and the radius of the circle determines the resonant tank energy and its associated conduction loss in the auxiliary circuit. Fig. 2.5(a) shows the previous ZCT operation of Figs. 2.1(a) and (b). Obviously, the reverse recovery of the main diode and the turn-on of the main switch are not affected by the ZCT circuit, and could produce high power loss in a practical circuit. The turn-off current of the auxiliary switch is I, which is the same as the turn-off current of the main switch in a hard-switching converter. Besides, the timing of the auxiliary switch directly determines the auxiliary circuit current peak, and is critical to the circuit operation. The state-plane trajectories of the ZCT topology shown in Fig. 2.1(a) with the modified control in Fig. 2.1(c) are shown in Fig. 2.5(b). All devices are now turned on and off with zero current, but the resonant circle is much larger. Besides, the timing of the auxiliary switch is still critical. The operation of the improved ZCT circuit, shown in Fig. 2.5(c), has a smaller resonant circle, so less resonant tank energy and less power loss are required. In addition, the auxiliary switch can always be turned off after being turned on for half the resonant cycle of $T_0 = 2\pi\sqrt{L_x C_x}$, so its control timing is independent of the circuit operation. This property significantly simplifies the control design.

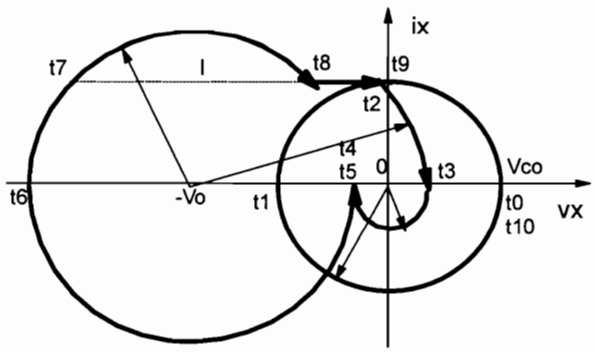
One distinctive advantage of these ZCT topologies is that all switch devices are switched under the zero-current condition. Therefore, switching losses are reduced to a large degree, so a better utilization of switches can be achieved at high switching



(a). For Fig. 2.1(b)



(b). For Fig. 2.1(c)



(c). For Fig. 2.2(b)

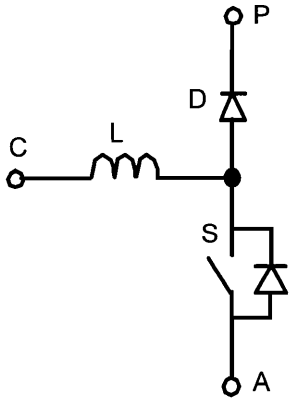
Figure 2.5 **Comparison of state-plane trajectories**. (c) has a smaller circle in the turn-off than (b), which means less energy and power loss in the auxiliary circuit.

frequencies. In addition, snubber circuits for di/dt and dv/dt limitations used in hard-switching converters are no longer required, and gate drive circuits can be simplified. These factors are especially significant for GTOs, whose snubber and gate drive circuits take a large portion of converter power loss and cost. The auxiliary switch has almost no switching loss and switching stress either, since it is turned on and turned off always with a zero-current condition. Low conduction voltage drop devices, such as GTOs, MCTs and IGBTs, can be used in the auxiliary circuit to reduce its conduction loss.

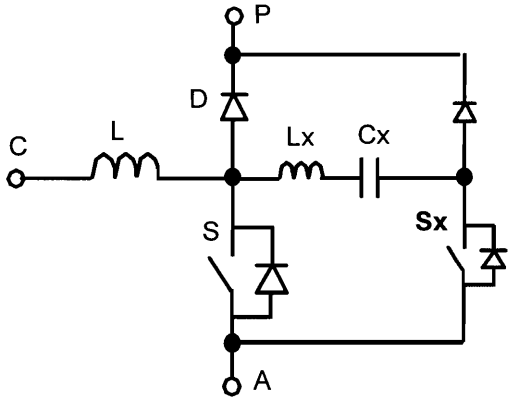
2.4 EXTENSION OF IMPROVED ZCT SCHEMES TO OTHER CONVERTERS

The proposed ZCT schemes achieve a similar switching loss reduction of resonant converters in PWM converters without increasing the voltage/current stress of switches, and are therefore suitable for high power applications. It is well known that any PWM converter can be viewed as special connections of the PWM cells, each consisting of a switch and a diode connected in a totem pole fashion, such as S and D in Figs. 2.1(a) and 2.2(a). The ZCT topologies in Figs. 2.2(a) and 2.5(a) can be used as ZCT cells to derive soft-switching converters in other topologies. The PWM cell and ZCT cells are illustrated in Fig. 2.6. By replacing every PWM cells in PWM converters with a ZCT cell, different ZCT converters can be easily derived. Several examples of dc-dc converters with the ZCT scheme presented in Fig. 2.2(a) are shown in Figs. 2.7(a) through (d). For some single-switch three-phase rectifiers, such as the DCM (discontinuous current mode) boost rectifier, this ZCT scheme can be directly applied to the PWM cell also, as is shown in Fig. 2.7(e). Since the switch turn-on loss is negligible in DCM converters, the auxiliary switch can be actuated only for switch turn-off commutation. In this case, the performance of the ZCT cell in Fig. 2.6(b) would be the same as the one shown in Fig. 2.6(c).

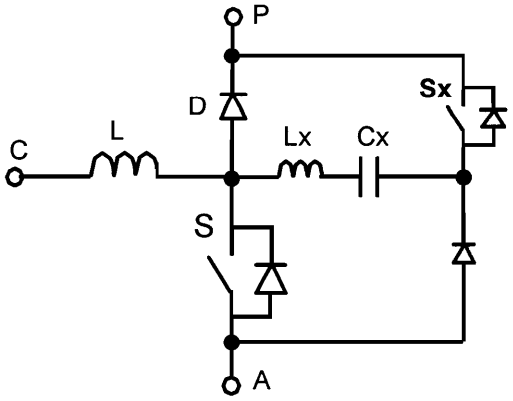
Many bridge type converters, such as full-bridge dc-dc converters, and three-phase voltage source inverters/boost rectifiers, are widely used in high-power applications. Since the load is usually inductive, the current in a half-bridge leg is commutated in a "pole-commutation" manner, i.e. from a switch to a diode in the opposite side of the same leg, or vice versa. Therefore, each leg can be divided into two PWM cells according to the switching commutation, and a ZCT cell can be used to replace each PWM cell. The LC resonant tank for a top switch and the bottom switch in the same leg can be combined, so only one resonant tank is required for a leg, as is shown in Fig. 2.8(a), in which the subcircuit shown in thick lines is a ZCT cell shown in Fig. 2.6(c). The voltage stress of



(a). PWM Cell Configuration



(b). ZCT Cell Proposed in [A34]



(c). Improved ZCT Cell

Figure 2.6 **PWM Cell and ZCT Cells**. The auxiliary circuit and the PWM cell (a switch-diode pair) can be treated as a three-terminal ZCT cell.

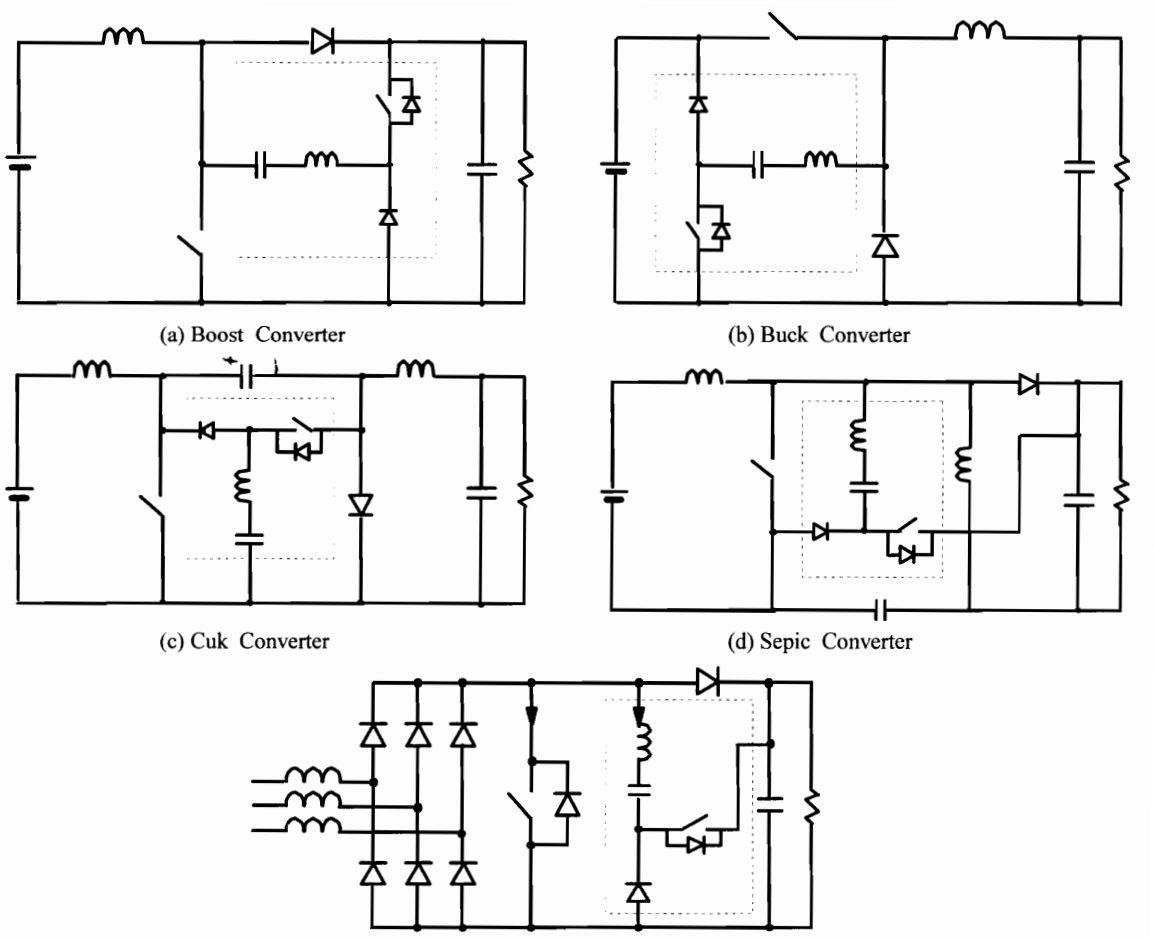
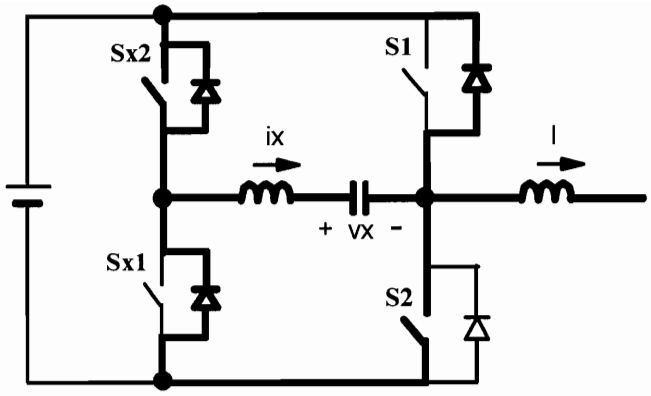
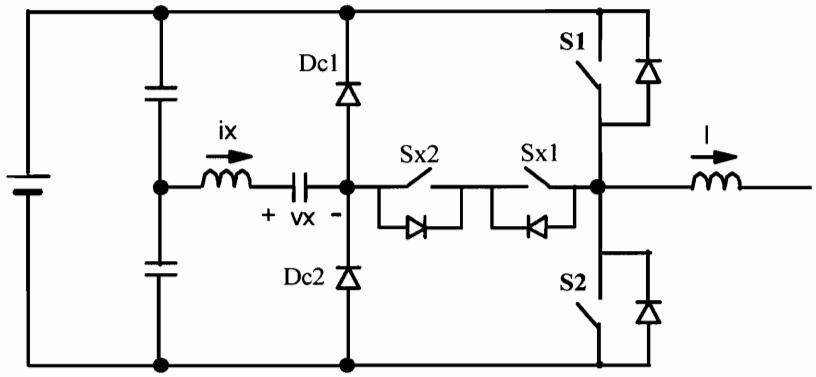


Figure 2.7 **Examples of several ZCT converters**. The PWM cell in hard-switching converters is directly replaced with a ZCT cell.

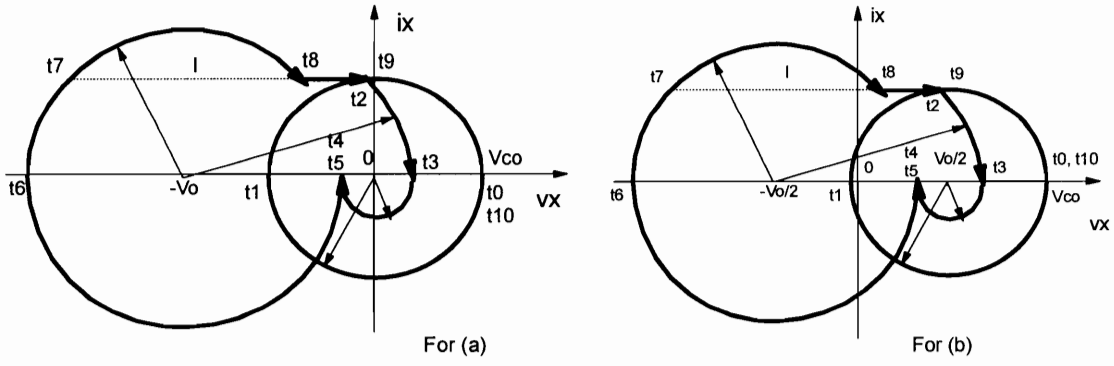
the resonant capacitor Cx is about twice that of the switches in this topology, the same as that in the original ZCT cell. This capacitor voltage peak can be reduced by the topology shown in Fig. 2.8(b), in which two series connected auxiliary switches are used for each leg, similarly to in the auxiliary resonant commutated pole (ARCP) converter in [B27]. The low power diodes Dc1 through Dc2 are used to clamp the auxiliary switch voltage, also similarly to in a practical ARCP. The ZCT circuit can be controlled to solve both turn-on and turn-off problems of the switches, which is not achieved in ARCP. Furthermore, the charge balance of the dc-link midpoint is automatically achieved in the ZCT topology. The corresponding state-plane trajectories of the operation one ZCT cell in these two half-bridge topologies are shown in Fig. 2.9(c), with the trajectories of (a), which is exactly the same as in a ZCT cell of Fig. 2.6(c), on the left, and the trajectory of (b) at the right. Obviously, the two trajectories are similar, the only difference being that vx in Fig. 2.9(b) is shifted by Vo/2 to the right. Therefore, the voltage stress of Cx is now reduced to about 1.5 times the dc-link voltage. These ZCT techniques can be used directly in full-bridge dc-dc and three-phase converters, with the examples of three-phase inverters shown in Fig. 2.9. The topology of hard-switching VSI is shown in Fig. 2.9(a). Fig. 2.9(b) shows the three-phase ZCT PWM voltage source inverters with the ZCT circuit of Fig. 2.8(a), and Fig. 2.9(c) shows the ZCT three-phase inverter with the ZCT circuit of Fig. 2.8(b). The three-phase ZCT inverter in Fig. 2.9(b) is topologically similar to the modified McMurry inverters for SCRs, except that the auxiliary switches are differently arranged, are uni-directional voltage devices, and block only up to the dc-link voltage in the ZCT inverter. Also, the operation of the auxiliary circuit is different because the auxiliary switches are controlled to achieve the soft-switching function in both turn-on and turn-off commutations of the main switches.



(a). Three-Phase VSI topology

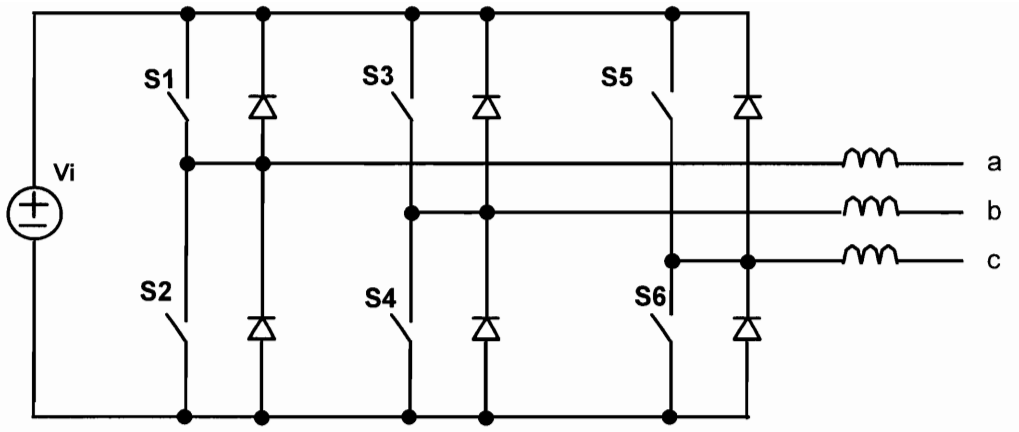


(b). Configuration of PWM Cells

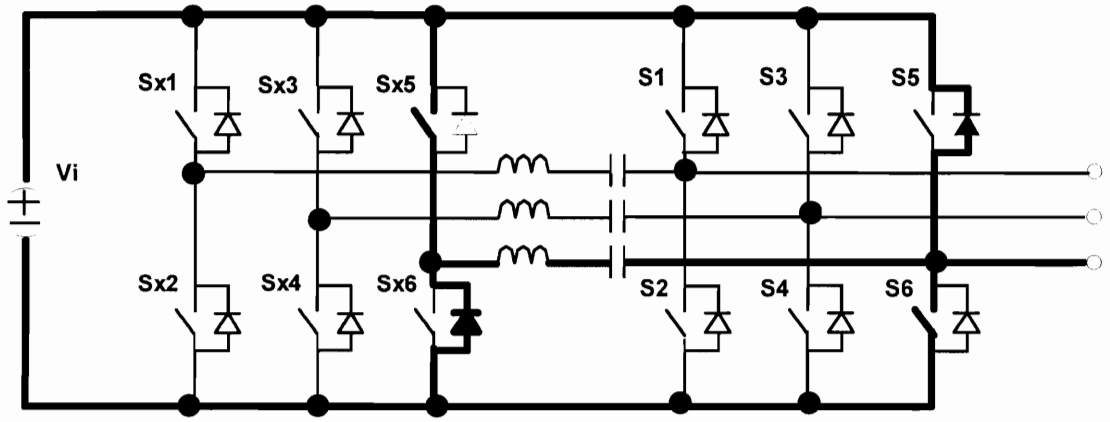


(c). State-trajectory of ZCT in (b).

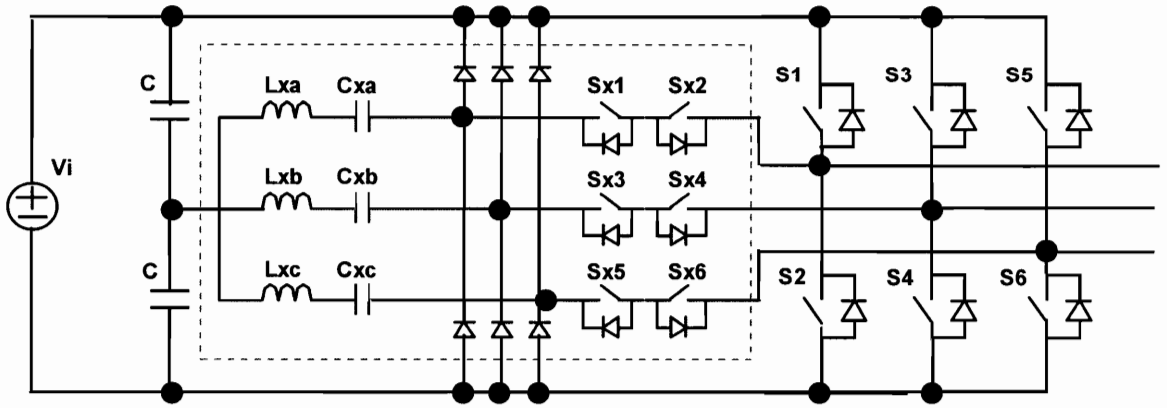
Figure 2.8 **ZCT topologies in bridge-type circuits**. The topology in (b) has a more balanced state-plane trajectory, so the voltage stress of resonant capacitor is smaller. Dc1 and Dc2 clamp the voltage of auxiliary switches to be the dc-link voltage.



(a). Three-phase PWM inverter



(b). ZCT three-phase inverter I.



(c). ZCT three-phase inverter II.

Figure 2.9 **ZCT three-phase inverters.** The soft-switching three-phase topologies are the direct applications of the topologies in Fig. 2.8.

2.5 DESIGN OF AUXILIARY CIRCUIT AND TEST RESULTS

It is desired that the soft-switching function could be achieved for all operating conditions. Therefore, the auxiliary circuit should be designed according to the maximum main inductor current, while its power loss should be minimized to achieve a good efficiency. We will discuss the design issues with the ZCT cell of Fig. 2.2(a) as an example to illustrate the basic considerations. Since the turn-off transition is more critical than the turn-on transition for high power devices, the following design procedure is mainly based on the turn-off requirement. To effectively reduce the switch turn-off loss, the duration of Turn-off Transition II, $T_{off} = T_8 - T_7$, should be long enough for most storage charge of the main switch to recombine. From the state-plane trajectory of Fig. 2.5(c), we can get:

$$T_{off} = 2\cos^{-1}(m)\sqrt{L_x C_x} = T_0 \cos^{-1}(m)/\pi, \tag{2.3}$$

where $m = I / I_{pk}$, $T_o = 2\pi\sqrt{L_x C_x}$. I is the main inductor current, and I_{pk} is the resonant peak of i_x during turn-off. Assuming v_x is zero at t5 without losing much accuracy, we can estimate I_{pk} to be:

$$I_{pk} \approx V_o / Z_0, \tag{2.4}$$

where $Z_o = \sqrt{L_x / C_x}$ is the characteristic impedance of the resonant tank.

The choice of T_{off} is device-dependent. Generally, T_{off} should be much longer than the current fall-time of the main switch. A longer T_{off} can be achieved by either increasing I_{pk} or increasing T_0. The design objective is to minimize the conduction loss caused by the soft-switching action for a given T_{off} through a proper choice of m. The design optimization requires power loss models for all switches, diodes, and reactive components. It is very difficult to find the optimum solutions analytically due to the complexity. According to the results obtained in a similar commutation circuit of SCR in

[A38] [A39], m can be chosen around 0.6. Once $m = M$ is chosen, Lx and Cx can be calculated from (2.3) and (2.4) as:

$$L_x = \frac{V_o T_{off}}{2MI\cos^{-1}(M)}, \quad C_x = \frac{MT_{off} I}{2V_o \cos^{-1}(M)}. \tag{2.5}$$

From Fig. 2.5(c), we can see that the conduction duration of the auxiliary switch is always 50% of the resonant cycle, i.e. $T_0 / 2$. The main switch can be turned on or off around the second resonant peak of ix, so the delay between the auxiliary switch turn-on signal and the main switch turn-on or off signal can be set to about $3T_0 / 2$. Therefore, the control timing of the soft switching is completely independent of circuit operation.

I_{pk} is almost constant for any input current. Since the ZCT circuit is designed to reduce the switching loss of the power devices in the worst case (i.e. at the maximum input current), the resonant current is more than necessary at light load, and the additional conduction energy loss caused by the resonant current could be higher than the saving on the switching loss. Therefore, the ZCT operation should be disabled at very light load to achieve good efficiency. Fortunately, since the thermal and electrical stresses of devices are low, the soft-switching function is not really required at light load.

There are some practical issues concerning implementing the auxiliary circuit also. The auxiliary switches should be selected mainly according to the junction temperature rise, and their current rating could be much lower than the main switches', since they conduct current only with a small duty cycle and are normally switched under the zero-current condition. The switching capability of the auxiliary switches seems not critical in normal applications. On the other hand, to ensure a high reliability or noise-immune operation of the converter, it might be desired that the auxiliary switches could turn off the resonant current peak without damage. Then, if IGBTs are used, the current rating of an auxiliary switch should be higher than half of the resonant current peak. The final choice of auxiliary switch current rating should be made according to the general system requirements in a specific application.

The effect of soft-switching schemes depends on the switching characteristics of the power devices. To evaluate the performance of the proposed ZCT schemes, two high-power devices are tested in practical circuits. One is MCT switch MCTV75P60E1 (75 A, 600 V), which has the typical switching characteristics of high power devices but is in plastic package TO-247. The other is a high power IGBT module CM400HA-24H (400 A, 1200 V).

The IGBT prototype converter is shown in Fig. 2.10. The switching frequency is selected to be 10 kHz. Typical switching voltage, current, and energy waveforms at 900 V, 100 A under both soft-switching and hard switching conditions are shown in Fig. 2.11. The switch energy, which is used to measure the switching loss, is defined as the integral of the switch voltage-current product during the switching transition. Obviously, due to the practical elimination of diode reverse recovery and zero-current switching in the ZCT circuit, the soft-switching operation gives much cleaner voltage and current waveforms than the hard-switching operation, with less noise emission and voltage stress.

Fig. 2.12 shows the efficiency improvement, switching loss, and turn-off voltage spikes at 900 V, 100 A. $T_0 = 0$ corresponds to hard-switching operation. For soft-switching operation, M is chosen to be 0.65, but To changes from $3\ uS$ to $6\ uS$ so that T_{off} changes from 0.8 uS to 1.6 uS. It can be seen that the total switching loss and voltage spike of IGBTs in the soft-switching operation can be reduced to about 20% of the values in the hard-switching operation if To is large enough. The highest efficiency improvement is achieved with $To = 4\ uS$. However, the reduction of switch voltage spike might be a major consideration in high-power applications, because the voltage stress determines the device voltage rating, which directly affects the cost and performance of the switches. Therefore, $\mathrm{To} = 5\ uS$ might be a good design choice for this example. Considering that the current falling time t_{fi} for the main switch is $0.3\ uS$ in the test circuit, To can be roughly set to be $(3 \sim 5)\ t_{fi}$ in a practical application. The

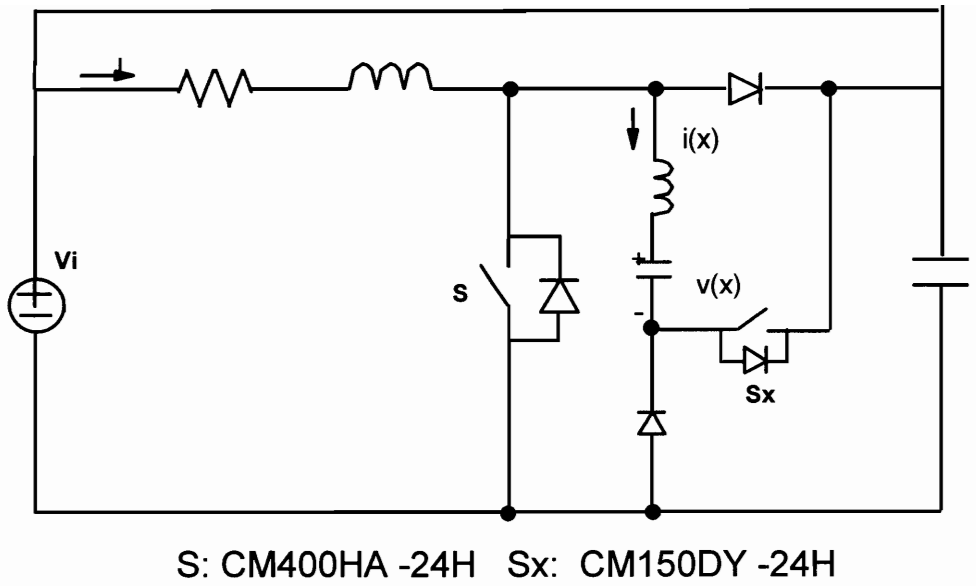
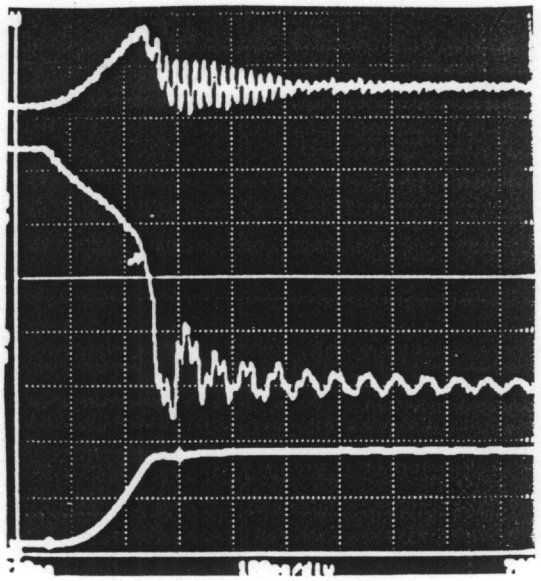
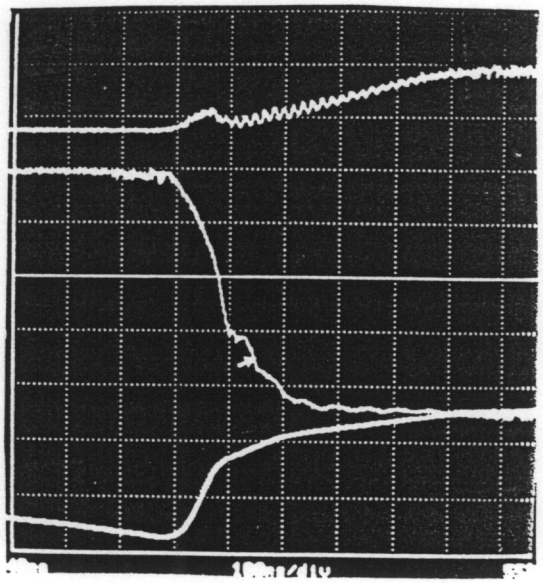


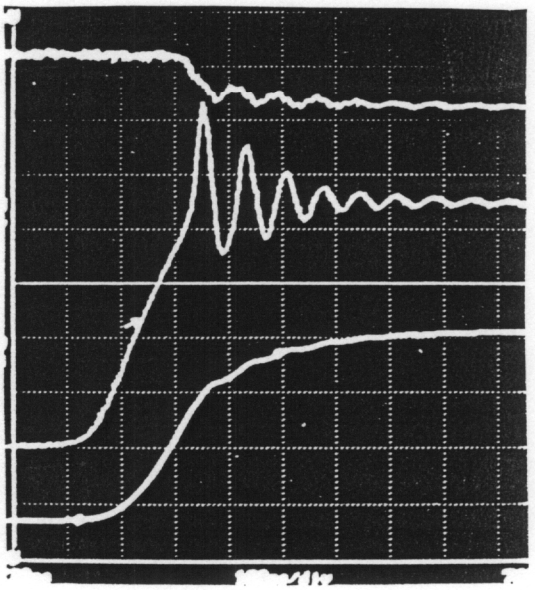
Figure 2.10 **ZCT test circuit with a high power IGBT module**. Main switch: 1200 V, 400 A, Auxiliary switch: 1200 V, 150 A (dual)



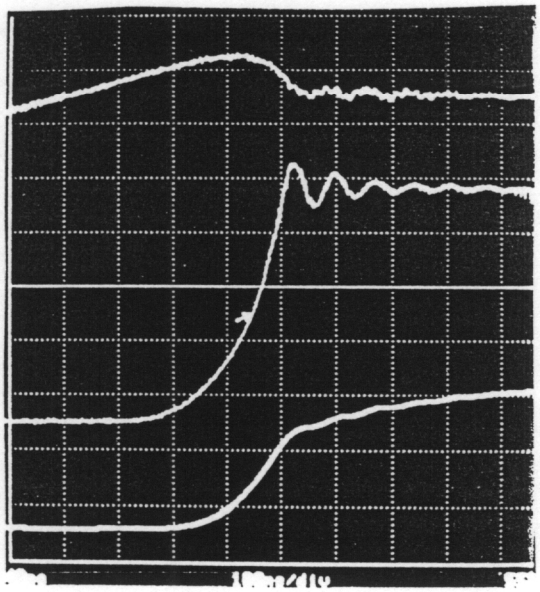
Hard-switching turn-on
Top: current 100 A/div, Mid: voltage 200 V/div
Bottom: energy 5 mJ/div, Time: 100 nS/div



Soft-switching turn-on
Top: current 100 A/div, Mid: voltage 200 V/div
Bottom: energy 1mJ/div, Time: 100 nS/div

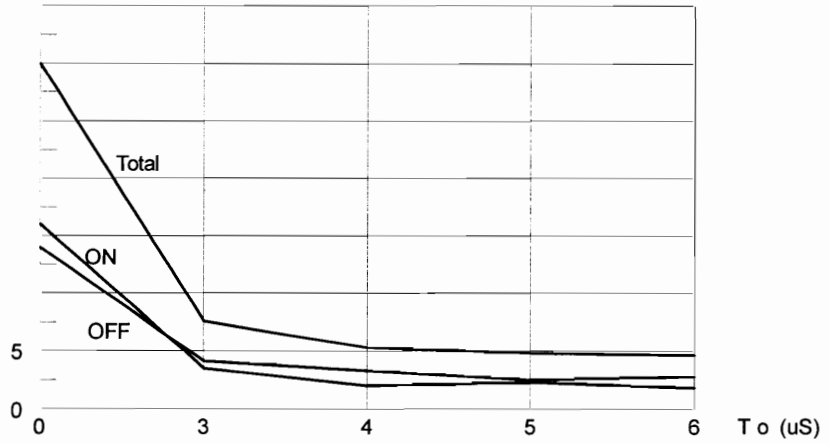


Hard-switching turn-off
Top: current 100 A/div, Mid: voltage 200 V/div
Bottom: energy 5 mJ/div, Time: 100 nS/div

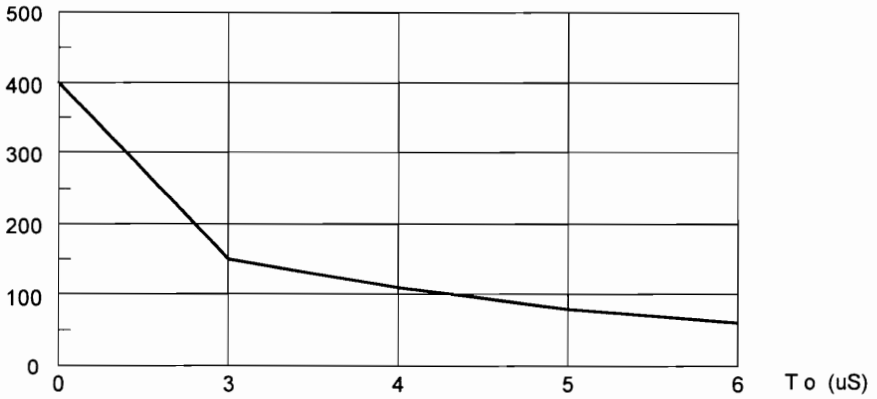


Soft-switching turn-off
Top: current 40 A/div, Mid: voltage 200 V/div
Bottom: energy 1mJ/div, Time: 100 nS/div

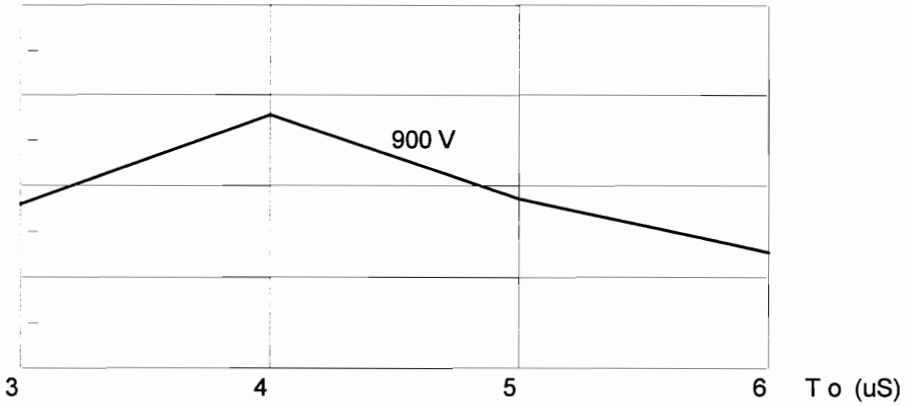
Figure 2.11 **Typical switching waveforms under soft switching and hard switching.** Testing conditions: Vce: 900 V, Ic: 100 A. The voltage spike at soft-switching turn-off is reduced to 20% of hard-switching value.



(a) Switching energy

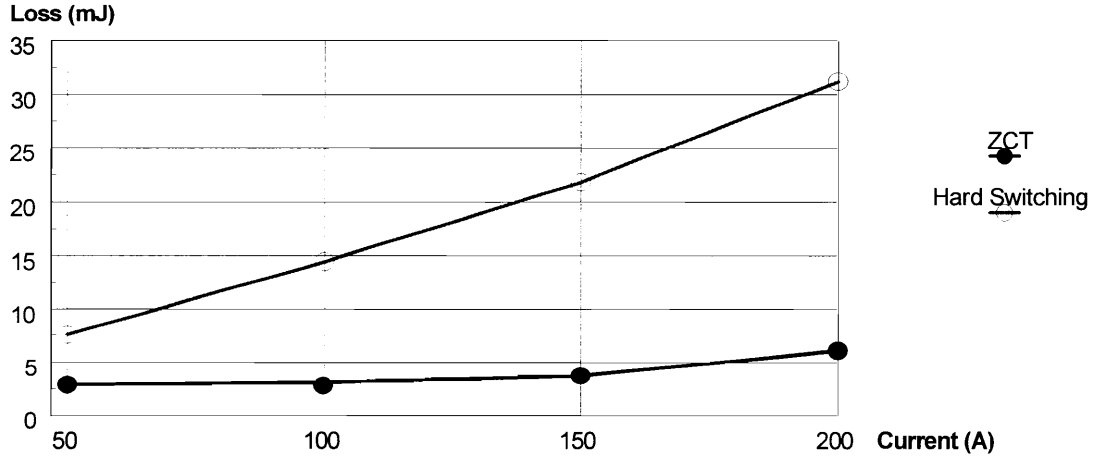


(b) Switch turn-off voltage spike

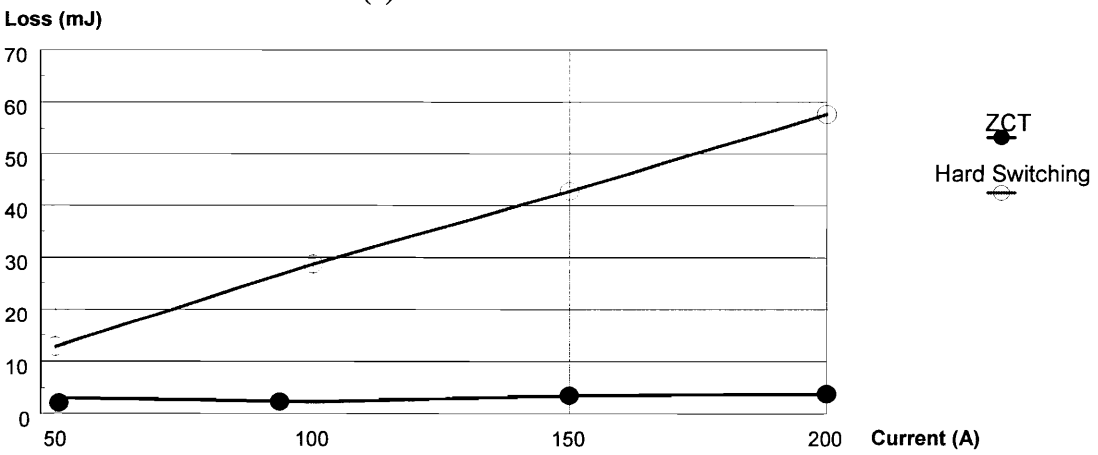


(c) Efficiency improvement

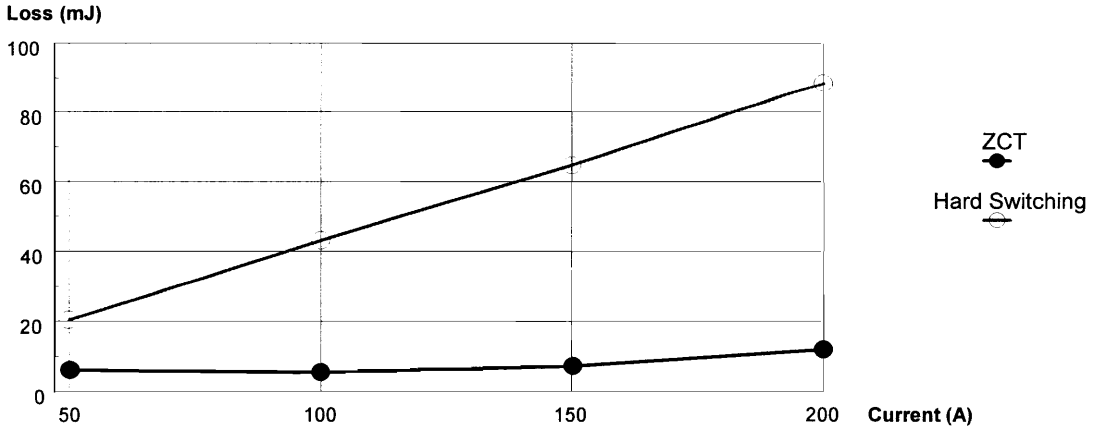
Figure 2.12 Switching losses and efficiency improvement at 900 V, 100 A.



(a) IGBT turn-on loss at 900 V



(b). IGBT turn-off loss at 900 V

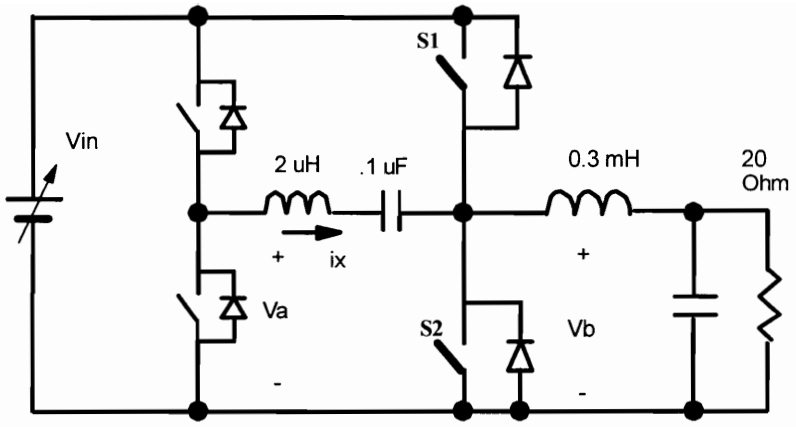


(c). Total switching loss

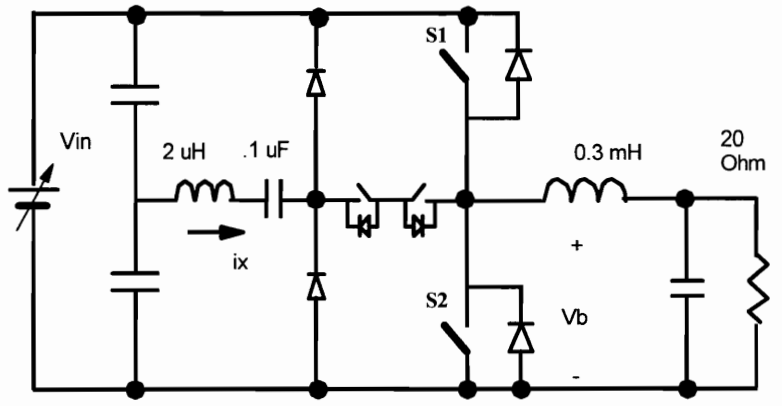
Figure 2.13 **Switching loss at 900 V with different currents.** The total switching loss with soft-switching is about 15% at 200 A, and about 30% at 50 A of hard-switching values.

switching losses of the main switch at 900 V and different currents at 70°C junction temperature are shown in Fig. 2.13. Due to the favorable operating condition under the ZCT operation, the switching losses are reduced significantly at every current level. Considering also the reduced voltage stress, the ZCT operation can significantly increase the power processing capability of a given device. Therefore, for a given application, a ZCT converter can use devices with lower voltage and current ratings (which are usually faster, cheaper, and have less power loss) than a hard-switching converter, achieving even more performance improvements and possibly cost reduction. Due to the more favorable switching conditions in a soft-switching converter, the requirement for the gate drivers can also be more relaxed. The overall system reliability might be increased as well.

Two MCT half-bridge converters with the ZCT cells shown in Figs. 2.8(a) and 2.8(b) are also built and tested. The test circuits are shown in Fig. 2.14. The switching frequency is 20 kHz in both circuits. The MCT device MCTV75P60E1 is used as the main switches, and the auxiliary switches are implemented as IGBTs IRGBC30U, which has a much lower current rating than the main switch. Fig. 2.15 shows the experimental waveforms. It can be seen that the circuit waveforms comply with the theoretical analysis and simulation. In Fig. 2.15(a), a small RC snubber is used to damp the ringing of Va when both auxiliary switches are off. Fig. 2.16 shows the measured efficiency. Considerable efficiency improvement is achieved by soft-switching operation. The topology presented in Fig. 2.14(a) has a higher efficiency than the topology shown in Fig. 2.14(b) due to its lower conduction loss in the auxiliary circuit. In the experiment, the hard-switching converter can only operate up to 300 V input voltage without a snubber, due to the limited safe operating area. However, the soft-switching converters can operate up to 430 V. This result suggests that the soft-switching schemes significantly reduce the switch stress and improve the device utilization.

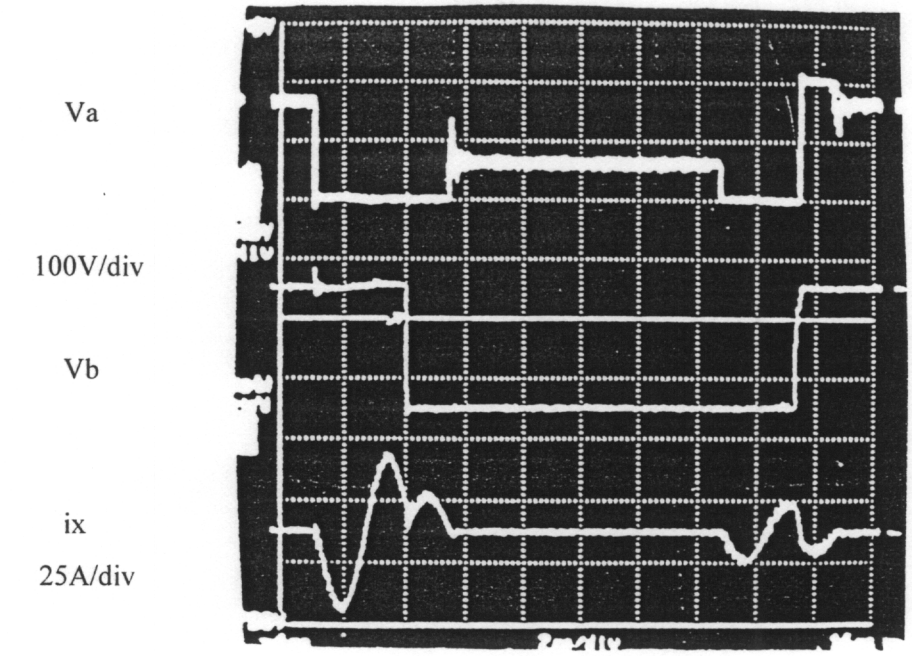


(a). A ZCT inverter leg with the topology of Fig. 2.8(a)

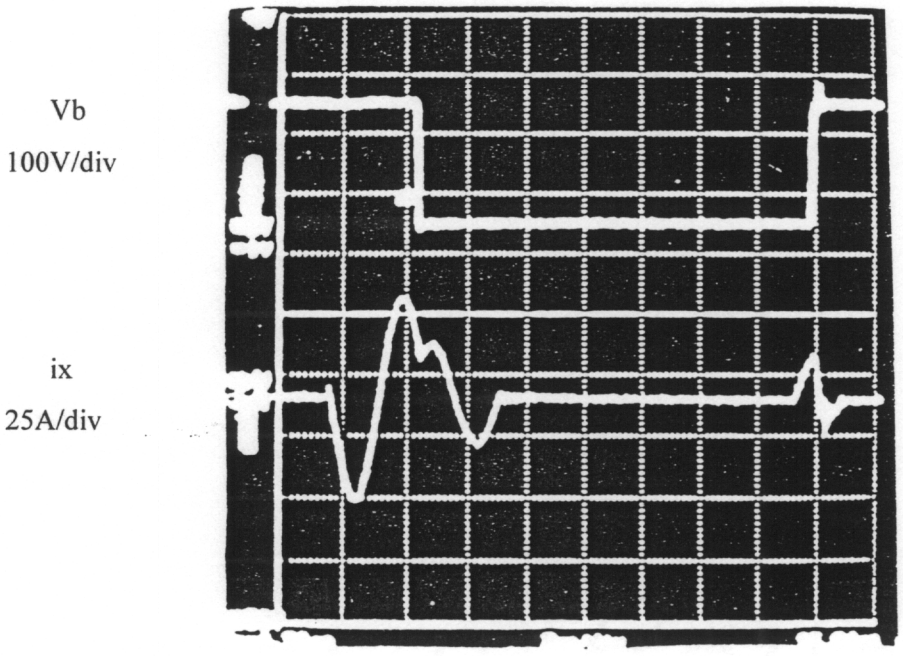


(b). A ZCT inverter leg with the topology of Fig. 2.8(b)

Figure 2.14 Experimental ZCT circuits with MCT.

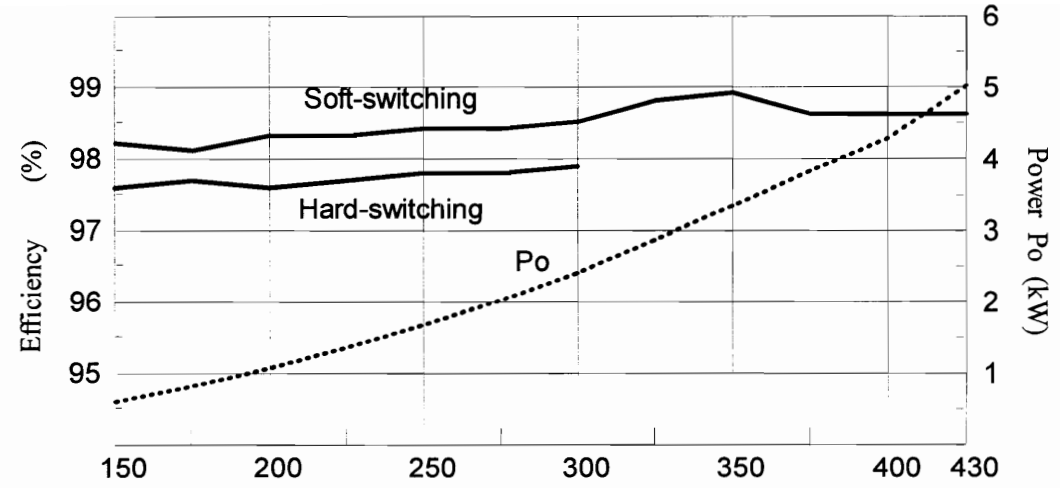


ZCT scheme in Fig. 2.12(a)

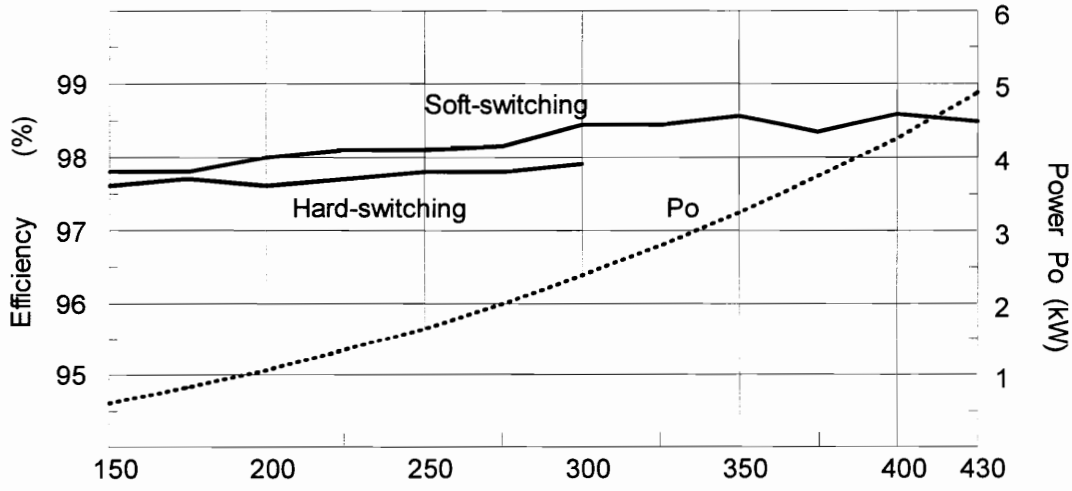


ZCT scheme in Fig. 2.12(b)

Figure 2.15 **MCT ZCT converter experimental waveforms.** Time scale is 2 uS/div.



(a) Prototype of Fig. 2.12(a)



(b). Prototype of Fig. 2.12(b)

Figure 2. 16 Measured efficiency of MCT converters.

2.6 CONCLUSIONS

Novel ZCT topologies are proposed for high-power applications. With the help of a low-power auxiliary ZCT circuit, the main switches are turned off under the zero-current condition, practically eliminating all turn-off losses. The turn-on current of the main switches is also reduced to around zero, so the switch turn-on loss and diode reverse recovery are also significantly reduced. The auxiliary switches are turned on and off with zero current, and can be implemented with low saturation voltage devices. The switches in the proposed ZCT converter have much lower switching loss and switching stress than in a conventional hard-switching converter, and therefore can operate at a much higher switching frequency and achieve a much higher power density. Also, the snubbers can be reduced or eliminated, and the gate drive circuit can be simplified in the ZCT converter. As a result, the implementation of the ZCT converter is simpler than with the conventional PWM topology, and its cost may be reduced, while its efficiency, EMI emissions, reliability, and dynamic performance are improved. The proposed topologies are relatively simple to design, and can be used in various dc-dc and three-phase converters. Experimental results prove that a significant efficiency improvement can also be achieved with the ZCT circuit, which is a distinctive advantage of the soft-switching circuit over the traditional passive snubbering approach.

3 THREE-PHASE ZERO-VOLTAGE TRANSITION BOOST RECTIFIERS/VOLTAGE SOURCE INVERTERS

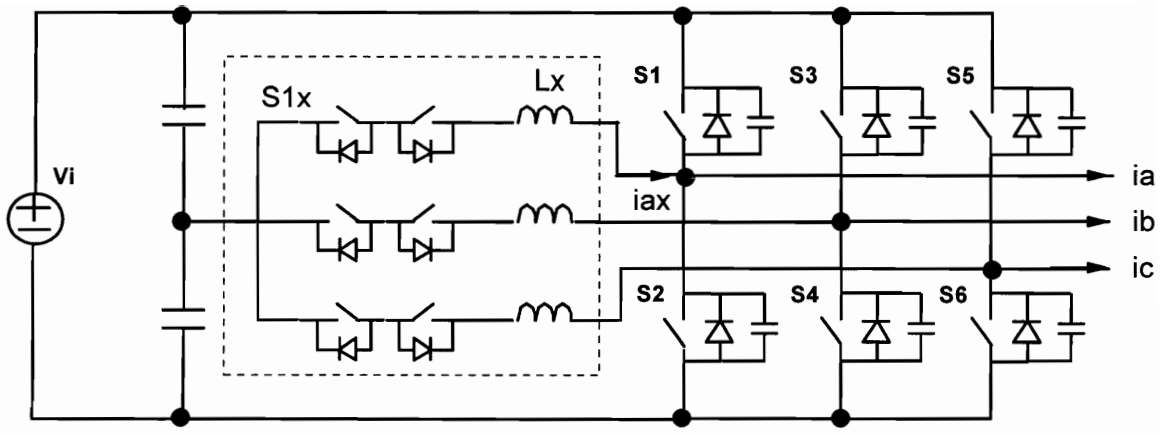
3.1 INTRODUCTION

Three-phase voltage source converters, including voltage source inverters and boost rectifiers, are widely used in industry applications. Three-phase voltage source inverters (VSIs) are widely used in many high power applications, such as motor drives, and uninterruptible power supplies (UPSs). Three-phase boost rectifiers are used as the front-end converters for motor drives and various power supplies.

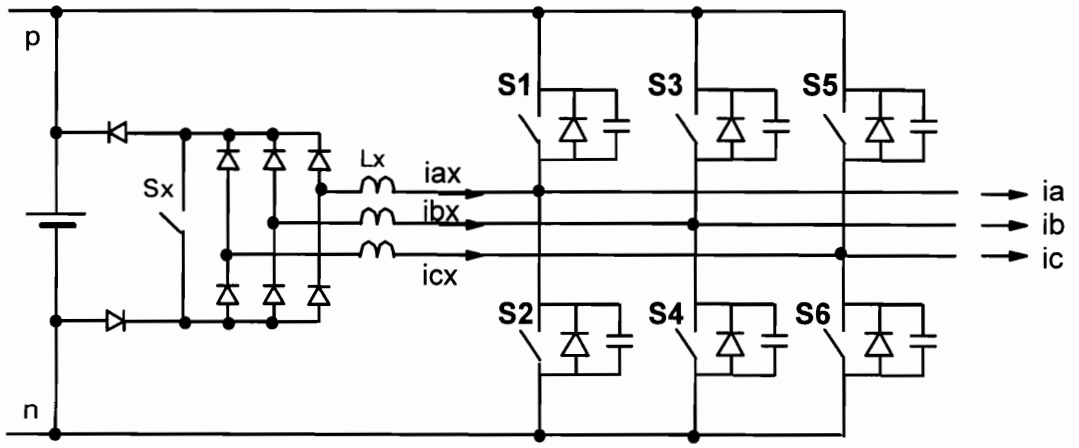
Soft switching techniques are an important issue in three-phase power converters also, especially in boost rectifiers, which require high quality input current, low EMI emission, and small reactive components. The development of soft-switching techniques for three-phase converters has been very rapid in the past decade. Most soft-switching techniques reported deal with the zero-voltage switching of the switches, since the turn-on loss of power switches is the dominating switching loss in many high-voltage medium-power applications, due to the severe diode reverse recovery problem. Due to the complexity of the three-phase circuitry, many soft-switching schemes apply the soft-switching mechanism, similar to QRC or ZVT techniques in dc-dc converters, to the common dc link instead of directly to each bridge switch. This dc-link commutation strategy is exemplified by the resonant dc link (RDCL) technique [B9] [B10] using the QRC concept and various parallel resonant, quasi-resonant, and ZVT techniques using the ZVT concept with a dc-link switch [B13]-[B22]. The major shortcoming of the dc-link commutation schemes is that an additional component, a switch or an inductor, is inserted into the dc link, and causes high power loss or more than minimum voltage stress to the main switches. To overcome these shortcomings, the auxiliary circuit can be placed at the ac side of the converter to apply the soft-switching mechanism directly to each main

switch, so the auxiliary circuit is not in the main power path and has less power loss, while the voltage stress of the main switches is kept at the minimum.

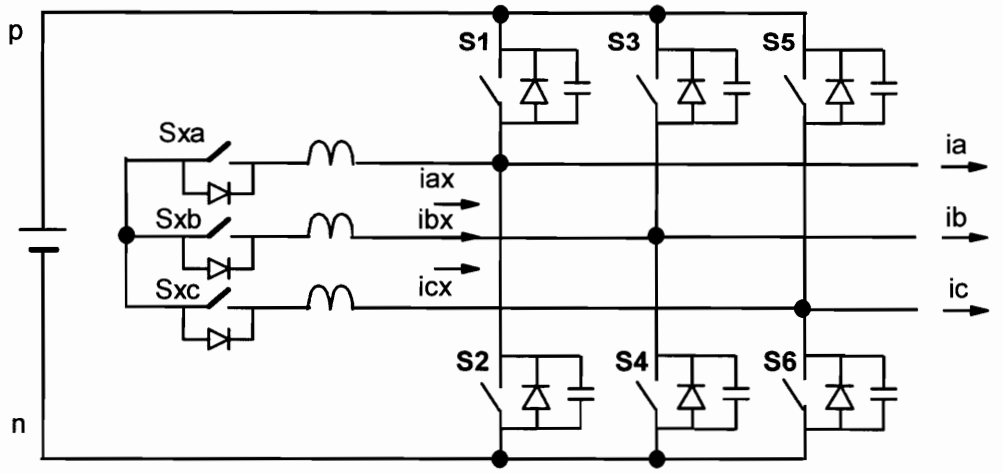
One example of ac-side soft-switching techniques is the auxiliary resonant commutated pole (ARCP) converter [B26, B27], shown in Fig. 3.1(a). The auxiliary circuit consists of three parts, one for each inverter leg. The major function of the auxiliary circuit is to shape the switch voltage to zero in the commutation from a diode to a switch in any phase leg. Any modulation scheme of the main power stage can be used in ARCP, since a functionally independent soft-switching circuit for each main switch is provided. Another advantage is that the auxiliary switches block only half of the dc-link voltage, and are turned off with zero current, which is very desirable in high power applications. The key waveforms in a turn-on commutation from D2 to S1 are shown in Fig. 3.1(d), which clearly shows the zero-voltage switching of the main switch S1. To get zero-voltage turn-on for the main switches, however, the currents in the resonant inductors have to be charged to higher than the corresponding phase current plus a "boost" current before the auxiliary circuit is allowed to resonate, so that there is enough energy to discharge the snubber capacitance completely. To provide a path for the extra charging current in this overcharging process, the anti-parallel switch of the outgoing diode is turned on at the beginning of the commutation, as is shown in Fig. 3.1(d) by the shaded area. This overcharging action will require the anti-parallel switch be turned off with certain current, as is illustrated by the turn-off of S2 at t2. This turn-off action is additional to the requirement of PWM control, and causes extra turn-off losses and conduction loss. In very-high-power, low-switching frequency applications, the control timing in the soft-switching transition can be adjusted according to the phase current, so that a minimum "boost" current, which is just enough to compensate for the power loss in the resonant circuit and discharge the incoming switch voltage to zero, is provided under any condition, and the extra turn-off current of the main switches is just the boost current, which can be significantly smaller than the phase current. Also, the large capacitor snubber affordable at a low switching frequency can further reduce the switch turn-off



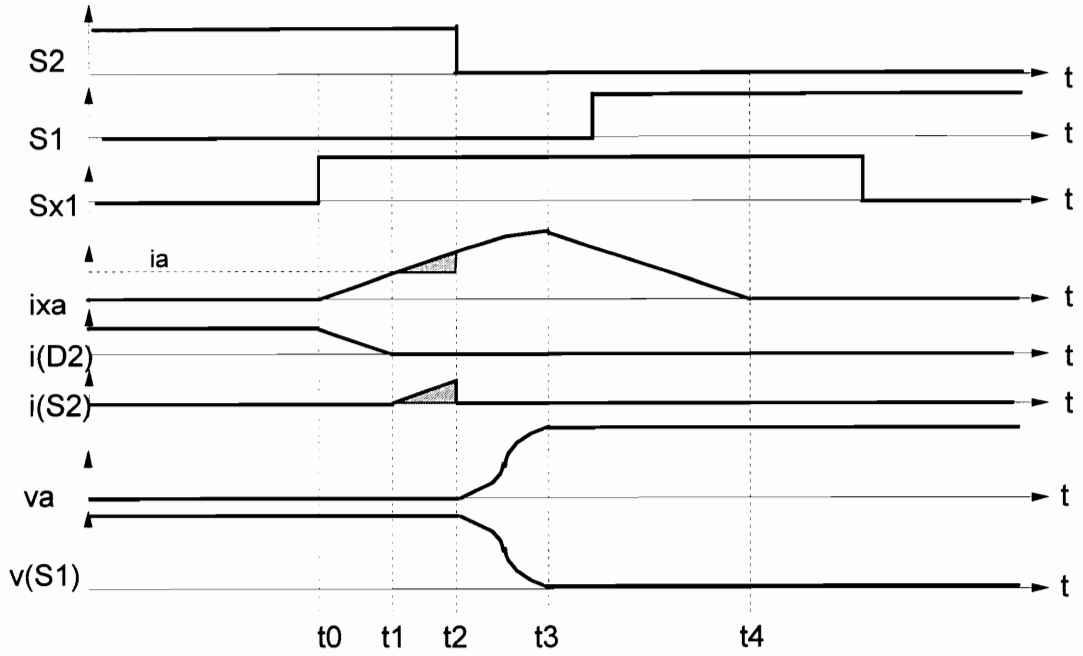
(a). Auxiliary resonant commutated pole inverter [B26, B27]



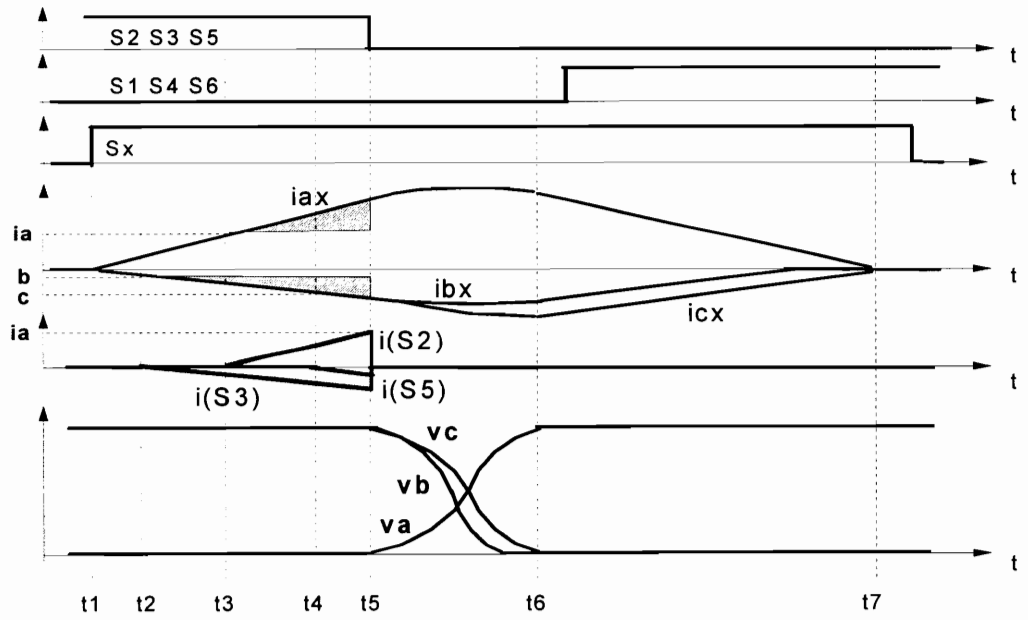
(b). Three-phase ZVT boost rectifier/voltage source inverter [B29, B42]



(c). Resonant snubber based three-phase inverter [B30]



(d). Commutation from D2 to S1 in ARCP



(e). Commutation from D2, D3, D5 to S1, S4, S6 in ZVT inverter

Figure 3.1 Existing soft-switched three-phase voltage source inverters/boost rectifiers. These techniques all use resonant overcharging to provide zero-voltage switching for main switches, and have extra main switch turn-off loss.

loss. Although its topology and control are complex, ARCP is still attractive in very-high -power applications. However, in a lower power level, the switching frequency is usually high, e.g. in the 20 ~ 100 kHz range. It is then impractical to adjust the soft-switching timing to the phase current due to the associated control complexity. Instead, the control timing is usually set according to the maximum phase current, and fixed for all operating conditions. With this control, the extra turn-off current of the main switches will be comparable to the phase current, or even higher than the phase current. Since only small snubber capacitors can be utilized due to the high switching frequency, the extra turn-off loss of the main switches is no longer negligible, and significantly limits the efficiency improvement attainable. Also, six auxiliary switches are required to achieve the soft-switching operation, and the high cost of the auxiliary circuit limits its applications.

A much simpler three-phase ZVT topology is proposed in [B29] [B42], trying to simplify the auxiliary circuit. This topology is shown in Fig. 3.1(b). The turn-ons of all bridge switches are synchronized with a modified space vector modulation scheme [B42], and one auxiliary switch can create ZVS turn-on conditions for all the main switches. Fig. 3.1(e) shows the key waveforms of the commutation from D2, D3, D5 to S1, S4, S4. The drawback of this topology is that one of the resonant inductors in the ZVT auxiliary circuits need to be charged to about twice the phase current peak, since the resonant inductors in different phases enter the overcharging mode at different times, as is illustrated by t2, t3 and t4 in Fig. 3.1(e) . The overcharging of the resonant inductors not only increases the current rating of the auxiliary circuit, but also results in more turn-off action of the main switches, and therefore "extra" turn-off loss. Compared with a hard-switching PWM counterpart with optimum modulation, the total turn-off current of the main switches in the ZVT inverter in each switching cycle is about four times higher in rectifier mode, and more than two times higher in inverter mode. Auxiliary resonant snubber topologies reported in [B30] [B31] use a concept similar to the ZVT concept. The operation of the auxiliary circuits is also similar to the principle discussed in [B29]. These topologies are mainly intended for brushless dc motor drives, in which non-

adjacent space vector modulation can be used. For general inverter/rectifier applications, the non-adjacent vector modulation reduces the dc-link voltage utilization and results in high current ripple. The delta-connected version uses six auxiliary switches, but still needs modification to the modulation scheme and requires large overcharging of the resonant inductors [B31], so it is not very attractive for general applications. The Y-connected version, shown in Fig. 3.1(c), requires three auxiliary switches, and is more appropriate than the delta-connected version for general three-phase applications. Its performance is similar to that of the ZVT inverter in [B42].

A common drawback for the existing ac-side commutation soft-switching scheme is that overcharging of resonant inductors is used to achieve the soft-switching function. The control of the overcharging is difficult, since, ideally, the timing of the auxiliary circuits should be adjusted according to phase currents. In high switching frequency applications, the duration of the resonant inductor charging stage is usually set according to the maximum phase current, in order to ease the control burden. Unfortunately, this fixed auxiliary circuit timing will cause large extra turn-off currents of the main switches, especially when the three-phase currents are small in light load. The overcharging problem is especially severe in the topologies in [B29]-[B31] [B42], where one of resonant inductors has to be charged to about twice the maximum phase current in every soft-switching commutation. The resulting high turn-off loss can severely limit, or even totally offset, the efficiency improvement of zero-voltage turn-on. This problem leaves a room for further improvements.

In this chapter, several new soft-switching techniques for three-phase converters will be investigated based on careful arrangement of SVM schemes. In section 3.2, SVM schemes for VSC will be discussed, and an "optimum" scheme will be identified. Based on this "optimum" SVM, generalized PWM cells will be identified and used to simplify three-phase ZVT topologies. A novel bi-directional ZVT PWM boost rectifier will be presented and evaluated in Section 3.3. With the help of a low power auxiliary circuit, the diode reverse recovery problem is completely eliminated in the proposed topology,

while the main switch turn-on voltage is reduced to zero in rectifier mode and to around 1/2 of the dc-link voltage in regenerative (inverter) mode. The current in the auxiliary circuit is automatically limited to the maximum phase current plus a resonant peak, and the soft-switching condition can be kept as long as desired. The extra turn-offs in the soft-switching topologies in [B29]-[B31] [B42] are also eliminated in rectifier mode and reduced in inverter mode. So, the energy dissipation and control complexity of the ZVT circuit, and turn-off loss of the main switches are reduced significantly compared to those described in [B29~B31, B42]. To reduce the voltage and current stresses of the auxiliary switches, Section 3.4 investigates soft-switching topologies with auxiliary switches connected to the midpoint of the dc link. The auxiliary switches in these schemes block only half of the dc-link voltage, and are turned off with zero current in rectifier mode; therefore, they have a much lower power loss and can be implemented at a lower cost. Many of these soft-switching schemes are tested experimentally to verify their operation. A simple power loss model for IGBTs is also developed based on experimental data, and used in switching model simulation to evaluate the efficiency performances of different soft-switching topologies. Significant efficiency improvements of the proposed soft-switching schemes over hard-switching converters are demonstrated in the simulation.

3.2 SPACE VECTOR MODULATION AND GENERALIZED PWM CELLS IN THREE-PHASE VOLTAGE SOURCE CONVERTERS

Various PWM schemes are used in three-phase converters to synthesize the desired voltages [E1]-[E9]. Space vector modulation (SVM) [E1]-[E5] [E7] [E8] has been increasingly used nowadays due to its superior performance. Some special arrangements of SVM schemes for soft-switching converters were studied in [B41] [B42]. Generally, in SVM schemes for zero-voltage switching converters, the turn-on of the main switches in all three phases should be synchronized so that only one turn-on instant could occur in each switching cycle; thus, one auxiliary switch can provide the soft-switching condition for a group of main switches. This section will describe several SVM schemes with active switch turn-on synchronization. The turn-on synchronization can also be easily implemented in other control schemes, such as the sinusoidal PWM (SPWM).

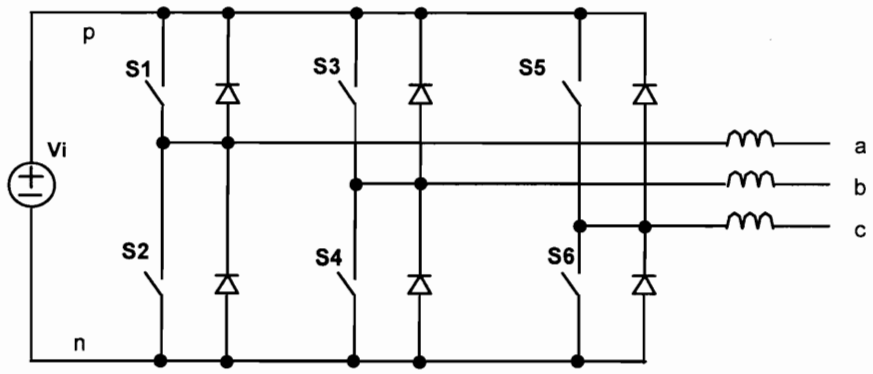
Any set of voltages or currents in a balanced three-phase system has only two independent variables. According to the SVM theory, the three-phase voltages and currents in a three-phase system can be represented in an orthogonal two-dimensional space (α-β plane) through a basis transformation, if the sum of corresponding three-phase variables is zero, or is not relevant to the circuit operation [E1] [E4]. The transformation from three-phase variables x_a, x_b, x_c to α-β system x_α, x_β is defined as:

$$\begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} = T \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix},$$

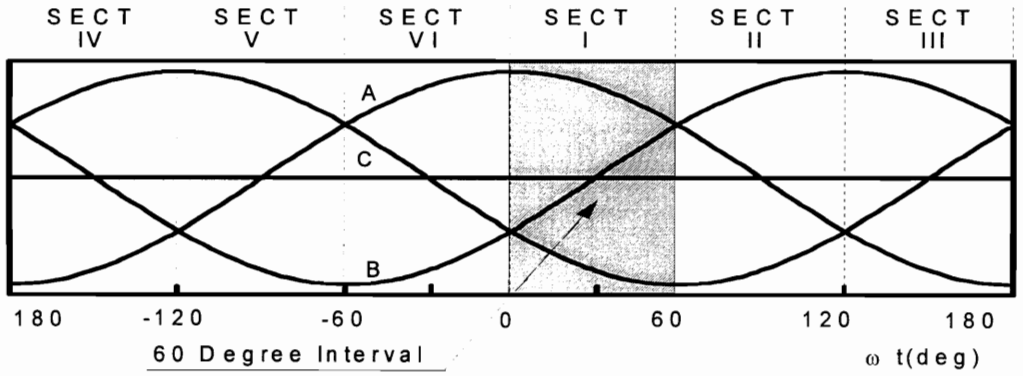
where $T = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix}$ is the transformation matrix.

Therefore, voltages and currents in a three-phase converter can be represented as vectors in the α-β plane. These vectors are called "space vectors". The trajectory of a vector representing any balanced set of three-phase sinusoidal variables (such as three phase or line voltages/currents) is a circle, with its radius proportional to the amplitude

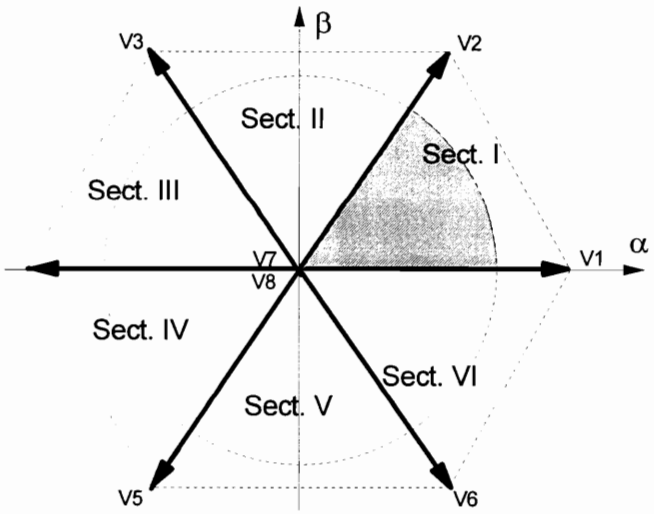
and rotating speed proportional to the frequency of the sinusoidal variables. A three-phase VSC can have eight switch states under the constraint that the two switches in any phase leg do not conduct simultaneously to avoid short-through of the bridge. These switch states are represented by the combinations such as "PNN", "PPN", etc. in Fig. 3.2. The sequence of the combinations is Phase A-Phase B-Phase C. "P" means that the phase is connected to the positive dc rail "p" of the dc link through the top switch in that phase leg, while "N" means that the phase is connected to the negative dc rail "n" of the dc link through the bottom switch in that phase leg. For the eight states, the phase voltages at each state can be represented as a space vector, denoted as V1 through V8 in Fig. 3.2(c). V1 through V6 are non-zero vectors, while V7(PPP) and V8(NNN) are zero vectors because their lengths equal zero. The six non-zero vectors divide the α-β plane into six sections, which are called Sector I through Sector VI. In steady state of balanced three-phase converters, the reference vector V_r for the averaged phase voltages rotates in the α-β plane with constant length. At any given time, V_r can be synthesized with the two adjacent non-zero vectors and zero vectors. Since the operation of the converter is symmetrical in every 60° interval, the 60° period of $\omega t = [0^o, 60^o]$ can be used to illustrate the modulation schemes. This corresponds to a reference vector in Sector I, as is shown in the shaded area in Fig. 3.2. According to the SVM principle, V1, V2, V7, and V8, should be used to synthesize the reference voltage vector. The selection of V7 or V8 as the active zero vector will not affect the phase voltages, but can affect the switching losses and implementation of the soft-switching circuit. To achieve zero-voltage turn-on of the main switches with minimum auxiliary circuit intervention, the proper way to choose active zero vector and switching sequence is to synchronize all active switch turn-on instants to facilitate the soft-switching operation.



(a). Three-phase voltage source converter



(b). Three-phase sinusoidal voltages



(c). Voltage space vectors of three-phase voltage source converters

Figure 3.2 Three-phase voltages and voltage space vectors in a three-phase voltage source converter. The switches in a VSC can produce six non zero space vectors, and two zero vectors. Three phase voltages can be synthesized with these vectors.

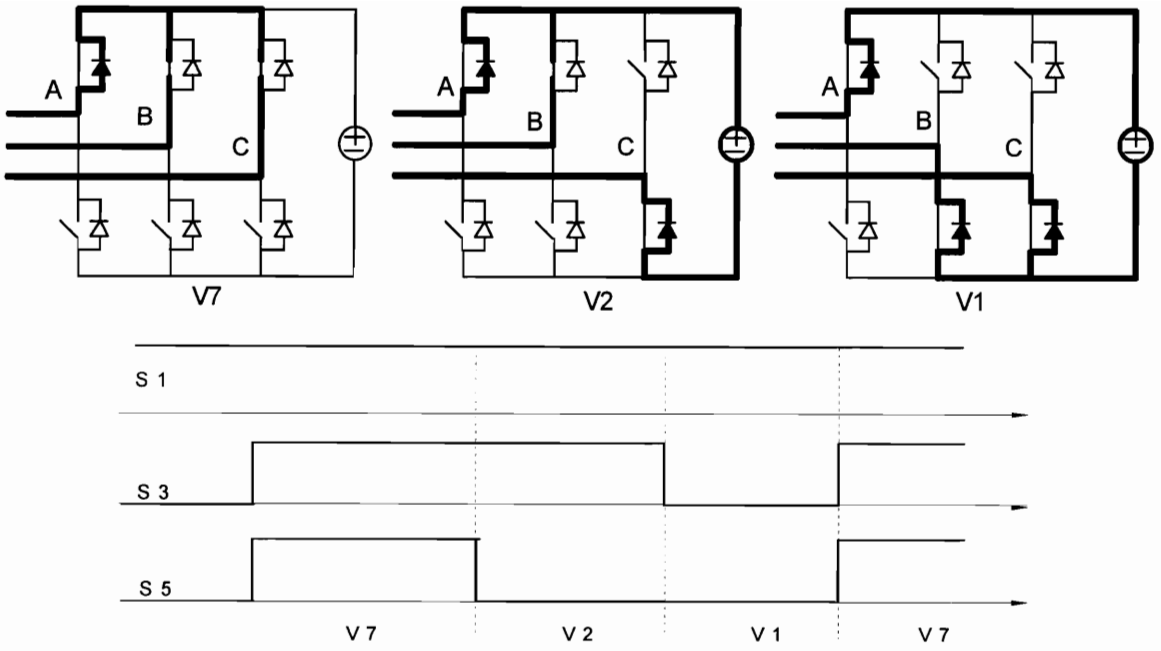
1. The modulation scheme in rectifiers

Phase currents are controlled in phase with phase voltages in rectifiers. Therefore, the current in Phase A has the highest magnitude among the three phases in the first 30° interval of Sector I, while the current in Phase C has the highest magnitude among the three phases in the second 30° interval. V7 ("PPP") is chosen as the active zero vector in the interval of $\omega t = [0^o, 30^o]$, which means that the current of phase A is conducted by D1 (the anti-parallel diode of S1) during this period. V8 ("NNN") is chosen as the active zero vector in the interval of $\omega t = [30^o, 60^o]$, which means that phase C current, the highest phase current, is conducted only by D6 during this period. Therefore, the highest phase current is conducted only by a diode and never switched, and both switching loss and conduction loss of the switches are minimized. The switching sequences and the corresponding gating signals are shown in Fig. 3.3 for different phase currents. The turn-on of S1 in (a) and S6 in (b) in these schemes does not affect the circuit operation, since the current is already conducted by its anti-parallel diode D1. Note that the active zero vector is toggled between V7 and V8 every 1/6 line cycle with these schemes.

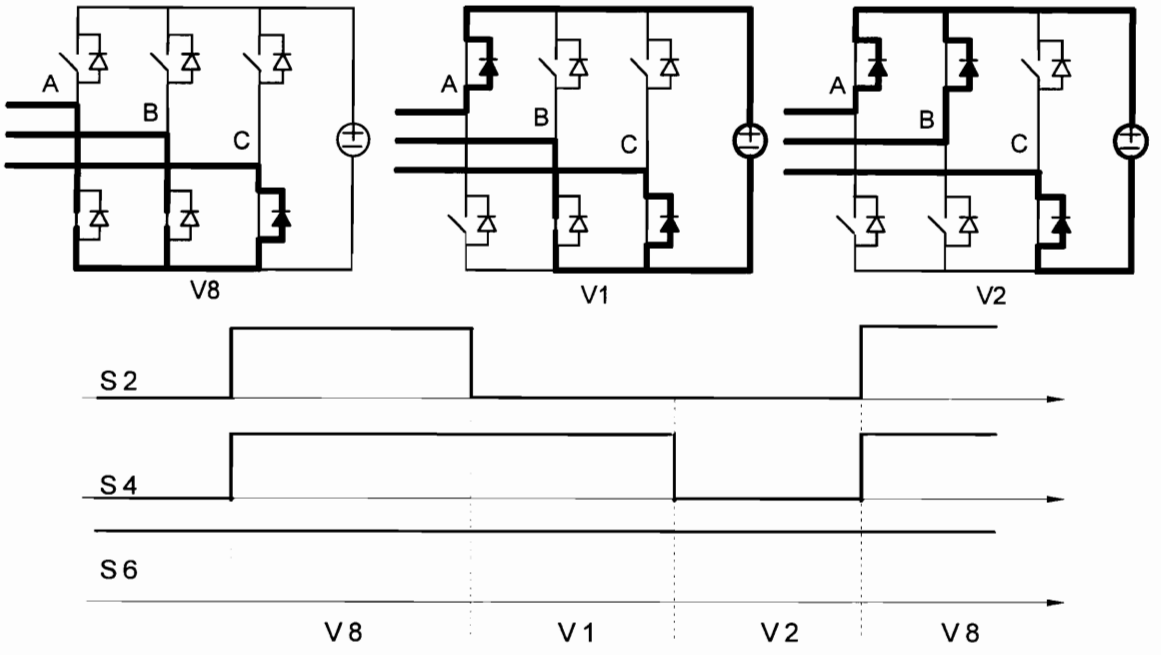
2. The modulation scheme in inverters

In inverter mode operation, the polarity of the three phase currents is reversed. If the displacement angle is within ±30°, the highest current in the given 60° interval is still in Phase A or Phase C. The switching of highest phase current can also be avoided through a proper selection of active zero vector: "PPP" if the highest current is in Phase A, and "NNN" if the highest current is in Phase C. All switch turn-ons in three phases can still be synchronized, and the corresponding switching sequences for different phase currents are shown in Figs. 3.4(a) and (b).

If the displacement angle is beyond the range of [-30°, +30°], as in some inverter applications for motor drive, modified SVM schemes like the one proposed in [B42] can be used instead, which also synchronize the switch turn-ons in all three phases.

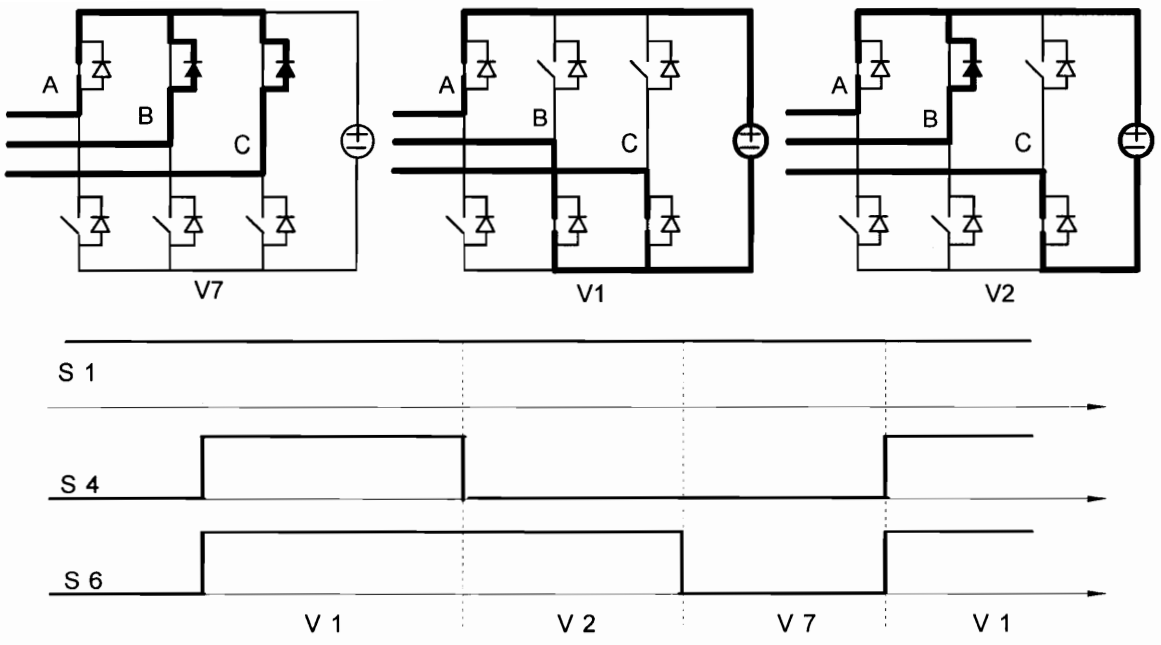


(a). Highest current in Phase A: switching sequence is V7--V2--V1--V7--

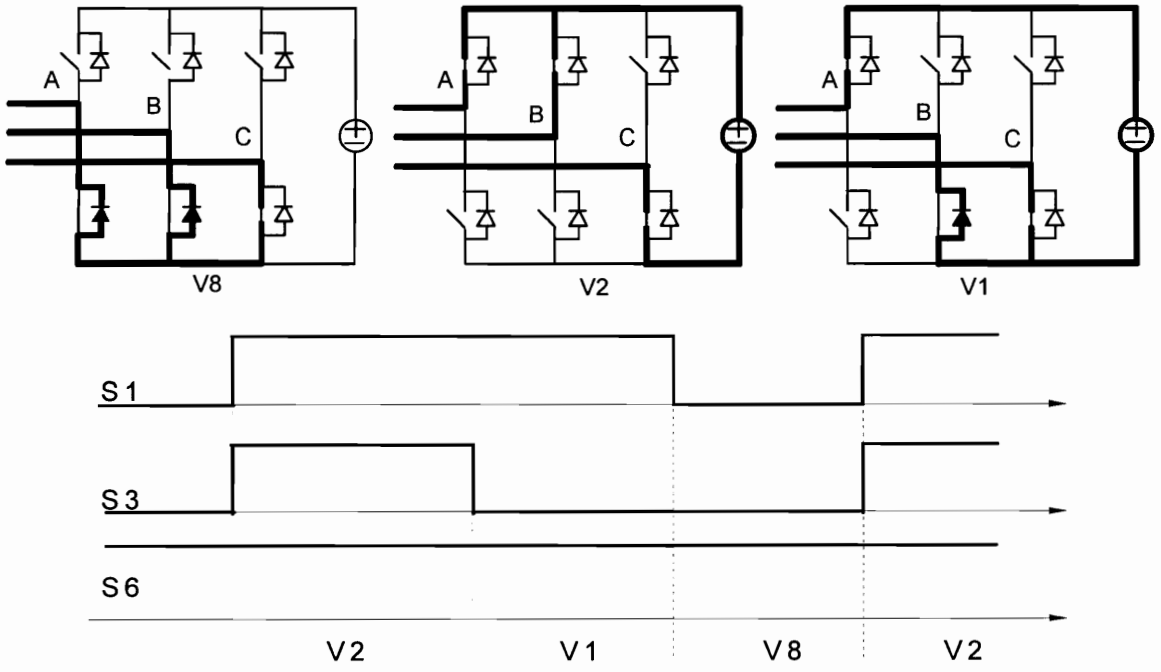


(b). Highest current in phase C: switching sequence is V8--V1--V2

Figure 3.3 **SVM scheme in rectifier mode(in Sector I).** The switch turn-on instants in three-phase are synchronized, and the switch carrying the highest current is not switched. The diodes at one side are turned off simultaneously.



(a). Highest current in phase A: switching sequence is V7--V1--V2--V7--



(b). Highest current in phase C: switching sequence is V8--V2--V1--V8

Figure 3.4 **SVM scheme in inverter mode (in Sector I).** Switch turn-on instants are synchronized, and the switch carrying the highest current is not switched. The conducting diodes at one side are turned off simultaneously.

According to the analysis and experimental results in [E37], the modulation schemes in Figs. 3.3 and 3.4 are optimum with regard to high frequency spectrum and switching loss. In these schemes, the conducting diodes on one side of the bridge are always turned off at the same time. If we only need to investigate the active switch turn-on process, i.e. the commutation from diodes to switches, as happened in zero-voltage turn-on commutation, the three top diodes behave like one "generalized" diode, and the three bottom diodes behave like another generalized diode, since the commutations of all diodes in one group, the top group or the bottom group, are synchronized. Similarly, the three top switches and three bottom switches can also be considered as two "generalized" switches. As a result, with regard to the turn-on process, a three-phase converter can be viewed as two "generalized" PWM cells which are shown in Fig. 3.5, and the soft-switching circuit can be simplified accordingly.

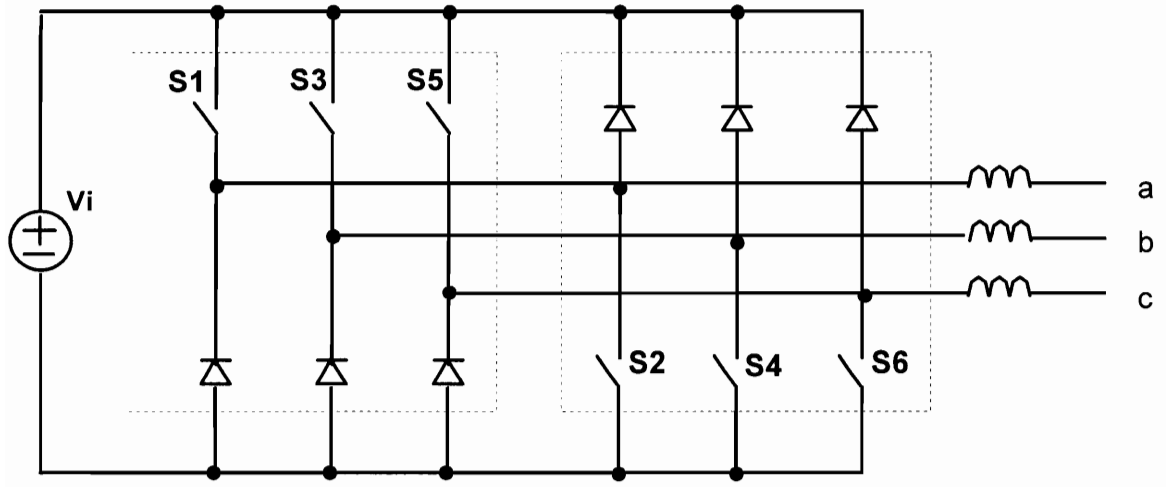
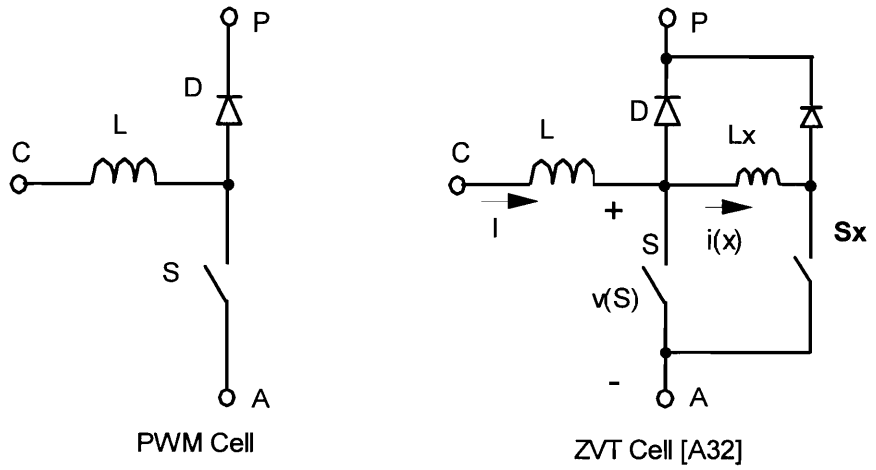


Figure 3.5 **Generalized PWM cells in a three-phase VSC**. The switches and diodes are divided into two groups, each having three switches and three diodes. Each group behaves like a PWM switch in the commutation from diodes to switches with the synchronized turn-on modulation schemes.

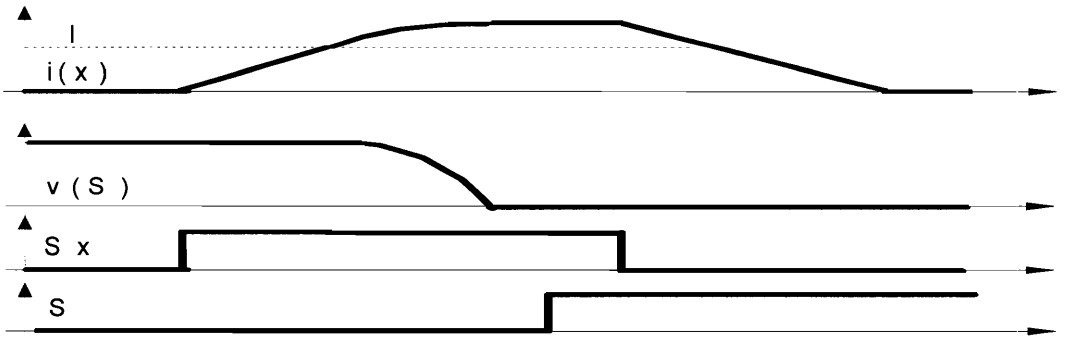
3.3 NOVEL THREE-PHASE ZVT BOOST RECTIFIER/ VOLTAGE SOURCE INVERTER

3.3.1 TOPOLOGY DEVELOPMENT

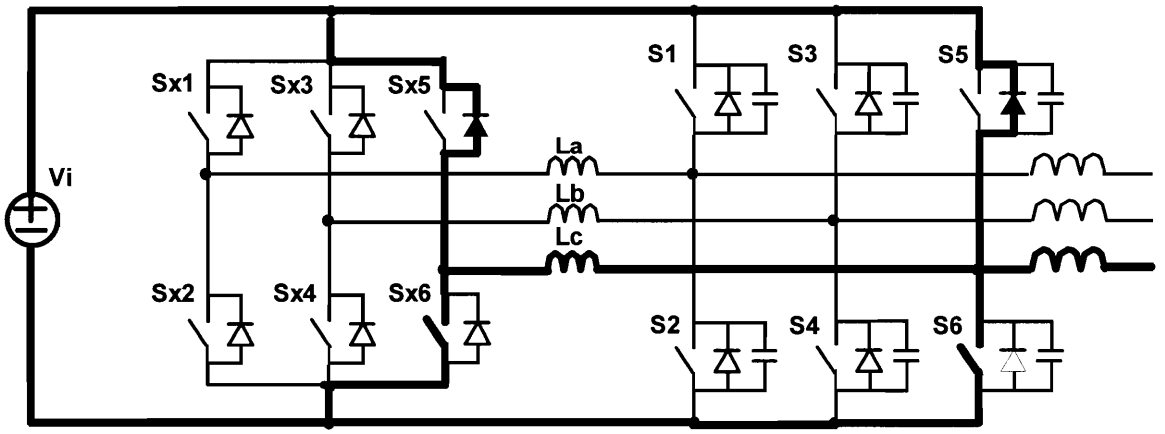
MOSFET and IGBT devices are widely used in low to medium power end of three-phase converters. MOSFETs and low power IGBTs have fast switching characteristics, and therefore have low turn-off losses. Zero-voltage switching is preferred in many applications due to its ability to eliminate switch turn-on loss and diode reverse recovery, and to reduce switch turn-off loss and phase voltage dv/dt through the use of capacitor snubbers. The zero-voltage transition (ZVT) techniques in [A32] [A33] use an auxiliary switch to shape the main switch voltage to zero in the turn-on transition, and effectively combine the advantages of zero-voltage switching and those of PWM control. The PWM cell and ZVT cell are shown in Fig. 3.6(a). The ZVT cell is actually two PWM cells, with the auxiliary PWM cell working in the discontinuous conduction mode (DCM). The auxiliary PWM cell is actuated only for a short duration before the main switch turn-on, to create the zero-voltage switching condition. Except in the turn-on commutation, the auxiliary PWM cell is inactive, and the ZVT cell operates as a PWM cell. The key waveforms of the ZVT cell during main switch turn-on commutation are shown in Fig. 3.6(b), which clearly demonstrates how the auxiliary circuit shapes the main switch voltage to zero. An intuitive ZVT three-phase converter can be obtained by changing the PWM cells in a three-phase PWM converter into ZVT cells. The resultant soft-switching topology is shown in 3.6(c). This topology is based on the basic ZVT cell in [A32], and has also a similar characteristics as the ZVT dc-dc converters presented in [A32]. A similar topology can also be developed using the modified ZVT topology in [A33], which utilizes a coupled inductor in the auxiliary circuit to reduce the auxiliary switch current stress, and requires that the control timing of the auxiliary circuit should be adjusted according to the main inductor current [B28].



(a). PWM cell and basic ZVT cell proposed in [A32]



(b). Key waveforms of ZVT cell operation



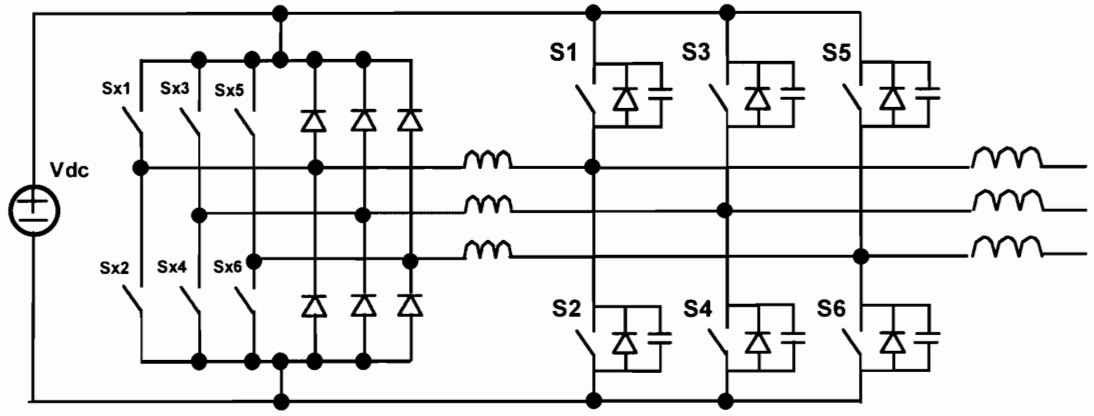
(c). ZVT Three-phase voltage source inverter

Figure 3.6 **An intuitive ZVT three-phase voltage source inverter.** ZVT mechanism is applied to each PWM cell, and the main switches are turned on with zero-voltage. The converter can be controlled with any modulation scheme.

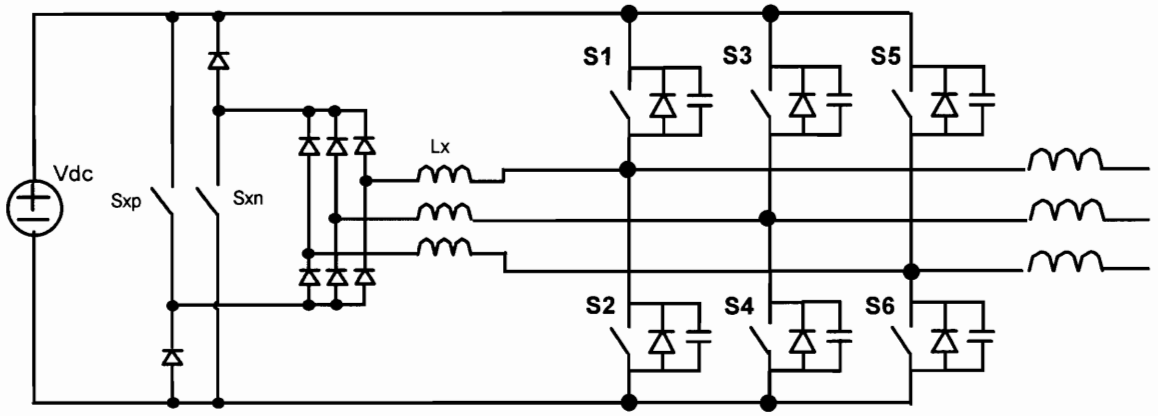
Compared with other soft-switching techniques, ZVT is a good candidate for low to medium power end of high-power applications, because it is relatively simple, and achieves soft turn-on of the main switches and soft turn-off of the main diodes without increasing the device voltage/current stresses. However, the basic topology shown in Fig. 3.6(b) requires six auxiliary switches, and is not cost-effective. Through the modulation schemes with the switch turn-on synchronization in the last section, the auxiliary circuit can be simplified. Fig. 3.7 illustrates the topology derivation process. In Fig. 3.7(a), the original ZVT topology of Fig. 3.6(b) is redrawn in another form without changing the real connection. Due to the main switch turn-on synchronization, the three auxiliary switches Sx1, Sx3, and Sx5 can be replaced by one auxiliary switch Sxp, while the other three auxiliary switches Sx2, Sx4, and Sx6 can be replaced by another auxiliary switch Sxn. The resultant topology is shown in Fig. 3.7(b). The relationship of the auxiliary switch control timing in these two topologies is also shown in Fig. 3.7(c). This simplification process is equivalent to apply the ZVT concept to the generalized PWM cell discussed in Fig. 3.5, as is shown in Fig. 3.7(d). Three resonant inductors are used for each generalized PWM cell in Fig. 3.7(d), since there are three main currents. The function of the diodes in series with the resonant inductors is to prevent the three phases from short-circuit through the resonant inductors. If the resonant inductors are shared between the two generalized PWM cells, the topology shown in Fig. 3.7(d) is directly simplified into the topology shown in Fig. 3.7(b). This illustrates how the generalized PWM cell concept can be used to derive simple ZVT topologies in three-phase converters.

The operation of the ZVT topology in Fig. 3.7(b) in rectifier mode can be explained with the example of the turn-on process in Fig. 3.3(a), i.e. the commutation from D4, D6 to S3, S5. The commutation process is shown in Fig. 3.8(a), and key waveforms are shown in Fig. 3.8(b).

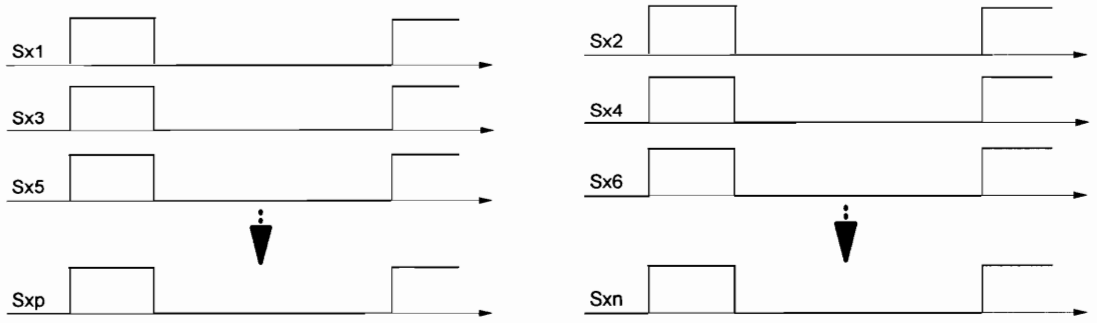
Charging Stage [t0, t2] Before S3 and S5 are turned on, Sxp is turned on first at t0. Then the resonant inductors in phase B and phase C start to be charged, and i_{bx} and i_{cx}



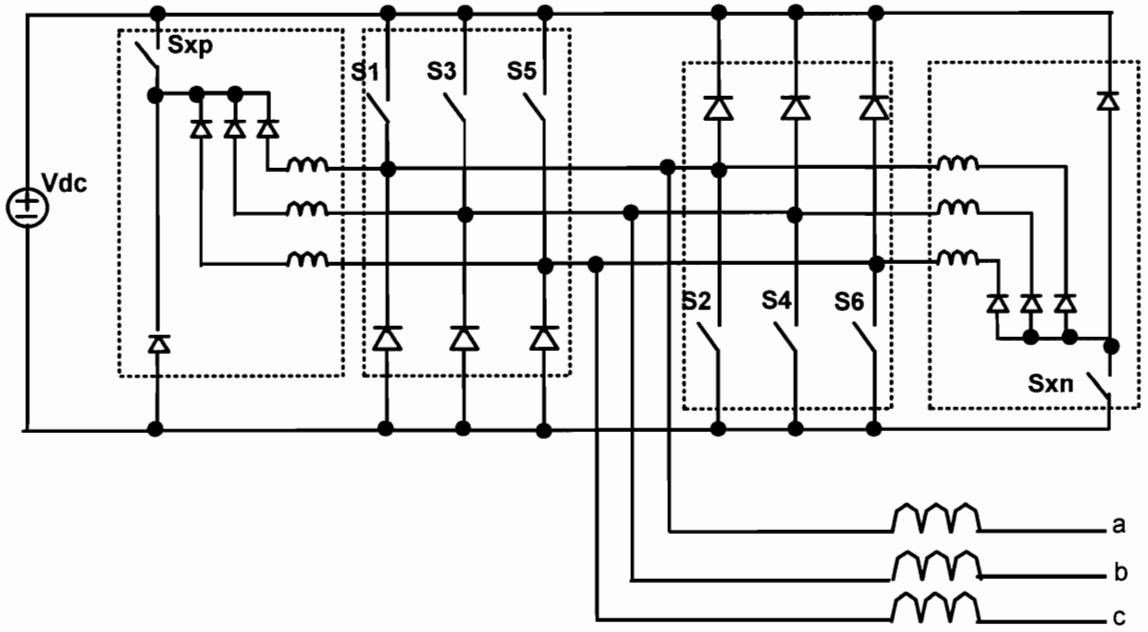
(a). Rearrangement of Fig. 3.6(b)



(b). Simplification of (a)



(c). Control timing of auxiliary switches



(d). Applying ZVT cells to the generalized PWM cells

Figure 3.7 **Simplification of three-phase ZVT topology**. The auxiliary switches for three main switches at one side can be combined into one due to the synchronization of main switch turn-on. This is equivalent to applying the ZVT mechanism to each generalized PWM cell, as is shown in (d).

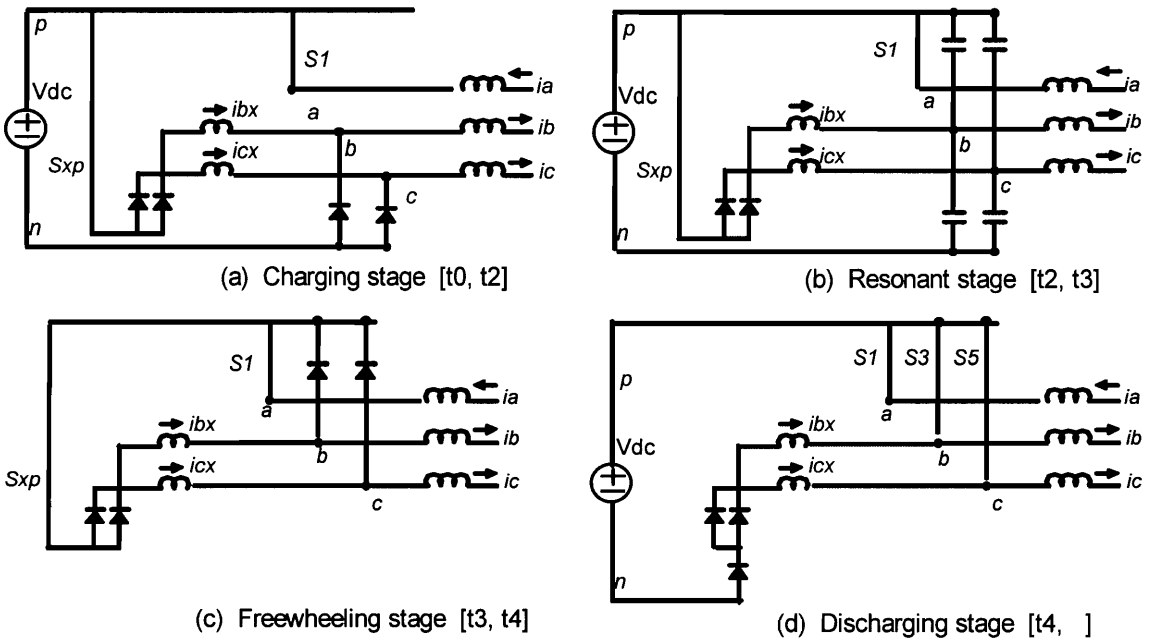
start to increase linearly. i_{ax} remains at zero, since no voltage is available to charge the resonant inductor in Phase A.

Resonant Stage [t2, t3] When a resonant current reaches the same value as the corresponding phase current, the diode in that phase is turned off naturally. Then the resonant inductor starts to resonate with the snubber capacitance in that phase. The starting time of the resonant stage for each phase depends on the phase current. In Fig. 3.8, Phase C starts to resonate at t1, while Phase B starts resonance at t2.

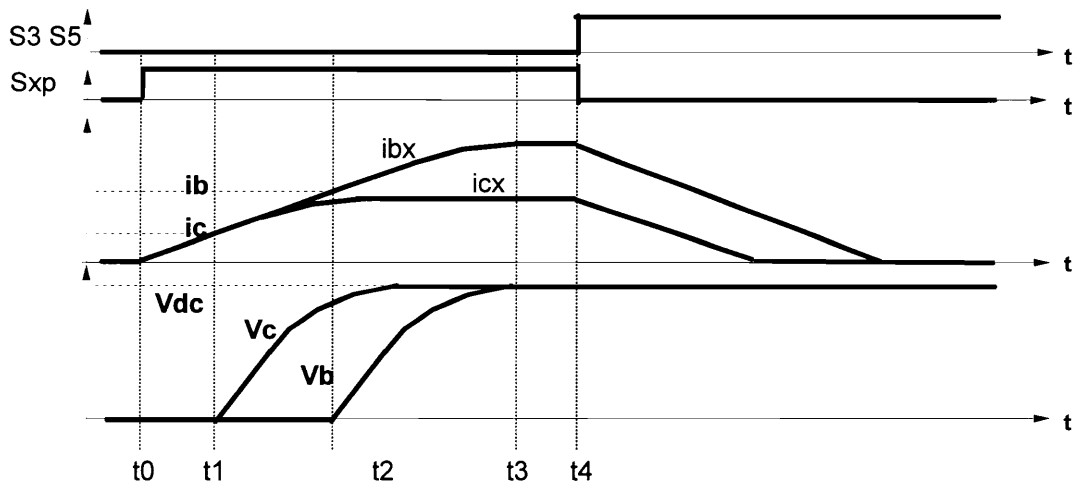
Freewheeling Stage [t3, t4] In the resonant stage, the node voltages V_b and V_c increase towards positive dc rail in a resonant fashion, and the voltages across S3 and S5 decrease gradually. When a node voltage reaches the positive dc rail voltage, the corresponding incoming switch voltage becomes zero, and its anti-parallel diode starts to conduct, clamping the switch voltage at practically zero. After t3, the voltages across S3 and S5 are both zero, and the three phase currents freewheel through the auxiliary circuit. The zero-voltage turn-on condition is created.

Discharge Stage [t4,] During the freewheeling stage, S3 and S5 can be turned on with zero voltage at any time, which is denoted as t4. Sxp is also turned off at the same time, so the resonant inductors start to be discharged. Since the outgoing diodes are turned off earlier, and the switch voltages are already reduced to zero, the switch turn-on loss and diode reverse recovery are eliminated. Because the energy in the snubber capacitors is completely recovered and delivered to the output in this stage, relatively large capacitors can be used to reduce the switch turn-off loss. When an auxiliary current is discharged to zero, the auxiliary diode in that phase is turned off naturally. After both auxiliary currents are discharged to zero, the auxiliary circuit is disconnected from the main power stage functionally, and the converter resumes its PWM operation.

In rectifier mode, zero-voltage turn-on can be achieved with the help of the auxiliary circuit, while PWM control, minimum voltage/current stress, and circulating energy of a PWM converter are still kept. A significant efficiency improvement can be



(a). Operating stages

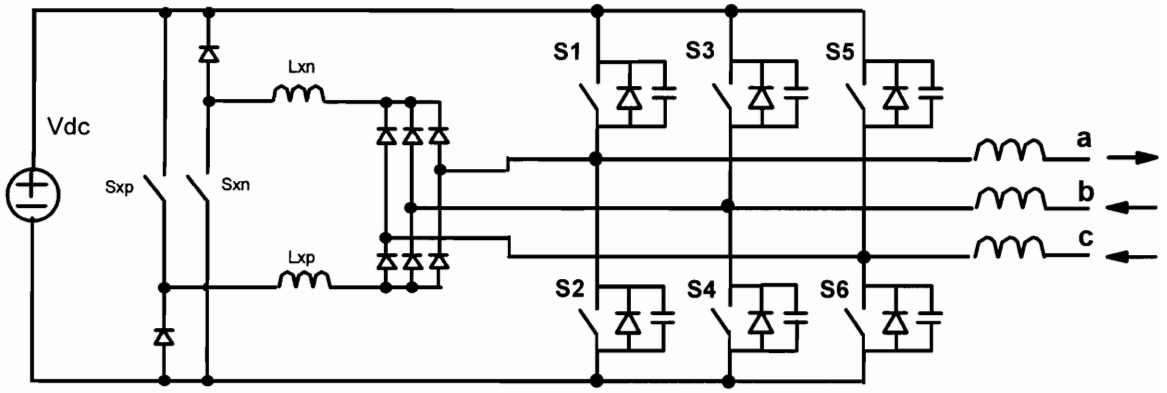


(b). Key waveforms

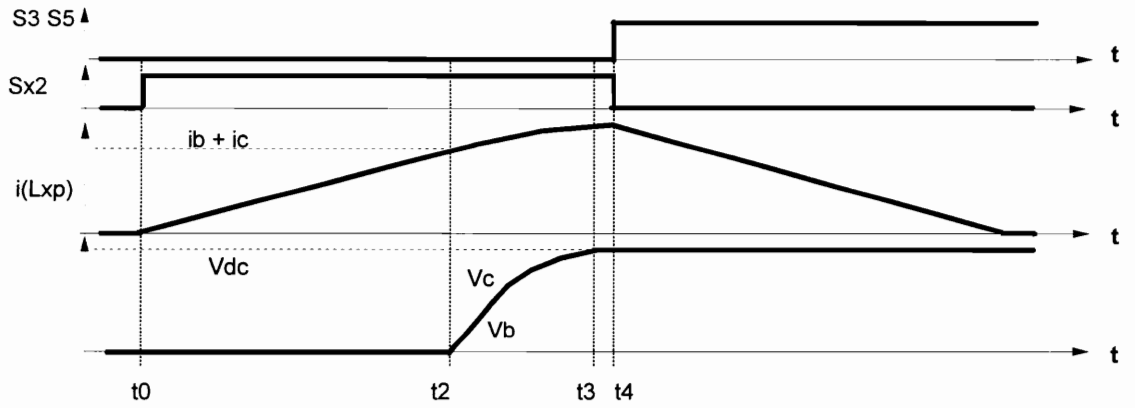
Figure 3.8 **Turn-on commutation for Fig. 3.7(b).** There are no resonant inductor overcharging and extra main switch turn-off. The switch turn-on loss and diode reverse recovery are eliminated. The resonant inductors cannot be discharged in inverter mode operation.

expected. However, in inverter mode, the switch turn-on transition starts from a zero vector where two diodes and one switch at the same side are conducting. Then this topology cannot discharge the resonant inductor for the phase which has an active switch conducting. For example, if S1, D3 and D5 are conducting, and D3 and D5 are to be commutated, Sx1 should be turned on to divert currents out of D3 and D5. However, the resonant inductor for Phase A will be charged also, and can not be discharged even after Sx1 is turned off. To discharge the resonant inductors, two auxiliary power supplies can be used in the auxiliary circuit, as is discussed in [B57]. However, the need of commutation power supplies is cumbersome and impractical in most applications.

The topology shown in Fig. 3.7(b) can be further simplified by shifting the resonant inductors into the auxiliary diode bridge, as is shown in Fig. 3.9(a). A resonant inductor is used for all switches at one side: Lxp for three top switches, and Lxn for three bottom switches. The zero-voltage turn-on process in rectifier mode is similar to that shown in Fig. 3.7(b), except that now the switch voltages are synchronized in the resonant stage, as is shown by the waveforms in Fig. 3.9(b). Still, this topology cannot be used in inverter mode, because the resonant inductors cannot be discharged. However, this topology can be further simplified. The two resonant inductors can be combined into one, and the two auxiliary switches can be rearranged to fully control the resonant inductor. The resultant topology is shown in Fig. 3.10. The resonant inductor can now be charged when the two auxiliary switches are turned on if the main bridge is not in a zero vector, and is discharged by the dc link voltage when the auxiliary switches are turned off. As a result, this topology can work in both rectifier and inverter modes, and is worthy of further investigation.



(a) Shifting resonant inductors into the auxiliary bridge



(b). Key waveforms of turn-on commutation in (a).

Figure 3.9 **Another simple ZVT topology for three-phase boost rectifiers.** The resonant inductors are shifted into the auxiliary diode bridge, so that the incoming switch voltages in the resonant stage become synchronized. The operation of this topology is similar to that shown Fig. 3.8(a). The resonant inductors still can not be discharged in inverter mode operation.

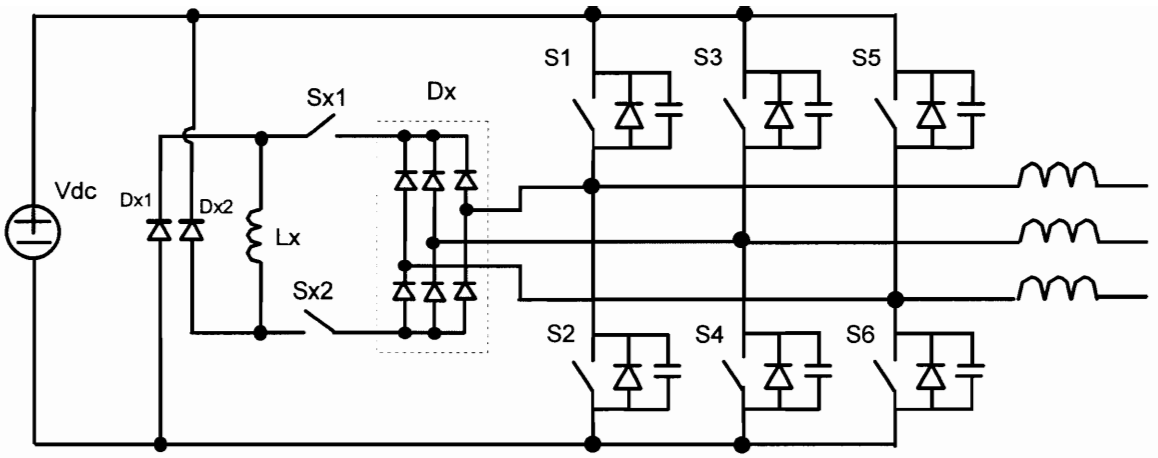


Figure 3.10 **A practical soft-switching three-phase boost rectifier/voltage source inverter**. The resonant inductors are shifted further, and are combined into one. The auxiliary switches can fully control the charging and discharging of the resonant inductor. This topology can work as both a rectifier and an inverter.

3.3.2 OPERATION OF THREE-PHASE BI-DIRECTIONAL ZVT BOOST RECTIFIER/ VOLTAGE SOURCE INVERTER

This ZVT topology consists of a standard PWM converter and a ZVT auxiliary circuit to help the main switch turn on. The ZVT auxiliary circuit consists of a resonant inductor Lx, two auxiliary switches Sx1 and Sx2, an auxiliary diode bridge Dx, and two clamp diodes Dx1 and Dx2. The two auxiliary switches are unidirectional and can be implemented as MOSFETs. The ZVT converter operates basically in the same way as its PWM counterpart, and the auxiliary circuit is active only during a short period prior to main switch turn-on. Because all the auxiliary devices are placed out of the main power path, the conduction loss and voltage/current stresses of the main switches, as well as the circulating energy, are all about the same as in its conventional PWM counterpart. On the other hand, because the auxiliary circuit is controlled to divert currents from the outgoing diodes and discharge the output capacitance of the incoming switches prior to their turn-on instants, the turn-on loss is reduced significantly, so high efficiency and low EMI emissions are achieved. With the SVM schemes shown in Figs. 3.3 and 3.4, the operation of the ZVT circuit can be exemplified by the following two cases: the first is typical in rectifier operation, and the second is typical in inverter operation.

1. From D1, D4 and D6 to D1, S3 and S5

The whole commutation process has four operation stages, which are shown in Fig. 3.11. Notice that switch S1 is kept on during the whole commutation. The turn-on of S1 does not cause any power loss, because D1 is already on.

(1) Charging Stage [t0, t1] Auxiliary switches Sx1 and Sx2 are turned on at t0, so the resonant inductor Lx is charged by the dc-link voltage $V_{dc,}$ and its current increases linearly with the rate of V_{dc} / L_x. At the same time, the currents in D4 and D6 are diverted into the auxiliary circuit.

(2) Resonant Stage [t1, t2] When the current i_x reaches *ia* at t1, diodes D4 and D6

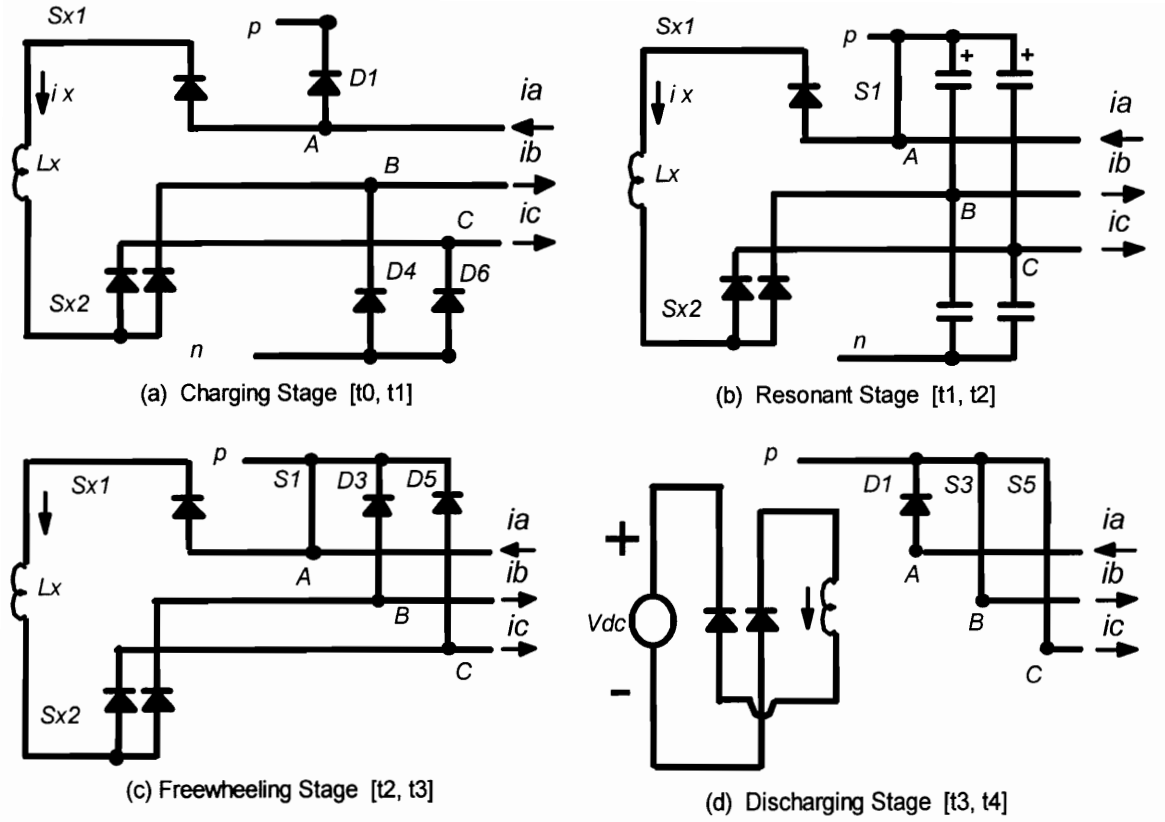


Figure 3.11 **A ZVT commutation in rectifier mode.** There are no resonant inductor overcharging and extra main switch turn-off.

turn off naturally, and Lx starts to resonate with the node capacitance of Phases B and Phase C. The voltages of nodes B and C increase towards the positive DC rail in a resonant manner. The auxiliary diode bridge forces the voltages across S3 and S5 to decrease at the same rate, because the resonant current always choose the lowest voltage path.

(3) Freewheeling Stage [t2, t3] When the voltages of nodes B and C reach the positive DC rail voltage at t2, the anti-parallel diodes D3 and D5 of S3 and S5 start conducting, so the current in Lx starts freewheeling through S1, D3, and D5. Because of the clamp action of D3 and D5, the switch voltages of S3 and S5 are kept at zero during this stage, creating the zero-voltage switching condition for S3 and S5.

(4) Discharging Stage [t3, t4] At t3, S3 and S5 are turned on with zero voltage. At the same time, Sx1 and Sx2 can be turned off, and the commutation energy in Lx is fed into V_{dc} through Dx1 and Dx2. Meanwhile, Lx is discharged by V_{dc}. At t4, i_x becomes zero, so Dx1 and Dx2 are turned off naturally, and the ZVT commutation is completed.

After t4, the auxiliary circuit keeps inactive, and the converter assumes its PWM operation until the next ZVT commutation.

The key waveforms of the commutation process are drawn in Fig. 3.12. Notice that no overlap between switch voltages and switch currents exists, so the turn-on losses are eliminated completely. Also, the resonant stage always starts from the time when i_x reaches the current in Phase A, and the control timing does not affect the peak of i_x. If the control timing is set for maximum input currents, then ZVT can be achieved under any load condition.

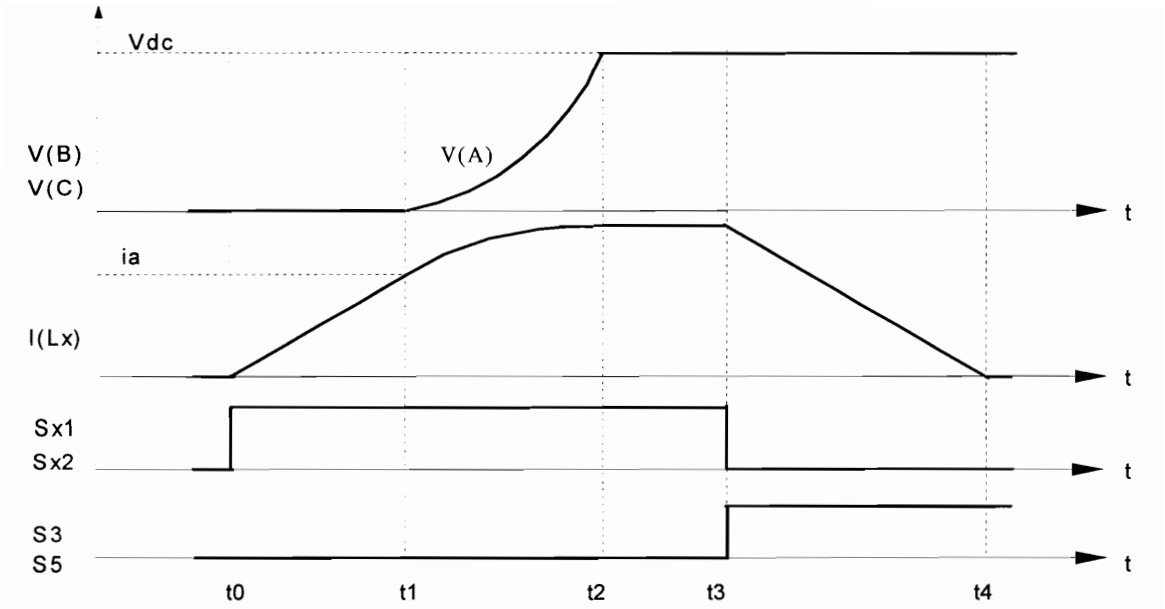


Figure 3.12 **Waveforms of ZVT commutation in rectifier mode.** Diode reverse recovery and switch turn-on loss are eliminated.

2. From S1, D3, and D5 into S1, S4, and S6

This is the typical turn-on commutation in inverter mode. At the beginning of the commutation, S1 is turned off first. The large current in phase A causes the voltage of node A to decrease rapidly, and D2 starts conduction soon. So the commutation is basically from D2, D3, and D5 to S1, S4, and S6. The commutation process consists of four stages, which are shown in Fig. 3.13.

(1) Charging stage [t0, t1] Prior to the turn-on of the main switches, Sx1 and Sx2 are turned on at t0. Then the current in Lx starts to increase, and the currents in the three outgoing diodes are reduced gradually.

(2) Resonant stage [t1, t2] When the current i_x reaches *ia*, the three outgoing diodes are turned off softly, and Lx starts to resonate with the node capacitance of nodes A, B, and C. The three node voltages resonate towards their opposite DC rails, and switch voltages decrease gradually.

(3) Freewheeling stage [t2, t3] When the three node voltages become equal (in this case 2/3 of V_o) at t2, the auxiliary diode bridge is shorted, and the resonance is stopped. Then i_x freewheels through Sx1, Sx2, and the shorted auxiliary diode bridge. The voltage across S1 is reduced to Vo/3, and the voltages across S4 and S6 are both reduced to 2Vo/3.

(4) Discharging stage [t3, t4] After t2, all diodes in the main bridge are off, and the main switch voltages are constant. Incoming switches S1, S4, and S6 are turned on with reduced voltages at t3. At the same time, Sx1 and Sx2 are turned off, so Lx is discharged by V_o through Dx1 and Dx2. When i_x is discharged to zero at t4, Dx1 and Dx2 are turned off naturally, and the commutation is completed. The auxiliary circuit keeps inactive until the turn-on commutation in the next switching cycle.

The key waveforms of this commutation are drawn in Fig. 3.14. Because the diode reverse recovery is eliminated and the remaining capacitive energy at turn-on is reduced to about 1/3 compared with the hard-switching operation, the turn-on losses are

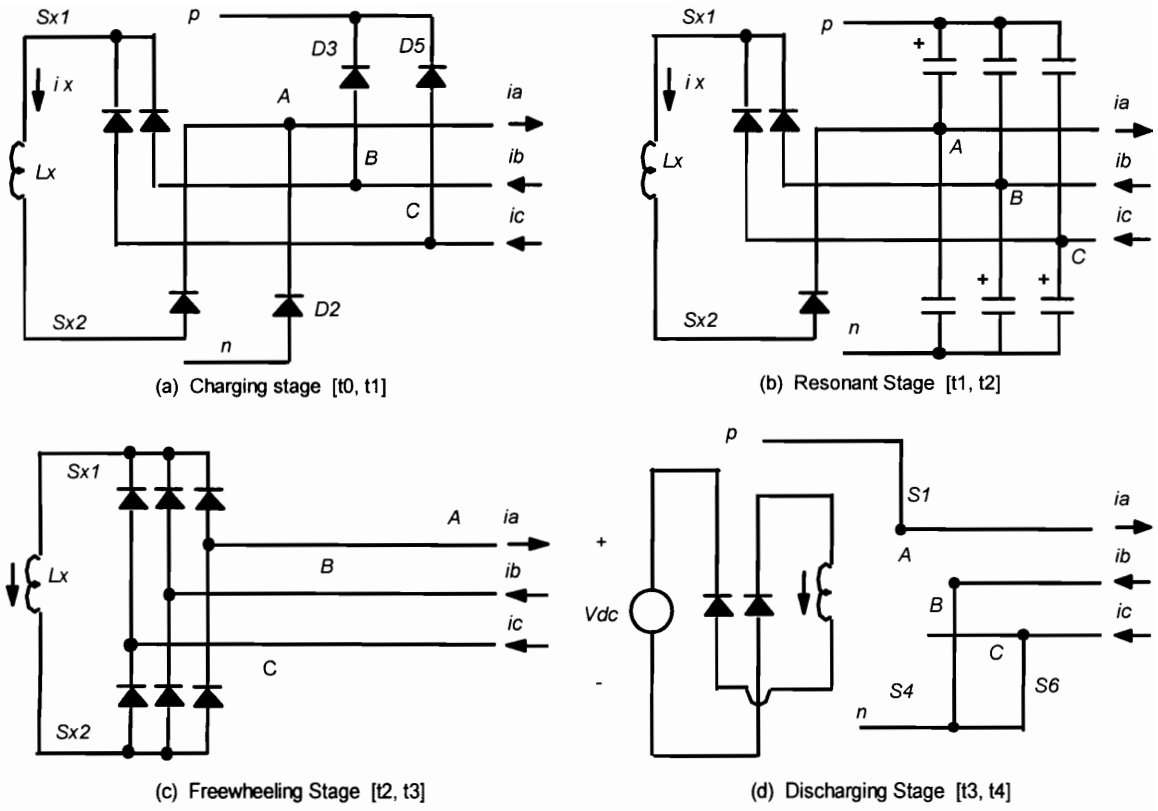


Figure 3.13 **A turn-on commutation in inverter mode.** Before the commutation starts, S1 is turned off to provide voltage to the commutation circuit, which causes extra main switch turn-off loss. There is no resonant inductor overcharging.

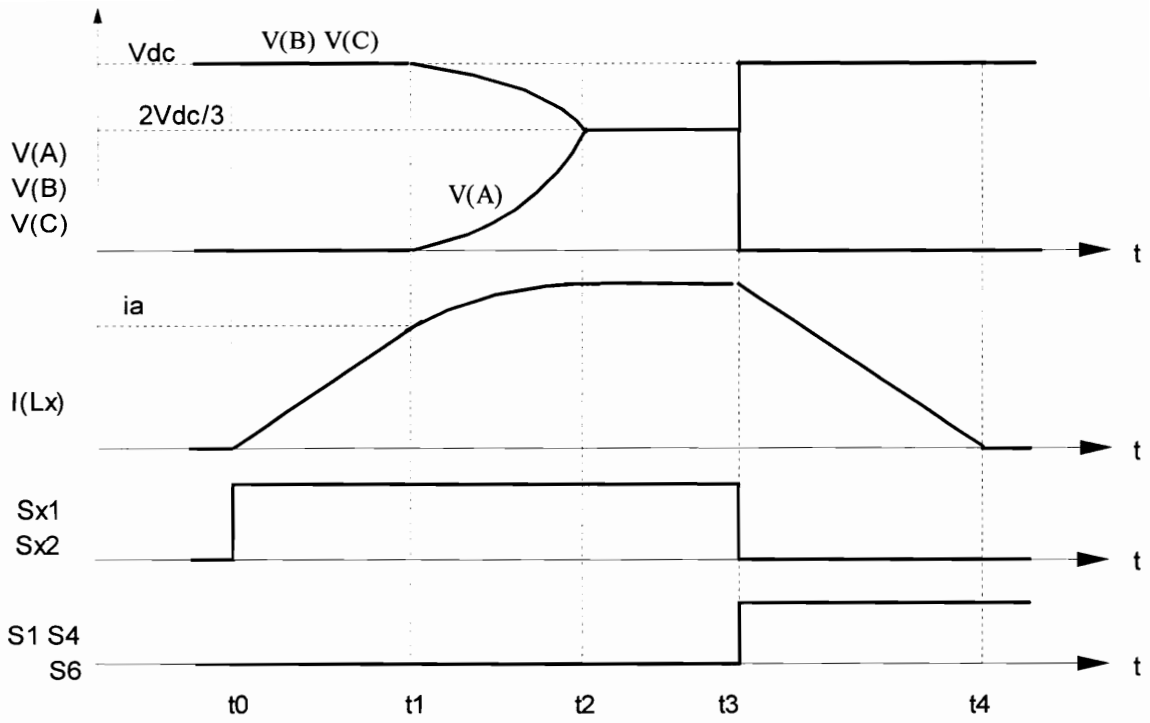


Figure 3.14 **Key waveforms in turn-on commutation in inverter mode**. The diode reverse recovery of the main power stage is eliminated, but the switch turn-on voltage cannot be reduced to zero.

significantly reduced, so high efficiency operation can still be achieved. However, the capacitance of the snubber capacitor, used to reduce switch turn-off loss, should be small to avoid high turn-on loss. Another important issue to notice is that three diodes in the auxiliary diode bridge are turned off abruptly when the main switches are turned on, and thus suffer from reverse recovery. This problem can be alleviated by the use of saturable inductors between the main bridge and auxiliary bridge, as is shown in Fig. 3.15.

From the above discussion, one can note that the current in Lx is limited to maximum phase current automatically in both rectifier mode and inverter mode operations, and the main switches can be turned on any time during the freewheeling stage. This possibility gives much freedom to the control timing of the ZVT circuit, and the soft switching function can be achieved with very large load and input ranges, if the control timing is set properly according to maximum phase current.

Table 3.1 summarizes the comparison of major features of several ZVT topologies, in which the topology of Fig. 3.10 is referred as Scheme I, and Scheme II is a new soft-switching topology to be discussed in Section 3.4. The overcharging of resonant inductors in [B29 - B31] is no longer required in the new topology, so it has a significantly lower main switch turn-off loss. Because the current in the auxiliary switches has lower peak and lasts a shorter time, the conduction loss in auxiliary circuit is also much lower, especially in light load condition. Even if in heavy load, the average current of auxiliary switches is just about 1/8 and the rms current about 1/4 of the corresponding value in [B29]. If the same switch devices were used, the auxiliary switch conduction loss in the proposed converter would be about 1/4 of that in [B42]. Moreover, the timing of the ZVT circuit is not critical and is similar to its ZVT DC/DC converter counterpart, while complex and accurate ZVT timing is required in [B29, B42] because the timing directly determines the auxiliary current peak and is critical to achieving soft switching.

It can be seen that the performance of this topology, as well as the ones in Figs. 3.8(b) and 3.10(a), is better in rectifier mode than in inverter mode. This feature is

Table 3.1 Feature Comparison of Soft-Switching Three-Phase Inverters

(a). In rectifier mode

	PWM	De Doncker's	Lai's	Vlatko's	Scheme I	Scheme II
Main Switch Turn-On VA	$V_{dc}I_{pk}$	0	0	0	0	$V_{dc}I_{pk}$ / 20
Main Switch Turn-Off VA	$V_{dc}I_{pk}$	~ $1.2V_{dc}I_{pk}$	~ $4V_{dc}I_{pk}$	~ $4V_{dc}I_{pk}$	$V_{dc}I_{pk}$	$V_{dc}I_{pk}$
No. of Aux. Switches	N/A	6	3~6	1	2	2
Aux. Switch Voltage stress	N/A	V_{dc} / 2	V_{dc}	V_{dc}	V_{dc}	V_{dc} / 2
Aux. Switch Peak Current	N/A	$1.1I_{pk}$	$2I_{pk}$	$2I_{pk}$	I_{pk}	I_{pk}
Aux. Switch Turn-Off Current	N/A	0	0	~0	I_{pk}	0
Soft Switching Timing	N/A	Critical	Critical	Critical	Not Critical	Not Critical

(b). In inverter mode

	PWM	De Doncker's	Lai's	Vlatko's	Scheme I	Scheme II
Main Switch Turn-On VA	> $V_{dc}I_{pk}$	0	0	0	~ 0	~ $V_{dc}I_{pk}$ / 10
Main Switch Turn-Off VA	> $V_{dc}I_{pk}$	~ $1.2V_{dc}I_{pk}$	~ $4V_{dc}I_{pk}$	~ $4V_{dc}I_{pk}$	$2V_{dc}I_{pk}$	$2V_{dc}I_{pk}$
No. of Aux. Switches	N/A	6	3~6	1	2	2
Aux. Switch Voltage stress	N/A	V_{dc} / 2	V_{dc}	V_{dc}	V_{dc}	V_{dc} / 2
Aux. Switch Peak Current	N/A	$1.1I_{pk}$	$2I_{pk}$	$2I_{pk}$	I_{pk}	I_{pk}
Aux. Switch Turn-Off Current	N/A	0	0	~0	I_{pk}	I_{pk}
Soft Switching Timing	N/A	Critical	Critical	Critical	Not Critical	Not Critical

common to other simplified ac-side soft-switching schemes also, since the auxiliary circuit cannot operate when the main power stage is in zero vectors. Therefore, These topologies are very suitable to be used as the front-end PFC converters for motor drives, where the converter works as a rectifier most of the time, and the current rating in inverter mode can be lower than in rectifier mode.

The modified ZVT technique with a coupled inductor in [A33, A34] can also be used to further reduce the power loss of the auxiliary circuit. Such a topology is proposed in [B51] for the topology in Fig. 3.10(b). A similar technique can be easily obtained with the rectifier topology of Fig. 3.10(a), which has only half the power loss in the auxiliary circuit as in Fig. 3.10(b). However, the topologies with coupled inductors require complex timing to achieve soft switching, which might not be practical for high switching frequency applications.

3.3.3 AUXILIARY CIRCUIT DESIGN AND EXPERIMENTAL RESULTS

The main power stage and control design of the ZVT converter are basically the same as in a conventional PWM converter and need not be discussed in detail.

The inductance of Lx is very important for the ZVT operation. A larger inductance helps to eliminate the diode reverse recovery problem completely, but results in more conduction loss in the auxiliary circuit and more duty cycle loss. Usually, the inductance can be determined by setting the charging stage duration to a little more than three times the diode reverse recovery time at full load, or by limiting *di/dt* in the charging stage to no more than a certain preset value, e. g. around 100 A/uS.

In most cases, Power MOSFET devices are used for the auxiliary switches. To reduce the conduction loss, the auxiliary switches should be turned off immediately at the end of the resonant stage at heavy load. The power loss in the auxiliary circuit is about the same in rectifier mode as in inverter mode, so only the ZVT operation in rectifier

mode is analyzed here. With an analysis similar to that in a boost dc-dc converter [A32], the peak of i_x can be found to be:

$$I_x = I_m + \frac{V_o}{Z_c}, \tag{3.1}$$

where $Z_c = \sqrt{Lx/(4C_s)}$. The rms current of the auxiliary switches is:

$$I_{aux} = \sqrt{[\frac{1}{3}\frac{{I_m}^3 L_x}{V_s} + 8V_o I_m C_s + (\pi - 1)\frac{{V_o}^2 C_s}{Z_c}]f_s}, \tag{3.2}$$

The average current of the diode in the auxiliary diode bridge is:

$$I_D = [\frac{{I_m}^2 L_x}{V_o} + (\pi + 2)I_m\sqrt{L_x C_s} + 6V_o C_s]\frac{f_s}{3}, \tag{3.3}$$

The average current of Dx1 and Dx2 is:

$$I_{Dx} = (\frac{{I_m}^2 L_x}{2V_o} + 2I_m\sqrt{L_x C_s} + 2V_o C_s)f_s. \tag{3.4}$$

In the above equations, I_m is the maximum phase current, Cs is the capacitance across a switch, and f_s is the switching frequency of the converter.

The voltage rating of all the power semiconductors in the auxiliary circuit should be V_{dc}.

A ZVT converter with the proposed topology has been built with IGBT modules. The specification is: input voltage 230 V~460 V, output voltage 750 V, output power 10 kW, and switching frequency 50 kHz. The power stage parameters are shown in Fig. 3.15. In the circuit, Dx3 and Dx4 are used to clamp the auxiliary switch voltages at their turn-off instants; otherwise the stray inductance of power leads may cause high voltage spikes to Sx1 and Sx2. The saturable inductor in series with the 20 uH resonant inductor is implemented as 4 turns on Toshiba Spike Killer SA14-8-4.5, and is used to absorb the resonance between Lx and parasitic capacitance in the ZVT circuit, mainly the junction capacitance of Dx1 and Dx2. Saturable inductors Lsa, Lsb, and Lsc, implemented also on SA14-8-4.5, are used to eliminate the reverse recovery of Dx in inverter mode.

Fig. 3.16 shows the experimental waveforms of the ZVT circuit operation in rectifier mode and in inverter mode. It can be seen that complete zero-voltage switching has been achieved in rectifier mode, so the switch turn-on loss is eliminated completely. The switch turn-on voltages in inverter mode are also reduced. The different operating stages of the ZVT circuit confirm what we analyzed previously, and verify the operation principle of the proposed soft-switching topology.

3.3.4 TOPOLOGY EVALUATION

It is very important to fairly compare the performance of different soft-switching schemes in a wide operating range with similar designs to obtain insight into practical application of soft-switching techniques. Experimental verification of three-phase soft-switching circuits is a laborious work. To compare experimentally the performance of different topologies under different operating conditions is beyond the scope of this work. Instead, switching model simulation with Saber simulating package is used to evaluate the performance of various soft-switching schemes. The effects of soft-switching operation on switching stresses, EMI noise, and circuit reliability are important, but are very difficult to quantify because they directly depend on the circuit implementation details. Instead, the power stage efficiency is used as the major indication of converter performance, because the power dissipation in a converter directly affects the design of power semiconductor devices and heatsink, which in turn determines to a large degree the converter cost and power density. The junction temperature of a power semiconductor device, which is determined by its power loss, also determines its reliability.

To simulate the efficiency performance of a converter, the switching loss of the main switches, and the power loss of the auxiliary circuit, which usually has switches, diodes, and LC components, have to be included in the simulation. Simple power loss models for these components are developed using ideal devices in Saber simulation program, and are used to evaluate different converter topologies. These models can easily

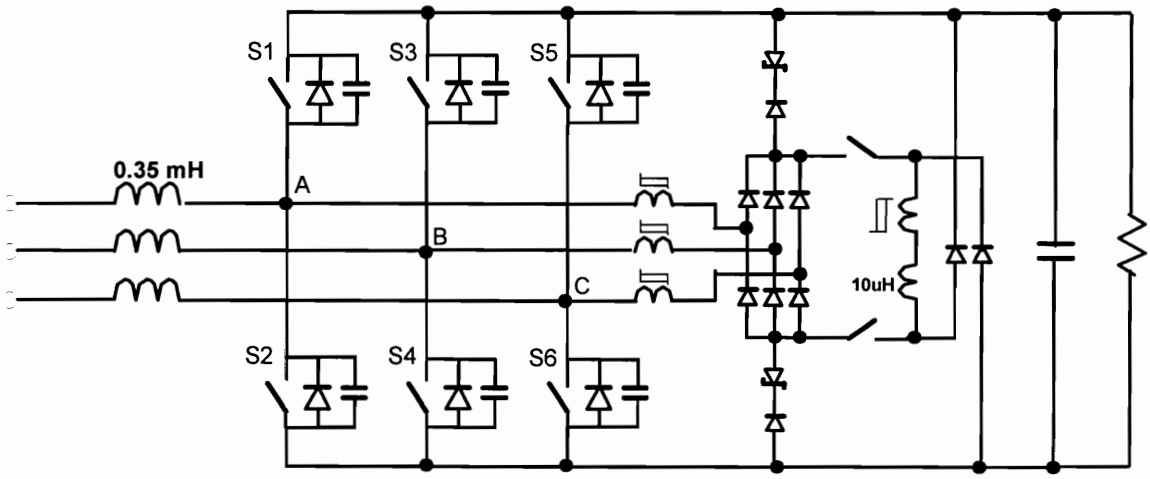
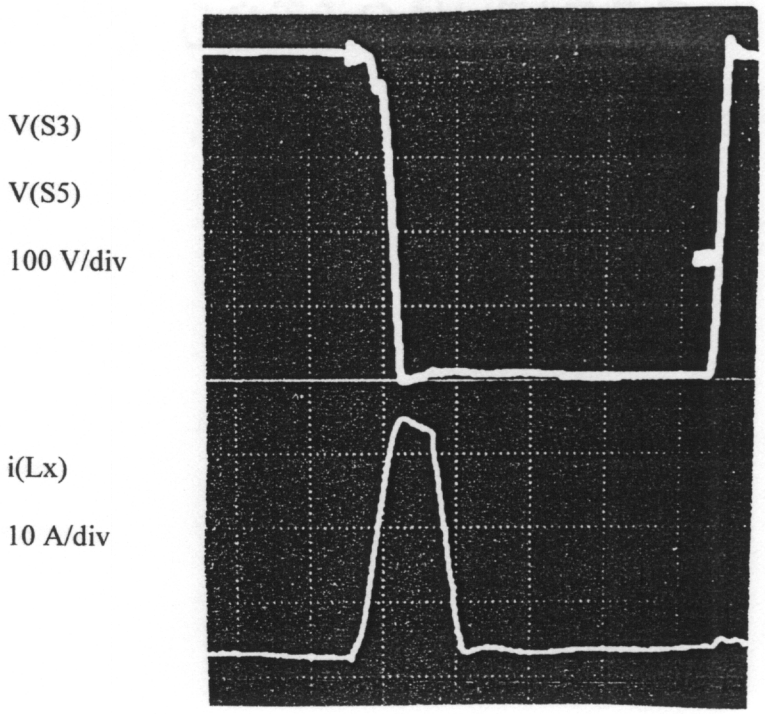
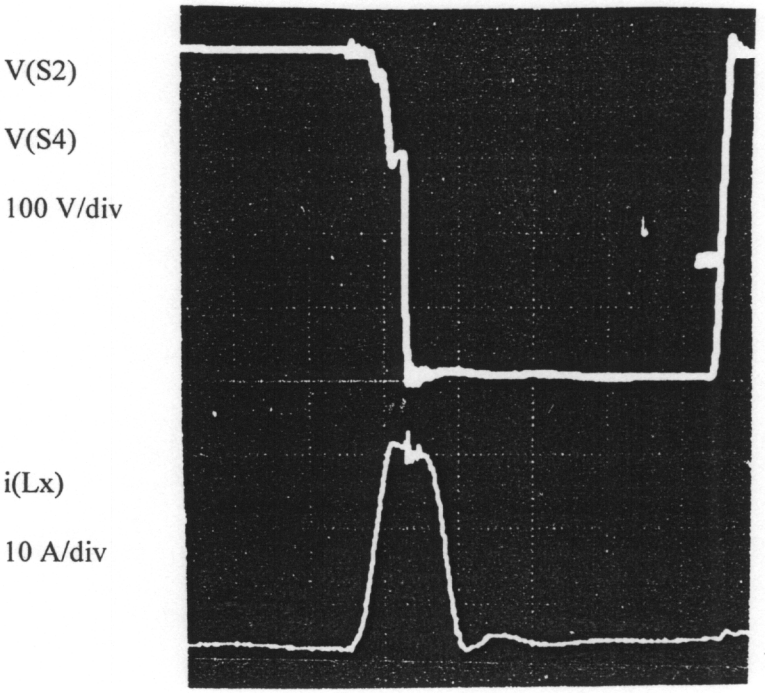


Figure 3.15 **Experimental circuit implementation ("Scheme I", shown as a rectifier).** A saturable inductor is in series with the resonant inductor to absorb the parasitic ringing. The three saturable inductors between the main bridge and the auxiliary diode bridge is to reduce the diode reverse recovery of the auxiliary diode bridge in inverter mode. The zener diodes and their series diodes are to clamp the voltages of the auxiliary switches during their turn-off. S1--S6: 3xCM50DY-24H; Sx1,Sx2: 2xIXTH12N90; Auxiliary Diodes: DESI12-10, Snubber capacitors: 2.2 nF each.



(a). In rectifier mode



(b). In inverter mode

Figure 3.16 **Experimental waveforms of turn-on commutation.** The time scale is 1 uS/div.

incorporate tested or databook switching loss data, are easy to use, and are fast in simulation. The details of these models are described in Appendix A.

The effect of soft-switching schemes depends on the power semiconductor devices used. The efficiency improvement of ZVT topologies is very significant with MOSFETs, because the dominating turn-on loss is eliminated, and the much lower turn-off loss can be effectively reduced with a small snubber capacitor. For IGBTs, which are used increasingly in three-phase converters, however, the improvement with ZVT is not so clear, because the IGBT turn-off loss is no longer negligible, and the effectiveness of snubber capacitors in reducing the turn-off loss is not significant. In this dissertation, two general three-phase applications are used to evaluate different soft-switching topologies. The first uses 600 V, 50 A IGBTs IXGK50N60AU1 with an internal diode. The dc-link voltage is chosen to be 450 V, which can be used for the 230 V ac system. The converter is evaluated in rectifier mode with 90 V rms input phase voltage (low end of 200 V ac system), and up to 10 kW output power. In inverter simulations, the load is assumed to be an RL load, and its resistance is changed according to the power level, while the amplitude of the output currents is kept constant to imitate the motor drive operation in constant-torque region. The load displacement angle is within 30°, so the highest phase current is not switched in the hard-switching SVM scheme. The second design uses a 1200 V, 50 A IGBT module CM50DY-24H (also with internal diodes). The dc-link voltage is chosen to be 900 V, which can be used in the 460 V ac system. The rms input phase voltage in rectifier mode is selected to be 176 V (the low line condition of 380 V ac system). The loss model parameters for the main switches are shown respectively in Table 3.2(a), in which the switching loss data are determined from test results at 125°C case temperature. A detailed procedure to calculate the switching loss model parameters can be found in Appendix A.

The ARCP converter of Fig. 3.1(a) is used as a base design of the auxiliary circuits in different soft-switching topologies. For the 450 V converter, one MOSFET device IXFM40N30 (300 V, 0.08Ω) is used as an auxiliary switch. Other soft-switching

Table 3.2 Switch Loss Model Parameters Used in the Simulation

(a). Main switches

	450 V Converter	900 V Converter
K_{on}	0.25	0.5
K_{off}	0.507	0.447
T_{on} (uS)	0.4758	0.3337
T_{off} (uS)	0.41	0.421
Vs (V)	1.1	1.1
Rs (Ohm)	0.015	0.022
Vd (V)	1.2	1.2
Rd (Ohm)	0.005	0.024

(b). Auxiliary Switches

	450 V converter		900 V converter	
	Vs (V)	*Rs* (Ohm)	*Vs* (V)	*Rs* (Ohm)
Scheme I	0	0.22	0	0.58
Scheme II	0	0.053	0	0.22
De Doncker's	0	0.16	4	0.1
Lai's	0	0.33	4	0.005
Vlatko's	0	0.11	0	0.29

schemes of Fig. 3.1(b), 3.1(c) and 3.10(b) are designed with a similar total auxiliary circuit cost: two MOSFET devices IXFM20N60 (600V, 0.35 Ω) in parallel as an auxiliary switch for Fig. 3.1(b), six IXFM20N60 in parallel as the auxiliary switch in Fig. 3.1(c), and three IXFM20N60 in parallel as an auxiliary switch in Fig. 3.10(b). For the 900 V converter, IGBT device IXGH25N120A (1200 V, 25 A) is used as the auxiliary switches for the topologies shown in Figs. 3.1(a) and 3.1(b), because these two topologies are able to turn off the auxiliary switches under the zero-current condition. Six MOSFET devices IXTH13N110 (1100 V, 0.92 Ω) in parallel are used as the auxiliary switch in Fig. 3.1(c), while three IXTH13N110 in parallel are used as an auxiliary switch in Fig. 3.10(b). The parameters of the auxiliary circuit parameters are shown in Table 3.2(b), in which the on-resistance of MOSFET devices is calculated at 125°C junction temperature. The voltage drop of diodes in the auxiliary circuit is assumed to be 1.5 V. The snubber capacitance across each main switch is 5.6 nF in 450 V converters, and 2.7 nF in 900 V converters. The snubbers selected can reduce the switch turn-off loss by around 30% of the hard-switching values, and the waveform distortion caused by them is still small. The resonant inductors are designed to limit the di/dt in the charging stage to about 100 A/uS. The inductance of each resonant inductor is selected to be:

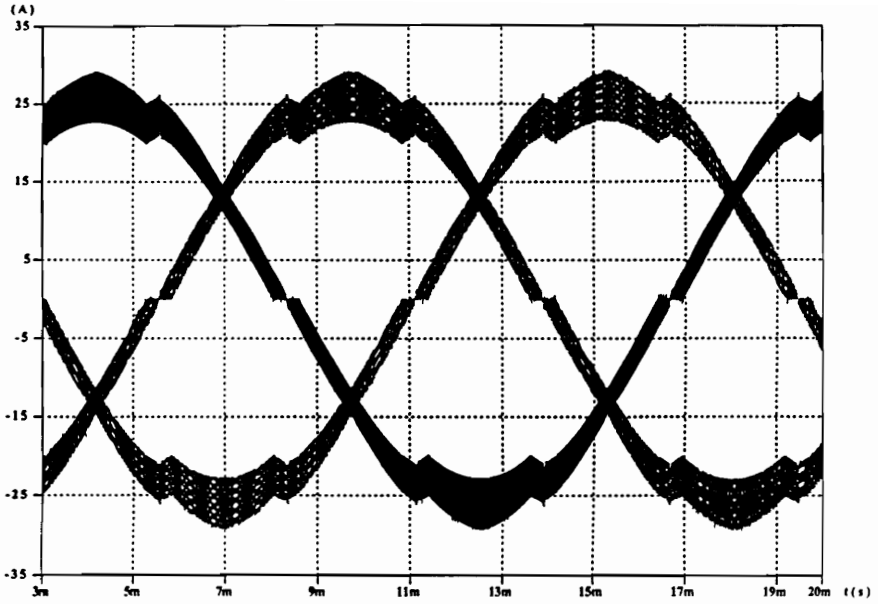
In ARCP (Fig. 3.1(a), labeled as De Doncker's in the following discussion): 4 uH for the 900 V converter, and 2 uH for the 450 V converter;

In the ZVT converter (Fig. 3.1(b), labeled as Vlatko's) and resonant snubber converter (Fig. 3.1(c), labeled as Lai's in the following discussion): 5.4 uH for the 900 V converter, and 2.7 uH for the 450 V converter;

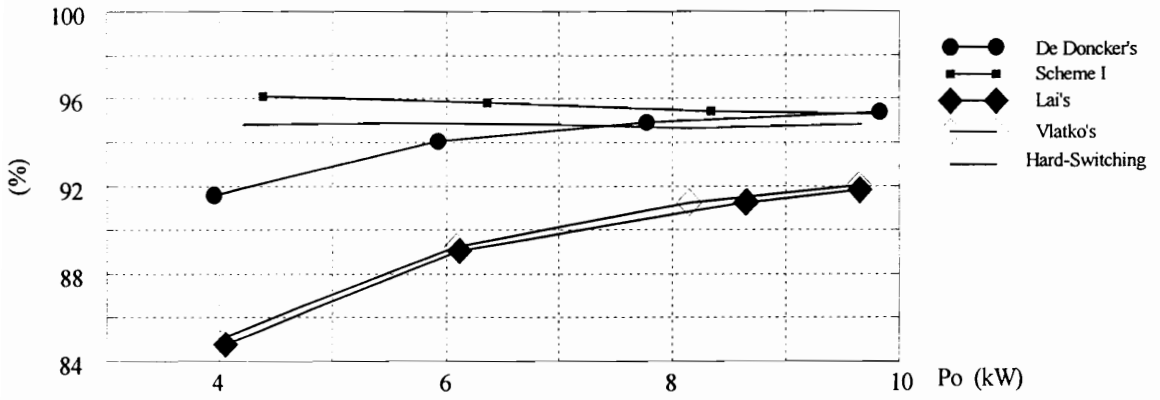
In the proposed new topology (Fig. 3.10, labeled as "Scheme I"): 8 uH for the 900 V converter, and 4 uH for the 450 V converter;

The power loss in the resonant inductors is represented by their series resistors, whose value is set to be 1.25 mΩ/uH according to a sample design.

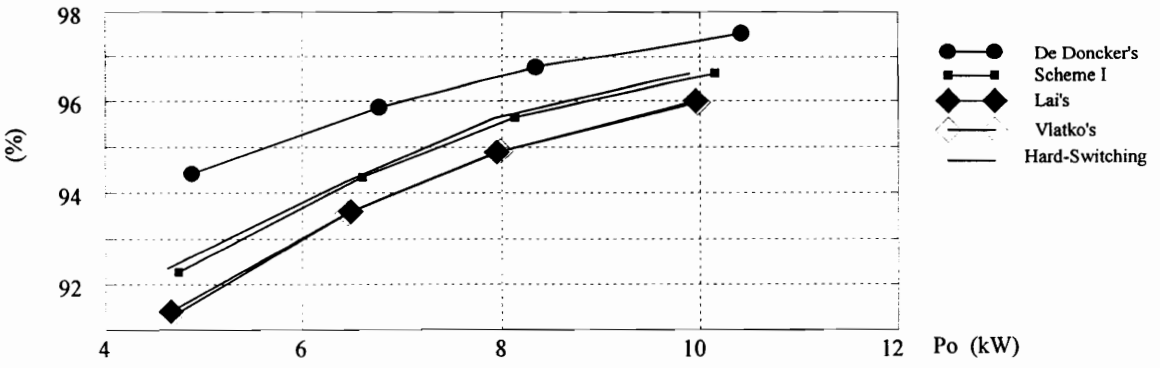
Simulation results are shown in Fig. 3.17. The input current waveforms shown in Fig. 3.17(a), which are obtained on a 900 V rectifier, are largely sinusoidal, and the



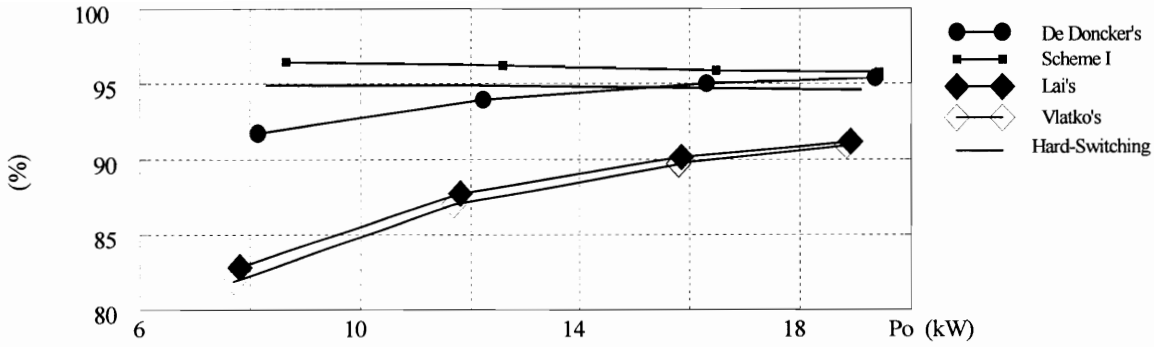
(a). Input current waveform



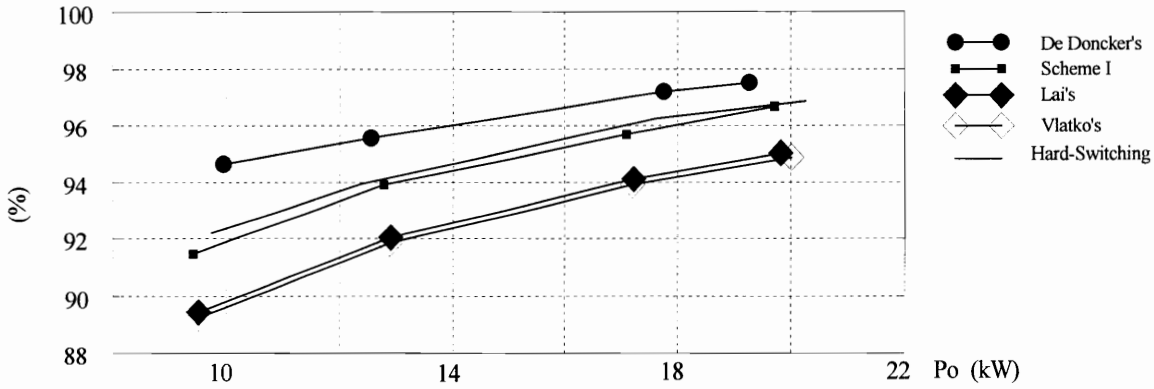
(b). Efficiency evaluation of 450 V rectifiers



(c). Efficiency evaluation of 450 V inverters



(d). Efficiency evaluation of 900 V rectifier



(e). Efficiency evaluation of 900 V inverters

Figure 3.17 **Simulation results**. The proposed soft-switching scheme achieves the highest efficiency in all topologies in rectifier mode. In inverter mode, only ARCP has efficiency improvement over hard-switching converters. However, in inverter mode, the new soft-switching scheme still has a significantly higher efficiency than Vlatko's ZVT topology and Lai's resonant snubber topology.

maximum peak-peak current ripple is about 8 A. The current distortion around the peak is typical in analog controlled rectifiers, in which the phase with highest current is not switched to reduce the switching loss. The current THD is around 4%, which is acceptable in most applications. Figs. 3.17(b) through (e) show the efficiency comparison of different topologies under different output power levels. Due to the elimination of extra turn-off loss, the proposed ZVT scheme, labeled as "Scheme I", achieves the highest efficiency in rectifier mode among all soft-switching topologies: around 96% in the 450 V rectifier, and around 97% efficiency in the 900 V rectifier. Its efficiency improvement over the hard-switching converter is more than 0.5% in the 450 V rectifier and more than 1% in the 900 V rectifier. In both the 450 V and the 900 V inverters, the efficiency of the proposed soft-switching scheme is close to hard-switching converters', but significantly higher than the efficiencies of the previous ZVT topology proposed by Dr. Vlatko and the resonant snubber circuit proposed by Dr. Lai. Among the evaluated soft-switching topologies, the ARCP topology proposed by Dr. De Doncker is the only one demonstrating efficiency improvement over its hard switched counterpart in inverter operation in the simulation. The soft-switching topologies proposed by Vlatko and Lai have almost the same efficiency, due to their similarity in operation. Because of the huge extra main switch turn-off loss, these two topologies do not show any efficiency improvement in the simulations. However, they can possibly achieve a certain efficiency improvement if MOSFET devices or larger capacitor snubbers can be used. The efficiency improvements of soft-switching topologies in the 900 V converters are considerably higher than in the 450 V converters, since 1200 V IGBT has higher turn-on loss than 600 V IGBTs. It should be noted that the junction temperature of all power switches is assumed to be 125°C in the simulations for all topologies. Considering that the junction temperature in a soft-switched converter can be lower than in a hard-switched converter, the efficiency improvement of soft-switched converters could be higher than the simulation results in a practical circuit. Also, in the simulation of inverter operation, the load displacement angle is within 30°, so the highest current is not

switched in the hard-switching inverter and in ARCP inverters. If the load displacement angle is beyond 30°, the efficiency of hard-switched inverter and ARCP will be lower than simulated, and other soft-switched inverters may achieve higher efficiency improvement.

The above simulation results only indicate the efficiency comparison with the same main power devices. Since the switches in the soft-switching topologies have lower switching stress than the switches in the hard-switching topology, the voltage and current rating of power devices can be lower in soft-switching converters than in hard-switching converters. Therefore, the efficiency comparison could be more favorable to the soft-switching topologies than is illustrated by the simulation. However, the comparison among different soft-switching topologies obtained from the simulation results would be still valid, since all these soft-switching converters have similar switching stresses.

3.3.5 CONCLUSIONS

The analysis, design, experimental results, and simulation results of novel zero-voltage-transition three-phase PWM boost rectifiers/voltage source inverters are presented for high-performance, medium-power applications. These converters incorporate simple ZVT circuits into conventional PWM converters to reduce the switching losses of power devices. The ZVT circuits are not in the main power path, are actuated only for a short period before the main switch turn-on, and so they process only a small portion of the converter input power. These soft-switching converters operate in a similar way as a conventional PWM converter most of the time, and can utilize any PWM schemes with active switch turn-on synchronized, so they still have all the desired advantages of a PWM converter, namely minimum voltage/current stress, minimum circulating energy, and fixed frequency operation. However, with the ZVT circuit, a switch is always turned on after the conducting diode in the same leg is turned off, so the diode reverse recovery problem, which is very severe and the main source of switching

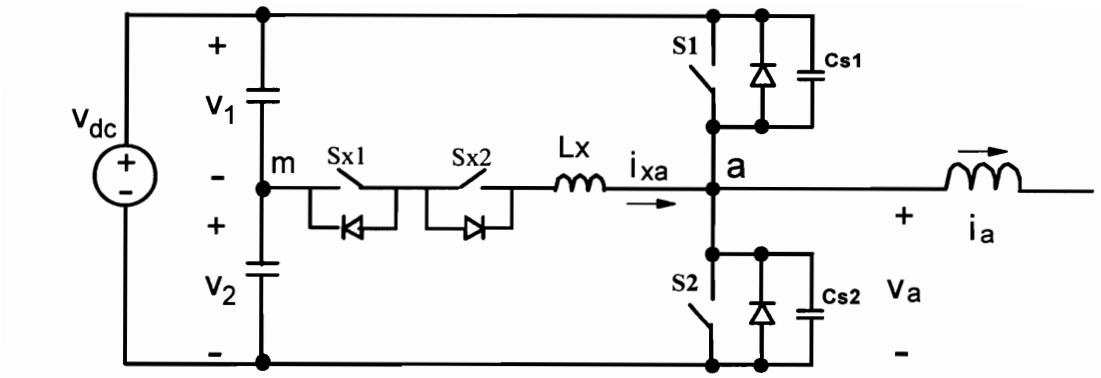
loss in a conventional high-voltage PWM converter, is eliminated completely. The switch turn-on voltage is also reduced in all these new topologies, further reducing the turn-on loss.

A ZVT bi-directional three-phase boost rectifier/voltage source inverter is analyzed and evaluated in detail. Compared to the pre-existing ac-side commutation ZVT converters, the proposed new ZVT topology does not need to overcharge the auxiliary inductor, and has fewer main switch turn-off events and lower auxiliary current peak, thus having the advantages of lower turn-off loss of the main switches, lower conduction loss in the auxiliary circuit, and simpler control requirements. The operation principle of the ZVT circuit is verified in experiments. Switching model simulation results with experiment-based power loss model prove that significant efficiency improvement over hard-switched converter can be achieved with this soft-switching scheme. Especially, the efficiency improvement of this topology in rectifier mode is higher than that of all other soft-switching topologies evaluated in this section, making the ZVT scheme very attractive in PFC applications.

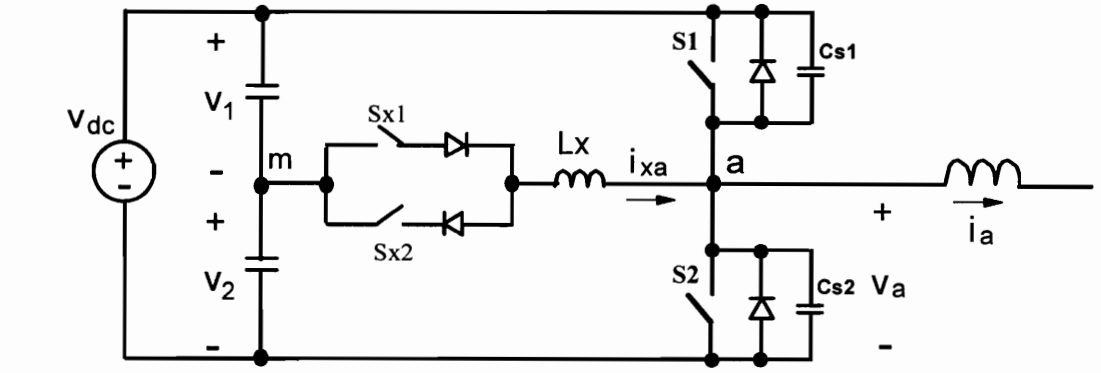
3.4 SOFT-SWITCHING THREE-PHASE BOOST RECTIFERS/ VOLTAGE SOURCE INVERTERS WITH REDUCED AUXILIARY SWITCH STRESSES

3.4.1 TOPOLOGY DEVELOPMENT

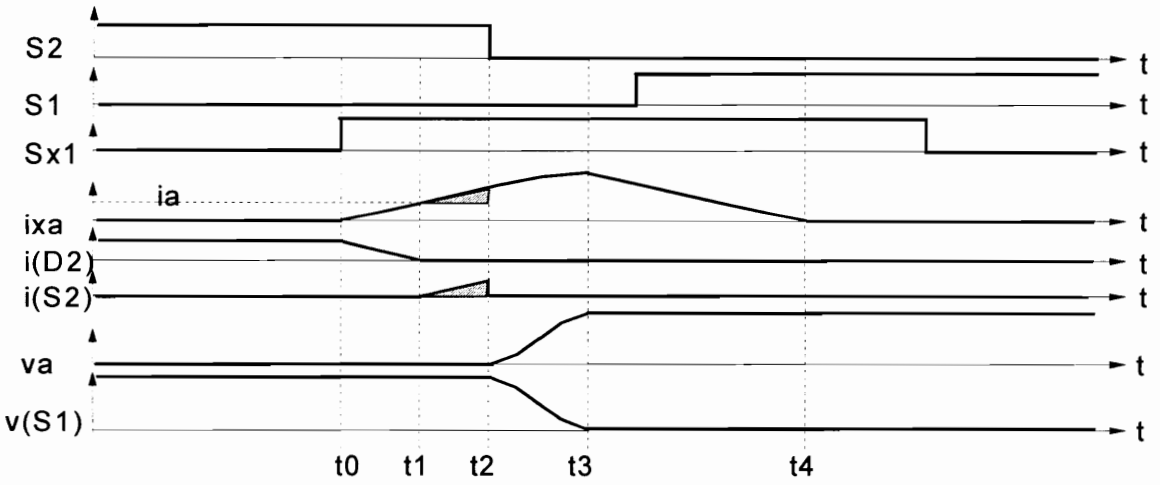
The ZVT converters discussed in the last section achieve soft switching for the main switches. However, like the basic ZVT cell in dc-dc converters, the auxiliary switches in the ZVT circuit have to withstand full dc-link voltage, and are turned off with high current. For high voltage applications, the auxiliary switches have to be implemented as several MOSFET devices in parallel to reduce the switch conduction loss, and thus have high implementation cost. Because the on resistance of MOSFET devices is approximately proportional to the square of their breakdown voltage, a lower voltage rating of the auxiliary switches can significantly reduce their conduction loss, and also the switching loss due to a lower switching voltage. Besides, a reduced voltage stress usually means that part of the dc-link voltage can be used to discharge the resonant inductor, so zero-current, and therefore loss-free, turn-off of auxiliary switches is possible, which allows low conduction loss devices, such as IGBTs and MCTs, to be used as the auxiliary switches. One method to reduce the auxiliary switch voltage stress in bridge-type converters is to connect the auxiliary switches to the midpoint of the dc link, as is shown in Fig. 3.18(a). The auxiliary switches Sx1 and Sx2 are current-unidirectional switches. Sx1 is used to achieve soft-switching in the commutation from D2 (the antiparallel diode of S2) to S1, while Sx2 is used to achieve soft-switching in the commutation from D1 (the antiparallel diode of S1) to S2. The two auxiliary switches Sx1 and Sx2 are connected to form a bidirectional switch, since the load current i_a is usually bidirectional. Another implementation of the auxiliary switches is shown in Fig. 3.18(b), which has the same operation concept as the one shown in Fig. 3.18(a). The operation of the auxiliary circuit can be exemplified by the commutation from D2 to S1. The main current i_a is



(a). Basic topology. Sx1 for S1 turn-on, and Sx2 for S2 turn-on



(b). Another implementation of the auxiliary switches



(c). Soft-switching commutation from D2 to S1. Auxiliary switches turned off with zero current.

Figure 3.18 **A modified ZVT cell for bridge-type circuit**. The auxiliary switches block only half the dc-link voltage, and are turned off with zero-current. However, the resonant inductor overcharging, shown in the shaded area, is still required to achieve zero-voltage turn-on of main switches.

assumed to be positive and constant during the soft-switching transition. The soft-switching commutation includes the following operating stages:

(a). Charging Stage [t0, t1] The current i_a is originally conducted by D2. S2 can also be turned on without affecting the converter operation. At t0, Sx1 is turned on to start the soft-switching transition. As the resonant inductor Lx is charged by the bottom half of the dc-link voltage, V2, i_{xa} increases with the rate of $V_{dc}/(2L_x)$, and the current in D2 is diverted into the auxiliary circuit with the same rate;

(b). Overcharging Stage [t1, t2] At t1, i_{xa} reaches the same magnitude as i_a, so the current inside D2 becomes zero, and D2 is turned off. Because S2 is turned on, the charging of Lx continues, and the extra current $i_{xa} - i_a$ is conducted by S2.

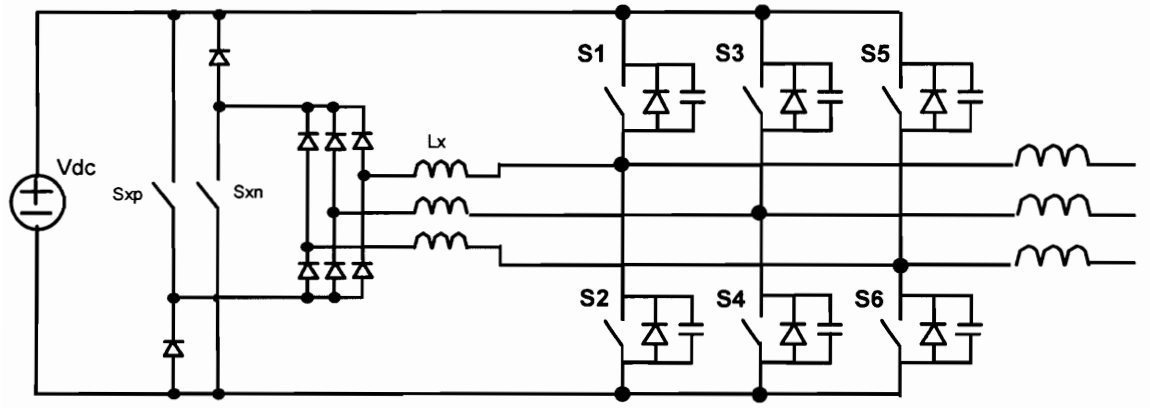
(c). Resonant Stage [t2, t3] After enough energy is built up in Lx, S2 can be turned off at t2. Then, Lx starts to resonate with the node capacitance, $C_{s1} + C_{s2}$. During the resonance, v_a increases towards the positive dc-link p, so the voltage across S1, v(S1), is reduced in a resonant manner.

(d). Discharging Stage [t3, t4] At t3, v(S1) is reduced to zero, so D1, the antiparallel diode of S1, starts to conduct, and clamps v(S1) at zero. Because the energy of Lx is built up high in the overcharging stage, the conduction of D1 will last for a short period, in which S1 can be turned on with the zero-voltage condition. Now Lx is discharged by the upper half of the dc-link voltage V1, and i_{xa} is reduced with the slope of $V_{dc}/(2L_x)$, so the current in S1 increases with the same slope, and the commutation energy stored in Lx is delivered back to the dc-link voltage source. When i_{xa} is discharged to zero at t4, the antiparallel diode of Sx2 is turned off under a zero current condition, and the auxiliary circuit is functionally disconnected from the main power stage. After t4, Sx1 can be turned off with zero current.

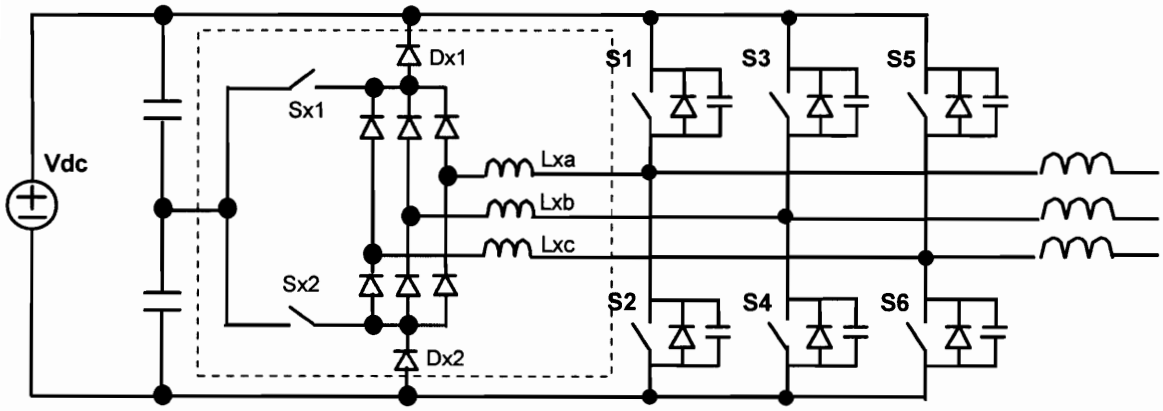
The key waveforms of this commutation are shown in Fig. 3.18(c). Clearly, the auxiliary switches need to withstand only half of the dc-link voltage, and are turned off with zero current. As a result, their voltage stress and current stress are both reduced. An

example of this concept in three-phase converters is the well-known auxiliary resonant commutated pole (ARCP) converter [B27] shown in Fig. 3.1(a). The split dc-link is usually implemented as two bulk capacitors. The charge balance of the dc-link midpoint "m" (i.e. the voltage balance of V_1 and V_2) can be maintained because i_{xa} is an ac current. However, in a single phase configuration as shown in Fig. 3.18(a), the charge balance can be achieved only at the ac line frequency, which could be very low in inverter applications. Therefore, very large dc-link capacitance is required to limit the voltage difference between the two half dc-link voltages V1 and V2 to a low value in low-line-frequency operations. In a three-phase configuration such as the ARCP, the dc-link charge balance becomes easier to maintain, since it can be achieved with triple the line frequency or even at switching frequency, depending on the modulation scheme used.

Simplified soft-switching topology can also be developed by incorporating the synchronized turn-on PWM and generalized PWM cell concept discussed in the last section. Fig. 3.19(a) redraws a simple soft-switching topology originally shown in Fig. 3.7(b). Using the same concept as in Figs. 3.18(a) and (b), the auxiliary switches can be connected to the midpoint of the dc link, as is shown in Fig. 3.19(b). Although the topology of Fig. 3.19(a) can only be used in rectifier mode, the new topology in shown in Fig. 3.19(b) can work in both rectifier mode and inverter mode, since now half of the dc-link voltage can be used to discharge the resonant inductors. This topology is a simplified version of the ARCP. With only two auxiliary switches required, this converter has a much lower circuit complexity and implementation cost than the ARCP, but can achieve a similar performance.



(a). A simple ZVT three-phase rectifier



(b). Connect the auxiliary switches to the dc-link midpoint to reduce their voltage stress

Figure 3.19 **Topology development of soft-switching three-phase boost rectifier/voltage source inverter with reduced auxiliary switch stress.** The principle of split dc link is applied to the simple ZVT topology of (a), so the auxiliary switch stress is reduced. The topology of (b) can also be used in inverter mode, because half of the dc-link voltage can be used to discharge the resonant inductors.

3.4.2 SOFT-SWITCHING OPERATION

As can be seen from Fig. 3.19(b), the whole converter consists of two parts: the main power stage which is the same as a hard-switching inverter bridge, and a shunt auxiliary ZVT circuit. The auxiliary circuit includes three resonant inductors, Lxa, Lxb, and Lxc; two auxiliary switches Sx1 and Sx2; an auxiliary diode bridge, and two clamping diodes, Dx1 and Dx2. Since the auxiliary switches are connected to the midpoint of the dc link, they need to break only half of the dc link voltage. The converter works in the same way as its PWM counterpart most of the time. The ZVT auxiliary circuit is used to help active switches turn on, and is active only for a short time in each switching cycle, so it has a much lower power rating than the main power stage. As in Section 3.3, the operation of the ZVT circuit can also be exemplified by the case of $v_A > 0 > v_B > v_C$. According to the modulation scheme, the typical turn-on commutation is from S1, D3, D5 to S1, S4, S6 in inverter mode operation, and from D1, D4, D6 to D1, S3 and S5 in rectifier mode operation. The ZVT circuit is used to help the commutation from a diode to a switch in any phase, and could be operated in a way similar to those described in [B27] [B29]-[B31] [B42], achieving complete zero-voltage switching of the main switches by overcharging the resonant inductor currents to a level higher than the phase currents to provide enough energy to discharge junction capacitors, as is shown in Fig. 3.18(c). This control method, however, will result in high extra turn-off loss of the main switches and high conduction loss in the auxiliary circuit. Considering the fact that the dominating part of switch turn-on loss is usually the diode reverse recovery loss in high power, high voltage devices, and the capacitive turn-on loss is usually negligible if the turn-on voltage and current are reduced, zero-voltage turn-on of the switches is not absolutely necessary, and the auxiliary circuit can be used to eliminate diode reverse recovery and to reduce switch turn-on voltage to as close to zero as possible. This control approach, which is used in the following discussion, can achieve higher efficiency than the one relying on overcharging control.

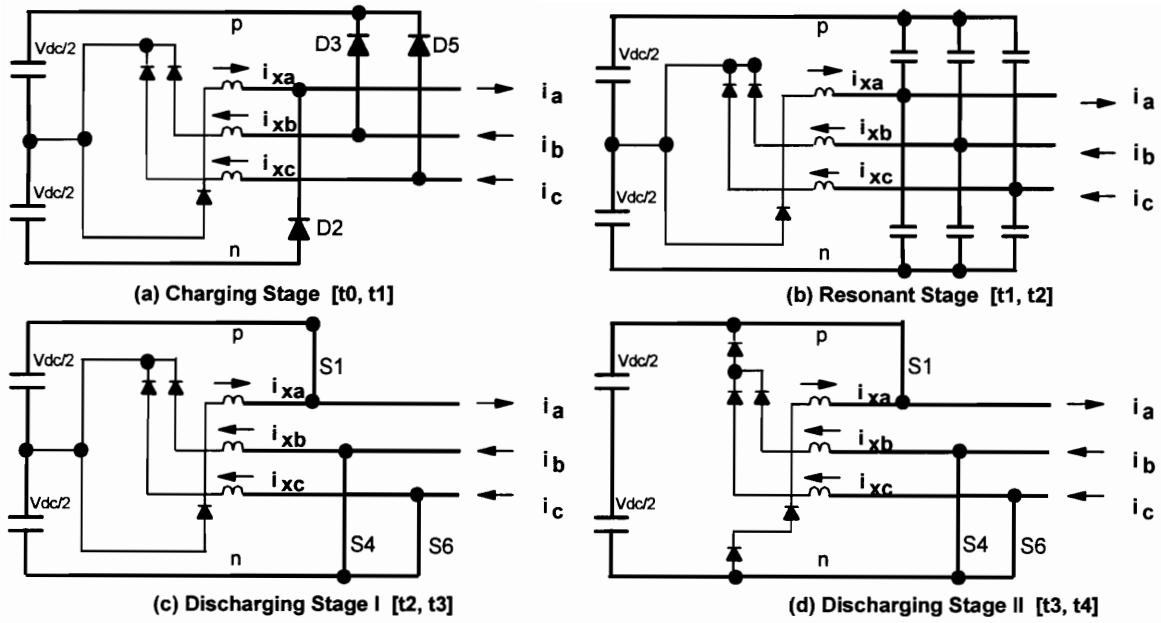
Mode A: Soft-switching commutation in inverter mode

The auxiliary circuit cannot be directly used if the main power stage is in a zero vector, since the resonant inductor connected to the unswitched phase, Lxa in this example, cannot be discharged unless additional commutation power supply is used. Therefore, at the beginning of the commutation, S1 is turned off, so the current in Phase A is transferred into D2, and the auxiliary circuit is used to reduce the switch turn-on loss in the commutation from D2, D3, D5 to S1, S4, S6. The active operating stages during the commutation are shown in Fig. 3.20(a).

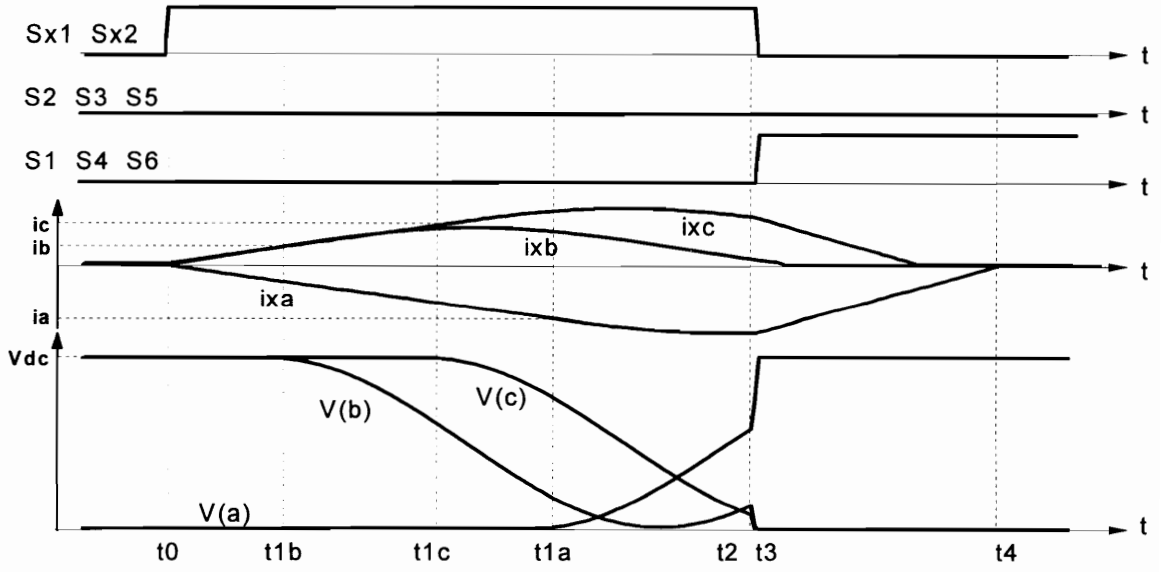
(a) Charging Stage [t0, t1] Before the main switches are turned on, the auxiliary switches Sx1 and Sx2 are turned on first. The resonant inductors Lxa, Lxb, and Lxc will start to be charged by half dc link voltage, and the currents in D2, D3, and D5 will be diverted into the auxiliary circuit. Note that the duration of this stage is different in the three phases, depending upon the phase current;

(b) Resonant Stage [t1, t2] When the current in any diode is reduced to zero, that diode is turned off naturally. The resonant inductor then starts to resonate with the node capacitance in its corresponding phase, and the node voltage moves towards the opposite dc rail. The current peak in a resonant inductor is the corresponding phase current plus a resonant peak of $V_{dc}/(\sqrt{2\,Lr/Cs})$, in which Lr is the resonant inductance, and Cs is the capacitance of each main switch.

(c) Discharging Stage I [t2, t3] S1, S4, and S6 can be turned on at the same time when the voltages across them are all reduced to around zero. Since the diodes are already turned off, diode reverse recovery loss is much reduced. Because the turn-on current, which is the difference between the corresponding phase current and resonant current, and the turn-on voltage of all switches are all reduced, the turn-on loss is reduced dramatically. The major turn-on loss will be the snubber capacitor energy loss, which should be designed to be much smaller than the switch turn-on loss in hard switching. After the main switches are turned on, the voltage across each resonant inductor is



(a) Active subtopologies.



(b) Simulated waveforms.

Figure 3.20 **Soft-switching commutation in inverter mode**. The diode reverse recovery is eliminated, but the switch turn-on voltage cannot be reduced to zero, because the resonant inductors are not overcharged. There is an extra main switch turn-off before the commutation starts.

reversed compared to the polarity in the charging stage, so the resonant inductor currents start to decrease.

(d) Discharging Stage II [t3, t4] Before any current in the resonant inductors reaches zero, the auxiliary switches should be turned off. Then the resonant inductors are discharged by the dc-link voltage through Dx1 and Dx2. When a resonant inductor current is reduced to zero, the corresponding diode in the auxiliary diode bridge turns off naturally. After all auxiliary diodes are turned off at t4, the whole auxiliary circuit is disconnected from the main power stage functionally, and the converter resumes its PWM operation until the next turn-on commutation. Since there is no extra main switch turn-off during the commutation except the one at the very beginning, and the current peak of auxiliary switches is limited automatically to a value a little higher than the phase currents, converter efficiency is improved compared to the ZVT topology in [B29, B42].

Note that the maximum possible duration of the Discharging Stage I changes with the phase currents. To simplify the control timing, we set the duration to be zero in our simulation and experiments, i.e. the auxiliary switches are turned off when the main switches are turned on. The simulated waveforms are shown in Fig. 3.20(b).

Mode B: Soft-switching commutation in rectifier mode

The auxiliary circuit is used to help switch turn on in the commutation from D4, D6 to S3, S5. The commutation process is shown in Fig. 3.21(a).

(a) Charging Stage [t0, t1] Before the main switches are turned on, the auxiliary switch Sx2 is turned on first. The resonant inductors Lxb and Lxc are charged by half of the dc-link voltage, and the currents in D3 and D5 are diverted into the auxiliary circuit. Similarly to in inverter mode, the duration of this stage in each phase depends on the phase current;

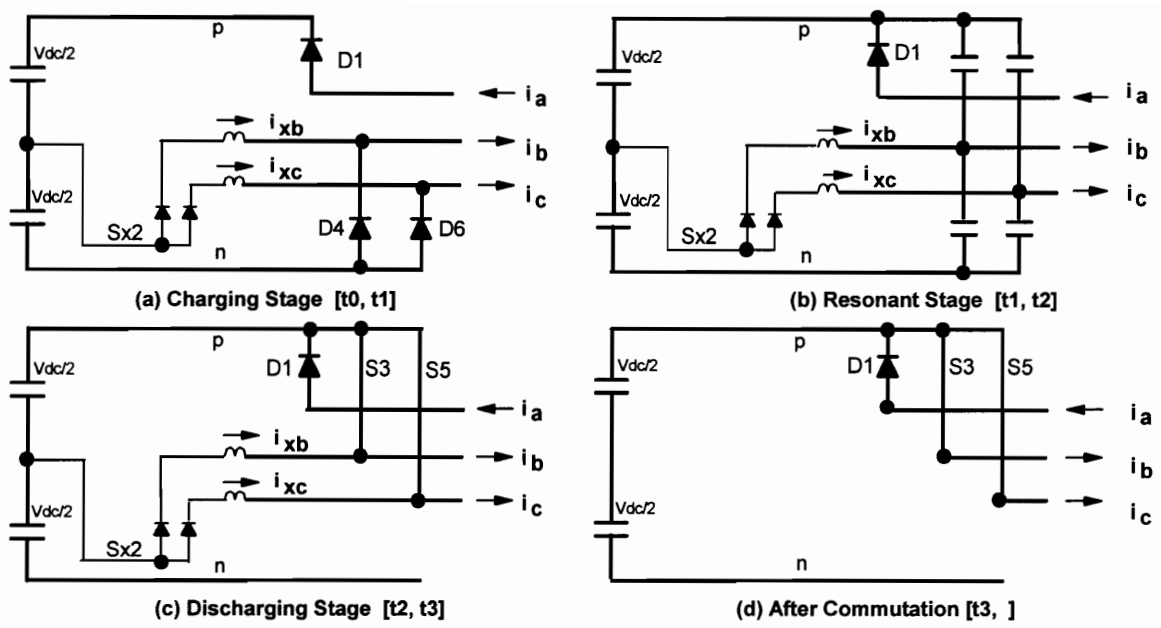
(b) Resonant Stage [t1, t2] When the current in any outgoing diode (D4 or D6) is reduced to zero, that diode is turned off naturally. The resonant inductor then starts to

resonate with the node capacitance in the corresponding phase, and the node voltage moves towards the positive dc rail.

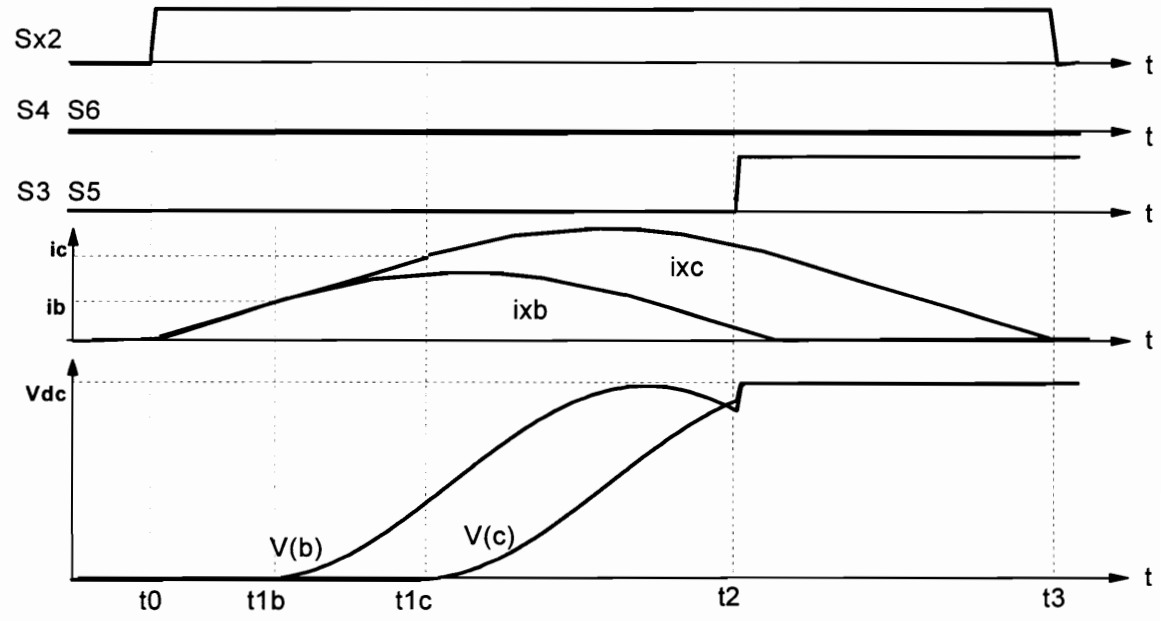
(c) Discharging Stage [t2, t3] S4 and S6 are turned on when the voltages across them are all reduced to around zero. Similarly to what happens in inverter mode, diode reverse recovery loss is avoided, and switch turn-on voltages and currents are reduced, so the turn-on loss is reduced dramatically. After the main switches are turned on, the resonant inductors L_{xb} and L_{xc} are discharged by half of the dc link voltage, so their currents are reduced linearly. When a resonant inductor current is reduced to zero, the corresponding diode in the auxiliary diode bridge turns off naturally. After enough time, the current in both resonant inductors, thus also in Sx2, can be reduced to zero. Then Sx2 can be turned off with zero current, and the converter resumes its PWM operation until the next turn-on commutation. No extra main switch turn-off is required in the PWM scheme and during the commutation, and the auxiliary switches are turned off with zero current. Also, only one auxiliary switch is actuated once in a switching cycle. Therefore, very high converter efficiency can be expected. The simulated waveforms are shown in Fig. 3.21(b).

In steady state, the charge balance of the dc link midpoint can be maintained naturally by the symmetrical operation of the three-phase converter. The ZVT network also provides some balance mechanism. For example, if the voltage between the midpoint and negative dc rail gets higher, the current flowing into the midpoint through the auxiliary switches will be smaller, and the current flowing out of the midpoint will be higher. The net charge transferred into the center point is negative, and it will cause the midpoint voltage to decrease. To accommodate the possible imbalance, especially in a very low output frequency operation, some external components, such as ballast resistors, or small modification to main switch timing, can be also utilized.

The performance comparison of this topology with other soft switching schemes is shown in Table 3.1, in which this topology is labeled as Scheme II. From the table, it is expected that this topology can achieve good efficiency improvement.



(a). Active subtopologies



(b). Simulated waveforms

Figure 3.21 **Soft-switching commutation in rectifier mode.** There are no resonant inductor overcharging and extra main switch turn-off. The diode reverse recovery is eliminated, and switch turn-on voltage is reduced.

3.4.3 CONVERTER DESIGN ISSUES

One of the design challenges in this topology is to reduce the switch turn-on voltage as much as possible with a fixed auxiliary circuit timing. The major difficulty to achieve this is that the duration of the charging stage in a phase changes with the phase current. Let t_c be the charging stage duration at a phase current of i, T_c be the charging stage duration at the maximum phase current of I_p, and T_r be the resonant period, i.e.:

$$t_c = 2\,L_r i / V_{dc}\,, \qquad T_c = 2\,L_r I_p / V_{dc}\,, \qquad T_r = 2\pi\sqrt{2L_r C_s}\,, \tag{3.5}$$

where L_r is the indutance of a resonant inductor,and Cs is the capacitance across each main switch. Assuming the power loss during the resonance is negligible, the voltage of the incoming switch during the resonant stage will be:

$$V_{sw} = \frac{V_{dc}}{2}(1+\cos(\omega_r (t - t_c))\,, \tag{3.6}$$

where $\omega_r = 1/\sqrt{2L_r C_s}$. In a practical circuit, there is always some power loss in the resonant devices. However, at the end of the charging stage, the storage charge in the outgoing diode will hold the charging stage a little longer, and the resulting extra charging energy will compensate for the resonant power loss. Therefore, the above equation is still a reasonable approximation to the real waveform.

If the switch is turned on at $t_{on} = (T_c + T_r)/2$, which is independent of the instantaneous phase current, then the turn-on voltage of the switch will be:

$$v_{on} = \frac{V_{dc}}{2}(1+\cos(\pi + (t_c - T_c/2))) = \frac{V_{dc}}{2}(1-\cos(\omega_r (t_c - T_c/2)))\,, \tag{3.7}$$

and the maximum turn-on voltage occurs at $t_c = 0$ (when the phase current is zero), and at $t_c = T_c$ (when the phase current is maximum):

$$V_{on} = \frac{V_{dc}}{2}(1-\cos(\omega_r T_c / 2)) \tag{3.8}$$

Fig. 3.22 shows the relation between the switch turn-on voltage and the phase current for different snubber capacitances. The top part of Fig. 3.22(a) presents half cycle

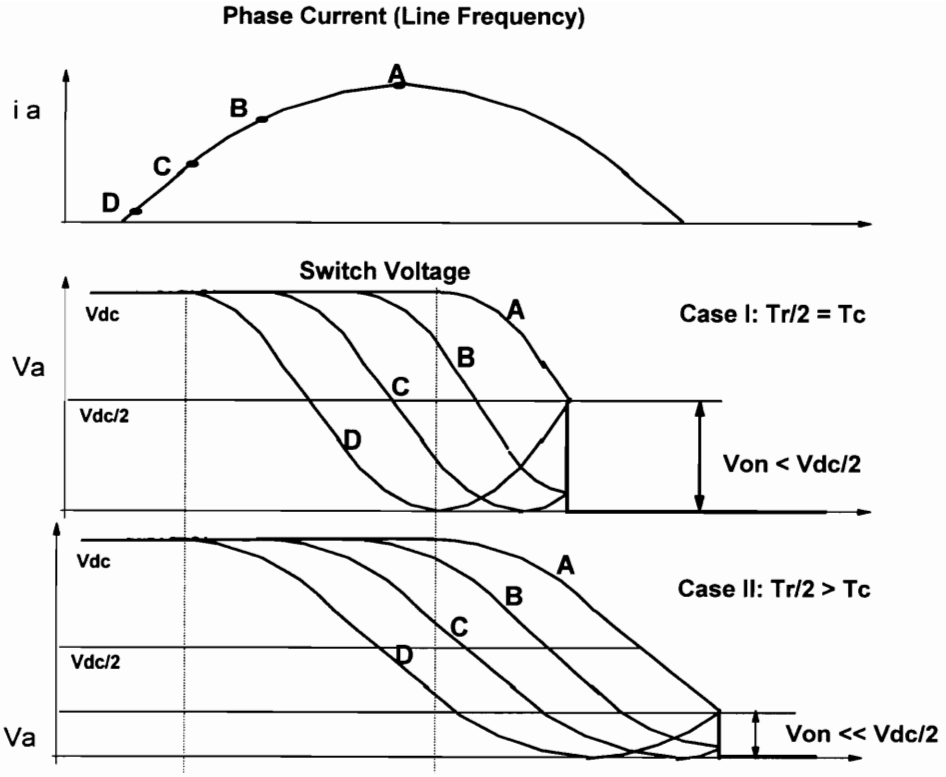
of the phase current, and the middle part and the bottom part of Fig. 3.22(a) give the switch voltage waveforms in the soft switching transition with different phase currents for different snubber capacitances. Obviously, if the maximum charging period T_c is half of the resonant period T_r, and the main switches are turned on with a delay of $1.5T_c$ after the auxiliary switches' turn-on, then the switch turn-on voltage can be kept lower than half the dc-link voltage under all conditions, as is illustrated by the above equation and the middle diagram of Fig. 3.22(a). Then the snubber capacitance across each main switch is:

$$Cs = 2L_r I_p{}^2 / (\pi^2 V_{dc}{}^2), \tag{3.9}$$

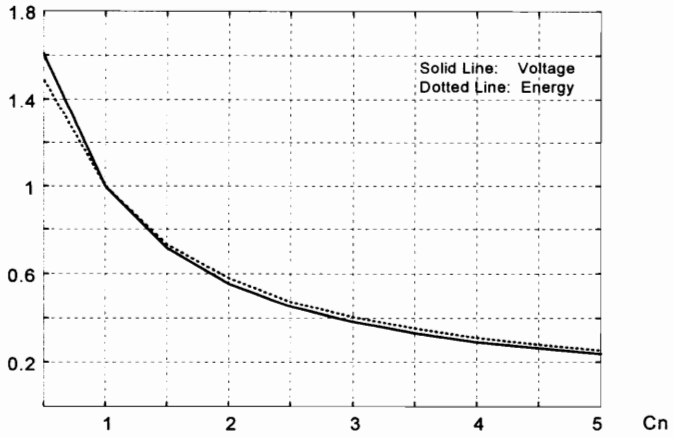
and the peak of the resonant current in the auxiliary circuit, I_r, is:

$$I_r = V_{dc} / (2\sqrt{L_r / (2C_s)}) = I_p / \pi, \tag{3.10}$$

With this design, all switch turn-on voltages can be reduced to below $V_{dc}/2$ for any phase current, and the resonant peak current is about 30% of Ip. Then, considering the average turn-on voltage to be around $V_{dc}/4$, the average capacitive turn-on energy would be about 1/16 of that in the conventional PWM converter. A larger Cs can reduce the turn-on voltage and capacitive turn-on energy further, as is shown by the waveforms in the bottom part of Fig. 3.22(a). Fig. 3.22(b) shows the maximum switch turn-on voltage and average snubber energy at turn-on as a function of the snubber capacitance, normalized to the values determined from $Tc = Tr / 2$. In the above diagram, the phase current is assumed to be of a sinusoidal waveform with an amplitude of I_p, which is the worst case in terms of power loss. Although a high snubber capacitance reduces the power loss in the main switches, it also increases the conduction loss in the auxiliary circuit and current distortion. Therefore, the selection of snubber capacitance is a design trade-off, which should be made considering the switching characteristics of the semiconductor devices in a practical application.



(a). Node A voltage, which equals the voltage across S2, under different phase current and snubber capacitance. A, B, C, D refer to the different phase currents shown in the top diagram.



(b). Normalized maximum turn-on voltage and average turn-on

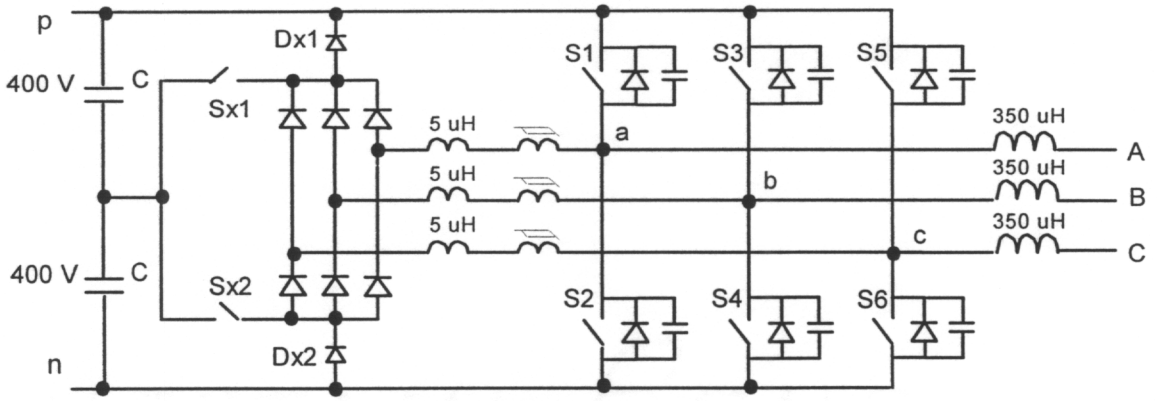
Figure 3.22 Switch turn-on voltage and energy loss as a function of snubber capacitance. Higher snubber capacitance can reduce the switch turn-on voltage and energy.

3.4.4 EXPERIMENTAL AND SIMULATION RESULTS

A prototype converter has been designed based on the proposed topology. The design specifications are: ac line-line rms voltage of 460 V, dc-link voltage of 800 V, output power of 10 kW, switching frequency 50 kHz. The main switches are CM50DY-24H, the auxiliary switches are IXYS IXTH24N50 each, and the diodes in the auxiliary circuit are IXYS DESI 12-10A. The snubber capacitance across each switch is 2.2 nF, which produces about 8 W total capacitive turn-on loss to the converter due to the non zero-voltage turn-on. Each 5-uH resonant inductor is built on TDK K6A T28-13-16 cores. A saturable inductor is in series with each resonant inductor to suppress the parasitic ringing, and is implemented as two turns on Toshiba spike killer SA14-8-4.5. The schematic of the power stage is shown in Fig. 3.23(a).

The prototype is tested under the following conditions: switching frequency 32 kHz, dc link voltage 380 V, and the rms line voltage at the ac side 200 V. The experimental waveforms of the commutation circuit in inverter mode are shown in Fig. 3.23(b). Fig. 3.23(c) shows the low frequency phase currents, which are sinusoidal. The efficiency measurements in rectifier and inverter modes are shown in Figs. 3.23(d) and (e), respectively. Every phase current is switched in hard-switched inverter mode operation, same as in the widely used SPWM control. It can be seen that over 1% efficiency improvement has been achieved in both rectifier mode and inverter mode.

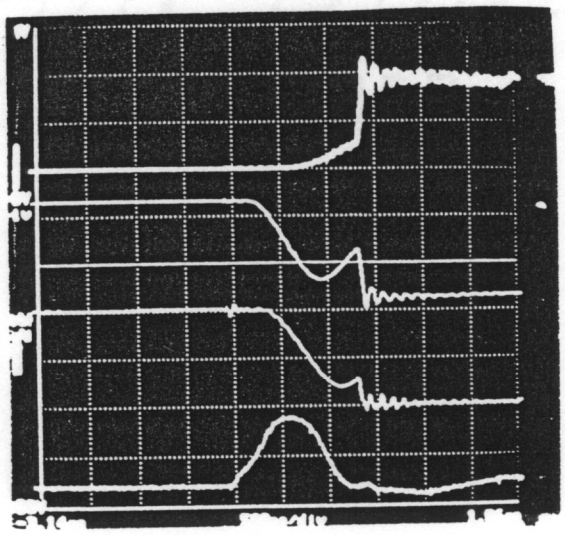
To compare this topology with other soft-switching topologies under the same operating conditions, computer simulation is used to evaluate the efficiency of several soft-switching topologies. The design and operating conditions are the same as in Section 3.3. The soft-switching topology of Fig. 3.19(b) is labeled as "Scheme II" in the following discussion. Each auxiliary switch is three MOSFET devices IXFM40N30 (0.08 Ohm, 300 V) in parallel for the 450 V converters, and three IXFM20N60s (600V, 0.35 Ohm) in parallel for the 900 V converters. The resonant inductor and snubber capacitor across each main switch is 2 uH and 5.6 nF, respectively, in the 450 V



(a). Experimental circuit

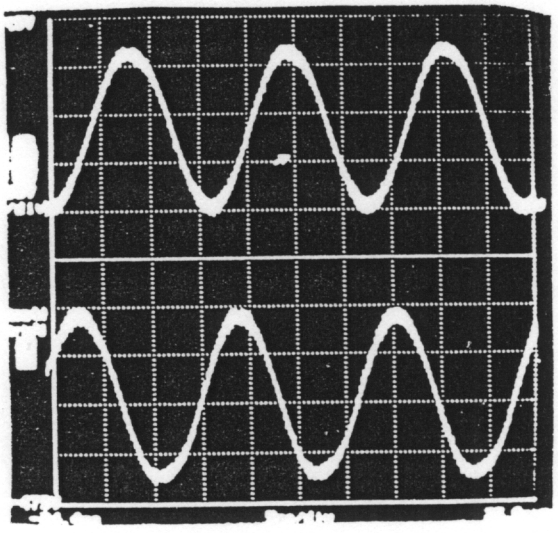
Node Voltages
100 V/div

Aux. Current
10A/div

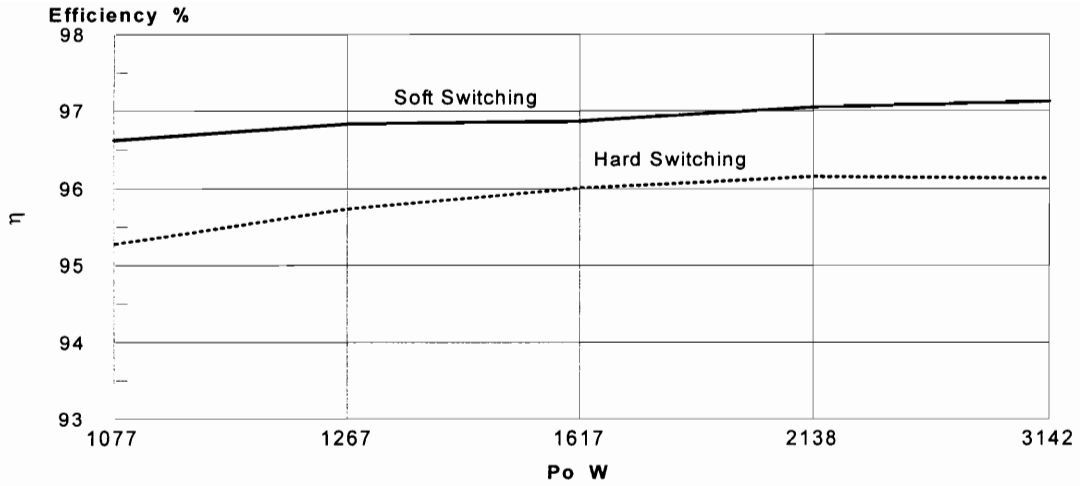


(b). Auxiliary circuit waveforms. Time scale: 500 nS/div.

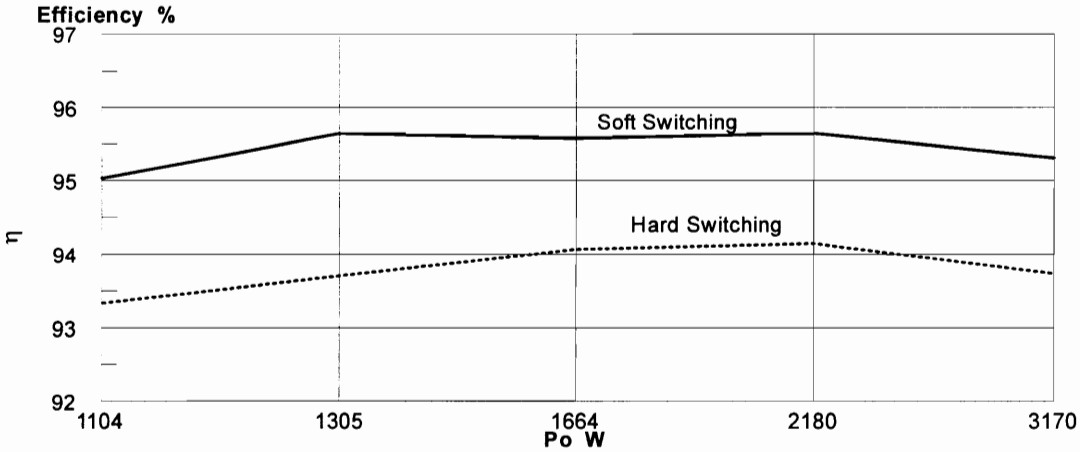
5A/div



(c). Low -requency phase currents. Time scale: 500 uS/div.



(d). Experimental efficiency in rectifier mode

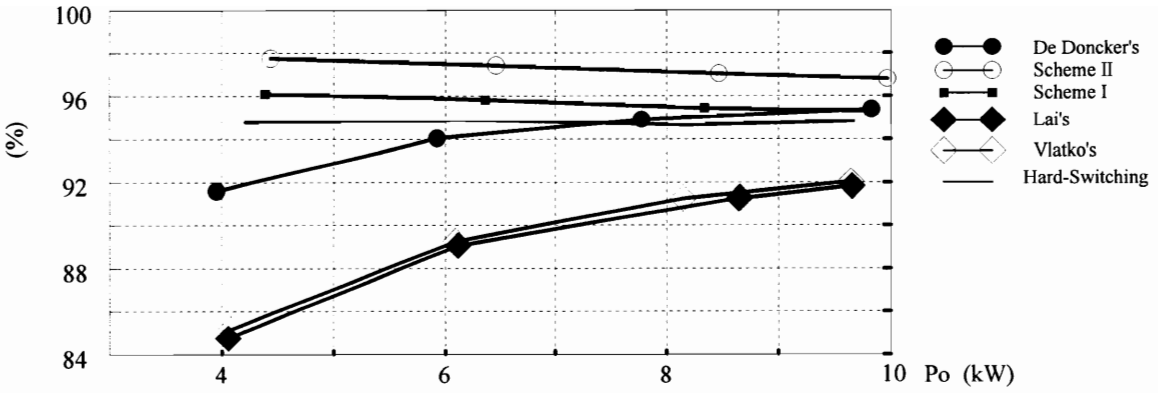


(e). Experimental efficiency in inverter mode. The hard-switching operation is with SPWM.

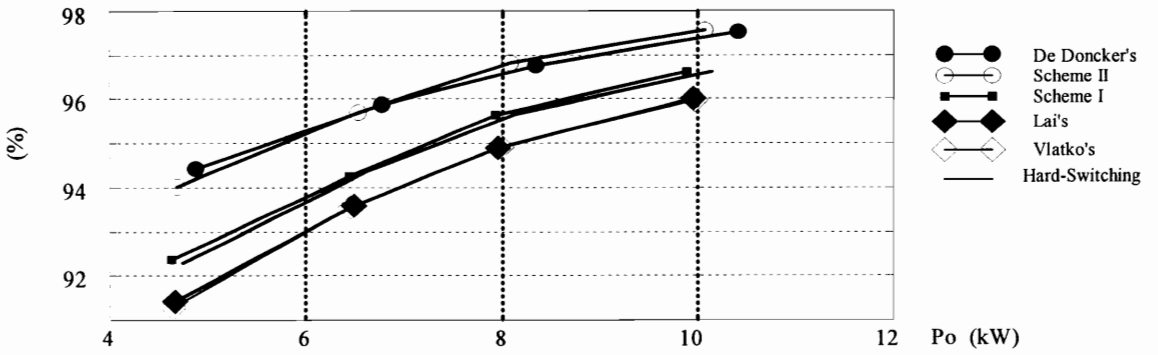
Figure 3.23 **A prototype converter and experimental results.** Significant efficiency improvement is achieved through soft-switching operation.

converters, and 5 uH and 2.7 nF, respectively, in the 900 V converters. The main power stage parameters , as well as the design of other soft-switching topologies, are the same as in the Section 3.3, with the loss model parameters shown in Table 3.2. The simulated efficiency data at 50 kHz switching frequency are shown in Figs. 3.24 (a) through (d). As expected, the new topology with reduced auxiliary switch stresses, "Scheme II", has the highest efficiency among all soft-switching schemes in rectifier mode, and has a very similar efficiency as the ARCP in inverter mode. Therefore, this topology is an attractive soft-switching circuit for medium-power, high-frequency three-phase applications.

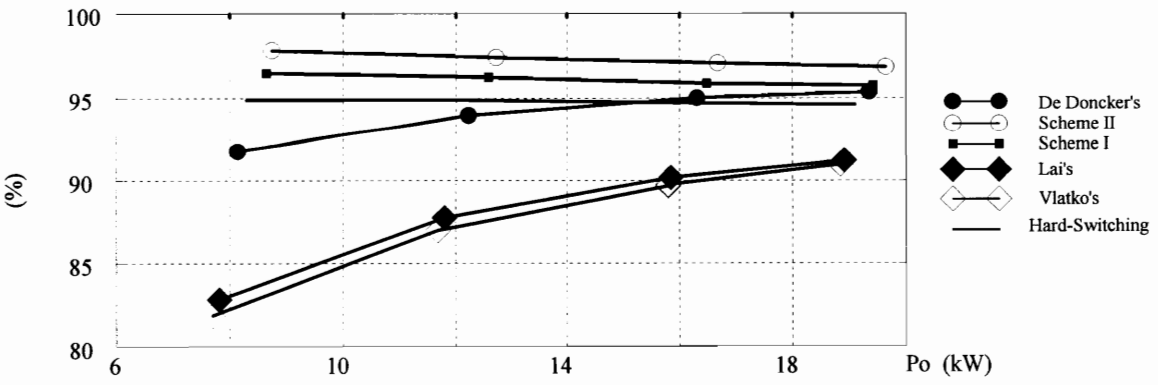
In the above simulation, the snubber capacitance is chosen to be small, and can reduce switch turn-off loss by about 40%. The control of the converter is not affected by the snubbers, since the duty cycle loss contributed by its charging/discharging is very small. A higher snubber capacitance can improve the converter efficiency by reducing the switch turn-off loss further. To evaluate the effect of snubber capacitance on the converter efficiency, these soft-switching topologies are also simulated with each snubber capacitance increased to 8.2 nF in 900 V inverters. The results are shown in Fig. 3.24(e). All soft-switching topologies, except Scheme I which has high turn-on voltage in inverter mode, have noticeably higher efficiency with 8.2 nF snubbers than with 2.7 nF snubbers, because the switch turn-off loss is lower with a larger snubber. However, the high snubber capacitance reduces the dc-link voltage utilization, increases the power loss in the auxiliary circuit, and causes more current distortion due to "zero-current clamp" effect. The choice of snubber capacitance in a specific application is a design trade-off.



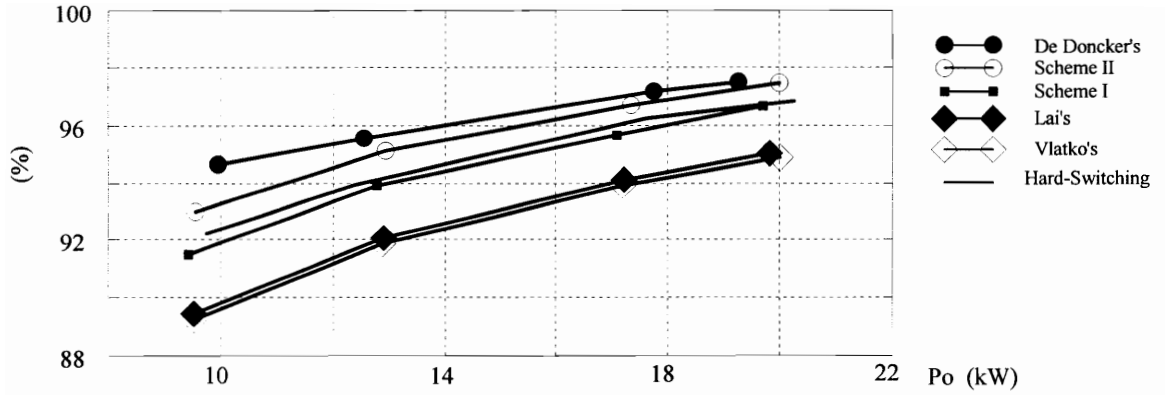
(a). 450 V rectifiers



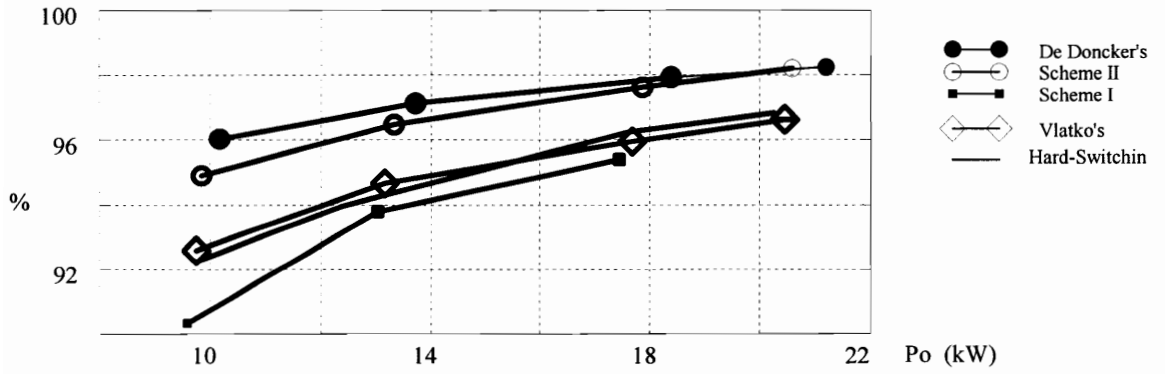
(b). 450 V inverters



(c). 900 V rectifiers



(d). 900 V inverters



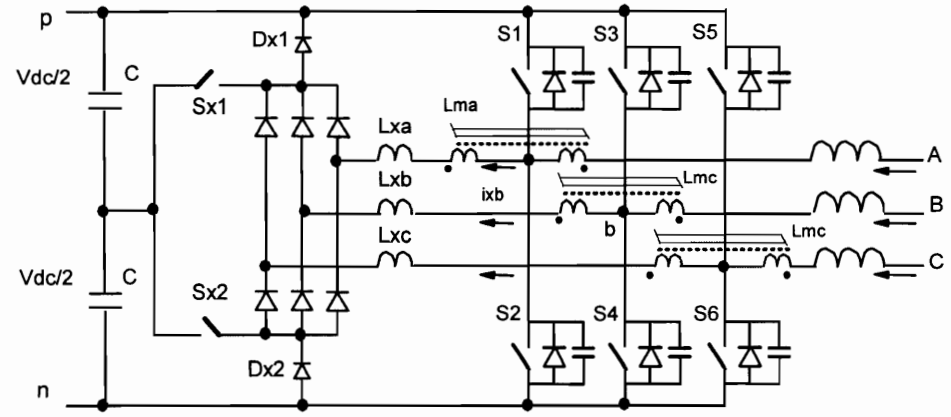
(e). 900 V inverter with 8.2 nF snubbers in soft-switching topologies

Figure 3.24 **Efficiency evaluation with simulation**. The new soft-switching scheme(Scheme II) achieves the highest efficiency among all topologies in rectifier mode. In rectifier mode, its efficiency is second to only ARCP.

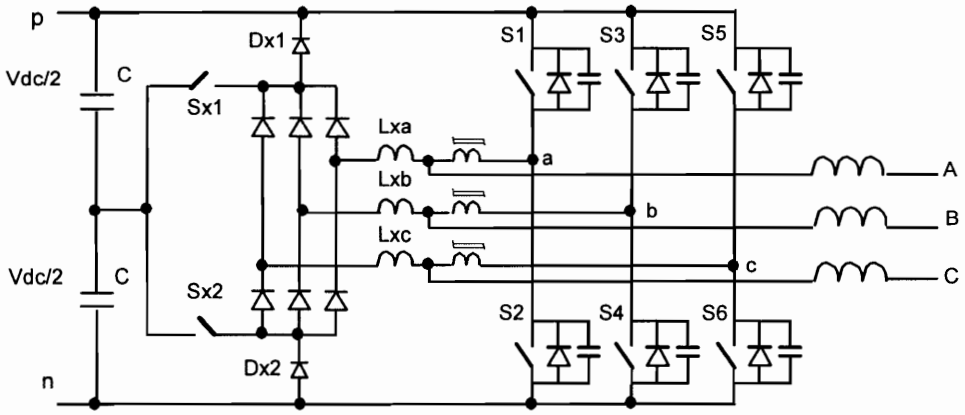
3.4.5 IMPROVEMENT ON THE SOFT-SWITCHING TOPOLOGY

In the topology shown in Fig. 3.19(b), the switch turn-on voltage is usually not negligible. Reducing the switch turn-on voltage will require the use of higher snubber capacitance, which could cause other problems. It could be beneficial for some applications to modify this topology so that the switch turn-on voltage can be reduced independently of the snubber capacitance.

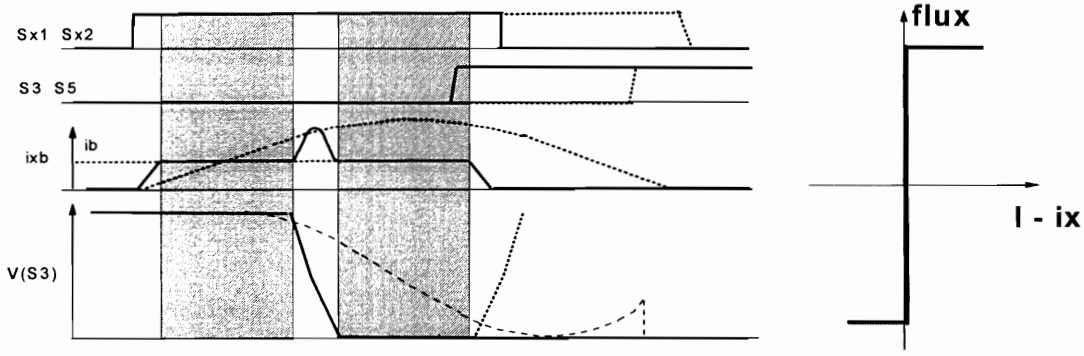
The switch turn-on voltage can be reduced through the use of nonlinear resonant inductors in the auxiliary circuit without using elaborate control timing. The basic principle can be explained by the topology shown in Fig. 3.25(a), in which Lma, Lmb, Lmc are saturable inductors with two windings each. Another slightly different implementation is shown in Fig. 3.25(b), which operates exactly the same as the one in Fig. 3.25(a). When the current in a resonant inductor equals its corresponding phase current, the coupled saturable inductor in that phase gets out of saturation, and its high inductance reduces the rate of switch voltage change. The operation of this topology can be illustrated by the typical waveforms in Fig. 3.25(b), taking phase B as an example. The linear resonant inductance is chosen to be very small. Therefore, when auxiliary switches are turned on, the auxiliary current i_{xb} will be built up to phase current i_b very quickly. Then Lmb gets out of saturation, so both i_{xb} and v(b) start to change very slowly due to the high inductance of Lmb, and diode reverse recovery of D3 is eliminated. As i_{xb} increases slowly to the saturation current of Lmb again, the resonant inductance becomes very small, so the resonance between Lxb and node capacitance brings v(b) towards zero quickly. When v(b) approaches zero, i_{xb} approaches i_b, and Lmb gets out of saturation again and presents high inductance to the resonant circuit. Therefore, v(b) stays around zero for a relatively long time, and S4 can be turned on in this period with very low voltage. In Fig. 3.25(b), the shaded areas illustrates the periods where Lmb is saturated, and the



(a). Basic topology



(b). Another implementation



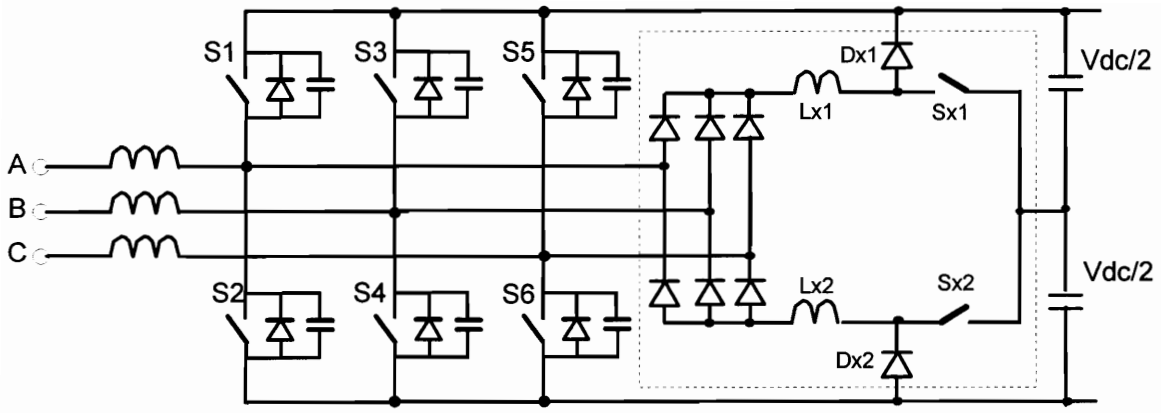
(c). Typical waveforms

Figure 3.25 **A ZVT topology with coupled saturable inductors**. The saturable inductors can increase the time of near-zero switch voltage, so the switch turn-on loss can be reduced to around zero.

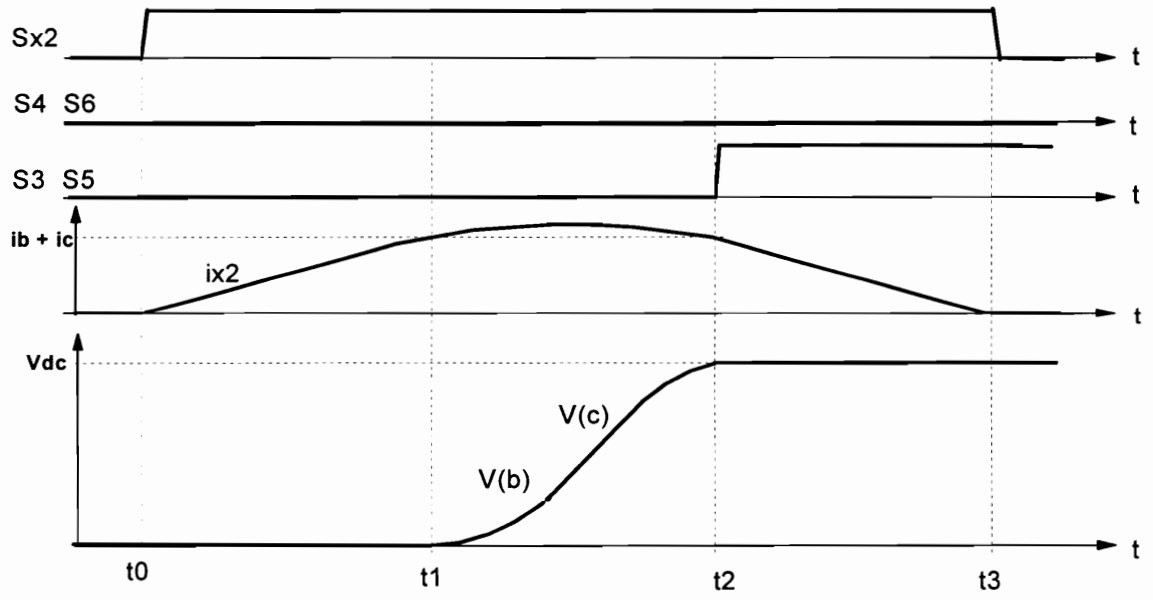
dotted curves are the simulation results without Lmb. Obviously, because the charging period is much reduced with saturable coupled inductors, switch turn-on voltages can be easily reduced to a low value. The use of saturable inductors to help improve soft-switching operation or to reduce power loss in the auxiliary circuit through the use of smaller linear resonant inductors can be generalized to any other ZVT and ZCT schemes.

3.4.6 MODIFIED TOPOLOGY FOR RECTIFIER APPLICATIONS

If soft switching is required only in rectifier mode, for instance in some front-end PFC converters for motor drives that operate in regenerative mode only for a short time or with a reduced current rating, a simpler topology shown in Fig. 3.26(a) can be used. The resonant inductors are shifted into the auxiliary diode bridge, so the main diodes in the charging stage will be turned off simultaneously, and the node voltages are synchronized in the resonant stage. The operation of this topology is very similar to that of the topology shown in Fig. 3.19(b), with the only difference in switch voltage waveforms occurring in the resonant stage. Since the auxiliary circuit will force voltages of the incoming switches to reach zero at the same time in the modified topology of Fig. 3.26(a), zero-voltage turn-on of the main switches can be achieved without overcharging the resonant inductors, provided the incoming switches are turned on at the right time. The key waveforms in the soft-switching commutation from D4, D6 to S3 and S5 are shown in Fig. 26(b), in which the voltages across S3 and S5 are reduced to zero at the same time, since v_b and v_c approach the positive dc link at the same time. Clearly, complete zero-voltage turn-on of the main switches is achieved. However, the control timing in the soft-switching transition needs to be adapted to the phase currents, similarly to the way it is done in the topology with coupled inductors proposed in [B51].



(a). Basic topology. The resonant inductors are shifted into the auxiliary diode bridge, so the main switch voltages are reduced to zero at the same time in the resonant stage.



(b). Operation waveforms in the commutation from D4, D6 to S3, S5.

Figure 3.26 **A simple ZVT three-phase boost rectifier with modified auxiliary circuit**. The synchronized reduction of incoming switch voltages makes it possible to achieve zero-voltage turn-on with a variable control timing.

3.4.7 CONCLUSIONS

Several new soft-switching three-phase PWM converter topologies are proposed and investigated in this section. Connected to the dc-link midpoint, the auxiliary switches in these topologies block only half of the dc-link voltage, so they have less power loss and can be implemented with faster and cheaper devices than in many other soft-switching circuits. Design issues and techniques to reduce the main switch turn-on voltages are also discussed. Two modified topologies are shown to be able to reduce switch voltages to a value close to zero without increasing snubber capacitance. An IGBT prototype converter is designed and tested, showing that above 97% efficiency in rectifier mode operation and nearly 96% efficiency in inverter mode operation have been achieved, with over 1% efficiency improvement over the hard-switching operation in both modes. Simulation results also demonstrate that the topologies proposed in this section achieve the highest efficiency improvement in both rectifier mode and inverter mode among several well-known soft-switching topologies, which makes them very attractive in medium-power, high-switching-frequency applications.

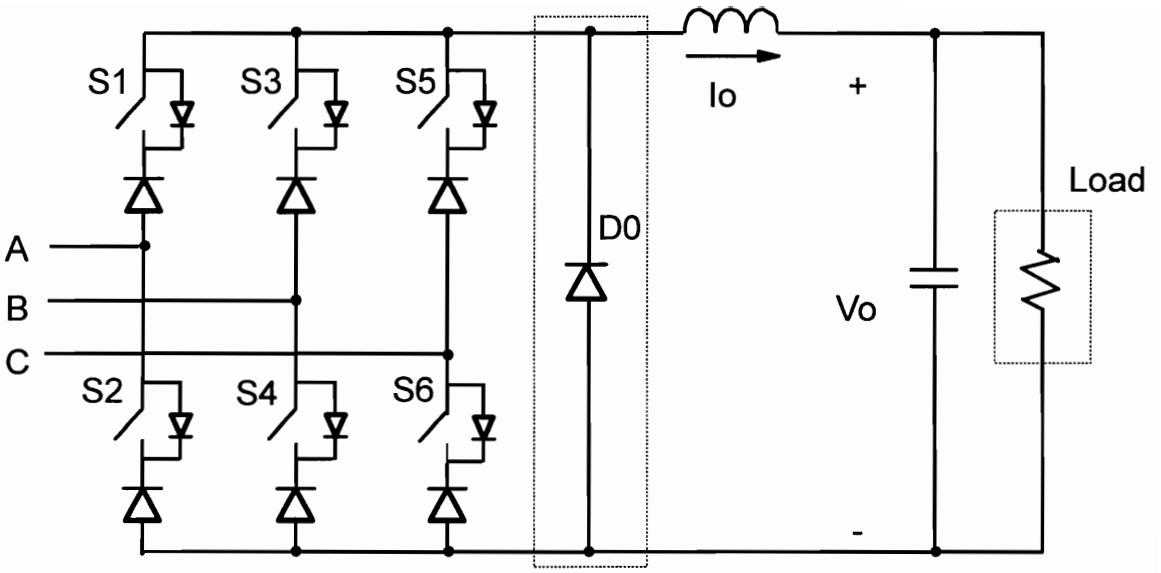
4 THREE-PHASE ZERO-VOLTAGE-TRANSITION BUCK AND BUCK-BOOST RECTIFIERS

4.1 INTRODUCTION

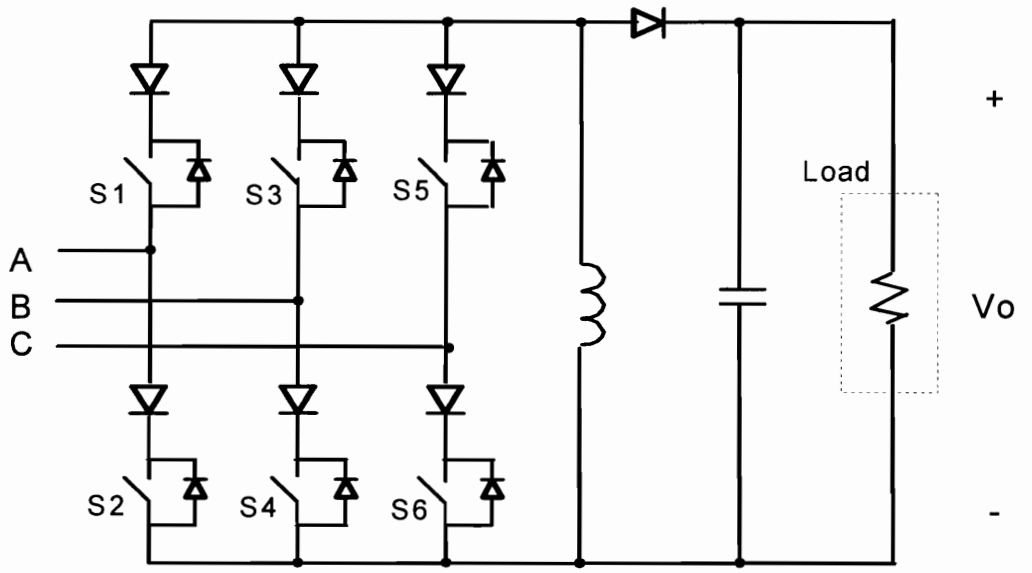
Current source converters, including current source inverters, buck, and buck-boost rectifiers, are the other widely used topology in three-phase power conversion. With the advent of self-turn-off high power devices, the application of current source inverters (CSI) is now limited only to very high power applications. The soft-switching techniques for CSIs are discussed in [D1]-[D9]. The buck-boost rectifier will not be discussed in detail, since it is rarely used. On the other hand, current source rectifiers, especially the three-phase buck rectifier, are increasingly gaining industrial acceptance because their performance contrasts with a boost rectifier's are favorable in some applications.

The basic topology of a three-phase buck rectifier is shown in Fig. 4.1(a), and the topology of a three-phase buck-boost rectifier is shown in Fig. 4.1(b). The bulky dc-link inductor behaves like a current source in both topologies. The buck rectifier has a freewheeling diode Do to reduce the converter conduction loss in the freewheeling stage. If the converter is to be operated in inverter mode also, this diode should be removed, with its electrical function replaced by shorting one or more legs in the bridge. Compared to the well-known boost rectifier, the performance differences of a three-phase buck rectifier include the following aspects:

- A boost rectifier requires a high output voltage, which causes a high voltage stress to the switches in the rectifier and its downstream converter. On the other hand, the output voltage of a buck rectifier is lower than the peak input voltage. For example, in a 380 V/460 V input system, the output voltage would be around 900 V in a boost rectifier, but can be $0 \sim 300$ V in a buck rectifier. While the boost rectifier is attractive for



(a). Three-phase buck rectifier



(b). Three-phase buck-boost rectifier

Figure 4.1 **Three-phase current source rectifiers.** The buck recifier in (a) uses a freewheeling diode to reduce the conduction loss.

relatively low input voltage, fixed output voltage applications, the buck rectifier seems more suitable with high input voltages or variable output voltages.

• The input currents of the boost rectifier are continuous, while the input currents of a buck rectifier are discrete pulses. Therefore, the input currents of the buck rectifier have higher rms values and high-frequency harmonic components than in a boost rectifier under the same input voltage and output power. Therefore, the requirements on the input filter are more aggravated in the buck rectifier than in the boost rectifier. However, the buck rectifier requires less output filtering, and its bulk dc-link inductor has usually a much lower inductance than the total of three boost inductors in a boost rectifier for the same application. The total reactive component requirement could be even lower in a buck rectifier than in a boost rectifier. Also, the total voltage swing in a buck rectifier is less than half of that in a boost rectifier, which could result in less common mode noise, and make the common mode filtering easier.

• Because the buck rectifier has a switch and a diode in series in each arm, and the input current is discontinuous, its conduction loss is always higher than the boost rectifier's. Considering that the conduction voltage drop of a diode is very close to an IGBT with the same voltage and current ratings in high power applications, the total conduction loss in the buck rectifier is more than twice higher than in a boost rectifier. The switching loss in a buck rectifier is roughly proportional to the input voltage for the same output power. At a low line condition, the buck rectifier has high conduction loss, but low switching loss; at a high line condition, the buck rectifier has low conduction loss but high switching loss. It is possible to keep the total power loss almost constant within the whole input voltage range. On the other hand, both the switching loss and the conduction loss reach their maximum at low input voltage condition in a boost rectifier, making its design optimization very difficult. The worst case power loss in a boost rectifier can be even higher than in a buck rectifier, as is illustrated by Fig. 4.8(b), to be discussed later. In addition, a boost rectifier needs additional components to limit the inrush current, resulting in additional conduction loss. As a result, the voltage and current ratings of power semiconductors, which have to be designed according to the

worst case operating condition, as well as the converter implementation cost, could be lower in a buck rectifier than in a boost rectifier.

• The buck rectifier can use open-loop or other simple current control schemes, and can control the inrush current easily by soft start of the switches. On the other hand, the boost rectifier usually requires complex closed loop current control to ensure sinusoidal current waveforms, and needs additional components to limit the inrush current. The buck rectifiers also have inherent short circuit protection, which makes them more reliable.

The choice between a buck rectifier and a boost rectifier in a specific application would involve complex trade-offs. However, a buck rectifier does offer certain advantages over a boost rectifier, and can be expected to find wide applications in high input voltage or variable output applications, such as dc motor drives, battery and SMES chargers, and magnet power supplies.

4.2 CURRENT SPACE VECTOR MODULATION

Similarly to the voltage space vectors in voltage source converters, current space vectors can be used to devise control schemes in current source converters, in which the dc-link inductor is very large and behaves like a current source in the steady-state operation. Different combinations of the bridge switches can produce different phase currents, which can be represented in the space vector form. The current space vectors and their corresponding switch combinations in a three-phase converter are shown in Fig. 4.2. The convention of switch combinations is the same as in voltage source inverters, with the additional "O" to represent the zero phase current, i.e. both switches in the phase do not conduct current. The zero current vector I_0, which is at the center of the hexagon, represents that all three input currents are zero, and can be produced by several switch combinations: either all switches are off (so the dc-link current is conducted by the freewheeling diode), or both the top switch and the bottom switch are simultaneously on in one or more legs (i.e. the bridge is shorted). According to current vector control [E5], a reference current vector I_r can be synthesized with two adjacent space vectors and a zero current vector. For example, a reference vector I_r in Sector I, as is shown in Fig. 4.2, can be synthesized by I1, I6, and a zero vector I0 with proper duty cycles. Due to the requirement of unity power factor in rectifiers, the average phase currents should be proportional to their respective phase voltages in each switching cycle, and can be controlled by adjusting the duty cycles of corresponding switches. The operation of the converter is symmetrical every 60°, and can be explained by the example of v(A)>0>v(B)>v(C), which is in Sector I, and Phase A has the highest voltage and current among the three phases. I1 is provided by turning on S1 and S4; I6 is provided by turning on S1 and S6; and I0 can be provided by turning on S1 and S2, or S3 and S4, or S5 and S6, or simply by letting the freewheeling diode conduct. Therefore, the gate drive signal of S1 can be kept on during the whole switching cycle, so the switches in the highest-

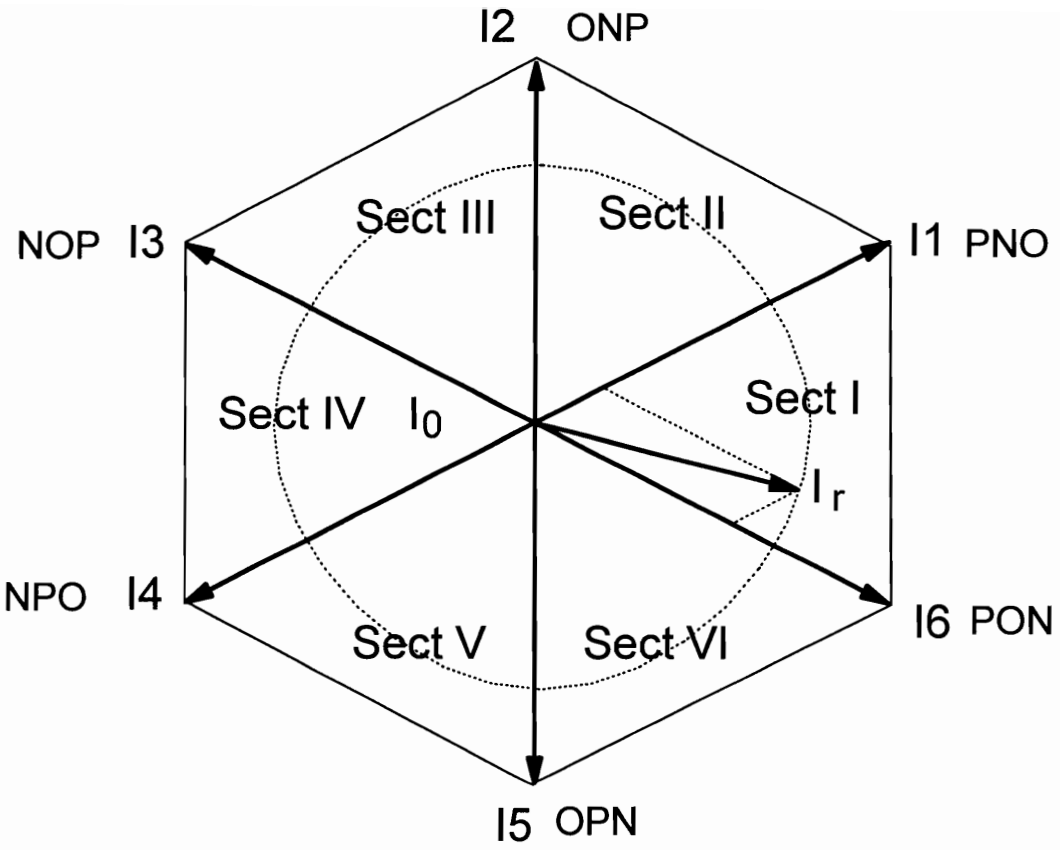
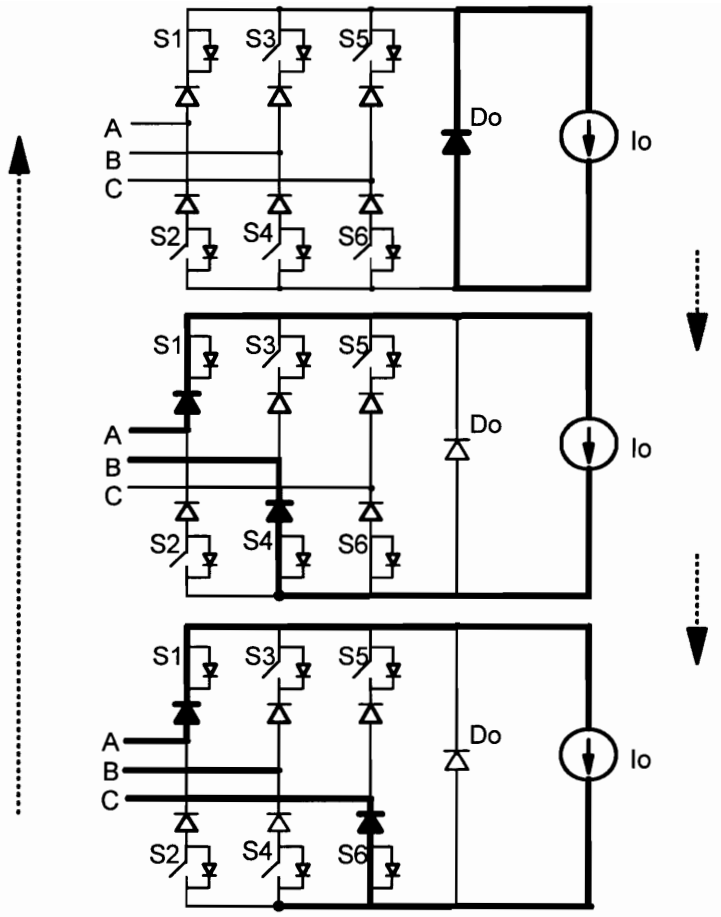


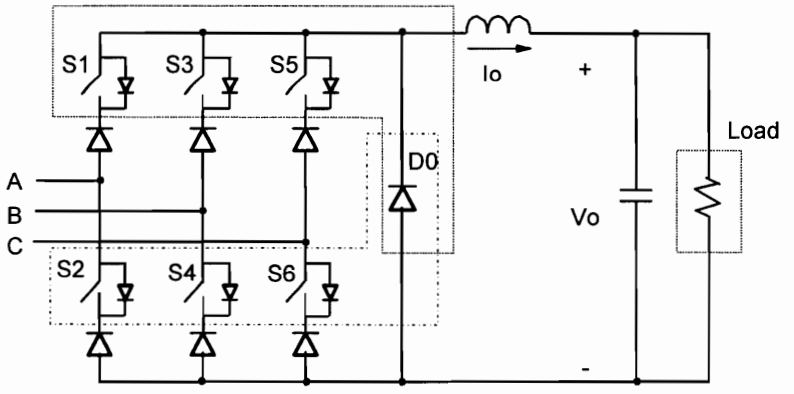
Figure 4.2 **Current space vectors in a three-phase buck rectifier**. The zero vector I_0 has several implementations with which all three phase currents are zero.

voltage phase would not be switched. To reduce the switching action and facilitate the soft-switching operation, the turn-on signals for S4 and S6 can be commanded on simultaneously at the beginning of a switching cycle. S2 can also be commanded on without affecting the converter operation. However, only S6 can conduct current at first, since the diode in the lower branch of Phase B is reverse-biased. Therefore, the actual current vector is I6. If S4 is not turned on at the beginning, it can be turned on with zero voltage as long as S6 is conducting. After S6 is turned off, S4 will start to conduct, and current vector I1 will be provided. After S4 is turned off, the converter will provide a zero vector I0, with D0 conducting . The vector sequence for this case is I0--I6--I1--I0--. Since the switches in phase A, which has the highest voltage among the three phases, are not switched, the switching loss is minimized. The modulation scheme is shown in Fig. 4.3(a). The performance of this modulation scheme would be very similar to the optimum "DD" scheme investigated for voltage source converters in [E37].

In this modulation scheme, a switch in the phase with the highest voltage magnitude (the top switch for positive voltage, and the bottom switch for negative voltage) is kept on, while all switches on the other side of the bridge are turned on at same time. For example, in the example discussed above, S1 is always on, and S2, S4, and S6 can be turned on at the beginning of each switching cycle. However, the real conducting switch is determined by the phase voltages. In the example, the priority is S6--S4--D0. S2 cannot conduct current, so its turn-on does not affect the converter operation. Due to the synchronization of switch turn-on signals, the typical turn-on commutation is always from the freewheeling diode to three switches on the same side. The six switches in a buck rectifier can be divided into two groups: the three top switches and the three bottom switches, with each group, together with the freewheeling diode, forming a generalized PWM cell. The configuration of the generalized PWM cells is shown in Fig. 4.3(b), in which S1, S3, S5, and D0 form a generalized PWM cell, and S2, S4, S6, and D0 form another generalized PWM cell. Simple soft-switching topologies can be easily derived based on the generalized PWM cell concept.



(a) Current space vector modulation for v(A)>0>v(B)>v(C)



(b). Generalized PWM cells in three-phase buck rectifier

Figure 4.3 **SVM scheme and generalized PWM cells.** The SVM scheme turns on switches of one side at the same time, so all switches are divided into two groups.

4.3 EXISTING SOFT-SWITCHING TECHNIQUES IN THREE-PHASE BUCK RECTIFIERS

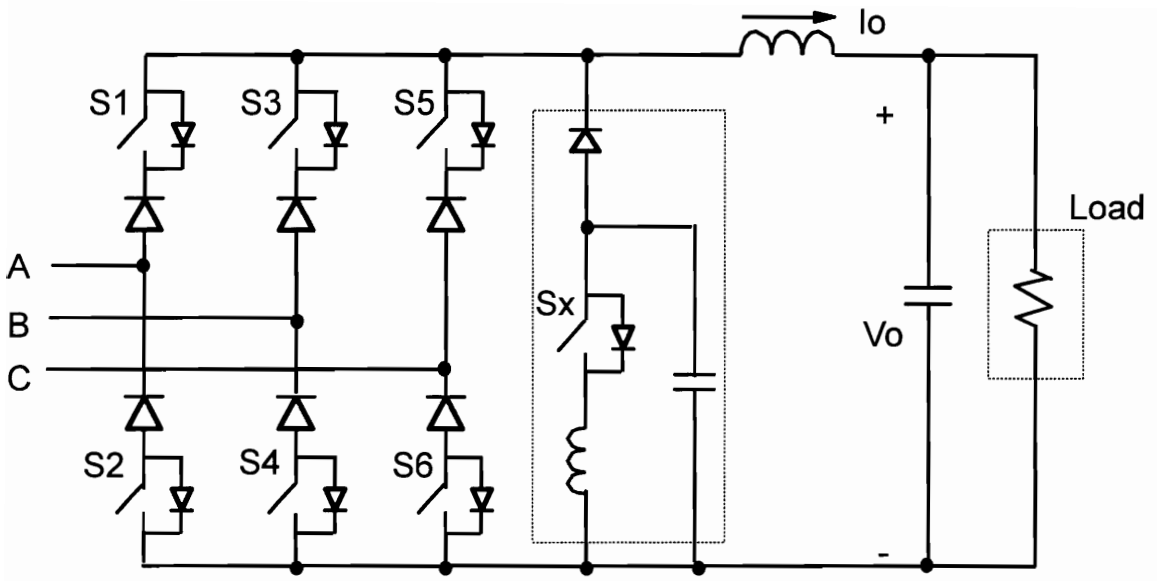
Recently, several soft-switching topologies for three-phase buck rectifier were investigated [D7] [D8] [D10] [D13], and are shown in Fig. 4.4. In these topologies, auxiliary circuits are used to shape the switch voltage to zero before the turn-on of the main switches in [D8] [D10] [D13], or to shape the switch current to zero at both turn-on and turn-off in [D7]. However, these topologies suffer from the following drawbacks:

- The soft-switching auxiliary circuits are connected to the dc link, and can shape the dc-link voltage, but cannot directly control the switch voltage. This is acceptable for very high power applications, where symmetric GTOs can be used as the main switches. In most applications, each bridge switch is implemented as a uni-directional voltage device, such as IGBT, MOSFET, MCT, or asymmetric GTO, and a diode in series; then, these schemes are not suitable because the energy of the switch junction capacitance, plus snubber capacitance if any, is trapped by the diode, and the resonance between this capacitance and the stray inductance in the bridge legs causes high voltage spike and power dissipation to the switches [D13]. To solve this problem, a snubber capacitor of a much higher capacitance than the switch capacitance has to be paralleled across each bridge diode, but then the switch turn-on voltage cannot be reduced to zero.

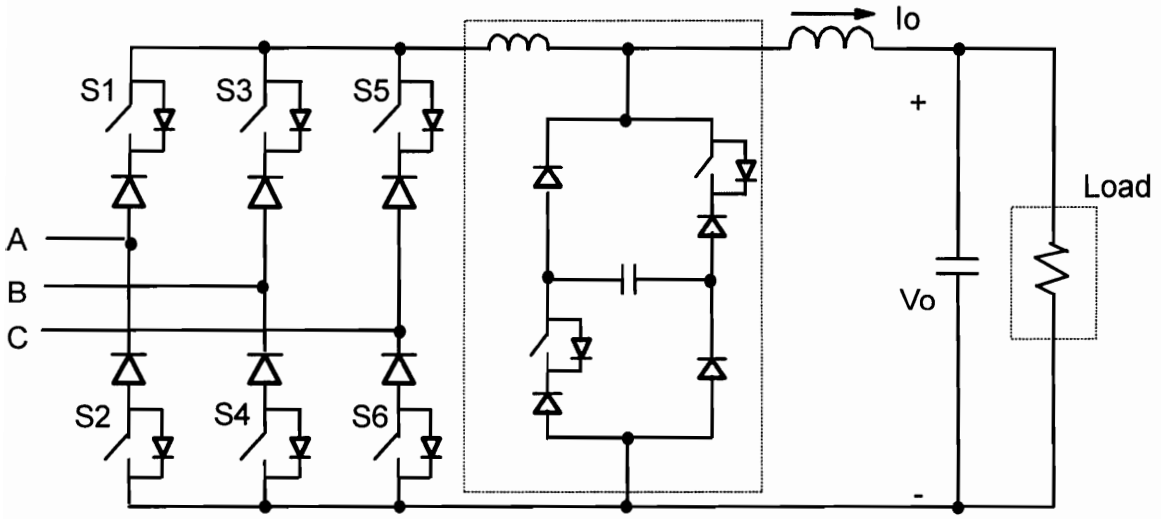
- The dc-link voltage is required to be negative in the soft-switching transition in [D8] [D10] [D13], so the dc link has to withstand bi-directional voltage. As a result, the freewheeling diode D0 has to be removed, and the conduction loss of the converter is higher than optimum.

- The soft-switching circuit consists of a resonant tank (a capacitor and an inductor) in [D7] [D10], and requires complex and accurate control timing. The voltage stress of the switches is not minimum and depends on the control timing also.

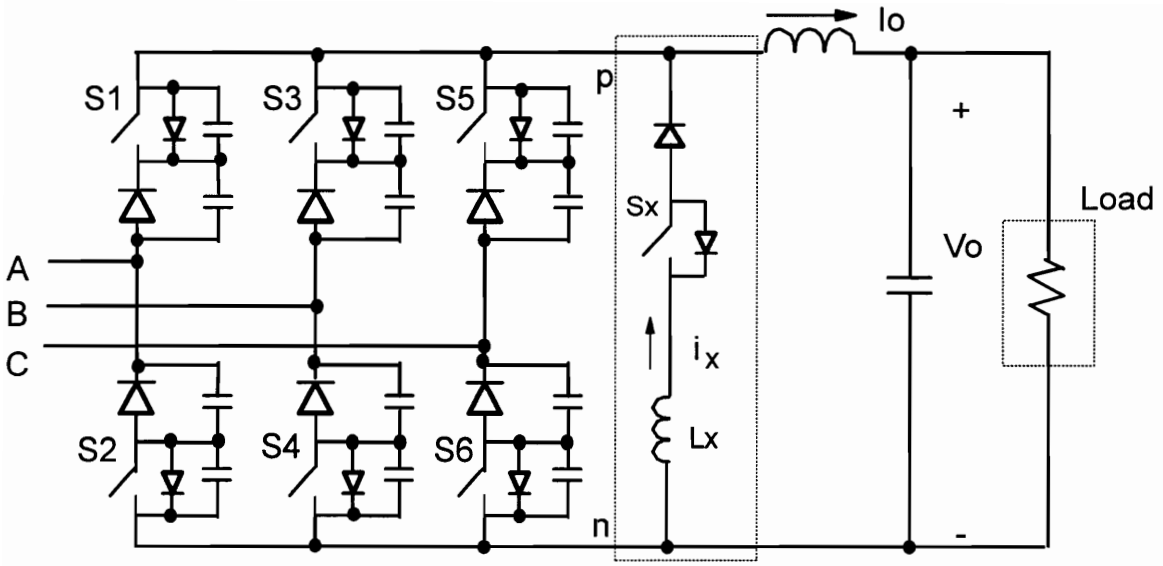
- The soft-switching circuit in [D8] [D13] requires a modified SVM scheme to



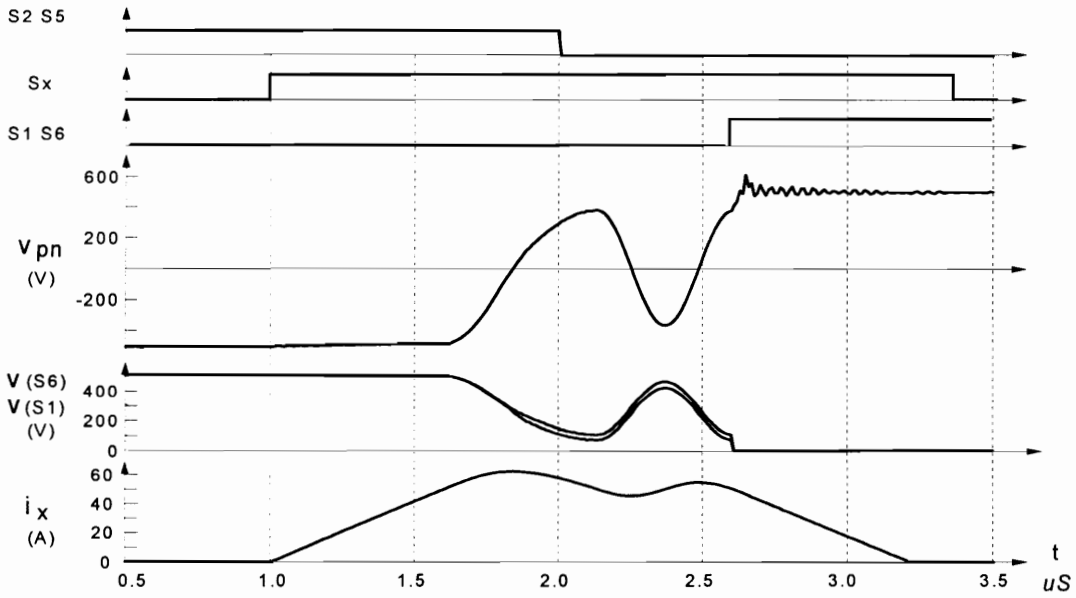
(a). Soft-switching topology in [D10]



(b). Soft-switching topology in [D7]



(c). ZVT topology in [D8, D13]



(d). Operation waveforms of the ZVT buck rectifier in [D13]

Figure 4.4 **Existing soft-switching techniques for three-phase buck rectifiers**. Auxiliary circuits are placed across the dc link, and the soft-switching operation is inefficient.

provide negative dc-link voltage to charge the resonant inductor, and this modification results in extra main switch turn-off events and more than optimum switch turn-off loss.

The simulated typical waveforms in the soft-switching transition of the topology shown in Fig. 4.4(c) are shown in Fig. 4.4(d). The simulated conditions are: Vac=500 V, Vbc=300 V, Io=50 A, resonant inductor inductance 6 uH, switch capacitance 0.3 nF each, diode snubber capacitance 5 nF each, stray inductance 20 nH in each arm. The simulation results indicate clearly that the switch voltages are oscillating before turn-on, and cannot be reduced to zero. However, since the diode reverse recovery is eliminated, and the switch turn-on voltage is relatively small, switching loss and stress reduction at turn-on is still achievable. However, the extra turn-off loss due to the modified SVM and the conduction loss increase due to the removal of the freewheeling diode can severely offset the efficiency improvement.

4.4 NEW THREE-PHASE ZERO-VOLTAGE-TRANSITION BUCK RECTIFIERS

Following the same derivation procedure as in Figs. 3.7 and 3.9, simple ZVT topologies can be easily developed for buck rectifiers by applying the ZVT mechanism to the generalized PWM cells shown in Fig. 4.3. The resultant ZVT topology is shown in Fig. 4.5. The auxiliary circuit, shown within the dotted frame, can be divided into two parts: one for the three top switches, and the other for the three bottom switches. Each part consists of an auxiliary switch, a resonant inductor, three auxiliary diodes, and one clamping diode. The parallel diode across each main switch conducts only a small current during a short time in soft switching transition, and can be the body diode of MOSFET, a small anti-parallel diode, or even the avalanche effect of IGBT or MCT. The snubber capacitors across the main switches can reduce the switch turn-off loss and voltage spike caused by the parasitic inductance. The snubber capacitor across the freewheeling diode is used to reduce the voltage spike of the dc link, and is optional.

The auxiliary circuit is used to achieve zero-voltage turn-on for the main switches, and is active only for a short period in one switching cycle. The control of the converter is basically the same as its hard-switching counterpart, so only the operation of the soft-switching transition will be discussed further. Considering the above example, the auxiliary circuit is used to help eliminate the switch turn-on loss in the transition from I0 to I6, i.e. from D0 to S4 and S6. Before this transition, D0 is conducting, switch voltage v(S2) is zero, v(S4) equals V_{AB}, and v(S6) equals V_{AC}. During the whole commutation, the dc-link inductor can be treated as a current source, since its current is constant. The complete ZVT operation is shown in Fig. 4.6 and takes the following stages:

[a] Charging Stage $[t_0, t_1]$ At t_0, Sx2 is turned on with zero current. Then the auxiliary current i(Lx2) will be established gradually as Lx2 is charged by the line voltage V_{AC}. At the same time, the current in the freewheeling diode D is reduced.

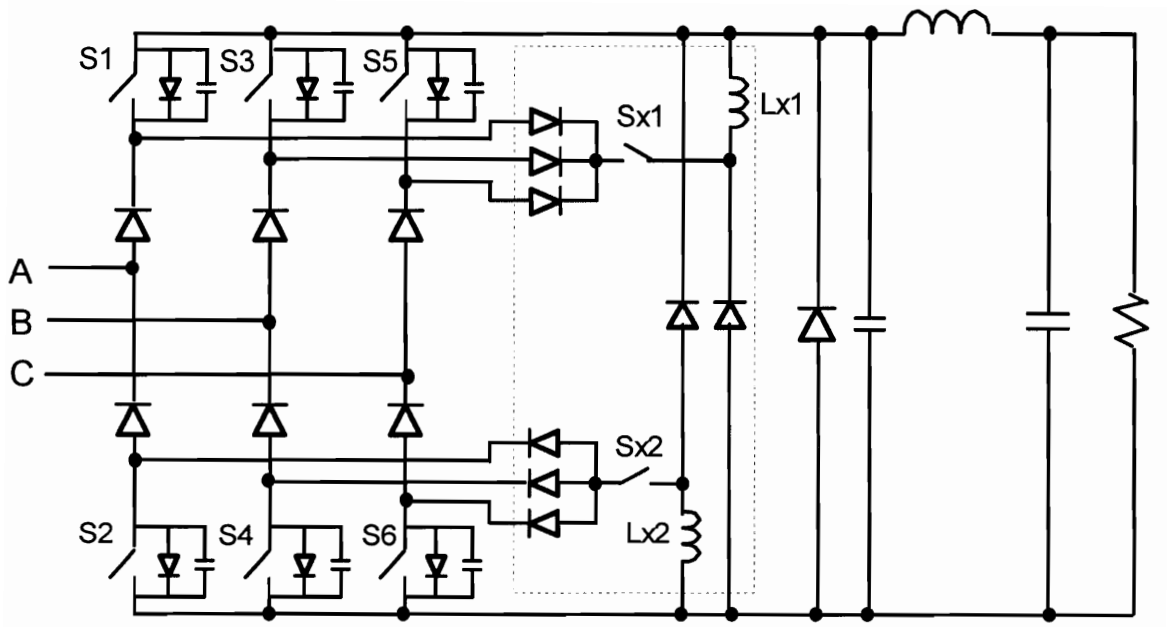


Figure 4.5 **A new ZVT topology of three-phase buck rectifier**. This topology utilizes the similar auxiliary circuit as the ZVT boost rectifier in Fig. 3.9, and is derived by applying the ZVT concept to the generalized PWM cells shown in Fig. 4.3.

[b] Resonant Stage I [t_1, t_2'] At t_1, i(Lx2) reaches the dc-link current I_{dc}, and all current is diverted out of D0, so D0 turns off naturally without reverse recovery. Then the snubber and junction capacitors of S6 and D0 start to resonate with Lx2, and the voltages across S6 are reduced gradually. During this stage, the energy of the snubber capacitors, plus any junction capacitance of S6 and D0, is transferred gradually to Lx2. The duration of this stage is determined by the difference between V_{AC} and V_{AB}. If these voltages are equal, then the converter will skip this stage and directly enter Resonant Stage II.

[c] Resonant Stage II [t_2', t_2] When the voltage across S6 is reduced to the same value as the voltage of S4, the capacitor across S4 joins the resonant process, and the voltages of S4 and S6 are reduced simultaneously.

[d] Freewheeling Stage [t_2, t_3] Since the resonant current picks up the lowest voltage path through the auxiliary diodes, the voltages across the two switches will be discharged to zero at the same time, and then will be clamped at nearly zero by the parallel diodes of these switches, and the auxiliary circuit will enter the freewheeling stage.

[e] Discharging Stage [t_3, t_4] During the freewheeling stage, S4 and S6 can be gated on. Because the initial current in Sx2 is higher than I, S4 and S6 will not conduct any current at first, so they are turned on under a zero-voltage and zero-current condition, and turn-on loss is eliminated. Then, Sx2 is turned off at t3, and the current in Lx2 is returned to the dc link through the clamping diode Dx2. As Lx2 is discharged by the dc link voltage, the energy stored in it is delivered to the output.

When the current in Lx2 is discharged to zero at t_4, Dx2 turns off naturally. To suppress the possible oscillation between the resonant inductor Lx2 and the junction capacitance of Dx2, a saturable inductor can be put in series with Lx2(as well as with Lx1) in a practical implementation. After t_4, the auxiliary circuit becomes inactive, and the converter resumes its PWM operation until the turn-on commutation in the next switching cycle. In the whole commutation process, there is no extra switching action of

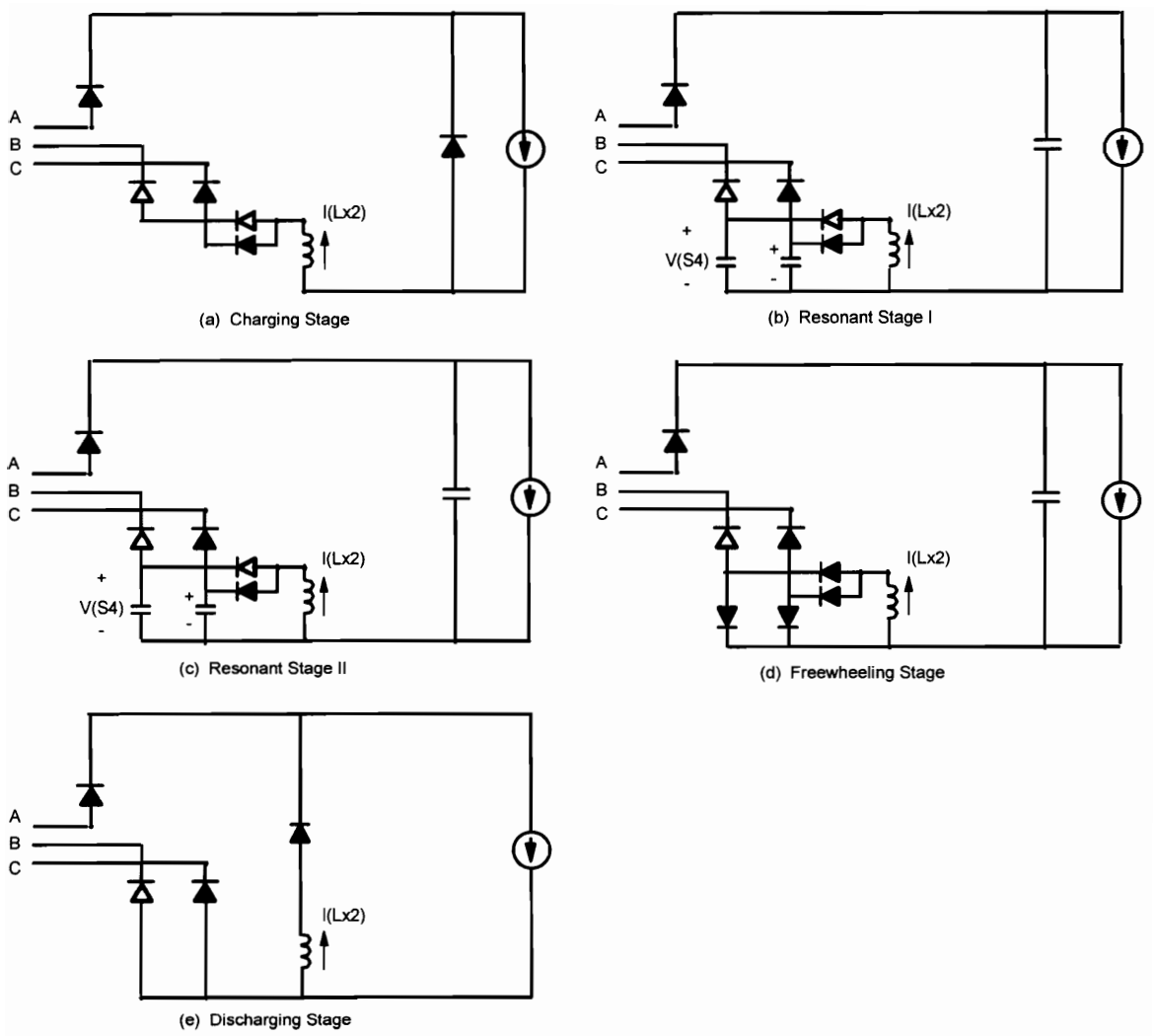
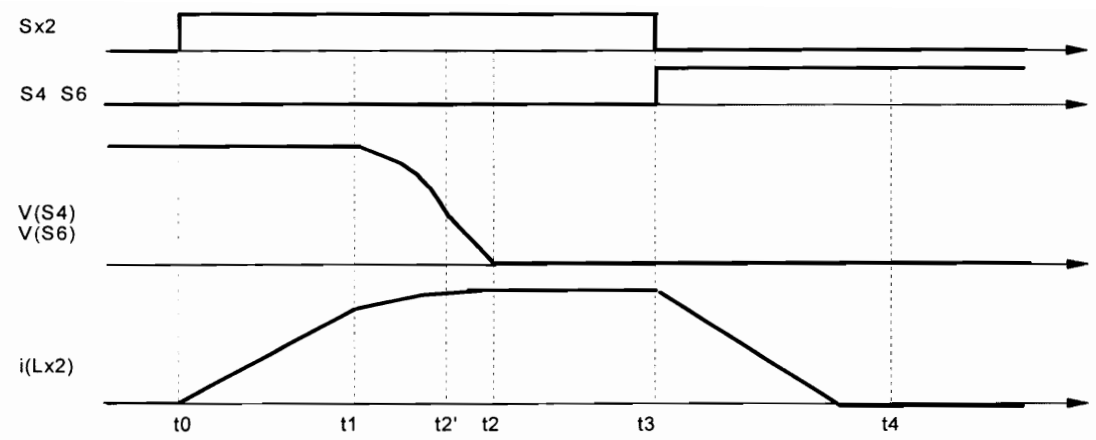


Figure 4.6 **Operating Stages during the ZVT commutation.** No extra main switch turn-off and extra space vector occur during the commutation.

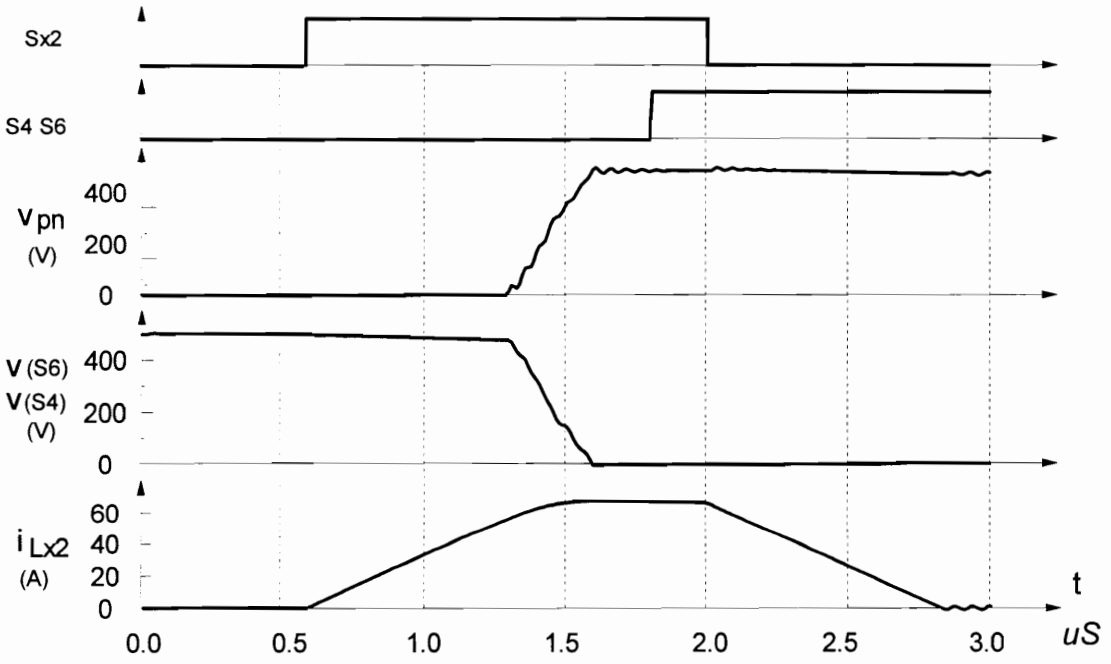
the main switches. Since the converter transfers power from the input to output during the most part of the soft-switching transition, the duty cycle loss due to the soft-switching function is also very small. Clearly, if soft switching can be achieved at full load, it can also be achieved under all load conditions with the same control timing. The voltage stress of all devices is only the peak line-to-line voltage.

The ideal waveforms in the soft-switching commutation are shown in Fig. 4.7(a) without considering circuit parasitics. The operation of this ZVT topology is also verified in simulation, with circuit parasitic inductance and capacitance taken into account. The simulated typical waveforms in the soft-switching transition are shown in Fig. 4.7(b), which completely comply with the above theoretical analysis. The simulation conditions are: Vac=500 V, Vbc=300 V, Io=50 A, resonant inductor inductance 6 uH, switch snubber capacitance 5.6 nF each, diode capacitance 0.3 nF each, stray inductance 20 nH in each arm. An RECD snubber is used for each auxiliary switch to reduce its dv/dt, and each clamp diodes of the resonant inductors are implemented as three diodes connected to the bridge switches. The different operating stages can be easily identified from the waveforms. The simulation results indicate clearly that the switch turn-on voltages and diode reverse recovery are completely eliminated, so the switch turn-on loss is completely nullified. The turn-off process of the main switches is the same as in a conventional PWM rectifier. However, because all snubber capacitor energy is recovered in the zero-voltage turn-on transition, a fairly large capacitor snubber can be used across each main switch, so that the turn-off loss and stress of the switches can be reduced.

Simulations are performed with the same device parameters as in Table 3.2 to evaluate performances of the proposed technology. The main switches are CM50DY-24H, with 2.7 nF-snubber capacitance, and the auxiliary switches are three IXTN21N100 (1100 V, 0.55 Ohm). The resonant inductors have an inductance of 6 uH, with a 7.5-mΩ series resistor representing their power loss. The dc-link inductance is 300 uH. The similation conditions are: input rms line voltage is 305 V, and the output voltage is 300 V. Fig. 4.8(a) shows the input current waveforms with a 5uH, 20 uF LC filter, having



(a). Ideal waveforms

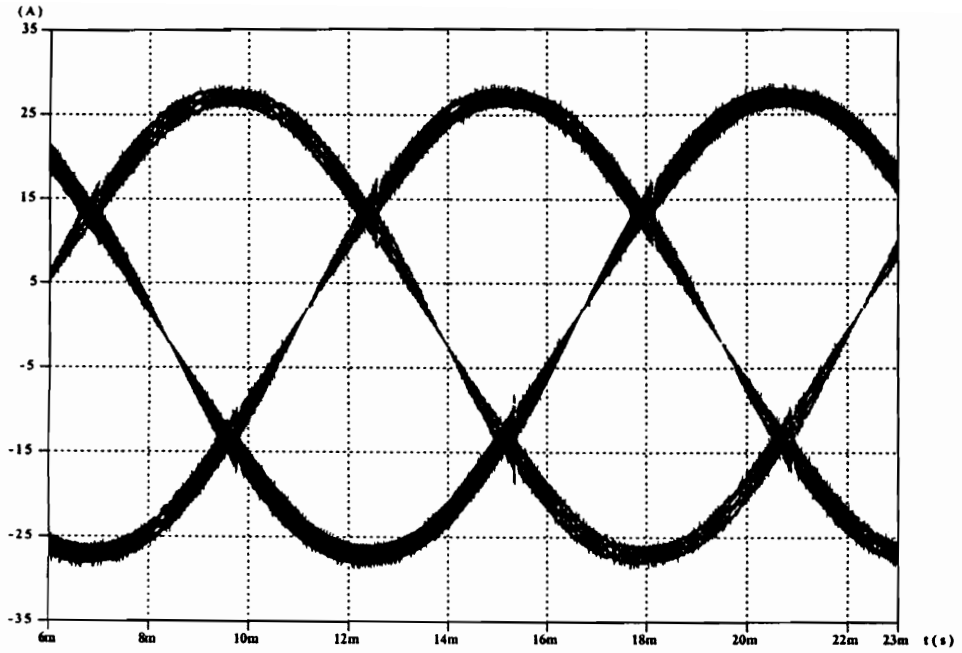


(b). Simulation waveforms

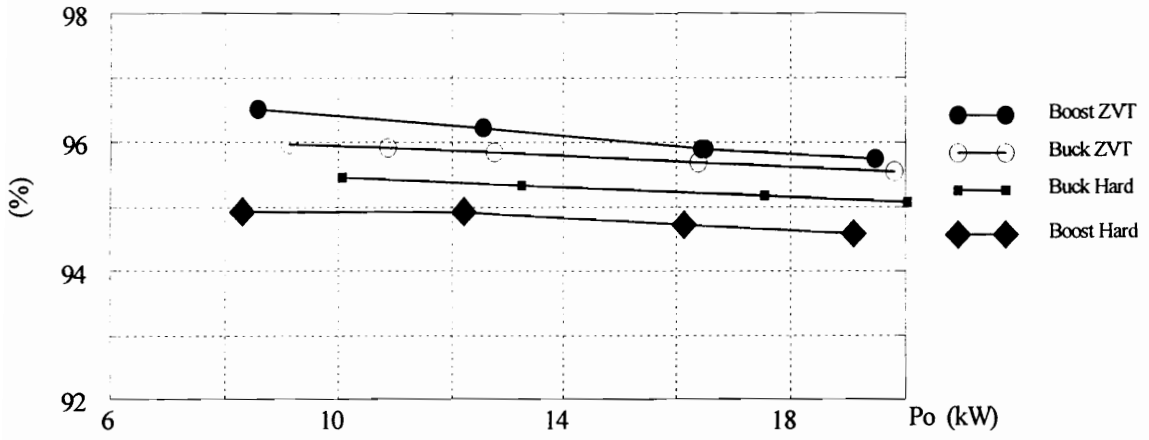
Figure 4.7. **Key waveforms of the ZVT commutation in a buck rectifier.** The only difference between theoretical waveforms and simulated waveforms is the small ringing of the simulated voltages and currents due to the parasitic inductance.

around 2% THD and 2 A peak-peak ripple. Compared with the current waveforms of a boost rectifier in Fig. 3.17(a) under the same operating conditions, the current ripple and distortion of the buck rectifier are much smaller, although much lower total inductance is used (315 uH in the buck rectifier vs 1200 uH in the boost rectifier). Fig. 4.8(b) shows the efficiency under both soft-switching and hard-switching conditions. It can be seen clearly that about 0.5% efficiency improvement has been achieved. The efficiency improvement is relatively low because the switching loss is low at low line condition. It can be expected that the efficiency improvement will be much higher at high-line conditions. The efficiency of boost rectifiers with the same input conditions is also shown in Fig. 4.8(b) for the purpose of comparison, in which Boost ZVT refers to Scheme I in Section 3.3. The output voltage of the boost rectifiers are set to be 900 V. The hard-switching buck rectifier has a higher efficiency than the hard-switching boost rectifier, due to the much reduced switching loss. However, the ZVT buck rectifier has a lower efficiency than the ZVT boost rectifier with the same input conditions, since the conduction loss in a buck rectifier is higher than in a boost rectifier. Because the output of a buck rectifier is much lower than in the boost rectifier, the downstream converter would be much easier to design, and could have a higher efficiency than with the high dc-link voltage of a boost rectifier. Besides, the inrush current control switch in a boost rectifier will cause certain efficiency reduction. Therefore, the system efficiency with a buck rectifier would be comparable to, or even higher than the system efficiency with a boost rectifier.

In the topology shown in Fig. 4.5, the auxiliary switches should be implemented as MOSFETs due to their hard turn-offs. If IGBT devices are to be used as the auxiliary switches, the magnetic feedback techniques presented in [A33] [A34] can be utilized to get nearly zero-current turn-off of the auxiliary switches. An example is shown in Fig. 4.9. The operating stages and main switch voltage waveforms of this topology are similar to those shown in Figs. 4.6 and 4.7, but now the control timing in the ZVT transition should be adjusted according to the dc-link current.



(a) Waveforms of input currents (with an LC filter of 5 uH, 20 uF)



(b) Efficiency comparison at 3X305 V input, 300 V output

Figure 4.8 **Simulation results of ZVT buck rectifier.** The switching frequency ripple and low frequency THD of the input currents are significantly lower than those of the boost rectifier shown in Fig. 3.18(a), under the same operating conditions. Buck rectifier has higher efficiency than boost rectifier in the hard-switching operation due to its lower switching loss, but lower efficiency in the soft-switching operation due to its higher conduction loss.

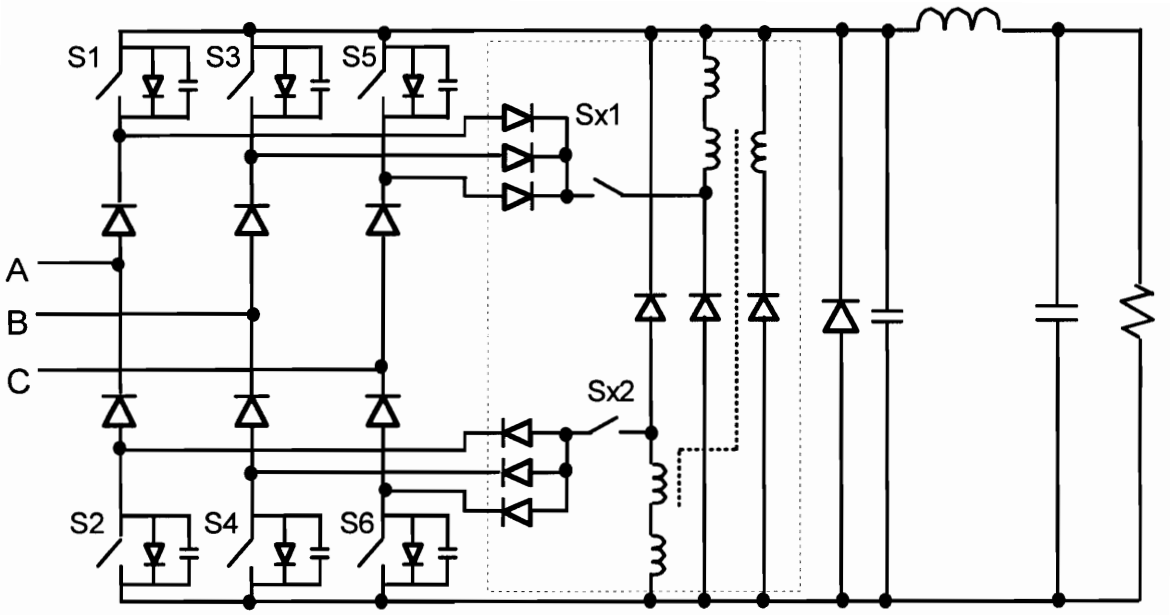
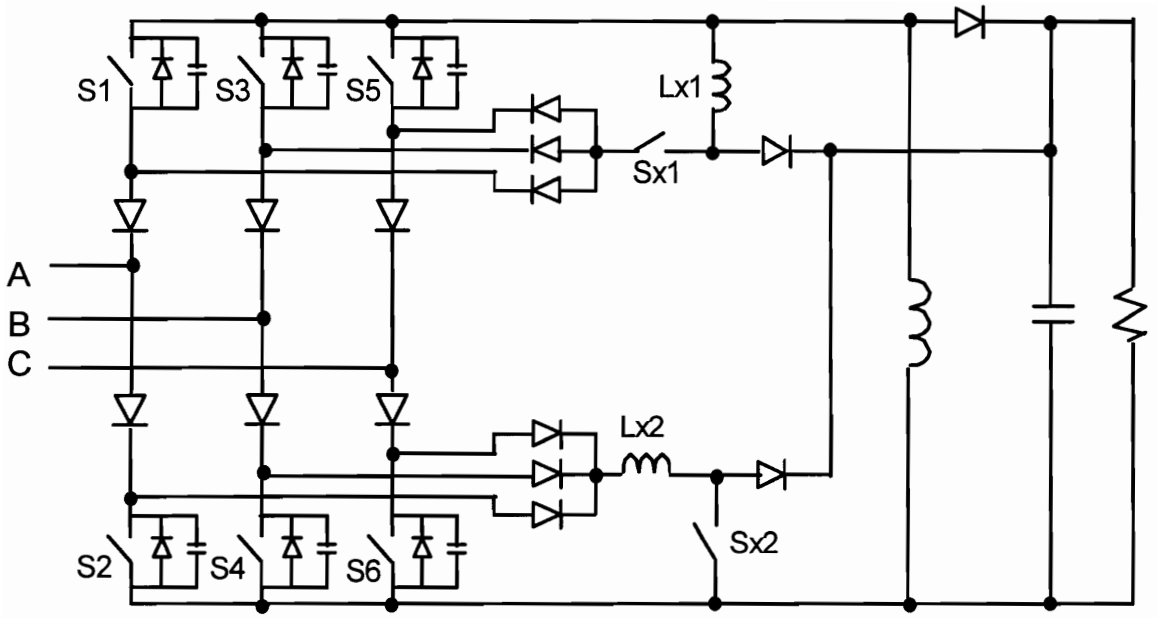


Figure 4.9 **Modified three-phase ZVT buck rectifier.** Coupled inductors are used to reduce the conduction loss and turn-off loss of the auxiliary switches.

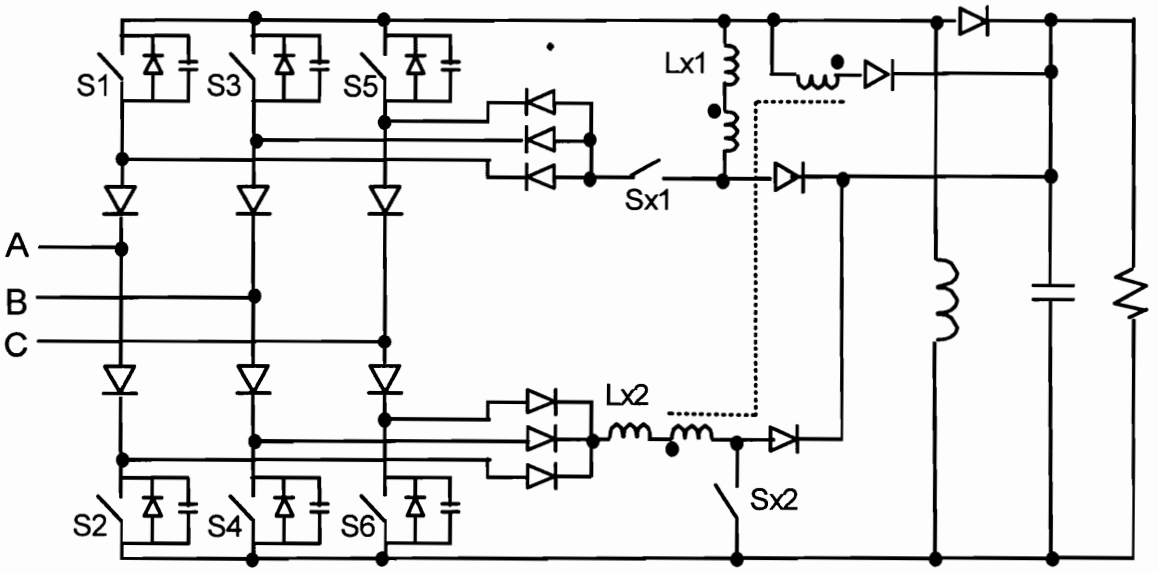
4.5 THREE-PHASE ZERO-VOLTAGE TRANSITION BUCK-BOOST RECTIFIERS

A boost rectifier can only have an output voltage higher than its input line voltage peak, while a buck rectifier can only output a voltage lower than 87% of its input line-line voltage peak. If the input or output voltage is required to vary in a wide range, then a three-phase buck-boost rectifier can be used. The above soft-switching techniques can also be easily applied to the three-phase buck-boost PWM rectifier, as illustrated in Figs. 4.10(a) and (b). The major advantage of these topologies is that any output voltage can be obtained, so the converter can work with wide input and output voltage ranges. The operation of the auxiliary circuit is very similar to that of the ZVT buck topologies of Figs. 4.5 and 4.9.

The most severe disadvantage of a buck-boost rectifier is that the inductance and current of the bulky inductor are much higher than in a boost or buck rectifier. As a result, the buck-boost rectifier is inferior in physical size and circuit efficiency, which severely limit its applications. Nonetheless, it provides an alternative for certain applications.



(a). ZVT three-phase buck-boost rectifier



(b). Modified version with coupled inductor

Figure 4.10 **Three-phase ZVT buck-boost rectifier**. The topology in (b) utilizes a coupled inductor to reduce the power loss of the auxiliary switches.

4.6 CONCLUSIONS

Novel zero-voltage transition topologies for three-phase buck and buck-boost rectifiers are presented. With the help of a low-power auxiliary circuit, the main switches are now all turned on with zero voltage, and therefore without any turn-on loss theoretically. Snubber capacitors can be used to reduce the switch turn-off loss and clamp the voltage spike during the turn-off transients. The proposed topologies can completely recover the snubber capacitor energy, and absorb the resonance between the snubber capacitors and stray inductance in the bridge legs. Therefore, the switch voltage stress is kept at minimum. The polarity of the dc-link voltage does not change in the soft-switching transition, which allows the use of a freewheeling diode and optimum SVM schemes to minimize the conduction loss and switching loss of the converter.

Due to the reduced switching loss, these soft-switching converters can operate at a much higher switching frequency, and therefore can achieve a higher power density and a better control performance than conventional hard-switching converters.

5 ZERO-VOLTAGE-TRANSITION DC-LINK TECHNIQUES FOR THREE-PHASE AC-DC-AC PWM CONVERTERS

5.1 INTRODUCTION

A simple way to implement the soft-switching function in a three-phase converter is to apply the soft-switching scheme to the dc link, so the auxiliary circuit can be simplified, because it doesn't need to deal with six main switches individually. A common practice of the existing dc-link soft-switching techniques [B9]-[B23] is to drive the dc-link voltage to zero before the main switches' turn-on, through the use of a parallel resonant circuit across the dc link. However, the resulting soft-switching schemes require additional dc-rail components (switches or inductors) in the main power path, which cause high voltage stress or high power loss.

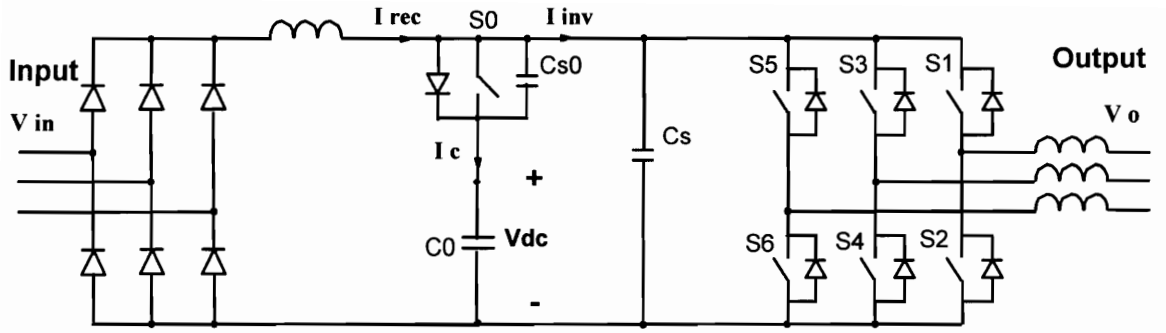
Many three-phase power conversion systems take the structure of ac-dc-ac conversion, i.e. have an ac-dc source converter (rectifier), and a dc-ac load converter (inverter). For example, in most variable speed ac motor drives, a three-phase diode rectifier, or in some cases a PWM rectifier, is used to get power from the utility, while a three-phase voltage source inverter (VSI) is used to control the motor. The dc link is common to both the rectifier and the inverter. An effective dc-link soft-switching scheme for this type of applications would be to shape the common dc-link voltage to zero, allowing the switching actions of both the rectifier and the inverter during the zero link voltage period to have low switching loss. The operation of the rectifier and that of the inverter can also be coordinated, so that the soft switching of power switches are achieved at the same time in both converters. In this way, a single set of soft-switching circuit could serve all switches in both the source converter and the load converter, simplifying the soft-switching auxiliary circuit and reducing its power loss at the same time. The techniques used will be basically similar to the dc-link commutation schemes in [B13]-

[B22], but the power rating, and therefore the implementation cost, will be lower, because now the current in the auxiliary circuit is only the difference between the inverter dc-link current and the rectifier dc-link current. The soft-switching converters will still be controlled in a PWM manner, and have control characteristics similar to those of a PWM converter. Most existing dc-link zero-voltage switching techniques use this principle at the switch turn-on, but it can also be applied to the switch turn-off, or both. Generally, it is not very desired to force the dc-link voltage to zero for every switching action, because this will result in high auxiliary circuit power loss, and low dc-link voltage utilization. Instead, the soft-switching circuit should be used only to reduce the dominant switching loss, and can be actuated only once in a switching cycle through the proper design of the converter modulation schemes.

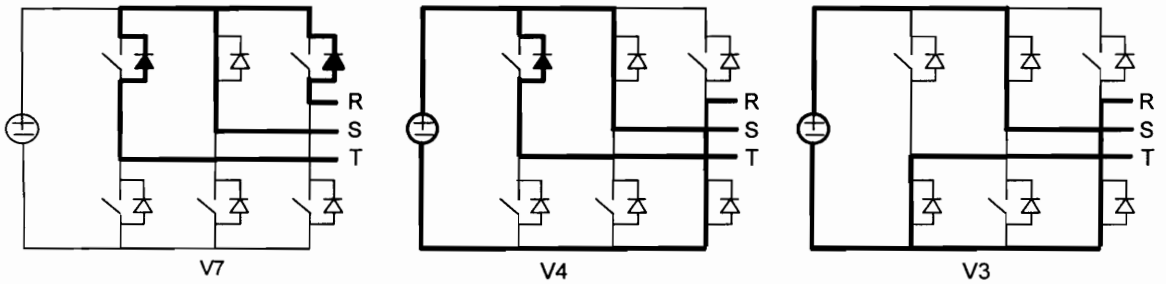
5.2 ZVT DC-LINK SCHEMES FOR SYSTEMS WITH A DIODE RECTIFIER

The simplest, but yet widely used front-end rectifier is a diode bridge. To limit the current peak and improve the power factor of a diode rectifier in high power applications, a bulky dc-link inductor is usually used. This bulky filter inductor keeps the dc-link current almost constant in the steady-state operation, so that the rectifier behaves like a current source on the dc link. Then a very simple soft-switching scheme, shown in Fig. 5.1(a), can be developed, taking the advantage of the current source. The only modification to the conventional PWM converter topology is that a dc-link clamp switch S0 is added between the bulk capacitor and the dc-rail of the inverter, so that the dc-link voltage can be shaped to zero when soft switching is desired.

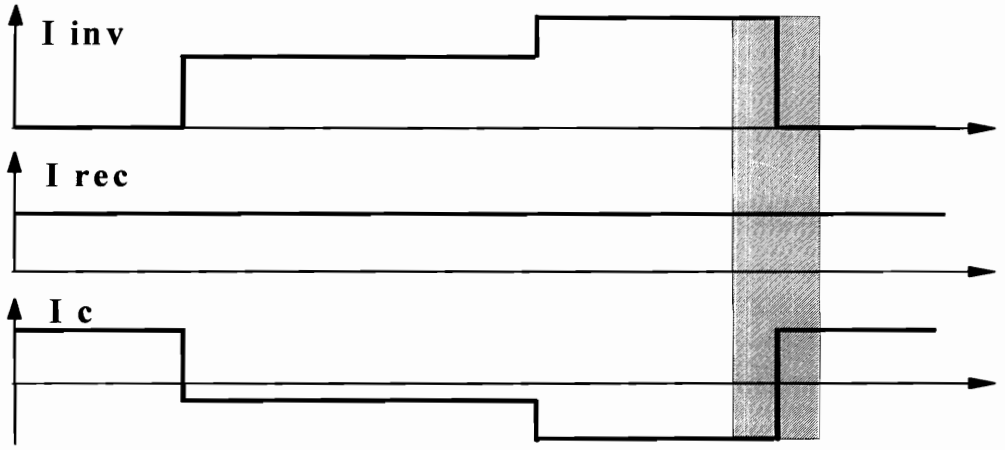
Nowadays, IGBTs are increasingly used in three-phase power converters. For many low-voltage IGBTs, the dominating switching loss is the switch turn-off loss, which can be reduced with this simple soft-switching topology. The rectifier dc-link current I_{rec} can be assumed to be constant in a switching cycle, and equal to the average current of the inverter dc-link current I_{inv}. A multi-stage filter may be required to reduce the pulsation of I_{rec} without using too large an inductor. However, the output stage of the filter should still behave like a current source. To reduce the intervention of the auxiliary circuit, the turn-off events of the inverter switches are synchronized in each switching cycle, so that before the turn-off, I_{inv} is at its maximum, and I_c is negative, so it can be used to discharge the dc-link voltage V_{pn} to zero. The operation of the converter will be described with the example of $V_s > 0 > V_t > V_r$, $i_s > 0 > i_r > i_t$. The reference directions of the currents are illustrated by arrows. According to the space vector modulation (SVM) theory, the inverter can be controlled with V3(NPN), V4(NPP), and V7(PPP). The modulation scheme for this example is shown in Fig. 5.1(b). The largest phase current (i_s in this case) is not switched, since S4 is kept on.



(a). Topology



(b). Space vector modulation scheme of the inverter with switch turn-off synchronized



(c). DC-link currents within a switching cycle

Figure 5.1 **Soft-switching dc-link ac-dc-ac converter with a diode rectifier.** The difference between *Iinv* and *Irec* at switch turn-off can be used to discharge the dc-link voltage to zero.

As mentioned earlier, I_{rec} can be considered constant during the soft-switching transition, and the rectifier is assumed to be a constant current source in the following analysis. The dc-link currents in a switching cycle are shown in Fig. 5.1(c). The soft-switching commutation is between V3 and V7, and will take the following operating stages:

(a). [t0, t1] Prior to entering the zero vector, the inverter is in V3. At t0, S0 is turned off. The turn-off current $I_c(0)$ is less than zero, since I_{rec} is practically constant for the whole switching cycle, and I_{inv} at t0 is much higher than its average value, considering the duty cycles and current ripple. The negative current I_c which was conducted by S0 will discharge the equivalent snubber capacitor, $Cs0 + Cs$, until $Vpn = 0$. The snubber capacitors should be designed to be large enough for the turn-off loss of S0 to be negligible.

(b). [t1, t2] After V_{pn} reaches zero at t1, all diodes in the inverter bridge will start to conduct and clamp V_{pn} at zero.

(c). [t2, t3] Then at t2, S1 and S5 in the inverter can be turned off. I_{rec} will start to charge the equivalent snubber capacitor. This is similar to a heavily snubbered turn-off, and the turn-off current now is reduced to I_{rec}; therefore, the turn-off loss is much reduced.

(d). [t3, t4] After t2, V_{pn} will linearly increase, due to I_{rec}'s charging Cs + Cs0. When V_{pn} reaches V_{dc} at t3, D0 starts to conduct and clamp V_{pn} at V_{dc}. The charging process is stopped, so S0 can be turned on with zero voltage at t4.

The above process is shown in Fig. 5.2, and the key waveforms during the soft-switching commutation are shown in Fig. 5.3. The charging and discharging times of the dc-link voltage are load-dependent. When the load currents are small, it may take a long time to charge or discharge the snubber capacitors in the soft-switching transition. To avoid unnecessary duty cycle loss, the soft switching can be disabled at light load.

In a conventional topology, a capacitor snubber, which is used to reduce the switch turn-off loss, results in additional turn-on loss, either in the switch or in a resistor. As a

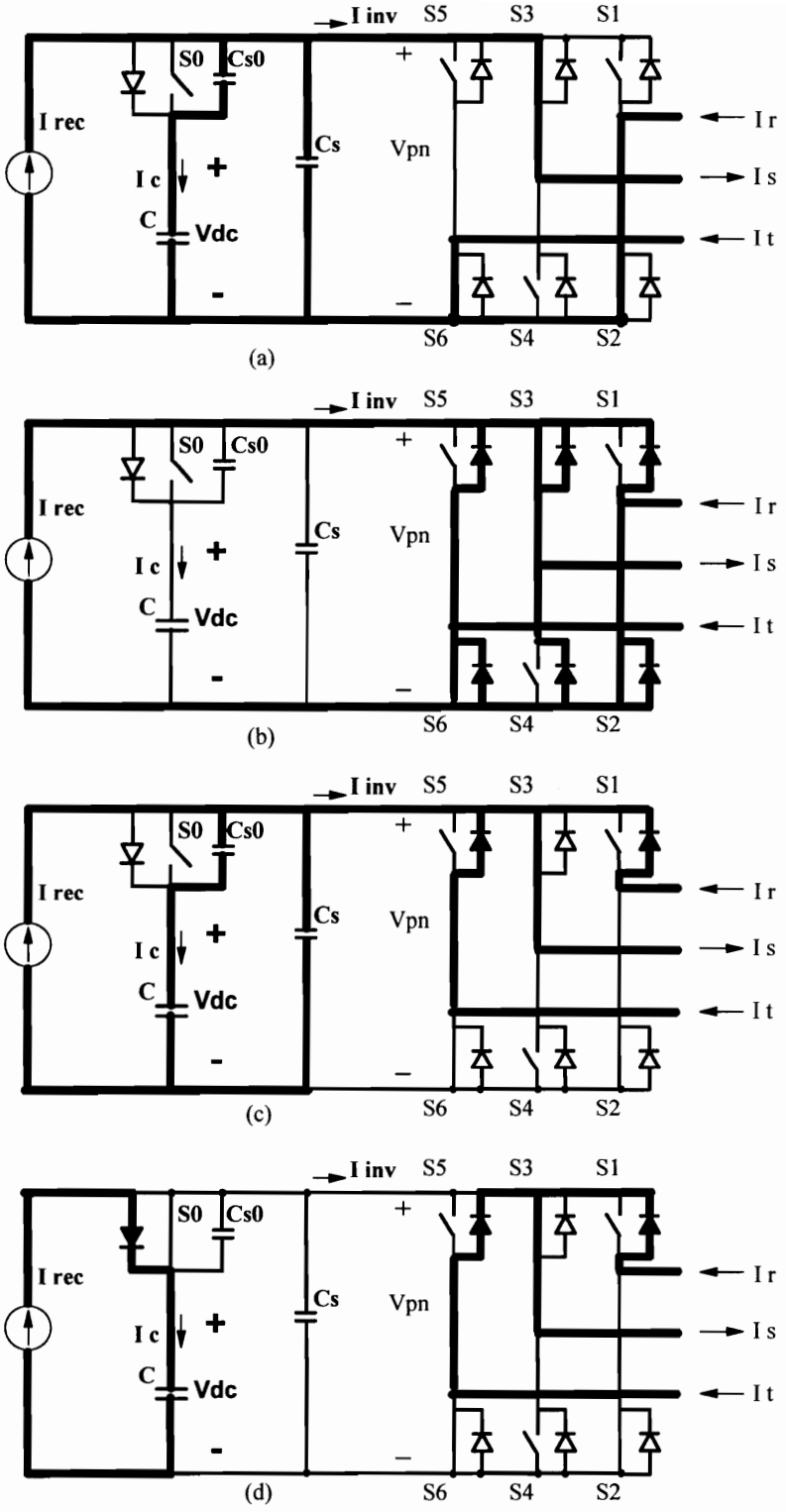


Figure 5.2 Operating stages in soft-switching turn-off transition.

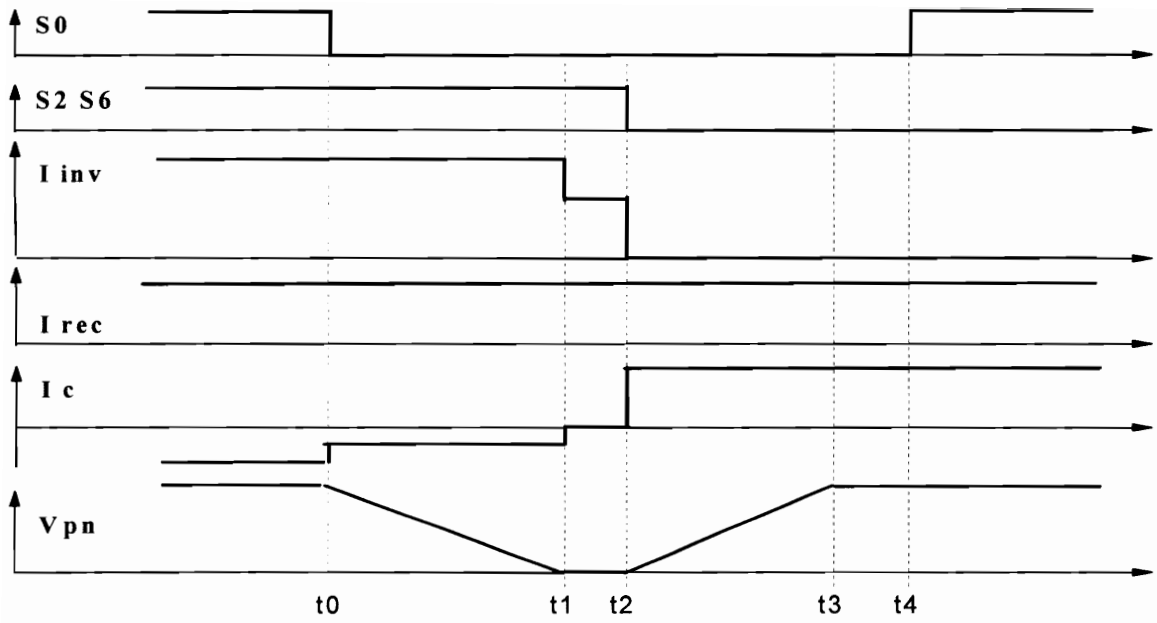
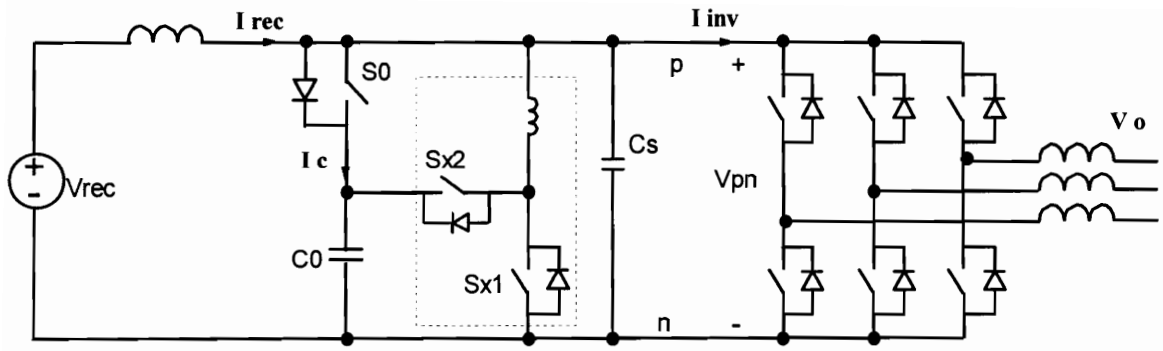


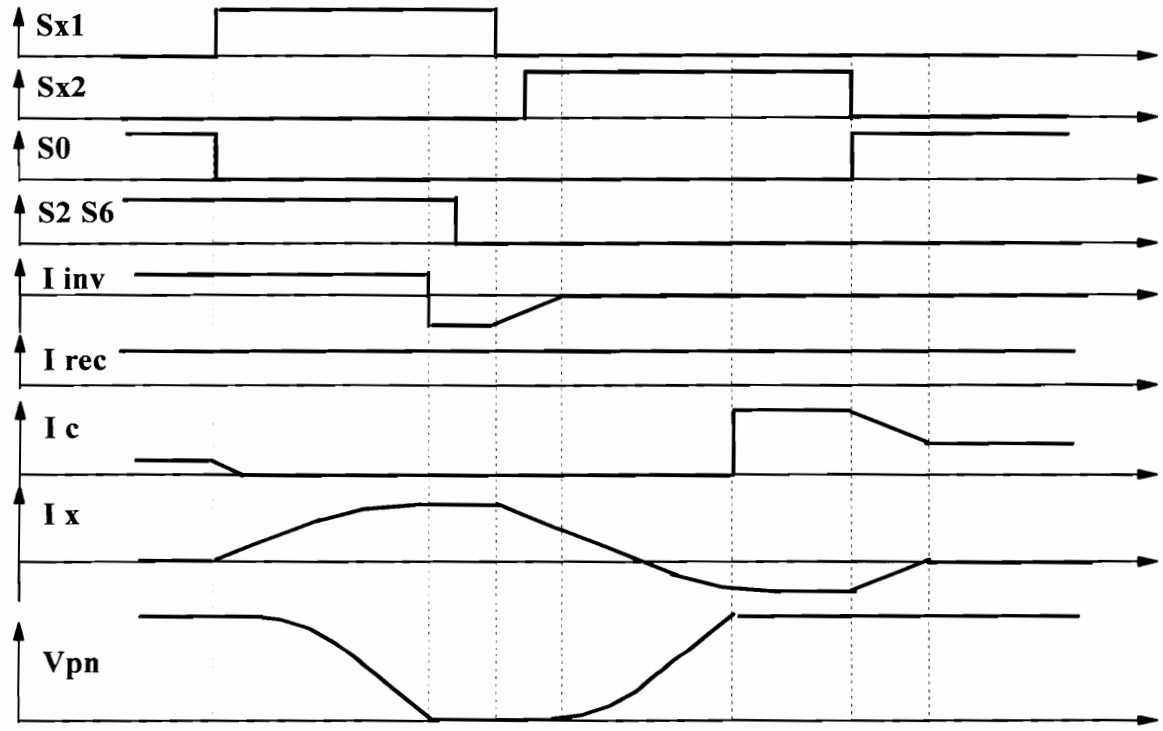
Figure 5.3 **Key waveforms in the soft-switching commutation**. The main switches are turned off with zero voltage, and the clamp switch S0 is turned on with zero-voltage. The capacitor snubbers of Cs and Cso reduce the turn-off loss of switches.

result, the use of snubber capacitors in a hard-switching converter usually increases total power loss. Therefore, the size of the snubber is very limited. Besides, a large snubber directly across each switch causes more waveform distortion in a three-phase inverter when the phase current is small due to the "zero-current clamp" effect. The essence of this topology is to separate the turn-off capacitor snubber from the switch turn-on loss. In the soft-switching topology shown in Fig. 5.1(a), the energy of snubber capacitors Cs and Cs0 is always delivered to the output, and does not cause any additional switch turn-on loss. Therefore, the snubber capacitors can be designed to be large enough to reduce the switch turn-off loss efficiently. Since the function of Cs and Cs0 is redundant, they can also be combined into one. The cost of the soft switching is mainly the power loss of S0. The maximum average current of Sc is usually below 1/3 of the maximum average value of I_{rec} or I_{inv} when the output voltage of the inverter changes from zero to its maximum value, and Sc is always turned on with zero voltage. Therefore, the power loss of S0 is moderate, and significant efficiency improvement can be achieved through the soft switching of inverter switches.

Usually, the change of the inverter currents is not very fast, and I_{rec} can follow the average value of I_{inv} pretty well, so the above soft-switching function can be achieved. In case of fast inverter current changes, I_c might be positive at t0, and an additional ZVT circuit should be used to shape V_{pn} to zero, as is shown in Fig. 5.4(a), in which Sx1 is to help bring the dc-link voltage to zero, and Sx2 is to help bring the dc-link voltage to the clamp voltage when I_{rec} is too small. The key operation waveforms in the soft-switching commutation are shown in Fig. 5.4(b), to illustrate the operation of this topology. Another advantage of this topology is that the duration of the dc-link zero-voltage condition after the main switches are turned off is now controlled by the control timing of Sx1, so the snubber capacitor Cs can be reduced without affecting the turn-off loss of the main switches. The addition of auxiliary switches can significantly improve the performance of the original topology, and should be considered for high-performance applications.



(a). A modified topology to achieve soft-switching under any operating condition



(b). Key operating waveforms in soft turn-off commutation

Figure 5.4 **A modified soft-switching dc-link topology with a diode rectifier.** The addition of a ZVT auxiliary circuit can ensure the charging and discharging of the dc-link voltage under any operating conditions. The current in the auxiliary circuit is determined by the difference between *Iinv* and *Irec*. The zero-voltage condition of the dc-link can be kept for as long as desired, and Cs can be very small. This topology can also be used to achieve zero-voltage turn-on for the main inverter switch.

Since the dc-link voltage in Fig. 5.4 can always be controlled by the auxiliary circuit, any soft-switching function can be achieved in this topology. For example, it can be easily controlled to provide zero-voltage turn-on of the main switches if wanted. In that case, the snubber capacitors can be distributed across each main switch to reduce its turn-off loss, and the turn-ons of the inverter switches should be synchronized. The converter operation would then be very similar to that in [B17], but the auxiliary circuit would have a much lower power loss, since its current rating is much lower. The power loss of the auxiliary switches can be further reduced with coupled inductors as discussed in [A33] if desired.

The topology shown in Fig. 5.1(a) can be compared with the one proposed in [B25]. Both are very simple, and provide soft turn-off function for inverter switches. However, in [B25], the dc-link switch is in the main power path, and has a much higher power loss than the clamp switch has in Fig. 5.1(a). In addition, in order to charge the snubber, the main switches are controlled to reverse the dc link current in each switching cycle in [B25], which results in a much higher switch turn-on loss and circulating energy. Topologically, the proposed converter is similar to the ZVS notch inverter in [B47], which has a small dc-link inductor and a clamp circuit, and provides zero-voltage turn-on for the main switches. In [B47], however, the clamp voltage, which is used to discharge the dc-link inductor before main switches are turned on, is significantly higher than the input voltage. In addition, the non-zero-voltage turn-on of the clamp switch limits the size of snubber capacitors, and thus also their capability to reduce switch turn-off loss. It can be expected that the techniques proposed in this section have a significantly higher efficiency than the ZVS notch inverter.

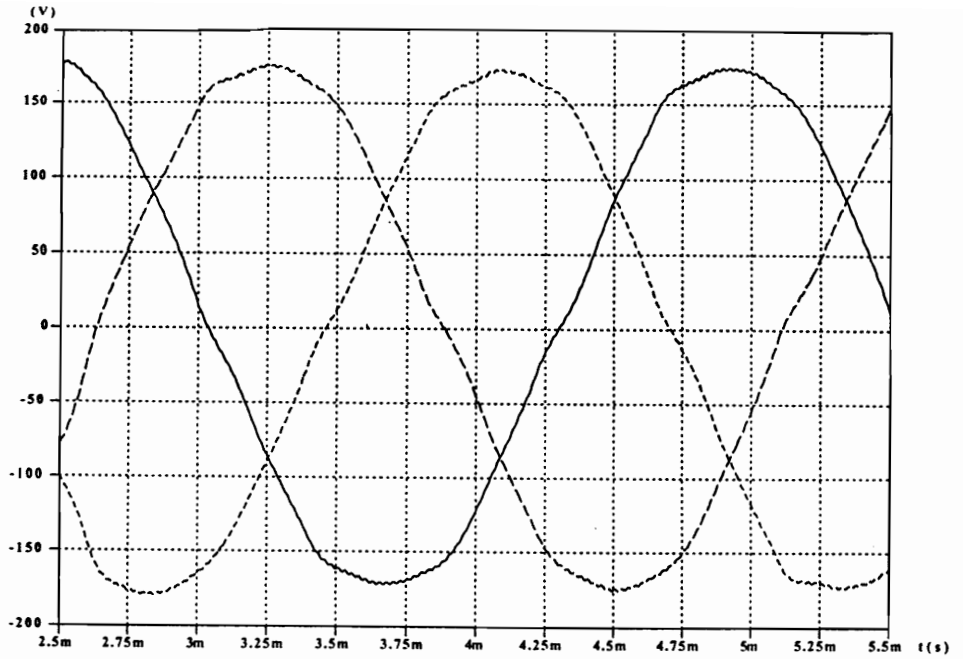
5.3 SIMULATION RESULTS

Switching model simulations are performed to evaluate the proposed topology. The simulated circuit is the topology shown in Fig. 5.1(a), with the parameters of dc-link filter inductance 1 mH, snubber $C_S + C_{S0} = 47nF$, inverter output inductance 500 uH in each phase, and an RC load of C = 5uF and R changing with power level. The rectifier output voltage is 400 V, and the power rating of the converter is 10 kW. The switching frequency is 40 kHz.

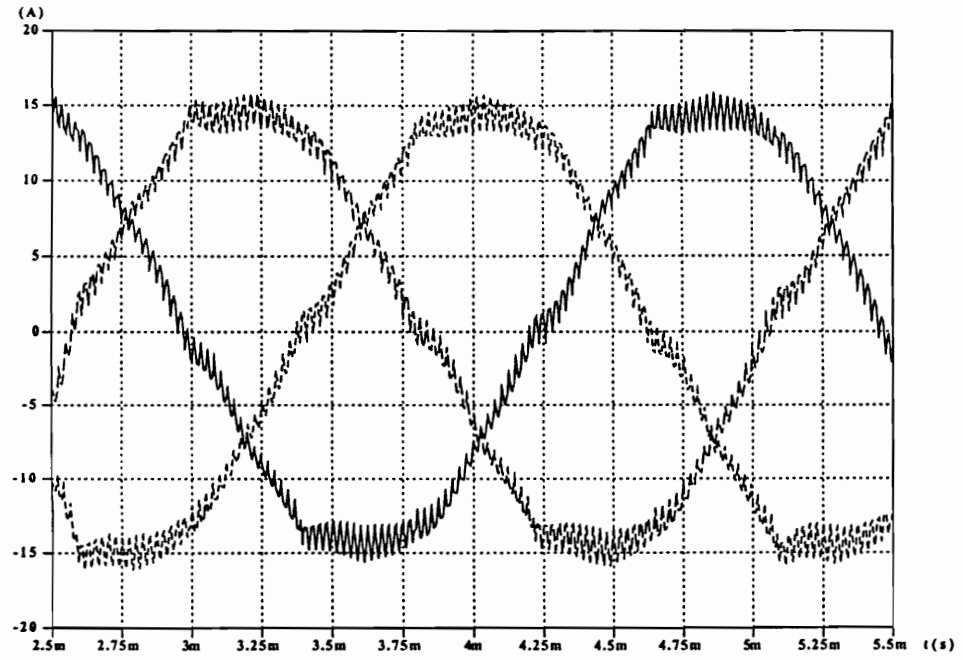
Fig. 5.5 shows the simulated output currents and output voltages of the inverter. As expected, all waveforms are sinusoidal. Fig. 5.6 shows the comparison of the clamp switch current and the inverter dc-link current. The curves in Fig. 5.6(a) correspond to motor drive type applications, where the amplitude of the output currents is kept constant, but the amplitude of the output voltages changes in the range of 25%~100% of rated value. The curves in Fig. 5.6(b) correspond to the power supply type application, where the amplitude of output voltages is kept constant but the load resistance changes in the range of 20%~100% of the rated value. In both cases, the peak clamp switch average current is lower than 30% of the maximum inverter dc-link current. Fig. 5.6(c) shows the turn-off current of S0 in a 60° interval for a motor drive type load at 10 kW and 230 V output. The turn-off current is also much lower than the inverter dc-link current, which means the turn-off loss of S0 is smaller than in other dc-link soft-switching schemes exemplified by those presented in [B17], where the dc-link switch is required to turn off the inverter dc-link current.

The loss models developed in Appendix A for 600 V IGBT IXGK50N60AU1 are used to evaluate the converter efficiency in simulation. Since the turn-off loss of an ultra fast low voltage IGBT such as the simulated device is usually more than twice its turn-on loss, and can be reduced to about 20% with a 47 nF snubber capacitor, the proposed zero-voltage turn-off technique can achieve a higher efficiency improvement than most zero-voltage turn-on techniques. Fig. 5.7 shows the simulated power stage efficiency with

motor drive load. The inverter soft-switching efficiency at full power is about 1.2% higher than in the hard-switching operation. More importantly, compared with the hard-switching operation, the total power loss of the inverter is reduced by about 30% with the soft-switching scheme, which means significant cost and weight/size reduction in a practical application.

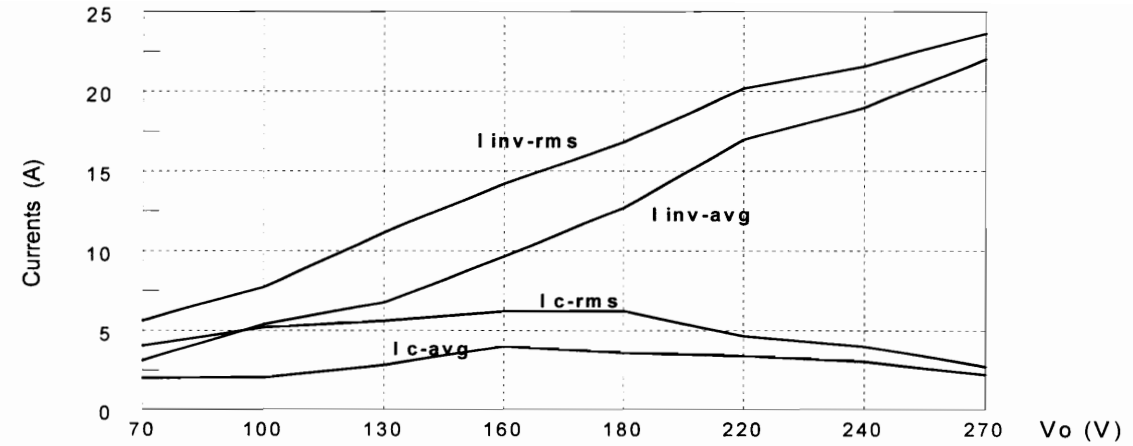


(a). Output voltages

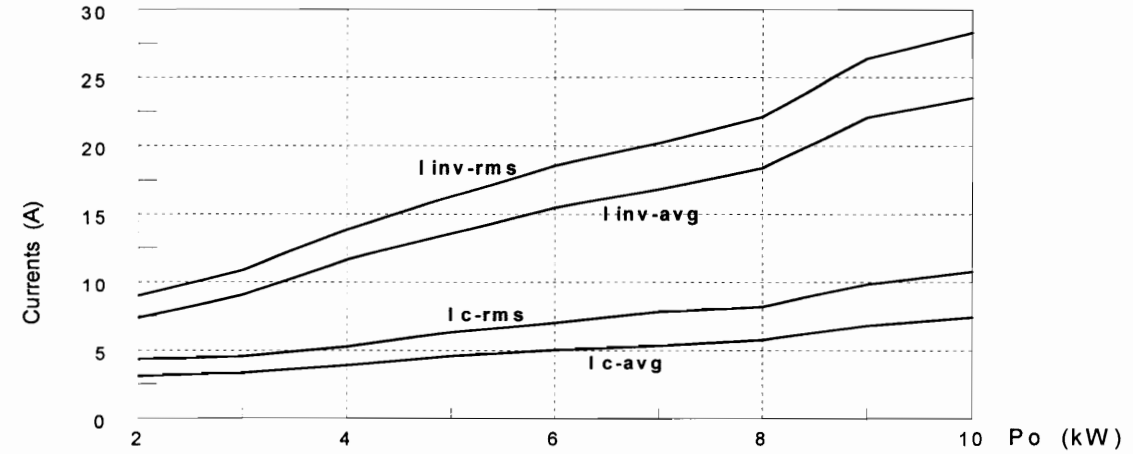


(b). Output Currents

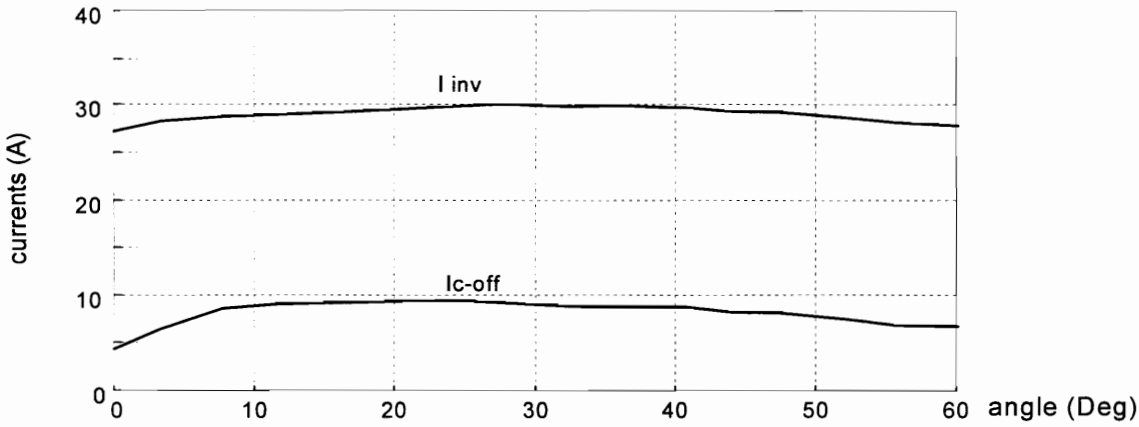
Figure 5.5 **Output voltages and currents**. All waveforms are sinusoidal.



(a). In motor drive type load



(b). In power supply type load



(c). Currents at soft-switching instants with motor drive loads at 10 kW

Figure 5.6 **S0 currents vs inverter currents.** The clamp switch current Ic is much lower than the inverter current in averaged value, rms value and instant value at soft-switching instant.

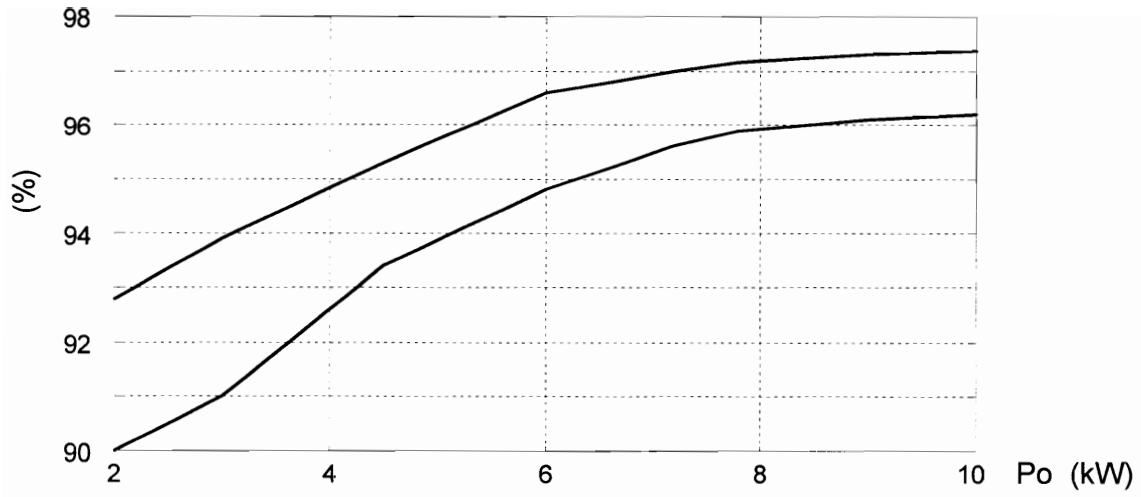
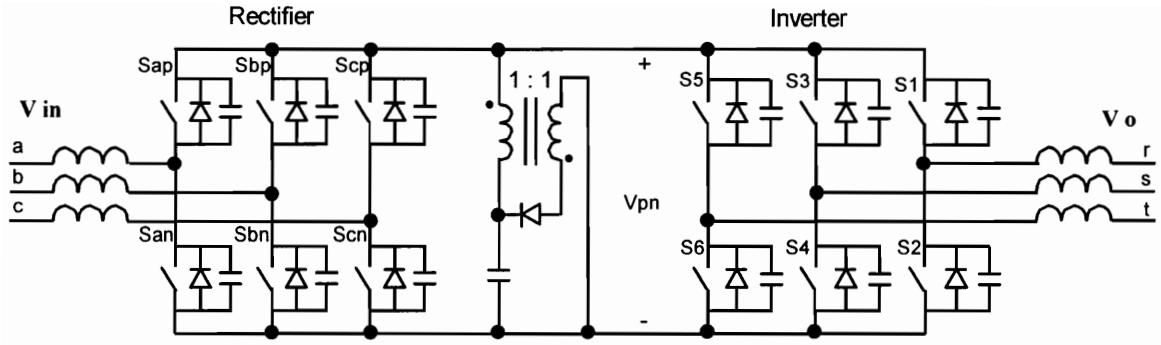


Figure 5.7 **Efficiency evaluation with motor type load**. The efficiency improvement at full load is about 1.2%, which results in about 30% loss reduction. Therefore, the soft-switching converter could use switches with less current rating, and have a lower implementation cost.

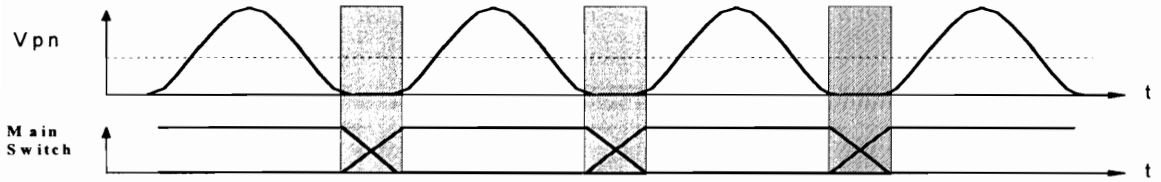
5.4 ZVT DC-LINK SCHEMES FOR SYSTEMS WITH A BOOST RECTIFIER

5.4.1 INTRODUCTION

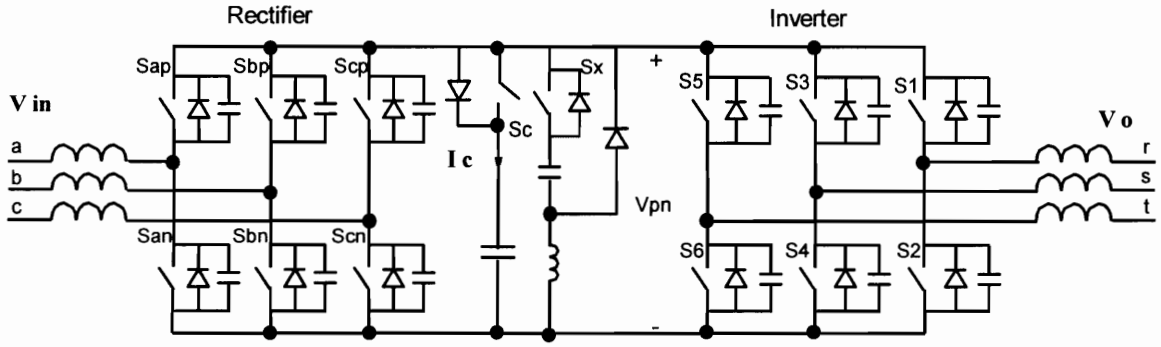
The performance of the ZVT dc-link topologies discussed in the Section 5.2 is limited by the diode rectifier, whose input current distortion and unregulated output voltage are not suitable for high-performance applications. A PWM boost rectifier can be used to improve the system performance. Many dc-link soft-switching schemes for three-phase PWM rectifiers and inverters are reported in [B8] [B13]-[B22]. These schemes deal with either a rectifier, or an inverter, and all have a dc-link switch in the main power path. If a rectifier and an inverter with these techniques are directly connected in an ac-dc-ac system, then there will be two additional components in the main power path, and their power loss can significantly offset the benefit of the soft-switching operation. Fortunately, if the soft-switching mechanism is applied directly to the common dc link of the rectifier and the inverter, the auxiliary circuit can be further simplified, and its power loss reduced. [B48] proposes to adopt a common actively clamped resonant dc link in a dual rectifier and inverter system for motor drives, and [B49] proposes to use a passive clamp resonant dc link in a dual rectifier and inverter system for the auxiliary power system in aircraft applications. The topology proposed in [B49] is shown in Fig. 5.8(a). Its operation principle, shown in Fig. 5.8(b), is that the rectifier switches and inverter switches are switched only when the dc-link voltage is zero, so that their switching losses can be dramatically reduced. However, similarly to the RDCL technique used in a single converter, the main power devices are subject to high voltage stress, and the inefficient discrete pulse modulation (DPM) control is still required to synthesize ac voltages. Another scheme is proposed in [B45] to implement the soft switching function in the common dc-link of ac-dc-ac PWM converters, and is shown in Fig. 5.8(c), with its operation principle shown in Fig. 5.8(d). The source converter (rectifier) and the load



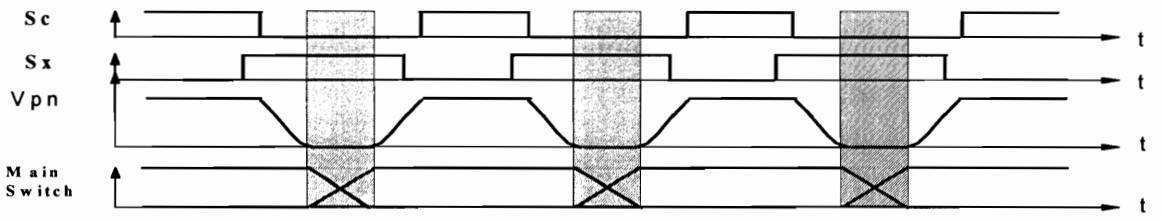
(a). RDCL double bridge converter [B49]



(b). Operation principle of (a)



(c). PWM resonant link bidirectional converter [B45]



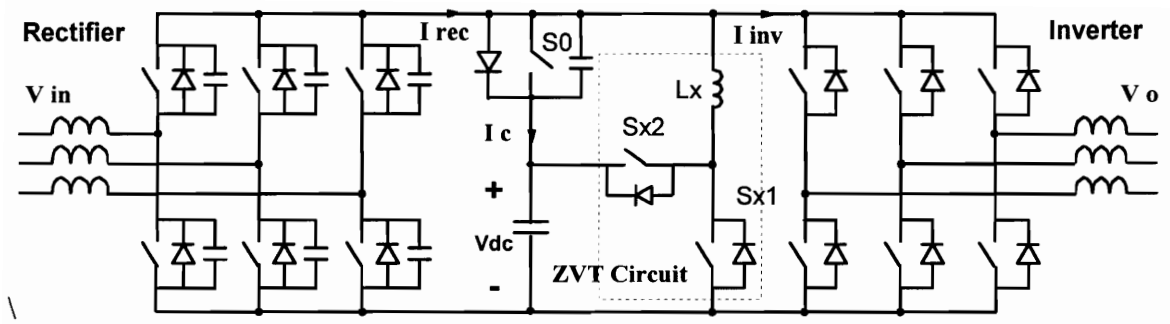
(d). Operation principle of (c)

Figure 5.8 **Existing three-phase AC-DC-AC soft-switching power converters.** A set of auxiliary circuit is used for both rectifier inverter switches and rectifier switches. The switching action of the main switches is allowed only during zero dc-link voltage periods, shown as shaded areas.

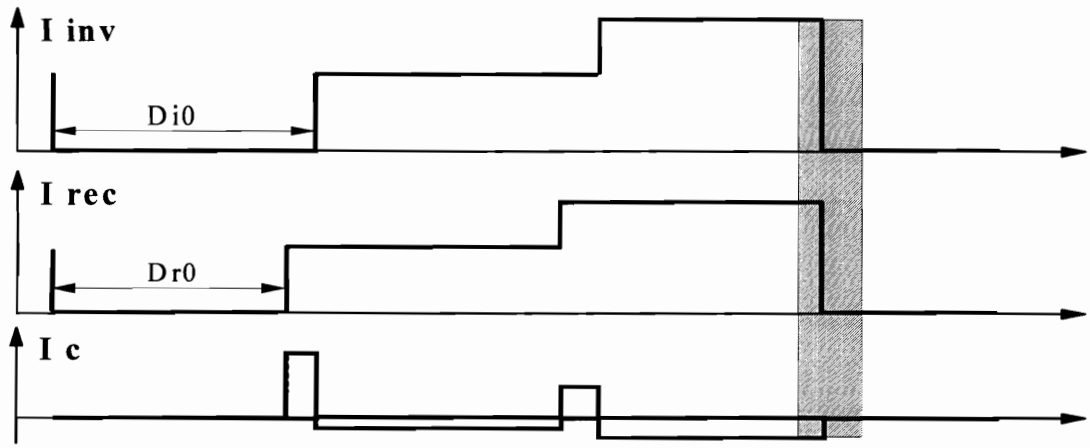
converter (a voltage source inverter) are both controlled in a PWM manner, and a low power auxiliary circuit is actuated to shape the dc-link voltage to zero whenever a main switch is to be switched. The static voltage stress of all switches is the same as in a hard-switching converter. To reduce the intervention of the auxiliary circuit, the switching actions of the rectifier switches and the inverter switches are always synchronized. However, the synchronization of every switching action of the rectifier switches and the inverter switches offsets much of the benefit of PWM control. Moreover, the soft switching is achieved by controlling the resonant current in the auxiliary circuit according to two threshold currents. This approach needs complex current and voltage sensing, and is not reliable for high-power applications. Also, no attempts have been made to minimize the power loss of the dc-link switch, and the high peak bi-directional resonant current creates high conduction loss in the auxiliary circuit.

5.4.2 NEW ZVT DC-LINK SCHEMES FOR THREE-PHASE CONVERTERS

The concept of the soft-switching topology shown in Fig. 5.4(a) can be easily extended to systems with a boost rectifier also. The new topology is shown in Fig. 5.9(a). The clamp switch S0 and its parallel diode D0, a ZVT circuit consisting of Sx1, Sx2, and Lx, and snubber capacitors are added into a standard ac-dc-ac system. The control of the rectifier is coordinated with the control of the inverter, so that a large portion of energy is delivered from the rectifier directly to the inverter without passing S0, and the power loss of S0 is reduced significantly compared with that in the previous dc-link soft-switching schemes [B13]-[B22]. This can be achieved by synchronizing the beginning of zero vector of the inverter with the beginning of zero vector of the rectifier in the modulation scheme, so that the direct energy transfer from the ac-dc converter to the dc-ac converter is kept at maximum. The operation of the converter system can be described with the example of $V_a > 0 > V_b > V_c$, $i_a > 0 > i_b > i_c$, $V_s > 0 > V_t > V_r$, $i_s > 0 > i_r > i_t$. The reference directions of currents are illustrated by arrows. According to the space vector



(a). A new ZVT dc-link topology for three-phase ac-dc-ac converters



(b). DC-link currents

Figure 5.9 **A new zero-voltage transition dc-link three-phase ac-dc-ac converter**. The turn-on of the rectifier switches and the turn-off of the inverter switches are synchronized through SVM, and the auxiliary circuit is actuated once in each switching cycle to brining dc-link voltage to zero, realizing soft-switching. The direct energy transfer from the rectifier to the inverter is maximized, and the power loss in the auxiliary circuit is small.

modulation (SVM) theory, the reference voltage vector of the rectifier is in Sector I, and can be synthesized with V1 (switch combination PNN), V2(PPN), and a zero vector V7(PPP). The reference voltage vector of the inverter is in Sector III, and can be synthesized with V3(NPN), V4(NPP), and V7(PPP). The modulation scheme for the rectifier is the same as the one in Fig. 3.3(a), and the modulation scheme for the inverter is the same as the one shown in Fig. 5.1(b). The largest currents, i_a in the rectifier and i_s in the inverter, are not switched, since Sap (Dap) and S4 are kept on. Notice that these schemes are very similar to the DD method proposed in [E37], which is deemed the optimum in terms of switching losses and high-frequency spectrum. The switching frequencies of the inverter and the rectifier are chosen to be the same, to facilitate the soft-switching intervention. The corresponding dc-link currents are shown in Fig. 5.9(b), in which the clamp current I_c is the difference between I_{rec} and I_{inv}, and is usually much smaller than I_{rec} and I_{inv} in both average and rms values. The shaded area illustrates the soft-switching commutation. The duty cycle of the rectifier zero vector is assumed to be smaller than the inverter zero-vector duty cycle in Fig. 5.9(b): $Dr0 < Di0$. The shaded area indicates the soft-switching operation region, in which the auxiliary circuit is used to help reduce the switching loss in the transition from the last nonzero vector into the zero vector in both the rectifier and the inverter. The snubber capacitance is Cs across each rectifier switch and is $Cs0$ across $S0$. These two snubber capacitors can be replaced by a lumped capacitor across p and n in the dc link also. Since the input and output phase inductances of the converters are large, the phase currents in both the ac-dc and dc-dc converters can be assumed constant during the soft-switching transition. The clamp voltage V_{dc} is also assumed constant in this process. The soft-switching process takes the following stages:

(a). [t0, t1] Prior to entering the zero vector, the rectifier state is V1 and the inverter state is V3. At t0, S0 is turned off. The turn-off current $I_c(t0)$ depends on the operation condition of the system. If $I_c(t0) > 0$, the current is conducted by the anti-parallel diode of S0, and this turn-off doesn't have any power loss. In this case, Sx1

should be turned on to bring the dc-link voltage *Vpn* to zero, which will be similar to the ZVT operation in [B8], but the auxiliary circuit has a very small power loss, since it only processes a small current determined by $I_{rec} - I_{inv}$. If $I_c(t0) < 0$ but its magnitude is small, Sx1 should also be turned on to accelerate the transient to $V_{pn} = 0$. If $I_c(t0) << 0$, as assumed in this example, S0 will be tuned off with a certain current, and after the turn-off, this current will discharge the equivalent snubber capacitors, $Cs0 + 3\ Cs$, until $V_{pn} = 0$. The snubber capacitors should be designed to be large enough for the turn-off loss of S0 to be negligible.

(b). [t1, t2] After V_{pn} is discharged to zero at t1, all diodes in the rectifier bridge and the inverter bridge will start to conduct and clamp V_{pn} at zero. This creates the zero-voltage switching condition.

(c). [t2, t3] Then, at t2, S3 and S5 in the inverter are turned off, and San and Scn in the rectifier are turned on at the same time. This switching action is accomplished at zero voltage, and therefore without power loss. The storage charges in the out-going devices will recombine naturally.

(d). [t3, t4] After t2, V_{pn} remains zero, since the current of the snubber capacitor is zero. Then according the PWM control, Scp is turned off at t3, and I_c starts to charge the equivalent snubber capacitor $Cs0 + 3\ Cs$, and V_{pn} increases gradually. If I_c is very small, or S2 is turned on before Scp is turned off in the case of $dr0 > di0$, Sx2 should be turned on to build up the dc-link voltage. However, the auxiliary circuit needs to provide only the charging current for the snubber capacitors, and has a very small power loss.

(e). [t4, t5] When V_{pn} reaches V_{dc} at t4, D0 starts to conduct and V_{pn} is clamped at V_{dc}. The charging process is stopped, and S0 can be turned on with zero voltage at t5.

Notice that there is also another alternative if $dr0 > di0$: only S6 is turned off at t1, and S2 remains on in the whole process. Then, after Sx2 is turned on at t3, the inverter will enter V4 naturally, without any turn-on loss occurring in S2.

The commutation process is shown in Fig. 5.10, and the key waveforms are shown in Fig. 5.11. With the help of the auxiliary circuit, the dc-link clamp switch and switches in the rectifier are turned on with zero voltage, and switches in the inverters are turned off with zero voltage. Notice that the zero-voltage condition is kept through the whole duration, where the inverter and rectifier are both in zero vector. Therefore, the turn-off loss of the inverter switches does not depend on the size of snubber capacitor, and switching losses are reduced significantly. The soft-switching operation can be always maintained for any inverter load displacement angle φ. However, if φ is beyond $\pm\pi/6$, then one switch carrying small current in the inverter is turned on (instead of being turned off) with zero voltage, but the total switching loss is still reduced.

The ZVT circuit, shown within the dotted frame in Fig. 5.9(a), is not always needed, and can be simplified or even eliminated for some applications. For example, if the input voltage of the rectifier is much higher than the output voltage of the inverter, *Dr0* is always smaller than *Di0*, so Sx2 would not be necessary. Also, if the rectifier input voltage is always lower than the inverter output voltage, I_c will be negative at t0, then Sx1 will not be necessary. Note that the current ripples in the phase currents of the rectifier and the inverter always try to make *Ic* more negative at t0, so Sx1 could be indeed removed in many practical applications. On the other hand, if desired, the inductor feedback technique in [A33] can be used to further reduce the power loss in the ZVT circuit, and the ZCT technique described in Chapter 2 can be used to improve the turn-off of S0. However, the basic operation principle remains very similar to that of Fig. 5.9(a).

The clamp switch current I_c is the difference between I_{inv} and I_{rec}, and is usually much smaller. Fig. 5.12(a) shows a comparison between I_c and I_{inv} in the average and rms values in a 10 kW motor drives for a 230 V system, obtained under the following conditions: rectifier input line-line rms voltage 184 V (low end of 230 V system), dc-link voltage 450 V, inverter load power factor 0.9, inverter output line-line rms voltage in the range of 24~240V as the motor speed is changed from 10% to full rated speed. The peak

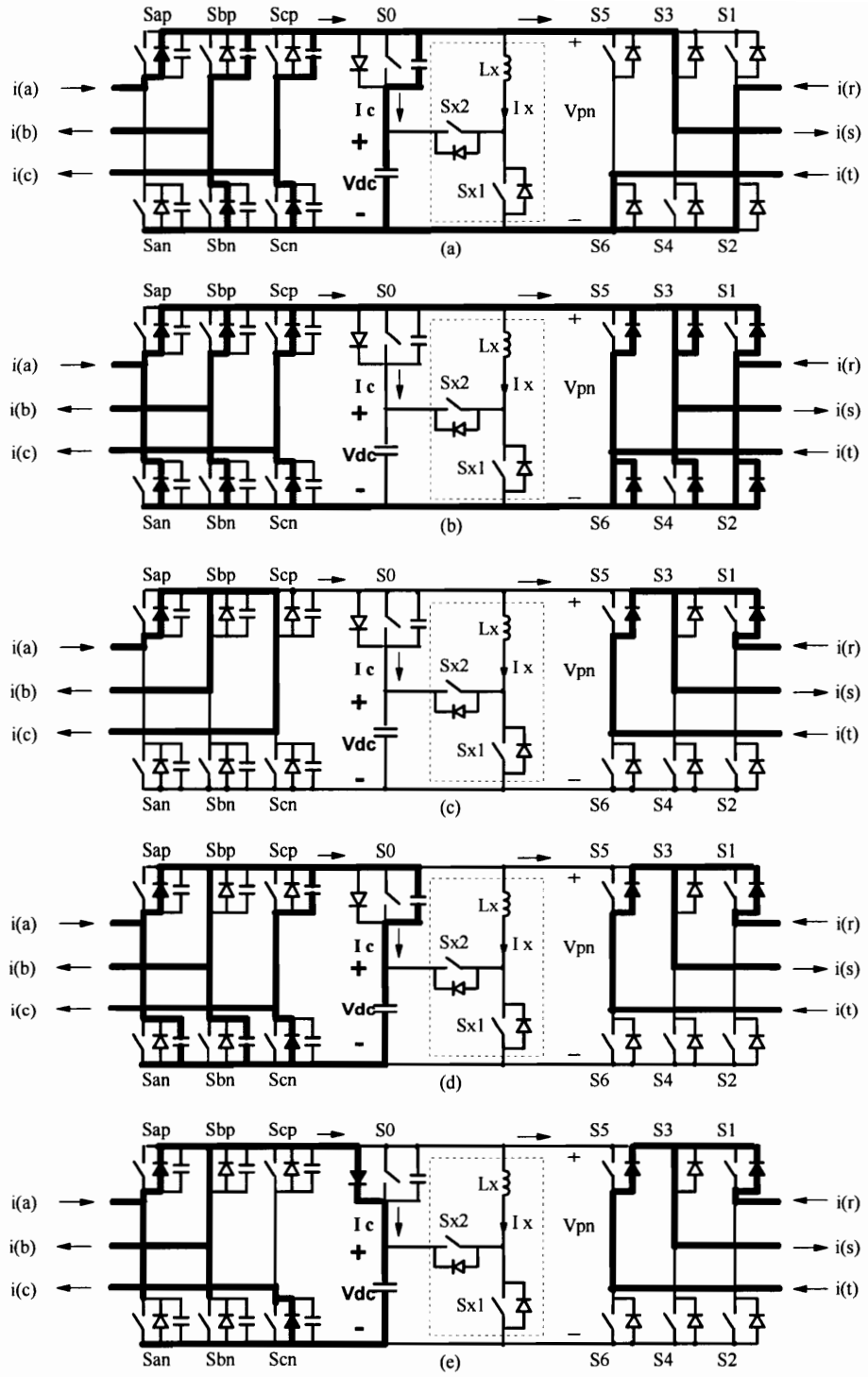


Figure 5.10 **Operating stages in the ZVT commutation**. The rectifier switches are turned on with zero-voltage, and the inverter switches are turned off with zero-voltage. The auxiliary switches are not actuated.

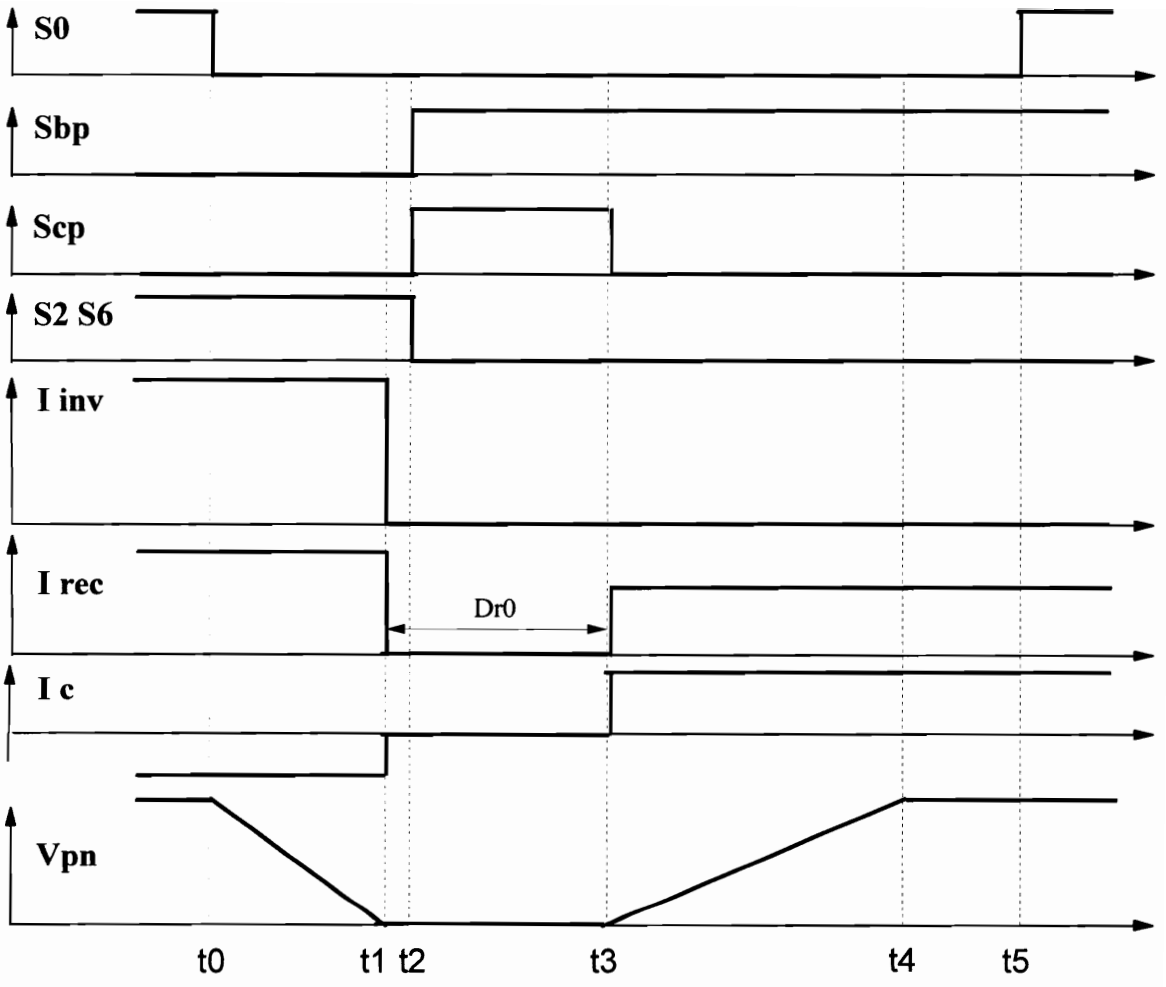
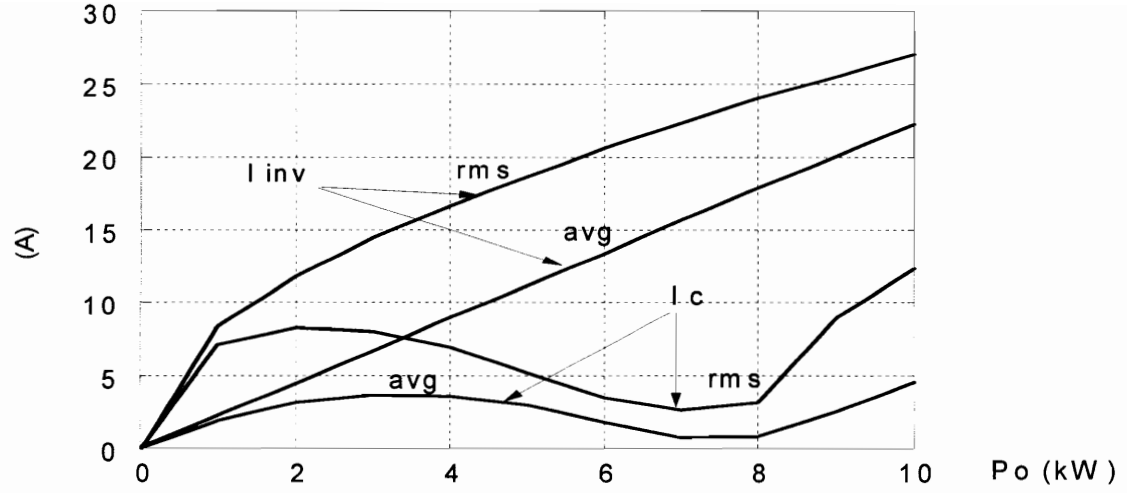


Figure 5.11 Key waveforms of the ZVT commutation.

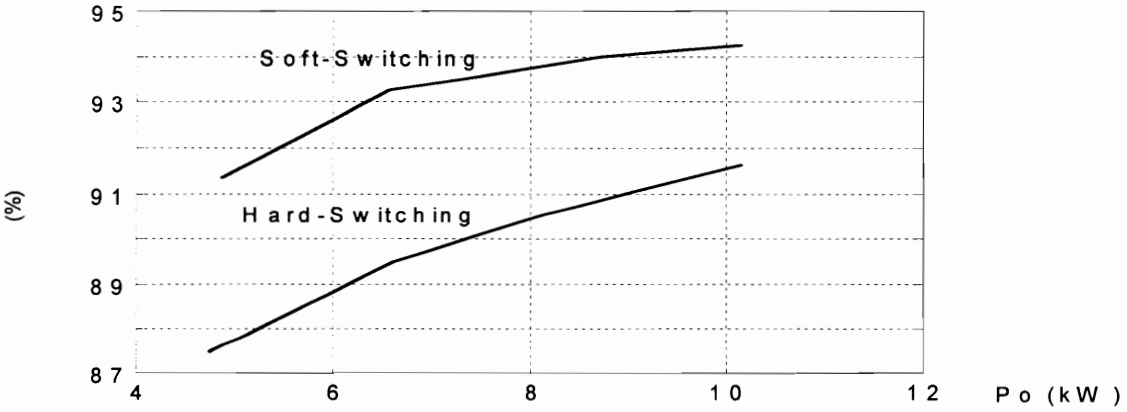
averaged current of the dc-link switch is below 25% of the inverter dc link current, so the resulting conduction loss is reduced to lower than 1/4 of that obtained in other schemes with a dc-link switch. Around full speed, where peak thermal stress of the converter occurs, the average current of S0 is about 1/5 of the inverter dc-link current. For constant output voltage power supplies, the proposed scheme can achieve the optimum performance, since the inverter will work in a condition similar to the full speed operation in motor drives. The turn-off current of S0 depends on the rectifier input voltages and rectifier output voltages. When they are close, the turn-off current is also much smaller than the peak current of inverter current, because I_{rec} and I_{inv} are comparable at t0. The converter system is evaluated at 50 kHz switching frequency with switching model simulation. The power stage parameters of the rectifier and inverter is the same as those of the 450 V converters simulated in Section 3.3. The dc-link clamp switch is also IXGK50N60AU1, and each auxiliary switch consists of three IXFM20N60 in parallel. The resistance of the RL load is changed in the simulation to get different output powers. The efficiency is shown in Fig. 5.12(b). As can be seen, more than 2.5% efficiency improvement is achieved with soft switching. Therefore, the power losses of the power switches are significantly lower in the soft-switching system than in the hard-switching system, so switches with lower current rating can be used, which further reduces the power loss and possibly the cost of the converter.

There can be other operation schemes for the topology presented in Fig. 5.9(b) also. The zero-voltage turn-on and turn-off for inverter switches and rectifier switches can be in any combination. For example, exchanging the inverter modulation scheme with the rectifier modulation scheme, the inverter switches can be turned on (instead of being turned off) with zero voltage, and the rectifier switches can be turned off with zero-voltage. If the beginning of the rectifier zero vector is synchronized with the end of the inverter zero vector, then the auxiliary circuit can be used to help all switches in both the rectifier and inverter to turn on with zero voltage. If the end of the rectifier zero vector is synchronized with the beginning of the inverter zero vector, then the auxiliary circuit can

be used to help all switches in both the rectifier and inverter to turn off with zero voltage. However, the current in the clamp switch and the auxiliary circuit will be higher. The choice of a particular soft-switching scheme should be made according to the device characteristics and special system requirement in a specific application.



(a). rms and averaged dc-link currents



(b). Converter efficiency

Figure 5.12 **Simulated dc-link currents and converter efficiency with motor type load**. The clamp switch current is much lower than the inverter dc-link current, so the power rating of Sc is much lower than the dc-link switch in existing ZVT schemes. The efficiency improvement of the soft-switching operation is about 2.5% at full load, and the converter loss is reduced by 30% through soft switching.

5.5 CONCLUSIONS

Novel dc-link soft-switching schemes for ac-dc-ac PWM converters are proposed. An auxiliary circuit consisting of a dc-link clamp switch and a parallel resonant circuit is used to shape the common dc-link voltage to zero when soft switching is required. By coordinating the control of the ac-dc converter and the dc-ac converter, most energy is transferred between these two converters without passing the clamp switch, so the power loss of the clamp switch can be minimized. The current in the auxiliary circuit is also less than the maximum inverter and rectifier current. With the help of the auxiliary circuit, the dc-link switch and the switches in the ac-dc converter are turned on with zero voltage, while the switches in the dc-ac converter are turned off with zero voltage. Therefore, the switching loss of the converters can be significantly reduced.

The basic concept of the proposed soft-switching schemes can be easily extended to other topologies. For example, the load converter can be a four-leg inverter to deal with an unbalanced three-phase load, or a dc-dc converter. The source converter could also be a chopper if the source were a current source. Any of the discussed schemes can be easily adapted to achieve soft switching in such systems with minimum modification.

6 SOFT-SWITCHING THREE-LEVEL PWM CONVERTERS FOR HIGH POWER APPLICATIONS

6.1 INTRODUCTION

In very high power applications, power switches have to withstand high voltage, which in many cases cannot be processed by a single device. Especially, with the fast development of power device technology, high power IGBTs are replacing GTOs, and even SCRs in up to lower megawatt power level. Since the voltage rating of IGBTs is still much lower than GTOs' and SCRs', circuit technology is necessary to expand the voltage capability of the switches. Traditionally, series connection of power devices is used to increase converter voltage rating. However, the voltage sharing of the series connected switches, especially during the turn-on and turn-off transients, is a serious problem. Although large and lossy snubbers are usually used, the switch voltage rating still has to be much derated to ensure reliable operation. As a result, converter cost and power loss are increased.

In recent years, multi-level converters are increasingly used to improve the situation. The multi-level structure ensures even device voltage sharing, and also provides extra means to reduce the switching loss and voltage/current ripple, thus achieving significant performance and cost improvement compared to simple device seriesing approach. Various aspects of multi-level dc-dc converters and three-phase converters are studied in [C1]-[C21]. In this chapter, a new multi-level two-quadrant chopper for SMES and motor drive applications will be presented to further demonstrate the operation principle and advantages of multi-level structure.

Soft-switching techniques of three-level converters are investigated in a few papers [C17]-[C21]. The soft-switching topology proposed in [C20] has two auxiliary switches in the main power path. Due to the high power loss of these auxiliary switches, this topology is not really suitable for high power applications. The three-level ARCP in

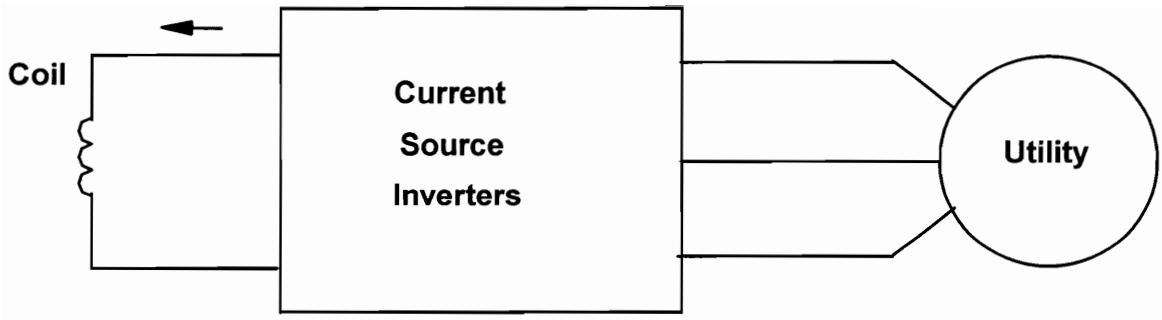
[C21] does not have auxiliary switches in the main power path. However, the auxiliary switches have 50% higher voltage stress than the main switches, making its implementation difficult. These two topologies provide zero-voltage turn-on for the main switches, but leave the main switch turn-off loss practically untackled; thus they cannot effectively alleviate the switching loss problem in high-power inverters. [C22] proposes a simple ZVT topology for a three-phase three-level boost rectifier. However, the auxiliary switch has to block the full output voltage, and is turned off with high current. Moreover, all three phase currents have to be commutated in each switching cycle, and this constraint causes more than optimum switch turn-off loss. In this chapter, the PWM switch cell concept will be used to derive soft-switching topologies for three-level inverters. Several simple ZVT three-level rectifier topologies will also be investigated.

6.2 MULTI-LEVEL TWO-QUADRANT BOOST CHOPPERS

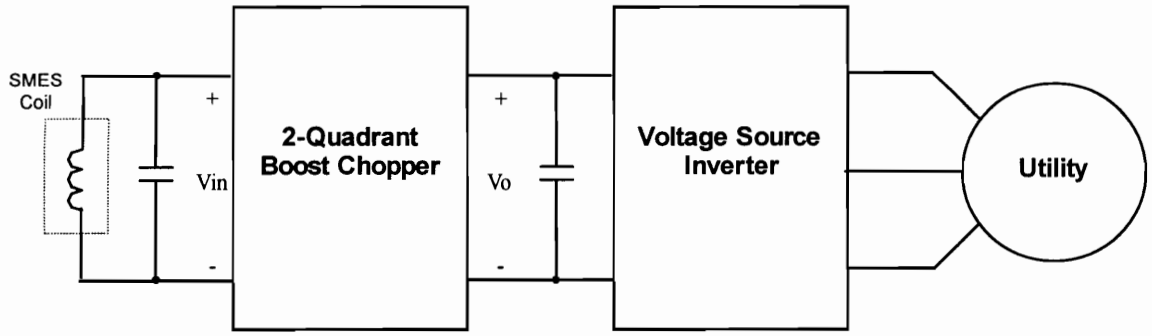
6.2.1 INTRODUCTION

In many applications, a current source is interfaced with a voltage source through a bi-directional power converter. Superconductive Magnetic Energy Storage (SMES) is a typical example. With the development of superconductive materials and power electronics techniques, SMES is emerging as a promising technique for bulky energy storage and fast-response power source, and its applications in utility industry, pulse power sources, UPS, and military applications are becoming reality. Typically, the SMES coil is interfaced to a power distribution system through bi-directional power converters (called power conditioning system, PCS). For some applications, the power distribution system is a dc voltage source, but predominantly, it is a three-phase ac voltage source. In the case of three-phase ac power system, the PCS can be either three-phase current source inverters (CSI), show in Fig. 6.1 (a), or three-phase voltage source inverters connected to two-quadrant boost choppers, shown in Fig. 6.1(b). In the second approach, the voltage source inverter (VSI) is used to control the power transfer between SMES and utility, and the currents in its switching devices are independent of the coil current. The two-quadrant boost chopper is connected directly to the superconductive coil, so the current ratings of its devices are determined by the maximum coil current, similarly to the devices in the current source inverters with the CSI approach. Since the coil current usually changes in a wide range (for example, coil current can be 30-100% of the full current in the normal operation), the second approach generally results in higher energy efficiency and lower system cost. For those applications with dc power system, only the two-quadrant chopper is needed in the PCS.

A two-quadrant boost chopper with SMES coil is shown in Fig. 6.2. Due to the huge size of the coil, the effect of parasitic capacitance is very pronounced. The



(a). CSI approach



(b). VSC approach

Figure 6.1 **Power conditioning systems for SMES**. The two-quadrant boost chopper is used to interface a current source (SMES coil) to a voltage source (the bulky dc-link capacitor).

resonance between parasitic capacitance and coil inductance can cause excessive power loss in the superconductor and even structure damages to the coil. To alleviate the resonance problem, a filter consisting of a capacitor and an inductor is inserted before the coil to smooth the coil voltage. Assuming that the coil voltage is constant in the steady state, the operation of the two-quadrant boost chopper is similar to that of a conventional boost converter in the coil discharging mode, but reassembles a conventional buck converter in the coil charging mode. The energy transfer in the converter is bi-directional, since V_{in} is reversible. The operation of the converter can be classified into the subtopologies shown in Fig. 6.3. The two zero-voltage subtopologies, (a) and (b) of Fig. 6.3, should be used alternately to achieve thermal balance between the two active switches, and to attain higher power capability. Only one of the two non-zero-voltage subtopologies, (c) and (d), should be used in a normal operation to reduce the inductor current ripple and switching loss. The duty cycle of the active non-zero-voltage subtopology determines the average voltage between a and b, and thus the power transfer of the converter. When the SMES coil is to be discharged, i.e. $V_{in} < 0$, the subtopologies of Figs. 6.3(a), (b), and (c) will be the active subtopologies. When the coil is to be charged, i.e. $V_{in} > 0$, the active subtopologies will be those of Figs. 6.3(b), (c) and (d). The operations in these two modes are similar to dc-dc converters, and only one switch needs to be switched in a switching cycle to control the converter. For example, when $V_{in} > 0$, i.e. in the charging mode, the (a)-(c)-(b)-(c)-(a)- switching sequence, referred to the subtopologies in Fig. 6.3, can be used, in which S1 and S2 are switched alternately to achieve thermal balance. Similarly, in the discharging mode, the switching sequence can be (a)-(d)-(b)-(d)-(a)-. In both operation modes, with the same duty cycle for both switches, the operation of the converter is almost identical to that of a dc-dc converter at any given time.

Due to the very high power requirement in most SMES systems, the power converters usually have to deal with both high current and high voltage. This section proposes a multi-level chopper structure to efficiently utilize the device voltage capability

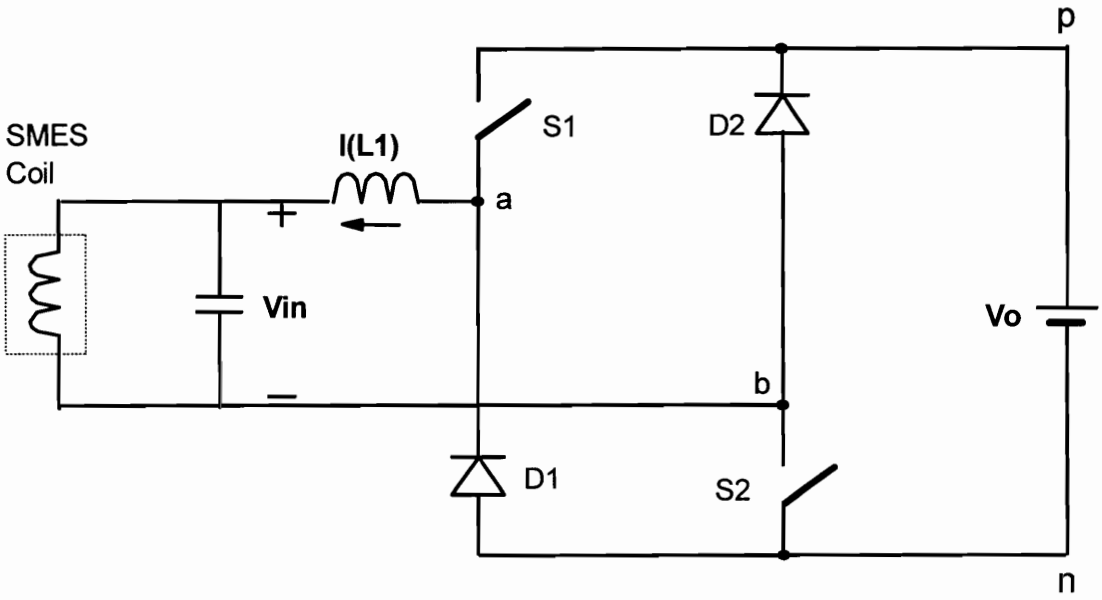


Figure 6.2 Schematic of two-quadrant boost chopper.

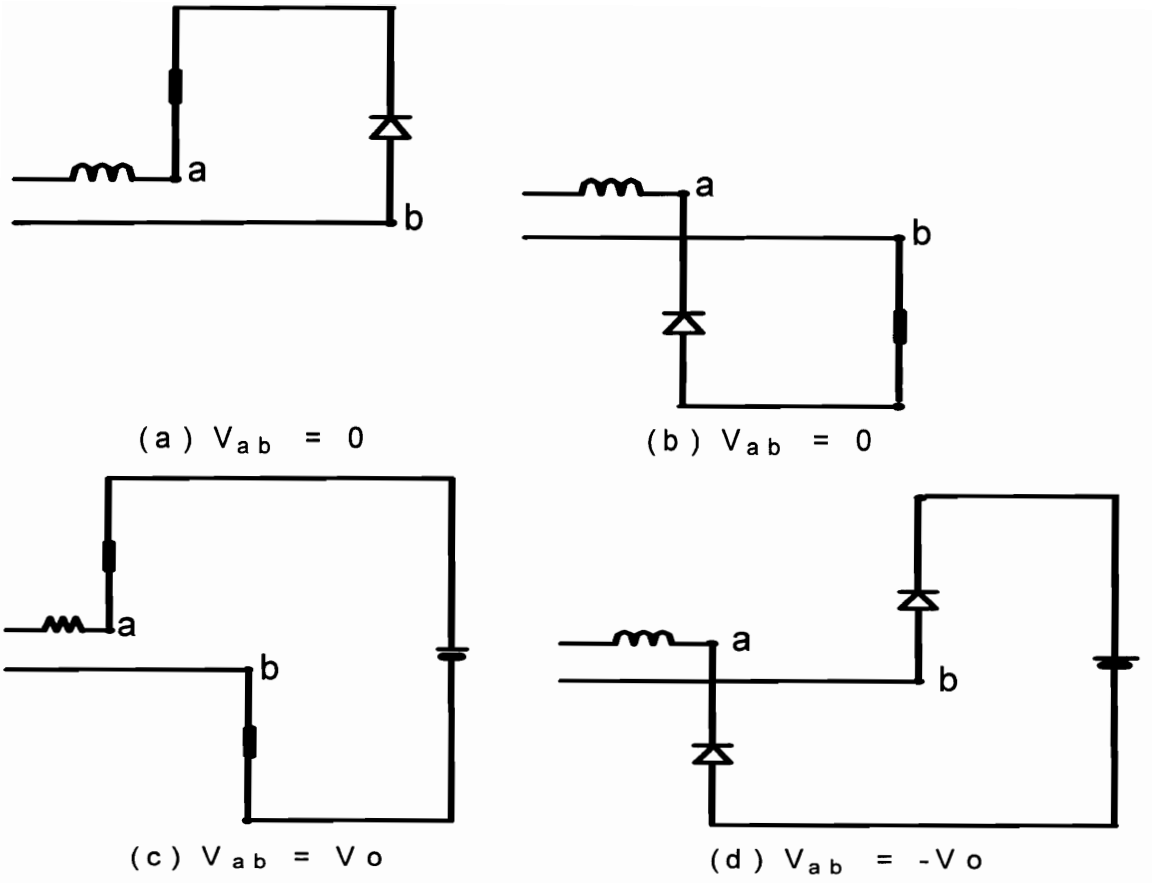


Figure 6.3 Subtopologies of two-quadrant boost chopper.

and improve the converter performance. Compared to the conventional two-level power converters, the multi-level topology can achieve higher efficiency and power density, and reduce system cost.

The topologies and control schemes proposed in this section are equally applicable to many other applications where a current source is interfaced with a voltage source, and the power flow is reversed by reversing the voltage across the current source, such as switching reluctance motor drives and magnet power supplies.

6.2.2 MULTI-LEVEL TWO-QUADRANT BOOST CHOPPERS

Multi-level power conversion has been an active research topic in high-power applications, especially in three-phase converters at megawatts power range. Three-level one-quadrant dc-dc converters have also been proposed for high-voltage uni-directional dc-dc power conversion [C16] [C17]. On the other hand, no research results on multi-level two-quadrant choppers have been reported.

Considering the uni-polarity of the filter inductor current, a general multi-level structure of the two-quadrant boost choppercan be derived by simplifying multi-level three-phase converters, and is shown in Fig. 6.4. A three-level chopper is shown in Fig. 6.5 as an example. The proposed three-level chopper has a basic structure similar to a conventional two-level chopper, but two additional clamping diodes Dc1 and Dc2 are used to clamp the maximum switch voltage at $V_o/2$. The two bridge diodes D1 and D2 need to block the voltage of V_o, and each can be implemented as two diodes in series if necessary. All switches and the clamping diodes only block the voltage of $V_o/2$. Similarly, the voltage rating of switches and clamping diodes in a k-level converter is reduced to $V_o/(k-1)$. Compared with the simple series approach, the switches have a much better voltage sharing in the multi-level structure, making it especially attractive for high-voltage applications. Since fewer power devices are required for a given

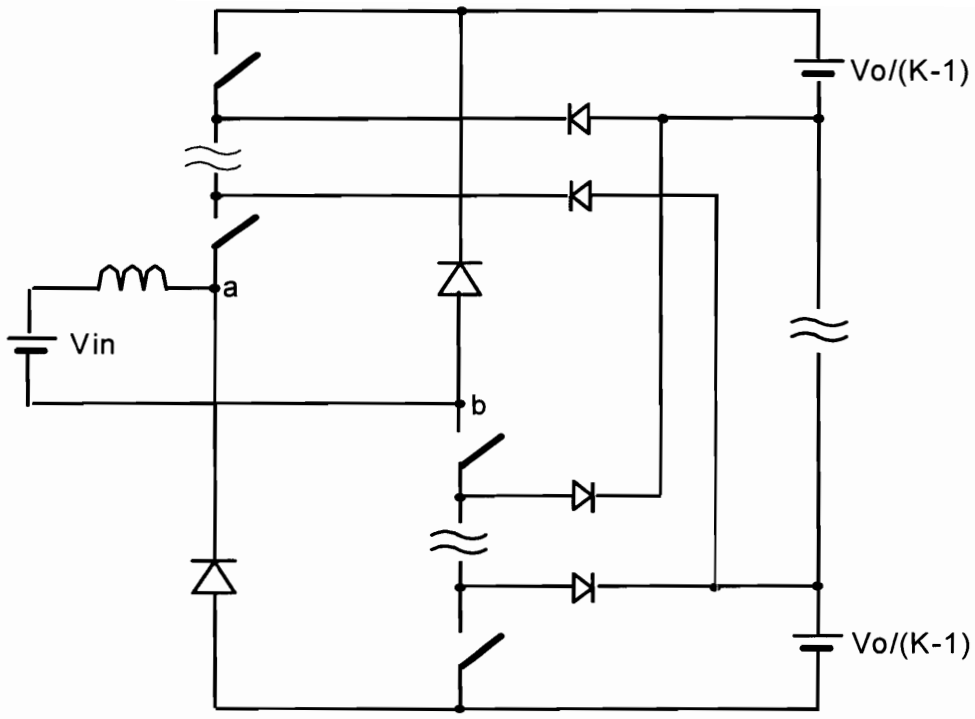


Figure 6.4 **Multi-level two-quadrant boost chopper.** The topology is similar to a multi-level three-phase inverter.

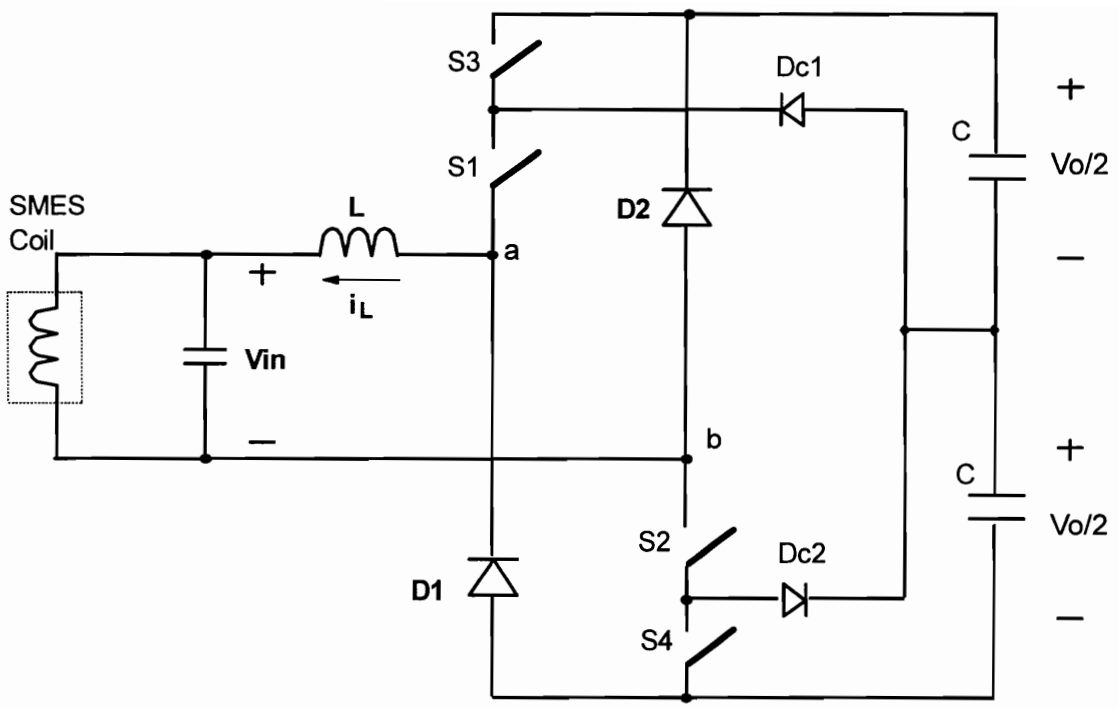


Figure 6.5 Three-level two-quadrant chopper.

application, higher reliability and efficiency, and lower converter cost can be achieved through multi-level conversion. This also provides a way to use fast and robust switch devices, such as IGBTs, in high voltage and high power applications. In addition, in a k-level chopper, k voltage levels are attainable in either power transfer direction. The PWM scheme can synthesize the desired voltage using only the two levels directly adjacent to it. Since the multi-level chopper can synthesize the required voltage with a better resolution, it has less ripple in the filter inductor current, and therefore requires a smaller filter than a conventional chopper. The switching loss of the chopper is also much reduced, since the voltage change in a switching action is only *Vo/(k-1)*.

In most cases, the voltage sources at the output are implemented as bulky capacitors. An important issue in multi-level converters is to maintain the charge balance of the bulky capacitors, so that even device voltage stress can be obtained. The above PWM scheme gives the best performance in terms of current ripple and switching loss, but generally cannot guarantee the charge balance of the bulky capacitors. The modulation scheme can be modified to achieve charge balance, but then the current ripple and switching loss will be increased. Basically, this multi-level structure requires extra circuits to regulate the voltages of the bulky capacitors. However, the three-level topology shown in Fig. 6.5 can achieve charge balance with the above-discussed PWM scheme, and therefore is more practical. The following discussion will be focused on the three-level chopper.

6.2.3 OPERATION OF THREE-LEVEL TWO-QUADRANT BOOST CHOPPER

In the steady state, the dc-link voltage V_o is constant. Due to the very large inductance, and thus very slow current change rate during the normal operation, a SMES coil can also be considered a constant current source. The power transfer is determined by V_{in}, which is the same as the average value of V_{ab} in the steady state. Different switch

combinations produce different values of voltage V_{ab}. By controlling the duty cycles of active subtopologies, V_{ab} can be controlled to be a desired value.

One of the most distinctive characteristics of the multi-level chopper is the availability of more subtopologies than in a two-level chopper. The possible subtopologies of a three-level chopper are shown in Fig. 6.6. It should be noted that more than one subtopologies are available for $V_{ab} = -V_o/2$, 0 and $V_o/2$. Through the proper use of these redundant states, PWM schemes can be developed to reduce the switching loss and inductor current ripple, and to maintain the charge balance of the dc-link midpoint without sacrificing other performances. The basic principle is to operate the chopper only with the subtopologies which produce voltage levels directly adjacent to V_{in} reference at any given time, in order to save the switching losses and reduce the filter inductor current ripple. The active subtopologies and switch control strategies for different operating ranges are shown in Table 6.1, in which the numbers of subtopologies refer to the figure numbers in Fig. 6.6. The term "PWM 1" means that the two switches are turned on alternately with the same duty cycle d, while the term "PWM 2" means that the two switches are turned off alternately with the same duty cycle of (1-d). The key waveforms obtained for $0.5 < V_{in}/\ V_o < 1$ are shown in Fig. 6.7(a). The gate signals for S1 and S2 are always "ON" and are not shown in the diagram for brevity. Fig. 6.7(b) shows the waveforms with conventional two-level control as a comparison. Clearly, in the three-level chopper, only one switch is switched at any given time, so the dynamic voltage sharing problem, which is the most serious problem in traditional series connected switches, is completely eliminated. The static voltage sharing of the switches is achieved by the clamping diodes. Therefore, the switch voltage rating can be fully utilized, and fewer switches, or switches with lower voltage rating, which are cheaper and more efficient than in traditional two-level choppers, are required.

For the same operating point, the conduction loss of the three-level chopper is about the same as in its two-level counterpart theoretically, considering that two power devices

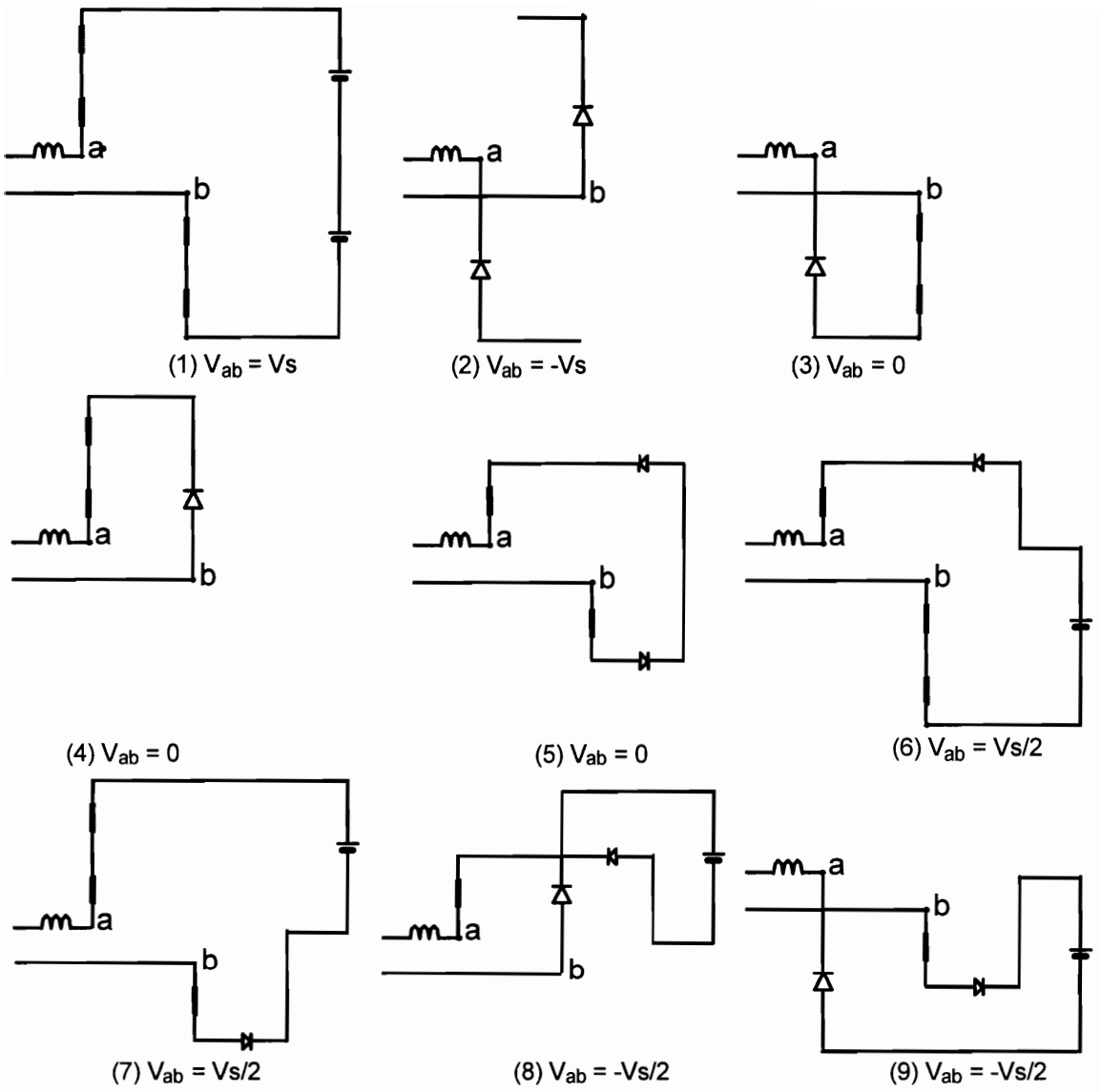


Figure 6.6 **Subtopologies of three-level two-quadrant chopper.** The redundant switch states can be used to minimize the switching loss, inductor current ripple, and to maintain dc-link midpoint charge balance.

Table 6.1. Control Strategies of Three-Level Chopper

Operating Range	Active Subtopologies	PWM Strategies
$-1 < V_{in}/V_o < -0.5$	(8), (9), (2)	S1, S2: PWM 1 S3, S4: Off
$-0.5 < V_{in}/V_o < 0$	(8), (9), (5)	S1, S2: PWM 2 S3, S4: Off
$0 < V_{in}/V_o < 0.5$	(6), (7), (5)	S1, S2: On S3, S4: PWM 1
$0.5 < V_{in}/V_o < 1$	(1), (6), (7)	S1, S2: On S3, S4: PWM 2

with the same voltage rating are required in series to block the voltage in a two-level chopper. Actually, a two-level converter will have more conduction loss than the three-level chopper, because more than two devices, or two devices with high voltage rating, are required due to the uneven voltage sharing. Moreover, the switching losses in the three-level structure are reduced to 50% of what they would be in a conventional two-level chopper, since only one switch is turned on/off at half the output voltage in each switching cycle. This will enable the three-level converters to operate at twice the switching frequency of a conventional two-level converter with about the same switching losses.

Another advantage of the multi-level chopper is the reduced current ripple. In the two-level converter, the peak-peak inductor current ripple is:

$$\Delta I_2 = \frac{V_o T_s d_2 (1 - d_2)}{L} = d_2 (1 - d_2) \frac{V_o T_s}{L} ,$$

where d_2 is the switch duty cycle: $d_2 = \frac{|V_{in}|}{V_o}$.

In the three-level converter, the ripple current peak can be calculated according to the operating ranges of V_{in}:

when $\frac{|V_{in}|}{V_o} < 0.5$:

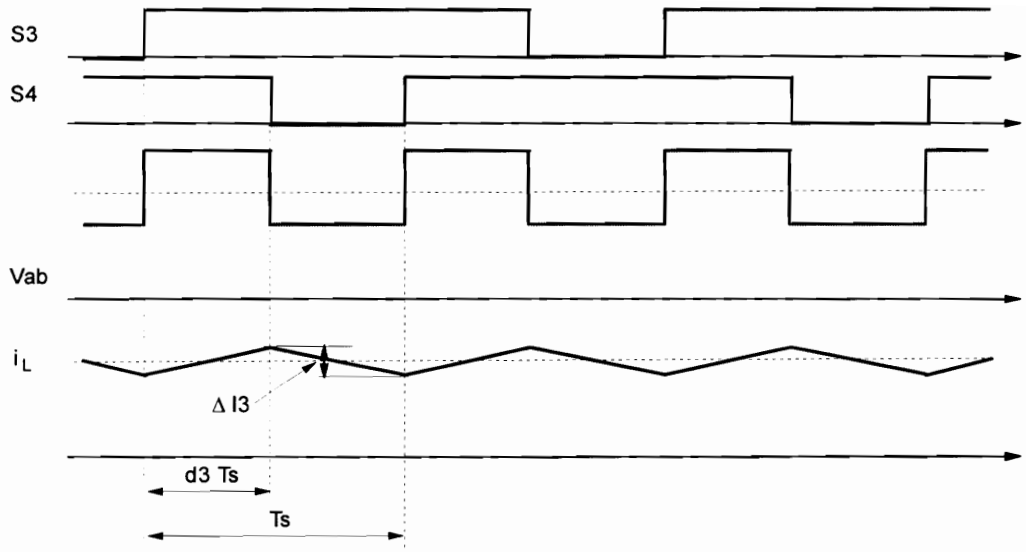
$$\Delta I_3 = \frac{V_o T_s d_3 (1 - d_3)}{L} = d_3 (1 - d_3) \frac{V_o T_s}{L} ,$$

where the duty cycle $d_3 = \frac{2|V_{in}|}{V_o}$;

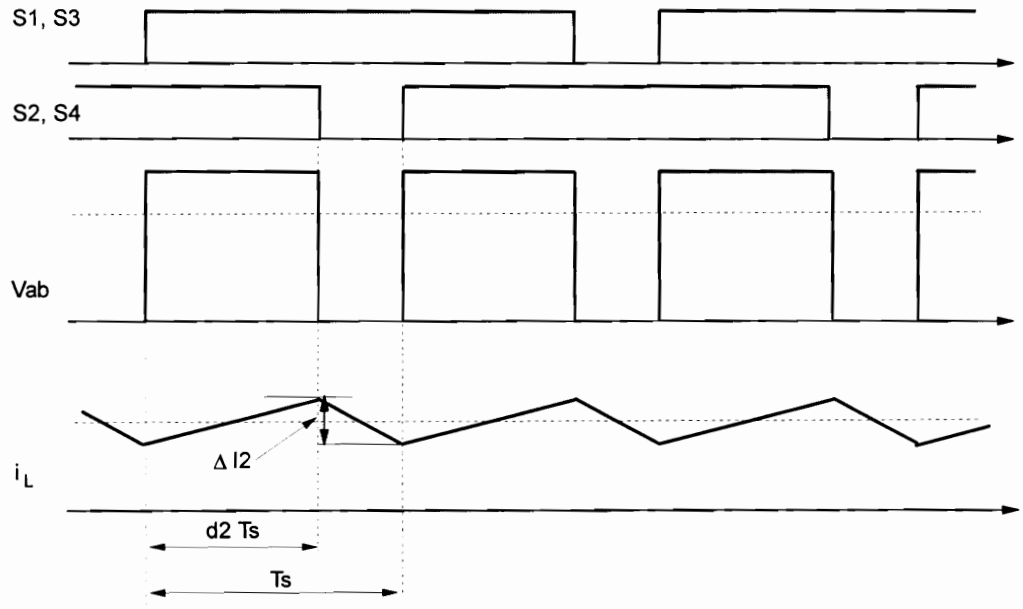
when $\frac{|V_{in}|}{V_o} > 0.5$:

$$\Delta I_3 = \frac{V_o T_s d_3 (1 - d_3)}{L} = d_3 (1 - d_3) \frac{V_o T_s}{L} ,$$

where the duty cycle $d_3 = \frac{2|V_{in}| - 1}{V_o}$.



(a) Three-level chopper



(b) With two-level control

Figure 6.7 **Key waveforms of two-quadrant choppers.** The three-level chopper has lower switching voltage and inductor current ripple.

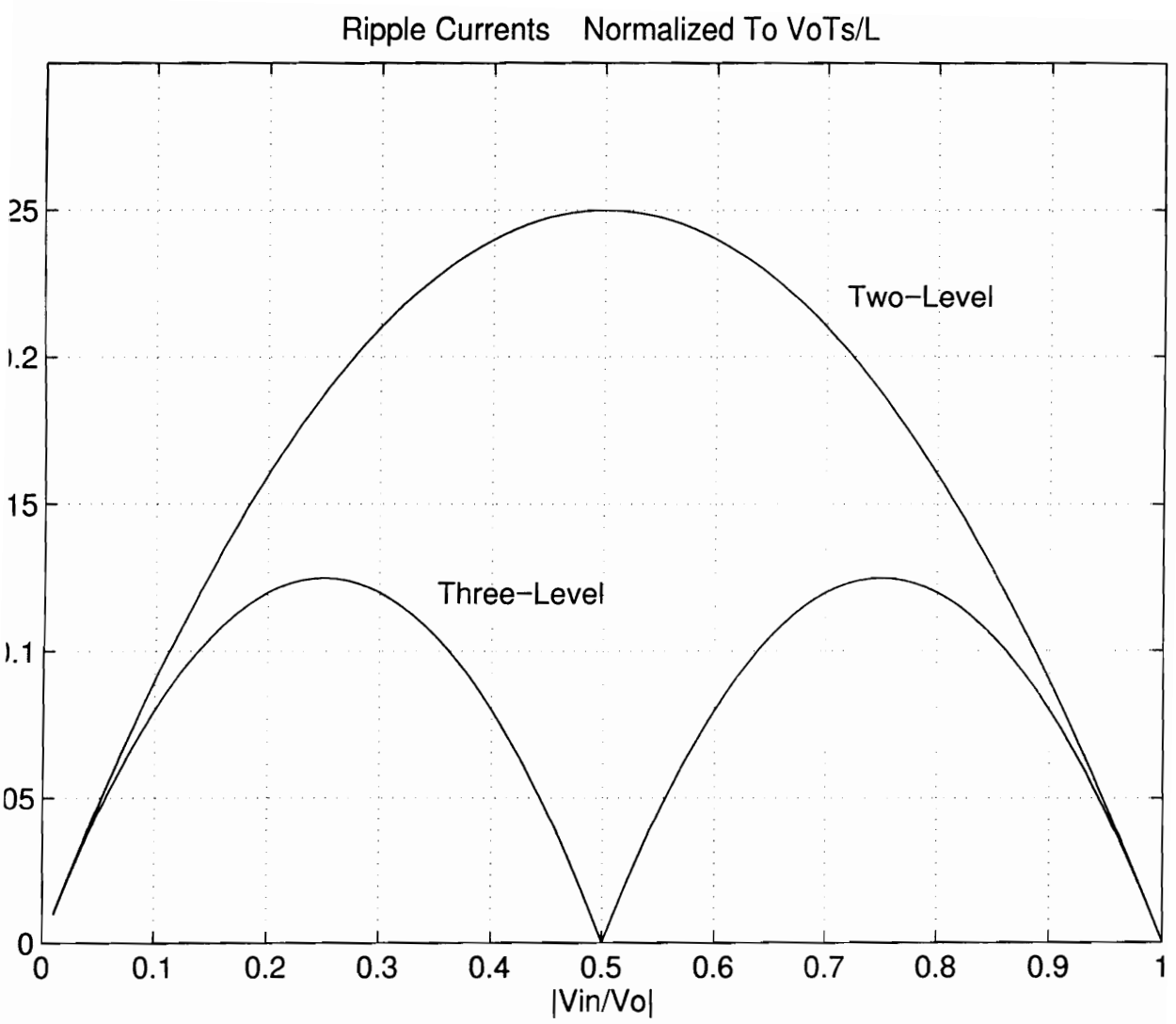


Figure 6.8 **Normalized peak-peak inductor current ripple.** The maximum ripple current of the three-level chopper is half that of the two-level chopper under the same power stage parameters.

The comparison of the peak-peak ripple currents with same converter parameters is shown in Fig. 6.8. The ripple currents are normalized to $V_o T_s / L$. As can be seen clearly, the maximum ripple current of the three-level converter is half the value of that of the two-level converter. The average and rms values of the ripple current over different V_{in} values in the three-level chopper are also reduced to half compared to a two-level chopper. Considering also the reduced switching loss, the product of the switching losses and ripple current in a three-level chopper would be only 25% of that in a conventional one with the same power stage parameters. As a result, the boost inductance can be reduced to 25% to get the same ripple current, making the three-level converter much lighter and smaller, or the switching frequency can be reduced to 25% to achieve higher efficiency. Generally, a k-level converter will have $1/(k-1)$ current ripple and switching loss compared to a conventional converter at the same switching frequency and inductance. Due to the reduced reactive component requirement, and lower voltage stress and power loss of the switches, a multi-level chopper has a significantly lower cost and higher efficiency than a two-level chopper for a given high voltage application.

The charge balance of the dc link center point can be maintained by the proper use of redundant subtopologies. For example, the subtopologies in Fig. 6.6(6) and (7) produce the same value of V_{ab}, but opposite charge flows in the neutral. By slightly adjusting the duty cycles of these subtopologies, any imbalance due to non-symmetry in the circuit and its operation can be easily corrected, and the two dc-link capacitor voltages can be maintained equal. Since the charge balance is maintained at the switching frequency, very high dc-link capacitance is not necessary.

6.2.4 SMALL-SIGNAL MODELING AND CHOPPER CONTROL

The control of the SMES system needs to define the division of the control function between the two-quadrant chopper and the VSI first. There are two apparent options:

(1). The output currents of VSI are controlled according to active and reactive power requirements, while the dc-link voltage is regulated by the two-quadrant boost chopper, which actually controls the active power flow between the SMES coil and the utility.

(2). The dc-link voltage and reactive power transfer of the VSI are controlled by the VSI, and the two-quadrant chopper is controlled according to system active power transfer requirement.

With the first control strategy, the control design of the two-quadrant chopper is very difficult, since the small-signal transfer functions are load-dependent and have right half plane zeros (RHZ) for some operating ranges. The system response is quite sluggish, since the control bandwidth is limited by the RHZ. With the second control strategy, on the other hand, the VSI, together with the dc-link capacitors, presents a voltage source to the chopper, and the chopper works basically as a bi-directional buck converter with an inductive load. With this strategy, the control of the boost chopper is more manageable, since its small-signal transfer functions are all independent of coil current and are minimum phase systems. We will develop the small-signal model of the three-level chopper according to the second control strategy.

With the PWM strategy shown in Table 6.1, only two switches are controlled in the PWM manner in any operating range, and the other two switches are either turned off or kept on. Ideally, the two actively controlled switches have the same duty cycle and are controlled alternately, as is shown in Fig. 6.7. The average model of the three-level converter is shown in Fig. 6.9, in which d is the effective duty cycle of the active switches. D_0 depends on the coil voltage, and is shown in Table 6.2. A small-signal model can be obtained by perturbing the duty cycle d, which is the only control variable in the converter. The resulting small signal model is shown in Fig. 6.10, in which the lower case variables i_1, i_2, v_1, and d represent small-signal variables.

The most distinctive feature of the small-signal model is that the model does not change with load condition, so the control design can be much simplified. From the

small signal model, we can easily get the control (duty cycle)-to-inductor current and coil voltage transfer function as:

$$G_i = \frac{i_l}{d} = \frac{Vo}{2}\frac{S^2 L_2 C + S(R_{l2} + R_c)C + 1}{\Delta},$$

$$G_v = \frac{v_{in}}{d} = \frac{Vo}{2}\frac{S^2 L_2 C R_c + S(R_{l2} R_c C + L_2) + R_{l2}}{\Delta},$$

where:

$$\Delta = S^3 L_1 L_2 C + S^2[L_1(R_{l2} + R_c) + L_2(R_{l1} + R_c)]C + S[(R_{l2} R_{l1} + R_{l2} R_c + R_{l1} R_c)C + L_1 + L_2] + (R_{l1} + R_{l2}).$$

The above transfer functions are plotted in Fig. 6.11. An obvious characteristic of the transfer functions is that the resonance between SMES coil and filter capacitor produces a pair of complex zeros in the control-to-inductor current transfer function G_i. To obtain good dynamics, and especially to ensure current sharing when multi converters are paralleled to increase the power capability, a multi-loop control scheme should be used. The outer loop, i.e. the coil voltage loop, controls the coil voltage, which in turn determines the active power transfer in the system. The inner loop, i.e. the inductor current loop, controls the filter inductor current. The output of the coil voltage controller is the reference for the inductor current. The low frequency gain of G_i, the control-to-inductor current transfer function, is very low due to the existence of complex zeros in very low frequency range, which presents a challenge to the current controller design. To achieve a reasonable low-frequency loop gain, an integrator has to be included in the current compensator to boost the low-frequency gain of the current loop.

Generally, the control of the multi-level chopper should be implemented with DSP or computers. For the three-level chopper, it is also feasible to implement the control strategy of Table 6.1 with discrete IC chips. The control scheme then would be conventional PWM control plus some simple logic. However, DSP-based control is still preferred, since advanced control techniques can be adopted to improve the dynamic performance.

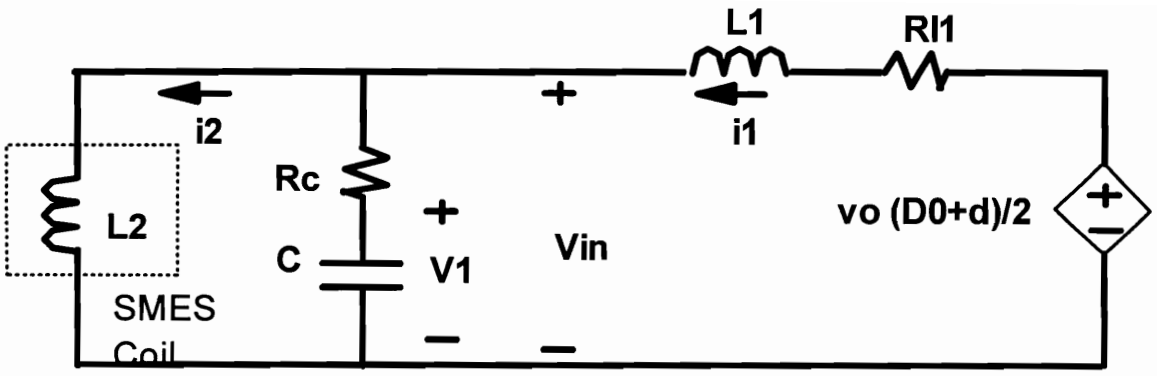


Figure 6.9 Average model of three-level chopper.

Table 6.2 Parameters of the Average Model

Operating Range	Average Voltage V_{ab}	D_0
$-1 < V_{in}/V_o < -0.5$	$V_o\frac{d-2}{2}$	-2
$-0.5 < V_{in}/V_o < 0$	$V_o\frac{d-1}{2}$	-1
$0 < V_{in}/V_o < 0.5$	$V_o\frac{d}{2}$	0
$0.5 < V_{in}/V_o < 1$	$V_o\frac{d+1}{2}$	1

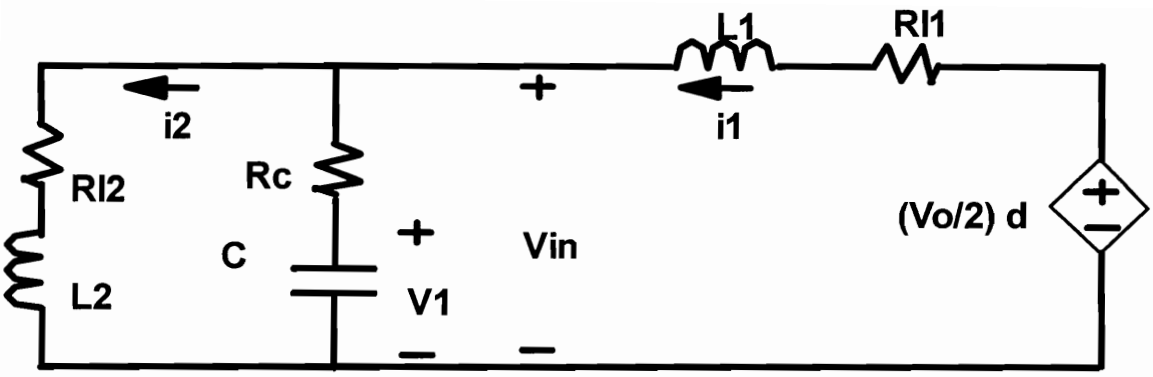
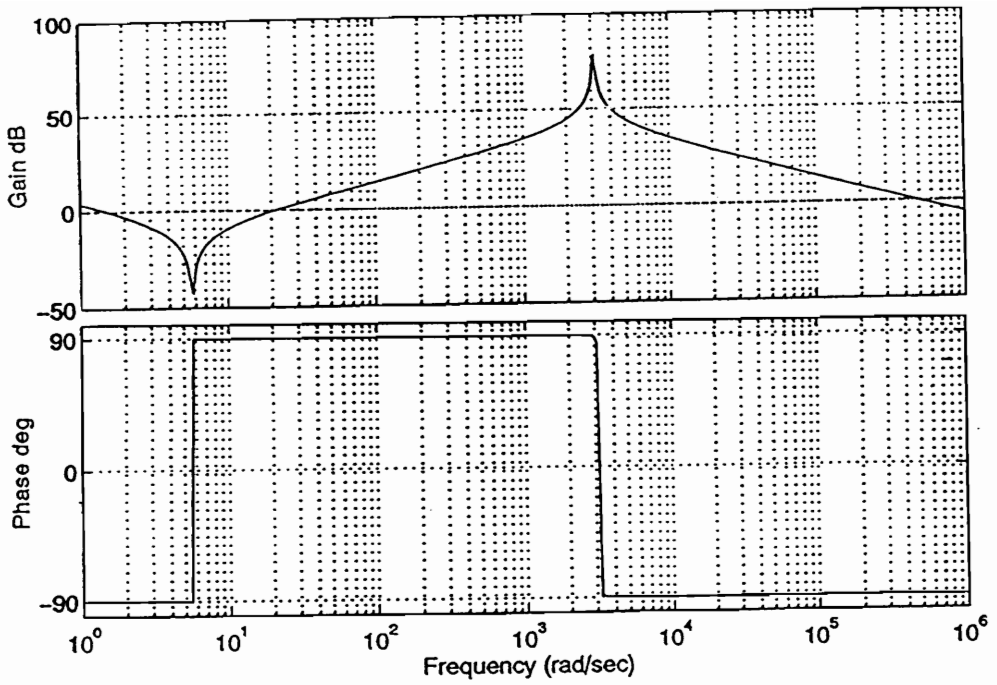
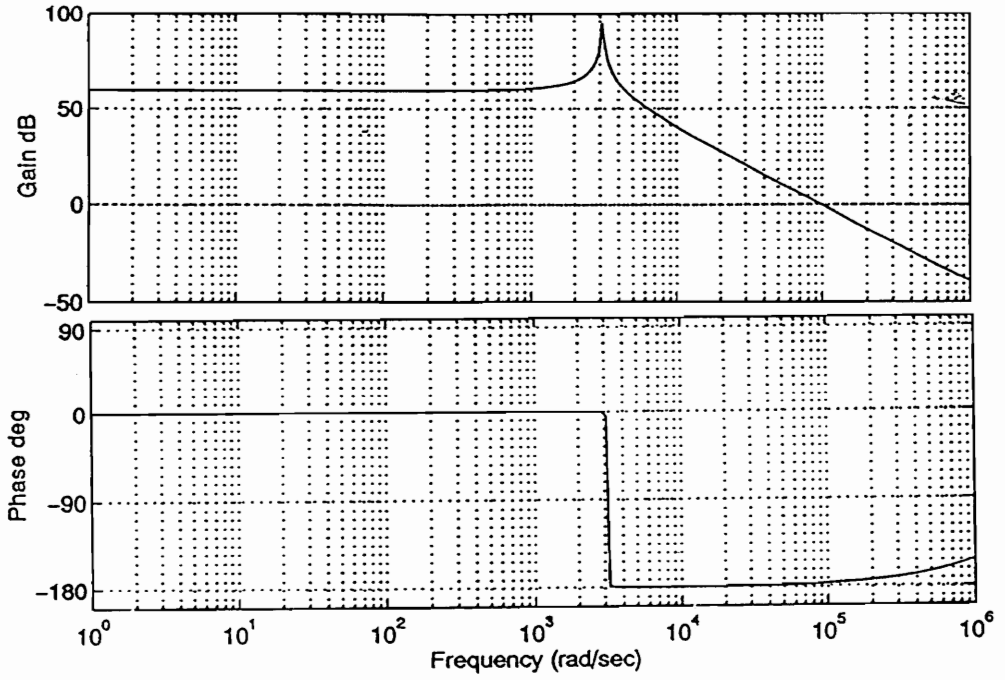


Figure 6.10 Small-signal model of three-level two-quadrant choppers.



(a). Control-inductor current tansfer function G_i



(b)..Control-to-voltage transfer function G_v

Figure 6.11 Power stage small-signal transfer functions.

6.2.5 SIMULATION RESULTS

Simulation has been carried out on an example system shown in Fig. 6.12. The SMES coil is a 600 H inductor with a 1000 A initial current. This corresponds to a 1 MW, 10 minutes power capability. The switching frequency of the converter is chosen to be 5 kHz. The simulated controller parameters are:

$$H_i(s) = (1.5 + \frac{3 \times 10^3}{S}) / (1 + \frac{S}{1.2 \times 10^4})$$

$$Hv(s) = (0.1 + \frac{60}{S}) / (1 + \frac{S}{6 \times 10^3})$$

The simulation results are shown in Fig. 6.13. Fig. 6.13(a) shows the key voltage and current waveforms in the steady state. The ripple of the inductor current is much smaller than in a two-level chopper, and the ripple of coil voltage is less than 1%. It can also be seen that the switch voltage is nicely clamped at 1000 V, half the output voltage. Fig. 6.13(b) shows the transient responses to a slope voltage reference. The coil current is constant during the whole transient and is not shown in the diagram. Obviously, the system is stable and follows the reference voltage quite well. The coil voltage response is reasonably smooth, greatly reducing the possibility of dangerous coil resonance. These results prove that the converter performance is satisfactory.

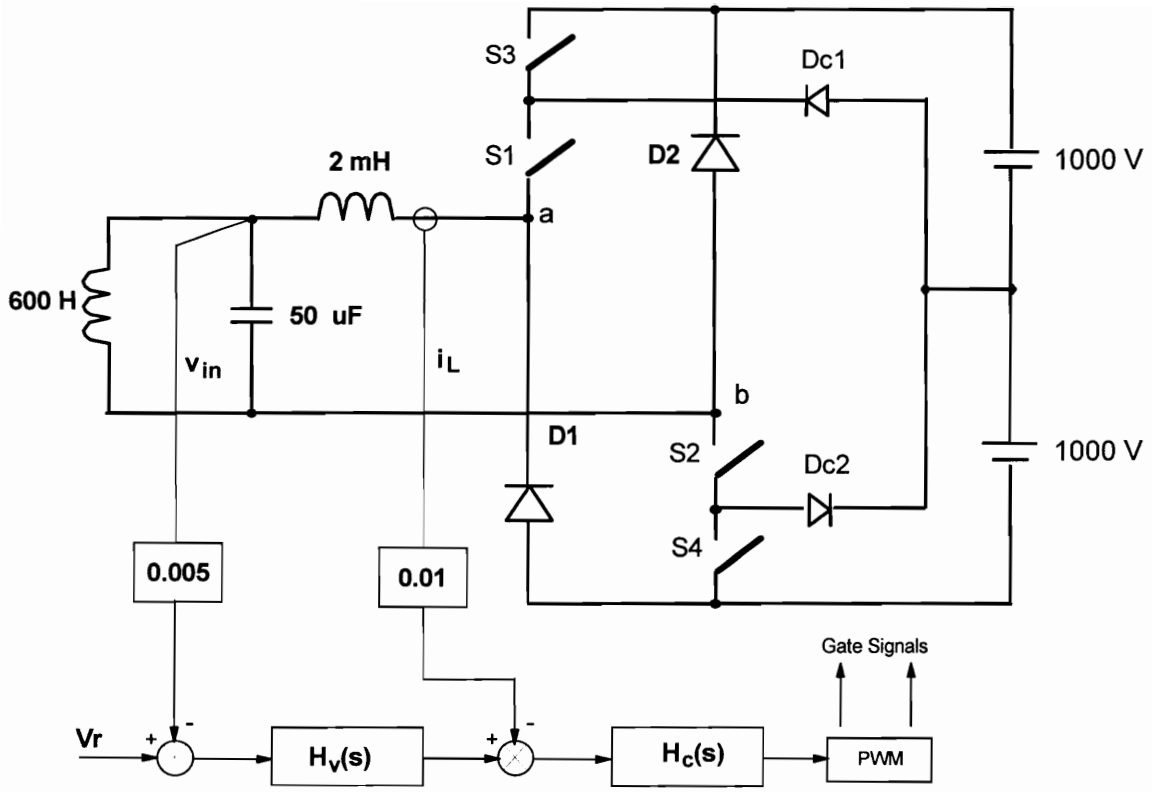
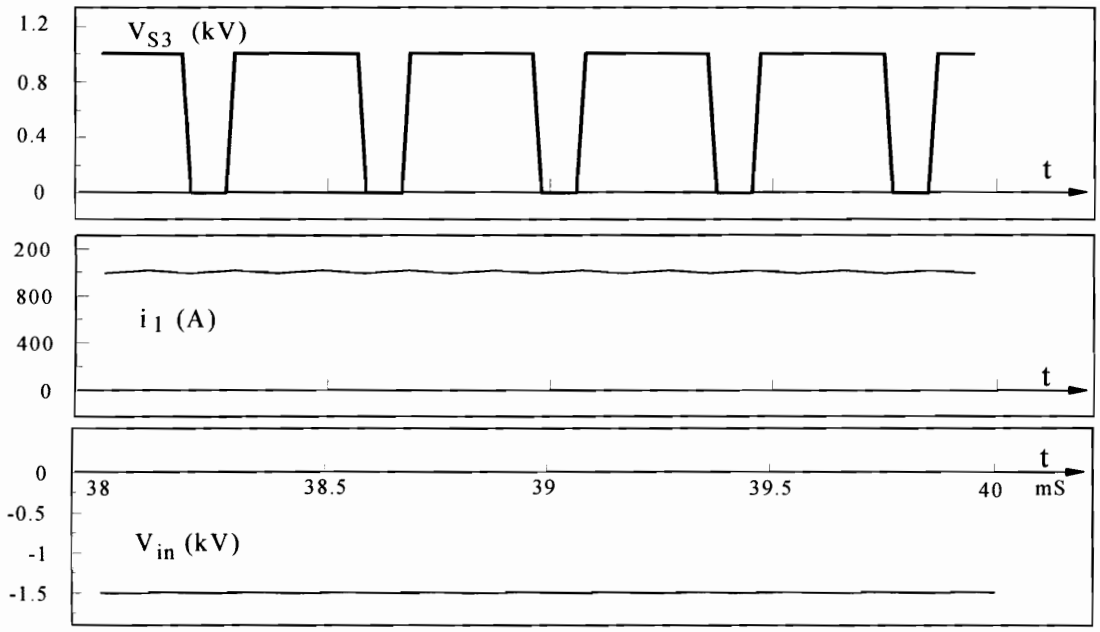
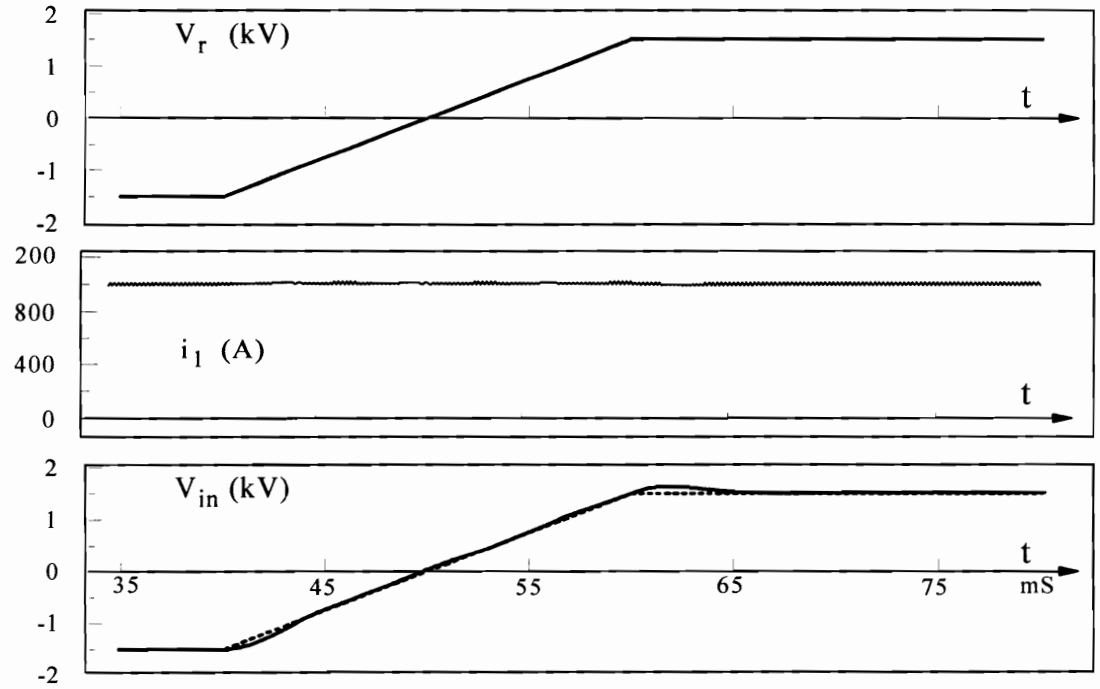


Figure 6.12 **Prototype converter used in the simulation.** Multi-loop control is used to enhance the control performance.



(a) Steady-state waveforms



(b) Transient responses

Figure 6.13 Simulation results.

6.2.6 SOFT-SWITCHING TECHNIQUES FOR TWO-QUADRANT BOOST CHOPPERS

The basic topology of three-level chopper is shown in Fig. 6.5. The main diodes in this topology need to block the full output voltage. For some applications, this is acceptable, since high-voltage diodes are available, and the series connection of diodes, if necessary, is not a big problem. However, it might be desired to reduce the voltage stress of the diodes in some other applications. The voltage rating of these diodes can be reduced by additional clamping diodes, as is shown in Fig. 6.14, where all switches and diodes block half the output voltage. Unlike other devices, the clamping diodes Dc3 and Dc4 do not conduct a significant current, and have a very small power rating. This section will investigate the soft-switching techniques for the basic two-quadrant three-level chopper topologies shown in Figs. 6.5 and 6.14

Lets first look into the soft-switching topologies for two-level choppers to gain some insight. Soft-switching topologies of the two-quadrant choppers can be obtained using the ZVT techniques and ZCT techniques with the concept of PWM cells. Due to the high power nature of the converters, the auxiliary switches in any soft-switching chopper should be switched with reduced stresses also. For example, the voltage rating of the auxiliary switches should not be higher than the main switches', and the turn-off current of the auxiliary switches should be zero, or at least much lower than the main inductor current. According to the switching commutation, in the two-level chopper of Fig. 6.2, S1 and D1 make up a PWM cell, while S2 and D2 make up the other PWM cell. The corresponding ZCT and ZVT soft-switching topologies based on the ZCT cell and ZVT cell are shown in Fig. 6.15. Fig. 6.15(a) shows the basic ZVT topology, which is the direct application of the ZVT technique proposed in [A32]. This topology is not practical, since the auxiliary switches are required to turn off high currents. A modified ZVT topology is shown in Fig. 6.15(b), which adopts the coupled inductor technique in [A33] to reduce the current stress of the auxiliary switches. Fig. 6.15(c) shows a ZCT

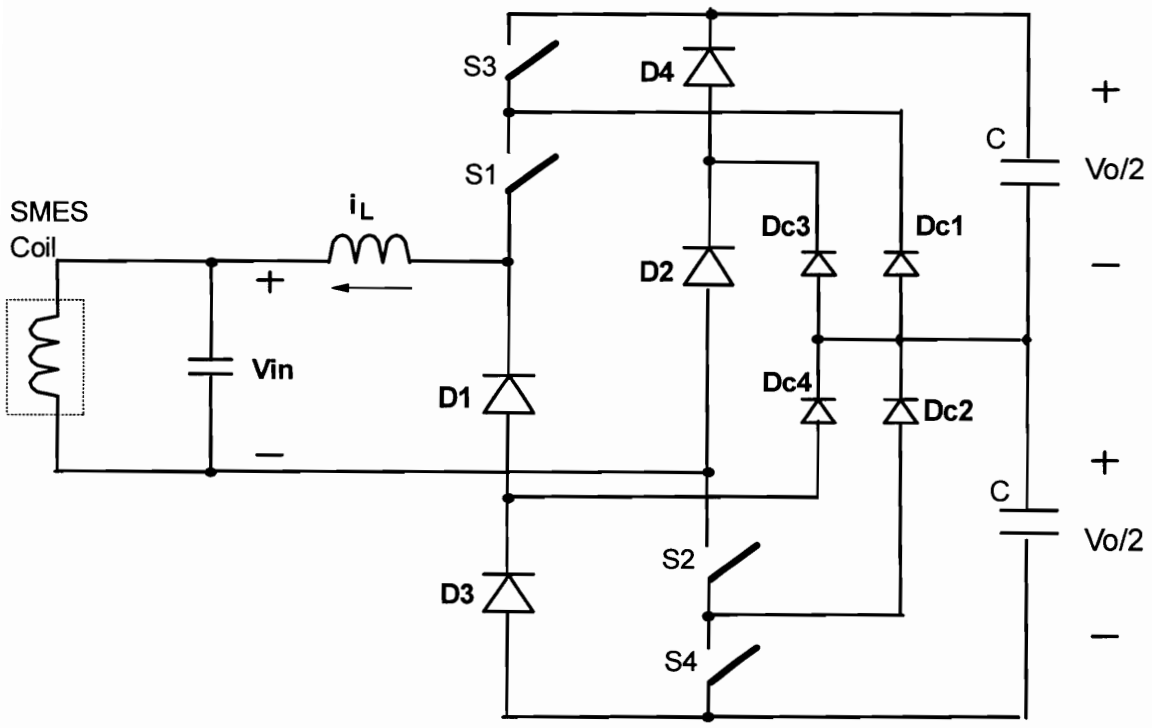
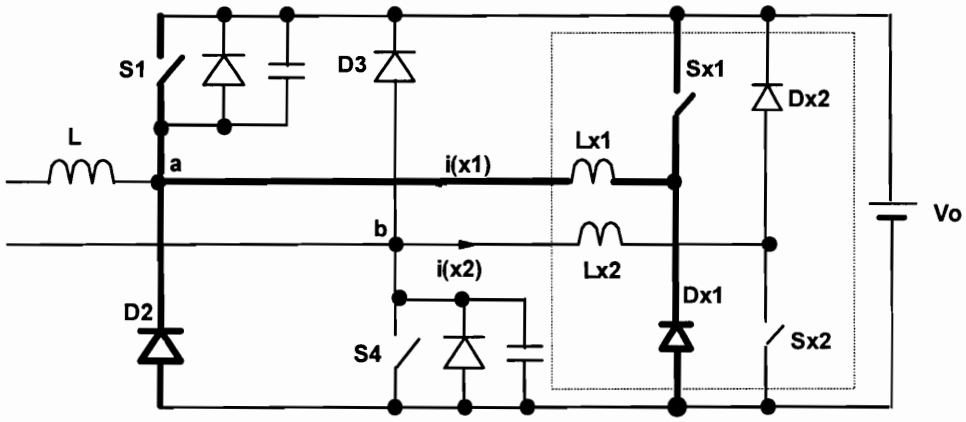
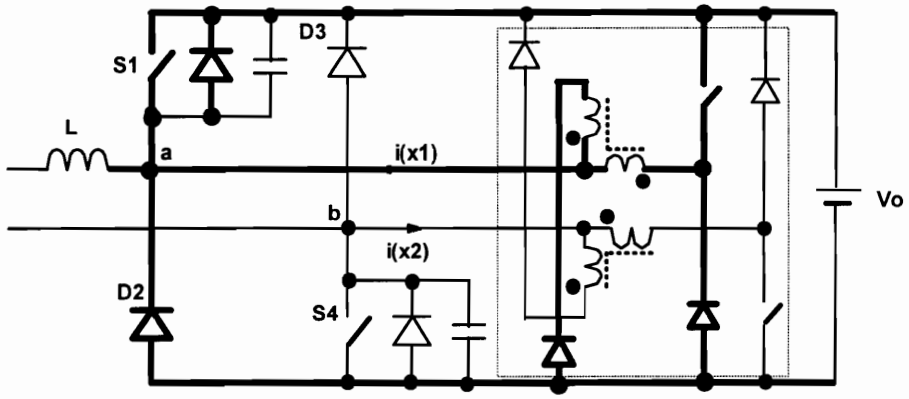


Figure 6.14 Three-level chopper with reduced diode voltages.

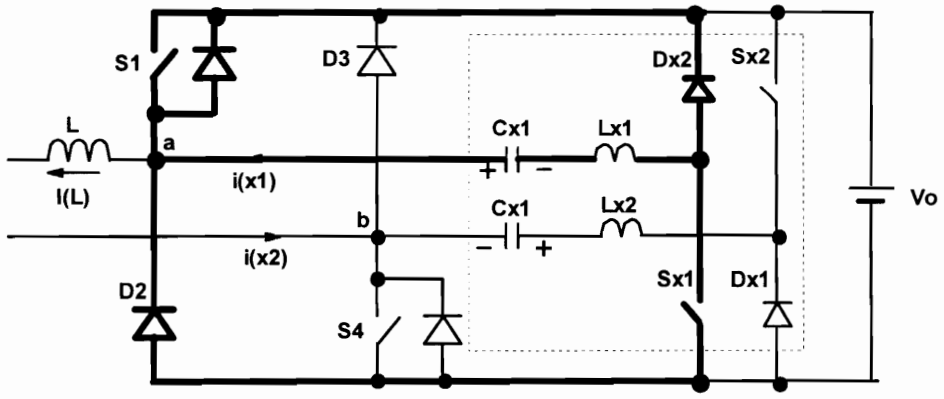
topology with the improved ZCT cell in Fig. 2.6(c). The operations of the soft-switching circuits in these topologies are exactly the same as in the dc-dc converters. In the three-level converter shown in Fig. 6.5 and with the control strategy of Table 6.1, four PWM cells can also be identified: S1 and D1, S2 and D2, S3 and Dc1, and S4 and Dc2. The ZVT and ZCT cell concepts can again be used to derive soft-switching topologies. The basic ZVT topology is shown in Fig. 6.16(a), and the modified ZVT topologies are shown in Figs. 6.16(b), which provides soft switching for the auxiliary switches also. Similar ZVT topologies can also be derived for the three-level converter in Fig. 6.14. However, if the ZCT cells are directly applied to the PWM cells in Fig. 6.5, the auxiliary switches will be subject to full dc-link voltage, which is twice the main switches' voltage stress, and thus not desired. Instead, the ZCT cells can be applied to the topology shown in Fig. 6.14 without increasing auxiliary switch voltage stress. The resultant topology is shown in Fig. 6.16(c). It should be pointed out that the ZCT topology has a small modification from the original ZCT cell. Two clamp switches, Sc1 and Sc2, are added to diodes D1 and D2, and are turned on when S3 and S4 are not conducting. The purpose of Sc1 and Sc4 is to clamp D1 and D2 voltages at zero, so that a current path is provided to the resonant current during the ZCT operation for S1, D3 and S2, D4 pairs. It should also be noted that Sc1 and Sc2 are always turned on and off with a zero-current and zero-voltage condition, and therefore their switching loss is negligible. Their conduction loss is also very small because of the short conduction time. Since the operation of the soft-switching schemes is very similar to that of the original ZCT and ZVT cells, no further description is necessary.



(a). Basic ZVT topology with the ZVT cell in [A32]

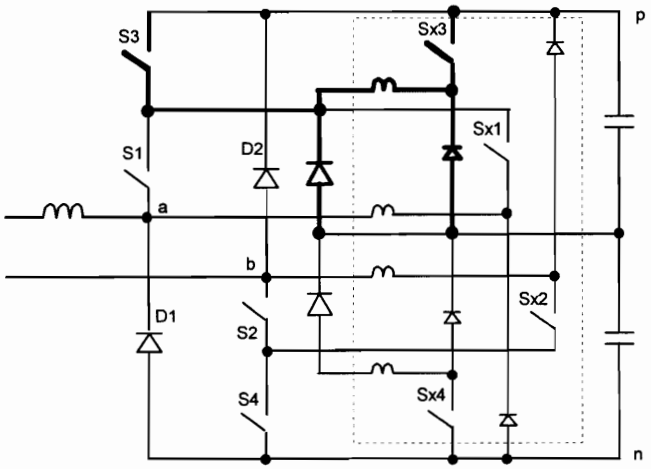


(b). Modified ZVT topology with coupled inductors in [A33]

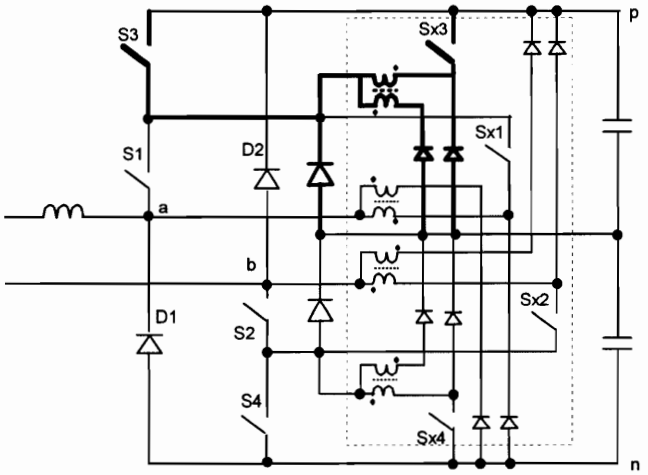


(c). ZCT topology with the ZCT cell in [A42]

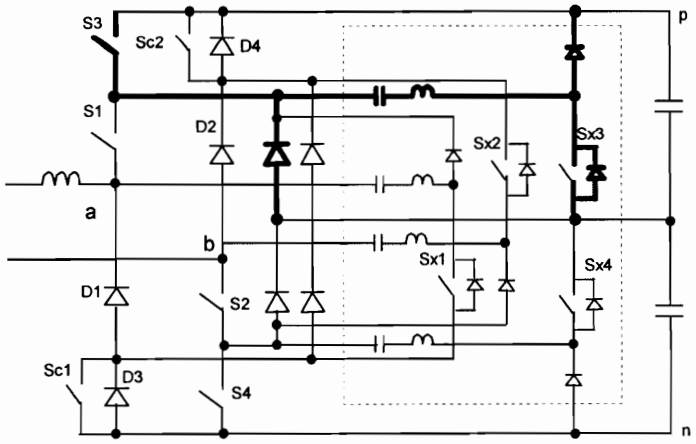
Figure 6.15 **Soft-switching two-quadrant choppers.** ZVT and ZCT mechanism is applied directly to each PWM cell.



(a). Basic ZVT three-level chopper



(b) Modified ZVT three-level chopper with coupled inductors



(c) ZCT three-level chopper

Figure 6.16 **Soft-switching three-level two-quadrant chopper**. ZVT and ZCT mechanism is directly applied to each PWM cell.

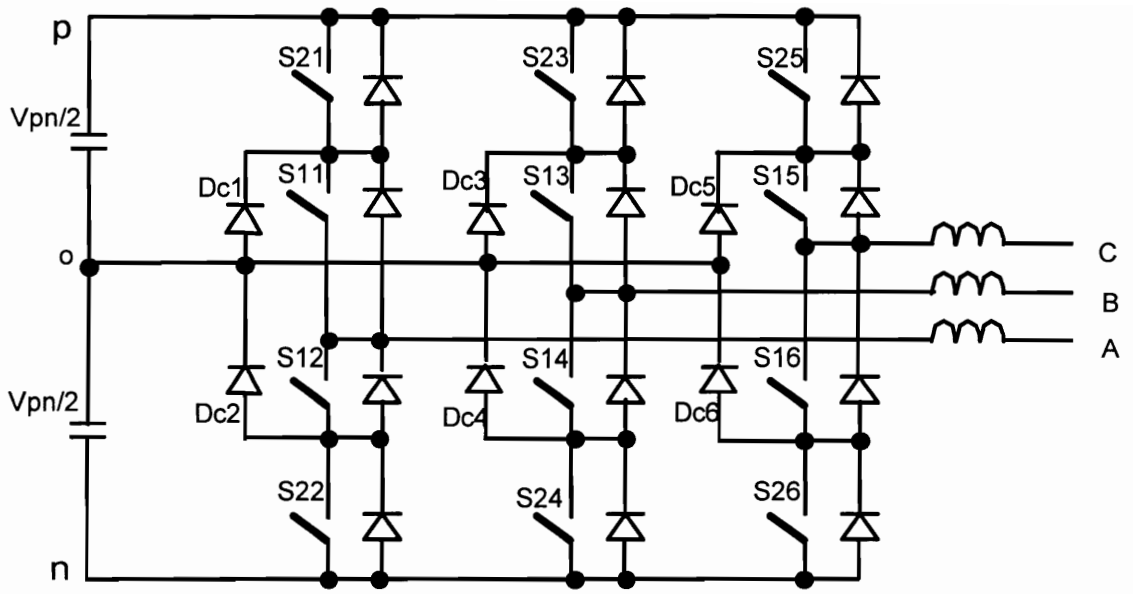
6.3 SOFT-SWITCHING TECHNIQUES OF THREE-LEVEL THREE-PHASE PWM VOLTAGE SOURCE INVERTERS

6.3.1 INTRODUCTION

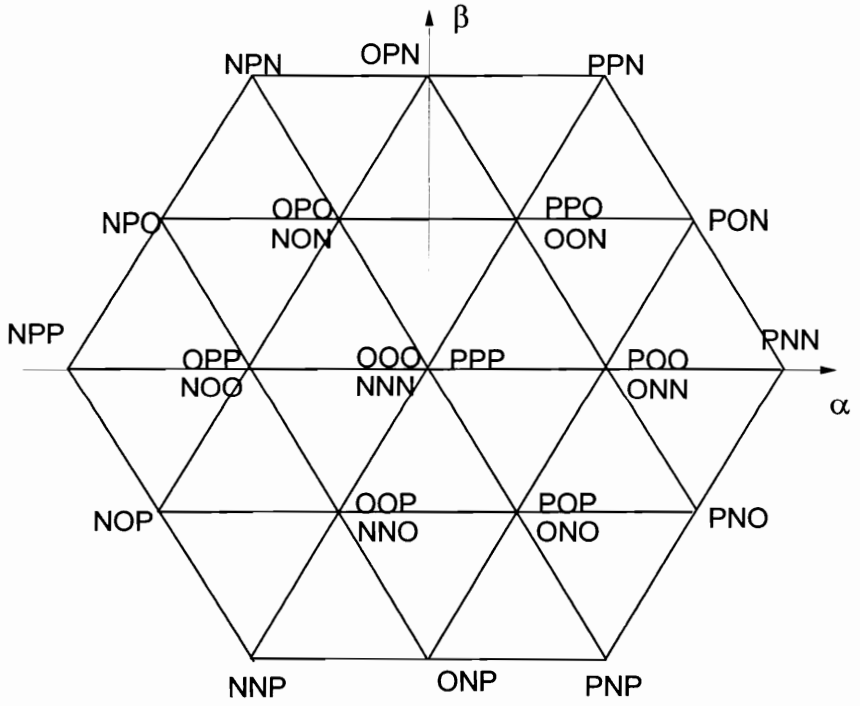
Soft-switching techniques are very important to reducing the switching loss, stress, and noise of multi-level three-phase converters. Again, to deal with the high voltage and high current, the auxiliary switches in the soft-switching circuit should have minimum switching loss and stress. In this section, using a three-level inverter as an example, PWM cells will be identified first in a inverter leg, and then ZVT and ZCT cells will be used to achieve soft switching for power switches.

6.3.2 SPACE VECTOR MODULATION AND PWM CELLS IN THREE-LEVEL THREE-PHASE PWM INVERTERS

The topology of a three-phase three-level inverter is shown in Fig. 6.17(a). S11~S16 are six inner switches, S21~S26 are six outer switches, and Dc1~Dc6 are six clamping diodes. According to the switch states, the phase nodes a, b, and c can be connected to three points: positive dc rail "p", negative dc rail "n", and center point "o"; thus, each phase can have three voltage levels: Vdc/2, 0, and -Vdc/2. The availability of more voltage levels than in a two-level inverter can be used to reduce the switching loss and output current ripple of the converter. As in the two-level inverters, voltage space vectors can be used to represent the voltages in a multi-level inverter. In a three-phase three-level inverter, twenty four non-zero and three zero voltage vectors can be produced by different switch combinations, as is shown in Fig 6.17(b). In Fig. 6.17(b), each node represents a voltage space vector, and the text next to it illustrates the corresponding switch combination. Various SVM schemes are proposed to optimize the performance of switching loss, output current ripple, and dc-link voltage balance [C9]-[C14]. However, in a good modulation scheme, any phase voltage is switched only between two adjacent



(a). Three-phase three-level inverter



(b). Voltage space vectors in a three-level inverter

Figure 6.17 **Three-phase three-level inverter and its space vectors.** The redundant vectors can be used to optimize switching loss, inductor current ripple and dc-link midpoint charge balance.

voltage levels at one switching event, for example, from Vdc/2 to 0, or from 0 to -Vdc/2, etc.. Then, there are four possible current commutation patterns in each inverter leg. Since the three inverter legs operate in the same manner, only one leg, here the Phase A leg, will be discussed. The current commutation patterns in Phase A are: between S21 and Dc1, between S12 and D21, between S11 and D22, and between S22 and Dc2. From these patterns, four PWM cells of the phase A leg can be identified, and are shown in Fig. 6.18. It should be noted that when an inner switch (S11~S16) is switched over with an outer diode (D21~D26), another inner switch in the same leg can be turned on also. For example, when the switching action is between S11 and D22, then S12 should be turned on. The turn-on of S12 does not affect the circuit operation except in the switching transition, because S12 does not conduct any current in the normal operation. However, S12 will provide a current path in soft-switching commutations.

6.3.3 SOFT-SWITCHING TOPOLOGIES FOR THREE-LEVEL INVERTERS

Soft-switching PWM topologies can be achieved by replacing the PWM cells with ZVT and ZCT cells discussed in Chapter 2 and Chapter 3. Several ZCT and ZVT topologies are shown in Fig. 6.19, with the example of one inverter leg. The ZCT topology shown in Fig. 6.19(a) is the direct application of the ZCT cell in Fig. 2.6(c). One of the ZCT cells is shown in Fig. 6.19(a) with thickened lines. The ZVT topology of Fig. 6.19(b) is the application of the modified ZVT technique in [A33], with the ZVT cells for S11 and S12 combined together. The operation of the ZVT cells and ZCT cells in these two topologies is similar to that in dc-dc converters. However, in the ZVT topology of Fig. 6.19(c), which is an extension of the ARCP technique in [B27], the charge balance requirement at the points of "po" and "no" will limit the operation of the auxiliary circuit. Without additional circuitry and control, the charge balance can be maintained in the converter only at zero power factor. Therefore, this topology is mainly for reactive power control such as in static var compensators (SVCs).

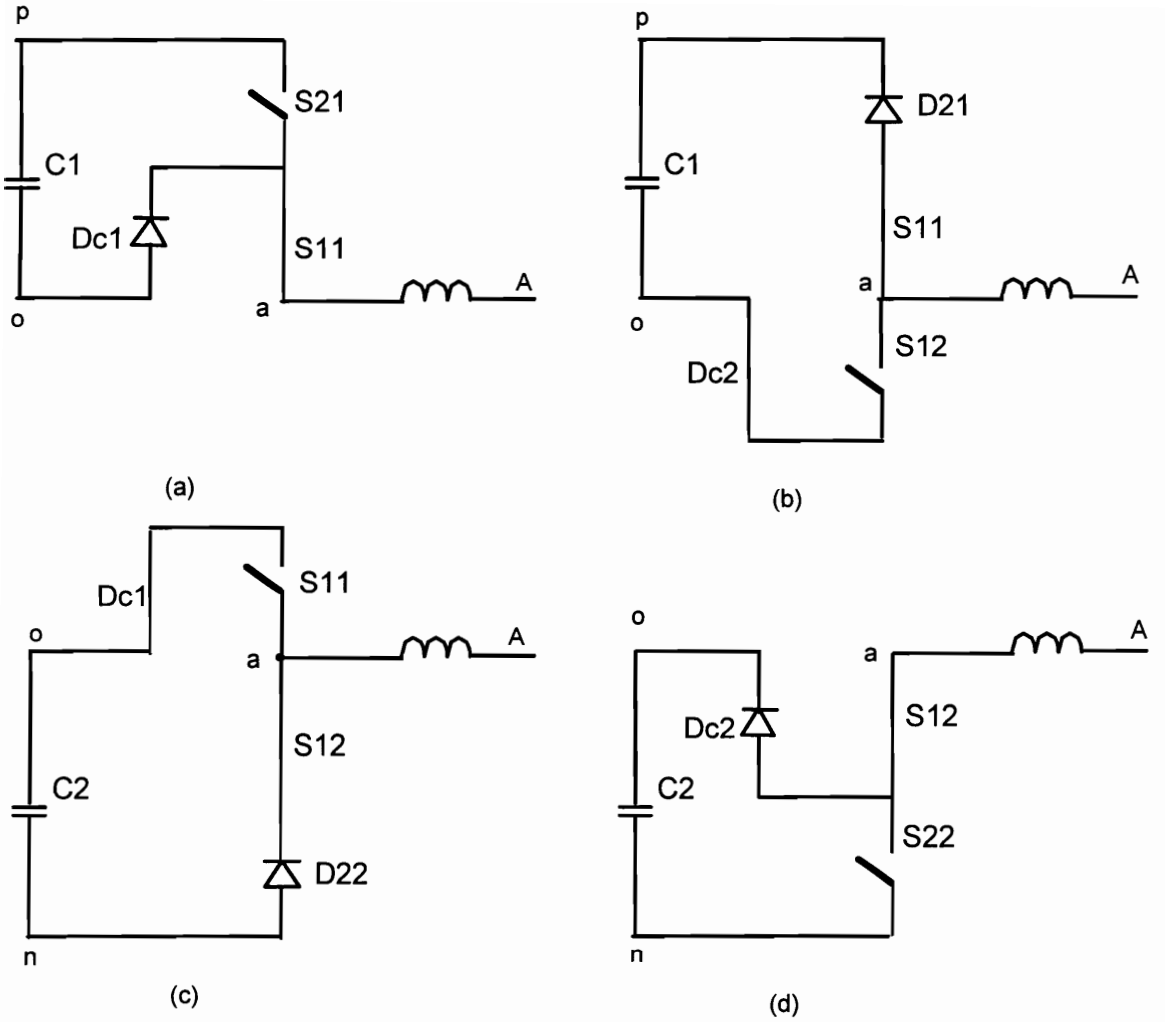
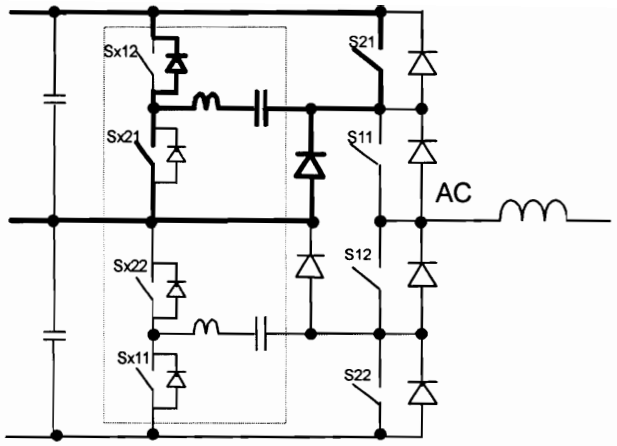
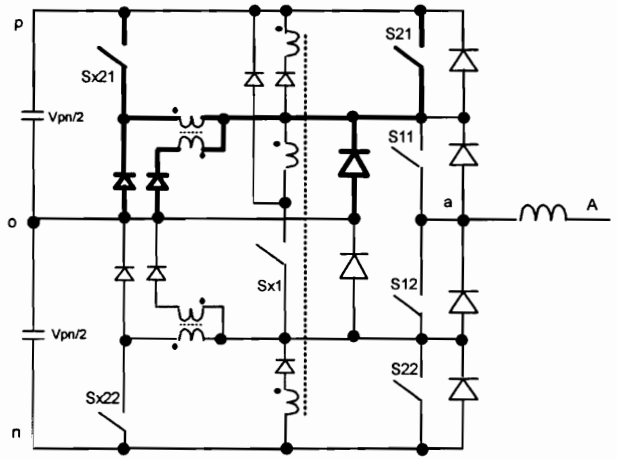


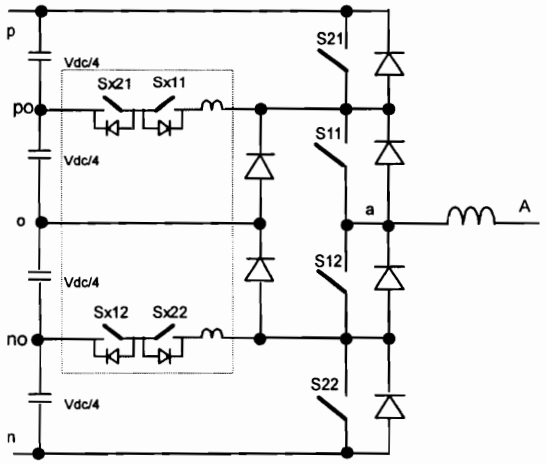
Figure 6.18 **PWM cells in a three-level inverter leg.** The switches and diodes are grouped into four switch-diode pair.



(a). ZCT topology



(b). ZVT topology with coupled inductor



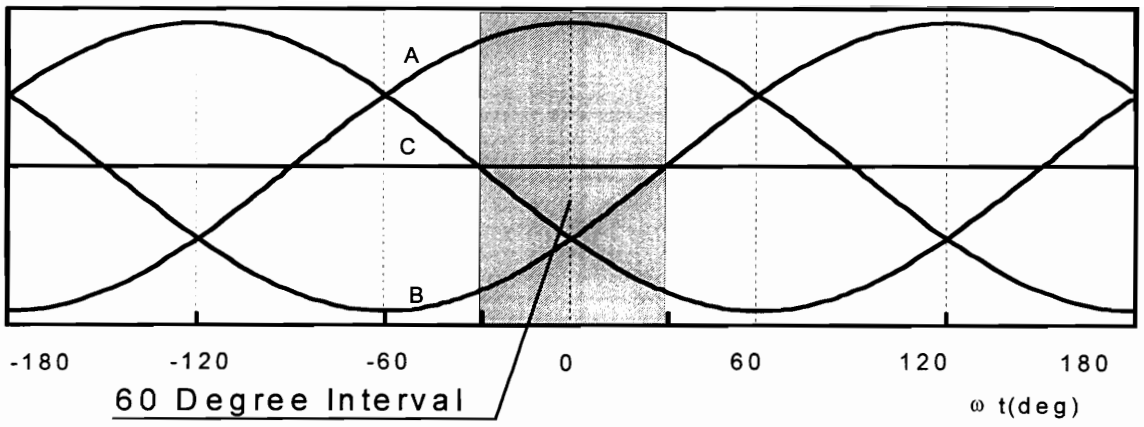
(c). ZVT topology with ARCP

Figure 6.19 **Soft-switching three-level inverter leg.** Soft-switching mechanism is directly applied to each PWM cell.

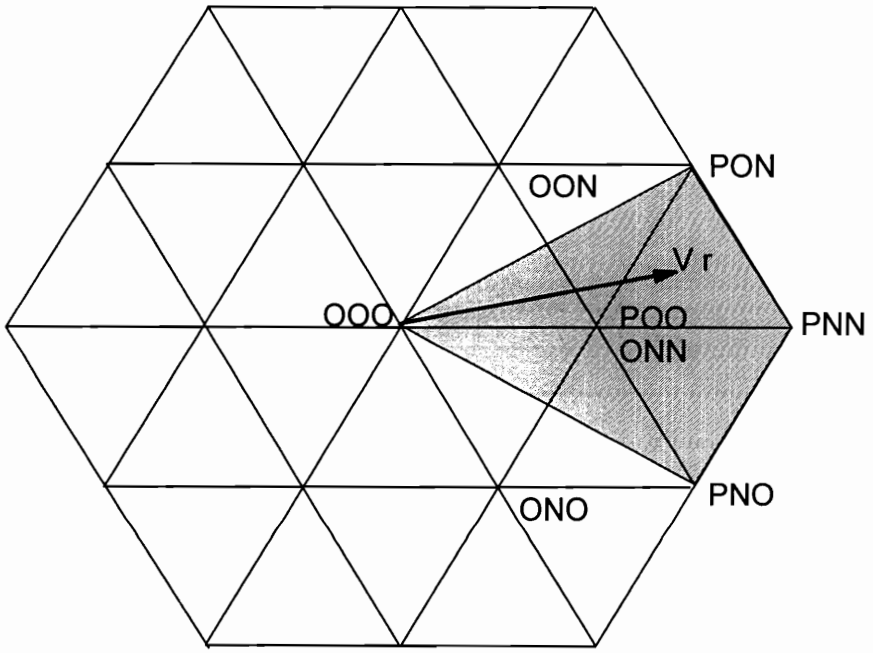
6.4 THREE-PHASE THREE-LEVEL ZERO-VOLTAGE TRANSITION BOOST RECTIFIERS

6.4.1 INTRODUCTION

The three-level boost rectifier is an attractive topology for high-power PFC applications, because the advantages of multi-level conversion are more prudent in rectifiers. For example, good input current control and low EMI emission are two principal requirements in PFC applications, which require a high switching frequency and low input current ripple. With the same power stage parameters, both the switching loss and maximum current ripple in a three-level rectifier can be reduced to half their values in a two-level rectifier. Although any multi-level inverter can operate as a rectifier also, the rectifier topology can be simplified, considering the fact that the input voltages and currents are controlled in phase in a PWM rectifier. Therefore, not all vectors in Fig. 6.17(b) are necessary to control a rectifier. For example, in the 60° interval of $v_a > 0$, $v_b < 0$, and $v_c < 0$ shown in the shaded area of Fig. 6.20(a), there exists a relationship between the three input currents: $i_a > 0$, $i_b < 0$, and $i_c < 0$. The reference voltage vector in this period will be in the shaded area shown in Fig. 6.20(b), and can be synthesized with only the switch combinations shown in Fig. 6.20(b), which are only a subset of the space vectors in Fig. 6.17(b). With this control scheme, the six outer switches never conduct current (but the outer diodes will conduct current). Due to the symmetry of the three-phase converter operation, this conclusion holds under other operating conditions also. Therefore, the six outer switches can be removed from an inverter topology, and the resultant three-level rectifier topology can be simplified from Fig. 6.17(a) into Fig. 6.21(a). This topology is the basis for further simplification. One drawback of this topology is that a phase current is always conducted by a diode and a switch(or its anti-parallel diode). Because an active switch conducts current only when that phase is connected to the dc-link midpoint, the switches and the clamping diodes can

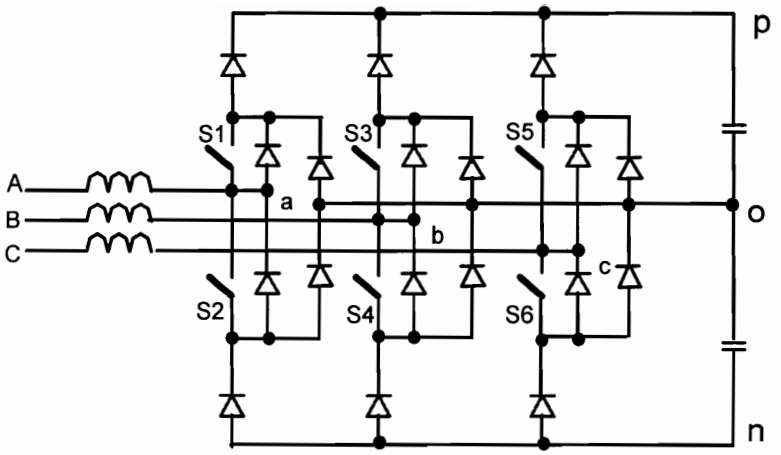


(a). Phase voltages

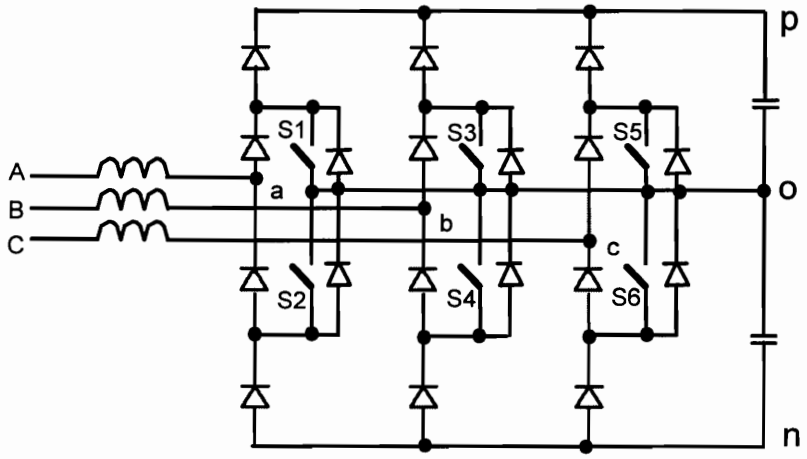


(b). Corresponding active space vectors

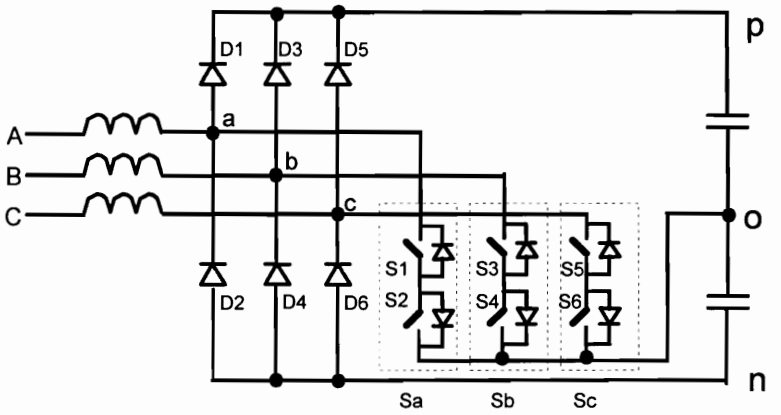
Figure 6.20 **Active voltage space vectors of three-level rectifier in a 60° interval.** Three-phase voltages within the shaded area in (a) correspond to space vectors in the shaded area of (b). The reference voltages in the shaded area can be synthesized with the eight vectors depicted in (b).



(a). Remove outer switches from three-level inverter. The active switches conduct current only when that phase is connected to the dc-link midpoint.



(b). Interchange the active switches with clamping diodes.



(c). Combine the diodes in the main power path to reduce conduction loss.

Figure 6.21 Topology development of three-phase three-level rectifiers.

exchange their positions without affecting the control of the converter. Such a rectifier topology, shown in Fig. 6.21(b), was proposed in [C5]. Now an active switch conducts current only when that phase is connected to the dc link center point. Therefore, the current rating of the active switches is reduced, resulting in lower power loss and converter cost. Still, a phase current is conducted by two devices at any time: either two diodes or a diode and a switch. By rearranging the switches, another three-level rectifier is developed in [C6] and shown in Fig. 6.21(c), in which the number of main diodes is reduced. The bi-directional switches Sa, Sb, and Sc can have different implementations, and the one shown in the figure is appropriate for IGBTs. At a lower power level, a bi-directional switch can be also implemented as a diode bridge and a switch when MOSFETs are used. It is also possible to shift the bi-directional switches into the main bridge, as discussed in [C23]. Then a phase current will be conducted by at least two diodes, and the converter will have more power loss.

The soft-switching technique of the three-level rectifiers has been addressed in [C22]. However, the ZVT topology proposed there requires the auxiliary switch to block full output voltage, and all three phase currents are commutated from diodes to switches in each switching cycle. Therefore, the turn-off loss of the main switches is increased compared with that in an optimum SVM scheme, offsetting the efficiency improvement of the soft-switching operation to a certain degree. In this section, using the main power stage of Fig. 6.21(c) as an example, several improved ZVT topologies will be presented.

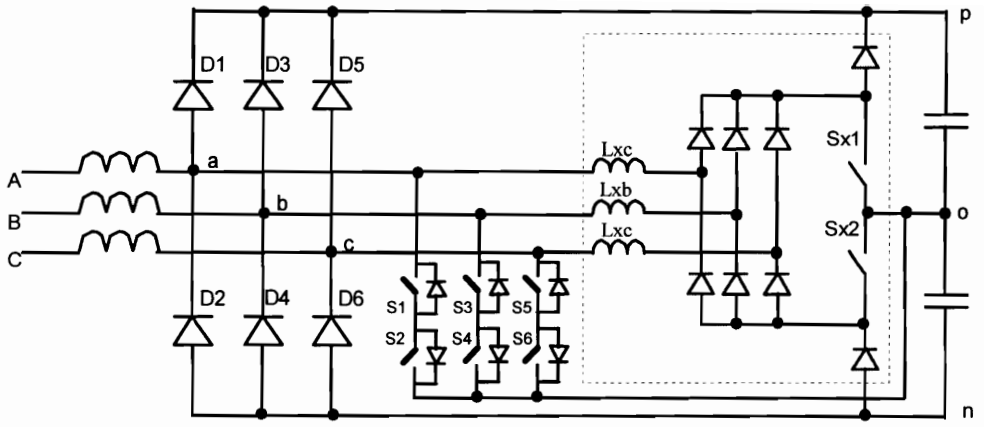
6.4.2 TOPOLOGY DESCRIPTION

Three similar ZVT topologies for the three-phase three-level rectifier shown in Fig. 6.21(c) are shown in Figs. 6.22(a), (b), and (c). The soft-switching auxiliary circuits have structures similar to the ZVT circuits for two-level converters discussed in Chapter 3. In all these topologies, Sx1 is used to help the commutation from D1, D3, and D5 to S1, S3, and S5, while Sx2 is used to help the commutation from D2, D4, and D6 to S2, S4, and

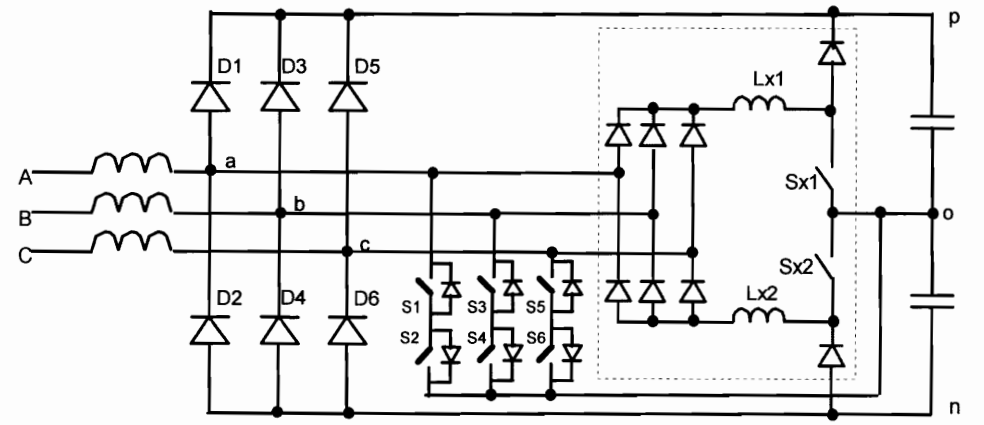
S6. The functional differences among these three topologies are very small, so only the one shown in Fig. 6.22(b) will be discussed in detail.

Consider the 60° interval of $v_a > 0$, $v_b < 0$, and $v_c < 0$ (thus $i_a > 0$, $i_b < 0$, and $i_c < 0$), which is shown as the shaded area of Fig. 6.20. With the available space vectors shown in Fig. 6.20(b), there exist a number of SVM schemes to control the converter. One example is shown in Figs. 6.23(a) through (f), in which the available vectors are shown as dotted lines with arrows, and the reference voltage vector Vr is shown as a solid line with an arrow. The whole 60° interval is divided into six regions, which are illustrated as shaded areas, and labeled as (a) through (f) in Fig. 6.23. The switching sequence for each region is shown at the bottom of each figure. Whenever the reference vector enters that region, the corresponding switching sequence will be used to control the converter. In this scheme, the vectors used are all adjacent to the reference vector, and there is one phase current not switched in each region, so the switching loss and current ripple are minimized, while the control capability is maximized. Notice that the conducting diodes on one side of the main diode bridge are always commutated off at the same time. For example, in the region shown in Fig. 6.23(d), D4 and D6 are turned off and Sb and Sc are turned on simultaneously in the transition from PNN to POO. Fig. 6.24(a) shows the converter PWM operating stages in a switching cycle, in which the auxiliary circuit provides soft-switching transition from PNN to POO. The active current path in each operating stage is shown as thick lines.

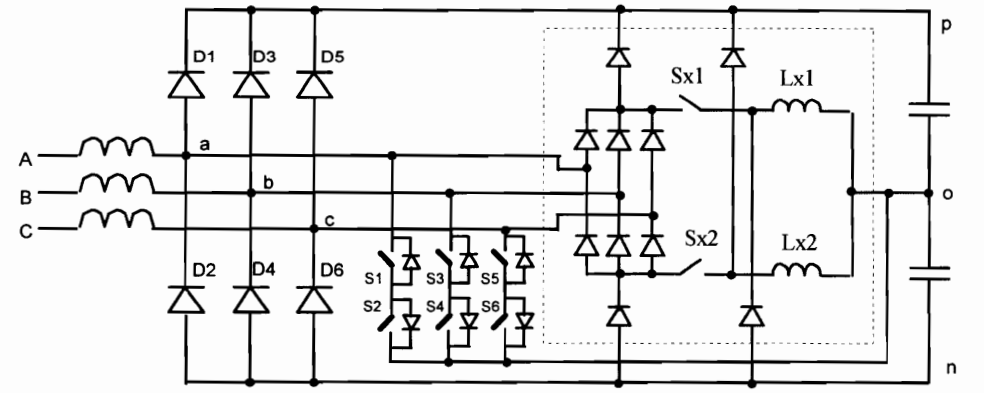
Before the turn-on commutation, D1, D4, and D6 are conducting the three phase currents. S2, S3 and S5 can be turned on without power loss, because their voltages are zero due to their forward-biased anti-parallel diodes. The turn-on of these switches does not affect the converter operation, because they cannot conduct currents due to the polarities of the phase currents. Since D1 is not to be switched, Sx1 will not be actuated, and Sx2 will be used in the soft-switching transition to help the commutation from D4, D6 to S4, S6.



(a). The soft-switching circuit is similar to that in Fig. 3.7(b).



(b). The auxiliary circuit is similar to that in Fig. 3.9(a).



(c). An alternative implementation of (b).

Figure 6.22 **Zero-voltage transition three-phase three-level rectifiers.** They operate similarly to the ZVT two-level boost rectifiers in Section 3.3.

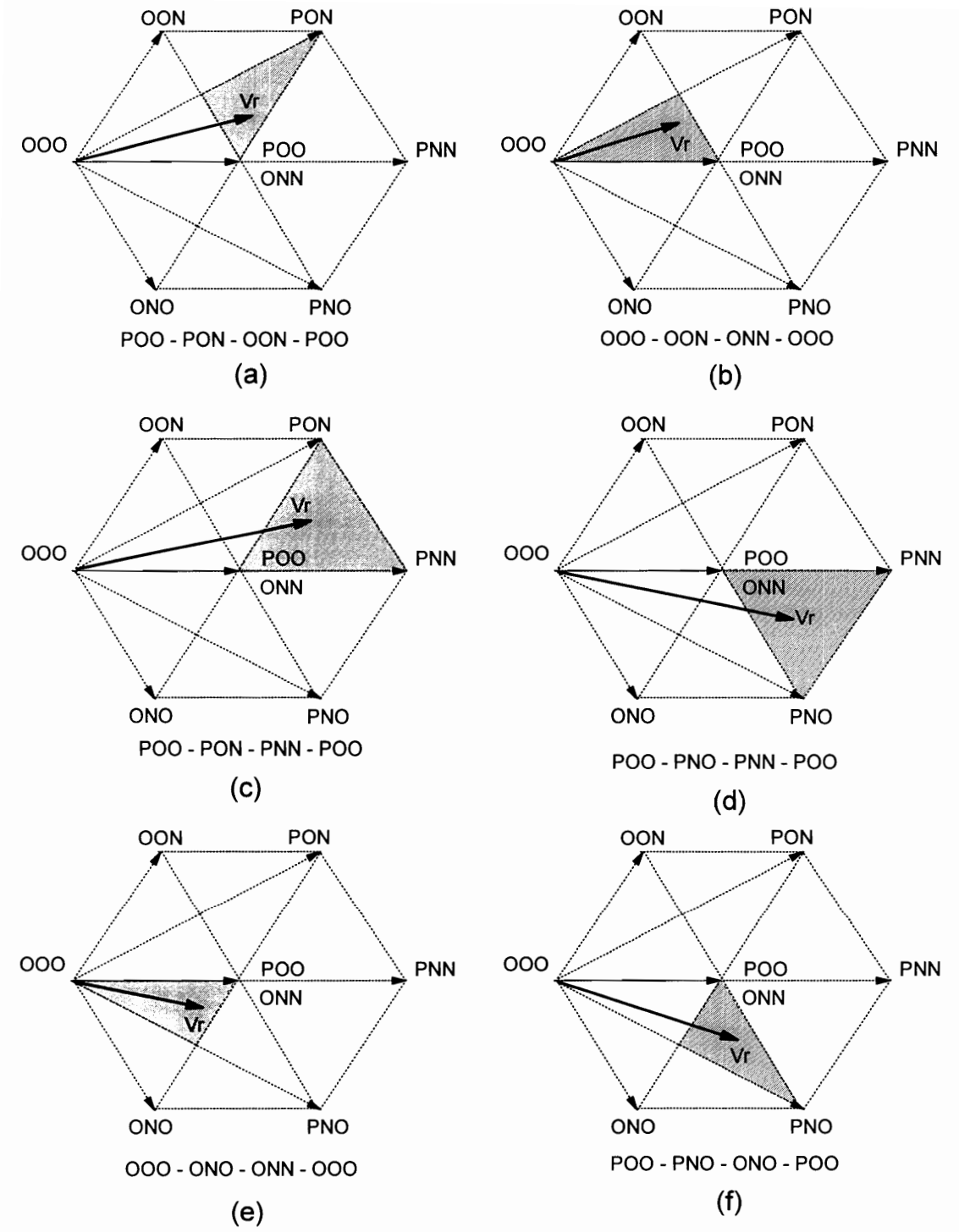


Figure 6.23 **An SVM scheme for three-level rectifier**. The reference vector is synthesized with adjacent vectors, and conducting diodes at the same side are turned off simultaneously.

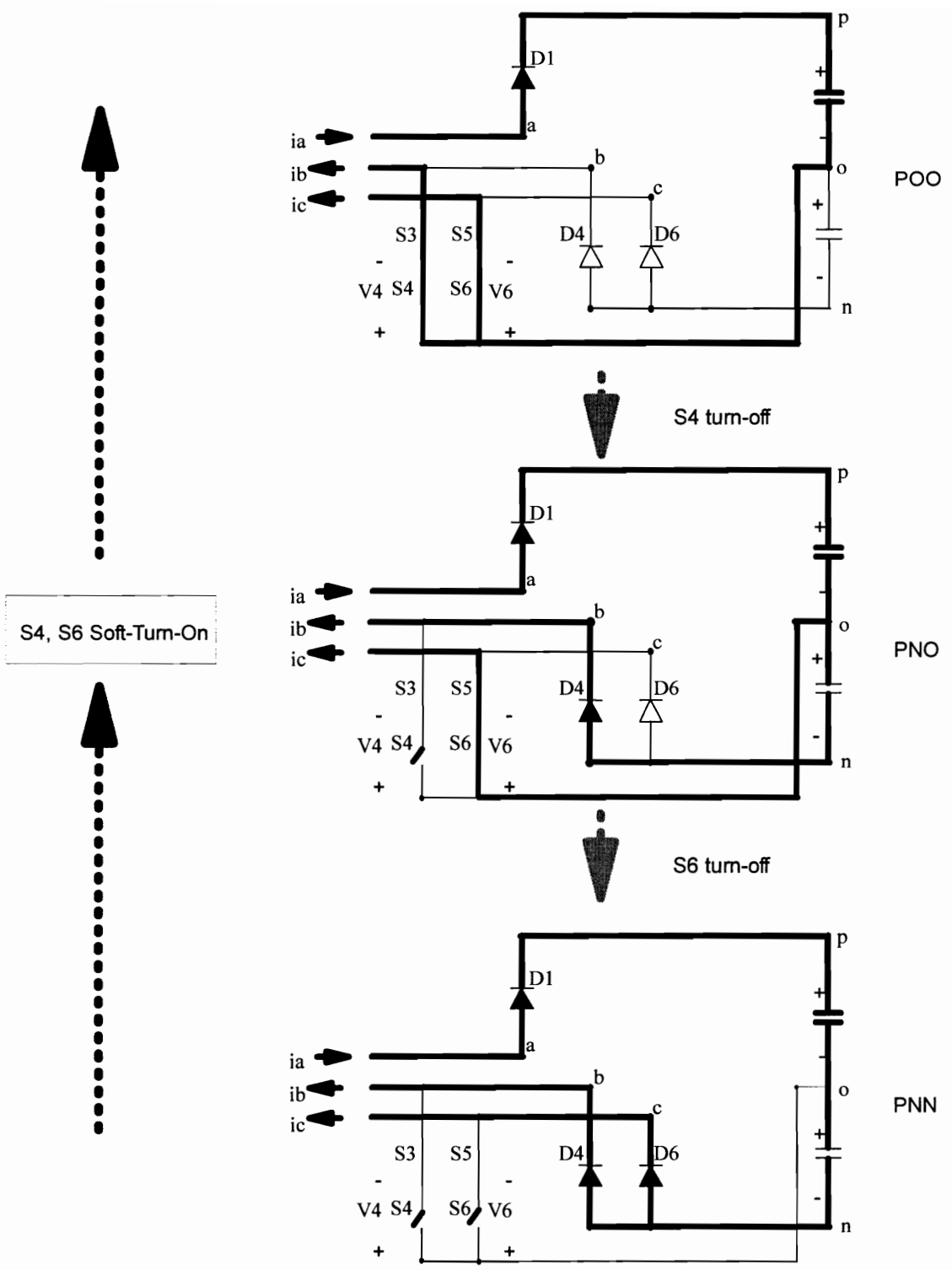
Charging Stage [t0, t1] At t0, Sx2 is turned on with zero current. Then Lx2 will be charged by the bottom half of the dc link voltage. With the increase of the auxiliary current ix2, the currents in D4 and D6 are gradually diverted into the auxiliary circuit.

Resonant Stage [t1, t2] At t1, ix2 reaches the sum of i(b) and i(c), so D4 and D6 are turned off under the zero-current condition. This turn-off is lossless due to the soft-switching condition. Then Lx2 will resonate with the capacitance of node b and node c, which includes the semiconductor junction capacitance and any snubber capacitors. Snubber capacitors, which are not shown in Fig. 6.22 for simplicity, can be placed across diodes D1 through D6, across switches S1 through S6, or between phase nodes a, b, c and the dc link midpoint "o". However, the last option, between a, b, c and the dc-link midpoint, is preferred, since the voltage rating of the capacitors is only half the output voltage, and one capacitor can serve two switches in that phase. During this stage, the voltages across D4 and D6 increase in a resonant fashion, and the voltages across S4 and S6 are reduced gradually.

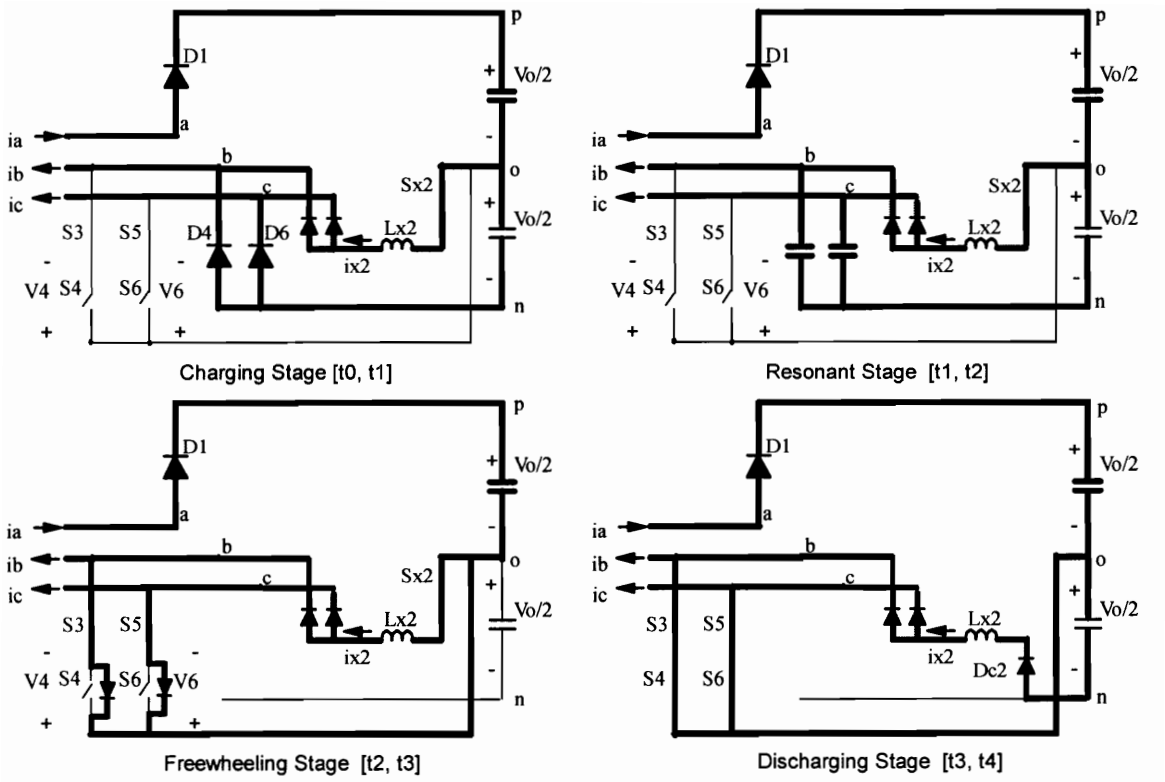
Freewheeling Stage [t2, t3] At t2, the voltages across S4 and S6 are reduced to zero simultaneously, so their anti-parallel diodes are turned on naturally. Then nodes b and c are clamped to the dc link midpoint o, and the currents are freewheeling between b, c, and o through the auxiliary circuit. Zero-voltage turn-on condition for S4 and S6 is created.

Discharging Stage [t3, t4] During the freewheeling stage, the voltages across S4 and S6 are clamped at zero, and S4 and S6 can be turned on with zero voltage at any time, which is depicted as t3. As soon as S4 and S6 are turned on, Sx2 can be turned off, so Lx2 will be discharged by the bottom half of the dc-link voltage. When ix2 is discharged to zero at t4, Dc2 is turned off naturally. After t4, the auxiliary circuit is functionally disconnected from the main power stage, and remains inactive until the next switch turn-on commutation. The converter resumes its PWM operation mode.

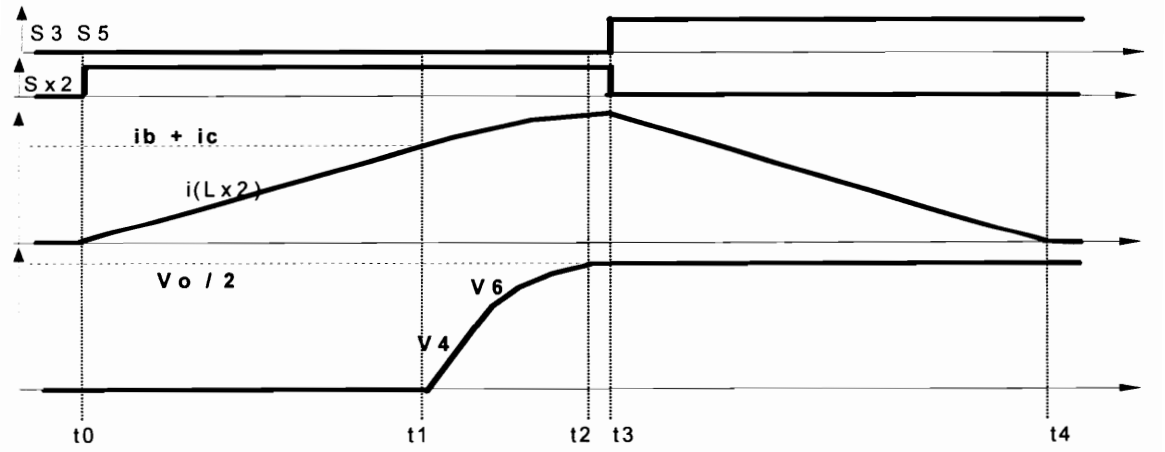
The operating stages of this commutation are shown in Fig. 6.24(b), in which the active current paths are shown as thick lines. The key waveforms in this soft-switching



(a). Converter operation with SWM in Fig. 6.23(d)



(b). Operating stages



(c). Key waveforms in soft-switching commutation

Figure 6.24 **Soft-switching operation of a ZVT three-level boost rectifier.** There is no extra turn-off in the soft-switching commutation. The diode reverse recovery and switch turn-on loss are eliminated with the help of the auxiliary circuit.

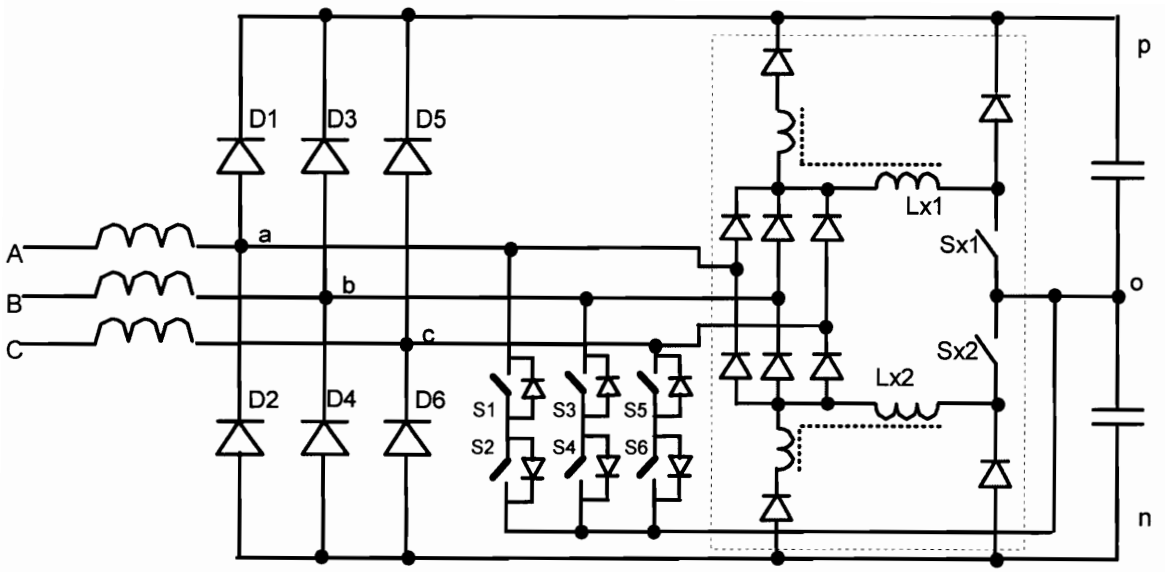
commutation are shown in Fig. 6.24(c). Due to the zero-voltage turn-on of the switches and elimination of diode reverse recovery, the switch turn-on loss is completely eliminated, while the turn-off loss can be reduced with the snubber capacitors. The voltage stress of the auxiliary switches and diodes is half the output voltage. However, the auxiliary switches are turned off with high current, and have to be implemented with MOSFETs. If the turn-off stress of the auxiliary switches is to be reduced, especially when IGBTs are used, the modified ZVT technique with coupled inductors in [A33] can be used to reduce the turn-off current. The modified topologies are shown in Figs. 6.25(a) and (b). With the modified topologies, however, the control timing during the soft-switching transition is critical, and should be adjusted according to phase currents.

For other three-level rectifier topologies, similar soft-switching circuits can be easily developed. Figs. 6.26(a) and (b) shows two examples of ZVT topologies for the rectifiers shown in Figs. 6.21(a) and (b). The ZVT topology for a three-switch version of three-level boost rectifier proposed in [C6] is shown in Fig. 6.26(c). The operation principle of the auxiliary circuits in Fig. 6.26 is similar to above discussions.

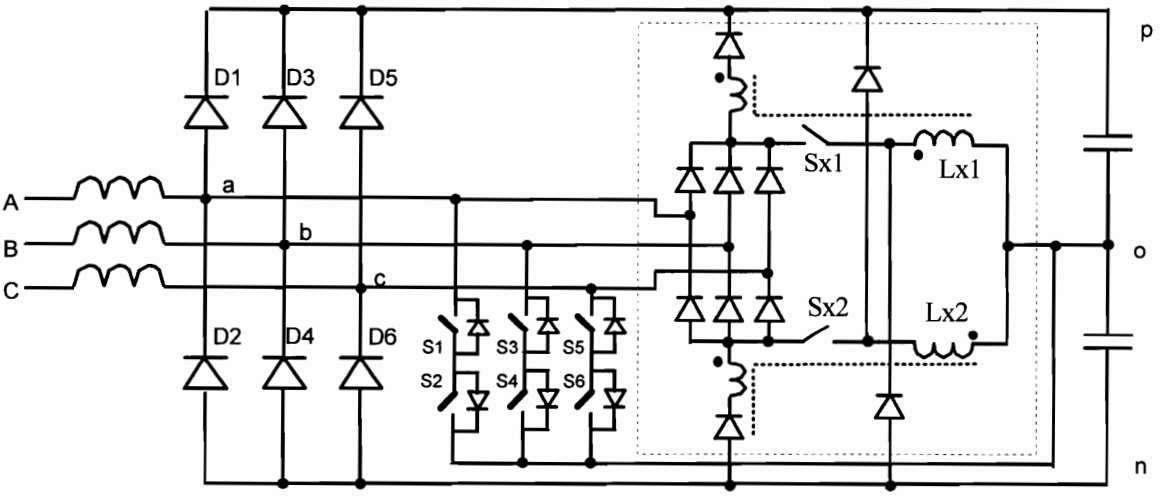
6.4.3 TOPOLOGY EVALUATION

The control and operation of hard-switching three-phase three-level boost rectifiers are analyzed in [C5] [C6] [C11] [C23]. The overall operation of the ZVT rectifiers is very similar to their hard-switching counterpart's, since the auxiliary circuit is actuated only for a short time during the switch turn-on commutation, and the control issues are also very similar. The major functional difference between the proposed ZVT topologies and the hard-switching converters is the soft-switching commutation, which reduces the switching loss and stress of the power semiconductors.

similarly to in previous chapters, switching model simulation with the simple power loss model described in Appendix A is used to evaluate the efficiency performance

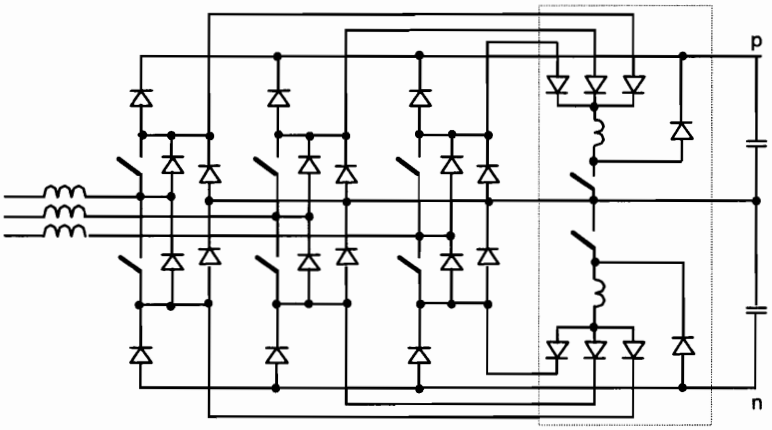


(a). A modified topology developed from Fig. 6.22(b).

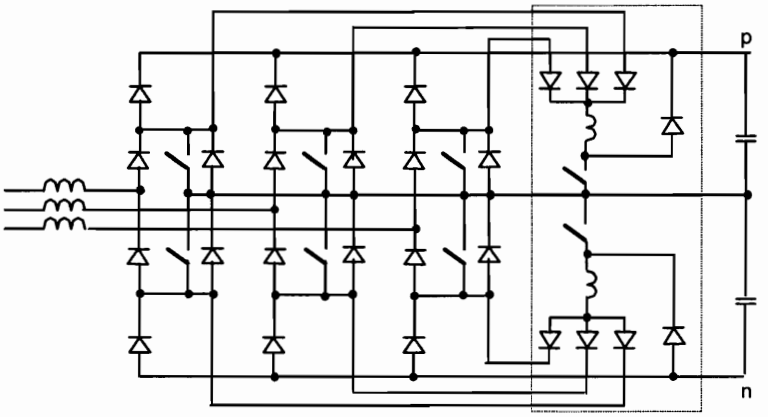


(b). A modified topology developed from Fig. 6.22(c).

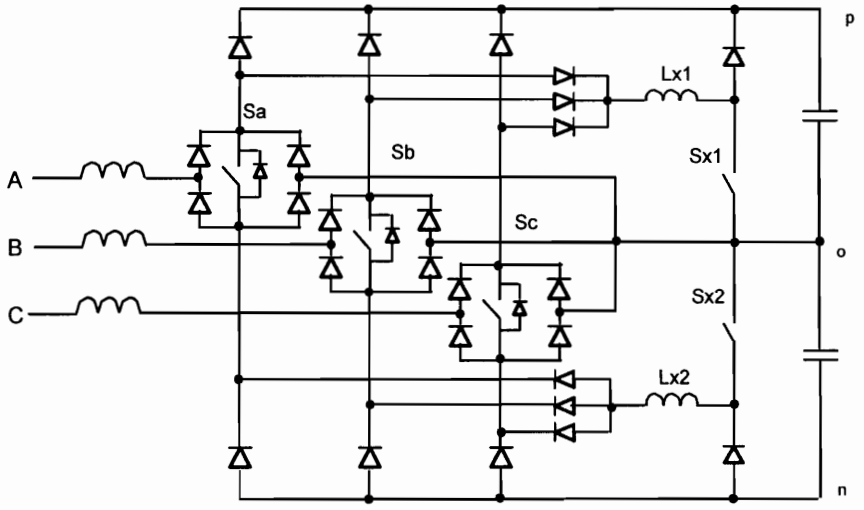
Figure 6.25 ZVT three-level rectifiers with coupled inductors. The auxiliary switch power loss is reduced by the coupled inductors.



(a). ZVT topology for Fig. 6.21(a)



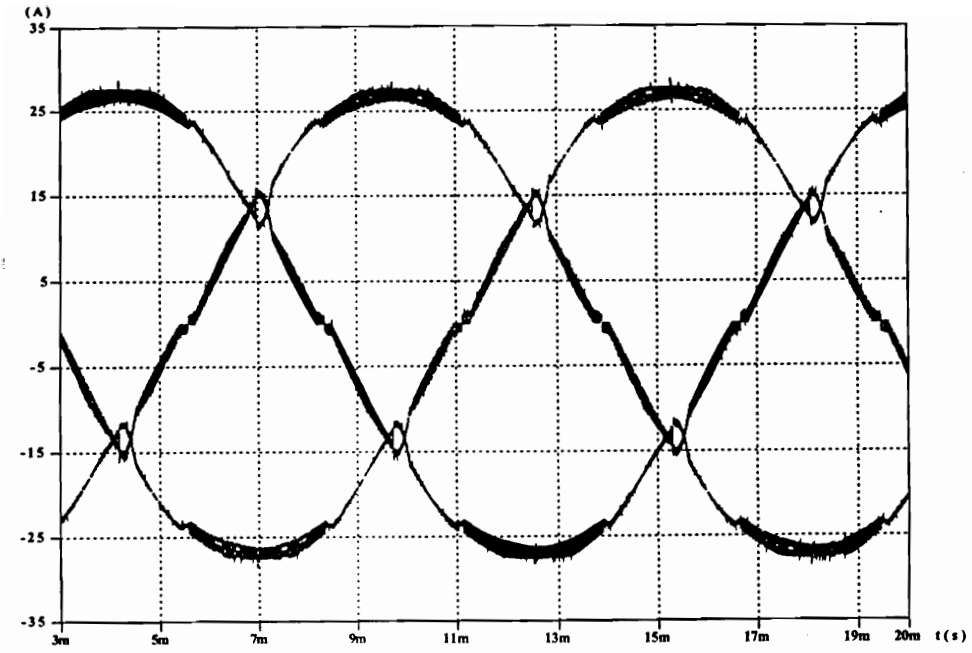
(b). ZVT topology for Fig. 6.21(b)



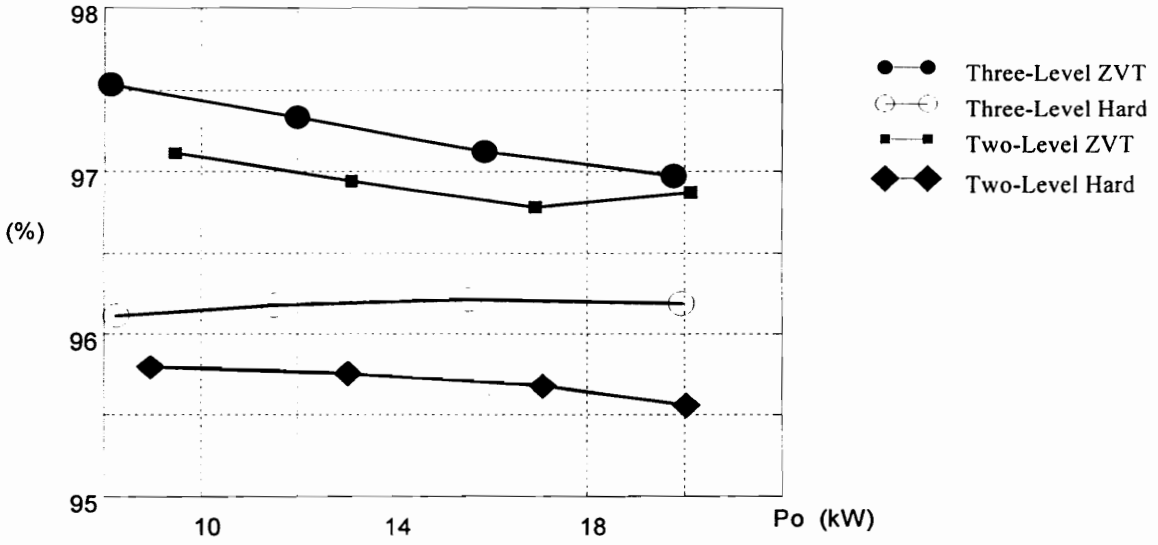
(c). ZVT topology for a three-switch version

Figure 6.26 Other forms of ZVT three-level rectifiers.

of the soft-switching converter. As an example, the three-level ZVT rectifier of Fig. 6.22(b) is simulated with the same parameters as in Fig. 3.16(a) and Table 3.2(a). The dc-link voltage is 900 V, while the input rms phase voltage is 213 V (the low line condition of the 460 V system). Each main switch is a 600 V, 50 A IGBT IXGK50N60AU1, and each auxiliary switch is three MOSFET IXFM20N60 in parallel. The capacitance of each snubber capacitor is 5.6 nF , and each resonant inductor has an inductance of 4 uH. Fig. 6.27(a) shows the simulated input currents, which are largely sinusoidal, and the current ripple is very small. The simulated efficiency data under both hard-switching and soft-switching conditions are shown in Fig 6.27(b). Clearly, the ZVT operation improves the converter efficiency over hard-switching operation by about 1%. To compare the three-level rectifier with the conventional two-level boost rectifier, the ZVT rectifier of Fig. 3.10(c) and its hard-switching counterpart are simulated also with the same operating condition as the three-level rectifier, and the efficiency data are shown also in Fig. 6.27(b). From the simulation results, the efficiency of the three-level rectifier is considerably higher than the two-level rectifier's in both hard-switching and soft-switching operations. Therefore, considering also that the switches in the three-level converter have only half the voltage stress of that in the two-level rectifier, the three-level boost rectifier is a high-performance, low-cost topology for three-phase PFC applications.



(a). Input current waveform



(b). Efficiency comparison

Figure 6.27 **Simulation of three-phase three-level ZVT rectifier.** The three-level rectifier has a higher efficiency than the two-level rectifier in both hard-switching mode and soft-switching mode.

6.5 CONCLUSIONS

This chapter investigates several new multi-level converter topologies: a multi-level two-quadrant boost chopper and its soft-switching techniques, ZVT and ZCT three-level voltage source inverters, and simple ZVT three-level boost rectifiers. Compared to a conventional two-level chopper, a three-level two-quadrant chopper proposed in this chapter reduces the maximum inductor current ripple and switching loss by half with the same power stage parameters, and demonstrates the typical advantages of multi-level converters. Soft-switching techniques for three-level voltage source inverters are developed through the concept of PWM cells, which are identified based on space vector modulation. Through careful examination of space vector modulation schemes, simple zero-voltage transition topologies for three-phase three-level boost rectifiers, which use fewer main switches than voltage source inverters, are also developed. These simplified ZVT auxiliary circuits utilize two auxiliary switches to help six main switches to realize zero-voltage turn-on, and can achieve about 1% efficiency improvement compared with the hard-switching operation. The efficiency of three-level rectifiers is also considerably higher than their two-level counterparts'. Compared to traditional two-level power converters, multi-level converters can achieve significant performance and cost advantages in high-power applications.

7 CONCLUSIONS AND FUTURE WORK

7.1 CONCLUSIONS

Soft-switching techniques alleviate the switching loss and stress problems in a PWM converter, and make the high-frequency operation of high-power converters feasible. The control performance and power density of a soft-switching converter can be improved due to its higher switching frequency and smaller reactive components. The switch's voltage and current rating in a soft-switching converter can also be reduced due to the favorable switching condition, possibly resulting in lower converter cost. To realize the potential performance improvement and cost reduction in practical high power applications, an effective soft-switching scheme should achieve the soft-switching function with minimum modification to the optimum PWM schemes, so the switch voltage/current stress, converter circulating energy, and extra switching action of the main switches can be minimized. The control timing of the auxiliary circuit should also be as simple as possible. This dissertation proposes and verifies several new soft-switching topologies which comply with these principles.

The improved zero-current-transition (ZCT) schemes presented in Chapter 2 achieve zero-current switching at both turn-on and turn-off for all main switches and auxiliary switches, practically eliminating switching losses and diode reverse recovery. These new topologies achieve a switching loss and stress reduction comparable to in a zero-current switching resonant converter, and have similar conduction loss and circulating energy of a PWM converter. Experimental results prove that they can reduce the total switching loss and switch voltage spike to below 20% of the hard-switching values with the proposed soft-switching technique. These ZCT schemes are well suited for very-high-power applications, where the switching loss and stress of power semiconductor devices are a primary concern.

The ZVT topologies for three-phase boost rectifiers/voltage sourcec inverters discussed in Chapter 3 achieve soft-switching function for all main switches using simple auxiliary circuits. With careful arrangement of space vector modulation schemes, the active switch turn-on instants in all three phases are synchronized, so that the auxiliary circuits are actuated only once in a switching cycle. A significant advantage of these topologies over the existing techniques is that the overcharging of resonant inductors is eleminated, so the extra main switch turn-off loss and control complexity are reduced. The operation principles of the ZVT topologies are verified experimentally. These topologies are also evaluated with a 450 V design and a 900 V design in both rectifier mode and inverter mode by computer simulation, in which simple power loss models based on experimental switching loss data are incorporated. Simulation results demonstrate that the proposed ZVT techniques can achieve higher efficiency improvement than all existing soft-switching techniques in rectifier mode. One of the proposed topologies, shown in Fig. 3.19(b), can also match the efficiency improvement of the well-known ARCP in inverter mode, but has a much simpler auxiliary circuit. These techniques could be excellent candidates for high-performance medium-power applications.

Practical ZVT techniques for three-phase buck and buck-boost rectifiers are also developed in Chapter 4. By connecting the auxiliary circuits directly to the main switches, these topologies accomplish zero-voltage turn-on for all main switches with an optimum current space vector modulation scheme. The resonance in the bridge arms, causing by the stray inductance and semiconductor devices' junction (or snubber) capacitance, is also absorbed by the auxiliary circuit, so the voltage stress of the switches are kept minimum. The soft-switching operation is verified by simulation results. Significant efficiency improvement through the soft-switching operation is also demonstrated in the simulation.

New ZVT dc-link schemes are also proposed in this work for three-phase ac-dc-ac power systems by applying the soft-switching mechanism to the common dc link. A dc-link clamp switch and shunt resonant circuit are inserted into a PWM ac-dc-ac converter,

and force the dc-link voltage to zero when soft switching is desired. With a coordinated control of the ac-dc converter and the dc-ac converter, most energy can be delivered from the rectifier to the inverter without passing the auxiliary circuit, and the auxiliary circuit deals with only the difference between the rectifier current and the inverter current. The power loss of the auxiliary circuit in the proposed topologies is significantly lower than in most existing dc-link commutation schemes, resulting in simpler and lower cost implementation of the soft-switching circuit. According to the simulation results in Chapter 5, the efficiency improvement of the proposed topologies over their hard-switching counterparts is usually in the range of 1 ~ 3% at a 50 kHz switching frequency, which means about 30% power loss reduction compared to hard switching, and an easier thermal management and possible cost reduction.

Novel three-level power conversion techniques are investigated in Chapter 6. A three-level two-quadrant boost chopper is first proposed to interface a current source with a voltage source for applications such as motor drives, magnetic power supplies and superconductive magnetic energy storage (SMES). This converter demonstrates the typical advantages of multi-level converters, i.e. even voltage sharing, low switching loss and low inductor current ripple. Soft-switching techniques for multi-level PWM converters are also studied. Through the concept of soft-switching PWM cells, ZCT and ZVT topologies for multi-level two-quadrant choppers and three-phase inverters are developed. Especially, simple ZVT topologies can be derived for three-phase three-level rectifiers based on synchronized turn-on of the main switches, with a similar concept in the two-level boost rectifiers. Simulation results prove that the three-level rectifiers have a higher efficiency than its two-level counterpart in both soft-switching and hard-switching operations, making them very attractive for high power PFC applications.

7.2 SUGGESTIONS FOR FUTURE WORK

It can be expected that soft-switching converters will be an increasingly viable alternative to the conventional hard-switching power conversion in many high performance applications. The techniques investigated in this dissertation have significant improvements over existing soft-switching techniques, and can be used in a wide range of applications. However, soft-switching techniques in high-power converters are still at the early development stage. To realize the full potential of soft switching for different applications, there are still more evaluation and practical design work needed. The efficiency improvement, i.e. the power loss reduction, of a soft-switching converter is an important advantage, which is relatively easy to evaluate, and has been demonstrated in this dissertation and in many papers by different authors. However, the soft-switching operation also creates favorable switching trajectories for power switches, thus improving the reliability, voltage-current stress, and EMI emissions of the power converter. These factors could have a significant impact on the performance, cost, and design practice of power conversion equipment, and need to be assessed in more detail in the future.

Of the techniques proposed in this dissertation, several topologies deserve further research, including:

- Testing the improved ZCT schemes at higher power levels to evaluate their ability to reduce the switching loss and stress of GTO-type devices at very high power application;
- Testing the soft-switching inverter topologies shown in Figs. 3.25(a) and (b) in a practical circuit, to evaluate the effect of coupled saturable inductors on the soft-switching operation;
- Many ZVT topologies of three-phase boost rectifiers, buck rectifiers, and three-level rectifiers have been proposed for PFC application, and their relative merits and limitations for typical applications need to be assessed;
- The dc-link schemes in Chapter 5 could be a cost-effective solution for many three-phase applications, and need to be evaluated experimentally.

References

1. Power Device Characteristics and Soft-Switching Techniques in DC-DC Converters

[A1] A. Petterteig and T. Rogne, "IGBT turn-off losses - in hard switching and with a capacitive snubber," *Proc. EPE'91*, pp.0-203 - 0-214.

[A2] A. Porst, "Ultimate limits of an IGBT (MCT) for high voltage applications in conjunction with a diode," *Proc. of the 6th Internat. Symposium on Power Semiconductor Devices & ICs*, 1994, pp. 163 - 170.

[A3] Powerex H-Series IGBT Databook, 1994.

[A4] Fuji N-Series IGBT Data Book, 1995.

[A6] IR IGBT Designer's Manual, 1994.

[A7] Harris MCT/IGBTs/Diodes Databook, 1995.

[A8] T. Undeland, F. Jenset, A. Steinbakk, T. Rogne, and M. Hernes, "A snubber configuration for both power transistors and GTO PWM inverters," *Proc. PESC'84*, pp. 42 - 53.

[A9] F. Blaabjerg, "Snubbers in PWM VSI inverter," *Proc. PESC'91*, pp.104 - 122.

[A10] P. H. Swanepoel and J. D. van Wyk, "Analysis and optimization of regenerative linear snubbers applied to switches with voltage and current tails," *IEEE Trans. Power Electronics*, pp. 433 - 441, No.4, 1994.

[A11] P. H. Swanepoel and J. D. van Wyk, "Design and optimization of voltage clamps for voltage source inverters," *Proc. PESC'92*, pp. 155 - 161.

[A12] S. Saito, T. Matsumoto, N. Tada, and H. Matsumura, "Evaluation of large-capacity GTOs' snubber circuits from aspects of circuitry and structure," *Proc. IPEC'95,* pp.1145 - 1150.

[A13] V. A. K. Temple, "Power semiconductors: faster, smarter and more efficient," *Proc. IPEC'95*, pp. 6 - 12.

[A14] X. Zhou, et. al., "A comparative study of switching losses of MCTs and IGBTs," *Proc. VPEC Seminar'95*, pp. 187 - 193.

[A15] F. Bauer etc. , "On the suitability of BiMOS high power devices in intelligent, snubberless power conditioning circuits," *Proc. of the 6th Internat. Symposium on Power Semiconductor Devices & ICs*, 1994, pp. 201 - 206.

[A16] S. Lefebvre, F. Forest, F. Calmon, and J. P. Chante, "Turn-off analysis of the IGBT used in ZCS mode," *Proc. of the 6th Internat. Symposium on Power Semiconductor Devices & ICs*, 1994, pp. 99 - 104.

[A17] K. Wang, F. C. Lee, G. Hua, and D. Borojevic, "A comparative experimental study of switching losses of IGBTs under hard-switching, zero-voltage-switching and zero-current-switching," *Proc. PESC'94*, pp. 1196 - 1204.

[A18] I. Widjaja, A. Kurnia, D. Divan, and K. Shenai, "Computer simulation and design optimization of IGBTs in soft-switching converters," *Proc. of the 6th Internat. Symposium on Power Semiconductor Devices & Ics*, 1994, pp. 105 - 109.

[A19] H. Dettmer, etc., "A comparison of the switching behavior of IGBT and MCT power devices," *Proc. of the 5th Internat. Symposium on Power Semiconductor Devices & ICs*, 1993, pp. 54 - 59.

[A20] A. Kurnia, H. Cherradi, and D. M. Divan, "Impact of IGBT behavior on design optimization of soft switching inverter topologies," *IEEE Trans. IA*, vol. 31, pp. 280 - 286, 1995.

[A21] M. Dehmlow, K. Heumann, and R. Sommer, "Comparison of semiconductor device losses in hard switched and zero voltage switched inverter systems," *Proc. EPE'93*, pp. 419 - 424.

[A22] A. Consoli, C. Licitra, S. Musumeci, and A. Testa, "Comparative investigation on power losses in soft-switching insulated gate devices," *Proc. of the 6th Internat. Symposium on Power Semiconductor Devices & ICs*, 1994, pp. 87 - 92.

[A23] A. Mertens, H. Skudelny, P. Caldeira, and T. Lipo, "Characterization of GTOs under different modes of zero current switching," *Proc. PESC'91*, pp.444 - 452.

[A24] R. W. De Doncker, O. Demirci, S. Arthur, and V. Temple, "Characteristics of GTOs and high-voltage MCTs in high-power soft-switching converters," *IEEE Trans. IA*, vol. 30, pp. 1548 - 1556, 1994.

[A25] G. L. Skibinski and D. M. Divan, "GTO characterization for zero voltage switching applications," *Proc. PESC'91*, pp. 437 - 443.

[A27] R. Oruganti and F. C. Lee, "Resonant power processors: Part I - state plane analysis," *IEEE Trans IA-21*, pp. 1453 - 1460, 1985.

[A28] K. Liu and F. C. Lee, "Resonant switches - a unified approach to improve performance of switching converters," *Proc. INTELEC'84*, pp. 334 - 341.

[A29] K. Liu, R. Oruganti, and F. C. Lee, "Resonant switches - topologies and characteristics," *IEEE Trans. Power Electron.*, vol. 2, pp. 62 - 74, 1987.

[A30] W. A. Tabiz and F. C. Lee, "Zero-voltage switching multi-resonant technique - a novel approach to improved performance of high frequency quasi-resonant converter," *Proc. PESC'88*, pp. 9 - 17.

[A31] G. Hua and F. C. Lee, "A new class of ZVS-PWM converters," *Proc. HFPC'91*, pp.244 - 251.

[A32] G. Hua, C.S. Leu, and F. C. Lee, "Novel zero-voltage transition PWM converters", *Proc. PESC'92*, pp.55-61

[A33] J. P. Gegner and C. Q. Lee, "Zero-voltage-transition converters using an inductor feedback technique," *Proc. PESC'94*, pp. 862-868.

[A34] J. P. Gegner and C. Q. Lee, "Zero-voltage-transition converters using a simple magnetic feedback technique," *Proc. APEC'94*, pp. 590-596.

[A35] G. Hua, X. Yang, Y. Jiang, and F. C. Lee, "Novel zero-current transition PWM converters," *Proc. PESC'93*, pp. 538 - 544

[A36] G. Hua and F. C. Lee, "Evaluation of switched-mode power conversion technologies," *First International Power Electronics and Motion Control Conf.*, 1994

[A37] G. Hua and F. C. Lee, "An overview of soft-switching techniques for PWM converters," *Proc. EPE'93*, pp. 12 - 26.

[A38] G. K. Dubey, "Classification of commutation methods," *Proc. IAS'81*, pp. 895 - 909

[A39] W. McMurray, "Thyristor commutation in dc choppers - a comparative study," *IEEE Trans. IA-14*, pp. 547-558, No. 6, 1978.

[A40] D. C. Martins, F. J. M. de Seixas, J. A. Brilhante, and I. Barbi, "A family of dc-dc PWM converters using a new ZVS commutation cell," *Proc. PESC'93*, pp. 524 - 530.

[A41] R. Streit and D. Tollik, "High efficiency telecom rectifier using a novel soft-switched boost-based input current shaper," *Proc. INTELEC'91*, pp. 720 - 726.

[A42] H. Mao, F. C. Lee, X. Zhou, and D. Boroyevich, "Improved zero-current-transition PWM converters for high power applications," *Proc. IAS'96, pp. 1145 - 1152.*

2. Soft-Switching Techniques in Three-Phase Voltage Source Converters

[B1] A. R. Prasad, P. D. Ziogas, and S. Manias, "An active power factor correction technique for three-phase diode rectifiers," *Proc. PESC'89*, pp. 58 - 66.

[B2] R. Y. Igarashi and, I. Takahashi, "Unity power factor three-phase rectifier using a single switching device," *Proc. IAS'94*, pp. 769-774.

[B3] J. W. Kolar, H. Ertl, and F. C. Zach, "Space vector-based analytical analysis of the input current distortion of a three-phase discontinuous-mode boost rectifier system," *Proc. PESC'93*, pp. 696-703.

[B4] Q. Huang and F. C. Lee, "Harmonic reduction in a single-switch, three-phase boost rectifier with high order harmonic injected PWM," *Proc. PESC'96*, pp. 1266-1271.

[B5] E. H. Ismail and R. W. Erickson, "A single transistor three-phase resonant switch for high quality rectification," *Proc. PESC'92*, pp. 1341-1351.

[B6] S. Gataric, D. Borojevic, and F. C. Lee, "Soft-switched three-phase rectifier with power factor correction," *Proc. APEC'94*, pp. 738-744.

[B7] G. Spiazzi and F. C. Lee, "Implementation of single-phase boost power factor correction circuits in three-phase applications," *Proc. IECON'94*, pp.

[B8] Y. Jiang, H. Mao, F. C. Lee, and D. Borojevic, "Simple high performance three-phase boost rectifiers," *Proc. PESC'94*, pp. 1158-1163.

[B9] D. M. Divan, "The resonant dc-link converter - a new concept in power conversion," *Proc. IECON'86*, pp. 648-656.

[B10] D. M. Divan and G. Skibinski, "Zero switching loss inverters for high power applications," *Proc. IAS'87*, pp. 627-634

[B11] S. Salama and Y. Tadros, "Quasi resonant 3-phase IGBT inverter," *Proc. PESC'95*, pp. 28 - 33

[B12] J. S. Lai and B. K. Bose, " A high frequency quasi-resonant dc voltage inverter for ac motor drive," *Proc. IAS'90*, pp. 1202-1207.

[B13] J. He and N. Mohan, "Parallel resonant dc-link circuit - a novel zero switching loss topology with minimum voltage stresses," *Proc. PESC'89*,pp. 1006-1012.

[B14] J. G. Cho, H. S. Kim, and G. H. Cho, "Novel soft-switching PWM converter using a parallel resonant dc-link," *Proc. PESC'91*, pp. 241-247.

[B15] L. Malesani, P. Tenti, P. Tomasin, and V. Toigo, "High efficiency quasi resonant dc-link converter for full-range PWM," *Proc. APEC'92*, pp. 472-478.

[B16] Y. Jiang and F. C. Lee, "Novel soft-switched three-phase boost rectifiers and voltage source inverters," *Invention Disclosure*, VTIP 93 - 081, Virginia Polytechnic Institute and State University, 1993.

[B17] K. Wang et. al., "Novel dc-rail soft-switched three-phase voltage-source inverters", *Proc. IAS'95,* pp. 2610 - 2617.

[B18] J. W. Choi and S. K. Sul, "Resonant bidirectional power converter: Part I - resonant circuit," *IEEE Trans. Power Electron.* vol. 10, pp. 479 - 484, 1995

[B19] Y. C. Jung, Hyo L. Liu, G. C. Cho, and G. H. Cho, "Soft-switching space vector PWM inverter using a new quasi-parallel resonant dc link," *Proc. PESC'95*, pp. 936 - 942

[B20] R. W. De Doncker and J. P. Lyons, "The auxiliary quasi-resonant dc link inverter," *Proc. PESC'91*, pp. 248 - 253

[B21] K. Yurugi, H. Yonemori, K. Hayasi, and M. Nakaoka, "Next generation space voltage vector ZVT-PWM ac-dc active power converter with auxiliary transformer-assisted resonant dc link," *Proc. PESC'94*, pp. 644 - 650

[B22] H. Yonemori, K. Hayasi, and M. Nakaoka, "A novel space-voltage vector modulated sinewave three-phase inverter with high frequency transformer-coupled resonant dc link," *Proc. PESC'94*, pp. 651 - 658

[B23] S. Chen and T. A. Lipo, "A passively clamped quasi resonant dc link inverter," *Proc. IAS'94*, pp. 841 - 848

[B24] J. A. Ferreira, A. van Ross, and J. D. van Wyk, "A generic soft switching converter topology with a parallel nonlinear network for high power application," *Proc. PESC'90*, pp. 298 - 304

[B25] A. Cheriti, et. al., "A rugged soft commutated PWM inverter for ac drives," *IEEE Trans. Power Electron.* vol 7, pp. 385 - 392, 1992

[B26] W. McMurray, "Resonant snubbers with auxiliary switches," *IEEE Trans IA-29*, pp. 355 - 362, 1993

[B27] R. W. De Doncker and J. P. Lyons, "The auxiliary commutated resonant pole converters", *Proc. IAS'90*, pp.1228-1235.

[B28] S. Frame, et al., "Three-phase soft-switching inverters for electric vehicle application," *VPEC Seminar'95*, pp.45-52

[B29] V. Vlatkovic, D. Borojevic, F. C. Lee, C. Cuadros, and S. Gataric, "A new zero-voltage-transition, three-phase PWM rectifier/inverter circuit," *PESC'93*, pp. 868-873.

[B30] J. S. Lai, et. al., "A novel resonant snubber based inverter," *Proc. APEC'95*, pp. 797 - 803.

[B31] J. S. Lai, et. al., "Delta configured auxiliary resonant snubber inverter," *Proc. IAS'95*, pp. 2618 - 2624.

[B32] P. Tomasin, "A novel topology of zero-current switching voltage-source PWM inverter for high power applications," *Proc. PESC'95*, pp. 1245-1251.

[B33] H. Matsuo, K. Iida, and K. Harada, "210 kVA soft switching PWM type ac auxiliary power supply system of the electric railway rolling stock using an improved ARCP three phase inverter with SI thyristor switches," *Proc. IPEC'95*, pp. 831 - 836.

[B34] S. J. Finney T. C. Green, and B. W. Williams, "Review of resonant link topologies for inverters," *Proc. of IEE*, Part B, vol. 140, pp. 103 - 114, 1993.

[B35] G. Venkataramanan, D. M. Divan, and T. M. Jahns, "Discrete pulse modulation strategies for high frequency inverter systems," *IEEE Trans. Power Electron.*, vol. 8, pp. 279 - 287, 1993.

[B36] D. M. Divan, G. Venkataramanan, and R. DeDoncker, "Design methodologies for soft switched inverters," *IEEE Trans. IA-29*, pp. 126 - 135, 1993.

[B37] S. J. Finney, T. C. Green, and B. W. Williams, "Spectral characteristics of resonant-link inverters," *IEEE Trans. Power Electron.*, vol. 8, pp. 562 - 570, 1993.

[B38] A. Mertens, "Performance analysis of three-phase inverters controlled by synchronous delta-modulation systems," *IEEE Trans. IA-30*, pp. 1016 - 1027, 1994.

[B39] G. Venkataramanan and D. M. Divan, "pulse width modulation with resonant dc link converters," *IEEE Trans. IA-29*, pp.113-120.

[B40] D. M. Divan, L. Malesani, P. Tenti, and V. Toigo, "A synchronized resonant dc link converter for soft-switched PWM inverters," *IEEE Trans. IA-29*, pp. 940 - 948, 1993.

[B41] L. Malesani, P. Tomasin, and V. Toigo, "Space vector control and current harmonics in quasi-resonant soft-switching PWM conversion," *Proc. IAS'94*, pp. 1122 - 1129.

[B42] C. Cuadros, et. al, "Space vector modulated, zero-voltage transition three-phase to dc bidirectional converter", *Proc. PESC'94*, pp. 16-24.

[B43] D. M. Divan and G. Venkataramanan, "Comparative evaluation of soft switching inverter topologies," *Proc. EPE'91*, pp. 2-013 - 2-017.

[B44] V. Vlatkovic, D. Borojevic, and F. C. Lee, "Soft-transition three-phase PWM conversion technology," *Proc. PESC'94*, pp. 79 - 84.

[B45] J. S. Kim and S. K. Sul, "Resonant link bidirectional power converter: Part II," *IEEE Trans. Power Electron.*, vol. 10, pp. 485 - 493, 1995.

[B46] V. G. Agelidis, P. D. Ziogas, and G. Joos, "Optimum use of dc side commutation in PWM inverters," *Proc. PESC'91*, pp.276 - 282.

[B47] V. G. Agelidis, P. D. Ziogas, and G. Joos, "An optimum modulation strategy for a novel notch commutated 3 Φ PWM inverters," *Proc. IAS'91*, pp.809 - 818.

[B48] S. Kondo, S. H. Yang, S. Takizawa, and H. Harashima, "Resonant dc link dual converter system for motor drives," *Proc. IAS'91*, pp. 789 - 794.

[B49] A. Julian, D. Vivan, and T. Lipo, "Double bridge resonant dc-link converter with variable input and output frequency," *Proc. APEC'96*, pp. 181 - 186.

[B50] T. A. Lipo, "Resonant link power converters - a new direction in power conversion," *Proc. of 2nd Int. Conf. on Electrical Drives*, 1988.

[B51] Q. Li, X, Zhou, and F. C. Lee, "A novel ZVT three-phase rectifier/inverter with reduced auxiliary switch stresses and losses," *Proc. PESC'96*, pp. 153 - 158.

[B52] J.S. Lai, R. W. Young, and J. W. McKeever, "Efficiency consideration of dc link soft-switching inverters for motor drive applications," *Proc. PESC'94*, pp. 1003 - 1009.

[B53] J. S. Lai, R. W. Young, G. W. Ott, and J. W. McKeever, "Efficiency modeling and evaluation of a resonant snubber based soft-switching inverter for motor drive applications," *Proc. PESC'95*, pp. 943 - 949.

[B54] H. Mao, F. C. Lee, X. Zhou and H. Dai, "Soft-switched three-phase PWM converters with reduced auxiliary switch stress," *Proc. PESC'96, pp.443 - 448.*

[B55] H. Mao, F. C. Lee, D. Boroyevich, and S. Hiti, "High performance three-phase power factor correction circuits," *Proc. IECON'95,* pp. 8 - 14.

[B56] H. Mao and F. C. Lee, "An improved zero-voltage-transition three-phase rectifier/inverter," *Proc. IPEC'95,* pp.853 - 858.

[B57] H. Mao and F. C. Lee, "Improved zero-voltage-transition 3-phase voltage link converters," *VPEC Seminar'94,* pp.53 - 62.

3. Three-level Power Converters

[C1] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point clamped PWM inverter," *IEEE Trans. on Ind. Appl.* , Vol. IA-17, No. 5, 1981

[C2] P. M. Bhagwat and V. R. Stefanovic, "Generalized structure of a multi-level PWM inverter," *IEEE Trans. Ind. Appl.*, No. 6, Nov/Dec 1983, pp. 1057 - 1069

[C3] M. Carpita and S. Tenconi, "A novel multilevel structure for voltage source inverter," *4th European Conf. On Power Electronics and Applications*, 1991, pp. 1_090 - 1_094

[C4] C. Hochgraf, R. Lasseter, D. Divan, and T. A. Lipo, "Comparison of multi-level inverters for static var compensation," *Proc. IAS'94*, pp. 921 - 928

[C5] Y. Zhao, Y. Li, and T. A. Lipo, "Force commutated three-level boost type rectifier," *Proc. IAS'93*, pp. 771-777.

[C6] J. W. Kolar and F. C. Zach, "A novel three-phase three-switch three-level PWM rectifier," *Proc. of 28th Power Conversion Conf.,* Nurnberg, Germany, 1994, pp. 125-138.

[C7] M. Velaerts, "New developments of 3-Level PWM strategies," *3rd European Conf. On Power Electronics and Applications*, 1989, pp. 411-416

[C8] S. Fukuda and A. Sagawa, "Modeling and control of a neutral-point-clamped voltage source converter," *Proc. IPEC'95*, pp. 470 - 475.

[C9] I. Miyashita, B. Kaku, and S. Sone, "A new PWM method for 3-level inverter based on voltage space vector suppressing the neutral point potential variation," *Proc. IPEC'95*, pp. 506 - 510.

[C10] S. Ogasawara and H. Akagi, "Analysis of variation of neutral point potential in neutral clamped voltage source PWM inverters," *Proc. IAS'93*, pp. 965 - 970.

[C11] J. W. Kolar, U. Drofenik, and F. C. Zack, "space vector based analysis of the variation and control of the neutral point potential of hysteresis current controlled three-phase/switch/level PWM rectifier systems," *Proc. PEDS'95*, pp. 22 - 33.

[C12] F. Z. Peng, J. S. Lai, J. McKeever, and J. VanCoevering, "A multilevel voltage source converter system with balanced dc voltages," *Proc. PESC'95*, pp. 1144 - 1150.

[C13] B. Kaku, I. Miyashita, and S. Sone, "Switching loss reduced PWM strategy for 3-level inverter," *Proc. IPEC'95*, pp.512 - 517.

[C14] M. Fracchia, T. Ghiara, M. Marchesoni, and M. Mazzucchelli, "Optimized modulation techniques for the generalized N-level converter," *Proc. PESC'92*, pp. 1205 - 1213.

[C14] H. L. Liu, G. H. Cho, and S. S. Park, "Optimal PWM design for high power three-level inverter through comparative studies," *IEEE Trans. Power Electron.*, vol. 10, pp. 38-47, 1995.

[C16] F. Hamma, T. A. Meynard, F. Tourkhani, and P. Viarouge, "Characteristics and design of multilevel choppers," *Proc. PESC'95*, pp. 1208 - 1214.

[C17] Y. Jiang and F. C. Lee, "Three-level boost converter and its application in single-phase power correction," *VPEC Seminar'94*, pp. 127 - 133.

[C18] J. R. Pinheiro and I. Barbi, "The three-level ZVS-PWM dc-dc converter," *IEEE Trans. Power Electron.*, vol. 8, pp. 486 - 492, 1993.

[C19] J. R. Pinheiro and I. Barbi, "Three-level zero-voltage-switching PWM dc-dc converters - a comparison," *Proc. PESC'95*, pp. 914 - 919.

[C20] W. Yi and G. H. Cho, "Novel snubberless three-level GTO inverter with dual quasi-resonant dc-link," *Proc. PESC'93*, pp. 880 - 883.

[C21] J. G. Cho, J. W. Baek, D. W. Yoo, and C. Y. Won, "Three-level auxiliary resonant commutated pole inverter for high power applications," *Proc. PESC'96*, pp. 1019 - 1026.

[C21] H. Mao, D. Boroyevich, and F. C. Lee, "Novel multi-level 2-quadrant boost choppers for superconducting magnetic energy storage," *Proc. APEC*'96, pp. 876 - 882.

4. Soft-Switching Topologies in Three-Phase Current Source Converters

[D1] Y. Murai and T. A. Lipo, "High frequency series resonant dc link power conversion," *Proc. IAS'88*, pp. 772 - 779.

[D2] Y. Murai, H. Ishikawa, and T. A. Lipo, "New series resonant dc link inverter for electric vehicle drives," *Proc. IAS'94*, pp. 443 - 447.

[D3] S. G. Abeyratne, T. A. Lipo. Y. Murai, and J. Horikawa, "Current clamped, modified series resonant dc-link power converter for a general purpose induction motor drive," *Proc. APEC'94*, pp. 267 - 274.

[D4] S. G. Abeyratne, et. al., "Current clamped, PWM quasi-resonant dc link series resonant converter," *Proc. IAS'94*, pp. 820 - 826.

[D5] G. Ledwich, E. DaSilva and T. Lipo, "Soft switched notching current source converters," *Proc. PESC'92*, pp. 1093 - 1097.

[D6] G. Ledwich and F. Shi, "Neutral commutated soft switched current source converter," *Proc. PESC'94*, pp. 714 - 718.

[D7] G. Moschopoulos and G. Joos, "A novel soft-switched PWM current source rectifier/inverter," *Proc. PESC'94*, pp. 978 - 984.

[D8] F. Leonardi, et. al., "Soft-switched PWM converter with inductive dc filter," *IEEE Trans. IA-31*, pp. 293 - 298, 1995.

[D9] S. Buso, et. al., "Soft-switched current-fed PWM inverter with space vector modulation," *Proc. IAS'94*, pp. 882 - 888.

[D10] J. A. Pomilio, L. Rossetto, P. Tenti, and P. Tomasin, "Performance improvement of soft-switched PWM rectifiers with inductive load," *Proc. PESC'94*, pp. 1425 - 1430.

[D11] D. Borojevic, V. Vlatkovic, and F. C. Lee, "A zero-voltage-switched, three-phase PWM switching rectifier with power factor correction," *Proc. HFPC'91*, pp. 252-264.

[D12] V. Vlatkovic, D. Borojevic, and F. C. Lee, "A zero-voltage-switched, three-phase isolated PWM buch rectifier," *IEEE Trans. Power Electron.*, vol. 10, no. 2, pp. 148-157.

[D13] V. Vlatkovic, "Three-phase power conversion using soft-switching PWM techniques," Ph. D. Dissertation, Blacksburg, VA, Oct. 1994.

5 Modeling and Control of Three-Phase Converters

[E1] J. Holtz, "Pulsewidth modulation - a survey," *IEEE Trans. Ind. Electr.*, vol. 39, no. 5, 1992, pp. 410-420.

[E2] A. Busse and J. Holtz, "A digital space vector modulator for the control of a three-phase converters," *Proc. PESC'82*, pp. 189-195.

[E3] A. M. Trzynadlowski and S. Legowski, "Minimum-loss vector PWM strategy for three-phase inverters," *IEEE Trans. Power Electron.*, vol. 9, no. 1, pp. 26-34, 1995.

[E4] H. W. van der Broeck, H. C. Skudelny, and G. K. Stanke, "Analysis and realization of a pulse width modulator based on voltage space vectors," *IEEE Trans. IA-24*, pp. 142 - 150, 1988.

[E5] Y. Minamoto and T. Ohnishi, "Instantaneous current vector controlled three-phase PWM converter," *Proc. ISPE'92*, pp. 111 - 116.

[E6] A. M. Trzynadlowski, F. Blaabjerg, J. K. Pedersen, R. L. Kirlin, and S. Legowski, ", "Random pulse width modulation techniques for converter-fed drive systems - a review," *IEEE Trans. IA-30*, pp. 1166 - 1175, 1994.

[E7] P. G. Handley and J. T. Boys, "Space vector modulation: an engineering review," *Proc. 4th Intl. Conf. on Power Electronics & Variable Speed Drive*, pp. 87 - 91, London, 1990.

[E8] J. T. Boys and P. G. Handley, "Harmonic analysis of space vector modulated PWM waveforms," *IEE Proc.*, vol. 137, Part B, pp. 197 - 204, 1990.

[E9] J. W. Kolar, H. Ertl, and F. C. Zach, "Influence of the modulation method on the conduction and switching sosses of a PWM converter system," *IEEE Trans. IA-27*, pp. 1063 - 1075.

[E10] R. D. Middlebrook and S. Cuk, "A general unified approach to modeling switching converter power stages," *Proc. PESC'76*, pp. 18 - 34.

[E11] V. Vorperian, "Simplified analysis of PWM converters using the model of the PWM switch Part I and Part II," *IEEE Trans. Aerospace and Electronic Systems*, vol. 26, no. 3, pp. 490-505, 1990.

[E12] W. Polivka, P. Chetty, and R. Middlebrook, "State-space average modeling of converters with parasitic and storage-time modulation," *Proc. PESC'80*, pp.

[E13] G. Hua, "Soft-switching techniques for pulse-width-modulated converters," *Ph. D. Dissertation*, VPI&SU, Blacksburg, 1994.

[E14] V. Vlatkovic, et. al., "Small-signal analysis of the zero-voltage switched full-bridge PWM converter," *Proc. HFPC'90*, pp. 262-272.

[E15] C. T. Rim, D. Y. Hu, and G. H. Cho, "Transformers as equivalent circuits for switches: general proofs and d-q transformation-based analyses," *IEEE Trans. Ind. Appl.*, vol 26, no. 4, 1990, pp. 777-785.

[E16] S. Hiti, D. Borojevic, and C. Cuadros, "Small-signal modeling and control of three-phase PWM converters," *Proc. IAS'94*, pp.1143-1150.

[E17] S. B. Han, N. S. Choi, C. T. Rim, and G. H. Cho, "Modeling and analysis of buck type three-phase PWM rectifier by circuit dq transformation," *Proc. PESC'95*, pp. 431 - 436.

[E18] R. Ampatipudi, D. Boroyevich, S. Hiti, and F. C. Lee, "Average and small-signal modeling of zero-voltage transition three-phase PWM boost rectifier," *Proc. APEC'94*, pp. 870-874.

[E19] D. M. Brod and D. W. Novotny, " Current control of VSI-PWM inverters," *IEEE Trans. Ind. APPl.*, vol. IA-21, 1985, pp. 562-570.

[E20] L. Malesani and P. Tomasin: "PWM current control techniques of voltage source converters - a survey," *Proc. IECON'93*, pp. 670 - 675.

[E21] B. Choi, B. H. Cho, R. B. Ridley, and F. C. Lee, "Control strategy for multi-module parallel converter system," *Proc. PESC'90*, pp. 225-234.

[E22] A. Busse and J. Holtz, "Multi-loop control of a unity power factor fast switching ac-dc converter," *Proc. PESC'82*, pp. 171 - 179.

[E23] S. Hiti and D. Borojevic, "Control of front-end three-phase boost rectifier," *Proc. APEC'94*, pp. 927-933.

[E24] L. Malesani, P. Tenti, E. Gaio, and R. Piovan, "Improved current control techniques of VSI PWM inverters with constant modulation frequency and extended voltage range," *IEEE Trans. Ind. Appl.*, vol. IA-27, 1991, no. 2, pp. 365-369.

[E25] L. Malesani, P. Mattavelli, and P. Tomasin, "Improved constant-frequency hysteresis current control of VSI inverters with simple feed-forward bandwidth prediction," *Proc. IAS'95*, pp. 2633 - 2640.

[E26] L. J. Borle and C. V. Nayar, "ZACE current controlled power flow for ac-dc power converters," *Proc. PESC'94*, pp. 539-546.

[E27] J. W. Kolar, H. Ertl, K. Edelmoser, and F. C. Zach, "Analysis of the control behavior of a bidirectional three-phase PWM rectifier system," *Proc. EPE'91*, pp. 95-100.

[E28] N. R. Zargari and G. Joos, "A three-phase current-source type PWM rectifier with feed-forward compensation of input displacement factor," *Proc. PESC'94*, pp. 363-368.

[E29] S. Hiti, V. Vlatkovic, D. Borojevic, and F. C. Lee, "A new control algorithm for three-phase PWM buch rectifier with input displacement factor compensation," *IEEE Trans. Power Electron.,* vol. 9, no. 2, pp. 173-180.

[E30] J. Espinoza and G. Joos, "On-line generation of gating signals for current source converter topologies," *Conf. Rec. ISIE'93*, pp. 674-678.

[E31] B. H. Cho, "*Modeling and analysis of spacecraft power systems*," Ph. D. Dissertation, Blacksburg, VA: VPI&SU, 1985.

[E32] M.F. Schlecht, "A line interfaced inverter with active control of the output current waveform," *Proc. PESC'80*, pp. 234-241.

[E33] F. Huliehel, F. C. Lee, and B. H. Cho, "Small-signal modeling of the single-phase boost high power factor converter with constant frequency control," *Proc. PESC'92*. pp. 475-482

[E34] R. B. Sepe and J. H. Lang, "Inverter nonlinearities and discrete-time vector current control," *Proc. IPEC'92*, pp. 494 - 501.

[E35] J. W. Choi and S. K. Sul, "A new compensation strategy reducing voltage/current distortion in PWM VSI systems operating with low output voltages," *IEEE Trans. IA-31*, pp. 1001 - 1008, 1995.

[E36] R. D. Middlebrook, "Input filter considerations in design and applications of switching regulators," *Proc. IAS'76*, pp. 366-382.

[E37] V. R. Stefanovic and S. N. Vukosavic, "Space-vector PWM voltage control with optimized switching strategy," *Proc. IAS'92*, pp. 1025 - 1033.

[E38] H. Mao, D. Boroyevich, and F. C. Lee, "Novel reduced-order small signal model for three-phase PWM rectifiers," *Proc. PESC'96, pp. 556 - 562.*

6. Patent and Invention Disclosures Related to This Work

[F1] H. Mao and F. C. Lee, "DC-link soft-switched AC-DC-AC converters," *VTIP* 96-032, Virginia Polytechnic Institute and State University, April 1996.

[F2] H. Mao and F. C. Lee, "Zero-voltage-transition three-phase buck and buck-boost rectifiers," *VTIP* 96-033, Virginia Polytechnic Institute and State University, April 1996.

[F3] H. Mao, F. C. Lee, and D. Boroyevich, "Novel zero-current transition DC-DC and three-phase converters", *VTIP* 95-054, Virginia Polytechnic Institute and State University, Oct. 1995.

[F4] H. Mao and F. C. Lee, "Zero voltage transition three-phase converters with reduced auxiliary switch stress", *VTIP* 95-055, Virginia Polytechnic Institute and State University, Oct. 1995.

[F5] H. Mao and F. C. Lee, "Soft-switched and multi-level 2-quadrant boost choppers", *VTIP* 95-056, Virginia Polytechnic Institute and State University, Oct. 1995.

[F6] H. Mao and F. C. Lee, "Improved zero voltage transition 3-phase PWM voltage link converters", *U. S. Patent 5, 574,636.*

Appendix A. Power Loss Model of IGBT Devices Used in the Simulation

It is very important to be able to evaluate the power loss in a converter by simulation, so that the efficiency performances of different topologies can be easily compared under the same operating conditions. Although some simulating programs such as Saber and Spice have physics-based component models for some power devices, these models are not suitable for three-phase converter simulation over a relatively long period, because:

(a) the model parameters are difficult to extract;

(b) models are available only for very limited components;

(c) simulation with these complex models is very time consuming and usually has convergence problems;

(d) the power loss, especially the switching loss, of power semiconductor devices is not computed accurately with these models.

To simulate the converter power loss in a real operation environment, simple component loss models can be developed with some "lossy" components added to the ideal devices. These loss models are shown in Fig. A.1.

- The power loss in an inductor has two parts: magnetic core loss and winding loss. It is very difficult to calculate the inductor power loss accurately. However, the purpose of the simulation is to compare the power loss of the hard-switching converter and different soft-switching converters, so only the resonant inductor loss in the auxiliary circuit needs to be modeled accurately. The current in the resonant inductors in all the soft-switching topologies discussed has similar waveforms and similar frequency spectrum, so their difference in power loss is mainly determined by the magnitudes of the currents they conducted. Since the flux in a resonant inductor is directly proportional to the current, and the core loss is mainly the eddy current loss, the inductor power loss, including both the winding loss and the core loss, is approximately proportional to the square of the inductor current, and can be modeled as a series resistance.

- Diode conduction loss is represented by its junction voltage Von and series resistance Rs.
- IGBT switch is modeled as an ideal voltage controlled switch (VCS) in series with an ideal diode to prevent reverse current. Its conduction loss is modeled by the diode on voltage Von and the on-resistance Ron of the VCS. MOSFET switches are usually used in the auxiliary circuit, and their conduction loss is modeled by the on-resistance of the voltage controlled switch.
- The switching losses of power semiconductor devices are modeled through PWM cells. The switching loss in a PWM cell (i.e. a switch-diode pair) is modeled as two current-controlled current pulse sources (CCCPS), as is shown in Fig. A.1(d). This is because the turn-on loss (including the diode reverse recovery loss) and the turn-off loss of a switch are approximately proportional to the voltage and current switched. The waveforms of the CCCPSs are shown in Fig. A.1(e). The CCCPS for turn-on loss, J_{on} with a duration of T_{on}, is connected across the diode, and has a magnitude proportional to the diode current prior to the switch's turn-on: $J_{on} = K_{on} i(D)$. The CCCPS for turn-off loss, J_{off} with a duration of T_{off}, is connected across the switch, and has a magnitude proportional to the switch current prior to its turned off: $J_{off} = K_{off} i(S)$. K_{on}, K_{off}, T_{on} and T_{off} are constant coefficients independent of circuit operation. The selection of T_{on} and T_{off} should result in $K_{on} < 1$ and $K_{off} < 1$ to ensure a correct simulation. Also, T_{off} will determine the effect of snubber capacitors in reducing switching turn-off loss. In the simulation, the loss model parameters of all IGBTs are extracted from experimental data.
- The turn-on loss of MOSFETs in the auxiliary circuit is assumed to be zero, because they are always turned on with zero current. Their turn-off loss is also small, and very difficult to measure. In the simulation, $K_{off} = 0.1$, and $T_{off} = 0.1$ uS are assumed.

The parameters of the conduction loss models are relatively straightforward, and

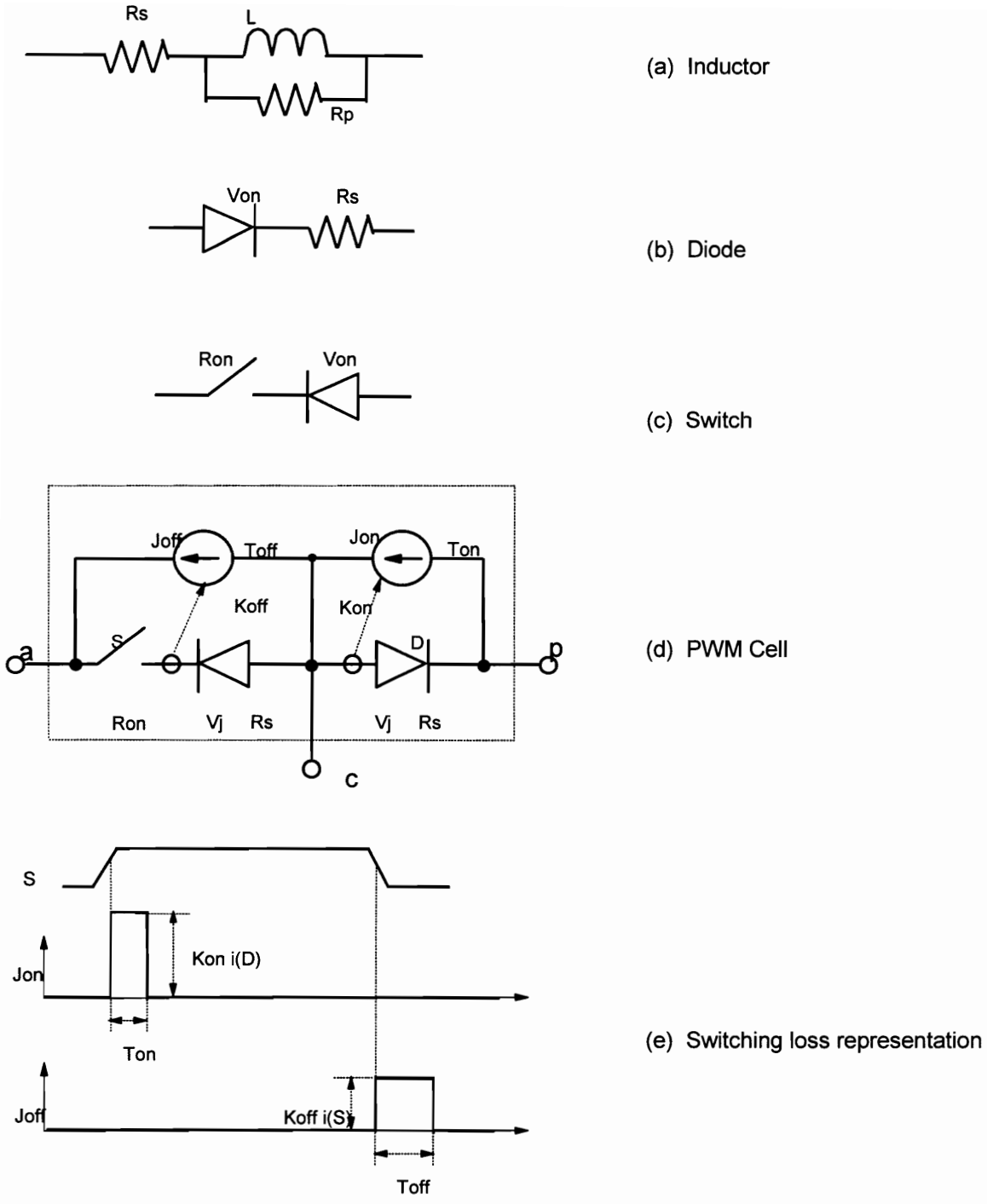


Figure A.1 **Loss model of major devices**. The power loss of the devices is represented by ideal component models.

can be calculated from the manufactures databooks or experimental results. The parameter extraction of switching loss models is more complex, and will be explained in detail. At 125°C junction temperature, the switching losses of IXGK50N60AU1 are measured with different snubber capacitance *Cs* and collector current *Ic,* under collector-emitter voltage V_{dc} = 300 V and 400 V. The switch loss data are listed in Table A.1. Similarly, the switching losses of CM50DY-24H at 125°C junction temperature, 500 V and 800 V collector-emitter voltages are tested, and are listed in Table A.2.

In the switching loss models shown in Fig. A.1(d) and (e), T_{on} and K_{on} are used to evaluate device turn-on loss (including diode reverse recovery loss), and T_{off} and K_{off} are used to evaluate device turn-off loss. The basic assumptions in this model are:

- Both the turn-on loss and the turn-off loss of a device in a hard-switching condition are proportional to the product of its switching voltage and switching current. The proportional coefficients are:

$$K_1 = K_{on}T_{on} \text{ for the turn-on loss,} \quad \text{(A1)}$$

$$K_2 = K_{off}T_{off} \text{ for the turn-off loss.} \quad \text{(A2)}$$

- The effect of snubber capacitance on the turn-off loss can be accounted on by a proper selection of K_{off} and T_{off}. This effect is important to correctly simulate the power loss in a zero-voltage switching (including zero-voltage transition) topology;
- The turn-on loss of IGBTs under zero-voltage switching conditions is neglected. According to our test results, the turn-on loss under a zero-voltage condition is usually below 5% of the hard-switching value, and doesn't have significant effect on converter loss. This facts also complies with the conclusions in [A14] [A17] [A20] [A21].

From the model in Fig. A.1(e), we know that the switching energy losses per switching event at a switch current of i_c and switch voltage of v_{dc} are calculated as:

Turn-On Loss: $$E_{on} = K_{on}T_{on}v_{dc}i_c = K_1 v_{dc}i_c, \quad \text{(A3)}$$

Turn-Off Loss without snubber capacitors:

Table A.1 Switching Losses of IXGK50N60AU1

V_{dc} = 300 V					
Turn-On		Turn-Off Cs = 0		Turn-Off Cs = 11.9	
Ic (A)	Eon (mJ)	Ic (A)	Eoff (mJ)	Ic (A)	Eoff (mJ)
10.27	0.334	20.75	1.316	20.63	0.788
20.7	0.706	30.65	1.88	30.25	1.25
30.8	1.1	39.97	2.38	39.5	1.71
39.8	1.46	49.63	2.96	50.1	2.12

V_{dc} = 400 V					
Turn-On		Turn-Off Cs = 0		Turn-Off Cs = 11.9	
Ic (A)	Eon (mJ)	Ic (A)	Eoff (mJ)	Ic (A)	Eoff
9.95	0.465	20.63	1.69	20.13	1.06
19.75	0.944	30.35	2.6	30.02	1.63
29.65	1.32	40.25	3.47	40.45	2.34
39.78	2.02	50.42	4.38	50.37	3.09

Table A.2 Switching Losses of CM50DY-24H

V_{dc} = 500 V			
Turn-On		Turn-Off Cs = 0	
Ic (A)	Eon (mJ)	Ic (A)	Eoff (mJ)
9.75	0.67	20.2	2.11
20.3	1.37	29.95	2.76
30.1	2.14	40.6	3.39
39.65	2.98	50.6	3.92

V_{dc} = 800 V					
Turn-On		Turn-Off Cs = 0		Turn-Off Cs = 5.6 nF	
Ic (A)	Eon (mJ)	Ic (A)	Eoff (mJ)	Ic (A)	Eoff (mJ)
10.15	1.54	19.8	3.18	20.3	2.07
20.45	2.97	30.15	4.9	30.1	3.32
30.6	4.65	39.25	6.19	39.95	4.47
39.8	6.2	50.15	7.72	49.65	5.81

$$E_{off} = K_{off} T_{off} v_{dc} i_c = K_2 v_{dc} i_c, \tag{A4}$$

Turn-Off Loss with a snubber capacitance of C_s and $T_{off} \geq \frac{C_s v_{dc}}{i_c(1 - K_{off})}$:

$$E_{off} = K_{off} T_{off} v_{dc} i_c - \frac{K_{off}}{2(1 - K_{off})} C_s V_{dc}^2 \tag{A5}$$

Turn-Off Loss with a snubber capacitance of C_s and $T_{off} < \frac{C_s v_{dc}}{i_c(1 - K_{off})}$:

$$E_{off} = \frac{K_{off}(1 - K_{off})}{2C_s} i_c^2 T_{off}^2 \tag{A6}$$

For each turn-on loss measurement under the hard-switching condition, equation (A3) can be used to calculate k_1:

$$k_1(j) = \frac{e_{on}(j)}{v_{dc}(j) i_c(j)}. \tag{A7}$$

where $e_{on}(j)$, $v_{dc}(j)$ and $i_c(j)$ are respectively the *jth* turn-on energy, switching voltage and switching current measurements. The current-weighted average value of k_1 can be used as K_1:

$$K_1 = \frac{\sum_j k_1(j) i_c(j)}{\sum_j i_c(j)}. \tag{A8}$$

K_1 is 1.1895×10^{-7} for IXGK50N60AU1, and 1.6687×10^{-7} for CM50DY-24H, according to (A7) and (A8). The maximum difference between the computed turn-on losses using (A3) and the tested switching losses under the same condition is 6.3% of the tested maximum turn-on loss for IXGK50N60AU1, and 14.3% of maximum turn-on loss for CM50DY-24H. This proves that the simple switching loss model is acceptable in loss analysis.

Theoretically, there is a freedom in choosing K_{on} and T_{on} according to (A1), as long as $0 < K_{on} < 1$ is satisfied. However, to reduce the discretation error in the simulation

due to the finite simulation time step, T_{on} should be chosen large enough. T_{on} should also be lower than the minimum on-time of the switches. In the simulations, $T_{on} = 0.5$ uS is chosen, which results in less than 4% discretation error if the maximum simulation time step is 20 nS. Then $K_{on} = 0.2379$ for IXGK50N60AU1, and $K_{on} = 0.3337$ for CM50DY-24H.

Similarly, for each turn-off loss measurement under the hard-switching condition, The following equation can be used to calculate k_2:

$$k_2(j) = \frac{e_{off}(j)}{v_{dc}(j) i_c(j)}. \qquad \text{(A9)}$$

where $e_{off}(j)$, $v_{dc}(j)$ and $i_c(j)$ are respectively the jth turn-off energy, switching voltage and switching current measurements. The current-weighted average value of k_2 can be used as K_2:

$$K_2 = \frac{\sum_j k_2(j) i_c(j)}{\sum_j i_c(j)}. \qquad \text{(A10)}$$

K_2 is 2.08×10^{-7} for IXGK50N60AU1, and 1.8856×10^{-7} for CM50DY-24H, according to (A9) and (A10). The maximum error of the simulated turn-off losses is 4.2% of the maximum turn-off loss for IXGK50N60AU1, and 1% of the maximum turn-off loss for CM50DY-24H, without snubber capacitors. This proves that the simple turn-off loss model is very accurate for these two devices.

Once K2 is calculated, optimum K_{off} and T_{off} can be chosen to minimize the maximum error of the turn-off losses calculated from (A5) and (A6) and the test data with snubber capacitors. The optimum parameters are $K_{off} = 0.507$, $T_{off} = 0.41$ uS for IXGK50N60AU1 with the maximum error of 9.3%, and $K_{off} = 0.447$, $T_{off} = 0.5167$ uS for CM50DY-24H with the maximum error of 7.1%.

Vita

The author was born in Yuechi, Sichuan, China on March 11,1964. He received his B. S. and M. S. degrees from Chongqing University, China in 1982 and 1989 respecctively, both in electrical engineering. From 1982 to 1986, he worked as an electrical engineer at Southwest Institute of Technology, Chengdu, China. From 1989 to 1992, he was a drive and control system engineer with Chongqing steel and Iron Design and Research Institute, Chongqing, China.

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