THREE-PHASE POWER CONVERSION USING
SOFT-SWITCHING PWM TECHNIQUES

by

Vlatko Vlatković

Dissertation submitted to the Faculty of the
Virginia Polytechnic Institute and State University
in partial fulfillment of the requirement for the degree of
Doctor of Philosophy

in

Electrical Engineering

APPROVED:

Borojević
Dušan Borojević, co-chairman

Fred C. Lee
Fred C. Lee, co-chairman

Dan Chen
Dan Y. Chen

William T. Baumann
William T. Baumann

Martin Klaus

October 11, 1994
Blacksburg, Virginia
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Dušan Borojević, co-chairman
Fred C. Lee, co-chairman
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(ABSTRACT)

This dissertation addresses several key issues related to high-frequency soft-switching PWM three-phase power converters. These are:

1. Analysis, synthesis, and design of three-phase soft-switching PWM power converter topologies,
2. Design of input EMI filters for three-phase converters, and
3. Design of microprocessor controllers for three-phase converters.

An analysis of existing soft-switching PWM techniques is performed, and two generalized soft-switching PWM converter circuit representations are derived. Based on these representations and common topological properties of three-phase and dc-dc PWM converters, two new procedures for synthesis of three-phase soft-switching PWM converters are derived. The two procedures are used to synthesize five new three-phase soft-switching PWM converter topologies suitable for wide range of applications.

A digital signal processor-based controller implementation example is presented. It demonstrates the feasibility of producing versatile, high-
performance, reliable, low-cost digital controllers for soft-switching PWM three-phase power converters operating at high switching frequencies.

A new approach to the design of input filters for ac power electronic circuits is presented here. This approach is based on the application of a vast body of knowledge about passive L-C filters that has existed for many years, but has not been used in power electronics. New passive and active filter pole damping schemes are applied to high-order elliptic filters, resulting in significant filter size reduction compared to the standard filter designs.
To Dragana and Nina
the loves of my life, and
to Edita and Angelo
who made it all possible.
Acknowledgements

In life you throw a ball.

You hope it will reach a wall and bounce back so you can throw it again.

You hope your friends will provide the wall.

Pablo Picasso

Being a student at VPEC is much like having a six-hour, ten-course meal with friends; everything from soup to desert complete with wine, cheese, and coffee, all cooked with love, skill, and good taste. One gets to indulge in rich and diverse flavors and textures of life with people with different backgrounds, cultures, ideas, and attitudes. It is quite clear that this work would not exist without support, trust, and love that they have given me. I acknowledge gratefully my advisers Dr. Dušan Borojević and Dr. Fred C. Lee who created
the possibility and space for my contributions. Their work and commitment to excellence was, and continues to be a true inspiration. Dr. Dan Y. Chen, Dr. William T. Baumann, and Dr. Martin Klaus served as my Advisory Committee members and pointed me in good directions. Juan Sabaté spent many hours with me in quest for questions and answers. Gichao Hua provided some of the most brilliant ideas that are in the foundation of this work. Dr. Wojciech Tabisz and Dr. Milan Jovanović provided many wise advices in situations of doubt and confusion. Yimin Jiang, Hengchun Mao, Laszlo Huber, Silva Hiti, and Goran Stojčić provided valuable discussions and ideas that lead to improvements of this work. Xinfu Zhuang, Carlos Cuadros, and Slobodan Gatarić helped obtain many of the experimental results. Kevin Covi and the IBM Corporation provided the financial support and challenging problems to solve. Teresa Shaw, Tammy Jo Hiner, Bill Cockey, Joyce Smith, and Xiangyu Xiao made sure everything ran clean and smooth. Edita and Angelo just loved me. So did Darcy and Jim. And Dragana and Nina.

When I stop and look back, I marvel and rejoice at how much my life has been enriched by these and other people too numerous to mention by name here. Thank you for bouncing back the ball.
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1.0 Introduction

1.1 Motivation and Objectives

Rapid development of autonomous power systems (for aircraft, spacecraft, ships, military and civilian electric vehicles) and information technology, as well as introduction of stringent harmonic pollution control laws have led to a permanently increasing demand for high-quality, economical, and efficient power conditioning equipment. Today's power converters are required to provide the following features:

1. regulated and undistorted voltages and currents,
2. unity power factor rectification,
3. high efficiency,
4. high power density, and
5. low electro-magnetic interference (EMI).
The primary objective of this work is to find three-phase, medium power range converters that meet these requirements.

To meet the above requirements in medium power applications, three-phase hard-switched PWM converters are most frequently used. The first two requirements are easily met by using one of the many available PWM modulation techniques. It is not the objective of this dissertation to address the issues related to PWM modulation strategies. However, the last three requirements present a problem because hard-switched PWM converters suffer from high switching losses and cause excessive EMI. Due to this, they are operated at relatively low switching frequencies, typically within the audible range, which results in their high weight and volume, and generation of undesirable audible noise.

Elimination of switching losses and reduction of EMI through implementation of some form of soft switching would enable an increase of the converter switching frequency, without reduction of conversion efficiency. This solution would lead to increased converter power density, and to improvements in converter electrical performance. For this reason, the primary methodology to be applied in this dissertation is the use of soft-switching techniques.

Soft-switching converters can be classified into two basic groups: resonant converters and soft-switching PWM converters. All resonant converters suffer from significantly increased current or voltage stresses compared to PWM converters, so soft-switching PWM converters are superior to resonant...
converters in medium and high-power applications. For this reason, only soft-switching PWM converters will be considered in the dissertation.

The creation of existing soft-switching converters has largely been the result of ingenuity and intuition of power supply designers. One of the objectives of this dissertation is to examine the properties of existing soft-switching PWM converters and create a more systematic way to generation of new three-phase soft-switching PWM converter topologies.

The increase of conversion frequency is certainly an effective method of converter filter size reduction. The high switching frequency itself, however, is not always sufficient to provide the desired filter size reduction. This is particularly true in the case of input EMI filters for three-phase rectifiers. With switching frequencies above 10 kHz, standards for EMI pollution become much more stringent than the harmonic pollution standards at frequencies below 10 kHz. For this reason, special care must be taken in input filter design, so that the benefits of increased switching frequency are maintained. It is the objective of this work to examine the issues involved in the design of rectifier EMI input filters, and to provide a systematic and complete design procedure for multiple-stage input L-C filters, that will enable simple and fast design of input filters that are significantly smaller than the ones presently used.

With the availability of three-phase converters switching at high frequencies and employing relatively complex control algorithms, the question of feasibility for reliable, low-cost, high-performance controllers becomes actual. It is one of the objectives of this dissertation to show that today's digital tech-
nology can be successfully used to meet all the converter control requirements in an economical and reliable way.

1.2 Review of Previous Research

In general, at power levels of several kilowatt and above, the switching frequency of hard-switched PWM converters, [A1]-[A11], is limited to the low kilohertz range by parasitics and nonidealties of power semiconductor devices. This limitation is fundamental because even though the power device characteristics are constantly improving, and will undoubtedly continue to do so in the future, there will always exist sufficiently high power levels and switching frequencies at which the power device parasitics will not be negligible. Furthermore, the hard-switched PWM converter control strategy results in high $dv/dt$ and $di/dt$ waveforms capable of producing severe EMI, and device stresses.

To mitigate the above problems, snubber and clamp circuits are widely used, [B1]-[B6], [D7]. They shape the switch voltage and currents so that the stresses are reduced, but they either increase the overall power dissipation, [B1]-[B3], or significantly increase the converter complexity, [B4], [B5].

The first soft-switching converters were the resonant converters, [C1]-[C8]. By adding high-frequency resonant circuits to the converter, the switch voltages and currents are shaped in such manner that there are no high $dv/dt$
and/or $di/dt$ transients, and that the switches are not exposed to high voltage and high current simultaneously.

The literature on resonant converters is very rich, especially in the area of dc-dc power conversion. In the area of three-phase resonant power conversion, the most notable place belongs to the resonant dc link (RDCL) converter, [C3], which enables operation at switching frequencies above 20 kHz and 2 kW. It provides zero-voltage switching (ZVS) conditions for the switches in the bridge by using a resonant circuit at the dc side. The resonant circuit produces high-frequency pulsating voltage across the bridge, and the switches are commutated at the instants when the bridge dc voltage is zero. The soft switching is achieved at the expense of two-fold increase of device voltage stress as compared to the hard-switched PWM converter. Additionally, all the inverter switches are required to switch synchronously with the resonant dc link. This requirement significantly reduces the converter’s ability to achieve fine resolution for synthesizing the input and output waveforms at higher power levels, because the attainable dc link resonant frequency is often not sufficiently higher than the frequency of the synthesized waveform.

Many enhancements of the RDCL converter have been introduced to alleviate these problems, [C4]-[C7]. This effort has resulted in reduction of device voltage stresses to as low as 1.3 times that of the PWM converters, and in development of control strategies capable of providing waveforms of quality comparable to those of PWM converters. However, they introduce auxiliary
switches which process up to 50 % of total power. This significantly reduces the converter efficiency and reliability.

The benefits of soft-switching PWM conversion were first realized in the area of dc-dc converters [D1]-[D10]. There exist three classes of soft-switching PWM converters: the quasi-squarewave converters (QSCs), [D1]-[D2], the soft-switching PWM bridge converters, [D3]-[D7], and the soft-transition (ST) PWM converters, [D9]-[D10].

In the QSCs, [D1]-[D2], the filter inductor runs in discontinuous conduction mode, and is utilized to achieve soft-switching for the power devices. The QSCs provide minimum switch voltage stresses and are capable of processing bidirectional power. Their main drawback is the high device current stress which makes the converters practical only for applications at power levels of several hundred watts.

The soft-switching PWM converter that has found the widest application is the full-bridge (FB) ZVS PWM converter, [D3]-[D7]. It uses resonance between the transformer leakage inductance and the switch output capacitances to provide soft switching for all the converter switches. Its control is simple, the device current and voltage ratings are the same as in the PWM converter, there are no added auxiliary components, and the converter is capable of efficient operation with switching frequencies exceeding 100 kHz. Since the converter provides ZVS, it is most suitable to implement it using power MOSFETs. Based on a similar principle, an FB-zero-current switched (ZCS)
PWM converter was introduced, [D8], which is more suitable for implementa-
tion with minority carrier devices, such as BJTs and IGBTs.

In the ST PWM dc-dc converters, [D9]-[D10], an auxiliary resonant network
is used to produce soft-switching. During the switching transition, the network
is activated to create resonance with the switch parasitic capacitance, and
provide soft switching conditions. After the switch commutation has been
completed, the auxiliary network becomes inactive, and the converter remains
functionally identical to its hard-switched PWM counterpart. Since the auxil-
iary network processes only a small fraction of the total converter power, the
ST technique is very well suited for high-power applications. The application
of this technique in dc-dc converters and single-phase power factor correction
circuits has yielded significant efficiency improvements over the hard-switched
PWM converters.

Application of soft-switching PWM techniques in three-phase power con-
version has only started recently, [E1]-[E9]. The use of QSC concept has been
proposed in only one instance. A ZVS matrix converter has been proposed,
[E1], that gives low device voltage stresses, and good spectral performance
of output voltages and input currents, but is only practical for power levels
below 2 kW due to high device current stresses.

The FB-ZVS-PWM concept has been extended to three-phase power con-
version in [E2] and [E3]. This topology provides transformer isolation, tight
output voltage control, and unity input power factor, all in a single stage power
processing unit. This topology is very well suited for medium power range applications in communication equipment and computers.

The first implementation of the ST PWM concept in three-phase converters has appeared under the names of auxiliary resonant pole inverter, and auxiliary resonant commutated pole inverter, [E4] and [E5]. The independent developments of the ST PWM techniques for dc-dc converters have led to the introduction of the zero-voltage transition (ZVT) three-phase rectifier-inverter, [E6], and finally to the generalization of the ST PWM concept and introduction of several new three-phase converters based on this principle, [E7]-[E9]. All of the ST PWM converters exhibit excellent performance, with minimal device current and voltage stresses.

There have only been a few contributions toward systematic generation of power conversion circuits, [F1]-[F7]. However, none of them is concerned with the synthesis of soft-switching PWM converters or three-phase converters. The work in [F1]-[F3] deals with generation of PWM topologies, while [F4]-[F7], and [H7], present a systematic approach to generation and classification of quasi-resonant and resonant converters.

Practically all papers that address the input filter design for switching power converters are in the area of dc-dc converters, [G1]-[G3]. The main design issue presented in these works is avoiding the impedance interaction between the converter and input filter. The filters are designed using the principle of filter pole separation, [G1]-[G2], which typically yields filters with fairly large component values. A different approach to input current filtering is pre-
sented in [G3], where active filtering is employed as a replacement for one filter stage. In [G5], it has been shown that the issues in design of input filters for ac converters are significantly different from those involved in the input filter design for dc-dc converters. This has created a space for the development of a new input filter design approach in [G6], which yielded filters featuring significant reduction in size, and improvement of performance.

1.3 Dissertation Outline and Major Results

The work presented in the dissertation is divided into the following major parts.

1. Principles of soft-switching PWM power conversion. This chapter is devoted to the development of methods for synthesis of three-phase soft-switching PWM converters. Two synthesis methods are presented, both derived from general properties of PWM converters and necessary conditions for soft-switching. These properties and conditions are derived from the known single-ended soft-switching PWM converters. First, basic topological properties of PWM converters are addressed, and an elementary PWM cell is distinguished. Based on common structural properties of semiconductor switching devices, a universal conceptual circuit model of a nonideal switch is derived. The notion of soft-switching is then general-
ized and defined in terms of switch voltages and currents during switching. Based on the above development, a set of possible elementary soft-switching PWM cells is generated. It is shown that all of the existing soft-switching PWM converters can be classified into only a few groups. To lay a groundwork for synthesis of three-phase converters, these results are applied to generation and classification of soft-switching PWM dc-dc bridge converters.

In order to apply the above described general results in three-phase PWM power converters and derive one synthesis procedure, methods for analysis of three-phase converters are presented. It is shown that, if viewed in a sufficiently small time interval, all three-phase converters can be reduced to dc-dc converters and elementary PWM cells. At that level, the elementary PWM cells can be transformed into soft-switching elementary PWM cells. The process of synthesis of three-phase converters from elementary soft-switching PWM cells is discussed in detail. The second synthesis method is more direct and is based on distinguishing topological similarities between soft-switching PWM dc-dc converters and three-phase PWM converters.

2. **Non-isolated soft-switching three-phase PWM converters.** Three new three-phase soft-switching PWM converters are generated: the ZVT boost rectifier / voltage source inverter (VSI), the three-level ZVT boost rectifier, and the ZVT buck rectifier. Their operation is analyzed, and their characteristics are described. The prototype of the ZVT boost rectifier / VSI has
been built to demonstrate the converter operation. The operation of the three-level ZVT boost rectifier and the ZVT buck rectifier is verified through simulation.

3. **Isolated soft-switching three-phase PWM rectifiers.** A three-phase ZVS PWM and a three-phase ZCS PWM bridge rectifiers with transformer isolation are presented. They are created as a generalization of the FB ZVS and FB ZCS PWM dc-dc converters. Their operation is described and their characteristics are discussed. The prototype of the ZVS rectifier has been built to demonstrate the converter operation. The operation of the ZCS converter is verified through simulation.

4. **Controller implementation for the ZVS three-phase buck rectifier.** A digital signal processor-based controller implementation for the three-phase ZVS buck rectifier switching at 100 kHz is presented. This controller implementation example clearly demonstrates the feasibility of producing versatile, high-performance, reliable, low-cost controllers for soft-switching PWM three-phase power converters operating at high switching frequencies.

5. **Input filter design for switching rectifiers with power factor correction.** It is shown that the issues involved in the design of power factor correction circuit input filters are significantly different from those involved in the design of input filters for dc-dc converters. In many cases, the EMI and power
factor requirements are impossible to meet using the existing filtering technology. The use of high order elliptic filters to achieve the required EMI attenuation and power factor is proposed. The new input filter technology provides a significant filter size reduction over the standard filter designs, minimizes the filter-converter interaction, and maintains a good converter power factor. New active and passive filter damping methods that guarantee optimal filter pole damping, while virtually eliminating damping resistor power dissipation, will be proposed. A filter design procedure that makes possible a simple and fast design of filters with an arbitrary number of stages is also presented.
2.0 Principles of Soft-Switching PWM Power Conversion

2.1 Introduction

The creation of the existing soft-switching converters has largely been the result of ingenuity and intuition of power converter designers. There have only been a few contributions toward systematic generation of power converters, and none of them were concerned with the synthesis of soft-switching PWM (SSPWM) three-phase converters.

The specific questions that are addressed in this chapter are:

1. Are there any topological similarities between different soft-switching PWM converters?
2. Are there any operation procedures common in all soft-switching PWM converters?

3. How can these common properties be generalized and modeled?

4. How can these general models be extended for the analysis and synthesis of three-phase soft-switching PWM converters?

The answers to these questions are addressed starting from two examples of simple single-ended dc-dc SSPWM converters. In these examples the notion of soft-switching is defined in terms of switch voltages and currents during switching. Based on this definition, a set of possible elementary SSPWM cells is generated. It is then shown that all existing SSPWM converters can be classified into only a few groups. A similar approach is taken to derive the structure and properties of bridge-type SSPWM converters.

In order to extend the results derived based on dc-dc converters to three-phase PWM power converters, methods for analysis and synthesis of three-phase converters are presented. It is shown that, if viewed in a time frame of high-frequency switching period, all three-phase converters can be reduced to dc-dc converters. At this level, the elementary PWM cells can be transformed into elementary SSPWM cells. The process of synthesis of three-phase converters from elementary SSPWM cells is discussed in detail.
2.2 Elementary Soft-Switching PWM Cells

2.2.1 An Intuitive Approach

Consider the simple ideal PWM converter shown in Figure 2.1.a. If both the diode and switch were ideal (infinitely fast and with no energy stored in them), the switching waveforms would look as in Figure 2.1.b. There would be no current-voltage overlap during switching, and no parasitic oscillations. Therefore, in an ideal PWM converter, all current and voltage waveforms would be square, and there would be no switching losses.

However, the finite transistor and diode switching speeds cause current-voltage overlap during switching, resulting in switching losses. Also, the component parasitic capacitances and inductances are excited by high $di/dt$ and $dv/dt$ causing parasitic oscillations, which result in additional switching loss increase and high device voltage and current stresses. Possible switching waveforms in a PWM converter are shown in Figure 2.1.c.

These problems can be resolved if the nonideal switching device characteristics are taken into account, and if some form of soft-switching is implemented.
Figure 2.1. Switching in a PWM converter: a) A simple PWM converter, b) switching waveforms in the ideal case, and c) switching waveforms in reality.
Example 1 (ZVT PWM boost dc-dc converter). Figure 2.2 shows the ZVT PWM boost dc-dc converter, [D9], and circuit waveforms during a switching transition in which the inductor current is commutated from the diode to the switch. The soft-switching is achieved in the following way:

Charging Phase. At the beginning of commutation, the auxiliary switch $S_\ell$ is closed, starting the charging phase of the commutation circuit. The current through inductor $L_\ell$ starts to increase from zero, gradually diverting the current from the diode $D$ to the commutation circuit. After some time, the current $i_\ell$ reaches the inductor current, $i_l$, and diode $D$ blocks. The rate at which the diode current is reduced is controlled by the inductance value of $L_\ell$. The gradual diode current reduction practically eliminates any problems with diode reverse recovery.

In hard-switched converters, the amplitude of the diode reverse recovery current (corresponding to the first largest current spike in Figure 2.1.c) is proportional to the voltage applied to the diode during the recovery. In high-voltage and high-power circuits, these spikes can reach extremely high values so that the diode reverse recovery represents one of the biggest problems in the operation of hard-switched converters.

Resonant and Clamping Phase. After $D$ has blocked, a resonance between the inductor $L_\ell$ and the parasitic capacitances of $D$ and $S$ starts. This leads to two things: $i_\ell$ further increases, reversing the currents $i_p$, $i_d$, and $i_m$, which are now flowing through the switch and diode parasitic capacitances. These negative currents cause gradual reduction of voltage.
Figure 2.2. The ZVT PWM boost dc-dc converter: Commutation from diode to MOSFET.
νs, and increase of νd. When νs reaches zero, the MOSFET body diode, DM, starts conducting, clamping the switch voltage to zero. At this time, S is turned on with no voltage across it and no current through it.

**Discharging Phase.** To complete the current commutation, Sx is opened, and ix starts flowing through Dx. This reverses the voltage across Lx so that ix gradually reduces to zero. The currents ip and is start increasing, and when they become positive again, is is transferred from DM to S, while νs is maintained at zero. Eventually, the entire current I is transferred to S, when the commutation circuit becomes inactive.

It should be noted that the commutation from S to D takes place naturally. When S is turned off, I charges the parasitic capacitance of S so that νs gradually increases until D starts conducting.

**Example 2 (ZVS PWM buck dc-dc converter).** Figure 2.3 shows the ZVS PWM buck dc-dc converter, [D13], and circuit waveforms during a switching transition in which the inductor current is commutated from the diode, D, to the transistor. The soft-switching is achieved in the following way:

**Resonant Phase.** Before the beginning of the commutation the auxiliary current ix = I is circulating through Sx, and the diode D is conducting the inductor current. The commutation process is initialized by opening Sx. This starts the resonance between Lx and the parasitic capacitance of S. The switch voltage νs is first increased, and then decreased in a reso-
Figure 2.3. The ZVS PWM buck dc-dc converter: Commutation from diode to MOSFET.
nant fashion, until it finally reaches zero. At that point, $DM$ starts con-
ducting, initiating the clamping phase.

**Clamping Phase.** In this phase $v_s = 0$, and $S$ is turned on with no
losses.

**Charging Phase.** $L_x$ is charged by the input voltage $V$ until its current
reaches $I$. At that point, $D$ blocks, and $v_d$ abruptly rises, causing some re-
verse recovery and oscillations between $L_x$ and the parasitic capacitance
of $D$.

Even though the two circuits form the above example differ very much in
topology and operation, the events leading to soft-switching are the same in
both converters. The soft-switching procedure can be summarized as follows:

1. **Reversal of $i_s$.** Reversal of $i_s$ is required because this reduces $v_s$ to zero
by discharging the switch parasitic capacitance. In the above examples,
the current reduction and reversal are achieved by connecting an auxiliary
inductor, $L_x$, to the circuit. Two other methods of doing this have been re-
ported in the literature. The first one is used in isolated bridge converters,
and utilizes the transformer leakage inductance, [D3]-[D8]. This method
will receive more attention in the later part of this chapter. The second
method uses the converter main filter inductor running with large current
ripple, and having a portion of the current negative for some time, [D1],
[D2]. This method is only practical for relatively low power applications due
to increased conduction losses caused by the large inductor currents. It is,
therefore, ill-suited for higher-power three-phase applications, and will not be addressed in more detail.

2. **Switching with zero volts across the switching device.** Since all semiconductor switches are passive devices, no voltage across them guarantees no losses. Once the device voltage has been reduced to zero by current reversal, it has to be clamped at zero for appreciable amount of time. This clamping is required for two reasons. First, all devices have finite switching speeds, and the device voltage has to be zero during the entire commutation process. Second, this creates a time interval in which the switch can be commutated, so that the turn-on or turn-off timing is not critical.

The voltage clamping is typically done by an antiparallel connection of a switch and a diode, such as $S$ and $DM$ in the above examples. $DM$ serves as the voltage clamping device during turn-on of $S$, while $S$ is the voltage clamping device during turn-off of $DM$.

The turn-off of diodes $D$ in both examples is improved by the addition of the auxiliary circuits, but is still not completely lossless. Gradual diode current removal is beneficial for reduction of current-voltage overlap during diode turn-off which significantly improves the switching conditions compared to the hard-switched converter. Some losses, however, are still present because there is no voltage clamping during turn-off of $D$, and the voltage $V$ is applied to $D$ the immediately after $i_D$ reaches zero. Therefore, both diodes experience some reverse recovery problems, the magnitude of which depends on the rate of decrease of $i_D$. 

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In both converters, the transistor turn-off is hard. This situation can be mitigated by connecting a capacitor in parallel to the transistor. The capacitor reduces the rate of voltage rise during turn-off, and thus reduces the switching loss. Since the voltage $v_s$ is reduced to zero before transistor turn-on, the energy stored in the capacitor is not dissipated.

In both examples, soft switching is achieved by adding an auxiliary commutation network to the elementary PWM switching cell. The main function of the networks is to shape the voltage across the switch, so that the soft-switching conditions can be achieved.

The SSPWM converters of Figure 2.2 and Figure 2.3 can be modeled by more general networks shown in Figure 2.4.a and b, respectively. Both the PWM buck and boost dc-dc converters are modeled as an elementary PWM switching cell with the inductor and capacitor replaced by dc current and voltage sources, respectively, and $S$ and $D$ are modelled by single-pole single-throw switches. The commutation circuits are modeled as current sources $i_x$, with standard waveforms that provide soft-switching. In Figure 2.4.a, one side of $i_x$ is connected to a single-pole double-throw switch which connects it either to point $a$ or to point $b$. The operation of this switch is synchronized with the commutation of the main switches, $S$ and $D$. The exact timing and operation of the commutation circuit switch depend on the particular PWM converter topology and implementation of $i_x$. Many different implementations are discussed throughout the dissertation.
Figure 2.4. Generalized SSPWM converter models: a) ZVT boost dc-dc converter, and b) ZVS buck dc-dc converter.
It is shown in the next section through more systematic and rigorous derivation that the two circuits of Figure 2.4 represent the models of all possible single ended SSPWM converters. The circuit of Figure 2.4.a models all SSPWM converters in which the commutation circuit is connected in parallel to the main power flow path. These circuits are known as ZVT and ZCT PWM converters, [D10], [E7].

The circuit of Figure 2.4.b models all SSPWM converters in which the commutation circuit is placed in the main power flow path. The SSPWM converters from this group originate from the family of quasiresonant converters (QRC), [H10], and also include multiresonant and resonant converters, [H10], as well as the quasi-square wave converters, [D1], [D2].

The significance of these representations is twofold. First, the resulting circuits are simple, so that the underlying principles for obtaining soft switching can be applied easily in all PWM converters, including the more complicated ones, such as three-phase PWM converters. Second, the process of obtaining soft-switching is viewed independently of the specific commutation circuit implementation. This enables generation of different commutation circuits depending on the PWM switch implementation (diode and MOSFET, diode and IGBT, two MOSFETs in a bridge, etc.), and particular switching action needs (ZVS or ZCS), [D10], [E7], [E5].
2.2.2 Generation and Properties of Elementary SSPWM Cells

The examples presented in the previous section open a possibility for approaching the question about obtaining soft-switching in PWM converters more generally. Some circuits must be added to PWM converters to obtain soft switching. If these circuits are modelled as current or voltage sources, in what ways can they be connected to the basic PWM converters, and what are the properties of the resulting circuits? This section will address these issues in a more formal manner.

A. SWITCH MODEL AND SOFT-SWITCHING CONDITIONS

The first step is to clearly define the notion of soft switching. In general, the term soft switching means switching without power loss. The definition of soft switching is closely related to the physical properties of semiconductor devices used in the PWM converter. These switching devices can be uncontrolled, like diodes, or controlled, like BJTs, IGBTs, MOSFETs, etc. All semiconductor switching devices have static and dynamic imperfections. Since the operation of semiconductor switches is based on conductivity modulation and charge storage, [H1], the nature of these imperfections is mostly resistive and capacitive. Inductive effects in semiconductor switches are typically very small. The inductances present in practical switches originate from the switch package geometry and stray inductances rather than from the physical prop-
erties of the semiconductor device. These inductances are therefore further regarded as parts of the circuitry external to the semiconductor device.

Based on this, a semiconductor switch can be modeled as a parallel combination of a controlled or uncontrolled passive nonlinear resistor and a controlled or uncontrolled passive nonlinear capacitor, as shown in Figure 2.5. The parallel connection is justified by the requirement that the switch behaves as a resistor in steady-state.

In PWM converters most switches are either voltage two-quadrant or current two-quadrant, and are most often implemented using more than one semiconductor device (with the exception of diodes and four-layer devices such as SCRs, MCTs, etc.). Implementation and performance of soft-switching circuits are largely determined by the main switch implementation. Figure 2.6 shows the typical characteristics and some possible implementations of switches in PWM converters. The main difference between the voltage and current two-quadrant switches as it relates to providing soft-switching conditions is in the voltage clamping capability of the switch. Current two-quadrant switches are typically implemented as an antiparallel connection of a diode and a transistor so that the diode can be used as a voltage clamping device for the transistor, and vice versa. In this situation, it is possible (though it is not necessarily always the case) to obtain ideal switching conditions for both the transistor and the diode. In contrast, voltage two-quadrant switches are implemented as a series connection of a diode and a transistor; therefore, the voltage across each of them is difficult to control. It is commonly the case that
Figure 2.5. Semiconductor switch model.
Figure 2.6. Implementation and characteristics of switches: a) Current two-quadrant, and b) voltage two-quadrant.
only the transistor has soft-switching conditions, while the diode suffers from reverse recovery. Both cases will be illustrated by several examples throughout the dissertation.

Since the model of Figure 2.5 is valid regardless of the switch implementation, in the further discussions all semiconductors used to implement the switch are modeled as a single R-C combination.

According to the switch model in Figure 2.5, soft-switching can be defined as:

**Definition 2.1:** Soft switching is transition from $R_s \approx 0$ to $R_s \to \infty$ or vice versa, such that $v_s(t) \equiv 0$ while $R_s \neq 0$ nor $\infty$. □

The symbol "≡" is used here to denote "identically equal" and implies that $v_s(t)$ and all its derivatives, $dv_s(t)/dt$, $a^2v_s(t)/dt^2$, etc., are equal to zero. The definition 2.1 is general in the sense that it is valid for both switch turn-on, and switch turn-off. The terms ZVS and ZCS, as well as the terms ZVS and ZCS converter, are precisely defined next.

**Definition 2.2:** Zero-voltage switching is switch turn-on or turn-off with $v_s(t) \equiv 0$. □

**Definition 2.3:** Zero-current switching is switch turn-on or turn-off with $i_s(t) \equiv 0$. □
Definition 2.4: A ZVS converter is a converter in which the transistor is turned on with $v_s(t) = 0$. □

Definition 2.5: A ZCS converter is a converter in which the transistor is turned off with $i_s(t) = 0$. □

Formally, the relationship between conditions $i_s(t) = 0$ and $v_s(t) = 0$ is a consequence of the following proposition:

Proposition 2.1: Assuming that in the model of Figure 2.5 $C_s$ is finite, and $R_s > 0$, the following statements are true:

(1) $v_s = 0 \Rightarrow i_s \equiv 0$, and

(2) $i_s = 0 \not\Rightarrow v_s = 0$.

Proof: (1) is true because from the two assumptions: $v_s = 0 \Rightarrow i_R = 0$, and $v_s = 0 \Rightarrow dv_s/dt = 0 \Rightarrow i_C = 0$. (2) is true because even if $i_s = 0$ there could be some charge stored in $C_s$ causing current through $R_c$. □

In other words, the above proposition implies that ZCS is lossless only if $v_s(t) = 0$. As it will shortly be illustrated by several examples, many ZCS converters do not provide the condition $v_s(t) = 0$, so there are some losses during
switch turn-off. This is the main reason why the ZCS converters are much less used in practice than the ZVS converters. The switching losses in ZCS converters are, however, much reduced compared to the hard-switching converters. There are many cases in which the switching conditions are not ideal but the switching losses are much smaller than in hard-switched converters.

In general, switching with $v_s(t) \approx 0$ and $i_s(t) \approx 0$ will be referred to as quasi-soft switching. Under these conditions, the $v_s(t) i_s(t)$ product is significantly smaller than in the hard-switched case. The quasi-soft switching conditions are typically obtained by controlling the rate of change of $i_s(t)$ and $v_s(t)$ during switching. The following definition introduces the terminology for switching in which the losses are reduced.

**Definition 2.6:** Quasi-soft switching is transition from $R_s \approx 0$ to $R_s \to \infty$ or vice versa, such that the $v_s(t) i_s(t)$ product is small while $R_s \neq 0$ nor $\infty$. □

In more practical terms the quasi-soft switching conditions can be obtained by reducing $v_s(t)$ or $i_s(t)$ or both to a value close to zero, and then maintaining this value small during switching. This is most often achieved by connecting reactive components to the switch, so that the rate of change of $v_s(t)$ or $i_s(t)$ is limited by something other than the switch and circuit parasitic components.

In all quasi-soft turn-on transitions, the energy stored in $C_s$ is dissipated. In many cases, however, the power dissipated in this way is much smaller than the $v_s(t) i_s(t)$ product during hard switching.
From the switch model (Figure 2.5) it can be seen that at switch turn-off:

\[ i_s(t) = i_R(t) + i_C(t), \quad (2.1) \]

and

\[ v_s(t) = R_s(t)i_R(t) + \frac{1}{C_s(t)} \int_0^t i_C(\xi) d\xi. \quad (2.2) \]

So, both \( v_s(t) \) and \( \frac{dv_s(t)}{dt} \) are proportional to \( i_s(t) \), which means that \( i_s \approx 0 \) provides quasi-soft switching conditions at both turn-off and turn-on. To intuitively illustrate the significance of the above definitions, several examples from practice are presented in which the switching transitions are analyzed using the above definitions.

**Examples 1 and 2 revisited.** It was mentioned before, that \( S \) turns on and \( DM \) turns off with \( v_s \approx 0 \). These switching conditions are ideal. The diode \( D \), however, turns off under quasi-soft switching conditions because \( i_D \) is reduced gradually to zero prior to diode turn-off. The voltage \( V \) is applied to the diodes shortly after \( i_D \) reaches zero, and as a result that they experience reverse recovery. In practice, this may not be a severe problem if \( L_x \) is designed so that the reduction of \( i_D \) is sufficiently slow. In that case excess carriers in the device are recombined by the time \( i_D \) reaches zero and diode switching losses are very small.
In both converters, the turn-off of $S$ is hard. Quasi-soft switching conditions can, in this case, be achieved by connecting a capacitor in parallel with $S$. The capacitor reduces the rate of switch voltage rise during turn-off, so switching losses are reduced. Since at turn-on of $S$ $v_S(t)=0$, the energy stored in $C_S$ is not dissipated. In the converter of Example 1 the capacitor placed in parallel to the switch also helps reduce the losses during turn-off of $D$. This, however, is not true in Example 2.

**Example 3 (ZCS quasi-resonant flyback converter in full-wave mode).**

Figure 2.7 shows the circuit and experimental waveforms of the ZCS flyback QRC in full-wave mode, [H11]. When the resonant inductor current $i_{LR}$ becomes negative, the voltage across $Q$ and $BD$ is clamped to zero due to conduction of APD. Under this condition, both $Q$ and $BD$ are turned off without losses. In this case, the zero-current and zero-voltage conditions of $Q$ and $BD$ are equivalent.

The turn-on of $Q$ is quasi-soft because the rate of current increase is reduced by $LR$. The turn-off of APD is also quasi-soft. Since $Q$ is off, there is no voltage clamping action during diode turn-off, and the diode experiences reverse recovery and large voltage stress due to interruption of $i_{LR}$. The diode turn-off, however, is still improved compared to the hard-switched case, due to the presence of $LR$. 

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Figure 2.7. ZCS flyback QRC in full-wave mode, [H11].
Example 4 (ZCS quasiresonant flyback converter in half-wave mode).

Figure 2.8 shows the circuit and experimental waveforms of the ZCS flyback QRC in half-wave mode, [H12]. The switch is a voltage two-quadrant switch and the conditions at turn-off are less than ideal. There is no voltage clamping device across $D1$, but $Q1$ has the antiparallel body diode. The turn-off of $Q1$ is lossless because its body diode conducts. The turn-off of $D1$ is quasi-soft because the rate of change of its current is limited by the transformer leakage inductance. Still, reverse voltage is applied to $D1$ during turn-off, and it experiences reverse recovery and losses. If in a hypothetical case the switch were implemented using a single semiconductor device, such as SCR, this converter would provide only quasi-soft switching conditions.

Comparing the four examples analyzed above, it is concluded that the ZVT boost converter (Example 1) provides overall the best switching conditions for its semiconductor devices. Switch voltages can be kept practically at zero during all switching transitions, which means that the switching is virtually lossless.

The soft-switching condition $v_s \equiv 0$ can be achieved by connecting circuits to the switch that shape the switch voltage during switching. Two trivial solutions, shown in Figure 2.9.a and b, use an ideal switch to achieve soft-switching conditions for the nonideal switch. The scheme in Figure 2.9.a can provide both soft turn-on and soft turn-off, while the scheme in Figure 2.9.b
Figure 2.8. ZCS flyback QRC in half-wave mode, [H12].
Figure 2.9. Methods for obtaining soft-switching conditions: (a) and (b) using ideal switches, (c) and (d) using external current sources, and (e) using a voltage source.
provides only soft turn-off. Both of these schemes have been used in practice, [D11], [D12]. In both cases, the ideal switch has been replaced by a MOSFET which assisted the commutation of much slower IGBTs or BJTs. These two schemes are of great significance and could be a subject of study and a basis for development of new semiconductor devices. However, they will not be considered here any further.

If the circuits for obtaining soft-switching in a more general case are modeled as current or voltage sources connected to the switch, there are three ways of obtaining soft switching, as shown in Figure 2.9.c, d, and e. The idea is to insert these switches later into a PWM cell, and obtain SSPWM cells in this way.

**B. ELEMENTARY PWM CELL**

The basic building block of any PWM converter is a single-pole, multiple-throw switch, shown in Figure 2.10.a. An N-throw switch consists of N throws that connect the pole \( p \) to the terminals 1 through \( N \). The pole is always connected to one and only one of the terminals, while a terminal may be left unattached. Therefore, in a PWM converter, an inductor or a current source, whose current must always have a path to flow, has to be connected to the pole of the switch. Also, a capacitor or a voltage source, which should never be shorted, may not be connected between the pole and a terminal, [H9]. The
resulting elementary PWM cell with ideal switches is illustrated in Figure 2.10.b.

In reality, PWM switching cell is implemented using nonideal switches. Due to their finite switching speed, the requirement that the switch pole be always connected to only one terminal is violated, and the pole is either connected to two terminals, or left open for a short period of time.

Shorting of two terminals typically occurs when the PWM switch is implemented using a diode and a controlled semiconductor switch - a situation present in practically all PWM converters. When the diode is conducting and it needs to be turned off, the controlled switch is gated on. Due to the reverse recovery of the diode, the two PWM switch terminals are shorted for some time. This generates a large current spike through the devices, and creates a significant amount of EMI.

Opening of both terminals is common in bridge circuits, where the PWM switch is implemented using two controlled switches. When the pole is disconnected for a short time, the switch parasitic capacitances can prevent the switch voltage from rising to destructive levels too fast. Even so, the switch voltage stress can be significantly increased, and a fair amount of EMI generated.

Using the switch model of Figure 2.5, the elementary PWM switching cell with nonideal switches is defined as:
Figure 2.10. Elementary PWM converter: a) PWM switch, b) elementary PWM cell with ideal switches, and c) elementary PWM cell with nonideal switches.
Definition 2.7: An elementary PWM switching cell with nonideal switches is a network $N$ that satisfies the following conditions:

1. Network $N$ contains only the following elements:
   a. two dc voltage sources, $V_1$ and $V_2$, such that $V_1 \neq V_2$, and at least one of the sources is non-zero,
   b. a non-zero dc current source $I$, and
   c. two switches, $S_1$, and $S_2$.
2. The switches $S_1$ and $S_2$ and the current source $I$ form a cut set.
3. $S_1$ and $V_1$ form a cut set, $S_2$ and $V_2$ form a cut set, and $S_1$, $S_2$, $V_1$, and $V_2$ form a loop.
4. The graph $\Gamma$ of $N$ is connected.
5. The $C-V$ loop degeneration is satisfied.$^1$

The elementary PWM cell is shown in Figure 2.10.c. The conditions 1 through 4 describe the elementary PWM switch elements and their connections. They would remain unchanged even if ideal switches were used. Condition 5, however, is the result of the switches not being ideal. The capacitances of the switches $S_1$ and $S_2$ form a $C-V$ loop with $V_1$ and $V_2$. In this situation, condition 5 guarantees that there are no infinite currents in the elementary PWM cell. Further, it implies that no voltage sources should be used in series with any of the switches to achieve soft-switching, because this

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$^1$ The terminology used in conditions 1–4 is in accordance with definitions given in [H5]. Referring to Figure 2.10.c, the condition 5 implies that the initial switch voltages at $t = 0$ satisfy $v_{S_1}(0) + V_1 - v_{S_2}(0) - V_2 = 0.$
would produce currents of infinite magnitudes. In effect, this eliminates the possibility of using the circuit of Figure 2.9.e for obtaining soft switching.

C. ELEMENTARY SOFT-SWITCHING PWM CELL

To obtain the basic SSPWM cell, the two remaining circuits in Figure 2.9.c and d are used. If any one of the switches in the elementary PWM cell is replaced by the circuits of Figure 2.9.c or d, two elementary SSPWM switching cells are obtained. They are shown in Figure 2.11, with a set of possible waveforms of \( i_x \). These waveforms have been derived from the circuits in Examples 1 and 2, but in general any waveform that provides soft-switching conditions can be used. Both circuits have already been derived intuitively in the previous section. The ideal single-pole double-throw switch in the circuit of Figure 2.11.a signifies that current source \( i_x \) can be connected in parallel with either \( S_1 \) or \( S_2 \), depending on which switch is assisted. Because the auxiliary circuit is connected in parallel to the switch, in the further text this circuit will be referred to as the type P elementary SSPWM cell. The circuit in Figure 2.11.b contains only one current source \( i_x \) and requires no switching of terminals to \( i_x \). This is because \( i_{S2} = I - i_x \), so that the current of both switches can be controlled with \( i_x \) connected in series with one of the switches. Due to the series connection of \( i_x \) and \( S_1 \), the circuit in Figure 2.11.b will be referred to as the type S elementary SSPWM cell.
Figure 2.11. Elementary SSPWM cells: a) Type P, and b) type S.
It is, thus, concluded that all the existing SSPWM converters can be modeled by the two elementary SSPWM cells. As was mentioned before, type P elementary SSPWM cell models all ZVT and ZCT PWM converters in which the commutation circuit is connected in parallel with the power flow, while type S elementary SSPWM cell models the quasiresonant, multiresonant, resonant, and quasi-squarewave converters in which the commutation circuit is always in series with the power flow.

Based on the topology of the two SSPWM cells some general properties of SSPWM converters can be derived.

**Proposition 2.2:** Switches $S_1$ and $S_2$ in the elementary SSPWM cell cannot have soft-switching conditions simultaneously.

**Proof:**

**Case 1: Type P elementary SSPWM cell:** Suppose $S_1$ and $S_2$ in Figure 2.11.a have simultaneous soft-switching conditions. From the Kirchoff’s voltage law (KVL) we have $v_{S1} + V_1 - v_{S2} - V_2 = 0$. According to definition 2.1, during switching $v_{S1} = v_{S2} \equiv 0$ which implies $V_1 - V_2 = 0$. This contradicts the condition 1.a of definition 2.7.

**Case 2: Type S elementary SSPWM cell:** Again suppose that both switches in Figure 2.11.b have soft-switching conditions. As shown earlier, $v_{S1} = v_{S2} \equiv 0 \Rightarrow i_{S1} = i_{S2} \equiv 0$. From the Kirchoff’s current law (KCL) $i_{S1} + i_{S2} - l = 0$. This gives $l \equiv 0$ which contradicts the condition 1.b of definition 2.7. □
This proposition leads to the following conclusions known from practice. If both switches should be switched under soft-switching conditions, there will be times during switching when either both switches are off or both switches are on. To avoid large switch voltage stress in the case when both switches are off, the auxiliary circuit should provide an alternative path for the current $I$. All circuits with this property will be type P SSPWM converters. To avoid large switch current stress when both switches are on, the auxiliary circuit should provide an alternative voltage blocking element. All circuits with this property will be type S SSPWM converters.

In many practical cases it is, however, not required to have soft-switching conditions for both switches simultaneously. So the following question can be asked: Should the switches $S_1$ and $S_2$ still be switched simultaneously even if only one switch needs to have soft-switching conditions? To answer this question consider the case of type P SSPWM cell in which $S_1$ should be turned off with soft-switching. Assume that both switches are switched simultaneously. During switching we require $v_{S1} \equiv 0$, and $v_{S2} \not\equiv 0$. This situation clearly does not violate any of the conditions in definition 2.7. It can, however, be seen that $S_2$ is turning on with a large voltage $v_{S2} = V_1 - V_2$, which will result in very large current through $S_2$. Therefore it is not recommended to switch both switches simultaneously, even if one of them does not require soft-switching. It can be shown using similar arguments that in all the remaining cases simultaneous switching causes either large current or large voltage stresses of the switches.
As a conclusion, if it is desired to provide soft-switching to either one of the switches $S_1$ or $S_2$ or to both of them, a switching dead-time or overlap time should be introduced. During the dead-time or overlap time, the auxiliary circuit must provide alternative current path or voltage blocking element, respectively.

2.3 Extension to DC-DC Bridge Topologies

Bridge converters are widely used in both dc-dc and dc-ac power conversion, while three-phase power converters are almost exclusively of bridge-type. It is, therefore, important to study the ways of obtaining soft-switching in bridge converters.

DC-DC bridge converters are either of half- or full-bridge type. We choose not to consider the half-bridge converters for two reasons. First, all three-phase circuits considered in the later parts of the dissertation are full-bridge circuits. Second, in general, all half bridge converters can be modelled by using the elementary PWM cells of Figure 2.10.c, so that all results related to soft-switching derived so far can be directly applied to half-bridge converters. In the further text, the term 'bridge' is used instead of the term 'full-bridge.'

The main feature of bridge topologies is that they can create and process voltages and currents of both polarities. There are two types of bridge converters: nonisolated and isolated. Nonisolated bridge converters are used in
applications where conversion of dc and low-frequency (frequency much lower than the switching frequency) ac currents and voltages is required. Isolated bridge converters are used almost exclusively in dc-dc conversion applications where isolation is required. The bridge is used to create high-frequency, purely ac voltages and currents which are passed through the isolation transformer, rectified, and filtered. The operation of nonisolated and isolated bridge converters is significantly different so that the issues related to obtaining soft-switching for the two bridge types are studied separately.

2.3.1 Nonisolated DC-DC Bridge Topologies

A nonisolated dc-dc bridge converter consists of two single-pole, double-throw switches sharing the same current source in their poles and the same voltage source between their terminals, as shown in Figure 2.12.a. The bridge is always implemented using four semiconductor switches, as shown in Figure 2.12.b. The two nonideal elementary PWM cells with only one voltage and one current source can clearly be distinguished.

Soft-switching converters can be obtained if the elementary PWM cells are replaced by elementary SSPWM cells. Several different soft-switching bridge converters can be obtained by using combinations of type P and type S cells. However, only the simplest possible case, in which the two PWM cells are modified with the same type of soft-switching circuitry, is considered here. There are two soft-switching bridge topologies with this property, and they are
Figure 2.12. Nonisolated bridge topologies: a) With ideal switches, and b) with nonideal switches.
shown in Figure 2.13.a and b. These topologies are obtained from the type P and type S elementary SSPWM cells in Figure 2.11.a and b, with with one of the voltage sources equal to zero.

Each of the two general soft-switching bridge topologies uses two auxiliary circuits to achieve soft switching. It would be beneficial if the commutation circuits could be simplified. In general, all switches in the bridge can be commutated at any given time. If the PWM modulation scheme is such that both single-pole double-throw switches are commutated at the same time, then the commutation circuitry cannot be simplified. In many cases, however, the two switches are never commutated simultaneously.

Consider, for example, the case of the bridge with type P cells in which \( l \) needs to be commutated from \( S_{ap} \) to \( S_{an} \) with the assistance of \( i_{xa} \) and \( S_{xa} \). During this operation, \( S_{bp}, S_{bn}, S_{xb} \), and \( i_{kb} \) are inactive. Therefore, some of the functions of \( S_{xa} \) can be performed by \( S_{bp} \) and \( S_{bn} \) if \( i_{xa} \) is connected to node b. In a similar way, \( S_{xb} \) can be eliminated during the commutation of \( S_{bp} \) and \( S_{bn} \). This results in a simplified circuit shown in Figure 2.13.c. The single source \( i_x \) provides soft-switching conditions for all bridge switches.

The bridge with type S cells can be simplified in the following way. If, for example, \( l \) needs to be commutated from \( S_{ap} \) to \( S_{an} \), while \( S_{bp} \) is on and \( S_{bn} \) is off, \( i_{xb} \) is inactive, e.g. \( i_{xb} = l \), and can be removed from the circuit without affecting its operation. If \( i_{xa} \) is moved in series with \( V \), soft-switching conditions for \( S_{ap} \) and \( S_{an} \) can still be achieved because \( i_{sap} = l - i_{xa} \). In a similar way, the source \( i_{xb} \) can be moved in series with \( V \). This results in the simplified circuit
Figure 2.13. **Soft-switching bridge topologies:** a) General soft-switching topology with type P cells, b) general soft-switching topology with type S cells, c) simplified type P topology, and d) simplified type S topology.
shown in Figure 2.13.d. The single source $i_x$ provides soft-switching conditions for all bridge switches.

In practice, the implementation of soft-switching in bridge circuits can be very simple due to the fact that voltages and currents of both polarities can easily be generated. To illustrate this, consider the implementation of the bridge converter of Figure 2.12.c, shown in Figure 2.14.a. The bridge converter is implemented with four MOSFETs, $S_{ap}$ through $S_{bn}$. The diodes $D_{ap}$ through $D_{bn}$ are the MOSFET body diodes. The commutation circuit is implemented using only one switch and an inductor.

Assume that before the commutation all switches are off, and $I$ flows through $D_{ap}$ and $D_{bn}$. The goal is to commutate the current from $D_{ap}$ to $S_{an}$. The circuit operation during the commutation is very similar to the operation of the soft-switching dc-dc converter example presented in the previous chapter. The function of the single-pole double-throw switch $S_x$ in Figure 2.4.a is taken over by $S_{bp}$ and $D_{bn}$.

**Charging Phase.** At the beginning of commutation, the auxiliary switch $S_x$ is closed, starting the charging phase of the commutation circuit. The current through inductor $L_x$, starts to increase from zero, gradually diverting the current form the diodes $D_{ap}$ and $D_{bn}$ to the commutation circuit. After some time, $i_x$ reaches the inductor current, $I$, and both diodes block.

**Resonant and Clamping Phase.** After $D_{ap}$ and $D_{bn}$ have blocked, a resonance between the inductor $L_x$ and the parasitic capacitances of nodes $a$ and $b$ starts. This swings the voltages of these nodes between the rails, reducing
Figure 2.14. Example of a nonisolated dc-dc ZVS bridge converter.
the voltages across $S_{an}$ and $S_{bp}$ in a resonant fashion. When $v_{an}$ and $v_{pb}$ become zero, diodes $D_{an}$ and $D_{bp}$ start conducting, clamping the switch voltages to zero. At this time, $S_{an}$ and $S_{bp}$ are turned on with no losses.

**Discharging Phase.** At this point, the voltage across $L_x$ has reversed, and as a result, $i_x$ gradually reduces to zero. This gradually increases the currents of $S_{an}$ and $S_{bp}$. Eventually, the entire current $I$ is transferred to the switches, when $S_x$ is turned off, and the commutation circuit becomes inactive. Finally, $S_{bp}$ is turned off, and the current $I$ is transferred to $D_{bn}$, completing the desired commutation.

If $S_x$ is implemented as a bidirectional switch, the commutation circuit can be used in a similar way even if $I$ flows in the opposite direction. In this implementation, the switch $S_{bp}$ has been used to assist in the auxiliary circuit operation and commutation of node a. For this reason, the commutation circuit implementation is even simpler than in the single-ended dc-dc converter.

### 2.3.2 Isolated DC-DC Bridge Topologies

The presence of the high-frequency transformer, its leakage inductance, and the diode rectifier in isolated bridge converters significantly influences the operation and achieving of soft switching. To analyze these influences, a simple transformer model is used. It is assumed that the transformer is an ideal transformer connected in series with an inductor. If this model is used, two bridge topologies with their secondary components reflected to the pri-
mary side exist: the voltage-fed and the current-fed isolated bridge converters, shown in Figure 2.15.a and b, respectively.

In the voltage-fed converter, the current source, $I$, is connected to the circuit through a diode rectifier bridge connected in series with the transformer leakage inductor, $L_{lk}$. Due to the presence of $L_{lk}$ the current $i_p$ can assume any value between $-I$ and $I$. In the cases when $i_p = I$ or $i_p = -I$, only two of the rectifier bridge diodes are conducting, and the source $I$ is reflected to the primary with a positive or negative sign, respectively. If $|i_p| \leq I$, however, all four rectifier diodes are conducting, shorting the current source. This situation leaves only the leakage inductance in the primary circuit. The three equivalent circuits connected between points $p$ and $n$ are shown in Figure 2.15.c. In normal bridge operation, all three topological states are periodically used in each switching cycle.

Similarly, in the current-fed converter, the output voltage source is connected to the primary through the diode bridge rectifier in series with $L_{lk}$. The three possible equivalent circuits of the network connected to points $p$ and $n$ are shown in Figure 2.15.d.

Using the principles for obtaining soft-switching already outlined in the previous sections, many soft-switching configurations can be created. Most of them would result in fairly complex and often impractical implementations. Emphasis here is given to two simple converter topologies that take advantage of the additional third topological stage and presence of the transformer leakage inductance to implement soft switching.
Figure 2.15. Isolated dc-dc bridge converters: a) Voltage-fed converter, b) current-fed converter, c) and d) equivalent circuits of networks connected between points a and b.
To illustrate this, the mechanism for obtaining soft switching in the ZVS full-bridge PWM converter, [D3]-[D7], shown in Figure 2.16, is described next. Consider the commutation at the instant $t_2$. Just before $t_2$, MOSFETs $S_{ap}$ and $S_{an}$ are on, and the primary current $i_p$, which is equal to the reflected output inductor current $i$, is flowing through $D_{ap}$ and $S_{an}$. The objective is to commutate the current from $S_{an}$ to $S_{bn}$. To accomplish this, $S_{an}$ is turned off at $t_2$. $i_p$ starts charging the parasitic capacitance of $S_{an}$ and discharging the capacitance of $S_{bn}$. This leads to increase of $v_{pn}$, and slight increase of $i_p$, so that $i_p > -i$. Because of this all four rectifiers start conducting, shorting the transformer secondary. This initiates a resonance between $L_{nk}$ and the capacitance of node $n$, further increasing $v_{pn}$ in a resonant fashion. When $v_{pn}$ reaches $V$, $D_{bn}$ starts conducting, clamping the voltage across $S_{bn}$ to zero. At that time $S_{bn}$ can be turned on with no losses.

The implementation of soft switching is extremely simple in this converter for the following three reasons:

- The primary currents are ac and the switching sequence is such that the primary current always discharges the capacitance of the switch that should be turned on next.
- All switches in the primary consist of antiparallel connection of a MOSFET and a diode. This provides a voltage clamping capability.
- The switch currents during commutation are shaped by the transformer leakage inductance. It serves as an energy storage element that prevents rapid current change. For achieving soft switching, the current must flow
Figure 2.16. Zero-voltage switched full-bridge PWM dc-dc converter.
in the proper direction during the entire commutation process. If in the above example the value of $L_{ik}$ would be too small, $i_p$ could reach zero before $v_{pn}$ reaches $V$ so that ZVS turn-on of $S_{bn}$ could not be achieved.

During this commutation, the transformer leakage inductance takes the role of the commutation current source, so that the converter could be modeled during this process by the circuit shown in Figure 2.17.a.

In the current-fed converter of Figure 2.15.b, the transformer leakage inductance can be used in the following way to achieve soft switching. It is seen that whenever the points $p$ and $n$ are shorted, either through $S_{an}$ and $S_{an}$, or through $S_{bp}$ and $S_{bn}$, the reflected secondary voltage, $V$, forces $i_p$ to zero. This mechanism is used to achieve ZCS for the bridge switches. The operation and an implementation of this converter have been described in [D8]. The equivalent model of this circuit is shown in Figure 2.17.b.

### 2.4 Extension to Three-Phase PWM Converters

Three-phase converters are much more complex than dc-dc converters. They contain more switches and operate with ac currents and voltages. The implementation of soft-switching is not a simple or obvious matter. This section presents two methods for applying the results derived so far to generation of three-phase soft-switching PWM converters.
Figure 2.17. Equivalent circuits of isolated bridge PWM dc-dc converters during soft commutation: a) Voltage-fed converter, and b) current-fed converter.
2.4.1 The Analysis-Synthesis Method

Three-phase converters represent a special class of converters with high level of circular symmetry, [H6]. Based on this symmetry, both the analysis and synthesis of the converters can be greatly simplified, [H9]. The symmetry of three-phase converter topology is a function of the circular symmetry of the three-phase converter terminal waveforms. The decomposition of the three-phase converter into its symmetrical subcircuits can be illustrated on the following example. Consider the boost rectifier, shown in Figure 2.18.a. It is assumed that the three phase currents, $i_a$, $i_b$, and $i_c$, are sinusoidal and in phase with their respective three phase voltages, $v_A$, $v_B$, and $v_C$. The three currents are shown in Figure 2.18.b. In each 60° interval marked in the current graph, none of the currents changes sign. Each of the intervals is marked by two sets of letters. The set of three letters, $(\alpha \beta \gamma)$, denotes the sequence of three phase currents in the following order:

$\alpha$: the current that does not have a zero value in the interval,

$\beta$: the current that is zero at the end of the interval, and

$\gamma$: the current that is zero at the beginning of the interval.

The set of two letters, $(s_{\alpha} s_{\beta \gamma})$ denotes signs of the phase currents in the following order:

$s_{\alpha}$: the sign of $\alpha$, and

$s_{\beta \gamma}$: the sign of $\beta$ and $\gamma$, 

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Figure 2.18. Three-phase boost rectifier: a) Converter topology, and b) phase currents.
where 'p' is used for 'positive,' and 'n' for 'negative.' It can be seen that both sets of numbers exhibit circular symmetry in the three-phase sequence.

The converter switches have to be operated so that none of the current source or inductor currents are interrupted, and none of the voltage sources and capacitors are shorted. Due to these constraints, in each 60° interval some switches and diodes are active, while others are either on or off during the entire 60° interval. For this reason the three-phase converter can be reduced to six active subtopologies each corresponding to a particular 60° interval of the three-phase current or voltage. The six active subtopologies of the boost rectifier corresponding to the six 60° intervals marked in Figure 2.18.b are shown in Figure 2.19. The arrows in the phase connections denote the actual phase current directions in each particular subtopology.

Each of the three-phase converter subtopologies can in fact be treated as a dc-dc converter. This is the case because in each subtopology, none of the three-phase variables changes sign. In addition to that, the converter switching frequency is always much higher than the frequency of the three-phase variables, so that they, in each subtopology, can be treated as slowly varying dc currents and voltages. With the three-phase converter decomposed in this way, we are in a position to implement soft switching in each of the subtopologies using the results derived in the earlier part of the chapter, and then synthesize the soft-switching three-phase converters from the soft-switching subcircuits.
Figure 2.19. Circularly symmetric active subtopologies of the three-phase boost rectifier.
Continuing the example of the boost rectifier, the six subtopologies of Figure 2.19 are examined more closely. It can be seen that each subtopology actually represents three single-ended dc-dc boost converters operating in parallel. For each one of them, soft-switching can be implemented in a way similar to that used in the example of Figure 2.2. This procedure can be repeated for all six PWM subtopologies resulting in six soft-switching PWM topologies shown in Figure 2.20. Notice that this is not the only possible soft-switching circuit implementation, and that all general results derived at the beginning of this chapter can directly be applied here.

It remains now to synthesize the soft-switching three-phase converter from the soft-switching subtopologies. All circuit components appear in more than one subtopologies, which means that the synthesis process has to involve the elimination of redundancy. The elimination of redundancy is self-evident in the case of the PWM converter if the analysis is performed 'backwards,' because no new branches and nodes are added to the circuit. The problem, however, arises if the synthesis has to be performed from the subcircuits that have new nodes and branches.

To address this problem, notice that the subtopologies come in pairs of complementary circuits. In complementary circuits, the signs of all three-phase variables are opposite, i.e. the two subtopologies correspond to the two points on the three-phase variable graph separated by exactly 180°. In the above example, the subtopologies \((\alpha \beta \gamma) (p \, n)\) and \((\alpha \beta \gamma) (n \, p)\) are complementary. Consider the example of the complementary topologies \((abc)(pn)\) and
Figure 2.20. Circularly symmetric soft-switching subtopologies of the three-phase boost rectifier.
(abc)(np), shown in Figure 2.21.a and b. If the same nodes of the two
topologies are connected, the resulting circuit is shown in Figure 2.21.c. The
circuit of Figure 2.21.c can also be obtained by merging any of the other
complementary subtopologies.

The question is now: can the three-phase topology resulting from merging
of the six soft-switching subcircuits be simplified? This problem is equivalent
to the problem of finding a three-phase topology with reduced number of
components that can be decomposed to the same set of subcircuits as the or-
iginal converter. In the case of the three-phase boost converter example, the
solution is shown in Figure 2.22. It is easily checked that both circuits reduce
to the same set of 60° subtopologies.

In general, the analysis-synthesis method consists of the following four
steps:

1. Identify the 60° dc-dc converter subtopologies.
2. Implement soft-switching for each of the subtopologies. This is done either
   based on an existing soft-switching technique for dc-dc converters, or
   based on the elementary SSPWM cells derived earlier.
3. Merge the common nodes and branches of the six soft-switching
   subtopologies, and eliminate trivial redundancies.
4. (Optional) simplify the soft-switching circuitry by finding a converter with
   reduced number of components that can be decomposed to the same set
   of subtopologies as the original soft-switching converter.
Figure 2.21. Merging of complementary subtopologies: a) and b) two complementary subtopologies, c) merged subtopology with redundancy, and c) merged subtopology with eliminated redundancy.
Figure 2.22. The final three-phase soft-switching boost rectifier.
The synthesis procedure presented above can become quite involved if the original three-phase converter is complex, such as the matrix converter, [A5], which decomposes into 36 subtopologies. In addition, the resulting soft-switching implementation may not be the optimal one in terms of component number, component voltage and current stress, etc. The direct synthesis procedure presented next is less systematic and more intuitive, but could sometimes lead to better results.

2.4.2 The Direct Synthesis Method

The direct synthesis method consists of the following four steps:

1. Identify elementary PWM cells in the three-phase converter.
2. Replace the elementary PWM cells with one of the elementary SSPWM cells of Figure 2.11.
3. Determine the appropriate implementation of sources $i_x$ and switches $S_x$ if used.
4. (Optional) simplify the soft-switching circuitry based on synchronization of the main switches.

To illustrate the application of this method, it is shown how the soft-switching boost rectifier of Figure 2.22 is derived using this method. Consider again the three-phase boost rectifier / VSI shown in Figure 2.23.a. Upon
closer examination of the converter, it is seen that its semiconductor switches constitute three elementary PWM cells consisting of three single-pole, double-throw switches sharing the same voltage source between their terminals, as shown in Figure 2.23.b. If every elementary PWM cell is replaced by a type P elementary SSPWM cell, a soft-switching converter is obtained as shown in Figure 2.23.c. The final two synthesis steps are to determine the appropriate implementation of sources \( i_{xa} \), \( i_{xb} \), and \( i_{xc} \), and possibly to simplify the converter implementation. Both of these steps are intuitive, and as will be shown in the next chapter, can result in different commutation network implementations. In this example, it is clear that the commutation networks can be implemented so as to obtain the ZVT converter of Figure 2.22. Being an intuitive step, the simplification of the soft-switching circuitry can be achieved in different ways. In the next chapter, it is shown how the converter of Figure 2.22 can be simplified by synchronization of the main bridge switches, and by transferring some of the functions of \( S_{xa} \), \( S_{xb} \), and \( S_{xc} \) to the main bridge switches in a way similar to that used to simplify the nonisolated dc-dc bridge converters of Figure 2.13.
Figure 2.23. Example of the direct synthesis method: a) The three-phase boost rectifier/VSI, b) equivalent circuit of the three-phase boost rectifier/VSI, and c) soft-switching three-phase boost rectifier/VSI with type P sells.
2.5 Conclusions

The results of this chapter are based on the following two conclusions:

1. the ideal switching condition for both switch turn-on and turn-off is that of having the switch voltage equal to zero during switching, and
2. soft switching can be obtained in PWM converters only by adding a commutation circuit, which can be modeled as a controlled current source.

Using this, two elementary SSPWM dc-dc converter representations were derived:

1. Converters with soft-switching commutation circuit in series with power flow, and
2. Converters with soft-switching commutation circuit in parallel with power flow.

The two elementary SSPWM cells have the following properties:

1. Converter switches cannot have soft-switching conditions simultaneously.
2. If it is desired to provide soft-switching to either one of the converter switches or to both of them, a switching dead-time or overlap time should be introduced. During the dead-time or overlap time, the commutation
circuit must provide alternative current path or voltage blocking element, respectively.

3. In order to obtain soft-switching conditions some means of switch voltage clamping must be provided.

Based on the generalized SSPWM converter representations and common topological properties of three-phase and dc-dc PWM converters, two procedures for synthesis of three-phase soft-switching PWM converters were derived. These procedures set a groundwork for synthesis of several new soft-switching three-phase PWM converters presented in the following chapters.
3.0 Nonisolated Three-Phase Soft-Switching PWM Converters

3.1 Introduction

Based on the results derived in the previous chapter, three new three-phase zero-voltage transition PWM converters are presented: a boost rectifier and voltage source inverter, a three-level boost rectifier, and a buck rectifier. Due to the relative complexity of the commutation circuits, all the converters are derived using the direct synthesis method.
3.2 Three-Phase Zero-Voltage Transition Boost Rectifier

/ Voltage Source Inverter

The three-phase ZVT boost rectifier/VSI presented here is derived from the ZVT converter of Figure 2.22 by simplification of the commutation circuit. The ZVT converter derived at the end of the previous chapter, using both analysis-synthesis and direct synthesis methods, is redrawn and shown in Figure 3.1.a. The possible waveforms of $i_{xa}$, $i_{xb}$, and $i_{xc}$, with converter phase currents as shown in the 60° shaded area in Figure 2.18.b, are shown in Figure 3.1.b. Closer examination of these waveforms, together with the commutation circuit topology, reveals that each leg of the commutation circuit bridge with its inductor operates as a single-phase boost rectifier running in the discontinuous current conduction mode (dcm). If the actions of the three legs are synchronized, i.e. if the turn-ons of switches in the three main converter legs are simultaneous, the three single-phase boost rectifiers can be implemented as a single three-phase rectifier running in dcm [A9], as shown in Figure 3.2.a. The currents $i_{xa}$, $i_{xb}$, and $i_{xc}$ maintain the same shape as in the three single-phase implementations, while the commutation network is actually implemented using only one controlled switch and a three-phase diode rectifier bridge. The addition of the diodes $D_{xp}$, $D_{xn}$, $D_{zp}$, and $D_{zn}$ is required to maintain the commutation circuit inactive while $S_x$ is off. The function of the all the
Figure 3.1. Three-phase ZVT converter with three independent commutation circuits: a) Converter schematics, and b) commutation circuit currents.
Figure 3.2. Three-phase ZVT boost rectifier/VSI: a) Converter schematic, and b) commutation circuit currents.
commutation circuit components will become clear in the following description of operation.

3.2.1 Rectifier Mode of Operation

In the following discussion of the rectifier mode of operation, it is assumed that there is no phase shift between the converter input currents and voltages. Consider the case when the input phase voltage and currents are within the $60^\circ$ interval shaded in Figure 2.18. Then in Figure 3.2, the voltage $v_A$ is positive, and $v_B$ and $v_C$ are negative, and the input phase current $i_a$ is positive, and $i_b$ and $i_c$ are negative. According to the six-step PWM algorithm, during the entire $60^\circ$ interval switch $S_{ap}$ is on, $S_{an}$ is off, and the remaining four switches are pulse-width modulated as was illustrated in Figure 2.19.a. Assume that switches $S_{ap}$, $S_{bn}$, and $S_{cn}$ are closed, while the currents are flowing through $D_{ap}$, $D_{bn}$, and $D_{cn}$. The goal is to commutate currents $i_b$ and $i_c$ from diodes $D_{bn}$ and $D_{cn}$ to switches $S_{bp}$ and $S_{cp}$, while achieving ZVS for all the switches and diodes involved in the transition.

Figure 3.3 shows the converter waveforms during a high-frequency switching period in the rectifier mode of operation. Figure 3.4 shows the corresponding equivalent topological states of the commutation circuit as they change through the switching period. The current sources represent input inductor currents which are considered constant during the switching period. The arrows in Figure 3.4 mark the actual current directions, rather than the
Figure 3.3. High-frequency waveforms in rectifier mode of operation.
Figure 3.4. Topological states of the commutation circuit: a) Charging phase, b) resonant phase, c) and d) discharging phase.
current reference directions as in Figure 3.2. The commutation action in this mode is very similar to that presented in the nonisolated dc-dc ZVT converter example in Chapter 2.

**Charging Phase.** At the beginning of the commutation, the auxiliary switch $S_x$ is closed, starting the charging phase of the commutation circuit. During this phase the circuit from Figure 3.2 is in the topological state shown in Figure 3.4.a. The currents through inductances $L_{xa}$, $L_{xb}$, and $L_{xc}$ start to increase from zero, gradually diverting the currents from $D_{ap}$, $D_{bn}$ and $D_{cn}$ to the commutation circuit. After some time, the currents of the auxiliary inductors exceed the respective input phase currents. At that point, all the main bridge diodes block, and their currents are commutated to their respective antiparallel switches. This arrangement eliminates the problems associated with the diode reverse recovery. The charging stage is continued until there is enough energy stored in the auxiliary inductors to charge/discharge the parasitic capacitances of nodes $a$, $b$, and $c$.

**Resonant and Clamping Phase.** After inductors $L_{xa}$, $L_{xb}$, and $L_{xc}$ have been charged, switches $S_{ap}$, $S_{bn}$, and $S_{cn}$ are opened, starting the resonant transition phase when the circuit is transferred to the topological state shown in Figure 3.4.b. The energy stored in the auxiliary inductors is used to charge the parasitic capacitances of nodes $a$, $b$ and $c$ in a resonant fashion, swinging the voltage of these points between the two dc rails. The voltage of node $a$ is clamped to the negative rail through $D_{an}$, while the voltages of nodes $b$ and $c$ are clamped to the positive rail through diodes $D_{bp}$ and $D_{cp}$, respectively. This
provides zero-voltage turn-on conditions for switches $S_{an}$, $S_{bp}$, and $S_{cp}$, and results in the reversal of voltages at the input of the commutation circuit, so the circuit is transferred into the state shown in Figure 3.4.c.

**Discharging Phase.** The turn-on of $S_{an}$, $S_{bp}$, and $S_{cp}$ initiates the commutation circuit discharging phase, in which the energy stored in the auxiliary inductors is returned to the dc side. Due to different initial currents in $L_{xa}$, $L_{xb}$, and $L_{xc}$ at the beginning of the discharging phase, the energy stored in the auxiliary inductors cannot be completely returned to the dc side. Therefore, when current $i_{xa}$ reaches zero, the auxiliary switch $S_x$ is turned off, and the residual energy from the auxiliary inductors $L_{xb}$ and $L_{xc}$ is transferred to the output (Figure 3.4.d). After the commutation circuit is deactivated, the switch $S_{an}$ is turned off. Current $i_a$ causes the voltage of node $a$ to swing to the positive dc rail, so that switch $S_{ap}$ can be turned on under ZVS condition, thus completing the desired commutation of nodes $b$ and $c$.

**Commutation from the Switches.** The soft commutation from $S_{bp}$ and $S_{cp}$ to $S_{bn}$ and $S_{cn}$, respectively, takes place naturally, without the assistance of the commutation circuit. When switches $S_{bp}$ or $S_{cp}$ are turned off, the parasitic capacitances of nodes $b$ and $c$ are discharged by currents $i_b$ and $i_c$, respectively, providing ZVS turn-on conditions for $S_{bn}$ and $S_{cn}$.

The operations of the circuit are similar for all different combinations of line voltages and currents.
3.2.2 Inverter Mode of Operation

When the converter operates in the inverter mode, the six-step PWM remains the same, i.e. during the entire shaded 60° interval of the desired ac phase voltages shown in Figure 2.18.b, switch $S_{ap}$ is on, $S_{an}$ is off, and the remaining four switches are pulse-width modulated. However, the currents are now of the opposite directions. Figure 3.5 shows the converter waveforms during a high-frequency switching period, in the inverter mode of operation.

Assume now that $v_A$ is positive, and $v_B$ and $v_C$ are negative, and that $i_a$ is negative, and $i_b$ and $i_c$ are positive. The commutation circuit is needed to assist the transition of currents from $D_{bp}$ and $D_{cp}$ to $S_{br}$ and $S_{cn}$, respectively. In this mode of operation, however, when $D_{bp}$ and $D_{cp}$ are conducting, current $i_a$ is flowing through $S_{ap}$, and the voltage at the input of the commutation circuit is zero. Therefore, $S_{ap}$ is turned off and $i_a$ is transferred naturally to $D_{an}$. In this way, a voltage is created at the input of the commutation network. The events taking place in the remaining part of the commutation cycle are similar to those in the rectifier mode of operation. The difference from the rectifier mode of operation is that in the inverter mode, the commutation of node $a$ is used to charge, while in the rectifier mode it is used to discharge the commutation inductors. This results only in different timing sequences for switches $S_{ap}$ and $S_{an}$ for the two operation modes.

In order to make it possible to use the commutation circuit only once within every switching cycle, the switching sequence is arranged so that the
Figure 3.5. High-frequency waveforms in inverter mode of operation.
current commutations from the diodes always take place at the same time. This arrangement results in different placements of voltage pulses within the switching cycle in different modes of operation. Detailed description of switching sequences for all possible phase angles is provided in [E10].

3.2.3 Commutation Circuit Design

The commutation circuit design consists of choosing the commutation inductor values, determining the timing for the auxiliary switch control, and selecting the commutation circuit components. Figure 3.6 shows simulated commutation circuit currents, with definitions of characteristic current and timing values. These definitions are used in the following derivations.

The auxiliary inductor value, \( L_x \), is chosen so that the duration of the charging phase can be slightly longer than the reverse recovery time of the bridge diodes. Referring to Figure 3.6, and Figure 3.4.a, the charging phase duration, \( T_c \), is given by:

\[
T_c = \frac{3 L_x}{2 V_{pn}} I_c, \tag{3.1}
\]

where \( I_c \) is the peak charging current.

The choice of \( I_c \) involves a trade-off between commutation circuit size and commutation circuit control complexity. Current \( I_c \) has to exceed the input phase current by a fixed amount, so that sufficient energy may be stored in
Figure 3.6. Commutation inductor currents.
the commutation inductors at the beginning of the resonant phase. From (3.1) it follows that if \( I_c \) follows the phase current variation, \( T_c \) will be a function of the phase current. Control implementation with variable \( T_c \) can be rather complex and impractical. For that reason, both \( T_c \) and \( I_c \) may be kept constant at a value that provides soft node commutation at maximum load. At light loads, the commutation circuit, therefore, processes more energy than is required for achieving the soft commutation. A value of \( I_c \) that guarantees soft switching at full load is \( I_c = \sqrt{3} \, I_m \), where \( I_m \) is the maximum peak phase current. This value is determined from the condition that all commutation inductor currents have to exceed their respective phase currents at the end of the charging phase. The worst-case condition occurs with \( \theta = 30^\circ \), as shown in Figure 2.18.b.

The duration of the resonant phase, \( T_r \), can be estimated as:

\[
T_r = \pi \sqrt{L_x/C} ,
\]

(3.2)

where \( C \) is the capacitance of nodes \( a, b, \) or \( c \). The resonant current amplitude, \( I_r \), can be estimated from Figure 3.4.b, as:

\[
I_r = \frac{2 \, V_{pn}}{3 \, \sqrt{L_x/C}} .
\]

(3.3)

The peak switch current, \( I_x \), is thus:

\[
I_x = I_c + I_r = \sqrt{3} \, I_m + \frac{2 \, V_{pn}}{3 \, \sqrt{L_x/C}} .
\]

(3.4)
The discharging phase duration, $T_d$, is approximately equal to the charging phase duration, $T_c$. The total on-time, $T_x$ of $S_x$ is given by:

$$T_x = T_c + T_r + T_d = \frac{3 \sqrt{3} I_m L_x}{V_{pn}} + \pi \sqrt{L_x C}.$$  

(3.5)

So, the auxiliary switch is controlled by a constant-frequency, constant-duty cycle clock signal. The timing of the bridge switches (turn-on and turn-off delays) is fixed, and does not depend on line or load variations or on the mode of operation.

The average value of the auxiliary switch currents, $\overline{i}_x$, is:

$$\overline{i}_x = \frac{i_x T_x}{2T},$$  

(3.6)

where $T$ is the switching period. The average switch current can be designed to be less than 5% of the peak phase current. The commutation circuit bridge diode average current rating is one third of $\overline{i}_x$, while the current rating of $D_x$ is even smaller.

Since the auxiliary inductors operate in the discontinuous current mode, $S_x$ is switched on and off with virtually no current. The auxiliary switch and diodes have to be able to block the auxiliary voltage $V_x$. 

Nonisolated Three-Phase Soft-Switching PWM Converters
3.2.4 Commutation Circuit Implementation and Variation of Switching Sequence

The switching sequence in the above converter is such that the main switches are used for both charging and discharging of commutation inductors. This fact has two consequences. First, the number of switchings per switching cycle is increased compared to the standard PWM converter from four to twelve. Since all six switch turn-on actions are soft, there are no losses associated with the increased number of turn-ons. The turn-off action is, however, hard, and this may offset some of the efficiency benefits gained by the use of the ZVT commutation circuit. This is particularly true if the bridge devices are not MOSFETs but IGBTs, because their turn-off losses are significant. Experimental results have shown, however, that even with IGBTs, the efficiency gain compared to standard PWM converter is around 1.5 %, [E10].

Second, the power transferred to \( V_{pn} \) is small, typically less than 0.2\% of the total power, so the losses in \( D_{xp}, D_{xn}, D_{zp}, \) and \( D_{zn} \) are very small. In addition to that, \( S_x \) is turned off with no current, so its turn-off losses are also small. The two zener diodes are needed to make sure that there is no current in the commutation circuit when \( S_x \) is off. Their breakdown voltage should be around 5 V. The implementation with zener diodes was originally proposed by Mao in [E11] as an improvement of the original commutation circuit implementation in which the residual commutation energy was dissipated in a resistor.
If the converter is operated in the rectifier mode only, the switching sequence can be simplified. The energy stored in the commutation inductors can be returned to the dc side through the commutation circuit instead of through the main bridge. In this case, the number of main bridge switching actions per cycle can be reduced to 8. Node a is not commutated to reverse the voltage at the input of the commutation circuit. Instead, \( S_x \) is opened at the end of the resonant and clamping phase, and the inductors are discharged by \( V_{pn} \). This technique reduces the main bridge switching losses but increases both the commutation circuit conduction losses and the turn-off losses of \( S_x \). The technique cannot be used in the inverter mode of operation. If node a is not commutated at the beginning of the charging phase, the commutation circuit cannot be activated because the voltage at its input is zero.

3.2.5 Experimental Verification, [E10]

Figure 3.7 shows the schematic of the 10 kW converter used to test the proposed soft-switching technique. The main bridge is a 1200 V, 50 A, IGBT six-pack. The converter switching frequency is 30 kHz. Figure 3.8 shows the converter waveforms during ZVT commutation in the rectifier mode, under 30% load. Figure 3.9 shows the converter high-frequency waveforms in the inverter mode of operation, under 60% load. Very clean waveforms in both figures demonstrate that the ZVT operation successfully absorbed all the circuit parasitics, and as a result parasitic ringing is eliminated, EMI is signif-
Figure 3.7. 10 kW ZVT rectifier/inverter prototype.
Figure 3.8. ZVT converter high-frequency waveforms in rectifier mode, [E10].
Figure 3.9. ZVT converter high-frequency waveforms in inverter mode, [E10].
Figure 3.10. ZVT converter low-frequency waveforms in inverter mode, [E10].
Figure 3.11. Efficiency measurements of the ZVT PWM and hard-switched PWM converters, [E10].
icantly reduced, and converter efficiency is improved. Figure 3.10 shows the
low-frequency converter currents. It is seen that they are very clean and un-
distorted. The soft commutation introduces some distortion into the low-
frequency waveforms. The procedure for the elimination of this influence is
described in [E10]. Figure 3.11 shows the efficiency measurement of the ZVT
prototype as a function of the load, compared to the efficiency of the hard-
switched PWM converter. The ZVT operation results in approximately 1.5 %
improvement in efficiency in the entire operating range.

3.3 Three-Phase Three-Level Zero-Voltage Transition

Boost Rectifier

In this section, a ZVT three-level rectifier is derived from the three-level
PWM boost rectifier shown in Figure 3.12, [A13]. The converter employs a
three-phase diode bridge, $D_{ap} - D_{cn}$, and three four-quadrant switches (imple-
mented here using six two-quadrant switches $S_{ap} - S_{cn}$) to provide sinusoidal
input currents, unity power factor, and regulated output voltage. The main ad-
vantage of this circuit over the conventional three-phase boost rectifier is that
the required voltage rating of the switches is only one half of the output volt-
age $V_{pn}$.

One of several ways in which the converter can be controlled is using
space vector modulation (SVM), [A5]. SVM provides a possibility of synchro-
Figure 3.12. Three-level PWM boost rectifier.
nizing the switch operation, so that soft-switching conditions can be achieved for all three switches simultaneously. To illustrate this situation, consider, without loss of generality, the time period during which the input currents are \( i_a > 0, i_b \leq 0, \) and \( i_c \leq 0 \). Under these conditions, switches \( S_{an}, S_{bp}, \) and \( S_{cp} \) are kept on all the time. The active subcircuit during this 60° interval is shown in Figure 3.13.a. A possible sequence of switching state vectors (SSV) is: \((p, n, n)\)-(o, o, o)-(p, n, o), where for example \((p, n, o)\) means that node \( a \) is connected to node \( p \) through \( D_{sp} \), node \( b \) is connected to node \( n \) through \( D_{bn} \), and node \( c \) is connected to node \( o \) through \( S_{cn} \). During this time period, the circuit shown in Figure 3.13.a can be represented with three single-pole double-throw switches, as shown in Figure 3.13.b.

To provide ZVS turn-on for the switches and soft turn-off for the diodes assistance from a commutation network is required on the transition from SSV \((p, n, n)\), where three bridge diodes are conducting, to SSV \((o, o, o)\) where the three switches are conducting. This operation is similar to the commutation in the two-level boost converter (explained in the previous section) operating in the rectifier mode, so that the same commutation circuit implementation can be used. The three-level ZVT boost rectifier and the simulated converter waveforms during the high-frequency switching cycle are shown in Figure 3.14.a and b, respectively. The operation of the commutation circuit can be described as follows.

**Charging Phase.** At the beginning of commutation, the auxiliary switch \( S_x \) is closed, starting the charging phase of the commutation circuit. The currents
Figure 3.13. Sub-topology of the three-level PWM boost rectifier: a) Active subcircuit, and b) equivalent subcircuit.
Figure 3.14. Three-level ZVT PWM boost rectifier: a) Converter topology, and b) high-frequency waveforms.
through inductances $L_{xa}$, $L_{xb}$, and $L_{xc}$, and diodes $D_{xap}$, $D_{xbn}$, and $D_{xcn}$ start to increase from zero, gradually diverting the currents form $D_{ap}$, $D_{on}$, and $D_{cn}$ to the commutation circuit. After some time, the currents of the auxiliary inductors reach the respective input phase currents. At that point, the main bridge diodes block. Note that the instant at which this happens is different for each leg of the bridge. $D_{bn}$ will block first because $i_b$ is the phase current with the smallest magnitude. $D_{ap}$ and $D_{cn}$ will block simultaneously at a later time. The gradual decrease of currents through the diodes practically eliminates the problems associated with the diode reverse recovery.

Resonant and Clamping Phase. After the diodes in the main bridge block, resonances between the auxiliary inductors $L_{xa}$, $L_{xb}$, and $L_{xc}$ and parasitic capacitances of nodes $a$, $b$, and $c$, respectively, start swinging the voltages of the nodes to zero. The node voltages are clamped at zero through the anti-parallel diodes of switches $S_{ap}$, $S_{bn}$ and $S_{cn}$. This provides ZVS turn-on conditions for the switches. The auxiliary inductor currents remain constant as long as $S_x$ remains closed.

Discharging Phase. To discharge the auxiliary inductors, switch $S_x$ is opened. This leads to conduction of diodes $D_{px}$ and $D_{nx}$, and application of output voltage $V_{pn}/2$ across each of the auxiliary inductors. The inductor currents reduce linearly to zero, and the energy stored in them is returned to the output. After all the auxiliary inductors have been discharged, the commutation circuit remains inactive for the remaining part of the switching cycle.
The remaining two switching transitions are completed without the assistance of the commutation circuit, by opening switches $S_{ap}$, $S_{bn}$, and $S_{cn}$ at the appropriate times.

The operation of the commutation circuit in the three-level rectifier is very similar to the commutation circuit operation in the two-level converter operating in the rectifier mode. The main difference is in the fact that in the three-level converter there is no boosting of commutation inductor currents. The boosting action is not needed because the voltage swing amplitude during commutation of nodes $a$, $b$, and $c$ is $V_{pn}$, while the voltage swing required to achieve ZVS is only $V_{pn}/2$. Therefore, ZVS is maintained under any line and load conditions, and the commutation inductor current magnitudes are always only slightly higher than the phase currents. This is expected to result in flatter efficiency v.s. load current characteristic, and in less critical timing for the commutation switch control.

The operation of this converter has been verified through simulation. Figure 3.15 shows the circuit waveforms during commutation circuit operation. The circuit with parameters $V_{pn} = 700$ V and $L_{xa} = L_{xb} = L_{xc} = 30 \mu$H was simulated at an instant when $i_a = 10$ A, $i_b = -1$ A, and $i_c = -9$ A.
Figure 3.15. Three-level ZVT PWM boost rectifier simulated waveforms.
3.4 Three-Phase Zero-Voltage Transition Buck Rectifier

The hard-switched PWM buck converter using SVM (or six-stepped PWM) is described in [H9]. The converter contains two elementary PWM cells and consists of two single-pole, triple-throw switches sharing the same current source in their poles, as shown in Figure 3.16.a. The direct synthesis method is used here to create a soft-switching converter. If the two PWM cells are replaced by two type P elementary SSPWM cells, a soft-switching converter is obtained as shown in Figure 3.16.b. If \( i_{xp} \) and \( i_{xn} \) are implemented as two inductors, a ZVT converter similar to the ZVT boost rectifier/VSI is obtained, as shown in Figure 3.16.c. The commutation circuit can be simplified by synchronization of the main bridge switches and by transferring some of the functions of \( S_{xp} \) and \( S_{xn} \) to the main switches. The final simplified ZVT buck rectifier is shown in Figure 3.17.a. The implementation and operation of the commutation circuit are very similar to those in other ZVT converter examples, with one noticeable difference: the switches used in the three-phase buck rectifier are voltage bidirectional, while in all converters presented so far, the switches are current bidirectional. This difference is significant because the voltage clamping during switching, necessary for soft-switching, is much more difficult to achieve in a voltage-bidirectional switch than in the current-bidirectional switch.

To illustrate the circuit operation in a high-frequency switching cycle, consider a time interval in which the input voltages are \( v_a > 0 > v_b > v_c \). Under
Figure 3.16. Three-phase ZVT PWM buck rectifier synthesis: a) PWM rectifier equivalent circuit, b) buck rectifier with type P elementary SSPWM cells, and c) implementation of the ZVT rectifier.

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Figure 3.17. Simplified ZVT PWM buck rectifier. a) Converter schematic, and b) high-frequency circuit waveforms.
unity power factor, the input phase currents satisfy the same relationship. During this time interval, switch $S_{an}$ is on all the time. At the beginning of the switching cycle switches $S_{ap}$, $S_{an}$, and $S_{cp}$ are on. Current $I$ flows through $S_{an}$, $D_{an}$, $S_{ap}$, and $D_{ap}$, while diode $D_{cp}$ is blocked. Figure 3.17.b shows the converter waveforms during the high-frequency switching cycle.

**Charging Phase.** The charging phase begins with the opening of $S_{ap}$, and closing of $S_x$. Switch $S_{cp}$ starts conducting, making $v_{pn} = -v_{ac}$, the voltage of currently the largest magnitude. Current $i_x$ starts increasing, gradually diverting the currents from the bridge to the commutation circuit. After some time, $i_x$ reaches $I$, and the bridge diodes block. The gradual decrease of currents through the diodes practically eliminates the problems associated with their reverse recovery.

**Resonant Phase.** After the diodes in the bridge block, the resonance between the auxiliary inductor $L_x$ and the parasitic capacitances between nodes $p$ and $n$ swings voltage $v_{pn}$ from $-v_{ac}$ to $v_{ac}$. In the process, the voltages across $S_{ap}$, $S_{bn}$, and $S_{cn}$ are reduced to zero, and they are turned on with no loss. Switch $S_{cp}$ is turned off with zero current. The voltage swing of $v_{pn}$ during the resonance is independent of the load current, so that soft-switching conditions can be achieved under any load conditions.

**Discharging Phase.** With voltage $v_{pn}$ reversed, $i_x$ linearly reduces, and current starts gradually increasing through $S_{ap}$, $D_{ap}$, $D_{cn}$, and $S_{cn}$. When $i_x$ reaches zero, $D_x$, blocks making the commutation circuit inactive for the remaining part of the switching cycle. Switch $S_x$ can then be turned off under
zero-current condition. The remaining commutations are performed without the assistance of the auxiliary network by opening $S_{cn}$ and $S_{bn}$ at the appropriate times. $S_{cp}$ is closed again immediately before the beginning of the next commutation circuit intervention.

The series connections of the switches and diodes in this converter create some difficulties in obtaining soft-switching. Due to the nonlinear nature of the diode and switch capacitances, $v_{pn}$ could swing during the resonant phase to a level close to $3v_{ac}$, subjecting the devices to a high voltage stress. To prevent this possibility, linear capacitors with capacitances much higher than the device capacitances should be connected in parallel with each device. Further, since the voltage swing is divided between the diode and the switch, the capacitance across the diode should be significantly larger than the one across the switch. This difference guarantees that most of the voltage change occurs across the switch, so that soft-switching conditions for the switch can be achieved.

Figure 3.18 shows a simulation of circuit waveforms during a commutation assisted by the ZVT circuit. The circuit parameters are $L_x = 5 \mu H$, switch capacitance $C_{cs} = 250 \, pF$, and diode capacitance $C_d = 1 \, nF$. The simulation conditions are $I = 12 \, A$, $v_a = 193 \, V$, $v_b = -52 \, V$, and $v_c = -141 \, V$. It can be seen that the voltage across $S_{cn}$ does not reduce to zero.
Figure 3.18. Simulated ZVT PWM buck rectifier high-frequency waveforms.
3.5 Conclusions

By virtue of elimination of several sources of switching losses, stresses, and noises, the proposed high-frequency boost rectifier/VSI is considered to be a prime candidate for high performance, high power applications where bidirectional power flow capability is required. The converter is deemed superior to the RDCL converters, [C1]-[C8], because it does not increase the voltage stress on the devices, and uses standard PWM control. The proposed converter matches the performance of the ARCP converter, [E5], while it uses significantly fewer circuit components for the implementation of the soft switching, at the expense of increased current and switching stress in the commutation circuit.

The three-level three-phase ZVT boost rectifier is a good candidate for power factor correction applications in which the input voltage is high (380-480 Vrms line-to-line), or for applications in which the input voltage range is relatively wide. In such cases, the converter can operate efficiently with high output voltage (close to 1000 V) while using MOSFETs rated for only 500 V. In addition, the converter provides two regulated output voltages of $V_{pn}/2$. These two outputs can be used as inputs to two separate isolated dc-dc converters, each using switches rated for $V_{pn}/2$, thus allowing for lower cost and higher efficiency operation.

The practical value of the ZVT buck rectifier is, to say the least, question-able. The main purpose of introducing the circuit was to illustrate the difficul-
ties of implementing soft-switching in converters with voltage bidirectional switches, and the importance of providing proper means of switch voltage clamping during switching.
4.0 Isolated Three-Phase Soft-Switching PWM Converters

4.1 Introduction

Based on the results derived in the Chapter 2, two new isolated three-phase soft-switching PWM converters are presented: a ZVS buck rectifier, and a ZCS boost rectifier. Due to the relative simplicity of the proposed soft-switching mechanisms, the two converters are derived using the analysis-synthesis method.

The single-stage three-phase PWM rectifiers presented in this section offer the following distinct features:

- soft switching for all power semiconductor switches;
- tight output voltage regulation with fast transient response;
- unity input power factor;
- no low-frequency harmonics on either input or output; and
- transformer isolation.

In the conventional approach, the above discussed features are typically accomplished using a two-stage conversion process employing a hard-switched, three-phase PWM rectifier followed by a dc-dc converter. The first stage provides rectification and power factor correction, while the second stage provides transformer isolation and tight output voltage regulation.

4.2 Three-Phase Zero-Voltage Switching Buck Rectifier

4.2.1 Converter Synthesis and Principle of Operation

Figure 4.1.a shows the circuit diagram of the hard-switched isolated PWM buck rectifier, [A8], [A10]. The converter can be divided into several functional blocks. The cycloconverter bridge \((S_{ap} \text{ to } S_{cn})\) is used to synthesize the high-frequency ac voltage \(v_{pn}\) from the three-phase input voltages. The four-quadrant switches are implemented as shown in Figure 4.1.b, where \(\pi\) denotes the two-quadrant part of a switch \(S_{ij}\) in Figure 4.1.a which conducts current when \(i_p\) is positive, while \(v\) denotes the switch part which conducts current when \(i_p\) is negative. The unity input power factor is obtained by using...
Figure 4.1. **Hard-switched PWM isolated three-phase buck rectifier**: a) Power stage schematic, b) four-quadrant switch implementation, and c) input phase voltages.

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a modified six-step PWM technique, so that the primary voltage \( v_{pn} \) contains no dc component. The high-frequency ac signal is transferred through the high-frequency transformer to provide input/output isolation. The secondary ac signal is rectified and filtered to obtain the desired output dc voltage.

A. PWM CONVERTER ANALYSIS

Within any 60° interval between two successive zero crossings of input phase voltages, shown in Figure 4.1.c, there are two line voltages that do not change sign. For example, in the 60° shaded area in Figure 4.1.c, the line voltages \( v_{ab} = v_a - v_b \), and \( v_{ac} = v_a - v_c \) are positive, and they both attain their maximum in this interval. The circularly symmetric active subcircuit in this interval is shown in Figure 4.2.a. The converter is controlled as two full-bridge (FB) converter subtopologies, \( x \) and \( y \), operating alternately within the switching cycle. The two subtopologies for the interval \(-30° \leq \theta \leq 30°\) are shown in Figure 4.2.b and c. Figure 4.3 shows the circuit principal waveforms within the 60° interval, with excessively increased switching period \( T \), so that PWM details can be observed. Different parts of the waveforms in Figure 4.3 are shaded according to the subtopology that is used to generate them. At the beginning of every switching cycle subtopology \( y \) is used. Switches \( S_{ap\pi} \) and \( S_{cn\pi} \) are turned on creating a positive voltage pulse across points \( p \) and \( n \) and a current pulse flowing from phase \( a \) into phase \( c \). In order to keep the transformer flux balanced, a negative voltage pulse of the same duration is next
Figure 4.2. Active subtopologies in the -30 to 30 degree range: a) The six-switch active subtopology, and b) the two full-bridge dc-dc converter-like subtopologies.
Figure 4.3. Modified six-step PWM waveforms: a) Phase voltages, b) primary voltage, c) phase current $i_b$, and d) phase current $i_c$. 
generated across points \( p \) and \( n \) by turning on switches \( S_{an} \) and \( S_{cp} \). The two pulses are separated by a zero-volt interval whose duration is chosen (for the purpose of transformer flux balancing) so that the distance between the adjacent pulses may be even throughout the switching cycle. In the remaining part of the switching cycle, the subtopology \( x \) is used to create another two voltage pulses across points \( p \) and \( n \), and two current pulses flowing from phase \( a \) into phase \( b \). Assuming that the converter output current is constant, the phase currents are synthesized from current pulses of constant magnitude. If the average phase currents, \( (\bar{i}_a, \bar{i}_b, \bar{i}_c) \), are to be sinusoidal and in phase with the phase voltages, the duration of the current pulses created by subtopology \( x \) has to be proportional to the phase voltage \( v_b \), while the duration of the current pulses generated by subtopology \( y \) has to be proportional to \( v_c \). \([H9]\). If these conditions are satisfied, the current \( \bar{i}_a \) is also sinusoidal and in phase with \( v_a \) due to the three-phase system symmetry and due to the fact that \( i_a = -i_b -i_c \).

**B. SOFT-SWITCHING PWM CONVERTER SYNTHESIS**

Because within every 60° interval the three-phase converter is operated as a set of two full bridge dc-dc converters, ZVS can be implemented in the same way as in the ZVS-FB-PWM dc-dc converter, \([D3]-[D6]\). For example, in subtopology \( x \) during the 60° interval, the antiparallel diodes of switches \( S_{ap} \), \( S_{bn} \), \( S_{bp} \), and \( S_{an} \) are forward biased because \( v_a > v_b \), and therefore
Figure 4.4. Sub-topology x redrawn as a full-bridge dc-dc converter.
these switches can be kept on all the time. In this case, the subtopology can be redrawn, as shown in Figure 4.4. This circuit can be operated in the ZVS mode when the active switches shown in Figure 4.4 have 50% duty cycle and the gate pulses for one vertical leg are phase-shifted with respect to the gate pulses of the other leg, [D3]-[D6]. The only topological modification compared to the PWM converter is that an inductor is added in series with the transformer. One of the six active soft-switching subtopologies is shown in Figure 4.5.a. The three-phase converter synthesis is now trivial, because the series inductor appears in the same branch in all six subtopologies. The three-phase ZVS buck rectifier is shown in Figure 4.5.b.

The complete operation of the three-phase circuit during a high-frequency switching period is illustrated in Figure 4.6 and Figure 4.7. Figure 4.6 shows the transformer primary voltage, \( v_{pn} \), and current, \( i_p \), the rectified secondary voltage, \( v_s \), and the current of phase \( a, i_a \). The gate drive signals for all twelve two-quadrant switches are shown in Figure 4.7, with the same time scale. Figure 4.7.a illustrates the operation of subtopology \( y \), while Figure 4.7.b illustrates the operation of subtopology \( x \) (the gate signals for \( S_{apx} \) and \( S_{snv} \) are repeated for clarity). It is seen from Figure 4.6 and Figure 4.7 that the circuit waveforms and the gate signals of subtopology \( y \) during the interval \( t_1 \) to \( t_7 \), and of subtopology \( x \) during the interval \( t_7 \) to \( t_{13} \), are identical to those in the ZVS-FB-PWM dc-dc converter. Since the operation of the ZVS-FB-PWM converter is well known, [D3]-[D6], a detailed switching cycle description is omitted.
Figure 4.5. Soft-switching PWM isolated three-phase buck rectifier: a) 60° subtopology, and b) the complete converter schematic.
Figure 4.6. ZVS rectifier high-frequency circuit waveforms: Primary voltage and current (top), rectified secondary voltage (middle), and current of phase a (bottom).
Figure 4.7. Switch gate-drive waveforms during switching period in Figure 4.6: a) Sub-topology y gate signals, b) subtopology x gate signals, and c) remaining gate signals.
It follows from the above discussion that only six out of twelve two-
quadrant switches in the converter operate in any given 60° interval. The other
six switches should be turned on during the entire interval. However, in a 30°
subinterval, one of the input phase voltages has a value that lies between the
other two, so the switches in the leg connected to this input phase have to be
turned off when the subtopology corresponding to this phase is not used. For
$0 \leq \theta \leq 30^\circ$, voltage $v_b$ is between $v_a$ and $v_c$, and consequently switches $S_{bp\pi}$
and $S_{bn\pi}$ can be kept on during the whole interval, except when switches $S_{cp\pi}$
and $S_{cn\pi}$, respectively, are on, as shown in Figure 4.7.c. This is to prevent a
short circuit between phases $b$ and $c$ through the antiparallel diodes of $S_{bp\pi}$
or $S_{bn\pi}$. During this interval, switches $S_{bp\pi}$ and $S_{bn\pi}$ are not switched under
zero-voltage conditions. However, the resulting switching losses are very low
for three reasons. First, these switches are never switching the full line-to-line
voltage, but only the difference between $v_b$ and $v_c$ which varies from 0 to
$(\sqrt{3}/2) V_m$, where $V_m$ is the amplitude of the phase voltage. Second, each
switch is operated without ZVS only during one 30° interval, and the total
switching losses are proportional to $1/(12T)$ rather than to $1/T$. Finally, the
switches turn off with no current, so there are no turn-off losses.

4.2.2 Steady-State Analysis

As is known from the operation of the ZVS-FB-PWM converter, and as can
be seen in Figure 4.6, the duty cycles of the transformer primary voltage
pulses are always longer than the duty cycles of the corresponding secondary voltage pulses, due to the presence of the isolation transformer and its leakage inductance. The implications of this difference, together with other effects relevant to the circuit design, are analyzed in this section, and the results of the analysis are used as a basis for the design procedure presented in Appendix C.

The analysis performed here is based on the assumption that the input phase voltages are sinusoidal and balanced. It is also assumed (unless otherwise stated) that the forward voltage drop across the diodes and the MOSFETs is zero, and that the rectifier diode capacitances are equal to zero. In addition, the analysis is performed with the assumption that the output voltage $V_0$ is constant.

**A. ZVS RECTIFIER DUTY CYCLE ANALYSIS**

Referring to Figure 4.6, the duty cycle of the primary voltage $v_{pn}$ is defined as:

$$d(\theta) = d_x(\theta) + d_y(\theta),$$  \hspace{1cm} (4.1)

where $d_x(\theta)$ and $d_y(\theta)$ correspond to the sum of duty cycles of the two voltage pulses created by subtopologies $x$ and $y$, respectively. The four primary voltage pulses are arranged as two pairs of pulses with duty cycles $d_x(\theta)/2$ and $d_y(\theta)/2$ separated by four zero-volt intervals of equal duration marked in Fig-
ure 4.6 as $d_0/4$. Similarly, the duty cycle of the rectified secondary voltage is defined as:

$$d_s(\theta) = d_{sx}(\theta) + d_{sy}(\theta),$$  \hspace{1cm} (4.2)$$

where $d_{sx}(\theta)$, and $d_{sy}(\theta)$ are defined as:

$$d_{sx}(\theta) = d'_{sx}(\theta) + d''_{sx}(\theta),$$
$$d_{sy}(\theta) = d'_{sy}(\theta) + d''_{sy}(\theta).$$  \hspace{1cm} (4.3)$$

The total loss of duty cycle (difference between primary and secondary voltage duty cycles) is defined as:

$$\Delta d(\theta) = \Delta d_x(\theta) + \Delta d_y(\theta) = d(\theta) - d_s(\theta),$$  \hspace{1cm} (4.4)$$

where:

$$\Delta d_x(\theta) = \Delta d'_x(\theta) + \Delta d''_x(\theta),$$
$$\Delta d_y(\theta) = \Delta d'_y(\theta) + \Delta d''_y(\theta).$$  \hspace{1cm} (4.5)$$

To simplify the notation, the following derivation is performed, without loss of generality, assuming that $-30^\circ \leq \theta \leq 30^\circ$. The input phase voltages are given by:

$$v_a(\theta) = V_m \cos(\theta),$$
$$v_b(\theta) = V_m \cos(\theta - 2\pi/3),$$
$$v_c(\theta) = V_m \cos(\theta + 2\pi/3).$$  \hspace{1cm} (4.6)$$
Because the primary and secondary duty cycles are not the same, the output voltage is given by:

\[ V_o = n[d_{sx}(\theta) \cdot v_{ab}(\theta) + d_{sy} \cdot v_{ac}(\theta)] , \quad (4.7) \]

where \( n \) is the transformer turns ratio \( n = N_{sec}/N_{prim} \). If it is desired that the average output voltage not contain any low frequency harmonics, then the secondary duty cycles should be made proportional to the input phase voltages:

\[
\begin{align*}
   d_{sx}(\theta) &= -D_m \left( v_b(\theta) / V_m \right), \\
   d_{sy}(\theta) &= -D_m \left( v_c(\theta) / V_m \right),
\end{align*} \quad (4.8)
\]

where \( 0 \leq D_m < 1 \) is the modulation index. After substituting (4.6) and (4.8) into (4.7), and after elementary trigonometric transformations, it follows that the output voltage is constant, and given by:

\[ V_o = \frac{3}{2} n D_m V_m . \quad (4.9) \]

It can further be shown that the input phase currents are proportional to input phase voltages, and are given by:

\[
\begin{align*}
   i_b(\theta) &= -d_{sx}(\theta) \cdot n \cdot I + \varepsilon_x(\theta) , \\
   i_c(\theta) &= -d_{sy}(\theta) \cdot n \cdot I + \varepsilon_y(\theta) ,
\end{align*} \quad (4.10)
\]

where \( I = V_0/R \) is the load current, and the functions \( \varepsilon_x(\theta) \) and \( \varepsilon_y(\theta) \) represent the additional distortion of the input currents due to the presence of small tri-
angular parts $t_1$ to $t_2$, $t_4$ to $t_5$, etc. Worst case input current spectrum analysis has shown, [E2], that these functions are small. The input current fundamental is phase shifted with respect to the phase voltage by less than $2.5^\circ$, and that the total harmonic distortion (THD) is less than 2 % due to this effect.

C. FILTER INDUCTOR CURRENT RIPPLE

In order to design the output filter inductor, it is necessary to know at which phase angle $\theta$ of the input voltage the filter current ripple reaches its maximum.

The output filter current ripple is analyzed by evaluating (4.6), (4.3) and (4.8) at $\theta = 0$ and $\theta = \pi/6$. Figure 4.8 shows the secondary voltage and the corresponding output filter inductor current ripple for $\theta = 0$ and $\theta = \pi/6$, respectively. At $\theta = 0$, $v_s$ consists of four equal-amplitude voltage pulses evenly distributed within $T$ (since $v_{ab} = v_{ac}$ at $\theta = 0$). The duty cycle of each pulse is $D_m/4$ and its amplitude is $V_0/D_m$, which is typically only 10-20 % above the output voltage. In this case the filter inductor ripple is minimal. At $\theta = \pi/6$, $v_s$ consists only of two pulses, each having a duty cycle of $(\sqrt{3} D_m)/4$, and amplitude of $(2V_0)/(\sqrt{3} D_m)$. The duty cycle of the other pair of pulses is zero (since $v_b = 0$ at $\theta = \pi/6$), and three of the zero intervals merge into one after the second pulse, as shown in Figure 4.8.b. Assuming that the loss of duty cycle $\Delta d$ is relatively small, the maximum filter inductor current ripple is calculated from Figure 4.8.b as:
Figure 4.8. Output filter inductor current ripple: a) $\theta = 0$, and b) $\theta = \pi/6$. 
\[
\Delta I_{\max} = \frac{3}{4} \left( 1 - \frac{\sqrt{3}}{2} D_m \right) T \frac{V_o}{L} . \tag{4.11}
\]

**D. LOSS OF DUTY CYCLE**

The selection of the transformer turns ratio, \( n \), and the modulation index, \( D_m \), is directly related to the loss of duty cycle, which depends on the choice of the switching frequency, leakage inductance, and the ZVS range. This interdependence is evaluated next.

From (4.2), (4.4), and (4.8), the primary duty cycle is given by:

\[
d(\theta) = \Delta d(\theta) - D_m \left[ \frac{v_b(\theta)}{V_m} + \frac{v_c(\theta)}{V_m} \right], \tag{4.12}
\]

where \( \Delta d(\theta) \) can be estimated from Figure 4.6, by using definitions (4.4) and (4.5), and Figure 4.5, as:

\[
\Delta d_x(\theta) = \frac{l'_{dx}(\theta) + l''_{dx}(\theta)}{v_{ab}(\theta) T} L_{ik},
\]

\[
\Delta d_y(\theta) = \frac{l'_{dy}(\theta) + l''_{dy}(\theta)}{v_{ac}(\theta) T} L_{ik}. \tag{4.13}
\]

In order to satisfy the constraint \( d(\theta) \leq 1 \), it is necessary to find the angle \( \theta \) at which \( d(\theta) \) attains its maximum. It is shown in Appendix A that \( d(\theta) \) is maximum for \( \theta = 0 \) if \( \Delta d(0) \leq 0.25 \). In practice, the loss of duty cycle \( \Delta d(0) \) should be limited to around 0.1. Therefore, in all practical designs, the choice of
maximum duty cycle has to be made at $\theta = 0$. Assuming full utilization of duty cycle, it follows from (4.12) that:

$$d(0) = D_m + \Delta d(0) = 1.$$  \hspace{1cm} (4.14)

From Figure 4.6 and (4.8), at $\theta = 0$,

$$I'_{dx}(\theta) = I''_{dx}(\theta) = I'_{dy}(\theta) = I''_{dy}(\theta) = n(2I - \Delta I(0)).$$  \hspace{1cm} (4.15)

The filter inductor current ripple is estimated from Figure 4.8.a by taking into account (4.14) as:

$$\Delta I(0) = \Delta d(0) \frac{V_0}{L} \frac{T}{4}.$$  \hspace{1cm} (4.16)

Since $v_{ab}(0) = v_{ac}(0) = 3V_m/2$, it follows from (4.13)-(4.16) and (4.9) that the loss of duty cycle is given by:

$$\Delta d(0) = \frac{8D_m \frac{n^2 L_{ik}}{RT}}{1 + D_m \frac{n^2 L_{ik}}{L}}.$$  \hspace{1cm} (4.17)

Using (4.17) and (4.14), the designer can choose $\Delta D(\theta)$, which will finally lead to the choice of $L_{ik}$, $T$, and the ZVS range.
E. ZVS RANGE AND REQUIRED DEAD TIMES

Conditions for ZVS are not the same for all switching transitions. Referring to Figure 4.6, at the leading edge transitions of $v_{pn}$ ($t_1$, $t_4$, $t_7$, and $t_{10}$), the energy stored in the leakage inductance is utilized to charge the parasitic capacitances of nodes $p$ or $n$ in Figure 4.5. However, at the trailing edge transitions of $v_{pn}$ ($t_3$, $t_6$, $t_9$, and $t_{12}$), the leakage inductance is in series with the reflected output filter inductor. The combined energy stored in both the leakage inductance and the output filter inductor is utilized to charge the capacitances of nodes $p$ or $n$. Since the energy stored in the output filter inductor is significantly larger than the energy stored in the leakage inductance, the ZVS condition can be easily achieved at the trailing edges.

When the converter operates with light load, the ZVS property is lost because the energy stored in $L_{lk}$ becomes smaller than the energy required to charge the parasitic capacitances of nodes $p$ or $n$ to the input line voltage. Since the energy in the capacitances is proportional to the square of the input line voltage, the worst case for achieving ZVS will occur when the input line voltage is the highest, i.e., $v_{pn} = \sqrt{3} V_m$, which occurs at $\theta = \pi/6$. The energy needed to charge the capacitance of nodes $p$ or $n$ at $\theta = \pi/6$ is:

$$E_c = \frac{1}{2} \left( \sqrt{3} V_m \right)^2 C_{eq}, \quad (4.18)$$

where $C_{eq}$ is:
\[ C_{eq} = \frac{8 + 2 \sqrt{2}}{3} C_M + C_T. \]  

(4.19)

as shown in Appendix B. In (4.19), \( C_M \) is the output capacitance of the two-quadrant switch (MOSFET) at \( \sqrt{3} V_m \), and \( C_T \) is the parasitic capacitance of the transformer.

The minimum energy stored in the leakage inductance required for ZVS is:

\[ E_l = \frac{1}{2} L_{lk} I_{cr}^2. \]  

(4.20)

Equating \( E_c \) and \( E_l \), and solving for \( L_{lk} \), gives:

\[ L_{lk} = \frac{(\sqrt{3} V_m)^2}{I_{cr}^2} C_{eq}. \]  

(4.21)

Current \( I_{cr} \) is the primary current at the end of the off-time, (e.g. at time \( t_{13} \) in Figure 4.6). The minimum \( I_{cr} \) occurs at \( \theta = \pi/6 \) and from Figure 4.8.a is given by:

\[ |I_{cr}| = n \left( I - \frac{1}{2} \Delta I_{\text{max}} \right), \]  

(4.22)

where \( \Delta I_{\text{max}} \) is given by (4.11). The maximum input voltage amplitude and the minimum load current at which ZVS is lost (ZVS range) are related through (4.21) and (4.22) with \( L_{lk} \) and \( \Delta I_{\text{max}} \). In the design of the converter, \( L_{lk} \) and \( T \)
(which from (4.11) determines $\Delta l_{\text{max}}$) have to be adjusted to achieve the desired ZVS range.

In order to achieve ZVS, it is necessary to provide some dead-time between turning one switch off and turning the other on, [D6]. The optimum dead time is equal to one fourth of the resonant period between $L_{ik}$ and $C_{eq}$, and can be estimated as:

$$\tau = \frac{\pi}{2} \sqrt{\frac{L_{ik}}{C_{eq}}}.$$  \hspace{1cm} (4.23)

In practice, the dead time needs to be adjusted experimentally due to wide variation of the equivalent capacitance, and the approximation (4.23) gives only a fairly good initial estimate of $\tau$.

### 4.2.3 Experimental Verification

Operation and performance of the proposed converter are illustrated using a 2 kW, 100 kHz rectifier shown in Figure 4.9. The converter power stage design is described in detail in Appendix C.

Figure 4.10 shows the waveforms obtained from the prototype operating at full load. Figure 4.10.a shows one input phase voltage and the corresponding current in front of the input filter. The current is undistorted, and in phase with the voltage. Figure 4.10.b shows the expanded view of the primary voltage $v_{pn}$, and primary current $i_p$. Both primary voltage and currents are very
Circuit diagram of the 2kW, 100 kHz ZVS rectifier prototype.

Figure 4.9.
Figure 4.10. Experimental circuit waveforms at 2 kW.
Figure 4.11. Experimental circuit waveforms at 800 W.
Figure 4.12. Experimental circuit efficiency measurements.
clean, illustrating the ability of the circuit to absorb the parasitic capacitances of the switches and the leakage inductance of the transformer, and thus making the high-frequency operation possible. Figure 4.10.c shows the corresponding rectified secondary voltage. The action of the clamping circuit and RC snubbers is apparent in the leading edges of $v_s$. Figure 4.11 shows the primary voltage and current waveforms at the operating point where the ZVS property is lost. The waveforms are still very clean because the ZVS property is lost only partially, and because the primary current is less than half of the full load current. The abrupt drop of current that coincides with the trailing edges of $v_{pn}$ is caused by the discharging of the snubber capacitors across the rectifier diodes.

The efficiency measurement for different values of load current is shown in Figure 4.12. The efficiency curve peaks between 40% and 50% of the full load current. The position of the peak coincides with the point at which the ZVS property is lost. At that operating point, the conduction losses and the switching losses are small. As the load current is increased, the conduction losses rise, and the efficiency is reduced. At low load currents, the switching losses become larger, and residual losses are more significant, so the efficiency rapidly drops below $I = 5A$. 

Isolated Three-Phase Soft-Switching PWM Converters
4.3 Three-Phase Zero-Current Switching Boost Rectifier

4.3.1 Converter Synthesis and Principle of Operation

Figure 4.13.a shows the circuit diagram of the hard-switched isolated PWM boost rectifier. The converter can be divided into several functional blocks. The cycloconverter bridge (Sap to Sco) is used to synthesize the high-frequency ac current Ip from the three-phase input currents. The four-quadrant switches are implemented as shown in Figure 4.13.b, where the notation for the two-quadrant switches is the same as in the ZVS buck rectifier. The unity input power factor is obtained by using a modified six-step PWM technique, so that the primary current Ip contains no dc component. The high-frequency ac signal is transferred through the high-frequency transformer to provide input/output isolation. The secondary ac signal is rectified and filtered to obtain the desired dc output voltage.

A. PWM CONVERTER ANALYSIS

For the purpose of simplified explanation, it is assumed, without loss of generality, that the phase voltages and currents are sinusoidal and in phase, and that the output voltage is constant. Since in this converter the three-phase input variable is current, the circularly symmetric circuit subtopologies are
Figure 4.13. Hard-switched PWM isolated three-phase boost rectifier: a) Power stage schematic, b) four-quadrant switch implementation, and c) input phase currents.
determined by the 60° intervals of phase currents in which none of the currents change sign. For example, the circularly symmetric subcircuit which is active in the 60° shaded area in Figure 4.13.c, is shown in Figure 4.14.a. The six active switches in this converter are voltage two quadrant. Unlike in the case of the buck rectifier, the operation of this converter cannot be reduced to two H-bridge subtopologies operating alternately, because at least one switch has to conduct current in each leg at all times.

Figure 4.15 shows the circuit principal waveforms within the 60° interval, with excessively increased switching period T due to which PWM details can be observed. The following explanation is valid for 0° ≤ θ ≤ 30°. The circuit operation is similar in the interval −30° ≤ θ ≤ 0° except that the roles of phases b and c are interchanged. At the beginning of every switching cycle switches \( S_{ap\pi} \), \( S_{bp\pi} \) and \( S_{cn\pi} \) are turned on, creating a positive voltage pulse across points a and b, and a and c, and positive \( i_p \) current pulse of value \( i_p = i_a \). The duration of this pulse is proportional to \( v_{ab} \). Next, \( S_{bn\pi} \) is turned off and \( S_{bp\pi} \) is turned on to reduce \( v_{ab} \) to zero. The reflected output voltage is still applied between points a and c. Current \( i_p \) drops to \( i_p = -i_c \). The duration of the second current pulse is proportional to \( v_{bc} \). Finally, \( S_{cn\pi} \) is turned off and \( S_{cp\pi} \) is turned on to create \( v_{ab} = v_{ac} = 0 \) and \( i_p = 0 \). To begin the second half of the switching cycle, \( S_{ap\pi} \) is turned off and \( S_{an\pi} \) is turned on to create negative transformer primary current. The switching sequence in this half-cycle is identical to that in the first half-cycle with "n" and "p", and "π" and "ν" switches interchanging their roles.
Figure 4.14. Active subtopology in the -30 to 30 degree interval.
Figure 4.15. Modified six-step PWM waveforms: a) Phase currents, b) primary current, c) voltage $v_{ab}$, and d) voltage $v_{ac}$.
B. SOFT-SWITCHING PWM CONVERTER SYNTHESIS

Even though the three-phase boost converter cannot be operated as two dc-dc converter bridges, soft switching can still be obtained in a way identical to that used in the ZCS full-bridge PWM dc-dc converter, [D8]. The only topological modification compared to the PWM converter is that an inductor is added in series with the transformer, and a capacitor is added at the transformer secondary. One of the six active soft-switching subtopologies is shown in Figure 4.16.a. The three-phase converter synthesis is now trivial, because both the inductor and the capacitor appear in the same branches in all six subtopologies. The three-phase ZCS boost rectifier is shown in Figure 4.16.b.

The operation of the three-phase circuit during a high-frequency switching period is illustrated in Figure 4.17 which shows the transformer primary current, \(i_p\), the secondary voltage, \(v_s\), and the voltages between points \(a\) and \(b\), and \(a\) and \(c\). The mechanism for obtaining ZCS relies on the use of the transformer leakage inductance for control of primary current slopes during switching. There are two types of switching transitions. The transitions at \(t_2\), \(t_4\), \(t_6\), and \(t_{10}\) use the output voltage to shape the primary current. The transitions at \(t_6\) and \(t_{12}\) rely on the resonance between \(L_{ik}\) and \(C_r\) to shape the primary current. Switching transition is always initiated by closing both switches in one of the legs, and thus shorting the transformer primary. For example, at \(t_2\), \(S_{bly}\) is closed. The entire reflected output voltage is thus applied to \(L_{ik}\) and the primary current gradually reduces. Current \(i_b\) gradually commutates.
Figure 4.16. *Isolated soft-switching PWM three-phase boost rectifier:* a) $60^\circ$ subtopology, and b) the complete converter schematic.
Figure 4.17. ZCS rectifier high-frequency circuit waveforms: Primary current (top), secondary voltage (middle), and line voltages ab and ac (bottom two, respectively).
from $S_{bn\pi}$ to $S_{bp\nu}$. At $t_3$, the entire current $i_b$ flows through $S_{bp\nu}$ and the diode of $S_{bn\pi}$ blocks. At that time, the transistor in $S_{bn\pi}$ can be turned off with no losses.

The transition at $t_6$ is initiated by closing $S_{an\nu}$. Since the transformer current is zero, the rectifier diodes are blocked, and a resonance between $C_r$ and $L_{lk}$ takes place. Both the primary current and secondary voltage now change in a resonant fashion. The current $i_a$ gradually commutates from $S_{ap\pi}$ to $S_{an\nu}$. At $t_7$, the entire current $i_a$ flows through $S_{an\nu}$ and the diode of $S_{ap\pi}$ blocks. At that time the transistor in $S_{ap\pi}$ can be turned off with no losses. The capacitor is further charged linearly by the input current $i_a$ until its voltage reaches $V_0$. At that point two rectifier diodes start conducting, connecting the converter input and output. In this transition, it is important that the resonant capacitor should contain enough energy to charge $L_{lk}$ to $i_a$, i.e.:

$$\frac{1}{2} V_0^2 C_r \geq \frac{1}{2} i_m^2 L_{lk},$$

where $i_m$ is the maximum amplitude of input phase current. If (4.24) is satisfied for the maximum input phase current amplitude, ZCS is maintained under any line and load conditions.

The converter operation has been verified through simulation which was performed with the following circuit component values and operating conditions: $L_{lk} = 20 \ \mu H$, $V_0 = 50 \ V$, $n = 1/10$, $C_r \approx 250 \ \text{nF}$, $i_a = 6 \ A$, $i_b = -4 \ A$, and $i_c = -2 \ A$. Figure 4.18 shows the simulated converter waveforms. This simulation has been performed under the assumption that the switches and diodes
Figure 4.18. Simulated circuit waveforms with ideal switches and diodes.
Figure 4.19. Simulated circuit waveforms with realistic switch and diode models.
in the primary are ideal, i.e. have no parasitic capacitance and no reverse recovery.

In reality, however, the switches and diodes are not ideal, and this converter cannot absorb these parasitic components and effects. Figure 4.19 shows the simulated waveforms with more realistic switch and diode models. To better illustrate the problem, slow diodes have been used in the simulation. It can be seen from Figure 4.19 that the diodes in the primary experience some reverse recovery and that there is a resonance between \( L_{ik} \) and the parasitic switch capacitances. These effects result in increased voltage stress on the primary devices.

In this simulation the overvoltage problem is mitigated using an active clamp connected between the points \( p \) and \( n \). The clamp circuit receives mainly the reverse recovery energy and clamps the voltage \( |v_{pn}| \) to 550 V. The energy entering the clamp circuit is delivered to the converter output through a low-power isolated dc-dc converter. The diode reverse recovery problem can further be reduced by connecting a small saturable inductor in series with each switch in the primary. In addition to this, an R-C snubber can be connected between points \( p \) and \( n \), to damp the high-frequency oscillation of \( v_{pn} \). In reality, the magnitude of the oscillation and reverse recovery is not severe. In a 5 kW, 50 kHz converter, for example, it has been found that it accounts for loss of efficiency of less than 1 %.
4.4 Conclusions

The proposed ZVS three-phase rectifier offers several significant advantages over the standard configurations. The overall efficiency and size of the proposed ZVS rectifier are superior to those of the standard configuration. In the ZVS rectifier, the total conduction losses are reduced due to the fact that the current flows through two switches and four diodes, while in the standard configuration, the current always flows through four switches and four diodes. In the ZVS rectifier, soft-switching conditions are provided for all devices. This condition eliminates the switching losses, significantly reduces the EMI problems, and eliminates the need for use of snubber circuits typically employed in hard-switched converters.

The total number of semiconductor components is smaller in the proposed ZVS rectifier than in the standard configuration. Twelve active switches and four fast rectifier diodes are required for the implementation of the ZVS rectifier. In the standard configuration, ten active switches and ten fast diodes are required. In addition to this, there is no intermediate filter in the ZVS rectifier. Being a buck-type converter, the ZVS rectifier is a good candidate for medium-power applications in which MOSFET is the preferred device.

The loss of ZVS property at light load conditions is inherent to the proposed circuit. However, this loss does not represent a problem, because the ZVS property is lost only partially at light loads. Furthermore, at light loads,
the conduction losses in the devices are very small, so the additional switching losses will not pose any thermal problems.

Even with the problems described above, the ZCS boost rectifier is an excellent candidate for rectifier applications in which the IGBT is the most favorable device choice, i.e., in applications in which the input voltage exceeds 500 V. This is typically the case in many telecommunication and computer applications which require power levels of several kilowatts and must accommodate universal input line range. In these cases this converter seems to provide performance that is superior in terms of efficiency and size compared to the performance of a two-stage converter.
5.0 Digital Controller for the Isolated ZVS Buck Rectifier

5.1 Introduction

In the past, digital control of switching power converters has not been widely used. Due to the relatively simple control algorithms and the high switching frequency applied in power conversion, the analog implementation of the control was usually simpler and cheaper. With the development of more complex power converters, such as three-phase converters, power factor correction circuits, matrix converters, etc., and particularly soft-switching three-phase converters, analog controllers become inadequate in terms of complexity, reliability, cost, and performance. This chapter illustrates feasibility and describes details of the implementation of a high-performance,
high-frequency, low-cost, simple, and versatile digital controller for the isolated ZVS buck rectifier.

5.2 Controller Functions

From the discussion of rectifier operation in Chapter 4, as well as from [H9], it can be concluded that a digital controller for the ZVS buck rectifier has to perform the following tasks in every switching cycle:

1. Determine the operating mode of the converter according to the present segments of the three-phase input and output quantities.
2. Calculate the duty cycles, \( d \), for the switches to perform the required current and voltage synthesis tasks.
3. Convert the duty cycle values into switching pulses of corresponding duration (PWM).
4. Distribute the pulses to the appropriate switches according to the present converter operating mode.

The functional block diagram of the controller is shown in Figure 5.1. The control process within each sampling interval starts by measuring the input phase voltages, \( v_a \), \( v_b \), and \( v_c \), converting them into digital form, scaling them, and thus producing the scaled measurement of input voltages \( u_a \), \( u_b \), and \( u_c \). Using this measurement, the present 30° segment of the input voltages is de-
Figure 5.1. Controller functional block diagram.
terminated in the functional block \( \text{SEG} \). The segment information is coded by a six-bit word \((S_{i0} \text{ to } S_{i5})\), in which the lower three bits \( S_{i0}, S_{i1}, \text{ and } S_{i2} \) represent the signs of the line voltages \( v_{ab}, v_{bc}, \text{ and } v_{ca} \), while the upper three bits, \( S_{i3}, S_{i4}, \text{ and } S_{i5} \), represent the signs of the phase voltages, \( v_a, v_b, \text{ and } v_c \), respectively. The upper three bits of the segment information are used in the multiplexer block, \( \text{MUX} \), to select the two input phase voltages with the same sign, \( u_x \), and \( u_y \). As discussed in Chapter 4, it is desirable that a rectifier draws input phase currents that are sinusoidal and in phase with the input phase voltages. Therefore, \( u_x \) and \( u_y \) are used as references for duty cycles, as given by \((4.8)\). The references \( u_x \) and \( u_y \) are multiplied by the modulation index \( D_m \), to obtain the duty cycles \( d_{sx} \) and \( d_{sy} \). The modulation index \( D_m \) is an input to the controller which, in general, supplied by the output regulation loops. Since in the ZVS buck rectifier the primary duty cycles are always bigger than the secondary duty cycles, the duty cycles \( d_{sx} \) and \( d_{sy} \) have to further be modified to obtain the primary duty cycles \( d_x \) and \( d_y \). In general the relationship between the primary and secondary duty cycles is:

\[
\begin{align*}
      d_x(\theta) &= d_{sx}(\theta) + \Delta d_x(\theta), \\
      d_y(\theta) &= d_{sy}(\theta) + \Delta d_y(\theta).
\end{align*}
\]  

(5.1)

The terms \( \Delta d_x \) and \( \Delta d_y \) are in general functions of \( \theta, I, \) and \( V_m \), and should be calculated in each switching cycle. However, they are also small, and can, therefore, in most cases be approximated by a constant, without significantly
increasing the distortion of input currents. This approximation has been used in the controller implementation presented here.

The calculated duty-cycle information \( d_x \) and \( d_y \) is sent to the PWM generators which generate a coded switching instant sequence, \( A \) through \( E \). The PWM signals \( A \) to \( E \), and the operating mode signals \( S_{16} \) to \( S_{15} \) are sent to the decoder which distributes the gate-drive signals to the appropriate converter switches. The decoder also performs the converter shut-down in case of software failure, overcurrent or overvoltage conditions, or in case of external shut-down request.

The functions encircled by the dashed line in Figure 5.1.a are performed by a DSP. The controller implementation and the division of controller tasks between software and hardware may vary depending on the power stage topology and the components used in the controller implementation. The following sections describe the implementation details of the controller for the isolated ZVS three-phase rectifier.

5.3 Controller Implementation

5.3.1 Hardware Implementation

The block diagram of the the controller hardware is shown in Figure 5.2. The controller prototype was implemented using a commercial personal
Figure 5.2. Control system block diagram.
computer-based, digital signal processing development system, [13], which contains the TMS320E14 DSP unit [14], 4 analog/digital (A/D) converters, RAM, and additional circuitry. Although the hardware of this development board is overdesigned for greater flexibility, the controller could be implemented with no more than four integrated circuits. This would include the DSP, with an additional data conversion integrated circuit, a single programmable logic device (PLD) for the implementation of the decoder, and an operational amplifier for the error amplifier.

The controller uses three A/D converters to sample the input phase voltages through an isolation transformer, providing the signals \( u_a \), \( u_b \), and \( u_c \). An additional A/D converter is employed to close the output voltage loop. The converter samples the error voltage obtained from the external error amplifier and compensation circuit, which is used as the modulation index \( D_m \). All the converters are mapped in the program memory space.

Because the primary voltage \( v_{pn} \) (Figure 4.6) consists of four pulses with equally distributed zero voltage intervals between them, five PWM signals, \( A-E \), and the synchronization signal SY, are required, instead of just two PWM signals A and B needed for standard rectifier control function shown in Figure 5.1. The controller employs five of the six TMS320E14 on-chip PWM generators to generate the pattern of switching instants for the converter, (A-E). The on-chip parallel I/O port is used to output the coded information on the converter operating mode \( (S_{ij} - S_{j5}) \), and the synchronization signal SY. The time-out protection signal \( WDT' \) is provided by the on-chip watchdog timer.
system. The switch decoder is implemented using an erasable PLD, [15], and auxiliary circuits. The signals from the decoder are fed to twelve independent, optically isolated gate drive circuits. Details of gate drive signal generation are provided in Appendix D.

5.3.2 Controller Software

The emphasis in designing the control software for this application was on speed. For that reason, the controller software was written entirely in machine code. The controller program is time-synchronized with the interrupt requests from the timer associated with the PWM generators. The period of the PWM generators is equal to the desired switching period, \( T/2 = 10 \mu s \). Because the execution of the controller program takes close to 20 \( \mu s \), only every second timer interrupt is accepted, so that the system sampling frequency is 50 kHz. The software synchronization signal SY is generated as a “waiting-for-interrupt” signal. It is high only when the software is waiting for the interrupt, i.e. only shortly before and after every second interrupt.

The entire controller program is placed in the interrupt service routine. Since there is only one interrupt in the system, the interrupt response is a single branch instruction, that transfers the program control to the interrupt service routine. When the controller program has completed its run, it waits for the next interrupt. None of the operation commonly performed as a response to an interrupt request are performed here. Since the program is ex-
executed in its entirety under interrupt, none of the register values, nor even the return address are saved. The listing and explanation of the controller program are provided in Appendix D.

5.4 Conclusions

The main features of the digital controller proposed in this chapter are implementation simplicity, high performance, universality, and low cost. The controller hardware could be implemented using no more than four integrated circuits: a data acquisition circuit, a DSP, a PLD for the implementation of the decoder, and an op-amp for the error amplifier.

Due to the versatility of digital circuits, the proposed controller could also be used in other applications such as three-phase inverters, three-phase power factor correction circuits, etc. This would only require modification of the controller software and reprogramming of the decoder PLD. Due to the low price and high software and hardware capabilities of currently available digital components, the cost of the entire controller could be very low.

The presented controller implementation example clearly demonstrates the feasibility of producing versatile, high-performance, reliable, low-cost controllers for soft-switching PWM three-phase power converters operating at high switching frequencies.
6.0 Input Filter Design for Switching Rectifiers with Power Factor Correction

6.1 Introduction

The design of input electromagnetic interference (EMI) filters for switching rectifiers and power factor correction (PFC) circuits is becoming increasingly important in the light of the new harmonic and EMI reduction standards. These standards impose very high switching noise attenuation requirements, often in excess of 100 dB. Such attenuation levels are all but impossible to meet using the existing input filter technology. They call for the use of three- or even four-stage input filters for which there are practically no design guidelines. The filters are typically designed on a trial-and-error basis, using circuit simulators. This type of design results in poor and bulky input filters which may account for the larger part of the converter weight and volume.
Unlike the case of the EMI filter design for dc-dc converters, [G1], the design of input filters for rectifier circuits has not yet been addressed. The issues in designing an EMI filter operating with ac power are different from and broader than those involved in the filter design for dc-dc converters; thus, the design guidelines provided in [G1] are inadequate for the PFC circuit input filter design. The use of standard input filter design procedures developed for dc-dc converters generally results in poor power factor due to large reactive currents through input filter capacitors, excessive power dissipation in damping resistors, or converter instability due to filter-converter impedance interaction.

This chapter addresses the PFC circuit EMI filter design and proposes the use of a new, high order input filter. The proposed technology provides great reduction in filter size and output impedance, while maintaining the power factor at a desired level. Attenuation levels in excess of 100 dB are easily attainable. Filter design procedure is provided that makes possible a simple and fast design of filters with arbitrary number of stages. New passive and active filter damping methods that guarantee optimal filter pole damping, while practically eliminating damping resistor power dissipation, are also presented.

The results presented in this chapter can directly be applied in single-phase PFC systems, even though the input filter design for such converters is often less difficult due to lower power processing requirement.
6.2 Rectifier Input EMI Filter Design Criteria

The three main requirements a PFC circuit input filter has to meet are:

1. required switching noise attenuation,
2. low input displacement angle between filter input voltage and current, and
3. overall system stability.

The first requirement is dictated by the EMI control standards, e.g. VDE 0871, MIL. STD. 461D. All of the mentioned standards require very low EMI levels. The required switching frequency attenuation provided by the input filter, for a typical 1 kW - 10 kW converter switching in the 50 kHz range, is between 60 and 120 dB, depending on the converter power and topology.

The second requirement exists only in the PFC circuit input filter design. Figure 6.1.a shows a simplified diagram of a PFC converter with an input filter. Figure 6.1.b shows the phasor diagram of the line frequency components of the system currents and voltages. This could represent either a single-phase PFC system or one phase of a three-phase system with phase-to-neutral voltages. A typical PFC circuit is operated in a way that produces converter average current, $i_a$, that is in phase with the converter voltage, $v_a$. Since the voltage drop across the input filter inductor $L$ is very small at line frequency, the voltage at the converter input is essentially equal to the line voltage $v_A$. 
Figure 6.1. Input voltage and current displacement due to input filter: a) A simplified PFC converter and input filter diagram, b) current and voltage phasor diagram.
The voltage $v_a$ causes reactive current, $i_c$, to flow through the filter capacitor $C$. The total current drawn from the line, $i_A$, is therefore phase-shifted relative to the input voltage, by the angle $\phi$, resulting in reduced input power factor. If $v_a$ and $i_a$ are given by:

\[
\begin{align*}
  v_a &= V_m \cos \omega t, \\
  i_a &= I_m \cos \omega t,
\end{align*}
\]

where $V_m$ and $I_m$ are the voltage and current amplitudes, respectively, the input current, $i_A$, in Figure 6.1 is:

\[
i_A = i_s + i_c = I_m \cos \omega t - \omega C V_m \sin \omega t.
\]  

Therefore, current $i_A$ leads voltage $v_A$ by a phase angle:

\[
\phi = \tan^{-1} \frac{\omega C V_m}{I_m}.
\]

The phase shift is proportional to the filter capacitance value, so in order to maintain high input displacement factor (IDF), defined as $\text{IDF} \equiv \cos \phi$, the capacitor size has to be minimized. This translates into an upper limit for the filter capacitor value, which from (6.3) is:

\[
C_{max} = \frac{I_m}{\omega V_m} \tan^{-1} \text{IDF}.
\]

In the case of multi-stage filters, $C_{max}$ represents the limit for the sum of all parallel capacitances in the filter, [G5].
The capacitor size limitation has several implications for the PFC circuit filter design. In order to meet the required attenuation specifications, the filter inductor size increases, which results in the overall filter size increase. Filter damping methods typically applied in the dc-dc converter filters cannot be used. The input filter output impedance, related to the total filter capacitance, is more difficult to control, potentially resulting in converter instability.

The third requirement amounts to controlling the impedance interaction between the input filter and the PFC converter. In general, the filter output impedance should be as low as possible when compared to the converter input impedance [G1], [G5], [G2]. The filter output impedance can be reduced by increasing the filter capacitor size. The impedance interaction constraint will practically determine the lower bound on the filter capacitor value. Additionally, proper filter pole damping is extremely important for achieving low filter output impedance for all frequencies, and thus overall system stability.

Finally, in order to keep the filter component values and size small, it is desirable to have the filter corner frequency as close as possible to the switching frequency, i.e. the filter should have a very steep pass-band-to-stop-band transfer characteristic. Therefore, only high-order filters can have a reasonable size and meet all the requirements in the PFC circuit.

One filter type that is known to provide these features is the Cauer-Chebyshev (CC) filter, [H2], also known as the elliptic-integral filter. A two-stage CC filter with normalized component values and a typical attenuation
Figure 6.2. **Cauer-Chebyshev filter**: a) Two-stage filter topology, b) typical attenuation characteristic.
characteristic are shown in Figure 6.2.a and b, respectively. The filter design procedure is discussed later in the chapter.

The filter shown in Figure 6.2.a can be used either in a single-phase or in a three-phase PFC system. In a three-phase system, the filter of Figure 6.2.a would be a per-phase filter connected between the line and neutral points, which can then be transformed into equivalent line-to-line filter if desired.

6.3 Passive Damping of Filter Poles

Figure 6.3 shows four possible filter pole damping methods. The damping method shown in Figure 6.3.a is typically used in dc-dc converters. This method is not applicable in ac power converters for the following reason. In order for the damping resistor to be effective, the capacitor in series with $R_d$ has to be at least ten times bigger than the other filter capacitor. This large capacitor can cause excessive dissipation at line frequency due to the ac current flowing through the damping branch. Also, the required wide spread of capacitance values is usually not possible with CC filters.

The damping method shown in Figure 6.3.b uses a parallel R-L branch. This method eliminates the excessive resistor dissipation, and is therefore widely used in ac power converter filters. The drawback of this method is that the parallel R-L branch provides an alternative path for high-frequency current, thus deteriorating the high-frequency attenuation capability of the filter.
Figure 6.3. Four passive filter pole damping methods.
In order to meet the required attenuation, the filter has to be overdesigned by typically more than 50 % when compared to filters shown in Figure 6.3.c and d, which results in excessively large components.

The damping method shown in Figure 6.3.c provides an optimal filter attenuation characteristic, and is normally used in low-power electronic circuits. This method, however, cannot be used in power electronic circuits due to excessive power dissipation in the damping resistor.

A new damping method proposed here is shown in Figure 6.3.d. It solves the dissipation problem of the series resistor damping scheme by providing an alternative line frequency current path through the inductor \( L_d \), without affecting the damping action of the resistor at high frequencies. The main drawback of the proposed damping method is that the corner frequency of the damping network given as \( f_d = R_d/(2\pi L_d) \) has to be significantly lower than the lowest filter pole frequency. This requirement typically results in a large value of \( L_d \).

### 6.4 Active Damping of Filter Poles

The problem of the passive damping method shown in Figure 6.3.d can be resolved by implementing the damping circuit using an active impedance simulation scheme. A possible active damping scheme is shown in Figure 6.4.a which replaces the \( R_d||L_d \) connection in Figure 6.3.d. The trans-
Figure 6.4. Active damping scheme: a) One circuit implementation, b) impedance characteristic.
former T1 is used to sense the line current. The low-frequency components of T1's secondary current are bypassed to ground through L. The high-frequency current components flow through C and R and create voltage at the output of the operational amplifier. The voltage \(v_d\) at high frequencies is proportional to the line current, i.e. \(v_d \approx R \frac{i}{n_1}\). This voltage is impressed across the secondary of the transformer T2, so that the effective resistance seen in the primary is:

\[
R_d = \frac{v_{qr}}{i} \approx \frac{R}{n_1 n_2},
\]  

(6.5)

at high frequencies. The corner frequency of L and C has to be much higher than the line frequency and much lower than the lowest input filter pole frequency. The resistor in parallel with L provides critical damping for the resonant circuit formed by L and C. The impedance characteristic, \(Z_{qr}\) seen in the circuit primary is shown in Figure 6.4.b, and is given by:

\[
Z_{qr}(s) = \frac{R}{n_1 n_2} \frac{s + \frac{n_2}{n_1 RC}}{s^2 + s \frac{2}{\sqrt{LC}} + \frac{1}{LC}}.
\]  

(6.6)

At low frequencies, \(Z_{qr}\) is the impedance of the inductor L reflected through T1. There is practically no current through C and R, so that the op-amp does not process any power. The placement of the zero:
\[ f_{zqr} = \frac{-n_2}{2\pi n_1 R C} \] (6.7)

is not very critical. The only requirement is that it should lie below the damping circuit pole frequency. Such a placement ensures that \( Z_{qr} \) is resistive above the pole frequency \( f_{pqr} = 1/(2\pi\sqrt{LC}) \).

This active circuit provides significant savings in size compared to the passive damping circuit realization. The power processed by the circuit is typically less than 0.1 % of the total converter power, so it can be easily implemented with high-power op-amps.

6.5 Cauer-Chebyshev EMI Filter Design Procedure

The design procedure presented in this section uses the already existing knowledge of CC filter design systematized and condensed in filter design tables such as those in [H2], or available in filter design computer programs, [11]. This approach leads to a very simple and flexible design procedure that can efficiently be used for the design of input filters of any order.

The first step in the filter design is the determination of the required filter attenuation. The allowable EMI voltage, \( V_{EMI} \), injected to the line by the converter at the switching frequency, can be determined from the EMI specifications. \( V_{EMI} \) is typically specified as a voltage drop on a 50 \( \Omega \) resistor \( R_{isn} \) (line
impedance stabilization network, [H3]), caused by the converter switching current. The switching frequency current, $I_{sw}$, generated by the converter can be determined analytically by Fourier analysis, by simulation [G4], or by measurement. With the knowledge of $V_{EMI}$ and $I_{sw}$, the required filter attenuation, $A_{min}$, at the switching frequency is given by:

$$A_{min} = \frac{R_{lsn} I_{sw}}{V_{EMI}}.$$  \hspace{1cm} (6.8)

Next, the total maximum filter capacitance has to be determined. For this purpose, the input displacement factor constraint has to be chosen as a desired minimum IDF under certain line voltage, $V_{lim}$, and current, $I_{lim}$, conditions, typically high-line, partial load. The total maximum filter capacitance can now be calculated using (6.4), with $I_m = I_{lim}$, and $V_m = V_{lim}$.

Next, the normalized filter parameters have to be determined. For this, the filter order, $n$, has to be chosen first. The choice may be made either by using filter order nomographs, [H2, page 142], or by reading the filter tables. The assumptions that should be made in the filter order choice are that the passband ripple is reasonable (e.g. $A_{max} \backsimeq 2 dB$) and that the converter is running under no-load condition ($R_{eq2} = \infty$). This will guarantee proper filter damping even under no load conditions. There is some freedom in the filter order choice. Filters of higher order may end up being smaller than those of lower order, so some engineering judgment should be used in each application. Notice that with a filter structure as shown in Figure 6.2.a (series inductor at the filter input, parallel capacitor at the filter output), $n$ is always
an even number. With the knowledge of $A_{min}$ and the filter order determined, the normalized filter parameters $L'_1$, $L'_2$, etc., $C'_2$, $C'_4$, etc., and $\Omega_z$, all defined in Figure 6.2, can be readily obtained from the filter tables.

The final design step is the filter denormalization. First, the reference frequency, $\omega_r$, is calculated as:

$$
\omega_r = 0.85 \frac{2 \pi f_{sw}}{\Omega_z},
$$

where $f_{sw}$ is the converter switching frequency. With the reference frequency calculated in this way, the frequency of the filter transfer function first notch will be 15 % below the switching frequency. It is important to place the switching frequency sufficiently far from the transition region, so that any variation of filter component values does not influence its attenuation characteristic at switching frequency significantly. The 15 % margin in (6.9) guarantees that if the filter is built using components with 10 % tolerance, the switching frequency will remain in the filter stop-band region. If components with wider tolerance are used, this margin has to be increased.

In general, the filter denormalization is done by choosing the value of any one filter component, and then calculating the values of the remaining filter components. This choice is based on different practical considerations, such as availability of a particular component, damping resistor power dissipation, total filter size, etc. In the filter design for PFC circuits, the filter should be denormalized and its total capacitance should equal $C_{max}$. Such denormali-
tion ensures that the *IDF* requirement is met. So, the damping resistor is calculated as:

\[
R_d = \sum_{i=1}^{i=n/2} \frac{C'_{2i}}{\omega_r C_{\text{max}}}.
\]  

(6.10)

The remaining filter components are calculated using:

\[
L_i = \frac{L_i' R_d}{\omega_r}, \quad i = 1,2,\ldots,n-1, \quad \quad (6.11)
\]

\[
C_k = \frac{C_k'}{\omega_r R_d}, \quad k = 2,4,\ldots,n.
\]

With the filter design completed, only the active damping circuit remains to be designed. The first step in doing this is to choose the transformer turns ratios, \(n_1\) and \(n_2\), according to the maximum line current and the operational amplifier voltage and current capabilities. With \(n_1\) and \(n_2\) known, \(R\) can be calculated from (6.5) and (6.10). T1's magnetizing inductance can be used as \(L\), and \(C\) can be calculated so that \(f_{pqr}\) is much higher than the line frequency, and much lower than the lowest filter pole frequency, \(f_{lp}\), e.g.

\[
C = \frac{1}{4 \pi^2 L f_{\text{line}} f_{lp}}.
\]  

(6.12)
Finally, it should be checked if \( f_{zqr} \), given by (6.7), is lower than \( f_{pqr} \). If not, \( n_1 \), \( n_2 \), \( R \) and/or \( C \) should be modified, and the damping circuit should be redesigned accordingly.

The use of the above design procedure is illustrated in the design of the two-stage filter shown in Figure 6.5 and is given in Appendix E. Since the procedure is applicable to the design of filters of any order, a possible three-stage implementation of the input filter that also meets the same specifications is shown in Figure 6.6.a. This illustrates the possibility of reducing the overall filter size by increasing the number of filter stages.

Figure 6.6.b shows a three-stage filter designed to meet the specifications of the example, but using the more conventional parallel R-L damping method. The total inductance in this filter is around 60 \( \mu H \) as compared to only 18 \( \mu H \) in the actively damped filter. The reduction of the inductor size leads both to significant reduction of the filter size and also to the reduction of the filter output impedance, thus contributing to the overall system stability.

The great advantage of using CC filters is illustrated when the above filters are compared with the standard LC filter designed for the same specification, which is shown in Figure 6.6.c.
Figure 6.5. Two-stage CC filter from the design example.
Figure 6.6. Comparison of different filters designed to meet the same specification: a) three-stage CC filter with active damping, b) CC filter with passive damping, and c) standard LC filter.
6.6 Experimental Verification

The filter in Figure 6.6.a has been implemented and tested. Figure 6.7 compares measured transfer functions of the filter which is damped passively using only the 1.7 Ω series resistor (as shown in Figure 6.3.c), with those of the filter using active damping. This comparison demonstrates that the active damping scheme provides the required damping without affecting the ideal filter transfer function.

Figure 6.8 shows the damping circuit performance under large-signal transient conditions. The filter is connected to a square-wave modulated active load drawing a 2.5 A sinusoidal current plus a 1 A square-wave current. The equivalent block diagram of the measurement setup is shown in Figure 6.9. Figure 6.8.a shows the filter input current (i in Figure 6.9) when the filter is not damped, i.e. with the active damping circuit turned off. The high-frequency oscillations originate from the undamped 5 kHz filter pole. Figure 6.8.b shows the same current when the damping circuit is operational. Figure 6.8.c shows the operational amplifier output voltage (v_d in Figure 6.4.a). It is seen that even though there is a large 60 Hz current component in the filter current, the voltage v_d contains only a very small 60 Hz component.
Figure 6.7. Measured filter transfer functions.
Figure 6.8. Filter responses to current transients: a) Filter input current without damping, b) filter input current with active damping, and c) op-amp output voltage.
Figure 6.9. Block diagram of the filter measurement setup used to obtain the large-signal filter responses.
6.7 Conclusions

Power converter designers face several difficult issues when designing input filters for PFC circuits: very high attenuation requirement, low filter output impedance requirement, and maintenance of high converter power factor. Meeting all these requirements is in most cases impossible using the standard filter design technology. In fact, the existence of “standard input filter design technology for PFC circuits” is indeed questionable. There are no analytical or systematic numerical design tools, and the designs are performed on a trial-and-error basis, which results in large and heavy filters.

A new approach to the design of input filters for power electronic circuits is presented here. This approach is based on the application of a vast body of knowledge about passive L-C filters that has existed for many years, but has not been used in power electronics. The main obstacle to applying this knowledge was the inadequate filter pole damping technology.

The new passive and active filter pole damping schemes provide damping without affecting the filter high-frequency attenuation characteristic. Applying these damping methods to high-order elliptic filters results in significant filter size reduction compared to the standard filter designs.

A design procedure for PFC circuit input filters is also presented. Relying on the existing, well organized, and readily available knowledge about passive L-C filters, the design procedure is simple and straightforward.
7.0 Conclusion and Future Work

This dissertation addressed several key issues related to high-frequency three-phase soft-switching PWM power converters. These are:

1. analysis, synthesis, and design of three-phase soft-switching PWM power converter topologies,

2. design of input EMI filters for three-phase converters, and

3. design of microprocessor controllers for three-phase converters.

The notion of soft-switching, often not very well defined and misused, was defined precisely in terms of switch voltage and current waveforms during switching. It was shown that the ideal switching condition for both switch turn-on and turn-off is that of having the switch voltage equal to zero during switching. Based on this conclusion and on common topological properties of PWM converters, two generalized soft-switching PWM converter circuit rep-
resentations were derived. It was shown that all existing soft-switching PWM converters can be placed in one of the two groups:

1. converters with soft-switching commutation circuits in series with power flow, and
2. converters with soft-switching commutation circuits in parallel with power flow.

The significance of this generalization is twofold. First, the two generalized converter representations can be used to classify and evaluate the existing soft-switching PWM converters. Second, and more importantly, the two simple generalized circuits can be used as starting point for synthesis of more complex soft-switching PWM converters, such as three-phase converters.

Based on the generalized soft-switching PWM converter representations and common topological properties of three-phase and dc-dc PWM converters, two new procedures for synthesis of three-phase soft-switching PWM converters were derived. The two procedures were used to synthesize five new three-phase soft-switching PWM converter topologies suitable for wide range of applications.

1. Nonisolated converters. The three nonisolated three-phase soft-switching PWM converters use the ZVT technique to eliminate or significantly reduce switching losses and diode reverse recovery problems. The addition of the commutation circuit does not result in any increase in component current
and voltage stresses over the conventional PWM counterpart. The converters are controlled by a slightly modified conventional PWM control algorithm. The soft switching is achieved using a low-power commutation circuit having only one controlled switch. All the components of the commutation circuit have very small average current ratings.

a. **ZVT boost rectifier/VSI.** By virtue of elimination of several sources of switching losses, stresses, and noises, the proposed high-frequency rectifier/inverter circuit is considered to be a prime candidate for high-performance, high-power applications where bidirectional power flow is required. The converter is deemed superior to the RDCL converters because it does not increase the voltage stress on the devices. The proposed converter matches the performance of the ARCP converter, while it uses significantly fewer circuit components for implementation of the soft switching, at the expense of increased current and switching stress.

b. **ZVT three-level boost rectifier.** This converter is a good candidate for power factor correction applications in which the input voltage is high (380-480 V line-to-line), or for applications in which the input voltage range is relatively wide. In such cases, the converter can operate efficiently with high output voltage (close to 1000 V) while using MOSFETs rated for only 500 V. In addition, the converter provides two regulated output voltages of \( V_{pn}/2 \). These two outputs can be used as inputs to
two separate isolated dc-dc converters, each using switches rated for 
\(V_{pn}/2\), thus allowing for lower cost and higher efficiency operation.

c. **ZVT buck rectifier.** Due to the series connection of diode and transistor 
in the voltage two-quadrant switch implementations, obtaining soft 
switching in this converter was difficult. The application of the ZVT 
technique resulted in achieving only a reduction of transistor turn-on 
losses. Even that was obtained at the expense of increased device 
voltage stress. The practical value of this circuit is, therefore, ques-
tionable. The main purpose of introducing this circuit was to illustrate 
the difficulties of implementing soft-switching in converters with voltage 
bidirectional switches, and the importance of providing proper means 
of switch voltage clamping during soft-switching.

2. **Isolated converters.** The single-stage three-phase PWM rectifiers offer the 
following distinct features:

- transformer isolation;
- soft switching for all power semiconductor switches;
- tight output voltage regulation with fast transient response;
- unity input power factor; and
- no low-frequency harmonics on either input or output.

a. **Three-phase ZVS Buck Rectifier.** Being a ZVS converter with hard 
switch turn-off, the isolated ZVS buck rectifier is an excellent candidate 
for applications in which MOSFETs are the most favorable device 
choice, i.e. in applications where the peak of input line voltage does not
exceed 500 V. These primarily include power conversion systems in aircraft and ships, which often use three-phase 208 V ac power. Under these conditions, the proposed converter can operate with good efficiency, while switching at very high frequency, providing high power density and low EMI.

b. **Three-phase ZCS Boost Rectifier.** The ZCS boost rectifier is an excellent candidate for rectifier applications in which the IGBT is the most favorable device choice, i.e., in applications in which the input voltage exceeds 500 V. This is typically the case in many telecommunication and computer applications with power level of several kilowatts and universal line input. Since this converter provides only quasi-soft switching conditions for some of its devices, some additional snubbing is required to achieve satisfactory EMI performance. Still, in many applications this converter seems to provide performance that is superior in terms of efficiency and size to the performance of a two-stage converter.

A DSP-based controller implementation example was presented that clearly demonstrates the feasibility of producing versatile, high-performance, reliable, low-cost controllers for three-phase power converters operating at high switching frequencies. The controller was applied to the control of the three-phase isolated ZVS buck rectifier switching at 100 kHz.

Due to the versatility of digital circuits, the proposed controller could also be used in other applications such as three-phase inverters, three-phase
power factor correction circuits, etc. This would only require modification of the controller software and reprogramming of the decoder PLD.

A new approach to the design of input filters for power electronic circuits was presented. This approach is based on the application of a vast body of knowledge about passive L-C filters that has existed for many years, but was not used in power electronics. The main obstacle to applying this knowledge was the inadequate filter pole damping technology.

The new passive and active filter pole damping schemes provide damping without affecting the filter high-frequency attenuation characteristic. Applying these damping methods to high-order elliptic filters results in significant filter size reduction compared to the standard filter designs.

A design procedure for PFC circuit input filters was also presented. Relying on the existing, well organized, and readily available knowledge about passive L-C filters, the design procedure is simple and straightforward.

Further research in the area of soft-switching three-phase PWM power conversion could include the following:

- Elimination of intuitive steps in the three-phase converter design procedure related to implementation and simplification of commutation circuits.
- Development of large- and small-signal models of soft-switching three-phase converters.
• Development of design procedure and experimental evaluation of the ZCS isolated boost rectifier.

• Experimental evaluation of the ZVT three-level boost rectifier.

• Analysis of converter operation under nonideal line conditions.

• A broader and more systematic study of filter design techniques that would make use of the existing general filter theory with the objective of developing design procedures for filters with minimum weight, power loss, phase shift, etc.

• Development of a universal three-phase power converter controller using advanced digital technology.

• Study of issues related to converter line synchronization under nonideal line conditions.
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I. CATALOGS AND SOFTWARE


J. STANDARDS


K. PATENTS AND INVENTION DISCLOSURES


Appendix A. Derivation of Maximum d in the

Isolated ZVS Buck Rectifier

In this derivation it is assumed that the output current ripple is small
compared to the load current, which is a realistic assumption at full load where
the loss of duty cycle is maximal.

From Figure 4.6:

\[ I'_{dx}(\theta) + I''_{dx}(\theta) \approx I'_{dy}(\theta) + I''_{dy}(\theta) \approx 4 n I, \]  \hspace{1cm} (A.1)

From (A.1) and (4.13):

\[ \Delta d_x'(\theta) \approx \frac{4 n I L_{lk}}{v_{ab}(\theta) T}, \quad \Delta d_y'(\theta) \approx \frac{4 n I L_{lk}}{v_{ac}(\theta) T}. \]  \hspace{1cm} (A.2)

Using (4.6), (4.2), (4.4), (4.8), and (A.2), it follows that:
\[
d(\theta) = -D_m \left( \cos(\theta - \frac{2\pi}{3}) + \cos(\theta + \frac{2\pi}{3}) \right) + \\
+ \frac{\sqrt{3}}{4} \Delta d(0) \left( \frac{1}{\cos(\theta + \frac{\pi}{6})} + \frac{1}{\cos(\theta - \frac{\pi}{6})} \right),
\]

(A.3)

where:

\[
\Delta d(0) = \frac{16nL_{lk}}{3V_m T}.
\]

(A.4)

d(\theta) has a maximum for \( \theta = 0 \) if its derivative is negative for \( 0 \leq \theta < \pi/6 \). If that is the case, we can write:

\[
d(0) = D_m + \Delta d(0) = 1,
\]

(A.5)

and require:

\[
\frac{d}{d\theta} d(\theta) \leq 0.
\]

(A.6)

Derivating \( d(\theta) \) with respect to \( \theta \) gives:

\[
\frac{dd(\theta)}{d\theta} = D_m \left( \sin(\theta - \frac{2\pi}{3}) + \sin(\theta + \frac{2\pi}{3}) \right) + \\
+ \frac{\sqrt{3}}{4} \Delta d(0) \left( \frac{\sin(\theta + \frac{\pi}{6})}{\cos^2(\theta + \frac{\pi}{6})} + \frac{\sin(\theta - \frac{\pi}{6})}{\cos^2(\theta - \frac{\pi}{6})} \right) \equiv
\]

\[
\equiv D_m f_1(\theta) + \Delta d(0) f_2(\theta).
\]

(A.7)

Solving (A.5), (A.6), and (A.7) for \( \Delta d(0) \) gives:
\[ \Delta d(0) \leq \frac{f_1(\theta)}{f_1(\theta) - f_2(\theta)} \equiv g(\theta). \quad (A.8) \]

It is easily checked that \( g(\theta) \geq 0.25 \) for \( 0 \leq \theta < \pi/6 \). So, for \( \Delta d(0) \leq 0.25 \), \( d(\theta) \) has a maximum at \( \theta = 0 \).
Appendix B. Derivation of Equivalent Capacitance

Ceq in the Isolated ZVS Buck Rectifier

The energy needed to charge the capacitance of nodes $p$ or $n$ at $\theta = \pi/6$ is:

$$
E_c = \frac{4}{3} (\sqrt{3} V_m)^2 C_M + \frac{4}{3} \left( \frac{\sqrt{3}}{2} V_m \right)^2 \sqrt{2} C_M + \frac{1}{2} (\sqrt{3} V_m)^2 C_T. \quad (B.1)
$$

To explain how each term in (B.1) is derived, we examine the transition time $t_1$ in Figure 4.6, taking place at $\theta = \pi/6$. Just before $t_1$, the primary current is circulating through the switches $S_{a p \pi}$ and $S_{a n \nu}$. At time $t_1$, $S_{a n \nu}$ opens, and $S_{c n \pi}$ closes. The first term of (B.1) is the energy required to charge the capacitances of $S_{a n \nu}$ and $S_{c n \pi}$. The variation of voltage across each of these switches is $\sqrt{3} V_m$. The term $4/3$ comes from the square-root dependence of the output capacitance of the MOSFET on the drain-to-source voltage [D5]. The second term of (B.1) comes from the switch capacitances of $S_{b n \pi}$ and...
At time $t_1$, the voltage between point $n$ and phase $b$ changes from $\sqrt{3} \frac{V_m}{2}$ to $-\sqrt{3} \frac{V_m}{2}$. Due to the presence of the antiparallel diodes across each MOSFET, the variation of voltage across each of the two MOSFETs in $S_{bn}$ is $\sqrt{3} \frac{V_m}{2}$, and the output capacitance of each MOSFET is modified accordingly. The last term of (B.1) is the energy required to charge the parasitic capacitance of the transformer. The equations (4.18) and (4.19) are easily derived by regrouping terms in (B.1).
Appendix C. Isolated ZVS Buck Rectifier Design

Procedure and Example

Due to the complicated relationship between $T$, $L/k$, and $\Delta d$ the design of the converter has to be performed in several iterations. The design is illustrated on the example prototype built for the following specifications:

- maximum output power: 2 kW,
- output voltage: $V_0 = 50$ V, and
- input rms line voltage: $3 \times 208$ V.

From these specifications, $V_m = 170$ V, and $I_{P}^{\text{max}} = 40$ A.

(1) Switching frequency. The carrier period $T$ is 20 $\mu$s. As shown in Figure 4.6, in every carrier period there are four voltage pulses of $v_{pn}$. Therefore, the switching frequency is $1/(T/2) = 100$ kHz. This switching frequency has been determined by the maximum speed of the microprocessor system used to control the converter.
(2) **Transformer turns ratio.** A possible starting point of the design is to assume the value of \( D_m \) at low line. An initial choice for \( D_m \) is 0.8. This leaves ample room for \( \Delta d(0) \) and for duty cycle overshoots during transients. With this value of \( D_m \), the first iteration for the transformer turns ratio \( n \) can be calculated from (4.9).

(3) **Output filter.** The output filter resonant frequency is chosen at 7 kHz, to provide adequate attenuation of output voltage switching frequency ripple. Assuming a maximal output filter inductor current ripple, the output filter inductor can be calculated using (4.11). It is important to keep the current ripple relatively small, because as seen from (4.21) and (4.22), high ripple reduces the ZVS range of the converter. The output filter inductor was chosen to give a maximum of 20% ripple at full load, i.e., \( \Delta I_{max} = 8 \text{ A} \).

(4) **Output rectifier.** In designing the output rectifier, more careful consideration has to be given to the problem of snubbing the voltage across the rectifiers. The parasitic capacitances of the rectifier diodes form a resonant circuit with the leakage inductance of the transformer. This resonant circuit causes high-frequency ringing across the rectifiers as a response to step changes of secondary voltage. If not snubbed or clamped, the initial voltage spike across the rectifiers can be several times larger than the steady-state voltage, and therefore has to be removed. This problem also exists in the ZVS-FB-PWM dc-dc converter, and can be mitigated using an RC snubber, a passive clamp circuit, or an active clamp circuit [D5]-[D7]. In the three-phase rectifier circuit the active clamp cannot be used because pulses of \( v_s \) vary in
magnitude. In this design, both a passive clamp circuit and RC snubbers were used. The clamp circuit limits the first voltage spike across the rectifiers, and transmits a part of the energy to the output. The RC snubbers across the rectifiers damp the remaining oscillations. In this design, 200 V, 50 A rectifier diodes were used. Such high voltage rating is required because a center-tapped-secondary transformer has been used. The total power dissipated in the clamp and the snubbers does not exceed 5 W.

(5) Power switches. For this design, 400 V, 25 A MOSFETs were selected. The on-resistance of the selected MOSFETs is 0.2 Ω, and the output capacitance $C_M$ is 160 pF.

(6) Leakage inductance. In this design step the capacitance of the transformer $C_T$ is assumed, and the value of leakage inductance is calculated. This can be done in two ways. One can choose $\Delta d(0)$, and calculate the leakage inductance from (4.17). Another way is to choose ZVS range, calculate $I_{cr}$ from (4.22), and finally calculate $L_{lk}$ from (4.21). When the converter is designed to provide a wide ZVS range, the loss of duty cycle $\Delta d(0)$ is relatively large, which has to be compensated by the increase in the transformer turns ratio, $n$. This increases the current in the primary, and leads to reduction in efficiency. On the other hand, if the ZVS range is narrow, and the ZVS property is lost with relatively high currents in the primary, the parasitic inductances and capacitances in the primary circuit can cause ringing of voltage across the switches and increase switching losses. In this design the ZVS voltage range is retained to 40% of full load. With $I = 16$ A and $\Delta I_{\text{max}} = 8$ A, (4.22) gives
$I_{cr} = 3A$. Assuming the transformer capacitance of $C_T = 200 \text{ pF}$, the required leakage inductance is $L_{lk} = 8\mu\text{H}$. This value of $L_{lk}$ causes loss of duty cycle $\Delta d(0) = 0.11$ at full load.

This completes the first design iteration. The obtained circuit parameters can be checked against different design criteria (for example if $D_m + \Delta D(0) \leq 1$, etc.). If the results of the first iteration are not satisfactory, the assumed values of the circuit parameters have to be corrected, and the design has to be repeated until satisfactory results are obtained.

A series dc blocking capacitor of 5 $\mu\text{F}$ has been placed in series with transformer to prevent any dc current from building up in the transformer primary. A single-stage input filter with corner frequency of 10 kHz has been placed in front of the converter.
Appendix D. Implementation Details of the Controller for the Isolated ZVS Buck Rectifier

D.1 Generation of Gate Drive Signals

The twelve gate-drive signals \( g_{ap\pi} \) – \( g_{cnv} \) for the twelve converter switches \( q_{ap\pi} \) – \( q_{cnv} \), respectively, are generated in the decoder as logic functions of the PWM signals \( A-E \), the synchronization signal \( SY \), the operating mode code \( S_{10} \) – \( S_{15} \), and the protection signal \( WDT' \). Figure D.1 shows the converter primary voltage \( v_{pn} \), the signals \( A-E \) and \( SY \), the auxiliary synchronization signal \( S \), and the six auxiliary active-gate-drive signals \( x_1, x_2, y_1, y_2, z_1, \) and \( z_2 \). The auxiliary signals are internal to the decoder, and are used as intermediate signals in the synthesis of the gate-drive signals.

The PWM signals have a constant period of \( T/2 \). The rising edges of \( v_{pn} \) at \( t = 0 \) and \( t = T/2 \), coincide with the rising edges of the PWM signals \( A-E \).
Figure D.1. Controller principal waveforms.
All other edges of \( v_{pn} \) coincide with one of the falling edges of the PWM signals. In this way, a complete switching instant information is provided by the PWM signals. Within the first half-period from 0 to \( T/2 \), the switching instants are coded by the PWM generators \( A, B, \) and \( C \), while in the second half-period, from \( T/2 \) to \( T \), the instants are coded by PWM generators \( C, D, \) and \( E \). To distinguish between the two half-periods, the synchronization signal \( S \) is created from \( SY \) and \( C \) with an edge-triggered flip-flop. The signal \( SY \) is high only during the short time interval around the switching cycle boundary \( (T) \) and is software generated.

Within any 30\(^\circ\) segment, there are only six switches that are actively involved in the power conversion process. The remaining switches are either on throughout the entire interval, or their gate-drive signals are complements of one of the six active gate-drive signals. The active switch controlling signals, \( x_1 \), \( z_2 \), are derived from the PWM signals and \( S \) in a straightforward manner. For example, \( x_1 = SB + S'E, y_1 = S'E' \), etc., where '(' denotes a logic complement.

The so obtained active gate-drive signals are distributed to the proper switches using the segment information \( S_{10} - S_{15} \). Figure D.2 shows the distribution of the gate-drive signals as functions of the present 30\(^\circ\) segment, for all twelve converter switches. The table entry '1' means that the switch is kept on during the entire interval, and the table entry '1p' is identical to '1', except that the switch is opened when a protective shut-down occurs, i.e. when \( WDT = 0 \).
<table>
<thead>
<tr>
<th>angle (deg)</th>
<th>-30 to 0</th>
<th>0 to 30</th>
<th>30 to 60</th>
<th>60 to 90</th>
<th>90 to 120</th>
<th>120 to 150</th>
<th>150 to 180</th>
<th>180 to 210</th>
<th>210 to 240</th>
<th>240 to 270</th>
<th>270 to 300</th>
<th>300 to 330</th>
</tr>
</thead>
<tbody>
<tr>
<td>$qap\pi_x$</td>
<td>1</td>
<td>1</td>
<td>1p</td>
<td>$y_2'$</td>
<td>$z_1$</td>
<td>$x_2$</td>
<td>$y_1$</td>
<td>$y_1$</td>
<td>$z_2'$</td>
<td>1p</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$qap\pi_y$</td>
<td>$x_1$</td>
<td>$x_1$</td>
<td>$z_2$</td>
<td>$z_2$</td>
<td>$y_1'$</td>
<td>1p</td>
<td>1</td>
<td>1</td>
<td>1p</td>
<td>$y_2$</td>
<td>$z_1$</td>
<td>$x_2$</td>
</tr>
<tr>
<td>$qbp\pi_x$</td>
<td>1p</td>
<td>$z_1'$</td>
<td>$y_2$</td>
<td>$y_2$</td>
<td>$x_1$</td>
<td>$x_1$</td>
<td>$z_2$</td>
<td>$y_1'$</td>
<td>1p</td>
<td>1</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>$qbp\pi_y$</td>
<td>$z_1$</td>
<td>$z_1$</td>
<td>$x_2$</td>
<td>$x_2$</td>
<td>$y_1$</td>
<td>$y_1$</td>
<td>$z_2'$</td>
<td>1p</td>
<td>1</td>
<td>1</td>
<td>1p</td>
<td>$y_2'$</td>
</tr>
<tr>
<td>$qcp\pi_x$</td>
<td>$y_1'$</td>
<td>1p</td>
<td>1</td>
<td>1</td>
<td>1p</td>
<td>$z_1'$</td>
<td>$y_2$</td>
<td>$y_2$</td>
<td>$x_1$</td>
<td>$z_2$</td>
<td>$z_2$</td>
<td></td>
</tr>
<tr>
<td>$qcp\pi_y$</td>
<td>$x_2$</td>
<td>$x_2$</td>
<td>$z_1$</td>
<td>$z_1$</td>
<td>$y_2'$</td>
<td>1p</td>
<td>1</td>
<td>1</td>
<td>1p</td>
<td>$z_2'$</td>
<td>$y_1$</td>
<td>$y_1$</td>
</tr>
<tr>
<td>$qan\pi_x$</td>
<td>1</td>
<td>1</td>
<td>1p</td>
<td>$z_1$</td>
<td>$z_2$</td>
<td>$x_1$</td>
<td>1</td>
<td>1</td>
<td>1p</td>
<td>$z_2'$</td>
<td>$y_1$</td>
<td>$y_1$</td>
</tr>
<tr>
<td>$qan\pi_y$</td>
<td>1p</td>
<td>$y_1$</td>
<td>$z_2$</td>
<td>$z_2$</td>
<td>$x_1$</td>
<td>$y_1$</td>
<td>$y_2$</td>
<td>$z_1'$</td>
<td>1p</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$qbn\pi_x$</td>
<td>1p</td>
<td>$z_2'$</td>
<td>$y_1$</td>
<td>$y_1$</td>
<td>$x_2$</td>
<td>$x_2$</td>
<td>$z_1$</td>
<td>$z_1$</td>
<td>$y_2'$</td>
<td>1p</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>$qbn\pi_y$</td>
<td>$y_2$</td>
<td>$y_2$</td>
<td>$z_1$</td>
<td>1p</td>
<td>1</td>
<td>1</td>
<td>1p</td>
<td>$y_1'$</td>
<td>$z_2$</td>
<td>$z_2$</td>
<td>$x_1$</td>
<td>$x_1$</td>
</tr>
<tr>
<td>$qcn\pi_y$</td>
<td>$y_2'$</td>
<td>1p</td>
<td>1</td>
<td>1</td>
<td>1p</td>
<td>$z_2'$</td>
<td>$y_1$</td>
<td>$y_1$</td>
<td>$x_2$</td>
<td>$x_2$</td>
<td>$z_1$</td>
<td>$z_1$</td>
</tr>
<tr>
<td>$qcn\pi_x$</td>
<td>$z_2$</td>
<td>$z_2$</td>
<td>$x_1$</td>
<td>$x_1$</td>
<td>$y_2$</td>
<td>$y_2$</td>
<td>$z_1'$</td>
<td>1p</td>
<td>1</td>
<td>1</td>
<td>1p</td>
<td>$y_1'$</td>
</tr>
</tbody>
</table>

$s_0$ | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
$s_1$ | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
$s_2$ | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
$s_3$ | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
$s_4$ | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
$s_5$ | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |

*Figure D.2. Distribution of gate-drive signals.*
D.2 Controller Software

The listing of the controller program is shown in Figure D.3. Some of the instructions in the program are self-explanatory, so only the larger functional blocks of the program are described here. The first such block performs the reading of the A/D converters. All data obtained from the A/D converters has to be scaled to avoid overflow during later numerical manipulations. The scaling is also performed to prepare the data for writing into the PWM generators, i.e. full-scale input from the A/D converters provides a 100% duty cycle of the PWM output. Since the scaling has to be done, it is convenient to perform the multiplication of input voltage samples by $D_m$ at the same time. The input from the first converter is a sample of $D_m$. This sample is scaled, and the obtained scaled $D_m$ is used to multiply the samples of the input phase voltages.

The scaled samples of the input voltages are used to determine the present 30° segment. This is performed by determining the sign of all phase and line voltages. To minimize the number of load and store instructions, the calculation of phase and line voltages is performed in the high 16 bits of the accumulator, while the result is coded and stored in the low 16 bits of the accumulator. For example, on address $p1_s$, the sample $u_a$ is loaded into the high accu, and the low accu is cleared. If the sample $u_a$ is positive, bit 3 of the low accu is set, and if it is negative, bit 3 of low accu remains 0. Next, the sample $u_b$ is subtracted from the high accu, to create the sample of the line
Figure D.3. Controller Software Listing.
voltage $v_{ab}$, without changing the contents of the low accu. If $v_{ab}$ is positive, bit 0 of the low accu is set, etc. The similar procedure is repeated for the remaining phase and line voltages, until the coded input voltage 30° segment is stored in the variable \textit{SEGMENT}.

The \textit{MUX} function in Figure 5.1.a is performed by a subroutine call. The subroutine starting address is coded by the sign bits 3, 4, and 5 in the \textit{SEGMENT} variable. There are six subroutines, one for every combination of the input phase voltage signs, i.e., one for every 60° segment of the phase voltages. One of the subroutines, "seg0", is shown at the end of the program listing. The subroutine reads the values of the two input phase voltage samples to be used as references, $u_x$ and $u_y$, takes the absolute value, and returns $d_x$ and $d_y$ on the software stack, and in the low accu, respectively. The remaining five routines are similar. There are two additional subroutines that cover the illegal sign combinations that can occur at the converter input due to noise interference. One of the two subroutines, "fault" , is listed here, and it returns $d_x = d_y = 0$.

With $d_x$ and $d_y$ determined, the duty cycles for each PWM generator are calculated. The duration of the zero-voltage interval is calculated and stored in the variable \textit{half-zero}.
Appendix E. Input Filter Design Example

In this example, a per-phase filter for the three-phase PWM buck rectifier designed in Appendix C, is presented.

- The filter is designed according to the VDE 0871 'Class A' specifications which allow no more than $V_{EMI} = 74$ dB$\mu$V of switching noise at 100 kHz with $R_{lissn} = 50$ $\Omega$.
- The converter is producing $I_{sw} = 1$ A.
- This yields a required filter switching frequency attenuation of $A_{min} = 80$ dB.
- IDF is required to be $IDF \geq 0.94$ with $V_{lim} = 170$ V and $I_{lim} = 3.5$ A.
- This yields $C_{max} = 14$ $\mu$F.
- The filter order is chosen as $n = 4$ with $A_{max} = 1.25$ dB.
- The normalized filter parameters are [H2, pp. 200-201] $\Omega_2 = 4.89$, $L'_1 = 1.11$, $L'_2 = 0.03$, $L'_3 = 1.96$, $C'_2 = 1.36$, and $C'_4 = 1.25$. 
• The reference frequency is $\omega_r = 109217$ rad/s.

• The damping resistor is $R_d = 1.7$ $\Omega$.

• The denormalized filter parameters are $L_1 = 17$ $\mu$H, $L_2 = 0.5$ $\mu$H, $L_3 = 30$ $\mu$H, and $C_2 = C_4 = 7$ $\mu$F.

• The active damping is implemented with $n_1 \approx n_2 = 50$, which gives $R = 4.3$ k$\Omega$. The magnetizing inductance of T1 is $L = 16$ mH. Since the lowest filter pole is at 5 kHz, the L-C corner frequency is chosen at 550 Hz, which gives $C = 5.2$ $\mu$F. The damping scheme is implemented with the PA26 power operational amplifier, [12].

• The damping circuit zero frequency is $f_{2z_r} = 7.1$ Hz.

• If passive damping of Figure 6.3.d is used, and the $R_d - L_d$ corner frequency is 1 kHz, $L_d = 250$ $\mu$H.
Vita

The author was born on January 12, 1963, in Novi Sad, Yugoslavia. He received his B.S. degree in electrical engineering from the University of Novi Sad in 1987. From 1987 to 1989 he was employed as a teaching and research associate the Institute for Power and Electronics, University of Novi Sad, where he worked on projects involving control of industrial machines and development of the Radio Data System, and assisted in teaching of Semiconductor Physics and Microprocessor Architecture. In 1989 he began studying at Virginia Tech and received his M.S. degree in electrical engineering in 1991, concentrating on modeling, analysis, and design of soft-switching dc-dc converters. Since 1991 his research was mainly in the area of high-frequency power conversion techniques for three-phase converters. In 1993 he was awarded the "Outstanding International Student Award" by the Bradley Department of Electrical Engineering, Virginia Tech, for academic and research excellence. The results obtained during his doctoral study led to issuing of a
U.S. patent for the ZVS isolated buck rectifier and filing of three more patent applications.