HIGH POWER SHUNT REGULATION OF SPACECRAFT SOLAR ARRAYS

by

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(ABSTRACT)

The operation of the basic shunt system for solar arrays is considered. The system is analyzed for stability with a constant power load. The implications of using switching type shunt elements for high power outputs are investigated.

The input filter is shown to affect the closed loop design of the system, as well as its weight. Analysis and modeling techniques are developed for a sequential shunt unit. The analysis of bus impedance and loop gain is verified against measurements on hardware. The factors that affect the design are described. The effect of non-linearities in the system is shown to cause limit cycle operation.

For more effective use of the input filters, alternatives to the existing scheme are considered, where the on-off and fine control sections are kept distinct. The basic requirements of the scheme are shown to be the suppression of on-off section current, and the inclusion of hysteresis in the control loop.
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Chapter 1: INTRODUCTION AND OVERVIEW

1.1. Objectives and scope of this work

Photovoltaic power systems with battery storage are the primary power source for earth orbiting spacecraft [32]. The trend in satellite power requirements has steadily increased, from 28V systems of a few hundred watts to an expected level of up to 1MW [1, 25, 29]. Power distribution efficiency considerations require the use of higher system voltages, up to 200 V. Much of the existing literature for regulation of spacecraft photovoltaic power is based on low voltage systems operating with small solar cells, often with linear control elements. Future needs call for higher power levels, where the regulator must be lightweight and efficient. These systems are also required to comply with more stringent specifications for bus quality, electromagnetic interference (EMI), etc.
Greater power densities necessitate the use of switching, rather than linear control elements. Tests based on hardware for switching shunt regulators have brought out a number of issues related to higher power systems. These are the effect of array capacitance on switching, input current ripple, instability due to the use of input filters, and system weight. These considerations have been published in [13, 14].

The main objectives of the present work are:

1. to identify the options for high power switching shunt regulators
2. to examine stability aspects
3. to determine the factors that influence the design
4. and to explore possible alternatives to existing shunt configurations.

First, the general features for a single section shunt stage are discussed in chapter 2. These relate to:

- Power dissipation
- Small signal stability
- Output impedance
- Implications for a switching type regulator
For high power levels, a large number of such single units must be operated in a multistage arrangement. The general features discussed in chapter 2 are next applied to the design of a sequential shunt switching unit (SSU) in chapter 3. The unit is modeled and the analysis compared with hardware test results. The factors that affect this design are identified, such as the effect of input filters on the stability of the system, and on the weight of the regulator. Finally, chapter 4 considers possible steps that can be taken to overcome these factors, and explores other alternatives.

1.2. Literature survey

Typical photovoltaic systems (Fig. 1.1(a)) consist of a solar array and regulator, together with a battery to store power for dark periods [20, 22, 27]. The battery is interfaced to the bus via a charge-discharge regulator. The available literature on shunt regulators is described below, mainly from the point of view of switching applications for high power use.
1.2.1. Solar array characteristics:

Conventional spacecraft arrays consist of crystalline silicon solar cells connected in series to provide the required voltage, forming a "string". A number of such strings are operated in parallel to provide the required current [4].

The V-I characteristic and equivalent circuit for a single string is shown in Fig. 1.1(b). The short circuit current $I_s$ is proportional to the illumination level. Both the short circuit current and the open circuit voltage $V_{oc}$ depend on the temperature, and decrease with aging. The working life of a typical array may extend from 5 [24] to 15 years [26]. The array is suitably oversized at the beginning of life (BOL) to ensure sufficient power at the planned end of life (EOL). Simulators used for the solar array are described in [5,12].

The solar cell dc characteristic is modeled [4] by the following implicit equations:

$$\begin{align*}
    i &= I_p - I_s \exp(v_p/v_T) - \frac{v_p}{R_p} \\
    v_p &= v - iR_A
\end{align*}$$

where

$$v = \text{cell output voltage}$$
Figure 1.1. The shunt regulator and characteristic for the solar array
\[ i = \text{cell output current} \]
\[ I_s = \text{reverse saturation current of the diode} \]
\[ v_T = \text{thermal voltage (0.026 V)} \]
\[ v_D = \text{diode voltage} \]

The entire array is modeled by scaling the impedance levels up by the number of cells connected in series.

Solar arrays have a parasitic output capacitance \( C_a \), as shown in Fig. 1.1(b), which must be considered for switching regulators. The theoretical basis for this capacitance is discussed by Zerbel and Decker [6]. Reference [5] provides an equivalent circuit for the array that includes a user-adjustable cell capacitance. However, no procedure is given to evaluate it. Measures to improve cell efficiency have resulted in larger capacitances for high power arrays [7]. Measured values for such arrays are provided in [2], where the capacitance is shown to be around 0.02 \( \mu \text{F} \) for a 240V, 2.5 A array string. The most recent data indicates that the value is a function of the array voltage, and of aging.

Due to the presence of the array capacitance, the effect of a switching regulator is to cause input current surges. Fleck and Lepisto [11] describe a 120 V, 10 kW sequential shunt unit which was field tested on a solar array. A current surge of 13 A was observed due to the array capacitance discharge. In addition to causing peak current stress in the switch, it is now recognized that the current surge must
also be suppressed to avoid electromagnetic interference. A specification for input current ripple is provided in [38]. The array capacitance is found to be a significant driving factor in the design of higher voltage systems [7,13]. The implications of this capacitance are discussed more fully in chapter 3.

1.2.2. Regulator topologies

Solar array elements and the associated controlling element have been grouped by Decker and Cassinelli [10] into four configurations, shown in Fig. 1.2. The controlling element may be a linear device, or an on-off switching element [19]. The merits of the four possible schemes are described in [9, 18]. The array configuration used depends on the application.

The main driving factors for earlier designs were dissipation in the linear controlling device, transistor voltage ratings, etc. With the availability of high voltage MOSFETs and the introduction of switching regulators, dissipation can be reduced. However, switching regulators add electromagnetic noise, which can interfere with telemetry signals.
Figure 1.2. Classification of array regulators
With increasing power levels, the evolution has been towards modular approach called *sequential switching* [3, 30, 15, 16, 17]. The advantages of the scheme [30] are:

- The output voltage ripple is kept low by fine switching of only one array section. Thus, the bus filter equivalent of only one module is required.
- The loss of one module does not affect bus voltage and can be easily tolerated.
- The modular design can be easily expanded to higher power requirements.
- Due to on-off operation of most devices, the power dissipated aboard the spacecraft is only a small fraction of the total power controlled [18].

This sequential technique uses either configurations (c) or (d) in Fig. 1.2, i.e., each array segment is capable of supplying the full voltage and the number of segments connected to the load depends on the required load current. The difference between the two configurations is the **series** or **shunt** connection for the controlling element.
1.2.3. Series vs shunt regulation

Figure 1.3 compares idealized operation of one array element under series and shunt switching, with on-off rather than linear operation. The shunt arrangement requires the use of blocking diodes to isolate array sections.

With the shunt switch, the array element is subjected to the excursion AB on the array characteristic, with every switching operation. The current is almost unchanged but a rectangular voltage is impressed on the array due to switching. With the series switch, the array makes the excursion BC along the array characteristic.

Peak current requirements are identical for both switches. The series switch must block a voltage

\[ V_d = V_{OC} - V_B \]  \hspace{1cm} [1.2.3]  

where \( V_B \) is the bus voltage and \( V_{OC} \) is the open circuit voltage of the array. The shunt switch must be rated for the full bus voltage \( V_B \). The current output to the bus capacitor and load is similar in both cases.

With linear control elements, there would be a dissipation of
Figure 1.3. Series vs shunt regulation with a switching element
\[ P_{SHUNT} = V_R(I_P - I_L) \]  

\[ P_{SER} = I_L(V_OC - V_R) \]  

With switching elements, this amount of dissipation is avoided inside the spacecraft, and a much smaller switching loss is added.

The series switching operation inherently draws pulsed current at the input. However, such series switching is often used in lower power systems [39]. The electromagnetic noise due to the pulsed current is reduced by slowing the MOSFET switching speed with a drain to gate capacitor.

Ideally, the shunt circuit does not need a filter, but an inductive filter must be used due to the parasitic array capacitance. This is discussed more fully in chapter 3. The effect of the filter is to smooth the array voltage waveform as well. Instead of the rectangular voltage, the array is now at a constant voltage \( D'V_R \), with some residual ac ripple.

With the commonly used topologies shown in Fig. 1.3(a) and (b), the series switch operates at lower voltage, but due to the pulsed input current it has an inherently larger input filter requirement. The shunt switch is therefore more widely used.
Special considerations may, however, require the use of a series switch, such as the ability to interrupt an arc [10].

The topologies in Fig. 1.3(a) and (b) use identical output filter configurations and differ only in that the series circuit has a pulsed input current. With switching regulators operating at duty ratio $D$, the shunt circuit (a) requires the array to operate at an average voltage of $D'V_n$, which is within the region AB marked on the characteristic. The array characteristic can be viewed also as a voltage source for the series switch. If an attempt is made to filter the series circuit as a voltage chopping buck configuration (Fig. 1.3(c)), a problem arises. If the overall configuration is of the type (c) in Fig. 1.2, the array is required to operate at a voltage of $V_s/D$, which is much larger than $V_n$ at small duty ratios. This large voltage does not exist on the array characteristic (Fig. 1.2). The individual string configuration (c) is therefore feasible only in the overall series system configuration of Fig. 1.2(b), where the individual string is not constrained to operate at a voltage $D'V_n$. This configuration requires complex make before break switching.

The series configurations also require floating switches, which are not simple to control down to dc (continuously on or off). With these remarks about the possible cases where series switches may be used, the rest of the present work focuses on the use of shunt switches only.
1.2.4. The partial shunt topology

The partial shunt circuit is shown in Fig. 1.4. The solar array is divided into two sections in series and only the lower section is shunted by the controlling element. This circuit has been used [8] in low power applications from 100 to 1200 W.

The main advantage of the circuit is that with a linear control element, instead of a dissipation of $V_p (I_p - I_l)$, the dissipation is only:

$$P_{PAR} = (V_R - V_U) (I_p - I_L)$$  \[1.2.6\]

where

$V_R = \text{bus voltage}$

$V_U = \text{voltage of upper section of array}$

$I_L = \text{load current}$

The circuit can be adapted to switching [8, 11] by using an on-off switch across the lower section, instead of a linear device. The lower section accounts for a fraction $m$ (typically about 2/3) of the total voltage. The array capacitances are $C_U$ and $C_L$ for the upper and lower sections. Because fewer sections are in series, these must be scaled up from the full array value $C$, i.e.,
Figure 1.4. The partial shunt system
\[ C_U = \frac{C_A'}{(1 - m)} \]  
\[ C_I = \frac{C_A}{m} \]  
[1.2.7]  
[1.2.8]

The capacitances \(C_A\) and \(C_A'\) are different because the average operating point on the characteristics are generally different for the two sections. When the switch is open, the full array is at \(V_\text{n}\) and the lower section is at \(mV_\text{n}\). The capacitances are charged to \((1 - m)V_\text{n}\) and \(mV_\text{n}\) respectively.

On closing the switch, the lower section is at 0 V and the switch lead is subject to the input current surge due to \(C_I\). However, \(C_U\) cannot discharge due to the blocking diode. It charges to a value \(V_{ocu}\), where \(V_{ocu}\) is the the open circuit voltage of the upper section only. On opening the switch, \(C_I\) charges from 0 to \(mV_\text{n}\) and \(C_U\) discharges from \(V_{ocu}\) to \((1 - m)V_\text{n}\).

The switching scheme is not competitive if filters have to be included in two lines for each string. Also, the lower section is usually sized for a large fraction of the bus voltage, so there is not a particularly appreciable change in capacitance and input current ripple as compared to a full shunt. However, due to the lower voltage swings, the \(\frac{1}{2}CV^2\) energies are smaller. Thus, it may be viable to place a small inductive filter in the upper line (where there is no switch) and to absorb the surge energy of the lower section in the switch. Absorbing the energy of the
surge in the switch is an alternative to the use of a filter [30]. This technique is also used in chapter 4. One further disadvantage of the partial shunt circuit is that it requires an extra lead to be brought in from the array, resulting in one more slip ring.
Chapter 2: SHUNT SYSTEM ANALYSIS

2.1. Introduction

This chapter examines solar array shunt regulation in general terms and describes the method for analyzing the system. The shunt operation principle is described first, followed by consideration of the dynamic characteristics. The stability of the shunt regulator is analyzed with a load connected to the system. A method of analysis and design of shunt regulator systems for stability and optimum dynamic performance is discussed. The shunt system can be regulated using either a proportional compensator, or a proportional-integral compensator to obtain zero steady state error. The parameter design for both types of compensators is described.
The differences in analysis and design for switching shunt regulators are examined. It is shown that despite the use of additional reactive components for the filters, the switching shunt also follows the same general principles. The analysis approach described in this chapter is applied to the specific case of a switching regulator in chapter 3.

2.2. Control concept: operation of regulator

The mode of operation of a solar array regulator can be described as shown in Fig 2.1. The macro model for the array equivalent circuit is shown in Fig. 2.1(a). At low voltage, the real diode does not draw any current and almost constant current is output from the array. At higher voltage, the diode begins to conduct and limits the array output voltage to a value equal to the conduction drop of the diode. A higher voltage array is represented by a number of diodes in series, and impedance levels are scaled up by the number of cells in series [4].

The main elements of the array equivalent circuit are:

\[ R_o = \text{dynamic resistance of the array} \]

\[ R_a = \text{series resistance of the array} \]
\( I_r = \text{array short circuit current} \)

A diagram of a shunt regulator system is shown in Fig. 2.1(a). The array, the shunt control element, and the bus capacitor are in parallel, and connected to the bus voltage, \( v_b \). The array operates in the constant current region, where the dynamic resistance \( R_b \) is large.

The bus voltage \( v_b \) is sensed and used to control the amount of current \( i_s \) that is shunted by the control element. Thus,

\[
i_s = Y_R(s)v_b
\]  

[2.2.1]

where \( Y_R \) represents the current shunted per volt of bus voltage error. \( v_b \) and \( i_s \) are incremental (small signal) quantities.

This equation indicates that the shunt regulator, including the compensator, can be represented [35, 23, 34] by placing an admittance of value \( Y_R(s) \) across the array as shown in Fig. 2.1(b). This admittance element \( Y_R(s) \) represents the regulating action of the control element, and includes the effect of the error amplifier as well.

The complete array and shunt regulator system is represented by the small signal equivalent circuit in Fig. 2.1(b). \( Z_a \) is the array output impedance. It is very large in the current source region. The closed loop system has a limited frequency re-
(a) Solar array and shunt regulator

(b) Small signal unterminated equivalent circuit

Figure 2.1. Shunt regulator operation

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sponse, which is included as the frequency dependence of the element \(Y_a(s)\). This is mainly due to the finite bandwidth of the compensator. The output impedance of the entire system is \(Z_o\), which consists of the array, the regulator, and the bus capacitor, \(C_b\), in parallel.

The closed loop bus impedance provided by the system depends largely on the admittance \(Y_a(s)\) within the regulator bandwidth. At higher frequencies, the admittance is decided by the bus capacitor, \(C_b\). A large value of \(Y_a(s)\) represents a stiff voltage source which provides a quality bus against load disturbances. It is possible, for instance, to shape the \(Y_a(s)\) with an integrator so as to retain a high value at low frequency, while reducing it at high frequency to provide a suitable stability margin. This produces a regulated system with zero steady state bus voltage error on load.

The closed loop design and stability can now be investigated by considering the circuit shown in Fig. 2.1(b). Unterminated by a load, the output impedance of the system is

\[
Z_o = \frac{Z_{OL}}{1 + Y_a(s)Z_{OL}} \tag{2.2.2}
\]

where the open loop impedance \(Z_{OL}\) is the impedance \(Z_d\) in parallel with the bus capacitor impedance. Since \(Z_d\) is large, \(Z_{OL}\) is approximately the same as the bus capacitor impedance.

Chapter 2: SHUNT SYSTEM ANALYSIS
The expression $Y_R(s)Z_{ol}$ may be identified as the loop gain of the system. The stability and dynamic performance of the load unterminated shunt regulator can be analyzed using the loop gain $T = Y_RZ_{ol}$.

### 2.3 Closed loop design

The shunt system identified in section 2.2 may be analyzed using the equivalent circuit in Fig. 2.1(b). The components of the regulator admittance $Y_R$ are shown in Fig. 2.2(a). These consist of the compensator transfer function $A(s)$ and the conductance $G_K$, which is the current shunted per volt of control voltage $v_C$, by the shunting element. Thus,

$$Y_R(s) = G_K A(s) = \frac{i_S}{v_R} \quad [2.3.1]$$

For the error amplifier function $A(s)$, two representative feedback compensators, the proportional and proportional integral types (Fig. 2.2(b)) are considered. Circuits for implementing these are discussed later in chapter 3.6 (Fig. 3.10). The compensator gains $A(s)$ can be written respectively as:

$$A_B(s) = \frac{A_M}{1 + s/\omega_C} \quad [2.3.2]$$

Chapter 2: SHUNT SYSTEM ANALYSIS
\[ A_{Pl}(s) = \frac{A_M(s + \omega_C)}{s(1 + s/\omega_C)} \]  \hspace{1cm} [2.3.3]

where

\[ \omega_C = \text{cutoff frequency} \]

\[ \omega_Z = \text{zero for integrating compensator} \]

\[ A_M = \text{gain of the proportional compensator or the midband gain of the proportional-integral compensator} \]

Figure 2.2(c) shows the closed loop design procedure using equations 2.2.2, 2.3.1, and 2.3.2. The open loop impedance \( Z_{ol} \) is that of the bus capacitor, with the addition of a very low frequency pole at the \( \omega_t = 1/CR_p \) corner due to the dynamic resistance \( R_p \). It has a high frequency zero at \( \omega_o = 1/CR_c \) due to the equivalent series resistance (ESR), \( R_c \). \( Y_r \) is plotted for both types of error amplifier, with the integrating type shown dotted. The loop gain \( T \) is the product of \( Z_{ol} \) and \( Y_r \). Finally, the closed loop bus impedance is obtained as per equation 2.2.2, using the loop gain and the open loop impedance.

Proportional compensator design is straightforward. The required low frequency value of the bus impedance is selected as a suitable feedback gain \( 1/Y_r \). The cutoff frequency of the error amplifier \( \omega_c \) must be chosen to be larger than the ESR zero of the bus capacitor. Beyond this zero, the loop gain may be very small if low
(a) Components of $Y_R$

(b) Proportional and integrating compensators

(c) Closed loop design by shaping the loop gain

Figure 2.2. Closed loop design considerations
ESR capacitors are used. Above the frequency at which the loop gain falls to unity, the $Z_o$ essentially follows the open loop impedance $Z_{ol}$, i.e., it becomes equal to the ESR in value. If the ESR is very small (e.g. 0.001 ohm with polypropylene capacitors) $R_e$ will be lower than typical low frequency values for $Z_o$.

The response with a proportional compensator is shown in Fig. 2.3. The bus voltage is regulated at 120V. A constant power load step of 180 W to 200 W is applied at .001 sec. The low frequency value of $Y_r$ is chosen to be 0.2 A/V in this example, though it will generally be larger. The error amplifier has a cutoff frequency of 5 kHz.

It is often required to regulate the bus more tightly, in order to maintain a very small voltage band for shunt regulation. This may be necessary for coordination with other regulating elements in the system, such as a battery discharge regulator [21, 20]. An integrating compensator may be used to reduce the steady state error to zero. With the integrating compensator, the loop gain $T$ assumes a 40 dB/decade slope. This must be corrected by the addition of a low frequency zero, $\omega_z$, in $Y_r$. This zero must be chosen well below $\omega_e$ to preserve the phase margin. By choosing it one decade lower (at 500 Hz in the example), the phase margin is similar that of a proportional compensator (about 90°).
Figure 2.3. Response to a step load change with proportional control
The response with the integrating compensator is indicated in Fig. 2.4. It is seen that the settling time is governed by the longer time constant, corresponding to $1/\omega_z = 0.322$ msec. The bus voltage is therefore seen to settle at the new value after about 4 such time constants, or .0012 sec. A faster response time is possible with a larger $\omega_z$, at the expense of decreased stability margin.

### 2.4. Design and stability analysis using impedance interaction

The design using the unterminated loop gain $T$ may be checked for stability for any given load input impedance by using impedance interaction analysis. Figure 2.5(a) indicates the connection of two systems, with $Z_o$ as the source impedance of the shunt regulator system and $Z_l$ as the input impedance of the load subsystem. On connecting the two systems, the looking-in impedance at the interface is seen to be:

$$Z_{BUS} = \frac{Z_o Z_l}{Z_l + Z_o} = \frac{Z_o}{1 + Z_l/Z_o} \quad [2.4.1]$$
Figure 2.4. Response to a step load change with proportional-integral control
The impedance ratio $Z_o/Z_L$ is referred to as the system loop gain and it represents a feedback mechanism between the source and load subsystems [28]. For assessing stability, the Nyquist criterion can be applied to the loop gain $Z_o/Z_L$.

The load impedance $Z_L$ typically consists of a constant power load preceded by an input filter as shown in Fig. 2.5(b). When the entire shunt system is considered as the source subsystem, the impedance $Z_o$ is that of a voltage source. The stability criterion requires that the $Z_o$ curve should lie below the $Z_L$ curve. The closed loop impedance $Z_o$ should be suitably shaped using the procedure in section 2.3 above to ensure this.

2.5. Implications for switching shunts

The design considerations in section 2.2 are directly applicable to linear shunts, where the shunt element $Y_r$ represents actual power loss, as indicated in Fig. 2.6(a). At high power levels, a switching regulator is necessary because, ideally, it does not involve power loss and the consequent need for large on-board heatsinks.
(a) Load and source impedances for analysis

(b) Load and source impedance plots

Figure 2.5. Impedance interaction analysis using load and source impedances
For the switching shunt (Fig. 2.6(b)), the bus voltage $V_R$ is now no longer the same as the array voltage $V_A$. This is a fundamental difference from the linear case and it allows the switching regulator to shunt the current without actually dissipating power. The regulator can be viewed as a DC transformer interposed between $V_A$ and $V_R$ with a transformation ratio of $D' : 1$ At the input side, the array provides the same current $I_A$ as the linear case, but at an average voltage of $V_A = D'V_R$, where $D' = 1 - D$, the fraction of the switching period for which the switch is open. At the output side, the current is $D'I_A$. The difference current $DI_R$ is shunted at the "A" terminal of the transformer. The input and output powers at the transformer are:

$$P_{IN} = I_A(D'V_R) = P_{OUT} = V_R(D'I_A)$$

[2.5.1.]

These power levels are indicated diagrammatically in Fig. 2.6(c), which may be compared with Fig. 2.6(a) for the linear shunt.

The voltages and currents considered above are average values. Due to the switching action, the actual input voltage and the output current are pulsating. An input filter is required to smooth the array voltage and the bus capacitor acts as an output filter by smoothing the output current ripple (Fig. 2.6(b)). The bus capacitor in this case is chosen based on the filtering action. This is discussed in Chapter 3. In general, the bus capacitor is essential for stability [31, 33].
Figure 2.6. Considerations for a switching type shunt
The average operating point on the array characteristic shifts to \( V_a \) on the array characteristic, which is on the same constant power curve as the load (Fig. 2.6(c), assuming a lossless converter).

The switching regulator input filter adds a series impedance between the array and the shunt unit. As shown in Fig. 2.7, it is necessary to analyze the dynamic interaction between the array-filter output impedance and the input impedance of the shunt unit (interface A), in addition to the load-source interaction at the output (interface B). In this case, the Nyquist criterion must be applied to the impedance ratio \( Z_s/Z_{iw} \), where \( Z_s \) is the array-filter impedance and \( Z_{iw} \) is the input impedance of the regulator. It may be noted that in this case (interface A), a current source (solar array output) is connected to the low impedance input of the switching regulator, which is a dual of the case where a low impedance voltage source is connected to a higher impedance load. In other words, in order to avoid the impedance interaction, \( Z_s \) must be much larger than \( Z_{iw} \) for stability.

Except for the conservation of power, it can be shown that the output impedance of the switching regulator is similar to that of the linear shunt, and is largely decided by the controller gain. It is shown in chapter 3 that the output impedance of the switching shunt is of the form:

\[
Z_O \approx \frac{1}{I_{pk}(s)} \tag{2.5.2}
\]
Analysis approach using impedance interaction

Figure 2.7. Impedance interaction analysis for a switching shunt
where

\[ d' = -k(s)v_B \tag{2.5.3} \]

Here \( k(s) \) is transfer function from bus voltage error to the control duty ratio, and is analogous to the expression \( G_kA(s) \) for the linear case. The components of \( k(s) \) are the compensator gain \( A(s) \) and the duty modulator function \( d'/v_c \), where \( V_r \) is the PWM ramp amplitude. The equivalent \( Y_R(s) \) of this system is:

\[ Y_R(s) = k(s)I_p \tag{2.5.4} \]

One more essential difference from the linear case is that this admittance is a function of \( I_r \), the short circuit current of the array. In the linear shunt, the \( G_k \) component of \( Y_R \) is independent of \( I_r \). The switching regulator characteristics are therefore liable to change with the illumination level at the array.

2.6. Summary of shunt system analysis

The output characteristics of the shunt regulator are shown to be largely decided by the feedback gain and the bus capacitor. The shunt regulator system is analyzed above for stability with a load, using load-source impedance interaction. General design using proportional and integrating amplifiers is presented.
The switching shunt is shown to follow the same principles, i.e., the output characteristics depend on the feedback gain. Due to the presence of the input filter, it is necessary to analyze the stability at two interfaces, using impedance interaction. The PWM unit of the switching shunt can be treated as an unterminated two-port for an optimum design approach. Stability analysis for the switching shunt indicates that due to the presence of the input filter, a dynamic interaction may take place unless the array-filter output impedance is kept high.
Chapter 3: MODELING, ANALYSIS AND DESIGN OF A SHUNT SWITCHING UNIT

3.1 Introduction

This chapter discusses the design and analysis aspects for a shunt switching unit. The factors that affect the design are investigated. The unit is modeled and analyzed and the test results from hardware are compared with the analysis. The test hardware consists of 22 strings driven by a solar array simulator [12] with a short circuit current of 2.5 A per string. A fixed capacitance of 0.02 uF [2] is included at the array simulator output, for each string. The bus voltage is regulated at 120 V.
The sequential switching arrangement [15, 30] is used, but fine control is achieved by fixed frequency PWM operation of one of the strings. As discussed in chapter 2, the presence of the array capacitance in a high voltage system causes certain problems which have not been addressed earlier in the literature. These are:

- input current surges, and the need to include an input filter
- the effects of the input filter on stability

The solar array capacitance and the input filter have an important role in SSU design. The presence of an input filter affects the closed loop dynamics in control design. In particular, the system stability is shown to deteriorate at small duty ratio $D$ and low illumination levels.

The following sections discuss input filter design, the equivalent circuit, the input current ripple, and the small-signal stability analysis of the system. It is also shown how non-linear effects serve to limit an unbounded response at the unstable operating points.
3.2 Input current surge problem

One of the driving factors in the design for a switching shunt regulator for a solar array is the \textit{capacitance} of the array. This parasitic capacitance causes input current surges if shorted by the shunt switch. The current surges take place in the long wires connecting the array to the regulator and are a source of electromagnetic noise and component stress. These surges must be suppressed by the use of input filters which, in turn, have an influence on the design of the closed loop.

Figure 3.1 shows one solar array string connected to the shunt switch. When the switch is open, the array capacitance $C_r$ is charged to the bus voltage $V_b$. When the switch closes, this capacitance is effectively shorted, causing a current spike limited only by the connecting wire impedance. On opening the switch again, the solar array current $I_r$ must first charge the capacitance to $V_b$ before any current can flow towards the SSU, resulting in a current dip.

Reference [11] describes a similar current surge of 13 A when a 10 kW, 120 V shunt unit was field tested on an actual solar array. In Appendix 1, it is shown that an upper bound for the current spike is:
\[ I_p = \frac{2V_B}{\sqrt{L_A/C_A}} \]  

where \( C_A \) is the solar array capacitance, \( L_A \) the stray inductance of the connecting wire, and \( V_B \) is the bus voltage. The actual current spike will be smaller than this value due to circuit resistance, and the resonant oscillations are rapidly damped out.

To overcome this problem, a filter consisting of a series inductor is included. By using a suitably large inductor, the current surge can be suppressed to a small ripple. Figure 3.2 shows the experimental results where a 2 A surge is reduced to a ripple of 250 mA by using a series inductor of 2 mH. The switching frequency is 45 kHz. With this filter, the array capacitor voltage does not vary from 0 to \( V_B \), but is approximately constant at \( D' V_B \), where \( D' \) represents the fraction of the duty cycle for which the switch is open.

In Appendix 1, state trajectory analysis is used to derive an expression for the peak to peak residual ripple. At \( D' = 0.5 \), and for a switching frequency greater than the resonant frequency, the ripple is given by:

\[ I_{r,p} = \frac{V_B}{\sqrt{L_f/C_A}} \tan \left( \frac{T_s}{4\sqrt{L_f/C_A}} \right) \]  

provided
(a) Shorting of array capacitance by the shunt switch

CA = 0.02 μF, VB = 120 V, sw frequency = 16 kHz

(b) Input current surge without a filter

Figure 3.1. Input current surge problem
where \( T_s \) is the switching period and \( L_f \) is the filter inductance. This expression can be verified with reference to Fig. 3.2.

If the switching frequency is high compared to the array-filter resonance frequency, i.e., \( T_s < \frac{\sqrt{2}}{C_a} \), then this expression can be simplified to:

\[
I_{PPMAX} \approx \frac{V_s T_s}{4 L_f}
\]  

[3.2.3]

The above expression assumes a constant array capacitance. Empirical data indicates that the array capacitance is usually not a constant, but varies with the array voltage and the illumination level. A representative simulation using available data is shown in Fig. 3.3. The array voltage with a filter is \( D' V_s \). With a constant capacitance, the maximum ripple takes place at \( D = 0.5 \). However, if the capacitance increases with array voltage, the maximum ripple takes place at a higher value of the capacitance (higher \( D' \)). The simulation in Fig. 3.3 indicates that this takes place at around \( D' = 0.75 \). Another feature of the non-linearity of the capacitance is that the array voltage ripple maximum does not coincide with the input current ripple maximum. These take place at different duty ratios.
Figure 3.2. Input current ripple with a filter
In addition to the input current ripple, it is necessary to consider the bus voltage ripple at the output. This is given [14] by:

\[ V_{pp_{MAX}} = I_p R_C + D'(1 - D') \frac{T_s I_p}{C} \]  \[3.2.4\]

Here, \( I_p \) is the array short circuit current and \( C \) is the bus capacitance. The first term represents the effect of the bus capacitor ESR, \( R_C \). The second term shows the effect of the size of the bus capacitor. The maximum voltage ripple is obtained by substituting \( D' = 0.5 \) in the above expression. Figure 3.4 shows the experimentally measured bus voltage ripple.

### 3.3 Input filter design

Given a ripple specification, the filter inductor can be chosen using Eq. 3.1.3 for a specified switching frequency. The filter inductor is also required to sustain a DC current component of value \( I_r \), which is the short circuit current of the array.

For the testbed hardware, with

\[ I_{rp} = 200 \text{ mA (specified ripple)} \]

\[ C_s = 0.02 \text{ uF} \]
Duty ratio \( D = 1 - D' \)

Array voltage ripple

Input current ripple

Simulation for input current ripple with varying duty ratio. A voltage dependent array capacitance was used, based on available data.

Figure 3.3.  Variation of input current and input voltage ripple with duty ratio
Figure 3.4. Measured bus voltage ripple at the SSU output
\( T_s = 1.1 \text{ us, (switching frequency } = 90 \text{ kHz).} \)

\( V_s = 120 \text{ V,} \)

the required inductor is 1.7 mH. The inductors used in the hardware are wound on air-gapped Metglas cores, allowing a DC current of 2.5 A. The inductance used is 2 mH.

The filter must be duplicated in all the sections and it is desirable to use the smallest possible inductor. Further reduction in ripple is possible by using an additional shunt capacitor as shown in Fig. 3.5(b). This divides the input current ripple between the array capacitance \( C_A \) and the filter capacitor \( C_F \), so that

\[
I_{pp} \approx \frac{C_F}{C_F + C_A} \frac{V_B T_s}{4 L_F} \tag{3.2.5}
\]

The complete design of either filter also requires suitable damping circuits due to control considerations which are discussed more fully in Appendix B.

The array circuit resistances \( R_a \) and \( R_s \) cannot be augmented to provide damping because they directly affect DC efficiency. A separate damping resistor \( R_{db} \) is required. This is isolated for DC using the capacitor \( C_p \). This circuit is analyzed in detail in Appendix B, where it shown that the optimal choice of damping components is:
Figure 3.5. Damping circuits for input filters
\[ C_D \gg C_A. \quad [3.2.6] \]

and

\[ R_{CD} = \sqrt{\frac{L_F}{C_A}} \quad [3.2.7] \]

For the above design example, with \( L_F = 2 \text{ mH} \) and \( C_A = 0.02 \text{ uf} \), suitable values for \( R_{CD} \) and \( C_D \) are 316 ohms and 0.2 uF, respectively. After choosing the inductor, the more accurate expression Eqn 3.2.2 should be used to compute the ripple.

### 3.4 Small signal equivalent circuit

The SSU system for analysis consists of two parts, (i) the PWM section and (ii) the strings connected continuously to bus capacitor. The system may be modeled by the equivalent circuit shown in Fig. 3.6(a). Each array section is represented by its equivalent circuit. The PWM part is connected to a single array section. The remaining \( n \) connected sections are in parallel, and are represented by a similar single section with impedances scaled down by a factor of \( n \). The contin-

Chapter 3: MODELING, ANALYSIS AND DESIGN OF A SHUNT SWITCHING UNIT
uously connected sections, therefore, have an impedance of $Z_s/n$, where $Z_s$ is the impedance of one section.

The PWM switch and diode are represented by the model of the PWM switch [36]. This circuit may be used to evaluate the control transfer function, the loop gain, and the closed loop bus impedance.

Generally, the bus capacitor impedance $Z_c$ is small enough to swamp out the impedance $Z_s/n$ of the $n$ connected sections. This is indicated in Fig. 3.6(b). In the analytical expressions derived below, the impedance $Z_s/n$ is ignored in comparison to $Z_c$. The impedance of the bus capacitor is:

$$Z_c = \frac{1 + sC_B R_C}{sC_R} \quad [3.4.1]$$
Figure 3.6. Small signal modeling of SSU
3.5 Design and analysis of the PWM shunt unit

3.5.1 Method of analysis

Following the discussion in chapter 2, the presence of the input filter requires the impedance interaction analysis at two interfaces A and B shown in Fig. 3.7(a). At interface A, the Nyquist criterion is applied to the impedance ratio $Z_s/Z_{in}$, where $Z_s$ is the array-filter impedance and $Z_{in}$ is the input impedance of the regulator. In order to avoid the impedance interaction, $Z_s$ must be much larger than $Z_{in}$ for stability.

A modular approach should be used for optimum design, treating the PWM unit as an unterminated two-port system. The shunt regulator control design can be optimized as an independent module. The stability of both the connected source and load subsystems can then be analyzed using the impedance comparison method.

3.5.2 Description using z-parameters
(a) Analysis approach using impedance interaction

(b) Equivalent circuit for the PWM unit

Figure 3.7. Impedance analysis approach and PWM unit representation
Figure 3.7(b) indicates the equivalent representation of the PWM unit using the model of the PWM switch [36]. $Z_c$ is the impedance of the bus capacitor and its ESR. The inputs to this unit are input current and load current. The outputs are the array side (input) voltage and the bus (output) voltage. A suitable description of the PWM unit, therefore, requires the use of $z$-parameters:

$$v_1 = z_{11}i_1 + z_{12}i_2$$

$$v_2 = z_{21}i_1 + z_{22}i_2$$

where the suffix '1' denotes input quantities and the suffix '2' indicates output quantities.

The $z$-parameters for this circuit on open loop can be derived using $d' = 0$ as:

$$z_{11} = D'^2Z_c$$  \[3.5.1\]  

$$z_{12} = D'Z_c$$  \[3.5.2\]  

$$z_{21} = D'Z_c$$  \[3.5.3\]  

$$z_{22} = Z_c$$  \[3.5.4\]

On closed loop, the controlling duty ratio is
\[ d' = -k(s)v_B = \frac{-A(s)v_B}{V_p} \]  

where

- \( V_p \) = PWM ramp amplitude
- \( v_B \) = small signal bus voltage
- \( V_B \) = dc bus voltage (a constant)
- \( I_p \) = short circuit array current (a constant)
- \( A(s) \) = compensator gain
- \( k(s) \) = overall compensator gain from \( v_B \) to the duty ratio \( d' \)

The \( z \)-parameters for the PWM section (Fig. 3.7(b)) on closed loop are:

\[ z_{11} = \frac{(D' - k(s) V_B) D' Z_C}{1 + k(s) I_p Z_C} \]  

[3.5.6]

\[ z_{12} = \frac{(D' - k(s) V_B) Z_C}{1 + k(s) I_p Z_C} \]  

[3.5.7]

\[ z_{21} = \frac{D' Z_C}{1 + k(s) I_p Z_C} \]  

[3.5.8]

\[ z_{22} = \frac{Z_C}{1 + k(s) I_p Z_C} \]  

[3.5.9]
3.5.3 Unterminated PWM unit design

The unterminated input and output impedances are given directly by the expressions for $z_{ii}$ and $z_{oo}$ respectively. The characteristic expression indicates that the unterminated loop gain is:

\[ T = k(s)I_pZ_C \]  \hspace{1cm} [3.5.10]

This consists of the following components, the compensator gain and the transfer function from control to output voltage:

\[ \frac{d^r}{V_B} = k(s) = A \frac{(s)}{V_P} \]  \hspace{1cm} [3.5.11]

\[ G_1 = \frac{V_B}{d^r} = I_pZ_C \]  \hspace{1cm} [3.5.12]

Here, $V_P$ is the PWM ramp amplitude. Figure 3.8 indicates the unterminated closed loop design procedure. The open loop output impedance $Z_{ol}$, impedance $Z_C$ of the bus capacitor (Eqn 3.5.4). The control transfer function $G_1$ follows from Eqn 3.5.12. The unterminated loop gain (Eqn. 3.5.10) is shaped by the compensator gain and is the product $k(s)G_1$. The compensator may either be the proportional or integrating type as shown in Fig. 3.9.

The closed loop bus impedance of the SSU is indicated as:
\[ Z_{CL} = \frac{Z_{OL}}{1 + G_1 k(s)} \]  

[3.5.13]

Figure 3.10 shows the experimentally measured loop gain compared to the modeled value using the equivalent circuit in Fig. 3.6. The closed loop bus impedance is shown in Fig. 3.11. These measurements are for an integrating error amplifier.

The following considerations affect the design of the compensator. The dominant pole in the closed loop bus impedance (Fig. 3.8) is seen to be at the integrator zero \( \omega_z \). The slope of the loop gain \( G_1(s)k(s) \) is 40 dB/decade to the left of this zero. To get adequate phase margin, the zero \( \omega_z \) should be small, but to get a fast closed loop response, it should be large. Also, the loop gain crossover should be sufficiently below the switching frequency.

For a switching frequency of 90 kHz, the loop gain crossover was chosen to be at 5 kHz. The integrator zero \( \omega_z \) is chosen at around 600 Hz, in order to comply with the above constraints.
Figure 3.8. Unterminated closed loop design and bus impedance
Figure 3.9. Error amplifier compensators
Figure 3.10. Theoretical and experimentally measured loop gain
Figure 3.11. Theoretical and experimentally measured bus impedance
3.5.4 Interaction analysis at interface A and B

The analysis for stability at interface A (Fig. 3.7(a)) may be performed using the array-filter impedance $Z_s$ and the input impedance $Z_{in}$ of the PWM unit using a load terminated PWM unit. The input impedance with a load termination $Z_L$ can be expressed in terms of the closed loop $z$-parameters (Eqns 3.5.6-9) as:

$$Z_{in} = z_{11} - \frac{z_{12}z_{21}}{\zeta_{22} + z_L}$$

[3.5.14]

This impedance works out to:

$$Z_{in} = \frac{Z_XD^2(1 - \frac{V_Bk(s)D'}{D})}{1 + I_pk(s)Z_X}$$

[3.5.15]

Here $Z_X$ is the parallel combination of $Z_c$ and $Z_l$. The array-filter output impedance $Z_s$ can be expressed as:

$$Z_s = \frac{R_D(1 + s(L_f/R_{in} + C_AR_A) + s^2L_fC_A)}{1 + sC_AR_D}$$

[3.5.16]

with the condition

$$R_D >> R_A$$

Here, the system loop gain to which the Nyquist criterion must be applied is $Z_s/Z_{in}$. Typical plots for the impedances $Z_{in}$ and $Z_s$ are plotted in Fig. 3.9(a) for
investigating impedance interaction. The source impedance $Z_s$ is the high impedance $R_n$ of the array at low frequencies, followed by a resonance at higher frequencies due to the filter inductor $L_f$ and the array capacitance $C_a$. The input impedance $Z_{in}$ has a low frequency value of $-D'V_0/I_r$. It is a negative resistance. The $Z_s$ plot must be designed to lie above the $Z_{in}$ plot for stability. For instance, an undamped input filter leads to a drop in the $Z_s$ plot (shown dotted). The filter must be suitably damped to avoid this.

The expression $-D'V_0/I_r$ indicates that there is a greater prospect of instability as the illumination level (i.e., $I_r$) decreases and the $Z_{in}$ plot moves up towards the (fixed) $Z_s$ plot. This must be taken into account in the design. Also, for a given $I_r$, the worst case duty ratio is $D' \approx 1$. The range of illumination level over which the $Z_{in}/Z_s$ interaction can be avoided depends mainly on how much $Z_s$ is greater than $V_0/I_r$. This analysis also indicates that one of the methods of ensuring stability is to use a larger filter inductor (larger $Z_s$), provided weight considerations allow it.

The stability analysis at interface B can be carried out using the closed loop output impedance $Z_o$ with a $Z_s$ source termination. This can be stated in terms of the $z$-parameters as:

$$Z_o = z_{22} - \frac{z_{12}z_{21}}{z_{11} + z_s}$$  \[3.5.17\]
(a) Interaction at interface A

(b) Interaction at interface B

Figure 3.12. Impedance interaction analysis at interfaces A and B
With the assumption $Z_c \ll Z_o$, this works out to:

$$Z_o = \frac{Z_c Z_s}{Z_s + Z_c k(s)(I_p Z_s - b' V_B)}$$

[3.5.18]

The system loop gain in this case is $Z_o/Z_o$. A typical converter load consists of a constant power load with an input filter, as shown in Fig. 3.12(b). The low frequency value of $Z_c$ in this case is again a negative resistance, followed by a resonance caused by the input filter. If instability is to be avoided, the $Z_o$ plot must lie well below the $Z_s$ plot. The effect of an inadequately damped array input filter on $Z_o$ is shown dotted.

3.5.5 Large signal simulation

The large signal EASY5 simulation in Fig. 3.13 demonstrates the operation of the SSU. The simulation is for a step load change from a load current of 17.5 A to 8 A, for a 120 V system. The array voltages and currents are shown for the transition. As the load step is applied, the PWM operation shifts from the lowest string to an upper string. Strings shown below the PWM string are shorted and do not contribute any current to the load.
Figure 3.13. Large signal simulation showing response to a step load change
3.6 Non-linear limiting effects

It has been shown above that due to the significant array capacitance and the input filter, the SSU design is unstable at large $D'$ and at low illumination. In particular, if the expression

$$\frac{D'V_B}{I_p Z_S}$$

is large compared to unity, it leads to small signal instability on closed loop operation. However, this does not lead to instability in the sense of an unbounded response. This is because the duty ratio modulator does not provide linear increments in D, but clamps it at a maximum value of 1.

The effect of the non-linear clamp on the duty ratio is to cause limit cycle operation. The following is a quantitative analysis of these limit cycles using the describing function method [37]. The limit cycles are shown to be stable and method for calculating the limit cycle frequency and amplitude is developed.

The main nonlinearity is the upper limit of 1 for the duty ratio $D'$. Fig. 3.14 shows the the earlier linear model for the power stage and the error amplifier replaced with an amplitude dependent gain $N(a)$. The output of the error amplifier is clipped, but the effect of the low pass filter in $G(s)$ is to smooth the waveform.
Linear model for power stage $G(s)$

Non-linear model for duty ratio limit of "1"

Combined model to determine possible limit cycles

Figure 3.14. Modeling for limit cycle analysis
back into a sinusoid. Using standard describing function analysis [37] for this system, the waveforms are analyzed using only the first harmonic content.

If there is a tendency towards oscillation, the gain of the feedback amplifier falls with the input amplitude. This limits the oscillation to some finite value. To find the amplitude and frequency of this type of operation, if a limit cycle exists, the system must satisfy:

\[ G(j\omega_a) = \frac{-1}{N(a)} \]  

[3.6.1]

where

\[ w_a = \text{limit cycle frequency} \]
\[ a = \text{limit cycle amplitude} \]

The nonlinear gain gain \( N(a) \) is real because it does not include any hysteresis [37], so the limit cycle frequency \( \omega_a \) can be found directly from

\[ \text{Im} \left( G(j\omega) \right) = 0 \]  

[3.6.2]

The gain of the error amplifier can be shown to be:

\[ N(a) = \frac{2}{\pi} \sin x + \frac{k}{\pi} (\pi - x - \frac{\sin 2x}{2}) \]  

[3.6.3]

where
Figure 3.15. Polar plot for the intersection of $G(s)$ and $-1/N(a)$
\[ x = \cos^{-1} \frac{1 - D'}{ka} \tag{3.6.4} \]

and \( k \) is the linear gain of the error amplifier.

Figure 3.15 shows the polar plot for \( G(j\omega) \) and the intersection with \( N(a) \) on the real axis. The amplitude of the limit cycle is found from the \( N(a) \) expression at the intersection. The directions of the plots [37] indicate a stable limit cycle. The actual time domain simulation in Fig. 3.16 confirms the presence of limit cycles of frequency and amplitude approximately equal to that predicted by the analysis. The frequency for this example is about 3 kHz and the limit cycle amplitude is 60 mV for the bus voltage.

It is found that the amplitude of oscillation on the bus voltage is small, but the associated cycles at the filter component levels are large. These can be a source of electromagnetic interference at a lower frequency than the ripple.

In practice, the SSU system has a number of additional non-linearities that affect the performance. The capacitance of the array \( C_a \) is a function of its voltage. The dynamic resistance \( R_o \) of the array varies with the operating point. All these nonlinearities have been simulated using EASY5 models. The simulations (Fig. 3.17) using the exact models have confirmed the basic results arrived at above,
Figure 3.16. Simulation showing limit cycles with only the duty ratio nonlinearity
Figure 3.17. Simulation showing limit cycles with other nonlinearities included.
i.e., low frequency bounded amplitude limit cycle operation takes place at "unstable" points. The amplitude of the bus voltage oscillations is small, but the filter components show larger amplitude oscillations.

3.7 Summary of small signal analysis

The above analysis shows that the solar array capacitance is a driving factor in the design of a switching shunt regulator. To avoid the current surges cause by this capacitance, an input filter is needed. The input filter, in turn, affects the dynamics of the the closed loop regulator.

The resonance between the array capacitance and the filter inductance must be adequately damped. In general, the system shows lowest phase margin at large D' and at low illumination levels. The ideal array without capacitance, and without the input filter, does not have these stability problems. Furthermore, it is shown that the circuit nonlinearities tend to prevent any unbounded response even at these unstable points. Limit cycle operation takes place with a low amplitude of oscillation at the bus voltage, but the oscillations in input current can still be a cause for concern.
Both the input current ripple as well as the stability aspects are improved by the use of a large filter inductor. However, since the filter must be used in each array section, this leads to increased weight of the SSU, which is undesirable for space applications. The implication of this is that if the SSU performance is to be improved without sacrificing weight, it is necessary to look at other alternative circuits. This is investigated in the next chapter.
Chapter 4: DEVELOPMENT OF A NEW OPTIMAL CONFIGURATION FOR THE SEQUENTIAL SHUNT

4.1 Introduction

It has been shown in chapter 3 that it is difficult to meet input current ripple and stability requirements in the SSU design. Unless a large filter inductor is used, there is prospective instability at large D' and at low illumination levels, i.e., ideally:
\[ \frac{D'V_B}{Z_{sl_p}} \ll 1 \] [4.1.1]

Here, the array-filter impedance \( Z_s \) depends on the array capacitance and the filter inductor, and the short circuit current \( I_p \) is a function of the illumination level.

The use of large filter components for each string implies increased \textit{weight} which is undesirable for high power space applications. The main focus of this chapter is, therefore, to develop a new technique that does not require the use of filters in all the strings.

It is apparent from the simulation in Fig. 3.13 that at any time only one filter for the PWM string is actually in use, because most of the strings are either shorted or connected to the bus continuously. It should be possible, therefore, to use fewer filter components in designated PWM strings which reduce the SSU weight. At the same time, the filter can be more elaborate, in order to meet the input ripple specification as well as stability criteria.

Originally, the effort was directed towards a method that closely approximates the SSU with filters in all the strings. This was necessary for modeling purposes, because it is impractical to include a large number of filter components and ob-
tain the simulation within a reasonable time. The "ring" model was developed for this purpose and it allows simulations for systems with a very large number of strings, while using much fewer (3, 5 or 7) actual filtered sections.

This model serves to illustrate the simplifications that are possible, and it was also implemented in hardware form, because a scheme that reduces the number of filters in a simulation is equivalent to reducing the weight of SSU in actual hardware.

The hardware implementation of the ring model demonstrated that practical implementation would require two modifications, i.e., extending the current range of the PWM section as compared to a single unfiltered section, and the introduction of hysteresis in the control loop. The following sections describe the evolution of the final alternate scheme, in the sequence described above.

4.2 The ring model

The primary purpose of the ring model is to obtain a response similar to the SSU with filters in all the strings, without actually using a large number of filters in
the simulation. Thus, the objective is to retain the same dynamics as the original SSU, which is not necessarily a requisite for any alternate scheme.

Figure 4.1 shows a conceptual representation of this model. The basic premise is that:

- due to the bus capacitor and error amplifier cutoff, the control voltage does not change abruptly
- consequently, only a few strings are in a dynamic state of transition at any instant.

In Fig. 4.1, these transition strings are indicated as an active band which moves up or down with the control voltage. The remaining strings are in a connected or disconnected state. During any large change of control voltage, a given string makes a transition from the on to off state (or vice versa) together with adjacent strings on either side. Thus, more than one string is in a state of transition. If the dynamics of the original SSU is to be truly represented, it cannot be represented by a single dynamic filtered PWM section, with the remaining strings in a static on or off state. This leads to the idea representing the system by more than one, but limited number of PWM sections. As the transition from the connected to disconnected state subsides in one filtered section, it can be interchanged with an unfiltered, disconnected section. The filtered section is then allowed to settle in a
Shown for $m=3$ ($k=1$)

Disconnected
PWM mode
Connected to the bus

$m = 2k + 1$

$$I_{Tot} = (n - k)I_F + \sum_{i=1}^{k+1} I_{Ai}$$

Figure 4.1. The ring model
disconnected state, so that it can later be made available for connection as a fresh string. In this way, a limited number of filtered sections are recirculated to simulate the effect of a large number of sections. The objective is to ensure that a transient

1. connection or disconnection is only made to a filtered section, and

2. if the transition has subsided in a filtered section, it can be exchanged with a static section in the same state, freeing the PWM section to accommodate another connection or disconnection as in (1).

The second point above indicates a wraparound requirement for the filtered section, so that the same section may be reused, rather than a new filtered section. This leads to the "ring" structure in the model.

These assumptions were made primarily to ensure that the response of the ring model closely approximates that of an SSU with filters in all the strings. They are not, in general, necessary in an alternate scheme. For instance, a control voltage change may directly connect or disconnect an unfiltered section in another scheme.

Let \( m \) represent the number of elements in this active band, where \( m \) is chosen to be an odd number. This allows an equal number of strings in transition on either side of the PWM string.
\[ m = 2k + 1 \]  \hspace{1cm} [4.2.1]

The control voltage represents the number of sections connected to the bus at any instant. This consists of a whole number and a fraction:

\[ \frac{v_c}{w} = n + f \]  \hspace{1cm} [4.2.2]

where

\[ n = \text{int} \left( \frac{v_c}{w} \right) \]  \hspace{1cm} [4.2.3]

Here \( w \) represents the comparator window, or the amount of control voltage that corresponds to one section. In order to use a limited number of filter components, \( k \) of these \( n \) sections are taken from a limited active band of \( m \) filtered sections. In the model, \( k \) of the band elements are always forced on, another \( k \) elements are forced off, and one element is provided with the fractional voltage \( wf \) for PWM operation.

The total current to the bus capacitor is:

\[ I_{TOT} = (n - k)I_F + \sum_{i=1}^{k+1} I_{R_i} \]  \hspace{1cm} [4.2.4]
where $I_s$ is the current from a single connected section in the model. $I_R$ is the current in one ring element. $k$ of these elements are connected to the bus, and one additional section operates in the PWM mode. This representation takes into account the dynamics of strings which are not in a settled state.

Figure 4.2 shows a comparison of the response for a step load change. The response obtained with 22 filtered strings is similar to the response from a ring model with $m = 3$. This is for a system with an integrator. If the control voltage changes more abruptly, the number of elements $m$ in the ring must be suitably increased.

Figure 4.3 shows a simulation for the string currents in a ring model with $m = 3$. In order for a re-used ring element to approximate a fresh string, the transients in each string must be allowed to subside before the element can be used. The simulation shows a settling time of less than 0.00025 sec for each string, for a transition from the on to off state.
Figure 4.2. Comparison of simulations for the full SSU and the ring model
Current in element 1

Current in element 2

Current in element 3

Control voltage

Integer number of strings connected to the bus (on-off)

Status of PWM ring elements (1, 2 or 3 PWMing)

Figure 4.3. String currents in the ring model
4.3 **Hardware implementation of the ring**

The ring model was next implemented in hardware in the form indicated in Fig. 4.4. In order to obtain the control functions indicated by Eqns 4.2.2, 4.2.3 and 4.2.4, the control voltage was digitized in an analog to digital converter (ADC). The less significant bits (LSB) in the output represent the fractional part \( w_f \) of the control voltage. The more significant bits (MSB) represent the integer part \( n_w \).

The wraparound feature ("ring" operation) was obtained by using the two least significant bits from the integer part. A 4-clement ring was driven by suitable logic, as shown in the Table (Fig. 4.4). The ring sections have the large filter inductors to allow PWM operation. The on-off strings are fitted with much smaller filter inductors.

During the exchange between a filtered section and a static unfiltered section, there is a current spike due to the abrupt switching of the latter, as there is no filter. This spike can be effectively suppressed by slowing the gate drive to the on-off MOSFETs. This is done by placing an RC network between the drive and the MOSFET gate. This method absorbs the \( \frac{1}{2}CV^2 \) array capacitance energy in the switch and is unsuitable for PWM operation of the switch at high frequency.
Thus, the filtered sections have the usual gate drives, while the unfiltered sections have delayed gate drives, instead of filters for preventing current surges.

The hardware scheme was implemented with discrete increments in duty ratio. During a transition from one string to the next adjacent string, the exchange process between the filtered and unfiltered section was found to cause regulation by rapid switching in and switching out of the ring. This form of operation is undesirable because the on-off MOSFETs are not configured for high frequency operation. It is necessary to ensure that fine control by the PWM string continues smoothly during this transition.

Thus, two desirable features were indicated by this hardware, if ring switching is to be avoided:

- the control range of the filtered (PWM) section should preferably be larger than that of a single on-off section (if the on-off section switches in a current of \( I_r \), the PWM section should control a current larger than \( I_r \))
- the simplified form of the ring control table must be modified to include hysteresis to discourage the ring switching

Only one PWM section is used. The circuit is discussed in the next sub-section.
**Figure 4.4.** Hardware implementation of the ring model

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**Chapter 4: DEVELOPMENT OF A NEW OPTIMAL CONFIGURATION FOR THE SEQUENTIAL SHUNT**

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Fine control by on-off operation between two adjacent strings, is the regular mode of operation in the original $S/\mathcal{R}$ regulator [30, 15]. Here, the switching frequency is variable, given by:

$$f = \frac{I_p A}{C_w} (1 - p)p$$  \[4.3.1\]

where $p$ is the fine control fraction, a number ranging from 0 to 1. The present work is concerned with a high voltage array with an appreciable array capacitance. This makes it impractical to absorb the $\frac{1}{2} C V^2$ energy of the capacitance in the switch, so this mode of operation is avoided. Instead, the functions of the on-off and fine control (PWM) sections are separated to allow greater design freedom:

- the on-off sections operate with small filters, and the switch is set up to absorb the capacitive energy due to occasional switching
- the fine control section operates at fixed frequency with heavy filtering, so there is no variation of voltage at the array capacitance within a switching period, i.e., no energy to be absorbed by the PWM switch.
- the use of a fixed switching frequency facilitates the design of the input filter for the PWM section.
- use of ground-referenced ramps, instead of the stacked ramps allows ramp amplitude to be independent of the comparator window $w$, allowing the use of larger ramp amplitudes for noise immunity
4.4 Single PWM section scheme

The single PWM section scheme (devised by Dong-Ho Lee) is based on the principles outlined above, with the following changes:

- instead of using a "ring", a single PWM circuit with a larger range is used

- analog circuits are used to derive the integral and fractional parts of the control voltage, instead of the digital scheme in section 4.3.

- the necessary hysteresis is incorporated in the control, to prevent switching between the filtered and non-filtered sections

Thus, the circuit is a practical implementation of the reduced filter concept, and not an attempt to preserve the dynamics of the original SSU, like the ring scheme. During a transition, the ring scheme (and the original SSU) switch in an additional filtered string. The new scheme switches in an unfiltered string, accompanied by an abrupt change in the PWM duty ratio. With a suitable implementation of hysteresis, the transition is smooth, and overcomes the problem of ring switching. The dynamics and equivalent circuit are identical, except during the transition. The net advantage of this is the complete elimination of
filters in all sections except the PWM section, and the consequent saving in weight.

Figure 4.5(a) shows the schematic for the single PWM section circuit. The single PWM section current range is extended by using two strings in parallel for the PWM switch. The circuit is damped following the procedure discussed in chapter 3.

The controls are similar to those described earlier, the chief difference being the introduction of hysteresis. The control voltage \( v_c \) is used to generate the desired number of on sections, by comparison with a set of stacked comparators. The PWM control voltage is obtained by the subtraction:

\[
v_{PWM} = A(v_c - nw)
\]  \hspace{1cm} [4.4.1]

where \( n \) represents the number of sections actually on, determined by inspecting the comparator outputs. \( w \) is the comparator window, as before. \( A \) is a constant.

Hysteresis is introduced in the comparator by using the voltage difference

\[
v_{COMP} = v_c - \frac{v_{PWM}}{A'}
\]  \hspace{1cm} [4.4.2]
to drive the comparator stack, instead of using \( v_c \) directly. \( A' \) is an attenuation constant, whose value must be chosen based on \( A \). By rearranging the equations (4.4.1 and 4.4.2), the input voltage to the comparator is:

\[
v_{\text{COMP}} = v_c(1 - \frac{A}{A'}) + \frac{A}{A'} n w
\]  \[4.4.3\]

The factors \( A \) and \( A' \) are chosen such that:

\[
v_{\text{COMP}} = 0.9 \ v_c + 0.1 \ n w
\]  \[4.4.4\]

This expression indicates that as \( n \) changes, the input to the comparator is altered, introducing hysteresis. The net result is outlined in Fig. 4.5(b), which shows that upward switching takes place at \( D' = 0.9 \), downward switching takes place at \( D' = 0.1 \), and any jump in the PWM section duty ratio, due to on-off switching is restricted to a range of about 0.5, well within the hysteresis difference.

Figure 4.5(c) indicates control waveforms for the scheme. The upper trace is a test control voltage. The middle trace represents the summation \( n w \) for the integer sections. The lower trace is the PWM control voltage, which is the difference of the other two voltages.

Figures 4.6 and 4.7 show large signal simulations for a load step change for the above scheme and for the original SSU.
Figure 4.5. Single PWM section SSU
Figure 4.6. Step load simulation for single PWM section SSU
4.5 Summary and performance for the new technique

The basic premise in the introduction of the new regulator is the separation of the filtered fine control function and the unfiltered on-off function. This allows separate designs for the on-off section (slow gate drive) and the PWM section (elaborate filter).

Each filter section adds to the weight, due to the inductor, and damping components. The weights of the MOSFETs, heatsink, gate drive, etc. are common to all circuits, and unavoidable. If the filter contributes to \( n \% \) of the unit weight, the single PWM scheme can reduce the weight by a factor of approximately \( n \% \). \( n \) may range from .5 to .75 or more, depending on the size of the MOSFET and the heatsink.

If the number of filtered sections is restricted, the circuit provides savings in weight, but also introduces some loss of redundancy, because the PWM section cannot be allowed to fail.
Figure 4.7. Step load simulation for original SSU with all strings filtered
In summary, the ring scheme was derived as a model with the same dynamics as the SSU with filters in all the strings. The ring models are used for simulations where it is impractical to introduce a large number of filter components. Hardware implementation of the ring scheme was tried, and it indicated the need for hysteresis in the control section, and the need to extend the current range of the PWM section to a value greater than that of an on-off section, for smooth transitions between strings. The final single PWM scheme solution uses hysteresis and is found to work without the need for the ring structure. Thus, the number of filters is reduced to one, and there are appreciable savings in the SSU weight and volume.
Chapter 5: CONCLUSIONS

This work has addressed various issues involved in high power switching shunt regulators. A general method of design and analysis of shunt regulator systems is presented, consisting of:

1. two-port unterminated modeling and design of the shunt
2. interaction analysis for stability with the load subsystem
3. interaction analysis with the source subsystem

The output characteristics of all shunt regulators are determined by the feedback gain and the bus capacitor. The switching shunt provides the same shunting action as a linear regulator, but without dissipating power. Switching shunt regulators require the use of an input filter. The load-source interaction analysis for a switching shunt indicates that the input filter must be properly designed to prevent instability.
Modeling and analysis techniques have been developed for analyzing the operation and stability of sequential switching shunt regulators. The array capacitance is shown to be a driving factor in switching regulator design. It necessitates the use of an input filter in order to prevent input current surges. These input filters affect the stability of the SSU and also contribute to its weight. The input filter is shown to bring in a dependence on the duty ratio $D'$ and the illumination level $I_r$ in the control transfer function. The need for suitable damping of the input filter was demonstrated. A large inductor is needed in order to meet stability and input current ripple requirements.

The input filters are not all operational at the same time. A new SSU scheme is developed, which uses only one PWM filter. The ring scheme can be used for representing large SSU systems in a model. It leads to the concept of separation of the fine control and on-off section functions. Thus, the input filter is required only in the fine control section and is eliminated from the remaining sections. The remaining on-off sections have an alternate approach to current surge suppression, namely, the use of slower gate drives for the MOSFETs. This separation of function leads to greater design freedom, and weight savings. The direct implementation of the ring scheme was found to demonstrate the need for hysteresis in the control, to prevent interaction between the fine control and on-off sections. This was subsequently implemented in the single PWM section.
scheme, which uses this hysteresis and dispenses with the ring to prevent the interaction.
REFERENCES


[38] Rocketdyne (Rockwell International) EMI specification: RC1806

Appendix A. STATE TRAJECTORY ANALYSIS FOR INPUT CURRENT RIPPLE

Current surge without filter

Figure A.1 (a) shows the two configurations assumed by the circuit when the switch is open and when it is closed. The bus capacitor is represented by the voltage source $V_b$, and the solar array by the current source $I_r$. There are two states $I_L$, the cable (filter inductor) current and $V_r$, the array capacitance voltage.

The circuit may be analyzed using the state trajectory approach [40]. The normalization bases are chosen as $V_b$ for voltage, and $V_b/Z_o$ for current, where

$$Z_o = \sqrt{\frac{L}{C_A}} \quad [4.1]$$
Figure A.1. State trajectory analysis for input current ripple
When there is no input filter, the inductor $L$ is the stray inductance of the connecting cable. The resonant oscillation is represented by the circle in Fig. A.1 (b). In practice, the oscillations are rapidly damped out, and the trajectory spirals inwards. However, this figure indicates the upper bound on the possible current surge. The value of the peak current is:

$$I_{FPN} = \frac{2V_B}{Z_O} = \frac{2V_B}{\sqrt{L/C_A}}$$ \hspace{1cm} [4.2]

The time associated with one resonant cycle, i.e., one full circle, is:

$$T_O = 2 \pi \sqrt{LC_A}$$ \hspace{1cm} [4.3]

**Current surge with input filter**

When an inductor filter is used, $L$ represents the filter, of value $L_F$. The topological mode centers [40] for the two circuit configurations are $(I_F, V_h)$ and $(I_F, 0)$. For effective filtering, the switching period must be higher than the period for one cycle i.e.,

$$T_S << T_O$$ \hspace{1cm} [4.4]
In this case, the trajectory consists of two small arcs as shown in Fig. A.1 (c). The relative sizes of the arcs depend on the duty ratio \( D' \). The arcs are equal if \( D' = 0.5 \). The angles subtended by the \( D' \) and \( D \) arcs at the topological mode centers are \( \phi \) and \( \theta \) respectively. The angles are obtained as fractions \( DT_s \) and \( D'T_s \) of the switching period \( T_o \):

\[
\frac{2\phi}{2\pi} = \frac{D'T_s}{T_o} \quad [A.5]
\]

so that

\[
\phi = \frac{\pi D'T_s}{T_o} \text{ radians} \quad [A.6]
\]

Similarly,

\[
\theta = \frac{\pi DT_s}{T_o} \text{ radians} \quad [A.7]
\]

Define the angle \( \alpha \) as:

\[
\alpha = \theta + \phi = \frac{\pi T_s}{T_o} \quad [A.8]
\]

and with \( R_1 \) and \( R_2 \) as the radii of the two arcs,

\[
R_1\sin\phi = R_2\sin\theta \quad [A.9]
\]
\[ R_1 \cos \phi + R_2 \cos \theta = 1 \quad [A.10] \]

Eliminating \( R_3 \), using the relation \( \theta + \phi = \alpha \),

\[ R_1 \sin \alpha = \sin \phi \quad [A.11] \]

The required ripple, which is \( 2R_3 \sin \phi \) can be expressed as:

\[ I_{pp} = 2 \frac{\sin \theta}{\sin \alpha} \sin \phi \quad [A.12] \]

This is a general expression for the ripple for any duty ratio. It can be simplified in order to be more meaningful in terms of circuit components. Taking the case of maximum ripple at \( D = D' = 0.5 \), in which case

\[ \theta = \phi = \frac{\alpha}{2} \quad [A.13] \]

and

\[ I_{pp} = \tan \phi \quad [A.14] \]

If the ripple is desired at some other duty ratio \( D \), a proportionate fraction of \( \alpha \) must be considered, instead of Eq. (A.13). On using the normalizing factors, this value can be written as:
\[ I_{pp} = \frac{V_B}{Z_O} \tan \frac{\pi T_S}{2T_O} \quad [A.15] \]

If the switching frequency is high, i.e., if \( T_S \ll T_O \), the sines can be replaced by the angles:

\[ I_{pp} = 2 \frac{\phi_0}{\alpha} = 2DD' \frac{\pi T_S}{T_O} \quad [A.16] \]

Differentiating with respect to \( D \), the maximum ripple is at \( D = 0.5 \), leading to the result:

\[ I_{pp_{\text{MAX}}} = \frac{V_B T_S}{4L} \quad [A.17] \]

This approximate expression does not contain \( C_s \), which is implicitly included in the assumption \( T_S \ll T_O \).
Appendix B. Choice of optimal damping resistor

Figure B.1(a) shows the array and filter circuit with a damping branch consisting of components $R_{cd}$ and $C_n$. Due to the component values, the contribution to damping of the dynamic resistance $R_n$ and the series resistance $R_A$ is negligible. The circuit can be simplified to the form shown in Fig. B.1(b).

Direct substitution of the exact expression for $Z_S$ into the expression for $G_1$ leads to fourth order polynomials. For the purpose of determining the damping components, it is sufficient the choose

$$C_D \gg C_A \quad [B.1]$$

and consider the approximate expression for $Z_S$ only beyond the $C_D R_{cd}$ corner, i.e., for
Figure B.1. Selection of filter damping components
\[ \omega > \frac{1}{C_B R_{CD}} \]  \[ [B.2] \]

The impedance \( Z_s \) is sketched in Fig. B.1(c). It can be seen that for optimum damping of \( Z_s \) itself, \( R_{CD} \) should be equal to the dynamic resistance:

\[ R_{CD} = \sqrt{\frac{L_F}{C_A}} \]  \[ [B.3] \]

It will be shown below that this is also the value which is best for (terminated) control to bus voltage transfer function, \( G \) sub 1 as well. Beyond the \( 1/C_B R_{CD} \) corner, \( Z_s \) can be approximated by:

\[ Z_s \approx \frac{R_{CD}(1 + sL_F + s^2L_FC_A)}{1 + C_AR_{CD}} \]  \[ [B.4] \]

On substituting this into the \( \psi_0/d \) i.e., \( G_1 \) expression:

\[ G_1 = -I_p Z_C \left( 1 - \frac{D'V_R}{Z_s I_p} \right) \]  \[ [B.5] \]

the expression for \( G_1 \) becomes

\[ G_1 = -I_p Z_C \frac{1 + \frac{s}{\omega_1 Q_1} + s^2/\omega_1^2}{1 + \frac{s}{\omega_0 Q_O} + s^2/\omega_O^2} \]  \[ [B.6] \]

where

Appendix B. Choice of optimal damping resistor
\[ \omega_o = \frac{1}{\sqrt{L_F C_A}} \quad \text{[B.7]} \]

\[ Q_o = \frac{1}{\omega_o L_F/R_{CD}} \quad \text{[B.8]} \]

\[ \omega_1 = \frac{\sqrt{A}}{\sqrt{L_F C_A}} \quad \text{[B.9]} \]

\[ Q_1 = \frac{A}{\omega_1 (L_F/R_{CD} - D' V_B C_A/I_p)} \quad \text{[B.10]} \]

\[ A = 1 - \frac{D' V_B}{I_p R_{CD}} \quad \text{[B.11]} \]

In order to remove the quadratic terms, it is necessary to strive for pole-zero cancellation with equal \( Q \)'s and equal \( \omega_o \) and \( \omega_1 \). From the above equations, the required conditions are:

\[ R_{CD} \gg \frac{D' V_B}{I_p} \quad \text{[B.12]} \]

\[ R_{CD} \ll \frac{L_F I_p}{C_A D' V_B} \quad \text{[B.13]} \]

Choosing an \( R_{CD} \) that is the geometric mean of these two values, gives:

\[ R_{CD} = \sqrt[\frac{L_F}{C_A}} \quad \text{[B.14]} \]
which is the same value that is needed for optimizing $Z_i$.

Figure B.1(d) shows an alternate LC filter with an additional shunt capacitor $C_F$. The damping of this filter can be designed the same way, if $C_d + C_F$ is used instead of $C_d$ in the above procedure.
Vita

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