TRANSPARENT ASYNCHRONOUS TRANSMITTER RECEIVER INTERFACE (TAXI) COMMUNICATIONS FOR FIBER OPTIC DATA LINKS

by

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(ABSTRACT)

Serial or parallel data links have been the primary tools of data transfer across physical layer boundaries for point-to-point communication systems. However there exists a trade-off between these two kinds of data transfer mechanisms based on their cost-effectiveness and complexity. A recent technological advancement has altered this trade-off considerations. A new chip-set from Advanced Micro Devices offers a high performance integrated alternative to traditional serial/parallel data transfer techniques. The Transparent Asynchronous Transmitter Receiver Interface chipset offers a new means to establish a transparent high speed serial link between two high performance parallel buses. The current TAXIchip set has a maximum effective data rate throughput of 140Mbps which is ten times faster than the RS-422 drivers and receivers. The TAXIchip set can be used in conjunction with the optical components and optical fiber to form a simple fiber optic communication link. The inherent advantages of optical communications can be combined with the versatility of the TAXIchip set to establish TAXI links using optical fiber to cover distances up to several kilometers.

This thesis will systematically develop on the TAXI communication system. Focus of the effort will be on understanding the functionality of the building blocks of the TAXIchip set and the encoding and decoding schemes of the chip set. On obtaining a complete understanding of the communication system fundamentals the communication system will be interfaced to the optical media with a specific reference to the development of the Optical Slip Ring.

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Chapter 1.0

Introduction

Advancement of technology and increase in complexity of systems has emphasized the need for high volume information exchange. Existing LAN standards such as Ethernet(IEEE 802.3) or TOKEN Ring(IEEE 802.5) become inadequate due to their limitations on speed. Point-to-Point data communications is carried out across physical layer boundaries by modern electronic systems using serial or parallel data links. It will be worthwhile to consider the cost/performance trade-off between these two modes of data transfer. Parallel data links are suitable for high speed data transfers since they can support high bandwidths. The parallel data links are compatible with different architectures. However these links involve costly multiconductor cables. They are susceptible to crosstalk, radio frequency interference and bit to bit skew. The serial data links are much simpler and less costly but their insufficient bandwidth make them unsuitable for high speed data transfers.

In the past high speed data communication called on the use of parallel buses which contributed towards a higher cost and a bulkier system due to the use of multiconductor cables. The parallel buses are limited by the drawbacks of the parallel data links discussed above. However recent technological advances have created a change of scenario. The cost/performance trade-off between serial and parallel data transfer techniques have been altered. A high performance integrated alternative to traditional serial/parallel data

transfer techniques has been evolved. This new alternative is known as the Transparent Asynchronous Transmitter Receiver Interface ,more popularly called the TAXI communications. The term TAXI is the trademark of Advanced Micro Devices which has brought out this novel architecture capable of supporting data rates up to 125 MHz which is roughly about 10 times faster than the data rate of conventional RS-422 line drivers and receivers. This is regarded as among the fastest communication standards in existence today. The versatility of the chip allows the user to achieve top performance with minimum hardware cost and minimum radio frequency interference effects.

The TAXI chipset can be used in conjunction with optical components and optical fiber to form a simple fiber optic communication system. Optical data links can be interfaced to the chipset easily thus utilizing all the advantages of fiber optic communications which will be discussed in detail in later chapters.

This thesis will systematically develop the technique of interfacing the TAXI chipset to the fiber optic transmitters and receivers with specific reference to the development of an optical slip ring system used in the new generation of computerized tomography systems. In chapter 2 background material on TAXI communications will be provided to understand the basic concepts of this new alternative to high speed data communications. This chapter will also describe the functional block diagrams of the transmitter and receiver sections of the TAXI chipset. Chapter 3 will discuss data encoding, decoding and error mechanisms in the TAXI communication system. Chapter 4 will present the ideas of interfacing the TAXI chipset to the fiber optic media. The basic design considerations and the board layout of the interface electronics will be presented in this chapter. Chapter 5 will discuss the practical applications of the interface developed in chapter 4 as applied to an optical slip ring. Various fiber optic approaches considered for the development of an optical slip ring will be discussed along with the physical limitations of each of the approaches. Test results on initial experiments conducted on the optical slip ring

prototypes will be presented.. Chapter 6 will discuss conclusions and topics of further research that resulted from this investigation into the TAXI communication system.

Chapter 2.0

Basic Concepts

As new applications surface new technologies are discovered and the existing technologies are updated to accommodate the needs of the specific application. The development of TAXI communication as a reliable alternative for high speed data communications has gained popularity and it is being applied to many real time systems. The TAXI chipset provides the means to establish a transparent high speed serial link between two high performance parallel buses. Since it is important to obtain a complete understanding of the TAXI chipset before interfacing it to the fiber optic media, this chapter will provide the necessary background information. First the general principle of operation of the TAXI chip with specific reference to its block diagram representation would be provided. Then the functional description of the TAXI transmitter and the TAXI receiver will be covered with emphasis on encoding and decoding principles of the chipset and error management.

2.1 General Principle of Operation

The TAXI chip™ integrated circuits is a general purpose interface used in point-to-point data communications at very high data rates over both co-axial and fiber optic media. It provides the means to establish a transparent high speed serial link between two high performance parallel buses. The TAXI chip™ set offers a high performance integrated alternative to traditional serial/parallel data transfer techniques. The TAXI chipset consists of a transmitter which performs the action of taking parallel data and transmitting it serially up to 175 MHz and a receiver which converts the serial data stream back to parallel form. In this way the TAXI chipset seeks to provide a parallel interface through a very high speed serial link. It is important to note that in the process the data bandwidth required by the system is maintained. The TAXI chip operates much like a single parallel register wherein data loaded into one side is read from the other side, except, in this case,

the other side is separated by a long serial link. TAXIs have twelve parallel interface pins which are designated as either as data or command bits. While data represents the normal message traffic between host systems, the commands may originate from the communication control section of a host. Command signals occur at a relatively infrequent rate but have priority over data. Each TAXI is programmed to select one of the following three bit modes of operation, 8 bits of data and 4 bits of command, 9 bits of data and 3 bits of command or 10 bits of data and 2 bits of command. For wider parallel channels TAXI's can be cascaded to compress multi-byte words into a single serial link. Flexible byte width and the option to cascade TAXI chips allow the user more freedom to move a maximum amount of data with a minimum number of components.

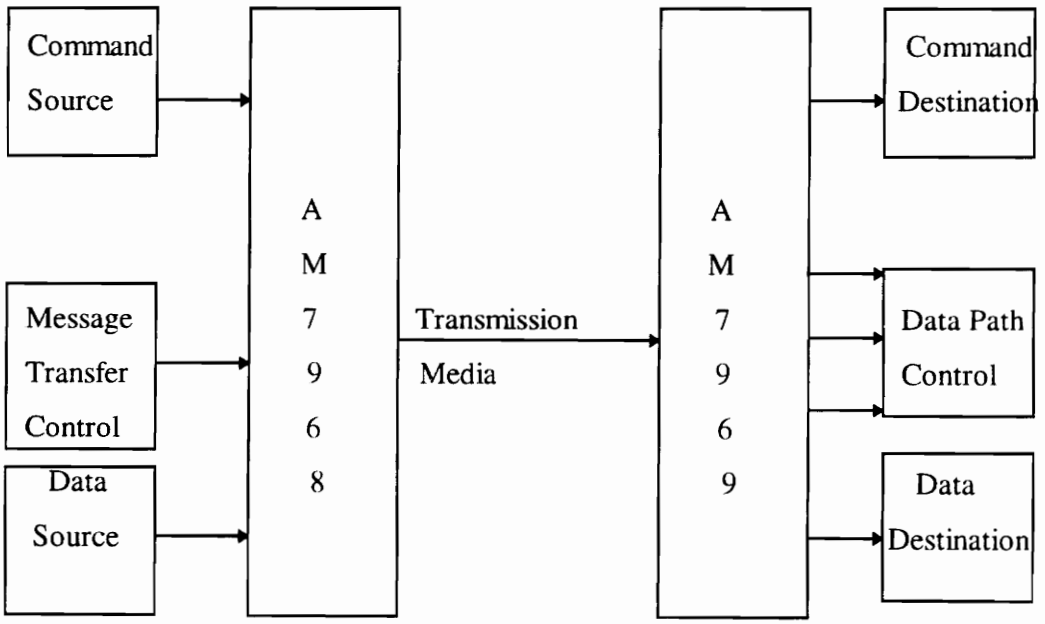


Figure 2.1 TAXIchip System Block Diagram

A block diagram representation of the TAXIchip system is shown in figure 2.1. The AM 7968 transmitter has 12 parallel inputs of data and command lines. The data lines serve to carry the normal message traffic while the command lines carry supervisory information

control information which includes communication specific commands such as Request-to-send or clear-to-send; application specific command such as Message Address follows, Message type follows , Initialize your system, Error, Re transmit, Halt etc. The DMS(data mode select) determines the data path width. When wired to GND the data is 8 bits and command 4 bits, when wired to V_{CC} data is 9 bits and command is 3 its and when left floating data is 10 bits and command 2 bits. Transmitter sends data if all of the command lines are logic 0 when the device is stroked; otherwise a command signal is sent when the transmitter is strobed.

Parallel information that is input through data/communication lines is captured by the input latch on the rising edge of the strobe pulse. An acknowledge signal is then sent back from the transmitter when it is ready to accept the next byte. Information is transferred to the encoder latch first and then through the data encoder and into the shifter on two successive byte clocks. Encoded patterns then come out of the shifter and through the media interface one bit at a time. Voids between transmitted data are filled with special sync. patterns which keeps the AM7969 PLL synchronized and define byte boundaries. The sync pattern maintains link synchronization and provides an adequate signal transition density to keep the receiver PLL circuits in lock. This was chosen for its unique pattern which never occurs in data or command messages. Thus sync can be used to establish byte boundaries. An important point of consideration is that the sync pattern utilized by the TAXI chipset keeps the automatic gain control (AGC) fiber optic transceiver circuits in their normal range because the pattern has zero dc offset. As data does not have to be sent every byte cycle, parallel data throughput in bytes/sec can be slower than the minimum specified transmission rate (40MHz, 32Mbs) for example illustrates the situation.

The data rate is set by an external crystal oscillator which runs at the byte rate. An internal PLL multiplies the byte rate by 10, 11 or 12(depending on whether the TAXIs are to be

programmed in the 8, 9 or 10 bit mode) to arrive at serial transmission rate. TAXI's use 4B/5B and or 5B/6B encoding schemes to expand each byte by two bits

The first operation of reception is that the AM7969 TAXI receiver accepts the message patterns into its shifter. On the next byte clock cycle pattern is parallel loaded into the decoder latch. One clock cycle later the pattern is passed through the data encoder, recognized either as data or command and captured by the appropriate output latch. The receiver thus detects the difference between data and command patterns and routes each to the proper output latch. A new data or command byte is then issued from the latch and accompanied by a data or command strobe. Byte rate clock information is also extracted from incoming patterns and provided for use by the receiving system. This is the general principle of operation of the TAXIchip system. Having understood the general block diagram it will be easier to consider the functionality of each of the building blocks of the TAXIchip system.

2.2 AM7968 TAXI transmitter - A functional description

The block diagram representation of the AM7968 transmitter is shown in figure 2.2. The transmitter essentially consists of an input latch, an encoder latch, a data encoder, a shifter and a media interface. The following sub-headings will deal in detail about each of these building blocks.

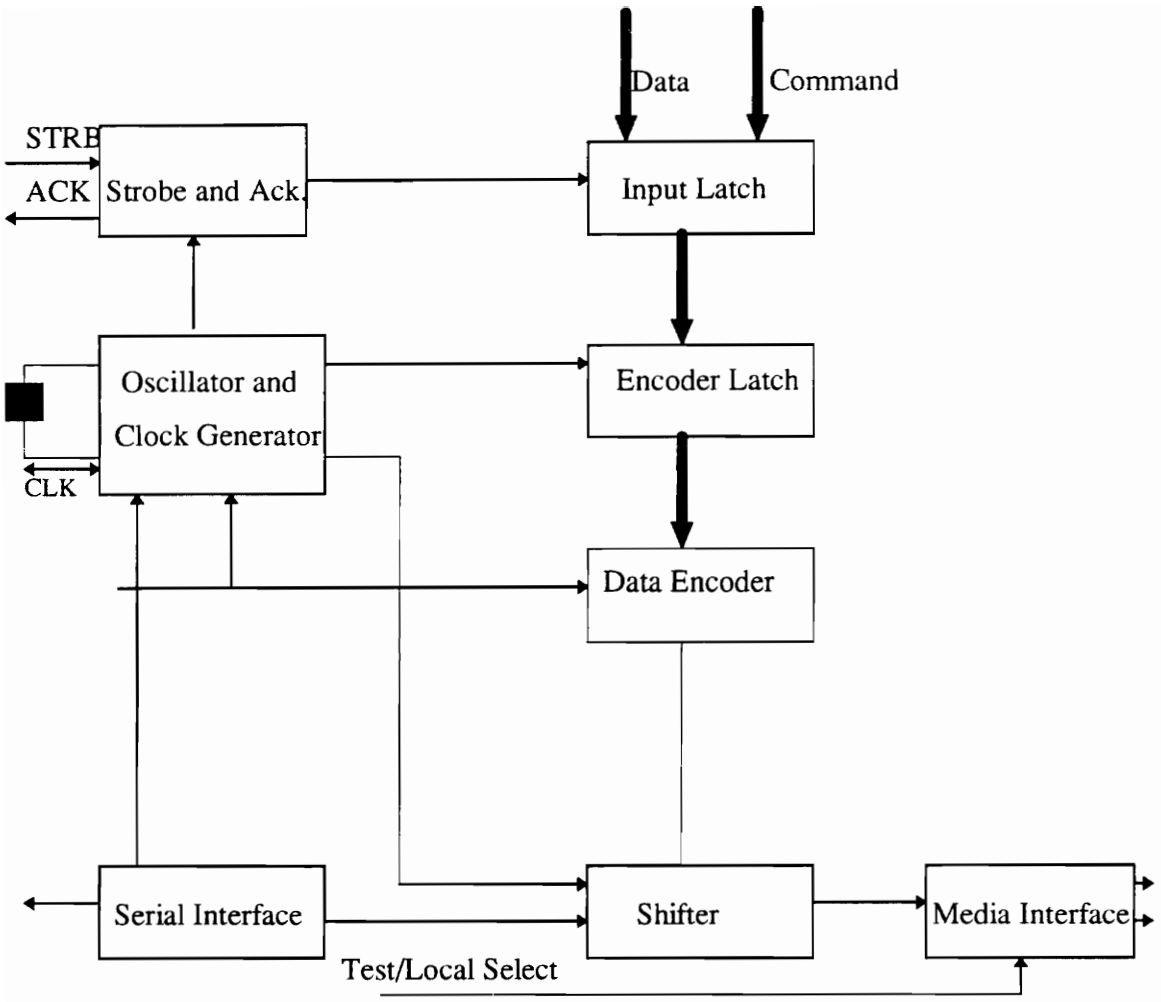


Figure 2.2 TAXI chip transmitter block diagram

2.2.1 CRYSTAL OSCILLATOR/CLOCK GENERATOR

The serial link speed is derived from a master frequency source(byte rate). This can either be the built-in crystal oscillator or a clock signal applied through X_1 pin . This signal is buffered and sent to the clock output when the transmitter is in the local mode.

2.2.2 INPUT LATCH

Asynchronous strobing of data and command signals is accommodated by the input latch by length divided into two stages. If STRB is asserted when both stages are empty, data/command bits are transferred directly to the second stage of the input latch and ACK rises shortly after STRB. This pattern will now move to encoder latch at the next falling edge of CLK. An input pattern is strobed into the first stage of the input latch only when the second stage is busy(contains previously stored data). The transmitter will be busy when STRB is asserted a second time in a given CLK cycle. Contents of the first stage are not protected from subsequent STRB's within the same CLK cycle. At the falling edge of CLK previously stored data is transferred from second stage to the encoder latch and new data is clocked into the second stage of the input latch. If in local mode ACK will rise at this time.

2.2.3 ENCODER LATCH

Input to the encoder latch is clocked by an internal signal synchronous with the shifted byte being sent on the serial link. Whenever a new input pattern is strobed onto the input latch it is transferred to the encoder latch at the next opportunity.

2.2.4 DATA ENCODER

The data encoder encodes 12 data inputs (8, 9 or 10 data bits or 4, 3 or 2 command inputs) into 10, 11 or 12 bits. The command data inputs control the transmitted symbol. When all are low data is sent unless a command is sent.

2.2.5 SHIFTER

The shifter is parallel-loaded from the encoder at the first available byte boundary. The shifter is being serially loaded at all times. As data is being shifted out of the transmitter the shifter fills from the LSB. If parallel data is available at the end of the byte; it is parallel loaded into the shifter and begins shifting out during the next clock cycle. Otherwise the serially loaded data fills the next byte. The serial data which loads into the shifter is generated by an internal state machine which generates a repeating sync pattern.

2.2.6 MEDIA INTERFACE

The Media interface is differential ECL referenced to +5V, capable of driving lines transmitted with 50Ω up to (V_{CC} -2) volts.

2.3 AM7969 TAXI Receiver- A functional description

The block diagram representation of the AM7969 receiver is shown in figure 2.3. The AM 7969 receiver essentially consists of an output latch, a decoder latch, a data decoder, a shifter a clock generator and a media interface. The following sub-headings will deal in detail with each of these building blocks.

2.3.1 CRYSTAL OSCILLATOR/CLOCK GENERATOR

It provides the data recovery PLL with the reference frequency at the expected byte rate of the data to be recovered. It is either a built-in crystal oscillator or an external CLK signal applied through the X_1 pin. Reference frequency source is then multiplied by 10(for 8 bit), 11(for 9 bit) or 12(for 10 bit) using an internal PLL.

2.3.2 MEDIA INTERFACE

SERIN+ and SERIN- inputs are to be driven by differential ECL voltages referenced to +5V. Serial data at these inputs will serve as the reference for PLL tracking.

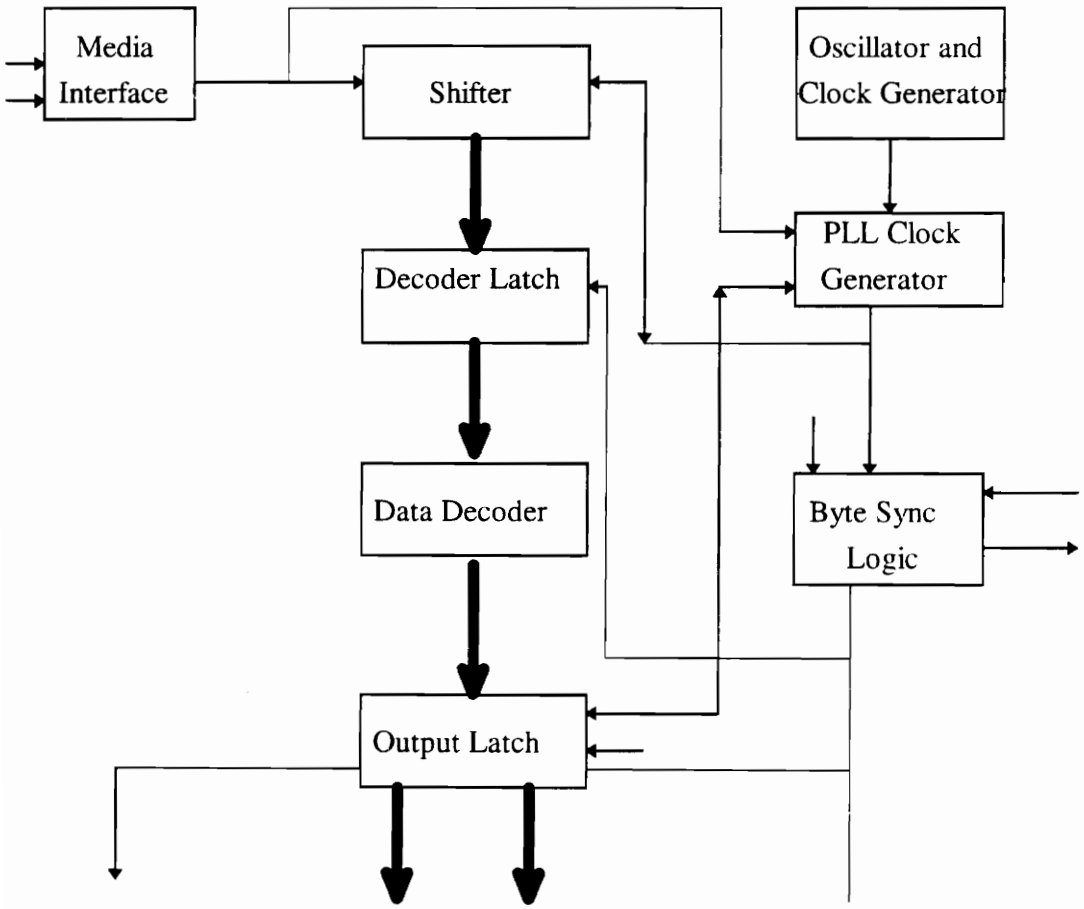


Figure 2.3 AM7969 TAXIchip receiver block diagram.

2.3.3 PLL CLOCK GENERATOR

A PLL clock recovery loop follows the incoming data and allows encoded clock/data stream to be decoded into a separated clock and data pattern. It makes use of the crystal oscillator and clock generator to predict the expected frequency of data and will track jittered data with a characteristically small offset frequency.

2.3.4 SHIFTER

It is serially loaded from media using the bit clock generated by the PLL.

2.3.5 BYTE SYNC LOGIC

The incoming data stream is a continuous stream of data bits without any significant signal which denotes byte boundaries. The byte sync logic will continuously monitor the data stream and upon discovering the data reserved code used for AM7969 Receiver Sync will initialize a synchronous counter which counts bits and indicates byte boundaries.

2.3.6 DECODER LATCH

Data is loaded from the shifter to this latch at each symbol/byte boundary. It serves as the input to data decoder.

2.3.7 DATA DECODER

It decodes the encoded 10, 11 or 12 data input to 12 outputs. It separates data symbols from command symbols and causes the appropriate strobe to be asserted.

2.3.8 PARALLEL OUTPUT LATCH

Output latch will be clocked by the byte clock and will reflect the most recent data on the link. Data pattern and command pattern will be latched to the respective outputs without affecting each other. Any data transfer either data or command signal will be latched to their respective output strobes. However there will be CSTRB's when there is no active data since sync is a valid command code. Any pattern which does not decode to either of these patterns is flagged as a violation. Output of the decoder during these violations is indeterminate and will result in either CSTRB or DSTRB output when the indeterminate pattern is transferred to the output latch.

This completes the functional description of the AM7968/ AM7969 TAXIchip system.

2.4 Operational Modes

The TAXI chip can be operated in a variety of modes such as TEST mode, LOCAL mode and CASCADE mode. A brief summary of these different modes of operation will be presented in this section. Apart from these modes of operation the TAXI system can also support Synchronous and Asynchronous operations. Local mode consists of a single Transmitter communicating with a single receiver over a serial medium. Cascade mode for the Am7968/Am7969-125 consists of a single transmitter driving two or more cascaded receivers over a single serial medium. The link may also be run in the test mode with external frequency multiplying and data tracking phase locked loops in order to verify the link.

2.4.1 Local mode

In Local mode operation a single Transmitter/ Receiver pair is used to transfer 8, 9 or 10 bits of parallel data over a serial link. Local mode essentially has a very fast and efficient

data throughput since data can be transferred on every clock cycle. Yet another advantage is that the host need not match the data rate set by the TAXI oscillator since the AM7968 automatically sends a SYNC pattern during each clock cycle in which no new data or command messages are being transmitted.

2.4.2 Cascade Mode

The cascade mode of operation is essentially for wide parallel buses. Each TAXIchip receiver monitors the serial link and a special acknowledgment scheme is used to direct symbols into each of the TAXI receivers. The AM7969 Receivers have their serial input pins tied to the optical data link while the IGM (Appendix A) of each TAXI receiver is connected to CNB of its next downstream neighbor. However the CNB of the first receiver is tied HIGH making it the only receiver in the chain that can act on the first non-sync pattern in a message.

2.4.3 Test Mode

The test mode switches can make the parts determinate, synchronous systems, instead of statistical, asynchronous ones. An automatic test system will be able to clock each part through the functional test patterns at any rate or sequence that is convenient. After the logic has been verified, the part can be put back into the normal mode, and the PLL functions verified knowing that the rest of the chip is functional.

2.5 Data Encoding, Violation and Syncs

In any communication system serial data transmission requires some form of encoding before the data are output to the transmission medium. Principles of encoding adopted in

the TAXI system will be discussed in detail in the next chapter. Violation logic adopted in the TAXI along with the TAXI error mechanism will be discussed in detail. The violation logic of the TAXI decodes the incoming data patterns and detects violation in data and command patterns. In the absence of data or commands a unique symbol(SYNC) is generated to maintain the synchronization of the link. This will also be discussed in relation with the error management of the TAXI system in the next chapter.

CHAPTER 3.0
DATA ENCODING, DECODING AND ERROR MECHANISMS

This chapter will introduce the coding rules used in the TAXIchip and develop on their characteristics which are important from a system designer's point of view. The electrical characteristics of the 4B/5B codes will be discussed in detail which is the code used to encode data in the TAXIchip system. The characteristics of the decoder will also be discussed when the inevitable data corruption will occur. The application of using the TAXI codes on some simple system protocols will also be discussed. The violation logic incorporated in the TAXI system is capable of detecting the common types of transmission errors.

3.1 TAXIchip encoding rules

Any data transmission system is prone to errors. It is mandatory for the system designer to obtain a complete understanding of the possible failure modes and characteristics of the system over which data is to be transmitted. Data is sent as either 8, 9 or 10 bits wide over the TAXI system. To simplify the encoding and decoding circuitry the data stream is divided into smaller groups. If a 8-bit data is sent it is divided into two 4-bit data and encoded using a 4B/5B encoder to produce a 10-byte data. 9-bit data is broken into a 4-bit and a 5-bit data and encoded using a 4B/5B and a 5B/6B encoder to produce a 11-bit data. A 10-bit data is broken into two 5-bit data and encoded using two 5B/6B encoders to produce a 12-bit byte.

The next step in this process is to serialize the encoded patterns and convert it from a Non-Return-to-Zero to Non-Return-to-Zero-Invert-ones(NRZI). This step is carried out to assure that there is sufficient number of transitions and adequate information for the data/clock recovery circuitry to track. The important property of any code chosen is that it

must have a minimum density of transitions for the Phase Locked Loop synchronizer to acquire the clock and there must not be a large interval without transitions. The TAXI code convention provides a maximum of four bit times between transitions and a minimum number of transitions per encoded symbol.

Apart from the clock synchronization issue some other issues have also been taken into account while deciding on the codes. Electrical interfaces intended for TAXI have also been taken into account . While AC coupled and DC coupled systems have varied effects on the system performance, the TAXI codes have been selected so as to provide the lowest offset. These concerns are important when we consider a DC -coupled and an AC-coupled TAXI-fiber optical interface. The unequal high and low times of the TAXI codes result in imbalance. This imbalance is a function of the codes effect on the media and can effect serial communication in many ways. It will be interesting to consider the effect of offset on fiber optic receiver modules. The main effects include a shift in the receiver amplifier automatic gain control circuit(AGC), or limiting the minimum usable signal level. By themselves these may not pose a serious threat to the system performance but they must be taken into consideration in the overall system design. The threshold shift in AC coupled systems can cause jitter in the data stream which must be removed by the receiving end. To obtain a better understanding of the above mentioned effects it will be useful to define and conceptualize the underlying principles of DC offset,threshold shift and consider a few typical examples. The next section will deal in these while introducing with a simple example of 4B/5B encoding.

3.2 DC Offset characteristics of TAXI codes

Figure 3.1 shows an example of 4B/5B encoding. The sequence of events starts off with data being converted from its Hexadecimal form to the 4B/5B equivalent. The case

depiced is for a 8-bit data and hence uses two 4B/5B encoders. It is then converted to its NRZI equivalent.

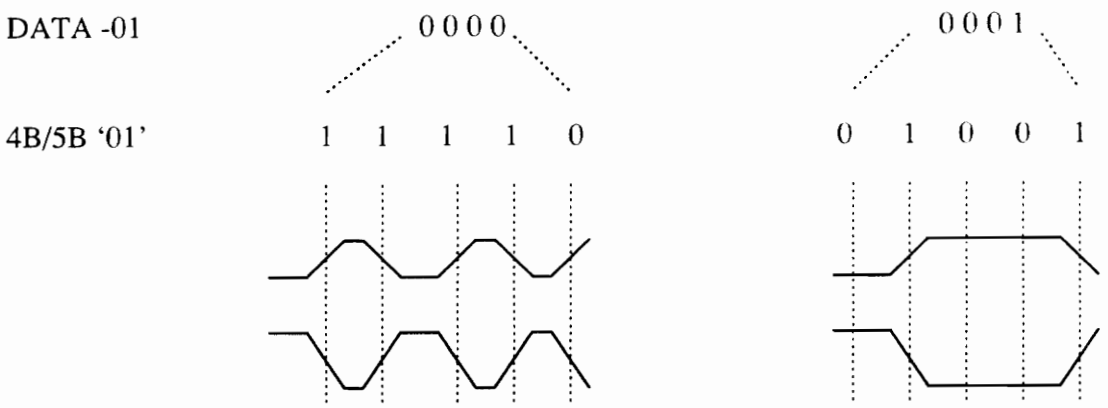


Figure 3.1 Example of 4B/5B Encoding

In figure 3.1 a transition indicates a data '1' while a no transition indicates a data '0'. The NRZ to NRZI transition is accomplished in a TAXI system by exclusively-oring the serial NRZ data with the previous data and buffering it through an ECL output buffer.

To examine the effect of DC offset let us consider an example of a 4B/5B offset as shown in figure 3.2 .

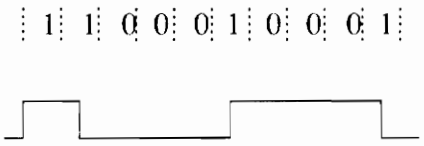


Figure 3.2 Example of a 4B/5B offset

In the above illustration it is clear that the pattern is DC balanced as there are equal number of highs and lows(5 Highs and 5 Lows).

3.3 TAXI System Error Management

Typical error sources in an optical fiber communication system include signal dispersion (i.e. spreading out of signal in time), gain shifting (the bandwidth required to transmit a given data pattern varies as a function of that data) and thermal noise in the receiver. Although optical fiber has an unlimited bandwidth, optical data links do not. The bandwidth limitation of the optical component can contribute to the gain shifting problem. Optical data converters are also susceptible to thermal noise which may manifest as signal jitter or impulse noise. Let us now briefly consider the various TAXI error mechanisms and their management.

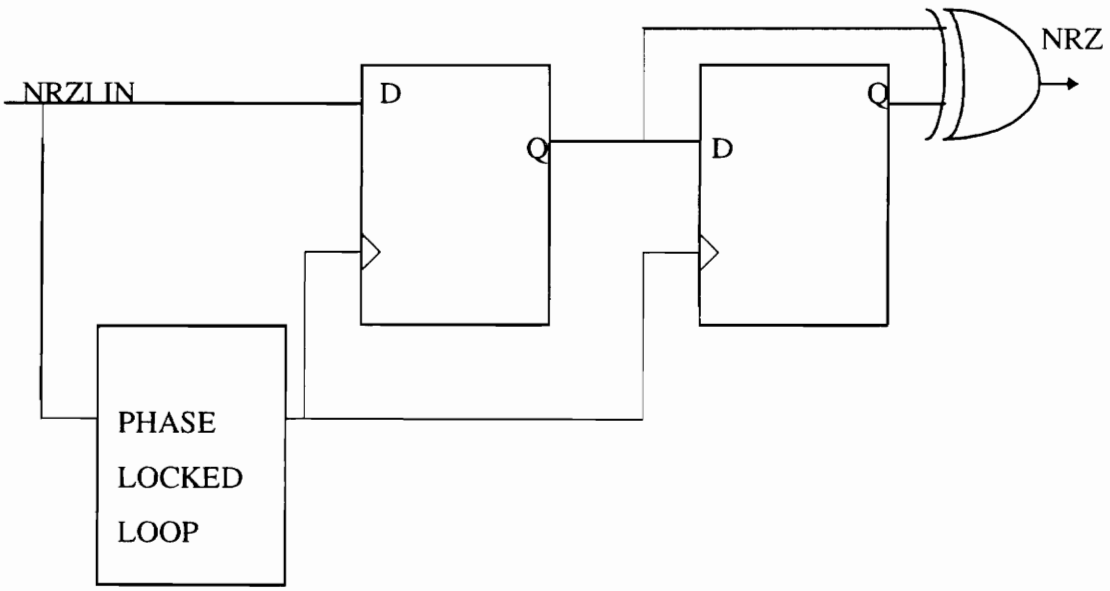


Figure 3.3. Model of TAXI receiver input.

The effect of phase jitter and impulse noise on NRZI decoding can be examined using the conceptual model of the TAXI receiver input circuit shown in Figure 3.3. The phase locked loop adjusts the phase of the sampling clock so that the data transitions occur in

the middle of the clock cycle. The NRZI is decoded into Non-Return-to-Zero by comparing each sample to the previous example. A zero is decoded if the current sample is the same as the previous one. Figure 3.4 illustrates the error caused due to the jitter and impulse on the decoded NRZ data.

When a received data pattern does not represent a valid coding symbol, the Am 7969 TAXI receiver activates its 'VLTN' pin to indicate that the current data is a 4B/5B coding violation. However, the Am7969 Receiver cannot detect the occurrence of a bit error that transforms one valid symbol into another valid , but incorrect, symbol. This means that a transmission error can change a valid data symbol into a different valid data symbol, or in a very few cases, into a valid command symbol. However the transformation of a valid command symbol into another valid command symbol is precluded by the TAXI coding scheme.

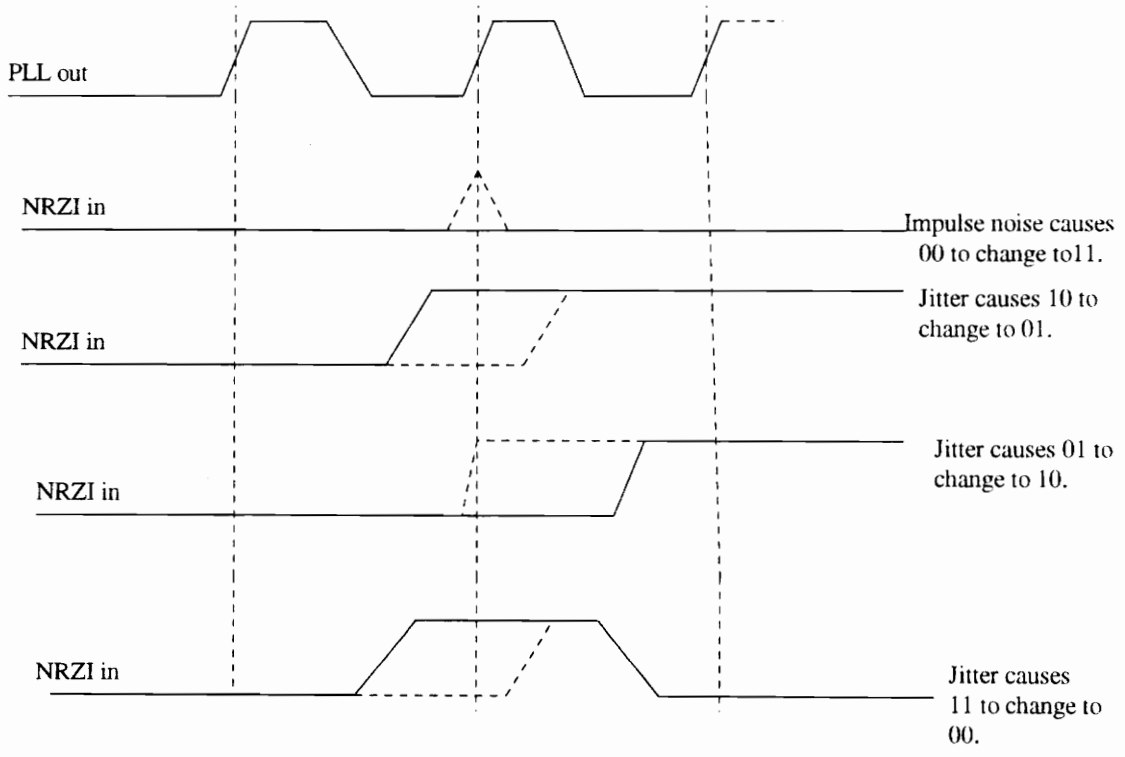


Figure 3.4. Sampling errors caused by impulse noise or jitter.

The probability of an undetected error in a communication channel can be reduced by increasing the redundancy of each transmission by adding one or more coded checkbits to every data message. The more redundancy, the smaller the probability that the error will escape detection. Methods of coding the checkbits vary in complexity, ranging from simply adding a parity bit to each byte of data, to powerful codes capable of correcting multiple burst errors in messages several kilobits long.

The simplest approach to TAXI error management is to rely on the resident violation logic which can detect illegal 4B/5B and 5B/6B codes. However this method is vulnerable to errors as discussed in the preceding paragraphs. Some other important approaches to TAXI error management include block-oriented error management, block checksum, Hamming codes, cyclic redundancy codes and Reed Solomon codes.

3.4 Bit Error Rate Considerations

The bit error rate of a communication channel determines the necessity for additional error detection and/or correction capability. For TAXI applications bit error rate performance in the order of 10^{-11} is acceptable. This error rate is suitably low for many TAXI applications. Since bit error rate is a function of signal to noise ratio at the receiver input, optical fiber, with its greater available bandwidth, noise immunity, and transmission efficiency, enables a TAXI link to operate over much greater distances, and at very high data rates. A typical application used in an optical slip ring is discussed in chapter 5. It is however evident that the optical fiber does not provide an error free environment. This medium is also susceptible to error producing effects similar to those in a co-axial cable, such as signal dispersion and gain shifting. Signal dispersion refers to the problem of signals spreading out in time while gain shifting involves the variation in the bandwidth required to transmit a data as a function of that data. Optical data links are very much bandwidth limited unlike optical fibers. It is this bandwidth limitation which contributes to the gain shifting problem. Optical data converters are also susceptible to thermal noise which may be manifested as signal jitter or impulse noise. Hence while designing the optical data link to be interfaced with the TAXI chipset these considerations need to be accounted for. The next chapter

will deal in detail about the optical transmitters and receivers and the associated design considerations for their interface with the TAXI chip.

CHAPTER 4.0

INTERFACING THE TAXI CHIP TO THE FIBER OPTIC MEDIUM

This chapter will deal with interfacing the TAXI chip to the fiber optic medium. DC coupled and AC coupled TAXI fiber optic transceiver interfaces will be introduced. Fiber optics has played an important role when the distance is too long, or the data rate is too high. In this context it is the next thought of the system designer to apply fiber optic interface to the TAXI system. Optical communication is favored when the transmission environment is noisy electrically or when the electromagnetic radiation from the wire is a concern. A detailed discussion of the inherent advantages of the optical medium is given in section 4.1. The transmitter and receiver design compatible with the TAXI chipset will be discussed in detail with special reference to the Hewlett Packard's HFBR - 510X/-520X series. Interface circuit guidelines involved in the TAXI interface will be discussed in detail. Hardware design consideration like the board layout is also addressed. This chapter will integrate the concepts introduced in the earlier chapters with the optical modules to present the user with a platform on which various applications can be realized.

4.1 Inherent Advantages of Optical Communication

The optical communication alternative comes into focus in light of the problems generated by the wire. Environmental noise coupling is eliminated in optical medium. There is no problem of optical cables being improperly grounded. The only portion of the link susceptible and sensitive to noise is the receiver end. This can also be easily controlled since it is contained within the host system which is receiving the data. To achieve this we can use a simple power supply filter. If the host system is very noisy we can apply electrostatic shielding. However traditionally the cost factor has always shifted the balance away from the fiber optic solution for short distance applications. A recent advancement to eliminate this disadvantage is discussed in the later sections.

4.2 Interfacing the TAXI chip to Fiber Optic Transmitters and Receivers

The TAXI chip can be used in conjunction with the optical components and optical fiber to form a simple fiber optic communication link as shown in Figure 4.1. Optical transmission has the advantages of immunity to Electromagnetic Interference, Radio Frequency Interference, low attenuation, electrical isolation, data security and wide bandwidth. These features favor the use of optical fiber as the serial media which will result in optimum performance of TAXI chipset link. The optical components namely the transmitters and the receivers can be chosen based on the nature of the application. While low power level applications may be addressed with the LED technology, high speed and high power level application may require the use of a laser diode capable of being modulated at very high frequencies. These applications will entail a higher cost of the components. The following sections will predominantly concentrate on the interface between the TAXI chips and the optical components.

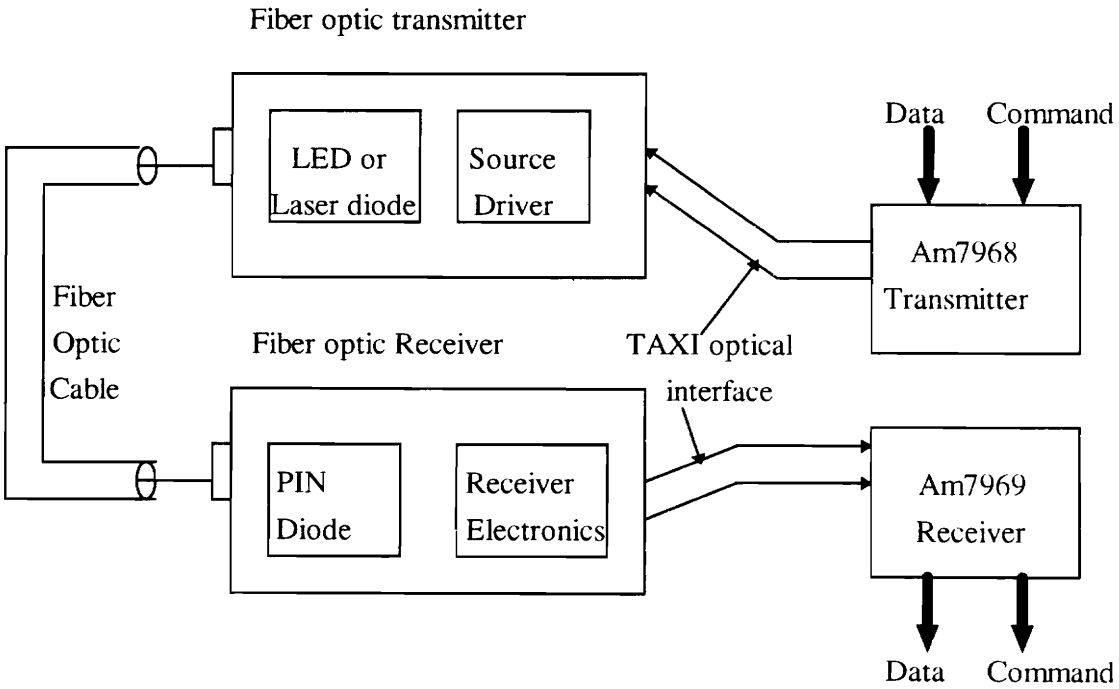


Figure 4.1. TAXI-based fiber optic link

The key elements of a digital optical link include the transmitter, the cable and the receiver. While designing an optical link, many interrelated variables such as the fiber source and photodetector operating characteristics should be considered. Performance and cost constraints are very essential constraints in fiber optic links. The main system requirements needed in analyzing slip ring optical link include:

(a) the desired transmission distance and link attenuation
(b) data rate or channel bandwidth, and
(c) bit error rate and power budget.

Many factors can change or distort the modulated waveform as it passes through the optical link. These changes may be attributed to the optoelectronic devices as isolated elements or due to their interaction with fiber optic transmission media. Bandwidth capabilities of sources, receivers and fiber optic transmission lines can limit the maximum rate of information transfer and signal format.

4.3 System Considerations

Since the communication system to be designed must support a high data rate advantage must be taken of the lower attenuation and minimum dispersion that occurs at wavelengths around 1300nm. However the choice of wavelength of operation is also influenced by the fiber material and properties as well as other system parameters. Hence the choice of operating wavelength can be made only after taking into account all these considerations.

The next consideration would be to interrelate the performance of the receiver, transmitter and optical fiber. In practice, characteristics of two of these elements are chosen and then the third is determined. We have decided to choose the receiver and transmitter characteristics and model the optical fiber accordingly.

Defining the logic level of the transmitter is very important. Since the proposed system is a very high speed system, ECL (Emitter Coupled Logic) is used. These circuits use -1.75V for low and -0.9V for denoting high state. Apart from the logic levels, the

transmitter has to produce the proper modulation code. A modulation code is a method of encoding digital data for transmission. The TAXI chip uses a NRZI code. In designing an optical fiber link, the format of transmitted signal is an important consideration because the decision circuitry in the receiver must be able to extract precise timing information from incoming input signal.

Since the required data rate is high and the system requires an inherent error detecting capability, the use of block codes is favored. It will be important to consider the distinction between data and signal rate. While data rate is the number of data bits transmitted in bits/second, signal rate is the number of symbols transmitted per second. Signal speed and data rate may not be the same depending on the modulation code used. For example, a NRZ code has the same signal and data rate, but for a Manchester code, the signal speed is twice its data speed. It must be emphasized that it is the baud rate and not the bit rate which is the true signaling speed of a system.

The output power of the transmitter is also of great significance. Since a laser diode drives 10 to 15 dB more optical power into a fiber than an LED and the lower dispersion capability of laser diodes favor its use as the optical source. The transmitter design needs further investigation and the specific requirements such as the desired coding, bandwidth and associated parameters of the proposed system have to be determined.

The receiver deals with the highly attenuated light signals. Hence it can be considered the principal component around which the design of a fiber optic system revolves. It is important to consider the fact that it is in the photodetector and first stage of amplification that the signal being transmitted is at its weakest and most distorted. Hence this can be considered as the central part of the link. In choosing a photodetector, we need to determine the minimum optical power that must fall on the photodetector to satisfy the bit error rate requirements at the specified data rate of 125 Mbps. Design, cost, complexity and sensitivity constraints dictate the receiver design. Dynamic range is also an important consideration. It specifies the minimum and maximum acceptable power levels .

4.4 DC-Coupled TAXI-Fiber Optic Transceiver Interface

DC coupling of the TAXI chip to the fiber optic medium is possible if the power supply requirements of the TAXI chip match those of the optical module. TAXI chipset power requirements are defined as V_{CC} = +5V and V_{EE} = GND. Moreover if the TAXI chipset and the optical module are connected to the same power and ground planes, a DC coupling will be sufficient. When passing data between the TAXI chipset and the optical module logic levels of the TAXI chip and the optical components must be matched since the data transfer is taking place at a very high speed and any mismatch will result in corruption of data received. A block diagram of the DC coupled TAXI fiber optic interface is shown in figure 4.2. It will be clear from the diagram that the TAXI chipset and the optical module are placed very close to each other and this eliminates the necessity of transmission line transitions.

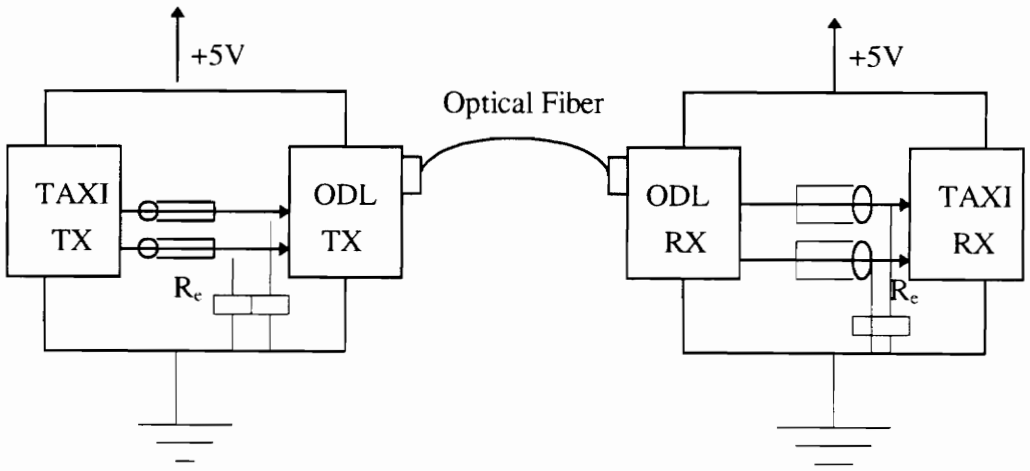


Figure 4.2 DC Coupled TAXI Fiber Optic Interface

In the above interface the purpose of the resistance R_e is to eliminate line reflections. This serves as a pull down resistor. It reduces the line reflections by reducing the reflection coefficient. However it is important to point out here that if the DC coupled interconnection is greater than three inches line terminations are required. The termination can be provided by introducing two resistances R1 and R2 in parallel in both the transmitting and receiving ends.

4.5 AC Coupled TAXI-Fiber Optic Interface

Some applications will require the TAXI chipset to optical transceiver link to be AC coupled. This situation will arise if the supply voltages of the optical components do not match those of the TAXI chipset. AC coupling via capacitors is shown in figure 4.3.

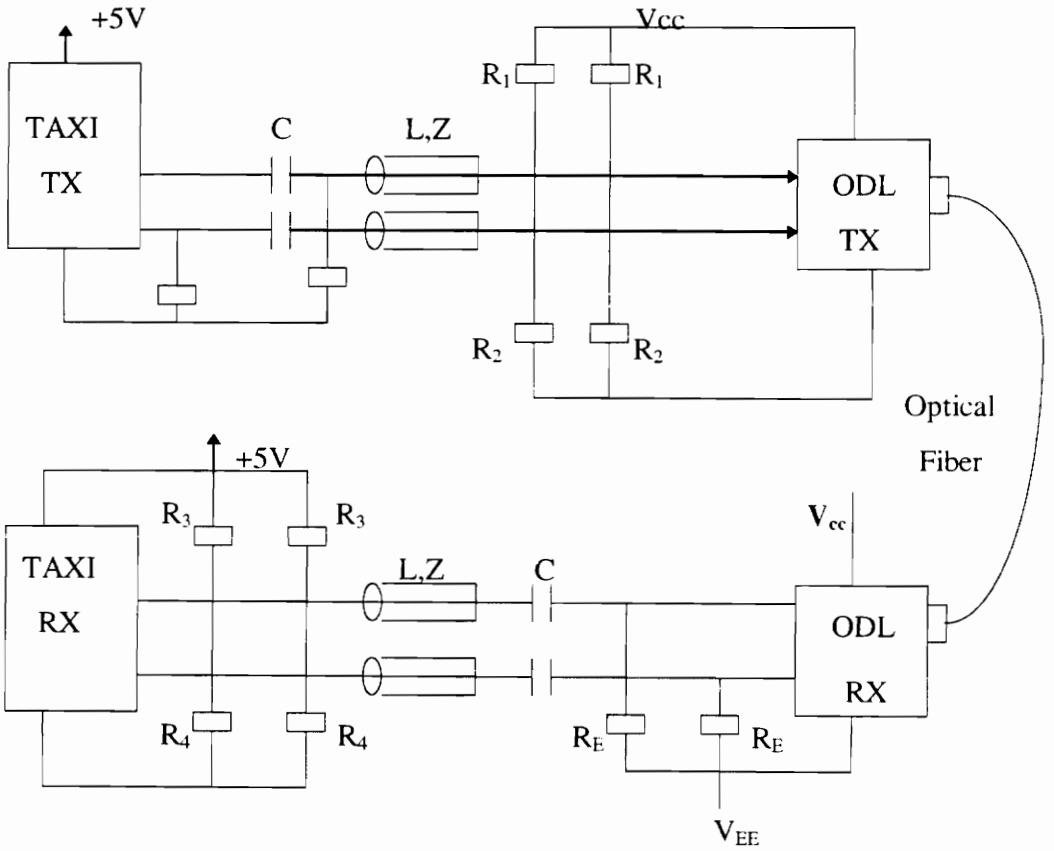


Figure 4.3 AC-Coupled TAXI Fiber Optic Interface

In the configuration shown R_E is the ECL output pull down resistor, C provides the AC coupling Z_o is the characteristic impedance, and R_1 and R_2 provide a matched line termination and bias voltage to the optical component's logic swing.

Design:

$$\frac{R1R2}{R1+R2} = \frac{R3R4}{R3+R4} = Z$$

$$V_{bb} = \frac{V_{IH} + V_{IL}}{2} = V_{EE} + \frac{(V_{CC} - V_{EE})R_2}{R_1 + R_2}$$

$$\frac{5R_4}{R_3 + R_4} = 3.7\ V$$

The connection diagram shown in figure 4.3 holds for any line length L, which separates the TAXI chipset and the optical module.

4.6 Layout Considerations for Fiber Optic Data Links

Fiber optic data links involve very small signal levels. This requires care in their layout. Any fiber optic data link receiver essentially consists of the photosensitive diode and an amplifier. The photo-diode essentially converts the light pulses into currents of around a few hundred nano-amps. This signal current is then amplified and translated into an ECL signal. The TAXI receiver being digital in nature switches currents in the order of milliamps. This switching noise is capable of corrupting light pulse data. It is essential to ensure that the signal and the noise do not flow in the same path. To achieve this we need to separate the optical ground plane and the power plane from the ground plane and the power plane used by the rest of the digital circuits. The following sections will deal in detail with the transmitter and receiver designs and their layout considerations for the interface.

4.7 Optical Transmitter Design

In this discussion two different transmitter designs will be dealt. The first transmitter design involve the use of a 10mw laser diode. In this design emphasis will be placed on the design considerations for the laser diode driver circuitry. This transmitter design will involve low speed applications wherein data rates up to 40 Mbps can be achieved. However the power output of this transmitter is much higher than the power level of the second transmitter design. The second transmitter design will be based on the Hewlett Packard's HFBR 510X/520X series of fiber optic transmitters and receivers.

4.7.1 Transmitter Design using Melles Griot laser diode

The objective of the design is to design a laser driver circuit for the available Melles Griot laser with the following specifications:

Peak output power = 10mW Operating current = 45mA

Threshold current = 32mA

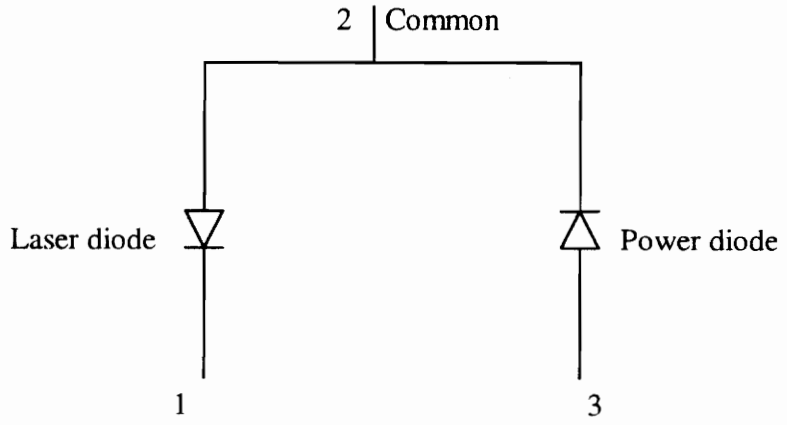


Figure 4.4 N-type configuration of the laser diode

The laser diode driver circuit design is based on the M66512 laser driver chip. The chip supports the N-type configuration of the Melles Griot laser diode which is shown in figure 4.4.

The driver is capable of providing upto 120mA of driving current with the current cutoff capability. It requires a single 5V power supply. The laser driving current is controlled by the externally applied voltage. Dual control voltage inputs, VL1 and VL2 precisely control the driving current. Laser output power is monitored through both the TTL level comparator output and the analog output. The PIN configuration of the laser diode driver chip is shown in Figure 4.5. The laser driver chip can support only upto 40 MHz switching speed. However it was sufficient to conduct the initial tests on the fluorescent dyes. The next step in this direction would be the development of a laser driver circuit capable of supporting 80 MHz switching speed. A brief description of the PIN configuration is given in Table 4.1.

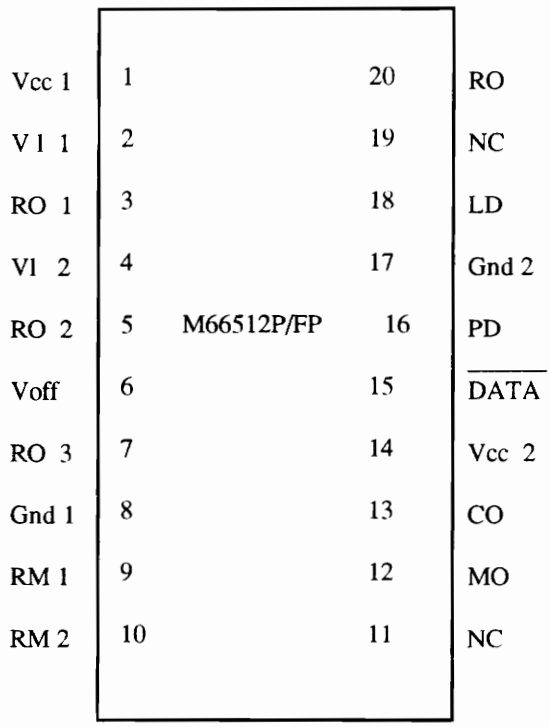


Figure 4.5 Pin configuration Mitsubushi M66512P/FP laser diode driver chip

Table 4.1 PIN configuration description of the M66512P/FP laser diode driver chip.

Terminal	Pin No.	Name	Function
LD	18	Laser output	To be connected to the laser diode cathode
PD	16	Monitor output	To be connected to the photo diode anode
VL 1	2	IL 1 control i/p	Voltage to set current source o/p current
R0 1	3	Load resistor	A load resistor for IL1 is connected to GND.
Vl 2	4	IL 2 control i/p	Voltage to set current source o/p current
RO2	5	Load resistor	A load resistor for IL 2 is connected to GND.
RO3	7	Load resistor	A load resistor for IL 3 is connected to GND.
DATA	15	Switching data	Digital data to switch the laser diode is applied.
RM 1 RM2	9 10	Monitor load resistor	A load resistor is connected between these two terminals to convert the monitor PD current/voltage
MO	12	Analog monitor	Voltage through RM1 and RM2 appears.
CO	13	Digital monitor	TTL level comparator o/p.
Voff	6	Laser current cut-off input	Internal current source are disabled when Voff is in 'L' level.
RO	20	Load resistor	A load resistor for the laser driving current.
Vcc 1	1	Power supply	Power supply terminal for analog circuit.
Vcc 2	14	Power supply	Power supply terminal for digital circuit.
GND 1	8	GND	GND terminal for analog circuit.
GND 2	17	GND	GND terminal for digital circuit.

4.7.1.1 *Control of laser driving current*

There are three current sources namely the IL1, IL2 and IL3. These current sources are controlled independently. The laser driving current required is 45mA. This could be achieved by the suitable combination of these three current sources.

$$IL = IL1 + IL2 + IL3 \qquad (1)$$

Now

$$IL1 = 12 * VL1 / R1 \qquad (2)$$

In this design the supply voltage is utilized to obtain VL1 and VL2 using a voltage divider circuit. Hence we have a voltage of 2.5V for VL1 and VL2.

Let us assign IL1 at 20mA , IL2 at 10mA and IL3 to vary. From (2) we have R1 ≅ 1.5K Ω. Similarly we have R2 = 6*VL2 / IL2. Thus we have R2=40K Ω. For R3 we utilize the internal reference voltage Vref and is given by R3 = 10*Vref / IL3. Vref is typically 1.4V. A variable potentiometer can be used for R3 to a value of 2K. TTL level digital data to switch laser diode is applied to terminal 15. Voff terminal is useful during power on stage to prevent rush current to laser diode. Laser output power is monitored by the included photodiode. A load resistor for internal current sources is connected between the RO and Vcc terminals. The voltage on RO terminal should be greater than 2.5V and then the value of load resistor is given by

$$RO(\Omega) = Vcc - 2.5V / \text{Maximum current(A)}$$

$$= 2.5 / .05A = 50\Omega$$

The laser driver includes a reset circuit which disables all the current circuits when Vcc is below 3.5V. Apart from these it is required to use an electrolytic capacitor between the Vcc1 and GND1 to stabilize the power supply. This is the basic design of the laser driver circuit for the given specifications of the laser and the circuit has been fabricated according to the design. The laser is operating currently in the continuous mode and further efforts could focus on building a circuit to support 80 MHz switching speed.

4.7.2 Design of a low cost fiber optic transmitter and receiver pair for the optical data link

The transmitter receiver design problem has been approached by considering the transmitter and receiver sections separately. The product line chosen for this design is based on the Hewlett Packards's HFBR-14X2 transmitter and HFBR-24X6 receiver. A brief description of each of these chips will be followed up with the design of the drive circuits for the transmitter and recommended ac Coupled Receiver circuit. A brief outline of the recommended design rules for the PCB design will also be included.

4.7.2.1 *High Speed Low Cost Fiber Optic Transmitter*

The HFBR-14X2 fiber optic transmitter contains an 820nm GaAlAs emitter capable of efficiently launching optical power into four different optical fiber sizes: 50/125μm, 62.5/125μm, 100/140μm and 200μm PCS. In our final working prototype this gives us the flexibility to choose the fiber size that is suitable for the application. The high coupling efficiency of the transmitter allows the transmitter to be driven at low current levels resulting in low power consumption and increased reliability of the transmitter. The HFBR-14X2 can typically couple -11.5dBm of optical power at 60mA into 100/140μm fiber cable. The double lens optical system assures consistent coupling efficiency.

4.7.2.2 *Recommended Drive Circuits*

The drive circuit used to supply current to the LED transmitter can significantly influence the optical switching characteristics of the LED. The optical rise/fall times and propagation delays can be improved by using certain circuit techniques. The LED drive circuit utilizes current peaking to reduce the typical rise fall times of the LED and a small pre-bias voltage to minimize propagation delay differences that causes pulse-width distortion. The circuit is expected to produce rise/fall times of 3ns and a total jitter including pulse-width distortion of less than 2ns. This circuit is definitely suitable for high speed data communications at signal rates upto 125 MBd.

4.7.2.3 *125 MHz Low Cost Fiber Optic Receiver*

The HFBR-24X6 Fiber Optic Receiver is designed to operate with the Hewlett Packard HFBR-14X2 fiber optic transmitters and supports the fiber optic cables supported by the transmitter. The lensed optical system assures consistent coupling into the receiver. The receiver output is an analog signal which allows follow -on circuitry to be optimized for a variety of distance/data rate. This analog signal can be converted into logic compatible form by using suitable low cost components. The HFBR-24X6 receiver contains a PIN photodiode and low noise transimpedance preamplifier integrated circuit. The optical signal received by the receiver is converted to an analog voltage. The output is a buffered emitter follower Due to the large signal amplitude this signal is much less susceptible to EMI, especially at high signal rates. A receiver dynamic range of 23dB over temperature is achievable if we assume BER to be 10^{-9}. The frequency response is typically dc to 125 MHz. Although it is analog receiver, it is made easily compatible with the digital systems.

4.8 Layout Rules For Through Hole Fiber Optic Transceiver

The PC board must be designed with a ground plane. To minimize the inductance from the ground and power leads to the transceiver separate power plane may be used. The cuts or openings in the ground and power plane must be minimized to reduce the parasitic inductance. Connections between the drive circuit and HFBR-14X2 must be of minimum length. This minimizes the noise emitted by the transmitter and improves the optical rise/fall time of the LED. To minimize the noise emitted by the transmitter and improve the optical response time of the LED a large 10μF capacitor and a 0.1μF capacitor should be located as close to the circuit which drives the LED. The low pass filter must be used to protect the fiber optic receiver from noise that is present in the 5V power supply.

This completes the discussion of the fiber optic transmitter and receiver design for interfacing with the fiber optic medium. The next chapter will deal with the applications of the TAXI chip to fiber optics.

CHAPTER 5.0
APPLICATIONS OF TAXI COMMUNICATIONS IN FIBER OPTICS

The previous chapters have systematically developed the concepts of the TAXI chipset and its application to the fiber optic medium. This chapter will involve the application of the acquired concepts to real time systems. A specific application of the TAXI chipset and associated communication systems to a slip ring used in medical imaging systems will be discussed in detail. The emphasis of this chapter will be on the different fiber optic approaches that were contemplated and experimented for the proposed ***Optical Slip Ring.*** The practical difficulties encountered in each of the approaches will be discussed and experimental results have also been included. The different fiber optic approaches include the nonlinear optics approach and the distributed scattering approach. A brief overview of the approaches will be presented in the following sections.

5.1 Slip Ring Communications

A slip ring is an electromechanical device that serves the purpose of passing data from stationary to rotating or rotating to stationary structures. The slip ring assembly consists of a metallic ring and a metallic brush that has a metallic and electrical contact with the ring. In the CT scanner the ring rotates while the brush is stationary. Figure 5.1 gives the simplified block diagram of the slip ring communication channel.

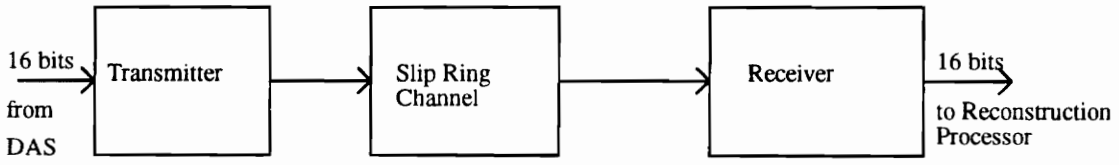


Figure 5.1. Slip ring communication channel.

The above block diagram represents a simplified version of a rotating circuit that accepts 16-bit wide parallel data, converts it into a serial bit stream, and modulates it for the channel. The modulated serial stream is then sent off to the slip ring assembly where data

is placed on the rotating ring and picked up by the stationary brushes. The serial data stream is then passed to the demodulator and converted back into a serial data stream 16 bits wide. This is the basic principle of operation of the slip ring communication channel. In the following sections a brief discussion of the existing communication board architecture for the rotating and stationary communication boards is presented. Accompanying each of these discussions is a list of system modifications that would be required to operate the communication boards at 125 Mbits/sec.

5.2 Stationary Communication Board

The existing stationary communication board provides a 5MByte/sec full duplex communication link between the rotating and stationary parts of the gantry. The stationary communication board essentially transmits the stationary controller (STC) CPU data. The stationary controller contains the stationary communication board (SCOM). The SCOM board also transmits the scan control commands. It receives the on board controller CPU data, the data acquisition subsystem data and data control. Basically, the two SCOM operations can be described as one which has no STC CPU intervention and one that enables the STC CPU to communicate with the on board controller CPU on the gantry.

The SCOM mother board consists of the TAXI transmitter that is essentially the transmit modem board, the TAXI receiver that serves as the receive modem board and an optional Stationary Automatic Retry Query (SARQ) board that serves to ensure the data integrity of the DAS data. The TAXI transmitter and receiver boards are of primary concern in our attempt to design the board to operate at 100-125 MHz.

5.3 Rotating Communication Board

The Rotating Communication Board (RCOM) provides a 5 Mbyte/sec full duplex communication link between the rotating and the stationary components of the slip ring gantry. The rotating communication board essentially transmits the On Board Controller (OBC) CPU data. The On Board controller contains the rotating communication board (RCOM). The RCOM board also transmits the DAS data and DAS data control. It

receives the STC CPU data and the scan control commands. Basically the RCOM operations can be classified into two operations; one which has no OBC CPU intervention and one that enables the OBC CPU to communicate with the on board controller CPU on the gantry.

The RCOM mother board consists of the TAXI transmitter that is essentially the transmit modem board, the TAXI receiver that serves as the receive modem board and an optional Rotating Automatic Retry Query (RARQ) board that serves to ensure the data integrity of the DAS data.

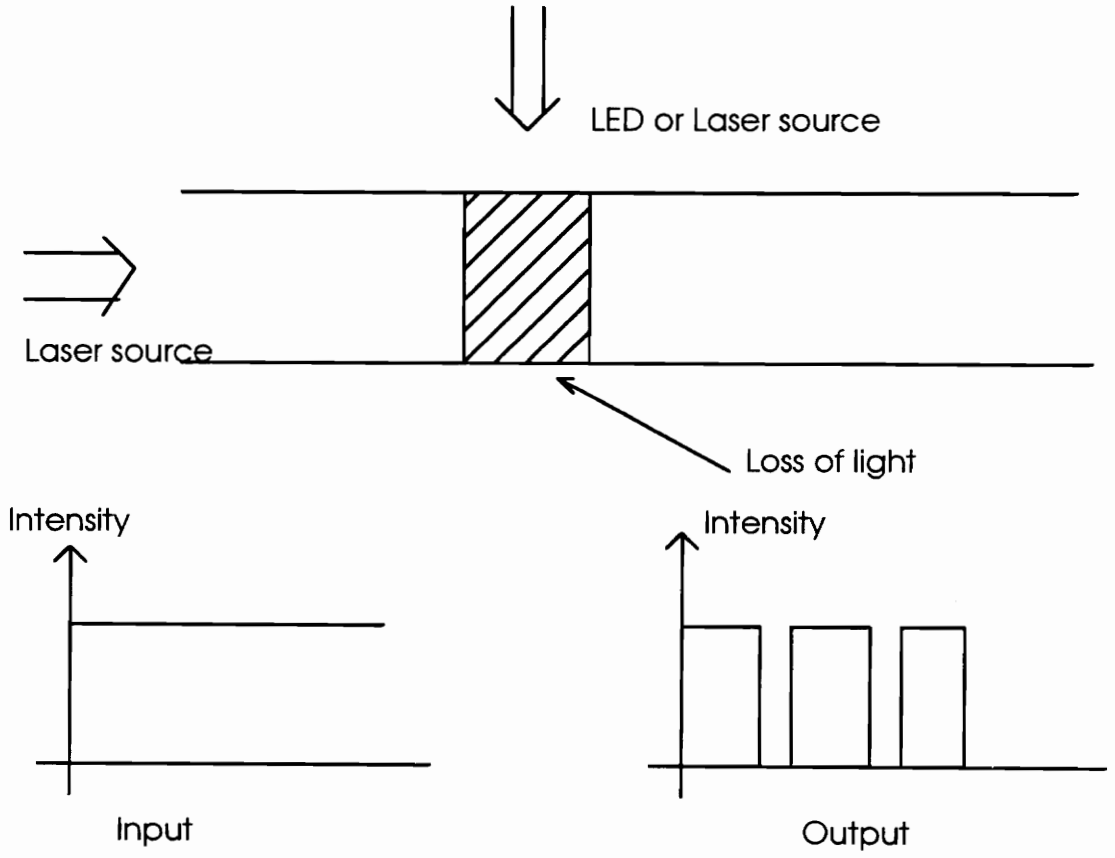
5.4 Non-Linear optics Approach

Non linear optics has witnessed intense activity during the last few years. The use of optical fibers for pulse compression is a well known application of the nonlinear optics. Among the important nonlinear effects are the Stimulated Raman and Brillouin scattering, optically induced birefringence, parametric four-wave mixing and self-phase modulation. Soliton effects were discovered as a result of interplay between dispersive and nonlinear effects. The interest in nonlinear optics is expected to increase in view of the development of photonics-based technologies for information management.

5.4.1 Schemes suggested for the current application

Extensive literature survey was carried out to determine the applicabillity of the nonlinear effects approach as a third possible alternative for the optical slip ring. The key to the utilization of the nonlinear effects approach lies in exploiting the changes which take place in the refractive indices when the fiber is suitably modulated by an external laser source.

In the first scheme a laser source is injected from one end of the fiber while another LED or laser source is used to externally modulate the fiber. A schematic of the proposed scheme is shown in figure 5.2. The nonlinear properties of the semiconductor materials doped on the fiber is utilized. The $CdSxSe_{1-x}$ are responsible for the special nonlinear properties of this glass type. Advantages of semiconductor doped glasses as nonlinear materials include homogeneity, and good mechanical and chemical stability. On further analysis of this scheme the use of semiconductor doped glasses does not seem to be a very favorable option. A table of nonlinear susceptibility and nonlinear refractive index as a function of wavelength is given for five different types of semiconductor doped glasses is given in table 5.1.



Fig, 5.2 Schematic of the external modulation approach on a semiconductor doped fiber

Table 5.1 Nonlinear optical properties of semiconductor glasses
χ =non linear susceptibility n_2 =refractive index

Glass type	χ	n_2	wavelength	pulse duration
RG 610	$1*10^{-10}$	$2, 1*10^{-8}$	590	0.1
RG 695	$3*10^{-9}$	$2,1*10^{-8}$	694.3	10
CS 3-68	$1,3*10^{-8}$	$7,4*10^{-8}$	532	10
CS 2-73	$5*10^{-9}$	$3,2*10^{-8}$	580	10
Y 52	$1,3*10^{-9}$		532	0,15

As is evident from the table the maximum wavelength of observation is only 694.3nm. The dispersive losses in the fiber is lowest in the wavelength range of 1.3μm. Moreover the TAXI communication system design is being designed for a wavelength of operation above 800nm. Moreover the doping of semiconductor materials on the silica fiber can lead to many materials issues and the cost effectiveness of the approach is yet to be determined. However this scheme is yet effective in producing pulsed outputs and further investigations are going on to determine the cost effectiveness of the scheme.

In the second approach the reflected light coming out from a fiber, which is externally modulated by a high power laser is utilized for producing the pulsed output. The main constraint of this approach is the cost of the high power laser involved. Alternative sources in the form of laser diode arrays are being considered to offset the huge costs involved with these high power lasers.

The reflectivity R is given by $R=(n-1/n+1)^{1/2}$ where $n=n_1/ n_2$ represents the ratio of the refractive index of the core and the cladding. Assuming a reflectivity of 0.01% the

required refractive index change was found out to be of the order of 10^{-4}. The power reflected can be sensed with a PIN photodetector which can detect up to 10nw of power.

5.5 Distributed Scattering Experiment

A new and promising approach has evolved as yet another alternative for the optical slip ring prototype. The approach is a non-contact approach utilizing a scattering effect on an optical fiber. The Figure 5.3 illustrates a fiber stretched along its length and uniformly heated for a particular length by a torch. The heating of the fiber results in the generation of scattering sites in the fiber. When a laser source impinges on the surface of the heat-treated fiber, the photons are scattered at these sites, and some of these photons are captured by the waveguide and transmitted. The transmitted optical signal is detected using a silicon detector and the power output is measured using an optometer. It is important to note here that the scattering also causes attenuation so the power collected in the fiber will diminish as it travels down the fiber. Attenuation coefficients measurements were made using different fiber samples. The scattering coefficient measurements were based on the following assumptions. Let P1 denote the power measured at the nearer end to the heated portion of the fiber. Let P2 denote the power measured at the farther end of the fiber. Let L be the length of the heated portion. Then the scattering coefficient ξ is given by

$$\xi = 10^* \log(P1/P2) /L \qquad (1)$$

The scattering experiment measurements along with some important observations is listed below.

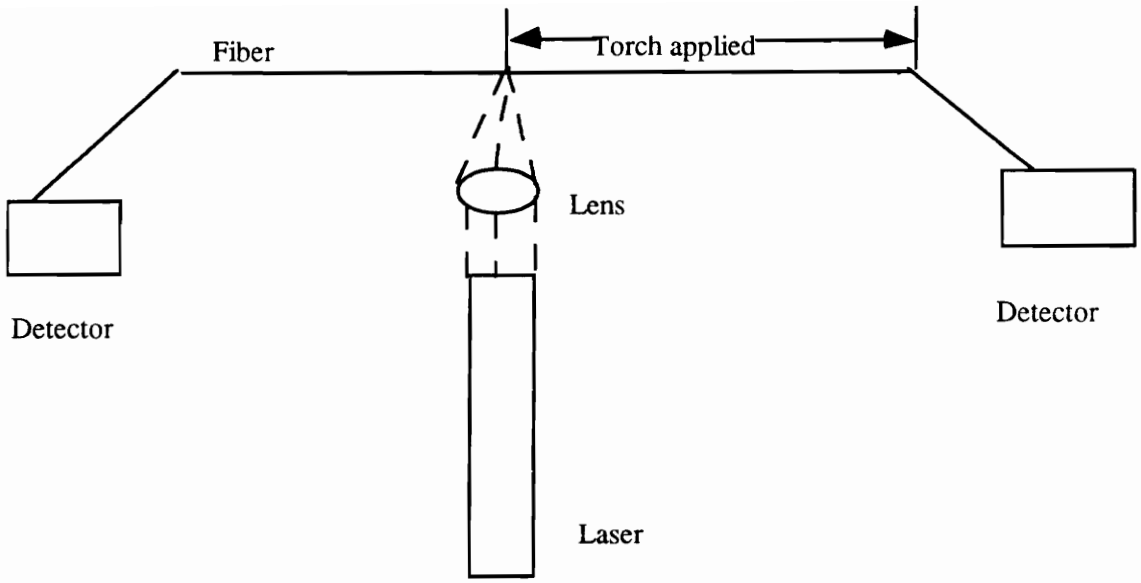


Figure 5.3 Experimental setup for the distributed light scattering approach

Sample 1 : HCS plastic clad optical fiber by Ensign Bickford

core diameter : 201 μm

cladding diameter : 300 μm

Test 1

P1 = 24.61nw P2 = 25.31nw

L=16cm

ξ = 10*log(24.61/25.31) / .16 dB /m =1.4 dB/m

Test 2

P1 = 26.38nw P2 = 27.04nw

L=16cm

ξ = 10*log(26.38/27.04) / .16 = 1.38dB/m

Sample 2 EO Tec plastic clad fiber by 3M

core diameter = 201 μm

cladding diameter = 300 μm

Test 1

P1 = 29.4 nw P2 = 30.78nw

L= 16cm

ξ = 10*log(29.4/30.78) / .16 = 1.47dB/m

Test 2

P1= 30.1nw P2 =30.78nw

L= 16cm

ξ = 10*log(30.1/30.78)/.16 = 1.396dB/m

Sample 3 Glass clad fiber by polymicro

core diameter = 200 μm

cladding diameter = 240 μm

Test 1

P1 = 6.3nw P2 = 9.1nw

L =0.57m

ξ = 10* log(6.3 / 9.1) / 0.57 dB /m = 7.1dB /m

Some important observations that have surfaced after the above experiments were conducted are:

(1) The attenuation coefficient is very critical to our application as the scattering coefficient determines the amount of loss that takes place along the length of the fiber and

this consequently affects the strength of the communication signal received at the end of the loop fiber which will be laid along the circumference of the slip ring.

(2) Another important observation has been that the core size plays a very important part in the distributed scattering effect. The above tests conducted on a 62.5/ 125 μm core/clad glass fiber failed to produce the desired results. However the results obtained from the plastic fiber tests have been very promising.

(3) The dopants present on the glass fiber may play a significant role in determining the scattering coefficients.

The main focus on this approach is to couple more light into the fiber so as to make the communication signal as strong as possible. Further experiments are underway to establish the reliability of the approach. Bending measurements to determine the mechanical properties of the fiber after heating the sample have also been performed. Extensive reliability tests have been conducted on the approach and the results obtained are encouraging. The scattered power measured was observed to be consistent with the measurements obtained during the initial tests. In order to determine the power coupled as a function of the time for which the fiber was heat treated, exposure time tests were conducted on the fiber and the results obtained have been tabulated in Table 5.2. The exposure time test essentially involved the exposure of the fiber to heat for different time periods and obtain the power scattered for each of these time periods.

Table 5.2 Experimental observations for different exposure times of the scattering experiment

Time of exposure(seconds)	Scattered power measured(nW)
5	0.345
60	8.4
120	10.8
180	21.2
300	60.8
500	120.4
1000	380.6
1200	468.4
1300	520.3
1400	580.4
1500	600.2
1600	640.4
1700	720.3
1750	770.6
1800	840.5
1900	860.5
2000	880.3

Sample 1: EO Tec plastic clad fiber by 3M core diameter = 201μm cladding diameter = 300μm

An interesting observation from the observed readings is that the scattered power increases with the increase in exposure time of the fiber to the flame. The distributed scattering approach is suitable for application purposes since it does not involve any contact mechanism. The approach entails a very low cost. However there is a drawback in the approach. The fiber becomes very brittle after being heat treated. A practical working prototype can however be developed and tested using the distributed scattering approach. This application of the TAXI chip to fiber optics is a very novel approach and can be the platform for the new generation medical imaging systems.

6.0 CONCLUSIONS

The systematic study and development of the TAXI communication system has been completed. Extensive literature survey and research papers have brought to light some of the commonly encountered problems in the communication system. In this chapter some of these problems will be addressed. The situations discussed solely concentrate on the fiber optic medium.

From a system designer's point of view it is desired that that the TAXI receiver's output be predictable and stable when TAXI transmitter stops transmitting. In a fiber optic-coupled system the designer must be able to use the TAXI receiver in a system where the TAXI receiver must appear inactive under the above mentioned condition. There are two possible ways of addressing this problem. If the optical receiver has a carrier detect output this signal may be used to flag an inactive state. If there is no such signal, the system designer can generate one using an ECL (Emitter Coupled Logic) one shot arrangement which will detect loss of edges after a predetermined period which can be set by the designer. The design of this time period is based on the desired response to loss of data.

Another point of consideration is the period of time for which the Reset pin of the TAXI chip has to be held low to insure the TAXI chip has been reset. The resetting action is carried out to allow graceful recovery from the rare occurrence of a PLL lock-up due to noise bursts on the serial data lines, as may occur when light is removed from certain optical links. In a fiber optic coupled system, loss of optical signal may cause the optical receiver to oscillate, causing the TAXI receiver to track the oscillation to an indeterminate frequency. Care must be taken to avoid the oscillation, or a reset can be used to recover from it. After reset the PLL begins tracking incoming data and the byte boundary remains undefined until the transmitted data includes a Sync. The sync is a unique bit pattern which forces the receiver to align itself to the correct byte boundary.

It can also be concluded that the TAXI chipset offers an easy-to-implement and reliable solution for high speed point-to point data links. However like all communication data links, the TAXI link is also susceptible to the introduction of errors from a variety of sources. However the rate of occurrences of these errors is sufficiently small that they are of little or no consequences in many applications. Due to data coding schemes used by the TAXI, the effects of transmission errors are manifested in non-obvious ways. However these error mechanisms are well understood and can be dealt effectively.

REFERENCES

1) AM7968/AM7969 TAXIchip™ Handbook, Advanced Micro Devices.

2) Govind P. Agrawal, Non Linear Fiber Optics(Academic Press, Inc.,1992).

3) P.N.J.Dennis, Photodetectors-An Introduction to Current Technology(Plenum Press, 1986).

4) Rodger E.Ziemer and Roger L.Peterson, Introduction to Digital Communication, (Macmillan Publishing Company, 1992).

5) Govind P.Agrawal, Fiber Optic Communication Systems(John Wiley and Sons, Inc., 1992).

6) Hewlett Packard Application Bulletin 78, Low Cost Fiber Optic Links for Digital Applications up to 155MBd.

7) Hewlett Packard Application Note 1066, Fiber Optic Solutions for 125MBd data communication aPPLICATIONS at Copper Wire Prices.

VITA

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