Current-Mode Control of a Magnetic Amplifier Post Regulator

by

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(ABSTRACT)

An analysis is presented on current-mode control of a magnetic amplifier post regulator. Small-signal models for a magnetic amplifier reset method are developed for post regulators operating in continuous conduction mode. A design procedure is given and experimental verification of the model is provided.

Acknowledgements

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I. Introduction

Multiple-output power supplies are used extensively in industry. When more than one of these outputs needs to be regulated, some sort of secondary regulation may be required. There are several ways to provide secondary regulation of multiple-output power supplies. Of these ways, magnetic amplifier post regulators are becoming increasingly popular.

Magnetic amplifiers and saturable reactors were used widely as self-oscillators, current senses, switches, etc. before semiconductor switches superseded their popularity. Recent development of amorphous magnetic materials with square B-H loops and reduced losses at high frequency has rekindled interest in using magnetic amplifiers as switches.

Many advantages make magnetic amplifiers attractive as post regulators: high efficiency and reliability, low parts count, high power density, simple control

circuitry, and low EMI. Also, since they present high impedance during main switch turn on, turn-on loss of the main converter switch is reduced.

Recently, models of the small-signal control loop behavior of the magnetic amplifier have been developed [1-7]. These models provide a basis for stabilizing the control loop and designing control circuitry for enhanced performance. Use of these models and typical magnetic amplifier regulation has been limited to single-loop voltage-mode control. Voltage-mode control is a scheme where the output voltage is fed back and used to modulate the leading edge of the voltage through the saturable switch.

However, current-mode control enhances performance and enables current sharing when the outputs are paralleled. Current-mode control is a scheme where both the output voltage and output filter inductor current are fed back to achieve regulation. In this thesis, an investigation of current-mode or multi-loop control of the magnetic amplifier regulator is reported. Control models, a control circuit design procedure, a discussion of the benefits of voltage- and current-mode control, and experimental verification are provided for the magnetic amplifier post regulator.

The operation of the magnetic amplifier switch is reviewed in Chapter II. The control method of the switch is discussed and different reset methods are presented. Small-signal models of the magnetic amplifier post regulator are described in Chapter III. An overview of conventional PWM switch-mode current-mode control for a buck converter is presented in Chapter IV.

Current-mode control models for the magnetic amplifier post regulator are presented in Chapter V. The analytic method used to model the current-mode controlled magnetic amplifier is based on the PWM current-mode control model of a buck converter reviewed in Chapter IV. Design examples are given and experimental results are compared with theoretical results. Conclusions regarding the advantages and disadvantages of magnetic amplifier current-mode control are drawn in Chapter VI.

II. Magnetic Amplifier Operation

Figure 2.1 shows a common magnetic amplifier post regulator configuration with a forward converter as the main regulator. The forward converter provides an alternating square wave voltage input to the magnetic amplifier secondary. The magnetic amplifier switch blocks the leading edge of the input square wave voltage, which is then rectified and averaged by an output filter. Regulation is achieved by modulating the switch blocking time. The magnetic amplifier switch blocking time is controlled by adjusting the control voltage, V_{reset}, based on the output. The details are discussed in the following sections.

2.1 Magnetic Switch

A magnetic amplifier or saturable reactor is an inductive element used as a controlled switch. It is wound on a core with a relatively square B-H loop

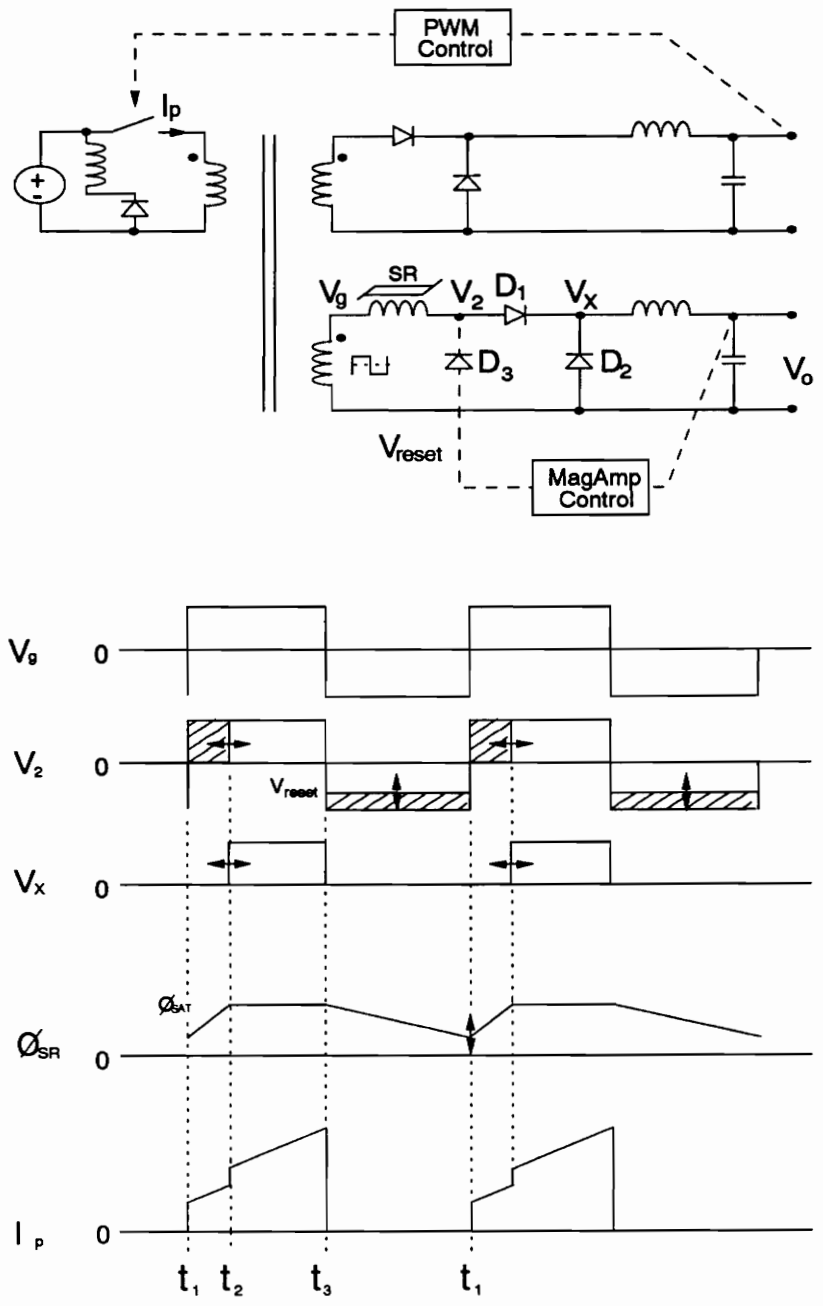


Figure 2.1. Forward Converter with a Magnetic Amplifier Post Regulator and Steady-State Waveforms.

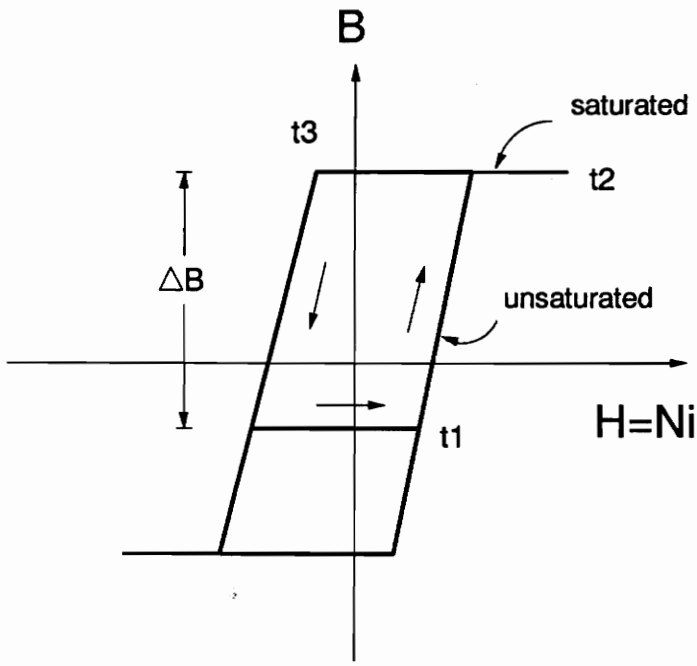


Figure 2.2. Operation on the B-H Loop of the Magnetic Amplifier Core.

(Figure 2.2) and, therefore, acts as a switch by being either saturated or unsaturated. When the core is unsaturated, it has a high inductance which blocks voltage; the current flow is very small (magnetizing current) and the magnetic amplifier acts as an open switch. When the core is saturated, it has very low impedance and allows the current to flow with very small voltage drop; thus, it acts as a closed switch. This switching action is the basis of the magnetic amplifier regulator technology.

Referring to Figure 2.1 and Figure 2.2, when the post regulator input voltage, V_g, goes negative at t_3, the voltage at V_2 is constrained by the control voltage V_{reset}. Since V_{reset} is less negative than the negative voltage applied at V_g, there is a positive voltage across the magnetic amplifier and current reverses through the magnetic amplifier, causing it to reset. The amount of reset volt-seconds, or ΔB, is determined by the difference between $V_{g\_}$ and the control voltage V_{reset} during the time V_g is negative (from t_3 to t_1). When V_g goes positive at t_1, V_g is blocked until the core becomes saturated at t_2. This requires the same volt-seconds as reset, thus

$$V_g(t_2 - t_1) = (V_{reset} - V_{g\_})(t_1 - t_3)$$

Therefore, by varying the magnitude of control voltage, V_{reset}, the reset volt-seconds are determined which in turn determine the blocking time. The procedure can be recapped with the following example: If V_o goes up, V_{reset} goes up (less negative), the reset volt-seconds increase, and the blocking time increases, thus bringing V_o down.

2.2 Reset Schemes

There are two ways to classify reset schemes. One is done according to the reset circuit and the other is done according to the reset power used. There are altogether four combinations.

2.2.1 Reset Circuit - Voltage and Current Reset

Figure 2.3 shows two types of reset circuits, voltage and current. With the voltage reset circuit, a control voltage is used to reset the magnetic amplifier. By varying the control voltage, the positive voltage across the magnetic amplifier during V_g's (Figure 2.1) negative swing is varied, thus changing the amount of reset which changes the amount of blocking time.

When the current reset configuration is used, a control current is used to determine the amount of reset. When the circuit reaches steady state, the flux resets to a dc level. Referring to Figure 2.1, as the input voltage, V_g, goes negative, D_1 turns off, and the output current freewheels through D_2. This causes the control current to flow back into the magnetic amplifier. This low frequency ac control current is added to the dc level, thus determining the

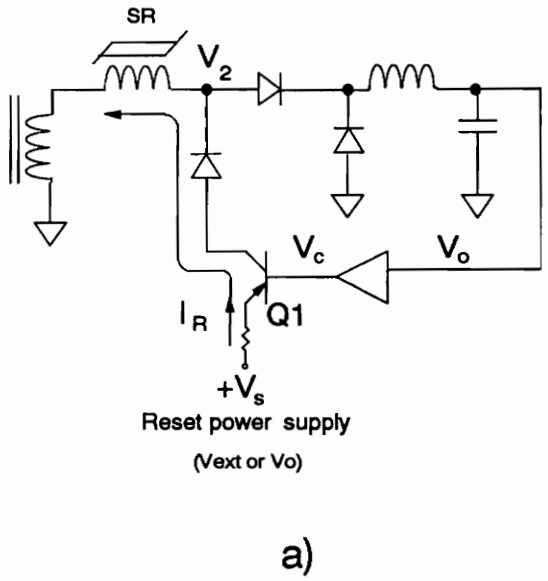


Figure 2.3. a) Current and b) Voltage Reset Circuits. [5]

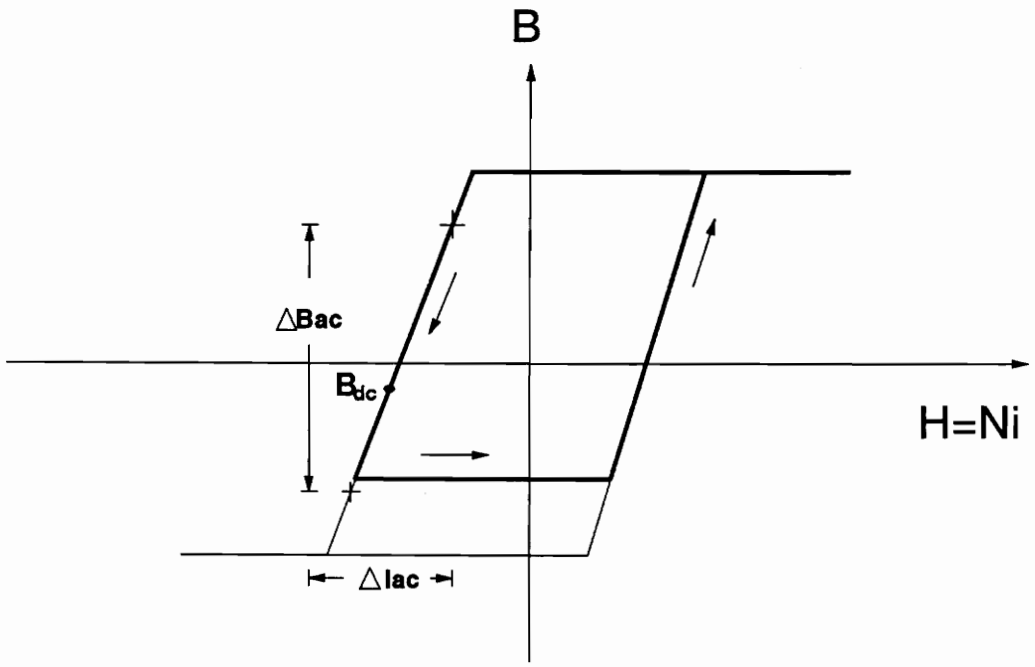


Figure 2.4. Current reset operation on the B-H Loop of the magnetic amplifier core. [5]

amount of reset. Figure 2.4 shows the current reset operation on the B-H loop of the magnetic amplifier core.

Referring to Figure 2.3a, the following scenario illustrates the current reset procedure: If V_o increases, V_{reset} decreases, causing the difference between V_s and V_{reset} to be larger, thus increasing the control current, I_R. This larger control current flows back into the magnetic amplifier, causing a longer reset, which results in a longer blocking time, thereby reducing the duty cycle and reducing V_o.

The current reset circuit of Figure 2.3a is used in this research because it does not require a negative supply in the control circuit and it exhibits lower phase lag at high frequencies than does voltage reset [5]. It should be noted that when the current reset configuration is used, the reset transistor, Q1, must be in its active region during reset, otherwise, the magnetic amplifier will be reset with a voltage and not a current.

2.2.2 Reset Power - Self Reset and External Reset

The reset of the magnetic amplifier requires power. This power can be supplied using an external supply (external reset) or can be supplied using the

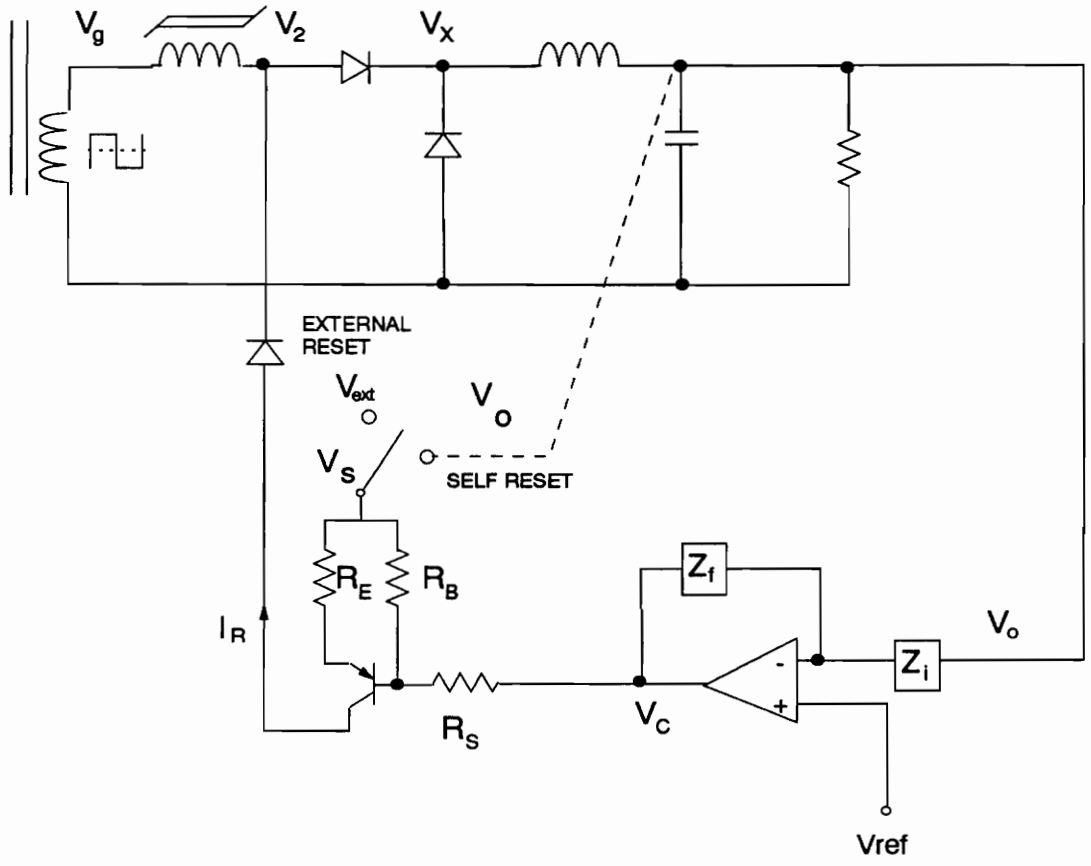


Figure 2.5. Self and External Reset Schemes.

output voltage of the post regulator (self reset). Figure 2.5 shows the two methods.

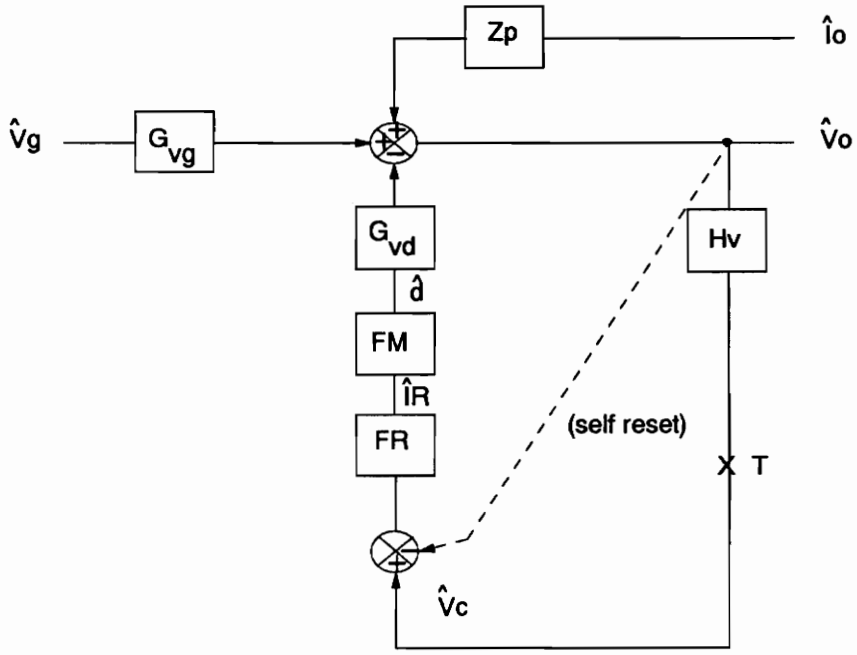
When the self reset scheme is used, the need for an external power supply is eliminated but short circuit protection is difficult to implement. When the output is short circuited, the supply voltage for the reset transistor becomes zero and there is insufficient reset voltage available to produce the large flux swing needed to block the next pulse. With the external reset scheme, the supply voltage for the reset transistor is not lost during a short circuit, so the magnetic amplifier can be designed to accommodate this short circuit condition.

The loop gains for the two different reset schemes vary significantly. The self reset method adds an extra feedback loop and causes a pole shift in the control loop gain [1-3].

III. Small-Signal Analysis of Voltage-Mode Control

In the past few years, there have been several papers characterizing the small-signal control loop behavior of the magnetic amplifier post regulator [1-7]. The formulas to approximate the small-signal loop transfer functions of the magnetic modulator and the reset circuit are explained in this chapter. These formulas will be used in the modeling of the current-mode controlled magnetic amplifier.

Figure 3.1 shows the equivalent small-signal model of a voltage-mode controlled magnetic amplifier post regulator (circuit shown in Figure 2.5). The transfer functions of the small-signal model are defined in the following sections.



$$Gvd = \frac{\hat{V}o}{\hat{d}} \qquad FM = \frac{\hat{d}}{\hat{I}R}$$

$$Gvg = \frac{\hat{V}o}{\hat{V}g} \qquad FR = \frac{\hat{I}R}{\hat{V}c}$$

$$Zp = \frac{\hat{V}o}{\hat{I}o} \qquad Hv = \frac{\hat{V}c}{\hat{V}o}$$

Figure 3.1. Small-Signal Block Diagram for Voltage-Mode Control

Table 3.1. Voltage Mode Control Transfer Functions

F_M	$\triangleq$	$\frac{\hat{d}}{\hat{I}_R} = \frac{0.4\pi\mu_m N^2 A_e f_s}{l_e V_g 10^8}$
F_R	$\triangleq$	$\frac{\hat{I}_R}{\hat{V}_c} = -\frac{R_B}{(R_B + R_S)R_E}$
G_{vg}	$\triangleq$	$\frac{\hat{V}_o}{\hat{V}_g} = \frac{D(1 + sR_cC)}{\Delta}$
G_{vd}	$\triangleq$	$\frac{\hat{V}_o}{\hat{d}} = \frac{V_g(1 + sR_cC)}{\Delta}$
Z_p	$\triangleq$	$\frac{\hat{V}_o}{\hat{I}_o} = \frac{R_l(1 + sR_cC)\left(1 + s\frac{L}{Rl}\right)}{\Delta}$
Δ	$\triangleq$	$1 + s\left((R_l + R_c)C + \frac{L}{R_L}\right) + s^2LC$
T	$\triangleq$	$F_M F_R G_{vd} H_v$
$T_{selfreset}$	$\triangleq$	$\frac{F_M F_R G_{vd} H_v}{1 + F_M F_R G_{vd}}$

3.1 Modulator Gain Transfer Function, F_M

The magnetic amplifier modulator gain F_M is defined by the ratio of the change in switch duty cycle to the change in reset current. This gain can be calculated using the following formula [3]:

$$F_M = \frac{\hat{d}}{\hat{I}_R} = \frac{0.4\pi\mu_m N^2 A_e f_s}{l_e V_g 10^8} \tag{3.1}$$

Where N is the number of turns, A_e is the cross section area of the core in cm^2, f_s is the switching frequency, l_e is the mean length of the core in cm, and V_g is the voltage across the transformer secondary during the magnetic amplifier blocking state. Appendix A gives a detailed derivation of this transfer function.

The average permeability, μ_m, is approximated by the following empirical formula:

$$\mu_m = \frac{(\Delta B)^2 f_s}{K_c P_L 10^6} \tag{3.2}$$

Where ΔB is the total flux density swing, K_c is a conversion factor (1.2 for Square 80 Permalloy, and 1.05 for Metglas 2714A), and P_L is the core loss density in watts/lb. The derivation of this formula is described in detail in reference [3].

3.1.2 Phase Delay of Magnetic Modulator

A phase delay associated with the magnetic amplifier modulator has been characterized in references [6,7]. This delay is caused by two factors. The first factor occurs because the reset of the magnetic amplifier occurs during the negative portion of the post regulator input square wave. This results in a delay of the leading edge of the power pulse. The other factor is attributed to the inductance of the magnetic amplifier during reset. When this inductance is combined with the impedance of the reset circuit, there is an L-R time constant which contributes to the delay.

The following formula characterizes the delay caused by the two factors:

$$\Phi_M = -(2D' + \alpha)\frac{\omega}{\omega_s}$$

where Φ_M is the modulator phase lag; D' is the duty ratio of the off time; α is the resetting impedance factor which is equal to 0 for a current source and equal to 1 when resetting from a low impedance source, and somewhere in between for an imperfect current source; and ω_s is the switching frequency in radians [6].

3.2 Reset Circuit Gain Transfer Function, F_R

The reset circuit transfer function is defined as the ratio of the change in error amplifier voltage to the change in reset current. The reset current, I_R, varies depending on which voltage is used to supply the reset circuit, (an external voltage or the output voltage [self reset]). When an external voltage is used, the following reset circuit gain transfer function is derived (see Appendix A for derivation):

$$F_R = \frac{\hat{I}_R}{\hat{V}_c} = -\frac{R_B}{(R_B + R_S)R_E} \tag{3.3}$$

Where the ratio of $R_B/(R_S + R_E)$ is typically 0.4 to 0.6.

When the output voltage is used to supply the reset circuit (self reset), the value of I_R becomes:

$$I_R = -\frac{R_B(\hat{V}_c - \hat{V}_o)}{(R_B + R_S)R_E} = F_R(\hat{V}_c - \hat{V}_o) \tag{3.4}$$

which illustrates the addition of an inner feedback path shown in Figure 3.1.

3.3 Power Stage Transfer Functions

The transfer functions G_{vd}, Z_p, and G_{vg} are the power stage transfer functions. G_{vd} is the control-to-output voltage transfer function:

$$G_{vd} = \frac{\hat{V}_o}{\hat{d}} = \frac{V_g(1 + sR_cC)}{(1 + s((R_l + R_c)C + \frac{L}{R_L}) + s^2LC)}$$

Z_p is the open-loop output impedance transfer function:

$$\frac{\hat{V}_o}{\hat{I}_o} = \frac{R_l(1 + sR_cC)(1 + s\frac{L}{R_l})}{(1 + s((R_l + R_c)C + \frac{L}{R_L}) + s^2LC)}$$

and G_{vg} is the open-loop audio susceptibility or input-to-output noise transmission transfer function:

$$\frac{\hat{V}_o}{\hat{V}_g} = \frac{D(1 + sR_cC)}{(1 + s((R_l + R_c)C + \frac{L}{R_L}) + s^2LC)}$$

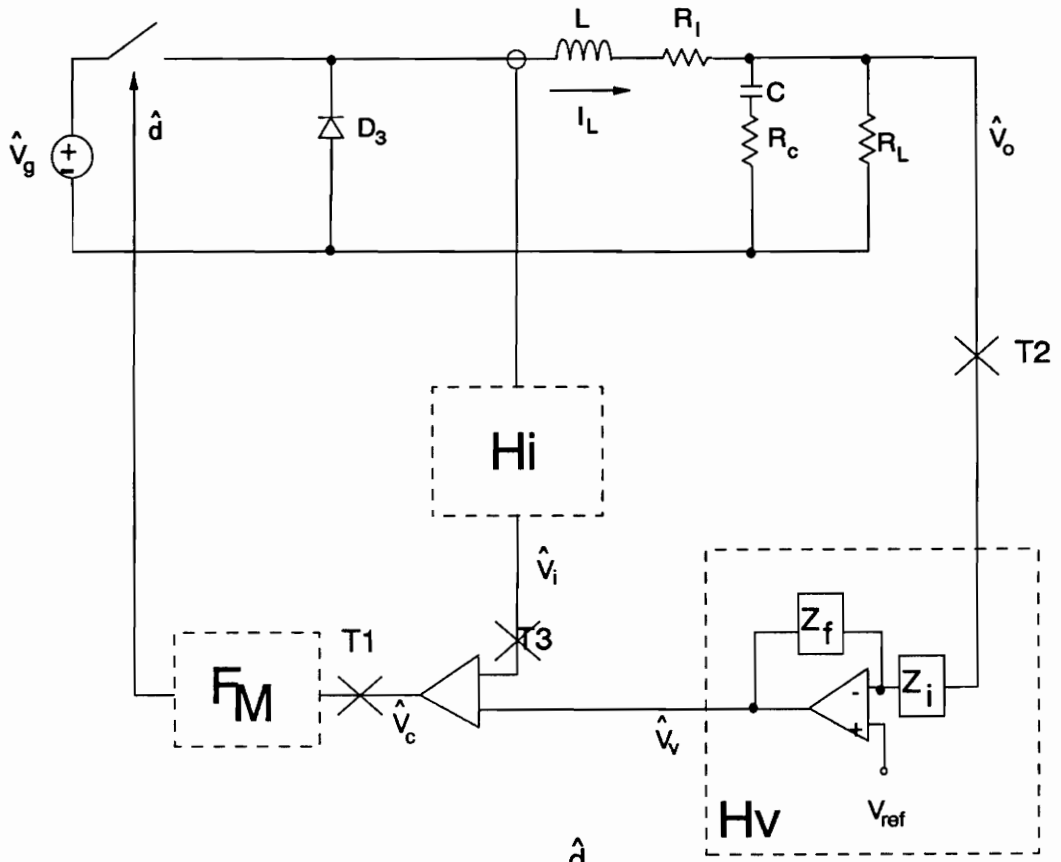
These transfer functions are derived using state-space analysis and are well known [8].

IV. Current-Mode Control

The operation of a magnetic amplifier post regulator is similar to the operation of a typical buck regulator, with the difference being the type of switch. Thus, the buck converter current-mode control model forms a basis for the magnetic amplifier current-mode control model which is discussed in Chapter V.

This chapter briefly reviews the conventional current-mode control model of a buck converter. The various loop gains are presented and discussed with regard to their contribution to dynamic performance. Design guidelines are given for enhanced dynamic performance. A more detailed discussion of this topic is presented in References [8-9].

4.1 Small-Signal Model of Current-Mode Control



Where $F_M \triangleq \dfrac{\hat{d}}{\hat{V}_c}$

$H_i \triangleq \dfrac{\hat{V}_i}{\hat{I}_L}$

$H_v \triangleq \dfrac{\hat{V}_v}{\hat{V}_o}$

Figure 4.1. Buck Converter with Current-Mode Control Blocks

Current-mode control describes a multi-loop control system in which both the output voltage and the inductor current information are fed back and used to modulate the duty cycle of the switch. Figure 4.1 shows a buck converter with the control blocks H_v, H_i and F_M outlined. H_v is the transfer function $\hat{V}_v/\hat{V}_o$ which describes the feedback of small-signal variations in output voltage. H_i is the transfer function $\hat{V}_i/\hat{I}_L$ which describes the feed back of small-signal variations in inductor current. The information from the output voltage feedback, $\hat{V}_v$, and the information from the inductor current feedback, $\hat{V}_i$, are summed together, resulting in the control voltage, $\hat{V}_c$. This control voltage, $\hat{V}_c$, is used to control the duty cycle of the switch. The F_M block contains the small-signal model of the duty cycle modulator and is defined as $\hat{d}/\hat{V}_c$. In this chapter, F_M is treated as a constant and the F_M model for the magnetic amplifier modulator gain is considered in the following chapter.

The equivalent small-signal block diagram of the buck converter is shown in Figure 4.2. The small-signal blocks F_M, H_v, and H_i denote transfer functions which describe the control aspects of the system. The remaining transfer functions describe the power stage of the system and are denoted by the by the small-signal blocks: G_{vd}, G_{id}, G_{vg}, G_{ig}, Z_p, and G_{ii}. These open-loop transfer functions describe the converter itself and do not change as a function of control. G_{vd} and G_{id} represent the control-to-output voltage and control-to-inductor current transfer functions respectively. G_{vg} and G_{ig} represent the input voltage-to-output voltage and the input voltage-to-inductor current transfer functions respectively. Z_p represents the open-loop output impedance which

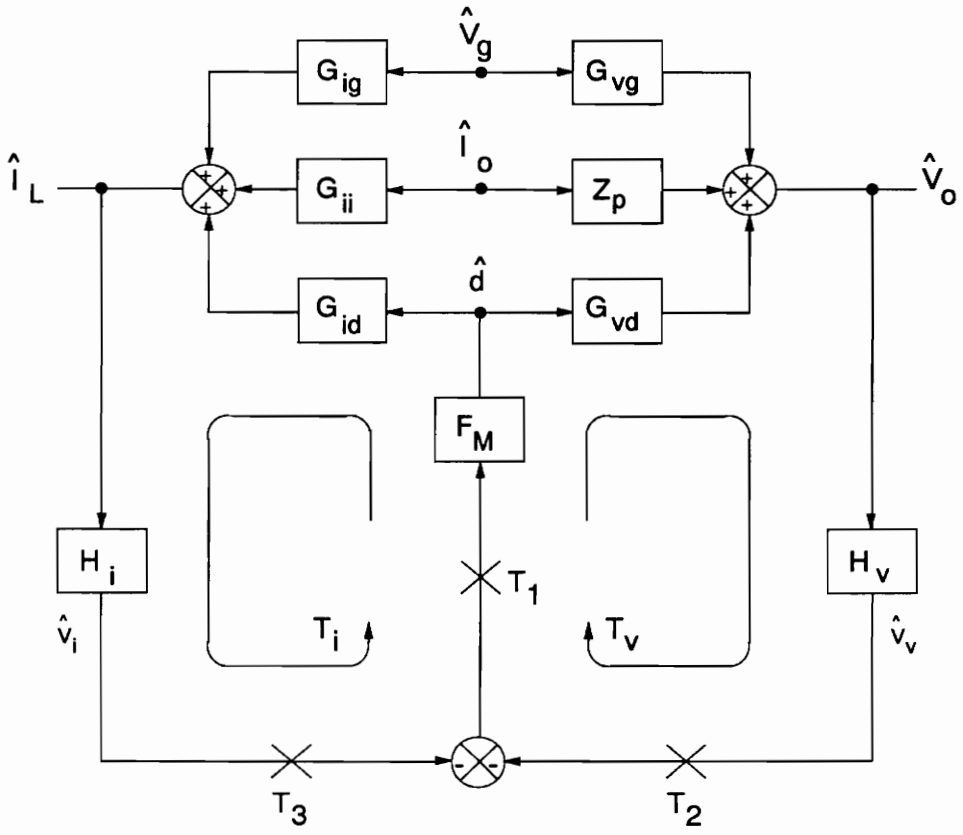


Figure 4.2. Small-Signal Block Diagram of a Current-Mode Control Converter

is output current-to-output voltage and G_{ii} represents the output current-to-inductor current transfer function.

The power stage transfer functions for the buck converter are given in Table 4.1. These transfer functions are well known and can be derived using state-space analysis. [8]

4.2 Dynamic Performance

The control system of power supplies is designed to meet specifications of closed-loop dynamic performance. Some parameters which define dynamic performance in a power supply are: audio susceptibility or input-to-output noise transmission, settling time and peak overshoot of the dynamic response to a step-load change (which may be translated as an output impedance measurement for small load changes), and stability.

4.2.1 Significance of Loop Gains

Single-Loop Control

In a single-loop voltage-mode control system, performance is directly related

Table 4.1. Small-Signal Transfer Functions of a Buck Converter

G_{vg}	$\frac{\hat{V}_o}{\hat{V}_g} = \frac{D(1+sR_cC)}{\Delta}$
G_{ig}	$\frac{\hat{I}_L}{\hat{V}_g} = \frac{D(1+sR_LC)}{R_L\Delta}$
G_{vd}	$\frac{\hat{V}_o}{\hat{d}} = \frac{V_g(1+sR_cC)}{\Delta}$
G_{id}	$\frac{\hat{I}_L}{\hat{d}} = \frac{V_g(1+sR_LC)}{R_L\Delta}$
Z_p	$\frac{\hat{V}_o}{\hat{I}_o} = \frac{R_l(1+sR_cC)\left(1+s\frac{L}{Rl}\right)}{\Delta}$
G_{ii}	$\frac{\hat{I}_L}{\hat{I}_o} = \frac{R_l(1+sR_LC)\left(1+s\frac{L}{Rl}\right)}{R_L\Delta} - 1$
Δ	$1 + s\left((R_l+R_c)C + \frac{L}{R_L}\right) + s^2LC$

T_i	$F_M G_{id} H_i$
T_v	$F_M G_{vd} H_v$
T_1	$T_i + T_v$
T_2	$\frac{T_v}{1+T_i}$
Z_o	$\frac{\hat{V}_o}{\hat{I}_o} = \frac{Z_p + T_i\left(Z_p - \frac{G_{vd}G_{ii}}{G_{id}}\right)}{1+T_i+T_v}$
A_s	$\frac{\hat{V}_o}{\hat{V}_g} = \frac{G_{vg}}{1+T_i+T_v}$

to the loop gain T which is well defined. For example, the closed loop audio susceptibility, A_s, in a voltage-mode control system is the ratio of the open-loop audio susceptibility, G_{vg}, (the output voltage-to-input voltage transfer function) to the loop gain T:

$$A_s = \frac{\hat{V}_o}{\hat{V}_g} = \frac{G_{vg}}{1 + T}$$

The same is true for the output impedance; the closed-loop output impedance, Z_o, is the ratio of the open-loop output impedance, Z_p to the loop gain T:

$$Z_o = \frac{\hat{V}_o}{\hat{I}_o} = \frac{Z_p}{1 + T}$$

Thus, the loop gain directly attenuates the audio susceptibility and output impedance in a voltage-mode control system. Stability is also directly determined by the voltage-mode control loop gain. The loop gain's bandwidth, phase margin, and gain margin are all direct measures of stability. The bandwidth of a voltage-mode control system is the frequency where the magnitude of the loop gain crosses zero dB, determining the frequency range in which the feedback gain is effective in attenuating the closed-loop characteristics. Phase margin is the distance between -180° and the loop gain phase at the frequency of loop gain zero crossover. Gain margin is the amount of dB that the system gain can be varied before it reaches instability when the phase is -180° and the gain is 0 dB.

Current-Mode Control

Current-mode control describes a multi-loop control system where both the output voltage and inductor current are used as feedback to achieve regulation. In a multi-loop, current-mode control system, the relationship between loop gain and dynamic performance is not as straightforward as in voltage-mode control. Because the additional inductor current feedback loop is included, there are now three places to break the loop instead of just one (Figure 4.2). These three different loop gains, T1, T2, and T3, produce three different bandwidths, phase margins, and gain margins. Thus, the closed-loop performance of the system cannot be determined directly from one particular loop gain but is found using a combination of two of the loop gains, the outer loop gain, T2, and the system loop gain, T1. [9] The following sections discuss the relationships between these loop gains and the closed-loop performance. Before discussion of closed-loop performance, however, two feedback loop gains T_i and T_v are introduced and explained in the following subsection.

Feedback Loops T_i and T_v

The feedback loops T_v and T_i are shown on the block diagram in Figure 4.2. The loop gain T_v denotes the feedback path of the output voltage loop and is the product of the small-signal blocks, $F_M G_{vd} H_v$. F_M is given by the modulator gain, G_{vd} is given by the converter power stage, and H_v is the control compen-

sation circuit transfer function which is designed. The loop gain for the voltage loop is the same loop gain used in voltage-mode control. The additional loop of current-mode control, T_i, denotes the feedback path of the inductor current loop and is the product of the small-signal blocks, $F_M G_{id} H_i$. Where F_M is the modulator gain, G_{id}, is given by the converter power stage and H_i is the designed control compensation circuit.

Relationship Between T1, T2 and T_i, T_v

T_i and T_v are introduced to provide a direct design link between T1, T2 and the compensation scheme. T1 and T2 are used to predict the performance. However, since it is easier to design the current loop, T_i, independently from the voltage loop, T_v, it is practical to define T1 and T2 as functions of T_i and T_v. Then the current loop, T_i, and the voltage loop, T_v, can be directly designed to meet T1 and T2's requirements for providing good loop gain performance and system stability.

The two loop gains used to predict performance can be measured at points T1 and T2 on the block diagram. T1 is called the system loop gain and T2 is called the outer loop gain. The system loop gain, T1, is derived from the small-signal block diagram (see Appendix) and is found to be the sum of the current loop, T_i, plus the voltage loop, T_v:

$$T1 = T_i + T_v$$

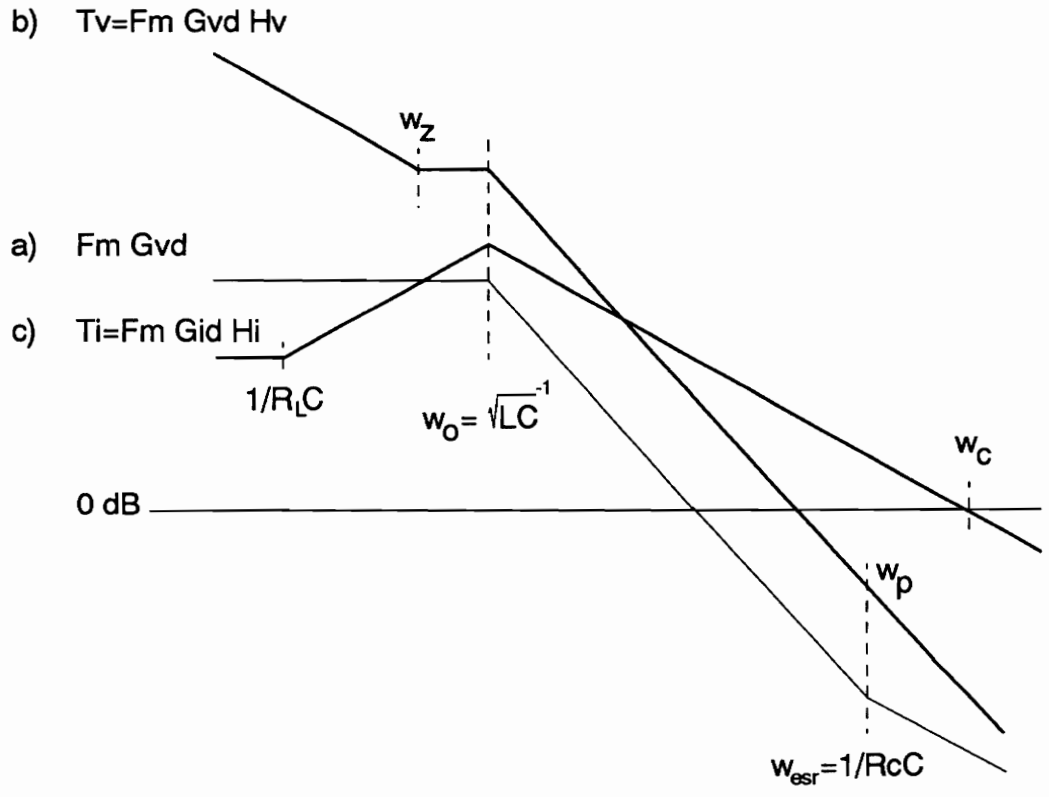


Figure 4.3. Asymptotic Bode Plots of gains: a) $F_M G_{vd}$, b) $T_v = F_M G_{vd} H_v$ and c) $T_i = F_M G_{id} H_i$.

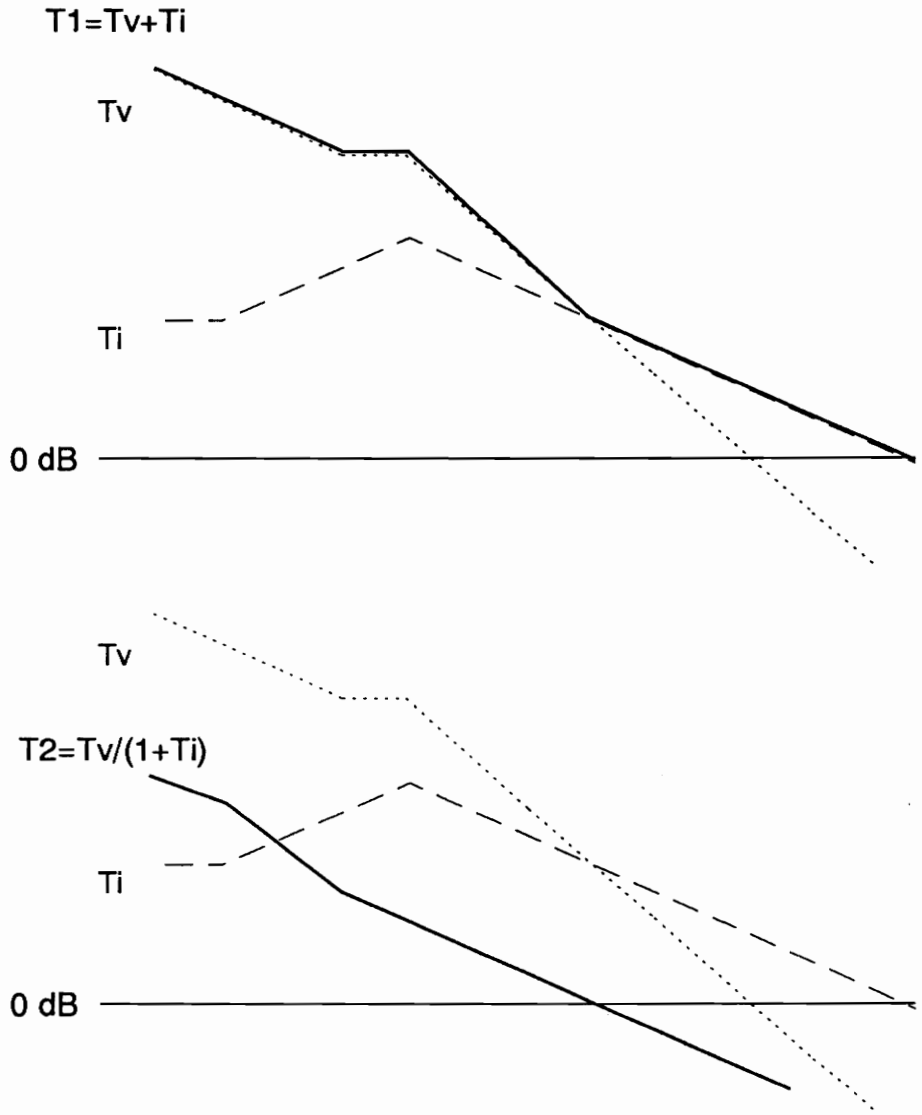


Figure 4.4. Relationship between T1,T2 and T_i, T_v

the outer loop gain, T2, is found to be:

$$T2 = \frac{T_v}{1 + T_i}$$

Thus, the two loop gains, T1 and T2, are expressed as functions of the feedback loops, T_i and T_v. Figure 4.3 gives asymptotic Bode plots of T_i and T_v and Figure 4.4 shows the relationship between T1, T2 and T_i and T_v.

Sections 4.2.2, 4.2.3, and 4.2.4 discuss how the loop gains, T1 and T2, affect performance and stability and Section 4.3 discusses how the feedback loops, T_i and T_v, are designed to achieve optimum T1 and T2 loop gains.

4.2.2 *Effect of Loop Gains on Audio Susceptibility*

The open-loop input-to-output noise transmission or audio susceptibility is given by the G_{vg} transfer function in Table 4.1. The closed-loop audio susceptibility is derived from the small-signal block diagram to be:

$$A_s = \frac{\hat{V}_o}{\hat{V}_g} = \frac{G_{vg}}{1 + T1}$$

for the buck converter. These derivations are provided in the Appendix. Thus, the system loop gain, T1 directly determines the attenuation of the closed-loop audio susceptibility in a buck converter. Also, since the bandwidth of T_i is larger than that of T_v and $T1 = T_i + T_v$, a high bandwidth of T_i implies good

closed-loop audio susceptibility performance and the peak value is independent of the bandwidth of T_v.

4.2.3 Effect of Loop Gains on Output Impedance

The open-loop output impedance is given by the transfer function Z_p in Table 4.1. Using the small-signal block diagram, the closed-loop expression of output impedance for buck converter's is:

$$Z_o = \frac{\hat{V}_o}{\hat{i}_o} \simeq \frac{Z_p}{1 + T1} + \frac{\frac{R_L}{1 + sR_LC}}{1 + T2}$$

at frequencies below the crossover of the current loop, T_i. The derivations are given in the Appendix. It can be seen from this expression that both T1 and T2 contribute to the closed-loop output impedance and neither gives direct information about the relationship between open-loop and closed-loop behavior. [9]

4.2.4 Stability

The system loop gain, T1, is the sum of the voltage loop, T_v, and the current loop, T_i. At low frequencies, the voltage loop gain, T_v is high, providing tight dc regulation. At high frequencies, due to its larger bandwidth, the current loop gain, T_i, dominates, taking advantage of its lower phase lag. The system loop gain, T1, gives direct information about closed-loop audio susceptibility attenuation in a buck converter and gives indirect information about the closed-loop output impedance. However, the gain margin and phase margin of the system loop gain, T1, are not a direct indications of the stability of the overall system, since both the voltage loop and the current loop would have to decrease in magnitude for the system to become unstable. The outer loop gain, T2, gives more valid information about overall system stability. The outer loop gain, T2, is the ratio of the voltage loop, T_v, to the current loop, T_i, below the current loop crossover and is the voltage loop gain, T_v, above the current loop crossover. Thus, T2's gain and phase margin predict relative stability and determine how much the voltage loop can be varied before the system becomes unstable.

Figure 4.5 shows three different sets of possible T_i, T_v combinations. Figure 4.5(a) is an unstable system, Figure 4.5(b) is stable but has a small bandwidth and dc gain, and Figure 4.5(c) is stable with large bandwidth and gain. This shows the significance of placing T_i's crossover frequency as high

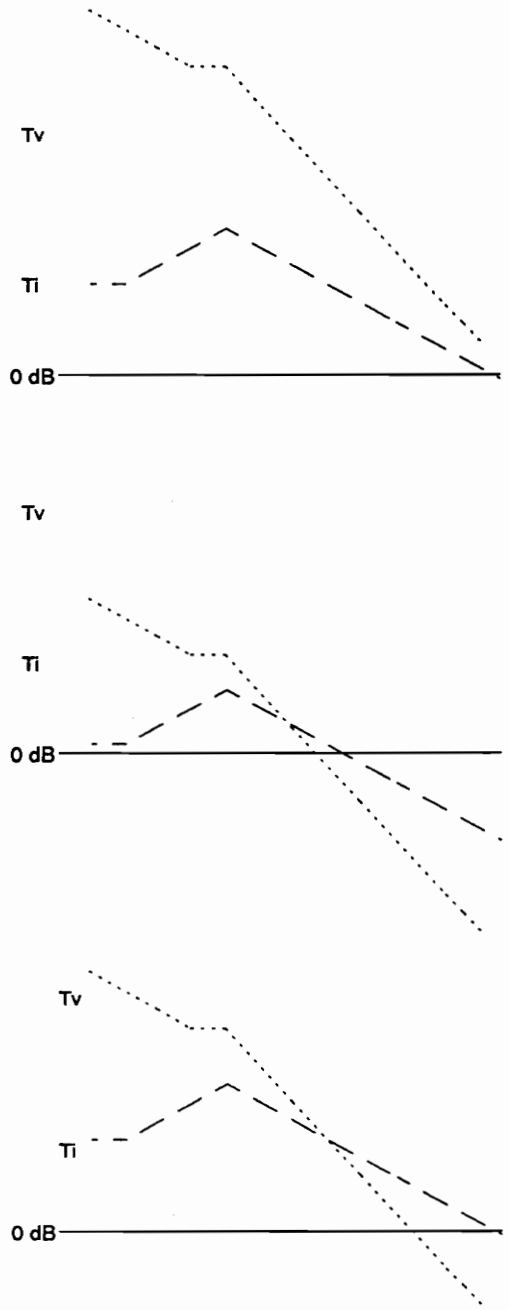


Figure 4.5. (a) Unstable, (b) Stable but small bandwidth and dc gain, and (c) Stable with large bandwidth and dc gain

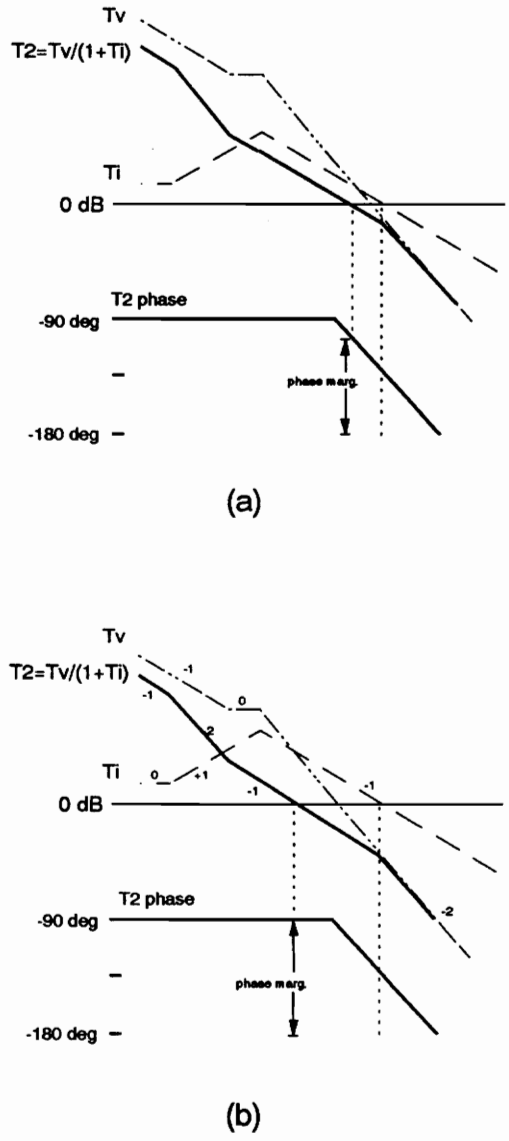


Figure 4.6. Effect of T_v magnitude: (a) small phase margin (less stable) (b) large phase margin (more stable).: Asymptotic phase plots drawn assuming second pole and first zero are close enough together to cancel their effect.

as possible. Once T_i's crossover is set, the gain of T_v can be increased or decreased which varies the phase and gain margin of T2. Figure 4.6 illustrates this.

4.3 Feedback Compensation Design Guidelines

The dynamic performance of the current-mode controlled buck converter cannot be directly determined by either of the loop gains, T1 or T2, independently; both are used to predict behavior. Since T1 and T2 are composed of the current loop, T_i, and the voltage loop, T_v, the effect of T1 and T2 on performance governs the design of T_i and T_v. It has been shown that T_i needs a high bandwidth, T_v needs a high dc gain, and the frequency at where these two feedback gains cross has an effect on stability. The following sections describe the design of T_i and T_v to meet these qualifications.

The voltage loop gain, T_v, is the product of the modulator gain transfer function, F_M, the control-to-output voltage transfer function, G_{vd}, and the voltage feedback controller, H_v. Since F_M is a constant and G_{vd} is given by the converter power stage design, the design of the voltage feedback controller, H_v, alters the loop gain of the voltage loop, $T_v = F_M G_{vd} H_v$. H_v typically has a zero and two poles:

$$H_v = \frac{\omega_I(1 + s/\omega_z)}{s(1 + s/\omega_p)}$$

The first pole is placed at the origin to assure tight DC regulation and the other pole cancels the ESR zero of G_{vd} to continue the voltage loop's -40 dB/dec slope after G_{vd}'s resonant frequency, thus attenuating switching noise. The zero is placed before the resonant frequency to prevent conditional stability in the system loop gain. Placing this zero higher in frequency improves the settling time of the dynamic response to a step-load change. Figure 4.3 shows asymptotic overplots of $F_M G_{vd}$ and $F_M G_{vd} H_v$. Because there is a double pole at the resonant frequency, the phase of T_v at crossover approaches -180°.

The current loop gain, T_i, is the product of F_M G_{id} H_i. F_M is a constant and G_{id} is a function of the converter power stage. H_i is a function of the current sense circuit and usually consists of a DC gain. Thus, the shape of the current loop gain, T_i, is determined by G_{id} and is shown in Figure 4.3. Because the control-to-inductor current transfer function, G_{id}, has a zero ($\omega_z = 1/R_L C$) before the resonant frequency, the slope after the resonant frequency becomes -20 dB/dec and the phase at crossover approaches only -90°. Since the system loop gain is the sum of the voltage loop and the current loop, placing the crossover of T_i as high as possible within the constraints of the circuit (and higher than that of T_v) takes advantage of this more stable phase and provides the benefits of current-mode control.

4.4 Summary

Current-mode control describes a two-loop control system in which both the inductor current and output voltage are fed back to achieve regulation. In a multi-loop control system, there is more than one place to measure the loop gain and no one particular loop can predict performance independently. Two of the loop gains in current-mode control are used to determine the closed-loop performance and stability.

The two loop gains, T1 and T2, both give information about the performance of the converter. T1 directly predicts the closed-loop audio susceptibility but does not give direct information about the closed-loop output impedance or stability of the system. T2 gives information about the stability of the system, but cannot be used to directly determine the closed-loop audio susceptibility or output impedance behavior.

T1 and T2 are composed of the current loop and the voltage loop gains, T_i and T_v. T1 is the sum of the two loops and T2 is the ratio of the voltage loop to the current loop at frequencies below the T_i crossover and the voltage loop at frequencies above the T_i crossover. Therefore, the performance of the converter can be determined by the design of these two loops.

The general design procedure is: (1) the crossover of T_i should be placed as high as possible within the constraints of the feedback circuit and (2) the

magnitude of T_v should be placed as high as possible within an acceptable phase margin.

V. Current-Mode Control of Magnetic Amplifier Post Regulator

This chapter presents a model of the current-mode control loop behavior of a magnetic amplifier post regulator circuit. The analysis summarized in Chapter IV is applicable to the magnetic amplifier post regulator and is used in this chapter. Section 5.1 describes current-mode control of the magnetic amplifier post regulator. The resulting small-signal model for the magnetic amplifier is presented in section 5.2. Based on this model, a detailed design procedure of the control circuit is illustrated with a numerical example in section 5.4. Experimental verification of the model is presented in section 5.6.

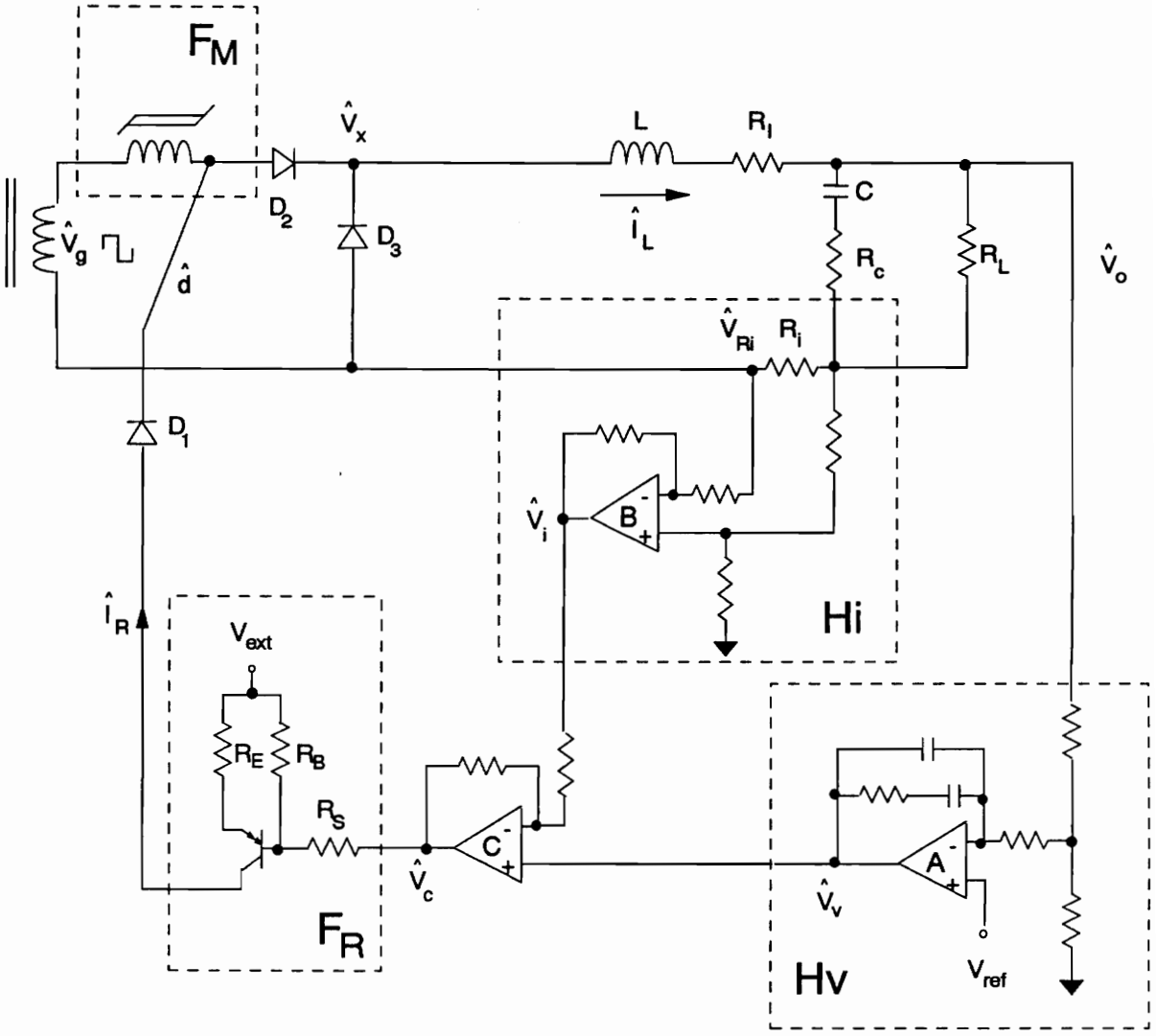


Figure 5.1. Current-Mode Controlled Magnetic Amplifier Post Regulator with External Reset

5.1 Description of Current-Mode Control of Magnetic Amplifier

Figure 5.1 shows a current-mode controlled magnetic amplifier post regulator. The control block H_v describes the feedback of small-signal variations in output voltage. As discussed in Chapter IV, H_v contains a zero and two poles which are implemented using the operational amplifier A configuration shown.

The control block H_i describes the feedback of small-signal variations in inductor current. In Figure 5.1, the inductor current information is taken by feeding back the voltage across the resistor R_i in the inductor current path. There are other methods of acquiring the inductor current information, some of which are discussed in Reference [9].

Operational amplifier C directly sums the current loop and the voltage loop together, resulting in a control voltage, $\hat{V}_c$. The control voltage, $\hat{V}_c$, is then converted to a control current, I_R, in the block F_R. The control current, I_R, is fed into the magnetic amplifier, determining the duty cycle as described by the small-signal transfer function, F_M, which has been discussed in detail in Chapters II and III.

The layout in Figure 5.1 was chosen for ease of measuring and demonstrating the various loops; it is possible to reduce the number of operational amplifiers and achieve the same results with less parts.

5.2 Small-Signal Analysis

Figure 5.2 shows the small-signal model of the magnetic amplifier post regulator circuit shown in Figure 5.1.

Breaking the loop at point T1 results in a system loop gain which is the sum of the inductor current loop gain, T_i, and the output voltage loop gain, T_v. The outer loop gain, T2, is $T_v/(1 + T_i)$. The transfer functions for closed-loop output impedance and audio susceptibility are as follows:

$$Z_o = \frac{\hat{V}_o}{\hat{I}_o} \simeq \frac{Z_p}{1 + T1} + \frac{\dfrac{R_L}{1 + sR_LC}}{1 + T2}$$

$$A_s = \frac{\hat{V}_o}{\hat{V}_g} = \frac{G_{vg}}{1 + T1}$$

The derivations for these transfer functions are given in the Appendix.

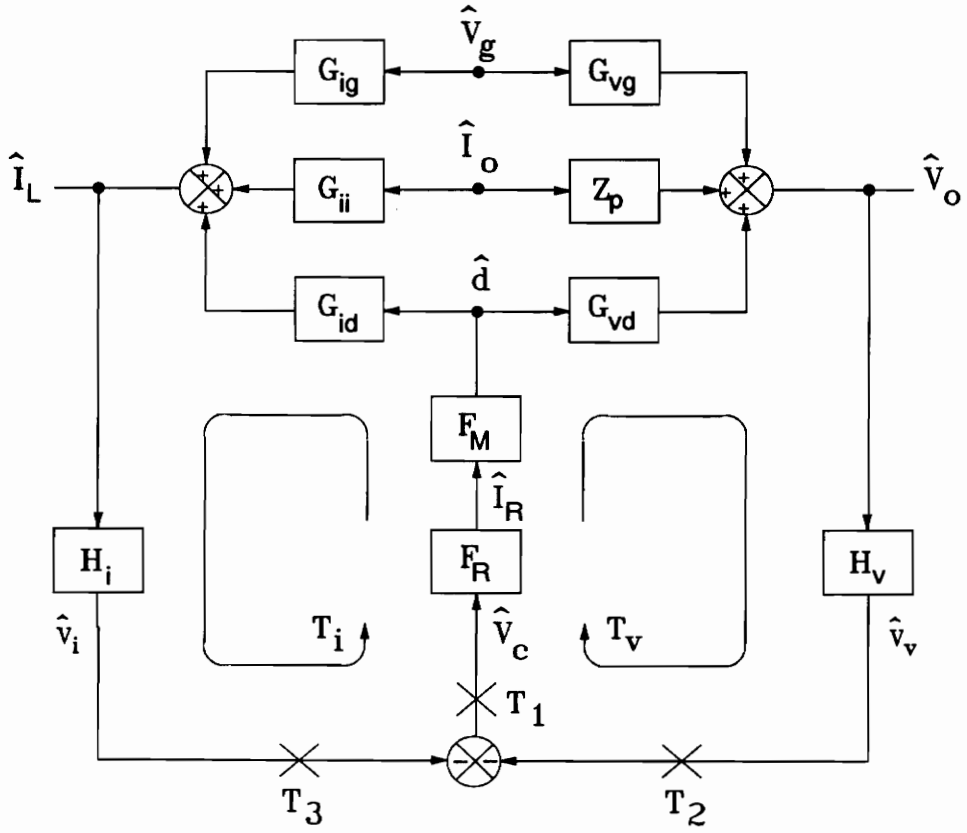


Figure 5.2. Small-Signal Block Diagram for Two-Loop Control with External Reset

Table 5.1. Open-Loop Power Stage Transfer Functions for Magnetic Amplifier Post Regulator

F_M	$\frac{\hat{d}}{\hat{I}_R} = \frac{0.4\pi\mu_m N^2 A_c f_s}{l_e V_g 10^8}$
F_R	$\frac{\hat{I}_R}{\hat{V}_c} = -\frac{R_B}{(R_S + R_B)R_E}$
G_{vg}	$\frac{\hat{V}_o}{\hat{V}_g} = \frac{D(1 + sR_cC)}{\Delta}$
G_{ig}	$\frac{\hat{I}_L}{\hat{V}_g} = \frac{D(1 + sR_LC)}{R_L\Delta}$
G_{vd}	$\frac{\hat{V}_o}{\hat{d}} = \frac{V_g(1 + sR_cC)}{\Delta}$
G_{id}	$\frac{\hat{I}_L}{\hat{d}} = \frac{V_g(1 + sR_LC)}{R_L\Delta}$
Z_p	$\frac{\hat{V}_o}{\hat{I}_o} = \frac{R_l(1 + sR_cC)\left(1 + s\frac{L}{Rl}\right)}{\Delta}$
G_{ii}	$\frac{\hat{I}_L}{\hat{I}_o} = \frac{R_l(1 + sR_LC)\left(1 + s\frac{L}{Rl}\right)}{R_L\Delta} - 1$
Δ	$1 + s\left((R_l + R_c)C + \frac{L}{R_L}\right) + s^2LC$

5.3 Loop Gains and Closed-Loop Performance

The magnetic amplifier small-signal block diagram shown in Figure 5.2 is very similar to the conventional multi-loop model shown in Figure 4.2. Therefore, the closed loop performance analysis presented in Chapter IV is applicable to the magnetic amplifier control loop behavior. The closed loop transfer functions for the external reset control method are shown in Table 5.2. With the exception of the F_M and F_R blocks which are derived for the magnetic switch in Chapter III, the transfer functions are the same as the conventional PWM switch-mode Buck converter and are well known.

Table 5.2. Closed-Loop Transfer Functions for Magnetic Amplifier Post Regulator with External Reset

T_i	$F_M F_R G_{id} H_i$
T_v	$F_M F_R G_{vd} H_v$
T_1	$T_i + T_v$
T_2	$\dfrac{T_v}{1+T_i}$
Z_o	$\dfrac{\hat{V}_o}{\hat{I}_o} = \dfrac{Z_p + T_i\left(Z_p - \frac{G_{vd}G_{ii}}{G_{id}}\right)}{1+T_1}$
A_s	$\dfrac{\hat{V}_o}{\hat{V}_g} = \dfrac{G_{vg}}{1+T_1}$

5.4 Design Guidelines

The design guidelines given in Chapter IV are equally applicable with the magnetic amplifier post regulator. The design goal is to raise the gain of T_i as much as practical, then design the error amplifier gain, H_v to ensure a large bandwidth and a stable system.

5.5 Control Design Example

In this example, the power circuit and the reset circuit parameters are given. This section outlines the procedure for designing the control compensation circuits shown in blocks H_i and H_v of Figure 5.3.

Power Stage and Reset Circuit Parameters

The power stage and the reset circuit parameters are given as follows and will remain the same throughout this thesis to allow for comparisons between the various control conditions:

$f_s = 50kHz$ $V_g = 58V$ $V_o = 12V$ $R_L = 2.4\Omega$

$L = 58\mu H$ $R_l = 232m\Omega$ $C = 314\mu F$ $R_c = 50.9m\Omega$

$R_B = 1k\Omega$ $R_S = 1k\Omega$ $R_E = 47\Omega$

D_{pri} = main converter duty cycle = 0.274

V_D = diode voltage drop = $1V$

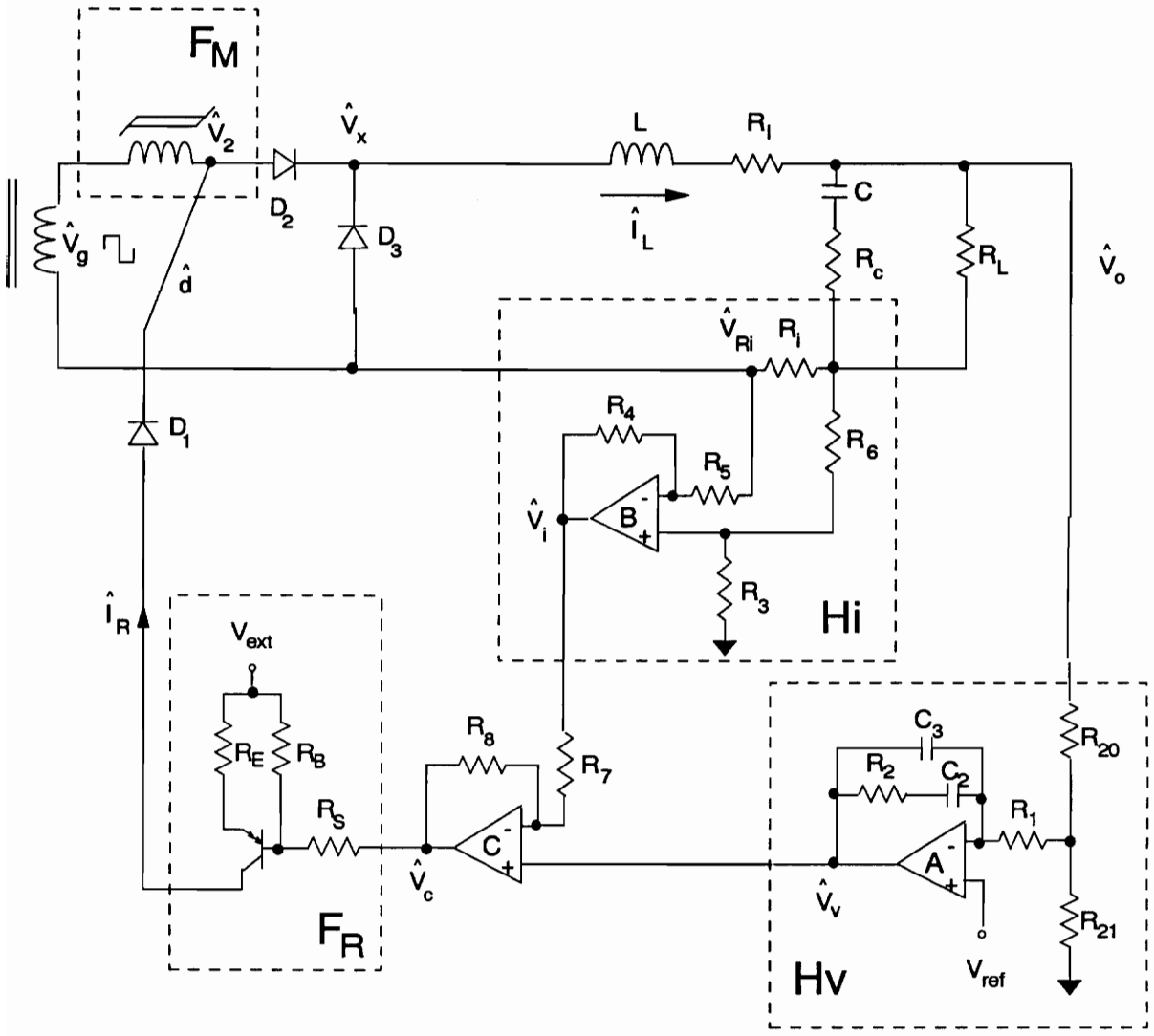


Figure 5.3. Current-Mode Controlled Magnetic Amplifier Post Regulator with External Reset

Magnetic Amplifier Parameters

Magnetics Inc. 50B10-1E METGLAS Alloy 2714A

$N = 36 \qquad A_e = 0.076cm^2 \qquad l_e = 6.18cm$

Step 1: Calculate F_R using Table 5.1

$$F_R = \frac{R_B}{(R_S + R_B)R_E} = \frac{1k}{(1k + 1k)47} = .01064 \tag{5.1}$$

Step 2: Calculate F_M using Table 5.1

a) Calculate ΔB

$$\Delta B = \frac{(D_{pri}V_g - V_o - V_D)10^8}{f_s N A_e} = \frac{[(0.274)(58) - 12 - 1]10^8}{(50k)(36)(0.076)} = 2114 \tag{5.2}$$

b) Find magnetic amplifier core loss P_L

At $\Delta B/2 = 1057$ and $50kHz$, $P_L = 6.34$ Watts/lb (from core catalog)

c) Calculate μ_M

$$\mu_M = \frac{\Delta B^2 f_s}{K_c P_L 10^6} = \frac{(2114)^2(50k)}{(1.08)(6.34)(10)^6} = 32634 \tag{5.3}$$

Where $K_c = 1.08$ for 2714A METGLAS, $K_c = 1.2$ for square 80 permalloy

d) Calculate F_M

$$F_M = \frac{0.4\pi\mu_M N^2 f_s A_e}{l_e V_g 10^8} = \frac{(0.4)(\pi)(32634)(36)^2(50k)(0.076)}{(6.18)(58)(10)^8} = 5.63 \qquad (5.4)$$

e) $F_M F_R = 0.06$

Step 3: Design Current Loop

a) Calculate T_i using Table 5.2

T_i is the current loop gain given by the following formula:

$$T_i = F_M F_R H_i G_{id} = \frac{F_M F_R H_i V_g (1 + sR_L C)}{R_L(1 + s((R_l + R_c)C + \frac{L}{R_L}) + s^2 LC)}$$

$$T_i = \frac{1.45H_i(1 + \frac{s}{1327})}{(1 + \frac{s}{8850} + \frac{s^2}{7410^2})} \qquad (5.5)$$

b) Find H_i to give the desired crossover frequency of T_i

The contribution from H_i is the amplification of the current loop and it is a constant. As described in Chapter IV, T_i 's crossover frequency needs to be placed higher than T_v 's. Because T_i has a zero before the resonant frequency, the double pole from the resonant frequency has a slope of -1 instead of -2 after the resonant frequency. Thus, if T_i 's crossover frequency is placed

higher than T_v 's, the -1 slope is taken advantage of and the system loop gain, $T1 = T_i + T_v$ will have a phase delay of 90° (instead of 180° from T_v) at crossover and the system will be stable. Also, to make the system bandwidth wide, T_i 's crossover should be placed as high as possible within the constraints of the op amps and half the switching frequency. Choosing a crossover frequency of $f_c \simeq 6kHz$, the magnitude of equation (5.5) is calculated to be:

$$|T_i|_{w_c = 35000} \simeq 1.46H_i$$

Since $|T_i| = 1$ at crossover, setting $H_i = |T_i|/1.46 = 1/1.46 \simeq 0.685$ will place the crossover frequency at 6 kHz and the resulting T_i transfer function is:

$$T_i = \frac{0.993(1 + \frac{s}{1327})}{(1 + \frac{s}{8850} + \frac{s^2}{7410^2})}$$

Step 4: Design Voltage Loop

a) Calculate T_v using Table 5.2

T_v is the voltage loop gain given by the following formula:

$$T_v = F_M F_R H_v G_{vd} = \frac{F_M F_R H_v V_g (1 + sR_c C)}{(1 + s((R_l + R_c)C + \frac{L}{R_L}) + s^2 LC)}$$

$$T_v = \frac{3.48H_v(1 + \frac{s}{62566})}{(1 + \frac{s}{8850} + \frac{s^2}{7410^2})} \tag{5.6}$$

b) Design H_v

$$H_v = \frac{\omega_I(1 + \frac{s}{\omega_z})}{s(1 + \frac{s}{\omega_p})}$$

ω_p is placed close to the esr zero, $1/R_cC$ to cancel it and to provide attenuation at the switching frequency. ω_z is placed before the resonant frequency so that the phase delay after the resonant frequency is 180° rather than 270°. ω_z also determines the settling time of the system. Choosing $\omega_p = 62566$ and $\omega_z = 4000$, equation (5.6) becomes:

$$T_v = F_M F_R G_{id} H_v$$

$$T_v = \frac{(3.48(1 + \frac{s}{62566}))}{1 + \frac{s}{8850} + \frac{s^2}{7410^2}} \frac{\omega_I(1 + \frac{s}{4000})}{s(1 + \frac{s}{62566})}$$

$$T_v = \frac{3.48\omega_I(1 + \frac{s}{4000})}{s(1 + \frac{s}{8850} + \frac{s^2}{7410^2})} \tag{5.7}$$

The voltage loop and the current loop should cross each other between the resonant frequency, ω_o and T_i 's crossover frequency, w_c so that T_i determines the system crossover frequency. The closer this crossing frequency, ω_x, is to w_c, the less phase margin there is. Choosing a ω_x of 20000, to determine ω_l, the magnitudes of T_i and T_v are arbitrarily set equal at $f_x \simeq 3.3kHz$:

$$|T_i|_{\omega_x = 20000} = 1.51 = |T_v|_{\omega_x = 20000} = .0001\omega_l$$

$$\text{Thus,} \quad \omega_l = 15100$$

And equation (5.7) becomes:

$$T_v = \frac{52548(1 + \frac{s}{4000})}{s(1 + \frac{s}{8850} + \frac{s^2}{7410^2})}$$

Step 5: Implementing H_i and H_v

a) Deriving the transfer functions of the circuit in Figure 5.3 results in the following:

From error amplifier A of Figure 5.3:

$$H_v = \frac{\hat{V}_v}{\hat{V}_o} = \frac{-\omega_l(1 + \frac{s}{\omega_z})}{s(1 + \frac{s}{\omega_p})} = -\frac{15100(1 + \frac{s}{4000})}{s(1 + 62566)}$$

$$\text{where } \omega_z = \frac{1}{R_2 C_2} \simeq 4000,$$

$$\omega_p = \frac{C_2 + C_3}{C_2 C_3 R_2} \simeq 62566,$$

$$\omega_l = \frac{R_{21}}{[R_1(R_{20} + R_{21}) + R_{20}R_{21}](C_2 + C_3)} \simeq 15100$$

$$H_i = \frac{\hat{V}_i}{\hat{I}_{R_i}} = \frac{R_4}{R_5} R_i \quad \text{where } R_3 = R_4, R_5 = R_6$$

However from summing amplifier C in Figure 5.3,

$$V_c = (1 + \frac{R_8}{R_7}) V_v - \frac{R_8}{R_7} V_i$$

$$\text{Thus, } H_v = -(1 + \frac{R_8}{R_7}) \omega_l \frac{(1 + \frac{s}{\omega_z})}{s(1 + \frac{s}{\omega_p})} \quad \text{and} \quad H_i = -\frac{R_8 R_4}{R_7 R_5} R_i$$

$$\text{Setting } R_7 = 5k\Omega,\ R_8 = 12k\Omega,\ R_{21} = 2k\Omega,\ R_{20} = 7.5k\Omega,\ R_i = 65m\Omega$$

$$\text{To attain } H_i \simeq 0.685 \quad \text{and} \quad H_v \simeq \frac{15100(1 + s/4000)}{s(1 + s/62566)},$$

The following values of components can be used:

$$R_1 = 100k\Omega pot \qquad C_2 = 3900pF$$

$$R_2 = 61k\Omega \qquad C_3 = 270pF$$

$$R_3 = R_4 = 13k\Omega$$

$$R_5 = R_6 = 2.9k\Omega$$

The value of R_1 is adjusted until the desired phase margin is achieved. Adjusting R_1 changes the value of ω_l which raises the T_v gain plot up and down, thereby adjusting the phase margin. As R_1 increases, the magnitude of T_v decreases, and the T2 phase margin is increased and the system is more stable.

5.6 *Experimental Verification*

The external reset circuit designed in the previous section is shown in Figure 5.4. This circuit was built and tested. Figure 5.5a shows the input voltage, V_g, the voltage at V_2, the difference between V_g and V_2 which is the voltage across the saturable reactor, and the rectified voltage, V_x. It can be seen from the saturable reactor voltage, $V_g - V_2$ that the reset volt-seconds is equal to the blocking volt-seconds (the spike is due to reverse recovery of diode D1). The amount of reset volt-seconds is determined by the reset control

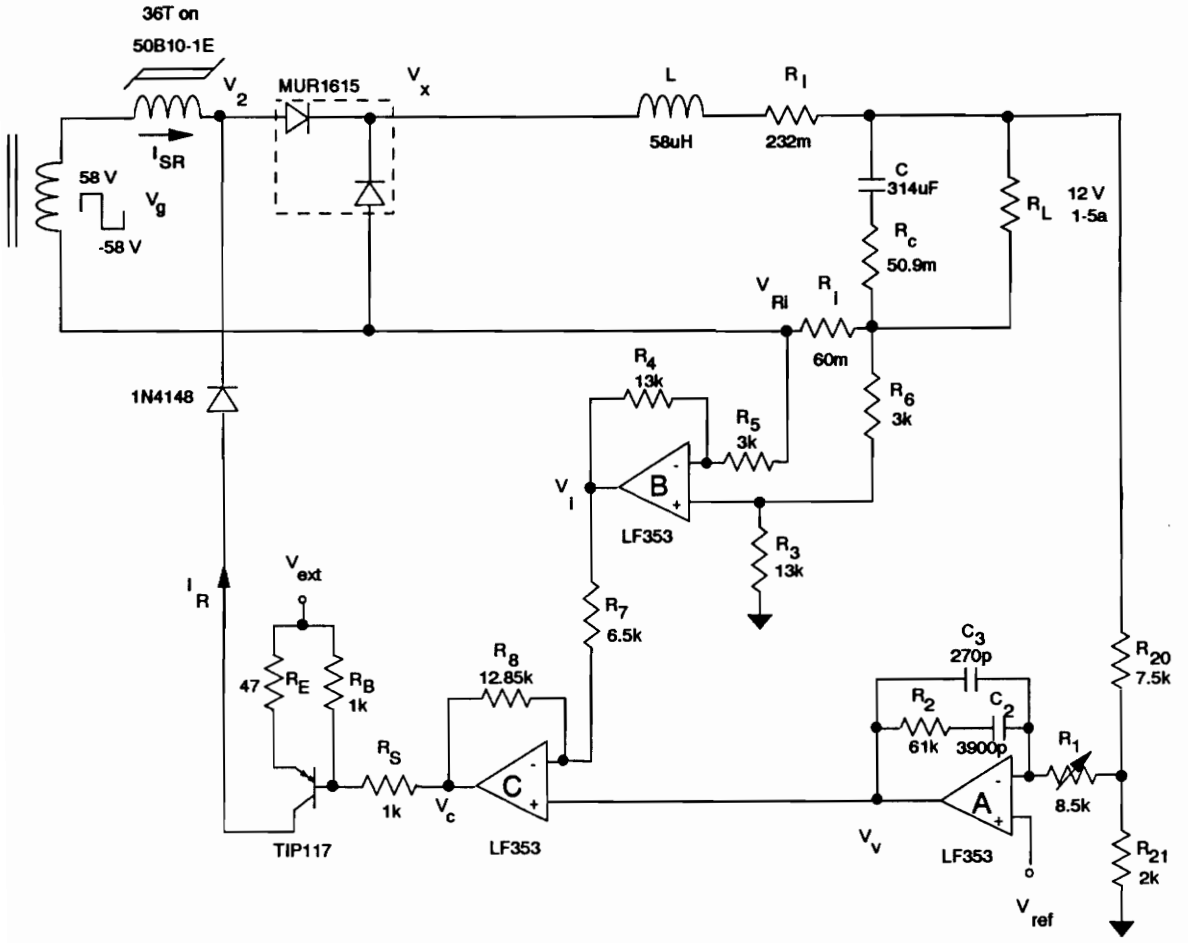


Figure 5.4. Complete Schematic of Current-Mode Control Magnetic Amplifier Post Regulator with External Reset

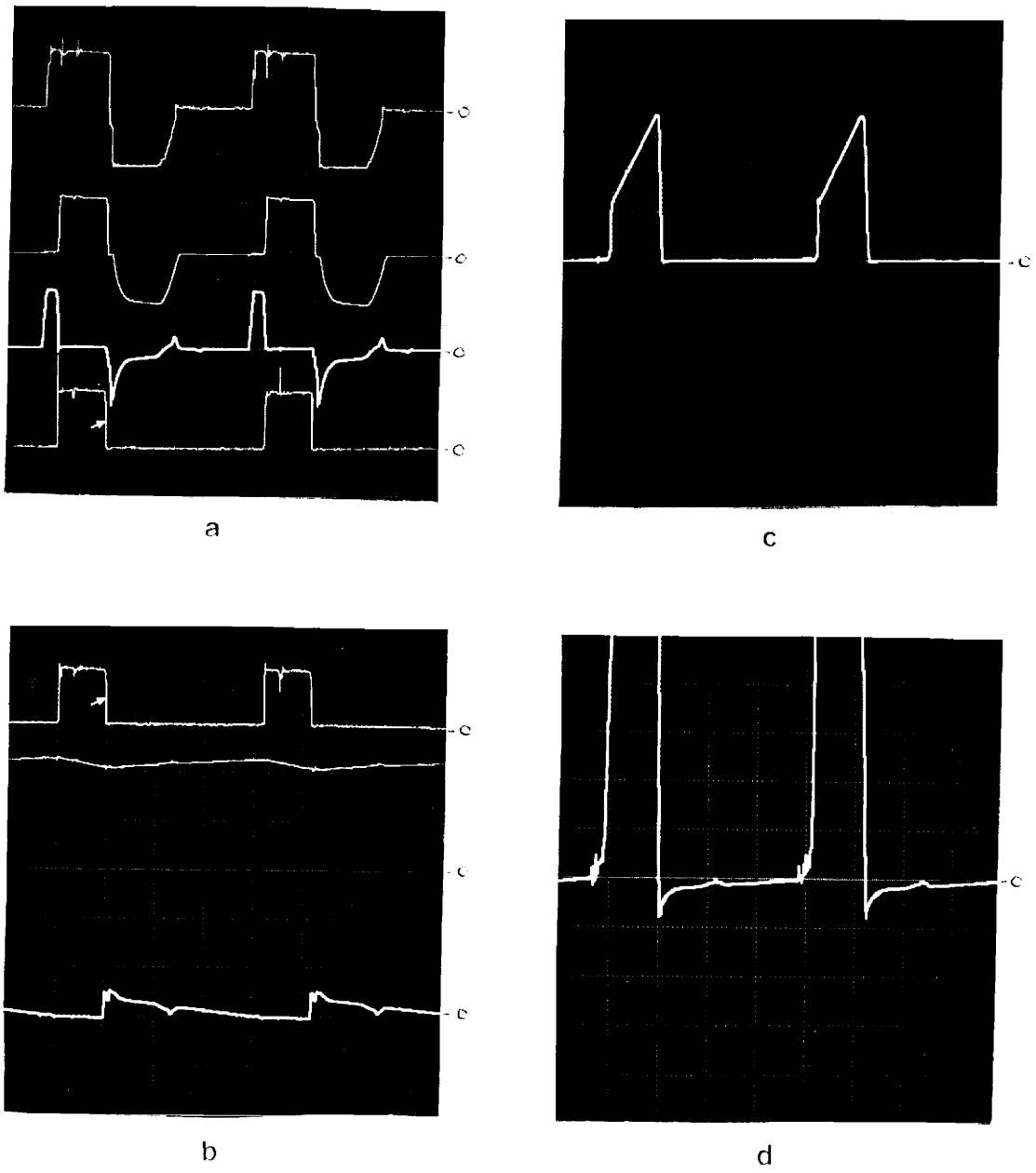


Figure 5.5. Circuit Waveforms: a) Vg, V2, Vg-V2 (MagAmp Voltage), Vx (Rectified Voltage) all 50V/div; b) Vx (50V/div), V_c (5V/div), I_R (Reset Current, 20mA/div); c) I_{SR} (MagAmp Current 2A/div) and d) I_{SR} (Expanded MagAmp Current, 20mA/div)

current (shown in Figure 5.5b. This reset current flows back into the saturable reactor once diode D1 turns off, thereby resetting the core. The amount of reset current is determined by the control voltage, V_c (Figure 5.5b): If V_o increases, V_v and V_i decrease, V_c decreases, $V_{ext} - V_c$ increases, causing the reset current, I_R, to increase, thus increasing the amount of reset. Figure 5.5d shows current through the saturable reactor.

To show the effect of varying the voltage loop, T_v, experimental results follow for three different magnitudes of T_v. Since ω_l is a function of R_1, by varying R_1, the height of T_v is moved up and down and the output impedance and audio susceptibility are changed.

The experimental results are plotted with the theoretical results. Theoretical results are found by plotting Bode plots of the transfer functions in MathCad. As discussed in Chapter III, the magnetic amplifier has a phase delay associated with it:

$$\Phi_M = -(2D' + \alpha)\frac{\omega}{\omega_s}$$

where Φ_M is the modulator phase lag; D' is the duty ratio of the off time; α is the resetting impedance factor which is equal to 0 for a current source and equal to 1 when resetting from a low impedance source, and somewhere in between for an imperfect current source; and ω_s is the switching frequency in radians. [6] This phase delay is incorporated in the MathCad theoretical results.

Since the input is alternating, measurement of audio susceptibility is not straightforward and only the theoretical results for audio susceptibility are given.

5.6.1 Test Setup

The experimental results are found using the HP4194 network analyzer. The test setups, taken from the VPEC Control Design Short Course Notes, are described as follows. Figure 5.6 shows the experimental test setup for the T1 and T2 loop gain measurements. The loop gain measurements are made by injecting a signal into the closed-loop system at points T1 and T2. A transformer couples the network analyzer's oscillator signal into the loop across a 51 Ω resistor, which minimizes the interaction with system dynamics. The analyzer's REF channel is placed to measure the injected signal into the loop and the TEST channel is placed to measure the output signal of the loop. The analyzer provides magnitude and phase measurements over frequency of its TEST channel over its REF channel which are placed as shown in Figure 5.6.

The closed-loop output impedance measurement is $\hat{V}_o/\hat{I}_o$. Referring to Figure 5.7, the network analyzer's oscillator voltage signal is injected across the output voltage and the output current is measured by acquiring the voltage across a 1 Ω resistor. The capacitor is used to block the converter output

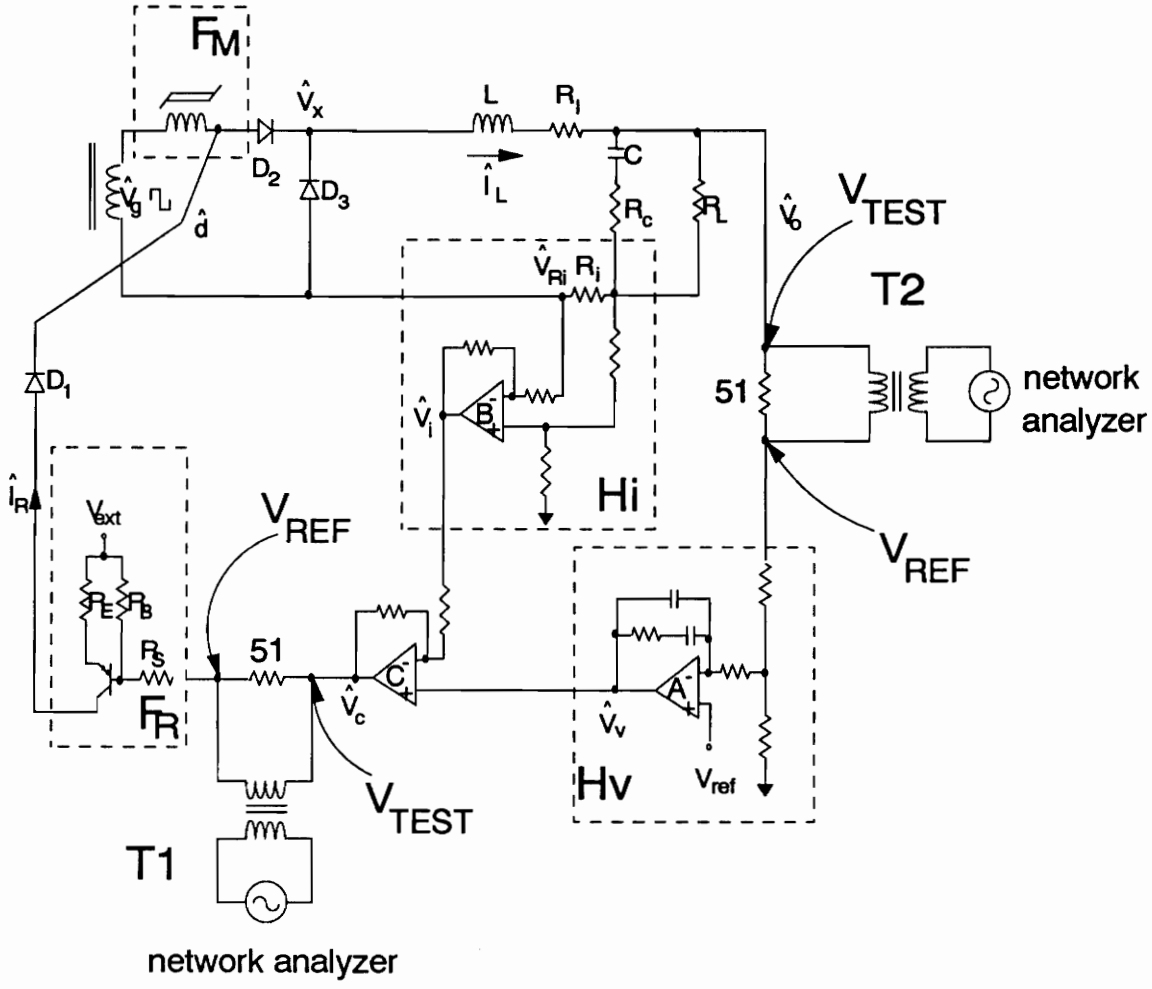


Figure 5.6. Experimental Setup for T1 and T2 Loop Gain Measurements Using HP4194 Network Analyzer

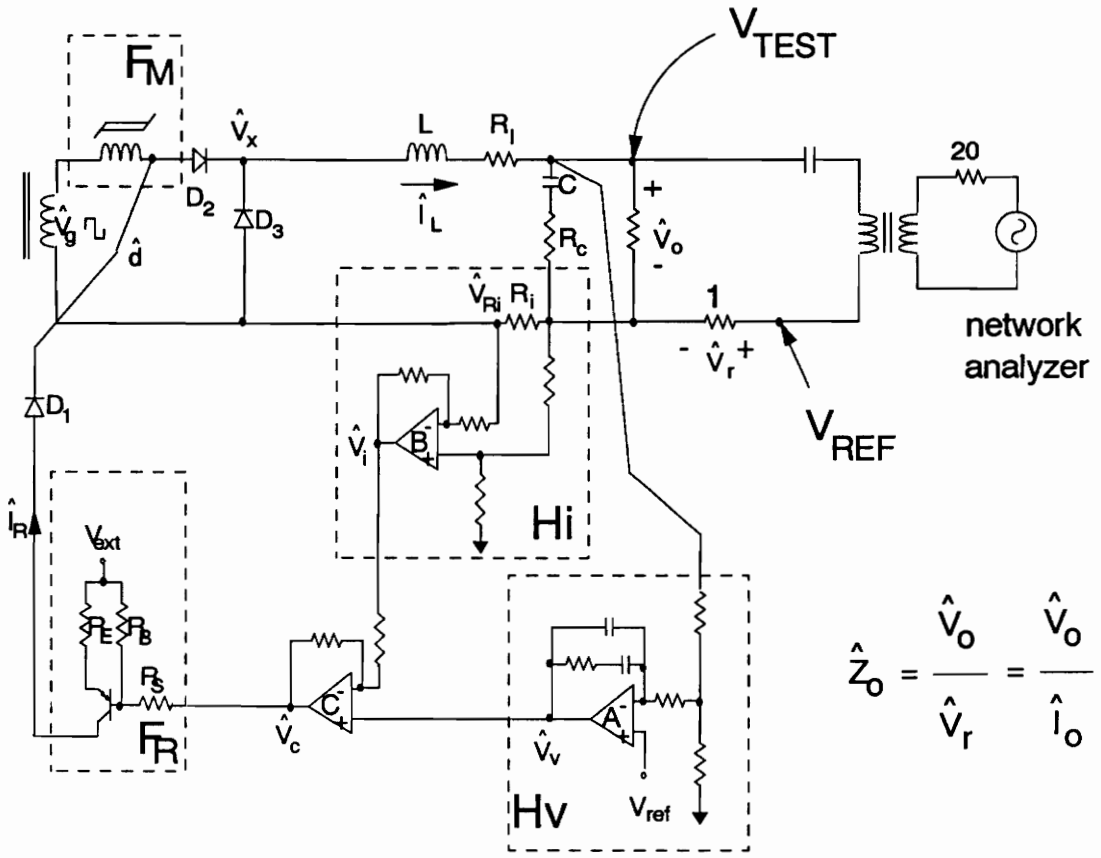


Figure 5.7. Experimental Test Setup for Output Impedance Measurement Using the HP4194 Network Analyzer

voltage. The network analyzer gives a measurement of its TEST channel over its REF channel, as placed in Figure 5.7

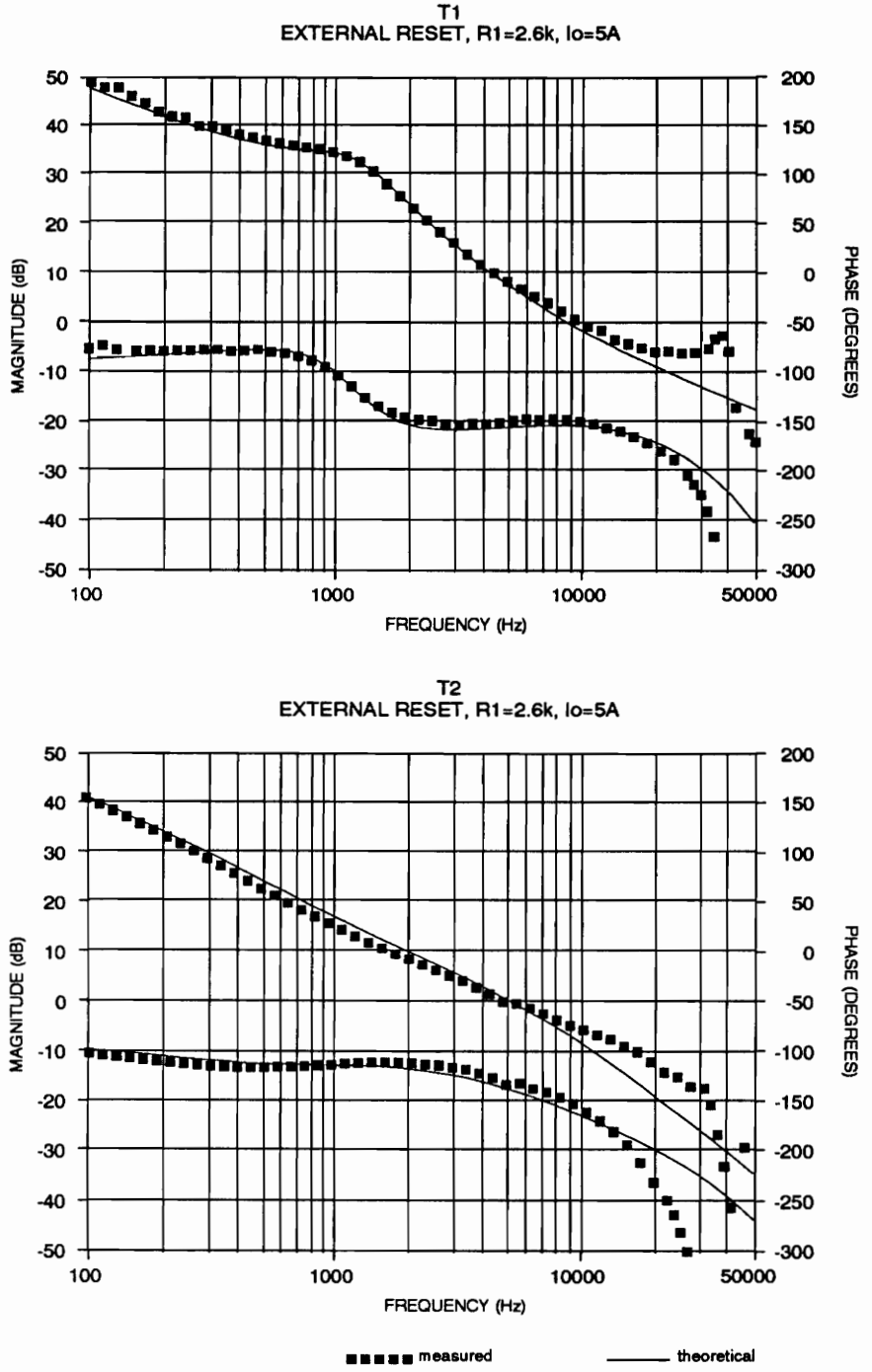


Figure 5.8. T1 and T2, $I_o = 5a$, $R_1 = 2.6k\ \Omega$: T_v increased, T2 on verge of instability

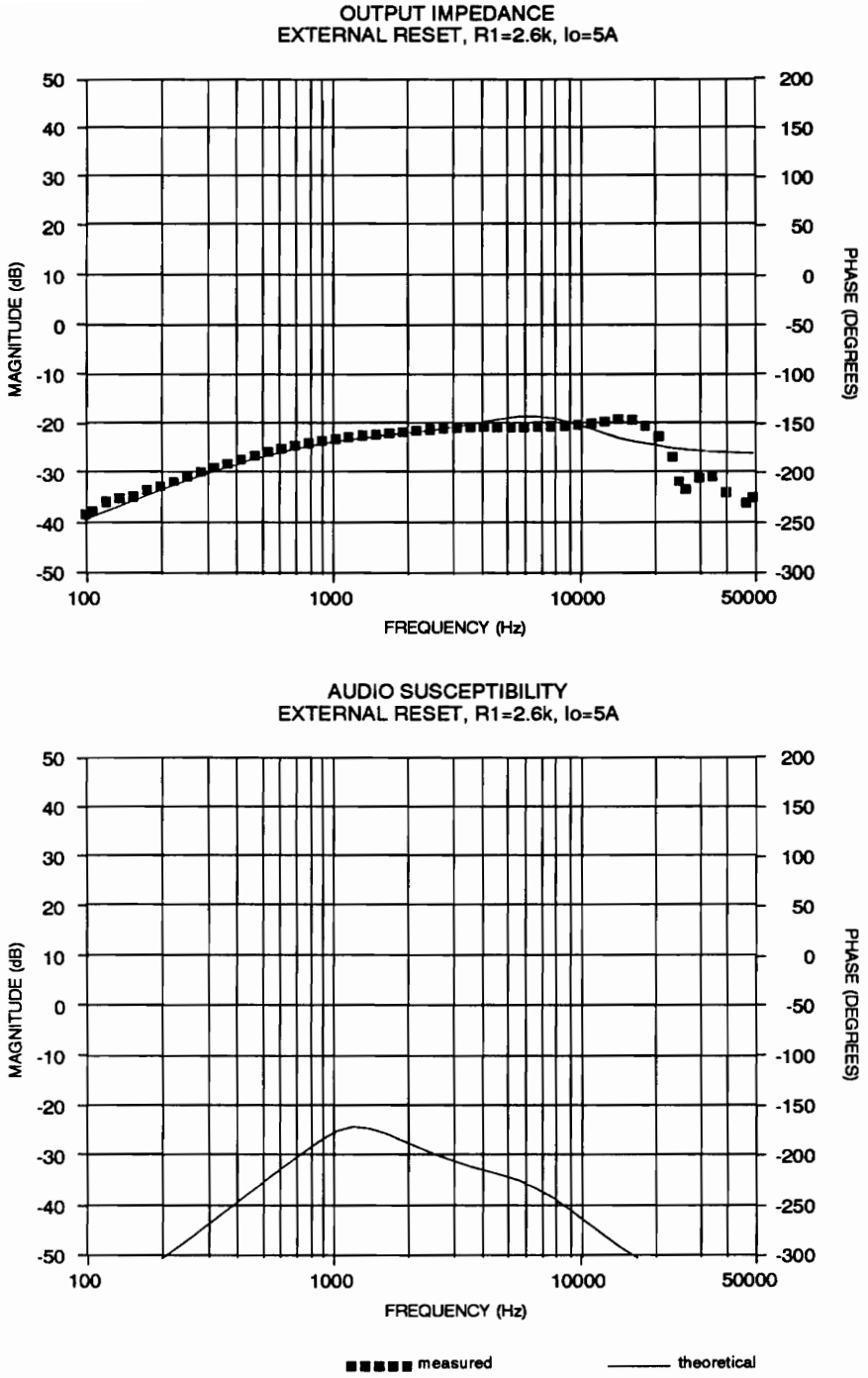


Figure 5.9. Output Impedance and Audio Susceptibility, $I_o = 5a$, $R_1 = 2.6k\ \Omega$: T_v increased, T2 on verge of instability

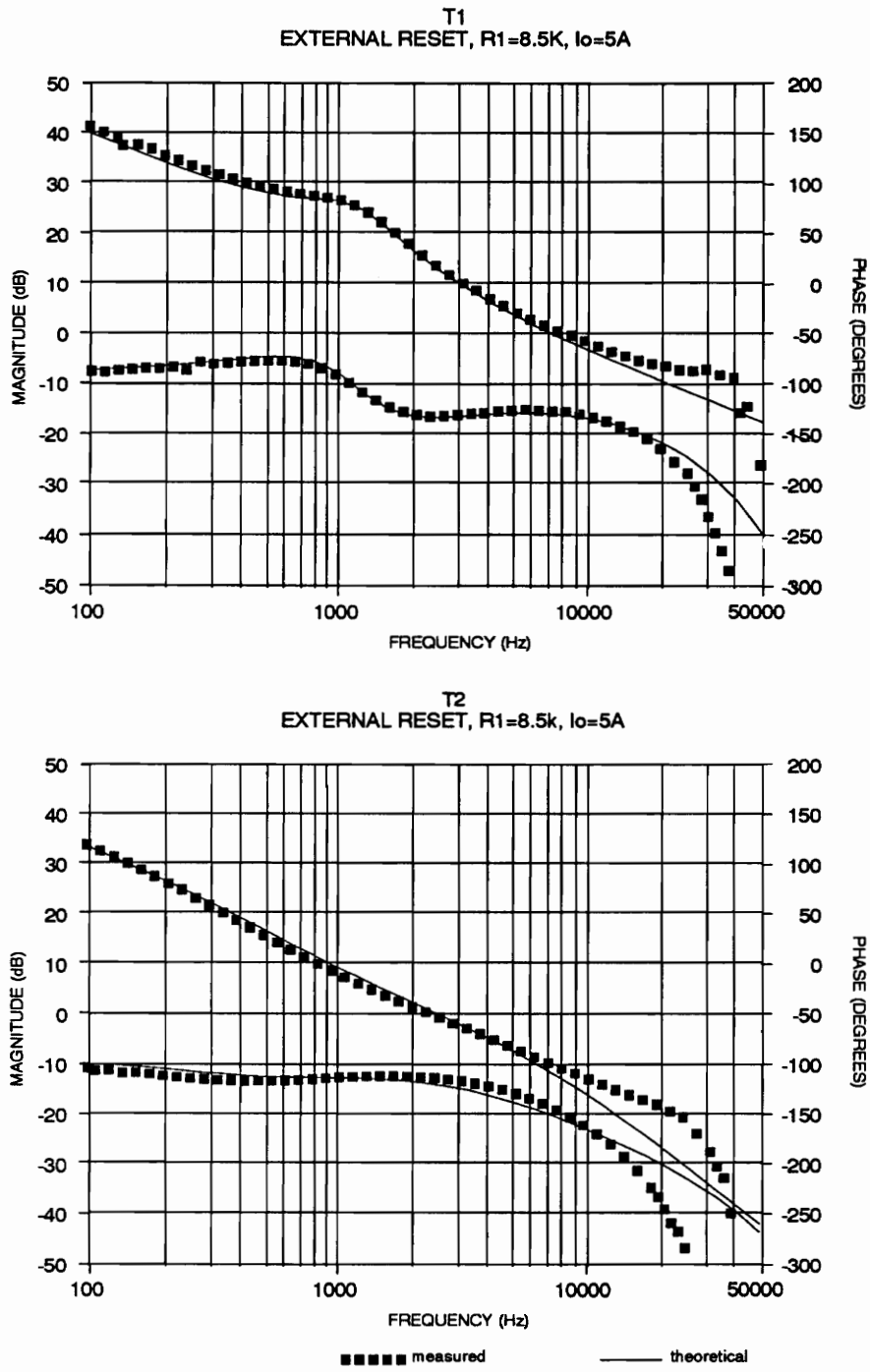


Figure 5.10. T1 and T2, I_o=5a, R_1=8.5k Ω: T_v nominal, T2 stable

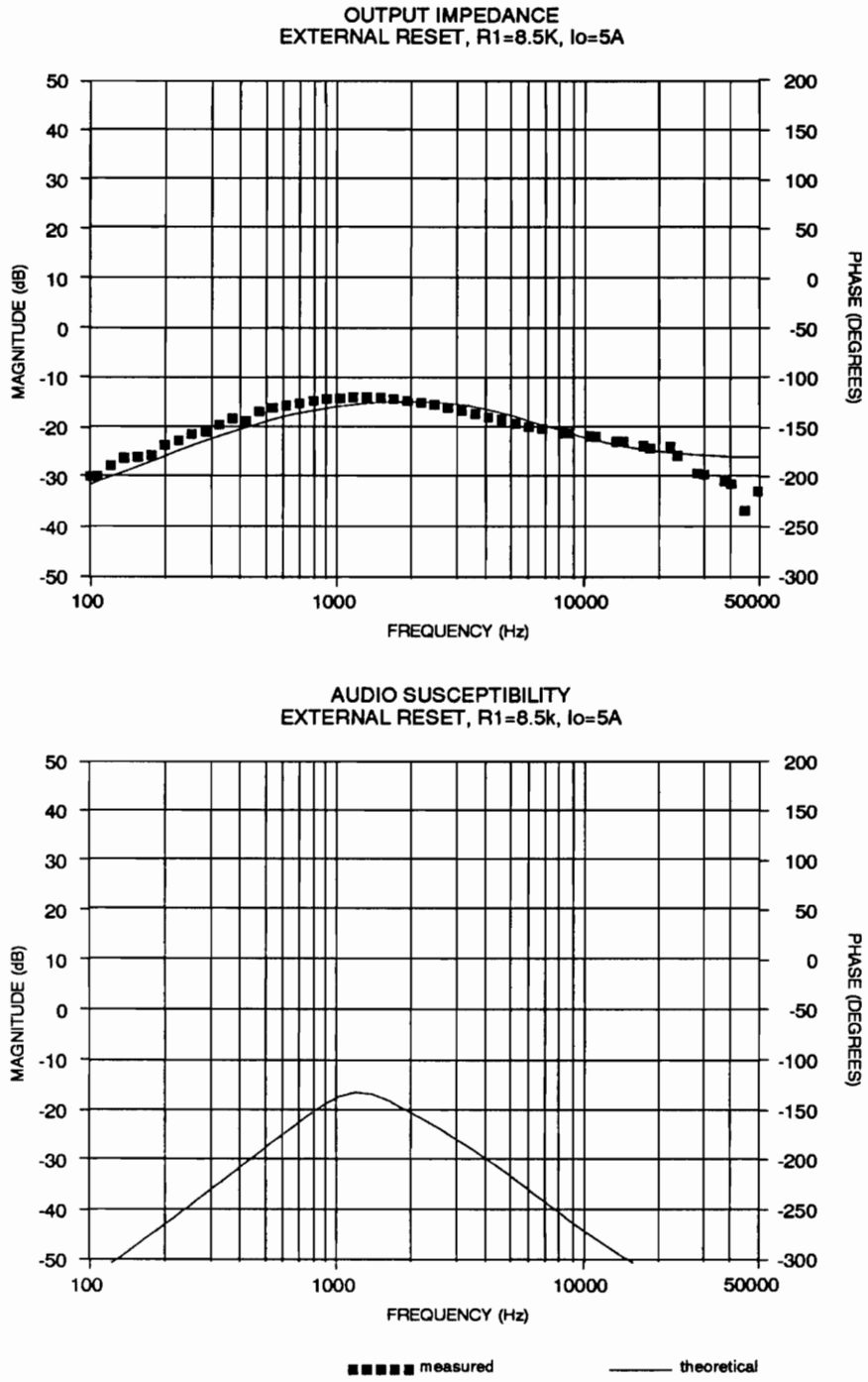


Figure 5.11. Output Impedance and Audio Susceptibility, $I_o = 5a$, $R_1 = 8.5k\ \Omega$: T_v nominal, T2 stable

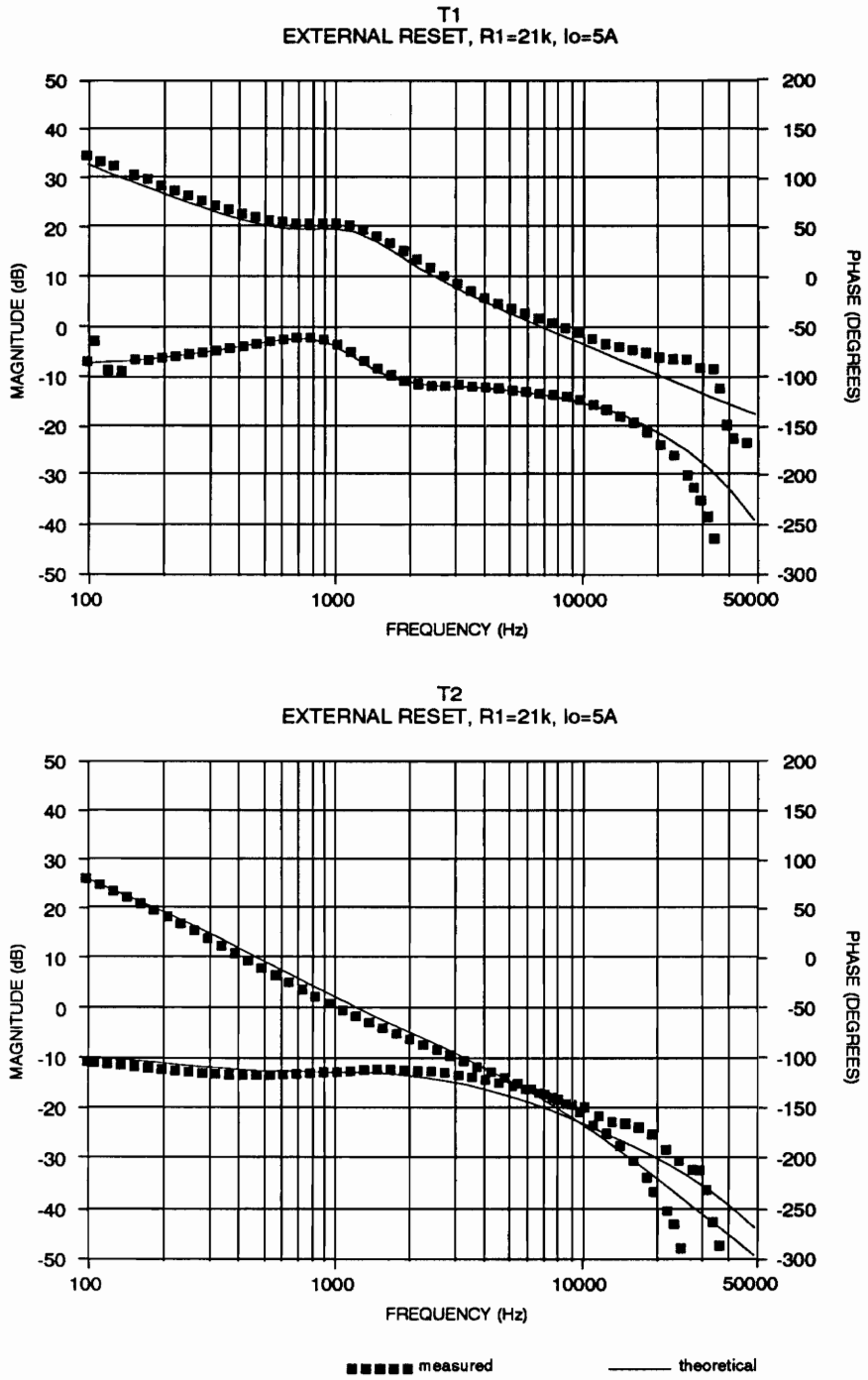


Figure 5.12. T1 and T2, $I_o = 5a$, $R_1 = 21k\ \Omega$: T_v decreased, T2 very stable

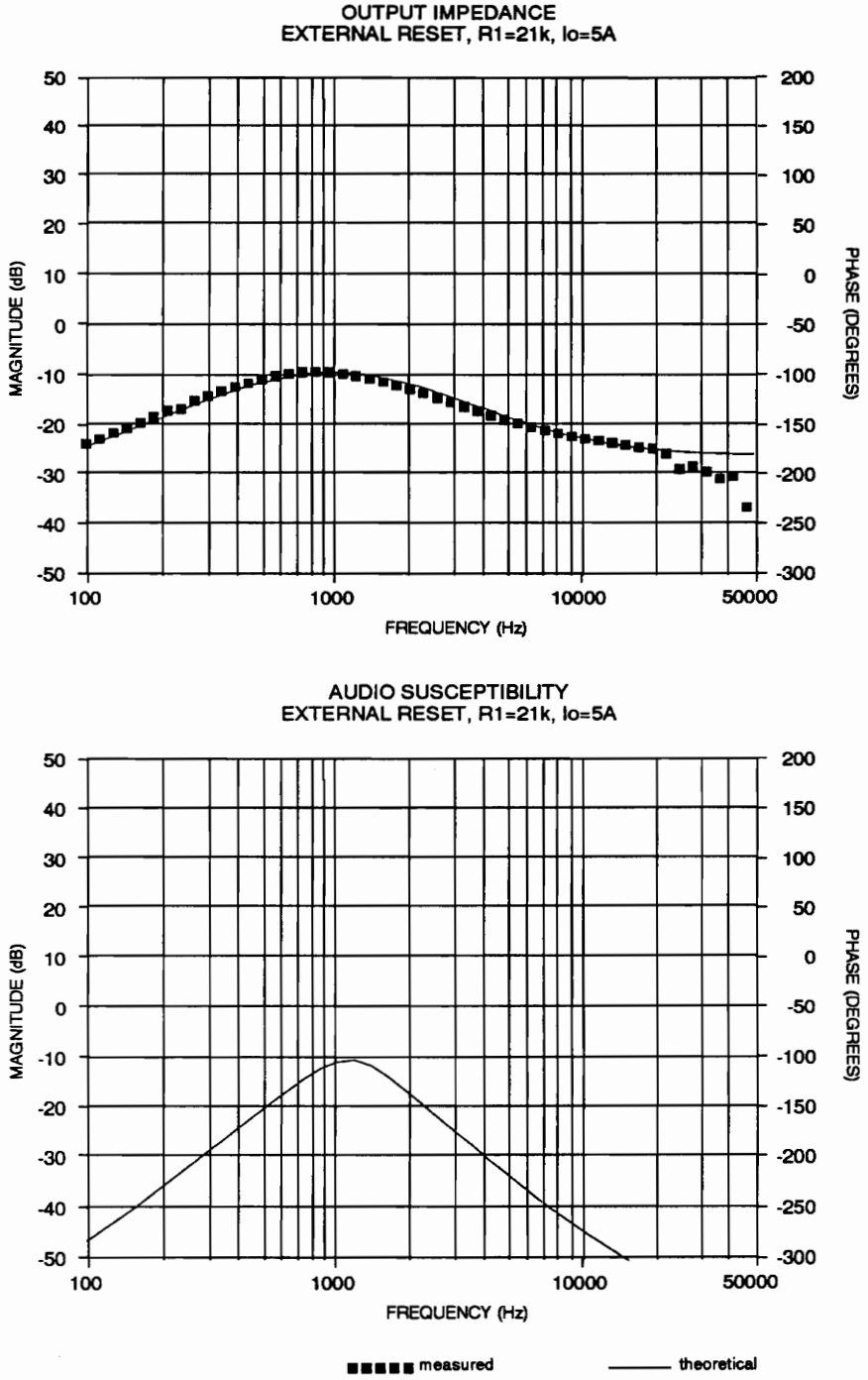


Figure 5.13. Output Impedance and Audio Susceptibility, $I_o = 5a$, $R_1 = 21k\ \Omega$: T_v decreased, T2 very stable

5.6.2 *Discussion of Results*

The measured results and the theoretical results matched very well at the lower frequencies and the model is accurate up to almost half the switching frequency in all of the measurements. At approximately half the switching frequency, there appears to be unexplained peaking in the measurements. A recent, continuous-time model for current-mode control of PWM converters [11] gives a new model based on an approximation of the sampled-data models. [12] This model shows that a new control-output-voltage transfer function $(\hat{V}_o/\hat{d})$ is created when the current loop is closed which includes a pair of complex poles at half the switching frequency. These poles would explain the peaking at half the switching frequency (and the discrepancy in phase delay). However, since the discrepancies occur at the high frequencies, the model presented in this thesis is quite adequate for design purposes.

It can be seen in the external reset results that as the voltage loop is lowered (by raising R_1), the phase margin of the outer loop gain, T2, is increased and the system is more stable. However, the performance is compromised and both output impedance and audio susceptibility increase.

5.7 Summary

In this chapter, current-mode control small-signal models were presented for a magnetic amplifier post regulator. A model was shown for the external reset method and a design example was given. Experimental verification of the model was provided.

VI. Conclusions

6.1 Summary

In this thesis, a magnetic amplifier post regulator was examined. The operation of the circuit, different types of reset methods, and a small-signal analysis were presented for the typical magnetic amplifier post regulator operation with voltage-mode or single-loop control. An extension of the analysis was made to incorporate current-mode or multi-loop control and small-signal models were developed. Experimental verification was presented.

Some motivations for using current-mode control are to allow for current sharing when parallel modules are used and to increase the performance especially when the main converter is slow.

Another motivation involves sensitivity of the circuit to the magnetic amplifier parameters changes that occur due to variations in headroom, loading, and temperature. In voltage-mode control, when external reset is used, the loop gain transfer function is $T = F_M F_R G_{vd}$. When self reset is used however, the loop gain transfer function becomes

$$T = \frac{F_M F_R G_{vd}}{1 + F_M F_R G_{vd}}$$

due to the inner loop formed. Thus, at frequencies below the zero dB crossover, the magnetic amplifier modulator gain, F_M and the reset circuit gain F_R are cancelled with self reset. This makes the voltage-mode controlled magnetic amplifier post regulator with self reset much less sensitive than the post regulator with external reset to changes in the magnetic amplifier parameters and reset circuit components at low frequencies [3].

With current-mode control however, both the self reset and external reset methods provide insensitivity to changes in the magnetic amplifier parameters at low frequencies. This is due to the fact that in the loop gains

$$T2 = (F_M F_R G_{vd} H_v)/(1 + F_M F_R G_{id} H_i)$$

with the external reset method and

$$T2 = (F_M F_R G_{vd} H_v)/(1 + F_M F_R G_{id} H_i + F_M F_R G_{vd})$$

with the self reset method, $F_M F_R$ is effectively cancelled when the magnitude of the denominator is much greater than 1. Therefore, with current-mode control, both self reset and external reset cancel F_M and F_R at frequencies below the zero dB crossover. Thus, combined with the advantages and disadvantages of using external reset and self reset, (such as easier implementation of short circuit protection with the external reset and elimination of an external supply with self reset), using current-mode control provides immunity to magnetic amplifier core variations with both reset methods.

In this thesis, for ease of demonstrating and measuring the various loop gains in the circuit, three operational amplifiers were used. In practice however, one operational amplifier may be used to perform the summation of the loops. Thus, the complexity and parts count of the current-mode control scheme is not much greater than that of the voltage-mode control scheme. This will be even more apparent with the future availability of integrated circuits for current-mode control of magnetic amplifiers.

6.2 *Suggestions for future work*

The analysis of the current-mode controlled magnetic amplifier post regulator was done with the externally supplied reset circuit. When the reset circuit of the magnetic amplifier switch is supplied by the output voltage (self reset), a fourth loop is added to the system, causing a shift in the LC corner frequency.

An analysis of the current-mode control behavior of the self reset magnetic amplifier post regulator would be worthwhile.

The experimental results and theoretical results matched very closely at the low frequencies. At the high frequencies and near the switching frequency, however, the measured results and theoretical results had some discrepancies. The phase dropped at a faster rate and sooner than predicted by the phase delay equation. There is also some unexplained peaking near the switching frequency. A more accurate method to predict this phenomenon can be developed.

The current sensing of the output filter inductor was done by putting a sensing resistor in its path. Another more efficient method of sensing the current might be to put a winding on the inductor itself. The control analysis for this method would be very similar if this were done.

Models for discontinuous conduction mode can also be developed. A recent comparison performed on a buck converter has found that the current-mode control performance is equal to or better than voltage-mode control performance. Also, it was found that the transfer functions differed very little when moving from continuous mode to discontinuous mode with current-mode control which is not the case in voltage-mode control. [10] Thus, operation in deep continuous conduction mode is not a requirement with current-mode control and the inductor can be made smaller. Since the magnetic amplifier post regulator small-signal analysis is similar to the buck converter analysis,

it should follow that this be true for magnetic amplifier circuits also. These results could be verified for magnetic amplifier post regulator in discontinuous mode of operation.

Bibliography

[1] I.J. Lee, D.Y. Chen, Y.P. Wu, C. Jamerson, "Modeling of Control Loop Behavior of Magamp Post Regulators," IEEE Transactions on Power Electronics, October, 1990.

[2] D.Y. Chen, J. Lee, C. Jamerson, "A Simple Model Predicts Small- Signal Control Loop Behavior of Magamp Post Regulator,"

[3] C. Jamerson, "Calculation of Magnetic Amplifier Post Regulator Voltage Control Loop Parameters" Proceedings of High Frequency Power Conversion Conference, April, 1987

[4] A. Urling, T. Wilson, H. Owen Jr., G. Cromwell, J. Paulakonis, "Modeling the Frequency-Domain Behavior of Magnetic-Amplifier-Controlled High-Frequency Switched-Mode Power Supplies," 1987 IEEE Applied Power Electronics Conference Proceedings, pp. 19-31.

[5] R. Tedder, "Limitations of the Magamp Regulator and an Improved Magamp Choke Design Procedure," 1988 IEEE Applied Power Electronics Conference Proceedings, pp. 109-117.

[6] R.A. Mammano, "Using an Integrated Controller in the Design of Mag-Amp Output Regulators," Unitrode Application Note U-109, 1987/1988 Unitrode Linear Integrated Circuits Databook, pp. 9-154 to 9-163.

[7] R.D. Middlebrook, "Describing Function Properties of a Magnetic Pulse-Width Modulator," Power Electronics Specialist Conference, 1972.

[8] R.D. Middlebrook, S. Cuk, "A Generalized Unified Approach to Modeling Switching Converter Power Stages," IEEE Power Electronics Specialists Conference, 1976.

[9] R.B. Ridley, B.H. Cho, F.C. Lee, "Analysis and Interpretation of Loop Gains of Multi-Loop-Controlled Switching Regulators," IEEE Transactions on Power Electronics, October 1988, pp. 489-498.

[10] D.M. Sable, R.B. Ridley, B.H. Cho, "Comparison of Performance of Single-Loop and Current-Injection-Control for PWM Converters which Operate in Both Continuous and Discontinuous Modes of Operation," IEEE Power Electronics Specialists Conference, 1990

[11] R.B. Ridley, "A New, Continuous-Time Model for Current-Mode Control," Proceedings of the Power Conversion and Intelligence Motion, October 16-19, 1989, pp. 455-464.

[12] A.R. Brown, R.D. Middlebrook, "Sampled-Data Modeling of Switching Regulators," Power Electronics Specialists Conference, June 29- July 3, 1981, pp. 349-369.

Appendix A. Small-Signal Transfer Function Derivations

A.1. Modulator Gain Transfer Function Derivation

The gain of the modulator is defined as the ratio of the change in switch duty cycle to the change in reset current:

$$F_M = \frac{\hat{d}}{\hat{I}_R} \tag{A.1}$$

From Ampere's Law,

$$\hat{I}_R = \frac{l_e \hat{H}_R}{0.4\pi N} \tag{A.2}$$

From B-H Characteristics,

$$\hat{H}_R = \frac{\Delta B}{\mu_m} \tag{A.3}$$

From Faraday's Law,

$$V_g = \frac{NA_e\Delta B}{\Delta t 10^8} \tag{A.4}$$

Perturbing eq. (A.4) by a small ac signal,

$$\Delta B = \Delta B_{DC} + \Delta\hat{B} \quad \text{and} \quad \Delta t = dT - \hat{d}T$$

and eliminating the dc quantity,

$$-V_g\hat{d}T = \frac{NA_e\Delta B}{10^8} \tag{A.5}$$

Combining eqs. (A.1), (A.2), and (A.4),

$$F_M = \frac{\hat{d}}{\hat{I}_R} = \frac{0.4\pi\mu_m N^2 A_e f_s}{l_e V_g 10^8} \tag{A.6}$$

A.2 Reset Circuit Gain Transfer Function Derivation

The reset circuit transfer function is defined as the ratio of the change in error amplifier voltage to the change in reset current

$$F_R = \frac{\hat{I}_R}{\hat{V}_c}$$

Solving for I_R,

$$I_R = [\frac{(V - V_c)R_B}{R_B - R_S} - V_{BE}]\frac{1}{R_E} \qquad (A.7)$$

where $V = V_o$ for self reset and $V = V_{ext}$ for external reset. For the external reset circuit, perturbing eq. (A.7) by a small ac signal,

$$I_R = I_R + \hat{I}_R \text{ and } V_c = V_c + \hat{V}_c$$

equating the small-signal quantities and assuming V_{ext} and V_{BE} are constant results in,

$$F_R = \frac{\hat{I}_R}{\hat{V}_c} = -\frac{R_B}{(R_B + R_S)R_E}$$

For the self reset circuit, substituting $V = V_o$ in eq. (A.7) and following the same procedure above results in,

$$I_R = -\frac{R_B}{(R_B + R_S)R_E}(\hat{V}_c - \hat{V}_o) = F_R(\hat{V}_c - \hat{V}_o)$$

Appendix B. Loop Gain Derivations

B.1 Outer Loop Gain (T2) Derivation

When the circuit is connected with the external reset scheme, an external power supply is used to power the reset transistor. The outer loop gain or T2 transfer function is found by breaking the voltage feedback loop in the block diagram. A simplified block diagram of the external reset circuit is shown in Figure B.1 and the following derivation is used to determine the T2 transfer function:

From the simplified small-signal block diagram, Figure B.1,

$$\hat{V}_o = \frac{\hat{V}_y}{H_v} \qquad (B.1)$$

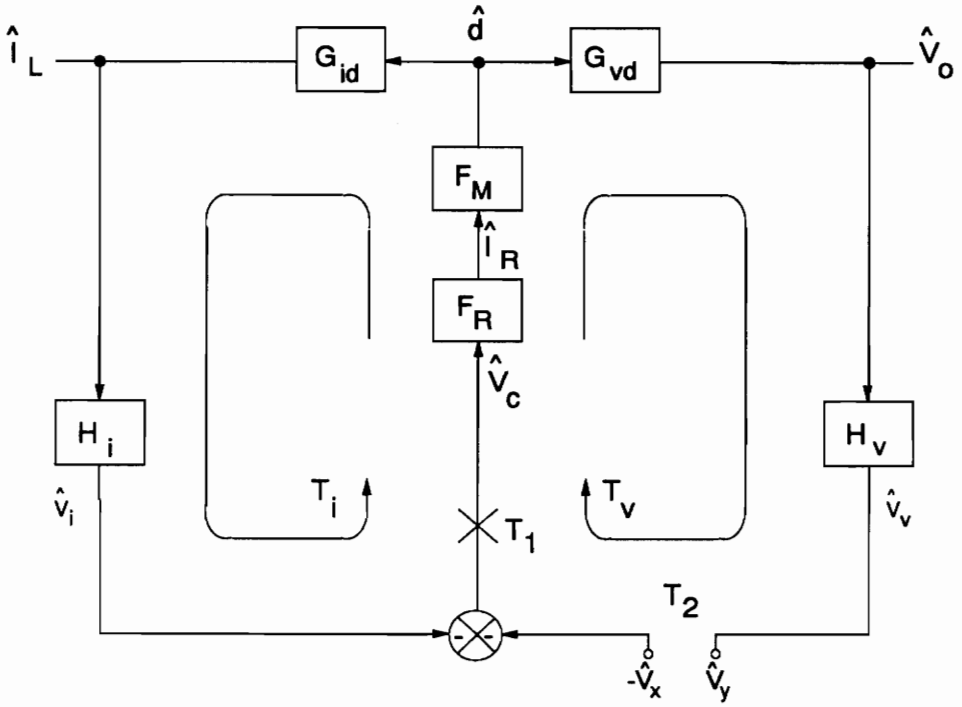


Figure B.1. Simplified Small-Signal Block Diagram for T2 Loop Gain Derivation

$$\hat{d} = \frac{\hat{V}_o}{G_{vd}} = \frac{\hat{V}_y}{H_v G_{vd}} \tag{B.2}$$

$$\hat{d} = F_M F_R(-\hat{d} G_{id} H_i + \hat{V}_x) \tag{B.3}$$

Substituting eq. (B.2) in eq. (B.3),

$$\frac{\hat{V}_y}{H_v G_{vd}} = F_M F_R\left(-\frac{\hat{V}_y G_{id} H_i}{H_v G_{vd}} + \hat{V}_x\right) \tag{B.4}$$

and regrouping,

$$\frac{\hat{V}_y}{\hat{V}_x}\left(\frac{1}{H_v G_{vd}} + \frac{F_M F_R G_{id} H_i}{H_v G_{vd}}\right) = F_M F_R \tag{B.5}$$

thus,

$$T2 = \frac{\hat{V}_y}{\hat{V}_x} = \frac{F_M F_R G_{vd} H_v}{1 + F_M F_R G_{id} H_i} \tag{B.6}$$

and from Table 5.2,

$$T2 = \frac{T_v}{1 + T_i} \tag{B.7}$$

B.2 System Loop Gain (T1) Derivation

The system loop gain or T1 transfer function is found by breaking the loop where the current feedback loop and the voltage feedback loop are summed. The simplified block diagram with the T1 loop broken is shown in Figure B.2. The derivation for this loop gain is as follows:

From the simplified small-signal block diagram, Figure B.2,

$$\hat{d} = \hat{V}_x F_M F_R \tag{B.8}$$

and

$$\hat{V}_y = \hat{d}(G_{id}H_i + G_{vd}H_v) \tag{B.9}$$

substituting eq. (B.8) into eq. (B.9),

$$\hat{V}_y = F_M F_R \hat{V}_x (G_{id}H_i + G_{vd}H_v) \tag{B.10}$$

and from Table 5.2,

$$T1 = \frac{\hat{V}_y}{\hat{V}_x} = F_M F_R G_{id} H_i + F_M F_R G_{vd} H_v = T_i + T_v \tag{B.11}$$

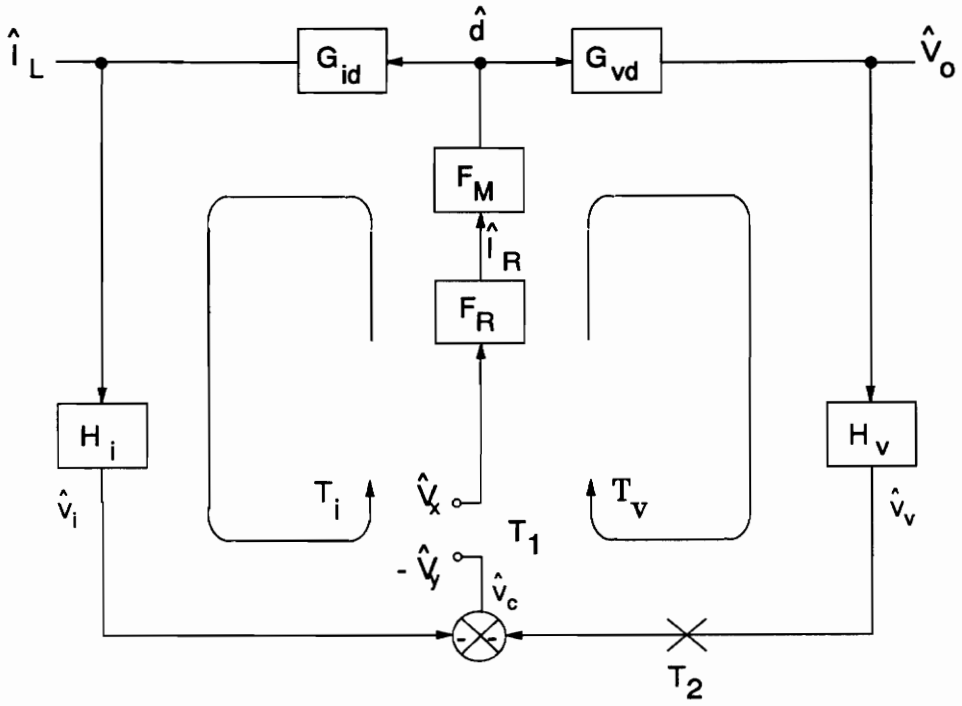


Figure B.2. Simplified Small-Signal Block Diagram for T1 Loop Gain Derivation

B.3 Output Impedance Closed-Loop Transfer Function Derivation

A simplified block diagram used to derive the closed-loop output impedance is shown in Figure B.3. The block diagram calculations are as follows:

From simplified block diagram, Figure B.3,

$$\hat{V}_o = \hat{I}_o Z_p + \hat{d} G_{vd} \qquad (B.12)$$

$$\hat{d} = - F_M F_R (\hat{I}_L H_i + \hat{V}_o H_v) \qquad (B.13)$$

and

$$\hat{I}_L = \hat{I}_o G_{ii} + \hat{d} G_{id} \qquad (B.14)$$

substituting eq. (B.14) into (B.13),

$$\hat{d} = - F_M F_R (\hat{I}_o G_{ii} H_i + \hat{d} G_{id} H_i + \hat{V}_o H_v) \qquad (B.15)$$

solving for $\hat{d}$,

$$\hat{d}(1 + F_M F_R G_{id} H_i) = - F_M F_R (\hat{I}_o G_{ii} H_i + \hat{V}_o H_v)$$

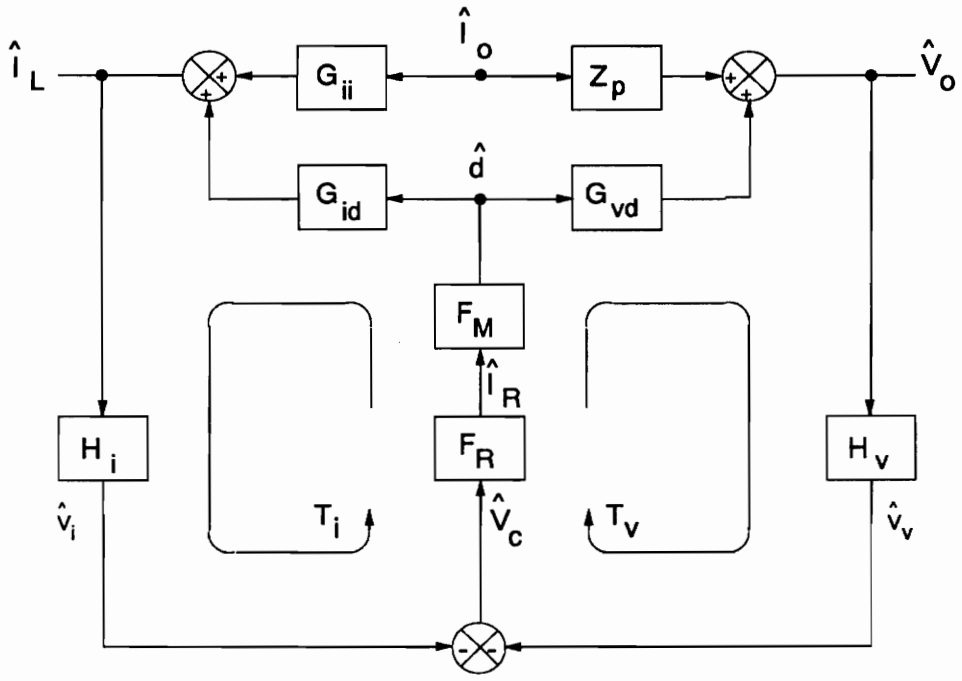


Figure B.3. Simplified Small-Signal Block Diagram for Closed-Loop Output Impedance Derivation

$$\hat{d} = -F_M F_R \frac{(\hat{I}_o G_{ii} H_i + \hat{V}_o H_v)}{(1 + F_M F_R G_{id} H_i)} \qquad (B.16)$$

substituting eq. (B.16) into eq (B.12),

$$\hat{V}_o = \hat{I}_o Z_p - \frac{G_{vd} F_M F_R (\hat{I}_o G_{ii} H_i + \hat{V}_o H_v)}{1 + F_M F_R G_{id} H_i} \qquad (B.17)$$

grouping like terms and using Table 5.2,

$$\hat{V}_o (1 + \frac{T_v}{1 + T_i}) = \hat{I}_o (Z_p - \frac{F_M F_R G_{vd} G_{ii} H_i}{1 + T_i}) \qquad (B.18)$$

thus,

$$Z_o = \frac{\hat{V}_o}{\hat{I}_o} = \frac{Z_p (1 + T_i) - F_M F_R G_{vd} G_{ii} H_i}{1 + T_i + T_v} \qquad (B.19)$$

and rewriting,

$$Z_o = \frac{Z_p + T_i (Z_p - \frac{G_{vd} G_{ii}}{G_{id}})}{1 + T_i + T_v} \qquad (B.20)$$

In the case of the magnetic amplifier post regulator, when the transfer functions from Table 5.1 are substituted in, eq. (B.20) can be rewritten as:

$$Z_o = \frac{\hat{V}_o}{\hat{I}_o} \simeq \frac{Z_p}{1 + T1} + \frac{\frac{R_L}{1 + sR_LC}}{1 + T2}$$

at frequencies below the crossover of the current loop, T_i.

B.4 Audio Susceptibility Closed-Loop Transfer Function Derivation

A simplified block diagram used to derive the closed-loop audio susceptibility is shown in Figure B.4. The block diagram calculations are as follows:

From simplified block diagram, Figure B.4,

$$\hat{V}_o = \hat{d}G_{vd} + \hat{V}_g G_{vg} \qquad (B.21)$$

$$\hat{d} = -F_M F_R(\hat{I}_L H_i + \hat{V}_o H_v) \qquad (B.22)$$

and

$$\hat{I}_L = \hat{V}_g G_{ig} + \hat{d}G_{id} \qquad (B.23)$$

substituting eq. (B.23) into (B.22) and solving for $\hat{d}$,

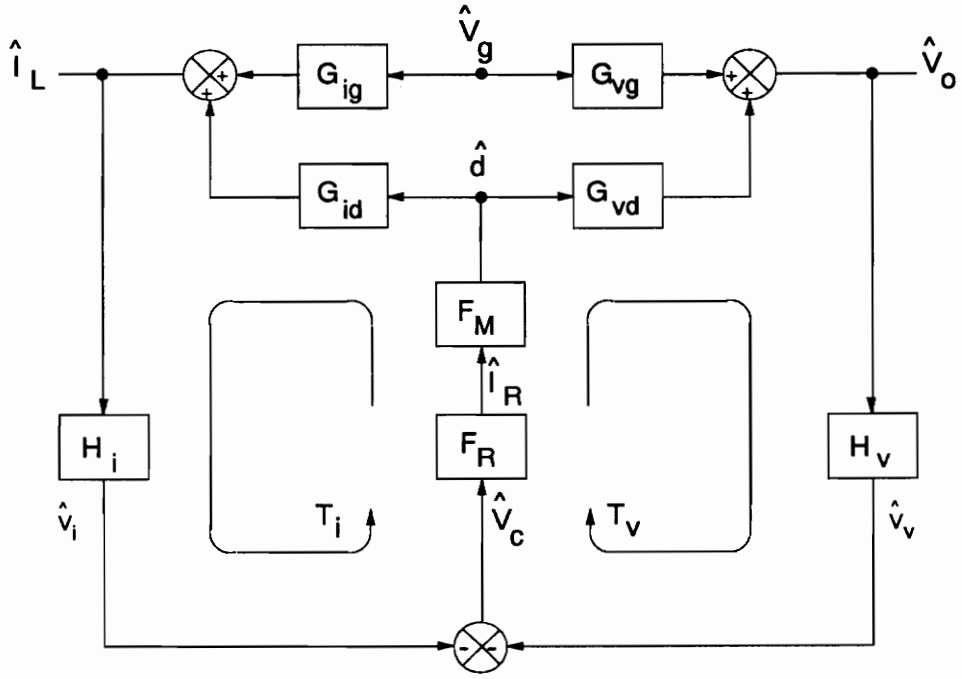


Figure B.4. Simplified Small-Signal Block Diagram for Closed-Loop Audio Susceptibility Derivation

$$\hat{d} = -F_M F_R \frac{(\hat{V}_g G_{ig} H_i + \hat{V}_o H_v)}{(1 + F_M F_R G_{id} H_i)} \tag{B.24}$$

substituting eq. (B.24) into eq (B.21),

$$\hat{V}_o = \frac{-F_M F_R G_{vd}(\hat{V}_g G_{ig} H_i + \hat{V}_o H_v)}{1 + F_M F_R G_{id} H_i} + \hat{V}_g G_{vg} \tag{B.25}$$

grouping like terms and using Table 5.2,

$$\hat{V}_o(1 + \frac{T_v}{1 + T_i}) = \hat{V}_g(G_{vg} - \frac{F_M F_R H_i G_{vd} G_{ig}}{1 + T_i}) \tag{B.26}$$

thus,

$$A_s = \frac{\hat{V}_o}{\hat{V}_g} = \frac{G_{vg}(1 + T_i) - F_M F_R H_i G_{vd} G_{ig}}{1 + T_i + T_v} \tag{B.27}$$

and rewriting,

$$A_s = \frac{G_{vg} + T_i(G_{vg} - \frac{G_{vd} G_{ig}}{G_{id}})}{1 + T_i + T_v} \tag{B.28}$$

In the case of the magnetic amplifier post regulator (buck converter family), when the transfer functions of Table 5.1 are used,

$$G_{vg} - \frac{G_{vd} G_{ig}}{G_{id}} = 0$$

Therefore, A_s reduces to:

$$A_s = \frac{G_{vg}}{1 + T_i + T_v}$$

Vita

The author was born in Upper Montclair, New Jersey in 1963. She received her bachelor of science degree in Electronics Engineering Technology from Trenton State College, New Jersey. She joined the Virginia Power Electronics Center at Virginia Tech in 1988 working toward her master of science degree in the field of power electronics.