Insulated Gate Bipolar Transistor (IGBT) Simulation Using IG-Spice

by

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(Abstract)

A physics-based insulated gate bipolar transistor (IGBT) model has been successfully implemented into a widely available circuit simulation package, IG-Spice. Based on the semiconductor physics, the model accurately predicts the nonlinear junction capacitance variations, recombinations, and conductivity modulation of the power device.

The procedure to incorporate the model into IG-Spice and various methods to ensure convergence are described. The IG-Spice IGBT model is presented, including all the physical effects which have been shown to be important in describing the device. Effectiveness of the model is shown by comparing the measured data for single device used in inductive load, and by comparing the static and dynamic current sharing of paralleled IGBTs. The simulated results are verified with experimental results. Accuracy is determined by the accuracy of the required parameters extracted.

To my Dad, Terry J. Mitter.

Acknowledgments

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Most of all, thank you GOD for giving me a new life!

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Chapter 1

INTRODUCTION

The Insulated Gate Bipolar Transistor (IGBT) was introduced into the family of power devices to overcome the high on-state loss of power MOSFETs while maintaining simple gate drive requirements. The IGBT combines both the bipolar and MOSFET structures and possesses the best features of both device types. Because the IGBT has a low power gate drive requirement, a high current density capability, and a high switching speed, it is preferred over other devices in many high-power applications.

A physics-based IGBT model suitable for general circuit simulation has been previously introduced [1-6] and verified for representative circuit operating conditions. This model is based on the analytical equations describing the semiconductor physics. The model accurately describes the nonlinear junction capacitances, moving boundaries, recombination, carrier scattering, and effectively predicts the device conductivity modulation. Although many types of power devices exist, the semiconductor device models presently provided within most circuit simulation programs are based upon microelectronics devices and cannot readily be used to describe the internal MOSFETs and internal bipolar transistors of the power devices.

Semiconductor device models within the Berkeley-Spice and Pspice circuits simulators are based upon the small signal models, and as result they, cannot accurately simulate the effect of power

devices such as IGBTs. The IGBT model implemented with IG-Spice overcomes these limitations by using the physics oriented model.

In Chapter 2 the physical structure of the IGBT device is discussed in order to give a clear understanding of the operation of this device. Also, the special characteristics of the IGBT device are briefly presented, and its switching characteristics discussed. The advantages and disadvantages of the IGBT are also discussed.

Chapter 3 looks at the equivalent circuit of Dr. Allen Hefner's model, along with the simplified classical circuit model. Special features of the analytical model which cannot be ignored are discussed, and the purpose of using this physics-oriented model is presented. Also a brief discussion of parameter extraction method is presented, as will the algorithm for the parameter extraction.

Chapter 4 discusses several Spice-related simulation packages and discuss why regular Berkeley Spice or Pspice was not appropriate. Here general Spice algorithms are observed in order to see what methods are required to implement circuit models. The in-depth discussion of the IG-Spice subroutines using the state variables is also presented, as are step-by-step procedures for implementing analytical equations.

Chapter 5 discusses the actual transformation of the physics model into IG-Spice form, controlled sources, in detail. Also certain criteria in implementing these controlled sources to ensure convergence are presented. Then the simulated results showing the special properties of the IGBT device are shown using the simulated data. The effectiveness of the model will be also shown by implementing it in a paralleled operation of the devices. Finally, the measured results and their accuracy are discussed.

Chapter 2

REVIEW of IGBT DEVICE CHARCTERISTICS

2.1 Introduction

In the power electronics arena there is a constant demand for compact, lightweight, and efficient power supplies. However, the demands for the power converters are not fully satisfied by power bipolar transistors (BJTs) and power MOSFETs. High current and high voltage BJTs are available, but their switching speeds are not satisfactory. Power MOSFETs have high speed switching, but high voltage and high current modules are not available.

The insulated gate bipolar transistor (IGBT) device is a power semiconductor device introduced to overcome the limitations of the power BJTs and power MOSFETs. This device eliminates the high on-state of the MOSFET while maintaining the simple gate drive of that device. This device is controlled by the gate voltage as that of a MOSFET, but the output current is that of a bipolar transistor. These devices combine best features of both the bipolar transistors and MOSFET.

In this chapter, a physical properties and IGBT structures will be reviewed.

2.2 Physical Operation of IGBT

A schematic structure of an n-channel IGBT device is shown in Fig. 2.1. The structure is similar to that of an Vertical Double Diffused MOSFET (VDMOSFET) with the exception that a p-type heavily doped substrate replaces the n-type drain contact of the conventional VDMOSFET (see Fig. 2.2). The p-type substrate is the emitter of bipolar and is the anode terminal of the device. When sufficient gate voltage is applied, the current that flows at the surface of the MOSFET channel enters the low doped epitaxial layer and appear as an drain current at the substrate. In turn the heavily doped p+ substrate injects minority carriers into the low n- epitaxial layer. The large n- area is needed in order to block high voltages, but it contributes to a large on-state resistance. But the minority carrier injection by the p- substrate serves to reduce this resistance and thus modulates its conductivity. The injected minority carrier density is typically 100 to 1000 times higher then the doping level of the n-type epitaxial drift region.

The minority carriers which did not recombine will diffuse towards the body, and they are collected by the body-epitaxial layer which has been reverse-biased in the forward conduction operation. The MOSFET is formed under the gate where the body meets the surface, and this MOSFET provides the electrons (majority carrier) for recombination in the epitaxial layer and some are injected into the p-substrate region. The schematic diagram showing the flow of the carriers is shown in Fig. 2.3.

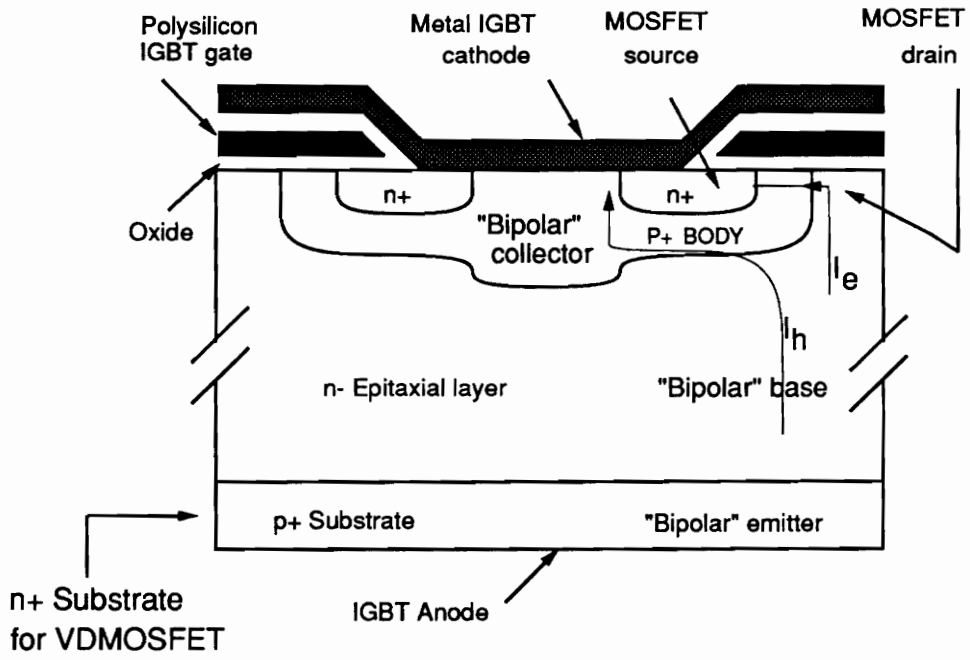

Figure 2.1. Basic structure of IGBT.

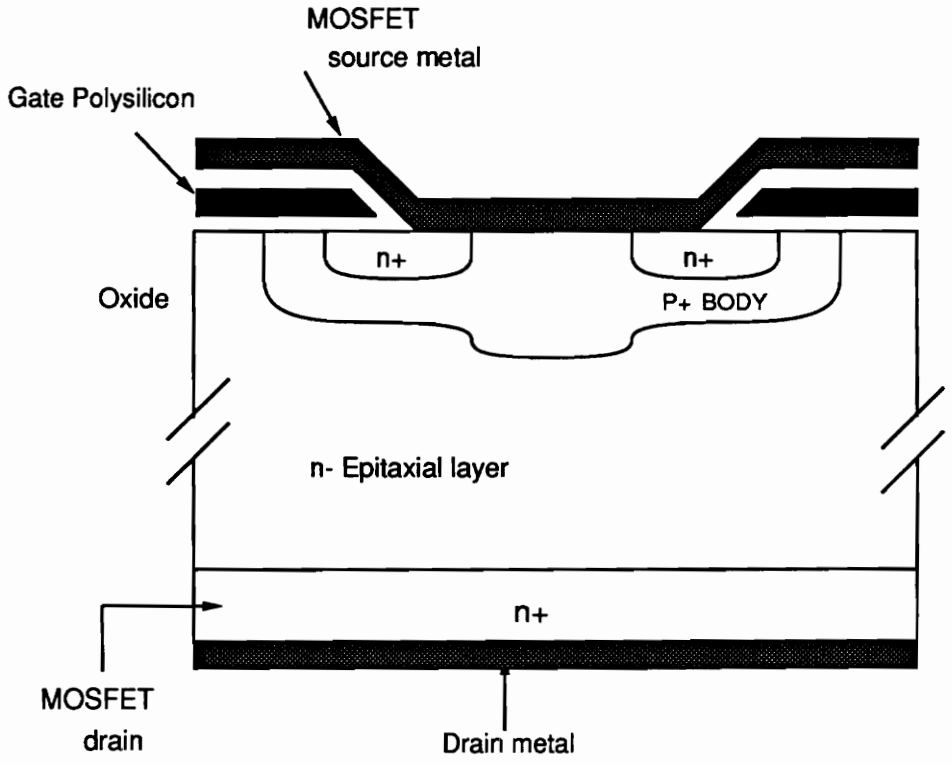

Figure 2.2. Basic structure of VDMOSFET.

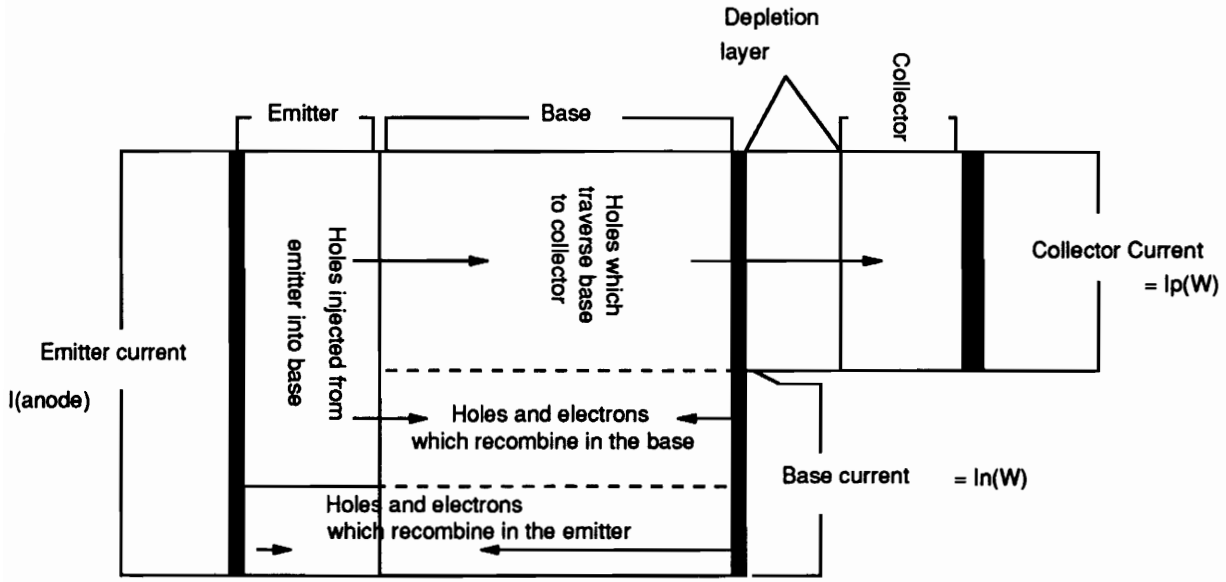

Figure 2.3. A schematic representation showing the carrier distribution.

2.3 IGBT Equivalent Circuit

The simplified equivalent circuit representing the internal structure is shown in Fig. 2.4. The circuit consists of n-channel MOSFET, PNP, and NPN bipolar transistor. (This is a conceptual model and should not be confused with the actual physical structure of the IGBTs.)

As shown in the model, the bipolars PNP and NPN form a four layer npnp structure of an SCR. If the gains of the both transistors are significant enough, the BJTs will latch on and behave just as an SCR. But this latching process is avoided by the base-emitter short resistance, $r'_{b,}$ in the equivalent circuit. This resistance act as an shunt to the base of the NPN; thereby bipolar NPN never turns on strong enough to start the latching process.

Since the current to the base of NPN bipolar is bypassed, NPN can be assumed to be off, and this assumption results in more simplified equivalent circuit of Fig. 2.5. This equivalent circuit only consists of an PNP bipolar and N-channel MOSFET. The simplified equivalent circuit clearly shows that the drain current of the MOSFET (electron current) supplies the base current of the PNP bipolar. The sum of electron current and hole current make up the total collector current of the IGBT device.

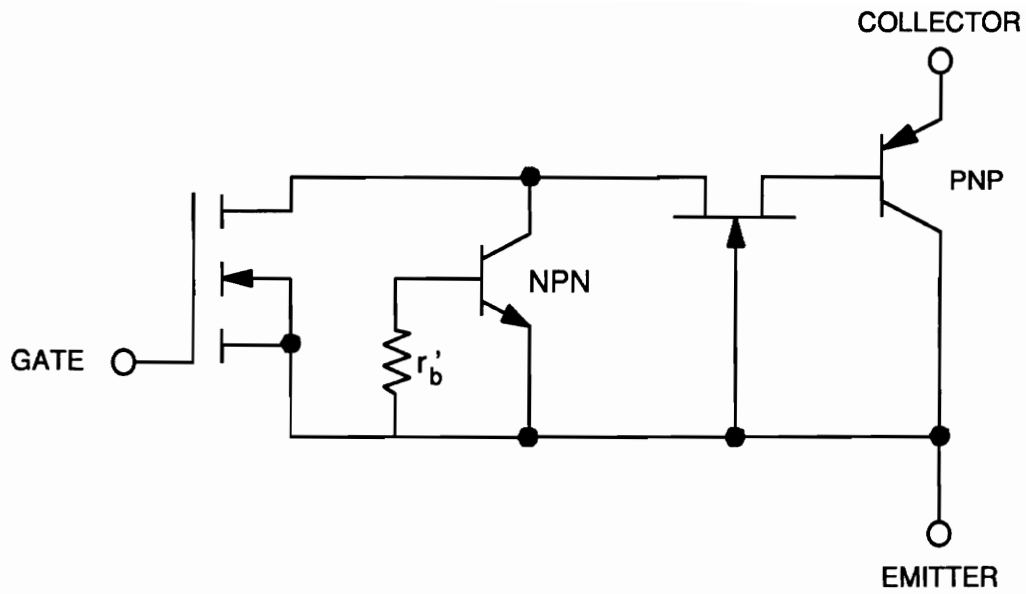

Figure 2.4. IGBT equivalent circuit showing the parasitic components.

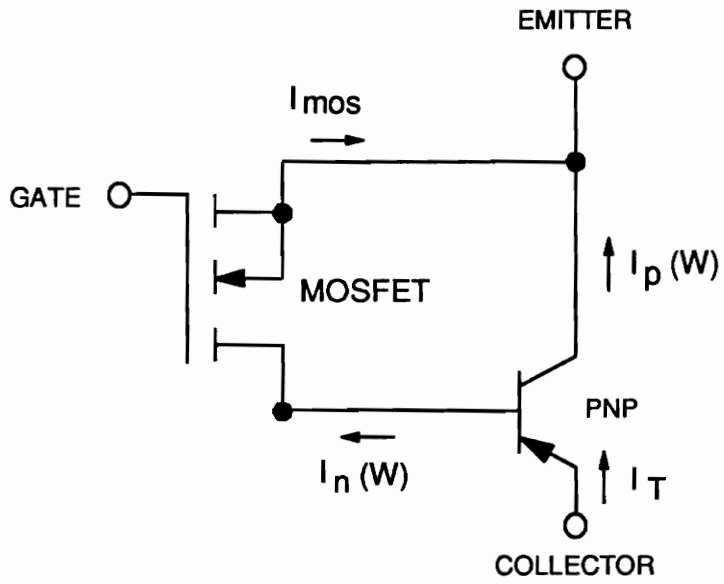

Figure 2.5. A simplified conceptual representation of IGBT.

2.4 Properties of IGBT

2.4.1 Ease of gate drive

As seen previously, the IGBT combines the best features of the devices mentioned. It uses the low power, voltage drive, gate drive to turn on and off, and possess as a high an input impedance gate as that of the MOSFET.

The structure of IGBT also reduces the reverse transfer capacitance, C_{rss}. This capacitance is the series combination of C_{je} of the PNP and C_{rss} of the MOS structure. This small capacitance results in a very low gate drive power requirement, since only small gate capacitance charging and discharging currents are required. For the same size die at 500 V, the gate charge required to switch the IGBT is about 20% smaller than that required for the FET.

Along with small Crss capacitance, the IGBT also exhibit small gate-to-drain capacitance C_{DG}. The large value of this feedback capacitance can cause complexity in gate drive circuits due to its coupling of the drain voltage swings to the gate, which can cause the device to turn on during turn-off time. This known as a dv/dt problem.

2.4.2 Low conduction loss

The conductivity modulation greatly increases the current-handling capability of an IGBT for a given die size. This conductivity modulation has been shown to increase the forward conducting current density at given anode voltage up to 20 times that of an equivalent MOSFET and five times that of an BJT [14]. Because this process reduce the on-resistance of the device, the conductions loss is minimized.

2.4.3 Positive temperature coefficient

The IGBT also has a favorable temperature coefficient for on-resistance [10]. At high currents the on-resistance increases with increase in temperature, and because of this moving resistance region, the device will not experience the thermal runaway or formulation of hotspots which occur in the power BJTs. In fact, it was shown that with increasing temperature, the variation in current is very little, and in parallel combination, it improved the current sharing of the devices [11].

2.4.4 No internal anti-parallel diode

With the removal of the source-gate short of MOSFET, IGBT can block reverse voltage (approximately -20 V); and with the use of series diode, blocking capability can be greatly increased. The absence of this anti-parallel diode protects the IGBT from reverse conduction problems in the free-wheeling diode, which can occur in power MOSFETs.

2.4.5 Current tail

Even with many favorable qualities, the IGBT device possess few unwanted characteristics. One of thiese is the slow switching speed compared to MOSFET. When the device operates in forward conduction, the high resistance region n- epitaxial layer is highly injected with excess minority carriers in the process of conductivity modulation. When the gate voltage is removed, this excess of minority carriers must be removed before the device stops conducting completely. The turn-off speed of the device is determined by the integral bipolar open base collector. This slow switching contributes to large switching energy and limited operation frequencies. Turn-on time is very fast and is determined by the rate of saturation of the integral PNP bipolar transistor [1].

2.5 Switching Characteristics

Because the IGBT is a MOS-type device, during turn-on the switching performance is dominated by the MOS structure of the device. When the gate drive voltage is brought above the threshold voltage of the gate-source of the IGBT, the MOSFET structure turns on very quickly and starts to conduct. The MOSFET drain current then becomes the base current of the integral bipolar PNP structure, and as a result, the turn-on speed of the IGBT is comparable to the power MOSFETs of equal input capacitance (C_{iss}).

Figure 2.6 shows the waveforms describing the switching characteristics of the IGBTs. The figure show the turn-on and turn-off characteristics of the device. From the figure it can be seen that there are three distinct intervals which comprise the total turn-off of IGBTs.

First part of the turn-off process is the delay time ($t_{d(off)}$), which is the effect of the time required for the gate drive to pull V_{gs} from its full value to the level at which the drain current begins to decrease.

The second interval is the initial fall time (t_{f1}), and this is the time required for the gate drive circuit to remove the charge injected into the gate by the gate-to-drain capacitance as V_{DS} increases during turn-off. This period is defined as the time it takes for I_D to drop from 90% of its full current down to approximately the 20% level. This period is greatly influenced by the gate drive design and its drive impedance, R_{GS}.

The third interval, defined as t_{f2}, is a result of minority carrier recombination in the bipolar PNP structure. This tailing effect is the direct result of internal base of the PNP structure, which cannot be excessed by the external means. Because this base of PNP is inexcessible, we cannot pull the excess minority carriers by reverse bias scheme. The rate at which this recombination can be controlled is a function of device design and process technology.

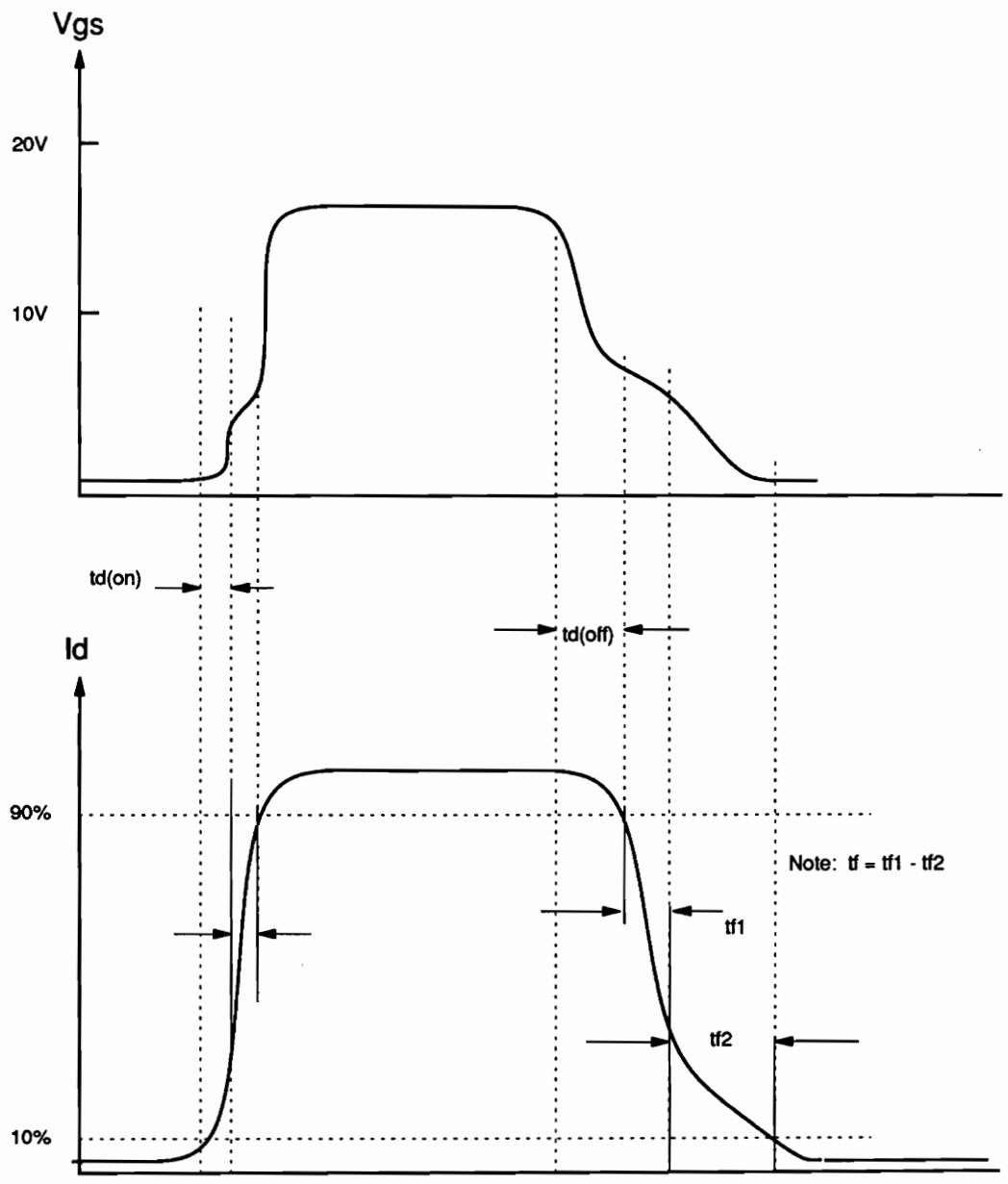

Figure 2.6. IGBT Switching Waveform for Turn-on and Turn-off.

2.6 Summary

The IGBT is a new power semiconductor device which possesses the best features of both the MOSFET and bipolar transistor. The device is controlled by a low power voltage gate drive similar to that of MOSFETs, and current is that of bipolar transistor. Large gate drive current power loss is avoided due to its simple gate drive. When operating in forward conduction mode, the conduction loss is reduced by the conductivity modulation achieved by high level minority carrier injection from the p+ substrate into the n- epitaxial region. It is seen that the current density is 20 times that of a MOSFET and five times that of a BJT because of the conductivity modulation. With removal of its internal parallel diode in MOSFET, the IGBT has the capability to block reverse voltage. At the present, a switching frequency of 10 Khz - 100 Khz can be used. An IGBT also has positive temperature coefficient which prevents the device from hotspot formation or thermal runaway.

Compared to the MOSFET, switching speed is relatively slow, and its disadvantage is that at switching-off time, a large current tail is present, which contributes to large switching energy loss. This tailing effect was due to the time required to remove the excess minority carriers within the deep n- region. Therefore, the switching on-time and off-time is limited by the open base integral bipolar and its saturation speed.

Chapter 3

IGBT PHYSICAL MODEL

3.1 Introduction

Recently, a physics-based IGBT model has been introduced [1-6]. This model is based on the analytical equations describing the semiconductor physics. The model accurately describes the nonlinear junction capacitances, moving boundaries, recombination, carrier scattering, and effectively predicts the device conductivity modulation.

In this chapter a new analytical model that has been introduced is reviewed. Then the equivalent circuit of this new physics-based model is discussed. Then the required parameter extraction algorithm is reviewed briefly.

3.2 Fundamentals of the Model

Most of the models that have been presented use the analytical approach with the simple MOS-BJT equivalent circuit as shown in Fig. 3.1. However, the models that use the equivalent circuit as shown in Fig. 3.1 cannot correctly describe all of the IGBT characteristics. The bipolar transistor of IGBT consists of a low-doped, wide base region, with the base contact at the collector end of the base (see fig. 3.2). This transistor is of a low gain ($I_n \sim I_p$) and is operated within the high-level injection mode for typical operation of the device. Traditionally, the bipolar transistor was assumed to have narrow base width, and at high level injection level it was assumed that the majority carrier current was much less than the minority carrier in the base, but because the IGBT bipolar is of low gain type, this view cannot be held if the correct IGBT characteristics are to be described. Because neither the hole current nor electron current is negligible for typical operation of the IGBT device, the ambipolar transport is used to describe the current flow within the wide base of the PNP bipolar of the IGBT.

In Fig. 3.3, it is seen that the base, collector, and the drain come into contact at a same point. This structure allows the electron currents supplied by the MOSFET to be entered at the collector edge of the base contact. This epitaxial layer-body junction is neutral of excess carrier concentration and is assumed to be zero in value; it is the point of contact between the bipolar transistor base and the MOSFET drain. The excess carrier concentration at the epitaxial layer-body junction is zero because this junction is reverse biased when the device is in forward conduction mode. As a result, the base current flows from the collector through the base in the same direction as the collector current (sum of the electron and hole currents) is constant throughout the base. As shown in the Fig. 3.1, the electron current at this junction is equal to the MOSFET current and the hole current, which make up the collector current of the bipolar

transistor and this current, remains constant throughout the base. Therefore, high level injection characteristics of the bipolar transistor can be characterized by using one dimensional ambipolar terms [6]. The sum of the MOSFET current and the collector current of the bipolar transistor make up the total current of the device.

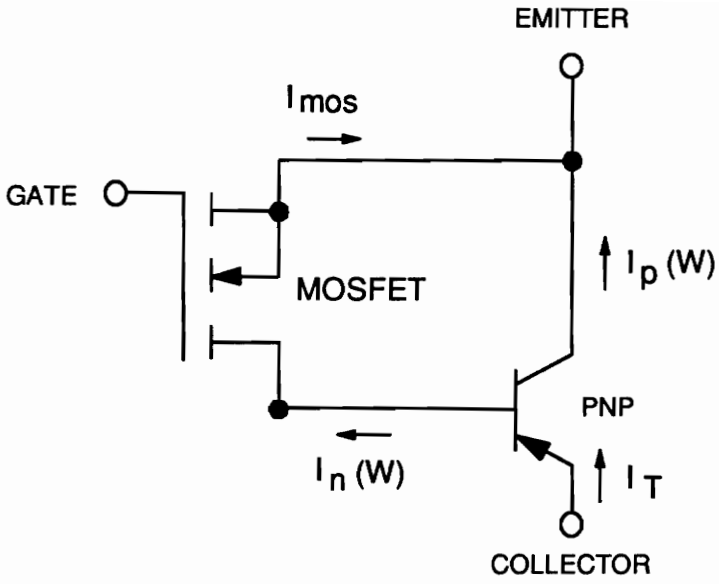

Figure 3.1. Simplified equivalent IGBT circuit.

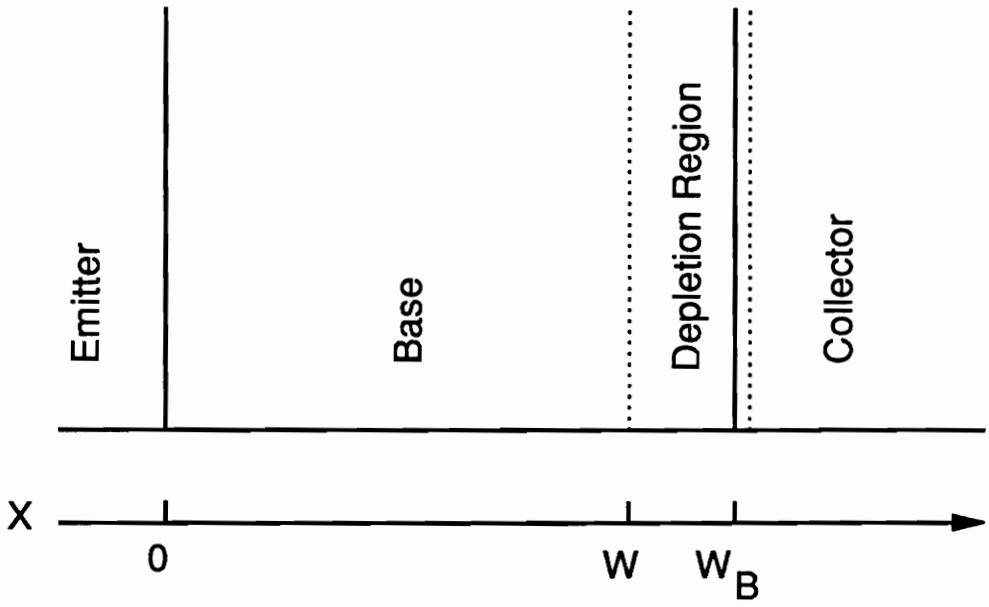

Figure 3.2. Coordinate representation for GBT model.

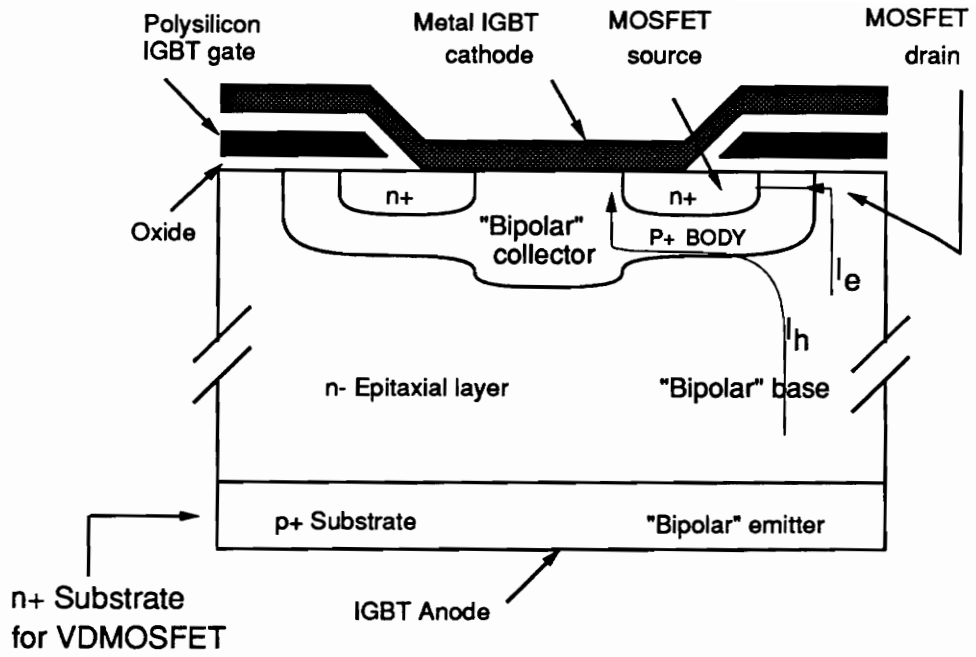

Figure 3.3. A Single n-channel IGBT cell.

3.3 IGBT Physical Model

Figure 3.4 shows the detailed IGBT equivalent circuit superimposed on one cell of an n-channel IGBT. In Fig. 3.4, the components connected between the emitter (e), base (b), and collector (c) nodes are associated with the bipolar transistor, and the components connected between the drain (d), gate, and source (s) nodes are associated with the VDMOSFET. As mentioned earlier, the structure of the IGBT is similar to that of the power VDMOSFET, with the exception that the n+ drain contact of the conventional MOSFET is replaced by the p^+ anode contact for the IGBT. Thus the MOSFET portion of the model behaves similarly to a VDMOSFET, with the exception that the lightly doped epitaxial layer of the IGBT is considered as the conductivity-modulated base resistance, R_b, of the bipolar transistor. In addition, the drain-source and the gate-drain depletion capacitances overlap with the base-collector depletion capacitance of the bipolar transistor, and hence this capacitance is only included in the MOSFET. The details of the equivalent circuit are discussed.

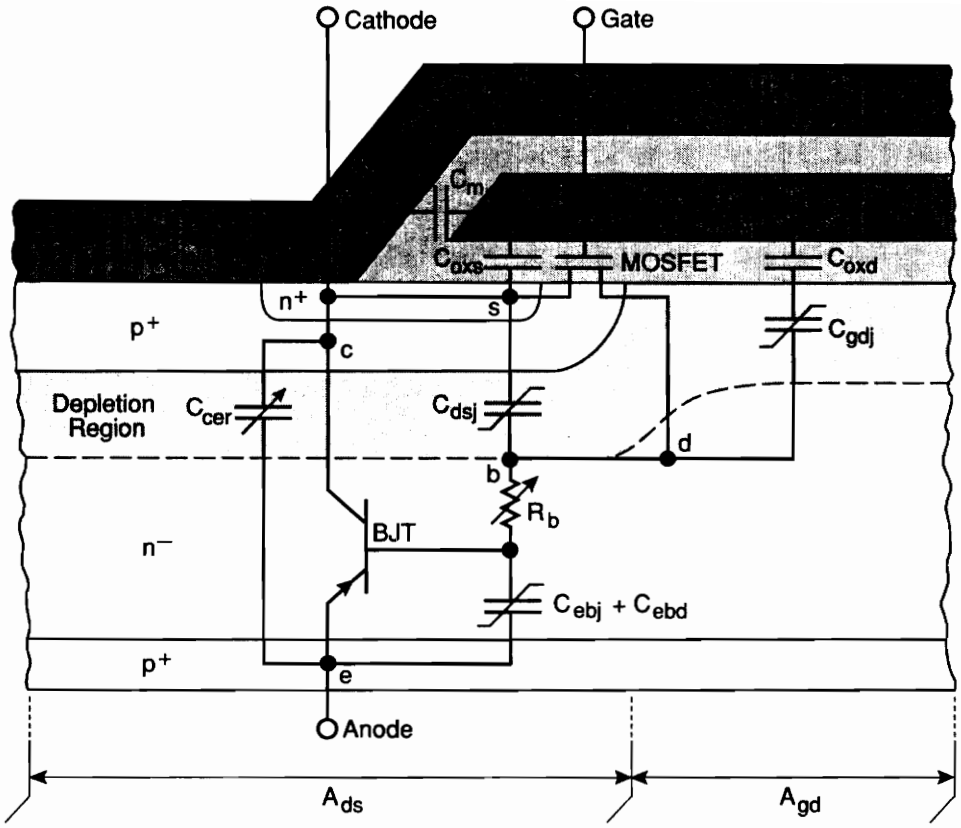

Figure 3.4. Detailed IGBT equivalent circuit components superimposed on a schematic of one cell of an n-channel IGBT.

3.3.1 VDMOSFET

The MOSFET componentsof the equivalent circuit are defined as follows:

C_{gs}	=	gate-source capacitance,
C_{oxs}	=	gate oxide capacitance of the source overlap,
C_m	=	source metallization capacitance,
C_{gd}	=	gate-drain feedback capacitance (Miller Capacitance),
C_{oxd}	=	gate-drain overlap oxide capacitance,
C_{gdj}	=	gate-drain overlap depletion capacitance, and
C_{dsj}	=	drain-source depletion capacitance,

where the MOSFET symbol represents the MOSFET channel current, I_{mos}. The VDMOSFET gate-source capacitance, C_{gs}, consists of the parallel combination of the gate oxide capacitance of the source overlap, C_{oxs}, and the source metallization capacitance, C_m. The VDMOSFET gate-drain feedback capacitance (or Miller capacitance) consists of the series combination of the gate-drain overlap oxide capacitance, C_{oxd}, and the gate-drain overlap depletion capacitance, C_{gdj}. The VDMOSFET drain-source capacitance, C_{dsj}, consists of the depletion capacitance of the drain-source junction. To describe IGBTs made with other MOSFET structures, only the components of Fig. 3.4 associated with the MOSFET portion of the device need to be changed.

3.3.2 Bipolar transistor

The bipolar transistor components of the equivalent circuit are defined as follows:

C_{cer}	=	collector-emitter redistribution capacitance,
R_b	=	conductivity-modulated base resistance,
C_{ebd}	=	emitter-base diffusion capacitance, and
C_{ebj}	=	emitter-base depletion capacitance,

where the BJT symbol represents the charge-controlled components of collector and base current. The collector-emitter redistribution capacitance, C_{cer}, is a result of the non-quasi-static behavior of the bipolar transistor base charge for the changing base-collector depletion width. This capacitance is orders of magnitude larger than the depletion capacitances and dominates the effective output capacitance of the IGBT during turn-off [1]. The bipolar transistor also contributes a conductivity-modulated base resistance, R_b, an emitter-base diffusion capacitance, C_{ebd}, and an emitter-base depletion capacitance, C_{ebj}.

3.4 Parameter Extraction

In the following section, the procedures for extracting the IGBT model parameters will be discussed briefly. Little has published on the extraction methods for the IGBT, and this is an on-going research process to determine the best and most efficient method. Therefore, the availability of information in IGBT parameter extraction is very limited.

(Extensive work has been done by Dr. Hefner in developing this IGBT model, and because of his expertise within the area of IGBT, the information for the procedures for parameter extraction will be from an article written by Hefner [4]. For further information concerning the IGBT model parameter extraction, it is advised that the reader refer to this article or contact Dr. Hefner at NIST.)

3.4.1 Parameter extraction algorithm

Table 3.1 and 3.2 show the list of device parameters that are needed for implementing analytical IGBT device model. The parameters in Table 3.2 are physical constants for the silicon at room temperature, and it is assumed that they don't change from device to device. Table 3.1 lists the parameters which need to be extracted. In Table 3.1 the nominal values are listed along with the required variables which are needed in order for any particular parameter to be extracted. The device active area is obtained by visual measurement of the device area [4], and to extract the other parameters, there are four types of measurements needed in order to obtain other parameters [4]. Below is the algorithm which need to be followed (the order of algorithm is essential due to the dependence of other parameters on the previous parameter measurement):

1. The turn-off current decay rate versus anode current is used to find the base lifetime, τ_{HL}.
2. The relative size of the turn-off current tail versus anode current and anode voltage is used to extract the emitter electron saturation current, I_{sne}, the metallurgical base width, W_B, and the base doping concentration, N_B.
3. The saturation current versus gate voltage is used to extract the MOSFET channel transconductance parameter, K_p, and the MOSFET channel threshold voltage, V_T.
4. The gate change and the gate-drain charge characteristics are used to extract the gate-source capacitance, the gate-drain overlap oxide capacitance, and the gate-drain overlap area.[1]

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1 A. R. Hefner, "Instant - IGBT Network simulation and Transient analysis Tool," NIST Special Publication Sp. 400-88, 1991.

Table 3.1. Device Parameters That Needs to be Extracted

A	$0.1\ cm^2$	Chip size
τ_{HL}	0.3 - 8.0 ms	Tail decay rate
I_{sne}	6.0×10^{-14} A	Tail size-vs-current
W_B	93 mm	Tail size-vs-V_A
N_B	$2 \times 10^{-14}\ cm^{-3}$	Tail size-vs-V_A
V_T	5.0 V	Saturation current-vs-V_{gs}
K_p	$0.36\ A/V^2$	Saturation current-vs-V_{gs}
C_{gs}	0.6 nF	Gate charge
C_{oxd}	1.6 nF	Gate charge
A_{gd}	$0.05\ cm^2$	Gate-drain charge

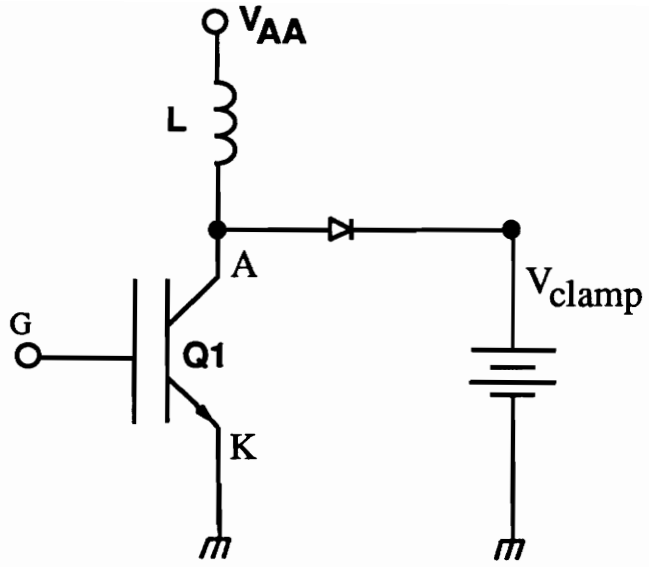
Table 3.2. Physical Constants of Si at T = 25^0 C

n_i	1.45×10^{10} cm^{-3}
μ_n	1500 $cm^2/V\text{-}s$
μ_p	450 $cm^2/V\text{-}s$
ϵ_{si}	1.05×10^{-12} F/cm
α_1	1.428×10^{20} $(cmVs)^{-1}$
α_2	4.54×10^{11} cm^{-2}
ν_{nsat}	1.1×10^7 cm/s
ν_{psat}	0.95×10^7 cm/s

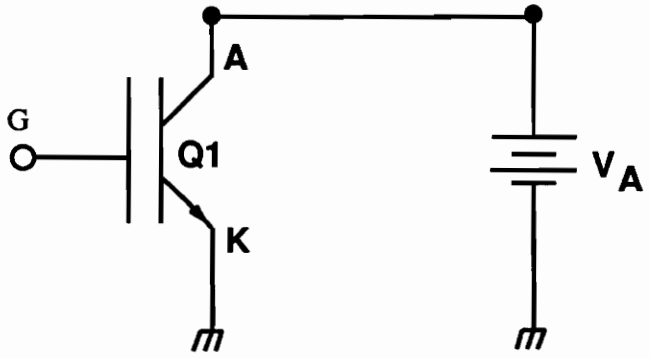
3.4.2 BJT parameters

Figure 3.5 shows circuits used to measure the base lifetime of the IGBT device. The measurement of current decay rate can be accomplished by the use of the clamped inductive test circuit (Fig. 3.5a) or constant anode voltage test circuit (Fig. 3.5b). The inductive load test circuit is better suited for the measurement of the small base lifetime because it gives a larger current tail. Figure 3.6 shows the desired waveforms for the current decay, $I_T(t)$. It is observed that the collector current initially falls rapidly and then tails off. This rapid current fall was assumed to be due to the injection of electrons from the drift region into the p+ substrate [4]. Another explanation for this phenomenon is due to the removal of gate voltage at the gate. When the gate voltage is brought to zero during the device turn-off, the electron current that was flowing through the inverted channel is abruptly shut off. The rest of the decay of the collector current is then assumed to be due to the recombination of the stored minority carriers in the n-base.

When setting up the circuits to measure the base lifetime, great care must be taken so that parasitics within the circuit are minimized as much as possible. If the inductive circuit is used, the inductor need to be a large value (1-mH), and the series diode with the clamp voltage need to be of very fast recovery type. Also the clamp voltage needs to be very 'stiff' (no variation in its voltage value). Usually a by-pass capacitor is used to reduce the effect of inductance due to the source lead. When this method is applied, a method of paralleling several different values of by-pass capacitances is suggested to reduce the possibility of oscillation with the load inductance. The circuit is needed to be adjusted time-to-time as to obtain the collector curve resembling the one shown in Fig. 3.6.



(a)



(b)

Figure 3.5. Circuit configurations for (a) clamped large inductive load, and (b) the constant anode supply voltage [4].

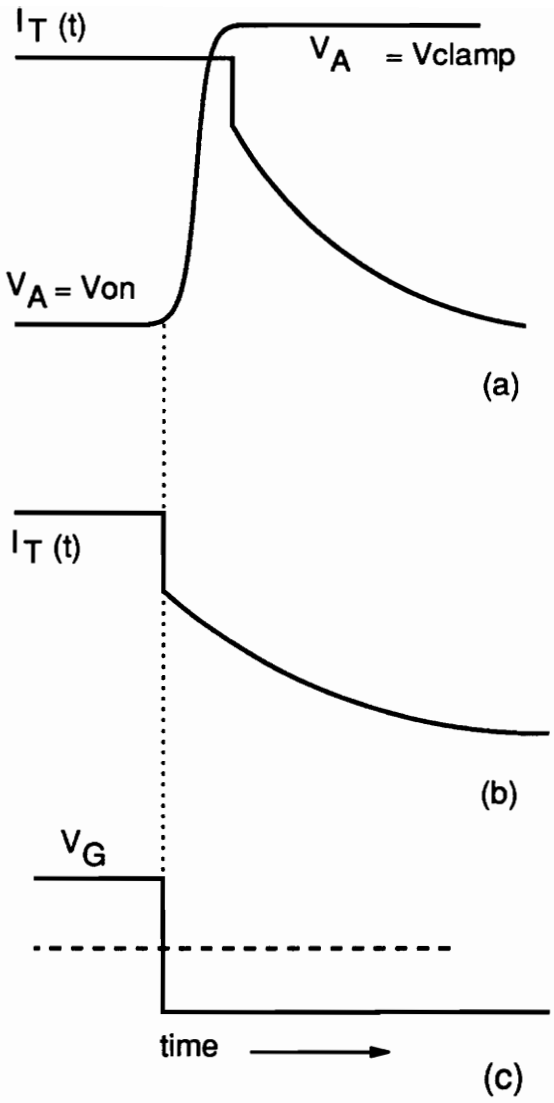


Figure 3.6. Example of turn-off switching waveforms for (a) clamped large inductive load, and (b) the constant anode supply voltage [4].

It was shown in [6] that the decay rate of the slowly decaying portion of the collector current was :

$$\frac{d\ln I_T}{dt} = \frac{dI_T}{dt} / I_T = -\frac{1}{\tau_{HL}}\left(1 + \frac{I_T}{I_k^{\tau}}\right), \tag{3.1}$$

where

$$I_{sne} \equiv \frac{q^2 A^2 D_p n_i^2}{I_k^{\tau} \tau_{HL}}. \tag{3.2}$$

The current decay time constants are then obtained by taking the time derivative of the log of the current waveform. It is advised that the measurements be taken at several different initial currents, while constantly calibrating the scales of the equipment measuring the collector current. Figure 3.7 shows the plotted data of measured current decay time constant versus instantaneous tail current for devices with different base lifetimes. Once the graph is plotted, the peaking of the plotted graph should be observed. This peak value is chosen as the base lifetime of the device. Equation (3.2) can be used to extract the emitter saturation current.

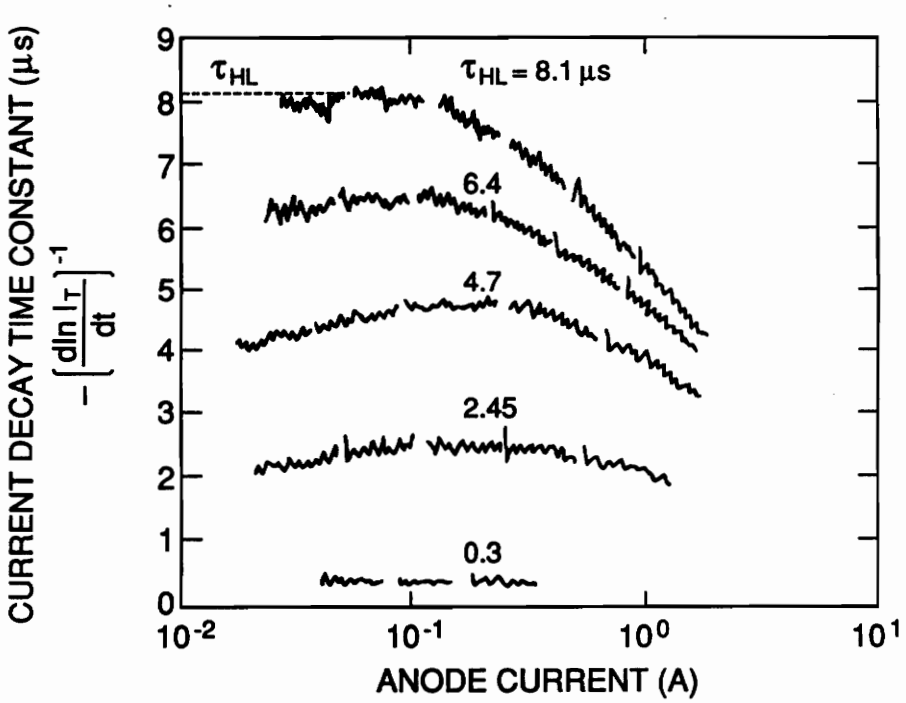


Figure 3.7. Experimental values of the current decay time constant versus current [4].

Figure 3.8a shows the turn-off current waveform for the constant anode voltage circuit. The current initially falls abruptly and then slowly decays. It was shown in [6] that the current decay requires a finite time for the excess carriers to assume a distribution that can be described by a simple model. But the current waveform can be extrapolated past the redistribution state of the current waveform (see Fig. 3.8b) to acquire the expression describing the relative size of the extrapolated current tail for constant anode supply voltage switching by:

$$\beta_{tr,v} = \beta_{tr,v}^{max}\left(1+\frac{I_T(0^+)}{I_k}\right)^{-1}, \tag{3.3}$$

where

$$\beta_{tr,v}^{max} = \left(\left(\frac{W}{2L}\right)^2 \frac{\coth\left(\frac{W}{L}\right)}{2\tanh\left(\frac{W}{2L}\right)} - 1\right)^{-1}, \tag{3.4}$$

and

$$I_{sne} = \frac{\tanh^2\left(\frac{W}{2L}\right)}{\left(\frac{W}{L}\right)^4}\left(\frac{(4qn_iAD_p)^2}{L^2\left(1+\frac{1}{b}\right)}\right)\cdot\frac{1}{\beta_{tr,v}^{max}I_k}. \tag{3.5}$$

The measured values of the extrapolated relative current tail size for constant anode voltage is shown in Fig. 3.9a. Figure 3.9b shows the measured values with a expected slope of $1/(\beta_{tr,v}^{max} I_k)$ and with a zero current intercept of $1/\beta_{tr,v}^{max}$. The solid line is fitted by using the least squares method. The slope of the least squares is then used with eq. (3.5) to obtain the parameter , and the zero intercept is used to extract the value of W at the given anode voltage, where the expression for W is given by [6];

$$W \approx W_B - \sqrt{2 \epsilon_{si} V_A / q N_B}, \tag{3.6}$$

then the appropriate equations which describe the W versus square root of anode voltage can be used to extract the values W_B and N_B.

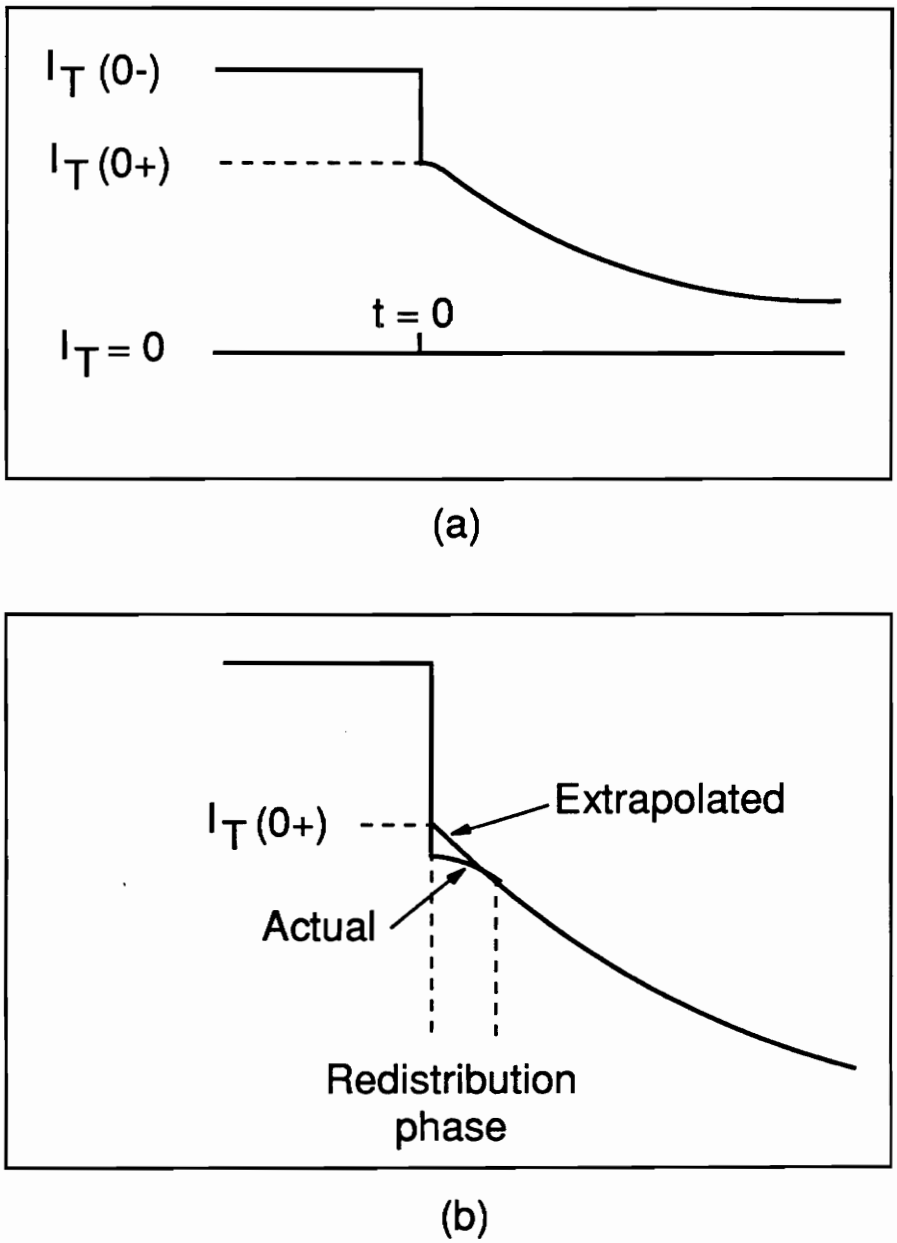
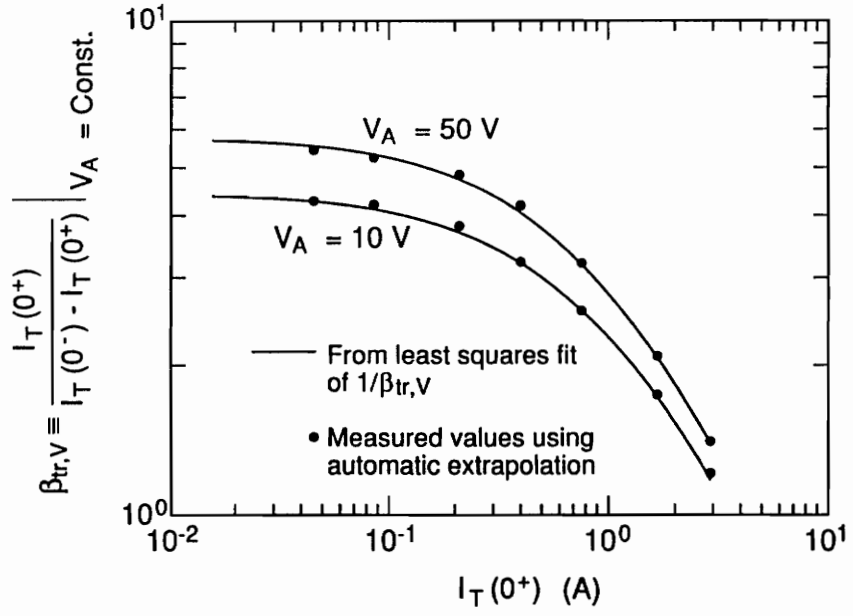
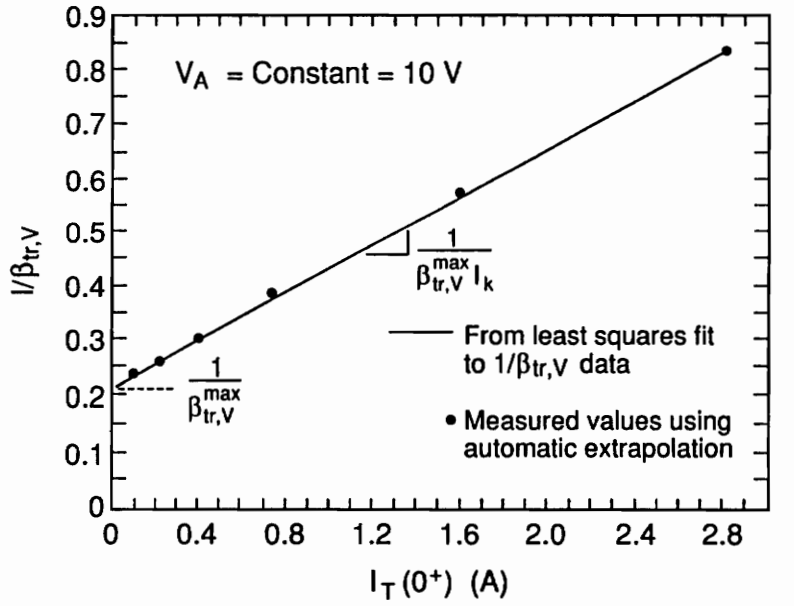


Figure 3.8. (a) Constant anode voltage turn-off current waveform indicating the current before and after the initial rapid current fall. (b) A diagram of the redistribuition phase on an expanded scale, showing the extrapolated valueof $I_T(0+)$ [4].



(a)



(b)

Figure 3.9. (a) Measured values of the relative size of the extrapolated current decay tail $1/\beta_{tr,v}$ versus current. (b) measured values and linear least-square fit for $1/\beta_{tr.v}$ versus $I_T(0+)$ [4].

3.4.3 MOSFET parameters

Figure 3.10 shows the transfer curve of the MOSFET portion of the IGBT device. The flat portion is the saturation region, and the linear region is the high resistance region. Because the MOSFET drives the bipolar PNP transistor, the current gain at the saturation region of the MOSFET is magnified by the PNP transistor, and this current gain for the steady-state common collector configuration is expressed as $(1 + \beta_{ss})$. Therefore, the saturation current characteristics can be found by dividing IGBT saturation current by the steady-state common collector current gain of the bipolar transistor:

$$I_T^{sat} = I_T^{sat} / (1+\beta_{ss}). \tag{3.7}$$

Figure 3.11a shows the bipolar common collector current gain versus the collector current which was previously measured in order to find the base lifetime of the device.

It was discussed in [6] that for the MOSFET channel current, the square root of the saturation current is linearly related to the gate voltage with a zero current intercept, V_T, with the a slope of $\sqrt{K_p / 2}$, and is expressed as:

$$\sqrt{I_{mos}^{sat}} = \sqrt{K_p / 2}(V_{gs} - V_T). \tag{3.8}$$

Figure 3.11b shows the plot of square root of the MOSFET current versus gate-source voltage which was obtained by dividing the IGBT saturation current by the common collector current gain. From this plot the parameters values of K_p and V_T are extracted.

To examine the MOSFET charging characteristics of the IGBT, the circuit is used so that the current flowing across the device very low, and the constant current is applied at the gate. This low anode current across the device is desirable because charge Q in the base of the bipolar portion of the device can be assumed to be zero. As a result, the waveforms obtained can be assumed to be the switching characteristics of the MOSFET portion of the device. Figure 3.12 shows the charging characteristics of the IGBT at a low anode current and for a constant gate current at approximately 20 mA. As shown in this figure, there are three phases associated with the charging characteristics of the IGBT device. During the first phase, V_{gs} rises with a constant linear slope because the constant gate current is charging the constant C_{gs} of the device. Therefore, the gate-source capacitance C_{gs}, is extracted at this constant slope region of phase 1 by dividing the gate current waveform by the time-rate-of change of the gate voltage. During the second phase, the V_{gs} remains virtually constant, as V_A falls the constant gate current is charging the gate-drain feedback capacitance C_{gd}. Therefore, the voltage dependant gate-to-drain capacitance can be extracted by dividing the constant gate current wave form by the time-rate-of-change of gate-to-anode voltage. The gate-to-drain voltage dependent capacitance is expressed as [6]:

$$C_{gdj} = \frac{A_{gdj} \epsilon_{si}}{\sqrt{2 \epsilon_{si} (V_A - 0.6 - V_{gs} + V_{Td} / qN_B}}. \tag{3.9}$$

Using the measured values of the C_{gdj} for high anode voltages, the parameters A_{gd}, and $(1/C_{gsj}^2)$ versus V_A - V_{gs} can be used to extract V_{Td}. During the third phase, V_A remains relatively constant, and the V_{gs} rises with a different slope as the constant gate current is charging the sum of the gate-drain overlap oxide capacitance C_{oxd}, and the C_{gs}. The value of C_{oxd} is extracted by subtracting the value of input capacitance during the first phase from that of during third phase.

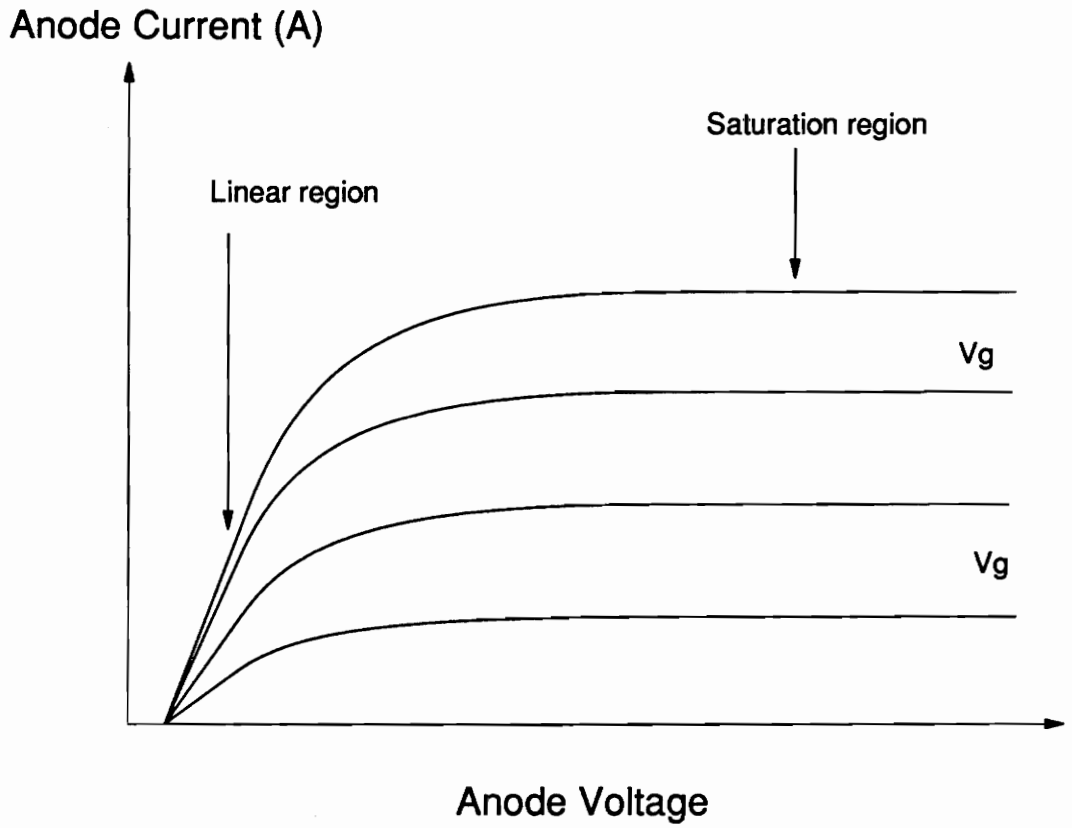
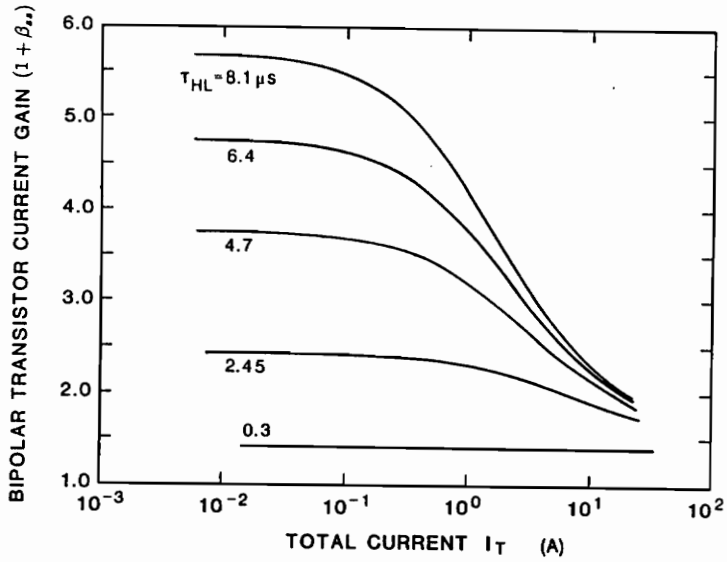
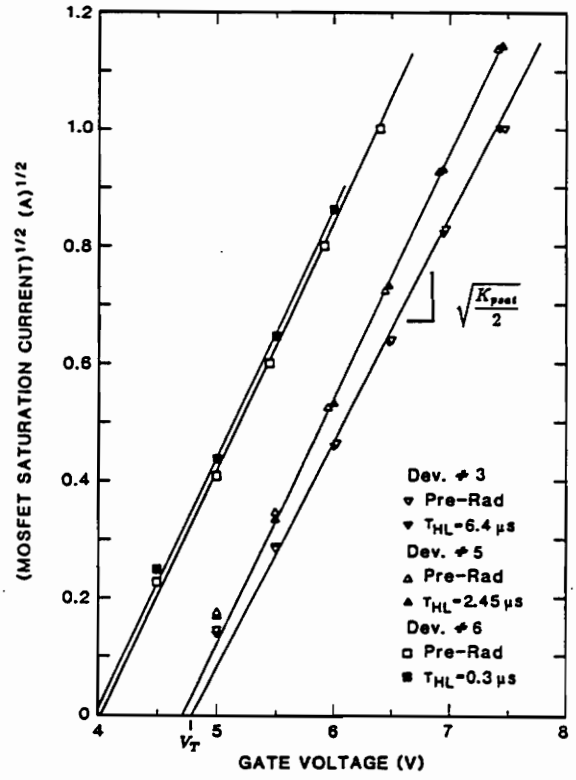


Figure 3.10. DC Transfer curve for IGBT indicating the saturation and linear region.



(a)



(b)

Figure 3.11. (a) Steady state common collector current gain versus anode current for bipolar of IGBTs with different base lifetime. (b) The square root of the MOSFET saturation current indicating the slope that is used to extract K_P and the zero currentintercept is used to extract V_T [4].

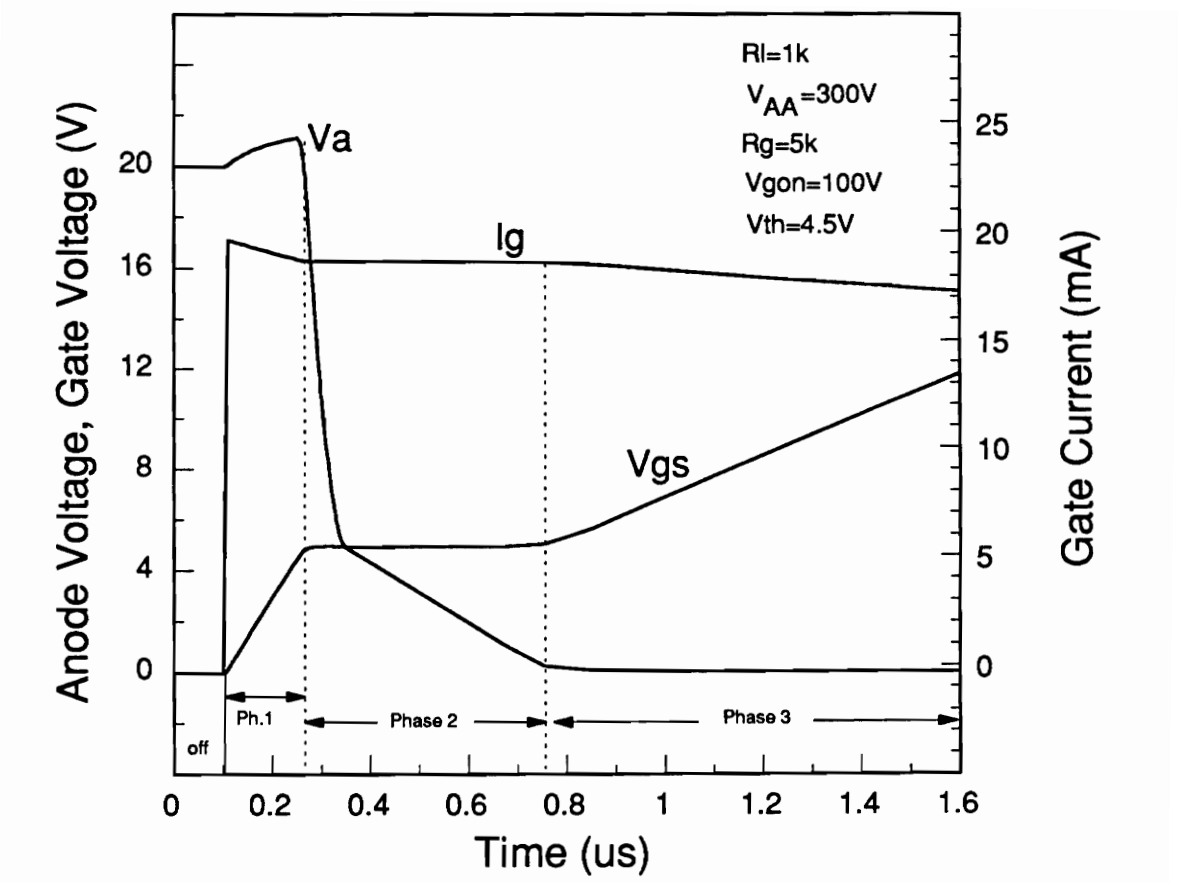


Figure 3.12. Measured gate and gate-drain charging characteristics for a low anode current and relatively constant gate current pulse (approximately 20 mA) [4].

3.5 Summary

The IGBT is a new power semiconductor device which possesses the best features of both the MOSFET and bipolar transistor. Due to its wide base low-doped region of the bipolar, the ambipolar equation must be used to describe the carrier concentration in the n- epitaxial layer.

It was shown that following characteristics of the proposed models are very important in correctly predicting the high level injection mode of wide base PNP transistor: 1) the base contact is at the collector edge, 2) the base current enters the collector edge first, 3) the sum of the electron and hole current make up total current which is constant throughout the base, and 4) because total current is constant throughout the base of the bipolar structure, this bipolar can be characterized by the one-dimensional ambipolar transport equations.

When extracting the required parameters for the IGBT physical model the steps presented for the algorithm must be done in correct sequence:

1. The turn-off current decay rate versus anode current is used to find the base lifetime, τ_{HL}.
2. The relative size of the turn-off current tail versus anode current and anode voltage is used to extract the emitter electron saturation current I_{sne}, the metallurgical base width W_B, and the base doping concentration N_B.
3. The saturation current versus gate voltage is used to extract the MOSFET channel transconductance parameter K_p and the MOSFET channel threshold voltage V_T.
4. The gate change and the gate-drain charge characteristics are used to extract the gate-sourcecapacitance, the gate-drain overlap oxide capacitance, and the gate-drain overlap area.

When setting up the test circuits for the parameter extraction, it is essential that the parasitic elements are reduced to its minimum values. Also, the measuring equipments should be constantly calibrated to ensure order that the measured values are correct. As discussed before, the accuracy of the model is only as good as the accuracy of the parameters that are provided by the user.

Chapter 4

THE IG-Spice

4.1 Introduction

Spice users often encounter difficulty analyzing a circuit which contain a device which the Spice cannot accurately model. This shortcoming is overcome by the use of the extensive modelling capabilities of IG-Spice. IG-Spice users have the ability to model any kind of semiconductor devices, or circuit functions.

In this chapter, the IG-Spice simulation program is reviewed. The requirements for implementing model equations into IG-Spice, and the procedures used to implement the general semiconductor model into IG-SPICE, are described.

4.2 Implementing General Device Models into IG-SPICE

SPICE users are constantly faced with the inability to analyze circuits that contain devices that are not well described by the SPICE semiconductor models. This can be overcome by the use of the programming capabilities of IG-SPICE. The IG-SPICE simulation program is an extended version of the SPICE-2 computer-aided design and analysis program. IG-SPICE is designed to be more graphics-oriented and provides the user with programming capability. This programming capability of IG-SPICE enables the user to implement general device models without having to add additional components such as diodes or transistors to emulate the device model equations. The ability to directly implement model equations as IG-SPICE controlled sources results in more computationally efficient simulations without the problems associated with convergence.

4.2.1 IG-SPICE user defined device models

When implementing model equations into the IG-SPICE user-defined model subroutine, the following formalities need to be considered in detail:

1. The model must be formulated as an interconnection of controlled current and voltage sources which depend upon controlling currents or voltages, but not both currents and voltages.
2. The variables must be normalized so that each variable that is solved for by the simulator has a comparable absolute error tolerance.
3. The independent variables must be converted into the current and voltage types.
4. In general, the partial derivatives of the expressions for the controlled sources with respect to the controlling variables must be evaluated.

The programming capability of IG-SPICE is made possible by the use of dependent controlled sources where the equations describing the controlled sources are implemented using the user-defined model subroutine. There are four types of controlled sources in the IG-SPICE simulation program:

Voltage-Controlled Current Source	(VCCS),
Voltage-Controlled Voltage Sources	(VCVS),
Current-Controlled Current Sources	(CCCS), and
Current-Controlled Voltage Sources	(CCVS).

In implementing these controlled sources into the user-defined model subroutine, the user must follow a particular format in order for the data to be passed properly between the IG-SPICE input file (which provides a list of voltages or currents and a list of constant model parameters) and the user-defined model subroutine (which computes the actual output voltage or current values based on the input lists). IG-SPICE requires that the inputs of the controlling variables be of only one source type: either all voltage or all current. Therefore, in the cases where the output is dependent upon both current and voltage type variables, the controlling variables of one of the types must be transformed into the other type.

4.2.2 IG-SPICE controlled sources

The IG-SPICE controlled sources are realized using the polynomial controlled sources of SPICE, which depend upon controlling variables. For example, the general input format for a voltage-controlled current source in all SPICE programs is as follows:

```
Gxxx <NS+>  <NS->  Poly(<ND>)        (<NC1+>, <NC1->)
        (<NC2+>, <NC2->) . . . <P0, P1, . . .> ,
```

where <NS+> and <NS-> are the output connection nodes of the controlled source, Poly(<ND>) specifies the dimension of the polynomial as ND, and P0, P1 . . . are the polynomial coefficients. For the voltage-controlled sources, the nodes <NCi+> and <NCi-> specify the positive and negative connections of the controlling voltage. For the current-controlled sources, the controlling voltage pair is replaced by the name of the null voltage source <VSx> which is specified as a current probe. The current probe statements have the form: VSx <NS+>, <NS-> 0Probe, where the nodes <NS+>, and <NS-> are introduced in the controlling current branch and have zero voltage between them.

However, when the programming capability of IG-SPICE is utilized to implement a general model expression, the polynomial coefficient values are not used in the input field. Instead, the program function name followed by the sequence of data are specified. This data is passed to the user-defined model subroutine to determine the values of the polynomial coefficients.

An example of the input field utilizing the programming capability of IG-SPICE is:

```
GImos  7 60 POLY(2) (30,60) (2, 60) Imos(Vt = 5.0).
```

GImos is the name of the voltage-controlled current source (VCCS) in which the current enters through positive node 7 and exits through negative node 60. POLY(2) specifies that the dimension of the number of controlling voltages is 2, where the node pairs (30,60) and (2,60) specify the controlling voltages. Imos is the name of the output function within the user-defined model subroutine, and Vt is an example of a data value which is passed to the function Imos.

4.2.3 Implementing partial derivatives of model functions

In addition to evaluating the source function, the user-defined model subroutine must also evaluate the partial derivative of the source functions with respect to each of the controlling variables. These partial derivatives are required by the numerical algorithms of the SPICE-based simulators to facilitate convergence. To describe the procedure for implementing the partial derivatives into the model subroutines, let the variable Y be an output (dependent source function), and let X1, X2, . . . Xn be the input variables (controlling sources). The source functions then take the form:

$$Y = F(X1, X2, \ldots Xn), \tag{4.1}$$

where F is the model equation that must be implemented to describe the controlled source.

In general, IG-SPICE controlled source functions must be expressed in the form of a polynomial expression:

$$Y = Co + C1*X1 + C2*X2 + \ldots . \tag{4.2}$$

The advantage of the IG-SPICE user-defined controlled sources is that the coefficients need not be constants, so that general expressions for the source functions containing conditional commands can be implemented. In IG-SPICE user-defined controlled sources, the coefficients of the polynomial expression represent the partial derivatives of the output source function with respect to the input controlling variables:

$$C_1 = \frac{\partial Y}{\partial X_1}, \quad C_2 = \frac{\partial Y}{\partial X_2}, \ldots\ldots C_n = \frac{\partial Y}{\partial X_n}. \tag{4.3}$$

The variable Co is then calculated as follows:

$$Co = Y - C1*X1 - C2*X2 - \ldots Cn*Xn, \tag{4.4}$$

so that the sum of the terms of the polynomial eq. (2) will be equal to the source function Y. The values of the bias-dependent coefficients calculated in the user-defined controlled source function are returned to the IG-SPICE controlled source, which is then interpreted just as the generic SPICE polynomial controlled source function.

4.2.4 Implementing time derivatives of controlling variables

Another very important feature of the IG-SPICE program is the ability to save the state of the system variables between time steps during the transient analysis. The values of the previous state can be retrieved within the user-defined model subroutine to implement complicated state equations which require the time rate-of-change of the controlling variable. Basically, the time rate-of-change of a controlling current or voltage is calculated in a differential manner, using the variable at the previous time step:

$$\frac{dV}{dt} = \frac{(V - V')}{\Delta t}, \tag{4.5}$$

where V' is the value of the variable V at the previous time step, and Δt is the time-step size.

4.3 IG-Spice Subroutines

Within IG-Spice, all of the user-defined subprograms are defined in a single subroutine called FORTFN. This subroutine is passed an index number based on the function name entered in the input listings. By default, the names F1 through F8 pass indices of 1 through 8 to subroutine FORTFN, or the user can specify the names that describe the controlled source which the are to be used for the subprograms with the FNNAME function.

4.3.1 Function FNNAME

In order to redefine the names of the user functions from the default names of F1 through F8, the functions subroutine FNNAME is used. An example of its format is shown below:

```
FUNCTION FNNAME(JFN)
REAL*8 FNNAME,NAMES(9)
DATA NAMES /'IMOS','IGD','IDS','IQ','IA','IB','IC','VEB','*END*'/
FNNAME=NAMES(JFN)
RETURN
END
```

This routine simply takes the integer value passed to it and returns the name that should be associated with that index in the FORTFN subroutine. For this particular case shown here, the names will be IMOS for index of 1, followed by IGD, IDS, IQ, IA, IB, IC, and VEB for indices 2 through 8. The name "*END*" must follow the last function name to indicate the end of the list of names. Also in the array NAMES, the number must be one greater than the total number of function names the user specified.

4.3.2 Subroutine FORTFN

Within IG-Spice, all of the user-defined FORTRAN subprogram is contained in this subroutine. If the user wishes to create a new subprogram, the user should specify its name using the function FNNAME, then append the subprogram to this one and make the appropriate branching changes. The subroutine should begin similar as the one shown below:

```
SUBROUTINE FORTFN(JFN,DATA,NDAT,ARG,NARG,COEF,TIME,VNAME,IPTR)
      IMPLICIT REAL*8(A-H,O-Z)
DIMENSION DATA(25),ARG(8),COEF(8)
COMMON /IGBTpar/ t,Wb,Nb,A,Isne,Vt,Kp,Cgs,Agd,Coxd,ccsflg,
&                sclflg,Vtd,Vnsat,Vpsat,Ut,ni,Un,Up,q,esi,Bvn,
&                Bvf,Vcb,Qt

GOTO(100, 200, 300, 400, 500, 600, 700, 800),JFN.
```

The subprogram begins at line 100, and the rest of the user subprograms would start on lines as specified (i.e., 200, 300. 400, 500,. . . , and 800).

Following are the definitions describing essential arguments and arrays which need to be specified when using the subroutine FORTFN:

JFN: Index to the actual subprogram (function) being called and its first executable statement is GOTO which will branch to various parts of the subroutine based on the value of JFN. Here, the indices 1 to 8 will cause branching to lines 100 through 800.

DATA: The data vector, the specified number determined how many user-specified ` constant can be used for particular function being executed.

NDAT: The number of data constants specified by the user.

ARG: The input argument vector. These are the controlling voltages or currents.

NARG: Number of controlling voltages or currents.

COEF: The vector function coefficients(Co, C1,...,Cn) for the ARG vector. This vector is used to return the value of the output back to the dependent source that had called this function. The values placed into the COEF array by this function will be used as the "polynomial dependent source" linear coefficients. The actual value of the output will becomputed using the equation;

$$\text{Output} = COEF(1) + ARG(1)*COEF(2) + ARG(2)*COEF(3) + \ldots + ARG(NARG)*COEF(NARG+1)$$

TIME: Current simulation time which is set by IG-Spice each time the routine is executed

VNAME: Name of the dependent source using the specified FORTRAN function.

As an simple example, consider the input listing which has function call as follows:

```
GImos  7 60 POLY(2) (30,60) (2, 60) Imos(Vt = 5.0).
```

During both the operating point calculation and each iteration of the transient analysis, this function specifications will cause a call to the FORTFN routine, and the following values will be passed:

JFN = 1,
NDAT = 1,
DATA(1) = 5.0,
NARG = 2,
ARG(1) = voltage at nodes(30,60),
ARG(2) = voltage at nodes(2, 60),
TIME = simulations time for this particular iteration, and
VNAME = "GIMOS".

The first argument of the subroutine, JFN, is the index to the actual subprogram being called, and the first executable statement is the GOTO which will branch to various parts of this subroutine based on the value of JFN (here , the indices 1 to 8 will cause branching to lines 100 through 800, assuming that the user has defined eight separate subprograms using this routine). The arrays DATA and ARG are the lists of constant data and input voltages/currents that were passed from the call in the IG-Spice input listings, and the integers NDAT and NARG are the number of data constants and input arguments that were specified for the call.

4.4 State Dependent Subprogram

All of the functions we have discussed were such that the output value was computed from the inputs and the parameter values specified. Often, functions cannot be described in terms just the inputs at the current timepoint, but rather require information that has been saved from the previous timesteps so that the output can be computed using these values. This use of past information is essential, and is the most important feature of the IG-Spice which allow us to implement the IGBT model into IG-Spice. Without this feature, the modeling of nonlinear characteristics of the IGBT device is not possible.

4.4.1 State subroutines

The IG-Spice provides the user with internal subroutines , named "GSTATE" and "RSTATE", in order to create state dependent subroutines [8]. The two subroutines are used to GET a STATE (to setup a state register) and RESET a STATE (update the value of the register. The format required to do this uses the parameter IPTR (which is one of the FORTFN subroutine variable list). Every dependent source in a circuit has its own IPTR register, and that register is passed to the FORTFN function each time it is called. Before the initial pass through the simulation, IPTR value of every dependent source is set to zero. Inside the FORTFN, the value of IPTR can be tested to see if its zero, and if zero, the initialization procedure begins.

When GSTATE routine is called, the IPTR value is passed. GSTATE then assigns a location in the internal STATE array for the variable that is being initialized, and return the reference index to it as an integer in IPTR. Whenever the user wishes to change the value of that state, RSTATE is

called and pass the IPTR value so that it knows where the variable to be changed is located.

In order to be able to use these two subroutines, the STATE array must be included in the common block of the FORTFN routine. The common block should look as following:

```
COMMON /STATES/ TOLD, TOLD2, ODT, STATE(500), STATE2(500), NSTATE.
```

The variables are defined as follows:

TOLD	= Simulations time at previous timestep
TOLD2	= Simulation time at 2nd previous step
ODT	= 1/(TIME - TOLD), or = 0 at DC
STATE(1..500)	= Array of state (can be changed by RSTATE)
STATE2(1..500)	= Permanent copy of states at last timestep
NSTATE	= Number of states currently allocated

4.4.2 Format for GSTATE/RSTATE calls

Following syntax is used to call the GSTATE and RSTATE subroutines:

```
CALL  GSTATE (initvalue, 1, IPTR)      or
CALL  GSTATE(initarray, n , IPTR)
CALL RSTATE(newvalue, 1, IPTR)         or
CALL RSTATE(newarray, n, IPTR)
```

where, "n" = number of states to initialize;
"initvalue" = value to initialize state to;
"initarray" = array of values for initialization;
"newvalue" = value to change existing state to;
"newarray" = array of values to reset states to.

In order to access the value that is stored in a particular location, the data is read directly out of the STATE array with an offset of IPTR. IF only a single state is defined, it is accessed as,

Oldvalue = STATE(IPTR+i),

while, if "n" states were defined, they can be accessed as,

Oldvalue(i) = STATE(IPTR+1) for i = 1 to n.

4.4.3 State subroutine example

For a clear understanding, here is a description of some capacitance values. Assume that C_{ds} represents the drain-source capacitance of a MOSFET. In order to simulate this non-linear capacitance, represent it as a voltage-controlled-current source. (This is due to limitations of IG-Spice program, as discussed earlier.) The current through this capacitance can be represented as:

$$I_{ds} = C \cdot \frac{dV_{ds}}{dt}. \tag{4.6}$$

This equation can be written in the form:

$$I_{ds} = C \cdot (V_{ds} - V_{dso}) \cdot ODT. \tag{4.7}$$

where

$$dV_{ds} = (V_{ds} - V_{dso}), \tag{4.8}$$

and

$$ODT = (Time - Told). \tag{4.9}$$

Since Vds is the controlling variable, it is declared a state variable. Now we can take the partial of Ids with respect to Vds:

$$\frac{\partial I_{ds}}{\partial V_{ds}} = C \cdot ODT = C_1 = Coef(2), \tag{4.10}$$

and

$$Coef(1) = Co = I_{ds} - Coef(2) \cdot V_{ds} = -C \cdot V_{dso} \cdot ODT. \tag{4.11}$$

The subroutine can be defined by the function name IDS:

```
GIDS 2 3 POLY(1) (5, 4) IDS.
```

The following subprogram can be written from the previous derivations:

```
If (IPTR .eq. 0.0) Call Gstate(Arg(1), 1, IPTR)
        Vdso = State(IPTR+1)
        Call RSTATE(ARG(1), 1, IPTR)
        Coef(1) = -C*Vds*ODT
        Coef(2) = C*ODT
Return
```

The first line of the program checks to see if the pointer is zero, and then it initializes the register for state variable Vds. Then the old value of Vds, is achieved and the state variable Vds is reset.

4.5 Summary

The IG-Spice graphics simulation program is an extended version of Spice-2 computer aided design and analysis program. It is designed to be more graphics-oriented and provide the user with FORTRAN programming capabilities. Employing this programming capabilities, almost any semiconductor device models and complicated circuit analysis can be accomplished without adding any additional branches in the circuit model, or without having to add addition Spice models to emulate the device characteristics. This results in less simulation time and better convergence. It was shown that when implementing the model within the Spice base programs, the following needed to be considered:

1. The model must be formulated as an interconnection of controlled current and voltage sources which depend upon controlling currents or voltages, but not both currents and voltages.

2. The variables must be normalized so that each variable solved for by the simulator has a comparable absolute error tolerance.

3. The independent variables must be converted into the current and voltage types.

4. In general, the partial derivatives of the expressions for the controlled sources with respect to the controlling variables must be evaluated.

Also when writing subroutine function in the IG-Spice, the partial derivatives of the expressions needed to be found in order to put it into polynomial form. The IG-Spice simulation program also allows the user to implement the state dependent equations with the use of internal subroutines STATE and RSTATE.

Chapter 5

IMPLEMENTATION of IGBT MODEL USING IG-Spice

5.1 Introduction

A physics-based model is desired in predicting the behavior of the IGBT. However, by using the analytical model, many complicated equations must be implemented in order that the model accurately describes the physical behavior of the device. It was shown in the previous chapter that the IG-Spice simulation program allows the user to implement complicated equations by means of using the supplied subprogram, which describes the desired functions.

In this chapter, the detailed implementation of these complicated equations are described. The techniques used to ensure convergence of the IG-Spice model, and the applicability of these techniques to other power semiconductor devices, are also reviewed. This technique is also applicable to other SPICE-based simulators, because all SPICE-based programs use the same numerical algorithms. The simulated results are verified experimentally with the measured values for the paralleled operation of the device.

5.2 IGBT Model Equations

The analytical IGBT model described in Chapter 3 is summarized in Tables 1 and 2. These equations are simplified expressions representing the functions of the equivalent circuit as shown in Fig. 5.1. The circuit in Fig. 5.2 is an IG-SPICE IGBT equivalent circuit representation of Hefner's IGBT analytical model. Figure 5.2 shows the interconnection of the various controlled sources required to implement the equations in Tables 1 and 2. The model is implemented using various controlled sources that there are dependent on node voltages or branch currents (but not both the currents and voltages) as required by IG-SPICE.

5.2.1 State equations/system variables

State equations for the analytical IGBT model are given in Table 5.3. There are five system variables which describe the IGBT model: base-emitter voltage, gate-source voltage, base charge, gate current, and the total device current, I_T. These state equations are dependent on the instantaneous values of the variables given in Table 5.4, and are also dependent on the external circuit parameters, I_T and I_g. These external current variables are dependent upon the external circuit configurations. Because the state equations are dependent upon the given system variables, dynamic circuit interaction is obtainable. The IG-Spice circuit simulation program will give the initial conditions for the system variables, V_{gs}, V_{bc}, Q, I_T, and I_g. As a result, some of the complicated equations can be simplified when implementing it into the IG-Spice.

State equation (dV_{gs} /dt) describes the time rate of change in the gate-to-source voltage and is dependent upon the junction capacitances and the base-collector voltage of the PNP bipolar. From the equivalent physical model, it is seen that the base-collector junction is the same as the drain-source junction of the VDMOSFET. The state equation (dV_{bc} /dt) describes the drain-source voltage which depend upon the current, charge, and nonlinear junction capacitances of the device. In turn, the state equation (dQ/dt) describes the base charge of the PNP transistor of the IGBT device. In order for the IG-Spice circuit simulator to correctly define these time-rate-of-change of the state variables, only the equations describing the currents, nonlinear junction capacitances, along with the charge Q, need to be described by the dependent polynomial functions (the procedures describing the base charge will be discussed later). The capacitances can be described by the dependent current sources.

The simplified representation of IGBT equivalent circuit is shown in Fig. 5.3. Note that the time rate of voltages are assumed to be given by the IG-Spice program, and only the nodes which describe the currents and capacitances at the appropriate branches need to be specified within the IG-Spice IGBT equivalent circuit.

Table 5.1. VDMOSFET Characteristics of IGBT Model.

$$\text{Imos} = \begin{cases} 0 & \text{for} \quad V_{gs} < V_T \\ \dfrac{K_{plin}\left[(V_{gs}-V_T)V_{ds} - \dfrac{K_{plin}V_{ds}^2}{2K_{psat}}\right]}{\left[1+\theta(V_{gs}-V_T)\right]} & \text{for} \quad V_{ds} \le (V_{gs} - V_T)\dfrac{K_{plin}}{K_{psat}} \\ \dfrac{K_{psat}(V_{gs}-V_T)^2}{2\left[1+\theta(V_{gs}-V_T)\right]} & \text{for} \quad V_{ds} > (V_{gs} - V_T)\dfrac{K_{plin}}{K_{psat}} \end{cases}$$

$$C_{gd} = \begin{cases} C_{oxd} & \text{for} \quad V_{ds} \le V_{gs} - V_{Td} \\ C_{oxd}C_{gdj}/(C_{oxd}+C_{gdj}) & \text{for} \quad V_{ds} > V_{gs} - V_{Td} \end{cases}$$

Table 5.2. Bipolar Characteristics of IGBT Model.

$$I_p(W) = \left(\frac{1}{1+b}\right) I_T + \left(\frac{b}{1+b}\right) \frac{4D_p}{W^2} Q + \frac{C_{bcj}}{3} \frac{Q}{Q_B} \frac{dV_{bc}}{dt}$$

$$I_n(W) = I_{mos} + I_{mult} + (C_{dsj} + C_{gd}) \frac{dV_{ds}}{dt} - C_{gd} \frac{dV_{gs}}{dt}$$

$$\frac{dQ}{dt} = I_n(W) - \frac{Q}{\tau_{HL}} - \frac{Q^2}{Q_B^2} \cdot \frac{4N_B^2}{n_i^2}$$

$$V_A = V_{bc} + V_{ebd}(Q, V_{bc}) + I_T \cdot R_b(Q, V_{bc})$$

Table 5.4. State equations for the IGBT analytical model.

$$\frac{dV_{gs}}{dt} = \frac{I_g}{C_{gs}+C_{gd}} + \frac{C_{gd}}{C_{gs}+C_{gd}} \cdot \frac{dV_{bc}}{dt}$$

$$\frac{dV_{bc}}{dt} = \frac{I_T - \frac{4D_p}{W^2} + \left(1+\frac{1}{b}\right)\left[\frac{C_{gd}}{C_{gs}+C_{gd}} I_g - I_{mos}\right]}{\left(1+\frac{1}{b}\right)\left[C_{dsj} + \frac{C_{gs}C_{gd}}{C_{gs}+C_{gd}} + \frac{C_{bcj}}{3}\frac{Q}{Q_B}\right]}$$

$$\frac{dQ}{dt} = I_{mos} + (C_{dsj}+C_{gd})\frac{dV_{bc}}{dt} - C_{gd}\frac{dV_{gs}}{dt} - \frac{Q}{\tau_{HL}} - \frac{Q^2}{Q_B^2} \cdot \frac{4N_B^2}{n_i^2}$$

Table 5.5. Functions of System Variables.

$$W_{gdj} = \sqrt{2 \epsilon_{si} (V_{ds} - V_{gs} + V_{Td}) / qN_{scl}}$$

$$W_{dsj} = \sqrt{2 \epsilon_{si} (V_{ds} + 0.6) / qN_{scl}}$$

$$W_{bcj} = \sqrt{2 \epsilon_{si} (V_{bc} + 0.6) / qN_{scl}}$$

$$W = W_B - W_{bcj}$$

$$BV_{cbo} = BV_f \cdot 5.34 \times 10^{13} \cdot N_{scl}^{-0.75}$$

$$M = 1 / \left[1 - (V_{cb} / BV_{cbo})^{BV_n} \right]$$

$$Q_B = qAWN_{scl}$$

$$C_{bcj} \equiv A \epsilon_{si} / W_{bcj}$$

$$C_{dsj} = (A - A_{gd}) \epsilon_{si} / W_{dsj}$$

$$C_{gdj} = A_{gd} \epsilon_{si} / W_{gdj}$$

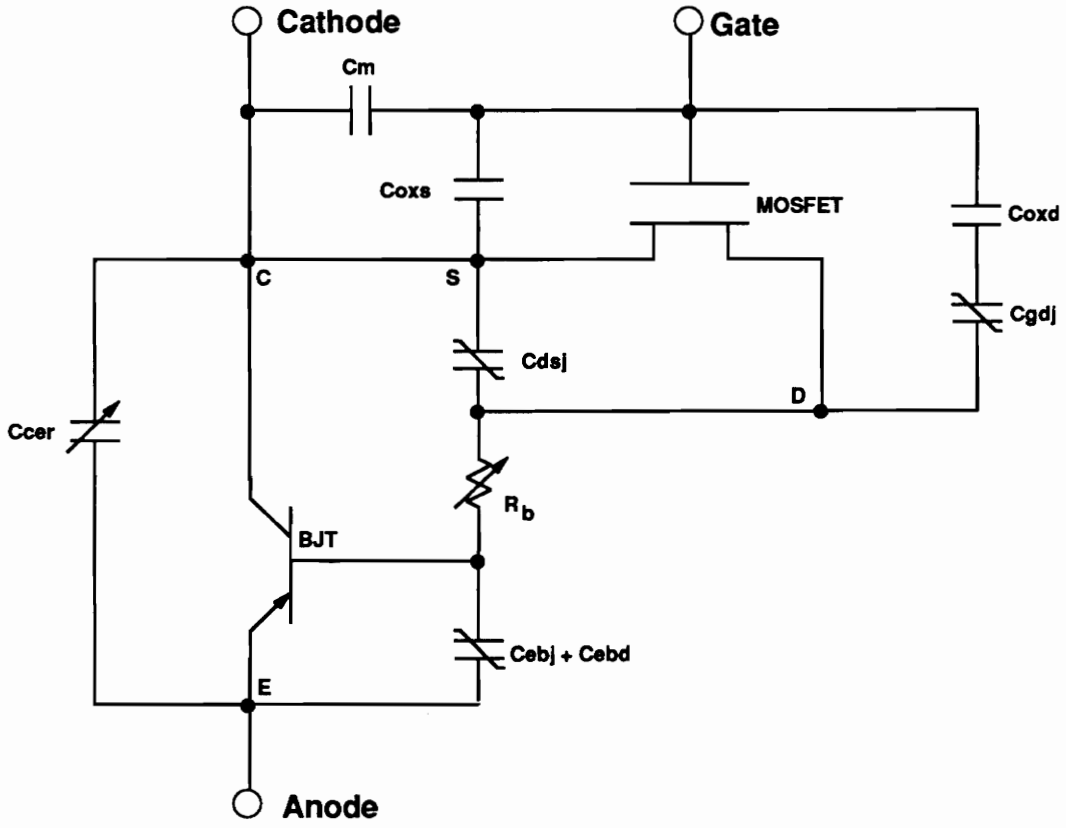


Figure 5.1. IGBT equivalent circuit.

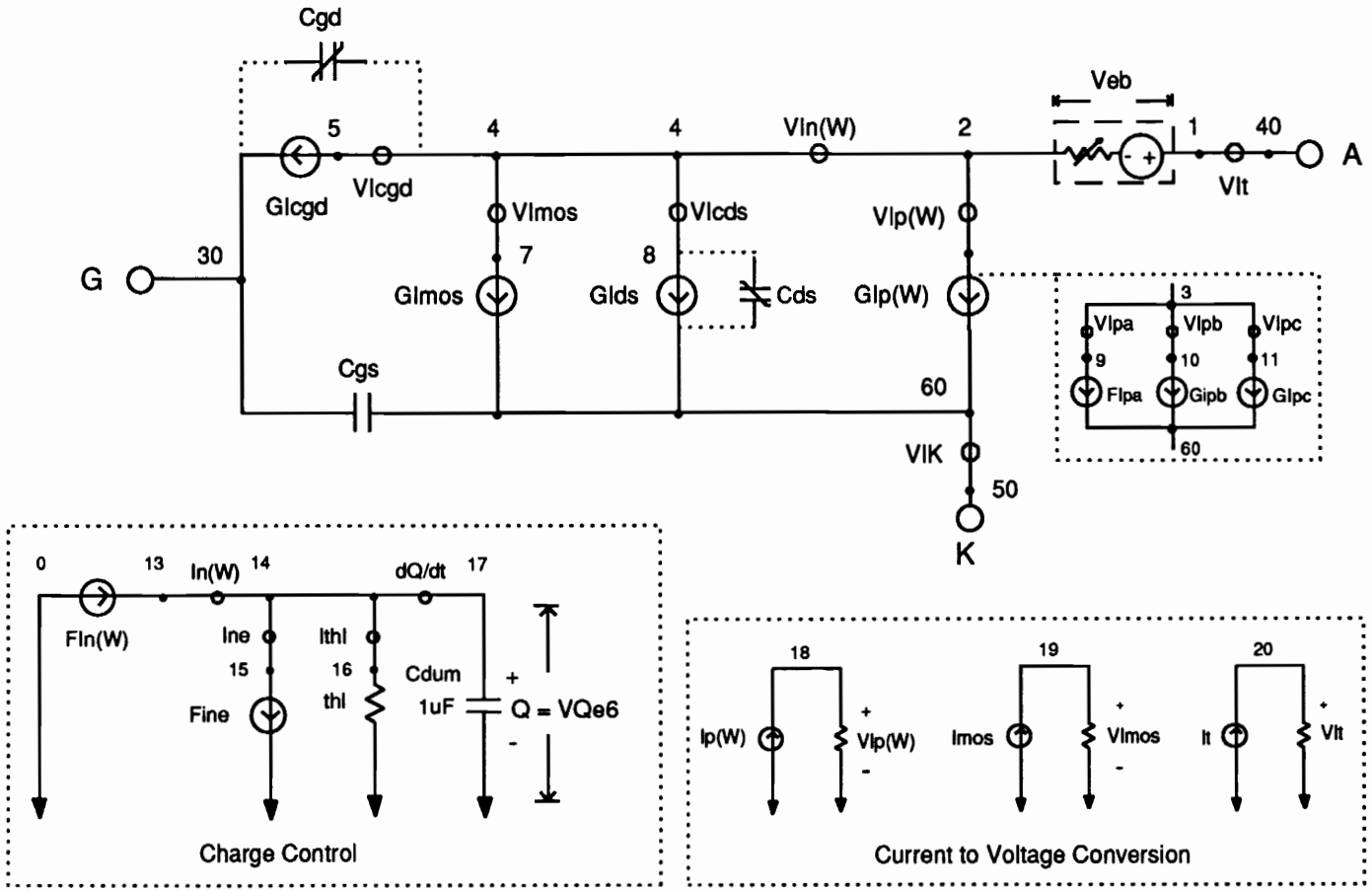


Figure 5.2. IG-Spice IGBT equivalent circuit.

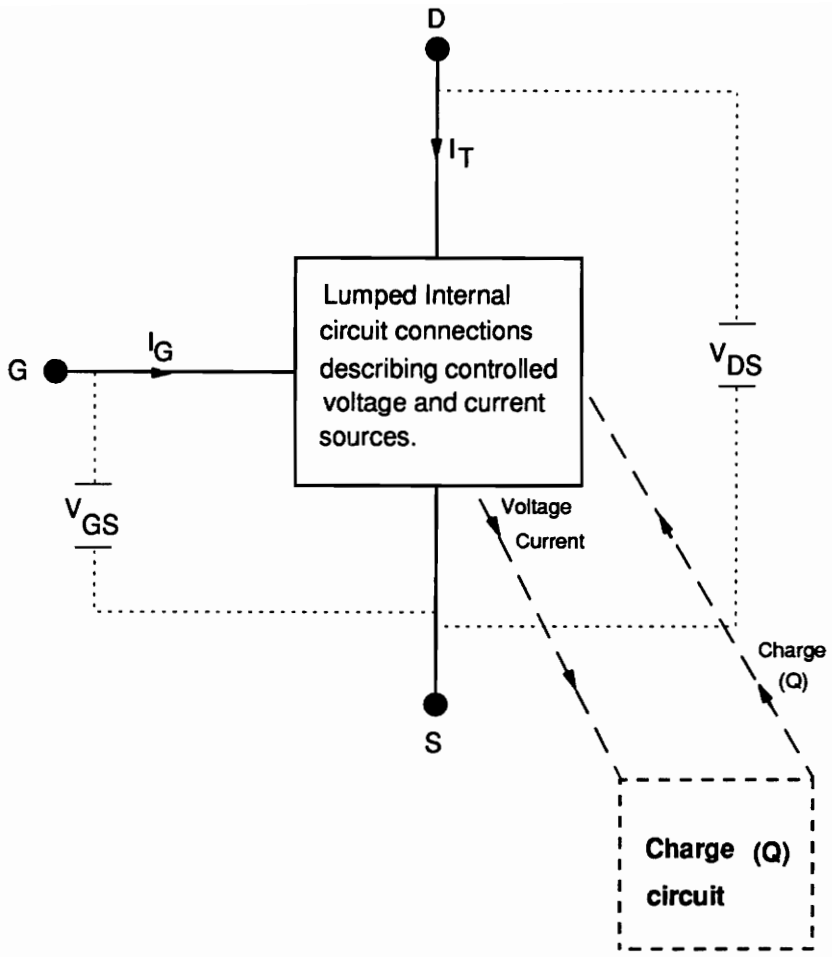


Figure 5.3. Simplified IGBT circuit expression for IGBT.

5.3 Implementation of Analytical Model

In general, IGBT can be represented as a PNP bipolar transistor supplied base current by the VDMOSFET. By understanding this concept, all the analytical expressions which describe the IGBT functions can be separated into the MOSFET portion and the BJT portion. But the equations describing the time-rate-of-change of base charge is implemented as a separate circuit, since it is neither voltage nor current. So the complicated equations have been represented into its simpler circuit form, and the procedures of IG-Spice need to be followed in order to implement the analytical expressions into the IG-Spice subroutines.

In the remainder of this section the procedures used to convert the equations which describe the IGBT into equivalent IG-SPICE current, and voltage sources, are discussed. The methods used to ensure convergence of the IG-SPICE model are also discussed.

In order to simplify the implementation process, the derivation of complete IG-Spice IGBT model is done in three separate sections: MOSFET, bipolar PNP, and base charge (Q).

5.3.1 MOSFET

As stated before, the MOSFET current supplies the electron current to the base of the bipolar transistor. This electron current, $I_n(W)$, consists of both static and dynamic currents that flow through the MOSFET. Thus the expression describing the electron current at the collector edge of neutral base is expressed as the sum of the MOSFET channel current and the displacement currents through the drain-source and gate-drain capacitances [3]:

$$In(W) = Imos + (Cdsj + Cgd)\frac{dVgd}{dt} - Cgd\frac{dVgs}{dt}, \tag{5.1}$$

where I_{mos} is given in terms of the system variables of the IGBT as discussed earlier, and the equations describing this current are shown in Table 1.

Since the equations describing the MOSFET current consists of three different controlling variables, the equation is best implemented if it is separated into three different controlled sources. The equivalent circuit describing this electron current can be seen in Fig. 5.4.

As discussed earlier, the coefficients for the subroutine needs to be calculated. Since V_{ds}, and V_{gs} are the system variables, the partial derivative of the I_{mos} expressions with respect to these system variables need to be found for each state. For example, the case where MOSFET current is to describe the condition when ($V_{ds} < V_{gs} - V_T$), the partial of the expression need to be found with respect to V_{gs} and with respect to V_{ds}. For the case where ($V_{ds} > V_{gs} - V_T$), only the partial of I_{mos} expression with respect to V_{gs} need to be found. In general, the key expressions describing the controlled dependent sources which contain aforementioned system

variables, the partial derivative with respect to these system variables need to be found. The partial derivatives describing each function of the IG-Spice IGBT model is given in Appendix C.

The latter descriptions of the electron current consists of nonlinear capacitances which are dependent upon system variable voltages, V_{gs} and V_{ds}. These nonlinear capacitances can be expressed in terms of voltage controlled current sources, since the current through them are dependent upon the time rate of change of voltages across them. The system variables are given by the IG-Spice, and only the nodes at the correct branches need to be specified to describe these dependent current sources.

From the Tables 1 and 2, there are numerous variables given which need to be calculated before the correct capacitance values can be found. Even though there exist system variables within these expressions, the partial expressions with respect to each system variables need not be found, because they are not directly describing the controlled current source. For example, the gate-to-drain capacitance needs to be expressed as a controlled current source, and its equation is given as follows:

$$C_{gdj} = \frac{Agd \in_{si}}{W_{gdj}}. \tag{5.2}$$

The expressions which are needed in order to find this value of capacitance is assumed constant, because only the current through the capacitance is of interest. Therefore, the partial derivatives are found when the system variables, V_{gs} and V_{ds}, are used to express the instantaneous current through the capacitance. The final expression is:

$$i_{cgd} = C_{gd}\frac{d(V_{ds} - V_{gs})}{dt}, \tag{5.3}$$

and using this expression, the coefficients for the subroutine which describe the current through the gate-drain capacitance are found. This expression can be written in the IG-Spice form which was described in the previous chapter:

$$i_{cgd} = C_{gd}(V_{ds} - V_{dso})ODT - C_{gd}(V_{gs} - V_{gso})ODT, \tag{5.4}$$

where

$$\frac{1}{dt} = \frac{1}{(TIME - TOLD)} = ODT, \tag{5.5}$$

$$\frac{dV_{ds}}{dt} = (V_{ds} - V_{dso}) \cdot ODT, \tag{5.6}$$

and

$$\frac{dV_{gs}}{dt} = (V_{gs} - V_{gso}) \cdot ODT. \tag{5.7}$$

In the IG-SPICE IGBT equivalent circuit model, this electron current is decomposed into three user-defined functions: *Imos*, *Icds*, and *Icgd*. The current sources corresponding to these functions are indicated in Fig. 5.1 as: *GImos*, *GIcgd*, and *GIcds*, respectively. The MOSFET channel current of the IG-SPICE IGBT model is described by the current source *GImos*, while the currents through the nonlinear capacitances (C_{gd} and C_{ds}) are represented by the controlled sources *GIcgd* and *GIcds*. These nonlinear voltage-dependent depletion capacitances (C_{gd} and

C_{ds}) are indicated on Fig. 5.2 by the capacitor symbols with diagonal lines through them.

The gate-source capacitance C_{gs} of the IG-SPICE IGBT model is assigned a fixed value. The feedback capacitance C_{gd} is voltage dependent and has a two-phase of dependency, (one phase for $V_{ds} < V_{gs} - V_{Td}$ and another for $V_{ds} > V_{gs} - V_{Td}$ as described in Table 1), where capacitor C_{oxd} is a fixed value. The drain-source depletion capacitance is also voltage dependent, but there is only one phase associated with this capacitance.

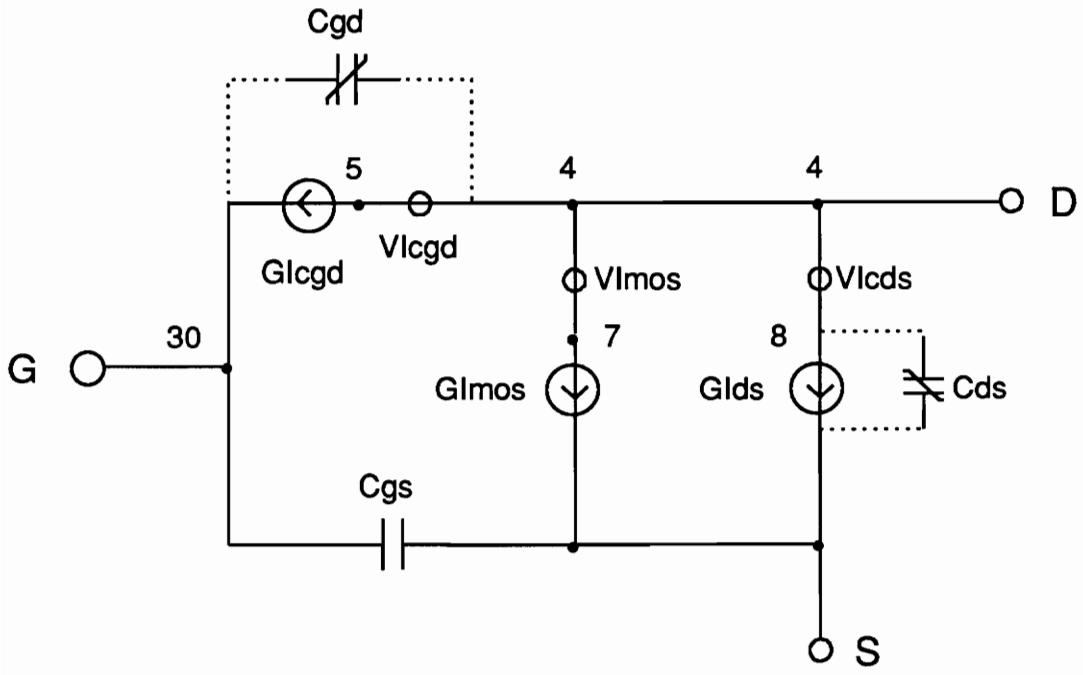


Figure 5.4. MOSFET equivalent circuit.

5.3.2 Bipolar transistor collector hole current

The hole current at the collector edge of the neutral base for the moving boundary condition is expressed as [3]:

$$I_p(W) = \left(\frac{1}{1+b}\right) I_T + \left(\frac{b}{1+b}\right)\frac{4D_p}{W^2}Q + \frac{C_{bcj}}{3}\cdot\frac{Q}{Q_B}\cdot\frac{dV_{bc}}{dt}. \qquad (5.8)$$

The first term on the right-hand side of this equation results from the coupling between the transports of electrons and holes for ambipolar transport; the second term is the high-level injection charge control term; and the third term is a non-quasi-static term which describes the redistribution of carriers for the moving boundary condition [1]. This third term is represented as the collector-emitter redistribution capacitance C_{cer}, in Fig. 5.1, which is proportional to the instantaneous change in the base, because this term depends on the time rate-of-change of the base-collector voltage.

Equation (5.8) depends upon current type, voltage type, and charge type controlling variables (ie., I_T, Q, V_{bc}). As previously mentioned, the controlling variables of the source functions need to be of one type: either current or voltage. To accomplish this, Eq. (5.8) is separated into three different dependent sources: *Flpa*, *Glpb*, and *Glpc*, which are paralleled to obtain the total bipolar transistor hole current $I_p(W)$. This paralleling method, which reduces the number of controlling source type conversions, ensures better convergence. The collector hole current portion of Fig. 5.2 is shown in Fig. 5.5.

The first term in Eq. (5.8) is represented as the current-controlled current source *Flpa*, where I_T is the total current of the device which is defined as a current source probe (see Fig. 5.1). The second and third terms are implemented as voltage-controlled current sources *Glpb* and *Glpc*, respectively, where the base charge Q is represented as a node voltage.

In the equation describing the hole current of the bipolar PNP, the system variables V_{gs} and V_{ds} are not used. Instead, the system variable Q is used. The charge Q can be described in terms of node voltage, and detailed description will be given in next section. The total current I_T, is just extracted from the equivalent circuit, and the expression which is dependent upon this current doesn't need to have a written subroutine. Instead, simple current multiplier can be used. The partial derivative of second term need to be found with respect to system variable Q. The coefficients of third term need to be found by finding the partial derivatives with respect to system variables, Q and V_{ds}. The equivalent expressions describing the voltage controlled current sources for last two expressions are:

$$i_{pb} = \left(\frac{1}{1+b}\right)\frac{4D_p}{W^2}Q, \tag{5.9}$$

and

$$i_{pc} = \frac{C_{bcj}}{3}\cdot\frac{Q}{Q_B}\cdot\frac{dV_{bc}}{dt}. \tag{5.10}$$

When the partial derivative of the first expression is found with respect to the system variable Q, the following expression results:

$$\frac{\partial i_{pb}}{\partial Q} = \left(\frac{b}{1+b}\right)\frac{4D_p}{W^2} = Coef(2), \tag{5.11}$$

and

$$Coef(1) = 0, \tag{5.12}$$

where the total expression describing this function is:

$$i_{pb} = Coef(2) \cdot Q. \tag{5.13}$$

For the third part of the Equation (5.8), the expression must be put into the IG-Spice format which describes the state equations because it requires the use of a time derivative. This equation is written as:

$$i_{pc} = \frac{C_{bcj}}{3} \cdot \frac{Q}{Q_B} \cdot (V_{bc} - V_{bco}) \cdot ODT. \tag{5.14}$$

Since the equation has two defined system variables (Q and V_{bc}), the partial derivatives with respect to both variables must be found. The expressions describing the partials of this equation is:

$$\frac{\partial i_{pc}}{\partial Q} = \frac{C_{bcj}}{3} \cdot \frac{1}{Q_B} \cdot (V_{bc} - V_{bco}) \cdot ODT = Coef(3), \tag{5.15}$$

$$\frac{\partial i_{pc}}{\partial V_{bc}} = \frac{C_{bcj}}{3} \cdot \frac{Q}{Q_B} \cdot ODT = Coef(2), \tag{5.16}$$

and

$$i_{pc} - Coef(3) \cdot Q - Coef(2) \cdot V_{bc} = -\frac{C_{bcj}}{3} \cdot \frac{Q}{Q_B} \cdot V_{bc} \cdot ODT = Coef(1). \tag{5.17}$$

Then the current describing the i_{pc} is expressed as:

$$i_{pc} = Coef(1) + Coef(2) \cdot V_{bc} + Coef(3) \cdot Q, \tag{5.18}$$

and this current value is passed to the main circuit of the IG-Spice IGBT model during the each time-step of transient analysis. The total hole current is then expressed as:

$$I_p(W) = i_{pa} + i_{pb} + i_{pc}, \tag{5.19}$$

where each current is expressed by its own functions.

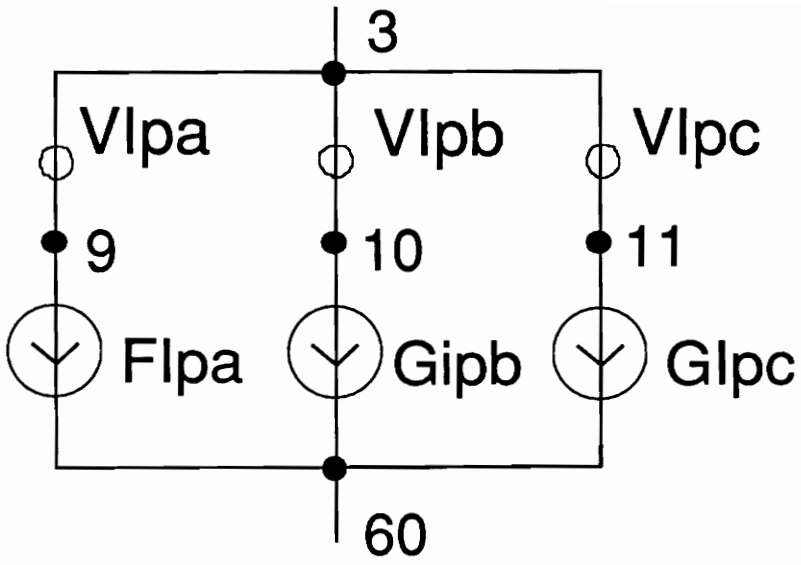


Figure 5.5. Equivalent circuit for collector hole current.

5.3.3 Bipolar transistor base charge control

The equation describing the conservation of excess majority carrier base charge is [6]:

$$\frac{dQ}{dt} = In(W) - \frac{Q}{\tau_{HL}} - \frac{Q^2}{Q_B^2} \cdot \frac{4N_B^2}{n_i^2} I_{sne}, \tag{5.20}$$

where the charge Q is supplied by the electron current at the collector edge of the base, $I_n(W)$, and is depleted by the recombination in the base (the second term on the right-hand-side of the equation), and by the injection of electrons into the emitter (third term on the right-hand-side of the equation). The same problem encountered with the hole current is encountered in Eq. (5.20). That is, the expression consists of several controlling sources, and it would be impractical to implement the whole equation within a single controlled source. Therefore, this equation is also separated into different parts. In addition, because Q is neither a current nor a voltage type, it must be converted as an voltage or current type.

To do this, the expression describing the relationship between the charge, capacitance, and voltage: Q = CV, is substituted into Eq. (5.20). By using C = 1 F, the voltage on the 1 F capacitance (VQ) represents the base charge Q, and the carrier lifetime t_{hl} can now be identified as a resistance. As a result, the following equivalent expressions are derived:

$$\frac{dQ}{dt} \equiv \text{net current through capacitance C}, \tag{5.21}$$

and

$$\tau_{hl} \equiv R = 10^{-6} : \text{ where } Q/R = I_{thl} = 10^{6}Q \tag{5.22}$$

In addition, because the value of the resistance associated with τ_{hl} is on the order of magnitude of 10^{-6} ohms, the values of (*VQ*) that are solved for by the simulator are many orders of magnitude smaller than the other voltages in the circuit. This would require that the error tolerance be made very small for the SPICE-based algorithm, which would result in much longer convergence times. This problem can be alleviated by normalizing Eq. (5.20) [4] in order to increase the resistance associated with τ_{hl} to a value on the order of 1.0. In doing this, a value of capacitance *1 uF* is used to convert the charge-type variable Q to voltage (VQe6) type variable.

Therefore, the normalized expressions are represented as follows;

$$Q' = 10^6 \cdot Q = V', \tag{5.23}$$

$$C' = \frac{V}{V'} = 10^{-6}\,\text{Farad} = 1\mu F, \tag{5.24}$$

and

$$Q \equiv 10^{-6} \cdot Q'. \tag{5.25}$$

The resulting normalized charge control expression is converted to an auxiliary circuit, which is shown in the IG-SPICE IGBT equivalent circuit of Fig. 5.2 and is repeated in Fig. 5.6. Note that since the charge Q' across the capacitance is in the order $10^6 \cdot Q$, the user must remember to multiply this variable VQe6 by 10^{-6} factor in order that the correct charge value may be passed to other functions which are dependent upon this system variable. When finding the coefficients of the function, the expression might result in Q^2. If this is the case, the normalized value of Q' need to be multiplied by a value 10^{-12}. This can be generalized so that the desired charge Q is equal to:

$$Q \equiv (Q')^n \cdot (10^{-6})^n, \tag{5.26}$$

where n represents the multiples of Q'.

In the base charge control circuit of Fig. 5.6, the current-controlled current sources, *Flnw* and *Flne*, describe the base current and the component of electron current injected into the emitter, respectively. The current through the resistance, *Rthl*, which emulates the recombination in the

base is represented by the current probe, *Ithl*. The current through the normalizing capacitance, *Cnorm*, represents the time rate-of-change of stored base charge (*VQe6*).

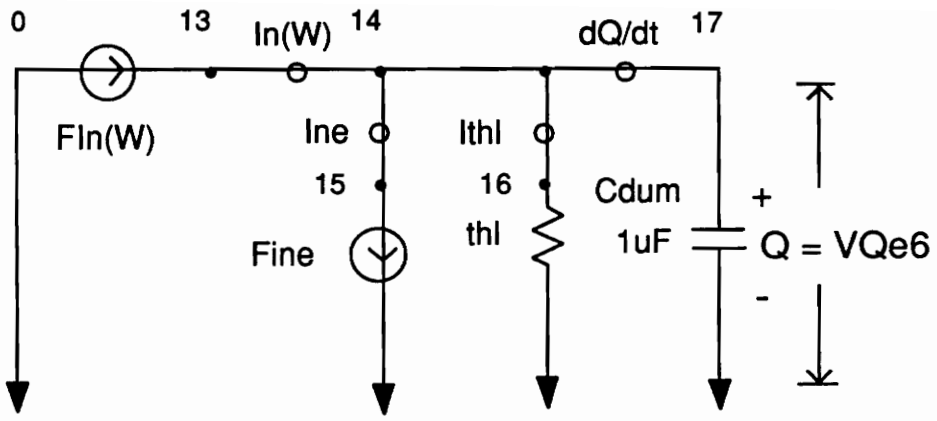


Figure 5.6. Base charge control circuit.

5.3.4 Emitter-base voltage and conductivity modulated resistance

The emitter-base voltage consists of three components as shown in Fig. 5.1: 1) the voltage drop across the conductivity-modulated base resistance, 2) the emitter-base diffusion capacitance potential, and 3) the emitter-base depletion capacitance potential. For forward conduction the emitter-base voltage was shown in [3] to be given by:

$$V_{eb} = V_{ebd}(V_{bc}, Q) + I_T \cdot R_b(V_{cb}, Q) + I_T \cdot R_s, \tag{5.27}$$

where the conductivity-modulated resistance R_b, and the potential drop across the emitter-base diffusion capacitance V_{ebd}, are obtained in terms of instantaneous values of both Q and V_{bc}. For dynamic operation, the total current I_T, can flow through the base before sufficient charge, Q, is present to modulate the base resistance R_b; thus IGBTs can exhibit dynamic saturation [3, 9]. The emitter-base junction depletion capacitance C_{ebj}, is important when the emitter-base junction is reverse biased or has a small forward biases, but for large forward bias, C_{ebd} is dominant.

Appendix B shows the equations that are needed to describe the behavior of the emitter-base voltage junction. To describe this emitter-base voltage and the conductivity-modulated base resistance R_b, a voltage-controlled voltage source (VCVS) is used. It was suggested in [8] that the current output ensures better convergence within the Spice-based programs, but due to the complexity and its function being dependent upon all the system variables, the choice was limited to implementation of the function as a voltage-controlled-voltage source. All of the current-type

controlling sources are transformed into voltage-type controlling sources by the use of the simple resistor networks shown in the lower right-hand corner of Fig. 5.1. Due to the complexity of the Veb function, the partial derivatives must be analyzed in detail in order to reduce the discontinuity between the partial derivatives associated with the junction depletion capacitance C_{ebj} and those associated with the diffusion capacitance C_{ebd}. In general, a discontinuity in the partial derivatives can cause convergence problems.

The function describing the emitter-base junction combines several detailed procedures which had to be implemented. Within this function, 1) the calculation of conductivity-modulated base resistance R_b, 2) the calculation of emitter-base voltage, and 3) calculation of carrier-carrier scattering effect needed to be implemented. Also, this function allows the model to behave as just a MOSFET or to behave as a complete IGBT device. Detailed description of the functions of the model is presented Appendix D.

This function does not require unique techniques in order to implement as the previous functions, but its difficulty lies in its complex analytical expressions, which require detailed attention when finding the partial differential equations for its coefficients. Its detailed derivation of each coefficients are described in Appendix C.

5.4 Simulation Results

Few of the unique features of the analytical model are mentioned in Chapter 3. Some of these features are: the conductivity modulation, carrier scattering, moving boundaries, recombination, and nonlinear junction capacitances.

The IG-Spice IGBT model is very flexible in that if the user needs to observe certain characteristics of the device, he only needs to specify the branch currents or node voltages which he wants to observe. For example, the nonlinear capacitance phenomena of the gate-drain capacitance can be observed by simply specifying the current probe Icgd (shown in Fig 5.1). Also, the model is unique in that the user can disregard the PNP bipolar transistor portion of the model and observe just the MOSFET portion.

In the following sections, the effectiveness of the model will be shown by discussing simulated results for the MOSFET, conductivity modulation, carrier scattering, current tail, and the simulated results for the inductive load switching characteristics.

5.4.1 MOSFET

In order to turn off the PNP bipolar transistor, the user only need to specify the variable t=-1. This tells the program that the model is MOSFET. It was discussed in [4] where Dr. Hefner described the parameter extraction method of the MOSFET parameters. In that paper, the author described the behavior of certain parameters. In order to test just how accurate the IG-Spice can identify the MOSFET, same test conditions were applied for the simulation. These tests were done so that the gate current was relatively constant (approximately 20 mA), and for a load which results in a low anode current. The simulation was done using the nominal parameter values shown in Table 4. The simulation results for the IGBT charging characteristics are shown in Fig 5.7 for V_A = 20 V, and Fig 5.8 for V_A = 300 V. These gate voltage waveforms consists of three phases, as shown in Fig 5.7. During the first phase, gate-source voltage V_{gs}, rises steadily due the gate current charging the steady gate-source capacitance C_{gs}, and the small high-voltage gate-drain C_{gd} capacitance. The second phase emphasizes relatively constant gate-source voltage, due to a small increase of V_{gs} necessary for the IGBT to supply small load current and the small output displacement current.

Figure 5.7 emphasizes the range for which C_{gd} is equal to gate-drain overlap oxide capacitance $V_{ds}<V_{gs}-V_{Td}$, and Fig 5.8 emphasizes the range for which C_{gd} is inversely proportional to the square-root of the gate-drain voltage. During the third phase of the gate voltage waveform, V_A remains relatively constant due to its on-state value, and V_{gs} rises with a constant slope (different from first state) as the gate current charges the sum of the gate-drain-overlap oxide capacitance and the gate-source capacitance. Figure 5.9 shows the effect of drain-source capacitance for Fig. 5.8 conditions.

5.4.2 Conductivity modulation

To show the effectiveness of the model, the voltages at the emitter-base were observed when the model was operating as just a MOSFET, and when it was operating as a complete IGBT model. Figure 5.10(a) show the emitter-base voltage V_{eb},when the conductivity modulation was applied. As can be seen, the maximum voltage is approximately 1 V for the circuit conditions given. Figure 5.10(b) shows the V_{eb} when PNP transistor is turned off, thereby turning off the conductivity modulation. The model is behaving just as a power MOSFET

5.4.3 Carrier-carrier scattering

Due to the temperature rise of the device, the random motion of the carriers increase. This random movement causes the carriers to collide with crystal lattice, thereby slowing the time required to readh the destination. Because this collision with the crystal lattice is within the device structure, the effective resistance of the device increases, and the simulated result of this effect is shown in Fig. 5.11. The simulation result show that the resistance of the device increases with carrier scattering within the IGBT semiconductor devices.

5.4.4 Current tail

The IGBT device structure is such that the base contact of the PNP transistor is internal, and the reverse current cannot be applied to speed up the turn off process. When the gate voltage is removed, the complete turn-off is dependent upon the carrier recombination. This inability to tap into the base of the PNP transistor causes the tailing effect of the IGBT device. This current tail can be observed in simulated result of Fig. 5.12. The length of this current tail is dependent upon the carrier lifetime of the device.

5.4.5 General circuit interaction

For the IG-Spice IGBT model to be effective, it needs to interact with external properties of the circuit being simulated. Figures 5.13 to 5.15 show the simulated results in which the device model was tested in an inductive load circuit. The simulated results show the anode voltage, anode current, gate current, and gate-source voltage. From the description of the anode voltage, it can observed that there is overshoot occurring due the inductor into the circuit. And if the anode current is observed, it can be seen that the gate resistance affects the turn-off time of the device and its current tail. So the model effectively interacts with external conditions of the circuits.

Table 5.1. Nominal Device Parameters.

τ_{HL}	7.5 μs
N_B	$2x10^{14}$ cm^{-3}
W_B	93 μm
I_{sne}	6.0×10^{-14} A
K_{Psat}	0.6 A/V^2
K_{Plin}	0.95 A/V^2
V_T	4.7 V
A_{gd}	0.05 cm^2
C_{oxd}	1.6 nF
C_{gs}	0.6 nF
V_{Td}	0 V
n_i	1.45×10^{10} cm^{-3}
μ_n	1500 $cm^2/V\text{-}s$
μ_p	450 $cm^2/V\text{-}s$
ϵ_{si}	1.05×10^{20} F/cm
α_1	1.428×10^{20} $(cmVs)^{-1}$
α_2	4.54×10^{11} cm^{-2}
ν_{nsat}	1.1×10^7 cm/s
ν_{psat}	0.95×10^7 cm/s
BV_f	1.0
BV_n	4.0
θ	0.01 V^{-1}

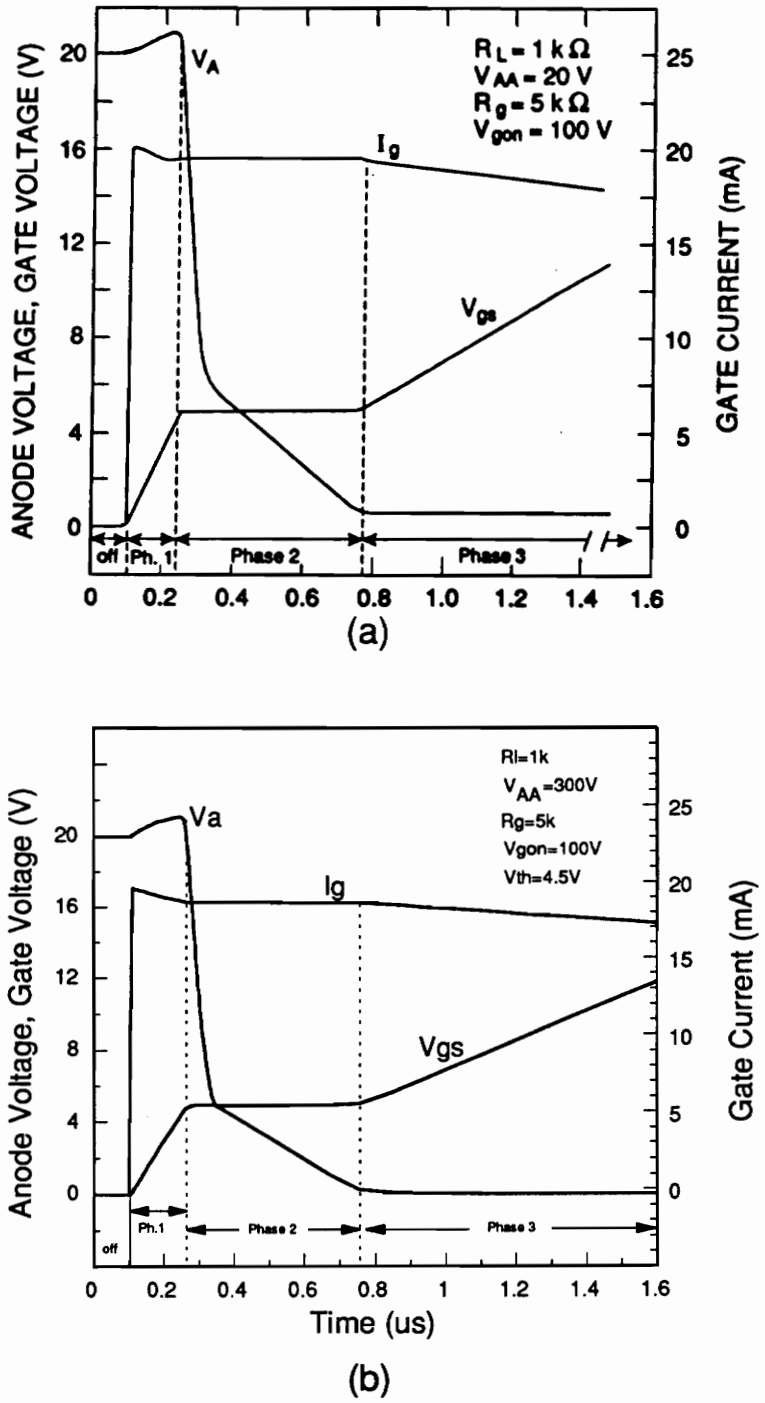


Figure 5.7. The charging characteristics for a low anode current and relatively constant current at 20 mA gate current for V_{AA}=20V: (a) measured, and (b) simulated with different threshold voltage.

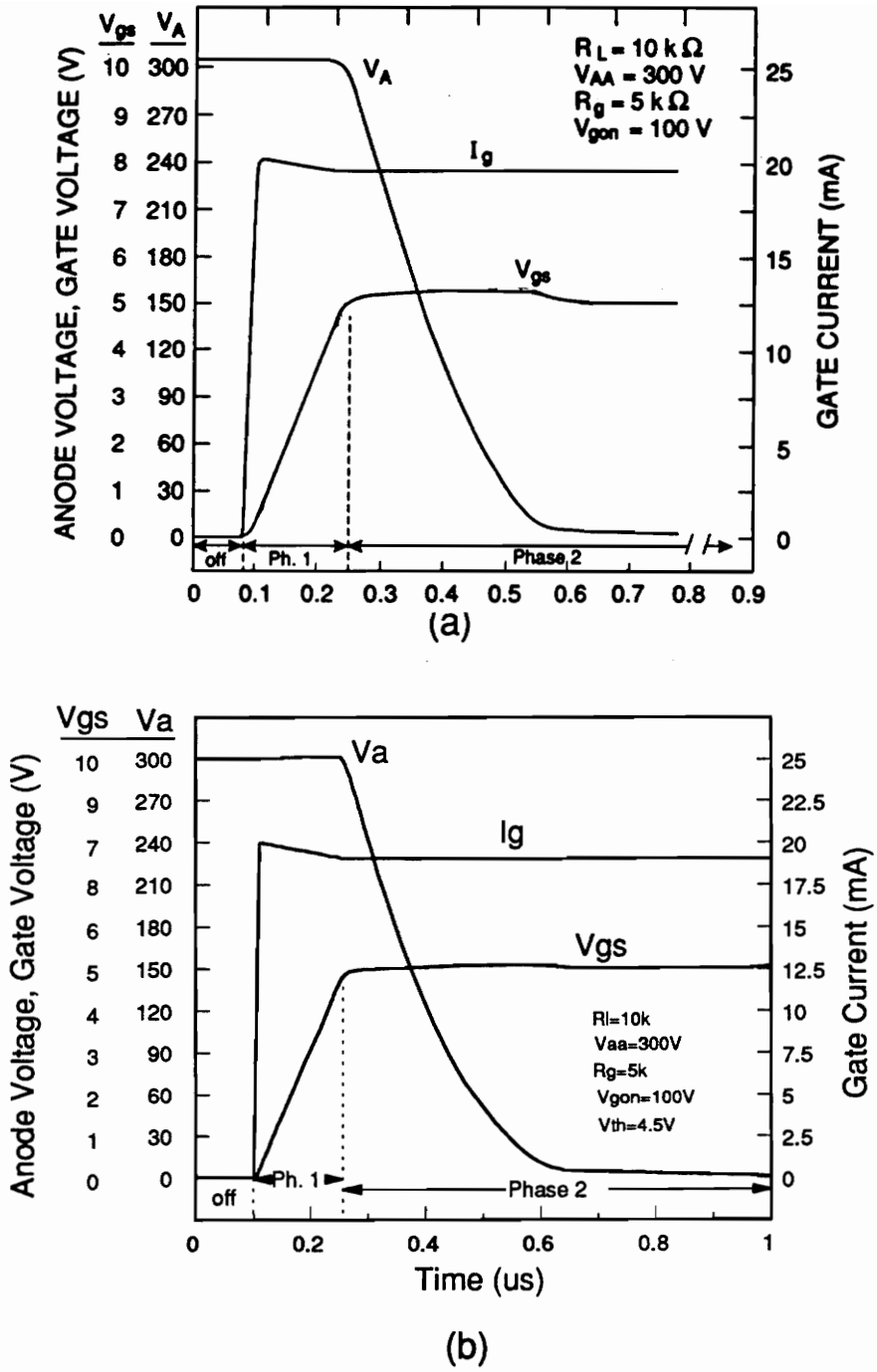


Figure 5.8. The charging characteristics for a low anode current and relatively constant current at 20 mA gate current for V_{AA}=300 V: (a) measured, (b) simulated with threshold voltage of 4.5 V.

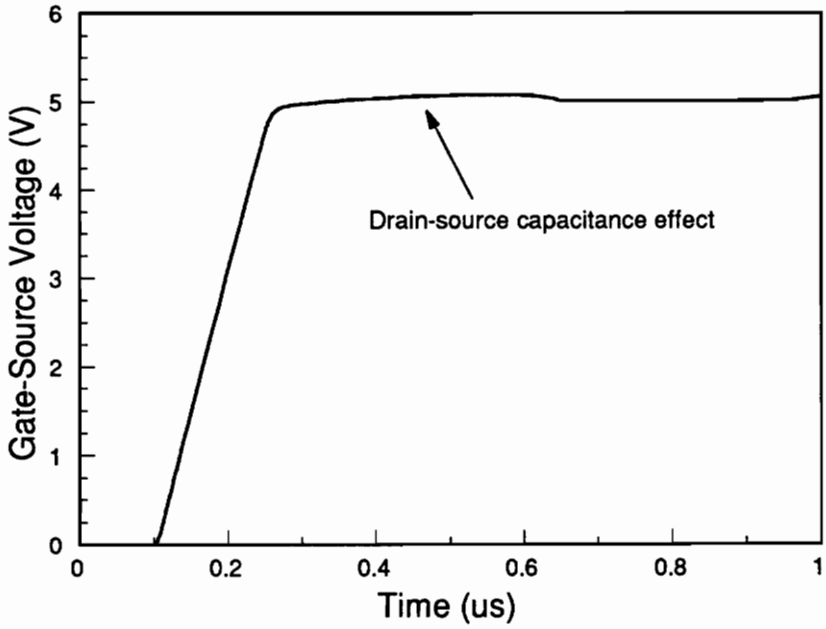


Figure 5.9. Gate-source voltage emphasizing drain-source capacitance effect on the IGBT device.

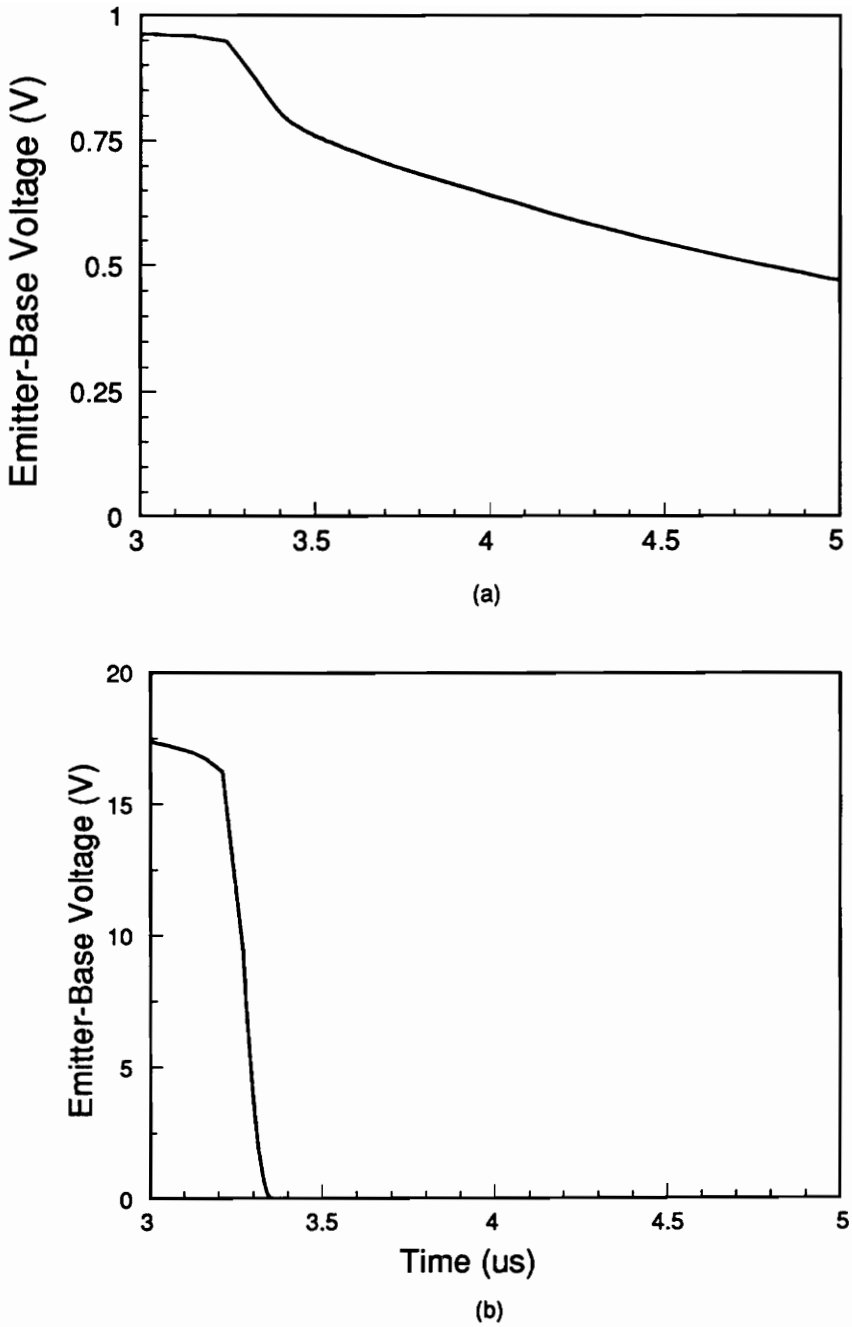


Figure 5.10. Emitter-base voltage: (a) conductivity modulated, and (b) MOSFET.

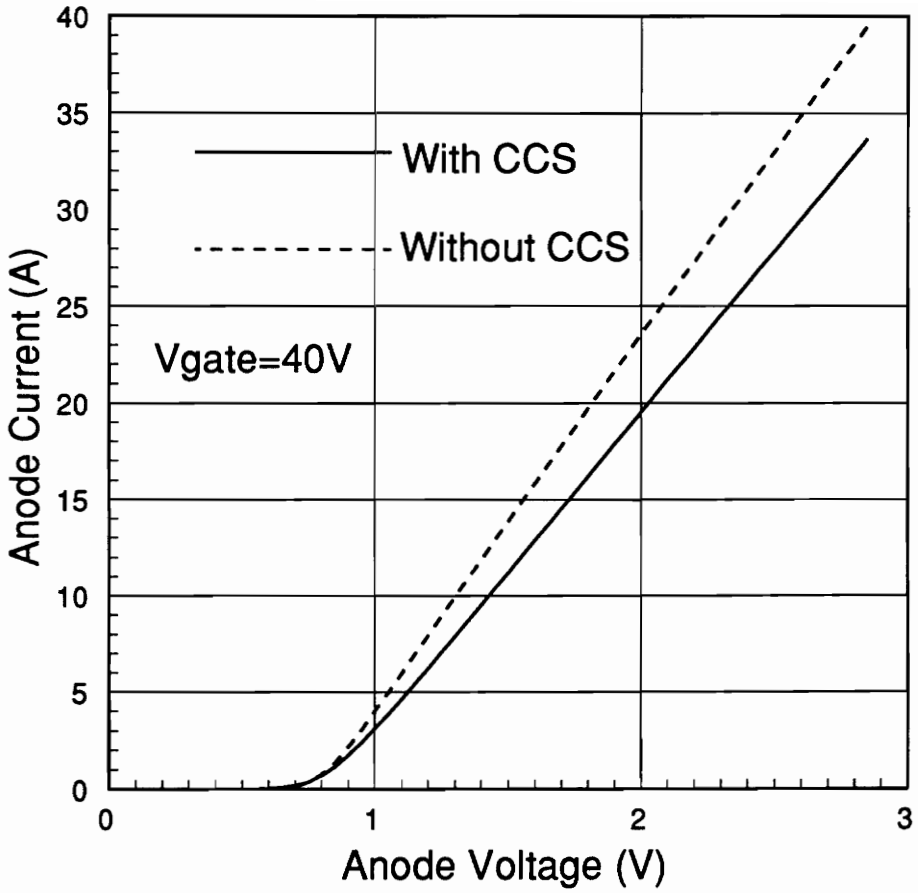


Figure 5.11. Carrier scattering effect on the device resistance.

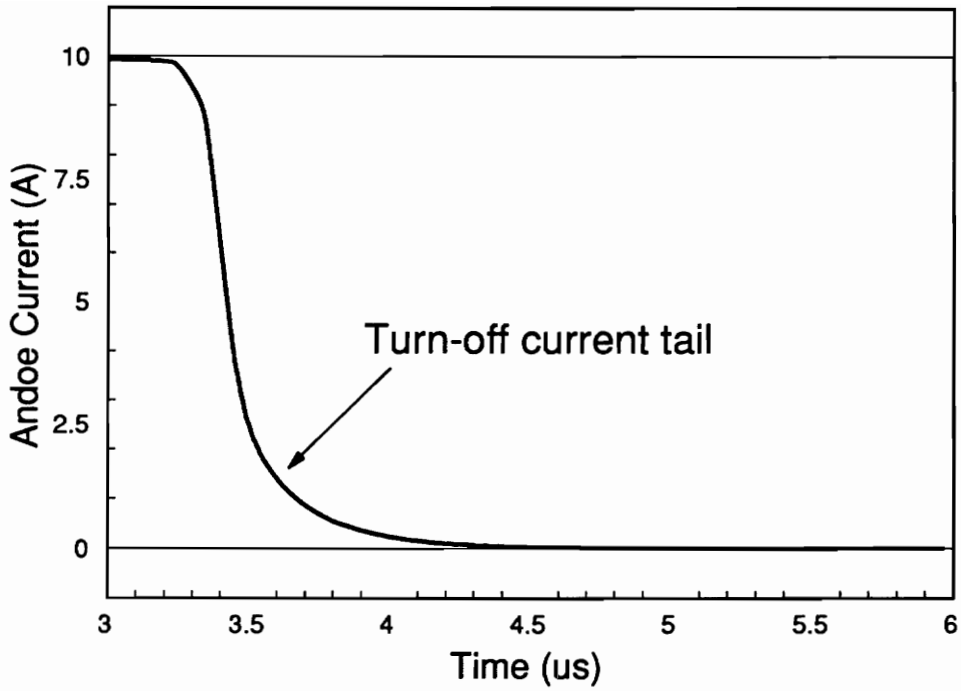


Figure 5.12. Anode current showing the effect of current tail.

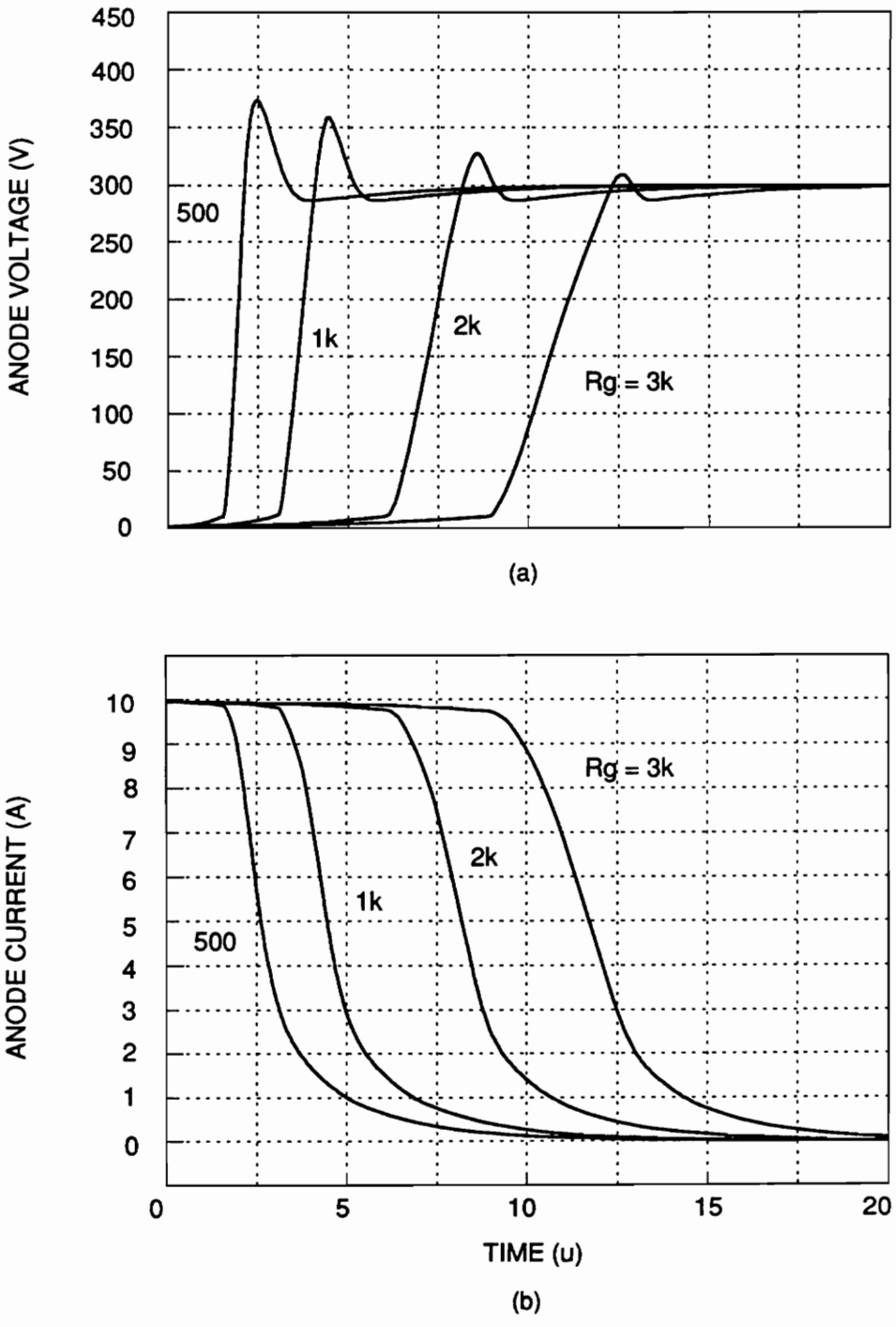


Figure 5.13. Simulation result for different gate resistances: (a) anode voltage, and (b) anode current.

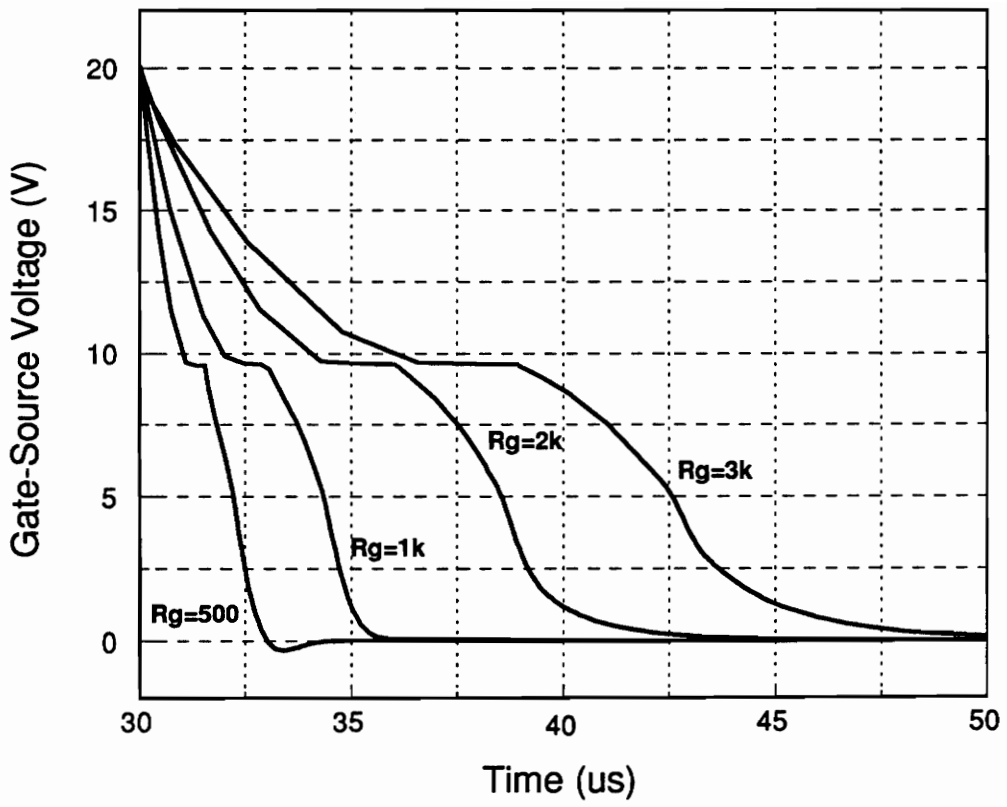


Figure 5.14. Simulation result for different gate resistances showing gate voltage.

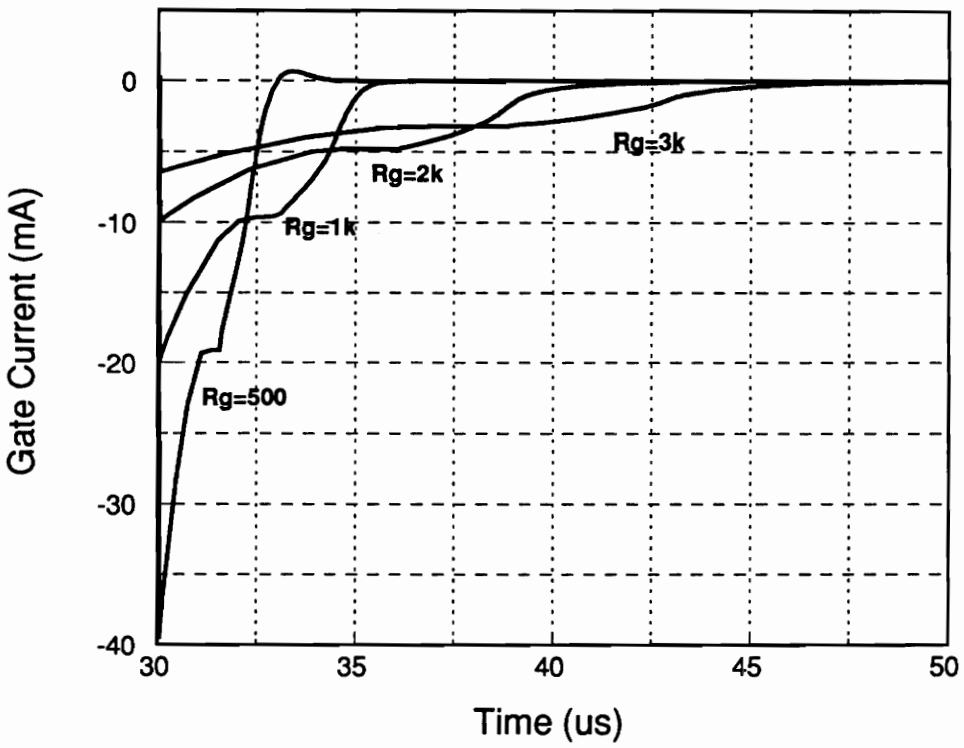


Figure 5.15. Simulation result for different gate resistances showing gate current.

5.5 Comparison of Simulation Results and Measured Values

In order to examine the effectiveness of the IG-SPICE IGBT model, tests were performed for single and paralleled IGBTs with inductive load circuits (see Figs. 5.16 and 5.17). The test conditions were such that the anode voltage was 300 V, and the gate voltage pulse amplitude was 20 V. The external load resistance *RL* was set so that the maximum steady-state current was 10 A. Table 4 shows the nominal values for the IGBT model parameters and the semiconductor device constants.

5.5.1 Single IGBT

The test circuit used to simulate the inductive load operation of a single IGBT is shown in Fig. 5.16. The simulated and measured anode voltage and anode current results are shown in Fig. 5.18. Extensive testing of the device was also performed for all of the circuit conditions presented in [3]. The simulated results of the IG-SPICE IGBT model are nearly identical to the results obtained in [3].

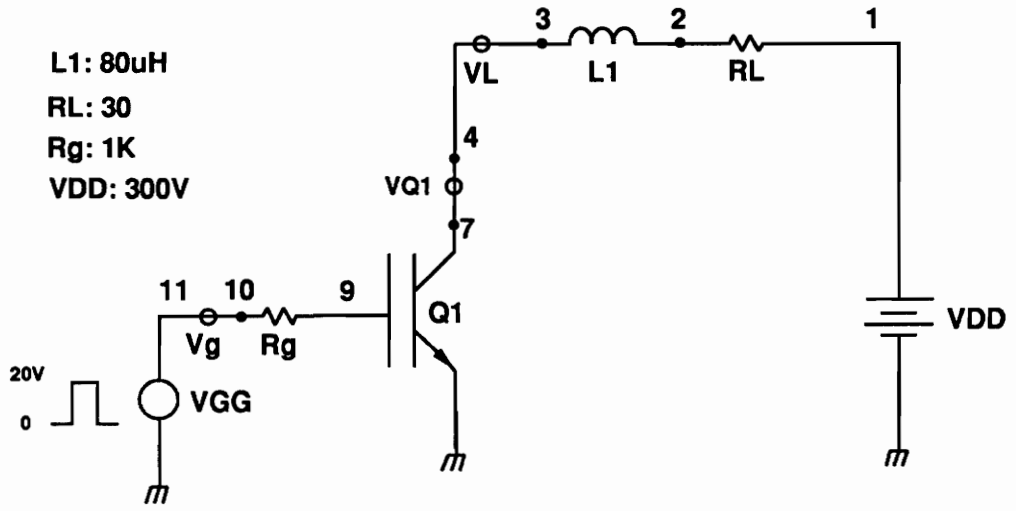


Figure 5.16. Inductive load operation for a single IGBT.

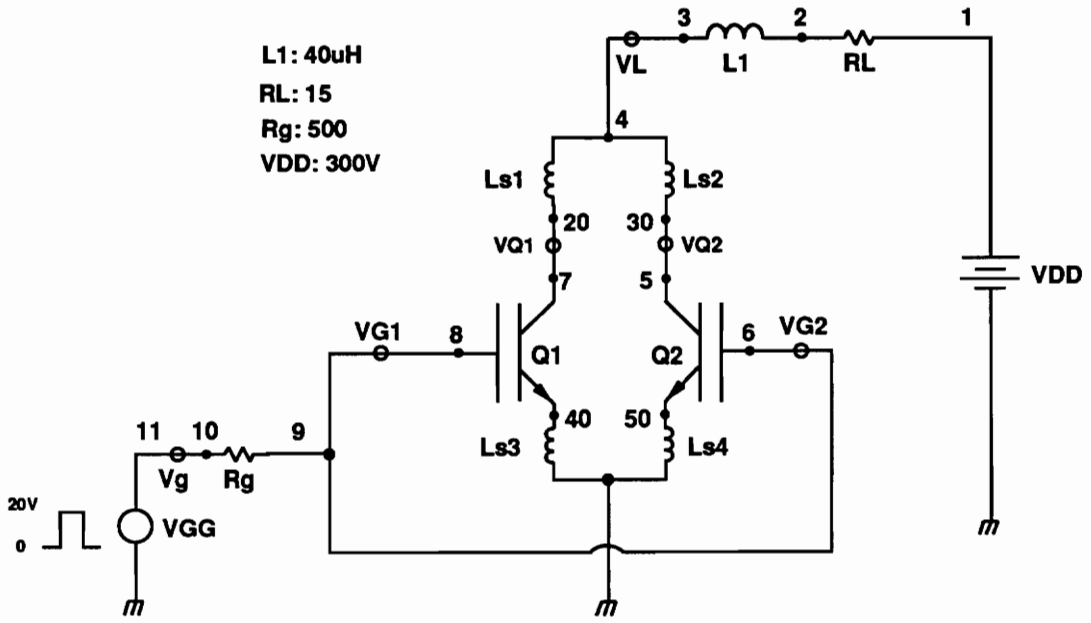
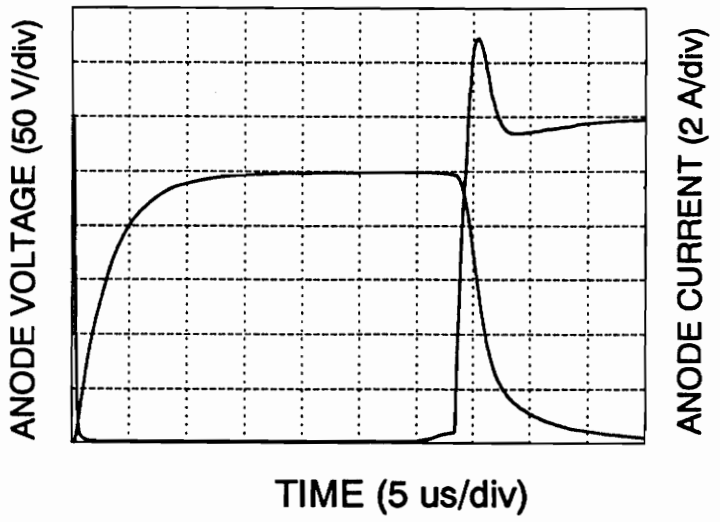
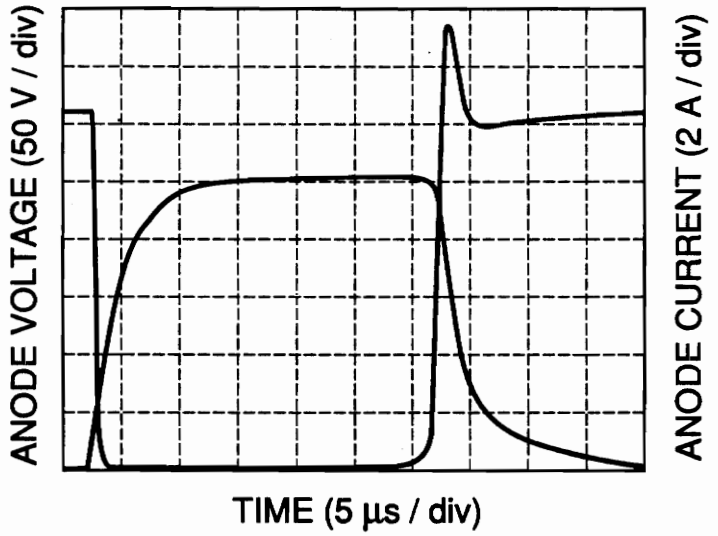


Figure 5.17. Paralleld IGBTs used in inductive load.



(a)



(b)

Figure 5.18. Anode current and voltage waveforms for a singe IGBT switched with an Inductive load: (a) simulated, and (b) measured.

5.5.2 Paralleled IGBT operation

Paralleled IGBTs are used extensively in power modules to obtain higher current ratings [10, 11]. However, the typical process variation of device model parameters within a given device type is significant enough to result in uneven static and dynamic current sharing if the paralleled devices are chosen randomly from a given lot of IGBTs of the same type. Simulations of paralleled IGBTs are given in Figs. 5.19 and 5.20 for variation in device parameters which are representative of a situation which would occur if the devices were not screened for similar parameters and were chosen randomly. The test circuit used to examine the paralleled operation of IGBTs is shown in Fig. 5.17.

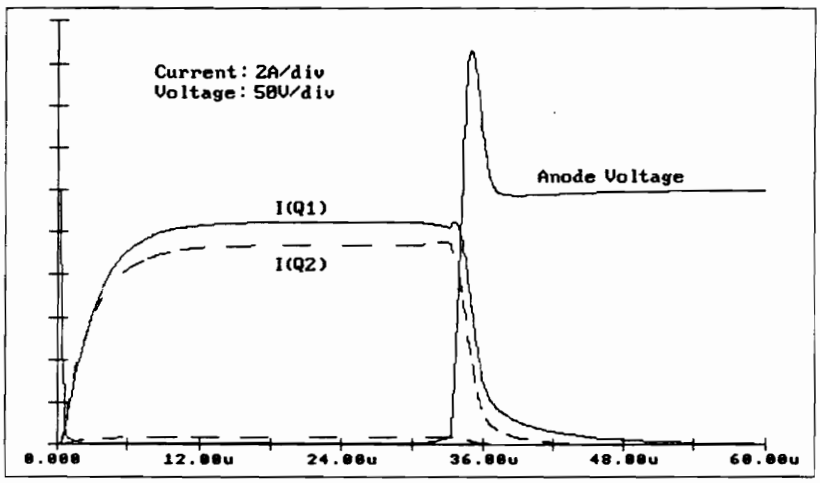
For the paralleled operation, the gate resistances (Rg1 and Rg2), load resistance RL, and the load inductance L1, were chosen so that the devices operated similar to the single IGBT circuit of fig. 5.16 when the nominal parameter values were used for both devices. In order to accomplish this task, the values of L, and RL were reduced by a factor of 2, and the gate resistor values were fixed at 1 kΩ for each device.

In order to observe how the dissimilar parameters affected current sharing of the paralleled IGBTs, the parameters lifetime τ_{HL}, threshold voltage Vt, and transconductances Kp, were varied from the nominal values. These parameters were chosen because the normal process variation of these parameters has the most impact on current sharing for parallel operation.

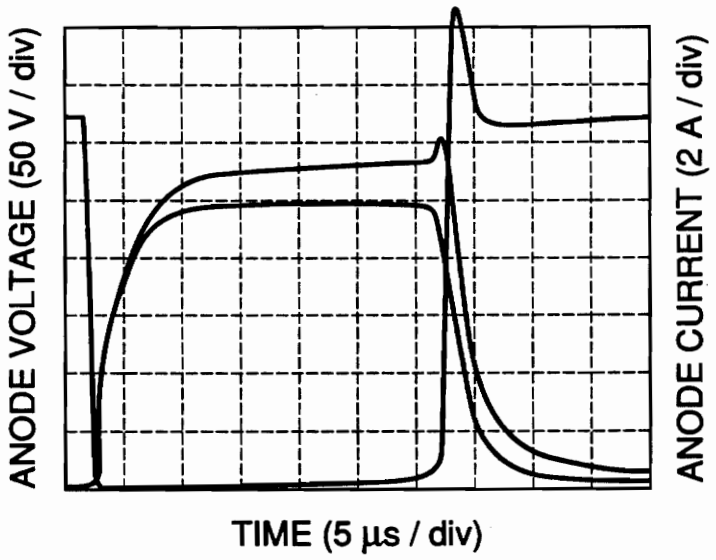
The test results for these parameter variations are shown in Figs. 5.19 and 5.20. Figure 5.19 compares (a) the simulated and (b) the measured anode current and voltage waveforms for paralleled IGBTs where the base lifetime of one of the devices is varied from the nominal values

in Table 4. (ie., τ_{hl} = 2.45 μs for one of the devices). Figure 5.20 compares the (a) simulated and (b) measured anode current and voltage waveforms for parallel operation of IGBTs where one of the devices has threshold voltage and transconductance that are varied from the nominal values (ie., Vt=3.8 V and Kp_{sat} = 0.64 A/V^2 for one of the devices).

The anode voltage and anode current waveforms of the paralleled IGBTs with different device base lifetimes (Fig. 5.19) are similar to those for the single device (Fig. 5.18), with the exception that the static current sharing of the paralleled devices is uneven, and the current tail is smaller for the lower lifetime device. For the devices with different MOSFET threshold voltages and transconductances (Fig. 5.20), a turn-on delay exists for the device with the lower transconductance, and a turn-off current spike exists for the device with the larger transconductance. The turn-on delay occurs for the lower transconductance device because it has a higher resistance than the other device until its gate voltage becomes large enough so that the on-state resistances of both devices are primarily determined by the bipolar emitter-base voltages. The turn-off current spike in the higher transconductance device occurs because the resistance of the low transconductance device becomes larger sooner than for the high transconductnace device, and the inductor current is transferred to the lower resistance, high transconductance device.

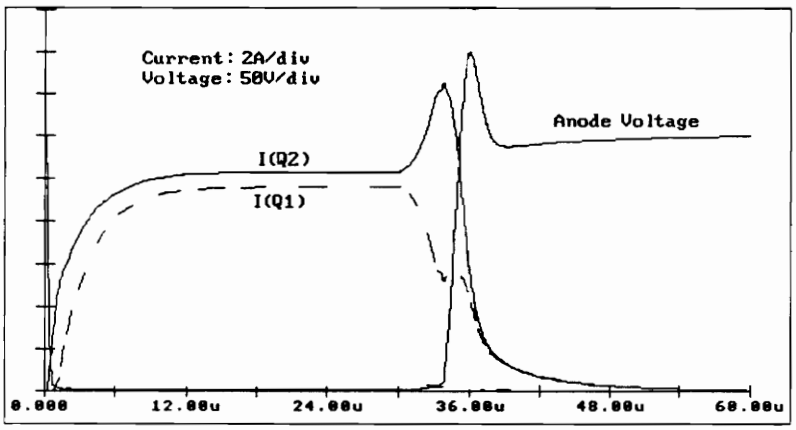


(a)

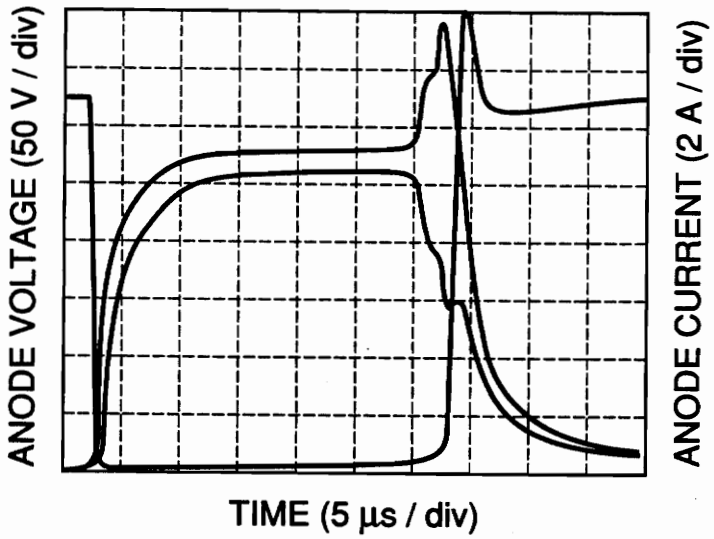


(b)

Figure 5.19. Paralleled IGBTs with variation in Lifetime: (a) simulated, and (b) measured.



(a)



(b)

Figure 5.20. Paralleled IGBTs with threshold voltage and transconductance variation: (a) simulated, and (b) measured.

5.6 Summary

A previously developed physics-based IGBT model is implemented into the IG-SPICE circuit simulator. The IG-SPICE circuit simulator was chosen for this study because it provides the user with programming capability. This programming capability is essential for implementing the complex model equations that are necessary to describe the behavior of the IGBT. When implementing physics-based models into IG-SPICE: 1) the model must be formulated as an interconnection of controlled sources, 2) the variables used to formulate the model must be normalized so that each variable has a comparable absolute error tolerance, and 3) the partial derivatives of the controlled source functions with respect to each controlling variable must be evaluated.

The IG-SPICE IGBT model developed in this paper is verified by comparing the results of the model with experimental results for various circuit operating conditions. The model performs well and describes experimental results accurately for the range of static and dynamic conditions in which the device is intended to be operated. The effectiveness of the IG-SPICE IGBT model is demonstrated by examining the effects of the normal process variation of the model parameters upon the static and dynamic sharing of paralleled IGBTs. The results indicate that the threshold voltage and transconductance variations tend to result in dynamic current spikes, whereas lifetime variations tend to result in uneven current tails. Both lifetime and transconductance variations result in uneven static sharing.

Chapter 6

Conclusions/Future Work

In Chapter 2 , a brief review of IGBT device physical structure and its opteration was presented. This review also included the description specific features of the IGBT device, and its switching characteristc was discussed. From the discussion, it was shown that the IGBT devices obtain higher current density then high power MOSFETs. The most noticeable advantage of the IGBT was the conductivity modulation in the wide base region of the integral PNP bipolar transistor. Because the device exhibits some of the bipolar characteristics, it was shown that one disadvantage of this device was the large current tail which can account for large switch losses.

In Chapter3, a physics-based analytical IGBT model was introduced. It was shown that the model accurately describes the low gain, wide base region of the IGBT device. The distinctive difference of IGBT compared with that of other power devices was that the external base contact was at the collector end of the base. As a result, a large inrush current can flow before the conductivity modulation is introduced in the PNP base of the device. This in effect accurately predicts dynamic saturation of the IGBT device. Also, the description of equivalent analytical circuit was introduced.

In Chapter 3, the parameter extraction algorithm was briefly discussed. It was shown that the large inductive clamped anode voltage circuit was more beneficial when extracting the

parameters for the low high-level base lifetime. The parameters were extracted using the dynamic characteristics of the device.

Chapter 4 described the Spice-related programs, and the discussion concluded that the implementation of this physical model into Spice-based simulation programs was only possible if it was implemented using IG-Spice. Some of the procedures in implementing the controlled dependent polynomial functions were briefly discussed. Also in this chapter, the capabilities of the IG-Spice program were introduced. The IG-Spice is used because the program provides the user with programming capabilities using the Fortran programming language. Most importantly, this subroutine also allows the user to implement differential equations describing the time-rate-of-change of currents and voltages.

The detailed procedures of implementing the analytical model into the IG-Spice was introduced in Chapter 5. Because there are so many complicated equations, simplifications of expressions are desirable in order to ensure better convergence within the IG-Spice program. It was shown in this chapter that the analytical model contained three (3) state equations which described the time rate of voltages and the time-rate-of-change in the base charge. Within these state equations there were five (5) system variables which can be used to express the state equations. It was shown that with the IG-Spice program, the state voltages can be obtained by simply assigning them as node voltages, and only the correct controlled dependent sources needed to be insterted into the branch of IG-Spice IGBT equivalent circuit. In this chapter, several methods of ensuring convergence was discussed: 1) normalize variables so that error tolerence is not exceeded, 2) convert all the controlling variables into current or voltage type, but not both types, and 3) the partial derivatives need to be continuous when making transistion from one state to another.

Also in Chapter 5, simulated results emphsizing the special capabilities of the IG-Spice IGBT model were introduced. Among these were: 1) conductivity modulation, 2) carrier-carrier scattering, and 3) abililty to separate the MOSFET portion from the PNP bipolar section and observe just the MOSFET portion. Finally, the effecitiveness of the model was shown by comparing the simulated results with those of measured values for the single and paralleled opertion of the device with the inductive load. From the testing, it was discussed that the variation in lifetime introduced steady-state current imbalance and dynamic imbalance during the turn-off. The variation of lifetime had little or no effect during the turn-on. Then the results for the variation of transconductance along with the MOSFET channel threshold voltage were discussed. The test results showed that the variation in these two parameters introduced current imbalance during the turn-on and turn-off. The current imbalance in the steady-state was more noticeable, and dynamic current sharing was much worse where it introduced the current spike during the turn-off. From the comparison of the simulated results and the measured results, it showed that the IG-Spice IGBT model proved to effectively predict the behavior of IGBT devices.

For future work, an extensive simuation using power converters is suggested. Also, the model should be tested under more severe conditions to see if it predicts circuit behavior correctly. When implementing the second order of the MOSFET portion of the model, several convergence problems were faced. It is suggested that future work should also include work on better convergence when implementing the complicated second order effects of the device. Also the avalanch breakdown effect still needs to be implemented as soon as possible (it only requires implementation of one more equation).

Appendix A

NOMENCLATURE

A	Device active area(cm^2).
$A_{ds} \equiv A\text{-}A_{gd}$	Body region area (cm^2).
A_{gd}	Gate-drain overlap area (cm^2).
$b \equiv \mu_n/\mu_p$	Ambipolar mobility ratio.
C_{bcj}	Base-collector depletion capacitance (F).
C_{dsj}	Drain-source depletion capacitance (F).
C_{ebj}	Emitter-base depletion capacitance (F).
C_{ebd}	Emitter-base diffusion capacitance (F).
C_{ebq}	Emitter-base capacitance (F).
C_{gd}	Gate-drain capacitance (F).
C_{gdj}	Gate-drain overlap depletion capacitance (F).
C_{gs}	Gate-source capacitance (F).
C_{oxd}	Gate drain overlap oxide capacitance (F).
$D \equiv \frac{2D_nD_p}{(D_n+D_p)}$	Ambipolar diffusivity (cm^2/s).

D_n, D_p	Electron, hole diffusivity (cm^2/s).
I_g	Gate current (A).
I_k	Tail size knee current (A).
I_k^{τ}	Tail decay rate knee current (A).
I_L	Load inductor current (A).
I_{mos}	MOSFET channel current (A).
I_{mos}^{sat}	MOSFET channel saturation current (A).
I_{sne}	Emitter electron saturation current (A).
I_T	IGBT anode current (A).
I_T^{sat}	IGBT anode saturation current (A).
K_p	MOSFET transconductance parameter (A/V^2).
$L \equiv \sqrt{D\tau}$	Ambipolar diffusion length (cm).
L_L	Series load inductance (H).
n_i	Intrinsic carrier concentration.
N_B	Base doping concentration (cm^{-3}).
n_{eff}	Effective base carrier base charge (C).
P_0	Excess carriers at emitter edge of base (cm^{-3}).
q	Electron charge (1.6×10^{-19} C).
Q	Instantaneous excess carrier base charge (C).
Q_B	Background mobile carrier base charge (C).

Q_0	Built-in emitter-base depletion charge (C).
R_b	Conductivity modulated base resistance (W).
R_g	Gate drive resistance (W).
R_L	Series load resistance (W).
V_A	Device anode voltage (V).
V_{AA}	Anode supply voltage (V).
V_{bc}	Applied base-collector voltage (V).
$V_{ds} = V_{bc}$	Applied drain-source voltage (V).
V_{ebq}	Emitter-base capacitor voltage (V).
V_{ebd}	Emitter-base diffusion potential (V).
V_{ebj}	Emitter-base depletion potential (V).
V_{gg}	Gate pulse generator voltage amplitude (V).
V_{gon}	Gate pulse voltage amplitude (V).
V_{gs}	Gate-source voltage (V).
V_T	MOSFET channel threshold voltage (V).
V_{Td}	Gate-drain overlap depletion threshold (V).
W	Quasi-neutral base width (cm).
W_B	Metallurgical base width (cm).
W_{bcj}	Base-collector depletion width (cm).
W_{dsj}	Drain-source depletion width (cm).
W_{gdj}	Gate-drain overlap depletion width (cm).
β_{SS}	Steady-state common emitter current gain.

$\beta_{tr,v}$	Constant anode supply voltage tail size.
ϵ_{si}	Dielectric constant of silicon (F/cm).
μ_{eff}	Effective ambipolar mobility ($cm^2/V \cdot s$)
μ_n, μ_p	Electron, hole mobility ($cm^2/V \cdot s$)
τ_{HL}	Base high-level lifetime (s).

Appendix B

ANALYTICAL EXPRESSIONS FOR IGBT MODEL

Table B.1. IGBT State Equations. [$]

$$\frac{dV_{gs}}{dt} = \frac{I_g}{C_{gs}+C_{gd}} + \frac{C_{gd}}{C_{gs}+C_{gd}} \cdot \frac{dV_{bc}}{dt}$$

$$\frac{dV_{bc}}{dt} = \frac{I_T - \frac{4D_p}{W^2} + \left(1+\frac{1}{b}\right)\left[\frac{C_{gd}}{C_{gs}+C_{gd}} I_g - I_{mos}\right]}{\left(1+\frac{1}{b}\right)\left[C_{dsj} + \frac{C_{gs}C_{gd}}{C_{gs}+C_{gd}} + \frac{C_{bcj}}{3}\frac{Q}{Q_B}\right]}$$

$$\frac{dQ}{dt} = I_{mos} + (C_{dsj}+C_{gd})\frac{dV_{bc}}{dt} - C_{gd}\frac{dV_{gs}}{dt} - \frac{Q}{\tau_{HL}} - \frac{Q^2}{Q_B^2} \cdot \frac{4N_B^2}{n_i^2}$$

[$] All the analytical expressions in this table was derived by Hefner in [6].

Table B.2. Functions of IGBT Sate Variables.

$$N_{scl} = N_B + I_p(W)/(qA\,V_{v_{psat}}) - I_{mos}/(qA\,V_{v_{nsat}})$$

$$W_{gdj} = \sqrt{2\,\epsilon_{si}\,(V_{ds} - V_{gs} + V_{Td})/qN_{scl}}$$

$$W_{dsj} = \sqrt{2\,\epsilon_{si}\,(V_{ds} + 0.6)/qN_{scl}}$$

$$W_{bcj} = \sqrt{2\,\epsilon_{si}\,(V_{bc} + 0.6)/qN_{scl}}$$

$$W = W_B - W_{bcj}$$

$$BV_{cbo} = BV_f \cdot 5.34\text{x}10^{13} \cdot N_{scl}^{-0.75}$$

$$M = 1/\left[1 - (V_{cb}/BV_{cbo})^{BV_n}\right]$$

$$Q_B = qAWN_{scl}$$

$$C_{bcj} \equiv A\,\epsilon_{si}/W_{bcj}$$

$$C_{dsj} = (A - A_{gd})\,\epsilon_{si}/W_{dsj}$$

$$C_{gdj} = A_{gd}\,\epsilon_{si}/W_{gdj}$$

$$C_{gd} = \begin{cases} C_{oxd} & \text{for} \quad V_{ds} \le V_{gs} - V_{Td} \\ C_{oxd}C_{gdj}/(C_{oxd} + C_{gdj}) & \text{for} \quad V_{ds} > V_{gs} - V_{Td} \end{cases}$$

Table B.3. IGBT Current Sources

$$I_p(W) = \left(\frac{1}{1+b}\right) I_T + \left(\frac{b}{1+b}\right) \frac{4D_p}{W^2} Q + \frac{C_{bcj}}{3} \frac{Q}{Q_B} \frac{dV_{bc}}{dt}$$

$$I_n(W) = I_{mos} + I_{mult} + (C_{dsj} + C_{gd}) \frac{dV_{ds}}{dt} - C_{gd} \frac{dV_{gs}}{dt}$$

$$I_g = (C_{gs} + C_{gd}) \frac{dV_{gs}}{dt} + C_{gd} \frac{dV_{bc}}{dt}$$

$$I_T = I_n(W) + I_p(W)$$

$$I_{gen} = 2q\, n_i\, A W_{bcj} / \tau_{HL}$$

$$I_{mult} = M \cdot I_{gen} + (M-1) \cdot (I_p(W) + I_{mos})$$

$$I_{mos} = \begin{cases} 0 & \text{for} \quad V_{gs} < V_T \\ \dfrac{K_{plin}\left[(V_{gs} - V_T) V_{ds} - \dfrac{K_{plin} V_{ds}^2}{2 K_{psat}}\right]}{\left[1 + \theta (V_{gs} - V_T)\right]} & \text{for} \quad V_{ds} \le (V_{gs} - V_T) \dfrac{K_{plin}}{K_{psat}} \\ \dfrac{K_{psat} (V_{gs} - V_T)^2}{2\left[1 + \theta (V_{gs} - V_T)\right]} & \text{for} \quad V_{ds} > (V_{gs} - V_T) \dfrac{K_{plin}}{K_{psat}} \end{cases}$$

Table B.4. Variables of IGBT Base-Emitter Voltage.

$$1/\mu_c = \left[\overline{\delta_p}\ln(1+\alpha_2\left(\overline{\delta_p}\right)^{-2/3}\right]/\alpha_1$$

$$\mu_{nc} = 1/(1/\mu_n + 1/\mu_c)$$

$$\mu_{pc} = 1/(1/\mu_p + 1/\mu_c)$$

$$\mu_{eff} = \mu_{nc} + \mu_{pc}\cdot Q/(Q+Q_B)$$

$$L = \sqrt{D_{ccs}\tau_{HL}}$$

$$P_0 = Q/\left(qALtanh\frac{W}{2L}\right)$$

$$\overline{\delta_p} = P_0\sinh(W/2L)/\sinh(W/L)$$

$$Q_0 = A\sqrt{2\epsilon_{si}\ qN_B 0.6}$$

$$n_{eff} = \frac{\frac{W}{2L}\sqrt{N_B^2 + P_0^2\,csch^2\left(\frac{W}{2L}\right)}}{\operatorname{arctanh}\left[\frac{\sqrt{N_B^2 + P_0^2\,csch^2\left(\frac{W}{L}\right)}\tanh\left(\frac{W}{2L}\right)}{N_B + P_0\,csch\left(\frac{W}{L}\right)\tanh\left(\frac{W}{2L}\right)}\right]}$$

Table B.5. Conductivity Modulation.

$$R_b = \begin{cases} W / q\mu_{nc} A N_B) & \text{for} \quad Q < 0 \\ W / q\mu_{eff} A n_{eff}) & \text{for} \quad Q \geq 0 \end{cases}$$

$$Vebj = 0.6 - (Q - Q_0)^2 / (2qN_B \in_{si} A^2)$$

$$V_{ebj} = \frac{kT}{q} \ln\left[\left(\frac{P_0}{n_i^2} + \frac{2}{N_B}\right)(N_B + P_0)\right] - \frac{D_{ccs}}{\mu_{nc}} \ln\frac{P_0 + N_B}{N_B}$$

$$V_{ebq} = \begin{cases} V_{ebj} & \text{for} \quad Q < 0 \\ \min(V_{ebj}, V_{ebd}) & \text{for} \quad Q_0 > Q \geq 0 \\ V_{ebd} & \text{for} \quad Q \geq 0 \end{cases}$$

$$V_{eb} = V_{ebq} + I_T \cdot R_b$$

$$V_A = V_{eb} + V_{cb}$$

$$\frac{dQ}{dt} = In(W) - \frac{Q}{\tau_{HL}} - \frac{Q^2}{Q_B^2} \cdot \frac{4N_B^2}{n_i^2}$$

Appendix C

Partial Derivative Expressions for the Coefficients of IG-Spice IGBT Functions

In this section the partial derivatives which are needed for the implementation of the analytical expressions are derived and presented for each functions. These functions describe the controlled dependent current sources or controlled dependent voltage sources. Derivations of coefficients for each function will be done in the order which they appear in the IG-Spice IGBT subroutines.

C.1 Function IMOS

Function Imos describes the MOSFET characteristics of the IG-Spice IGBT model, and it is implemented as the current controlled current source GImos which is described in the input file shown in the Appendix C (which lists the nodes and controlled dependent functions). The MOSFET portion of the IGBT describes two states which describe the linear and saturation regions of the device.

For the linear region:

$$V_{ds} \le V_{gs} - V_T, \tag{C.1}$$

$$Imos = K_p (V_{gs} - V_T) V_{ds} - K_p \frac{V_{ds}^2}{2}, \tag{C.2}$$

$$Coef(2) = \frac{\partial Imos}{\partial V_{gs}} = K_p \cdot V_{ds}, \tag{C.3}$$

$$Coef(3) = \frac{\partial Imos}{\partial V_{ds}} = K_p (V_{gs} - V_T) - K_p \cdot V_{ds}. \tag{C.4}$$

The IG-Spice expression is:

$$Imos = Coef(1) + Coef(2) \cdot V_{gs} + Coef(3) \cdot V_{ds}, \tag{C.5}$$

and

$$\begin{aligned} Coef(1) &= Imos - Coef(2) \cdot V_{gs} - Coef(3) \cdot V_{ds}. \\ &= (-K_p \cdot V_{gs} \cdot V_{ds}) + (0.5 \cdot K_p \cdot V_{ds} \cdot V_{ds}) \end{aligned} \tag{C.6}$$

For the saturation region:

$$Vds > Vgs - VT, \tag{C.7}$$

and

$$Imos = Kp(Vgs - VT)^2 / 2., \tag{C.8}$$

where

$$Coef(2) = \frac{\partial Imos}{\partial Vgs} = Kp \cdot (Vgs - VT), \tag{C.9}$$

and

$$\begin{aligned} Coef(1) &= Imos - Coef(2) \cdot Vgs \\ &= 0.5 \cdot Kp(VT \cdot VT - Vgs \cdot Vgs) \end{aligned} \tag{C.10}$$

C.2 Function IGD

This function describes the nonlinear voltage dependent drain-to-gate feedback capacitance C_{gd}. There are two states for the IMOS function, but finding the partial derivatives for two different case is not necessary. This capacitance can be expressed as a voltage controlled current source, and the expression can be written as:

$$i_{gd} = Cgd\frac{dVgd}{dt}, \tag{C.11}$$

which can be rewritten as:

$$i_{gd} = Cgd(Vgd - Vgdo) \cdot ODT. \tag{C.12}$$

Recall that the variable ODT is the same expression as 1/dt. Therefore only the partial derivatives of Eq.(B.12) need to be found with respect to V_{gd}, and only the appropriate capacitance values need to be assigned depending on its states. The coefficients are expressed as:

$$\mathrm{Coef}(2) = \frac{\partial i_{gd}}{\partial V_{gd}} = C_{gd} \cdot \mathrm{ODT}, \tag{C.13}$$

and

$$\mathrm{Coef}(1) = i_{gd} - \mathrm{Coef}(2) \cdot V_{gd} = -C_{gd} \cdot V_{gdo} \cdot \mathrm{ODT}. \tag{C.14}$$

The capacitance C_{gd} is expressed as following:

For the first case $(Vds \leq Vgs - VT)$,

$$C_{gd} = C_{oxd}, \tag{C.15}$$

and for the second case $(Vds > Vgs - VT)$,

$$C_{gd} = \frac{C_{oxd} C_{gdj}}{(C_{oxd} + C_{gdj})} = C_{oxd} / (1.0 + C_{oxd} / A_{gd} / e_{si} \cdot W_{gdj}), \tag{C.16}$$

where the final expression for Eq. (B.16) in the above form is to ensure convergence when there is a value near zero. This expression will ensure that equation is never divided by zero.

C.3 Function IDS

This function describes the drain-to-source capacitance, and its expression can be expressed just as C_{gd}, only the system variable Vds is used. The capacitance is expressed as voltage dependent current source:

$$i_{ds} = C_{dsj} \cdot \frac{V_{ds}}{dt}, \tag{C.17}$$

and its IG-Spice form is:

$$i_{ds} = C_{dsj} \cdot (V_{ds} - V_{dso}) \cdot ODT, \tag{C.18}$$

and

$$Coef(2) = \frac{\partial i_{ds}}{\partial V_{ds}} = C_{dsj} \cdot ODT, \tag{C.19}$$

where

$$Coef(1) = i_{ds} - Coef(2) \cdot V_{ds} = -C_{dsj} \cdot V_{dso} \cdot ODT. \tag{C.20}$$

The other expressions are the functions of the system variables, and they are implemented as just as shown in Appendix B.

C.4 Function IQ

This function describes the third part of the equation describing time-rate-of change of base charge, and it is designated as Fine in the IG-Spice IGBT equivalent circuit. It is designated as variable IQ because the current flowing is dependent on the base charge. This function is expressed voltage controlled current source, where all the controlling variables are currents that are converted to voltages (see IG-Spice IGBT equivalent circuit). This expression is:

$$i_Q = \frac{Q^2}{Q_B^2} \cdot \frac{4N_B^2}{n_i^2} \cdot I_{sne}, \tag{C.21}$$

where

$$Coef(2) = \frac{\partial i_Q}{\partial Q} = \frac{2Q}{q_B^2} \cdot \frac{4N_B^2}{n_i^2} \cdot I_{sne}, \tag{C.22}$$

and

$$Coef(1) = i_Q - Coef(2) \cdot Q = -\frac{Q^2}{Q_B^2} \cdot \frac{4N_B^2}{n_i^2} \cdot I_{sne}. \tag{C.23}$$

But the variable Q is a normalized variable which was discussed in Chapter 5. The normalized variable was:

$$Q' = Q \cdot 10^6, \tag{C.24}$$

and

$$Q = Q' \cdot 10^{-6}. \tag{C.25}$$

In the subroutine the variable Qt was assigned the value Q' x 10^{-6}. Therefore, the expressions for the coefficients need to be rewritten as:

$$\mathrm{Coef}(2) = \frac{2Qt}{Q_B^2} \cdot \frac{4N_B^2}{n_i^2} \cdot I_{sne} \cdot 10^{-6}, \tag{C.26}$$

and

$$\mathrm{Coef}(1) = -\frac{Qt^2}{Q_B^2} \cdot \frac{4N_B^2}{n_i^2} \cdot I_{sne}. \tag{C.27}$$

The expression for Coef(2) is multiplied by the factor 10^{-6} because the system variable Q by default is normalized value. The expression for Coef(1) need not be multiplied by the factor 10^{-6} because within the function the variable Qt is dfined so that it would give the denormalized value of Q. Recall that the output of the function is represented as:

$$i_Q = \mathrm{Coef}(1) + \mathrm{Coef}(2) \cdot Q', \tag{C.28}$$

where the Q' is the controlling variable; in order to obtain the correct value of Q, the expression for the Coef(2) must be multiplied by the factor 10^{-6}. Therefore the correct output expression should be of the form:

$$i_Q = \mathrm{Coef}(1) + \mathrm{Coef}(2) \cdot Q' \cdot 10^{-6}. \tag{C.29}$$

C.5 Function IA

This function is simply a first part of the expression describing the collector hole current of the PNP bipolar transistor, and it is expressed as:

$$i_A = \left(\frac{1}{1+b}\right) \cdot I_T, \tag{C.30}$$

where the variable (b) is the expression describing the ambipolar transport, and I_T is the total current of the IGBT device and also is the controlling variable. When the partial with respect to I_T is found, the following results for the coefficients of the function:

$$Coef(2) = \frac{\partial i_A}{\partial I_T} = \frac{1}{1+b}, \tag{C.31}$$

$$Coef(1) = 0, \tag{C.32}$$

and the output expression for this function is equal to:

$$i_A = Coef(2) \cdot I_T. \tag{C.33}$$

C.6 Function IB

This function is the output expression for the second portion of the collector hole current expression as shown in Appendix A. Its expression is given as:

$$i_B = \left(\frac{b}{1+b}\right) \cdot \frac{4Dp}{W^2} \cdot Q', \tag{C.34}$$

and

$$Coef(2) = \frac{\partial i_B}{\partial Q} = \left(\frac{b}{1+b}\right) \cdot \frac{4Dp}{W^2} \cdot 10^{-6}, \tag{C.35}$$

$$Coef(1) = 0, \tag{C.36}$$

where

$$i_B = Coef(2) \cdot Q' \cdot 10^{-6}. \tag{C.37}$$

C.7 Function IC

This is the final expression of the collector hole current, which is:

$$i_C = \frac{C_{bcj}}{3} \cdot \frac{Q' \cdot 10^{-6}}{Q_B} \cdot \frac{dV_{bc}}{dt}, \tag{C.38}$$

and it can be written as;

$$i_C = \frac{C_{bcj}}{3} \cdot \frac{(V_{bc} - V_{bco}) \cdot ODT}{Q_B} \cdot Qt, \tag{C.39}$$

where

$$Qt = Q' \cdot 10^{-6}. \tag{C.40}$$

The Coefficients of the function are:

$$Coef(3) = \frac{\partial i_C}{\partial Q'} = \frac{C_{bcj}}{3} \cdot \frac{(V_{bc} - V_{bco}) \cdot ODT}{Q_B} \cdot 10^{-6}, \tag{C.41}$$

$$Coef(2) = \frac{\partial i_C}{\partial V_{bc}} = \frac{C_{bcj}}{3} \cdot \frac{Qt}{Q_B} \cdot ODT, \tag{C.42}$$

and

$$Coef(1) = i_C - Coef(2) \cdot V_{bc} - Coef(3) \cdot Q', \tag{C.43}$$

where

$$i_C = Coef(1) + Coef(2) \cdot V_{bc} + Coef(3) \cdot Q'. \tag{C.44}$$

C.8 Function VEB

This function describes several special features of the IGBT. Besides finding the emitter-base voltage, it calculates the base resistance R_b, carrier scattering CCS, and checks if the model behaves just as MOSFET. As a result, there are many complicated equations which have been implemented in this function. The output of the function is the voltage value, and the function is described by the voltage controlled voltage source. Therefore, the system variables that were current type had to be transformed into voltage type (see right hand corner of IG-Spice IGBT equivalent circuit). Appendix A shows many of the complicated analytical expressions which had to be implemented for this function.

The VEB function is programmed to output the emitter-base voltage which is represented by the expression:

$$V_{eb} = V_{ebq} + I_T \cdot R_b. \tag{C.45}$$

Therefore, this function must pass a voltage value expressed eq. (B.45).

In this function there are four cases which need to be checked:

1. case if it is MOSFET,
2. case for $Q < 0$,
3. case for $Q_0 > Q \geq 0$, and
4. case for $Q > 0$.

For the case when the device is behaving just as MOSFET, the output expression for the function is:

$$V_{eb} = I_T \cdot R_b. \tag{C.46}$$

In the subroutine (see line 800 in source code), there are three argument vectors. As discussed in Chapter 4, the output expression for the IG-Spice subroutine is in the form:

$$\text{Output} = \text{Coef}(1) + \text{Coef}(2) \cdot \text{Arg}(1) + \text{Coef}(3) \cdot \text{Arg}(2) ... + \text{Coef}(n) \cdot \text{Arg}(n) \tag{C.47}$$

where Arg(n) represents the controlling system variables discussed in Chapter 5. In the subroutine, the current variable I_T, is defined as Vit and is equal to vector Arg(3). The partial expression with respect to variable I_T is:

$$Coef(4) = \frac{\partial V_{eb}}{\partial I_T} = R_b, \tag{C.48}$$

and

$$Coef(1)....Coef(3) = 0. \tag{C.49}$$

Ordinarily, Coef(1) could have been assigned the value of Coef(4) and Coef(4) assigned as zero. But since there are four cases in this function, and three other cases contain Coef(4), all the cases need to have Coef(4). This is necessary in order to ensure continuous transition between different conditions, and to ensure better convergence.

For the second condition (Q < 0):

$$V_{ebj} = 0.6 - (Q - Q_0)^2 / (2qN_B \in_{si} A^2) + I_T \cdot R_b, \tag{C.50}$$

where

$$R_b = \frac{W}{(q\mu_{nc} A N_B)}, \tag{C.51}$$

$$Coef(4) = \frac{\partial V_{eb}}{\partial I_T} = R_b, \tag{C.52}$$

$$Coef(3) = 0, \tag{C.53}$$

$$Coef(2) = \frac{\partial V_{eb}}{\partial Q} = -(Q - Q_0) \cdot K \cdot 10^{-6}, \tag{C.54}$$

where

$$K = 1.0 / q / N_B / A^2 / \in_{si}, \tag{C.55}$$

and

$$Coef(1) = (0.5 \cdot Q \cdot Q \cdot K) - (0.5 \cdot Q_0 \cdot Q_0 \cdot K) + 0.6. \tag{C.56}$$

Recall that in the subroutine:

$$Q = Qt = 10^{-6} \cdot Q'. \tag{C.57}$$

The IG-Spice output expression is:

$$V_{eb} = Coef(1) + Coef(2) \cdot Q' + Coef(3) \cdot I_T. \tag{C.58}$$

Cases 3 and 4 are combined in the subroutine, and its expression is:

$$V_{eb} = V_{ebj} + I_T \cdot R_b, \tag{C.59}$$

and this expression describes the forward biased condition of the IGBT device. In the forward biased state, there are two states where the base-emitter junctiion voltage is dependent upon: 1) due to the diffusion, and 2) due to depletion. When diffusion capacitance is dominant, the expression becomes:

$$V_{eb} = V_{dif} + I_T \cdot R_b, \tag{C.60}$$

where

$$V_{dif} = \frac{kT}{q} \ln\left[\left(\frac{P_0}{n_i^2} + \frac{1}{N_B}\right)(N_B + P_0)\right] - \frac{D_{ccs}}{\mu_{nc}} \ln\frac{P_0 + N_B}{n_i^2}, \tag{C.61}$$

and

$$R_b = \frac{W}{(q\mu_{eff} An_{eff})}. \tag{C.62}$$

Equation (B.61) is rewritten as :

$$Vdif = Ut \cdot \ln\left[\left(\frac{P}{n_i^2}+\frac{1}{N_B}\right)(N_B+P_0)\right]-\frac{D_{ccs}}{\mu_{nc}}\ln\frac{P+N_B}{n_i^2}\cdot I_{sne}, \tag{C.63}$$

where

$$P = Qt / A / L / tnh / q, \tag{C.64}$$

and

$$Ut = \frac{kT}{q}. \tag{C.65}$$

Equation (B.62) is very complicated, and the variable P contains the system variable Q, which needs to be considered in order to find partial expression of Eq. (B.62) with respect to Q. Therefore, the chain rule is used to find the partial expressions for the Coef(2).

Following are the expressions for this routine:

$$Coef(4) = \frac{\partial V_{eb}}{\partial I_T} = R_b, \tag{C.66}$$

$$Coef(3) = 0, \tag{C.67}$$

$$Coef(2) = \frac{\partial V_{eb}}{\partial P} = Ut \cdot \left[\frac{(2P+N_B)N_B+n_i^2}{(P+N_B)\left(PN_B+n_i^2\right)}\right]\cdot dP - \frac{D}{\mu_{nc}(N_B+P)}\cdot dP, \tag{C.68}$$

where

$$dP = \frac{\partial P}{\partial Q} = (Q / A / L / \tanh / q) \cdot 10^{-6}. \tag{C.69}$$

In the subroutine the following substitutions are made in order to simplify the expression:

$$Fa = Ut \cdot \left[(2P + N_B) + n_i^2 \right], \tag{C.70}$$

$$Fb = (P + N_B)\left(N_B P + n_i^2 \right), \tag{C.71}$$

$$Fc = \frac{dP \cdot D}{\left[\mu_{nc} (N_B + P) \right]}, \tag{C.72}$$

$$dVebj = \frac{Fa}{Fb - Fc} = Coef(2), \tag{C.73}$$

and

$$Coef(1) = Vdif - dVebj \cdot Q'. \tag{C.74}$$

The final expression is:

$$V_{eb} = Coef(1) + Coef(2) \cdot Q' + Coef(4) \cdot I_T. \tag{C.75}$$

When depletion capacitance is dominant, the expressions is:

$$V_{eb} = I_T \cdot R_b + V_{dep}, \tag{C.76}$$

and the expression is the same as in the case when Q < 0.

Appendix D

PROGRAM DESCRIPTION

The subroutine for the IG-Spice IGBT model contains several functions which interact with the internal routines of IG-Spice simulation program. The functions which are present in the IG-Spice IGBT subroutines are:

Function FNNAME,
Function FPNAME,
Function ROOT,
Function Dccs, and
Subroutine FORTFN,

where the IG-Spice functions (IMOS, IGD, IDS, IQ, IA, IB, IC, and VEB) are contained in the subroutine FORTFN.

The function FNNAME was discussed in Chapter 4, and it will not be discussed in this section. The remaining functions; FPNAME, ROOT, Dccs, and the IGBT functions which describe the controlled dependent current voltage sources.

D.1 Function FPNAME

This function, like the FNNAME, is supplied by the IG-Spice program. The application of this function is to behave as variable checker. All the variables which are used by the IG-Spice IGBT functions are defined here. For example, there are twenty-one (21) variables which need to be defined, so these variables need not to be typed in every time different functions are being executed. Before any IGBT functions are executed, this routine constantly checks for the assigned variables and changes the value if the user has defined it to be different from the default values. Below is the common variables which are passed to IGBT functions:

variables	default values	units	Description
t	7.1e-6	(s)	---- base high-level lifetime
Wb	0.0093	(cm)	---- metallurgical base width
Nb	2.0e4	(cm^3 * E-10)	---- base doping concentration
A	0.1	(cm^2)	---- device active area
Isne	6.5e-14	(A)	---- emitter electron saturation current
Vt	5.0	(V)	---- MOSFET channel threshold voltage
Kp	0.38	(A/V^2)	---- MOSFET transconductance
Cgs	0.6e-9	(F)	---- gate-source capacitance
Agd	0.05	(cm^2)	---- gate-drain overlap area
Coxd	1.6e-9	(F)	---- gate-drain overlap oxide capacitance
ccsflg	-1.0	(+/-)	---- carrier-carrier scattering flag
sclflg	-1.0	(+/-)	---- velocity saturation flag
Vtd	0.0	(V)	---- gate-drain overlap depletion thresh.
Vnsat	1.0e7	(cm/s)	---- electron saturation velocity
Vpsat	1.0e7	(cm/s)	---- hole saturation velocity.

The variables listed above can be changed from device to device as the user defines them. The remaining parameters are physical constants of silicon and are assumed to remain unchanged:

Ut	0.0259	---- thermal potential
ni	1.45	---- intrinsic carrier concentration
Un	1500.0	---- electron mobility
Up	450.0	---- hole mobility
q	1.7e-9	---- electron charge
esi	8.854e-14*11.9	----dielectric constant of silicon,

where all of the densities are normalized to E-10, and the electron charge q is normalized to E+10.

The sample format for defining variables within the function is given by:

```
DIMENSION PIGBT(21),VIGBT(21)
DATA NIGBT /21/
DATA PIGBT /'t','Wb','Nb','A','Isne','Vt','Kp','Cgs','Agd',
+          'Coxd','ccsflg','sclflg','Vtd','Vnsat','Vpsat',
+          'Ut','ni','Un','Up','q','esi'/
DATA VIGBT /7.1e-6,0.0093,2.0e4,0.1,6.5e-14,5.0,0.38,0.6e-9,
+          0.05,1.6e-9,-1,-1,0.0,1.0e7,1.0e7,0.0259,1.45,
+          1500.0,450.0,1.6e-9,1.05e-12/
```

The dimension is the number of variables which need to be defined and saved. In this example, there are twenty-one (21) variables, and twenty-one (21) data values. The input order of variables and data that it represents *must be in the same order.* When the program is executed the function checks for any change in the defined variables, and if there is any change to any variable, it then assigns the new data to that variable, and these data are passed to the IGBT model subroutine. Below is the example of how the data are extracted from the function FPNAME:

```
t=      Data(1)
Wb=     Data(2)
Nb=     Data(3)
A=      Data(4)
Isne=   Data(5)
Vt=     Data(6)
Kp=     Data(7)
Cgs=    Data(8)
Agd=    Data(9)
Coxd=   Data(10)
ccsflg= Data(11)
sclflg= Data(12)
Vtd=    Data(13)
Vnsat=  Data(14)
Vpsat=  Data(15)
ni=     Data(17)
Un=     Data(18)
Up=     Data(19)
q=      Data(20)
esi=    Data(21).
```

Note that the name of the variable and the data it represents must be in the same sequence, or the wrong data value can be assigned to the defined variables. The variable name can be changed to different names when they are being accessed from the FPNAME function. It is desirable that these data values are accessed before the first function is executed. In this case, the data are excessed in the IMOS function because this function is executed before any others, and this accessed data is then made available to other functions by using the COMMON definition in the subroutine FORTFN.

For example, the common statement "IGBTpar" is used to have all the variables and its values available to other functions:

```
      COMMON /IGBTpar/ t,Wb,Nb,A,Isne,Vt,Kp,Cgs,Agd,Coxd,ccsflg,
     &                 sclflg,Vtd,Vnsat,Vpsat,Ut,ni,Un,Up,q,esi,Bvn,
     &                 Bvf,Vcb,Qt/
```

Therefore, any other subroutines which need to use these variables need to have the same common statement along with the variable names. This method is desirable so that redundancy of typing is reduced, and this method reduces error which is associated with typing.

In order to change any of the data, they need to be entered during the first IGBT model function call. For example, in the IGBT data file (IGBT subcircuit), the first function is the GIMOS. Therefore, the change of data for the defined variables is done as follows:

```
      GIMOS  7 60 POLY(2) (30,60) (2,60) IMOS(Vt=5.6,t=1.5E-6).
```

In this example the threshold voltage is assigned the voltage of 5.6 V, and the carrier lifetime is assigned the value of 1.5E-6 seconds. The order of data can be entered in any sequence.

D.2 Functions ROOT /Dccs

The function ROOT is a modified translation of the Algol 60 Procedure Zero given in Richard Brent's, Algorithms for Minimization Without Derivatives, Prentice-Hall, Inc., (1973). This function finds the zero of the function that is passed to it and is called during the execution of function VEB. This function along with the function Dccs is only called during the emitter-base voltage function. The function Dccs finds the carrier carrier diffusivity during the execution of VEB function. (The VEB function description details this further.)

The rest of the functions that are described below are contained within the subroutine FORTFN, and they are the actual IG-Spice IGBT model routines used to emulate the IGBT device characteristics. In the following discussions the variables are defined as:

Vgs ---- gate-source voltage,
Vds ---- drain-source voltage,
Vcb ---- collector-base voltage,
Vipw ---- voltage representation of collector hole current Ip(W),
Vimos ---- voltage representation of MOSFET channel current Imos,
Qn ---- normalized charge value which is equal VQe6 (see Fig. 5.2),
Qt ---- denormalized charge equal to Q which is defined as (Qn*1.0e-6),
Nscl ---- collector-base space charge density,
Wdsj ---- drain-source depletion capacitance, and
Wgdj ---- gate-drain depletion capacitance.

D.3 Function IMOS

This function describes the MOSFET channel current of the IGBT device. Because this function is the first function to be executed by the subroutine FORTFN, the data for the variables which are needed by the other functions need be excessed at this time. Since the common statement is used in the subroutine FORTFN, the excessed data will be made available to other functions because they are all executed inside the subroutine FORTFN. The IMOS function describes the MOSFET characteristics for the linear and saturation region of the device. The controlling variables for this routine are Vgs and Vds, and they are assigned an appropriate argument vector [ARG(n)]. Here, the Vgs is assigned the Arg(!) because its voltage was entered first in the IGBT subcircuit data file (see Appendix E. where GIMOS is indicated). (The method of entering these controlling variables was discussed in Chapter 4.)

D.4 Function IGD

This function describes the nonlinear gate-drain feedback capacitance of the IGBT device. The nonlinearity of the capacitance is dependent upon the time-rate-of-change gate-drain voltage. The function will check to see if time is equal to zero (indicating DC biased condition), and if it is zero, it is returned without any further execution. But during the transient analysis, it will emulate the feedback capacitance by finding the current flowing through the capacitance. This routine is shown in line 200 in the source code (see Appendix E).

This function has five (5) controlling variables: Vgd, Vgs, Vds, Vipw, and Vimos, where Vipw and Vimos are the voltages representing the current values of the Ip(W) and In(W). Recall that the

controlling variables need to be of one type, either voltage or current, but not both type. The currents had to be converted to voltage because the collector-base space charge density, which describes the change in the gate-drain overlap depletion width, needed to be found, and this depletion width determine the nonlinear feedback capacitance Cgd.

Remember that the values Nscl and Wgdj are considered as constant expressions, and only the partial expression of the current flowing through the gate-drain capacitance is found. But in reality they are constantly changing because the voltages and currents change with time.

D.5 Function IDS

This routine describes the voltage-dependent nonlinear capacitance of drain-source, of the IGBT device, and is indicated in line 300 of source code. The function behaves similar to the previous function IGD, except the function has three controlling variables; Vds, Vipw, Vimos, and needs drain-source depletion width in order to find the correct drain-source capacitance, Cdsj.

D.6 Function IQ

This function describes the recombination due to the injection of electrons into the emitter of the IGBT device, and its output is the current value to the voltage controlled current source indicated by the variable FIne in the IG-Spice IGBT equivalent circuit (see Fig. 5.2). This function has the following controlling variables: Qn, Vds, Vipw, and Vimos. The variables that are needed to find the correct current values are: Nscl, Qb (background carrier charge in undepleted base), and W (quasi neutral base width).

D.7 Function Ia

This function describes the coupling between the transports of electrons and holes for ambipolar transport, and is the first term of the equation describing the collector hole current Ip(W). This function is dependent upon just the total device current (It). The variable b represents the ambipolar mobility ratio between the electron and hole. The function is represented by the current controlled current source and is indicated by the expression Fipa in the IG-Spice IGBT equivalent circuit.

D.8 Function Ib

This function represents the high-level injection charge control term of the collector hole current expression. The function is described as voltage controlled current source, and is represented by Gipb in the equivalent circuit. In the subroutine FORTFN, the routine is defined in line 600 which shows the controlling variables along with the variables Dp (hole diffusivity) and b (mobility ratio). The function supplies current value to the main circuit.

D.9 Function Ic

This function describes the last part of the collector hole current expression, and it describes the redistribution of carriers for the moving boundary condition in the collector-base region. This function is dependent on the time-rate-of-change in base-collector voltage and the base charge. The changing variables Wbcj, W, Qb, and Cbcj need to be calculated in order to correctly describe the redistribution of the carriers for the moving boundary. The current value is passed

to the main circuit, and is represented by the variable Gipc in the IG-Spice IGBT equivalent circuit.

D.10 Function VEB

The function VEB evaluates the IGBT conductivity modulated base resistance and the emitter-base junction voltage. The controlling variables of this function are:

Qn ---- normalized charge variable and is represented by VQe6 in the IG-Spice IGBT equivalent circuit,

Vcb ---- base-collector voltage, and

Vit ---- voltage representation of the total device current, It.

This function checks if the device is functioning just as MOSFET or as a complete IGBT device. The device will behave as an MOSFET if the base lifetime (t) is assigned the value -1 by the user. Also, the routine checks if the carrier carrier scattering need to be found: if the flag ccsflg is assigned the value -1, the carrier scattering will not be simulated. But if the ccsflg is assigned the positive value of 1.0, the function will evaluate the diffusivity due to the carrier-carrier scattering. When ccsflg is set to 1.0, the routine will call the external function Dccs, and the routine Root.

This VEB subroutine calculates the following variables which are used locally:

W ---- quasi-neutral base width,

Wcbj ---- collector-base depletion width,

L ---- ambipolar diffusion Length,

P ---- carrier concentration at the emitter edge of the base,
Pmid ---- carrier concentration at the center of base,
Unc ---- electron mobility including carrier-carrier scattering,
Upc ---- hole mobility including carrier-carrier scattering,
Ucinv ---- component of inverse mobility due to carrier-carrier scattering,
wl ---- w/L,
cosch ---- hyperbolic cosecant of w/l,
tnh ---- hperbolic tangent of w/1/2,
cth ---- hyperbolic cotangent of w/l,
Ueff ---- low-, high-level injection effective mobility,
Navg ---- radical in the Neff expression,
x ---- used to evaluate **arctnh** using log identity,
arctnh ---- inverse hyperbolic tangent in Neff expression,
Vdep ---- emitter-base capacitance voltage for depletion capacitance dominant,
Vdif ---- emitter-base capacitance voltage for diffusion capacitance dominant, and
Qo ---- equilibrium emitter-base junction depletion charge.

When iterating the effective base mobility including the effect of the carrier-carrier scattering for high free carrier levels, the following variables are calculated:

Root ---- routine to find the root of the external function Dccs(D),
D ---- ambipolar diffusivity including carrier-carrier scattering,
Dhi ---- upper bound on Dccs,
Dlo ---- lower bound on Dccs, and
TOL ---- tolerance level for Dccs.

The emitter-base routine is defined as the voltage controlled voltage source, and a voltage value is passed to the main circuit. It s represented by the variable Veb in the IG-Spice IGBT equivalent circuit.

Appendix E

Using IG-Spice IGBT Program

In this section, step by step demonstration on how the IG-Spice IGBT model is used with IG-Spice circuit simulation program is given. The procedure of using the IG-Spice IGBT model is demonstrated by using the model in a inductive load circuit for the conditions given for Figure 5.18. The detailed explanation of the IG-Spice program will not be given in this section because they can be obtained in the IG-Spice manual [8].

E.1 IG-Spice IGBT Model Organization

Within the IG-Spice IGBT model there are two main files: IGBT.FOR and IGBT.DAT. The IGBT.FOR is a FORTRAN file and contains the subroutines for the emulation of IGBT device characteristics. The library file, IGBT.DAT, contains the node specifications that describe the IG-Spice IGBT equivalent circuit. In order to run the program, the FORTRAN file must be compiled and linked with the IG-Spice program. Further discussion of these two files are discussed below.

E.1.1 IGBT.FOR

This file contains the source codes for the IG-Spice IGBT model describing dependent current or voltage sources as described in Appendix D. IGBT. FOR is a text file, and can be easily accessed and stored in a floppy diskette. The complete source code is listed in the Appendix F.

For the IG-Spice program to recognize the IGBT model subroutines, the IGBT.FOR file need to be compiled and linked with the main program. When IGBT.FOR is successfully compiled, an IGBT.OBJ file will be created. This IGBT.OBJ object module is then linked to the main IG-Spice program. (The procedure for compiling and linking model subroutines are described in [8].) Once the linking process is finished, there will be an IGBT.EXE file in the sub directory.

To run the IGBT.EXE, the library file containing the IG-Spice IGBT sub circuit, and the input IG-Spice files must be defined. The example of assigning the library and input file is given below:

ASSIGN LIBRARY IGBT.DAT, and

ASSIGN INPUT IGBT.IGS,

where IGBT.DAT file contains the IGBT sub circuit, and IGBT.IGS is the IG-Spice input file describing the external circuit node connections.

IG-Spice can then run the IG-Spice IGBT model by the typing the command:

RUN IGBT.

E.1.2 IGBT.DAT

This file contains the descriptions of interconnections of nodes which describe the controlled current and voltage sources (see Fig. E.1). All the node numbers correspond with the node numbers of IG-Spice IGBT equivalent circuit shown in Fig. E.2.

In IGBT.DAT, the IG-Spice IGBT model is assigned the sub circuit name IGBT, and the three terminal nodes of the IGBT device is assigned in the following order: gate, anode, and cathode. To observe any specific behavior of the IG-Spice IGBT model, the sub circuit can be used as input file with few modifications.

As discussed in the Appendix D, the model parameter values are inputted through this sub circuit. For example, the threshold voltage parameter Vt, need to be changed to a value of 4.3 V. This is accomplished by typing the following in the line which calls the IMOS function:

GIMOS 7 60 POLY(2) (30,60) (2,60) IMOS(Vt=4.3).

More than one parameter can be specified as long as the parameter variables have been defined in the IGBT.FOR source code file.

Recall that if there are no change in parameter values, the line calling IMOS function is just left as shown:

```
GIMOS  7 60 POLY(2) (30,60) (2,60) IMOS,
```

and the program will use the default values that are in the IGBT.FOR file.

In changing the base lifetime parameter, the resistance value RTHL must also be changed. As an example, the base lifetime need to be changed to 8 us. Following is the appropriate changes which need to be made in the IG-Spice IGBT sub circuit:

```
GIMOS  7 60 POLY(2) (30,60) (2,60) IMOS(t=8e-6), and
RTHL   16  0  8.0.
```

Notice that the resistance RTHL, is assigned a whole value, and is assigned the exact value for the line calling the function IMOS. Recall, this is due to defining the base lifetime as a resistance value in the base charge control circuit (see Fig. E.2).

E.2 Example of Using the IGBT Model

The following example is to simulate the single IGBT interaction in a inductive load circuit as shown in Fig. E.3.

The parameters are given as follows, Vt=4.7V, and t=7.1 e-6 seconds. Then the appropriate change must be made in the IGBT.DAT file:

RTHL 16 0 7.1, and

GIMOS 7 60 POLY(2) (30,60) (2,60) IMOS(Vt=4.7, t=7.1e-6),

where default values are used for other parameters that have not been specified in the sub circuit file.

The appropriate input file describing the node connections of the circuit is shown in Fig. E.4. Remember that the sub circuit of IGBT must be called in the input file. Next, the library file and input file must be assigned:

ASSIGN LIBRARY IGBT.DAT, and

ASSIGN INPUT IGBT.IGS.

The program is executed by typing:

RUN IGBT.

```
LIBRARY IGBT
.SUBCKT IGBT  30  40  50
```

```
*IGBT SUBCKT G    A   K
RVIP    18  0 1
RIMOS  19  0 1
RVIT     20  0 1
CGS      30  60 0.6NF
RTHL     16  0 7.1
CDUM   17  0 1UF
*
GIMOS  7 60 POLY(2) (30,60) (2,60) IMOS
GICGD  5 30 POLY(5) (4,30) (30,60) (4,60) (18,0) (19,0) IGD
GICDS  8 60 POLY(3) (4,60) (18,0) (19,0) IDS
FINW    0 13 VINW 1
GIQ  15  0 POLY(4) (17,0) (2,60) (18,0) (19,0) IQ
FIA    9 60 POLY(1) VIT IA
FIPW  0 18 VIPW 1
FIMOS 0 19 VIMOS 1
FIT   0 20 VIT 1
GIB  10 60 POLY(4) (17,0) (2,60) (18,0) (19,0) IB
GIC  11 60 POLY(4) (4,60) (17,0) (18,0) (19,0) IC
EVEB  1  2 POLY(3) (17,0) (2,60) (20,0) VEB
*
VIT      40  1    0PROBE
VIPW   2  3      0PROBE
VIPA    3  9      0PROBE
VIPB    3 10     0PROBE
VIPC    3 11     0PROBE
VINE    14 15   0PROBE
VINW   2  4      0PROBE
VTHL    14 16   0PROBE
VDQT   14 17   0PROBE
VNN     13 14   0PROBE
VIMOS 4  7      0PROBE
VICGD  4  5      0PROBE
VICDS  4  8      0PROBE
VIK      60 50   0PROBE
.ENDS IGBT
.ENDL
```

Figure E.1. IGBT sub circuit describing the node connections of IG-Spice IGBT equivalent circuit.

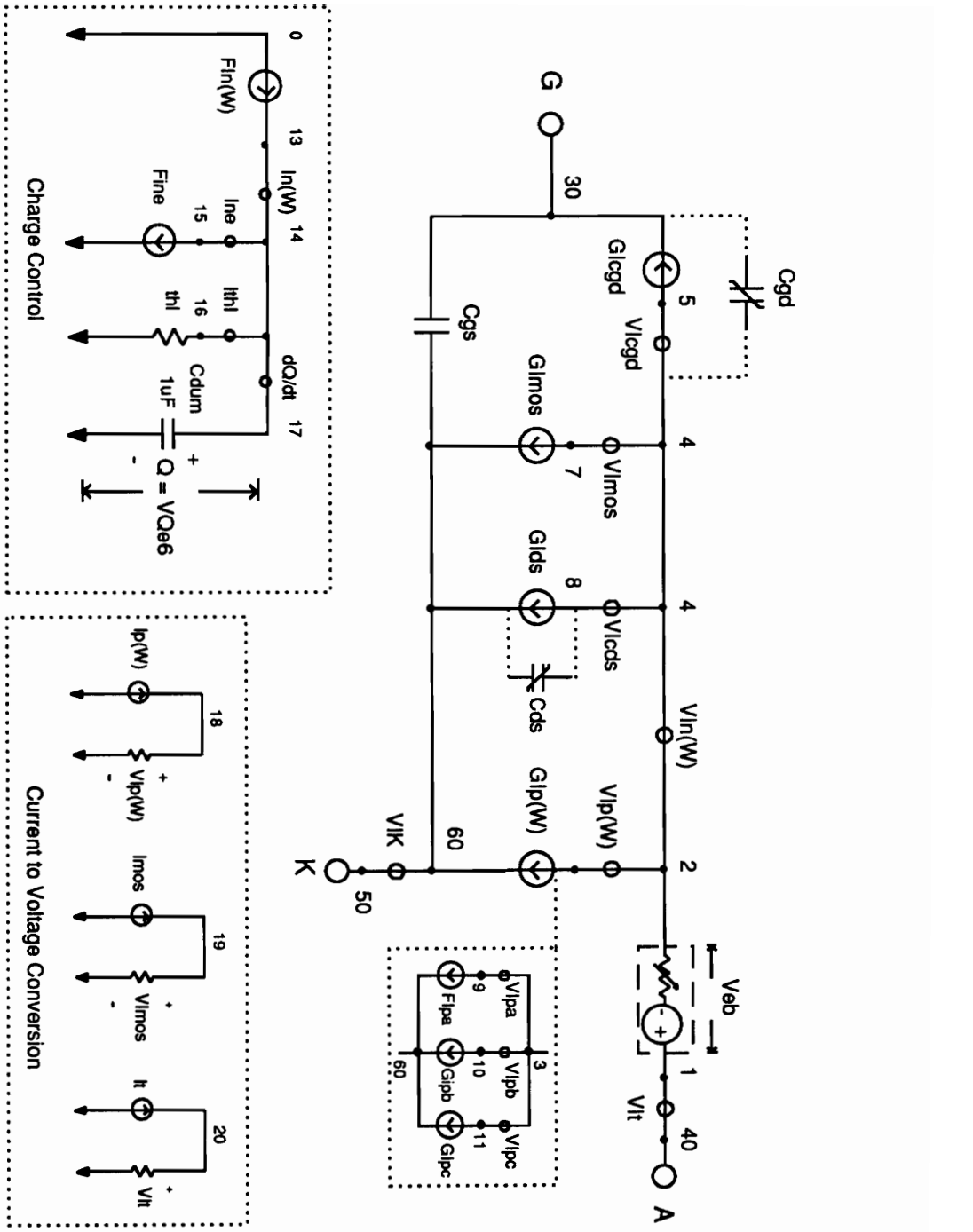


Figure E.2. IG-Spice IGBT equivalent circuit.

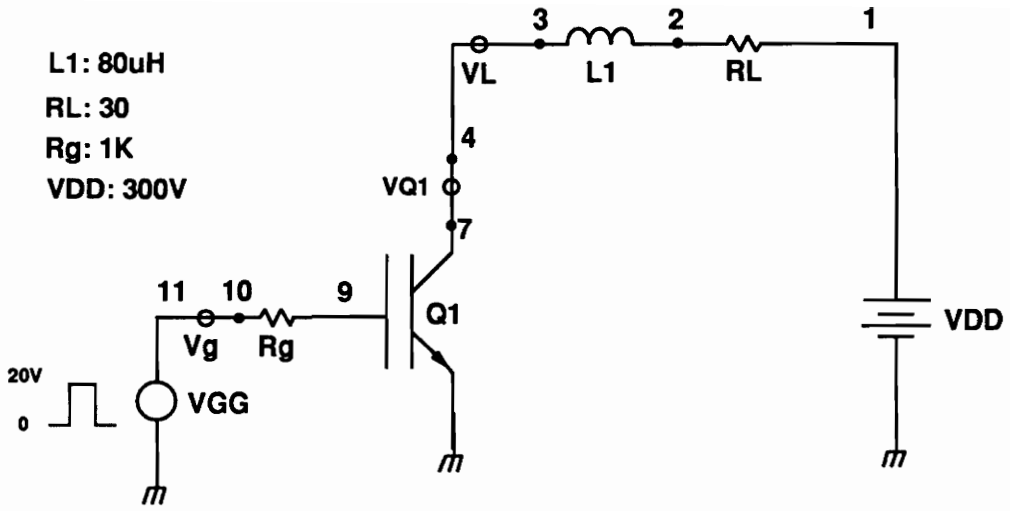


Figure E.3. Inductive load operation for a single IGBT.

```
*IGBT ANALYSIS
VDD 1 0 300
VGG 7 0 PULSE(0 20 0 20N 20N 30UPW 60USPER)
L1    2   3    80UHENRY
RL    1   2    30
RG 10   9    1K
VL    3   4    0PROBE
VG 11  10    0PROBE
XIGBT   9 7 0 IGBT
.OPTIONS ITL5=0 LIMPTS=1000000
.TRAN .01U 60U
.PLOT TRAN V(4) I(VL) I(VG) V(7)
.LIBRARY IGBT
.END
```

Figure E.4. Input file describing the node connections for Fig. E.3.

Appendix F

IG-Spice IGBT SUBROUTINES

```
      FUNCTION FNNAME(JFN)
      REAL*8 FNNAME,NAMES(9)
      DATA NAMES /'IMOS','IGD','IDS','IQ','IA','IB','IC','VEB','*END*'/
      FNNAME=NAMES(JFN)
      RETURN
      END

C     ------------------------------------------------------
C     ASSIGN PARAMETER VALUES AND THEIR
C     DEFAULT VALUES
C     ------------------------------------------------------
      FUNCTION FPNAME(JFN,IDAT,PNAME,PVAL)
c     ------------------------------------------------------------------------------------
c     This function allows one to enter parameter in variable
c     expression form.  It checks for the variables and
c     assigns that values which the user specified.  The routine
c     then stores this values in the Data(21) array.  So in order
c     to retrieve these values we need to specify 'expression=Data(n)'.
c     ------------------------------------------------------------------------------------
      IMPLICIT REAL*8(A-H,O-Z)
      REAL*8 Kp,Isne,Nb,ni
      COMMON /IGBTpar/ t,Wb,Nb,A,Isne,Vt,Kp,Cgs,Agd,Coxd,ccsflg,
     &                 sclflg,Vtd,Vnsat,Vpsat,Ut,ni,Un,Up,q,esi,Vbn
     &                 Bvf,Vbc,Qt,Dccs
c
c     ------------------------------------------
c     NIBT=NUMBER OF VARIABLES
C     PIGBT=VARIABLE NAMES
C     VIGBT=DEFAULT VALUES
C     ------------------------------------------
      DIMENSION PIGBT(21),VIGBT(21)
      DATA NIGBT /21/
      DATA PIGBT /'t','Wb','Nb','A','Isne','Vt','Kp','Cgs','Agd',
     +           'Coxd','ccsflg','sclflg','Vtd','Vnsat','Vpsat',
     +           'Ut','ni','Un','Up','q','esi'/
      DATA VIGBT /7.1e-6,0.0093,2.0e4,0.1,6.5e-14,5.0,0.38,0.6e-9,
     +           0.05,1.6e-9,-1,-1,0.0,1.0e7,1.0e7,0.0259,1.45,
     +           1500.0,450.0,1.6e-9,1.05e-12/
```

```
C       ------------------------------------------------
C       FPSET IS A INTERNAL SUBROUTINE
C       ------------------------------------------------
      FPNAME=FPSET(IDAT,PNAME,PVAL,PIGBT,VIGBT,NIGBT)
      RETURN
      END

c
c
          FUNCTION ROOT(AX,BX,F,TOL)
          REAL AX,BX,F,TOL
C
C         A ZERO OF THE FUNCTION F(X) IS COMPUTED IN THE INTERVAL AX,BX.
C
C  INPUT..
C  AX  LEFT ENDPOINT OF INITIAL INTERVAL
C  BX  RIGHT ENDPOINT OF INITIAL INTERVAL
C  F   FUNCTION SUBPROGRAM WHICH EVALUATES F(X) FOR ANY X IN
C         THE INTERVAL AX, B
C
C  TOLDESIRED LENGTH OF THE INTERVAL OF UNCERTAINTY OF THE
C         FINAL RESULT ( .GE. 0.0)
C
C  OUTPUT..
C
C  ROOT ABCISSA APPROXIMATING A ZERO OF F IN THE INTERVAL AX,BX
C
C
C         IT IS ASSUMED THAT F(AX) AND F(BX) HAVE OPPOSITE SIGNS
C         WITHOUT A CHECK.  ROOT RETURNS A ZERO X IN THE GIVEN INTERVAL
C         AX, BX TO WITHIN A TOLERANCE 4*MACHEPS*ABS(X)+TOL, WHERE MACHEPS
C         IS THE RELATIVE MACHINE PRECISION.
C
C         THIS FUNCTION SUBPROGRAM IS A SLIGHTLY MODIFIED TRANSLATION OF
C         THE ALGOL 60 PROCEDURE ZERO GIVEN IN RICHARD BRENT, ALGORITHMS
C         FOR MINIMIZATION WITHOUT DERIVATIVES, PRENTICE - HALL, INC., (1973).
C
C
          REAL*8 A,B,C,D,E,EPS,FA,FB,FC,TOL1,XM,P,Q,R,S
C
C  COMPUTE EPS, THE RELATIVE MACHINE PRECISION
C
          EPS=1.0
10        EPS=EPS/2.0
          TOL1=1.0+EPS
          IF(TOL1 .GT. 1.0) GO TO 10
C
C  INITIALIZATION
C
          A=AX
```

```
        B=BX
        FA=F(A)
        FB=F(B)
C
C  BEGIN STEP
C
20      C=A
        FC=FA
        D=B-A
        E=D
30      IF(ABS(FC) .GE. ABS(FB)) GO TO 40
        A=B
        B=C
        C=A
        FA=FB
        FB=FC
        FC=FA
C
C  CONVERGENCE TEST
C
40      TOL1=2.0*EPS*ABS(B)+0.5*TOL
        XM=0.5*(C-B)
        IF(ABS(XM) .LE. TOL1) GO TO 90
        IF(FB .EQ. 0.0) GO TO 90
C
C  IS BISECTION NECESSARY
C
        IF(ABS(E) .LT. TOL1) GO TO 70
        IF(ABS(FA) .LE. ABS(FB)) GO TO 70
C
C  IS QUATRATIC INTERPOLATION POSSIBLE
C
        If(A .NE. C)GO TO 50
C
C  LINEAR INTERPOLATION
C
        S=FB/FA
        P=2.0*XM*S
        Q=1.0-S
        GO TO 60
C
C  INVERSE QUADRATIC INTERPOLATION
50      S=FA/FC
        R=FB/FC
        S=FB/FA
        P=S*(2.0*XM*Q*(Q-R)-(B-A)*(R-1.0))
        Q=(1-1.0)*(R-1.0)*(S-1.0)
```

```
C
C  ADJUST SIGNS
C
60      IF(P .GT. 0.0) Q=-Q
        P=ABS(P)
C
C  IS INTERPOLATION ACCEPTABLE
C
        IF((2.0*P) .GE. (3.0*XM*Q-ABS(TOL1*Q))) GO TO 70
        IF(P .GE. ABS(0.5*E*Q)) GO TO 70
        E=D
        D=P/Q
        GO TO 80
C
C  BISECTION
C
70      D=XM
        E=D
C
C  COMPLETE STEP
C
80      A=B
        FA=FB
        IF(ABS(D) .GT. TOL1) B=B+D
        IF(ABS(D) .LE. TOL1) B=B+SIGN(TOL1,XM)
        FB=F(B)
        IF((FB*(FC/ABS(FC))) .GT. 0.0) GO TO 20
        GO TO 30
C
C  DONE
C
90      ROOT=B
        RETURN
        END
```

```
C
C  FUNCTIN TO ITTERATE CCS DIFFUSIVITY
C
      Function Dccs(D)
c
c
      Real*8          t,Wb,Nb,A,Isne,Vt,Kp,Cgs,Agd,Coxd,ccsflg,
     &                sclflg,Vtd,Vnsat,Vpsat,Ut,ni,Un,Up,q,esi,BVn,
     &                BVf,Vcb,Qt,Dccs
      COMMON /IGBTpar/  t,Wb,Nb,A,Isne,Vt,Kp,Cgs,Agd,Coxd,ccsflg,
     &                sclflg,Vtd,Vnsat,Vpsat,Ut,ni,Un,Up,q,esi,Bvn,
     &                Bvf,Vcb,Qt
      Real*8  W,Wcbj,D,L,P,Pmid,Unc,Upc,Ucinv,wl
c
c
c
      Wcbj=sqrt(2.0*abs((Vcb+0.6)/q/Nb))
      W=(Wb-Wcbj)
      If(W .lt. 1.0e-10) W=1.0e-10
      L=sqrt(t*D)
      wl=W/L
      P=Qt/A/L/Tanh(wl/2.0)/q
      Pmid=P*sinh(wl/2.0)/sinh(wl)
c
c     1/Uc=Ucinv
c
      Ucinv=sqrt(Pmid*(Pmid+Nb))*LOG(1.0+4.54e11/10.0**(20.0/3.0)
     &  /( (Pmid+Nb)*(Pmid+ni**2/Nb) )**(1.0/3.0) )/1.428e10
c
      Unc=1.0/(1.0/Un+Ucinv)
      Upc=1.0/(1.0/Up+Ucinv)
      Dccs=2.0*Ut*Unc*Upc/(Unc+Upc)-D
      Return
      End


    SUBROUTINE FORTFN(JFN,DATA,NDAT,ARG,NARG,COEF,TIME,VNAME,IPTR)
     IMPLICIT REAL*8(A-H,O-Z)
     DIMENSION DATA(25),ARG(8),COEF(8)
     External Dccs
     COMMON /STATES/ TOLD,TOLD2,ODT,STATE(500),STATE2(500),NSTATE
     REAL*8 Navg,L,K,Kp,Nb,Isne,ni,Inw,It,Nscl,Dccs,D,Dlo,Dhi,Tol
      COMMON /IGBTpar/ t,Wb,Nb,A,Isne,Vt,Kp,Cgs,Agd,Coxd,ccsflg,
     &                sclflg,Vtd,Vnsat,Vpsat,Ut,ni,Un,Up,q,esi,Bvn,
     &                Bvf,Vcb,Qt
      GOTO(100, 200, 300, 400, 500, 600, 700, 800),JFN
```

```
c       ------------------------------------------------------------------
c       Assign parameters
c       *NOTE:* - One needs to enter changed paramters when-
c                 - calling the first function 'IMOS'.-
c       ------------------------------------------------------------------
100     t=      Data(1)
        Wb=     Data(2)
        Nb=     Data(3)
        A=      Data(4)
        Isne=   Data(5)
        Vt=     Data(6)
        Kp=     Data(7)
        Cgs=    Data(8)
        Agd=    Data(9)
        Coxd=   Data(10)
        ccsflg= Data(11)
        sclflg= Data(12)
        Vtd=    Data(13)
        Vnsat=  Data(14)
        Vpsat=  Data(15)
        Ut=     Data(16)
        ni=     Data(17)
        Un=     Data(18)
        Up=     Data(19)
        q=      Data(20)
        esi=    Data(21)
c
c
c       ------------------------------------------
c       Calculate Mosfet Current (Imos)
c       ------------------------------------------
        Vgs=Arg(1)
        Vds=Arg(2)
         If(Vgs .ge. Vt)Then
          If(abs(Vds) .lt. (Vgs-Vt))Then
C           ---------------------------------------------------
c           Imos=Kp*(Vgs-Vt)*Vds-.5*Kp*abs(Vds)*Vds
c           ---------------------------------------------------
            Coef(3)=Kp*(Vgs-Vt)-Kp*abs(Vds)
            Coef(2)=Kp*abs(Vds)
            Coef(1)=-Kp*Vgs*abs(Vds)+0.5*Kp*abs(Vds)*Vds
          Endif
          If(abs(Vds).ge.(Vgs-Vt))Then
             If(Vds .gt. 0.0)Then
c            ----------------------------------------
c            Imos=0.5*Kp*(Vgs-Vt)*(Vgs-Vt)
c            ----------------------------------------
             Coef(2)=Kp*(Vgs-Vt)
              Coef(1)=0.5*Kp*(Vt*Vt-Vgs*Vgs)
             Endif
```

```
            If(Vds .lt. 0)Then
C             ---------------------------------
c             Imos=-0.5*Kp*(Vgs-Vt)**2
c             ---------------------------------
                Coef(2)=-Kp*(Vgs-Vt)
                Coef(1)=-0.5*Kp*(Vt*Vt-Vgs*Vgs)
              Endif
            Endif
          Else
              Imos=0.0
            Coef(1)=0.0
          Endif
          Return
C         ------------------------
C           Cgd routine
c         ------------------------
200       If(Time .eq. 0)Return
          Vgd=Arg(1)
          Vgs=Arg(2)
          Vds=Arg(3)
          Vipw=Arg(4)
          Vimos=Arg(5)
c
          Nscl=Nb
          If(sclflg .gt. 0.0)Then
            Nscl=Nb+Vipw/(q*A*Vpsat)-Vimos/(q*A*Vnsat)
          Endif
c
c         ------------------------------------------------
c         Get the correct capacitor value(Cgd)
c         ------------------------------------------------
          Cgd=Coxd
          If(Vds .gt. Vgs)Then
            Wgdj=sqrt(2.0*esi*abs((Vds-Vgs)/q/Nscl))
            Cgd=Coxd/(1.0+Coxd/Agd/esi*Wgdj)
          Endif
c         ----------------------------
c         Calculate C*dVgd/dt
c         ----------------------------
          If(Iptr .eq. 0.0) Call Gstate(Arg(1), 1, Iptr)
            Vgdo=State(Iptr+1)
            Call Rstate(Arg(1), 1, Iptr)
            Coef(1)=-Cgd*Vgdo*Odt
            Coef(2)=Cgd*Odt
          Return
```

```
c       --------------------------------
c       Cds Routine C*dVds/dt
c       --------------------------------
300     If(Time .eq. 0.0)Return
          Vds=Arg(1)
          Vipw=Arg(2)
          Vimos=Arg(3)
c
        Nscl=Nb
        If(sclflg .gt. 0.0)Then
          Nscl=Nb+Vipw/(q*A*Vpsat)-Vimos/(q*A*Vnsat)
        Endif
c
         Wdsj=sqrt(2.0*esi*abs((Vds+0.6)/q/Nscl))
        If(Wdsj .lt. 10.0e-8) Wdsj=10.0e-8
          Cdsj=(A-Agd)*esi/Wdsj
c
        If(Iptr .eq. 0.0) Call Gstate(Arg(1), 1, Iptr)
          Vdso=State(Iptr+1)
          Call Rstate(Arg(1), 1, Iptr)
          Coef(1)=-Cdsj*Vdso*Odt
          Coef(2)=Cdsj*Odt
         Return
c       ------------------------
c       Get IQ for dQ/dt
c       ------------------------
400     If(t .lt. 0.0)Return
          Qn=Arg(1)
          Qt=Qn*1.0e-6
          Vds=Arg(2)
          Vipw=Arg(3)
          Vimos=Arg(4)
C
        Nscl=Nb
        If(sclflg .gt. 0.0)Then
          Nscl=Nb+Vipw/(q*A*Vpsat)-Vimos/(q*A*Vnsat)
        Endif
c
        Wdsj=sqrt(2.0*esi*abs((Vds+0.6)/q/Nscl))
        If(Wdsj .lt. 10.0e-8) Wdsj=10.0e-8
          W=Wb-Wdsj
          Qb=q*A*W*Nb
c       -------------------------------------------------
c       IQ=Q*Q/(Qb*Qb)*4*Nb*Nb*Isne/(ni*ni)
c       -------------------------------------------------
        Coef(1)=-Qt*Qt/(Qb*Qb)*4.0*Nb*Nb*Isne/(ni*ni)
        Coef(2)=2.0*Qt/(Qb*Qb)*4.0*Nb*Nb*Isne/(ni*ni)*1.0e-6
        Return
```

```
c       ----------------
C         find Ia
c       ----------------
500     If(t .lt. 0.0) Return
        b=Un/Up
        It=Arg(1)
c       -----------------
c       Ia=1/(1+b)*It
c       -----------------
         Coef(2)=1.0/(1.0+b)
        Return
c       -----------
c         find Ib
c       -----------
600     If(t .lt. 0.0)Return
         b=Un/Up
         Dp=Ut*Up
         Qn=Arg(1)
         Qt=Qn*1.0e-6
         Vds=Arg(2)
         Vipw=Arg(3)
         Vimos=Arg(4)
c
         Nscl=Nb
         If(sclflg .gt. 0.0) Then
          Nscl=Nb+Vipw/(q*A*Vpsat)-Vimos/(q*A*Vnsat)
         Endif
c
         Wdsj=sqrt(2.0*esi*abs((Vds+0.6)/q/Nscl))
         W=Wb-Wdsj
c       --------------------------------
c       Ib=b/(1+b)*4*Dp/(W*W)
c       --------------------------------
         Coef(2)=b/(1.0+b)*4.0*Dp/(W*W)*1.0e-6
        Return
c
c       -------------
c         Find IC
c       -------------
700     If(Time .eq. 0.0)Return
        If(t .lt. 0.0)Return
         Vbc=Arg(1)
         Qn=Arg(2)
         Vipw=Arg(3)
         Vimos=Arg(4)
c
         Nscl=Nb
         If(sclflg .gt. 0.0)Then
           Nscl=Nb+Vipw/(q*A*Vpsat)-Vimos/(q*A*Vnsat)
         Endif
```

```
c
        Qt=Qn*1.0e-6
        Wbcj=sqrt(2.0*esi*abs((Vbc+0.6)/q/Nscl))
        If(Wbcj .lt. 10.0e-8) Wbcj=10.0e-8
        W=Wb-Wbcj
        Qb=q*A*W*Nscl
        Cbcj=A*esi/Wbcj
c
        If(Iptr .eq. 0.0) Call Gstate(Arg(1), 1, Iptr)
        Vbco=State(Iptr+1)
        Call Rstate(Arg(1), 1, Iptr)
c       ----------------------------------------
c       Ic=Cbcj/3*(Vbc-Vbco)*Odt/Qb*Q
c       ----------------------------------------
        Coef(1)=-Cbcj/3.0*Qt/Qb*Vbc*Odt
        Coef(2)=Cbcj/3.0*Qt/Qb*Odt
        Coef(3)=Cbcj/3.0*(Vbc-Vbco)*Odt/Qb*1.0e-6
        Return
c       ----------------------------------------
c       Emitter-Base Junction Voltage
c       ----------------------------------------
c
800     Qn=Arg(1)
        Vcb=Arg(2)
        Vit=Arg(3)
        Qt=Qn*1.0e-6
c
c       --------------------------------
c       Evaluate model variables
c       --------------------------------
c
        Wcbj=sqrt(2.0*esi*abs((Vcb+0.6)/q/Nb))
        W=abs(Wb-Wcbj)
        Qo=A*sqrt(2.0*esi*q*Nb*0.6)
        K=1.0/q/Nb/A**2/esi
c
c       -------------------------------
c       Test if MOSFET Vebj=0
c       -------------------------------
c
        If(t .lt. 0.0)then
          Rb=W/Un/A/q/Nb
          Coef(1)=0.0
          Coef(4)=Rb
          Return
        Endif
```

```
c
c       ---------------------------
c       Test for reverse bias
c       ---------------------------
c
        If(Qt .lt. 0.0)Then
          Rb=W/Un/A/q/Nb
c         Vebj=-0.5*(Qt-Qo)**2/q/Nb/A**2/esi+0.6
c         Veb=It*Rb+Vebj
          Coef(1)=0.5*Qt*Qt*K-0.5*Qo*Qo*K+0.6
          Coef(2)=-(Qt-Qo)*K*1.0e-6
          Coef(4)=Rb
          Return
        Endif
c
c       ------------------------------------------------------------
c       Test if flag for carrier-carrier scaattering is set
c       ------------------------------------------------------------
        If(ccsflg .gt. 0.0)Then
          D=2.0*Ut*Un*Up/(Un+Up)
          Dhi=D
          Dlo=D+Dccs(D)
          TOL=1.0e-4*D
          D=root(Dlo,Dhi,Dccs,Tol)
c
c       ------------------------------------------------
c       Evaluate functions of the model variable
c       ------------------------------------------------
         L=sqrt(t+D)
         wl=w/L
         cosch=1.0/sinh(wl)
         tnh=Tanh(wl/2.0)
         cth=1.0/tanh(wl)
         P=Qt/A/L/tnh/q
         Pmid=P*sinh(wl/2.0)/sinh(wl)
c       ------------------------------------------------------------------------
c       1/Uc=Ucinv : the recripical component of mobility due to high
c                    free carier level (carrier-carrier) scattering
c       ------------------------------------------------------------------------
          Ucinv=sqrt(Pmid*(Pmid+Nb))*LOG(1.0+4.54e11/10.0**(20.0/3.0)
     &    /((Pmid+Nb)*(Pmid+ni**2/Nb))**(1.0/3.0))/1.428e10
c
c         Uc=1.428/(sqrt(Pmid*(Pmid+Nb))*LOG(1.0+4.54e11
c    &    /10.0**(20.0/3.0)/((Pmid+Nb)*Pmid)**(1.0/3.0)))
c
          Unc=1.0/(1.0/Un+Ucinv)
          Upc=1.0/(1.0/Up+Ucinv)
c
c***    ELSE: case neglecting carrier-carrier scattering.
c
```

```
      Else
        Unc=Un
        Upc=Up
        D=2.0*Ut*Un*Up/(Un+Up)
c     ------------------------------------------------
c     Evaluate functions of the model variable
c     ------------------------------------------------
        L=sqrt(t*D)
        wl=w/L
        cosch=1.0/sinh(wl)
        tnh=Tanh(wl/2.0)
        cth=1.0/tanh(wl)
        P=Qt/A/L/tnh/q
      Endif
c     ------------------------------------------------------------------
c     Evaluate the forward biased IGBT emitter base voltage
c     ------------------------------------------------------------------
      Ueff=Unc+Upc*P/(P+Nb)
      Navg=sqrt(Nb**2+P**2*cosch**2)
      x=Navg*tnh/(Nb+P*cosch*tnh)
      ARCTNH=0.5*LOG((1.0+x)/(1.0-x))
      Rb=1.0/Ueff/q*2.0*L/Navg*ARCTNH/A
      Vdep=-0.5*(Qt-Qo)**2*K+0.6
      Vdif=Ut*LOG((P+Nb)*(P/ni**2+1.0/Nb))-D/Unc*LOG((Nb+P)/Nb)
      If(Vdif .lt. Vdep .or. Qt .gt. Qo)then
        Vebj=Vdif
c       Veb=It*Rb+Vebj
c       ------------------------------------------
c       Take partial of Vdif with respect to
c       P, and then use chain rule to find
c       the derivative of Vidf with respect
c       to Qt
c       ------------------------------------------
        dP=(1.0/A/L/tnh/q)*1.0e-6
        Fa=Ut*dP*(ni**2+Nb*(2.0*P+Nb))
        Fb=(P+Nb)*(Nb*P+ni**2)
        Fc=(D*dP)/(Unc*(Nb+P))
        dVebj=Fa/Fb-Fc
        Coef(1)=Vdif-dVebj*Qn
        Coef(2)=dVebj
        Coef(4)=Rb
      Else
c       Vebj=Vdep
        Coef(1)=0.5*Qt**2*K-0.5*Qo**2*K+0.6
        Coef(2)=-(Qt-Qo)*K*1.0e-6
        Coef(4)=Rb
      Endif
      Return
      End
```

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Vita

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