Design And Fabrication Of An Underwater Digital Signal Processor Multichip Module On Low Temperature Cofired Ceramic

by

Wendy Hayth-Perdue

Thesis submitted to the Faculty of the

Virginia Polytechnic Institute and State University

in partial fulfillment of the requirements for the degree of

Master of Science

in

Electrical Engineering

Approved:

Aicha Elshabini-Riad
A. Elshabini-Riad, Chairperson

D.J. Moore, Co-Chairperson

S.M. Riad

December, 1994

Blacksburg, Virginia
An Underwater Digital Signal Processor (UDSP) multichip module (MCM) was designed and fabricated according to specifications outlined by the Naval Surface Warfare Center (NSWC), Dahlgren Division. Specifications indicated that low temperature cofired ceramic (LTCC) technology be used to fabricate the MCM with surface dimensions of 2"x2". The top surface of the module was to be designed to enclose mounted components and bare dice, and the bottom surface was to be equipped with a 144 pin grid array (PGA). The LTCC technology selected for this application incorporated DuPont's 951 Green Tape™ and compatible materials and pastes. A mixed metal system using inner silver system and outer surface gold system was used. Harris Corporation's FINESSE MCM™, a computer-aided design (CAD) tool, was used to design the surface components and produce the circuit layout. FREESTYLE MCM™, an autorouter, was used to accomplish the routing of the signal layers. The design information provided by FINESSE MCM™ and FREESTYLE MCM™ was utilized to produce the artwork necessary for fabrication. Fabrication of the module was accomplished in part using thick film processes to produce the conducting areas on each layer. The layers were stacked in
a press, laminated, and fired. Conducting areas were screen printed on the top surface of the module for wire bonding and on the bottom surface of the module for pin attachment.

The main objectives of this thesis work were to convert silicon UDSP MCM to ceramic using LTCC, learn a new tool in CAD design that incorporates an autorouter, apply the tool to design a MCM-C module, and to develop criteria to evaluate the MCM. Future research work includes conducting line continuity testing, materials evaluation to determine reactions at interfaces and via filling, and resistance and electrical crosstalk measurements on the module.
ACKNOWLEDGMENTS

The author would like to thank the Naval Surface Warfare Center, Dahlgren Division, for making this project possible, and Mindy Mierzwa of Harris Corporation for her technical guidance throughout this work. The author would also like to thank Fred Barlow for his support throughout this project.

I would like to extend my sincere gratitude and appreciation to my advisor, Dr. Aicha Elshabini-Riad, for her support and commitment to my growth and understanding of microelectronics throughout my education at Virginia Tech. I would also like to offer my sincere thanks to Dr. D.J. Moore for his support and guidance throughout this project, and to Dr. Sedki Riad, for his guidance and service on my committee. My sincere thanks is also extended to Monty Hayes for his advise and support over the years.

I would like to thank my dear husband, Jimmy, for his unwavering support and understanding throughout my work. I would also like to thank my parents for their encouragement and commitment throughout my education.
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CHAPTER I
INTRODUCTION

The objective of this thesis work was to design, fabricate, and evaluate an Under Water Digital Processor (UDSP) Multichip Module (MCM) for the Naval Surface Warfare Center (NSWC), Dahlgren Division. This MCM was made of ceramic referred to as MCM-C and was to be fabricated using low temperature cofired ceramic (LTCC) material, specifically DuPont's 951 AT Green Tape™. Another objective was to design the MCM package using a new tool with computer-aided-design (CAD), specifically FINESSE MCM™ equipped with an autorouter, FREESTYLE MCM™.

The research described in this thesis will illustrate the capabilities of various MCM technologies, specifically MCM-C, and the progress achieved with recent advancements in design tools and processing. MCM-C is the most widely used and available MCM technology, and therefore the most reasonable choice for this application, particularly when considering the relatively low cost, high performance, rigidity, and hermeticity benefits.

This thesis is structured to give an overview of the background considerations, design, and process of the UDSP MCM. Chapter One gives a brief overview of the research topic and illustrates the structure of the thesis. Chapter Two provides background on MCM technology, including MCM-Laminate (MCM-L), MCM-Deposited (MCM-D), and MCM-Ceramic (MCM-C), and on component availability, reliability, and
attachment. Chapter Three describes the computer-aided-drawing (CAD) software (FINESSE MCM™) and the routing software (FREESTYLE MCM™) that was used to design the module. A description of the design requirements of the research work are also included in Chapter Three. Chapter Four demonstrates how FINESSE MCM™ and FREESTYLE MCM™ were utilized for this particular project. Chapter Five describes the fabrication process and the evaluation of the module. Chapter Six provides a conclusion to summarize the work conducted in this thesis and guidelines for future directions.
CHAPTER II
MCM TECHNOLOGIES

2.1 Introduction

Microelectronics packaging is a technology that is vitally needed for the advancement and performance of microcircuits. High performance circuits are often hindered by packaging design and material selection, rather than by imperfections in the circuit design. The primary functions of a microelectronics package are power distribution, signal distribution, heat distribution, and circuit protection.[1] In many applications, the packaging system used does not meet the basic needs and requirements of the circuit, such as proper transmission of signals and heat dissipation. In addition, the packaging material can also add undesired bulk to the circuit. Current trends in microelectronics dictate that circuits become smaller, faster, and more dense, and that microelectronics packaging techniques must be capable of accommodating these trends, as well as continuing in a traditional role of circuit protection and proper distribution of heat, power, and signals.

One form of packaging that meets these current trends is the multichip module (MCM). In general, a MCM consists of unpackaged components (bare die) mounted on a high density multilayer interconnect substrate. The multilayer substrate provides both interconnects and packaging for the circuit.[2] More specific guidelines are necessary for the material systems that are used to fabricate MCMs. These requirements include a low
dielectric constant and low resistivity conductors for increased signal speed, fine line width and pitch for increased circuit density, multilayer capability for increased circuit density and operation speed, and the ability to fabricate precise conductor lines with tight tolerance with regards to width, thickness, and spacing for reproducibility.[3] Meeting these requirements results in benefits that include reduced electrical losses, improved speed capability, lower cost for the desired performance, and reduced size and weight.[4]

The dielectric material used for the bulk of the module and as the substrate carrier also has requirements to be met. As mentioned previously, the material should possess a low dielectric constant to allow high speed signals to propagate. A low loss tangent is also necessary to minimize the attenuation of signal voltage. To decrease the chance of short circuits, the dielectric material should have a high resistivity and high dielectric strength. Low water absorption will minimize variations in the dielectric constant when a module is subjected to high humidity conditions. A low coefficient of thermal expansion (CTE), high thermal conductivity, and high mechanical strength are needed to minimize thermal stresses. Finally, to ensure structural integrity, the material must be ductile, adhesively strong, and it must be stable upon change in temperature and exposure to chemicals and solvents.[5]

In accordance with the requirements stated above, three types of MCM technologies have emerged. These three different forms of MCMs are MCM-Deposit (MCM-D), MCM-Laminate (MCM-L), and MCM-Ceramic (MCM-C).
2.1.1 MCM-D

The Institute for Interconnecting and Packaging Electronic Circuits (IPC) has developed definitions for the three types of available MCM technologies. MCM-Ds are defined as multichip modules that are constructed using unreinforced low dielectric ($k<5$) materials that are adjacent to the signal plane, with a base substrate of ceramic, silicon, copper, glass-reinforced laminate, metal, or metal composites. Conductors are fabricated by sputtering or plating metals such as aluminum, copper, or gold, which are subsequently patterned with photolithography techniques.[4] MCM-D currently offers the capability of producing the highest performance circuits with extremely high circuit density and small size, both of which dominate over the density and size capabilities of MCM-C and MCM-L. Table 2.1 shows a comparison of important aspects of the three technologies. The high circuit density and small size is further enhanced by using substrates such as silicon that allow fabrication of passive components into the substrate itself. This process not only reduces size and increases density, but the overall cost of the module is decreased as well by eliminating the purchase of various components.[6] Compared to MCM-C and MCM-L, MCM-D offers the highest performance, although at the highest cost. Until recently, MCM-D has offered the smallest line width, line spacing, and via diameter, all of which attribute to circuit density higher than MCM-C or MCM-L, although advancements in MCM-L make it possible to compete with the circuit density of MCM-D. Also, MCM-D can offer the highest signal speed capability because of an extremely low dielectric constant. MCM-D is not widely used, however, due to the limited maturity of
the technology. Since the technology is not widely used and production volume is relatively low, MCM-D is the most costly to produce.

2.1.2 MCM-L

MCM-Ls are described by the IPC as multichip modules that utilize laminated printed circuit board technology. Dielectric layers consist of resin materials such as epoxies, polyimides, or acrylics, and are reinforced with materials such as fiberglass, quartz, or Kevlar. Conductors are usually deposited copper, and vias are also fabricated with copper by electroless plating, followed by additional electrodeposition.[4] This processing has become the most predominately used MCM technology for a variety of low performance applications due to production capability and due to its low cost.[7] Until recently, MCM-Ls have exhibited the largest line width, line spacing, and via size, and the highest dielectric constant compared to MCM-D and MCM-C technologies. Recent advances in the MCM-L area have resulted in the development of dielectrics that exhibit a low dielectric constant (k=3.8), and processing that enables small line width and line spacing (1.6-2 mils) and small via diameter (2-2.4 mils) to be manufactured.[8] These values are comparable to those of both MCM-C and MCM-D.

2.1.3 MCM-C

The IPC defines MCM-Cs as multichip modules constructed of ceramic or glass ceramic that acts as both dielectric (k≥5) and as the base substrate for the circuit
components. Conductors and vias are made with a fireable metal material utilizing conventional thick film technology.[4] MCM-C has often been the MCM technology of choice because it represents a good compromise of the two previously discussed MCM technologies. MCM-C often provides a lower dielectric constant and higher circuit density than MCM-L, although at a higher cost. As compared to MCM-D, MCM-C has a higher dielectric constant and lower circuit density, but the cost is considerably lower than MCM-D. MCM-C is a mature technology and, because it utilizes existing thick film technology, MCM-C can be readily integrated into companies that have an established thick film infrastructure.

2.1.4 Summary

Each form of MCM technology has its own benefits and disadvantages. Research continues in each area in an effort to improve on existing advantages and to overcome disadvantages of each material system. However, the material system does not make up the entire module. Issues that involve components and component attachment must also be addressed for MCM technologies to progress to their fullest potentials.
<table>
<thead>
<tr>
<th></th>
<th>MCM-D</th>
<th>MCM-C</th>
<th>MCM-L (recent advances)</th>
</tr>
</thead>
<tbody>
<tr>
<td>substrate material</td>
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<td>glass ceramic</td>
<td>epoxy glass, aramides, polyimides, fluoropolymers</td>
</tr>
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<td>$k = 4.8-9.6$</td>
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</tr>
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<td>8-10</td>
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<tr>
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<td>8-10</td>
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<tr>
<td>via diameter (mils)</td>
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<td>20-25</td>
</tr>
<tr>
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<td>20-300</td>
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<td>good</td>
<td>good</td>
</tr>
<tr>
<td>relative cost</td>
<td>high</td>
<td>medium</td>
<td>low</td>
</tr>
</tbody>
</table>
2.2 Known Good Die

To obtain the maximum benefit of the packaging qualities of MCM technologies, unpackaged components, or bare die, are used to manufacture modules. Often bare die can be difficult to obtain unless the company fabricating the module can also supply the bare die.[9] Because these bare die have no lead attachments, it is difficult, if not impossible, to test each individual die for defects. It is therefore becoming increasingly necessary for die manufacturers to test the die prior to selling them. To obtain these "known good die" (KGD), elaborate testing has to be conducted. This testing includes burn-in, defined as "an electrical test to screen out components with infant mortality latent defects," and also a one hundred percent die level test over a wide range of temperatures.[10] This testing enables manufacturers to produce KGD which are formally defined as "unpackaged ICs that are known at a high confidence level to perform to packaged device specifications, and will continue to perform to specifications throughout their useful life."[11] Using KGD to manufacture MCM modules can decrease rework and assembly costs, as well as greatly increase product reliability.

Unfortunately, the availability of KGD is extremely limited, and those that can be found cost approximately two to four times as much as packaged bare die. Some manufacturers work around this availability problem by using untested bare die and incorporating into their yield analysis the probability that a certain number of die will fail, knowing that module yield decreases as the number of bare die populating a module increases. This procedure can sometimes be less costly than using all KGD. It is also beneficial to use a die attach method that can be reworked so that die can be replaced.
Some die attach methods can even be used to test the die when the module is partially assembled. If the die can be easily replaced, then the need for KGD decreases. Future trends in MCM technology require that KGD become increasingly available and that they become less expensive. Current trends, however, indicate that it is more feasible and economical to replace defective bare die than to attempt to use one hundred percent KGD until the price of KGD comes down.[12]

2.3 Chip Attachment Technologies

There are basically three available technologies for forming interconnects between bare die and the substrate. These technologies are wire bonding, tape automated bonding (TAB), and flip-chip bonding.

2.3.1 Wire Bonding

Wire bonding consists of diffusing two metals together to form a bond. The most common methods of wire bonding are thermocompression bonding, ultrasonic bonding, and thermosonic bonding. Thermocompression bonding utilizes elevated temperature and pressure to accomplish wire bonding; ultrasonic bonding uses ultrasonic energy in conjunction with pressure. Thermosonic bonding combines pressure, temperature, and ultrasonic energy to accomplish wire bonding.[15] Wire bonding is currently the most widely used bonding technology, partially due to its availability and reliability. Reasons for its widespread use are that the bonds can be inspected visually, bond integrity can be
tested, and die attachment and bonding can be reworked if necessary. Wire bonding is also suitable for prototyping and low volume applications.

Although wire bonding is widely used, it has disadvantages which are partially resolved with TAB or flip-chip technologies. Wire bonding requires a larger bonding area and processing time as compared to the other two technologies. The longer processing time is a result of having to create bonds one at a time, rather than making several, if not all, simultaneously. Difficulties occur when using wire bonding with MCM-L structures because localized heating may damage the substrate. Another disadvantage of wire bonding is that it requires gold plating on the substrate for bonding.[10,14]

2.3.2 Tape Automated Bonding

Tape automated bonding (TAB) is "a series of identical, fine-pitch copper lead frames supplied on a continuous sprocketed reel movie film tape made of polyimide with each movie frame containing on lead frame."[10] Each frame contains bonds that connect the die to the substrate. Bonding is accomplished in such a way that attachments can be made to the die without immediately making attachments to the substrate. This allows testing of the die prior to module completion, which is an advantage of TAB technology. Like wire bonding, TAB possesses the advantage of reworkability. TAB possesses some advantages over wire bonds such as a lower bond profile, substrate attachment with solder (not gold), and a higher reliability because the bonds created with the TAB process are more ductile than those created with wire bonding.
One major disadvantage of TAB technology is that because bonding areas on die are not a standard size and do not have standard spacing, a specific frame must be made for each application. This disadvantage makes TAB technology unsuitable for low volume applications.[10,14]

2.3.3 Flip-Chip Bonding

Flip-chip bonding is the newest bonding technology of the three technologies being discussed. Flip-chip bonding requires that the die first be bumped with solder on the die contacts. The die are then flipped and connected to metallization on the substrate through reflow soldering. Because the die are connected directly to the signal line, bonding area is virtually nonexistent, decreasing the distance, and therefore the time, a signal has to travel between dice. Other advantages also exist with flip-chip technology. One example is the capability to test the dice before module completion. This is accomplished by positioning the die in place, pressing them down to make a temporary contact with the metallization, and then testing the entire module. Even though this testing procedure is not as efficient as when the die are tested individually, bad die can still be found before module completion, thus greatly increasing module yield. As compared to wire bonding and TAB technologies, flip-chip technology offers the most dense interconnects, shortest paths for signal travel, lowest bond profile, and easiest reworkability.

Even though flip-chip offers a number of benefits that are superior to wire bonding and TAB, it still has many disadvantages which prohibit it from being readily integrated.
into MCM technology. One of these disadvantages is the lack of availability of bumped die. Currently, only companies that can both design the modules and supply themselves with bumped chips can overcome this disadvantage. Placement of flip-chips is difficult because they must be placed precisely on the signal connections. Inspection of these connections is difficult and must be performed through X-ray techniques -- inspection cannot be done visually. Finally, because the chips do not make contact with the surface of the substrate except at the bonding areas, heat transfer becomes difficult because the chips cannot utilize the high thermal conductivity of the substrate.[10,14]

2.4 Conclusion

MCM technology is continuing to gain acceptance as the preferred interconnect and packaging solution. In order for MCM technology to progress into new markets, however, there are still issues that must be addressed, such as KGD and viable bonding techniques. MCMs already play an integral part in high speed, high performance applications such as computers, workstations, and military applications. Current research is improving MCM technology to allow high performance modules to be fabricated at a reasonable cost. As an example of a military application, an Under Water Digital Process (UDSP) MCM-C was designed and fabricated for the Naval Surface Warfare Center (NSWC). The chapters to follow describe this design and fabrication process.
CHAPTER III

DESCRIPTION OF FINESSE MCM™ AND FREESTYLE MCM™

3.1 Introduction

FINESSE MCM™ is a computer-aided-drafting (CAD) software package for multichip module (MCM) applications that is used to design components and to place these components in a circuit layout. FREESTYLE MCM™ is an autorouter that uses design information from FINESSE MCM™ to properly connect components with signal lines. MCM modules containing several layers can be designed in FINESSE, and FREESTYLE will route the signal lines on and through these layers. FREESTYLE can be operated and monitored until the design is one hundred percent routed.

3.2 Structure of FINESSE Files

When FINESSE is first accessed, the user is in the "entry" state. The entry state is where most administrative duties are accomplished, such as opening, deleting, and listing the available files. From the entry state the user can access the "project" state and "circuit" state. The project state is simply a place where several circuits can be stored. The circuit state is where most of the design work is performed and saved in the circuit library. Library management is accomplished in the circuit state to design and access components, circuit layout, and other necessary elements of the design. The flow chart in Figure 3.1 provides an overall view of the FINESSE management structure.
The first circuit that should be accessed after FINESSE is installed is the "startpoint.mcm" circuit. This file should have its default values customized for the user, company, or research institution to comply with their own standards for MCM circuit design. Once modified, all new circuits should be started from the startpoint.mcm circuit.

3.3 Design Default Settings

The user can specify design default settings by modifying the design "parameters." Parameters represent settings within the circuit, most of which can be customized by the user for the particular design work being performed. The "set parameter" command is used to change these defaults and is available to the user from almost anywhere in FINESSE. These parameters are important to set such items as the standard unit of measure, the number of layers, and the output device, as well as various other items that assist the user with specifying design requirements for the circuit. These parameters can be set or modified anytime during the design process, but it is often easier to set some of these parameters before design work begins. A number of these parameters are dependent on one another, and if one parameter is changed, the others must also be modified accordingly, which leads to numerous changes in the entire circuit that can be avoided if some care is taken when setting parameters at the start of the design process. An example of a parameter that must be defined prior to beginning the design process is the number of signal layers the completed module will possess. If this parameter must be modified after any artwork has been completed, such as artwork that defines a via, it is necessary to
redefine the artwork. If the user wants a via name to be available for all layers, and the number of layers increases, the via would have to be redefined to accommodate for the added layers.

3.4 Pad Design

Because diepads and bondpads are used in several different component definitions, they are defined separately from the components as "padstacks". Padstacks are also used to define via dimensions. Before creating any component definitions, padstacks for the die wire bonding pads (diepads) and bonding pads for the surface of the substrate (bondpads) should be made. Via padstacks can also be made at this time, but they are not needed until the components are placed in the circuit layout.

3.5 Component Design

A complete component design is called a "package". This includes diepad locations, bondpad locations, and package dimensions. Figure 3.2 is an example of a component drawn as a package.

After the necessary padstacks are defined, a package can be made. Each component is made by creating an individual package. The package is first opened and named. A rectangle is then drawn to define the dimensions for the package. Diepads are positioned on the rectangle and numbered according to component specifications. After the diepads are placed, the bondpads are placed outside of the component, making a "via
template". The via template indicates how the wire bonds will connect to the diepads and extend out to the bondpads. Once the via template is added, the package is complete.

3.6 Layout

Before opening the layout, all package designs should be complete and the netlist prepared in a format that FINESSE can read as defined in the FINESSE manual.[16] FINESSE checks to see if the components listed in the netlist are contained in the circuit library. The layout state cannot be accessed if a component package does not exist in the library, therefore the user must complete all necessary package definitions in order to begin the circuit layout. Packages can be modified after the layout is placed, but all packages should be defined in some capacity for the layout to open. Also, FINESSE will not recognize any changes made to the netlist unless the user deletes the current layout and creates a new one. It is therefore beneficial for the user to make sure that the netlist is free of errors before the layout is accessed.

After the layout is successfully opened, the layer rules should be defined. These rules include defining the order in which the layers will be built, the width of signal lines, the spacing between signal lines, and the minimum distance components and signal lines can be located from the edge. These rules can be defined for each individual layer. Another rule is the "paired layer" rule which defines which layers can have connections between them. Often, it is desired to have staggered vias instead of straight or through vias. A comparison of staggered and through vias is shown in Figure 3.3.[15] Through
vias are more likely to have integrity problems than staggered vias, therefore staggered vias are usually preferred.

With the layer rules defined, the user can place the components using the "place component" command from the pull down menu. Each component is positioned as desired with the aid of the mouse. After all the components are placed, the via template should be changed to wire bonds by using the "create wire bonds" command from the pull down menu.

At this point, the user has the option of either starting the autorouter or placing "via fanouts." A via fanout is a series of vias that originate on an upper layer and continue down through several layers until the desired layer is reached. Via fanouts provide a path for the autorouter to follow to access inner layers. Via fanouts are not mandatory, but are recommended for modules with over six to eight layers since the path they provide to lower layers can decrease the time it takes to complete the routing process. Once the user has incorporated the desired via fanouts, the autorouter can be initiated.

3.7 Routing With FREESTYLE MCM™

When the layout is complete, the FREESTYLE MCM™ autorouter can be accessed from the layout state. Once FREESTYLE has been accessed, routing options can be set to user specifications. For example, if the user prefers that no routing be conducted on a specified layer, the user can turn the layer "off" so that FREESTYLE will not route on that particular layer. Another example would be to set the "via grid" spacing.
The via grid spacing tells FREESTYLE the minimum distance one via can be placed from another. Setting the via grid often speeds up the routing process considerably.

Once all the necessary parameters have been set, the user can initiate the autorouting process. It is usually necessary for FREESTYLE to make several passes to fully route the design, the number of passes depending on the complexity of the design. Several "clean" passes should also be incorporated into the autorouting process. The clean passes will reroute all wires, attempting to reduce the number of vias to improve manufacturability. "Critic" passes can also be incorporated into the routing process. These passes eliminate unnecessary deviation of signal lines, but will not reroute the wires.

FREESTYLE can also be run in the background of the workstation computer by using a "do" file. This allows the user to start the routing and to be able to logout of the workstation computer while FREESTYLE is running. Commands can be entered in the do file that provide FREESTYLE with information such as the number of routing and cleaning passes to make, which layers to cut off (avoid routing on), via grid spacing, and to which file the routes should be written. The user can also specify in the do file that FREESTYLE generate a status file. The status file can be monitored during the routing progress.

Once autorouting is complete, the routes can be loaded into the layout in FINESSE, completing the module design. The information that is now in the completed design can be used to fabricate the module.
3.8 Conclusion

The previous sections have outlined the design process used when working with FINESSE MCM™ and FREESTYLE MCM™. The steps outlined were used to design and route the UDSP MCM for NSWC. Specifications indicated by NSWC had to be considered before design of the module was started. These specifications included that low temperature cofired ceramic (LTCC) technology be used to fabricate the MCM with surface dimensions of 2x2". The bottom surface was to be equipped with a 144 pin grid array (PGA) to match a footprint provided by NSWC. Figure 3.4 illustrates the basic layout of the PGA. The top surface of the module was to be designed to enclose mounted components. This was designed by leaving area around the edge of the surface of the MCM free of components and signal lines. This area was to be later accommodated with a brazing ring for lid attachment.

The following chapter indicates how the MCM was designed and routed using the FINESSE MCM™ and FREESTYLE MCM™ software. The module was designed to meet specified NSWC requirements and to meet with typical MCM-C design values.
Figure 3.1. FINESSE MCM™ file structure.
Figure 3.2. Example of a package with diepads, bondpads, and wirebonds. Wire bonds made and bondpads placed with via template.
Figure 3.3 Comparison of through and staggered vias.[15]
Figure 3.4. Bottom surface of module illustrating PGA.
CHAPTER IV

MODULE DESIGN USING FINESSE MCM™ AND FREESTYLE MCM™

4.1 Overall Design

A schematic of the overall electrical design is illustrated in Figures 4.1. The design was first completed with eight tape layers, line widths of five mils, and line spacings of five mils. Bondpad size was 5x10 mils and the via size was defined as seven mils in diameter (the recommended via size for use with low temperature cofired ceramic (LTCC) tape systems). The line width for the TOP layer was defined as one mil, which is comparable to the actual width of a wire bond. Components and metallization on the surface of the substrate were given a clearance from the edge of the module of 350 mils. This clearance was specified to accommodate for the brazing ring to be used for attaching the lid. Clearance from the edge for metallization of subsequent layers was defined as 40 mils which is equal to the distance from the edge of the substrate to the center of the pin grid array (PGA) pads on the outer ring.

It was necessary to complete a second design to increase processing capability and to improve the reliability of the module. This was accomplished by increasing the line width, line spacing, and bondpad size. Component definitions were modified to increase spacing between bondpads and to accommodate for the increase in bondpad size. It was desired to achieve line widths and line spacings of ten mils, and a bondpad size to of 10x10 mils. The bondpad locations were modified for each component, using ten mil
spacing between the bondpads or larger, if space allowed. Bondpads were placed a
distance from the edge of the die such that wire bonds would be approximately 40 to 100
mils in length. The preferred range in which wire bonds can easily be fabricated is
between 40 and 90 mils.[18] Problems occurred when bondpads were placed around the
two components with the most connections -- the BX1750 and the XILINX processors.
There was not enough room around either component to have ten mil wide bondpads with
ten mil spacing, and keep the wire bonds between 40 and 100 mils long. For the BX1750,
the ten mil wide bondpad was used, but the spacing had to be decreased to seven mils.
The XILINX presented a larger problem because of the numerous connections being made
to the component. To keep to the 40 to 100 mil goal for wire bond length, the bondpad
size had to be reduced to 6x6 mils and the spacing between the bondpads was reduced to
six to seven mils. The final design for this project used seven mil lines with five mil
spacing on the first two tape layers (I1 and I2), and ten mil lines with ten mil spacing on
subsequent layers. Although it was desired to have ten mil lines with ten mil spacing on all
layers, the XILINX and the BX1750 forced a reduction in line width and spacing on the
first tape layer. This carried over to the second layer because the vias extending down
through the first layer to the second layer could only be five mils apart and seven mils
wide. Routing from these points on the second layer to subsequent layers could be spread
out to achieve the desired ten mil line width and ten mil spacing. Figure 4.2 depicts this
situation. All other aspects of the layout design remained the same as that of the previous
design that was routed entirely using five mil lines and spaces.
4.2 The Design Process

The following is a summary of the overall design process for this project. The summary gives an overall view of how the final design was accomplished using the FINESSE MCM™ and FREESTYLE MCM™ software.

First, the startpoint.mcm file was altered by changing the standard unit of measure from millimeters to mils. A circuit was opened, starting from the startpoint.mcm file, and named. The next step was to set the parameter to define the number of signal layers for the module (the SIGNAL LAYERS parameter). For this circuit design, the number of layers was set to ten. At least eight tape layers were needed to ensure structural integrity when using LTCC tape systems. The final design for this module used eight layers of tape. A profile of the module is shown in Figure 4.1. Of the ten layers defined in FINESSE, two layers were not in fact physical tape layers. These two layers were the TOP and BOTTOM layers. The actual tape layers were defined as INNER layers. The TOP layer is where the diepads were defined. Connections were made to the surface layer of the module (layer 11) by wire bonds. During the routing process, the TOP layer was cut off so no routing could be performed on that layer. If routing had been allowed on the TOP layer, the signals would have been created on a nonexistent physical layer. The BOTTOM layer is also not a tape layer, but consists of the screen printed PGA array. This layer was also cut off during the routing process because it was undesirable to have signal lines on the bottom surface of the module.
The ANTI LAYERS parameter was also set before design work began. This parameter defines the number of "mask" layers. The mask layers are were via locations are defined, whereas signal layers are where the signal lines are defined. The ANTI LAYERS parameter was also set to ten in order to have a via mask for each signal layer. If the correct number of ANTI LAYERS had not been defined, FINESSE would not have been able to process the via locations and send them to a file.

The SIGNAL LAYERS parameter and the ANTI LAYERS parameters were defined before padstacks were made. Padstack definitions require the user to declare on which layers the padstack is available. Diepads, for example, only needed to be defined on the TOP layer because that is the only place they were used, but vias needed to be defined for all layers because they were used to route down through the BOTTOM layer. Defining padstacks therefore requires that the number of layers be predetermined. If the number of layers is redefined after the design process has been started, the padstacks, as well as several other design criteria, would have to also be redefined. Changing the number of layers can require the user to make many changes in the existing design for it to be consistent with the new number of layers. The user can easily make errors when making these changes, therefore it is best to define the number of layers before any design work is completed to avoid possible confusion and error.

The diepad and bondpad padstacks were created next. The diepads were defined as 4x4 mils and, as stated previously, the bondpads were defined as 10x10 mils and 6x6 mils. The via padstack was also created at this time with a diameter of seven mils. Before
using any of these padstacks, the VIA NAME parameter had to be considered. This parameter is changed before a padstack is placed so that the desired padstack will be used. For instance, while creating components the VIA NAME was set to DIEPAD, but if a circular via was desired in the layout, the VIA NAME parameter had to be changed or else FINESSE would place a square diepad rather than a circular via. It was necessary to change the VIA NAME parameter to DIEPAD before package definitions were created.

The package definitions were made next using the specifications found on the data sheets supplied by vendors. Rectangles were drawn to create each component's outer dimensions. Diepads were placed on the rectangles by visually analyzing their approximate locations from the data sheets. The locations of the diepads were not critical because the wire bonding process does not require perfect alignment from the diepads to the signal lines.

After successfully placing the diepads, the bondpads were placed by creating a via template. As was discussed previously, the VIA NAME had to be changed to acquire the padstack with the desired dimensions. For making the via template, the VIA NAME parameter was changed to BONDPAD. The via template was placed by first choosing the diepad where the wire bond would originate. The point desired for termination of the wire bond was selected a distance away (approximately 40 to 100 mils) from the component to indicate where the bondpad was to be placed. The point was chosen again to place the bondpad at that position. The bondpad appeared and the procedure could be continued.
with another diepad. The above procedure was accomplished for each component until all the packages were completed and saved.

The PGA array was also made as a component. A round padstack was made with a diameter of 75 mils and placed according to the pattern indicated by specifications. The PGA array was placed in the layout at the same time as the other components.

With the components completed and the netlist ready for importing, the layout could be started. Using the "open layout" command from the pull down menu, FINESSE prompted the user for additional information, such as the location of the parts list and netlist files, and then the layout state was accessed.

After opening the layout, the layer rules had to be set. First, the "build order" was defined by making the TOP layer the first signal layer and the BOTTOM layer the last signal layer. The INNER and MASK layers were defined between the TOP and BOTTOM layers in descending order, with the MASK layers staggered in-between the INNER layers. To prevent through vias, the layers had to also be "paired." The TOP layer was paired with I1, I1 with I2, I2 with I3, and so on until the BOTTOM layer was reached, which was paired back up to layer I8. A via could therefore go from layer I1 to I2 because they were paired, but not from layer I1 to I3, since they were not paired, thus preventing a through via.

Layer rules were also defined for line widths, spacing, and clearances. Line widths were set to one mil for the TOP layer, seven mils for layers I1 and I2, and ten mils for subsequent layers. Line spacing was set to one mil for the TOP layer, five mils for layers
I1 and I2, and ten mils for subsequent layers. Clearance from the edge of the module for
the TOP layer and layer I1 was defined as 350 mils to allow space for the brazing ring.
Clearance from the edge on subsequent layers was 40 mils.

With the layer rule modification complete, the components could be placed. One
parameter setting that was modified to assist with component placement was the
COMPONENT CLEAR parameter. This parameter would give an error message if a
component was placed too close to another component. This parameter was first set to
45 mils, but was overridden in special cases to place some components closer than the
specified clearance.

Using the "place component" command from the pull down menu, each component
was accessed. Each component (complete with via template) appeared in outline form,
attached to the mouse cursor so that it could be positioned as desired. As the components
were placed, a string of connections going from the component to others that had been
placed (the component net) would appear. By rotating the component and changing its
position, the number of crossovers in the net could be reduced. This allowed for fewer
conflicts between connections with one another, and therefore routing could be
accomplished more easily.

A tool that also assisted with device placement is the density histogram. This tool
was accessed from the pull down menus with the "display density" command. Graphs
appeared at the top and to the left of the drawing, representing signal density. Large
spikes in these graphs would represent an extremely dense signal area, indicating that the components should be rearranged to provide a more uniform signal distribution.

Once all the components were placed, via fanouts were incorporated into the design to help with the routing, as discussed previously. All fanouts originated from bondpad locations on layer I1 and terminated on layer I8. A staggered via configuration was used for all fanouts. After the via fanouts were added, the design was ready to be routed.

4.3 The Routing Process

The FREESTYLE MCM™ autorouter could be run while logged in from the workstation console or it could be run in batch mode using a "do" file. It was found that running FREESTYLE from the console was not feasible because the routing process consumed a large amount of time (twenty-four hours, if not more). Instead of running FREESTYLE from the console, a "do" file was written that contained information for FREESTYLE on which layers to forbid routing, the via grid spacing, the number of routing passes to complete, the number of cleaning passes to complete, and where to write the routes file and status file. An example of a "do" file is shown in Figure 4.3. The TOP, BOTTOM, and I1 layers were cut off during the routing process to prevent routing on those layers for reasons discussed previously, and the via grid spacing was set to twenty. The number of routing and cleaning passes varied from what is indicated in the "do" file. Often after the requirements of the "do" file were completed, the module was not
completely routed, therefore additional routing passes were accomplished, continuing with the most recent set of routes.

It should be noted in what manner FREESTYLE accomplished its routes and how this was a benefit when the actual part was made. First of all, the module was routed such that a minimum number of vias were used, resulting in extremely high signal density for the first routed layer, with decreasing density on subsequent layers and a sparse density on the last routed layer. Even with the high signal line density on some layers, it was beneficial to have as few vias to fill as possible due to the tedious nature of manufacturing the vias. If the signal lines had been evenly distributed through the module, a high number of vias would have resulted. The directions the signal lines were routed was also important to improve the manufacturability of the part. FREESTYLE routed each layer either vertically across the surface of a layer or horizontally, staggering the layers (vertically, then horizontally, then vertically, and so on as depicted in Figure 4.4). This method prevented any nonuniformities or bulging that would have occurred if routed lines were placed directly on top of each other (Figure 4.5).

Once the routes were completed, the "critic" command was used within FREESTYLE to take out unnecessary path deviations in the signal lines. The "spread" command was also used to add extra space between signal lines when there was room to do so. Neither the "critic" command nor the "spread" command introduce new conflicts when altering routes. Both commands are simply to improve manufacturability.
At this point the routes were saved to a file and loaded into the FINESSE layout, completing the design. With the design complete, plot files were generated to begin making the module. Routed layers are illustrated in Figures 4.6.1 through 4.6.10.

4.4 Conclusion

FINESSE MCM™ and FREESTYLE MCM™ were successfully utilized to design and route the MCM for NSWC. The information obtained from the completed design was used to generate artwork for the fabrication process. The following chapter indicates how the fabrication of the module was accomplished.
Figure 4.1. Cross-sectional view of the NSWC MCM.
Figure 4.2. Widths and spacings of lines and vias. Dimensions are in mils. Layers I5 through I8 are similar to I3 and I4, with 7 mil vias and 10 mil line widths and spacings. Layer I1 and I2 have 7 mil vias and lines, with 5 mil spacing.
autosave on /usr2/finesse/proj1/x00520001/navy.wrs
status_file /usr2/finesse/proj1/x00520001/navy.file
unselect layer TOP
unselect layer II
unselect layer BOTTOM
GRID VIA 20
COST DIAGONAL 0
route 5
clean 2
route 3
write route /usr2/finesse/proj1/x00520001/navy.rte
report status /usr2/finesse/proj1/x00520001/navy.sts

Figure 4.3. Example of a "do" file
Figure 4.4. Illustration of horizontally and vertically routed layers and how they are stacked in a module.
Figure 4.5. Indication of how poor density distribution can warp a package.
Figure 4.6.1. Top layer of wire bonds, diepads, and bondpads (layer TOP).
Figure 4.6.2. Surface layer of module (inner layer I1).
Figure 4.6.3. Second tape layer of module (inner layer I2).
Figure 4.6.4. Third tape layer (inner layer 13).
Figure 4.6.5. Fourth tape layer (inner layer I4).
Figure 4.6.6. Fifth tape layer (inner layer I5).
Figure 4.6.7. Sixth tape layer (inner layer I6).
Figure 4.6.8. Seventh tape layer (inner layer 17).
Figure 4.6.9. Eighth tape layer (inner layer I8).
Figure 4.6.10. Bottom printed layer.


CHAPTER V

MODULE FABRICATION

Before the fabrication process could begin, the necessary materials had to be obtained. A list of these materials appears in Table 5.1. As discussed previously, DuPont's 951 AT Green Tape™ was used as the substrate material. Gold based conducting pastes were used to screen print the conducting areas on the top and bottom outer surfaces of the module. Silver based conducting pastes were used for the conducting lines and for the via fill of the inner layers. A ruthidium based conducting paste was used for the top and bottom layer via fill to act as a transitional medium between the silver paste used in the interior of the module and the gold paste used on the surface of the module. The majority of the conducting areas were printed in silver rather than gold to reduce cost. The gold metallization was necessary for the outer surfaces because it is the required material for wirebonding and for pin attachment.

After the materials for fabrication were obtained, the first step in the process was to blank the tape layers and create the vias. A press was used to punch out 3x3" squares of Green Tape™. Next, the via holes were drilled in the tape layers. This was accomplished by first downloading the via coordinates from the Finesse design for each layer. A file was created for each layer that included via coordinates and size. This information was processed by a computer interfaced with laser unit and then utilized by the laser to drill the required holes in the tape layers. Stainless steel mask layers were
drilled during the process of making vias in the tape layers. After the vias were drilled, they were filled by placing the mask on top of the respective tape layer and a squeegee was used to push the via paste through the mask and into the vias. Each layer was then dried in an oven at 120° C for 10 minutes. Vias were then inspected under a microscope, and vias that were under or over filled were corrected.

After the via coordinates were obtained from Finesse, the Finesse design was utilized to generate artwork that would be used to create the screen printing masks. Each layer design was plotted on rubylith at 10 times the design size with an additional 12% increase to take into account the shrinkage of Green Tape™ in the X an Y directions. Each rubylith layer was then photographed and reduced to produce a photo positive. The screens were made by covering them with emulsion, attaching the positive to the emulsified screen, and then exposing the screen to ultraviolet light. The emulsion under the patterned area of the positive was protected from the light, and the rest of the emulsified screen hardened from the exposure. This pattern was then washed out with warm water and allowed to dry. A screen for each layer was fabricated in this manner. After the screens were completed, they were used to print thick film conducting paste on the corresponding layers.

Once the signal lines were printed on all the interior layers (excluding the top and bottom surfaces), the layers were stacked in a laminating die. Successive layers were rotated 90° to compensate for shrinkage variability in the X and Y directions. The layers were laminated in a hydraulic, uniaxial press under 3000 psi of pressure at 70° C for 10
minutes. The module was then placed in a box oven to through an ash/fire cycle, shown in Figure 5.1. After the module completed the cycle, it was trimmed to the desired size of 2x2".

Next, the outer surface metallizations were printed. The PGA pads were screen printed on the bottom surface of the substrate. DuPont's 5062 was first printed, dried, and fired, followed by a printed layer of DuPont's 5063, which was also printed, dried, and fired. After the bottom surface metallization was printed, the top surface metallization was also printed, dried, and fired. A graphite holder for the PGA pins was constructed to hold the pins in a position so that they would line up correctly with the screen printed PGA. The pins were dropped into the holder and the module was placed on top of the pins. A fused silica setter was placed on top of the module and then the entire unit was flipped over so that the pins dropped down and touched the PGA pins. The unit was then placed in a nitrogen atmosphere at a peak temperature of 390° C and then allowed to cool. Finally, the components were to be attached and wirebonded to the surface bonding pads.
Table 5.1. Materials used for fabrication.

<table>
<thead>
<tr>
<th>LTCC Material</th>
<th>DuPont 951 AT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inner metallization</td>
<td>DuPont 6141 Ag/Pd</td>
</tr>
<tr>
<td>Top layer metallization</td>
<td>DuPont 5715 Au</td>
</tr>
<tr>
<td>Top and bottom layer via fill</td>
<td>DuPont 5750 Ru</td>
</tr>
<tr>
<td>Inner via fill</td>
<td>DuPont 6142 Ag/Pd</td>
</tr>
<tr>
<td>Pin attachment metallization</td>
<td>DuPont 5062 Au and 5063 Au</td>
</tr>
</tbody>
</table>
Figure 5.1. Profile for ash/fire cycle. The profile was based on optimization of processing parameters.
CHAPTER SIX

EVALUATION AND CONCLUSION

6.1 Evaluation of the Module

Evaluation of the module has been accomplished by adjusting for proper alignment when printing signal lines and by evaluating the proper filling of the vias by inspecting them under a microscope. Complete evaluation of the module will include line continuity testing as well as materials evaluation which will include comprehensive spectroscopy to determine reactions at interfaces and via filling. It is also hoped to accomplish resistance and electrical crosstalk measurements.

Currently, the module has been through the fabrication process, except for attachment of the dice. Problems experienced with this initial fabrication were via under and over filling, and nonuniform shrinkage of the tape. Fabrication of successive modules has shown improvement, but addition work is still needed for completion of the module.

6.2 Conclusion

An underwater digital signal processor (UDSP) multichip module (MCM) was designed and fabricated using low temperature cofired ceramic technology (LTCC). A new CAD tool, Finesse MCM, was used to design the module. The layout information form Finesse MCM was used by an autorouter, FREESTYLE MCM, to accomplish the
interconnects. The information from these tools was used to create artwork for fabrication of the module. The module was then fabricated using MCM-C technology.
REFERENCES


VITA

Wendy Hayth-Perdue was born in Portsmouth, Virginia in 1970. After attending high school at Nansemond-Suffolk Academy, she continued her academic career at Virginia Polytechnic Institute and State University (Virginia Tech). She successfully completed her Bachelor's degree in Electrical Engineering with a concentration in Electronics in 1992. Through the influence of the International Society for Hybrid Microelectronics (ISHM), which she was the president of for two years, Wendy decided to further her education by pursuing a Master's degree in Electrical Engineering at Virginia Tech. Her Master's work involved research in the area of multichip modules. She continues to pursue her education through the Ph.D. program in Electrical Engineering at Virginia Tech, extending her interests into the realms of radio and microwave frequencies.

Wendy Hayth-Perdue