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DESIGN OF HIGH-DENSITY DC/DC CONVERTERS

by

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(ABSTRACT)

Zero-Voltage-Switching Multi-Resonant-Converter (ZVS-MRC) techniques are applied with hybrid microelectronics fabrication technologies to design and implement efficient, high-density (>50 W/in^3) dc/dc converters.

A low-profile high-density power stage of a 25 W dc/dc flyback ZVS-MRC is designed and built, and experimental results are shown. A high-density control circuit for a 50 W forward ZVS-MRC is designed using an integrated controller. This circuit is implemented into the high-density power stage previously designed by Tabisz and Lee to attain an overall converter power density of above 80 W/in^3. A low-profile interleaved winding structure, fabricated by laminating copper-on-polyamide, for the transformer in the 50 W ZVS-MRC is introduced. Finite element analysis is performed to show the advantages gained with this structure.

To my mother, Wong Chee Cheng

and my wife-to-be, Stella

with all my love

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1 INTRODUCTION

High-density dc/dc switch-mode power converters are increasingly used in everyday life. Their significant presence can be felt in the medical, computer, manufacturing, automobile, distributed power systems and aerospace industries, among others. In medicine, the ever-increasing demand for artificial organs requires miniature power supplies for its industry's electronics. The computers require high-density power supplies for use in laptops. In the automotive industry, compact and light weight power supplies feed ever increasing electronic processors to provide an "ergonomic" environment and yet keep down the weight of the automobile to enable fuel economy.

The size of magnetic and capacitive components, typically contributing to a major portion of a power converter's volume and weight, can be reduced significantly by increasing switching frequency into the megahertz range.

Conventional pulse-width-modulation (PWM) converters operating at such high switching frequencies are usually accompanied by increased switching stresses and losses. The presence of leakage inductances in transformers and output capacitance in semiconductor devices causes the power devices to undergo inductive turn-off and capacitive turn-on, respectively. Inductive turn-off causes large voltage spikes across the power switch, increasing switching stress, loss and noise. Capacitive turn-on causes the energy stored in the output capacitance, $\frac{1}{2}$ CV^2, to be dissipated internally. Several techniques have been developed to improve the switching behavior of semiconductor devices at such high frequencies [1]. The zero-voltage-switched (ZVS) multi-resonant conversion (MRC) technique, developed by Tabisz and Lee [2], removes the undesirable effects of parasitics by incorporating all of the parasitic elements into a resonant network around the semiconductor

devices. The resonant network so formed causes all the semiconductor devices to operate with ZVS. This technique substantially reduces the switching losses and permits efficient operation in the megahertz range.

Hybrid microelectronic technologies have played major roles in the implementation of high-density circuits. The combination of the multi-layered thick-film fabrication technique and surface mount technology has been a successful alternative to multilayer printed circuit boards as the main interconnection technology in modern electronics. Through an additive deposition process, conductor traces and insulation layers are printed onto a thermally conductive substrate. With shorter and well-defined traces achievable through this process, lead inductances in the circuit are kept to a minimum. Components can be surface-mounted to achieve an integral low profile structure. Monolithic chips can be interconnected through thermosonic and ultrasonic wire bonding operations. Substrates with better thermal conductivity and surface properties are increasingly available. Copper clad substrates can be used to supplement the thickness and material homogeneity of conductor traces otherwise not achievable through thick-film printing. Circuits etched on thin films or foils as substrates present yet another alternative/addition to the fabrication of high-density circuits.

With increased circuit density achievable through hybrid microelectronics and other multilayer circuit technologies, and the problems of parasitics at multi-megahertz operating frequencies resolved with the application of the ZVS-MRC technique, innovating efficient dc/dc converters with extremely high power densities present an interesting endeavour.

This thesis revolves around three high power-density related projects. Chapter 2 studies the feasibility of designing and implementing a low-profile and high-density power stage of a dc/dc 25 W flyback converter. Chapter 3 studies the feasibility of designing and

implementing a very high-density control circuit to supplement the high-density power stage of a 50 W forward ZVS-MRC, previously designed by Tabisz and Lee [2]. Chapter 4 examines the copper losses incurred and improvements to be made in the low-profile power transformer used in the forward converter of the previous chapter. Chapter 5 summarizes the work done.

2 LOW-PROFILE FLYBACK ZVS-MRC

2.1 Introduction

Flyback converters are popular in applications where low cost is of primary concern. The low cost of this converter stems from its low parts count and simplicity. In addition, this converter is extremely appealing to miniaturization through thick-film hybridization.

A high-frequency flyback dc/dc converter using ZVS-MRC techniques is designed and built. The conversion technique governing this topology enables very high switching frequency operation leading to even smaller components and lower cost without sacrificing efficiency.

In this chapter, a detailed steady-state analysis is performed and conditions leading to ZVS outlined. The specifications for a board mountable flyback ZVS-MRC is given, and the design of this converter is described in detail. The construction of the breadboarded circuit is discussed. Power stage optimization and dc electrical characteristics will be presented. The fabrication process of a similar circuit built using thick-film hybrid techniques is briefly described. The electrical characteristics of the thick-film flyback converter are presented. Waveforms for both circuits are presented, and finally, a comparison between the two circuits is made and discussed.

2.2 Steady-State Analysis

Figure 2.1 shows the circuit diagram of a flyback ZVS-MRC. The resonant inductor, L_R, absorbs the transformer leakage inductance. C_S is placed across the switching transistor to absorb its output capacitance. C_D is placed across the secondary of the transformer to absorb the junction capacitance of the rectifier and the interwinding capacitance of the transformer windings. L_R, C_S, and C_D form a resonant network that provides ZVS for the two semiconductor devices.

Figure 2.1 also shows the theoretical waveforms of the flyback ZVS-MRC. There are five stages of operation in one switching cycle. To simplify the analysis of the operation, the secondary circuit of the transformer is reflected into the primary side, shown in Fig. 2.2. The following assumptions are made in the analysis:

(1) The magnetizing inductance of the transformer is sufficiently large so that the magnetizing current is constant and can be replaced by a constant current source, I_M.

(2) The output capacitance, C_F, is sufficiently large so that the output ripple voltage is neglected.

(3) The winding resistance and wire resistance are negligible.

(4) The semiconductor devices are ideal, where there are no time delays in turn-on or turn-off, no leakage current flowing during the off-state, and no forward voltage drop.

The analysis is done by deriving the state equations for each stage and then solving for them using Laplace transforms.

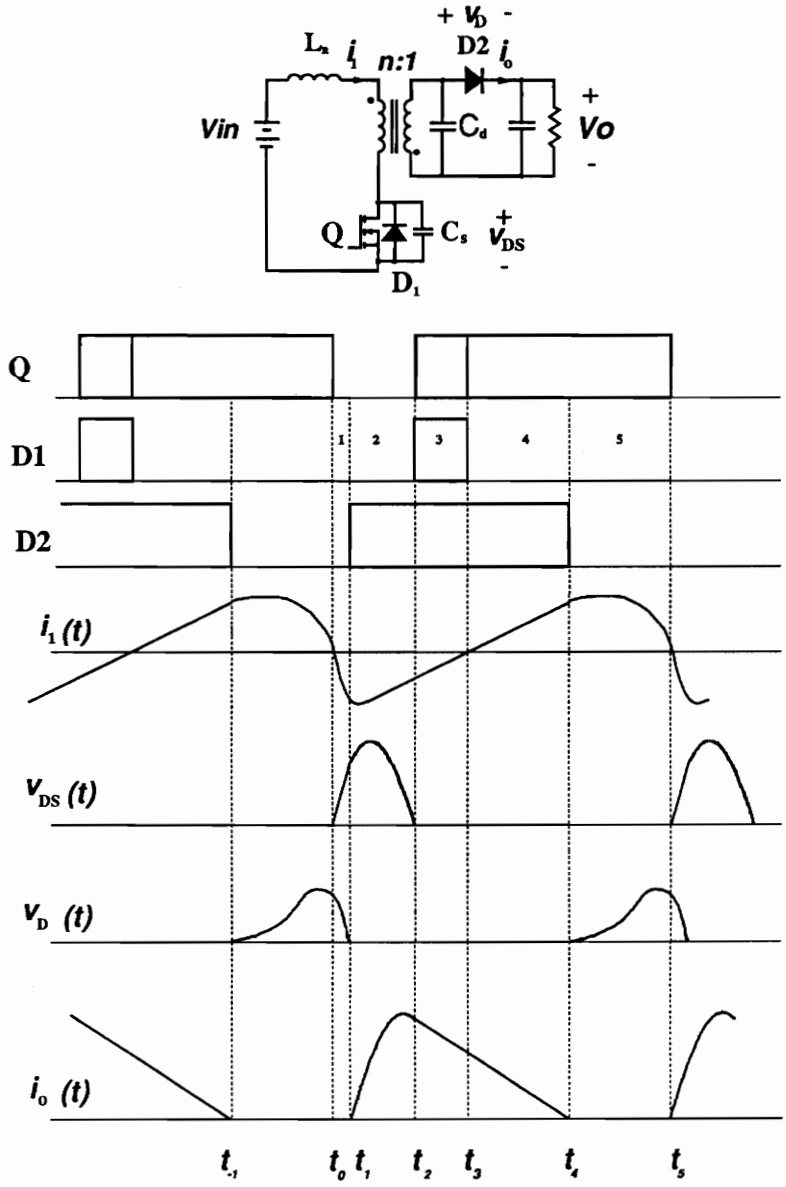


Figure 2.1. Flyback ZVS-MRC Steady-State Waveforms

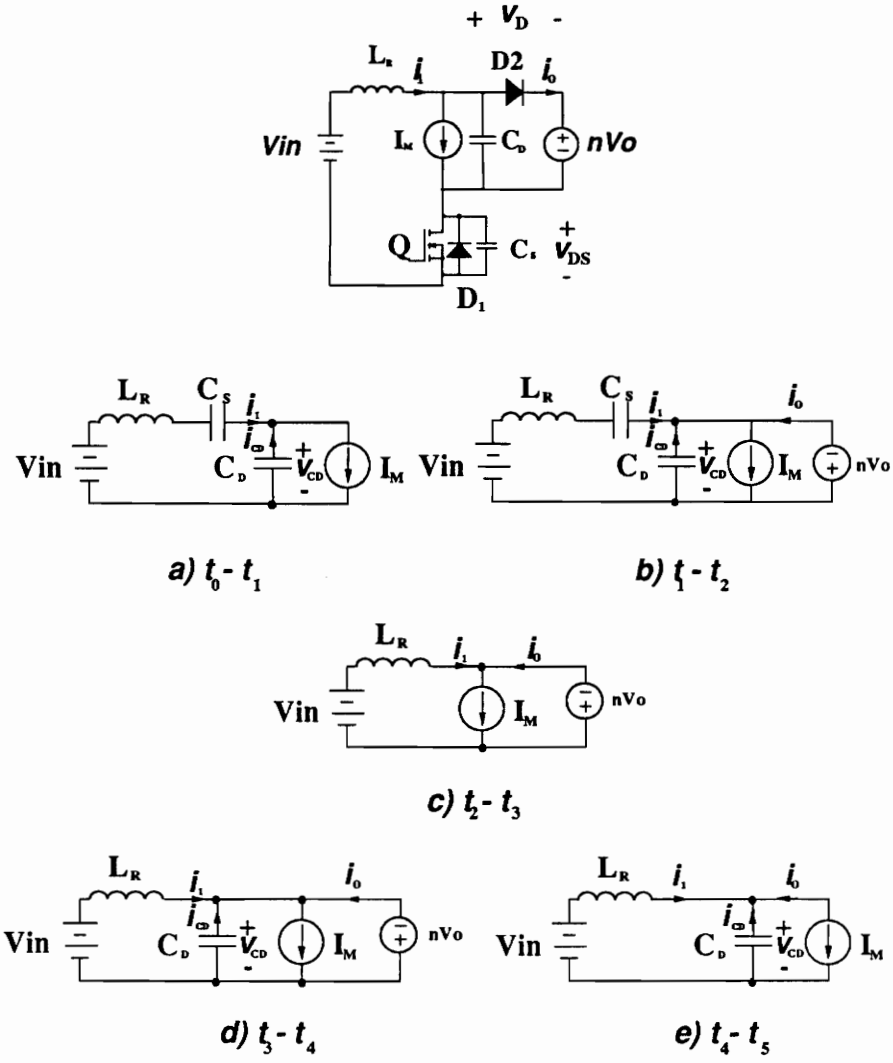


Figure 2.2. Equivalent Circuits at Different Stages

Stage 1 (t_0 - t_1): Q off, D_2 off

Figure 2.2a) shows the equivalent circuit of this stage. After the switch turns off, the magnetizing current, I_M, flows into C_S, C_D, and through L_R. The current through L_R is supplied from the magnetizing current. This current interacts with the resonant components and is decreasing in the form:

$$i_1(t) = \frac{C_S}{C_S + C_D} I_M + \left\{ I_1(t_0) - \frac{C_S}{C_S + C_D} I_M \right\} \cos \frac{(t)}{\sqrt{L_R C_p}} + \left\{ \sqrt{\frac{C_N}{1 + C_N}} \frac{(nV_o + V_i)}{Z_o} \cos(t_0 - t_{-1}) \right\} \sin \frac{(t)}{\sqrt{L_R C_p}},$$

(2.1)

where

$$C_p \equiv \left(\frac{1}{C_S} + \frac{1}{C_D} \right)^{-1},$$

$$Z_o \equiv \sqrt{\frac{L_R}{C_S}},$$

$$C_N \equiv \frac{C_D}{C_S} \text{ and}$$

$$t_{-1} \equiv \text{equivalent to } t_4.$$

The rest of the magnetizing current charges C_D. This circulating current is expressed by:

$$i_{CD}(t) = i_1(t) - I_M = \frac{C_N}{1 + C_N} I_M - \left\{ I_1(t_0) - \frac{1}{1 + C_N} I_M \right\} \cos \frac{(t)}{\sqrt{L_R C_p}} - \sqrt{\frac{C_N}{1 + C_N}} \frac{(nV_o + V_i)}{Z_o} \cos(t_0 - t_{-1}) \sin \frac{(t)}{\sqrt{L_R C_p}}.$$

(2.2)

From the time-varying component of Eq. (2.2), a larger C_D or C_N will cause the resonant frequency to reduce. A higher resonant frequency of the ac circulating current which flows through the transformer windings will induce higher eddy currents. A smaller oscillation frequency with an increase in C_D will therefore mean a reduced eddy current contribution in the transformer.

The voltage across the switch begins to rise in the manner expressed by:

$$v_{DS}(t) = \frac{I_M}{C_S + C_D}(t) + \sqrt{\frac{C_N}{1 + C_N}} Z_o \left\{ I_1(t_0) - \frac{I_M}{1 + C_N} \right\} \sin \frac{(t)}{\sqrt{L_R C_p}}. \quad (2.3)$$

From the sinusoidal component of the above expression, increasing C_D allows the voltage across the switch to rise at a slower rate. $v_{DS}(t_1)$ decreases with an increase in C_D. This value determines the ZVS capability of the converter discussed later.

The voltage on the secondary of the transformer, being the voltage across C_D, falls in sinusoidal manner as expressed by:

$$v_{CD}(t) = v_{CD}(t_0) - \frac{I_M}{C_S + C_D}(t) + \sqrt{\frac{L_R}{C_N(C_S + C_D)}} \left\{ I_1(t_0) - \frac{I_M}{1 + C_N} \right\} \sin \frac{(t)}{\sqrt{L_R C_p}}. \quad (2.4)$$

This stage ends when $v_{CD}(t)$ decreases to -nVo at t_1. At this time, the secondary diode, D_2, starts conduction. The voltage across the D_2 is $v_D(t) = nV_O + v_{CD}(t)$, and at t_1:

$$v_D(t_1) = 0. \quad (2.5)$$

Stage 2 (t_1 - t_2) Q off, D_2 on

Figure 2.2b) shows the equivalent circuit for this stage. The drain-to-source voltage begins to increase and then decrease in a sinusoidal fashion, characteristic of ZVS, expressed by:

$$v_{DS}(t) = v_{DS}(t_1) + i_1(t_1)Z_o \sin\frac{(t)}{\sqrt{L_R C_S}}. \tag{2.6}$$

Since the resonance period of the switch voltage during this stage is fixed by L_R and C_S, the point at which this voltage goes to zero depends on its value at the beginning of this stage. The lower the initial value, the easier it resonates to zero.

The voltage across the rectifier capacitor, $v_{CD}(t)$, is clamped at -nVo. Consequently, $v_D(t) = 0$. The inductor current continues to decrease in a resonant fashion expressed by:

$$i_1(t) = I_M - i_o(t) = i_1(t_1)\cos\frac{(t)}{\sqrt{L_R C_S}} + i_1'(t_1)\sqrt{L_R C_S}\sin\frac{(t)}{\sqrt{L_R C_S}}, \tag{2.7}$$

where $i_1'(t_1)$ is a derivative of the inductor current in stage 1 taken at t_1, and is negative. When $i_1(t)$ goes negative, current is returned to the source. The output current is supplied from the magnetizing current and begins to increase from zero in a sinusoidal fashion expressed by:

$$i_o(t) = I_M - i_1(t). \tag{2.8}$$

This stage ends when the drain-to-source voltage reaches zero at t_2. At this time, the body diode of the switching transistor, D_1, turns on.

Stage 3 (t_2 - t_3) D_1 on, D_2 on

Figure 2.2c) shows the equivalent circuit for stage 3. During this stage, the body diode, D_1, is in conduction. The drain-to-source of the switch is shorted by its body diode, D_1; hence its voltage remains at zero. The resonant inductor current increases linearly from its negative value expressed by:

$$i_1(t) = i_1(t_2) + \frac{V_i + nV_o}{L_R}(t). \tag{2.9}$$

The output current starts decreasing linearly as:

$$i_o(t) = I_M - i_1(t). \tag{2.10}$$

The voltage across the resonant rectifier capacitance, C_D, remains clamped at -nVo. Therefore no current flows through C_D, leaving the magnetizing current to be distributed between $i_1(t)$ and $i_o(t)$. This stage ends at t_3 when the inductor current, $i_1(t)$ reaches zero. At this time, the body diode of the switch turns off, and all of the magnetizing current flows to the output:

$$i_o(t_3) = I_M. \tag{2.11}$$

Stage 4 (t_3 - t_4) Q on, D_2 on

Figure 2.2d) shows the equivalent circuit of the converter during this stage. Mathematically, this stage is the identical to stage 3. The output current continues to decrease linearly:

$$i_o(t) = I_M - \frac{(V_i + nV_o)}{L_R}(t). \tag{2.12}$$

The inductor current continues to increase linearly as:

$$i_1(t) = i_1(t_3) + \frac{V_i + nV_o}{L_R}(t). \tag{2.13}$$

Since the secondary diode is still on, the secondary of the transformer or $v_{CD}(t)$ remains clamped at -nV_o, or $v_D(t) = 0$.

This stage ends when the output current, $i_o(t_4) = 0$. At which time, the secondary diode stops conduction, and the output section of the converter is disabled.

Stage 5 (t_4- t_5) Q on, D_2 off

Figure 2.2e) shows the equivalent circuit of the converter at this stage. Q remains on, while the secondary diode, D_2, is off. The magnetizing current is now being supplied by the source. The inductor current is flowing in a sinusoidal manner from the resonant network formed by L_R and C_D. This current is expressed by:

$$i_1(t) = I_M + \frac{V_i + nV_o}{Z_n} \sin \frac{(t)}{\sqrt{L_R C_D}}, \tag{2.14}$$

where

$$Z_n \equiv \sqrt{\frac{L_R}{C_D}},$$

The voltage across D_2 increases sinusoidally from 0 as:

$$v_D(t) = (nV_O + V_i)\left\{1 - \cos \frac{(t)}{\sqrt{L_R C_D}}\right\}. \tag{2.15}$$

This stage ends when the switch, Q, is once again turned off. The switching cycle repeats.

Lossless Switching

From the operation of $v_{DS}(t)$ and $v_D(t)$, it is evident that both of these semiconductor devices experience ZVS in the MRC. In addition, the secondary diode undergoes ZVS as well.

Also evident from this analysis, the larger C_D, the easier it is to achieve ZVS. This is however accompanied with an increase in the voltage stress on the MOSFET. These characteristics can be verified both experimentally and from the conversion ratio plots of the flyback ZVS-MRC from Tabisz [3]. This ease of ZVS lies largely in the region of Stage 1. As in Stage 2, the resonant period is fixed by L_R and C_S only. In Stage 1, the slower the rise of $v_{DS}(t)$, the easier this voltage returns to zero in Stage 2. The condition for ZVS is governed by the inequality implied from Eq. (2.6):

$$|i_1(t_1)Z_o \sin\frac{(t-t_1)}{\sqrt{L_R C_S}}| \geq \frac{I_M}{C_S+C_D}(t_1-t_0)+\sqrt{\frac{C_N}{1+C_N}}Z_o\left\{I_1(t_0)-\frac{I_M}{1+C_N}\right\}\sin\frac{(t_1-t_0)}{\sqrt{L_R C_P}}. \quad (2.21)$$

The voltage across the flyback rectifier, $v_D(t)$, is shaped to flow in a quasi-sinusoidal manner from the resonant network formed by C_S, C_D and L_R. Interestingly, the current through this rectifier exhibits zero-current-switching (ZCS) prior to turn-off. Therefore the rectifier experiences very low switching losses.

2.3 Design

2.3.1 Design Specifications

The specifications of the high-density flyback ZVS-MRC are given below:

- Input voltage range 25 - 30 V
- Output voltage 5 V
- Output power 25 W
- Minimum switching frequency 1.5 MHz
- Full load efficiency 75 %
- Power Stage Density > 120W/in^3
- Height of Converter ≤0.25 in.

The motivation using these specifications was to prove the feasibility of producing a very high density power converter suitable for use as a board mount power module as part of a distributed power system. This 0.25 inch high module enables direct placement onto the logic board it supplies, creating a closer proximity to the loads. Close proximity to the loads reduces transmission losses.

2.3.2 Converter Design

2.3.2.1 Semiconductor Devices

The design guidelines for this converter are obtained from Tabisz [3]. Several initial values of turns ratio were used. Using these turns ratio, the corresponding stresses on the semiconductor devices were calculated. An optimum turns ratio was then selected based on the semiconductor stresses and losses in the transformer.

The initial turns ratio, n_{ini}, was calculated by (Eqs. (4.25) to (4.32) of [3]):

$$n_{ini} = \frac{\eta_{FL} V_{INmax}}{V_o} = \frac{(0.75)(30)}{5} \approx 5.$$

Turns ratios of 2, 3, 4, and 5 were considered. From here the semiconductor stresses for the each turns ratio considered were calculated.

For a turns ratio of 3, the following steps were used:

$$M_{\max} = \frac{nV_o}{\eta_{FL} V_{INmin}} = \frac{(3)(5)}{(0.75)(25)} = 0.80,$$

$$M_{\min} = \frac{nV_o}{V_{INmax}} = \frac{(3)(5)}{(30)} = 0.50.$$

Using the dc characteristics for the flyback ZVS-MRC [3] reproduced in Fig. 2.3, the minimum value of the normalized resistance, R_{Nmin}, that can support the conversion-ratio range was determined. A minimum C_N was chosen to support ZVS and minimum voltage stress:

$$R_{Nmin} = 0.2\Omega,$$

$$C_N = 2.$$

The minimum load resistance was calculated as:

$$R_{Lmin} = \frac{V_o^2}{P_{o_{max}}} = \frac{5^2}{25} = 1\Omega.$$

The characteristic impedance, Z_o, was calculated as:

$$Z_o = \frac{n^2 R_{Lmin}}{R_{Nmin}} = \frac{(3^2)(1)}{0.2} = 45\Omega.$$

From Fig. 2.3, the MOSFET voltage stress at full load and high line is:

$$V_{DSpeak(HL\text{-}FL)} = 3.5(nV_o + V_{INmax})$$
$$= 3.5(3 \times 5 + 30)$$
$$= 158V,$$

while at low line and full load, it is:

$$V_{DSpeak(LL\text{-}FL)} = 3.6(nV_o + V_{INmin})$$
$$= 3.6(3 \times 5 + 25)$$
$$= 144V.$$

Therefore, the maximum voltage stress occurs at high line and full load, $V_{DSpeak(HL\text{-}FL)}$ = 158 V.

The MOSFET current stress at high line and full load is:

$$I_{Dpeak(HL\text{-}FL)} \le nV_o\left(1 + \frac{1}{M_{\min}}\right)\frac{\sqrt{C_N}}{Z_o} + \frac{I_{o_{\max}}}{n}(1 + M_{\min})$$
$$= (3)(5)\left(1 + \frac{1}{0.50}\right)\frac{\sqrt{2}}{45} + \frac{5}{3}(1 + 0.50)$$
$$= 3.91A,$$

and at low line and full load, it is:

$$I_{Dpeak(LL\text{-}FL)} \le nV_o\left(1 + \frac{1}{M_{\max}}\right)\frac{\sqrt{C_N}}{Z_o} + \frac{I_{o_{\max}}}{n}(1 + M_{\max})$$
$$= (3)(5)\left(1 + \frac{1}{0.80}\right)\frac{\sqrt{2}}{45} + \frac{5}{3}(1 + 0.50)$$
$$= 4.06A.$$

Therefore, the maximum current stress on the MOSFET occurs at low line and full load, $I_{Dmax(LL\text{-}FL)}$ = 4.06 A.

The maximum rectifier voltage stress occurs at low line and full load and is:

$$V_{Dmax} = 2V_o\left(1+\frac{1}{M_{\min}}\right)$$

$$= (2)(5)\left(1+\frac{1}{0.50}\right)$$

$$\approx 30V.$$

The peak current stress on the rectifier at high line and full load is:

$$I_{Dpeak(HL\text{-}FL)} \le 2I_{o_{\max}}(1+M_{\min}) + n^2V_o\left(1+\frac{1}{M_{\min}}\right)\frac{\sqrt{C_N}}{Z_o}$$

$$= (2)(5)(1+0.50) + (3^2)(5)\left(1+\frac{1}{0.50}\right)\frac{\sqrt{2}}{45}$$

$$\approx 19.2A,$$

and the peak current stress on the rectifier at low line and full load is:

$$I_{Dpeak(LL\text{-}FL)} \le 2I_{o_{\max}}(1+M_{\max}) + n^2V_o\left(1+\frac{1}{M_{\max}}\right)\frac{\sqrt{C_N}}{Z_o}$$

$$= (2)(5)(1+0.80) + (3^2)(5)\left(1+\frac{1}{0.80}\right)\frac{\sqrt{2}}{45}$$

$$\approx 21.2A.$$

Therefore the peak current stress on the rectifier occurs at low line and full load, $I_{Dpeak(LL\text{-}FL)} = 21.2$ A.

These calculations were repeated for n=2, 3, 4 and 5, and the different stresses for different values of turns ratio are tabulated in Table 2.1.

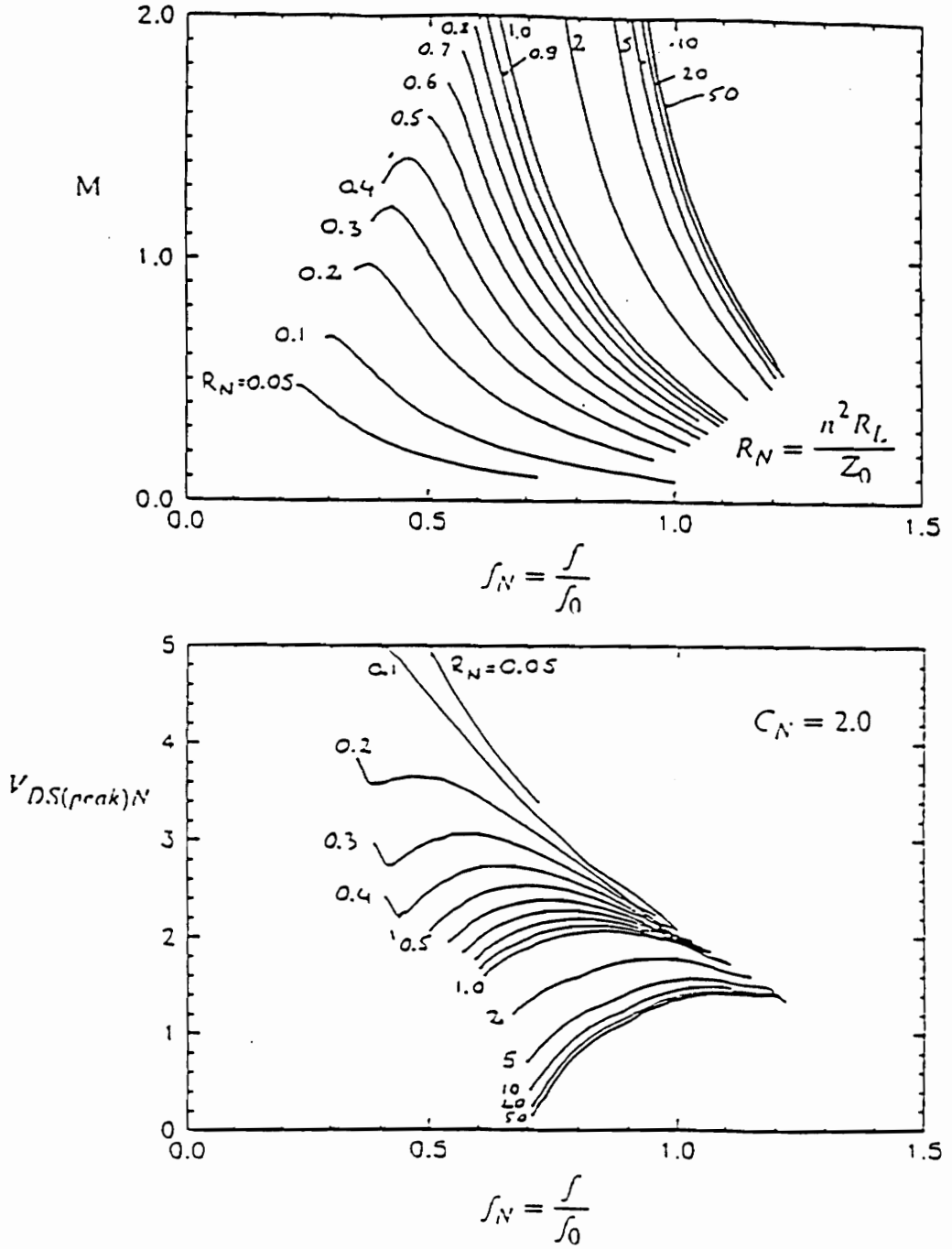


Figure 2.3. DC Conversion Ratio/ Voltage Stress Characteristics of Flyback ZVS-MRC

Table 2.1. Semiconductor Stresses for Different C_N and Turns Ratio, n

n	C_N	R_{Nmin}	Vds_{peak}(V)	V_{Rpeak}(V)	I_{Dpeak}(A)	I_{Rpeak}(A)
2	1.50	0.1	168.0	40	4.70	17.1
	2.0	0.1	178.5	40	4.85	17.3
	3.0	0.1	196.0	40	5.08	17.8
3	1.5	0.2	144.0	30	3.90	20.8
	2.0	0.2	158.0	30	4.06	21.2
	3.0	0.2	171.0	30	4.30	21.8
4	1.5	0.3	140.0	25	3.50	24.3
	2.0	0.3	150.0	25	3.61	24.8
	3.0	0.2	200.0	25	3.43	24.1
5	1.5	0.5	132.0	22	3.40	29.0
	2.0	0.4	148.5	22	3.32	28.3
	3.0	0.3	187.0	22	3.24	27.9

2.3.2.2 Resonant Components

From Table 2.1, to ensure coverage of load range (from 1 A to 5 A) and ZVS, and at the same time reasonable stresses on the semiconductor devices, n=3 and C_N = 2 are selected. From Fig. 2.3, f_{Nmin} = 0.45, and the resonant frequency:

$$f_o = \frac{f_{S_{\min}}}{f_{N_{\min}}} = \frac{1.5 \times 10^6}{0.45} = 3.33MHz.$$

The resonant components are calculated as:

$$L_R = \frac{Z_o}{2\pi f_o} = \frac{45}{2\pi \times 3.33 \times 10^6} = 2.15\mu H,$$

$$C_S = \frac{1}{2\pi f_o Z_o} = \frac{1}{2\pi 3.33 \times 10^6 \times 45} \approx 1nF,$$

$$C_D = n^2 C_N C_S = (3^2)(2)(1000 \times 10^{-12}) = 18nF.$$

2.3.2.3 Transformer Design

The core used was H_{7C4} material from TDK. This material has an initial permeability of 2300, and a saturation flux density of 390 mT at 100°C. Although its saturation flux density is higher at lower temperatures, it is safer to design the core for operation at a higher temperature due to the relatively low efficiency expected from a high-density packaging of the converter. Although a low permeability core exhibits lower core losses, their saturation flux densities are also acceptable. Use of a high permeability core requires relatively fewer turns to achieve a desired magnetizing inductance. The window area of the core will also be smaller, resulting in a lower profile transformer. To support the dc magnetizing current in a flyback converter, the core is gapped. A gapped, high permeability core, H_{7C4}, was therefore preferred.

The magnetizing inductance of the transformer, which stores the flyback energy, was desired to be at least four times the resonant inductance. This was to avoid substantial interaction with the resonant inductance, and also to maintain the ac component of the magnetizing current at a low level. If the ac component of the magnetizing current is high, losses in the transformer windings due to skin effect and proximity effect will increase. These losses are especially significant at MHz operating frequencies.

In this design, B_{DCmax} was set at 225 mT and B_{acmax} at less than 120 mT to anticipate the use of a small transformer.

The dc component of the magnetizing current is calculated as:

$$I_{INmax} \approx \frac{P_o}{\eta_{FL} V_{INmin}} + \frac{I_o}{n},$$

$$= \frac{25}{0.75 \times 25} + \frac{5}{3},$$

$$= 1.33 + 1.67A = 3.00A.$$

The magnetizing inductance is given by the following equation from Snelling [4]:

$$L_m = \frac{N_p^2 \mu_o A_e}{l_g}, \tag{2.16}$$

where $L_m \equiv$ primary magnetizing inductance, mH,

$l_g \equiv$ total length of air-gap, mm,

$N_p \equiv$ primary turns,

$A_e \equiv$ area of core, mm^2, and

$u_o \equiv$ permeability of free space.

The DC flux density is given by the equation:

$$B_{DC} = \frac{\mu_o N_p I_{INmax}}{l_g}, \tag{2.17}$$

or conversely, the length of the air-gap, l_g, is expressed by:

$$l_g(\text{mm}) = \frac{\mu_o I_{INmax} N_p}{B_{DC}} \tag{2.18}$$

$$= \frac{(4\pi \times 10^{-7})(3.00) N_p}{225 \times 10^{-3}}$$

$$= 0.0189 N_p,$$

where $B_{DC} \equiv$ dc flux density, T, and

$I_{INmax} \equiv$ dc current, A.

A closed form of the conversion ratio with respect to the switching frequency of the flyback ZVS-MRC is unattainable analytically. Thus direct determination of duty ratio, $d \equiv t_{on}/f_s$, is not possible. The maximum duty ratio is, however, assumed to be less than 0.7. The maximum ac flux density swing, $B_{ac_{max}}$, is expressed by:

$$B_{ac_{max}} = 2 \times \frac{nV_o d}{f_{Smin} N_p A_e}, \tag{2.19}$$

where $f_{Smin} \equiv$ minimum switching frequency, MHz.

Conversely, the minimum core area, $A_{e\,min}$, is expressed by:

$$\begin{aligned} A_{emin}(mm^2) &= 2 \times \frac{nV_o d}{f_{Smin} N_p B_{ac}} \\ &= 2 \times \frac{3 \times 5 \times 0.7}{1.5 \times 120 \times 10^{-3} \times N_p} \\ &= \frac{116.68}{N_p}. \end{aligned} \tag{2.20}$$

For the same flux densities and magnetizing inductance, various core sizes and gap lengths were calculated from Eqs. (2.16), (2.18), and (2.20). These parameters are tabulated in Table 2.2.

Table 2.2. Primary Turns Versus Core Area

Np	$A_{emin}(mm^2)$	$l_g(mm)$
3	38.9	0.05
6	19.4	0.10
9	13.0	0.15

From Table 2.2, tradeoffs can be seen. For $N_p = 3$, the core area is the largest (slightly more than twice the size of the next closest). For a high-density power hybrid, it is more desirable to have as small a magnetic core as possible. For these reasons, a core area of smaller than 38.0 mm^2 was chosen. For N_p of 9, the core area is the smallest. However, the gap length is also the largest. Although the core loss was apparently the lowest, the copper loss for this configuration was the worst. The relatively large air-gap introduces greater fringing flux. A greater amount of copper material will be intersected by this non-uniform magnetic field, generating greater copper losses from eddy currents. As a compromise, N_p of 6 is chosen together with its core size requirement of 19.4 mm^2 minimum and l_g of 0.1 mm.

A C-core, CY8-8, was chosen. The C-shape geometry was preferred because it presented a compromise between increased circuit density and axissymmetric magnetic performance. The straight edges provide less of an obstruction than the circular edges to additional rectangular component placement.

Therefore, the transformer designed uses half of a high permeability H_{7C4} C-core, CY8-8 from TDK, whose cross-sectional area is 20 mm^2. The other half of the core is an I-piece, ground from the same material. This produces a low profile structure. As the gap would go across the core, the air-gap required is $l_g/2$ or 0.05 mm. The total flux density of the selected core is calculated as:

$$B_{DC_{\max}} = \frac{4\pi \times 10^{-7} \times 6 \times 3.00}{0.1} = 225mT,$$

$$B_{ac_{\max}} = 2 \times \frac{3 \times 5 \times 0.7}{1.5 \times 6 \times 20} = 116.7mT,$$

$$B_{total} = B_{DC_{\max}} + B_{ac_{\max}} = 225mT + 58.35mT = 283.35mT < B_{sat} at\, 100^{o}C.$$

2.4 Hardware

2.4.1 Breadboard Construction

The design was constructed on a breadboard and tested. The switching transistor used was a 200 V MOSFET, IRF640, by International Rectifier. The on-resistance of this MOSFET is 0.18 Ω. The rectifier was a 40 A, 160 mil square, Schottky diode from Semetex. Since the junction capacitance is absorbed in the resonant capacitor, C_D, a larger size higher current rating Schottky diode, such as the 160 A, 300 mil square rectifier from Semetex, could have been used. Again, a compromise was made in order to facilitate optimum use of the physical layout space to achieve a power density goal of above 50 W/in^3. As large dc currents flow through C_D and C_S, these resonant capacitors were NPO chip capacitors with low ESR's. The output capacitors were tantalum chip capacitors.

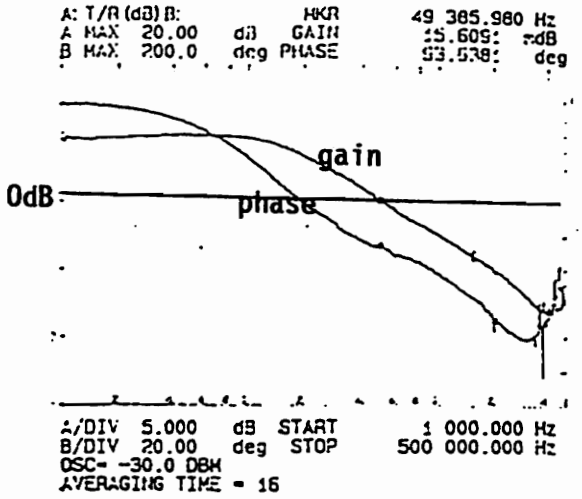
The values of external resonant components added were the calculated values less the parasitic values. For example, the external resonant inductance added is 2.1 μH minus the leakage inductance of the transformer as seen from the primary side. Similarly, the external C_D added is the calculated C_D less the junction capacitance of the flyback diode. As the parasitic capacitances are nonlinear and voltage dependent, initial estimates were made from their specified values at 25 V from the data sheets. Optimization was to be performed at a later stage.

The gate drive and control was provided by the use of Signetics' prototype NE5580 integrated controller [5]. This controller was designed for operation of up to 10 MHz

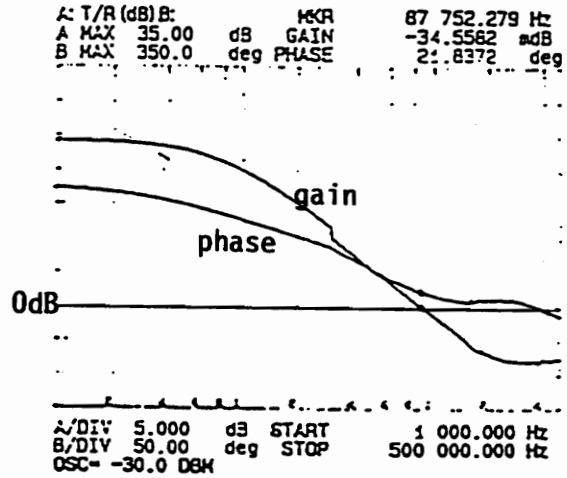
resonant frequency.

The circuit was initially tested in open-loop. The voltage and current waveforms were obtained for various lines and loads. The voltage and current stresses on the switching transistor and the rectifier were recorded and compared to the calculated values.

The circuit was then tested in closed loop. This was done by studying the control-to-output plots measured on the HP 4194A Impedance/Gain-Phase Analyzer, shown in Fig. 2.5. As a small signal model for the ZVS-MRC is not yet been developed, only approximations about the small signal characteristics were made. The open loop control-to-output characteristics measured at low line and full load is shown in Fig. 2.5. From this figure, the first double pole occurs at about 15 KHz. This was probably due to the large magnetizing inductance interacting with the large output filter capacitance. The right-half plane zero is seen at about 80 KHz. Using voltage-mode control, the crossover frequency is thus severely limited by the right-half plane zero and the low double pole. A three-pole, two-zero combination did not provide sufficient phase margin, making the converter unstable. An integrator incorporating a 10 nF capacitor and an 11 $K\Omega$ was eventually used to yield a high dc gain of 80 dB and a crossover frequency of 6.5 KHz with a phase margin of 43.2 degrees at high-line and full-load.



a)



b)

Figure 2.5. Open-Loop Control-to-Output Transfer Functions at Full Loads:

a) Low-Line,
b) High-Line.

2.4.2 Optimization

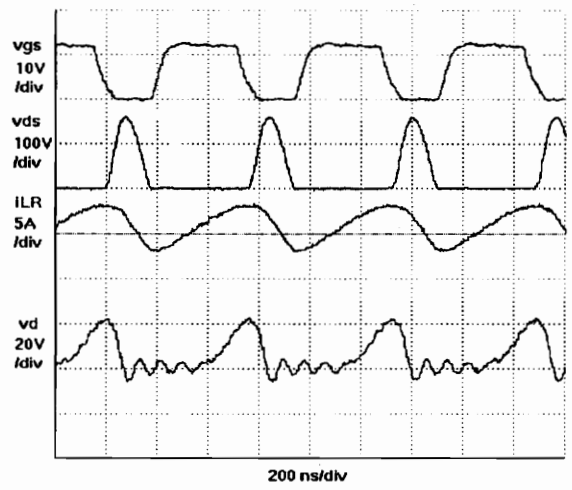
Optimization in order to achieve maximum efficiency was not straightforward. It cannot achieved simply by changing only one resonant component. All three resonant components must be reiterated. The combination of C_S and C_D were adjusted until ZVS and full load at low line could be achieved. Care was taken to observe the voltage stress across the active switch, which increases with C_D. With an increase in C_D, the voltage stress across the active switch, the input current, and the switching frequency is increased. These effects are consistent with the characteristics seen from Eq. (2.21). The resonant inductor was increased to increase the characteristic impedance, thereby reducing the input current. However, this increase in resonant inductance also resulted in an increase in the voltage stress of the active switch, a reduction in the load range, and a decrease in the switching frequency. Too low a switching frequency may cause the ac flux density of the transformer to be large enough, causing saturation.

In order to provide current limiting, the maximum on-time was fixed so that the minimum controller frequency was slightly less than the designed minimum switching frequency. However, an extra long on-time will result in a reduction of load range due to the nonlinear characteristics of the converter as can be seen from Fig. 2.3. From this figure, if normalized frequency f_N is too small, the load lines begin to bend downwards, signifying a reduction in load range. For example, in Fig. 2.3, for $R_N = 0.2$, at f_N below 0.38, the load line starts to dip.

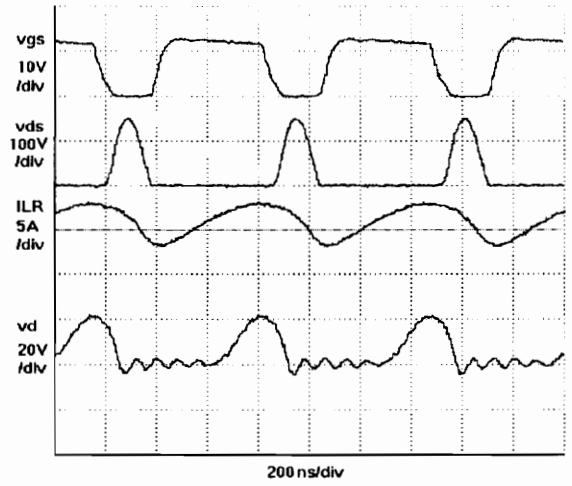
The experimental data for the breadboarded flyback is tabulated in Table 2.3 and waveforms are shown in Figs. 2.6 and 2.7.

Table 2.3. Experimental Data of Breadboard Flyback

Vin(V)	Iin(A)	Vo(V)	Io(A)	Vds_{peak}(V)	fs(MHz)	η(%)
25	1.31	5.01	5.00	151.0	1.52	76.49
26	1.28	5.01	5.00	154.5	1.61	75.42
27	1.24	5.02	5.00	156.5	1.65	74.97
28	1.20	5.02	5.00	156.5	1.69	74.70
29	1.16	5.02	5.00	159.5	1.74	74.61
30	1.13	5.02	5.00	162.0	1.77	74.04
25	1.06	5.01	4.00	127.0	1.80	75.62
26	1.03	5.01	4.00	129.5	1.87	74.83
27	1.00	5.02	4.00	133.5	1.91	74.37
28	0.98	5.02	4.00	137.5	1.95	73.18
29	0.95	5.02	4.00	141.5	1.99	72.89
30	0.92	5.02	4.00	143.5	2.03	72.75
25	0.80	5.04	3.00	110.5	2.12	75.60
26	0.77	5.04	3.00	112.5	2.18	75.52
27	0.75	5.04	3.00	114.5	2.22	74.67
28	0.73	5.04	3.00	117.0	2.27	73.97
29	0.71	5.04	3.00	119.5	2.31	73.43
30	0.69	5.04	3.00	123.0	2.36	73.04
25	0.55	5.05	2.00	95.5	2.54	73.45
26	0.53	5.06	2.00	97.0	2.61	73.44
27	0.51	5.06	2.00	99.5	2.64	73.49
28	0.49	5.06	2.00	100.5	2.69	73.76
29	0.47	5.06	2.00	101.5	2.74	74.25
30	0.46	5.07	2.00	102.0	2.80	73.48
25	0.29	5.08	1.00	81.0	3.15	70.07
26	0.28	5.08	1.00	82.0	3.21	69.78
27	0.27	5.08	1.00	83.5	3.24	69.68
28	0.26	5.08	1.00	85.5	3.29	69.78
29	0.25	5.08	1.00	86.5	3.34	70.07
30	0.24	5.08	1.00	87.0	3.37	70.56



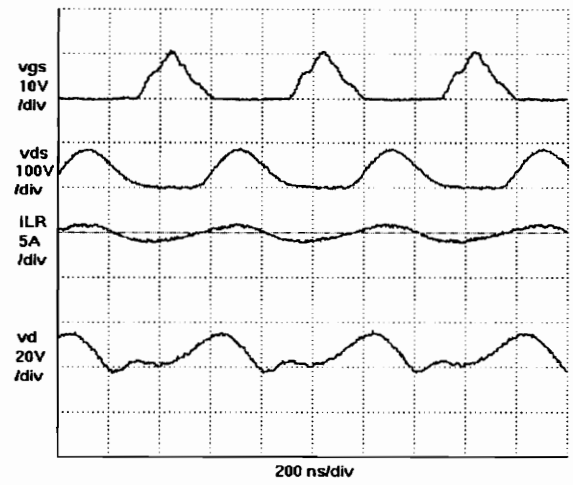
(a)



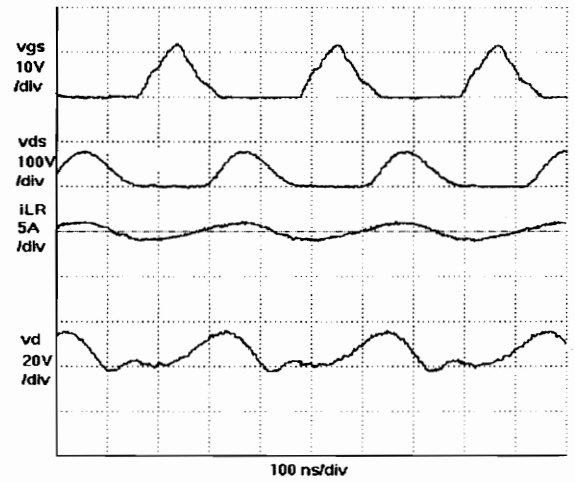
(b)

Figure 2.6: Operating Waveforms of the Breadboarded Flyback at Full Load:

(a) High-Line,
(b) Low-Line.



(a)



(b)

Figure 2.7: Operating Waveforms of the Breadboarded Flyback at 1A Load:

(a) High-Line,
(b) Low-Line.

2.5. Hybridization

2.5.1. Hybrid Layout

The layout of the thick-film hybrid flyback ZVS-MRC is shown in Fig. 2.8. The artwork is generated from a computer-aided-design software package, *MICROCAD*, developed by the Hybrid Microelectronics Laboratory at Virginia Tech.

There were three layers. The first layer consists of the ground plane. A through-hole was opened in the ground plane where the gate of the MOSFET was to be wire-bonded to the output driver port of the controller. If this hole was not opened, ultrasonic aluminum bonding could puncture through the second layer and short the gate to ground. The second layer consists of the isolation dielectric material. This layer electrically isolates the top layer from the bottom layer. During fabrication, this layer was screen printed three times, each print individually fired. This was to overlap any pin-holes present in any one layer. Pin-holes cause undesirable shorts between neighboring conducting layers. Vias opened in this layer were therefore made 5% larger to accomodate the poor resolution gained from repeated printing. The third layer consists of the signal paths. For small signal paths, the conductor width was minimized at 10 mils. For the power paths, the conductor widths were increased to a minimum of 50 mils to reduce the dc resistance.

Apart from the MOSFET, where a chip was used, all other parts were obtained as surface mount packages. Available component sizes were recorded. Every dimension in any component was given with tolerance, so the smaller of the two limits was used. This was to facilitate maximum contact with the conductor pads. The components were then

drawn as blocks with specific dimensions and placed. Component locations needed to be replaced many times during the course of the artwork design to eventually arrive at an optimum layout.

The controller was placed as close as possible to the MOSFET. This was to ensure the shortest path for the output of the controller to the gate of the MOSFET. The output of the converter was laid close to the controller to reduce lead inductance causing a delay to the compensation.

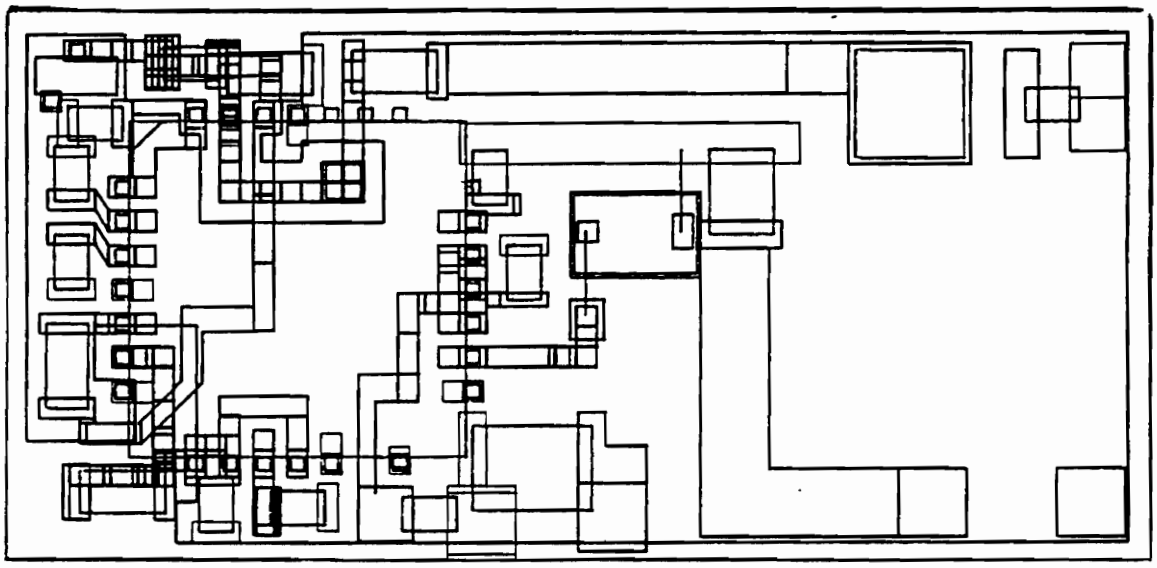


Figure 2.8. Layout of the Thick-Film Flyback ZVS-MRC

2.5.2 Substrate Selection

The substrates considered were Beryllia, Aluminum Nitride, Ferrite, and 96% Alumina. Although Berryllia possesses the highest thermal conductivity, its toxicity limits manual fabrication and handling. Aluminum Nitride has a higher thermal conductivity and lower cost than Beryllia. However, its poor adhesion to thick-film pastes made it an unacceptable choice. Ferrite was also considered as a substrate. The magnetic properties of this substrate was thought to reduce the EMI in the circuit by absorption of the stray magnetic fields. It also seemed viable then to use only one half of another magnetic core to close the magnetic path in a power transformer. The windings could be printed onto the magnetic substrate [6]. This would have the advantage of heat dissipation of copper loss by conduction through the substrate. In terms of production economics, it looked very attractive as then mass production of wound transformers could be automated with repeatable leakage inductance, a parameter very important in power converter design. However, the setbacks in using Ferrite as a substrate offset the benefits gained. The fragility of ferrite material makes processing extremely difficult. A tiny chip will create a propagated crack across the entire substrate. As the material is actually in the form of compressed powder, after repeated processing via multi-printing and firing, more cracks appear from handling. The surface of a ferrite substrate was very rough and uneven. Examined closer, many "potholes" were seen. Adhesion of printed material was poor. 96% Alumina was finally selected as it is very popular due to its ease of handling, good thermal conductivity, and relatively low cost.

2.5.3 Pastes Selection

Conductive and Dielectric pastes were used for the three layers. The first layer consisted of the ground plane, in which a conductive paste was used. The second layer was the insulation layer separating the ground plane from the signal paths which were formed on the third layer. This second layer required a dielectric paste. The third layer used a conductive paste for its signal paths.

Conductive pastes used are primarily required to have low resistivity and strong adhesion to the substrate. The secondary requirements include solderability, suitability for bonding, printing capability, processing conditions, and cost. As examples, gold paste is highly conductive and chemically inert, but the high solubility of common solders in gold makes soldering difficult. It is also very expensive. Copper is of fairly low cost and possess high conductivity, but it has to be fired in an inert or reducing atmosphere to prevent oxidation and subsequent severe reduction of conductivity as well as impairing solderability.

For multilayer work, as well as for providing insulation, dielectric pastes should possess low permittivity, hermeticity, and resistance to flow during repeated firings. Its low permittivity minimizes the capacitive coupling between layers and provides a high breakdown voltage. It must be hermetic to prevent pin-holes from shorting out alternate layers. Good resistance to flow during repeated firings will preserve the fine details of shape, particularly vias or through holes for connection between layers.

2.5.4 Fabrication

The fabrication process started after the thick-film layout was completed. Each layer of the layout was enlarged ten times the actual size. This enlargement facilitated checking of details and registration. The enlarged layers were then individually scribed onto a piece of Rubylith. Rubylith is a two-layer plastic (red and clear) laminate and areas of the red plastic were peeled to define the pattern. Photographic reduction was then used to reproduce the layout on a high contrast film. The image on the film upon exposure is the actual layout of the circuit.

5" by 5" wire mesh screens of 325 and 280 mesh counts were used. Screens typically come in mesh counts of 80 to 475. The larger the mesh count, the higher the resolution but the lower the thickness of the print. For the isolation layer, a screen with a mesh count of 325 meshes per square inch was used. The relatively high resolution was important in producing a more hermetic isolation layer. The isolation layer was then printed and fired three separate times to build up thickness and prevent further pin-holes from occuring. For the ground plane or the first layer, a 280 mesh count screen was used. The resolution of this layer was not as important as the thickness was to reduce dc resistance. One via was opened in this ground layer as a preventive measure against shorting from the top layer when ultrasonic wire bonding was used to attach the gate of the power MOSFET to the gate path on that top layer. The ground plane was printed two times post-fired to build up thickness. Figure 2.9 shows the comparison of thickness achieved between one print and three post-fired prints.

Relatively thick emulsions from ULANO with a CDF rating of 7 were used for all layers. These emulsions were then applied onto the screens and dried. The negatives

containing the images of each layer were aligned on their respective screens. These prepared screens were then exposed under ultra-violet light. The exposed screens were then rinsed with warm water and then dried thoroughly.

The first layer, using a Silver paste, was doubly printed with a squeegee speed of 20 cm/s. The snap-off distance was set at 30 mils, and a 45° angle of attack squeegee with an applied force of 12 N was used. The relatively large snap-off distance was to reduce the cling zone formed from thick printing over a large surface area. These parameters were to ensure an evenly thick distribution of the paste over a wide area. Subsequent printing of the first layer required an additional snap-off distance of 5 mils each time. The paste viscosity of the Silver paste used was enhanced to achieve good columniation of the conductor during printing and not to degrade resolution. Two methods for doing this were reported by Hopkins [10]. Both methods require sophisticated preparation, a simplified method used here was to refrigerate the paste. In this way, the cold paste was still very viscous when printed onto the substrate. The conductors printed appeared to be thick and well resolved. Three separate printings and firings of the first layer yielded a post-fired thickness of 1.1 mils.

The second layer used a dielectric composition paste 5704 from duPont. Again the paste was refriegerated prior to immediate use. The thickness achieved in one single print was not as important as the resolution of the vias. A 325 mesh screen was used for good via resolution. A relatively slower squeegee speed of 10 cm/s was used to ensure uniformity of print rather than thickness. A double wet print pass was used to increase uniformity and minimize pinholes. A 45° angle of attack squeegee with a force of 12N and a snap-off distance of 30 mils were used. Three separately post-fired printings produced a thickness of 1.8 mils.

In the third and final layer, the signal paths used the same silver paste as for the first layer. The snap-off distance was set at 20 mils due to relatively small areas to be thick printed on. A 325 mesh count screen was set for high resolution of signal lines as these lines were typically of width 10 to 20 mils. Other than the snap-off distance, the printer settings were the same as for the second layer.

Upon completion of all three layers, the substrates were tested for short and open circuits. A yield of 100% was achieved. Apart from the magnetics, all other components were reflow soldered. Solder paste with added 2% silver composition was used. The 2% silver serves as an additive to prevent leaching. The paste was deposited manually because the number of solder pads did not justify screen printing them. The reflow station was set for a maximum belt temperature of 205° celsius and a preheat temperature of 165° celsius. The speed was set at 10 cm/min. The MOSFET die was soldered on prior to attachment of the other components. This was to facilitate ease of wire bonding from the die to the signal paths, without other components, otherwise present, to obstruct the nozzle of the bonder. For reliable bonding, the surface of the conductor paths must be cleaned of oxides. Upon successful bonding and testing of the MOSFET, all other components were mounted. The final package is shown in Fig. 2.10.

Figure 2.9. Fired Thickness Versus Number of Prints:

Top Trace: Single Post-Fired Print,

Bottom Trace: Triple Post-Fired Prints

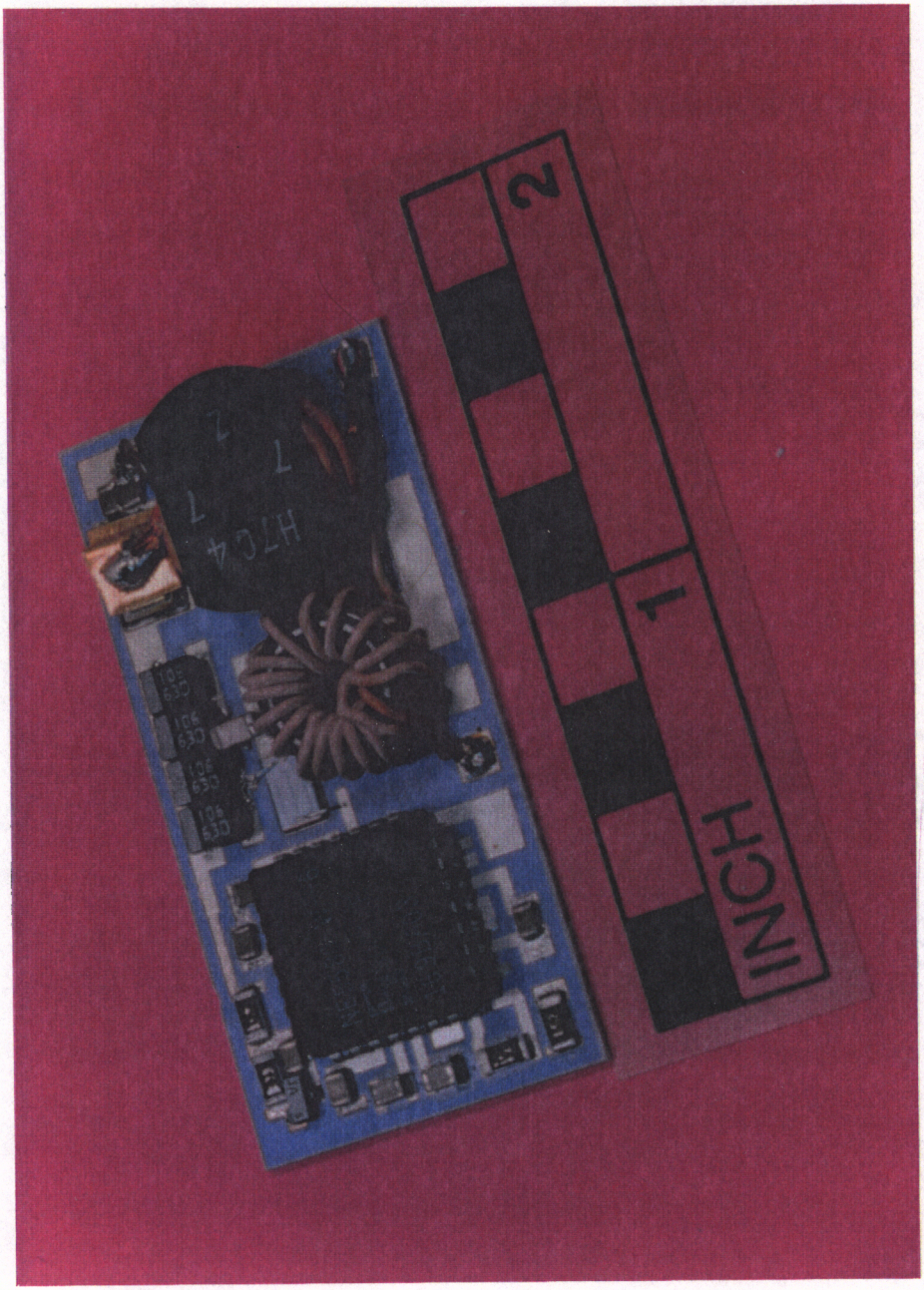


Figure 2.10. Thick-Film Flyback ZVS-MRC

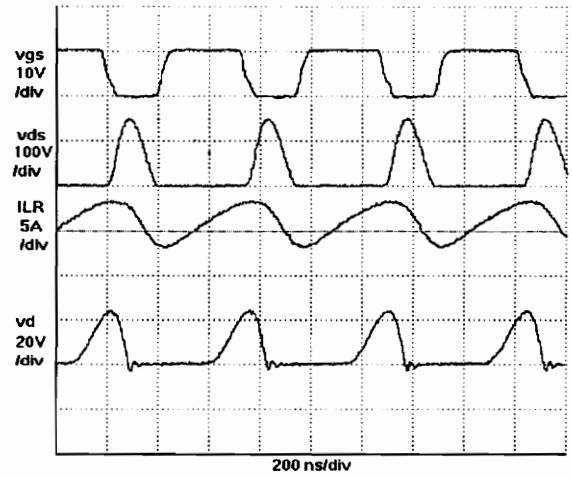
2.6 Electrical Performance and Comparison

The performance of the hybridized flyback ZVS-MRC was recorded with respect to various lines and loads and is shown in Table 2.4. The waveforms are shown in Figs. 2.11 and 2.12. Due to the shorter conductor paths in the hybridized flyback, lead inductances were greatly reduced. Consequently, parasitic oscillations were greatly reduced and cleaner waveforms compared to the breadboarded version were observed. For an equivalent efficiency, however, the voltage stress of the active transistor in the hybridized flyback was 7% lower at high-line and full load. The switching frequency was also higher.

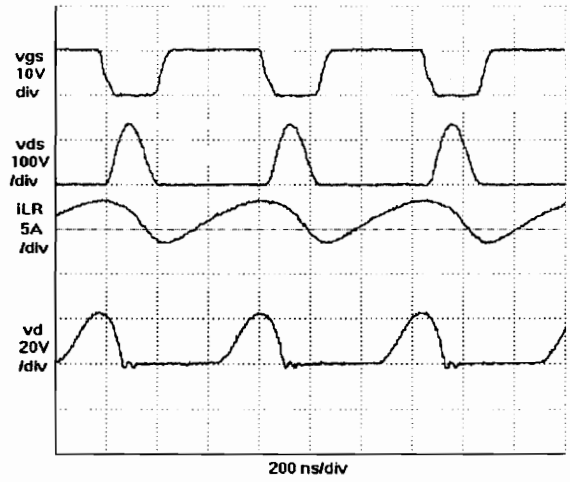
Figures 2.13 and 2.14 provide plots where the comparison of voltage stresses and efficiency with respect to the two flyback versions can be seen clearly. By resorting to currently available substrates which are clad with 10 mil thick of copper on Alumina/Aluminum, the power dissipation will be less and the thermal management enhanced, thereby increasing efficiency and reliability of the circuits. These substrates will resolve the problems generally present with conventional thick-film fabricated power circuits where the power runs are usually too thin.

Table 2.4. Performance Data for Thick-Film Flyback

Vin(V)	Iin(A)	Vo(V)	Io(A)	Vds_{peak}(V)	fs(MHz)	η(%)
25	1.33	5.06	5.00	138.0	1.52	76.10
26	1.29	5.06	5.00	139.0	1.64	75.43
27	1.25	5.06	5.00	141.0	1.70	74.96
28	1.21	5.06	5.00	145.0	1.75	74.68
29	1.17	5.06	5.00	148.0	1.79	74.57
30	1.14	5.07	5.00	152.0	1.83	74.12
25	1.07	5.07	4.00	121.0	1.85	75.81
26	1.04	5.07	4.00	124.0	1.90	75.00
27	1.00	5.08	4.00	126.0	1.94	75.26
28	0.97	5.08	4.00	130.0	1.98	74.82
29	0.95	5.08	4.00	133.0	2.02	73.76
30	0.92	5.08	4.00	136.0	2.07	73.62
25	0.81	5.09	3.00	107.0	2.15	75.41
26	0.78	5.09	3.00	109.0	2.21	75.30
27	0.75	5.09	3.00	112.0	2.24	75.41
28	0.73	5.09	3.00	114.0	2.28	74.71
29	0.71	5.09	3.00	117.0	2.32	74.16
30	0.69	5.09	3.00	120.0	2.36	73.77
25	0.55	5.09	2.00	92.0	2.54	74.04
26	0.53	5.10	2.00	94.0	2.60	74.02
27	0.51	5.10	2.00	96.0	2.63	74.07
28	0.49	5.10	2.00	98.0	2.68	74.34
29	0.48	5.10	2.00	101.0	2.72	73.28
30	0.47	5.10	2.00	102.0	2.74	72.34
25	0.29	5.11	1.00	74.0	3.10	70.48
26	0.28	5.11	1.00	76.0	3.16	70.19
27	0.27	5.11	1.00	77.0	3.18	70.10
28	0.26	5.11	1.00	78.0	3.21	70.19
29	0.26	5.11	1.00	80.0	3.25	69.78
30	0.25	5.11	1.00	82.0	3.28	68.13



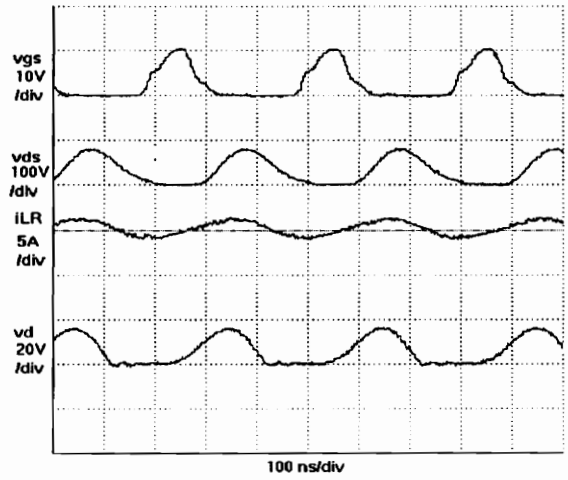
(a)



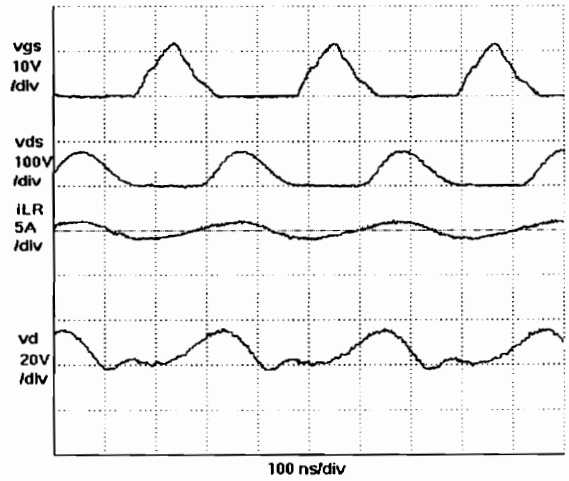
(b)

Figure 2.11: Operating Waveforms of the Hybridized Flyback at Full Load:

(a) High-Line,
(b) Low-Line.



(a)



(b)

Figure 2.12: Operating Waveforms of the Hybridized Flyback at 1 A Load:

(a) High-Line,
(b) Low-Line.

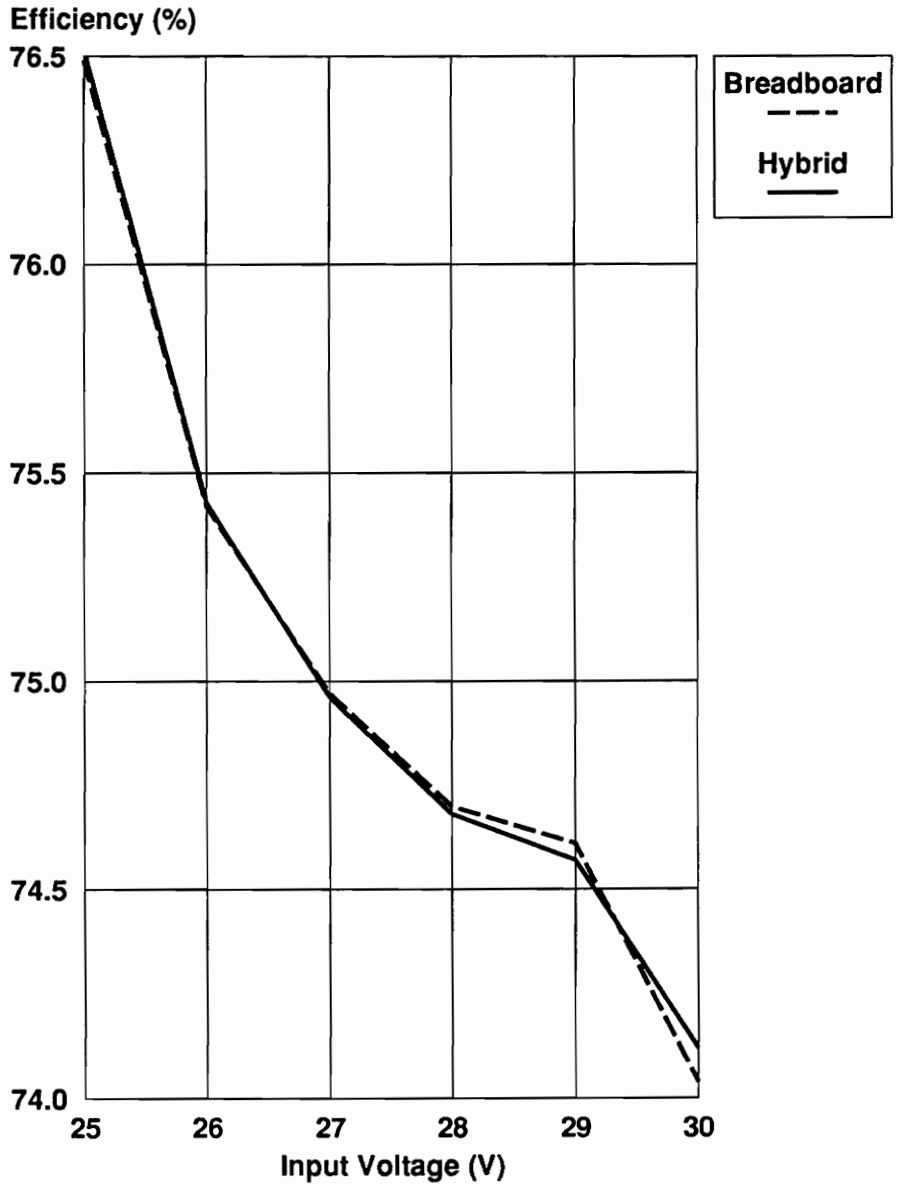


Figure 2.13. Comparison of Full load Efficiency at Different Lines

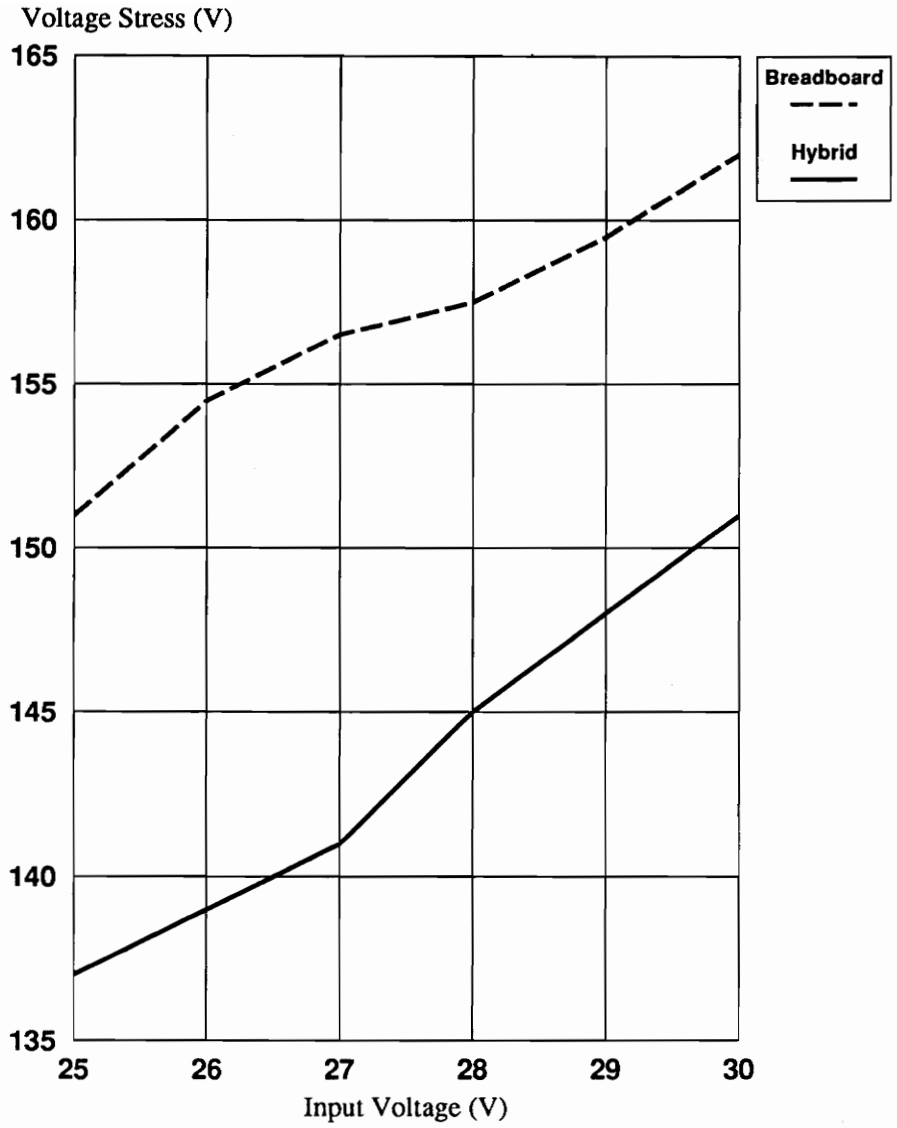


Figure 2.14. Comparison of Full Load Voltage Stress at Different Lines

2.7 Summary

Flyback converters are popular in applications requiring low power levels because of low parts count and simplicity. They combine the actions of an isolating transformer, an output filter inductor, and a flywheel diode in a single transformer. As a result of this magnetic intergration, the circuit provides extremely low-cost and efficient stabilized dc outputs. The low number of parts makes this converter very appealing to hybridization.

The problems associated with parasitics at high switching frequencies are overcome by the application of the ZVS-MRC technique. In this technique, all the parasitics of the components are absorbed in the resonant network formed to shape the transistor and the rectifier voltage in a quasi-sinusoidal fashion. This will enable ZVS for the semiconductor devices. This technique optimizes the efficiency of this converter at high frequencies.

In this chapter, a steady-state analysis was performed. The resonant network comprising of L_R, C_S and C_D shapes the voltage waveforms of both the semiconductor devices to flow in a quasi-sinusoidal fashion. The steady-state analysis also showed that the rectifier experiences both soft turn-on with ZVS and soft turn-off with ZCS and thereby the switching losses on the rectifier are much reduced. A design of the converter was presented. Selection of components with respect to physical size and characteristics were discussed, in particular the planar power transformer. One circuit was built on a bread-board and another on a ceramic substrate using thick-film hybrid techniques. The performance of both circuits were recorded and compared. Waveforms from the circuit fabricated using thick-film hybrid techniques show significantly cleaner waveforms in addition to reduced voltage stress for an equivalent efficiency. The hybridized circuit possessed an overall power density of 55 W/in^3 and attained a full load efficiency of

76.1%. The control circuitry of this converter was not optimized for size as it did not include start-up and self-bias. In the next chapter, a control circuitry is optimized which includes these functions and by utilizing chip and wire techniques, the density of this control circuit can be shown to be made very high.

3. HIGH-DENSITY CONTROL CIRCUIT

3.1 Introduction

A 50 W forward ZVS-MRC had been designed and hybridized [2]. The input voltage range is from 45 V to 55 V. The output voltage is at 5 V, and the minimum switching frequency is at 2.71 MHz. An efficiency of 83% was achieved at full load and nominal line. The crossover frequency of the control was around 80 KHz. Using discrete surface mount components and two pulse transformers for providing feedback isolation, the overall power density of the converter achieved 50 W/in^3.

From the thick-film layout of the converter shown in Fig. 3.1, the control circuit alone occupied more than 50% of the space. This control circuit, which was simplified to facilitate hybridization, provided the basic functions: output voltage control, self-bias and start-up circuits. It did not include under- and overvoltage lockout, overvoltage protection, soft start and overload protection. A project was initiated to reduce the space taken up by the simplified control stage by using an integrated controller to push the overall power density to above 50 W/in^3.

In this chapter, requirements met by the original simplified control circuit are briefly discussed. The integrated controller that meets the requirements is presented. Due to the primary side biasing of the controller, feedback isolation is needed. Various commonly used techniques for feedback isolation are discussed and the one that meets the high-density requirement is presented. The benefits and limitations of using such a technique are shown. The control loop design incorporating the feedback isolation is discussed. To

maintain the integrity of the converter to provide its own bias voltages, the start-up and the self-bias circuitry are shown and discussed. Finally, the hybridization process with respect to the layout and component attachment techniques is presented.

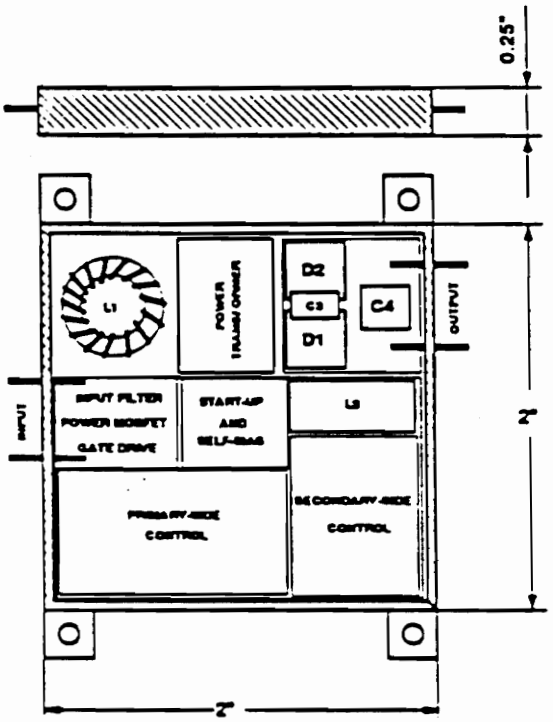


Figure 3.1. 50 W/in^3 Forward ZVS-MRC

3.2 Requirements

In the previous control circuit, the feedback isolation was supplied by use of two pulse transformers: one for on-time control and the other for off-time control. The start-up circuit was implemented using a MOSFET configured in a linear regulation mode. Self-bias was provided from an auxiliary winding of 1.5 turns on the power transformer through a peak detector. The output voltage was regulated by voltage mode control implementing two poles and one zero in the compensation network to provide a bandwidth of approximately 80 KHz.

In the present design, an attempt was made to include basically the same functions and further increase the power density by use of a high-frequency resonant mode integrated controller. The controller must be capable of operation up to 5 MHz, which is the maximum switching frequency for the forward ZVS-MRC designed. The feedback isolation circuitry must be simple and possess very few parts.

To enhance the power density, the total footprint needed to support the control circuitry must be small. Peripheral circuitry, if incorporated for proper operation, should be simple and possess the least parts count possible.

The final design is prematurely shown in Fig. 3.2.

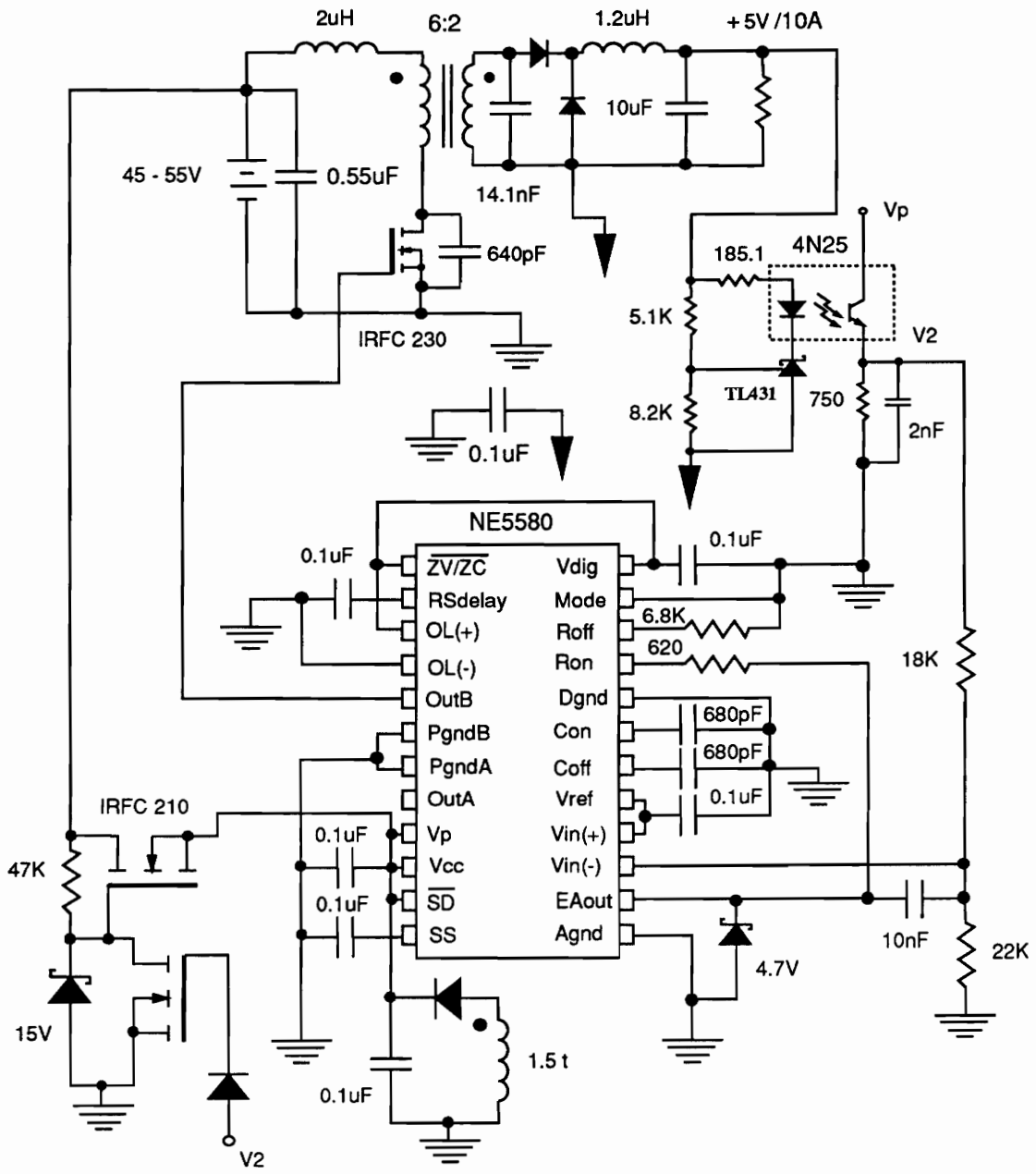


Figure 3.2. Control Circuit for the 83 W/in^3 Converter

3.3 Integrated Controller Features

The integrated controller selected was a prototype resonant mode controller NE5580 from Signetics, which is currently unavailable commercially [5], which was reproduced in Fig. 3.3. This controller is capable of operation at frequencies of up to 10 MHz. It is suitable for ZVS converters since the on-time can be programmed and off-time can be fixed with external capacitors and resistors. The internal error amplifier boasts a 10 MHz unity-gain bandwidth. This controller has provisions for soft start, restart delay, and overcurrent protection capabilities through simple component addition. Furthermore, it possesses an internal gate driver with 1.5 A capability. Housekeeping regulated voltage is also provided within the chip. Automatic overvoltage protection is provided from an internal digital monitoring circuitry within the VCO.

a) Programmable On-Time and Fixed Off-Time

In the forward ZVS-MRC designed, the minimum off-time is determined by the time taken for the voltage across the MOSFET to resonate to zero. This time is then set by a resistor, R_{OFF}, which is connected across the R_{OFF} terminals. R_{OFF} in turn is connected to the V_{DIG} (5 V) pin, which sets up a constant current to charge a capacitor, C_{OFF}, from 1 V to 2.5 V. The conversion ratio of the converter is varied with the on-time. This on-time control is realized by connecting the output of the error amplifier to the VCO through a resistor, R_{ON}, setting up a variable current to charge up a capacitor, C_{ON}, from 1 V to 2.5 V. Therefore, the off-time is fixed while the on-time is varied according to the conversion ratio requirements.

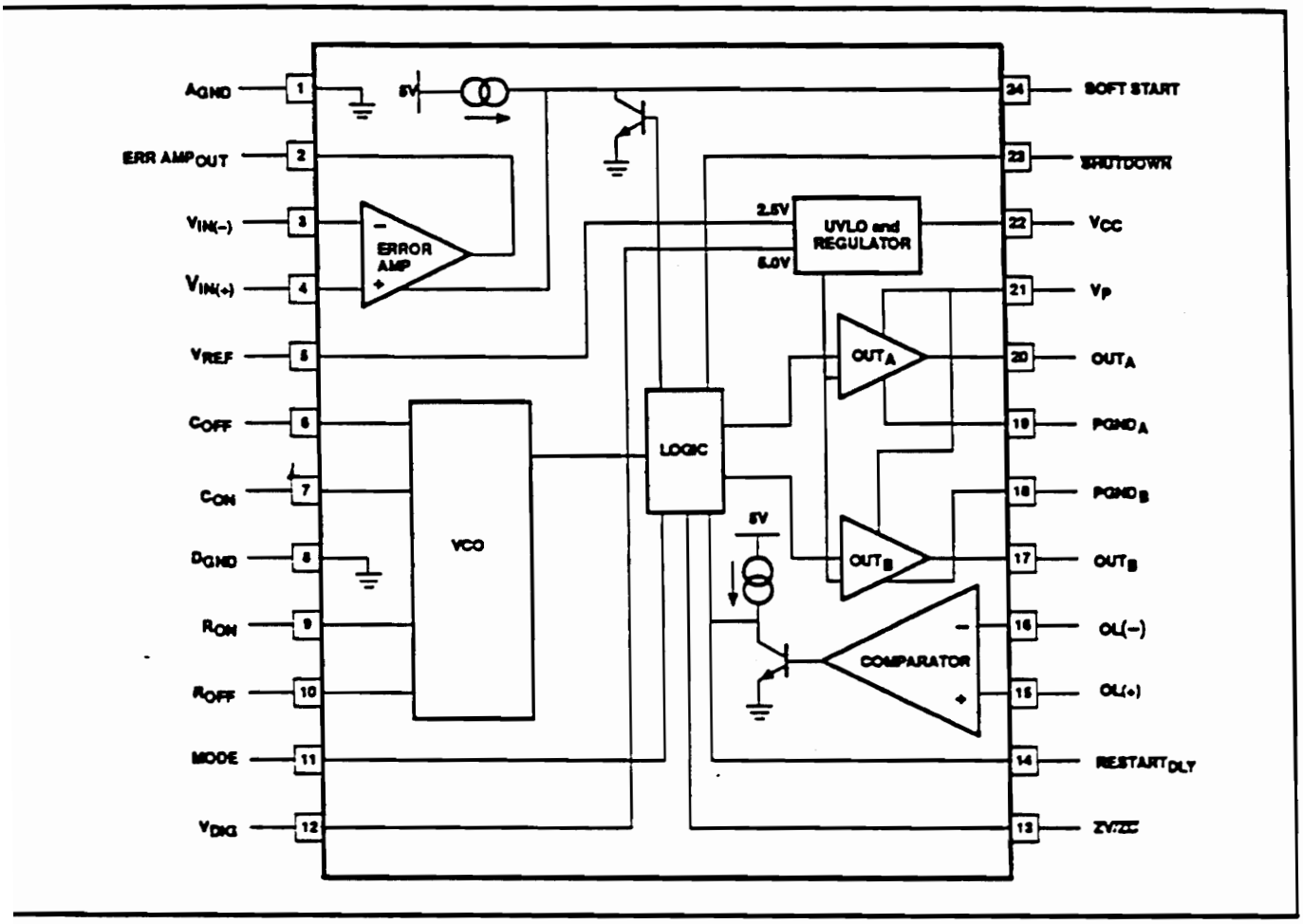


Figure 3.3. NE5580 Controller

b) Voltage Regulator and Reference

An internal voltage regulator provides a non-trimmed 5 V at the V_{DIG} pin and a measured 2.7 V bandgap reference at the V_{REF} pin. The 5 V regulator provides a bias voltage for the internal circuitry. The 2.7 V reference is used extensively as a voltage reference for the internal circuits. Both V_{DIG} and V_{REF} are disabled before the supply voltage to the controller reaches the upper threshold of 10 V. Once activated, these internal biasing voltages, V_{DIG} and V_{REF}, will be disabled again when the supply voltage drops below 8 V, thus providing undervoltage lockout.

c) Error Amplifier

The error amplifier in the chip compares the isolated feedback output voltage, connected to $V_{IN(-)}$, with the reference 2.7 V, connected to $V_{IN(+)}$, to generate an output voltage proportional to the error voltage between these two terminals. The output of the error amplifier is clamped at 4.7 V by an external zener diode.

d) Soft Start

The soft start function is achieved through an internal 10 μA current source and a 0.1 μF capacitor connected between the SOFT START pin and ground. This current charges the capacitor during start-up, gradually increasing the error amplifier output voltage to control the VCO frequency until the control loop takes over. The relatively large SOFT START capacitor ensures no overshoot even if a relatively long delay until full regulation takes over occurs. This has the advantage of added protection to the chip, especially if started up at light load.

e) Restart Delay

A 0.1 μF capacitor is placed across the $RESTART_{DLY}$ pin and ground. An internal 10 μA current source charges up this capacitor from 1 V to 2.5 V. This causes a "hiccup" delay when a fault occurs. This delay has the advantage of intermittently shutting down the controller, hence reducing the risk of damage through continuous operation in the event of a fault.

f) Overcurrent Protection

Overcurrent protection on this converter was achieved by limiting the maximum on-time. This is done by placing a fixed resistor between the R_{ON} terminal and the output of the error amplifier. The maximum on-time limits the minimum switching frequency and hence the conversion ratio of the converter.

g) Overvoltage Protection

The controller also has an automatic overvoltage protection built into its VCO. When excessive voltage occurs at the error amplifier output, internal digital circuitry within the VCO detects it and automatically disables the VCO.

3.4 Feedback Isolation

3.4.1 Preliminary Considerations

Feedback from the secondary of the converter must be isolated for two reasons: First, the chip is biased from the primary, and second, the minimum input voltage is 45 V. Regulations mandate that transformer coupled converters with input voltages in excess of 42 V require isolation between the primary and secondary grounds.

Magnetic, capacitive, and optical are the three methods of isolation commonly used. Magnetic coupling is provided in the form of transformers, shown in Fig. 3.4a. The output voltage sensed is compared to a reference voltage in an error amplifier. The error output signal is then used to modulate a high-frequency carrier wave which is then transmitted across the isolation barrier through a coupling transformer. On the primary side, the transmitted signal is recovered by a peak detector which then averages the signal. The averaged error signal is then recompared with the reference voltage from the NE5580 for further processing. A number of factors were considered in the use of this method for isolation. The magnitude of the ripple voltage from the peak detector and its effects on closed-loop operation, the imposition of layout space by the size of the coupling transformer, the effects of the leakage inductance from the coupling transformer, the number of supporting components for the isolation system, and the complexity of configuration for proper operation. These would add to the complexity and parts count which is undesirable for high-density purposes.

Capacitive coupling is another means of isolation, shown in Fig. 3.4b. Similarly,

the output voltage is compared with the reference voltage from an error amplifier. This error signal is then amplitude modulated and sent across a pair of capacitors instead. On the primary side, the process repeats just as in magnetic coupling. The major setback of this technique compared to magnetic coupling is its extreme susceptibility to noise. One method of improving this setback is to modulate the amplitude with a carrier frequency of about ten times the switching frequency. As the minimum switching frequency of the converter was designed at 2.7 MHz, and close proximity of the power and the control stages was required to achieve high density, this method was not used due to the large EMI within the package, in addition to the relatively large number of parts.

The last method for consideration was the use of an opto-coupler. An opto-coupler consists of a photo-diode that radiates energy proportional to the current flowing through it, and a photo-transistor that utilizes this radiated energy to cause a linearly-related collector current to flow. The collector current then flows through an external resistor to reproduce a voltage proportional to the sensed voltage. In terms of parts count, this technique is very desirable as the only external components are four resistors, one capacitor, and one precision voltage regulator. These additional supporting components can be placed under the opto-coupler. The legs of the opto-coupler are then clipped to accomodate the overall converter package. As the primary aim of the project is to maximize the circuit density of the control circuit, the opto-coupler was chosen as the isolation device between the primary and the secondary grounds.

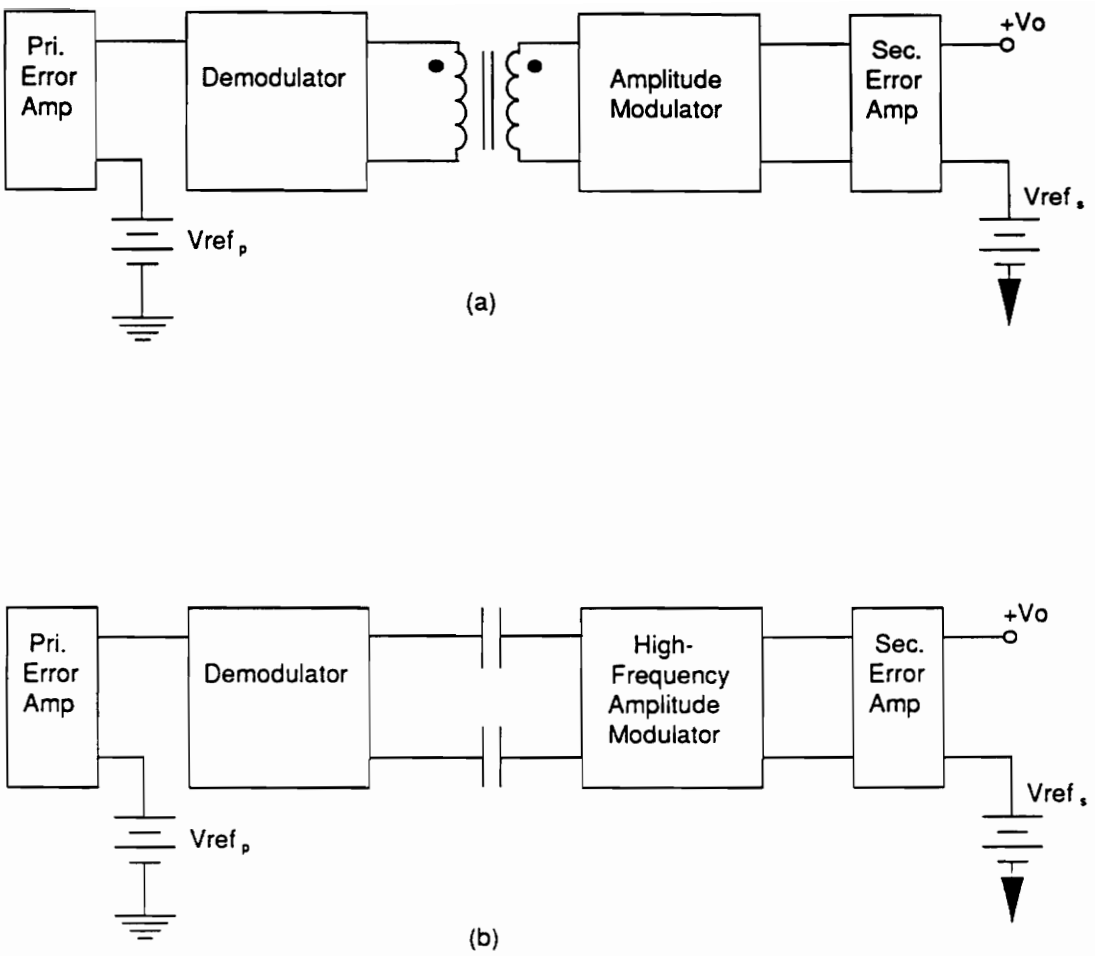


Figure 3.4. a) Magnetic Coupling and b) Capacitive Coupling

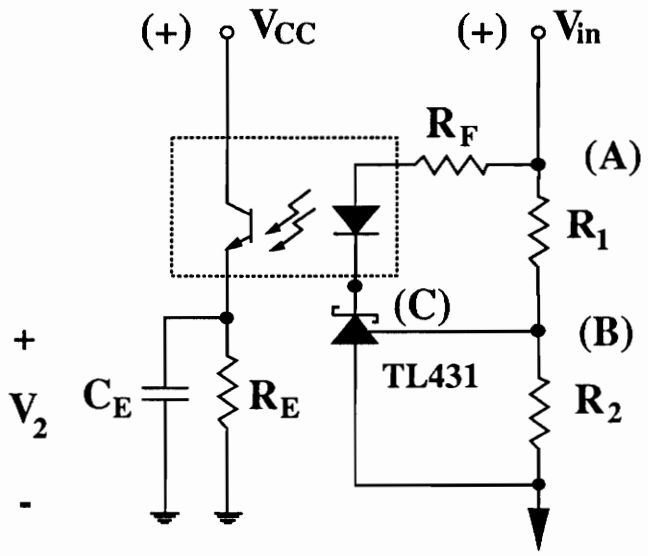


Figure 3.5. Opto-Isolation Circuit

3.4.2 Principle of Operation

Figure 3.5 shows the diagram of an opto-coupler configured to provide isolation for the NE5580 integrated controller. The voltage at the output of the converter is tied to point A. This voltage is divided by the resistor network at B to provide a regulated voltage at point C. The difference between the voltages at point A and point C will cause a forward current to flow across the forward resistor, R_F. The forward current causes the *pn* junction to emit photons. Within the enclosure, the radiated photons will strike the base of the photo-transistor across the isolation barrier. The photons striking the base-collector region will generate electron-hole pairs. The bias voltage, V_{CC}, of the opto-coupler creates an applied electric field which causes the electron-hole pairs to move, thus causing a current to flow. The collector current then flows across the resistor, R_E, and generates voltage, V_2. V_2 is linearly proportional to the sensed output voltage through design for operation of the opto-coupler in the linear region. C_E is placed in parallel with R_E to decouple noise picked up by the base of the photo-transistor.

3.4.3 Design

The opto-coupler selected was a 4N25 from Motorola. The forward voltage of this chip was rated at 1.2 V. From the dc current transfer ratio (CTR) for a V_{CC} of 10 V the linear range of these characteristics can be obtained with the forward current ranging from 1 to 10 mA. In the control circuit design, the VCC for the opto-coupler was also tied to the bias voltage for the NE5580 chip. This bias voltage is obtained from the start-up and self-bias sections of the circuit. As such, the bias voltage is not at precisely 10 V. Although the bias voltage can be clamped to 10 V by a zener diode, this extra component can be deleted by readjusting R_F to work with the unclamped bias voltage. Therefore, the forward current required to establish the dc operating point is no longer the same as obtained from the published CTR characteristics. The published characteristics served only as a guideline. The actual forward current range is estimated to be slightly higher since the bias voltage is 12.5 V. R_F was initially calculated assuming the bias voltage was clamped at 10 V, and reiterated until the desired linear range was obtained with the unclamped bias voltage. Assuming a forward current of 7 mA, with the TL431 providing a regulated 1.9 V, the forward voltage drop of the photo-diode rated at 1.5 V and the output voltage of the converter to be regulated at 5 V, the initial forward resistor needed is given by the equation:

$$R_F = \frac{Vin - V_{ref} - V_F}{I_F} = \frac{5 - 1.5 - 1.9}{7 \times 10^{-3}} = 225\Omega.$$

Running the converter under open-loop, and with the bias voltage to the opto-coupler supplied from the self-bias winding of the power transformer, the relationship between the output voltage at the power stage and the output voltage of the opto-coupler with RF = 185.1 Ω was recorded and plotted as shown in Fig. 3.6.

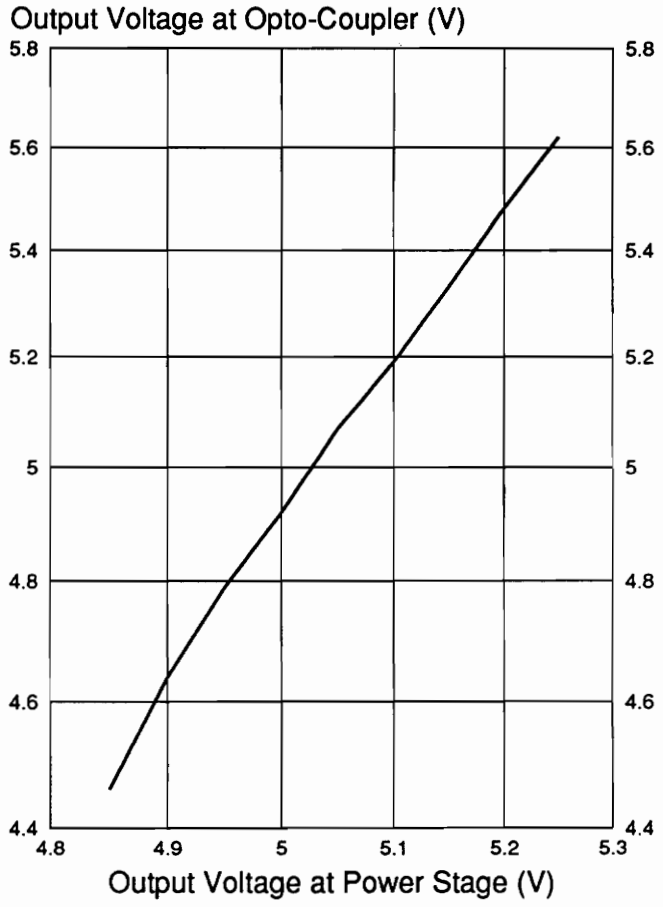


Figure 3.6. DC Characteristics of 4N25 Under Converter Operating Conditions

3.4.4 Advantages

The advantages of using the opto-coupler were the following:

1 low parts count,

2 simplicity, and

3 low cost.

The components needed to support the operation of the opto-coupler consists of an additional voltage regulator, four resistors, and one capacitor. In comparison with the isolation techniques using magnetic or capacitive coupling, where there is the additional amplitude modulator, demodulator, and a host of resistors and capacitors, the opto-coupler indeed offers the lowest parts count and is very appealing for hybridization.

The opto-coupler is simple to use as there is only the need to establish the dc operating point. This is done by simply interchanging the three resistor values. In the amplitude modulation technique, it is more complicated as the leakage of the coupling transformers have to be accounted for, the carrier frequency has to be selected and designed for, and the demodulator has to be designed for.

The opto-coupler isolation system is low in cost because of primarily the low parts count, and its simplicity. This feature is extremely attractive in view of production economics.

3.4.5 Limitations

The limitations of using an opto-coupler are the following:

1 susceptibility to noise, and

2 limited bandwidth.

The opto-coupler is susceptible to noise from the base of the photo-transistor. Figure 3.7 shows such an effect from the noise picked up from the drain-to-source voltage of the power MOSFET. The lower waveform belongs to the voltage across the emitter of the opto-coupler. This voltage is in phase with the drain-to-source voltage of the MOSFET. At a distance of about 2 inches from the MOSFET, the peak-to-peak voltage of this noise was almost 3 V. This noise has the undesirable effect of rendering the control unstable. To decouple the noise appearing at the output of the opto-coupler, capacitors can be placed across either the base, the collector or both. The larger the capacitor used, the better the decoupling. Decoupling capacitors, however, have the undesirable effect of further reducing the phase margin. Figure 3.8 shows the control-to-output transfer functions of the converter without any decoupling capacitors in the opto-coupler circuit.

Figure 3.9 shows the waveform at the output of the opto-coupler when the 100 pF decoupling capacitor is added at the base. The noise voltage has a peak-to-peak value of 0.43 V and is in phase with the drain-to-source voltage of the MOSFET. Figure 3.10 shows the control-to-output transfer function of the converter with a 100 pF decoupling capacitor placed across the base of the opto-coupler. Placing the decoupling capacitor across the emitter of the opto-coupler gives a higher phase margin than if placed at the base. Fig. 3.11 shows the control-to-output transfer function of the

converter with the output taken at the emitter of the opto-coupler, when a 220 pF decoupling capacitor is placed at the emitter. The phase margin is higher than that of Fig. 3.10 even though the capacitor used is larger. The waveform of the noise pickup with the 220 pF decoupling capacitor across the emitter is similar to Figure 3.9.

The system phase margin incorporating an opto-coupler is low. This is because opto-couplers introduce an additional pole in the feedback loop. This pole will be shifted lower with an increase in temperature, age, and the addition of a decoupling capacitor in the opto-coupler. From Fig. 3.12, this pole is located at around 60 KHz (R_L = 750 Ω) for Motorola's 4N25 opto-coupler, which is also where the double pole of the power stage is. Hence there is a -60 dB/decade slope from 40 KHz, which is extremely difficult to compensate for high crossover frequency and stability with voltage mode control.

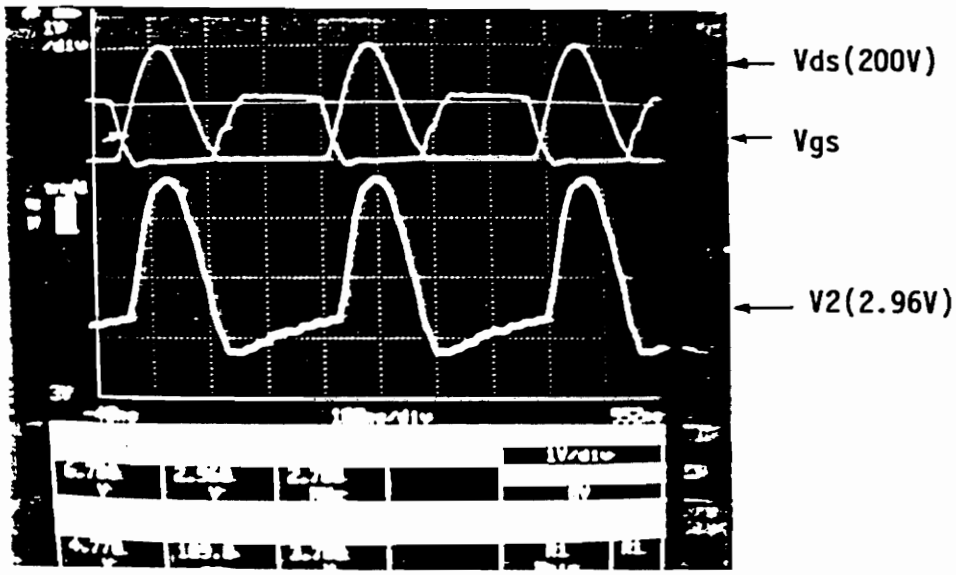
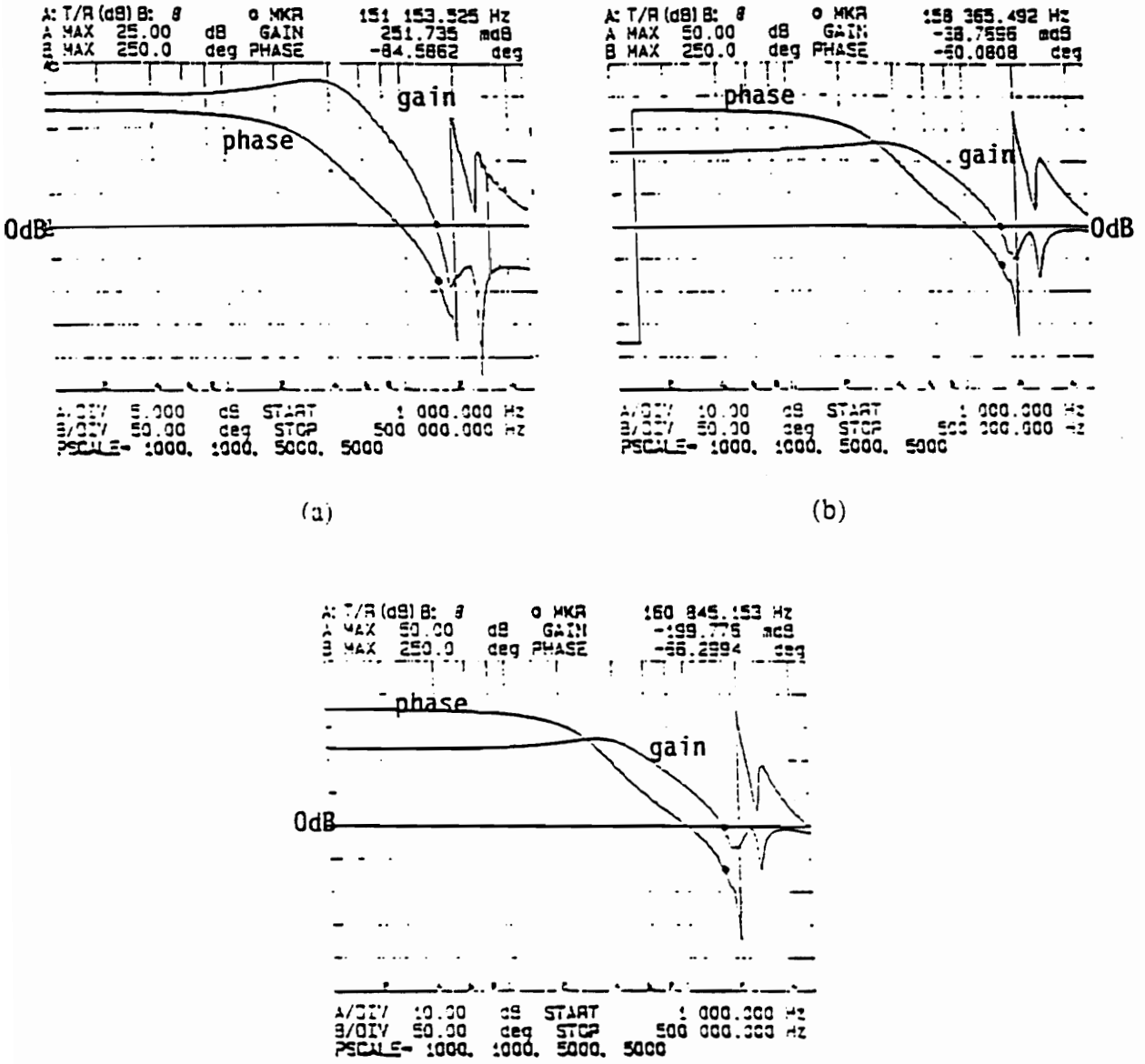


Figure 3.7. Noise Pickup at the Emitter of the Opto-Coupler Without a Decoupling Capacitor



(a) (b)

(c)

Figure 3.8. Open-Loop Control-to-Output Transfer Functions Without a Decoupling Capacitor in the Opto-Coupler:

(a) Low-Line and Full Load.
(b) Nominal Line and Full Load.
(c) High Line and Full Load

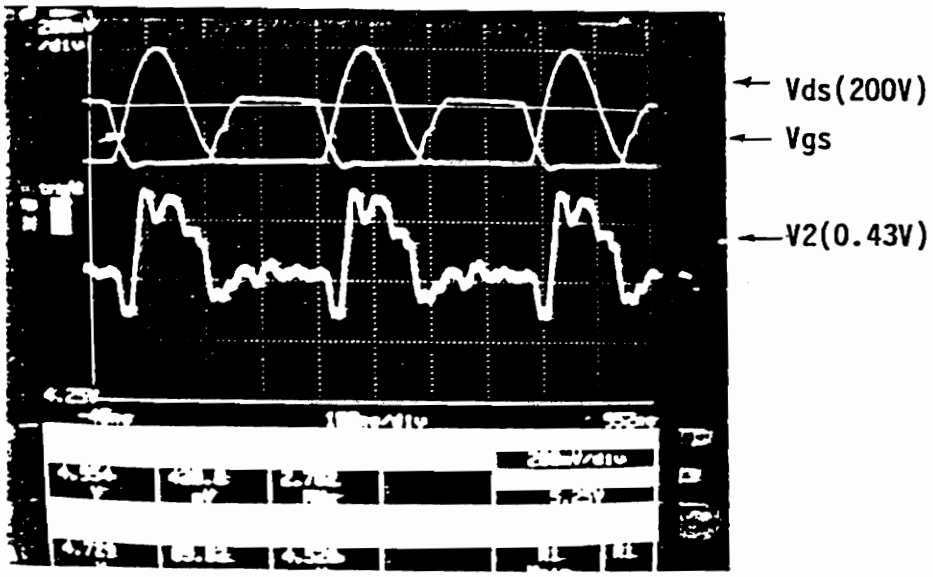


Figure 3.9. Noise Pick-up at the Emitter of the Opto-Coupler With a 100 pF Decoupling Capacitor Across the Base

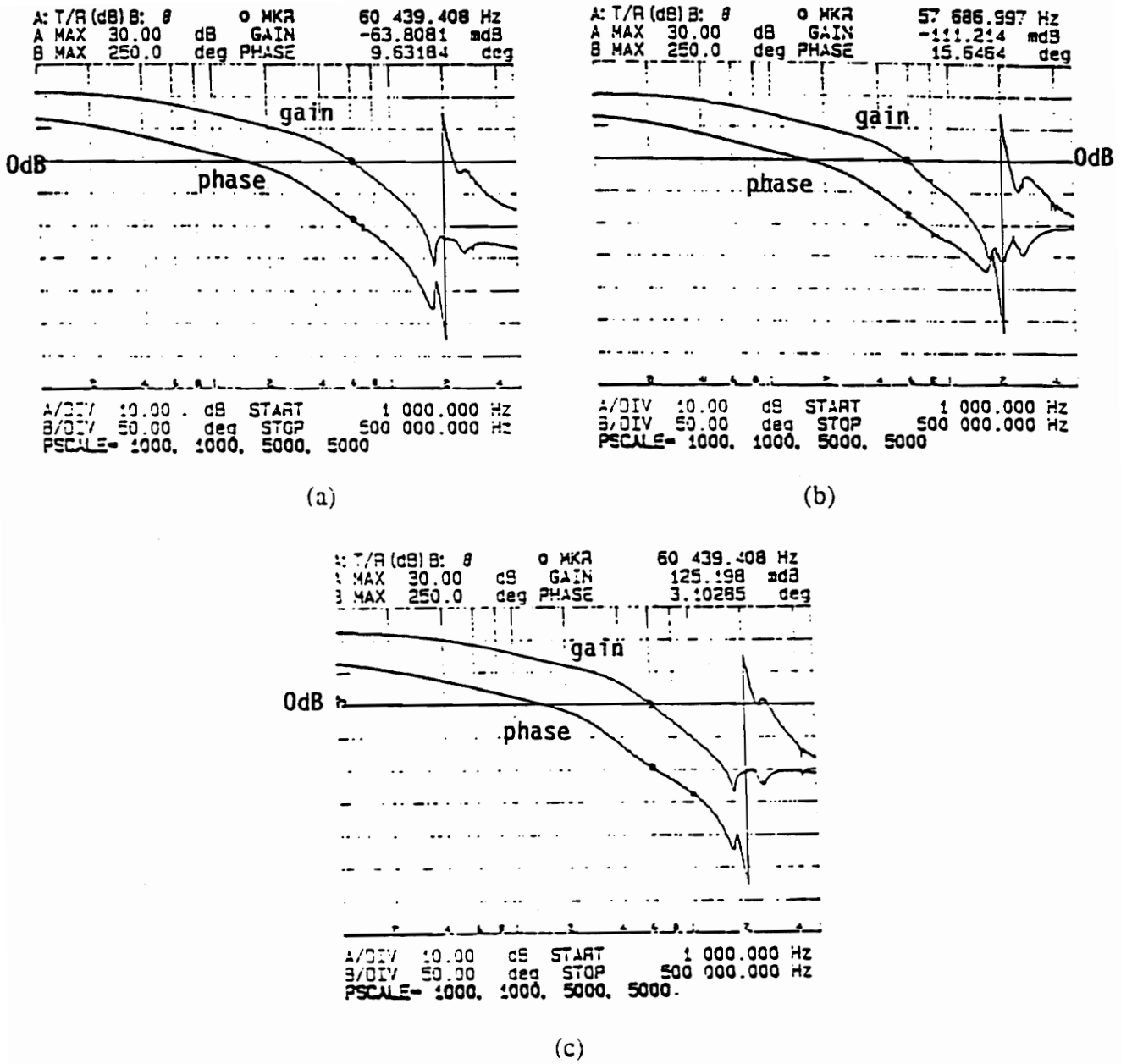


Figure 3.10. Open-Loop Control-to-Output Transfer Functions with a 100 pF Across the Base of the Opto-Coupler:

(a) Low-Line and Full Load,
(b) Nominal Line and Full Load,
(c) High-Line and Full Load

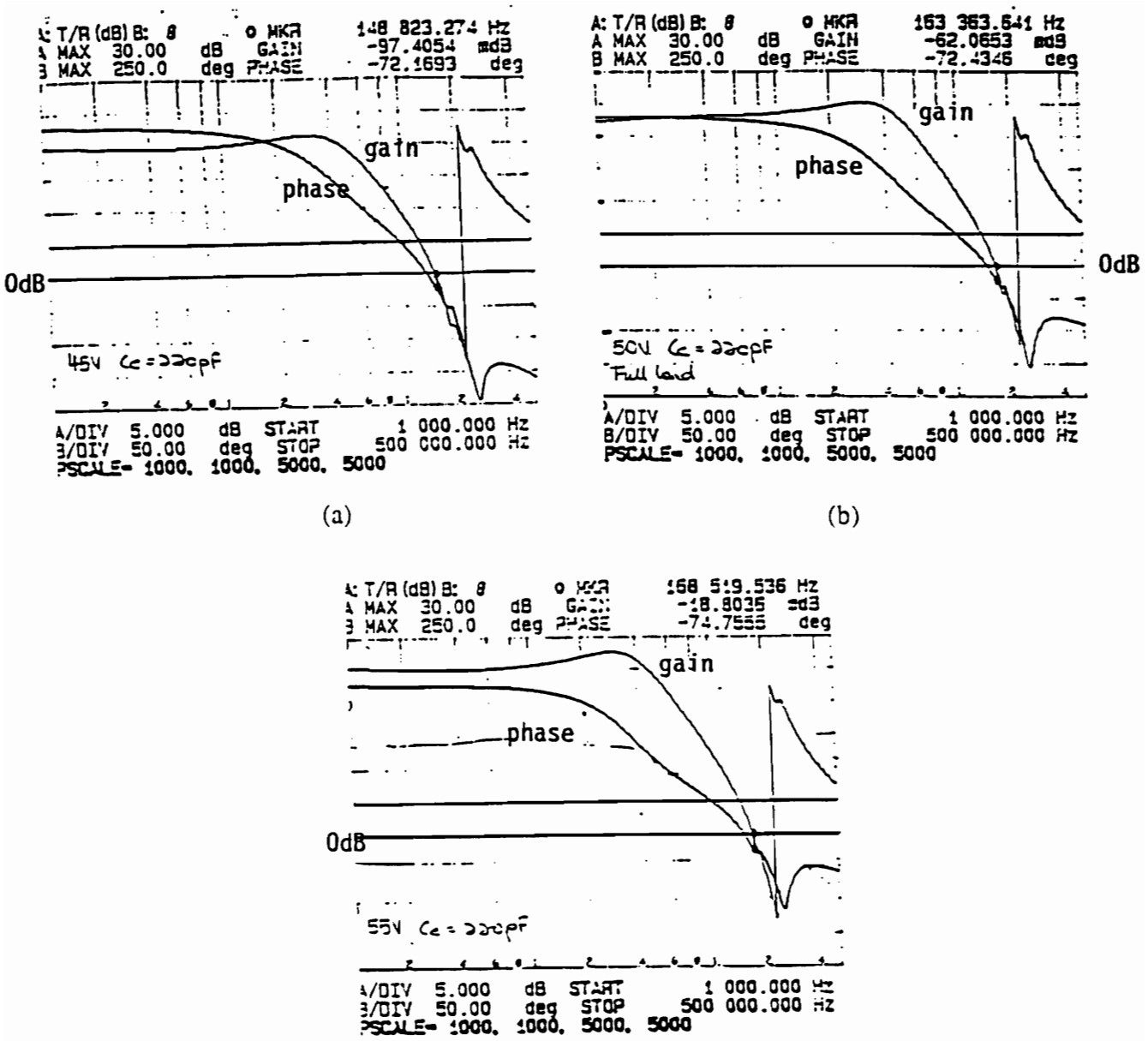


Figure 3.11. Open-Loop Control-to-Output Transfer Functions with a 220pF Across the Emitter of the Opto-Coupler.

(a) Low-Line and Full Load.
(b) Nominal Line and Full Load,
(c) High-Line and Full Load

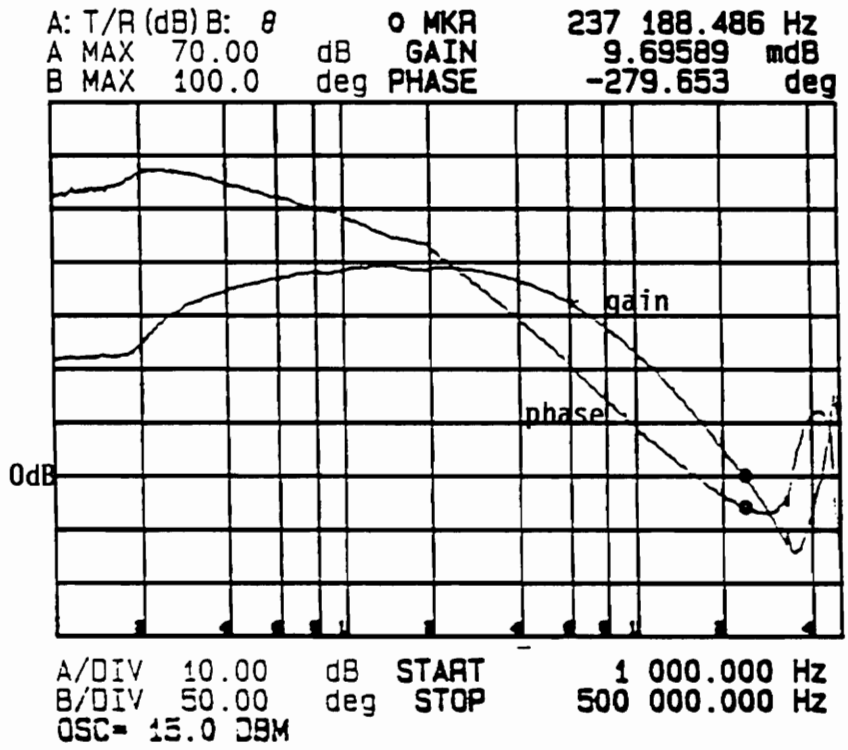


Figure 3.12. Output-to-Input Transfer Function of the Opto-Coupler Under Converter Operating Conditions

3.5 Control Loop Design

The open loop control-to-output transfer function of the power converter without the opto-coupler was obtained using the HP 4194A Impedance/Gain-Phase Analyzer. The control-to-output characteristics were obtained from low-line, light load to high-line, full load conditions. These characteristics are shown in Figs. 3.13 to 3.15. The transfer functions were measured from the output of the error amplifier to the output voltage of the power stage before the opto-coupler. Two prominent glitches are seen from these characteristics, but these two glitches are unknown as yet due to the inavailability of a generalized small-signal model for the ZVS-MRC to explain such occurrences. Since an opto-coupler was used in the feedback, it was natural to obtain plots of the control-to-output of the opto-coupler transfer function with the opto-coupler included to study the difference. These characteristics are shown in Fig. 3.16. These were measured from the output of the error amplifier to the output of the opto-coupler. From these plots, it is seen that the dc gain is higher than those taken without the opto-coupler. This is due to the amplification effect of the opto-coupler. The slope at the 0 dB line is much steeper, suggesting that the corner frequency of the opto-coupler is very low. It appeared that this corner frequency was around 40 KHz. This was also the output filter corner frequency of the power stage without the opto-coupler. Hence the phase delay from the opto-coupler caused almost a -60dB/decade slope from the corner frequency.

A variety of voltage-mode compensation schemes were devised to counter this problem. Using a three-pole, two zero compensation scheme, the crossover frequency of the control loop is high. However, the phase margin suffered due to the added phase delay from the opto-coupler. There were many iterations with different pole-zero placement.

Figure 3.17 shows the set-up for the loop-gain measurement to properly facilitate a low impedance at the reference node and high impedance for the test node. Figure 3.18 shows the loop gain of the converter using the following pole and zero placements, which were the best yet:

$$fz_1 = 22.7 \text{ KHz},$$

$$fz_2 = 38.0 \text{ KHz},$$

$$fp_2 = 970.5 \text{ KHz},$$

$$fp_3 = 1.05 \text{ MHz, and}$$

$$fc = 62.7 \text{ KHz}.$$

The phase margins of the loop gains at nominal and high lines, full load are above 45 degrees, and their crossover frequencies are above 70 KHz. However, at low line and full load, the phase margin of the loop gain was only 26 degrees, yet the crossover frequency was at 171 KHz. This imposes instability in the system. This could be seen to be true as the system at this condition was frequently unstable when attempts were made to measure its loop gain. The high crossover frequency measured was also unreliable and other pole-zero compensation schemes offered worse results. Clearly this was the cause from the opto-coupler pole. In the hybridized version, the noise effect will be made worse due to the closer proximity of the opto-coupler to the switch. More capacitance will be needed to decouple this noise, introducing even more phase delay in the feedback system. From the transfer functions where slopes in excess of -60dB/decade slope are experienced, it became evident that the use of voltage-mode control alone was not sufficient to stabilize the system with a high crossover frequency.

As the primary objective was to design a very high density control circuit, the tradeoff was to forego the complex compensation scheme and use a simple integrator

as the compensation instead. Through the use of an integrator, the crossover frequency was below 10 KHz; however, the dc gain was very high (70 dB). This high dc gain provided the converter with a very accurate dc output. In addition, the integrator only used a resistor and a capacitor as compared to the three-pole, two-zero scheme where a total of three resistors and two capacitors had to be used. Therefore the use of an integrator justified the criteria for high density.

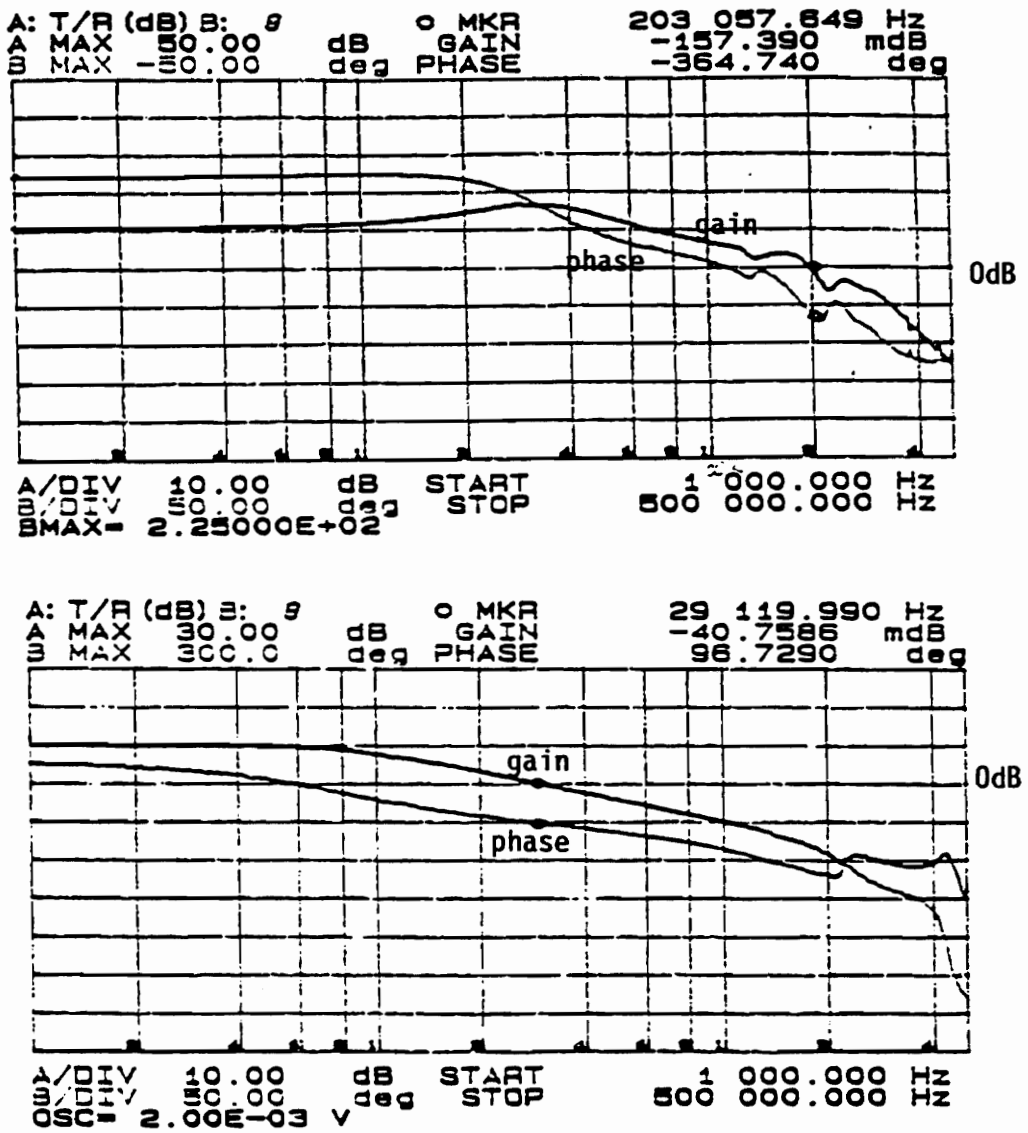
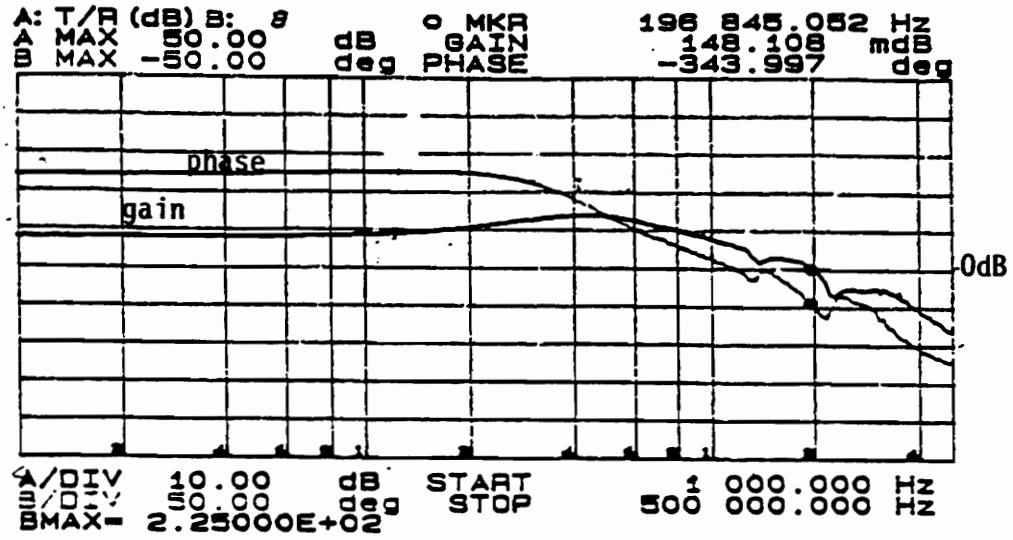


Figure 3.14. Open-Loop Control-to-Output Transfer Functions Without the Opto-Coupler:

Top Trace: Nominal Line and Full Load,
Bottom Trace: Nominal Line and 1A Load



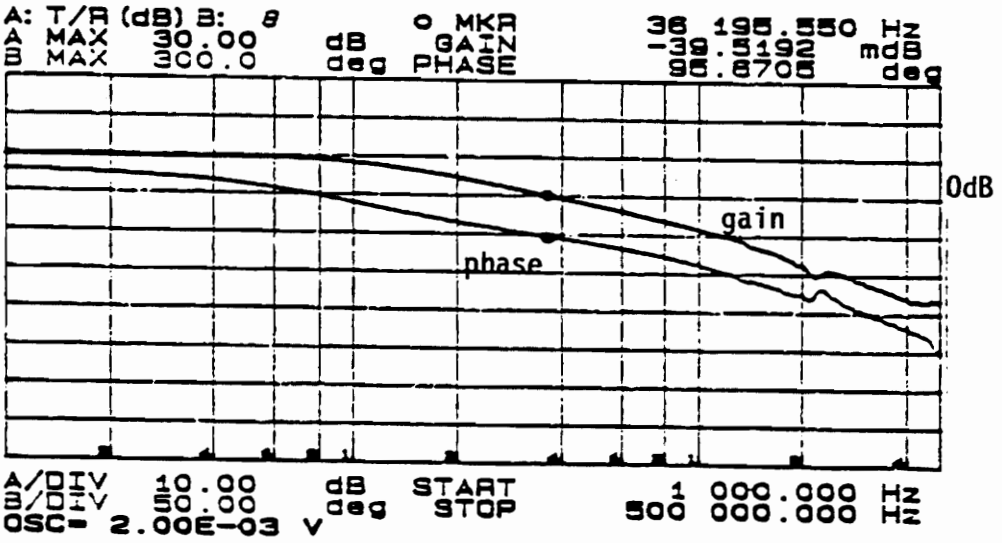
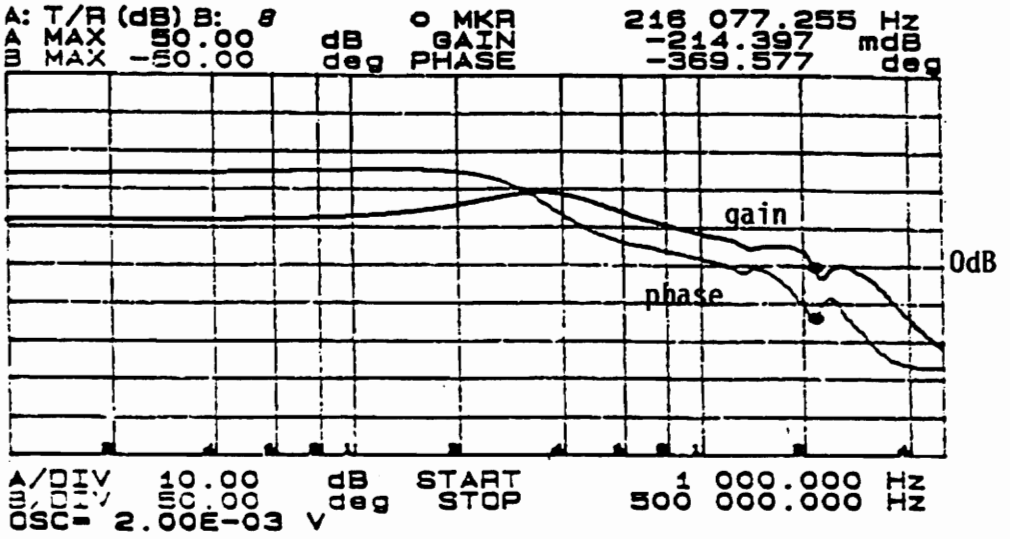


Figure 3.13. Open-Loop Control-to-Output Transfer Functions Without the Opto-Coupler:

Top Trace: Low-Line and Full Load,
Bottom Trace: Low-Line and 1A Load



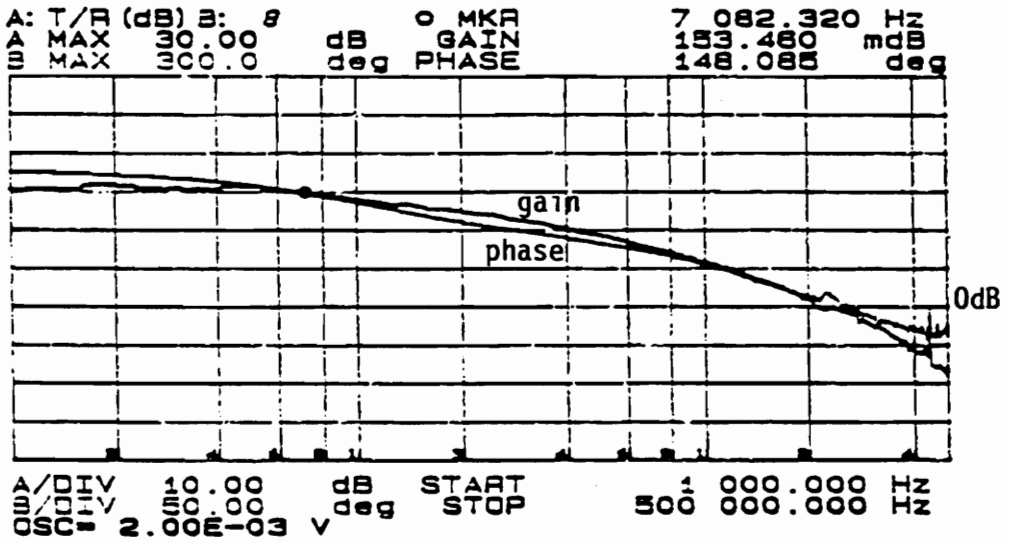
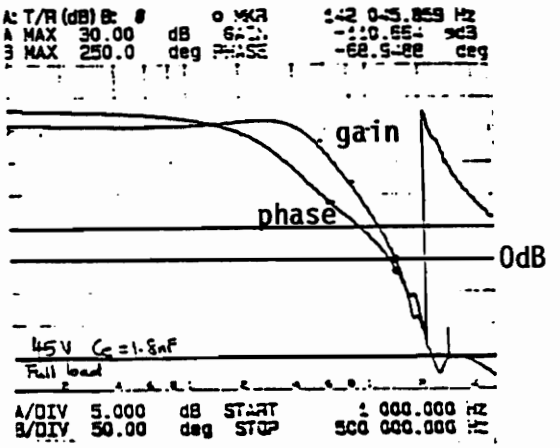
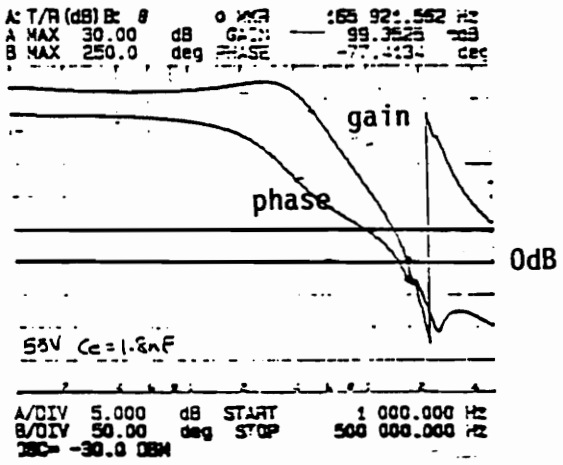


Figure 3.15. Open-Loop Control-to-Output Transfer Functions Without the Opto-Coupler:

Top Trace: High-Line and Full Load,
Bottom Trace: High-Line and 1A Load



(a)



(b)

Figure 3.16. Open-Loop Control-to-Output Transfer Function with the Opto-Coupler and C_E = 1.8 nF:

(a) Low-Line and Full Load.
(b) High-Line and Full Load

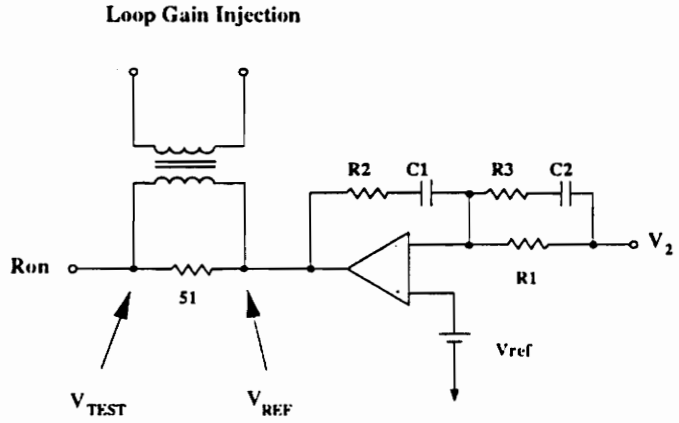
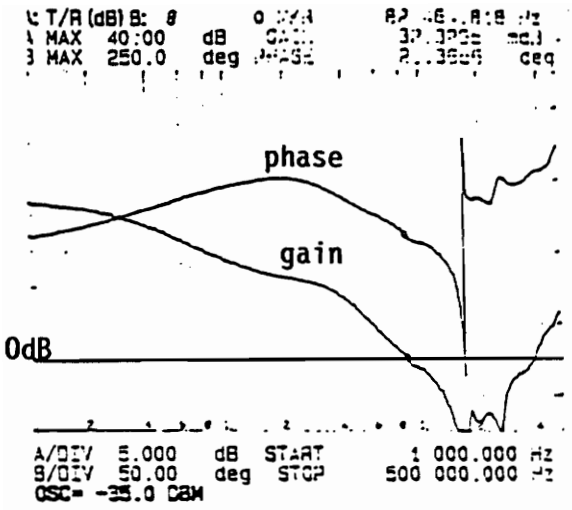
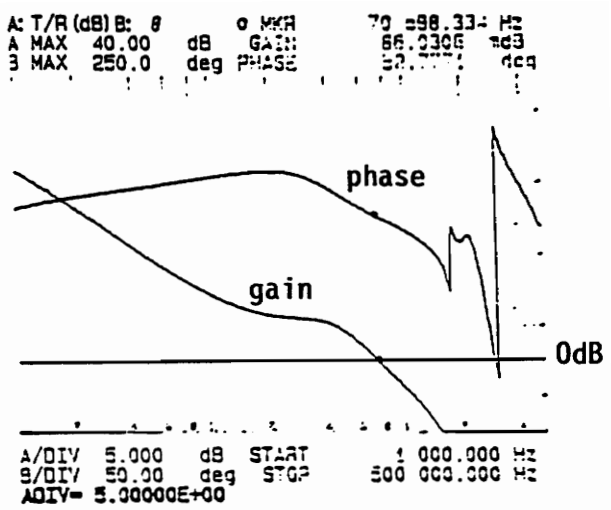


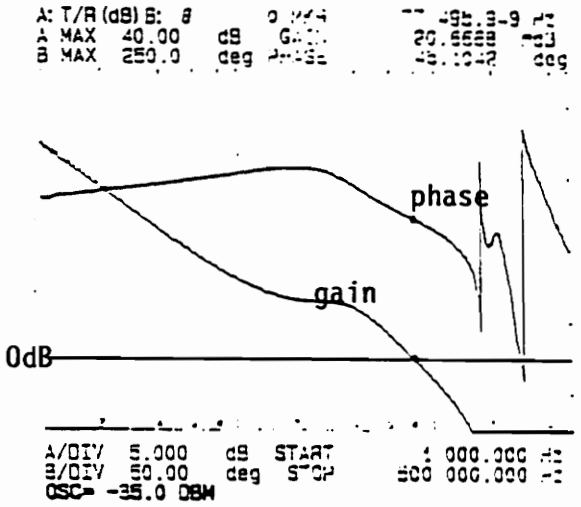
Figure 3.17. Set-Up for Loop-Gain Measurements



(a)



(b)



(c)

Figure 3.18. Loop-Gains of the Converter with C_E = 1.8 nF:

(a) Low-Line and Full Load,
(b) Nominal Line and Full Load,
(c) High-Line and Full Load

3.6 Start-Up and Self-Bias

To maintain the integrity of the converter, start-up and self-bias schemes were implemented.

Figure 3.19 shows the diagram for the start-up and self-bias circuitry. When Vin is applied at the input, MOSFET IRFC 210 acts as a linear voltage regulator. The gate-to-source voltage of this MOSFET is clamped to a maximum of 15 V by the zener diode. A large resistor, 47 KΩ, is placed to reduce the dissipation in the zener diode. A 0.1 μF charging capacitor stabilized the bias voltage. The start-up has to be shut down once normal operation of the converter is achieved. This is to prevent continuous power dissipation in the start-up circuitry. A low threshold voltage MOSFET, SVN 10K, was placed in parallel with the zener diode. When the converter is supplying the output voltage, the opto-coupler will produce an output proportional to this voltage only in the range from 4.7 V. When the output voltage from the opto-coupler reaches the threshold voltage of SVN 10K, this MOSFET turns on. The voltage across the zener diode is now shorted to ground. As this voltage is also the gate-to-source voltage of the linear voltage regulating MOSFET, this MOSFET is now turned off, and the start-up circuitry is disabled.

The self-bias circuit consists of a peak detector. This self-bias circuit is simple and possesses very low parts count. A voltage regulator exists internally in the controller so that an external voltage regulator as in the 50 W/in^3 design is made redundant.

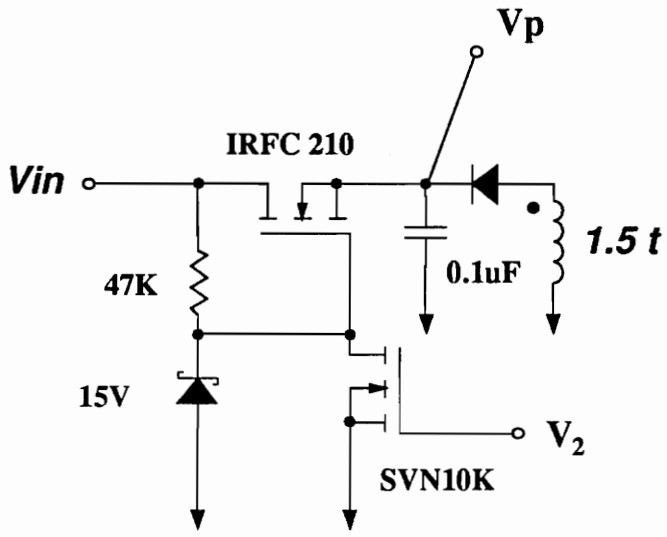


Figure 3.19. Start-Up and Self-Bias Circuitry

3.7 Hybridization

3.7.1 Layout

The controller NE5580 was obtained in its chip form. This was to achieve a small component size and also for heat dissipation by direct conduction through the substrate. All semiconductors and TL431 were also obtained and mounted in their die form for similar reasons. Even though resistors and capacitors can be printed directly onto the substrate by the use of thick-film hybrid techniques, this method was not used. This was because of the minor adjustments to be made by trimming upon assembly in order to fine tune the circuit. The slightly less area involved then would not justify the time and expense needed to ensure proper operation in a prototype.

The opto-coupler was obtained and used in its discrete Dual-in-Line package. Although it appeared cumbersome in a hybrid package, nevertheless the pheripheral components in support of the opto-coupler, for example the resistors, capacitor, and the voltage regulator TL431, can be positioned underneath the opto-coupler. The legs of the opto-coupler are then clipped to match the required height of the package.

Altogether there were three separate layers. The first layer consists primarily of the ground plane and routing of certain signal paths. This reduces the total number of layers for ease of fabrication and production economical. The substrate was 1.900 inches long by 0.470 inches wide and 0.025 inches high. The control circuit used less than 2/3 of the entire substrate. The other 1/3 was occupied by the output filter inductor alone.

As 1 mil gold bond wires were used for attachment, the design rules used were slightly different. Connection pads were made smaller and situated closer to the components. For the 1 mil gold wire connection, 15 mils by 15 mils pads were used and separated from the component by 20 mils. This was sufficient distance for the nozzle of the thermosonic wire bonder to clear the component and yet make strong bonds. For the 10 mil aluminum wire connection, the pads were 25 mils by 25 mils and separated by 25 mils. These pads have to clear of oxides to ensure successful adherence of the bonds. Vias for the 1 mil gold wire bonds were made about 10% larger than its bonding pads. This was to prevent too much loss of resolution from deposition and adherence of glass onto the ground layer, both of which have the effect of making the contact area potentially too small for successful bonding.

As the substrate pattern was only 1.900 inches long by 0.470 inches wide, it was very efficient to reproduce this pattern four times onto a 2 inch by 2 inch substrate. Upon printing and firing all three layers, each individual substrate pattern was scribed to size using a laser scribing system.

The 1 mil gold wire bonds could have been easily sheared if caution was not exercised during mounting of other components. As component placement was not done by automatic placement machines, the components were manually mounted with great care. Bonds have to be checked and rechecked to ensure no breakage or crossovers. The control circuit was portioned into the various sections, e.g., start-up, feedback isolation, etc. These various sections were individually checked and tested. Test leads were not soldered to conductors on the substrate to prevent conductor traces from lifting off the substrate as the test leads were often mechanically forced from connecting/disconnecting to probes. The probes were made to be in contact with the conductor

pads by firmly holding the probes with extreme care not to upset the bonds. Upon successful testing of each section of the control circuit, the entire control circuit was tested. Once the control circuit was tested successfully, the power stage was connected, and the entire package was tested before enclosure in an aluminum casing.

3.7.2 Resulting Power Density

The finished package is shown on the right of Fig. 3.20. The overall power density of the converter was calculated to be 83.33 W/in^3.

Several improvements can be made with this high density control circuit. To increase the crossover frequency of the control, another method of isolation has to be used. The research group at AT & T Bell Labs has recently published a paper describing a monolithic signal isolator with a unity-gain-bandwidth of 1 MHz [9]. It uses capacitive coupling with its own internal closed loop control to regulate the error to a minimum. The chip can be used to provide isolation without any auxiliary circuitry. This product is very attractive as the bandwidth is high in addition to the extremely low parts count. This chip, when used with the NE5580, will extract the maximum benefit from its 10 MHz error amplifier. When this product becomes commercial, it will be of great use in control circuits designed for high-frequency switched-mode power supplies requiring feedback isolation.

In terms of mass production and increased circuit density, printed resistors and capacitors can be used, and trimming will be automated once the prototypes are finalized. Use of low-temperature co-fireable ceramics (LTCC) will be very desirable for incorporation of printed resistors and capacitors in addition to providing more reliable and economical production of multi-layered circuits. Use of printed resistors and capacitors together with LTCC will push the overall power density of the existing design to a much higher level. It will be possible to increase the density of the current

control circuit to twice its present capacity. As wire bonding in industry is also traditionally an automated process, the entire control circuit can be mass produced, increasing reliability and reducing manufacturing costs.

3.8 Electrical Performance

The efficiency reached a maximum of 80.2% at full load and low line. The controller starts dc output voltage regulation at 44.2 V. At an input voltage of 33.6 V, the start-up circuit is disabled and the self-bias takes over to provide a Vp of 13.4 V to the control chip and Vcc of 10.25 V to the opto-coupler. The dc output voltage regulation was excellent. At loads of less than 7.8 A, the controller shut down due to insufficient current from the self-bias circuit to supply for the increased power consumption in the controller for driving at higher frequencies.

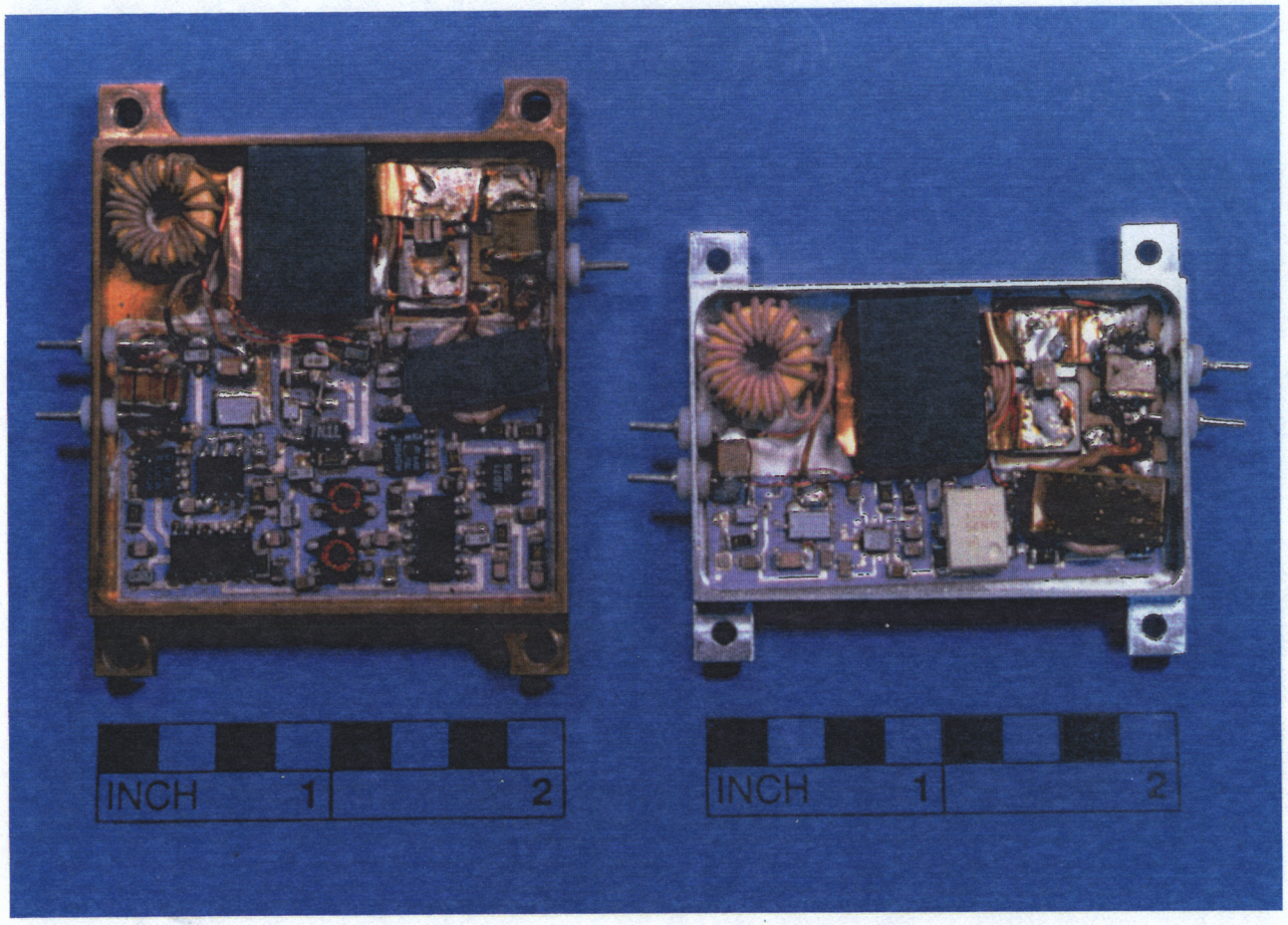


Figure 3.20. Comparison of the Physical Size Between the Two Versions.

Left: Previous 50 W/in^3 version,
Right: New 83.33 W/in^3 version

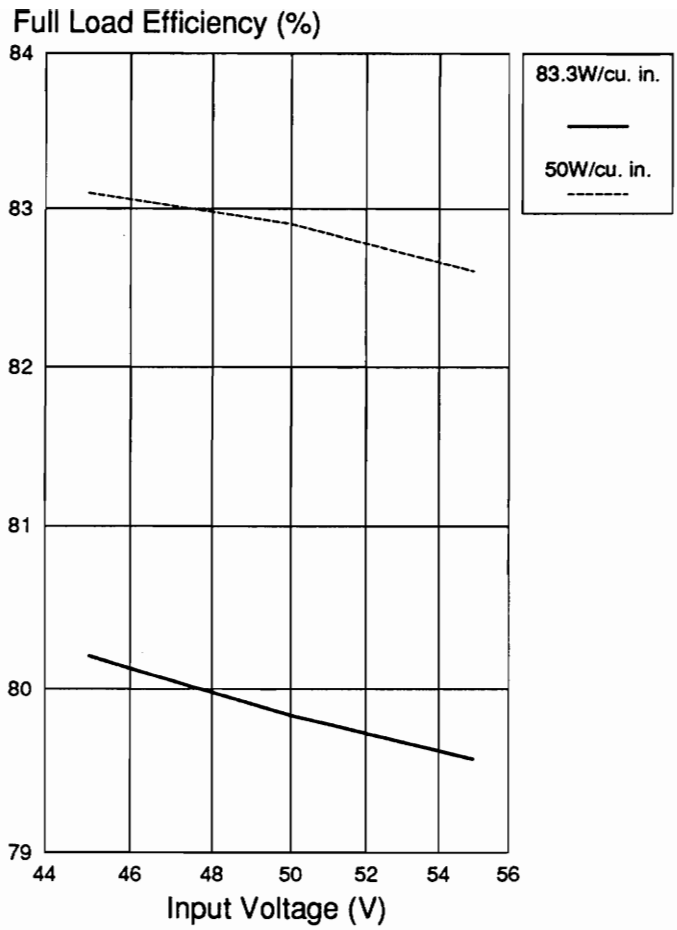


Figure 3.21. Comparison of Efficiency at Full Load Between the Previous Version and the New Version of the 50 W Forward ZVS-MRC

3.9 Summary

A new high-density control circuit for a 50 W forward ZVS-MRC had been designed and built with hybrid microelectronics techniques. This higher density control circuit was to replace a previously built control circuit of the forward converter, which had achieved an overall power density of 50 W/in^3. The new high-density control circuit has more protection features than its counterpart. These include soft start, overcurrent overvoltage protections, restart delay for the controller to go into a "hiccup" mode upon fault detection and undervoltage lockout. These features were inherent with the NE5580 control chip. With the new control circuit, much fewer components were used, which accounted for the much higher density of this circuit. The new control circuit boosts the previous overall power density of the converter by more than 65% to 83.33 W/in^3. The start-up and self-bias schemes of both converters were similar. The maximum efficiency of the 83.33W/in^3 converter was lower than the previous 50 W/in^3 converter by 2.9%. This comparison is illustrated in Fig. 3.21. The loss in efficiency was mainly due to the power dissipation in the control chip. The dynamic performance of the 50 W/in^3 was superior. This is because an opto-coupler was not used in its feedback isolation.

Figure 3.20 also shows the difference in size between the two converters. The new high-density control circuit is signficantly smaller than the previous version. In the previous version, a large space between the resonant inductor and the control substrate was left vacant. In the new version, this space was used to accomodate the input filter capacitors. Due to the very much reduced components, automation in production of the

new controller is very easily accomplished. In thick-film manufacturing facilities, wire-bonding of gold and aluminum wires are automated through use of computers, and component placement is done by automated pick-and-place machines.

4 LOW-PROFILE TRANSFORMER WINDINGS

4.1 Introduction

The converter in Chapter 3 was designed and successfully implemented as a low-profile, high-density module. The low-profile of this converter was determined mainly by the height of the power transformer.

The transformer in this converter operating at a minimum of 2.71 MHz exhibits relatively high copper losses compared to transformers in converters operating at frequencies in the KHz range. In this chapter, a commercial software package, which uses the finite element method to solve electromagnetic field equations, is used to analyze the copper losses in low-profile planar transformer windings. Two types of winding configurations are analyzed. One type is the existing round wire-copper foil winding configuration used in the 50 W forward ZVS-MRC transformer in Chapter 3. The other type is a proposed interleaved configuration. The effects of an interleaved versus the round wire-copper foil winding configuration in the forward converter are analyzed and discussed.

An interconnect scheme and a layout for interleaving windings is proposed and benefits are discussed. Finally, a fabrication scheme is suggested which takes advantage of fully automated facilities that mass-produce printed-circuit-boards.

4.2 Low-Profile Magnetics

The design of an efficient, small, and economical transformer is always a challenge, no matter what power supply topology is used. The size of switching converters cannot be reduced significantly by simply increasing the switching frequency. Magnetic components are the largest single components in any power converter.

Low-profile magnetics, in the form of planar transformers, are utilized for a variety of reasons. They would reduce the overall height of the converter to meet low-profile requirements, typically 0.25" for board-mount power supplies. Planar transformers, with their larger surface area-to-volume ratios than conventional magnetics, allow better heat removal by presenting a larger area for convection. The flat structure of the low-profile magnetics make it simple and natural to tie it to a heat sink, allowing further heat removal by conduction. Therefore core and copper losses can be quickly and efficiently dissipated.

Planar transformers evenly "squeeze" the magnetic field in the window. The magnetic field across the windings is more uniform. Fringing fields are restricted to small areas at the edges of the winding conductor. This will help to reduce the copper losses in the windings. The closer proximity of the windings to each other and the core will enhance magnetic coupling. This has the effect of reducing the leakage inductance and the ac winding resistance. Figure 4.1 shows the structures of an E-E core and an E-I core. Suppose both cores (of isotropic material) possess the same cross-sectional areas to provide the ac flux density for a given design. The mean magnetic path length, l_m, of the E-I core is relatively less. The magnetizing inductance is therefore effectively increased:

$$L_m = \frac{N_p^2 \mu_o \mu_r A_e}{l_m}, \tag{4.1}$$

where

$L_m \equiv$ primary magnetizing inductance, mH ,

$l_m \equiv$ mean magnetic path length, mm ,

$N_p \equiv$ primary turns ,

$A_e \equiv$ cross-sectional area of core, mm^2 , and

$\mu_o\mu_r \equiv$ permeability of core.

The increased magnetizing inductance will reduce the magnetizing current flowing through the windings, which in turn helps to reduce copper losses.

Although the advantages of using a low-profile transformer are numerous, there is one limitation, however, with respect to copper losses. From Fig. 4.2, the length of the winding needed to wrap around the middle leg of the core is increased. This effective increase in the winding length will increase the dc resistance of the copper winding. In turn, the overall winding resistance will be higher than that of a non-planar winding. Different winding configurations can be implemented to control this resistance. Interleaving and paralleling the primary and the secondary windings is one method of reducing the winding resistance.

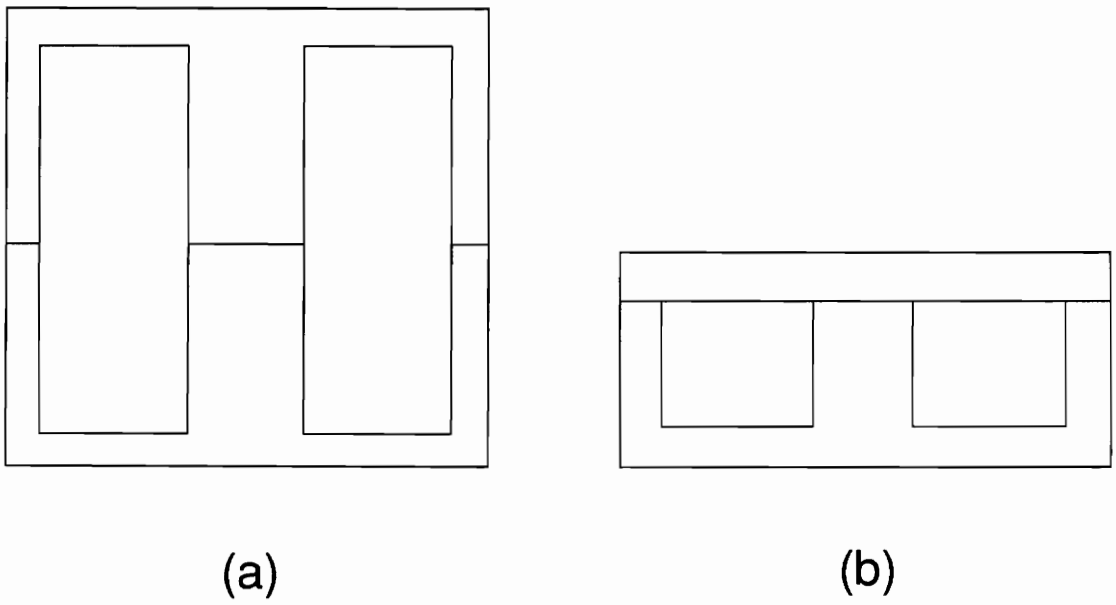


Figure 4.1. (a) E-E Core vs (b) E-I Core

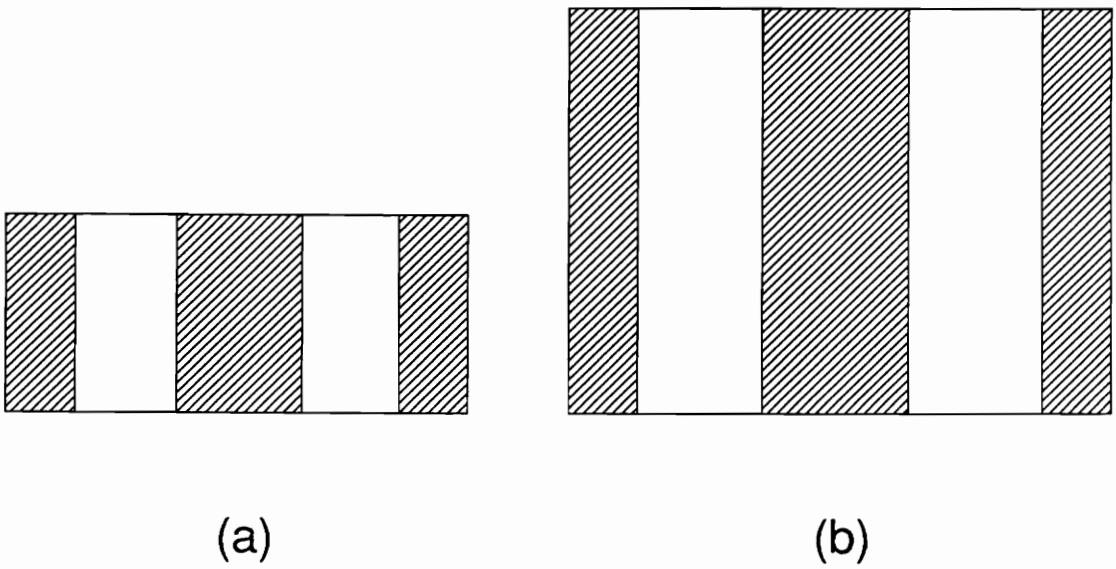


Figure 4.2. Cross-Section of Center Leg of (a) Conventional and (b) Low-Profile Transformer

4.3 Planar Windings

To accomodate planar magnetic structures, flat planar windings can be used. The use of copper foils is one example. By sandwiching these windings, tighter coupling can be achieved, leading to less leakage inductance. The window area is very efficiently utilized, and the magnetic field parallel to the windings is more uniform. Through a fabrication process to be discussed in Section 4.6, these windings are laminated under heat and pressure. This process enables fabrication to be automated, achieving repeatable short-circuit impedance, parameters very crucial to the design of high-frequency switching converters. By keeping the windings stacked together and closer to the core, the heat within the core, generated from copper losses, can be more efficiently dissipated by conduction from the windings, through the core, and into the heat sink. This will increase the reliability of the transformer. By selecting a low dielectric constant material as the insulation between layers, a relatively low interwinding capacitance can be achieved.

Planar winding structures have the capacity to be interleaved to reduce the ac winding resistance, and paralleled to reduce the dc winding resistance. In the next Section, 4.4, finite element analyses are performed to show the reduction of copper losses that can be achieved through interleaving. Paralleling the windings will increase the effective thickness of the windings. Since

$$R_{DC} = \frac{\rho l}{wt}, \tag{4.2}$$

where

$\rho \equiv$ resistivity of the winding conductor,

$l \equiv$ mean length of the winding,

$w \equiv$ width of the winding, and

$t \equiv$ thickness of the winding.

By simply increasing the thickness of the windings, the dc resistance of the windings can be reduced.

At higher switching frequencies, copper losses arise from skin and proximity effects. Figure 4.3 shows both skin effects and proximity effects of two planar strips of copper foil. The sourcing current through the left layer will generate a magnetic field around it. This magnetic field will induce opposing eddy currents within the left layer conductor itself. These eddy currents will oppose the main current in the middle of the conductor and enhance it near the surface. This is called the skin effect. The current density is non-uniform and is more concentrated at the surface than in the middle of the top layer. Eddy currents flowing along the right edge of the left layer conductor will in turn create a magnetic field between this conductor and the second layer conductor on the right. This magnetic field will then cause an eddy current opposite in direction to flow on the left edge of this second layer conductor. Eddy currents induced this way through linkage of a conductor with an alternating field generated by another conductor is called the proximity effect. Both these effects give rise to eddy currents which flow through very narrow regions near the surface of the conductor, thereby creating high ac resistance. The higher the frequency, the larger the eddy currents and the narrower the region of flow. A thick conductor will not be efficient for current flow at high frequencies as the current will only be confined to the narrow regions near the edges, on the order of the skin depth, while the inner portion is not utilized at all.

By interleaving the primary and the secondary, the peak magnetic fields between layers can be reduced, and subsequently, the eddy currents reduced. Reducing the conductor thickness to two times the skin depth will cause the eddy currents flowing on both edges to cancel. To increase the effective thickness of any one turn, different layers can be parallelled to make up that turn.

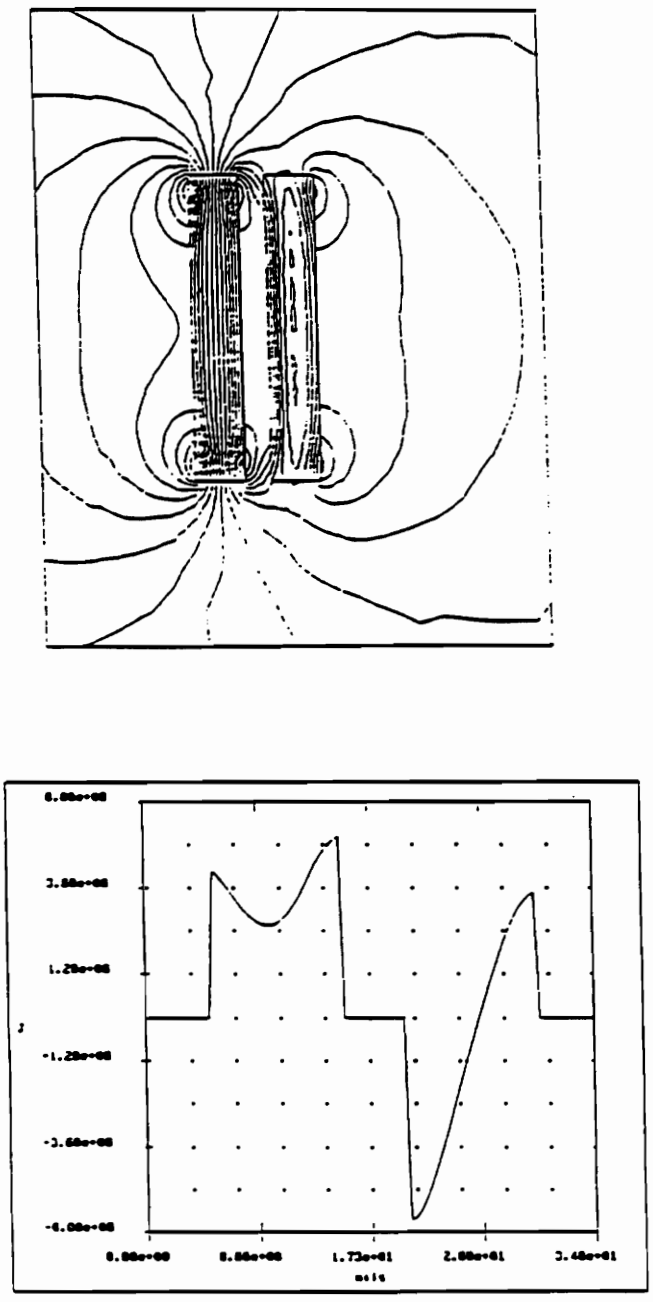


Figure 4.3. Skin Effect Versus Proximity Effect

4.4 Copper Loss Analysis Using Finite Element Analysis

The copper loss in transformer windings is caused by eddy currents circulating in narrow regions of the conductors. These currents arise from both the skin and proximity effects in the windings at high frequencies.

The calculation of eddy currents is done by solving for A and ϕ in the field equations [8]:

$$\nabla \times \frac{1}{\mu} \nabla \times \vec{\mathbf{A}} = (\sigma + j\omega\varepsilon)(-j\omega\vec{\mathbf{A}} - \nabla\phi), \tag{4.3a}$$

$$\int_S (\sigma + j\omega\varepsilon)(-j\omega\vec{\mathbf{A}} - \nabla\phi) dS = I, \tag{4.3b}$$

where

$\vec{\mathbf{A}}$ is the magnetic vector potential,

I is the current through S,

ϕ is the electric scalar potential,

μ is the magnetic permeability,

σ is conductivity,

ω is the angular frequency at which all quantities are oscillating, and

ε is the permittivity.

The right-hand side of Eq. (4.3) is the current density and the displacement current. For this analysis where the frequency used was 2.71 MHz, the displacement current term can be neglected as it is relatively minute compared to the current density term.

Upon solution of $\vec{\mathbf{A}}$, the expressions for $\vec{\mathbf{B}}, \vec{\mathbf{H}}, \vec{\mathbf{J}}$ and finally copper loss or P_{loss} are obtained in the following manner:

$$\vec{\mathbf{B}} = \nabla \times \vec{\mathbf{A}}, \tag{4.4}$$

$$\vec{\mathbf{H}} = \frac{1}{\mu}\vec{\mathbf{B}}, \tag{4.5}$$

$$\vec{\mathbf{J}} = \nabla \times \vec{\mathbf{H}} - \varepsilon\frac{\delta\vec{\mathbf{D}}}{\delta t} = (\sigma + j\omega\varepsilon)(-j\omega\vec{\mathbf{A}} - \nabla\phi), \tag{4.6}$$

and

$$P_{loss} = \frac{1}{2}\int_{vol}\frac{1}{\sigma}\vec{\mathbf{J}}\cdot\vec{\mathbf{J}}\,dv. \tag{4.7}$$

Equation (4.3) was solved for $\vec{\mathbf{A}}$ using numerical analysis methods. Finite element analysis is one such method which allows for solution to the electromagnetic field problem with respect to geometry and material. A finite element analysis program, Maxwell[R] from Ansoft Corporation [7], was used.

The geometry of the transformer and its windings are created with the *Meshmaker* module of this software. The program then breaks up the geometry of the problem into a mesh of triangles. The nodes or vertex and midpoint of each side of the triangle serve as the individual boundary conditions for the diffusion equation (4.3). Quadratic interpolation is used to determine the solution between nodes. A solver in cylindrical coordinates was used to treat the transformer as being axissymmetric, so that the problem can be reduced from three-dimensional to two-dimensional. The triangles are further refined to accomodate the problem to be solved for greater detail and accuracy. Around the edges of the conductors, the inner edges of the ferrite and the interfaces between the ferrite and the windings, the triangles are made smaller to accurately model for a refined

solution at these critical places. Around the edges of the conductor and the surfaces of the conductor facing the ferrite material, the size of each triangle is reduced to at least half of the skin depth. The skin depth of any medium is defined as:

$$\delta = \sqrt{\frac{2}{\omega\sigma\mu}}, \tag{4.8}$$

where

δ is the skin depth of the medium, m,

ω is the angular frequency of the penetrating field, rad/s,

σ is the conductivity of the medium, mhos/meter, and

μ is the permeability of the medium, H/m.

At 2.71 MHz, the skin depth of copper, using the above equation, is calculated to be 1.58 mils.

Figure 4.4 shows the geometry of a forward transformer with interleaved foil windings, with triangles imposed. Careful selection of strategic positions for mesh refinement is needed in order to limit the memory requirements of the computer and computing time. An IBM model 70 using an INTEL 80486 microprocessor with 8 MB of Random-Access-Memory (RAM) was used.

The solution of the diffusion equation is dependent upon the boundary conditions imposed, definition of material properties, and sources. The series connection of the primary turns are modelled by treating them as individual current sources providing the same current. The two secondary turns are modelled by serially connecting two sets of parallel conductors. Each set of parallel conductors are modelled by treating them as current sinks recieving identical current. The winding geometry is such that the separation between the primary and secondary is very small compared to its width. This will cause

the magnetic field to be uniform between the primary and the secondary. Since only the eddy currents are analyzed, the permeability of the ferrite is entered as a constant number, independent of variation with flux level.

The current densities, magnetic field strength, and the flux density distribution are phasor quatities with in-phase (0°) and out-of-phase (90°) components. The in-phase component are dominated by the external magnetic fields, and the eddy currents generated fields are at a minimum. The out-of-phase component is produced by the eddy currents while the external magnetic field is at a minimum. Therefore the phasor sum of these fields will give a complete representation of the fields caused by both the external and the induced (internal) sources.

In this analysis, the forward transformer was used. Both the round wire-copper foil and the interleaved planar winding structures are studied with respect to this transformer used in the forward ZVS-MRC. A turns ratio of 6:2 was used to closely relate these analyses to the converter from the previous chapter.

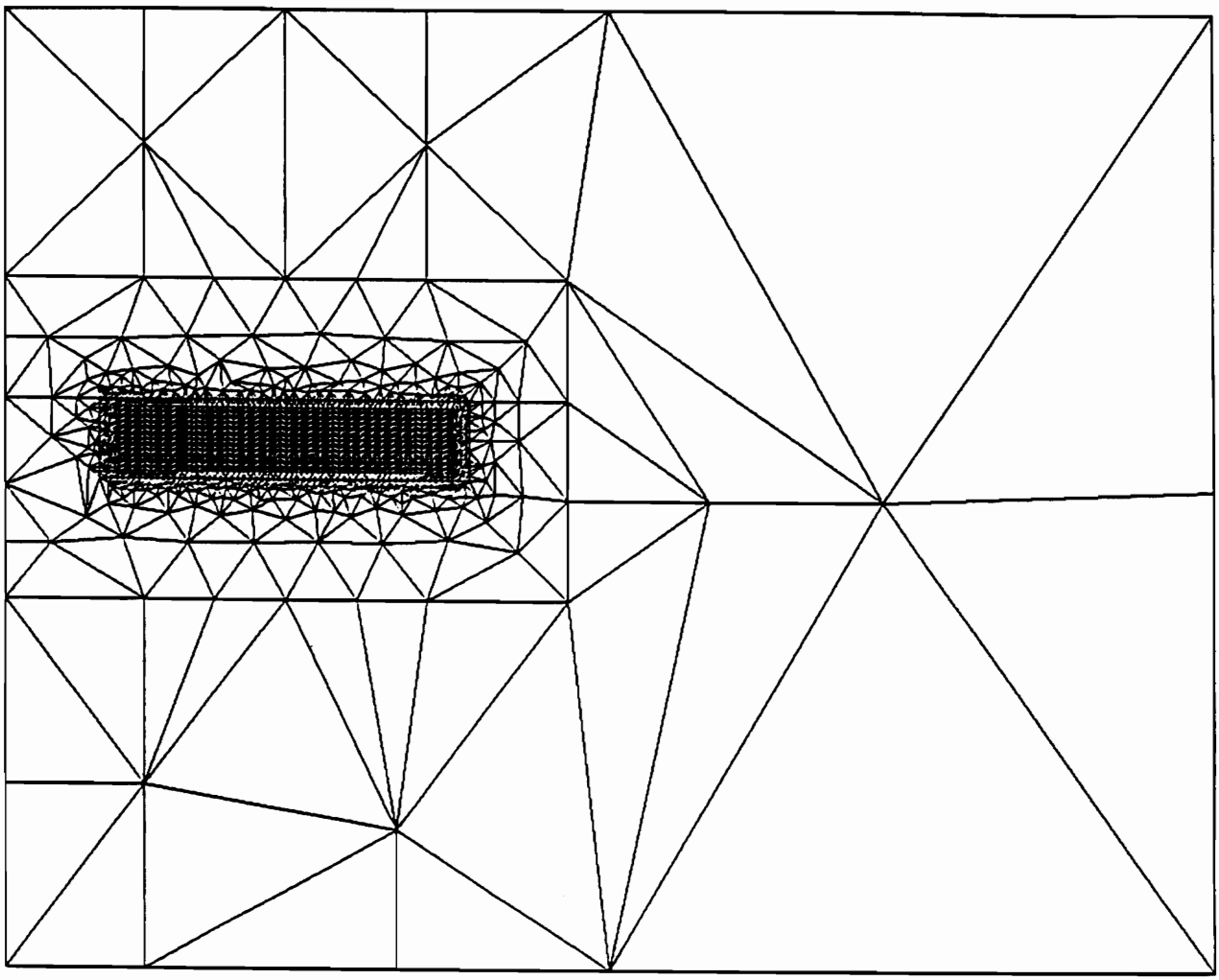


Figure 4.4. Forward Transformer

4.4.1 50 W ZVS-MRC Forward Transformer

The copper losses in the ungapped transformer, used in the forward converter similar to the one in Chapter 3, was studied. An ungapped transformer with core permeability of 125, similar to Ferramic's Q1 material, was used. The axissymmetric structure used in the analysis is different from the transformer used in the forward ZVS-MRC in Chapter 3, which was an E-I structure. The axissymmetric structure resembles a half of a pot-core and an I piece from the same material. The window has a height of 50 mils and a width of 230 mils.

Two types of winding configurations were analyzed. The first winding configuration resembles that used in the forward converter in chapter 3. This configuration consists of six primary turns of AWG #20 solid wire sandwiched between two secondary 5 mil thick and 210 mil wide copper foils. The second winding configuration was made up of twelve 1.3 mil thick and 210 mil wide copper foils stacked in a way that enabled interleaving. Each foil was separated by a distance of 1 mil.

The currents through each winding are obtained from the dc operating characteristics of the power stage used in Chapter 3. In this converter, there is a net magnetizing current of -0.36 A flowing through the transformer. Therefore 2.7 A is sourced through the primary winding, and 9.18 A is sunk from the secondary windings to result in a net magnetizing current of -0.36 A. The currents are assumed to be purely sinusoidal and oscillating at 2.71 MHz, the minimum switching of the forward converter in Chapter 3. The geometries for the interconnections and end pads were not incorporated, and hence copper losses that arise from fringing fields in the window resulting in eddy currents in the interconnects or end terminations were not analyzed.

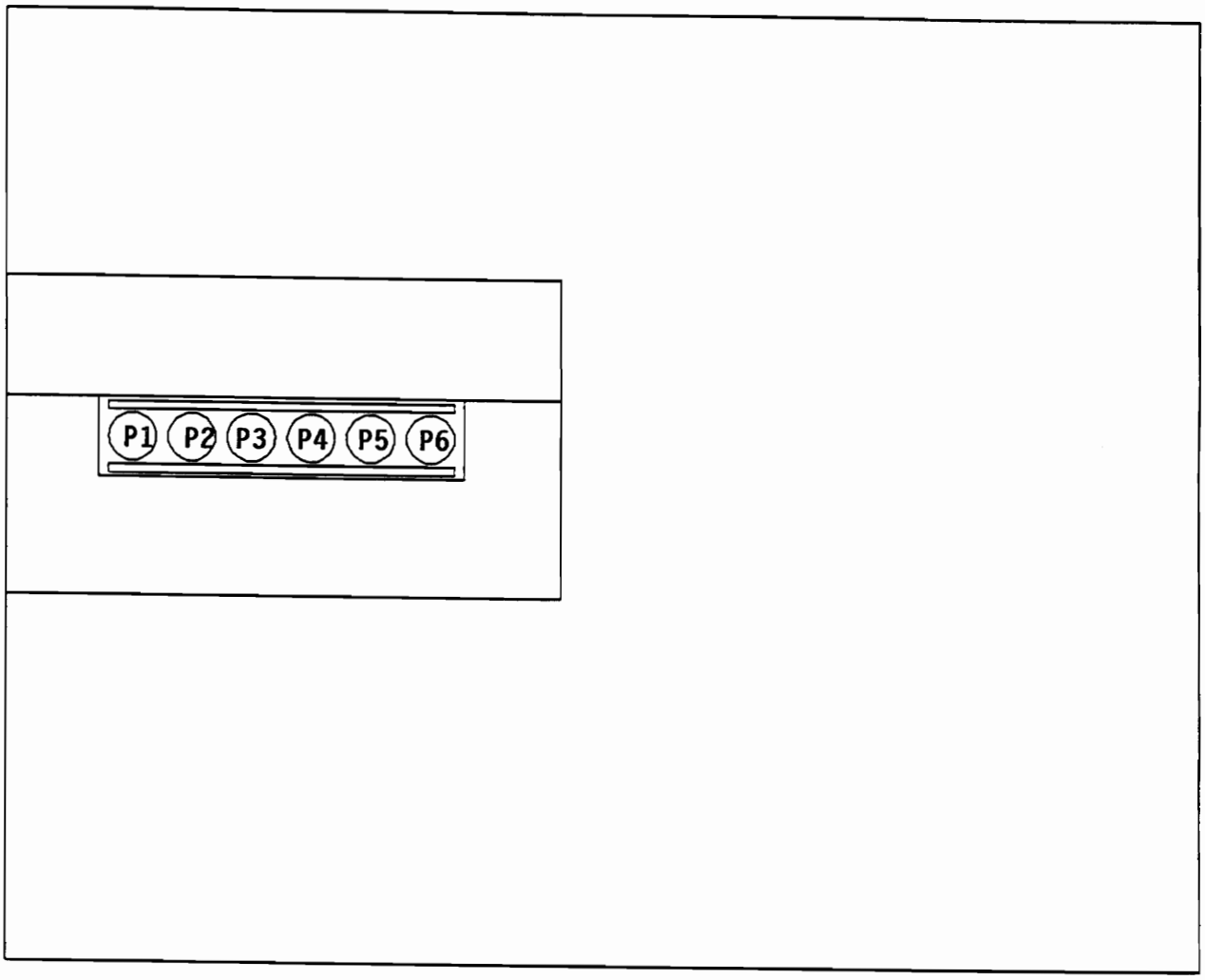


Figure 4.5. Round Wire-Copper Foil Wound Axissymmetric Transformer

4.4.1.1 Round Wire-Copper Foil Windings

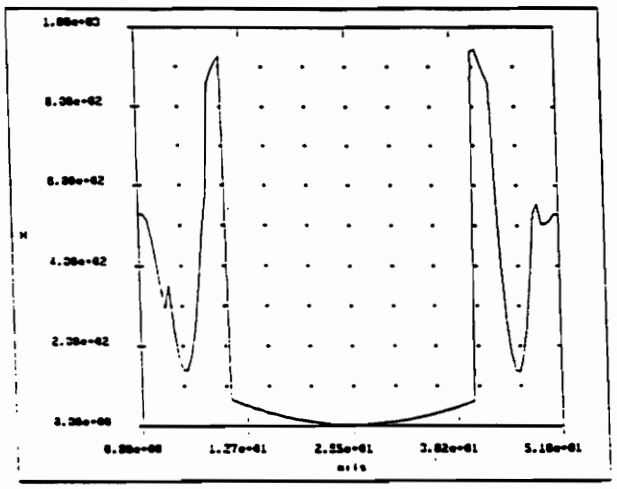
The winding configuration for the converter in Chapter 3 is shown in Fig. 4.5. The two secondary turns are made up of two copper foils indicated by *A* and *B*, respectively. The primary turns are made up of AWG #20 magnet wire sandwiched between the two copper foils and are indicated by *P1-P2-...-P6* to create a 2-section winding.

The magnetic field strength distribution profile is shown in Fig. 4.6(a). This profile was taken at 160 mils from the edge of the center leg for illustration purposes. The current density, J, is spatially related to the magnetic field strength, H, from Eq. (4.6). The location where the difference in magnetic field strength with respect to the spatial location is the greatest will induce the highest eddy currents. In relation to Figs. 4.6(a) to 4.6(b), it is seen that the interlayer gaps between the primary and the secondary windings have extremely high magnetic fields. Subsequently the conductors in the vicinity of these high fields have very high current densities. Consequently, eddy current losses in these conductors are the highest. The *highest* magnetic field strength in the *overall* winding structure was 2.105 X 10^4 A/m.

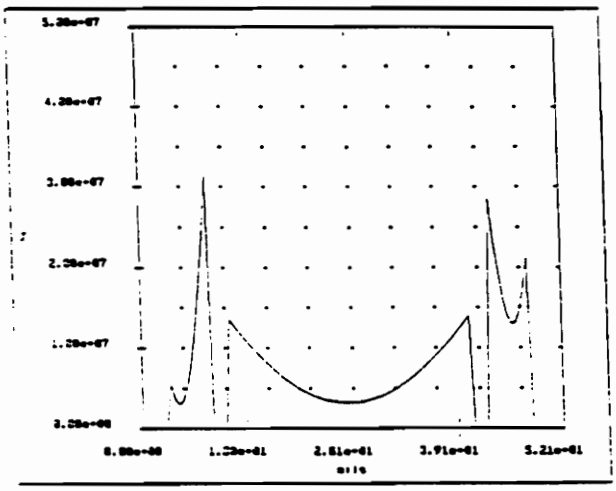
To illustrate the profile of the current distribution in the windings, the current density distribution, taken at 160 mils from the edge of the center leg, is shown in Fig. 4.6(b). The current density in the primary conductors keeps increasing toward the edges of the round wire cross-section, evidence of the skin effect. The edges of the secondary foils closest to the primary wires exhibit high current densities as a result of skin and proximity effects. The *highest* current density in the *overall* winding configuration was 7.25 X 10^8 A/m^2.

The flux distribution in the transformer structure is shown in Fig. 4.7. The flux is tangential near the interlayer gaps between the primary and the secondary. The fluxes also tend to be tangential to the surface of the round conductors. It can be seen from the edges of the copper foil that fluxes non-tangential to their widths will induce large eddy currents. All other flux lines are absorbed by the relatively low reluctance ferrite material.

The copper loss in the windings was computed from Eq. (4.2) and found to be 0.31 W. The copper loss calculated by Tabisz and Lee [2], for the transformer in the converter used in Chapter 3, was 0.53 W. The difference in the two calculated copper loss values stems from the assumptions used for the finite element analysis. The actual value included losses from the non-axissymmetric structure of the E-I core, the interconnections and end terminations, and the multiple harmonic content of the actual currents.



(a)



(b)

Figure 4.6. Distribution in Windings of Round Wire-Copper Foil Wound Forward Transformer:

(a) Magnitude of the Magnetic Field Strength,
(b) Magnitude of the Current Density

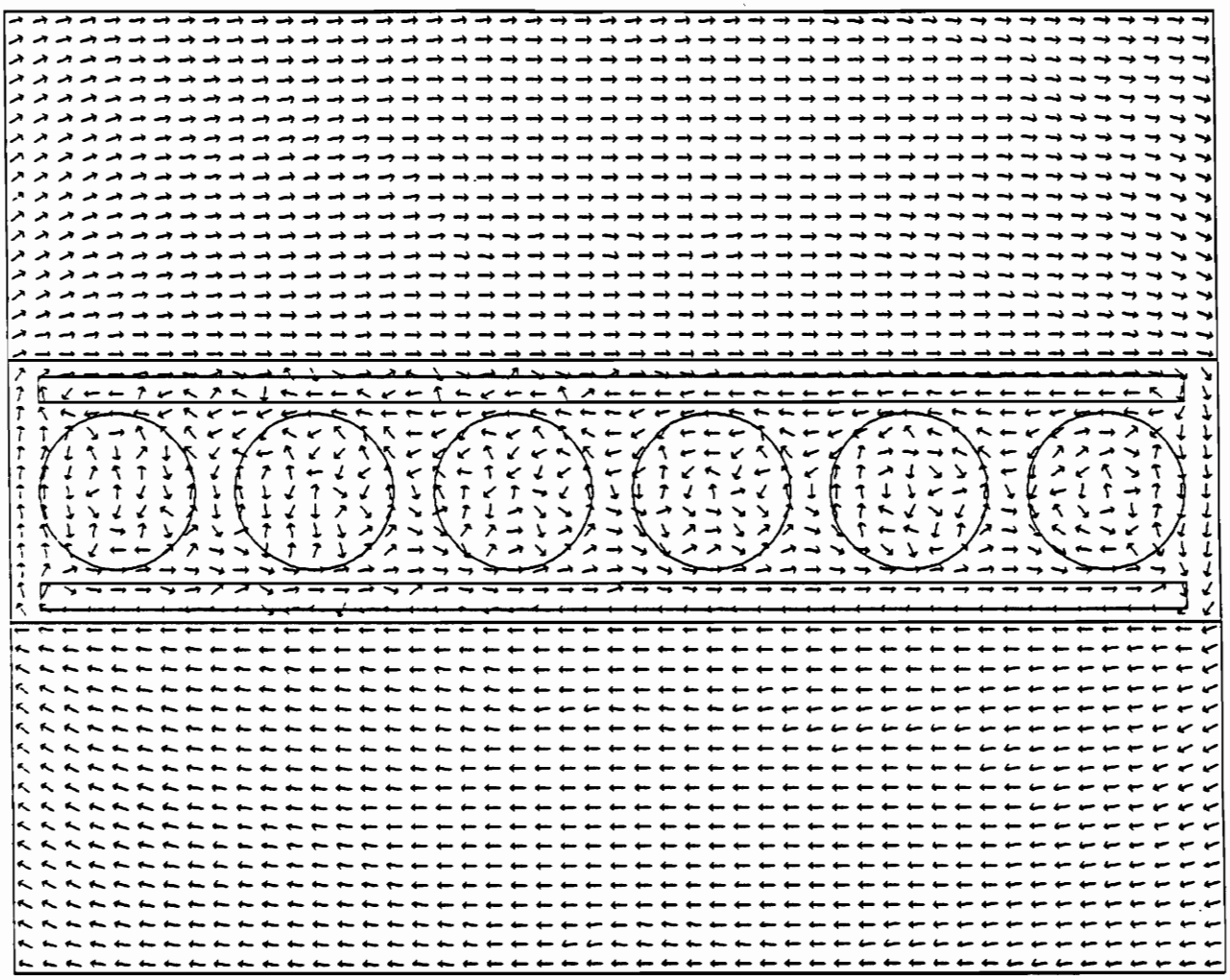


Figure 4.7. Flux Distribution ($\omega t = 0°$) in Round Wire-Copper Foil Wound Forward Transformer

4.4.1.2 Interleaved Windings

The winding configuration in this structure was *P1-A1-B1-P2-P3-A2-B2-P4-P5-A3-B3-P6*. The secondary windings are interleaved with the primary in this way for sectionalization into a 6-portion winding of two layers per portion. Each primary and secondary winding pair constitutes a portion. The greater the number of portions, the smaller the number of layers forming each portion. For example, in a non-interleaved winding configuration such as *P1-P2-P3-P4-P5-P6-A1-A2-A3-B1-B2-B3*, there is only one primary-secondary winding pair, which makes for only one portion. There are 12 layers that fill this portion. From Dowell's analysis [11], a smaller number of layers per portion will constitute a smaller ac resistance. This reduction in ac resistance stems from a greater number of portions which will effectively divide to reduce the magnetic field build-up.

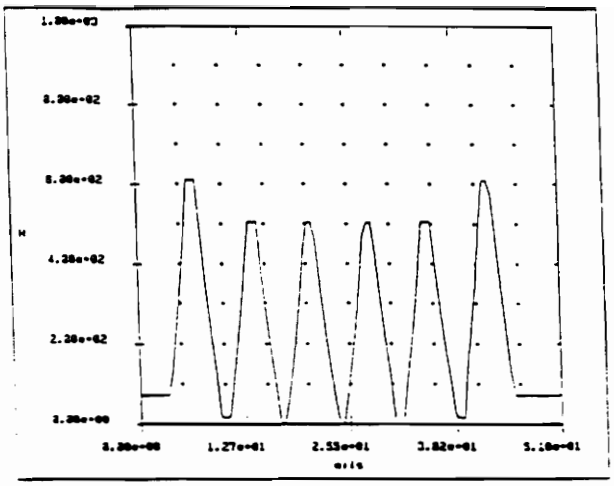
The magnetic field strength versus spatial distance profile is plotted as shown in Fig. 4.8(a). As in the previous winding configuration, the magnetic field strength distribution was plotted from a distance of 160 mils from the edge of the center leg. From this figure, the magnetic field strength is very evenly distributed. The magnetic field strength from *P1-A1* and *B3-P6* interlayer gaps exhibit elevated magnitude. This was due to the presence of magnetic field at the gaps between the ferrite and *P1* and *P6*, respectively. The *magnetic* field strength of 5.73×10^3 A/m for the *overall* winding structure is more than 3.5 times less than that in the previous round wire-copper foil combination. In this interleaved structure, the magnetic field arising from one primary turn is reduced by an opposing magnetic field from the immediately adjacent secondary turn whose current is flowing the other way. Therefore the overall

magnetic field is reduced in this process. This reduction in magnetic field subsequently produces less EMI to the rest of the converter circuit.

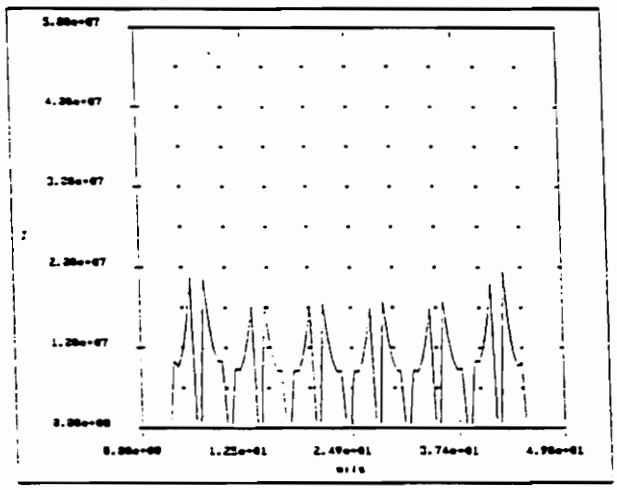
The total current density in the windings caused by both external and internal sources are shown in Fig. 4.8(b). Due to the reduced magnetic fields in the interlayer gaps, the eddy current contribution is also reduced, which explains the reduced overall current density in the windings. The current density is well distributed among all layers. The *highest* current density in the *overall* winding structure reached a maximum of about 1.12 X 10^8 A/m^2, which is more than 13 times less than the previous winding configuration. The much lower current density with the present winding configuration shows that the copper material is better utilized for current flow.

The flux distribution in the transformer structure is shown in Fig. 4.9. Apart from the fringing flux around the edges of the windings, the flux in all interlayer gaps is almost entirely tangential to the conductor surfaces. The relatively smaller magnitude magnetic fluxes will reduce the leakage inductance of this structure.

The copper loss in these interleaved windings was calculated to be 0.11 W. The copper loss of 0.31 W from the previous round wire-copper foil combination was about three times greater.



(a)



(b)

Figure 4.8. Distribution in Interleaved Windings of Forward Transformer:

(a) Magnitude of the Magnetic Field Strength,
(b) Magnitude of the Current Density

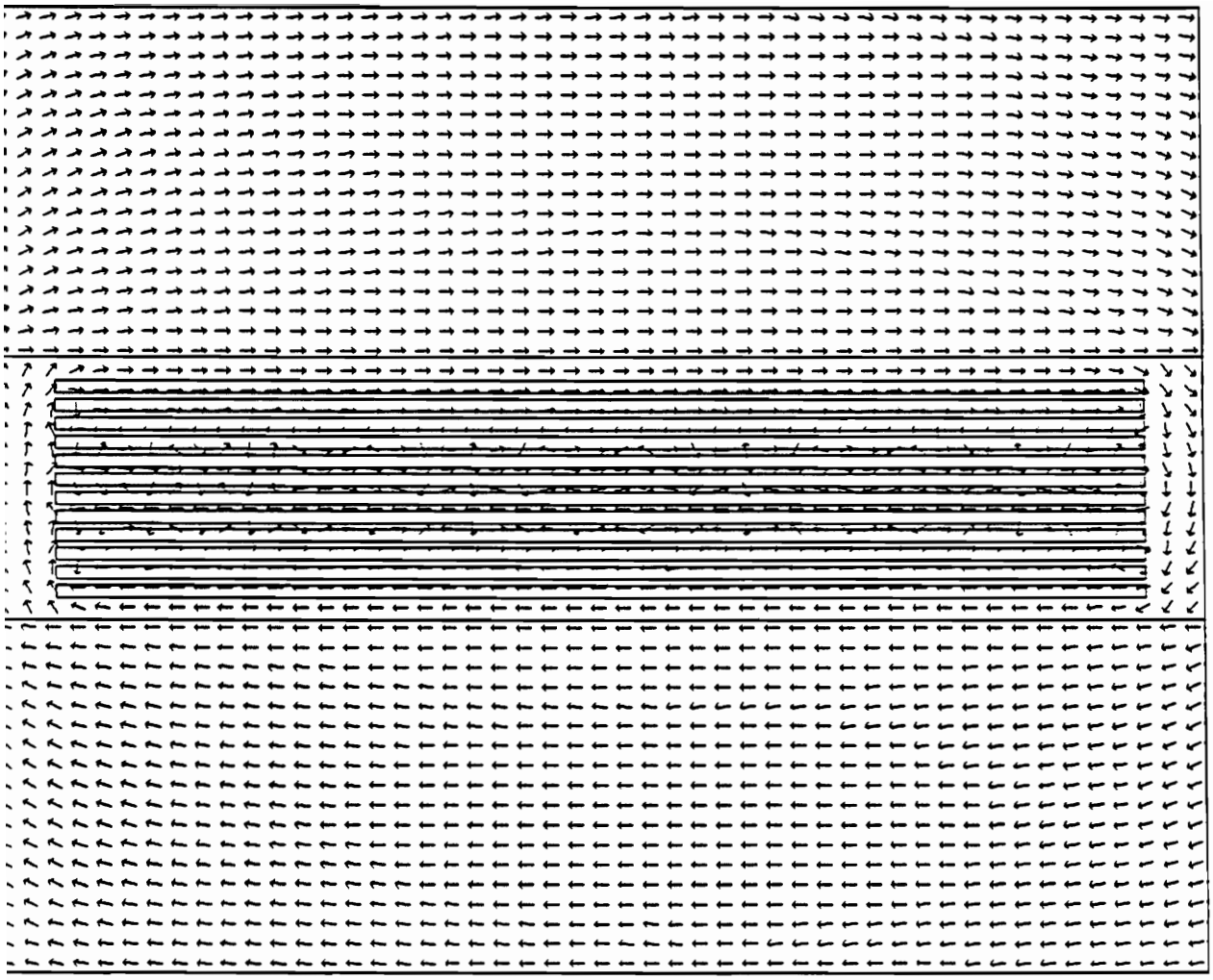


Figure 4.9. Flux Distribution ($\omega t = 0°$) of Interleaved Forward Transformer

4.5 Interconnection Method

To connect the different layers in series and/or parallel, an interconnection scheme must be devised. A buried interconnect adopted from Printed-Circuit-Board (PCB) fabrication technique is used. Figure 4.10 shows the interconnect scheme for interleaving the primary and secondary windings; in addition it is also suitable for paralleling different layers. In the interleaved winding structure, the first layer (primary/secondary) is connected in series to the third layer (primary/secondary) via an interconnect strip on the second layer (secondary/primary). Vias are opened to either connect them in series or parallel. This scheme provides flexibility in that serial and parallel connections can be done by simply repositioning the via locations. An additional flexibility in this scheme is that it allows different interleaving configurations to be realized by piecing together different combinations of skew symmetrically patterned layers. For example, if the configuration *P1-S1-P2-S1-P3-S2-P4-S2-P5-S1-P6-S2* is changed from configuration *P1-P2-S1-P3-P4-S2-P5-P6*, the required number windings are selected interconnecting through different via locations. Therefore, layers can be mass produced as they possess identical layout. Different layers can be pieced together to achieve different configurations much like building a sandwich.

This scheme has the additional advantage in that the number of layers is not limited to the window width but by the window height instead. With the more common method of constructing planar windings, shown in Fig. 4.11, the number of layers that can be interconnected are limited by the window width. As adequate lateral separation is needed to safely provide a through hole via from one layer to the next, it is obvious that this method is very restrictive when a small transformer requires many layers or winding turns.

In addition, the larger window width required will increase the length of any conducting layer, therefore increasing the dc resistance of the winding. With the present scheme for a window height of 50 mils, with a 1 ounce copper (1.3 mil) etched on a 1 mil polyamid and laminated together with 1 mil adhesive, a maximum of 15 layers can be accomodated in this window.

The top and bottom layers can be etched for pads to provide interconnecting pads to the "outside" world. This will enable electrically surface mounting of the entire transformer structure to the circuit. The converter is then deemed to be made up of entirely surface mountable components, including the transformer.

The interconnecting vias are to be plated as in the method used in PCBs. By plating the vias, conductor uniformity can be obtained. Hermeticity is also ensured. Since this is also an automated process, the entire transformer can be mass produced with repeatably low short-circuit impedances. From the low dielectric constant of the insulating Polyamid, a relatively low interwinding capacitance can also be achieved. As these parasitic reactances are very crucial in switching converters, the repeatability of these parasitic components will ensure greater reliability in final assembly and testing. The ability to surface mount the transformers will further add to the reliability and overall manufacturability of the converter.

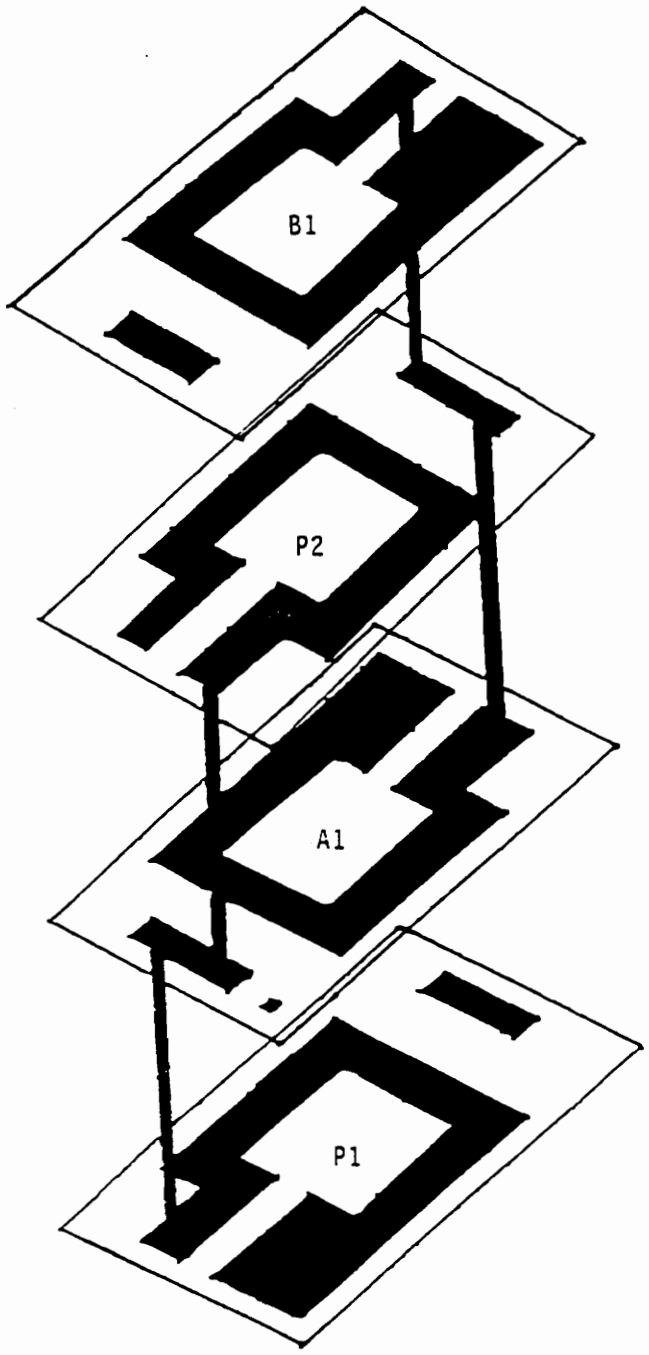


Figure 4.10. Buried-Via Interconnect Scheme

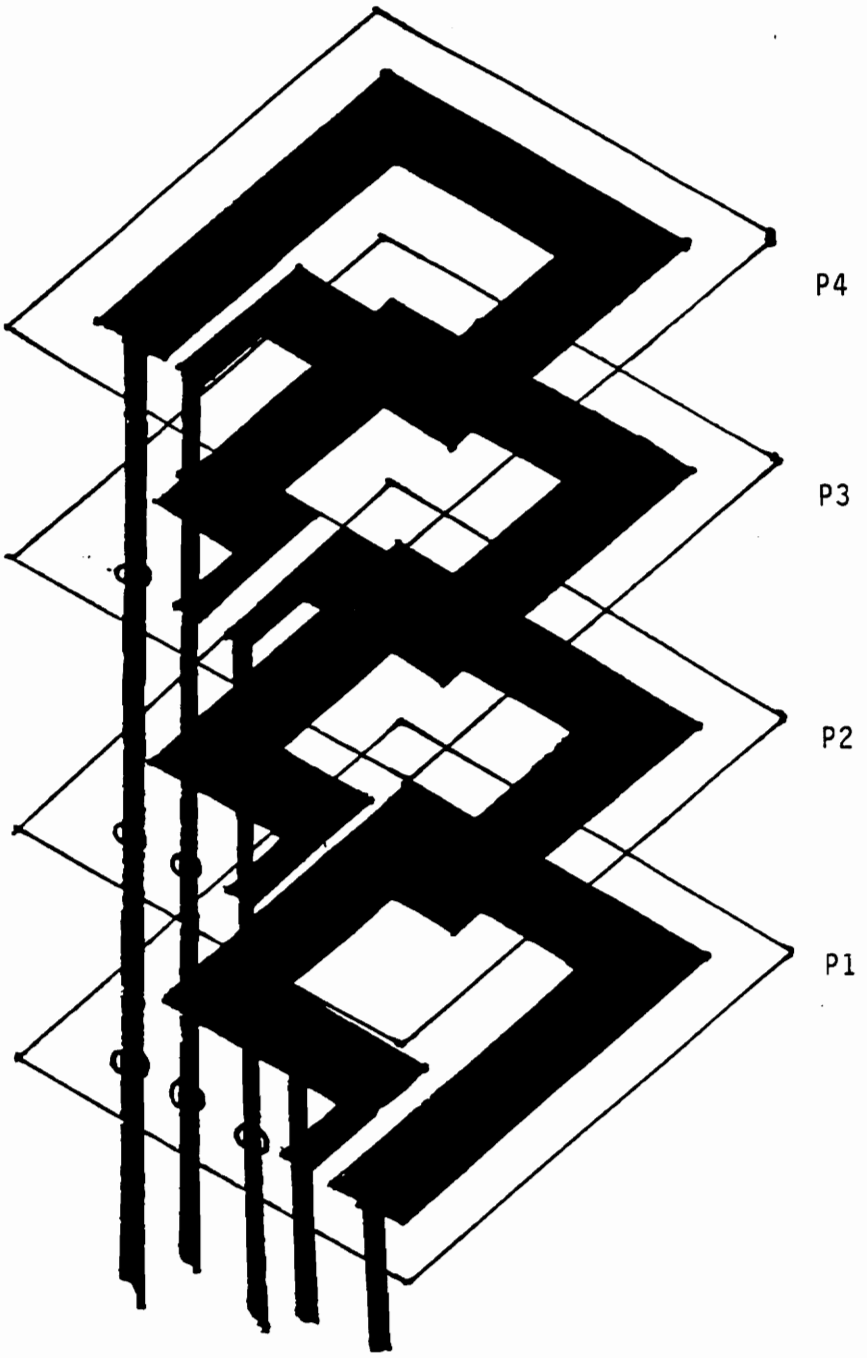


Figure 4.11. Through-hole Interconnect Scheme

4.6 Fabrication Technique

The planar windings are implemented using a flexible winding fabrication technique [8]. Pre-patterned copper foil already adhered to the Polyamid insulating layer is first etched. Vias are then opened either by using a high speed drill or a laser scribing system. Different layers conforming to the desired configurations are stacked in order. Vias were filled by an electrically conducting epoxy. Upon establishing the desired configuration, the entire structure is laminated under heat and pressure for a pre-determined period of time. Upon cooling, the structure will assume its low profile as shown in Fig. 4.12. This figure shows a 6:2 winding configuration with the primary interleaved with the secondary.

Due to the limited capabilities of a prototype fabrication facility, the winding structures were not realizable enough to provide accurate data. The problems encountered stemmed from the use of electrically-conductive epoxies to fill the vias. Electrically conductive epoxies compose of embedded conducting metallic particles in an organic binder, similar to conductor pastes used in the thick-film process. Therefore, the microstructure reveals conductive material which is not homogeneous throughout the epoxy. The binders in the epoxy would serve as gaps in the metallic content. In the presence of high frequency magnetic fields, these internal non-uniformly distributed non-metallic gaps will cause the formation of large fringing fluxes. These fringing fluxes will cause large eddy currents to flow in the conductive particles within the epoxy. The eddy current loss in the epoxy alone dominates the overall copper loss of the winding structure.

These structures utilizing the buried interconnect scheme are best fabricated in a printed-circuit-board manufacturing facility, where automated equipment are used for

laminating PCB's with buried vias, due to the hazardous chemicals involved in such work. Fabrication of such structures are done by sequentially copper-plating and laminating subsequent layers. Such a process is shown in Fig. 4.13. This is a more expensive process than the through-hole process, where the entire structure is laminated and then has vias filled by plating through-holes once. The main advantage of going to buried interconnects, with respect to transformer windings, include capability of a much higher number of layers without restriction to the window width. As the window width can be smaller and yet accomodate a large number of layers, the dc and ac resistances of the windings are smaller. This is a feature very attractive to the design of efficient high-density transformers.

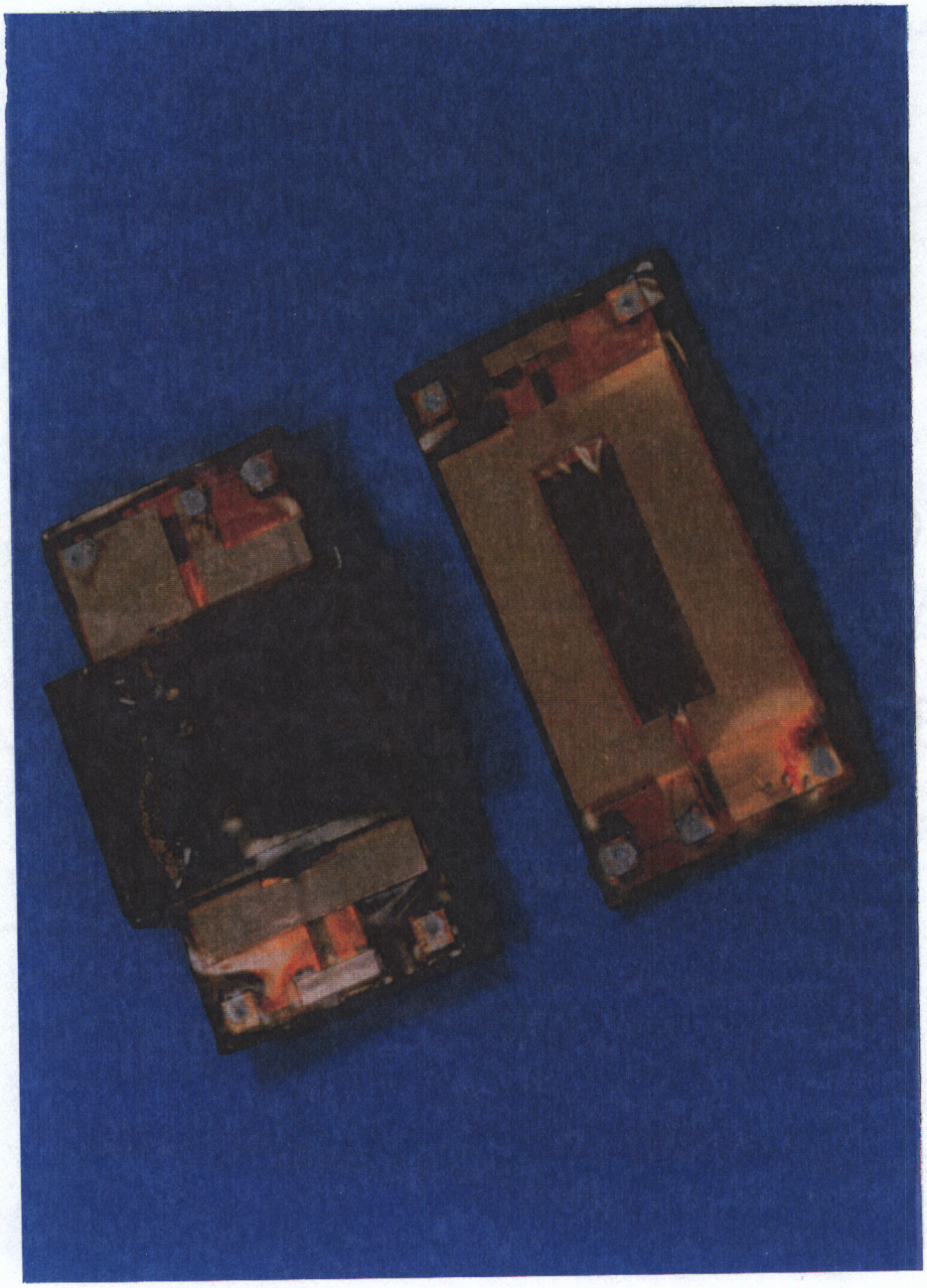


Figure 4.12. Prototype Interleaved Low-Profile Transformer

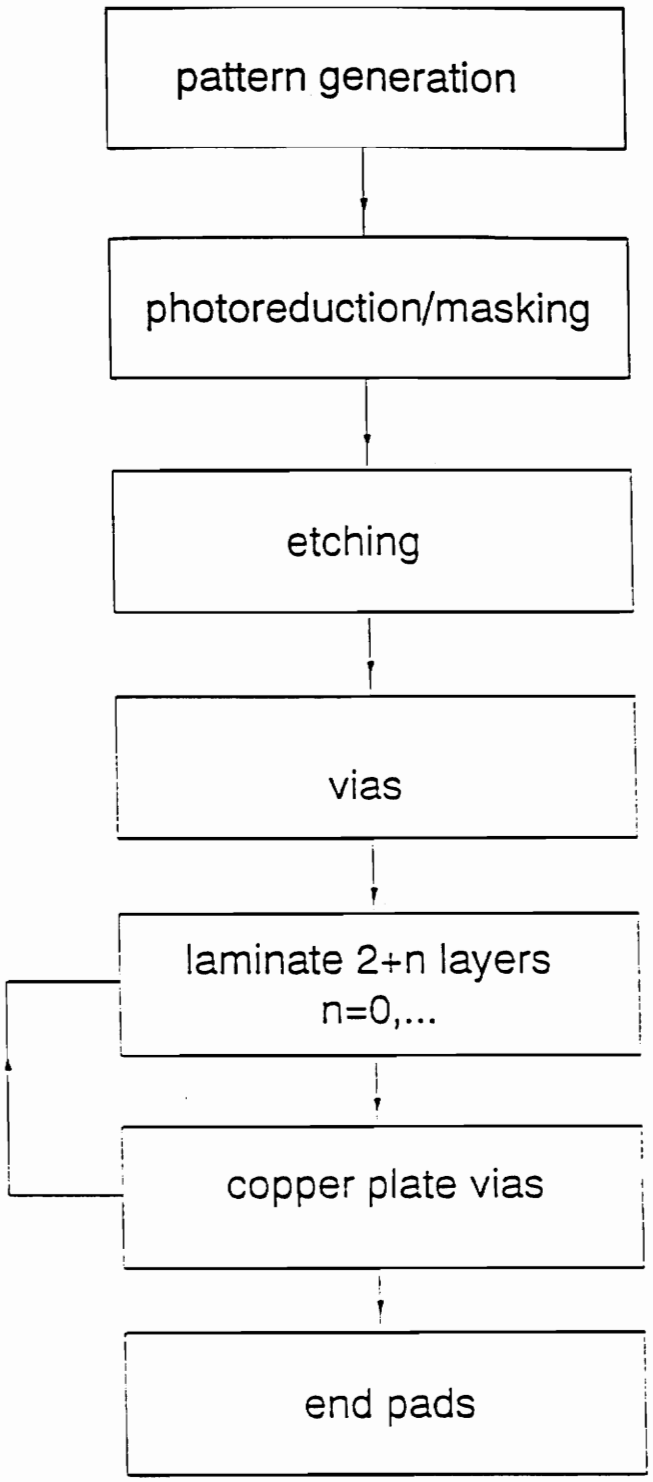


Figure 4.13. Process Flow-Chart for Fabricating Buried-Via Interconnection Windings

4.7 Summary

In this chapter, the round wire-copper foil versus the interleaved winding configurations used in the 50 W forward ZVS-MRC are studied.

For the transformer in the forward converter, 6-portioned interleaved windings so constructed would reduce the copper loss about three times. This is due to the greater reduction of the interlayer magnetic fields from multiple sectioning. Subsequently, the eddy currents generated are less than those in the 2-section round wire-copper foil winding configurations. If performance with respect to converter efficiency improvement from reduced copper loss in the transformer, less EMI and efficient use of copper material in the transformer windings is premium, then the benefits of using interleaved windings more than offset the costs involved in fabrication of these windings with the proposed interconnect scheme.

The interconnect scheme proposed allows automation and mass-production of windings with repeatable parasitic parameters. It also allows an increased number of layers not limited by the transformer width, but only by the transformer height. As these winding layers are typically in the order of mils thick, the window height, if needed, more than offsets the lateral width needed for via connection. This scheme appears attractive for the production of very efficient and high density transformers to be used in high-frequency switching power converters.

5 CONCLUSIONS

In this thesis, the feasibility of implementing very high-density power converters are investigated. The power stage, control stage, and magnetics have been individually investigated for implementation as high density power hybrids with hybrid microelectronics technology while adopting the ZVS-MRC technique for converter design at MHz frequencies.

A high density 25 W dc/dc flyback converter has been designed and built. It operated with a maximum efficiency of 76.1%. The power density of the converter was 55 W/in^3. With the implementation of a low-profile transformer, the converter was limited to 0.25" high, which makes it highly suitable for use as a board-mount supply. The high-density circuit has reduced lead inductances, which significantly reduced the voltage stress on the MOSFET. The waveforms obtained were also very clean. Due to the close contact of the transformer core to the thermally conductive substrate, the heat generated from core and copper losses are efficiently dissipated, increasing reliabilty. The losses dissipated in the relatively thin and narrow conductors can be reduced by using a metallic substrate clad with a thicker copper foil. This also improves heat dissipation.

A high density control circuit for a 50 W forward ZVS-MRC was designed and built. The use of an integrated controller with an opto-isolation circuit enabled the overall density of the converter to exceed 80 W/in^3. In comparison with a previous 50 W/in^3 version of the converter whose control circuit was designed and built using discrete surface mount components with a magnetic isolation circuit, the integrated controller circuit provided greater protection features, simpler circuitry with much less components, and a power-density increase of more than 65%.

The low-profile transformer of the 50 W forward ZVS-MRC was analyzed for its copper losses. The copper losses were analyzed using a finite element method software package for electromagnetics. The existing winding structure consisted of six primary turns of wire sandwiched between two secondary copper foils. A low-profile interleaved winding made from laminating copper etched on Polyamide was introduced. A finite element analysis was performed to show that winding structures using finite element analysis revealed that the interleaved structure relatively reduced the copper losses by about three times. The lower magnitude and more uniform current density distribution in the interleaved structure revealed more efficient use of copper material in the windings. The magnetic field strength of the interleaved structure was also reduced, presenting less EMI to the rest of the circuit. An interconnect scheme and and a fabrication process suitable for automation was introduced.

Future work is suggested in the areas where limitations currently exist. In the flyback converter, the application of aluminum substrates clad with relatively thick copper should be investigated. This should increase the efficiency by providing better heat dissipation and relatively low resistance conductor paths. The control circuitry should be optimized to include start-up and self-bias to completely modularize the converter. When ferrite substrates with better surface and mechanical properties become available, examination of feasbility of implementing filter circuits on such substrates should prove worthwhile. With respect to the high-density control circuit for the forward converter, a better isolation circuit in terms of simplicity and fast dynamic response characteristics should be investigated for implementation. This will be a straightforward task when the monolithic isolation chip, designed and developed by the team from AT&T Bell Labs [9], becomes commercially

available. In terms of low-profile magnetics, the eventual physical realization of the proposed interleaved winding structure for implementation into the converter to verify the analyzed results and qualify the potential applications should prove valuable.

REFERENCES

[1]. F. C. Lee, "High-Frequency Quasi-Resonant and Multi-Resonant Converter Technologies", IEEE International Conference on Industrial Electronics Proc., pp. 509-521, 1988.

[2]. W. A. Tabisz and F. C. Lee, "Design of High-Density On-Board Single- and Multiple-Output Multi-Resonant Converters", High-Frequency Power Conversion Conference Proc., pp. 45-57, 1990.

[3]. W. A. Tabisz, "High-Frequency Multi-Resonant Power Conversion Techniques", Ph.D. Dissertation, VPI & SU, Sept. 1990.

[4]. E. C. Snelling, Soft Ferrites, Butterworth, London, 1988.

[5]. C. Chin, J. Tero, M. Jovanovic, R. Ridley and F. Lee, "A New I.C. Controller for Resonant Mode Power Supplies", IEEE Applied Power Electronics Conference Proc., pp. 459-466, 1990.

[6]. P. Gradzki and F. C. Lee, "Design of High-Frequency Hybrid Power Transformer", IEEE Applied Power Electronics Conference Proc., pp. 319-326, 1988.

[7]. Ansoft Corporation, Maxwell^{R} Users Guide, 1990.

[8]. C. F. Coombs, Printed Circuits Handbook, Third Edition, McGraw-Hill Inc., 1988.

[9]. G. Knoedl, L. J. Turgeon, S. A. Rawls and J. W. Bess, "A Monolithic Signal Isolator", IEEE Applied Power Electronics Conference Proc., pp. 165-172, 1989.

[10]. D. C. Hopkins, "Development of a High-Density, Off-Line, Quasi-Resonant Converter Using Hybrid Techniques", Ph.D. Dissertation, VPI & SU, Aug. 1989.

[11]. P. L. Dowell, "Effects of Eddy Currents in Transformer Windings", Proc. IEE, Vol. 113, No. 8, pp. 1387-1394, August 1966.

VITA

The author was born on February 13, 1963 in Singapore. He graduated from the Singapore Polytechnic with a Diploma in Electrical Engineering in 1983 before enlisting in the Singapore Armed Forces for mandatory military service.

Upon discharge in 1986, he came to the United States in the Fall of that year to be enrolled in the Undergraduate program in Electrical Engineering at Virginia Polytechnic Institute and State University. As an undergraduate, he worked in the Hybrid Microelectronics Laboratory at Virginia Tech for three years under the direction of Dr. F. W. Stephenson. Upon graduation with a BSEE in the Spring of 1989, he joined the Virginia Power Electronics Center as a graduate research assistant to begin work towards his MSEE degree with Dr. Fred Lee as his principal advisor. His area of research interests are in high frequency power conversion, magnetics and high density packaging.

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He and Ms. Stella Tan will wed in October, 1991.