Analysis of High Density Interconnect Alternatives In Multichip Module Packaging Using the Analytic Hierarchy Process

by

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(Abstract)

Packaging of high density integrated circuits offers many challenges in the electronics industry today. Advanced requirements for high performance computing are starting to take advantage of multichip modules that are smaller in size and weight, use less energy, and cost less than prior technologies. This project and report provides a summary of the processes of multichip module packaging, and describes some of the companies and their technologies currently involved in the industry today. An advanced computer system is proposed that would require a high density multichip module. Functional requirements and performance specifications are identified for the system.

Many design decisions are required to determine the best integrated circuit package for the system, with trade-off analysis being key in the selection process. One comparative analysis worthy of study is the evaluation of high density interconnection alternatives.

Two technologies of multichip module designs are compared using the Analytic Hierarchy Process. Main attributes of the alternatives are chosen that are key to the design and have significant differences. The attributes are defined in detail and weighted based on their importance to the model. Performance data is also used in the comparisons of alternatives.

A spreadsheet program was developed to quickly enter the weighted values and performance data, perform the matrix calculations, and determine the final rankings of the alternatives. Sensitivity analysis was then applied to determine what effect a change in the value of a particular attribute had on the outcome of the rankings. Results of the sensitivity analysis for key attributes are graphically plotted.

Table of Contents

Figures

Tables

1.0 Introduction

Much interest has been generated to the application of multichip module (MCM) technology in the packaging of electronic circuits. Integrated circuits (ICs) have become faster and more complex through advances in semiconductor fabrication techniques. Until recently, enclosing the chips in packages for final assembly had evolved into a mature technology, with a predominant number of ICs packaged individually and mounted on printed circuit boards.

Current and future applications, however, point to a need for electronic systems requiring higher speeds, reduced weights and lower costs. Key to meeting these requirements is the use of high density interconnect (HDI) techniques for mounting several integrated circuit devices in a single, tightly spaced module.

High density packaging not only puts more memory and processing into a smaller footprint but using multiple chips also allows for a more flexible design. Integrating commercial, off-the-shelf (COTS) circuit devices into an MCM package eliminates significant development, design and production costs. Turnaround time for such an MCM is also greatly reduced because all the chips do not have to be custom designed from scratch.

In a time of shrinking budgets, the Department of Defense (DoD) has particular interest in the development of the high density multichip module. The military and space applications of the DoD, however, require more stringent packaging standards than typical commercial components to withstand harsh environments and achieve high levels of

reliability. Traditional solutions for DoD have led to very specific, custom designs leading to higher costs.

The key to meeting the industry's faster computing needs as well as military and space demands for electronics will be in providing high performance, high density packages that allow the flexibility for various chip sizes, designs and interconnections. The enclosure will also have to provide extremely rugged and reliable protection for many types of commercial grade ICs at a reasonable cost.

In this project and report, different multichip module processes and technologies available in the industry today are reviewed. Key product developments for MCM packaging are identified and described in detail.

Requirements for an advanced multichip module are defined in a proposed mission scenario, which is a new, high speed multi-processor workstation. Such an application places emphasis on factors such as performance, cost, streamlined packaging, reliability and expandability.

Of the factors that affect the design for such a high density multichip module package, chip interconnection is considered to be of prime importance. Two high density MCM technologies have been developed that are competing vigorously in both military and commercial markets and have distinctly different chip interconnect designs. The first, known as High Density Interconnect (HDI), is an advancement over traditional wire bonding and uses thin film metallurgy to make I/O connections. The second, Very Large Scale Integration, Chip On Silicon (VCOS), employs the flip chip method to connect the integrated circuits to a thin film mettalized silicon substrate.

Selection of the chip interconnection technique depends not only on cost but on several design factors. To assist in the selection process, the Analytic Hierarchy Process (AHP) is presented here. Key attributes of the multichip module are identified, performance data is applied and the attributes are weighted according to their importance in the overall design.

A spreadsheet computer program is used to calculate the overall rating of the chip interconnection alternatives presented, using AHP. The rating results can be used to help justify a technology or design features used in the MCM fabrication.

Sensitivity analysis is applied to key factors of the chip interconnection alternatives. Graphical representations are used to illustrate the effects attributes may have on the outcome of the decision process. An advantage of the sensitivity analysis is to show at what point the weight of the attribute will change the rating of a particular alternative to where it no longer is the desired choice.

1.1 Packaging Concepts for Integrated Circuits

The central component of any electronics system is the active device, which in the case of the integrated circuit package is the transistor. Through the years, improvements in the transistor in terms of reduced size and increased speeds have been the main driving force for progress in the packaging arena, continually tightening the constraints of size, weight, cost and consumption of energy.

In order for the active device to perform, it must be physically connected to other components so that it sends and receives the

appropriate signals to and from the outside world. In the case of multichip modules, this interconnection becomes a complex pattern that may need to be overlaid in several process steps. Often the chips must also connect to other discrete, secondary devices necessary to satisfy the design function.

The device or devices must also be protected from damage by the environment. For military or space applications, this environment could include excessive vibrations, shock, salt spray, heat and radiation.

Finally, the electronics give off heat when in operation. To avoid circuit damage from this heat, the design must include a means of heat dissipation. Therefore, to provide the necessary functions to physically support the devices, interconnect them, protect them and cool them the circuits must be encapsulated in a protective package, the concept which is shown in Figure 1.

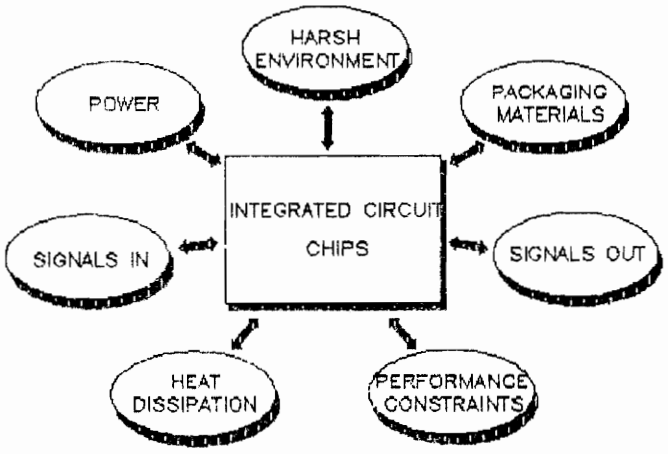

FIGURE 1: PACKAGING CONCEPTS OF THE INTEGRATED CIRCUIT

Integrated circuit packaging also has its drawbacks. Enclosing the devices in a protective shell increases the size and weight of the assembly, and adds more variability to performance and reliability factors. Most importantly, providing the proper packaging adds costs, which can often be more than the costs of the devices themselves.

Thus, the process of designing the appropriate package for high density integrated circuits is a combination of many functional requirements balanced with the constraints of the design. This is shown in Table 1.

Table 1. IC Packaging Factors

FUNCTIONS	CONSTRAINTS
Interconnection	Performance
Physical Support	Size
Environmental protection	Weight
	Testability
Heat Dissipation	Reliability
	Cost

These packaging factors apply in general to all integrated circuit assemblies. As the analysis of chip interconnection alternatives is undertaken in Section 4, certain constraints do not play a major role. For instance, size, weight and testability are all assumed to be equal for the alternatives when they are examined at the system level. On the other hand, cost, performance and reliability will vary between the choices, and hence they are attributes chosen to be applied in the decision making process.

1.2 Process Overview of Integrated Circuit Packaging

A general process flow for IC packaging is given in Figure 2. The first step is preparation of the semiconductor chips, or die. If the package is a single chip custom design, the manufacturer will most likely produce the circuits on its own wafer line. Before the chips are packaged, they are tested while in the wafer form. The wafer is precisely aligned, and finely tipped electrical probes make contact with the I/O pads of each chip. A computer connected to the probes provides an electrical stimulus to each die and measures the response. If a chip does not pass the test, it is marked for later separation from the wafer and then discarded. The wafer is then indexed through all of its useful sites and "probed" until it is fully tested.

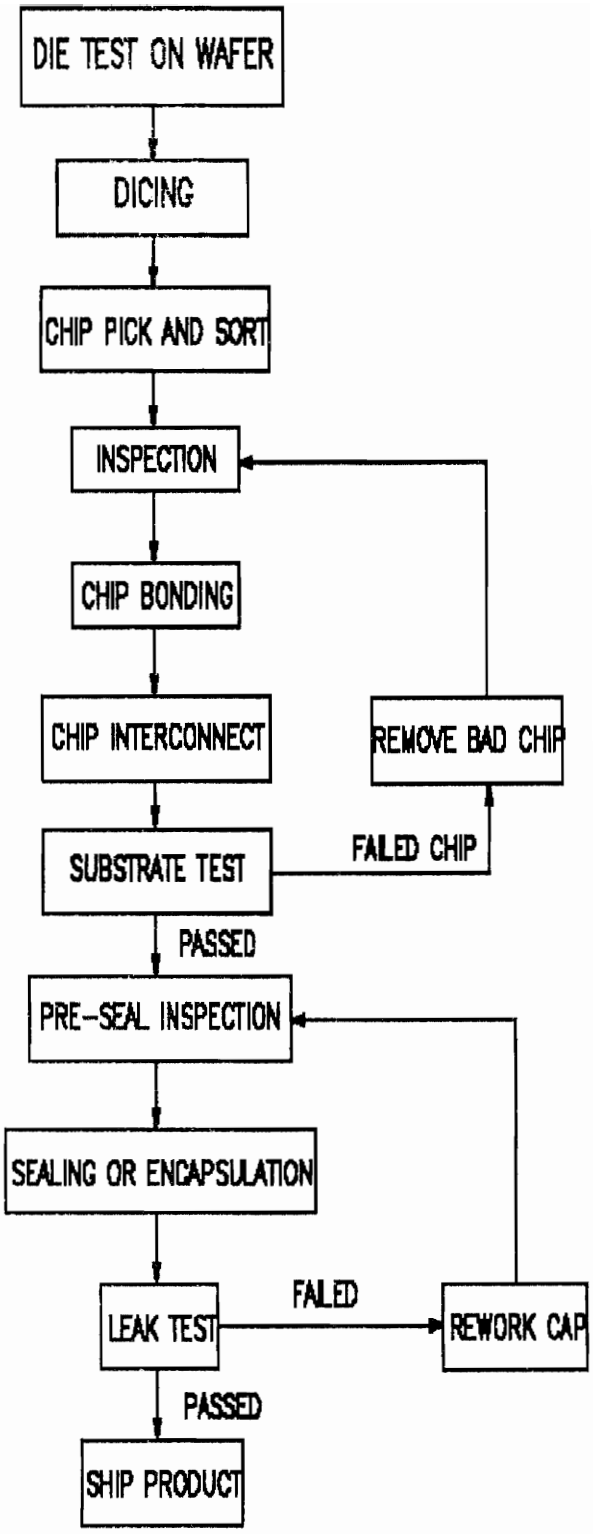

FIGURE 2. FLOW CHART FOR IC PACKAGING ASSEMBLY

Once the wafer has been tested, the die must be physically separated out and sorted into useful chips and rejects. The wafer is mounted onto a rigid frame with a mylar adhesive or secured to a vacuum chuck. It is then placed under a diamond tip circular wafer saw, which proceeds to cut very precise rows and columns, or "dice" the wafer so that all the devices are separated. The diced wafer is then place on a machine known as a chip picker, which physically removes the individual devices and sorts them into different chip carriers depending on whether they tested good or bad.

The next step in the IC assembly process is mounting the chip into the package. The device or devices are placed onto a smooth substrate surface that can be made of aluminaceramic or silicon, that has a metallized pattern overlaid on the surface for eventual connection to the die. Single chip packages that require high volume production normally utilize a stamped leadframe for reduced costs.

The semiconductor chips are typically mounted on the substrate with their active side up. In this case the die are bonded using either a gold-silicon eutectic, epoxy or glass-filled epoxy. Choice of the bonding material is dependent on the relative importance of the mechanical, electrical and thermal characteristics of the package. A comparison of the three is shown in table 2.

The chips, however, do not have to be mounted active side up. IBM has been long using a flip-chip process known as controlled collapsible chip connection (C-4). In recent years, this process has been adapted in various forms by several other companies in the industry. In this process, a solder ball or bump is formed on each I/O pad of the device. This pattern of solder balls is then aligned with a

duplicate pattern on the substrate and placed together. The chip and substrate solder balls are then reflowed together at high temperature to form both the signal connection and the bond of the device to the substrate.

TABLE 2. CHIP TO SUBSTRATE BONDING ALTERNATIVES
(ADAPTED FROM PRACTICAL VLSI FABRICATION FOR THE 90'S, ICE CORPORATION, 1990.)

DIE ATTACH TECHNIQUE	CONDUCTIVITY	CURING TEMP	MAX POST ATTACH TEMP	SHELF LIFE	COMMENTS
GOLD-SILICON EUTECTIC	THERMALLY AND ELECTRICALLY CONDUCTIVE	> 377 DEG C	475 DEG C	INDEFINITE	VERY EXPENSIVE REQUIRES DIE SCRUBBING POTENTIAL FOR VOIDS ON LARGE DIE SIZES ESTABLISHED PROCESS
EPOXY	THERMALLY CONDUCTIVE ONLY THERMALLY AND ELECTRICALLY CONDUCTIVE (SILVER OR GOLD BEARING)	120 C TO 175 C	300 C TO 400 C	8 MONTHS TO 12 MONTHS ---------- POT LFE FOR TWO COMPONENT MATERIALS: 4 HOURS TO 4 DAYS	INEXPENSIVE MAY REQUIRE TWO COMPONENT SYSTEM (RESIN AND HARDENER) NO SCRUBBING ESTABLISHED PROCESS
GLASS FRIT	THERMALLY AND ELECTRICALLY CONDUCTIVE (SILVER BEARING)	70 C TO 120 C DRYING FOLLOWED BY 420 C TO 460 C FUSION	500 DEG C	9 MONTHS	MODERATELY EXPENSIVE ONE COMPONENT SYSTEM NO SCRUBBING RELATIVELY NEW PROCESS FOR SILVER-BEARING GLASS

If the flip-chip process is not used, then interconnection of the devices to the substrate or leadframe can be achieved using wire bonds or a version of tape automated bonding (TAB). TAB processes are more practical for high volume, low cost operations and use copper

leads that are bonded or "bumped" with elevated pads on the ends of the leads. A simple heating tool can then be used to gang bond the leads to the pads of the device. Other versions of TAB include bumped TAB, which eliminates additional metallurgy being applied to the chips at the wafer level, and flip-TAB, which employs the TAB process in joining a flipped chip to a substrate.

Additional testing may take place prior to final encapsulation depending on the volume and yield requirements of the particular part. Testing at this point helps assure that good connection was made between device and substrate. Also, depending on how much heat is generated by the devices in the package, additional thermal conduction material may be added before sealing. This may be in the form of a paste or even a metal, and is often applied to the backside of devices that are flip-chip bonded to the substrate. This process step helps provide a more continuous path from the chip surface to the inside surface of the cap, increasing heat transfer capabilities.

Various module sealing techniques include transfer plastic molding, for inexpensive single chip leadframe packages, to circumferential sealing of metal caps with solder or epoxy.

2.0 Industry Background

2.1 Packaging Developments For Multichip Modules

As system speeds and performance requirements increase, the use of materials and processes in IC packaging will have a greater effect

and be much more important than in the past. No longer will packaging designers be able to assume that basic configuration decisions will hold for mounting, connecting and sealing the chips. The implications of the choices they make in the packaging will affect the very core of the system performance - that of optimally moving the signals from one device to another in the system.

Of the key decisions to be made in the packaging area, many fall into the category of materials selection. What is the best choice for a substrate carrier? Is the performance of dielectrics a key issue in the design? Is reworkability a key to the system's life-cycle? Is longevity, and hence reliability, a major concern, placing crucial emphasis on attributes such as hermetic sealing? Are there space limitations that require a more densely packed, multichip assembly? These questions and others must be closely scrutinized as various packaging alternatives are traded off in the preliminary design phase of IC project.

One trend that cannot be argued is that computer processing speeds are rapidly increasing and will continue to increase through to the next century. 300 megahertz (MHz) workstations with 3 nanosecond cycle times and 10 million gates that will need to dissipate around 1500 watts of heat are expected to be introduced on the market in the next 5 years[1].

Such a "superworkstation" would require high density multichip modules at the very least. To meet such advanced performance specifications, it is anticipated that hundreds of chips would be stacked

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1 Maliniak, D., **Future Packaging Depends Heavily on Materials**, Electronic Design, January, 1992.

and interconnected at a rate of about 1000 inches of wiring per inch squared. Several modules would still required for the memory and processing tasks, but it is expected that further advances in IC miniaturization would reduce the packaging so that only one MCM would be needed.

These reductions would bring with it a similar reduction in computer cost. Whereas initial offerings of the advanced workstation would be around $5000, it is hoped that reductions in chip counts and packaging requirements would by the year 2000 bring the cost down to around $2000.

For the near future, the costs of multichip module packaging are still considerably higher than single chip packaging, and thus their applications will continue to be focused primarily on the high end computer systems as well as customized military and space applications. There will not be wide spread use of MCM's in many other electronic products until they are needed to overcome performance constraints of the single chip packages.

When might this happen? There are at least two indicators today that may open the door for greater use of the MCM.

The shift to multichip modules could begin in high end desktop workstations as clock rates of the processors start to reach the 100 MHz range. Also, if larger cache memory is needed as is expected with future RISC-based, vector processing applications, the single chip, although continuing to advance with on board memory, may not be enough. MCM's will provide a key advantage in bringing the cache memory and the central processor into close proximity.

Whatever the reason, as demand for multichip modules increases, more and more emphasis will be placed on the proper selection of materials and processes that will provide the best performance at the least cost for the particular application involved.

2.1.1 Substrate Alternatives

Many choices of substrate are available today to carry the multiple chip sets in today's expanding packaging technologies.

Most prominent in use today in the low end of computer applications are laminated substrates that are fabricated and wired with processes similar to a printed circuit board. These substrates, referred to as MCM-L, are advantageous because they are inexpensive, but their wiring density is only in the 50 to 150 cm/cm^2 range. Processing speeds are also not capable of extending much past 200 MHz.

Advances in MCM-L technology in areas such as improved laminates and the addition of polyimides will increase the substrate performance somewhat and allow some gains in MCM applications at the low end due to its lower cost. As performance requirements increase, however, it is not likely that the MCM-L will be the substrate of choice for most multichip modules, especially ones of high density. Stability is a major concern for the material since it would be subjected to much higher thermal stresses as more and more chips are added to the module design.

Cofired ceramic is a second alternative for consideration as a substrate material, having been successfully used for many years in the

high end mainframe market. This technology, known as MCM-C, uses many ceramic layers to achieve higher densities of between 100 and 250 cm/cm^2. This process intensive technology is very costly, keeping most of the use and application to the most powerful computers.

Recent advances in the MCM-C area have led to increased performance of ceramic substrates. Glass-ceramic substrates, introduced by IBM in their System/390 computers, is a 5 in^2 package that can contain upwards of 120 chips. The substrate contains 63 layers and has one of the lowest dielectric constants in commercial production. Signal propagation is approximately 25% faster than on comparable alumina-ceramic modules with copper wiring densities up to 660 cm/cm^2.

As wiring densities on substrates for high end performance applications continue to increase every year, the usefulness of ceramic begins to have limitations. The primary reason for this is that ceramic substrates cannot be fabricated flat enough. As the line widths of the signal connections in the substrate get smaller and smaller, the imperfections of the ceramic will start to have a significant impact on yields.

To move into the gigahertz range for processors, it is likely that thin film deposited silicon substrates, known as MCM-D, will receive increased attention and use. MCM-D substrates are advantageous because they can be processed using the same or similar tooling as fabricating semiconductor IC's, which also allow more precise and miniaturized signal patterns. In addition, using silicon for both the substrate and the device to be mounted will allow for the best compatibility in thermal cycling. When the components are heated and cooled during normal use, the stress on the connections between chip

and substrate are significant, and dissimilar movements between the materials will cause joint fatigue and ultimately system failure.

Cost is the key drawback to the relatively newer technology. Present costs for MCM-D substrates range between \$50 to \$100 per in^2. Wiring densities, however, can be realized between 200 and 400 cm/cm^2, making them feasible alternatives when I/O counts surpass what is typical of the cofired ceramics.

A second important issue with MCM-D's is the dielectric material. Research has been ongoing into various materials with both lower and higher dielectric constants. As performance requirements increase, more concern is placed on the materials for their ability to withstand stress and to be compatible. This is illustrated in Figure 3.

For example, the lower the dielectric constant, the better the insulating qualities of the material. This is a key factor in the speed of signal propagation from chip to chip, as noise and capacitance will have an adverse affect on the signal performance. Recent developments such as integrating decoupling capacitors into multi-layer substrate fabrication have improved signal performance within the MCM-D substrate.

For the designer, the choice of substrate material and dielectric options will ultimately rely on a cost performance analysis of the application involved.

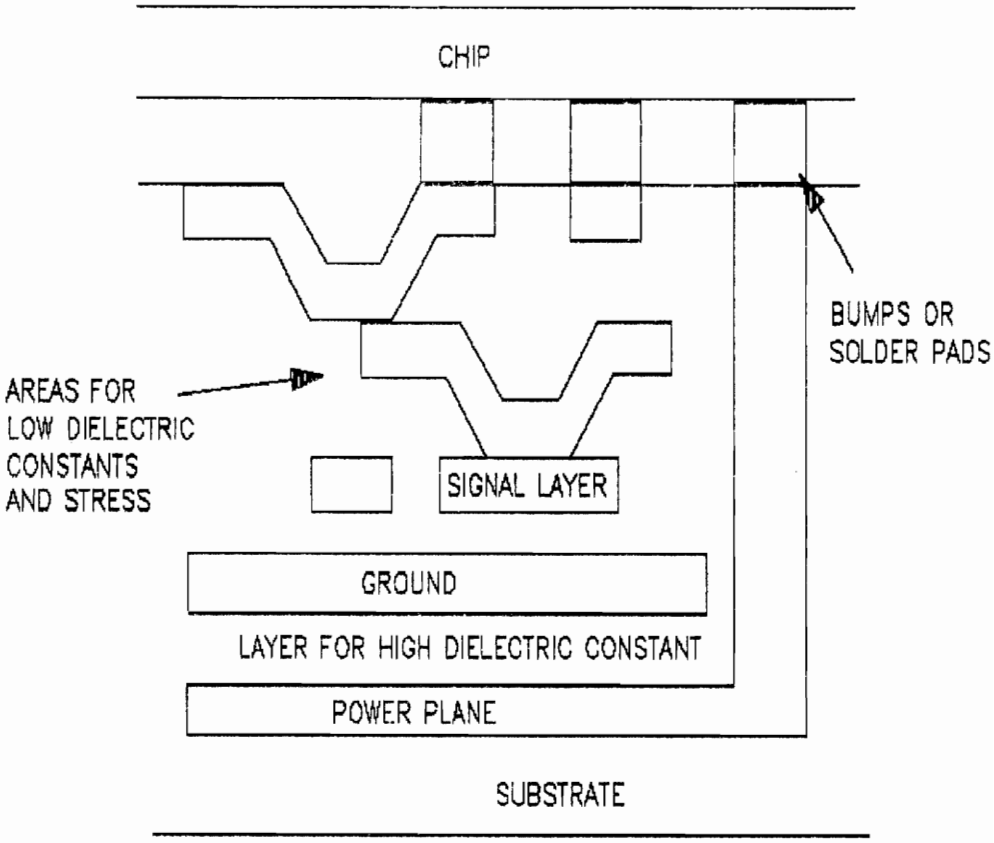

FIGURE 3. KEY FACTORS FOR DIELECTRIC MATERIALS

2.1.2 Chip Attachment Alternatives

As the substrates have evolved in the multichip module field, so too have the methods of chip interconnection and attachment. The four main methods that presently are available for consideration are wire bonding, tape automated bonding (TAB), flip-TAB, or flip-chip.

As more and more IC devices are placed closer and closer together on the same substrate, conventional wire bonding techniques can no longer be considered realistic to perform chip interconnection. Not only is there very little surface area left between chip locations to attach wires, but also the I/O counts of the individual devices have increased to the point where the physical connections are no longer limited to the periphery of the device.

A key restraint then for each of the interconnection methods is the minimum amount of space allowed between each device on the substrate. Current wire bonding technology employed by General Electric and Texas Instruments [8] lets the chips mount about 0.1 in. apart. Both TAB and flip-TAB reach their limit around 0.05 in., leaving just enough space for the leads to mount around the circumference.

The flip-chip method is by far the best space saver, requiring just 0.01 in. to separate the IC's. Typically, 0.02 in. are left in the layout to permit substrate repair or chip removal if necessary.

A disadvantage to the tight spacing allowed by the flip-chip method is the difficulty of handling the additional heat created. Thermal interface pastes have been shown to be helpful in improving heat transfer. When applied to the backside of a device flip-chip

mounted to a substrate, the paste provides a conductive path from the chip directly out to the module cap.

Whereas wirebonding is not as efficient a space saver as flip-chip, it is lower in cost. Also, as the wirebonding processes continue to improve, it will still command a significant share of the high end computer market.

With the integration of many different vendor IC's on one multichip module, a major concern exists with handling exposed silicon die, due to the fragile nature of the chips and their sensitivity to static. Testing the chips once they are in house can be a difficult process which adds significant cost to the product.

A new approach using wire bonding has been employed by General Electric and Texas Instruments which mounts the chips face up and then applies layers of metal and polyimide with the chips and substrates already bonded together. If rework is needed, the interconnecting layers can be removed, a new chip mounted, and new connections made via a computer driven laser patterning tool. Chips can be mounted as close as 0.01 in. apart. Thermal conductivity is improved as heat is transferred directly from the backside of the chip to the substrate out of the module. Also, devices do not require any C-4 pads or bumping, saving additional processes and cost.

2.1.3 Other High Density Interconnect Alternatives

To date, most emphasis placed on high density multichip packages has been on the placing of the devices horizontally on the surface of a

substrate. In order to achieve even higher integration, some packaging groups are looking beyond this design philosophy toward a version of mounting chips on their edges, stacking them like a cube.

This form of 3D packaging has been pursued for combining several high density memory chips into a small a space as possible. Once the devices have been stacked, the I/O from each top chip surface is rerouted with one additional layer of metallization out to one edge of the chip. These connections can then be bumped and TAB bonded or wire bonded to a leadframe or substrate.

3D packaging can result in tremendous performance or storage gains. For example, a cube of 10 1-Megabit (Mbit) static random access memory (SRAM) chips yields a memory density of 83 Mbits/in^3, compared with 2 Mbits/in^3 for conventional surface mounted devices.

Although still in the early research and development stages, 3D integrated circuit packaging is expected to play a significant role in future high performance computer systems.

Another variation in high density packaging permits a mixing of flip-chip IC's, surface mounted devices and through hole pin lead components onto a specially designed printed circuit board. Developed by IBM's Technology Applications Laboratory in Yasu, Japan, it is considered an extension of the MCM-L technology. Creating multiple wiring layers using photosensitive epoxy for insulating, the wiring density has been doubled compared to conventional pc boards.

Although the development of the surface laminar circuit (SLC) board does not come close to the densities of ceramics or thin film silicon substrates, it does provide a lower cost means of taking advantage of the flip-chip technology. This will hopefully allow some

high performance circuit devices to be applied to more low end computer systems.

Of major importance concerning all the packaging advancements of multichip modules is more flexible circuit design, leading to decreased development and overall product costs. The ability to take standardized, mature chip designs and integrate them into a high density package while still maintaining high switching speeds, environmental protection and reliability has been foremost in taking advantage of the new interconnection techniques.

2.2 Key Examples In the Industry

2.1.2 General Electric High Density Interconnect Technology (HDI)

General Electric, with support from the Advanced Research Projects Agency (ARPA), has developed multichip module packages that provide a fifteen fold reduction in area over conventional circuit boards. A typical comparison of similar processor units and associated electronics between a standard printed circuit board and the high density interconnect package is shown in Figure 4. The elimination of individual enclosures for IC's, the reduction of signal line lengths and the virtual elimination of final assembly operations all lead to significant decreases in costs and size and increases in performance of the system.

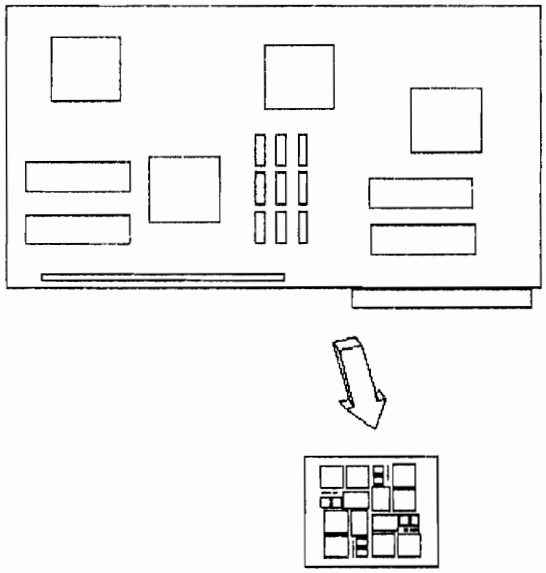

FIGURE 4. TYPICAL REDUCTION IN SIZE USING HIGH DENSITY MULTICHIP MODULE PACKAGING

The advantages of the PC board in the past were that it was well suited to maintenance, test and rework since individual circuits could be replaced or repaired without the need for a complete new card. These benefits can still be realized at the multichip module level given the new processes that are now utilized. The GE high density interconnect (HDI) module assembly process, shown in Figure 5, begins with the preparation of the substrate.

Rectangular pockets, or "chip wells" are milled into a finished piece of alumina ceramic using a diamond tipped cutter on a computer controlled milling machine. A metallization process then applies the signal and power lines that will eventually tie into the IC's and connect them to the outside world.

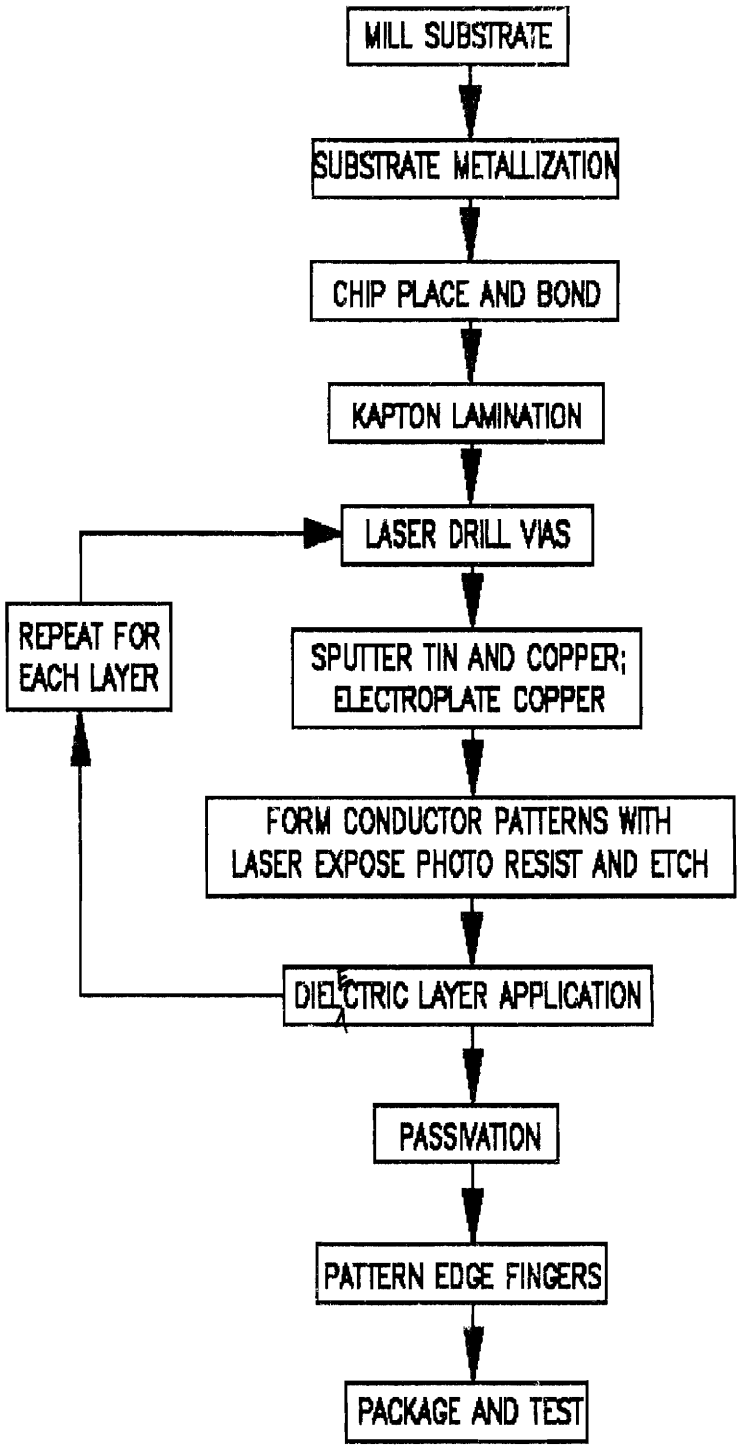

FIGURE 5. HDI PROCESS FLOW

Next actual IC chips, surface mount capacitors and resistors are attached to the substrate using conductive and non-conductive thermoplastic resins. Positional accuracy of the devices at this stage is somewhat coarse, and is not sufficient for mechanical alignment for making I/O connections.

A thin laminate sheet[2] is then applied over the entire top surface of the assembly, which serves to seal the substrate surface, act as the first layer of dielectric and fills in gaps created by oversized IC chip pockets. The substrate/carrier is then placed under a computer controlled scanning laser, which maps the exact positions and rotations of the IC's, and then adaptively performs the via hole drilling at all required locations.

Titanium and copper metals are next applied using sputter and electroplating processes. Negative photoresist is spun onto the surface and then etched to form necessary connector patterns. A second laser pass is then required to produce the final metallized connections.

Another layer of dielectric is now applied to the assembly to seal the components. Further layers can now be applied over this initial layer, if necessary, repeating the steps above, providing multiple layer connections and increased I/O capacity. General Electric has successfully built and tested HDI assemblies up to five layers.

When all layer applications are complete, passivation is applied for a final seal from outside contaminants. Then, after final test, if no defects are discovered, the HDI module can then be given its final packaging and testing prior to shipment.

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2 "Kapton," is a trademark of Du Pont Co.

2.2.2 IBM VLSI, Chip-on-Silicon Technology (VCOS)

IBM has recently shown advances in multichip module technology with the development of Very Large Scale Integration (VLSI) Chip-On-Silicon IC packages, known as VCOS. In the commercial sector, IBM designed the package to house the CMOS-II RS6000 chip processor set on a single module. This packaging scheme is becoming increasingly popular as more and more applications seek to take advantage of the RISC processing hardware.

The Federal System's Company (FSC) within IBM has sought to incorporate the VCOS packaging technology and commercially designed IC's and use them in conjunction with their own RISC System/6000 radiation hardened devices. In doing so FSC has replaced up to nine single chip packages with one multichip VCOS assembly, achieving a twelvefold reduction in active circuit board area. Also, by providing a hermetic seal at the card level using the high density hermetic card (HDHC), FSC is able to integrate commercial IC's into its system designs and still meet the rigid environmental and reliability requirements that are a part of the space and military applications.

The VCOS fabrication starts with the silicon substrate. Standard semiconductor processing techniques are used to apply the thin film wiring on top of the silicon. For dense I/O applications such as the RISC processor set, multiple layers are formed by intermittently applying insulating polyimide between the layers of metal.

To connect the IC devices to the substrate, IBM's flip-chip technology is used. C-4 pads are evaporated into place on both the substrate and chip active sides and then joined through a rigidly

controlled solder reflow process. Thermal expansion variations are minimized because the chip and substrate are both made of silicon, providing the solder joints with long life and high reliability.

Connection of this multichip substrate to the next higher level of assembly is achieved using flexible interconnect tape. This process is similar to Tape Automated Bonding (TAB) with the exception that the tape is applied in four individual segments on each edge of the substrate instead of all at once. Hot gas tooling is used to reflow solder for making the connection bonds to both the substrate and the board.

The VCOS multichip package was not designed for a highly protective hermetic seal at the module level, and on its own would not qualify for use in military of space applications. The HDHC design overcomes this, providing a hermetic seal at the card level. In addition, the VCOS module was initially designed to be cooled by forced air convection through a large heatsink mounted to the module cap. The Hermetic Card eliminated this by providing a conduction cooling path from the back of the substrate through the board and frame and out through the chassis.

2.2.3 Thin Film Copper on Microsubstrates

Another alternative to the packaging of multichip modules is the use of ceramic substrates with multiple levels of copper and polyimide for high density interconnection to the IC chips. This special substrate component was developed by Micro Substrate, Inc, and is

used in a similar fashion as the two previously mentioned technologies, but has certain key features which distinguish it from the HDI or the VCOS substrates.

First and foremost, both sides of the ceramic substrate are used to make high density interconnects. If one side is used for mounting the IC chips and the other side for multi-layer circuit I/O, then the ability to rework devices is provided without delaminating the polyimide layers.

The microsubstrate also has the feature of a decoupling capacitor to provide stability between the power and ground lines. This is achieved by applying a thin layer of tantalum pentoxide between the power plane and the ground plane. This process allows for integration into the package, which is not possible with silicon substrates.

Finally, chip bonding techniques are not limited to one process. Wire bond, tape automated bonding and flip-chip attachments can all be potentially used with the microsubstrate.

3.0 A System Definition for MCM Requirements

3.1 Mission Scenario/Functional Requirements

A high performance computer system is desired for scientific applications in the academic communities and corporate laboratories. It will be required to perform intense calculations and complex mathematical analysis in relatively short time periods. It must be able to

handle large operating systems, and local and wide area network management software.

Traditionally, these tasks were accomplished through the use of robust mainframe or minicomputers that required considerable personnel to support and maintain, as well as separate rooms and air conditioning for operation. The objective of the new system will be to accomplish the computation and communication requirements in a stand alone workstation that would reside in a normal office environment.

Achieving this high performance will require high central processing unit (CPU) speeds as well as multiple processor units. Clock rates starting at 300 Mhz are to be assumed, with the potential to eventually reach 1 gigahertz. Initial active memory required will be 128 megabyte (Mb) with the potential expansion to 512 Mb.

The processor and memory devices must be packaged as closely together as possible to maintain performance requirements as well as save space in the unit. The computer system unit design is projected to be a tower chassis that will be able to fit next to or underneath standard office furniture. Only one card slot in the chassis is allowed for processor and memory installation for the basic unit.

Heat dissipation is planned using air convection only. Muffin fans located in the rear of the unit will create the air flow that will cool the integrated circuit packages.

The computer workstations are expected to operate in a full time or near full time capacity, 24 hours/day, 7 days/week. The minimum mean time between failure (MTBF) of the MCM's is to be 40,000 hours.

When service is required, ease of maintenance is crucial to bringing the system back on line as quickly as possible. All modules

and system boards will be designed with self diagnostics and provide fault isolation to the board level. The board will be the lowest level of spare assembly, be replaced in the field and shipped back to the factory for rework or scrap. The mean time to repair (MTTR) will consist of overnight or express shipment of the spare board and board replacement in the system by the user. Maintenance time, excluding shipment and handling, should be less than 30 minutes.

Expandability is important in the system design. Upgrading to future components that allow faster processing and larger memory should be accomplished by a simple PC board substitution or multichip module replacement.

Demand for the high performance computing machine should be relatively strong. Initial pricing for the system is to be targeted at around $25,000, but it is anticipated that streamlined manufacturing and cost/performance improvements in the semiconductor devices and packaging will continue to drive the price down to where the cost is competitive with current high end workstations. Production rates are forecasted at 1000 units/month.

3.2 MCM Design Alternatives in the System

Determining the choice for the integrated circuit package necessary to meet the system requirements will be accomplished in the preliminary design phase, as illustrated in Figure 6.

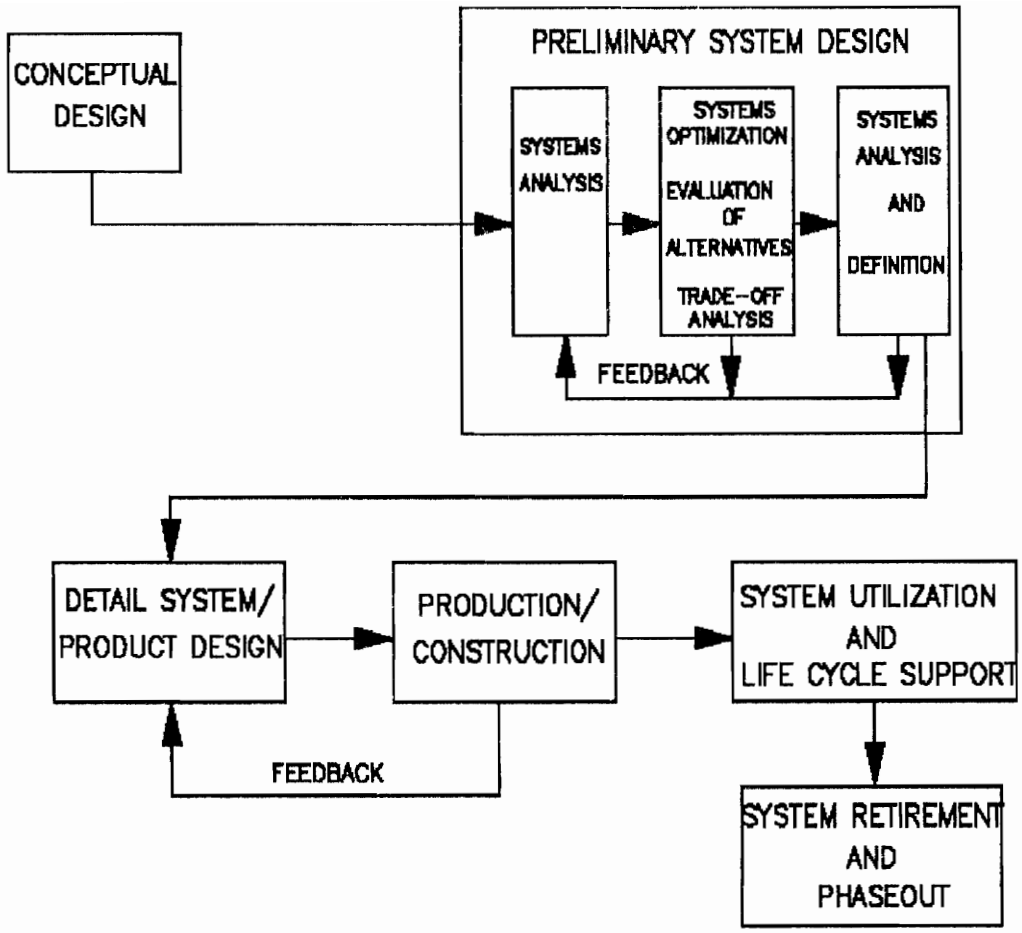

FIGURE 6: SYSTEM LIFE CYCLE PROCESSES
(ADAPTED FROM SYSTEMS ENGINEERING AND ANALYSIS, BLANCHARD AND FABRYCKY, 1990)

The need for high processing speed, large memory storage and future expandability in a relatively small package point towards the use of MCM-D, or deposited thin film technology. Although higher in cost than laminated substrate (MCM-L) or ceramic substrate (MCM-C) assemblies, the MCM-D technology appears to be the only one capable of

achieving the high densities needed to meet the current and future system requirements. A trade-off analysis between the MCM-D technologies in general vs. MCM-C's and single chip module packages would be required to verify this decision.

Given the MCM-D as the type of technology to be used, a key issue to resolve is whether the devices for the module can be purchased off the shelf, or whether a custom chip or chips will be needed for the system. For the requirements stated in the previous section, it is assumed that commercial off the shelf devices will meet initial system needs. Future upgrades for higher performance, however, may require custom circuits and special chip designs. Additional analysis will be useful to know at what point system performance can no longer be improved with existing chip sets. Going to custom or state of the art devices not only increase material costs of MCM fabrication, but lower yields of the new chips will increase rework costs and possibly reduce reliability.

The effect that the design of the multichip module has on operation, maintenance and disposal costs of the system should also be considered at this point in the preliminary system design. Although the MCM will influence these, it is assumed here that the choice between alternatives will not change the costs at the system level. The levels of reliability for the choices, although different, are all high enough to meet system requirements. What is important to recognize here is that the costs attributable to the MCM are identified for the various parts of the system life cycle and they can be justified in the final design.

Two MCM-D technologies currently involved in intense competition and development are the GE high density interconnect (HDI) design and

the IBM VLSI Chip on Silicon (VCOS) package. Until recently, these multichip module offerings were geared primarily towards military and space applications, where performance, reliability and reduced packaging take precedence over cost. This is changing today as defense budgets are reduced or eliminated and both companies seek to increase their customer base to make MCM production more feasible.

The following section provides an in depth comparative analysis of the two types of high density interconnect technologies, and makes use of the Analytic Hierarchy Process to rate the alternatives to aid in making the design decisions for the optimum system.

4.0 Comparative Analysis of Chip Interconnection Alternatives

4.1 Definition of Attributes

Electrical Performance - Delays in signals associated with the type of chip interconnections, line widths and dielectric materials are features that affect the electrical performance of the MCM package and hence the processing speed of the computer.

Materials with lower dielectric values in the thin film layers provide the best conditions for signal propagation. High dielectric materials, on the other hand, provide the best insulation between power and signal lines, minimizing the noise produced.

Electrical performance can be determined by measuring the inductance, capacitance and resistance values present in the module package.

Thermal Performance - the ability of the multichip module package to remove heat from the integrated circuits so that the system will operate without any performance degradation or failure.

Reliability - the projected Mean Time Between Failure (MTBF) for the multichip module package.

Rework - the process by which the MCM is disassembled, defective or outdated devices are removed, new devices are attached, the module is resealed and reused.

Risk - achieving higher processing speeds not only will require enhanced packaging of the MCM but faster semiconductor chips as well. These devices will initially be manufactured with lower yields, putting a greater demand on efficient rework, and may potentially have reliability problems. Mature chips and processes, on the other hand, will reduce rework burden and thus overall costs.

Production Cost - The dollar amount required to produce one high density interconnect MCM given a production rate of 1000 modules/month. Each alternative is assumed to have the same number of devices assembled into the package.

Rework Cost - The dollar amount required to support rework of a percentage of the multichip modules, assuming yield rates of the particular integrated circuits chosen in the design.

4.2 The Analytic Hierarchy Process

The decision of choosing the appropriate materials or process technologies for high density multichip modules can be categorized as a multiattribute decision problem, and is well suited for the analytic hierarchy process. Developed by Thomas Saaty, AHP has been applied successfully in many fields engineering, science and business.

In this process, functional hierarchies, or levels, are defined for the particular problem. For the decision of alternatives for chip interconnection, these levels are outlined in Figure 7.

The top level represents the overall objective in the decision and is called the focus, which is in this case is determining the optimum high density interconnect package for the particular application. The alternatives are positioned at the bottom of the hierarchy chart.

Attributes for the two alternatives are shown in the middle of the hierarchy chart in Figure 7. The main attributes are shown as being Level II in the process. These can be further broken down into sub-attributes, which would then constitute a Level III.

Each level of attributes may have several elements, but typically 5 to 9 attributes are the maximum number that allow for accuracy in evaluating the alternatives. It is important to maintain the analysis on the key elements that affect the alternatives.

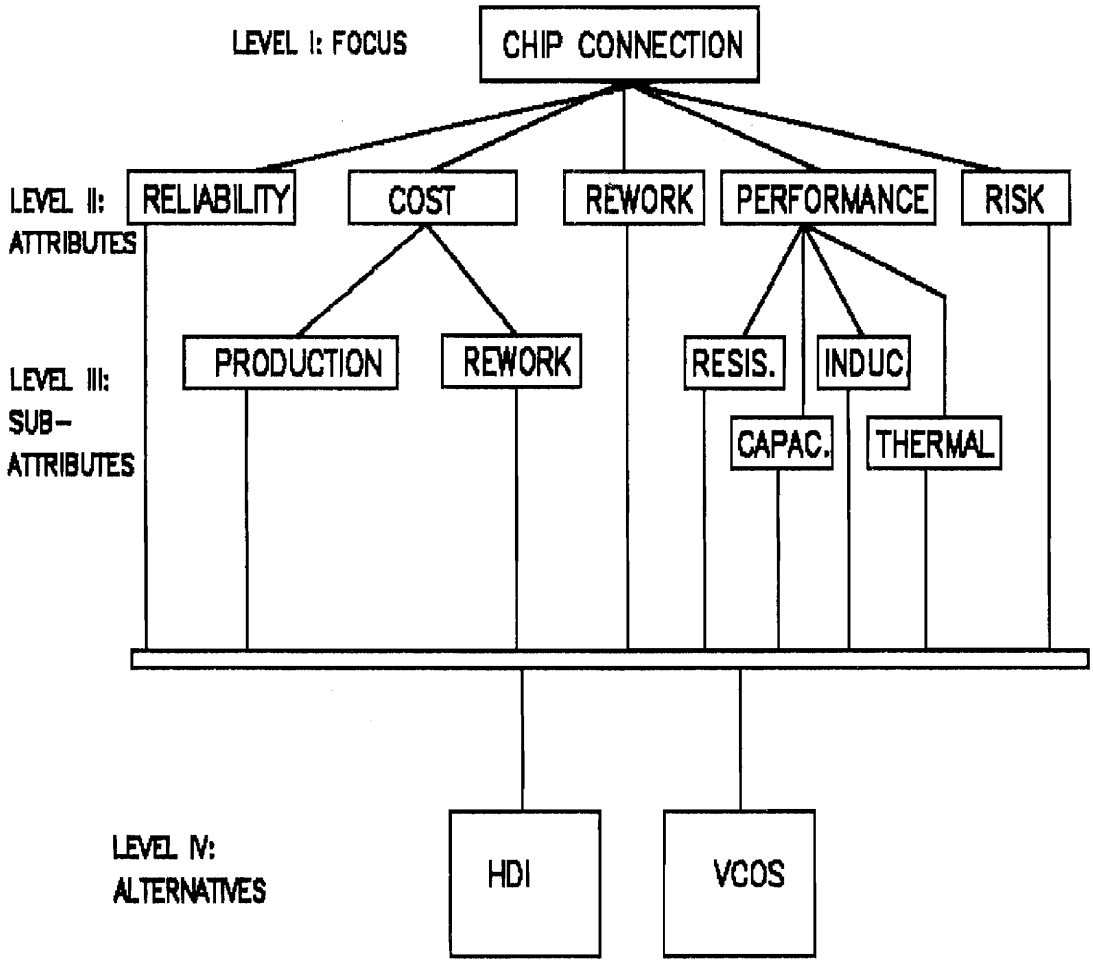

FIGURE 7. CHIP CONNECT DECISION ANALYSIS USING AHP

The methodology in using the analytic hierarchy process is to take the attributes, sub-attributes and alternatives and make a series of pairwise comparisons of a given level with respect to the level just above. The attributes and sub-attributes are also weighted with respect to one another to establish their relative importance. Next, the alternatives are compared and weighted against each other for each sub-attribute and each attribute. Matrix algebra is used to calculate the overall priority weights or score of each alternative. Consistency ratios are also determined from the matrices, with a consistency ratio less than 0.1 considered acceptable for the analysis.

A spreadsheet computer program calculates the overall rating and ranking of alternatives for AHP. The program allows for easy adjustment of the weights for each attribute to quickly examine the effect on the outcome of the alternatives. In addition, performance data can be used in place of weighted numbers in comparing attributes. This is most useful when actual numbers are known, such as costs or benefits (dollars), cycle time (hours), payback (months or years), or technical data gathered from measurement or experimentation.

The AHP calculations for alternatives for the chip interconnection model are shown in Appendix A.

4.3 Rating the Attributes

4.3.1 Weighting the Attributes at the System Level

It is desirable for the system engineers who defined the computer workstation described in Section 3 to choose a multichip module alternative that best meets system needs. To do this, the engineers should look at the main attributes of the MCM's and determine, to the best of their ability, how important each attribute is relative to the system. This understanding can then be applied to the first level matrix (Level II) in the Analytic Hierarchy Process to compare the attributes against each other. From initial data gathered, it has been determined that both multichip module alternatives will meet minimum system requirements.

The five main attributes of the MCM alternatives that affect the system are cost, performance, reliability, rework and risk. These attributes are by no means final in the decision process for the multichip module. As information is synthesized in the preliminary design phase for the system, the objectives for the computer workstation could well be adjusted, leading to the promotion or demotion of one or more of the attributes as well as adjustment to the weighting factors in the Level II matrix.

Cost is always a key consideration in any selection process. Often the least expensive alternative is the sole criterion for selection once minimum requirements are met. In this case, however, system engineers are not rigidly constrained. Surveys have indicated that customers purchasing computer systems in this category place a greater emphasis

on performance related factors than price, as compared to personal computer purchases, where price is a much more important discriminator.

Realizing that customers would likely pay more for higher performance relative to currently available systems within the same range, system engineers may consider the performance attribute to be more important than the cost attribute. Reliability, however, cannot suffer for the sake of performance. If increased performance comes at reduced reliability then, in general, it is not desirable. Thus, reliability is to be rated equally important as performance and slightly more important than low cost.

The rework process will have a bearing on the MCM selection for expansion and upgradability. System designers would like to take advantage of future IC devices that are faster and of higher capacity while making use of the current MCM package. The rework process would allow the multichip module to be removed, disassembled, refitted with new devices, resealed, and retested. Although this requirement is important, engineers believe that the high level of uncertainty with future chip designs puts the factor of rework as less important than cost and much less important than reliability and performance.

Risk is the final main attribute to be scrutinized. Availability and timely delivery are important in meeting customer expectations. Choosing a multichip module design with mature processes and proven field data is less risky than an alternative whose state-of-the-art processes may perform well in the laboratory but has little or no field data to back it up. System engineers may be willing to take some risk, but not much, to achieve a better system. This approach leads the

system engineers to assign risk slightly less of an importance relative to rework, less importance relative to cost, and much less importance relative to performance and reliability.

The preceding background on the five main attributes of the multichip modules can now be used to assign weights in the Level II matrix of the Analytic Hierarchy Process. The general question is asked, "How much more important is attribute A (e.g., lower cost) relative to attribute B (e.g. performance)?" The weighting scale developed by the system engineers is shown in Table 3.

TABLE 3. Weighting Scale Factors

Much More Important	4
More Important	3
Slightly More Important	2
Equally Important	1
Slightly Less Important	1/2
Less Important	1/3
Much Less Important	1/4

The process of weighting attributes is not an exact science, but rather is a judgment of a perceived importance of one attribute over another. Poor or faulty judgments could lead to inaccurate results. Sensitivity analysis helps to minimize this by showing the effect a weight or a percent share that one attribute has on the outcome of the

decision that is being made. Section 5 provides key examples of sensitivity analysis based on the output from the AHP analysis.

Based on the systems review of attributes, and the weighting scale factors in Table 3, the Level II matrix can be calculated. The percent share values for each main attribute can then be determined as shown in Table 4.

Table 4: Level II Comparisons

	Cost	Perf	Reliab	Rew	Risk	
Cost	1.000	0.333	0.500	3.000	4.000	
Perf	3.000	1.000	1.000	4.000	4.000	
Reliab	2.000	1.000	1.000	4.000	3.000	
Rew	0.333	0.250	0.250	1.000	2.000	
Risk	0.250	0.250	0.333	0.500	1.000	
	Normalized					Avg
Cost	0.152	0.118	0.162	0.240	0.286	0.191
Perf	0.456	0.353	0.324	0.320	0.286	0.348
Reliab	0.304	0.353	0.324	0.320	0.214	0.303
Rew	0.051	0.088	0.081	0.080	0.143	0.089
Risk	0.038	0.088	0.108	0.040	0.071	0.069

4.3.2 Weighting the Attributes Between Alternatives

Performance - Electrical performance data on resistance, inductance and capacitance [7] have shown the HDI to be better than VCOS. Resistance values are measured in m-ohms, inductance values in nH and capacitance values in pF. Thermal performance from Ozmat [10] also give an advantage to the HDI technology. Since the backside of the

chip offers full surface contact between chip and substrate on the HDI technology, better heat transfer is obtained than the VCOS solder joint path.

Thermal performance could be improved on the VCOS package by adding thermally conductive paste to the device backside, creating a constant path for heat out through the module cap. At this time, though, the added process and manufacturing steps are too costly. Overall performance for the VCOS MCM is considered to be sufficient at this time, but as more powerful devices are used that run hotter, additional heat dissipation methods will need to be considered.

The values for resistance, inductance, capacitance and thermal resistance are given in Appendix A, Table A7.

<u>Reliability</u> - Both the HDI thin film metallurgy and the VCOS solder joint appear to meet the reliability specification set out in the computer system requirements. There is a lengthy history on C4 studies to support the flip chip method reliability, as well as years of field data on thousands of various computer systems. HDI interconnections, on the other hand, have indicated high reliability in initial test samplings, but have little field use history. Also, there is no data quantifying the impact of the thin film processes on top of the devices after they are placed, unlike C4, which performs chip join after all thin films have been processed on the substrate.

Based on historical data on similar MCM packages, VCOS is expected to have a MTBF of 85,000 hours, and HDI is estimated to be about 50,000 hours. Also, since both alternatives currently exceed

system requirements, reliability will be rated low relative to the other attributes in the Level II analysis.

Rework - Although GE has claimed straightforward rework processes with HDI, to date no data has been released in support of this. Complete destruction and rebuild of the interconnect structure must be accomplished for proper HDI rework. This cost is comparable to initial fabrication costs, as reported by GE at the 1991 High Density Interconnect Symposium at DuPont.

The flip chip method employed by VCOS, however, has had a mature rework process for multichip modules for many years, is non-destructive and is only a fraction of initial build costs. Thus the rating for VCOS rework is weighted as much better than HDI.

Risk - Since more data is available on flip chip interconnect processes than HDI and rework processes for VCOS are more efficient, then the level of risk for HDI will be higher than for VCOS. Since some newer high speed IC's will be used to meet future processor and memory requirements resulting in lower yields and additional rework and upgrade, VCOS is weighted as a better risk than HDI.

Production Costs - For equivalent I/O capacities, number of chips and production rates, it is assumed that VCOS will be slightly more costly to produce than HDI, due to the additional C4 processes on the device and substrate required for chip attachment. Based on circuit complexity, number of devices required to meet system requirements

and production forecasts, the HDI module is estimated to cost $3,500 and the VCOS module $4,000.

Rework Costs - Rework costs for HDI will be higher due to the destruction and reconstruction necessary for the thin film layers, and these processes are still being developed. It is assumed that 1 chip is being replaced, the new device attached, reconnected and the module resealed and retested. HDI rework costs per module will be approximately $3,000 whereas VCOS rework will cost $1,000.

The values defined above are entered into the AHP spreadsheet program in Appendix A. The ratings outcome indicate that the VCOS technology is the preferred choice over HDI, but only by a slight margin, .508 to .492.

5.0 Sensitivity Analysis

The close overall ratings of the alternatives in the chip interconnect model indicate that sensitivity analysis is very important in the decision making process.

In the sensitivity analysis, the weight of one of the attributes under examination is allowed to vary by adjusting the corresponding values for the attribute in its respective main comparison matrix. The spreadsheet program then automatically calculates the percentage weights, averages and final rankings of the alternatives.

For the chip interconnection model, the weight or performance of certain attributes can significantly affect the outcome of the decision.

The analysis of reliability is shown first in Figure 8. It can be seen that a relatively small increase in the MTTF hours for HDI will improve the enough to make it the desired alternative. At an increase of just 6000 hours for HDI reliability, the alternatives become equally desirable.

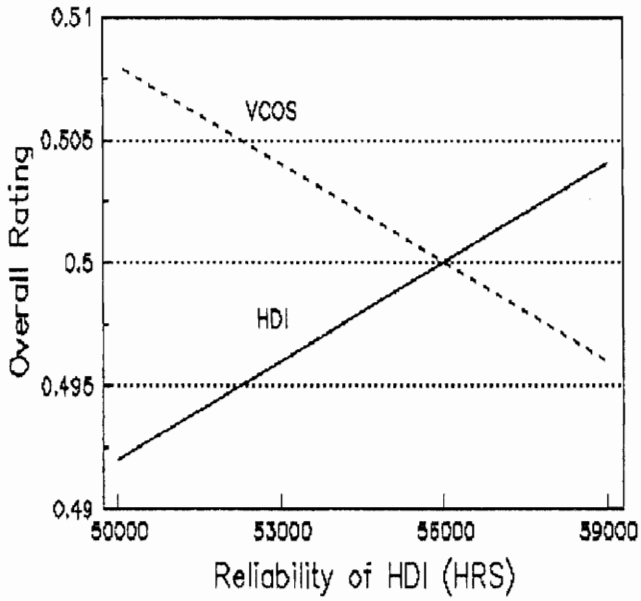

FIGURE 8. SENSITIVITY ANALYSIS FOR RELIABILITY

Figure 9 shows at what point cost improvements in HDI rework could cause the outcome preference of the alternatives to switch. If all other factors in the model remain unchanged, then HDI rework costs must be reduced to approximately $1750 before it can be considered equally desirable as VCOS. Since cost at the system level was allocated

only a weight of .191, it can be concluded that higher weighting of cost would result in a lower cost reduction required for HDI to become the better alternative.

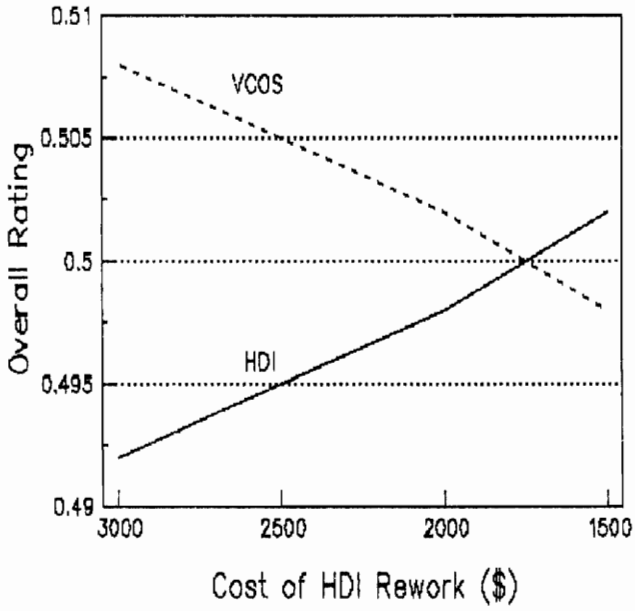

FIGURE 9. SENSITIVITY ANALYSIS FOR REWORK COST

A third attribute sensitive to the outcome is risk. Figure 10 illustrates how the weighting of HDI relative to VCOS with respect to risk has on the outcome of the decision analysis. In the current model, HDI is considered riskier than VCOS and is given the value .333 to VCOS's .667. It can be seen from Figure 10 that adjusting the weight to just above .5 (slightly risky) would make the decision outcome equal,

whereas a weight of 1 (equally risky) would push the outcome in favor of HDI.

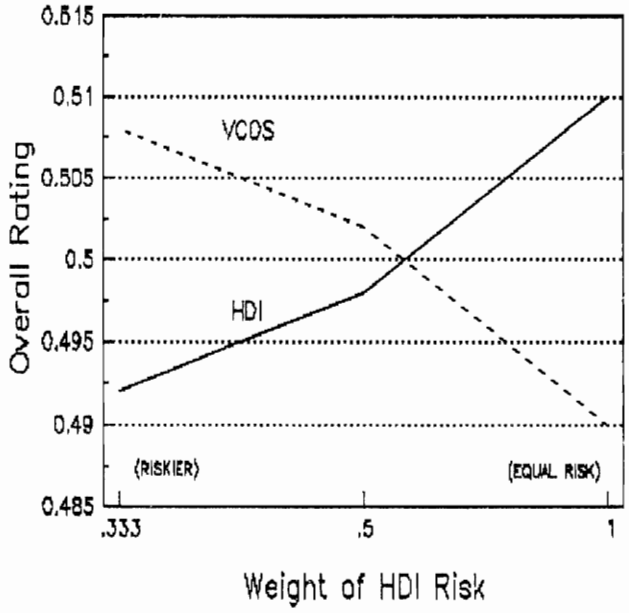

FIGURE 10. SENSITIVITY ANALYSIS FOR RISK

In the Level II comparisons, attributes are also shown to be sensitive, but their relationships are not as linear as in the comparison of attributes between alternatives, due to the greater number of relationships in the larger matrix. A good example is the weight of performance relative to reliability in the Level II matrix. In the initial model, performance was weighted equally to reliability. If performance is allowed to increase in importance relative to reliability, then HDI can

become the preferred alternative again. This relationship is illustrated in Figure 11.

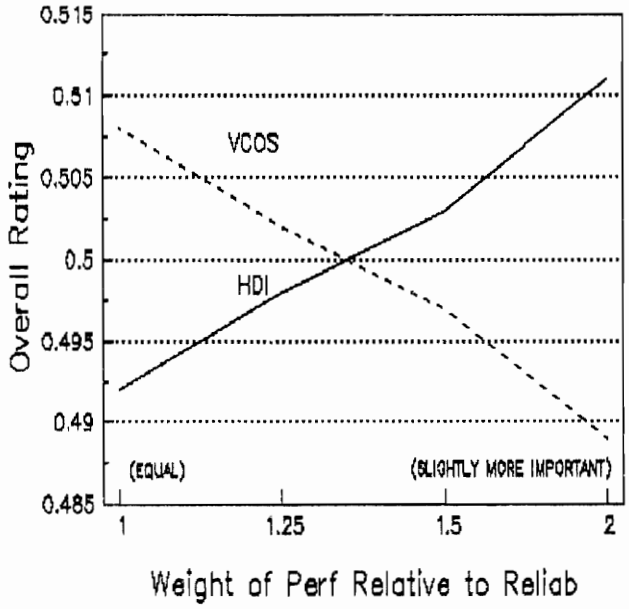

FIGURE 11. SENSITIVITY ANALYSIS OF PERFORMANCE RELATIVE TO RELIABILITY FOR LEVEL II COMPARISONS

A second Level II relationship that is sensitive is the weight of cost relative to reliability. Figure 12 shows that if cost is given slightly more importance than reliability as opposed to slightly less importance, than HDI becomes just about equal in rating to VCOS. As more weight is given to cost, e.g., it were to become more important or much more important than reliability in the model, the ratings of the two alternatives stay virtually the same.

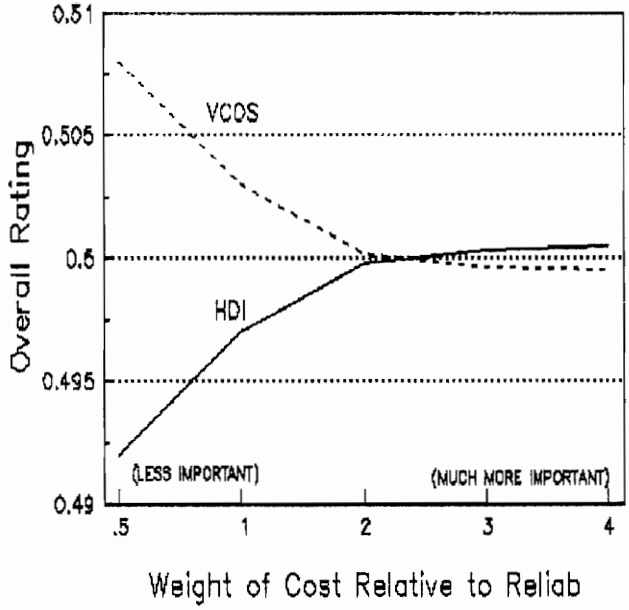

FIGURE 12. SENSITIVITY ANALYSIS FOR COST RELATIVE TO RELIABILITY FOR LEVEL II COMPARISIONS

6.0 Conclusions

The high density, multichip module industry has shown tremendous growth in recent years. As a result, many different designs have been produced, offering many different alternatives for use in high performance computing systems.

This paper reviewed many of the key processes and materials that are important in the MCM industry today in the industry, and identified some key products that are competing for business in both the commercial and military markets. The trends of multichip module

packaging were reported as well as the outlook for developments in the future.

The results of the initial AHP model, based on the values and the weights provided, show that VCOS chip interconnection is the preferred high density interconnect technology over HDI. The performance characteristics of HDI are arguably better, but the more stable, mature and better defined processes of VCOS give it the advantage at this point.

Sensitivity analysis can reveal how this outcome may change, when key attributes are weighted higher or lower or certain cost or performance values are improved. It can be concluded from the sensitivity analysis that improving the reliability and reducing the rework cost of HDI technology will improve their case quite a bit. In addition, if the mission scenario for the multichip module placed more emphasis on performance, than HDI would gain additional advantage. An example of this would be if the processing speeds were required to be at the Ghz level from the start, as opposed to achieving those in future upgrades. This would have justified additional weight being applied to the performance attribute, clearing the way for HDI to be the potential technology of choice.

7.0 Further Research Potential

A comparison of the alternatives of multichip module packaging designs using the general background information provided here would not be sufficient for a real world analysis. The cost data supplied here

for the MCM's is derived from costs associated from low volume, military specific applications, where costs are currently in the 10-15K range per module [7]. It is assumed that higher volumes and production efficiencies will reduce those costs to below 5K. In addition, detailed cost data from all areas of the life cycle analysis such as R&D, manufacturing, and O&M are needed to make truly accurate comparisons.

The AHP model presented here, though, still provides a good framework to begin the analysis. The model can always be enhanced by adding new attributes or substituting new performance data into the comparisons.

Trade-off studies beyond the scope of this paper could be considered to further analyze high density, multichip module applications. A good example is the trade-off between the limitations of the single chip module and the point where MCM's take over; a study could determine exactly where the cut off point would occur.

8.0 Bibliography

1. Blanchard, B.S., and Fabrycky, W.J., Systems Engineering and Analysis, Prentice Hall, 1990.

2. Bowman, et.al., Practical VLSI Fabrication For the 90's, Integrated Circuit Engineering Corporation, Scottsdale AZ, 1990.

3. Canada, J.R., and Sullivan, W.G., Economic and Multiattribute Evaluation of Advanced Manufacturing Systems, Prentice Hall, 1989.

4. Gdula, M., et.al., "A 36-Chip Multiprocessor Multichip Module Made With the General Electric High Density Interconnect Technology," Electronic Components and Technology Conference, May, 1991.

5. Grau, P.F., "Use of the Analytic Hierarchy Process In Choosing Computer Aided Design Tools," Virginia Tech ISE 5434 Term Paper, December, 1992.

6. IBM FSC Internal Report on the High Density Hermetic Card, June, 1992.

7. IBM FSC Technical Report, "A Critical Analysis of High Density Interconnect MCM's," No. 93-IBM-01, June, 1993.

8. Liu, Y.S., "Laser Metal Deposition For High-Density Interconnect," Optics and Photonics News, June, 1992.

9. Maliniak, David, "Future Packaging Depends Heavily on Materials," Electronic Design, January, 1992, pp. 88-97.

10. Ozmat, Burhan, "Interconnect Technologies and the Thermal Performance of MCM," IEEE Transactions on Components, Hybrids, and Manufacturing Technology, Vol.15, No.5, October, 1992.

11. Panicker, M.P.R., and Salinas-simons, F., "Thin Film Copper: Polyimide Multichip Modules on Microsubstrates," Surface Mount International Conference and Exposition, August, 1991.

12. Sabatini, J.E., "MCM Design Using High-Density Packaging," Surface Mount Technology, March, 1992.

13. Vardaman, E. Jan, and Ng, Lee H., "A Cost/Performance Analysis of Multichip Module Interconnects," ISHM Proceedings, 1991, pp. 27-32.

9.0 Appendix A

AHP Calculations For Chip Interconnect Model

The first step in the analysis is to compare the relative importance of the 5 main attributes, known as Level II. The question is asked, "How many times more important is attribute A (reliability) relative to attribute B (manufacturing cost)?" The comparison data is listed in the matrix in Table A1.

Only the values to the top right of the diagonal need to be identified, since the other values are simply the reverse comparisons of the same pairs. The bottom left values from the diagonal become the inverse values of those to the top left of the diagonal. The values are then normalized and averaged across the rows, also shown in the second section of the Table A1.

Table A1: Level II Comparisons

	Cost	Perf	Reliab	Rew	Risk	
Cost	1.000	0.333	0.500	3.000	4.000	
Perf	3.000	1.000	1.000	4.000	4.000	
Reliab	2.000	1.000	1.000	4.000	3.000	
Rew	0.333	0.250	0.250	1.000	2.000	
Risk	0.250	0.250	0.333	0.500	1.000	
			Normalized			Avg
Cost	0.152	0.118	0.162	0.240	0.286	0.191
Perf	0.456	0.353	0.324	0.320	0.286	0.348
Reliab	0.304	0.353	0.324	0.320	0.214	0.303
Rew	0.051	0.088	0.081	0.080	0.143	0.089
Risk	0.038	0.088	0.108	0.040	0.071	0.069

At the Level III analysis, the sub-attributes under Manuf. $ and Performance are weighted relative to one another in the same manner as was depicted in level II, and are shown in Table A2 and Table A3.

Table A2. Cost Attributes

	Prod$	Rew$	
Prod$	1.000	2.000	
Rew$	0.500	1.000	
	Normalized		Avg
Prod$	0.667	0.667	0.667
Rew$	0.333	0.333	0.333

Table A3. Performance Attributes

	Res	Ind	Cap	Therm	
Res	1.000	1.000	1.000	1.000	
Ind	1.000	1.000	1.000	1.000	
Cap	1.000	1.000	1.000	1.000	
Therm	1.000	1.000	1.000	1.000	
	Normalized				Avg
Res	0.250	0.250	0.250	0.250	0.250
Ind	0.250	0.250	0.250	0.250	0.250
Cap	0.250	0.250	0.250	0.250	0.250
Therm	0.250	0.250	0.250	0.250	0.250

Level IV next analyzes the two alternatives, HDI and VCOS, with respect to each of the five main attributes. Performance data is used to compare the attributes of reliability in Table A4. Weighted values are used to compare rework and risk, which are shown in Table A5 and A6.

Table A4. Alternative Comparisons With Respect to Reliability

	HOURS
HDI	50000
VCOS	85000
	Normalized
HDI	0.370
VCOS	0.630

Table A5. Alternative Comparisons With Respect to Rework

	HDI	VCOS	
HDI	1.000	0.250	
VCOS	4.000	1.000	
	Normalized		Avg
HDI	0.200	0.200	0.200
VCOS	0.800	0.800	0.800

Table A6. Alternative Comparisons With Respect to Risk

	HDI	VCOS	
HDI	1.000	0.333	
VCOS	3.000	1.000	
	Normalized		Avg
HDI	0.250	0.250	0.250
VCOS	0.750	0.750	0.750

Performance and cost data is used in the matrix arithmetic instead of fractional weights for the attributes of performance and manufacturing cost. The actual values are normalized and averaged in the same fashion as the weighted fractions. The results are given in Table A7 and Table A8.

Table A7. Comparison of Alternatives With Respect to Performance

	Res	Ind	Cap	Therm	
	0.250	0.250	0.250	0.250	
HDI	2.000	0.010	0.001	10.38	
VCOS	1.000	0.080	0.008	13.10	
	Normalized				Avg wrt Weights
HDI	0.667	0.889	0.889	0.558	0.751
VCOS	0.333	0.111	0.111	0.442	0.249

Table A8. Comparison of Alternatives With Respect to Cost ($)

	Prod$	Rew$	
	0.667	0.333	
HDI	3500	3000	
VCOS	4000	1000	
	Normalized		Avg wrt weights
HDI	0.533	0.250	0.439
VCOS	0.467	0.750	0.561

The final ranking of each alternative is determined by taking the averages from each of the comparison matrices, normalizing them with

respect to the weighted values of each of the attributes and averaging all values for each alternative. The final ranking results are shown in Table A9.

Table A9. Final Ranking of Alternatives

	Cost	Perf	Reliab	Rework	Risk	
	0.191	0.348	0.303	0.089	0.069	
						RANK
HDI	0.439	0.751	0.370	0.200	0.250	0.492
VCOS	0.561	0.249	0.630	0.800	0.750	0.508