NOVEL ZERO-VOLTAGE SWITCHING TECHNIQUES FOR
PULSE-WIDTH-MODULATED CONVERTERS

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Thesis submitted to the Faculty of the Virginia
Polytechnic Institute and State University in partial
fulfillment of the requirements for the degree of

MASTER OF SCIENCE

in
Electrical Engineering

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May 28, 1991

Blacksburg, Virginia
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(ABSTRACT)

Two new classes of soft switching pulse-width-modulated (PWM) converters, named zero-voltage-switched (ZVS) PWM converters and zero-voltage-transition (ZVT) PWM converters, are proposed.

The proposed ZVS-PWM converters combine the merits of conventional PWM and ZVS-QRC techniques. They are capable of regulating the output for a wide load and input voltage range while maintaining constant-frequency operation. By employing a saturable inductor, the load range under which ZVS is maintained can be significantly extended without increasing the voltage stress of the power switch. The parasitic oscillations between the diode junction capacitance and the resonant inductor are also significantly reduced.

In the new class of ZVT-PWM converters, both the power switch and the rectifier diode are operated with zero-voltage switching, and are subjected to low voltage and current stresses associated with those in their PWM counterparts. Thus switching losses are significantly reduced at a slight increase in conduction losses. In addition, the circuit optimization is simplified because of constant-frequency operation.

The operation principles of the proposed converters are described by using several examples. Several breadboarded converters are implemented to verify the theoretical analysis and to demonstrate the feasibility of the proposed technologies.
Acknowledgements

I would like to express my sincere appreciation to my advisor, Dr. Fred C. Lee, for his guidance and support throughout the course of this work. I also wish to thank Dr. Milan M. Jovanovic and Dr. Dan Chen for their contributions as members of my committee and for their suggestions regarding the final manuscript.

It has been a pleasure to associate with the excellent faculty, staff, and graduate students at the Virginia Power Electronics Center (VPEC). I thank all of them for their friendship which has made my stay in VPEC enjoyable.

I am also sincerely grateful to Prof. Shipeng Huang for his guidance during my early days in the area of power electronics and for imparting some of his vast practical knowledge to me.

Finally, I wish to take this opportunity to thank my parents for their sacrifices they made in bringing me up. Their caring support and encouragement have been a source of my confidence and inspiration to me.
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CHAPTER 1
INTRODUCTION

The continuing domination of "hard-switching" pulse-width-modulated (PWM) topologies in switching converters can be attributed to the circuit simplicity and ease of control. However, in the quest for smaller size and lighter weight power supplies compatible with ever shrinking portable computers, communication equipment, and hand tool, etc, it is necessary to operate the converters at higher frequencies. Using the conventional PWM technique for high-frequency operation, several problems are inherent.

The higher switching frequency results in increased switching losses. The switching losses at turn-on are mainly caused by an abrupt change of the energy stored in the parasitic capacitances of the semiconductors. When the transistor turns on, the energy stored in its output capacitance is dissipated in the device; meantime, the rectifier's junction capacitance is dissipatively charged through the active switch. At turn-off, switching loss is primarily caused by the leakage inductance of the power transformer. As the active switch is turned off, the sharp di/dt across the leakage inductance induces a voltage spike. To limit device voltage stress, dissipative snubbers are usually used.
Using the interleaving technology, the leakage of the transformer can be greatly reduced. However, it is at the penalty of much increased winding capacitances. The energy stored in these winding capacitances will also be dissipated during turn-on of the power switch, causing additional capacitive turn-on loss.

Furthermore, the PWM converters exhibit high dv/dt and di/dt in their operation, which cause excessive EMI. If not adequately characterized and controlled, these EMI noise can easily affect the operation of other equipment. In addition, the control circuit of the converter also suffers from poor noise immunity.

Recently, a number of "soft switching" converter technologies have been proposed to overcome the above-mentioned drawbacks of the conventional PWM technique. They include: the zero-current-switched (ZCS) quasi-resonant converters (QRCs) [1-5], the zero-voltage-switched (ZVS) QRCs [6-11], the ZVS multi-resonant converters (MRCs) [11-20], and the ZVS quasi-square-wave converters (QSCs) [21-24]. The ZCS technique reduces the switching losses by turning on and turning off the transistor at zero-current, while the ZVS technique eliminates the switching losses by turning on and turning off the power switch at zero voltage.

High switching speed, large peak current capability, ease of drive, wide SOA, avalanche and dv/dt capability have made power MOSFETs the logical choice in high-frequency converter designs. Various studies have concluded that zero-voltage switching as opposed to zero-current switching, is preferred for high-frequency conversion where power MOSFETs are used [7,25,26]. The features of several typical zero-voltage switching techniques are reviewed below.

1. INTRODUCTION
A. ZVS-QRC Technique

A ZVS-QRC topology is derived from its PWM counterpart by addition of a resonant capacitor across the active switch and a series resonant inductor. Figure 1.1 shows the circuit diagram and key waveforms of the buck ZVS-QRC. The zero-voltage switching of the power switch is achieved by utilizing the resonance between the resonant inductor \( L_r \) and the resonant capacitor \( C_r \). The advantages and the limitations of the ZVS-QRC technique are summarized as following:

**Advantages**

- the power switch operates with zero-voltage switching; and
- the power switch is subjected to minimum current stress same as in its PWM counterpart.

**Limitations**

- the power switch suffers from an excessive voltage stress which is proportional to the load range;
- the load range is limited;
- the interaction of the rectifier’s junction capacitance with the resonant inductor causes severe parasitic oscillations, which may result in an instability in the closed-loop system; and
- the variable frequency operation makes circuit optimization difficult to achieve.

1. INTRODUCTION
Fig. 1.1. Circuit diagram and key waveforms of the buck ZVS-QRC.
B. ZVS-MRC Technique

ZVS-MRCs can be generated from PWM topologies by replacing the PWM switch with the multi-resonant switch [12]. The multi-resonant network absorbs all major parasitic components, including transistor output capacitance, diode junction capacitance, and transformer leakage inductance into the resonant circuit. Figure 1.2 gives the circuit diagram and typical waveforms of the buck ZVS-MRC converter. Its operation is fully described in [12]. The key features of the ZVS-MRCs are summarized in the following:

**Advantages**

- both the transistor and rectifier operate with zero-voltage switching, reducing switching losses and noise;
- all essential parasitic reactances of the power circuit are absorbed and utilized in a controlled manner;
- zero-voltage-switching operation can be maintained for full load range; and
- much reduced EMI.

**Limitations**

- both switches suffer from voltage and current stresses much higher than those in the PWM counterparts, thus conduction losses are increased while switching losses are reduced;
- a relatively large resonant inductor is required, causing additional core loss and copper loss, and offsetting the reduction of size in high-frequency operation; and
- variable frequency operation.
Fig. 1.2. Circuit diagram and typical waveforms of the buck ZVS-MRC.
Similar to the ZVS-QRCs, the ZVS-MRCs require constant off-time control. When operated with a wide input and load range, they have to modulate their switching frequency over a wide range. As a result, the optimum design of the power stage is difficult to achieve. Constant-frequency operation can be achieved by replacing the passive switch in a ZVS-MRC with an active switch [20-21]. The main disadvantage of the constant-frequency MRCs is the increased circulating energy. The circuit efficiency is reduced especially at light load.

C. ZVS-QSC Technique

The zero-voltage switching in a ZVS-QSC is achieved by utilizing the resonance between the filter inductor and the resonant capacitor [21-24]. The circuit diagram and key waveforms of the buck ZVS-QRC are shown in Fig. 1.3 [22]. The operation of the ZVS-QSCs is somewhat similar to the PWM converters operating in the discontinuous-current mode. The merits and limitations of the ZVS-QSCs are summarized as following:

**Advantages**

- both the transistor and the rectifier operate with zero-voltage switching; and

- both switches are subjected to minimum voltage stress same as in their PWM counterparts.

**Limitations**

- the switches suffer from high peak current more than twice that in the PWM counterpart;

- a large filter capacitor is needed due to high ac current through the filter inductor;
Fig. 1.3. Circuit diagram and key waveforms of the buck ZVS-QSC.
the conversion ratio for zero-voltage switching is limited (e.g., \( V_o > 0.5 \) \( V_i \) for buck converter); and

- variable frequency operation -- variable \( T_{ON} \) and variable \( T_{OFF} \) control.

Constant-frequency operation of the ZVS-QSCs can also be achieved by replacing the passive switch with an active switch. As a result, last two limitations mentioned above are eliminated.

Generally speaking, the primary objective in selecting these "soft switching" converters is to alleviate device switching losses. Other advantages inherent with these soft switching technologies include low \( dv/dt \) or \( di/dt \) stresses, low EMI, and a good transient response. The choice of a "soft switching" topology usually invokes substantial penalties in terms of higher VA ratings of the switches and the reactive elements, which result in significantly higher conduction losses of the switches and the copper loss of the power transformer. Therefore, a more desirable converter topology would be one which combines the desired features of both resonant converters and the PWM converters, including low switching losses, low voltage and current stresses of the devices, and constant-frequency operation. One successful example is the well-known full-bridge (FB) ZVS-PWM converter [26-30]. It combines the advantages of the conventional FB-PWM converter and the FB-ZVS-QRC while avoiding their respective limitations [31].

This thesis presents two families of new "soft switching" converter topologies, in an attempt to achieve the best features of the resonant converters and PWM converters. In Chapter 2, a new class of ZVS-PWM converters is proposed. The new converters combine the merits of the conventional PWM and the ZVS-QRC techniques. It is shown that the FB-ZVS-PWM converter is simply a member of this family of converters. It is

1. INTRODUCTION
also shown that the performance of the new converters can be further improved by using a saturable inductor. Chapter 3 presents a novel zero-voltage-transition (ZVT) PWM technique which leads to the creation of a new family of ZVT-PWM converters. The proposed ZVT-PWM technique minimizes the switching losses and conduction losses. Conclusions of this research endeavor are presented in Chapter 4.
CHAPTER 2
A NEW FAMILY OF ZERO-VOLTAGE-SWITCHED PWM CONVERTERS

2.1 INTRODUCTION

The ZVS-QRC technique eliminates the capacitive turn-on loss which plagues ZCS-QRCs and PWM converters [7, 11]. The drain-to-source voltage of the power MOSFET in ZVS-QRCs is shaped to zero prior to turn on, thus eliminating energy dissipation, noise, and the Miller effect. In addition, the active switch in a ZVS-QRC is subjected to relatively low current stress and hence is preferable over that of the ZCS-QRC technique for high-frequency conversion where MOSFETs are employed.

However, the ZVS-QRC technique has its limitations. First, the power switch in a single-ended ZVS-QRC suffers from excessive voltage stress which is proportional to the load range. Using the buck ZVS-QRC as an example, for a 10% to 100% load range, the peak voltage stress of the power switch can be 11 times the input voltage.
Therefore, a high voltage MOSFET accompanied with high on-resistance and large input capacitance has to be used, thus results in a substantial increase of the conduction loss and the gate driver loss. Second, a wide switching frequency range is required for a ZVS-QRC to operate with a wide input voltage and load range. The wide frequency range makes optimization of the power transformer, input/output filters, control circuit, and power switch drive circuit difficult. For example, to decrease conduction loss, power MOSFETs with low on-resistances are preferred. However, MOSFETs with low on-resistance are accompanied by large input capacitances, which can cause significant driver loss at high-frequency operation, especially at high line and light load [10, 11].

Another limitation of the ZVS-QRC technique is the parasitic ringing between the resonant inductor and the diode junction capacitance. The parasitic ringing results in an increase of the switching noise and possible instability in the closed-loop system [6].

The voltage stress of the power switch in a ZVS-QRC can be reduced at the expense of a partial loss of ZVS at light load. This does not cause a thermal problem since the switch conduction loss is very low at light load. In addition, with partial voltage applied, the capacitive turn-on loss is relatively low compared to that of a PWM converter or a ZCS-QRC. However, if an external capacitor is added to the FET output capacitance, the partial loss of the ZVS at light load can be intolerable [10, 11]. With a wide load range, optimization of ZVS-QRCs is difficult to achieve.

This chapter presents a new class of ZVS-PWM converters. Employing an auxiliary switch across the resonant inductor in a ZVS-QRC, it allows the new converter to operate with a constant frequency and makes circuit optimization easily attainable. This chapter also shows that the use of a saturable inductor can further improve the performance of the proposed ZVS-PWM converters.

2. A NEW FAMILY OF ZVS-PWM CONVERTERS
2.2 A FAMILY OF ZVS-PWM CONVERTERS

2.2.1. ZVS-PWM Switch

Figure 2.1(a) shows the basic configuration of the ZVS quasi-resonant switch, which represents the sub-circuit extracted from ZVS-QRCs by shorting voltage sources and filter capacitors and opening filter inductors [21]. To achieve zero-voltage switching, the off-time of the power switch is fixed. The output voltage is regulated by varying the on-time of the switch. By adding an auxiliary switch (S1) across the resonant inductor, the ZVS-PWM switch shown in Fig 2.1(b) is obtained. This auxiliary switch makes the off-time of the power switch (S1) controllable. It enables the converter to regulate the output while operating at a fixed switching frequency.

In the ZVS quasi-resonant switch, the resonant inductor begins to oscillate with the resonant capacitor soon after the power switch is turned off. The power switch (S) is turned on with zero-voltage switching after the resonance brings the voltage across C or S to zero. The off-time of the power switch is determined by the resonant period of the resonant components. Thus a ZVS-QRC operates with constant off-time control. Consequently, a ZVS-QRC operating with a wide input voltage or load range has a wide frequency range.

In Fig. 2.1(b), S1 is turned on before the power switch is turned off. When the power switch is turned off, the resonant inductor current continues to flow through S1 for a period of time, during which the energy stored in the resonant inductor remains
Fig. 2.1. Equivalent circuits of: (a) ZVS quasi-resonant switch, and (b) ZVS-PWM switch.
unchanged until \( S1 \) is turned off, where the resonant inductor begins to oscillate with resonant capacitor. The power switch is turned on after the resonance brings the capacitor voltage to zero. By controlling the time interval of the freewheeling stage, the off-time of the power switch can be varied, enabling the converter to operate with a fixed frequency.

To introduce the operation principle of the ZVS-PWM converters, the buck ZVS-PWM converter is used as an example. The circuit schematic and key waveforms of the buck ZVS-PWM converter are shown in Fig. 2.2. The new circuit differs from a buck ZVS-QRC by using an auxiliary switch in parallel with the resonant inductor. The output filter inductor is considered as a current source in the analysis. As shown in Fig. 2.3, five topological stages exist within one switching cycle:

1. \( T_0-T_1 \): The active switch \( S \) is turned off at \( T_0 \). The freewheeling diode \( D \) is off, and the resonant inductor current remains at \( I_0 \) value during this interval. The resonant capacitor (\( C_r \)) is charged linearly until its voltage reaches the input voltage. The equivalent circuit of this topological stage is shown in Fig. 2.3(a).

2. \( T_1-T_2 \): At time \( T_1 \), \( D \) is turned on, starting the freewheeling interval. The \( L_r \) current still remains constant by circulating through the auxiliary switch \( S1 \). Therefore the energy stored in the resonant inductor (which is used to achieve ZVS for \( S \)) stays unchanged.

3. \( T_2-T_3 \): At time \( T_2 \), \( S1 \) is turned off, and the resonance between \( L_r \) and \( C_r \) begins. This interval lasts until \( T_3 \), when the voltage applied to \( S \) (or \( C_r \)) is forced to zero by the conduction of the anti-parallel diode.

4. \( T_3-T_4 \): \( S \) is turned on with ZVS during this time interval. The \( L_r \) current increases linearly while the diode \( D \) current decreases. At \( T_4 \), diode \( D \) is turned off with ZCS.
Fig. 2.2. Buck ZVS-PWM converter and its key waveforms.
Fig. 2.3. Equivalent circuits for five operation stages.
(5) \( T_4-T_6 \): S1 is turned on with ZVS before S is turned off. This interval lasts until \( T_0 \), when S is turned off, and the cycle is repeated.

Compared to the buck ZVS-QRC, this converter possesses an extra freewheeling stage \((T_1-T_2)\), during which the resonant inductor current flows through S1 and remains constant. Constant-frequency operation is achieved by controlling this freewheeling time interval \((T_1-T_2)\). Furthermore, the resonant interval \((T_2-T_3)\) can be relatively short with respect to the switching period. This feature makes operation of the proposed circuit similar to that of the conventional PWM converter for most portions of the cycle.

The circuit design strategy for the proposed buck ZVS-PWM converter is quite different from that of the buck ZVS-QRC. To limit the switch voltage stress, the circuit can be designed to lose ZVS property at about 50% load. Thus the maximum voltage stress of the active switch is approximately three times the input voltage at full load. At light load, ZVS is partially lost. This does not cause a thermal problem since the conduction loss is low at light load. Furthermore, due to the low switching current and the constant frequency operation, this switching loss is not significant. At very light load, the operation of the proposed circuit is similar to that of a conventional PWM buck converter.

When the resonant frequency of the buck ZVS-PWM converter is designed to be much higher than the switching frequency, the parasitic ringing across the rectifier becomes less pronounced. The high frequency ringing can be easily suppressed. In addition, due to the constant frequency operation, snubber loss is constant with changes in load current. The buck ZVS-PWM converter presents a significant improvement over the ZVS-QRC counterpart.
2.2.2. Basic ZVS-PWM Topologies

A ZVS-PWM converter can either be derived from a conventional PWM converter or a ZVS-QRC. By simply adding an auxiliary switch across the resonant inductor in ZVS-QRCs, the new class of ZVS-PWM converters is generated.

The procedure for converting a PWM topology into a ZVS-PWM topology is also straightforward. To derive a ZVS-PWM converter from a PWM converter, the following steps are followed:

1. A resonant capacitor is added in parallel with the power switch.
2. A resonant inductor is inserted in the loop containing the power switch and the diode.
3. An auxiliary switch is placed in parallel with the resonant inductor.

The above steps should only be viewed as a simple way of describing the relative positions of the resonant components. In fact, there exist several topological variations for each basic ZVS-PWM converter, which can be identified by using the capacitor- and inductor-shift rules [32]. This issue is essentially identical to that found in ZVS-QRCs. The shifting of a resonant component results a different dc bias applied to that component, but does not affect the basic operation of the circuit.

The six basic ZVS-PWM converter topologies, buck, boost, buck-boost, Cuk, Sepic, and Zeta, are shown in Fig. 2.4. Since the auxiliary switch is in parallel with the resonant inductor, it has to be a voltage-bidirectional switch, which can be implemented by a MOSFET in series with a reverse-voltage blocking diode.
Fig. 2.4. Six basic ZVS-PWM converter topologies:

(a) buck, (b) boost, (c) buck-boost,
(d) Cuk, (e) Sepic, and (f) Zeta.
2.2.3 ZVS-PWM Topologies with Isolation Transformer

By simply adding an auxiliary switch across the resonant inductor in each isolated ZVS-QRC topology, the isolated ZVS-PWM converters are generated. Figure 2.5 shows several basic ZVS-PWM converter topologies with isolation transformers.

Two interesting isolated topologies generated by using the ZVS-PWM switch are the full-bridge (FB) and half-bridge (HB) ZVS-PWM converters, as shown in Fig. 2.5 (c) and (d). Since the maximum voltage stress of the primary switches in these two converters is clamped to the input voltage, they are particularly useful for off-line applications.

The operation of the FB-ZVS-PWM converter is fully described in [26-29]. The configuration of this converter is identical to that of the FB-ZVS-QRC. However, its operation differs from the latter by applying phase-shift control [33], which essentially creates an extra freewheeling operation stage during which the resonant inductor current circulates through the upper or lower two switches. During the freewheeling time, the voltage across the transformer primary or secondary is zero; and the resonant inductor current is circulating through the upper or lower half of the bridge. Thus the equivalent circuit during this operation stage is identical to that with an auxiliary switch employed across the resonant inductor. Consequently, no auxiliary switch is needed in this particular topology.

The HB-ZVS-PWM converter combines the merits of the conventional HB-PWM converter and the HB-ZVS-QRC. The use of the auxiliary switch introduces an additional freewheeling stage within the operation of the HB-ZVS-QRC. Constant-frequency operation is achieved by controlling this freewheeling time interval. Since the
Fig. 2.5. Several topologies of the isolated ZVS-PWM converters:
(a) forward, (b) flyback,
(c) full-bridge, and (d) half-bridge.
transformer leakage and the output capacitances of the MOSFETs are utilized to achieve ZVS, switching losses are significantly reduced at a limited increase of conduction loss. The auxiliary switch (S3) also operates with ZVS and is subjected to a voltage stress of only half of the input voltage. The auxiliary switch must be a bidirectional switch. It can be implemented by either two anti-parallel MOSFETs or a bridge-type switch consisting of one MOSFET and four diodes. The HB-ZVS-PWM converter can be well used for low-to-mid power conversion applications.

The operation and the key waveforms of the HB-ZVS-PWM converter are similar to those of the FB-ZVS-PWM converter. The major difference is that during the freewheeling time, the resonant inductor current in the HB converter circulates through the auxiliary switch instead of flowing through the upper or lower two switches as is the case in the phase-shift controlled FB-ZVS-PWM converter.

2.2.4 Experimental Verifications

A 1 MHz, 100 W buck ZVS-PWM converter has been breadboarded to verify the operation of the buck ZVS-PWM converter. The circuit regulates at 24 V output with a 48 V input. Figure 2.6 shows the circuit diagram of the breadboarded converter. The FET output capacitance ($C_{oss}=650$ pf at $V_{ds}=25$ V) is used as the resonant capacitor ($C_r$). The control circuit is implemented by a PWM controller, UC 3823. It is simple compared to the control circuit of the buck ZVS-QRC. Power MOSFET S is driven by a fast driver, TSC 429.
Fig. 2.6. Circuit diagram of the experimental 1 MHz, 100 W buck ZVS-PWM converter.
Fig. 2.7. Experimental waveforms of the buck ZVS-PWM converter at: 
(a) full load, (b) half load, and (c) 25% load. 
1st waveform: $V_{GS}$, 20 V/div; 
2nd waveform: $V_{GS1}$, 20 V/div; 
3rd waveform: $V_{DS}$, 50 V/div; 
4th waveform: $V_D$, 50 V/div; 
5th waveform: $I_L$, 5 A/div; 
Time scale: 200 ns/div.
The converter in Fig. 2.6 is designed to ensure ZVS operation above 50% load; thus the maximum voltage stress of the power switch is approximately three times the input voltage. Figure 2.7 shows the oscillograms of the circuit operating at full load, half load, and 25% load. It can be seen that the ZVS operation is maintained at half load. At 25% load, the power switch is turned on with half of the input voltage, and ZVS is partially lost; the capacitive turn-on loss is approximately a quarter of that in a buck PWM converter. At very light load, the operation of the converter is similar to the buck PWM converter.
2.3 IMPROVEMENT OF THE ZVS-PWM CONVERTERS

2.3.1 ZVS-PWM Converters Using a Saturable Inductor

The power switch in single-ended ZVS-QRCs suffers from an excessive voltage stress proportional to the load range, this is one of the major limitations of the ZVS-QRC technique. For instance, the maximum voltage stress of the active switch in the buck ZVS-QRC is [10]:

\[ V_{DS_{\max}} = \left( 1 + \frac{R_{L_{\max}}}{R_{L_{\min}}} \right) V_{\max}. \]  \ (2.1)

The maximum voltage stress of the power switch in a single-ended ZVS-QRC is proportional to the load range. The voltage applied to the active switch or the resonant capacitor reaches its maximum value as the resonant inductor reaches zero current, that is, when the inductor energy is completely transferred to the resonant capacitor. Thus this maximum voltage stress is essentially determined by the energy stored in the resonant inductor.

Consider the case when a saturable inductor is used as the resonant inductor. The B-H characteristics of a linear inductor and a saturable inductor are shown in Fig. 2.8. For the saturable inductor, its inductance becomes zero when the inductor current exceeds the critical saturation current, I_c. The energy stored in a inductor is determined
Fig. 2.8. B-H characteristics of a saturable inductor and a linear inductor.
by the integral of the H field over the flux density, i.e.:

$$E = \int H dB.$$  \hspace{1cm} (2.2)

For a linear inductor, this energy is $\frac{1}{2}L_JI^2$. Therefore, for a ZVS-QRC with a linear resonant inductor, the amount of the circulating energy (stored in the resonant inductor) is dependent on the load current. To achieve zero-voltage switching under given load range, the amount of the energy stored in the resonant inductor at minimum load has to be sufficient to discharged the energy stored in the resonant capacitor. Therefore, the wider the load range, the higher the circulating energy, and the higher the voltage stress of the transistor. The maximum energy stored in a saturable inductor is $\frac{1}{2}L_{ssat}I^2$, which is not dependent on the inductor current after it saturates. Therefore, if a saturable inductor is used in a ZVS-QRC, the maximum circulating energy will be limited by the saturation inductor energy. If the saturable inductor is designed to saturate at minimum load, the energy stored in the inductor remains constant as the load current increase (as shown in Fig. 2.8). Consequently, with a saturable inductor is employed, a ZVS-QRC can achieve a much wider ZVS load range without further increasing the voltage stress of the power switch [34].

If the linear inductor is replaced by a saturable inductor in a ZVS-PWM converter, the situation will be similar. The operation of the improved converters is illustrated by using the buck converter shown in Fig. 2.9. The operation of this circuit is slightly different from that in Fig. 2.2 during time $T_0$ to $T_4$. When S is turned off at $T_0$, the inductor
Fig. 2.9. Buck ZVS-PWM converter using a saturable resonant inductor and its key waveforms.
current decreases very quickly, until the inductor gets out of saturation. The inductor energy \((\frac{1}{2}L_iJ_c^2)\) remains unchanged until \(T_2\), where \(S1\) is turned off, and the inductor \(L_r\) starts to resonate with the capacitor \(C_r\). When the resonant inductor reaches zero current (where its energy is completely transferred to \(C_r\)), the power switch reaches its maximum voltage, \(V_{DS\text{Max}}\):

\[
V_{DS\text{Max}} = V_i + \sqrt{\frac{L_{ro}}{C_r}}I_c.
\] (2.3)

To ensure the zero-voltage turn-on of the power switch at \(T_3\), the inductor energy has to be large enough to discharge \(C_r\) to zero voltage, i.e.:

\[
\frac{1}{2}L_{ro}J_c^2 \geq \frac{1}{2}C_rV_i^2.
\] (2.4)

Equations (2) and (3) imply that to achieve ZVS, the maximum voltage stress of the power switch cannot be less than twice the input voltage. However, since the energy stored in the saturable inductor is constant, the maximum voltage stress of the power switch is load independent. Therefore, a wider ZVS load range can be achieved without increasing the voltage stress of the power switch. Theoretically, if the inductor in a buck ZVS-PWM converter is designed to have a critical current \(I_c\) equal to one-fifth of the maximum load current, the converter will operate with 20% load to full load ZVS range, while keeping the peak voltage stress as low as twice the input voltage.

2. A NEW FAMILY OF ZVS-PWM CONVERTERS
During the interval \( T_3-T_4 \), the inductor current increases linearly until it reaches \( I_c \) at \( T_4 \), when the inductor saturates, and its current rises abruptly to \( I_e \). Meanwhile, the voltage across the diode also rises abruptly to \( V_d \), causing parasitic ringing between the diode junction capacitance and the resonant inductor. With a saturable inductor, this parasitic ringing is less severe, since the inductance is drastically reduced after the core is saturated. Another benefit of using a saturable inductor is the reduced conduction loss in \( S1 \). Due to the low conduction current (\( I_c \)) during the freewheeling time (\( T_1-T_2 \)) when \( S1 \) is on, a small auxiliary switch can be used.

By simply replacing the resonant inductor in a ZVS-PWM converter by a saturable inductor, the improved ZVS-PWM converters are derived. Several topologies of the ZVS-PWM converters using a saturable inductor are illustrated in Fig. 2.10. The advantages of the improved converters can be summarized as following:

- wider load range can be achieved with ZVS without increasing the circulating energy;
- the parasitic ringing between the resonant inductor and the rectifier junction capacitance is significantly reduced;
- conduction loss of the auxiliary switch is reduced.

For the single-ended topologies shown in Fig. 2.10(a)-(c), the first merit implies that the converter can achieve a wider load range with ZVS without significantly increasing the voltage stress of the active switch. For the HB or FB topologies, however, the maximum voltage stress of the active switches is automatically clamped to the input voltage. In this case, the use of a saturable inductor reduces the circulating energy.
Fig. 2.10. Several topologies of the ZVS-PWM converters with a saturable inductor:
(a) buck, (b) boost, (c) buckboost, (d) full-bridge, and (e) half-bridge.
by increasing the effective duty cycle, which leads to a reduction in the current stress of the primary switches and in the voltage stress of the secondary rectifiers. A detailed analysis of the FB-ZVS-PWM converter using a saturable inductor will be given in the following section.

One design consideration of the ZVS-PWM converters using a saturable inductor is the high core loss due to the large flux change and high-frequency operation. However, the size of the saturable core in this case is rather small since the magnetic material with very high permeability can be employed, thus the total core loss is still limited.

2.3.2. FB-ZVS-PWM Converter Using a Saturable Inductor

The FB converter topology is widely used for mid- and high-power conversion since the switches are subjected to relatively low voltage and current stresses. Among a number of recently developed converter technologies, the FB-ZVS-PWM converter technique is deemed most desirable for many applications [26-30] since it combines the benefits of both the ZVS-QRC and PWM techniques while avoiding their major drawbacks. It utilizes the leakage inductance of the power transformer and the parasitic capacitances of the MOSFETs to achieve ZVS for the power switches. As a result, switching losses are significantly reduced. Furthermore, the converter operates with a fixed frequency, enabling the design optimization of the circuit easily attainable.

However, due to the requirement of a relatively large resonant inductor, the FB-ZVS-PWM converter operates with high circulating energy, which substantially
increases the current stress of the primary switches, voltage stress of the rectifier diodes, and the parasitic oscillations between the resonant inductor and the diode junction capacitances. These are major limitations of the FB-ZVS-PWM converter [35].

Figure 2.11 shows the circuit diagram and the key waveforms of the FB-ZVS-PWM converter. Compared to its PWM counterpart, the FB-ZVS-PWM converter uses a resonant inductor (Lr) to achieve zero-voltage switching of the primary switches. The size of the inductor is determined by the load and input voltage range under which zero-voltage switching is maintained. To reduce the switching losses for a wide load and input voltage range, a large resonant inductance is required. However, a large resonant inductance causes higher circulating energy that significantly increases the conduction loss. Therefore, the load current under which zero-voltage switching is maintained is relatively limited in practical circuits [35, 37].

The amount of the circulating energy is dependent on the loss of duty cycle at the secondary side. From Fig. 2.11, it can be seen that the duty cycle of the secondary-voltage, D_s, is smaller than that of the primary voltage, D. The loss of the duty cycle is caused by the finite time (t_1-t_2) necessary to change the direction of primary current due to the presence of the large resonant inductor. Given input voltage, the loss of duty cycle is determined by the output current and the charging slope (V_l/L_r) of the inductor current. A larger resonant inductance or higher output current leads to a greater loss of duty cycle. The effective duty cycle on the transformer secondary side of the FB-ZVS-PWM converter, D_e, is [29]:
Fig. 2.11. FB-ZVS-PWM converter and its key waveforms.
\[ D_* = \frac{D}{1 + \frac{L C}{N^2 R}} \]  

(2.5)

where \( R \) is the load resistance, \( f_* \) is the switching frequency, and \( N \) is the transformer turns ratio \((N = N_p/N_s)\). On the other hand, the output voltage is dependent on the effective duty cycle:

\[ V_o = \frac{2D_i V_i}{N}. \]  

(2.6)

A larger resonant inductance corresponds to a smaller effective duty cycle, which in turn requires a smaller transformer turns ratio \((N)\) to meet the line conditions. Consequently, the primary current, \( I_p/N \), is increased, leading to higher conduction losses. At the same time, the voltage stress of the secondary diodes, \( 2V_i/N \), is also increased, requiring the use of rectifier diodes with higher voltage rating and higher forward voltage drop.

Another drawback of the FB-ZVS-PWM converter is the severe parasitic ringing between the diode junction capacitances and the resonant inductor, especially for high output voltage. It is more severe than that in the FB-PWM converter since the resonant inductance in the ZVS-PWM converter is considerably larger than the transformer leakage inductance of the conventional PWM converter. The ringing frequency is:

\[ f_r = \frac{N}{2\pi \sqrt{L C}}. \]  

(2.7)
where \( C \) is the equivalent capacitance of the rectifier diodes and the transformer windings. For large value of \( L_r \), the ringing frequency is low, and hence the ringing is difficult to suppress. Thus the diode voltage stress and switching noise are also substantially higher than that of the PWM converter [30,37].

The above-mentioned drawbacks of the FB-ZVS-PWM converter can be alleviated by using a saturable inductor [35,36].

The circuit diagram and the key waveforms of the improved FB-ZVS-PWM converter with a saturable inductor are shown in Fig. 2.12. It should be noted that a power transformer with a minimum leakage inductance is preferred in this case. The operation of the modified circuit is slightly different from that of the previously discussed FB-ZVS-PWM converter. At time \( t_2 \) or \( t_5 \), the inductor current reaches its critical saturation current, \( I_c \), and the inductor is saturated. Then the inductor current rises abruptly until it reaches the reflected filter inductor current, \( I_f/N \), at the same time the secondary voltage also jumps to \( V_f/N \). Consequently, the effective duty cycle of the converter is increased by \( \Delta D_e \), as shown in Fig. 2.12. Assuming an ideal saturable inductor, when switch S1 is turned off at \( t_3 \), the inductor current will decrease quickly until it reaches \( I_c \) and the inductor gets out of saturation. Thus the switch current stress during the freewheeling stage is decreased, and the conduction loss of the primary switches is reduced.

Another benefit of using a saturable inductor is the reduction of parasitic oscillations between the diode junction capacitances and the resonant inductor. When a linear resonant inductor is used, the diode junction capacitances starts to resonate with the
Fig. 2.12. FB-ZVS-PWM converter incorporating a saturable inductor and its key waveforms.
inductor at the $t_2$ and $t_5$, when the diodes suffer from a prompt reverse voltage. The large resonant inductance produces low frequency ringing that increases rectifier voltage stress and switching noise. With a saturable inductor, this parasitic ringing is dramatically reduced, since the resonant inductor gets saturated at time $t_2$ and $t_5$, and its inductance is much reduced before the abrupt voltage is applied to the rectifier diodes. The much reduced inductance results in less ringing with the junction capacitances of the diodes. Since the ringing frequency is significantly higher than the switching frequency, it is easier to snubber.

The advantages of the FB-ZVS-PWM converter incorporating a saturable resonant inductor are summarized as following:

- reduced conduction loss of the switches due to reduced circulating energy;
- increased effective duty cycle resulting in the use of a larger transformer turns ratio to minimize the current in the primary circuit and the voltage in the secondary circuit;
- reduced secondary parasitic ringing and rectifier voltage stresses, so that rectifier diodes with lower voltage rating and lower forward voltage can be used;
- wider load range can be achieved with ZVS without increasing the circulating energy.

The size of the saturable inductor is very small since magnetic material with very high permeability can be employed. Nevertheless, due to a large flux change in the core (from negative saturation area to positive saturation area), the switching frequency range of the converter might be limited to several hundred KHz, which is mainly determined by the thermal tolerance of the core material.
Another way to implement the proposed scheme is to move the resonant inductor from the primary to the secondary, as shown in Fig. 2.13(a). The operation of this converter is identical to that of the FB-ZVS-PWM converter with the saturable inductor in the primary since the secondary inductor can be reflected to primary during each operation stage. It also works for the circuit with a FB rectifier, as shown in Fig. 2.13(b). However, the flux in Lr1 or Lr2 only operates in the first quadrant instead of travelling from negative saturation to positive saturation as was the case in circuit shown in Fig. 2.11; thus the core loss is significantly reduced compared to the circuit operating at the same switching frequency in Fig. 2.11.

2.3.3. Experimental Verifications

A 500 KHz, 100 W buck ZVS-PWM converter using a saturable inductor is implemented to verify the theoretical analysis. The circuit diagram of the breadboarded converter is the same as that in Fig. 2.6, except that the resonant inductor is replaced by a saturable reactor, which is implemented with six turns on a small H7F-ER-9.5/5-Z core.

Figure 2.14 shows the oscillograms of the buck ZVS-PWM converter using a saturable inductor. It can be seen that ZVS is maintained at 15% load. Compare to the buck ZVS-PWM converter operating at the same input and output conditions in Fig 2.6, this converter achieved a much wider ZVS load range. The incorporation of the saturable inductor extends the ZVS load range from 50% load to 15% load without increasing the voltage stress of the power switch.
Fig. 2.13. FB-ZVS-PWM converter using saturable inductors at secondary with:
(a) a half-bridge rectifier, and
(b) a full-bridge rectifier.
Fig. 2.14. Experimental waveforms of the buck ZVS-PWM converter using a saturable inductor at:
(a) full load, (b) half load, and (c) 15% load.
1st waveform: $V_{GS}$, 20 V/div;
2nd waveform: $V_{GSP}$, 20 V/div;
3rd waveform: $V_{DS}$, 50 V/div;
4th waveform: $V_P$, 50 V/div;
5th waveform: $I_{LP}$, 5 A/div;
Time scale: 500 ns/div.
Another 500 KHz, 200 W FB-ZVS-PWM converter using a saturable inductor is also implemented to demonstrate the feasibility of the improved ZVS-PWM converter technique. It is regulated at 5 V output with a 250-350 V input and a 0-40 A load range. The power stage in Fig. 2.12 consists of the following components:

**S1-S4** - IRF740 (International Rectifier);
**DR1,2** - 60CNQ030 (International Rectifier);
**Lf** - core: H7C4-RM7Z52B, 5.5 turns;
**Lr** - core: H7F-ER9.5/5Z, 6 turns;
**TR** - core: half 3F3-782E272 (Philips);
  - primary: 58 turns of 100/44 Litz wire;
  - secondary: 2 turns, center tapped, 3 mil Cu foil;
**Cin** - 0.33 uF / 400 V metal polypropylene;
**Cf** - 4 X 15 uF tantalum & 3 X 0.33 uF ceramic.

The transformer turns ratio was designed at Np/Ns=29 to get 5 V/40 A output with a 0.9 duty cycle at 250 V input. The saturable inductor is implemented with six turns on a small ungapped H7F-ER-9.5/5-Z core. Figure 2.15(a) shows the experimental waveforms of the FB-ZVS-PWM converter using the saturable resonant inductor on the primary side. If a linear resonant inductor were used, the transformer turns ratio would have to be decreased to Np/Ns=24 to get the same output under the same input and duty cycle conditions. This results in a significant increase in the primary conduction loss (about 40%) and rectifier voltage stresses (shown in Fig. 2.15(b)). The increased rectifier voltage stress necessitates the use of a Schottky diode with higher voltage rating and

2. A NEW FAMILY OF ZVS-PWM CONVERTERS
Fig. 2.15. Experimental waveforms of the 500 KHz, 200 W FB-ZVS-PWM converter with:

(a) a saturable resonant inductor, and
(b) a linear resonant inductor

at $V_i=250$ V and $D=0.9$. 
higher forward voltage drop. Here both circuits are designed to maintain zero-voltage switching above 65% load at nominal line (Vi=300 V). In addition, the secondary parasitic ringing in the circuit with a saturable inductor is much less than that with a linear inductor, as can be seen from Fig. 2.15.

To reduce core loss of the saturable reactor and to further extend the load range for zero-voltage switching, another design was attempted with the saturable inductors in the secondary. The converter was designed to maintain ZVS above 45% load at 300 V input. Each saturable inductor was implemented with 1.5 turns on half H7F-ER-9.5/5-Z core. Figure 2.16 gives the overall efficiency of the breadboarded converter. Due to reduced saturable core loss, this circuit has higher efficiency (about 0.8%) over that with the saturable inductor in the primary. Including the control circuit and driver losses, a maximum overall efficiency of 88.6% is achieved.
Fig. 2.16. Overall efficiency of the 500 KHz, 200 W FB-ZVS-PWM converter with the saturable inductors in the secondary.
2.4 SUMMARY

Switching losses, stresses, and noise due to parasitic oscillations are inherent with the PWM technique, and these limitations have restricted the PWM converters from operating at higher frequencies for size/weight reduction and for performance improvement. Although the ZVS-QRC technique has eliminated most of the switching losses and parasitic oscillations associated with the power switch(es), it imposes additional constraints to the power converter circuits, such as high voltage stresses, limited load range, and variable frequency operation. This chapter presents a novel circuit configuration which combines the merits of the PWM and ZVS-QRC techniques. Employing an auxiliary switch across the resonant inductor of a ZVS-QRC, it creates a freewheeling stage within the quasi-resonant operation. The advantages of this additional freewheeling stage are two-fold. First, it enables constant-frequency operation by controlling the time interval of this freewheeling stage. Second, the freewheeling stage could occupy a substantial portion of a cycle so that the proposed circuit resembles that of a conventional PWM converter. Resonant operation takes place only during a small portion of a cycle and is used only to create a ZVS condition for the power switch. In this way, the circulating energy required for ZVS-QRC operation can be significantly reduced. To further enhance the circuit capability of handling a wide load range, a saturable inductor is employed to replace the linear resonant inductor. A 10:1 load range can be obtained while maintaining ZVS for the power switch without significantly increasing its voltage stress.
The detailed operation of the new converters is discussed by using the buck ZVS-PWM converter and the FB-ZVS-PWM converter as the examples. A prototype 1 MHz, 100 W buck ZVS-PWM converter, and a 500 KHz, 100 W buck ZVS-PWM converter employing a saturable inductor are breadboarded to demonstrate the operation of the proposed converters. It is shown that the use of a saturable inductor extends the ZVS range from 50% to 15% load, while limiting the switch voltage stress close to three times the input voltage. In addition, another 500 kHz, 200 W FB-ZVS-PWM converter using a saturable inductor was also implemented to demonstrate the feasibility of the new technique.

The proposed technology can be considered as an extension of the ZVS-QRC technique. Among the large family of the ZVS-PWM converters, the FB-ZVS-PWM converter and the HB-ZVS-PWM converter are deemed most attractive for practical applications, since the power switches are subjected to minimum voltage stress (Vi) as those in their PWM counterparts.
CHAPTER 3

NOVEL ZERO-VOLTAGE-TRANSITION PWM CONVERTERS

3.1 INTRODUCTION

High-frequency high-efficiency operation of dc-dc converters for size and weight reduction requires an substantial reduction of switching losses in traditional pulse-width-modulated (PWM) converters. In recent years, a number of converter topologies have been studied to achieve this goal. Unfortunately, switching losses in these new circuits can only be reduced at the expense of much increased voltage and current stresses of the switches, which lead to a significant increase in conduction loss.

The active switch in a ZVS-QRCs is subjected to relatively low current stress, a desirable feature when a MOSFET is used as the power switch. However, the power switch in a single-ended ZVS-QRC suffers from an excessive voltage stress which is proportional to the load range. Although the active switch operates under favorable
switching condition, operation of ZVS-QRCs is adversely affected by the junction capacitance of the rectifier. Interacting with the large resonant inductor, this parasitic capacitance causes severe switching noise and may result in a possible instability in a closed-loop system.

The ZVS-MRC technique utilizes major parasitics of the power stage. All semiconductor devices in a ZVS-MRC operate with zero-voltage switching, which substantially reduces the switching losses and switching noise. Nevertheless, both active and passive switches in a ZVS-MRC are subjected to high voltage and current stresses, which lead to a significant increase in the conduction loss. The advantage of smaller size of the reactors (the power transformer and filters) due to high-frequency operation is also partially mitigated by the need for a relatively large resonant inductor, whose size is usually comparable to that of the power transformer. This resonant inductor also causes considerably high core loss and copper loss.

The ZVS quasi-square-wave converter (QSC) technique offers zero-voltage switching for both the active and passive switches without sacrificing their voltage stresses. This is a very desirable feature for high-frequency conversion where MOSFETs are used, since power MOSFETs favor the zero-voltage switching operating mode, and their conduction characteristics are strongly dependent on voltage rating. However, the switches in a ZVS-QSC suffer from a high current stress which is greater than twice of that in its PWM counterpart, thus the conduction losses are greatly increased. In addition, the high turn-off current of the switch tends to increase the turn-off loss.
This chapter presents a novel class of zero-voltage-transition (ZVT) PWM converters. By using a resonant network in parallel with the switches, the proposed converters achieve zero-voltage switching for both switches without increasing their voltage and current stresses. The buck ZVT-PWM converter is used as an example to illustrate the operation of the new converters in the following section.
3.2 BUCK ZVT-PWM CONVERTER

The buck ZVT-PWM converter is used to illustrate the operation of the new class of converters. Figure 3.1 shows the circuit diagram and the key waveforms of the buck ZVT-PWM converter. It differs from a buck PWM converter by adding a resonant network consisting of a resonant inductor (Lr), a resonant capacitor (Cr), an auxiliary switch (S1), and a clamp diode (D1). Cd represents the parasitic capacitances of the power switch and the rectifier. By applying the capacitor-shift rule, the parasitic capacitance of the rectifier can be placed across the output capacitance of the power switch. To simplify the analysis, the output filter inductor is considered as a current source. As shown in Fig. 3.2, eight operation stages exist within one switching cycle:

(a) T0-T1: The auxiliary switch S1 is turned on at T0, and the resonance between Lr and Cr begins. The Lr current increases until it reaches Io at T1, where Cd joins the resonance.

(b) T1-T2: Lr current continues to increase. Cd is discharged until it reaches zero voltage at T2, where the anti-parallel diode of S begins to conduct.

(c) T2-T3: The anti-parallel diode of S is on, and S is turned on with zero-voltage switching during this time interval. The voltage across the resonant capacitor decreases until it reaches zero, and the clamp diode D1 is on.

(d) T3-T4: Lr current decreases linearly until it reaches zero at T4. Due to the use of the clamp diode D1, the Cr voltage does not go negative.
Fig. 3.1. Circuit diagram and key waveforms of the buck ZVT-PWM converter.
Fig. 3.2. Equivalent circuits for different operation stages.
(e) T4-T5: The anti-parallel diode of S1 is on. Cr is charged in a resonant fashion until it reaches its maximum voltage (2 Vi) at T5.

(f) T5-T6: S1 and D are off during this interval.

(g) T6-T7: At T6, S is turned off with zero-voltage switching. Cd is charged linearly by the filter inductor current (Io) until it reaches Vi at T7, where the diode is turned on.

(h) T7-T0: This interval is identical to the freewheeling stage of the buck PWM converter. At T0, S1 is turned on again, starting another switching cycle.

It can be seen that the voltage and current waveforms of the switches in the new converter are square-like except during the turn-on and turn-off switching intervals where the zero-voltage resonant transition takes place. The ZVT time T0-T4 and T6-T7 can be very short with respect to the switching cycle, so the operation of the new converter resembles that of the buck PWM converter during most portions of the cycle. Thus both the active and passive switches are zero-voltage switched and are subjected to low voltage and current stresses associated with those in the buck PWM converter. The auxiliary switch (S1) also only handles small transition energy and operates with zero-current switching. Consequently, the switching losses are significantly reduced at a minimized increase of conduction loss.

The zero-voltage switching characteristics of a ZVS-QRC or a ZVS-PWM converter is related to the load current and input voltage. The zero-voltage switching property is usually difficult to maintain at light load since the energy stored in the resonant inductor at light load is not sufficient to discharge the resonant capacitor before the active switch is turned on. The situation is opposite in a ZVT-PWM converter. In the buck ZVT-PWM converter, the FET capacitance (Cd) is discharged by utilizing the

3. NOVEL ZVT-PWM CONVERTERS
energy stored in the resonant network. Before the auxiliary switch is turned on, the resonant capacitor has been charged to $2V_i$, thus this energy is equal to $\frac{1}{2}Cr(2Vi)^2$. A part of energy is used to discharge $Cd$ during the transition time (T0-T4), while the other part is to supply the load current. The amount of the latter portion energy is directly dependent on the output current, and obviously it is less with a lighter load. Consequently, zero-voltage switching property is easier to maintain at light load.

For a ZVS-QRC or a ZVS-PWM converter, it is more difficult to achieve zero-voltage switching at high line. As discussed in Section 2.3.1, to achieve zero-voltage switching, the energy stored in the resonant inductor before turning off the MOSFET has to be large enough to discharge $Cr$. For a fixed load current, the energy stored in the resonant inductor is constant. The amount of the energy needed to discharge $Cr$ ($\frac{1}{2}C_rV_i^2$), however, increases with square of the input voltage. Consequently, the zero-voltage switching property is harder to achieve at high line in a ZVS-QRC or a ZVS-PWM converter. A ZVT-PWM converter is contrary. In the buck ZVT-PWM converter shown in Fig. 3.1, when the input voltage increases, the energy stored in the resonant capacitor is $\frac{1}{2}C_r(2V_i)^2$, which is used to discharge $Cd$, also increases. Thus the zero-voltage switching characteristics of a ZVT-PWM converter are not sensitive to the line change.
3.3 A NEW FAMILY OF ZVT-PWM CONVERTERS

The concept of ZVT as illustrated in the buck ZVT-PWM converter can be extended to any PWM topology. Simply by adding a resonant network (as shown in Fig. 3.1) across the diode in PWM converters, six basic ZVT-PWM converter topologies are derived, as shown in Fig. 3.3.

It has been pointed out that the switches in a ZVT-PWM converter are subjected to low voltage stresses, same as those in its PWM counterpart. This feature can be explained by using the sub-circuit shown in Fig. 3.4(a), which can be extracted from a PWM topology simply by opening the filter inductor(s). In Fig. 3.4(a), S is the active switch with a body diode D_S, D is the rectifier diode, and V_{DC} is a dc voltage source that represents the input/output voltage or the filter capacitor voltage. It is obvious that the maximum voltage across the active switch or the diode can not exceed V_{DC}. Therefore, the switches in any converter containing this sub-circuit suffer from the same voltage stresses as those in its PWM counterpart. A ZVS-QSC or a ZVT-PWM converter contains this sub-circuit, thus the switches are subjected to a higher voltage stress.

Figure 3.4(b) shows another sub-circuit extracted from a ZVS-QRC by opening the filter inductor(s), where L_r is a resonant inductor and C_r is resonant capacitor. Due to the presence of the resonant inductor, the maximum volatge stress of S is not limited to V_{DC} any more. Similarly, a ZVS-PWM converter or a ZVS-MRC also contains such a sub-circuit, thus the power switch is subjected to a voltage stress much higher than that in its PWM counterpart.
Fig. 3.3. Six basic topologies of the ZVT-PWM converters:
(a) buck, (b) boost, (c) buck-boost,
(d) Cuk, (e) Sepic, and (f) Zeta
Fig. 3.4. (a) a sub-circuit extracted from a PWM converter; 
(b) a sub-circuit extracted from a ZVS-QRC converter.
For each basic ZVT-PWM converter, there exists a number of topology variations. Figure 3.5 gives several topology variations of the buck ZVT-PWM converter. The operation principle of these circuits resembles that of the converter in Fig. 3.1, i.e., the auxiliary switch in each circuit is turned on before the active switch is turned on so that the energy stored in the resonant network can discharge \( C_d \) to zero voltage prior to turn-on of the active switch.

Figure 3.6 shows several isolated topologies of the ZVT-PWM converters. Similar to the ZVS-QSC technique, the limitation of the isolated ZVT-PWM converters is that they do not utilize the leakage of the power transformer. Therefore, the transformer should be designed with a minimum leakage. The leakage (and ac winding loss) of a transformer can be minimized by using the interleaving technology, at the penalty of much increased winding capacitances [38-42]. When the conventional PWM technique is used, the energy stored in these winding capacitances will be dissipated in the switches, thus significantly increasing the capacitive turn-on loss. Using the ZVT-PWM converter technique, these winding capacitances becomes part of \( C_d \), thus its energy is fed back into the input source during the zero-voltage switching transition.

When a converter is operated with high output-voltage, Schottky diodes usually can not be used as rectifiers. Thus high-voltage diodes with reverse recovery have to be employed. In a conventional PWM converter, a ZVS-QRC, or a ZVS-PWM converter, the rectifier diode is subjected to an abrupt reverse voltage right after turn-off; thus the high-voltage diode suffers from a severe reverse-recovery problem that significantly increases the switch stresses and the switching losses. Using the ZVT-PWM converter technique, this problem is less pronounced, since the passive switch in a ZVT-PWM converter is also commutated under zero-voltage switching. Consequently, the boost ZVT-PWM converter is a good candidate for power factor correction application.
Fig. 3.5. A number of topology variations of the buck ZVT-PWM converter.
Fig. 3.6. Several isolated topologies of the ZVT-PWM converters:
(a) forward, (b) flyback, (c) Cuk, and (d) Sepic.
3.4. **EXPERIMENTAL VERIFICATIONS**

3.4.1. Experimental Buck ZVT-PWM Converter

A 500 kHz, 100 W buck ZVT-PWM converter has been successfully implemented to demonstrate the operation of the new converters. It is regulated at 24 V output with a 40-60 V input. The power stage in Fig. 3.1 consists of the following components:

- S - IRF540 (International Rectifier),
- S1 - IRF630 (IR) in parallel with 31DQ06 (Scottky),
- D - 8TQ100 (Schottky),
- Lr - 1.5 uH,
- Lf - 500 uH,
- Cr - 4.7 nF Mica, and
- Co - 15 uF tantalum.

Figure 3.7 shows the oscillograms of the experimental circuit operating under different line and load conditions. It can be seen that the experimental waveforms agree with the theoretical analysis. Both the MOSFET and the rectifier diode operate with zero-voltage switching for the full line range and load range, while imposing low voltage and current stresses. As can be seen from Fig. 5(e), zero-voltage switching operation is still maintained at a 5% load, while the converter is operating in the discontinuous conduction mode. The breadboarded converter achieved a maximum efficiency of 94.5% at full load and low line.
Fig. 3.7. Experimental waveforms of the 500 kHz, 100 W buck ZVT-PWM converter at:
(a) low line, full load; (b) high line, full load;
(c) nominal line, full load; (d) nominal line, half load;
and (e) nominal line, 5% load.
1st waveform: $V_{GS}$ 20 V/div;
2nd waveform: $V_{DS}$ 50 V/div;
3rd waveform: $V_{GS},p$ 20 V/div;
4th waveform: $V_{Dr}$ 50 V/div;
5th waveform: $I_{Lr}$ 7.5 A/div.
3.4.2. Experimental Forward ZVT-PWM Converter

Another 600 kHZ, 50 W forward ZVT-PWM converter is implemented. Figure 3.8 shows the circuit diagram of the breadboarded converter. It regulates 5 V output with a 36-60 V input. The power transformer is implemented on a half H7C4-LP 23/8Z core. Since the auxiliary switch S1 operates with zero-current switching, the conduction of the slow MOSFET body diode should be prevented. This is usually done by using a Schottky diode in series with the FET and then adding an external fast-recovery diode. Here this problem is solved simply by using an external Schottky diode, as shown in Fig. 3.8. Since the body diode of the small FET IRF520 (S1) has a much higher forward voltage ($V_D=2.0$ V & 4 A) than the external Schottky diode, most conduction current flows through the Schottky diode.

Figure 3.9 shows the experimental waveforms of the converter operating at full load, half load and 5% load at $V_i=48$ V. The power stage achieved a maximum efficiency of 88% at low line and full load. With a reduced input voltage range, the converter efficiency can further be improved.
Fig. 3.8. Circuit diagram of the experimental forward ZVT-PWM converter.
Fig. 3.9. Experimental waveforms of the 600 KHz, 50 W forward ZVT-PWM converter at nominal line:
(a) full load, (b) half load, and (c) 5% load.
1st waveform: $V_{GS}$, 20 V/div;
2nd waveform: $V_{DS}$, 50 V/div;
3rd waveform: $V_{SEC}$, 20 V/div;
4th waveform: $V_{CPR}$, 100 V/div;
5th waveform: $I_{LR}$, 5 A/div.
3.5 SUMMARY

High-frequency, high efficiency dc-dc conversion requires much reduced switching losses in the conventional PWM converters while avoiding a significant increase in conduction losses. Using a number of recently developed resonant converter technologies, the switching losses can be reduced at significantly increased voltage and current stresses of the switches, thus leading to a significant increase of conduction loss and cost. This disadvantage makes the resonant technologies less attractive for practical applications.

This chapter presents a novel ZVT-PWM converter technology. It combines the advantages of the conventional PWM and resonant converter techniques. The advantages of the proposed ZVT-PWM converters are summarized as following:

- both the active and passive switches operate with zero-voltage switching;
- both switches are subjected to low voltage and current stresses associated with those in its PWM counterpart;
- the small auxiliary switch operates with zero-current switching;
- the zero-voltage-switching property can be easily maintained for full line range and full load range; and
- the design optimization of the circuit is easily attainable since the new converters operate with constant frequency.
The operation of the proposed converters was analyzed by using the buck ZVT-PWM converter as an example. A 500 kHz, 100 W buck ZVT-PWM converter and a 600 kHz, 50 W forward ZVT-PWM converter were breadboarded to demonstrate the feasibility of the proposed technique.

Since the rectifier diode in a ZVT-PWM converter is also zero-voltage switched, the proposed technique is attractive for high-voltage output applications (e.g., power factor correction circuits) where the rectifier suffers from severe reverse-recovery problem when traditional PWM, ZVS-QRC, or ZVS-PWM techniques are employed.
CHAPTER 4
CONCLUSIONS

In order to reduce size and weight of power suppliers, high-frequency operation of dc-dc converters has been widely pursued in the power electronics field. Using the conventional PWM technique for high-frequency operation can magnify the inherent problems of the PWM converters, such as high switching losses and severe EMI noise. These limitations can be alleviated by using "soft switching" converter technologies.

In most "soft switching" converters, higher VA ratings are observed for the switches and reactive components, which result in significant increase in conduction loss. Thus, a reduced switching loss is usually offset by an increased conduction loss. To operate a converter at higher frequencies and also more efficiently, it is paramount to minimize the circulating energy and component stresses.

Variable-frequency operation of converters often results in poor utilization of reactive components (including power transformer, input/output filters, resonant reactors). In order to derive a greater benefit from a high-frequency operation, it is desirable to operate the converters with a constant frequency. It can be concluded that an ideal con-
verter topology should combine the best features of resonant-type and conventional PWM converters, which include low switching losses, low voltage and current stresses of the devices, and constant-frequency operation.

This thesis presents two classes of new converters, featuring zero-voltage switching and constant-frequency switching. The ZVS-PWM technique combines the merits of the PWM and ZVS-QRC techniques. By simply using an auxiliary switch across the resonant inductor of a ZVS-QRC, it creates a freewheeling stage within the quasi-resonant operation, and enables the converter to operate with a constant frequency. Furthermore, a saturable reactor can be used to replace the resonant inductor. In this case, the load range under which zero-voltage switching is maintained can be extended without significantly increasing the circulating energy or the voltage stress of the power switch. Among the new family of ZVS-PWM converters, the FB-ZVS-PWM and the HB-ZVS-PWM topologies are deemed most desirable for practical applications, since the active switches are subjected to minimum voltage stress, as in their PWM counterparts. The ZVS-PWM technique can be considered as a extension of the ZVS-QRC technique.

The second family of new converters, i.e., the ZVT-PWM converters, combine the advantages of the "soft switching" converters and the PWM converters. A ZVT-PWM converter uses a resonant branch in parallel with the switches to achieve zero-voltage switching transition. This branch acts only during switching transition time, thus the operation of the new converter resembles that of a PWM converter during most of the switching cycle. As a result, both the transistor and the rectifier in a ZVT-PWM converter operate with zero-voltage switching, eliminating most of the switching losses. ZVT-PWM converters also feature low conduction loss since the switches are subjected to low

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voltage and current stresses associated with those in its PWM counterpart. Consequently, switching losses are greatly reduced without significantly increasing the conduction loss. Unlike the ZVS-QRC, ZVS-MRC, and ZVS-PWM techniques, ZVT-PWM converters can easily achieve zero-voltage switching at light load. Thus, when a ZVT-PWM converter is designed to meet zero-voltage switching at full load, zero-voltage-transition property will be maintained for the entire load range.

The detailed operation of the proposed converters is analyzed. A number of experimental converters have also been implemented to demonstrate the feasibility of the proposed techniques. To get better understanding of the new converters, some detailed dc analysis is required.

The zero-current switching technique is not addressed in this thesis. However, due to poor turn-off switching characteristics of high-power, minority-carrier, semiconductor devices (such as IGBTs, GTOs, and MCTs), zero-current switching topologies are very desirable for high-power applications when high-power devices must be used. In fact, by applying circuit duality to the ZVS-PWM converters, a family of ZCS-PWM converters can be easily derived [43]. This area deserves further investigation in the future.

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REFERENCES


VITA

The author was born in Yiyu, Zhejiang, P.R. China on May 19, 1965. He received his B.S. degree and M.S. degree from Zhejiang University in 1985 and 1988, respectively, both in electrical engineering.

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