A CASE STUDY IN AUTOMATED TESTING

by

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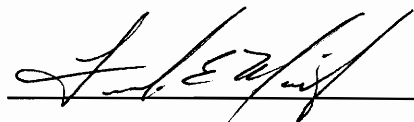

Frank Mintz

Blacksburg, Virginia
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ABSTRACT

As electronics technology has become more complex over the past few years, finding a suitable and cost effective testing method has become increasingly difficult. Very Large Scale Integration (VLSI) packaging technologies are making accurate diagnosis of printed circuit boards more costly and time consuming. Furthermore, a number of business related factors impact the suitability of any test approach.

The purpose of this project is the application of system engineering methodologies in the selection of the best automated testing approach for a new system. The system engineering effort will transform an operational need into a description of system performance parameters and a preferred system configuration through the interative process of requirements definition, functional analysis, synthesis, optimization, and requirement allocation. The integration of technical parameters will assure the capatibility of all physical, functional, and program interfaces in a manner that optimizes the total system design and definition.

An up-front engineering effort will help to identify acquisition cost and the on-going costs of operation and maintenance, both of which have equally important roles in determining the optimum test strategy.

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1.0 DEFINITION OF NEED

E-Systems, an electronic systems engineering company, has been contracted to design and develop a next generation large scale data processing system. The new data processing system will replace an existing system and be located at the same single consumer location. The system is expected to operate 24 hours a day, be operational 95% of the time, and meet all consumer requirements for maintainability, reliability, and usability.

The data processing system is designed to include built-in test such that, in event of failure, faults may be isolated down to the circuit board with a 95% degree of thoroughness, and an ambiguity level of three candidate boards. The faulty circuit boards are sent to the depot maintenance shop where repair is accomplished through the removal and replacement to ICs (which are discarded at failure). The objective is to provide a test capability for system circuit boards that will verify performance, diagnosis faults, and isolate failed components. It is anticipated that, based on system utilization requirements, 84 faulty circuit boards will be returned to the depot each year for corrective maintenance. In each instance, fault isolation will be accomplished to the IC with 90% degree of thoroughness, the process time will not exceed 3 days, and the applicable IC shall be returned to stores as a spare. The system component will consist of an estimated 400 digital circuit card assemblies that have to be maintained by the above test capabilities. The complexity of test will be the same for all circuit card assemblies.

The proposed test capability must incorporate the following provisions:

- Digital Logic Circuit Cards
- 14.5 inch x 15.71 inch board size
- Up to seven different logic families or voltage levels at the I/O
    1. TTL
    2. ECL and ECL Differential
    3. RS-232
    4. RS-422
    5. BTL
    6. IPL
    7. Ethernet
- Components will include surface mount, PGA, and through-hole devices
- Components on both sides of the circuit card
- Bus-oriented circuit cards having tri-stated devices and bus networks
- Minimum lead spacing of 100 mil

A more complete specification of test capability is provided in section 3.2.1 - System Requirements for Circuit Card Maintenance.

1.1 Manual or Automatic Test

The new system, through the use of new technologies, will substantially increase the capabilities of the system mission while decreasing the hardware and personnel requirements of operation and hardware maintenance. The down-sizing of hardware will be on the range of 600 Circuit Card Assemblies (CCA) to 125 CCAs. Although fewer boards are required, the complexity of these cards has increased many magnitudes. The next generation digital circuit boards will include:

- large pin-count devices;
- multiple internal and external data buses;
- application-specific ICs;
- surface-mounted devices, which may be loaded on both sides of the board;
- multilayer board structures;
- VLSI modules (containing multiple devices soldered to a common substrate and packaged as a single unit); and
- components with very high data rates.

Increasing levels of integration and advanced packaging technologies presents the particularly difficult problem of testability of the new circuit cards "outside-the-systems".

Growing complexity slows manual probing by multiplying the number of points which must be contacted. Packaging techniques like surface-mount restrict (or prohibit altogether) probe's ability to contact internal nodes. The complexity of the boards and increasing number of potential faults make manual testing "outside-the-system" impractical. "In-the-system" or off-line manual testing for the new system involves the use of circuit card extenders and standard test equipment. The average system downtime to isolate component failures in the off-line method has been approximated at 30 hours. The Turn Around Time (TAT) for manual testing "outside-the-system", depot maintenance, would be substantially higher than 30 hours without the system to provide high speed timing integrity and full functional testing. The technical expertise necessary for this particular method would be beyond intermediate technician capabilities. Manual test at the depot level cannot meet system specifications for processing time or diagnostic resolution. Automated Test Equipment resolves this problem by providing high diagnostic accuracy while significantly reducing diagnostic time. Decisions regarding the type of test equipment to be used for depot maintenance will be based upon repair policies, overall maintenance plans and planned number of systems. Tradeoffs are made of test requirements at each maintenance level, considering test complexity, time to fault isolate, operational environment, logistic support requirements, development time and cost. The degree of testing automation must be consistent with the planned skill levels of the equipment operators and maintenance personnel. Using the right diagnostic approach gets

inventory critical to mission operation back into productive use more rapidly and reduces the demands on skilled technicians and operators. The selection of a test strategy and degree of testing automation necessary to meet system requirements will be covered in-depth in section 2.0 Feasibility Study.

1.2 "Outside-the-System" vs. "Inside-the-System" Testing

In order to isolate and achieve a reasonable level of complexity and cost, a trade between complete "outside-the-system" fault isolation coverage versus some "in-the-system" fault isolation must be made. This trade has historically been resolved through an understanding with the system customer that a minimum of 90 percent fault coverage via an "outside-the-system" testing configuration is an acceptable compromise. The next generation system shall also work to this goal. The remaining 10 percent of faults shall be isolated "in-the-system" during system down times. Given the expected availability of system component down times, the isolation of these remaining faults "in-the-system" appears reasonable. The cost factors for the different test configurations will be evaluated next.

The cost of diagnosing faults on the printed digital circuit card for the new system can be evaluated by comparing manual and automatic tests. Total cost will be calculated from the volume of boards, the time required to diagnose the average board, the technician cost and the transport and repair costs for boards sent to depot maintenance. An explanation of the cost equation can be seen in Figure 1. The cost equation is used for the comparison of several scenarios (see

COST OF DIAGNOSING FAULTS ON A PCB

TOTAL COST = LABOR COST + TRANSPORT AND REPAIR COSTS

Vl = volume diagnosed locally

Vd = volume returned to Maintenance Depot

T = diagnose time averaged over all board types

W = technician cost (wages, benefits)

K = transport and repair costs for boards returned to depot

N = logistical volume returned to maintenance depot

Total Cost = TWV+ NK

Figure 1

Figure 2). Scenario 1 looks at all circuit card fault isolation being performed during off-line system time in a manual mode. The second scenario models the situation of 100% fault isolation being performed on an ATE at the Maintenance Depot. The third and fourth scenarios compare 90% of testing accomplished off-site with the ATE and the remaining 10% by off-line manual testing. The difference between scenario 3 and 4 is a decrease in technician skill and cost for the ATE. A cost summary of all the scenarios show the lowest total cost for testing to be the 100% ATE at $215,000 for the system lifetime. The 100% ATE test configuration is taken out of consideration for the reasons mention above leaving scenario #4 as the lowest cost. Scenario #4 consists of off-line manual testing being perform 10% of the time with highly skilled technician and the other 90% by a lower skilled

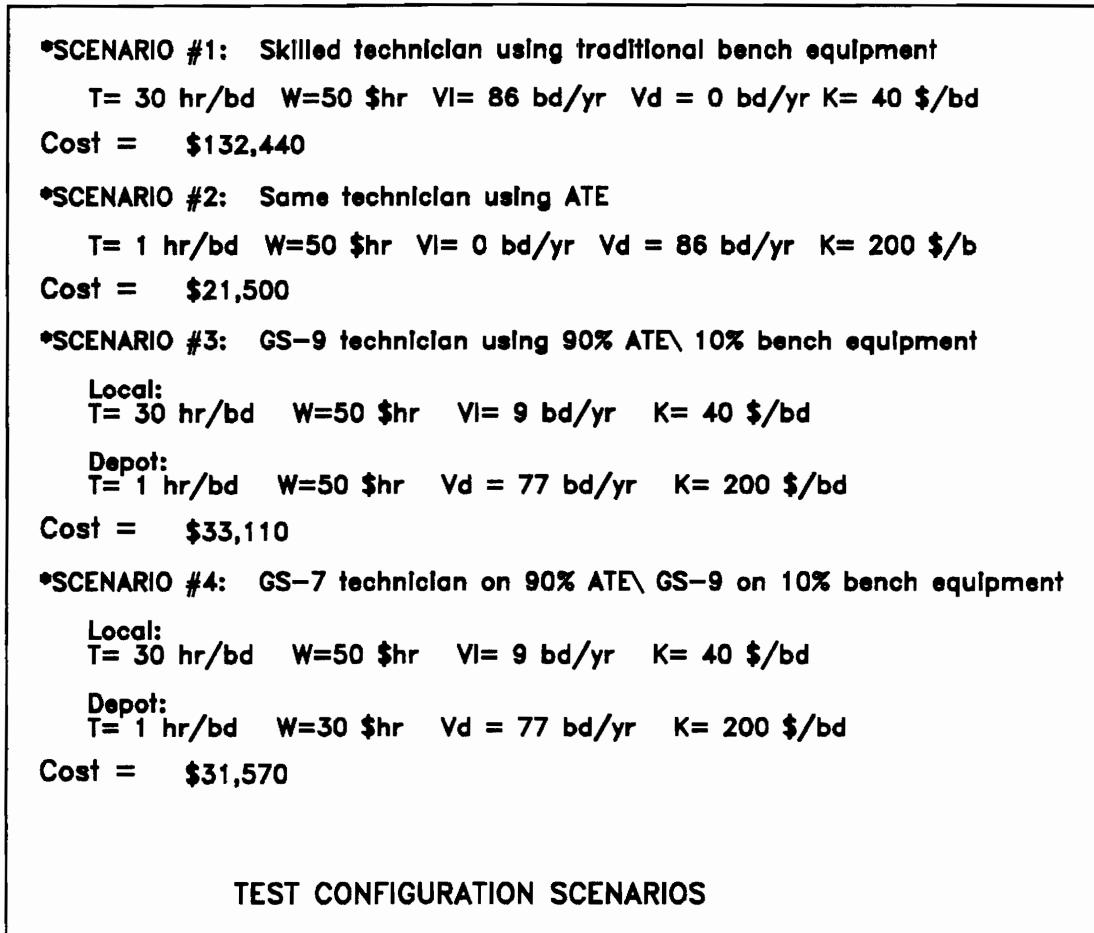

Figure 2

technician on the ATE. This method has a total lifetime cost of $315,700. The test configuration with the largest cost was 100% off-line manual testing with a lifetime cost of $1,324,400.

$$A_i = 1 - \frac{num\ of\ bd\ fails\ per\ yr\ x\ avg\ diagnose\ time}{operating\ time\ x\ 1\ year}$$

Two other cost factors need to also be analyzed in order to correctly select a test configuration. These factors are the inherent availability obtainable with the different configurations and the cost impact from the off-line system downtime. An

estimate of the impact on availability for each test configuration can be calculated by using the above formula. The formula produces a 71% availability for the totally manual test configuration which is unacceptable for this contract. The combination of 10% manual test and 90% Automatic Test Equipment produces an availability of 97% which is an acceptable combination. The purpose of this exercise was to show that an alternative method of test is needed for this system due to its high operating time and large availability requirements. The system availability requirements could have also been meet by increasing reliability with a parallel backup system. However, the cost of replicating a system of this magnitude and expense is not a viable alternative. In addition, discard of failed boards is also not a consideration due to the high cost and complexity of the system circuit boards. The system availability specifications can be realistically met with a combination of off-line manual test and "outside-the-system" automated test.

1.3 System Maintenance Concept

The system maintenance concept and repair policy consists of on-site organizational maintenance and off-site depot maintenance (see Figure 3). Organizational maintenance consist of the utilization of built-in diagnostic to verify system operation. In the event of a failure, system diags will identify a Card Candidate List (CCL) for the isolation of the defective circuit card assembles. In addition, diagnostic will also be used for off-line manual testing of failed boards that cannot be repaired at the depot level. The transportation time for assemblies,

parts, and IC(s) from the system site to the depot is approximately 30 minutes. The majority of parts and components are stored on-site with a small stock of commonly used components located at the depot. All spare circuit card assemblies are stored on site for immediate access. The spare board pool will enable the system Mct specification of 1.0 hr to be met. Maintenance personnel located on-site range from GS7 technicians for day to day maintenance to degreed engineers for system level problems.

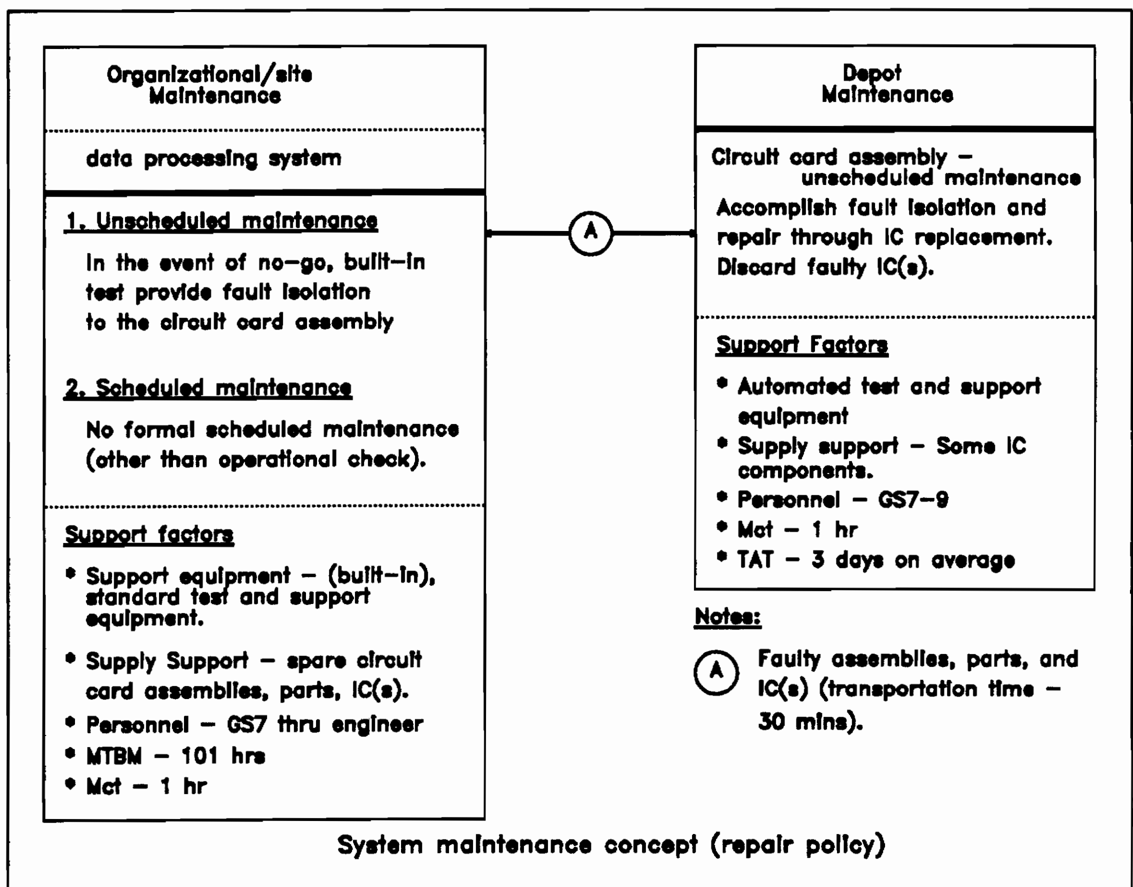

Figure 3

The depot maintenance facility is located close to the consumer site for quick transportation times. The transport time for the return of repaired boards or

parts is 30 minutes. The Turn Around Time (TAT) of the current system is largely determined by the level of spares available. A circuit card being sent to the maintenance depot for repair will be prioritized by mission impact. This produces TATs of as little as a few hours to a mean average of three days for a circuit board with ample spares. The logistical pipeline for the next generation system will be the same as current system and can be seen in block diagram form in Figure 4.

The depot also provides quality assurance and rework services for the consumer site. The depot will operate and maintain an automated test equipment system to repair all defective circuit cards. Personnel will consist of GS7 through GS9 for operation and maintenance of the ATE. A detailed explanation of the system support plan will be presented in section 4.0 System Maintenance Concept.

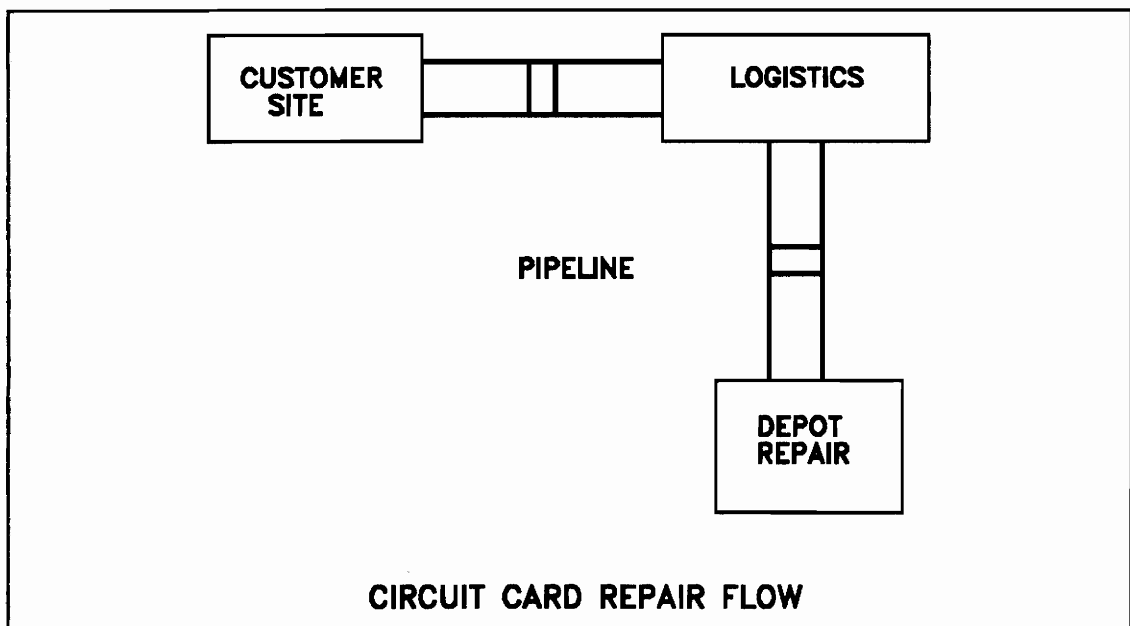

Figure 4

1.4 Systems Engineering Effort

The customer has also contracted E-systems to operate and maintain the system during its life cycle similar to the current system. The maintenance depot has been tasked with the selection of a digital ATE system that will meet the off-line test requirements of the new system within a set budget of $3,300,000. The ATE selection process will be accomplished in conjunction with the conceptual design phase of the new system. The system engineering effort needed to adequately define test requirements will consist of many processes including, but not limited to, degree of testing automation, conceptual design, and supportability analysis.

2.0 FEASIBILITY STUDY

The feasibility study for this project consist of the evaluation of alternative test technologies and the selection of a test strategy. The test strategy for the ATE must meet all system requirements.

2.1 Test Strategy Selection

Choosing a test solution requires a good working knowledge of all aspects of the product to be tested and the system's operation. The typical fault spectrum for the proposed system needs to be determined. From this data, the type of ATE necessary can be better identified.

Understanding the technical parameters which must be tested is the first step. This process begins with a good working knowledge of the type of technology to be addressed. The ATE system of choice must be capable of measuring all real-world specifications. The resolution and accuracy of parameters to be generated or measured also affects the selection and, ultimately, the cost of the ATE system required. Certain parameters must be considered which normally are not covered in the test procedure. These parameters relate to diagnostic capability. If diagnostics to the component level are required, a knowledge of the projected fault spectrum is another factor necessary to determine the ATE system required. Many ATE Systems do not diagnose every possible type of fault. The types of technology to be tested also can dictate the test philosophy or strategy to be

invoked for system development. Depending on system operation, several solutions may be required.

A test strategy should determine what must be tested, the type of tester to be used, the type of fault problems that are occurring on present and future printed circuit cards and also the overall capabilities of the plan. Customer and off-site maintenance personnel should also be included in any test strategy and plan. This can often save a considerable amount of operation and maintenance cost in the life cycle of a system. Therefore, it is advisable to include Field Service Support in any test strategy development cycle.

2.2 Economic Factors

Economic issues are important once the technical requirements have been addressed. ATE selection for a new system requires early involvement in the design system design process to help pinpoint testing problems that may become more expensive to solve later. The ATE purchase is only the tip of the iceberg. In the first year of purchase, there can be a large investment in test fixtures, program development and training. Depending on how a department's budget is structured, much of this will come out of the capital equipment budget. When selecting an ATE vendor, be certain a true first-year budget is in place. A system with no fixtures or programs is not very useful. A breakdown of the ATE cost structure can be seen in Figure 5.

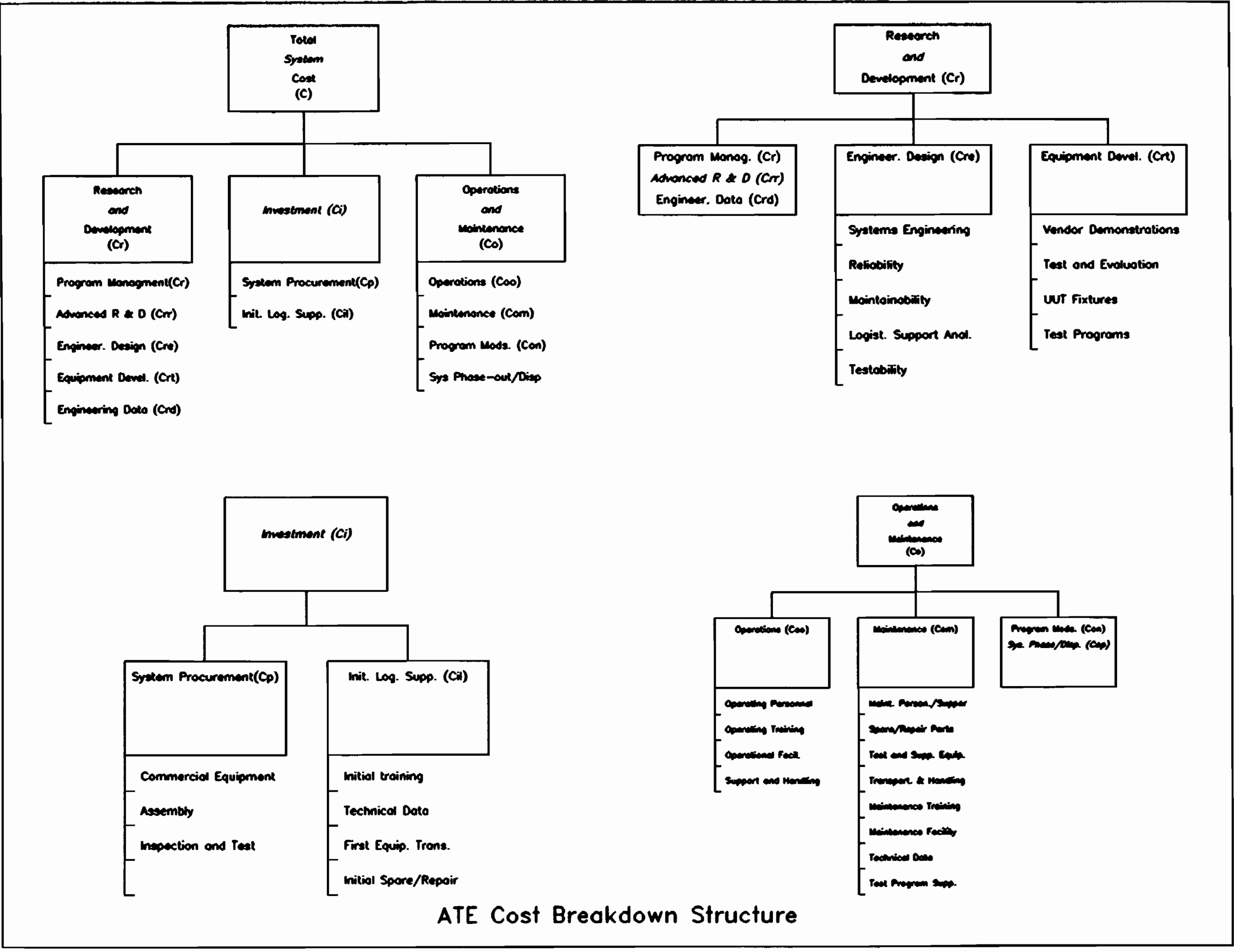

Figure 5

2.3 System Architectures/Topology

An brief overview of the types of ATE and their capabilities available today follows:

2.3.1 Functional Test

Functional test is the oldest test philosophy in ATE. A functional test system normally puts the Unit-Under-Test (UUT) through its paces as if it were connected to the system for which it is designed.

The emulative type of functional test is an exception. In this type of system, the ATE replaces, or emulates, the microprocessor or boot ROM on the UUT. The UUT is tested from the microprocessor kernel out to the edge connectors and not the reverse, as in the case of regular functional test.

In either case, the UUT is tested at its normal operating characteristics. Functional test potentially has the highest possible fault coverage of any ATE philosophy, with yields up to 98% of all potential faults.

Detection of manufacturing defects normally is very slow in functional testers because the system usually does not have access to all test points on the UUT simultaneously. The fault is traced via a guided probe which the operator connects to various points based on prompts by the test program.

The area of major concern with functional test pertain to test-program development. Since the UUT is tested as a whole, the programmer must have an intimate knowledge of the UUT in order to write code.

The ATE vendor should have a number of tools to assist the programmer. Some of these features include links to CAD/CAE files, high-level programming language, on-line help and program debugging tools.

2.3.2 Digital In-Circuit Testing

The digital in-circuit system functionally tests the Ics by stimulating the inputs and verifying the outputs for the proper logic state. Component probing is static during card testing with ATE probe connections made through a "bed-of-nails" fixture. The unique bed-of-nails fixture is developed having a nail layout corresponding to the card IC placement. Input and output patterns are stored in a library element for each device to be tested. Programming usually consists of placing copies of the necessary library elements in a directory and modifying the elements to suit any on-board configurations.

When considering in-circuit testing, two points must be considered. First, the in-circuit test will detect few timing related conditions because the test system is working with each device individually. Race conditions would be undetected in this philosophy. An evaluation of the projected fault spectrum will help determine if this is a problem.

The second issue is related to the technology to be tested. In-circuit testing uses a technique called backdriving to test each IC. This can put undue stress on some ASICs if the system does not have adequate control of the input signals. This issue must be discussed with the ATE vendor.

An evaluation of the ATE system and the UUTs also may indicate that the majority of the UUTs can be tested without fear of damage to devices. The devices that are not tested may be so reliable that test at this stage will not be necessary.

2.3.3 Cluster Testing

By nature, the cluster approach is the best. The cluster ATE system can employ a composite of the above philosophies. Cluster testing combines the advantages and disadvantages of both functional testing and in circuit testing. Cluster testing is basically a scaled-up version of in-circuit testing and a scaled-down version of functional testing. Cluster testing requires a unique bed-of-nails fixture for each card design to allow ATE to probe cluster boundaries. In cluster testing, a card is divided into typically four to eight functional clusters and tested on an ATE. Cluster testing is similar to in-circuit testing in that the clusters are tested independently of the other clusters. But within each cluster, functional testing techniques are used to isolate the fault. Each cluster is tested using functional test methods. As in functional testing, guided probe diagnostics are used to help isolate the failure. This requires that a simulation and fault-grading database be developed for the ATE similar to the database generated for functional testing. Test complexity is greater than in-circuit testing but less than functional.

COST FACTORS	
FUNCTIONAL TESTING	
DESIGN FOR TEST (17 DESIGNS X 40 HOURS X $50/HOUR)	= $34,000
TEST FIXTURES (2 FIXTURES X $20,000)	= $40,000
TEST DEVELOPMENT (17 DESIGNS X 17 WEEKS X $50/HOUR X 1.2)	= $693,600
FUNCTIONAL TOTAL	= $767,600
IN-CIRCUIT TESTING	
DESIGN FOR TEST (17 DESIGNS X 100 HOURS X $50/HOUR)	= $85,000
TEST FIXTURES (14 DESIGNS X $15,000 + 3 DESIGNS X $30,000)	= $300,000
TEST DEVELOPMENT (17 DESIGNS X 16 WEEKS X $50/HOUR X 1.2)	= $652,800
IN-CIRCUIT TOTAL	= $1,037,800
CLUSTER TESTING	
DESIGN FOR TEST (17 DESIGNS X 80 HOURS X $50/HOUR)	= $68,000
TEST FIXTURES (17 FIXTURES X $12,000)	= $204,000
TEST DEVELOPMENT (17 DESIGNS X 16 WEEKS X $50/HOUR X 1.2)	= $652,800
CLUSTER TOTAL	= $924,800

TEST STRATEGY – INITIAL COSTS

Figure 6

2.4 Evaluation of Testing Alternatives

The initial evaluation of alternatives is shown on Figure 6. As we begin to explore the cost effectiveness of the various alternatives it will be helpful to begin with developmental costs for the different test strategies.

Initial testing costs will be quantified as consisting of the cost of the ATE and fixtures, engineering cost of Design-For-Test, and the card test program development cost. The Design-For-Test process is define as the testibility philosophy which takes into consideration the post-design testing phase, and which attempts to reduce the effort and cost of testing. The fixtures cost will be derived

by multiplying the estimated typical cost of a test fixture by the expected number of card designs for the new system. The Design-For-Test cost is the engineering cost associated with adding DFT features to the card designs. It is assumed that the parts cost for DFT is negligible and any board area requirements of DFT has no impact. The cost for test development is the test engineering time required for all the phases of test development.

2.4.1 In-circuit costs

The typical in-circuit fixture cost for existing 15 x 15 Interactive System card designs is $15,000. It has been estimated that three of the 17 card fixture designs for in-circuit testing would be more expensive ($30,000) due to double-sided surface mount components.

2.4.2 Functional costs

Only one fixture is needed for functional testing since all circuit cards in the new system have the same I/O connector (480 pin). The fixture cost on the functional strategy represents one fixture design and one spare. The fixture cost is higher ($20,000) than the other two alternatives due to fact that a better fixture technology is needed to maintain high signal integrity at high functional testing speeds.

2.4.3 Cluster costs

Cluster testing fixtures require a reduced number of nails and wire than in-circuit testing due to the decrease in required node probing. Therefore, the $15,000 cost of in-circuit testing is reduced to $12,000 for cluster testing fixtures.

COST FACTORS

FUNCTIONAL TESTING REPAIR	
COST OF REPAIRS ON TESTER(90% OF CARDS) = 864(90%)(1 HOUR)($50/HOUR) + 778($200)	= $194,500
COST OF REPAIRS IN SYSTEM(10% OF CARDS) = 864(10%)(30 HOURS)($50/HOUR) + 86($40)	= $132,440
FUNCTIONAL TOTAL	= $336,940
IN-CIRCUIT TESTING REPAIR	
COST OF REPAIRS ON TESTER(80% OF CARDS) = 864(80%)(.5 HOUR)($50/HOUR) + 691($200)	= $155,480
COST OF REPAIRS IN SYSTEM(20% OF CARDS) = 864(20%)(30 HOURS)($50/HOUR) + 173($40)	= $266,120
IN-CIRCUIT TOTAL	= $421,600
CLUSTER TESTING REPAIR	
COST OF REPAIRS ON TESTER(84% OF CARDS) = 864(84%)(.75 HOUR)($50/HOUR) + 726($200)	= $172,400
COST OF REPAIRS IN SYSTEM(16% OF CARDS) = 864(16%)(30 HOURS)($50/HOUR) + 138($40)	= $212,920
CLUSTER TOTAL	= $385,320

TEST STRATEGY – UTILIZATION COSTS

Figure 7

2.4.4 Repair Costs

The next cost factors to evaluate the test strategies against is the cost of circuit card repair in and out of the system (see Figure 7). The operational repair costs are based on the estimated number of card failures over the lifetime of the system

and the average fault detection of the specific test strategy. The number of lifetime card failures is based on the total number of cards in the system and the MTBF of the cards. The MTBF of the system has been calculated to be 101 hours. This results in an estimate of 864 card failures over the 10 year life of the system.

2.4.5 Test Strategy Summary

Figure 8a and 8b summarize the costs of functional, in-circuit, and cluster testing. Functional testing has proved to dominate the other two test strategies having the lowest overall cost with the highest percentage of fault detection.

2.5 Diagnostic Methodology Selection

The next step in developing a test plan is the selection of diagnostic tools and techniques that enable the isolation of failed GO/NO-GO functional tests. Diagnostics to locate the fault are typically approached in one of three ways: interactive instrument approaches, "walking clip" in-circuit testing, or a probe-oriented diagnostic technique.

2.5.1 Interactive diagnostics

Interactive diagnostics involve creating and using a database to isolate faults. The user takes nodal measurements such as frequency, voltage, and logic analysis and compares them to previously learned "good" values. Some of the advantages to this approach include the relatively low initial cost and the brief

COST FACTORS

FUNCTIONAL TESTING

INITIAL COST	= $767,600
TOTAL COST OF BOARD REPAIR	= $336,940
FUNCTIONAL TOTAL	= $1,104,540

IN–CIRCUIT TESTING

INITIAL COST	= $1,037,800
TOTAL COST OF BOARD REPAIR	= $421,600
IN–CIRCUIT TOTAL	= $1,459,400

CLUSTER TESTING

INITIAL COST	= $924,800
TOTAL COST OF BOARD REPAIR	= $385,320
CLUSTER TOTAL	= $1,310,120

TEST STRATEGY TOTAL COSTS

Figure 8a

programming time compared to the other alternatives. The major disadvantages are slow throughput and the need for technicians who are skilled and knowledgeable in measurement analysis and operation of the Unit-Under-Test.

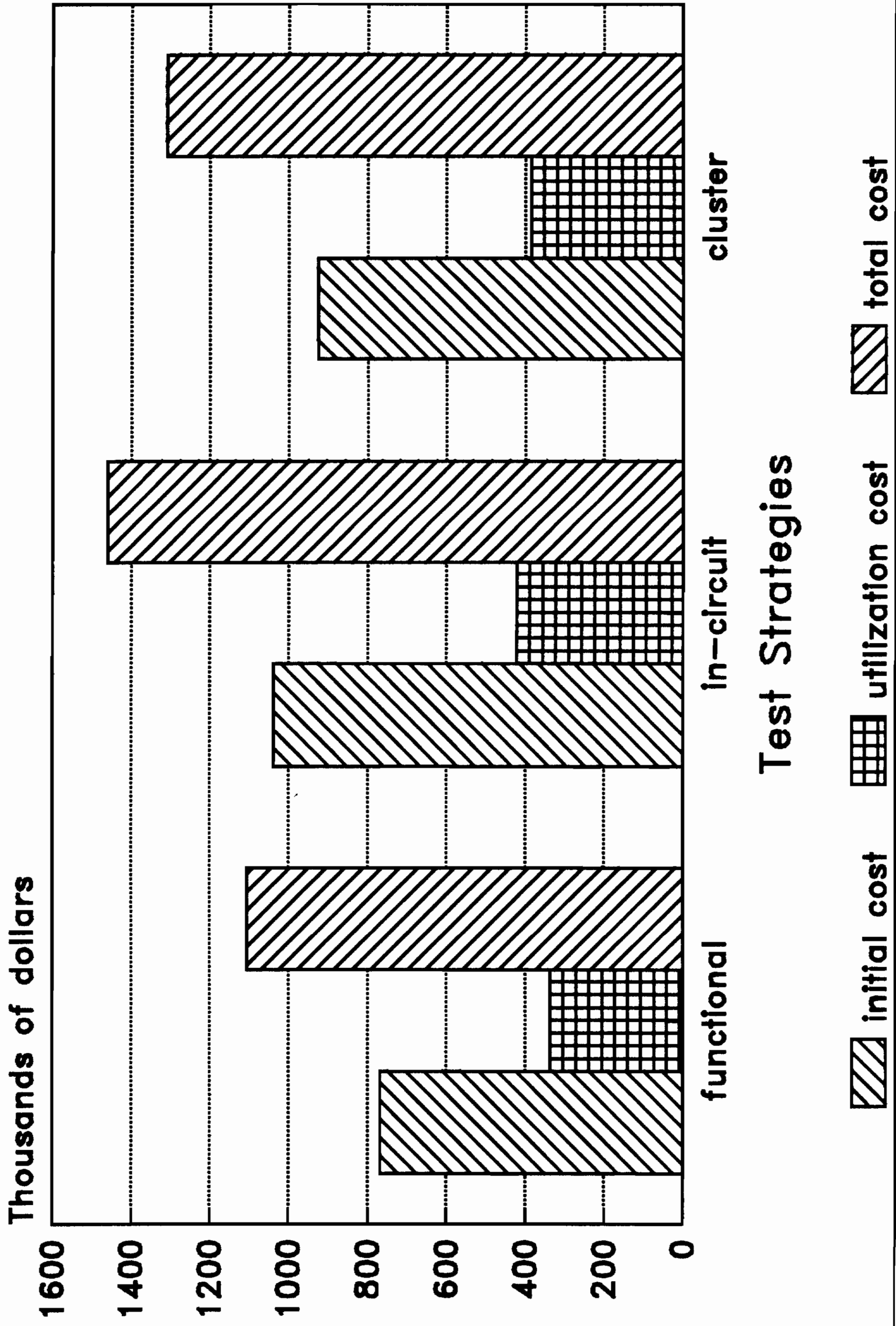

Figure 8b

2.5.2 "Walking clip" in-circuit diagnostics

"Walking clip" in-circuit testing uses IC clips and programmed test routines to isolate faulty components or nodes on the board. Here, the technician "walks" an IC clip through the section of the board that failed the functional test until the faulty component is identified. Advantages of this approach are the short start-up time and the low operating and programming skills needed to prepare and run the diagnostics. The major disadvantages are the relatively slow throughput and low level of test comprehensiveness.

2.5.3 Probe-oriented diagnostics

The third option is a computer driven probe-oriented diagnostic approach which can be accomplished be employing either fault tree analysis, guided probe diagnostics or the combination of both.

A fault tree is implemented in application software and directs a probing sequence for each possible fault. While this approach is useful enough for simple boards containing SSI or MSI devices, it becomes unwieldy for more complex boards. The reason is that as board circuitry increases in complexity, the number of necessary probing paths multiplies and becomes very cumbersome for programming. In addition, fault tree analysis is more error prone since the programmer must decide which nodes to probe and in what order. This problem can be combated with certain CAE tools that simulate the circuit card.

Guided probe diagnostics use a software algorithm based on a representation of the circuit and the results of the previous measurement to guide the operator to the next node to be measured. The actual measured output is compared to the expected readings. If the actual data differs from the expected data, the operator is instructed to probe the next layer of driving logic. The user repeats this process until a diagnostic based on analysis of the failing measurements can be reached. The advantages of this diagnostic approach are the low operating skill level required and high level of test comprehensiveness. The limitations include the high initial test program investment and the high level of programming skills needed.

2.6 Evaluation of Diagnostic Alternatives

A number of business related factors impact the affordability and suitability of a given diagnostic approach. The nine factors most commonly used in selecting the optimal ATE diagnostic are listed in Figure 9[1]. Each of the diagnostic

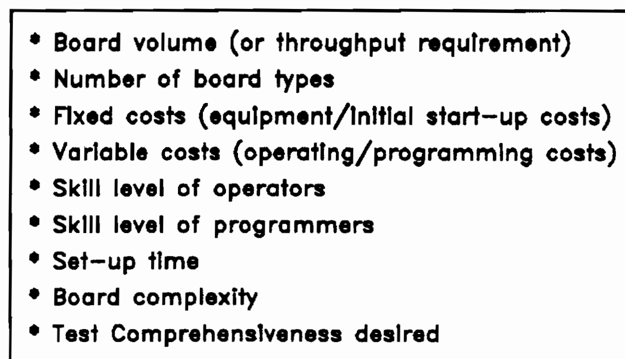

Figure 9

techniques discussed offers differing strengths and weaknesses for each of the nine decision factors that are listed. Interactive techniques demand the least amount of programming skill, but do demand highly skilled technicians or operators. Guided probe techniques, on the other hand, demand higher-skilled programmers, but allow for lower-skilled operators.

Interactive approaches require little programming expense but demand a high recurring test investments (beyond highly skilled technicians) and longer test times. Guided probe and fault tree approaches eliminate much of the instrumentation costs, but have higher programming costs.

Interactive approaches cope better with high board-type environments, but not as well with high board-volume demands. Guided probe offers the high throughput the large board volume demands, but falls down in a high board-type mix where time and cost of programming becomes a bigger factor.

2.6.1 Selection Model

The nine business factors discussed above can be put in a simple mathematical model to help determine the most suitable diagnostic approach for our situation (refer to table I)[2]. In this model weights have been assigned to each of the diagnostic approaches for all nine decision criteria. By selecting the most important four or five criteria and adding the relative weights of the scores for interactive, in-circuit, guided probe diagnostics, or fault tree analysis, the relative suitability of each diagnostic approach will be measured.

Table I

SELECTION FACTORS	GUIDED PROBE	FAULT TREE	"WALKING CLIP"	INTERACTIVE
	DIAGNOSTIC SOLUTIONS			
HIGH BOARD VOLUME	9	9	5	1
HIGH NUMBER OF DIFFERENT BOARDS	4	2	8	10
LOW OPERATOR SKILL LEVEL	8	8	8	0
LOW FIXED COST	3	3	8	10
LOW VARIABLE COST	8	10	5	1
LOW PROGRAMMING SKILL LEVEL	4	2	7	11
HIGH TEST COMPREHENSIVENESS	8	7	3	6
LOW START-UP TIME	3	1	8	12
HIGH BOARD COMPLEXITY	9	3	8	4

WEIGHTING FACTORS IN DIAGNOSTIC DECISION MAKING

In this model, the higher the score, the more suitable the approach. Each probe-oriented technique is treated separately due to some major differences between fault tree analysis and guided probe diagnostics. Please note that the weights are based on field experience, not theoretical data. The new system will consist of a broad mix of highly complex boards. The "off-line-system" board repair performed at the maintenance depot will consist of a low volume of boards with high test comprehension. Lower-skilled technicians (GS-7) will be responsible for ATE system operation. Low variable cost will also be an ATE system criteria since the initial programming and equipment cost will overshadow the ATE operating or

variable costs. Using the weights for number of different boards, skill level, low variable costs, test comprehension, and board complexity we find:

Guided Probe	4 + 8 + 8 + 8 + 9 = 37
Fault Tree	2 + 8 + 10 + 7 + 3 = 30
In-Circuit	8 + 8 + 5 + 3 + 8 = 32
Interactive	10 + 0 + 1 + 6 + 4 = 21

The guided probe technique rated the highest of all the alternatives with a 37. Fault tree and in-circuit were relatively close in summed weights with the interactive approach rating substantially lower. A simplified version of the selection model is shown in Table II with the higher weighted criteria indicated for the decision matrix. Utilization of the simplified model indicates guided probe and fault tree as the dominating diagnostic solutions(see Table III).

When considering the major diagnostic approaches, clear differences exit. The probe-oriented techniques, guided and fault dictionary both rated high for our specific application. The controlling criteria being high board complexity and the low variable costs. The next step in the selection of a diagnostic solution will be to analysis the probe-oriented techniques to identify which of these approaches best meet system requirements.

Table II

DIAGNOSTIC SOLUTIONS

SELECTION FACTORS	GUIDED PROBE	FAULT TREE	"WALKING CLIP"	INTERACTIVE
HIGH BOARD VOLUME	■	■		
HIGH NUMBER OF DIFFERENT BOARDS			■	■
LOW OPERATOR SKILL LEVEL	■	■	■	
LOW FIXED COST			■	■
LOW VARIABLE COST	■	■		
LOW PROGRAMMING SKILL LEVEL				■
HIGH TEST COMPREHENSIVENESS	■	■		■
LOW START-UP TIME				■
HIGH BOARD COMPLEXITY	■			

SIMPLIFIED MATRIX FOR DIAGNOSTIC APPROACH DECISION MAKING

2.6.2 Guided Probe, Fault Dictionary, or Both

Guided probe analysis and the fault dictionary have complementary sets of advantages and drawbacks. Guided probe requires a large data base and is relatively slow; it can take even a experienced operator many minutes to probe back to the source of a fault on complex, bus-structured boards. The fault dictionary uses a much smaller data base and is much faster, identifying likely fault locations in just a few seconds.

But guided probe generally yields better diagnostic resolution. The fault dictionary, whose individual stimulus and response listings (or "fault signatures")

Table III

SELECTION FACTORS	DIAGNOSTIC SOLUTIONS: GUIDED PROBE	FAULT TREE	"WALKING CLIP"	INTERACTIVE
HIGH BOARD VOLUME	■	■		
HIGH NUMBER OF DIFFERENT BOARDS			■	■
LOW OPERATOR SKILL LEVEL	⊠	⊠	⊠	
LOW FIXED COST			■	■
LOW VARIABLE COST	⊠	⊠		
LOW PROGRAMMING SKILL LEVEL				■
HIGH TEST COMPREHENSIVENESS	⊠	⊠		⊠
LOW START-UP TIME				■
HIGH BOARD COMPLEXITY	⊠			

SIMPLIFIED MATRIX FOR DIAGNOSTIC APPROACH DECISION MAKING

may describe more than one fault, cannot always diagnose a problem with absolute certainty and in some cases must indicate several "most-likely" fault locations.

Increasing levels of integration and advanced packaging technologies are challenging the diagnostic capabilities of guided probe and fault dictionary alike. The next generation system circuit boards will include:

- large pin-count devices
- multiple internal and external data busses

- application-specific Ics
- surface-mounted devices, which may be loaded on both sides of the board
- multilayer board structures
- VLSI modules (containing multiple devices soldered to a common substrate and packaged as a single unit), and
- components with very high data rates.

Growing complexity slows guided probe by multiplying the number of points which must be contacted. Packaging techniques such as surface-mount restrict (or prohibit altogether) probe's ability to contact internal nodes.

The non-invasive fault dictionary works independently of board packaging, but more complex boards and the increasing number of potential faults are making it harder to provide good diagnostic resolution. A larger fault universe always demands an extremely efficient fault simulation capability to create a dictionary large enough to be useful.

Although recent developments have enhanced the capabilities of fault dictionary and guided probe individually, the greatest diagnostic efficiencies are often realized combining the two techniques. A quick initial diagnosis will likely fault sites by the dictionary eliminating the need to probe painstakingly back from an output. The guided probe for its part, can find faults which the dictionary alone is unable to pinpoint. A tight integration, in which the probe algorithm consults the

fault dictionary before it selects each probe point, can achieve very high diagnostic accuracy while significantly reducing diagnostic time.

2.6.3 Diagnostic Solution Conclusion

Recent advances in guided probe and fault dictionary hardware and software have provided a powerful, flexible set of diagnostic tools for today's complex VLSI boards. The linking together of the guided probe and the fault dictionary in a continuous interaction can be a powerful means of speeding overall diagnostics and repair times. A technique which permits the guided probe algorithm to access the fault dictionary data base not just at the start of probing but throughout the process reduces the number of points which must be probed to make a diagnosis.

2.7 Test Strategy/Plan Trade Summary

The ATE system trade study began with the evaluation of the three test strategies: functional, in-circuit, and cluster. Analysis of these testing approaches against initial costs and operational repair costs revealed functional testing dominating with the lowest overall life cycle cost. The next step was the selection of an optimum diagnostic solution for the fault isolation of failed GO/NO-GO functional tests. A decision matrix was utilized to highlight weighted modeling criteria of our ATE system requirements. The results of the modeling indicated that the probe-oriented diagnostics would best suit our system specifications. The final

step was the decision of using guided probe with or without the fault dictionary capability. An evaluation of the state of today's guided probe and fault dictionary hardware and software showed considerable benefits from the pairing. These benefits include enhanced VLSI capabilites, reduced fault isolation time, and an increase in diagnostic accuracy. These benefits will help in reducing costly "in-system" repair time. The cost of adding the fault dictionary is considered moderate since full-card simulation will be performed as part of board design and independent of the test method. Therefore, fault grading is the only added CAE cost.

3.0 ATE SYSTEM OPERATIONAL REQUIREMENTS

The generation of system operational requirements will be accomplished by analyzing the definition of need and the feasibility study. The requirement specification will consist of ATE system operating characteristics, the maintenance concept for the ATE system, and the identification of specific design criteria.

3.1 Mission Definition

The prime mission the Digital Automatic Test Equipment is the performance evaluation of Circuit Card Assemblies (CCA) that permits the user to identify faults to the component. This scenario is depicted in Figure 10.

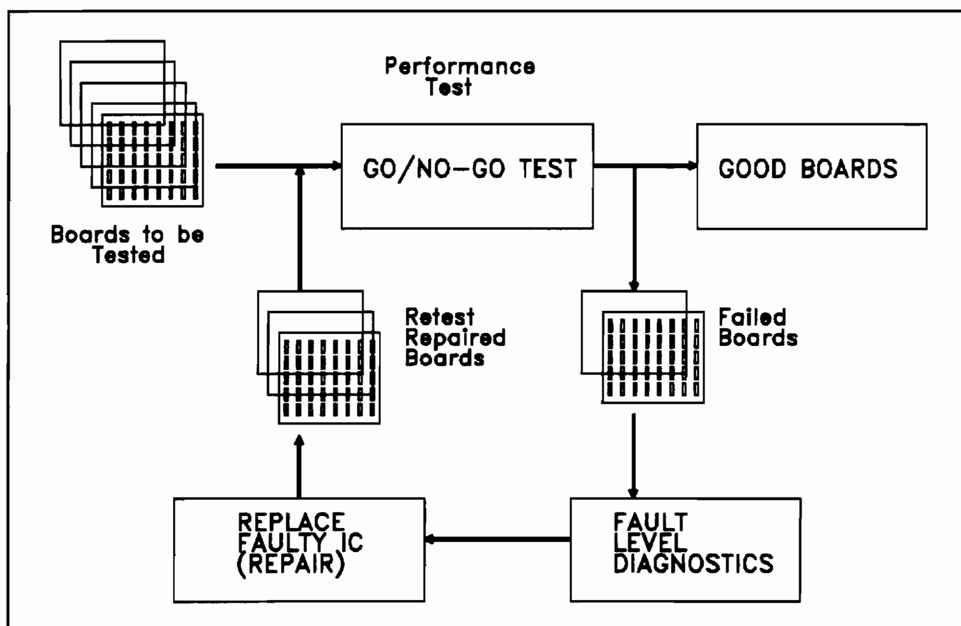

Figure 10

Go/No-Go Test - The first level of CCA test is verification to determine whether the board operates functionally to specification.

Fault Level Diagnostics - The second level of CCA test is finding what went wrong on the board and identifying it so it can be repaired.

3.2 Performance of Physical Parameters

3.2.1 System Requirements for Circuit Card Maintenance

The following section will specify the hardware and software requirements placed on the development of the next generation system digital circuit cards. The specifications will focus on the requirements needed for the maintenance of Printed Circuit Boards.

3.2.1.1 Hardware Specifications

The maintenance depot will use the Digital Automatic Test Equipment to test printed circuit cards with the following characteristics:

- Digital Logic Circuit Cards
- 14.5 inch x 15.71 inch board size
- Up to seven different logic families or voltage levels at the I/O
    1. TTL
    2. ECL and ECL Differential
    3. RS-232
    4. RS-422
    5. BTL

6. IPL

7. Ethernet

- Components will include surface mount, PGA, and through-hole devices
- Components on both sides of the circuit card
- Bus-oriented circuit cards having tri-stated devices and bus networks
- Minimum lead spacing of 100 mil

3.2.1.2 Computer Aided Engineering (CAE) Equipment

The following is a list of the CAE platforms, software and networking being used in the development of the next generation system.

CAE software:

System Expert Release 5.1

- includes: CADAT simulation and fault simulation
  VISULA PCB Editor

Computer and Networking:

Sun Microsystem workstations

- types: SPARCstation
  SPARCserver

Ethernet

- protocol: TCP/IP

3.2.2 ATE General Requirements

The ATE shall have the following capabilities relating to diagnostics:

1. Capability to test cards as described in section 3.2.1 (hardware specification)

2. Capability to test a common circuit card edge connector for a maximum 480 signal I/O

3. Graphical User Interface for data entry and test program control

4. Capability to provide a minimum of six 40 Mhz clock signals with at least the following formats:

   - return to zero
   - return to one
   - return to complement

   In addition, the clock shall have a programmable duty cycle with a range of at least 10% to 90%

5. Capability to manually generate test patterns and test control programs using additional equipment or software other than that provided with the ATE. This programming shall be

accomplished using either a high-level programming language or a graphical user interface.

6. Capability to accept a test program from a logical simulator

7. Capability to generate all stimulus and monitor responses needed for UUT verification

3.2.3 ATE Hardware Requirements

3.2.3.1 Interface To Unit Under Test

The ATE mechanical and electrical interface (hereafter referred to as the receiver) on the ATE shall be of such construction as to promote good data, clock and power transmission to the UUT. The ATE receiver shall have the following characteristics:

1. Allow for Interface Test Adapters (fixtures) to be built that can support the system circuit cards while maintaining all the features of the ATE.

2. Mechanical parts designed so as to handle, as a minimum, 10,000 cycles fixtures put on and taken off the ATE before replacements due to wear is necessary.

3. Electrical design such that signal integrity from the ATE to the UUT is maintained.

4. Electrical design such that proper grounding between the UUT and the ATE is maintained.

5. Electrical connections should be made through either a mechanical zero-insertion-force connector or through a bed-of-nails configuration using vacuum for pull-down.

The receiver base shall be a common product from the vendor with Interface Test Adaptor mounting kits available from third party fixtures houses. The receiver shall be designed such that the Interface Test Adapters can be built for a reasonable cost.

3.2.3.2 Characteristics of Pins to Unit Under Test

The ATE 480 I/O pins shall have the following capabilities and characteristics:

1. Capability to provide simultaneous input stimuli across the I/O to the UUT.

2. Capability to simultaneously switch all 480 I/O from any combination of logic-high or logic-low states to the complement state at the full rate of the ATE while maintaining data integrity in the ATE, receiver unit and on the UUT.

3. Capability to reprogram any combination of the 480 I/O to a drive, monitor, or tri-state condition at the maximum data rate of the ATE.

4. Capability of operating at dynamic rates of at least 10 Mhz at all programmable voltage levels.

5. A pattern depth of at least 16,384 on each I/O data pin.

6. Capability to unequally program each I/O to be either a driver, receiver, monitor, or clock.

7. Capability for each I/O to uniquely support bus simulation.

8. Capability to support at least two logic families of voltage levels (both high and low thresholds). Capability to program these voltage families/levels on a pin-by-pin basis across the range of I/O.

3.2.3.3 DC Power Supplies (for UUT)

DC power supplies shall have remote programming capability of both voltage amplitude and current limiting. The DC output of the power supplies shall be usable as either positive or negative sources. All DC supplies shall be remote sensed at the base of the ATE receiver described in the above section. The wiring for the UUT power supplies and grounding shall be available at the ATE receiver also discussed in the Interface to Unit Under Test section. Each power supply shall have at a minimum an accuracy of +/- (0.05% of full range + 0.05% of programmed voltage) @ 25 degrees C and +/- (0.05% of full range + 0.05% of programmed current) @ 25 degrees C.

The following supply specifications shall apply at the sensing points:

Quantity	Voltage Range	Minimum Current
1	0-7 V (nominally +5.2 V)	48A
1	0-7 V (nominally +2.0 V)	8A
1	0-7 V (nominally -2.0 V)	38A
1	0-7 V (nominally -4.5 V)	30A
1	0-20 V (nominally -5.2 V or -15.0 V)	3A
1	0-20 V (nominally +15V)	3A

This power supply will be used as a -5.2 V or as -15.0 V power supply for different circuit cards under test. Supply voltages required at the test connector are +5.2 Vdc, +2.0 Vdc, -2.0 Vdc, -4.5 Vdc, -5.2 Vdc, -15.0 Vdc and +15 Vdc.

3.2.3.4 Input Electrical Power (ATE)

The equipment shall maintain specified performance when input power is supplied from sources having the following characteristics:

Voltage:	Three-phase Wye 208 V +/- 10%
Frequency:	60Hz +/- 0.5%
Line-to-Line Voltage:	10% of the arithmetic
Variation for 3 phase system:	average of the three phases
Waveform Harmonic Content:	< = 5%

Wire sizes, voltage ratings, hardware sizes, etc., associated with the power distribution, shall be in accordance with the vendor's best commercial practice for similar equipment. The electrical power neutral line shall not be connected to the chassis of the cabinets or racks but shall maintain a minimum of one megohm isolation. Safety ground for three-wire 120 volt outlets, capable of carrying full rated current of the input power lines, shall be connected to the cabinet or rack.

The chassis of the cabinets or racks shall contain a cabinet ground bus, and the electrical power neutral line shall be connected to this bus. Convenience

outlets providing 120 VAC 60 Hz technical power and safety ground shall also be connected to the cabinet/console ground bus. The ATE system shall have at least four of the convenience outlets.

3.2.3.5 Power-Fail Protection

Power-fail protection shall be built-in providing an orderly shutdown in the event of a power interruption. Program data shall not be lost and no damage shall be induced to the logic card tester or the UUT upon loss or restoration of power.

3.2.3.6 Overload Protection

The ATE system shall be supplied with a primary power protective device and circuits, such as to protect the equipment from damage due to electrical overload. Protective devices shall be replaceable or resetable within five minutes. The ATE system shall be supplied with a protective mechanism to shutdown the ATE system if the ambient air temperature or internal air temperature exceeds Vendor's recommended maximum operating temperature of the system.

3.2.3.7 Input Power Cable and Connector

The equipment shall be supplied with a conventional power plug and cable (safety ground type with strain relief provision) between 15 and 20 feet long.

3.2.3.8 ATE Power Supplies

The ATE system shall be supplied with all self-contained power supplies to make a complete system.

3.2.3.9 Safety Features (Fail Safe)

The ATE system shall contain the following safety features:

1. Damage prevention whereby a measurement device lead cannot be connected to more than one UUT pin at a time. This is limited to the ATE system provided by the Vendor and does not include anything beyond the UUT side of the ATE receiver.

2. Damage prevention whereby a stimulus device lead cannot be connected to more than one UUT pin at a time. This is limited to the ATE system provided by the Vendor and does not include anything beyond the UUT side of the ATE receiver.

3. Time-out features

4. Power short protection to the UUT

5. Power-down features upon recognition of power-short on the ATE, interface test adaptor of UUT.

3.2.4 ATE Software Requirements

3.2.4.1 Computer Aided Engineering Interface

The Vendor shall provide a means to retransfer data from the system development CAE to the ATE. The CAE to ATE interface shall have the following capabilities:

1. Capability to process netlist from the specified CAE equipment to the ATE. The data conversion shall be complete and not require manual intervention. Specifically, the CAE to ATE interface shall provide unique and, for the most part, recognizable names on the ATE for parts, signal or node names.

2. Provide a preliminary ATE rules check on data input from the CAE equipment identifying simulation timing for clock and data performed beyond the capabilities of the ATE.

This interface shall support the latest version of the CAE vendors software released prior to the invitation of bids. In addition to supporting the current versions of the CAE vendors software, the seller shall state in writing the policy of the seller provided software updates to new versions of the CAE software. The policy should include a worst-case schedule for updating the ATE interface to future releases of the CAE software. This worst-case schedule shall not exceed 60 days for the update following a new release from Racal-Redac. The policy should also include pricing information relating to the updates.

3.2.4.2 Automatic Test Equipment User Interface

The ATE shall support a Graphical User Interface (GUI). The ATE GUI shall have the following capabilities and features:

1. User interaction in the test development process will be with a graphical-flow diagram.

2. Context sensitive menus and data input dialogues such that invalid options are not presented and invalid data entry is detected.

3. Capability to graphically interrogate and input data into the test databases. Specifically, waveforms stored in the ATE databases shall be displayed and edited graphically.

4. GUI based on an industry standard windowing technique.

5. Consistent windowing and menu across all tool sets provided by the ATE in the test program development environment and in the production testing environment.

6. Capability to graphically identify to the operator the component to be probed in a guided probing sequence using Gerber PCB data obtained from the specified CAE equipment.

7. Oriented to the English language.

Any programming or normal ATE operations not using the GUI shall be oriented to the English language. Assembly language type programs are not acceptable in the routine task of building test programs or operating the ATE.

The software (whether GUI or command line oriented) shall provide operational features such as:

1. Single step execution
2. Stop at command (breakpoint)
3. Stop on failure
4. Loop on failure
5. Recycle to top of test program
6. Automatic branching or routing

3.2.4.3 On-Line Programming Requirements

The ATE software shall contain an on-line compiler feature allowing a test program to be edited and recompiled on the ATE systems with no other computer equipment or system required. Off-line remote terminal and programming features are desired, however. All test programs shall have the capability of being written and debugged on-line, using the ATE user interface described in the section above (ATE User Interface). The on-line feature shall provide all software diagnostics, syntactical errors, etc., as feedback information to the operator within seconds.

Source listings of test programs shall be available for on-line display at any time during operation. There shall be immediate access to routines for ATE diagnostics and Unit Under Test (UUT) test programs at all times. The ATE system shall be capable of performing multiple file transfers, interchange files, as well as

editing of files. Keyboard access shall be provided to access any file stored on system memory devices independent of the automatic test program or test implementation program. An executive program shall exist which provides as a minimum the following functions:

1. Amount of memory actually in use
2. Amount of memory available
3. Storage device directory
4. Source listing of test programs
5. File history (added, deleted and changed)
6. Time-out indicators

3.2.4.4 Self Test

The test routines shall be designed within the ATE to insure that the equipment meets its published specifications and requirements specified herein. Comprehensive diagnostics shall be provided for all workstation functions and peripheral devices. Self-test shall be provided for all stimulus devices and measurement devices as well as display and memory devices.

Isolation programs shall exist to identify the failing least replaceable unit which will be replaced with a spare device.

3.3 Utilization Requirements

The system will be designed to operate continuously, 24 hours a day, 365 days a year. The actual operating period will be approximately 8 hours a day. The system will remain powered up at all times unless maintenance actions are required. This has been determined to decrease component failure due to power cycling. All scheduled maintenance will be performed during non-working hours. Provisions will be made for continued operation of the hard drives when the external supply of electrical power is interrupted.

3.4 Operational Life Cycle

The proposed system is expected to fully satisfy the customer's requirements for an extended period of 10 years. After this time, it is anticipated that advancing technology will render the computers and peripherals obsolete. The system will be designed to accommodate growth of over 50% of its current size. This will enable the customer to upgrade and increase fixtures, test programs, and peripherals as needed. The replacing of software with updated versions will be included in the life-cycle cost data. Updating software applications to the current market version will be necessary in some cases to maintain standards.

3.5 Effectiveness Factors.

The system's primary effectiveness requirements are defined as operational availability, reliability (expressed in MTBF), maintainability (expressed in Mct), and

supportability (defined by the maintenance concept). These factors will be based on historical evidence from previous users of similar Digital Automatic Test Equipment systems.

The effectiveness of the tester will be measured by the technical characteristics discussed in the following paragraphs. More specifically, operational availability, reliability, and maintainability will be the Figures of merit used to express the system effectiveness of the ATE. Due to impact to company productivity, a high mean time between failure will be established to satisfy system objectives. With ample preventative maintenance (PM) time during non-working hours, maintenance downtime (MDT) during working hours will be minimal. Before precise quantitative measures of effectiveness can be placed on the system, some assumptions must be made. The ATE system's effectiveness is dependent upon the effectiveness of each of its subsystems and their relationships. We must assume that the operators of the workstation and the tester will use the equipment in the correct manner and for the purpose that it was intended. The operator responsible for tester will require an intermediate skill level of no less than GS-7. The measures of effectiveness presented below are ignoring failure caused by inadequate performance on the part of humans involved in a "system function," as these Figures are too difficult to assess. This reference to system function only includes those necessary for operation of the system.

A MTBF of 2500 hours is a system requirement. We can assume an exponential distribution, thus the failure fate is given by = 1/1800 = .0004. Using

the exponential reliability function R(t) with a time period t of 120 hours we have:

$$R(t) = e^{-(\lambda)t}$$
$$= e^{-.0004(120)}$$
$$= e^{-.048}$$
$$= 0.951$$

Thus over a time period of 120 hours or 5-day work week the system has a reliability of .95.

The MTBF was obtained by a comparison of different vendors' information on systems of similar operational requirements. This includes failure rates, such as equipment damage rate, wear-out rate and manufacturing defects. Therefore, the mean time between unscheduled maintenance ($MTBM_u$) is found to be approximately the same as the MTBF. Preventative maintenance will be done every four weeks or 672 hours to ensure proper performance of most component parts. This does not include most organization maintenance which can be accomplished during system operation. Thus the mean time between scheduled maintenance ($MTBM_s$) is 672 hours. Given a $MTBM_u$ of 2500 hours and a $MTBM_s$ of 672 hours we can calculate the average time between all maintenance actions (MTBM):

$$MTBM = \frac{1}{1/MTBM_U + 1/MTBM_S}$$
$$= \frac{1}{1/2500 + 1/672}$$
$$= 530$$

Another substantial factor to consider in determining operational availability is the total time that the ATE is down during maintenance actions (MDT). This is expressed as an average over all maintenance actions including LDT, ADT, and M explained below. The logistics delay time (LDT) is relatively small since spare part availability and vendor service support were major considerations in the maintenance concept. Also, administration delay time (ADT), although difficult to compute, will be significantly decreased with the vendor suppling intermediate and depot maintenance. The mean active maintenance time (M) has been computed at .6 hours considering all individual maintenance actions required for each subsystem. Using the three factors mentioned above (ADT, LDT, M), a mean maintenance downtime MDT of 1.0 hour has been established for the system. Operational availability is considered a good Figure to base the system's effectiveness upon. Given an MTBF of 530 hours and an MDT of 1.0 hour the operation availability of the system (A_o) is computed by:

$$A_o = \frac{MTBM}{MTBM + MDT}$$

$$= 530/531$$

$$= 0.9981$$

This provides a standard for the system to meet.

3.6 Environment

The ATE system will be located in the lab section of the maintenance depot. The lab is atmospherically controlled with proper ventilation. The system will not

need any special environmental conditions with the exception of the cooler tubes for the UUT. The environmental conditions specifications are as follows:

Equipment Non-operating

Temperature-Ambient:	0 to 140 degrees F
Relative Humidity:	10%-90% RH, non-condensing
Barometric Pressure:	30 o 5.44 In. Hg.

Equipment Operating

Temperature-Ambient:	59 to 86 degrees F
Relative Humidity:	80% Maximum
Barometric Pressure:	Normal Atmospheric Pressure

The transportation of the system components will be performed by the vendor.

4.0 SYSTEM MAINTENANCE CONCEPT

The buyer has specified the need for a full lifetime support package that will maximize full system availability while minimizing support costs. It has been determined through a life cycle cost analysis that a maintenance contract with the tester vendor is substantially more cost effective than any plan in which the maintenance depot provides their own maintenance capability. The cost of maintenance personnel, training, acquisition and inventory costs for repair parts and support equipment are prohibitively high. A company in the business of suppling product source can spread many of these costs among customers, thus reducing the cost of individual contracts.

4.1 Levels Of Maintenance

Maintenance for the system will consist of both corrective and preventative actions. Corrective maintenance is required to restore the system or a subsystem to full operating capability after the occurrence of an operating fault. This includes any condition that reduces the system or a subsystem to less than full capability. Preventative maintenance actions are intended to prolong the life of various units and components and ensure their proper operation. Each of these two types of maintenance may be performed at one of three different levels - organizational, intermediate, or depot. Organizational maintenance will be performed on-site, usually with the equipment in place by employees of the company. Intermediate maintenance will also be performed at the facility but is accomplished by a vendor

technician who travels to the site and provides all required test and support equipment, supplies and repair parts. Depot level maintenance occurs when the vendor technician determines that a unit or component must be removed and sent out for more extensive repair. The following paragraphs provide more detail on each level of maintenance.

4.1.1 Organizational Maintenance - Maintenance at this level is limited to periodic and scheduled checks of equipment performance. Simple procedures will be provided in the form of a detailed procedural packet including guidelines and tools for keeping maintenance records. Typical maintenance actions performed at this level will include cleaning, tolerance and alignment checks, built-in tests on electronic equipment, and minor adjustments as directed by the vendor maintenance instructions. The software maintenance will be performed by the same persons responsible for organizational maintenance. The maintenance contracts will require vendor training of persons responsible for organizational maintenance in addition to training on maintenance of the Software Operating System.

4.1.2 Intermediate Maintenance

Unscheduled service calls will be in response to trouble calls from the customer. The response time will be specified in the service contract at limits to maintain the systems MDT. Service visits by vendor technicians will be conducted

on a periodic, scheduled basis to perform routine preventative maintenance which is beyond the capability of organizational maintenance personnel.

4.1.3 Depot Maintenance

Maintenance actions requiring capabilities beyond that of Intermediate level will be handled by the vendor's depot. A decision may be made to either discard and replace the item or to replace it with a spare and send the faulty item to the vendor for repair.

4.2 Repair Policies

Detailed instructions will be provided in a form that will allow the organizational level maintenance personnel to quickly and easily determine the correct procedure to follow in many different situations. Preventive maintenance procedures will inform personnel how to recognize and identify faults or conditions which warrant additional action. They will indicate exactly what actions organizational maintenance personnel are to take and when to call the vendor service number for advice or a service call. System operating procedures will give system users and maintenance personnel further information on operating fault recognition and isolation and procedures for corrective action or service call criteria.

4.3 Logistic Support

An integrated logistics support plan will be devised to provide continued satisfaction to the maintenance depot through the life cycle of the ATE system. This plan places emphasis on the highest possible degree of system availability through component reliability and through quick reaction supportability should system malfunction or damage occur. This is accomplished through a supply of ready spares and spare parts and quick response service from vendor technicians. An important factor in the success of the logistics support plan is a training program for system users and organizational maintenance personnel. The maintenance plan recommended provides an easy to follow set of procedures which include diagnostic tests during system operation. In this way, system maintenance evolves directly from the operational functions of the system. More detailed technical inspections will be conducted on a scheduled basis by a vendor technician, but high service costs will be avoided by having a vendor trained customer employee perform periodic preventative maintenance procedures. Logistic support for the system includes a number of elements of support, each of which is provided in a specified form under the maintenance contract:

4.3.1 Maintenance Instructions

These are the guidelines mentioned above for guiding the maintenance personnel step-by-step through organizational level preventive and corrective maintenance procedures. They consist of individual cards for each unit and

component. These cards include not only procedures but also technical notes, tools and supplies required, required periodicity and criteria for deferring corrective action to the intermediate level.

4.3.2 Technical Data

Data required for organizational maintenance specified in the maintenance policy will be provided at no extra cost.

4.3.3 Maintenance Scheduling Tools

Scheduling aid and procedures for managing preventive maintenance at the organizational level.

4.3.4 Spares and Supplies

Needed for preventive and corrective maintenance specified for the organizational level to be provided at no extra cost to the customer under the maintenance contract.

4.3.5 Repair Parts, Test Equipment and Supplies

Required for intermediate level maintenance or depot maintenance to be provided by the vendor.

4.4 Maintenance Effectiveness (F.O.M.)

The principal Figures of merit for maintenance will be Mean Time Between Failures (MTBF), Mean Corrective Maintenance Time (Mct) and Maintenance Down Time (MDT). These Figures will help the designers to target a required level of maintainability for all subsystems, units and components and will provide a measure of the effectiveness of the system.

5.0 ADVANCED SYSTEM PLANNING

The following discussion outlines the management plan to be taken in the development of the ATE system. The unique nature of utilizing commercially available systems compared with projects in which a system is designed and built from scratch dictates that a highly modified version of the classic program management plan be employed. The two documents used in the project are the system specification (type A) and the system engineering management plan. Due to the relatively small size of the maintenance depot engineering team, an organization and staffing breakdown will not be necessary.

5.1 Specifications

Figure 11 & 12 (type A)

Figure 13 - System Functional Diagram

5.2 System Engineering Management Plan (SEMP)

Figure 14 - Milestone Chart

Figure 15 - System Engineer Process

Figure 16 - Engineering Specialty Integration

SYSTEM SPECIFICATION (TYPE A)

GENERAL DESCRIPTION OF SYSTEM FUNCTION	AN ATE SYSTEM CONSISTING OF TWO BASIC COMPONENTS: HARDWARE (TESTER, WORKSTATION, FIXTURES, PERIPHERALS, etc.) AND SOFTWARE. THE ATE SYSTEM PROVIDES FAULT ISOLATION ON ALL SYSTEM CIRCUIT CARDS DOWN TO THE COMPONENT LEVEL.
OPERATIONAL REQUIREMENTS	CAPABILITY TO TEST SYSTEM CIRCUIT CARDS ASSEMBLIES CAPABILITY TO ACCEPT A TEST PROGRAM FROM A LOGIC SIMULATOR CAPABILITY TO GENERATE ALL STIMULAS AND MONITOR RESPONSES NEEDED FOR UNIT-UNDER-TEST CAPABILITY OF A TESTING A COMMON 480 PIN CONNECTOR CAPABILITY OF SUPPORTING A GRAPHICAL-USER-INTERFACE
MAINTENANCE CONCEPT DEFINITION	ORGANIZATIONAL MAINTENANCE - PERFORMED ON-SITE BY CUSTOMER INTERMEDIATE MAINTENANCE - VENDER SERVICE CONTRACT DEPOT MAINTENANCE - VENDOR SERVICE CONTRACT LOGISTICAL SUPPORT - SUPPORT CONTRACT WITH VENDOR
SYSTEM FUNCTIONAL DIAGRAM	SEE FOLLOWING ATE SYSTEM DIAGRAM

Figure 11

SYSTEM SPECIFICATION (TYPE A)		
EFFECTIVENESS CHARACTERISTICS	SYSTEM BUDGET	$ 3,300,000
	MTBM	530 HOURS
	MDT	1.0 HOUR
	MTBF	2500 HOURS
	A	0.9981
	SKILL LEVEL	GS 7 (ORGANIZATIONAL MAINTENANCE)

Figure 12

ATE SYSTEM FUNCTIONAL DIAGRAM

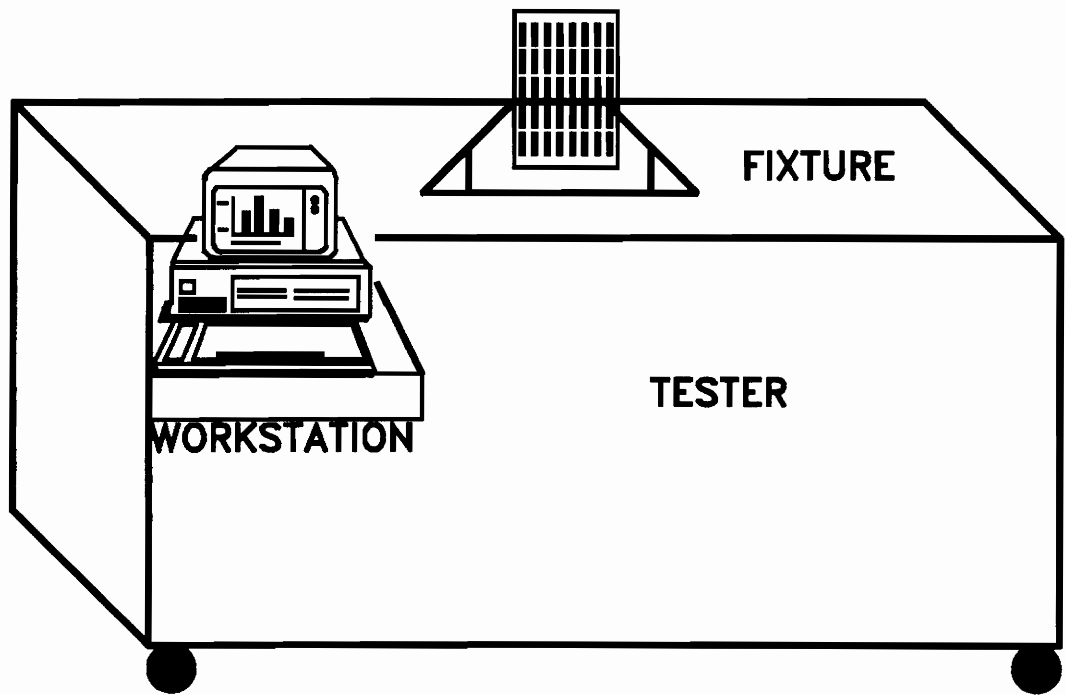

Figure 13

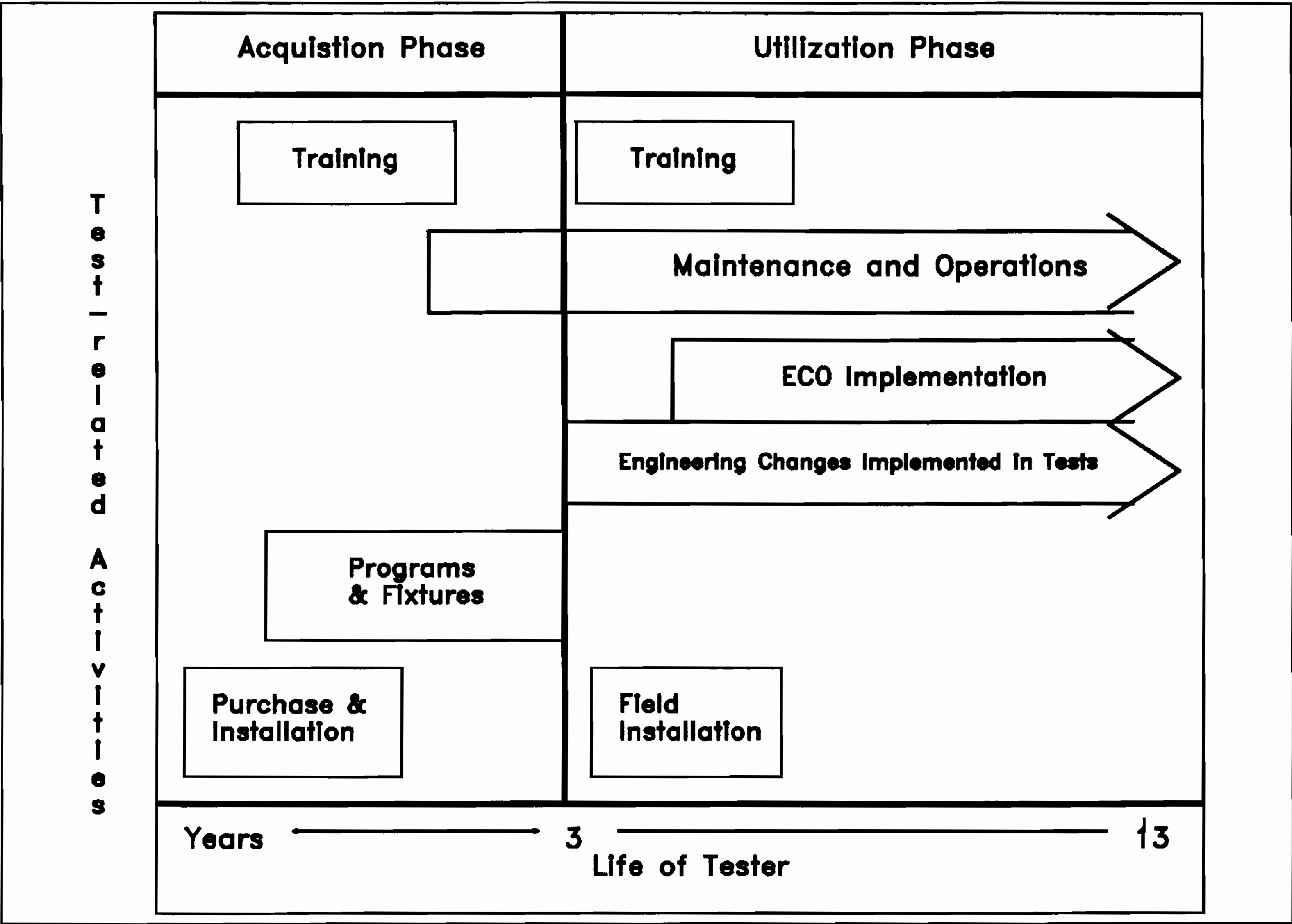

Figure 14

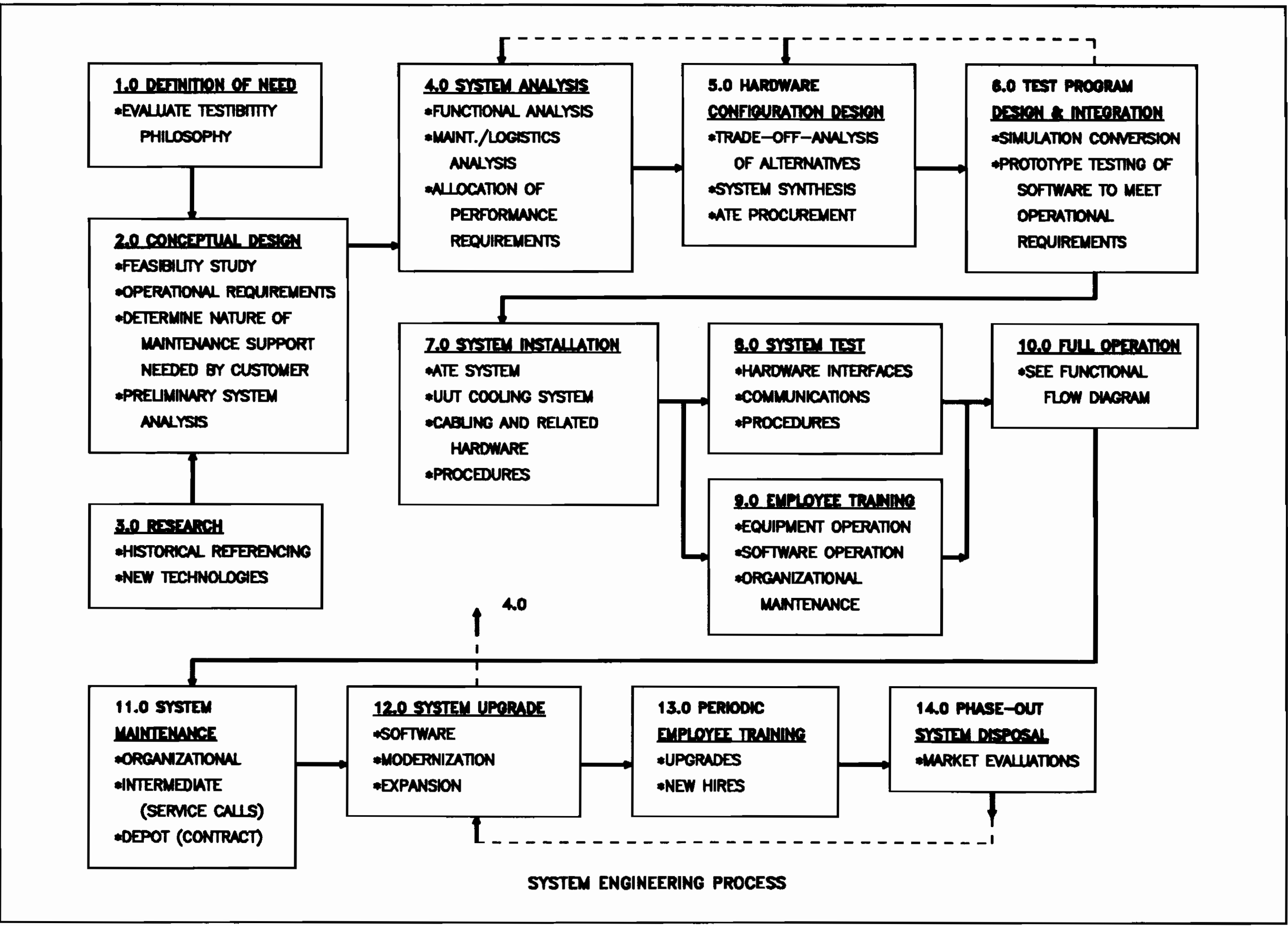

Figure 15

5.2.1 Figure 15 - Description

1. Definition of Need - E-Systems has been contracted to design and develop a next generation large scale data processing system. Another division of E-System will be responsible for the operation and maintenance of the new system for its intended 10 year life span. The maintenance depot responsible for "off-line-system" maintenance will conduct a detailed site survey of the present depot to determine the nature of current maintenance problems. Together with system engineers developing the new system, specific requirements for a Digital Automatic Test Equipment system will be developed to meet the customers' needs while attempting to reduce life cycle cost.

2. Conceptual Design - Taking the results of the site survey, the systems engineering team responsible for test began the iterative process of turning the customers' needs and constraints into a set of high level requirements. In developing these requirements, the team considered not only the performance needs for this application but also the need for maintainability and supportability. Out of the conceptual design phase began to emerge a system configuration

and also a maintenance concept with an integrated logistics support plan.

3. Research - The ATE system need is compared to the performance and reliability history of a number of components to develop the most efficient and cost effective configuration. The application of emerging technologies is also considered to enhance future upgrades and decrease system obsolescence.

4. System Analysis - This phase of preliminary design took the results of the conceptual design phase together with the latest advances from the product development line and began the process of system integration. This started with a detailed functional analysis to identify the test strategy and a diagnostic method to achieve it. Next, performance requirements were determined from the definition of need and allocated to these components. Once this was accomplished, the designers had a basis on which to select specific hardware components. Specification of components was based on the definition of a maintenance concept as well. The relationship between the maintenance concept and the system and component specification ensures that the final system design will be

maintainable and supportable as well as operationally effective from a performance standpoint.

5. Hardware Configuration Design - This is the system integration phase where performance and supportability requirements are translated into specific component configurations. This phase is similar to the detailed design phase in the classic system engineering process except none of the components of this system are to be designed from scratch. They will all be "off the shelf" items from companies with proven product lines. E-Systems system engineers will conduct trade-off studies for alternatives using historical cost and performance information gathered from other similar systems.

6. Test Program Design & Integration - This phase consist of the E-System test engineering group converting the CCA simulations over to test programs on the selected ATE. The ATE is then used to program and debug the test for each individual circuit card and its associated connection fixture. The completed card test will meet the operational requirements for percent defect detects on all assemblies. The selected ATE will be used for type II testing of the prototype test programs. The test programs will be designed for

maximum speed and efficiency. The package will then be evaluated on performance and compatibility.

7. System Assembly and Installation - During this phase, careful attention is paid to any difficulties that might indicate the need for an adjustment to the system design or to the maintenance plan.

8. System Test - This is a complete program of type III testing which will be accomplished after installation at the customer's site but before complete turnover to the customer for normal operation. It will include performance and maintainability demonstrations and a test of the procedures.

9. Employee Training - Training of E-System employees actually starts before system assembly and installation. Employees will be sent to vendor training classes for the software applications they will be using. The personnel in charge of organizational maintenance will be sent to vendor technical training classes as well as participating in and monitoring installation to receive further on-site maintenance procedure training. Once installation is complete, employees will be trained in system operation. This will be expedited by an easy-to-use GUI menu system and procedures.

10. Full Operation - After completion of performance and maintainability demonstrations, the customer will accept or reject the system. Assuming acceptance, the customer will assume full responsibility for the operation and the organizational maintenance of the system with vendor intermediate maintenance support as outlined in the maintenance concept.

11. Periodic Employee Training - Training needed for software/hardware upgrades. This also includes software application program training for new hires. System operations will be on-the-job training for new hires.

12. System Maintenance - The ATE vendor will provide maintenance support at the intermediate and depot levels in accordance with the warranty contract. At the end of this contract the customer can opt to renew or evaluate the possibility of E-Systems taking over maintenance at the intermediate and depot levels. An integrated logistics support plan will provide repair parts, ready spares, and technical data required for the system to perform the organizational level maintenance as specified in the maintenance contract.

13. System Upgrades - At any time during the projected life of the system, the customer may elect to upgrade the installed configuration due to company expansion, new technology, needed capability, or system overloading. All elements of the system are designed with the capacity to accept expansion or addition of components. The ATE will have unused card slots as well as I/O ports for external hardware. The workstation is essentially designed independent from the tester and may be upgraded independently.

14. Phase-Out and Disposal - Since it is impossible to predict at what time the system will become completely obsolete, it will be necessary to periodically evaluate the market. This will enable the customer to decide whether to phase out parts of the system and replace or upgrade others. At the end of the projected life cycle, the system should again be compared to the current standard and a decision made of the cost effectiveness of further upgrades or disposal.

ENGINEERING SPECIALTY INTEGRATION

RELIABILITY AND MAINTAINABILITY FACTORS

CONCEPTUAL DESIGN AND ADVANCE PLANNING STAGE	PRELIMINARY SYSTEM DESIGN PHASE	CONFIGURATION DESIGN AND CONSTRUCTION PHASE	OPERATIONAL USE AND SYSTEM SUPPORT PHASE
QUANTITATIVE AND QUALITATIVE RELIABILITY REQUIREMENTS FOR SYSTEM (MTBM, , MTBF, MDT) AND RELIABILITY PLANNING	ALLOCATION OF RELIABILITY REQUIREMENTS, RELIABILITY ANALYSIS AND TRADE-OFFS, RELIABILITY PREDICTIONS, FORMAL DESIGN REVIEW	RELIABILITY ANALYSIS AND TRADE-OFFS, RELIABILITY PREDICTIONS, RELIABILITY TEST AND EVALUATION; RELIABILITY DATA COLLECTION, ANALYSIS, AND CORRECTIVE ACTION, FORMAL DESIGN REVIEW AND APPROVAL	RELIABILITY DATA COLLECTION, ANALYSIS, AND EVALUATION; SYSTEM MODIFICATION AS REQUIRED
MAINTENANCE CONCEPT, QUALITATIVE AND QUANTITATIVE MAINTAINABILITY REQUIREMENTS (MTBM, MTBF, MDT), MAINTAINABILITY PLANNING	ALLOCATION OF MAINTAINABILITY REQUIREMENTS, MAINTAINABILITY ANALYSIS AND TRADE-OFFS, MAINTAINABILITY PREDICTIONS, FORMAL DESIGN REVIEW	MAINTAIN ANALYSIS AND TRADE-OFFS, MAINTENANCE ENGINEERING ANALYSIS, MAINTAINABILITY PREDICTIONS, MAINTAINABILITY DEMONSTRATIONS, MAINTAINABILITY TEST AND EVALUATION; MAINTAINABILITY DATA COLLECTION ANALYSIS, AND CORRECTION ACTION, FORMAL DESIGN REVIEW AND APPROVAL	MAINTAINABILITY DATA COLLECTION, ANALYSIS, AND EVALUATION; SYSTEM MODIFICATION AS REQUIRED

Figure 15

6.0 SYSTEM FUNCTIONAL ANALYSIS

At this point we are ready to initiate the functional requirements definition process. The organizational structure of the maintenance depot, although not part of this study, will be explored in order to thoroughly define the operational activities of the ATE system. The process will help to initiate the further refinement of ATE system requirements. Based on the study completed to this point we will state that the overall system requirement is to design and implement an integrated Digital Automatic Test Equipment System for the next generation system.

6.1 Operational Activities

This process initiation is shown in Figure 17. Note that the identification of operational activities follows the organizational structure of the maintenance depot enterprise. As operational functions are further identified the operational activities may be subject to change or modification. Of importance is the information flow depicted in Figure 17. At this point, the intent is that all operational activities be fully integrated with each other with links between the elements representing either tasking or the transfer of information. The operational functions are defined below:

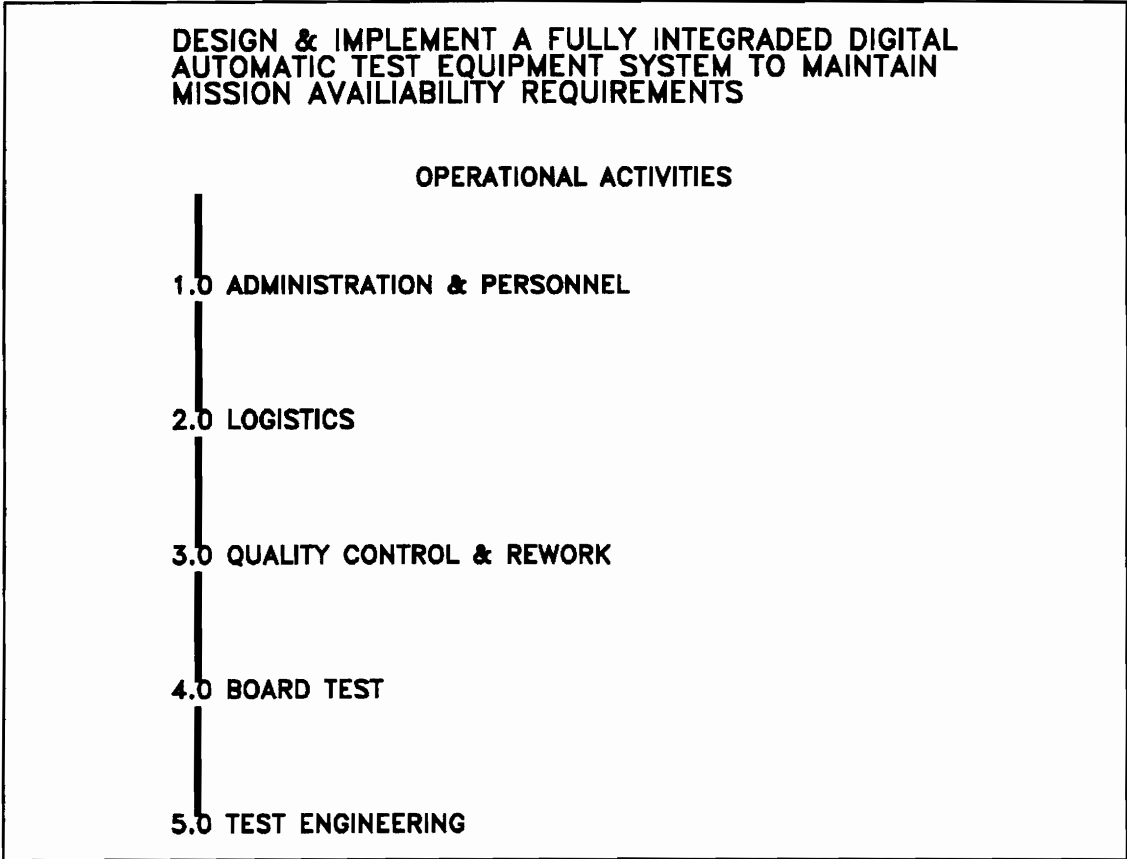

Figure 17

1. Administration & Personnel

This functional area includes accounting, finance, personnel, secretarial support and payroll.

2. Logistics

This functional area includes shipping and receiving, inventory and purchasing.

3. Quality Control & Rework

This functional area includes incoming and outgoing board inspection, component removal and replacement, and overall process quality.

4. Board Test

This functional area consist of Circuit Card Assembly verification and testing through the use of Automatic Test Equipment.

5. Test Engineering

This functional area includes card test programs.

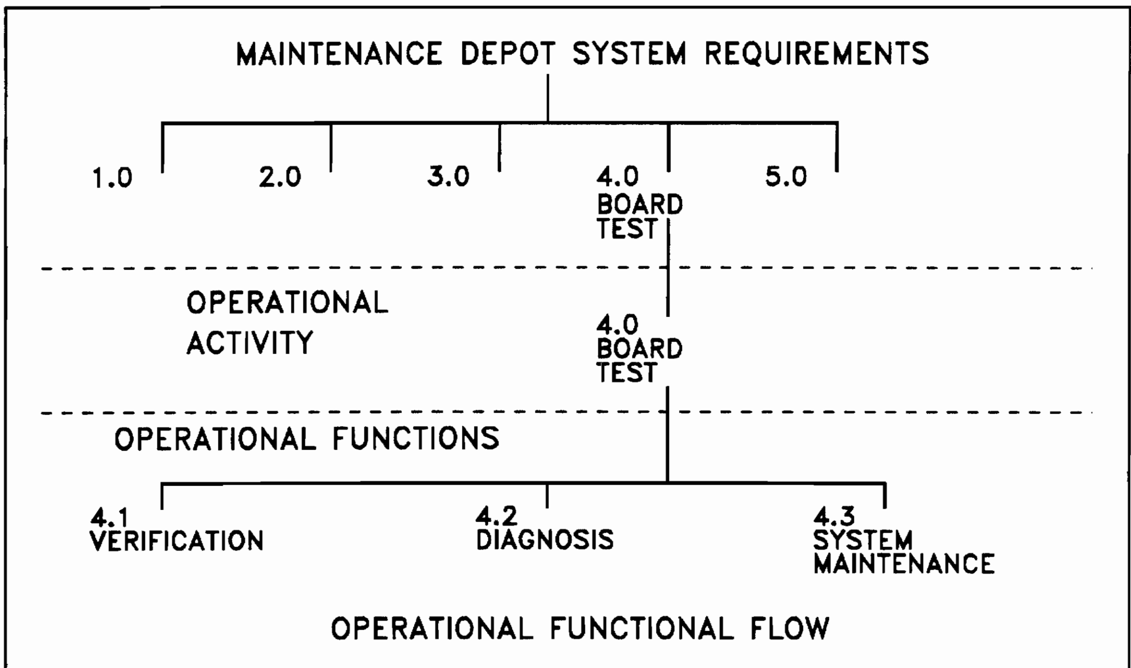

Figure 18

For the purpose of this study we will examine in detail the operational functions that are directly impacted by the integration of a new ATE system. We will begin by further examination of the operational functions of the operational activity known as Board Test. Refer to Figure 18 which further defines the operational functional flow for our maintenance depot system. At this point it is important to remember that we want to satisfy our overall ATE system requirements from the top down through the entire system. Therefore, when we begin to design the implementation of our integrated testing system using the ATE, needs must be satisfied at every level. For example, requirements will have to be addressed and satisfied at operational function 4.3 which we have defined as the system maintenance function.

6.2 Operation Functions and Subfunctions

As the operational functions for each of the selected operational activities begin to come into focus the ability to further breakdown each operational function into further subfunctions will present itself, (refer to Figure 19). The subsequent breakdown of subfunctions will begin with Board Verification. The verification subfunction begins with the installation of the Unit-Under-Test into the ATE. The performance of the UUT is examined using its individual test program. A GO/NO-GO scenario determines the necessity for additional ATE diagnostics or the need for In-System-Testing.

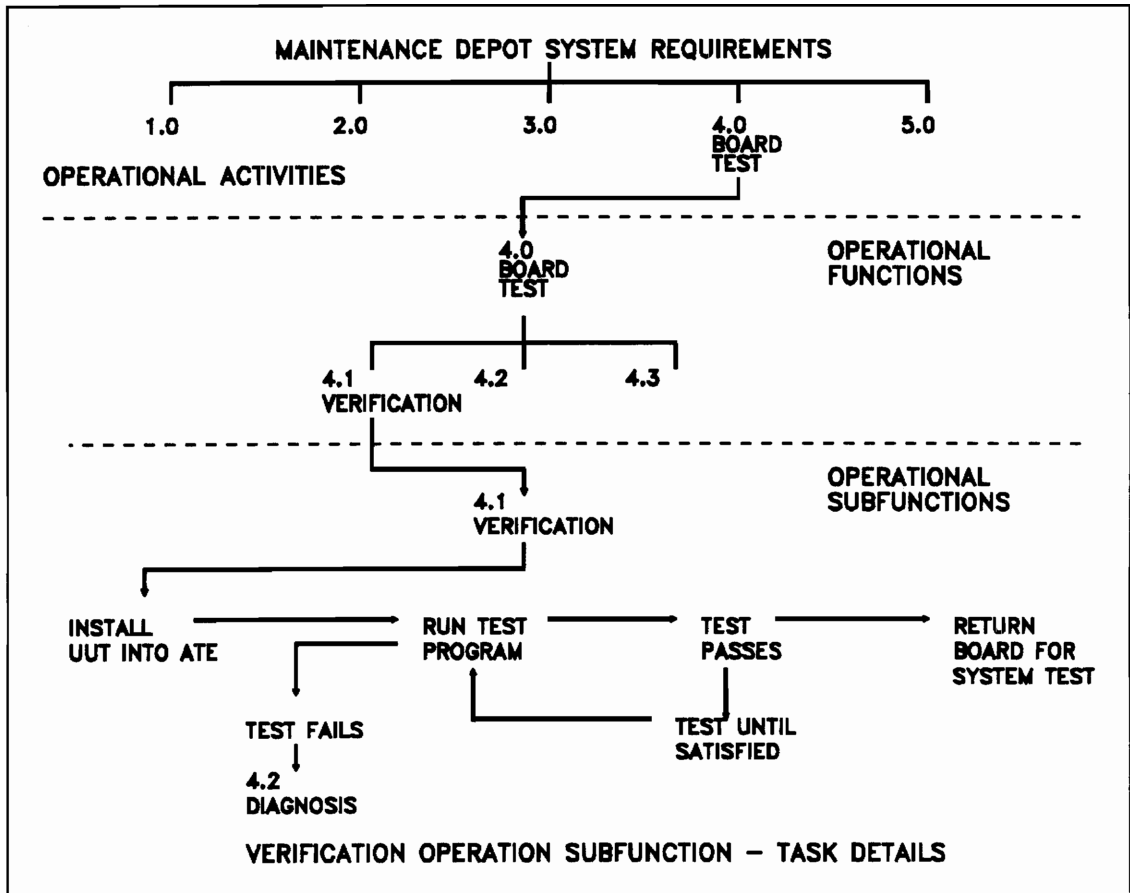

Figure 19

The diagnostic subfunction begins with the repeatability of failure symptoms (refer to Figure 20). A repeatable or hard fault can then be troubleshot from the functional level down to the component level. The final step is the return of the unit to the Quality Control & Rework function for repair, leading in a feedback loop to the function Board Test.

The final function of the maintenance depot system to be evaluated is Test Engineering due to its obvious connections to the Automatic Test Equipment System. The Test Engineering function is responsible for all aspects of the ATE test programs. In the present maintenance environment, this task entails the

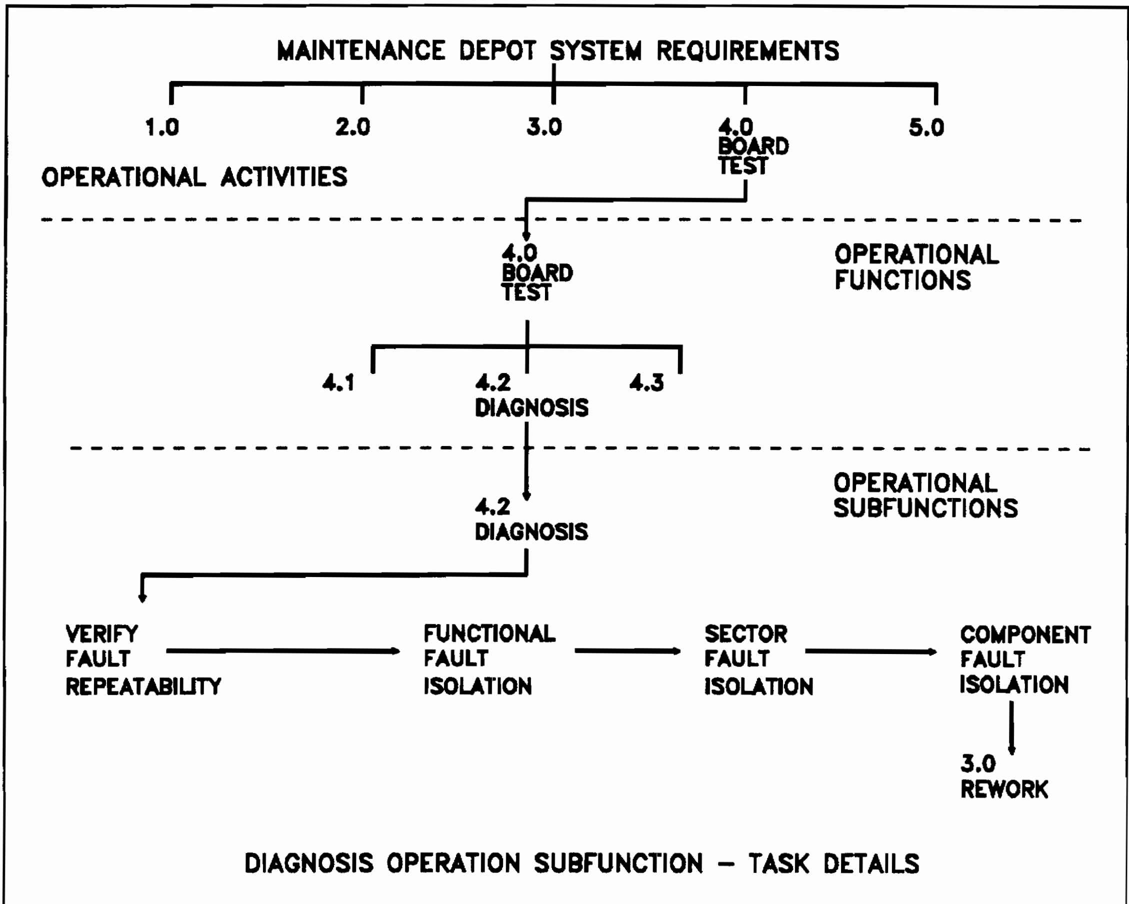

Figure 20

intimate knowledge of over a thousand card test and their idiosyncracies. The group is small and consists of higher labor grade personnel with high skill levels. Test Engineering will be tasked with learning the new system's card test programs. The developed expertise will then be used to properly train ATE operators and solve higher level testing problems.

The card test programs will be developed by E-Systems factory test engineers during the R & D phase. During system operation these engineers will

be available for direct and indirect intervention into problems outside the expertise of the maintenance test engineers.

6.3 System Maintenance Functions

Within the maintenance depot it has been proposed that the responsibility for systems maintenance rest within the Board Test element. That being the case maintenance considerations will have to include both the system hardware and software of the selected ATE system. Figure 21 proposes a scheme that will provide various levels of maintenance support for the system.

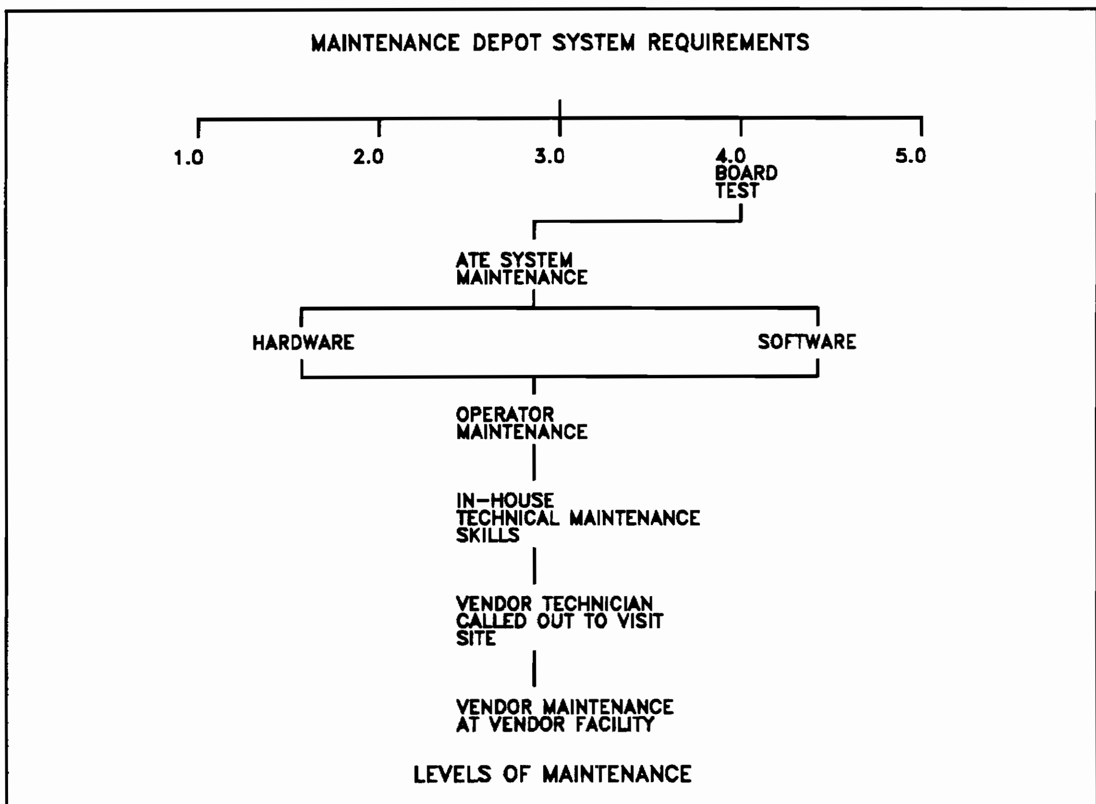

Figure 21

6.3.1 Levels of Maintenance

The first level proposed is the operator maintenance function followed by organizational capability to perform minor maintenance and repair on the system components. Once the skill level required is beyond that of the in-house capability, then a vendor supplied technician could perform a site visit to repair and or evaluate the equipment. If on-site repair is not possible, then the next step is the physical removal of the defective subsystem by the vendor technician and a timely sparing or repair at the vendors depot maintenance.

6.3.2 Training

Looking closely at the operator training function shows that the role of the systems maintenance element is to insure that operators are properly trained. Training will include such elementary skills as visual inspection, operational check-out for the ATE system and caring for the system equipment. As part of the operational check-out, the operator must decide if the system is functioning satisfactorily or if malfunction has occurred. In the event that malfunction is discovered, then the problems will be directed back to the system maintenance function. Specifically the problem will be directed for further test and evaluation. This organizational flow is shown on Figure 22.

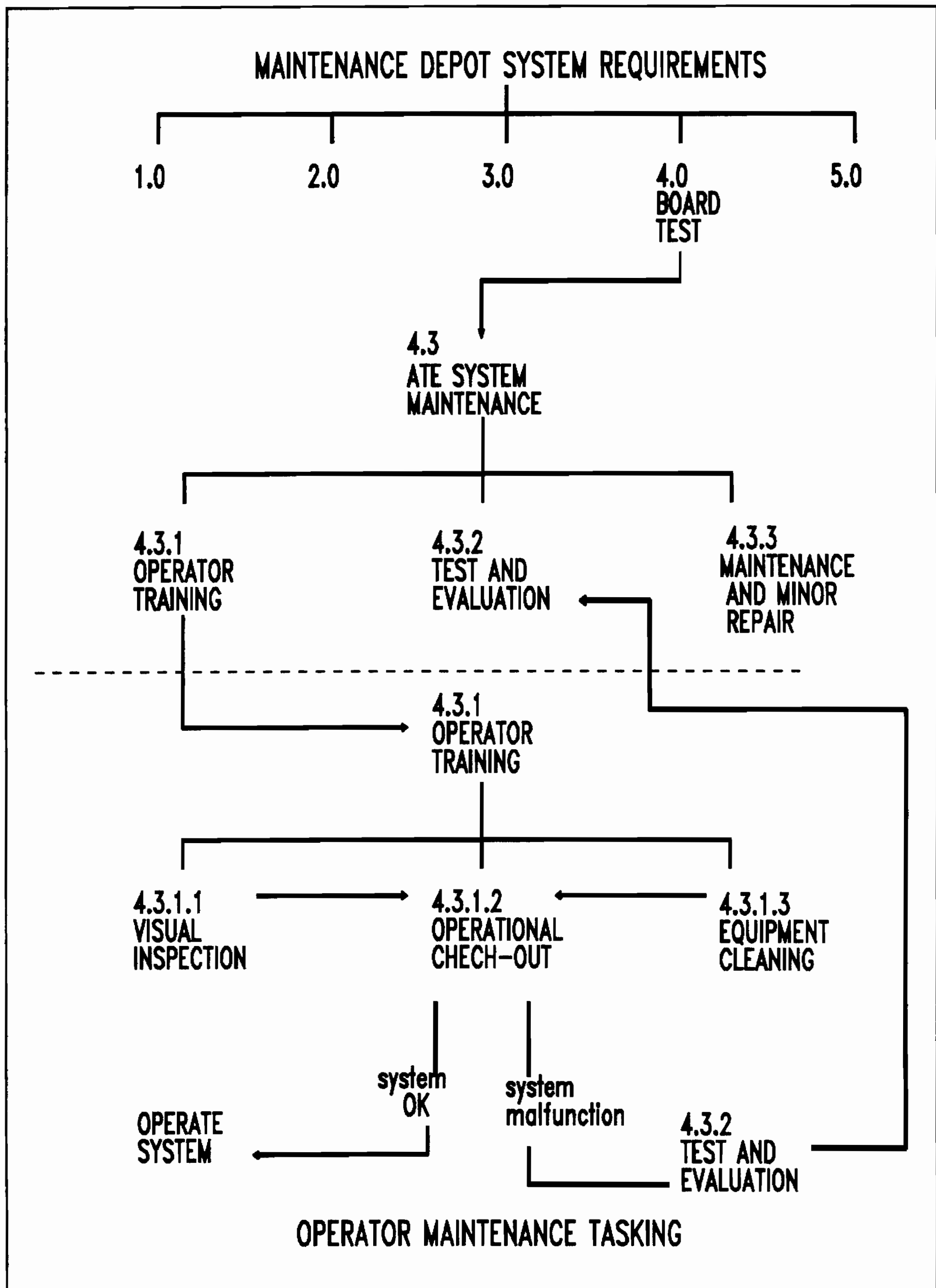

Figure 22

6.3.3 Test Evaluation and Repair

The test and evaluation task can be triggered by either operator reported malfunction or by the implementation of a scheduled preventative maintenance program. In either case, what happens after test and evaluation is the same. Expertise should exist within the organization to perform minor maintenance and repair. This can consist of minor servicing, external adjustments and the removal and replacement of system components. Once this level of effort has been expended the subsystem or component is either returned to service or it is determined that a higher level of maintenance skill is required. The first stage beyond in-house repair could be the visit of a vendor's representative to the operational site (refer to Figure 23). The vendor's technician will either correct the problem or refer the problem to the next higher level of maintenance ability at the vendor's facility. The referral to the vendor's facility could occur because of the lack of skill on the part of the vendor's technician or because certain tests and repairs can only be performed at the vendor's shop. The vendor will either repair the unit or, if repair is not possible the unit will be replaced with a new or remanufactured unit. Note that at every level the possibility for repair exists. If repair is successful the unit is then returned to either service or spare inventory.

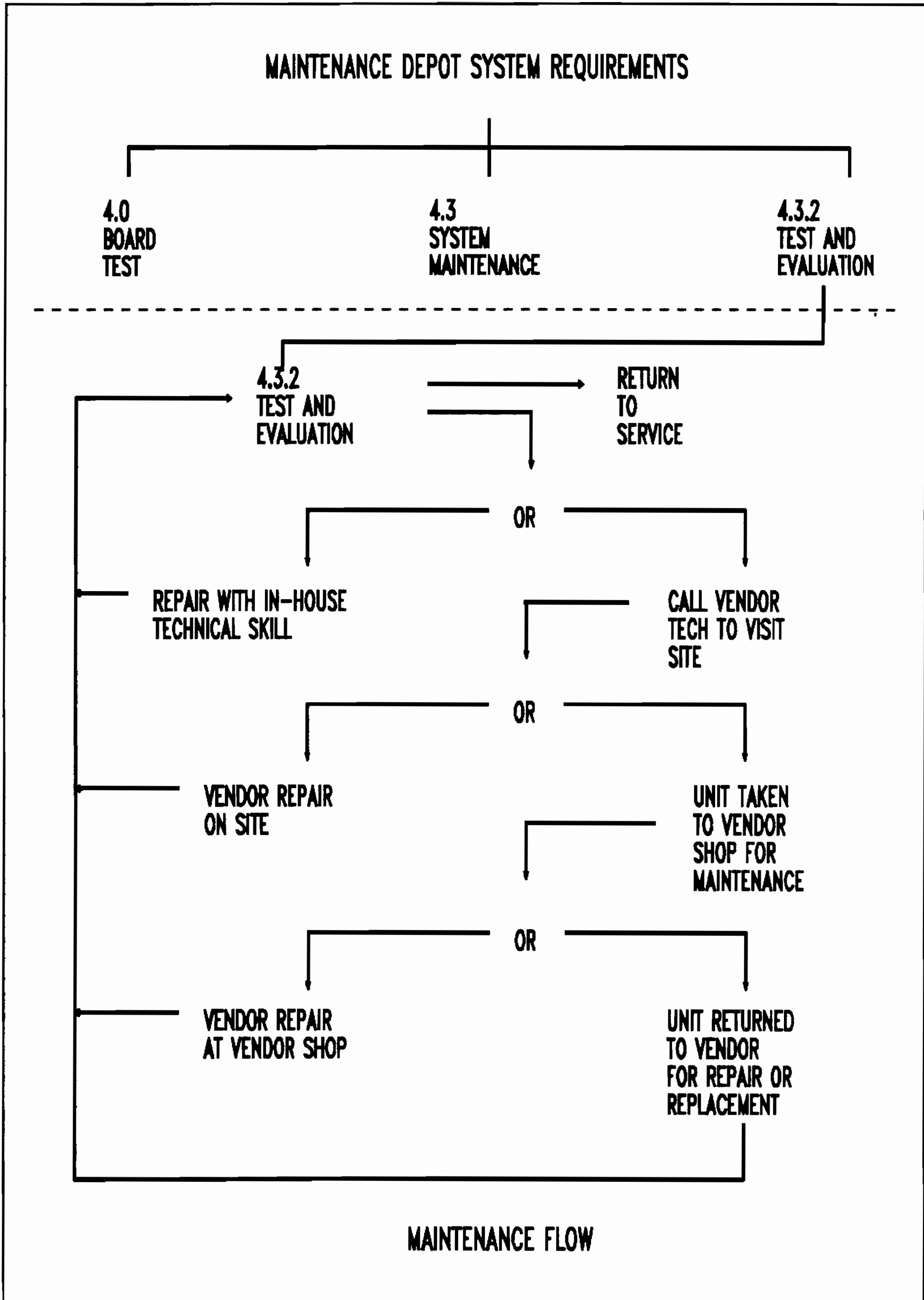

Figure 23

7.0 ALLOCATION OF REQUIREMENTS

Thus far, there has been a narrow focus on the operational functions and the maintenance functions that would be required to describe the ATE system activities. At this point, we can begin to identify system components that may be available to satisfy the proposed operational and maintenance function.

7.1 Major System Components

First, we will consider the major elements of the system components. These components are shown on Figure 24 and consist of:

1. Workstation Location (If not connected to ATE)
2. Hardware Placement Location
3. Support Furniture
4. Hardware
5. Software
6. Support Personnel (Internal)
7. Training
8. Vendor Support (External)

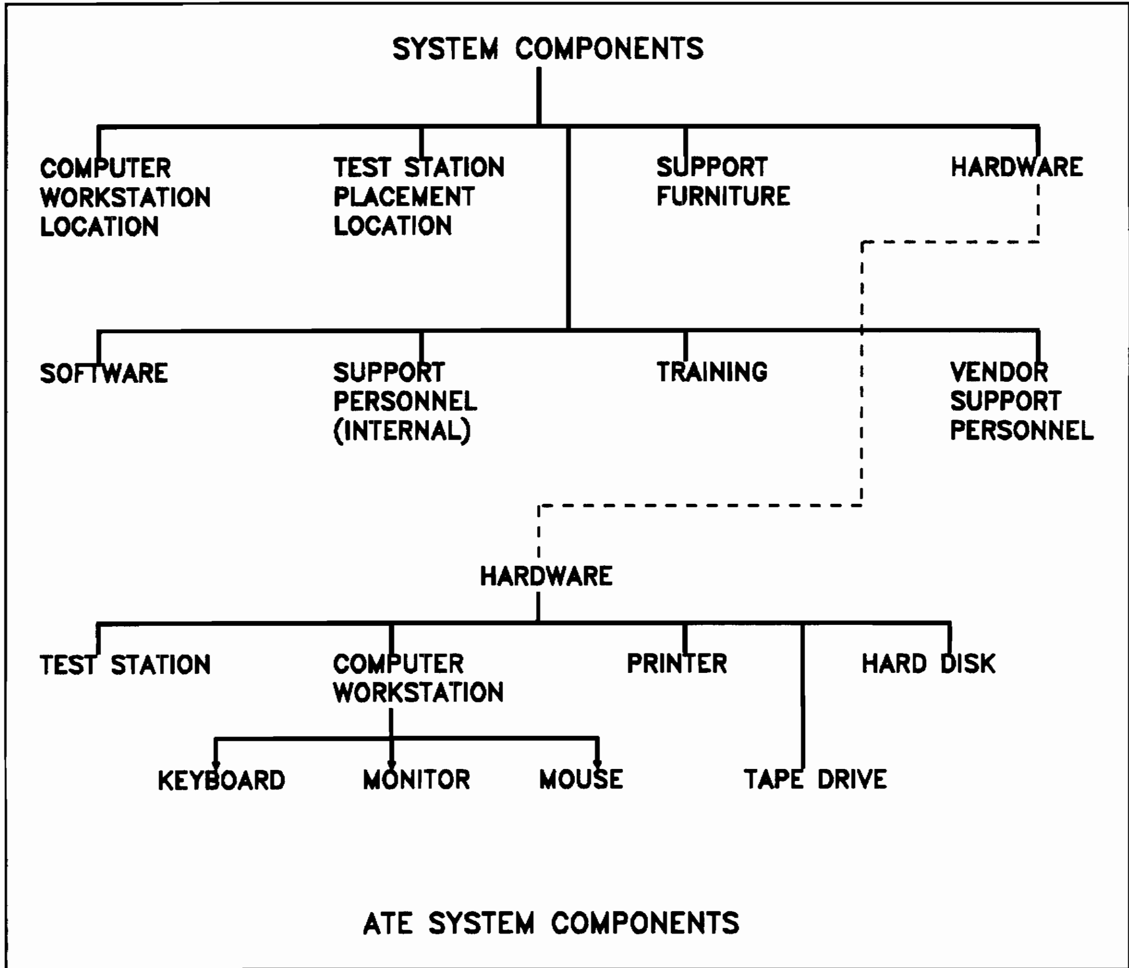

Figure 24

7.1.1 Hardware Available to Support Functional Requirements

A close examination of item 4 "Hardware" will provide us with the following preliminary list of equipment that could be made available to support the functional requirements (refer to Figure 24).

The Digital ATE shall include the following testing capabilities:

- Test Station
- Computer workstation
- Peripherals
    1. Color monitor
    2. Hard disk
    3. Tape drive - useable for uploading and downloading of test programs to the ATE
    4. Keyboard
    5. Mouse or Track Ball
    6. Printer

All the of the elements under the heading "system components" in Figure 24 are related to one another to varying degrees. All system hardware will occupy "space" and that space will need to be identified. This may mean use of an existing facility of the requirement for the construction /lease/rental of an new facility.

7.2 Miscellaneous Allocation Considerations

As decisions are made as to the installation locations of the hardware, other concerns will become apparent. These will include environmental concerns (AC

requirements) and power requirements to name a few. The installation of hardware also includes identifying the location for the test station, computer workstation, and all additional support equipment. These locations will typically require continuous and ongoing operator access. This will also include any special furniture required to support the equipment. Employees will then require training on the use of the equipment in addition to the use of the software. An in-house support capability will be created to provide technical assistance on both the use of the hardware and the software including test programs. Realizing that the in-house capabilities will have limitations it will be important to arrange for external support as required. External support could be required for both the system's hardware/software and the card test programs.

7.3 System Functional Requirements and Allocation

It is at this point where we begin to identify the functional requirements in greater detail and begin the process of allocating these requirements among the elements of the system.

7.3.1 The Overall ATE System

After careful study the following initial parameters were initially established for the ATE system (see Figure 25). The mean time between maintenance (MTBM) was set at approximately 500 hours, the maintenance man-hours per operating hour (MMH/OH) was set at 0.0166, skill level fixed at a GS-7 and ATE

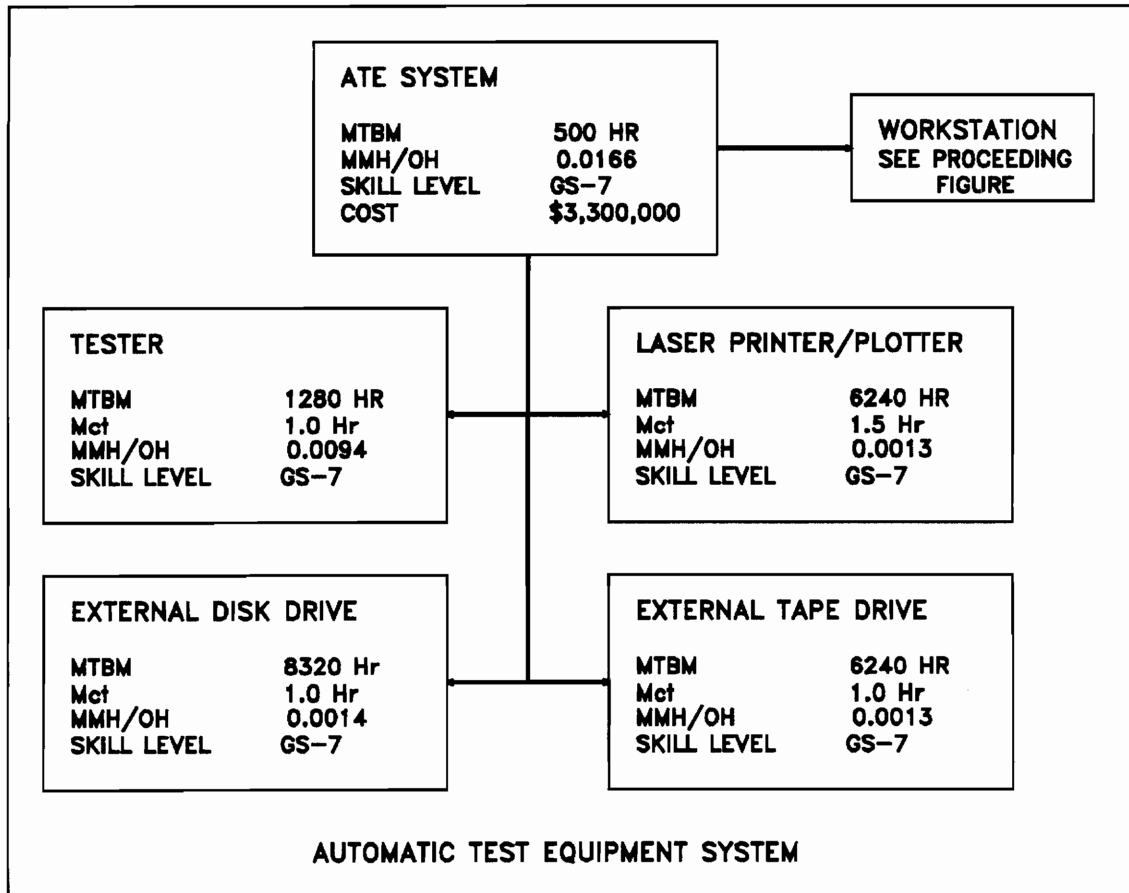

Figure 25

system cost at $3,300,000. This was arrived at through a top-down and bottom-up analysis. A discussion of this procedure is warranted and is a follows:

•**Tester:** The MTBM for this unit was set at 1280 hours (40 hours x 4 weeks x 8 months) with a mean corrective maintenance time (Mct) established as one hour. MMH/OH for the unit was set a 0.0094 (12 hours/ 1280 hours).

•**Printer:** The MTBM for this unit was set at 6240 hours (40 hours x 52 weeks x 3 years) with a Mct established at one and one half hours. MMH/OH for this unit was set at 0.0013 (8 hours / 6240 hours).

•**External Tape Drive:** The MTBM for this unit was set at 6240 hours (40 hours x 52 weeks x 3 years) with a Mct established at one hour. MMH/OH for this unit was set at 0.0013 (8 hours / 6240 hours).

•**External Disk Drive:** The MTBM for this unit was set at 8320 hours (40 hours x 52 weeks x 4 years) with a Mct established at one hour. MMH/OH for this unit was set at 0.0014 (12 hours / 8320 hours).

•**Workstation:** The MTBM for this unit was set at 1620 hours (40 hours x 40 weeks) with a Mct established at one hour. MMH/OH for this unit was set at 0.0032. This unit was then broken down into four assemblies (see Figure 26) - the computer, monitor, keyboard, and mouse assemblies.

- **Computer:** The failure rate per hour was set at 1 failure per 8320 hours of operational life or 0.0001. MMH/OH was set at 0.0014 (12 hours / 8320 hours).

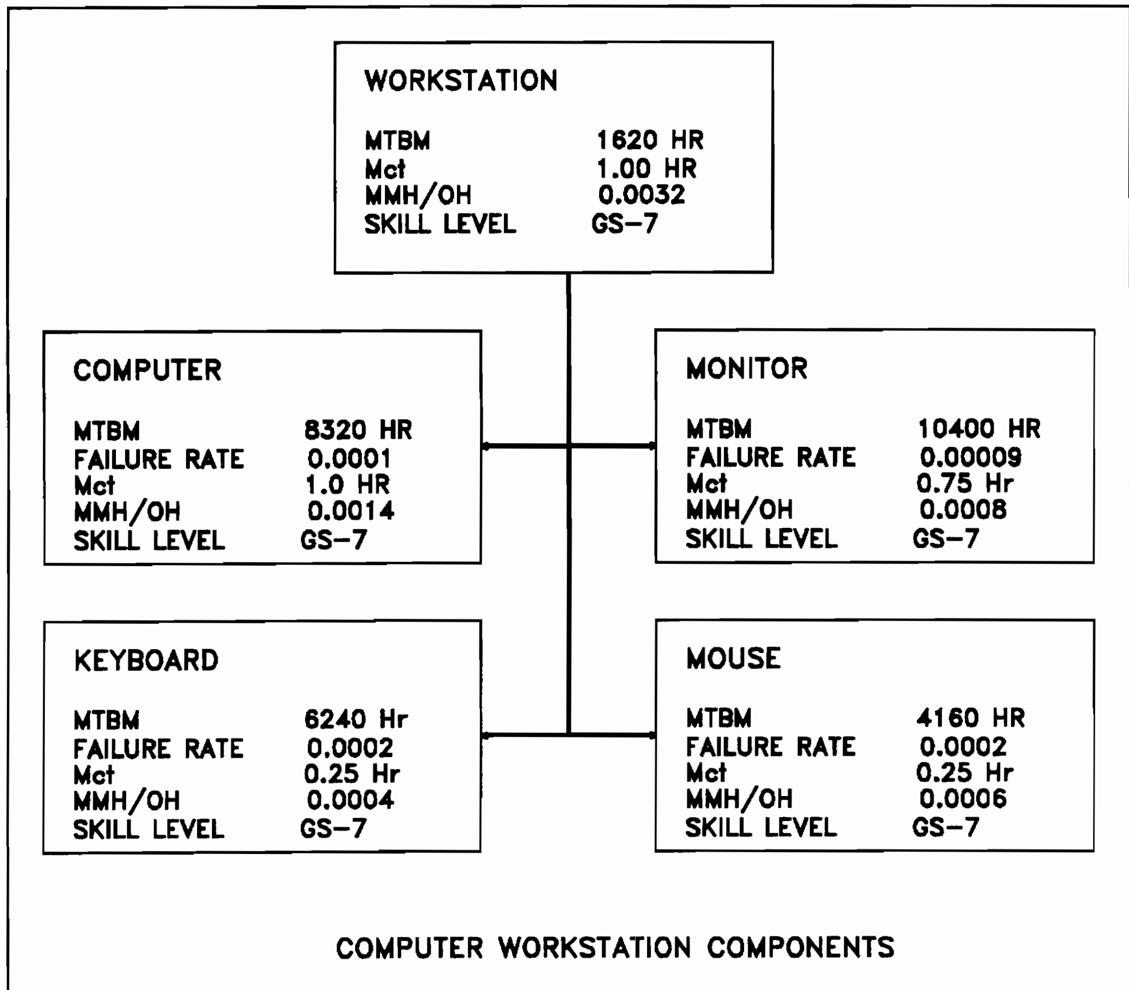

Figure 26

- **Monitor:** The failure rate per hour was set at 1 failure per 10400 hours of operational life or 0.00009. MMH/OH was set at 0.0008 (8 hours / 10400 hours).

- **Keyboard:** The failure rate per hour was set at 1 failure per 6240 hours of operational life or 0.0002.

MMH/OH was set at 0.0004 (2.4 hours / 6240 hours).

- **Mouse:** The failure rate per hour was set at 1 failure per 4160 hours of operational life or 0.0002. MMH/OH was set at 0.0006 (2.4 hours / 4160 hours).

8.0 TEST STRATEGY\PLAN TRADE SUMMARY

The ATE system trade study began with the evaluation of the three test strategies: functional, in-circuit, and cluster. Analysis of these testing approaches against initial costs and operational repair costs revealed functional testing to have the lowest overall life cycle cost. The next step was the selection of an optimum diagnostic solution for the fault isolation of failed GO/NO-GO functional tests. A decision matrix was utilized to highlight weighted modeling criteria of our ATE system requirements. The results of the modeling indicated that the probe-oriented diagnostics would best suit our system specifications. The final step was the decision of using guided probe with or without the fault dictionary capability. An evaluation of the state of today's guided probe and fault dictionary hardware and software showed considerable benefits from the pairing. These benefits include enhanced VLSI capabilites, reduced fault isolation time, and an increase in diagnostic accuracy. These benefits will help in reducing costly "in-system" repair time. The cost of adding the fault dictionary is considered moderate since full-card simulation will be performed as part of board design and independent of the test method. Therefore, fault grading is the only added CAE cost.

8.1 Model Considerations

It is at this point in the preliminary design process that system modeling would be advantageous. However this might best be accomplished through a vendor provided demonstration model. This could be achieved by visiting a similar

manufacturing enterprise with a comparable system in use. It is through this method that the actual satisfaction of all proposed functional and operational requirements could be demonstrated. This procedure can be further enhanced by:

- Simulation of various operational requirements which are introduced into the system.
- Observing system responsiveness, speed, reliability, ease of use, etc.

By observing the various Automatic Test Equipment systems in an actual real-time operating environment, an assessment of the actual operating characteristics of each system can be made. Significant differences between the systems should be noted and made part of the evaluation and selected process.

9.0 ATE CANDIDATE EVALUATION

The final step in the preliminary design is the initial evaluation of candidate ATE systems against system requirements. These five ATE systems were selected from a larger set of similar systems after meeting certain minimal criteria. These criteria consisted of functional test capabilities, digital tester, and data rate capabilities of at least 10 Mhz. As we begin to explore the cost effectiveness of

INITIAL ATE CANDIDATE COST	
TERADYNE L393/397	$ 1,780,000
TERADYNE L353/357	$ 1,470,000
HEWLETT-PACKARD	
(50 Mhz)	$ 467,000
(100 Mhz)	$ 951,579
(200 Mhz)	$ 1,394,000
SCHLUMBERGER	$ 957,675
SUMMATION SIGMASERIES	$ 350,000

Figure 27

the various systems it will be helpful to begin with the first cost for the five candidate systems (Figure 27). These first costs will be used during the detailed design phase to perform a full life cycle analysis on the primary candidates. The initial evaluation will begin by highlighting noteworthy capabilities of each tester and specifying their advantages and disadvantages. Appendix A details the technical specifications of each tester.

9.1 Teradyne L393/L397

The Teradyne L393 ATE is an ECL based high data rate (40 Mhz) functional tester with the capability of reaching a data rate of 80 Mhz in a 2 to 1 interleave mode. The L393 is essentially the same ATE with the capability to support twice as many channels as the L393. The L393 tester consists of a "per pin" architecture with 32 K of RAM behind each channel for patterns and control. All levels of Fault Trace Diagnostics and Fault Dictionary are fully supported.

Advantages\Disadvantages

The Teradyne L393 is considered to be one of the best functional testers on the market today. It allows for both speed and diagnostics in one box. At data rates up to 80 Mhz the tester can catch many timing related problems that slower testers are not capable of measuring. Also, the fault trace and fault dictionary diagnostics packages can reduce card debug/repair times to less than 30 minutes on most cards. The speed, signal integrity and functionality of this ATE allow it to be useful as a design verification tool as well as a "card tester". The 80 Mhz data rate can run most cards "at speed," and the diagnostic tools can help to insure that the card runs as predicted by the simulation before it is ever plugged into the system. This capability reduces risk to the backplane by catching manufacturing faults before the card is plugged in. Using the diagnostic capabilities, it can also reduce the time to debug a problem in the card (part failure), design (timing problems), or simulation (to ensure simulation matches the actual hardware).

9.2 Teradyne L353/L357

The Teradyne L353 is a CMOS based In-Circuit tester capable of data rates up to 20 Mhz. The L357 is essentially the same ATE with the capability to support twice as many channels as the L353. This tester can be configured to provide functional, In-Circuit, or combinational testing. Teradyne provides cards for either 1 to 2 or 1 to 10.5 multiplexing. The greater amount of multiplexing capability reduces the actual channel count thus reducing functional testing capability. Each channel is supported by 16K of Ram for patterns and control. The L353 incorporates the same diagnostic capabilities as the L393 for any functional block testing that might need to be done.

Advantages\Disadvantages

The Teradyne L353 allows both functional and in-circuit testing to be done on the same tester. The 20 Mhz data rate is among the fastest in the in-circuit environment and is fast enough for most functional applications. This tester also has the capability to be upgraded to run at the same speeds as the L393, but in doing so, the tester can only perform functional testing, all in-circuit capabilities will be lost. The support of a Fault Dictionary and the Fault Trace diagnostics enhances the debug capability for any functional blocks being tested, thus reducing debug/repair time to a minimum. Design verification is somewhat limited on this ATE due to the slower data rate.

9.3 Schlumberger S790

The hardware modularity of the S790 allows for custom configuration for either functional, in-circuit, or combinational testing. The basic modules of this digital system are the user interface (SUN 3 Workstation), tester controller (68020 up), universal digital pins and digital timing sub-system. The controller handles the flow of information, compiles test programs, controls the tester peripherals and, in general, executes all test activities. The digital sub-system allows up to eight timing event frames with up to eight timing waveforms each. The pin electronics and timing facilities allow for data stimulus and capture rates of 10 Mhz (Full Format Mode), 20 Mhz (Interleave Mode) and 40 Mhz (Data Mode). In Full Format Mode, all pins are independent and all timing capabilities are available. In Interleave Mode, 2 pins are interleaved as 1 giving half as many channels at twice the data rate with full timing capability. In Data Mode, pins are independent, but timing capability is reduced. Each channel has 16Kx4 RAM in both Format and Interleave Modes. In Data Mode, each channel scheme allows more pins to be used for holding unused signals at user-defined levels. Full diagnostics are supported by the ANALYST and TACTICIAN software packages for the S790.

Advantages/Disadvantages

The Schlumberger S790 can achieve a data rate of 40 Mhz, but at this rate, bi-directionals cannot be switched and other timing features cannot be accessed. The next lower speed (20 Mhz) offers full timing capability but with half as many

pins. At 10 Mhz all capabilities of the tester are available to all pins. The S790 can mix modes on different pins allowing maximum speeds on critical pins. If an appropriate setup can be obtained, then optimal speeds can be reached for card design verification. Otherwise, if 10 Mhz is the only available configuration, speed becomes a limiting factor for both design verification and test development. The most impressive part of the S790 system is the software. The heart of the S790 is the Computer Aided Test Engineering (CATE) workstation. CATE utilizes an interactive graphic environment for its test development and diagnostic tools. Tools such as the SCHEMATIC MANAGER and DIGITAL WORKBENCH assist in design verification, test development and card debug. CATE interfaces to the simulator through a software package called CADDIF. Through a combination of Simports and Testports a bi-directional link between the tester and the CADAT simulator is obtained with a waveform editor used to change stimulus patterns for both.

9.4 Hewlett-Packard HP82000

The HP82000 is an ASIC tester that can be reconfigured to achieve functional card test. This system can be configured for either 50 Mhz, 100 Mhz, or 200 Mhz operation. There is an approximate doubling of system cost with each doubling of operating speed. At maximum speed, each pin can drive data in Delayed Non Return to Zero (DNRZ) format and compare data in edge strobe mode. Each channel in multiplex mode (2 pins per channel) uses additionally the resources of the adjacent channel. Drive formats are DNRZ, RZ and R1. Edge and

window strobe modes are offered on the receive side. For the 50 Mhz configuration, each channel can have 256k of memory for vectors and sequences. Diagnostics other than GO/NO-GO are not supported.

Advantages/Disadvantages

The HP82000 is a purely functional GO/NO-GO test system built for ASIC testing. Being an ASIC tester, no functional diagnostic tools are available with this system other than card (chip) edge verification. Any diagnostic tools needed would have to be developed. The advantages of this system are the lower cost for the 50 Mhz speed range, the signal integrity and signal generation capabilities. No post-processor between CADAT and the 82000 currently exists; a program would need to be written to translate from CADAT vector files to HP82000 input and output files.

9.5 Summation SigmaSeries

This system is a custom configuration for strictly functional testing. The digital stimulus and response of this system is handled by DSR10 cards through pods connected to the back of the test head. The DSR10 cards can provide 20 Mhz data rates with 16K RAM behind each pin for only the logic family associated with the connected pod. Pods must translate from the received logic family to the drive/measurement system. This method lessens the need for active parts on the personality adapters; however, it is not a per pin architecture and thus will require

personality adapters for signal routing to each card under test. Control of the test function is performed by a Compaq 386/25e Deskpro Computer running Compaq DOS version 5.0. No diagnostic capability, other than GO/NO-GO testing with a failure report, and no postprocessor from CADAT currently exists. The price above does include a CADAT vector translator offered by third party vendor.

Advantages/Disadvantages

The major advantage of the SigmaSeries test equipment is the cost. It is one of the lowest cost systems on the market. With this low cost come some unique problems. The pod technology requires a personality adapter for each card under test for signal routing and will require designing the pods with proper termination for signals on the cards under test. The pod design can be done either in-house or by a third party vendor. Summation will provide the majority of components with the remaining system components; pod modifications, CADAT translator, UUT power supplies, receiver interface, and cabinet and workstation - coming from third-party vendors.

9.6 ATE Candidate Summary

The Teradyne L393 is the 40/80 Mhz functional ATE considered in conjunction with high-speed functional test for the new system. This ATE combines the capabilities of testing most of the system cards at, or close to, normal clock and data rates with full functional diagnostics. This tester supports the CADAT

simulation, guided probe and fault dictionary. The L393 was the only viable option for analysis with the 40/80 functional test method with diagnostics.

The Teradyne L353 is a 20 Mhz combinational test system. Depending upon the configuration, this ATE can perform functional testing up to 20 Mhz with full diagnostics. This tester supports the CADAT simulation, guided probe and fault dictionary. The Teradyne L393 does meet initial requirements for functional 20 Mhz test methods.

The Summation SigmaSeries ATE is a rack type ATE for custom testing applications. It has a maximum data rate of 20 Mhz and controls data input and output through pods that connect to a patch panel. Each card under test for this ATE will either require a fixture or signal routing card to handle routing different voltage levels to the appropriate pods. No diagnostics exist for this ATE, and any simulation support programs would have to be developed. Due to the test and diagnostic limitations of this system, it was eliminated from further considerations.

The Schlumberger S790 is a 10 Mhz combinational test system which, depending on configuration can perform functional testing up to 40 Mhz on all channels with full diagnostics. This tester has possibly the tightest link with the CADAT simulator due to company ties, however, the software and the system are still relatively new and not field proven. The Schlumberger S790 does meet initial requirements for further analysis for functional (10/20/40 Mhz) test methods.

The Hewlett-Packard HP82000 is a 50 Mhz functional ASIC test system with capabilities for full card go/no-go functional test. This ATE has possibilities for a

functional test analysis, but the lack of diagnostics or simulation support eliminated the HP82000 from consideration for functional test methods.

Due to the system requirements of at least 480 channels, CADAT simulation support and probe technique diagnostics, the following ATE are being considered for full life cycle cost analysis: Teradyne L393, Teradyne L353, and Schlumberger S790. The systems engineering process necessary to complete this evaluation is beyond the scope of this project. This process would entail further comparisons of the remaining three ATE candidates against system requirements, specifically MTBF, A, and MDT. The final system would be selected after careful considerations were made of all life cycle costs possibly incurred from each ATE testing solution. The prime candidate would be the one that most accurately filled system requirements at the lowest economical burden to the customer.

The initial evaluation of the two alternatives, Teredyne and Schlumberger, show the Schlumberger two be the best choice. The Schlumberger provides the best graphical user interface and will be the easiest to convert the simulation programs over on due to company ties with the simulation vendor. Comparing the two alternatives finds Schlumberger to also have the easiest diagnostic interface with all the latest in technology (bells and whistles).

10.0 CONCLUSION

The topic of this project, "automated testing", was chosen because of my interest in this area and my desire to study this in-flux subject matter. The complexity of present and up-coming technologies require a different approach to test then what has been used in the past. This project attempts to define the process necessary to analyze a need for test, and select the correct test strategy.

- Lessons Learned:
  1. Assure that the definition of need fully justifies a requirement for automated testing
  2. Analyze the reliability of fixture connectors
  3. Verify that the chosen ATE system provides a man/machine interface (GUI) that is up to today's standards

One possible area for future research is the design-for-test philosophy. This philosophy, while well established, is not as fully implemented as would be expected. Integration of the test engineering and design engineering functions is needed to maximize this technology. The effects on test with a fully integrated design-for-test system would be interesting. Could the majority of fault isolation be performed in-system with scaled up system diagnostics? How does this effect the need for external ATE equipment? Is the software requirement for full in-system diagnostics prohibitively high? As can be seen, this area is rich with possibilities

for research. The ever increasing complexity of electronic systems is going to require an up-front systems analysis to properly select methods to verify performance and isolate faults.

ENDNOTES

1. Dian L. Melius and Stephen G. Eichenlaub, Diagnosing Faults On PCB's Using ATE (GenRad Inc., 1989), p. 29.

2. Melius and Eichenlaub, p.32.

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Diagnosing Faults on PCB's Using ATE. Dian L. Melius and Stephen G. Eichenlaub. GenRad, Inc., 1989.

APPENDIX A. ATE CANDIDATE SPECIFICATIONS

Teradyne L393/L397

Maximum L393 pin configuration: 1,152 I/O

Maximum data rate @ 1,152 I/O: 40 Mhz.

Maximum data rate @ 576 I/O: 80 Mhz.

Maximum drive/detect skew: +/-3 ns.

Mimimum edge resolution: 250 ps.

Minimum pulse width: 10 ns.

Maximum number of timing phases (0): 8.

Maximum number of timing windows: 8.

Drive/detect voltage range: +10.2v / -2.5v.

Drive/detect accuracy: drive+/-20mv, detect+/-(60mv+1%).

Overdrive current: 60 ma

Teradyne L353/L357

Maximum L357 pin configuration: 6,048 I/O

Maximum data rate: 40 Mhz.

Maximum drive/detect skew: +/-5ns.

Mimimum edge resolution: 1 ns.

Minimum pulse width: 50 ns.

Maximum number of timing phases (0): 8.

Maximum number of timing windows: 8.

Drive/detect voltage range: +7.5v / -5v, detect +10v/-5v.

Drive/detect accuracy: drive+/-50mv, detect+/-(100mv+1%).

Overdrive current: 500 ma

Current load: +/-10 ma (programmable).

Fault Dictionary fully supported.

16 levels of Fault Trace analysis supported (full support).

Summation SigmaSeries

Maximaum functional pin configuration: 3360 bedirectional I/O Logic levels designed into pods - 32 uni-directional signals per pod).

Maximum data rate: 20 Mhz.

Maximum drive/detect skew: +/-13 ns/+/-13 ns.

Minimum edge resolution: 10 ns.

Maximum number of timing strobes: 8.

Maximum number of timing states: 3 to 256 T-states for a major cycle.

Drive/detect voltage range: Configured by hardware in pod.

Fault Dictionary not supported.

Fault Trace analysis not supported.

Schumberger S790

Maximum in-circuit pin configuration: 3,840 I/O

Maximum functional pin configuration: 960 I/O

Maximum data rate: 40 Mhz(Data Mode).

Maximum drive/detect skew: +/-3ns.

Mimimum edge resolution: 200 ps.

Minimum pulse width: 10 ns.

Maximum number of timing phases (0): 8.

Maximum number of timing windows: 8.

Drive/detect voltage range: +5v for DS, +/-15v for DS 3..

Overdrive current: +/-500 ma for DS 1, +/-100 ma DS 3.

Fault Dictionary fully supported.

Fault Trace analysis supported.

Hewlett-Packard HP82000

Maximum functional pin configuration at 200Mhz: 512 I/O

Maximum functional pin configuration at 50Mhz: 512 I/O

Maximum data rate: 200 Mhz (D200) 50 Mhz (D50).

Maximum drive/detect skew: +/-500ps/ +/-800ps at 50 Mhz.

Maximum drive/detect skew: +/-250ps/ +/-500ps at 200 Mhz.

Mimimum edge resolution: 200 ps at 50 Mhz.

Mimimum edge resolution: 50 ps at 200 Mhz.

Minimum pulse width: 8ns at 50 Mhz

Minimum pulse width: 3.5 ns at 200 Mhz.

Maximum number of timing phases: 2 edges and 2 memory bits per vector

Maximum number of timing windows: timing edges are per pin programmed.

Drive/detect voltage range: -4v to 8v / -4v to 7.5v at 200 Mhz.

Drive/detect voltage range: -2v to 7v / -2v to 7v at 50 Mhz.

Fault Dictionary not supported.

Fault Trace analysis not supported.