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SUSCEPTIBILITY EVALUATION OF COMBINATIONAL LOGIC IN VLSI CIRCUITS

by

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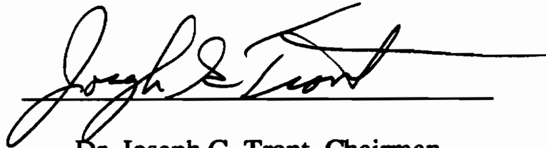

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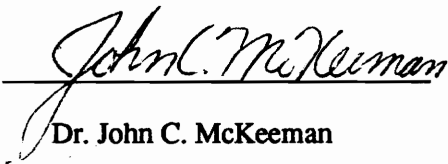

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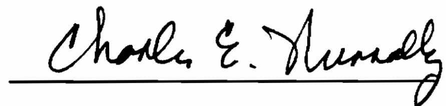

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April, 1990

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(ABSTRACT)

A number of errors occur in digital systems operating in a harsh radiation environment. These errors are due to transient faults which may cause a temporary change in the state of the system without any permanent damage. These transient faults are referred to as Single Event Upsets (SEUs). Because of their random and non-recurring nature, such faults are very difficult to detect and hence are of source of great concern.

This thesis examines the logical response of combinational logic circuits to SEUs. Time domain analyses of a large number of circuits attempts to determine the affect of an SEU on a flip-flop which might lay at the end of a chain of combinational logic gates. In this way, the concept of an upset window, as it pertains to different types of logic gates is introduced. The results of the simulations carried out on various blocks of combinational logic are discussed. A program called SUPER (**SU**sceptibility **PrE**diction p**R**ogram) is developed. SUPER predicts the probability of a circuit fault occurring given that a cosmic ray with certain energy characteristics impinges on an arbitrary point within an IC. IC. The input variables to SUPER include the radiation level, the duration of the

radiation, the types of gates the radiation affects, the signal path, the type of voltage pulse that the radiation produces (rising or falling) and the time (with respect to the clock pulse) that the radiation is incident on the circuit. The output of SUPER consists of a prediction as to whether or not the incident radiation causes a change in the output of a flip-flop.

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Chapter 1. Introduction

Semiconductors are the backbone of most of today's high-tech systems for commercial, industrial, and defense applications. Whether they are found in land, air, satellite or space platforms, such devices are often subjected to severe heat, cold, vibration, and shock. Various kinds of radiation which occur in nature can also present critical environmental problems. In fact, it has been known for years that radiation can change the electrical properties of solid state devices, leading to possible system failure.

Anomalies in communication satellite operation have been caused by the unexpected triggering of digital circuits. These anomalies are caused by the change of a single bit from a logic 0 to a logic 1, or vice versa in memories and related semiconductor storage devices (flip-flops, registers, counters). These are transient faults by nature, because the exact time and location of the fault cannot be predicted in advance. In addition, the fault is only temporary. Once the radiation event is finished, no permanent damage is left to the system. That is, when the device is written to once again, there is no indication of permanent damage and so the bit-flip is referred to as a **soft error** or **a single event upset (SEU)** [1-4]. These two terms will henceforth be used interchangeably.

Radiation induced errors are caused by ionized electron-hole pairs being produced by a single particle such as a heavy ion component of cosmic rays, or an alpha particle,

proton, neutron or even an energetic (15-25 MeV) photon. In a space environment, the ionizing radiation that is absorbed by a device can be accumulated over a long period of time; for example, 10K rads(Si) in 20 years. This is referred to as **total dose** radiation. However, in a weapons environment, a device may be subjected to an extremely large dose within a very short period of time. Doses can be of the order of 10^4 - 10^8 rads/sec (Si) for a few nanoseconds. This type of radiation is referred to as **transient radiation**. Unlike total dose radiation, where a threshold accumulation of the total dose is required before the damage becomes unacceptable, even one particle can cause an upset although its probability is low. Experiments have shown that the fluence required for a single upset to occur ranges from about 200 heavy ions/cm^2 up to 10^6 - 10^9 protons/cm^2 for a single susceptible device type. There is, however, for each device type a critical amount of charge which must be deposited within a microscopic sensitive region of the device if an upset is to occur. If a given particle is incapable of depositing sufficient charge (the charge being proportional to the energy deposited), then there will be no bit-flip, regardless of the total fluence [5].

The prime source of the energetic charged particles that give rise to SEUs in the space environment are cosmic rays. The exact sources of these cosmic rays are yet unknown. Existing evidence suggests that, except for the highest energies, these particles come from sources within our galaxy [1-4]. Cosmic rays are highly penetrating and have measurable fluxes at very high energies. When these cosmic rays pass through air, they collide with air nuclei and break into lighter nuclides. Generally, a few nucleons and alpha particles (helium atoms with electrons stripped off) are emitted. The fragments retain roughly the same energy/nucleon as the incident nucleus. These collisions generally cause ionization of the air and accelerate the cosmic rays. Cosmic rays arriving

in our solar system consist of the nuclei of all the elements in the periodic table and electrons.

The amount of cosmic ray activity depends on a number of factors. One of these factors is the solar cycle. This cycle of solar activity, waxes and wanes with a period of 11 years. This period of 11 years is accepted by most scientists, though some consider the cycle to last 22 years. The worst radiation environment is during the time of minimum solar activity, at which time cosmic ray activity is at a maximum. Particles present in solar flares and those present in the interplanetary medium are also responsible for SEUs. Large solar flares are very rare and they contribute to the particle environment less than 2% of the time. Protons and alpha particles in the Van Allen belts also have sufficient energies to cause SEUs. Many satellites that intercept these belts at the South Atlantic anomaly experience upsets at a greater rate than usual. The galactic cosmic ray composition is qualitatively similar to the universal composition of matter, the most abundant element being hydrogen. The abundance of elements with atomic numbers greater than 26 is negligible, and can be ignored for all practical purposes. It should however be noted, that if a microelectronic component is struck by one of these rare nuclei, an enormous amount of charge would be liberated, leading to a soft error even in devices commonly thought to be insensitive to this effect. [6-7].

SEUs can be used to determine the quality and reliability of a product, however it is very difficult to test for SEUs, as they are not detected by the conventional testing methods. Further, if a rarely used circuit in a complex chip fails, it is very difficult to distinguish the cause of the failure, as it is hard to determine whether or not the circuit has failed due to a SEU. Since SEUs are so difficult to track down, the SEU detection mechanisms do

cause false alarms. There have been literally hundreds of upsets in dozens of military satellites that have occurred over the years [5]. SEUs can also arise in ground based systems caused by the minute amounts of naturally occurring radioactive alpha emitters present in IC packages, or from the secondary cosmic ray particles impinging on the earth. Obviously, vulnerability to SEUs must be considered in the design of future space platforms. In order to assess the vulnerability of any proposed design, engineers must have a reliable means of estimating SEU rates in the radiation environments that can be expected during the mission. Besides requiring a reliable model of the near-earth particle radiation environment, this also requires experimental measurements and circuit modeling to establish the parameters that determine the SEU sensitivity of each device in a circuit.

Radiation incident at a particular node in an IC in a satellite system causes a voltage pulse at that node. This voltage pulse causes an SEU which may propagate through a combinational logic block to a flip-flop, causing it to temporarily change to an erroneous state. This thesis examines the logical response of combinational logic circuits to SEUs. A program that predicts the probability of a circuit fault occurring due to an SEU is developed.

Chapter 2 is a literature survey on SEU effects and remedies. It also discusses previous work on the subject of predicting SEUs and circuit failures due to SEUs. Chapter 3 discusses the mechanism of SEUs in combinational logic. Chapter 4 consists of the assumptions and the results obtained from the simulations done on combinational logic blocks to determine the effect of SEUs on circuit performance. Chapter 5 discusses the

program SUPER and includes a pseudocode and three examples. Chapter 6 summarizes the work done and gives direction to future work in this area.

Chapter 2. Literature Survey

2.1 SEU Effects and Remedies

Active research into the details of SEUs caused by ionizing radiation has been going for more than 10 years [5]. Various models that estimate SEUs have been developed and experimental studies have been carried out at JPL, NASA, NRL and various other research laboratories to verify these models. Although the basic mechanism for SEUs is well established for most situations, the number of predictions for particular device types and particular technologies is very limited.

The increasing frequency with which bit upsets are reported in space and the recurring failure of certain device types in different missions demands a full scale assessment of the susceptibility of binary storage devices used in satellites and spacecraft. At present, methods of addressing the SEU problem are not entirely satisfying. Some of the remedies available to designers are [8]:

- Change the environment
- Shield the satellite circuits
- Use purer materials
- Change the susceptible parts and use radiation hardened technology

- Introduce a strong local magnetic field
- Increase the power per gate
- Apply fault-tolerant computing architectures

Changing the environment requires changing the circuit's place (or time) in it. Cosmic rays and other ionizing radiation, radiation belts, and solar flares will not go away; but certain time conditions and paths through outer space are better than others. The safest paths in the earth orbit are the low equatorial altitudes.

Shielding the environment is generally a low yield approach. For example, 10 grams / sq cm (1.5 inches of aluminum) of shielding over and above the outer skin of the spacecraft, does not alter the cosmic ray spectra above 10 Mev/u. It barely makes a factor of two difference in the SEU rates due to the ionizing radiation. In some environments, it can even be a detriment due to the heavier payload.

It is a known fact that radiation from the packaging materials can be a source of soft errors. The antidote to this problem is to modify the process by adding layers of doping near the surface of the packaging, to reduce the collection efficiency. This method does not eliminate the problem, it only reduces the error rate, and that too at a very high processing cost. Changing the susceptible parts is a job best done before the design begins. By using technology that is tested to be radiation hardened, the error rate can be reduced. At present, CMOS/SOI is the best, because results of experiments show that it has the lowest error rates. In this technology, the substrate acts like a buried insulator and eliminates a large portion of the PN junction depletion region, thus greatly reducing the field inversion and latch-up problems. Thus to cause an SEU, it necessary for the ionizing

radiation to produce the required upset-level charge in a much shorter path. The VHSIC class of circuits could be the best for satellite use because of their high speeds and low power consumption. But at present, little is known about the SEU immunity to the VHSIC class of circuits with cell sizes of a micron or less [8].

Using a strong magnetic field along with shielding is an expensive and dubious approach, since such an artificial magnetic field in space would develop its own magnetosphere filled with trapped particles. The cure could be worse than the disease!

Increasing the power per gate makes use of the fact that by keeping the power per gate constant at a level where a soft error due to the ionizing radiation is almost impossible, the error rate can be significantly reduced. The problem with this method is that as the level of integration increases, it would be necessary to find some new methods to cool the system, as conventional cooling methods would no longer be able to remove the heat generated.

Thus, in the long run, a fault-tolerant computer seems to be the ultimate answer. When examining fault-tolerant techniques in terms of total redundancy, like Triple Modular Redundancy (TMR) or other powerful coding techniques, it is seen that they work very well. But when the overhead in terms of area and power is taken into account, it is seen that the area and power overhead is more than 200% above non-TMR circuits if a single error tolerance in an arbitrary logic function is required. This penalty is realized before the time overhead spent in voting on the results is taken into consideration. Another possible fault-tolerance mechanism for soft errors is the use of encoding of the output lines of a single unit.

A very important asset of the TMR technique is that it is not specialized just for soft errors. It will work as well for permanent errors. However, the area and power overhead are very high, and are not well-suited to satellite applications.

These are only some of the ideas that have been considered by researchers. A fertile imagination could supply many more concepts, but each will only partially address the total problem, which is indeed very vast.

2.2 Previous Work

Over the years, various experimental studies were undertaken to verify the models of the single event upsets that have been incurred by active spacecraft and satellite systems. Kolanski, Price, et al. [6] reported that single event upsets were observed in some of the devices tested in their experiments at the Berkeley cyclotron. They used argon and krypton ions (energy ~ 2 MeV/nucleon) to simulate the behavior of the iron group of heavy ions in cosmic rays. Their goal was to verify the models used for predicting radiation induced soft errors in computer memories and to ascertain if the memory devices planned for project Galileo would withstand the ionizing radiation. Their tests showed that the Sivo [7] model was in reasonable accord with the predicted error rate although the data they gathered showed more variability between devices than was predicted by Sivo.

Pickel and Blandford [10] have also reported work with argon and krypton ions at the Berkeley cyclotron for a number of NMOS and CMOS memories. They observed bit flips and latch-up in accordance with their model for these devices. Their results are also in agreement with the results reported by others, in that static and dynamic RAM's are generally more susceptible to upset when bipolar or NMOS technology is used than when CMOS technology is used.

Guenzer et al. [11-12] reported tests of 16K dynamic RAMs using protons and neutrons. They showed that these devices were susceptible to upset via nuclear reactions that generated multi-MeV alpha particles. They postulated that the alpha particle discharges either the storage capacitor, the floating bit line or the reference capacitor used by the sense amplifier. Guenzer et al. also expanded their efforts to include 4K RAMs, and the results showed that there was little difference in the response of the 4K and the 16K RAMs.

McNulty et al. [13] also irradiated both static and dynamic RAMs with protons and neutrons. The soft error rates for the static RAMs was about two orders of magnitude lower than that of the dynamic RAMs exposed under identical conditions.

Blake and Mandel [14] studied the SEU latch-up rate of a satellite system containing 384 Harris HM-6508 RAMs over a period of two years. The observed SEU rate was consistent with the predictions based on laboratory tests using the Berkeley 88 inch cyclotron.

Shoga et al. [15] carried out an experiment aboard the Hughes Corporation Leasat vehicle to monitor SEUs in a memory consisting of 93L422 RAMs. They used the simultaneous measurement of the high energy galactic cosmic rays and solar flare environment from a previous experiment and estimated the SEU rate for the RAMs. The average estimated rate was $2.13 * 10^{-4}$ upsets/bit-day.

Brucker [16] irradiated different versions of a CMOS/SOS 4K static memory with argon and krypton ions. It was interesting to note that the device did not latch-up, although it did exhibit bit flips. Another factor worth noting was that small variations in the processing had a significant effect on the electrical parameters, and these were observed to correlate with different radiation effects.

Savaria et al. [17] proposed an approach for providing fault-tolerance to soft errors by filtering the transients at the register inputs. The disadvantage of this approach was that it slows down the clock rate, and thus the system throughput.

Kerns et al. [18-19] studied the ion-induced SEUs in CMOS static RAMs and proposed a methodology to reduce the SEU rate by introducing a decoupling resistance between memory cells. They also proposed an algorithm [23] that optimized CMOS combinational logic circuits for operation in a total dose radiation environment. However, again the resistor inserted in the circuit tends to slow the operational behavior of the circuit.

The literature review summarized in the previous paragraphs, indicates that little work has been done on SEU effects on combinational logic. Device testing for SEUs has typically been performed on RAMs. The primary upset mechanism in these RAM circuits is a change in the stored charge in the memory cells resulting in stored data errors that are readily observable. Most of the research work done consists of simulation of the radiation environment in a cyclotron. The device under test is irradiated by cosmic rays and its functioning is compared with a copy of that device, called the golden device, which is outside the cyclotron. Combinational logic SEU testing, on the other hand, requires a capability of detection and storage of extremely narrow error pulses on the order of a few nanoseconds, which is a significantly more difficult test problem.

Chapter 3. Mechanism for SEUs

3.1 Basic Mechanism

The basic mechanism that causes an SEU is based on the fact that all logic device types will exhibit a change of state if sufficient radiation is incident on the device. This radiation deposits a charge within a specific parallelpiped shaped microscopic region (**sensitive volume**) of the chip, where it can induce a change in the amount of charge on a key capacitance. In the silicon of integrated circuits, this has the effect of adding to or subtracting from the local charge in a sensitive volume. There will be a change of state only if the charge deposited is greater than a certain minimum charge (**critical charge**). This charge gives rise to a voltage spike in the circuit. The critical charge is determined by the total node capacitance, the threshold voltages of the associated transistors, and the circuit sensitivity as determined by RC time constants.

In cosmic rays, there is a heavy ion component (known as the iron group) as well as protons of almost limitless energies. The heavy ions penetrate through the semiconductor in generally straight-line paths. Coulombic interactions result in energy transfer to electrons, producing secondary electrons that have a wide spectrum of energies, and travel in random directions. These secondary electrons spread from the original ion path for a distance up to a few microns, losing energy by ionization of the semiconductor material.

Loss of energy due to ionization is represented by the **stopping power** of the nuclide. The stopping power is the rate of energy loss and is a function of particle type, energy, and material through which the particle is passing. It is also known as the **Linear Energy Transfer (LET)**. LET increases as the square of the cosmic ray energy. The heavy ions in the cosmic rays transfer maximum charge to the material due to their high stopping power. For upset computations the cosmic ray spectra are converted into LET spectra. LET spectra show the cosmic ray flux as a function of the stopping power in silicon. Instead of being classified according to the amount of energy, they are classified according to the rate at which they give up energy in silicon. LET is not a monotonic function of charge. In fact, the lowest LET occurs at high energies (few GeV/nucleon) while the highest LET occurs at a few MeV/nucleon. There is no direct relation between the cosmic ray spectra and the SEUs, because the rate of energy deposited by a cosmic ray bears a complicated functional relation to its total energy. It depends mostly on the following factors: solar cycle, geomagnetic field strength, atmospheric depth, and device orientation.

Given the IC device parameters, the LET spectra may be converted into upset probabilities. In any environment, the probability of upset depends on a critical charge and sensitive volume (which are device dependant parameters) in addition to the cosmic ray LET spectrum. The critical charge is the number of free electron-hole pairs necessary in the neighborhood of a junction to cause an upset. These pairs are created at a rate of one pair per 3.6eV of deposited energy [22]. The sensitive volume is characterized by a chord length distribution giving the relative frequencies of each path length. The energy deposited is proportional to this path length. This charge is then, by definition of the sensitive volume, able to accumulate and cause the change in the device state. The

critical charge is a few pC for devices where the gate length is of the order of 10-20 μm. It varies roughly as the inverse square of the gate length.

The result of a cosmic ray passing through the IC material is a cylindrically shaped path of ionization through the crystal, with an intense core of ionization that varies approximately as $1 / r^2$ with distance away from the center of the core. This ionization process is very fast, being on the order of picoseconds, and will be treated as an instantaneous deposition of energy, and corresponding charge, along the whole path travelled by the ion [9].

Thus, whether a particle will cause a state change is determined by comparing the threshold energy of a cell to the particle's LET in silicon times the length of its path through the cell. The latter product is a normalized LET value that can be associated with any particle regardless of its atomic species. The LET-spectrum is much more useful than other techniques of expressing the galactic cosmic ray environment in analyses of the effects on MOS circuits because the only aspect of significance for a particle is the rate of energy deposition dE / dx or LET.

A MOS transistor can modeled as a capacitor with the metal gate and semiconductor channel as the plates and the gate oxide (silicon dioxide SiO_2) as the dielectric. A typical n-channel transistor is shown in Figure 1. The ionizing radiation produces its effects in the gate oxide region. These effects are the threshold voltage shifts and channel mobility degradation.

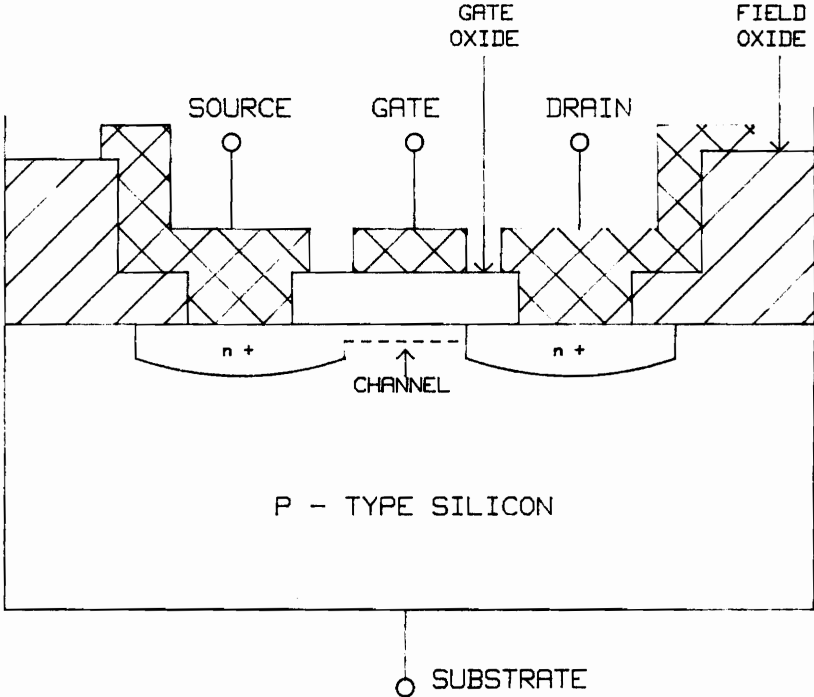


Figure 1. MOSFET n-channel Transistor

The ionization process is shown in Figure 2. The condition prior to irradiation, at time t = 0- is shown in Figure 2a. At time t = 0 the ionizing energy is delivered to the SiO_2 (Figure 2b) and the electron-hole population is generated. Immediately after the ionization, the process of electron-hole recombination occurs (Figure 2c). At this time, electron transport occurs. Electron mobility is about 4-5 orders of magnitude larger than the hole mobility, and due to the applied voltage, any electrons that do not undergo recombination are swept towards the gate and removed (Figure 2d), leaving behind the less mobile holes. These holes will begin a transport process towards the silicon - silicon dioxide interface (Figure 2e). Some of the holes will pass into the silicon, while the others will be trapped near the interface of the gate oxide and bulk silicon. This trapped positive charge builds up, and makes it easier to create the n - channel (the inversion layer). This lowers the threshold voltage and thus makes it more susceptible to upset.

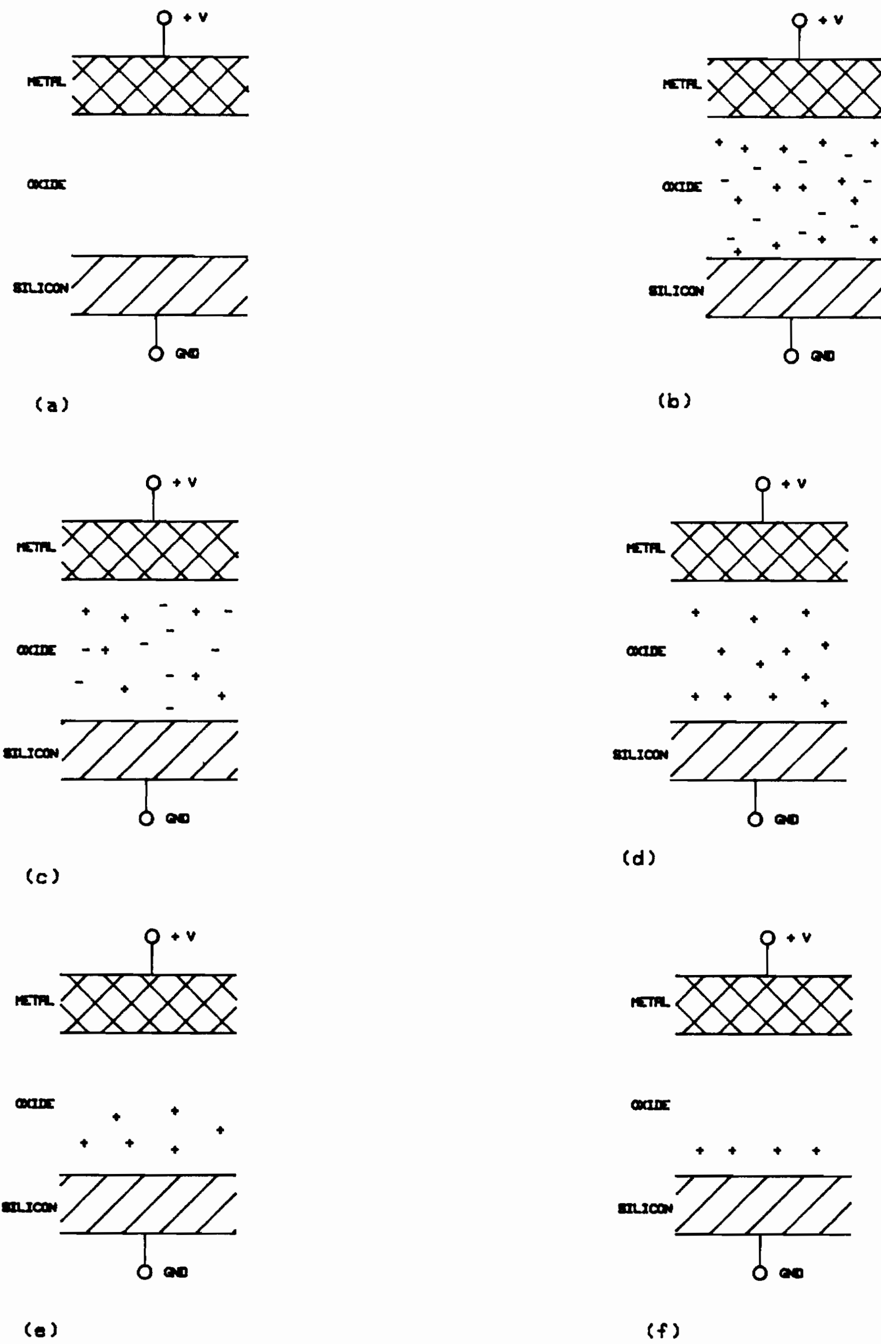


Figure 2. Charge Carrier Transport Mechanism

3.2 SEUs IN COMBINATIONAL LOGIC

SEUs were first noticed in flip-flops, and therefore, almost all of the literature on the subject relates to the study of storage elements. But, SEUs also affect combinational logic. Typically, a digital system consists of several stages of combinational logic followed by a storage element such as a flip-flop. An SEU in combinational logic produces a voltage transient at the site of incidence, after which the pulse propagates forward through the circuit. Little, if any at all, reporting has been done on the SEU testing of combinational logic. All the research and testing work that has been done on SEUs has been performed on the testing of different RAMs and microprocessors that contain internal storage. As pointed out earlier, the basic upset manifestation in these memory circuits is flip-flop toggling, resulting in stored data errors that can be easily observed.

On the other hand, the manifestation of SEUs in combinational logic is considerably different and more complex than that for RAMs. The main reason for this difference is that, the sensitive and storage regions in the RAM cells are identical. The upset occurs when a storage node, intercepted by an energetic particle, collects sufficient charge to change the information stored. In combinational logic, the sensitive and storage regions may be completely disjoint. In combinational logic, the ion-induced events can generate voltage transients that mimic normal signals propagating through a pipeline of logic gates. If a voltage transient has sufficient energy for a critical amount of time, and if it

finds a path or multiple paths to a latch, or finds paths to multiple latches, it will cause the erroneous signal to be latched and alter the state of the latch.

Figure 3 illustrates the above point very well. This figure is a gate level representation of a binary full adder. From this figure, it can be clearly seen that an incident particle on the input node of a logic gate can propagate through different paths and cause errors in multiple latches or take different paths and cause an error on a single latch. For example, if the radiation is incident on input node A, it can cause a change in either of the sum and carry outputs or both. These outputs are likely to find their way to latches and may be latched as erroneous data.

It is the latched logic that finally records the single event errors, whatever the mechanism. The circuit regions devoted to combinational logic can focus the single event errors onto storage elements, thereby magnifying the latch vulnerability.

Thus, the criteria for SEUs in combinational logic, propagating through to a latch and inducing it to change its state are:

1. The incident particle must have sufficient amplitude to cause a voltage transient at a node. This transient will propagate through combinational logic and reach the input node of a flip-flop.

2. There must exist a path, called the critical path, that would allow the voltage transient to propagate from the node on which the radiation is initially incident to the input node of the flip-flop.

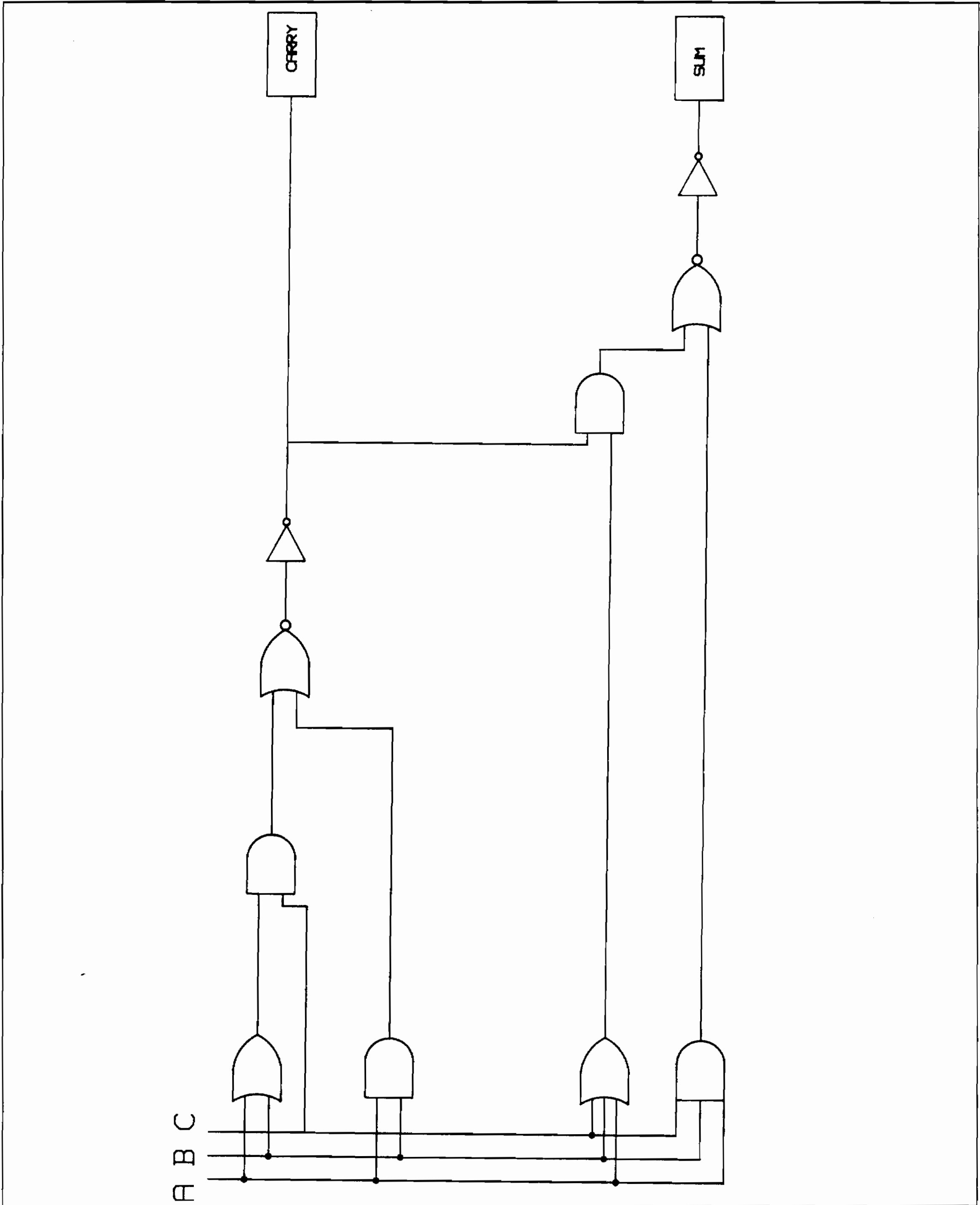


Figure 3. Binary Full Adder

3. The arrival of the voltage transient must correspond with the clock pulse of the flip-flop, and should be present for a certain minimum time. This minimum time is the sum of the setup and hold times for the D input of the flip-flop. It is the same as the time that must be observed for normal data input to the flip-flop.

A single event will be latched, and cause an observable upset only if all the above three conditions are met.

Chapter 4. SEU Prediction Using Simulations

4.1 Introduction

This chapter discusses various aspects of the simulations carried out to find the susceptibility of combinational logic to the effects of radiation.

Various blocks of combinational logic, consisting of gates cascaded in series and leading to a flip-flop or a number of flip-flops were simulated using RELAX [20]. RELAX is a circuit simulation program developed at the University of California at Berkeley. Voltage pulses of variable amplitude and pulse width were applied to the various nodes in the circuit on which the radiation was assumed to be incident. The voltage pulse simulates the effects created by the charge separation caused when the ionizing radiation passes through an IC region. The effect on the circuit behavior was evaluated. This characterization was done to determine how errors in the combinational logic contribute to the total number of errors observed in the circuit's flip-flops.

4.2 Simulation Assumptions

The simulations were performed on three type of logic gates: INVERTER, NAND, and NOR. This was done because these gates are the basic building blocks for any CMOS

circuit. Note that throughout this thesis, it is assumed that the ionizing radiation will affect only a single node.

4.2.1 Number of inputs per gate:

Simulations were carried out only on two input gates, since the probability of two input gates being upset is much higher than for gates with more than two inputs. As shown in the discussion below and in the tables on the following pages, the probability that a two input gate will be upset is 100% more than that of the same gate with three inputs.

In Table 1 is shown inputs A and B and the resulting output for a two input NAND gate. Also shown is an input column A' which depicts the situation where the input has been modified by a radiation event. The gates' resultant output is listed as Y'. From Table 1 it is seen that, if one of the two inputs to a gate changes its logic state, there is a 50% chance that the logic state of the output will also change. This is true for both NAND and the NOR gates as shown in Table 2. For the case of a three input gate (see Table 3), the output will change only 25% of the time when one of the inputs changes its state. In the case of a four input gate (see Table 4), the probability of the output changing state, when one of the inputs is perturbed, are even lower. The output will change its state only 12.5% of the time. Effectively, if the number of inputs to a NAND or NOR gate is m, the probability of the output changing its state when one of the inputs changes its state is given by $1 / 2^{m-1}$.

4.2.2 Radiation charge collection:

Figure 4 shows a model for the charge collection mechanism in a typical CMOS circuit. The radiation incident on a circuit node induces a rapid charge buildup at that node. This,

in turn, produces a rapidly changing voltage spike at that node. This change in voltage is responsible for the change in logic state of that particular node. The voltage spike which is produced as a result of the charge collected can be modeled as a voltage source at the input node to the gate. What actually happens at the transistor level can be better understood with the help of Figure 2. The incident radiation affects the threshold voltage making it easier to create the channel between the drain and the source.

Table 1: 2 input NAND gate

A	A'	B	Y	Y'
0	1	0	1	1
0	1	1	1	0
1	0	0	1	1
1	0	1	0	1

Table 2: 2 input NOR gate

A	A'	B	Y	Y'
0	1	0	1	0
0	1	1	0	0
1	0	0	0	1
1	0	1	0	0

Table 3: 3 input NOR gate

A	A'	B	C	Y	Y'
0	1	0	0	1	0
0	1	0	1	0	0
0	1	1	0	0	0
0	1	1	1	0	0
1	0	0	0	0	0
1	0	0	1	0	0
1	0	1	0	0	0
1	0	1	1	0	1

Table 4: 4 input NAND gate

A	A'	B	C	D	Y	Y'
0	1	0	0	0	1	1
0	1	0	0	1	1	1
0	1	0	1	0	1	1
0	1	0	1	1	1	1
0	1	1	0	0	1	1
0	1	1	0	1	1	1
0	1	1	1	0	1	1
0	1	1	1	1	1	0
1	0	0	0	0	1	1
1	0	0	0	1	1	1
1	0	0	1	0	1	1
1	0	0	1	1	1	1
1	0	1	0	0	1	1
1	0	1	0	1	1	1
1	0	1	1	0	1	1
1	0	1	1	1	0	1

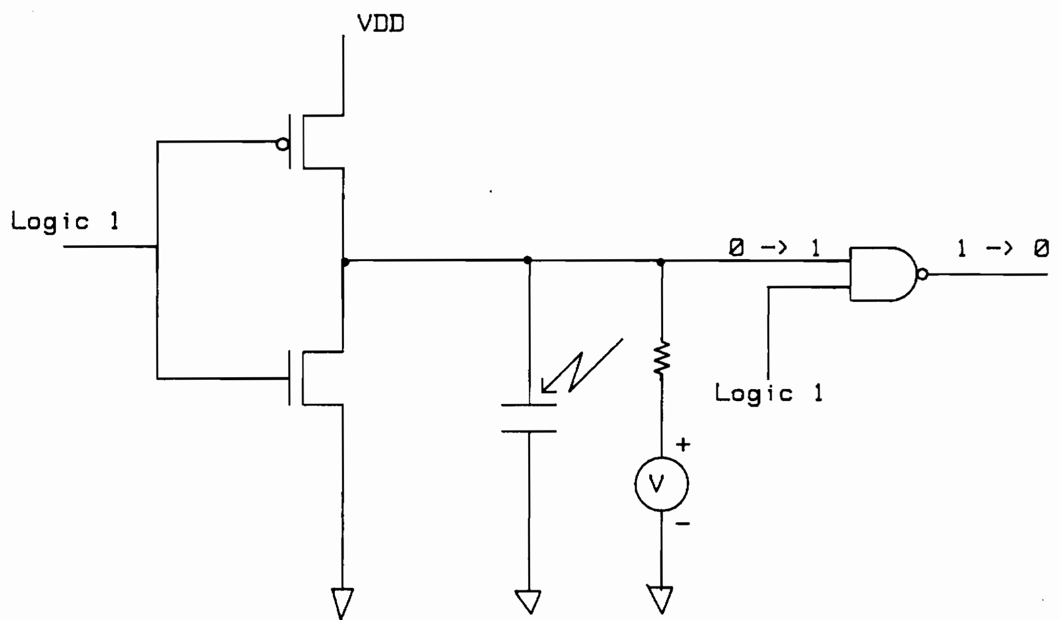


Figure 4. Model for the charge collection mechanism

While carrying out the simulations the volume under the gate of the transistor is considered to be the sensitive volume. The source volume is not considered in the sensitive volume because in CMOS technology, the source node of the transistor is always connected to either V_{dd} or ground, and thus will not be affected by a voltage transient. The drain volume is not considered for the following reason. Consider the minimum sized transistor shown in Figure 5. Hence the gate area is $6\lambda^2$ and the drain area is $18\lambda^2$. So the drain area is three times as large as the gate area. If we compare the gate volume with the drain volume, we see that the drain volume is 10 - 20 times greater than the gate volume because the drain depth (metallurgical junction depth X_j) is 3-6 times larger than the gate oxide thickness (t_{ox}).

This indicates that the drain is much larger than the gate and is therefore more likely to be struck by ionizing radiation. However, even though the gate node is less likely to be struck, it is observed that it is more susceptible to upset than the drain node. The reason for this is that the overall capacitance of the gate is less than that of the drain. From the relation Q = C * V, it is seen that if the same amount of charge (Q), is generated at the gate and the drain nodes by the ionizing radiation, the voltage (V) generated by the charge will be more at the gate, because it has less capacitance (C) than the drain.

Also, ultimately the voltage at the gate controls the logic level of the output and so while performing the simulations, the gate volume is considered as the sensitive volume, and the drain volume is ignored.

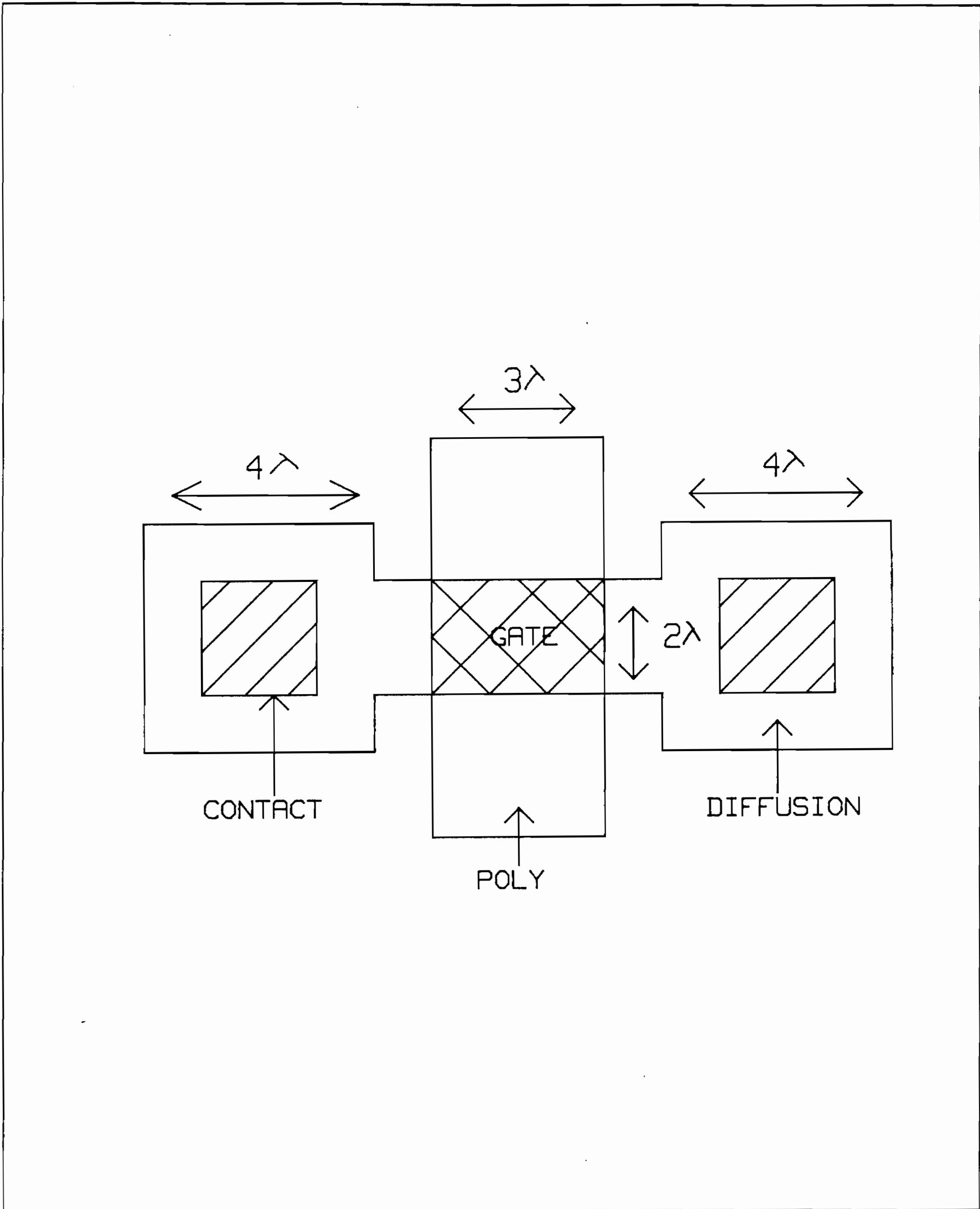


Figure 5. Layout of minimum size transistor

4.2.3 Gate Design:

Consider the truth table of a two input NAND gate. For a voltage transient on one of the nodes (node A) to propagate through and cause the output to change its state, the other input node (node B) of the gate must be a logic 1. If input node B is at logic 0, then the output will be logic 1 irrespective of the logic level at node A, and the effect of the voltage transient will be masked. Thus, the voltage transient will cause the output of the gate to change its state, only if one of the input nodes of the NAND gate is at logic 1, and if the voltage transient hits the other input node. If the SEU causes a logic 0 -> 1 effect at the input, then the output of the gate will go from a logic 1 -> 0.

A similar analogy holds for the NOR gate. In this case for a voltage transient to be incident on one of the input nodes, propagate through the gate, and cause the output to change its state, the other input to the gate, must be at a logic 0. Otherwise, the effect of the voltage transient will be masked and will not be observed at the output of the gate.

Figures 6 and 7 show the layouts of typical CMOS NAND and NOR gates respectively. For the purpose of the simulations, one of the inputs is held at V_{dd} for the NAND gate, and at 0 V for the NOR gate. Depending on the size and type of the gate, it makes from a minor to a significant difference as to which of the two inputs is kept at V_{dd} or ground.

Consider the case of the NAND gate given in Figure 6. In this gate, if the input of the lower n-transistor (input B) is held to logic level 1, then the drain of that transistor (node number 1), is always at ground. Thus the output of the NAND gate depends on the logic level of input A. If input A is a logic 1, then the upper n-transistor is also turned on, and

there is a direct path to ground, so the output goes to logic 0. If a voltage transient is produced at node A and causes it to go to a logic 0, then there is a path from V_{dd} to the output, and only node 2 must be charged for the output to go to logic 1. Similarly, if input A is originally a logic 0, node 2 is charged to V_{dd}. If it changes to a logic 1 then only node 2 has to be discharged to ground for the output to go to logic 0, as node 1 is already held to ground.

Now consider what happens if the input of the upper n-transistor is held at logic level 1 (i.e., input A was now held to V_{dd}). For this case, both node 1 and node 2 would have to be charged or discharged everytime the voltage at the input other node changes. Thus rise and fall times for the circuit are increased and the overall circuit operates slower.

Next consider the case of the NOR gate shown in Figure 7. In this gate, if the input of the upper p-transistor (input A) is held at logic level 0, then the drain of that transistor (node number 1), is always at V_{dd}. Thus, the output of the NOR gate now depends on the logic level at input B. If input B is a logic 0, then the lower p-transistor is also turned on, and there is a direct path to V_{dd}, so the output goes to logic 1. If a voltage transient at input B causes it to go to a logic 1, then there is a path from ground to the output, and only node 2 must be discharged for the output to go to logic 0. Similarly, if input B is originally a logic 1, node 2 is at ground. If input B changes to a logic 0, then only node 2 must be charged to V_{dd} for the output to go to logic 1, as node 1 is already at V_{dd}.

If the input of the lower p-transistor was held to logic level 0 (i.e., input B was held to ground), then both node 1 and node 2 must be charged or discharged every time the input to the other node changes.

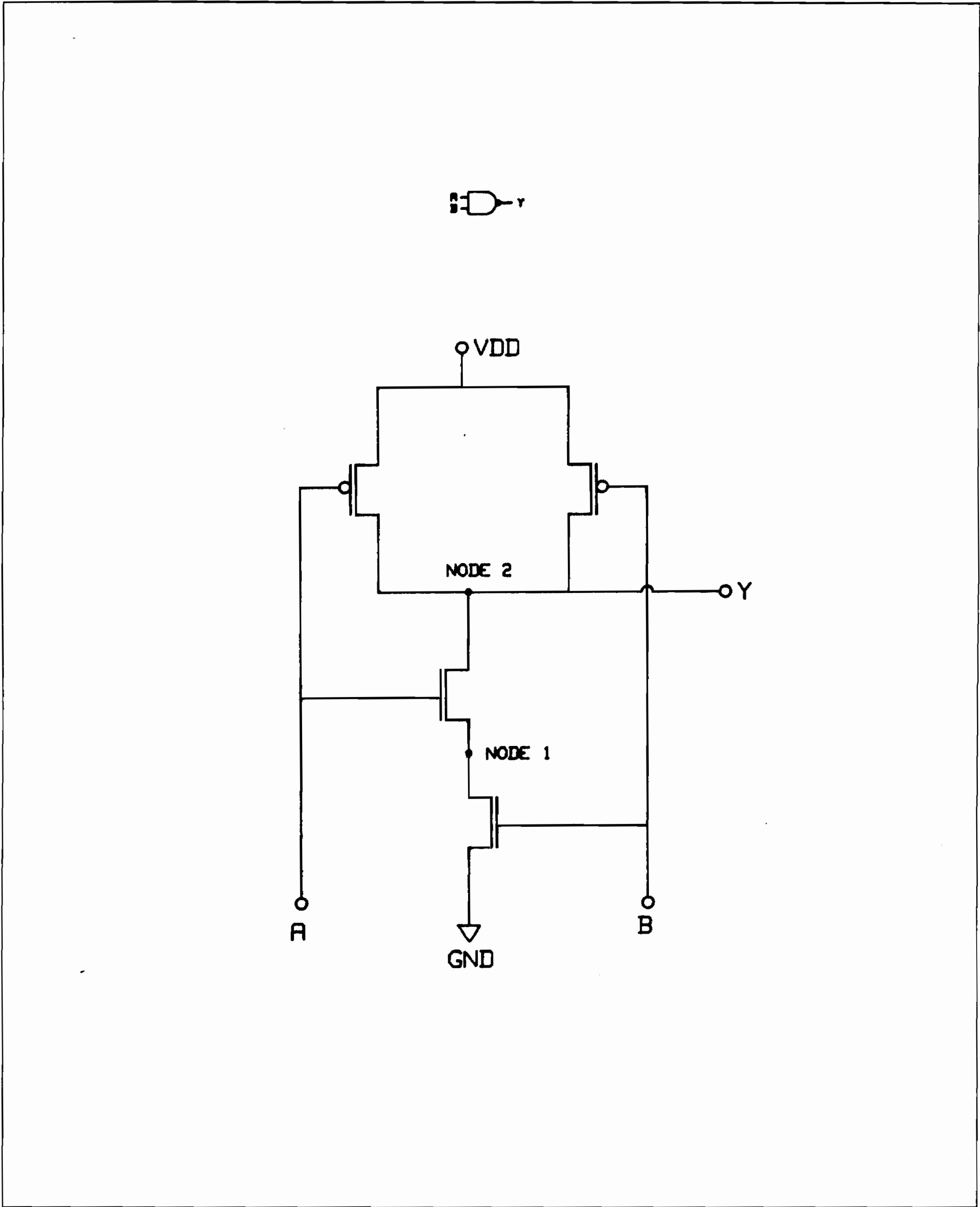


Figure 6. Transistor level representation of the NAND gate

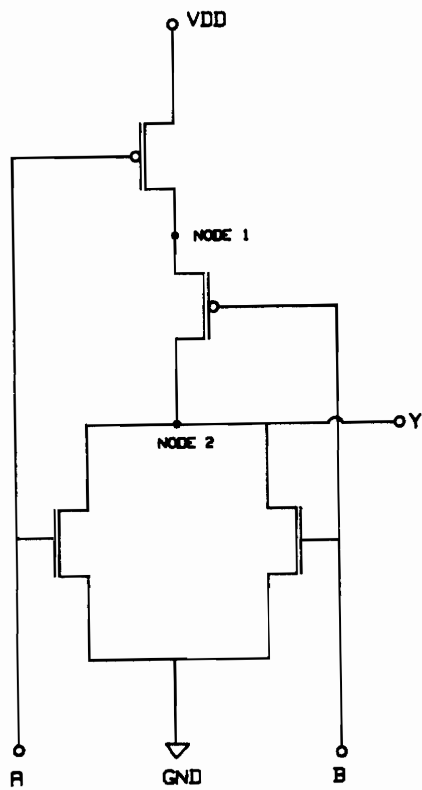


Figure 7. Transistor level representation of the NOR gate

Again, there is an increase in the rise and fall times making the circuit slower.

Since worst case effects are being considered, in the case of the NAND gate, the input to the lower n-transistor (input A) is held at logic level 1 for all simulations. Similarly, for the NOR gate the input of the upper p-transistor (input A) is held at logic level 0.

4.2.4 Pulse Width:

For any pulse waveforms of the form shown in shown in Figure 8, the pulse width is measured from the first transition through the switching voltage to the return transition through the switching voltage. The switching voltage is taken to be 2.5 V with no hysteresis. This value is derived from fact that a two input gate with one input connected to either V_{dd} or ground becomes an INVERTER. The switching voltage of an INVERTER with a ß ratio of 1 is $V_{dd}/2$, which in this case is 2.5 V.

4.2.5 Transistor Sizes (ß ratios):

The simulations are performed using the parameters for the 1.5μ technology obtained from MOSIS. Scalable p-well technology is used to lay out the simulated circuits using MAGIC [21]. Minimum sized transistors are designed according to the design rules. These transistors are used because they would be more vulnerable to voltage transients than transistors having a larger size. If minimum size transistors are not affected by the transient radiation, then it is not possible for transistors having larger dimensions to be affected. In other words, this is a worst case test. The width of the p-transistors is twice the width of the corresponding n-transistors in order to maintain a ß ratio each of 1. This produces equal rise and fall times in the standard inverter circuit.

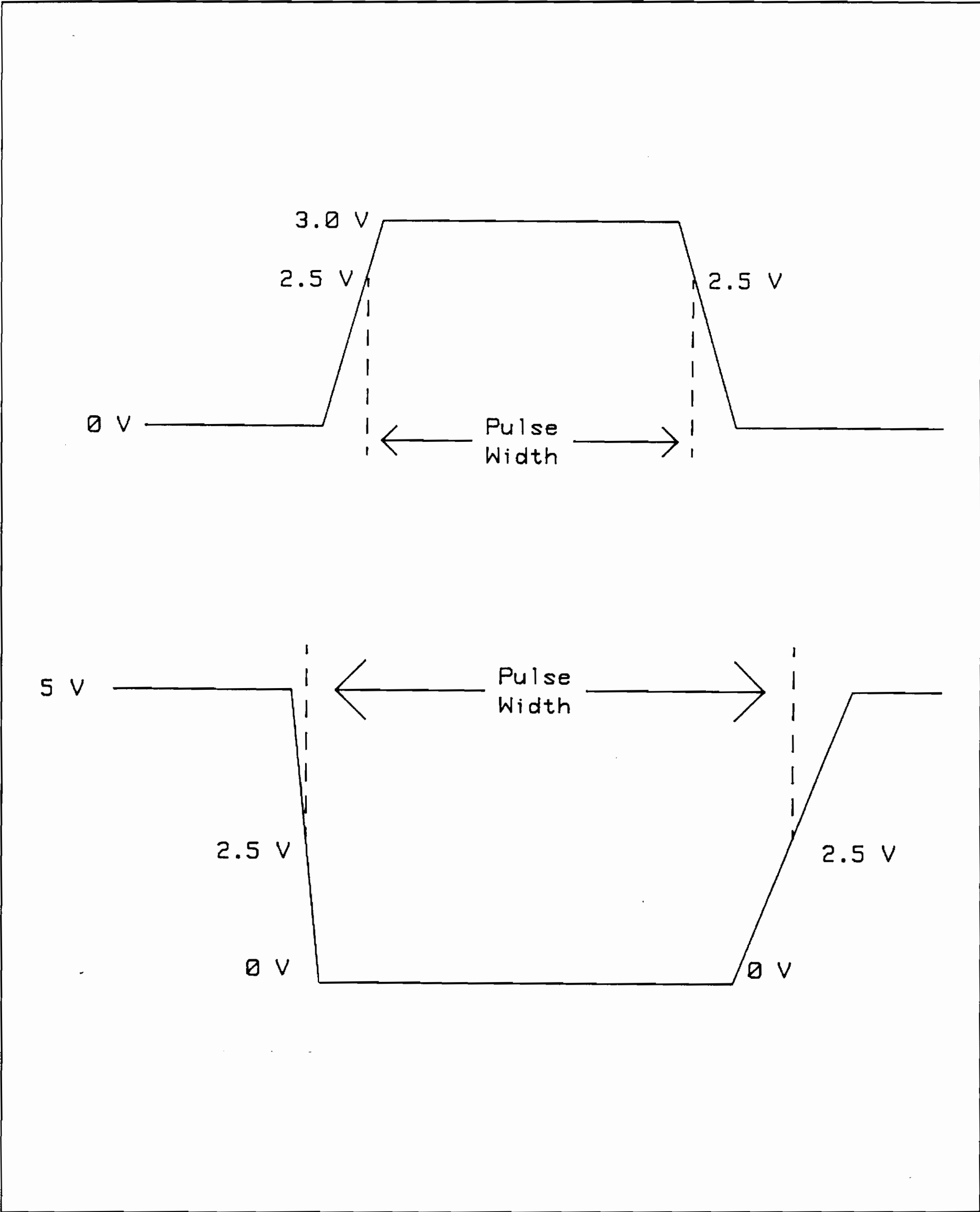


Figure 8. Representation of Pulse Width

4.2.6 Delay Times:

The delay time is defined as the time it takes for a logic transition to pass from the input to the output of a device. The delay time measurement, as shown in Figure 9, is taken to be the time elapsed from when the input signal crosses the defined threshold voltage to when the output voltage crosses the same threshold voltage. As mentioned earlier, this threshold voltage is taken to be 2.5 V.

4.2.7 Flip-Flop Design:

The flip-flop used in the simulations is a simple D-type flip-flop as shown in figure 10. It consists of two transmission gates and two INVERTERS. When the clock is high, the output Q is set to D, and the output value is latched on the falling edge of the clock pulse. When the clock transitions to 0, a feedback path around the INVERTER pair is established. This causes the current state of Q to be stored. The input is ignored when the clock is zero. Figure 11 is an example of when a transient pulse at the input of the flip-flop is not latched at its output. Figure 12 is an example of when a transient pulse at the input of a flip-flop is latched at its output.

4.2.8 Conversion from RADS to Volts:

The energy transferred to a material by ionizing radiation is measured in terms of **rads (Radiation Absorbed Dose)**. The effect of radiation incident on a circuit is the generation of a voltage transient. This section shows how to convert the incident radiation given in units of rads to the effect felt at the circuit node in terms of volts.

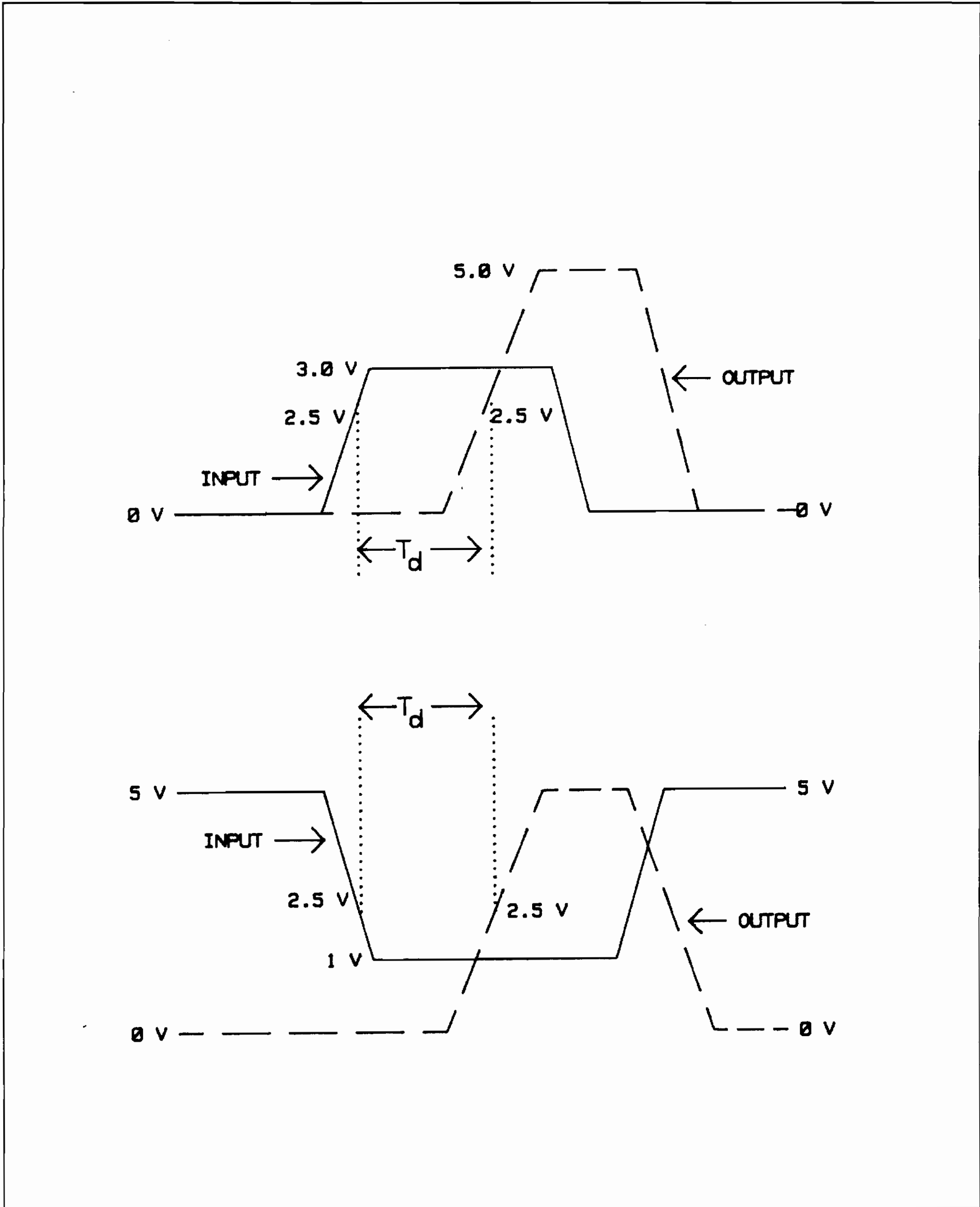


Figure 9. Representation of Delay Time for inverting & non-inverting gates

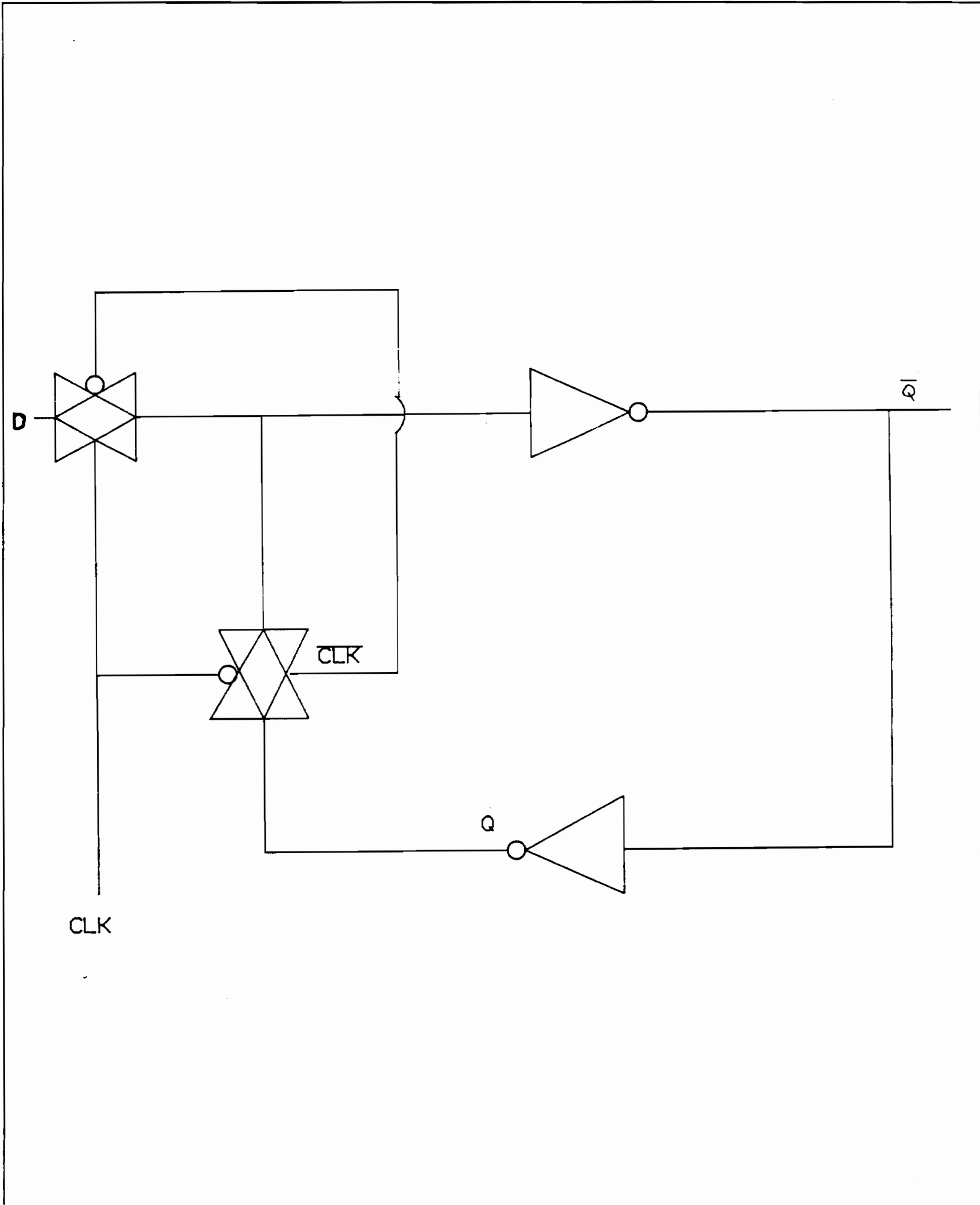


Figure 10. D flip-flop

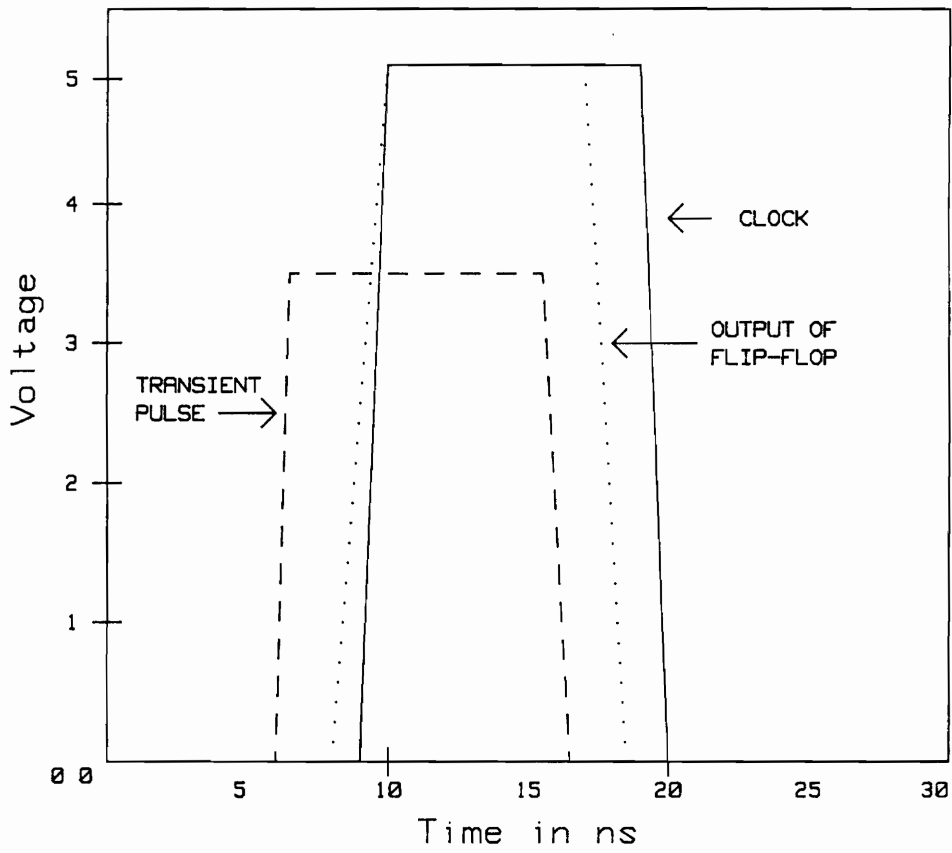


Figure 11. Transient pulse not latched on at output of flip-flop

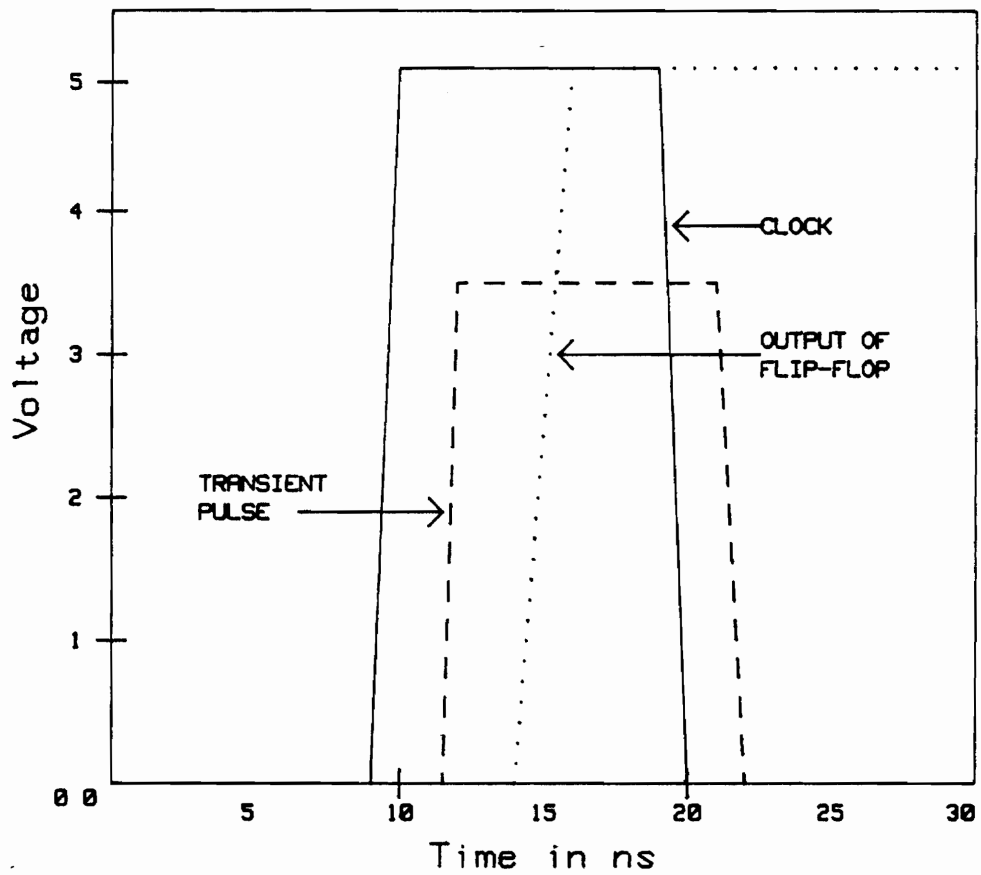


Figure 12. Transient pulse latched on at output of flip-flop

One rad of ionizing radiation transfers 100 ergs of energy per gram of material. The material must be specified, because this energy will differ with each material.

Thus, when one gram of silicon is irriadiated by one rad (silicon) of radiation, 100 ergs of energy are transferred from the radiation to the silicon. The intensity, also known as the ionizing dose rate of radiation, is measured in rads/sec. A typical range of the intensity of radiation studied in the radiation hardening problem is 10^4 to 10^7 rad/sec.

It is evident that as the dose increases, the number of carriers generated in silicon will also increase. In the space environment, a device may be subjected to an extremely large dose with a short period of time (up to a few nanoseconds).

Now how do these terms relate to the actual device? Let us consider, what happens when one rad of radiation strikes a particular node in the circuit.

1 rad = 100 ergs/gram * 2.33 gram/cm^3

Converting ergs to joules gives,

1 rad = 100 * 10^{-7} Joules/gram * 2.33 gram/cm^3

$\therefore$ 1 rad = 2.33 * 10^{-5} Joules/cm^3

Multiplying each side by 10^4 and converting from cm^3 to μm^3, we have

10^4 rads = 2.33 * 10^{-12} Joules/μm^3

Now consider the affected gate volume, for example,

$L = 3\mu m$; $W = 4.5\mu m$; $t = 0.04\mu m$

giving a volume = $0.54\mu m^3$

Taking the affected volume into account,

10^4 rads = $2.33 * 0.54 * 10^{-12}$ Joules

$\therefore$ 10^4 rads = $1.26 * 10^{-12}$ Joules

Now W_E, the energy stored in a capacitor is given by $0.5CV^2$

$\therefore$ $V = (2W_E/C)^{0.5}$

$V = (0.252 * 10^{-12} / 0.011pF)^{0.5}$

where the value of the capacitance is obtained from the given device dimensions.

$\therefore$ $V = 4.78$ V

Thus, radiation of 10^4 rads on a volume of $0.54\mu m^3$ equals $1.26 * 10^{-12}$ Joules of energy, which is equivalent to a voltage spike of 4.78 V at that node.

Alternatively, the voltage spike generated by the ionizing radiation could be determined from the number of electron-hole pairs. The radiation is absorbed by the silicon bulk, creating electron-hole pairs. To create a single charge pair, 3.6 eV is required [22]. Then 1 rad (Si) of radiation generates a total of

$$\frac{100(erg/gram) * 2.33(gram/cm^3)}{10^7(erg/Joule) * 1.6*10^{-19}(Joule/eV) * 3.6(eV/pair)} = 4*10^{13} \text{ (e-h)/cm}^3 \qquad (1)$$

electrons and holes. In the above equation, 2.33 gram/cm^3 is the density of Si, 10^7 erg/joule, 1.602 * 10^{-19} Joule/eV, and 3.6 eV/pair are physical constants.

The voltage generated by the ionizing radiation could be determined from above equation. Assuming that no carrier recombination takes place, the product of the number of electrons and the charge of an electron gives the total charge transferred to the circuit. Since the capacitance at that node is known once the geometry is specified, the voltage can easily be found using the relation V = Q / C.

Considering the same amount of radiation to be incident on the same volume as given in the last example, the total charge transferred to the circuit is:

$$Q = (4 * 10^{13}) * (10^5) * (1.6 * 10^{-19}) * 10^{-12}\ C/\mu m^3$$
$$\therefore\ Q = 0.64 * 10^{-12}\ C/\mu m^3$$

where 1.6 * 10^{-19} is the charge of an electron, 10^5 is the ionizing radiation in rads, and 10^{-12} is the conversion factor from cm^3 to μm^3.

$$V = Q / C = (0.32 * 10^{-12}\ C/\mu m^3) / (0.01\ pF)$$
$$\therefore\ V = 3.2\ V$$

Thus, the voltage spike generated has an amplitude of 3.2 V. Taking into account the assumptions made in this model, this value of voltage is in reasonable agreement with the value obtained from the earlier method. The program SUPER uses the first method to convert from rads to volts.

4.3 Simulation Results

Simulations are performed on blocks of combinational logic consisting of NAND gates, NOR gates and INVERTERS, configured as shown in Figures 13 to 15.

The simulations are performed on all the gates and the voltage pulses were varied in amplitude from 0 to 15 V and vice versa. In this way the effect of having the input transition from 0 --> 1 and 1 --> 0 is studied. The voltage pulses are varied in steps of 0.5 V, except between 2 V and 4 V, where they are varied in steps of 0.1 V. The pulse width is varied from 1 ns to 10 ns in steps of 0.1 ns. The time the radiation is incident is varied from 2 ns before the rising edge of the clock to 9 ns after the rising edge of the clock pulse, in steps of 1 ns.

In Figures 16 through 21 are shown pulses of various amplitudes and pulse widths input to node A of the first gate in the chain of gates in the path leading to the flip-flop. Along with the inputs the resultant pulse produced at the output of the last gate in the chain, which is the input to the flip-flop is shown. The figures also show the clock pulse, and the waveform produced at the output of the flip-flop.

Consider the series of NAND gates of Figure 13. The effect of a voltage pulse of 3.0 V with a 5 ns pulse width incident on node A of gate # 1 is shown in Figure 16. From the data file it is seen that this 3.0 V pulse produces a 5 V output after two stages, but there is a degradation of the pulse width. By the time the pulse reaches the input of the flip-flop, it has shrunk to 4.2 ns.

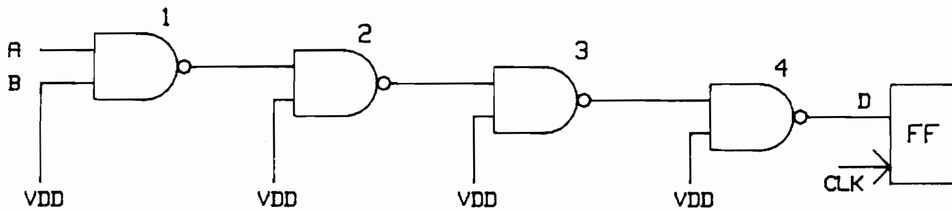


Figure 13. Four NAND gates in series with a flip-flop

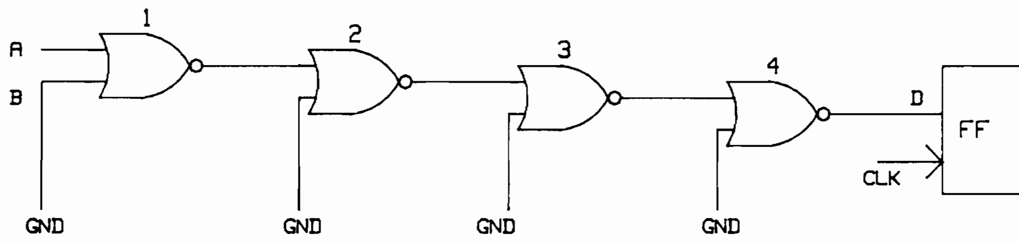


Figure 14. Four NOR gates in series with a flip-flop

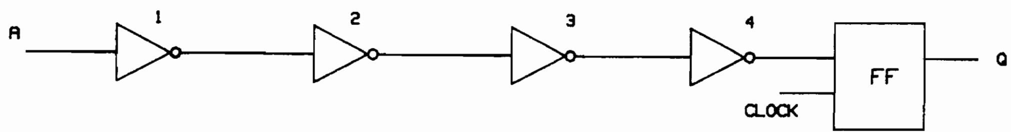


Figure 15. Four INVERTERS in series with a flip-flop

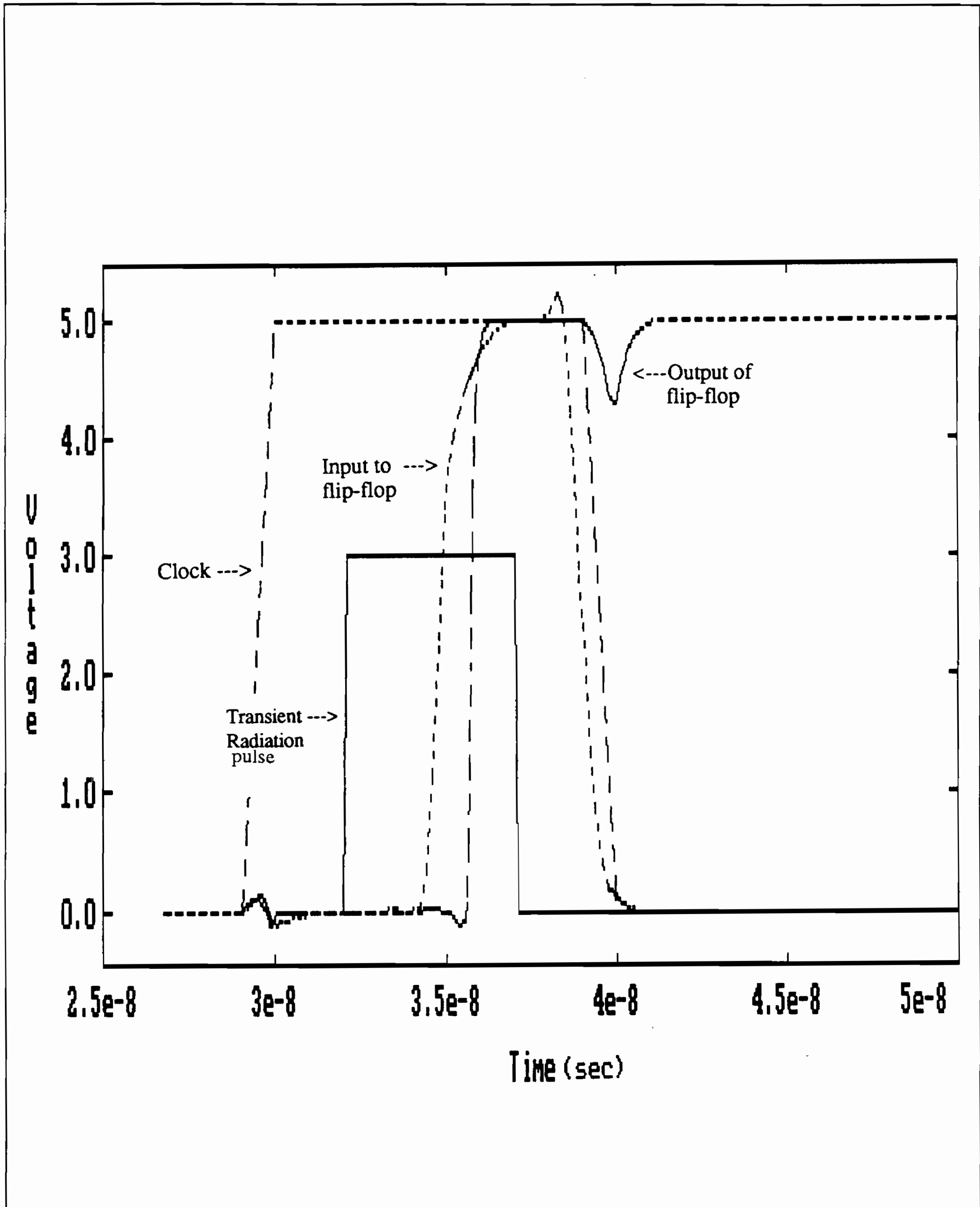


Figure 16. Timing diagram of a 0 --> 1 pulse applied to a NAND gate path

Since the clock is high when the voltage transient reaches the input of the flip-flop, the output of the flip-flop follows the input and also goes high. Just before the output return to its unperturbed state of low, the clock goes low, and so the output is latched at a logic 1 and is thus considered to be upset.

Shown in Figure 17, is the case where a pulse of magnitude 5.0 V and width of 5 ns is applied to node A of gate # 1. The normal voltage applied to the gates is 5 V.

This transient pulse is negative with respect to the normal input and causes a transition from logic 1 --> 0. Since this is a strong pulse (any pulse with amplitude greater than 3.5 V is considered to be a strong pulse as it can be pulled up to 5 V), it is propagated through 4 gates, to the input of the flip-flop without any degradation.

Since the clock is high when the voltage transient arrives at the input of the flip-flop, the output of the flip-flop follows the input and goes low. While the output is low, the clock goes low, and so the voltage transient is latched and the output of the flip-flop stays low even though the input returns high after 5 ns.

Consider the series of NOR gates in Figure 14. Shown in Figure 18 are the effects of a voltage pulse of 2.5 V having a pulse width of 9 ns, incident on node A of NOR gate # 1. Since the amplitude of the pulse is near the switching voltage, it barely manages to toggle the output of gate # 1. However, as the effect of the transient pulse propagates through to the input of the flip-flop, the signal reaches an amplitude of 5 V.

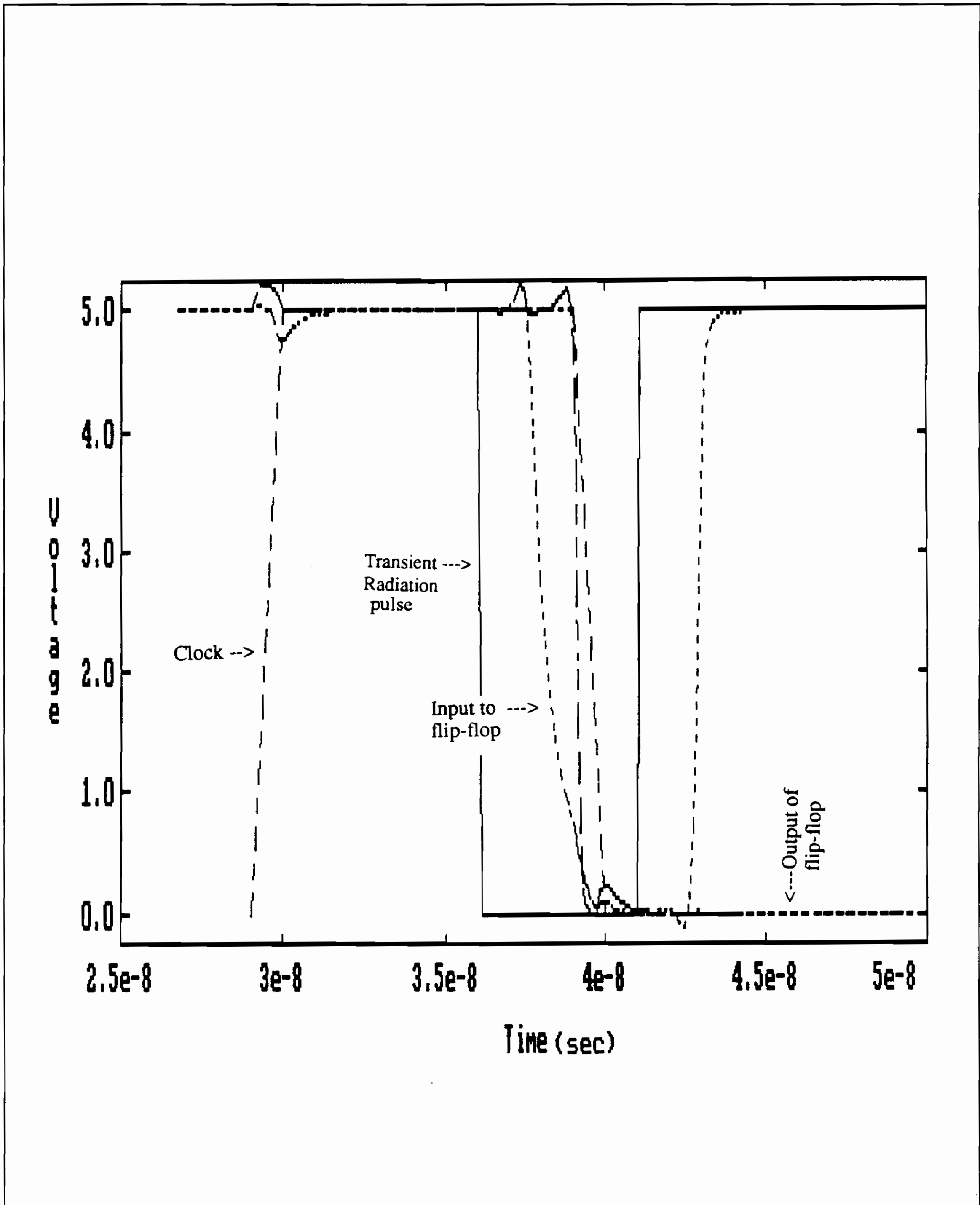


Figure 17. Timing diagram of a 1 --> 0 pulse applied to a NAND gate path

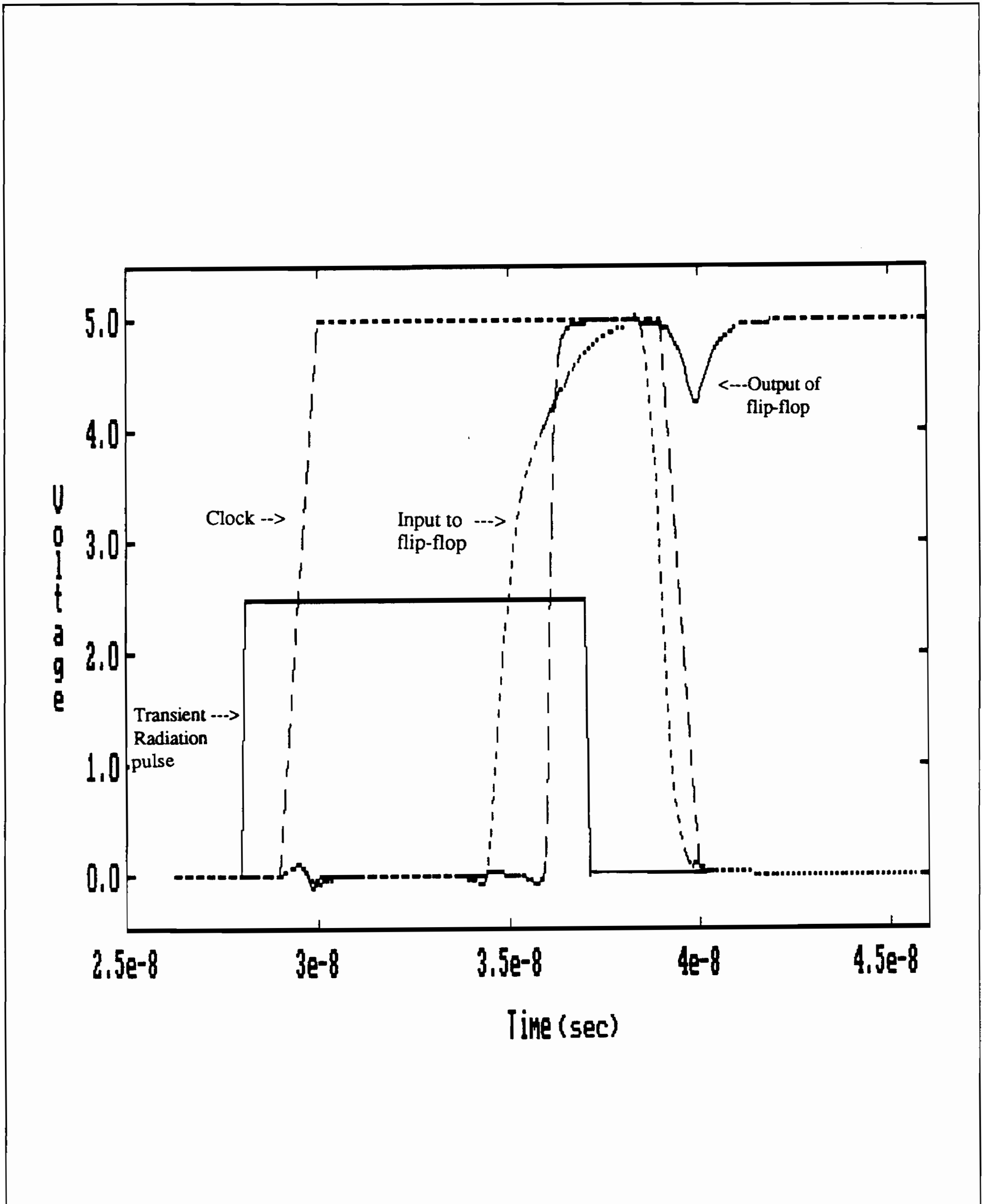


Figure 18. Timing diagram of a 0 --> 1 pulse applied to a NOR gate path

Note however, that the transient pulse width has degraded from 9 ns to 4 ns. Even so, the transient still manages to cause an upset, because its arrival time is such that it coincides with the falling edge of the clock pulse and thus an erroneous value is latched.

Figure 19 shows the effect of a 5 V transient pulse with a pulse width of 2 ns, incident on node A of NOR gate # 1. An upset is caused in this case since the voltage transient is present at the input of the flip-flop when the clock goes low. After passing through four gates, there is only a slight degradation of the pulse. The amplitude falls from 5.0 V to 4.5 V and the pulse width decreases to 1.7 ns.

This is because the transient pulse width is very narrow. Hence before the output of the gate reaches it's final value, the input changes states. Even so, the transient manages to cause an upset.

Consider the series of INVERTERS of Figure 15. The effect of a 3.0 V pulse of width 3 ns, as it is propagated through four INVERTERS to the input of the flip-flop is shown in Figure 20.

The pulse at the input of the flip-flop is a 5 V pulse (5 --> 0 V), with a pulse width of 2 ns. The output of the flip-flop follows the input. Just when the output is rising back to 5 V, the clock goes low, and the output of the flip-flop is latched to logic 0 and thus is considered to be an upset.

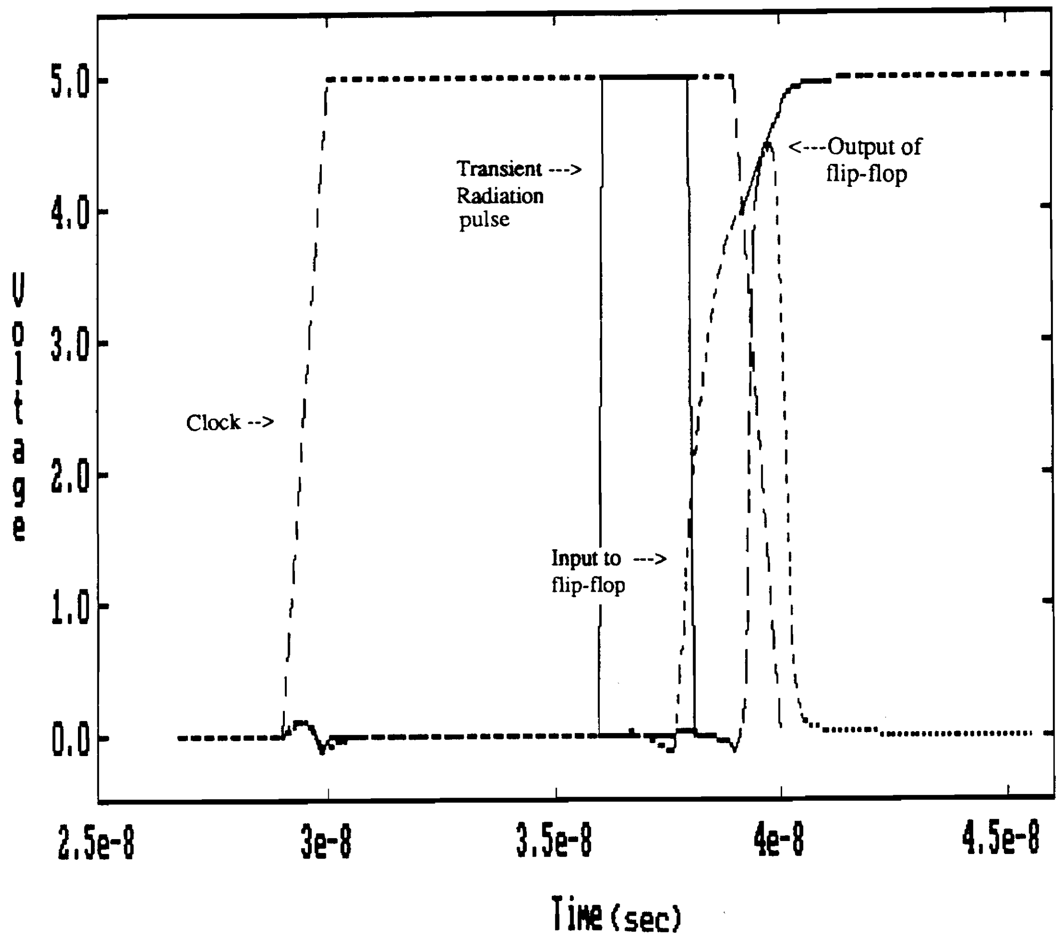


Figure 19. Timing diagram of a 0 --> 1 pulse applied to a NOR gate path

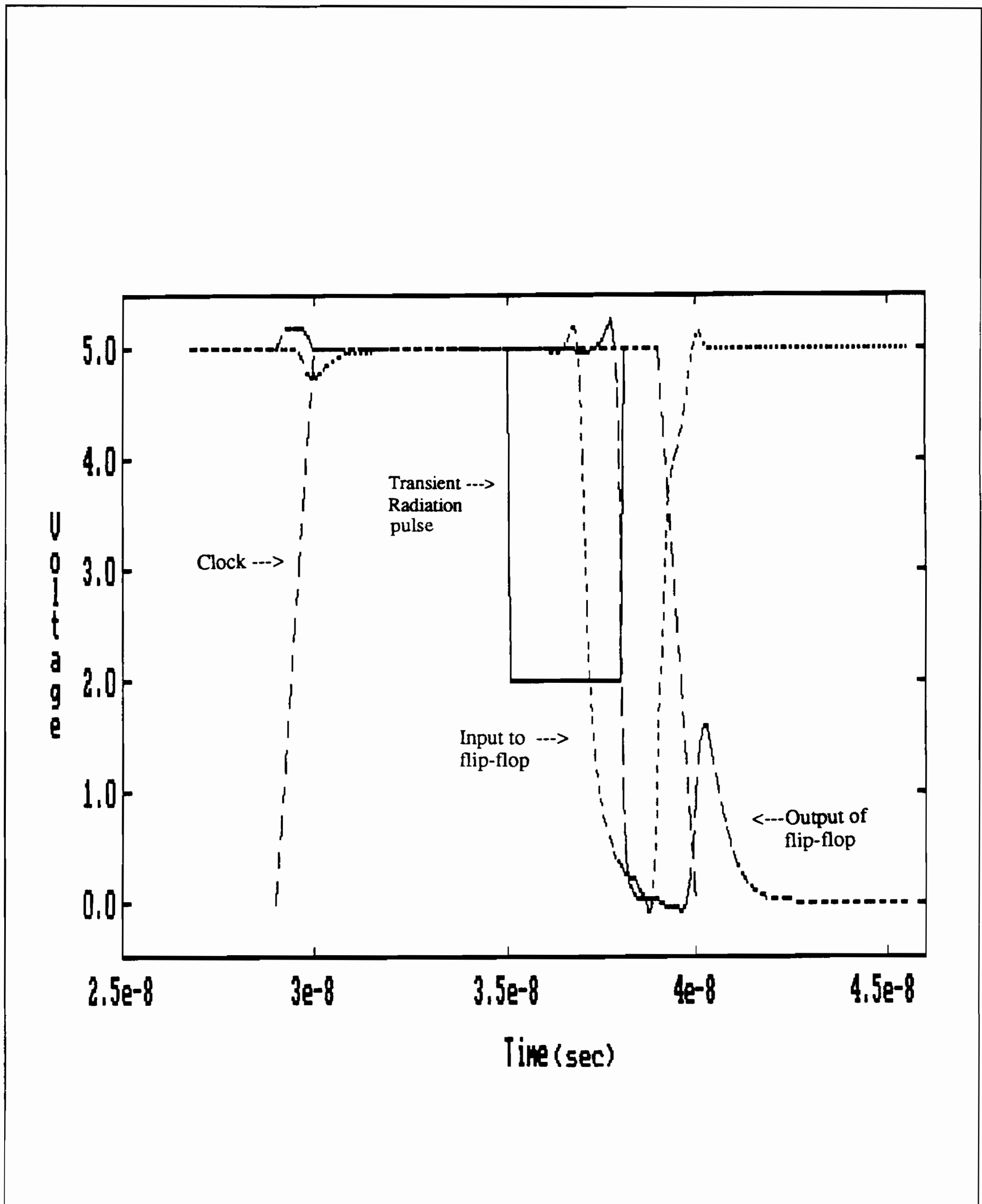


Figure 20. Timing diagram of a 1 --> 0 pulse applied to an INVERTER path

Figure 21 shows the circuit response when a 10 V pulse is incident on the circuit. The behavior of this pulse is the same as that of a 5 V pulse, as it is pulled down to the supply voltage, which is 5 V in this case.

The concept of an **Upset Window** was introduced in this thesis. An upset window is a three dimensional way to graphically represent a large amount of simulation data. An upset window shows whether an upset is caused when ionizing radiation with certain energy characteristics, duration, and arrival time, impinges on a circuit. Ionizing radiation on combinational logic that falls within an upset window, causes an observable change at the output of the flip-flop.

Each upset window represents the data obtained from approximately 300 simulations. The susceptibility of any combinational logic directly depends on the area enclosed within an upset window. The larger the window, the more the upset susceptibility.

Upset windows for the circuits in Figures 13 to 15 are shown in Figures 22 through 27. Figure 22 shows the upset windows for the circuit of Figure 13 , which consists of four NAND gates in series with a flip-flop. This upset window pertains only to a 0 --> 1 logic transition when the transient pulse is incident on node A.

By examining the different upset windows, it is seen that in general NAND gates are more susceptible to upsets than NOR gates for a 0 --> 1 transition. The Upset Windows for the 2.5 V and 2.7 V pulses are much larger in area for the NAND gate than for the NOR gate.

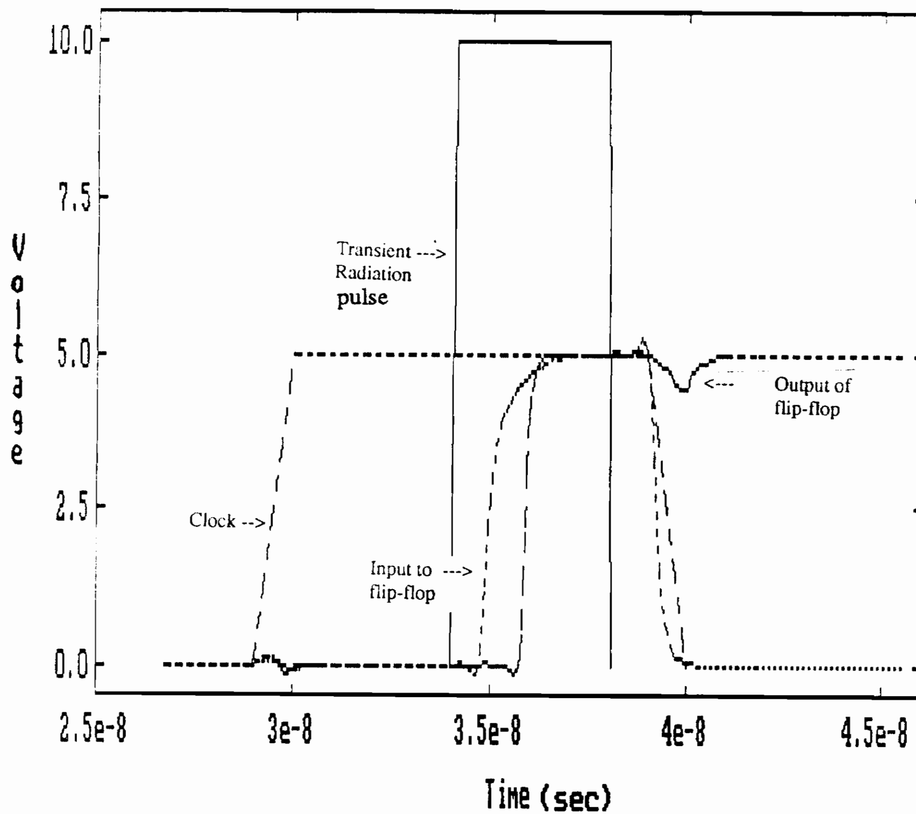


Figure 21. Timing diagram of a 0 --> 1 pulse applied to an INVERTER path

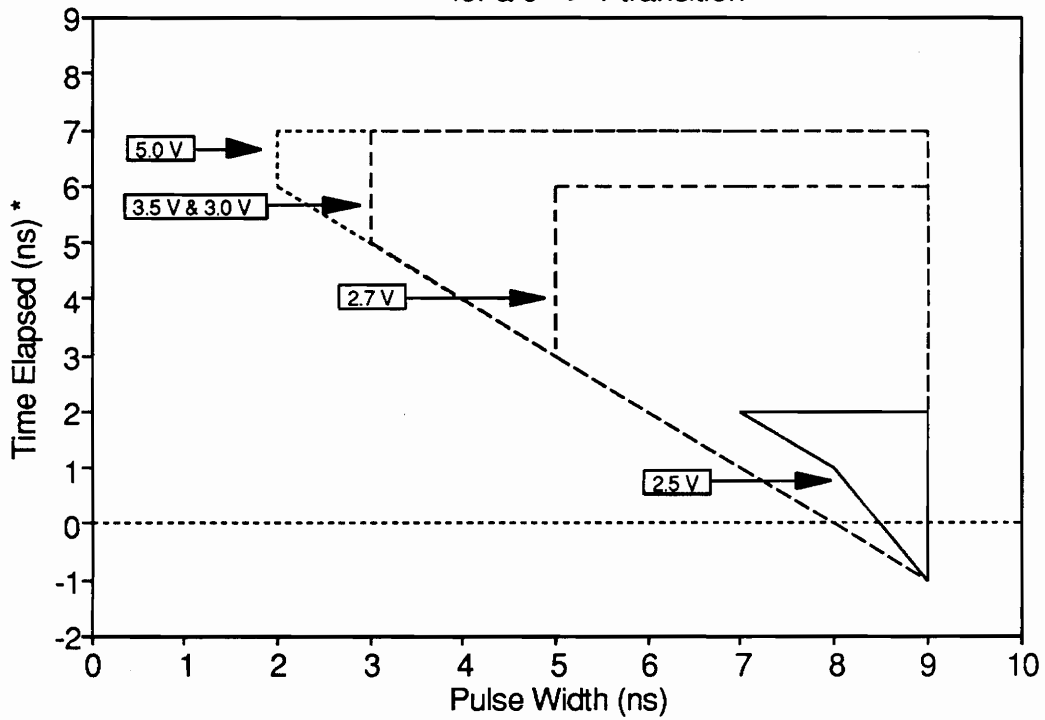


Figure 22. Upset Windows for the NAND gate chain for 0 --> 1 transition

In fact, in the case of the NOR gate, the upset window for a 2.5 V transient pulse is just a single point. A 2.5 V pulse, in this case, would cause an upset only if it has a pulse width of 9 ns and it is incident on the circuit at node A 1 ns before the rising edge of the clock pulse.

The windows in this figure correspond to upsets caused by voltage pulses of 2.5 V, 2.7 V, 3.0 V, 3.5 V and 5.0 V, respectively. Figure 23 shows the upset windows for the same circuit but for a 1 --> 0 logic transition.

Figure 24 shows the upset windows for the circuit of Figure 14, which consists of four NOR gates in series with a flip-flop, or a 0 --> 1 transition.

Once again, the windows in this figure correspond to upsets caused by voltage pulses of 2.5 V, 2.7 V, 3.0 V, 3.5 V and 5.0 V. Figure 25 shows the upset windows for the same circuit but for a 1 --> 0 transition.

Figure 26 shows the Upset Windows for the circuit of Figure 15, which consists of four INVERTERS in series with a flip-flop, or a 0 --> 1 transition. The windows in this figure correspond to upsets caused by voltage pulses of 2.5 V, 2.7 V, 3.5 V and 5.0 V. Figure 27 shows the upset windows for the same circuit but for a 1 --> 0 transition.

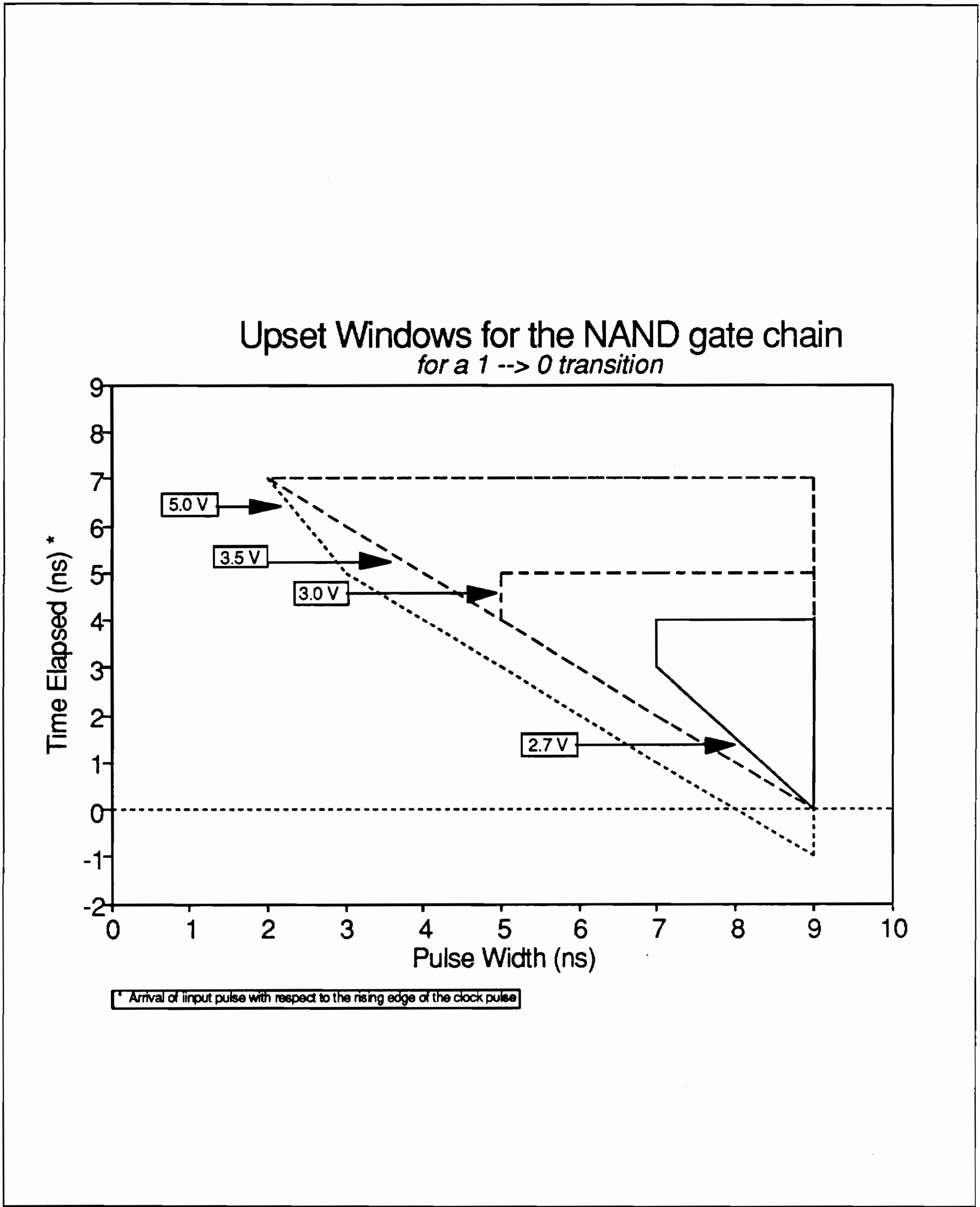


Figure 23. Upset Windows for the NAND gate chain for 1 --> 0 transition

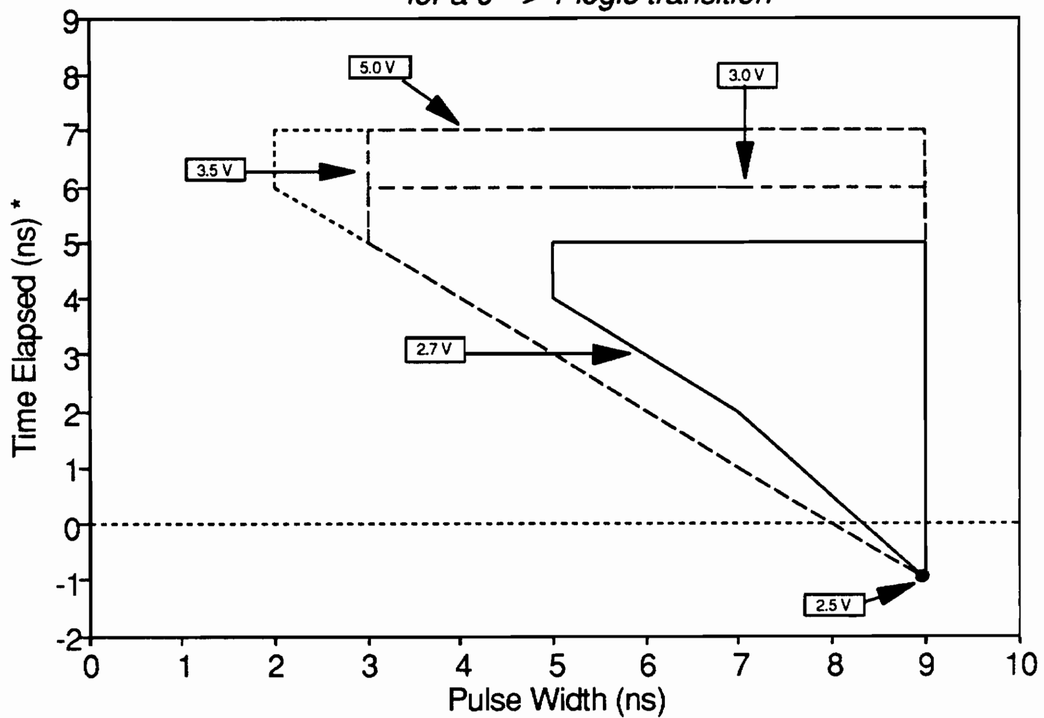


Figure 24. Upset Windows for the NOR gate chain for 0 --> 1 transition

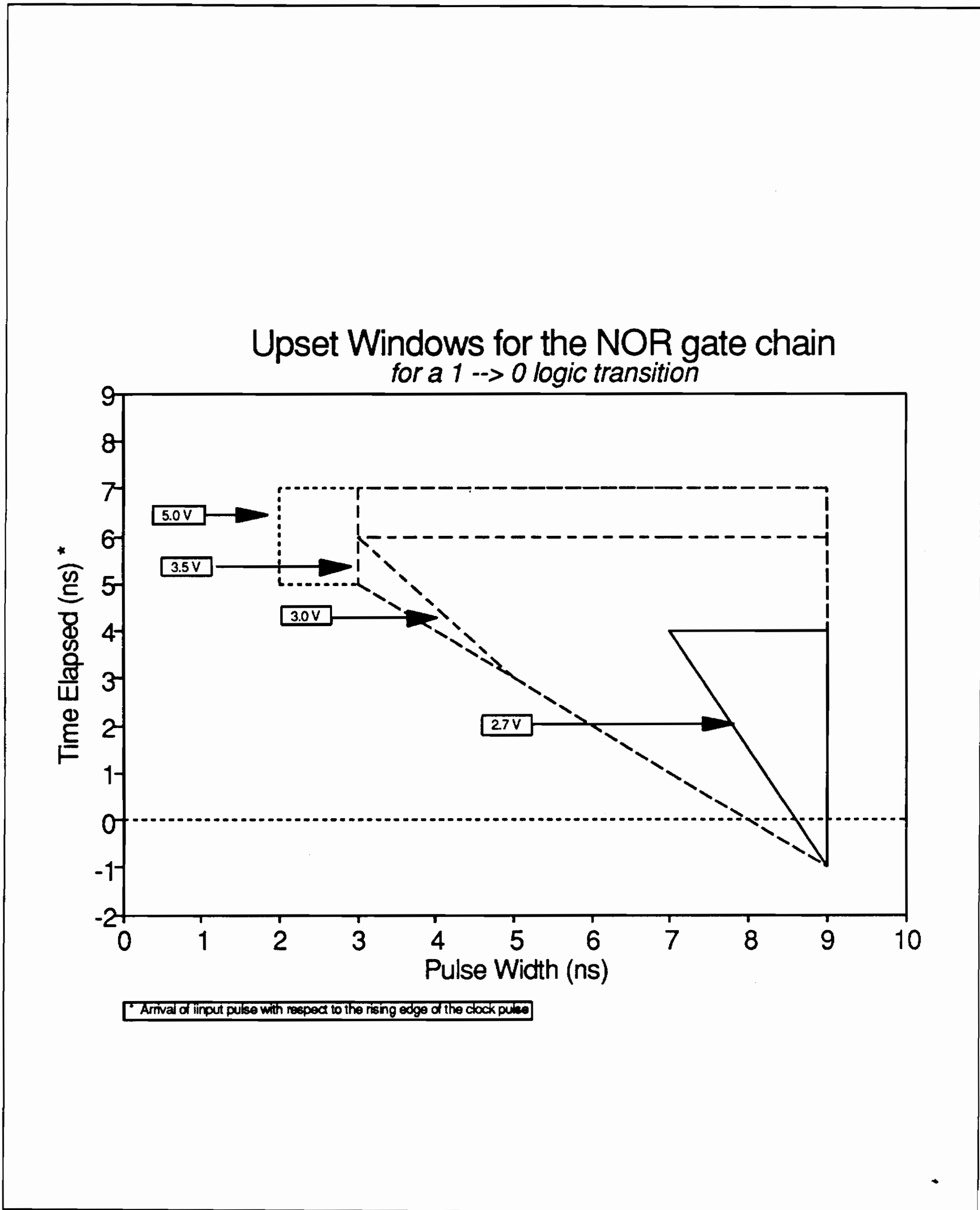


Figure 25. Upset Windows for the NOR gate chain for 1 --> 0 transition

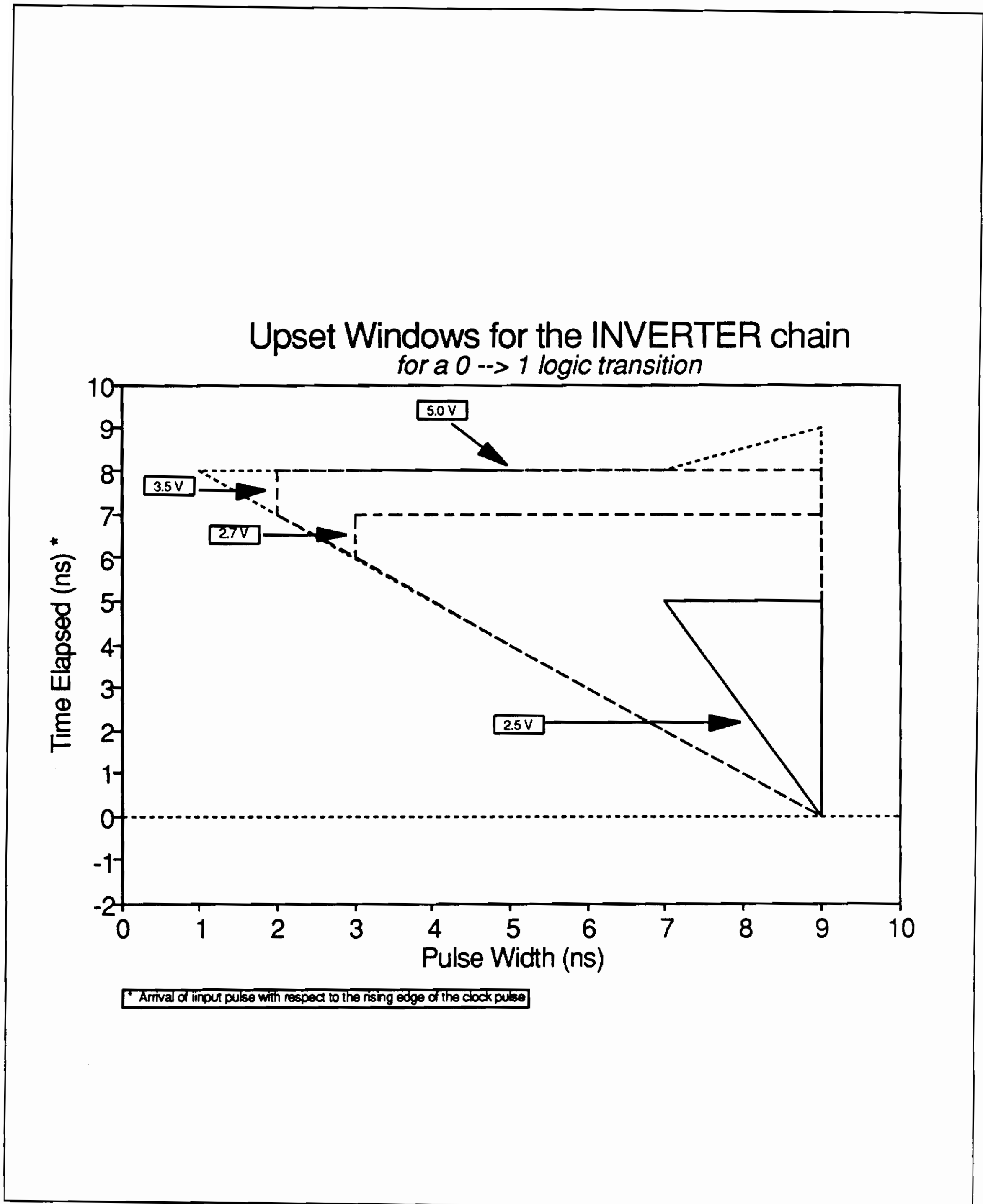


Figure 26. Upset Windows for the INVERTER chain for 0 --> 1 transition

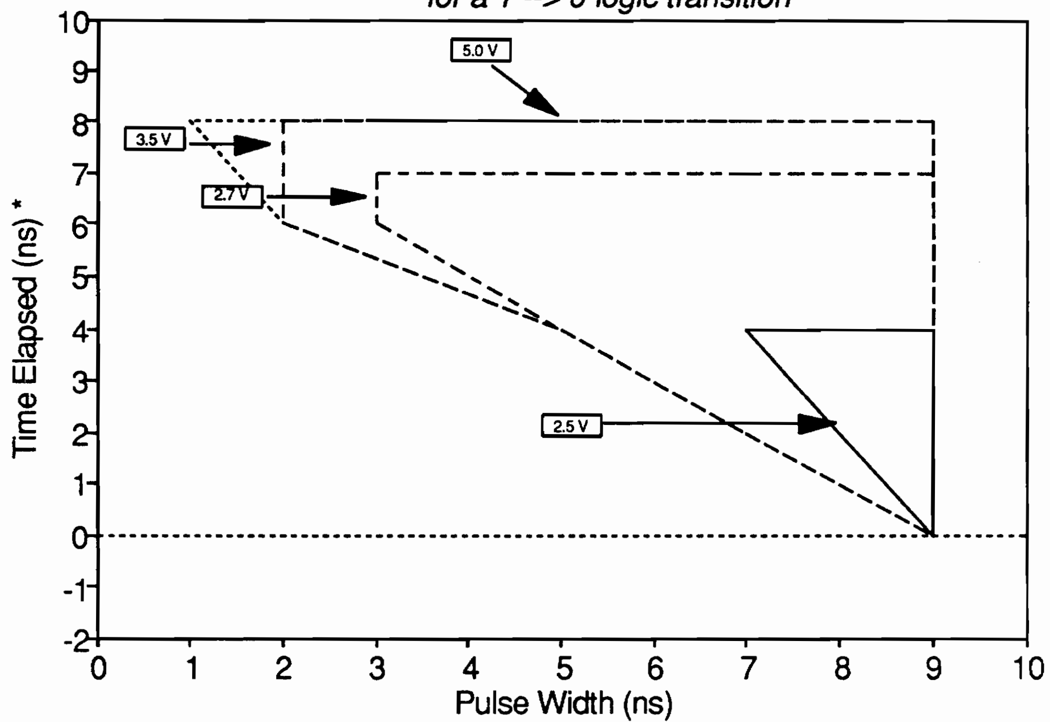


Figure 27. Upset Windows for the INVERTER chain for 1 --> 0 transition

In the case of a 1 --> 0 transient input, it is observed that the NOR gate is more susceptible to upsets than the NAND gate. This is indicated by the fact that the upset windows for the NOR gate cover more area than those of the NAND gate. The output transition from a logic 1 to a logic 0 takes place when the input voltage drops a little more than 2.5 V. As such, a 2.5 V pulse does not cause an upset. Hence there is no upset window for this 1 --> 0 transition. Notice that for the 1 --> 0 upset windows, the different voltage levels annotated beside the upset windows indicate negative voltage drops. For example, the 3.5 V upset window, actually indicates the upsets occurring when the voltage drops from 5.0 V to 1.5 V. Similarly, the 5.0 V upset window shows the upsets occurring when the voltage drops from 5.0 V to 0 V.

The INVERTER is observed to be more susceptible to upset than either the NAND or the NOR gates. The areas covered by the upset windows of the INVERTER for different voltage pulses are larger than the upset windows for the corresponding voltage pulses for either the NAND or the NOR gates. This can be attributed to the smaller number of transistors in the inverter, and hence smaller propagation delay time.

Based on the physical dimensions of the individual transistors in the logic gates, the p-transistors have an equivalent on-resistance of 2R, while the n-transistors have an equivalent on-resistance of R. Depending on the logic state of the transistors, the equivalent resistance is taken to be between V_{dd} and the output node or between V_{ss} and the output node. By studying the basic layout of the gates, it is seen that for a 0 --> 1 transition, the NAND gate has an equivalent on-resistance of 2R versus the 4R of the NOR. Having a higher resistance makes the NOR gate slower, and thus more upset tolerant. In the case of a 1 --> 0 transition, the NAND gate again has an equivalent on-resistance of 2R while that of the NOR gate is only R. Thus the NOR gate is more

susceptible than the NAND for 1 --> 0 logic transitions. In the case of the INVERTER, for the 0 --> 1 transition the equivalent on-resistance is 2R, while it is R for a 1 --> 0 transition. Hence, it is as susceptible as the NAND gate for a 0 --> 1 transition, and as susceptible as the NOR gate for a 1 --> 0 transition.

The data obtained from the simulations is stored in a rich database. The database consists of six files. There are two files each for the three gates. One of the two files of each gate in the database consists of the results obtained from the 0 --> 1 transition, while the other file consists of the results from the 1 --> 0 transitions. The program SUPER references the database to determine the response of a logic gate to the ionizing radiation.

5.0 SUPER - SUsceptibility PrEdiction pRogram

5.1 Introduction

SUPER is the acronym for the SUsceptibility PrEdiction pRogram. It is a simple user-friendly interactive program developed as a part of this thesis. It predicts the susceptibility of combinational logic circuits in a radiation environment. This chapter explains the complete working of the program. Section 2 gives a brief explanation of the program flow using pseudocode. Section 3 explains the operations performed by the program in detail. Section 4 contains a few examples of predicted susceptibility rates of sample circuits.

5.2 Pseudocode for SUPER

1) Input radiation level in rads or in volts. If rads is used then convert it to transient voltage.

2) Input the transient pulse width.

3) Input the number of gates in the critical path. This is the number of gates that precede a flip-flop.

4) Select the type of gate that the radiation is incident on, also the type of voltage pulse that the radiation causes (rising or falling). Then select the pulse width of the incident pulse.

5) Select the type of gate at each stage in the critical path. The voltage transient pulse toggles between rising and falling as it passes through each gate in the critical path.

6) The pulse width of the voltage transient for each gate in the critical path (after the first one) is determined automatically by referencing the database. The database contains the results of the circuit simulations. The user also has a choice of selecting the pulse width for any gate (overriding the pulse width obtained by the simulations).

7) Input the time in nanoseconds when the radiation was incident on the first gate with respect to the falling edge of the flip-flop clock pulse.

8) After searching through the database to determine the effect of the transient pulse on each of the gates, the program predicts if the voltage transient would be propagated to the input of the flip-flop. If the voltage transient propagates to the input of the flip-flop, the program predicts the upset probability by looking for transient pulse and clock pulse coincidence.

5.3 Program Algorithm

This section discusses the algorithm of the program SUPER. The initial inputs to the program are: ionizing radiation in rads or volts and, the pulse width of the voltage transient generated by the ionizing radiation. As mentioned earlier, simulations were done on the three basic logic gates and many combinations of the transient voltage and the pulse width were simulated. The results of these simulations, specifically the following: gate output voltage, resultant pulse width, and gate delay were stored in the database.

To observe the effect of the ionizing radiation on a chain of logic gates leading to a flip-flop, the tansient voltage and the pulse width at the input of the first gate are entered. The program then references the database and obtains the gate output voltage, the resultant puse width and, the gate propagation delay. This output voltage and pulse width are the input to the next gate in the chain. Based on the type of logic gate, the program again references the database and obtains new values for the output voltage and the pulse width. It continues this till the end of the chain is reached and the voltage transient is now at the input of the flip-flop.

The probability of the voltage transient propagating from the input of the first gate it is incident on, to the input node of a flip-flop is known as the **conditional probability**. This probability depends on the number of inputs to each gate and also the type of the gate. For example, there is a 50% chance that the output of a 2 input NAND gate will change states when one of the inputs does so (from Table 1), and so the conditional probability is 0.5. Now if the voltage transient passes through another NAND gate, the conditional probability will be 0.5 * 0.5 = 0.25.

Even if the voltage transient due to the ionizing radiation reaches the input node of a flip-flop, it might not be latched at the output of the flip-flop. This is because it might have been incident on the input node of the flip-flop when the flip-flop clock was low and become zero by the time the clock went high. Another reason for the voltage transient not being latched may be that it did change the state of the flip-flop, but could not hold on to it till the clock went low.

Whether a voltage transient at the input of the flip-flop be latched on or not is determined as shown in Figure 28. The clock pulse is divided into three regions A, B, and C. The voltage transient falls in these regions based on these conditions:

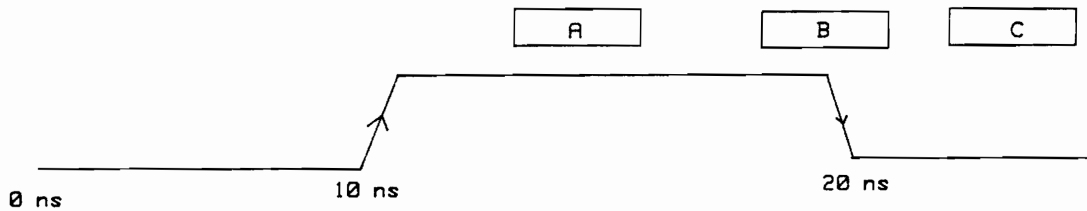
Region A: Reference time + Propagation delay time + Pulse Width < 20 ns.

Region B: Reference time + Propagation delay time + Pulse Width > 20ns AND

Reference time + Propagation delay time < 20 ns.

Region C: Reference time + Propagation delay time > 20 ns.

Here, the reference time refers to the time at which the voltage transient is incident on the input node of the flip-flop with respect to the rising edge of the flip-flop clock pulse. The upper limit on the time that can be input is 20 ns, because the clock period is 20 ns, and any time greater than 20 ns falls within the next clock cycle. Once a transient pulse arrives within the next clock pulse, the reference time also changes. Thus, the time of arrival of the radiation event is always taken to be between 0 and 20 ns of the start of any clock cycle. The start of the clock cycle is defined to be just after the falling edge of the clock. If the voltage transient occurs in regions A and C, as shown in the figure, it is not latched at the falling edge of the flip-flop and thus no error occurs.



A = REFERENCE + PROP DELAY + PULSE WIDTH < 20

B = REFERENCE + PROP DELAY + PULSE WIDTH > 20 &&
REFERENCE + PROP DELAY < 20

C = REFERENCE + PROP DELAY > 20

Figure 28. Timing diagram to determine upsets

The propagation delay time represents the time taken for the voltage transient to propagate from the input node of the gate on which the radiation event is incident to the input of the flip-flop. The pulse width refers to the pulse width the voltage transient has when it is at the input of the flip-flop.

The probability that the voltage transient at the input of the flip-flop is latched at its output is called the **coincidence probability**. The coincidence probability is the ratio of the transient pulse width at the input of the flip-flop to the period of the flip-flop clock.

The overall probability or the susceptibility, that the radiation event incident on node A causes the flip-flop to latch to an erroneous state is the product of the propagation probability and the coincidence probability.

5.4 Program Operation

This section gives a step by step description of the operation of the SUPER program. The program runs in an interactive window environment on the IBM PC or compatible. The source code of SUPER and the database files require about 1 MB of disk space. SUPER can run from a high density 1.44 MB floppy disk drive, and is not required to run from the hard disk. SUPER also does not require a co-processor or a VGA graphics card, and so can be operated from a basic computer system. Within the environment the user operates the program by using the arrow keys, the 'Y' and 'N' keys and the return key. Help can be obtained at any stage in the program by pressing the F1 key.

5.4.1 Radiation input to the circuit:

The program initially prompts the user to input the dose of radiation incident on the circuit. The incident radiation can be input either in rads or in volts. The user can toggle between the two input units modes by pressing either the space-bar key or the up & down arrow keys. Once a particular input mode is selected using the return key, the value of the incident radiation is next entered. If a voltage corresponding to the transient radiation is entered, then the program moves on to the next step. If the radiation is input in rads, then it is first converted to volts. The conversion of rads to volts is discussed in chapter 4.

The program next prompts the user to input the pulse width of the voltage transient. This pulse width is the time period for which the effect of the transient voltage pulse lasts at the incident gate. This time is in nanoseconds, and is usually from 0.1 ns to about 10 ns. Then the user enters the total number of gates in the critical path. After entering the number of gates in the critical path, specific details for each of the gates may be changed. The user must select from among the three basic gates: NAND, NOR, or the INVERTER. Next, the effect of the radiation is selected. This can be either a rising or a falling pulse. This effectively defines the unperturbed state of the circuit input to e either logic 0 when a 0 --> 1 transition is selected or logic 1 when a 1 --> 0 transition is chosen.

Based on the strength of the voltage transient and the type of gate, the resultant pulse width is determined from the database. When asked to input the pulse width, the default value from the database is selected (the value based on the simulation results), or a new value can be input by the user. Similarly the propagation delay time for the different gates is fixed, based on the simulation results. Once again the option exists to use values other than the default values.

5.4.2 Arrival time of voltage transient

Now the user must input the time at which the voltage transient is incident on the circuit with respect to the falling edge of the flip-flop clock pulse. Data is always assumed to be latched on the falling edge of the flip-flop clock. The clock used in the simulations is a free running 50 MHz clock with a rise and fall time of 1 ns, and a 50% duty cycle. The clock speed is taken to be 50 MHz as it is typical of the speed at which present day VLSI circuits operate. The option to change the time when the data is latched to the rising edge of the flip-flop clock and to change the clock speed also exists. These are program constants, and if they are changed, the source code of SUPER has to be compiled again.

The user can input any time between 0 and 20 ns, as the relative arrival time of the radiation-induced transient voltage. Once the arrival time of the transient is entered, the program goes through the database and determines whether or not the voltage transient is latched at the falling edge of the clock pulse and causes an error. If the voltage transient is latched, then the program calculates the probability of an upset. At this point, if the user wants to input another arrival time and see the probability of upset he can do so by simply pressing the 'Y' key and entering a new value. This allows the user to input different arrival times and form an upset window for that particular circuit. Pressing the return key at the prompt, causes the program to use the default 'N' input and exit.

If the user realizes that an incorrect input value has been entered during one of the previous stages, the option exists to go back to that stage at any time. Going to the previous stage can be done by pressing the page-up key. To go to values that were entered more than one stage before the present one, the page-up key must be depressed

more than once. After the correct value has been entered, the user can go step by step to the original point in the program by simply pressing the page-down key.

5.5 Examples

5.5.1 Example 1

Consider the circuit shown in Figure 29. The response of the circuit when ionizing radiation of $7 * 10^5$ rads is incident on node A for 5 ns is determined. Assume that the radiation is incident on node A, 10 ns before the falling edge of the clock pulse. To reach the flip-flop, the voltage transient generated by the radiation must to pass through 2 NAND gates, 1 INVERTER, and 1 NOR gate, in that order.

When SUPER is run, the first question asked in the interactive mode for the user to enter is the radiation level in rads or in volts. Input the radiation level in rads. For this example it is $7 * 10^5$ rads. The second question asked is for the user to enter the transient pulse width. For this example it is 5 ns. The third question asked is for the user to enter the number of gates in the critical path. Since there are 2 NAND gates, 1 INVERTER, and 1 NOR gate in the critical path, the number 4 is entered. The ionizing radiation of $7 * 10^5$ rads causes a voltage pulse of 6.7 V. This voltage pulse is assumed to be a rising pulse. For this transient to propagate through the NAND gate, the other input of this NAND gate is assumed to be at logic level 1. Thus, the output of the NAND gate goes from a logic level 1 to a logic level 0 (from 5 V to 0 V). The pulse width and the propagation delay are obtained from the database.

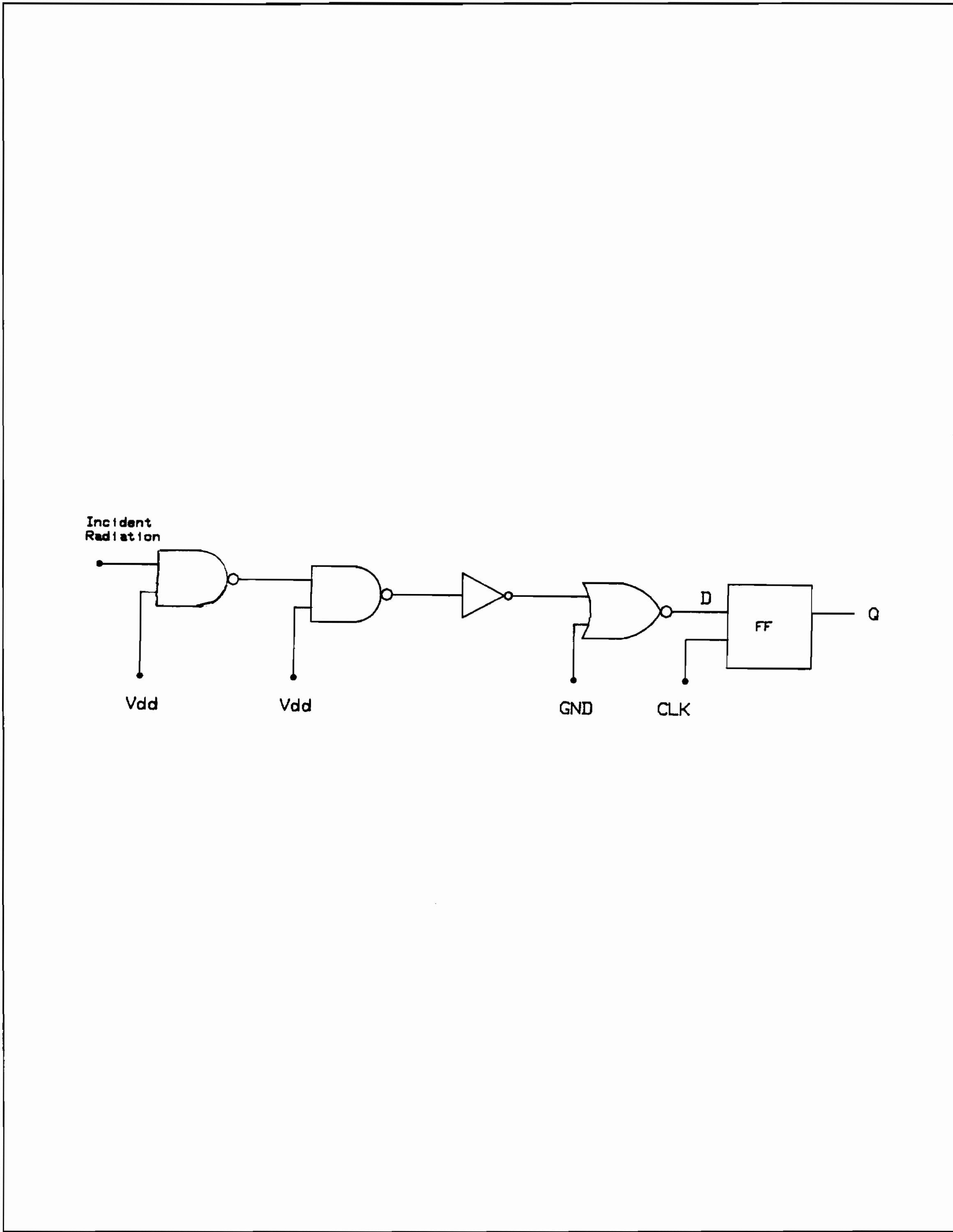


Figure 29. Circuit diagram of example 1

Now the output of the first NAND gate is 0 V, and the propagation probability is 50%. This is the input to the second gate in the chain, which is also a NAND gate. Since this input has changed from a logic 1 to a logic 0, the output of this NAND gate changes from a logic 0 to a logic 1. The propagation probability now is 50% of the propagation probability of upset after the first gate. So the propagation probability is now 25%. Now the output of the second NAND gate is the input to the INVERTER. So the output of the INVERTER is now a logic 0, instead of the logic 1. The probability of upset is still 25%, because the output of the INVERTER is always the complement of its input. This logic 1 at the output of the INVERTER is one of the inputs of the NOR gate, which is the last gate before the flip-flop. For this siganl to propagate to the NOR gate output, the other input of the NOR gate is considered to be a logic 0. When the voltage transient propagates through the NOR gate, it has changed the output of the NOR gate from a logic 1 to a logic 0. The propagation probability is now 50% of the earlier propagation probability, and so is 12.5%.

At this stage in the circuit, the effect of the voltage transient has propagated through four gates and is now at the input to the flip-flop. In order for the transient to pass the flip-flop and be latched at its output, the voltage transient must have changed the state of the flip-flop and be holding that change at the falling edge of the flip-flop clock. The voltage transient at node A occurs 10 ns before the falling edge of the clock pulse and lasts for 5 ns. So after considering the gate delays obtained from the database, it is seen that the voltage transient goes to zero 1.5 ns before the falling edge of the clock pulse. As such the transient error is not latched. If the same voltage transient occurred at node A, 8 ns before the falling edge of the clock pulse, then it would be latched at the falling edge of

the flip-flop clock. The clock period, in this case, is 20 ns, whereas the pulse width of the voltage transient is 5 ns, which means that the coincidence probability is 25%.

The overall probability that the radiation event incident on node A causes the flip-flop to latch to an erroneous state is the product of the propagation probability and the coincidence probability. In other words, the susceptibility, is 0.25 * 0.125, which is 0.0312. Thus, there is a 3.12% chance of the radiation event incident at node A propagating through the circuit and causing an observable upset at the output of the flip-flop.

5.5.2 Example 2

Consider the circuit shown in Figure 30. This circuit has a radiation of $4 * 10^5$ rads of width 7 ns incident on node A. The ionizing radiation is incident at node A 11 ns before the falling edge of the clock pulse. In this case the voltage transient generated by the radiation has to propagate through one NOR gate and one NAND gate to reach input node of the flip-flop. The radiation of $4 * 10^5$ rads gives rise to a voltage transient with an amplitude of only 2.0 V. Thus the voltage transient dies down and the output of the NOR gate does not change, and there is no upset.

5.5.3 Example 3

For this example again consider the circuit shown in Figure 30. For this example, it is assumed that the radiation incident on node A produces a voltage transient of amplitude 5 V with pulse width 10 ns. This voltage pulse is assumed to be a falling pulse. For this transient to propagate through the NOR gate, the other input of this NOR gate is assumed to be at logic level 0.

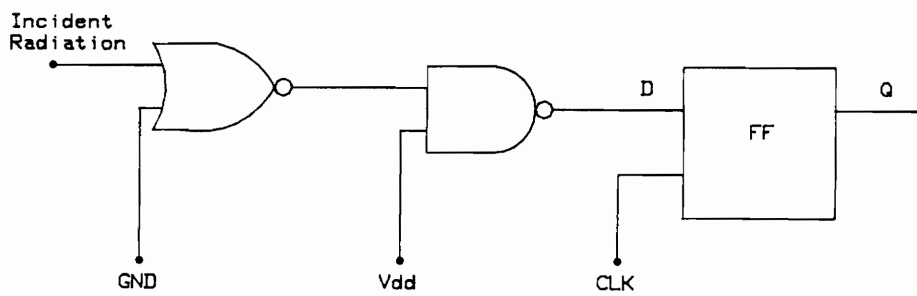


Figure 30. Circuit of examples 2 & 3

Thus, the output of the NOR gate goes from a logic level 0 to a logic level 1 (from 0 V to 5 V). The pulse width and the propagation delay are obtained from the database. The propagation probability is now 50%. The voltage transient is now at the input of the second gate in the chain, which is a NAND gate. Since this input has changed from a logic 0 to a logic 1, the output of this NAND gate changes from a logic 0 to a logic 0. The propagation probability now is 50% of the propagation probability of upset after the first gate. So the propagation probability is now 25%.

At this stage in the circuit, the effect of the voltage transient has propagated through the two gate chain and is now at the input to the flip-flop. In order for the transient to pass the flip-flop and be latched at its output, the voltage transient must have changed the state of the flip-flop and be holding that change at the falling edge of the flip-flop clock. The voltage transient at node A occurs 9 ns before the falling edge of the clock pulse and lasts for 10 ns. The coincidence probability is 50%. After considering the gate delays obtained from the database, it is seen that the voltage transient is latched at the output of the flip-flop. Thus in the case of this example, the susceptibility is In other words, the susceptibility, is 0.25 * 0.50, which is 0.125. Thus, there is a 12.5% chance of the radiation event incident at node A propagating through the circuit and causing an observable upset at the output of the flip-flop.

Chapter 6: Conclusion

The purpose of this research was to examine the logical response of combinational logic circuits to SEUs. Representative combinational circuits were modeled and simulated and their response to voltage transients produced by radiation was observed.

Over 3000 simulations were carried out on the three basic two input CMOS gates: NAND, NOR and INVERTER using RELAX. All possible combinations of voltage transient values, pulse widths, and transient arrival times were covered in the simulations. The concept of an upset window as it pertains to these logic gates was introduced. A program called SUPER (SUsceptibility PrEdiction pRogram) was developed. SUPER predicts the probability of a circuit error occurring given that ionizing radiation with certain energy characteristics impinges on an IC at a particular time and place.

Since the susceptibility is predicted for circuits operated in a radiation environment in space, temperature effects on circuit behavior need to be considered. Changes in temperature affect the electron and hole mobility and thus the switching voltage and the delay times may vary with the change of temperature. RELAX does not consider how temperature effects circuit behavior. Future research could take temperature effects into account and thus predict a more accurate susceptibility rate. Future research could also look into the area predicting susceptibilities of the VLSI circuits when they are scaled

down to sub micron sizes. Predicting the susceptibility in these cases, will be harder as parasitic resistances and capacitances and other second order effects will contribute substantially to circuit performance and will have to be considered. Future research could also look into modifying the upset windows so that they would include a fourth dimension. The fourth dimension would show upset windows for different technologies.

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VITA

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