High-Efficiency Low-Voltage High-Current Power Stage Design Considerations for Fuel Cell Power Conditioning Systems

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ABSTRACT

Fuel cells typically produce low-voltage high-current output because their individual cell voltage is low, and it is nontrivial to balance for a high-voltage stack. In addition, the output voltage of fuel cells varies depending on load conditions. Due to the variable low voltage output, the energy produced by fuel cells typically requires power conditioning systems to transform the unregulated source energy into more useful energy format. When evaluating power conditioning systems, efficiency and reliability are critical. The power conditioning systems should be efficient in order to prevent excess waste of energy. Since loss is dissipated as heat, efficiency directly affects system reliability as well. High temperatures negatively affect system reliability. Components are much more likely to fail at high temperatures. In order to obtain excellent efficiency and system reliability, low-voltage high-current power conditioning systems should be carefully designed.

Low-voltage high-current systems require carefully designed PCB layouts and bus bars. The bus bar and PCB trace lengths should be minimized. Therefore, each needs to be designed with the other in mind. Excessive PCB and bus bar lengths can introduce parasitic inductances and resistances which are detrimental to system performance. In addition, thermal management is critical. High power systems must have sufficient cooling in order to maintain reliable operation.

Many sources of loss exist for converters. For low-voltage high-current systems, conduction loss and switching loss may be significant. Other potential non-trivial sources of loss include magnetic losses, copper losses, contact and termination losses, skin effect losses, snubber losses, capacitor equivalent series resistance (ESR) losses, and body

diode related losses. Many of the losses can be avoided by carefully designing the system. Therefore, in order to optimize efficiency, the designer should be aware of which components contribute significant amounts of loss. Loss analysis may be performed in order to determine the various sources of loss. The system efficiency can be improved by optimizing components that contribute the most loss.

This thesis surveys some potential topologies suitable for low-voltage high-current systems. One low-voltage high-current system in particular is analyzed in detail. The system is called the V6, which consists of six phase legs, and is arranged as a three full-bridge phase-shift modulated converter to step-up voltage for distributed generation applications. The V6 converter has current handling requirements of up to 120A. Basic operation and performance is analyzed for the V6 converter. The loss within the V6 converter is modeled and efficiency is estimated. Calculations are compared with experimental results. Efficiency improvement through parasitic loss reduction is proposed by analyzing the losses of the V6 converter. Substantial power savings are confirmed with prototypes and experimental results. Loss analysis is utilized in order to obtain high efficiency with the V6 converter. Considerations for greater current levels of up to 400A are also discussed. The greater current handling requirements create additional system issues. When considering such high current levels, parallel devices or modules are required. Power stage design, layout, and bus bar issues due to the high current nature of the system are discussed.

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1 INTRODUCTION

This thesis will examine design considerations when developing high-efficiency low-voltage high-current power stages for fuel cell power conditioning systems. Electrical and mechanical factors will be considered in order to improve system efficiency as well as reliability.

1.1 Motivation

Isolated low-voltage high-current power systems have several potential applications. One common application is with renewable energy sources, such as fuel cells and photovoltaics, which tend to produce low-voltage high-current output and an output voltage that can vary depending on the load conditions. In addition to various alternative energy sources, batteries may also provide low-voltage high-current output. Many residential and industrial loads do not accept low-voltage high-current input. In order to convert the energy into something more useful, it should be processed using power conditioning circuitry.

One popular option for alternative energy generation systems is to return the renewable energy to the utility grid. By doing so, the stress on the utility grid and existing power plants can be reduced. Since less power is required from traditional polluting sources, there are environmental advantages. In order to return the power to the utility grid, a dc-ac inverter is required for fuel cell and photovoltaic systems. The dc-ac inverter requires a high dc voltage input in order to produce a proper ac waveform to send power back to the grid. Therefore, an isolated dc-dc converter is required to boost the voltage from fuel cells or photovoltaics. The dc-dc converter must be capable of taking low-voltage high-current input and producing high-voltage low-current output. The figure below shows the block diagram for a distributed generation system with isolation via high frequency transformer using a fuel cell as the initial power source.

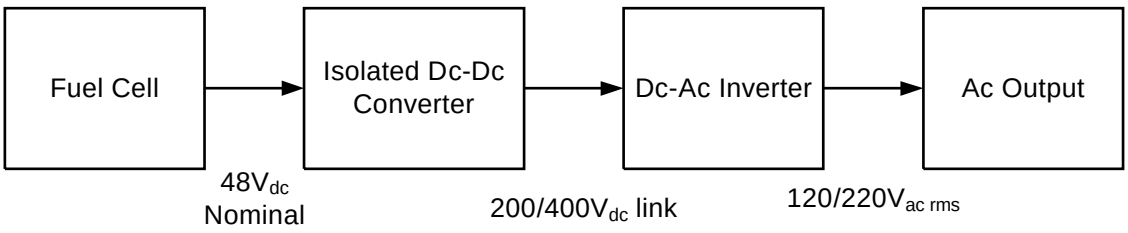

Figure 1.1 – Distributed generation via high frequency transformer

A less desirable alternative involves having a non-isolated dc-dc converter produce a relatively low dc voltage. The low-voltage dc feeds into a dc-ac inverter to produce a low-voltage ac output which then feeds into a 50/60Hz line frequency transformer. The line frequency transformer is able to boost the ac voltage to utility grid levels. The latter method involving the line frequency transformer is not desirable due to size and cost. Line frequency transformers are very large, heavy, and expensive due to the low operating frequency. The figure below shows the block diagram of a distributed generation system with line frequency transformer, again, using a fuel cell as the initial power source.

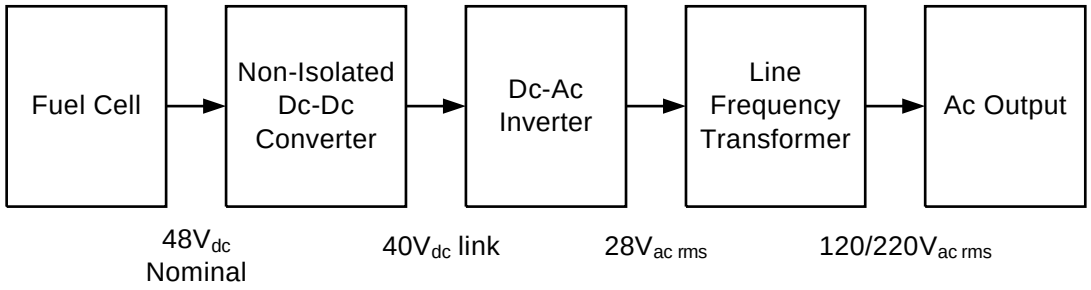

Figure 1.2 – Distributed generation via line frequency transformer

In order to reduce excess loss and improve system reliability, the system designer should consider many factors. In this thesis, an isolated dc-dc converter for step-up fuel cell applications is examined. Prototypes are constructed and experimental efficiency results are provided. Analysis of system losses is conducted in order to discover potential areas for efficiency improvement. Key design areas for low-voltage high-current systems are discussed in order to obtain high efficiency.

1.2 Sources of Loss

In every power conditioning system, regardless of input and output conditions, there are losses involved. Understanding potential sources of loss is critical in order to obtain high efficiency for a system. Losses can be categorized in two major groups. The first group consists of primary sources of loss such as conduction loss, switching loss, magnetic core losses, and copper losses. The second category of loss is parasitic loss. Parasitic losses may come from many different sources. For example, parasitic inductance, parasitic capacitance, capacitor equivalent series resistance (ESR), skin effect, proximity effect, body diode conduction, etc, all contribute parasitic losses to the system.

1.2.1 Conduction Loss

All semiconductor devices have conduction losses when current is flowing through them. Depending on the device, the voltage drop and therefore, the loss will be different. The conduction loss of a MOSFET can be calculated by considering the MOSFET as a resistor. The R_{DS-ON} of the MOSFET is the resistance used in the calculation. While estimates can be made, true loss will be slightly off due to variability in R_{DS-ON}. Variability in manufacturing can affect the R_{DS-ON} of individual devices but a nominal value can be utilized for loss estimation. Temperature also affects the R_{DS-ON} of a MOSFET. MOSFETs have a positive temperature coefficient. Therefore, as temperature increases, the R_{DS-ON} of the MOSFET will increase.

Diodes are another common source of conduction loss. The power loss through a diode can simply be calculated by multiplying the diode forward voltage and the current through the diode. The voltage drop across a diode is fairly constant but increases slightly with higher current. Variability in diode forward drop also exists much like the MOSFET. Manufacturing variability also affects diode forward drop voltage. In addition, temperature also affects the diode as well. Unlike the MOSFET, diodes have a negative temperature coefficient. Therefore, as the temperature increases, the diode voltage and loss will decrease.

Other semiconductor devices have different voltage drop and power loss characteristics. This thesis primarily considers MOSFETs and diodes for semiconductor devices but equivalent circuit models may be constructed for other devices. For example, an Insulated-Gate Bipolar Transistor (IGBT) may be modeled as a constant voltage drop and resistor in series.

1.2.2 Switching Loss

Under normal switching conditions, semiconductor devices consume power when switching to a different state. For example, when a MOSFET switches from the off state to the on state, initially, V_{DS} is high and I_D is zero. Under normal or hard switching condition, first, the current rises to the operating value and then V_{DS} drops to close to zero. The figure below shows a very simplified diagram of the MOSFET turn-on transition waveform.

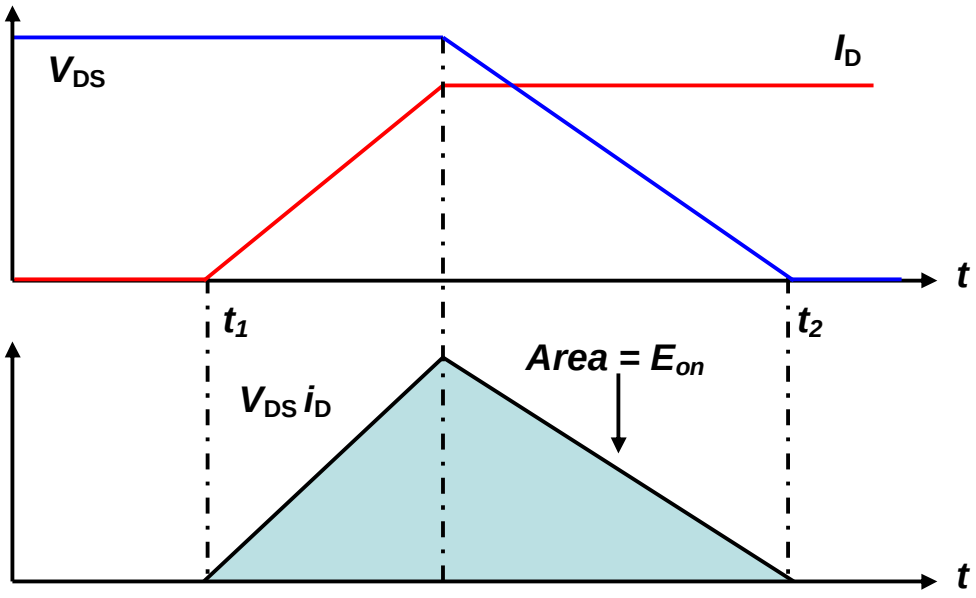

Figure 1.3 – Simplified MOSFET turn-on transition waveform

The next figure shows a simplified diagram of the MOSFET turn off transition waveform.

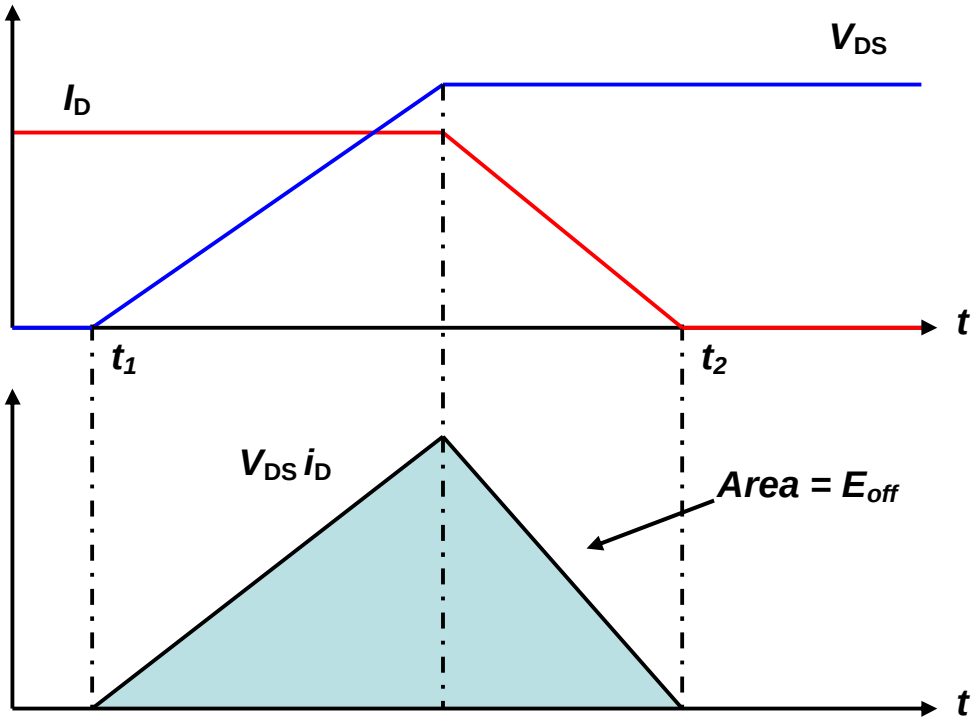

Figure 1.4 – Simplified MOSFET turn-off transition waveform

Due to the overlap of V_{DS} and I_D, power is lost during MOSFET state transition. The power loss can be estimated by finding the area underneath the intersection of the V_{DS} and I_D waveforms and multiplying by the frequency. The equations below can be used to estimate the power loss.

$$E_{on} = \frac{1}{2} V_{DS}\, I_D \left(t_2 - t_1\right) \quad \text{(Eq. 1.1)}$$

$$E_{off} = \frac{1}{2} V_{DS}\, I_D \left(t_4 - t_3\right) \quad \text{(Eq. 1.2)}$$

$$P_{loss-sw} = \left(E_{on} + E_{off}\right) f_s \quad \text{(Eq. 1.3)}$$

The equations above are a crude estimation due to several factors. First, the equations do not find the true area underneath the curve. The true V_{DS} and I_D waveforms are not perfectly linear with rigid transitions. Second, the V_{DS} and I_D may suffer from distortion due to parasitics, noise, etc.

1.2.3 Other Losses and Parasitics

As mentioned previously, parasitic losses may encompass a number of different losses. These losses can be particularly difficult to estimate and calculate.

A common source of parasitic loss is parasitic capacitance and parasitic inductance. Parasitic capacitance and inductance can create ringing and spikes on waveforms. The ringing and spikes can create additional losses. For example, switching loss was discussed above. During MOSFET transition, parasitic inductance and capacitance can create ringing on the V_{DS} and I_D waveforms. The ringing increases the area underneath the intersection of the V_{DS} and I_D waveforms.

Parasitic inductance and capacitance can pose a danger for the system as well. The voltage and current spikes induced by the parasitics can damage or kill devices. For example, for an inductor, the voltage can be calculated as follows.

$$V = L \frac{di}{dt} \qquad \text{(Eq. 1.4)}$$

Typically, the parasitic inductance is very small but the di/dt value can be quite large. In a high current system, the change in current is large. The change in time can also be very small due to the fast switching nature of MOSFETs. Therefore, the di/dt value can be very large due to the large current and small time period. This creates a very large voltage spike despite the small inductance. The voltage spike can also decrease system efficiency indirectly. In order to protect the devices, snubbers or Transient Voltage Suppressors (TVSs) may be used to clamp the voltage. Unfortunately, snubbers and TVS devices consume power. Also, the voltage rating of the MOSFET may have to be increased to provide a safe margin to sure that it can survive the transient voltage spikes caused by the parasitic inductance. This typically means increasing the MOSFET $R_{DS\text{-}ON,}$ which leads to reduced system efficiency.

Similarly, parasitic capacitance can cause a large current spike due to its current characteristic.

$$I = C \frac{dv}{dt} \qquad \text{(Eq. 1.5)}$$

Parasitic capacitances can also cause current spikes due to inrush current. When the capacitor has no charge and a voltage is applied across it, a large current flows to the capacitor to charge it. This condition may also create a substantial current spike.

Another source of parasitic loss is copper conduction loss. Ideally, copper would have no resistance and there would be no power lost no matter how much current was flowing. Unfortunately, copper does have a very small resistance. The power lost can be calculated by the simple equation below.

$$P_{cu} = I_{rms}^{2} R \qquad \text{(Eq. 1.6)}$$

Under low current conditions, the current is small and the resistance is very small. Therefore, copper loss is typically considered trivial. For high current conditions, even though the resistance is very small, the current is very large. Therefore, it is possible for copper conduction losses to contribute a substantial amount of loss. The resistance of copper will increase as temperature increases. Systems which are subject to heat or have thermal issues, will suffer copper losses.

Most high current systems employ a bus bar to carry large amounts of current. The main purpose of the bus bar is to provide enough copper for current flow. In addition, the bus bar can serve as a heat sink. If the bus bar is connected directly to a device pin, heat may be dissipated from the device to the bus bar. This is advantageous since reducing the temperature of a MOSFET can reduce the $R_{DS\text{-}ON}$.

Dc-dc converters must use magnetic components for various purposes including waveform filtering and electrical isolation. Magnetics can contribute losses to the system in the form of core loss and copper loss. Typically, reduction of core loss leads to an increase in copper loss and vice versa. Therefore, careful magnetic design optimization is important in order to reduce losses.

Core loss occurs because energy is not completely recoverable when changing the magnetization of a core material. Core loss for transformers is determined by the applied voltage-seconds. The core loss is not dependant on the current through the transformer. If the input voltage condition remains the same, the core loss will remain constant regardless of load current. Therefore, minimizing core loss is important for low power efficiency. Under many applications, core loss may account for a relatively large percentage of loss for a system under light load. When a system is under high load, other

losses such as conduction and switching losses will dominate instead. The core loss of a material can be estimated by the following equation.

$$P_{fe} = K_{fe} (\Delta B)^{\beta} A_e \ell_m \quad \text{(Eq. 1.7)}$$

K_{fe} = Constant of proportionality

ΔB = Peak ac flux density

β = Core property

A_e = Effective core area

ℓ_m = Effective core length

While this equation may be used to find the core loss, finding the coefficients K_{fe} and ß can be difficult. Some manufactures may provide the coefficients but often times, they may not be available. Therefore, calculating the core loss based on the equation can be very cumbersome.

Instead, the preferred method for determining the core loss is by using manufacture datasheets. Manufactures typically provide a plot of specific power loss as a function of peak flux density. The specific power loss is provided in terms of watt per volume. Peak flux density can easily be calculated for dc-dc converters. Using the plot, the core loss can easily be calculated based on basic values such as peak flux density, turns ratio, core volume, switching frequency, etc.

In addition to core loss, magnetic components have copper losses. There are three types of copper losses. The first type is simple low frequency copper loss. Low frequency copper loss is caused by the inherent resistance within copper. Typically copper is considered a lossless conductor, but that assumption is not applicable for high current systems. The low frequency copper loss can be calculated with the same method as mentioned above.

The next type of copper loss is due to skin effect. At high frequencies, current tends to flow on the surface of a conductor and not in the center of the conductor. Since the center of the conductor is not utilized, the effective copper area is reduced and resistance of the conductor increases at high frequencies. The skin depth or penetration depth is the depth from the surface of a conductor through which current will flow. The penetration depth can be calculated with the equation below and is primarily based on the

switching frequency. The higher the switching frequency employed, the lower the penetration depth.

$$\delta = \sqrt{\frac{\rho}{\pi \cdot \mu \cdot f}} \qquad \text{(Eq. 1.8)}$$

The final type of copper loss is due to proximity effects. The current flowing through a conductor will generate a flux. If two conductors are within close proximity, the flux can penetrate the second conductor. The flux induces a current to be produced that opposes the flow of current. Therefore, the effective current within the copper is increased and copper loses tend to increase. Primary and secondary windings may be interleaved in order to reduce losses due to proximity effects.

In addition to the above mentioned losses, several other sources of losses exist. Diode reverse recovery issues can cause significant losses if diode performance is poor. Diode reverse recovery occurs when the diode makes a sudden transition from an on state to an off state. The diode reverse recovery can cause substantial voltage ripple and noise. Not only does the voltage ripple cause extra loss, the voltage ripple, which can resemble a reverse going voltage spike, can kill or damage devices if the spike has sufficiently large amplitude or is of sufficient duration. Other switching components can create additional voltage ripples and spikes within the system. Noise is also generated from high frequency switching, which can create problems. Unfortunately, many of these losses are very difficult to estimate and characterize.

1.3 Packaging, Layout, and Other Mechanical Issues

Mechanical issues such as packaging and layout can have significant effects within the system. Packaging clearly affects the system when one considers its impact on air circulation over the circuitry. Fan placement, package size, and air flow obstruction, all affect thermal factors of the system. Temperature greatly affects the performance of some components such as MOSFETs, diodes, transformers, etc. Depending on the device package, cooling solutions may differ. Through-hole components are typically designed to easily be mounted to heat sinks. Surface mount components are typically designed to dissipate heat into the PCB. As discussed later, clad boards can be utilized to cool surface mount devices.

Layout also greatly affects the system. First, the layout is crucial as poor design can lead to significant parasitic capacitance and inductance. Long traces within a board can cause excessive ringing due to parasitic inductances. The ringing caused by parasitics can kill devices due to over voltage or create additional losses. For example, switching waveforms distorted by parasitic inductances and capacitances will have additional losses.

In addition, for high current applications, copper losses can become significant. The resistivity of a trace is dependant on the cross-sectional area and the length. Therefore, reducing trace length becomes particularly critical. Typically bus bars are used for high current paths. Attaching the bus bar to the PCB or devices can be non-trivial. Therefore, the two need to be considered together when being designed.

1.4 Isolated Low-Voltage High-Current Converter Considerations

The first system that will be considered is a 5kW dc-dc converter for distributed generation applications. Dc-dc converters for fuel cell distributed generation applications must handle low-voltage high-current input and should have very high efficiency for reliability and cost reduction. The nominal output condition of the fuel cell may be considered to be approximately 50V and 100A. When selecting a dc-dc converter topology for distributed generation applications, a number of factors are important to consider. First, electrical isolation is required. Therefore, the topology must include transformer isolation. As mentioned previously, it is possible for systems to obtain electrical isolation through line frequency transformers; however, this option is highly undesirable. If a line frequency transformer were to be utilized, a non-isolated converter topology may be selected.

Next, the system must be capable of high conversion ratios. A boost converter based topology may be used or high conversion ratio may be achieved by transformer. A boost converter based topology allows for a wider input voltage range. A buck converter based topology must rely on transformer turns ratio in order to obtain high conversion ratio. Relying on transformer turns ratio for high conversion ratio has a number of disadvantages. First, the maximum output voltage is strictly limited by the input voltage and the transformer turns ratio. If the source voltage drops due to high power loads, the buck converter based topology cannot properly compensate for the voltage drop. In addition, if a high turns ratio is utilized, the leakage inductance of the transformer may be excessively high. The leakage inductance may cause additional parasitic losses in the system.

Although this sounds redundant, a low-voltage high-current system must be capable of handling high currents. For example, to achieve 5kW output power level, the input current must be greater than 100A if a 50V nominal input fuel cell is utilized.

Finally, high efficiency is critical for energy applications. High efficiency can translate into better system reliability as well as cost reduction in energy related applications. High efficiency means there is less heat produced. Less heat results in lower

component temperatures, which increases component and system reliability. High efficiency also may translate into various cost savings. With higher efficiency, the system requires less thermal management which can be a significant part of system cost. Some sources, such as fuel cells, have costs associated with operation. Therefore, higher efficiency can result in reduced costs for operation.

1.5 Single-Phase Isolated Low-Voltage High-Current Dc-Dc Converter Topologies

Selecting the proper dc-dc converter topology is critical in order to obtain high efficiency and high reliability for a system. Some topologies are better suited for certain applications. A number of converter topologies could potentially be utilized for distributed generation applications. Topologies based on the push-pull, half-bridge, and full-bridge converters are possible. All the mentioned topologies have isolation and are capable of high conversion ratio, but each has advantages and disadvantages.

The push-pull converter is undesirable due to the center-tap primary configuration and high primary side device voltage stress. The push-pull converter only has one device in the primary conduction path but this advantage is negated due to the high voltage stress applied to the device. The high voltage stress requires the use of a higher drain-to-source breakdown device, which requires that the device have a high $R_{DS\text{-}ON.}$ In addition, the transformer may be likely to saturate due to the center tap configuration. The push-pull converter topology is shown in the figure below.

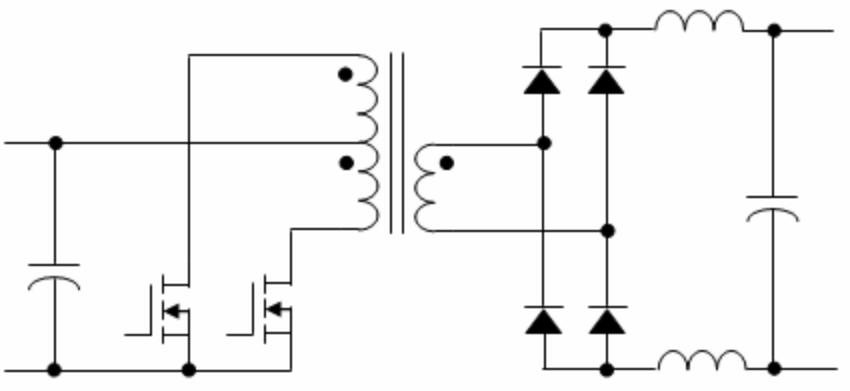

Figure 1.5 – Push-pull converter topology

The half-bridge converter topology is undesirable for step-up applications as only half the input voltage is utilized. Consequently, the current stress of the devices is doubled. The half-bridge converter topology is much more advantageous for step-down applications where the utilization of half of the input voltage is not detrimental. The half-bridge converter topology is shown below.

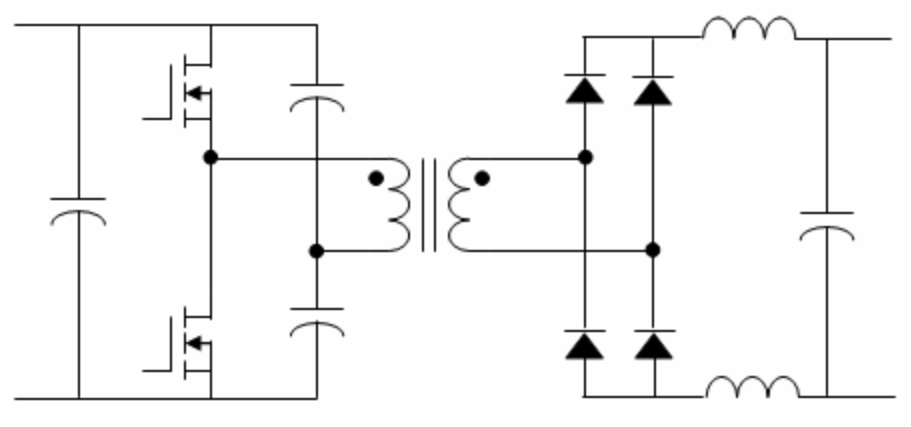

Figure 1.6 – Half-bridge converter topology

The full-bridge converter has several advantages compared to the topologies mentioned above. First, the full input voltage range is utilized without additional voltage stress. Therefore, the current stress of the individual devices is not as high as that in a half-bridge converter. In addition, the full-bridge converter is able to utilize various control schemes such as frequency modulation and phase-shift modulation in order to achieve soft switching conditions. Full-bridge converter topology variations are also possible in order to improve upon its shortcomings. While the full-bridge topology has several advantages, device count, system complexity, control complexity, and other factors can all be significant disadvantages.

The full-bridge converter is desirable in low-voltage high-current applications due to its flexibility and ability to utilize low voltage devices without increasing current stress. The full-bridge converter may be utilized as a buck based topology or a boost based topology. The basic configuration of the full-bridge converter is shown below.

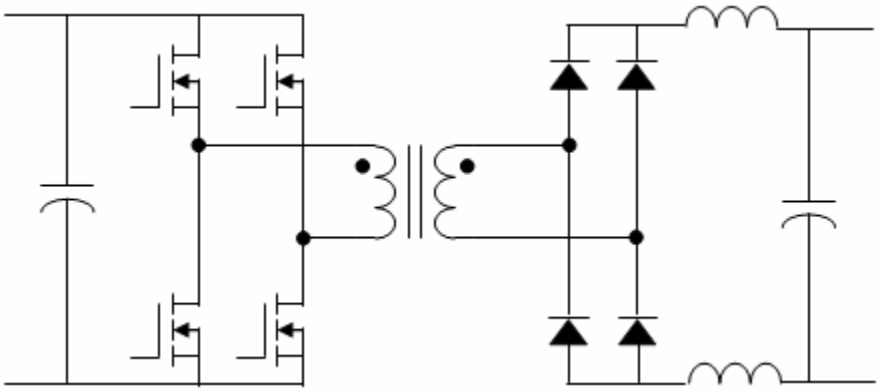

Figure 1.7 – Full-bridge converter topology

1.5.1 Voltage Fed Full-Bridge Converter

The figure below shows the basic topology of the voltage source full-bridge converter. The converter typically requires clamping on the secondary side. Higher blocking voltage diodes may be selected in order to avoid the snubber but the forward voltage drop will increase. A carefully designed snubber should be able to properly protect the rectifier diodes without producing excessive amounts of loss. The circuit below shows the rectifier with a resistor, capacitor, and diode (RCD) snubber for ripple clamping and device protection.

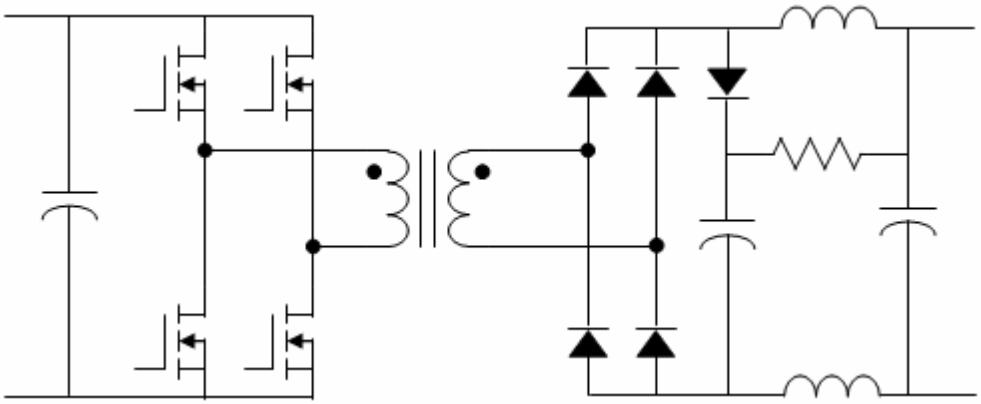

Figure 1.8 – Voltage fed full-bridge converter topology with rectifier snubber

The voltage fed full-bridge converter is a buck converter based topology. This means that the converter relies on the transformer turns ratio if high conversion ratio is desired. The converter is not capable of supplying an output voltage greater than the input voltage times the transformer turns ratio. As mentioned previously, if heavy load causes the source voltage to drop, the converter will not be able to compensate effectively. If lower output voltage is desired, the voltage fed full-bridge converter is able to properly regulate the output.

No clamping circuitry is required on the primary side as shown above. The voltage stress seen by the primary side MOSFETs is effectively the input voltage. Therefore, low voltage rating MOSFETs may be utilized, which are desirable for low-voltage high-current systems due to their lower $R_{DS\text{-}ON}$. Since the dc-dc converter will see high input currents, low $R_{DS\text{-}ON}$ is crucial for the primary side. As mentioned previously,

a snubber circuit may be used to clamp the secondary side voltage and protect the output diodes. Therefore, the diode blocking voltage does not have to be excessively high.

The voltage fed full-bridge converter may achieve soft switching conditions with phase shift modulation. Unfortunately, soft switching conditions may be limited in range for the leading leg. Large leakage inductance may be used in order to obtain soft switching over a wider range, but the leakage inductance may create a loss of duty cycle.

1.5.2 Current Fed Full-Bridge Converter

The current fed full-bridge converter is a boost converter based topology. The circuit topology is shown in the figure below. The converter is shown with an active clamp circuit on the primary side.

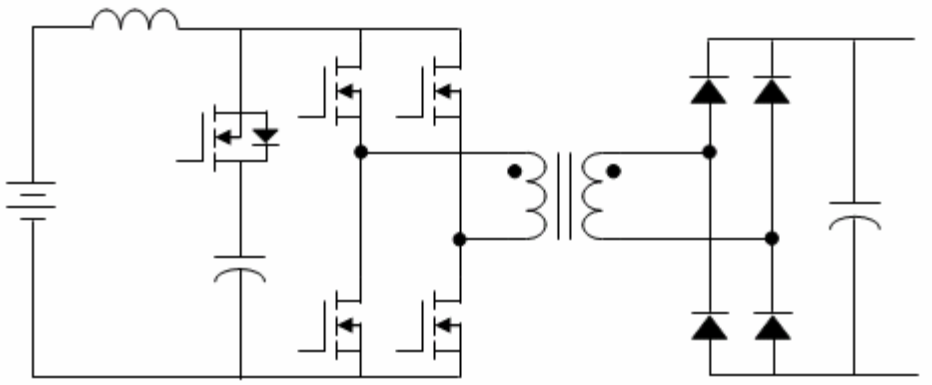

Figure 1.9 – Current fed full-bridge converter topology with active clamp

The current fed full-bridge converter is able to easily achieve high conversion ratio due to its relation to the boost converter topology. In addition, transformer turns may be utilized to provide even greater conversion ratio. The current fed full-bridge converter is capable accepting a very wide range of input voltages due to its ability to adjust conversion ratio beyond the input voltage times the transformer turns ratio. Therefore, even at high load conditions where source voltage may drop, the current fed full-bridge converter will be capable of maintaining a constant output. If lower output voltage is desired, the current fed full-bridge converter must obtain it through transformer turns ratio.

As mentioned previously, for low-voltage high-current systems, low voltage MOSFETs are critical in order to reduce conduction loss. If severe ripple is experienced on the primary side, higher voltage rating devices must be utilized instead. The higher voltage devices will contribute more conduction loss due to their higher $R_{DS\text{-}ON}$. Therefore, an active clamp is required to reduce ringing for the primary side MOSFETs. Despite the use of an active clamp, the voltage ringing on the primary side cannot be damped completely.

Due to the active clamp circuitry, there may be circulating energy with in the primary side [1]. The circulating current may be limited at the cost of loss of Zero Voltage Switching (ZVS) and ringing across the devices.

Timing of the active clamp switch adds complexity to control. If proper control and conditions are achieved, ZVS turn-on may be achieved for all devices. In addition, ZCS turn-off may be achieved for the bottom switches. Unfortunately, the top switches turn off at hard switching conditions. Therefore, snubbers may be required for the upper switches [1].

1.5.3 Analysis of Single-Phase Full-Bridge Converter Topologies

As mentioned previously, the full-bridge converter topology is desirable among the various high power converter topologies. The sections above have discussed two major categories of full-bridge converter topologies. Each converter type has its advantages and disadvantages. In the end, the voltage fed full-bridge converter topology is desirable. The conduction losses for low-voltage high-current systems are expected to be dominant. Therefore, low voltage MOSFETs are crucial in order to obtain high efficiency.

In order to further reduce conduction losses, the effective primary side conduction path resistance should be reduced. Three methods are possible in order to reduce conduction losses. The first method is to simply use lower $R_{DS\text{-}ON}$ devices. Using better devices is desirable as the solution is very simple. Unfortunately, beyond a certain point, lower $R_{DS\text{-}ON}$ devices may become difficult to find or very expensive as they may only exist as modules.

Another option is to simply parallel several MOSFETs. Therefore, the equivalent $R_{DS\text{-}ON}$ may be reduced. MOSFETs have a positive temperature coefficient which allows for parallel operation. Suppose two MOSFET devices are in parallel. Due to manufacturing tolerances, one device has a slightly lower $R_{DS\text{-}ON}$ compared to the other. Once current flows, the device with lower $R_{DS\text{-}ON}$ will carry more current due to lower resistance. The MOSFET with lower $R_{DS\text{-}ON}$ will begin to heat up more due to the greater current. The increase in junction temperature will cause the lower $R_{DS\text{-}ON}$ MOSFET to increase its $R_{DS\text{-}ON}$. If the $R_{DS\text{-}ON}$ increases, the current will be diverted to the other switch. Many situations can occur where device temperature or resistances are not equal. Therefore, positive temperature coefficient is critical for safe current sharing between paralleled devices. Devices such as diodes with negative temperature coefficients cannot safely be paralleled. For high-power applications, however, the interconnect parasitic resistances and inductances between paralleled devices tend to create noticeable losses and noises due to circulating current between devices.

The last option is to utilize multiple phases instead of parallel devices to avoid circulating currents. Multiple phases provide the same primary benefit as parallel devices.

The current is shared between multiple phases and therefore, the conduction loss per device is decreased. In addition, multiple phases provide a number of advantages over a single phase as discussed in the next section. Multiple phases may be used in conjunction with parallel devices to further drive conduction losses down.

1.6 Multiphase Isolated Low-Voltage High-Current Dc-Dc Converter Topologies

A multiphase topology has a number of advantages. The multiple phases share the currents within the system. Therefore, from a conduction loss are reduced since the RMS current through a single device is reduced. In addition, the effective frequency of the system is increased which allows for reduction in passive components such as inductors and capacitors. Passive components are typically the largest and most expensive components within a system. Therefore, reduction in passive component requirements is highly desirable. If a three phase topology is utilized, three phase transformer topologies such as Δ-Δ, Δ-Y, Y-Δ, and Y-Y may be utilized. The three phase transformer configurations may be used in order to increase or decrease the conversion ratio without additional turns. Since no additional turns are necessary, the leakage inductance may be reduced and duty cycle loss may in turn be reduced. Finally, with a multiphase topology, coupled transformer configurations are possible. Coupled transformers would be able to reduce the overall transformer size. The primary disadvantage with a multiphase topology is the complexity of control. Additional control circuitry is required in order to realize multiphase operation.

In order to obtain high efficiency, a multiphase converter should be utilized. The multiphase topology is desirable over paralleling several devices. Utilizing multiple phases addresses the key issues for distributed generation application converters. Higher current handling as well as higher efficiency is possible with multiple phases. In addition, with a three phase transformer configuration, the conversion ratio may be increased or decreased without additional turns.

A number of multiphase high power dc-dc converter topologies exist [2]-[10]. Two in particular, found in [13] and [14] are suitable for low-voltage high-current step-up applications.

1.6.1 Three-Phase Asymmetrical Pulse Width Modulation Half-Bridge Converter with Y-Y Transformer

Based on the previous analysis, a three-phase asymmetrical pulse width modulation half-bridge converter with Y-Y transformer is possible, as proposed by Oliveira in [13], for fuel cell distributed generation applications. The figure below shows the circuit topology.

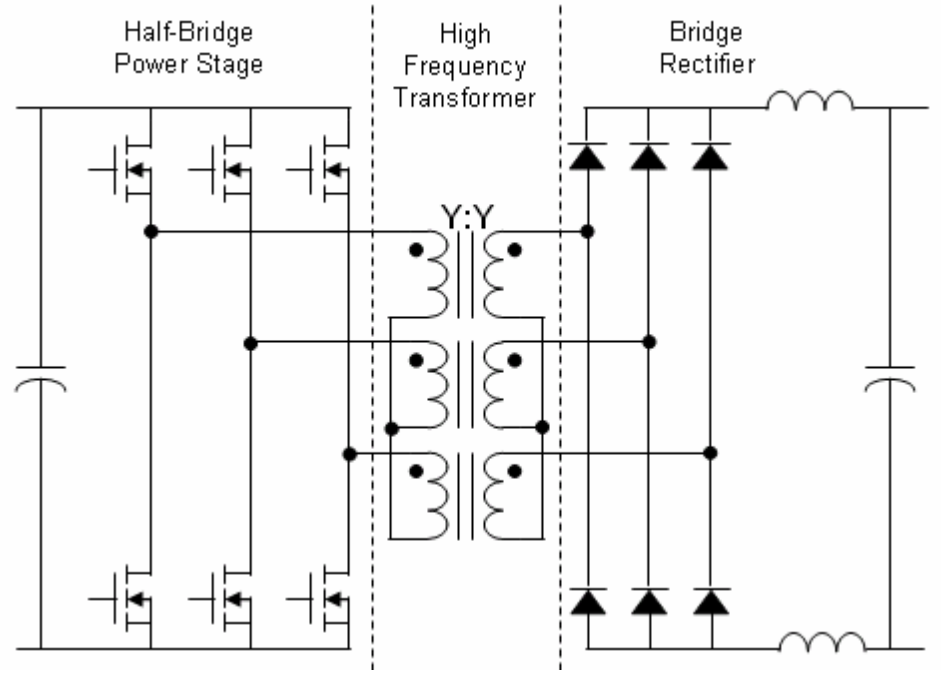

Figure 1.10 – Three-phase half-bridge converter with Y-Y transformer and bridge rectifier

The three-phase half-bridge converter is able to utilize the full input voltage. In addition, there is no need for split dc capacitor. The split dc capacitors from the single-phase half-bridge converter must be capable of handling very high levels of current. Therefore, eliminating the need for the split dc capacitor is desirable.

The asymmetrical pulse with modulation scheme allows for soft switching to be achieved. The soft switching mechanism is very similar to the soft switching for the phase-shift modulation full-bridge converter. Therefore, both converters may reduce switching losses. Unfortunately, even when selecting low R_{DS-ON} devices such as the IXYS FMM150-0075 with 3.2mO R_{DS-ON}, the current handling capability may not be enough. The multiphase structure helps distribute the current between many devices but

losses are still significant. In order to have a safe level of conduction losses, parallel devices may be required in addition to multiple phases. Paralleling devices can cause some additional problems when dealing with through-hole devices such as the FMM150-0075. Due to the nature of the package, paralleling devices can introduce significant amounts of parasitics such as resistance and inductance. If 12 devices are to be utilized, the full-bridge configuration is more desirable in order to avoid parallel device configurations.

1.6.2 Three-Phase Phase-Shift Modulated Full-Bridge Converter with Δ-Y Transformer

Based on the previous analysis, a three-phase phase-shift modulated full-bridge converter with Δ-Y transformer is desirable, as proposed by Liu in [14], for fuel cell distributed generation applications. The topology of the converter is shown below.

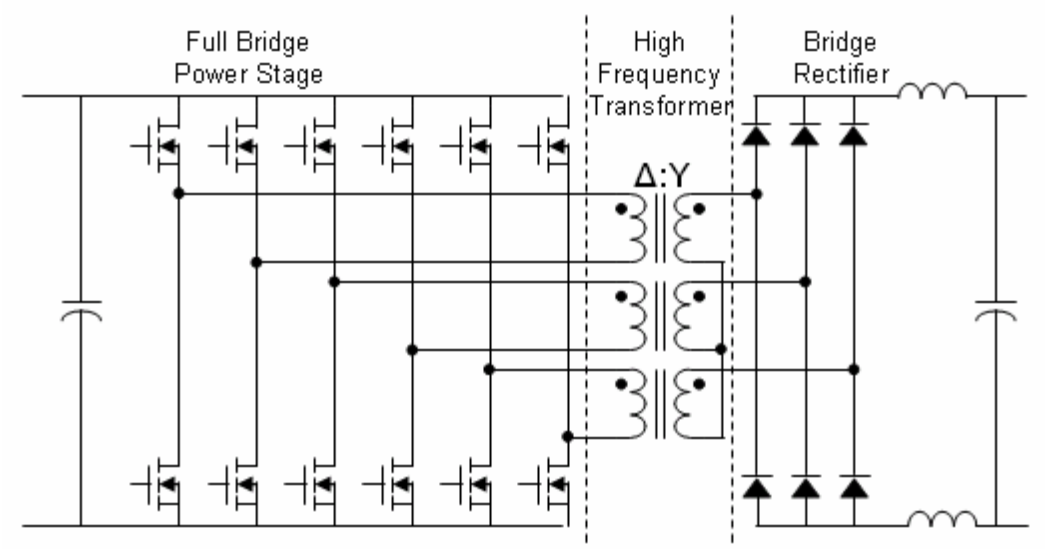

Figure 1.11 – Three-phase full-bridge converter with Δ-Y transformer and bridge rectifier

The topology shown above holds several advantages for low-voltage high-current systems where voltage step-up is required. As mentioned previously, the multiphase nature allows current to be shared between phases and, therefore, devices. Thus, the conduction loss is decreased, therefore increasing both current handling capability and efficiency. The multiphase nature also increases the effective switching frequency, therefore reducing the size of passive components.

The three-phase topology allows the converter to utilize a Δ-Y transformer configuration. The Δ-Y transformer configuration doubles the conversion ratio without any increase in turns ratio. Increasing the turns ratio creates excessive leakage inductance which leads to parasitic losses such as duty cycle reduction.

While conduction loss may be dominant in low-voltage high-current systems, switching losses may still be very significant. Therefore, the soft switching conditions

achieved by the topology shown above are very beneficial. The soft switching conditions reduce switching loss, thereby increasing current handling capability and efficiency.

The three-phase phase-shift modulated full-bridge converter with Δ-Y transformer and full bridge rectifier will be referred to the V6 converter for simplicity. Further details regarding the V6 converter are discussed in the later sections.

1.7 Thesis Outline and Major Results

The first chapter introduces some applications for low-voltage high-current power systems. In addition, typical sources of loss for low-voltage high-current systems are covered. Standard sources of loss such as conduction loss and switching loss are important. Other sources of loss in the form or parasitics are also important to consider. Low-voltage high-current systems will suffer greatly from current dependant parasitics such as contact and termination, capacitor ESR, copper loss, etc. Some converter topologies for low-voltage high-current systems are surveyed.

In the second chapter, a 50V, 100A, 5kW three-phase full-bridge dc-dc converter design is analyzed. The converter is called the V6 converter. The V6 converter takes low voltage high current input and boosts the voltage to approximately 400V. Basic operation of the V6 converter is discussed. Characteristics and advantages regarding the V6 converter are also presented. Experimental waveforms representing the characteristics of the V6 converter are presented as well.

The third chapter performs loss analysis for the V6 converter. Various sources of loss are considered and calculations are performed in order to model the loss and efficiency for the V6 converter. The calculated loss and efficiencies are compared to experimental results. Initially, the calculation and experimental results do not correspond well. The experimental results indicate a lower efficiency than the calculations due to parasitic losses which are difficult to model and predict. New transformers are designed in order to reduce parasitic losses within the V6 converter. With the new transformers, the parasitic losses, are greatly reduced and the calculated efficiency and experimental efficiency match significantly better. In particular, non-full ZVS condition, skin effect, and contact loss are the most likely sources of parasitic losses.

The fourth chapter discusses considerations for systems requiring even greater current capabilities. A low-voltage high-current three-phase half-bridge converter is considered. The half-bridge converter may see input currents of up to 400A RMS. When dealing with such high currents, various considerations are required. In particular, bus bar design and PCB layout are critical for reducing parasitics. Thermal considerations are also significant. The half-bridge converter utilizes several parallel surface-mount

MOSFETs. MOSFETs allow for parallel operation due to their negative temperature coefficient. Also, a clad board is utilized for improved thermal management.

The fifth chapter provides conclusions for the work presented in this thesis. In addition, directions for future research are provided.

The thesis carefully analyzes a low-voltage high-current power system. Detailed loss analysis is provided for a three-phase full-bridge converter. By analyzing the losses within a converter, the system designer is able to know where improvements are possible and desirable. For low-voltage high-current systems, it is important to consider standard sources of loss such as conduction and switching losses. Also, parasitic losses are critical to the system. Particularly, current or resistance related parasitic losses can create large amounts of loss due to the high current nature of the system. Measures can be taken in order to reduce the parasitic losses in the system. In addition to performance analysis, other concerns are examined as well. Mechanical factors such as PCB layout and bus bar are also critical for low-voltage high-current power stages. Finally, thermal management should be carefully considered. Suitable thermal management is required for safe and reliable operation of the system. Electrical, mechanical, and thermal issues are considered for higher current conditions.

2 V6 CONVERTER OPERATION AND WAVEFORMS

This chapter will discuss the V6 converter as found in [14]-[24] and show some experimental results. As mentioned previously, the V6 takes low-voltage high-current input and produces high-voltage low-current output. The table below shows major specifications of the V6.

Table 2.1 – V6 converter specifications

Nominal Input Voltage	50V
Rated Full Load Input Current	100A
Nominal Output Voltage	400V
Rated Full Load Output Current	12.5A
Transformer Turns Ratio	1:4 (2:4:4)
Rated Full Load Power Output	5000W

The actual transformer used for the V6 converter has two primary turns. There are two secondary windings, each with four turns. Depending on the application, the turns may be placed in series to obtain a 2:8 ratio. For this application, the two secondary windings are placed in series to obtain an effective 1:4 ratio. Different transformer turns may be used to adjust the output voltage to suit various applications.

2.1 Operating Principles of the V6 Converter

The V6 converter is a three-phase, six-leg, phase-shift modulated full bridge converter with Δ-Y transformer. As mentioned previously, it was proposed by Liu in [14]. Detailed information regarding the V6 may be found in references [14]-[24]. The V6 converter is used for voltage boosting applications. The V6 converter takes the low voltage and boosts it to high voltage. While many different topologies are available to boost voltage, the V6 converter was selected in particular due to its high efficiency. As mentioned previously, high efficiency is able to save power as well as improve system reliability with reduced heat. The figure below shows the V6 converter topology.

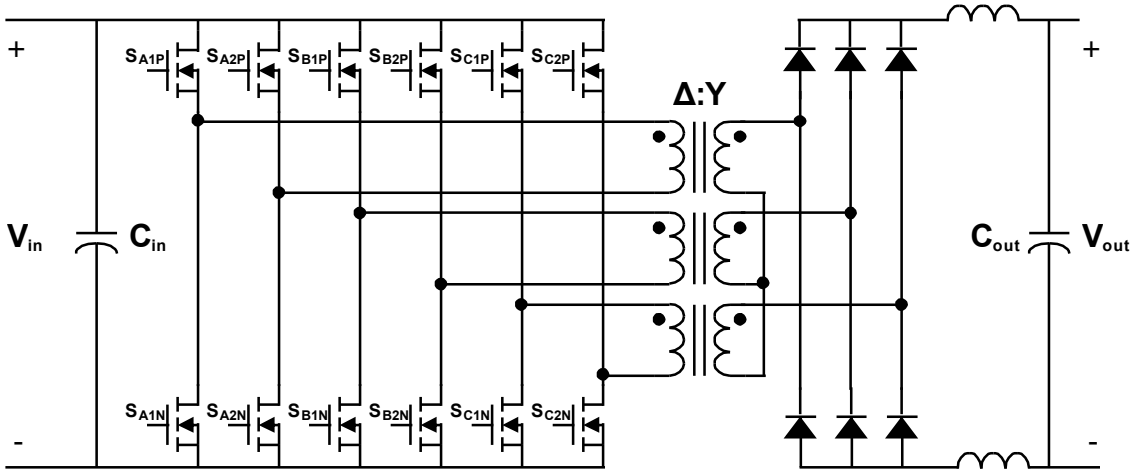

Figure 2.1 – V6 converter: Three-phase full-bridge dc-dc converter with Δ:Y transformer and bridge rectifier

The device naming convention in the figures above and below is as follows. The first letter in the subscript denotes the phase. There are three phases A, B, and C. The next subscript is either 1 or 2. A number of 1 denotes that the device is in the leading leg while a 2 signifies that the device is in the lagging leg. The final subscript letter is either P or N. The P implies that the device is the top device of the phase leg while the N means that the device is the bottom device.

Once again, the V6 converter employs phase-shift modulation (PSM) control. Traditional PWM converters use the duty-cycle to control the output or conversation ratio. Under phase-shift modulation, phase-leg device pairs are switched complementarily

at 50% duty cycle. Phase-shift modulation utilizes the phase-shift, a, to control the output or conversation ratio. The three phase legs in the V6 converter are identical except for a 120° phase shift. The figure below shows the three-phase interleaved phase-shift control for the V6 converter.

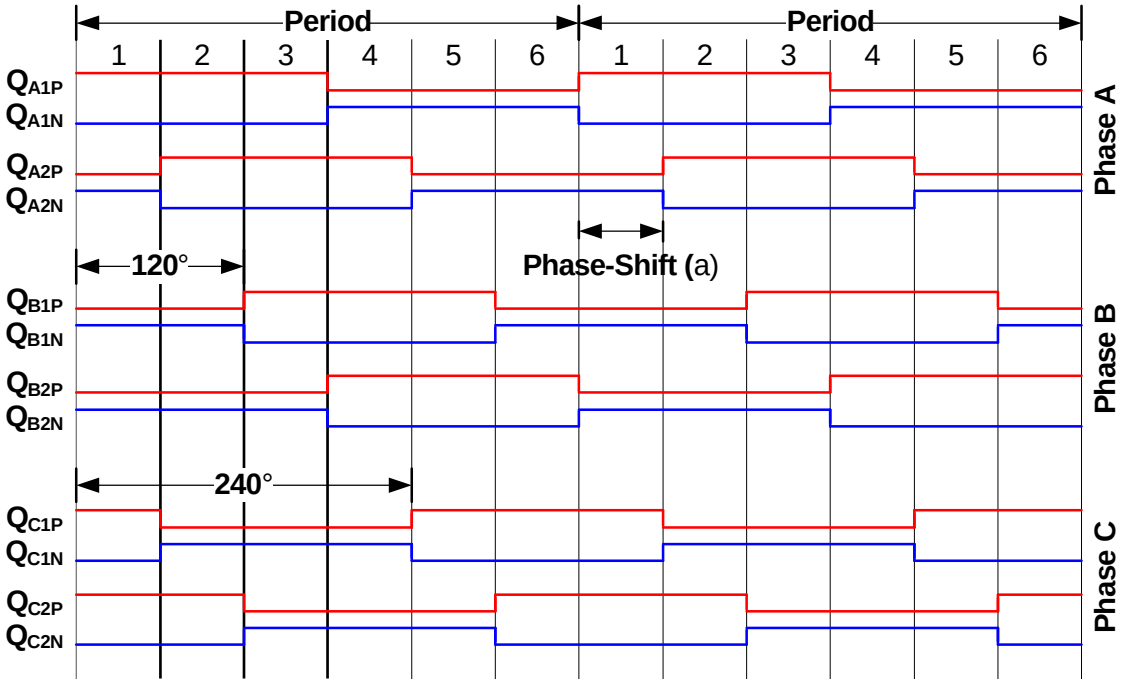

Figure 2.2 – V6 converter control configuration

The phase-shift, a, can range anywhere from 0° to 360°. Due to the nature of the control, a phase shift of 60° is identical to 300°. For standard phase-shift modulated converters, maximum conversion ratio is achieved at 180°. Increasing the phase-shift angle any further reduces the conversion ratio. Due to the V6 converter's topology, the maximum conversion ratio is achieved at 120° and the conversion ratio is constant up to 240°. For control purposes, the maximum phase-shift is limited to 180°. The limit on the phase-shift does not affect operation since phase-shifts exceeding 180° are redundant. The figure below shows the relationship between phase-shift and the conversion ratio.

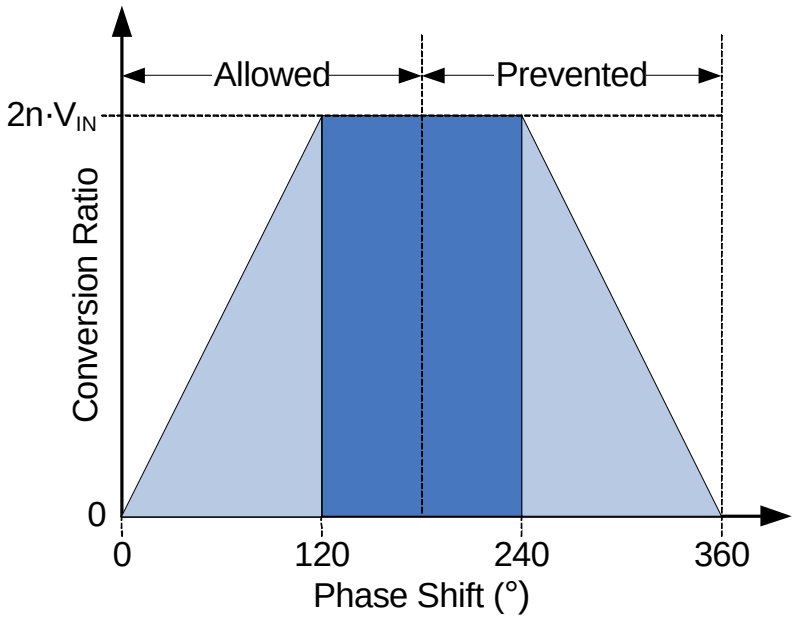

Figure 2.3 – V6 conversion ratio diagram

As the figure above shows, the maximum conversion ratio is $2n \cdot V_{IN}$, where n is the transformer turns ratio. The maximum output voltage is limited due to the fact that the V6 converter is a buck derived model. Therefore, the voltage cannot be boosted without the aid of transformer turns ratio. The figure above also indicates that the conversion ratio is twice the transformer turns ratio. This is due to the Δ-Y transformer configuration. Under sinusoidal conditions, the Δ-Y transformer configuration yields a square-root of three voltage gain. The V6 converter applies square waveforms through the transformer and, therefore, the voltage gain is two instead.

The figure below shows the applied voltage waveform for a single phase at 120° phase-shift. Maximum conversion ratio is achieved under the condition shown below. Increasing the phase-shift will not increase the conversion ratio due to the topology. Increasing the phase-shift will change the applied transformer voltage waveforms but will not have a significant effect on the transformer current waveforms. The lack of change in the current waveforms coincides with the limit in conversion ratio. The voltage waveforms through the transformers are rectified on the secondary by a simple three-phase diode bridge rectifier. At full duty cycle, once the waveforms are rectified, the output voltage and current is effectively flat. Further information regarding this can be found in [14] and [15].

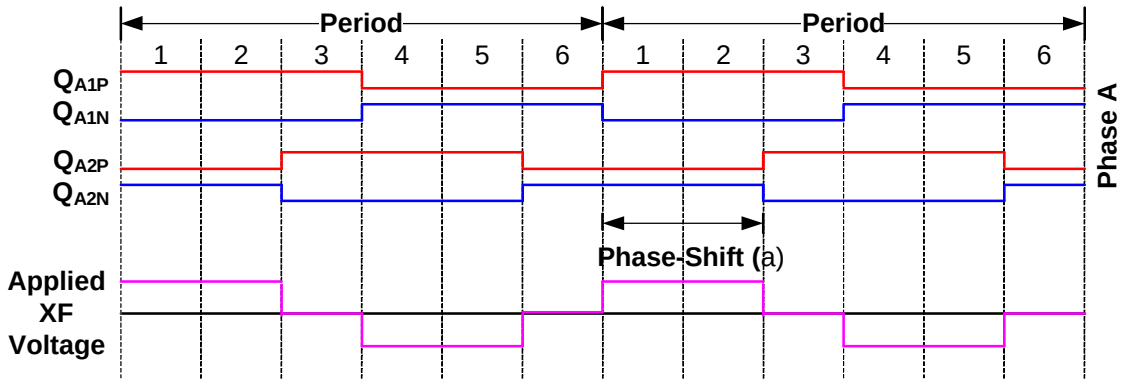

Figure 2.4 – V6 applied transformer voltage waveform for 120° phase shift

The next figure shows the transformer current waveform of three phases. Under full duty cycle, at any given moment, one phase is carrying about half the current in the positive direction while one phase carrying the other half of the current in the negative direction. Once again, the figure is drawn under 120° phase shift condition.

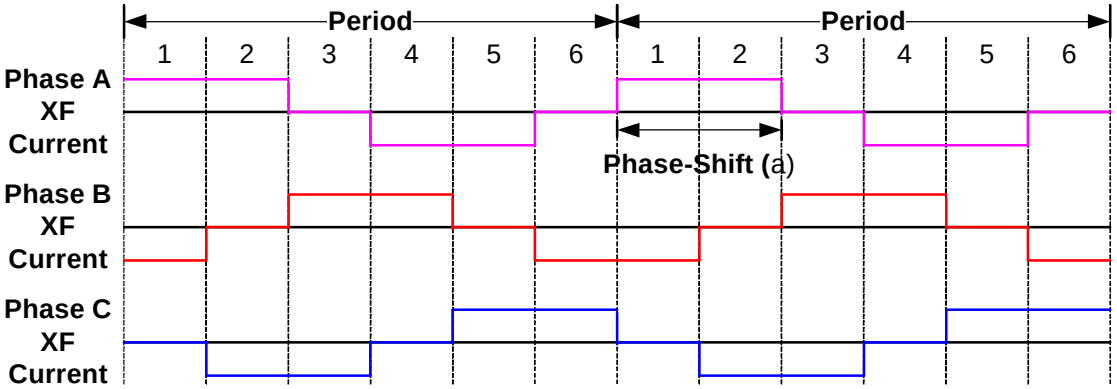

Figure 2.5 – V6 transformer current waveforms for 120° phase shift

2.2 V6 Converter Characteristics and Advantages

The V6 converter has many advantages and is therefore able to achieve high efficiency. Reference [15] indicates efficiencies as high as 97% at 2.5kW power level. In order to achieve such high efficiency, careful design is required. The high efficiency can be attributed to factors that include:

- Low R_{DS-ON} MOSFETs
- Low forward drop diodes
- Soft switching
- Three-phase interleaved topology

2.2.1 Conduction Loss Considerations

In order to obtain high efficiency for low voltage high current systems, conduction loss is a great concern. The V6 converter may see input currents as high as 120A. In order to minimize conduction loss, proper selection of devices is critical. Low R_{DS-ON} MOSFETs are utilized on for the V6 converter for reduced losses. If further reduction of MOSFET conduction loss is desired, several options exist. Some examples are listed below:

- Selection of lower R_{DS-ON} MOSFETs
- Paralleling MOSFETs
- Increase number of interleaved phases

Conduction loss is also a problem for the secondary side as well. Diodes typically have high voltage drops. Although the secondary side current for the V6 is much lower than the primary, the current is still significant. The secondary side current may reach as high as 15A. Utilizing low forward drop diodes help reduce the diode conduction losses.

2.2.2 Switching Loss Considerations

Phase-shift modulation allows the converter to achieve soft switching conditions. When considering efficiency and reliability, soft-switching is very useful. Many converter topologies are available that achieve soft-switching with the use of auxiliary components. The V6 converter is able to achieve soft-switching without any auxiliary components. Switching loss is dependant on both voltage and current. As input power increases, the loss will also increase. Therefore, switching loss can become significant unless soft switching is achieved. Under full conversion ratio, the V6 converter is able to achieve soft switching conditions in all cases except one. The table below shows the soft switching conditions for the V6 converter with 120° – 240° phase shift.

Table 2.2 – V6 soft switching conditions

Condition	Leading Leg	Lagging Leg
Turn On	ZCS	ZVS
Turn Off	ZCS	None

At light load conditions, full ZVS condition may not be achieved. Under light load conditions, the energy in the leakage inductance of the transformer is not enough to discharge the output capacitance of the MOSFET. Therefore, partial ZVS conditions may be achieved. ZCS conditions for the leading leg are maintained throughout all power levels.

With ZCS condition, there is no transition loss due to zero current, but the MOSFET output capacitance is discharged into the MOSFET. When the MOSFET turns on, the output capacitance is effectively shorted, creating a large perturbation. This condition creates significant noise as well as small amounts of power loss, depending on the output capacitance of the MOSFET.

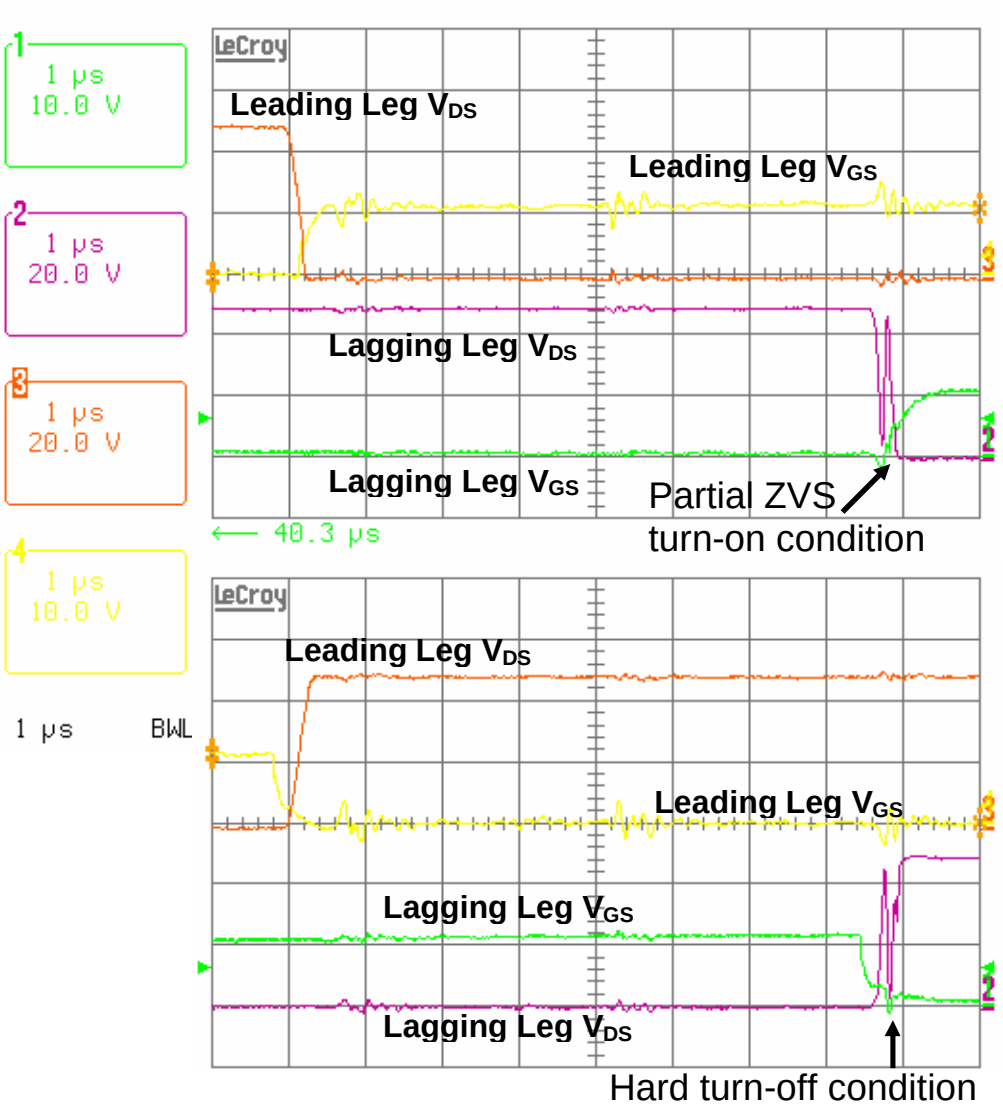

Figure 2.6 – V6 converter partial ZVS condition waveform

The figure above shows the partial ZVS turn-on condition is observed for the lagging leg. The turn-off condition is hard switching for the lagging leg as expected. Once again, the leading leg turn-on and turn-off waveforms do not show any ZVS condition because they only achieve ZCS. The waveforms were captured at 1200W output condition.

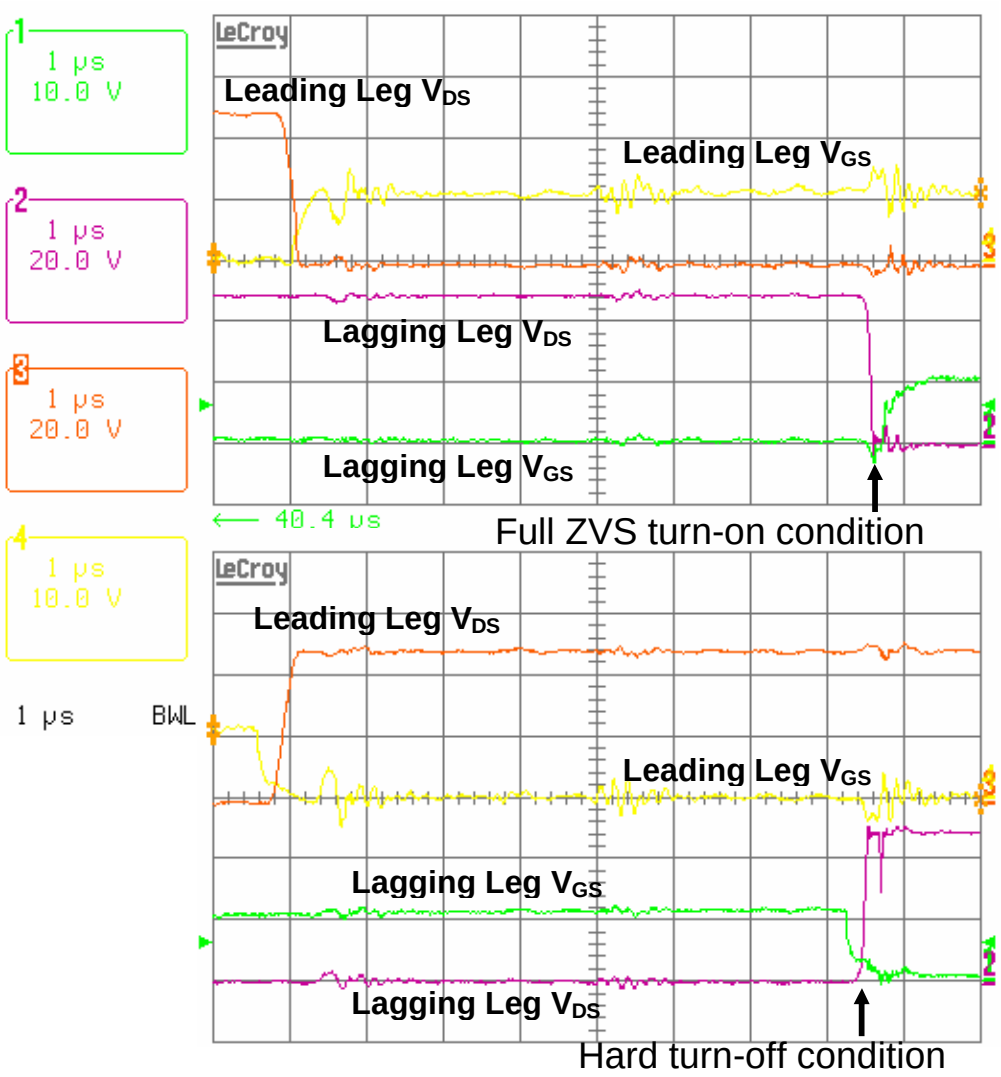

Figure 2.7 – V6 converter full ZVS condition waveform

The figure above shows the full lagging leg ZVS turn-on condition. The waveform was taken at 2.75kW. No ZVS condition is shown on the leading leg as the leading leg only achieves ZCS for both turn-on and turn-off. Lagging leg turn-off is hard switching as shown above.

2.2.3 Three-Phase Interleaved Design

As mentioned previously, the V6 employs a multiphase design, specifically, a three-phase interleaved design. Multiphase converters have additional phases that are paralleled. The control signals of the phases are interleaved with a phase shift. For a three phase interleaved converter, there is a 120° shift between phases. The phase shift is determined by dividing 360° by the number of phases. Multiphase converters have several advantages over single phase converters.

- As a result of the multiple interleaved phases, the effective frequency of the system is increased without increasing actual switching frequency. For the case of the V6 converter, the effective frequency is increased by a factor of six. Therefore, for 50kHz switching, the effective frequency becomes 300kHz. The increase in effective frequency allows for reduction in passive filtering components such as capacitors and inductors. Passive components can add substantial size, weight, and cost to a high power system. Therefore, an increase in effective frequency is highly desirable.
- Higher power rating is also possible with multiphase converters. The current is shared between phases and the RMS current through individual switches can be reduced.
- A Δ-Y transformer configuration is desired due to the increase in voltage output. The three phase interleaved design allows for the Δ-Y transformer configuration to be realized.

The primary disadvantage with multiphase converters is the complexity of design. In order to implement multiphase design, complex control techniques are required. Single phase designs are simple to implement with analog chips. Some multiphase converters with particularly complex control may require digital control in the form of digital signal processors (DSP). Despite the added complexity, the benefits such as reduction of passive components are very attractive.

2.2.4 Other Loss Considerations

Another potential significant source of loss is magnetic loss. Magnetic components should be properly designed in order to reduce loss. The transformers in the V6 can contribute losses in many different forms. Core loss, winding loss, and contact loss could be significant sources of loss for the transformers. Unfortunately, core loss cannot be measured very easily. Therefore, in order to estimate the losses, calculations may be performed as shown in a further section. Winding loss and contact loss are also difficult to measure. The dc-winding loss can be estimated and measured as shown in Chapter 3 but contact loss is not easy to calculate or measure. True winding loss is difficult to measure and calculate due to parasitics such as skin effect and proximity effect. Similarly, true contact loss is difficult to measure and calculate due its dependence on mechanical conditions. Also, temperature can greatly affect the contact resistance as well. Overall, the high current nature of the system means that parasitic resistances are particularly dangerous. The high frequency transformer used by the V6 should be carefully selected in order to avoid excessive losses.

High current systems may significantly strain dc link capacitors. For loss and reliability reasons, high quality capacitors should be utilized. In order to estimate the current stress on the capacitors, simulations were conducted. From simulation, the RMS capacitor current increases fairly linearly based on input current and load current. Unfortunately, the value of the RMS capacitor obtained by simulations is heavily dependent on parasitics such as series resistance, parasitic inductance, etc. If parasitics related to the source are small, the load on the dc link capacitors is reduced. Unfortunately, the test set-up for the V6 utilizes lengthy cables as well as a source-impedance. Therefore, the source parasitics used in our measurements are relatively high. Based on simulation, the dc-link capacitors in the V6 converter must sustain a RMS current approximately 50% -60% of the total input current. The figure below shows a sample simulation waveform. The figure on top shows the RMS input current compared to the RMS capacitor current. The plot on the bottom shows transformer current waveform and capacitor current.

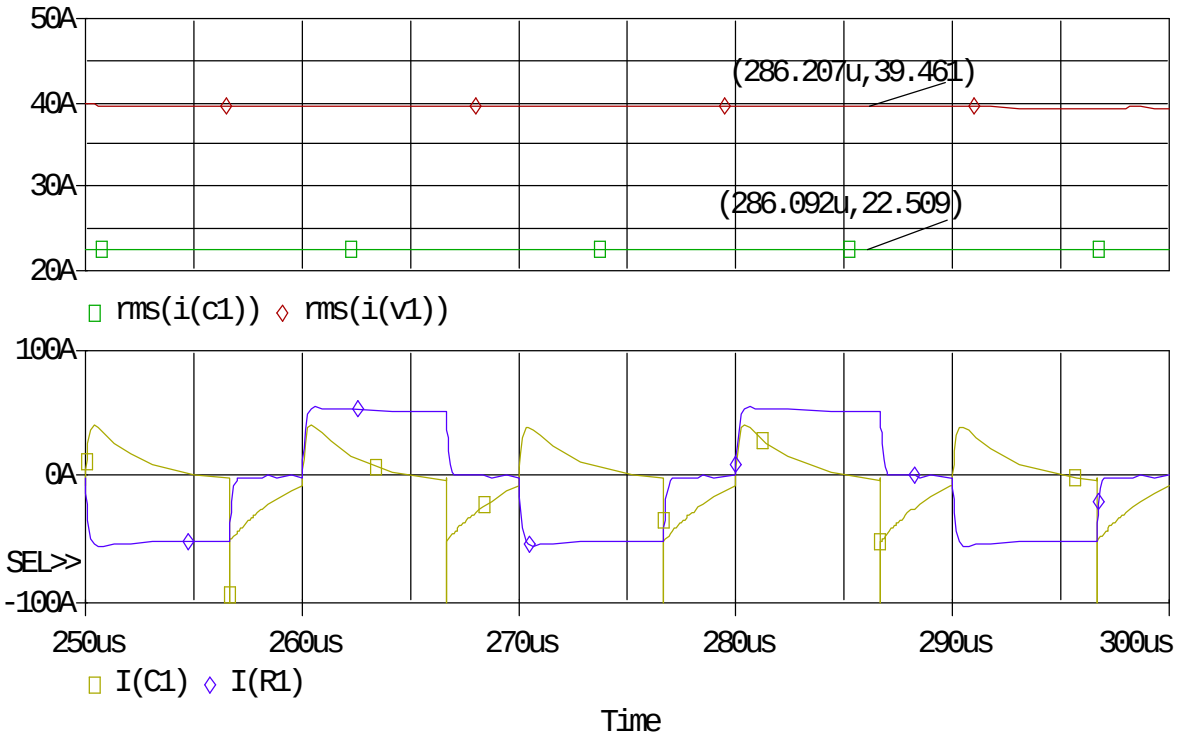

Figure 2.8 – Simulation of capacitor current for V6 converter

In order to minimize losses due to capacitor ESR, the V6 converter utilizes high quality film capacitors across the dc bus. The film capacitors have very low ESR and are capable of high frequency performance. In addition, several capacitors are placed in parallel to reduce the ESR and losses.

Another potential source or loss is the snubber on the rectifier side. The reverse recovery ripple for the rectifier diodes is very severe. The figure below shows the severity of the voltage spikes.

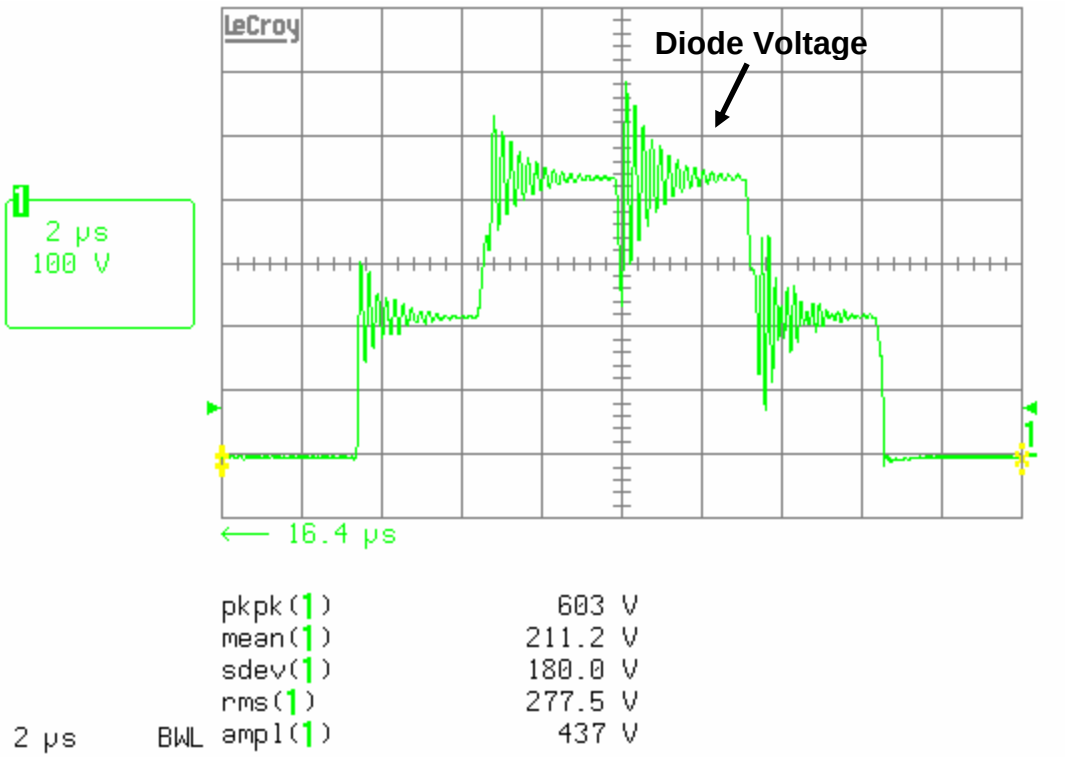

Figure 2.9 – Diode blocking voltage waveform without snubber

The rectifier diodes see extremely high voltage spikes. Higher voltage rating diodes are required or a snubber must be used to damp the voltage ripple seen by the diodes. For this application, lower voltage rating diodes are desired in order to minimize the forward drop. Therefore, a snubber is used to protect the diodes from over voltage. A simple resistor-capacitor-diode (RCD) snubber is used as shown below.

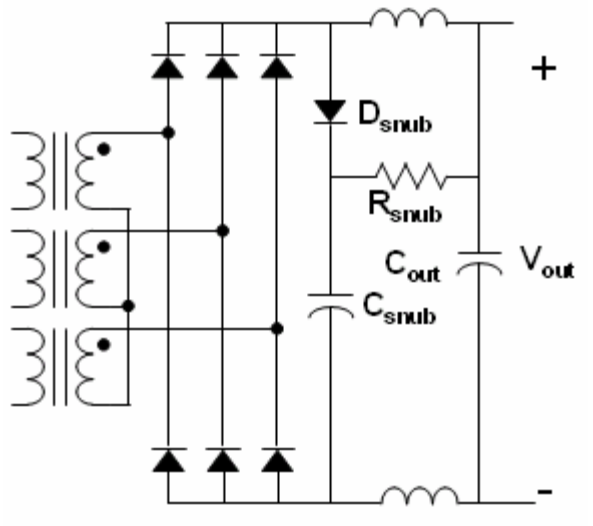

Figure 2.10 – V6 rectifier snubber circuit

Depending on the RC values of the snubber, the snubber can operate as a voltage clamp snubber or rate of rise snubber. For this application, a voltage clamp snubber is desired. The only reason that the snubber is employed is to protect the diodes from over voltage. For the voltage clamp snubber, the RC time constant is much longer and the snubber capacitor maintains a relatively constant voltage.

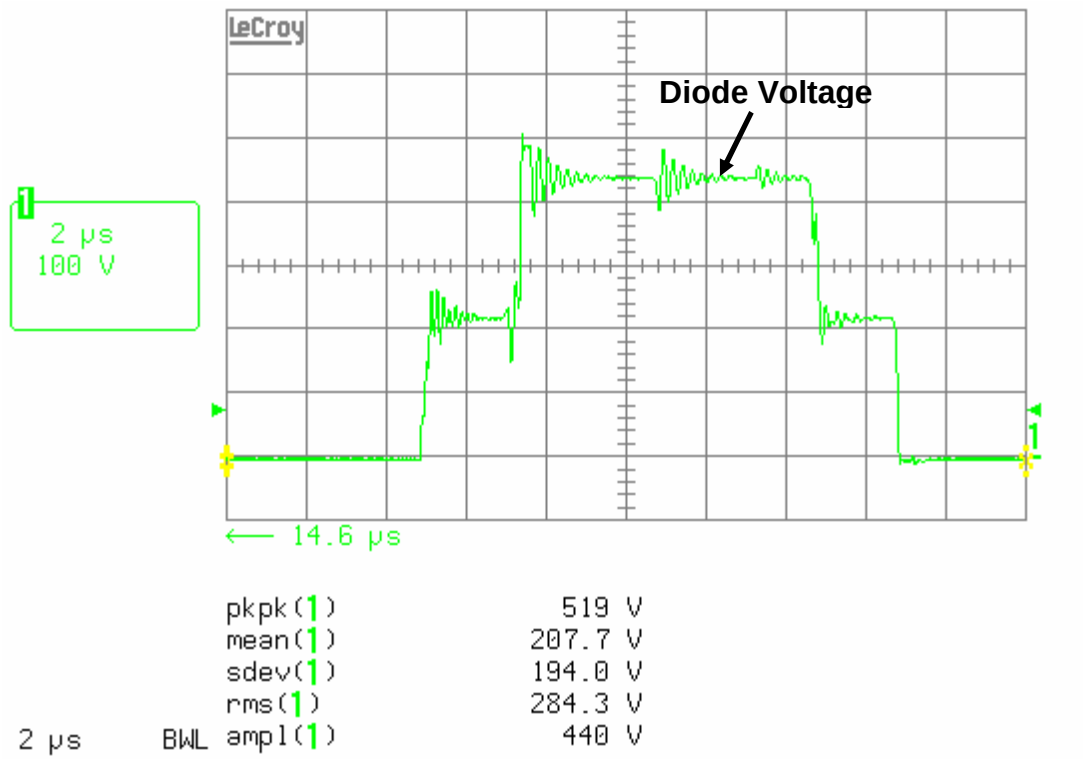

Figure 2.11 – Diode voltage with snubber

The figure above shows that the voltage clamp mode snubber is able to properly clamp the voltage spikes. Depending on the parasitics and snubber design, the snubber loss may be significant. In order to confirm that the loss from the snubber is not too significant, the RMS voltage across the resistor can be measured. The power dissipation of the snubber is effectively the power dissipated by the resistor. The diode and capacitor may have small amounts of loss but it should be relatively trivial. Using the oscilloscope, the RMS voltage across the resistor is easy to measure. The use of a voltage clamp snubber greatly reduces snubber losses. If a rate of rise snubber was used, the power loss would be extremely high due to the high effective switching frequency.

The power dissipation of the snubber is small at lower power and increases with output power level. The snubber loss being to decreases at middle power level instead of continue to increase. At higher power levels, the loss begins to increase again. The increase in snubber loss can be attributed to greater stored energy in the leakage inductance as well as more severe ringing. Therefore, as the power level increases, the snubber loss should increase. The decrease of the snubber loss is caused by the achievement of full ZVS condition. As mentioned previously, the V6 converter may not achieve full ZVS condition at low power levels. Hard switching or partial ZVS conditions can cause unnecessary perturbations to the system, which cause ringing. Once ZVS condition is reached, the perturbations are greatly reduced and, therefore, the required clamping effect is reduced.

The snubber loss is very small compared to other losses. A sample snubber loss measurement at approximately 2.5kW condition is shown below. The measurement below shows more severe ringing due to higher power levels. The diode voltage is still safely clamped below the voltage rating of the diode. The power loss observed in the measurement below is approximately 1W.

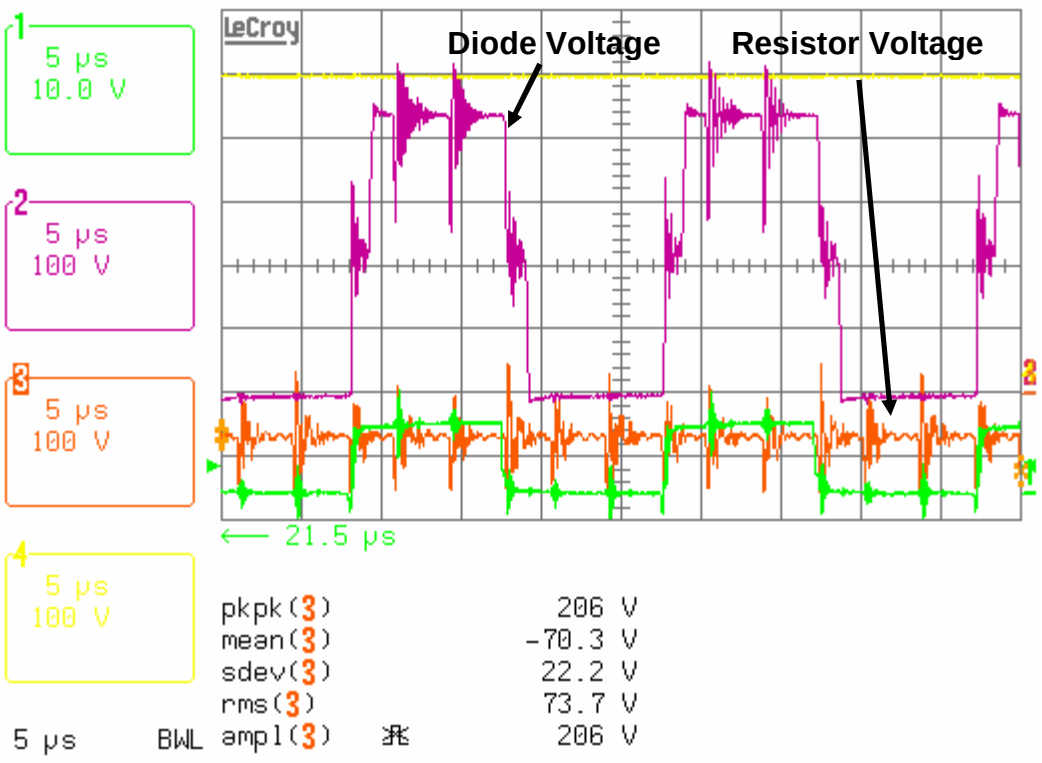

Figure 2.12 – Snubber loss measurement at middle power level.

The following figure shows the diode voltage and resistor voltage waveforms for high power level condition.

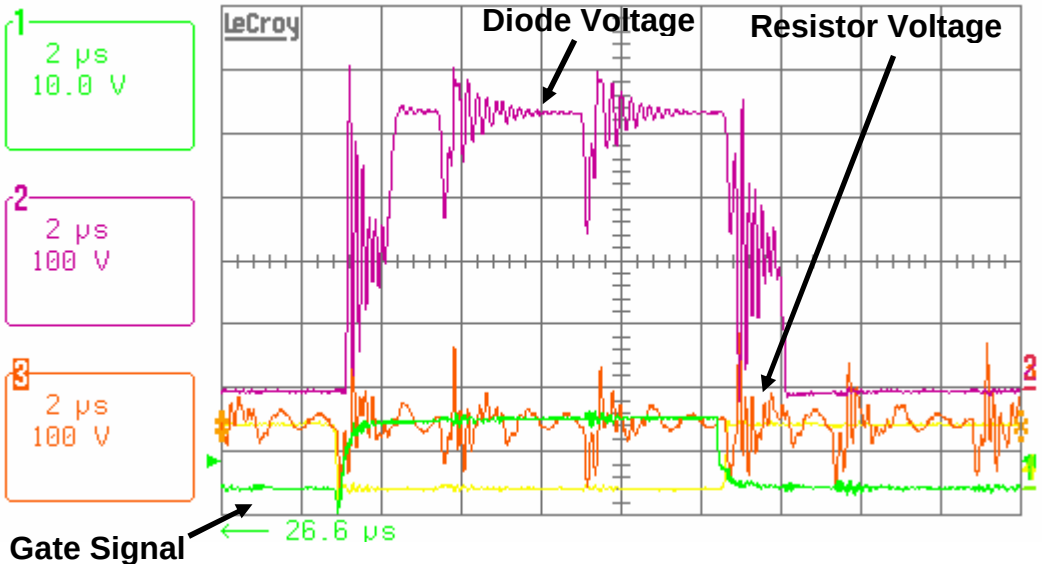

Figure 2.13 – Snubber loss measurement at high power level.

Figure 2.8 shows that the diode voltage is clearly clamped at approximately 500V. The ringing looks very severe but the resistor RMS voltage is still relative small. The loss through the resistor is still less than 1W.

In the two figures above, channel 1 is the gate signal for a MOSFET. As shown in Figure 2.7, the noise on the gate signal is rather severe. The noise is due to the lack of full-ZVS condition. The gate signal is much cleaner in Figure 2.8. The lack of noise can be attributed to achievement of full ZVS condition by the V6 converter. Once again, the full ZVS condition helps reduce ringing and the RMS resistor voltage, Therefore, the power dissipated by the snubber is also reduced.

2.3 V6 Packaging and Layout

As mentioned in the introduction, packaging and layout are critical in low voltage high current designs. The V6 converter must handle high current input. Special packaging and layout concerns must be taken into account for the high current design.

The bus bar plays a critical roll in the V6 layout. The bus bar must provide the positive and negative dc bus connection for each phase leg. In addition to the input bus bar, small output bus bars are added. Addition of bus bars where there is high current is critical to reduce conduction and termination losses. The picture below shows the prototype V6 converter and rectifier board.

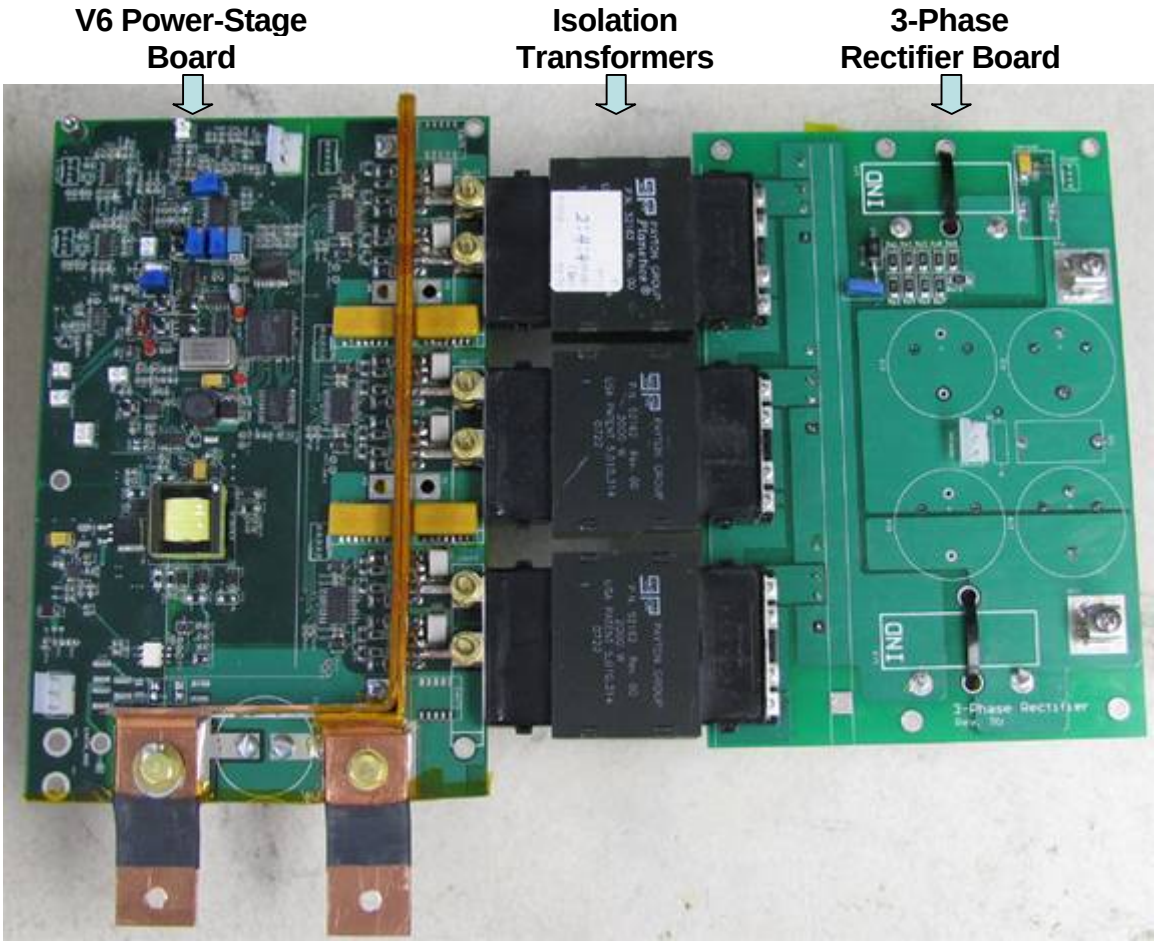

Figure 2.14 – Picture of V6 converter and rectifier

Even when using thicker copper PCBs, the current carrying capability is limited. Extremely wide traces would be required in order to have suitable current carry capability, which would lead to unnecessary parasitic inductance since components cannot be placed as close together. Even with thick traces, termination is a concern. The contact between the device pin and PCB would still not be ideal for high current situations.

The use of bus bars allows for more efficient use of space. Components may be placed closer together as there is sufficient space for the external bus bar. Also, the termination issue is reduced. The V6 improves upon the termination issue by directly connecting the bus bar to the device pin. Conduction loss can be reduced by connecting the bus bar directly to the device. Often, device pins are not ideal for carrying high current. Therefore, it is important to attach the bus bar as close to the device body as possible. The bus bar can also provide thermal cooling. Heat can be dissipated from the device, through the pin, onto the bus bar. For the V6, the primary method of heat dissipation for the devices is a heat sink and fan. The fan is not necessary unless operating under high power condition.

While the bus bar layout is visible in the figure above, it may not be very clear. The figure below shows a simplified layout of the V6 converter clearly defining the bus bar location, MOSFET location, and transformer location.

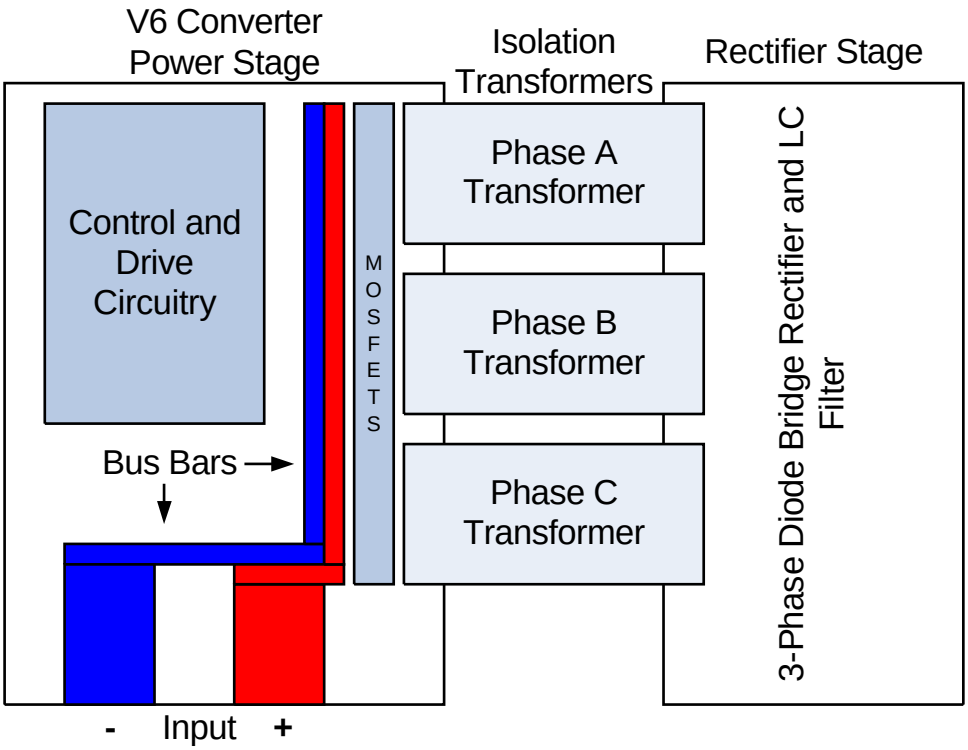

Figure 2.15 – Diagram of V6 converter and rectifier configuration

As the picture above shows, the bus bar and MOSFETs are very close together. The MOSFET pins are able to connect directly to the bus bar to minimize parasitics. The output of the MOSFETs goes to the high frequency transformers, which are also very close to the devices. Minimizing the high current conduction path is important. This helps minimize parasitic inductance and resistance and therefore helps reduce parasitic losses.

3 V6 LOSS ANALYSIS AND EFFICIENCY

As mentioned previously, the V6 converter is able to achieve very high efficiency. In order to obtain high efficiency, proper topology selection is critical but understand the sources of system loss is also crucial. This chapter will analyze the various sources of loss in the V6 converter. Many sources of loss exist in a system. First, primary sources of loss will be considered. Some primary sources of loss are easy to model while others may be more difficult. Primary sources of loss include the following.

- MOSFET conduction loss
- Diode conduction loss
- Switching loss
- Transformer core loss
- Transformer winding loss

Both MOSFET conduction loss and diode conduction losses are fairly easy to estimate as long as circuit operation is properly understood. Complications arise when temperature effects are taken into account. Losses increase for MOSFETs at higher temperatures and losses decrease for diodes at higher temperatures. A rough temperature prediction can be used to improve the models. Switching loss may be difficult to estimate accurately due to various parasitics. Package and PCB parasitic inductances may alter switching times and switching waveforms. Both core and dc transformer winding losses are relatively easy to estimate, although thermal effects can create inaccuracies.

In addition to the above mentioned primary sources of loss, several parasitic sources of loss exist. The parasitic losses include but are not limited to the following:

- Snubber loss
- Capacitor ESR loss
- Body diode conduction loss
- Skin effect
- Proximity effect
- Contact and termination loss
- Switching losses due to loss of soft switching condition
- Various losses due to temperature variation

The parasitic losses mentioned above are particularly difficult to characterize. This thesis will primarily examine snubber loss, capacitor ESR loss, and body diode conduction loss. The losses due to skin effect and proximity effect are very difficult to model. Skin effect losses can be prevented for the most part by utilizing copper windings which are thin enough to ensure that sufficient surface area is available. Proximity effects are difficult to predict as the effect is heavily dependant on how the transformer is wound. Contact and termination losses are also difficult to model and predict. The resistance of a contact may be very small but under high current conditions, the loss can be substantial. Switching losses due to non-full ZVS condition is once again, difficult to predict. Partial ZVS conditions are possible as shown previously. Therefore, the actual loss is very difficult to model. Finally, the system suffers from losses due to temperature variations. It is difficult to know exact junction temperatures of devices or core temperatures. The temperature is also dependant on cooling and environmental factors as well. Temperature effects are partially considered in order to form better models.

3.1 V6 Conduction Loss Analysis

In order to analyze the conduction loss for the V6, the converter operation must be considered. Ideally, the V6 converter should be operated with maximum duty cycle in order to obtain highest efficiency. Therefore, conduction loss analysis will be calculated for the maximum duty cycle condition. Under maximum duty cycle, the V6 converter conducts with 2 phases. The figure below shows the second and third phase conducting together in order to supply the output.

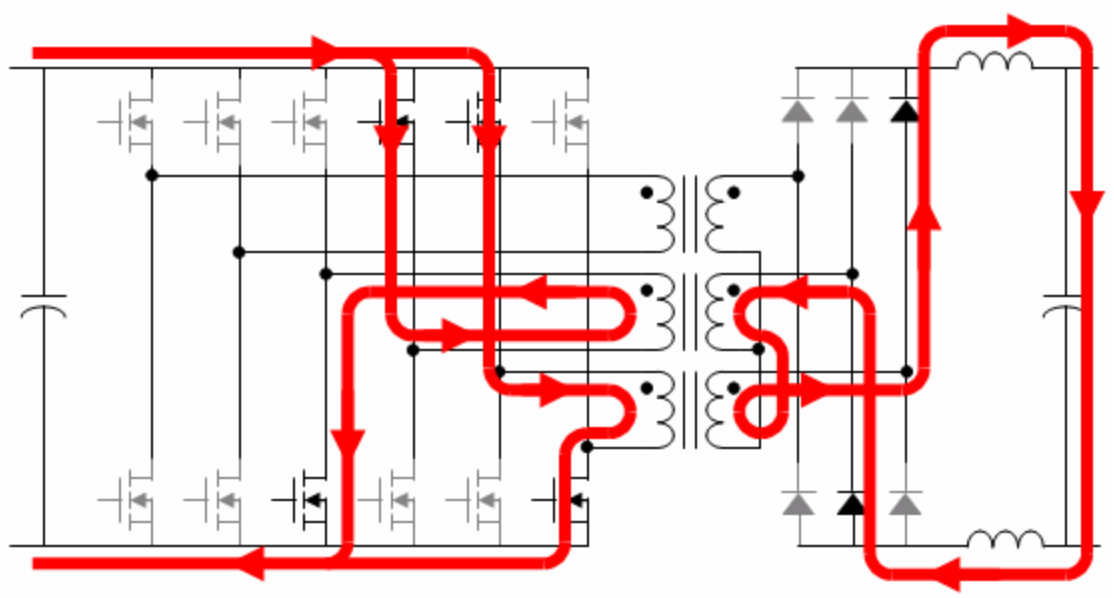

Figure 3.1 – Sample current path for V6 converter under full duty cycle

Under some conditions, it is possible for all three phases to conduct at the same time. If this condition does take place, the third phase typically conducts a minimal amount of current. Two of the phases share the majority of the current. The leakage inductance of the transformer typically prevents the current from being shared equally despite two phases being in parallel. A lower leakage inductance would help the phases share current but can disrupt ZVS conditions. The figure below shows the V6 converter's phase current or transformer current waveforms under full duty cycle. Full duty cycle occurs when the phase shift between 120° and 180°.

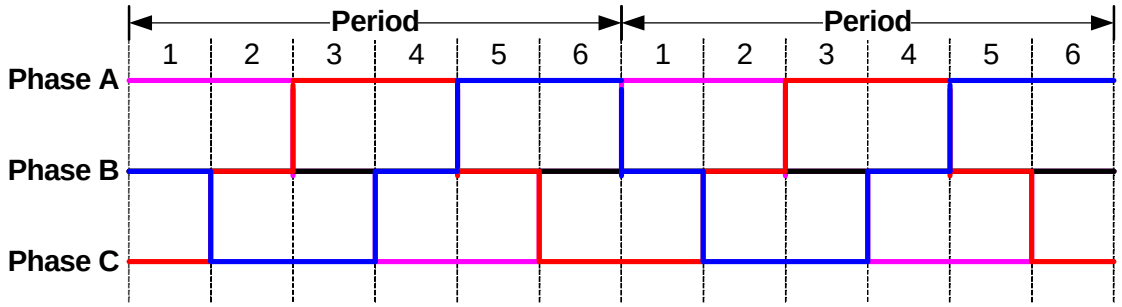

Figure 3.2 – Ideal phase current waveform under full duty cycle

The figure above shows that current is basically conducted by two phases at all times. One phase is always conducting in the positive direction and another phase is conducting in the negative direction. As mentioned previously, a third phase may contribute a small amount of current instead of zero current as shown in the figure above. The minor current is not shown for simplicity. Detailed information regarding the operation of the V6 converter can be found in [14] and [15].

The calculation for conduction loss is simple once operating conditions are analyzed. First, the conduction loss for the primary will be calculated. As shown above, during full duty cycle, the input current is equally shared by two phases. The case where a parallel conduction path is available via the third phase will be ignored. The additional conduction path reduces losses and, therefore, is not the worst case condition. Each phase shares half the current but has two switches in the path. This means the effective resistance per phase must be doubled.

I_{in} = Total Input Current

$$P_{c-MOS} = 2 \cdot \left(\left(\frac{I_{in}}{2} \right)^2 \cdot 2 \cdot R_{DS-ON} \right) \qquad \text{(Eq. 3.1)}$$

As mentioned previously, in order to minimize the conduction loss, a low $R_{DS\text{-}ON}$ MOSFET is important. The V6 converter utilizes the IXYS FMM150-0075. The FMM150-0075 is a 75V 150A device. The typical $R_{DS\text{-}ON}$ is 3.2mO, which is very low. The $R_{DS\text{-}ON}$ of the device can vary greatly depending on the junction temperature. Therefore, losses at different junction temperatures should be considered. Based on the manufacturer's datasheet, the approximate typical $R_{DS\text{-}ON}$ value at certain temperatures can be calculated.

Table 3.1 – Approximate MOSFET R_{DS-ON}

Temperature	Approximate R_{DS-ON}
25°C	3.2mO
50°C	3.84mO
75°C	4.32mO
100°C	4.64mO

According to the manufacturer datasheet, the increase in R_{DS-ON} due to temperature is fairly linear. Therefore, the temperature coefficient of the device can be calculated. The temperature coefficient is the % increase in resistance per 1°C rise in temperature. The temperature coefficient is calculated as approximately 0.006 or 0.6% rise in resistance per 1°C rise in temperature.

In order to apply the temperature coefficient, we must estimate the junction temperature of the MOSFET at different operating conditions. This is particularly difficult since the junction temperature is dependent on several factors including cooling system, ambient temperature, layout, packaging, etc. Better cooling systems yield lower junctions temperatures. Lower junction temperatures translate into increased system reliability. At 110% load condition, one can assume 75°C junction temperature for relatively safe temperature margins. At 10% load condition, it can be assumed that the device temperature will be close to ambient. The junction temperature of the MSOFET has a nonlinear relationship with power level. This is due to the fact that the power loss at low power levels is much smaller than the power loss at higher power conditions. The table below shows the estimated junction temperature and R_{DS-ON} at various operating conditions.

Table 3.2 – Estimated MOSFET junction temperature at various operating conditions

I_{in} (A)	P_{in} (W)	Estimated Junction Temp. (°C)	Rise in Temp. Over Ambient (°C)	% Increase in R_{DS-ON} Due to Temp.	New R_{DS-ON} Based on Junction Temp. (mO)	$P_{conduction-MOS}$
10	500	25	0	0	3.20	0.32
20	1000	27	2	1.2	3.24	1.30
30	1500	29	4	2.4	3.28	2.95
40	2000	31	6	3.6	3.32	5.30
50	2500	34	9	5.4	3.37	8.43
60	3000	37	12	7.2	3.43	12.35
70	3500	40	15	9	3.49	17.09
80	4000	45	20	12	3.58	22.94
90	4500	50	25	15	3.68	29.81
100	5000	60	35	21	3.87	38.72
110	5500	75	50	30	4.16	50.34

As shown above, the conduction loss increases rapidly with increase in current. Also, the junction temperature of the device can make a substantial difference on the conduction loss. Whenever there are losses, the loss will be converted to heat and will increase the junction temperature of the device. Increases in junction temperature causes the R_{DS-ON} of the MOSFET to increase which in turn creates more losses.

The table above shows the conduction loss due to the semiconductor portion. The manufacturer also specifies an additional resistance from the pin to chip. This resistance is due to the device package, wire-bound, etc. The resistance specified by the manufacturer, 1.6mO, is significant and cannot be ignored. Copper also has a temperature coefficient which affects the resistance of the interconnects as temperature changes. Therefore, when including the pin to chip resistance, the resistance should be adjusted based on the temperature as well. The temperature coefficient of copper is 0.0039 or 0.39%. Now, a more accurate conduction loss estimate can be developed. The table below shows conduction loss figures including the pin to chip resistance.

Table 3.3 – Estimated MOSFET conduction loss including pin to chip resistance

I_{in} (A)	P_{in} (W)	Estimated Junction Temp. (°C)	Rise in Temp. Over Ambient (°C)	% Increase in Copper Due to Temp.	Copper Res. Based on Junction Temp. (mO)	Total Primary Cond. Loss (W)
10	500	25	0	0	1.600	0.480
20	1000	27	2	0.78	1.612	1.940
30	1500	29	4	1.56	1.625	4.412
40	2000	31	6	2.34	1.637	7.924
50	2500	34	9	3.51	1.656	12.572
60	3000	37	12	4.68	1.675	18.379
70	3500	40	15	5.85	1.694	25.390
80	4000	45	20	7.8	1.725	33.976
90	4500	50	25	9.75	1.756	44.032
100	5000	60	35	13.65	1.818	56.904
110	5500	75	50	19.5	1.912	73.471

3.2 Diode Conduction Loss Analysis

In addition to MOSFET conduction losses, the V6 has diode conduction losses on the secondary side. Diode conduction loss is also simple to calculate based on diode forward voltage drop and output current. The equation below may be used to calculate the diode conduction loss.

$$P_{loss} = I \cdot V_f \quad \text{(Eq. 3.2)}$$

Just as the conduction path for the input current was analyzed, the conduction path for the output current must be analyzed. At full duty cycle, the output current effectively flows through two diodes at all times. If a third phase on the primary is conducting, it is possible for a third diode to become active and share some of the current. Typically, the current in the third diode is minimal. Since a lower forward voltage drop is observed at lower forward currents, the conduction by the third diode would reduce overall losses. The diode conduction loss will be calculated based on 2 diode conduction in order to achieve the worst case estimation. Therefore, the total diode conduction loss for the system can be calculated with the equation below.

$$P_{c-diode} = 2 \cdot I \cdot V_f \quad \text{(Eq. 3.3)}$$

The forward voltage drop of a diode can vary significantly based on junction temperature and forward current. The manufacturer's datasheet will typically have forward voltage drop values based on current and junction temperature. The table below shows approximate forward voltage drop based on current and temperature for the diode selected for use in the V6 converter. The listed forward voltage drop is approximate especially since the forward voltage drop may vary due to manufacturing tolerances. The table lists the approximate output power of the V6 converter based on current and an output voltage of 400V. Finally, the total conduction loss by the diodes is listed based on the above equation. The total power lost accounts for the conduction of two diodes at all times.

Table 3.4 – Approximate diode conduction loss

Output Current (A)	P_{out} (V_o = 400)	V_f@25°C (V)	V_f@125°C (V)	Total P_{loss} 25°C (W)	Total P_{loss} 125°C (W)
1.25	500	0.76	0.525	1.9	1.3125
2.5	1000	0.85	0.625	4.25	3.125
3.75	1500	0.9	0.67	6.75	5.025
5	2000	0.93	0.695	9.3	6.95
6.25	2500	0.96	0.72	12	9
7.5	3000	0.975	0.735	14.625	11.025
8.75	3500	0.99	0.749	17.325	13.1075
10	4000	1.015	0.77	20.3	15.4
11.25	4500	1.03	0.78	23.175	17.55
12.5	5000	1.045	0.8	26.125	20
13.75	5500	1.07	0.82	29.425	22.55

As shown above, the forward voltage drop varies greatly depending on forward current and temperature. Diodes have a negative temperature coefficient and therefore, the forward drop decreases as temperature increases. Higher temperatures will increase reverse bias currents: however, the current values are still very small and should not contribute substantially to the losses.

Once again, when considering the system loss, temperature effects should be considered. Unfortunately, the junction temperature is once again dependent on thermal management and environmental conditions. In order to obtain a slightly better model, when calculating the system efficiency, low temperature losses are used at low power while middle temperature loss estimates are used at higher power conditions

3.3 V6 Switching Loss Analysis

As mentioned in the introduction, switching loss is also a common source of loss in switching converters. Switching loss may be estimated by calculating the area underneath the V_{DS} and I_D waveforms and multiplying by the switching frequency and switching times. Loss must be calculated for both turn-on and turn-off conditions to find the total switching loss. As mentioned in the introduction, the equations below can be used as crude estimates of the area underneath the V_{DS} and I_D waveforms or the switching energy.

$$E_{on} = \frac{1}{2} V_{DS} I_D (t_2 - t_1) \quad \text{(Eq. 3.4)}$$

$$E_{off} = \frac{1}{2} V_{DS} I_D (t_4 - t_3) \quad \text{(Eq. 3.5)}$$

$$P_{loss-sw} = (E_{on} + E_{off}) f_s \quad \text{(Eq. 3.6)}$$

The values for t_{off} and t_{on} should ideally be measured. Sometimes, measurement may be difficult. Typically, the device manufacturer will provide some typical values for t_{off} and t_{on} and values for E_{off} and E_{on} maybe provided as well. Unfortunately, the values for t_{off}, t_{on}, E_{off}, and E_{on} are dependent on many factors including temperature, current, gate resistor, gate voltage, load type (resistive or inductive), etc. Typically, the values provided by the manufacturer will not match exactly. If the test conditions are very similar, then the manufacturer's datasheet may provide a reasonable estimate. The manufacturer does provide a plot of switching energy vs. load current based on inductive switching.

Based on the plot, the switching energy can be determined for various current conditions. The switching energy can be modified in order to better reflect the V6 system conditions instead of the datasheet test conditions. For example, the datasheet uses a 10O gate resistor test case. The V6 employs a gate turn-off diode for faster device turn-off transition. The turn-off diode is able to reduce the time required to turn-off the device and therefore, reduce turn-off transition loss. Based on the datasheet, the reduced turn-off resistance should reduce E_{off} by approximately 40% compared to the 10O gate resistor test case provided in the datasheet. The turn-on energy data in the datasheet is based on

10O gate resistance as well. The V6 converter utilizes a 4.7O resistor instead. Therefore, the switching energies can be adjusted in order to better reflect the system conditions. The table below shows the adjusted estimated switching energies.

Table 3.5 – Corrected turn on and off energies values

Current (A)	E_{on} Corrected (mJ)	E_{off} Corrected (mJ)
20	0.060	0.060
40	0.105	0.120
60	0.150	0.210
80	0.195	0.300
100	0.255	0.400
120	0.315	0.515
140	0.375	0.640

With some measured values of E_{on} and E_{off}, an equation can be developed to describe E_{on} and E_{off}. The fitted equations are in the following form.

$$E_{on} = k \cdot I^{l} \quad \text{(Eq. 3.7)}$$

$$E_{off} = m \cdot I^{n} \quad \text{(Eq. 3.8)}$$

Coefficients k, l, m, and n can be determined to best fit the data points.

The figure below shows the curve for turn-on switching energy. The following equation was used to fit the data points.

$$E_{on} = 0.00197 \cdot I^{1.06} \qquad \text{(Eq. 3.9)}$$

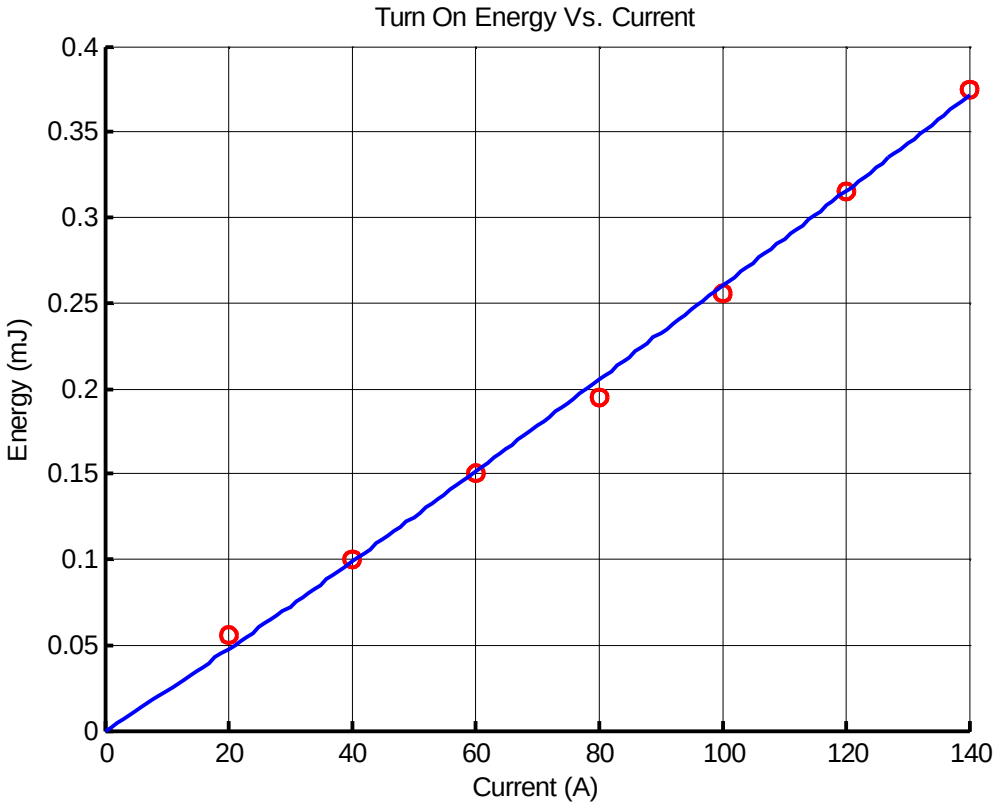

Figure 3.3 – Turn-on energy data samples and fitted line

The figure below shows the curve for turn-off switching energy. The following equation was used to fit the data points.

$$E_{off} = 0.00102 \cdot I^{1.3} \qquad \text{(Eq. 3.10)}$$

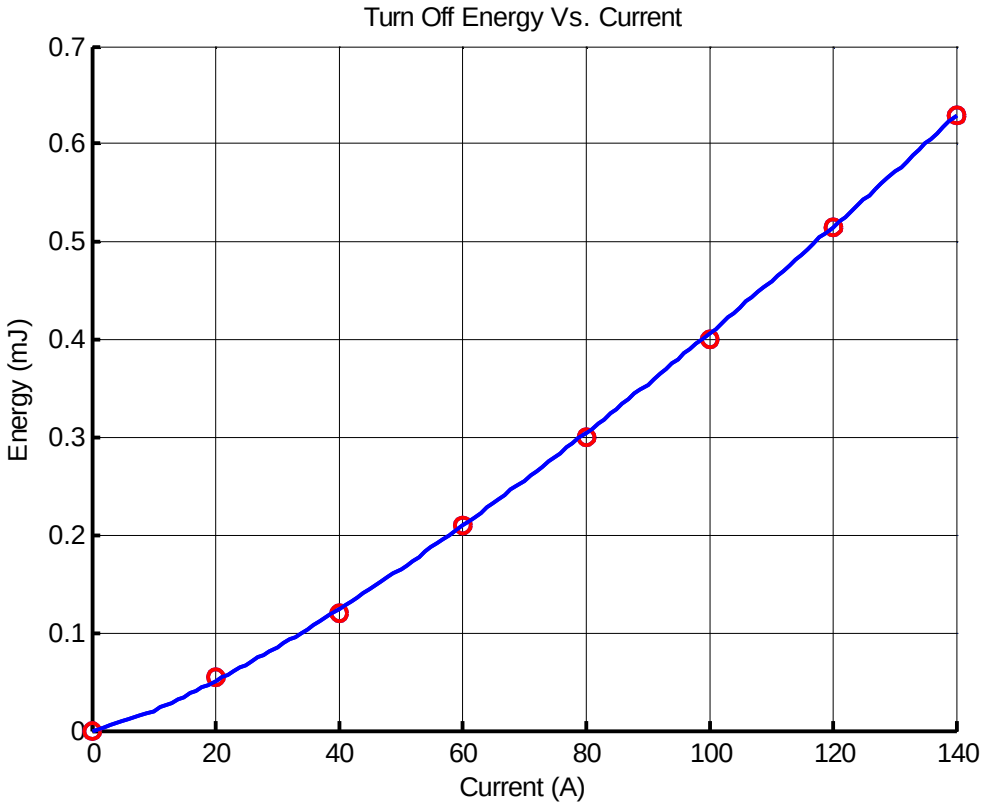

Figure 3.4 – Turn-off energy data samples and fitted line

With the equation, the switching energy for any current can easily be estimated.

Table 3.6 – Detailed E_{off} estimates

Current (A)	E_{on} (mJ)	E_{off} (mJ)
0	0	0
5	0.0108	0.008
10	0.0226	0.020
15	0.0348	0.035
20	0.0472	0.050
25	0.0597	0.067
30	0.0725	0.085
35	0.0853	0.104
40	0.0983	0.123
45	0.1114	0.144
50	0.1246	0.165
55	0.1378	0.187
60	0.1511	0.209

The table above shows more detailed values turn-off values which were calculated based on the equation. Based on the table above, the switching loss is simple to calculate. The total switching energy for typical hard switching condition can be estimated by multiplying the sum of E_{on} and E_{off} with the switching frequency.

In order to calculate the switching loss for the V6 converter, the soft switching conditions must be considered. If soft switching is achieved, the switching loss for that particular device can be reduced significantly. Under ZVS or Zero Current Switching (ZCS) conditions, the switching loss can be considered zero. As mentioned previously, the V6 achieves different soft switching conditions depending on the phase leg and whether the condition is turn-on or turn-off. The V6 soft switching table is shown again for convenience.

Table 3.7 – V6 soft switching conditions

Condition	Leading Leg	Lagging Leg
Turn On	ZCS	ZVS
Turn Off	ZCS	None

The lagging leg ZVS turn on condition can easily be lost under light load condition as noted in [15]. The lagging leg ZVS is dependant on the leakage inductance of the transformer. When the load is light, and, therefore, the input current is small, there is not enough energy to discharge the output capacitance of the MOSFETs. Under sufficiently high load conditions, the V6 converter achieves some sort of soft switching condition in all devices except for lagging leg turn off. Therefore, when calculating the switching loss under sufficiently high load conditions, only the lagging leg turn-off loss needs to be considered. Even under lighter load conditions, partial soft-switching can be achieved by the V6 converter. This is discussed further in a later section. The total switching loss for the V6 operating at full duty cycle and sufficiently high load can be estimated with the equation below. The equation below reflects the fact that each leg has two switches which do not achieve soft switching turn off and there are three phases. A total of six devices do not achieve a soft switching condition for turn off.

$$P_{loss\_sw} = 6\left(E_{off}\right)f_s \qquad \text{(Eq. 3.11)}$$

Table 3.8 – Turn-on and turn-off energies from datasheet and corrected values

Total Input Current (A)	Approximate Phase Current (A)	E_{off} Corrected (mJ)	Total $P_{loss-sw}$ f_s = 40kHz (W)	Total $P_{loss-sw}$ f_s = 50kHz (W)	Total $P_{loss-sw}$ f_s = 60kHz (W)
0	0	0	0	0	0
10	5	0.008	1.99	2.49	2.99
20	10	0.020	4.90	6.12	7.34
30	15	0.035	8.28	10.35	12.42
40	20	0.050	12.02	15.03	18.04
50	25	0.067	16.08	20.10	24.12
60	30	0.085	20.38	25.47	30.56
70	35	0.104	24.89	31.11	37.33
80	40	0.123	29.62	37.02	44.42
90	45	0.144	34.51	43.14	51.77
100	50	0.165	39.58	49.47	59.37
110	55	0.187	44.81	56.01	67.21
120	60	0.209	50.16	62.70	75.24

As show in the table above, the switching losses can be very substantial and increases with frequency. Even with just one condition out of four failing to achieve soft switching, the loss is very high. The above calculation does not account for the non-full ZVS condition shown in the previous chapter. The lack of full-ZVS condition means the switching loss will not be negligible but the switching loss is difficult to predict without having detailed switching waveforms.

In addition to switching transition loss, there is additional switching loss due to the discharging of the MOSFET output capacitance at turn on. For ZCS condition, no switching loss was assumed but power loss occurs when the output capacitance of the MOSFET is discharged. The power loss can be calculated with the equation below.

$$P_{MOS-\cos s} = \frac{1}{2} \cdot C \cdot V^2 \cdot f_s \qquad \text{(Eq. 3.12)}$$

The loss is approximately 0.375W based on 1nF output capacitance, 50V input, and 50 kHz switching. Switches obtaining ZVS turn-on condition do not suffer from this loss since the output capacitance is already discharged at turn-on.

3.4 V6 Transformer Core Loss Analysis

As discussed in the introduction, magnetic components such as inductors and transformers typically have core loss associated with them. The steps discussed in the introduction can be used to calculate the core loss. The first step is to find the applied voltage-seconds as defined below. The voltage seconds is dependent on the duty cycle. Full duty cycle is assumed for this calculation. During full duty cycle, the time period for the equation below is 1/3 the switching period. The voltage is simply the input voltage. Different values for the applied voltage-seconds can be calculated to account for variability in the input source. Sources such as fuel cells and photovoltaics may vary in output voltage.

$$\lambda(t) = \int_{t_1}^{t_2} v(t)dt \qquad \text{(Eq. 3.13)}$$

Table 3.9 – Applied voltage-seconds for different input voltages and switching frequencies

Input Voltage (V)	40kHz Switching	50kHz Switching	60kHz Switching
44	$366.67V \cdot \mu s$	$293.33V \cdot \mu s$	$244.44V \cdot \mu s$
46	$383.33V \cdot \mu s$	$306.67V \cdot \mu s$	$255.56V \cdot \mu s$
48	$400.00V \cdot \mu s$	$320.00V \cdot \mu s$	$266.67V \cdot \mu s$
50	$416.67V \cdot \mu s$	$333.33V \cdot \mu s$	$277.78V \cdot \mu s$
52	$433.33V \cdot \mu s$	$346.67V \cdot \mu s$	$288.89V \cdot \mu s$
54	$450.00V \cdot \mu s$	$360.00V \cdot \mu s$	$300.00V \cdot \mu s$

Based on the applied voltage seconds, the peak flux density (ΔB) can be calculated with the following equation.

$$\Delta B = \frac{\lambda(t)}{2 n_1 A_e} \qquad \text{(Eq. 3.14)}$$

n_1 = Primary Transformer Turns Ratio

A_e = Effective Core Area of Transformer

The peak flux density is dependent on applied voltage-seconds, primary transformer turns ratio, and effective core area. Since peak flux density is directly related

to core loss, one can easily see how to modify the transformer design to reduce core loss. Typically, the input voltage cannot be changed but switching frequency can be increased to reduce applied voltage-seconds. Unfortunately, increases in switching frequency may lead to increased switching loss. Primary turns ratio can easily be increased as long as there is sufficient space, but copper resistance and losses will increase due to increased winding lengths. Larger cores may be used to increase effective core area but size and cost of the transformer will increase.

The table below compares peak flux density values with input voltage, number of primary turns, and switching frequency. The core employed by the V6 is the EI64 core. The effective core area of the EI64 is 511mm^2. The V6 high frequency transformer uses two primary turns. The table below shows different primary turns for comparison.

Table 3.10 – Peak flux density compared with input voltage, primary turns, and switching frequency

Input Voltage (V)	Number of Primary Turns	Peak Flux Density 40kHz Switching (T)	Peak Flux Density 50kHz Switching (T)	Peak Flux Density 60kHz Switching (T)
44	1	0.3588	0.2870	0.2392
	2	0.1794	0.1435	0.1196
	3	0.1196	0.0957	0.0797
46	1	0.3751	0.3001	0.2501
	2	0.1875	0.1500	0.1250
	3	0.1250	0.1000	0.0834
48	1	0.3914	0.3131	0.2609
	2	0.1957	0.1566	0.1305
	3	0.1305	0.1044	0.0870
50	1	0.4077	0.3262	0.2718
	2	0.2038	0.1631	0.1359
	3	0.1359	0.1087	0.0906
52	1	0.4240	0.3392	0.2827
	2	0.2120	0.1696	0.1413
	3	0.1413	0.1131	0.0942
54	1	0.4403	0.3523	0.2935
	2	0.2202	0.1761	0.1468
	3	0.1468	0.1174	0.0978

Some key trends may be noticed from the data above:

- Increases in input voltage increases peak flux density.
- Increases in switching frequency decreases peak flux density.
- Increasing the number of primary turns decreases peak flux density

Once the peak flux density is known, the core loss can be estimated. The equation for core loss calculation is shown below.

$$P_L = af^{\,c} B^{\,d} \qquad \text{(Eq. 3.15)}$$

P_L = Power loss in $\frac{mW}{cm^3}$

B = Peak flux density in kG

f = frequency in kHz

The following are coefficients and are defined below.

$a = 0.158$

$c = 1.36$

$d = 2.86$

Since P_L is in mW / cm^3, the effective volume of the EI64 core is required to get the core loss.

V_e = 35,539 mm^3 = 35.539 cm^3

The equation for power loss yields the individual transformer core loss. Since there are three transformers in the V6, the power loss value must be multiplied by three to obtain the total core loss for the V6.

Table 3.11 – Total core power loss compared with input voltage, primary turns, and switching frequency at 80°C

Input Voltage (V)	Number of Primary Turns	Total Core Loss 40kHz Switching (W)	Total Core Loss 50kHz Switching (W)	Total Core Loss 60kHz Switching (W)
44	1	98.19104	70.25979	53.44843
	2	13.52465	9.677453	7.361888
	3	4.241359	3.03487	2.308704
46	1	111.5025	79.78469	60.69427
	2	15.35815	10.9894	8.359916
	3	4.816348	3.446298	2.621688
48	1	125.9352	90.1119	68.55044
	2	17.34608	12.41184	9.44201
	3	5.439768	3.892381	2.961035
50	1	141.5309	101.2713	77.03969
	2	19.49421	13.94892	10.6113
	3	6.113426	4.374411	3.327727
52	1	158.3313	113.2927	86.18464
	2	21.80826	15.60472	11.87091
	3	6.839116	4.893673	3.722743
54	1	176.3776	126.2055	96.00779
	2	24.29392	17.38331	13.22393
	3	7.618625	5.451444	4.147054

By looking at the table above, it is easy to notice that the number of primary turns has a very large effect on the total core loss. The nominal operating condition for the V6 is 50V input, 50 kHz switching, and 2 primary turns. Therefore, the core loss is approximately 14W.

Like many other devices components, core loss is heavily dependant on temperature. The transformer core temperature coefficient varies and may be negative or positive over different temperature ranges. At low temperatures, the core loss is typically high. The core loss decreases as temperature increases. At a certain point, there is an inflection point and the core loss increases again as temperature increases. The temperature range that minimizes the core loss is dependant on the material of the core.

The core loss variation due to temperature is also dependant on frequency and peak flux density which core loss estimations even further.

3.5 V6 Transformer Copper Loss Analysis

As discussed previously, transformers may have copper loses in addition to core losses. The copper losses are increased further due to skin and proximity effects if the transformer is not properly designed. Copper loss simply due to current is easy to estimate, but the loss estimation becomes substantially more difficult when other factors such as skin effect and proximity effects are considered. In order to improve the loss model, the dc resistance of the transformer winding can at least be considered. The dc resistance of a transformer winding can be calculated with the following equation.

$$R = \rho \frac{l}{A} \qquad \text{(Eq. 3.16)}$$

ρ = Resistivity of copper $= 1.724 \cdot 10^{-6}\ \Omega \cdot cm$ at room temperature

l = Length of winding

A = Cross-sectional area of copper

The specifications for the transformers used in V6 converter are as follows:

l = 13 inches = 33.02cm

A = 25600mil^2 = 0.165cm^2

R = 0.3448 O

In order to confirm the calculations, the dc resistance of the transformer can be directly measured. The measurement can be performed by running dc current through the transformer winding and measuring the voltage drop across the terminals. With the voltage and current values known, the resistance is simple to calculate.

Table 3.12 – Measured dc winding resistance for primary side

Current (A)	Voltage Drop (mV)	Resistance (mO)
1.0038	0.328	0.3268
2.0022	0.633	0.3162
3.0058	0.934	0.3107
4.0035	1.248	0.3117
5.0309	1.581	0.3143
5.509	1.736	0.3151
6.017	1.899	0.3156

The data above shows that the calculated resistance and the measured resistance values are close. A primary winding dc resistance of 0.32 mO will be assumed for loss calculations. With the dc resistance, the low frequency copper loss can be calculated. The figure below shows the low frequency copper loss at various power levels.

Table 3.13 – Estimated winding loss on primary side

Input Power (W)	RMS Current Per Phase (A)	Low Frequency Conduction Loss per Phase (W)	Total XF Low Frequency Copper Loss (W)
500	3.3333	0.0036	0.0107
1000	6.6667	0.0142	0.0427
1500	10.0000	0.0320	0.0960
2000	13.3333	0.0569	0.1707
2500	16.6667	0.0889	0.2667
3000	20.0000	0.1280	0.3840
3500	23.3333	0.1742	0.5227
4000	26.6667	0.2276	0.6827
4500	30.0000	0.2880	0.8640
5000	33.3333	0.3556	1.0667
5500	36.6667	0.4302	1.2907

As shown in the table above, the low frequency copper loss is relatively small compared to many other sources of loss such as MOSFET conduction loss and diode conduction loss. The copper loss shown above does not account for increase in the copper resistance due to increase in temperature. Losses such as core loss, contact loss, and copper loss, create heat and raise the temperature of the transformer windings. This in turn causes copper losses to increase. The increase in temperature also makes copper more susceptible to skin effect. Skin effect can greatly increase the effective resistance of a high frequency transformer winding and, therefore, creating additional losses. Even if wire is selected such that skin depth matches the copper thickness, the current density varies throughout the depth. Therefore, greater amounts of current will flow at the surface

and less current at the center of the conductor. The conductor is still not fully utilized and therefore, the effective resistance will increase.

The calculations and measurements above help model the primary side copper winding loss. The secondary side of the transformer may also have copper loss as well. The dc resistance of the secondary side was also measured to help estimate conduction loss in the secondary winding.

Table 3.14 – Measured dc winding resistance for secondary

Current (A)	Voltage Drop (mV)	Resistance (mO)
1.006	3.032	3.0139
2.0049	6.034	3.0096
3.0055	9.039	3.0074
4.0022	12.033	3.0065
5.0313	15.129	3.0069
6.035	18.148	3.0071

The measurements show that the dc resistance of the secondary winding is approximately 3mO. The transformer utilized by the V6 converter had two secondary windings which are put in series. Therefore, the equivalent resistance is actually 6mO. The higher resistance can be attributed to smaller copper as well as longer winding length. The resistance in the secondary is much greater than the primary winding resistance but the current is much smaller. The table below calculates the low frequency conduction loss for the secondary winding.

Table 3.15 – Estimated winding loss on secondary side

Input Power (W)	RMS Current Per Phase on Secondary (A)	Low Frequency Conduction Loss per Phase (W)	Total XF Low Frequency Copper Loss (W)
500	0.8333	0.0042	0.0125
1000	1.6667	0.0167	0.0500
1500	2.5000	0.0375	0.1125
2000	3.3333	0.0667	0.2000
2500	4.1667	0.1042	0.3125
3000	5.0000	0.1500	0.4500
3500	5.8333	0.2042	0.6125
4000	6.6667	0.2667	0.8000
4500	7.5000	0.3375	1.0125
5000	8.3333	0.4167	1.2500
5500	9.1667	0.5042	1.5125

The calculations above show that the low frequency copper loss on the secondary side is actually greater than the primary. Despite the lower current, the secondary suffers from higher losses due to the higher winding resistance.

3.6 V6 Snubber Loss Analysis

Calculating power loss for the snubber is rather difficult since it can be dependant on switching characteristics. Based on simulation, the power loss of the voltage clamp configuration is relatively low. As the load increases, the snubber loss increases due to the increased stored energy in the leakage inductance. At higher loads when full ZVS condition is obtained, the snubber loss decreases due to less severe perturbations. Hard switching conditions create heavy voltage spikes and ripples, which must be damped by the snubber. The table below shows some estimated snubber loss figures based on simulation.

Table 3.16 – Snubber loss estimation at various load conditions

Input Power (W)	Estimated Snubber Power Loss (W)
500	0.1
1000	0.2
1500	0.4
2000	0.7
2500	1
3000	0.6
3500	0.7
4000	0.8
4500	0.9
5000	1
5500	1.1

3.7 Capacitor ESR Loss

Many other parasitic losses exist within the system. For example, capacitor ESR is a concern, particularly for high current systems. Capacitors are important for maintaining waveform quality and reducing voltage spikes and ripples. These capacitors may have to supply and draw large amounts of current. The capacitor ESR losses can become significant when the current is large. Paralleling additional capacitors can help reduce losses due to capacitor ESR since RMS current through individual capacitors is reduced. Simulation results show that the total RMS current seen by the input dc-bus capacitors is approximately 50% of the input current. The ESR of the capacitor can be found in the manufacturer datasheet or measured. The V6 utilizes six film capacitors near the primary MOSFETs.

$$P_{Loss\ -\ ESR} = I_{rms}{}^{2} \cdot R_{ESR} \qquad \text{(Eq. 3.17)}$$

Based on the simple equation above, the capacitor ESR loss can be estimated.

Table 3.17 – Capacitor ESR loss estimation

Input Current (A)	Approximate RMS Capacitor Current (A)	Approx. Current per Capacitor (A)	Power Loss per Capacitor (W)	Total Power Lost (W)
10	5	0.833	0.007	0.042
20	10	1.667	0.028	0.167
30	15	2.500	0.063	0.375
40	20	3.333	0.111	0.667
50	25	4.167	0.174	1.042
60	30	5.000	0.250	1.500
70	35	5.833	0.340	2.042
80	40	6.667	0.444	2.667
90	45	7.500	0.563	3.375
100	50	8.333	0.694	4.167
110	55	9.167	0.840	5.042

3.8 Body Diode Conduction Loss

The body diode may conduct in the V6 converter during the dead time. For each switching period, only two diodes conduct per phase. A total of 6 diodes will conduct per switching period in the V6 converter. Due to the poor performance and high voltage drop of the body diode, loss may occur through body diode conduction. The body diode conduction loss can be calculated with the following equation.

$$P_{BodyDiode\ -Cond} = I \cdot V \cdot t \cdot f_s$$

The body diode forward voltage drop is estimated to be 1.1V based on the data sheet. Diode voltage drop will depend on temperature and current but unfortunately, detailed information regarding the body diode is not available. A dead time interval of 300ns is used. The value may vary due to component tolerances in the gate drive circuitry. The table below shows the predicted body diode conduction loss.

Table 3.18 – Body diode conduction loss estimation

Input Power (W)	Body Diode Conduction Loss (W)
500	0.247
1000	0.495
1500	0.742
2000	0.990
2500	1.237
3000	1.485
3500	1.732
4000	1.980
4500	2.227
5000	2.475
5500	2.722

3.9 Other Parasitic Losses

Another source of loss, which is difficult to estimate is parasitic inductance. Parasitic inductance can cause excessive voltage spikes during switching. Switching waveforms affected will see larger losses in addition to higher voltage stress. Higher voltage stress may lead to device failure. If higher voltage rating devices are used, typically conduction loss of the device increases since the voltage rating has increased.

Termination is another major parasitic loss, especially for high current situation. Each mechanical connection made introduces termination losses. Mechanical connections do not have perfect contact and a small resistance exists between the two contacts. Ideally, mechanical contacts should be eliminated where possible and one piece of copper should be used for connection. The mechanical contacts may have a small resistance but the loss can become very high due to the large currents of high current systems. The loss would be simple to calculate with the conduction loss equation, but the resistance is difficult to predict since the resistance is due to the physical construction. Under high current conditions, the terminals can get hot due to the power loss. The higher temperature increases the resistance of copper, further increasing parasitic losses. In addition to mechanical contact resistance, the resistance increases further if two different materials are used for contacts.

As mentioned previously, skin effect and proximity effect can also create significant amounts of loss. Skin effect raises the effective resistance of the transformer winding. Since large currents are flowing through the transformer, an increase in resistance can create large amounts of loss.

3.10 V6 Efficiency Estimation

Based on the loss estimations above, the efficiency of the V6 converter can be estimated. Once again, the temperature and other factors have a significant effect on system efficiency. For this estimation, the following conditions will be assumed.

Table 3.19 – Efficiency estimation test conditions

Nominal Input Voltage	50V
Input Current	20 – 110A
Nominal Output Voltage	400V
Output Current	2.5A – 12.5A

The following table summarizes the total losses at various operating conditions

Table 3.20 – Loss summary with 50V input and varied current conditions

Input Power (W)	MOSFET Conduction Loss (W)	MOSFET Switching Loss (W)	Diode Loss (W)	Core Loss (W)	Snubber Loss (W)	Body Diode Cond. Loss (W)	XF Cond. Loss (W)	Cap. ESR Loss (W)
500	0.48	2.865	1.606	14	0.1	0.25	0.023	0.04
1000	1.94	6.495	3.687	14	0.2	0.50	0.093	0.17
1500	4.41	10.725	5.887	14	0.4	0.74	0.209	0.38
2000	7.92	15.405	8.125	14	0.7	0.99	0.371	0.67
2500	12.57	20.475	10.5	14	1	1.24	0.579	1.04
3000	18.38	25.846	12.825	14	0.6	1.49	0.834	1.50
3500	25.39	31.486	15.216	14	0.7	1.73	1.135	2.04
4000	33.98	37.396	17.85	14	0.8	1.98	1.483	2.67
4500	44.03	43.516	20.362	14	0.9	2.23	1.877	3.38
5000	56.90	49.846	23.062	14	1	2.48	2.317	4.17
5500	73.47	56.386	25.987	14	1.1	2.72	2.803	5.04

Based on the loss numbers, the total power loss can be calculated and the efficiency of the system can be estimated.

Table 3.21 – Efficiency summary with 50V input and varied current conditions

Input Current (A)	Input Power (W)	Total Power Lost (W)	Power Lost (%)	Estimated System Efficiency (%)
10	500	19.633	3.93	96.073
20	1000	27.550	2.76	97.245
30	1500	36.547	2.44	97.564
40	2000	47.815	2.39	97.609
50	2500	60.825	2.43	97.567
60	3000	74.635	2.49	97.512
70	3500	90.564	2.59	97.412
80	4000	108.672	2.72	97.283
90	4500	128.417	2.85	97.146
100	5000	151.457	3.03	96.971
110	5500	178.707	3.25	96.751

3.11 V6 Experimental Efficiency Results

The efficiency of the V6 converter has been measured using prototype hardware. Similar input and output conditions as the calculations are used. Once again, the following conditions are used.

Table 3.22 – Efficiency measurement conditions

Nominal Input Voltage	~50V
Input Current	0 – 110A
Nominal Output Voltage	~400V
Output Current	0A – 14A

The input voltage is raised slightly at higher power levels in order to maintain 400V output. The test load points are slightly different due to availability of load but the results should give a good idea of the efficiency curve. The table on the next page shows various efficiency measurements.

Table 3.23 – Efficiency measurement with 50V input and varied current conditions

Input Power (W)	Output Power (W)	Total Power Lost (W)	Power Lost (%)	System Efficiency (%)
203	167	36	17.62%	82.38%
303	267	36	11.75%	88.25%
475	439	36	7.51%	92.49%
701	663	37	5.29%	94.71%
963	924	40	4.10%	95.90%
1128	1085	43	3.80%	96.20%
1304	1259	45	3.42%	96.58%
1466	1419	47	3.21%	96.79%
1617	1568	49	3.06%	96.94%
1850	1794	56	3.01%	96.99%
2120	2059	61	2.87%	97.13%
2390	2322	67	2.82%	97.18%
2612	2538	74	2.82%	97.18%
2885	2803	82	2.85%	97.15%
3157	3066	91	2.89%	97.11%
3432	3331	101	2.95%	97.05%
3646	3537	109	2.98%	97.02%
3922	3802	120	3.06%	96.94%
4199	4067	132	3.14%	96.86%
4270	4135	135	3.17%	96.83%
4555	4406	149	3.27%	96.73%
4828	4666	162	3.37%	96.63%
4944	4775	169	3.42%	96.58%
5209	5022	186	3.58%	96.42%
5491	5286	205	3.74%	96.26%
5782	5557	226	3.91%	96.09%

3.12 Comparison of Calculated and Experimental Efficiency

The next figure shows the efficiency lines of the calculations and the experimental results on the same plot.

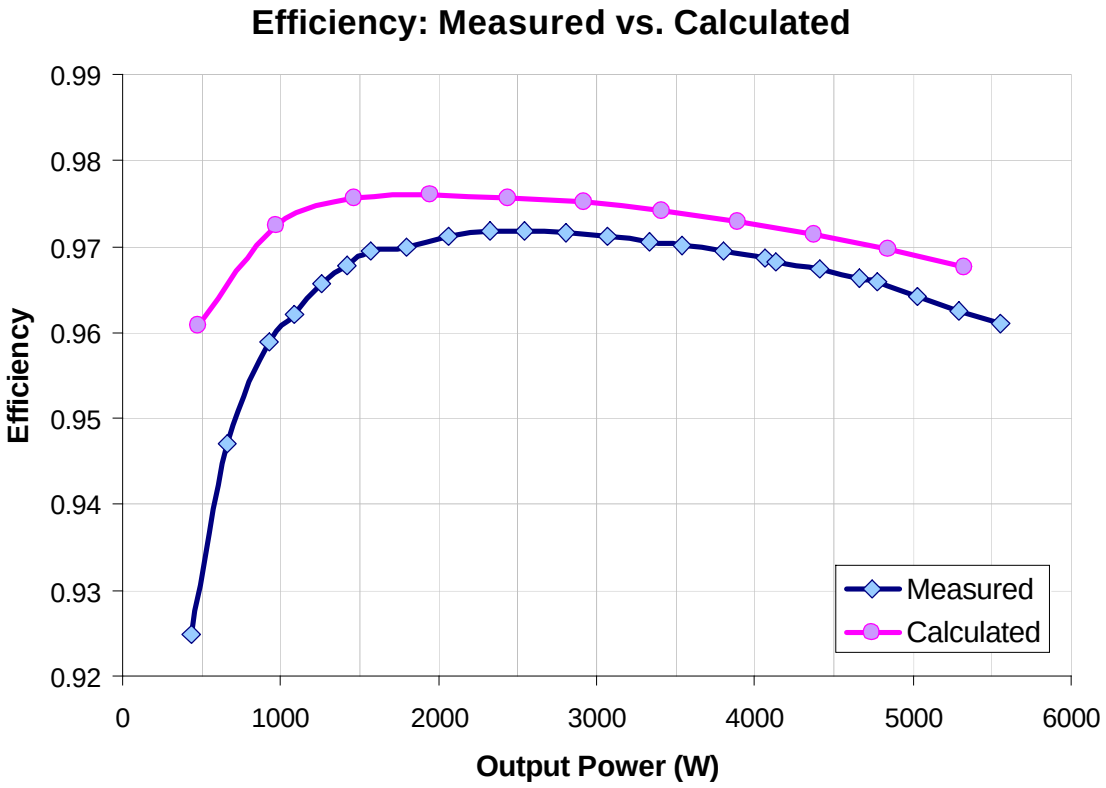

Figure 3.5 – V6 calculated and experimental efficiency curves

The efficiency estimates are fairly close but there are still some discrepancies. The difference at light to middle load conditions can most likely be attributed to lack of full-ZVS switching condition. The lack of full-ZVS switching condition creates additional switching losses, which are very difficult to characterize and estimate. This is due to the fact that the switching waveforms are not ideal in shape and are difficult to predict.

At higher power levels, the discrepancies in efficiency are current related. In particular, skin effect and termination losses are most likely significant. The contacts for high current components are not ideal and contribute a small resistance within the high current path. Despite the small resistance, the high current can create substantial power

losses. Since bus bars are required due to the high current input, the terminals between the bus bar, PCB, device, transformer, etc, cannot be avoided. Skin effect can greatly increase the resistance of power traces and connections.

Also, the experimental results show that the power loss under approximately 650W operation level is relatively constant. A substantial amount of loss contributed should be voltage dependent losses.

In order to improve the curve matching of the measured and calculated efficiencies, transformer-device contact, proximity, and skin effect losses can be considered. The parasitic losses are dependent on the layout, packaging, materials, etc and are difficult to measure and estimate. If the total parasitic contact/termination resistance and skin-effect resistance in the primary current path is considered to be 3mO, the efficiency curves should match much better at higher power levels. The figure below shows an efficiency curve with the added resistance.

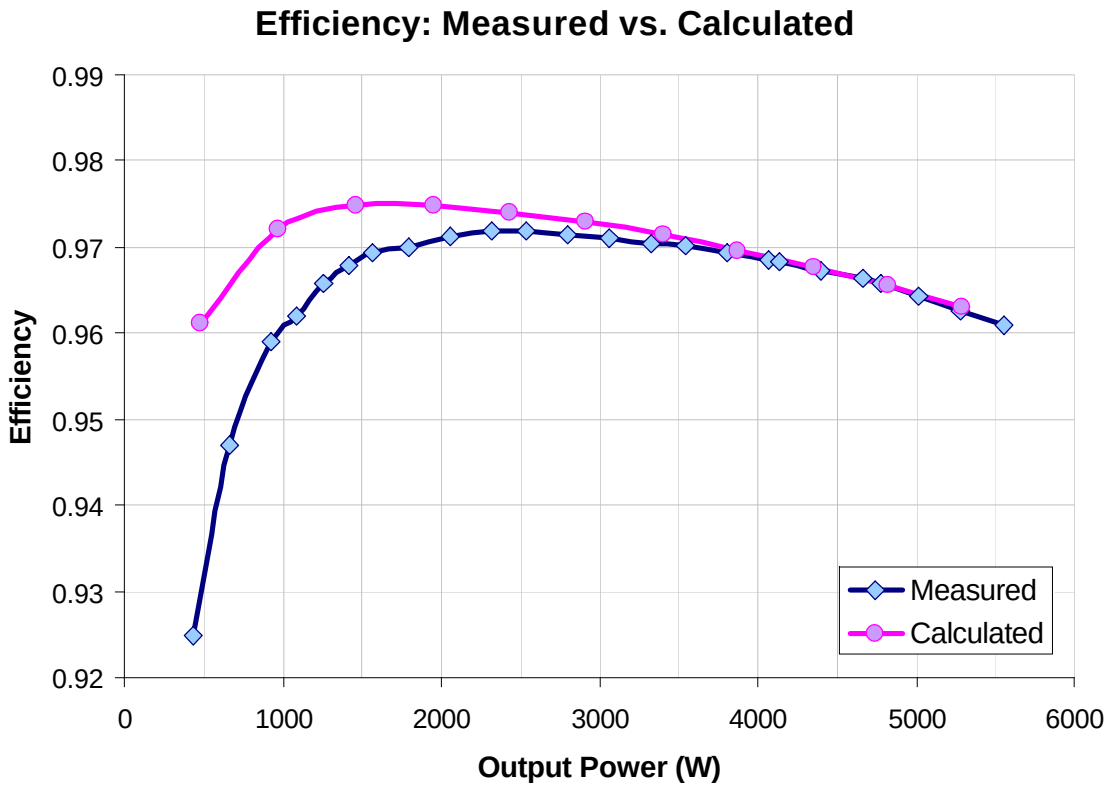

Figure 3.6 – V6 calculated and experimental efficiency curves including predicted parasitic resistance loss

Based on the experimental results and power loss models, the breakdown of losses can be analyzed. The losses within the system can be categorized and compared. Based on the analysis, the efficiency of the system can be improved and high efficiency may be obtained. The table below analyzes the approximate composition of losses at 1kW, 3kW, and 5kW power levels.

Table 3.24 – Loss composition at various power levels for baseline V6 converter

	Loss at 1kW (W)	% of Total Loss @ 1kW	Loss at 3kW (W)	% of Total Loss @ 3kW	Loss at 5kW (W)	% of Total Loss @ 5kW
MOSFET Conduction	1.94	4.91	18.38	22.02	56.90	30.31
Switching	6.49	16.43	25.846	30.97	49.85	26.55
Diode Conduction	4.25	10.75	12.825	15.37	23.06	12.28
Core	14.00	35.41	14.00	16.78	14.00	7.46
Winding	0.50	1.25	0.834	1.00	2.31	1.23
Parasitics	12.67	32.03	11.29	13.52	40.14	21.38
Total	39.84		83.16		186.27	

The following figure shows the approximate composition of system losses as based on the data from the table above.

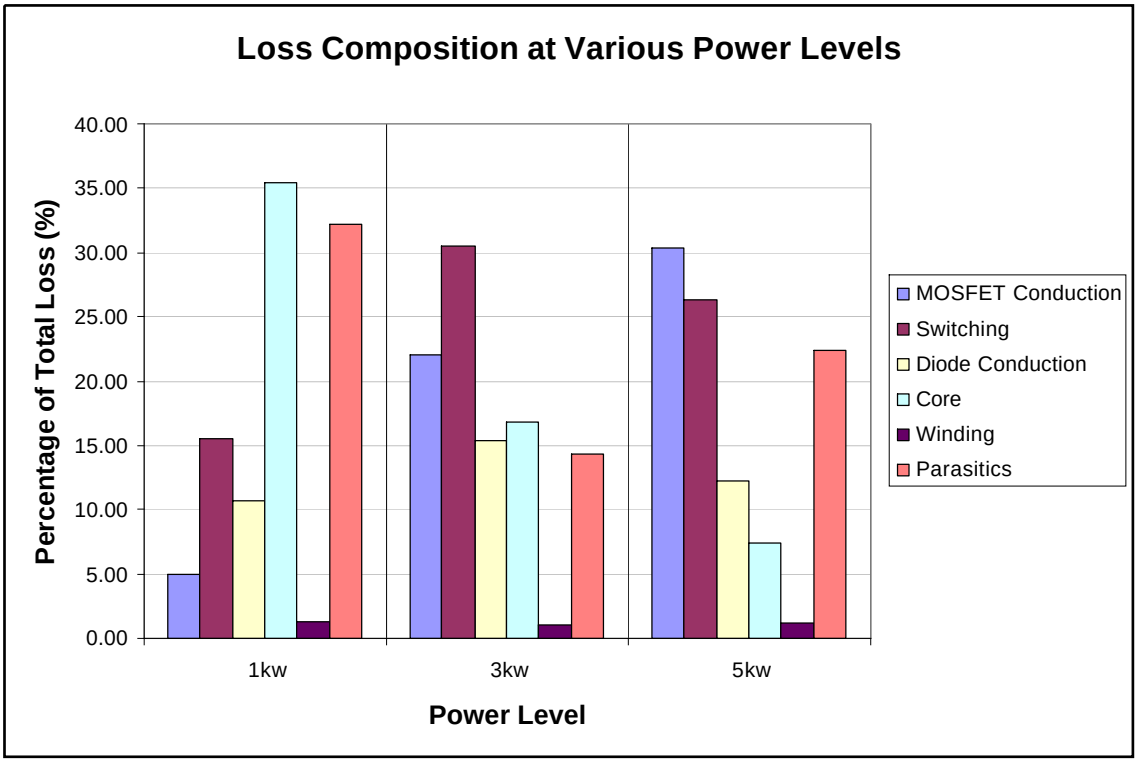

Figure 3.7 – Baseline V6 loss composition

The figure above shows that the parasitic losses and core losses are dominant at low power levels. Conduction and switching losses are dominant at middle power levels. At high power conditions, conduction, switching, and parasitics are dominant. The lower power parasitics should be due to incomplete soft switching conditions while high power parasitics are due to skin effect and contact losses.

3.13 V6 Efficiency Improvement

By analyzing system losses, components that contribute significant amounts of loss can be targeted and improved. After comparing the composition of losses, a new transformer design was selected in order to improve the system efficiency of the V6 converter. As shown in the previous section, a substantial amount of losses in the V6 is due to core loss and parasitics. Both core loss and parasitic losses can be reduced with better designed transformers.

Lower power efficiency suffers greatly due to core loss. The efficiency of the converter can be improved by designing an improved transformer which has reduced core loss. Increasing the primary turns allows for substantial reduction in core loss. The increase in primary turns reduces the peak flux density which reduces the transformer core loss. Based on previous calculations, the core loss at 50V input and 50 kHz switching is approximately 14W with two primary turns. The core loss can be reduced to approximately 4.5W with 3 primary turns. Under light load conditions, particularly under 1000W, the efficiency gain may be over 1%.

In addition to the decreased core loss, the leakage inductance can be increased in order to promote better soft switching characteristics at low power conditions. The increase in leakage inductance should reduce switching losses at low power and middle power conditions.

The new transformers also employ more copper and high frequency Litz wire. The additional turns actually increases the overall dc resistance of the transformer winding due to the increase in winding length. The use of additional copper helps offset the resistance gains due to additional length. The use of Litz wire helps reduce losses due to skin effect. The previous design utilized copper sheets, which offer less surface area compared to Litz wire.

Finally, the new design provides improved contacts for reduced contact/termination losses. The previous design used brass connections in between transformer terminal and the PCB. The new version utilizes direct transformer terminal contact to a copper block on the PCB.

In conclusion, the new transformer design offers several advantages over the previous design. The advantage should yield power savings over the entire output power range. The following parasitic losses should be reduced greatly with the new transformer losses.

- Core loss – The reduction in core loss should improve light load efficiency greatly.
- Switching loss due to lack of full-ZVS condition – Full ZVS condition is obtained at higher load so this should also help light load efficiency
- Copper loss - The use of Litz wire should reduce the increase in winding resistance caused by skin effect.
- Contact / Termination – The reduction in contact resistance should improve efficiency at high power levels.

The figure below shows the prototype transformer units connected to the V6 power-stage and rectifier boards.

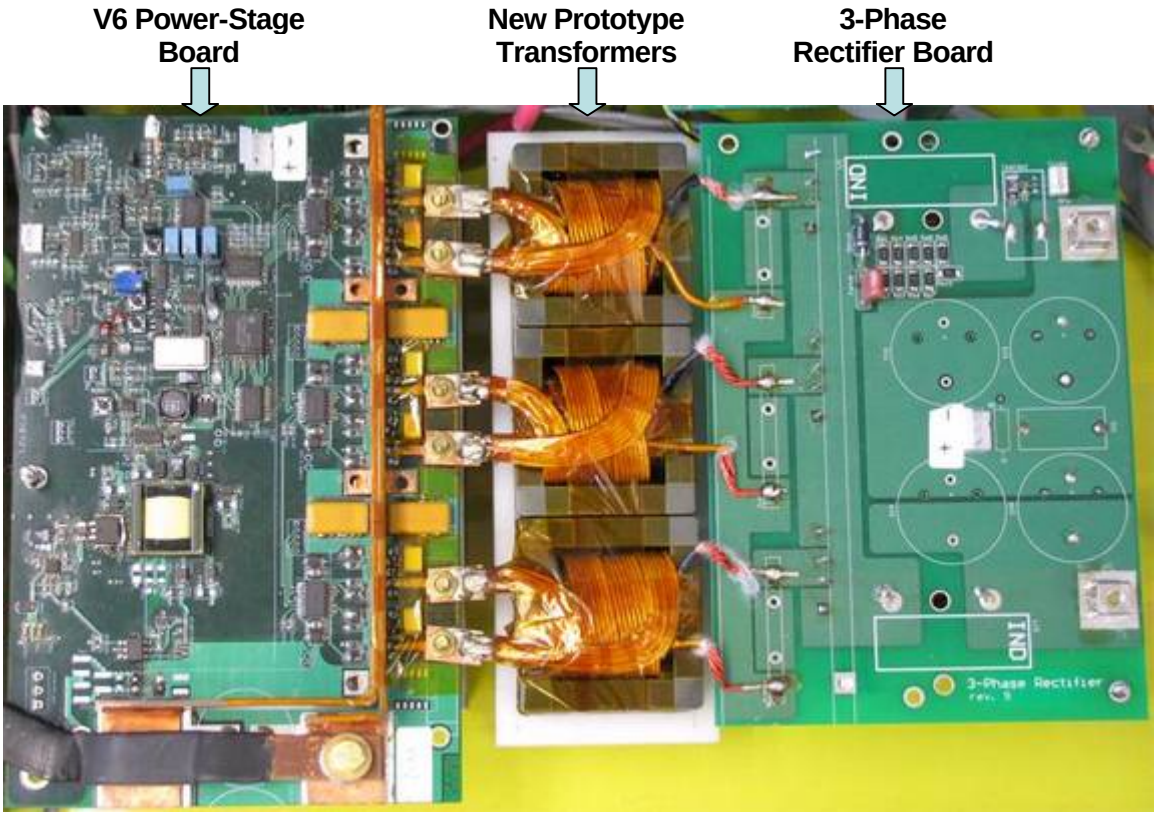

Figure 3.8 – V6 unit with new prototype transformers

3.14 Efficiency Prediction of V6 with New Transformers

The system efficiency of the V6 converter with new transformers can be calculated. Minor adjustments are made to the efficiency calculations in order to form a better model. The conduction loss will remain the same as before, simply including the pin to chip loss but no other additional parasitic resistances. The core loss was modified to 4.5W from 14W based on calculations from the previous section. The new transformer design utilizes a 3:13 turns ratio instead of 2:8. Therefore, the rectifier diode conduction loss has been reduced slightly in order to account for the slightly higher output voltage and, therefore, low output current. Finally, the transformer winding conduction loss was recalculated using new measured winding resistances. Due to the additional turns, the winding resistance of the new transformers is actually greater than the previous transformers despite having more copper area. Still, the savings from core loss is greater than the additional loss from transformer copper loss. The table below shows the predicted loss numbers.

Table 3.25 – Loss summary for new transformer V6 with 50V input and varied input current conditions

Input Power (W)	MOSFET Conduction Loss (W)	MOSFET Switching Loss (W)	Diode Loss (W)	Core Loss (W)	Snubber Loss (W)	Body Diode Cond. Loss (W)	XF Cond. Loss (W)	Cap. ESR Loss (W)
500	0.48	2.865	1.755	4.5	0.1	0.25	0.047	0.04
1000	1.94	6.495	3.926	4.5	0.2	0.50	0.189	0.17
1500	4.41	10.725	5.439	4.5	0.4	0.74	0.425	0.38
2000	7.92	15.405	7.506	4.5	0.7	0.99	0.756	0.67
2500	12.57	20.475	9.700	4.5	1	1.24	1.181	1.04
3000	18.38	25.846	11.848	4.5	0.6	1.49	1.700	1.50
3500	25.39	31.486	14.057	4.5	0.7	1.73	2.314	2.04
4000	33.98	37.396	16.490	4.5	0.8	1.98	3.023	2.67
4500	44.03	43.516	17.945	4.5	0.9	2.23	3.826	3.38
5000	56.90	49.846	20.362	4.5	1	2.48	4.723	4.17
5500	73.47	56.386	22.948	4.5	1.1	2.72	5.715	5.04

Based on the loss numbers in the figure above, the total system efficiency can be calculated as shown in the table below.

Table 3.26 – Efficiency calculations of V6 with new transformers

Input Current (A)	Input Power (W)	Total Power Lost (W)	Power Lost (%)	Estimated System Efficiency (%)
10	500	10.037	2.007	97.993
20	1000	17.912	1.791	98.209
30	1500	27.018	1.801	98.199
40	2000	38.448	1.922	98.078
50	2500	51.708	2.068	97.932
60	3000	65.858	2.195	97.805
70	3500	82.221	2.349	97.651
80	4000	100.831	2.521	97.479
90	4500	120.321	2.674	97.326
100	5000	143.977	2.880	97.120
110	5500	171.885	3.125	96.875

The reduction in core loss helps boost low power efficiency compared to the previous estimation. The high power efficiencies are fairly similar since core loss is voltage dependant and not current dependant. The new calculations predict peak efficiencies of greater than 98%.

3.15 V6 Efficiency Measurements with New Transformers

Prototype transformers were built to confirm that the discrepancies between the measured and calculated efficiencies were in fact due to parasitic losses. The old transformer turns ratio was equivalently 1:4 (2:8). The new transformer utilizes a slightly higher turns-ratio of 1:4.33 (3:13). The higher turns-ratio allows 400V output voltage to be maintained at full load condition. If a 3:12 turns-ratio was used, 400V output voltage could not be maintained at full load due to losses. The table below shows the efficiency values obtained during experimental testing.

Table 3.27 – V6 efficiency measurement with new transformers

P_{in} (W)	P_o (W)	P_{loss} (W)	Efficiency (%)
277.58	264.90	12.68	95.43
409.68	396.69	12.99	96.83
534.39	520.45	13.94	97.39
559.37	545.33	14.04	97.49
734.54	718.63	15.91	97.83
996.05	976.70	19.35	98.06
1128.31	1106.97	21.33	98.11
1518.58	1489.87	28.70	98.11
1907.69	1869.98	37.70	98.02
2618.93	2561.36	57.58	97.80
3421.44	3338.49	82.94	97.58
3783.15	3688.54	94.62	97.50
4074.35	3969.72	104.63	97.43
4429.72	4310.78	118.94	97.31
5023.47	4877.40	146.07	97.09
5381.00	5215.06	165.94	96.92
5721.21	5537.19	184.02	96.78

3.16 Analysis of V6 Efficiency with New Transformers

The figure below shows the efficiency of the V6 converter with new transformers compared to the efficiency measurements with the old transformers.

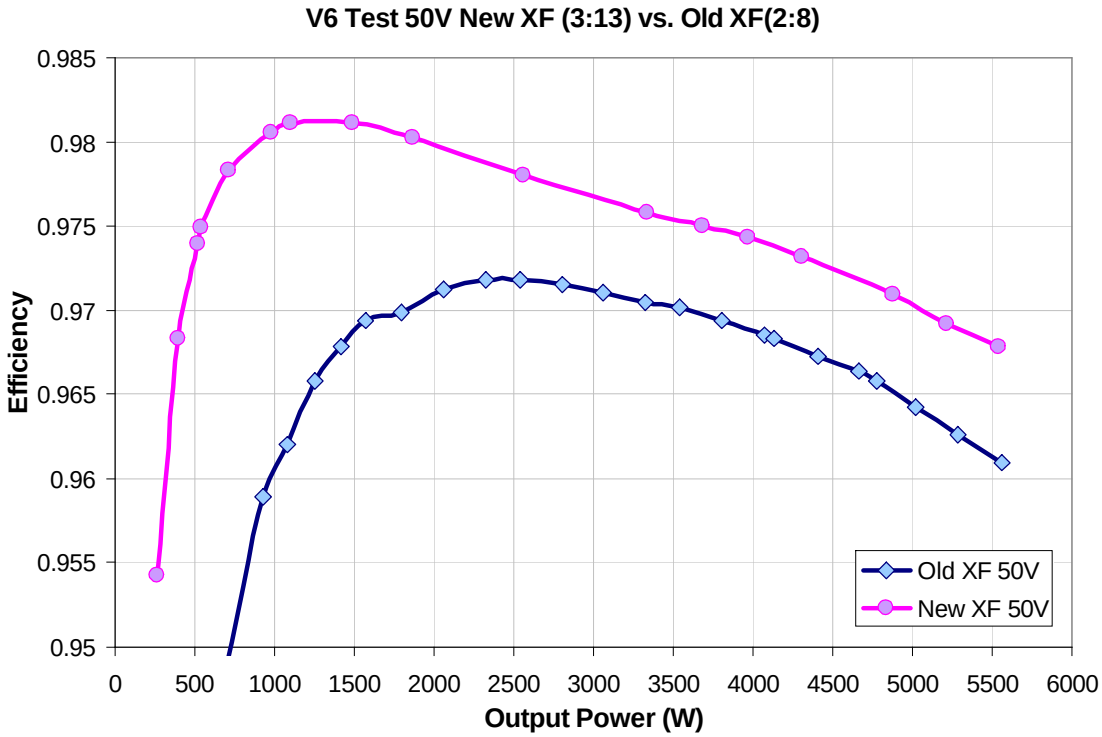

Figure 3.9 – V6 efficiency comparison with new transformer and old transformer

As the Figure 2.9 shows, the new transformers are able to greatly improve the efficiency of the V6 converter. The peak efficiency is now 98.1% and occurs at much lighter load. This implies that the parasitic losses at light load such as core loss and switching loss have been greatly reduced. Higher load efficiency is greater as well. The increase can be attributed to the reduction in contact resistance and reduction of skin effect related losses.

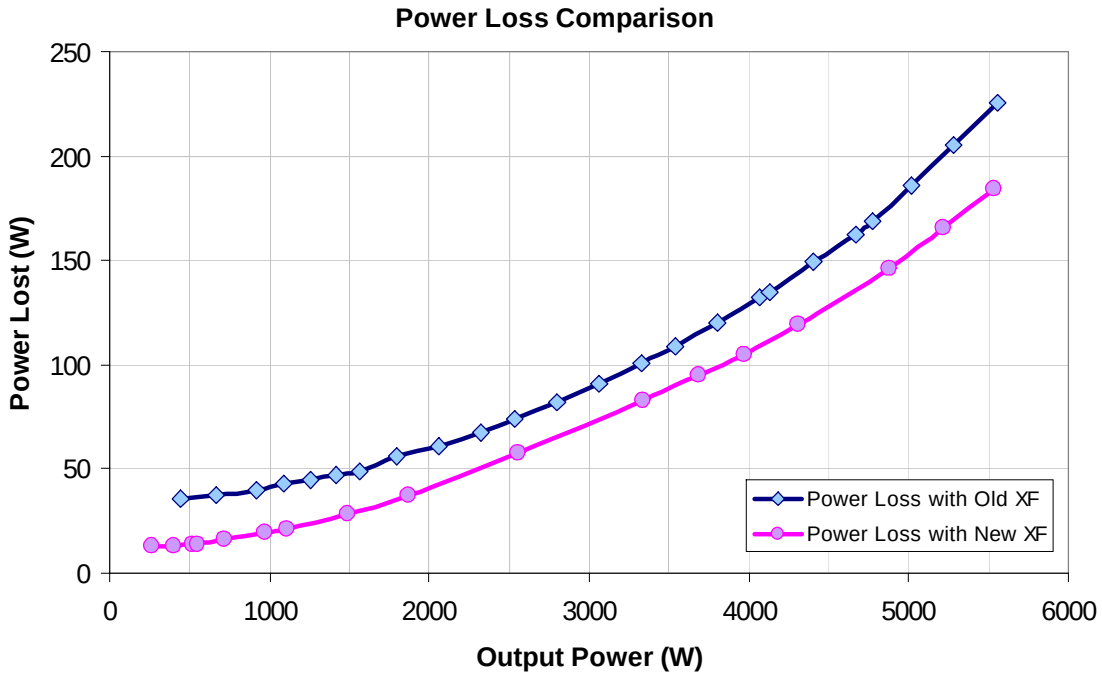

Figure 3.10 – V6 power loss comparison with new transformer and old transformer

The plot above shows the total system power loss comparison. Due to the scaling, it may be difficult to get the full feel of how much power is saved between the two systems. The figure below shows the approximate system power savings with the new transformers compared to the old transformers. The figure below gives a much better picture of how the power savings between the two systems scales with relation to output power.

The power loss difference is the least at middle power. At low power, the core loss and switching loss savings are significant. At middle power, the old transformers are able to provide proper ZVS condition as well but the parasitic conduction losses are not significant. Therefore, the power loss savings is the least during middle power. At high power, the loss difference is clearly increasing due to the parasitic conduction loss. The parasitic conduction losses could come from a variety of sources including transformer winding skin effect, winding proximity effects, transformer termination and contact.

The figure below shows the power savings growing rapidly as output power, and therefore output current, increases. Conduction loss grows exponentially as current increases. Despite the fact that the new transformers were measured to have greater

winding resistance, the new transformers are able to offer significant high power savings. This indicates some other sort of parasitic resistance such as skin effect resistance or contact/termination resistance was significant in the previous transformers. Therefore, minimization of parasitic losses such as these is critical for low voltage high current systems.

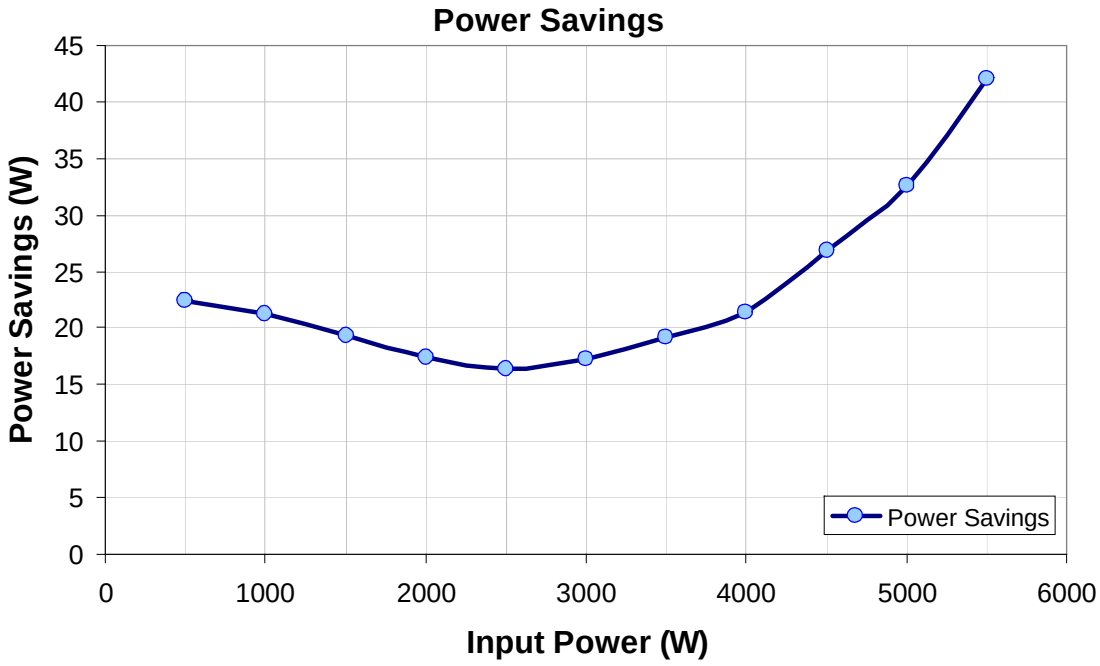

Figure 3.11 – V6 power savings due to new transformer design

The losses within the system can also be categorized for analysis. By viewing which losses are dominant, further efficiency improvements can be considered. The table below shows the power losses at 1kW, 3kW and 5kW conditions. The table also shows the percentage of the total loss that each loss source contributes. Primary sources of loss are considered individually while parasitics are grouped together. Once again, the parasitics are capacitor ESR, snubber loss, and body diode conduction loss.

Table 3.28 – Loss composition at various power levels with new transformers

	Loss at 1kW (W)	% of Total Loss @ 1kW	Loss at 3kW (W)	% of Total Loss @ 3kW	Loss at 5kW (W)	% of Total Loss @ 5kW
MOSFET Conduction	1.94	11.30	19.11	29.29	78.09	46.79
Switching	4.08	23.77	16.98	26.02	37.34	22.37
Diode Conduction	3.93	22.87	11.85	18.15	22.95	13.75
Core	4.00	23.30	4.00	6.13	4.00	2.40
Winding	0.19	1.10	1.70	2.61	5.72	3.42
Parasitics	3.03	17.66	11.62	17.81	18.81	11.27

The following figure displays the data above, graphically.

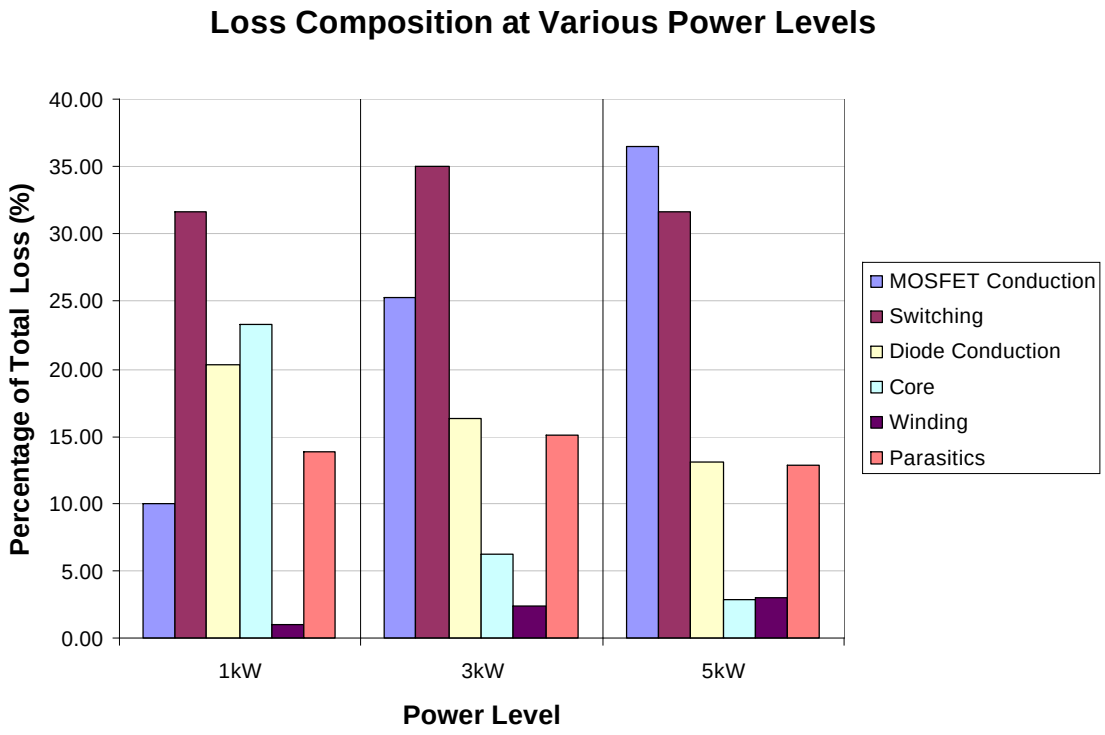

Figure 3.12 – New V6 power loss composition

As shown in the graph above, at light load conditions, switching loss, diode loss, and core loss are dominant factors. At middle power level, switching loss is still the most dominant source of loss. MOSFET conduction loss is the second most significant. At

high power conditions, MOSFET conduction loss grows to the greatest source of loss. Switching loss is the second largest contributor of losses. Compared to Figure 3.7, the parasitic and core losses have decreased substantially. Previously, core loss and parasitics were the most dominant factors at light load conditions and much more prevalent at higher power levels.

The predicted efficiency and measured efficiency with the new transformers may also be compared. The efficiency figures should be much closer with the elimination of parasitic losses. The figure below shows a comparison of the efficiency curves.

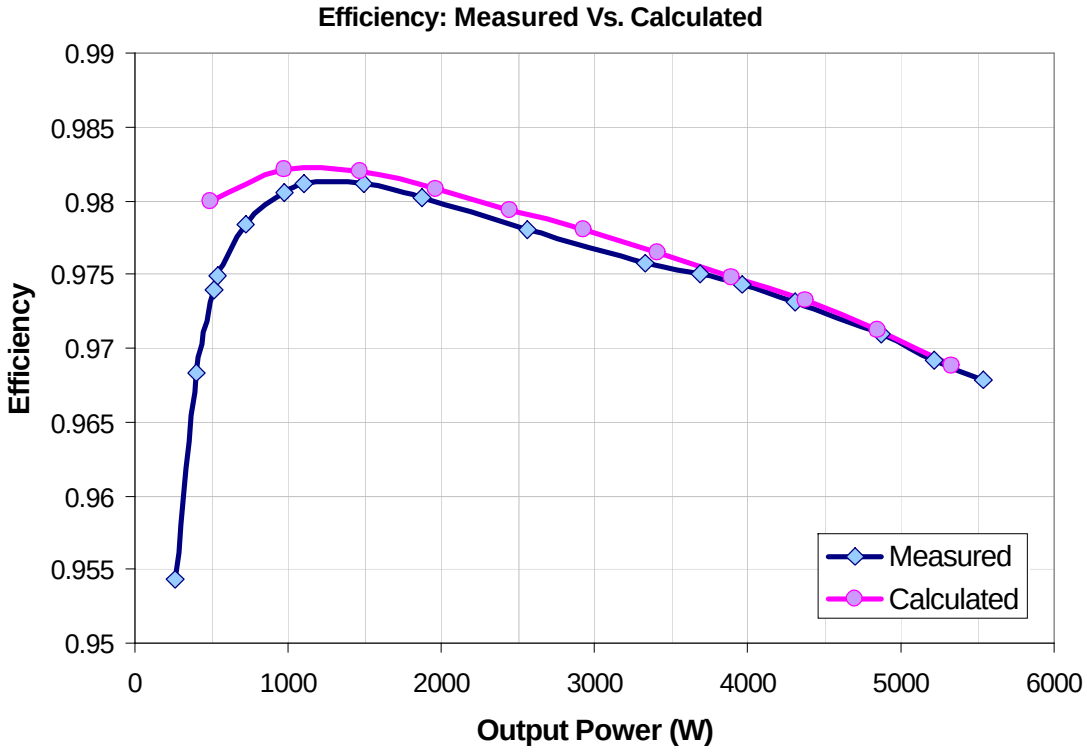

Figure 3.13 – Comparison of measured and calculated efficiencies with new transformers

As shown in the figure, the measured and calculated efficiencies are much closer with the new transformers. The new transformers are able to significantly reduce the parasitic losses. There are still some discrepancies between the measured and calculated efficiencies. Once again, the light load efficiency discrepancy can be attributed to the lack of full-ZVS condition at light load conditions. The new transformers help reduce the light load divergence greatly by increasing the leakage inductance. Better light load soft switching conditions improve the matching of the two curves. The slight discrepancies at

middle power level may be due to snubber losses, inaccurate temperature models, non-full ZVS condition, etc. The efficiency prediction and measurement with the old transformers had a significant offset. With the new transformers, the contact/termination and skin effect losses have been greatly reduced, therefore, significantly improving the efficiency curve matching at high power levels. Based on the above, it is clear that parasitic losses contribute a significant amount of losses in the system.

3.17 Summary of V6 Converter Loss and Efficiency

In this chapter, the losses in the V6 converter have been analyzed. Mathematical models were created in order to analyze and predict common sources of loss within the V6 converter. The primary sources of loss considered include the following:

- Primary side MOSFET conduction loss
- Primary side MOSFET switching loss
- Secondary side diode rectifier conduction loss
- Transformer core loss
- Transformer winding loss

In addition to primary sources of loss, some other parasitic loss sources were considered.

- Body diode conduction loss
- Capacitor ESR loss
- Secondary side rectifier snubber loss

Other parasitic losses are much more difficult to estimate and calculate. These losses include but are not limited to the following:

- Termination and contact losses
- Skin effect and proximity effect losses in the transformer
- Failure to achieve full soft switching condition for primary side MOSFETs
- Rectifier side diode reverse recovery effects
- Various thermal effects

The models and calculations were compared to experimental results. The original calculations and experimental results did not match well. The experimental results yielded a lower efficiency than the prediction. Various other parasitic losses caused the offset in the results. In particular, transformer core loss, termination and contact losses, skin effect losses, and non-full ZVS switching condition were suspected as causes for significant amounts of loss. In addition, running the system and observing hot spots helps identify components which contribute loss.

The composition of system losses were analyzed in order to find dominant sources of loss. Parasitic and core losses were found to be very significant at most power levels. Many of the parasitic losses as well as core loss could be reduced with better

designed transformers. Therefore, new prototype transformers were constructed to help reduce the losses within the V6 converter. With the new transformers, the efficiency improved greatly. The new transformers significantly reduce the parasitic and core losses within the system. With the new transformers, the system saved anywhere from 15W to 40W depending on the power level. The peak efficiency moved up to 98% from the previous value of 97.2%. The peak efficiency also occurs at much lower power. The calculated efficiency for the new system and the experimental data match well except at low power conditions. Low power conditions contain switching losses due to loss of soft switching, which are particularly difficult to characterize.

As mentioned previously, the power savings from the new transformers are significant. At low and middle power levels, the power savings are approximately 20W but at higher power levels, the power savings grow to up to 45W. Experimental results show that parasitic losses can comprise a significant percentage of total system loss. In particular, parasitic losses dependent on current are very dangerous for low voltage high current systems. For example, capacitor ESR, skin effect, contacts and termination, etc are key sources of parasitic conduction losses. Therefore, parasitic losses should carefully be considered for high current systems.

4 CONSIDERATIONS FOR HIGHER CURRENT LEVELS

In the previous chapter, a power stage design with 100A peak input current was analyzed. Care must be taken in designing the power stage in order to obtain proper operation as well as system reliability. If the power stage is not properly designed, the system will suffer from excessive losses which will severely reduce system reliability. Power stages with even greater currents requirements have similar design considerations but certain areas may need further consideration. This section will discuss power stage considerations for a system expected to sustain up to 400A currents.

Due to higher currents, multiphase design and parallel devices are required. Even for a multiphase full-bridge converter, parallel devices will be required. If through-hole devices must be placed in parallel, excessive parasitics will introduced. Therefore, a surface mount device such as the IRFS3207 with D^2PAK package is desirable. The IRFS3207 has very low R_{DS-ON} as well with 3.6mO. The use of MOSFETs in the low-voltage high-current system allows for paralleling of devices.

If utilizing parallel surface mount devices, the three-phase half-bridge structure may be used. The three-phase asymmetrical pulse width modulation half-bridge converter was discussed in a previous section. The primary disadvantage was the need to parallel devices compared to the three-phase full-bridge converter. If both converters require parallel devices, the half-bridge converter may be utilized instead in order to allow more freedom in device count. Either three-phase half-bridge of three-phase full-bridge topology would be acceptable when utilizing parallel surface mount devices. Therefore, this section will consider the three-phase half-bridge topology with Y-Y transformer connection and bridge rectifier as shown below. The half-bridge structure is simply half of a full-bridge structure. Therefore, if desired, the topology below could easily be converted into a full-bridge structure.

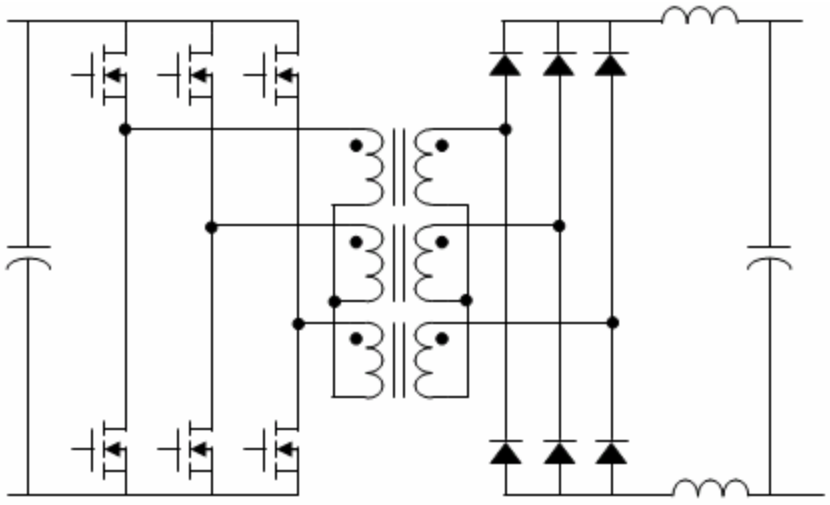

Figure 4.1 – Three-phase half-bridge converter with Y-Y transformer

Instead of paralleling devices, modules may also be considered depending on cost and availability. Well designed modules are able to reduce parasitics compared to parallel devices. Poorly designed modules may yield little in the form of parasitic reduction for the system.

Modules provide additional mechanical advantages. First, modules are designed to be mounted on heat sinks. Therefore, thermal management is simplified greatly due to the package. In addition, high current modules are typically designed such that bus bars may be connected easily. Therefore, bus bar design for a module may be simpler compared to other surface mount or through-hole devices.

Unfortunately, the cost of the modules is a significant issue as modules tend to be expensive. In addition, a small or partial failure in the module renders it unusable. Therefore, the entire module must be replaced. Parallel devices allows for individual components to be replaced. Thus, parallel devices are able to provide good performance without extravagant costs. Thermal issues may be addressed with a clad board as described in the next section.

4.1 Mechanical, Packaging, and Thermal Considerations

As current levels and therefore power levels increase, the thermal considerations become critical. For example, if a 50V, 400A converter is considered, the power level is 20kW. If the 20kW converter operates at 97% efficiency, the 3% of efficiency loss generates 600W of power loss. That 600W is dissipated as heat and suitable cooling is required in order to prevent system failure. Thermal considerations become very significant for high power systems.

Thermal management can be classified into two categories. The two categories are passive cooling and active cooling. The former requires no power for cooling while the latter consumes power for cooling.

Passive cooling involves allowing the device to dissipate heat into the ambient air. A heat sink may be attached to the device in order to increase heat dissipating abilities. The heat sink is able to provide greater surface area for the heat to dissipate. Another option for certain device packages is to provide large copper planes on the PCB. After the device is soldered to the PCB, the device can dissipate heat into the large copper plane in the PCB. Unfortunately, this style cooling is limited by package and it is not able to dissipate significant amounts of heat.

Active cooling requires some sort of power for operation. For example, fans, which circulate air, or water cooled heat sinks are considered active cooling. Active cooling is able to provide superior cooling performance compared to passive cooling. Of course, active cooling consumes power as the trade off. In high current and high power systems, active cooling is more likely required.

A combination of heat sink and fan is economical for high power systems. The heat sink is able to increase surface area for better heat dissipation while the fan circulates air to carry heat away from the heat sink. The V6 converter in the previous section utilizes a heat sink and fan combination. The fan is only required at higher power levels. Larger heat sinks and fans with greater flow can be used to increase cooling. The trade off is size, weight, power consumption, and system cost.

Another potential way to improve cooling performance is the use of clad boards. If a surface mount device is utilized, clad boards can be used to provide additional

cooling for the devices. Clad boards have an aluminum substrate attached to the bottom of the PCB for cooling. A heat sink can easily be attached to the board for significant cooling. A cross-section of a clad board looks as follows.

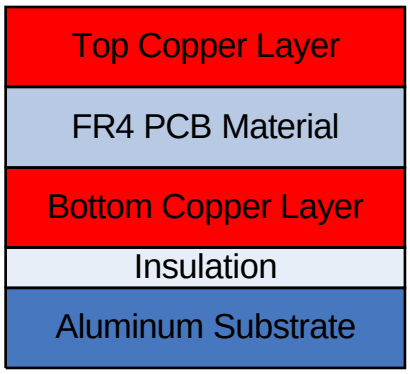

Figure 4.2 – Cross-section of aluminum clad board

Once again, the clad board is useful when considering surface mount devices. If non-surface mount devices are used, then the device may utilize its own heat sink and a clad board is not necessary. The V6 converter's devices are through-hole and are therefore able to utilize a heat sink directly. The 400A half-bridge converter utilizes surface mount (D^2Pak) devices for parallel operation. Utilizing a clad board is critical in order to dissipate heat and protect the devices as well as ensure reliability.

4.2 Bus Bar Configuration

Just as the V6 converter, any low voltage high current system should utilize a bus bar to deliver current. The three-phase half-bridge converter requires an input bus bar as well as three output bus bars, one for each output phase. The significant number of bus bars greatly complicates layout and bus bar design. In addition, the paralleling of so many devices complicates the design as well. First, the board is effectively divided into three sections. One section for each output phase. Next, each output phase section is separated into three sections. The separation into three sections is for several reasons. The first is for better current distribution. If too many devices are put next to each other, having effective current distribution is very difficult. Parasitic resistance and inductance could cause significant problems. Another advantage is that the current carrying density requirement of the PCB copper is reduced as it is separated into three parallel sections. The PCB layout is organized as follows:

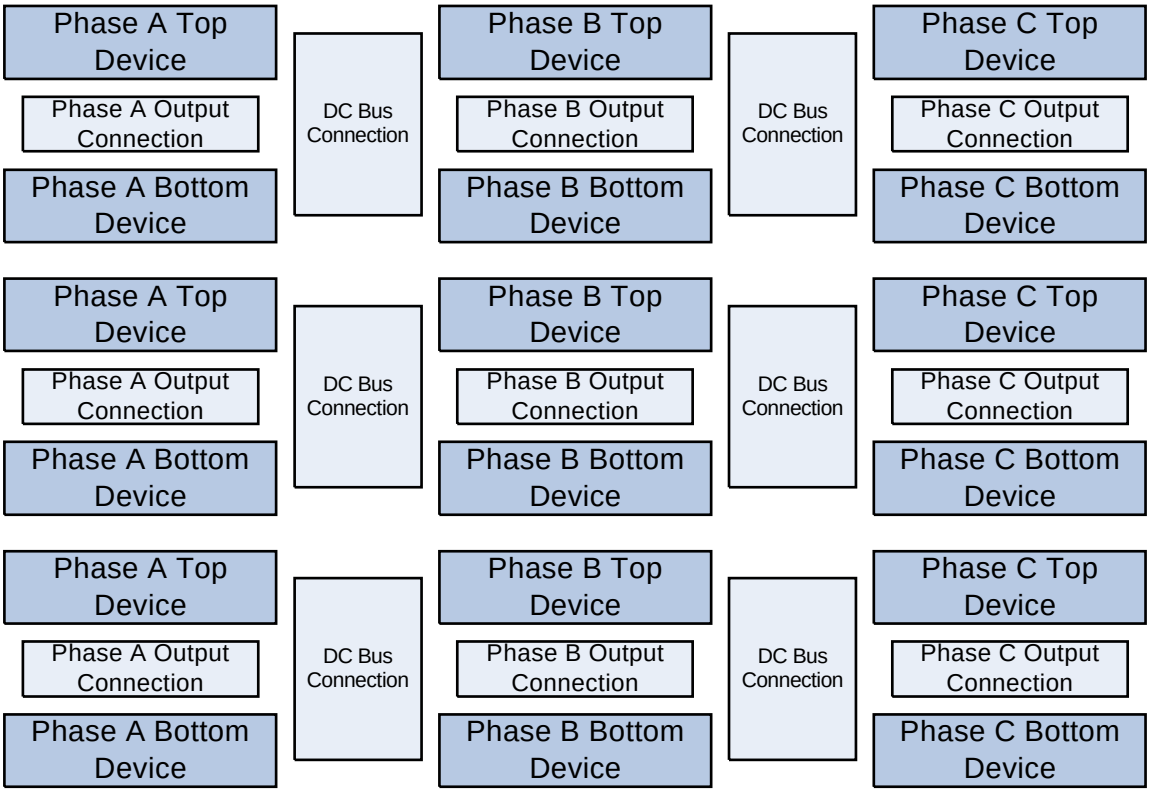

Figure 4.3 – Half-bridge converter layout structure

Each ‘device’ in the figure above is actually 4 MOSFETs in parallel. Therefore, instead of directly placing 12 devices next to each other, 3 sets of 4 devices are placed next to each other. Based on the PCB layout, the input and output bus bars are configured in the manner below.

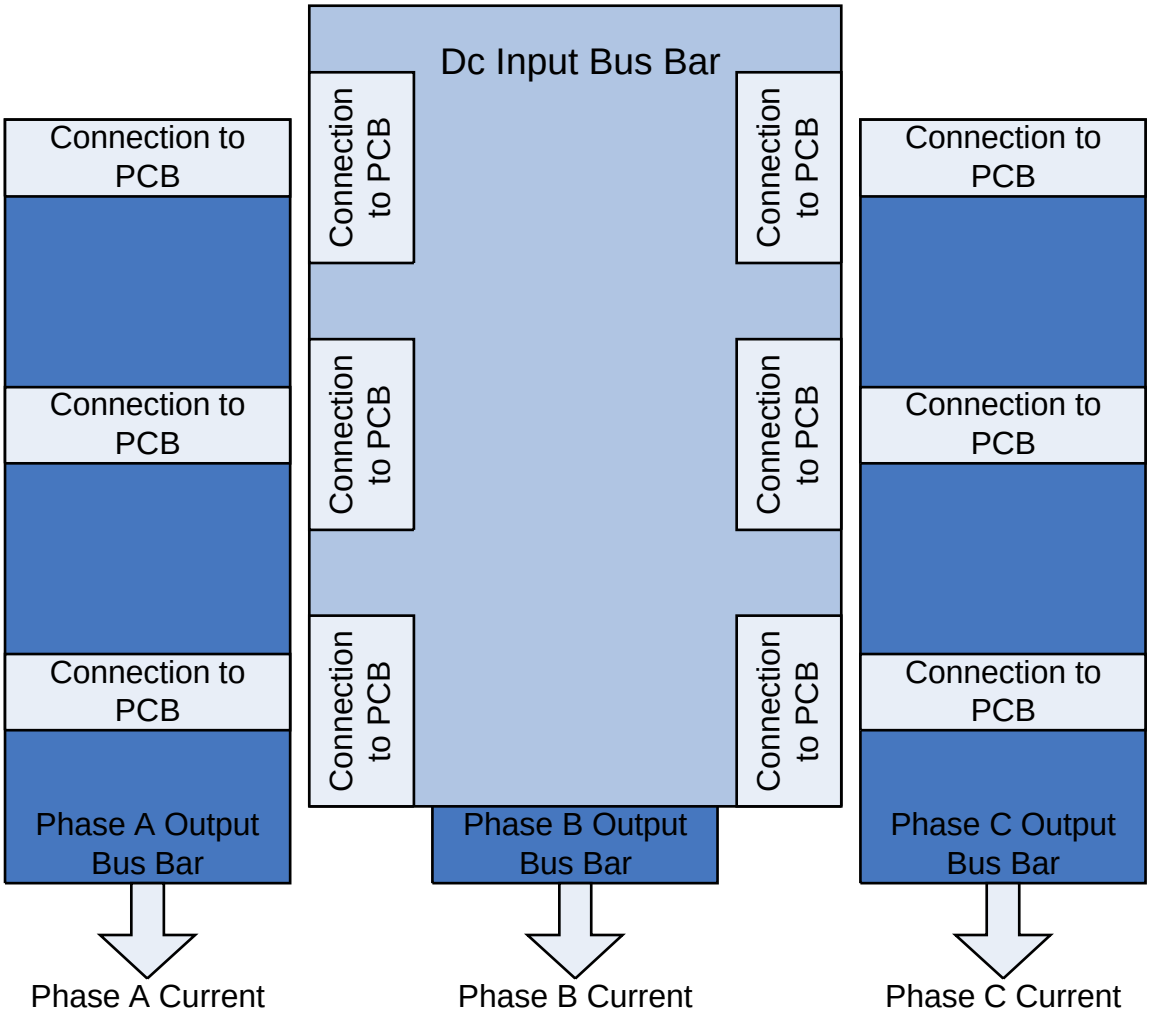

Figure 4.4 – Half-bridge converter bus bar structure

As shown in the figure above, each matching phase output connection is connected the corresponding bus bar. The dc bus bar goes above the phase B output bus bar and connects to the sides. The dc positive and dc negative bus bars are placed on top of each other to reduce the parasitic inductance. The positive and negative PCB

connections are also next to each other. This configuration allows the dc bus bars and ac bus bars to be connected very close to the devices. This design also allows the input power and output power to be on separate sides. Having the input and output connections on opposite sides is typically desirable for packaging. The following figure shows the power stage board attached to a heat sink. In addition, the dc and ac bus bars are in place. The gate drive board and DSP board are not present.

Figure 4.5 – Picture of half-bridge converter bus bar configuration

4.3 Summary for Higher Current Levels

For high current systems, standard sources of loss apply. Conduction losses and switching losses can be significant. Conduction loss is an obvious source of loss due to the high current nature of the system. As mentioned previously, conduction loss can be reduced by selecting low $R_{DS\text{-}ON}$ devices. Conduction loss can be further reduced by paralleling many devices. MOSFETs allow for parallel operation due to their positive temperature coefficient. Multiple phases and parallel devices may be used together in order to achieve greater reduction of conduction losses.

Switching loss is another key source of loss. When paralleling many devices, the switching loss can become greater than the conduction losses. Switching loss is dependent on both gate resistance and frequency. These variables can be modified in order to reduce switching loss. If faster switching times are utilized in order to reduce switching losses, noise issues may arise.

In addition to the primary sources of loss, parasitic losses can be prevalent. Losses due to the MOSFET body diode may be significant. The diode reverse recovery loss can be very severe depending on the converter topology. The reverse recovery can be reduced by modifying the switching times. In addition, the body diode conduction may create significant amounts of loss as well.

Capacitor ESR can also contribute significant problems for the system. The capacitors can produce a significant amount of loss due to the high currents. In addition, the capacitors may become a liability if they sustain significant power losses. The capacitors become very likely to fail if they suffer high power losses and therefore, high temperatures. Other typical parasitics are of concern as well. Bus bars should be sized properly in order to minimize low frequency conduction losses. Contacts and termination should be carefully considered as well.

When expanding to higher current levels, many of the same concerns still exist as the V6 converter. Conduction loss is a primary concern due to the high current levels. In order to accommodate the high currents, multiple phases and parallel devices are required. When considering parallel devices, a number of mechanical issues arise. The package of the device can significantly impact the parasitics of the system. Through-hole

devices are not ideal for parallel operation as they are likely to introduce parasitics. Surface mount devices are desirable for parallel operation as they may be placed very close to each other. Modules are the most favorable as they have the potential to introduce the least amounts of parasitics. Unfortunately, modules have the highest cost. In addition, the device package also affects the following mechanical issues:

- Bus bar
- Layout
- Packaging
- Thermal management

Bus bar design is critical for minimization of parasitic resistances and inductances. Layout should also minimize parasitic resistances and inductances as well. The layout must also accommodate the bus bar. Therefore, the design of the bus bar and layout should be completed while considering the other. Packaging and thermal management both affect each other. Cooling is clearly important due to the very high power levels and potential for losses. Packaging affects cooling and cooling affects the packaging. Therefore, the two should be considered together. If considering surface mount devices, a clad board can be considered for thermal management. The system should be designed while considering all of the above.

5 CONCLUSION AND FUTURE RESEARCH DIRECTION

The objective of this thesis is to consider issues regarding high-efficiency low-voltage high-current power stages. Low-voltage high-current power stages are suitable for many applications including renewable energy, distributed power, etc. For energy applications, efficiency and reliability are critical. Therefore, loss analysis should be utilized in order to improve system efficiency and reliability. In order to obtain high efficiency, conduction losses, switching losses, losses due to other sources and parasitics, bus bar, layout, and thermal management should all be carefully considered.

Conduction losses are of great concern for high current systems. For low-voltage high-current systems, the majority of losses at high power levels can be attributed to conduction losses. In order to reduce conduction losses, better devices, parallel devices, and multiple phases may be utilized. MOSFETs may be used in parallel due to the positive temperature coefficient. A combination of parallel devices and multiple phases is desirable for very high current systems. When considering parallel devices, the device package creates a significant impact. Through-hole devices may create significant parasitics while surface mount devices may not suffer as heavily from parasitics. Modules would be the most ideal for parasitic reduction but the most costly.

Switching losses are another primary source of losses. Switching losses may be reduced by obtaining soft-switching conditions for devices. Soft-switching may be obtained by topology or control scheme. Auxiliary circuits may also be used to obtain soft-switching conditions for some converters.

Other sources such as magnetics and parasitics may contribute additional losses. Magnetics, MOSFET body diode, parasitic inductance, parasitic capacitance, parasitic resistance, etc may all contribute further losses to the system.

Bus bars and PCB layout should be carefully considered in order to reduce parasitic resistance and inductance. Bus bars are essential for the high current applications as even the minor resistance of copper may contribute conduction loss. Layout should be optimized in order to accommodate the bus bar and reduce parasitics.

For thermal management, several options exist such as heat sinks, fans, water cooling, etc. Through-hole devices are typically designed to be mounted on heat sinks. Surface mount devices can be difficult to cool effectively due to the package. Many

surface mount devices are designed to dissipate heat into the PCB. Clad boards are designed to have heat sinks attached to one side. This greatly increases the heat dissipation capabilities of the PCB. With a combination of heat sink and fan, the heat dissipation capabilities may be greatly improved.

In this thesis, detailed analysis was provided for a three-phase six-leg phase-shift modulated full-bridge converter, called the V6. The V6 converter may see inputs currents up to 120A. The V6 converter is desirable for energy applications as it is able to achieve very high efficiencies and high conversion ratios. The baseline V6 converter is able to achieve 97.2% peak efficiency.

In order to further improve system efficiency, system losses were analyzed. Based on the loss analysis, it was determined that new transformers would be able to provide significant power savings. With new transformers, the V6 converter is able to achieve a peak efficiency of approximately 98.1%. The peak power savings due to the new transformers is approximately 40W. At low power, the new transformers are able to offer significant efficiency improvement due to core loss and soft switching over a wider range. At high power levels, the new transformers improve efficiency by reducing skin effect and contact losses.

Careful design with loss, mechanical, and thermal considerations in mind is critical in order to achieve high efficiency. Loss analysis may be used in order to further improve efficiency for a system. By analyzing losses, the system designer may see where efficiency improvements are possible. In this thesis, several items have been covered.

- Discussion of considerations for high-efficiency low-voltage high-current power stages.
- Loss analysis for the V6 converter was completed.
- Based on loss analysis, new transformers were designed to reduce core losses and various parasitic losses.
- Efficiency of the V6 converter was improved to 98% peak.
- Considerations for systems handling over 400A have been discussed

5.1 Future Research Direction

The research presented in this thesis analyzes various considerations for low-voltage high-current system. Discussion included sources of loss for low-voltage high-current systems as well as introducing other concerns such as layout, mechanical factors, thermal, etc. The research presented could be expanded in many directions.

- Further detailed parasitic loss analysis for the V6 converter. While some parasitics were addressed, many other sources of parasitics exist which can be modeled or measured.
- Further efficiency improvement potential for the V6 converter exists. In addition, the effects of different input and output conditions may be analyzed.
- Many low-voltage high-current converter topologies exist. Analysis is possible in order to compare differences and similarities between various converter topologies.
- Detailed loss and efficiency analysis of the three-phase half-bridge converter discussed in this thesis.
- Analysis for different modulation and control schemes.

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