Processing and Properties of Die-attachment on Copper Surface by Low-temperature Sintering of Nanosilver Paste

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Abstract

As the first level interconnection in electronic packages, chip attachment plays a key role in the total packaging process. Sintered nanosilver paste may be used as a lead-free alternative to solder for die-attachment at sintering temperature below 300 °C without applying any pressure. Typically, the substrate, such as direct bond copper (DBC) substrates, has surface metallization such as silver or gold to protect the copper surface from oxidation during the sintering process. This study focused on developing techniques for die-attachment on pure copper surface by low-temperature sintering of nanosilver paste. One of the difficulties lies in the need for oxygen to burn off the organics in the paste during sintering. However, the copper surface would oxidize, preventing the formation of a strong bond between sintered silver and copper substrate.

Two approaches were investigated to develop a feasible technique for attachment. The first approach was to reduce air pressure as a means of varying the oxygen partial pressure and the second approach was to introduce inert gas to control the sintering atmosphere. For the first method, die-shear tests showed that increasing the oxygen partial pressure (P_{O2}) from 0.04 atm to 0.14 atm caused the bonding strength to increase but eventually decline at higher partial pressure. Scanning electron microscopy (SEM) imaging and energy dispersive spectroscopy (EDS) analysis showed that there was insufficient oxygen for complete organics burnout at low P_{O2} condition, while the copper surface was heavily oxidized at high P_{O2} levels, thus preventing strong bonding. A maximum bonding strength of about average 8 MPa was attained at about P_{O2} = 0.08 atm. With the second method, the die-shear strength showed a significant increase to about 24 MPa by adjusting the oxygen exposure temperature and time during sintering.

The processing conditions necessary for bonding large-area chips (6 mm × 6 mm) directly on pure copper surface by sintering nanosilver paste was also investigated. A double-print process with an applied sintering pressure of less than 5 MPa was developed. Die-shear test of the attached chips showed an average bonding strength of over 40 MPa at applied pressure of

3 MPa and over 77 MPa under 12 MPa sintering pressure. SEM imaging of the failure surface showed a much denser microstructure of sintered silver layer when pressure was applied. X-ray imaging showed a bond layer almost free of voids. Because the samples were sintered in air, the DBC surface showed some oxidation. Wirebondability test of the oxidized surface was performed with 250 μm-diameter aluminum wires wedge-bonded at different locations on the oxidized surface. Pull test results of the bonded wires showed a minimum pull-strength of 400 gram-force, exceeding the minimum of 100-gf required by the IPC-TM-650 test standard.

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Chapter 1

Introduction

Electronic packaging not only provides electrical connection or isolation, but also mechanical support, thermal cooling, and the physical protection for power electronics components. The packaging technology is as important as the electrical components and circuit layout for the total performance of single-chip or multi-chip module [1]. Over the past twenty years, there have been tremendous breakthroughs in silicon (Si) technology for semiconductors. High-frequency synthesis and miniaturization in physical size lead to much denser devices and a wider field of applications. It keeps pushing the limits of existing electronic packaging technology [2]. More and more demands from electronic technologies surged from sections such as automotive [3] and aerospace [4] industries. Their requirements are faster, more functions and the ability of withstanding extreme conditions.

Generally, overall performance of a power module depends on electrical, thermal and mechanical characteristics of packaging materials. The schematic of a simplified device packaging structure is shown in Figure 1.1. A typical power semiconductor module usually contains seven parts as follows:

1. Power semiconductor chips (die) -- the core of the module, such as Si devices;
2. Multilayer substrates -- for circuits connection and insulation, such as direct-bond-copper (DBC), direct-bond-aluminum (DBA), etc.;
3. Die-attach materials -- for bonding and mechanical connections between the chips and substrate, such as solder alloys and electrical conductive epoxies;
4. Power interconnections -- for the electrical interconnection between chips and substrates, such as aluminum or gold wire bonding;
5. Encapsulate materials -- dielectric materials for sealing the whole packaging, such as silicone gel;
6. Heat sink -- for the cooling of the whole module, such as copper or aluminum metal block;
7. Plastic case and cover – thermoset and thermoplastic materials.

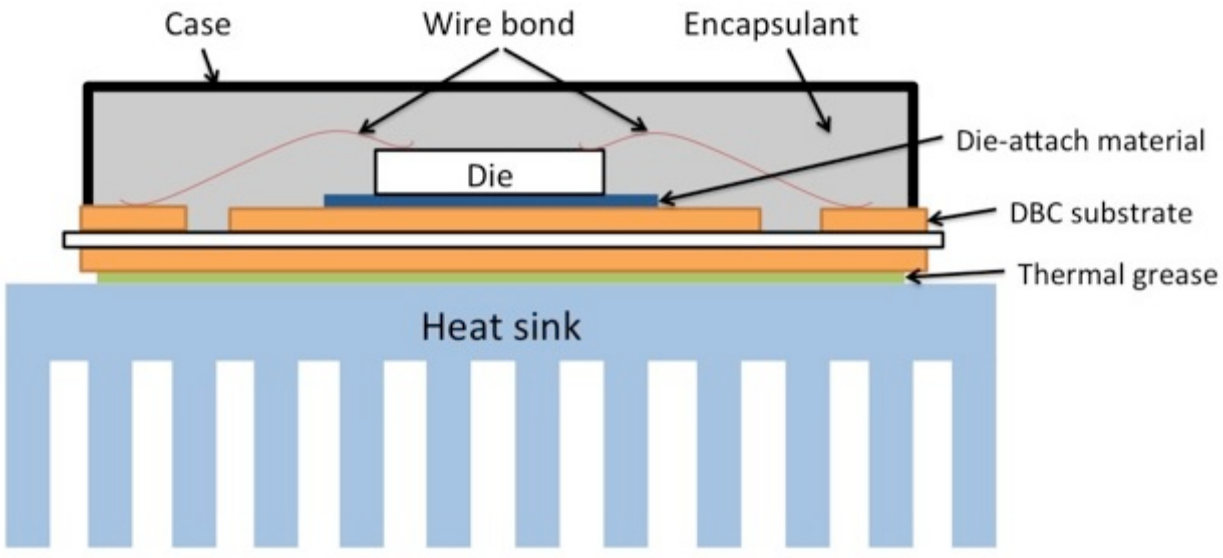


Figure 1.1 Schematic layout of a simplified package

Designing electronics packages involves considerations from different aspects of materials processing and reliability under various working environments. In order to keep pace with the development of semiconductor devices and improve the performance and reliability of the module, deeper understandings of the materials for packaging are important.

1.1 Chip-level packaging: die-attachment

Semiconductor chips are attached to substrates using different kinds of die-attach materials. Depending on the configuration of the attachment, the die-attach material may be electrically conducting or insulating. However, in either case, high thermal conductivity of the die-attach layer is preferred for heat dissipation generated from the working device [5]. With the development of wide band gap semiconductor materials such as SiC or GaN, devices made from these materials usually have high current density and high working temperature [6, 7]. The heat dissipation ability of die-attach layer is becoming more critical. For the conductive epoxies, they are made of polymers mixing with conducting fillers. Cured polymers epoxy layer usually have comparative lower thermal conductivity comparing to that of an metal alloy layer of interconnection, such as solder alloys or sintered silver [8]. In this section, a comparison of current soldering reflow technologies and the emerging silver sintering technologies is presented. After the comparison, a new type of die-attach material - nanosilver paste is introduced.

1.1.1 Solder reflow vs. sintering of silver

(a) Solder reflow

Solders are eutectic or off-eutectic alloys that contain two or more kinds of metals. The melting point of the alloy can be considerably lower than the melting points of all the individual pure metals forming the alloy. This makes it possible for solder alloys to be used as die-attach materials. A die-attach solder can be either a solder paste suitable for the stencil or screen printing, or a solder preform (sheet). For the solder reflow process of die-attachment, the solder is placed between the chip and substrate. Heat is applied to melt the solder alloy. During the melting stage, the molten solder can dissolve a portion of metals from both the chip and substrate surfaces. When the whole assembly cools down, a solder joint is formed.

For decades, the most commonly used solder alloy is eutectic lead-tin alloy (63Sn-37Pb). The reason for its widespread use is its combination of high ductility and acceptable thermal conductivity for most applications [9]. It is regarded to be the standard by which all other die-attach materials are compared to. Figure 1.2 [10] shows the suggested reflow temperature profile for 63Sn-37Pb eutectic solder. It melts at approximately 183 °C and solder processing is normally performed around 220 °C. Solder alloys should have a small two-phase region for ease of processing. A eutectic alloy is the optimum composition since it has a direct transformation from liquid to solid at the eutectic point. If the two-phase region is too large, the joint members have the opportunity to move with respect to one another during solidification. This results in an irregular, coarse, and sometimes cracked joint surface that often has poor mechanical properties [11].

However, lead based solder alloys have detrimental environmental and healthy issues. The element lead has been cited by the Environmental Protection Agency as one of the top 17 chemicals posing the greatest threat to human life and the environment [12]. European nations issued a directive on “Waste from Electrical and Electronic Equipment” on the 1st of January 2004 [13]. This directive required that the use of lead and some other toxic elements be eliminated in the electrical and electronic manufacture. Thus, a lot of work has been launched to develop lead-free solders to deliver the same performance as lead-based solders. The common goal is to determine which alloys should be used to replace the estimated 50,000 metric tons of lead-tin solder currently used each year.

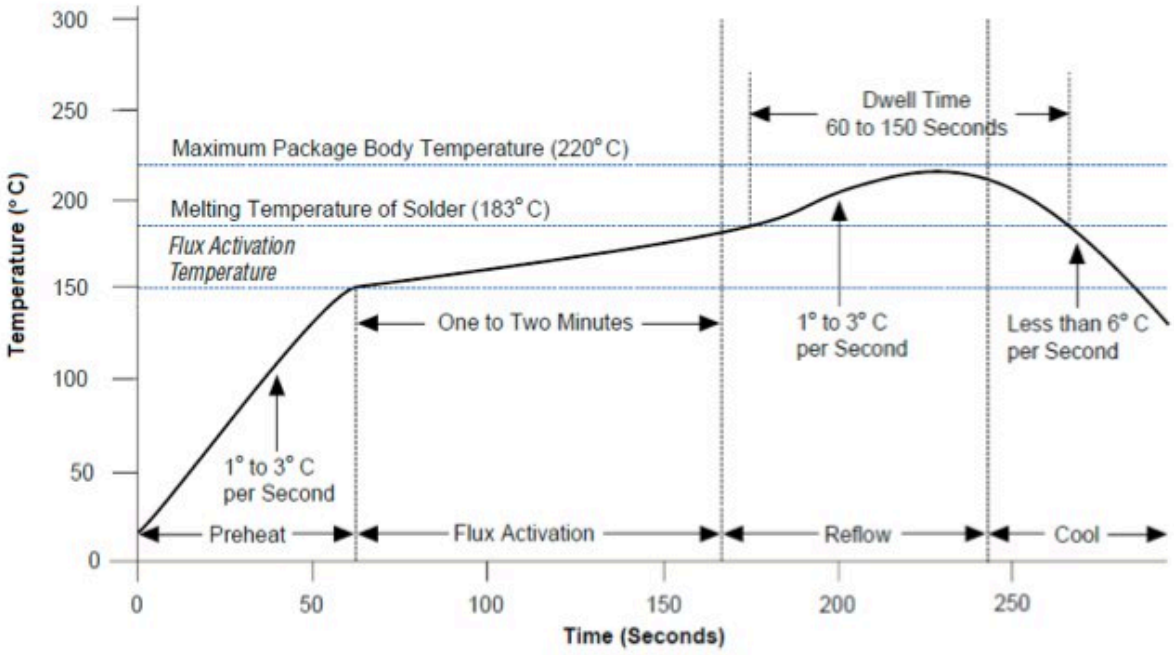


Figure 1.2 Suggested heating profile for 63Sn-37Pb eutectic solder [10].

The materials chosen to replace lead must meet a variety of requirements, such as be availability worldwide in large quantities, non-toxic, recyclable and comparative low cost. Elements that are available in quantities sufficient to satisfy the high volume of demand include tin, copper and silver. Current industry trend is to use the near-eutectic tin-silver-copper alloy. Some commercially viable examples are 99.3Sn/0.7Cu, 96.5Sn/3.5Ag, and 96.5Sn/3.0Ag/0.5Cu (SAC 305). All of these solder alloys have different melting points, mechanical properties, wetting characteristics and cosmetic appearances when compared to tin-lead solders. The ideal lead-free solder alloy should have good electrical and mechanical properties, good wetting abilities, no electrolytic corrosion, acceptable cost, and current and future availability for different applications [14].

Usually, the soldered die-attachment joints are susceptible to fatigue failure under cyclic temperature loading because of its low yield strength and the accumulation of high inelastic strains during deformation. This reliability issue becomes more severe if the junction temperature of future semiconductor device is raised to 175 °C or even higher [15]. Thus one of the foremost challenges need to overcome is the low melting temperature of solder joints. The increased operating temperature is getting closer to the melting point of solders, thus making the attachment susceptible to thermo-mechanical and metallurgical problems.

(b) Sintering of silver

The sintering of powder compacts had been widely applied in microelectronics for making hybrid circuits, co-fired multilayer metal/ceramic interconnecting substrates, multilayer ceramic capacitors, magnetic components, etc. Basically, sintering is a heating process that causes the powder particles to bond together, resulting in significant strengthening and improved thermal, electrical properties for the whole structure [16]. It can be classified into several types based on the mechanisms that are thought to be responsible for shrinkage or densification. For the silver powders or flakes, the sintering process is based on solid-state diffusion, which means the sintering of silver paste is solid-state sintering. There is no phase transition during the sintering of silver, which offers an opportunity to form a bonding below the melting temperature of silver.

Solid-state sintering process can be divided into three stages [17, 18]: initial stage, intermediate stage and final stage. There is no clear distinction between stages. However, we can still distinguish one stage from another. Figure 1.3 is the representation of each stage. In the initial stage, the particles rearrange and there is an increase in inter-particle contact. Necks form rapidly between particles. During the intermediate stage, the porous structure becomes smooth and develops an interconnected structure between particles, which gives a larger average grain size with fewer grains. Densification is assumed to take place by the reduction in cross section of the pores. For the final stage, pores are becoming unstable and start to close. The grain growth is evident for this stage.

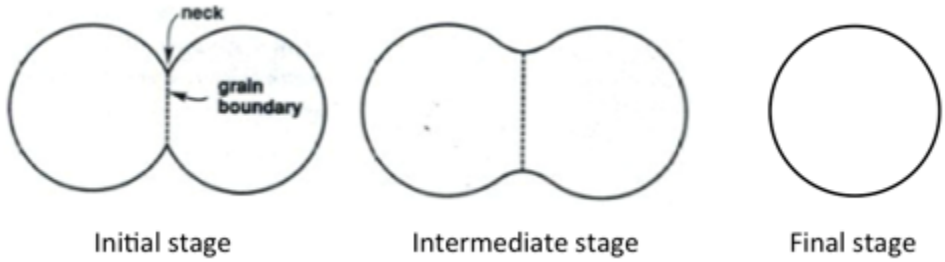


Figure 1.3 Different stages for solid-state sintering.

Base on the theory of solid-state sintering, an alternative technique from solder reflow was engineered. This so-called low temperature joining technique (LTJT) was based on the sintering of silver powders and flakes. These silver powders and flakes were coated with organic

additives. These additives were for the production process of the silver powders [19]. Since the conventional sintering of existing thick-film silver pastes normally requires a temperature that may be substantially higher than the maximum temperature a semiconductor device can tolerate, any means of lowing the sintering temperature is desirable and necessary for the successful implementation.

The LTJT bonding was formed by a solid-state sintering process. Because of the high melting point of silver (961 °C), this sintering process contains no liquid phase. Therefore, it was predicted that the interconnection possesses good stability even at temperatures higher than the processing temperature.

Figure 1.4 is a schematic of LTJT technology [20]. Silver paste can be applied by screen or stencil printing, spray coating, and automated dispensing. The silver flakes are suspended in organic solvent with a viscosity adjustable to the respective application method. After applying the silver paste, the organic solvent has to be evaporated at a relatively low temperature, about 150 °C [21]. Chips were mounted on top of the paste after the drying stage. During the sintering process, a hydraulic press nearly about 40 MPa pressure is used to provide uniaxial pressure, which is usually applied at 230 - 250 °C to promote the sintering and densification of the silver powders and flakes [22]. Figure 1.5 shows the SEM image of sintered silver layer of LTJT [23].

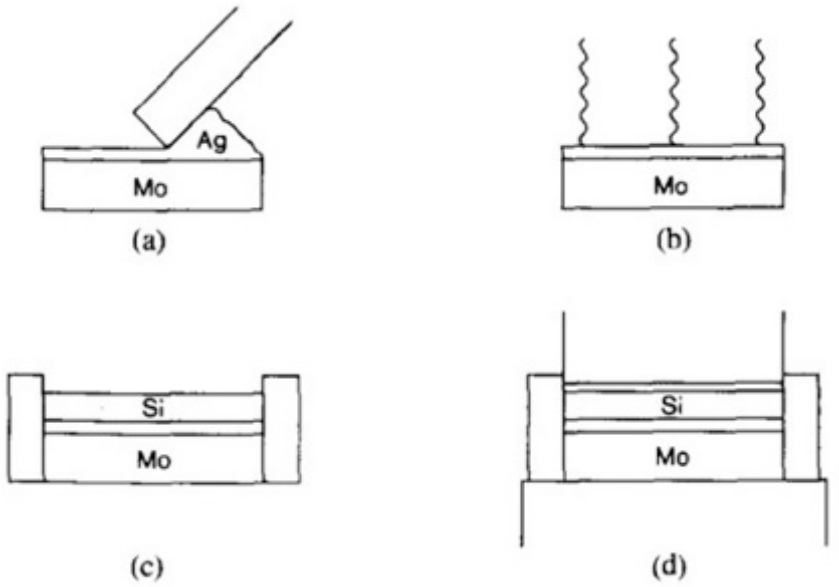


Figure 1.4 Schematic representation of the low-temperature joining process: (a) Deposition of the Ag powder; (b) drying; (c) positioning of the device on the substrate; (d) sintering under pressure [20].

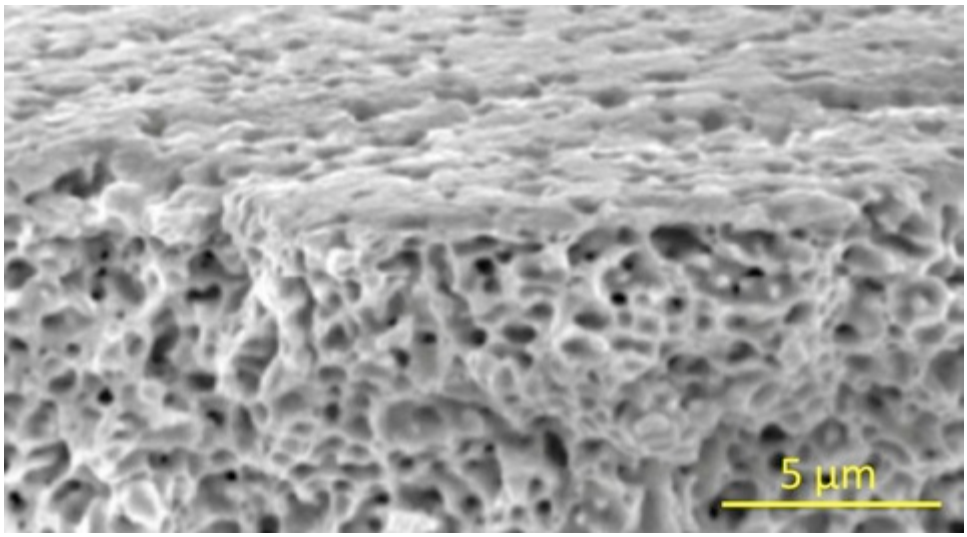


Figure 1.5 SEM image of sintered silver layer of LTJT [23].

(c) Comparison between solder reflow and sintering of silver

Table 1.1 is a list of some measured properties of LTJT sintered silver joints compared with several kinds of solder joints. It shows that sintered silver joints have much better electrical conductivity comparing to traditional types of solder. Meanwhile, the thermal conductivity of sintered silver joints is more than three times better than that of soft solder attachment, which means a very low thermal resistance from the die-attach layer can be achieved. Another advantage of sinter silver joints is the large range of application temperature (< 961 °C), making it a promising die-attach technology for high temperature application.

Table 1.1 Properties comparison of LTJT sintered silver with solder alloys.

	Processing temperature	Max. use temperature	Electrical conductivity 10^5 $(\Omega\text{-cm})^{-1}$	Thermal conductivity (W/K-cm)	Die-shear Strength (MPa)
Lead-tin solder	217°C	< 183°C	0.69	0.51	35
Lead-free solder	260°C	< 225°C	0.75	0.70	35
Gold-tin solder	310°C	< 280°C	0.625	0.58	30 - 60
LTJT Sintered silver	< 250°C	< 961°C	3.8	2.4	40

Because of the high melting temperature of the sintered silver, it is expected that the reliability of the LTJT layer is much better than that of the solder layer. A significant improvement in the temperature cycling reliability test has been obtained by applying the LTJT technique in a large-area device attachment [24]. The results showed sintered silver joints have more than 10 times longer lifetime than standard solder layers. Power cycling results of modules with an LTJT sintered silver layer also proved the excellent reliability of it [25].

However, solder alloys also have their advantages compare to LTJT sintered silver. First, solder reflow technique has a much longer history. For decades, numerous researches on different kinds of solder alloys have already established an exhaustive knowledge base about the physical metallurgy, mechanical properties, flux chemistries, manufacturing processes and reliability data. Besides, in today's electronic industry, companies all have their mature productive assembly line based on solder reflow techniques. While for LTJT, a serious drawback is the use of high range quasi-static pressure (40 MPa or 400 Kg-force per cm^2 chip area), in order to obtain the high density at less than 300 °C by using the existing types of thick-film silver pastes. The need of such large pressure has limited the application of this technology because it significantly decreases the production throughput and places much higher demands on the flatness and thickness of chip and substrate. Also, the application of external pressure tends to increases the cost of equipment and complicate the manufacturing process.

1.1.2 Nanosilver LTJT

Since the LTJT sintered silver layer has such superior properties, any approach for lowering the application threshold is desirable and necessary. There is a requirement for searching methods to lower or even eliminate the high range pressure for sintering. Based on this, a new technology, nanosilver LTJT, was developed: by reducing the particle size of silver to nanoscale, mixing with different kinds of organic additives, nanosilver paste was introduced in this section.

In sintering theory, the particle size is a crucial factor for the densification process. In the Mackenzie-Shuttleworth sintering model [26], assume ρ is the density, the densification rate $d\rho/dt$ is given by

$$\frac{d\rho}{dt} = \frac{3}{2}\left(\frac{\gamma}{r} + P_{applied}\right) \times (1-\rho)\left(1 - \alpha\left(\frac{1}{\rho} - 1\right)^{\frac{1}{3}} \times ln\frac{1}{1-\rho}\right)\frac{1}{\eta} \qquad (1.1)$$

where γ is the surface energy; r is the particle radius; and $P_{applied}$ is external pressure or stress. The part $\frac{\gamma}{r} + P_{applied}$ would be the driving force of densification, so the densification rate is dependent on the particle size. If the sintering process without external pressure, by reducing the size from 1 μm to 100 nm, we increase the densification driving force for 10 times. Thermodynamically, nanoscale materials have significantly high driving force, because of the large specific surface energy. This could realize the low-temperature sintering process.

Another theoretical foundation for nanosilver paste is the mass transport mechanisms of solid-state sintering. There are six different types of mass transport mechanisms. Figure 1.6 and Table 1.2 shows these mechanisms [27]. Three of them are controlled by surface transport: vapor diffusion, surface diffusion and lattice diffusion (from surface). They are usually occurred at low temperatures, resulting in neck formation between particles or grain growth, but do little to the actual densification of the particle system. The other three are controlled by bulk transport: plastic flow, grain boundary diffusion and lattice diffusion (from grain boundary). They are usually occurred at high temperature ranges, which will contribute to the shrinkage and densification of the system. If a non-densification mechanism is preceded, it will consume the total driving force of sintering, which makes it difficult to achieve high-density structure. So for developing the sintering process for die-attachment, we need to avoid the non-densification mechanisms.

Based on this theory, Lu *et al*. investigated the fabrication process of nanoscale silver paste [28, 29]. The formulation process of the paste is shown in Figure 1.7. Nanoscale silver particles, which in the scale of 50 - 100 nm, could easily start agglomerating at room temperature. In order to prevent them from agglomeration, they were attached by short hydrocarbon chains of surfactant, then they were separated by long hydrocarbon chains of binder. Organic solvent as the function of thinner, were added in to adjust the viscosity of the paste for the printing application. After ultrasound agitation, the paste was in the form similar to the commercialized solder paste. More details of paste formulation can be found at somewhere else [30].

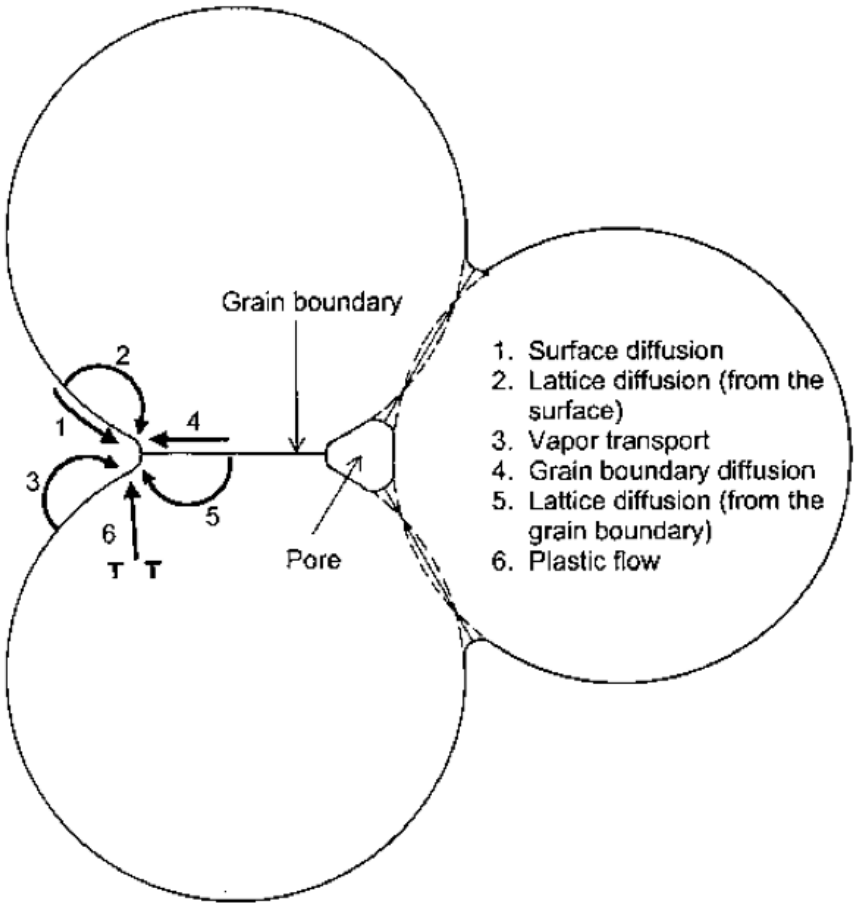


Figure 1.6 Six types of mass transport mechanisms of solid-state sintering [27].

Table 1.2 The transport paths, sources and sinks of matter during sintering [27].

Transport	Source of atoms	Sink of atoms	Densification
1. Surface diffusion	Surface	Neck	No
2. Lattice diffusion	Surface	Neck	No
3. Vapor diffusion	Surface	Neck	No
4. Boundary diffusion	Grain boundary	Neck	Yes
5. Lattice diffusion	Grain boundary	Neck	Yes
6. Plastic flow	Dislocations	Neck	Yes

Figure 1.7 Basic formulation process of nanosilver paste.

When the paste is heated up to a certain temperature, usually above 250 °C, the organics in the paste can be totally burn off with the assistance of oxygen. After that, the silver particles start to sinter, which can realize the die-attachment process by diffusion bonding. Figure 1.8 is an SEM image of nanosilver paste sintered at 275 °C without applying any pressure, which shows a relative density of about 80% of bulk silver. This improvement not only makes the 3-D high-density integration possible, but also greatly reduces the fabrication complexity and the cost. Nanosilver pastes can be either screen/stencil-printed or syringe-dispensed and they can be served as a direct substitution to the commercially available silver paste or solder paste.

The sintered nanosilver paste almost has the same electronic and thermal conductivity and a wide range of working temperature with LTJT sintered silver. For small area (< 3 mm × 3 mm) die-attachment, the silver joints formed by the low-temperature sintering technology have a bonding strength about 40 MPa on the silver-coated substrates, similar to the eutectic solder joint strength [31].

The porous microstructure gives the sintered material a low modulus of around 10 GPa comparing to that of bulk silver 75 GPa, making it mechanically compliant for relieving thermo-mechanical stresses in the attachment [32]. Bai *et al* demonstrated the high thermo-mechanical reliability of the low-temperature sintered silver die-attachment using a combination of die-shear and thermal cycling experiments [33]. Sintered nanosilver joints failed over 4000 cycles with temperature of 50 - 250 °C (cycle time 7.5 min).

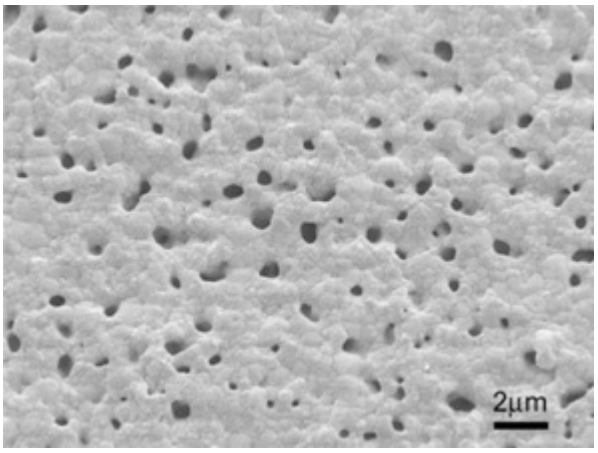


Figure 1.8 SEM image of nanosilver paste after sintering at 275 °C.

1.2 Copper application in electronic packaging and limitations

Copper is a ductile metal. Pure copper is soft and malleable; an exposed surface has a reddish-orange tarnish. Copper and copper alloys are widely used in microelectronic packaging. Compare to other metals, copper has low cost, high thermal and electrical conductivity, easy fabricating, and wide range of attainable mechanical properties. Copper is usually the material for lead frames, traces in printed circuit board (PWB), die-attach substrates, and heat sinks [34].

However, copper oxidation has been considered as a serious problem in electronic packaging. The copper oxide layer is not self-protected, so the copper is readily oxidized more or less. The oxidation layer would generate poor adhesion for the copper surface interconnections, and it would also form cracks or delamination for multilayer structures that contain copper [35, 36].

1.2.1 Applications of copper in electronic packaging

Several application areas of copper are discussed as follows:

(a) Lead frame

Copper and copper alloys serve as the most dominant lead frame materials [37, 38]. The copper alloy lead frame mechanically supports the chip during the assembly of packaging and to connect the chip electrically with the outer pins. Typically, lead frame strips are made first, and then the copper alloy lead frames are manufactured by etching on the lead frame strips. The

process of etching lead frames involves coating with photoresist film, exposing through the lead frame pattern using an ultraviolet light, and the developing the finished pattern. Figure 1.9 [39] is typical image of copper lead frame.

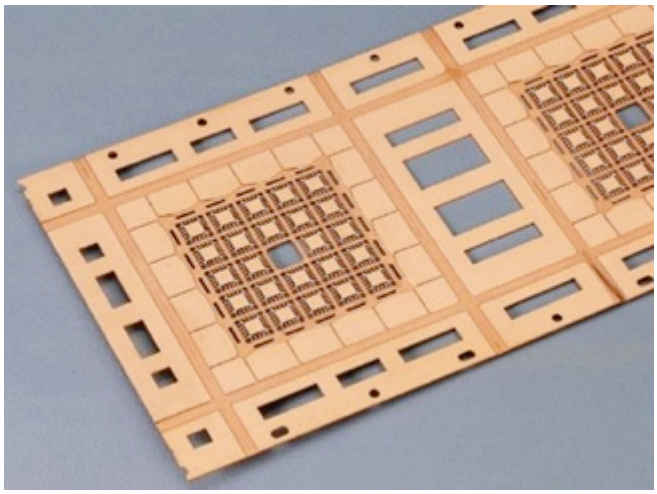


Figure 1.9 Copper lead frame [39].

(b) Traces in PWB

Printed wiring board (PWB) is used to mechanically support and electrically connect electronic components using conductive pathways, tracks or signal traces etched from electrical conductive sheets laminated onto a non-conductive substrate. It is also referred to as printed circuit board (PWB).

Copper is most widely used conducting materials in PWB manufacture [40]. The copper traces are derived from copper cladding that is integral to substrate materials and/or from the electrolytic and electro-less copper plating. The copper conductors in PWB can also be made by copper foil on an insulating substrate to form the desired circuits. Figure 1.10 shows a typical PWB board with copper trace on it.

(c) Die-attach substrates

For die-attachment, the substrates can provide mechanical support for the devices, conductive traces, insulation and heat removal pass. Direct bonded copper (DBC) substrate has been widely used in power electronics industry [41, 42]. Characteristic features of DBC substrate are thick solid copper conductors bond on both side of an alumina or aluminum nitride base-plate. Figure 1.11 is the schematic of a typical DBC substrate.

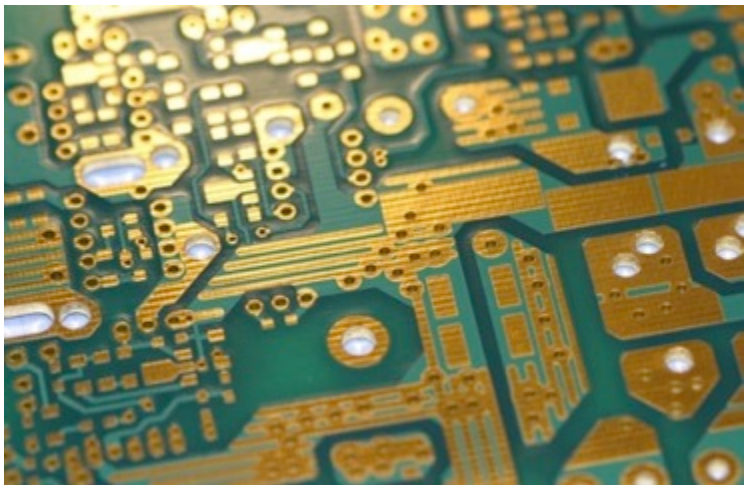


Figure 1.10 PWB board with copper trace on it.

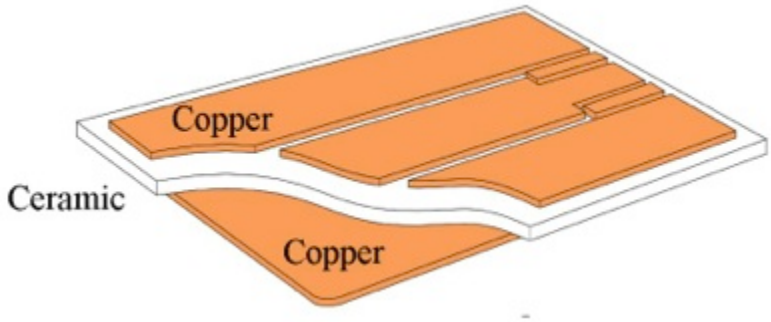


Figure 1.11 Schematic of DBC substrate.

DBC probably is the most widely used substrate material in power electronics due to its high current-carrying capacity, high thermal and electrical conductivity. Another advantage is its controlled coefficient of thermal expansion (CTE) (6 – 8 ppm/K for alumina-based DBC and 4 – 5 ppm/K for aluminum nitride-based DBC), which matches well with that of semiconductor devices (2.3 – 4.7 ppm/K for Si, and 4.5 – 4.9 ppm/K for SiC). DBC substrate also provides advantages in lower weight compared with many other heavy metal substrates, which is one of the most critical points in space applications.

(d) Heat sink

Heat sink is commonly used to transport heat dissipated by devices to a heat exchanger. By spreading the heat to a large surface area, it can cool down the system by radiation or convection. Copper has a high thermal conductivity twice that of aluminum, so copper heat sinks are highly suitable for cooling devices that are very small with a concentrated source of heat.

Nowadays, the most widely used copper heat sinks are laminated metal sandwiches consisting of two layers of copper bonded to a central constraining layer of Invar or molybdenum, referred to as copper-clad Invar (CCI) and copper-clad molybdenum (CCM) [43].

The requirements for heat sinks are high thermal conductivity and compatible CTE to other components in the assembly. For both CCI and CCM, the thermal conductivities are higher than 160 W/m K. For the CTE, CCI is 5.5 ppm/K while CCM is 6.0 ppm/K, which are close to the DBC substrates and semiconductor devices.

1.2.2 Copper oxidation and effects in electronic packaging

(a) Theoretical analysis of copper oxidation

With a lot of advantages, copper have already well applied in electronic packaging technology as one of the main materials for the lead frames, PWB and die-attach substrates. However, the applications of copper have been limited by oxidation of the copper.

M. Lenglet *et al* studied the early stages of low temperature (< 573 K) copper oxidation [44]. They believed that there was unambiguously a fast process of Cu to Cu_3O_2 and a slow process for the formation of CuO. They demonstrated the mechanism of nucleation of CuO as a result of the aggregation of vacancies internally in cuprous oxides.

Generally, there are two steps of copper oxidation [43]: A Cu_2O is a p-type semiconductor with negatively charged vacancies. The growth of the Cu_2O takes place on the top surface through the mass transport of Cu^+ ions and electrons in a direction normal to the surface via vacancies. However, Cu_2O is hardly observed in experiments because it is thermodynamically unstable in air. The second stage of oxidation, the formation of the CuO from Cu_2O is usually a slower process. It is governed by the diffusion of oxygen into the oxide. Detailed discussion of copper oxidation will discussed as follows.

When a clean surface of Cu is exposed to oxygen, the gas molecules are chemisorbed and formed a monolayer of oxide. It follows with a rapid oxidation process, in which the movement of Cu^+ ions across the oxide layer is controlled by the strength of the electric field between the metal and the chemisorbed oxygen. As the film thickness grows, the effect of the electric field diminishes as its gradient decreases and a slower, diffusion dependent process of the parabolic law becomes important. The critical film thickness for the transition to the diffusion process depends upon the metal and the model employed in describing thin film oxidation. In copper the

transition is assumed to take place at around 100 to 1,000 Å thickness, thus an oxide film of 10^{-4} cm is considered to be thick film [45, 46].

The reactions occurring in the Cu – Cu_2O – O_2 system consists of Cu^+ ions electrons entering the oxide-metal interphase ($Cu \rightarrow Cu^+ + e^-$) and diffusing out to the oxide-gas boundary where oxidation proceeds ($2\ Cu^+ + 2\ e^- + 1/2\ O_2 \rightarrow Cu_2O$). The empirical oxidation rate is given by $dx/dt = k/x$. where k (cm^2s^{-1}) is the parabolic rate constant and x is the oxide film thickness. This rate equation is in agreement with the general observation that, as the oxide becomes thicker, the rate of reaction becomes slower. Integration of the rate equation results in a parabolic equation or the parabolic law [47, 48]:

$$x^2 = 2kt \tag{1.1}$$

In the parabolic law, k is depended on the oxygen concentration and the temperature. In order to minimize the effects of copper oxidation during all kinds of packaging processes, two different ways can decrease the oxidation: control the oxygen partial pressure when copper expose to higher temperature; minimize the time of high temperature exposure.

(b) Effects of copper oxidation

One example is discussed to explain the effects of copper oxidation.

C.T. Chong, et al studied the oxidation of copper lead frame [49]. They found that copper oxidation caused the delamination of lead frames die pad and molding compound in the package at elevated temperature used in assembly such as die attach curing and wire-bond. The die attach curing step they applied was typically performed in the temperature region of 150 °C for about 3 hours, and the wire-bond temperature was ranging from 180 °C to 280 °C with duration time about 20 to 200 seconds. These conditions cause the copper lead frames to oxide.

In this case, the copper oxidation due to die attach curing can be minimized by setting the oven with inert atmosphere. However, the wire-bond process is usually processed in an open air, so that the copper lead frame oxidation induced by wire bonding was severe. As a result, the copper oxidation separated the lead frame from the molding compound, as shown in Figure 1.12. Adhesion test were performed after post mold cure. The results generally showed that a copper

lead frame exposed to higher temperature for longer periods have lower adhesion strength to the mold compound.

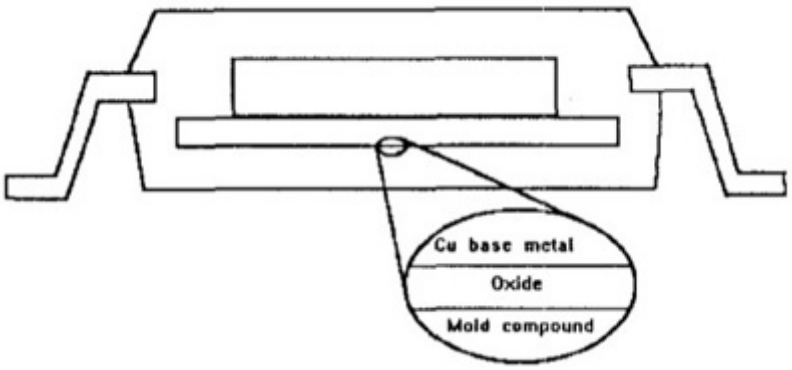


Figure 1.12 Copper oxide layer between base metal and mold compound [49].

1.3 Motivation and objectives of this research

1.3.1 Motivation of research

As introduced and discussed in the previous sections, die-attachment, being regarded as the first step for the semiconductor packaging, has to meet an increasing requirement of high performance, high reliability and low cost. Compared to the traditional solder reflow die-attach technology, LTJT sintered silver joints have much better electrical and thermal conductivity and also much higher reliability. However, the drawback for LTJT technology is the high range pressure requirement during the sintering.

In order to lower or even eliminate the assisted pressure for sintering, one possible way is to reducing the size of particles to nanoscale. A new die-attach material – nanosilver paste was introduced. This approach utilizes the large thermodynamic driving force for densification by increasing surface area to volume ratio and particle surface curvature. Former studies have already demonstrated the process of low-temperature sintering technique applying the nanosilver paste. The sintered nanosilver joints has the advantages as follows:

1. This technology has the ability to eliminate the use of external pressure during the low-temperature sintering process. Unlike solder reflow, the processing temperature of nanosilver paste is far below the melting point of element silver [50]. The sintered silver

film or joint can retain their shapes at the sintering temperatures. So it is well suit to 3-D high-density power package.

2. Sintered nanosilver layer has very high electrical and thermal conductivities. Both the electrical and thermal conductivities of the low-temperature sintered silver are about 3-5 times of those of the best solders and also much higher than those of the conductive epoxies [30].
3. The sintered nanosilver joints were demonstrated to have excellent reliability. The low-temperature sintered silver has around 20% porosity. The porous microstructure gives the sintered material a low effective modulus at about 10 GPa, which is even lower than eutectic lead-tin solder. So it can transfer less of thermal stress due to the semiconductor-metal CTE mismatch. Meanwhile, the sintered joint is pure silver with a much higher melting point than any kind of solder, its reliability is high because the phase separation and creep failure are avoided or greatly reduced [51].

With such good features, low temperature sintering of nanosilver paste is a promising lead free solution for semiconductor devices attachment. However, one limitation of this technology is the surface metallization requirement. In former studies of die-attachment using nanosilver paste, the substrates needed to be metallized with silver or gold. The metallization layer has a huge effect on the overall performance of the sintered joints. Most commercialized substrates, such as DBC, usually has pure copper surface. The surface metallization technologies for substrates, such as electrolytic plating, physical or chemical vapor deposition and sputtering, usually contain many complicated steps and require expensive equipment. These surface metallization technologies increase the total cost of the substrate manufacturing and lower the productivity. This research endeavors to overcome this surface metallization issue of substrate for the application of nanosilver paste, thus lower the total cost of packaging.

1.3.2 Objectives of research

In order to broaden the application scope of nanosilver paste, different processes were developed in this study for realizing sintered nanosilver die-attachment directly on pure copper surface. The specific objectives of this research are listed as follows:

1. To understand the mechanism of solid-state sintering and silver/copper inter-diffusion bonding process: theoretically understanding of the joining mechanisms for the joining technology.
2. Develop processes for low-temperature sintering of nanosilver paste on pure copper surface. The main issue is to control the copper oxidation during the sintering process.
3. For large area attachment, former studies shows that by applying low range pressure (< 5 MPa) during the sintering process, the sintered joints would be very strong, voids free and very reliable. In this study, another objective is to realize the large area die-attachment on pure copper surface by modifying the low-pressure assisted sintering process.

1.4 Organization of thesis

Based on objectives mentioned above, this thesis is divided into the following sequence:

Chapter 1 has provided the different technologies of chip-level packaging. Comparison between typical solder reflow technology and LTJT is provided. Based on this comparison, nanosilver LTJT was introduced as another die-attachment solution with good performance and high reliability. The last part is the advantages, applications and limitations of metal copper in the electronic packaging.

Chapter 2 introduces the development of heating profile for small area die-attachment. After that, different approaches of small area die-attachment on pure copper surface by sintering of nanosilver paste are discussed. Different evaluation methods and results are given at the end of this chapter.

Chapter 3 concentrates on large area die-attachment on pure copper surface. Based on the process developed by former studies. A modified process was introduced to realize such kind of joining. Similar evaluation methods are performed as for small area die-attachment. Due to the applying of pressure during sintering, it can only be done in open air. Copper substrates may got certain degree of oxidation. Wirebondability test was performed at last to evaluate the effect of oxidation.

Chapter 4 summarizes this study and provides recommendation for future work.

Chapter 2

Small area (< 3 mm × 3 mm) die-attachment on Cu surface by nanosilver LTJT

This chapter describes a process for attaching chips with small area (< 3 mm × 3 mm) onto pure Cu surface by nanosilver LTJT. Base on the fundamentals of nanosilver paste, the process for small area die-attachment was discussed. After that, different processes for attaching small chips onto pure Cu surface were developed. The key issue for this kind of attachment is the oxygen partial pressure (P_{O2}) of the atmosphere during the sintering. There is a conflict between burning off the organics in the paste and the Cu oxidation. Due to this conflict, two different methods to control the P_{O2} during the sintering were developed: *I*. generating a negative pressure of air by using a pump; *II*. introducing inert gas atmosphere to control sintering atmosphere. Dummy samples were made to evaluate the bonding strength and microanalysis of the failure surface was followed in order to understand the bonding strength.

2.1 Small area die-attachment process using nanosilver paste

The heating process used for attaching small area chips onto substrate was based on the thermo gravimetric analysis (TGA) and differential scanning calorimetry (DSC) data of the nanosilver paste. Figure 2.1 shows the TGA and DSC results. Weight loss was due to the evaporation of solvents in the paste below 180 °C, an exothermic reaction in the paste with a peak in the DSC curve at around 180 °C. A second exothermic reaction, which also produced a weight loss, showed a peak at about 275 °C. The silver content in the paste was approximately 82 % because after the second exothermic reaction all the organics in the paste have been burned off.

Based on the data, we developed the heating profile of low-temperature sintering of nanosilver paste for attaching small area chips, which shows in Figure 2.2. The total process is about 80 min. After going through this profile, a reasonably high bonding strength can be obtained.

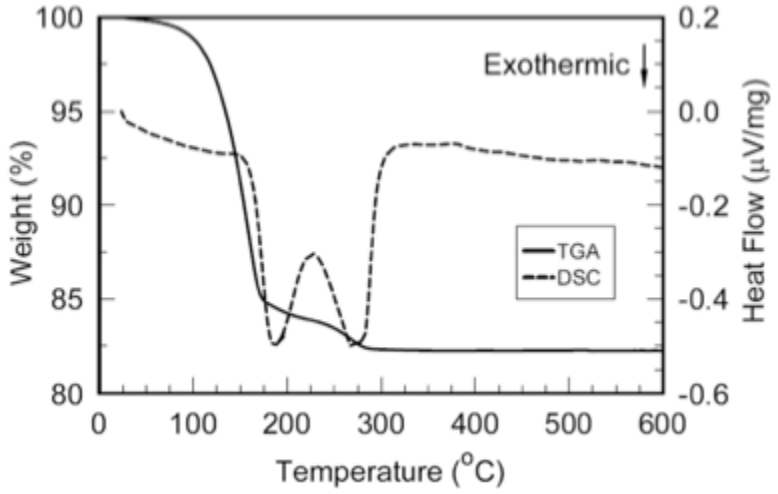


Figure 2.1 TGA and DSC traces of nanosilver paste heated in air with rate 10 K/min.

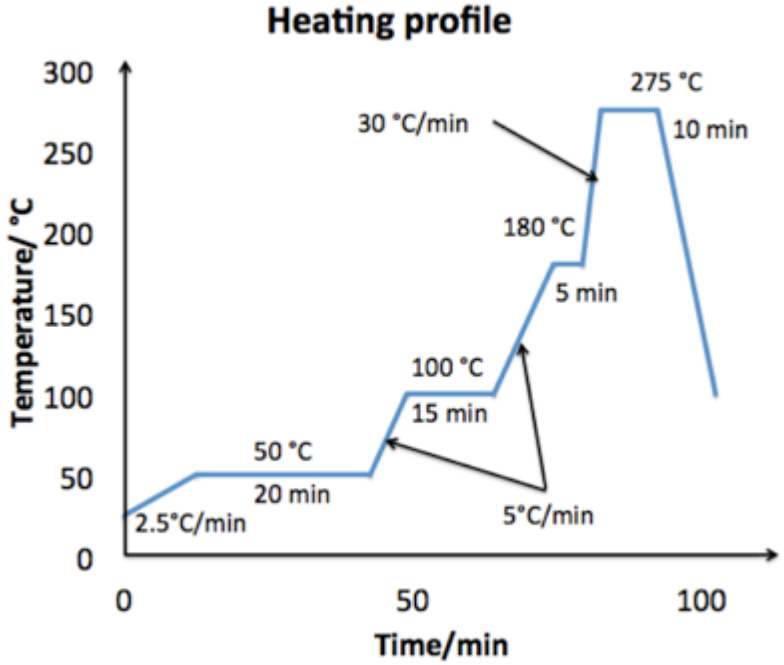


Figure 2.2 Designed heating profile for sintering nanosilver paste for attaching small area chips.

2.2 Process development of die-attachment on pure Cu surface

2.2.1 Control P_{O2} during sintering

From Figure 2.2, the processing temperature can reach 275 °C and soaking about 10 min. If Cu surface goes to such high temperature in the air, it will get severely oxidized, which could prevent the strong bonding formation. In order to minimize the degree of Cu oxidation, the P_{O2} of

sintering atmosphere was manipulated in our process. Two different methods were applied: *I*. Using a mechanical pump to generate a negative air pressure during sintering; *II*. Introducing inert gas to adjust the P_{O2} at different sintering stage. For method *I*, P_{O2} is equal to 21% of the total pressure we generated. For method *II*, pure nitrogen was used because it is inert to pure Cu and organic removal process. Besides, it is also comparatively cheap.

2.2.2 Sample making and experimental setup

Direct bonded copper (DBC) substrates without any surface metallization were applied in this study. They were cut into pieces measured at 10 mm × 15 mm. Due to the difficulty of obtaining shear strength from attached silicon devices, alumina mechanical chips were used instead. For the dummy mechanical chips, we chose alumina pieces with Ag metallization layer on it, because alumina pieces are easy to obtain much flatter surfaces and edges than Cu pieces after cutting into the dimension of 3 mm × 3 mm. To bond the mechanical chips onto DBC substrates, Cu surface was slightly etched by diluted hydrochloric acid to remove the oxidation layer on it. Then it was ultrasonic cleaned in organic solvents acetone and ethanol, separately. After cleaning, a layer of nanosilver paste was stencil printed onto the substrate. Figure 2.3 shows the schematic of stencil printing process. The thickness of the printed paste layer was about 50 μm. Dummy chips mounted on the paste layer immediately after printing. Figure 2.4 is the schematic showing the sample configuration. Since the dummy chips were in small size, no sintering external pressure was needed during the whole bonding process.

Figure 2.5 shows the setup we used to carry out our sintering process under different oxygen partial pressure. The main part of it is a self-made bell-jar vacuum chamber. There is a hot plate inside, which is connected to a temperature controller (Fuji PXR-7). At the top of the chamber there is a vacuum gauge, from which we can read the atmospheric pressure inside the chamber. Thus P_{O2} is about 21% of the gauge reading. The exhaust pipe underneath the chamber can be connected to a pump or a tank of pure N_2. By adjusting the air-inlet valve, we managed the control of P_{O2} inside the chamber.

For method *I*, experiments were done at P_{O2} ranging from 0.04 atm to 0.14 atm with an increment of 0.02 atm. For each P_{O2} condition, a set of five samples was processed and sintered follow the same heating profile.

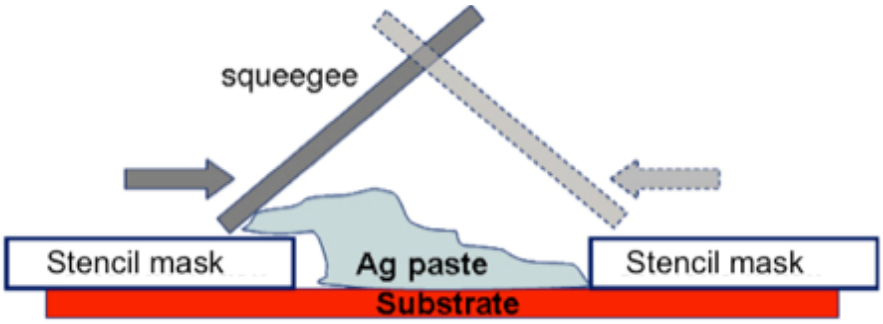


Figure 2.3 Schematic of stencil printing process for nanosilver paste.

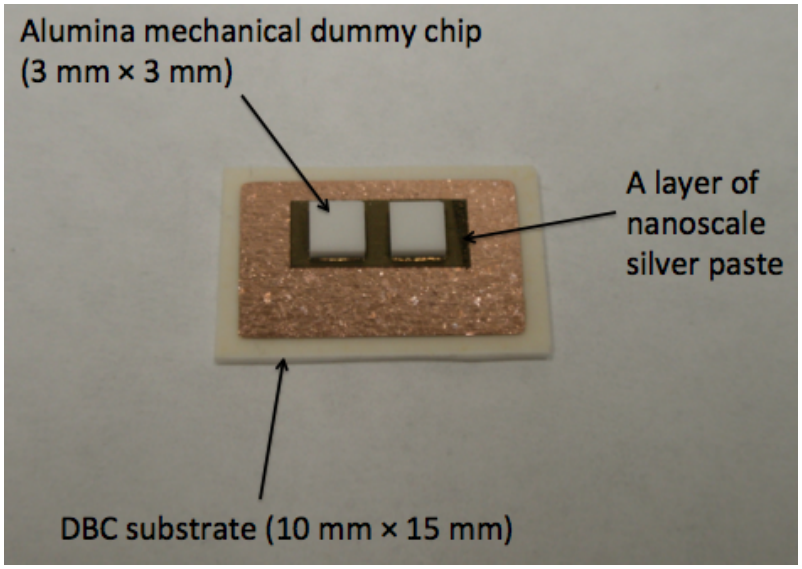


Figure 2.4 Sample configuration of 3 mm × 3 mm die-attachment on Cu surface before sintering.

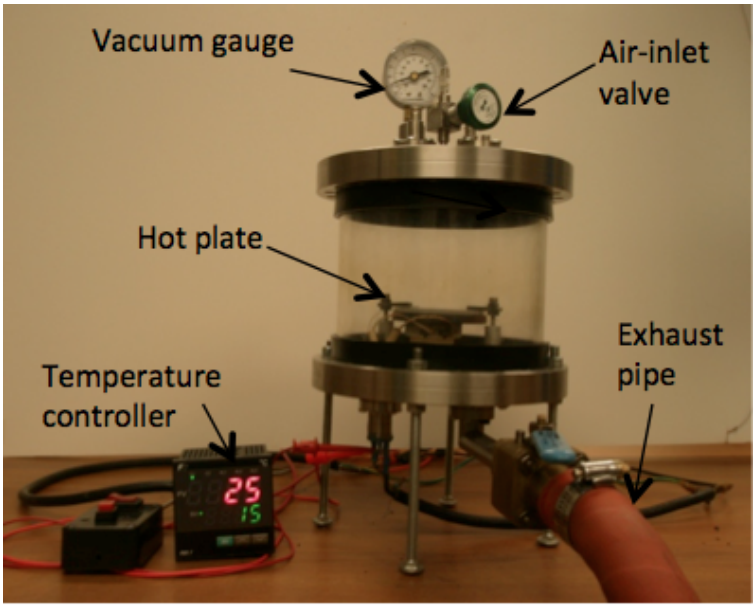


Figure 2.5 Experimental setup for sintering of nanosilver paste with controlled P_{O2}.

2.2.3 Evaluation of sintered joints

Die-shear strengths of the samples were measured by shear test. The schematic of the test method and the shearing fixture is shown in Figure 2.6.

Based on the data of shearing test. Same-sized silicon dummy chips were also attached onto Cu surface following different processes. After sintering samples were cut through the middle, mounted in the epoxy and well polished for the SEM observation and EDS analysis of the cross-section. One of the fine polished samples is shown in Figure 2.7.

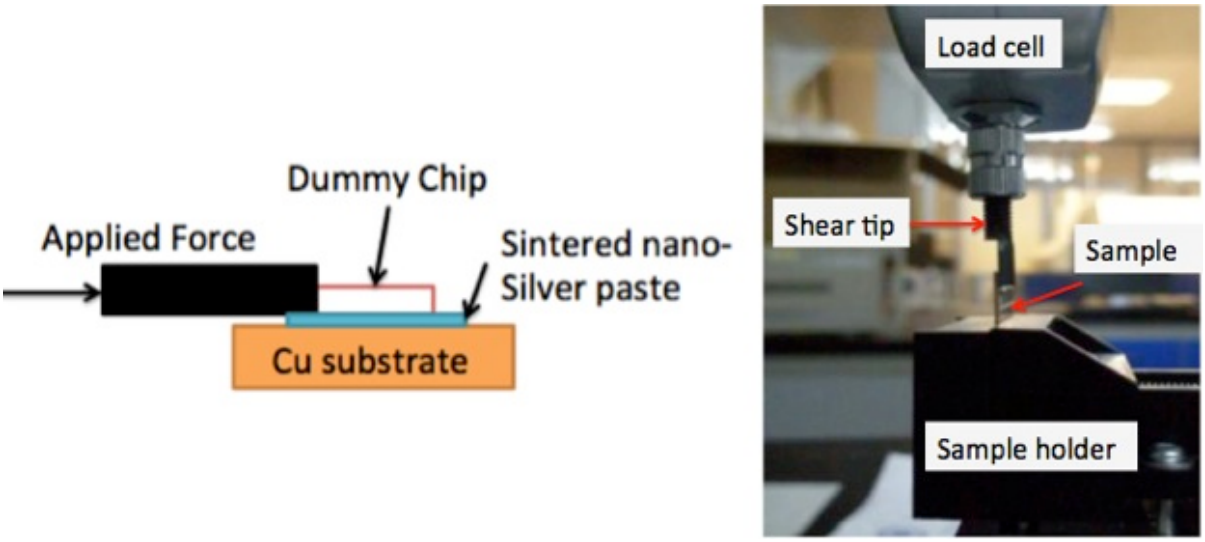


Figure 2.6 Schematic of die-shear test and shearing fixture.

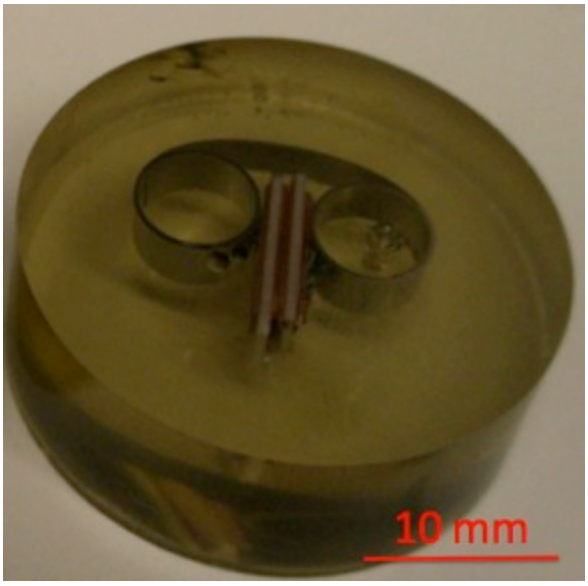


Figure 2.7 Fine polished sample for SEM imaging and EDS analysis

2.3 Results and discussion

2.3.1 Method *I*: Sintering at negative air pressure

For this method, the temperature profile for the sintering is shown in Figure 2.2. Plotted in Figure 2.8 is a bar chart showing the die-shear strength versus oxygen partial pressure of dummy chips bonded on pure copper substrates. P_{O2} is ranging from 0.04 atm to 0.14 atm. It can be seen that the die-shear strengths for all the samples are below 10 MPa. The strengths of this situation are not as strong as the joints sintered on the silver coated Cu, which is usually above 30 MPa shear strength [52]. This means it is difficult to obtain strong bonding by merely reducing the air pressure of the sintering atmosphere. However, it is still possible to find a trend in the results that may be useful in optimizing the process.

The die-shear tests showed that increasing the oxygen partial pressure from 0.04 atm to 0.14 atm caused the bonding strength to increase but eventually declined at higher region. Maximum bonding strength average 8 MPa was attained at P_{O2} = 0.08 atm. For different P_{O2} situations, explanations of the trend are discussed as follows.

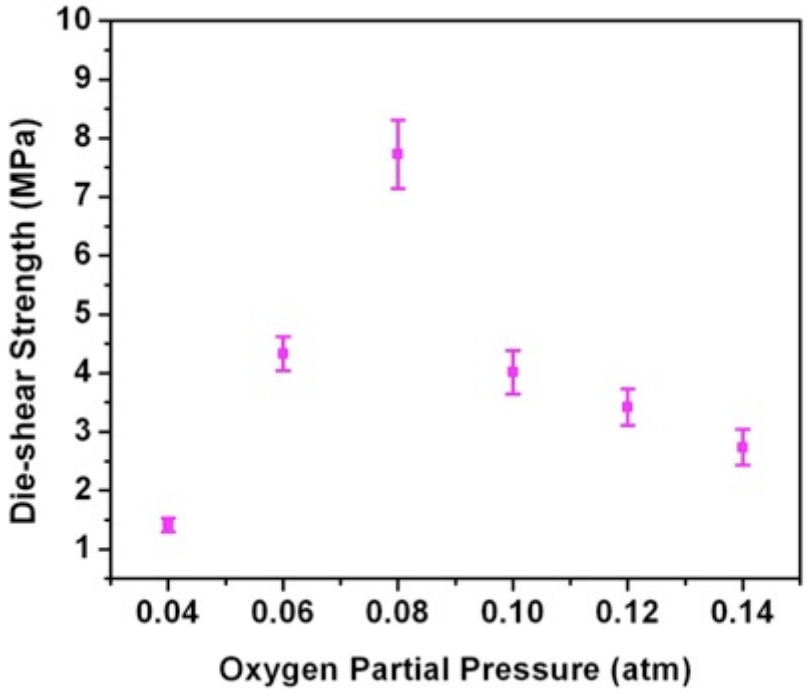


Figure 2.8 Die-shear strengths of 3 mm × 3 mm sample sintered at different P_{O2}.

(a) Sintering under P_{O2} lower than 0.04 atm.

Figure 2.9 is the optical image of the failure surface of a chip after shearing, which was sintered under $P_{O2} < 0.04$ atm. Black residues are clearly visible on the surface. Figure 2.10 is a SEM image with high magnification (× 30,000) of the Ag layer after going through the heating profile on the failure surface, from which we can see that the silver particles were still in the original nanoscale. Thus the low die-shear strength can be explained: at very low oxygen partial pressures (< 0.04 atm), the sintering process of silver particles did not proceed properly because of the incomplete binder burn out with lack of oxygen. The residual organics blocked the particle contact, so there was hardly any densification process occurred after the samples went through the heating profile.

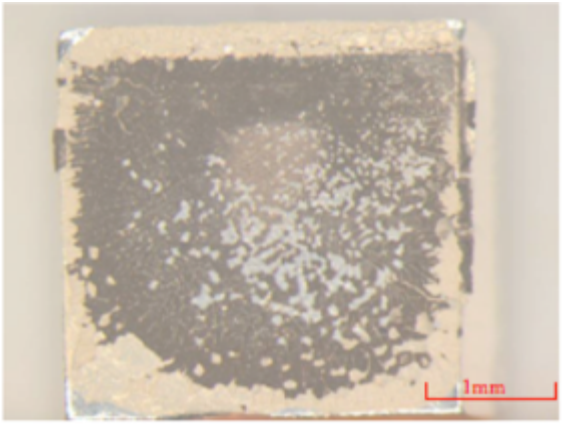


Figure 2.9 Optical image of failure surface of dummy chip ($P_{O2} < 0.04$ atm).

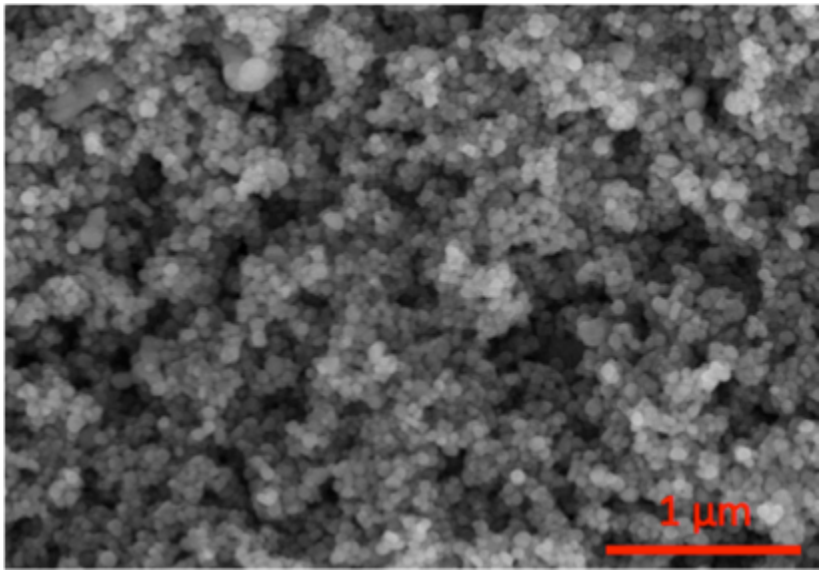


Figure 2.10 SEM image of sintered Ag on failure surface of dummy chip ($P_{O2} < 0.04$ atm).

(b) Sintering under P_{O2} higher than 0.14 atm.

The optical image (Figure 2.11) and the SEM image of Ag layer with same magnification (Figure 2.12) are also presented. The SEM image shows a much denser microstructure compared to that shown in Figure 2.10, which means that the nanoscale silver particles had undergone through the densification process and got much dense structure. However for this situation, it was still unable to form strong joint. The optical image shows that some dark-red regions on the failure surface of dummy chips after shearing. EDS analysis was performed on these dark-red regions, which is shown in Figure 2.13. It shows the high peaks of copper and oxygen in the data. So we believe this dark-red layer is Cu oxide. Therefore, at 0.14 atm of P_{O2}, the organics in the paste were able to burn out so as to allow the densification of silver particles. But, the high oxygen partial pressure also caused the Cu to be severely oxidized, resulting in low die-shear strength because of a dense and weak Cu oxide layer formed at the interface of Cu and Ag.

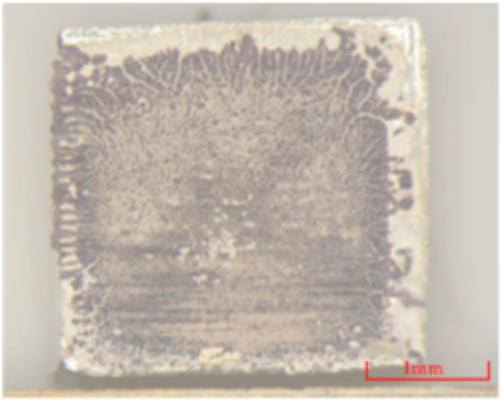


Figure 2.11 Optical image of failure surface of dummy chip ($P_{O2} > 0.14$ atm).

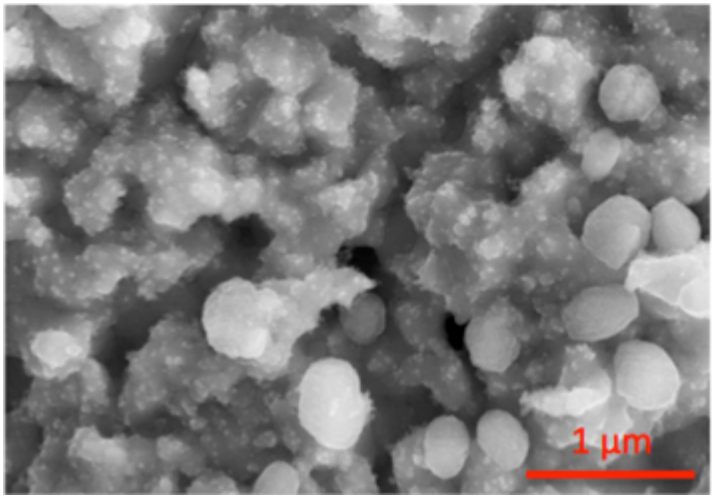


Figure 2.12 SEM image of sintered Ag on failure surface of dummy chip ($P_{O2} > 0.14$ atm).

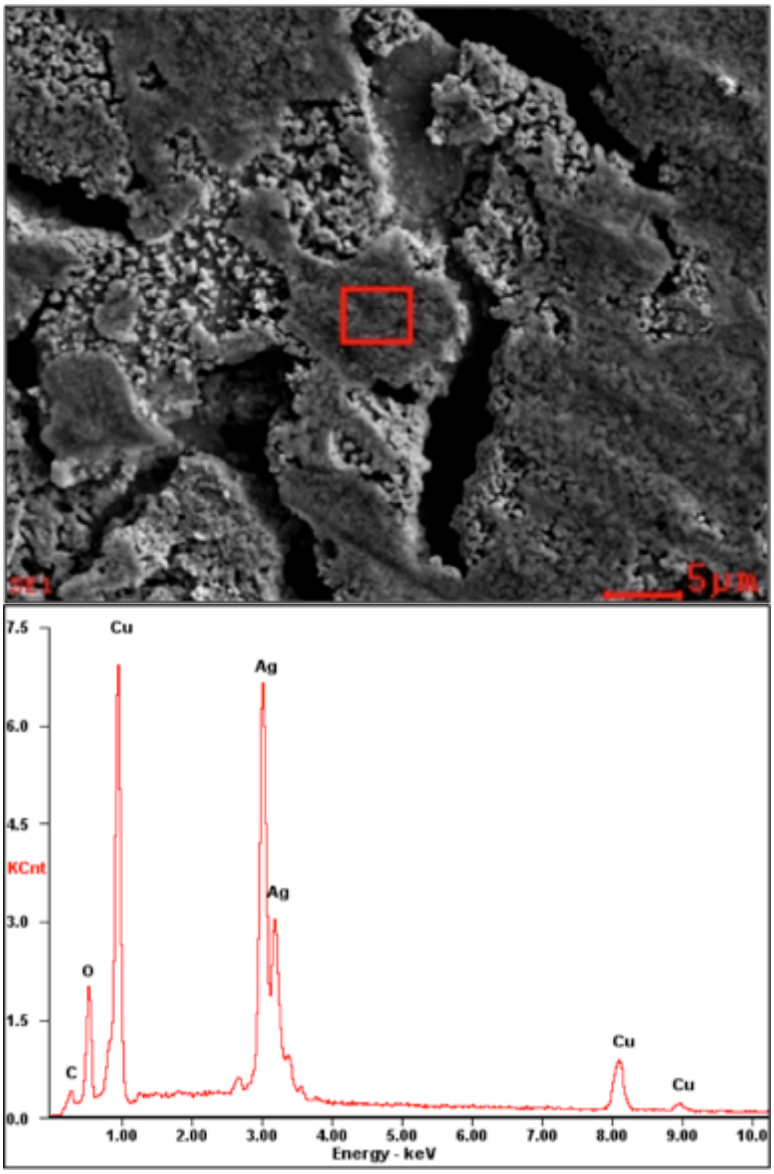


Figure 2.13 EDS analysis of the dark-red layer on failure surface of dummy chip.

(c) Sintering at P_{O2} = 0.08 atm (Peak die-shear strength)

Figure 2.14 is an optical image of the failed surface of a chip bonded at P_{O2} = 0.08 atm. Compared to those shown in Figure 2.9 and Figure 2.11, the surface has neither the black organic residue nor dark-red Cu oxide. Figure 2.15 is a SEM micrograph of Ag layer. Compare to Figure 2.12 and Figure 2.13, no separated nanoscale silver particles can be seen, which means the Ag particles had undergone significant enough consolidation process. That is the reason for that peak bonding strength can be achieved in this situation.

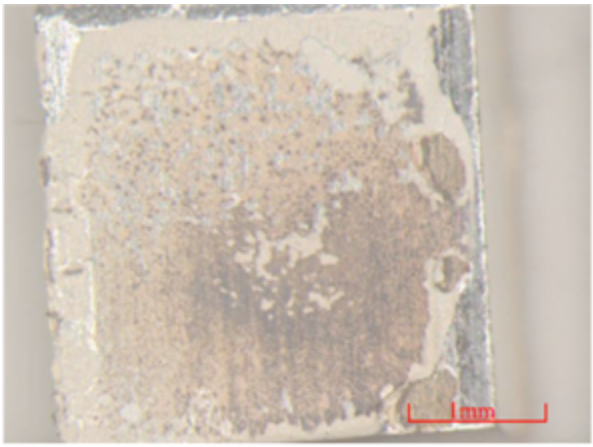


Figure 2.14 Optical image of failure surface of dummy chip (P_{O2} = 0.08 atm).

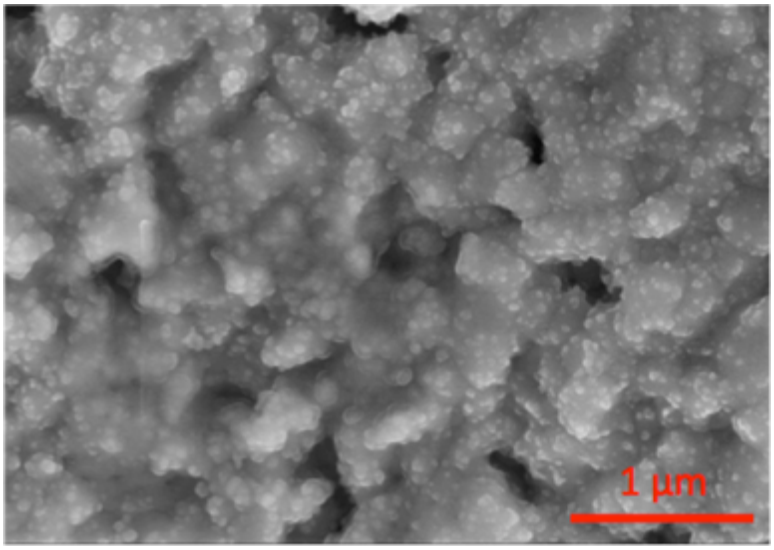


Figure 2.25 SEM image of sintered Ag on failure surface of dummy chip (P_{O2} = 0.08 atm).

2.3.2 Method *II*: Introducing inert gas N_2 atmosphere

For this method, two gas flow meters were used for mixing the sintering atmosphere, which is shown in Figure 2.16. One was connected to a tank of high purity N_2, and the other was connected to a tank of compressed air.

Figure 2.17 shows the thermo gravimetric analysis (TGA) data of the nanoscale silver paste in air and N_2. The two traces almost overlap each other below 180 °C. It indicates that weight loss of the nanosilver paste during the drying process (< 180 °C) has no relation with O_2. Based on this fact, a new process, Process-N_2, was developed for adjusting the P_{O2} at different heating stages (shown in Figure 2.18).

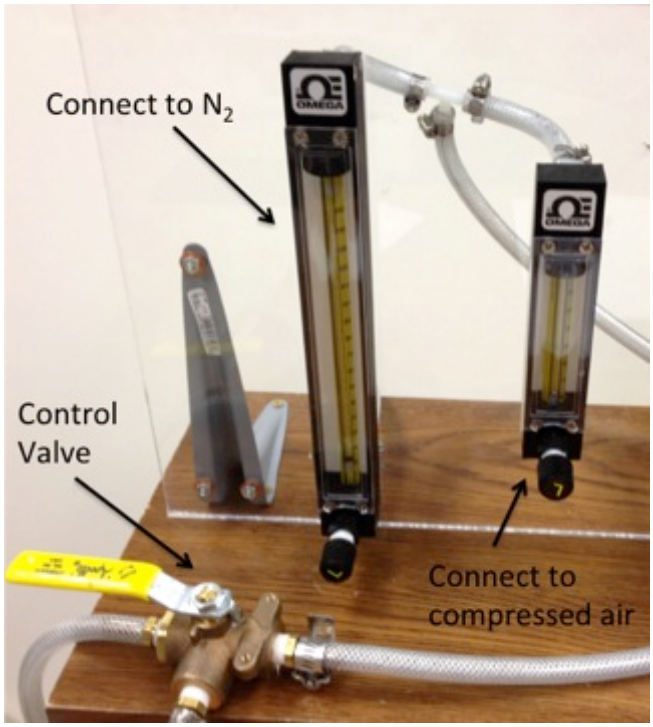


Figure 2.16 Flow meters for mixing the gas.

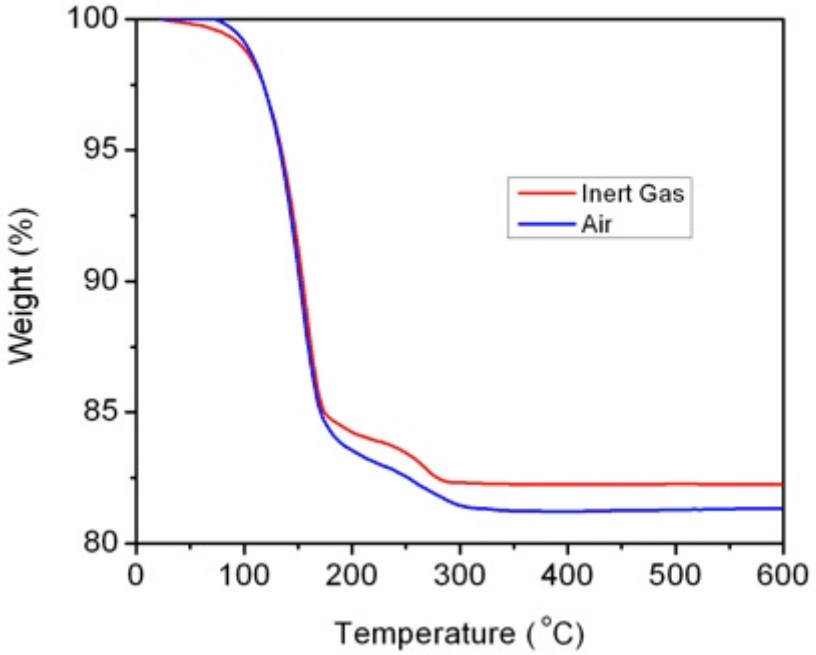


Figure 2.17 TGA traces of nanosilver paste heated in air and N_2.

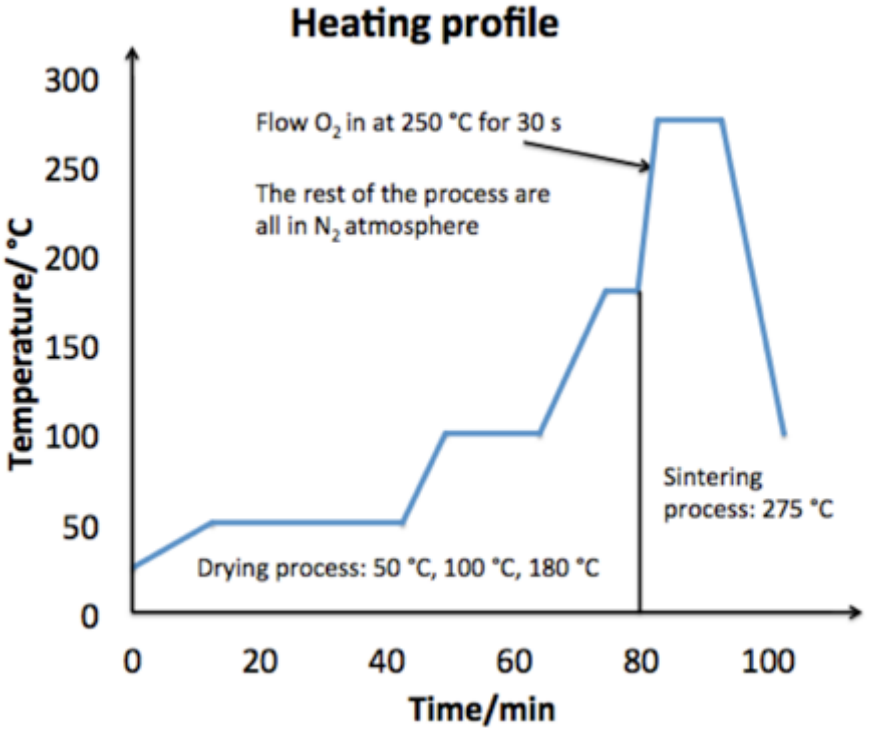


Figure 2.18 Modified process for small area die-attachment on Cu surface: Process-N_2.

In order to reduce the Cu oxidation, the total process was improved by setting the drying step of the process (< 180 °C) in the atmosphere of pure N_2. After drying, an airflow step was added to the new process. Compressed air was flowed into the chamber at around 250 °C for about 30 seconds with the flow rate about 500 ccm. The purpose of this airflow procedure is to burn out the binders in the paste, which is essential for the nanoscale Ag particles to initiate sintering. Five sets of the samples were made and the die-shear tests were performed on them.

The average die-shear strength of the samples made by Process-N_2 including the error bar is plotted in Figure 2.19. For comparison, the typical die-shear strength data of those same-sized chips bonded on a silver-plated substrate along with the highest die-shear strength data by using method *I* were also plotted in Figure 2.19. The die-shear strength of Process-N_2 got a huge improvement though it is still a little lower then the typical bonding strengths of chips attached on silver-plated substrates.

After achieving high die-shear strength with Process-N_2, another process was tried to compare: the only difference compared with Process-N_2 was that the drying process of the samples was in the lowest possible vacuum degree that generated by the mechanical pump. Several sets of the samples made by following this process and then the die-shear tests were done

on these samples. The average die-shear strengths were below 5 MPa. This indicates that if the samples were dried in a low vacuum degree, they could not form a strong bonding afterwards. One possible reason is that the low vacuum degree would lower the boiling point of the solvent in the paste, thus by following the same heating profile would accelerate the evaporation rate of the solvent. This would cause the debonding in the paste layer before Ag particles sintering. This would be the reason for the low bonding strengths of those samples we made by method *I*, controlling the P_{O2} with a pump. Thus, low vacuum degree was avoided in the rest of research.

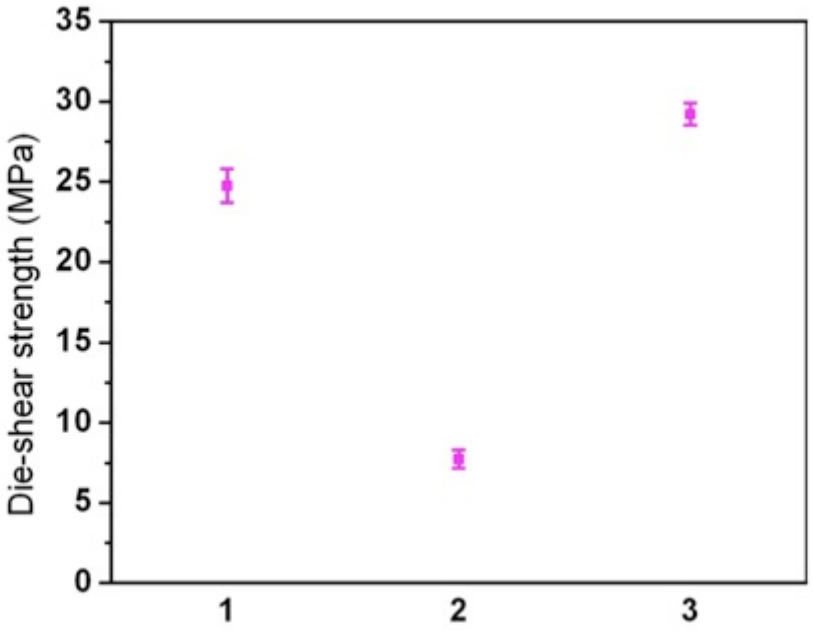


Figure 2.19 Die-shear strengths of different sintered nanosilver die-attachment samples (1) on Cu surface by following Process-N_2; (2) on Cu surface by using pump to generate negative pressure (highest condition); (3) on Ag-coated substrates.

The samples following the Process-N_2 got huge improvement on die-shear strength. Figure 2.20 is a typical SEM image that shows the failure surface of the substrate by following the Process-N_2 with high bonding strength (28 MPa). It can be seen that after shearing off the chip, there was still a layer of sintered Ag attached on the Cu surface. Which means that the failure of the bond during the shearing was happened inside the sintered Ag layer or Ag/chip interface, not the sintered-Ag/Cu interface. Before O_2 (air) flow into the chamber, the binders in the paste were still stable. So Ag particles still remained at nanoscale and separated by the binders. Once the O_2 flowed into the chamber, it burned out the binders in the paste layer with a

high reaction rate. Because the temperature at this time is high (> 250 °C), the driving force for sintering of those nanoscale Ag particles is also huge. Thus the Ag particles sintered rapidly and form a dense layer of Ag and Ag/Cu interface. From the failure model of shearing, it seems that the Ag-Cu bond formed before the Cu surface got heavily oxidized during the O_2 flow step.

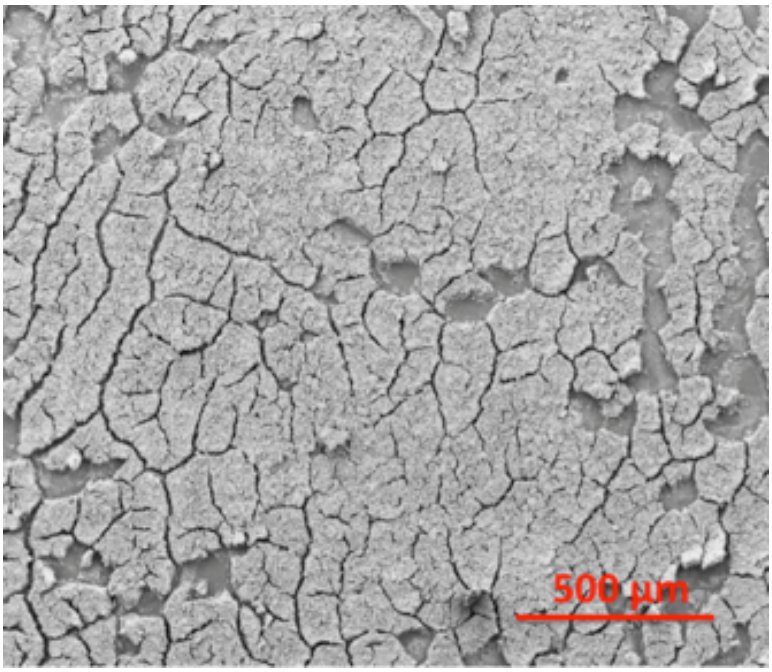
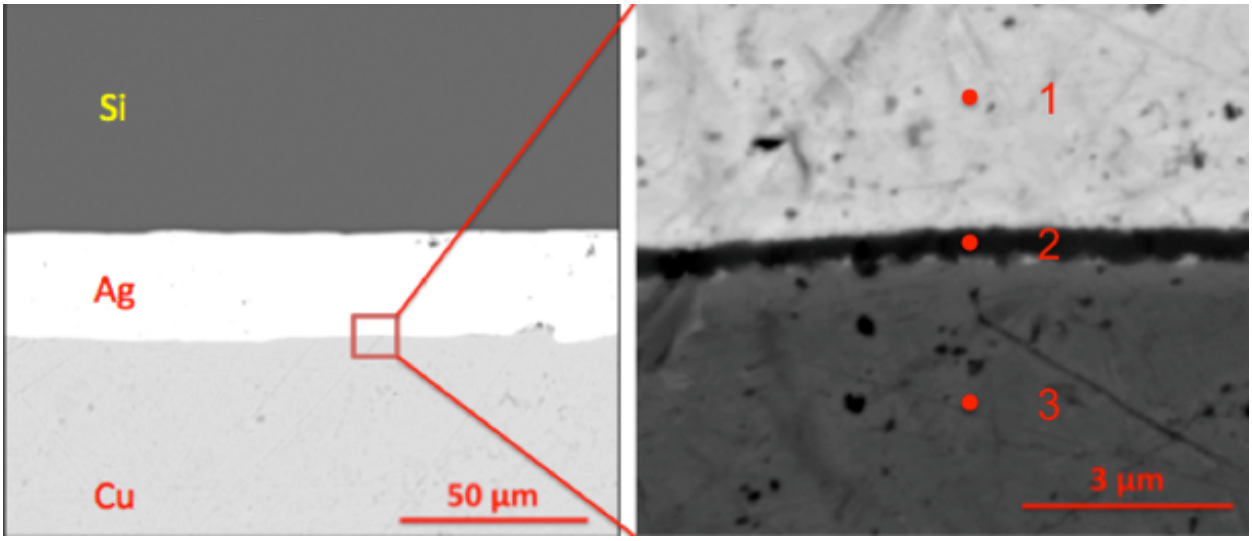


Figure 2.20 SEM image of typical failure surface of Cu substrate after shearing (Process-N_2).



(a) (b)

Figure 2.21 (a) SEM image of cross-section of Si dummy chips attached on Cu surface by following Process-N_2; (b) SEM images of the inter section layer between sintered Ag and Cu.

Table 2.1 EDS analysis of the interfaces

Mass ratio % / Element / Spectrum	C	O	Cu	Ag
1	1.44	7.72	2.83	88.02
2		7.17	58.49	34.34
3	1.07	4.06	94.87	

The same size (3 mm × 3 mm) silicon dummy chips, whose surface coated with Ag, were attached on DBC substrates with pure Cu surface by following Process-N_2. These samples were cut through in order to observe the cross-section of the joint. Figure 2.21(a) is the SEM image of the cross-section: the joint is closely packed and the sintered Ag layer is in the middle. The thickness of the sintered Ag layer is about 25 μm. A thin black layer can be observed between the sintered Ag and Cu surface. Figure 2.21(b) is the SEM image of this layer with high magnitude. The thickness of this black layer is about 500 nm. EDS analysis was also done on this layer, which shows in Table 2.1. Based on the mass ratio of element O and Cu, it appears to be Cu_2O layer. But in this layer there is also a huge mess amount of element Ag, which means that this black layer is a mixing layer of Cu_2O and sintered Ag. So by following Process-N_2, Cu surface will have a certain degree of oxidation, but it cannot form a dense layer of oxide to separate the sintered Ag with Cu, which means that sintered Ag and Cu can form bonds through the thin Cu_2O layer, or the Cu_2O layer was formed after the formation of Ag/Cu bonds. All the above discussions can explain why much stronger bonding can be achieved by following Process-N_2.

2.4 Summary of small area die-attachment on Cu surface

Nanosilver paste is a new type of lead free die-attachment, which is formulated by mixing organic dispersant, binder and thinner with nanoscale Ag particles. After going through a heating profile (< 275 °C), the organics in the paste can be totally burned off thus the nanoscale silver particles can go through the sintering process and form a dense microstructure. Low-

temperature sintering of nanosilver paste can realize small area die-attachment without applying any pressure. The processes of small area die-attachment on pure Cu surface had been developed. Two different methods were discussed in this chapter.

For method *I*: Sintering at negative air pressure generated by a pump, the average die-shear strength is below 10 MPa. With the increasing of P_{O2} from 0.04 atm to 0.14 atm, the die-shear strength increases first and then decreases at higher end. Peak strength can be achieved with sintering atmosphere P_{O2} = 0.08 atm. Microanalysis showed that at low P_{O2} condition (< 0.04 atm), the organics in the paste cannot be totally burned off. While at high P_{O2} (> 0.14 atm) condition, the Cu surface experienced heavily oxidation. Both of these two conditions caused low bonding strengths. Peak strength of condition P_{O2} = 0.08 atm is due to neither organic residue blocking sintering of particles, nor dense oxide layer blocking bond formation.

For method *II*: Introducing inert gas N_2 atmosphere during sintering. Process-N_2 was developed by setting the drying stage (< 180 °C) in pure N_2 and adding an airflow step at above 250 °C for about 30s with flow rate about 500 ccm. By following Process-N_2, the average die-shear strength can improve significantly to 24 MPa. Microanalysis showed that after shearing, a layer of sintered Ag layer was still attached on Cu substrate, which means that the failure surface is not the sintered Ag/Cu interface. A very thin Cu_2O and sintered Ag mixing layer can be observed at the interface, which cannot prevent the Ag/Cu bonding formation.

Chapter 3

Large area (> 3 mm × 3 mm) die-attachment on Cu surface by nanosilver LTJT

This chapter describes a process for attaching chips with large area (> 3 mm × 3 mm) onto pure Cu surface by low-temperature sintering of nanosilver paste. A review of large area die-attachment using nanosilver paste was given. For attaching large area chip, a low range of pressure (< 5 MPa) was needed due to the out-gassing of organics in the paste layer during sintering process. By applying pressure, much denser Ag layer can be achieved after sintering. In order to realize the large area die-attachment on pure Cu surface, a new double print process was developed. 6 mm × 6 mm dummy chips were attached on DBC with pure Cu surface to evaluate the bonding strength, which followed by the microanalysis of the sintered Ag layer. Since the samples were pressure sintered in the air, there was a certain degree of oxidation on the DBC substrate. In the whole process of module making, wire-bond is the following step after die-attachment. Wire-bond pull tests were done on the partially oxidized substrate in order to check the feasibility of this process in module making.

3.1 Large area die-attachment by low-temperature sintering of nanosilver paste

3.1.1 Challenges for large area die-attachment using nanosilver paste

The first challenge is from the organic burning off process. For nanosilver paste, there is a certain amount of organics, which need to be totally burned out by following the same sintering process as small area die-attachment. If the attaching area becomes larger (> 3 mm × 3 mm), the paste in the center of the area is much more difficult to be properly sintered. This phenomenon is clearly shown in Figure 3.1, which is a half-inch thick copper rod surface. The debond surface was in the sintered silver layer. A lot of dark-color organics were still left in the middle while the edge of it was much well sintered. This structure has much lower bonding strength compare to

small area attachment. Figure 3.2 shows the SEM images of different areas. In the poorly sintered paste area, the nanoscale silver particles in the paste still maintained as shown in Figure 3.2(a). But in the well-sintered paste area, obvious growth and densification can be seen as shown in Figure 3.2(b).

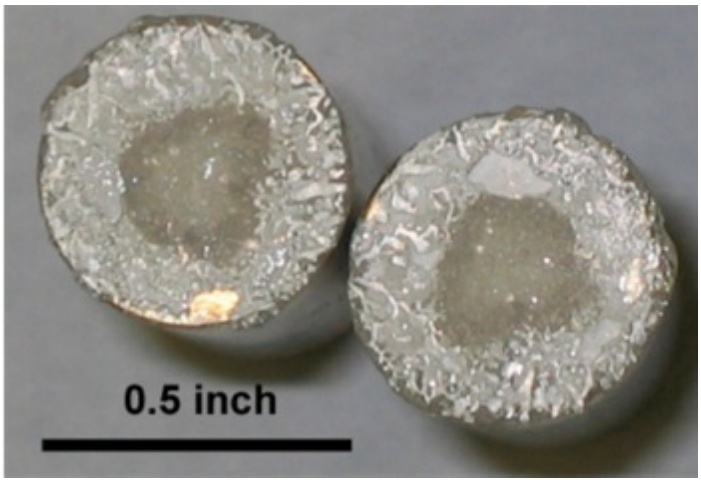
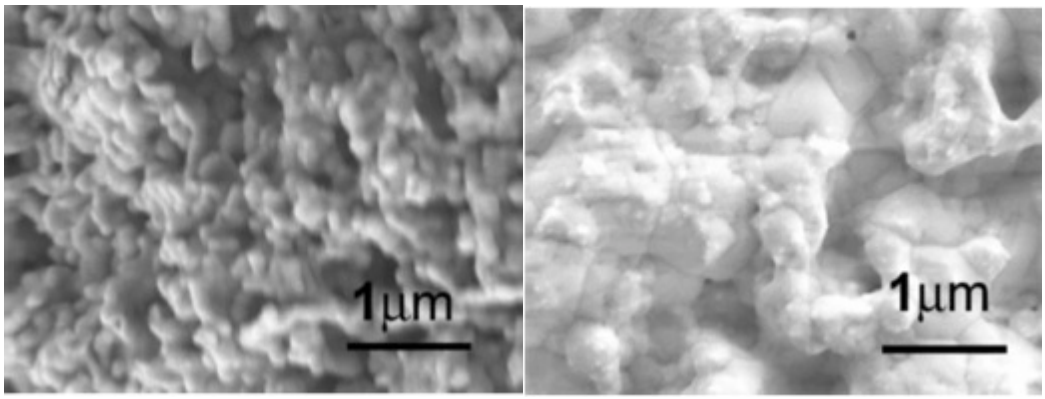


Figure 3.1 Low-temperature sintered nanosilver paste attaching half-inch thick rod surfaces after debonding.



(a) (b)

Figure 3.2 The comparison microstructures of (a) incomplete sintered nanosilver paste with (b) complete sintered area.

Another challenge for large area die-attachment using nanosilver paste is the density of sintered structure. The paste has out-gassing and shrinkage processes during the sintering. For large area attachment, the organics in the center need paths for burning off, which may also generate a pushing force against the chip, alone with the shrinkage of paste during drying, it would generate a loose structure, which will cause the low bonding strength. Figure 3.3 is an

optical image of nanosilver paste sintered underneath a 6 mm × 6 mm glass by following the same heating profile of small chip attachment, which shows a river like pattern.

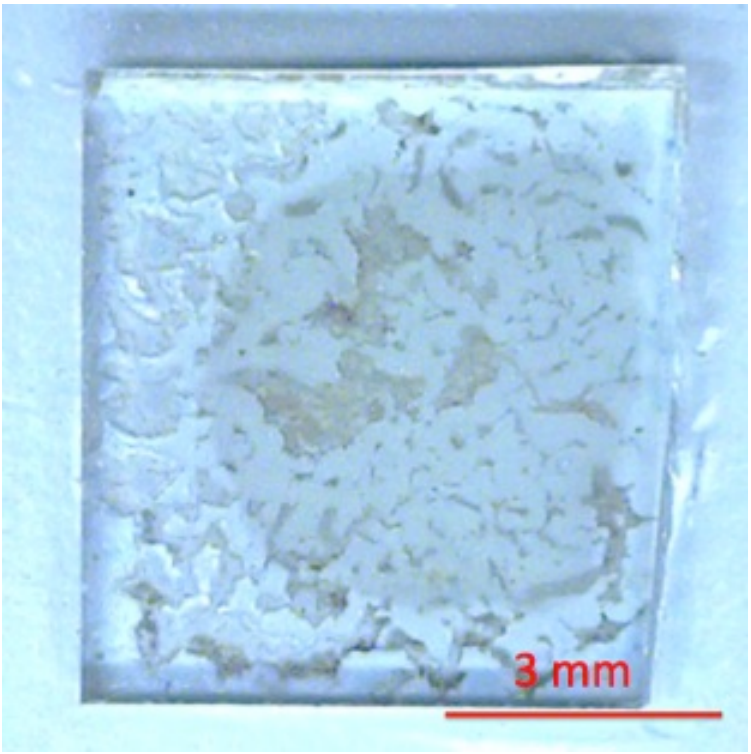


Figure 3.3 Optical image of nanosilver sintered underneath a 6 mm × 6 mm glass.

3.1.2 Process for large area die-attachment using nanosilver paste

In order to overcome these challenges, a double-print, low-pressure assisted sintering process was developed for large area die-attachment using nanosilver paste.

(a) Double-print process

This technique is for overcoming the first challenge: organic removal. The strategy is removing as much organics as possible before sintering step, which introduced as a double-print process as follows:

Firstly, a layer of nanosilver paste was stencil-printed onto a substrate to a thickness of 50 – 100 μm. The metal squeegee used for printing was shown in Figure 3.4(a). After first layer print, the sample went through an open drying step according to the profile in Figure 3.5. The peak drying temperature is 180 °C. After cooling down to room temperature, a thin second fresh paste layer of 5–10 μm was printed onto the dried first layer using the same stencil but a rubber

squeegee shown in Figure 3.4(b), which has a soft edge. This second layer acts as a wetting layer between the dried first layer and the chip, so it should be very thin. After second printing, the chip was mounted onto the wet layer. Then, the attached assemblies were ready for the sintering process.

(a) (b)

Figure 3.4 The squeegees used for stencil printing process: (a) metal squeegee; (b) rubber squeegee.

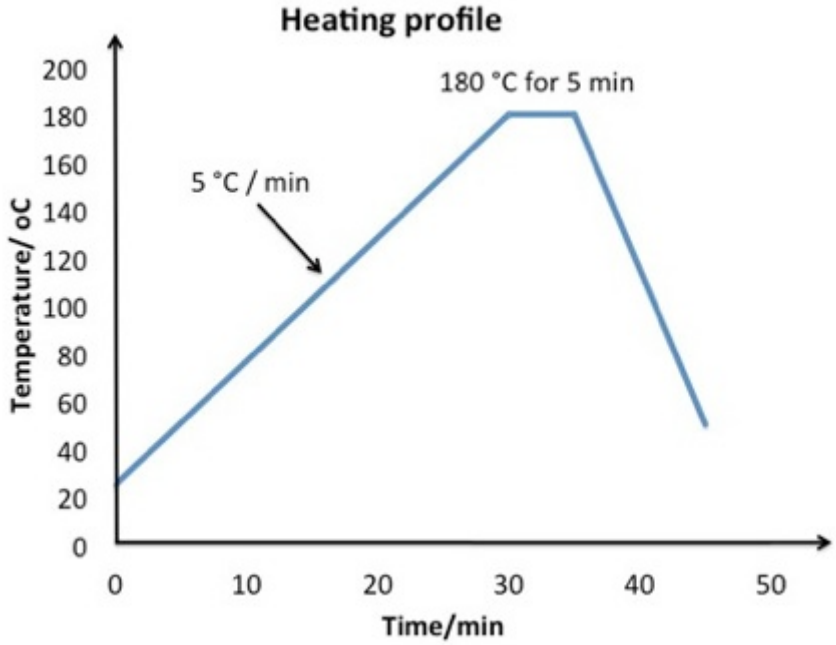


Figure 3.5 Designed heating profile for open drying step of first layer of paste.

(b) Low-pressure assisted sintering process

Low range pressure (< 5 MPa) was applied for the sintering of the assemblies. This technique is for overcoming the second challenge: loose structure. In the former study of large area die-attachment, a self-made hot press (Figure 3.6) was used to apply pressure during the sintering [53]. Hardened steel head was machined and polished to provide pressure. A force gauge was used to measure the peak force when shearing off the dummy chips from substrates. A temperature controller was setup to control the temperature, the heating rate, as well as the soaking time of the hot plate. The first thin print of paste can be sufficiently dried at 180 °C with the dried paste attaining sufficient hardness to resist deformation by pressures below 10 MPa. Besides, the wet second layer paste is very thin, after sintering no paste was squeezed out from the underneath of the chips. With the proper heating profile, the dried layer will also be essentially crack-free, an important condition since drying-induced defects will carry over into the sintered structure with correspondingly negative effect on the die-shear strength, and potentially the reliability. After the pressure assisted sintering, the joints were formed.

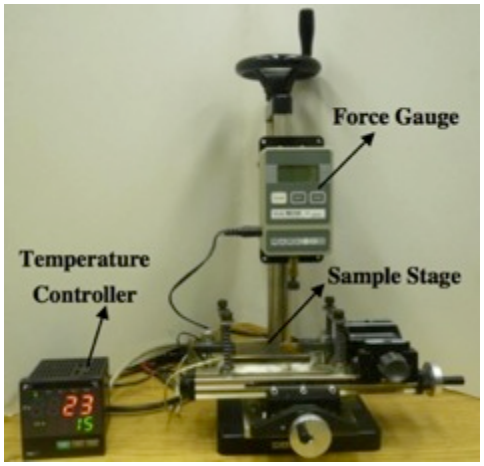


Figure 3.6 Self-made hot press for pressure assisted sintering of nanosilver paste.

3.2 Large area die-attachment on Cu surface by sintering of nanosilver paste

3.2.1 Process modifications for large area attachment on Cu surface

Since the objective is to attach large area chips directly onto pure Cu surface, the double-print method that was used successfully on Ag-coated surfaces needs to be modified for Cu

surface case, while the temperature was still kept at or below the previous sintering temperature range and a low range applied pressure was still maintained.

The key issue for large area die-attachment on pure Cu surface by this double-print, low-pressure assisted sintering is still preventing the oxidation on Cu surface. In order to get the same strong bonding as sintered joints on Ag coated substrate, two modifications were done on the process as follows:

First, the first layer of the printed paste needs to be dried in the pure N_2. Because the peak drying temperature is 180 °C, Cu surface would got an oxidation layer at such temperature if it is heated in the open air. Since the paste is only dried, the binders are still inside the paste, which separate the Ag particles and prevent them from sintering. After drying, no Ag/Cu bonds are formed. If the oxidation layer forms between the dried paste and pure Cu surface, further sintering step of paste is not able to form Ag/Cu bonds.

Second, fast heating rate was applied at the pressure assisted sintering step. If the process time can be shortened, the oxidation degree of Cu surface would be less. The best way to do it is applying the heat and pressure at the same time. The Carver hot press (Figure 3.7) was used for this case. There are two big hot plates in parallel, which are connected to temperature controller. And there is a pressure gauge for measuring the applied pressure during sintering. There are two hot plates, which can be pre-heated to the sintering temperature. Then the sample can be inserted between them and pressure can be applied on immediately. By this way, the oxidation degree of Cu surface can be minimized.

Figure 3.7 Carver hot press for pressure assisted sintering of nanosilver paste.

3.2.2 Sample making and evaluation tests

Pure Cu surface DBC substrates were cut into the dimension of 10 mm × 15 mm. The dummy chips were obtained from alumina substrates that were metalized with silver via physical vapor deposition and diced into 6 mm × 6 mm pieces by a wafer saw equipped with a diamond blade. Before attachment, the Cu surface of the DBC substrate was etched with dilute acid to remove the oxidation layer. Then both chips and substrates were ultrasonically cleaned in acetone and alcohol to remove organic contaminants. Samples of the chip and DBC substrate before attachment are shown in Figure 3.8.

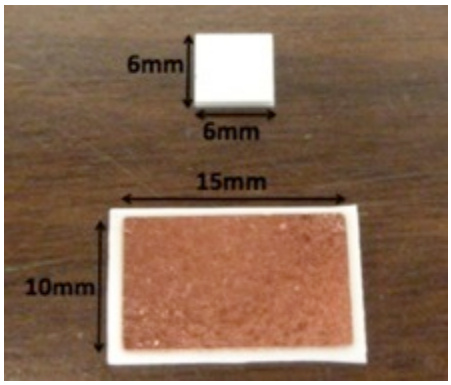


Figure 3.8 Dimensions of the dummy chips and DBC substrates for attachment.

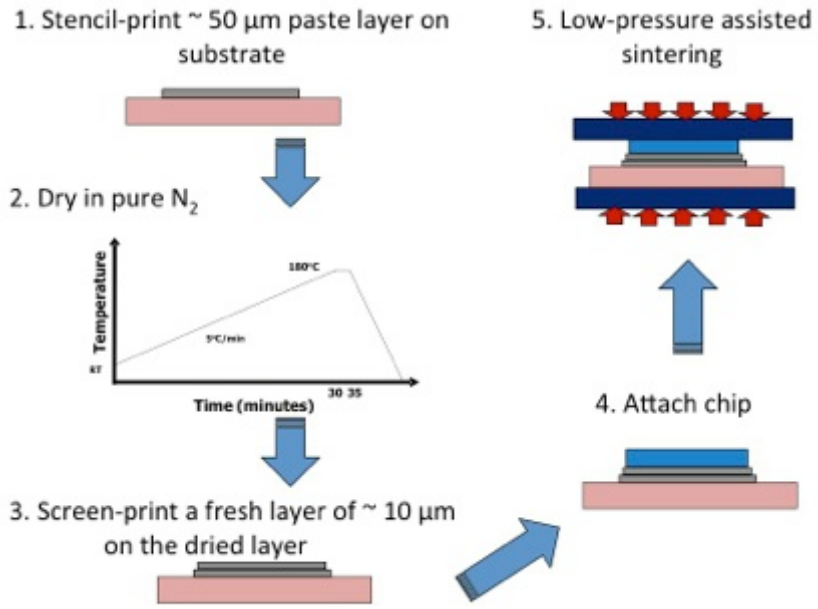
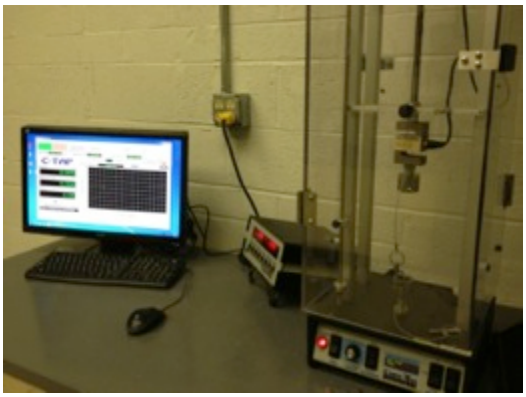


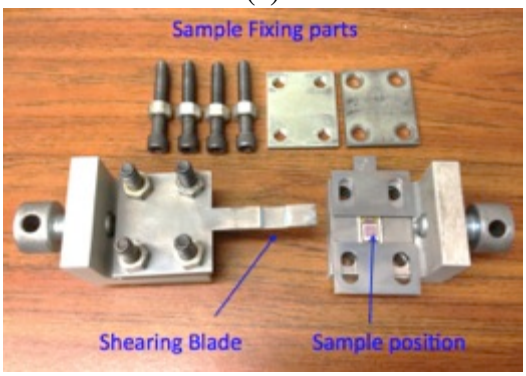
Figure 3.9 The double-print, pressure-assisted sintering process for 6 mm × 6 mm die-attachment on Cu surface.

Based on the discussion of 3.2.1, the total process for the attachment is illustrated in Figure 3.9. The double print process for attaching large area chips was applied. The first layer of paste, which was about 50 μm thick, was dried in the pure N_2 in the same setup for small area die-attachment (Figure 2.10). Then another wet layer (~ 10 μm) was printed on the dried first layer followed by chip mounting. The chip/substrate assembly was sintered at 275 °C in air for 5 min while under low pressure applied perpendicular to the joint surface with the Carver hot press. The hot plates were pre-heated to 275 °C, thus the heat and pressure were able to apply on the sample simultaneously. In order to even the pressure on the whole area of the chip, high temperature rubber was used as a cushion.

For different applied pressures (0, 1, 3, 5, 12 MPa), a set of 5 samples was made. The die-shear strengths of the attachments were measured by die-shear tests using a shearing fixture fitted to an Instron tensile tester, which are shown in Figure 3.10(a). The design of the fixture (Figure 3.10(b)) was made to impart essentially a pure shear force on the test sample joint layer. A simplified schematic of the test is shown schematically in Figure 3.11.



(a)



(b)

Figure 3.10 Equipment for large area die-shear test: (a) Instron tensile tester; (b) shearing fixture

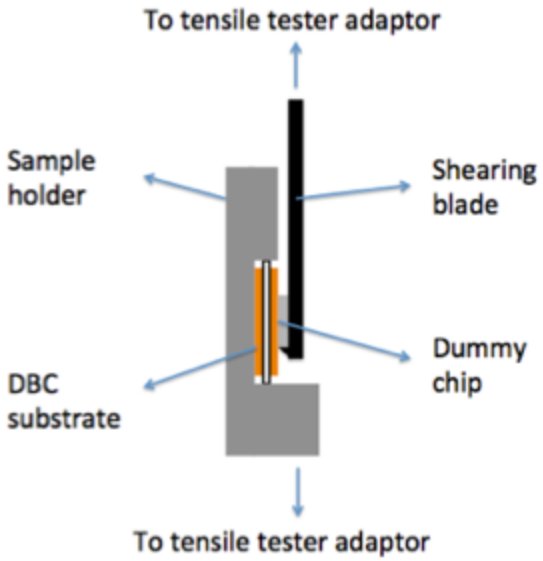


Figure 3.11 Schematic of 6 mm × 6 mm die-shear test

The shear test results for the different attachment fabrication parameters provided a feedback for determining the optimum attachment process. After that, silicon dummy chips were also attached to DBC with Cu surface by applying 5 MPa pressure during sintering. X-ray CT characterization was applied to Si dummy samples to nondestructively determine the internal structure of the silver joint layer. The fracture surfaces of the sheared off samples were observed by SEM imaging. To evaluate the effect and extent of oxidation on the exposed Cu area during sintering, 250 μm diameter aluminum wires were bonded to the copper surface and pull testing was performed.

3.3 Results and discussion

3.3.1 Die-shear strength

Figure 3.12 is a plot of the shear strengths of the alumina dummy chip / Cu surface attachments by sintering the nanosilver paste with applied pressure ranging from 0 MPa to 12 MPa. The average shear strengths are 7.6, 25.3, 40.3, 58.6 and 77.4 MPa for applied pressures of 0, 1, 3, 5 and 12 MPa, respectively. Corresponding error bars are also added upon the average strength. This plot clearly shows that the measured evolution of the shear strength as a function of applied pressure is significant. The results also show that beyond 5 MPa the increase in shear strength tapers off with only a small incremental gain per MPa.

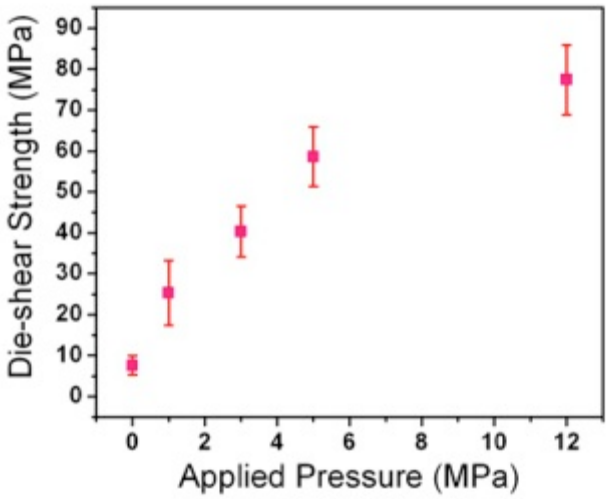
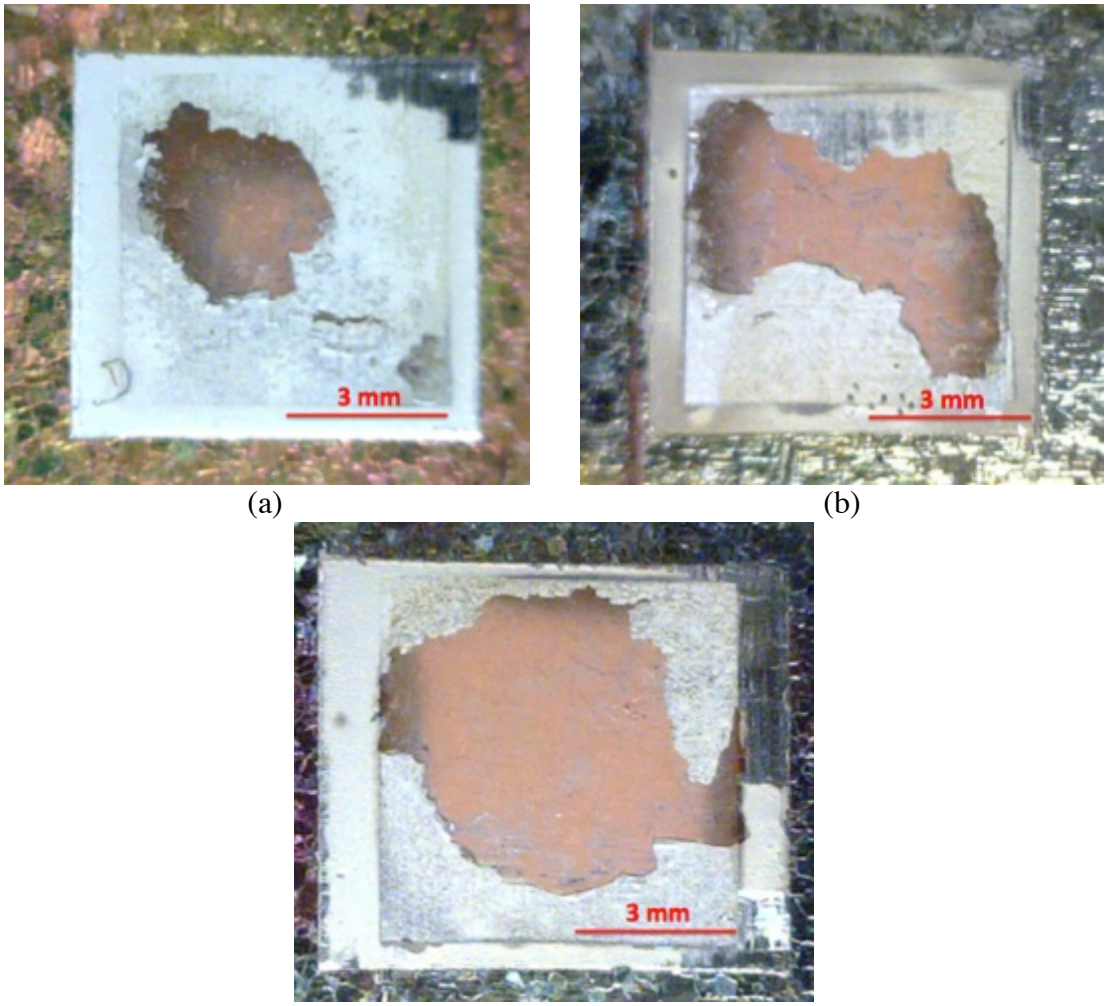


Figure 3.12 The die-shear strengths of 6 mm × 6 mm die-attachment on Cu surface sintered with different applied pressure.

If the objective is to simply match the typical die-shear strength of a solder attachment, e.g., 40 MPa, then the data shows that a pressure of a mere 3 MPa or even less is sufficient. When compared to the 40 MPa used in the original LTJT method, this is a huge improvement. The fact that it is possible to obtain these values by bonding directly on copper is also a significant improvement, because the same results can only be obtained on Ag-coated substrates previously. The die-shear strength is low for the 0 MPa condition. That is because there was a poor initial contact between the chip and dried first layer of paste, even though there was also a thin wet second layer. That bonding may not be closely packed without pressure during sintering. Typical failure surfaces of pressure-assisted sintered samples (1, 3, 5 MPa) after die-shear testing are shown in Figure 3.13. A trend can be observed in the mode of failure with increasing pressure. At lower pressure, the area of debond at the copper/sintered silver interface is smaller while it increases at higher applied sintering pressures. This trend also corresponds to increasing die-shear strength. The reason for this trend is that: when increasing the applied pressure, the sintered Ag layer would have denser microstructure. So the main weak link of the entire structure kept shifting from the inside the Ag layer to the Ag / Cu interface. During sintering, residual solvent and binder removal will advance from the outer edges to the center of the attachment area. Thus, the center will start developing strength later relative to the outer areas. This explains why delamination exposing the copper surface invariably occurs at the center, as it remains the weak point after sintering.



(a) (b)

(c)

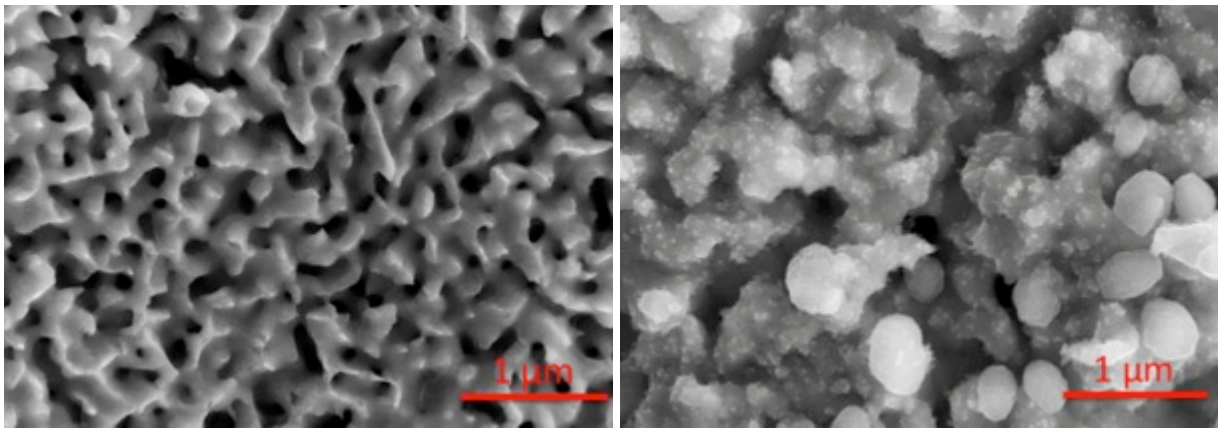
Figure 3.13 Typical die-shear failure surfaces of samples sintered with different assisted pressure: (a) 1 MPa; (b) 3 MPa; (c) 5 MPa

Applying pressure would have several possible effects on the sintering process and sintered joint. External pressure will force the silver particles closer together for increased connectivity (and therefore enhanced sintering) while also enhancing contact with the interface with the chip and copper. The sintered density would also increase with pressure as a result of the enhanced rearrangement of the particles. These effects would be manifested as an increase in the joint strength.

3.3.2 Microanalysis of the sintered Ag layer

Figure 3.14 shows the SEM images of typical failure surfaces after shearing. Figure 3.14(a) is a typical SEM image of failure surface of the pressure sintered Ag layer. Compare to

the Ag layer sintered without pressure (Figure 3.14(b)), the elongated structure is much more clearly, which correlates the larger shear force we need to apply when doing the die-shear tests. This means the microstructure is much denser for pressure assisted sintered samples. The failure is usually a mixed mode with both interfacial and cohesive (within joint layer) types. The failure surface on the Cu substrate does not reveal oxidation suggesting the Ag/Cu bond might be able to form before and have protected the Cu surface from oxidation, which is due to the fast heating rate and short sintering period.



(a) (b)

Figure 3.14 SEM images of the failure surface of sintered Ag layer: (a) sintered with 3 MPa pressure; (b) sintered without pressure.

With increasing pressure, the joint layer achieves higher density and strength such that the central interfacial debond area progressively increases as more of the failure shifts to interfacial failure at the Ag/Cu interface.

For the silicon dummy chips attached on the same DBC substrates, they were used to obtain images showing the uniformity of the joint layer non-destructively by X-ray CT scanning. Figure 3.15 is a typical X-ray imaging of the sintered attachment layer. No voids and cracks are visible confirming the sintered Ag layer is very uniform. It should be noted that this method could not directly provide evidence of interfacial debonding.

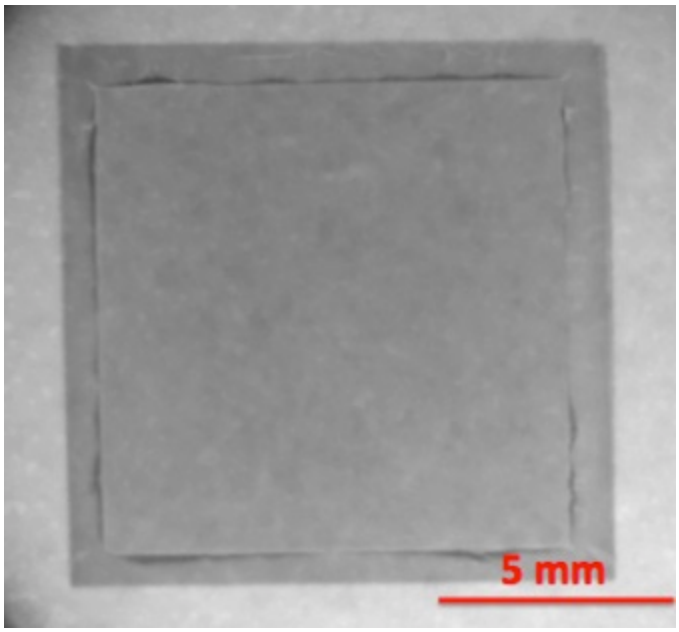


Figure 3.15 X-ray image of the sintered Ag attachment layer on Cu surface obtained by the double-print, pressure assisted sintering process.

3.3.3 Wire-bond quality test on partially oxidized Cu surface

The sintering process was done in air at 275 °C, which inevitably led to a certain oxidation of the exposed Cu surface. Since we used a rubber piece as a cushion when sintering, the pressure we applied would seal the unattached area of substrate surface at a certain degree. So the degree of the oxidation would not be comparable to a totally exposed surface.

For the process of module making, the following step of die-attachment is wire-bond. To qualitatively determine the extent of surface degradation by oxidation, fresh DBC substrates were put through the same conditions as the sintering process, and 250 μm thick aluminum wires were wire-bonded over the oxidized surfaces using a wire-bonder. Pull tests were performed following procedures in IPC-TM-650 standard [54] tests for wire-bond quality. Figure 3.16 shows the pull test fixture along with an oxidized DBC sample containing an array of bonded wires. This sample was wire-bonded using the same parameters as wire-bonded on the non-oxidized substrates. The bond failure mode and pull strength data of several samples are shown in Table 3.1. Based on the standard, the minimum requirement of the pull strength is 100 grams force for our 250 μm thick Al wires, which is shown in Figure 3.17. This is much more than met by this sample. The test confirmed that the degree of oxidation on the Cu surface after the die-

attachment process is not severe enough to prevent the attachment of wires with the necessary strength.

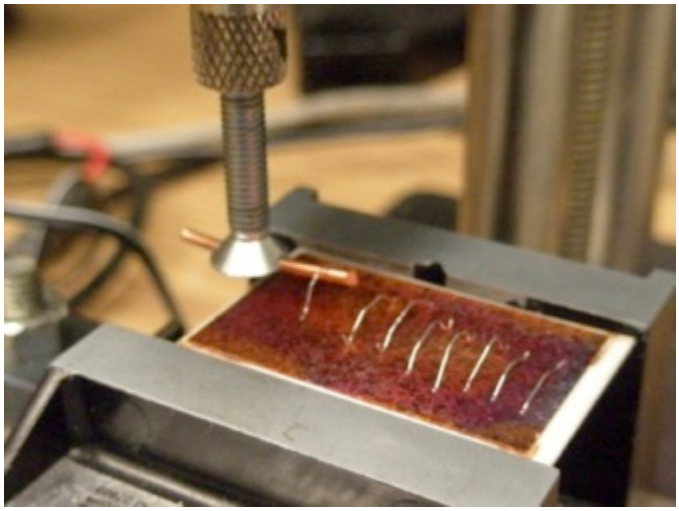


Figure 3.16 Schematic of pull test of the wire bonds on oxidized Cu surface.

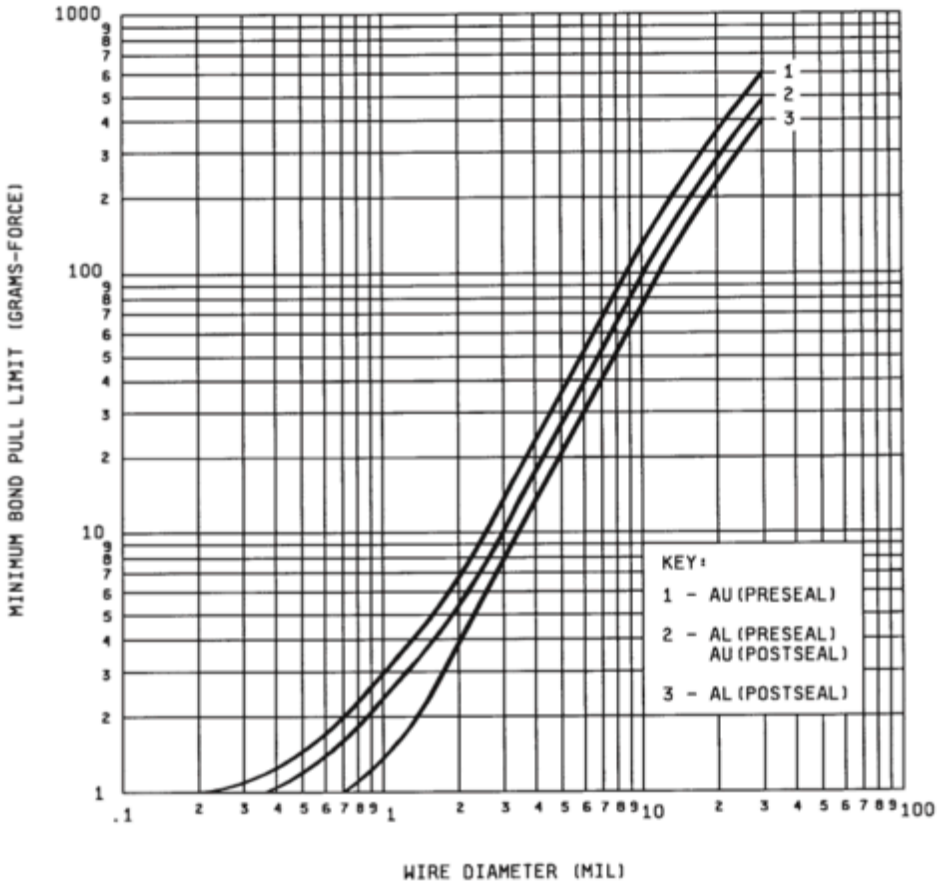


Figure 3.17 Minimum bond pull limits of different kinds of wires [54].

Table 3.1 Bond failure mode and pull strength data

Sample #	Failure mode	Break force (gf)
1	Bond lift off	408.6
2	Bond lift off	471.5
3	Wire break at bond	590.2
4	Bond lift off	499.7
5	Wire break at bond	511.4

3.4 Summary of large area die-attachment on Cu surface

The two challenges for the large area die-attachment are as follows: for the center of covered area, the organics in the paste is difficult to be burned off; the out-gassing of the organics burning off would form loose sintered Ag structure. In order to overcome these challenges, a double-print, low-pressure assisted sintering process was developed. By following this process, high quality joints can be obtained for the large area die-attachment on Ag-coated substrate.

In order to realize the large area die-attachment on Cu surface, two modifications of the process were needed: set the first layer paste drying step in pure N_2; speed up the sintering process. Thus a double print process for the attachment of large area chips on a pure copper surface with sintered nanoscale silver paste was demonstrated in this chapter.

Average shear strengths in excess of 40 MPa was obtained by applying only a 3 MPa pressure on a 6mm × 6mm chip during the sintering process. The resulting sintered Ag layer is very dense and uniform, with no cracks or voids visible in the X-ray images. While the copper on the rest of substrate partially exposed to air during sintering suffered oxidation, the degree of oxidation was not severe enough to prevent the formation of wire bonds that meet the IPC-TM-650 standard.

Chapter 4

Summary and future work

4.1 Summary

For the die-attach material, nanoscale silver paste was developed as a lead free alternative of traditional die-attach materials such as solder alloys. The sintered joints have much better high-temperature capability, as well as better thermal, electrical, and mechanical performance compare to solder joints.

This study focuses on the process development and evaluation of die-attachment on pure copper surface. Unlike the silver or gold metallized substrates, copper surface would suffer oxidation during the low temperature (≤ 275 °C) sintering process. Different processes were developed for small area and large area die-attachment on pure copper surface respectively.

4.1.1 Small area nanosilver LTJT on copper surface

Two different approaches were discussed for small area die-attachment on copper surface:

Method *I* was trying to use a mechanical pump to control P_{O2}. With P_{O2} ranging from 0.04 atm to 0.14 atm, die-shear strengths of dummy chips attached on copper surface increased first and then decreased after P_{O2} = 0.08 atm. At low P_{O2} condition (< 0.04 atm), there was not enough oxygen to burn off all the organics in the paste. While at high P_{O2} (> 0.14 atm) condition, oxidation layer is too thick so as to prevent the formation of strong bonding. P_{O2} = 0.08 atm is an optimized situation which neither organic residue blocking sintering of particles, nor dense oxide layer block bonding formation. However, the peak strength is still lower than 10 MPa.

Method *II* was trying to mix the inert gas N_2 for sintering. Process-N_2 was developed with modified gas mixing process for different heating stages. The drying stage (< 180 °C) was set in pure N_2 while adding an airflow step at above 250 °C for about 30 s. The average die-shear strength got a huge improvement to 24 MPa. Microanalysis showed the failure surface of shearing test was inside the sintered Ag layer rather than Ag/Cu interface. Which means the Ag/Cu bonds formed before the copper surface got oxidation.

4.1.2 Large area nanosilver LTJT on copper surface

For large area die-attachment, low range pressure (< 5 MPa) was necessary for generating a uniform sintered layer. Compare to the large area die-attachment on Ag-coated surface, copper surface would suffer from oxidation during the heating. Based on this concern, a modified process was developed: double print - first layer of paste with 50 μm thick was totally dried to 180 °C in pure N_2 to avoid the oxidation before bonding formation; second layer of paste with 10 μm thick to ensure the chip wetting, fast speed sintering combined with applying pressure was realized by a hot press.

Die-shear data shows the evident effect of applied pressure. Average die-shear strengths exceeded 40 MPa by applying 3 MPa pressure on a 6mm × 6mm chip during sintering, and it can get 77 MPa by applying 12 MPa. X-ray scanning of the sintered silver layer showed that there was no cracks or big voids. SEM images of failure surface after shearing showed much more elongated structure than non-pressure sintered silver layer, which explains the high shearing strength.

Due to the equipment difficulty of realizing pressure-assisted sintering in inert atmosphere, the rest area of copper substrate would exposed to air during sintering, thus lead to partially oxidation. The wire-bond ability test was performed on those areas. The degree of oxidation was not severe enough to prevent the formation of wire bonds based on the minimum requirement of IPC-TM-650 standard.

4.2 Future work

4.2.1 Reliability tests

Reliability is the biggest concern in electronics packaging manufacture. After applying different processes, the die-shear strength for the die-attachment on pure Cu surface is comparable to the number on Ag-coated surface. But there still may have oxidation issue when this kind of structure working at elevated temperatures. In order to test the reliability of die-attachment on pure Cu surface, high temperature Aging and thermal cycling tests are required.

4.2.2 Simulation

Although work has been reported about the simulation of die-attachment with solder joint, thermo-mechanical stress in the die-attachment with sintered-silver has not been studied. Simulation may be done on software like ANSYS. The simulation result can be compared with the observation in this work.

4.2.3 Module making

Due to the high performance and high density of the integrated circuits packaged in power modules, this technique become one of the tremendous interest in electronic technology. Considering the capability of die-attachment on pure Cu surface by sintering nanosilver paste, it is worthy of investigating the technique for processing power module by nanosilver LTJT and DBC substrates with Cu surface.

References

[1] R. R. Tummala, *et al*., *Microelectronics Packaging Handbook: Semiconductor packaging* vol. 2: Springer, 1997.

[2] J. Hornberger, *et al*., "A novel three phase motor drive utilizing silicon on insulator (SOI) and silicon-carbide (SiC) electronics for extreme environment operation in the army future combat systems (FCS)," in *IMAPS Proceedings*, 2004.

[3] J. G. Kassakian and D. J. Perreault, "The future of electronics in automobiles," in *Power Semiconductor Devices and ICs, 2001. ISPSD '01. Proceedings of the 13th International Symposium on*, , pp. 15-19, 2001.

[4] W. C. Nieberding and J. A. Powell, "High-temperature electronic requirements in aeropropulsion systems," *Industrial Electronics, IEEE Transactions on,* 1982, pp. 103-106.

[5] D. D. L. Chung, *Materials for electronic packaging*: Digital Press, 1995.

[6] C. Buttay, *et al*., "State of the art of high temperature power electronics," *Materials Science and Engineering: B,* vol. 176, pp. 283-288, 2011.

[7] J. Hornberger, *et al*., "Silicon-carbide (SiC) semiconductor power electronics for extreme high-temperature environments," in *Aerospace Conference, IEEE Proceedings*, vol. 4, pp. 2538-2555, 2004.

[8] R. R. Gomatam and E. Sancaktar, "Fatigue and failure behavior of silver-filled electronically-conductive adhesive joints subjected to elevated temperatures," *Journal of adhesion science and technology,* vol. 18, pp. 849-881, 2004.

[9] K. Suganuma, *Lead-free soldering in electronics: science, technology and environmental impact*: New York: Marcel Dekker, 2004.

[10] Altera Corporation, "Reflow soldering guideline for surface mount devices," http://www.altera.com/literature/an/an081.pdf.

[11] K. Kim, *et al*., "Effects of intermetallic compounds on properties of Sn-Ag-Cu lead-free soldered joints," *Journal of Alloys and Compounds,* vol. 352, pp. 226-236, 2003.

[12] E. Wood and K. Nimmo, "In search of new lead-free electronic solders," *Journal of Electronic Materials,* vol. 23, pp. 709-713, 1994.

[13] M. Abtew and G. Selvaduray, "Lead-free solders in microelectronics," *Materials Science and Engineering: R: Reports,* vol. 27, pp. 95-141, 2000.

[14] J. Arnold*, et al*., "Roadmap of lead-free assembly in north America," in *JiISSO/PROTEC Forum 2002*, Japan, 2002.

[15] U. Scheuermann and P. Wiedl, "Low temperature joining technology-a high reliability alternative to solder contacts," in *Workshp on Metal Ceramic Compsites for Functional Applicant*., Vienna, Austria, pp. 5, 1997.

[16] W. Kingery*, et al*., "Introduction to ceramics" *John Willey & Sons, NY*, 1976.

[17] D. W. Richerson, *Modern ceramic engineering: properties, processing, and use in design* vol. 29: CRC Press, 2006.

[18] A. I. H. Committee, *Engineered Materials Handbook: Ceramics and glasses* vol. 4: CRC Press, 1991.

[19] H. Schwarzbauer and R. Kuhnert, "Novel large area joining technique for improved power device performance," *Industry Applications, IEEE Transactions on,* vol. 27, pp. 93-95, 1991.

[20] H. Schwarzbauer and R. Kuhnert, "Novel large area joining technique for improved power device performance," in *Industry Applications Society Annual Meeting, Conference Record of the IEEE*, vol. 2, pp.1348-1351, 1989.

[21] R. Amro*, et al*., "Power cycling at high temperature swings of modules with low temperature joining technique," in *Power Semiconductor Devices and IC's, IEEE International Symposium on*, pp. 1-4, 2006.

[22] C. Goebl*, et al*., "Low temperature sinter technology die attachment for power electronic applications," in *Integrated Power Electronics Systems (CIPS), 2010 6th International Conference on*, pp. 1-5, 2010.

[23] U. Scheuermann and P. Beckedahl, "The road to the next generation power module - 100% solder free design," in *Integrated Power Systems (CIPS), 2008 5th International Conference on*, pp. 1-10, 2008.

[24] R. Eisele*, et al*., "Pressure sintering for thermal stack assembly," in *Proceedings of PCIM07*, Nurnberg, 2007.

[25] R. Amro, *et al*., "Double-sided low-temperature joining technique for power cycling capability at high temperature," in *Power Electronics and Applications, 2005 European Conference on*, Dresden, pp. 10, 2005.

[26] G. W. Scherer, "Sintering of low-density glasses: I, Theory," *Journal of the American Ceramic Society,* vol. 60, pp. 236-239, 1977.

[27] M. N. Rahaman, *Ceramic processing and sintering: 2nd edition*: Marcel Dekker, 2003.

[28] J. G. Bai, *et al*., "Low-temperature sintered nanoscale silver as a novel semiconductor device-metallized substrate interconnect material," *Components and Packaging Technologies, IEEE Transactions on,* vol. 29, pp. 589-593, 2006.

[29] Z. Zhang and G. Q. Lu, "Pressure-assisted low-temperature sintering of silver paste as an alternative die-attach solution to solder reflow," *Electronics Packaging Manufacturing, IEEE Transactions on,* vol. 25, pp. 279-283, 2002.

[30] G. Bai, "Low-temperature sintering of nanoscale silver paste for semiconductor device interconnection," Ph.D dissertation, Virginia Tech, Blacksburg, 2005.

[31] G. Q. Lu, *et al*., "A lead-free, low-temperature sintering die-attach technique for high-performance and high-temperature packaging," in *High Density Microsystem Design and Packaging and Component Failure Analysis, 2004. HDP '04. Proceeding of the Sixth IEEE CPMT Conference on*, pp. 42-46, 2004.

[32] J. G. Bai, *et al*., "Thermomechanical reliability of low-temperature sintered silver die-attachment," in *Thermal and Thermomechanical Phenomena in Electronics Systems, 2006. ITHERM '06. The Tenth Intersociety Conference on*, pp. 1126-1130, 2006.

[33] J. G. Bai and G. Q. Lu, "Thermomechanical reliability of low-temperature sintered silver die attached SiC power device assembly," *Device and Materials Reliability, IEEE Transactions on,* vol. 6, pp. 436-441, 2006.

[34] M. L. Minges, *Electronic materials handbook: packaging* vol. 1: CRC Press, 1989.

[35] *ASM Handbook: Vol 13: Corrosion*, ASM International, USA, 1987.

[36] C. Tan, *et al*., "Corrosion study at Cu-Al interface in microelectronics packaging," *Applied surface science,* vol. 191, pp. 67-73, 2002.

[37] K. S. Choi, *et al*., "Copper lead frame: an ultimate solution to the reliability of BLP package," *Electronics Packaging Manufacturing, IEEE Transactions on,* vol. 23, pp. 32-38, 2000.

[38] J. Ma, *et al*., "Trends and development of copper alloys for lead frame," *Journal of Functional Materials,* vol. 33, pp. 1-4, 2002.

[39] Changway Inc., information from www.changway.com.

[40] P. Johnston, "Printed circuit board design guidelines for ball grid array packages," *Journal of Surface Mount Technology,* vol. 9, pp. 12-18, 1996.

[41] J. Schulz-Harder, "Advantages and new development of direct bonded copper substrates," *Microelectronics Reliability,* vol. 43, pp. 359-365, 2003.

[42] J. Schulz-Harder and K. Exel, "Recent developments of direct bonded copper (DBC) substrates for power modules," in *Electronic Packaging Technology Proceedings, 2003. ICEPT 2003. Fifth International Conference on*, pp. 491-496, 2003.

[43] Z. Ying, "Study of copper applications and effects of copper oxidation in microelectronic package," *Theses Partial Fulfillment of MatE,* vol. 234, pp. 13-17, 2003.

[44] M. Lenglet and K. Kartouni, "Characterization of the initial stages of copper oxidation by optical absorption and photoluminescence," *Rev Metall CIT*, pp. 1637-1645, 1993.

[45] N. F. Mott and R. W. Gurney, *Electronic processes in ionic crystals*: Dover New York, 1964.

[46] O. Kubaschewski and B. E. Hopkins, *Oxidation of metals and alloys*: Butterworths, 1967.

[47] A. Seybolt, "Oxidation of metals," *Advance of physics*, vol. 12, pp. 1-43, 1963.

[48] Y. Ebisuzaki and W. Sanborn, "Oxidation kinetics of copper: An experiment in solid state chemistry," *Journal of Chemical Education,* vol. 62, p. 341, 1985.

[49] C. T. Chong, *et al*., "Investigation on the effect of copper leadframe oxidation on package delamination," in *Electronic Components and Technology Conference, 45th Proceedings,* pp. 463-469, 1995.

[50] J. G. Bai, *et al*., "Control of nanosilver sintering attained through organic binder burnout," *Journal of Materials Research,* vol. 22, p. 3494-3500, 2007.

[51] T. Wang, *et al*., "Low-temperature sintering with nano-silver paste in die-attached interconnection," *Journal of Electronic Materials,* vol. 36, pp. 1333-1340, 2007.

[52] J. G. Bai, *et al*., "Processing and characterization of nanosilver pastes for die-attaching SiC devices," *Electronics Packaging Manufacturing, IEEE Transactions on,* vol. 30, pp. 241-245, 2007.

[53] L. Jiang, "Thermo-mechanical reliability of sintered-silver joint versus lead-free solder for attaching large-area devices," M.S. Thesis, Virginia Tech, 2010.

[54] The Institute for Interconnecting and Packaging Electronic Circuits, "IPC-TM-650, Test methods manual".