Modeling and Simulation of Analog Devices using PRECISE

by

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Thesis submitted to the Faculty of the
Virginia Polytechnic Institute and State University
in partial fulfillment of the requirements for the degree of
Master of Science
in
Electrical Engineering

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July, 1988

Blacksburg, Virginia

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(ABSTRACT)

The design and development of computer models to simulate analog devices and their effects on circuit applications has been investigated at length. The focus of this research is the development of theoretical and computer models for discrete devices using the popular simulator PRECISE, PRogram for Evaluating Circuits in an Interactive Simulation Environment [3], using a new method for model construction.

This new method develops a model approximating the mathematics of the simulation via perturbations and iterations [19]. The models developed by the new method in each case yield a minimum simulation accuracy of 90 percent in circuit applications. In comparison, models developed by the conventional method, which uses measured data to complete physical constructs of SPICE 2G.6 [5], offer a lower accuracy for the same circuits. Hence, the new method is more effective than the old method and also much faster, since the model generation process is now automated and does not require time-consuming manual measurements and calculations spread out over a long period of time.

With further development, a computer model can also be developed for the theoretical model presented in this thesis for the Gallium Arsenide Metal Semiconductor Field Effect Transistor (GaAs MESFET) device using the same methodology that has been used to develop the computer model for the Bipolar Junction Transistor (BJT) device. Hence this research, in addition to developing a library of a hundred and fifty odd successful models in the PRECISE and SPICE formats for the diode and BJT, can also be used to develop a new model for the GaAs MESFET, which would make both PRECISE and SPICE easier and more user friendly as circuit simulators.

Acknowledgements

I take this opportunity to thank everyone who has contributed towards the completion of this thesis. I would especially like to thank Dr. A. A. Riad, my principal advisor, for the time she spent offering guidance, information, and suggestions to my work. I would like to thank other members of my graduate committee, Dr. J. G. Tront, for his advice on SPICE3 and suggestions to modeling approach, and Dr. S. M. Riad for his comments. Also, I take this opportunity to thank Mr. M. I. Hymes and Mr. R. J. Brown, both of the Allied-Signal Aerospace Company, Microelectronics and Computer- Aided Engineering Centers, without whose guidance and support this thesis could not have been completed.

I am deeply indebted to my friend and colleague M. Z. Khan for his help in preparation of this thesis.

Finally, I thank my mother for her unfailing admiration and support necessary for me to complete this work.

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Chapter I

INTRODUCTION

Discrete devices like the Bipolar Junction Transistor (BJT), Schottky diode or metal semiconductor (MS) diode and the Gallium Arsenide Metal Semiconductor Field Effect Transistor (MESFET) have many applications where digital switching is required. The effects that active semiconductor discrete devices have on a circuit's performance can be illustrated by computer simulation in the time domain. But the simulation process requires an accurate model of the device. Thus, the focus of this research is the development of a computer model for the Diode and the BJT, and a theoretical model for the GaAs MESFET.

Because of its general capabilities, interactivity and speed as well as excellent customer support, PRECISE Version 2.2 is chosen to be the computer package for simulating these devices. Chapter II examines the salient features of PRECISE and its ability to perform in an interactive simulation environment. The focus of the research then emphasizes the approach taken to model these devices.

The first component, the Diode, is modeled in Chapter III. This chapter also provides a brief description of the model format used in PRECISE. By examining the physical mechanism of the diode, various parameters are determined. These parameters are then used in the simulation and compared against actual datasheet parameters for that particular device. After verification, the diode model is placed in a central library of models for circuit simulation purposes.

The second component, the Bipolar Junction Transistor (BJT), is modeled as described in Chapter IV, using the same method outlined above. In this model, parameter values from laboratory measurements, such as I-V curves and C-V curves as described by Getreu [1], are also considered. After verification, the model is placed in a library for future use.

The third component, the Gallium Arsenide Metal Semiconductor Field Effect Transistor (MESFET), is described in Chapter V. In this model, various parameters such as those described by Curtice [14] have been used to determine the physical characteristics of the device. A computer model using these parameters and the methodology used to create other device models can be used to generate computer models for the MESFET. Also in this chapter, the BJT models are used to simulate an inverter circuit. Simulation results are compared to actual measured response times, obtaining a minimum accuracy of 85 percent for the BJT models. This method therefore shows positive signs for modeling effectiveness and accuracy.

Chapter VI summarizes the research work by comparing the model parameters to the actual devices and verifying the accuracy of the models generated by using the outlined methods. With automation, these methods can replace the conventional manual measurement method and thus simplify the use of PRECISE and other circuit simulators based on the Berkeley SPICE simulator, which is now an established standard for analog circuit simulation.

Chapter II

PRECISE AS A TOOL FOR ANALOG SIMULATION

2.1 *Introduction*

The ability to anticipate the performance of an analog circuit greatly assists the design engineer. But when many linear and nonlinear components add to the complexity of the network, an exact solution is usually impractical and hard to find. For such cases, particularly due to the large number of iterative calculations necessary, computers are used to simulate the circuits.

Computer simulation offers several advantages [1]. Simulation of prototype circuits can replace experimental 'breadboard' versions. Simulated prototypes can be monitored with or without stray circuit board capacitances and loading effects and these parameters can be compensated for in the actual design. Worst case and sensitivity analyses can be performed on simulated prototypes. Hence, circuit simulation simplifies design engineering to a large extent.

Various circuit simulation algorithms, such as, SPICE, PRECISE, and SABER have been developed for analog simulation. SPICE has been one of the most popular algorithms used by academicians due to its tradeoff between general capabilities for high computational speed for transient analysis. In the commercial world, PRECISE has been one of the most widely accepted analog simulators due to performance enhancements gained over SPICE, maintaining the same standard netlist format as SPICE, its ability to perform interactively, and the excellent customer support offered.

This chapter presents an introduction to the analog simulator PRECISE, an acronym for 'PRogram for Evaluating Circuits in an Interactive Simulation Environment' [3]. Theoretical as well as computer models have been developed by the author to generate accurate models of actual semiconductor devices, to be used in circuit simulation.

These models can be used both in typical as well as worst-case simulation runs. The chapter addresses the capabilities of PRECISE as compared to other popular simulators that are available. It also describes the work done by the author to make PRECISE much easier to use at the circuit level, and illustrates the importance of modeling and simulation in the commercial and research environment.

2.2 Importance of Modeling and Simulation

Without circuit modeling and simulation capabilities, computer-aided engineering (CAE) systems offer little more than a drafting aid. The difficulty of creating models, mistrust of existing models, and unfamiliarity with available software tools have often limited designers to the physical circuit breadboard as the only method of proving a design. Vendor backed IC models, powerful new simulation and modeling languages, and common standards for command syntax and definitions are now making software modeling and simulation the accepted approach [20].

Better understanding of the available software modeling approaches should help designers select the most appropriate simulation or analysis scheme. Ranging from the transistor to the subsystem level, models go under a wide range of names, both generic and proprietary. Some models are only for specific hardware; others are or will soon become universal. Many address the needs of hardware designers, and others cater to systems engineers. Above all, in the commercial world, evolving technology changes every week.

To perform simulation at the transistor or switch level requires a circuit description, but not necessarily a language. Simulation of analog circuits predates that of digital circuits by more than a decade, the most important of the simulators to start the analog simulation concept being Berkeley SPICE. Thanks to its popularity, the SPICE input format for circuit netlist descriptions is an established standard for low-level circuit descriptions.

Many companies now offer enhanced versions of SPICE, a popular one amongst them being PRECISE. This analog simulator was evaluated in performance against SPICE Version 2G.6 [5] and HSPICE Version 2G.47 [4]. Performance evaluation was done on a four hundred device Complementary Metal Oxide Semiconductor (CMOS) one bit stack and a CMOS operational amplifier. Simulations included transient analysis and a swept frequency analysis [22]. The performance criteria consisted of the following:

- **Accuracy:** Analytically, the results obtained with all three simulators were quite close. The same models were used in each case. Some minor differences were noted in device capacitance parameters. Gate to drain conductance and transconductance figures were within one percent.

- **Simulation Time:** The one bit stack simulation using PRECISE was forty percent faster than using HSPICE and nearly fifty percent faster than using SPICE. This simulation time difference is significant, considering that the total simulation time on SPICE was approximately five hours long, using a VAXStation 2000 standalone workstation. The time for the operational amplifier (opamp) frequency response simulation was a factor of two faster using PRECISE. The total simulation time was about one minute in this case.

- **Convergence:** Convergence problems were experienced with the stack circuit at -55 ° C using both HSPICE and SPICE. The convergence problem seemed to be alleviated on PRECISE. This result was encouraging and positive but not necessarily conclusive in view of the amount of time spent on the problem. The analog circuit exhibited convergence problems using HSPICE, and the iteration timestep had to be increased from 1 ps to 100 ps. Consequently, the resolution decreased in order to arrive at a solution.

- **Interactivity:** This feature is useful primarily for smaller simulations where the circuit can be quickly examined and the CPU time is short. It also allows one to check for syntax errors in the circuit file and to check for the correctness of circuit entry and certain commands without sending the entire job for simulation.

- **Batch Mode:** To run in batch mode, two files must be generated for PRECISE, and only one each for HSPICE and SPICE.

- **Other Features:** PRECISE hardcopy plot outputs can be supported on a number of plotters and printers, and plots can be viewed on a number of display devices. This facility is limited to fewer devices using HSPICE, and only to character plots using SPICE. This can prove to be a disadvantage for high resolution plots using HSPICE and SPICE. A color graphics enhancement is available for displaying results on PRECISE. This facility is not available on HSPICE and SPICE.

2.3 *Overview of PRECISE*

PRECISE is an interactive simulation software package for analog Integrated Circuit (IC) and system design [3,23]. It is a user friendly language expressed in engineering terms, making the program easy to use and learn. Interactivity and a built-in editor allow command corrections and circuit topology error corrections to be made easily.

Subcircuit and external file capabilities allow a modular or structured approach. These same features also enable the creation of shareable libraries containing commonly used cells, processes and devices. PRECISE also has the ability to run in batch mode.

From a simple circuit description, one can perform AC single point, temperature multipoint, DC single point and double sweep, AC frequency, Mixed domain, worst case, simple and transient Monte Carlo, noise, sensitivity, Fourier, distortion, parametric and transfer function analysis using PRECISE. Various output commands are available, including the ability to display currents and voltages, element and model values, plots, prints, probes and displays. Descriptive commands such as set, sim, gauss, random, tolerance and external model, subcircuit and function files are available. PRECISE can support a wide variety of models, including bipolar NPN and PNP transistors, JFETs, multiple level MOSFETs, diodes, and more recently, Gallium-Arsenide MESFETs and operational amplifiers.

2.4 Generating a PRECISE Netlist

Writing a netlist for an analog circuit essentially follows the same guidelines as SPICE. The circuit is described in terms of dependent and independent current and voltage sources, active and passive elements and devices in terms of nets and nodes. This process is outlined in more detail in the following sections.

2.4.1 Defining the Circuit

Before writing a netlist in the PRECISE format, the model should be defined for its specific function. A design of the circuit should be drawn on paper, specifying node numbers and element names. Node numbers must be integers or alpha names and the datum or ground node must be 0. Element names begin with a keyletter, i.e., R for resistors, V for voltage sources, Q for bipolar transistors, and so on.

2.4.2 Describing the Circuit

The next step is to describe the circuit to the computer system. This is done by using the editor. The filetype of the circuit description must be .CKT.

The first few lines can be comment lines preceded with a '*', which are ignored by PRECISE. As mentioned before, PRECISE recognizes an element by the first letter which is called the keyletter. If the element name begins with an R, we have a resistor, etc. Table 1 on page 9 lists the different elements and their respective keyletters. The keyletter can be followed by up to seven more characters. Table 2 on page 9 illustrates the file structure used within PRECISE.

Input is a free format. Accepted delimiters are blanks and commas. To continue a statement on the next line, the new line must start with a '+' to indicate continuation. Nodes can be numbered 0 thru 9999, having 1 to 8 alphanumeric characters. The ground node MUST be 0. Number fields have an integer or exponent format. They may be followed by a scale factor.

Table 1. Elements and Keyletters used in PRECISE

ELEMENT	KEYLETTER
Resistor	R
Capacitor	C
Inductor	L
Mutual Inductor	K
Transmission Line	T
Diode	D
Transistor	Q
JFET	J
MOSFET	M
GASFET	B
Voltage	V
Current	I
VCVS	E
VCCS	G
CCCS	F
CCVS	H
Subcircuit	X

Table 2. File structure used in PRECISE

FILENAME	DESCRIPTION
.CKT	Network Topology
.USE	Command File
.SUB	Subcircuits and Macromodels
.MOD	Model Descriptions
.FUN	Function Descriptions

The variables allowed in PRECISE are resistor, linear capacitor, independent voltage and current sources, MOSFET geometric values, transmission line values and model parameter values.

Table 3. Measurement Units used in PRECISE

MEASURE	UNITS
Capacitance	Farad
Charge	Coulomb
Conductance	Mho
Current	Ampere
Frequency	Hertz
Inductance	Henry
Phase	Degree
Power	Watt
Resistance	Ohm
Temperature	° C
Time	Second
Potential	Volt
Distance	Meter
Area	Meter^2

Table 4 illustrates scale factors used in PRECISE.

Table 4. Scale Factors Used in PRECISE

UNIT	SCALE FACTOR
T	1E12
G	E9
ME	1E6
K	1E3
MI	2.54E-5
M	1E-3
U	1E-6
N	1E-9
P	1E-12
F	1E-15

Scale factors may be upper or lowercase. However, it is advisable to keep them lowercase to avoid confusion with element keyletters.

Table 5 on page 11 illustrates the various output formats available in PRECISE.

Table 5. Output Formats in PRECISE

NAME	OUTPUT FORMAT
Node Voltages	V(n1) V(n1,n2)
Currents	I(elem) I(elem,n1)
AC Voltages	VM(n1) VP(n1) VR(n1) VI(n1) VDB(n1)
AC Currents	IM(vx) IP(vx) IR(vx) II(vx) IDB(vx)
Noise	INOISE(x) ONOISE(x) where x is R,I,M,P or DB
Distortion	HD2(x) HD3(x) SIM2(x) DIM2(x) DIM3(x) where x is R,I,M,P or DB
Element Value	E(elem)
Model Value	MD(mod,parm) Diode MQ(mod,parm) BJT MJ(mod,parm) JFET MM(mod,parm) MOS MB(mod,parm) GASFET

A comment may be incorporated in a .CKT file by inserting a '*' in the first column of a line. PRECISE simply ignores this line. A comment may not be the first line in a .MOD, .FUN, or .SUB file.

2.5 *Approach to Analog Device Modeling*

A typical semiconductor analog device is fabricated in a unique fashion, to enable the incorporation of various characteristics that enable it to function in a particular manner.

Modeling of devices to be used later in simulation and design has a twofold objective: A device can be modeled prior to fabrication to understand how it will behave under test conditions, and to ensure that it works theoretically. On the other hand, the modeled device can be used as a building block to enable the design of a circuit or a large subsystem and to test this circuit to check and verify functional behavior. Hence, it is imperative that an accurate representation of the device be available in model format. For the model generating process, each characteristic of the device needs to be incorporated into the model, to ensure satisfactory behavior that adheres to the datasheet parameters. In most circumstances, one finds that building a model for an analog device is a delicate process; at extreme conditions, devices do not behave as expected due to the parasitics involved. In such cases, certain 'forcing' elements are incorporated to make sure that the device behaves as expected.

The models are developed from datasheet parameters using an iterative process that the author has developed. This process offers a high degree of correlation between the manufactured device and the modeled device. The model generation process begins with the manufacturer's specification on device performance. These values are input to a program that the author has developed, that generates a model which can then be directly tested in PRECISE. Each device is then connected in test configurations and simulated. Wherever possible, the values are adjusted to give the best fit to the manufacturer's data.

The completed model is then placed in a device library. Access to the devices is made by the part name. PRECISE finds the model by looking for it in the library specified during a simulation.

2.6 Summary

From the numerous features described, it can be seen that PRECISE is a very powerful tool for analog circuit simulation as compared to other analog simulators with respect to simulation time, convergence, interactivity, and numerous other features that are available. With a large device library, these features can be utilized to their best to simulate prototype circuits without 'breadboard' experimentation prior to actual circuit fabrication.

With the incorporation of various parasitics that appear on an actual physical circuit board, worst case simulations can be performed and these parasitics can be accounted for in the actual circuit. Procedures for the process to generate an accurate diode model are described next in Chapter III. A total of sixteen parameters can be incorporated in the model building process. These parameter values allow PRECISE to be used as an enhanced tool for computer simulation.

Chapter III

DEVELOPMENT OF A DIODE MODEL

3.1 Introduction

In this chapter, the diode is modeled for simulation with PRECISE. The development of this model starts with the examination of the model definitions used for various devices within PRECISE (Section 3.2). This understanding is necessary in order to utilize each model accurately and to incorporate various temperature effects. The chapter then extends to explain the determination of the various PRECISE parameters for the diode model which are used to incorporate various nonlinear effects into the diode model (Section 3.3). Section 3.4 concludes the chapter with a summary discussion of the modeling technique.

3.2 Model Constructs used in PRECISE

The definition of an active element is a two step process. In the first step, the element node connections, geometries and the model name are described [3,5]. In the second step, the model associated with the model name in step one is defined. Creating a model definition consists of assigning user values to model parameters. These model parameters then determine the characteristics of the element.

In PRECISE there are two forms of model definitions: 1) the model line, and 2) the model file, which will be described in the following sections.

3.2.1 Model Line Format

MODEL mname type(pname1=pval1,...)

The Model line is stored in the circuit description file with the filetype .CKT. It specifies a set of model parameters that will be used by one or more devices. Mname is the model name, and it must match the mname on the element line. There are eight types of models as shown in Table 6.

Table 6. Model types available in PRECISE

TYPE	**ELEMENT**
NPN	NPN BJT model
PNP	PNP BJT model
D	Diode model
NJF	N-channel JFET model
PJF	P-channel JFET model
NMOS	N-channel MOSFET model
PMOS	P-channel MOSFET model
GASFET	GaAs MESFET model

The parameter values are defined by following the parameter name with an operator and the parameter value. Model parameters can also be assigned a user-defined variable or function.

3.2.2 Model File

The format for the model file is the same as the model line. The advantage here is that this file can be used in several circuit descriptions. The model definition need not be repeated, and user libraries can be created.

3.2.3 Temperature effects

Temperature effects can be provided for some model parameters. It is also possible to provide temperature dependent functions for model parameters. TNOM is an option. The default value is 27 °C or 300 °K, and this can be changed with the OPTIONS command. TNOM is the temperature at which the specified data is measured. TEMPDC is the simulation temperature. The default value is TNOM, and it can be changed with the SET command. It can also be swept over a range of values. VT is defined as kT/q (k is Boltzmann's constant, T is the temperature in Degrees Kelvin and q is the electron charge). This can be changed with the SET command, or can be swept. Changing VT changes TEMPDC and vice versa.

Temperature effects for some model parameters are included in PRECISE. It is also possible to write functions for these parameters, and to use this option, the command OPTIONS NOTEMP=2 must be used before any analysis. Failure to do this can lead to inaccurate results for some command sequences.

3.3 Physics of the Diode Model

The dc characteristics of the diode are determined by the parameters IS and N. Charge storage effects are modeled by a transit time TT, and a nonlinear depletion layer capacitance determined by the parameters CJO, VJ and M. Reverse breakdown is modeled by an exponential increase in the reverse diode current and is determined by the parameters BV and IBV [3,8,9,17,18].

The area factor used on the diode element line determines the number of equivalent parallel devices of a specified model. The ones that are multiplied by the area are marked with a '*', and the ones that are divided are marked with a '/' under the heading 'area' as shown in Table 7 on page 18.

The diode model includes reverse breakdown and depletion and diffusion charge storage elements for p-n junctions. The model is applicable to junction, Schottky-barrier and Zener diodes. The characteristics of a diode are modeled by two nonlinear capacitors, a resistor and a current source as shown in Figure 1 on page 19[9,11,17].

The model parameters determine the values of these components. The area factor used on the diode element line determines the number of equivalent parallel devices of a specified model. The constants that will be used throughout this discussion are listed in Table 8.

Table 8. Physical Constants used in the Diode Model

SYMBOL	DESCRIPTION	VALUE	UNITS
k	Boltzmann constant	8.62E-5	eV/K
q	Electron charge	1.602E-19	coulombs
T	Temperature	TNOM + 273	K
VT	Thermal voltage	kT/q	volts
NI	Intrinsic carrier concentration	1.45E10	cm^{-3}
eox	Permittivity of SiO_2	3.45E-11	F/meter
esi	Permittivity of *Si*	1.04E-10	F/meter

Table 7. Model Parameters used for the Diode Model

NAME	PARAMETER	UNITS	DEFAULT	EXAMPLE	AREA
IS	saturation current	A	10E-14	10E-14	*
RS	ohmic resistance	Ohm	0	10	/
N	emission coefficient	-	1	1.1	
TT	transit time	sec	0	0.1ns	
CJO	zero bias junction capacitance	F	0	2pf	*
VJ	junction potential	V	1	0.6	
M	grading coefficient	-	0.5	0.33	
EG	activation energy for temp. effect on IS	eV	1.11	1.11 Si 0.67 Ge	
XTI	saturation current temp. exponent	-	3.0	3.0	
KF	flicker noise coefficient	-	0	1E-16	
AF	flicker noise exponent	-	1	1	
BV	reverse breakdn voltage	V	∞	40	
IBV	current at breakdn voltage	A	10E-3	10E-3	
IK	forward knee current	A	0	10E-3	
IKR	reverse knee current	A	0	10E-3	
KMS	metal-semiconductor charge storage	0	1		

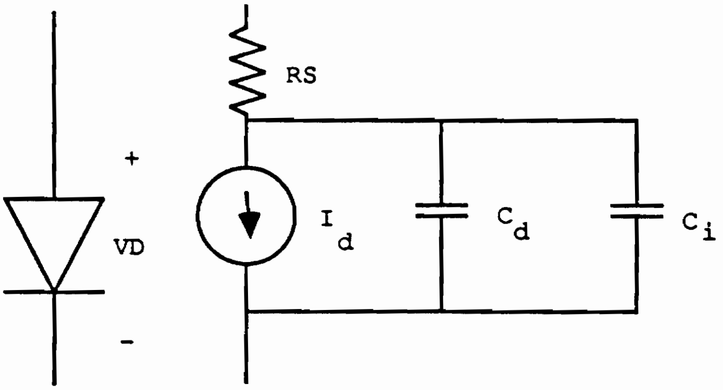

Figure 1. Equivalent Diode Model Implementation

3.3.1 Current Equation

The general current equation for the diode is described as a function of the saturation current [9]:

$$ID = IS(e^{VD/VTE} - 1) \qquad [3.1]$$

where

$VTE = NVT$

$N =$ emission coefficient

$VD =$ voltage across the diode

$IS =$ saturation current

3.3.2 Breakdown

Input parameters BV and IBV determine the I-V characteristics of the diode in the breakdown region [3].

If VD $<=$ -BV, the diode current is defined as:

$$ID = IS[e^{-(BV+BD)/VT} - 1 + \frac{BV}{VT}] \qquad [3.2]$$

where

$BV =$ reverse breakdown voltage ($>$ 0)

$VD =$ voltage across the diode

$IS =$ saturation current

In the breakdown region the diode current ID must be continuous. In order to satisfy this condition the diode current at breakdown, IBV′, must be equal to ID when VD = -BV.

$$IBV' = ID = IS\frac{BV}{VT} \qquad [3.3]$$

Hence, if IBV < IBV′, the program resets it to IBV′. If IBV > IBV′, the parameter BV is modified by the program to assure that IBV is the amount of current at breakdown, i.e., when VD = -BV. The problem becomes one of iteratively solving for BV such that when VD = -BV,

$$IBV = ID = IS[e^{-(BV+VD)/VT} - 1 + \frac{BV}{VT}] \qquad [3.4]$$

Substituting $VD = -BV_{n+1}$ in (3.4) and rearranging terms,

$$BV_{n+1} = BV_n - VT\ln(\frac{IBV}{IS} + 1 - \frac{BV_n}{VT}) \qquad [3.5]$$

where

BV_n = present value of BV

BV_{n+1} = Modified value of BV

Substitute BV_{n+1} in (3.1).

If $ID - IBV < RELTOL(IBV)$ then set $BV = BV_{n+1}$. Otherwise, the iterative process is repeated.

RELTOL is the relative tolerance used for iteration purposes in PRECISE.

The Diode I-V Characteristic is as shown in Figure 2 on page 22.

3.3.3 Knee Current

The ideal diode equation implies the same exponential increase in diode current with increasing forward voltage, independent of the level of current. For high levels of current density, the diode characteristic differs from the ideal curve. The program models this high level injection effect in terms of a knee current. The parameter IK models this effect in the

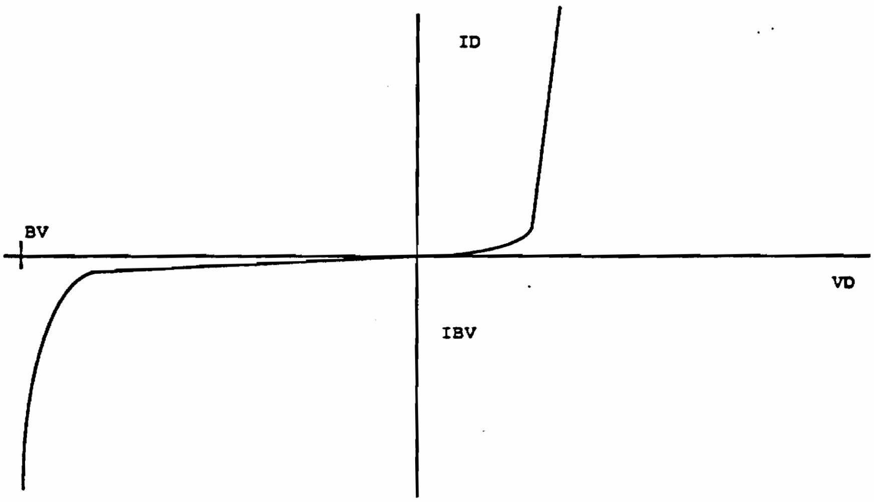

Figure 2. Diode I-V Characteristic.

forward region, and IKR models it in the reverse region. This current is the predicted ideal current at which the actual current is half the ideal current for that voltage.

In the forward region,

$$ID = \frac{IS(e^{V/VTE} - 1)}{1 + \frac{IS}{IK}(e^{V/VTE} - 1)} \tag{3.6}$$

In the reverse region,

$$ID = \frac{IS(e^{-VX} - 1 + \frac{BV}{VT})}{1 + \frac{IS}{IKR}(e^{-VX} - 1 + \frac{BV}{VT})} \tag{3.7}$$

where

$$VX = \frac{(BV + VD)}{VT}$$

IK, IKR and BV = input model parameters

3.3.4 Charge Storage

The parameters CJO, M, VJ, FC and TT control the charge storage characteristics of the diode [9]. In the diode there are two charge contributors, depletion and diffusion charges. When the diode is reverse biased, the depletion charge dominates. In the forward biased region, the diffusion charge dominates. The total capacitance is the sum of the depletion and diffusion charges.

3.3.4.1 Depletion Capacitance

If VD > FC*VJ, the depletion capacitance is:

$$Cd = AREA \times CJO(1 - \frac{VD}{VJ})^{-M} \qquad [3.8]$$

If FC*VJ > = VD, then:

$$Cd = \frac{AREA \times CJO}{(1 - FC)^{1+M}}[1 - FC(1 + M) + \frac{M \times VD}{VJ}] \qquad [3.9]$$

The depletion capacitance under reverse bias can be derived from dopant concentration using Poisson's equation [8,9]:

$$\frac{d\phi^2}{d^2x} = -\frac{\rho(x)}{e_s} \qquad [3.10]$$

where

ϕ = potential

e_s = permittivity of Si

$\rho(x)$ = dopant density

x_n = depth of depletion region, donor side

x_p = depth of depletion region, acceptor side

Integrating $\frac{d\phi^2}{d^2x}$ twice over the width of the depletion region we can derive an expression for depletion width as a function of the built in potential, VJ and the applied voltage, VD. We assume the electric field = 0 at $-x_p$ and x_n (i.e.,$\frac{d\phi}{dx} = 0$) and that the electric field and ϕ are continuous.

Assuming an abrupt junction dopant profile, M = 0.5 as shown in Figure 3 on page 25, we have

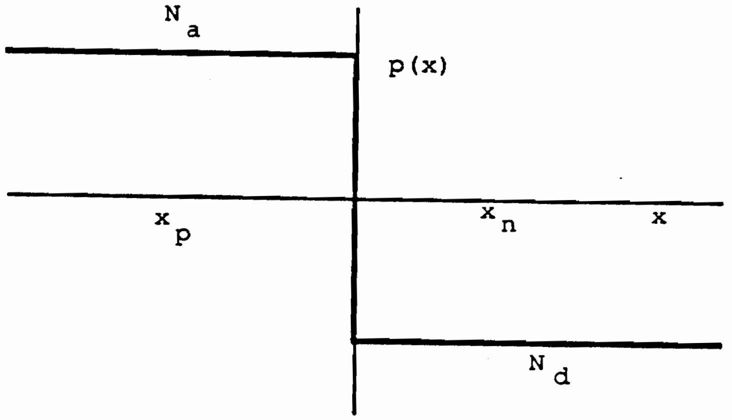

Figure 3. Abrupt Junction Dopant Profile.

$$\frac{d\phi^2}{d^2x} = -\frac{\rho(x)}{e_s} \qquad [3.11a]$$

$$\frac{d\phi^2}{d^2x} = -q\frac{N_d}{e_s}, \qquad 0 \le x \le x_n \qquad [3.11b]$$

$$\frac{d\phi^2}{d^2x} = q\frac{N_a}{e_s}, \qquad -x_p \le x \le 0 \qquad [3.11c]$$

Integrating and using boundary conditions that the electric field is zero at x_n and $-x_p$ yields:

$$\frac{d\phi}{dx} = -q\frac{N_d}{e_s}(x - x_n) \qquad [3.12a]$$

$$\frac{d\phi}{dx} = -q\frac{N_a}{e_s}(x - x_p) \qquad [3.12b]$$

Integrating again and using boundary conditions that at x_n, $\phi = \phi_n$ and at $-x_p$, $\phi = \phi_p$ yields:

$$\phi = -q\frac{N_d}{2e_s}(x - x_n)^2 + \phi_n \qquad [3.13a]$$

$$\phi = -q\frac{N_a}{2e_s}(x + x_p)^2 + \phi_p \qquad [3.13b]$$

Since ϕ is continuous at $x = 0$, we can derive the expression for the junction potential, the input parameter VJ.

$$VJ = \phi_n - \phi_p = \frac{q}{2e_s}(N_a x_p^2 + N_d x_n^2) \qquad [3.14]$$

Assuming the system is in equilibrium, $qN_a x_p = qN_d x_n$. We can solve for depletion width, $x_t = x_n + x_p$ by solving the equilibrium and junction potential equations simultaneously:

$$x_t = [\frac{2e_s}{q} \quad \frac{N_a + N_d}{N_a N_d} \quad VJ]^{1/2} \qquad [3.15]$$

Under back bias conditions, this becomes:

$$x_t = [\frac{2e_s}{q} \quad \frac{N_a + N_d}{N_a N_d} \quad (VJ - VD)]^{1/2} \qquad [3.16]$$

where

VD = back bias voltage

By definition of small signal capacitance,

$$Cd = AREA \times \frac{dQ}{dVD} \qquad [3.17]$$

where

$AREA$ = area of diode, an input parameter

Q = charge in depletion region

VD = reverse bias voltage

C = depletion capacitance

Since $Q = qN_d x_n = qN_a x_p$ [9],

$$\frac{dQ}{dVD} = qN_d \frac{dx_n}{dVD} = qN_a \frac{dx_p}{dVD} \qquad [3.18]$$

Using $x_p = (\frac{N_d}{N_a})x_n$ and (3.15) yields:

$$\frac{dx_n}{dVD} = \frac{1}{N_d} [\frac{e_s N_a N_d}{2q(N_a + N_d)(VJ - VD)}]^{1/2} \qquad [3.19]$$

Therefore,

$$Cd = AREA \times qN_d \frac{dx_n}{dVD} = AREA \times [\frac{qe_s N_a N_d}{2(N_a + N_d)(VJ - VD)}]^{1/2} \qquad [3.20]$$

Rearranging yields:

$$Cd = AREA \times CJO(1 - \frac{VD}{VJ})^{-1/2} \qquad [3.21]$$

where

$$CJO = [\frac{qe_s N_a N_d}{2VJ(N_a + N_d)}]^{1/2}$$

CJO is an input parameter, dependent on dopant profile and junction potential. For a linear junction dopant profile, M = 0.33.

$$CJO = [\frac{aqe_s^2}{12VJ}]^{1/3} \qquad [3.22]$$

where

a = slope of linear junction of dopant profile

For Metal Semiconductor Junctions [10], the depletion capacitance for Schottky diodes differs from that for p-n junctions. The parameter KMS models this effect:

$$CD = AREA \times CJO(1 - \frac{VD + KMS}{VJ})^{-1/2}, \qquad VD \leq FC \times VJ - KMS \qquad [3.23]$$

$$CD = \frac{AREA \times CJO}{(1 - FC)^{1-M}} \times [1 - FC \times (1 - M) + M \times \frac{(VD + KMS)}{VJ}], \quad VD > FC \times VJ - KMS \qquad [3.24]$$

The Depletion C-V Curve is illustrated in Figure 4 on page 29.

3.3.4.2 *Diffusion Capacitance*

The diffusion capacitance models the stored charge of the minority carrier under forward bias conditions. The charge is:

$$Q = TT \times I_d \qquad [3.25]$$

where

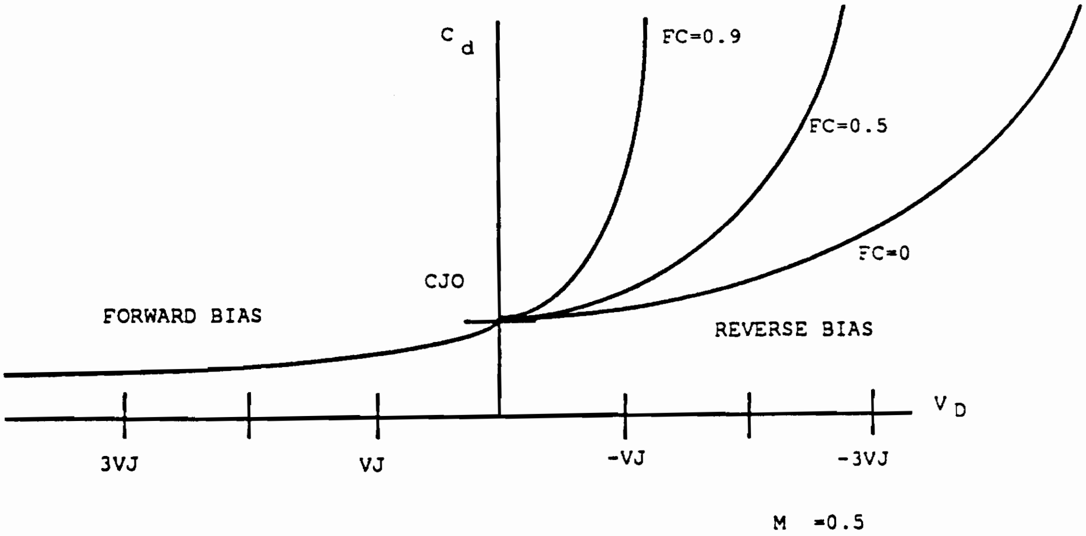

Figure 4. Depletion C-V Curve for Diode Model

$Q =$ charge

$TT =$ transit time, input model parameter

$I_d =$ diode current

Using the definition of small signal capacitance, C = dq/dv, we can solve for diffusion capacitance:

$$Ci = \frac{TT \times AREA \times IS}{VTE} \; e^{VD/VTE}, \qquad VD \geq -BV \qquad [3.26a]$$

$$Ci = \frac{TT \times AREA \times IS}{VT} \; e^{-(BV+VD)/VT}, \qquad VD < -BV \qquad [3.26b]$$

where

$VTE = N \times VT$

$N =$ emission coefficient, input parameter

$VD =$ voltage across diode

$IS =$ saturation current, input parameter

The Diffusion C-V Curve is as shown in Figure 5 on page 31.

3.3.5 Charge

In nodal analysis, all elements are represented by current sources and conductances. In the diode model, charge is used to derive equivalent conductance and current source for the capacitors. An expression for charge is derived by integrating the definition of small signal capacitance, C = dq/dv, from 0 to VD. Charge associated with depletion capacitance is [9]:

$$Qd = \frac{VJ \times AREA \times CJO}{1-M}\left[-1(1-\frac{VD}{VJ})(1-\frac{VD}{VJ})^{-M}\right], \qquad VD < FC \times VJ \qquad [3.27]$$

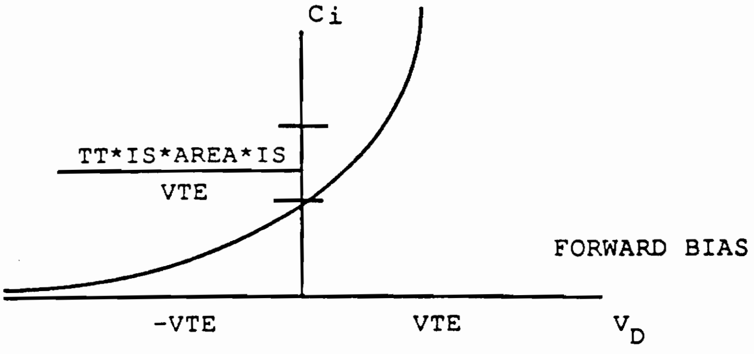

Figure 5. Diffusion C-V Curve for Diode Model

$$\begin{aligned} Qd = {} & AREA \times CJO \times F1 + \frac{AREA \times CJO}{F2} \times [F3 \times (VD - FC \times VJ)] \\ & + \frac{M}{2VJ}(VD^2 - FC^2 \times VJ^2) \end{aligned} \quad , \quad VD \geq FC \times VJ \tag{3.28}$$

where

$F1 = \frac{VJ}{1-M}[1-(1-FC)^{1-M}]$

$F2 = (1-FC)^{1+M}$

$F3 = 1 - FC \times (1+M)$

$AREA$ = area of diode

VD = voltage across diode

CJO = zero bias junction capacitance, input parameter

M = grading coefficient, input parameter

VJ = junction potential, input parameter

FC = coefficient for forward bias depletion capacitance

The charge associated with diffusion capacitance is:

$$Qi = TT \times I_d \tag{3.29}$$

where

TT = transit time, input parameter

I_d = diode current

3.3.6 Temperature Effects

Temperature dependence of the saturation current in the junction diode model is determined by:

$$Is = Is(T_o)\left(\frac{T}{T_o}\right)^{XTI/N} \times e^{\frac{qEG}{NK}\left(\frac{T-T_o}{TT_o}\right)} \tag{3.30}$$

where

N = emission coefficient

EG = activation energy

XTI = saturation current temperature exponent

T = present temperature

T_o = previous temperature

Note that for Schottky barrier diodes, the value of the saturation current temperature exponent, XTI, is usually 2.

CJO and VJ are temperature dependent due to internally calculated energy gap, Egi.

$$Egi = 1.16 - \frac{7.02 \times 10^{-4} \times T^2}{T + 1108} \qquad [3.31]$$

CJO and VJ are recalculated at each different temperature using the modified Egi.

$$VJ_1 = \frac{T}{T_o}(VJ_o + PBT_o) - PBT_r \qquad [3.32]$$

$$CJO_1 = CJO_o \times (1 + M) \times [400 \times 10^{-6}(T - T_r) + \frac{PBO - VJ_1}{PBO}] \qquad [3.33]$$

where

$$PBT = 2VTT \times (1.5\ln\frac{T}{T_r} + q\frac{egiT}{2VT(T)} + \frac{1.115}{2kT_r})$$

$$VT(T) = \frac{kT}{q}$$

$$egiT = 1.16 - \frac{7.02 \times 10^{-4} \times T^2}{T + 1108}$$

$$PBO = \frac{T_o}{T_r}(VJ_o + PBT_o)$$

VJ_o = value of VJ at previous temperature

T_r = reference temperature

CJO_o = value of CJO at previous temperature

3.3.7 Noise Model

The noise model for the diode is as shown in Figure 6 on page 35. The current source, i_{nrs}, models thermal noise generation in the ohmic region:

$$i_{nrs} = \left(\frac{4kT}{RS}\right)^{1/2} \qquad [3.34]$$

The current source, i_{nd}, models shot and flicker noise:

$$i_{nd} = \left(2qI_d + \frac{KF}{Freq}(I_d)^{AF}\right)^{1/2} \qquad [3.35]$$

where

$AF =$ flicker noise exponent, input parameter

$KF =$ flicker noise coefficient, input parameter

$Freq =$ frequency

The diode model parameters AF and KF are estimated from measurements of diode noise at low frequency. For Silicon diodes, KF = 1E-6 and AF = 1 typically.

3.4 Summary

The models developed by the method outlined in this chapter are as shown in Appendix C. A total of seventy nine commercial diodes are modeled for use in computer simulations involving functional circuits. A sample template file for general use in the PRECISE format is shown in Appendix A. This can be modified to suit the SPICE format by following the equivalent commands given in Appendix B. A test file to verify the current - voltage plot and the reverse recovery time for the diode models is also included in Appendix A. To avoid convergence

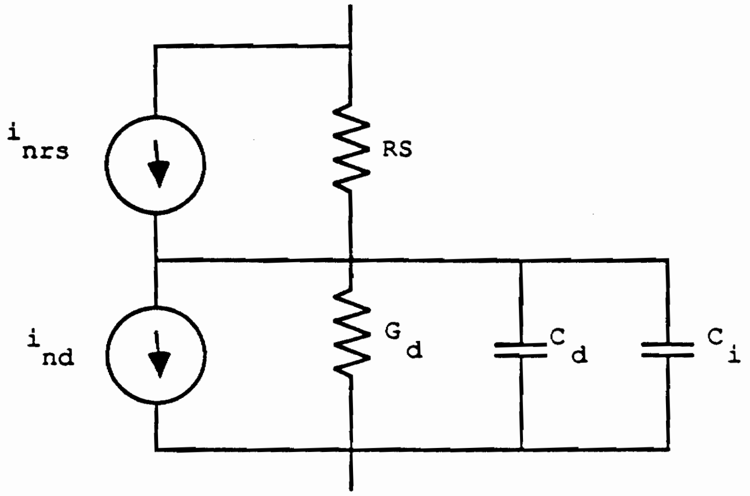

Figure 6. Noise Model for Diode.

problems that can arise while using the simulator, a set of OPTIONS commands have been included that prevent oscillations within the diode model. Chapter IV discusses the development of the BJT model, and the computer program generated to develop and store each model in the model library.

Thus, determination of the sixteen parameters allows the development of an accurate diode model that can be used for best and worst case simulations using either of the simulators that is based on the Berkeley SPICE standard.

Chapter IV

DEVELOPMENT OF A BIPOLAR JUNCTION TRANSISTOR MODEL - BOTH NPN AND PNP

4.1 *Introduction*

The bipolar junction transistor model is an adaptation of the integral charge control model of Gummel and Poon [12]. This modified model extends the original model to include several effects at high bias levels. The model will automatically simplify to the simpler Ebers-Moll model [6,12] when values for certain parameters are not included. The parameter names used in this modified Gummel-Poon model have been chosen to be more easily understood by the program user, and to better reflect both physical and circuit design concepts.

Section 4.2 explains the phycical constructs of the BJT model and the various parameters considered in modeling the dc characteristics of the BJT. In Section 4.3, the hybrid π parameters that are used to model the ac characteristics are explained. Section 4.4 explains the noise model. The chapter concludes with a summary in Section 4.5.

4.2 Physics of the BJT Model

The dc model is defined by the parameters IS, BF, NF, ISE, IKF and NE which determine the forward current gain characteristics, IS, BR, NR, ISC, IKR and NC which determine the reverse current gain characteristics, and VAF and VAR which determine the output conductance for forward and reverse regions. Three ohmic resistances RB, RC and RE are included which may be temperature dependent. RB can be high current dependent. Base charge storage is modeled by forward and reverse transit times, TF and TR, the forward transit time TF being bias dependent if desired, and nonlinear depletion layer capacitances which are determined by CJE, VJE, and MJE for the B-E junction, CJC, VJC, and MJC for the B-C junction and CJS, VJS, and MJS for the C-S junction [2,3,6,12,13].

The BJT parameters used in the modified Gummel-Poon model are listed in Table 9 on page 39 and Table 10 on page 40. The area factor used on the BJT element line determines the number of equivalent parallel devices of a specified model.

The characteristic of the BJT is modeled with three voltage dependent current sources, three nonlinear capacitors, two linear resistors, one nonlinear resistor and a diode. The ohmic resistance of the collector and emitter regions of the BJT are modeled by the two linear resistors RC and RE as shown in Figure 7 on page 41 [3].

4.2.1 DC Characteristics

The dc characteristics of the BJT are determined by twenty model parameters: IS, BF, NF, VAF, IKF, ISE, NE, BR, NR, VAR, IKR, ISC, NC, RB, IRB, RBM, RE, RC, ISS AND NSS [12]. The simple Ebers-Moll model is obtained by assigning values to the model parameters IS, BF, BR, RE, RB and RC and letting the rest of the model parameters assume default values. The integral charge model proposed by Gummel and Poon is obtained by assigning values for the

Table 9. Modified Gummel-Poon BJT Parameters

NAME	PARAMETER	UNITS	DEFAULT	EXAMPLE	AREA
IS	transport saturation current	A	1E-16	1E-15	*
BF	ideal max forward β		100	100	
NF	forward current emission coefficient		1	1	
VAF	forward Early voltage	V	∞	200	
IKF	corner for forward β high current roll-off	A	∞	0.01	*
ISE	B-E leakage saturation current	A	0	1E-13	*
NE	B-E leakage emission coefficient		1.5	2	
BR	ideal max reverse β		1	0.1	
NR	reverse current emission coefficient		1	1	
VAR	reverse Early voltage	V	∞	200	
IKR	corner for reverse β high current roll-off	A	∞	0.01	*
ISC	B-C leakage saturation current	A	0	1E-13	*
NC	B-C leakage emission coefficient		2	1.5	
RB	zero bias base resistance	Ohms	0	100	/
IRB	current where base resistance falls half of its min value	A	∞	0.1	*
RBM	min base resistance at high currents	Ohms	RB	10	/
RE	emitter resistance	Ohms	0	1	/
RC	collector resistance	Ohms	0	10	/
CJE	B-E zero bias depletion capacitance	F	0	2pf	*
VJE	B-E built in potential	V	0.75	0.6	
MJE	B-E junction exp. factor		0.33	0.33	
TF	ideal forward transit time	sec	0	0.1ns	
XTF	coefficient for bias dependence of TF		0		
VTF	voltage describing VBC dependence of TF	V	∞		

Table 10. Modified Gummel-Poon BJT Parameters

NAME	PARAMETER	UNITS	DEFAULT	EXAMPLE	AREA
ITF	high current parameter for effect on TF	A	0		*
PTF	excess phase at freq = 1/(TF*2pi) Hz	deg	0		
CJC	B-C zero bias depletion capacitance	F	0	2pf	*
VJC	B-C built in potential	V	0.75	0.5	
MJC	B-C junction exp. factor		0.33	0.5	
XCJC	fraction of B-C depletion cap connected to internal base node		1		
TR	ideal reverse transit time	sec	0	10ns	
TLEV	temperature model switch		0	0 or 1	
CJS	zero bias collector substrate cap	F	0	2pf	*
VJS	substrate junction built in potential	V	0.75	0.5	
MJS	substrate junction exponential factor		0	0.5	
XTB	forward and reverse β temperature exp.		0		
EG	activation energy for temp. effect on IS	eV	1.11		
XTI	temperature exp. for IS		3		
KF	flicker noise coefficient		0		
AF	flicker noise exponent		1		
FC	coefficient for forward bias depletion cap. formula		0.5		
ISS	substrate diode saturation current	A	0	1E-16	*
NSS	substrate diode emission coefficient		1	1.2	
TCCR1	tempco for collector resistor	C^{-1}	0	1E-3	
TCCR2	tempco for collector resistors	C^{-2}	0	1E-5	
TCBR1	tempco for base resistor	C^{-1}	0	1E-3	
TCBR2	tempco for base resistors	C^{-2}	0	1E-5	
TCER1	tempco for emitter resistor	C^{-1}	0	1E-3	
TCER2	tempco for emitter resistors	C^{-2}	0	1E-5	

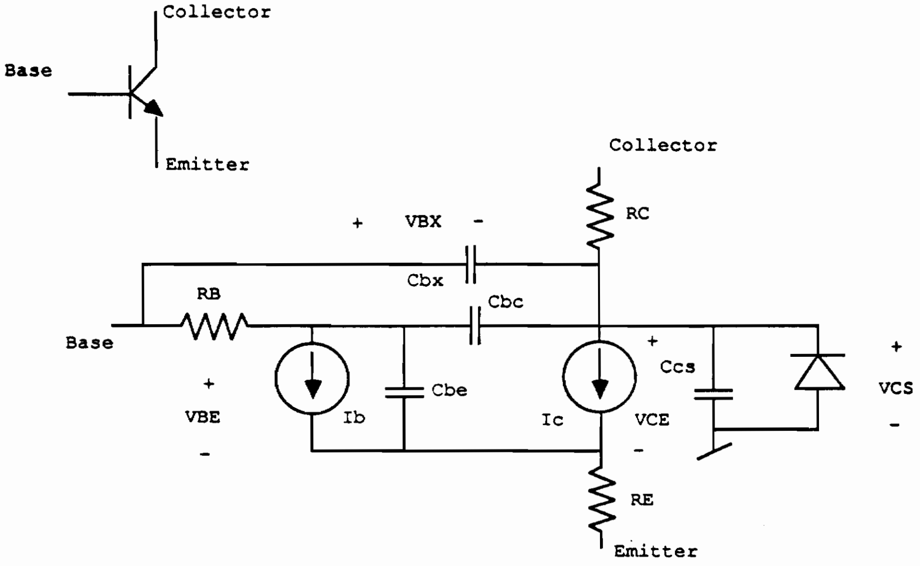

Figure 7. Equivalent BJT Representation.

Ebers-Moll model plus the parameters VAF, IKF, NE, ISE, VAR, IKR and ISC. The remainder of DC model parameters are used for additional model refinements.

4.2.2 Current Equations

The base current Ib and collector current Ic are determined by the following equations:

$$I_b = \frac{IBE}{BF} + IBEN + \frac{IBC}{BR} + IBCN \qquad [4.1]$$

$$I_c = \frac{(IBE - IBC)}{QB} - \frac{IBC}{BR} - IBCN \qquad [4.2]$$

where

$$IBE = IS \times AREA(e^{VBE/VT \times NF} - 1)$$

$$IBEN = ISE \times AREA(e^{VBE/VT \times NE} - 1)$$

$$IBC = IS \times AREA(e^{VBC/VT \times NR} - 1)$$

$$IBCN = ISC \times AREA(e^{VBC/VT \times NC} - 1)$$

$$QB = Q1 \times (1 + (1 + 4Q2)^{1/2})$$

$$Q1 = (1 - \frac{VBC}{VAF} - \frac{VBE}{VAR})^{-1}$$

$$Q2 = \frac{IBE}{IKF} + \frac{IBC}{IKR}$$

The base charge QB is the total majority carrier charge in the base region divided by the zero bias majority carrier charge:

$$QB = 1 + \frac{1}{VAF} \int_0^{VBE} \frac{\delta V}{(1 - V/VJE)^{MJE}} + \frac{1}{VAR} \int_0^{VBC} \frac{\delta V}{(1 - V/VJC)^{MJC}} \qquad [4.3]$$

$$-\frac{IS \times AREA}{QB \times IKF}(e^{VBE/VT \times NF} - 1) + \frac{IS \times AREA}{QB \times IKF}(e^{VBC/VT \times NR} - 1)$$

At zero bias equation (4.3) yields the result QB = 1. The integral terms model charge storage in the emitter and collector depletion regions, whereas the exponential terms model majority carrier excess charge in the base region. This excess majority carrier charge equals the injected minority carrier charge because of charge neutrality.

The equation for QB may be restated as the simpler equation:

$$QB = Q1 + \frac{Q2}{QB} \qquad [4.4]$$

Solving for QB yields:

$$QB = \frac{Q1}{2} + \frac{1}{2}\ (Q1^2 + 4Q^2)^{1/2} \qquad [4.5]$$

QB is further simplified to yield the approximate expression:

$$QB = \frac{Q1}{2} \times (1 + (1 + 4Q^2)^{1/2}) \qquad [4.5a]$$

Depletion layer charge storage in the base is accounted for by the Q1 component of the base charge. By definition, Q1 is unity at zero bias. This statement reflects the fact that the physical basewidth and the electrical basewidth are equal at zero bias. If both junctions are forward biased, the electrical basewidth is larger than the physical basewidth, and Q1 > 1. If both junctions are reverse biased, Q1 < 1 since the electrical basewidth is less than the physical basewidth.

Q1 is approximated by the equation:

$$Q1 = (1 - \frac{VBC}{VAF} - \frac{VBE}{VAR})^{-1} \qquad [4.6]$$

The relative significance of bias upon basewidth, and therefore base charge, is determined by the two parameters VAF and VAR. If VAF is assigned a value and VAR, IKR and IKF are defaulted, the collector current for the forward active region becomes:

$$Ic = IS \times AREA \times e^{VBE/VT \times NF} \times (1 - \frac{VBC}{VAF}) \qquad [4.7]$$

The small signal conductance, g_o, is proportional to Ic.

$$g_o \simeq \frac{Ic}{VAF} \qquad [4.8]$$

Because of the simplified representation of Q1, actual devices exhibit an output conductance slightly different from g_o. The output conductance is estimated at a particular operating point either from curve tracer measurements or from small signal measurements. Using the output conductance one may obtain a value for VAF as shown below. The graph of Ic versus VCE may also be used to directly obtain a value for VAF as shown in Figure 8 on page 45. The reverse early voltage, VAR, has an analogous role in the reverse region of operation.

The Q2 component of base charge accounts for the excess majority carrier base charge that results from injected minority carriers. This charge is defined by the equation:

$$Q2 = \frac{IBE}{IKF} + \frac{IBC}{IKR} \qquad [4.9]$$

Excess majority carrier base charge is insignificant until high level injection is encountered. If VAF and VAR are infinite and Ic is considerably smaller than IKF, then the collector current in the forward active region is approximately:

$$Ic = IS \times AREA \times e^{VBE/VT \times NF} \qquad [4.10]$$

If Ic is considerably larger than IK, then the collector current obeys the asymptotic relation:

$$Ic = IS \times AREA \times IKF \times e^{VBE/2VT \times NF} \qquad [4.11]$$

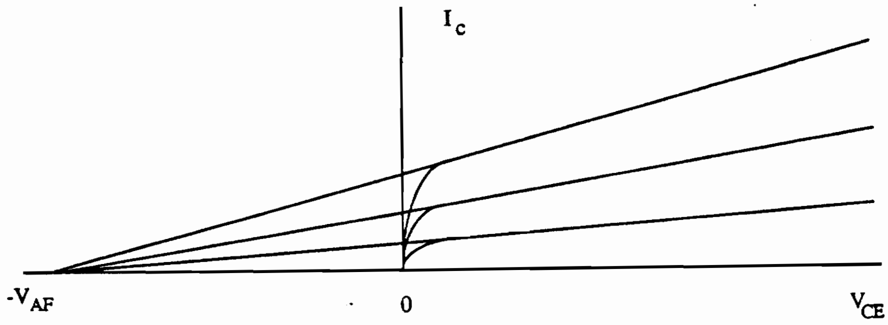

Figure 8. Graph of Ic versus VCE.

So the effective emission coefficient of the collector current changes from NF, in low level injection, to 2*NF, in high level injection.

The reverse knee current, IKR, has the analogous role in the reverse region.

The saturation current, IS, is related directly to the zero bias majority carrier profile in the base. The parameter IS is the extrapolated intercept current of the graph of log Ic versus VBE in the forward region, or of the graph of log Ie versus VBC in the reverse region. Experimentally, IS is usually estimated from several Ic, VBE points in the region of operation where Ic nearly obeys the ideal exponential characteristic. This is shown in Figure 9 on page 47.

The forward current gain, BF_{eff}, and the reverse current gain, BR_{eff}, are defined by the equations:

$$BF_{eff} = \frac{Ic}{Ib}, \qquad VBE > 0, VBC < 0 \qquad [4.12a]$$

$$BR_{eff} = \frac{Ie}{Ib}, \qquad VBE < 0, VBC > 0 \qquad [4.12b]$$

For the Ebers-Moll model BF_{eff} and BR_{eff} are independent of the operating point and are equal to the input parameters BF and BR [13].

The base current in the BJT consists of an ideal component which has an emission coefficient, NF, and a non ideal component which has an emission coefficient, NE, that typically ranges from 1.5 to 2. The non ideal base current, IBEN, results from depletion layer or surface recombination. The parameters ISE and NE determine the relative magnitude of IBEN in the forward region.

In the reverse region, NR has the same effect as NF in the forward region and NE and ISE determine the relative magnitude of IBCN.

The effect of the non ideal B-C component is illustrated as shown in Figure 10 on page 48.

The effect of the series resistances, RB and RE on the graph above have been omitted for simplicity. Therefore, the collector current is ideal with an inverse slope of 2.3*NF*VT. The base current is the sum of the ideal component, with the same inverse slope, and a non ideal

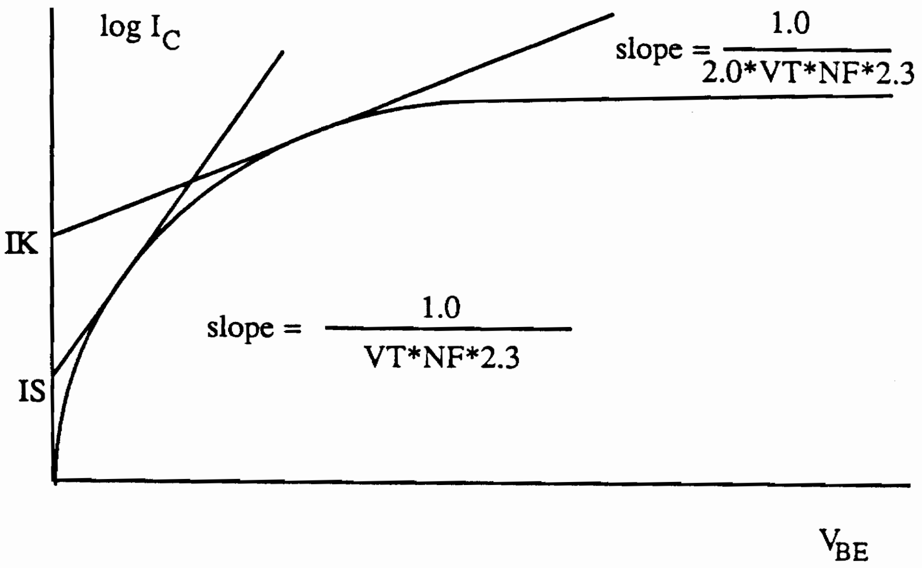

Figure 9. Graph of log Ic versus VBE.

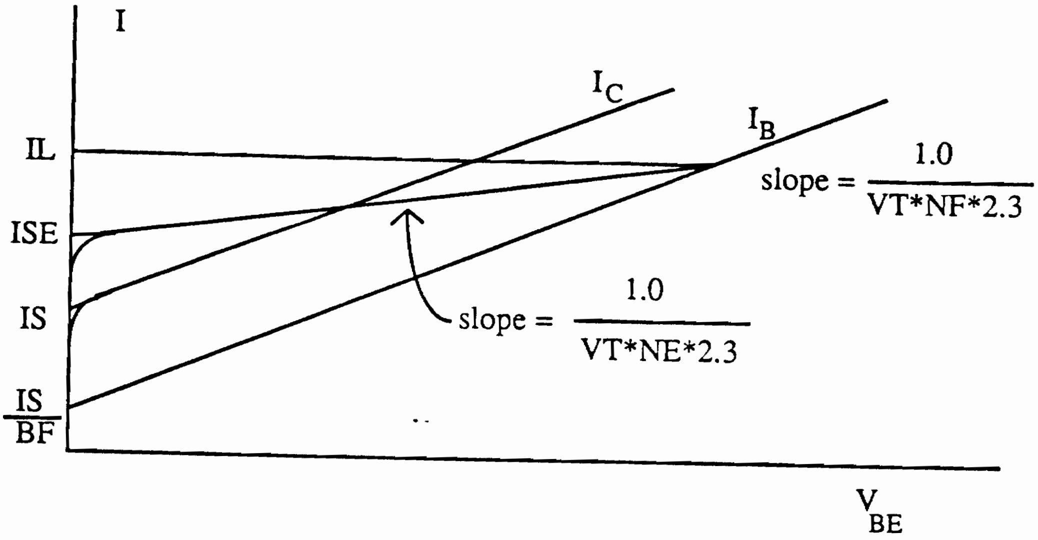

Figure 10. Effect of non ideal B-C component.

component with an inverse slope of 2.3*NE*VT. For small values of VBE, the non ideal component dominates the total base current. For larger values of VBE, the ideal component of base current dominates the total base current. The asymptotic breakpoint between non ideal and ideal base current region occurs when the collector current equals IL, where IL is given by the equation:

$$IL = ISE \times BF^{\mathrm{NE/NE-1}} \tag{4.13}$$

The effect of the non ideal component of base current is a drop in the common emitter current gain, BF_{eff}, at low levels of collector current. Asymptotically, BF_{eff} is constant at a value BF if the collector current is larger than IL. On the other hand, BF_{eff} decreases with a slope of (1 – 1/NE) if the collector current decreases below IL.

The parameters ISE and NE are determined from the graph of log I_b versus VBE in the forward region or are inferred from the graph of log BF_{eff} versus log I_c in the forward region. ISC and NC have the same role in the reverse region as ISE and NE in the forward region. This is illustrated in Figure 11 on page 50.

4.2.3 Base Resistance

Due to current crowding the base resistance, Rb, varies nonlinearly with current. The input parameters RB, IRB and RBM are used to define the base resistance Rb as follows:

$$\mathrm{Rb} = \frac{RBM}{AREA} + 3 \times RBI \times \frac{(Z2 - Z1)}{Z1 \times Z2^2} \tag{4.14}$$

where

$$RBI = \frac{\mathrm{RB}}{AREA} - \frac{RBM}{AREA}$$

$$Z1 = \tan Z2$$

$$Z2 = \frac{-1 + (1 + \frac{14.590 \times \mathrm{Ib}}{IRB \times AREA})^{1/2}}{2.432 \times (\frac{\mathrm{Ib}}{IRB \times AREA})^{1/2}}$$

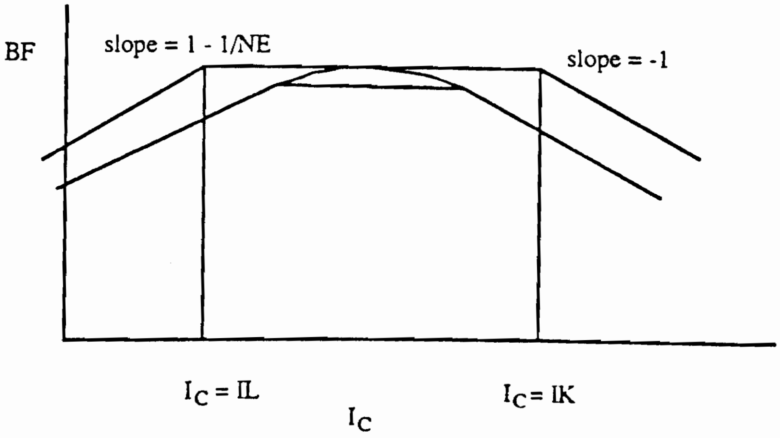

Figure 11. Determination of ISE and NE.

$AREA$ = area specified on element line

Note: If IRB has the value of zero then $\text{Rb} = \frac{RBM}{AREA} + \frac{RBI}{QB}$

4.2.4 Substrate Diode

In NPN transistors in integrated circuits, the p type substrate, n type collector and p type base form a parasitic PNP transistor [7]. This can cause a collector substrate current which is dependent on the base collector voltage. The parameters ISS and NSS model this effect. The current is given by:

$$ICS = ISS \times AREA \times (e^{VBC/VT \times NSS} - 1) \qquad [4.15]$$

where

VBC = internal B-C voltage

VT = thermal voltage

ISS = saturation current (> 0)

NSS = emission coefficient

If ISS is zero then this effect is not modeled.

4.2.5 Charge Storage

In the BJT model there are three areas of charge storage, the base emitter junction, the base collector junction and the collector substrate junction.

4.2.5.1 Base Emitter (B-E) Charge

The base emitter charge, Qbe, consists of two components, diffusion and depletion. The model parameters affecting the diffusion charge are TF, XTF, VTF and ITF. The model parameters affecting the depletion charge are FC, CJE, VJE and MJE [21].

If VBE < = 0,

$$Qbe = TF \times IBE + \frac{VJE \times CJE \times AREA}{1 - MJE} \quad (1 - (1 - \frac{VBE}{VJE})^{1-MJE}) \tag{4.16a}$$

If 0 < VBE < FC*VJE,

$$Qbe = TF' \times IBE + \frac{VJE \times CJE \times AREA}{1 - MJE} \quad (1 - (1 - \frac{VBE}{VJE})^{1-MJE}) \tag{4.16b}$$

If VBE > FC*VJE,

$$\begin{aligned} Qbe = TF' \times IBE + CJE \times AREA \times F1 + \frac{AREA \times CJE}{F2}(F3 \times (VBE - FC \times VJE)) \\ + \frac{MJE}{2VJE}(VBE^2 - FC^2 \times VJE^2) \end{aligned} \tag{4.16c}$$

where

$$TF' = TF \times [1 + XTF \times e^{VBC/VTF}](\frac{IBE}{IBE + ITF})^2$$

$$F1 = \frac{VJE}{1 - MJE}(1 - (1 - FC)^{1-MJE})$$

$$F2 = (1 - FC)^{1+MJE}$$

$$F3 = 1 - FC \times (1 + MJE)$$

$TF =$ input parameter TF, ideal forward transit time

$QB =$ defined under current equations

$IBE =$ defined under current equations

$VBE =$ B-E voltage

$AREA =$ area from the element line

Note: The input model parameter VTF defaults to infinity in which case the expression $e^{VBC/VTF}$ becomes 1. The input model parameter ITF defaults to 1.

4.2.5.2 *Base Collector (B-C) Charge*

The base collector junction charge also consists of two components, diffusion and depletion. To model the non-uniform charge distribution and current crowding, the depletion component of charge is distributed across the base to collector junction by the model parameter XCJC. XCJC must be greater than zero but less than one. Other model parameters affecting the depletion components are FC, CJC, MJC and VJC. The model parameter affecting the diffusion charge component is TR.

If VBC < FC*VJC,

$$Qbc = TR \times IBC + \frac{VJC \times CJC \times AREA \times XCJC}{1 - MJC} \times (1 - (1 - \frac{VBC}{VJC})^{1-MJC}) \qquad [4.17a]$$

If VBC > = FC*VJC,

$$\begin{aligned} Qbc = {} & TR \times IBC + CJC \times AREA \times XCJC \times (F1 + (\frac{F3}{F2}) \times (VBC - FC \times VJC)) \\ & + \frac{MJC}{2 \times VJC}(VBC^2 - FC^2 \times VJC^2) \end{aligned} \qquad [4.17b]$$

To model the non uniform charge distribution the collector capacitor is distributed. One charge element is connected from the internal base node to the internal collector node, described above in the depletion portion of the Qbc term. The other charge element, Qbx, is connected from the external base node to the internal collector node and is controlled by the voltage VBX. VBX is the voltage from the external base to the internal collector. Qbx is defined as follows:

If VBX < FC*VJC,

$$Qbx = \frac{VJC \times CJC \times AREA}{1 - MJC} \times (1 - XCJC) \times (1 - (1 - \frac{VBX}{VJC})^{1-MJC}) \qquad [4.17c]$$

If VBX > = FC*VJC,

$$Qbx = CJC \times AREA \times (1 - XCJC) \times (F1 + \frac{F3}{F2}(VBX - FC \times VJC)) + \frac{MJC}{2 \times VJC}(VBX^2 - FC^2 \times VJC^2) \qquad [4.17d]$$

where

$F1 = \frac{VJC}{1 - MJC}(1 - (1 - FC)^{1-MJC})$

$F2 = (1 - FC)^{1+MJC}$

$F3 = 1 - FC \times (1 + MJC)$

$IBC =$ defined under current equations

$VBC =$ B-C voltage

$AREA =$ area specified in element line,

4.2.5.3 *Collector Substrate (C-S) Charge*

The collector to substrate charge is modeled as a depletion charge. The input model parameters affecting the depletion charge are VJC, CJS and MJS.

If VCS < 0,

$$Qcs = \frac{VJS \times CJS \times AREA}{1 - MJS}(1 - (1 - \frac{VCS}{VJS})^{1-MJS}) \qquad [4.18a]$$

If VCS > = 0,

$$Qcs = VCS \times CJS \times AREA \times (1 + \frac{MJS \times VCS}{2 \times VJS}) \qquad [4.18b]$$

where

$VCS =$ voltage from collector to substrate

$AREA =$ area specified in the element line

4.2.6 Capacitance

Using the definition of capacitance, C = dq/dv, we can generate the capacitance equations by differentiating the charge terms, equations (4.16), (4.17), and (4.18).

4.2.6.1 Base Emitter (B-E) Capacitance

The model parameters affecting the base to emitter diffusion capacitance are TF, XTF, VTF and ITF [21].

The model parameters affecting the base to emitter depletion capacitance are FC, CJE, VJE and MJE.

If VBE < = 0,

$$Cbe = \frac{TF \times IS \times AREA}{VT \times NF} e^{VBE/VT \times NF} + CJE \times AREA \times (1 - \frac{VBE}{VJE})^{-MJE} \tag{4.19a}$$

If 0 < VBE < FC*VJE,

$$\begin{aligned} Cbe = {} & \frac{TF}{QB} \times \frac{IS \times AREA}{VT \times NF} e^{VBE/VT \times NF} \times (1 + XFTe^{VBE/VTF} \times (\frac{IBE}{IBE + ITF}))^{2} \\ & \times (3 - \frac{2 \times IBE}{IBE + ITF}) - IBE \times Qx + CJE \times AREA \times (1 - \frac{VBE}{VJE})^{-MJE} \end{aligned} \tag{4.19b}$$

where

$$Qx = Q1 \times \frac{QB}{VAR} \times \frac{IS \times AREA \times e^{VBE/VT \times NF}}{VT \times NF \times IKF(1 + 4(\frac{IBF}{IKF} + \frac{IBC}{IKR}))^{1/2}}$$

If VBE > FC*VJE,

$$\begin{aligned} Cbe = {} & \frac{TF}{QB} \times \frac{IS \times AREA}{VT \times NF} e^{VBE/VT \times NF} \times (1 + XFTe^{VBE/VTF} \times (\frac{IBE}{IBE + ITF}))^{2} \\ & \times (3 - \frac{2 \times IBE}{IBE + ITF}) - IBE \times Qx + \frac{CJE \times AREA}{F2} \times (F3 + \frac{MJE \times VBE}{VJE}) \end{aligned} \tag{4.19c}$$

where

$$Qx = Q1 \times \frac{QB}{VAR} + \frac{IS \times AREA \times e^{VBE/VT \times NF}}{VT \times NF \times IKF(1 + 4\frac{IBE}{IKF} + \frac{IBC}{IKR})^{1/2}}$$

$F2 = (1 - FC)^{1+MJE}$

$F3 = 1 - FC \times (1 + MJE)$

QB = defined under current equations

VAR = reverse Early voltage

IKF = corner for forward beta high current rolloff

IS = transport saturation current

NF = forward current emission coefficient

$AREA$ = area specified in the element line

VBE = B-E vlotage

4.2.6.2 Base Collector (B-C) Capacitance

To model the non uniform charge distribution, the base to collector capacitance, as in the charge equations, is distributed by the input model parameter, XCJC. The collector capacitor is distributed by connecting one capacitor, Cbx, from the external base node to the internal collector node controlled by the voltage VBX, and another capacitor, Cbc, from the internal base node to the internal collector node, controlled by the voltage VBC.

XCJC must be greater than zero but less than one. Other model parameters affecting the base to collector depletion capacitance are FC, CJC, MJC and VJC. The model parameter affecting the base to collector diffusion capacitance is TR.

If VBC < FC*VJC,

$$Cbc = \frac{TR \times IS \times AREA}{VT \times NR} \times e^{VBC/VT \times NR} + CJC \times XCJC \times AREA \times (1 - \frac{VBC}{VJC})^{-MJC} \qquad [4.20a]$$

If VBC > = FC*VJC,

$$Cbc = \frac{TR \times IS \times AREA}{VT \times NR} \times e^{VBC/VT \times NR} + \frac{CJC \times XCJC \times AREA}{F2} \times (F3 + MJC \times \frac{VBC}{VJC}) \qquad [4.20b]$$

If VBX < FC*VJC,

$$Cbx = CJC \times (1 - XCJC) \times AREA \times (1 - \frac{VBX}{VJC})^{-MJC} \qquad [4.20c]$$

If VBX > = FC*VJC,

$$Cbx = \frac{CJC \times (1 - XCJC) \times AREA}{F2} \times (F3 + \frac{MJC \times VBX}{VJC}) \qquad [4.20d]$$

where

$F2 = (1 - FC)^{1+MJC}$

$F3 = 1 - FC \times (1 + MJC)$

IS = transport saturation current

NR = forward current emission coefficient

$AREA$ = area specified in the element line

4.2.6.3 *Collector Substrate (C-S) Capacitance*

The collector to substrate capacitance is modeled as a depletion capacitance. The input model parameters affecting the collector to substrate capacitance are VJC, CJS and MJS. The collector to substrate capacitance is given by the following equation:

If VCS < 0,

$$Ccs = CJS \times AREA \times (1 - \frac{VCS}{VJS})^{-MJS} \qquad [4.21a]$$

If VCS > 0,

$$Ccs = CJS \times AREA \times (1 + \frac{MJS \times VCS}{VJS}) \qquad [4.21b]$$

where

$AREA$ = area specified in the element line

4.2.7 Transient Modifications

Excess phase or time delay resulting from base doping and the transport of minority carriers through the neutral base is modeled by replacing IBE at some particular time t, with IBE at time t-PTF*TF. Backward Euler integration is used to obtain the value of IBE at t-PTF*TF. This is then used in place of IBE in the collector current term.

4.2.8 Temperature effects

Temperature dependence of the saturation current in the BJT model is determined by:

$$IS = IS(T_o) \times \left(\frac{T}{T_o}\right)^{XTI} \times e^{\frac{(qEG/k)(T-T_o)}{T\times T_o}} \qquad [4.22]$$

where

N = emission coefficient

EG = activation energy used in calculation of IS

XTI = saturation current temperature exponent

T = present temperature

T_o = previous temperature

CJE, VJE, CJC and VJC are temperature dependent due to the internally calculated energy gap, Egi. Egi has the following temperature dependence:

$$Egi = 1.16 - \frac{7.02 \times 10^{-4} \times T^2}{T + 1108} \qquad [4.23]$$

CJX and VJX, where X may be either an E for emitter or a C for collector, are recalculated at each different temperature using the modified Egi:

$$VJX_1 = \frac{T}{T_o} \times (VJX_o + PB(T_o)) - PB(T_r) \qquad [4.24]$$

$$CJX_1 = CJX_o \times (1 + M) \times (400 \times 10^{-6} \times (T - T_r) + \frac{PBO - VJX_1}{PBO}) \qquad [4.25]$$

where

$$PB(T) = 2VT(T) \times 1.5\ln(\frac{T}{T_r}) + q(egi\frac{(T)}{2VT(T)} + \frac{1.115}{2kT_r})$$

$$VT(T) = \frac{kT}{q}$$

$$egi(T) = 1.16 - \frac{T2 \times 7.02 \times 10^{-4}}{T + 1108}$$

$$PBO = \frac{T_o}{T_r}(VJ_o + PB(T_o))$$

$VJX_o =$ value of VJX at previous temperature

$CJX_o =$ value of CJX at previous temperature

$T_r =$ reference temperature

Due to the thermal voltage VT, temperature appears explicitly in the exponential terms of the BJT model equations.

Temperature effects on Beta are carried out by appropriate adjustment to the values of BF, ISE, BR and ISC. In the following equations the X may be either a F, R, C or E representing the forward beta, reverse beta, collector saturation current or emitter saturation current respectively.

TLEV = 0 (default)

$$BX' = BX \times (\frac{T}{T_o})^{XTB} \qquad [4.26a]$$

$$ISX' = ISX \times (\frac{T}{T_o})^{XTI/XTB} \times e^{\frac{(qEG/Nk)(T - T_o)}{T \times T_o}} \qquad [4.26b]$$

TLEV = 1

$$BX' = BX \times (1 + XTB \times (T - T_o)) \qquad [4.27a]$$

$$ISX' = ISX \times \frac{e^{\frac{(qEG/Nk)(T - T_o)}{T \times T_o}}}{1 + XTB \times (T - T_o)} \qquad [4.27b]$$

where

BX = BF or BR, the ideal maximum forward or reverse beta

XTB = input parameter, forward and reverse temperature exponent

ISX = input parameter ISE or ISC, the B-E or B-C leakage saturation current

XTI = input parameter, temperature exponent for saturation current

T = present temperature

T_o = previous temperature

Temperature changes affect the resistance values of the series resistances. Each resistor for the emitter, base and collector can use a first and second order temperature coefficient. The resistances are calculated as:

$$RX(T) = RX(TNOM) \times (1 + TCXR1 \times (T - TNOM) + TCXR2 \times (T - TNOM)^2) \qquad [4.28]$$

where

RX = RC, RB or RE

$TCXR1$ = TCCR1, TCBR1 or TCER1

$TCXR2$ = TCCR2, TCBR2 or TCER2

T = TEMPDC

4.3 Hybrid 'pi' Model

The schematic shown in Figure 12 on page 62 is known as the simplified Hybrid 'pi' model. This circuit is a first order small signal model for the BJT transistor [9]. The small signal model applies for a particular DC operating point. The value of gm and r_π depend on the DC operating point, and they will change when the dc bias changes. The transconductance (gm) is the coefficient for the voltage controlled generator which gives the relationship of small signal collector current to small signal B-E voltage.

$$i_C = gm \times vbe \qquad [4.29]$$

The base and emitter form a p-n junction, which is modeled by a diode. For small signal analysis this diode is represented by r_π. The value of r_π is the resistance between the base and emitter junction for a particular I_B.

The base and collector also form another p-n junction. When the transistor is biased in the forward active region this junction is reverse biased. This is modeled with another resistor r_μ shown in Figure 13 on page 63. A reverse biased junction is ideally an open circuit; therefore, r_μ is very large.

The resistance r_x models the resistance of the silicon material of the base region between the external node b and the ideal node b′. The value of r_x is typically a few tens of ohms. Resistance r_o models the slight effect of collector voltage on the collector current in the active region of operation. Typically, r_o is in the range of tens to hundreds of kilohms. Figure 14 on page 64 shows the high frequency model.

Capacitor C_π is composed of two parts; diffusion capacitance which depends on bias current, and junction depletion capacitance which depends on VBE, the dc voltage across the junction.

The capacitor C_μ is entirely a depletion capacitance and its value depends on VBC. These capacitors model the frequency response of the bipolar transistor.

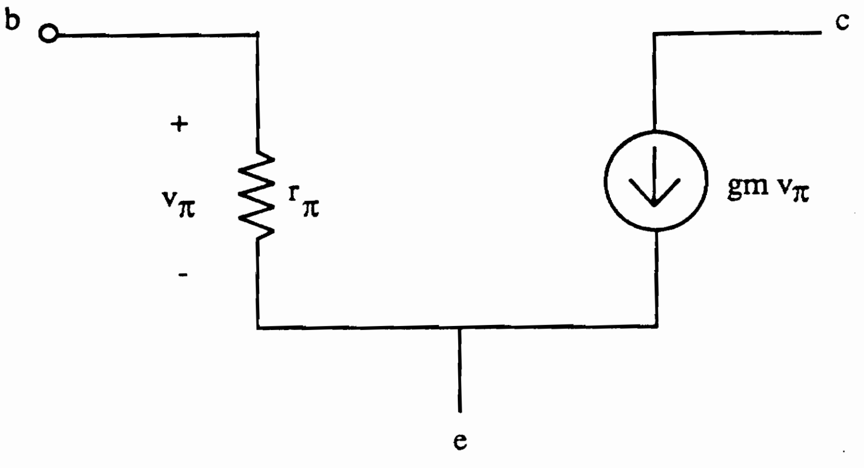

Figure 12. Simplified Hybrid 'pi' Model.

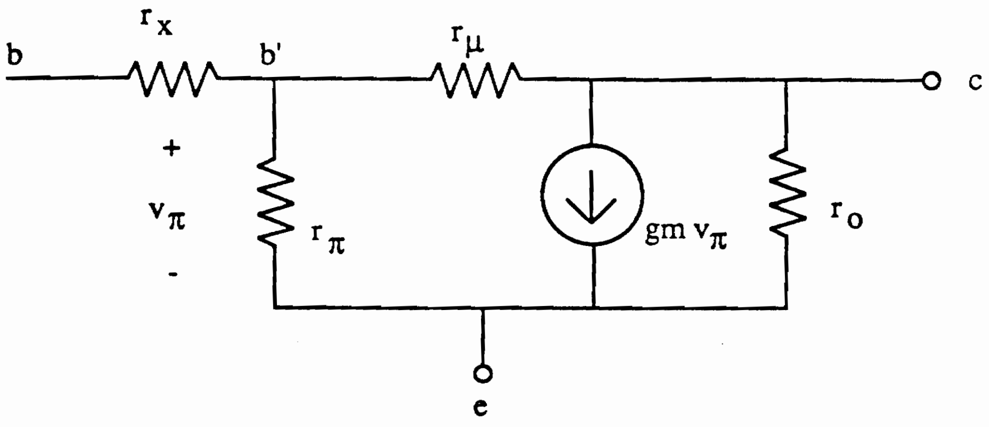

Figure 13. Low Frequency Hybrid 'pi' Model.

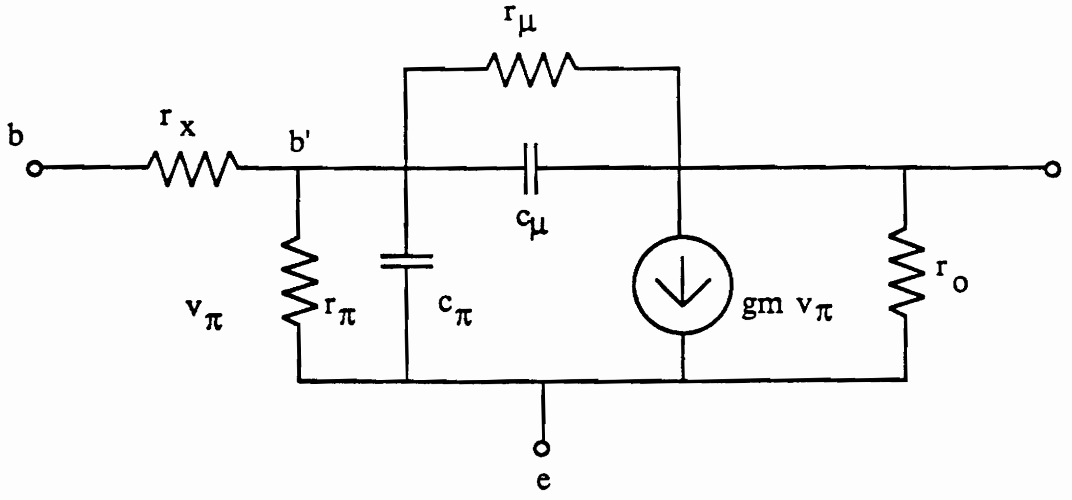

Figure 14. High Frequency Hybrid 'pi' Model.

4.4 Noise Model

The noise model for the BJT is as shown in Figure 15 on page 66. The current sources inrb, inrc and inre model the thermal noise generation in the ohmic region for the base, collector and emitter respectively. The value of inrx is:

$$inrx = (\frac{4kT}{RX})^{1/2} \qquad [4.30]$$

where x maybe either B, C or E for the base, collector or emitter respectively.

The current source inb and inc model the shot and flicker noise of the junctions. The values are:

$$inc = (2qIc)^{1/2} \qquad [4.31]$$

$$inb = (2qIb + \frac{KF \times Ib^{AF}}{Freq})^{1/2} \qquad [4.32]$$

where

AF = input parameter AF, flicker noise exponent

KF = input parameter KF, flicker noise coefficient

$Freq$ = frequency

The model parameters AF and KF are estimated from measurements of the diode noise at low frequency. For silicon diodes, typical values for these parameters are KF = 1E-6 and AF = 1 [3].

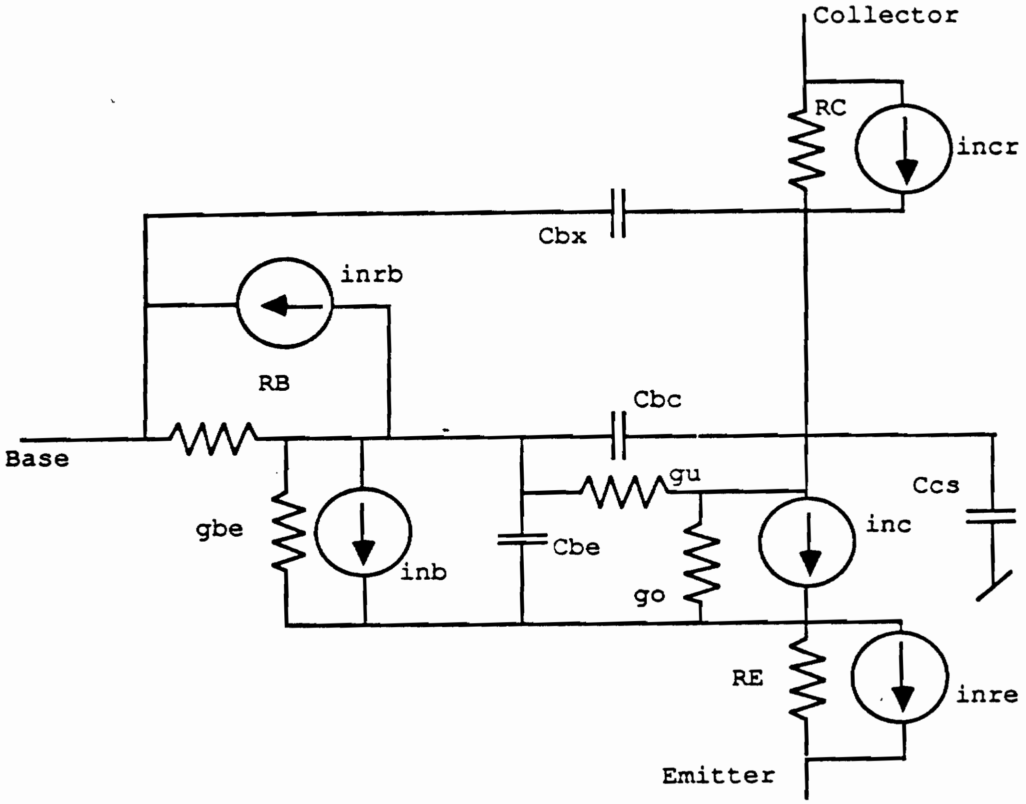

Figure 15. BJT Noise Model.

4.5 Summary

The models developed by using the method outlined in this chapter are as shown in Appendix C. A total of seventy six models have been modeled using this method. Files for testing some of these parameters and a computer program developed to generate the BJT model are as shown in Appendix A. To verify some of the important parameters associated with each transistor, the PROBE command can be used within PRECISE to display some of the computed results, which compare very favorably against comparisons with actual devices as will be shown in Chapter VI.

Thus, using the methods outlined in this chapter, accurate models for BJTs can be easily developed.

Chapter V

DEVELOPMENT OF A GALLIUM ARSENIDE METAL SEMICONDUCTOR FIELD EFFECT TRANSISTOR AND SIMULATIONS ON BIPOLAR JUNCTION TRANSISTORS

5.1 Introduction

In this chapter, a theoretical description for the development of a GaAs MESFET model is explained [14,16]. The physics for developing such a model are detailed in Section 5.2. Section 5.3 uses the BJT models in order to simulate an inverter circuit. Actual and measured response times are compared, showing the effectiveness of the models that have been developed. The chapter concludes with a general summary in Section 5.4.

5.2 Physics of the Gallium Arsenide Metal Semiconductor Field Effect Transistor

The characteristics of the GaAs MESFET can be modeled using two ideal diodes, two nonlinear capacitors, one linear capacitor, three linear resistors and one current source [14,15,16]. Upto two different drain current equations can be chosen. The constants, model parameters, diode currents, charge and temperature effects are common to both levels of drain current equations. The equivalent representation is shown in Figure 16 on page 70.

The area of the GaAs MESFET is determined by the value assigned to AREA in the element line. A total of sixteen parameters can be calculated in order to generate an accurate model. The model parameters are shown in Table 11 on page 71.

5.2.1 Diode current

The junction diodes are modeled by the ideal equation:

$$Igx = IS \times AREA(e^{VGX/VT} - 1) \qquad [5.1]$$

where

IS = input parameter IS, the saturation current

$VGX = VGS$, G-S voltage or VGD, G-D voltage

$AREA$ = area of GaAs MESFET from the element line

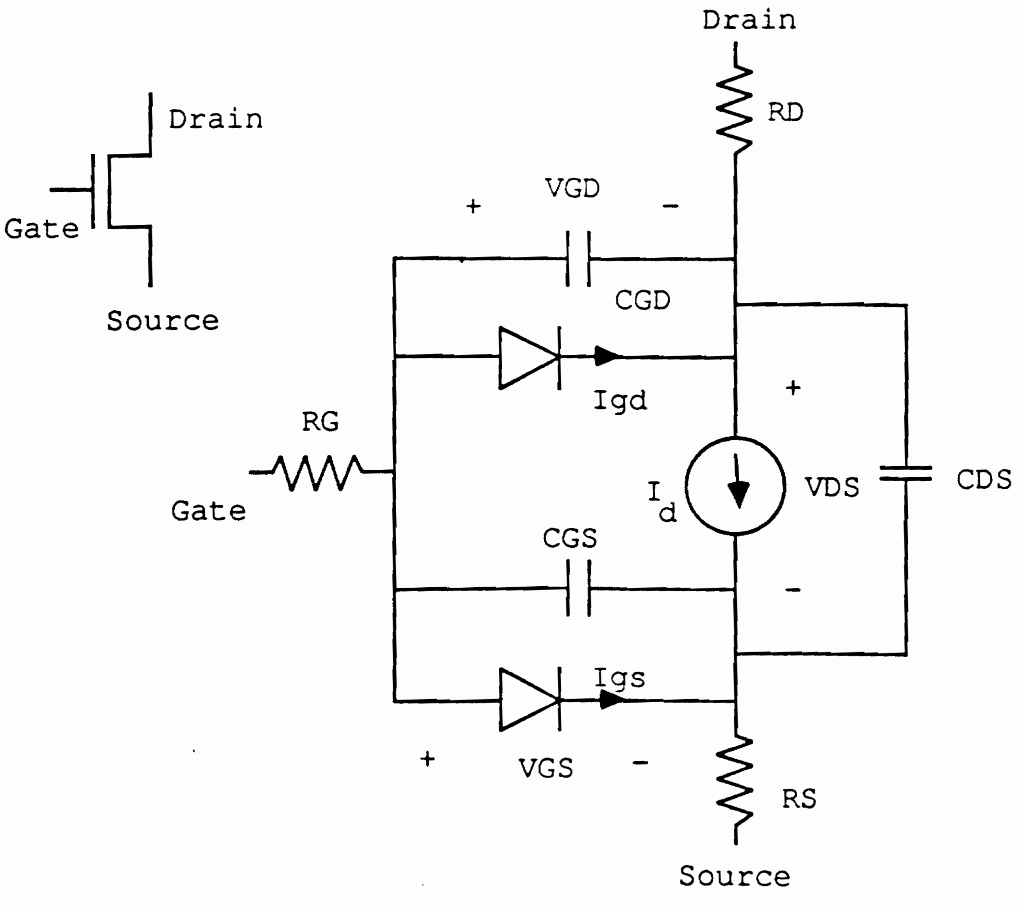

Figure 16. GaAs MESFET representation.

Table 11. GaAs MESFET model parameters

NAME	MODEL PARAMETER	UNITS	DEFAULT	EXAMPLE	AREA
LEVEL	current equation		1		
VTO	threshold voltage	V	-2.5	-2.0	
VBI	gate potential	V	1.0	0.9	
RG	gate resistance	Ohm	0	10	
ALPHA	Tanh constant	1/V	2.0	2.0	
BETA	transconductance	A/V**2	1E-4	1E-3	*
LAMBDA	channel length modulation	1/V	0	1E-4	
CGS	zero bias G-S junction capacitance	F	0	5pF	*
CGD	zero bias G-D junction capacitance	F	0	1pF	*
CDS	D-S capacitance	F	0	1pF	*
IS	junction saturation current	A	1E-14	1E-14	*
RD	drain resistance	Ohm	0	100	/
RS	source resistance	Ohm	0	100	/
TAU	transit time under gate				
DELAY	gate delay (level 2)	Sec	0	10ps	
K	VDS multiplication factor		1	1.5	

5.2.2 Charge Storage

Charge storage in a GaAs MESFET occurs in the G-S, G-D and D-S junctions. This charge is modeled by the capacitances CGS, CGD and CDS [15,16].

$$CGX = CGX(1 - \frac{VGX}{VBI})^{-1/2} \qquad [5.2]$$

where

$VGX =$ voltage across the junction

$CGX =$ input parameter CGS or CGD, the zero bias junction capacitance

$VBI =$ input parameter VBI, the built-in voltage

The D-S junction charge is modeled by the linear capacitor CDS.

5.2.3 Charge

In nodal analysis all elements are represented by current sources and conductances. In the GaAs MESFET model charge is used to derive the equivalent conductance and current source for the G-S and G-D capacitors. An expression for the charge is derived by integrating the definition of small signal capacitance, C = dQ/dV, from 0 to VGS. The result is

$$QGX = 2 \times VBI \times CGX \times (1 - (1 - \frac{VGX}{VBI})^{1/2}) \qquad [5.3]$$

5.2.4 Drain Current Equations

The model parameter LEVEL determines which drain current equation the model will use.

5.2.4.1 *LEVEL = 1*

In LEVEL one, the drain current Id is determined by the parameters VTO, BETA, LAMBDA, and ALPHA [14,15]. VTO is negative for most GaAs MESFETs. The parameter LAMBDA determines the effect of channel-length modulation.

In the forward region, VDS > = 0.

If VGS < = VTO,

$$Id = 0 \tag{5.4a}$$

If VGS > VTO,

$$Id = \mathrm{BETA} \times (1 + \mathrm{LAMBDA} \times VDS)(VGS - VTO)^2 \times \tanh(\mathrm{ALPHA} \times VDS) \tag{5.4b}$$

In the reverse region, VDS < 0.

If VGD < = VTO,

$$Id = 0 \tag{5.4c}$$

If VGD > VTO,

$$Id = -\mathrm{BETA} \times (1 - \mathrm{LAMBDA} \times VDS)(VGD - VTO)^2 \times \tanh(\mathrm{ALPHA} \times VDS) \tag{5.4d}$$

where

VDS = D-S voltage

VGS = G-S voltage

VGD = G-D voltage

BETA = input transconductance parameter

LAMBDA = channel-length modulation parameter

VTO = threshold voltage parameter

ALPHA = Tanh constant parameter

The transit time is the time delay between a change in the G-S voltage and a corresponding change in the D-S conduction current. It takes on the order of 10 picoseconds for a change in current after the gate voltage is changed in a one micron gate length GaAs MESFET [14]. The transient drain current then becomes:

$$Id = Id(VGS - VDS)_{DC} - GM \times \mathrm{TAU} \times \frac{dVGS}{dt} \qquad [5.5]$$

where

TAU = transit time under gate

GM = transconductance

$\frac{dVGS}{dt}$ = derivative of G-S voltage with respect to time

5.2.4.2 LEVEL = 2

The LEVEL two model accounts for the variations in the D-S voltage and the gate delay [15]. The D-S voltage, VDS is multiplied by the input parameter K. For the purpose of this discussion, this product is referred to as VDS′.

In the forward region, VDS′ > = 0.

If VGS-VTO < 0,

$$Id = 0 \qquad [5.6a]$$

If 0 < VGS-VTO < VDS′,

$$Id = \text{BETA} \times (1 + \text{LAMBDA} \times VDS')(VGS - VTO)^2 \qquad [5.6b]$$

If 0 < VDS′ < VGS-VTO,

$$Id = \text{BETA} \times VDS' \times (1 + \text{LAMBDA} \times VDS') \times (2 \times (VGS - VTO) - VDS') \qquad [5.6c]$$

In the reverse region, VDS′ < 0.

If VGD-VTO < 0,

$$Id = 0 \qquad [5.6d]$$

If 0 < VGD-VTO < -VDS′,

$$Id = -\text{BETA} \times (1 - \text{LAMBDA} \times VDS') \times (VGS - VTO)^2 \qquad [5.6e]$$

If 0 < -VDS′ < VGD-VTO,

$$Id = -\text{BETA} \times VDS' \times (1 - \text{LAMBDA} \times VDS') \times (2 \times (VGS - VTO) - VDS') \qquad [5.6f]$$

where

VDS = D-S voltage

K = VDS multiplication factor

$VDS' = K \times VDS$

VGS = G-S voltage

VGD = G-D voltage

BETA = Transconductance parameter

LAMBDA = channel-length modulation parameter

VTO = threshold voltage parameter

The transit time is the delay between a change in the G-S voltage and a corresponding change in the D-S conduction current. It takes on the order of 10 picoseconds for a change in current after the gate voltage is changed in a one micron gate length GaAs MESFET [14]. This effect is modeled by using the input parameter DELAY. When DELAY is specified the model uses the G-S voltage, VGS, at the present simulation time minus DELAY to calculate the drain current at the present simulation time. The transient drain current then becomes

$$Id(VGS(t), VDS(t)) = Id(VGS(t - DELAY), VDS(t)) \qquad [5.7]$$

where

$Id(VGS(t), VDS(t))$ = drain current calculation

$VGS(t)$ = G-S voltage at the present time

$VDS(t)$ = D-S voltage at the present time

$Id(VGS(t - DELAY), VDS(t))$ = drain current calculated with G-S voltage

$VGS(t - DELAY)$ = G-S voltage at time (t - DELAY)

t = present simulation time

5.3 Analysis using the Models

The goal of this section is to evaluate the accuracy of the BJT models developed using the method outlined in Chapter IV. Since tests performed on individual models prove that the models are sufficiently accurate, the models have been used to simulate the behavior of a two stage buffer circuit, which actually consists of two single stage inverter circuits staged together as shown in Figure 17 on page 79. Both of the transistors used in this circuit saturate to the same degree as the transistor in a single stage inverter circuit. The netlist and test files used for the circuit as well as the response time plot from simulation results are shown in Appendix D. The response times are also compared against actual circuit response times, which were measured after wiring the circuit together using actual oscilloscope probes. The measuring equipment consisted of the Hewlett-Packard 4190A L-C-R meter and the Hewlett-Packard 8012B Pulse Generator, as well as the Tektronix 7603 Oscilloscope.

The measured and simulated response times are shown in Table 12 on page 78. Comparisons indicate that good accuracy is achieved in simulation, thus indicating that the models developed by the method outlined in Chapter IV are fairly accurate. Four response times are compared: the delay time (td), the rise time (tr), the storage time (ts) and the fall time (tf).

The data in Table 12 on page 78 shows that with sufficient temperature stabilization, fairly accurate results can be obtained even in measuring shorter response times. Calculating the largest percent variation for the data of each response time, the tolerance is given and recorded as shown in Table 13 on page 78.

Hence it can be seen that circuit response measurements can be measured to within 90% accuracy or greater.

Using an anticipated accuracy of about 75%, the PRECISE simulation results were checked for accuracy. Three variations of the circuit were simulated to check the credibility of the models. The overall accuracy from these analyses rates the performance of the models.

The two stage buffer circuit shown in Figure 17 on page 79 was simulated using measured values of all components. Rc, with a nominal value of 470 Ohms, was measured as 464 Ohms. Rs was measured as 3.91 KOhms. Q1 was modeled using the transistor model for 2N2222. Table 14 on page 78 indicates the response time comparisons for the three variations of the two stage buffer circuit.

Table 12. Measured and Simulated Response Time Data

(A) Measured Data.

Experiment #	td	tr	ts	tf
1	20.0	121.3	45.4	27.0
2	21.0	119.7	45.0	26.4
3	20.0	121.0	45.2	26.7

(B) Simulated Results. TNOM = 27 ° C.

Experiment #	td	tr	ts	tf
1	19.8	125.7	43.9	26.0

Table 13. Error Analysis of the measured data.

td	tr	ts	tf
5%	1.4%	0.8%	2.2%

Although Variations 1 and 2 show that the models yielded very good accuracy, Variation 3 shows that the models failed to represent the circuit. With Rc at 56 Ohms, the measured value of Vce was 0.5V, which indicates that the transistor may not have fully saturated. Since the model yielded significant errors for this particular result, it may be concluded that a link between degree of saturation and model accuracy exists.

Hence, the simulations and measured results prove that the models developed yield a significantly accurate characteristic for the particular device.

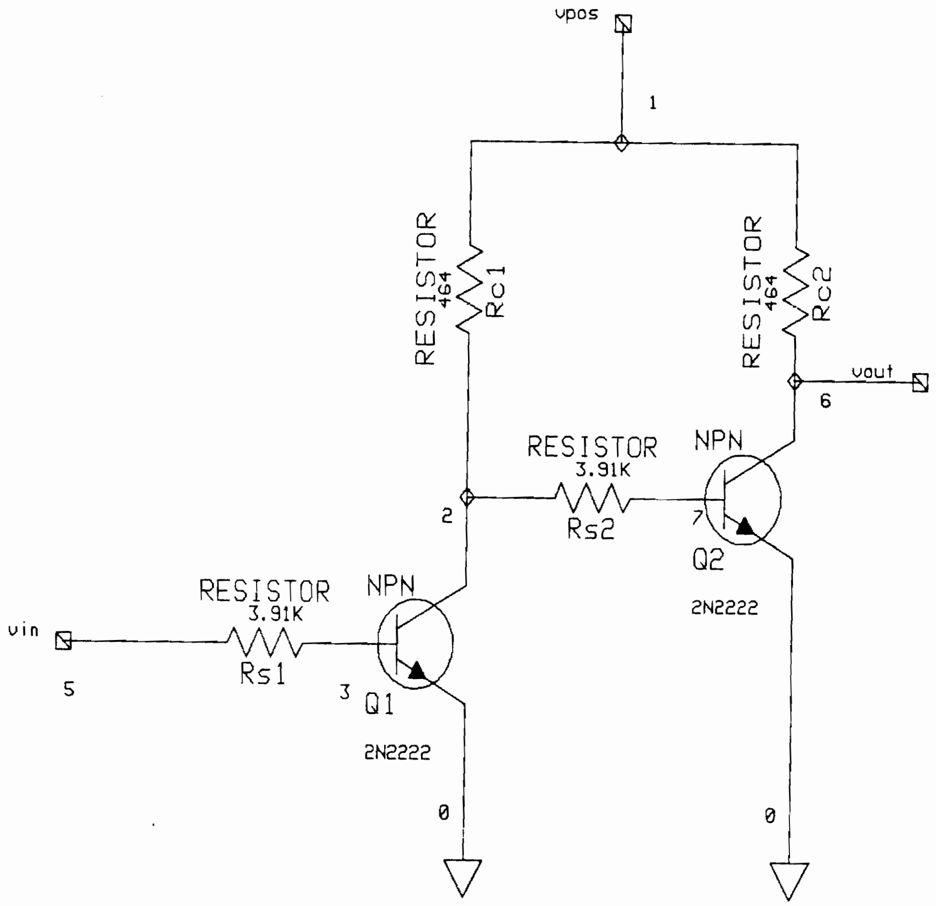

Figure 17. Circuit used in Simulation

Table 14. Response Time Comparisons

Variation 1: V1 = 5V

Case	**td**	**tr**	**ts**	**tf**
Real Circuit	20.1	121.0	45.2	26.9
PRECISE	21.9	102.3	41.0	22.8

Variation 2: VCC = -1V

Case	**td**	**tr**	**ts**	**tf**
Real Circuit	14.2	140.3	76.9	31.6
PRECISE	17.3	129.4	72.3	30.0

Variation 3: Rc = 56 Ohms

Case	**td**	**tr**	**ts**	**tf**
Real Circuit	14.2	459.0	121.9	461.0
PRECISE	11.9	221.9	45.1	59.0

5.4 Summary

In this chapter, a theoretical description for the development of a GaAs MESFET model was explained. To date, no models have been developed using the method outlined, as commercial data for common GaAs devices is not readily available. The BJT models developed were used in PRECISE to simulate a two stage buffer circuit. Thus, the accuracy of the models was verified by comparison in actual measurements. While a low tolerance of error was allowed, it was found that in most simulation runs, an accuracy greater than 75% was achieved. This is very significant, comparing results with previous research work done in this area [19]. The significance of these results is reviewed in Chapter VI.

Chapter VI

CONCLUSIONS

In this research, models were developed for three device components, namely diodes, BJT's and GaAs MESFETS, with computer models being developed for diodes and BJT's. Conventional measurement methods were used to measure device parameters and the model development method was optimized to reflect these parameters. The two methods were compared in the simulation for a two stage buffer to ensure the accuracy of the models thus developed, thus showing that accurate models can be developed for computer simulations using the methods outlined in Chapters III and IV.

Usually, models of this nature are used in transient simulation, and specifically, BJT models may be used in digital switches. For such simulations, the rise time, the storage time, the fall time and the delay time usually limit the switching speed. The most critical of these is the Storage time, which occurs as the BJT moves from the saturation to the cutoff region. This time is usually an order of magnitude greater than the other delay times. The largest component of this Storage time is the time required for the BJT to leave saturation and enter the active region. This requires that excess charges stored in the base region be removed [1]. In order to prevent the BJT from entering the saturation region and to minimize Storage time to increase switching speed, transient modifications are made as shown in section 4.2.7. Obviously, applications of this nature are speed oriented.

The complexity of the mathematics and sheer size of the circuit may make the calculations difficult and impractical. Thus an iterative approach is required which usually requires a computer for speed and accuracy for the large number of calculations involved. One of the better computer programs developed for such transient analyses is PRECISE, which also offers general capabilities at relatively better computational speeds than most other simulators based on the Berkeley SPICE standard. PRECISE readily incorporates linear components such as resistors, capacitors and inductors into simulation models. Nonlinear components require more complex modeling. For the diode models, BJT models and GaAs MESFET models, nonlinear equations parallel the I-V and C-V curves. Some constants that vary among individual components are left as adjustable parameters for the user. Hence, the nonlinear models are used by determining values for these parameters. The selection of these values affect the accuracy of the simulation results. Thus the main focus of this research was the determination of parameter values and characteristics to give the models acceptable accuracy.

The diode model was derived by determining sixteen parameters for device behavior. A number of commercially available diodes were modeled using the approach outlined in Chapter III. This method yielded models with good accuracy in modeling all the essential device characteristics.

The BJT model was derived by determining a total of forty-nine parameters for the modified Gummel-Poon model. This model could be simplified to the simpler Ebers-Moll model with sixteen parameters if certain characteristics were not necessary. A number of commercially available BJT's were modeled using this approach, outlined in Chapter IV. Using these parameters, the models were used to simulate a two stage buffer circuit. Conventional measurements on a fabricated circuit confirmed that the simulations yielded models of comparable accuracy to an actual device. The response time results were found to agree to upto 90 percent with the measured response times. This accuracy proved that with the modeling approach followed, very accurate computer models could be generated for simulation purposes. Three different variations of the circuit operation were simulated to confirm the results.

A method to develop a GaAs MESFET model was also outlined. However, no computer models were developed as datasheets for these devices could not be obtained. A total of fifteen parameters were determined to be necessary in order to model a reasonably accurate device.

Hence, this research has shown that this method can be used to replace the conventional measurement method and the "breadboarding" that is normally employed to test such discrete circuits. The modeling process can be automated using the program outline, thus making device and circuit simulation and behavior much easier to predict.

More research can be done to try and improve the accuracy of the models developed. Temperature effects that are currently modeled could be improved upon. GaAs MESFET models could be developed. An algorithm to develop models for operational amplifiers and other discrete integrated devices could be researched. The method could also be applied to frequency response analyses to further determine domain limitations.

In summary, computer models were developed for the diode and BJT devices to allow for the accurate simulation of circuit applications using these devices. A theoretical model was also developed for the GaAs MESFET device. The models yielded accuracies up to 90 percent in comparison with actual circuit behavior. Thus, these methods offer a distinct advantage over the conventional measurement method. They are simpler to use, thus making PRECISE a very powerful simulation tool for the design engineer.

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Appendix A

TEMPLATE AND TEST FILES FOR PRECISE MODELS

This template file describes the various simulation commands that are used in PRECISE.

```
* TEMPLATE.USE    SAMPLE "USE" FILE FOR PRECISE

OPTIONS LIMPTS=1000 ITL5=1E6 OFLDEV=5 METHOD=GEAR

* ADDLIB 1 [MMP.SPELIB]

* SPELIB IS THE SPICE GENERATED LIBRARY

SIM filename

****************************

* DC ANALYSIS

*
```

```
DCSP (NO OUTPUT UNLESS PROBE COMMAND IS USED)
PROBE */K*/N*
*  *=EVERYTHING, K*=DEVICES WITH KEYLETTER, N*=ALL NODES
SWEEP TEMPDC/VT/PARAMETER FROM _ TO _ BY/DEC/OCT _
+ [AND _ FROM _ TO _ ...]
* NOTE: IF A VOLTAGE SOURCE NEEDS TO BE SWEPT, IT HAS TO BE GIVEN
* A NAME. THIS DIFFERS FROM SPICE.
SENSITIV V(_) V(_) I(_)
*
****************************
* AC ANALYSIS
*
ACSP FREQ
* FOR SINGLE POINT ANALYSIS
*
SWEEP FREQ FROM _ TO _ BY/DEC/OCT _
* FOR MULTI POINT ANALYSIS    LINEAR INCREMENT/PTS PER DECADE/OCTAVE
*
NOISE V(OUTPUTNODE) [INPUTSOURCE]
*
****************************
* TRANSIENT ANALYSIS
*
UIC ON/OFF
SWEEP TIME FROM _ TO _ BY _
FOURIER [FREQ] V(_) V(_) ETC
OPTIONS FORPTS=[NO OF PTS IN FOURIER ANALYSIS]
*
```

```
****************************

* OUTPUTS

*

KEEP *

PLOT V(_) [(_,_)] V(_) [(_,_)] [FROM _ TO _]

*

* IT IS PERMISSIBLE TO USE ANY OF THE FOLLOWING OUTPUTS

* INSTEAD OF NODE VOLTAGES:

*   I(ELEMENTNAME) I(ELEMENTNAME, NODENUMBER)

*   EXCEPT THAT CURRENTS CAN BE MONITORED ONLY IN VOLTAGE

*   SOURCES UNLESS A DC ANALYSIS IS BEING PERFORMED

* VR VI VM VP VDB

* IR II IM IP IDB

* INOISE(R/I/M/P/DB) ONOISE(R/I/M/P/DB)

PRINT

* SAME AS PLOT

*

* TO DIRECT OUTPUT TO A FILE OR DEVICE, USE THE FOLLOWING COMMANDS

*

ASSIGN FILENAME/DEVICENAME

OFFLINE

*

****************************

* OPTIONS (WITH DEFAULTS)

*

OPTIONS GMIN=1E-12

 + RELTOL=0.05

 + ABSTOL=1NA
```

```
+ VNTOL=50UV
+ CHGTOL=1E-14
+ NUMDGT=4
+ ITL5=20000
* TRANSIENT ITERATION TOTAL LIMIT
+ LIMPTS=201
+ OFLDEV=
+ DEVICE=
+ METHOD=
*
* TO GET A GRAPHICS OUTPUT, USE OPTIONS OFLDEV=5
* THEN USE LASER PRINTER WITH THE COMMAND:
* IMPRINT/TEK FILENAME AFTER EXITING PRECISE/SPICE
* OR USE A TEK 4014 WINDOW ON THE MICROVAX TO VIEW OUTPUT
* OR USE A TEK 4014 WINDOW ONLINE WITH OPTIONS DEVICE=5
* USE METHOD=GEAR TO AVOID OSCILLATION WITH TRANSISTOR MODELS
*
***************************
*
* OTHER FEATURES
* PROBE
* LIBRARY COMMANDS
* SET
* SPICE
* WIDTH
*
***************************
*
```

```
GO
DEASSIGN
*
***************************
* TO GET EXTRA PLOTS IN OFFLINE FILES, ADD COMMANDS IN THE
* FOLLOWING ORDER, WITH THE "KEEP" COMMAND PRIOR TO FIRST GO ABOVE
*
* PLOT ___
* ASSIGN ___.LIS
*
* OFFLINE
* GO
* DEASSIGN
*
* REPEAT AS NECESSARY
***************************
ONLINE
***************************
```

```
* DIODE TEST USE FILE
OPTIONS LIMPTS=1000 ITL5=1E6 OFLDEV=5 METHOD=GEAR
**************************
* DC ANALYSIS GENERATES CURRENT/VOLTAGE PLOT FOR DIODE
SWEEP IBIAS FROM 0 TO 1 BY 0.01
**************************
* OUTPUTS
PLOT V(1, 2)
ASSIGN DTEST1.LIS
OFFLINE
GO
DEASSIGN
**************************
* TRANSIENT ANALYSIS LOOKS AT REVERSE RECOVERY TIME
UIC OFF
SWEEP TIME FROM 0 TO 0.1US BY 1NS
SET IBIAS=1.1
**************************
* OUTPUTS
KEEP *
PLOT V(2) (-1, 1)
ASSIGN DTEST2.LIS
OFFLINE
GO
DEASSIGN
PLOT V(1)
ASSIGN DTEST3.LIS
OFFLINE
```

```
GO

DEASSIGN

ONLINE

**************************

* NOTE: THIS FILE CAN BE GENERALIZED BY ALLOWING THE DIODE AND

* PULSE PARAMETERS TO BE SET OR VARIED FROM THE USE FILE

**************************
```

This file contains test circuits to detemine the behavior of the Bipolar Junction Transistor Models.

```
TT1.SPC    DC TEST OF NPN TRANSISTOR MODEL
* BETA=20
* IB=1MA
* VAF=50
*************************
DC    VC        0       50        1
*  SOURCE    VSTART    VSTOP     INCR
PLOT DC I(VC)
IB 0 1 DC 1MA
VC 3 0 DC 10
Q1 3, 1, 0 T2N2222
*************************
MODEL T2N2222 NPN ......
* ACTUAL MODEL FROM LIBRARY
*************************
WIDTH IN=80 OUT=80
END
* THIS TEST FILE IS IN SPICE FORMAT
```

```
TT2.SPC    TRANSIENT TEST FOR NPN TRANSISTOR MODEL
************************
* NOTES:
* 1. STORAGE DELAY IS DETERMINED BY TR, BR AND BF
* 2. INCLUSION OF CJE MAY PREVENT OSCILLATION WITH TR AND TF
```

```
* 3. OSCILLATION WILL OCCUR WITH THE FOLLOWING MINIMAL PARAMETERS:
*    TF, BF, BR, IS
************************
* CONDITIONS:
* IB=1MA
* IBR=1MA
* IC=10MA
************************
TRAN   10NS   500NS
     STEP   STOP   START    MAX    UIC
PLOT TRAN V(3) V(1) I(VCC)
************************
IIN 1 0 PWL(0, -1MA  10NS, -1MA  11NS, 1MA)
RIN 1 0 10K
RLOAD 4 3 1K
Q1 3,1,0 T2N2222
VCC 4 0 DC 10
************************
MODEL T2N2222 NPN....
* ACTUAL MODEL FROM LIBRARY
************************
OPTIONS NOMOD RELTOL=0.00001 VNTOL=0.001V CHGTOL=1E-17
OPTIONS METHOD=GEAR ABSTOL=0.001PA
WIDTH IN=80 OUT=80
END

TT3.SPC   TEST MODEL FOR COBO
* Q1 IS DEVICE UNDER TEST
```

```
* VBIAS IS DC BIAS, COLLECTOR TO BASE
* NODE 10 VOLTAGE EQUALS COBO IN PICOFARADS
************************
AC DEC 1 1MHZ 1.1MHZ
PRINT AC VM(10) IM(VMON) IM(VAC)
************************
VBIAS 1 0 DC 10
VAC 1 2 AC 1.0
VMON 3 0 DC 0
H1 10 0 VMON 159K
* H1 TRANSFORMS MONITORED CURRENT INTO VOLTAGE WITH
* THE PROPER SCALEFACTOR
RDUM 10 0 1K
RE 4 0 100M
Q1 2, 3, 4 T2N2222
************************
MODEL T2N2222 NPN...
* ACTUAL MODEL FROM LIBRARY
************************
WIDTH IN=80 OUT=80
END
```

This program calculates the parameters necessary to build a Bipolar Junction Transistor Model from data sheet specifications.

```
! SPTRAN.BAS  FEBRUARY 11, 1988
! PROGRAM STRUCTURE                          &
! 1-9        COMMENTS                         &
! 10-31      INFORMATION FOR THE USER &
! 32-33      SUPPRESS NOTES                   &
! 35-47      TYPE NO. AND NPN/PNP INPUTS
! 50         DC PARAMETERS                    &
! 54-59      USER NOTES                       &
! 60-65      BF                                &
! 70-110     RC CALC FROM VCE(SAT) DATA
! 119-135    BR                                &
! 140        RE CALC FROM RC                  &
! 150        RB CALC FROM RC                  &
! 154-175    IS                                &
! 300-308    AC PARAMETERS                    &
! 310-320    TF CALC FROM FT                  &
! 325-369    TR CALC FROM BF, BR, TS         &
! 929-1060   USER NOTES                      &
! 1064-2040  CJC CALC FROM COBO      &
! 2050-2070  CJE CALC FROM CIN       &
! 2080-3020  CJC & CJE DIAGNOSTICS & NOTES
! 3030-3050  JUNCTION AREA                   &
! 3900-3927  DISPLAY MODEL OUTPUT    &
! 4000-5000  STORE MODEL OUTPUT      &
```

```
4! ADD CJE CALCULATION
5! USE TT1.SPC TO TEST MODEL FOR DC
6! USE TT2.SPC TO TEST MODEL FOR TRANSIENT RESPONSE
7! USE TT3.SPC TO TEST MODEL FOR COBO
10 PRINT "THIS PROGRAM GENERATES SPICE2 MODEL PARAMETERS"
20 PRINT "FROM TRANSISTOR DATA SHEET PARAMETERS"
30 PRINT "FOR BJT'S UING THE EBERS MOLL MODEL"
31 PRINT " "
32 INPUT "SUPPRESS NOTES (Y/N)";MO$
33 IF (MO$<>"Y" AND MO$<>"N") THEN GOTO 32
35 INPUT "TYPE NUMBER";T$
36 IF T$="" THEN GOTO 35
40 INPUT "NPN OR PNP";P$
45 IF P$="NPN" THEN GOTO 50
46 IF P$="PNP" THEN GOTO 50
47 GOTO 40
50 PRINT "DC PARAMETERS"
54 IF MO$="Y" THEN GOTO 60
55 PRINT "NOTES:"
56 PRINT "1. MODEL DOES NOT VARY HFE WITH COLLECTOR CURRENT"
57 PRINT "2. MODEL DOES NOT INCLUDE SLOPE OF COLLECTOR CURRENT"
58 PRINT "   CURVES UNLESS VA IS SPECIFIED"
59 PRINT "3. SOFT KNEE ON COLLECTOR CURRENT CURVE NOT INCLUDED"
60 INPUT "FORWARD DC GAIN (HFE)";BF
65 IF BF=0 THEN GO TO 60
70 PRINT "VCE (SAT) CHARACTERISTIC"
80 PRINT "NOTE: INPUT A SINGLE DATA POINT OF IC AND VCE (SAT)"
90 INPUT "VCE (SAT)-VOLTS";VS
```

```
95 IF VS=0 THEN GOTO 90
100 INPUT "IC AT VCE (SAT)-MA";IC
105 IF IC=0 THEN GOTO 100
110 RC=VS/(0.001*IC)
119 IF MO$="Y" THEN GOTO 130
120 PRINT "NOTE: REVERSE BETA AFFECTS OFFSET OF VCE (SAT) AND STORAGE"
121 PRINT "      DELAY. A WORST CASE VALUE OF 1.0 CAN BE ASSUMED"
130 INPUT "REVERSE BETA=";BR
135 IF BR=0 THEN GOTO 130
140 RE = 0.1*RC
150 RB=RC
154 IF MO$="Y" THEN GOTO 170
155 PRINT "NOTE: 'IS' IS PROPORTIONAL TO JUNCTION AREA"
156 PRINT "      MAJOR EFFECT IS ON VBE"
157 PRINT "      TYPICAL VALUES ARE:"
160 PRINT "      SMALL I.C. TRANSISTOR: 1E-16"
161 PRINT "      SMALL HIGH CURRENT TRANSISTOR: 6E-13"
162 PRINT "      (DIFFERENCE IN VBE IS ONLY 0.2 VOLTS)"
165 PRINT " "
170 INPUT "IS=";IS
175 IF IS=0 THEN GOTO 170
300 PRINT "AC PARAMETERS: GAIN-BW, STORAGE DELAY AND CAPACITANCE"
304 IF MO$="Y" THEN GOTO 310
305 PRINT "NOTES:"
306 PRINT "1. STORAGE DELAY (TS) MUST BE > 0.5(FWD BETA)/(GAIN-BW)"
307 PRINT "2. BF MUST BE > 10 FOR THE TR CALCULATION TO BE VALID"
308 PRINT " "
310 INPUT "GAIN-BW PRODUCT FT=(MHZ)";FT
```

```
315 IF FT=0 THEN TF=0

320 IF FT>0 THEN TF=1/(FT*1E6)

325 ! CALCULATION OF TR FROM BF, BR, TS

330 ! CALCULATION OF ALPHAS

335 AF=BF/(1+BF)

340 AR=BR/(1+BR)

345 ! T(SAT) IS NAMED TA

350 INPUT "STORAGE DELAY TS=(NSEC)";TB

351 TR=1 ! SET PREMATURELY TO 1 TO AVOID GETTING STUCK IN A LOOP IF TR<0

355 TS=TB*1E-9

356 IF TS=0 THEN GOTO 369

357 IF BF<10.1 THEN PRINT "INVALID VALUE OF BF"

358 IF BF<10.1 THEN GOTO 60 ! ALLOWS USER TO START OVER

360 TA=TS/LOG(2/((10/BF)+1))

365 TR=(TA*(1-AF*AR)/AR)-TF*AF/AR

368 IF TR<0 THEN PRINT "TR IS NEGATIVE; BF, TF AND TS ARE INCONSISTENT"

369 IF TR<0 THEN GOTO 305

929 IF MO$="Y" THEN GOTO 1060

930 PRINT "NOTES:"

940 PRINT "1. FOR EBERS MOLL MODEL, NF AND NR ALWAYS = 1.0"

950 PRINT "2. RC IS CALCULATED FROM VCE (SAT) DATA"

960 PRINT "3. RE IS APPROXIMATED AS 0.1*RC"

970 PRINT "4. RB IS APPROXIMATED AS 1.0*RC"

980 PRINT "5. MAJOR EFFECT OF RE AND RB IS ON VBE"

990 PRINT "6. VOLTAGE BREAKDOWN EFFECTS ARE NOT INCLUDED"

1010 PRINT "7. TF IS CALCULATED FROM FT"

1020 PRINT "8. TR IS CALCULATED FROM TS, BF, BR, TF"

1030 PRINT "9. CJC IS CALCULATED FROM COBO AND VOLTAGE"
```

```
1040 PRINT "10. SPICE2 OUTPUT MAY OSCILLATE. THIS IS DUE TO COMPUTATION"
1050 PRINT "    ERRORS WITHIN SPICE2 AND MAY BE CORRECTED USING THE
1060 PRINT "    GEAR INTEGRATION ALGORITHM AND/OR REDUCING TIMESTEP"
1062 PRINT "    OR TOLERANCE OPTIONS USING THE OPTIONS COMMAND"
1064 PRINT " "
1065 ! CJC CALCULATION FROM COBO
1066 ! COBO=CJC/(1-(V/VJC))¢MJE
1070 PRINT "ENTER COBO AND VOLTAGE AT WHICH IT IS SPECIFIED (IF NOT 10V)"
1075 INPUT "COBO (PF)";COBO1
1080 COBO=COBO1*1E-12
1090 INPUT "VOLTAGE (VOLTS)";VCOBO
2000 IF VCOBO=0 THEN VCOBO=10
2020 MJC=0.33
2030 VJC=0.75
2040 CJC=COBO*(1+(VCOBO/VJC))¢MJC
2050 MJE=0.33
2060 VJE=0.75
2070 CJE=0
3000 PRINT "CJE=";CJE*1E-12;"PF"
3010 ! CJC IS TYPICALLY 0.3PF/SQ.MIL OF JUNCTION AREA, AND CAN BE
3020 ! USED TO CALCULATE 'IS' AS AN APPROXIMATION. SOMETIMES, THIS
3025 ! NUMBER CAN BE GROSSLY WRONG DUE TO PROGRAM LIMITATIONS
3030 AREA=CJC/0.3E-12
3040 PRINT "COLLECTOR JUNCTION AREA IS APPROXIMATELY ";AREA;" SQ.MILS"
3900 PRINT "SPICE2 MODEL OF TRANSISTOR IS AS FOLLOWS:"
3905 PRINT " "
3910 PRINT ".MODEL T";T$;"  ";P$;" (BF=";BF;" BR=";BR;" RC=";RC;
3920 PRINT "+ RE=";RE;" RB=";RB;" IS=";IS;" NF=1 NR=1"
```

```
3925 PRINT "+ TF=";TF;" TR=";TR;" CJC=";CJC;" CJE=";CJE;" )"

3935 PRINT "* HFE=";BF;" VCE (SAT)=";VS;" V @";IC;" MA"

3940 PRINT "* BW=";FT;" MHZ"  STORAGE DELAY=";TB;" NS  COBO=";COBO1;" PF"

3950 PRINT " "

4000 INPUT "STORE MODEL (Y/N)";M$

4005 IF (M$ < > "Y" AND M$ < > "N") THEN GOTO 4000

4010 IF M$="N" THEN GOTO 9999

4015 MN$="T"+T$+".SPC"

4020 PRINT "MODEL WILL BE STORED IN FILE ";MN$

4030 OPEN MN$ FOR OUTPUT AS FILE #1

4040 PRINT #1,".MODEL T";T$;"  ";P$;" (BF=";BF;" BR=";BR;" RC=";RC

4050 PRINT #1,"+ RE=";RE;" RB=";RB;" IS=";IS;" NF=1  NR=1"

4060 PRINT #1,"+ TF=";TF;" TR=";TR;" CJC=";CJC;" CJE=";CJE;" )"

4070 PRINT #1,"* HFE=";BF;" VCE (SAT)=";VS;"V @";IC;" MA"

4080 PRINT #1 "* BW=";FT;" MHZ   STORAGE DELAY=";TB;" NS   COBO=";COBO1;" PF"

5000 CLOSE #1

9999 END
```

Appendix B

PRECISE AND SPICE EQUIVALENT COMMANDS

This section is intended for users familiar with SPICE. It lists the equivalent PRECISE commands.

In SPICE, the circuit topology and commands go into a single file with the filetype .CKT. In PRECISE, the file structure is divided in two sections, one containing the circuit topology with the filetype .CKT, and the other containing the command structure with the filetype .USE.

The following are the equivalent syntax structures for both simulators:

SPICE	**PRECISE**
Circuit selection and Options	
No equivalent	SIM circuitname
OPTIONS	OPTIONS
OPTIONS LIST	TYPE filename .CKT
OPTIONS ACCT	QUERY RUN
Convergence Aids	
NODESET	NODESET

IC	INITIAL
DC Single Point	
OP	DCSP
	DISPLAY ELEMENT *
	DISPLAY MODEL *
	PROBE *
SENS	SENSITIV
TF	TF
AC Multi Point	
ACDEC/OCT/LIN	SWEEP FREQ FROM beg
incr beg end	DEC/TO/BY end OCT incr
PRINT AC	PRINT
PLOT AC	PLOT
DISTO	DISTO
NOISE	NOISE
PRINT DISTO	PRINT
PLOT DISTO	PLOT
PRINT NOISE	PRINT
PLOT NOISE	PLOT
	GO
Transient	
TRAN incr end	SWEEP TIME FROM 0 TO end BY incr
PRINT TRAN	PRINT
PLOT TRAN	PLOT
FOURIER	FOURIER
	GO
DC Multi Point	
PRINT DC	PRINT

PLOT DC	PLOT
	GO

Appendix C
PRECISE MODEL LIBRARY

```
*********************************************
*                                     *
*   THIS IS THE SPICE MODEL LIBRARY....    *
*                                     *
*********************************************
*
*
*
*
*********************************************
*                                     *
*.            DIODES                     *
*                                     *
*********************************************
*
*
*
*
LIBRARY D1N63
MODEL D1N63 D( IS=2.87E-13 RS=100.000 N=.99486 TT=1.60E-07

+ CJO=4.58E-10 PB=0.50000 M=0.50000 )
ENDL
*
LIBRARY D1N100
MODEL D1N100 D( IS=2.50E-06 RS=17.000 N=2.6327 TT=6.05E-10

+ CJO=5.01E-13 PB=0.50000 M=0.50000 )
ENDL
*
LIBRARY D1N140
MODEL D1N140 D( IS=2.87E-12 RS=10.000 N=0.9949 TT=1.60E-07

+ CJO=3.46E-11 PB=0.50000 M=0.50000 )
ENDL
*
LIBRARY D1N191
MODEL D1N191 D( IS=1.25E-15 RS=50.000 N=0.9949 TT=1.60E-08
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+ CJO=5.01E-13 PB=0.50000 M=0.50000 )
ENDL
*
LIBRARY FD200
MODEL FD200 D( IS=3.00E-11 RS=0.374 N=1.4715 TT=6.69E-07

+ CJO=4.48E-12 PB=0.96000 M=0.38900 )
ENDL
*
LIBRARY UT262
MODEL UT262 D( IS=1.52E-09 RS=0.100 N=1.6125 TT=1.03E-06

+ CJO=2.40E-11 PB=1.00000 M=0.41000 )
ENDL
*
LIBRARY D1N270
MODEL D1N270 D( IS=1.24E-06 RS=2.420 N=1.6753 TT=2.11E-08

+ CJO=4.00E-12 PB=0.50000 M=0.50000 )
ENDL
*
LIBRARY D1N279
MODEL D1N279 D( IS=1.24E-06 RS=6.000 N=1.6753 TT=1.90E-08

+ CJO=3.59E-11 PB=0.50000 M=0.50000 )
ENDL
*
LIBRARY FD300
MODEL FD300 D( IS=3.00E-11 RS=0.374 N=1.4715 TT=6.69E-07

+ CJO=4.48E-12 PB=0.96000 M=0.38900 )
ENDL
*
LIBRARY D1N457
MODEL D1N457 D( IS=1.20E-10 RS=0.630 N=1.6125 TT=1.37E-07

+ CJO=1.88E-12 PB=1.00000 M=0.33300 )
END
*
LIBRARY UT484
MODEL UT484 D( IS=1.72E-11 RS=0.250 N=1.3163 TT=1.69E-08

+ CJO=2.19E-10 PB=0.75000 M=0.50000 )
ENDL
*
LIBRARY D1N486A
MODEL D1N486A D( IS=2.27E-10 RS=2.000 N=1.4333 TT=2.71E-07

+ CJO=1.27E-11 PB=0.50000 M=0.50000 )
ENDL
*
LIBRARY SD500
MODEL SD500 D( IS=3.97E-14 RS=1.000 N=0.9949 TT=1.60E-05
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+ CJO=4.58E-09 PB=0.50000 M=0.50000 )
ENDL
*
LIBRARY FD600
MODEL FD600 D( IS=4.89E-09 RS=0.475 N=1.8341 TT=1.26E-09

+ CJO=1.01E-12 PB=1.00000 M=0.08800 )
ENDL
*
LIBRARY FDA630
MODEL FDA630 D( IS=2.52E-09 RS=0.392 N=1.7432 TT=1.33E-09

+ CJO=1.40E-12 PB=1.00000 M=0.04930 )
ENDL
*
LIBRARY D1N645
MODEL D1N645 D( IS=2.51E-10 RS=0.532 N=1.4828 TT=3.23E-06

+ CJO=1.18E-11 PB=0.86400 M=0.57700 )
ENDL
*
LIBRARY D1N646
MODEL D1N646 D( IS=2.20E-10 RS=0.100 N=1.4333 TT=6.72E-07

+ CJO=1.60E-11 PB=1.00000 M=0.50000 )
ENDL
*
LIBRARY D1N647
MODEL D1N647 D( IS=1.60E-09 RS=0.100 N=1.7591 TT=4.91E-07

+ CJO=7.70E-12 PB=1.00000 M=0.51000 )
ENDL
*
LIBRARY D1N648
MODEL D1N648 D( IS=2.80E-09 RS=0.100 N=1.8429 TT=3.62E-06

+ CJO=6.60E-12 PB=1.00000 M=0.48000 )
ENDL
*
LIBRARY D1N649
MODEL D1N649 D( IS=2.51E-10 RS=0.532 N=1.4828 TT=4.25E-06

+ CJO=1.18E-11 PB=0.86400 M=0.57700 )
ENDL
*
LIBRARY D1N658
MODEL D1N658 D( IS=3.90E-09 RS=2.000 N=1.7591 TT=8.53E-08

+ CJO=1.80E-12 PB=1.00000 M=0.11000 )
ENDL
*
LIBRARY D1N659
MODEL D1N659 D( IS=1.40E-11 RS=45.000 N=1.1484 TT=7.75E-08

+ CJO=2.08E-11 PB=0.80000 M=0.40000 )
ENDL
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*
LIBRARY D1N661
MODEL D1N661 D( IS=8.24E-15 RS=10.000 N=0.9949 TT=3.20E-09

+ CJO=7.44E-12 PB=0.50000 M=0.33300 )
ENDL
*
LIBRARY D1N695
MODEL D1N695 D( IS=7.80E-07 RS=1.000 N=1.5480 TT=9.30E-09

+ CJO=7.64E-13 PB=0.60000 M=0.17000 )
ENDL
*
LIBRARY FD700
MODEL FD700 D( IS=5.15E-11 RS=5.670 N=1.5992 TT=4.42E-10

+ CJO=7.73E-13 PB=1.04000 M=0.07970 )
ENDL
*
LIBRARY D1N746A
MODEL D1N746A D( IS=1.40E-10 RS=0.010 N=1.0000 TT=1.01E-07

+ CJO=1.30E-09 PB=1.00000 M=0.47000 BV=3.30 IBV=1.00E-02 )
ENDL
*
MODEL D1N747A D( IS=1.38E-10 RS=24.000 N=1.1450 TT=1.05E-07
LIBRARY D1N747A

+ CJO=5.05E-12 PB=0.75000 M=0.50000 BV=3.60 IBV=1.92E-02 )
ENDL
*
LIBRARY D1N748A
MODEL D1N748A D( IS=1.14E-10 RS=23.000 N=1.1518 TT=1.00E-07

+ CJO=4.78E-10 PB=0.75000 M=0.50000 BV=3.90 IBV=2.00E-02 )
ENDL
*
LIBRARY D1N749A
MODEL D1N749A D( IS=8.95E-11 RS=22.000 N=1.1587 TT=9.35E-08

+ CJO=4.56E-10 PB=0.75000 M=0.50000 BV=4.30 IBV=2.00E-02 )
ENDL
*
LIBRARY D1N750A
MODEL D1N750A D( IS=4.84E-11 RS=19.000 N=1.1835 TT=8.91E-08

+ CJO=4.25E-10 PB=0.75000 M=0.50000 BV=4.70 IBV=2.00E-02 )
ENDL
*
LIBRARY D1N751A
MODEL D1N751A D( IS=3.80E-11 RS=17.000 N=1.2056 TT=8.55E-08

+ CJO=4.08E-10 PB=0.75000 M=0.50000 BV=5.10 IBV=2.00E-02 )
ENDL
*
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LIBRARY D1N752A
MODEL D1N752A D( IS=1.25E-11 RS=11.000 N=1.2565 TT=8.01E-08

+ CJO=3.82E-10 PB=0.75000 M=0.50000 BV=5.60 IBV=2.27E-02 )
ENDL
*
LIBRARY D1N753A
MODEL D1N753A D( IS=6.25E-12 RS=7.000 N=1.2900 TT=7.39E-08

+ CJO=3.52E-10 PB=0.75000 M=0.50000 BV=6.20 IBV=2.00E-02 )
ENDL
*
LIBRARY D1N754A
MODEL D1N754A D( IS=4.60E-12 RS=5.000 N=1.3030 TT=6.90E-08

+ CJO=3.29E-10 PB=0.75000 M=0.50000 BV=6.80 IBV=2.00E-02 )
ENDL
*
LIBRARY D1N755A
MODEL D1N755A D( IS=5.18E-10 RS=6.000 N=1.2943 TT=6.41E-08

+ CJO=3.06E-10 PB=0.75000 M=0.50000 BV=7.50 IBV=2.00E-02 )
ENDL
*
LIBRARY D1N756A
MODEL D1N756A D( IS=7.24E-12 RS=8.000 N=1.2772 TT=5.76E-08

+ CJO=2.75E-10 PB=0.75000 M=0.50000 BV=8.20 IBV=2.00E-02 )
ENDL
*
LIBRARY D1N757A
MODEL D1N757A D( IS=1.04E-11 RS=10.000 N=1.2647 TT=5.30E-08

+ CJO=2.53E-10 PB=0.75000 M=0.50000 BV=9.10 IBV=2.00E-02 )
ENDL
*
LIBRARY D1N758A
MODEL D1N758A D( IS=3.40E-11 RS=17.000 N=1.2019 TT=4.81E-08

+ CJO=2.30E-10 PB=0.75000 M=0.50000 BV=10.00 IBV=2.00E-02 )
ENDL
*
LIBRARY D1N759A
MODEL D1N759A D( IS=5.05E-10 RS=30.000 N=1.0932 TT=4.34E-08

+ CJO=2.07E-10 PB=0.75000 M=0.50000 BV=12.00 IBV=2.00E-02 )
ENDL
*
LIBRARY D1N903
MODEL D1N903 D( IS=7.60E-12 RS=100.000 N=1.3627 TT=3.10E-08

+ CJO=1.37E-12 PB=0.80000 M=0.24000 )
ENDL
*
LIBRARY D1N914
MODEL D1N914 D( IS=2.90E-09 RS=2.000 N=1.8000 TT=4.68E-07
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+ CJO=2.53E-11 PB=0.90000 M=0.50000 )
ENDL
*
LIBRARY D1N914B
MODEL D1N914B D( IS=8.70E-10 RS=2.000 N=1.6125 TT=8.27E-08

+ CJO=2.45E-12 PB=0.90000 M=0.19000 )
ENDL
*
LIBRARY D1N962B
MODEL D1N962B D( IS=6.00E-12 RS=0.400 N=1.0000 TT=1.10E-07

+ CJO=2.56E-11 PB=1.00000 M=0.43000 BV=11.00 IBV=.350 )
ENDL
*
LIBRARY D1N963B
MODEL D1N963B D( IS=4.25E-12 RS=11.500 N=1.1622 TT=1.12E-07

+ CJO=3.83E-10 PB=0.75000 M=0.50000 BV=12.00 IBV=1.04E-02 )
ENDL
*
LIBRARY D1N964B
MODEL D1N964B D( IS=9.40E-12 RS=13.000 N=1.1518 TT=1.12E-07

+ CJO=3.83E-10 PB=0.75000 M=0.50000 BV=13.00 IBV=9.23E-03 )
ENDL
*
LIBRARY D1N965B
MODEL D1N965B D( IS=1.37E-11 RS=16.000 N=1.1349 TT=9.84E-08

+ CJO=3.35E-12 PB=0.75000 M=0.50000 BV=15.00 IBV=8.75E-03 )
ENDL
*
LIBRARY D1N966B
MODEL D1N966B D( IS=1.37E-11 RS=17.000 N=1.1217 TT=9.84E-08

+ CJO=3.35E-10 PB=0.75000 M=0.50000 BV=16.00 IBV=7.65E-03 )
ENDL
*
LIBRARY D1N967B
MODEL D1N967B D( IS=4.35E-11 RS=21.000 N=1.0840 TT=9.84E-08

+ CJO=3.35E-10 PB=0.75000 M=0.50000 BV=18.00 IBV=7.14E-03 )
ENDL
*
LIBRARY D1N968B
MODEL D1N968B D( IS=9.90E-11 RS=25.000 N=1.0488 TT=9.46E-08
ENDL
*
LIBRARY D1N969B
MODEL D1N969B D( IS=2.53E-10 RS=29.000 N=1.0157 TT=8.99E-08

+ CJO=3.06E-10 PB=0.75000 M=0.50000 BV=22.00 IBV=5.52E-03 )
ENDL
*
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LIBRARY D1N971B
MODEL D1N971B D( IS=5.60E-09 RS=41.000 N=0.9149 TT=6.74E-08

+ CJO=2.30E-10 PB=0.75000 M=0.50000 BV=27.00 IBV=4.63E-03 )
ENDL
*
LIBRARY D1N972B
MODEL D1N972B D( IS=9.50E-11 RS=49.000 N=1.0459 TT=6.74E-08

+ CJO=2.30E-10 PB=0.75000 M=0.50000 BV=30.00 IBV=4.08E-03 )
ENDL
*
LIBRARY D1N995
MODEL D1N995 D( IS=7.30E-07 RS=15.000 N=1.4333 TT=1.76E-08

+ CJO=4.00E-12 PB=0.50000 M=0.50000 )
ENDL
*
LIBRARY FDM1000
MODEL FDM1000 D( IS=4.04E-09 RS=4.500 N=1.9645 TT=2.57E-09

+ CJO=9.77E-13 PB=1.00000 M=0.27400 )
ENDL
*
LIBRARY D1N2199
MODEL D1N2199 D( IS=2.00E-09 RS=10.000 N=1.7124 TT=1.33E-08

+ CJO=1.99E-12 PB=0.50000 M=0.50000 )
ENDL
*
MODEL H2969 D( IS=1.00E-04 RS=2.000 N=3.9897 TT=1.50E-09
LIBRARY H2969

+ CJO=4.07E-12 PB=0.80000 M=0.08000 )
ENDL
*
LIBRARY D1N3016
MODEL D1N3016B D( IS=2.53E-10 RS=3.500 N=1.3921 TT=2.03E-07

+ CJO=6.87E-10 PB=0.75000 M=0.50000 BV=6.80 IBV=3.71E-02 )
ENDL
*
LIBRARY D1N3017B
MODEL D1N3017B D( IS=5.95E-10 RS=4.000 N=1.3921 TT=2.03E-07

+ CJO=6.87E-12 PB=0.75000 M=0.50000 BV=7.50 IBV=3.50E-02 )
ENDL
*
LIBRARY D1N3018B
MODEL D1N3018B D( IS=2.81E-10 RS=4.500 N=1.3921 TT=2.03E-07

+ CJO=6.87E-12 PB=0.75000 M=0.50000 BV=8.20 IBV=3.11E-02 )
ENDL
*
LIBRARY D1N3019B
MODEL D1N3019B D( IS=2.94E-10 RS=5.000 N=1.3821 TT=2.03E-07
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+ CJO=6.87E-10 PB=0.75000 M=0.50000 BV=9.10 IBV=2.80E-02 )
ENDL
*
LIBRARY D1N3020B
MODEL D1N3020B D( IS=4.55E-10 RS=7.000 N=1.3723 TT=1.68E-07

+ CJO=5.73E-10 PB=0.75000 M=0.50000 BV=10.00 IBV=2.43E-02 )
ENDL
*
LIBRARY D1N3021B
MODEL D1N3021B D( IS=1.77E-10 RS=8.000 N=1.3531 TT=1.68E-07

+ CJO=5.73E-10 PB=0.75000 M=0.50000 BV=11.00 IBV=2.25E-02 )
ENDL
*
LIBRARY D1N3022B
MODEL D1N3022B D( IS=1.77E-10 RS=9.000 N=1.3531 TT=1.68E-07

+ CJO=5.73E-12 PB=0.75000 M=0.50000 BV=12.00 IBV=2.11E-02 )
ENDL
*
LIBRARY D1N3023B
MODEL D1N3023B D( IS=2.84E-10 RS=10.000 N=1.3437 TT=1.62E-07

+ CJO=5.51E-10 PB=0.75000 M=0.50000 BV=13.00 IBV=1.90E-02 )
ENDL
*
LIBRARY D1N3024B
MODEL D1N3024B D( IS=2.84E-10 RS=14.000 N=1.3030 TT=1.62E-07

+ CJO=5.51E-10 PB=0.75000 M=0.50000 BV=15.00 IBV=1.71E-02 )
ENDL
*
LIBRARY D1N3025B
MODEL D1N3025B D( IS=2.84E-10 RS=16.000 N=1.2857 TT=1.53E-07

+ CJO=5.20E-10 PB=0.75000 M=0.50000 BV=16.00 IBV=1.56E-02 )
ENDL
*
LIBRARY D1N3026B
MODEL D1N3026B D( IS=4.46E-10 RS=20.000 N=1.2647 TT=1.53E-07

+ CJO=5.20E-10 PB=0.75000 M=0.50000 BV=18.00 IBV=1.40E-02 )
ENDL
*
LIBRARY D1N3027B
MODEL D1N3027B D( IS=4.55E-10 RS=22.000 N=1.2325 TT=1.44E-07

+. CJO=4.91E-10 PB=0.75000 M=0.50000 BV=20.00 IBV=1.23E-02 )
ENDL
*
LIBRARY D1N3028B
MODEL D1N3028B D( IS=4.55E-10 RS=23.000 N=1.2286 TT=1.44E-07
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+ CJO=4.91E-10 PB=0.75000 M=0.50000 BV=22.00 IBV=1.13E-02 )
ENDL
*
LIBRARY D1N3070B
MODEL D1N3070 D( IS=4.23E-09 RS=1.650 N=1.7752 TT=1.62E-08

+ CJO=1.76E-12 PB=1.00000 M=0.16600 )
ENDL
*
LIBRARY D1N3071
MODEL D1N3071 D( IS=9.10E-09 RS=1.600 N=1.9350 TT=4.13E-07

+ CJO=2.00E-12 PB=1.00000 M=0.19000 )
ENDL
*
LIBRARY D1N3600
MODEL D1N3600 D( IS=5.06E-09 RS=0.600 N=1.8517 TT=1.03E-10

+ CJO=9.07E-13 PB=0.85000 M=0.05000 )
ENDL
*
LIBRARY D1N3605
MODEL D1N3605 D( IS=3.77E-09 RS=0.777 N=1.9545 TT=2.95E-09

+ CJO=9.98E-13 PB=1.28000 M=0.04970 )
ENDL
*
LIBRARY D1N3669
MODEL D1N3669 D( IS=1.30E-10 RS=2.000 N=1.3821 TT=3.36E-07

+ CJO=2.55E-11 PB=0.80000 M=0.46000 )
ENDL
*
LIBRARY D1N4001
MODEL D1N4001 D( IS=1.02E-08 RS=0.054 N=1.9017 TT=4.39E-06

+ CJO=3.00E-11 PB=0.81000 M=0.50000 )
ENDL
*
LIBRARY D1N4003
MODEL D1N4003 D( IS=4.20E-09 RS=0.500 N=1.7591 TT=3.88E-06

+ CJO=2.30E-10 PB=1.00000 M=0.48000 )
ENDL
*
LIBRARY UT4410
MODEL UT4410 D( IS=9.18E-11 RS=0.200 N=1.0963 TT=6.36E-09

+ CJO=1.15E-10 PB=0.75000 M=0.50000 )
ENDL
*
LIBRARY D1N4610
MODEL D1N4610 D( IS=2.52E-09 RS=0.392 N=1.7432 TT=1.33E-09

+ CJO=1.57E-12 PB=0.10000 M=0.04930 )
ENDL
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*
LIBRARY SLC8077
MODEL SLC8077 D( IS=5.25E-12 RS=1.100 N=1.4828 TT=3.36E-07

+ CJO=3.00E-12 PB=1.00000 M=0.50000 )
ENDL
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*
*
*
*********************************************
*                                    *
*.    BIPOLAR JUNCTION TRANSISTOR            *
*                                    *
*********************************************
*
*
*
*
LIBRARY T2N910
MODEL T2N910 NPN( BF=91.93 C2=15.0 NE=1.5 IK=0.060

+ IS=1.83E-14 VA=100.0 VB=20.0 BR=4.509 C4=0.0 NC=1.5 IKR=0.060

+ CJC=2.27E-11 MC=0.310 PC=0.900 CJE=5.11E-11 ME=0.200 PE=0.900

+ RC=8.000 RB=13.000 RE=.300 TF=2.63E-09 TR=1.10E-07 )
ENDL
*
LIBRARY T2N914
MODEL T2N914 NPN( BF=115.27 C2=14.9 NE=1.5 IK=0.050

+ IS=7.73E-15 VA=100.0 VB=20.0 BR=0.817 C4=0.0 NC=1.5 IKR=0.050

+ CJC=4.76E-12 MC=0.130 PC=0.900 CJE=6.34E-12 ME=0.320 PE=0.800

+ RC=9.100 RB=25.000 RE=1.00 TF=3.83E-10 TR=2.55E-07 )
ENDL
*
LIBRARY T2N918
MODEL T2N918 NPN( BF=59.47 C2=39.3 NE=1.5 IK=0.025

+ IS=1.55E-15 VA=100.0 VB=20.0 BR=0.573 C4=0.0 NC=1.5 IKR=0.025

+ CJC=1.75E-12 MC=0.120 PC=0.800 CJE=2.22E-12 ME=0.150 PE=0.500

+ RC=11.500 RB=12.000 RE=8.50 TF=2.14E-10 TR=3.27E-08 )
ENDL
*
LIBRARY T2N995
MODEL T2N995 PNP( BF=98.60 C2=101. NE=1.5 IK=0.200

+ IS=1.52E-16 VA=100.0 VB=20.0 BR=1.175 C4=0.0 NC=1.5 IKR=0.200

+ CJC=1.52E-11 MC=0.176 PC=1.010 CJE=1.24E-11 ME=0.320 PE=1.080
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+ RC=2.000 RB=25.000 RE=1.00E-06 TF=2.91E-08 TR=5.18E-07 )
ENDL
*
LIBRARY T2N1131
MODEL T2N1131 PNP( BF=27.767 C2=122. NE=1.5 IK=2.747

+ IS=5.49E-14 VA=100.0 VB=20.0 BR=3.471 C4=0.0 NC=1.5 IKR=2.747

+ CJC=7.37E-11 MC=0.361 PC=0.963 CJE=6.58E-11 ME=0.496 PE=1.630

+ RC=0.100 RB=1.820 RE=1.00E-6 TF=2.71E-09 TR=1.58E-08 )
ENDL
*
LIBRARY T2N1132
MODEL T2N1132 PNP( BF=76.378 C2=39.8 NE=1.5 IK=0.071

+ IS=1.99E-15 VA=100.0 VB=20.0 BR=1.056 C4=0.0 NC=1.5 IKR=0.071

+ CJC=7.45E-11 MC=0.361 PC=0.936 CJE=6.58E-11 ME=0.496 PE=1.630

+ RC=7.000 RB=6.500 RE=1.00E-6 TF=5.61E-09 TR=4.45E-08 )
ENDL
*
LIBRARY T2N1228
MODEL T2N1228 PNP( BF=22.329 C2=923. NE=1.5 IK=2.500

+ IS=2.11E-16 VA=100.0 VB=20.0 BR=0.690 C4=0.0 NC=1.5 IKR=2.500

+ CJC=1.37E-10 MC=0.176 PC=1.010 CJE=1.74E-10 ME=0.320 PE=1.080

+ RC=0.100 RB=2.000 RE=1.00E-6 TF=7.88E-08 TR=2.10E-06 )
ENDL
*
LIBRARY T2N1289
MODEL T2N1289 NPN( BF=1.400 C2=11.3 NE=1.5 IK=0.025

+ IS=5.77E-09 VA=100.0 VB=20.0 BR=9.000 C4=0.0 NC=1.5 IKR=0.025

+ CJC=1.73E-11 MC=0.500 PC=0.500 CJE=1.73E-11 ME=0.500 PE=0.500

+ RC=20.000 RB=10.000 RE=1.00E-6 TF=4.01E-09 TR=1.78E-08 )
ENDL
*
LIBRARY T2N1342
MODEL T2N1342 NPN( BF=60.274 C2=27.4 NE=1.5 IK=0.192

+ IS=3.40E-14 VA=100.0 VB=20.0 BR=1.614 C4=0.0 NC=1.5 IKR=0.192

+ CJC=1.87E-11 MC=0.430 PC=0.800 CJE=3.99E-11 ME=0.340 PE=0.800

+ RC=2.600 RB=12.000 RE=1.00E-6 TF=1.57E-09 TR=5.15E-07 )
ENDL
*
LIBRARY T2N1483
MODEL T2N1483 NPN( BF=27.767 C2=57.5 NE=1.5 IK=0.187
```

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+ IS=3.67E-14 VA=100.0 VB=20.0 BR=4.988 C4=0.0 NC=1.5 IKR=0.187

+ CJC=7.56E-10 MC=0.333 PC=0.500 CJE=3.88E-10 ME=0.330 PE=0.500

+ RC=2.670 RB=12.000 RE=1.00E-6 TF=1.28E-07 TR=1.92E-06 )
ENDL
*
LIBRARY T2N1490
MODEL T2N1490 NPN( BF=68.600 C2=39.4 NE=1.5 IK=0.250

+ IS=9.96E-15 VA=100.0 VB=20.0 BR=0.247 C4=0.0 NC=1.5 IKR=0.250

+ CJC=2.91E-12 MC=0.079 PC=1.100 CJE=3.25E-12 ME=0.310 PE=1.060

+ RC=2.000 RB=20.000 RE=1.00E-6 TF=3.07E-10 TR=9.74E-09 )
ENDL
*
LIBRARY T2N1506A
MODEL T2N1506A NPN( BF=40.020 C2=30.8 NE=1.5 IK=0.217

+ IS=9.32E-14 VA=100.0 VB=20.0 BR=5.003 C4=0.0 NC=1.5 IKR=0.217

+ CJC=5.14E-11 MC=0.500 PC=0.800 CJE=1.62E-10 ME=0.390 PE=0.900

+ RC=1.000 RB=23.000 RE=1.00E-6 TF=8.06E-10 TR=3.97E-07 )
ENDL
*
LIBRARY T2N1724
MODEL T2N1724 NPN( BF=56.933 C2=24.2 NE=1.5 IK=0.005

+ IS=1.55E-15 VA=100.0 VB=20.0 BR=7.117 C4=0.0 NC=1.5 IKR=0.005

+ CJC=1.00E-09 MC=0.399 PC=0.921 CJE=2.40E-09 ME=0.399 PE=0.921

+ RC=99.000 RB=99.000 RE=1.00E-6 TF=9.04E-09 TR=1.03E-07 )
ENDL
*
LIBRARY T2N2126
MODEL T2N2126 NPN( BF=35.44 C2=1.63E+03 NE=1.5 IK=11.10

+ IS=4.15E-17 VA=100.0 VB=20.0 BR=4.430 C4=0.0 NC=1.5 IKR=11.10

+ CJC=2.64E-09 MC=0.410 PC=0.800 CJE=1.79E-09 ME=0.500 PE=0.800

+ RC=0.025 RB=0.350 RE=0.01 TF=3.02E-07 TR=4.69E-06 )
ENDL
*
LIBRARY T2N2188
MODEL T2N2188 PNP( BF=115.27 C2=3.81E-02 NE=1.5 IK=0.250

+ IS=2.82E-06 VA=100.0 VB=20.0 BR=14.408 C4=0.0 NC=1.5 IKR=0.250

+ CJC=4.27E-11 MC=0.333 PC=0.500 CJE=1.71E-11 ME=0.333 PE=0.500

+ RC=2.000 RB=5.000 RE=1.00E-6 TF=1.02E-09 TR=1.96E-08 )
ENDL
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*
LIBRARY T2N2243A
MODEL T2N2243A NPN( BF=125.87 C2=5.58 NE=1.5 IK=0.040

+ IS=9.56E-14 VA=100.0 VB=20.0 BR=2.912 C4=0.0 NC=1.5 IKR=0.040

+ CJC=3.29E-11 MC=0.410 PC=0.800 CJE=7.34E-11 ME=0.410 PE=0.800

+ RC=10.000 RB=124.000 RE=1.00E-6 TF=9.82E-10 TR=3.65E-07 )
ENDL
*
LIBRARY T2N2187
MODEL T2N2187 PNP( BF=46.22 C2=16.4 NE=1.5 IK=0.033

+ IS=6.21E-14 VA=100.0 VB=20.0 BR=1.032 C4=0.0 NC=1.5 IKR=0.033

+ CJC=9.03E-12 MC=0.410 PC=0.700 CJE=5.85E-12 ME=0.360 PE=0.800

+ RC=15.000 RB=10.000 RE=1.00E-6 TF=5.02E-11 TR=3.47E-10 )
ENDL
*
LIBRARY T2N2223
MODEL T2N2223 NPN( BF=104.66 C2=7.64 NE=1.5 IK=0.056

+ IS=8.87E-14 VA=100.0 VB=20.0 BR=0.052 C4=0.0 NC=1.5 IKR=0.056

+ CJC=3.45E-11 MC=0.410 PC=0.900 CJE=6.47E-11 ME=0.410 PE=0.800

+ RC=9.000 RB=32.000 RE=1.00E-6 TF=4.08E-11 TR=2.95E-07 )
ENDL
*
LIBRARY T2N2845
MODEL T2N2845 NPN( BF=70.03 C2=25.6 NE=1.5 IK=0.200

+ IS=2.76E-14 VA=100.0 VB=20.0 BR=2.580 C4=0.0 NC=1.5 IKR=0.200

+ CJC=9.22E-12 MC=0.230 PC=0.900 CJE=4.78E-12 ME=0.370 PE=0.900

+ RC=2.000 RB=25.000 RE=1.00E-6 TF=1.52E-11 TR=5.59E-10 )
ENDL
*
LIBRARY T2N2887
MODEL T2N2887 NPN( BF=67.57 C2=20.8 NE=1.5 IK=0.385

+ IS=1.12E-13 VA=100.0 VB=20.0 BR=0.296 C4=0.0 NC=1.5 IKR=0.385

+ CJC=1.15E-10 MC=0.490 PC=0.800 CJE=4.58E-10 ME=0.390 PE=0.900

+ RC=0.300 RB=13.000 RE=1.00E-6 TF=2.74E-10 TR=2.04E-06 )
ENDL
*
LIBRARY T2N3021
MODEL T2N3021 PNP( BF=56.93 C2=1.08 NE=1.5 IK=0.510

+ IS=1.96E-09 VA=100.0 VB=20.0 BR=0.480 C4=0.0 NC=1.5 IKR=0.510
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+ CJC=4.10E-10 MC=0.434 PC=0.614 CJE=6.51E-10 ME=0.475 PE=1.220

+ RC=0.300 RB=7.800 RE=.200 TF=2.97E-10 TR=1.17E-06 )
ENDL
*
LIBRARY T2N3026
MODEL T2N3026 PNP( BF=173.60 C2=.357 NE=1.5 IK=0.510

+ IS=1.89E-09 VA=100.0 VB=20.0 BR=1.007 C4=0.0 NC=1.5 IKR=0.510

+ CJC=4.10E-10 MC=0.434 PC=0.614 CJE=6.51E-10 ME=0.475 PE=1.220

+ RC=0.400 RB=7.800 RE=.200 TF=1.19E-10 TR=3.93E-07 )
ENDL
*
LIBRARY T2N3117
MODEL T2N3117 NPN( BF=698.61 C2=37.9 NE=1.5 IK=0.357

+ IS=1.42E-17 VA=100.0 VB=20.0 BR=0.136 C4=0.0 NC=1.5 IKR=0.357

+ CJC=8.69E-12 MC=0.350 PC=0.900 CJE=7.16E-12 ME=0.400 PE=0.900

+ RC=1.400 RB=2.180 RE=1.00E-6 TF=7.62E-10 TR=6.81E-08 )
ENDL
*
LIBRARY T2N3244
MODEL T2N3244 PNP( BF=161.39 C2=7.63 NE=1.5 IK=0.250

+ IS=1.08E-13 VA=100.0 VB=20.0 BR=6.875 C4=0.0 NC=1.5 IKR=0.250

+ CJC=4.71E-11 MC=0.410 PC=0.800 CJE=5.50E-11 ME=0.450 PE=1.000

+ RC=1.400 RB=20.000 RE=1.00E-6 TF=4.86E-10 TR=5.77E-08 )
ENDL
*
LIBRARY T2N3468
MODEL T2N3468 PNP( BF=48.60 C2=70.6 NE=1.5 IK=0.515

+ IS=9.99E-15 VA=100.0 VB=20.0 BR=0.140 C4=0.0 NC=1.5 IKR=0.515

+ CJC=6.42E-11 MC=0.380 PC=0.900 CJE=1.24E-10 ME=0.490 PE=0.900

+ RC=0.220 RB=1.000 RE=.750 TF=7.72E-10 TR=9.14E-07 )
ENDL
*
LIBRARY T2N3498
MODEL T2N3498 NPN( BF=115.27 C2=8.30 NE=1.5 IK=0.169

+ IS=1.57E-13 VA=100.0 VB=20.0 BR=2.849 C4=0.0 NC=1.5 IKR=0.169

+ CJC=1.98E-11 MC=0.378 PC=0.900 CJE=6.55E-11 ME=0.518 PE=1.280

+ RC=1.660 RB=12.700 RE=1.30 TF=2.26E-09 TR=9.61E-07 )
ENDL
*
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LIBRARY T2N3501
MODEL T2N3501 NPN( BF=198.60 C2=15.8 NE=1.5 IK=3.472

+ IS=8.86E-14 VA=100.0 VB=20.0 BR=24.825 C4=0.0 NC=1.5 IKR=3.472

+ CJC=6.83E-11 MC=0.330 PC=0.500 CJE=1.01E-10 ME=0.330 PE=0.500

+ RC=0.100 RB=1.440 RE=1.00E-06 TF=1.78E-09 TR=6.48E-09 )
ENDL
*
LIBRARY T2N3502
MODEL T2N3502 PNP( BF=278.60 C2=3.11 NE=1.5 IK=0.071

+ IS=8.90E-14 VA=100.0 VB=20.0 BR=1.585 C4=0.0 NC=1.5 IKR=0.071

+ CJC=1.10E-11 MC=0.361 PC=0.936 CJE=1.71E-11 ME=0.496 PE=1.630

+ RC=7.000 RB=6.500 RE=1.00E-06 TF=6.12E-09 TR=4.07E-08 )
ENDL
*
LIBRARY T2N3503
MODEL T2N3503 PNP( BF=278.60 C2=6.43 NE=1.5 IK=0.071

+ IS=9.90E-15 VA=100.0 VB=20.0 BR=1.272 C4=0.0 NC=1.5 IKR=0.071

+ CJC=1.10E-11 MC=0.361 PC=0.936 CJE=1.72E-11 ME=0.490 PE=1.630

+ RC=7.000 RB=6.500 RE=1.00E-06 TF=5.61E-09 TR=4.09E-08 )
ENDL
*
LIBRARY T2N3600
MODEL T2N3600 NPN( BF=59.47 C2=1.68 NE=1.5 IK=0.025

+ IS=2.18E-11 VA=100.0 VB=20.0 BR=7.434 C4=0.0 NC=1.5 IKR=0.025

+ CJC=1.75E-12 MC=0.120 PC=0.800 CJE=2.22E-12 ME=0.150 PE=0.500

+ RC=11.500 RB=12.000 RE=8.50 TF=1.71E-10 TR=1.03E-08 )
ENDL
*
LIBRARY T2N3635
MODEL T2N3635 PNP( BF=138.60 C2=13.1 NE=1.5 IK=0.071

+ IS=9.49E-15 VA=100.0 VB=20.0 BR=1.237 C4=0.0 NC=1.5 IKR=0.071

+ CJC=3.25E-11 MC=0.361 PC=0.936 CJE=6.53E-11 ME=0.496 PE=1.630

+ RC=7.000 RB=6.500 RE=1.00E-06 TF=5.61E-10 TR=1.03E-08 )
ENDL
*
LIBRARY T2N3737
MODEL T2N3737 NPN( BF=98.60 C2=41.6 NE=1.5 IK=0.207

+ IS=2.33E-15 VA=100.0 VB=20.0 BR=0.956 C4=0.0 NC=1.5 IKR=0.207

+ CJC=9.84E-12 MC=0.270 PC=0.750 CJE=7.90E-11 ME=0.370 PE=0.750
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+ RC=0.100 RB=20.000 RE=.420 TF=3.08E-11 TR=1.43E-07 )
ENDL
*
LIBRARY T2N3738
MODEL T2N3738 NPN( BF=138.60 C2=.765 NE=1.5 IK=0.181

+ IS=1.32E-10 VA=100.0 VB=20.0 BR=0.190 C4=0.0 NC=1.5 IKR=0.181

+ CJC=4.77E-11 MC=0.340 PC=0.900 CJE=2.16E-10 ME=0.378 PE=0.900

+ RC=0.490 RB=19.200 RE=.840 TF=6.57E-07 TR=5.41E-05 )
ENDL
*
LIBRARY T2N3766
MODEL T2N3766 NPN( BF=138.60 C2=3.87 NE=1.5 IK=0.185

+ IS=9.89E-13 VA=100.0 VB=20.0 BR=0.031 C4=0.0 NC=1.5 IKR=0.185

+ CJC=1.18E-10 MC=0.312 PC=1.150 CJE=2.30E-10 ME=0.428 PE=0.940

+ RC=0.320 RB=23.000 RE=.410 TF=8.57E-09 TR=9.48E-06 )
ENDL
*
LIBRARY T2N3792
MODEL T2N3792 PNP( BF=198.60 C2=7.13 NE=1.5 IK=0.059

+ IS=1.66E-14 VA=100.0 VB=20.0 BR=0.060 C4=0.0 NC=1.5 IKR=0.059

+ CJC=2.62E-10 MC=0.300 PC=0.750 CJE=5.28E-10 ME=0.330 PE=0.750

+ RC=8.000 RB=2.400 RE=.500 TF=2.76E-08 TR=3.13E-06 )
ENDL
*
LIBRARY T2N3913
MODEL T2N3913 PNP( BF=138.60 C2=6.24 NE=1.5 IK=0.013


+ IS=1.58E-14 VA=100.0 VB=20.0 BR=11.331 C4=0.0 NC=1.5 IKR=0.013

+ CJC=2.35E-11 MC=0.500 PC=0.800 CJE=2.35E-11 ME=0.500 PE=0.800

+ RC=34.000 RB=127.000 RE=5.80 TF=5.68E-09 TR=6.97E-08 )
ENDL
*
LIBRARY T2N3914
MODEL T2N3914 PNP( BF=231.93 C2=5.27 NE=1.5 IK=0.020

+ IS=8.88E-15 VA=100.0 VB=20.0 BR=21.868 C4=0.0 NC=1.5 IKR=0.020

+ CJC=2.35E-11 MC=0.500 PC=0.800 CJE=2.35E-11 ME=0.500 PE=0.800

+ RC=21.000 RB=129.000 RE=3.80 TF=2.91E-09 TR=4.24E-08 )
ENDL
*
```

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LIBRARY T2N3915
MODEL T2N3915 PNP( BF=465.26 C2=3.40 NE=1.5 IK=0.025

+ IS=5.04E-15 VA=100.0 VB=20.0 BR=34.834 C4=0.0 NC=1.5 IKR=0.025

+ CJC=2.35E-11 MC=0.500 PC=0.800 CJE=2.35E-11 ME=0.500 PE=0.800

+ RC=18.000 RB=131.000 RE=2.10 TF=1.53E-09 TR=2.94E-08 )
ENDL
*
LIBRARY T2N4125
MODEL T2N4125 PNP( BF=138.60 C2=1.54 NE=1.5 IK=0.030

+ IS=2.68E-12 VA=100.0 VB=20.0 BR=17.325 C4=0.0 NC=1.5 IKR=0.030

+ CJC=3.45E-12 MC=0.266 PC=0.750 CJE=3.91E-12 ME=0.188 PE=0.750

+ RC=0.800 RB=150.000 RE=1.40 TF=3.76E-10 TR=1.05E-08 )
ENDL
*
LIBRARY T2N3960
MODEL T2N3960 NPN( BF=76.38 C2=87.7 NE=1.5 IK=0.085

+ IS=2.16E-16 VA=100.0 VB=20.0 BR=0.426 C4=0.0 NC=1.5 IKR=0.085

+ CJC=4.04E-12 MC=0.261 PC=0.750 CJE=3.01E-12 ME=0.246 PE=0.750

+ RC=1.500 RB=39.000 RE=2.00 TF=9.65E-11 TR=2.66E-10 )
ENDL
*
LIBRARY T2N718A
MODEL T2N718A NPN( BF=115.27 C2=9.41 NE=1.5 IK=0.077

+ IS=4.88E-14 VA=100.0 VB=20.0 BR=3.204 C4=0.0 NC=1.5 IKR=0.077

+ CJC=4.68E-11 MC=0.370 PC=0.900 CJE=7.89E-11 ME=0.360 PE=0.900

+ RC=5.600 RB=60.000 RE=.500 TF=5.34E-09 TR=3.44E-07 )
ENDL
*
LIBRARY T2N797
MODEL T2N797 NPN( BF=56.93 C2=.443 NE=1.5 IK=0.033

+ IS=1.88E-09 VA=100.0 VB=20.0 BR=7.117 C4=0.0 NC=1.5 IKR=0.033

+ CJC=8.89E-12 MC=0.333 PC=0.500 CJE=5.77E-12 ME=0.333 PE=0.500

+ RC=5.000 RB=150.000 RE=1.00E-06 TF=2.76E-10 TR=1.82E-09 )
ENDL
*
LIBRARY T2N976
MODEL T2N976 PNP( BF=115.27 C2=4.39E-02 NE=1.5 IK=0.100

+ IS=7.32E-07 VA=100.0 VB=20.0 BR=14.408 C4=0.0 NC=1.5 IKR=0.100

+ CJC=2.86E-12 MC=0.293 PC=0.665 CJE=7.27E-12 ME=0.608 PE=0.862
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+ RC=2.000 RB=50.000 RE=1.00E-06 TF=1.45E-10 TR=2.79E-09 )
ENDL
*
LIBRARY T2N1225
MODEL T2N1225 PNP( BF=48.96 C2=.208 NE=1.5 IK=0.086

+ IS=7.57E-08 VA=100.0 VB=20.0 BR=0.523 C4=0.0 NC=1.5 IKR=0.086

+ CJC=3.69E-12 MC=0.190 PC=0.400 CJE=4.57E-12 ME=0.470 PE=0.500

+ RC=5.800 RB=20.000 RE=1.00E-06 TF=9.20E-09 TR=2.94E-07 )
ENDL
*
LIBRARY T2N1301
MODEL T2N1301 PNP( BF=98.60 C2=.533 NE=1.5 IK=0.100

+ IS=6.11E-10 VA=100.0 VB=20.0 BR=12.325 C4=0.0 NC=1.5 IKR=0.100

+ CJC=2.82E-11 MC=0.333 PC=0.500 CJE=1.74E-11 ME=0.333 PE=0.500

+ RC=5.000 RB=50.000 RE=1.00E-06 TF=4.57E-09 TR=1.73E-08 )
ENDL
*
LIBRARY T2N1499A
MODEL T2N1499A PNP( BF=42.35 C2=.120 NE=1.5 IK=0.050

+ IS=3.64E-07 VA=100.0 VB=20.0 BR=5.294 C4=0.0 NC=1.5 IKR=0.050

+ CJC=7.05E-12 MC=0.333 PC=0.500 CJE=7.21E-12 ME=0.333 PE=0.500

+ RC=10.000 RB=50.000 RE=1.00E-06 TF=6.02E-09 TR=1.38E-08 )
ENDL
*
LIBRARY T2N2048
MODEL T2N2048 PNP( BF=68.60 C2=7.51E-02 NE=1.5 IK=0.005

+ IS=3.48E-08 VA=100.0 VB=20.0 BR=9.000 C4=0.0 NC=1.5 IKR=0.005

+ CJC=1.89E-11 MC=0.333 PC=0.500 CJE=7.21E-11 ME=0.333 PE=0.500

+ RC=100. RB=100.000 RE=1.00E-06 TF=6.15E-10 TR=1.78E-08 )
ENDL
*
LIBRARY T2N2087
MODEL T2N2087 NPN( BF=56.93 C2=7.18 NE=1.5 IK=0.357

+ IS=4.35E-12 VA=100.0 VB=20.0 BR=0.418 C4=0.0 NC=1.5 IKR=0.357

+ CJC=3.31E-11 MC=0.333 PC=0.500 CJE=8.82E-11 ME=0.333 PE=0.500

+ RC=1.000 RB=14.000 RE=1.00E-06 TF=1.07E-09 TR=1.09E-08 )
ENDL
*
LIBRARY T2N2102
MODEL T2N2102 NPN( BF=48.60 C2=264. NE=1.5 IK=12.5
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+ IS=4.45E-15 VA=100.0 VB=20.0 BR=4.143 C4=0.0 NC=1.5 IKR=12.5

+ CJC=2.12E-11 MC=0.373 PC=2.500 CJE=2.70E-11 ME=0.446 PE=1.250

+ RC=0.040 RB=0.120 RE=1.00E-06 TF=6.46E-07 TR=4.65E-07 )
ENDL
*
LIBRARY T2N2258
MODEL T2N2258 PNP( BF=68.60 C2=19.5 NE=1.5 IK=3.333

+ IS=1.12E-12 VA=100.0 VB=20.0 BR=8.575 C4=0.0 NC=1.5 IKR=3.333

+ CJC=1.71E-11 MC=0.200 PC=0.200 CJE=4.21E-11 ME=0.300 PE=0.800

+ RC=0.100 RB=1.500 RE=1.00E-06 TF=2.92E-09 TR=2.13E-07 )
ENDL
*
LIBRARY T2N2695
MODEL T2N2695 PNP( BF=125.87 C2=14.2 NE=1.5 IK=0.122

+ IS=1.69E-14 VA=100.0 VB=20.0 BR=0.718 C4=0.0 NC=1.5 IKR=0.122

+ CJC=1.97E-11 MC=0.330 PC=0.900 CJE=4.87E-11 ME=0.350 PE=0.800

+ RC=2.700 RB=40.000 RE=.100 TF=9.27E-10 TR=1.46E-07 )
ENDL
*
LIBRARY T2N3108
MODEL T2N3108 NPN( BF=56.93 C2=78.0 NE=1.5 IK=3.472

+ IS=3.07E-14 VA=100.0 VB=20.0 BR=7.117 C4=0.0 NC=1.5 IKR=3.472

+ CJC=5.47E-11 MC=0.330 PC=0.500 CJE=1.01E-10 ME=0.330 PE=0.500

+ RC=0.100 RB=1.440 RE=1.00E-06 TF=1.29E-09 TR=1.48E-08 )
ENDL
*
LIBRARY T2N3252
MODEL T2N3252 NPN( BF=56.93 C2=21.4 NE=1.5 IK=0.263

+ IS=1.18E-13 VA=100.0 VB=20.0 BR=4.894 C4=0.0 NC=1.5 IKR=0.263

+ CJC=1.47E-11 MC=0.230 PC=0.800 CJE=5.74E-11 ME=0.400 PE=0.900

+ RC=1.800 RB=18.000 RE=.100 TF=5.17E-10 TR=5.76E-08 )
ENDL
*
LIBRARY T2N3507
MODEL T2N3507 NPN( BF=106.29 C2=21.6 NE=1.5 IK=1.250


+ IS=8.18E-14 VA=100.0 VB=20.0 BR=13.287 C4=0.0 NC=1.5 IKR=1.250

+ CJC=4.23E-11 MC=0.250 PC=0.800 CJE=3.00E-10 ME=0.100 PE=1.000
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```
+ RC=0.200 RB=0.100 RE=.200 TF=1.83E-10 TR=9.59E-07 )
ENDL
*
LIBRARY T2N2219
MODEL T2N2219 NPN( BF=200.8 C2=153.1 NE=1.826 IK=.9321

+ IS=5.746E-14 VA=100.0 VB=20.00 BR=62.45 C4=16.08 NC=1.138 IKR=.2327

+ CJC=1.820E-11 MC=.5000 PC=1.000 CJE=2.667E-11 ME=.5000 PE=.9000

+ RC=2.619 RB=1.000E-09 RE=1.000E-06 TF=3.874E-10 TR=3.001E-07 )
ENDL
*
*
LIBRARY T2N2222
MODEL T2N2222 NPN( BF=241 C2=3.16 NE=1.35 IK=.35

+ IS=3.52E-14 VA=100 VB=100 BR=13.1 C4=60.6 NC=1.61 IKR=.106

+ CJE=23.8PF ME=.43 PE=1.0 CJC=14.7PF MC=.42 PC=1.0

+ RE=.26 RC=.30 RB=2.1 TF=.31NS TR=89NS )
ENDL
*
LIBRARY T2N706
MODEL T2N706 NPN( BF=519.0 C2=31.55 NE=1.428 IK=4.304E-02

+ IS=1.030E-14 VA=100.0 VB=20.0 BR=500.0 C4=83.88 NC=1.155 IKR=7.158E-02

+ CJC=4.500E-12 MC=.1400 PC=1.000 CJE=5.600E-12 ME=.3500 PE=.9000

+ RC=10.09 RB=3.500E-03 RE=.1000 TF=1.000E-10 TR=5.351E-07 )
ENDL
*
LIBRARY T2N722
MODEL T2N722 PNP( BF=493.8 C2=39.04 NE=1.395 IK=.1107

+ IS=1.050E-14 VA=100.0 VB=20.0 BR=500.0 C4=28.00 NC=1.134 IKR=.6077

+ CJC=1.660E-12 MC=.4500 PC=.8000 CJE=2.900E-11 ME=.4200 PE=1.000

+ RC=5.237 RB=8.920 RE=.1000 TF=1.604E-08 TR=6.243E-07 )
ENDL
*
LIBRARY T2N743
MODEL T2N743 NPN( BF=145.9 C2=46.01 NE=1.396 IK=.1786

+ IS=5.969E-15 VA=100.0 VB=20.0 BR=500.0 C4=62.70 NC=1.157 IKR=8.844E-02

+ CJC=5.600E-12 MC=.2500 PC=.8000 CJE=4.790E-12 ME=.3900 PE=.9000

+ RC=8.008 RB=203.2 RE=1.000E-06 TF=6.271E-10 TR=1.373E-07 )
ENDL
*
LIBRARY T2N834
MODEL T2N834 NPN( BF=1206. C2=46.24 NE=1.388 IK=5.509E-02
```

```
+ IS=3.593E-15 VA=100.0 VB=20.0 BR=500.0 C4=175.7 NC=1.107 IKR=4.528E-02

+ CJC=7.540E-12 MC=.3100 PC=.9000 CJE=1.010E-11 ME=.5000 PE=.8000

+ RC=9.619 RB=4.959 RE=1.000E-06 TF=1.333E-10 TR=1.031E-06 )
ENDL
*
LIBRARY T2N835
MODEL T2N835 NPN( BF=137.8 C2=39.42 NE=1.380 IK=2.582E-02

+ IS=3.465E-15 VA=100.0 VB=20.0 BR=500.0 C4=93.45 NC=1.141 IKR=1.105E-02

+ CJC=5.180E-12 MC=.1600 PC=.8000 CJE=7.460E-12 ME=.3400 PE=.9000

+ RC=17.59 RB=5.332 RE=.1000 TF=1.863E-09 TR=3.189E-06 )
ENDL
*
LIBRARY T2N915
MODEL T2N915 NPN( BF=236.5 C2=56.36 NE=1.571 IK=1.741E-02

+ IS=1.153E-14 VA=100.0 VB=20.0 BR=10.14 C4=179.6 NC=1.199 IKR=5.274E-03

+ CJC=5.040E-12 MC=.4100 PC=.8000 CJE=7.340E-12 ME=.3100 PE=.9000

+ RC=8.470 RB=3.941 RE=1.000 TF=1.502E-09 TR=1.030E-05 )
ENDL
*
LIBRARY T2N916
MODEL T2N916 NPN( BF=130.1 C2=117.0 NE=1.687 IK=4.458E-02

+ IS=4.846E-15 VA=100.0 VB=20.0 BR=3.416 C4=94.25 NC=1.175 IKR=1.044E-02

+ CJC=6.940E-12 MC=.3400 PC=.9000 CJE=7.530E-12 ME=.3000 PE=.9000

+ RC=31.88 RB=37.52 RE=1.000 TF=1.057E-09 TR=5.719E-06 )
ENDL
*
LIBRARY T2N1613
MODEL T2N1613 NPN( BF=300.0 C2=10.00 NE=1.500 IK=.2500

+ IS=2.296E-11 VA=100.0 VB=20.0 BR=5.328 C4=293.9 NC=1.988 IKR=1.183

+ CJC=2.660E-10 MC=4.460 PC=1.680 CJE=6.090E-11 ME=.3230 PE=.7130

+ RC=.9735 RB=1.458 RE=1.000E-06 TF=1.778E-09 TR=2.615E-08 )
ENDL
*
*
LIBRARY T2N2060
MODEL T2N2060 NPN( BF=100.2 C2=157.6 NE=1.519 IK=1.039

+ IS=6.762E-16 VA=100.0 VB=20.0 BR=2.144 C4=77.26 NC=1.098 IKR=7.356E-02

+ CJC=4.310E-11 MC=.4450 PC=.6050 CJE=7.230E-11 ME=.4450 PE=.9750
```

```
+ RC=1.946 RB=96.84 RE=6.000 TF=2.710E-09 TR=2.145E-07 )
ENDL
*
LIBRARY T2N2802
MODEL T2N2802 PNP( BF=189.5 C2=49.68 NE=1.479 IK=2.465E-02

+ IS=1.212E-15 VA=100.0 VB=20.0 BR=77.67 C4=14.79 NC=1.084 IKR=3.517E-02

+ CJC=2.310E-11 MC=.5000 PC=.7500 CJE=1.040E-11 ME=.5000 PE=.7500

+ RC=7.227 RB=1.000E-09 RE=3.100 TF=2.294E-09 TR=1.579E-07 )
ENDL
*
LIBRARY T2N2804
MODEL T2N2804 PNP( BF=186.8 C2=47.96 NE=1.484 IK=2.505E-02

+ IS=1.588E-15 VA=100.0 VB=20.0 BR=500.0 C4=22.08 NC=1.145 IKR=2.356E-02

+ CJC=2.310E-11 MC=.5000 PC=.7500 CJE=1.040E-11 ME=.5000 PE=.7500

+ RC=7.900 RB=1.000E-09 RE=3.100 TF=1.113E-09 TR=8.803E-08 )
ENDL
*
LIBRARY T2N2894
MODEL T2N2894 PNP( BF=166.8 C2=24.42 NE=1.460 IK=.2016

+ IS=1.510E-14 VA=100.0 VB=20.0 BR=142.0 C4=16.20 NC=1.145 IKR=.1482

+ CJC=4.410E-12 MC=.1760 PC=1.010 CJE=4.420E-12 ME=.3200 PE=1.080

+ RC=2.192 RB=31.50 RE=1.000E-06 TF=8.815E-10 TR=5.914E-09 )
ENDL
*
LIBRARY T2N2907
MODEL T2N2907 PNP( BF=502.7 C2=16.56 NE=1.437 IK=8.828E-02

+ IS=1.568E-14 VA=100.0 VB=20.0 BR=61.17 C4=73.39 NC=1.318 IKR=3.792E-02

+ CJC=2.350E-11 MC=.5000 PC=1.000 CJE=2.850E-11 ME=.4200 PE=1.000

+ RC=.3048 RB=1.000E-06 RE=.2000 TF=4.487E-10 TR=7.202E-08 )
ENDL
*
*
LIBRARY T2N3309
MODEL T2N3309 NPN( BF=233.3 C2=282.2 NE=1.473 IK=.4399

+ IS=1.448E-14 VA=100.0 VB=20.0 BR=6.964 C4=10.54 NC=1.174 IKR=7.594

+ CJC=1.600E-11 MC=.2500 PC=1.000 CJE=2.400E-11 ME=.3300 PE=1.000

+ RC=1.600 RB=2.705 RE=.1000 TF=2.198E-10 TR=2.202E-08 )
ENDL
*
LIBRARY T2N3866
MODEL T2N3866 NPN( BF=103.1 C2=7.101 NE=1.536 IK=.1686
```

```
+ IS=1.538E-12 VA=100.0 VB=20.0 BR=4.863 C4=100.1 NC=1.490 IKR=.1355

+ CJC=5.400E-12 MC=.3660 PC=1.000 CJE=7.230E-12 ME=.5200 PE=1.100

+ RC=8.282 RB=3.143 RE=.5000 TF=2.379E-10 TR=2.842E-08 )
ENDL
*
LIBRARY T2N3867
MODEL T2N3867 PNP( BF=193.5 C2=17.78 NE=1.376 IK=2.165

+ IS=5.752E-13 VA=100.0 VB=20.0 BR=8.389 C4=21.78 NC=1.247 IKR=.2139

+ CJC=1.930E-10 MC=.4450 PC=1.000 CJE=3.230E-10 ME=.4750 PE=1.000

+ RC=3.521E-02 RB=.4002 RE=.1400 TF=1.182E-09 TR=3.484E-08 )
ENDL
*
LIBRARY T2N3906
MODEL T2N3906 PNP( BF=267.8 C2=998.4 NE=2.057 IK=7.732E-02

+ IS=3.154E-15 VA=100.0 VB=20.0 BR=500.0 C4=112.8 NC=1.309 IKR=1.080E-02

+ CJC=4.720E-11 MC=.7000 PC=.2000 CJE=2.320E-11 ME=.2000 PE=.9000

+ RC=.2175 RB=2.843 RE=1.000E-06 TF=3.954E-08 TR=2.574E-08 )
ENDL
*
LIBRARY T2N5337
MODEL T2N5337 NPN( BF=287.6 C2=.6250 NE=1.289 IK=3.520

+ IS=2.722E-12 VA=100.0 VB=20.0 BR=66.39 C4=44.20 NC=1.345 IKR=.4473

+ CJC=3.440E-10 MC=.4800 PC=1.000 CJE=1.280E-09 ME=.4500 PE=1.000

+ RC=7.205E-03 RB=7.136E-02 RE=4.500E-02 TF=2.786E-09 TR=1.632E-07 )
ENDL
*
END
```

Appendix D

TEST FILES FOR THE TWO STAGE BUFFER CIRCUIT

```
* TWO STAGE BUFFER CIRCUIT

* PRECISE TEST FILE - MAY BE CONVERTED TO SPICE FORMAT

* CIRCUIT COMPONENTS AND NETLIST

RS1             5      3             3.91KOHMS

RS2             2      7             3.91KOHMS

RC1             1      2             464OHMS

RC2             1      6             464OHMS

VPOS            1      0             DC 5V

VIN             5      0      PULSE (0   5   500N   7.5N   7.5N   1U)

* DESCRIPTION                 V1  V2 TD     TR     TF     PW

Q1              2      3      0      T2N2222

Q2              6      7      0      T2N2222
```

```
* TRANSISTOR MODEL DESCRIPTION
MODEL T2N2222 NPN (BF=241  C2=3.16  NE=1.35  IK=0.35
+ IS=3.52E-14  VA=100  VB=100  BR=13.1  C4=60.6  NC=1.61
+ IKR=0.106  CJE=23.8PF  ME=0.43  PE=1.0  CJC=14.7PF  MC=0.42
+ PC=1.0  RE=0.26  RC=0.30  RB=2.1  TF=0.31NS  TR=89NS)
* OSCILLOSCOPE PROBE DATA
RPROBE       6     8          75.9OHMS
LPROBE       8     9          187NH
CPROBE       9     0          12.9PF
*SIMULATION DATA IN A SEPARATE FILE
*MAY BE COMBINED INTO A SINGLE FILE FOR SPICE USE
END
```

SIMULATION FILE FOR BUFFER CIRCUIT

```
SIM BUFF
SET VIN=0
DCSP * DC SINGLE POINT ANALYSIS
PRO N* V*  *PROBE ALL NODES AND VOLTAGES
PRO R* L* C*  *PROBE ALL PASSIVE COMPONENTS
PRO Q*   *PROBE ALL TRANSISTOR PARAMETERS
OPTIONS LIMPTS=10000
OPTIONS ITL5=25000
OPTIONS TNOM=27
OPTIONS NUMDGT=7
OPTIONS RELTOL=0.001
OPTIONS METHOD=GEAR
*OPTIONS COMMANDS FOR ITERATION SETTINGS
```

```
*MAY BE OMITTED IF CIRCUIT DOES NOT OSCILLATE
SWEEP VIN FROM 0 TO 5 BY 0.5
*V(5) IS VIN, V(6) IS VOUT
PLOT DC V(5) V(6) (*,*)
*(*,*) FOR AUTOMATIC CALIBRATION OF PLOT
GO
SWEEP TEMPDC FROM -55 TO 125 BY 5
PLOT V(5) V(6) (*,*)
* TO CHECK TEMPERATURE VARIATIONS
GO
* TRANSIENT ANALYSIS
SET VIN=0
ACSP
PRO Q*
SWEEP FREQ FROM 1 TO 100MHZ DEC 3
PLOT VM(3) VM(7)
GO
PLOT V(5) V(6)
GO
END BUFF
```

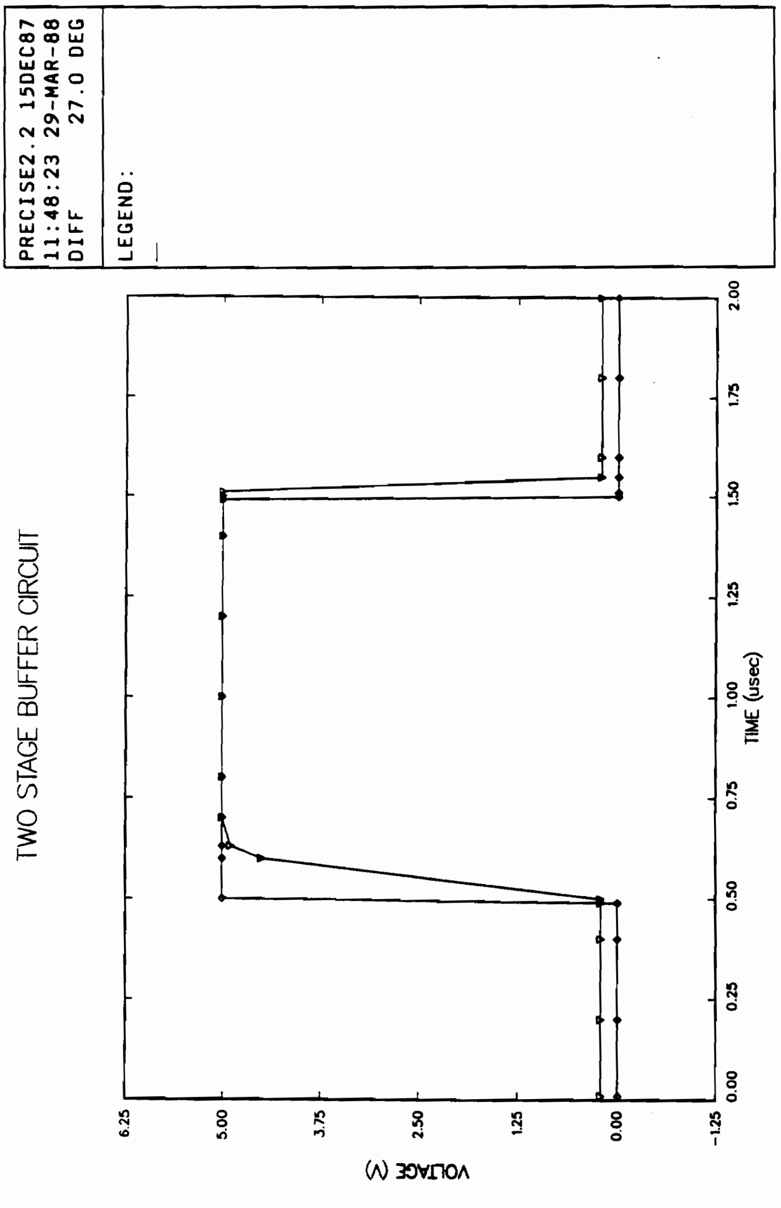

Figure 18. Response Time Plot.

Vita

Manoj M. Pansare was born on 8 December 1961 in Bombay, India. He received his Bachelor of Science degree in Electronics and Telecommunications Engineering from the College of Engineering in Poona, India in May 1985. He later joined Virginia Polytechnic Institute and State University in September 1985 to pursue a Master of Science Degree in Electrical Engineering. During his graduate program, Manoj worked as a cooperative education student for the Allied-Signal Aerospace Company, Computer-Aided Engineering Center as a Design Engineer. In July 1988, he completed his Masters Degree. Manoj will be returning to continue his professional interests at Allied-Signal Aerospace Company, Microelectronics and Computer-Aided Engineering Centers in Columbia, Maryland.

M. M. Pansare

Manoj M. Pansare

22 July 1988.