An Improved Electronic Ballast for the Fluorescent Lamps

by

Wei Chen

Thesis submitted to the Faculty of the

Virginia Polytechnic Institute and State University

in partial fulfillment of the degree of

MASTERS OF SCIENCE

IN

ELECTRICAL ENGINEERING

APPROVED:

Fred C. Lee

Fred C. Lee

Borojevic

Dusan Borojevic

Guichao Hua

Guichao Hua

August, 1995

Blacksburg, Virginia

.2

AN IMPROVED ELECTRONIC BALLAST FOR THE FLUORESCENT LAMPS

by

Wei Chen

Committee Chairman: Dr. Fred C. Lee

Electrical Engineering

ABSTRACT

The "charge pump" electronic ballast circuit, which employs a charging capacitor and a high frequency ac source to implement the power factor correction (PFC), has become an attractive topology for ballasting the fluorescent lamps because it eliminates the use of a bulky boost inductor. But the high voltage stress on the semiconductor devices at light load conditions, the high total harmonic distortion (THD) of the line current, and the poor crest factor (CF) of the lamp current in this circuit make it difficult to manufacture this circuit into a cost-effective ballast product. This thesis analyzes the problems associated with the "charge pump" electronic ballast, and proposes several innovative methods to solve the problems, resulting in a high performance and cost-effective technology.

Acknowledgment

I would like to express my most sincere gratitude to my advisor, Dr. Fred C. Lee, for his constant support and invaluable instructions during the course of this work. His encouragement and patience have been the source of the help throughout my graduate studies.

I wish to express my deep thanks to Dr. Guichao Hua for his valuable suggestion regarding this work, and for his tremendous help during my two-year stay at Virginia Power Electronics Center (VPEC). I want to thank Dr. Dusan Borojevic for serving as my committee member. I would also like to express my gratitude to Dr. Dan Y. Chen for providing me the valuable course, power semiconductor devices and magnetic components, and for his suggestion at the beginning of this work.

I would like to express my sincere appreciation to Mr. Tokushi Yamauchi of Matsushita Electric Works, Ltd., Boston R & D Lab, for his selfishless support and valuable discussions during the period of this work. I also wish to thank Mr. Jinrong Qian for his suggestion and help on this work.

Thanks are also extended to Dr. Juan A. Sabate and Dr. Milan M. Jovanovic, for their guidance during my early days at VPEC. Special thanks are due to Mr. Robert Watson. Without his help, I will not be able to finish this work so smoothly.

It has been a pleasure staying at VPEC. I would like to thank VPEC staffs, Teresa Shaw, Tammy Hinner and Bill Cockey for making my stay such an enjoyable experience. I also appreciate the friendship from my fellow VPEC students, Kunrong Wang, Ju Zhang, Ping Han, Ning Dai, Michael Zhang, Chih Yi Lin, Hengchun Mao, Qiong Li, Richard Zhang, Qihong Huang, Dongbing Zhang, Wilson Zhou, Kun Xing, Glenn Skutt, Goran Stojcic, Silva Hiti, Musiri Shrivathan, Ravindra Ambatipudi, Jayenda Rajagopalan, Liliana Grajales, and other people whose names are too many to mention here.

I am deeply indebted to my late father, my mother and my elder sister for their unfailing confidence in me and their sacrifices for my education. The completion of my Masters of Science degree is dedicated to my late father as a fulfillment of his last wish.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

Chapter 1 Introduction

As the industry demand for the high frequency electronic ballast has grown rapidly in recent years, a number of innovative topologies have emerged. Among them, the "charge pump" electronic ballasts have gained popularity for the discharge lamp due to their simplicity and low cost [1-8].

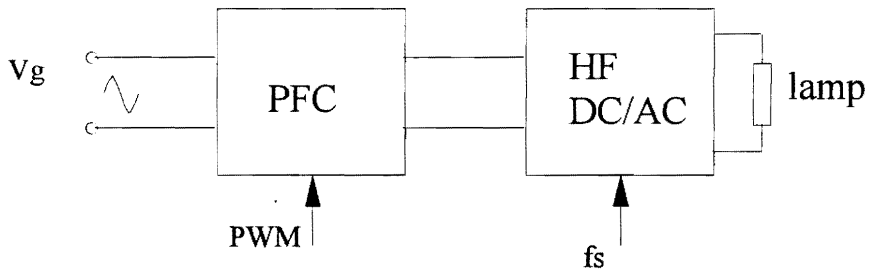


Fig. 1.1 Conventional two-stage configuration for electronic ballast

Since the electronic ballast is an ac/ac power processor, which converts the line frequency ac power into high frequency ac power to light the lamp, the ballast circuit consists of two stages: ac/dc rectification with PFC and dc/ac inversion (as shown in Fig. 1). Figure 1.2 shows an example of the conventional electronic ballast: a PFC boost converter followed by a parallel resonant inverter. Since there are two controls available in this circuit, the good performance, such as good unity power factor, low crest factor of the lamp current[1], and good dimming of the light, etc., can be easily obtained. However, the two-stage approach requires two sets of power stages and control circuits. The cost of this electronic ballast is high.

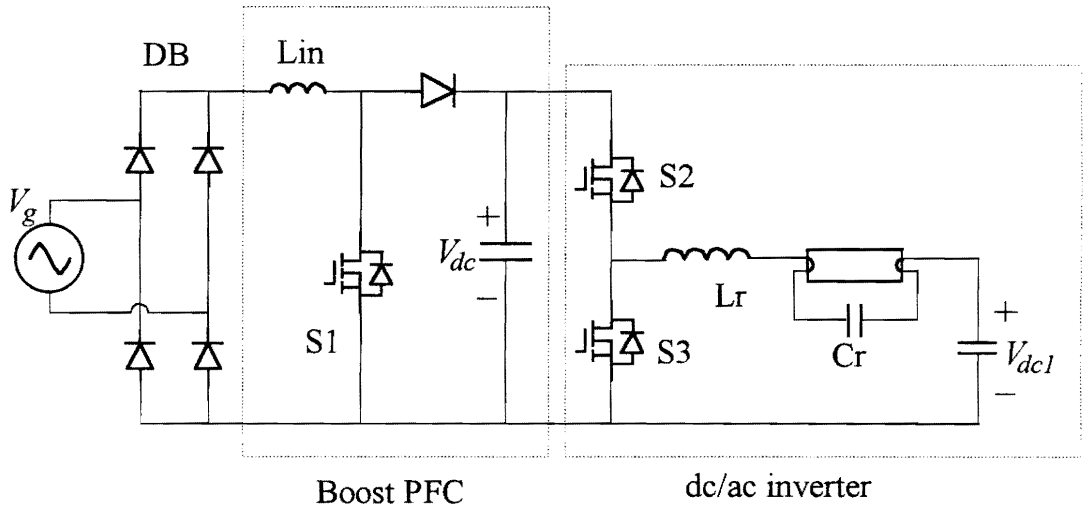
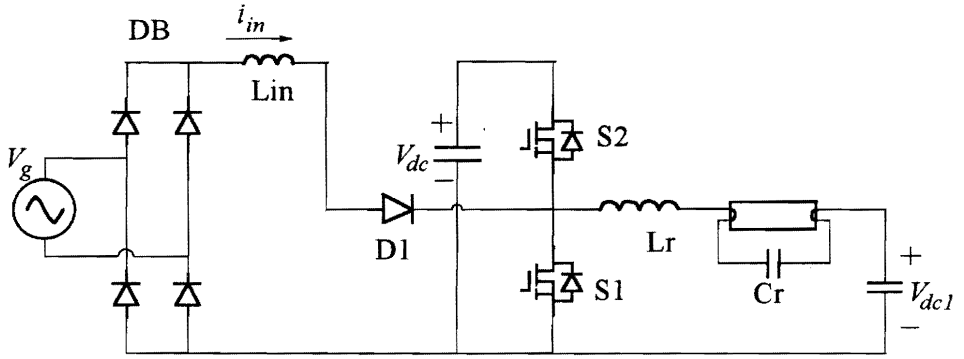


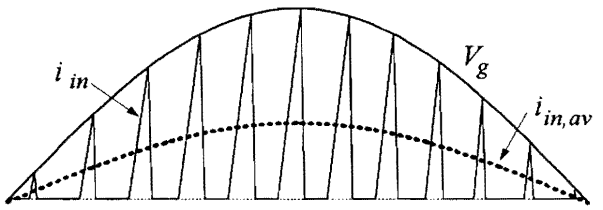
Fig. 1.2 An example of two-stage electronic ballast

[1] The crest factor of the lamp current is defined as: $CF = I_{la,pk} / I_{la,rms}$. The peak value $I_{la,pk}$ and the rms value $I_{la,rms}$ of the lamp current are measured on the basis of one line cycle.

If we operate the boost converter into the discontinuous current mode (DCM), some extent of PFC is naturally obtained [9-10]. Therefore, two stages can be integrated into one stage. One example [1] is shown in Fig. 1.3. Two switches in this circuit are complementarily switched to drive the resonant inverter tank. At the same time, the lower switch implements the boost switch function, and the anti-parallel diode of the upper switch functions as the diode in the boost converter. The fast diode in series with the boost inductor ensures the DCM operation of the boost inductor. In this topology, the ripple across the dc bus is usually very small. So the crest factor of the lamp current can be low. Duty cycle control or frequency control can be adopted. With duty cycle control,



(a)



(b)

Fig. 1.3 Boost integrated electronic ballast [1]:

(a) circuit diagram, (b) typical waveforms

the resonant tank current is sensed in order to turn on the MOSFET switch only when its body diode conducts. Otherwise, the reverse recovery current of the body diode may kill the MOSFET device. Under frequency control, the dc bus voltage can increase significantly at light load operating conditions [10]. An additional protection circuit is needed to prevent the switches from suffering the overvoltage. The lower switch on the totem pole in this circuit usually has a much larger current stress than the upper switch, because it has to take the sum of the boost inductor current and the resonant inverter tank current. Consequently, the size of the lower switch is larger than that of the upper switch. In order to reduce the THD of the input current, the dc bus voltage should be high enough. The voltage stress of the semiconductor devices can be high.

Another type of electronic ballast circuit, employing a charging capacitor and the high frequency ac source (either voltage source or current source) to implement PFC, was proposed recently [1-8] This type of ballast circuit is sometimes called "charge pump" circuit. Figure 1.4 describes the principle diagram which employs the charging capacitor Cin and the high frequency ac *voltage* source (HFVS). By designing the dc bus voltage, V_{dc}, higher than the input line voltage, V_g, the diodes Dc and DB will not conduct at the same time. Then the input current equals the positive charging current of Cin (the current direction shown in Fig. 1.4.a), which is regulated by V_a, V_g and V_{dc}. If the charge variation of Cin (which is proportional to the variation of V_c, as shown in Fig. 1.4.b) follows the input voltage, the input average current will follow the input voltage. The good input power factor can be obtained.

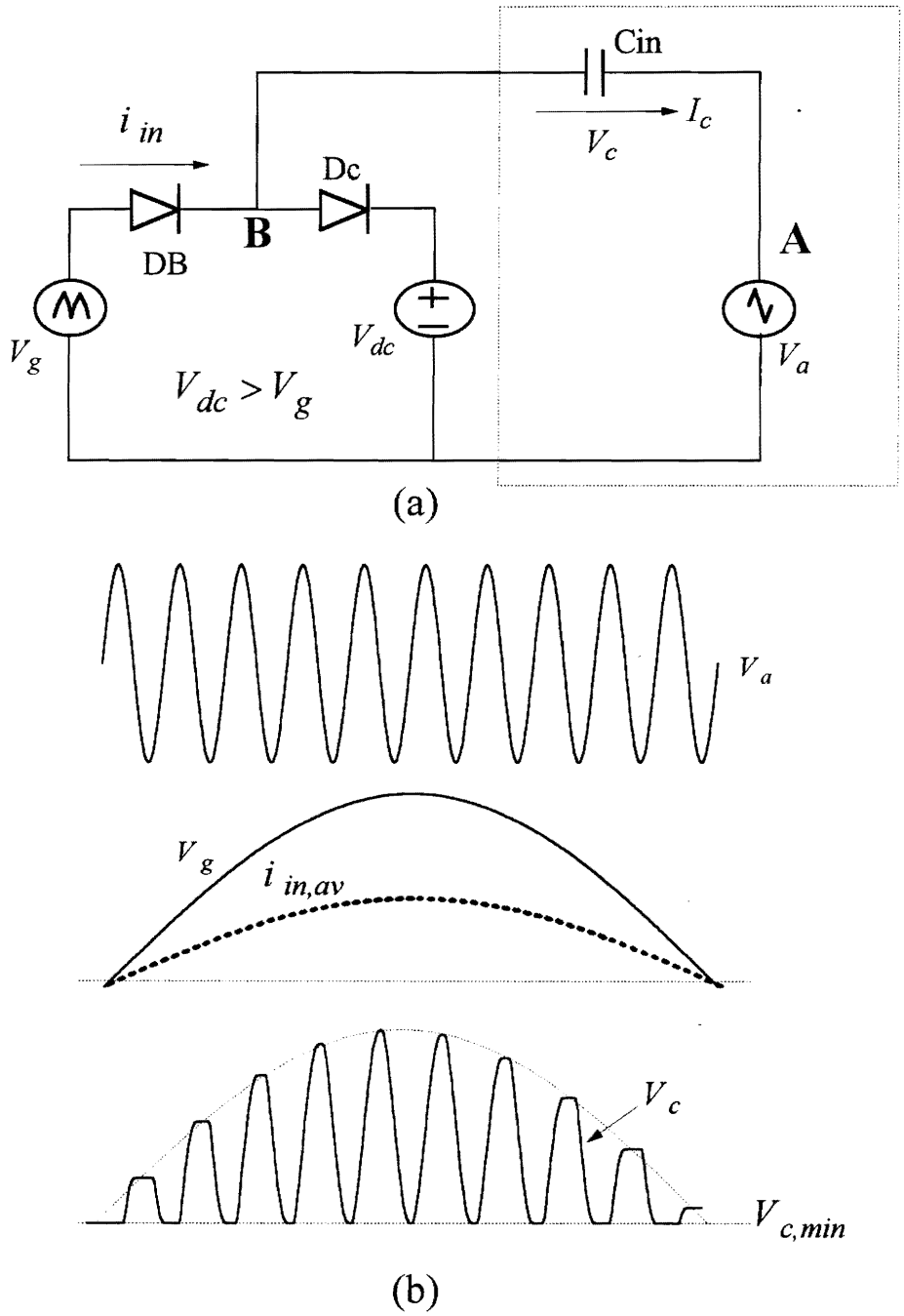


Fig. 1.4 "Charge pump" circuit employing HFVS:

(a) principle schematics (b) typical waveforms

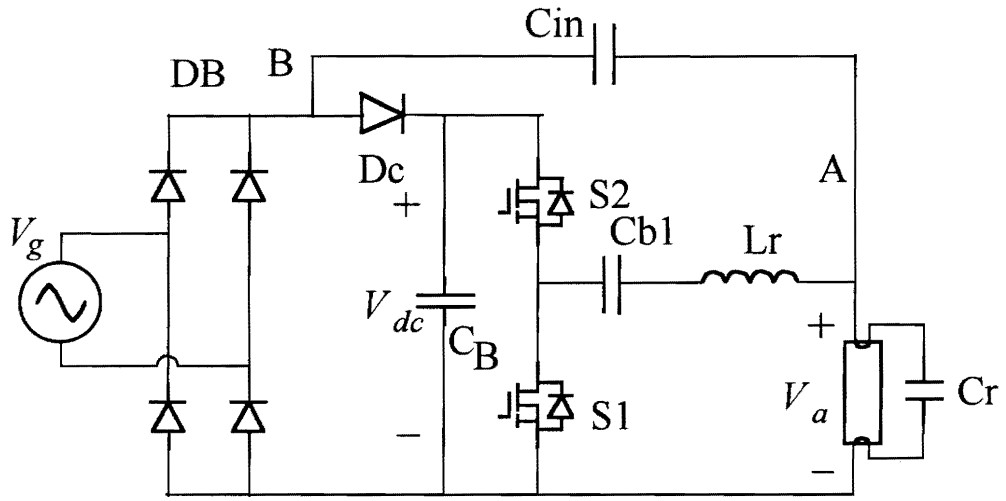


Fig. 1.5 An example of "charge pump" ballast employing HFVS

One example of the "charge pump" circuit is shown in Fig. 1.5. Compared to the boost integrated circuit shown in Fig. 1.3, this circuit replaces the boost inductor by a charging capacitor. It should be noted that the current stresses of two switches in this circuit are the same. Therefore, this type of circuit is potentially low-cost. However, the switches still suffer high voltage stress under light load conditions. Furthermore, due to the injection of the line ripple through Cin, the crest factor of the lamp current and the THD of the line current can be high.

In this thesis, the operation principles and the existing problems of the "charge pump" circuit employing HFVS (shown in Fig. 1.5) are analyzed (Ch.2). A class of novel methods of reducing the dc bus voltage at light loads are proposed (Ch. 3). The approach to improving the normal operation performances including the input power factor, the THD

of the input current and the crest factor of the lamp current is developed. Finally, the conclusions are drawn (Ch. 5).

Chapter 2 Analysis of "charge pump" electronic ballast

Figure 2.1 shows the "charge pump" electronic ballast for the fluorescent lamp. This is the basic topology in this thesis. The isolation transformer serves two purposes: providing the required lamp voltage and preheating the lamp filaments.

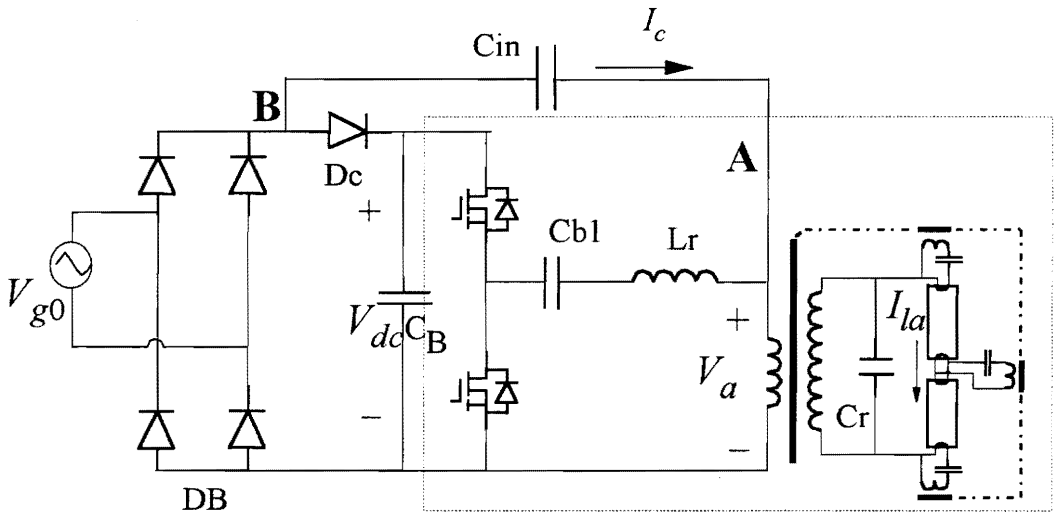


Fig. 2.1 Basic electronic ballast circuit for the fluorescent lamp

The circuit can be separated into two parts: PFC and dc/ac inversion. The equivalent circuit is shown in Fig. 2.2: DB stands for the rectifier diodes, V_g is the rectified input voltage. Through proper design, the lamp voltage amplitude can be roughly constant during the line cycle. Consequently, V_a is regarded as a constant amplitude high frequency ac source. In order to regulate the input current, Dc and DB should not be on at the same time. This implies that V_{dc}, the dc bus voltage, should be always higher than the line voltage. So it is requested that V_{dc} be larger than the line peak voltage, V_{gp}. Since the line

frequency is usually much lower than the switching frequency, the line voltage V_g is regarded to be constant in one switching cycle.

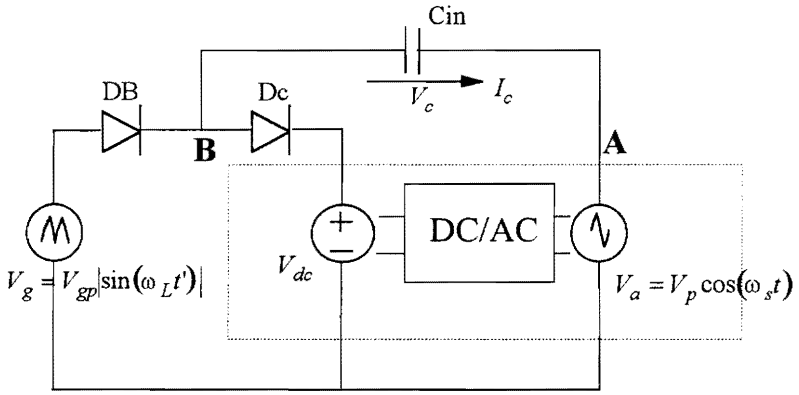


Fig. 2.2 The equivalent circuit consists of two parts:
(1) PFC, (2)dc/ac inverter

2.1 Principle of power factor correction (PFC)

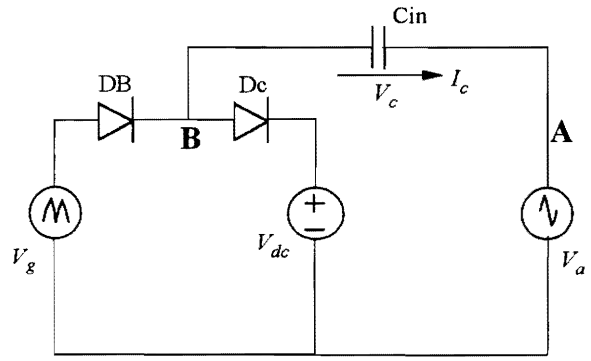


Fig. 2.3 The equivalent circuit of PFC

To facilitate the understanding of the PFC principle in a "charge pump" circuit, the equivalent circuit for PFC is introduced as shown in Fig. 2.3: V_a is treated as the independent high frequency ac source, V_{dc} and V_g are regarded as constant dc voltage

source in one switching cycle. Four power stages in one switching period are shown in Fig. 2.4, and the waveforms in Fig. 2.5. Based on the assumption of zero on-voltage-drop of diodes and switches, the operation in one switching cycle is analyzed as follows.

2.1.A Steady state operation

Stage 1 [0, α] : shown in Fig. 2.4 (a)

During this stage, since the voltage at node B, V_b, is lower than V_{dc}, and higher than V_g, both Dc and DB are off. So there is no current flowing through the input capacitor, Cin. As a result, V_c, the voltage across Cin, is unchanged. V_a keeps decreasing, pulling down V_b. This stage ends at $\varpi t=\alpha$, when V_b becomes equal to V_g.

Stage 2 [α, π] : shown in Fig. 2.4 (b)

DB starts to conduct at $\varpi t=\alpha$. V_b is clamped to V_g. To make V_b constant, V_c has to increase when V_a continues decreasing. Cin is thus charged by the rectified line current. At $\varpi t=\pi$, V_a decreases to the negative peak value, and V_c reaches its maximum point:

$$V_{c,\max} = V_p + V_g, \tag{2.1}$$

where V_p is the ac amplitude of V_a.

Stage 3 [π, π+β] : shown in Fig. 2.4 (c)

After $\varpi t=\pi$, V_a increases from its negative peak value, $-V_p$. V_b becomes higher than V_g, forcing DB to be reversely biased. Since V_b is lower than V_{dc}, Dc still blocks. Similar to Stage I, there is no current flowing through the input capacitor, Cin. V_c remains unchanged. V_a keeps increasing, boosting V_b up. This stage ends at $\varpi t=\pi+\beta$.

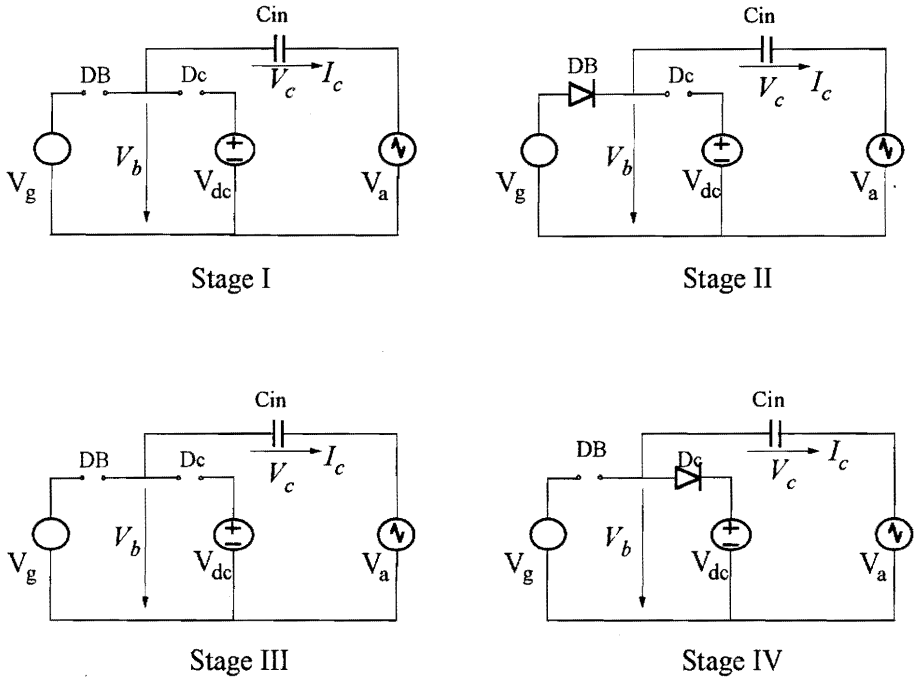


Fig. 2.4 Four power stages of PFC circuit

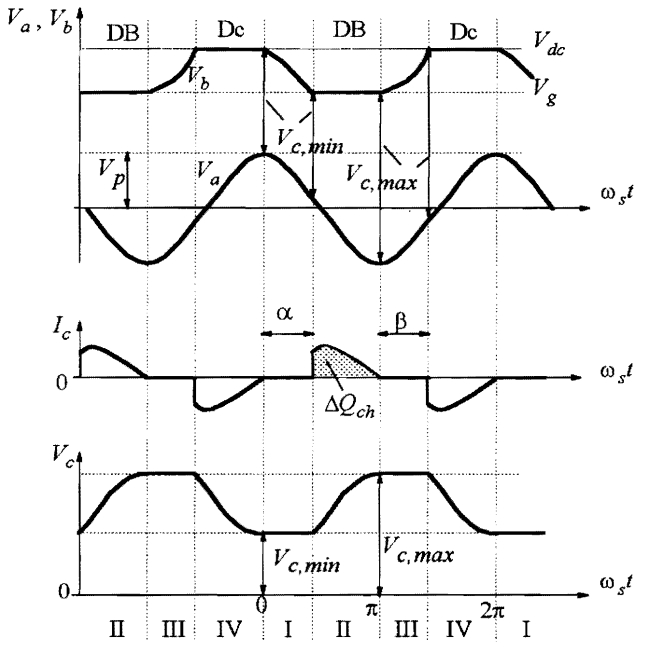


Fig. 2.5 Theoretical waveforms of four power stages

Stage 4 [π+β, 2π] : shown in Fig. 2.4 (d)

At ϖt=π+β, V_b becomes equal to V_{dc}. Dc starts to conduct. To keep V_b equal to V_{dc}, V_c has to decrease when V_a continues increasing. The discharging current of Cin flows into V_{dc}. At ϖt=2π, V_a increases to its positive peak value, and V_c reaches its minimum point:

$$V_{c,\min} = V_{dc} - V_p. \tag{2.2}$$

After ϖt=2π, the circuit operation enters Stage I again. The next switching cycle will be repeated.

2.1.B Condition for unity input power factor

From the above analysis, we can see that the line current only flows in during Stage II. Therefore, the input current in this circuit is discontinuous and is regulated by the charging and discharging of the capacitor Cin. A more detailed analysis of the charge variation of Cin reveals the operation condition for the unity input power factor.

During the charging stage, the charge variation of Cin is

$$\Delta Q_{ch} = C_{in}(V_{c,\max} - V_{c,\min}). \tag{2.3}$$

By substituting Eqs. (2.1) and (2.2) into Eq. (2.3), we can obtain

$$\Delta Q_{ch} = C_{in}(V_g + 2V_p - V_{dc}). \tag{2.4}$$

Since the rectifier diodes conduct only in the charging stage (Stage 2) over the whole switching cycle, the average input current in one switching cycle equals the average charging current of Cin, which is

$$i_{in,av} = I_{ch} = f_s \cdot \Delta Q_{ch} \tag{2.5}$$

or

$$i_{in,av} = f_s C_{in}(V_g + 2V_p - V_{dc}). \tag{2.6}$$

For a good power factor, we expect the input current to follow the input voltage, i.e.,

$$i_{in,av} \propto V_g. \tag{2.7}$$

If we design

$$V_{dc} = 2V_p, \tag{2.8}$$

we have

$$i_{in,av} = f_s C_{in} V_g \propto V_g. \tag{2.9}$$

This implies that the circuit has a good power factor if Eq. (2.8) is satisfied. Here, we assume that V_a is sinusoidal waveform. In fact, V_a can be any kind of waveform with a constant ac amplitude. As long as the ac peak-to-peak value of V_a equals V_{dc}, the good power factor will be guaranteed.

From Eq. (2.6), we can also see that V_p , the peak value of V_a, should be no smaller than half of V_{dc} in order to avoid line current distortion at zero-crossing of line voltage. If V_p is smaller than half of V_{dc}, the line current will become zero when $V_g \leq | V_{dc} - 2V_p |$.

2.1.C Input power estimation

Under the assumption of well designed input filter, $V_{dc} \geq V_{gp}$, and constant V_p with $V_p \geq V_{dc}/2$, we can derive the expression for the input power flowing through Cin, P_{in}.

As we have

$$V_g = V_{gp}|\sin(\omega_L t)| \tag{2.10}$$

and

$$P_{in} = \frac{2}{T_L}\int_0^{T_L/2} V_g i_{in,av} dt\,, \tag{2.11}$$

by substituting Eqs. (2.6) and (2.10) into Eq. (2.11), we obtain

$$P_{in} = \tfrac{1}{2} f_s C_{in}\left[V_{gp}^2 + \tfrac{4}{\pi}\left(2V_p - V_{dc}\right)V_{gp}\right]. \tag{2.12}$$

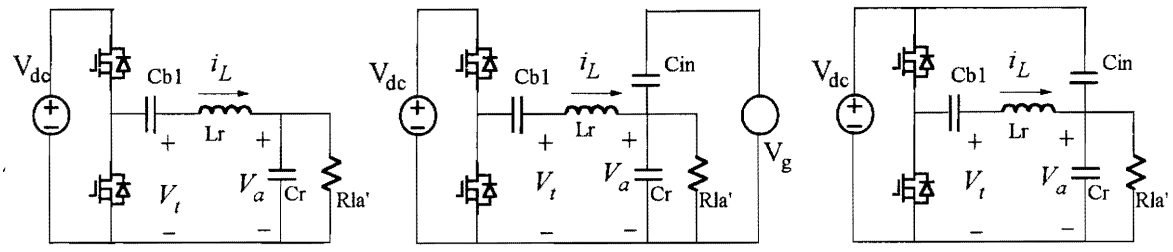
Under the condition PF=1, we have $V_{dc} = 2V_p$. Then Eq. (2.12) becomes

$$P_{in} = \tfrac{1}{2} f_s C_{in} V_{gp}^2\,. \tag{2.13}$$

Equation (2.13) is useful in the circuit design. If the line voltage, the input power, and the switching frequency are given, Cin can be chosen accordingly.

2.2 Analysis of inverter operation

The inverter is basically an LC parallel resonant circuit. Since the input capacitor, Cin, is switched into the resonant tank during Power Stages (II) and (IV) and is switched off in Power Stages (1) and (III), the voltage across the lamp, V_a, can vary very much in half line cycle.



(a) Stages I & III (b) Stage II (c) Stage IV

Fig. 2.6 Topological stages of resonant inverter

The inverter topologies of different power stages are shown in Fig. 2.6. The waveform is shown in Fig. 2.7. In each switching cycle, Cin is switched into the resonant tank for the angle interval, $2(\pi-\alpha)$, which is determined by the line voltage. When the line voltage is low, this angle is small; if the line voltage is high, the angle is large. Moreover, as shown in Fig. 2.6(b), V_g is connected to the resonant inverter during Power Stage (II). Therefore, V_a is affected by the line voltage.

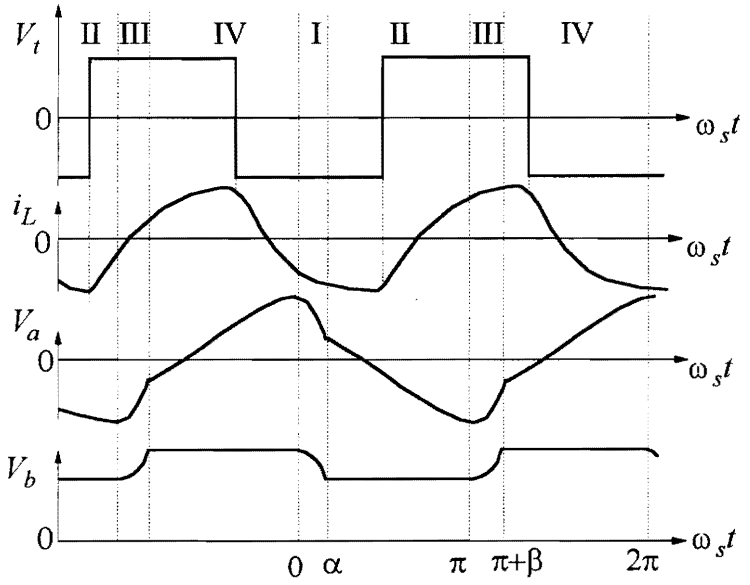


Fig. 2.7 Theoretical waveform of the resonant tank

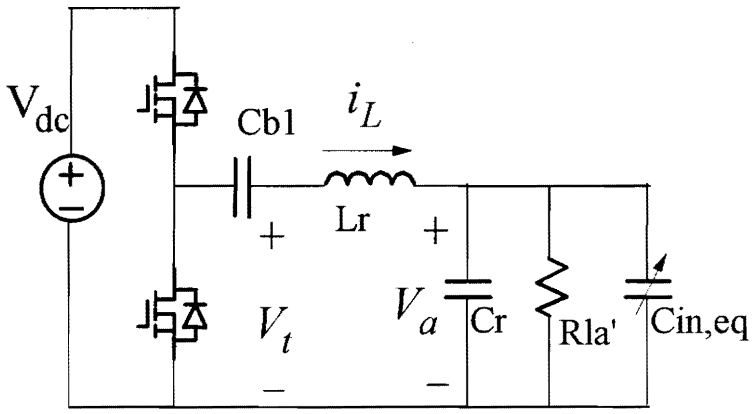


Fig. 2.8 The equivalent circuit of the inverter

The approximate equivalent circuit of the resonant inverter is shown in Fig. 2.8. The equivalent capacitance of Cin appears to in parallel with Cr, and its value is a function of the line voltage. No strict mathematical expression is available. But generally speaking, $C_{in,eq}$ is large when the line voltage is high, and small when the line voltage is low. $C_{in,eq}$ reaches its maximum value, Cin, when the line voltage is the highest. Consequently, the approximate inverter voltage conversion gain curves under different line voltages are obtained as shown in Fig. 2.9. It is noted that when the line voltage is low, the resonant peak is at high frequency. So the circuit may run into the capacitive mode (like Curve A shown in Fig. 2.9.b), especially at light loads, resulting in the loss of zero-voltage-switching (ZVS) of the semiconductor switches. Due to the reverse recovery of the body diode of the MOSFET, the turn-on power loss of the switches can be substantially high. This should be taken care of during the design.

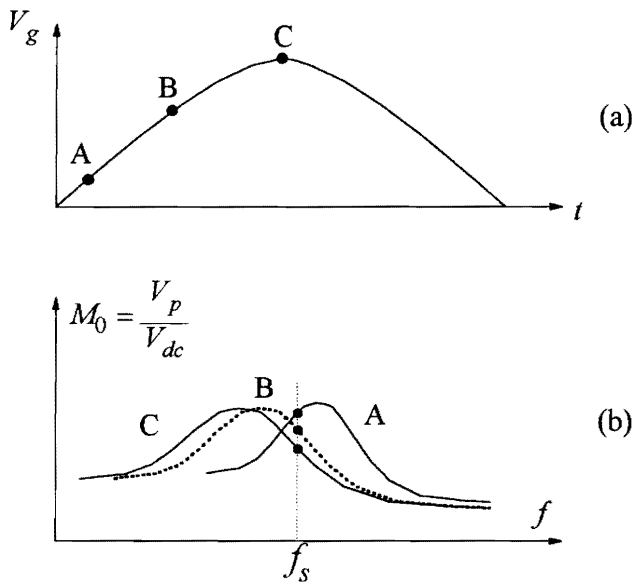


Fig. 2.9 The voltage conversion gains under different line voltages

2.3 Design issues

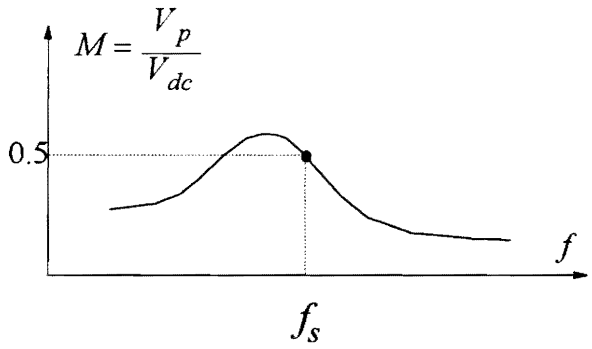


Fig. 2.10 The approximate voltage gain of the inverter

In practice, if we manage to group the inverter gain curves in Fig. 2.9(b) close enough, we may be able to obtain an approximate voltage gain curve of the inverter (shown in Fig. 2.10). To achieve the unity input power factor, the voltage gain, $M=V_p/V_{dc}$, should equal

0.5. No strict design guideline for the resonant tank is available. But the following design procedure is preferred:

i) given P_{out}, f_s, V_{gp}, and efficiency specification η, C_{in} is at first chosen according to Eq. (2.14):

$$C_{in} = \frac{2P_{out}}{\eta \cdot f_s \cdot V_{gp}^2}; \tag{2.14}$$

ii) given the output voltage peak value, $V_{la,pk}$, the transformer primary to secondary turns ratio is estimated as

$$N = \frac{V_p}{V_{la,pk}} = \frac{V_{dc}}{2 \cdot V_{la,pk}}, \tag{2.15}$$

where V_{dc} is usually chosen slightly higher than V_{gp};

iii) finally, based on the simulations or the experiments, Lr and Cr are chosen to yield M=0.5 and $V_p \cong$constant.

2.4 Limitations of the "charge pump" electronic ballast circuit

There are several limitations in this circuit: high THD of the input current, high crest factor of the lamp current, and high dc bus voltage at light load operations.

2.4.A Reason for high THD and high crest factor

From Fig. 2.9(b), we can predict that V_p is variable over half line cycle. The direct penalty of this variation is the poor crest factor of the lamp current. Since the variation of V_{dc} is negligible, Eq. (2.8) cannot be always satisfied during the half line cycle. From Eq. (2.6),

we can see that the input current will not follow the input line voltage. The input power factor is degraded, and the THD of the line current increases.

As shown in Fig. 2.7, the lamp current waveform consists of two distinct parts. The wave shape of the lamp current is not purely sinusoidal. This is another reason for poor crest factor of the lamp current.

2.4.B Reason for high dc bus voltage (V_{dc}) at light load conditions

The way to understand this problem is to examine Eq. (2.12) closely. We can see from this equation that the higher f_s, Cin, or V_p, the higher the input power flowing through Cin; the higher the V_{dc}, the lower the input power flowing through Cin. At the steady state operation, the input power flowing through Cin equals the output power if $V_{dc}>V_{gp}$ is satisfied. At the light loads, the output power reduces, the parameters on the right hand side of Eq. (2.12) have to change to make both sides of Eq. (2.12) equal.

Usually, the operation of the electronic ballast for the fluorescent lamp includes three operation modes: preheat, start-up and normal lighting. The approximate voltage conversion gains of the inverter tank under different load conditions are shown in Fig. 2.11.

At the preheat mode of the lamp operation, the lamp voltage should be much smaller than the starting voltage. Because the lamp is not turned on, the circuit is operating under the light load conditions. The switching frequency for the preheat mode has to be much higher than that for the normal lighting. If the lamp voltage at the preheat mode is not low

enough, V_{dc} at light load has to increase in order to satisfy Eq. (2.12). This can be expressed as:

$$P_{in}\downarrow \text{ and } f_s\uparrow \Rightarrow V_{dc}\uparrow.$$

At the start-up mode operation, the lamp voltage is much higher than that at the normal lighting. Usually, the switching frequency at the start-up mode is very close to that at the normal lighting in order to obtain the sufficiently high ignition voltage. However, the output power at start-up mode is still much lower than that at normal lighting because the lamp is not ignited. According to Eq. (2.12), in order to decrease the input power to match the low output power, V_{dc} at start-up mode has to increase dramatically compared to that at normal lighting. This can be expressed as:

$$P_{in}\downarrow \text{ and } V_p\uparrow \Rightarrow V_{dc}\uparrow.$$

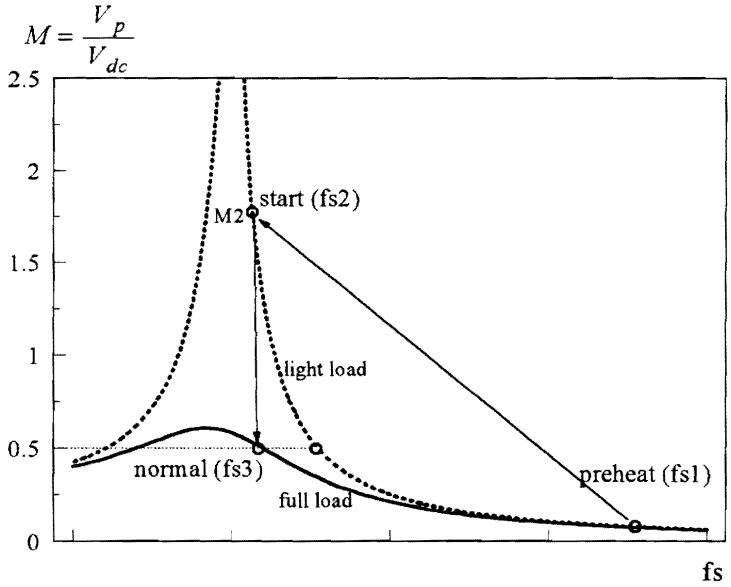


Fig. 2.11 The voltage conversion gain of the inverter under different loads

Chapter 3 Approaches to reducing dc bus voltage at light load conditions

Light load conditions in a "charge pump" electronic ballast always cause high dc bus voltage (V_{dc}) according to the analysis in Ch. 2. This chapter provides general principles of reducing V_{dc} at light loads. The proposed solutions of reducing V_{dc} for the fluorescent lamp ballast are addressed in this chapter. Experimental results are also provided for the verifications.

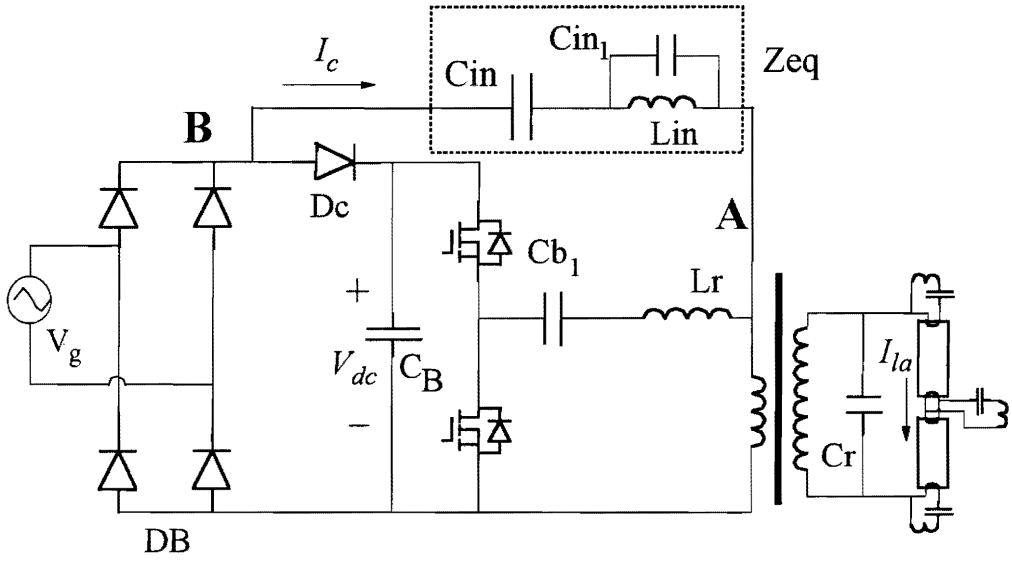
3.1 General principle of reducing dc bus voltage at light loads

The solutions of reducing V_{dc} can be found from Eq. (2.12): if we are able to decrease the equivalent Cin or V_p (ac amplitude of V_a) at light loads, V_{dc} can be reduced. The original resonant tank can be regarded as a first stage resonance. To obtain a decreased Cin or/and V_p at light loads, a second-stage resonance is introduced. The basic idea is to operate the circuit in different resonance domains to obtain different V_p or equivalent Cin under the different load conditions.

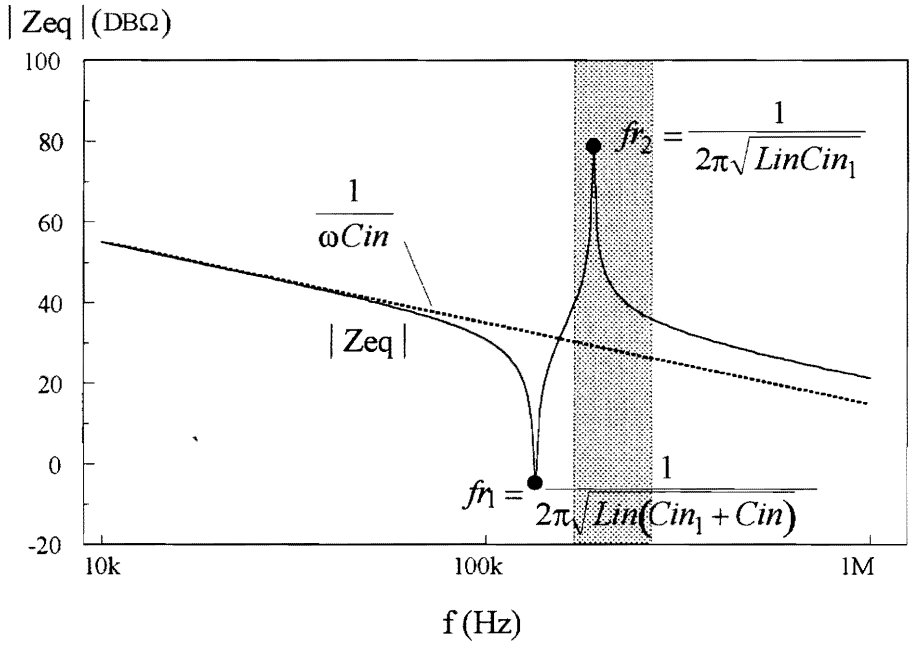
3.1.A) Reducing V_{dc} at light loads by decreasing Cin

There are several ways to modulate the equivalent capacitance of Cin. Figure 3.1 shows one example by introducing a second-stage resonance in the Cin branch. At fr_2, Lin

resonates with Cin_1, introducing an extremely high impedance. As a result, the equivalent capacitance of the Cin branch is reduced.

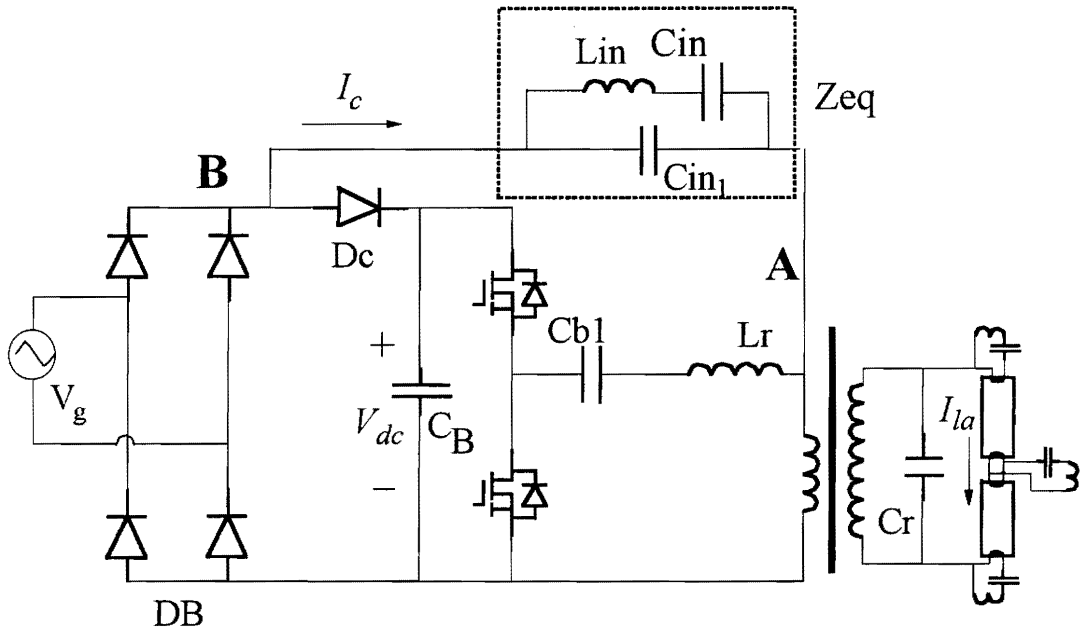


(a)

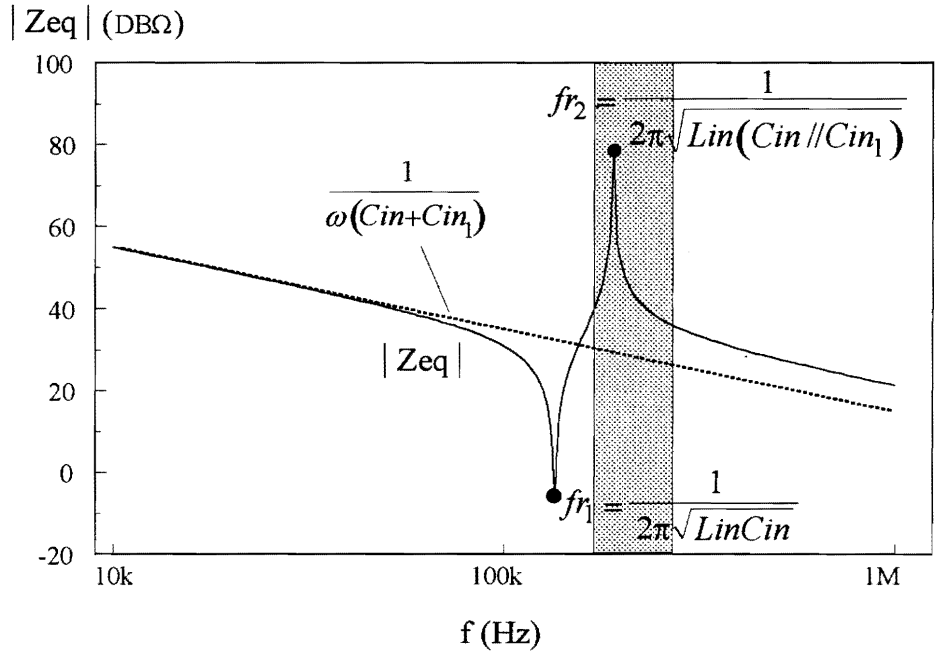


(b)

Fig. 3.1 One example of changing C_{in} by using a parallel resonant tank
(a) schematic diagram, (b) the equivalent impedance



(a)



(b)

Fig. 3.2 Second example of changing C_{in} by using a resonant tank

If we set the light load operating frequency around fr_2, we can limit the input current flowing through Cin (according to Eq. 2.6), and the input power is reduced automatically. Accordingly, V_{dc} can be low. The practical light load frequency is set inside the shaded area shown in Fig. 3.1(b). Since Z_{eq}, the equivalent impedance of the Cin branch, is infinitely large at fr_2, it has little effect on the inverter resonant tank. Therefore, the resonant peak of the inverter tank can be determined from Lr and Cr directly. The high lamp voltage for the light loads (e.g. lamp preheat, start-up, etc.) can be easily obtained.

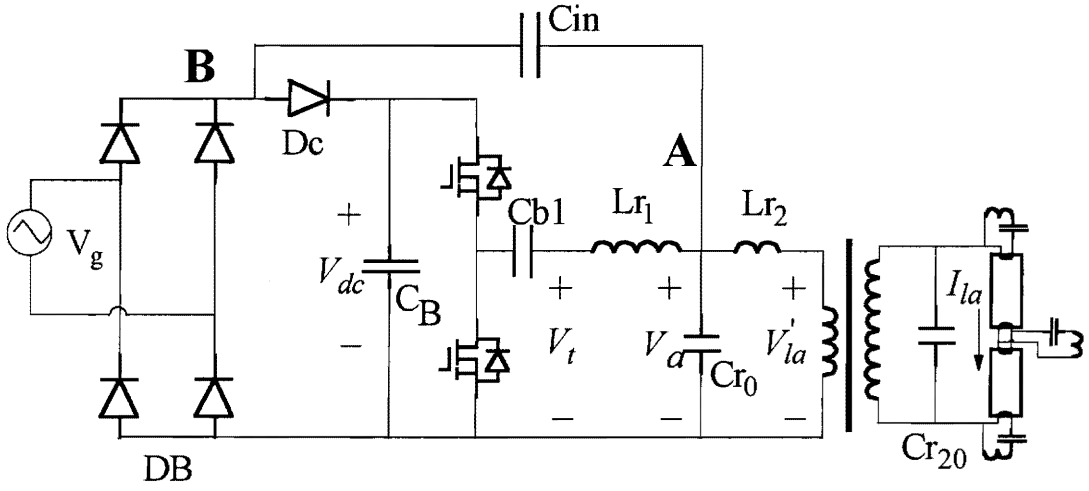
Figure 3.2 shows another example of modulating Cin at light load frequency. The principle is similar to that shown in Fig. 3.1.

3.1.B) Reducing V_{dc} at light loads by decreasing V_p

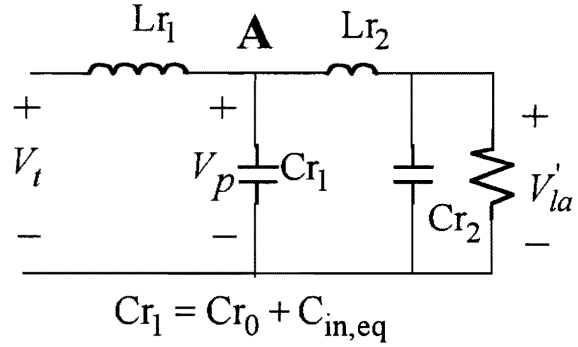
As predicted by Eq. (2.12), the input power flowing through C_{in} can be reduced if V_p is reduced. Consequently, V_{dc} at light loads can be reduced. However, the lamp voltage at light load is usually higher than that at full load. To reconcile these two contradictory requirements, an inductor Lr_2 has to be inserted between Terminal A and the transformer primary side (Fig. 3.3.a).

Figure 3.3 (b) shows the approximate ac equivalent circuit for the inverter tank: Cr_1 is the equivalent capacitance across point A; Cr_2 and R_{la}' are the reflected Cr_{20} and the lamp resistance respectively. The normalized voltages V_p and V_{la}' (the transformer primary voltage) at light load and full load are plotted in Fig. 3.4 (the reference for the normalization is V_t).

Under light load conditions, Lr_2 resonates with Cr_2 at fr_2. V_p, the ac amplitude of V_a, can be close to zero (as shown in Fig. 3.4.a). The input power flowing through Cin is reduced greatly. Therefore, the dc bus voltage at light loads can be low. The primary voltage V_{la}' can still be relatively large due to the resonance between Lr_2 and Cr_2 (as shown in Fig. 3.5) compared to V_p.



(a)



(b)

Fig. 3.3 Reducing V_p at light loads:
(a) circuit diagram, (b) approximate ac equivalent circuit for inverter tank

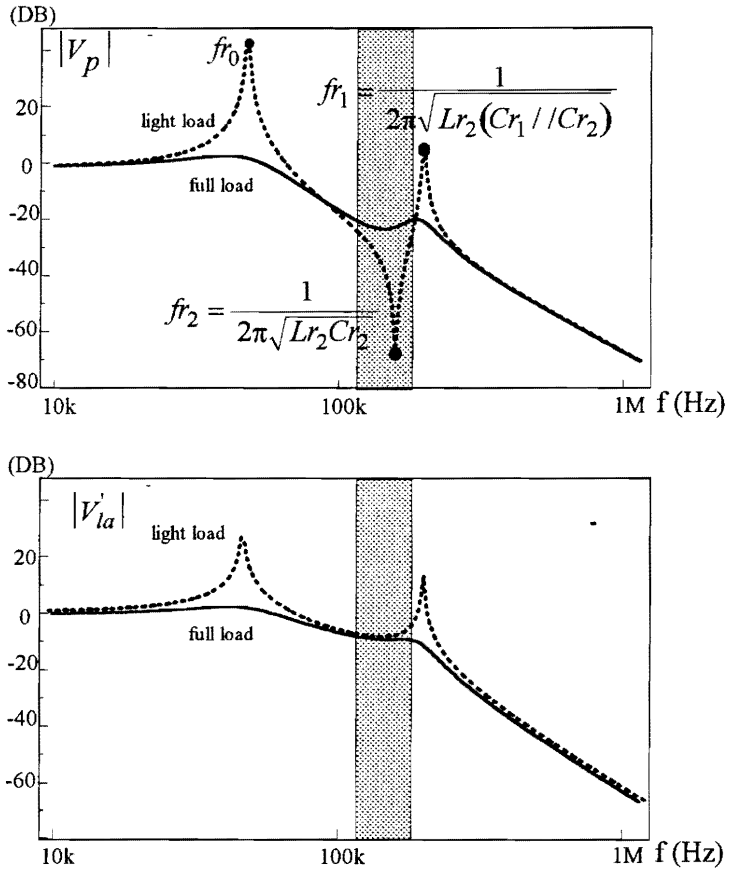


Fig. 3.4 Bode plots of normalized V_p and V_{la}' at light load and full load

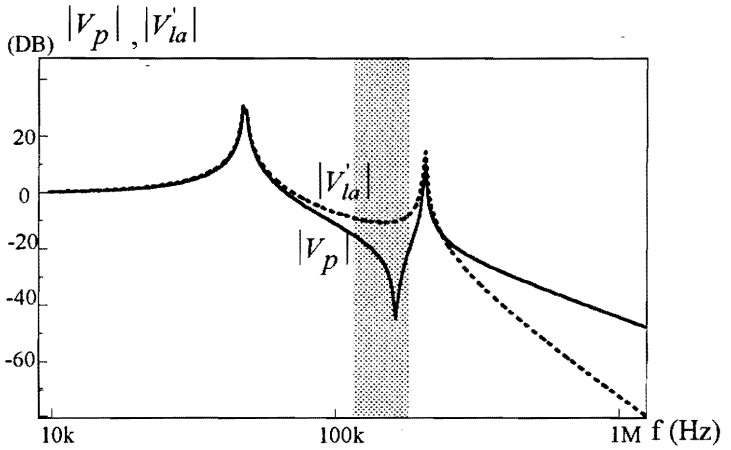


Fig. 3.5 Comparisons of V_p and V_{la}' at light load

Combining Methods 3.1.a and 3.1.b is also feasible. Two additional inductors (Lin and Lr_2) introducing the second-stage resonance can be coupled into one. However, the design becomes complicated.

3.2 Design strategies of reducing V_{dc} at light loads in the fluorescent lamp ballast

3.2.A) Strategy I: high frequency second-stage resonance (HFSR) technique with instant start-up

The basic idea of this strategy is to provide sufficient preheating for the lamp filaments. At the same time, the dc bus voltage at the preheat mode is limited to a low level by applying the second-stage resonance technique. As shown by the experiments, the voltage and the time required for the lamp ignition can be greatly reduced if the filaments are sufficiently preheated. In this case, if we instantly sweep the frequency to the ignition point fs_2 (see Fig. 2.11) at the end of the preheat mode, it is very possible to ignite the lamp in a few switching cycles. Therefore, V_{dc} can be far below its steady state value when the lamp is lit on. Since the lamp characteristics vary according to the temperature, aging, gas pressure etc., the lamp may not be turned on under certain circumstances when V_{dc} reaches the limit. So the restart and protection circuit is necessary. The technique can be further implemented in the following manner.

3.2.A.i)Reducing V_{dc} at the preheat mode by employing the high frequency second-stage resonance (HFSR)

The preheating of the filaments is very important to the fluorescent lamp. Insufficient preheating will require higher voltage to ignite the lamp, and may cause improper start-up of the fluorescent lamp which shortens the lamp life.

Usually, the lamp voltage at the preheat mode in a ballast circuit shown in Fig. 2.1 should be large enough to provide the sufficient preheating current. According to the analysis in Ch.2, however, low V_p is required in order to maintain low V_{dc} at the preheat mode.

To reconcile these two contradictory requirements, the second-stage resonance technique introduced in the previous section (Sect. 3.2) can be applied. The preheating frequency is set close to the second-stage frequency fr_2. Since the preheating frequency can be much higher than the normal operating frequency, the size of the additional resonant components required for the second-stage resonance is small. This technique will be referred to as high frequency second-stage resonance (HFSR) in the later discussion.

By applying the technique introduced in Section 3.1.a (Figs. 3.1 and 3.2), the equivalent Cin at the preheat mode is reduced, and the input power flowing through the Cin branch can be small even if V_p is large. As a result, V_{dc} is low. Since the Cin branch at the preheat mode has little effect on the resonant tank, high lamp voltage can be easily obtained by adjusting Lr or Cr. Due to the modulation of Lin, the equivalent capacitance of the Cin branch at a normal operating frequency is higher than the pure capacitor (as shown in Figs. 3.1(b) and 3.2(b)). Consequently, a smaller input capacitor can be used. The efficiency at

full load can be improved. However, Lin also distorts the input current shape. Too large magnitude for Lin is not desired.

If we apply the technique introduced in Section 3.1.b (Figs. 3.3), low V_{dc} and relatively high lamp voltage can be obtained at the same time. Due to the high fr_2, the value of Lr_2 is usually small. Lr_2 can be integrated into the leakage inductance of the isolation transformer. The magnetic component number in the circuit does not increase. The additional cost is negligible.

3.2.A.ii) Restart and protection scheme

As mentioned before, under sufficient preheating, instant start can ignite the lamp before V_{dc} rises high. However, under some circumstances such as low temperature, end of lamp life, etc., a higher lamp voltage and longer time are required to ignite the lamp. It is possible that the lamp is not ignited when V_{dc} reaches the limit. So the restart scheme is necessary. Besides, when the lamp fails (e.g., evacuated or operated with emitter-less), the circuit will operate at extremely light load conditions. Since the ignition frequency and the normal operating frequency are much lower than fr_2, the HFSR technique does not protect the semiconductor devices from suffering high voltage stress under these circumstances. So the protection circuit is needed. The protection circuit, the restart scheme, and the principle waveforms are shown in Figs. 3.6 and 3.7.

The basic idea of the protection and restart scheme is to sense the dc bus voltage. Once the circuit detects the V_{dc} level to be higher than the maximum allowable level, say, 450 V, the timing resistor of the control circuit is reduced. Therefore, the frequency is pushed to

the preheating frequency fs_1. V_{dc} will drop down gradually. Once V_{dc} drops below a certain value, say, 410 V, we can restart the lamp by sweeping the switching frequency from fs_1 to fs_2 very quickly, just like in the normal starting procedure. The hysteresis, ΔV_{dc}, is determined by the R2/R1 in Fig. 3.6. If the lamps cannot be ignited for a certain number of times of the start-up attempts, we can shut down the circuit.

Since the voltage determining the ignition of the lamp is the peak value instead of the rms value, the spikes on the lamp voltage (shown in Fig. 3.7.b) will help in starting the lamps. This is similar to the lamp waveform in the low frequency ballast which uses the saturation transformer to help ignite the lamp.

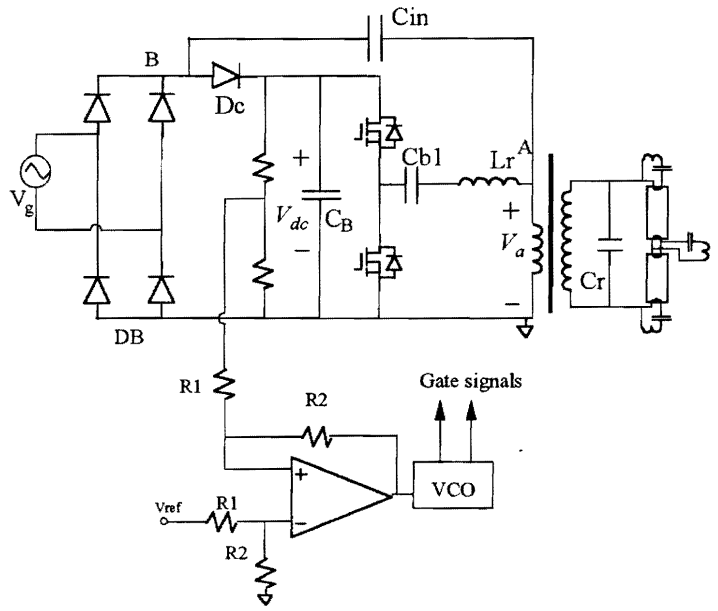
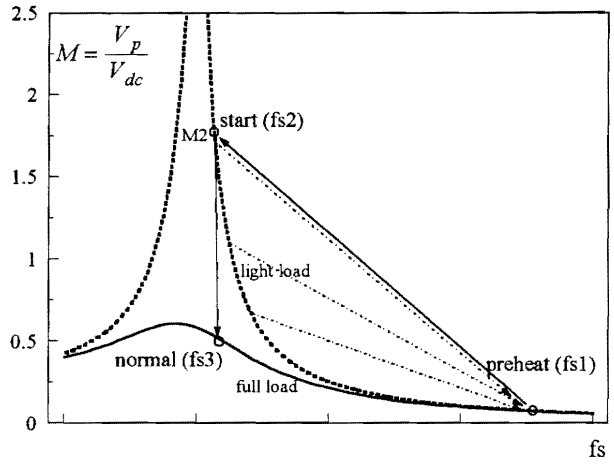
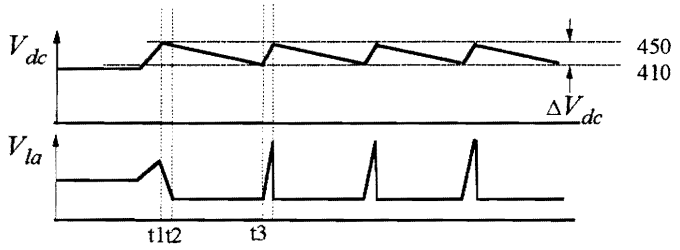


Fig. 3.6 Diagram of protection circuit



(a)



(b)

Fig. 3.7 Schemes and principle waveforms of restart and protection

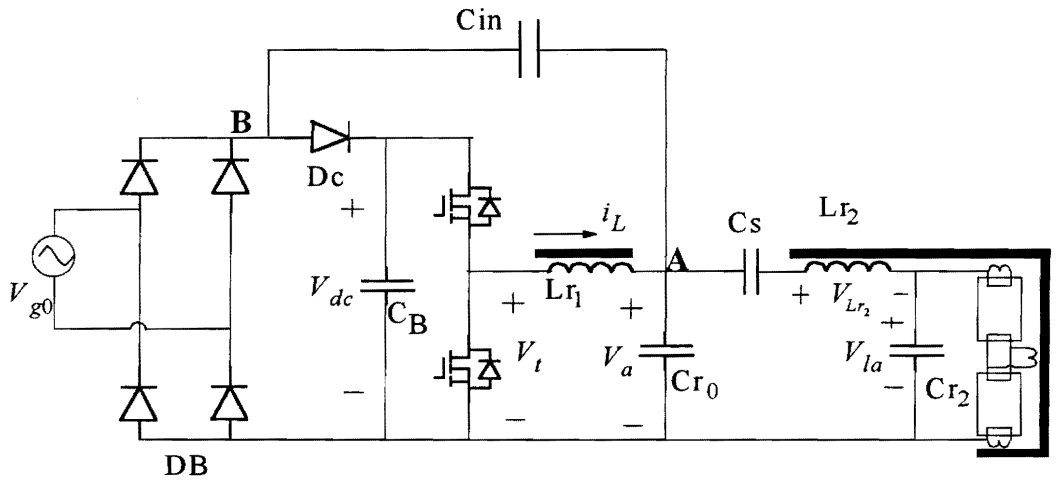
3.2.B) Strategy II: "low" frequency second-stage resonance (LFSR) technique

With the HFSR techniques, the second-stage resonance frequency fr_2 is much higher than the first-stage resonance frequency, fr_0, the voltage gain around fr_2 is not high enough to ignite the lamp and to maintain the lamp lighting. So the start-up frequency has to be much lower than fr_2. Therefore, the HFSR technique cannot lower the steady state dc bus

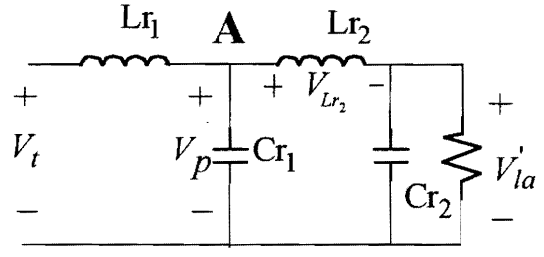
voltage at the start-up mode, an alternative is to consider moving the *second-stage* resonance peak close to *the first-stage* resonant peak, fr_0. This technique is referred to as "low" frequency second-stage resonance (LFSR) in the following discussion.

Figure 3.8 shows the circuit diagrams. The approximate ac equivalent circuit consists of two LC resonant stages. The blocking capacitor, C_s, moves the lamp side to reduce its conduction loss and to reduce the maximum voltage across the input capacitor, Cin. Lr_2 and Cr_2 form a parallel resonant tank. Through proper design, Lr_2 and Cr_2 can provide the desired lamp voltage. Meanwhile, V_p, the ac amplitude of V_a, can still remain roughly half of V_{dc} to obtain the good input power factor. Therefore, the transformer can be eliminated if the isolation is not required. In addition, the filament windings can be coupled to Lr_2. The reason for doing so will be explained later. Since the LFSR technique requires a large additional inductor (Lin or Lr_2), the technique designed to reduce Cin (Section 3.1.a) becomes impractical because a large magnitude for Lin usually causes the distortion of the line current. Therefore, the technique of reducing V_p (Section 3.1.b) is the only candidate for the LFSR technique.

Figure 3.9 shows the bode plots of the normalized voltages under light load and full load. It is preferable to operate the circuit at the frequency inside the shaded areas in Fig. 3.9. It should be noted that V_p at light load is always lower than that at full load inside the shaded area. Through proper design, low V_{dc} at light loads can be achieved. In addition, V_{la} at light load is always higher than that at full load; the high lamp voltage required for a low output power operation is also obtained.



(a)



$$Cr_1 = Cr_0 + C_{in,eq}$$

(b)

Fig. 3.8 LFSR technique:
(a) circuit diagram, (b) approximate ac equivalent circuit for the resonant tank

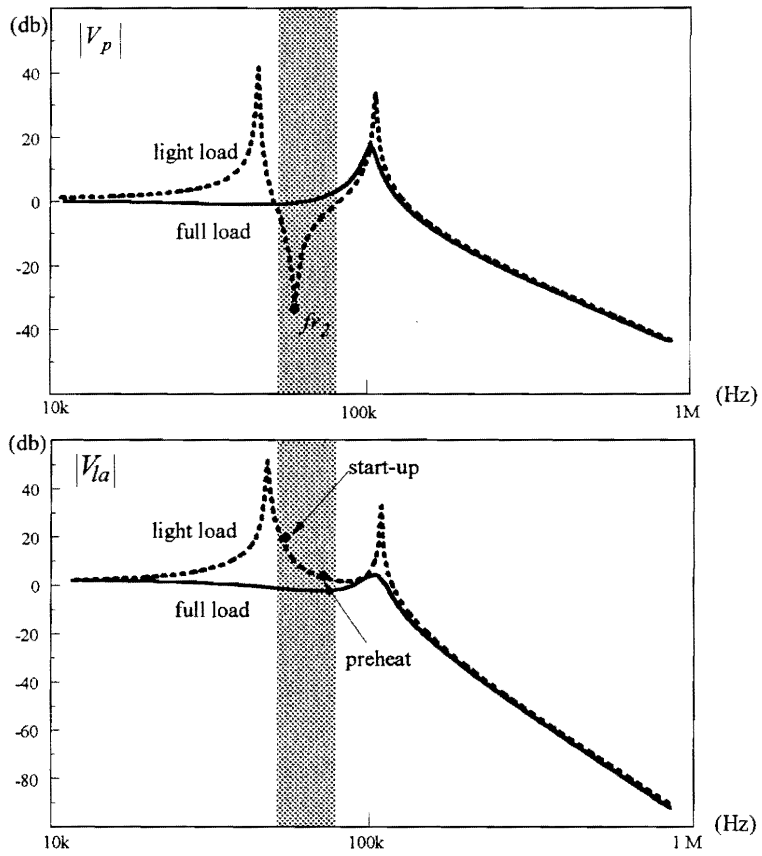


Fig. 3.9 Normalized V_p and V_{la}

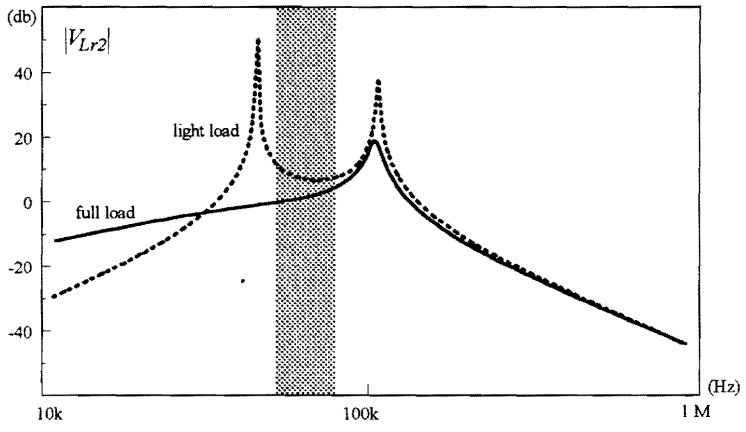


Fig. 3.10 Normalized V_{Lr2}

The filament windings in this circuit are coupled to Lr_2 (Fig. 3.8). The purpose is to reduce the filament power loss at full load. As shown in Fig. 3.10, inside the shaded area, V_{Lr2} at light load is larger than that at full load. Therefore, the filament current at full load can be reduced.

Although the LFSR technique increases the size of Lr_2, it can greatly reduce the size of Lr_1. The reason is that V_p at the startup mode is much smaller than that with high frequency second-stage resonance technique. The volt-seconds applied on Lr_1 at the startup mode are reduced dramatically. Therefore, the maximum inductor current decreases significantly. The size of Lr_1 can be much smaller.

The major advantage of this strategy is that high voltage can be continuously impressed on the lamp during the lamp start-up mode without facing the possibility of the running away of V_{dc}. In case of the lamp failure, the light load characteristics automatically prevent V_{dc} from rising high. The reliability of the electronic ballast improves. In the contrast, the HFSR technique has to rely on the protection circuit when the lamp fails. Moreover, the proper ignition of the lamp very much depends on the control circuit parameters and the lamp characteristics. In practice, since these component parameters are discrete, the ignition time varies from lamp to lamp. It may become an annoying experience if it takes dozens of restart attempts (usually it takes several hundred milliseconds for one restart attempt) to turn on a lamp. Unsynchronized ignitions of the different lamps in a large room can also become a mental nuisance.

3.3 Experimental results:

The experiments were carried out to verify the proposed strategies of reducing the dc bus voltage at light loads. Two FHF32 lamps (manufactured by Matsushita) were used. This type of lamp requires 0.4 Arms preheating current (for 1 second preheat time) and 400 Vrms per lamp ignition voltage (107 Vrms per lamp for 45-W output power). The input line voltage is 277 Vrms or 392 V_{peak}. The goal was to limit the maximum V_{dc} at startup instant to be less than 450 V.

3.3.A) Experimental results of Strategy I: HFSR with instant startup

Both second-stage resonance techniques were carried out. Under room temperature, both methods achieve the desired low V_{dc} at start-up instant.

3.3.A.i) Reducing Cin at the preheat mode

Figure 3.11 shows the experimental result of the circuit shown in Fig. 3.1(a). The components were chosen as: Cin=20.6 nF, Lin=100 uH, Cin_1=10 nF, Lr=520 uH, Cr=1 nF, the transformer turns ratio=1:1.8. Due to the modulation of Lin, the equivalent Cin is larger than its real value at the normal operating frequency(see Fig. 3.1.a). So Cin is smaller than that calculated by Eq. (2.14). The preheating current of more than 600 mA was achieved at a frequency of about 120 kHz. The steady-state V_{dc} at the preheat mode was about 385 V.

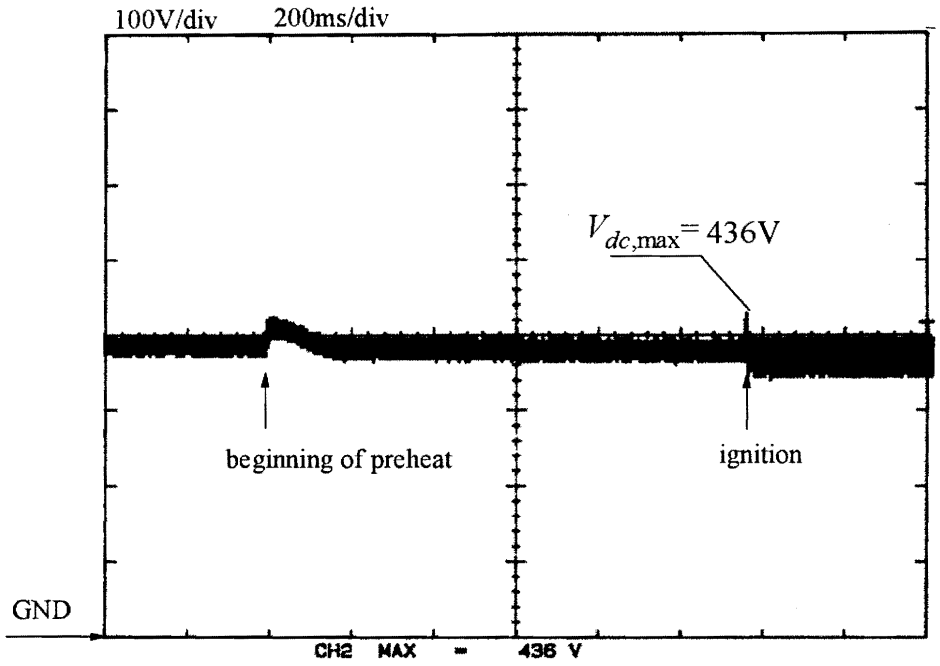


Fig. 3.11 Experimental results of Strategy I by reducing Cin

The bump of V_{dc} shown in Fig. 3.11 at the beginning of the preheat mode can be reduced by "soft-start": the frequency is set to a frequency higher than fr_2, e.g., 200 kHz, in the beginning of preheating, and then swept to fr_2, e.g., 120 kHz, gradually. As shown in Fig. 3.11, the maximum V_{dc} at the preheat and start-up modes is only about 436 V.

3.3.A.ii) Reducing V_p at the preheat mode

The circuit shown in Fig. 3.3(a) was implemented to reduce V_p at the preheat mode . Figure 3.12 shows the experimental result. In this experiment, the components were: Lr_1=500 uH, Cr_0=3.3 nF, Cin=28 nF, Lr_2=100 uH, Cb=47 uF (450 V), Cr_2=1.5 nF, the transformer turns ratio=1:1.82. The preheating current of about 480 mA was achieved at

the frequency of about 150 kHz. The steady state Vdc at the preheat mode was about 405 V. Under instant start-up, the maximum V_{dc} at ignition instant was about 424 V.

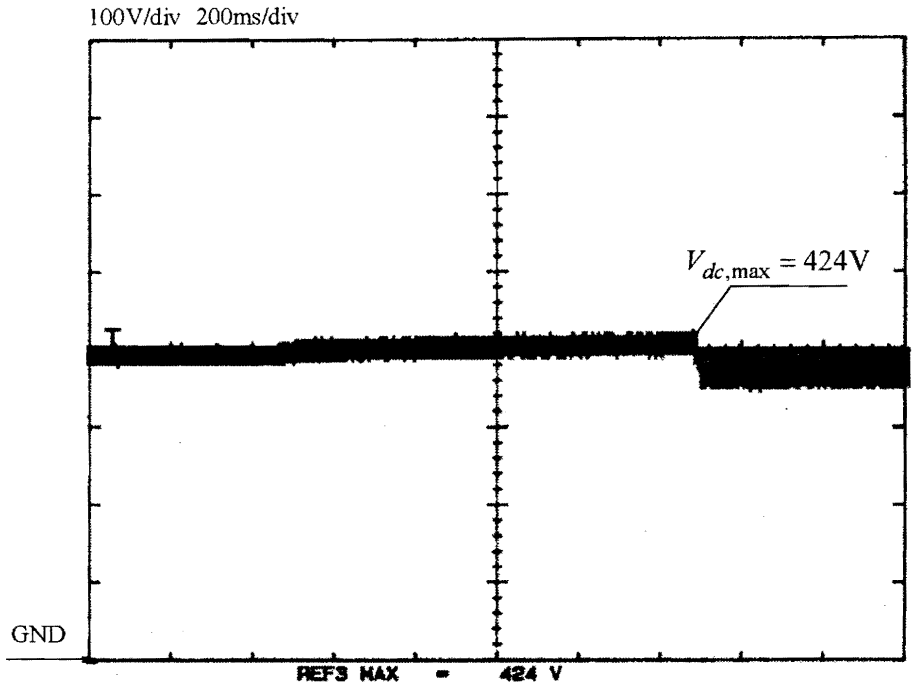


Fig. 3.12 Experimental results of Strategy I obtained by reducing V_p

3.3.B) Strategy II: LFSR technique

The circuit shown in Fig. 3.8(a) was carried out. Figure 3.13 shows the experimental result. The components were chosen as: Lr_1=520 uH, Cr_0=10 nF, Lr_2=710 uH, Cr_2=12 nF and Cin=36 nF. The preheating frequency was 55 kHz, the ignition frequency was 47 kHz. Steady-state V_{dc} was 385 V at preheat mode and 450 V at the startup mode. The preheating filament current was about 480 mA. From Fig. 3.13, we can see that the maximum V_{dc} at startup instant is only about 420 V.

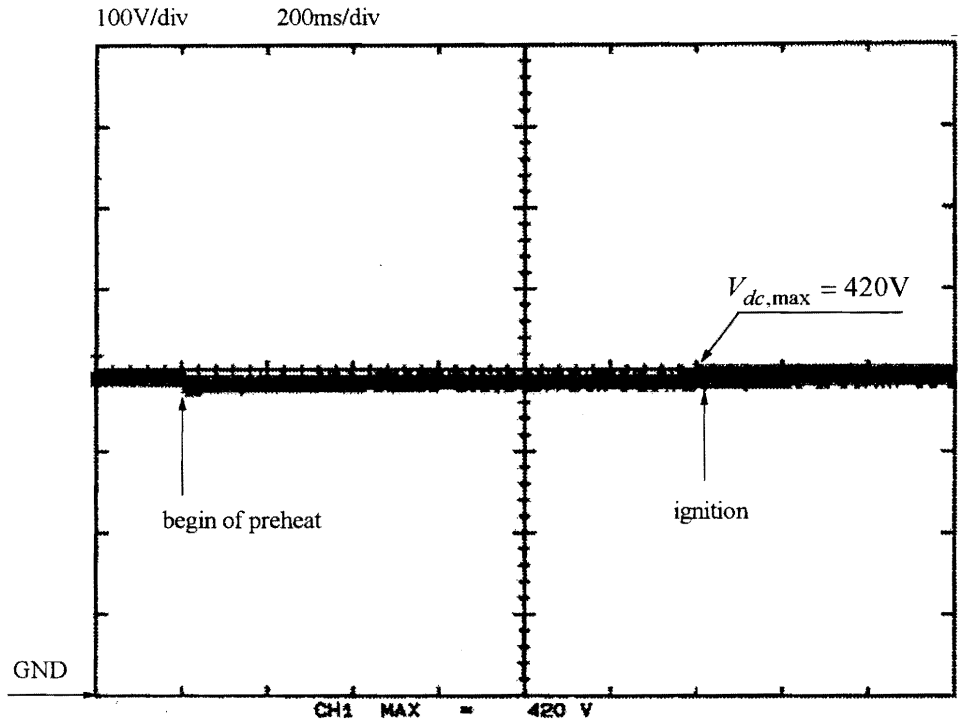


Fig. 3.13 Experimental result of Strategy II

3.4 Summary

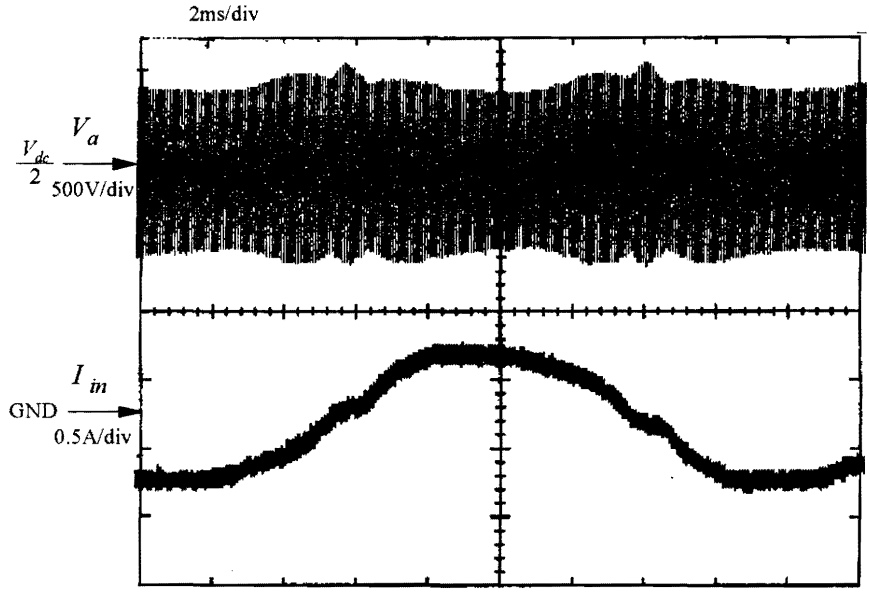
In this chapter, the second-stage resonance techniques were proposed to reduce the dc bus voltage (V_{dc}) at light loads operation. Two strategies of reducing V_{dc} at light loads were developed for the electronic ballast operation. Strategy I, which applies the HFSR technique to reducing V_{dc} at the preheat mode and adopts the instant start-up to limit the maximum V_{dc}, proves to be effective in the lab. But this strategy might not be viable in practice. On the contrary, the LFSR technique can limit V_{dc} under any load conditions through proper design. The reliability of the circuit improves. If the isolation is not required, the number of magnetic components does not increase. Furthermore, the size of the original inductor Lr_1 is greatly reduced. The total cost can be reduced.

Chapter 4 Approach to reducing the THD of the input current and the crest factor of lamp current

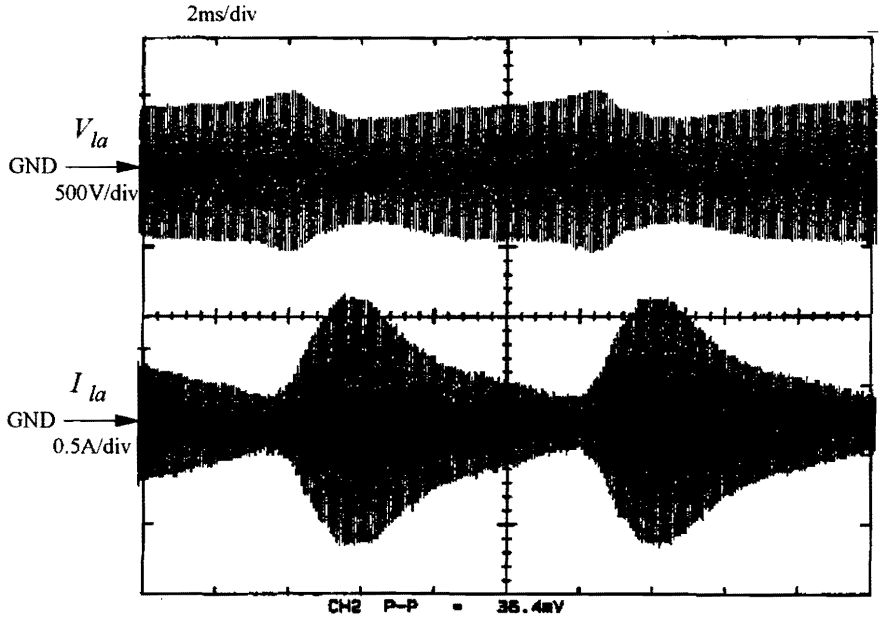
Because of the existence of Cin, V_a is affected by the line voltage (Section 2.2). The 120-Hz ripple is imposed on the envelope of V_a. Thus the crest factor of the lamp current is high. In addition, the condition for the unity power factor, $2V_p=V_{dc}$, cannot be satisfied all the time in a complete line cycle. As a result, the input current is not purely sinusoidal. The THD of the input current increases.

By applying LFSR technique (Section 3.3.b), the waveform of the lamp current can be near sinusoidal because of the second filter stage: Lr_2 and Cr_2. But there is still the 120-Hz ripple on the envelope of V_a. The input current waveform is still distorted. Since this 120-Hz ripple is amplified by the second LC stage, the crest factor of the lamp current can be very poor.

Figure 4.1 shows the experimental waveforms of the input current, lamp voltage and lamp current. The power factor was measured to be 0.98, the THD was 10.4% and the crest factor of the lamp current was about 2.4. The components were: Cin=36 nF, Cr_0=10 nF, Lr_1=420 uH, Cr_2=12 nF and Lr_2=710 uH. The preheating frequency was 55 kHz. The steady state V_{dc} is 387 V. The ignition frequency was designed to be 47 kHz, and the corresponding steady state V_{dc} was 450 V. The normal operating frequency was 40 kHz, and the lamp output power was about 80 W.



(a)



(b)

Fig. 4.1 Experimental waveforms of LFSR technique:
(a) input current and V_a, (b) lamp voltage and lamp current

Since the reason for the high THD of the input current is the 120-Hz ripple on the envelope of V_a, the input current waveform can be improved if the envelope of V_a is smoothed out. If the circuit shown in Fig. 3.8.(a) is designed so that the envelope of V_a is

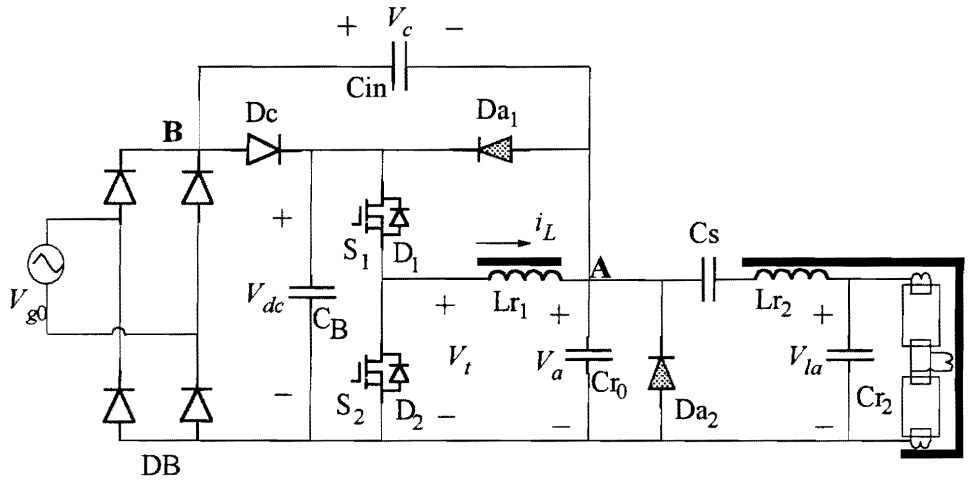


Fig. 4.2 The modified circuit with LFSR

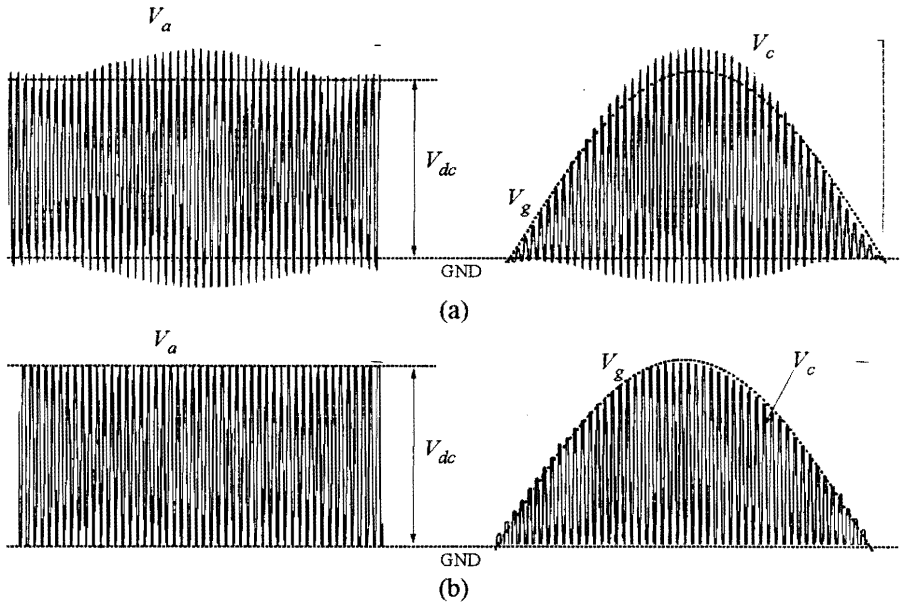


Fig. 4.3 Waveforms of V_a and V_c: (a) without Da_1 and Da_2, (b) with Da_1 and Da_2

always larger than the dc bus, i.e., $2V_p > V_{dc}$, the simple diode clamping technique can be applied. The proposed circuit is shown in Fig. 4.2. Compared to the circuit shown in Fig. 3.8(a), two extra diodes, Da_1 and Da_2, are added to clamp the envelope of V_a.

4.1 Analysis of the operation principle of the proposed circuit

The key waveforms of this circuit are described in Fig. 4.3. Without the diodes Da_1 and Da_2, the circuit is designed so that the peak-to-peak value of V_a, $2V_p$ (or $V_{a,pp}$), is never smaller than V_{dc}. The waveforms V_a and V_c are depicted in Fig. 4.3(a). Under this condition, the input current will not follow the input voltage according to Eq. (2.6). After adding diodes Da_1 and Da_2, $V_{a,min}=0$ and $V_{a,max}=V_{dc}$ result (see Fig. 4.3.b). Correspondingly, we can have $V_{c,max}=V_g$ and $V_{c,min}=0$. Then the input average current becomes

$$i_{in,av} = f_S C_{in}(V_{c,\max} - V_{c,\min}) = f_S C_{in} V_g \propto V_g . \qquad (4.1)$$

Therefore, the good input power factor is automatically obtained without any additional control.

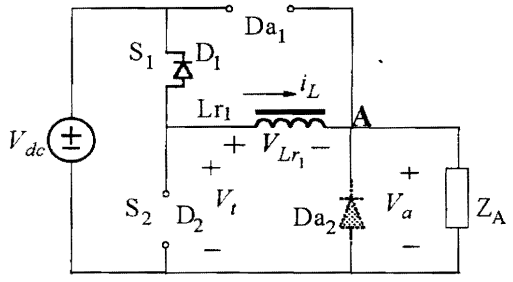
The steady state operation in one switching cycle includes six types of operation modes in one switching cycle, as shown in Fig. 4.4. Z_A stands for the impedance seen from point A. The six operation modes are explained as follows.

Mode 1:

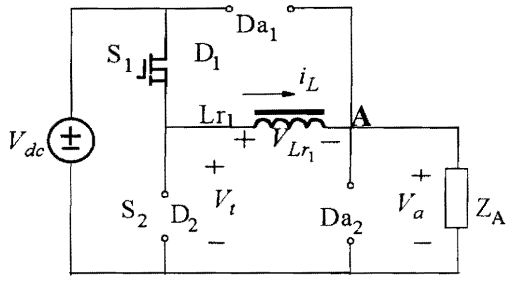
S_2 is off. The negative inductor current flows through D_1. S_1 can be turned on with ZVS. In this mode, V_a is less than V_{dc}. V_{Lr1} is always positive. Consequently, the magnitude of the inductor current i_L decreases. This mode ends when i_L decreases to zero.

Mode 2:

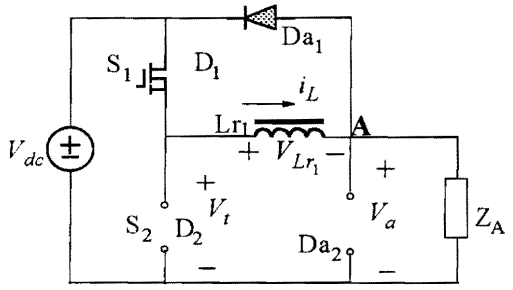
S_1 conducts. Since V_a is between 0 and V_{dc}, both Da_1 and Da_2 are off. The positive inductor current i_{Lr1} keeps increasing due to the polarity of the inductor voltage. The operation mode ends when V_a reaches V_{dc}, or when S_1 turns off.



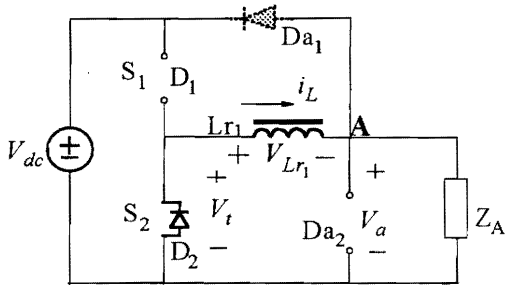
MODE 1: $i_L < 0$ & $0 \le V_a < V_{dc}$



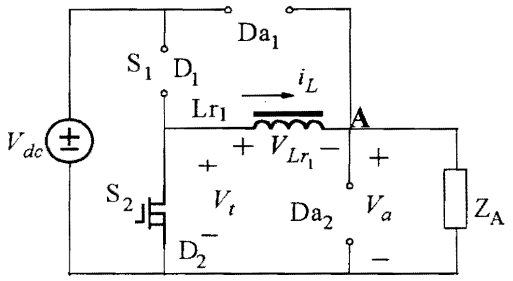
MODE 2: $i_L > 0$ & $0 < V_a < V_{dc}$



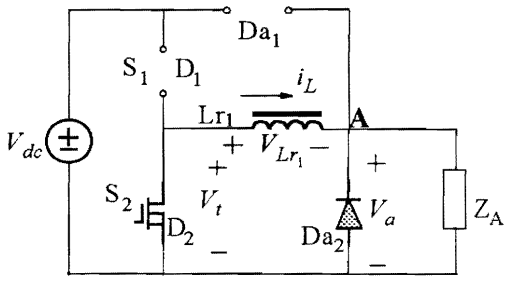
MODE 3: $i_L > 0$ & $V_a = V_{dc}$



MODE 4: $i_L > 0$ & $0 < V_a \le V_{dc}$



MODE 5: $i_L < 0$ & $0 < V_a < V_{dc}$



MODE 6: $i_L < 0$ & $V_a = 0$

Fig. 4.4 Six operation modes in the proposed circuit

Mode 3 (clamping mode):

Da_1 and S_1 conducts, V_a is clamped to V_{dc}. V_{Lr1} is zero; therefore, i_{Lr1} remains constant. This mode ends when V_a becomes less than V_{dc}, or when S_1 turns off.

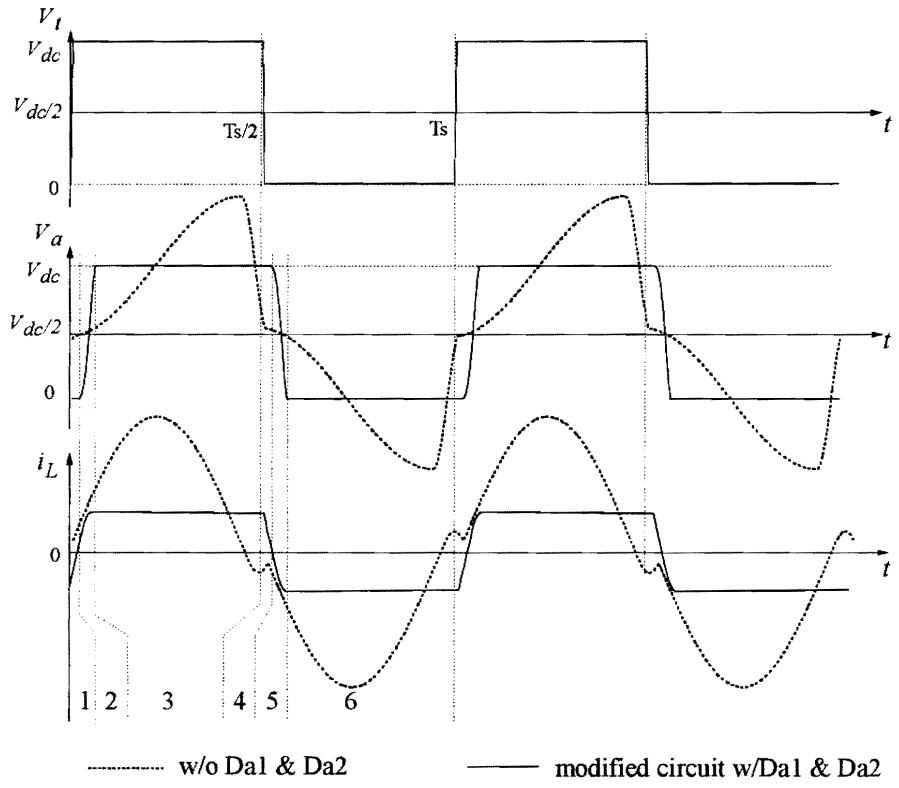


Fig. 4.5 Simulation waveforms of the inverter tank with and without Da_1 and Da_2

Mode 4:

S_1 is off, forcing the positive inductor current to flow through D_2. Consequently, ZVS turn-on of S_2 is obtained. In this operation mode, V_a is always positive. Consequently, the inductor voltage V_{Lr1} is always negative. The inductor current decreases. This mode ends when the inductor current becomes zero.

Mode 5:

S_2 is on. Neither Da_1 nor Da_2 conducts. V_a is between V_{dc} and zero. The voltage applied on Lr_1 is negative. Therefore, the inductor current keeps increasing in the opposite direction as shown in Fig. 4.4. This mode ends when V_a decreases to zero, or when S_2 turns off.

Mode 6 (clamping mode):

V_a is clamped to zero. The inductor current freewheels through Da_2 and S_2. This mode ends when V_a becomes larger than zero, or when S2 turns off.

There are many kinds of operation sequences in one switching cycle. The most common one is : Mode 1→2→3→4→5→6.

4.2 Merits of the proposed circuit

Through the proper design, Da_1 and Da_2 conduct exactly once in each switching throughout the entire line cycle. The peak to peak value of V_a ($2V_p$) is then clamped to V_{dc} during the whole line cycle. The proposed circuit will have a near unity power factor, a reduced THD and an improved crest factor. Moreover, ZVS is always ensured even if the original resonant tank (without Da_1 and Da_2) is operated in the capacitive mode.

4.2.A Ensured ZVS operation:

Because of the polarity of the voltage applied on Lr_1, the magnitude of the inductor current i_L always increases in Modes 2 and 5, and remains constant during Modes 3 and 6. The inductor current is thus always positive at the turn-off of S_1 (the end of Mode 2 or 3) and negative at the turn-off of S_2 (the end of Mode 5 or 6). Therefore, ZVS turn on of S_2

(in Mode 4) and ZVS turn-on of S_1 (in Mode 1) are always ensured regardless whether the original resonant tank (without Da_1 and Da_2) operates in the capacitive mode or in the inductive mode. This is a big improvement upon the original circuit in Fig. 2.1.

As shown in Fig. 4.5, the original resonant tank (without Da_1 and Da_2) is operated in the capacitive mode (i_L leads V_t). The dotted trace stands for the waveforms in the circuit without Da_1 and Da_2: the inductor current i_L leads the tank voltage V_t, resulting in the loss of ZVS. With the diodes Da_1 and Da_2, the inductor current always lags the tank voltage. ZVS is therefore maintained.

4.2.B Improved power factor and reduced THD of input current:

Since the positive and negative peaks of V_a are clamped to V_{dc} and zero respectively, the peak-to-peak value of V_a always equals to V_{dc}. From the previous discussion, the good input power factor is always guaranteed. The THD of the input current is very small. This is one major merit of the proposed circuit shown in Fig. 4.2.

4.2.C Improved crest factor

Another major merit of this proposed circuit is the improvement of the crest factor of the lamp current. Since the 120-Hz ripple of V_{dc} is negligible, the ac amplitude of V_a can be considered constant over half line cycle. After being filtered out by Lr_2 and Cr_2, the lamp voltage can be a very good sinusoidal waveform with the roughly constant amplitude. The crest factor of the lamp current is thus reduced.

4.3 Design considerations:

Design of the proposed circuit shown in Fig. 4.2 is outlined as follows:

i) by choosing V_{dc} to be slightly higher than V_{gp}, and assuming that the peak-to-peak value of V_a is V_{dc}., i.e., $2V_p=V_{dc}$, C_{in} is chosen according to Eq. (2.14);

ii) Lr_2 and Cr_2 are designed at first to provide the desirable second-stage resonant frequency (refer to Section 3.2.b) and the required lamp voltage;

iii) assuming the nonexistence of Da_1 and Da_2, Lr_1 and Cr_1 can be chosen to obtain $2V_p>V_{dc}$ all over the half line cycle (it should be noticed that V_p need not be constant as in Step iii in Section 2.3).

After that, Da_1 and Da_2 are added.

4.4 Experimental Results

Figure 4.6 shows the experimental waveforms of input current, V_a, lamp voltage and lamp current. The components were chosen as: Lr_1=400 uH, Cr_1=1.2 nF, Cin=30 nF, Lr_2=820 uH and Cr_2=10 nF. The input line voltage was 277 Vrms, V_{dc} was 397V at the normal operating frequency of 48 kHz. Output power was measured to be 94 W. It can be seen from Fig. 4.6(a) that the envelope of V_a is flat over the line cycle and the input current is very close to a sine wave. From Fig. 4.6(b), we can see that the lamp voltage envelope is also flat over line cycle. Consequently, the lamp current amplitude variation is much smaller than that shown in Fig. 4.1(b). The power factor was measured to be 0.995, and

THD was 4.3%. The crest factor of the lamp current was greatly reduced. CF=1.62 was measured.

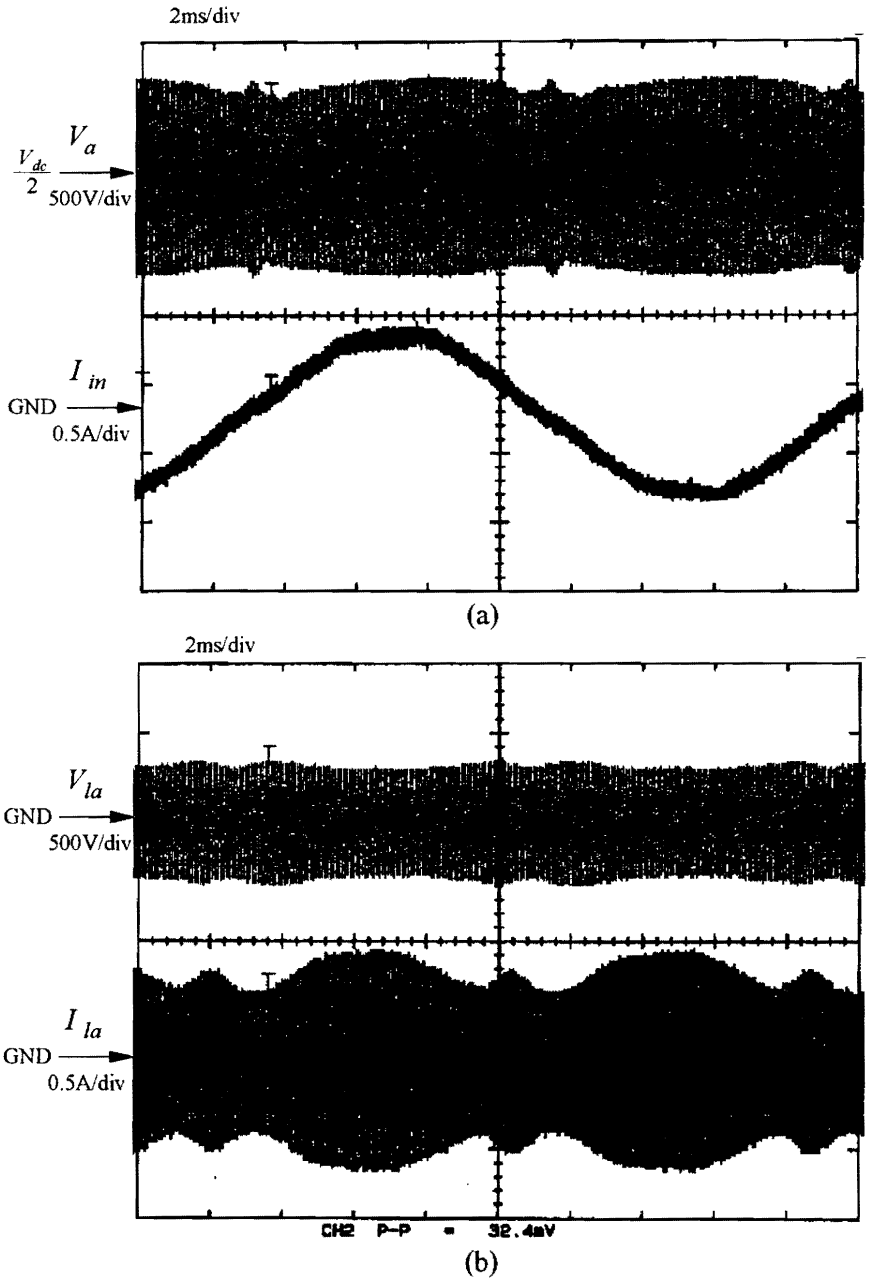


Fig. 4.6 The experimental results of proposed circuit:
(a) input current and V_a, (b) lamp voltage and lamp current

Figure 4.7 shows the experimental waveform of V_{dc}. The steady state V_{dc} for the preheat mode was 392 V at the frequency of 55 kHz, and 420 V at the ignition frequency of 48 kHz. The maximum V_{dc} at the ignition instant was measured to be about 416 V.

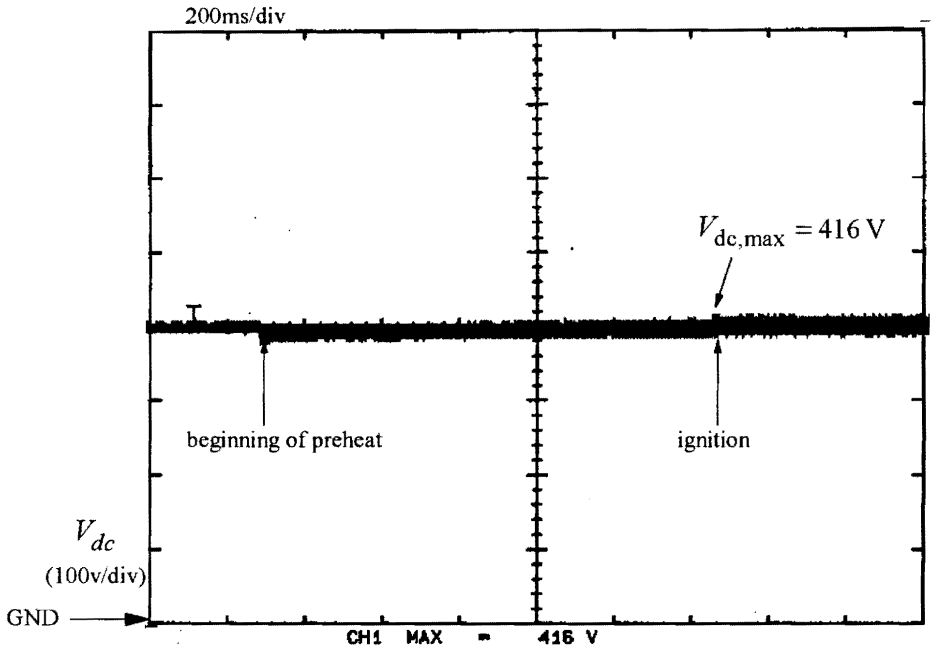


Fig. 4.7 V_{dc} in the proposed circuit

4.5 Summary

By applying the LFSR technique, the proposed circuit reduces the steady state dc bus voltage at light loads including the startup operation mode. With the employment of two clamping diodes, this ballast has a near unity power factor, and a small THD without any additional control. Moreover, the crest factor of the lamp current is reduced to about 1.6. Due to the freewheeling stage introduced by the clamping diodes, the circulating energy in this circuit increases. The efficiency may suffer slightly.

Chapter 5 Conclusion

The "charge pump" electronic ballast has become an attractive ballast topology for the discharge lamps because it eliminates the need of the bulky boost inductor. However, the devices in this circuit suffers the high voltage stress under light load conditions; the THD of the input current and the crest factor of the lamp current are high because of the existence of the charging capacitor. To solve these problems, the novel techniques of reducing the dc bus voltage at light loads have been proposed; the diode clamping technique has been employed to reduce the THD of the input current and the crest factor of the lamp current.

The general principle of reducing the dc bus voltage at light loads is to employ the second-stage resonance to reduce V_p or equivalent Cin. The HFSR technique can provide sufficient preheating at low V_{dc}. Combined with the instant startup and the proper restart scheme, this technique can greatly reduce the maximum V_{dc} at the ignition instant. Experiments showed that the HFSR technique can limit the maximum V_{dc} to less than 450 volts with 277 Vrms input line voltage while V_{dc} at full load is about 400 volts. However, this circuit cannot reduce the steady state V_{dc} at the startup mode. When the high voltage continuously impresses on the lamp without igniting it, V_{dc} invariably ramps up. The protection and restart circuit has to be activated. Due to the discrete characteristics of the lamps and the ballasts, the lamps in one room may not be turned on at the same time by adopting this kind of technique. It has become a big concern for the ballast product.

The LFSR technique can reduce the steady state V_{dc} at light loads including the start-up mode. So the high ignition voltage can be continuously impressed on the lamp without increasing V_{dc}. The experiments showed that the steady-state dc bus voltage at the start-up mode can be below 450 V (with 277 Vrms input). Although an additional inductor is needed, the size of the original resonant inductor (Lr_1) is reduced greatly. The transformer can be eliminated if the isolation is not required.

Due to the influence of the charging capacitor Cin, there exists 120-Hz ripple on the envelope of V_a (the high frequency ac voltage source). By adding two clamping diodes, the envelope of V_a is smoothed out. The experimental results showed that the near unity input power factor(> 0.99) , the low THD of input current (< 10%), and the low crest factor of the lamp current(< 1.7) can be achieved with the open-loop control.

Table 5.1 Performance comparison

	original circuit (Fig. 2.1)	HFSR w/instant start (Figs. 3.1, 3.2, 3.3)	LFSR w/diode clamp (Fig. 4.2)
power factor	0.925	0.93	0.993
THD	9.5%	10.5%	4-8%
crest factor	1.9-2.1	1.9-2.1	1.5-1.7
max. V_{dc} at startup instant	> 900 V	< 450 V	< 450 V
steady-state V_{dc} at start-up mode	> 900 V	> 900 V	< 450 V

Table 5.2 Non-magnetic component comparison

	original circuit (Fig. 2.1)	HFSR w/instant start (Figs. 3.1, 3.2, 3.3)	LFSR w/diode clamp (Fig. 4.2)
bridge diodes	1000 V	500 V	500 V
fast diodes	2 of 1000 V	2 of 500 V	4 of 500 V
MOSFETs	2 of 1000 V	2 of 500 V	2 of 500 V
bulk cap	1000 V	450 V	450 V
high frequency cap	3 of 1000 V	4 of 500 V	4 of 500 V

Table 5.3 Comparison of the magnetic components' volume (unit: cm^3)

	original circuit (Fig. 2.1)	HFSR w/instant start (Figs. 3.1, 3.2, 3.3)	LFSR w/diode clamp (Fig. 4.2)
Lr_1	35.3	35.3	21
Lr_2 or Lin	0	1.9	21
transformer	26.8	26.8	0
total	62.1	64	42

Table 5.1-3 list the performance and components comparison among the original circuit (shown in Fig. 2.1), the circuits using HFSR techniques (shown in Figs 3.1, 3.2 and 3.3) and the circuit using the LFSR and the diode clamp techniques (shown in Fig. 4.2). As can be seen from Table 5.1-3, by employing the LFSR and the diode clamping techniques, the circuit performance is improved dramatically; the voltage stresses of all the semiconductor

components and capacitors are reduced by half; and the number of the magnetic components remains the same while the size is reduced if the isolation is not required. Therefore, the cost of the proposed circuit shown in Fig. 4.2 is reduced dramatically.

In conclusion, from the points of both of the performance and the cost, the improved circuit (shown in Fig. 4.2) is a promising topology for the fluorescent lamp ballast.

References:

[1] Minoru Maehara, "Inverter device for stable, high power-factor input current supply", U.S. Patent 5274540, Dec. 28, 1993

[2] Gin P. So, "Combination ballast for driving a fluorescent lamp or tube and ballast protection circuit", U.S. Patent 5387846, Feb. 7, 1995

[3] Adan F. Hernandez and Gert W. Bruning, "High frequency inverter with power-line-controlled frequency modulation", U.S. Patent 5404082, Apr. 4, 1995

[4] Peter W. Shackle, "Circuit for powering a gas discharge lamp", U. S. Patent 5412287, May 2, 1995

[5] Lloyd J. Perper, "Adaptive resonant ballast for discharge lamps", U. S. Patent 5003231, March 26, 1991

[6] Peter W. Shackle, "Electronic ballast with two transistors and two transformers", U. S. Patent 5416388, May 16, 1995

[7] Charles B. Mattas and Jos R. Bergervoet, "Lamp ballast with frequency modulated lamp frequency", U. S. Patent 5410221, April 25, 1995

[8] Jozef R. M. Bergervoet, "High frequency discharge lamp", U. S. Patent 5400241, March 21, 1995

[9] Machael Madigan, Robert Erickson and Esam Ismail, "Integrated high quality rectifier-regulators", IEEE PESC'92 Record, Volume II, pp.1043-1051

[10] Milan M. Jovanovic, Dan M. C. Tsang and Fred C. Lee, "Reduction of voltage stress in integrated high-quality rectifier-regulators by variable frequency control", IEEE APEC'94 Proceedings, Volume 2, pp.569-575

Vita

The author was born in Fuzhou, China, on July 10, 1970. He received the Bachelor of Science degree in Electrical Engineering from Zhejiang University, Hangzhou, China, in June, 1992. From 1992 to 1993, he was in the Masters of Science (M. S.) program at the same university. Since 1993, he has been with Virginia Power Electronics Center at Virginia Polytechnic Institute and State University, Blacksburg, Virginia, working toward his M. S. Degree. His research interest includes the high frequency dc/dc power converter, high frequency ac distributed power system, and high frequency electronic ballast.