MODELING AND SIMULATION OF SURFACE MOUNT PACKAGES

by

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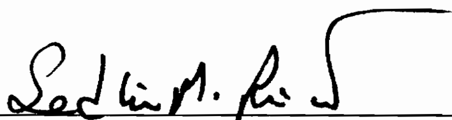

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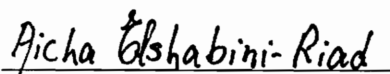

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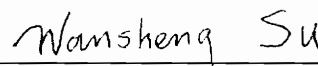

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by

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(ABSTRACT)

The objective of this thesis is to develop an understanding and performance evaluation of plastic packages for surface mount devices. Of particular interest in this work are packages for use in the gigahertz range. In order to accurately model these packages, time and frequency domain measurements of two different packaged structures are performed. Equivalent electrical circuit models for the structures are then derived and compared with measured results to determine quality of fit and validity of these models. With this modeling technique, various package parasitics affecting the circuit performance can be evaluated and compensated for in the electrical equivalent models.

Acknowledgments

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Chapter 1

Introduction

1.1 Overview

The objective of this thesis work is to provide a methodology for determining equivalent circuit models of structures in surface mount packages at high frequencies. This approach is demonstrated by developing equivalent circuit models for two specific structures, a packaged wirebond and a packaged through. The packaging used for these structures is a small outline integrated circuit (SOIC) package. Chapter 1 contains an introduction to the thesis work. Chapter 2 presents a review of current literature in the field of wireless/microwave packages and structures (such as amps and mixers). Chapter 3 presents the methodology and two examples. Chapter 4 provides a summary, conclusions, and directions for future work.

1.2 Wireless Surface Mount Packages

With the advent of high frequency wireless communications, a great demand has been created for amplifiers which are able to perform at frequencies in the GHz range. Most amplifiers which are able to operate at this frequency range are made of the binary compound Gallium Arsenide (GaAs), a semiconductor material which is known for its

ability to operate at high frequencies. At high frequencies, circuit performance is greatly affected by the package type and its material. Most circuit packaging at high speeds involves the use of stripline geometries and the packages are fabricated based on this concept. In an effort to make high speed packaging less expensive and with a smaller footprint, it is desirable to place GaAs and other high frequency semiconductor circuits in a standard plastic SOIC package.

In order to fully utilize the SOIC package in microwave applications, it must first be electrically characterized. SOIC packages are surface mountable packages used for op-amps, digital devices, timers, and other low power semiconductor circuits. The characterization of SOIC surface mount packages will be achieved in two primary stages. The first stage of characterization involves determining network models for specific portions of Package A, a SOIC package. Time domain measurements will be performed on a number of packages to determine repeatability of the measurement process. From these measurements, network models will be derived using the Modified Transient Circuit Analysis Package (MTCAP) network simulation package and the models will be verified through comparison with frequency domain measurements. The second stage of surface mount package characterization will involve the measurement and development of network models for a second surface mount package, Package B, a SOIC package.

Chapter 2

Background and Literature Review

2.1 Introduction

With the advance of high frequency wireless communications, a great demand has been created for circuits which are able to perform at frequencies in the GHz range. These demands include the amount of noise generated, the power efficiency, the gain, and the overall circuit size. At high frequencies, circuit performance is also greatly affected by the type of packaging involved. Most circuits operating at high frequencies involve the use of stripline geometries to connect the monolithic circuit to the outside world. In an effort to make these microwave circuits smaller, these geometries are included on the substrate with the circuits themselves. Such packages are called Monolithic Microwave Integrated Circuits (MMICs). The use of MMIC packages has increased in recent years as the demand for more and better communication services has increased. One area of rapid growth has been in the field of compact cellular personal communications. It is this area that GaAs integrated circuits are expected to make their biggest headway into areas which in the past have been dominated by silicon (Si) integrated circuits.

In the area of wireless communications, the market is expected to grow from $26 million in 1992 to $492 million in 1997, and to expand further to $989 million by the year

2000. In 1997, GaAs is projected to control a total of 61.3% of the wireless integrated circuit market with 38.1% of this being from power amplifiers and the remaining 23.2% coming from the sale of receivers and other transmitters.[1] With this large expected increase in demand of wireless ICs, it is important to understand the history of MMICs (microwave monolithic integrated circuits).

The appearance of MMICs came about with the technological advances in the late 1970's of GaAs processing. In an effort to reduce the size of the microwave integrated circuits (MICs) of the time (usually a hybrid microwave integrated circuit or HMIC), designers began to place the active and passive components of the MIC onto the semiconductor substrate itself. This allowed for the fabrication of multiple circuits with a single processing step by having more than one circuit per wafer.

In GaAs MMIC structures, many materials are used, not just the GaAs. For the conductors, gold is used and is deposited to a thickness of several skin depths to reduce the amount of skin loss. The capacitors that are integrated into a monolithic structure use silicon dioxide (SiO_2) or tantalum oxide (Ta_2O_5) as a dielectric material. The thin film resistors that are also integrated into the MMIC are formed of either nichrome (NiCr), tantalum (Ta), or simply doped GaAs. This ability to easily integrate all the normally external components of a microwave circuit gives the MMIC its advantage. This ability also leads to some problems in that the trimming of values after fabrication is impossible and at best extremely difficult. It is, therefore, important for the designer to include effects such as any discontinuities, bias networks, extraneous coupling, and packaging

effects, such as the dielectric constant of the packaging medium and any lossy effects of a lead frame.

2.2 Packaging Materials/Types

The most common types of MMIC packaging in use today are the metal package (hereafter referred to as a "can") and the plastic packages which are commonly used in the surface mount industry. The most common types of plastic packages are the Small Outline Integrated Circuit package (SOIC), the Plastic Leaded Chip Carrier (PLCC), and the Quad Flat Pack (QFP) family. A drawing of a common SOIC package is given in Figure 2.1. In high frequency applications, the composition and design of the lead frame can lead to many problems in the form of parasitics such as lead inductance, lead-lead mutual coupling, and lead-ground capacitance. The most common alloys used to fabricate the lead frames are known as Alloy 42, composition C194, and composition C151.[2] Another concern for the high frequency IC designer is the type of material surrounding the lead frame and IC within. There are four common types of encapsulants used in industry. The ceramic-based encapsulant most commonly used is BeO (beryllium oxide), BeO gives an excellent hermetic seal for the IC and is commonly used in aerospace and military applications. A second material sometimes used is a polyethermide, but this encapsulant

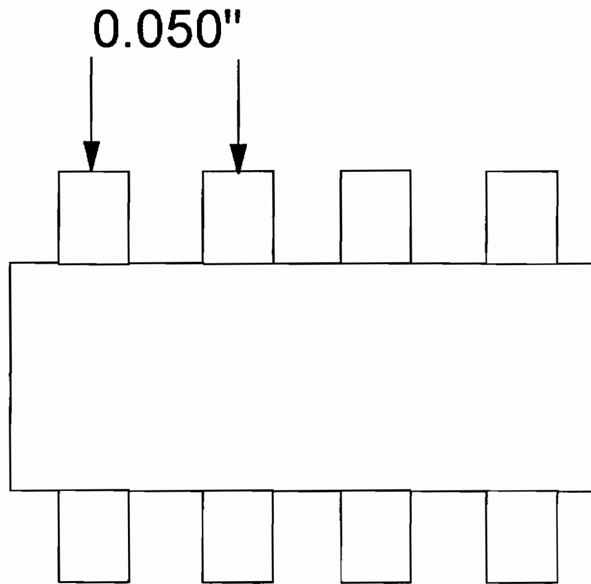

Figure 2.1 SOIC Package

has been used less and less as people switch to better encapsulants such as fused silica and epoxy resin. These materials have desirable mechanical qualities as well as good electrical qualities.[2] A standard SOIC package can typically be found with 1 mil gold wire bonds used to connect the leads with the integrated circuit. These bonds can also add some delay and parasitics of their own at high frequencies.

2.3 Current Types of Surface Mount Packages Being Used

The most common types of packages used in industry today are the SOIC (Small Outline Integrated Circuit) package, the PLCC (plastic leaded chip carrier), and the QFP (quad flat pack). The defining measure for these packages is lead pitch and lead count. Lead pitch is defined as the distance between centers of adjacent leads of a package. The lead count is simply the total number of leads that the package has. It should also be noted that of the three package types, the SOIC is limited (as a JEDEC[1] standard) to only have pins on opposing sides; that is not the case with the QFP and PLCC. The PLCC is characterized by utilizing the J-lead type on all four sides of the package. The J-lead is described graphically in Figure 2.2. The final of these packages is the QFP which is an entire family of surface mount devices. The QFP is the first of the "fine pitch" surface mount

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[1] JEDEC is the Joint Electron Device Engineering Council of the Electronic Industry Association.

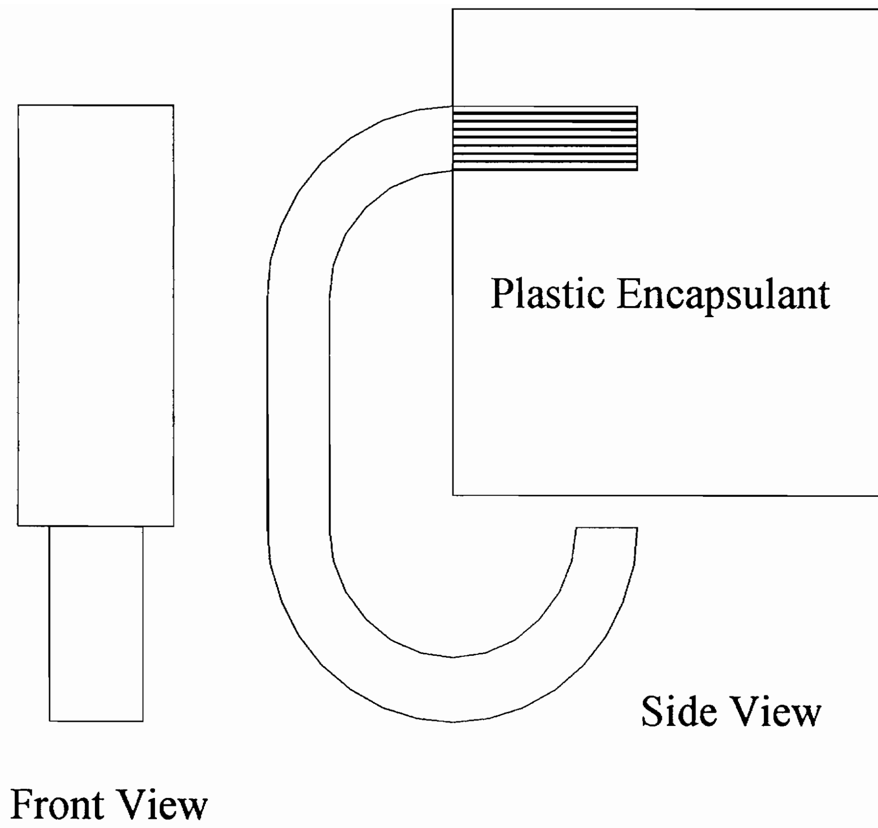

Figure 2.2 J-Lead

packages. Fine pitch is defined as having a lead pitch of less than 25 mils.[3] In future applications where height is a strict requirement, the TQFP, or Thin QFP, is expected to gain widespread use. Another new package which is growing in popularity is the thin PLCC package, offering a reliable package with low off-contact distance.

2.4 Drivers for Packaging

Surface mounted devices and surface mount technology began in an effort to improve electrical performance and to increase circuit density on printed circuit boards (PCBs). Surface mounted devices have many advantages. The advantages for the electronics designer include: 50-70% higher packaging densities, faster automated manufacturing, higher pin count on components, and better high frequency performance. Surface mount packaging is not without its disadvantages, however. Some of the disadvantages of surface mounted components are a lack of industry wide standards (besides the efforts of groups such as JEDEC) and a high initial cost for a company switching from thru-hole technology or just starting in the electronics business. These factors have been taken into account for some of the many applications of GaAs MMICs which are in use today. Gallium Arsenide FETs are now commonly used for low noise amplifiers, high gain amplifiers, broadband amplifiers, mixers, oscillators, phase shifters, and switches.[4]

2.5 A Review of Current Work

Other research groups and companies have begun to examine the SOIC package for microwave use in recent months. F. Ndagijimana, et al.,[5] published a paper on "The Inductive Connection Effects of a Mounted SPDT in a Plastic Package." This paper included the development of several parameters of an "S0-8" package. From the package dimensions given in the paper, the lead width of the package was 32 mils with a lead-lead spacing of 15 mils. The packages used for this work were ~16 mil leads with ~16 mil spacing. Another paper published by Woytaszek and Crowe[6] presents "typical values" for such parasitics as lead inductance, capacitance lead to ground, mutual inductance lead to lead, and capacitance lead to lead. But the author presents no basis in the paper for these numbers. The article often refers to the companies use of fused lead frames, but there is no distinction given as to whether the numbers presented are for a custom or fused frame. A third paper in publication recently, "Microwave Frequency Characterization and Modeling of Plastic Integrated Circuit Packages," by Sanders, et al.[7] of Florida Institute of Technology, presents results for a "standard" SOIC package. However, by all indications in the paper (e.g. the figures), the package used in this work was not a standard outline package. It is also useful to note the methodology used in the published work involves time domain gating using an HP8510 Network Analyzer, which has a time domain resolution of <5ps, as compared with the HP54124A TDR test set used for this work, which has a time domain resolution of ~1ps. Also of note, all models derived in this paper were done using frequency domain matching only. This group also used a

custom test fixture, designed and built in-house. In the reported frequency domain measurements, a resonance was observed at 2.2 GHz; this resonance was claimed by the authors to be internal to the package. This resonance does not appear in the SOIC measurements performed for ITT-GTC by Virginia Tech.

This attention to packaging and packaging parasitics has been made necessary by the significant headway GaAs MMICs have made into the field of personal communications. These integrated circuits are of great use to manufacturers of cellular and wireless telephones and to the manufacturers of pagers alike. The frequency bands of interest to these manufacturers are commonly the L and S bands, covering ~ 1-4 GHz. A general list of important criteria for a MMIC is:

- low bias voltage
- low power consumption
- low noise.

As discussed previously, these areas are ideally suited for the GaAs MMIC. A review of current literature shows that this is the case.

Many of the industry magazines which are devoted to wireless technology are often used as a launch pad for most companies to announce their newest GaAs MMIC breakthroughs. In the March 1994 issue of Wireless Design and Development[8] , Japanese firm Mitsubishi announces a GaAs MMIC designed to work in 1.89 to 1.95 GHz range with an output power of 26 dBm and a supply voltage of 5 V. This IC is an example of the demands of the wireless market. The many applications of GaAs MMICs

are evidenced in last years IEEE MTT-S conference in Atlanta. Kobayashi et al.[9] have developed and constructed a single-pole, double-throw (SPDT) switch constructed using a pin structure on GaAs which operated in the X band (8-12 GHz). Another example of GaAs MMIC technology at work is a paper by Ho, et al. which used 0.3 mm gate length MESFETs to fabricate a working amplifier with 16.6 dB of gain at 47 GHz.[10] Some systems have more stringent noise requirements and demand a better noise figure (NF) at the sacrifice of some gain. Wang et al. have demonstrated a 100 GHz amplifier with a NF of 4 dB.[11] These few examples demonstrate the high frequency capabilities of gallium arsenide microwave circuits.

As an example of how MMICs have become important, IEEE now holds a Monolithic Circuits Symposium. At this symposium, papers are presented which represent the latest in MMIC design and performance. Ohgihara, et al. have demonstrated a GaAs JFET-based amplifier and mixers operating in the L-band.[12] Morkner, Frank, and Millicker from Hewlett Packard have developed a low noise amplifier which operates from 1.5-8 GHz with NF=1.5 dB (see Figure 1).[13] Another paper that demonstrates how MMICs have advanced into the cellular market is a paper by Hara, et al. who demonstrate a AlGaAs/GaAs BJT which operates at 1.9 GHz and is useful for the next generation of digital wireless telephones.[14]

With the continued demands of wireless communications, gallium arsenide-based monolithic microwave integrated circuits will play an ever increasing role in the success of the wireless industry. With the important driver of small size with good output power,

cellular telephone makers supporting both AMPS and DECT standards will continue to search for complete power amp solutions.

Chapter 3

Modeling and Measurement of Structures

3.1 Introduction

The approach taken in this thesis research is to first acquire time domain waveforms of the structure which is to be modeled using Time Domain Reflectometry (TDR). In the time domain approach, a step waveform, f(t), is generated from a pulse generator, an HP54124A. At every discontinuity in the device under test (DUT), a reflection occurs; these reflections are then measured on the oscilloscope mainframe HP54214A. Different discontinuities produce different variations in the reflected waveform; for example, an inductance will be seen as a "bump" in the TDR waveform(Figure 3.1). A capacitance will be seen as a "dip" in the waveform(Figure 3.2). At times, simple discrete elements do not adequately describe the delays that can occur in measured systems. In this case, one may use a transmission line as part of the model. By piecewise modeling the acquired TDR waveform, an electrical equivalent circuit model can be produced. It should be noted, however, that this model is not unique. Toscano, et. al.[15] has presented a paper illustrating that while no model is unique, a model generated in the time domain is valid also in the frequency domain range. This frequency range is affected by various factors such as the accuracy of modeling discontinuities, duration of time window, and iteration accuracy. It is important in the

derivation of the circuit model that the physical layout of the DUT be taken into consideration. From these acquired waveforms, an in-house time domain circuit simulation program is used to derive the equivalent circuit of the structure (MTCAP). MTCAP requires two acquired waveforms in order to model the system under test. The first of these acquired waveforms is a reference "open" that is used as the input to the DUT and is taken from a convenient point in the overall system. The second waveform that is needed is the reflection of the input pulse as it propagates through the system. A simplified schematic of a TDR setup is shown in Figure 3.3.

An inherent advantage of modeling in the time domain is the ability to perform the fit in a "linear" fashion. Modeling is accomplished one element at a time. When one portion of the waveform is closely fitted, the modeler is able to move on to the next discontinuity. When modeling in the frequency domain, the modeler is only able to develop models based on fits over the entire range, not one component at a time.

When the equivalent circuit model is obtained, the Fast Fourier Transform (FFT) of both the acquired TDR waveform and the simulated TDR waveform (from MTCAP) is computed. This frequency domain waveform is then compared to S-Parameter measurements taken on the Hewlett Packard 8510 Network Analyzer. This comparison is achieved as a check to compare fit in the frequency domain. From the TDR measurements, S_{11} can be computed using this technique. When taking the Fourier transform of a waveform, it is important that the waveform used as a reference, and the waveform generated from that reference, be a pulse and pulse response, respectively. In

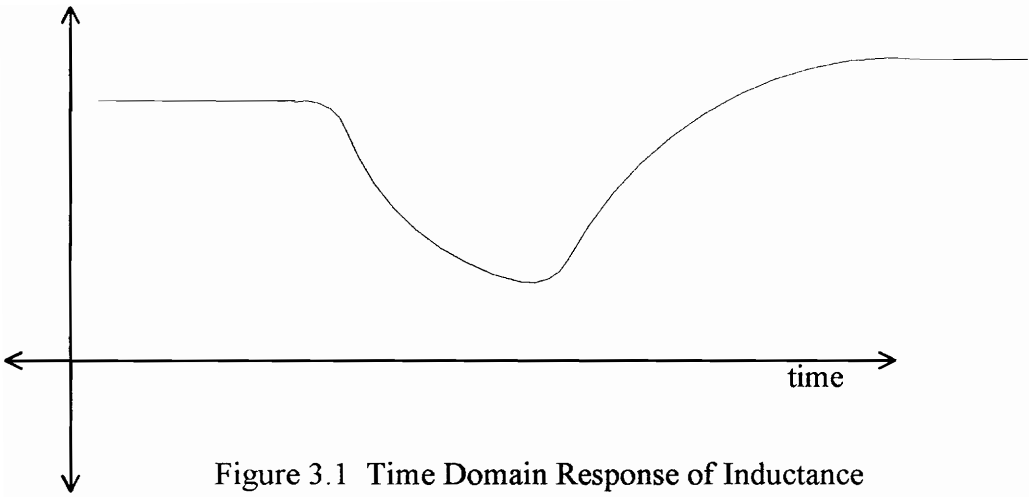

Figure 3.1 Time Domain Response of Inductance

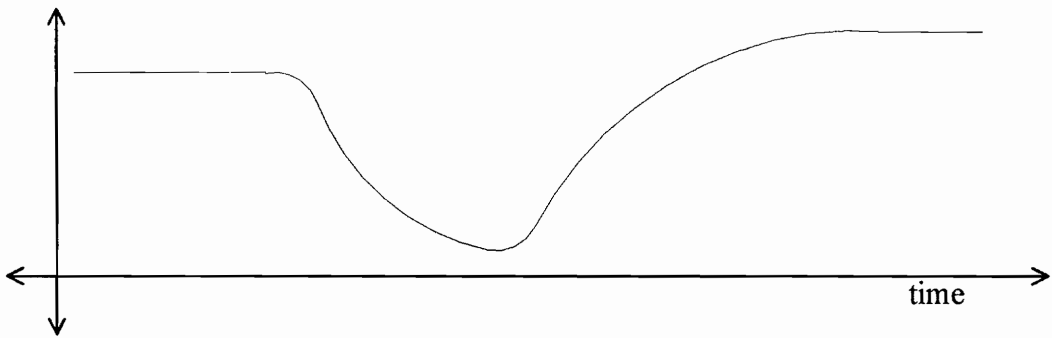

Figure 3.2 Time Domain Response of Capacitance

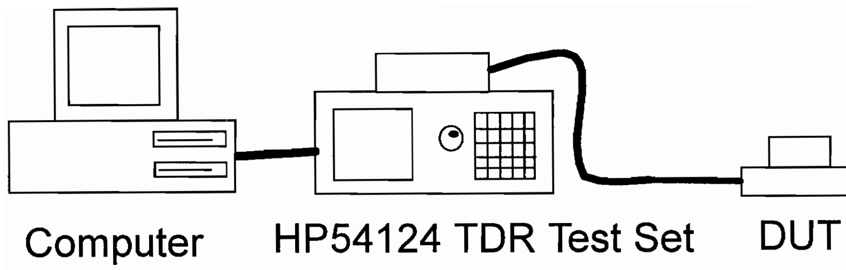

Figure 3.3 Time Domain Measurement Setup

order to find H(jω) by the Fourier transform, it is necessary to take a numerical derivative of the input waveform, x'(t), and the measured waveform, y'(t). In order to find the impulse response of the system h(t), one needs to convolve x(t) and y(t) in the time domain. It is more efficient and, in this case, desired, to simply perform the operation in the frequency domain. To compensate for the fact that the input pulse is non-periodic, a derivative approach is used where the derivative of the input pulse is used as the input impulse to the system(see Figure 3.4). The waveform is then padded with leading zeros[1] to to achieve a greater accuracy in the frequency domain. The derivative is also taken of the acquired TDR response, and it is padded with zeros such that both waveforms contain the same number of points. This new waveform (Figure 3.5) is the impulse output of the system. A Fast Fourier Transform (FFT) is then performed on these two new waveforms to get their frequency domain representations (Figure 3.6, Figure 3.7). Next, one can apply the formula in Equation 3.1, and we get the reflected impulse response of the system (or S_{11}, see Figure 3).

$$H(j\omega) = \frac{Y(j\omega)}{X(j\omega)} \qquad 3.1$$

It is important to note that in the Fourier transform, the region of information is related to the time domain window and the number of points in the transform by Equation (3.2). It is observed that in order for the information region to contain 50 points (from dc to 10 GHz), there must be 2048 total points in the transform.

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[1] It is important to note that, for a FFT, the total number of points in the waveform be equal to 2^n, where n is any integer greater than zero.

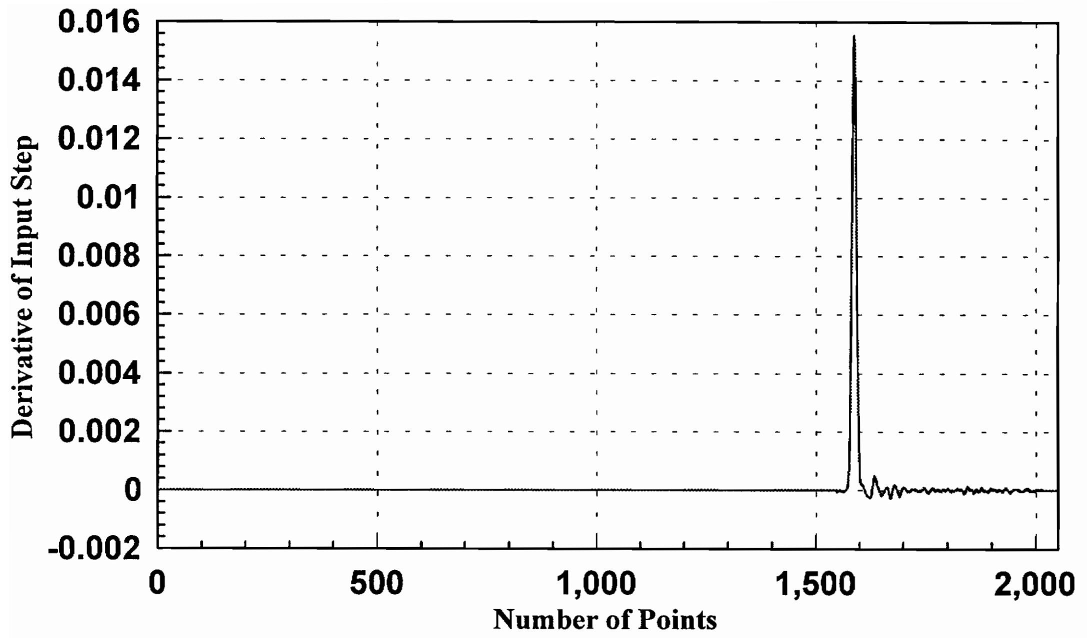

Figure 3.4 Derivative of the Input Step to the System

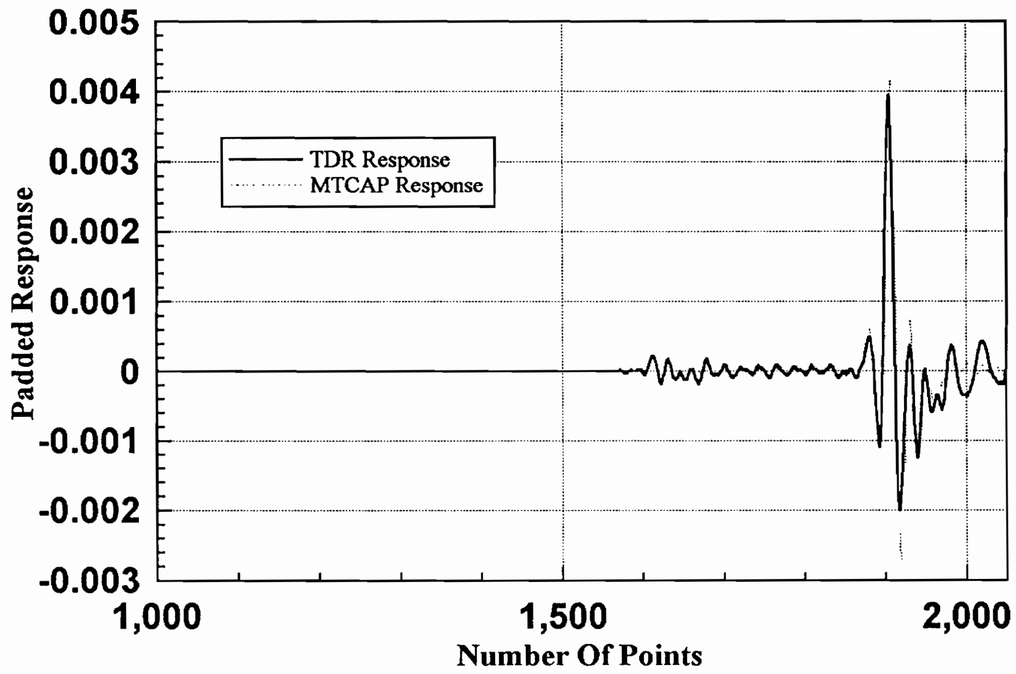

Figure 3.5 Padded Derivative of TDR Response of System

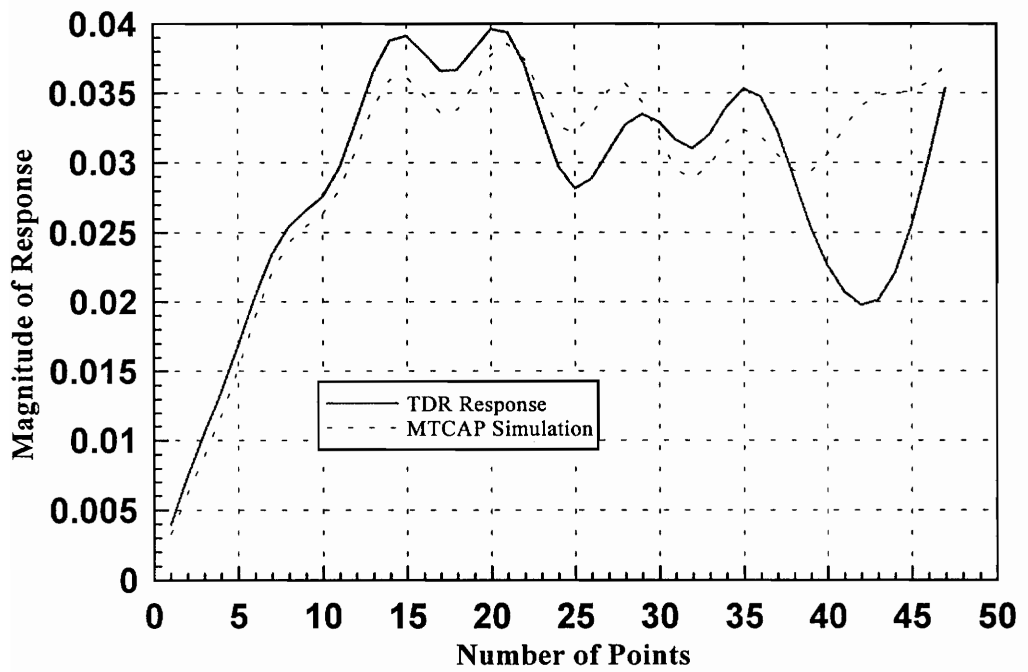

Figure 3.6 Magnitude of Output Response in Frequency Domain

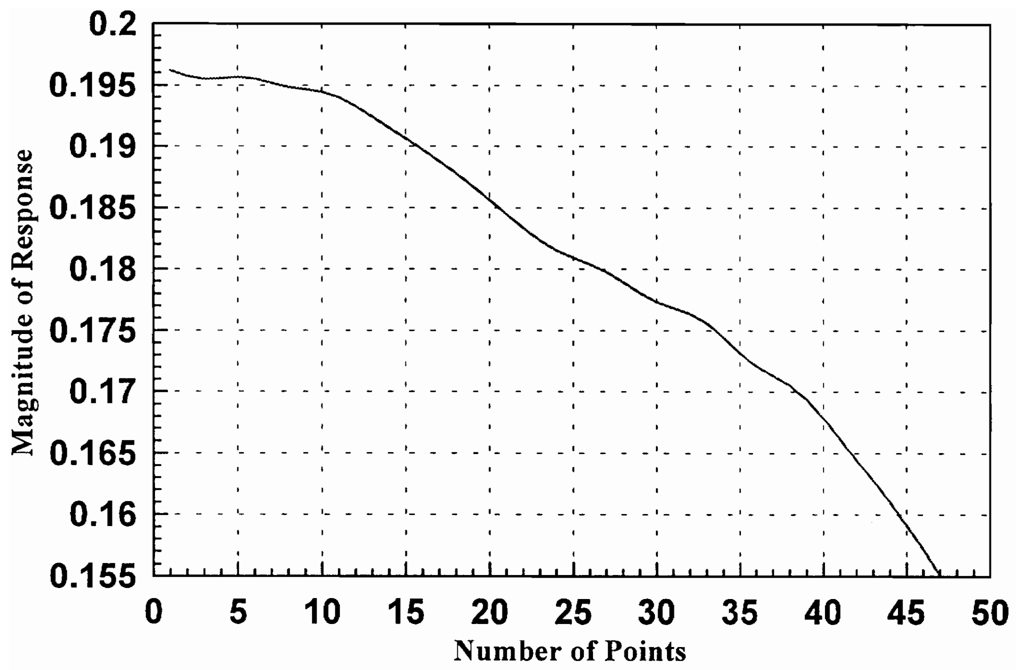

Figure 3. 7 Frequency Domain Response of Input Pulse

$$\Delta f = \frac{1}{N*\Delta t} \qquad 3.2$$

After all necessary mathematical manipulation is completed, the computed S_{11} is then compared with the measured S_{11} from the HP8510 Network Analyzer. This gives a comparison in both the time domain and in the frequency domain of the same waveform.

3.2 Time Domain Measurements

3.2.1 Package A

The package which was investigated for this work was the package labeled as Package A, a packaged bondwire. A sketch of Package A illustrated is in Figure 3.8. In order to measure the TDR response, the package was inserted into a test fixture made by InterContinental Microwave and provided by ITT-GTC. The reference waveform was acquired at the open end of the coaxial line, at the beginning of the test fixture. The acquired reference waveform is shown in Figure 3.9.

It can be seen from the TDR waveform that a large impedance was present within the structure. This impedance was due to the long wirebond section in the middle of the package. This inductance may be modeled in several ways; as several distributed LC sections, as a transmission line, or as a lumped inductor. Of these, the most preferable for accuracy in the frequency domain is the transmission line model. In order to arrive, however, at specific values for this inductance, and to arrive at how the inductance varies

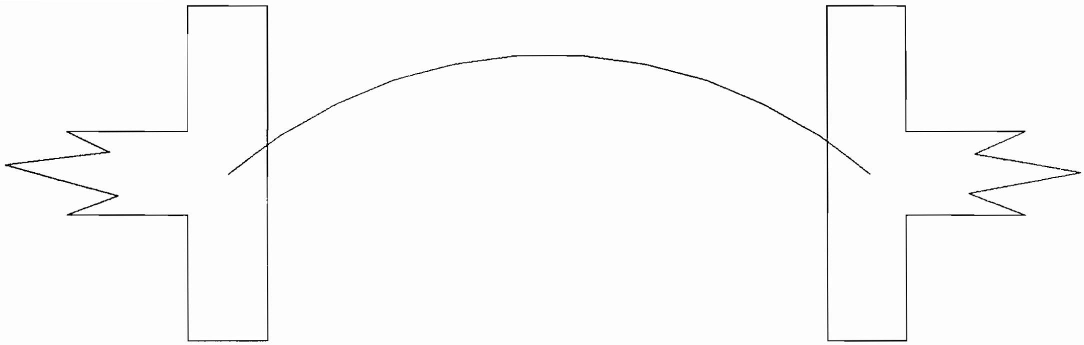

Figure 3. 8 Sketch of Package A.

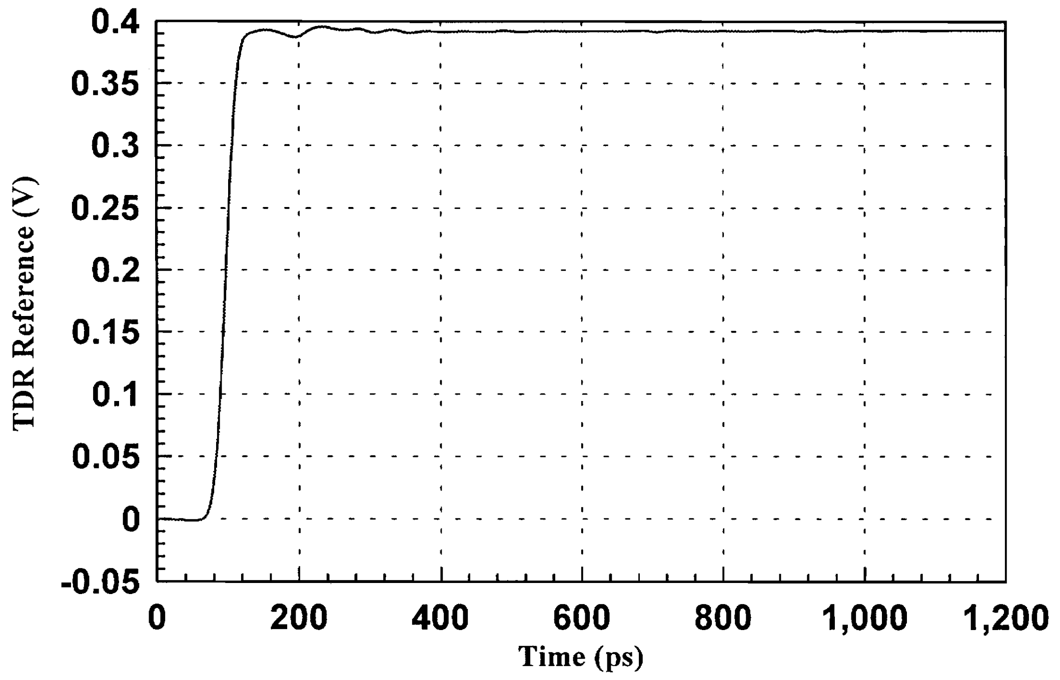

Figure 3.9 TDR Reference for MTCAP

with linear distance within the structure, a distributed LC section model was used. To arrive at suitable values for the inductance and capacitance values in these sections, the actual package dimensions and the impedance calculated from the height of the TDR response led to estimated initial values that were used to find initial approximate values for these parasitics. These values could be manipulated in the MTCAP software package provided that the impedance and the velocity associated with a section remained relatively constant. It is important to note that the actual impedance of the line may not be the same as that calculated from the height of the TDR response if the wirebond is too short to allow the wave to propagate through the bond before a reflection occurs from the end of the wirebond. This calculated impedance value does give a sufficient lower bound for the impedance of the ladder sections present in the middle of the structure. For an estimate of the upper bound, a formula for the inductance and capacitance of a round conductor suspended above an infinite ground plane (Figure 3.10) was used(Equation 3.3, 3.4). Given these approximate values as a starting point, the MTCAP simulation software package was used to adjust these elements to match the actual TDR waveform. A comparison is illustrated in Figure 3.11.

$$L = \frac{\mu \cosh^{-1}(D/2a)}{2\pi} \qquad 3.3$$

$$C = \frac{2\pi\varepsilon}{\cosh^{-1}(D/2a)} \qquad 3.4$$

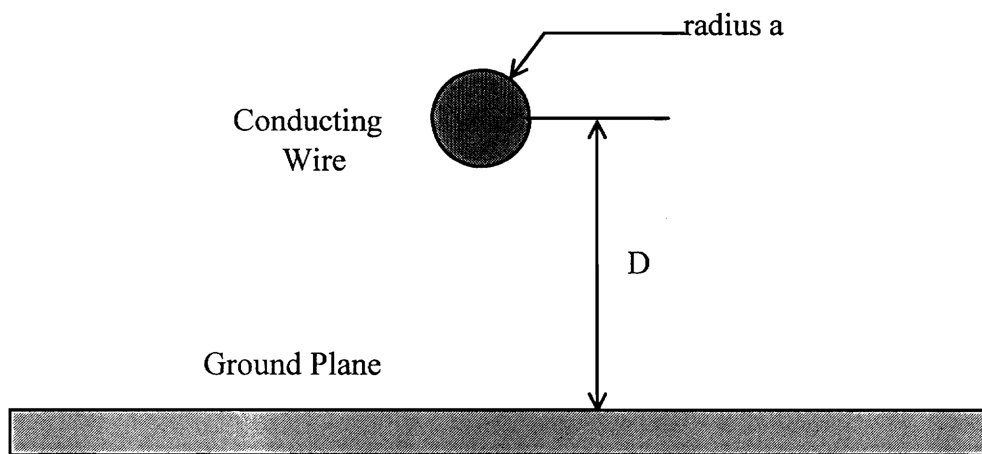

Figure 3.10 Round Conductor Above Infinite Ground Plane

3.2.2 Package B

Package B was used to find an equivalent circuit model for the second structure of interest, a through structure. This package is graphically described in Figure 3.12. Similarly, the reference waveform was taken at the beginning of the test fixture. In order to accurately derive the beginning of the actual structure of interest, several waveforms were acquired with short circuits at various places in the structure. With this time domain comparison, the actual structure can be reasonably spotted and isolated. This structure also exhibited a large inductance. In order to arrive at an equivalent circuit for this structure, the transmission line model was used to model this large inductance. To arrive at a suitable starting value, as well as a starting electrical network, the actual physical dimensions and layout of the structures were analyzed to get an initial network model with reasonable starting values. Given this start, the MTCAP simulation package was used to tweak the component values and arrive at a the desired equivalent circuit. The comparison of the TDR response and the MTCAP simulation is shown in Figure 3.13.

3.3 MTCAP Software Package

The software package used for simulating the circuits in the time domain is called MTCAP. The Modified Transient Circuit Analysis Package was written at Virginia Tech so that accurate time domain network simulation could be performed. The input to the MTCAP program is a circuit file similar to a PSpice circuit file. The MTCAP circuit file requires an input waveform file which is used as the input to the system. The circuit file

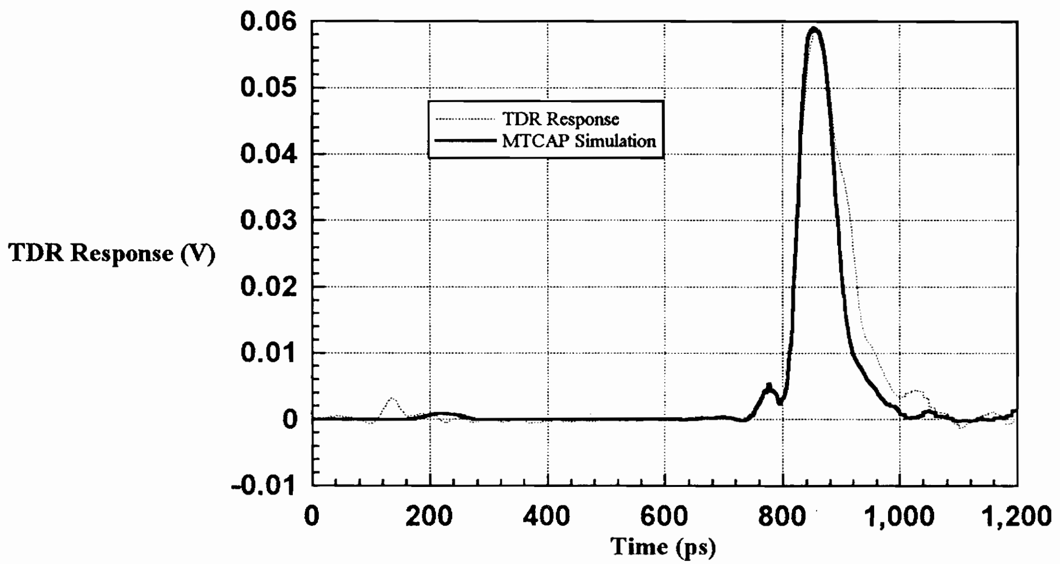

Figure 3.11 Comparison of TDR Response and MTCAP Simulation for Package A.

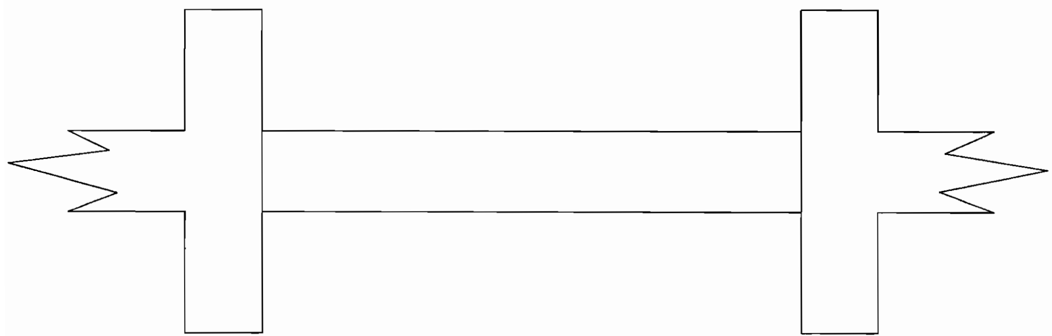

Figure 3.12 Sketch of Package B.

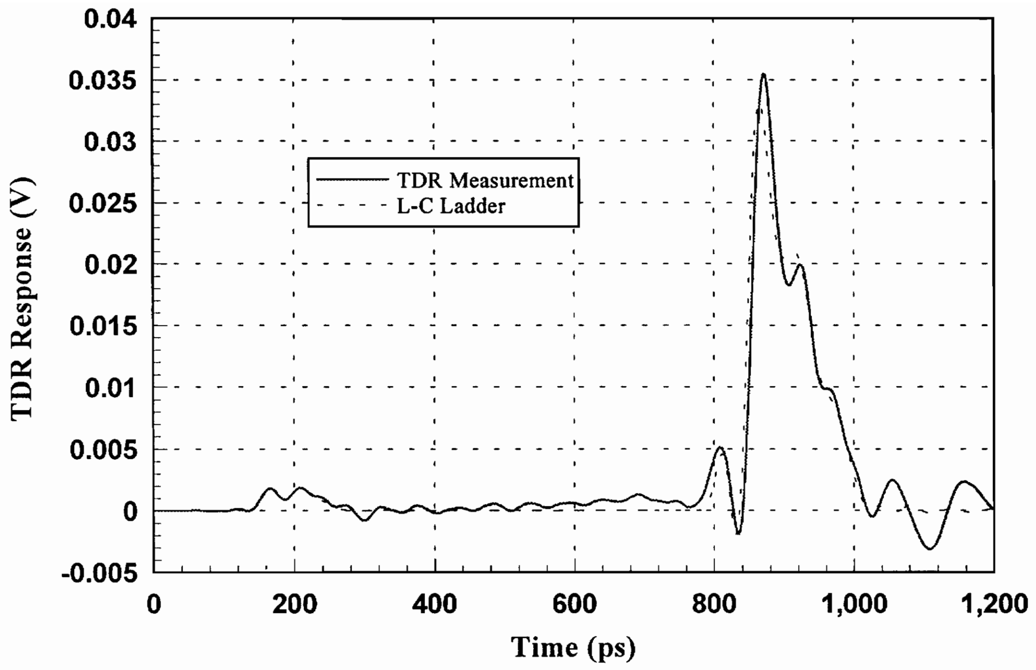

Figure 3.13 Comparison of TDR Measurement and MTCAP Simulation for Package B.

must also contain another waveform which is used for comparison. MTCAP takes a circuit file composed of elements connected by numbered nodes and computes the reflected waveform across any two number nodes. Generally, the nodes of interest for a TDR simulation are one and two. Appendix A contains the MTCAP circuit files used for this work and a review of the software package.

3.4 S-Parameter Measurements

In order to validate the time domain model, S-parameter measurements of the same structures needed to be made. The S-Parameter measurements were performed using the same custom text fixture as the TDR measurements. The calibration method used was a one-port calibration using the standards that were supplied with the test fixture. The standards supplied with the test fixture were evaluated by InterContinental Microwave and their measured performance showed that these standards were good in the frequency range from dc to 6 GHz. This calibration was performed at the beginning of packages. A one-port calibration method was used in order to closely mirror the calibration used in acquiring the TDR response. The measured $|S_{11}|$, FFT of the TDR, and the FFT of the MTCAP simulation for Package A are shown in Figure 3.14. The measured |S11|, FFT of the TDR measurement, and FFT of the MTCAP simulation for Package B are shown in Figure 3.15.

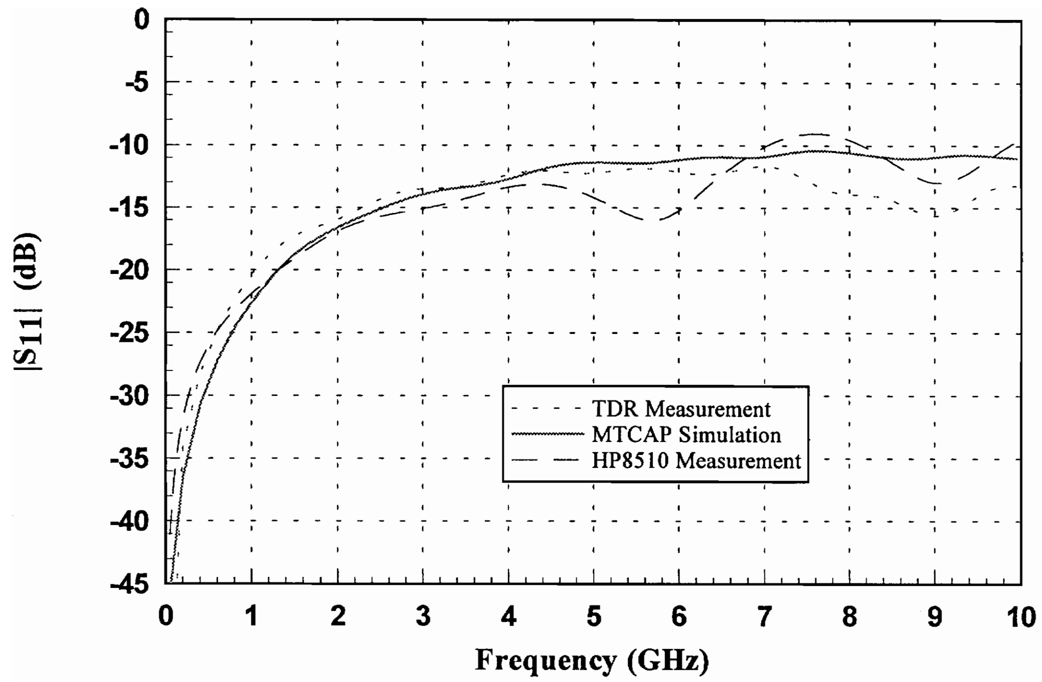

Figure 3.14 Comparison of $|S_{11}|$ for Package A

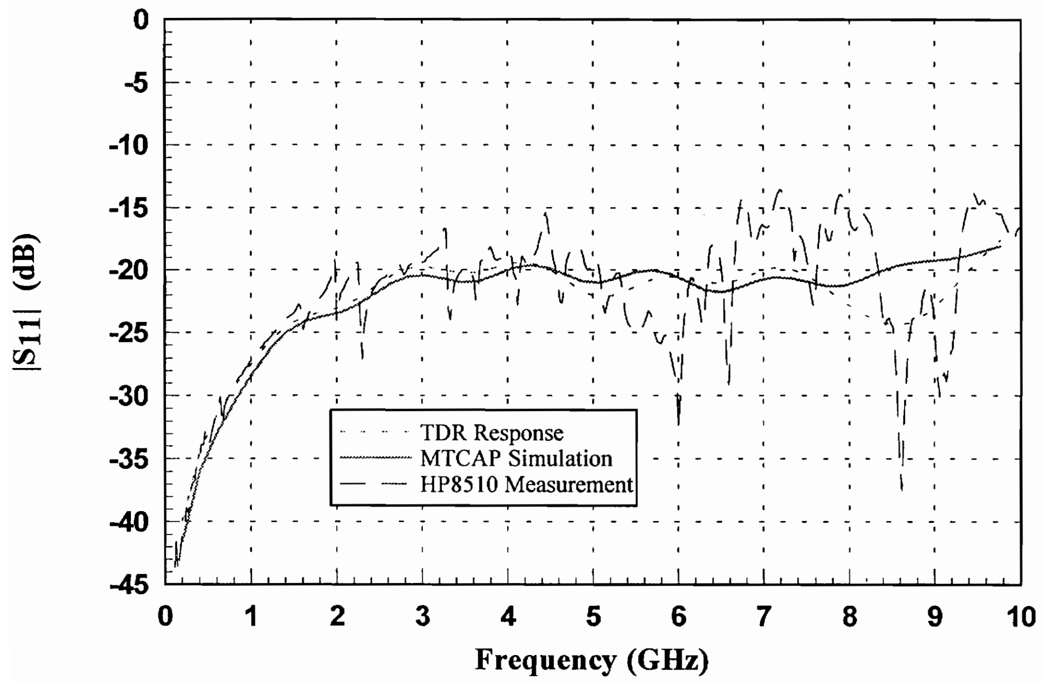

Figure 3.15 Comparison of $|S_{11}|$ for Package B

3.5 Conclusion

The purpose of this work was to use time domain network analysis and synthesis methods in order to derive an equivalent circuit for two distinct surface mount packages. These equivalent circuits derived were physically based circuit models having both a time domain and frequency domain match. In order to perform this work, time domain reflectometry (TDR) methods were used to acquire step response waveforms of each structure. From these waveforms, the MTCAP simulation package was used to derive an equivalent circuit model to represent the structures. The simulated waveform and the acquired TDR waveform were then run through an FFT algorithm to find the frequency domain equivalent. This frequency domain representation of the waveforms was then used to develop computed $|S_{11}|$ waveforms to compare to the actual waveforms measured directly from the HP8510 Network Analyzer. It can be seen from both Figure 3.14 and Figure 3.15 that this methodology has proven to be effective at the derivation of equivalent networks for a variety of structures, with time domain errors in the millivolt range and frequency domain errors of the order of a few dBs.

Chapter 4

Results and Conclusion

4.1 Conclusions

In the electronics packaging industry, there is a constant demand for smaller packages that operate at higher frequencies with a greater power dissipation. In order to meet these new demands, the industry developed the surface mount package. With the smaller leads of the surface mount package, the parasitics were minimized at lower frequencies in a smaller package with the same number of pins as a conventional DIP (dual in-line package). It should also be noted that DIPS were of no use in thick film hybrids, which do not allow for the through-hole technology of the DIP package. As technology progresses towards wireless electronics, the frequencies at which these small packages are required to operate increases, as does the lead count for these packages. Upon an increase in the circuit complexity, one needs to address the parasitics problem. The problems that parasitics create are many, from changing the fundamental frequency of operations of amplifiers to changing the gain of these amplifiers through the entire passband by decibels. It is also true, however, that these parasitics can be recognized, measured, explained, and even compensated for in a given circuit design. That was the focus of this work; to find, measure, explain, and characterize the parasitics associated

with two specific packages. Through the work in this thesis, a process for developing models for packaging parasitics for any type of package has been developed. This methodology has proven in the cases of these two packages to be accurate, as the frequency domain comparisons illustrated.

4.2 Future Work

Future work in this area can consist of testing different structures within the SOIC package. The structures that should be considered are fused lead and batwing packages. These packages can also be tested with a thermal slug to find the effects of the lead frame and slug on ground return. It is also desirable to measure different lengths of bondwires to develop a more accurate model for the bonds.

Steps may be taken in order to refine the experiment and methodology described in this thesis work. In future work, it would be desirable to construct a test fixture having a larger usable range. The test fixture used in this work was usable up to a frequency on the order of 6 GHz. Future work can also focus on using more advanced time domain calibration techniques to obtain a more accurate time domain model.

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VITA

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