OPTIMIZED DESIGN AND ANALYSIS OF A VOLTAGE-FED, PUSH-PULL, AUTOTRANSFORMER BATTERY DISCHARGER FOR THE NASA SPACE PLATFORM

by

Scott W. Deuty

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APPROVED:

Fred C. Lee  
F. C. Lee, Co-Chairman

Bo H. Cho  
B. H. Cho, Co-Chairman

Dan Chen  
D. Y. Chen

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Committee Co-Chairmen: Dr. F. C. Lee and Dr. B. H. Cho

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(ABSTRACT)

A contract was awarded to the Virginia Power Electronics Center to compare two battery discharger topologies for use on the Earth Observing System. The following report is the result of the optimal design, build and test of Voltage-Fed, Push-Pull Autotransformer battery discharger topology.

The main thrust of this document is to achieve an optimal efficiency. The list of available parts is restricted to only those that are approved. Derating guidelines restrict the choice of power stage semiconductors in a manner that degrades efficiency so efficiency gains are sought by optimization of the power stage magnetics. A second goal of the design is to achieve optimal small and large signal performance.
Acknowledgements

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To my friends at VPEC, I will always remember you. Erik Kvalheim and Lori Gomezperalta are the people my wife and I spent the majority of time with here in Blacksburg. We did everything together from wallyball to camping to using them as guinea pigs to try out new recipes. I wish them well in their upcoming marriage. I will also remember Karen Wilburn and how her stories about her three children and sense of humor allowed me to escape the pressures of graduate school. I spent many hours on the wallyball court with the remaining wallyball crew of C. S. Mitter, Tom Sizemore, Steve Shulz, Sahibul Islam, Richard Farrington, John Eng, and Jon Sahaydak. Our Friday night episodes were a lot of fun. Gone but not forgotten are Sayeed Ahmed, Jeff Boylan, and
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Dedication

This document is dedicated to my wife Elizabeth for her complete and trusting faith in me. She gave up a lot in order for me to return to school. Many times the pressure and living situation caused me to be a difficult person to live with but she rarely complained. She shouldered all of the financial and daily chores in order to free up my time for research. The depressing job market in Montgomery County coupled with the lack of social interaction made this a long and difficult stay for her. We went through some difficult times together during our stay here including one time that neither of us could walk for one week due to back injuries. She also endured a difficult knee operation. I am really anxious to graduate and give her all that I have promised over the last two years.
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1. INTRODUCTION

As a part of the Global Change Research Program, NASA has initiated an Earth Observing System (EOS) to monitor the ever changing environment. An important part of the EOS is a polar-orbiting platform. The power supply for this platform and the relative bus voltages are themselves an object of research.

A team of graduate engineers at the Virginia Power Electronics Center (VPEC) performed the research on the power system for the project (called NASA Space Platform). A specific task was to investigate one of two possible battery discharger topologies.

These electronic modules use an input voltage from a battery and provide a regulated bus voltage for the instrumentation of the Space Platform. The load of the battery discharger ranges on the order of zero to two kilowatts while the input voltage of the battery itself varies over a limited range of 53 to 84 Vdc.

The following thesis summarizes the design and analysis for one battery discharger topology.
1.1 Battery Discharger Topology Selection

The specifications for the battery discharger studied are given in Table 1.1. Based on these specifications, an in-depth study for the selection of an optimum topology was performed in [1] by comparing a simple boost converter, a voltage-fed push-pull autotransformer (VFPPAT) and a multi-module boost converter.

The main focus of [1] was to optimize the battery discharger for efficiency, weight and dynamic characteristics by using a computer-based electronic spreadsheet program to figure the power loss of each converter. By plotting weight vs. frequency for curves representing efficiencies of 95%, 96%, and 97%, an optimal topology was determined. The results show that the multi-module boost converter is an optimal battery discharger topology in terms of efficiency. The VFPPAT topology was a viable option for the battery discharger. A project research grant from NASA was awarded to the VPEC to further investigate the findings of [1].

Two power converter topologies were considered for the research program of the battery discharger for the Space Platform. These include a four-module boost converter (FMBC) shown in Figure 1.1, and a VFPPAT shown in Figure 1.2. This document reports on the optimization of the design, methods of the build and analysis of the test results of the VFPPAT topology. First, however, a brief comparison of the two topologies is presented.
**Table 1.1 Battery Discharger Design Specifications**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage Range</td>
<td></td>
</tr>
<tr>
<td>Optimal Performance Range</td>
<td>64 Vdc to 84 Vdc</td>
</tr>
<tr>
<td>Regulation Range</td>
<td>53 Vdc to 84 Vdc</td>
</tr>
<tr>
<td>Output Voltage Range</td>
<td>120 Vdc ± 4%</td>
</tr>
<tr>
<td>Output Voltage Ripple</td>
<td>200mV peak-to-peak</td>
</tr>
<tr>
<td>Output Power Range</td>
<td>0 W to 1800 W</td>
</tr>
<tr>
<td>Output Current Range</td>
<td>0 Amps to 15 Amps</td>
</tr>
<tr>
<td>Input Current Ripple</td>
<td>250 mA peak-to-peak</td>
</tr>
<tr>
<td>Switching Frequency</td>
<td>40 kHz</td>
</tr>
<tr>
<td>Efficiency Goal</td>
<td></td>
</tr>
<tr>
<td>(low line = 64 Vdc, high load = 15 Amps)</td>
<td>96 %</td>
</tr>
<tr>
<td>Transient Performance</td>
<td></td>
</tr>
<tr>
<td>Output Voltage Peaking Range</td>
<td>115.2 Vdc - 124.8 Vdc</td>
</tr>
<tr>
<td>Output Settling Time</td>
<td>10 msec</td>
</tr>
</tbody>
</table>
Figure 1.1 Power Stage Schematic and Waveforms of the Four Module Boost Converter
Figure 1.2 Power Stage Schematic and Waveforms of the Voltage-Fed, Push-Pull Autotransformer Converter
1.1.1 Four-Module Boost Converter (FMBC)

The FMBC topology offers several advantages. Boost topologies in general are current-fed and have continuous input current. Very little input ripple current exists because of the presence of the power inductor on the input. The FMBC offers an even lower current ripple by splitting the current into four modules which operate out of phase and multiply the ripple frequency to four times the switching frequency of 45 kHz. By sharing the output current among four modules, the current stress on any one switch is reduced.

The FMBC also exhibits some undesirable qualities. The four switches require a discrete pulse-width modulator (PWM), which splits the four phases for the FMBC and provides other PWM functions which are normally present on an integrated circuit (IC). The presence of these additional components increase parts count and therefore reduces reliability. However, reliability is enhanced for the FMBC because it can operate with only three phases functioning. Because the inductor resides on the input of the FMBC, the output will require filtering of the discontinuous diode current to meet output ripple specifications.

1.1.2 Voltage-Fed Push-Pull Autotransformer (VFPPAT)

The VFPPAT presents several advantages. The push-pull operation along with the non-isolated nature of the autotransformer allows for a single PWM chip to be used to directly drive the MOSFETs (whose source terminals connect to the same ground as the input, output, and PWM reference). Because the push-pull operation requires only two switches operating 180° out of phase, a PWM IC (such as the UC1825) can be used; this
is not the case for the FMBC with its four-phase PWM. The presence of the inductor on the output of this buck-derived converter allows for a continuous output current to flow over most of the power range. Peak-to-peak ripple current is less than for a boost converter, thus eliminating the need for an additional output filter stage.

Many of the disadvantages of the VFPPAT result from its buck-derived nature. A discontinuous input current will require filtering to meet the ripple current specification. In addition, this high current ripple will not allow an input capacitor with a high equivalent series resistance (ESR) value. By using low ESR, polypropylene capacitors, the capacitor ripple current rating will not be exceeded. Any imbalance in the transformer may cause "flux walking" to occur. This problem may damage the switching devices by allowing the transformer to saturate and pass large current through the drain. The use of current-injection control (CIC) insures flux walking does not occur by level detecting both the dc and ac portions of the transistor drain current.

Figure 1.2 shows the tapped version of the VFPPAT along with the resulting waveforms. These waveforms illustrate the push-pull nature of the converter. Figure 1.3 uses thick lines to show that each time a switch is gated ON, the diode connected to the opposing winding conducts. This provides a voltage of Vin to each primary on every other gating of the switch, and a primary voltage of zero when both switches are OFF. Because the switch transistors are operated 180° out of phase, the primary voltage is constantly reversed due to the polarity of the primaries, and complete flux balance will take place provided the circuit and waveforms are completely symmetrical.
a. Switch S1 ON (time t1, Figure 1.2)

b. Both Switches OFF (time t2, Figure 1.2)

c. Switch S2 ON (time t3, Figure 1.2)

(Note: Thick lines indicate conducting paths.)

Figure 1.3 VFPPAT Conduction Modes
By noting the applied voltages for times $t_1$, $t_2$, and $t_3$, the voltage across the inductor can be found as shown in Eqs. 1.1 and 1.2. Where $N$ is the turns ratio of one primary plus secondary (as shown in Figures 1.2 and 1.3).

$$VL_{ON} = (N + 1) \times Vin - Vo \quad (\text{either switch ON}), \text{ and}$$

$$VL_{OFF} = Vin - Vo \quad (\text{both switches OFF}).$$  \hspace{1cm} (1.1) \hspace{1cm} (1.2)

For steady state operation the flux for the ON-time of the inductor must equal the flux for the OFF-time. This phenomenon known as flux balance uses the switching period $T_s$ and the duty cycle at the inductor D (Note that the duty cycle of each switch is D/2) multiplied by the inductor voltage. Using the flux balance relationship the gain is found in equation 1.3.

Flux Balance: \hspace{1cm} \Delta \Phi_{ON} = VL_{ON} \times D \times T_s = \Delta \Phi_{OFF} = VL_{OFF} \times (1 - D) \times T_s \hspace{1cm} (1.3)

$$Gain = M = (Vo/Vin) = N \times D + 1$$  \hspace{1cm} (1.3)
1.2 Summary

An introduction of the battery discharger research for the Space Platform has been presented, and the operation of the topologies to be considered was discussed. The basic operation of the VFPPAT transformer has been presented, and the resulting gain was calculated. Thus the foundation for the design of the parameter values has been established.

The results of the trade-off study [1] determined that the FMBC and VFPPAT topologies would provide the efficiency and size needed for the Space Platform battery discharger. Of these two topologies, the VFPPAT provides a challenge to optimize the design such that the resulting efficiency and performance is comparable to that of the FMBC. The VFPPAT can be designed in a manner which may make it more reliable than the FMBC. Finally, by investigating all areas of the power stage of the VFPPAT, a valuable lesson in optimizing the performance of high power converter operation can be learned.
2. VFPPAT POWER STAGE DESIGN AND PARAMETER VALUE SELECTION

Establishment of the parameter values of the circuit components to meet the design specifications is performed along with choice of each component in accordance with the approved parts list [1]. The autotransformer turns ratio and inductor value are chosen first, and the resulting voltage and current levels are used to determined the remaining power stage components.

A limited number of flight approved semiconductors causes the design to rely on optimization of the power stage magnetics for achievement of the best efficiency. Therefore the semiconductors are chosen and the values of the magnetic components are determined in this chapter, and the magnetics design is detailed in Chapter 3.
2.1 General Power Stage Analysis

The design of the power stage is begun by calculating the maximum duty cycle and then choosing a value for the autotransformer turns ratio. The resulting voltage levels are then calculated.

**Autotransformer Turns Ratio and Converter Duty Cycle Range**

The establishment of the gain equation along with the input specifications listed in Table 1.1 allows the design stage to begin. By noting that the input voltage regulation range from Table 1.1 is 53-84 Vdc and the output voltage is 120 Vdc, both the duty ratio D and the turns ratio N (Fig. 1.2) can be chosen. The choice of D is based on the maximum duty cycle a typical PWM IC can produce at the switch (D/2). This value reaches a theoretical maximum of 50% for the chosen UC1825 PWM. However, when variables such as rise and fall times are considered, this value can safely be assumed to be a maximum of 45%. The maximum duty cycle will occur at low line (53 Vdc). By using the gain Eq. 1.3 The minimum turns ratio is determined as follows:

\[
N_{\text{min}} = \frac{(V_{\text{o}}/V_{\text{in}})_{\text{min}} - 1}{D_{\text{max}}} = \frac{(120V/53V) - 1}{0.9} = 1.405.
\]

Because this is a minimum value, N=1.5 was selected to accommodate for any drops in the semiconductors or other components. Also, 1.5 is favorable for winding the autotransformer because it allows for an integer number of turns to be wound for a complete set of conductors for all primaries and secondaries. The design then simply taps two series windings for a primary (autotransformer winding ratio of 1 in Fig. 1.2) and taps a third winding for the secondary giving a total of N=1.5.
The establishment of a turns ratio allows the duty cycle range of the converter to be calculated. This ratio is found by using Eq. 1.3 as follows:

\[
D_{\text{min}} = \frac{(V_o - V_{in_{\text{max}}} + V_{de})}{(V_{in_{\text{max}}} - V_{qe}) \times (N + 1) - V_{in_{\text{max}}}} = \frac{(120V - 84V + 1.5)}{(84V - 1.65V) \times (1.5 + 1) - 84V} = 0.31, \text{ and}
\]

\[
D_{\text{max}} = \frac{(V_o - V_{in_{\text{min}}} + V_{de})}{(V_{in_{\text{min}}} - V_{qe}) \times (N + 1) - V_{in_{\text{min}}}} = \frac{(120V - 53V + 1.5)}{(53V - 1.65V) \times (1.5 + 1) - 53V} = 0.91,
\]

where the voltage drops are assumed to be:

\[
V_{qe} = \text{estimated primary voltage drop} = 1.65 \text{ V, and}
\]

\[
V_{de} = \text{estimated secondary voltage drop} = 1.50 \text{ V.}
\]

The duty cycles calculated are twice the duty cycle seen by the switch. Therefore the duty cycles seen at the switch are as follows:

\[
D_{\text{switch, min}} = \frac{D_{\text{min}}}{2} = \frac{0.31}{2} = 0.155, \text{ and}
\]

\[
D_{\text{switch, max}} = \frac{D_{\text{max}}}{2} = \frac{0.91}{2} = 0.455.
\]

The maximum duty cycle of 0.46 is attainable with the UC1825 IC chosen for this design. This value is achieved using the dead-time capacitor calculation specified by the manufacturer’s data sheet, and it is calculated in Chapter 5.
**Power Stage Voltage Levels**

Voltage levels experienced by the power stage components can be determined by using Kirchoff's Voltage Law and Fig. 1.2. The voltage of the switch is equal to the input voltage or twice the input voltage when the opposing switch is OFF or ON, respectively and is given by Eq. 2.1:

\[
V_{ds(\text{opposing switch ON})} = 2V_{in}, \quad \text{and} \quad \tag{2.1a}
\]

\[
V_{ds(\text{opposing switch OFF})} = V_{in}. \tag{2.1b}
\]

Autotransformer primary voltage levels are equal to \(V_{in}\) when either switch is ON and zero when the switches are OFF as given by Eq. 2.2:

\[
V_{prim(\text{either switch ON})} = V_{in}, \quad \text{and} \quad \tag{2.2a}
\]

\[
V_{prim(\text{either switch OFF})} = 0. \tag{2.2b}
\]

Autotransformer secondary voltages are equal to the primary voltages through the turns ratio as shown in Eq. 2.3:

\[
V_{sec(\text{either switch ON})} = V_{prim} \times (N-1) = V_{in} \times (N-1) = 0.5V_{in}, \quad \text{and} \tag{2.3a}
\]

\[
V_{sec(\text{either switch OFF})} = \frac{V_{prim}}{(N-1)} = 0. \tag{2.3b}
\]

The voltage experienced by the inductor is established next (Eq. 2.4):

\[
V_{L(\text{switch ON})} = (N+1) \times V_{in} - V_{o} = 2.5V_{in} - V_{o}, \quad \text{and} \tag{2.4a}
\]

\[
V_{L(\text{switch OFF})} = V_{in} - V_{o}. \tag{2.4b}
\]

The reverse voltage on the diode occurs only when the adjacent switch is conducting as found using Eq. 2.5:

\[
V_{rr} = (V_{L} + V_{o}) - V_{in} \times (N + 1) = 2N \times V_{in}. \tag{2.5}
\]
Finally, the voltage levels of the input and output capacitors are simply the input and output voltage, respectively, as shown in Eqs. 2.6 and 2.7:

\[ V_{Ci} = V_{in}, \text{ and} \]
\[ V_{Co} = V_{o}. \]  \hspace{1cm} (2.6) \hspace{1cm} (2.7)

The resulting component voltage levels for low line and high line input voltages are shown in Table 2.1.
<table>
<thead>
<tr>
<th>Voltage Designation</th>
<th>Voltage Level Low Line (Vin = 53 Vdc)</th>
<th>Voltage Level High Line (Vin = 84 Vdc)</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{ds}(\text{opposing switch ON}) )</td>
<td>106.0 V</td>
<td>168.0 V</td>
</tr>
<tr>
<td>( V_{prim}(\text{either switch ON}) )</td>
<td>53.0 V</td>
<td>84.0 V</td>
</tr>
<tr>
<td>( V_{sec}(\text{opposing switch OFF}) )</td>
<td>26.5 V</td>
<td>42.0 V</td>
</tr>
<tr>
<td>( V_{L}(\text{either switch ON}) )</td>
<td>12.5 V</td>
<td>90.0 V</td>
</tr>
<tr>
<td>( V_{tr} )</td>
<td>159.0 V</td>
<td>252.0 V</td>
</tr>
<tr>
<td>( V_{Ci} )</td>
<td>53.0 V</td>
<td>84.0 V</td>
</tr>
<tr>
<td>( V_{Co} )</td>
<td>120.0 V</td>
<td>120.0 V</td>
</tr>
</tbody>
</table>
2.2 Power Stage Component Selection

Now that the voltage levels are known, the inductor value is determined, and the resulting peak current and root-mean-square (rms) current levels are then found. Based on these levels, the input and output capacitors and the semiconductor devices to be used for the switches and rectifiers are chosen.

2.2.1 Inductor

Inductor Value

The choice of an inductor value for the VFPPAT is related to many factors such as: ripple current, power loss, power level at which discontinuous operation begins, size, and weight. An optimization program was conducted [1] and the resulting value of 94 μH was chosen for optimal efficiency. The following discussion illustrates how the inductor value affects the output ripple current (for other factors in the optimization refer to [1]).

The presence of the inductor on the output of the converter is advantageous only if the peak-to-peak inductor current level can be kept to a minimum, thereby reducing the output ripple current and the ripple voltage produced by the capacitor ESR. The peak-to-peak inductor current is most affected by the applied voltage $V_L$, and by the duty cycle value (which was shown to be a function of the input voltage level in Eq. 1.1). Eq. 2.8 shows the peak-to-peak inductor current relationship to the voltage across the inductor:

$$\Delta I_L = \frac{V_L \times D}{2f \times L}.$$  \hfill (2.8)
The peak-to-peak inductor current will be greatest at high input voltage, where the applied inductor voltage will be 90 V as shown in Table 2.1. A plot of the ΔIL versus inductor values illustrates this relationship and provides insight into the optimized inductor value (Fig. 2.4). The inductor value of 94 μH chosen produces a relatively low peak-to-peak inductor current of 3.68 A which allows for a minimal output voltage ripple. This choice of inductance value will produce a respectable sized inductor with minimal gap loss as will be shown in the power loss analysis (Chapter 6).

\[
\Delta IL = \frac{90V \times 0.31}{2 \times 40kHz \times 94\mu H} = 3.68 \text{ A peak-to-peak}
\]
Figure 1.2 Peak-to-Peak Inductor Current vs. Inductance
**Inductor Current**

Now that the inductor value is determined, the peak and rms current levels are developed and values are presented. Because the load range has a minimum level of 0 A, the inductor current will have to become discontinuous at an output level between the specified 0 and 15 A. The output current level at which discontinuity occurs is half of the 3.68 A determined for Vin=84 Vdc earlier. Therefore discontinuous inductor current was chosen in [1] and occurs at 1.84 A dc load current or 216 W output power for Vin=84 Vdc. Maximum peak inductor current will occur at maximum load current as shown in Eq. 2.9:

\[
IL_{pk} = I_{load_{max}} + \frac{(\Delta IL_{max})}{2} = 15A + \frac{(3.68A)}{2} = 16.84\,A.
\]

(2.9)

**Remaining Power Stage Current Levels**

As shown in Fig 1.2, the primary of the autotransformer will experience three different waveform levels depending on whether the adjacent MOSFET switch is in the ON state, the opposite MOSFET is in the ON state, or both MOSFETs are OFF, as shown in Eq. 2.10. The peak primary current from Fig. 1.2 is the autotransformer turns ratio multiplied by the inductor current:

\[
ItI_{(S1\,ON)} = N \times IL = IsI, \text{ and}
\]

(2.10a)

\[
ItI_{(S2\,ON)} = IL, \text{ and}
\]

(2.10b)

\[
ItI_{(S1\,and\,S2\,OFF)} = \frac{IL}{2}.
\]

(2.10c)
Similarly, the diode currents will conduct the inductor current when the opposite switch is ON, no current when the adjacent switch is ON, and half the inductor current if both switches are ON, as shown in Eq. 2.11. Note that the secondary currents of the autotransformer are equal to the diode currents which are developed below:

\[ ID_{I(S1 \text{ ON})} = IL, \text{ and} \]  

\[ ID_{I(S2 \text{ ON})} = 0, \text{ and} \]  

\[ ID_{I(S1 \text{ and S2 OFF})} = \frac{IL}{2}. \]  

The input current is the sum of the two primary currents (I\text{t1} and I\text{t2}), and the capacitor current is the input current without the dc level, as shown in Eq. 2.12:

\[ ICI_{(\text{either switch ON})} = (I\text{t1} + I\text{t2}) - \frac{(N + 2) \times I_o}{2}, \text{ and} \]  

\[ ICI_{(\text{both switches OFF})} = IL - \frac{(N + 2) - I_o}{2}. \]  

The output capacitor will experience the peak-to-peak inductor current (ie. the ac portion of the inductor current) as shown in Eq. 2.13:

\[ ICo = \Delta IL. \]  

The peak current level values are presented in Table 2.2.
### Table 2.2 Peak Current Values of Power Stage Components

<table>
<thead>
<tr>
<th>Current Designation</th>
<th>Maximum Current Value</th>
<th>Maximum Current Value</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Low Line (Vin = 53 Vdc)</td>
<td>High Line (Vin = 84 Vdc)</td>
</tr>
<tr>
<td>$I_{sw_{peak}}$</td>
<td>23.6 A</td>
<td>25.3 A</td>
</tr>
<tr>
<td>$I_{prim_{peak}}$</td>
<td>23.6 A</td>
<td>25.3 A</td>
</tr>
<tr>
<td>$I_{sec_{peak}} = I_{D1_{peak}}$</td>
<td>15.8 A</td>
<td>16.8 A</td>
</tr>
<tr>
<td>$I_{L_{peak}}$</td>
<td>15.8 A</td>
<td>16.8 A</td>
</tr>
<tr>
<td>$I_{Co_{peak}}$</td>
<td>0.8 A</td>
<td>1.8 A</td>
</tr>
<tr>
<td>$I_{in_{peak}}$</td>
<td>42.1 A</td>
<td>39.4 A</td>
</tr>
<tr>
<td>$I_{Cl_{peak}}$</td>
<td>15.9 A</td>
<td>13.1 A</td>
</tr>
</tbody>
</table>
The rms current levels are based on the peak current levels which were developed in the previous section. The waveforms and time periods mentioned are illustrated in Fig. 1.2. Starting with the transformer the rms currents are shown in Eqs. 2.14 and 2.15:

\[
I_{prim_{rms}} = \sqrt{\frac{1}{T} \left( \int_{0}^{T} (ltl(t))^2 \, dt + 2 \int_{0}^{T} (ltl(t))^2 \, dt + \int_{0}^{T} (ltl(t))^2 \, dt \right)}, \quad \text{and} \quad (2.14)
\]

\[
I_{sec_{rms}} = \sqrt{\frac{1}{T} \left( 2 \int_{0}^{T} (ldl(t))^2 \, dt + \int_{0}^{T} (ldl(t))^2 \, dt \right)}. \quad (2.15)
\]

The rms current level as experienced by either switch is shown in Eq. 2.16:

\[
Isl_{rms} = Is2_{rms} = \sqrt{\frac{1}{T} \left( \int_{0}^{T} (ltl(t))^2 \, dt \right)}. \quad (2.16)
\]

The rms current level of the output inductor is found using Eq. 2.17:

\[
Il_{rms} = \sqrt{\frac{2}{T} \left( \int_{0}^{T} (ill(t))^2 \, dt + \int_{0}^{T} (ill(t))^2 \, dt \right)}. \quad (2.17)
\]

The output capacitor rms current is shown by Eq. 2.18:

\[
Ico_{rms} = \sqrt{\frac{2}{T} \left( \int_{0}^{T} (il(t) - io)^2 \, dt + \int_{0}^{T} (il(t) - io)^2 \, dt \right)}. \quad (2.18)
\]

Finally, the input capacitor current can be found using Eq. 2.19:

\[
Ici_{rms} = \sqrt{\frac{2}{T} \left( \int_{0}^{T} (ilt(t) + it2(t))^2 \, dt + \int_{0}^{T} (ilt(t) + it2(t))^2 \, dt \right)}. \quad (2.19)
\]

A summary of the expected power stage rms current levels is presented in Table 2.3.
Table 2.3 RMS Current Values of Power Stage Components

<table>
<thead>
<tr>
<th>Current Designation</th>
<th>Maximum Current Level</th>
<th>Maximum Current Level</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Low Line (Vin = 53 Vdc)</td>
<td>High Line (Vin = 84 Vdc)</td>
</tr>
<tr>
<td>$I_{sw_{rms}}$</td>
<td>15.2 A rms</td>
<td>8.9 A rms</td>
</tr>
<tr>
<td>$I_{prim_{rms}}$</td>
<td>18.3 A rms</td>
<td>11.1 A rms</td>
</tr>
<tr>
<td>$I_{sec_{rms}} = I_{D1_{rms}}$</td>
<td>10.2 A rms</td>
<td>6.7 A rms</td>
</tr>
<tr>
<td>$I_{L_{rms}}$</td>
<td>15.0 A rms</td>
<td>14.9 A rms</td>
</tr>
<tr>
<td>$I_{Co_{rms}}$</td>
<td>0.5 A rms</td>
<td>1.2 A rms</td>
</tr>
<tr>
<td>$I_{in_{rms}}$</td>
<td>36.1 A rms</td>
<td>24.4 A rms</td>
</tr>
<tr>
<td>$I_{Cp_{rms}}$</td>
<td>11.2 A rms</td>
<td>11.6 A rms</td>
</tr>
</tbody>
</table>
2.2.2 MOSFET Switch Transistors

The switching transistor will experience the following maximum voltage and current levels (from Tables 2.1, 2.2, and 2.3):

\[ V_{d_{\text{max}}} = 168.0 \text{ V}, \]
\[ I_{sw(\text{pk})_{\text{max}}} = 25.3 \text{ A peak}, \text{ and} \]
\[ I_{sw(\text{rms})_{\text{max}}} = 15.2 \text{ A rms}. \]

MOSFET switch transistors are approved for flight by NASA and will be used because implementation is easier and performance is better than for bipolar switch transistors. The MOSFET chosen for this design is the IRF350, an approved part. The data for this device is listed in Table 2.4.
<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{ds_{\text{max}}}$</td>
<td>400 V</td>
</tr>
<tr>
<td>$I_{d_{\text{max}}} (T_c=25^\circ \text{C})$</td>
<td>15 A Continuous</td>
</tr>
<tr>
<td>$I_{d_{\text{max}}} (T_c=50^\circ \text{C})$</td>
<td>11.6 A Continuous</td>
</tr>
<tr>
<td>$I_{d_{\text{max}}} (T_c=100^\circ \text{C})$</td>
<td>9 A Continuous</td>
</tr>
<tr>
<td>$I_{d_{\text{max}}}$</td>
<td>60 A (Repetitive Pulse)</td>
</tr>
<tr>
<td>$P_{d_{\text{max}}} (T_c=87^\circ \text{C}, T_j=105^\circ \text{C})$</td>
<td>72 W</td>
</tr>
<tr>
<td>$R_{ds_{\text{ON}}}$</td>
<td>$0.34 , \Omega \ (I_{ds}=20 , \text{A}, V_{gs}=15 , \text{V})$</td>
</tr>
<tr>
<td>$C_{iss_{\text{max}}} (V_{gs}=0, \text{V}, V_{ds}=50, \text{V}, f=1, \text{MHz})$</td>
<td>2000 pf</td>
</tr>
<tr>
<td>$C_{oss_{\text{max}}} (V_{gs}=0, \text{V}, V_{ds}=50, \text{V}, f=1, \text{MHz})$</td>
<td>200 pf</td>
</tr>
<tr>
<td>$C_{rss_{\text{max}}} (V_{gs}=0, \text{V}, V_{ds}=50, \text{V}, f=1, \text{MHz})$</td>
<td>50 pf</td>
</tr>
<tr>
<td>$V_{gs_{\text{max}}}$</td>
<td>$\pm 20 , \text{V}$</td>
</tr>
</tbody>
</table>
The derating guideline [2] requires the rated maximum transistor values be reduced to the following levels:

\[ V_{ds_{\text{max(derated)}}} = 75\% \times V_{ds_{\text{max}}} = 0.75 \times 400V = 300V, \]

\[ I_{d_{\text{max(derated)}}} = 75\% \times I_{d_{\text{max}}} = 0.75 \times 11.8A = 8.7A \left( T_C = 50^\circ C \right), \]

\[ P_{d_{\text{max(derated)}}} = 60\% \times P_{d_{\text{max}}} = 0.6 \times 72W = 43.2W \left( T_j = 105^\circ C \right), \text{ and} \]

\[ T_{j_{\text{max(derated)}}} = 60\% \times T_{j_{\text{max}}} = 0.6 \times 150^\circ C = 90^\circ C. \]

Each switch requires the use of two IRF350 MOSFETs in parallel for each switch. This will allow the derated continuous drain current requirement to be met by having each switch pass a drain current of 7.6 A rms, and, it will reduce the total ON resistance of the one switch leg to one-half of the 0.34 \Omega exhibited by the IRF350. This lowering of the switch ON resistance will reduce conduction loss.

The 400 V drain-to-source voltage rating (which is derated to 300 V) is the main reason for choosing this device, because it will allow the 168 V applied level to exist with some overshoot. Otherwise, a smaller device would be specified to reduce the parasitic capacitances and the ON resistance of the drain.

Paralleling MOSFETs is not without its problems, however. The output capacitance (\text{Coss}) is doubled when MOSFETs are paralleled, and problems can develop due to using devices with unequal parasitics, resulting in unsynchronized switching and/or unequal sharing of drain current. These problems have been solved through the use of a reliable drive scheme (Chapter 5) and careful circuit layout to reduce and equate parasitics.

The expected power dissipation due to conduction is:

\[ P_{Q1_{\text{ON(max)}}} = I_{d}^2 \times R_{d_{\text{ON}}} = \left( \frac{15.2 A \text{ rms}}{2} \right)^2 \times 0.34\Omega = 19.6 W. \]
The power dissipation of the device when it is ON should compare favorably with the derated 43.2 W at Tj=105° C when the switching losses are added (provided proper heat sinking is implemented).

2.2.3 Rectifier Diodes

Rectifier diodes are subject to the following voltage and current levels (from Tables 2.1, 2.2, and 2.3):

\[ V_{TR_{\text{max}}} = 252.0 \text{ V}, \]

\[ ID_{pk_{\text{max}}} = 16.8 \text{ A peak, and} \]

\[ ID_{rms_{\text{max}}} = 10.2 \text{ A rms.} \]

A check of the approved parts list [2] shows that no diodes can meet the required derated voltage and current levels. Initially the design was to use two 1N5816 diodes \( V_{TR_{\text{max}}} = 150 \text{ V} \) in series to handle the 252 V reverse voltage. This set of two diodes was to be paralleled so that each string would conduct half of the 10.2 A rms rectifier current \( ID_{avg_{\text{max}}} = 20 \text{ A} \). NASA determined that a failure of one of the series diodes could go undetected and was difficult to test for.

The next design chosen used UES706 diodes as a viable replacement. These diodes are rated for a reverse voltage of 400 V peak (which is derated to 325 V), an average forward current of 20 A each (which is derated to 60% provided the junction temperature stays below \( T_D \)), and a peak forward current of 300 A for 8.3 msec. The temperature \( T_D \) is found from the derating guideline [2] to be:

\[ T_D = T_{j(\text{derated})} - (\text{Derating Factor}) \times (T_{j(\text{max})} - T_M), \]

\[ T_D = 60\% \times 105^\circ \text{ C} - 60\% \times (105^\circ \text{ C} - 90^\circ \text{ C}) = 54^\circ \text{ C}. \]
The maximum temperature of the case should remain around 50° C, which is the heat sink temperature. Therefore the junction temperature will be more than 54° C, and the diodes will have to be paralleled to meet the current specification. Paralleling the diodes will reduce the power loss due to the forward voltage drop. These rectifiers will not have to be put in series to meet the applied reverse voltage. However, ringing will have to be kept to less than a 325 V peak. The UES706 diodes are available in a D0-4 package and must meet final approval for space flight. The number of these diodes required will be half of the number of 1N5816 diodes, therefore increasing mean time between failure (MTBF) and reliability.

2.2.4 Output Capacitor

The output capacitance value for the 120 V bus has been determined by NASA to be 2000 uf. However, fifteen to twenty-five feet of twisted, shielded, #10 AWG wire is between the converter and the output capacitor bank, making it necessary to have some capacitance placed at the converter output. The value chosen for the output capacitor was 10 uf. This value is low enough not to alter the final capacitance of the capacitor bank when the converters are paralleled, and high enough to support transients at the converter outputs.

For the test circuit, the output capacitor value of 10 uf was implemented using two 5 uf polypropylene capacitors with the following information:

<table>
<thead>
<tr>
<th>Part number</th>
<th>CFR13ALC505</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage rating</td>
<td>200 Vdc</td>
</tr>
<tr>
<td>ESR value</td>
<td>0.011 Ω</td>
</tr>
<tr>
<td>Maximum ripple current (Tc=85° C)</td>
<td>8.5 A rms.</td>
</tr>
</tbody>
</table>
These parts meet the applied rms current of 0.6 A each (Table 2.3) and can be used for the 120 V output provided the derating is not less than 50%. Note that although these capacitors were chosen for breadboard testing, their size is rather large when compared to other approved styles such as the M39006 series. The choice of another style for flight use may reduce the size and must have an ESR value and rms current rating compatible with the applied 1.2 A rms current.

2.2.5 Input Capacitor

The input capacitor has two restrictions placed on it by this topology. The rms input current is a maximum 11.6 A (Table 2.3), and the converter input impedance will need to see a rather low impedance from the input capacitor. For these reasons the input capacitor was chosen at 20 uf; it is composed of two 10 uf polypropylene capacitors in parallel. The information for these capacitors is as follows:

<table>
<thead>
<tr>
<th>Part Number</th>
<th>CFR14LLC106</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage Rating</td>
<td>200 Vdc</td>
</tr>
<tr>
<td>ESR Value</td>
<td>0.009 Ω</td>
</tr>
<tr>
<td>Maximum Ripple Current (Tc=85°C)</td>
<td>10.9 A rms.</td>
</tr>
</tbody>
</table>

The maximum rms current applied to each capacitor is 5.8 A. This value easily meets the rated level of 10.9 A rms. The maximum applied voltage of the input capacitor is 84 Vdc vs. a rated value of 200 Vdc.
2.3 Summary

Establishment of an autotransformer turns ratio and resulting duty cycles allowed the power stage voltage levels to be calculated and an inductor value to be determined. Power stage current levels were then determined, and components were chosen in accordance with the approved parts list [2].
3. POWER STAGE MAGNETICS

Chapter 2 established the required autotransformer turns ratio and inductor value for the VFPPAT power stage. This chapter will present the design considerations of the autotransformer and inductor. Optimization of these two components is crucial to the choice of the VFPPAT as the final battery discharger topology. The limitations set on the design by the power stage semiconductor devices and capacitors requires the design of efficient, light-weight magnetics for this topology to maintain a respectable efficiency and size. Select design equations are presented, as are measured and manufacturer’s data.
3.1 Autotransformer

The design of the autotransformer began by choosing a core based on an area product calculation. It proceeded to the design of the windings to fit the window area of the chosen core. The ultimate goal of the final design was to achieve a balance of power dissipation so that the winding and the core each account for half of the total autotransformer power loss.

3.1.1 Core Design

Calculation of the area product begins with basic magnetics equations (which are derived from Faraday’s law and Ohm’s law). From Faraday’s law, the law of flux balance can be stated as shown in Eq. 3.1, where $Ae$ is the effective area of the core, $\Delta B$ is the flux excursion, $V_{\text{eff}}$ is the voltage applied to the primary, and $B_{\text{max}}$ is the maximum flux density of the core material:

$$V_{\text{eff}} = \frac{Np \times \Delta \Phi}{\Delta T} = \frac{Np \times \Delta B \times Ae \times f}{0.5 \times D} = \frac{Np \times 2B_{\text{max}} \times Ae \times f}{0.5 \times D}. \quad (3.1)$$

The flux density usage of the H7C4 material is illustrated in Fig. 3.1.
$\Delta B = 0.4 \text{ Tesla}$

$B = 0.2 \text{ Tesla max}$

Figure 3.1 Flux Density Usage of TDK H7C4 Material
The choice of a core will be based on the area product \((Ap = Ae Aw)\) value of the core where \(Aw\) is the window area of the core. Solving for the effective area Eq. 3.1 becomes Eq. 3.2:

\[
Ae = \frac{Vp \times D}{4 \times Np \times B_{max} \times f} = \frac{(Vin - Vqe) \times D}{4 \times Np \times B_{max} \times f}.
\]  

(3.2)

To find the area of the window, the area of the windings \((Wra)\) must be determined from the area of the primary \((Ap)\), the area of the secondary \((As)\), and the assumed current density \((J = 300 \ A/m^2)\) using Eq. 3.3.

\[
Ap = \frac{Itprim_{rms}}{J},
\]  

(3.3a)

\[
As = \frac{Itsec_{rms}}{J}, \text{ and}
\]  

(3.3b)

\[
Wra = 2 \times (NpAp + NsAs) = 2 \times \frac{NpItprim_{rms} + NsItsec_{rms}}{J}.
\]  

(3.3c)

The winding is assumed to use about forty percent of the window area; therefore, the window utilization factor \(Ku\) is set to 0.4, and Eq. 3.4 is used to solve for the area of the window \((Aw)\):

\[
Aw = \frac{Wra}{Ku} = 2 \times \frac{NpItprim_{rms} + NsItsec_{rms}}{J \times Ku}.
\]  

(3.4)

By using the autotransformer turns ratio \(N\) and combining equations 3.2 and 3.4 into Eq. 3.5, the minimum area product in \(m^4\) is determined:

\[
Ap = Ae Aw = \frac{(Itprim_{rms} + (N - 1) \times Itsec_{rms}) \times D \times Vp}{Ku \times 2B_{max} \times f \times J}.
\]  

(3.5)

By operating H7C4 ferrite material by TDK corporation at a conservative maximum flux density of 0.2 Tesla (Fig. 3.1), the value of the area product is found to be \(5.759 \times 10^8 \ m^4\).
\[ Ap = \frac{(18.3A + (1.5 - 1) \times 10.2A) \times 0.91 \times 51.35V}{40\% \times 2 \times 0.2\text{Tesla} \times 40\text{kHz} \times 300 \frac{A}{m^2}}, \quad \text{and} \]

\[ Ap = 5.759 \times 10^{-8} \text{ m}^4 = 5.759 \times 10^4 \text{ mm}^4. \]

Several transformer designs were attempted based on the required area product of 5.759 x 10^4 mm^4. Initially a TDK PQ40/40 core with an area product of 6.55 x 10^4 mm^4 was chosen. However, it was determined that a TDK ETD44 core with an area product of 5.334 x 10^4 mm^4 would provide similar performance and would be easier to wind. The actual benefits of choosing this core will become apparent in the following sections. The TDK information [3] on the two cores is provided in Table 3.1 for reference during the design of the windings.
Table 3.1 Autotransformer Core Data
(Source: TDK Ferrite Cores Catalog [3])

<table>
<thead>
<tr>
<th>Parameter</th>
<th>ETD44 Core</th>
<th>PQ 40/40 Core</th>
</tr>
</thead>
<tbody>
<tr>
<td>Effective Core Area (Ae)</td>
<td>175 mm²</td>
<td>201 mm²</td>
</tr>
<tr>
<td>Window Area (Aw)</td>
<td>305 mm²</td>
<td>326 mm²</td>
</tr>
<tr>
<td>Area Product (Ap)</td>
<td>57590 mm⁴</td>
<td>65530 mm⁴</td>
</tr>
<tr>
<td>Core Volume (Ve)</td>
<td>18000 mm³</td>
<td>20450 mm³</td>
</tr>
<tr>
<td>Inductance/turns² (AL)</td>
<td>4000 nH/N²</td>
<td>4300 nH/N²</td>
</tr>
<tr>
<td>Maximum Foil Width (FW)</td>
<td>1.0 &quot;</td>
<td>1.0 &quot;</td>
</tr>
</tbody>
</table>
3.1.2 Windings Design

Because of the desire to optimize the autotransformer design, an evaluation of several types of windings was performed and the resulting design equations are presented. Windings considered for the autotransformer include Litz wire, standard transformer wire, and copper foil. Each type of winding has several advantages and disadvantages.

**Litz Wire**

Litz wire is normally used for high-frequency power converters with switching frequencies on the order of 200 kHz and higher. The design of Litz wire reduces loss due to the skin effect at these higher frequencies. It also is a stranded wire which is much more flexible than standard transformer wire. The manner in which Litz wire is insulated does not allow for the conductor to comprise as great of a percentage of the window as standard transformer wire or copper foil. Due to the VFPPAT switching frequency of 40 kHz and lower percentage of the window used by the copper, Litz wire was not used for this design.
Standard Transformer Wire

Standard transformer wire offers excellent coupling properties along with the effective use of the core window. However, the rms currents the primary and secondary windings carry cause the required diameter of the transformer wire to be large in order to meet the targeted current density value of $J = 300 \, \text{A/m}^2$. The use of several twisted wires of a reduced diameter will reduce losses due to the skin effect while still achieving the desired current density. However, this method does reduce the effective use of the window because of the additional insulation of several twisted wires vs. for one wire. In addition, the twisted wire can never be wound tightly enough to occupy the same amount of space as a single wire. Physically, the friction created while twisting and winding the twisted bundle of wires stresses the insulation to a point that may jeopardize reliability.

Two autotransformers were built using the twisted wire method with three #18 AWG wires and one #18 AWG wire used for the primary and secondary, respectively. This configuration did allow for a design with a respectable power loss of the winding. However, the physical implementation of a standard transformer wire design required the core window size to increase, and the design reverted from a PQ40/40 core to a PQ50/50 core. By using the larger core, the design did not achieve the desired balance of power loss between the core and winding. The added core size and difficulty of physical implementation of the windings caused the use of the standard transformer wire to yield to the use of foil windings in the autotransformer.

Foil Windings

When wound correctly, foil windings allow for the most effective use of the core window. The coupling of foil windings is not as effective as standard transformer windings since foil must be wound in layers, therefore increasing the distance of the outer windings from the center leg of the core. Also, the act of layering the foil can cause a design to exhibit larger winding capacitance than for the use of either wire style.
Physically the tapping of the windings for a foil autotransformer can create problems and cause the design to favor physical considerations in place of electrical characteristics. For example, the tapping may require two windings to be adjacent to each other even though the arrangement does not provide the most desirable coupling for the windings. Problems like this can lead to a transformer imbalance, which can cause flux walking or transmission of the 40 kHz switching frequency to the output as an undesired harmonic.

Copper foil is available in various thicknesses using the units of mils (0.001") and widths in integer values of inches (1", 2", etc.). The best method to insulate foil is to use capton tape, which is available in widths based on integer units of inches. This creates an insulating problem by not allowing the tape to extend beyond the foil enough to electrically insulate it. Capton tape can be ordered in custom widths, but the required minimum orders result in a great expense and a large amount of unused stock. A solution is to reduce the foil width, which decreases the cross sectional area of the copper and raises its resistivity and increases the windings losses. A second solution of overlaying the tape was implemented even though it increased the amount of window area taken up by the tape and therefore reduced the amount of window area the copper foil could use.

Foil windings were determined to be the most effective for the autotransformer design. Many of the problems associated with the use of foil windings can be solved by careful use of insulating and winding methods. The most desirable foil width is one inch. Both of the cores chosen thus far can accommodate a foil width of one inch (FW = 1").
**Autotransformer Windings Design Equations**

The final autotransformer design is shown in Fig. 3.3. To calculate the number of primary windings \((N_p)\), Eq. 3.2 is rearranged and the result is rounded to the next highest even integer (even integers assure the secondary can be wind in full turns rather than fractional turns). This calculation is performed using the ETD44 data from Table 3.1:

\[
N_p = \frac{D_{\text{max}} \times V_p}{\Delta B \times A_e \times 2f} \times 10^6 = \frac{0.91 \times (53V - 1.65V) \times 10^6}{0.4\,\text{Tesla} \times 175\,\text{mm}^2 \times (2 \times 40\,\text{kHz})} = 8.4\,\text{Turns}.
\]

Rounding 8.4 to the next highest even integer results in the number of primary turns being \(N_p=10\) turns. Eq. 3.2 is rearranged to verify that the number of primary turns will not cause the transformer to exceed the desired flux excursion of 0.4 Tesla:

\[
\Delta B = \frac{D_{\text{max}} \times V_p}{N_p \times A_e \times 2f} \times 10^6 = \frac{0.91 \times (53V - 1.65V) \times 10^6}{10T \times 175\,\text{mm}^2 \times (2 \times 40\,\text{kHz})} = 0.335\,\text{Tesla}.
\]

After determining the flux excursion to be appropriate with \(N_p=10\) turns, it is a simple manner to determine the number of secondary turns \(N_s\):

\[
N_s = N_p \times (N - 1) = 10T \times (1.5 - 1) = 5\,\text{turns}.
\]

With the number of primary and secondary windings determined for optimal core operation, all that remains is to calculate the foil thickness, number of foil strips to use in parallel, and the resulting window utilization factor \((K_{u\text{actual}})\). The use of one 5 mil foil winding \((F1Th = 0.005")\) was determined to be optimal for the primary and the secondary. The skin effect will not be present since the skin depth will be greater than 5 mils. Note that the thickness of the capton tape used to insulate the windings is approximately 1.5 mils \((TpTh = 0.0015")\). Window usage was calculated to be an achievable 41.2%:
Total Foil Area \(= 2 \times (FtTh + TpTh) \times (Np + Ns) \times FW\),

Total Foil Area \(= 2 \times 0.0065'' \times 15\text{Turns} \times 1'' = 0.195 \text{ sq in}, \) "and

\[ K_n_{\text{actual}} = \frac{TWA \text{ sq inches}}{Aw \text{ mm}^2} \times 645.16 = \frac{0.195 \text{ sq inches}}{305 \text{ mm}^2} \times 645.16 = 0.412. \]

3.1.3 Autotransformer Measured and Performance Testing Results

The choice of the TDK ETD44 core with the 5 mil foil used for the windings resulted in the autotransformer parameters shown in Table 3.2. An initial comparison of the efficiency of the VFPPAT converter was performed for each of the autotransformers which were wound. This comparison, along with the description of the four transformers, is presented in Fig. 3.2. The results show the foil design using the ETD44 core provides the best converter efficiency. These results directed the study towards pursuing the foil/ETD44 core as the autotransformer of choice for the VFPPAT battery discharger topology.
Table 3.2 Autotransformer Parameter Values
(ETD44 Core, 5 mil foil, Np=10 turns, Ns= 5 turns)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Measured Value (40 KHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Primary Inductance (Magnetizing Inductance)</td>
<td>472 uH</td>
</tr>
<tr>
<td>Secondary Inductance</td>
<td>117 uH</td>
</tr>
<tr>
<td>Primary Leakage Inductance</td>
<td>220 nH</td>
</tr>
<tr>
<td>Secondary Leakage Inductance</td>
<td>117 nH</td>
</tr>
<tr>
<td>Primary Capacitance</td>
<td>11 nf</td>
</tr>
<tr>
<td>Secondary Capacitance</td>
<td>5.5 nf</td>
</tr>
<tr>
<td>Primary DCR</td>
<td>4 mΩ</td>
</tr>
<tr>
<td>Secondary DCR</td>
<td>2 mΩ</td>
</tr>
</tbody>
</table>
Figure 3.2 VFPPAT Efficiency Measurements Comparing Four Autotransformers
3.2 Inductor

The inductance value used by the VFPPAT was chosen to be 94 uH in Chapter 2. The inductor core choice and the windings design are performed in this section. As with the autotransformer, design equations are presented, and the inductor parameters are then calculated.

The core type considered for this design is the Magnetics, Inc. MetGlas class of cut "C" cores. These cores were chosen initially for their high saturation flux density. In addition, the low ac flux of the VFPPAT design will prove beneficial when determining the amount of power dissipated in the air gap.

Due to the desire to use one inch wide foil windings in the inductor, cores that accommodate this foil width were sought. After initial consideration of power handling capability and manufacturer's data, the core chosen was the MetGlas MC0007 cut "C" core. The data for this core is presented in Table 3.3.
### Table 3.3 Inductor Core Data
(Magnetics Inc. MetGlas Cut "C" Core # MC0007)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Parameter Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Effective Core Area (AeL)</td>
<td>0.43 cm²</td>
</tr>
<tr>
<td>Window Area (AwL)</td>
<td>2.028 cm²</td>
</tr>
<tr>
<td>Area Product (ApL)</td>
<td>0.872 cm⁴</td>
</tr>
<tr>
<td>Core Volume (VeL)</td>
<td>3.526 cm³</td>
</tr>
<tr>
<td>Stacking Factor</td>
<td>0.8</td>
</tr>
<tr>
<td>Maximum Foil Width (FWL)</td>
<td>1.0 &quot;</td>
</tr>
<tr>
<td>Saturation Level (Begins)</td>
<td>0.6 Tesla</td>
</tr>
<tr>
<td>Saturation Level (75% Permeability)</td>
<td>1.1 Tesla</td>
</tr>
<tr>
<td>Saturation Level (Hard Saturation)</td>
<td>1.6 Tesla</td>
</tr>
<tr>
<td>Core Loss (1.1 Tesla, 80kHz)</td>
<td>50 Watts/lb</td>
</tr>
<tr>
<td>Weight</td>
<td>0.077 lbs.</td>
</tr>
<tr>
<td>Power Handling</td>
<td>0.025 in.⁴</td>
</tr>
</tbody>
</table>
The important parameter in determining the core effectiveness is the flux density level, $BL_{\text{max}}$. To calculate this value the area of the winding $WraL$ must first be calculated. By assuming two 2 mil foil strips will be 7 mils thick when insulated with capton tape and by assuming the winding can use 75% of the window with bobbin in place, the winding area is calculated in Eq. 3.6 (where 6.5416 scales inches to cm):

$$WrL = \frac{\text{Winding Area}}{75\%} \times 6.5416,$$

and

$$WrL = \frac{0.007 \text{sq inches}}{0.75} \times 6.5416 = 0.061 \text{ cm}^2.$$

The maximum flux level $BL_{\text{max}}$ is calculated in Eq. 3.7:

$$BL_{\text{max}} = \frac{WrL}{ApL} \times \left( I_{\text{load}_{\text{max}}} + \frac{VL_{\text{max}} \times D_{\text{min}}}{4L \times f} \right) \times L \times 10^4,$$

and

$$BL_{\text{max}} = \frac{0.061 \text{ cm}^2}{0.872 \text{ cm}^3} \times \left( 15A + \frac{90V \times 0.31}{4 \times 90uH \times 40KHz} \right) \times 94uH \times 10^4 = 1.11 \text{ Tesla}.$$

The maximum flux density level of 1.1 Tesla is within the capability of the core material. Tests showed the inductor would saturate at 20 A of dc current, therefore, the peak inductor current of 16.8 A from Table 2.2 should not jeopardize operation of the inductor.

Using the equation provided by the manufacturer, the power handling capability is determined (Eq. 3.8). The resulting value of 0.0264 in$^4$ is near the core value of 0.025 in$^4$ from Table 3.3:

$$Power \ Handling = \frac{13 \times V_o \times I_{\text{load}_{\text{max}}}}{10 \times BL_{\text{max}} \times 2f},$$

and

$$Power \ Handling = \frac{13 \times 120V \times 15A}{10 \times 1.1 \text{Tesla} \times 2 \times 40KHz} = 0.0264 \text{ inches}^4.$$
To determine the number of turns for the inductor winding (NL), Eq. 3.9 and \( I_{\text{peak}} \) from Table 2.2 are used:

\[
NL_{\text{max}} = \frac{IL_{\text{peak}}}{BL_{\text{max}} \times AeL \times 10^{-4}} \times L, \text{ and} \tag{3.9}
\]

\[
NL_{\text{max}} = \frac{16.8A}{1.1\text{Tesla} \times 0.43cm^2 \times 10^{-4}} \times 94\mu H = 34 \text{ turns}.
\]

Eq. 3.9 is rounded to the next highest integer value. Physically the design is able to accommodate thirty-two turns (\( NL_{\text{actual}} = 32 \text{ turns} \)) of the parallel 2 mil copper strips insulated with capton tape.

The gap needed to produce an inductance value of 94 \( \mu \)H is determined by Eq. 3.10. The results are rounded to the integer value of 24 mils. The nature of the cut "C" core requires insertion of 12 mils of paper in each gap to achieve the required gap of 24 mils:

\[
l_g(mils) = \frac{0.4 \times \pi \times (NL)^2 \times AeL \times 10^{-4}}{2.54 \times L} \times 0.1, \text{ and} \tag{3.10}
\]

\[
l_g(mils) = \frac{0.4 \times \pi \times (32T)^2 \times 0.43cm^2 \times 10^{-4}}{2.54 \times 94\mu H} \times 0.1 = 24 \text{ mils}.
\]

The inductor was built and tested, and the resulting parameters are presented in Table 3.4. The actual inductance value was approximately 100 \( \mu \)H, and the device performed well. Therefore the design was considered successful.
Table 3.4 Power Inductor Parameter Values
(Core: MC007 Magnetics Inc. Cut "C" Core, 24 mil gap)
(Winding: Two-2 mil foil strips in parallel, NL = 32 turns)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Measured Value</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>(80 Khz)</td>
</tr>
<tr>
<td>Inductance (No DC Current Applied)</td>
<td>100 uH</td>
</tr>
<tr>
<td>Inductance (0-20 A of DC Current Applied)</td>
<td>100 uH</td>
</tr>
<tr>
<td>DCR</td>
<td>23 mΩ</td>
</tr>
</tbody>
</table>
3.3 Summary

Design optimization of the magnetics was performed, and the resulting measured parameters of the autotransformer and power inductor were presented. The final schematic of the magnetics is presented in Fig. 3.3. All power stage components have been determined, and the resulting power stage schematic is presented in Fig. 3.4.
Ns = 5 turns, 5 mil foil

Np = 10 turns, 5 mil foil

Core: TDK ETD44

Np = 10 turns, 5 mil foil

Ns = 5 turns, 5 mil foil

Key
Internal Tap = Short Line
External Lead = Long Line

a. Autotransformer

Core: Magnetics Inc. Cut "C" Core #MC0007

Windings: 32 turns of two 2 mil foil strips in parallel

b. Inductor

Figure 3.3 Power Stage Magnetics Schematics
Figure 3.4 Final Power Stage Schematic
4. INPUT FILTER

The completion of the power stage design requires that an input filter be considered before the control loop is addressed in order to compensate for any interaction between the converter and filter.
4.1 Input Filter Design

The VFPPAT topology is buck-derived and therefore, has a high peak-to-peak input current value which is given by equation 4.1 (using values from Table 2.2):

\[ I_{in_{p-p}}(\text{max}) = I_{\text{prim}_{\text{peak}}} - (I_{\text{load}_{\text{max}}} - (I_{L_{\text{peak}}} - I_{\text{load}_{\text{max}}})) \]  \hspace{1cm} (4.1)

\[ I_{in_{p-p}}(\text{max}) = 42.1Apk - (15Adc - (15.8Apk - 15Adc)) = 29.7 \text{ A } p-p \]

The specified input current ripple is 250 mA peak-to-peak. In view of the large difference between specified and actual input current, it is obvious that an input filter is needed to attenuate the ripple current. The amount of attenuation (IFA\text{atten}) is calculated as follows:

\[ IFA\text{atten} = 20 \times \log \left( \frac{27.9A_{p-p}}{250mA_{p-p}} \right) = 41 \text{ dB} \]

This 41 dB attenuation will have to take place at the inductor switching frequency of 80 kHz. The large amount of attenuation required of the input filter could result in substantially large filter components that could jeopardize the choice of the VFPPAT for the battery discharger topology. Therefore it is necessary to optimize the filter design for performance and size. Several methods of filtering were investigated. Reference [5] provided insight into reducing the task of filter design, and as a result, a two section filter was chosen. The two-stage filter used is shown in Fig. 4.1.
L1 = 10 \, \text{uH}, \, L2 = 2 \, \text{uH}, \, R = 0.6, \, C1 = 100 \, \text{uf}, \, \text{and} \, C2 = 20 \, \text{uf}

Figure 4.1 Input Filter Schematic
The gain of the filter is found by analysis of the impedances of the components, and the result is reproduced in Eq. 4.2:

\[
Gain = \frac{1 + sRC1}{(1 + sRC1)(1 + s\frac{L1}{R})(1 + s\frac{L2}{R})(1 + sRC2)}.
\]  

(4.2)

Several assumptions on the relations of the component values reduces Eq. 4.2 to Eq. 4.3:

\[
Gain \approx \frac{1}{(1 + sRC2)(1 + s\frac{L2}{R})(1 + s\frac{L1}{R})}.
\]  

(4.3)

Assumptions:

\[C1 \gg C2, \quad L1 \gg L2, \quad \frac{L1}{R} \ll RC1, \quad \frac{L2}{R} \ll RC1\]

Pole Frequencies:

\[
\omega_1 = \frac{1}{RC2}, \quad \omega_2 = \frac{R}{L2}, \quad \omega_3 = \frac{R}{L1}.
\]

Thus, the methods used in [5] result in the input filter impedance approximation shown in Eq. 4.4:

\[
IFZ = \frac{sL1}{(1 + s\frac{L1}{R})(1 + sRC2)}.
\]  

(4.4)

The output impedance of the input filter must be less than the closed loop input impedance of the converter by a desired margin in order for the filter to work properly and to avoid interaction with the converter. At this stage the filter design is approximated. The closed loop input impedance of the converter will be verified later.
4.1.1 Component Values

The establishment of the filter characteristic can produce the desired Q if the position of the three poles is determined correctly. In order for proper damping to occur, the Q value must be around one. Positioning of the poles was determined by trial and error using a PSPICE program. Pole frequencies are shown below:

\[ f_1 = 13.26 \text{ kHz}, \]
\[ f_2 = 47.75 \text{ kHz}, \text{ and} \]
\[ f_3 = 9.55 \text{ kHz.} \]

This particular input filter requires that C1>C2, which allows the input capacitor value of C2=20 uf chosen in chapter 2 to remain. The large peak-to-peak current produced by the converter will be seen across C2, which is two low ESR polypropylene style capacitors in parallel. Had another filter style been chosen so that C2>C1, the implementation of a large C2 value would have made for several tantalum capacitors in parallel in order to meet rms current ratings. With the chosen filter C1>C2 requirement, C1 will see very little rms current due to the presence of L2, and C1 can be a tantalum style capacitor, thereby reducing the filter size.

Having determined the size of C2 and the amount of attenuation, the size of the damping resistor is determined by setting the corner frequency of R and C2 at the first corner frequency f1:

\[ R = \frac{1}{2\pi C_2 f_1} = \frac{1}{2\pi \times 20 \text{ uf} \times 13.26 \text{ kHz}} = 0.6 \Omega. \]

The second resonant frequency, f2, is based on the value of R and L2:

\[ L_2 = \frac{R}{2\pi f_2} = \frac{0.6 \Omega}{2\pi \times 47.75 \text{ kHz}} = 2 \text{ uH}. \]
The third resonant frequency, \( f3 \), is based on the value of \( R \) and \( L1 \):

\[
L1 = \frac{R}{2\pi f3} = \frac{0.6\Omega}{2\pi \times 9.55kHz} = 10 \text{ uH}.
\]

A check of the assumptions reveals that the component values are as desired by the approximation:

\[
C1 = 100\text{uf} \gg C2 = 20\text{uf}, \quad L1 = 10\text{uH} \gg L2 = 2\text{uH},
\]

\[
\frac{L1}{R} = 1.7 \times 10^{-5} \ll RC1 = 6 \times 10^{-5}, \quad \text{and} \quad \frac{L2}{R} = 3.3 \times 10^{-6} \ll RC1 = 6 \times 10^{-5}.
\]

The \( Q \) value can now be calculated from the chosen inductor values. As shown the \( Q \) value of 1.5 is near the value of 1 desired for optimal damping:

\[
Q = \left( \frac{L1}{L2} \right)^{\frac{1}{2}} = 4\sqrt{\frac{10\text{uH}}{2\text{uH}}} = 1.5.
\]

### 4.1.2 Component Selection

\( C1 \) will experience the entire input voltage range of 53 Vdc to 84 Vdc. As was mentioned earlier, \( C1 \) carries an insignificant amount of ripple current. Therefore, \( C1 \) was chosen based exclusively on the desired value and voltage rating. The style chosen for \( C1 \) was a tantalum CLR style capacitor which has a voltage derating of 50% of rated voltage. Therefore, the rated voltage will have to be twice the maximum input voltage or 168 Vdc minimum. The part chosen for the breadboard was rated at 250 Vdc.
The value of L1 was determined earlier to be 10 uH. Implementation of this design was performed using a Magnetics, Inc. MPP core #55071 with 13 turns of three #16 AWG transformer wires in parallel. The paralleling of transformer wires was the result of optimizing the power loss due to the dc resistance of the winding and the skin effect. Core losses for this design are negligible due to the presence of a low ac flux.

L2 is a 2 uH inductor and operates under conditions similar to L1. Therefore, the windings consist of seven turns of three #16 transformer wires in parallel, and the core is a Magnetics, Inc. MPP #55059. The actual measured values of L1 and L2 are shown in Table 4.1. These values are used for analysis of the power dissipation and small-signal performance later in this document.
Table 4.1 Input Filter Measured Magnetics Components Values

<table>
<thead>
<tr>
<th>Component</th>
<th>Parameter</th>
<th>Measured Value (80 kHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>L1</td>
<td>Inductance</td>
<td>10.2 uH</td>
</tr>
<tr>
<td>L1</td>
<td>DCR</td>
<td>1.5 Ω</td>
</tr>
<tr>
<td>L2</td>
<td>Inductance</td>
<td>2.4 uH</td>
</tr>
<tr>
<td>L2</td>
<td>DCR</td>
<td>649 mΩ</td>
</tr>
</tbody>
</table>

L1  Core: MPP55071; Magnetics, Inc.
    Windings: 13 turns of 3-#16 AWG in parallel

L2  Core: MPP55059; Magnetics, Inc.
    Windings: 7 turns of 3-#16 AWG in parallel
4.2 Input Filter Performance

Although [5] is an approximation procedure and not an optimization routine, the filter performance provided the desired attenuation at the inductor ripple frequency of 80 kHz. Figs. 4.2a and 4.2b show the measured gain and impedance, respectively. Each plot also includes the associated phase. The gain diagram shows the attenuation to be 44 dB at 80 kHz, which is in excess of the required 41 dB attenuation.

Fig. 4.3 shows the output impedance of the input filter and the input impedance of the converter. Note that the input impedance of the converter gain plot never crosses that of the output impedance of the input filter. By the input filter having a lower output impedance than the converter impedance, the converter will not interact with the filter, which is the indication of a properly designed input filter.
a. Filter Gain and Associated Phase

b. Filter Output Impedance and Associated Phase

4.2 Input Filter Measured Characteristics
Impedance (dB ohms)

Frequency (Hz)

Figure 4.3 PSPICE Model Comparison of the Input Filter Output Impedance with the Input Impedance of the Converter

(Model Conditions for Input Impedance: Low Line, Full Load)
Figure 4.4 Small-Signal PSPICE Model of the VFPPAT

(Using Ridley PWMCCM [7])
4.3 Summary

The amount of attenuation required for the input current ripple to meet specified level of 250 mA was found to be 41 dB. From this a two section filter was designed, and the required values were calculated. The selection of the components was then performed. The performance results indicated the filter would provide proper attenuation without interfering with the converter operation. The small-signal model was also introduced and is used in Chapter 5 for analyzing the small-signal characteristics.
5. CONTROL BOARD DESIGN OPTIMIZATION

This chapter contains the design of all of the control board components, including the PWM and drive circuitry, along with the CIC loop and voltage loop. For convenience, the final control board schematic is presented in Fig. 5.1. Note that the power stage was designed to the input voltage regulation range of 53 Vdc minimum, while optimization of the efficiency, and the small and large-signal performance is related to the input voltage performance or efficient operating range with a minimum of 64 Vdc input (refer to Table 1.1). Survival related items (such as Vsense in Fig. 5.2) are designed to perform over the regulation range.
Figure 5.1 Control Board Schematic
5.1 Design of PWM and MOSFET Gate Drive Circuitry

**PWM Circuitry**

The initial choice of a UC1825 PWM was determined in Chapter 2. The choice of this IC was based on the need for dual output drivers which operated 180° out of phase and on the approved parts list [2] available selection.

The manufacturer’s data sheet [6] on the UC1825 PWM provides a graph for the user to program the dead time of the gate drive using the timing capacitor \( C_T \). The amount of dead time needed is found from the maximum duty cycle required by the gain (\( D_{\text{max}} = 0.91 \)):

\[
\text{Dead Time} = \frac{1}{2} \times \frac{1 - D_{\text{max}}}{2 \times f} = \frac{1}{2} \times \frac{1 - 0.91}{80\text{kHz}} = 0.56 \text{ usec}.
\]

The value provided by the data sheet graph is 7 ns. A value of \( C_T = 4.7 \text{ ns} \) was chosen to allow for regulation under worst case conditions and was proven to provide proper regulation at low line (53 Vdc), full load (15 A).

Once the timing capacitor value was chosen, the timing resistor value was selected from the manufacturer’s chart for the switching frequency of 40 kHz. A value of \( R_T = 3900 \Omega \) was chosen, and the resulting switching frequency was 40.2 kHz.
Gate Drive Circuitry

The use of parallel IRF350 MOSFET switching transistors for each primary was discussed in Chapter 1. Implementation of a drive circuit for parallel MOSFETs can become complicated due to mismatched parasitics of the device or wiring. Slow triggering by one device can result in all of the drain current flowing through the parallel device, threatening reliability. For this reason the use of one UC1707 driver chip per switch (i.e. per pair of IRF350 MOSFET switches) was used.

The use of the drivers provide fast switching of the MOSFETs. Even though the drive capabilities of the UC1825 PWM are similar to the drivers found in the UC1707 IC, the UC1707 has dual drivers that drive one MOSFET each; this makes for a more desirable arrangement. The UC1707 chips were removed to test the ability of the UC1825 PWM to drive the parallel IRF350 MOSFETs. Although switching times were comparable, the overall current drawn by the control circuit increased and the PWM ran hotter to the touch. Gate switching waveforms are included with the power loss analysis section of this document.

It was necessary to insert a 1 kΩ resistor between the 12 Vdc housekeeping voltage and the driver Vc connection on the UC1825 PWM (pin 13 in Fig. 5.1). This is due to the presence of a 5.7 V zener within the UC1707 driver IC which clamps all input voltages to a digital level. The 1 kΩ resistor limited the current through the zener and avoided the application of the 12 V housekeeping level across a 5.7 V zener. Note that the OR gate (Fig. 5.1) for the timing ramp must be tied to the output of the driver to minimize effects due to delays within the driver. Fig. 3.4 shows a 1kΩ resistor across each MOSFET’s gate and source terminals. This resistor is recommended by the manufacturer to prevent false triggering of the gate.
5.2 Current-Injection Control (CIC) Loop

As mentioned earlier, the CIC loop senses the switch current. This allows both the dc and ac components to be fed back. The use of the dc level is essential to maintaining flux balance within the autotransformer. The ac slope of the waveform contributes to the performance of the CIC gain characteristic by its relation to the external ramp slope [7].

**Determining Parameter Values**

The current loop schematic and accompanying waveforms are pictured in Fig. 5.2. In deciding to use the UC1825, one of the limiting factors was the low output level produced by the error amplifier. This level of 4.5 V is further reduced by an internal offset voltage of 1.25 Vdc at the other comparator input as shown in Fig. 5.2 (pin 7 Fig. 5.1). The summation of a ramp and sense voltage (Vsense) would have to be lower than 4.5 V - 1.25 V = 3.25 V. This level could be difficult to achieve due to the amount of attenuation required to step down the peak switch current (Isw_peak = 25.3 A) to a level of Isense. Any large switching spikes could generate noise and false trigger the PWM comparator. With the alternative of the design of a discrete PWM circuit, the goal was to retain the use of the UC1825 PWM.
a. Schematic

b. Waveforms

Figure 5.2 CIC Loop Schematic and Waveforms
With reference to Fig. 5.2, the design of the CIC loop components began with the calculation of the sense voltage \( V_{\text{sense}} \). This value was based on the error amplifier output voltage, the 1.25 V offset, and the maximum external ramp value \( V_{\text{ramp}}_{\text{max}} \). \( V_{\text{ramp}}_{\text{max}} \) was chosen to be 1 V. The actual ramp value was varied to attenuate the peaking of the converter at half of the switching frequency [7]:

\[
V_{\text{sense, max}} = VE/A_{\text{min}} - V_{\text{ramp}}_{\text{max}} - 1.25 \text{ V offset},
\]

\[
V_{\text{sense, max}} = 4.5V - 1.0V - 1.25 \text{ V offset} = 2.25 \text{ V}.
\]

Design of the sense resistor is based on the turns ratio of the current sense transformer (N2) and the value of \( V_{\text{sense}} \). The desire to reduce the current in the secondary of the current sense transformer results in values of N2 between 100 and 200. This will reduce the peak current \( I_{\text{sense, peak}} \) to levels of 253 mA and 127 mA, respectively, allow for a reasonable sense resistor value (\( R_{\text{sense}} \)), and reduce the wire gauge of the secondary winding. Based on these predictions, N2 was selected to be 200. The primary carries high current and will remain a straight wire of one turn. The value of \( R_{\text{sense}} \) can now be determined:

\[
R_{\text{sense, max}} = \frac{V_{\text{sense, max}}}{I_{\text{sense, max}}} = \frac{V_{\text{sense, max}}}{I_{\text{peak}}/N2},
\]

\[
R_{\text{sense, max}} = \frac{2.75V}{25.3A} \times 200 \text{ turns} = 21.73 \Omega.
\]

The actual value used for \( R_{\text{sense}} \) was 16.5 \( \Omega \).

The leading edge of the \( V_{\text{sense}} \) waveform will exhibit a large spike which can be attributed to the peaking of the switch current at turn ON. This peak must be filtered or it will cause false triggering of the switches. The filter arrangement consists of an RC filter network (\( R_{f} \) and \( C_{f} \) in Fig. 5.2). The value of \( C_{f} \) is determined experimentally to be 37 nF which allows proper regulation to occur over all line and load ranges. The value of \( R_{f} \) is
then calculated so that the corner frequency of the filter is at least ten times greater than
the 80 kHz switching frequency to avoid introducing additional phase lag in the loop.
The calculation of $R_f$ is as follows:

$$R_f \leq \frac{1}{2\pi \times C_f \times 10f} = \frac{1}{2\pi \times 37nf \times 10 \times 80kHz} = 5.4\Omega.$$  

The value used for $R_f$ was 3.9 $\Omega$.

**Resulting New Plant Characteristics (CIC Loop Closed)**

The use of a CIC loop reduces the open-loop control-to-output transfer function to a
single pole roll off (where the single pole replaces the double pole formed by the output
capacitor and inductor) as shown in [7]. This makes compensating the current loop eas-
ier. The open-loop transfer function was measured only after the slope of the external
ramp was determined experimentally to be $7.9 \times 10^4$ V/sec. Fig. 5.3 shows the predicted
and measured gain and phase of the new plant. The plot shows the gain exhibiting a
slope of -1 up to the ESR zero of the 2000 uf bus capacitor which is at 3.4 kHz and a
cross-over frequency of 664 Hz. Agreement with the model is good.
Figure 5.3 Open-Loop Control-to-Output Characteristic with CIC Loop Closed
5.3 Voltage Loop Design and Optimization

The introduction of the new plant obtained when measuring the control-to-output transfer function with the CIC loop closed allows the designer to begin developing the compensation network. The chosen compensation network and resulting characteristics are presented in Fig. 5.4. Note that the voltage follower is present for two reasons. First, the voltage follower represents the mode controller amplifier that will be incorporated when the battery discharger is mated to the system. Second, the output of the op amp provides a virtual impedance of zero which eliminates the impedance interaction of the attenuation resistors Ra and Rb so that the control loop performance is easier to calculate and obtain. The amount of attenuation provided by Ra and Rb is given in Eq. 5.3:

$$\text{Output Attenuation} = 20 \times \log \frac{R_b}{R_a + R_b},$$  \hspace{1cm} (5.3)

$$\text{Output Attenuation} = 20 \times \log \frac{3.4k\Omega}{100k\Omega + 3.4k\Omega} = -29.7 \, \text{dB}.$$  

The resulting reference voltage for dc bias of the compensator is 4 Vdc as shown:

$$\text{Reference Voltage} = \frac{120V \times 3.4k\Omega}{100k\Omega + 3.4k\Omega} = 3.95 \, Vdc.$$ 

The compensator characteristic shows that components C2, R1, and R3 determine the poles and zero, while the gain can be manipulated by changing C3. The values chosen for these components were the result of optimization of the loop performance.
a. Schematic

fp1 (@ origin)  

fp2 = 5.3 kHz

fz = 530 Hz

\[ \text{Gain} = \frac{sC2(R1 + R3) + 1}{sC3R1(sC2R3 + 1)} \]

\[ R1 \gg R3 \quad C2 \gg C3 \]

\[ fp2 = \frac{1}{2\pi C2R3} \quad ; \quad fz = \frac{1}{2\pi C2R1} \]

\[ R1 = 3k\Omega, \quad R3 = 300\Omega, \quad C3 = 610pf, \quad C2 = 100nf \]

b. Characteristic

Figure 5-4 Compensation Schematic and Characteristic
Effects of the 20' Cable

A twenty foot cable of #10 AWG wires exists between the output of the converter and the system-required 2000 uf bus capacitor. The optimization procedure for the compensator took place with the twenty foot, twisted pair of #10 AWG wires taken into consideration. These wires will simulate the actual spacecraft's twisted, shielded pair that will be present between the output of the converter and the 2000 uf capacitor of the load. The resulting inductance of this cable tended to resonate with the output capacitors of the power converter at 27 kHz. This resonance interacted with the optimization of the control loop performance. Therefore, the analysis of the cable and damping network is presented before the small-signal performance data.

The impedance of the output capacitors, cable, and load are shown in Fig. 5.5. Note the load resonates at 27 kHz without the damping network. As will be shown with the small-signal performance data, the addition of the damping network eliminated peaking in the voltage loop and reduced its effect on the output impedance.
a. Measured Characteristic

b. Actual and Equivalent Parasitic Schematic

Figure 5.5 Impedance of Output Capacitors, Dynamic Load, and 20’ Cable
5.4 Measured Small-Signal Performance

**Voltage Loop Performance**

The resulting loop gain performance of the voltage loop (CIC loop closed) is shown in Fig. 5.6 for the case of low line, full load. The loop exhibits a wide bandwidth with a cross-over frequency of 5.3 kHz and a phase margin of 63°, this indicates a stable design. Once again, the model agrees with the measured data. A full performance analysis of the loop over line and load is shown in Figs. 5.7 and 5.8.
Figure 5.6 Loop Performance with 20' Cable; Low Line, Full Load
Figure 5.7 Loop Gain With 20 Foot Cable (64 V Input)
Figure 5.8 Loop Gain With 20 Foot Cable (84 V Input)
Output Impedance

Output Impedance of the system is shown in Fig. 5.9 in magnitude of dB ohms along with the associated phase. The damping network (Fig. 5.5) reduced the peaking of the output impedance at the frequencies above 5 kHz. Below 5 kHz, the converter has an average of less than 25 mΩ. Above 5 kHz the impedance peaks at 45 mΩ which is the approximate value of the ESR of the 2000 uf capacitor bank. The PSPICE plot verifies the measured data from the HP4194a impedance analyzer to 10 kHz. The accuracy of the measured data above 10 kHz is questionable due to the limited bandwidth of the Dynaload when used in the constant current mode (which is the only mode available for full output power).

It is noted that the final spacecraft system will require investigation and optimization of the cable interacting with the battery discharger. The methods discussed here were applied to a cable and 2000 uf capacitor similar to the final product. The actual system will need to be characterized and optimized in order to obtain good performance. A reduction in the peak output impedance is expected to take place when using the actual capacitors due to the reduced ESR. Similarly, using the actual shielded cable should result in improved performance. Figs. 5.10 and 5.11 show the effects a varying load has on the output impedance at input voltages of 64 Vdc and 84 Vdc, respectively.
Figure 5.9 Output Impedance with 20' Cable

(Low Line, High Load)
Figure 5.10 Output Impedance With 20 Foot Cable (64 V Input)
Figure 5.11 Output Impedance With 20 Foot Cable (84 V Input)
5.5 Measured Large-Signal Performance

Stepped Output Current

The specifications (Table 1.1) call for the transient performance to achieve a settling time of 10 msec and to retain a peaking range of 115.2 V to 124.8 V. The converter performance shown in Fig. 5.12 achieves a settling time of 0.4 msec with and a critically-damped voltage waveform with peaks of 119.9 V maximum and 119.7 V minimum. The output level difference for the two different current levels can be attributed to the measured breadboard values having a finite gain of the error amplifier and a finite output impedance at dc.
Figure 5.12 Stepped Load Response

(2 A to 13 A)
**Output Voltage Ripple**

The specified output voltage ripple is 200 mV peak-to-peak as defined in Table 1.1. The actual ripple voltage for inputs of 64 Vdc and 84 Vdc are shown in Figs. 5.13 and 5.14, respectively. The converter complies well with the specified maximum ripple voltage by producing output ripple voltage levels of 50 mV and 70 mV for input voltage levels of 64 Vdc and 84 Vdc, respectively. Note that the higher output ripple voltage which occurs at 84 Vdc input voltage is expected due to the higher peak-to-peak inductor current.

**Input Current Ripple**

Input ripple current is specified as 250 mA peak-to-peak in Table 1.1. The measured peak-to-peak ripple is shown in Figs. 5.13 and 5.14. The input ripple current levels are 220 mA peak-to-peak and 150 mA peak-to-peak for input voltages of 64 Vdc and 84 Vdc, respectively. Note that the value is higher for the 64 Vdc case as expected due to the higher peak currents entering the autotransformer at the lower voltages.
Figure 5.13 Input Current Ripple and Output Voltage Ripple

(Vin = 64 Vdc)
Power Stage Waveforms (Vin = 84 VDC)

Performance Summary

\[ i_L = 3.8 \text{ Amps p-p} \]
\[ i_{IN} = 150 \text{ mA p-p} \]
\[ v_o = 70 \text{ mV p-p} \]

Vin = 84 VDC  \quad Vo = 120 VDC
lin = 22 Amps  \quad Io = 15 Amps
Pin = 1874 Watts  \quad Po = 1800 Watts
Efficiency = 96%

Figure 5.14 Input Current Ripple and Output Voltage Ripple

(Vin = 84 Vdc)
5.6 Summary

The use of CIC was shown to make closing the voltage loop a much easier process and to help performance. The closed loop design has been presented and the resulting small and large-signal tests show the converter exhibiting excellent performance within the specified levels. Cross over of the voltage loop is 5.3 kHz with a 63° phase margin. The output impedance shows some disagreement between the measured and predicted data. The predicted level for the output impedance never exceeds -27 dB (45mΩ).
6. POWER STAGE PERFORMANCE

The efficiency and converter regulation are presented as measured at the converter outputs, and power loss of the 20' cable is studied. Analysis of the efficiency includes power losses of the individual components of the power stage and the effects design optimization has on increasing the efficiency. Note that the heat sink temperature during most of the measurements reaches a maximum of 50°C.

6.1 Regulation

The converter exhibits excellent regulation over varying line and load conditions as shown in Fig. 6.1 where actual data is supplemented with a straight-line approximation. The required regulation range allows the input to be a minimum of 53 Vdc and a maximum of 84 Vdc. Note that the converter output varies only one volt or 0.8% for all line and load changes. The allowed change on the output is ±4% as specified in Table 1.1. Loads measured are from 1 A (120 W) to 15 A (1800 W) out.
a. Input Voltage = 53 Vdc

b. Input Voltage = 64 Vdc

c. Input Voltage = 74 Vdc

d. Input Voltage = 84 Vdc

Figure 6.1 Output Voltage Regulation Data and Straight-Line Approximation
6.2 Efficiency

The efficiency is first presented as it was measured at the input and output terminals of the converter with the 20' cable attached but not included in the efficiency calculations. The individual power loss of the power stage components is then presented, and a loss contribution of the power stage components is shown.

6.2.1 Efficiency at the Terminals

The converter efficiency is shown in Fig. 6.2 where the input voltage spans the range of 64 Vdc to 84 Vdc. The targeted efficiency for the converter is 96% at low line (64 Vdc), full load (15 A). The cable robs the converter of 12 W (0.7%) at this operating point as shown in Fig. 6.3. Therefore, at the converter output, the converter will actually see the 94.5% efficiency (Fig. 6.2) at the converter and 93.8% at the end of the 20' cable.

The targeted efficiency for low line, full load was 96%, and the value achieved was 94.5%. An assessment of the difference is provided in the summary at the end of the chapter.
Figure 6.2 Efficiency over Line and Load

(Power loss of the 20' cable has been subtracted.)
Figure 6.3 Power Lost to 20' Cable Based on Output Current
6.2.2 Power Dissipation in the Power Stage Components

The desired efficiency of 96% mentioned in the specifications (Table 1.1) must occur at low line (Vin = 64 Vdc) and full load (Io = 15 A). Therefore, the analysis of the power dissipated by each component will be performed for this operating point.

Figures 6.4, 6.5, and 6.6 show the waveforms for the diode current and voltage, inductor current and voltage, and current into the autotransformer, respectively. These currents are essential for establishing the power dissipation of each component. From Fig. 6.4 the time one switch is on is Ton=7.8 us, and the period is Tp=23.9 us. From these values the duty cycle for low line, full load and the period can be calculated:

\[ f = \frac{1}{T_p} = \frac{1}{23\mu\text{sec}} = 41.8\text{kHz}, \]

\[ D_{(\text{low line, full load})} = \frac{T_{on}}{T_p} = \frac{7.8}{23.9} = 0.326. \]
Figure 6.4 Diode Current and Voltage (Low Line, Full Load)
Figure 6.5 Inductor Current and Voltage (Low Line, Full Load)
Figure 6.6 Autotransformer Input Current (Low Line, Full Load)
Inductor Power Dissipation

The inductor will have three major contributors to the total power loss. These include: windings loss due to the dc resistance, core loss, and gap loss. The windings loss ($PL_{DCR}$) is based on the inductor rms current as measured by the Tektronix 11401 oscilloscope:

$$PL_{DCR} = IL_{rms}^2 \times DCR = (14.9A)^2 \times 0.023\Omega = 5\ W.$$  

The core loss ($PL_{core}$) and gap loss ($PL_{gap}$) were estimated using manufacturer's data and graphs. Note that $Ki=0.78$ is the gap loss coefficient, and $D=0.375''$ is the lamination width of the MC0007 core [8]:

$$PL_{core} = 50\left(\frac{W}{lbs}\right)\times weight = 50\left(\frac{W}{lbs}\right)\times 0.077lbs = 3.85\ W,$$

$$PL_{gap} = Ki \times D \times lg \times 2f \times B_{ac}^2,$$

$$PL_{gap} = 0.78 \times 0.375cm \times \left(2.54\ cm/in\right) \times 0.024'' \times (0.124Tesla)^2 = 0.86\ W.$$  

The total loss of the inductor is the sum of the windings loss, core loss, and gap loss and is equal to 9.7 W.

MOSFET Power Dissipation

The MOSFET power dissipation was mainly due to the ON resistance of the device. The use of a snubber eliminated most of the switching loss as shown by the 50 nsec delay in the drain current (Fig. 6.8). The rms drain current of the MOSFET was a measured value of 13.625 A for one set of switches in parallel, and the measured drain-to-source voltage drop was 3.5 V. The total power loss for all of the switches is shown in the following equation:

$$PQ_{ON} = 2 \times I_{sw_{rms}} \times V_{ds_{ON}} = 2 \times 13.625A_{rms} \times 3.5V = 31.2\ W.$$  

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Snubber Power Dissipation

The snubber circuit that best damped the ringing of the autotransformer leakage inductance and Coss of the MOSFETs was found experimentally and had a capacitance value of 10 nf and a resistance of 9 Ω (6-56 Ω, 2 W resistors in parallel). The power dissipation of this circuit is shown below:

\[ P_{snub} = 4 \times C_{snub} \times V_{in}^2 \times f = 4 \times 10nf \times (64V_{dc})^2 \times 40kHz = 6.8 \, W. \]

Rectifier Diodes Power Dissipation

Oscilloscope observations showed the rectifiers switching very fast and exhibiting no crossing of the current and reverse voltage waveforms, and therefore, little switching loss. Only the ON loss contributions to the power dissipation were considered. This loss is shown in the following equation (where the current and voltage are from Fig. 6.4):

\[ PD_{ON} = 2 \times I_{D_{rms}} \times V_{D_{ON}} \times \frac{Ton_{diode}}{T_P} = 2 \times 9.1A_{rms} \times 2.7V \times \frac{16.1\mu sec}{23.9\mu sec} = 33W. \]
**Autotransformer Power Dissipation**

The autotransformer will dissipate power in the dc resistance of the winding, the leakage inductance of the winding, and in the core. These losses are summarized in the following equations:

\[ P_{wind} = 2 \times ((Isw_{rms})^2 \times PrimDCR + (ID_{rms})^2 \times (PrimDCR + SecDCR)), \]

\[ P_{wind} = 2 \times ((13.625A_{rms})^2 \times 0.004\Omega + (9.1A_{rms})^2 \times (0.004\Omega + 0.002\Omega)) = 2.5 \text{ W}, \]

\[ Plk = (lk \times Ibw_{rms} + (lk + lks) \times ID_{rms}^2) \times 2f, \]

\[ Plk = (220nH \times 13.6A_{rms})^2 + (220nH + 117nH) \times 9.1A_{rms}^2 \times 2 \times 40kHz = 5.7 \text{ W}, \]

**Total Windings Loss = Pwind + Plk = 2.5W + 5.7W = 8.2 W,**

\[ P_{core} = l_{in}^* \times V_{in} - 2 \times P_{snub} = 266mA \times 64Vdc - 6.8W = 10.2W, \]

where \( l_{in}^* \) is the input current into the autotransformer measured with the secondaries disconnected.

The power loss of the transformer is 44.6% loss to the windings and 55.4% to the core. The almost equal division of the power loss between the core and windings indicates a good transformer design.

**Output Capacitor Power Dissipation**

The output capacitor power dissipation occurs when the ac inductor current passes through the ESR of the capacitor. The measured ac inductor current is 798 mA rms, and the equivalent ESR of two 5 uf capacitors in parallel is 6.5 m\( \Omega \). The resulting power is a mere 4 mW:

\[ P_{Co} = ILa_{rms}^2 \times ESR_{Co} = (798mA_{rms})^2 \times 6.5m\Omega = 4 \text{ mW}. \]
**Input Capacitor Power Dissipation**

Because of the large input rms current flowing in the input capacitors, the power dissipation is considered separately from the remaining input filter components. The input capacitor power dissipation is a result of the ac input current into the autotransformer passing through the ESR of the capacitor. The measured ac autotransformer inductor current is 7.9 A rms (Fig. 6.6), and the equivalent ESR of two-10uf capacitors in parallel is 4.5 mΩ. The total power dissipation of the two-10 uf input capacitors is only 0.3 W, therefore, the choice of polypropolene capacitors is optimal:

\[ PCI = I_{inac_{rms}}^2 \times ESR_{ci} = (7.9A_{rms})^2 \times 4.5m\Omega = 0.3\ W. \]

**Input Filter Power Dissipation**

The input filter inductors experience loss only to the windings. The small ac flux makes the core loss negligible. Also, the small ac current through the 0.6Ω resistor and 100uf capacitor (C1) do not contribute to the power loss of the filter. The entire filter power loss was found to be 4 W which is excellent.

\[ P_{filter} = I_{filter_{rms}} \times (VL1 + VL2) = 31.4A_{rms} \times (85mV + 43mV) = 4 \ W \]

**Total Power Loss**

The total power converter loss was measured to be 109.5 W and the summation of the power component losses was a total of 103.3 W proving the analysis was accurate to within 5.6%. This accuracy is acceptable with the measurement methods used and considering that no drops due to connectors or miscellaneous items were considered. Fig. 6.7 shows a pie chart of the loss contribution (where the loss due to the output capacitor is omitted because of its small value).
Figure 6.7 Power Loss Analysis Pie Chart
(The loss due to the output capacitor was small enough to be omitted.)
Figure 6.8 Gate Turn ON and Drain Turn OFF Waveforms
6.3 Summary

The goal of a 96% efficient design at low line, full load was not achieved. However, two changes in the specifications were implemented after the 96% goal was established in [1]. The input voltage minimum for regulation was lowered from 53 Vdc to 64 Vdc, making it necessary to add secondaries to the autotransformer windings. The additional windings increased the power loss of the autotransformer and MOSFETs. Also, the recently established input current ripple value of 250 mA resulted in losses in the input filter inductor windings. These losses can be reduced at the expense of using larger inductors, which is not recommended since the filter inductors were optimized for size.

The measured converter efficiency at the terminals matches well with the loss contribution analysis. The loss contribution chart (Fig. 6.7) shows that the optimization in the design of the power stage magnetics benefits the overall performance. The largest loss contribution to the total loss is in excess of 60%, and this is due to the semiconductor devices. The MOSFET switch voltage rating resulted in choosing a device with higher drain resistance, which caused increased power loss. Rectifier diode losses are about as low as the choice of diodes will allow (the devices currently being used are not on the approved parts list [2]). The use of synchronous rectifiers may help increase efficiency but will also increase complexity. Finally, the large semiconductor losses have a direct effect on the heat sink size since all of the semiconductor devices are heat sink mounted.
7. SUMMARY

A possible candidate for the battery discharger topology has been optimally designed and the performance results presented. The converter performed well for the duration of the testing and produced clean waveforms (ie. waveforms that did not exhibit substantial amounts of ringing). Estimated power density of the power stage for the final design was 50 W/in$^3$. The final performance summary of the VFPPAT battery discharger is shown in Table 7.1.

All of the specified levels were obtained with the exception of efficiency. Unfortunately, efficiency is the most important parameter in the choice of the final battery discharger topology. As mentioned earlier, the original specifications did not require the input voltage range to be less than 64 Vdc. The minimum input voltage level of 53 Vdc required secondaries on the autotransformer, and the demanding input current ripple specification of 250 mA required a two section input filter. These additions caused additional power loss. Had the specifications not been changed, 96% efficiency would most likely have been possible as predicted in [1].

Optimization of the magnetics design proved to be beneficial to the final efficiency. The autotransformer was designed three times and four devices were built. In order to balance the core losses of the autotransformer with the windings loss, foil windings had to be used. Each device resulted in increased efficiency and a reduction in size over its predecessor. The final design achieved an almost equal division of power loss between the winding and the core. The power inductor as well as the autotransformer are compact in size with very efficient use of the window for each device.
One area in which the VFPPAT topology exhibited exceptional performance was related to the control loop. Current loop control benefited the large- and small-signal performance. The resulting voltage loop cross over frequency of 5.3 kHz at 63° phase margin is very good. The settling time of the converter to a stepped load is excellent at 0.4 msec.
### Table 7.1 Battery Discharger Adherence to Design Specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
<th>Value Achieved</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Input Voltage Range</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Efficient Operating Range</td>
<td>64 Vdc to 84 Vdc</td>
<td>64 Vdc to 84 Vdc</td>
</tr>
<tr>
<td>Regulation Range</td>
<td>53 Vdc to 84 Vdc</td>
<td>53 Vdc to 84 Vdc</td>
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<tr>
<td><strong>Output Voltage Range</strong></td>
<td>120 Vdc ± 4%</td>
<td>119.5 Vdc ± 0.4%</td>
</tr>
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<td>Output Voltage Ripple</td>
<td>200mV peak-to-peak</td>
<td>70mV peak-to-peak</td>
</tr>
<tr>
<td>Output Power Range</td>
<td>0 W to 1800 W</td>
<td>0 W to 1800 W</td>
</tr>
<tr>
<td>Output Current Range</td>
<td>0 A to 15 A</td>
<td>0 A to 15 A</td>
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<td>Input Current Ripple</td>
<td>250 mA peak-to-peak</td>
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</tr>
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<td>Switching Frequency</td>
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</tr>
<tr>
<td>Efficiency (low line, full load)</td>
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<td>94.5%</td>
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<tr>
<td>Transient Performance</td>
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<td></td>
</tr>
<tr>
<td>Output Voltage Peaking Range</td>
<td>115.2 - 124.8 Vdc</td>
<td>119.7 - 119.9 Vdc</td>
</tr>
<tr>
<td>Output Settling Time</td>
<td>10 msec</td>
<td>0.4 msec</td>
</tr>
</tbody>
</table>

1 Figure 6.1  
2 High Line (Vin = 84 Vdc), Full Load (Io = 15 Adc); Figure 5.14  
3 Low Line (Vin = 64 Vdc), Full Load (Io = 15 Adc); Figure 5.13  
4 Figure 6.4  
5 Figure 6.2  
6 Low Line (Vin = 64 Vdc), Load Cycled 2 Adc to 13 Adc; Figure 5.12  
7 Figure 5.12
REFERENCES


REFERENCES


VITA

The author was born in Fulton, New York on September 12, 1961. He attended Phoenix Central Schools in Phoenix, New York and graduated in 1979. He then attended the State University of New York (SUNY) at Geneseo, New York where he majored in Physics, 3-2 Engineering. In 1983 he completed his three years at Geneseo and entered Syracuse University at Syracuse, New York to complete the final two years of his 3-2 engineering requirement. The final degrees awarded in 1985 were a Bachelor of Arts in Physics with a Computer Science minor from SUNY Geneseo and a Bachelor of Science in Electrical Engineering from Syracuse University.

From 1985 to 1989, the author worked for Motorola's Government Electronics Group in Scottsdale, and then Chandler, Arizona where he designed power supplies for communications equipment.

In May of 1989, Scott began his graduate education with a summer position at General Electric's R&D Center in Schenectady, New York where he started the initial phase of researching power conversion at frequencies above 20 MHz.

In August of 1989 Scott started graduate study at Virginia Tech and continued the research in high frequency power conversion. In March of 1990, the author joined the team of the NASA Space Platform where he remained until his graduation in April of 1991.

Scott W. Deerty