High Efficiency SEPIC Converter For High Brightness Light Emitting Diodes (LEDs) System

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ABSTRACT

This thesis presents an investigation into the characteristics of and driving methods for light emitting diode (LED) lamp system. The characteristic of the light emitting diode (LED) lamp is described and the requirements of the ballast for the light emitting diode (LED) lamp are presented.

Although LED lamps have longer lifetime than fluorescent lamps, the short lifetime limitation of LED driver imposed by electrolytic capacitor has to be resolved. Therefore, an LED driver without electrolytic capacitor in the whole power conversion process is preferred. A single phase, power factor correction converter without electrolytic capacitors for LED lighting applications is proposed, which is working in discontinuous conduction mode (DCM). Different with a conventional SEPIC converter, the middle capacitor is replaced with a valley-fill circuit. The valley-fill circuit could reduce the voltage stress of output diode and middle capacitor under the same power factor condition, thus achieving higher efficiency. Instead of using an electrolytic capacitor for the filter, a polyester capacitor of better lifetime expectancy is used.

An interleaved power factor correction SEPIC with valley fill circuit is proposed to further increase the efficiency and to reduce the input and output filter size and cost. The interleaved converter shows the features such as ripple cancellation, good thermal distribution and scalability.

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CHAPTER 1

OVERVIEW AND BACKGROUND OF RESEARCH

1.1 Introduction

Light or visible light is the electromagnetic radiation of a wavelength that is visible to the human eye (about 400-700nm), or up to 380-750nm [1]. It is unthinkable if this world had no solar energy for just a day. During the past 100 years, man has never given up the search for effective light sources. The research of converting electric power to light energy in a simple manner has driven the development of modern lamps in the past decades [2]. Electrical lighting sources have been an important part in human being's daily life since Edison invented the first incandescent lamp in 1879 [3,4]. When the fluorescent lamps were first developed in 1938, electrical lighting sources achieved a milestone. From then on, a novel concept, 'gas discharge lamp' was proposed [5, 6], and many new types of electrical lamps were invented after that, such as, high pressure mercury lamps (HPM), high pressure sodium lamps (HPS), metal halide lamps (MH), flash-lamps filled with inert gas [7, 8].

Nowadays lighting consumes approximately 10–15% of the global energy requirement [9]. Given the increasing concerns about energy saving, the improvement for the overall efficiency of lighting systems is of significant importance. Fluorescent lamps are well known for decades to be an efficient light source, which are mainly used for home and office lighting. Recently, a new type of lamps: light emitting diode (LED) lamps are born. The LED lamps that are now available can reliably offer over 120

lumens from a one-watt device. Due to the high-efficiency, the LEDs are increasingly attractive in the world, especially for industrial applications such as the street light [9-11].

The major characteristics, which should be considered when choosing a lamp, are the luminous efficacy, lifetime, and lumen depreciation. Luminous efficacy is the measure of the lamp's ability to convert input electric power, in watts, into output luminous flux, in lumens, and is measured in lumens per watt (lumens/watt). The life of a lamp is the number of hours it takes on average for 50% of lamps of the same kind to fail. The lumen depreciation is the decrease in lumen output that occurs as a lamp is operated [12].

Incandescent lamps (light bulbs) create light by running electricity through a thin filament, thereby heating the filament to a very high temperature so that it glows to produce visible light. The lifespan of an incandescent lamp is around 1,000 hours, which is much shorter than that of other common used lamps such as either a fluorescent lamp and LED lamp [9].

Fluorescent lamp is a gas-discharge lamp, which uses the electricity to excite mercury vapor, then in turn to produce short-wave ultraviolet light. The ultraviolet light is absorbed by a phosphor coating inside the lamp, causing it to produce visible light. While the heat generated by fluorescent lamps is much less than its incandescent counterpart, energy is still lost in generating the ultraviolet light and converting this light into visible light. Fluorescent lamps have life spans around 10,000 to 20,000 hours. [1, 12, 13]. Mercury has been used during the manufacturing of fluorescent lamp, which

is another disadvantage of the fluorescent lamp- safety issue.

1.2 Light emitting diode (LED) Lamps

1.2.1 The Principle and Characteristic of Light emitting diode (LED) Lamps

A light-emitting-diode (LED) is a semiconductor diode that emits light when an electric current is applied in the forward direction of the device, as in the simple LED circuit [14]. When the LED is forward biased, electrons recombine with electron holes and release energy in the form of photons. This effect is the electroluminescence where incoherent and narrow-spectrum light is emitted from the p-n junction in a solid state material. A LED lamp is a type of solid state lighting (SSL) that uses light-emitting diodes (LEDs) as the source of light, rather than electrical filaments, plasma (used in arc lamps such as fluorescent lamps). An LED is usually a small area (less than 1 mm^2) light source, often with optics added directly on top of the chip to shape its radiation pattern [15]. The color of the emitted light depends on the composition and condition of the semiconducting material used, and can be infrared, visible, or ultraviolet. The basic construction of high power high brightness Philps LED is illustrated in Fig.1.1 [30]. It includes the lens, LED chip, silicon submount, thermal heatsink, cathode lead, bond wire and outer package [16].

Before the high brightness LEDs come into the market, the LEDs have been widely used as indicator on electronic devices and battery powered applications for decades [17]. These applications include cell phone handsets, digital still cameras, automotive lighting [18, 19], emergency lighting [17, 20], and LCD backlighting

[21-26], and so on. Due to the high rise in luminous efficiency that high brightness LEDs have experienced in the last recent years, many new applications such as using as street lamps have been researched [27-29].

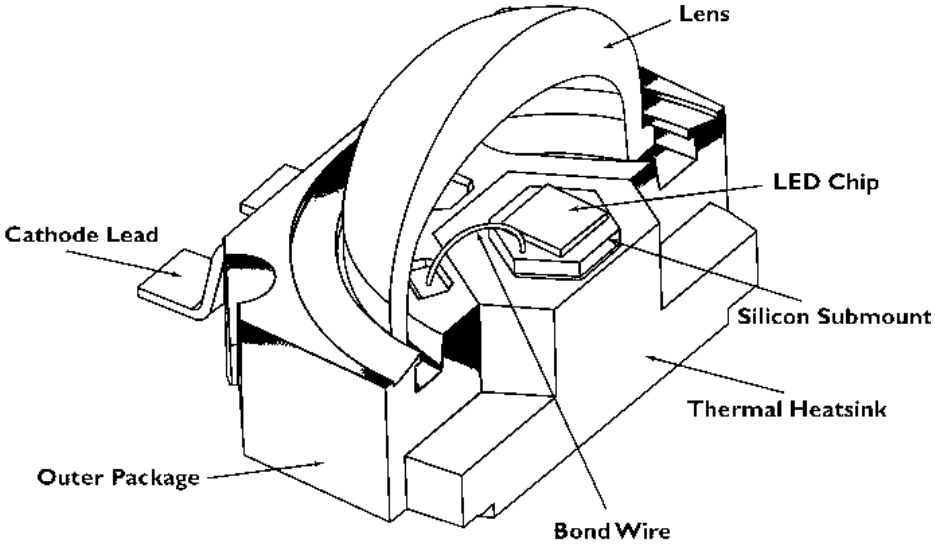


Figure 1.1 Basic construction of High Brightness Philps LED

Compared to the gas discharge lamps including fluorescent lamps, the advantages of using LED are mainly embodied in the following aspects [14, 30]:

- Long lifetime: LEDs have a relatively long lifetime, which are 35,000 to 50,000 hours of useful life, though time to complete failure may be longer. Some LED manufacturers claim lifetime of 100,000 hours, but this point has not been practically confirmed and needs justifications [9, 31-33]. Fluorescent lamp typically are rated at about 10,000 to 15,000 hours, depending partly on the conditions of use, and an incandescent light bulbs typically are rated at 1,000–2,000 hours [10, 34].
- High Efficiency: LEDs produce more light per watt than incandescent bulbs and

fluorescent lamps. High brightness LEDs are now available that can offer over 120 lumens from a one-watt device, or much higher outputs at higher drive currents [32].

- Full Dimming: LEDs can very easily be dimmed, unlike fluorescent lamps. There are two methods to dim LEDs lamps, include: pulse-width modulation (PWM) dimming and analog dimming. Pulse-width modulation dimming turn the light on and off very quickly at varying intervals. Pulse-width modulation dimming is a more efficient means to modulate the intensity of the light produced by the LED lamp [35, 36].
- Small Size: LEDs are relatively small and are easily mounted onto printed circuit boards, thus providing design flexibility, as they can be arranged in rows, rings, cluster [9, 26].
- Mercury-free: Based on the solid state lighting, LEDs contain no hazardous mercury or halogen gases, unlike fluorescent and most HID gas discharge technologies [13, 37]. GaN-based LEDs do not contain any heavy metals or arsenic.

Although LED lamps have a lot of advantages over fluorescent lamps, the disadvantages of using LEDs are also obvious:

- High price: LEDs are currently relatively more expensive than the conventional lighting technologies such as fluorescent lamps and HID lamp. However, when considering the total cost including the replacement costs and the long lifetime of LED lamps, LEDs are beginning to threaten the conventional lamps [14].

- Temperature dependence: LED performance largely depends on the junction temperature of LED and the ambient temperature of the operating environment. Over-driving the LED in high ambient temperatures may result in overheating of the LED package, eventually leading to the failure of LED. Adequate heatsink is required to maintain long lifetime. This is especially important when considering automotive applications where the device must operate over a large range of temperatures [14, 18, 19].
- Voltage sensitivity: A small voltage variation across the LEDs can lead to a large change of the LEDs current. Therefore, LEDs should be supplied with current source rather that voltage source to keep good performance of LEDs [38].

According to [39, 40], for the current level near the rated current, the forward voltage V_F can be approximated by Eq. (1.1). In this equation, I_F represents the LED current, V_{LED} represents the linear coefficient, V_{DIODE} represents voltage drop of the ideal diode, R_{LED} represents the series intrinsic resistance in the power LED. The series resistance causes the inclination in the curve and is the main factor responsible for Ohmic losses.

$$V_F = V_{LED} + R_{LED} \cdot I_F + V_{DIODE} \tag{1.1}$$

The LED can be represented by an electrical model as shown in Fig.1.2. This electrical model has a good accuracy for current values near the LED rated current.

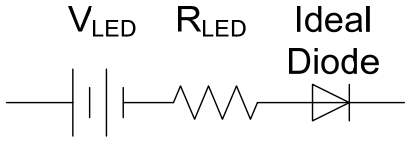


Figure 1.2 LED electrical model

1.3 Ballasts for Light emitting diode (LED) Lamps

1.3.1 Topology and Performance Requirements of Electronic Ballast Circuit

Development of highly reliable and highly efficient electronic driver for Light emitting diode (LED) has always been a hot research topic [9, 31, 41]. Generally, high performance electronic driver design for Light emitting diode (LED) lamp should satisfy the following requirements.

A. High Power Factor

In AC power system, the power factor is the ratio of the real power flowing to the load to the apparent power of the converter. Due to the non-linear load in the circuit, which distorts the wave shape of the current drawn from AC source, the real power can be smaller than the apparent power and the power factor will be less than unity. LED driver should incorporate power factor correction (PFC) techniques to improve the consumption of electrical energy and to provide agreement with power quality standards [42]. Nowadays, international standards has been published, which set requirements to limit the magnitudes of harmonic currents injection into the public supply system. Utilizing PFC not only ensures that the LED driver system compliance with the specifications and standards [43, 44], but also improves the efficiency of the circuit. The advantages of PFC include:

- PFC can improve the voltage quality. Load with lower power factor draw more current from the source than the load with a higher power factor. As power

factor decreases, the line current increases, which causes greater voltage drops in the conductors and lower voltage delivered at the load. With PFC, the voltage drops are reduced.

- PFC can increase the efficiency of the LED driver. Both reactive power and distortion power produce extra current, which increase the energy lost in the driver and reduce the system efficiency.
- PFC can increase the capacity of the LED driver. When the system's power factor is improved, the amount of reactive current is reduced and more power can be drawn from the existing transformers and distribution lines.

Therefore, the exploration for PFC techniques in LED driver is highly desirable. Generally, there are two methods for correcting the power factor and suppressing harmonic distortion: the passive PFC method and the active PFC method. Passive PFC uses only line-frequency reactive components, while the active PFC uses active devices and high frequency reactive components.

In recent years, some topologies were developed to improve the power factor performance of LED driver, such as a high power factor single stage SEPIC converter working in DCM mode with universal input range [28, 31, 45, 46]. A quasi-active power factor correction circuit for LED lamp with high efficiency is presented in [47]. A single stage Flyback converter for hight brightness LED lamp is proposed to realize PFC function in [48]. In those topologies, near-unity power factor is realized.

B. Dimming control

Another important feature for the LED driver is the dimming control. This feature can optimize the consumption of electrical energy in LED lighting systems. For applications such as LCD backlighting, dimming provides brightness and contrast adjustment. Dimming white light LED systems can be accomplished by two techniques: continuous current reduction and pulse-width-modulation (PWM) [22, 49, 50, 53, 54]. With analog dimming, 80% brightness can be achieved by supplying 80% of the maximum current to the LED. Drawbacks of this method include LED color shift and the need for an analog control signal [51]. PWM dimming is achieved by applying full current to the LED at a reduced duty cycle. PWM is better because it can have a larger dimming range, and also can solve the problem of color shift [36, 52].

C. High Efficiency and low cost

Due to the market pressure, it is desirable that the cost of LED driver as low as possible [40]. In recent years, different topologies have been proposed to achieve high efficiency of ballast circuits for LEDs. A synchronously-rectified (SR) flyback converter with the proposed multi-function circuit is proposed in [29]. The proposed circuit can detect the zero crossing of the current to realize zero current switching (ZCS) in order to reduce switching loss. The proposed auxiliary circuit can work as a LC snubber and also a housekeeping circuit. And hence, this converter has high efficiency all over the operating and load range. In [55], a charge pump circuit for LED lamps is proposed. The series-charge and parallel-discharge operation gives the efficiency better than the conventional converters with ac line input since no magnetic components are adopted.

D. Long lifetime

Compared with other conventional lamps, an attractive feature of LEDs is longevity, which is typically 100,000 hours [56],. The lifetime expectancy is much longer than that of fluorescent lamps, which is typically 10,000 - 20,000 hours. Although LED lamps have longer lifetime than fluorescent lamps, the short lifetime limitation imposed by electrolytic capacitors in the LED driver has to be eliminated [57,58].

1.3.2 A topology study of the existing LED driver.

A number of topologies have been used as high brightness LED driver. As LEDs use low voltage DC source, hence the simple and common topologies can be used to drive LEDs [9].

Flyback converter is one of the most frequently used candidate for the low power LED driver especially when isolation is desirable [9, 20]. Working in discontinuous conduction mode (DCM), the input harmonics normally meets the IEC1000-3-2 standards. A Boost converter is suitable for high efficiency, large LED string applications where isolation is not mandatory [17, 24, 59, 60]. However, since boost converter can only step up the voltage, it is suitable for large strings of LEDs in series when the input is the AC mains.

The SEPIC converter has excellent power factor correction performance, but the efficiency is not comparable with the other solutions [28, 46]. It does not have a

transformer and the associated leakage ring effect as in a flyback converter so the voltage stress of active device in SEPIC is much lower than that in flyback converter. [45] proposes an interleaved SEPIC converter for the offline LED lighting applications. The magnetic components in this circuit are integrated to reduce cost and board space.

Cuk converter can drive LED at different input voltage range, from a universal input voltage or battery. The input and output inductors create a smooth current at both of the input and output of the converter, which can reduce the size and cost of EMI components, while the buck, boost and buck-boost have at least one side with pulsed current. [61] proposed a universal input digital controlled Cuk converter with both nonpulsating input current and nonpulsating output current.

For medium power applications, symmetrical and asymmetrical half bridge converters [31] can be used with high efficiency. The transformer runs in two quadrants, indicating better utilization of the magnetic core, and smaller size of the magnetic components for both the transformer and output inductor. Resonant converter has also been used to drive LEDs. [41] proposes resonant converter with high power density and very low switching losses for driving LEDs. Two stages converter for LED lamps can be integrated into single stage to further reduce the cost and gain high efficiency. An integrated single stage integrated Buck-Flyback Converter is proposed in [39].

1.4 Organization of the Thesis

The contents of this thesis are as follows:

In *Chapter 1*, a comprehensive overview on the lighting development will be

proposed. The characteristic of the light emitting diode (LED) lamp will be described. The requirements of the ballast for the light emitting diode (LED) lamp will be presented. The organization of the thesis will be described.

In *Chapter 2*, a single phase, power factor correction converter without electrolytic capacitors for LED lighting applications is proposed, which is a modified SEPIC converter working in discontinuous conduction mode (DCM). Different with a conventional SEPIC converter, the middle capacitor is replaced with a valley-fill circuit. The principle of the theory will be derived. The valley-fill circuit could reduce the voltage stress of output diode and middle capacitor under the same power factor condition, thus achieving higher efficiency. The proposed converter will be verified with experimental results.

In *Chapter 3*, an interleaved power factor correction SEPIC with valley fill circuit is proposed to further increase the efficiency and reduce the input and output filter size and cost. The proposed interleaved converter shows the features such as ripple cancellation, good thermal distribution and scalability. The proposed converter will be verified with experimental results.

Chapter 4 is the summary of the thesis.

CHAPTER 2

A SINGLE PHASE SEPIC WITH VALLEY FILLED CIRCUIT FOR LED APPLICATION

2.1 Introduction of SEPIC Converter

Single-ended primary-inductor converter (SEPIC) is a buck-boost derived converter, which could step down and step up the input voltage. Different with traditional buck-boost converter, SEPIC has non-inverting output. As shown in Fig 2.1 , the middle capacitor C1 works as coupling capacitor.

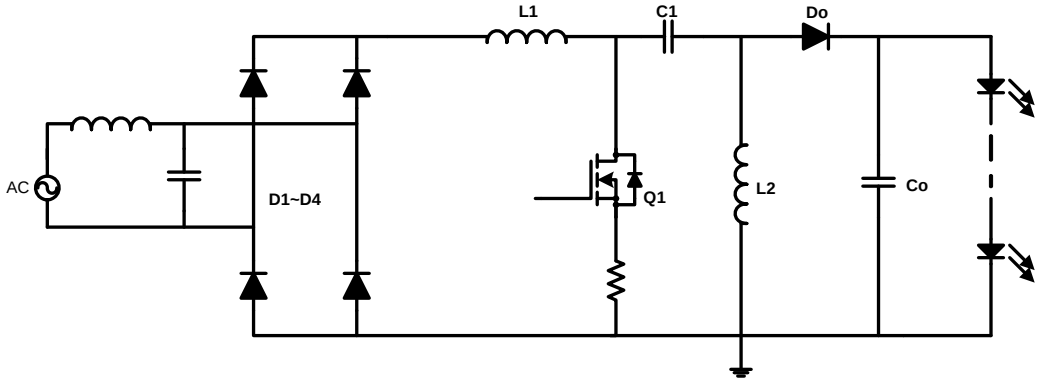


Figure 2.1 Offline SEPIC schematic

A SEPIC converter can work in continuous conduction mode (CCM) and Discontinuous conduction mode (DCM). In CCM steady state, since the average voltage across L_1 and L_2 is zero, the average voltage across coupling capacitor C_1 is input voltage (V_{in}). Since the average current flowing through C_1 is zero, the inductor L_2 is the only source of output current. The average current through inductor L_2 is the average

current of the load, which is independent of the input voltage.

In CCM, since the average voltage across the inductor L_1 and L_2 are both zero. Therefore, the voltage of middle capacitor will follow the input voltage and the middle capacitor has no low frequency energy storage function. Output capacitor takes the function of low frequency energy storage. Therefore, the output capacitance need be large to achieve a good output voltage regulation.

In CCM, since the voltage across the middle capacitor C_1 is the input voltage V_{in}, by applying voltage-second balance for inductor L_1 (neglecting the forward voltage drop of output diode), the output to input voltage ratio can be obtained as:

$$\frac{V_o}{V_{in}} = \frac{D}{1-D} \tag{2.1}$$

Therefore, SEPIC is a buck-boost derived converter. The inductor L_1 and Q_1 create the standard boost converter, which creates a voltage higher than input voltage and the magnitude is determined by the duty cycle of the MOSFET Q_1. Because the voltage across C_1 is V_{in}, the output voltage is V_{Q1}-V_{in}. If V_{Q1} is larger than two times of input voltage, the output voltage is greater than input voltage. Otherwise, it works as a step down converter.

The middle capacitor of SEPIC could be usually non-polarized capacitor such as Film capacitor because the voltage of the middle capacitor of SEPIC may reverse its direction in every switching circle. However, in some cases, the electrolytic capacitor could be used. In CCM, the electrolytic capacitor could be used since the capacitor

voltage ripple is relatively small.

In CCM SEPIC, since the average voltage across C_1 is V_{in}. The magnitude of voltage across L_1 and L_2 are the same so that they could be wound in the same core. And the mutual inductance is zero if the polarity of the windings is correct. Therefore, the two inductors are coupled and SEPIC can be seen as a similar flyback converter.

The small-signal model of SEPIC is required for building the SEPIC since the compensation depends on the control characteristics of SEPIC. Accurate small signal model for SEPIC is a difficult analytical task. There is a simplified analysis of the SEPIC converter [102], which neglects the parasitic resistances of inductors and capacitors.

Based on this simplified analysis, the control-to-output transfer function is obtained as below:

$$\frac{v_o(s)}{d(s)} = \frac{1}{D'^2} \frac{(1 - s \cdot \frac{L_1}{R} \cdot \frac{D^2}{D'^2})(1 - s \frac{C_1(L_1 + L_2)R \cdot D'^2}{L_1 \cdot D^2} + s^2 \frac{L_2 \cdot C_1}{D})}{\left(1 + \frac{s}{\omega_{o1} Q_1} + \frac{s^2}{\omega_{o1}^2}\right)\left(1 + \frac{s}{\omega_{o2} Q_2} + \frac{s^2}{\omega_{o2}^2}\right)} \tag{2.2}$$

where

$$\omega_{o1} \approx \frac{1}{\sqrt{L_2(C_1 + C_o) + L_1\left(C_o \cdot \frac{D^2}{D'^2} + C_1\right)}} \tag{2.3}$$

$$Q_1 \approx \frac{R}{\omega_{o1}\left(L_1 \cdot \frac{D^2}{D'^2} + L_2\right)} \tag{2.4}$$

$$\omega_{o2} \approx \frac{1}{\sqrt{\frac{1}{L_2 \cdot \frac{C_1}{D^2} \| \frac{C_o}{D'^2}} + \frac{1}{L_1 \cdot (C_1 \| C_o)}}} \tag{2.5}$$

$$Q_2 \approx \frac{R}{\omega_{o2} \cdot (L_1 + L_2) \cdot \frac{C_1}{C_o} \cdot \frac{\omega_{o1}^{\ 2}}{\omega_{o2}^{\ 2}}} \tag{2.6}$$

As shown in the Eq. (2.2), the SEPIC is fourth-order denominator converter. There are two double poles in CCM SEPIC. For numerator, the first term is a single right half plane zero (RHPZ). The second term is a complex RHPZ. RHPZs are a result of converters where the response to an increased duty cycle is to initially decrease the output voltage. When the power MOSFET is turned on, the inductor L1 is disconnected to the load. This generates the first RHPZ. Therefore, the expression only depends on the input inductor L1, the load resistor R, and the duty cycle, D. The complex RHP zeros correspond to the fact that the second inductor is disconnected to the load when the power MOSFET is turned on.

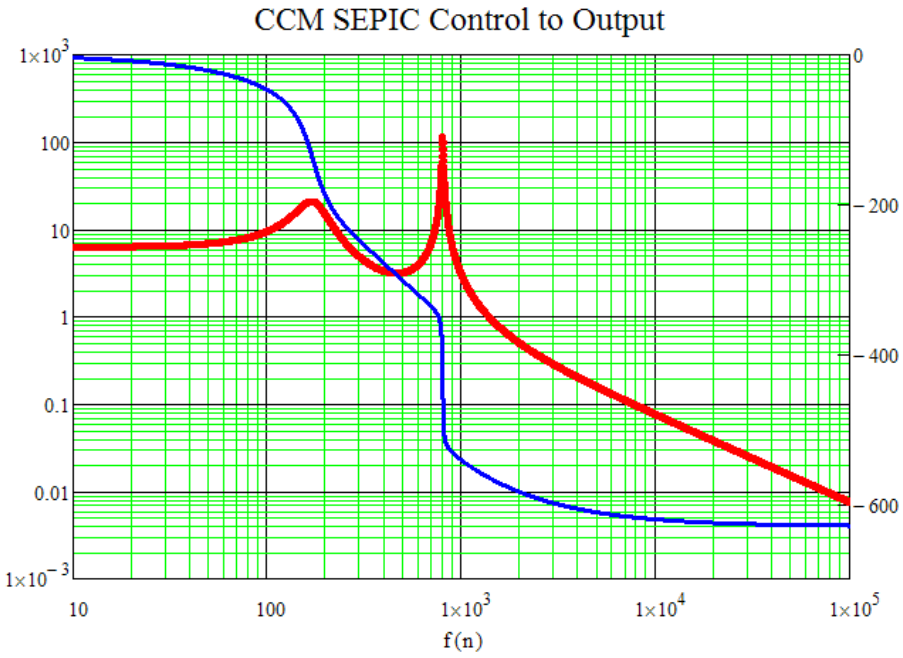


Figure 2.2 Bode plot of control to output transfer function of CCM SEPIC

Figure 2.2 shows the control to output transfer function in a typical CCM SEPIC design. The red curve is the magnitude and the blue curve is the phase of the transfer function. As shown in the Bode plot, there are two resonant frequency predicted in the Eq. (2.2).

With low values of damping resistors, the converters has four poles (i.e. two resonant frequency), and three right-half-plane-zeros. This generates large phase delay after the second resonant frequency, which is due to the delay of second resonance and the additional delay of the three RHPZ. Therefore, it is undesirable to control the converter at a frequency beyond the second resonance. Therefore, the bandwidth of the CCM SEPIC should be below the extreme phase delay of the second resonance

frequency.

2.2 Principle of DCM Operated SEPIC converter

As discussed above, the middle capacitor in CCM SEPIC has no line-frequency energy storage function and the output capacitance need be large to store the line frequency energy and suppress the low frequency voltage ripple for LED applications. Therefore, it is very difficult to eliminate the electrolytic capacitors in CCM SEPIC with low output voltage ripple, which is highly desirable for LED lighting application. For DCM operation of SEPIC, according to [45, 62], there are two types of DCM operation. The first one is defined as the current of the output diode is in continuous current mode or not. When the output diode current is zero, the inductor L_1 current and inductor L_2 current are not zero and equal to each other. In this case, the middle capacitor still has no low frequency energy storage function since its low frequency voltage still follows the input voltage due to continuous current of inductor L_1 and L_2. For the second type of DCM operation, which the inductor L_1 current and inductor L_2 current will both reach zero in a switching period. After the inductor L_1 current reaches zero, the voltage of middle capacitor will not follow input voltage any more and will have the low frequency energy storage function. Therefore, for the second type of DCM SEPIC, by allowing a relative large voltage ripple across the middle capacitor, the capacitance value of middle capacitor and output capacitor could be largely reduced thus eliminating the electrolytic capacitors.

However, the DCM SEPIC PFC converter has some drawbacks. When the input voltage is universal, the voltage stress for the middle capacitor and the output diode are very high. Therefore, a valley-fill circuit is added to the DCM SEPIC PFC converter.

2.3 Proposed DCM Operated SEPIC derived converter

2.3.1 Principle of Proposed DCM Operated SEPIC derived converter

By replacing the middle capacitor with the valley fill circuit in the typical SEPIC converter, a modified SEPIC is derived and is shown in Fig2.3. The valley fill circuit contains two capacitors and three diodes. The two capacitors are charged in series and are in parallel to feed the load. The converter operates at discontinuous current mode to realize the power factor correction automatically.

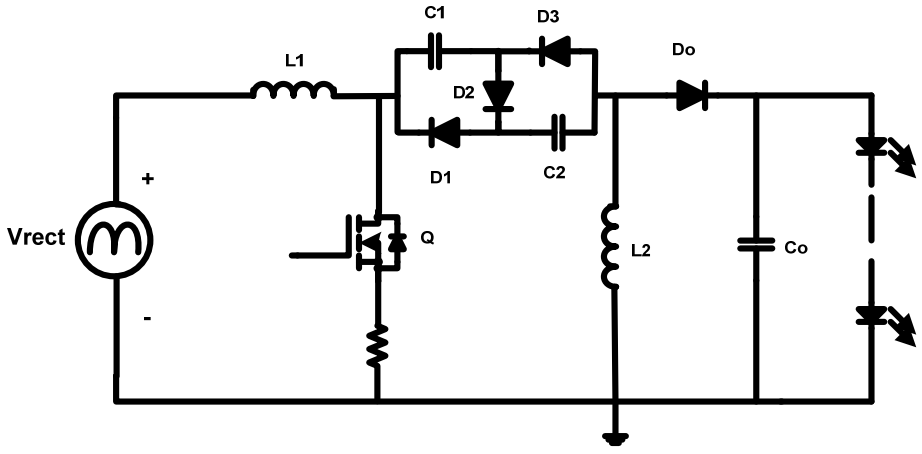


Figure 2.3 Proposed valley fill SEPIC PFC circuit

Some basic assumptions are made for the analysis of the proposed converter.

1) The input voltage V_{in} is pure sinusoidal waveform.

2) The capacitance of middle capacitor C_1 and C_2 and output capacitor C_o are large enough so that in a switching period T_s, the voltage across these capacitors: V_{c1},V_{c2}, and V_o could be assumed to be constant.

3) All of the MOSFET and diodes, inductors, capacitors are ideal without any parasitic components.

4) The inductors L_1 and L_2 both work in discontinuous conduction mode (DCM). The current of inductor L_1 reaches zero before current of inductor L_2 reaches zero.

Fig 2.4 shows the steady state current waveforms of proposed converter. There are four intervals during one switching period:

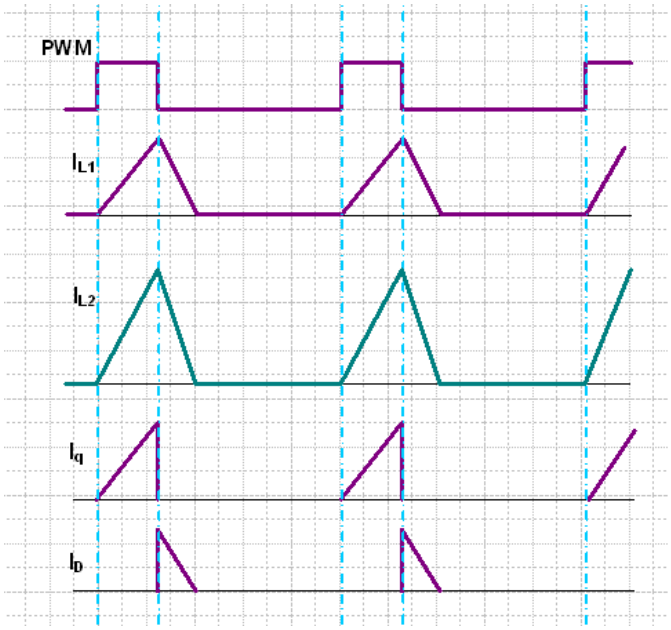
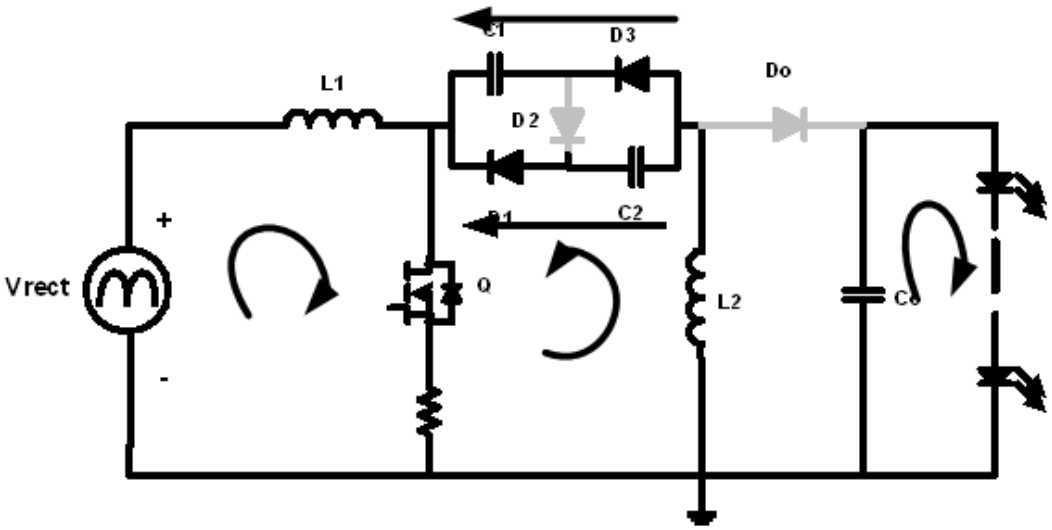
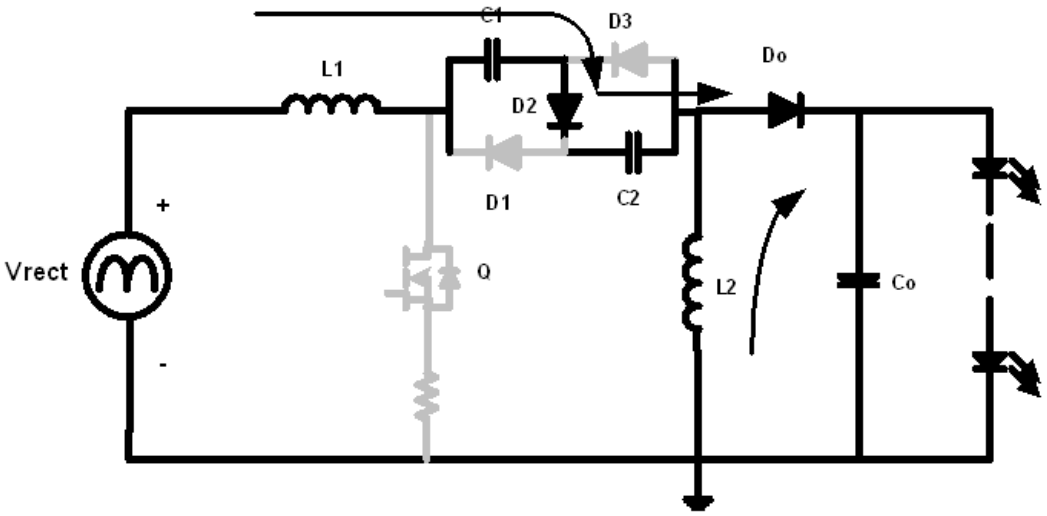


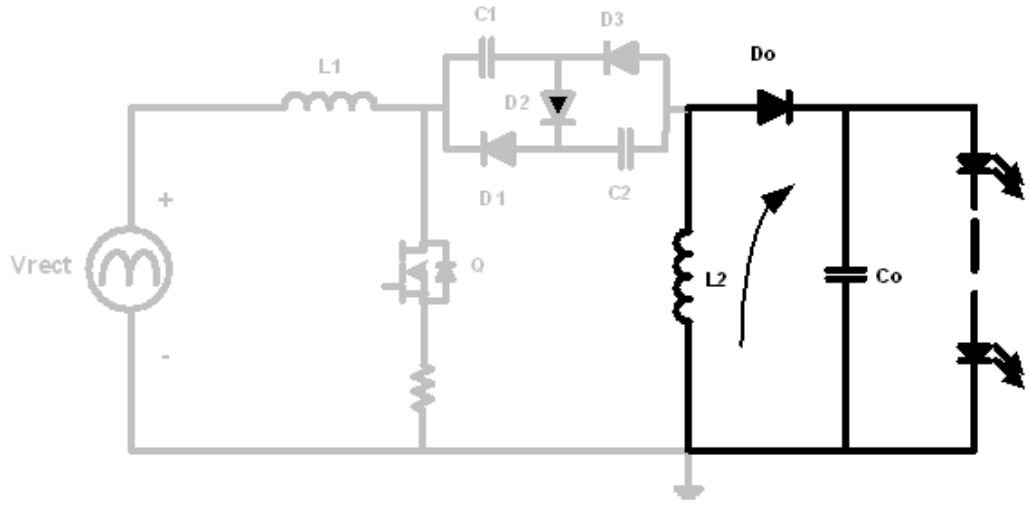
Figure 2.4 The steady state current waveforms of proposed converter



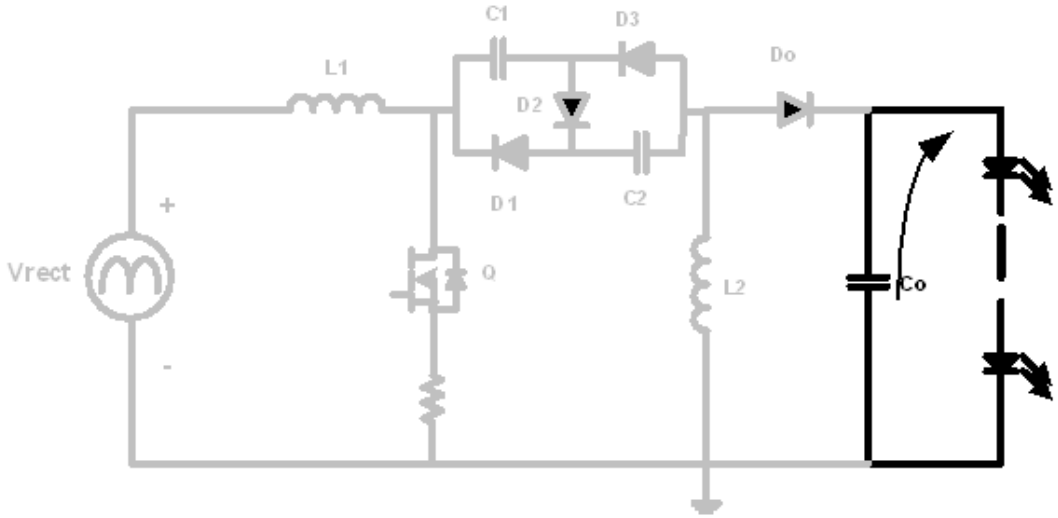
(a) Interval [t0,t1]



(b) Interval [t1,t2]



(c) Interval [t2,t3]



(d) Interval [t3,t4]

Figure 2.5 Equivalent circuit during different intervals

1) **Interval [t0,t1]:** The switch turns on for a period of T_{on}, and the output diode is off. Inductors L_1 are charged by the input voltage and the two capacitors C_1, C_2 in the valley fill circuit are connected in parallel to feed the inductor L_2. Both of the inductor currents

ramp up linearly. Therefore, the currents of L_1 and L_2 are given in (2.7), (2.8). The MOSFET current is the sum of the two inductor currents, and is given in (2.9).

$$i_{L1}(t) = \frac{V_{in}}{L_1} \cdot t \tag{2.7}$$

$$i_{L2}(t) = \frac{V_{c1}}{L_2} \cdot t \tag{2.8}$$

$$i_Q(t) = i_{L1}(t) + i_{L2}(t) \tag{2.9}$$

2) **Interval [t1,t2]:** The switch turns off, and the diode is on for a period. Both inductor currents freewheel through the diode and the inductor L_1 and L_2 currents ramp down linearly. The two capacitors C_1, C_2 in the valley fill circuit are charged in series by the inductor L_1 current. At the end of this interval, the current of inductor L_1 reaches zero. The L_1 current reduces according to (2.10). The L_2 current reduces according to (2.11). The diode current is the sum of both the inductor currents, as shown in (2.12).

$$i_{L1}(t) = \frac{V_{in}}{L_1} \cdot D_1 \cdot T_s + \frac{V_{in} - 2 \cdot V_{c1} - V_o}{L_1} \cdot t \tag{2.10}$$

$$i_{L2}(t) = \frac{V_{c1}}{L_2} D_1 \cdot T_s - \frac{V_o}{L_2} \cdot t \tag{2.11}$$

$$i_D(t) = i_{L1}(t) + i_{L2}(t) \tag{2.12}$$

3) **Interval [t2,t3]:** After the current of inductor L_1 reaches zero, the inductor L_2 continues to freewheel through the output diode. This interval does not end until the current of inductor L_2 reaches zero.

4) **Interval [t3,t4]:** Both the switch and the output diode are off for a period of T_{off}. The output capacitor C_o continues to charge the load.

Apply the voltage-second balance to the inductor L_1:

$$D_1 \cdot V_{in} \cdot \sin(\omega_l t) = D_2 \cdot (2 \cdot V_{c1} + V_o - V_{in} \cdot \sin(\omega_l t)) \tag{2.13}$$

Since the proposed SEPIC PFC converter works in DCM, the inductor L_1 and L_2 peak current in a switching cycle is derived as:

$$i_{L1\_pk} = V_{in}\sin(\omega_l t)\frac{D_1 \cdot T_s}{L_1} \tag{2.14}$$

$$i_{L2\_pk} = V_{c1}\frac{D_1 \cdot T_s}{L_2} \tag{2.15}$$

As shown in the equation(2.14), the peak current envelope of inductor L_1 is sinusoidal waveform.

The average inductor current in a switching cycle is derived as:

$$i_{L1\_av(t)} = \frac{1}{2}\cdot i_{L1\_pk}\cdot(D_1 + D_2) = \frac{\left|\sin(\omega_l t)\right| V_{in}\cdot D_1^{\,2}}{2f_s \cdot L_b \cdot (1 - \frac{V_{in}\cdot\left|\sin(\omega_l t)\right|}{2\cdot V_{c1} + V_o})} \tag{2.16}$$

So the input current is:

$$i_{in(t)} = \frac{\sin(\omega_l t) V_{in}\cdot D_1^{\,2}}{2f_s \cdot L_b \cdot (1 - \frac{V_{in}\cdot\left|\sin(\omega_l t)\right|}{2\cdot V_{c1} + V_o})} \tag{2.17}$$

The input current is normalized with a base of $\frac{V_{in}\cdot D_1^{\,2}}{2f_s \cdot L_b}(1 - \frac{V_{in}}{2\cdot V_{c1} + V_o})$ for simpler analysis. Then the normalized input current is obtained as:

$$i_{in(t)}^{\,*} = \frac{\sin(\omega_l t)}{(1 - m\cdot\left|\sin(\omega_l t)\right|)}\cdot(1-m) \tag{2.18}$$

where

$$m = \frac{V_{in}}{2\cdot V_{c1} + V_o} \tag{2.19}$$

The normalized input current is plotted in Fig 2.6. The input current distortion is caused by the ratio m. The larger the ratio is, the worse the distortion of input current is.

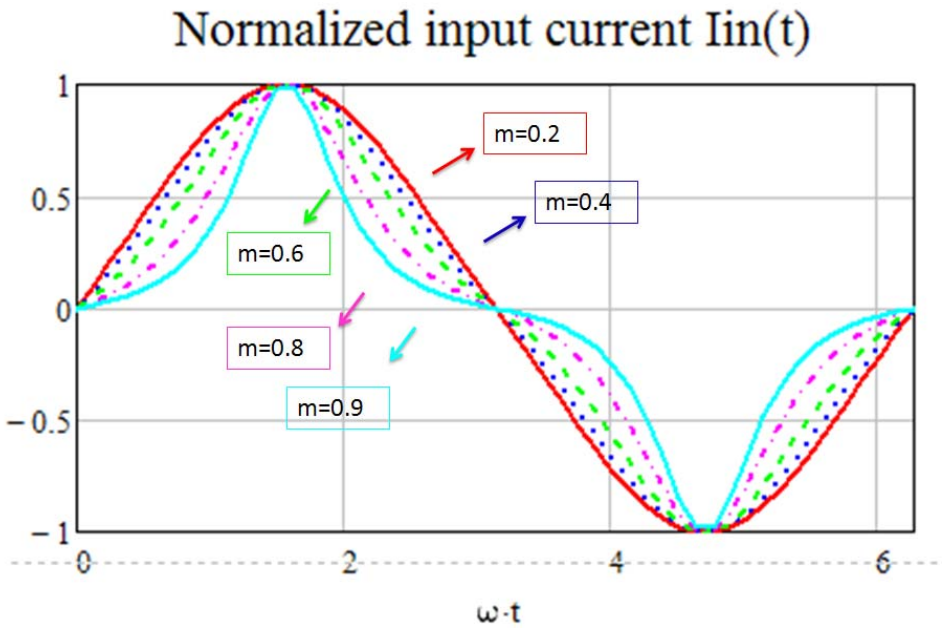


Figure 2.6 Normalized input current versus ratio *m*

As can be seen in the Fig 2.6 above, the ratio: $V_{in}/(2V_{c1}+V_o)$ has a great influence on the distortion of the input current. The higher ratio leads to a poorer distortion. This is because if the ratio is higher, the falling time of input current is longer. Since the average value of input current in falling time is not a sinusoid waveform. The falling time is shorter and thus the input current waveform is closer to the sinusoid waveform.

The average of input power over one ac line cycle is obtained as:

$$P_{in}=\frac{1}{\pi}\int_0^{\pi} i_{in}(t)\cdot v_{in}(t)dt=\frac{1}{\pi}\int_0^{\pi}\left(\frac{\sin(\omega_l t)V_{in}\cdot D_1^{\,2}}{2f_s\cdot L_b\cdot\left(1-\frac{V_{in}\cdot\left|\sin(\omega_l t)\right|}{2\cdot V_{c1}+V_o}\right)}\right)\cdot V_{in}\sin(\omega_l t)\,dt$$

$$=\frac{V_{in}^{\,2}\cdot D_1^{\,2}}{2\pi L_b f_s}\int_0^{\pi}\left(\frac{\sin^2(\omega_l t)}{\left(1-\frac{V_{in}\cdot\left|\sin(\omega_l t)\right|}{2\cdot V_{c1}+V_o}\right)}\right) \qquad (2.20)$$

The power factor is defined as the ratio of real power over apparent power. So the power factor is obtained as:

$$PF = \frac{\frac{1}{\pi}\int_0^{\pi} i_{in}(t)\cdot v_{in}(t)dt}{V_{RMS}\cdot\sqrt{\frac{1}{\pi}\int_0^{\pi} i_{in}(t)^2 dt}} = \frac{\sqrt{2}\int_0^{\pi}\frac{(\sin\omega t)^2}{1-\frac{V_{in}|\sin\omega t|}{2V_{c1}+V_o}}}{\sqrt{\frac{1}{\pi}\int_0^{\pi}\frac{(\sin\omega t)^2}{\left(1-\frac{V_{in}|\sin\omega t|}{2V_{c1}+V_o}\right)}}} \tag{2.21}$$

As can be seen in the equation above, the power factor is a function of the ratio: $(2V_{c1}+V_o)/V_{in}$. The power factor function is plotted in Fig 2.7. The result shows that a lower ratio leads to a better power factor. Therefore, for the same input voltage and output voltage, the power factor is determined by the average middle capacitor voltage V_{c1}, by neglecting the voltage ripple across the middle capacitor.

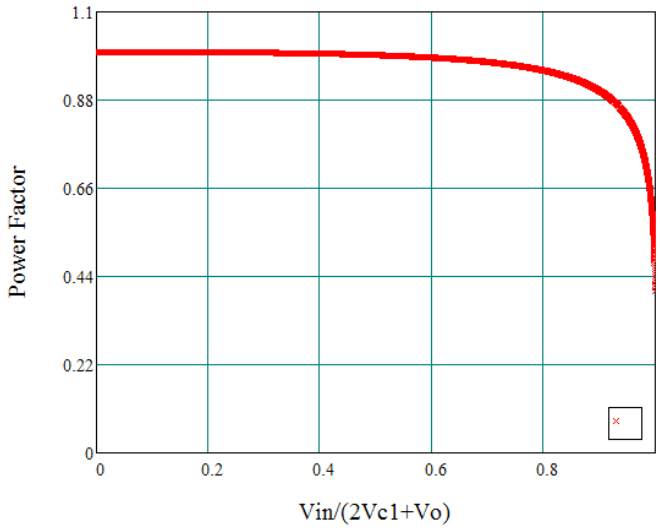


Figure 2.7 The power factor as a function of $V_{in}/(2V_{c1}+V_o)$

Assuming the efficiency of the converter is η. So:

$$P_{in}\cdot\eta = P_o \tag{2.22}$$

According to the equ(2.22), the duty cycle D_1 can be calculated as:

$$D_1 = \frac{1}{V_{in}} \sqrt{\frac{P_o \cdot L_b \cdot f_s \cdot 2\pi}{\eta \cdot \int_0^{\pi} \frac{(\sin \omega t)^2}{\left(1 - \frac{V_{in}|\sin \omega t|}{2V_{c1} + V_o}\right)}}} \tag{2.23}$$

According to the charge balance of middle capacitor C_1:

$$\frac{1}{2} \cdot \left(\frac{i_{L2\_pk}}{2} \right) \cdot D_1 \cdot T_s = \frac{1}{2} \cdot \left(i_{L1\_pk} \right) \cdot D_2 \cdot T_s \tag{2.24}$$

Where

$$i_{L2\_pk} = V_{c1} \frac{D_1 \cdot T_s}{L_2} \tag{2.25}$$

$$i_{L1\_pk} = V_{in} \sin\left(\omega_l t\right) \frac{D_1 \cdot T_s}{L_1} \tag{2.26}$$

Therefore,

$$\frac{1}{2} \cdot \left(\frac{V_{c1} \frac{D_1 \cdot T_s}{L_2}}{2} \right) \cdot D_1 \cdot T_s = \frac{1}{2} \cdot \left(V_{in} \sin\left(\omega_l t\right) \frac{D_1 \cdot T_s}{L_1} \right) \cdot D_2 \cdot T_s$$

$$\frac{L_2}{L_1} = \frac{V_{c1} \cdot D_1}{2 \cdot V_{in} \cdot \sin\left(\omega t\right) \cdot D_2} \tag{2.27}$$

According to equ(2.13),

$$\frac{L_2}{L_1} = \frac{V_{c1} \cdot (2 \cdot V_{c1} + V_o - V_{in} \cdot \sin\left(\omega_l t\right))}{2 \cdot {V_{in}}^2 \cdot \sin^2\left(\omega t\right)} \tag{2.28}$$

Average equ(2.28) over the ac line period, (2.29) can be derived.

$$\frac{L_2}{L_1} = \frac{V_{c1}}{2\pi \cdot {V_{in}}^2} \int_0^{\pi} \frac{(2 \cdot V_{c1} + V_o - V_{in} \cdot \sin\left(\omega_l t\right))}{\sin^2\left(\omega_l t\right)} d\omega t \tag{2.29}$$

From this equation, three conclusions could be made:

1) The ratio of L_2/L_1 is independent of the duty cycle D_1

2) The higher the ratio of L_2/L_1, the larger the middle capacitor voltage V_{c1}.

3) The voltage across the middle capacitor C_1 and C_2 is independent of load.

Assuming the power factor is unity, the desired instantaneous load power is not equal to the desired instantaneous input power. Therefore, some elements within the system must supply or consume the difference between the instantaneous input power and output power. In this proposed converter, the middle decoupling valley-fill capacitors C_1 and C_2 works as a low-frequency energy storage element. The difference between the instantaneous input power and instantaneous output power flows through the capacitors. When the instantaneous input power is larger than instantaneous output power, the energy flows into the capacitors, and voltage of the capacitors increase. Likewise, when the instantaneous input power is lower than instantaneous output power, the energy is released by the capacitors, and voltage of the capacitors decrease, as shown in Fig 2.8.

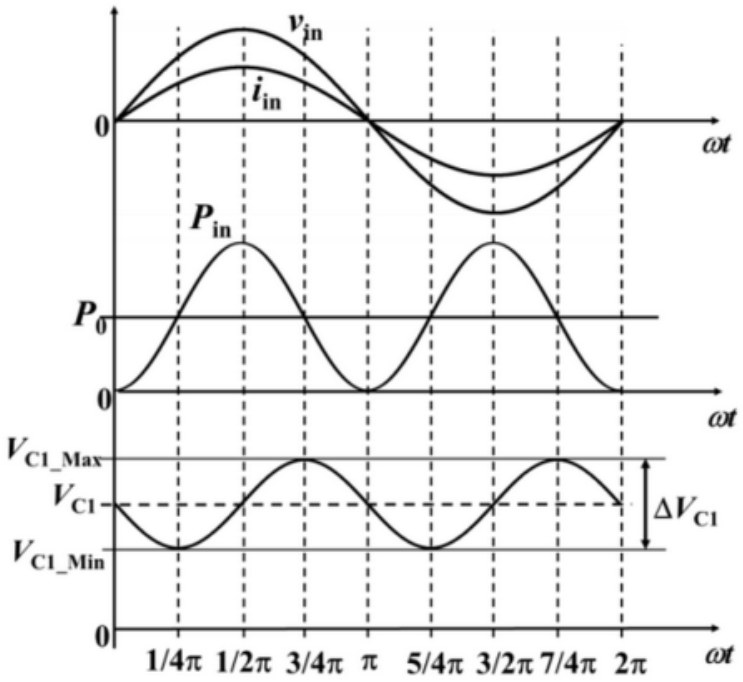


Figure 2.8 The middle capacitor voltage over the ac line period

Assuming the power factor is unity and no input current distortion, the instantaneous input power is obtained as:

$$P_{in}(t) = V_{in}(t) \cdot I_{in}(t) = V_m \sin(\omega t) \cdot I_m \sin(\omega t) = \frac{V_m \cdot I_m}{2}\left[1 - \cos(2\omega t)\right] \tag{2.30}$$

The average of input power over ac line period is the output power, therefore:

$$P_o = \frac{V_m \cdot I_m}{2} \tag{2.31}$$

The stored energy of capacitor C_1 in valley-fill circuit is

$$\Delta E = \frac{1}{2} C_1 \cdot V_{\max}{}^2 - \frac{1}{2} C_1 \cdot V_{\min}{}^2 \tag{2.32}$$

According to Fig 2.8, the difference between the instantaneous input power and instantaneous output power is obtained as:

$$\Delta E = \int_{\frac{1}{4}\pi}^{\frac{3}{4}\pi} P_{ac}(t)dt = \frac{P_o}{\omega_{line}} \tag{2.33}$$

Thus the energy stored in each capacitor in valley-fill circuit is obtained as:

$$\Delta E_{c1} = \Delta E_{c2} = \frac{1}{2}\int_{\frac{1}{4}\pi}^{\frac{3}{4}\pi} P_{ac}(t)dt = \frac{P_o}{2\cdot\omega_{line}} \tag{2.34}$$

According to equ(2.32),(2.34):

$$\frac{P_o}{2\cdot\omega_{line}} = \frac{1}{2}C_1\cdot V_{\max}{}^2 - \frac{1}{2}C_1\cdot V_{\min}{}^2 \tag{2.35}$$

The low frequency voltage ripple of V_{c1} and V_{c2} can be derived:

$$\Delta V = \frac{P_o}{2\cdot\omega_{line}\cdot V_o\cdot C_1} \tag{2.36}$$

Therefore, the voltage ripple of the middle capacitor is determined by the average voltage and capacitance of the middle capacitor, for the same output power.

In the typical PFC, since usually the output capacitor takes the responsibility of low-frequency energy storage, the capacitance need be large so that the low- frequency ripple of output voltage is as low as possible, especially for LED application. In LED application, a small output voltage variation could lead to large output current variation. However, for the proposed SEPIC converter, it is unnecessary that the output capacitance is large because DCM operation makes the middle valley-fill capacitors work as low frequency energy storage capacitors rather than the output capacitor, thus minimizing the need for the low-frequency capacitance since the voltage ripple of middle valley-fill capacitors could be large. Therefore, by working at DCM and

allowing a relative large voltage ripple across the middle capacitors in valley-fill circuit, it can eliminate the electrolytic capacitors in the proposed converter while maintaining high power factor and good output regulation.

2.3.2 The Voltage and Current Stress of the devices and components.

According to the operating principle discussed above, the maximum voltage stress for the MOSFET Q_1 can be estimated as:

$$V_{q1\_\max} = V_{c1\_\max} + V_{c2\_\max} + V_o = 2 \cdot V_{c1\_\max} + V_o \tag{2.37}$$

V_{c1_max} and V_{c2_max} is the maximum voltage of middle capacitor C_1 and C_2.

Since some parasitic ringing may be observed during MOSEFT turn-off transient, 20%-30% margin for voltage stress need be considered for the selection of the MOSFET Q_1.

The maximum voltage stress for the output diode D_o is

$$V_{do\_\max} = V_{c1\_\max} + V_o = V_{c2\_\max} + V_o \tag{2.38}$$

Since the maximum current of inductor L_1 and L_2 happens at the peak voltage of maximum input line, the maximum current stress for MOSFET Q_1 is obtained as:

$$I_{Q1\_\max} = I_{L1\_\max} + I_{L2\_\max} = \frac{\left(V_{HL\_PK} \cdot D_{\min}\right) T_s}{L_1} + \frac{\left(V_{c1\_\max\_HL} \cdot D_{\min}\right) T_s}{L_2} \tag{2.39}$$

I_{L1_max} is the maximum current of inductor L_1, and I_{L2_max} is the maximum current of inductor L_2. V_{HL_PK} is the peak voltage of maximum input line, D_{min} is the duty cycle under the peak voltage of maximum input line condition. $V_{c1\_max\_HL}$ refers to the middle capacitor voltage under this condition.

The current stress for the output diode D_o is obtained as:

$$I_{Do\_\max} = I_{L1\_\max} + I_{L2\_\max} = \frac{\left(V_{HL\_PK} \cdot D_{\min}\right)T_s}{L_1} + \frac{\left(V_{c1\_\max} \cdot D_{\min}\right)T_s}{L_2} \tag{2.40}$$

Therefore, both Q_1 and D_o carry the sum of the maximum current of inductor L_1 and L_2. The maximum current of inductor L_1 and L_2 happens at the peak voltage of high input line. Therefore, the selection for the output diode should be based on this equation.

According to the operation principle of the proposed converter, the voltage stress of the diodes D_1-D_3 in the valley fill circuit is V_{c1_max}. The current stress for diode D_2 is the peak current of inductor L_1. The current stress for diodes D_1 and D_3 is the one half of peak current of inductor L_2.

The voltage stress for the middle capacitor C_1 and C_2 can be calculated in equ(2.29) under the peak of maximum input voltage.

The valley-fill circuit could reduce the voltage stress of output diode and middle capacitor under the same power factor condition, thus achieving higher efficiency.

2.4 Experimental Results

A 60W prototype has been built in the Lab and tested to verify the design. The operating conditions are:

Input Voltage V_{in}: 130V

Line Frequency: 60Hz

Output Voltage: 50V

Switching Frequency(f_{sw}): 60kHz

Maximum Output Power(P_o): 60W

The main circuit component values and parameters are given according to the design equations above, and given in Table 2.1.

Table 2.1 Summary of selected components.

Inductor L1	L1: 180uH PQ3220 Core
Inductor L2	L2: 120uH,PQ3220 Core
MOSFET	STB12NM60N, 600V,10A.
Output Diode	Schottky, PDS4150 150V,4A
Rectifier Diode Bridge	S3G, 400V, 3A
Diodes in Valley-fill Circuit	Schottky, SS28,80V,2A
Capacitors in Valley-fill	Cap 16uF,300V Film Polyester
Output Capacitor	Cap 15uF,63V,Metal Polyester
Controller	UCC3844

Some of the key waveforms at 100% load are shown in Fig2.9-Fig2.12. It can be seen that the input current follows the input voltage. The input current distortion is very

small. The power factor measured at the full load is 0.95. The measured input current harmonics at full load and at 110V input voltage are compared with the harmonics standards IEC 61000-3-2 Class C, which is the harmonics standard for lighting applications. As shown in the Figure 2.13, the results show that the individual harmonics are within the IEC 61000-3-2 Class C limits.

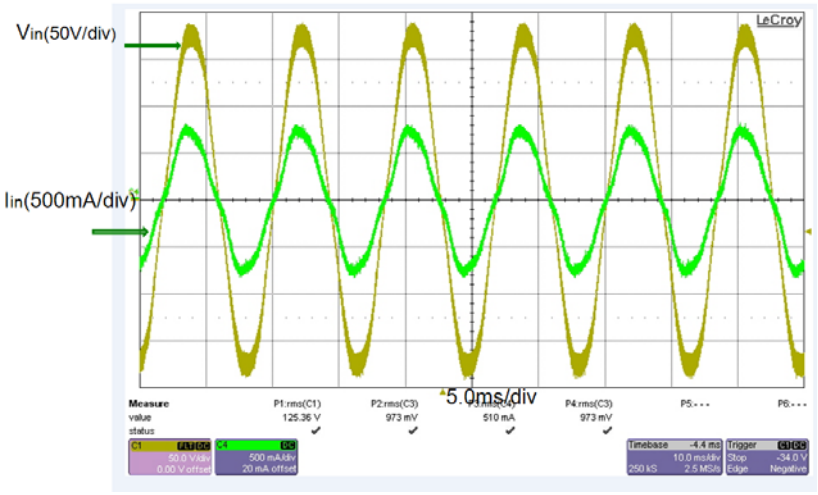


Figure 2.9 Input current(500mA/div) and input voltage (50V/div)

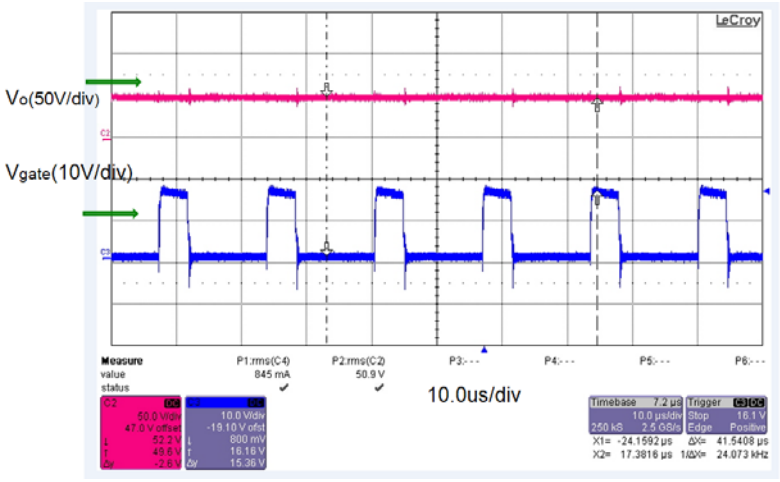


Figure 2.10 Gate driving signal (10V/div), output voltage(50V/div)

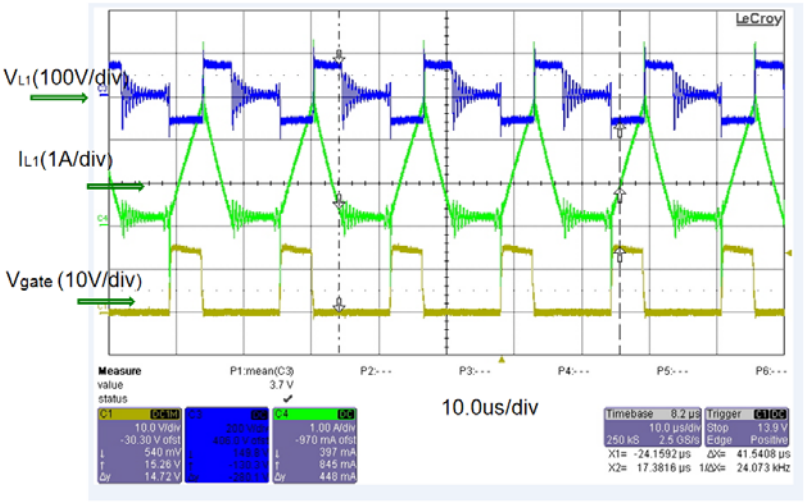


Figure 2.11 Gate driving signal (10V/div), inductor L_1 current(1A/div) and voltage(100V/div)

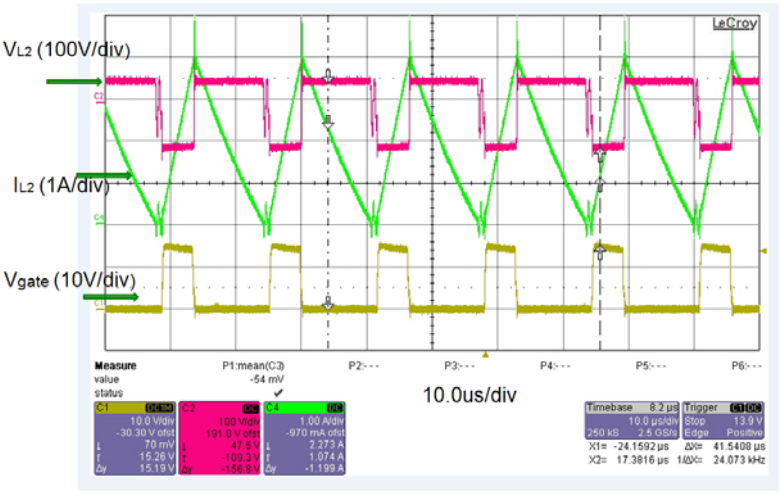


Figure 2.12 Gate driving signal (10V/div), inductor L_2 current(1A/div) and voltage(100V/div)

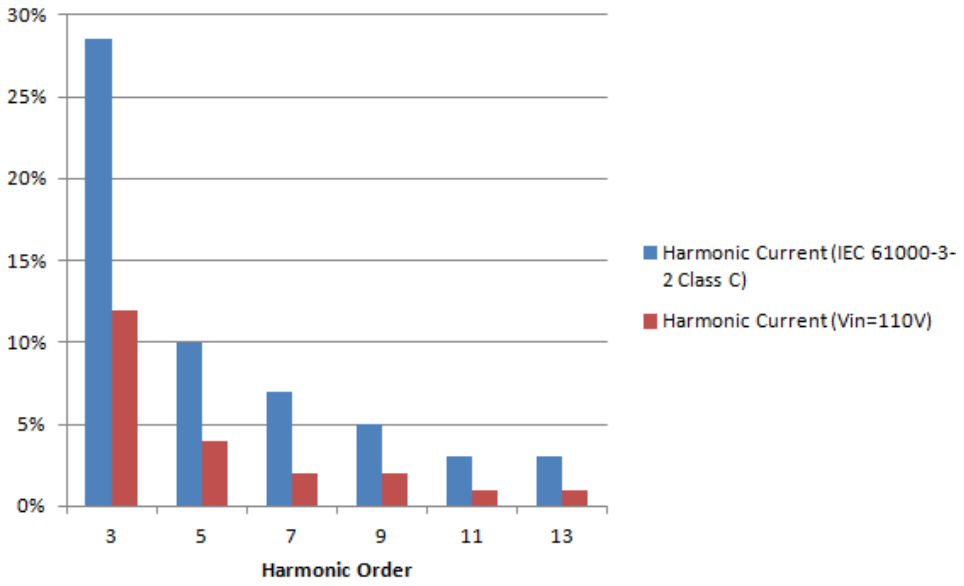


Figure 2.13 Measured input current individual harmonics compared with IEC 61000-3-2 Class C standard

2.5 Loss Distribution

In order to obtain higher efficiency, we have to estimate the power losses distribution for each component in the proposed SEPIC converter and figure out which parts cause majority of the power losses and how to reduce the unnecessary losses.

In the proposed SEPIC converter, power losses normally consist of two types: conduction losses and switching losses. The conduction losses include power switch conduction loss, diode conduction losses, SEPIC inductor copper losses, capacitor ESR losses, and other stray resistive losses. The switching losses include power switch switching loss. The majority of the power losses in the SEPIC converter are due to the

losses in inductors and MOSFET.

2.5.1 Inductor Losses

The power losses of inductor L_1 and L_2 include core loss and copper loss. Magnetic materials exhibit core loss, due to the low frequency hysteresis of the B-H loop and to the induced high frequency eddy currents flowing in the core material. The physics of core loss is extremely complex. No one has yet produced an analysis that allows us to predict core loss from material structure and chemical makeup. All core loss data is strictly empirical. There is an Empirical equation for core loss calculation. Constant coefficients are assigned to a, c, d. It is just curve fitting to the empirical data.

$$P_{fe\_density} = a \cdot \left(f_{sw}\right)^{c} \cdot \left(\Delta B\right)^{d} \tag{2.41}$$

Where f_{sw} is kHz and the flux density ΔB is in Tesla, a, c, d are curve fitting parameters that depend on the type of the core material. Over a small range of frequencies, this empirical equation works reasonably well.

Therefore, the total core loss is obtained:

$$P_{fe} = P_{fe\_density} \cdot V_e \tag{2.42}$$

V_e is the volumn of the magnetic core.

The copper losses of the inductors include the DC copper loss and high frequency proximity effect caused loss. To eliminate the proximity losses, Litz wire is used in the inductors. Many strands of small gauge insulted copper wire are bundle together, and are externally connected in parallel. To be effective, the diameter of the strands should

be sufficiently less than one skin depth.

Therefore, the DC copper losses for the inductor are:

$$P_{cu} = I_{rms}{}^2 \cdot R \tag{2.43}$$

2.5.2 MOSFET Losses

The power loss in any MOSFET is the combination of the switching losses and the MOSFET's conduction losses:

$$P_{MOSFET} = P_{SW} + P_{COND} \tag{2.44}$$

The calculation of conduction loss is straightforward as specified in equ(2.45) below:

$$P_{COND} = \left(I_{ds}{}^{rms}\right)^2 R_{ds\_on} \tag{2.45}$$

Where R_{ds_on} is the conduction resistance at the maximum operating MOSFET junction temperature, and I_{ds_rms} is RMS current of MOSFET.

For discontinuous conduction mode (DCM), there is no reverse recovery issue no matter what kinds of output diodes are used, thus no reverse recovery loss in the MOSFET caused by the diodes. The total switching losses for MOSFET is obtained as:

$$P_{SW\_TURNON} = \frac{1}{2} T_{on} V_{ds} I_{ds\_on} f_{sw} + \frac{1}{2} T_{off} V_{ds} I_{ds\_off} f_{sw} \tag{2.46}$$

Where T_{on} is the turn on time in one switching period, I_{ds_on} is the MOSFET current at the moment of its turn-on, T_{off} is the turn off time in one switching period, I_{ds_off} is the MOSFET current at the moment of its turn-off. V_{ds} is the drain to source voltage of MOSFET, and f_{sw} is the switching frequency.

2.5.3 Diode Losses

The rectifier diode forward voltage drop is a dominant factor determining the power supply efficiency. The condition loss of the diode is average current of diode times the forward voltage drop of the diode. Therefore, the conduction losses of the diodes in valley-fill circuit can be calculated. Since the average current of the output capacitor is zero. Therefore, the average current of the output diode is the output current.

$$P_{COND} = V_F \cdot I_o \tag{2.47}$$

Where V_F is the forward voltage of the output diode.

Since the input is the AC line, conduction losses occur in the input bridge rectifier diodes. The total power loss in the input bridge rectifier is obtained as:

$$P_{input\_rectifier} = 4 \cdot V_{F\_rectifier} \cdot I_{av\_rectifier} \tag{2.48}$$

Where $V_{F\_rectifier}$ is the forward voltage drop of each input diode in the diode bridge rectifier and $I_{avg\_rectifier}$ is the average forward current for each diode in the bridge rectifier.

After the power loss calculations, the power loss distribution is given in Fig.2.14. The efficiency results at different load conditions are given in Table.2.2. Plot these efficiency data and efficiency with different load curve is obtained as shown in Fig 2.15.

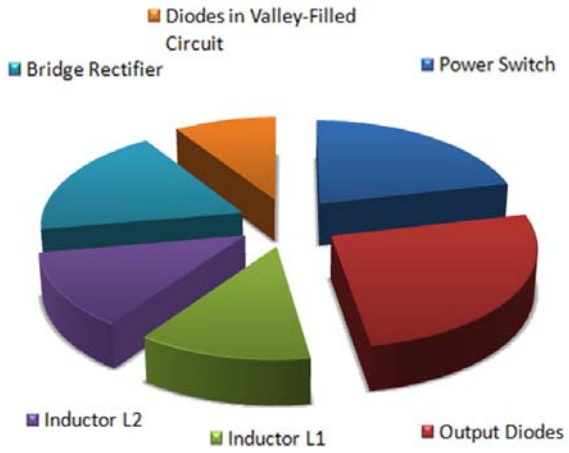


Figure 2.14 The power loss distribution of the proposed SEPIC converter

Table 2.2 Efficiency results at different load conditions

60-W Load Test Results	V_{inRMS} (V)	I_{inRMS} (mA)	V_{bus} (V)	I_o (mA)	η (%)
20%	125.1	114.9	49.98	240	83.5
40%	125.3	213.1	49.83	480	89.6
60%	125.4	312.8	49.74	720	91.3
80%	125.2	415.1	49.65	960	91.7
100%	125.5	517.9	49.51	1200	91.4

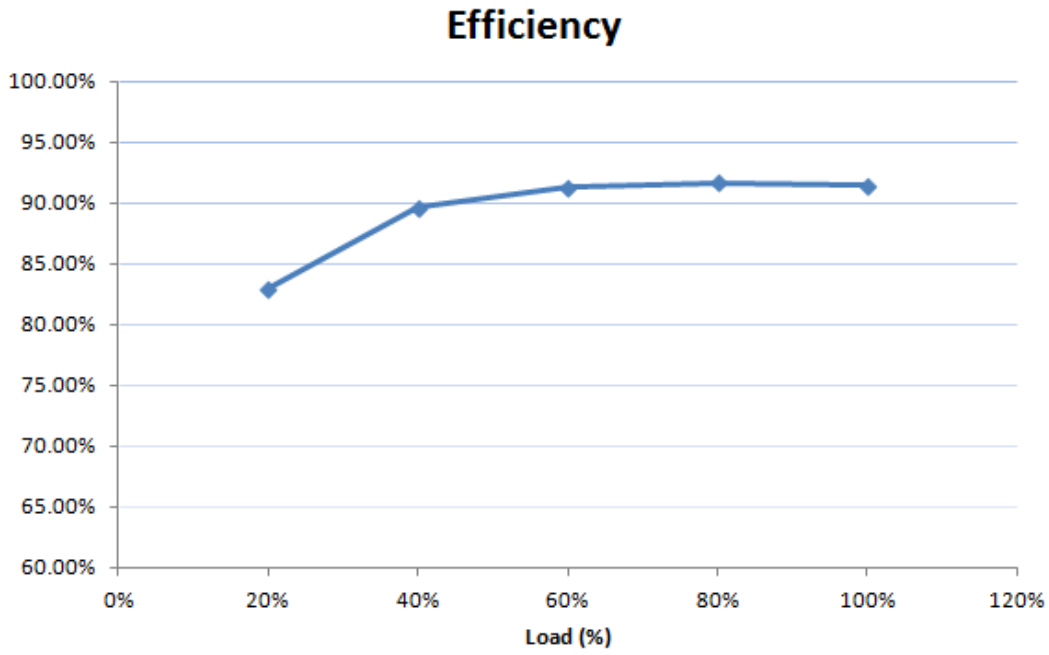


Figure 2.15 Efficiency curve at different load conditions

2.6 Chapter Summary

A single phase valley-fill SEPIC PFC converter is proposed for LED lighting application. By adding a valley-fill circuit into the DCM operation SEPIC, the converter can eliminate the electrolytic capacitors and reduce the voltage stress of output diode and middle capacitors under the same power factor condition.

CHAPTER 3

INTERLEAVED SEPIC WITH VALLEY FILLED CIRCUIT FOR LED APPLICATION

3.1 Introduction of interleaving technique

Interleaving technology has been applied to many applications in the field of power electronics, especially in high power applications. Since in high power application, the voltage and current stress of the device can go beyond the limit so that the power device cannot handle. In this case, paralleling the devices can provide the solution, but one major concern of this solution is the current sharing and voltage sharing. There is another solution, which is paralleling the converters instead of power devices. By paralleling the converters and making each channel a phase shift, the interleaved converter can be proposed and some beneficial features such as ripple cancellation and better thermal performance can be achieved.

In lower power level, such as SMPS power stage architecture, the interleaving technique can also be applied. In such applications, some concerns have been listed below

1. The ESRs of the input and output filter capacitors cause large heat dissipation from the high switching pulsed current. Interleaving multiple converters can

significantly reduce the ripple current of the input capacitors and output capacitors so that reduce the thermal stress of the capacitors.

2. N-channel interleaved converter increases the ripple frequency to be n times the individual switching frequency. Since the ESR of the tantalum capacitors is inversely proportional to the frequency. Therefore, interleaving technique can effectively reduce the filter capacitor size and weight.
3. In the case that higher power levels are required than the initial design at the beginning. Higher power levels can be achieved with interleaved converter by adding additional identical modules.

Therefore, the interleaving technique has been investigated and applied to many applications. The multi-phase/interleaved buck converter for Voltage Regulator (VR) application has been mostly investigated and explored [63-65].

3.2 Review of Multi-Phase Buck for VR Application

A Voltage Regulator Module (VRM) is a buck converter that can provide the CPU supply voltage, which converts +5V or +12V to a lower voltage required by CPU.

For the older generation microprocessor VR, the single phase synchronous buck topology is widely adopted, as shown in Fig3.1 [63]. However, although the output voltage of the VR tends to drop, the output current increases a lot so that the total power consumptions of CPU increase continuously. It is impossible for a single buck converter to handle such large current stress and power consumption. Naturally the devices are

paralleled to handle the high current stress, as shown in Fig3.2. The bulk capacitors are used for energy storage and the decoupling capacitors are used to limit the voltage spike during load transient. Due to the large current, the bulk capacitors and decoupling capacitors need be increased a lot to meet the tight output voltage regulation. However, it is not a practical solution. Because (1) there is no enough space in the motherboard to place so many capacitors. (2) so many capacitors cost too much.

Instead of paralleling devices, researchers at Virginia Tech proposed a multi-phase buck converter for VRM [64, 65], as shown in Fig3.3. The proposed multiphase buck converter is controlled by phase-shifting their clock signals. The interleaving method can increase effective ripple frequency and cancel the output ripple current. Therefore, the interleaving technology can effectively reduce the output capacitor requirement. Since single phase buck converter adopts large output inductance in order to reduce the output current ripple, the large output inductance can limit the energy transfer speed during load transient. With interleaving method and output ripple cancellation, the output inductance in each phase can be reduced a lot, and the voltage regulation during transient is much better improved.

The multiphase buck converter can also make the thermal dissipation evenly distributed due to its current distribution. And the multiphase buck converter can get better light load efficiency. With interleaving method and phase shedding by reducing the number of operating phase at light load, the light-load efficiency of the multiphase converter can be improved.

The multiphase buck can not only handle larger output current, but also has better power scalability, which can keep step with future increasing microprocessor power requirement. Nowadays, 20A rating current for each phase has become a standard approach. Therefore, the industry widely adopted this multi phase buck solution for VR application.

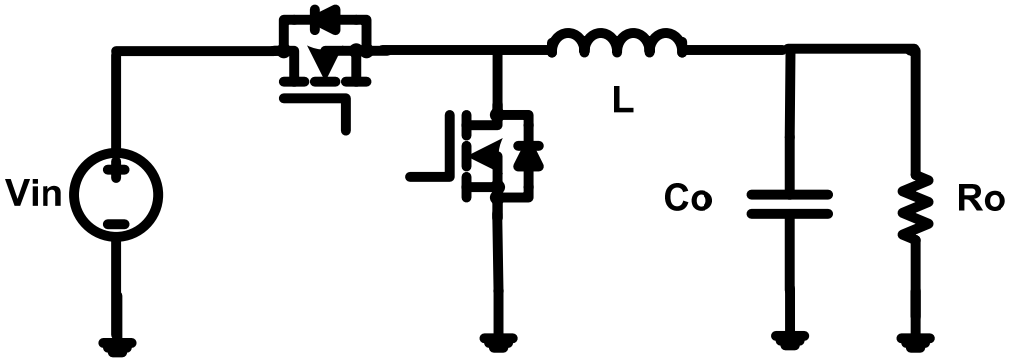


Figure 3.1 Single phase synchronous buck converter

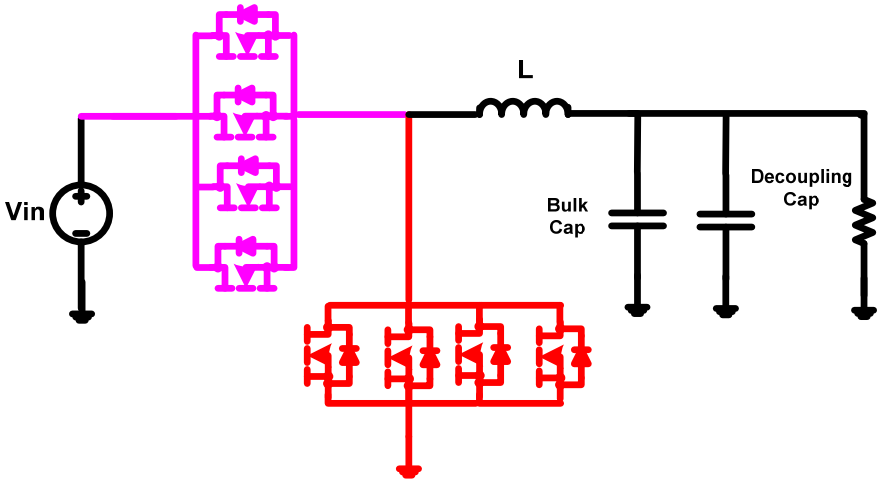


Figure 3.2 Single phase buck converter with paralleling devices

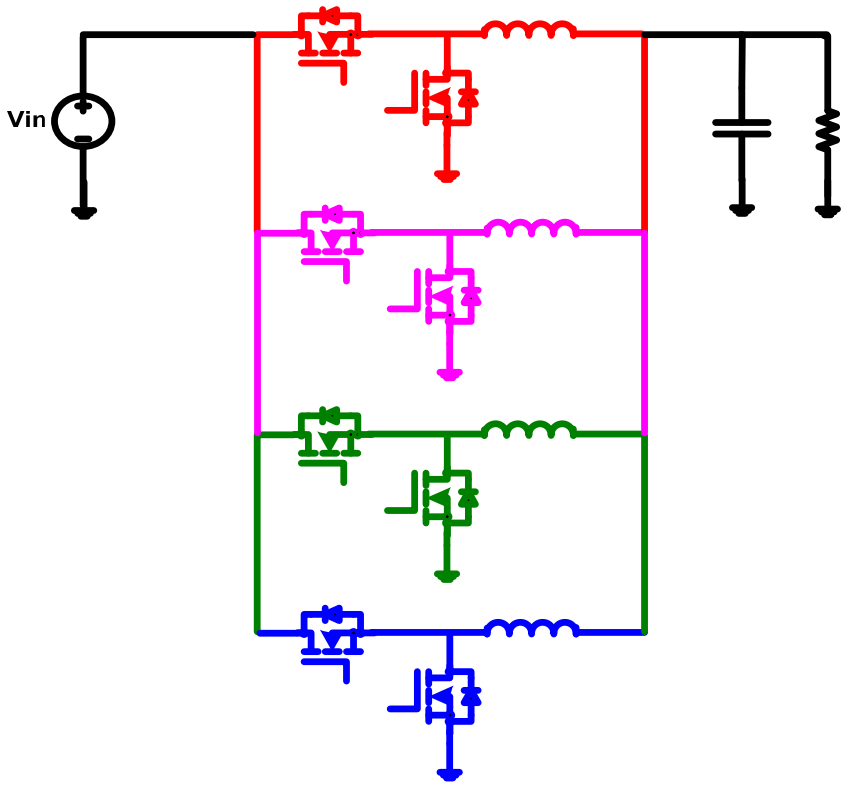


Figure 3.3 The multiphase buck converter with interleaving each phase

3.3 Interleaved SEPIC with valley fill circuit

Interleaving technology has been used in the proposed SEPIC in order to further reduce the filter size, and gain higher efficiency. The mechanism is that through interleaving of the converters in parallel with phase shift of each other, some ripple can be totally cancelled due to the phase shift and the RMS current of output capacitor is reduced. Therefore, the size of output capacitor and EMI filter can be greatly reduced.

Interleaved SEPIC converter with valley fill circuit is shown in Fig.3.4. The converter works in peak current mode control and discontinuous current mode so that it

has high power factor, and can handle high power with reduced number of component count.

As shown in Fig.3.4, $DB_{1\text{-}4}$ are the rectifiers, $L_{1a,b}$, $L_{2a,b}$ are the inductors. D_{1a}, D_{1b} are the output diodes in each phase, and *SA*, *SB* are the MOSFETs. C_o is the output capacitor, The PWM controller is typical peak current mode controller. A type II compensator is applied. The phase A and phase B are 180 degree interleaved. Fig.3.5 shows the operating current and voltage waveforms.

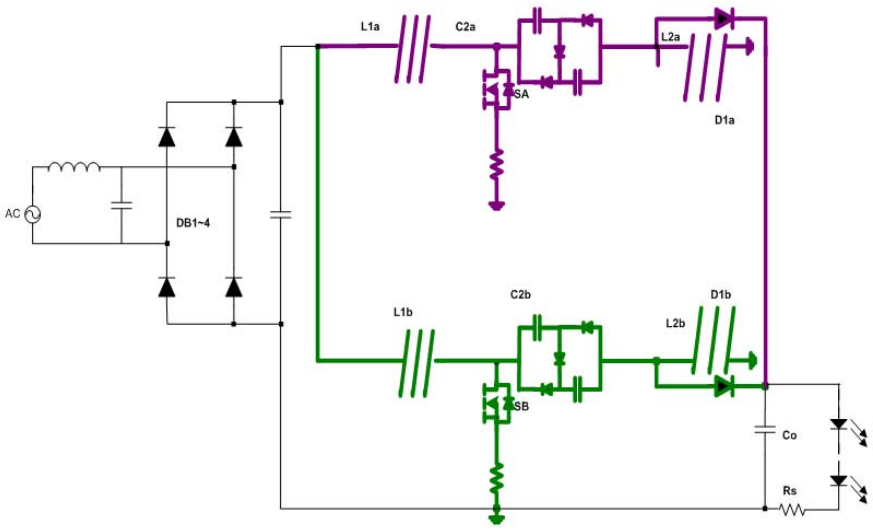


Figure 3.4 Schematic diagram of proposed interleaved SEPIC with valley fill circuit.

There are some advantages of using proposed interleaved SEPIC converter, including:

- The combined current ripple is minimized due to the current ripple cancellation.
- Reduced size of input filter.
- Spread the dissipated power design and ease the thermal design.

- High power factor.
- DCM operation of inductor current in SEPIC converter with valley fill circuit to eliminate the issue of current sharing, and reduce the complexity of controller.
- More phases of converters can be interleaved.

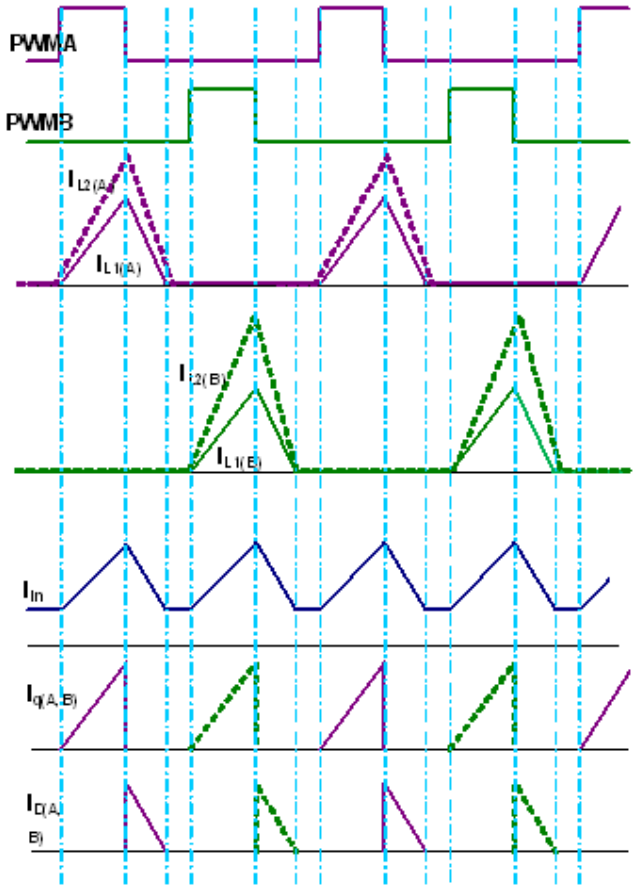


Figure 3.5 The operating current and voltage waveforms

3.4 Experimental Results for the proposed interleaved SEPIC with valley fill circuit

100W prototype has been built in the Lab and tested to verify the design. The operating conditions are:

Input Voltage V_{in}: 110V

Line Frequency: 60Hz

Output Voltage: 60V

Switching Frequency(f_{sw}): 70kHz

Maximum Output Power(P_o): 100W

Some of the key waveforms at 100% load are shown in Fig3.6-Fig3.9. It can be seen that the input current distortion is very small. The power factor measured at 100% load is 0.96. The measured input current harmonics at full load and at 110V input voltage are compared with the harmonics standards IEC 61000-3-2 Class C, which is the harmonics standard for lighting applications. As shown in the Figure 3.10, the results show that the individual harmonics are within the IEC 61000-3-2 Class C limits. The results are almost the same as the proposed single phase Modified SEPIC.

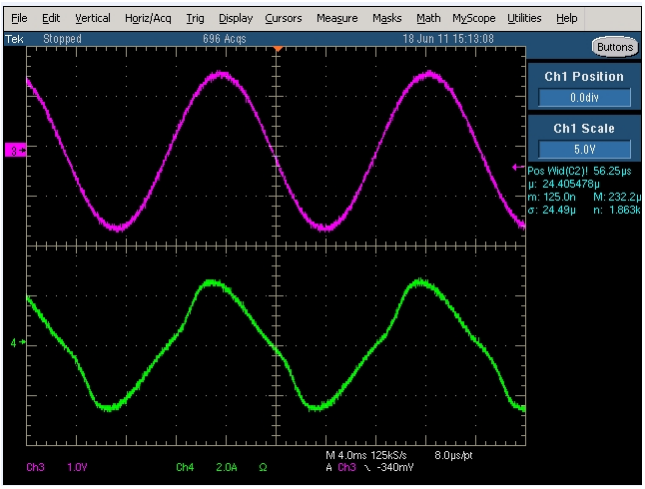


Figure 3.6 Input current(2A/div) and input voltage (50V/div)

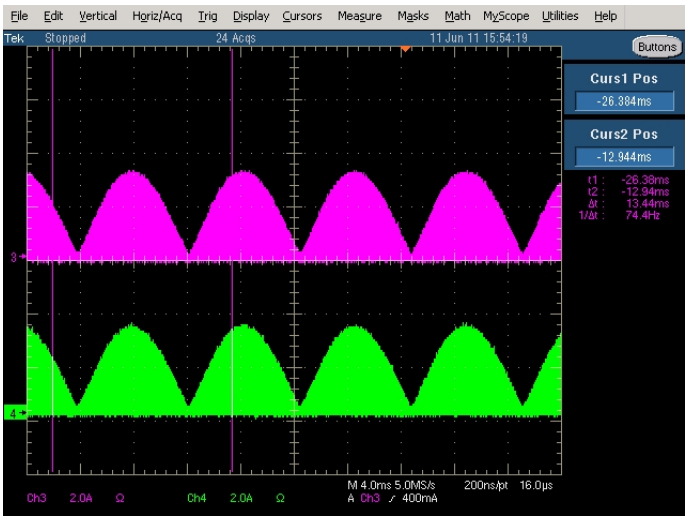


Figure 3.7 Inductor L_{1a} current(2A/div) and inductor L_{1b} current(2A/div)

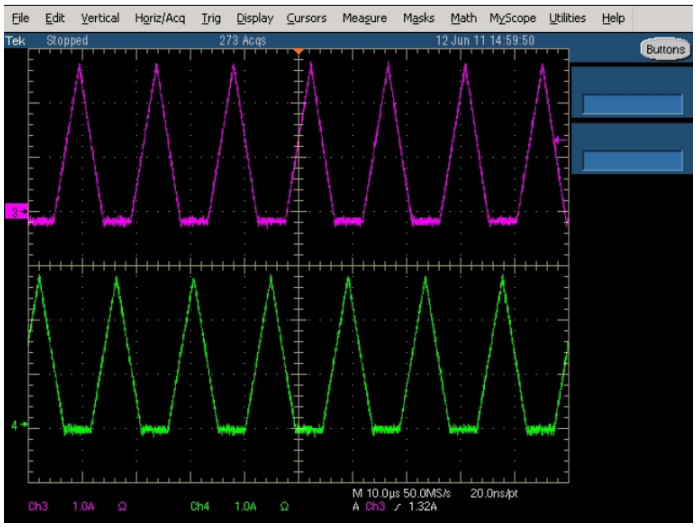


Figure 3.8 Zoom in inductor L_{1a} current(1A/div) and inductor L_{1b} current(1A/div)

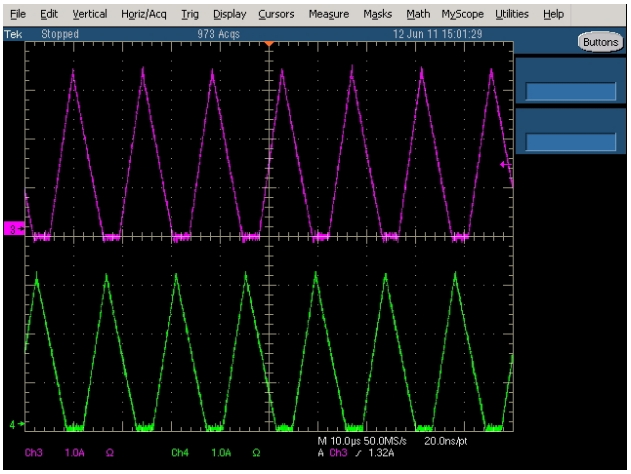


Figure 3.9 Zoom in inductor L_{2a} current(1A/div) and inductor L_{2b} current(1A/div)

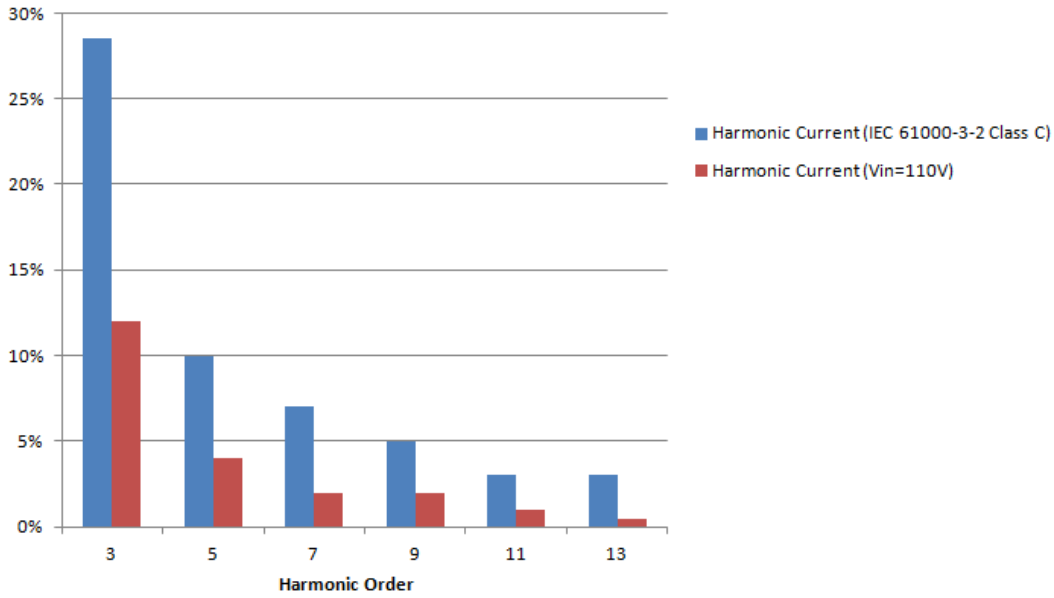


Figure 3.10 Measured input current individual harmonics compared with IEC 61000-3-2 Class C standard

The main circuit component values and parameters are given according to the design equations in chapter 2, and given in Table 3.1. The efficiency results at different load conditions are given in Table 3.2. The efficiency curve at different load conditions is obtained as shown in Fig3.11.

Table 3.1 Summary of selected components.

Inductor $L_{1a,b}$	190uH EER42 Core
Inductor $L_{2a,b}$	110uH EER42 Core

MOSFET	STB12NM60N, 600V,10A.
Output Diode	Schottky, PDS4150 150V,4A
Rectifier Diode Bridge	S3G, 400V, 3A
Diodes in Valley-fill Circuit	Schottky, SS28,80V,2A
Capacitors in Valley-fill Circuit	Cap 16uF,300V Film Polyester
Output Capacitor	Cap 15uF,63V,Metal Polyester

Table 3.2 Efficiency results at different load conditions

100-W Load Test Results	V_{inRMS} (V)	I_{inRMS} (mA)	V_{bus} (V)	I_o (mA)	η (%)
20%	122.8	195.2	60.55	333	84.1
40%	122.8	365.1	60.43	667	89.9
60%	122.5	536.9	60.31	1000	91.7
80%	122.3	714.5	60.25	1333	91.9
100%	122.6	890.3	60.11	1667	91.8

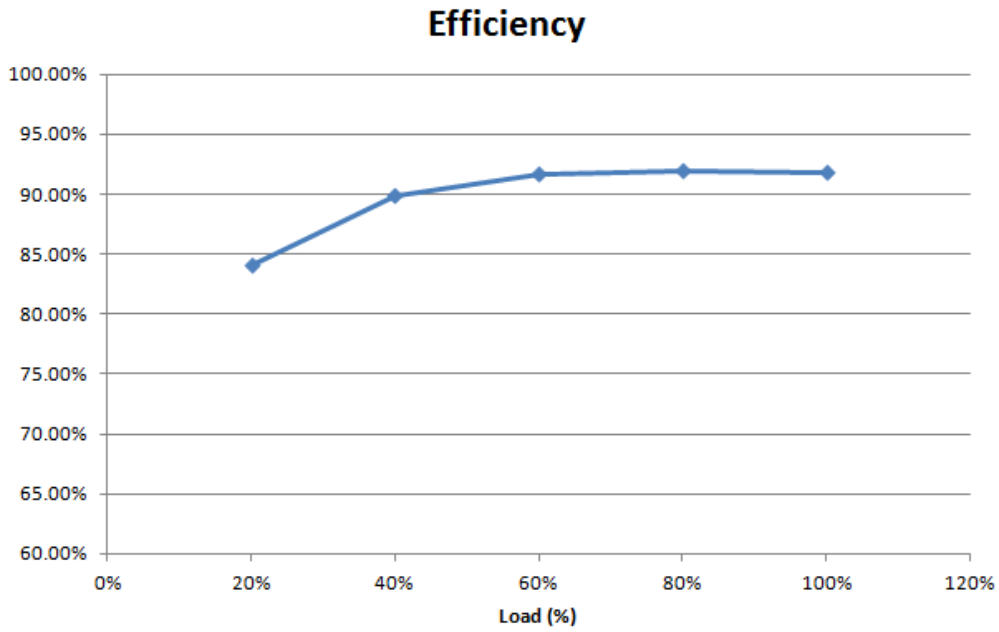


Figure 3.11 Efficiency curve at different load conditions

3.5 Chapter Summary

An interleaved power factor correction SEPIC with valley fill circuit is proposed to further increase the efficiency and to reduce the input and output filter size and cost. The proposed interleaved converter shows the features such as ripple cancellation, good thermal distribution and scalability. The proposed converter is verified with experimental results.

CHAPTER 4

CONCLUSIONS AND SUGGESTIONS FOR FUTURE RESEARCH

4.1 Conclusions

This thesis describes an investigation into the light emitting diode (LED) lamp driven by electronic ballast. The comprehensive overview on the lighting development is given. The characteristic of the light emitting diode (LED) lamp is described. The requirements of the ballast for the light emitting diode (LED) lamp are presented.

A single phase, power factor correction converter without electrolytic capacitors for LED lighting applications is proposed, which is a modified SEPIC converter working in discontinuous conduction mode (DCM). Different with a conventional SEPIC converter, the middle capacitor is replaced with a valley-fill circuit. The principle of the theory is derived. The valley-fill circuit could reduce the voltage stress of output diode and middle capacitor under the same power factor condition, thus achieving higher efficiency. The proposed converter is verified with experimental results.

An interleaved power factor correction SEPIC with valley fill circuit is proposed to further increase the efficiency and to reduce the input and output filter size and cost. The proposed interleaved converter shows the features such as ripple cancellation, good thermal distribution and scalability. The proposed converter is verified with

experimental results.

4.2 Contributions and Suggestions for Future Work

The contributions of the author include:

- Design and implement a single phase, power factor correction converter without electrolytic capacitors for LED lighting applications, which is a modified SEPIC converter working in discontinuous conduction mode (DCM).
- Propose and implement an interleaved power factor correction SEPIC with valley fill circuit to further increase the efficiency and reduce the input and output filter size and cost.

Compared with discontinuous conduction mode, interleaved critical conduction mode PFC, which is based variable frequency modulation, can add some advantages including lower peak current and better thermal management to gain better efficiency. In addition, it also has smaller differential mode EMI filter than a single stage converter with the same total power rating. Hence how to design a critical conduction mode control for the proposed Modified SEPIC converter is a good topic for future work. And how to design the coupled inductors between the interleaved converters working in variable-frequency will be also a good topic for future work.

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