

Formation and Rupture of Nanofilaments in Metal/TaO_x/Metal Resistive Switches

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Abstract

There is an increased interest in the Conductive Bridge Random Access Memory (CBRAM) and Resistive Random Access Memory (RRAM) because of their excellent scaling potential, low power consumption, high switching speed, good retention and endurance properties. Although, various mechanisms have been proposed to explain the switching behavior in CBRAM devices, i.e. metal ion migration and subsequent formation and rupture of conductive filament, formation of conductive path via oxygen ion transport etc, there are still many aspects of these mechanisms that are little understood or are being disputed. This work probes the details of the switching mechanisms on a new level and asks questions like:

- 1) How is the formation of nanofilament affected by various degrees of Cu diffusion stopping power of the inert electrode? To answer this question, resistive switches with very thin Cu layers covering the Pt electrode were fabricated and analyzed.
- 2) How does a limited source of active ions impact the formation and rupture of nanofilaments? To answer this question, new samples with limited Cu supply were fabricated and analyzed.
- 3) What is the mechanism of nanofilament formation in Pt/TaO_x/Pt resistive switches where the active copper electrode is removed and replaced by inert Pt electrode.
- 4) What are the most suitable conditions (material structure of the device and operation conditions) to set and reset multi nanofilaments?

This work summarizes the current status of analysis of the data obtained while attempting to explain interesting phenomena like volatile switching and multiple filament formation experienced by modifying the switch structures.

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Chapter 1: Introduction

In this chapter, the nanocrossbar resistive switch will be discussed in detail to understand and highlight the importance of this device, its evolution, different mechanisms involved in its operation and its applications. Various mechanisms have been proposed to explain the resistive switching behavior i.e. metal ion migration and the subsequent formation and rupture of the metal conductive filament, formation of conduction path via oxygen ion transport. However there are still many aspects of these mechanisms that are little understood or are being disputed. Furthermore the need to understand the switching mechanism when the conventional switch structure is modified during fabrication and the resulting quality of the conductive filament has spurred this research topic.

1.1 Resistive Switch/RRAM

1.1.1 Basic Definition

A resistive switch also called resistive random access memory (RRAM) is presently one of the most promising candidates in the field of non-volatile memory development and it depends upon internal reduction and oxidation reactions to induce the resistance switching phenomenon. The basic structure of a resistive switch is a MIM structure, where the material 'I' is an ion or mixed ion-electron conducting material sandwiched between typically two different electron conductor metal electrodes 'M'. Oxides, higher chalcogenides or ionic solids are most commonly used as the material I [1]. There are various material systems such as GeTe, GeSe, Ag-Ge-S, TiO₂ and Cu doped SiO₂ [2] which exhibit resistive switching behavior and among these, binary transition metal oxides are the most impressive material systems because of simple structure, ease of fabrication and excellent compatibility with the complementary metal oxide semiconductor (CMOS) backend technology. TaO_x which has been extensively used in the course of this research as the electrolyte material is one such transition metal oxide.

1.1.2 Device Operation

A resistive switch is essentially a two terminal device that transitions between a high resistive state (HRS) and a low resistive state (LRS) by the application of a SET and RESET voltage pulse. Conventionally both these states are stable and non volatile. Three most important types

of RRAMs are conductive bridge RAM (CBRAM), valence change memory (VCM) and thermo-chemical memory [1]. There are two modes of operation of the resistive switch, unipolar mode and the bipolar mode. In the bipolar mode, the resistive switching is dependent on the polarity of the applied voltage which means that if it changes from HRS to LRS on the application of positive voltage, then it will change from LRS to HRS on the application of negative voltage. In the unipolar mode the resistive switching is dependent on the amplitude of the applied voltage and not the polarity i.e. it changes from HRS to LRS and vice-versa on the application of the same polarity voltages but of different magnitudes. Again there is interplay between electrochemical and thermo-chemical redox processes which determines the type of the resistive switch as well as its polarity. The unipolar switching characteristics can be explained by the dominance of the thermo-chemical reactions (thermal dissolution model induced by Joule's heating) over the electrochemical reactions (ion migration model). Bipolar switching characteristics are observed when the ionic migration model prevails. Figure 1 shows the two basic operation modes i.e. bipolar and unipolar modes operation of the resistive memory cells [3] [4].

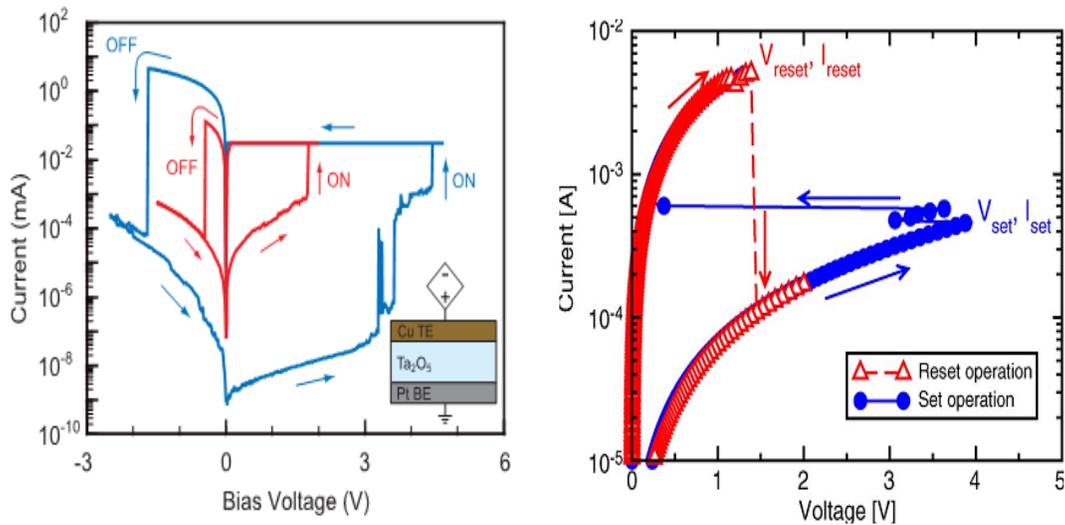


Figure 1 : Bipolar and Unipolar modes of operations[3][4](© [2010] Nanotechnology)(© [2009] IEEE). Used under fair use, 2012.



Figure 2: Conductive filament rupture by thermal diffusion

1.1.3 Resistive switching performance evaluation parameters

1. Forming

Forming is the phenomena of the formation of the conductive filament in the electrolyte for the first time in a virgin/fresh device. Forming voltages are typically much higher than the SET voltages and can be sometimes as high as 5V. However it is not essential that every cell needs an electroforming step, sometimes the cell can be set directly. Thus the condition for electroforming as well as the need for electroforming step depends upon the structure of the MIM system [1]. During the forming process, a limiting current called the compliance current is applied to the resistive switching circuit from the external circuit so as to prevent the permanent damage of the device by the flow of excess current into the circuit.

2. Set

SET is the phenomena of re-establishing the conductive filament bridge after it has been broken at least once either by Joule's heating or by electrochemical migration of ions. Typically set voltages are significantly lower than forming voltage and just like the forming step, a limiting current i.e. the compliance current needs to be applied to the device from the external circuit to protect the device from permanent damage. SET leads the device into the low resistive state (L.R.S) also called the ON state. The resistance of the switch during this state is also called as the ON resistance or the R_{ON} .

3. Reset

RESET is the phenomena of rupture of the conductive filament bridge either by the ion migration (bipolar mode) or thermal dissolution caused by Joule's heating (unipolar mode). Reset leads the device into the high resistive state (H.R.S) or the OFF state. The resistance of the switch during the reset state is also called as R_{OFF} .

4. Compliance Current

Compliance current is the current limit applied by the external circuit during the SET or form process in order to prevent the devices getting permanently damaged. In the course of the current work, the Keithley 4200-SCS probe station was used to characterize the devices and the compliance current limit is also applied by it. The normal range of compliance current used in the present work is 10 μ A to 1 mA which allows the device operation with any damage. There is no need to apply a compliance current limit while trying to reset the device.

5. Resistance Ratio

The ratio of the R_{OFF}/R_{ON} is termed as the resistance ratio of the resistive switch. Typically R_{OFF}/R_{ON} ratios > 10 are required for cost effective RRAM chips [1].

6. Endurance

Endurance of a resistive switch denotes the maximum number of times the cell can be set and reset until the ON or OFF state falls out of the predefined acceptance window [1].

7. Retention

Retention is the ability of the resistive memory cell to keep the stored information if the cell is not addressed [1].

1.2 Conductive Bridge RAM

1.2.1 Basic Structure

Conductive Bridge RAM, a subset of RRAM is being considered as the future of non volatile memory devices due to its extremely low power consumption and higher scalability, high switching speed and good retention and endurance properties [5]. The basic structure of a conductive bridge RAM is given in Figure 3. It typically consists of a stack of active-metal electrode/solid electrolyte/inert-metal electrode. The active metal can be any oxidizing metal like Cu or Ag which is capable of providing fast diffusing mobile metal ions. For the electrolyte, a large selection of materials i.e. Cu_2S , SiO_2 , GeS , Ta_2O_5 , AgGeSe , TaSiO , HfO_2 is available which allow the transport of ions, with greater mobility as compared to regular solid state

materials [6]. For the inert electrode, metals like Pt, Ir or W are generally used. The simplest schematic of a nanocrossbar resistive switch as seen under an optical microscope is as shown in Figure 4. The top and the bottom electrode lines run perpendicular to each other.

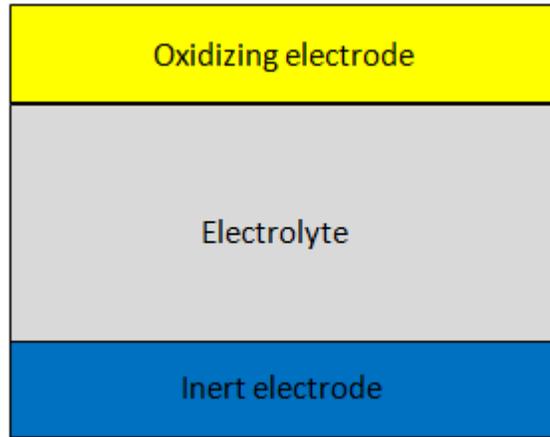


Figure 3: Stack structure of a CBRAM

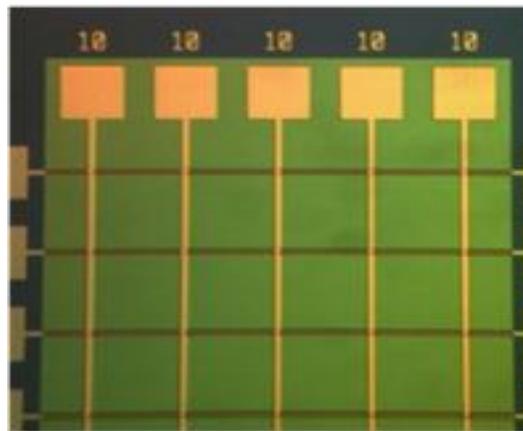


Figure 4: Optical micrograph of the crossbar architecture

1.2.2 Device Operation

The switching mechanism in a CBRAM is mostly believed to be based on the formation and rupture of a conductive filament either due to migration of metal ions (from the anode) in the solid electrolyte towards the cathode (thereby forming a metal filament between the anode and the cathode) [7] or the migration of oxygen ions towards the anode (formation of conductive path by the means of an oxygen vacancy filament) [8]. When a positive bias is applied, the active electrode (anode) gets oxidized and the fast metal ions (either Ag^+ or Cu^{2+}) begin drifting towards the bottom electrode (cathode) under the electric field and get reduced thereby forming

the conductive metal filament there. This conductive filament keeps growing vertically from the cathode until it makes a contact with the anode. When the anode and cathode are connected by the complete metal filament, the device is set to be SET. When the applied voltage polarity is reversed, the metal atoms start dissolving at the tip of the conductive filament touching the anode and break the conductive filament connecting the anode and the cathode leading the device into the RESET state. Again in many oxides, especially the transition metal oxides, oxygen ion defects like the oxygen vacancies are much more mobile as compared to the metal ions. Moreover this oxygen vacancy migration can be brought about by two mechanisms namely the oxygen vacancies forming a hopping conductive path similar to a percolation effect [8] and the oxygen vacancies acting as dopants thereby making the electrolyte conductive [9]. Details about the oxygen vacancy bridge will be given in the section on mechanism of the operation of a Pt/TaO_x/Cu device. The Figures 5 and 6 show the formation of Cu filament by cation migration and oxygen vacancy filament by the percolation effect respectively.

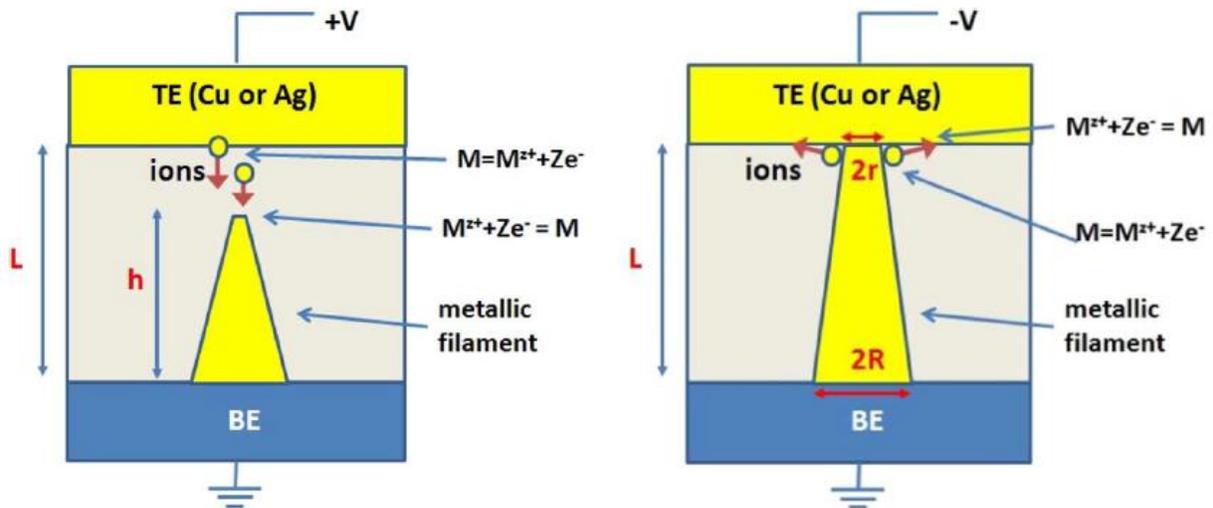


Figure 5: Schematic of the switching process in CBRAM cell. (a) CF grows vertically and (b) CF laterally dissolves [7] (© [2011] IEEE). Used under fair use, 2012.

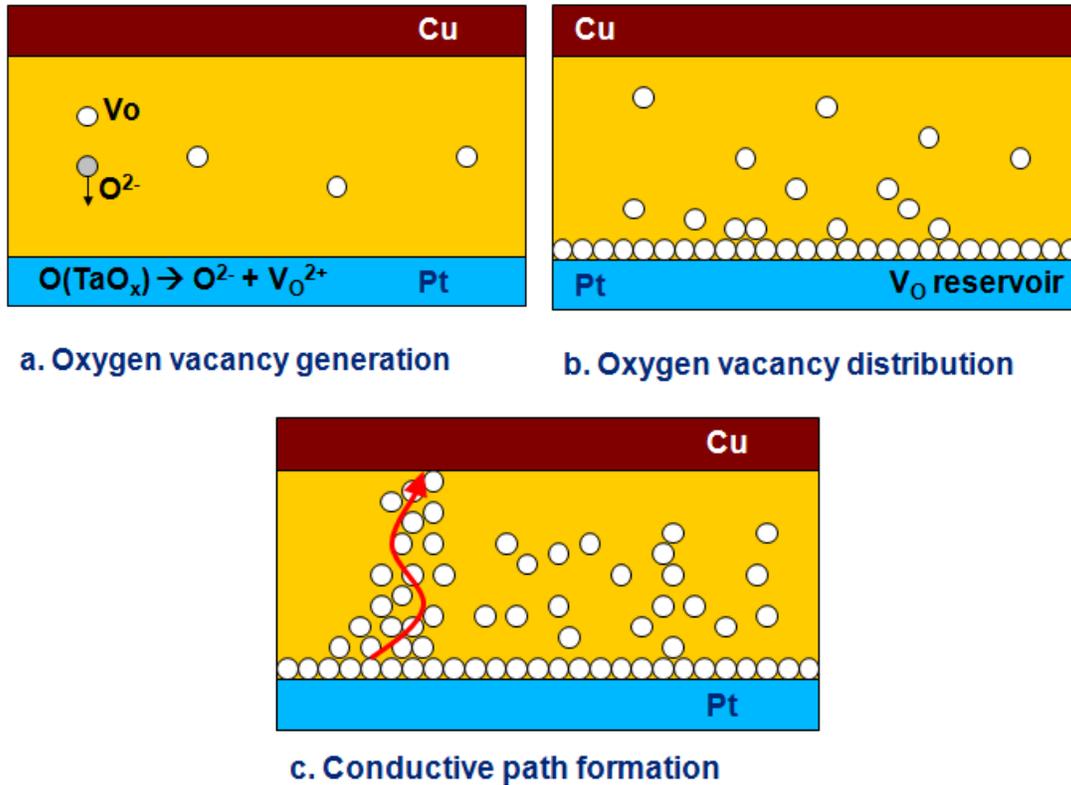


Figure 6: Switching process in CBRAM cell due to [O] vacancy filament

1.3 Moore's law and need for resistive switches

Gordon Moore published Moore's law in 1975 which ever since then has been the fundamental driver of the semiconductor technology growth. Moore's law predicts that the number of transistors on an integrated circuit (IC) double every 2 years [10]. Scaling of semiconductors is the technique of reducing the feature sizes to increase the number of transistors that can be fitted on a chip (transistor density) thereby improving the overall performance of the chip. Transistor scaling is also said to be the true measure of Moore's Law for the fact that, as long as transistor scaling is possible, the law will hold true. Scaling mainly aims towards attaining low power consumption, higher operation speed, higher density and lower operating voltages. Scaling also makes the chips much more affordable as well as allowing a multitude of different circuits to be implemented on the same chip hence increasing the overall complexity of the circuit. So far scaling has been used very aggressively and there isn't much time before it will reach its physical limit and Moore's law will stop holding true. Some of the recent works have suggested that a single atom transistor may be the end of Moore's law [11]. Again the aggressive and relentless transistor scaling has an adverse effect on device reliability [12] and it becomes both

expensive and difficult to obtain reliable devices. These are some of the most important reasons behind the increased interest in resistive memories to replace the CMOS nonvolatile memories in the recent years. Figure 7 shows the scaling of the chip size as a result of Moore's law.

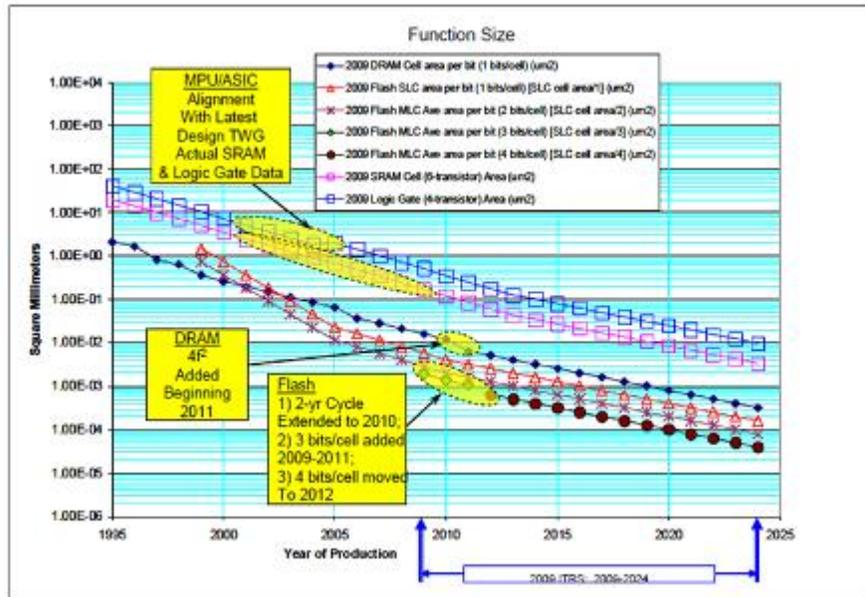


Figure 7: 2009 ITRS Product Function Size Trends [13]. Used under fair use, 2012.

1.4 Applications

Two-terminal resistive switches suggested in the past as a replacement of floating gate electrodes in non-volatile random access memory and as the switching elements in reconfigurable logic circuits [14] are now making inroads in stateful logic operations [15], neural networks [16] and chaotic circuits. The resistive switching device was first discovered in the 1960s and it shows a strong potential of reaching the scaling limit below 20 nm. There has been an increased interest generated recently in the areas of Conductive Bridge Random Access Memory (CBRAM) and Resistive Random Access Memory (RRAM) because of their excellent scaling potential, low power consumption, high switching speed, excellent retention and endurance properties and compatibility with CMOS backend process technology. There are several advantages of using a RRAM over a floating gate electrode for nonvolatile memory applications. The programming of floating gates involves addition and removal of electrons to and from a floating gate electrode which is a very complicated procedure involving carrier injection and tunneling while on the other hand, a RRAM can be programmed with the

application of voltage pulses. Again there are severe constraints on the scaling of floating gates based on coupling capacitances, resistance while scaling of RRAM is very simple and is just limited by lithographic constraints.

1.5 Evolution of resistive memories.

The resistive switching was first discovered in oxides long back in 1960s when this novel phenomenon was reported in an Au/SiO/Au structure. However the research on resistive switching eventually faded away by the 1980s because of the stability issues, limitations of the contemporary analytical tools which put severe limitations on the exploration of the mechanism and last but not the least due to the emergence and rapid development of Si semiconductor based memories. However in the early 2000s, the interest in RRAM research was renewed due to important discoveries by Asamitsu et al. [17], Kozicki et al. [18] and Beck et al. [19].

1.6 Pt/TaO_x/Cu Device

1.6.1 TaO_x as electrolyte

Before the actual fabrication of resistive switching devices, literature survey of the various materials available to act as the solid electrolyte was done. Resistive switching property is displayed by a wide range of solid electrolytes such as GeSe, Cu₂S, Ag₂S and Ta₂O₅ but the switches other than Ta₂O₅ switch have much lower set voltage or turn on voltages and since the major focus here is on the purpose of putting the resistive switches to use in the non volatile memory area, lower set voltages are not desirable. It was observed that the Ta₂O₅ switch has threshold voltages above the operating voltages of the CMOS devices and hence they are the most appropriate to be used in the non volatile switching [20] [21]. One more reason for using Ta₂O₅ as the solid electrolyte here is that it has smaller ionic diffusion coefficient for Cu⁺ ions, and thus the threshold voltage for set is comparatively larger than other electrolytes and hence it has better retention properties. It is however very difficult to deposit a highly pure Ta₂O₅ using e-beam evaporation thus the actual electrolyte used during the course of this work is TaO_x. TaO_x has a much higher endurance i.e. 10¹⁰ cycles as compared to 10⁴ of Ta₂O₅. The deposition of TaO_x was done by e-beam evaporation of Ta₂O₅ source without any oxygen injection into the PVD chamber.

1.6.2 Cu as anode

For the purpose of forming the anode either of the metals, Cu or Ag can be chosen. For the fabrication of the devices under study, Cu was selected as the anode because of its much lower cost. The thickness of the Cu layer for the top electrode was chosen to be 150 nm for all the devices since a thinner layer of Cu has a much higher resistance.

1.6.3 Pt as cathode

For the purpose of the inert electrode Pt was chosen over ruthenium and tungsten since it is easier to deposit Pt using Physical vapor deposition. The melting temperature of Pt is 1769° Celsius and e-beam evaporation gives relatively good quality Pt film. The melting temperature of Ruthenium is 2700° Celsius and the quality of film deposited by e-beam evaporation is very poor. Tungsten has a melting temperature of 3401° Celsius and although it gives a good quality film through e-beam evaporation, its higher melting point makes it all the more difficult to deposit it. The thickness of the Pt lines deposited was kept consistent at 60 nm to 61 nm for all the devices.

1.7 Switching mechanism of Pt/TaO_x/Cu device

The Pt/TaO_x/Cu resistive devices are typically set and reset by applying positive and negative voltages to the Cu electrode while the Pt inert electrode is kept grounded. A Cu or oxygen vacancy conductive filament (CF) forms and ruptures during the set and reset operations, and the device works as a CBRAM in terms of the conduction mechanism. When a positive forming/set voltage is applied to the Cu electrode, the Cu gets oxidized to Cu⁺ ions and the Cu⁺ ion migrate towards the Pt electrode under the influence of the high electric field and the reduction and electro-deposition of Cu⁺ ions takes place on the surface of the Pt electrode in the form of Cu atoms. This process results in the formation of a Cu filament which grows back from the Pt electrode to the Cu electrode. Once this filament connects the two electrodes, there is a sharp drop of resistance leading the device into a low resistance state. Again the oxygen vacancy [O] conductive filament can also be established in TaO_x by applying a negative forming voltage on the Cu electrode and therefore the same device conforms to RRAM functionality. According to what has been observed so far, the Cu- and [O]- based switching can be well separated by the polarity and magnitude of the set voltages [22]. During the RRAM functionality which is

exhibited under negative bias voltages, the following electrode-reduction reaction occurs in the TaO_x layer:



The O²⁻ ions migrate from the Cu electrode to the Pt electrode under the negative bias voltages. The vacancies [O] left behind by O²⁻ ions form conductive filaments and the resistive state changes. Figure 8 shows the two different types of conductive filaments inside a single Pt/TaO_x/Cu switch.

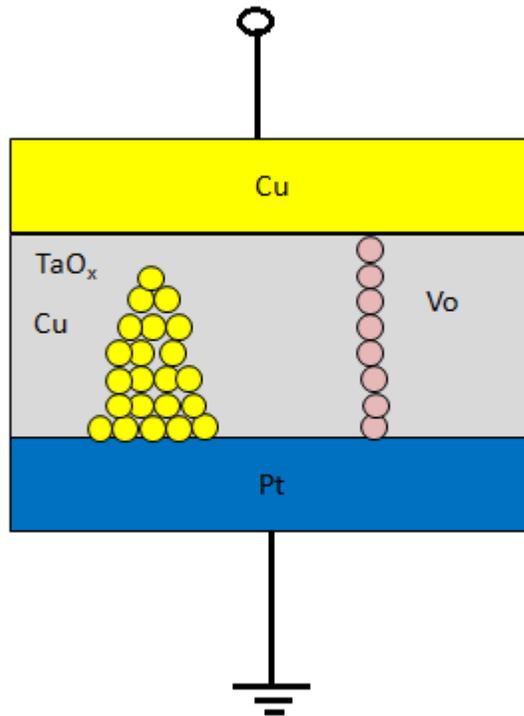


Figure 8: Structure of a single switch

1.8 Electrical Characterization

For the purpose of electrical characterization, the Keithley 4200 –SCS (Semiconductor Characterization System) has been used at room temperature. This system allows a complete characterization of devices, materials and semiconductor processes. During the current work, the DC static voltage sweep was provided by the external circuit to the resistive memory cell. The Pt bottom electrode is kept grounded and the bias voltage was applied to the Cu top electrode. The two most important parameters of the characterization circuit are the sweep rate and compliance current. Sweep rate is defined as the rate of change of voltage with time. The sweep rates used

for the device characterization in course of the current work are 0.01V/step, 0.001V/step and 0.005 V/step. For some part of the characterization, sweep rate as low as 0.005 V/step has been used in order to obtain much refined I-V characteristics for the devices. In the SET or form operation, a typical compliance current of 10 μ A ~ 1 mA was used. The bias voltage can be swept from 0 V to \pm 6 V for either SET or RESET. With this setup, the devices can be switched stably and repeatedly without any significant permanent damage. The experimental set used for the electrical characterization is as given in Figure 10.

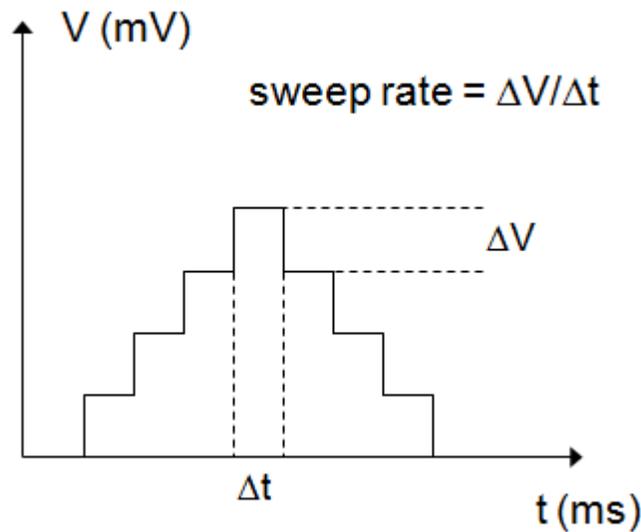


Figure 9: Sweep Rate definition

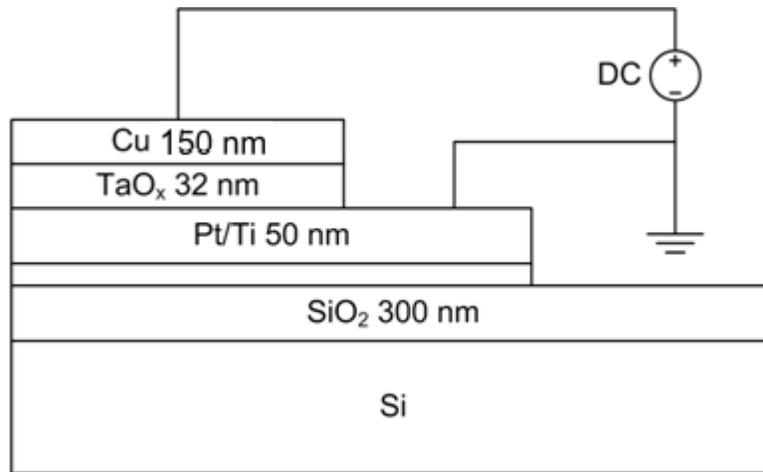


Figure 10: Cross sectional view of Cu/TaO_x/Pt nonvolatile memory device.

1.9 I-V Characteristics

Figure 11 shows the I-V characteristics of a typical Cu/TaO_x/Pt device. Again the device covered under this research work i.e. a Cu/TaO_x/Pt device can be switched between the HRS and LRS based on the formation and rupture of two types of nanofilaments in the same device: Cu and oxygen vacancy conductive bridges based on the polarity of switching voltage in both bipolar and unipolar regimes [22]. During the course of the current research, the focus has been on elucidating the formation and rupture of Cu filament bridges. Figure 12 and Figure 13 show unipolar switching and bipolar switching by the Cu filament and oxygen vacancy filament respectively.

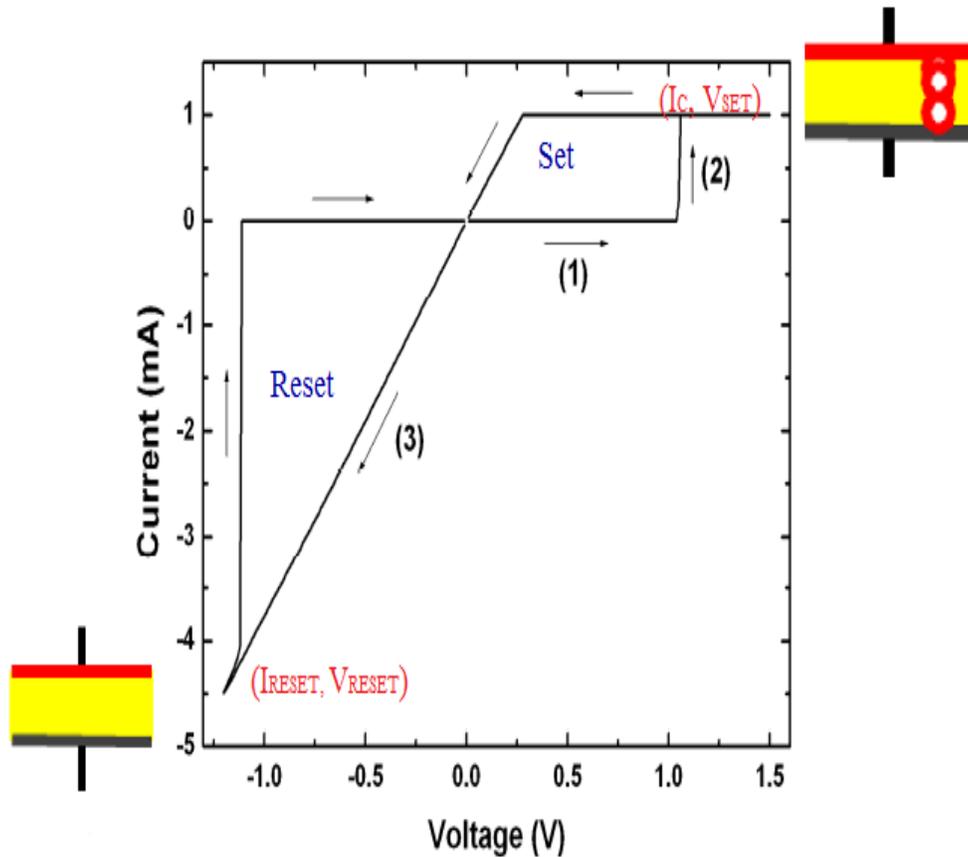


Figure 11: The bipolar switching characteristic of a single Cu/TaO_x/Pt cell. The set voltage is 1.05 V and the reset voltage is -1.11 V.

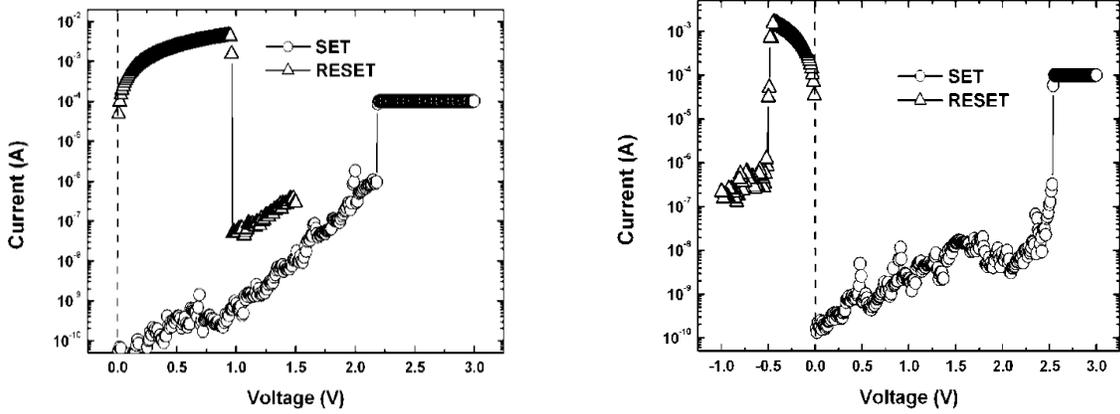


Figure 12: Unipolar and Bipolar mode switching for Cu filament bridge [22](© [2012] ECS). Used under fair use, 2012.

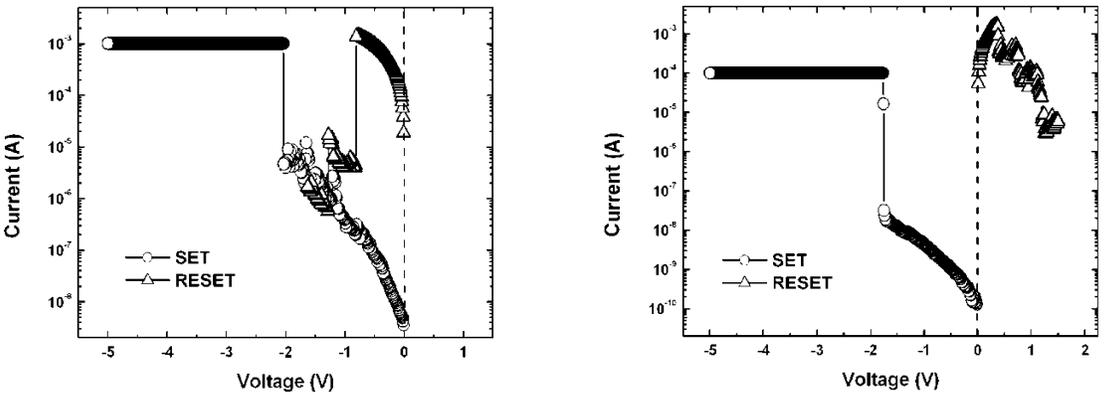


Figure 13: Unipolar and Bipolar mode switching by oxygen vacancy filament [22](© [2012] ECS). Used under fair use, 2012.

1.10 Structure of Cu filament

The current work is focused towards achieving a the better understanding of the Cu conductive filament, as such a literature survey was done on the CBRAM switches to understand the structure and shape of this Cu filament. It is believed that the Cu filament evolution has in essence 4 stages i.e. vertical growth, lateral growth, lateral dissolution and vertical dissolution based resulting from electric field driven ion migration. Just before the SET, the electric field is concentrated across the tip and as a result drives the ion migration vertically while before a RESET operation there is a lateral electric field at the top of the filament which drives the ion

migration laterally [7]. Based on this theory the structure of the conductive filament during the set and reset process should have a conical structure with a broader base on the Pt electrode as given by Figure 14.

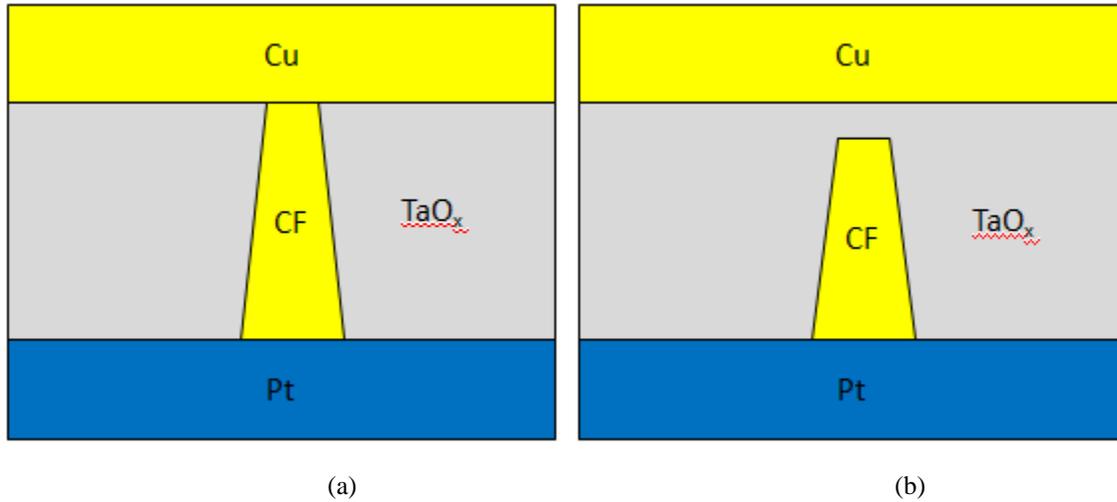


Figure 14: Resistive switch (a) ON state and (b) OFF state

Chapter 2: Fabrication

2.1 Purpose of research

As mentioned in the very beginning, the purpose of this current work is to understand the mechanism of injection and diffusion of the metal ions from the anode into the electrolyte and the subsequent formation and rupture of the metal filament when the conventional witch structure is modified. So the first step was to fabricate the simple resistive switches with a Pt/TaO_x/Cu structure and characterize them completely. After this, resistive switches were fabricated with a delta layer of Cu in between the inert Pt electrode and electrolyte. The structure of these devices is a Pt/ δ -Cu/TaO_x/Cu stack to understand the effect of this delta layer of Cu atoms on the SET and RESET process of these devices as compared to the simple resistive switches. Again, to understand the mechanism of Cu ion diffusion when the source of Cu atoms is limited in the resistive switches, devices with a limited source of Cu ions were fabricated. The structure of a limited metal ion source device is a stack of Pt/TaO_x/ δ -Cu/Pt, with the δ -Cu layer being as thin as 6 nm. Also during the course of characterization of the Pt/ δ -Cu/TaO_x/Cu devices, the novel phenomenon of volatile resistive switching was discovered and in order to elucidate the mechanism of volatile switching operation Cu/TaO_x/Cu devices were also fabricated. Again Pt/TaO_x/Pt devices were also fabricated to understand the switching operation in the absence of metal ions. Another experiment was to establish the effect of scaling of the solid state dielectric thickness on the forming voltage, so in addition to simple resistive switch of dielectric thickness of 32 nm, two more devices were fabricated with a dielectric thickness of 16 nm and 8 nm respectively.

2.2 Test Structures

All the devices mentioned in the previous sections were fabricated on 4 inch silicon wafers in a crossbar array on a thermally oxidized Si wafer. The metal electrodes and the solid state electrolyte were deposited by e-beam evaporation and were patterned by lift-off technology. The top electrode runs perpendicular to the bottom electrode and each intersection of the top and bottom metal lines is single resistive switching cell. The various devices fabricated during the course of this current work are describes below with the exact thickness of each layer.

1. Simple resistive switch

- 1) Pt (61nm)/ TaOx (32nm) / Cu (150nm)
- 2) Pt (61nm)/ TaOx (16nm) / Cu (150nm)
- 3) Pt (61nm)/ TaOx (8nm) / Cu (150nm)

2. Intermediate or δ Cu layer devices

- 1) Pt (61nm)/Cu (9.5nm)/TaOx (16nm)/Cu (150nm)
- 2) Pt (61nm)/Cu (6.5nm)/TaOx (16nm)/Cu (150nm)
- 3) Pt (61nm)/Cu (3.5nm)/TaOx (16nm)/Cu (150nm)

3. Limited Cu ion source devices

- 1) Pt (61nm)/TaOx (16nm)/Cu (12nm)/Pt (61nm)
- 2) Pt (61nm)/TaOx (16nm)/Cu (6nm)/Pt (61nm)

4. Devices without any stopping electrode

Cu (150nm)/TaOx (16nm)/Cu (150nm)

5. Devices without any mobile metal ion source

Pt (61nm)/ TaOx (16nm)/Pt (61nm)

2.3 Process Flow

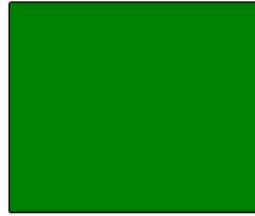
A process flow was designed for each crossbar structure using a set of three masks. In the sections that follow, a detailed review of the process flow as well the various optimizations applied to each of the process steps for the different devices will be discussed. All the crossbar structures have been fabricated on Si substrates. Among the three masks, one of them was used for patterning the bottom electrode, the second one to pattern the electrolyte layer and the third mask was used to pattern the top electrode.

2.3.1 Simple resistive switch

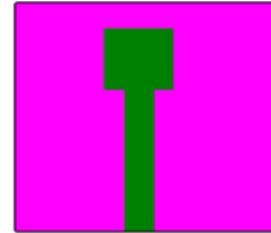
The silicon substrates were first cleaned using the RCA -1 and RCA-2 cleaning procedures and then these wafers were thermally oxidized inside a furnace at a temperature of 1050 °Celsius to

deposit about 750 nm to 800 nm of silicon dioxide. Then the patterning for the bottom electrode is done using the mask aligner. Along with the patterning the first electrode, this first patterning step also patterns the alignment marks which help us in accurate alignment of the device during the subsequent processing steps. The actual patterning is performed by coating the silicon substrate with approximately 1 μm thick layer of the AZ -5214 E-IR photoresist. Then it is followed by UV exposure, reversal bake at 117 ° Celsius, flood exposure and development of the photoresist leaving a negative image of the mask lines on the substrate. After this, the e-beam evaporation of a thin layer of Ti about 10 nm to 12 nm thick in the automatic mode of the PVD - 250 is done. This Ti layer aids the adhesion of Pt to the silicon surface. This is followed by the e-beam evaporation of Pt in the manual mode of the PVD 250 at an e-beam current of 180 mA. After taking the sample out of the evaporation chamber, it is allowed to cool down for a while and then the lift off is performed by immersing the wafer in acetone solution for about 5 to 10 minutes. The lift off process removes the metal from unwanted regions and leaves the required Pt metal lines on the substrate. After the lift off, the patterning for the blanket deposition of TaO_x is done. It is to be remembered that before each resist coating, a solvent clean procedure involving the use of acetone, IPA and DI water followed by the blow dry using a nitrogen gun has to be performed. After the patterning for TaO_x and subsequent development step, deposition of TaO_x is done using the e-beam evaporation of pure Ta₂O₅ pellets using PVD 250 without any oxygen injection into the evaporation chamber in the automatic mode. This is followed by the lift off which leaves a layer of TaO_x on the device area. Again the patterning for the top electrode is performed which is followed by the development. Then e- beam evaporation of Cu is done in the automatic mode of PVD 250 tool and the last step in the process flow is the lift off which leaves the desired crossbar structure. The lift off process following evaporation of TaO_x or Cu involves immersing the wafer in acetone as well as subjecting it to ultrasonic vibrations for 10- 11 minutes. Figure 15 shows the process flow for the fabrication of a simple resistive switch with a Pt/TaO_x/Cu structure.

(1) Thermally grown SiO₂

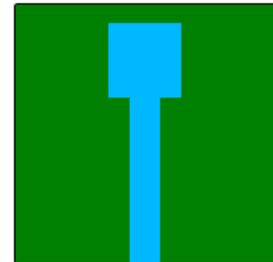
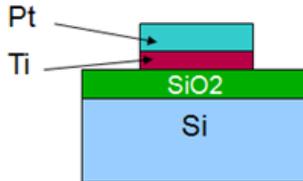
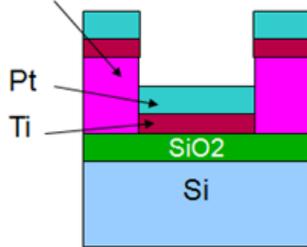


(2) Spin coated with AZ 5214E-IR, Prebake, UV exposure, reversal bake, flood exposure, PR developed.

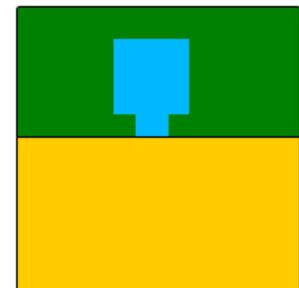
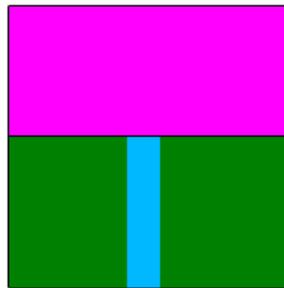
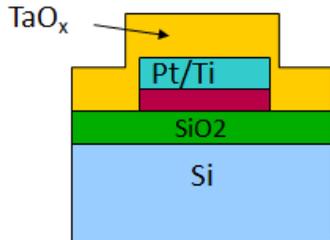


(3) Pt/Ti E-Beam Evaporation(PVD 250, manual mode) at pressure 2×10^{-6} tor and dep rate 1 A/sec and current 160mA and Liftoff

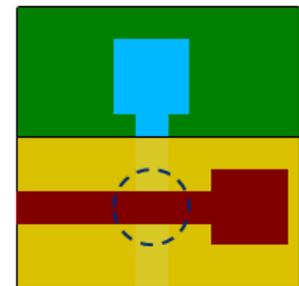
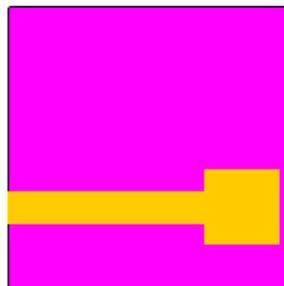
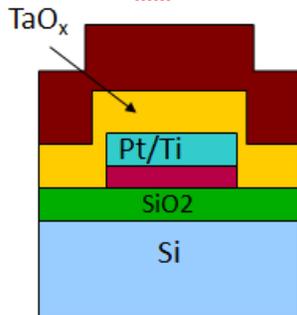
Photoresist



(4) TaO_x E-beam Deposition (PVD 250, auto mode) at pressure 2×10^{-6} tor, dep rate 1 Å/sec with no oxygen injection in the chamber and Liftoff



(5) Cu E-beam Deposition(PVD 250, auto mode) at a of pressure 2×10^{-6} tor, dep rate 5 Å/sec and dc current of 90 mA and Liftoff



Device Cell

Figure 15: Process Flow for Pt/TaOx/Cu resistive switch fabrication

2.3.2. Resistive switch with δ -Cu layer

In all, 3 intermediate copper layer devices were fabricated starting with 9.5nm thick layer of intermediate copper. The other two devices had 6.5nm and 3.5 nm of intermediate Cu layer respectively. The fabrication process flow for these devices is a little different from the conventional resistive switch in that the intermediate Cu layer is deposited through the e-beam evaporation of Cu in the manual mode immediately after the deposition of Ti/Pt (bottom electrode) and the subsequent liftoff leaves the bottom Pt electrode with a layer of Cu on top of it. The rest of the process flow is the same as a conventional resistive switch.

2.3.3 Limited source resistive switch

Two devices with a limited source of Cu ions were fabricated. The thickness of Cu layer in one of these devices is 12 nm and the second one is 6 nm. The fabrication process is similar to that of simple resistive switching devices until the patterning and development for the topmost electrode. However after the development, instead of depositing 150 nm thick layer of Cu in the automatic mode of PVD 250 (as is the case in a simple resistive switch), the e-beam evaporation of Cu is done in the manual mode to provide the 6nm/12nm layer of Cu and this is immediately followed the deposition of Pt layer with the thickness identical to the thickness of the bottom Pt electrode. So in principle the limited source providing Cu layer and the top Pt electrode layer are patterned together. The subsequent lift off leaves us with the desired device structure.

2.3.4 Cu/TaO_x/Cu device

In these devices the processing steps are almost the same as for the fabrication of a simple resistive switch except for all the metallization steps. The top and bottom electrode here are made of Cu which is deposited using e- beam evaporation of Cu in the automatic mode of PVD 250.

2.3.5 Pt/TaOx/Pt device

The fabrication of these devices was the most difficult compared to the rest, mostly because the adhesion of the topmost Pt later gives a lot of issues. As such, the patterning process step for the topmost electrode had to be optimized in order to obtain a good device. It was found that after the development step, it was critical to do a bake at 100 ° Celsius on the hot plate for 2 min in order to aid in the adhesion of the Pt deposited using the e-beam evaporation.

2.4 Characterization of process steps

In order to make sure that each processing step is performed under optimum conditions, each process step was individually characterized to make sure that each of them is repeatable and gives the best possible results with the process step immediately following/preceding it.

2.4.1 Cleaning Procedures

In semiconductor device fabrication/processing, cleaning is one of the most important process steps which need to be performed especially before a high temperature processing step like solid state diffusion, oxidation or chemical vapor deposition. Contamination of silicon devices results in degradation of device performance and poor reliability and thus it is extremely important to control the contamination of semiconductor devices from particulate, metallic, organic or other contaminants like native oxide. Most of these contamination sources are from the various processing steps and hence it is extremely important to clean the substrate properly during the processing.

There are two major cleaning mechanisms i.e. dry cleaning and wet chemical cleaning and among these two basic mechanisms various cleaning recipes are used to remove the different types of contaminants from the Si surface. In wet chemical cleaning, solvents or acids are used either to dissolve the contaminant by converting it into a soluble compound or to wash it off by force. In dry or vapor cleaning, the contaminants are removed from the wafer surface in the gas phase by converting it into a volatile compound or by knocking it off the Si surface. The most commonly used cleaning solvents in semiconductor processing are acetone, IPA (isopropyl alcohol) and DI (De-ionized) water. Cleaning a wafer surface with acetone, isopropyl alcohol and DI water, in that specific order removes residual organic impurities from the wafer surface.

Any solvent clean of silicon wafers is always followed by a De-ionized (DI) water rinse, subsequent blow drying using a nitrogen gun which is then followed by a dehydration bake.

RCA clean is the most standard wafer cleaning process used in the semiconductor industry to remove residual organic and inorganic impurities from the silicon surface. The RCA clean is a combination of two different cleaning steps called the RCA-1 clean [23] and the RCA-2 clean [24]. While doing the RCA clean, it is extremely important that non-metal wafer tweezers are used so as to prevent the contamination of wafer during the cleaning process. RCA-1 (also called the SC-1 or standard clean-1) is a cleaning procedure used for removing organic residue from silicon wafer surface. RCA-1 cleaning solution is a mixture of water (H_2O), ammonium hydroxide (NH_4OH) and hydrogen peroxide (H_2O_2) with a volume ratio of 5:1:1. The exact procedure to do RCA-1 clean is to add NH_4OH to water in a pyrex beaker and heat it to a temperature of around 70-75 °C on a hot plate and then H_2O_2 is added to the solution. As soon as H_2O_2 is added, the solution starts bubbling vigorously. After 1-2 minutes of adding H_2O_2 , the wafer is immersed into the RCA-1 mixture for 15 minutes. A stir bar may also be placed into the beaker in order to aid the uniform mixing of the solution.

The RCA-1 clean basically works on the mechanism of sequential oxidative desorption and complexing with $H_2O_2-NH_4OH-H_2O$, so in the process the silicon surface gets oxidized and typically it is important to remove the thin oxide layer after the RCA-1 clean. For stripping the oxide layer off the Si surface the wafer is immersed in a solution of H_2O and HF with a volume ratio of 50:1 for about 30 s-1 min and then the wafer is rinsed in the DI water for sufficient time to remove any traces of the acid from it. This process should be repeated as long as the entire oxide layer is stripped off the Si surface. A good test of it is to observe if water is adhering to the surface of the wafer or not. If it is it means the entire oxide layer has not been etched and it needs further immersion in the etchant since silicon dioxide is hydrophilic and silicon surface is hydrophobic.

After the silicon oxide etch, RCA-2 clean is carried out to remove metal impurities as well as alkali contaminants. RCA-2 cleaning solution is a mixture of water (H_2O), hydrochloric acid (HCl) and hydrogen peroxide (H_2O_2) with a volume ratio of 6:1:1. The exact procedure to do RCA-2 clean is to add HCl to water in a pyrex beaker and heat it to a temperature of around 70-75 °C on a hot plate and then H_2O_2 is added to the solution. As soon as H_2O_2 is added, the solution starts bubbling vigorously. After 1-2 minutes of adding H_2O_2 , the wafer is immersed

into the RCA-1 mixture for 10 minutes. Again just as in the case of RCA-1 clean, the RCA-2 clean is also followed by an oxide etch since the RCA- 2 also leaves the surface oxidized.

2.4.2 Thermal Oxidation

After thoroughly cleaning the wafer using RCA-1 and RCA-2 procedure, silicon wafer is oxidized thermally to grow silicon dioxide. The cleanroom facility at Virginia Tech has a thermal oxidation furnace in which wet/dry thermal oxidation can be carried up to the maximum temperature of 1100 ° Celsius for 4 inch wafers. The furnace has 3 thermocouples and when loading the wafers into the furnace, it is made sure that the front of the quartz wafer boat is in line with the middle thermocouple to ensure the uniform oxide growth on all the wafers. The procedure for thermal oxidation is as followed. The clean wafers are loaded on the quartz wafer boat. The furnace temperature is set at 600 ° Celsius and high purity nitrogen gas is purged into the furnace chamber to prevent premature oxidation on the wafer. After this the furnace temperature is set at 1000 ° Celsius all the while keeping the N₂ purge on, as soon as the required temperature of 1000 ° Celsius is achieved, the nitrogen purge is stopped and oxygen gas in introduced into the chamber and dry oxidation of the wafer is carried out at least for 5 minutes. After the dry oxidation run is concluded, wet oxidation is performed. For this the oxygen gas supply is made to pass through a bubbler containing water at about 95-97 ° Celsius and this combination of oxygen and water vapor is introduced into the furnace and wet oxidation is carried out.

The rate of oxide growth dry/wet is predicted by Deal-Grove model [25]. The various factors influencing thermal oxidation include temperature, ambient type (dry O₂, H₂O), pressure inside the chamber, substrate doping and substrate crystallographic orientation. For the devices covered during this work, about 750 nm - 800 nm of silicon dioxide was deposited on the silicon at a furnace temperature of 1050 ° Celsius which takes around 2 hours to complete. After the completion of the wet oxidation run, another run of dry oxidation is performed for 5 minutes. After this the oxygen supply is cut off and nitrogen gas is purged into the chamber and the furnace temperature controller is set at 600 ° Celsius. Once the furnace temperature comes back to approximately 600° Celsius, the wafer boat is taken out of the furnace and allowed to cool down to room temperature before further processing. The thickness of the silicon dioxide film

can be measured by using the Filmetric- interferometer thin film thickness measurement system inside the cleanroom.

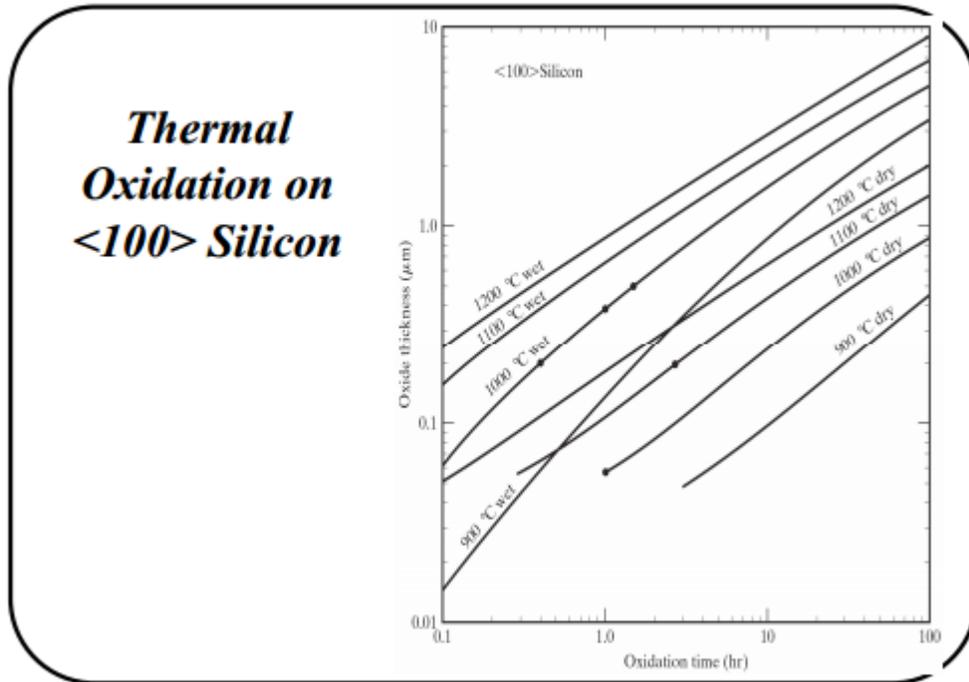
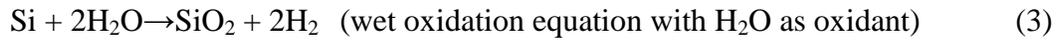
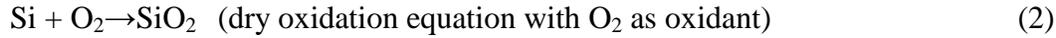


Figure 16: Thermal oxidation of a silicon wafer of crystallographic orientation '100' [26]. Used under fair use, 2012.

2.4.3 Photolithography

In the semiconductor industry photolithography is the most commonly used lithography technique used for transferring patterns from the mask on to the silicon substrates. Photolithography involves the use of a liquid called photoresist which is a photosensitive polymer consisting of three components: a base material (resin), a photoactive compound (PAC) and a solvent. This photoresist is spread out on the silicon substrate in the form of a thin film using a spin coater. The thickness of the photoresist film depends upon the spin coater chuck's rotation speed and photoresist viscosity among many other factors. The properties of the PAC change on the exposure to ultraviolet light thereby either inhibiting or promoting the dissolution of the resin in the developer solution based on the type of photoresist. There are two different types of photoresist available: positive photoresist and negative photoresist. In case of a positive

photoresist, the PAC is deactivated and the photoresist breaks down upon exposure and the exposed areas are washed away using a developer solution leaving the unexposed areas which are insoluble in the developer thereby giving a positive image of the mask in the photoresist. In a negative photoresist, the photoresist in the exposed areas polymerize and are rendered insoluble while the unexposed areas are washed away by the developed solution leaving a reverse image of the mask in the photoresist. A glass photomask patterned with chrome was used here. The portion of the photo mask covered with chrome is opaque and does not allow the ultraviolet light to pass through it while the remaining of the photo mask areas are transparent and allow the UV light to pass through it. The mask aligner MA-6 has been used for all the photolithographic processing. MA-6 is suitable for use with either the I-line (365 nm) or the G-line (436nm) wavelength. Here channel 2 of the MA-6 (436nm wavelength) which is set at a constant intensity of 11.5 mW/cm^2 has been used for exposure of all the samples.

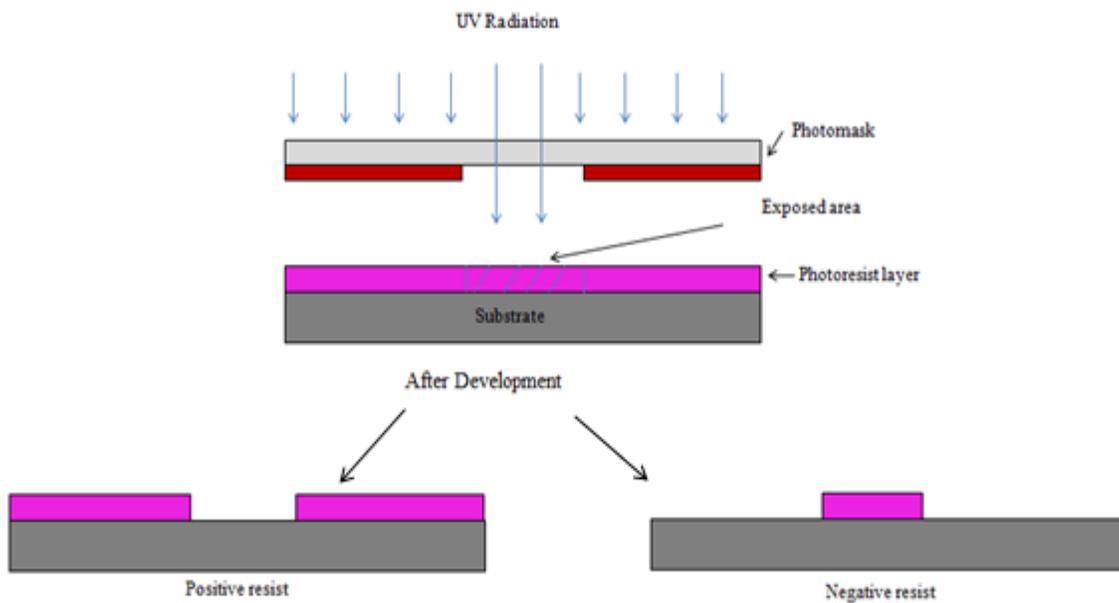


Figure 17: Negative and Positive Photolithography

2.4.4 Mask Layout:

A catalog mask was designed for fabricating the nanocrossbar resistive switches. For the fabrication of a resistive switch, three masks are needed. The first mask is used for patterning the bottom electrode (Pt), the second mask is used for the patterning of the electrolyte (TaOx) and the last or the third mask is used for patterning the top electrode (Cu). There is an additional mask that has devices with size ranging from 35 μm to 1 μm for the two electrodes and 1 μm X 1 μm to 20 μm X 20 μm for the Via points. The mask is designed in such a way that there are 100 devices of each size. Instead of 4 separate masks, the same catalog mask has 4 masks. Any of the 4 masks can be used by rotating the mask by 90° clockwise and placing it on the mask holder. Mask 1 is used for patterning the bottom electrode, mask 2 is used for patterning the solid electrolyte which and Mask 4 is used for patterning the top electrode. Each of these masks has an alignment mark which is located at the bottom left corner. The alignment marks aid in the proper alignment of the device during the various processing steps. Figure 18 shows the complete design of the catalogue mask. Figure 19 and 20 show the design of Mask 4 and Mask 2 respectively.

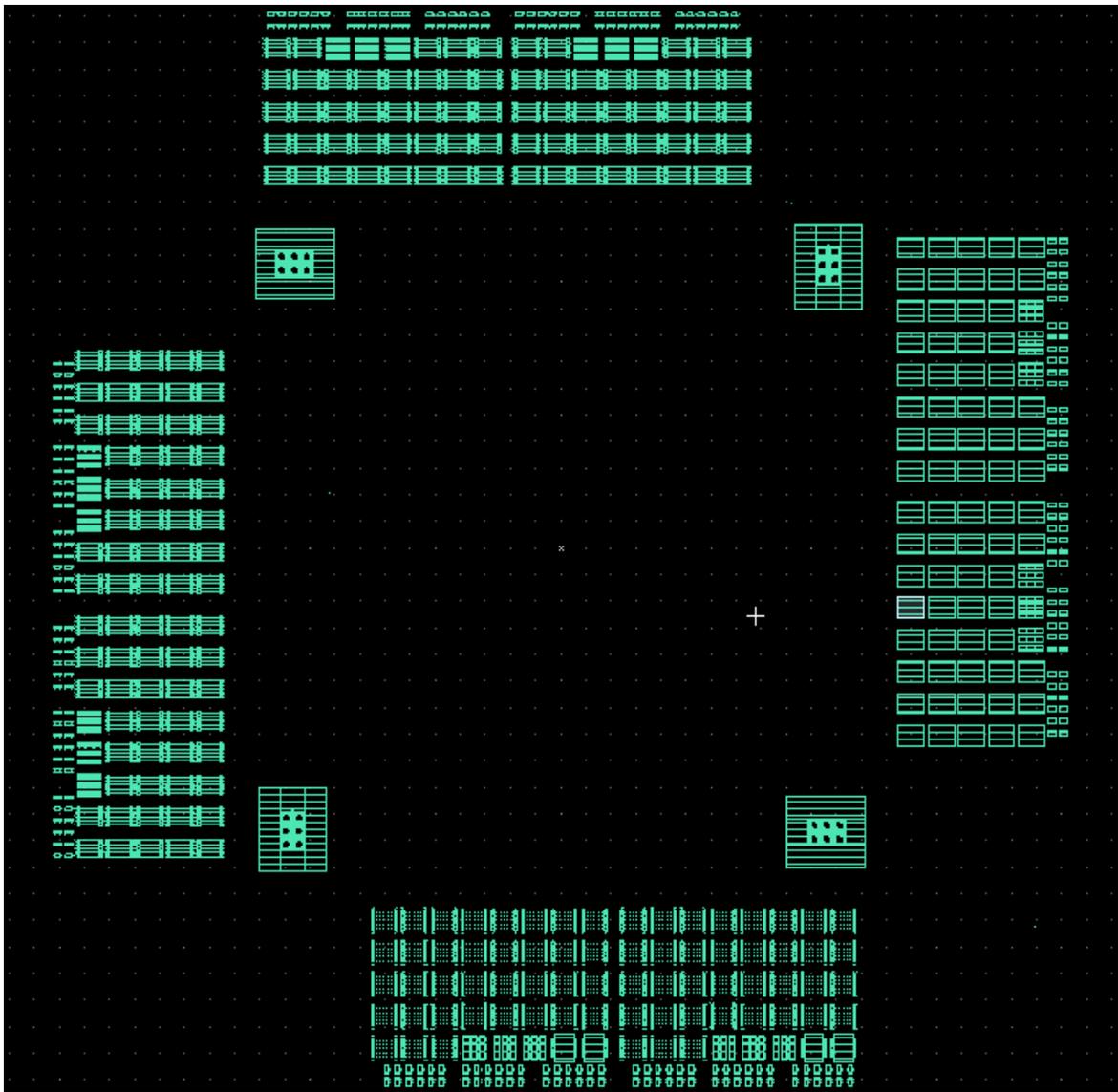


Figure 18: Complete Design of the catalog mask

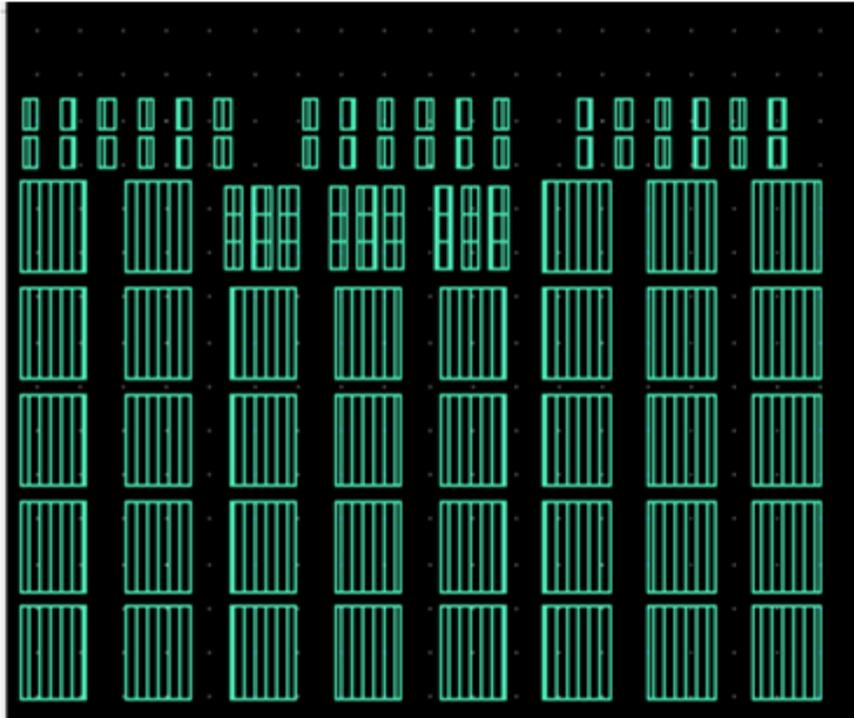


Figure 19: Enlarged view of the mask used for patterning TaOx layer

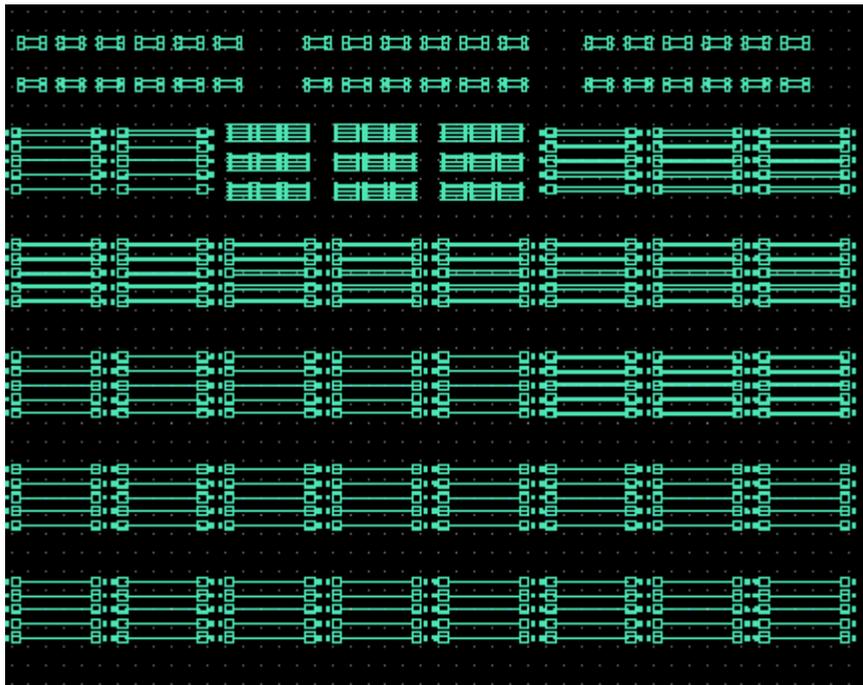


Figure 20: Enlarged view of the mask used for patterning the top electrode

2.4.5 PVD

Physical vapor deposition is a method for depositing thin films on the silicon substrate by the means of actual physical transfer of the source from either a crucible or sputter target on to the substrate surface in the gaseous phase. The PVD tool used in Virginia Tech cleanroom facility is the Kurt Lesker PVD 250 which has been used extensively for e-beam evaporation based thin film deposition during the course of this research. The source material which comes in the form of pellets is preconditioned in a crucible and to start with the deposition the substrate as well as the source present inside the PVD chamber has to be brought to a very low pressure in the range of 2×10^{-6} Torr - 4×10^{-6} Torr. Once this low pressure is achieved a beam of electrons is focused on the crucible thus melting the material inside and the evaporation begins thus coating the inside of the chamber. The chamber also has a quartz crystal which monitors the actual rate of deposition as well as the thickness of the film. The PVD runs both in the automatic and manual deposition mode.

In the automatic mode, the user is required to set the final thickness of the film as well as the average rate deposition rate and then the tool performs the deposition based on the chamber pressure, power ramp rate and current deposition rate. In the manual mode, the user controlled parameters are longitudinal and lateral amplitudes of the e-beam, the effective deposition rate, rate of increase of the current. There is a quartz crystal inside the PVD chamber which monitors the deposition rate and reports the thickness of the film to the user based on the density and Z-ratio of the material being evaporated. Z-ratio of a material is defined as the parameter that corrects the frequency change to a thickness transfer function for the effects of acoustic impedance mismatch between the crystal and the evaporated material. It is important to note down the life of the crystal before starting the deposition and the crystal needs to be replaced if its' life falls below a value of 33%.

The fabrication of the devices covered under this work requires the evaporation of Ti, Pt, TaO_x and Cu. While Ti and TaO_x as well as the Cu for the top electrode can be evaporated using the automatic mode, however the deposition of Pt and intermediate layers of Cu require the operation of the PVD tool in the manual mode. Pt while being evaporated tends to spit out of the crucible everywhere inside the chamber and in order to prevent this, the current needs to be ramped up and ramped down very slowly which can be achieved only via manual mode. The Z ratio of Pt is 0.245 and the density is 21.45 g/cm³. As for δ -Cu deposition very thin layers of Cu

need to be deposited and this can be done only via the manual mode. The Z ratio of Cu is 0.437 and the density is 8.93 g/cm^3 . For a chamber pressure of 2×10^{-6} Torr, a deposition rate of 1 \AA/sec is achieved at a current of 180 mA. For the deposition of very thin layers of Cu, a detailed study of the effective deposition rates at different current intensities was performed. It was found that at 2×10^{-6} Torr of chamber pressure, a deposition rate of 0.004 \AA/sec is achieved at 65mA of current. Again at 2×10^{-6} Torr of chamber pressure, a deposition rate of 0.1 \AA/sec is achieved at 71mA of current. At the same chamber pressure, a current of 75mA gives a deposition rate of 0.4 \AA/sec and a current of 80 mA gives a deposition rate of 0.7 \AA/sec . It was found that for the deposition of Cu layers as thin as 3 nm, the e-beam shutter needs to be opened for approximately 46 sec at 80 mA current. Also for the deposition of TaOx, e-beam evaporation of pure Ta₂O₅ pellets was carried out without any oxygen injection in the chamber. The Z ratio of Ta₂O₅ is 0.3 and the density is 8.2 g/cm^3 . The deposition rate is kept at 2 \AA/sec and it is found that the average current during the deposition is 140 mA.

2.4.6 ALD

Atomic layer deposition in principle is chemically similar to chemical vapor deposition since the deposition of thin films is based on the mechanism of chemical reaction on the surface of the substrate. ALD reaction however breaks the CVD reaction into two half reactions. ALD is a method of depositing thin films on the substrate surface with a precision of 0.1 \AA per cycle. Typically an ALD reaction uses two chemicals known as precursors and each of these precursors are kept separate during the reaction. The substrate is exposed to each of these precursors sequentially and after each exposure, the chamber is purged with nitrogen or argon to remove the excess precursor from the last exposure before the surface can be exposed to the new precursor. ALD is a self limiting process and the films grown are conformal and it is ideal for the deposition of high dielectric materials like oxides. In an attempt to deposit pure Ta₂O₅, the ALD system in Virginia Tech cleanroom facility was used. However it was found that the subsequently grown films had adhesion issues with the bottom Pt layer and lift off of the electrolyte layer removed the entire Ta₂O₅ even from the desired areas of the mask pattern. So eventually PVD was used all the thin film deposition processes in this research.

2.4.7 Lift off:

Liftoff and etching are two most commonly employed patterning techniques employed in combination with photolithography. While etching is a subtracting technique, liftoff is an additive process. Negative photoresist are best suited for lift off processes. Acetone has been used as the liftoff solvent. The liftoff of Pt is comparatively very easy since Pt lifts off within 2-3 minutes of the wafer being immersed into the acetone. It is to be noted that we do not employ ultrasonic mechanical vibrations while doing the lift off of platinum since it might lead to the lift off of Pt from the needed areas. The procedure for liftoff is to immerse the wafer in acetone and then subject it to ultrasonic vibrations for 10-11 minutes.

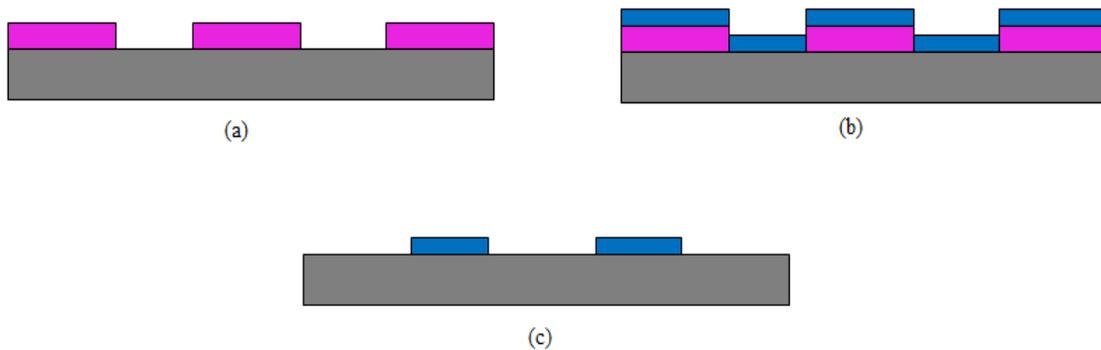


Figure 21: Lift off Process (a) Photoresist coat and patterning, (b) Thin film deposition and (c) removal of photoresist and thin film above it, after lift off

2.4.8 Photoresist recipe

As already mentioned in the process flow, negative or image reversal photolithography technique had been used for the fabrication processing of nanocrossbar resistive switches. For obtaining a reverse image of the mask lines on the photoresist pattern, an image reversal bake followed by a flood exposure is needed after the first ultraviolet exposure. For this purpose the photoresist AZ 5214 E-IR is used which can be used for either positive or negative photolithography. Before the application of the photoresist the wafer first needs to be cleaned using the most widely used solvent cleaning technique ie acetone and IPA. It is extremely important to clean the wafer with IPA thoroughly to remove any traces of acetone from the substrate. After this the wafer is cleaned with de-ionized water for more than 2-3 minutes. This is followed by blow drying using a nitrogen gun and eventually by a dehydration bake done on the hot plate at a temperature of 100 ° Celsius for about 4-5 minutes. It is very important to do

the dehydration bake before photoresist coating because any residual moisture reduces the photoresist adhesion to the silicon substrate. After this hexamethyldisilazane (HMDS) which promotes photoresist adhesion on silicon and other substrates as well is spin coated on the substrate surface. About 8 drops of HMDS is spun on the substrate at 4000 rpms for 45 sec. This is followed by the softbake of HMDS at 100 ° Celsius for 1 minute on the hot plate. Initially baking of HMDS was not done and the smaller features could not sustain the liftoff procedure and the metal lines of features of 1µm to 2 µm used to liftoff along with the photoresist. Baking of HMDS improves the adhesion of the photoresist and hence the resolution of the smallest metal lines. After this the photoresist is spin coated on to the substrate so as to obtain a photoresist layer of thickness slightly greater than 1 µm. The photoresist thickness depends on the viscosity of the photoresist as well as the rotational speed of the spin coater. In order to ensure the uniformity of the photoresist, the spin coating of AZ 5214 E-IR is done in 3 steps. The spin coater is set to rotate at a speed of 800 rpms for 5 sec, 3000 rpms for 35 sec and then 500 rpms for 5 sec in the end.

Photoresist spin coating is followed by soft-bake done on the hot plate at 100 ° Celsius for 1 min 20 sec to evaporate the solvent thereby improving resist adhesion. After this UV exposure is done using the constant intensity channel-2 of the MA-6 (435 nm wavelength and an intensity of 11.5mW/cm²) for about 5.4 seconds. During the initial fabrication processing the contact mode used was soft contact since a glass mask is being used however it was observed that the smaller features could not be transferred from the mask on the substrate, so the contact mode was changes to vacuum contact which provides a much higher resolution. The next step is the reversal bake on the hot plate at 117 deg for 1 min 40 sec which renders the exposed resist areas insoluble in the developer. However it is very important to have a delay of at least 1 min between the first UV exposure and image reversal bake for a 1µm thick photoresist film. This delay ascertains the outgassing of nitrogen to prevent bubble formation during reversal bake. Then the flood exposure is performed which is at least greater than 200 mJ/cm² (g-line for about 60 sec). This second exposure also called as the flood exposure since no mask is used during this exposure and it increases the solubility of the unexposed resist areas and during the process improves developer's selectivity and resolution properties. Flood exposure is then followed by the development process. The developer solution used for AZ 5214 E-IR is a solution of AZ 400K and water in the ratio of 1:4. The development time is usually 15-20 sec and after the

development the negative image of the mask is obtained on the substrate. The wafer is then rinsed in the DI water for more than 1 minute and then blow dried with a nitrogen gun and the remaining photoresist pattern is observed under an optical microscope to ensure correct pattern transfer.

Chapter 3: Simple Resistive Switches

This chapter deals with the detailed characterization of simple resistive switches which have a Pt/TaO_x/Cu stack structure. This chapter serves as the basis for comparison of the resistive switching behaviors of all the other resistive switches fabricated throughout the course of the current research work.

3.1 I-V Characteristics

Given below is a simple IV characteristics graph for a simple memory cell when the dual voltage sweep is performed on it, i.e. first a positive sweep is done from 0 V to 1.5 V where the current gets limited by the compliance current limitation and the switch goes into the low resistive state and then the voltage is swept from 1.5 V to 0 V and then from 0 V, it is swept in the negative regime up to a maximum negative voltage of -1.2 V where no compliance current limitation is exerted on the switch and then the final step of the sweep is done from -1.2 V to 0 V to bring it back to the origin once again. The magnitude of compliance current used during the positive sweep was 1 mA.

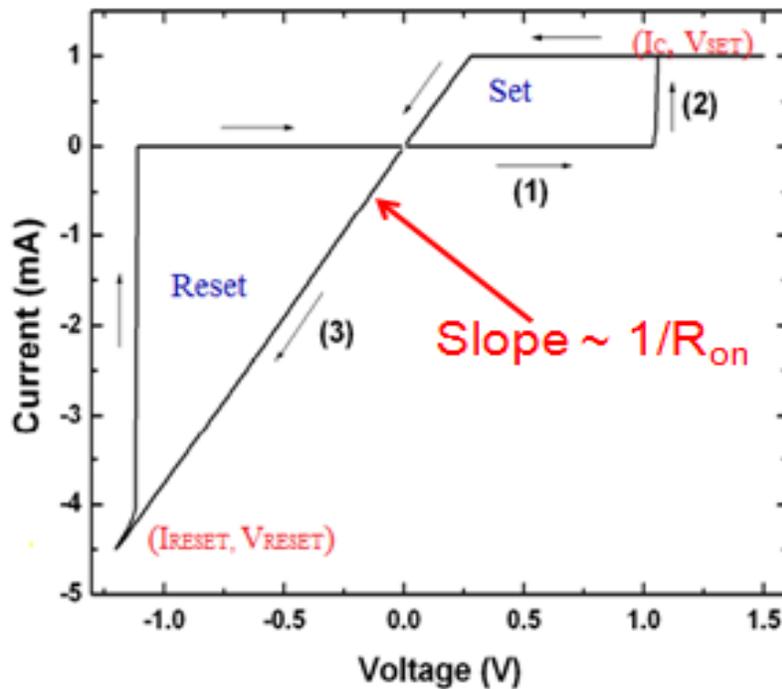


Figure 22: Hysteresis Curve of simple resistive switch

3.2 R_{ON} vs. size

As mentioned earlier, these devices have cells ranging from a minimum size of $1\mu\text{m}^2$ to a maximum of $1225\mu\text{m}^2$. So in order to study the effect of scaling the device sizes on the various device parameters, a comparison of the R_{ON} vs. the cell area or size was done and it was found that R_{ON} or the ON state resistance is independent of the area. The read voltage is 0.01 V and the sweep rate is 0.01 V/step. The non dependence of R_{ON} on device area indicates the existence of a single filament inside the cell area, when the device is in the SET state.

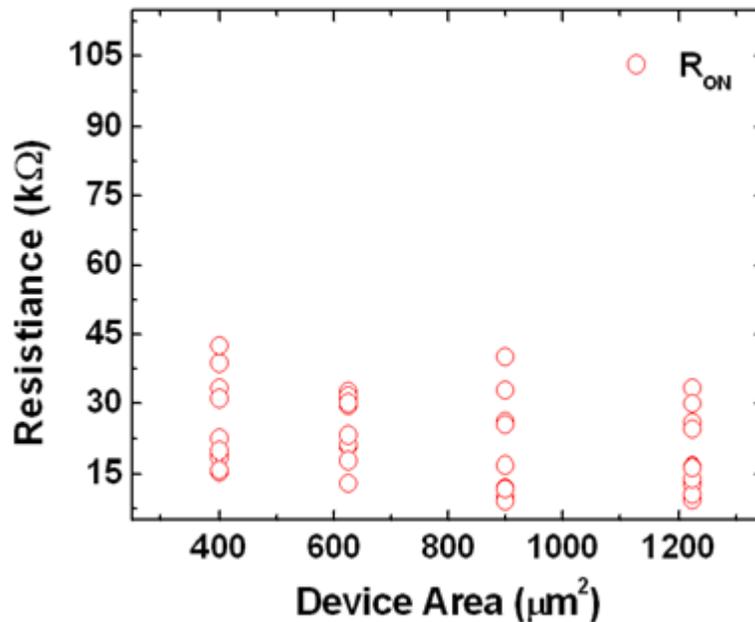


Figure 23: Plot of R_{ON} variation with device area

3.3 R_{OFF} vs. size

When the same study was performed on the resistance of the switch when it was in the higher resistive state, R_{OFF} was found to be dependent on the cell area and hence it is a more homogenous effect. R_{OFF} spans over more than 1 order of magnitude and it can be attributed to a variety of causes such as wide variation of local temperature during Joule's heating, variation of local conductivity, incomplete rupture of the Cu filament, process variation during the deposition of the oxide layer as well as the roughness of the metal and electrolyte surface.

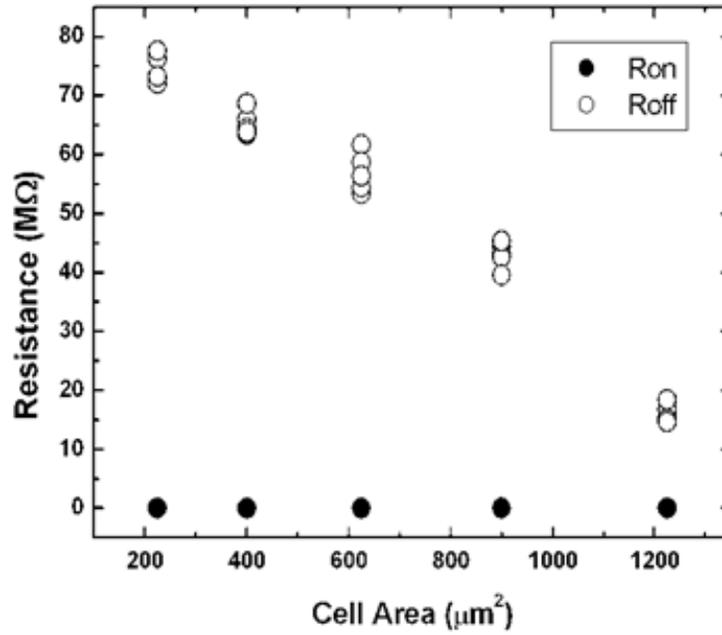


Figure 24: Plot of R_{OFF} and R_{ON} variation with area

3.4 R_{ON} vs. Compliance current

From the literature it is widely established that R_{ON} is inversely proportional to the compliance current and during the course of characterization of the devices under study it was observed that this relationship in fact holds true.

$$R_{\text{ON}} = C/I_C \quad (4)$$

It is quite understandable since a larger compliance current would lead to the formation of a much stronger bridge. A higher compliance current leads to a stronger electric field and as a result promotes more lateral growth for the formation of a stronger bridge/filament whereas a lower compliance current results in the formation of a weaker bridge due to lesser lateral growth of the filament.

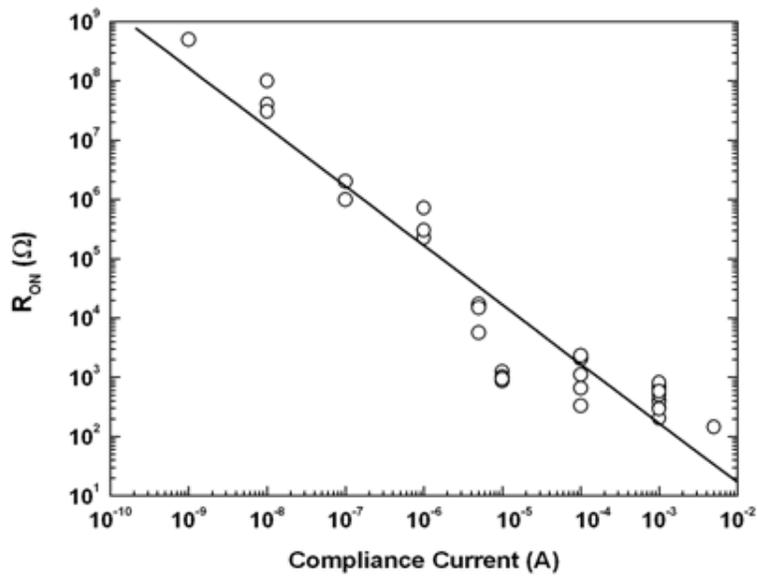


Figure 25: Variation of R_{ON} with Compliance Current [27]. Used under fair use, 2012.

3.5 V_{SET}/V_{RESET} Range

Although smaller SET and RESET voltages are observed, the major ranges of V_{SET} and V_{RESET} are (0.5 V, 2 V) and (-0.5 V, -1.5 V), respectively.

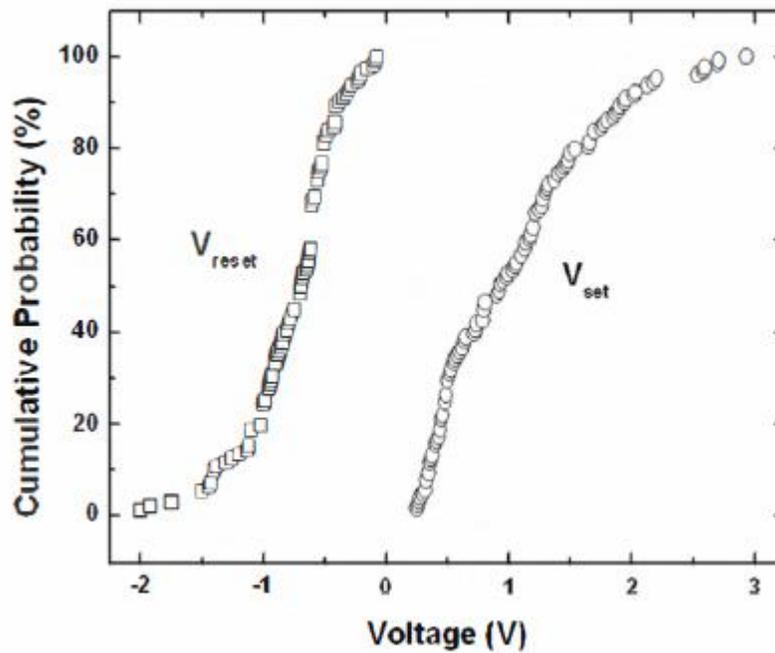


Figure 26: V_{SET}/V_{RESET} of Cu/TaOx/Pt resistive devices [27]. Used under fair use, 2012.

Chapter 4: Volatile switching of CF in Pt/ δ -Cu/TaO_x/Cu

The primary motivation behind the fabrication of these devices was to study the effect of the intermediate copper layer on the SET and RESET processes. In these devices a novel phenomena was observed. These devices show evidence of volatile switching of the conductive filament. Volatile switching of the conductive filament means that once the conductive bridge has been established at a certain finite voltage V_{SET} , the device remains in the low resistive state (LRS) only as long as the applied voltage is maintained at the same level. As soon as the applied voltage is 0 V or approaches 0 V, the device reverts back to high resistive state (HRS), thus rendering a RESET operation redundant. In other words the LRS which is characterized by the existence of the conductive filament is only dynamically stable as long as high enough voltage is applied.

4.1 I-V Characteristics

The thickness of the Cu δ - layer between the TaO_x and the Pt bulk electrode is 6.5 nm. It is believed that the δ -Cu layer remains intact after the processing of the entire device because of low Cu diffusivity in TaO_x at 300K since the entire processing has been done at room temperature. The measured resistance ratio of the HRS to LRS is 10^2 to 10^5 . Figures 27 and 28 show 15 consecutive volatile switching cycles of a Pt/ δ -Cu/TaO_x/Cu cell in the linear and log scale.

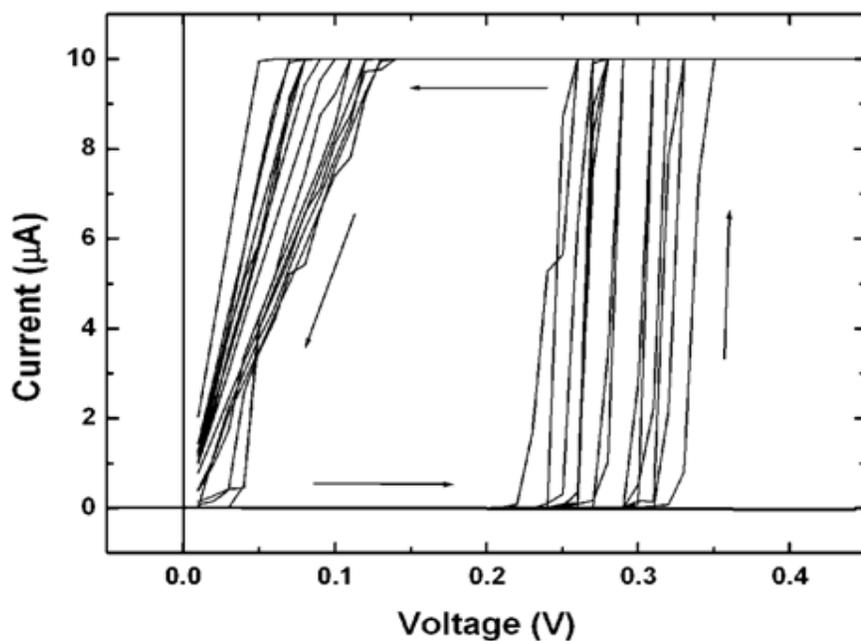


Figure 27: Fifteen consecutive volatile switching curves of a Cu/TaO_x/δ-Cu/Pt device in linear scale (CC :10μA)

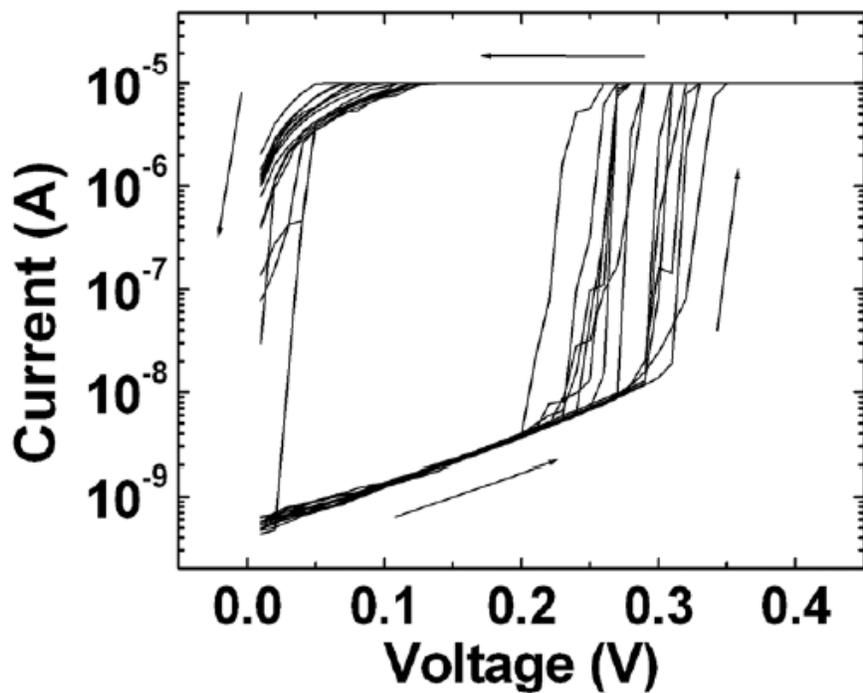


Figure 28: Fifteen consecutive volatile switching curves of a Cu/TaO_x/δ-Cu/Pt device in log scale (CC :10μA).
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4.2 Volatility Hypothesis

The reason for this spontaneous dissolution of the conductive filament (CF) is an upset balance between the field-supported Cu^+ flux (F_{Cu^+}) and the self diffusion flux of Cu (F_{Cu}) in the CF and through the interface between the Cu bridge and the Cu δ -layer on the Pt electrode as shown conceptually in the Figure 29 (b). In the absence of the Cu δ -layer, as is the case in conventional devices, the Cu diffusion flux at the interface of CF with Pt electrode is null because of the ion stopping power of the inert Pt electrode as shown in Figure 29 (a). When the device is in the SET state, only the F_{Cu^+} flux is significant. The F_{Cu} flux which is capable of depleting the Cu atoms from the CF exists only at the tip of the CF touching the Cu electrode. The radius of the contact cross-section between the filament and the Cu electrode is less than 10 nm, as a result F_{Cu} is very small. Hence while being operated in the positive regime the bridge tends to strengthen thus decreasing its resistance in the process. When a δ -layer of Cu is introduced in the conventional stack, it enables a Cu diffusion flux from the established Cu bridge at the broad base (on the Pt side i.e. opposite end to the tip of the bridge) into the δ -layer and this flux is further enhanced by the elevated local temperatures from Joule's heating. This Cu self diffusion flux (F_{Cu}) tends to remove Cu from the CF. If the removal of Cu is larger than the incoming Cu^+ flux (F_{Cu^+}), the CF is bound to dissolve.

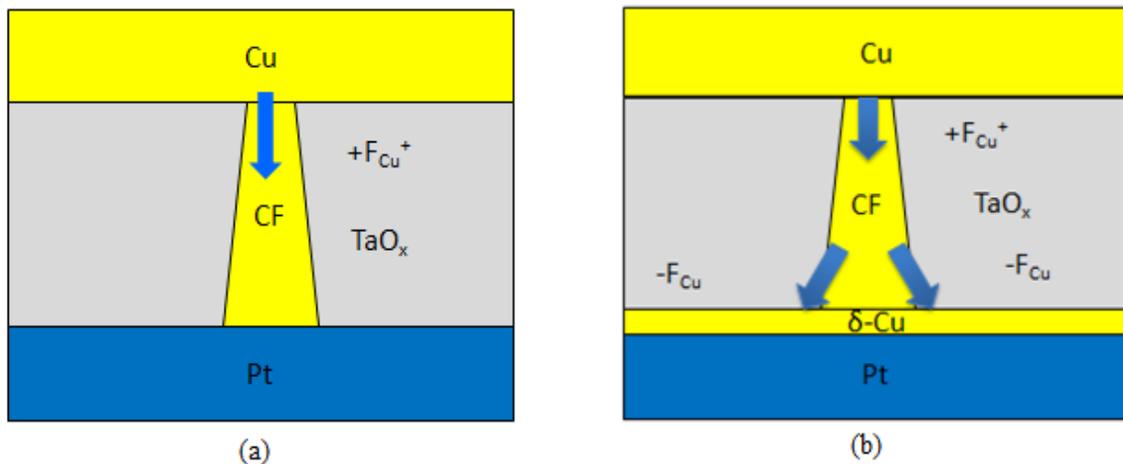


Figure 29: Conceptual view of the Cu^+ and Cu fluxes in (a) non volatile switching in Pt/TaO_x/Cu devices (b) volatile switching in Pt/ δ -Cu/TaO_x/Cu devices.

For devices with 5 nm to 8 nm thick Cu δ -layer, slightly increasing the thickness of δ -layer may lead to larger F_{Cu} . Beyond this critical thickness range, the F_{Cu} flux will cease to depend on the thickness of the δ -layer and would start to behave like a bulk Cu electrode.

4.3 Verification of Hypothesis

4.3.1 Cu/TaO_x/Cu device

For the verification of the proposed hypothesis, Cu/TaO_x/Cu devices were fabricated and it was found that a stable Cu bridge formation cannot be observed. The Cu atoms of the CF formation dissolve quickly in the Cu counter electrode and as such Cu bridge formation is not stable.

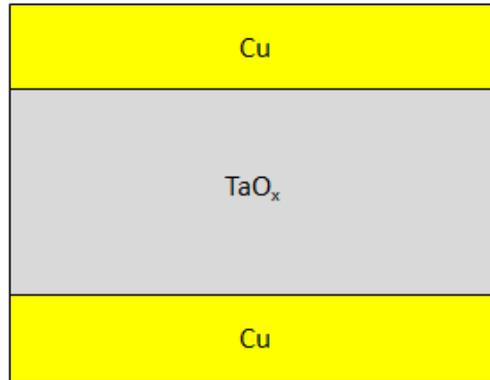


Figure 30: Structure of Cu/TaO_x/Cu device

4.3.2 Interrupted Sweep Test

To further test this theory of Cu self diffusion flux, the voltage for the SET operation for the δ -Cu devices was swept in the positive direction and then back to 0. However before reaching 0V, the voltage sweep was suspended at a finite voltage and let sit for some time. Figure 31 shows the results of the interrupted sweep. For curves 1 and 2, the negative sweep has been halted at 0.2 V and 0.15 V, respectively. An abrupt current drop is observed in the I-V characteristics, which is equivalent to increased resistance of the Cu bridge, but it stabilizes at a lower value indicating that a Cu bridge is still in place with a higher R_{ON} resistance. Thus the CF stabilizes itself by increasing the R_{ON} and thus reducing Joule's heating and as a result F_{Cu} . For curve 3, however the negative voltage sweep was halted at 0.1 V itself and it is found that the resistance changes to the level of the R_{OFF} state, indicating the rupture of the CF. For curve 1 and 2, the voltage across the solid state electrolyte is still large enough to support a larger F_{Cu}^+ as compared

to F_{Cu} . For curve 3 however F_{Cu}^+ decreases significantly lower than F_{Cu} thus leading to the rupture of the bridge. Curve 0 shows an interrupted sweep back to 0 V. At sufficiently small voltages, the F_{Cu}^+ flux is too small to replenish the Cu atoms in the bridge lost due to the diffusion at the interface of CF and the Cu δ -layer.

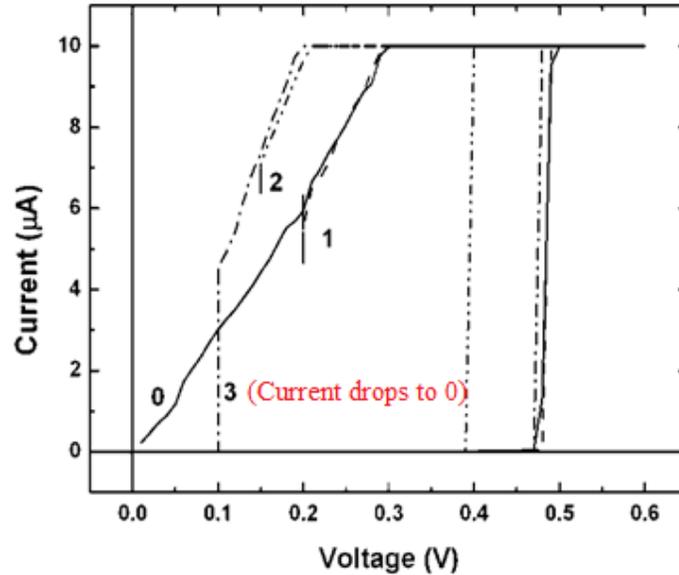


Figure 31: Resistive state transitions during the volatile switching operations. For curves 1, 2 and 3, the sweep is halted at a small but non-zero voltage. Reprinted with permission from [Tong Liu, Mohini Verma, Yuhong Kang, and Marius Orlowski, Applied Physics Letters, Vol. 101, Page 073510 – 073514, (2012)]. Copyright [2012], American Institute of Physics.

4.4 Nonvolatile Switching

The volatile switching behavior as described in the previous sections was observed under a low compliance current of 10 μ A. The same cell when used at a higher value of compliance current of about 1 mA shows consistent non-volatile switching behavior. The Figure 32 below shows two consecutive non volatile switching cycles of the same cell under a higher compliance current of 1 mA. A RESET operation now becomes necessary to rupture the CF as the Cu bridge now becomes nonvolatile. V_{RESET} voltage is found to be about -0.6V. After the RESET, the same device can be reliably operated in the volatile mode if the compliance current is kept below several hundreds of μ A. Thus the same δ -Cu device can be switched reliably from volatile to non volatile behavior.

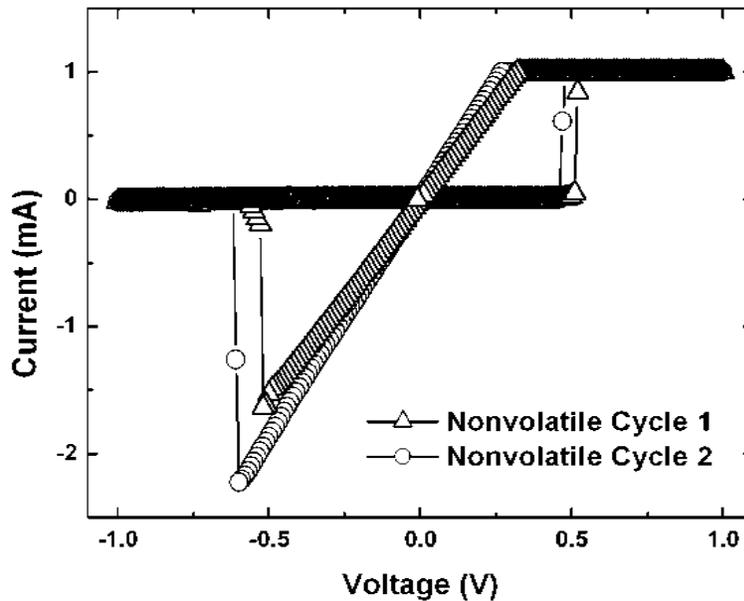


Figure 32: Non volatile switching in Pt/ δ -Cu/TaO_x/Cu devices at high compliance current. Reprinted with permission from [Tong Liu, Mohini Verma, Yuhong Kang, and Marius Orlowski, *Applied Physics Letters*, Vol. 101, Page 073510 – 073514, (2012)]. Copyright [2012], American Institute of Physics.

4.5 Volatile Switching vs. Nonvolatile Switching

Both the volatile (in δ -Cu devices) and nonvolatile (in conventional resistive switches) resistive switching behaviors were characterized and compared with each other. The retention property of the two different switching behaviors was also characterized and it was found that the volatile cells are characterized by a retention time less than 0.5 seconds whereas the retention for nonvolatile devices is at least 10^6 seconds. The SET voltages for volatile devices V_{SET} is found to be largely independent of the voltage ramp rate as shown in Figure 33 in contrast to conventional nonvolatile devices [28]. Again the V_{SET} for volatile devices is found to be significantly lower than that of the conventional Cu/TaO_x/Pt devices which makes them useful for low power application. Similar to the nonvolatile resistive switches, the ON-state resistance R_{ON} depends on the compliance current I_c during the SET operation. The relation can also be fitted by a reciprocal function, $R_{ON} = K/I_c$, as shown in Figure 34. The distributions of R_{ON} , R_{OFF} , and V_{SET} are shown in Figures 35 and 36. As it can be seen from Figure 35 and 36, with the Cu δ -layer, tighter distribution of V_{SET} , R_{OFF} , and R_{ON} are obtained than for nonvolatile Cu/TaO_x/Pt devices. The improvement in V_{SET} distribution of the volatile Pt/Cu/TaO_x/Cu

device over the conventional nonvolatile devices is tenfold as shown in Figure 36. In general, the insertion of a Cu δ -layer with adjusted thickness below 6.5 nm offers an additional control parameter to optimize also nonvolatile switching behavior with much tighter V_{SET} , R_{OFF} , and R_{ON} distributions than the conventional devices.

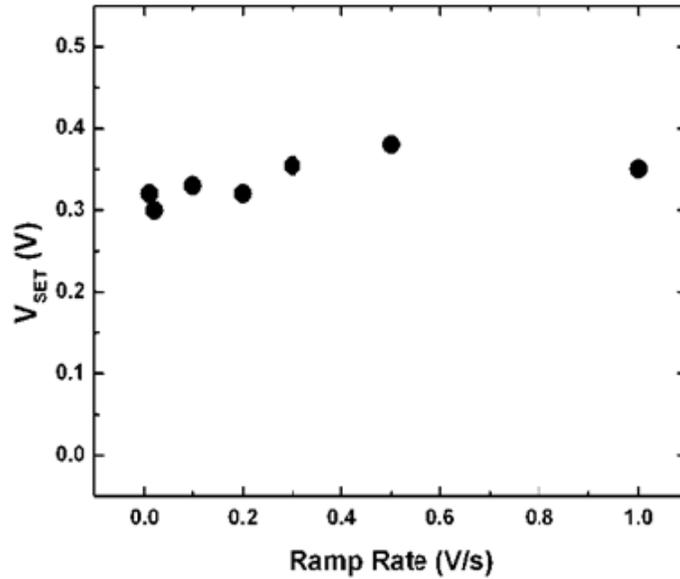


Figure 33: V_{SET} of volatile switching devices at different ramp rates. Reprinted with permission from [Tong Liu, Mohini Verma, Yuhong Kang, and Marius Orlowski, Applied Physics Letters, Vol. 101, Page 073510 – 073514, (2012)]. Copyright [2012], American Institute of Physics.

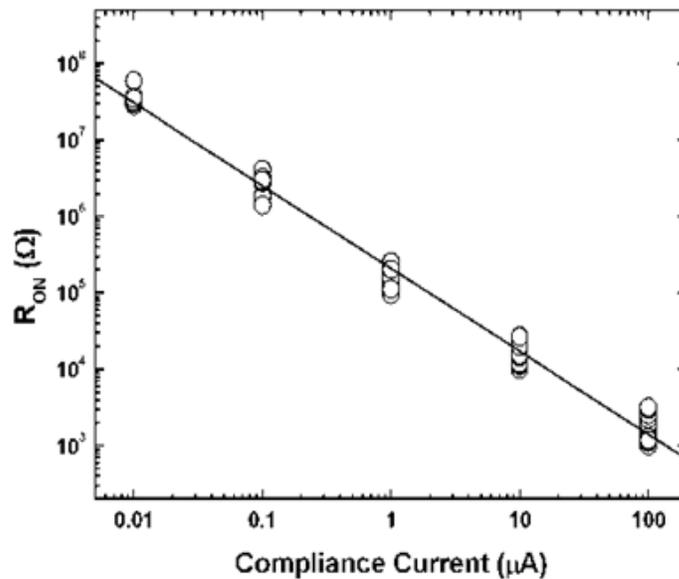


Figure 34: Dependence of R_{ON} on compliance current. Reprinted with permission from [Tong Liu, Mohini Verma, Yuhong Kang, and Marius Orlowski, Applied Physics Letters, Vol. 101, Page 073510 – 073514, (2012)]. Copyright [2012], American Institute of Physics.

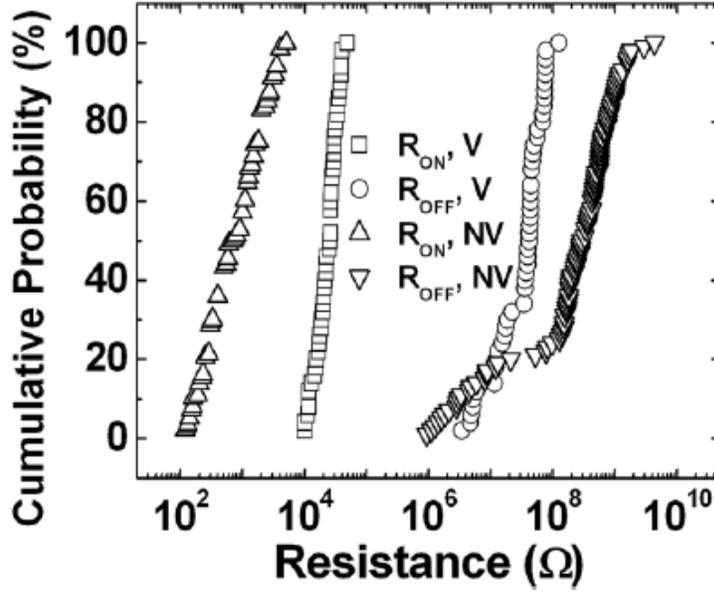


Figure 35: R_{ON} and R_{OFF} distributions of volatile (V) and nonvolatile (NV) devices. Reprinted with permission from [Tong Liu, Mohini Verma, Yuhong Kang, and Marius Orlowski, Applied Physics Letters, Vol. 101, Page 073510 – 073514, (2012)]. Copyright [2012], American Institute of Physics.

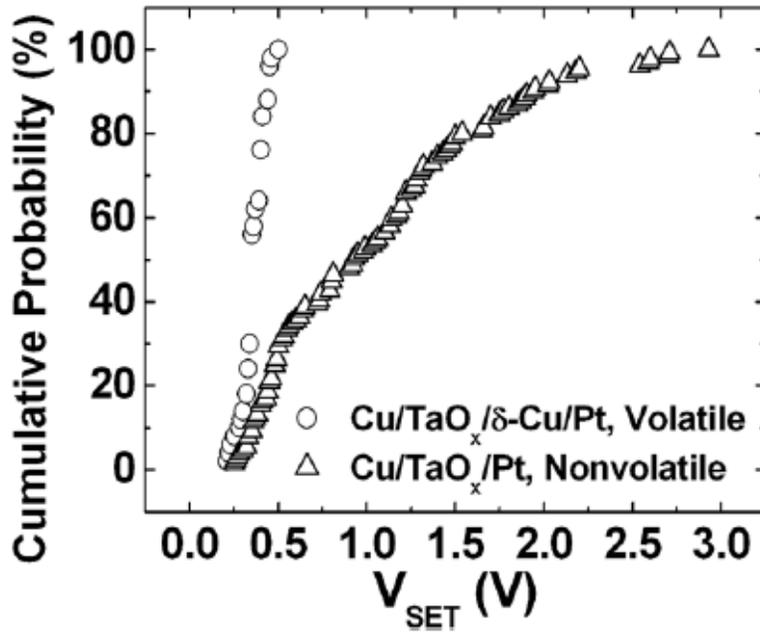


Figure 36: V_{SET} distribution of volatile and nonvolatile devices. Reprinted with permission from [Tong Liu, Mohini Verma, Yuhong Kang, and Marius Orlowski, Applied Physics Letters, Vol. 101, Page 073510 – 073514, (2012)]. Copyright [2012], American Institute of Physics.

Chapter 5: Resistive Switching of CF in Pt/TaO_x/Cu/Pt

This experiment was carried out in an attempt to achieve a better understanding of the mechanism of formation of Cu CF as well as the diffusion of Cu ions in the electrolyte and the subsequent redistribution of Cu atoms in the switch structure if the source of Cu ions is limited. The source of Cu ions (needed to form a CF) was limited through the fabrication of a device which has a Pt/TaO_x/Cu/Pt structure, i.e. an extremely thin layer of Cu is introduced in between the electrolyte and the top electrode which is identical to the bottom electrode (inert Pt electrode). Thus this device has a symmetrical structure in terms of selection of the two electrodes, however a slight asymmetry is introduced in the form of the thin Cu layer (12 nm). It was observed that this device typically tries to achieve symmetry through the diffusion of Cu ions so as to distribute the Cu symmetrically on both sides of the electrolyte. In addition to this these devices also show evidence of co-existence of multiple filaments in the solid electrolyte.

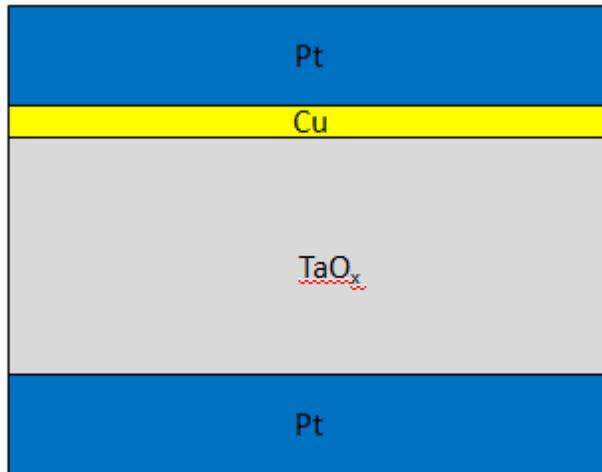


Figure 37: Structure of a limited Cu source resistive switch.

5.1 12 nm limited source device

5.1.1 DC Sweep with compliance current

These devices are capable of being SET (positive bias applied to the top Pt electrode, bottom Pt kept grounded) and RESET (negative bias applied to the top Pt electrode, bottom Pt kept grounded) similar to conventional resistive switches although with slightly higher SET voltages

than conventional Pt/TaO_x/Cu devices. Several of these devices, however show an interesting phenomena which is discussed in detail underneath.

The characterization of limited Cu source device (12 nm thick Cu layer) has been done with a compliance current of 1 mA and DC sweep ranging from 0V to ± 4 V. The figures that follow along with the I-V graphs describe the ongoing mechanism in detail.

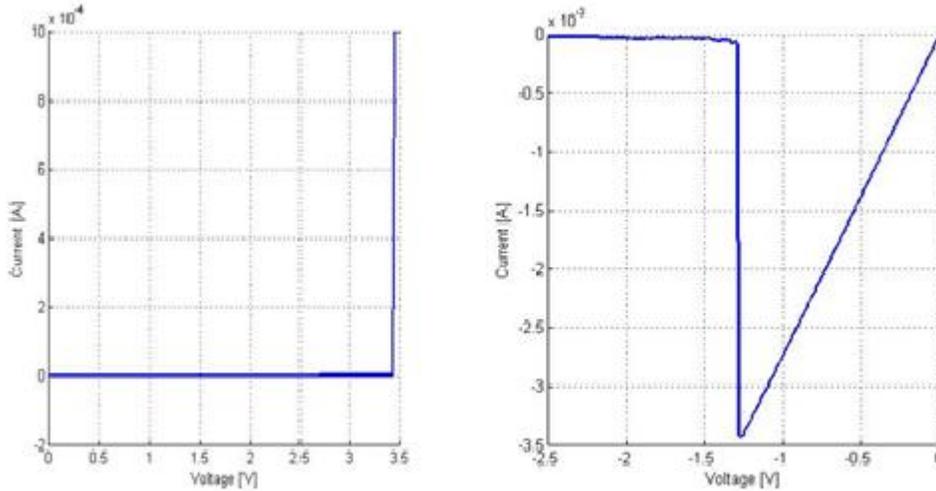


Figure 38: Form and Reset

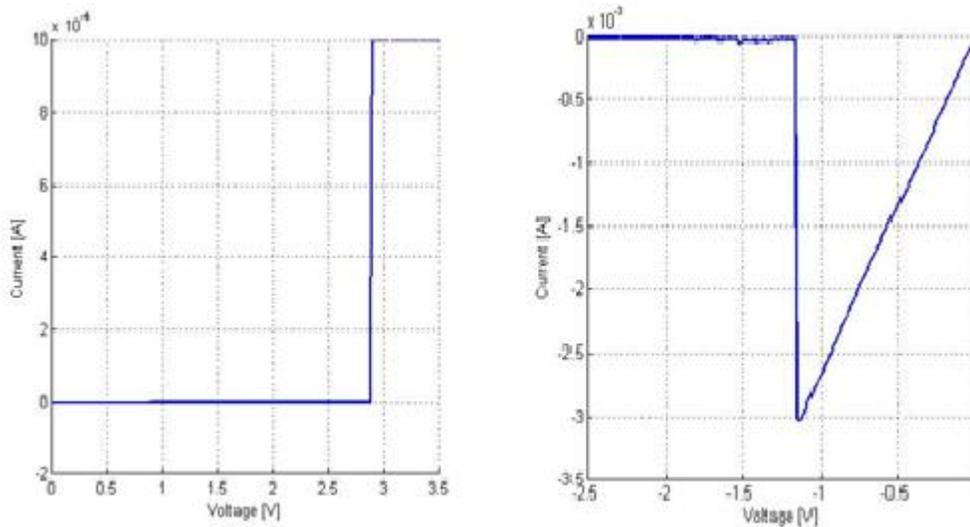


Figure 39: Set 1 and Reset 1

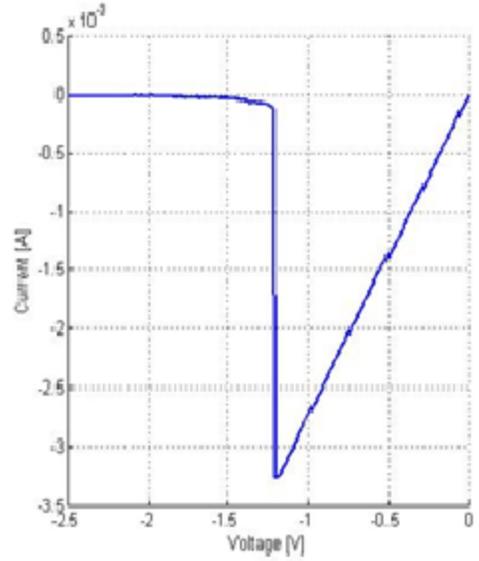
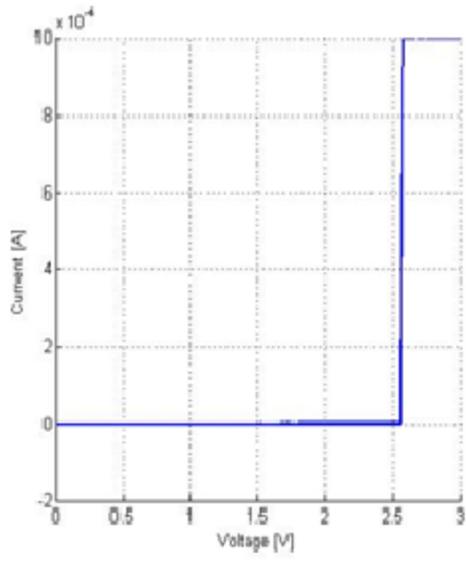


Figure 40: Set 2 and Reset 2

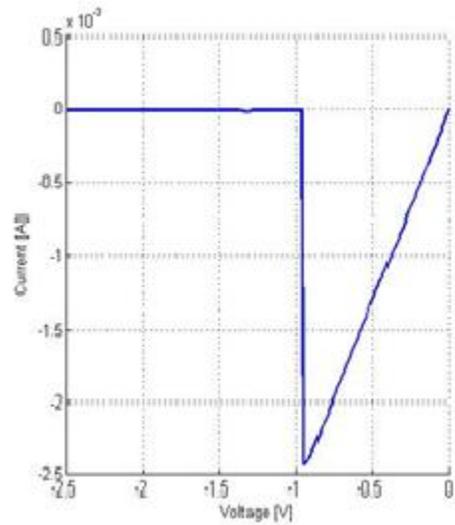
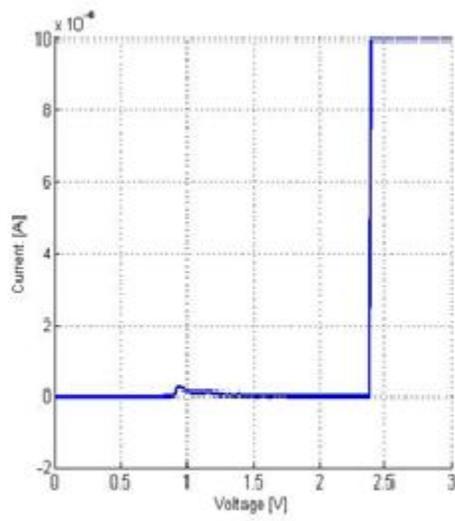


Figure 41: Set 3 and Reset 3

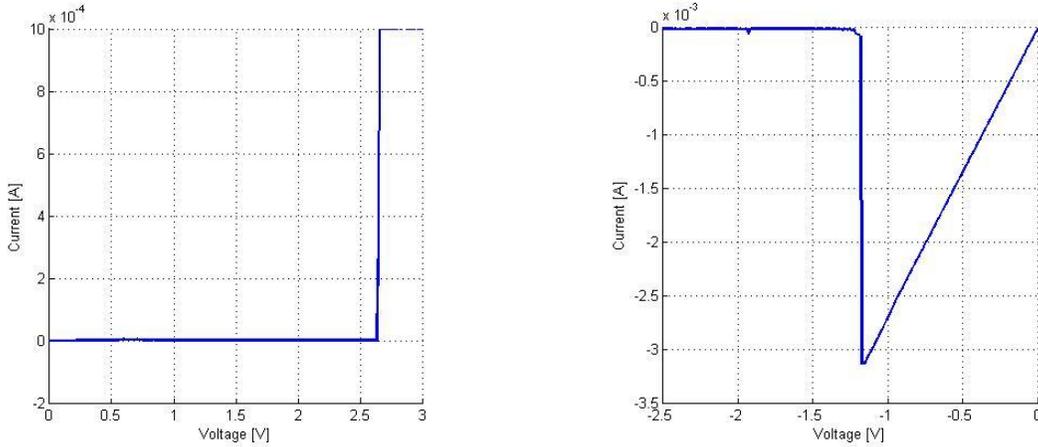


Figure 42: Set 4 and Reset 4

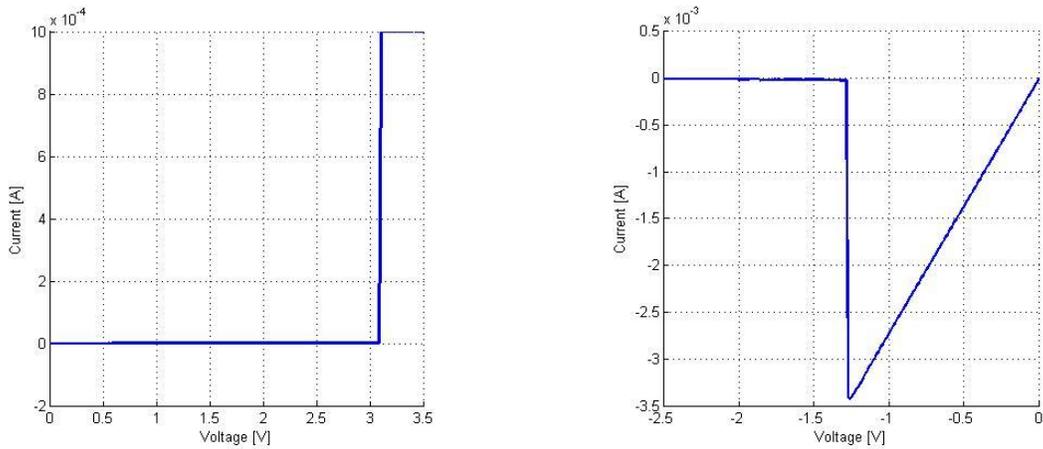


Figure 43: Set 5 and Reset 5

One of the cycles turns out to be volatile, as clearly seen below in Figure 44, the RESET I-V characteristics show that the current remains 0 until about -0.8 V and then jumps to 0.5 mA for a brief interval of time before going back to 0 again, clearly indicating the volatility of the CF as the filament bridge is unable to sustain itself against the elevated local temperature caused by Joule's heating.

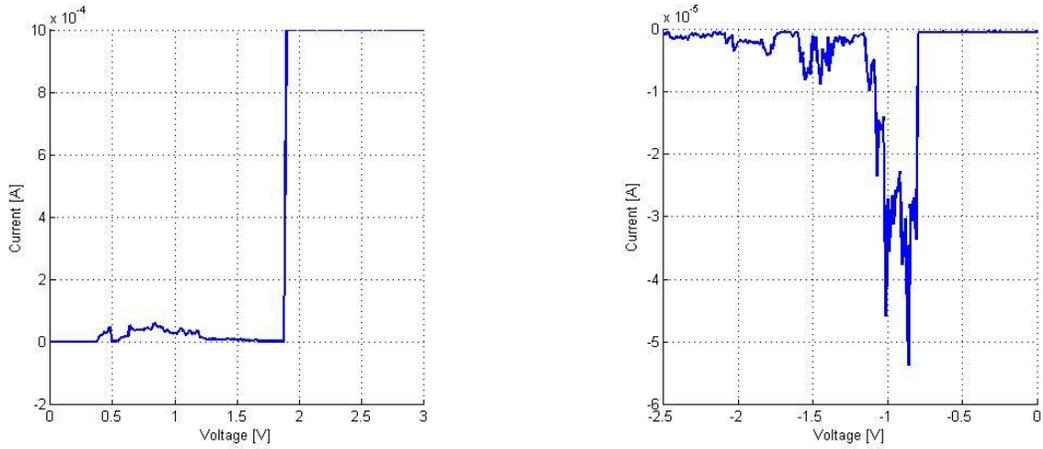


Figure 44: Set 6 and Reset 6

After one volatile cycle the device goes back to normal non volatile switching, i.e. Figure 45 onwards, for few more switching cycles.

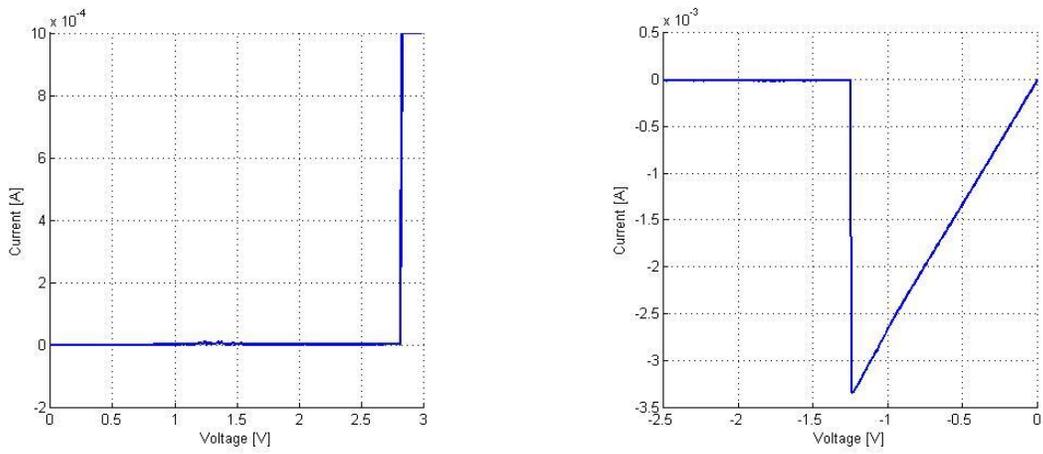


Figure 45: Set 7 and Reset 7

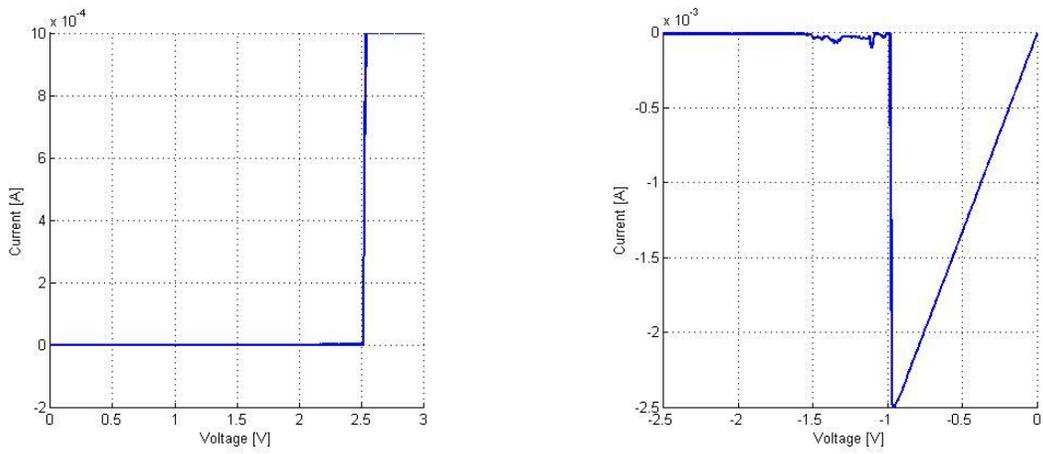


Figure 46: Set 8 and Reset 8

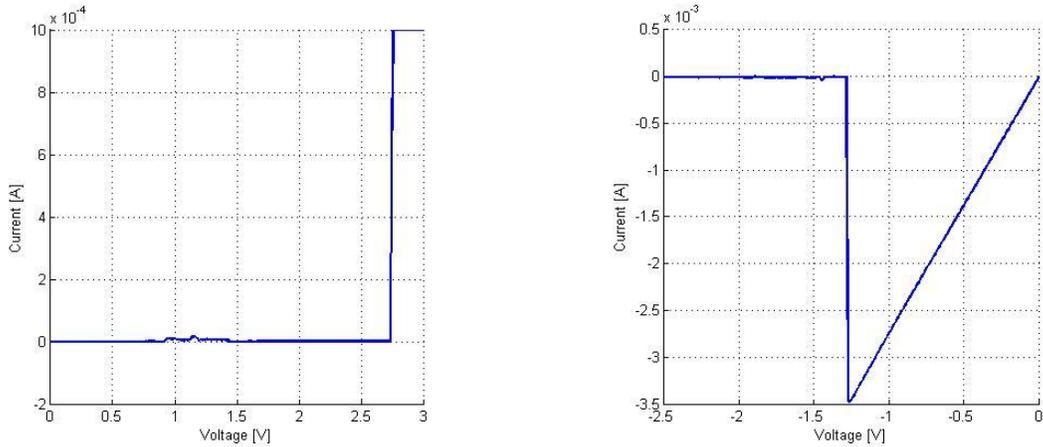


Figure 47: Set 9 and Reset 9

After a certain number of cycles of SETs and RESETs (about 10 -15 cycles), these devices start to RESET immediately after being SET, and then undergo a SET again, all occurring during the same positive sweep and within a very small voltage range. It is found that when this cell is swept at a compliance current of 1 mA from 0 V to 4 V, it undergoes a SET operation at about 1 V, stays in the SET state for 0.3 V further positive sweep and underwent a RESET operation at around 1.3 V and then it again undergoes a SET operation at 1.5 V, with all of this occurring during the course of the same positive sweep from 0 V to 4 V. One hypothesis behind this occurrence of this phenomenon also referred to as pulsing in the following sections, might be the presence of several incomplete bridges of almost equal strength (same width) yet different height (in different CF growth stage) competing with each other to get completed.

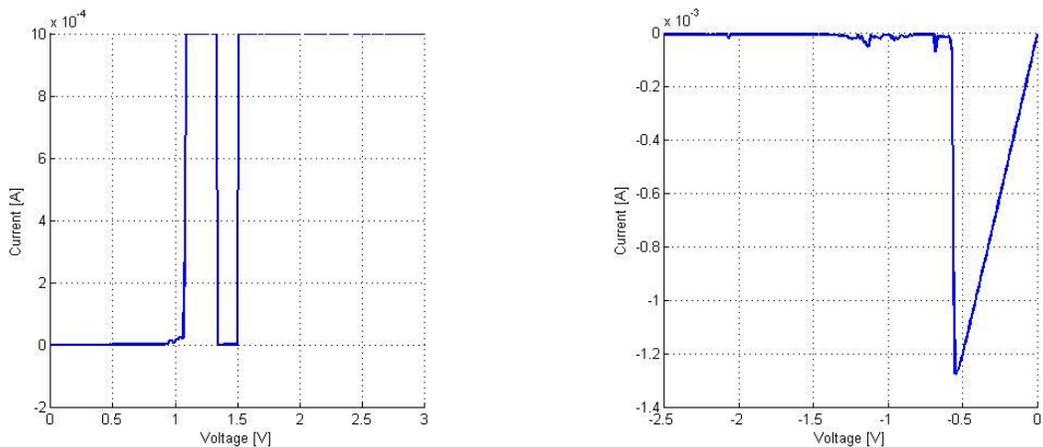


Figure 48: Set 10 and Reset 10, positive sweep shows pulsing i.e. quick rupture after set and then sets again.

It is believed that there are different stages of the CF growth i.e. vertical growth (to establish connection), lateral growth to strengthen the CF [16]. As a result while trying to SET, the CF

which has the greatest height among all the other incomplete bridges experiences strongest electrical field at its tip and as a result it is the one which gets connected first due to this electrical field. Once this bridge is completed, in the conventional devices the next step should be the lateral growth which leads to the strengthening of the bridge typically, however since in these structures the source of Cu ions is itself limited so these devices do not have enough material (Cu ions) to actually bring about lateral growth and as a result is unable to strengthen itself and dissolves due to even slightly elevated temperatures caused by Joule's heating. This also drives the Cu ions from the dissolved CF to move to other disconnected bridges. Now the incomplete bridge that has the maximum height starts experiencing the electric field at its tip which forces it to complete and hence that CF completes leading the cell again into the SET state. We can conclude that the strength of these competing CF bridges is almost the same as the slope of the graphs or the average resistance of the different bridges for the successive cycles was found to be almost comparable i.e. 357,367,384,400, 387, 382,367, 400, 357, 416 Ω .

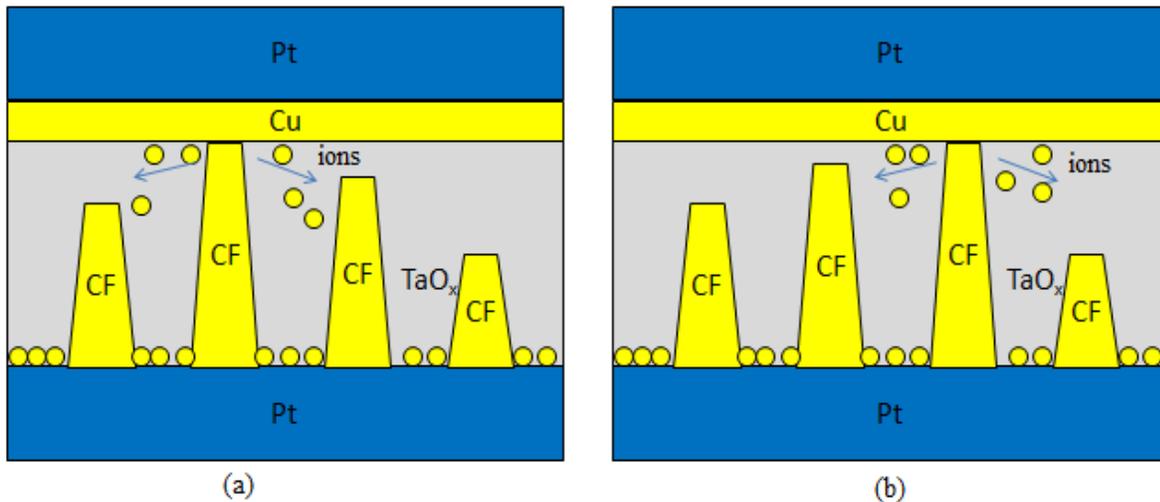


Figure 49: Conceptual view Cu ion diffusion and filament formation (a) Middle CF completes the conductive path, third CF is the next highest incomplete CF (b) Middle CF unable to strengthen itself and ruptures, third CF completes the conductive path

5.1.2 DC Sweep without Compliance Current

After the cell starts behaving like pulsing circuit (undergoing quick SETs and RESETs) in the positive domain as shown in Figure 46, the compliance current limitation was removed for further positive sweeps. Based on the hypothesis that the device tries to achieve a state of symmetry, it should be able to SET and RESET in both the domains and therefore CC is

removed from positive sweep since no CC limit is used for negative sweeps (0.1 A). From Figure 50, it is observed that the current keeps on increasing once the compliance current limitation was removed, and at a certain voltage of the same polarity, with a slightly higher magnitude, the cell undergoes RESET.

When the cell was swept in the negative regime it undergoes SET at -1.1 V as shown in Figure 51. Figure 51 also indicates multiple bridge formation since current jumps twice before becoming constant. Moreover since the SET operation occurred during the negative sweep, it denotes the existence of multiple complete Cu CFs with their base on the top Pt electrode and tip at bottom Pt electrode (indicating that the Cu ion diffusion from thin Cu- layer on the side of top Pt electrode and its subsequent precipitation on the bottom Pt electrode has become significant so that layer of Cu atoms near bottom Pt electrode now act as the source). However it was also discovered that even after removing the CC limitation, the bridges do not rupture in further negative sweep (up to -5 V).

One might argue that this is an [O] vacancy bridge but the range of SET voltages (in the negative regime) for [O] vacancy bridge based switching has been found to be in the range of -3 V to -7 V [11] and -1.1 V is much lower than that. Thus it is safe to say that it is indeed a Cu bridge which was established due to the Cu ions originating from the layer of Cu atoms close to bottom Pt electrode. This layer of Cu atoms on the side of bottom Pt electrode comes into existence due to significant diffusion of the Cu from the initially deposited Cu δ - layer. This observation implies that, indeed the Cu atoms try to get distributed equally on both sides of the electrolyte layer and the device tries to achieve symmetry. It might be safe to say that this observation gives boost to the hypothesis of symmetry achievement by the device.

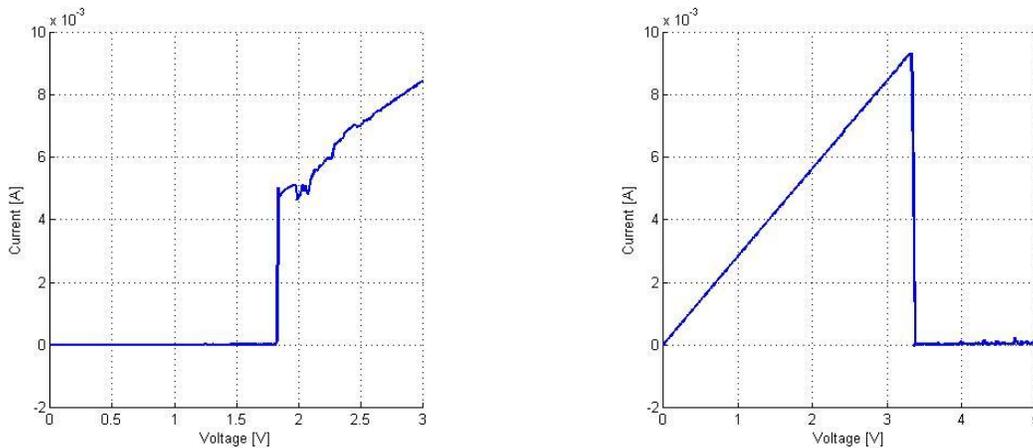


Figure 50: Set and Rupture in the positive sweep after removal of compliance current

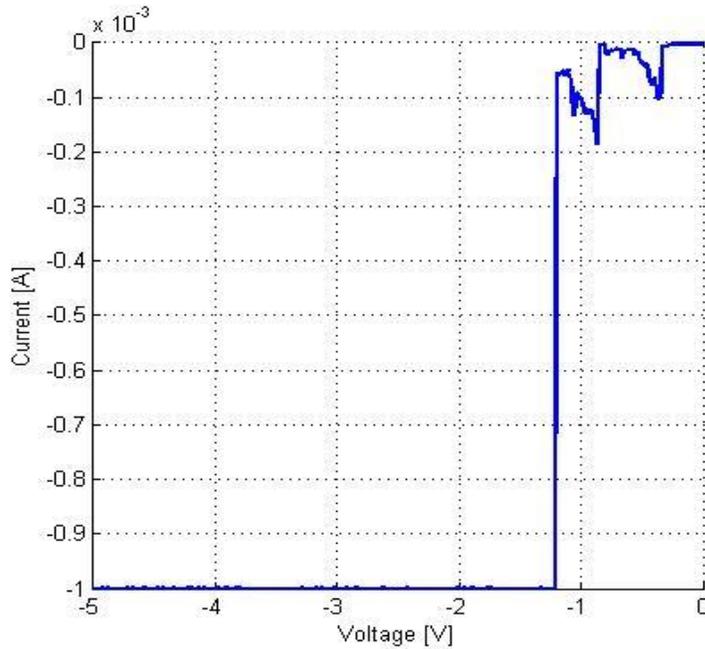


Figure 51: Set in the negative regime indicates the formation of at least two conductive filaments, one bridge forms but ruptures quickly after it and then two subsequent current jumps (one small and one large jump) are observed.

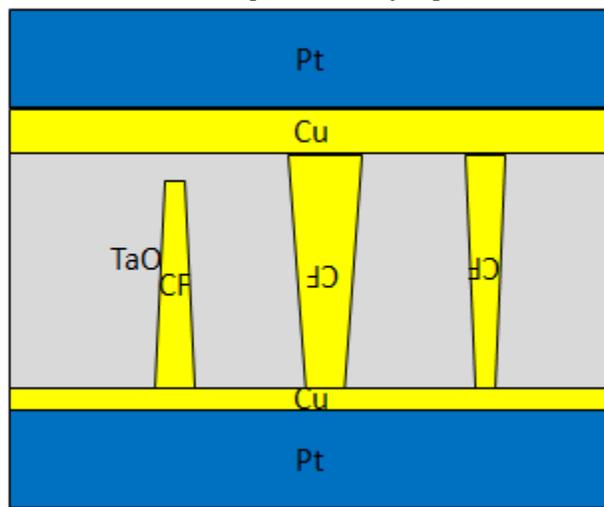


Figure 52: Conceptual view of filament formation (one strong CF and other slightly weak CF) based on the set in the negative regime in Figure 40, the first incomplete CF denotes the CF that was formed and ruptured during the previous positive sweep as shown in Figure 48.

5.1.3 Multiple bridges from both sides

The most interesting observation in the characterization of limited source devices was the formation of multiple filaments in the electrolyte, with the layers of Cu atoms on both sides of the electrolyte acting as source. One such I-V characteristic of multiple bridge formation and rupture is given in Figure 53 which is a continuation of characterization from Figure 51. There is

distinct evidence of at least two bridges if not more, one of the bridges already exists right from beginning of positive sweep, however there is another bridge which SETs itself at about 3 V, causing a sudden jump in the current and then RESETs back at 4 V. Among the two bridges, the first formed one is the one with its broader base at the top Pt and tip at the bottom Pt electrode (since it was SET in negative sweep i.e. Figure 51) and the second newly formed one is a weak bridge which has its broad base at the bottom Pt electrode and tip at the top Pt electrode.

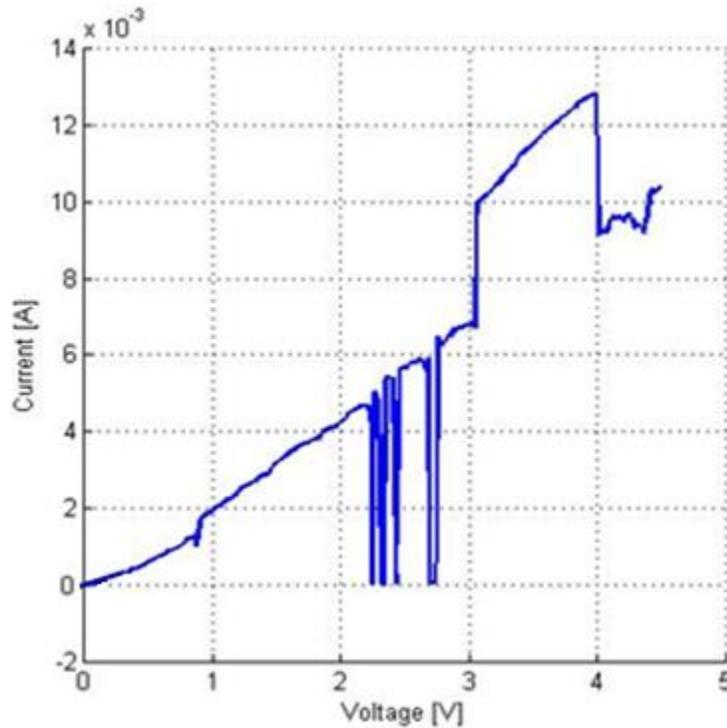


Figure 53: Positive sweep shows the formation and rupture of second filament in the unipolar mode while the first filament formed during negative sweep remains in place.

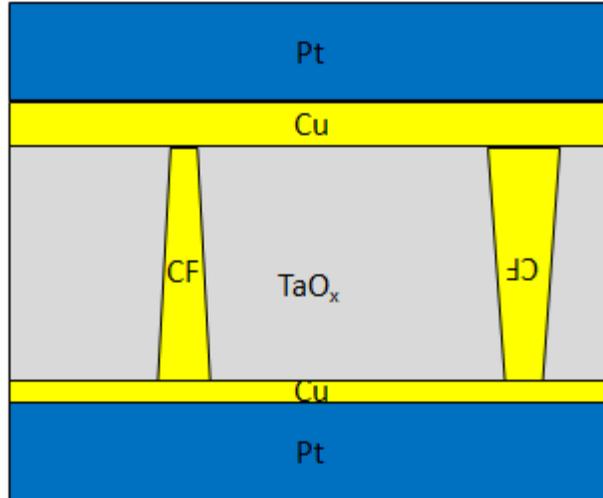


Figure 54: Conceptual view of the CF formation based on the I-V characteristics in Figure 51. Left CF is formed in the positive sweep and Right CF is formed in previous negative sweep.

5.1.4 Multiple bridges from same side

The phenomenon of multiple bridge formation from the same side of the switch structure (all bridges have the same source of Cu ions) was also observed in further characterization. It was also found that the bridge that forms second is the first to rupture. However it is almost impossible to rupture the first bridge despite multiple sweeps in both the positive and negative directions and this bridge is almost permanent. In Figure 55, the voltage is swept from 0 V to 7 V with a sweep rate of 0.005 V/step. Small sweep rate is used to resolve the multiple bridge formation and rupture. It can be seen that there were already multiple bridges and at $V_{\text{RESET2P}} = 1.9$ V, one of the bridges ruptures (sudden current drop followed by ohmic current behavior) and then it SETs itself again at $V_{\text{SET2P}} = 2.7$ V (current jump followed by ohmic behavior) and it was found that the slope/resistance before the rupture and after the subsequent re-establishment is the same. The slope of the 1st portion of the Figure 55 (before the second bridge is re-established) is 400 Ω and after the bridge is re-established the slope of the 2nd portion of the graph is 300 Ω , so it can be said that the resistance of the conductive path goes down considerably after the establishment of the second bridge.

For the Figure 56, it was observed that at $V_{\text{SET2N}} = -2$ V one more bridge SETs and again at $V_{\text{RESET2N}} = -2.7$ V, this bridge ruptures. The slope of the 1st portion of the graph when only one bridge was in place is $R_{\text{ON1}} = 400$ Ω and the slope of the 2nd portion of the graph when both the

bridges co-exist, the slope is $R_{ON\ eq} = 318\ \Omega$. Comparing it with the data from Figure 55, it can be concluded that the equivalent resistance when both the bridges exist is $300\ \Omega$ and when only one bridge exists is $400\ \Omega$. From the formula of parallel resistance, the resistance of the ruptured bridge is found to be $R_{ON2} = 300 \times 400 / (400 - 300) = 1200\ \Omega$. Thus this bridge is much weaker as compared to the first bridge. It is safe to conclude that both of these bridges are established in the negative regime (possible conceptual view can be described by Figure 57) and most importantly the second bridge is capable of operating in the unipolar mode. Not much can be deducted about the first bridge though, since it could not be ruptured despite numerous attempts.

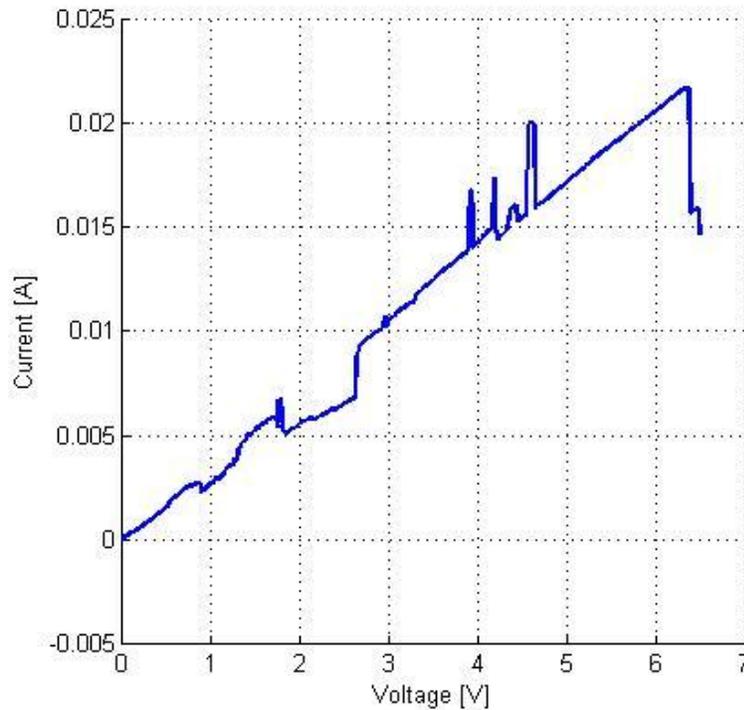


Figure 55: Positive sweep breaks one of the bridges established in negative sweep and after some time the bridge re-establishes itself.

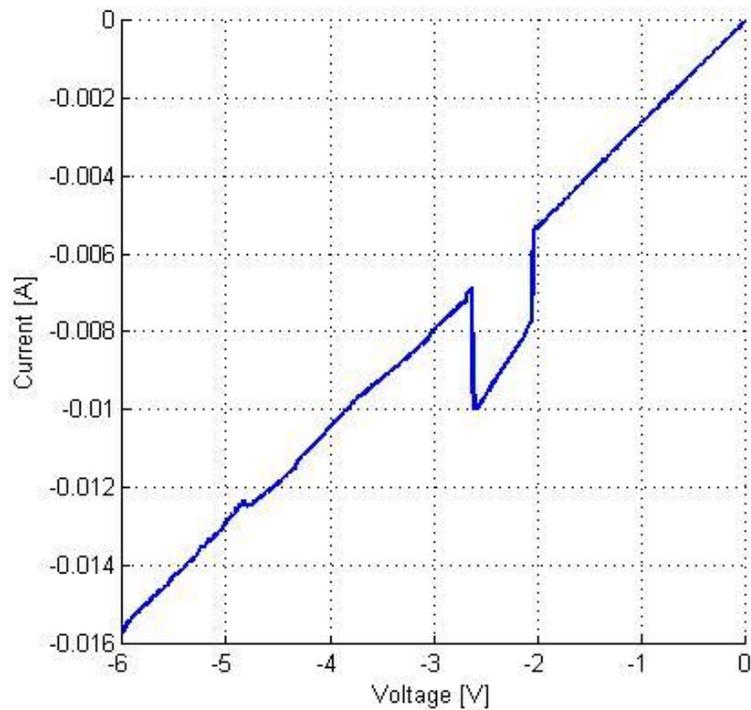


Figure 56: Negative sweep shows the formation of a second bridge and its subsequent rupture.

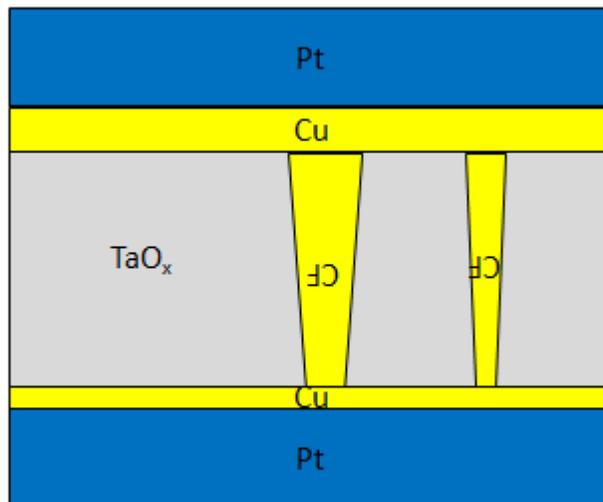


Figure 57: Conceptual view of multiple bridges from the same side with the layer of Cu atoms on the bottom Pt electrode acting as the source.

5.1.5 Observations and Conclusion:

It is possible to establish multiple incomplete filaments inside the cell at the same time if the Cu ion source is limited and each of these filaments compete with each other to complete the conductive path from the cathode to the anode. Again as the Cu ions starts getting diffused and redistributed to the both sides of the electrolyte in the form of equally thick layer of Cu atoms,

there are multiple filaments established in the electrolyte at the same time, one filament with a broader base at the bottom Pt electrode and the other filament with a broader base at the top Pt electrode indicating the symmetry achievement by the device. It is also observed that it is most difficult to break the filament that has been established first. Generally the filaments which are established later are also ruptured before the first one. In none of the cases so far, it was possible to rupture the filament that was formed the earliest. The reason that the CF formed second is always ruptured first is related to the detailed structure of the CF. The tip of the CF cone formed second is less exposed to the current and is more fragile than the tip of the Cu CF formed first and hence it ruptures first [29].

Also it is easier to observe multiple filaments mode operation in limited source devices if compliance current limitation is removed. This is one major reason why, before the removal of compliance current, there is only CF among multiple incomplete CFs which gets completed as shown in Figure 49. After removing the compliance current, multiple complete CFs can be established simultaneously which is quite understandable since increasing or removing the compliance current, would lead to creation of a much stronger bridge which can sustain much higher Joule's heat. Figure 58 is conceptual view of the order in which the filaments are formed and ruptured based on the above DC characterization. In the end one of the bridges turns out to be permanent and remains un-ruptured.

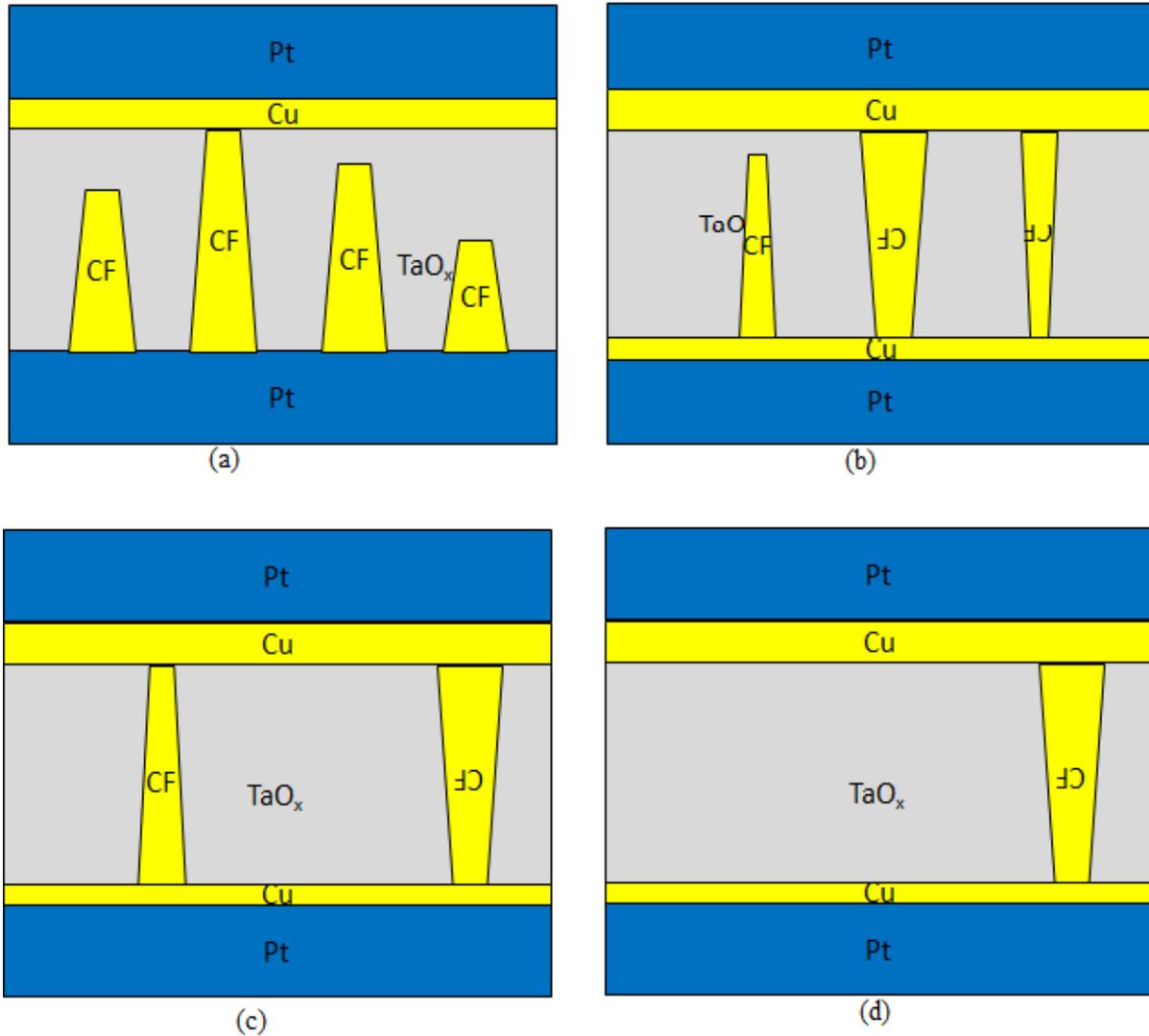


Figure 58: Conceptual view of order of formation and rupture of Cu CF in the limited source structure caused by the redistribution of Cu atoms in the electrolyte as understood from I-V characteristics.

5.2 6 nm Limited source device

Although these devices operate at lower compliance currents (10 μA) the DC characteristics are very noisy and unpredictable, so slightly higher compliance currents (100 μA) were used.

5.2.1 DC Sweep with compliance current

The DC characterization of devices with 6nm thick layer of Cu was performed with a Compliance Current of 100 μA and a sweep rate of 0.005V/step for the SET characteristics and a compliance current of 0.1 A with 0.01V/step for RESET characteristics. One unique feature of

all these graphs is a RESET with a slope rather than a straight line sharp reset. Instead of a sharp drop in current, the current seems to decrease linearly then it finally becomes 0 showing the absence of any conductive path between the two electrodes. One explanation might be that there are multiple filaments in the electrolyte and these filaments break in quick succession incapable of being resolved in the characterization set up and what appears as a triangle might be several small drops in the current, happening within very small intervals. It was also observed that these devices start to show the pulsing behavior first mentioned in the section on 12 nm devices very soon, after just about 2-3 cycles which is quite consistent since in these devices there is less Cu atoms available for diffusion and redistribution. Also evidence of volatile switching is also found in these devices.

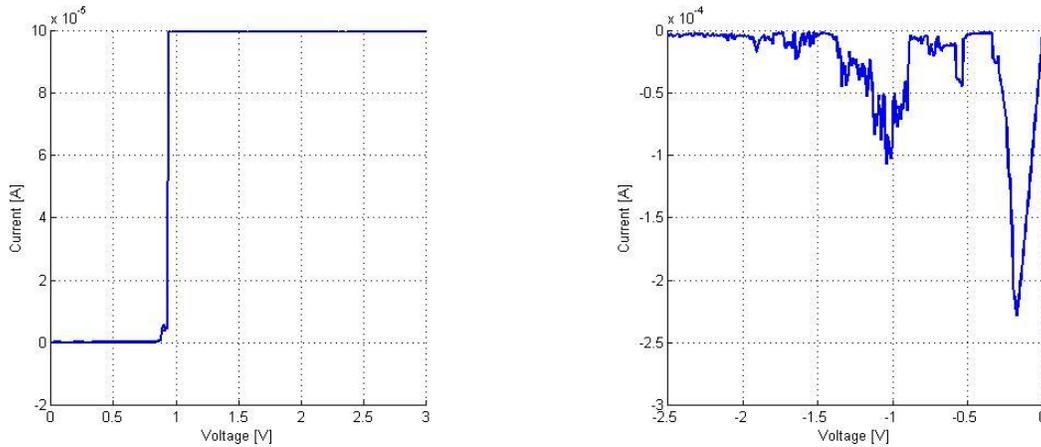


Figure 59: Form and Reset

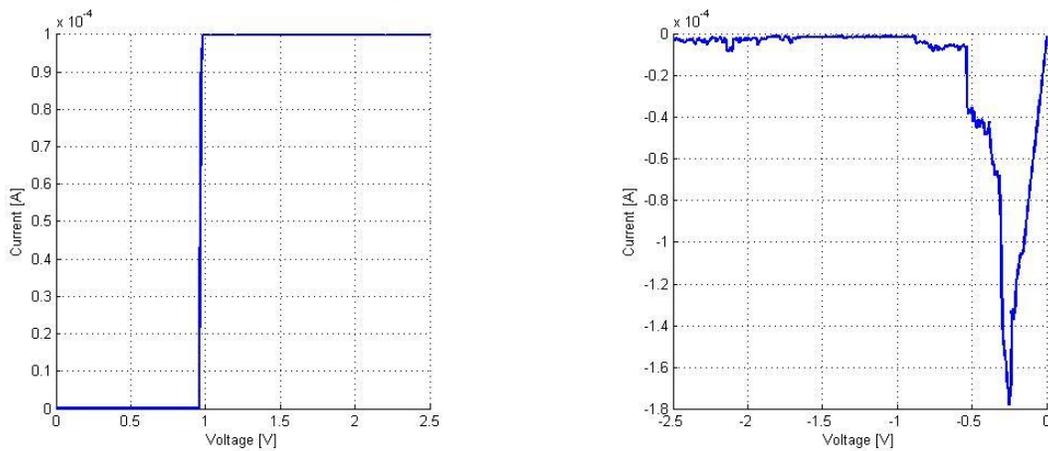


Figure 60: Set 1 and Reset 1

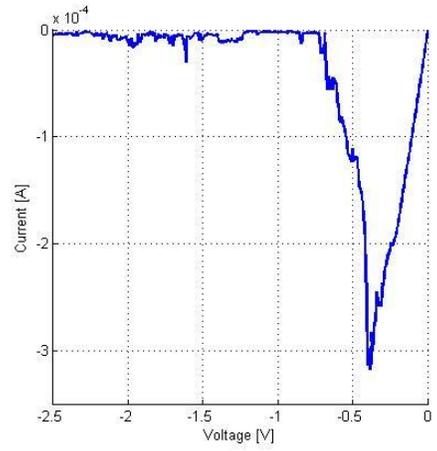
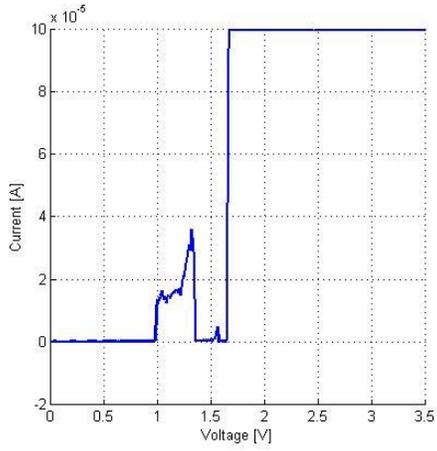


Figure 61: Set 2 and Reset 2

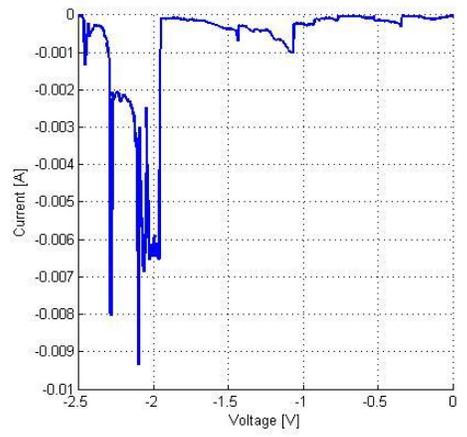
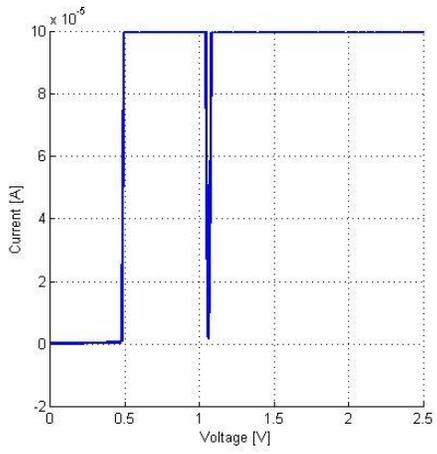


Figure 62: Set 3 and Reset 3

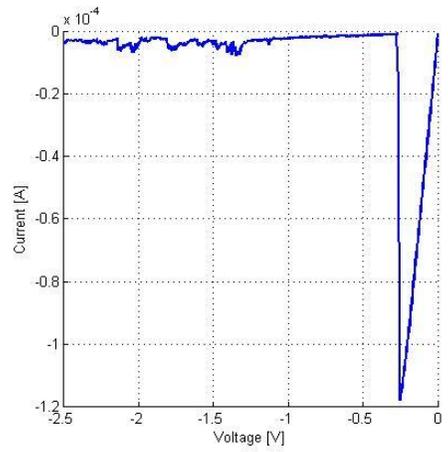
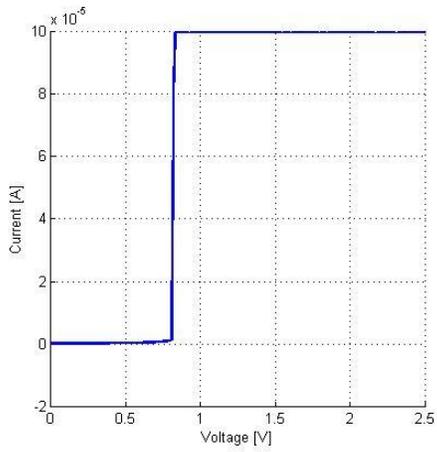


Figure 63: Set 4 and Reset 4

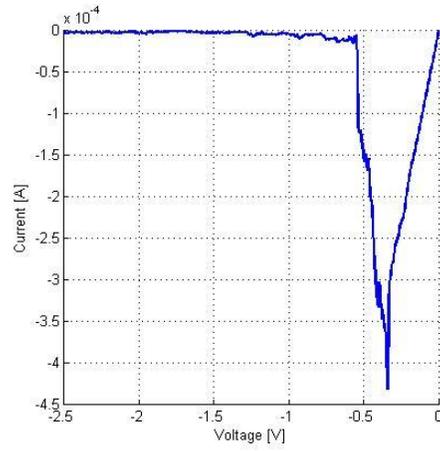
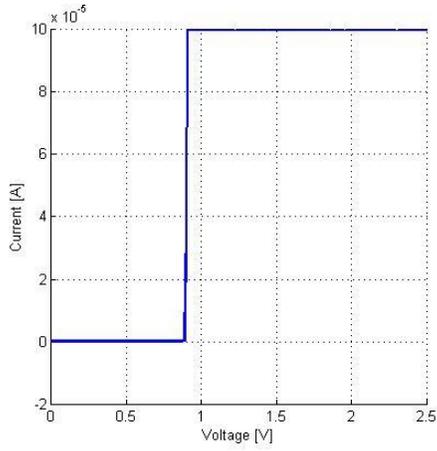


Figure 64 Set 5 and Reset 5

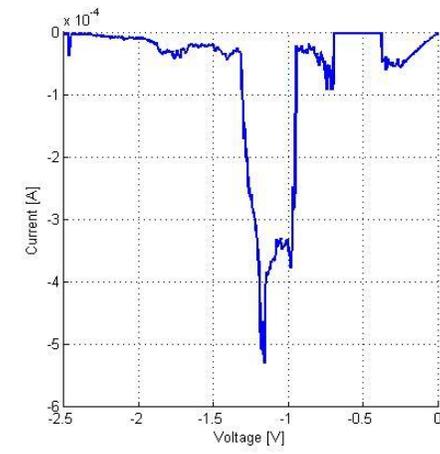
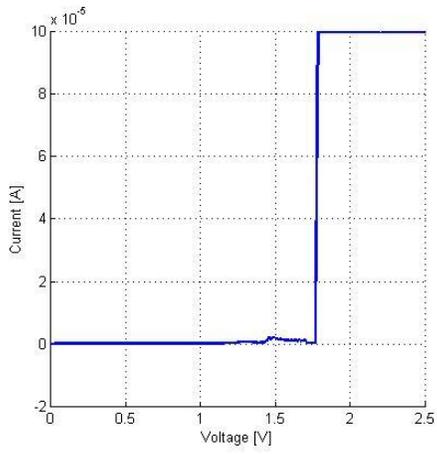


Figure 65 Set 6 and Reset 6

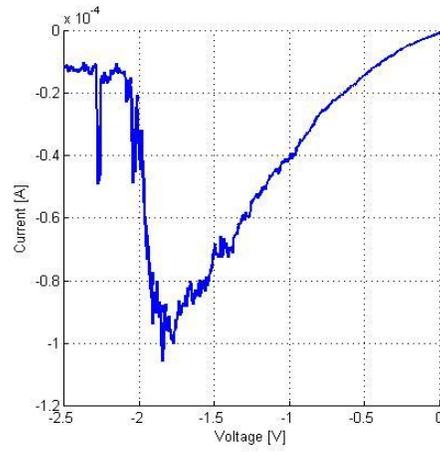
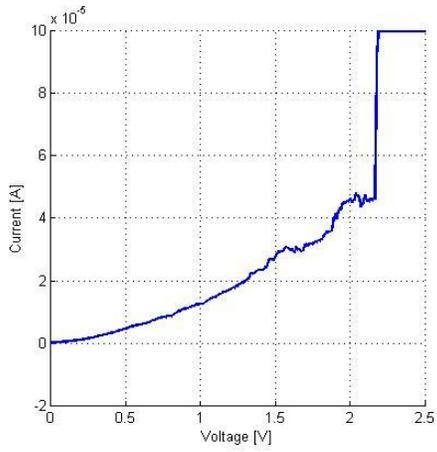


Figure 66: Set 7 and Reset 7

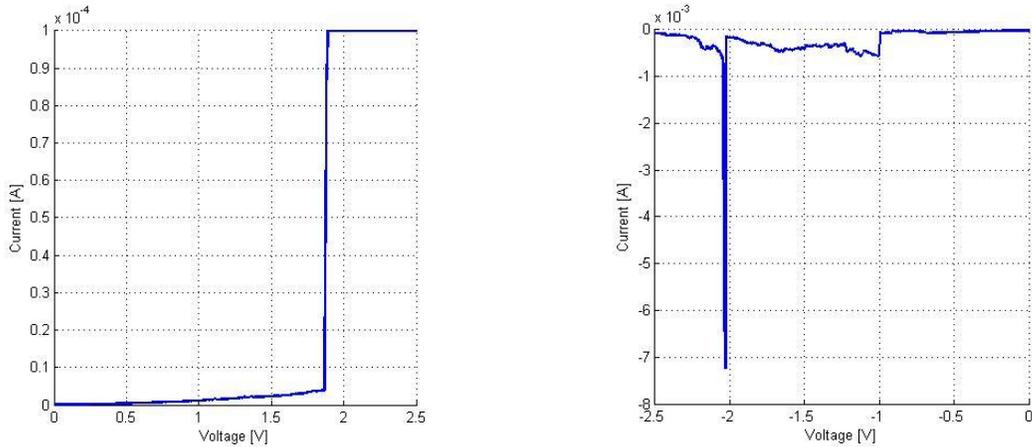


Figure 67: Set 8 and Reset 8, however the bridge turns out to be volatile.

5.2.2 Evidence of Multiple Bridges

For 6 nm limited Cu source devices, it was observed that when the sweep rate was kept at 0.001 V/step and compliance current of 1 mA was used and a DC sweep from 0 to 5 V was performed for one such cell, it was observed that the device SETs very gradually by the means of several small current jumps and in the RESET characteristics also, the current does not drop abruptly. The current seems to drop in several small steps as shown in Figure 69 (at least 3 for this particular cell) clearly indicating the presence and rupture of multiple filaments. Thus the lower sweep rate resolves the I-V characteristics and reveals that, what looks like a linear decrease of current in Figures 59 and 60 is actually a stepwise current drop.

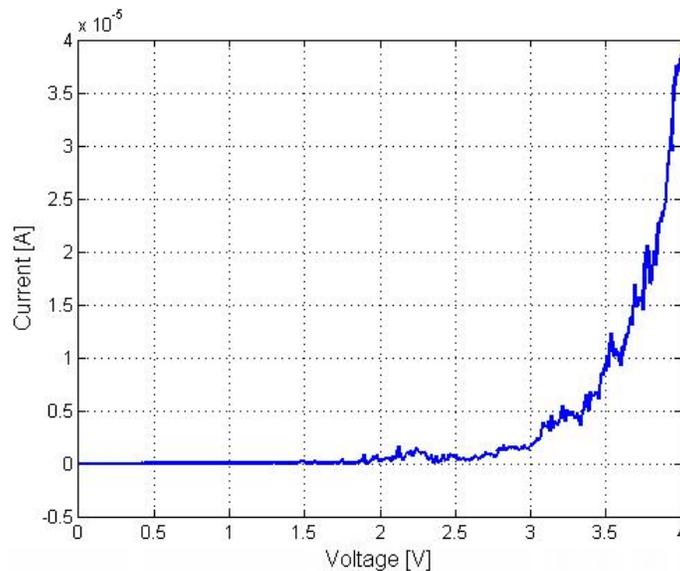


Figure 68: Form

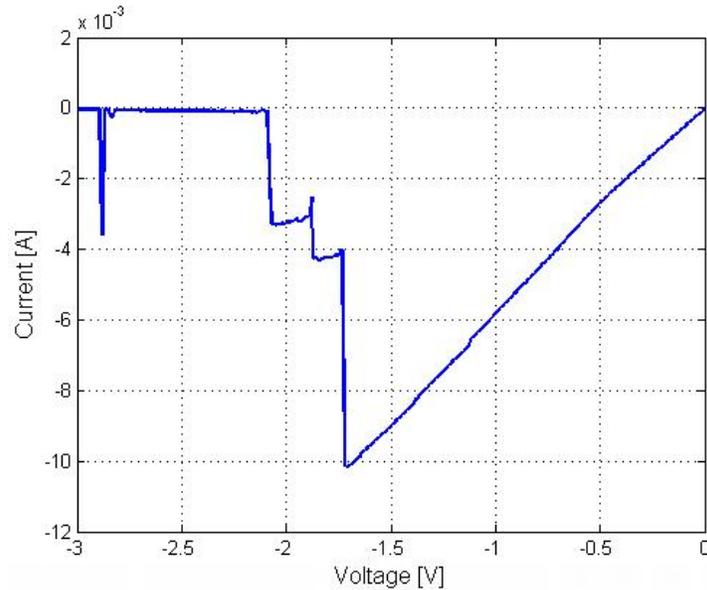


Figure 69: Reset clearly indicates the rupture of three bridges.

5.3 Multi-bit operation

Multiple filaments that can be formed and ruptured successively aid in multi level operation of the resistive switching cell and would be advantageous for a multi-bit nonvolatile memory storage cell. On the basis of the current work, it can be concluded that that limiting the source of Cu ions and operating the device at higher compliance currents are two factors which aid in the formation of multiple filaments as observed by the ease of establishing the multiple filaments in a limited source device as compared to the simple resistive switch.

5.4 ON resistance Hypothesis and Results

According to this hypothesis, the R_{ON} values for 6nm Cu limited source devices should be much higher than the R_{ON} values for the 12nm Cu limited source devices. The reasoning behind this thinking being, that for a 6nm limited source device even though there is just enough supply of Cu atoms to form a bridge, yet they are not sufficient to form a strong bridge even if the highest allowable compliance current of 1 mA is used.(The higher the compliance current, the stronger the bridge is). In both the cases there is limited supply of active ions and as a result lateral growth of the filament is limited. However in case of 6 nm limited source device, there is much less Cu and as a result it undergoes much lesser lateral growth and hence has a higher resistance.

Keeping this in mind, the R_{ON} was measured for several cells on both the devices. Again it is well known that R_{ON} is independent of the size of the cells [18]. It is to be noted that the comparison has been made on the same sized cells for both the devices to take into account any undesired effect of scaling of cell sizes on the observations.

Device	R_{ON} 6nm Cu device (Ω)	R_{ON} 12nm Cu device(Ω)
Cell 1	185	128
Cell 2	490	196
Cell 3	353	150
Cell 4	270	312
Cell 5	242	253
Cell 6	247	395
Cell 7	636	264
Cell 8	448	314
Cell 9	964	286
Cell 10	800	818
Cell 11	963	949
Cell 12	434	923

Table 1: Comparison of R_{ON} for 6 nm and 12 nm limited source devices.

The general trend of the data supports the proposed hypothesis apart from some exceptions which might have been as a result of slight process variations since the two devices were fabricated separately. But looking at the data it is safe to conclude that the lowest R_{ON} measured for a 12 nm limited source device is still lower than the lowest R_{ON} measured for a 6 nm limited source device. Hence the hypothesis can be safely assumed to have tested true.

5.5 Comparison between 6 nm and 12 nm devices

Since there is lesser source material (Cu atoms) available for establishing a bridge in a 6nm limited source device, it starts showing pulsing behavior, described in the above sections, after only 2-3 cycles of SETs and RESETs whereas the 12nm limited source device has to be at least

taken to 10-12 cycles of SETs and RESETs in order for it to be able to display the pulsing behavior (multiple incomplete filaments competing with each other to get completed). The lesser the Cu atoms are, the lesser switching cycles it takes for them to redistribute themselves symmetrically on both sides of the electrolyte. However it was not possible to establish the hypothesis of symmetry achievement in case of 6nm limited Cu source devices from the available data, perhaps owing to the extremely limited availability of Cu atoms in them.

Chapter 6: Additional Work

6.1 Effect of scaling electrolyte thickness

In an attempt to understand the effect of scaling of the dielectric (TaO_x) thickness on the overall device characteristics, three devices each with a different thickness of the solid dielectric i.e. 32 nm, 16 nm and 8 nm were fabricated. The motivation behind this experiment was to prove that apart from showing the expected scaling in the forming voltages as the dielectric thickness is scaled [1], there should not be any significant change in the I-V characteristics of the devices. All three devices were characterized under identical conditions i.e. the same compliance current (1 mA), the same sweep rate (0.01V/step) and the same range of voltage sweep (0 V to 5 V). It was observed that the average forming voltage for the cells with a 32 nm dielectric thickness was 4.3 V while the average forming voltage for 16 nm devices was around 2.2 V to 2.3 V and for the cells with 8 nm thick dielectric layer, the average forming voltage was 1.4 V. Also for cells with 8 nm thick TaO_x layer, the forming and SET voltages are approximately the same.

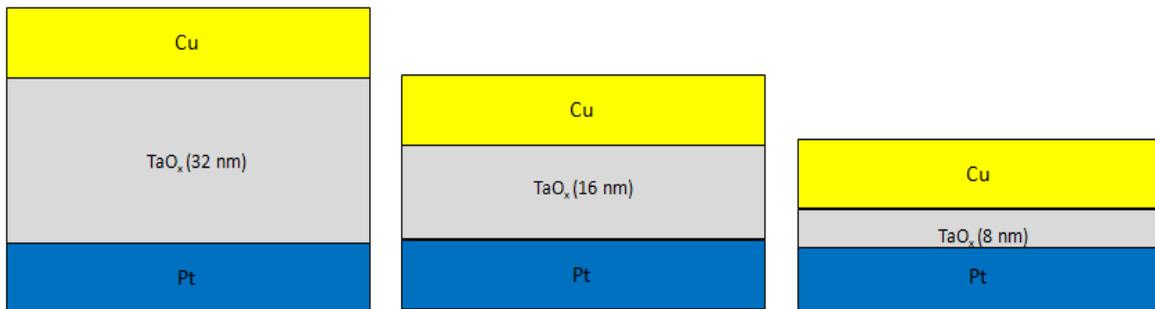


Figure 70: Resistive devices with varying electrolyte thickness

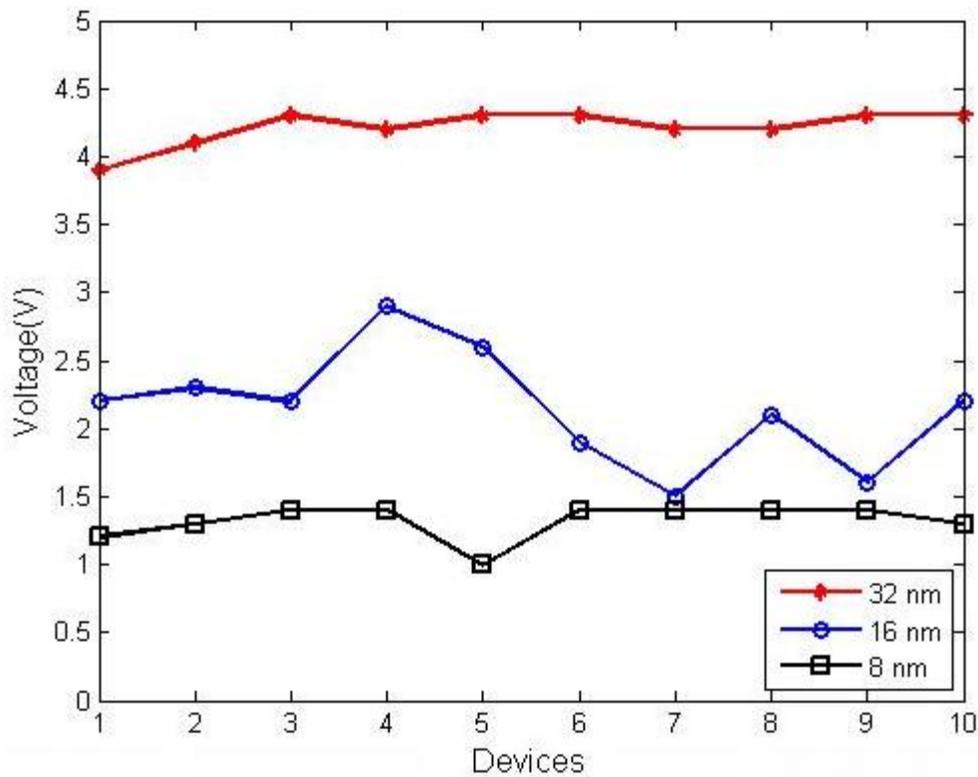


Figure 71: Plot of forming voltages for 10 cells from each of the three devices.

One very interesting phenomena was observed during the characterization of the 8 nm TaO_x devices. Most of the cells were found to be already PRESET and could not be reset. The term PRESET implies that these devices showed the evidence of existence of a conductive path even without the application of a voltage pulse and this conductive path could not be broken by the application of a voltage pulse either. However there were a few cells of size 10 μm X 10 μm which were capable of being formed or SET. It is to be noted that these cells are the smallest sized cells that can be characterized with the probe tips available for the characterization system. The average forming voltage for these devices was around 1.4 V. Again these cells could not be switched for more than 3-4 cycles on an average. After 2-3 cycles, most of these cells start showing a constant ohmic behavior which indicates the presence of a permanent conductive path between the electrodes. One possible explanation for this might be that when very thin layers of TaO_x are deposited using PVD, the film is not uniformly dense (since the oxide deposition by PVD is non planar) and might actually be porous so that the Cu atoms can diffuse through the gaps in the dielectric thereby creating a permanent bridge. The layer of Cu atoms deposited

using PVD is non conformal and as such the effect of forming voltage scaling with dielectric scaling can only be observed if the effective thickness of the dielectric is higher than a certain minimum thickness which ensures that there is no direct contact between the two electrodes.

Thus the forming voltage scales with the thickness of the dielectric only after some minimum thickness $V_{\text{form}} \sim (t_{\text{TaOx}} - t_{\text{min}})$. t_{min} is characterized by rough Cu surface and extrusions. This hypothesis can be checked by replacing PVD TaOx with much denser and uniform ALD TaOx. It is also seen that set voltages for $t_{\text{TaOx}} > t_{\text{min}}$ are not affected by t_{TaOx} .

6.2 Resistive Switching of Pt/TaOx/Pt device

As widely understood through literature, ideally a Pt/TaOx/Pt device being structurally symmetrical should behave as a unipolar switch [1]. However it was observed that even these symmetrically fabricated devices were capable of switching in the bipolar regime.

6.2.1 Negative Sweep First

If the negative sweep was performed first (negative bias provided to top Pt electrode and bottom Pt electrode kept grounded), these devices are able to SET immediately without even requiring a forming process. One such SET and RESET are shown in Figures 72 and 73.

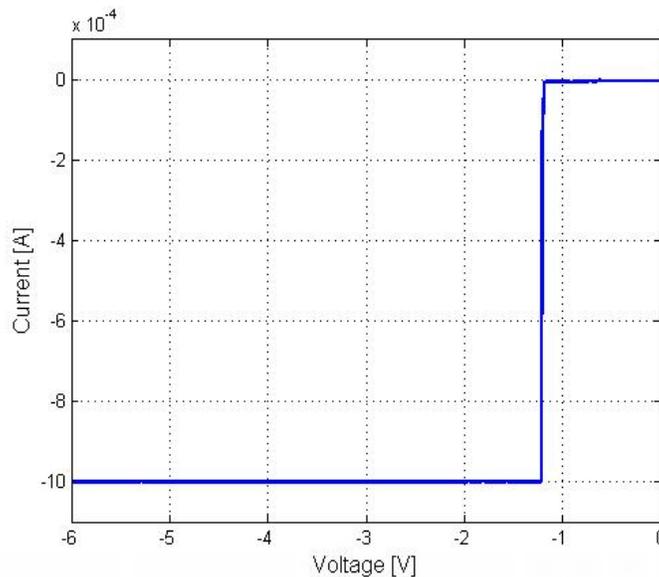


Figure 72: Set/Form

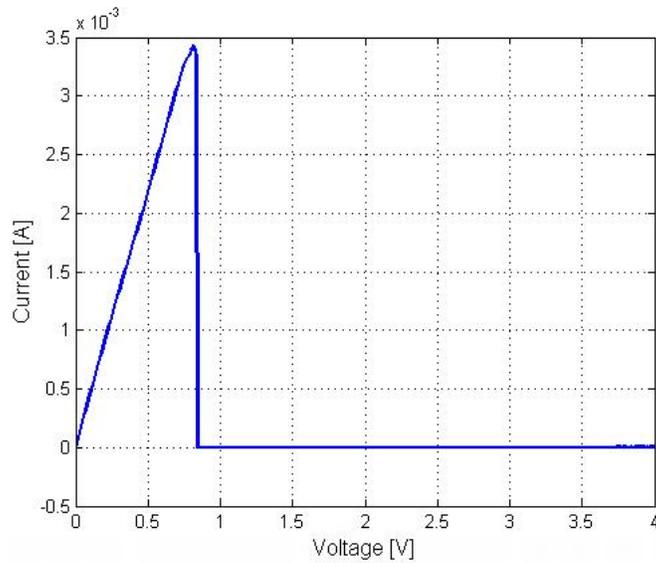


Figure 73: Reset

6.2.2 Positive Sweep First

If a positive sweep was used first (positive bias provided to the top Pt electrode and bottom Pt electrode kept grounded), the same devices needed a forming process which turns out to be volatile and after this forming process, these devices can be SET and RESET in the usual manner but with much higher SET (5 V, 8 V) and RESET voltages (-2 V, -5 V).

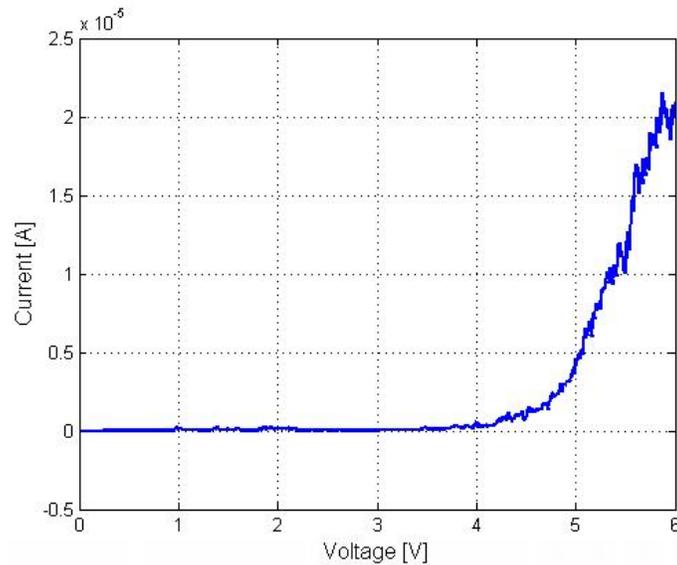


Figure 74: Form (volatile)

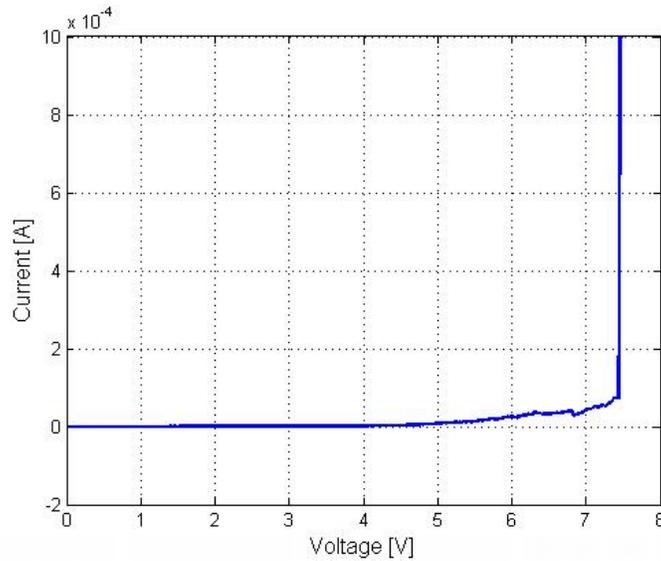


Figure 75: Set (Nonvolatile)

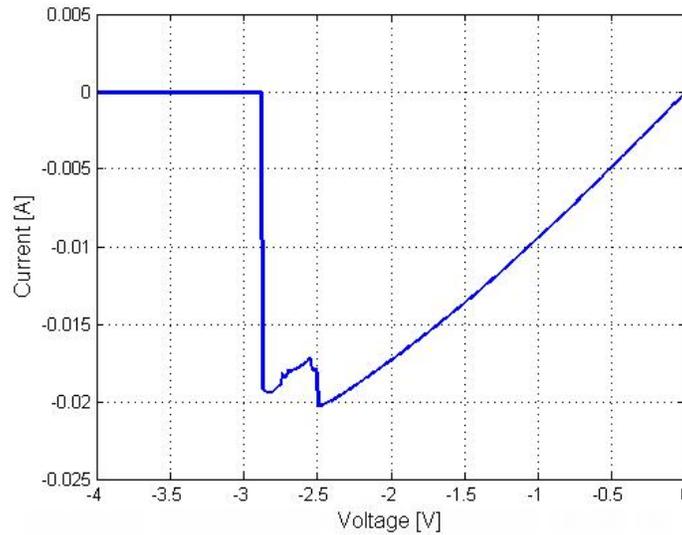


Figure 76: Reset

6.2.3 Conclusion:

Theoretically, all the Pt/TaOx/Pt devices should behave in a symmetrical manner (with same range of SET and RESET voltages) irrespective of whether a positive sweep or a negative sweep is performed first, since these devices are structurally symmetrical. However the actual results reveal that the devices are not actually symmetrical in terms of their DC characteristics. When a negative sweep is used, the devices are able to SET readily without a forming step however for a positive sweep, a forming process is needed. One very interesting feature is that this forming step is actually volatile and in order to establish a nonvolatile bridge, a second

positive sweep is needed. Thus based on polarity of the initial sweep, an asymmetry is established in the system which also makes it possible for the devices to operate in the bipolar mode. Further study is needed in this area to understand the exact mechanism which brings about this asymmetry.

The mechanism of operation of these devices is believed to be the formation and rupture of oxygen vacancy bridges since the bridge formation in these devices was observed at much higher voltages consistent with the oxygen vacancy bridge formation in Pt/TaO_x/Cu devices which are capable of operating in both the unipolar and bipolar regimes [22]. However from the data collected so far, it has not been possible to operate these devices in the unipolar mode in contrast to the reported behavior [22]. So further probing of these devices is needed to ensure if unipolar behavior can be observed since the absence of unipolar behavior could indicate that there is a totally different mechanism responsible for the formation of the bridge in the devices processed during the course of this research.

The Form and RESET graphs for these devices show a gradual increase or drop in current rather than a sudden abrupt jump. One possible hypothesis put forward to explain this phenomenon is that instead of a single conductive path, there are several possible conductive paths which are not completely independent of each other. The Figure 77 shows the conceptual view of two such conductive paths inside the dielectric, while path 2 is almost straight and has a lower resistance, path 1 curves throughout the thickness of the dielectric and has a much higher resistance. So at a certain instant the conductive path 2 breaks and conductive path 1 becomes complete, thus raising the resistance of the whole device while still keeping the device in the ON state.

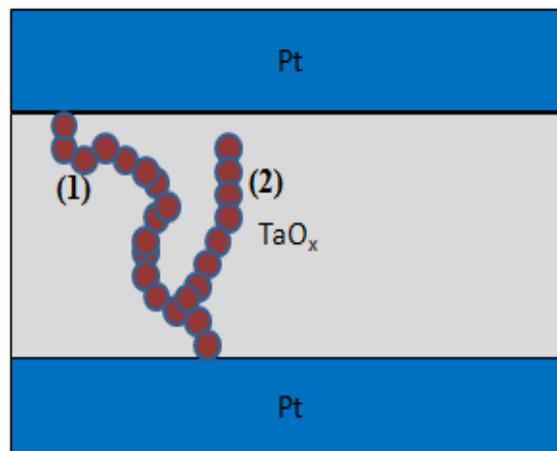


Figure 77: Conceptual view of conductive path inside a Pt/TaO_x/Pt device

Chapter 7: Conclusion and Future Work

During the course of this research work, various resistive switch devices were fabricated and characterized to understand how exactly is the formation of nanofilament affected by the various degrees of Cu diffusion stopping power of the inert Pt electrode. A Pt/ δ -Cu/TaO_x/Cu crossbar structure was fabricated to probe this. This device showed the novel phenomena of volatile resistive switching under low compliance currents and reliable nonvolatile switching under high compliance currents. The characterization of this device reveals that the introduction of the δ -layer of Cu affects greatly, the self diffusion flux of Cu in the CF through the interface between the Cu bridge and the Cu δ -layer on the Pt electrode, which is ideally null in the absence of the δ -Cu layer. In other words the introduction of the δ -layer upsets the balance between field supported Cu⁺ flux and the Cu self diffusion leading to the volatility of the filament.

Again to understand the diffusion of Cu ions and subsequent formation and rupture of conductive Cu filament, when the source of Cu ions is limited, devices with a Pt/ TaO_x/ δ -Cu /Pt structure were fabricated and characterized. The source of Cu ions in these devices is a very thin layer of Cu (12 nm and 6 nm respectively). The characterization of these devices revealed a very interesting feature. Through the diffusion of Cu ions in the electrolyte and the subsequent redistribution of Cu atoms on both sides of the electrolyte, these devices try to achieve symmetry in their I-V characteristics. In such structures, it was observed that the filament formation was possible from either side (with its broader base on either) of the Pt electrodes. These devices also show the evidence of multiple filaments simultaneously which is a very crucial feature that will help in the multilevel application of these switches. These devices also show volatile switching behavior along with the usual non volatile resistive switching.

Another experiment was performed to establish the scaling of forming voltages with the scaling of the dielectric thickness [1] and it was found that the forming voltages decreased with the electrolyte thickness as expected. However it was also discovered that if the dielectric is scaled beyond a certain thickness, the resistive cells turn out to be PRESET even without the application of a voltage pulse which might be attributed to the non conformal nature of the oxide film deposited using PVD.

7.1 Future work

As discussed above, multiple filament formation was observed in the resistive devices with a limited source of Cu ions when the compliance current limitation was removed. An in-depth understanding of the interplay between the thickness of the Cu layer which acts as the limited source and compliance current value limit, is needed, to bring about multiple filament formation in a controlled manner. The control of individual SET and RESET operations for each of these filaments may pave the way for a deployment of a multi-filament cell for multi-bit nonvolatile RAM and in order to achieve this, the rupture of the first formed CF is extremely important which has not been possible during the current work. While it was possible to SET and RESET the later formed CFs but the first formed unfortunately could not be ruptured. One way to achieve this might be to use a lower compliance current while forming the first bridge to keep it weak enough to allow it to rupture and then using a higher compliance current during the formation of the second CF to produce sufficient voltage drop across the electrolyte [29].

Another way to reduce the range of variation in the SET and RESET voltages in the consecutive switching cycles as well as to ensure the deposition of a planar layer of electrolyte would be the deposition of Ta₂O₅ using ALD rather than the deposition of TaO_x using PVD since it would ensure lesser defects in the electrolyte.

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