Design of a Battery Charger for the NASA EOS Space Platform

by

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(ABSTRACT)

A battery charger design for the NASA Earth Observing System (EOS) Space Platform has been developed and tested. This thesis discusses the design of the battery charger power stage and its current and voltage control loops. The charger was designed to minimize the mass and to maximize the efficiency. In addition to restoring energy to the batteries, this charger regulates the spacecraft bus voltage during the transition between eclipse and sunlight. The battery charger design and analysis was facilitated by use of the model for the pulse-width-modulated (PWM) switch and the new continuous-time model for current-mode control. Analyses of the battery charger small-signal behavior are compared to hardware measurements to verify modeling accuracy.

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1. Introduction

1.1 Overview

In order to understand global change and man's interaction with the environment, the U.S. Global Change Research Program has been established. NASA's contribution to this program is their Mission to Planet Earth, a system of low earth orbit spacecraft which will perform comprehensive global measurements. These space platforms, which are part of NASA's Earth Observing System (EOS), are to be launched starting in 1998. To facilitate the design of the actual spaceflight hardware, NASA Goddard Space Flight Center (GSFC) has funded the Virginia Power Electronics Center to design a prototype Space Platform power system. As for all spacecraft power systems, the battery charger is a fundamental system component. This thesis describes the design of the prototype Space Platform battery charger.

To fully understand the design of this battery charger, it is necessary to know how the Space Platform power system operates. A simplified block diagram of this direct energy transfer power system is shown in Fig. 1.1. The primary power source is the solar array which supplies the 12 KW needed by the payload and housekeeping loads on the spacecraft power distribution bus. Though represented as a single resistor, R_{BUS}, these bus loads are a collection of various types (constant current, constant power, etc.). To help stabilize the bus voltage against load transients, a large capacitor, C_{BUS}, is placed on

the bus. During the 64 minute sunlit portion of the spacecraft's 100 minute, 440 mile altitude polar orbit, the bus voltage is regulated at 120 VDC by a solar array shunt regulator. This sequential shunt regulator maintains fine control of the bus voltage by pulse-width modulating a single solar array string. During the sunlight period, the batteries are charged at a commanded rate until full capacity is obtained. This operating condition of the charger is referred to as the current regulation mode. The battery charging is terminated subject to the volt/temperature (V/T) control circuitry within the charger.

The battery and its charger are mated with a battery discharger to form an orbital replacement unit (ORU). The Space Platform has four battery ORU modules, all of which are operated in parallel in a manner that ensures equal power sharing. The entire spacecraft power system is modular to facilitate servicing and to provide a high degree of fault tolerance and redundancy.

During the 36 minute eclipse period, the spacecraft load is supplied from the batteries through the dischargers which regulate the bus voltage. When the spacecraft is in the transition between eclipse and sunlight, the charger regulates the bus voltage. This operating condition is subsequently referred to as the bus voltage regulation mode. Many spacecraft use the solar array shunt regulator to control the bus voltage during this transition period, but this alternate method is more efficient since the excess solar array current is used to charge the batteries instead of being shunted to ground. To control the shunt regulator, charger, and discharger during the various transitions, a central Power Control Unit (PCU) is employed. Therefore, the voltage delivered to the spacecraft loads is uninterrupted and well regulated under all possible operating conditions.

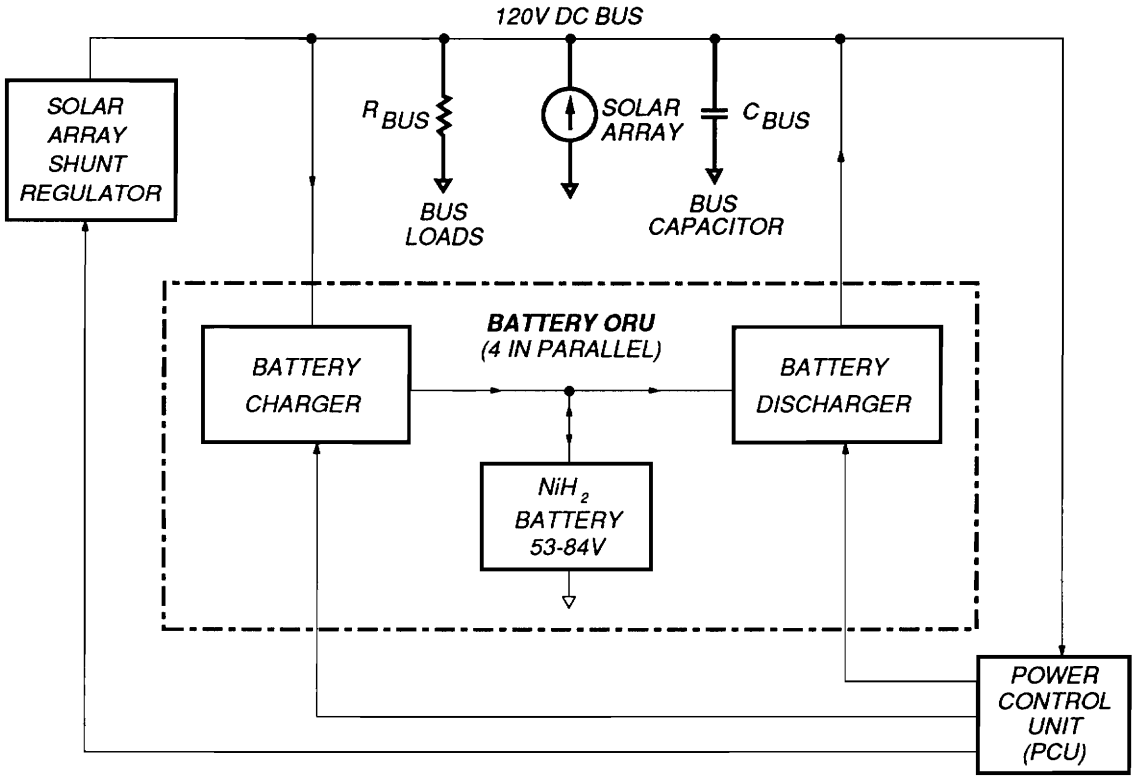


Fig. 1.1. Space Platform Power System

1.2 Design Specifications

Listed below are the battery charger design specifications:

Input Voltage = 120 VDC ±4%,

Output Voltage = 53 to 84 V,

Output Power = 1470 W Ave/1930 W Pk,

Nominal Efficiency = 96%,

Switching Frequency = 90 KHz,

Output Current = 0.85 A to 23 A dc

(in 16 equal steps of 1.5 A each),

Output Ripple Current = 0.23 A pk-to-pk,

Bus Ripple Voltage = 200 mV pk-to-pk, and

Bus Voltage Transient Settling Time < 10 mS.

Given the input and output voltage levels, a natural and effective switchmode topology for the battery charger is a buck converter. Though other suitable topologies exist for an application such as this, the buck converter was chosen for its simplicity and well documented behavior. Future efforts on this research project will evaluate alternative charger topologies. Therefore, a tradeoff analysis can later be performed to determine the benefits of each topology. Such an analysis has already been performed on the Space Platform battery discharger [1].

The spacecraft batteries have a 50 AH capacity and consist of 54 series nickel hydrogen cells. For a normal 30% depth of discharge (DOD), the battery voltage ranges

from 64 to 84 V. However, the charger is designed to operate with a 53 V battery, an abnormal condition occuring at 100% DOD with cell voltages falling to near 1 V. The batteries will be charged at 16 different commanded rates ranging from 0.85 A to 23 A, with 1.5 A increments between each charge rate. Rate 1 is 0.85 A which corresponds to C/60 where C is the battery ampere-hour capacity. Since rate 16 is 23 A, this corresponds to (50 AH)/(23 A)=C/2.2. As for most batteries, the current ripple must be kept to a minimum, so the charger's output current is attenuated to below 1% of the maximum charge rate (230 mA pk-to-pk). The charger is to have eight V/T curves to ensure adequate charging under all conditions of battery voltage, temperature, and life. For simplicity, three V/T curves are designed into the charger described in this thesis.

The charger is designed to maintain a nominal efficiency of 96% while delivering 1500 W to the battery. A 90 KHz switching frequency was chosen because of the stipulation that the charger and discharger frequencies must contain the same harmonics. Since the optimum power conversion frequency for the discharger was found to be 45 KHz, the 90 KHz frequency for the charger satisfies the harmonic requirement and produces a compact and lightweight charger design.

During the bus voltage regulation mode, the charger must produce less than 200 mV pk-to-pk of switching ripple across the 120 V bus. The charger must also keep bus voltage transients less than ±4.8 V, with a settling time less than 10 mS.

Designing a battery charger to meet the above specifications involves trading off mass, efficiency, and reliability. Increasing the efficiency of the charger produces a heavier design: reduction of ohmic and magnetic losses requires larger power circuit components. Similarly, designing a charger for minimum mass yields a converter with a

low efficiency. Therefore, a careful balance between these critical design parameters is required. To ensure high reliability, component selection and derating was guided by the GSFC Preferred Parts List (PPL-18).

1.3 Thesis Outline

The design of the battery charger power stage is presented in Chapter 2. Included in this chapter is the design of the input and output filters, the power switching semiconductors, and the power MOSFET gate drive circuit. The major design constraints in the power stage are mass and efficiency. While these are often conflicting parameters, the charger was designed in a manner to minimize mass while maintaining a high efficency. To increase the efficiency, four MOSFETs are placed in parallel to form the active power switch. A unique gate drive circuit is designed to simultaneously drive the four power MOSFETs. The charger output filter is designed with two stages so that the battery current ripple content is reduced to 1%. The main energy storage inductor in the output filter is designed using a Metglas core so that the mass can be minimized.

Chapter 3 presents the design of the charge current and V/T control circuits. This design work is facilitated by use of the model for the pulse-width-modulated (PWM) switch and the new continuous-time model for current-mode control. To improve performance, all charger control loops use current-mode control. The V/T control circuit has three V/T curves and is designed to be operated by digital command. The charge current regulation circuit is also designed to be commanded digitally since there are 16 battery charge rates. The charge current loop uses average current-mode control to ensure regulation of the dc current into the battery. The battery current is sensed by a

dual current transformer circuit which is designed to keep the current regulation error less than 1%. The duty cycle-to-inductor current transfer functions are presented for both CCM and DCM. These transfer functions are effectively single-order which allows for a straightforward feedback loop design. The design of the feedback loops is presented along with measured and predicted Bode plots so that modelling accuracy can be verified. Furthermore, the charge current loop stability is demonstrated by measurement of its transient response.

Chapter 4 discusses the design of the bus voltage regulation control circuitry. Due to the unique nature of this control scheme, several very interesting results are obtained. Current-mode control is implemented because of the need for current sharing between battery ORUs. The transfer functions for the inductor current and the bus voltage are presented for the continuous and discontinuous conduction modes (CCM and DCM). The closed-loop transfer functions are very complex since they are third order; however, simplified results are presented which allow intuitive design. The feedback loop design is discussed, and measured Bode plots are compared with predicted results obtained from PSpice models. The voltage loop performance is verified by examining the charger output impedance, transient response, and conducted emissions.

The conclusions drawn from the design of this battery charger are presented in Chapter 5.

2. Power Stage Design

2.1 Introduction

The design of the battery charger power stage is shown in Fig. 2.1. An input filter smooths the pulsating current drawn by the charger power stage. The bus voltage, V_{BUS}, is chopped by the MOSFETs at the switching frequency, f_S. This PWM voltage is smoothed by the charger's two stage output filter. The power stage is carefully designed so that mass and losses are minimized. The main energy storage inductor is designed with a Metglas core to reduce mass. The MOSFET gate drive circuit is designed to simultaneously drive all devices in parallel.

2.2 Power Switching

2.2.1 Power MOSFETs

Since the power MOSFETs must be capable of withstanding a V_{DS} stress of 120 V, a 200 V component must be selected. The best choice for a 200 V MOSFET from the NASA Preferred Parts List is the IRF250. These MOSFETs have a continuous I_D rating

of 19 A (at a case temperature=100°C). Though the I_D waveform is trapezoidal as shown in Fig. 2.2, it can accurately be approximated by a squarewave. Under this approximation, the maximum RMS drain current is

$$I_{Drms\max} = I_{BAT\max}\sqrt{D_{\max}} = (23A)\sqrt{\frac{84V}{120V}} = 19.2\,A,$$

occurring at V_{BAT}=84 V, where the maximum duty cycle is $D=V_{BAT}/V_{BUS}=0.7$. Since 75% derating is needed for I_D , it is clear that a single IRF250 is not capable of handling the maximum drain current. One or more parallel MOSFETs are needed. The additional MOSFETs not only increase the current capability, but also improve the charger efficiency, since the effective MOSFET on-state resistance is reduced. Assuming equal current sharing, the MOSFET conduction loss is

$$P_{on} = \frac{1}{n} I_{BAT}^2 D R_{DSon},$$

where n is the number of MOSFETs, R_{DSon} is the MOSFET on-state resistance, and I_{BAT} is the average battery current.

The reduced conduction loss is partially offset by an increase in the switching loss due to the capacitance of the additional MOSFETs. During the off-time, the MOSFET capacitances C_{DS} and C_{DG} are charged up to a potential equal to the bus voltage. These are nonlinear capacitances that vary inversely with voltage. These capacitances become large when the junction voltages are low. However, since the energy storage is proportional to the square of the voltage, the maximum energy storage occurs at 120 V. The capacitive energy is dissipated in the MOSFETs during the on-time, resulting in a loss equal to

$$P_{sw} = \frac{n}{2}(C_{DG} + C_{DS}) V_{BUS}^2 f_S .$$

To minimize the MOSFET losses, the number of parallel devices must be carefully chosen. Neglecting gate drive losses, the MOSFET loss that is dependent on the number of parallel devices is

$$P_T = P_{on} + P_{sw} = f(n, I_{BAT}, V_{BAT}, D).$$

To find the value of n that yields the lowest value of P_T, the partial derivative of P_T with respect to n is set equal to zero:

$$\frac{\partial P_T}{\partial n} = 0,$$

where the solution is

$$n = \frac{I_{BAT}}{V_{BUS}} \sqrt{\frac{2 R_{DSon} D}{C_T f_S}} \quad . \tag{2.1}$$

For nominal values of R_{DSon} (70 mΩ), D (0.60), and C_T (1100 pF), the value n=4 satisfies Eq. (2.1) for a median I_{BAT} value of 16 A. With four MOSFETs, the effective R_{DSon} is 18 mΩ. The maximum conduction loss is

$$P_{on\max} = \frac{1}{n} I_{BAT\max}^2 D_{\max} R_{DSon\max},$$

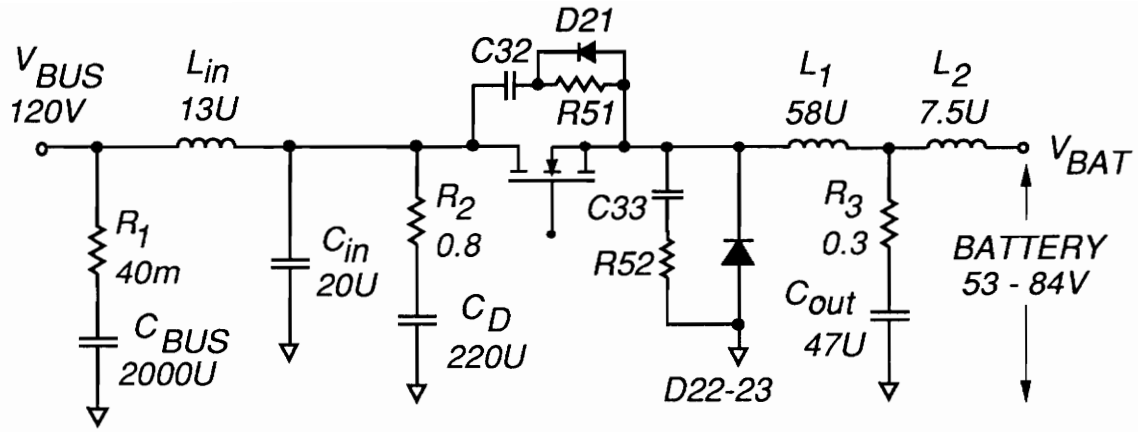
$$P_{on\max} = \left(\frac{1}{4}\right)(23A)^2 (0.7)(85m\Omega) = 7.9\ W.$$

The maximum switching loss P_{sw} is

$$P_{sw\max} = \frac{n}{2}(C_{DSmax} + C_{DGmax}) V_{BUS}^2 f_S,$$

$$P_{sw\max} = \left(\frac{4}{2}\right)(1200pF + 500pF)(120V)^2 (90KHz) = 4.4\ W.$$

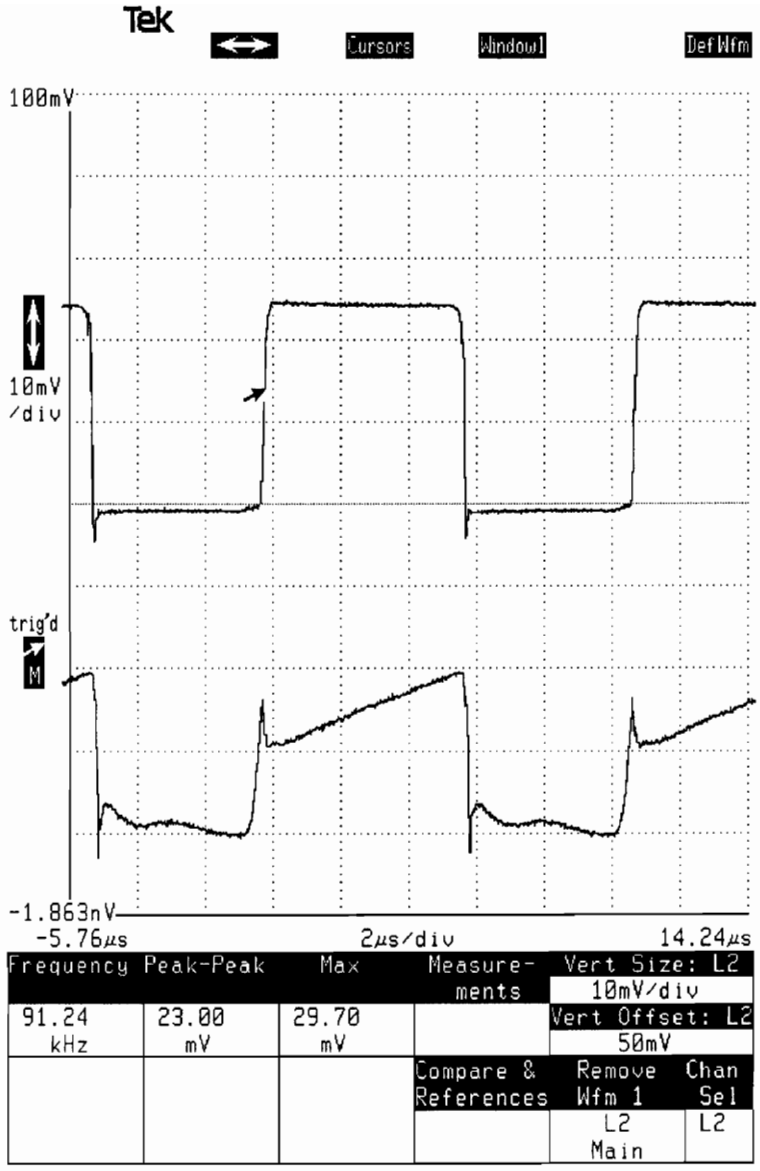
The maximum sum of P_{sw} and P_{on} is P_{Tmax}=12.3 W. The maximum RMS drain current per MOSFET is (19.2 A)/4=4.8 A. Clearly, at low charging currents, the switching loss is much greater than the conduction loss. As the battery current increases, the conduction loss becomes a much larger portion of the total MOSFET loss.



POWER MOSFETs: IRF250, FOUR IN PARALLEL

POWER RECTIFIERS D22-23: UES706, TWO IN PARALLEL

Fig. 2.1. Battery Charger Power Stage



Top: MOSFET source voltage, 50 V/div

Bottom: MOSFET drain current, 5 A/div

Fig. 2.2. Power MOSFET Voltage and Current Waveforms

Waveforms of the MOSFET source voltage and drain current are shown in Fig. 2.2. The MOSFET waveforms are clean and free of spikes due to the snubber placed across the MOSFET drain and source, as shown in Fig. 2.1. When the MOSFETs turn off, the drain current is rapidly interrupted. Without the snubber, a large positive voltage spike would be induced on the drain because of the energy stored in the interconnection inductance between the MOSFETs and C_{in}, the input filter capacitor. As the MOSFETs are turned off, the snubber provides a low impedance path for the drain current through R51 and C32, thus preventing the generation of a voltage spike.

At the end of the MOSFET off-time, the snubber capacitor, C32, is charged up to 120 V. As the MOSFETs turn on, the energy in C32 is quickly discharged via diode D21 into the MOSFETs. The power loss of this snubber is

$$P_{snubl} = \frac{1}{2}(C32)V_{BUS}^2 f_S ,$$

$$P_{snubl} = \frac{1}{2}(1000pF)(120V)^2(90KHz) = 0.65\ W.$$

2.2.2 Power Rectifiers

To meet current derating, two UES706 rectifiers are needed in parallel to form the passive power switch. These 400 V rectifiers are rated for 20 A continuous current (at a case temperature=100°C). Under normal operating conditions, the maximum total RMS rectifier current is

$$I_{RECTmax} = I_{BATmax}\sqrt{1 - D_{\min}} ,$$

$$I_{RECTmax} = (23A)\sqrt{1 - \frac{(64V)}{(120V)}} = 15.7\,A.$$

Therefore, each rectifier carries a maximum current of 7.9 A, which is 40% of the device rating. Additional parallel rectifiers produce minimal gains in efficiency due to their exponential voltage/current characteristic. Furthermore, the efficiency gain is offset by the additional rectifier mass. The reverse voltage applied to these rectifiers is 120 V, which is only 30% of the device rating.

The total maximum rectifier conduction loss is

$$P_{RECT} = V_{f,\max} I_{RECTmax} \sqrt{1 - \frac{V_{BATmin}}{V_{BUS}}},$$

$$P_{RECT} = (0.93V)(15.7A)\sqrt{1 - \frac{64V}{120V}} = 10.0\,W,$$

where the rectifier forward voltage (V_f) is measured at 25°C.

Waveforms of the rectifier voltage and current are shown in Fig. 2.3. As shown in Fig. 2.1, a snubber is placed across the rectifiers to damp out the high frequency oscillations that occur after the rectifiers turn on. The snubber capacitor, C33, charges up to the bus voltage while the rectifiers are off. The energy stored in C33 is dissipated in R52, the snubber resistor, when the rectifiers turn on. The rectifier snubber power loss is

$$P_{snub2} = \frac{1}{2}(C33)V_{BUS}^2 f_S,$$

$$P_{snub2} = \frac{1}{2}(1000pF)(120V)^2(90KHz) = 0.65\,W.$$

Top: Rectifier voltage, 50 V/div

Bottom: Rectifier current, 5 A/div

Fig. 2.3. Power Rectifier Voltage and Current Waveforms

2.3 MOSFET Gate Drive Circuit

Designing a circuit to drive the four MOSFETs in parallel is a challenging task. As shown in Fig. 2.4, the 90 KHz PWM drive signal is transformer coupled up to a 120 V level. A 12 V dc bias supply, referenced to the MOSFET sources, provides the current necessary to drive each gate capacitance. Therefore, the drive transformer does not carry large pulsating currents which could couple noise back into the UC3823 PWM chip. In order to minimize the interactions between the individual MOSFETs, a bipolar buffer stage drives each MOSFET. Without these buffer stages, it is very difficult to switch the MOSFETs cleanly. The differing V_{GS} thresholds cause the devices to turn on at different times, thus upsetting the current balancing. The resulting MOSFET turn-on transients are skewed, and unless the individual gates are decoupled from each other, the device switching can become erratic.

2.3.1 Drive Circuit Design

The frequency of the drive circuit is set by the timing components R28, C15, and C16. A 0.6 mA reference current is established by the timing resistor R28 (4.7 KΩ). To fine-tune the oscillator frequency to 90 KHz, the value of R28 is adjusted. The constant reference current produces a linear sawtooth ramp across pin 6 of the PWM chip where the timing capacitors C15 and C16 are connected. Since each capacitor value is 6800 pF, the effective timing capacitance value is 3400 pF. The amplitude of the ramp at pin 6 is 1.8 V. The timing capacitors form an ac voltage divider so that the ramp height is reduced to 0.9 V. The reduced ramp is fed to the PWM comparator input at pin 7. As

described in Chapter 3, for charger stability it is important to adjust the height of the external ramp relative to the current sense gain. Since the signal at pin 6 has a 1 V dc offset, resistors R53 and R54 establish the proper dc level at pin 7.

Since the UC3823 PWM chip has a single-ended output stage, the frequency of the PWM signal at the output (pin 14) is 90 KHz. The supply voltage to the UC3823 is 12 V dc. Because there is a 1 V drop across the positive rail of the output stage, the PWM signal at pin 14 switches between 11 V and ground. The 11 V PWM signal is ac coupled through C9 to the drive transformer; therefore, flux balance is assured for the drive transformer. Since the dc voltage across the transformer primary is zero, the average voltage of the signal at pin 14 is dropped across C9. The drive circuit waveforms are shown in Fig. 2.5.

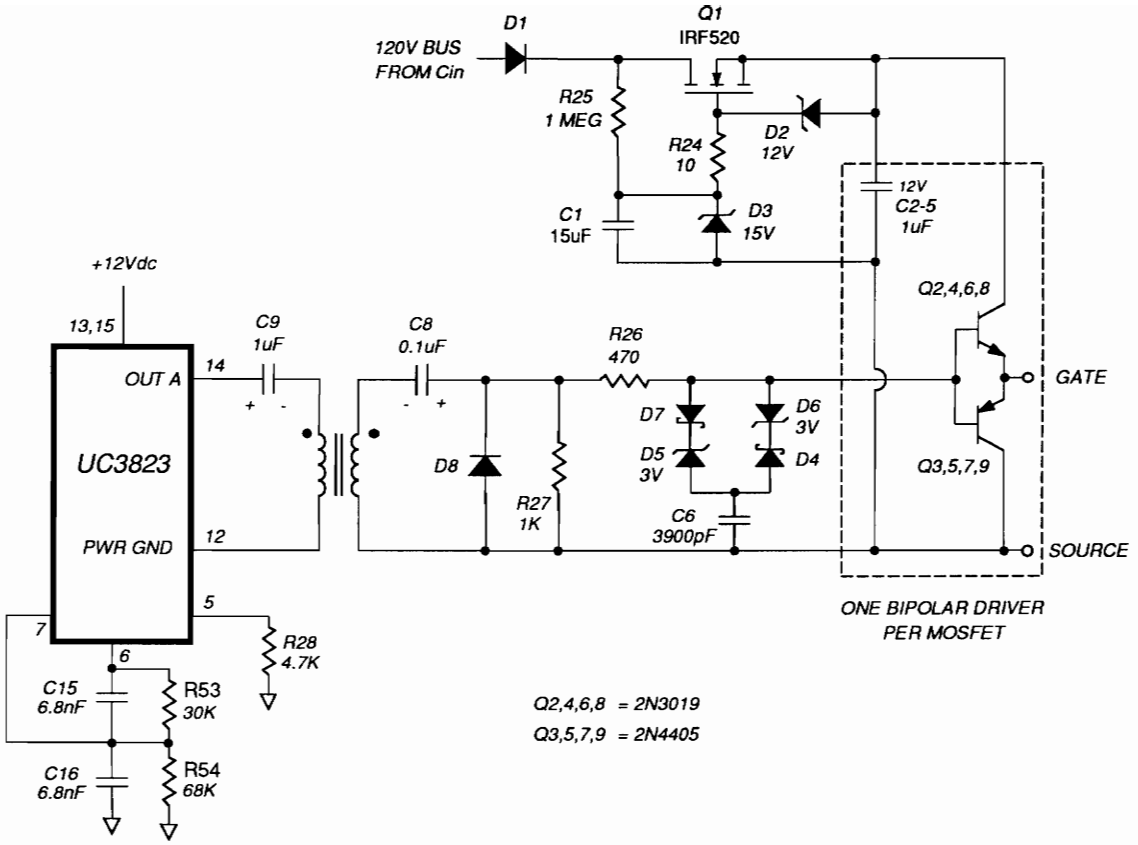


Fig. 2.4. MOSFET Gate Drive Circuit

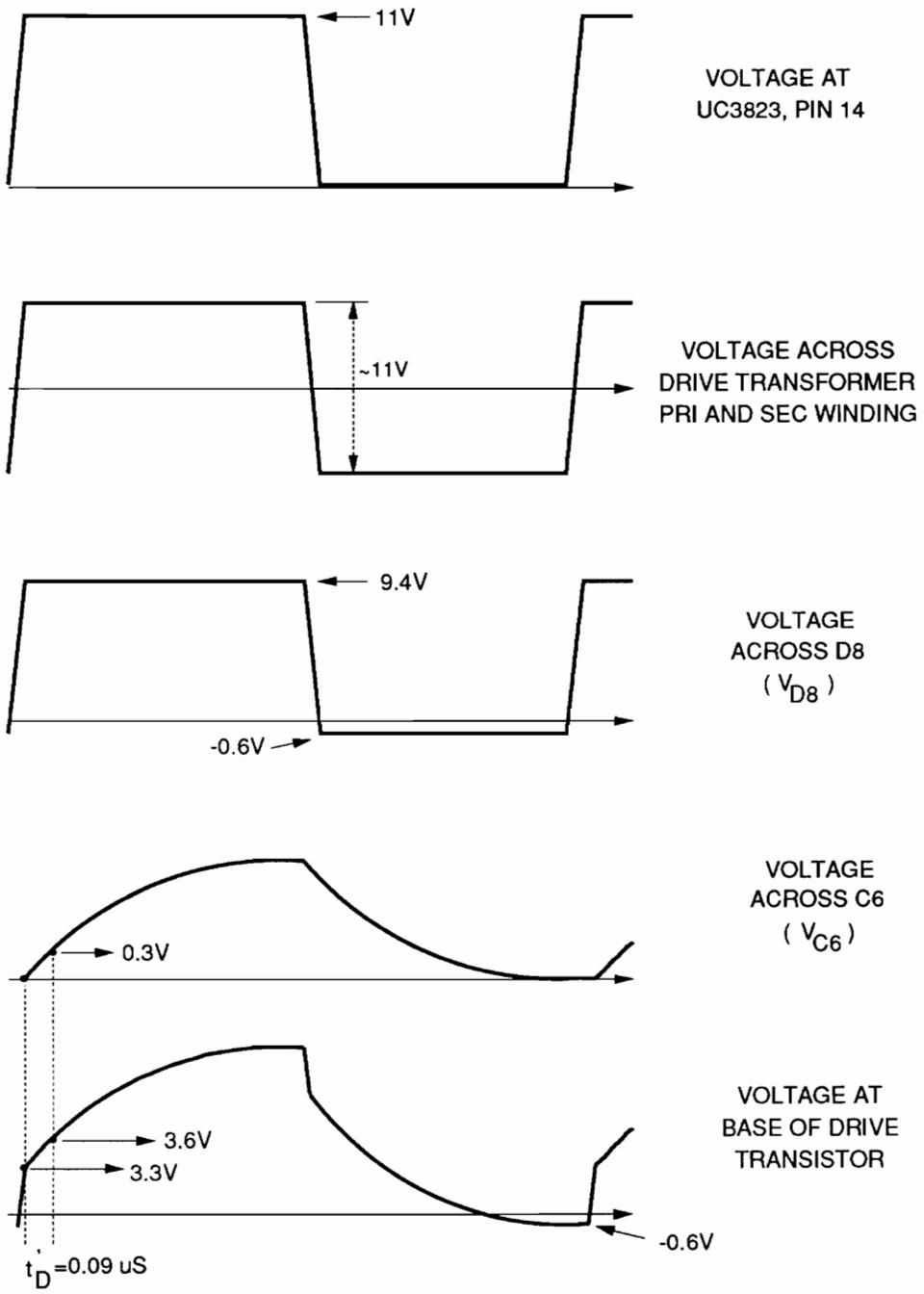


Fig. 2.5. MOSFET Drive Circuit Waveforms

Since the drive transformer has a unity turns ratio, the voltage across the secondary winding is 11 V. The PWM signal is ac coupled by C8 to the diode D8. The value of C8 is large enough (0.1 μF) so that the voltage droop across it is less than 0.5 V. Due to the cumulative impedance of the transformer, C9, and C8, the PWM signal amplitude is reduced to 10 V across D8. The dc voltage across C8 is the average voltage across D8. During the "on" period, the PWM signal is high, so D8 is biased off. Similarly, during the "off" period, the PWM signal is low, causing D8 to conduct. The anode of D8 is tied to the secondary ground, which is also connected to the MOSFET sources. Since D8 conducts during the "off" period, the PWM signal is -0.6 V during this period. As shown in Fig. 2.5, during the "on" period, the PWM signal is 10 V - 0.6 V = 9.4 V. To damp out oscillations, R27 (1 KΩ) is placed in parallel with D8. This drive circuit easily handles duty cycles ranging from 10 to 90%. This is important since the duty cycle will be as low as 10% during the V/T mode.

The speed of the drive circuit is controlled by the exponential charging of C_6 through R26. The selected speed is fast enough to efficiently switch the MOSFETs while minimizing the generation of electromagnetic interference (EMI). Very fast switching speeds also produce higher rectifier reverse recovery current spikes which not only exacerbate EMI problems, but also increase rectifier and MOSFET switching losses. The value of R26 (470 Ω) is chosen to control the base current in the driver transistors (Q2-Q9). Through experiment, a value of 3900 pF for C6 is found to produce the best switching speed.

Because the time constant of R26 and C6 is so long (1.8 μS), there is a long delay before the MOSFET gate-to-source threshold voltage (V_T) is reached. This time delay is

$$t_D = -(R26)(C6)\ln\left(1 - \frac{V_T + V_{BE}}{V_{D8}}\right),$$

$$t_D = -(470\Omega)(3900pF)\ln\left(1 - \frac{3V + 0.6V}{9.4V}\right) = 0.9\ \mu S,$$

where V_{BE} is the base-emitter drop of the driver transistor, and V_{D8} is the "on" voltage applied to the R26/C6 network. A 0.9 μS delay is unacceptable since it causes a large phase shift in the frequency region where the control loops reach unity gain. To reduce the propagation delay of the PWM signal, as shown in Fig. 2.4, C6 is placed in series with a diode network. As shown in Fig. 2.5, C6 remains uncharged until V_{D8} reaches 3.3 V, the voltage necessary to cause D7 and D5 to conduct. Therefore, the MOSFET gates are very rapidly charged up to 3.3 V. As V_{D8} rises above 3.3 V, the diodes conduct, allowing the charging of C6 to control the rise time of the MOSFET gate voltage. When the voltage at the base of the drive transistor reaches V_T+V_{BE}=3.6 V, the MOSFETs start to turn on. The PWM signal delay is reduced to the time needed to charge C6 up to $V_T + V_{BE} - V_{D7} - V_{D5} = 0.3\ V$:

$$t'_D = -(R26)(C6)\ln\left(1 - \frac{V_T + V_{BE} - V_{D7} - V_{D5}}{V_{D8} - V_{D7} - V_{D5}}\right),$$

$$t'_D = -(470\Omega)(3900pF)\ln\left(1 - \frac{3V + 0.6V - 3V - 0.3V}{9.4V - 3V - 0.3V}\right) = 0.09\ \mu S\ .$$

As indicated earlier, the bipolar driver transistors serve as a buffer to isolate the four MOSFETs from each other. Each driver transistor acts as a voltage follower when the MOSFETs are charged and discharged. The NPN transistor charges the gate-to-source capacitance (2000 pF), and the PNP transistor removes this charge to turn the MOSFETs off. Therefore, the peak gate voltage is one V_{BE} drop below the peak of the base voltage waveform shown in Fig. 2.5. This allows a peak gate voltage as high as

8.8 V, thus driving the MOSFETs further into saturation. During the gate discharge period, the gate voltage is one V_{BE} drop above the base voltage waveform shown in Fig. 2.5. Therefore, the gate-to-source is pulled down very close to zero, providing several volts of noise immunity. Because of the high current gain of the driver transistors, the large (up to 1 A) current impulses needed to turn on the MOSFETs are derived from the floating 12 V drive bias supply. Therefore, the drive transformer is practically free of impulse currents, which reduces the noise coupled back into the PWM chip.

2.3.2 Drive Transformer Design

Since high magnetic coupling is needed, a toroid core is selected for the drive transformer. As a result, the transformer has low leakage inductance, allowing for a fast and noise-free PWM signal transmission. To further ensure high coupling, the turns ratio is 1:1, and the primary and secondary windings are wound bifilar. To reduce the transformer size, a high permeability core material is needed. The material selected is a TDK manganese zinc ferrite: H5B. The core permeability is 5000, and the material saturates at 3100 Gauss at 80°C. To guard against core saturation during startup and fault conditions, the core size is selected to provide at least a 2 to 1 safety margin. The core size chosen is T6-12-3, where the outer diameter is 12 mm, the inner diameter is 6 mm, and the height is 3 mm. The primary and secondary windings each have 30 turns, so at 50% duty cycle the maximum core flux density is

$$B_{\max} = \frac{(E)10^8}{4 f_S A_e N},$$

$$B_{\max} = \frac{(11V)10^8}{4(90KHz)(.0865cm^4)(30T)} = 1180\,Gauss,$$

where E is the maximum primary voltage, A_e is the core cross sectional area, and N is the number of primary turns.

To reduce the voltage drop in the windings, a large gauge wire size (#23 AWG) is used. Since each winding requires 18 in. of wire, the winding resistance is only 30 mΩ.

To obtain low transformer magnetizing current, the primary magnetizing inductance must be high. This transformer primary has an inductance equal to

$$L_p = A_L N^2 = (1800nH/turn^2)(30turns)^2 = 1.6\,mH,$$

where A_L is the core inductance per turn. The resultant primary magnetizing current is

$$I_m = \frac{E}{4L_p F_S} = \frac{(11V)}{4(1.6mH)(90KHz)} = 19\,mA\,pk-pk.$$

2.3.3 Bias Supply Design

To operate the bipolar driver transistors, it is necessary to have a +12 V bias power supply referenced to the MOSFET sources. The design of this supply is shown in Fig. 2.4. This bias supply delivers the current needed to charge up the gate capacitances when turning on the MOSFETs. Because a large amount of charge is needed in a short time to turn on the MOSFETs, this supply must have a low output impedance and fast response. Therefore, output filter capacitors C2-C5 are located locally beside the collector of each NPN driver transistor. Though the peak gate currents are nearly 1 A, the average current delivered by this bias supply is only

$$I_{BIAS,ave} = \frac{n}{2} C_{GS}(V_{D8} - V_{BE}) f_S\,,$$

$$I_{BIAS,ave} = \left(\frac{4}{2}\right)(2000pF)(9.4V - 0.6V)(90KHz) = 3.2\ mA.$$

The bias supply output voltage is regulated at 12 V by the series pass MOSFET Q1. The gate voltage reference for Q1 is held constant at 15 V by the zener diode D3. To damp out high frequency oscillations, R24, a 10 Ω resistor, is inserted between D3 and the gate of Q1. For protection, D2, a 12 V zener, is placed between the gate and source of Q1. The bias current for D3 is supplied through R25. To minimize the power dissipation, the selected value of R25 is high (1M Ω). Since the average voltage at the anode of D3 is that of the battery, the maximum voltage across R25 is

$$V_{R25max} = V_{BUS} - V_{D1} - V_{D3} - V_{BATmin} = 120V - 0.7V - 15V - 53V = 51.3\ V.$$

The resulting dc bias current into D3 is

$$I_{D3} = \frac{V_{R25max}}{R25} = \frac{51.3V}{1M\Omega} = 51\ \mu A,$$

which dissipates this power in R25:

$$P_{R25} = V_{R25max}\, I_{D3} = (51.3V)(51\mu A) = 3\ mW.$$

To maintain a steady voltage across D3, a large capacitor, C1, is placed in parallel with D3. To prevent the discharge of C1 during the power stage MOSFET on-time, D1 is inserted between Q1 and Cin, the charger input filter capacitor.

2.4 Input Filter

Due to the pulsating nature of the input current to the battery charger, an input filter is needed to attenuate the conducted emissions to the spacecraft bus. As shown in Fig. 2.1, the input filter is primarily composed of a single section formed by L_{in} and C_{in}.

2.4.1 Filter Design

The capacitor selection for C_{in} is dependent on the maximum current drawn by the battery charger. Since the RMS current in C_{in} is high, it is necessary to select a capacitor with a low ESR; therefore, a polycarbonate capacitor is chosen. Thus the losses in C_{in} are minimized. Though the volume of these capacitors is large, the capacitance per unit mass is comparable to that of electrolytic capacitors. Under maximum load, the charger input current can be accurately approximated by a PWM squarewave. Under this assumption, the RMS value of the current in C_{in} is

$$I_{Cin,rms} = I_{BATmax}\sqrt{DD'}.$$

The maximum value of $I_{Cin,rms}$ is found by solving for the derivative of $I_{Cin,rms}$ with respect to D and setting the result equal to zero:

$$\frac{dI_{Cin,rms}}{dD} = 0.$$

The solution occurs at D=0.5, where

$$I_{Cin,\max} = \frac{1}{2}I_{BATmax} = \frac{1}{2}(23A) = 11.5\,A.$$

To handle 11.5 A RMS of ripple current, two 10 μF polycarbonate capacitors (part number CFR14LLC106) are used in parallel. These capacitors are rated for 10.9 A RMS (at 85°C); therefore, each capacitor is safely stressed up to only 53% of its current rating. The voltage rating of these capacitors is 200 V. Since the maximum applied voltage is 120 V, these capacitors are only stressed at 60% of their voltage rating. Since the ESR of each capacitor is 9 mΩ, the effective ESR of C_{in} is only 4.5 mΩ. The maximum power loss in each capacitor is

$$P_{Cin} = \left(\frac{11.5A}{2}\right)^2 (4.5m\Omega) = 0.15\ W.$$

The equivalent series inductance (ESL) of these capacitors is also very low: 24 nH. Therefore, the resonance of each capacitor and its ESL is adequately high: 325 KHz.

To reduce mass, the filter resonant frequency is chosen as high as possible while maintaining low output impedance and adequate ripple current attenuation. In order to meet these objectives, a value of 13 μH is needed for L_{in} . The resulting filter resonant frequency is

$$f_{0,in} = \frac{1}{2\pi\sqrt{L_{in}C_{in}}} = \frac{1}{2\pi\sqrt{(13\mu H)(20\mu F)}} = 9.87\ KHz.$$

Lossless damping of the input filter is provided by the ac coupling of R_2 across C_{in}. To produce low peaking in the filter transfer function at the resonant frequency, the value of R_2 is chosen to be equal to $Z_{0,in}$, the filter characteristic impedance:

$$Z_{0,in} = \sqrt{\frac{L_{in}}{C_{in}}} = \sqrt{\frac{13\mu H}{20\mu F}} = 0.8\ \Omega\ .$$

The Q of the input filter is

$$Q_{in} = \frac{Z_{0,in}}{R_2} = \frac{(0.8\Omega)}{(0.8\Omega)} = 1.$$

Since C_D, the 220 μF ac coupling capacitor, is in series with R_2, the ESR of this capacitor need not be low; therefore an electrolytic capacitor is chosen. Because $C_D \gg C_{in}$, the damping resistor, R_2, appears in parallel with C_{in} and L_{in} at the filter resonant frequency. Therefore, the filter effectively has a second order response [2]. The input filter transfer function, $H_I(s)$, can accurately be approximated by

$$H_I(s) = \frac{1}{1 + \frac{L_{in}}{R_2}s + L_{in}C_{in}s^2} \quad .$$

A plot of this transfer function is shown in Fig. 2.6, where the 10 KHz resonant peak in the filter gain is only +1.8 dB. Furthermore, it can be seen that the input filter provides -38 dB attenuation of the 90 KHz current harmonic. This transfer function is valid for both directions of signal flow. More specifically, the charger's input current ripple is attenuated in the same manner as is the bus voltage ripple across this filter. As shown in Fig. 2.7, in the bus voltage regulation mode, the maximum charger input current ripple is 320 mA pk-pk, and the 90 KHz bus voltage ripple is less than 30 mV pk-pk. The bus voltage ripple is primarily the product of the charger input current ripple and the ESR of the bus capacitor.

The output impedance of this filter as seen by the charger is

$$Z_I(s) = \frac{L_{in}s}{1 + \frac{L_{in}}{R_2}s + L_{in}C_{in}s^2} \quad .$$

A plot of the output impedance of this filter is shown in Fig. 2.8. The peak output impedance at the resonance is -1.8 dB, or 0.8 Ω, which is the value of R_2 . At low frequencies, the impedance is determined solely by L_{in} , and above the filter resonance, the impedance is determined by C_{in} .

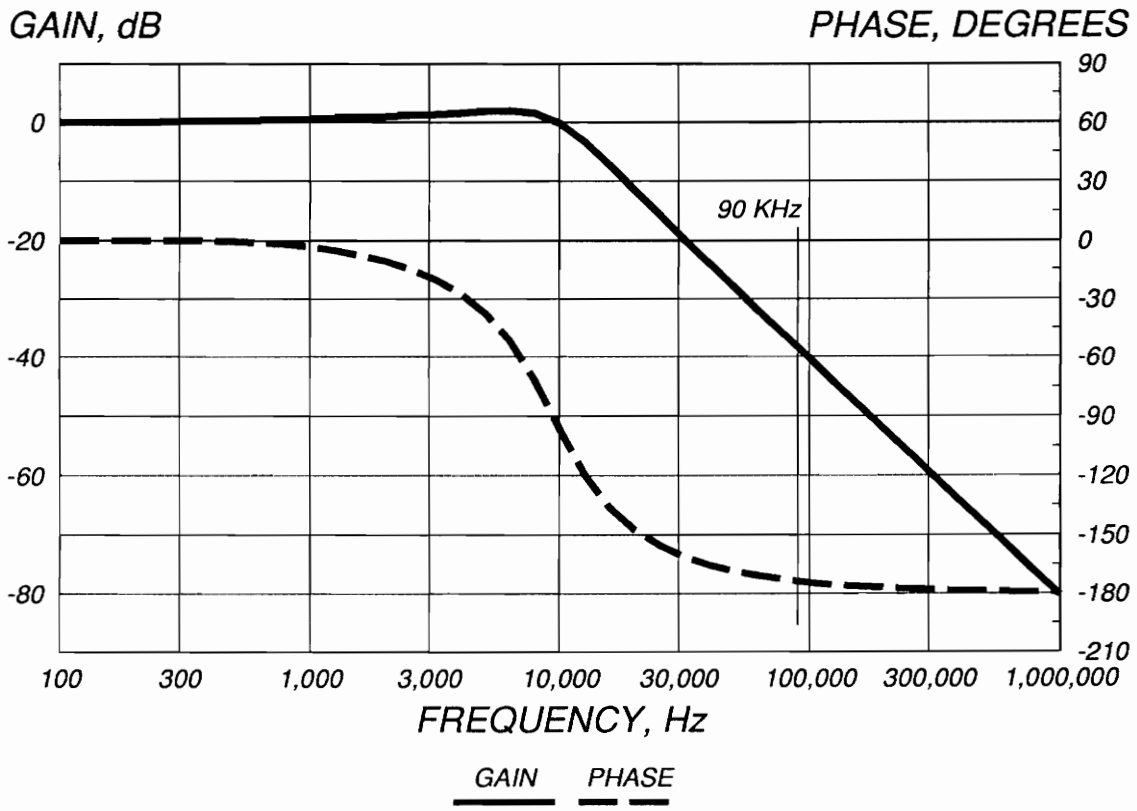
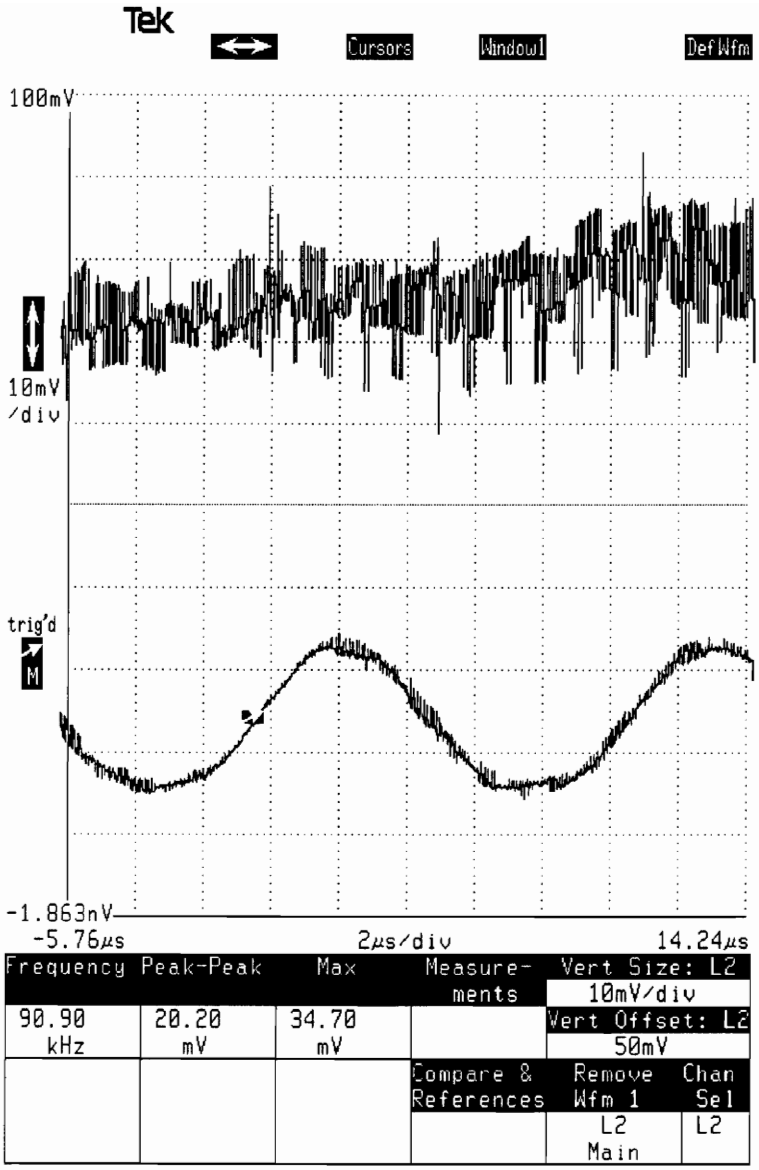


Fig. 2.6. Input Filter Transfer Function



Top: Bus voltage ripple, 10 mV/div

Top: L_{in} ripple current, 200 mA/div

Fig. 2.7. Input Filter Ripple Waveforms

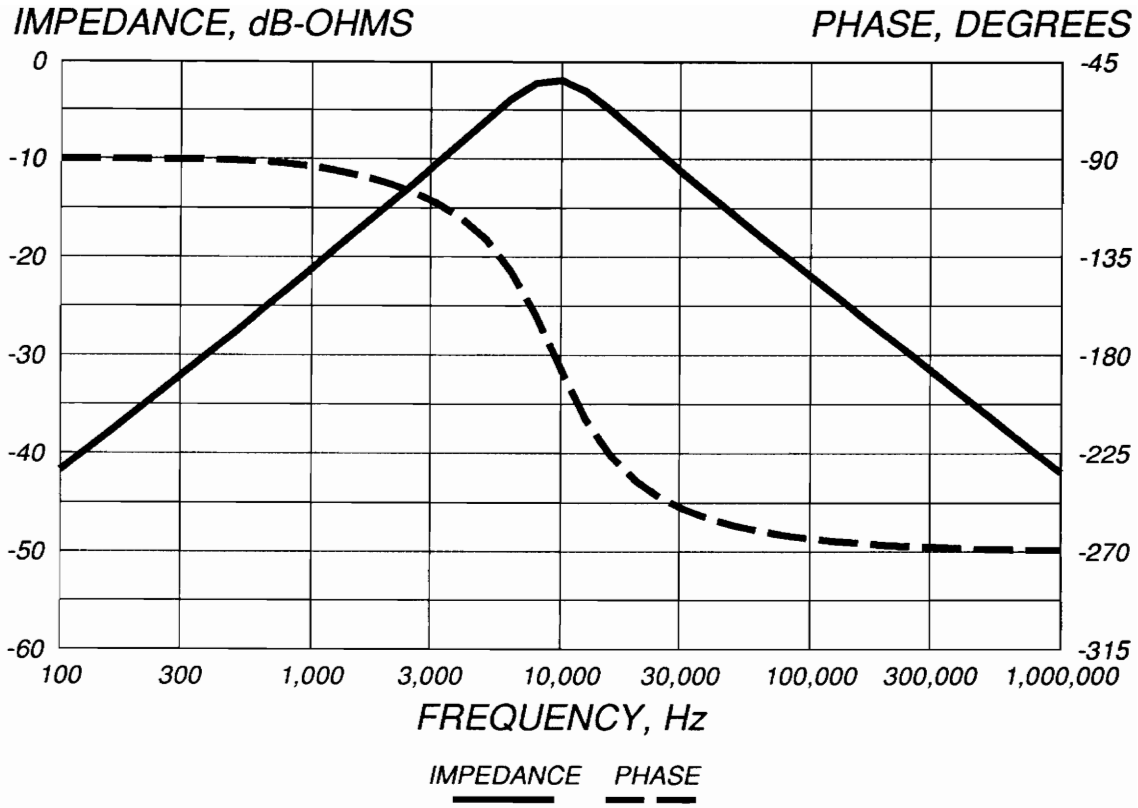


Fig. 2.8. Input Filter Output Impedance

2.4.2 Input Filter Inductor Design

The maximum current flowing in L_{in} occurs when the charger is delivering 23 A to a 64 V battery. Under these conditions, the current in L_{in} is

$$I_{Lin,\max} = \frac{V_{BAT} I_{BAT}}{\eta\, V_{BUS}},$$

$$I_{Lin,\max} = \frac{(64V)(23A)}{(0.94)(120V)} = 13.0\,A,$$

where η is the charger efficiency. To handle this large amount of dc current, a molypermalloy powder (MPP) toroid core is used. MPP cores are capable of supporting a high level of dc flux with minimal permeability reduction. To select the core size, the maximum inductive energy storage must be calculated:

$$E_{Lin} = \frac{1}{2} L_{in} I_{Lin,\max}^2,$$

$$E_{Lin} = \frac{1}{2}(13\mu H)(13A)^2 = 1.1\ mJ.$$

The smallest core capable of storing this amount of energy is the Magnetics 55848. The required number of turns are

$$N_{Lin} = \sqrt{\frac{L_{in} l_m 10^8}{0.4\pi\mu A}},$$

$$N_{Lin} = \sqrt{\frac{(13\mu H)(5.09cm^2)10^8}{0.4\pi(60)(.226cm^2)}} = 19.7T \sim 20T,$$

where l_m is the mean core magnetic path length, μ is the core permeability, and A is the core cross sectional area.

The amount of core permeability reduction under maximum current must be determined. First, using Ampere's Law, the maximum value of H_{Lin}, the magnetic field, must be found:

$$H_{Lin} = \frac{0.4\pi N_{Lin} I_{Lin,\max}}{l_m},$$

$$H_{Lin} = \frac{0.4\pi(20T)(13A)}{(5.09cm^2)} = 64\ Oersted.$$

From the dc magnetization curves in the Magnetics data book, for the maximum level of H_{Lin}, the core permeability is reduced by 24%. Therefore, the inductance of L_{in} falls to 10 μH under worst case conditions. Also determined by the magnetization curves, the maximum core flux density is 3300 Gauss, well below the saturation level of 7000 Gauss.

The maximum ac current in L_{in} is 0.11 A RMS, resulting in a 0.64 V RMS drop. The induced ac flux density is

$$B_{ac} = \frac{E_{RMS}10^8}{4ANf_S},$$

$$B_{ac} = \frac{(0.64V)10^8}{4(0.226cm^2)(20T)(90KHz)} = 39\ Gauss.$$

From the Magnetics 60 μ core loss curves, this level of B_{ac} causes a very small core loss:

$$P_{core} = (0.02W/Lb)(0.023Lb) = 0.5\ mW.$$

The inductor is wound with #15 AWG wire. Since 20 turns requires 22 inches of wire, the winding resistance is $R_{Lin} = (22in)(0.27m\Omega/in) = 5.9\ m\Omega$. The maximum copper loss in L_{in} is

$$P_{cu} = I^2_{Lin,\max} R_{Lin} = (13A)^2(5.9m\Omega) = 0.99\ W.$$

The windings are spaced far enough apart to minimize the parasitic capacitance. Since the winding capacitance is only 2.6 pF, the self-resonance of this inductor is very high: 27 MHz. This is very important in reducing the conducted emissions and susceptibility of the battery charger.

2.5 Output Filter

Since the battery current must have a very low ripple content, a two section output filter is used. If a single inductor were to be used as the output filter, the inductor mass would be prohibitively large. As shown in Fig. 2.1, the output filter is composed of L_1, L_2, and C_{out}. The filter component values are selected to give the required current attenuation while minimizing losses and mass.

2.5.1 Filter Design

The first inductor, L_1, reduces the 90 KHz ripple current to 5.5 A pk-pk. The second inductor, L_2, reduces the ripple to below 230 mA for an overall filter current attenuation of -42 dB. Both current ripple waveforms are shown in Fig. 2.9. The center leg of the output filter contains C_{out} in series with R_3 , a damping resistor. The value chosen for C_{out} is 47 μF since this amount of capacitance is needed to keep the ac voltage across C_{out} less than 1 V. This greatly simplifies the output filter design and analysis since the C_{out} ripple voltage can be assumed to be zero. Since C_{out} is in series with R_3, the ESR of this capacitor need not be low, so an electrolytic capacitor is used. To achieve the necessary filter attenuation, an inductance of 6.6 μH is chosen for L_2. The filter characteristic impedance is

$$Z_O = \sqrt{\frac{L_T}{C'_{out}}} = \sqrt{\frac{6.6\mu H}{20\mu F}} = 0.57\ \Omega,$$

where

$$L_T = \frac{L_1 L_2}{L_1 + L_2} = \frac{(58\mu H)(7.5\mu H)}{58\mu H + 7.5\mu H} = 6.6\ \mu H,$$

and C'_{out} is the value of C_{out} at 10 KHz. (The capacitance of the capacitor used for C_{out} decreases with frequency.)

For effective damping, the value of R_3 is kept close to Z_O so that the filter Q is close to unity. The Q of the output filter is

$$Q_O = \frac{Z_O}{R_3} = \frac{0.57\Omega}{0.3\Omega} = 1.9.$$

The R_3 value, however, must also be minimized to reduce losses. The switching ripple current in L_1 flows through R_3. Therefore, the power loss in R_3 is

$$P_{R3} = \left(\frac{I_{L1,pp}}{2\sqrt{3}}\right)^2 R_3,$$

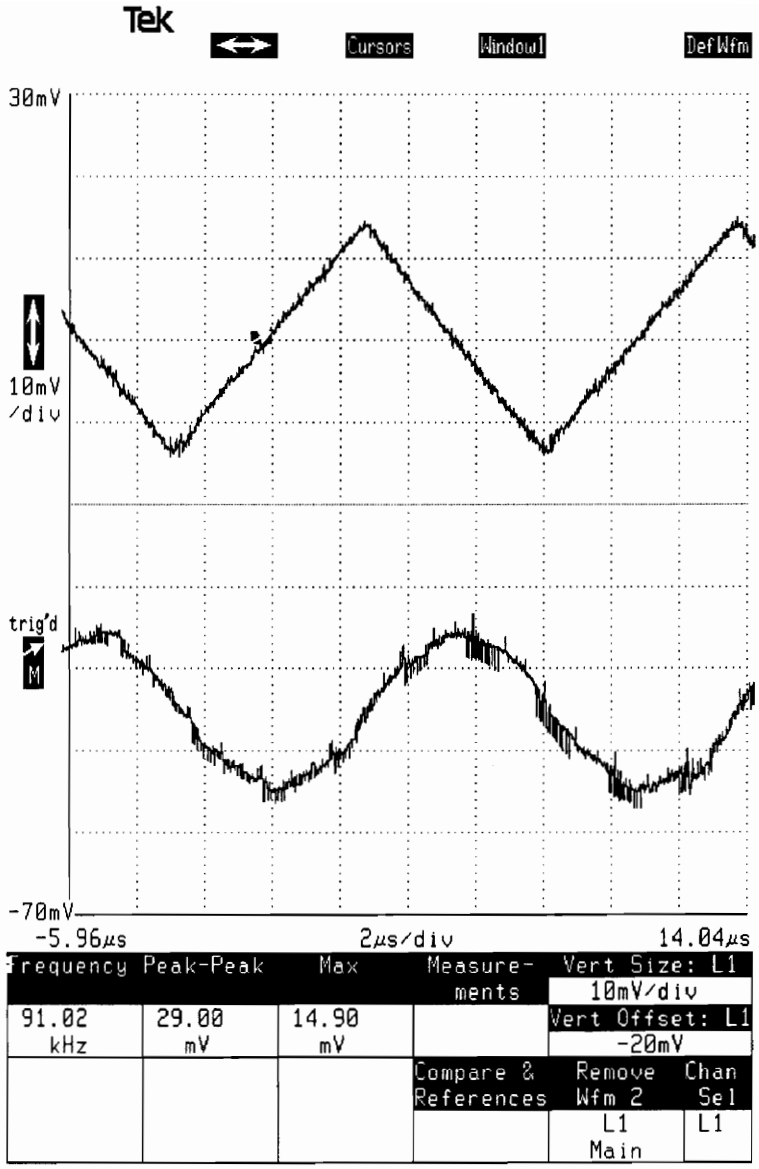
$$P_{R3} = \left(\frac{(5.5A)}{2\sqrt{3}}\right)^2 (0.3\Omega) = 0.76\ W.$$

Since the ESR of the capacitor selected for C_3 is 0.3 Ω, a separate resistor for R_3 is not needed.

The transfer function of this filter, interpreted as the response of the current in L_2 to a change in the current in L_1, is

$$H_O(s) = \frac{\hat{i}_{L2}}{\hat{i}_{L1}} = \frac{1 + R_3 C_{out} s}{1 + R_3 C_{out} s + L_2 C_{out} s^2} \quad ,$$

where R_{BAT} is assumed to be zero since $R_3 \gg R_{BAT}$. A plot of this transfer function is shown in Fig. 2.10. At 13 KHz, there is a complex pole set due to C_{out} and L_2. There is also a zero at 26 KHz caused by C_{out} and R_3. Thus the transfer function has a -20 dB per decade slope at 90 KHz.



Top: L1 current ripple, 2 A/div

Bottom: L2 current ripple, 100 mA/div

Fig. 2.9. Output Filter Current Ripple Waveforms

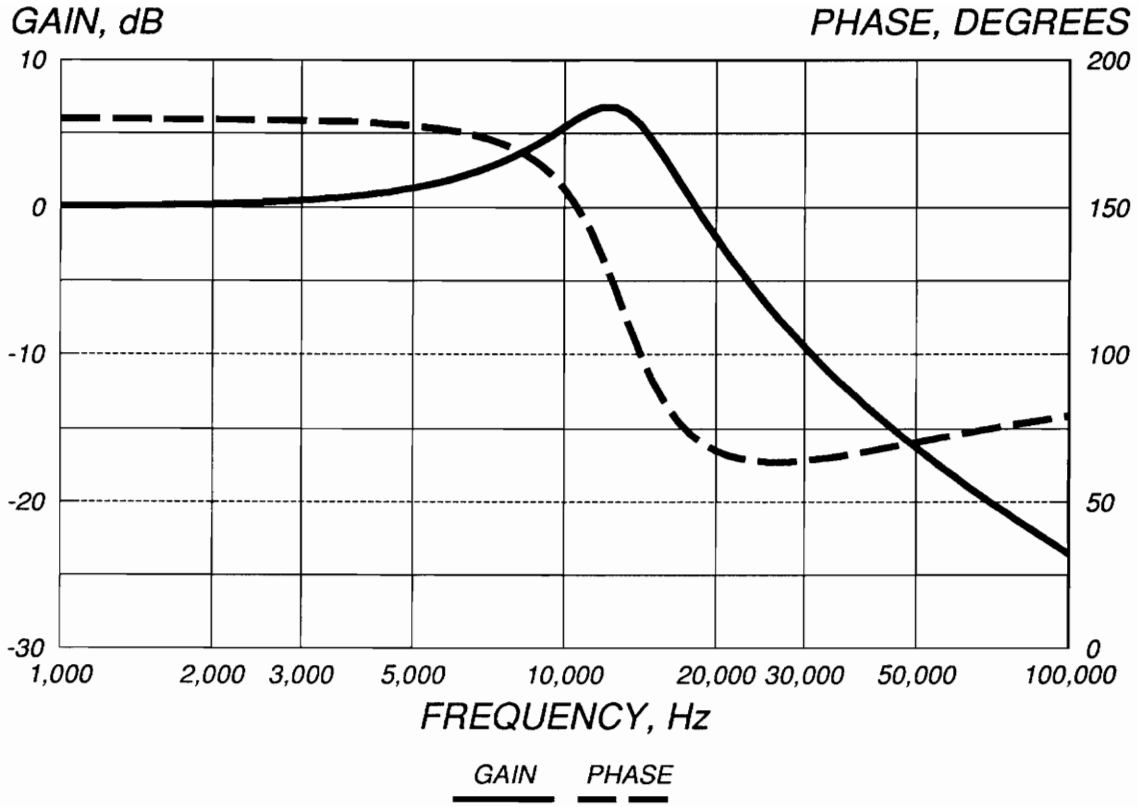


Fig. 2.10. Output Filter Transfer Function

2.5.2 Inductor L_1 Design

The design of L_1, the main energy storage inductor, is crucial since this component has a great impact on the charger's efficiency and mass. To facilitate the selection of the best design for this inductor, all the inductor design equations were placed in a spreadsheet program. By incorporating different core sizes and design parameters in the spreadsheet program, it was possible to choose an inductor design that minimized the mass and losses.

A cut C-core with 1 mil laminated Metglas was chosen for this inductor. Because of the thin laminations and the high resistivity of Metglas, the core losses are less compared to other laminated core materials. Since the saturation flux density, B_{max}, is so high (1.4 Tesla) for this magnetic material, the mass of this inductor can be minimized. This is seen in the relation [3] used to select the core size through the area product A_p:

$$A_P = 0.84\left[\frac{L_1 I_{BAT\,PK}^2}{B_{\max} K_W}\right]^{1.16},$$

$$A_P = 0.84\left[\frac{(58\mu H)(25.75A)^2}{(1.4T)(0.4)}\right]^{1.16} = 0.0375\ in^4,$$

where K_W is the core window area utilization factor. K_W is defined as the ratio of the total conductor cross sectional area to the available core window area. Since K_W = 0.4, the remaining 60% of the core window area is needed for the bobbins and conductor insulation. To maximize K_W, copper foil is used as the conductor. Thus the copper loss of the inductor is minimized.

After evaluating numerous cores with area products close to the value calculated above, the Magnetics core MC1200 was selected. To calculate the required number of turns, the energy storage and the current density was determined. The maximum inductive energy storage is

$$W_{L1} = \frac{1}{2} L_1 I_{L1peak}^2 ,$$

$$W_{L1} = \frac{1}{2} (58\mu H)(25.75A)^2 = 0.0192\,J.$$

The current density is

$$J_{L1} = \frac{4.805 W_{L1}}{B_{max} K_W A_p} ,$$

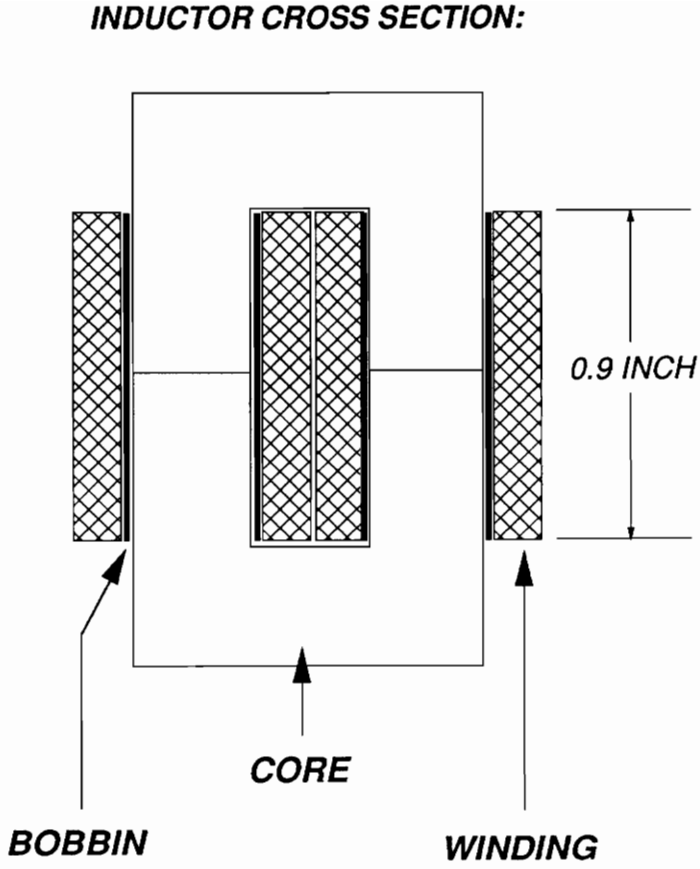
$$J_{L1} = \frac{4.805(0.0192J)}{(1.3T)(0.4)(0.035in^4)} = 5.07\ A/mm^2 ,$$

where the actual A_p value is used, and the maximum value of B_{max} is 1.3 T for safety purposes. The required number of turns is

$$N_{L1} = \frac{A_W K_W J_{L1}}{I_{BATmax}} ,$$

$$N_{L1} = \frac{(242mm^2)(0.4)(5.06A/mm^2)}{(23A)} = 21.3\,T,$$

where A_W is the core window area. To obtain an even number of turns, the value of N_{L1} is set to 22. As shown in Fig. 2.11, the inductor is wound with two separate bobbins, each containing 11 turns. This split winding approach halves the core gap loss produced in a single bobbin inductor [3]. The bobbins are cut from 40 mil thick fiberglass tubes that are sized to fit snugly over the core.



CORE: MAGNETICS MC1200-1B (METGLAS)

SPLIT BOBBIN: 11 TURNS EACH OF 7 MIL FOIL

GAP: 17 MIL NOMEX PER LEG

Fig. 2.11. Construction of L1 Inductor

Since the length of the core window is 1 inch, the copper foil is cut to 0.9 inch to provide a 0.05 inch margin at each end of the winding. The necessary thickness of the copper foil is

$$T_f = \frac{1.55 A_W K_W}{N_{L1} G},$$

$$T_f = \frac{1.55(242 mm^2)(0.4)}{(22T)(0.9in)} = 7.5\ mils/turn,$$

where G is the width of the copper foil. Due to constraints in the availability of copper foil, the conductor is formed by stacking 5 mil and 2 mil foils. To wind each bobbin, 28 inches of foil are needed. The resulting total winding resistance is 6.4 mΩ. The maximum copper loss is $P_{CU} = (23A)^2(6.3m\Omega) = 3.33\ W$.

To insulate the turns from each other, the copper foil stack is covered with 2 mil thick Kapton tape. This tape is very durable and has excellent dielectric properties. To minimize the copper losses, it is important to use a very thin tape so that thicker copper foil can be used. Thin tape, however, increases the winding capacitance. For this inductor design, the winding capacitance is 20 pF, which results in a sufficiently high resonant frequency (5 MHz).

Due to the high permeability of the core material, the inductance is determined from the length of the core gap. From [3], the total gap length is

$$l_g = \frac{0.4\pi N_{L1}^2 A_C 10^{-8}}{L_1},$$

$$l_g = \frac{0.4\pi(22T)^2(0.605 cm^2)10^{-8}}{58\mu H} = 0.0636\ cm,$$

where A_C is the core cross sectional area. Since there is a thin insulation layer on each lamination, the effective value of A_C is 80% of the overall core cross section area. Because of the fringing flux at the gaps in the core, the inductance is increased. Therefore, to obtain the required inductance, the gap length must be increased. The new gap length is

$$l_g' = l_g\left(1 + \frac{l_g}{\sqrt{A_c}}\ln\left(\frac{5.08G}{l_g}\right)\right),$$

$$l_g' = (0.0636cm)\left(1 + \frac{(0.0636cm)}{\sqrt{(0.605cm^2)}}\ln\left(\frac{5.08(0.9in)}{(0.0636cm)}\right)\right) = 0.086\ cm.$$

Since the total gap length is 0.086 cm, the gap in each individual leg is 0.043 cm, or 17 mils. Because it is an incompressible material, nomex is used to form the 17 mil spacers in each core leg.

The gap length, l_g', must be minimized to reduce the fringing flux, which causes a gap loss when eddy currents are induced in the core laminations. The gap loss, P_G, is largely dependent on the ac flux density, B_{ac}, where

$$B_{ac} = \frac{6.28 \times 10^{-5} N_{L1} I_{ac}}{l_g'},$$

$$B_{ac} = \frac{6.28 \times 10^{-5}(22T)(5.5A)}{(0.086cm)} = 0.088\ Tesla,$$

where I_{ac} is the peak-to-peak amplitude of the current in L_1. The resulting gap loss is

$$P_G = 0.099 D_W l_g' f_S B_{ac}^2,$$

$$P_G = 0.099(0.375in)(0.086cm)(90KHz)(0.088Tesla)^2 = 2.23\ W,$$

where D_W is the lamination width. The core loss, P_C, is highly dependent on the switching frequency:

$$P_C = 3.42 \times 10^{-10} A_C l_M B_{ac}^{2.04} f_S^{2.23},$$

$$P_C = 3.42 \times 10^{-10} (0.604 cm^2)(9.53 cm)(0.088 Tesla)^{2.04} (90 KHz)^{2.23} = 1.55\ W,$$

where l_M is the core magnetic path length [3]. The total core loss is

$$P_C + P_G = 3.8\ W.$$

The maximum total inductor loss is

$$P_{TOT} = P_{CU} + P_C + P_G = 3.33W + 3.8W = 7.1\ W.$$

2.5.3 Inductor L_2 Design

To reduce the battery current ripple below 230 mA pk-pk, L_2 must be 7.5 μH. According to NASA, there is approximately 5 ft of cable connecting the charger to the battery. This cable length was installed in the prototype charger power system. The inductance of the cable was measured at 1.2 μH. Therefore, the remaining 6.3 μH of L_2 consists of a discrete inductor. An MPP toroid core was selected for this inductor. To select the core size, the maximum inductive energy storage was calculated:

$$E_{L2} = \frac{1}{2} L_2 I_{BAT,\max}^2,$$

$$E_{L2} = \frac{1}{2} (6.3 \mu H)(23A)^2 = 1.7\ mJ.$$

To store this amount of energy, the Magnetics 55848 core is chosen. The required number of turns are

$$N_{L2} = \sqrt{\frac{L_2 l_m 10^8}{0.4\pi\mu A}},$$

$$N_{L2} = \sqrt{\frac{(6.3\mu H)(5.09cm^2)10^8}{0.4\pi(60)(.226cm^2)}} = 14\ Turns,$$

where l_m is the mean core magnetic path length, μ is the core permeability, and A is the core cross sectional area.

The amount of core permeability reduction under maximum current must be determined. First, using Ampere's Law, the maximum value of H_{L2}, the magnetic field, must be found:

$$H_{L2} = \frac{0.4\pi N_{L2} I_{BAT,\max}}{l_m},$$

$$H_{L2} = \frac{0.4\pi(14T)(23A)}{(5.09cm^2)} = 79\ Oersted.$$

From the dc magnetization curves in the Magnetics data book, for the maximum level of H_{L2}, the core permeability is reduced by 33%. Therefore, the inductance falls to 4.2 μH under worst case conditions. However, the inductance of the battery cable is not a function of current. Thus the minimum total L_2 value is 5.7 μH, a 24% reduction from normal. Also determined by the magnetization curves, the maximum core flux density is 3900 Gauss, well below the saturation level of 7000 Gauss.

The maximum ac current in L_2 is 0.082 A RMS, resulting in a 0.23 V RMS drop. The induced ac flux density is

$$B_{ac} = \frac{E_{RMS} 10^8}{4ANf_S},$$

$$B_{ac} = \frac{(0.23V)10^8}{4(0.226cm^2)(14T)(90KHz)} = 20\ Gauss.$$

From the Magnetics 60 μ core loss curves, this level of B_{ac} causes a very small core loss:

$$P_{core} = (0.006W/Lb)(0.023Lb) = 0.2\ mW.$$

The inductor is wound with four parallel strands of #18 AWG wire. Since 14 turns requires 18 inches of wire, the winding resistance is

$$R_{L2} = (18in)(0.133m\Omega/in) = 2.4\ m\Omega.$$

The maximum copper loss in L_2 is

$$P_{cu} = I^2_{BAT,\max} R_{L2} = (23A)^2(2.4m\Omega) = 1.27\ W.$$

2.6 Summary

The design of the power stage has been presented for the Space Platform power system. Mass and efficiency are the major design constraints. Therefore, the power switching components and the input and output filters are designed for minimum losses and mass. A summary of the power stage component masses is given in Table 2.1, where the total mass is 309 grams (10.9 oz).

A graph of the battery charger efficiency is shown in Fig. 2.12. The housekeeping power consumption is not included in these measurements. Since this power is typically only 0.6 W, this omission has virtually no effect on the overall charger efficiency. These measurements are made with four Fluke model 77 digital multimeters (DMM). The charger input and output voltages are measured directly with a pair of the DMMs. The

charger input and output currents are measured by sensing the voltage across precision noninductive 0.01 Ω meter shunts installed in the charger input and output lines. Since the current signals have an appreciable 90 KHz ripple content, the shunt voltages are fed through a low-pass filter before being routed to the DMMs. Thus any measurement errors due to high frequency limitations of the DMMs are eliminated.

The worst case charger efficiency occurs when the battery voltage is 64 V. The efficiency is lowest here since the power rectifier voltage drop is the highest percentage of the battery voltage. Furthermore, with low battery voltage, the input current to the charger will also be maximum, causing maximum conduction losses in the input filter and power semiconductors. As expected, the efficiency increases with battery voltage.

Table 2.1. Power Stage Component Mass

Component	Value	Quantity	Mass (each) (grams)	Mass (total) (grams)
L_{in}	13 μH	1	26	26
C_2	10 μF	2	33	66
C_D	220 μF	1	20	20
MOSFET	IRF250	4	13	52
Rectifier	UES706	2	7	14
L1	58 μH	1	94	94
C_{out}	47 μF	1	9	9
L2	6.3 μH	1	28	28
Total				309

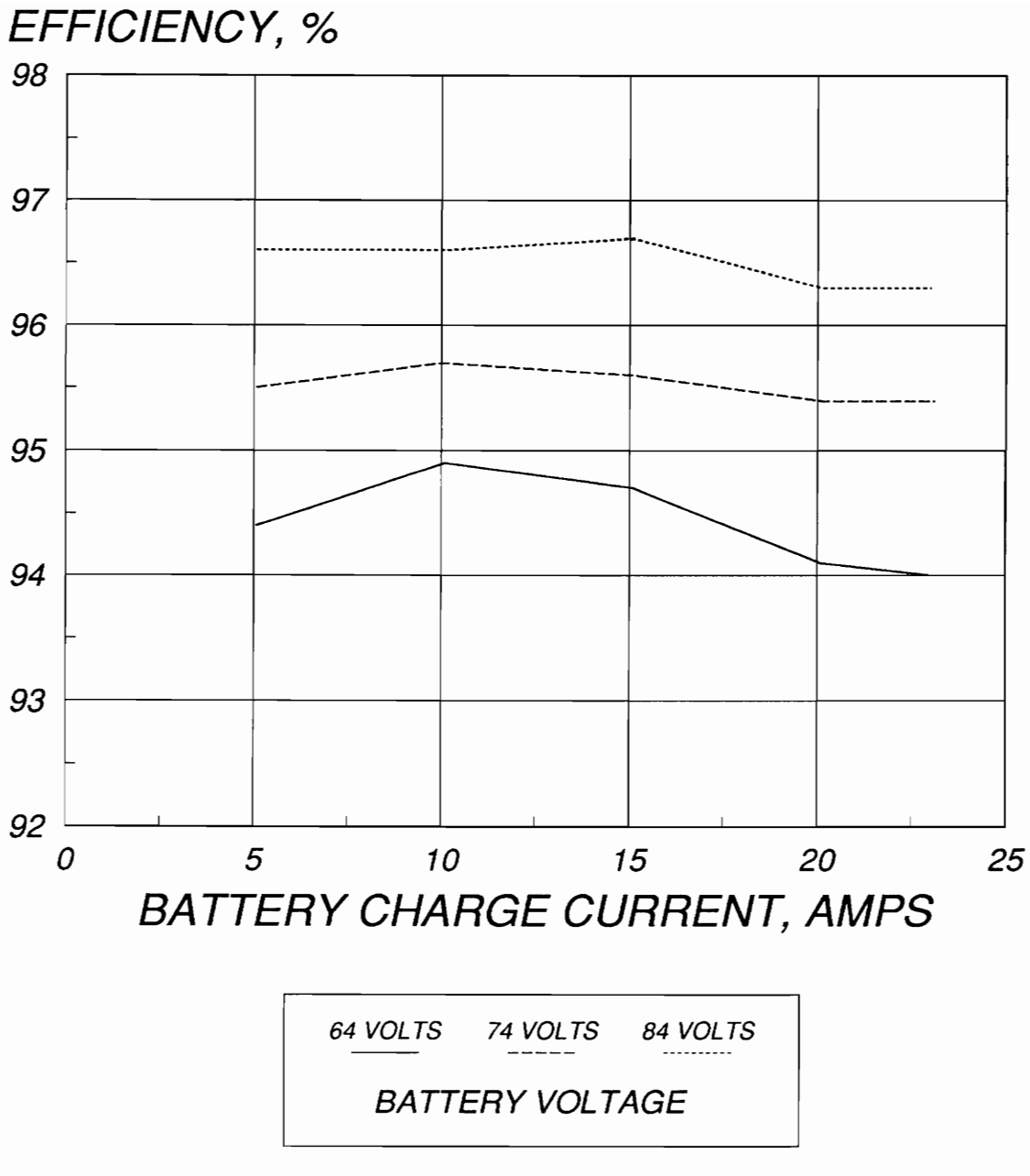


Fig. 2.12. Battery Charger Efficiency

3. Current Regulation Mode

3.1 Introduction

This chapter describes the design of the two battery regulation feedback loops: charge current and V/T. As shown in Fig. 3.1, the charger has three basic control loops that are ORed together to produce a control signal, v_c, which is fed to the PWM circuit. Since each loop has an integrating error amplifier, only one loop is active at a time. The voltage loop senses and regulates the bus voltage during the transition from eclipse to sunlight. Thus during the voltage regulation mode, the charge current and V/T loops are inactive. When the solar array generates enough power to charge the battery and to supply the load required by the spacecraft, the charge current loop is activated. The charge current loop regulates the battery charging current according to I_{REF}, the commanded rate. When the battery approaches a full state-of-charge, the V/T loop controls the charging current according to the battery voltage and temperature. For the charge current loop, average current mode control is implemented through the integrating error amplifier U4. Furthermore, for each loop, current injection control is employed by summing i_S, the instantaneous inductor current, with the control signal v_c. The resulting signal, v_r, is compared against a ramp to generate a PWM signal (d) to control the power stage.

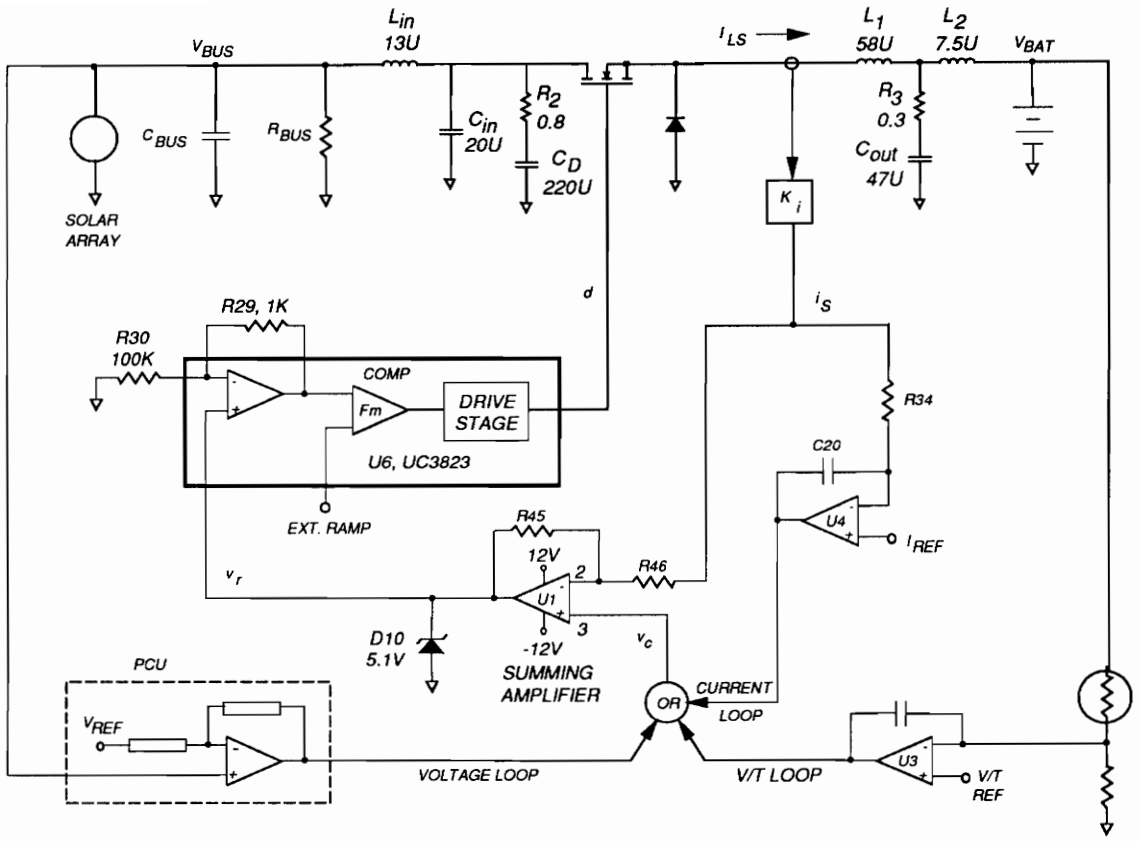


Fig. 3.1. Battery Charger Control Circuit

3.2 Charge Rate Selection Circuit

The primary purpose of the charger is to control the manner in which energy is returned to the battery. Proper design of the charge current regulation circuitry is necessary to ensure that the batteries will be recharged in a manner enabling them to last through the tens of thousands of cycles in their five year life span. The batteries are charged at the 16 different current levels provided by the rate selection circuit. The commanded charge rates range from 0.85 A to 23 A, with 1.5 A increments between each charge rate. Rate 1 is 0.85 A which corresponds to C/60 where C is the battery ampere-hour capacity. Since rate 16 is 23 A, this corresponds to (50 AH)/(23 A)=C/2.2.

3.2.1 Current Sensing

In order to properly regulate the dc level of the charging current, the battery current must be sensed accurately. A dual current transformer approach was used in this design because it is an accurate and high speed current sense method. As shown in Fig. 3.2, a current transformer (CT), T2, senses the MOSFET drain current, another CT, T3, senses the rectifier current, and the two signals are added together. The result is i_S, a replication of the instantaneous current in L_1. The current sense gain is designated as K_i as shown in Figs. 3.1 and 3.7. Because the current in L_1 is sensed, the actual battery current, i_{L2}, is not directly regulated. However, because the average values of the inductor currents are identical, this method of current sensing enables regulation of the dc current into the battery.

The CT*s* are carefully designed so that the current sensing error is less than 1%. The current sensing accuracy is limited by the CT magnetizing current; therefore, the CT magnetizing inductance must be large. However, to minimize mass, the CT core size must not be too large. To satisfy these requirements, the Magnetics core 50153-1F is used. This toroid core consists of a 1 mil thick continuously wound supermalloy tape. The high core permeability makes it possible to obtain a high inductance without an excessive number of turns. The CT is designed with 200 turns of #30 AWG wire. The inductance of CT winding is

$$L_{CT} = \frac{\mu N^2 A_e}{l_m},$$

$$L_{CT} = \frac{(12000)(400\pi \times 10^{-11} H/cm)(200T)^2 (0.038cm^2)}{3.49cm} = 45\ mH,$$

where μ is the core permeability, A_e is the effective core cross sectional area, and l_m is the core magnetic path length. The maximium core magnetizing current is

$$I_{mag} = \frac{V_{on} T_{on,\max}}{2L_{CT}},$$

$$I_{mag} = \frac{(3V)(8\mu S)}{2(45mH)} = 0.27\ mA\,peak,$$

where V_{on} is the maximum CT secondary voltage during the period $T_{on,max}$, occuring under maximum duty cycle. Since the turns ratio is 200:1, the maximum CT secondary current is I_{BATmax} /200 = (23 A)/200 = 115 mA p-p. The error due to the magnetizing current is

$$CT\,error = \frac{0.27mA}{115mA} = 0.23\%.$$

The maximum core flux density is

$$B_{\max} = \frac{V_{on} 10^8}{4 f_S A_e N},$$

$$B_{\max} = \frac{(3V)10^8}{4(90KHz)(0.038cm^2)(200Turns)} = 110\ Gauss,$$

which is well below the core saturation level of 6500 Gauss.

To reset the CTs, the diode networks formed by D12-15 are used. During the CT "off" time, the voltage across the secondary winding changes polarity, causing the zener diode to conduct. Thus volt-second balance is achieved. To ensure core resetting under all conditions, the zener voltage must be adequately high. The maximum volt-seconds during the CT "on" time is $V_{on} T_{on,\max} = (3V)(8\mu S) = 24\ \mu VS$. To reset the CT, the following reverse voltage must be applied to the secondary during the "off" time:

$$V_{rev} = \frac{24\mu VS}{T_S - 8\mu S} = \frac{24\mu VS}{11.1\mu S - 8\mu S} = 7.7\ V.$$

Since the zener voltage is 10 V, the CT is reset under all conditions.

The current sense gain is

$$K_i = \frac{R32}{N} = \frac{20\Omega}{200Turns} = 0.1\ V/A = -20\ dB\Omega.$$

An oscillograph of the voltage across R32, the current sense resistor, is shown in Fig. 3.3. To filter out the high frequency spikes in the voltage across R32, the low pass filter formed by R31 and C18 is used. The filter corner frequency is

$$f_{cs} = \frac{1}{2\pi \times R31 \times C18} = \frac{1}{2\pi(82\Omega)(3300pF)} = 590\ KHz.$$

As shown in the bottom waveform in Fig. 3.3, the voltage spikes are smoothed out.

R33, a 100 Ω resistor, and test points TP1 and TP2 are provided to allow injection of a transformer coupled signal so that the current feedback loop can be measured.

3.2.2 Rate Selection Circuit Design

As shown in Fig. 3.1, the sensed current signal, i_S, is fed to an error amplifier (U4), where it is subtracted from I_{REF}, the charge current reference signal. As shown in Table 3.1, there are 16 different commanded values of battery charge rates. The 16 different values of I_{REF} are provided by the digital-to-analog (D/A) converter shown in Fig. 3.4. The error signal, i_S - I_{REF}, is integrated by the amplifier, so the steady-state current regulation error is zero. Since the dc value of the battery current is regulated, this amplifier produces average current mode control [6]. The amplifier gain is

$$A_{U4} = \frac{1}{2\pi f \times R34 \times C20} = \frac{1}{2\pi f(33K\Omega)(3300pF)}.$$

This gain is selected to provide a high (-36dB) attenuation of the ripple content of i_S. Since the amplitude of the ac portion of i_S is (5.5 A)/K_i = 0.55 V p-p, the 90KHz component of v_c, the amplifier output signal, is only 9 mV p-p. Therefore, v_c is essentially pure dc and insensitive to variations in the peak-to-peak amplitude of i_{L1} occurring under different duty cycles. The v_c signal is subsequently added back to the sense signal, i_S, and the resulting waveform is compared against a sawtooth ramp to generate the duty cycle. As detailed in the Section 3.6, the addition of i_S to v_c produces the benefits of conventional current mode control.

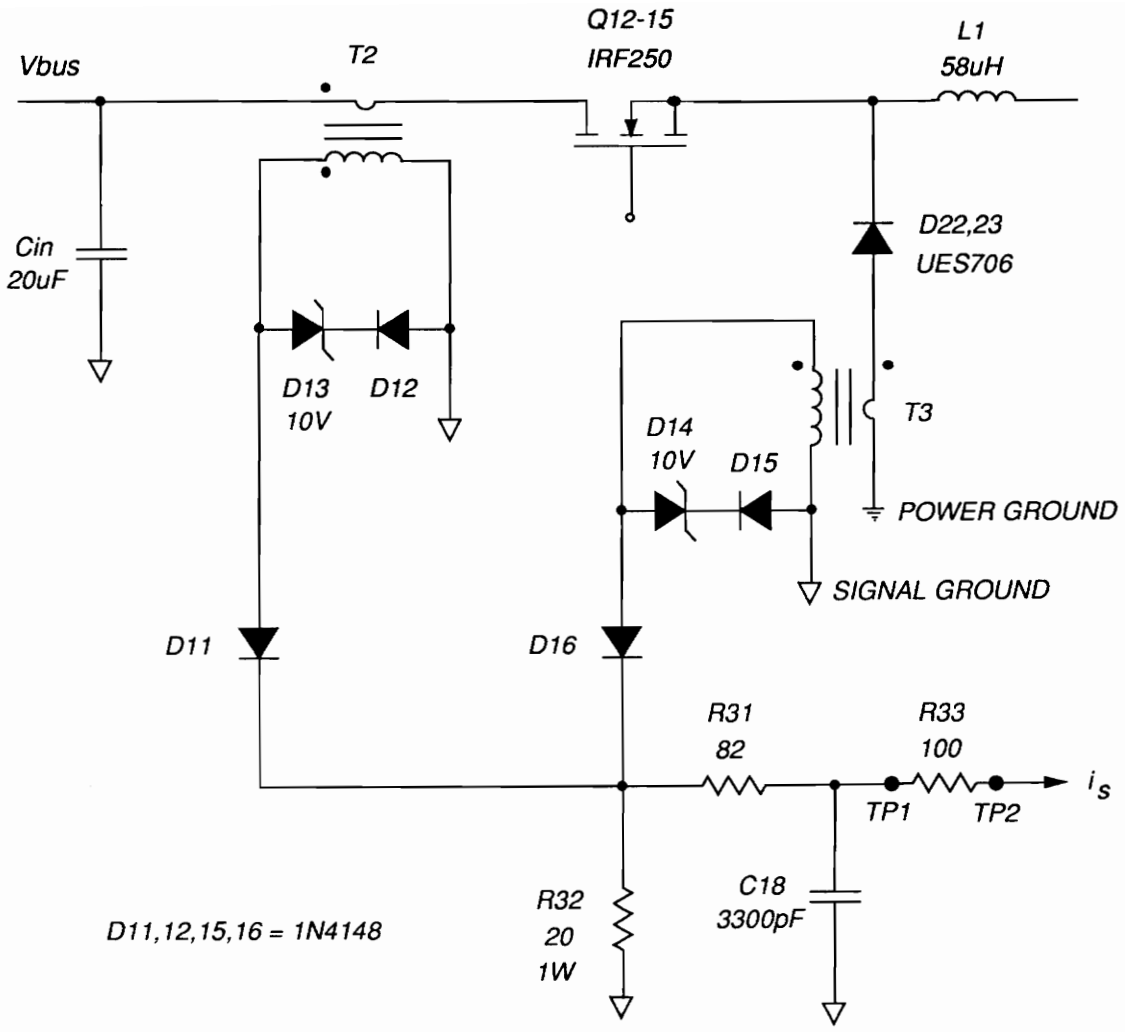
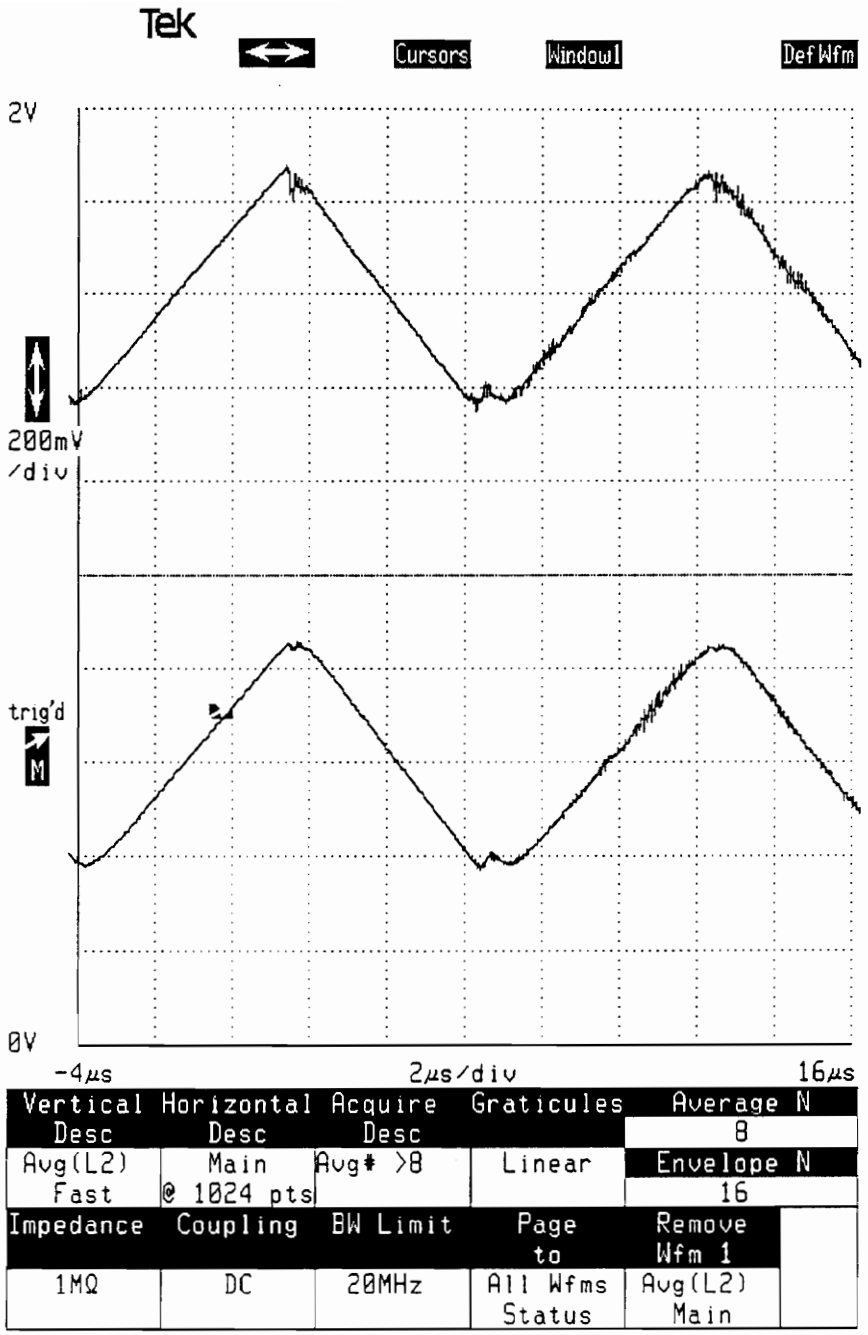


Fig. 3.2. Battery Current Sense Circuit



Top: V_{R32} , 0.2 V/div. Bottom: I_S , 0.2 V/div.

Fig. 3.3. Current Sense Waveforms

Table 3.1. Charge Current Rate Selection

CHARGE RATE	CURRENT (AMPS)	COMMAND DATA			
		S1	S2	S3	S4
1	0.85	0	0	0	0
2	2.33	0	0	0	1
3	3.80	0	0	1	0
4	5.28	0	0	1	1
5	6.76	0	1	0	0
6	8.23	0	1	0	1
7	9.71	0	1	1	0
8	11.19	0	1	1	1
9	12.66	1	0	0	0
10	14.14	1	0	0	1
11	15.62	1	0	1	0
12	17.09	1	0	1	1
13	18.57	1	1	0	0
14	20.05	1	1	0	1
15	21.52	1	1	1	0
16	23.00	1	1	1	1

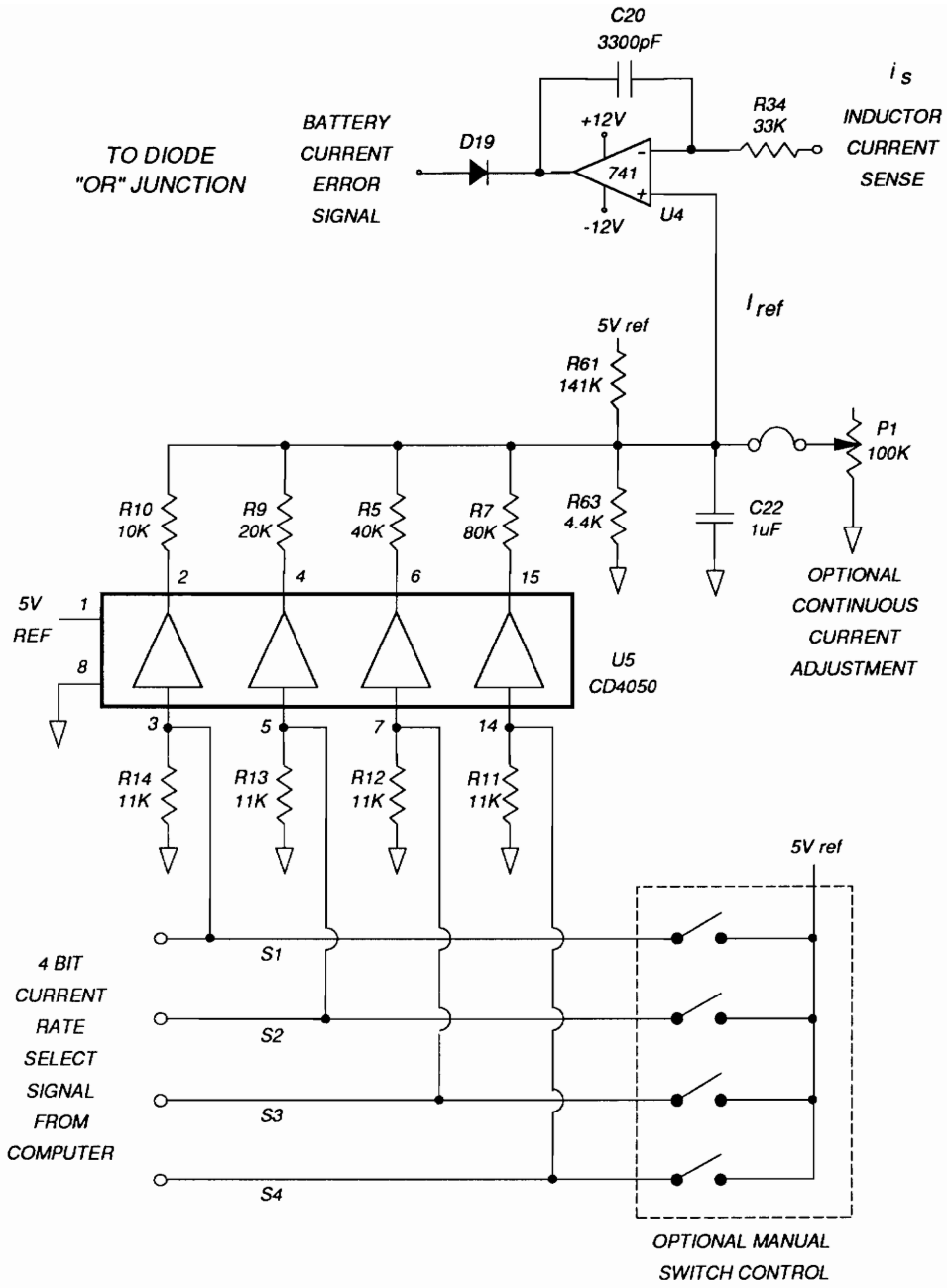


Fig. 3.4. Charge Rate Selection Circuit

Since there are 16 charge current rates, the digital command contains 4 bits. In the absence of a computer, the commands are issued manually by switches S1-4 across pulldown resistors R11-14. Capacitor C22 provides debouncing of the manual switch commands. The D/A converter is formed by four CMOS buffers in U5 and the binary resistor network of R10, 9, 5, and 7. To ensure high accuracy for the charge current reference signal (i_{REF}), the values of R10, 9, 5, and 7 (10, 20, 40, 80 KΩ) are much higher than the saturated channel resistance (100 Ω) of the CMOS buffers. To provide the necessary dc offset, the voltage divider formed by R61 and R63 is used. When the command (0,0,0,0) is issued, the value of i_{REF} must be (Rate 1)K_i = (0.85 A)(0.1 V/A) = 0.085 V. In this case, since R10, 9, 5, and 7 are switched to ground, the following relation holds:

$$i_{REF} = (5Vref)\frac{R_x \parallel R63}{R_x \parallel R63 + R61},$$

$$0.085V = (5Vref)\frac{4.44K\Omega \parallel R63}{4.44K\Omega \parallel R63 + R61}, \tag{3.1}$$

where

$$R_x = R10 \parallel R9 \parallel R5 \parallel R7 = \left(\frac{2}{3}\right)^2 R10 = \left(\frac{4}{9}\right)(10K\Omega) = 4.44\,K\Omega.$$

When the command (1,1,1,1) is issued, the value of i_{REF} must be (Rate 16)K_i = (23.0 A)(0.1 V/A) = 2.30 Vdc. In this case, since R10, 9, 5, and 7 are switched high to the 5 V reference, the following relation holds:

$$i_{REF} = (5Vref)\frac{R63}{R_x \parallel R61 + R63},$$

$$2.30V = (5Vref)\frac{R63}{4.44K\Omega \parallel R61 + R63}. \tag{3.2}$$

The solution of Eqs. (3.1) and (3.2) is R61 = 141 KΩ and R63 = 4.4 KΩ. The values of these two resistors are adjusted slightly during test to account for initial component tolerances. The increment between adjacent values of i_{REF} is

$$\frac{(Rate\,16 - Rate\,1)K_i}{(Total \quad \# \quad of \quad rates) - 1} = \frac{(23.0A - 0.85A)(0.1V/A)}{16 - 1} = 0.148\ V.$$

To assist during testing, a method is provided for continuous adjustment of the charge current reference signal. By adjusting the 100 KΩ potentiometer P1, the value of i_{REF} can be varied continuously from 0 to 2.3 V. To disable this adjustment, the jumper between P1 and C22 is removed.

The accuracy of the charge current regulation circuit is shown in Table 3.2. Since the error specification is 1% of the full scale battery current, the regulation error must be less than ±0.23 A for each charge rate. As shown in Table 3.2, the measured regulation error meets the specification for each charge rate. Since the charger is in DCM, the current error for rate 1 is much larger than the error for rate 2. In DCM, the ringing in the L1 inductor current waveform during the dead-time causes the relatively large current error for rate 1.

Table 3.2. Charge Current Regulation Accuracy

Rate	Commanded Current (A)	Actual Current (A)	Current Error (A)
1	0.85	0.64	-0.21
2	2.33	2.36	0.03
3	3.80	3.74	-0.06
4	5.28	5.24	-0.04
5	6.76	6.70	-0.06
6	8.23	8.21	-0.02
7	9.71	9.66	-0.05
8	11.19	11.16	-0.03
9	12.66	12.69	0.03
10	14.14	14.20	0.06
11	15.62	15.66	0.04
12	17.09	17.18	0.09
13	18.57	18.66	0.09
14	20.05	20.19	0.14
15	21.52	21.66	0.14
16	23.00	23.20	0.20

3.3 V/T Control Circuit

As the battery is charged at a constant current, the battery voltage rises until the V/T control circuit is activated. The V/T control circuit, shown in Fig. 3.5, gradually reduces the current until the battery is fully charged. The battery voltage is sensed with a voltage divider containing a thermistor to account for the effects of battery temperature. The battery state-of-charge is dependent on temperature. Therefore, to ensure proper charging of the battery under all conditions, there are several V/T reference levels [5].

The V/T control circuit design is based upon the set of battery V/T curves. A set of V/T curves for the Space Platform nickel hydrogen batteries is shown in Fig. 3.6. Though the Space Platform V/T control circuit is to have eight V/T curves, for simplicity, only three curves are used in this prototype charger design. The bottom curve (1), is used at the beginning of life for the spacecraft. As the battery degrades, it is necessary to switch to higher curves to ensure full charging of the battery. Therefore, at the end of life for the battery, it will be necessary to operate on curve 3, which is 7% higher than curve 1.

The temperature of the batteries will be maintained between -10 and +20°C. Since the voltage of a fully charged battery is temperature dependent, the V/T curves have a particular slope: -0.2 V/°C. Thus for a given V/T curve, the voltage at the end of charge is 8% higher at -10°C than at +20°C.

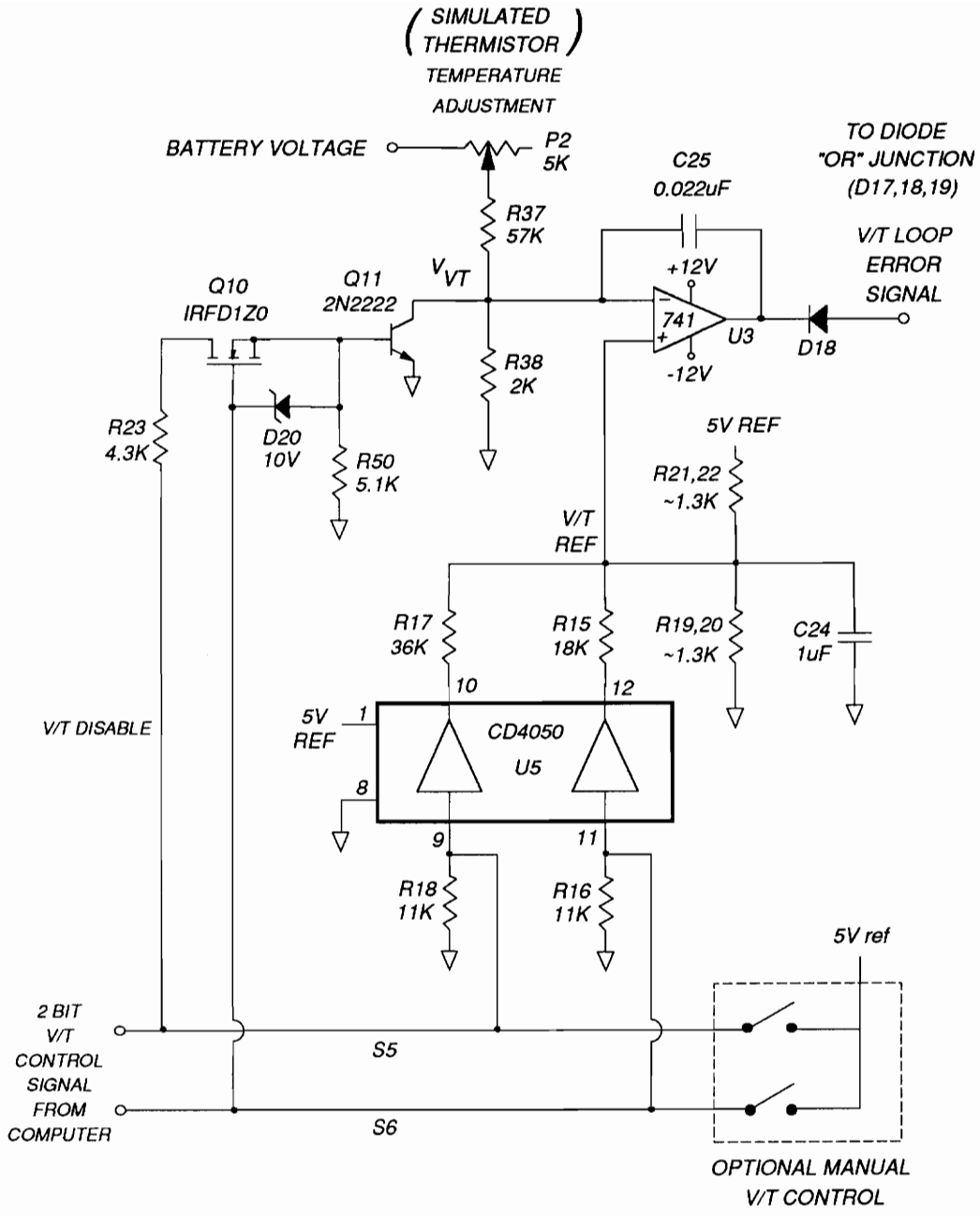


Fig. 3.5. Volt/Temperature Control Circuit

CURVE	S5	S6
1	0	0
2	1	0
3	0	1
V/T DISABLE	1	1

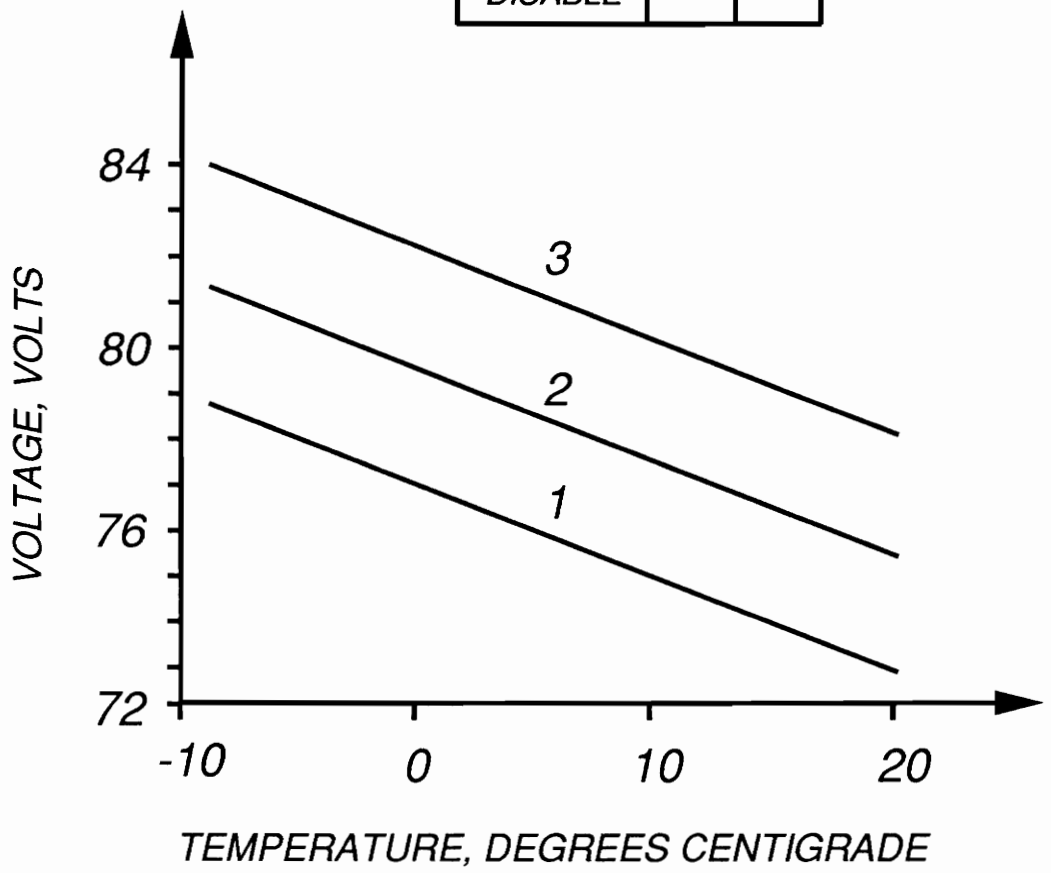


Fig. 3.6. Battery Charger V/T Curves

As shown in Fig. 3.5, to simulate the battery thermistor, a potentiometer (P2) is inserted in the resistive divider used to sense the battery voltage. To minimize power dissipation, the total divider resistance ($R_T = R_{P2} + R37 + R38$) is carefully chosen. For a power loss less than 1/8 W, the total resistance must be greater than

$$R_T = \frac{V_{BATmax}^2}{(1/8W)} = \frac{(84V)^2}{(0.125W)} = 56\,K\Omega.$$

Since the nominal divider output voltage (V_{VT}) is chosen as 2.5 V, the value of R38 can be selected:

$$R38 \geq \frac{V_{VT}R_T}{V_{BATmax}} = \frac{(2.5V)(56K\Omega)}{(84V)} = 1.7\,K\Omega.$$

Thus R38 is set to 2 KΩ. To find the values of R37 and R_{P2}, the following nominal conditions are assumed: R_{BAT} = 74 V, R_{P2} = 0, T = -10°C, and V_{VT} = 2.5 V. The sum of R_{P2} and R_{37} is

$$R_{UP} = R37 + R_{P2} = R38\frac{(V_{BAT} - V_{VT})}{V_{VT}}, \tag{3.3}$$

$$R_{UP} = (2K\Omega)\frac{(74V - 2.5V)}{2.5V} = 57\,K\Omega.$$

Thus $R37 = 57K\Omega$. When the battery temperature increases to +20°C, V_{VT} must decrease by 8%: $V'_{VT} = V_{VT}(0.92) = (2.5V)(0.92) = 2.3V$. Using Eq. (3.3), the new value of R_{UP} must be

$$R'_{up} = (2K\Omega)\frac{(74V - 2.3V)}{2.3V} = 62\,K\Omega.$$

The 5 KΩ difference between R'_{up} and R_{up} is the value needed for P2. As shown in Fig. 3.7, the battery temperature is simulated by the potentiometer P2. Full clockwise rotation corresponds to +20°C and R_{P2} = 5 KΩ. At full counterclockwise rotation, the P2 resistance is zero, indicating a temperature of -10°C.

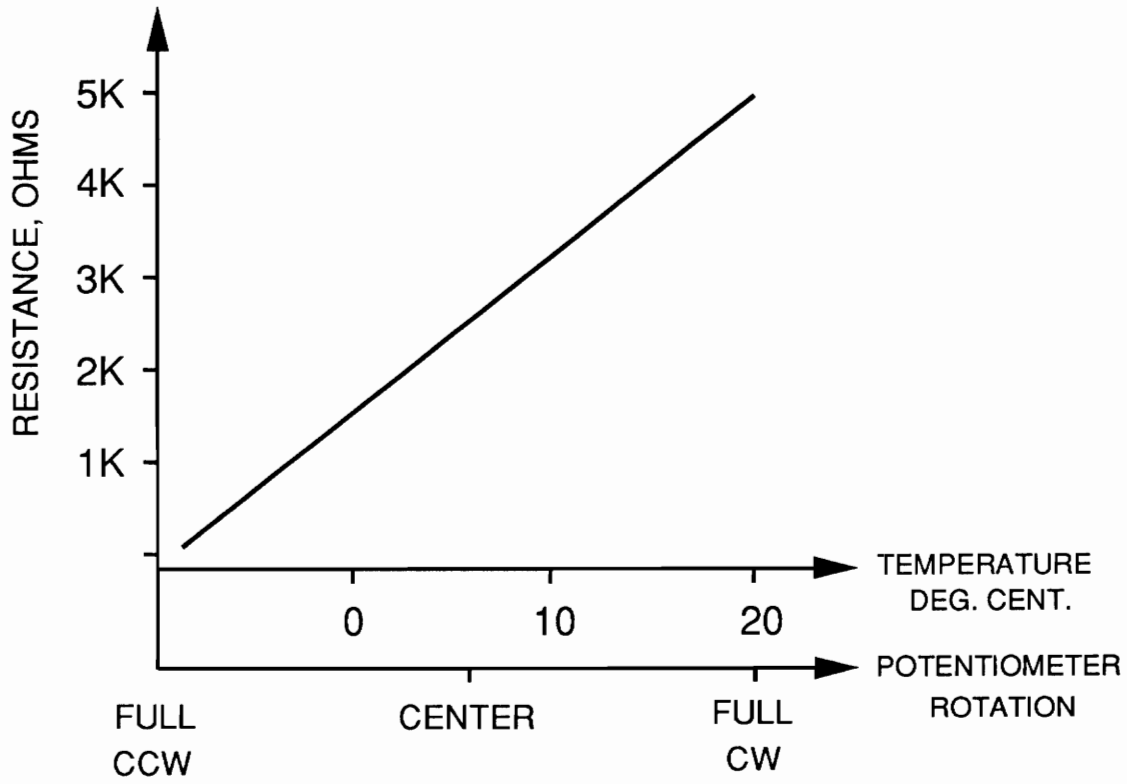


Fig. 3.7. Simulated Battery Thermistor

As shown in Fig. 3.5, the sensed battery voltage (V_{VT}) is subtracted from a reference voltage, and the error signal is amplified by U3. The feedback capacitor C25 is selected to give a low amplifier bandwidth:

$$BW_{U3} = \frac{1}{2\pi\, R37 \times C25} = \frac{1}{2\pi(57K\Omega)\,(0.022\mu F)} = 127\ Hz.$$

The U3 bandwidth need not be high because the battery voltage changes very slowly. The V/T feedback loop analysis is identical to that of the charge current regulation loop which is covered in Section 3.6.

Since the V/T circuit is controlled by a digital signal, a D/A converter is used to generate the three V/T curves. Since the control signal consists of 2 bits, there are 4 possible V/T commands. As shown in Fig. 3.6, three commands are used for V/T curve selection, while one command is used to disable the V/T control circuit. In the absence of a computer, the commands can be issued manually by switches S5 and S6 across the pulldown resistors R18 and R16. Capacitor C24 serves to debounce the signals from S5 and S6. The D/A converter is formed by the U5 CMOS buffer gates and the binary resistor network of R17 and R15. Since the channel resistance of a saturated CMOS gate is fairly high (100 Ω), R17 and R15 must be at least 10 KΩ to minimize inaccuracies in the D/A converter. Thus R15 is set to 18 KΩ, and

$$R17 = 2(R15) = 2(18K\Omega) = 36\ K\Omega.$$

To obtain the 7% shift between V/T curves 1 and 3, the values for R19 through R22 must be determined. Four resistors are used in this voltage divider so that precision voltage reference levels can be obtained. The D/A converter output tracks the value of V_{VT}, which is nominally 2.5 V. Therefore, nominally

$$R19 + R20 = R21 + R22 = R_D,$$

where R_D is to be determined. It is assumed that curve 1 is selected, and V_{VT} = 2.5 V. Therefore, R15 and R17 are switched to ground by the D/A converter, and the following equation holds:

$$\frac{V_{VT}}{5Vref} = \frac{R15 \parallel R17 \parallel R_D}{R15 \parallel R17 \parallel R_D + R_D},$$

$$\frac{2.5V}{5V} = \frac{18K\Omega \parallel 36K\Omega \parallel R_D}{18K\Omega \parallel 36K\Omega \parallel R_D + R_D}. \tag{3.4}$$

When curve 3 is selected, V_{VT} will be 7% higher, which is $(2.5V)(1.07) = 2.675\ V$. The D/A converter will switch R15 high and R17 low, so the following relation holds:

$$\frac{V_{VT}}{5Vref} = \frac{R17 \parallel R_D}{R17 \parallel R_D + R_D \parallel R15},$$

$$\frac{2.675V}{5V} = \frac{36K\Omega \parallel R_D}{36K\Omega \parallel R_D + R_D \parallel 18K\Omega}. \tag{3.5}$$

The solution of Eqs. (3.4) and (3.5) is R_D = 1.3 KΩ. To eliminate the initial tolerances of R15, R17, and the 5 V reference, the values of R19-22 are adjusted during test.

When the V/T command signal is (1,1), the V/T control circuit is disabled. The MOSFET Q10 saturates, allowing Q11 to be biased on. Therefore, the negative input of U3 is pulled low, forcing the output of U3 to be high. The Q11 base current is controlled by R23, and R50 holds the base voltage near ground when the V/T circuit is enabled. For

protection, a 10 V zener diode is placed across the gate and source of Q10. When the command is (S5,S6) = (0,0) or (1,0), Q10 is biased off, along with Q11. When the command is (0,1), Q10 is biased on, but Q11 cannot be turned on because the drain of Q10 is grounded.

3.4 Small-Signal Modelling

In order to design the charger control loops, it is desirable to simplify the power stage. The input filter (L_{in} and C_{in}) can safely be deleted, assuming that there is no undesired dynamic interaction between the filter and the regulator. Furthermore, since $L_1 \gg L_2$, the output filter can be accurately represented as a single inductor, L_S, whose value is $L_1 + L_2$. As shown in Section 3.5.1, by deriving the duty cycle-to-L_1 current transfer function, it can be shown that C_{out} can be neglected in the charger small-signal analysis.

To facilitate the design of the control loops, the PWM switch model [4] is used to characterize the switching action of the power stage MOSFETs and rectifiers. As shown in Fig. 3.8, the PWM switch model is inserted into the simplified charger power stage. The model's voltage source depends on the steady-state values of D and the voltage between the active and passive terminals. The current source depends on the dc value of I_{BAT}, the current flowing out the common terminal. Since the ESR of the input filter capacitor is so low, the PWM switch parameter r_e is not included. The control signal, v_A, equals $v_c(1+K_2)$, where K_2 is the gain (R_{45} / R_{46}) of the summing amplifier shown in Fig. 3.1.

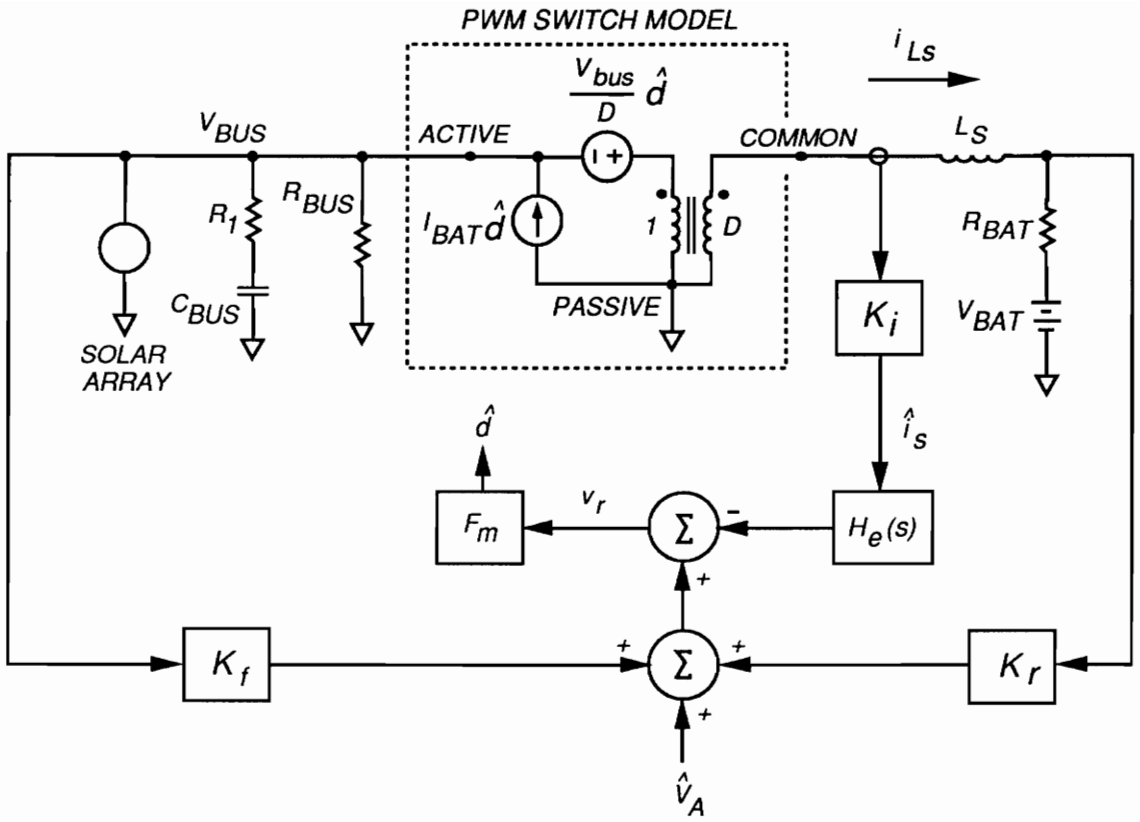


Fig. 3.8. Battery Charger Control Model

Since all three charger control loops use current mode control, it is important to model this control method accurately. The new continuous-time model for current mode control [11] provides a simple and effective method for characterizing this type of sampled-data control. As shown in Fig. 3.8, the sensed current (i_S) is multiplied by the sampling gain, $H_e(s)$. This sampling gain can accurately be modelled as a complex pair of right half plane (RHP) zeros at half the switching frequency:

$$H_e(s) = 1 + \frac{s}{\omega_n Q_Z} + \frac{s^2}{\omega_n^2}, \tag{3.6}$$

where

$$Q_Z = -\frac{2}{\pi},$$

and

$$\omega_n = \pi f_S .$$

The sampled current is added to the control voltage, v_A, along with feedback of the input and output voltages through the gains k_f and k_r. As given in [11] for a buck converter, these feedback gains are

$$k_f = \frac{-D K_i}{L_S f_S}\left(1 - \frac{D}{2}\right), \tag{3.7}$$

and

$$k_r = \frac{K_i}{2 L_S f_S}.$$

As shown in Fig. 3.8, the control signal v_r is multiplied by the comparator gain, F_m:

$$F_m = \frac{f_S}{S_N + S_E}, \tag{3.8}$$

where S_N and S_E are the slopes of the sensed on-time current and the external ramp, respectively.

3.5 Transfer Functions

During the current regulation mode, the bus voltage is controlled by the solar array shunt regulator. Therefore, the bus impedance seen by the charger in this mode is ideally zero. Consequently, the bus capacitor has no effect on the charger transfer functions in the current regulation mode. To design the current regulation feedback loop, it is necessary to find the duty cycle-to-L1 inductor current transfer function, designated as F_{di}. This transfer function changes as the charger moves between CCM and DCM. The boundary between these modes occurs when

$$I_{BAT} = \frac{V_{BAT} D'}{2L_1 f_S}.$$

When V_{BAT} = 84 V, the boundary occurs when I_{BAT} is 2.41 A. When V_{BAT} = 64 V, the boundary increases to I_{BAT} = 2.86 A.

3.5.1 Continuous Conduction Mode

It is shown in this section that the inductor current transfer function can be accurately described as single-order. Using the PWM switch model in Fig. 3.8 and the complete two-stage output filter, the exact duty cycle-to-L_1 current transfer function is derived for CCM:

$$\frac{\hat{i}_{L1}}{\hat{d}} = \frac{V_{BUS}[L_2C_{out}s^2 + C_{out}(R_{BAT} + R_3)s + 1]}{L_1L_2C_{out}s^3 + C_{out}[L_1(R_{BAT} + R_3) + L_2R_3]s^2 + (L_1 + R_{BAT}R_3C_{out} + L_2)s + R_{BAT}}. \quad (3.9)$$

Since $L_1 \gg L_2$, and $R_{BAT} \ll R_3$, Eq. (3.9) can be simplified considerably:

$$\frac{\hat{i}_{L1}}{\hat{d}} = \frac{V_{BUS}}{R_{BAT}} \frac{L_2C_{out}s^2 + C_{out}R_3s + 1}{(L_TC_{out}s^2 + C_{out}R_3s + 1)\left(1 + \frac{sL_S}{R_{BAT}}\right)}, \quad (3.10)$$

where L_T is the parallel combination of L_1 and L_2, and $L_S = L_1 + L_2$. The transfer function given by Eq. (3.10) consists of a pair of complex left half plane (LHP) zeros at $\omega_a = \frac{1}{\sqrt{L_2C_{out}}}$. This transfer function also has a set of complex LHP poles at $\omega_b = \frac{1}{\sqrt{L_TC_{out}}}$. Since L_T is approximately equal to L_2, then ω_a is very close to ω_b. Consequently, the complex pole/zero pairs effectively cancel each other out, and the transfer function becomes

$$\frac{\hat{i}_{L1}}{\hat{d}} = \frac{V_{BUS}}{R_{BAT}}\left(\frac{1}{1 + s\frac{L_S}{R_{BAT}}}\right). \quad (3.11)$$

Since $L_S \approx L_1$, the transfer function, designated as F_{di}, is

$$F_{di} = \frac{\hat{i}_{Ls}}{\hat{d}} \approx \frac{\hat{i}_{L1}}{\hat{d}}.$$

A plot of the exact transfer function, as given by Eq. (3.11), is shown in Fig. 3.9, where the pole/zero cancellation is clearly seen at 10 KHz. This plot accurately reflects the approximated transfer function in Eq. (3.11). The dc gain is V_{BUS} / R_{BAT} which is normally

$$\frac{V_{BUS}}{R_{BAT}} = \frac{(120V)}{(20m\Omega)} = 76\,dB,$$

where R_{BAT} is the total resistance of the battery, L_1, and L_2. The low frequency pole is located at $R_{BAT} / 2\pi L_S$, which is normally

$$\frac{R_{BAT}}{2\pi L_S} = \frac{0.02\Omega}{2\pi(65.5\mu H)} = 49\,Hz.$$

A plot of the approximated transfer function given by Eq. (3.11) is identical to the plot in Fig. 3.9 with the exception of the small resonance at 10 KHz. Since R_{BAT} is very small, the dc gain of F_{di} is very high. Therefore, the steady-state duty cycle is largely independent of the battery current. In other words, as the dc battery current varies, the duty cycle of the charger effectively remains unchanged. Since the resistance of the battery varies widely with its state of charge [7], this dc gain and pole location are also highly variable.

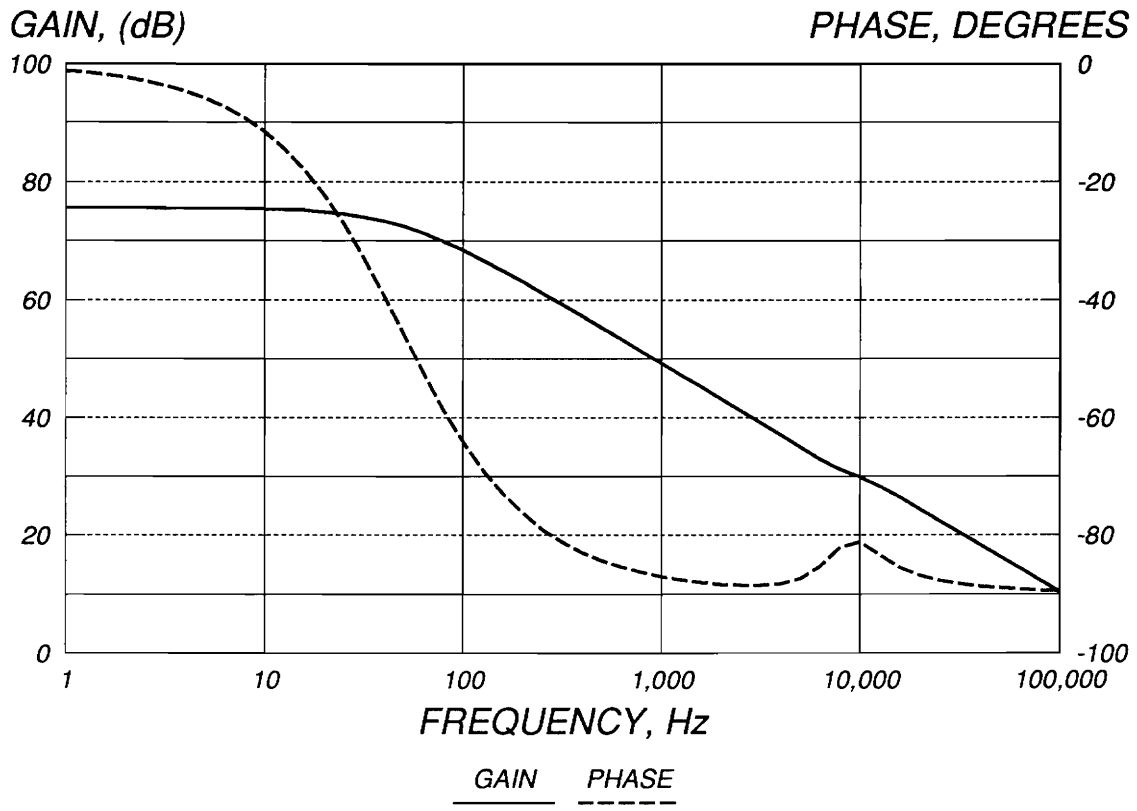


Fig. 3.9. Duty Cycle-to-L1 Current Transfer Function

3.5.2 Discontinuous Conduction Mode

The nature of the duty cycle-to-inductor current transfer function is very different in DCM. The steady-state DCM duty cycle is a strong function of the battery current:

$$D = \sqrt{\left(\frac{1}{M} - 1\right)\frac{I_{Ls}}{2\,L_S\,f_S V_{BUS}}} \quad ,$$

where

$$M = \frac{V_{BAT}}{V_{BUS}} .$$

Since the current in DCM is so low, the voltage drop across the battery resistance is small; thus R_{BAT} can be neglected. Using the DCM model of the PWM switch, the duty cycle-to-inductor current transfer function is derived [14]:

$$F_{di} = \frac{\hat{i}_{Ls}}{\hat{d}} = \frac{2\,I_{Ls}}{D}\left(\frac{1}{1+\frac{s}{\omega_p}}\right),$$

where

$$\omega_p = \frac{(1-M)V_{BAT}}{I_{Ls}\,L_S} .$$

The pole ω_p is located at very high frequencies. As the battery current approaches zero, ω_p tends toward infinity. Since the minimum pole frequency is 25.4 KHz, this transfer function can be treated as a constant gain when the charge current feedback loop is designed. The dc gain of F_{di} is also high: 44 dB at maximum DCM battery current. The dc gain decreases with battery current. However, at a battery trickle charge of 0.25 A, the dc gain is still high: 34 dB.

3.6 Current Feedback Loop

3.6.1 Feedback Loop Design

The design of the current feedback loop is facilitated by the block diagram in Fig. 3.10. This diagram can be simplified by solving for the gain from v_A to i_{Ls}. This gain is denoted as G_f:

$$G_f = \frac{\hat{i}_{Ls}}{\hat{v}_A} = \frac{F_m F_{di}}{1 + T_i},$$

where

$$T_i = F_m F_{di} K_i H_e(s) K_2,$$

and K_2 is the gain of the U1 amplifier that sums the control voltage (v_c) with feedback of the inductor current (i_S). This gain is

$$K_2 = \frac{R45}{R46} = \frac{20K\Omega}{20K\Omega} = 1.$$

At frequencies below 10 KHz, G_f can be greatly simplified since $H_e(s)$ is near unity in this region. Furthermore, since F_{di} is so large, the 1 in the denominator of G_f can be neglected. With these simplifications, G_f is reduced to a constant value of $1/K_iK_2$. Herein lies the value of current mode control for this loop: variations in F_{di} do not affect the loop gain, denoted by T_o in Fig. 3.10. Once G_f is determined, the outer loop gain, $T_O(s)$, is easily solved:

$$T_O = \frac{K_1}{s}(1 + K_2) G_f K_i.$$

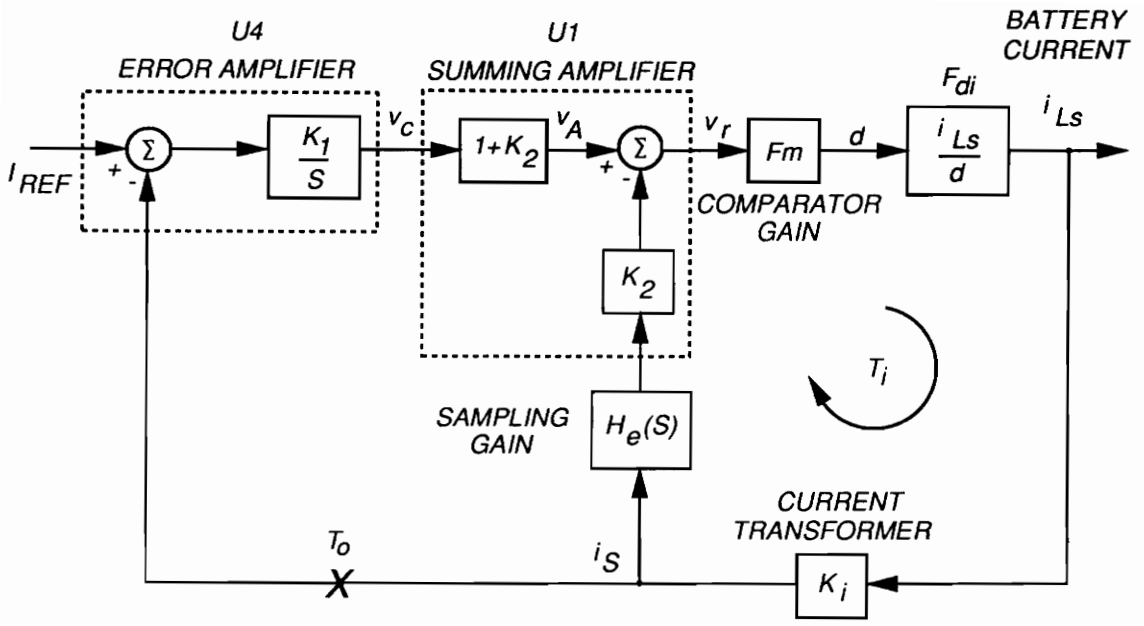


Fig. 3.10. Current Regulation Control System

This loop gain is very simple to compensate due to its first order nature. The loop crossover frequency is determined by K_1, the gain of the integrating error amplifier U4. This gain is K_1 = 1/ (R34)(C20) = 1/ (33 KΩ)(3300 pF). Measured and predicted Bode plots for the current loop in CCM are shown in Fig. 3.11. The current loop gain crosses over at 3 KHz where the phase margin is 83 degrees. The additional phase lag near 10 KHz is due to $H_e(s)$, the sampling gain. The predicted results are obtained from a PSpice model of the charger; this model is presented in the Appendix. As can be seen in Fig. 3.11, the predicted results agree closely with the measurements.

The loop gain is different in DCM due to changes in F_{di}. A measured DCM Bode plot of the outer loop is shown in Fig. 3.12. Because the gain of F_{di} is lower, the loop gain crosses over at a lower frequency: 2KHz. The phase margin remains at 83°.

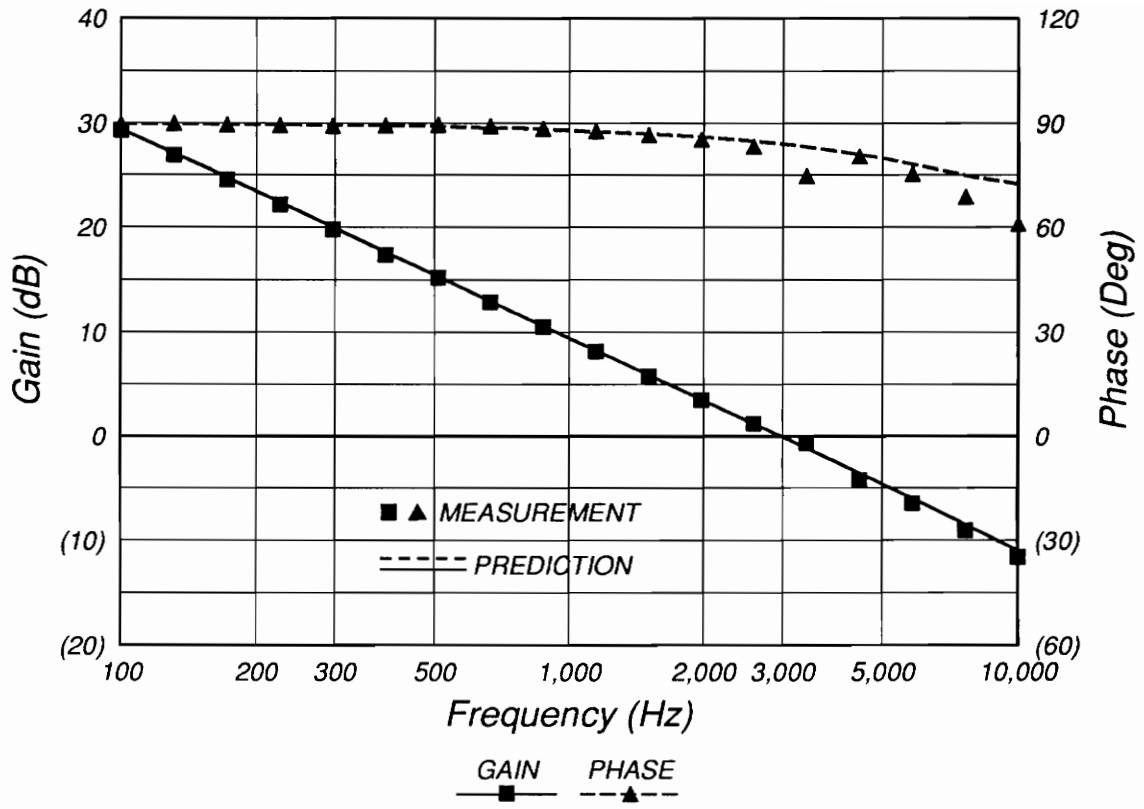


Fig. 3.11. CCM Current Loop (T_o) Bode Plot

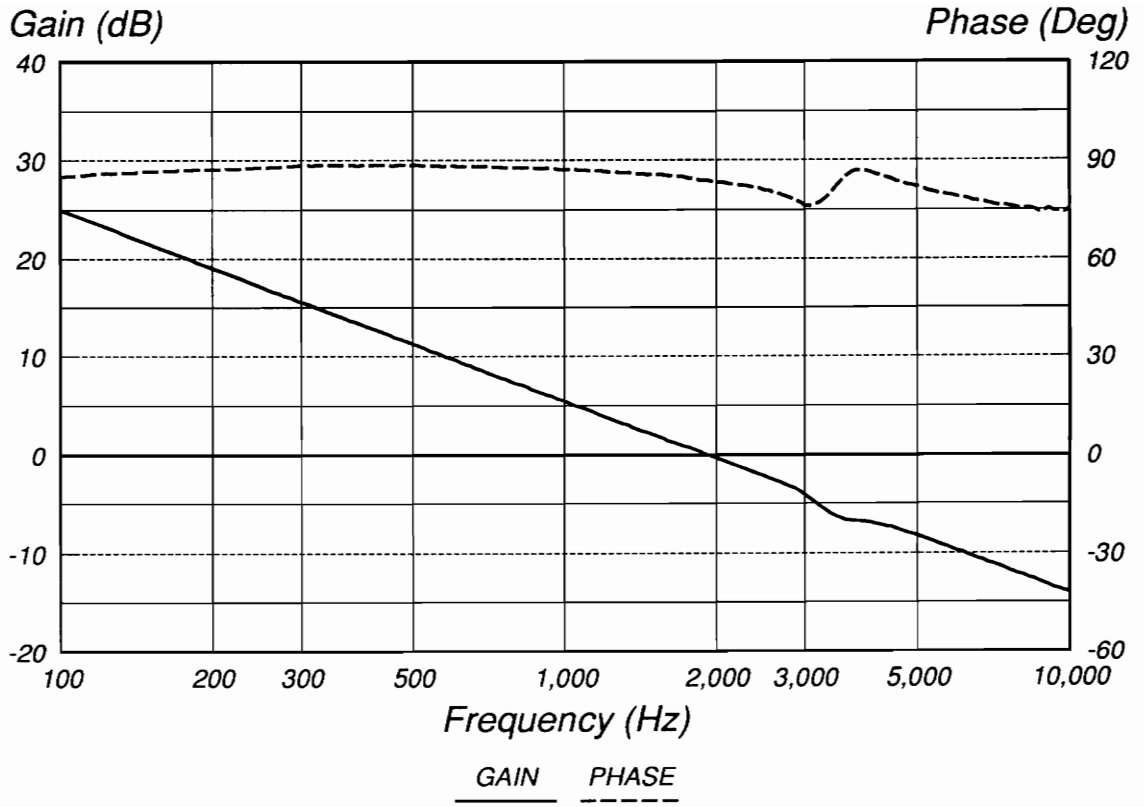
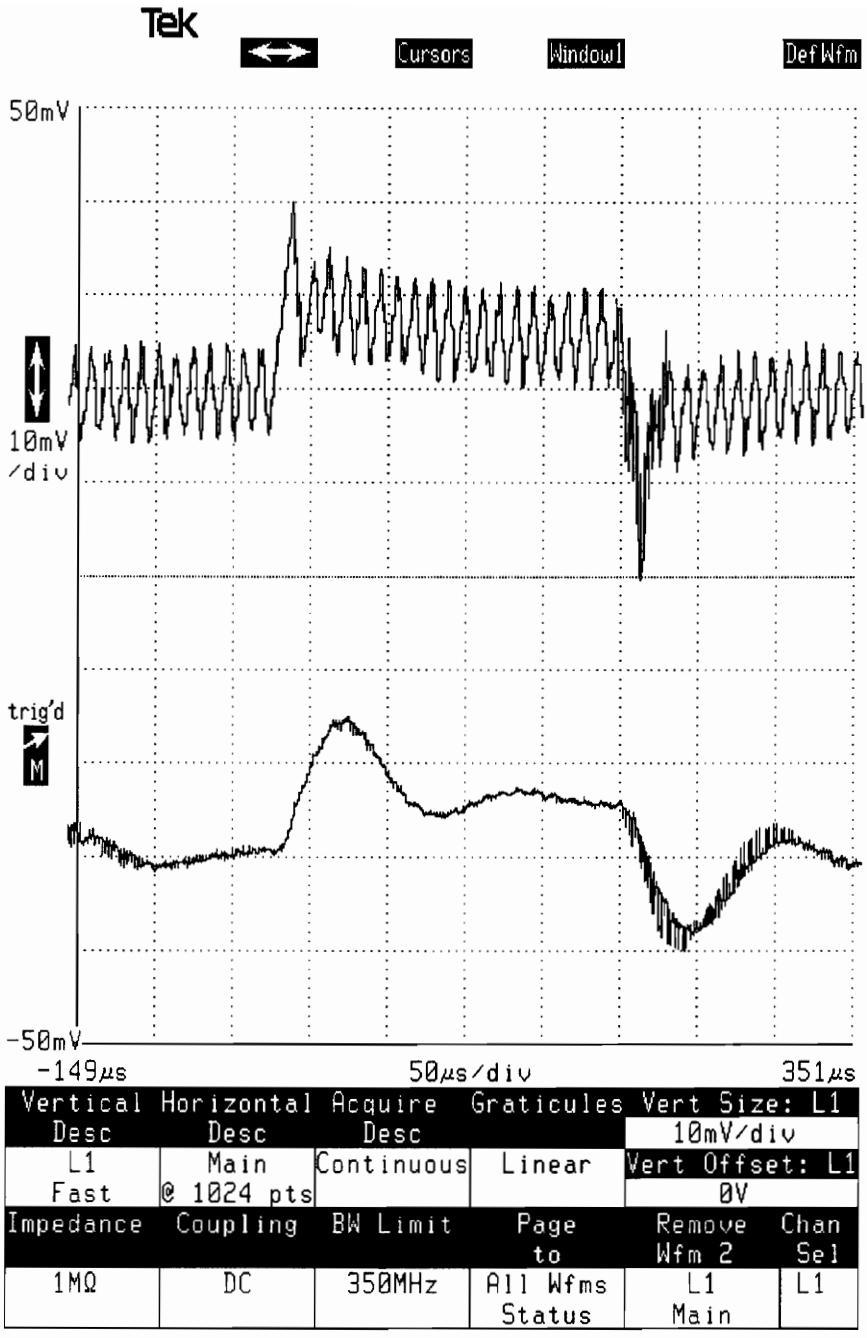


Fig. 3.12. DCM Current Loop (T_o) Bode Plot

3.6.2 Transient Response

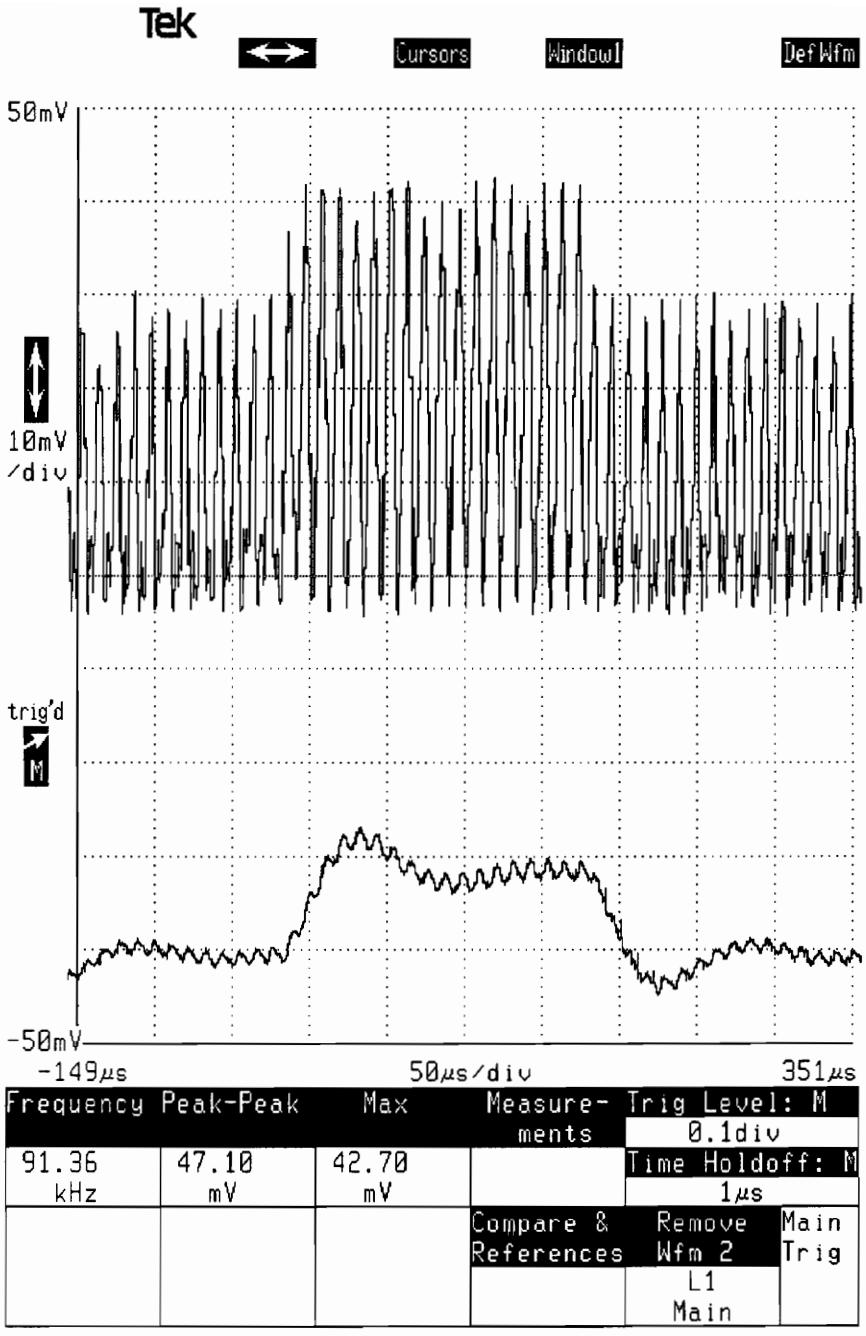
The transient response of the charge current feedback loop is determined by stepping the value of the reference signal, i_{REF}. To do this, a function generator producing a 5 KHz squarewave is connected to the positive input of U4. By adjusting the magnitude of this squarewave, the battery current is programmed. As shown in Fig. 3.13, the reference signal causes the inductor currents, i_{L1} and i_{L2}, to be stepped between 10 and 13 A. At the positive transition, the current in L1 increases rapidly from an average of 10 A since the duty cycle is nearly 100%. The rate of increase is determined by the value of L1 and the bus and battery voltages. After 100 μS, the current in L1 settles to a new average steady-state value of 13 A. Because of the integrating error amplifier, the final steady-state current regulation error is zero [8].

The transient response of the charge current regulation loop in DCM is similar to that in CCM. As shown in Fig. 3.14, the current reference is stepped in a manner to cause the battery current to alternate between 1 and 2 A. The response of i_{L2}, the actual battery current, is very similar to the CCM response in Fig 3.12.



Top: I_{L1} , 5 A/div. Bottom: I_{L2} , 5 A/div.

Fig. 3.13. CCM Current Loop Step Response



Top: I_{L1} , 1 A/div. Bottom: I_{L2} , 1 A/div.

Fig. 3.14. DCM Current Loop Step Response

3.7 Summary

The design of the current regulation mode circuitry has been presented. The design of the charge current and V/T regulation loops was facilitated by use of the PWM switch model and the new continuous-time model for current mode control. The charge current regulation loop uses average current mode control to regulate the average battery current. Current injection control is also implemented by summing the current error signal with the instantaneous inductor current. By doing this, the system loop gain is made insensitive to variations in the duty cycle-to-inductor current transfer function.

The duty cycle-to-inductor current transfer functions were derived for CCM and DCM. Though the charger output filter is third order, it was shown that for the purposes of small-signal analysis, the output filter can accurately be modelled as a single inductor. The CCM transfer function has a very high gain that is inversely proportional to the resistance of the battery. This transfer function also has a low frequency pole that is dependent on the inductor value and the battery resistance. The DCM transfer function has a lower dc gain and a high frequency pole. The gain is proportional to the battery current, whereas the pole varies inversely with current.

The battery current is sensed by a dual current transformer circuit. The current transformers are designed to keep the sensing error less than 1%. The charge current and V/T regulation circuit error signals are ORed with the voltage regulation circuit error signal so that the correct operating mode is automatically selected. The charge current and V/T control circuits are controlled by digital commands, so D/A converters are

designed to produce dc reference signals from a digital input. The charge current is regulated at 16 different rates, and the current errors are verified to be less than 1% for each rate.

4. Voltage Regulation Mode

4.1 Introduction

The Space Platform battery charger assumes the role of regulating the bus voltage during the transition between eclipse and sunlight. By simply controlling the current drawn from the bus, the charger behaves as a shunt regulator, and regulates the bus voltage. As the solar array becomes fully illuminated, the charger's current eventually reaches the level required to charge the battery at the constant commanded rate. At this point, the transition from voltage to current regulation is automatically made by the control circuitry within the charger.

During the bus voltage regulation mode, the battery charger regulates its input voltage; hence, in this mode, the charger behaves as if it were a boost converter, where the battery voltage is the "input," and the bus voltage is the "output" variable. If the positions of the power stage rectifiers and MOSFETs were interchanged, the charger would indeed look like a conventional boost dc/dc converter. This apparent topology transformation produces a boost converter with negative load current since the direction of current flow is into the battery [13,14].

Since the Space Platform power system is to consist of parallel battery charger/discharger modules, current mode control is used in the charger's voltage regulation

loop to ensure equal current sharing among the individual battery chargers. Furthermore, current mode control enhances the performance of the charger voltage loop by minimizing the differences in control characteristics encountered in moving between CCM and DCM [12].

4.2 Bus Voltage Sensing

In the Space Platform, the battery charger is physically located 20 feet from the main spacecraft bus. As shown in Fig. 4.1, there are 20 ft. cables carrying both power and control signals. To accurately simulate the actual spacecraft power system, these long cables were inserted into the hardware setup containing the prototype battery charger. The bus voltage is sensed remotely through a resistive voltage divider contained in the Power Control Unit (PCU). The sensed bus voltage signal is amplified by the non-inverting opamp U10. The gain from the bus voltage to the output of U10 is

$$\frac{\hat{v}_{U10}}{\hat{v}_{BUS}} = \left(\frac{R66}{R66+R65}\right)\left(\frac{R67+R68}{R68}\right).$$

To simplify this gain, R65 is set equal to R67, and R66 is set equal to R68. Thus this gain is unity. R69, the 100 Ω resistor on the output of U10, is used an injection point for small-signal measurements of the voltage loop.

The output signal from U10 is used to drive three amplifiers: U11, 12, and 13. U11 is the error amplifier for the battery discharger, and U12 is the battery charger error amplifier. The solar array switching shunt unit is driven by the U13 amplifier. The volt-

age divider formed by R71-73 is designed to provide a 1 V dead-band between the set-points for the three amplifiers. The compensation for the battery charger voltage loop is provided by U12.

Since the PCU circuitry is located so far from the battery charger, separate ±12 V housekeeping supplies are used. Because of the distance involved, the ground reference of the PCU is not the same in the battery charger. To eliminate the effects of the different grounds, the voltage error signal from the output of U12 in the PCU is sensed differentially by U2 in the charger. As shown in Fig. 4.1, the input to U2 is V_+ - V_-. The output of U2 is

$$V_{U2} = (V_+ - V_-)\left(\frac{R39}{R40(1 + sR39 \times C27)}\right). \tag{4.1}$$

Since R39 = R40 = 10 KΩ, U2 provides unity gain. To filter out high frequency noise, C27 is set to 100 pF, thus providing a 159 KHz low pass filter. To obtain the output indicated in Eq. (4.1), the values of the components in the network formed by R42, R41, and C29 are identical to the values of R39, R40, and C27.

The output signal from U2 is fed to D17, which is part of the diode "OR" network that determines the charger operating mode. The signal v_C at the common anodes is fed to pin 3 of U1, the amplifier that sums in the instantaneous inductor current signal (i_S). To provide noise immunity, R35 is sized low enough to provide a nominal current of 2 mA into the diode "OR" network.

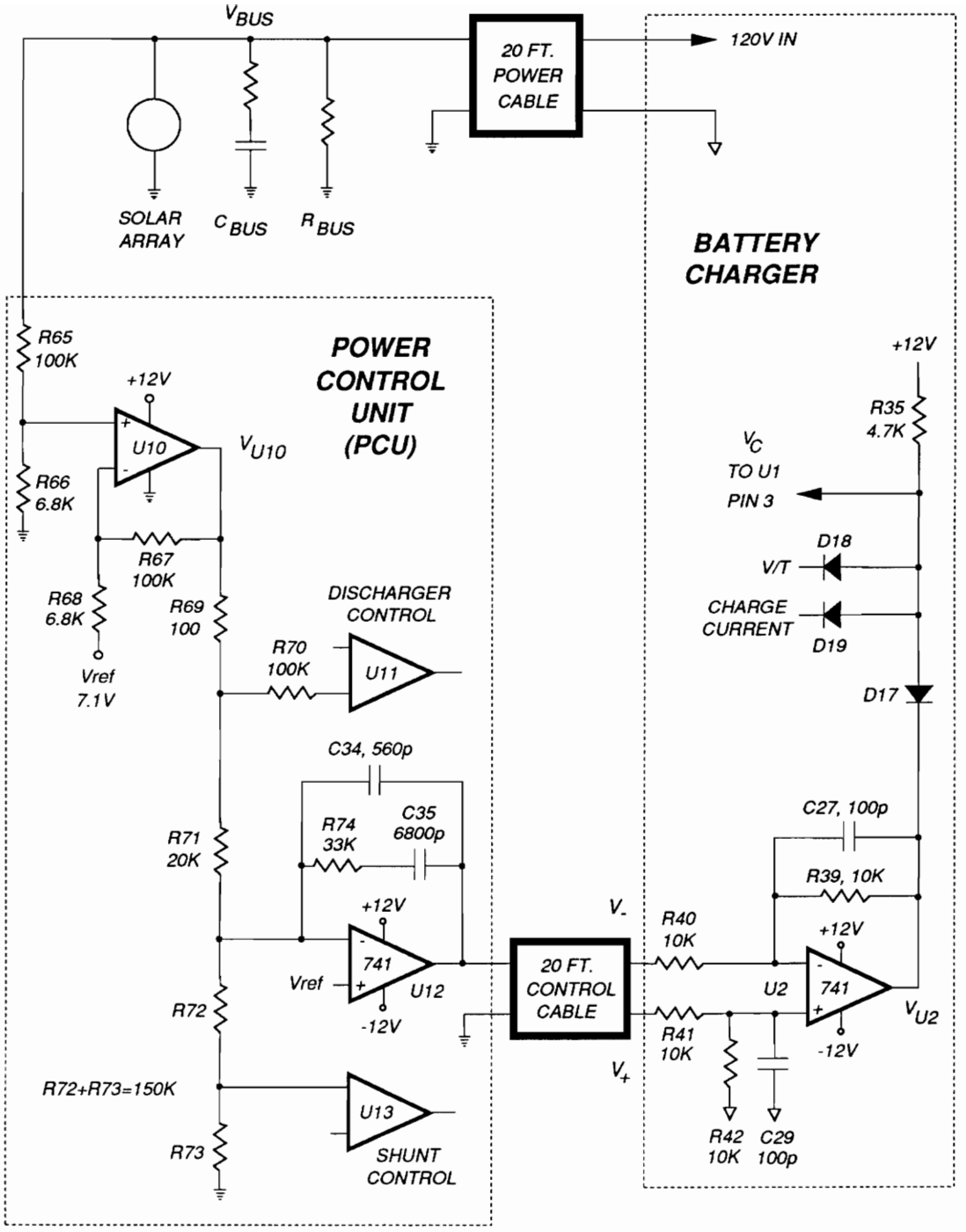


Fig. 4.1. Bus Voltage Sensing and Control

4.3 Open-Loop Transfer Functions

4.3.1 Continuous Conduction Mode

During the bus voltage regulation mode, the solar array appears as a current source; therefore, the bus capacitor and loads enter into the charger transfer functions. The combined resistance of the solar array and all loads connected to the bus is referred to as R_{BUS}. This resistance is referred to as r_{eq} by Kim in [13] and [14]. Since many of the loads on the spacecraft bus are constant-power, the value of R_{BUS} may be negative. However, during the design and testing of the prototype charger described in this thesis, the value of R_{BUS} was always positive. For a detailed analysis of the charger transfer functions with a negative value of R_{BUS}, see [14].

Using the control model in Fig. 3.8, the open-loop power stage transfer functions are derived for the bus voltage regulation mode. The open-loop CCM duty cycle-to-bus voltage transfer function, F_{dv}, is

$$F_{dv} = \frac{\hat{v}_{BUS}}{\hat{d}} = \frac{-V_{BUS}}{D} \frac{\left(1 + \frac{s}{\omega_{Z1}}\right)\left(1 + \frac{s}{\omega_{Z2}}\right)}{\Delta(s)}, \tag{4.2}$$

where

$$\omega_{Z1} = \frac{1}{R_1 C_{BUS}},$$

$$\omega_{Z2} = \frac{V_{BAT}}{I_{Ls} L_S},$$

and

$$\Delta(s) = s^2 \frac{L_S C_{BUS}}{D^2} + s\left[\frac{L_S}{D^2 R_{BUS}} + \left(\frac{R_{BAT}}{D^2} + R_1\right) C_{BUS}\right] + 1 .$$

A plot of this transfer function is shown in Fig. 4.2. Note that the dc gain of F_{dv} is negative: an increase of the duty cycle produces a decrease of the bus voltage. Thus the phase of F_{dv} is 180° at low frequencies. The dc gain is high, usually near 200 (or 46 dB). The zero ω_{Z1} is caused by C_{BUS} and R_1, the bus capacitor and its ESR. The value used for C_{BUS} is 2000 μF. Since R_1 is normally around 40 mΩ, ω_{Z1} occurs at 2.3 KHz. Since the equivalent series inductance (ESL) of C_{BUS} is 40 nH, the resonance of C_{BUS} and its ESL is sufficiently high (190 KHz) to be neglected in the charger small signal analysis. The other zero of F_{dv}, ω_{Z2} , is a function of L_S and the dc values of the battery voltage and current. This zero location is clearly highly variable since it depends on I_{Ls}, the battery current. Since the normal CCM range of I_{Ls} is 2.6 to 23 A, the zero ω_{Z2} varies from 7.8 to 68 KHz for a 74 V battery. The roots of $\Delta(s)$, the characteristic equation, are located at

$$f_\Delta = \frac{D}{2\pi\sqrt{L_S C_{BUS}}},$$

which is 290 Hz for a 74 V battery. The Q of Δ(s) is determined primarily by the battery resistance and the values of C_{BUS} and its ESR. Because of the two zeros, the phase of F_{di} eventually returns to 180°, and the gain attains a zero slope.

The open-loop CCM duty cycle-to-inductor current transfer function, given by F_{di}, is derived:

$$F_{di} = \frac{\hat{i}_{Ls}}{\hat{d}} = (V_{BUS} - D R_{BUS} I_{Ls}) \frac{\left[1 + \frac{s}{\omega_{Z3}}\right]}{\Delta(s)}, \qquad (4.3)$$

where

$$\omega_{Z3} = \frac{V_{BUS} - DR_{BUS}I_{Ls}}{V_{BUS}R_{BUS}C_{BUS}}.$$

A plot of this transfer function is shown in Fig. 4.3. As indicated by Eq. (4.3), depending on the operating conditions, the dc gain of F_{di} may be positive or negative. The low frequency dc gain is moderately high: 26 dB. Note that the location of ω_{Z3} may be either in the LHP or RHP, depending on the polarity of the dc gain. In Fig. 4.3, ω_{Z3} is a RHP zero at 7 Hz. Because the dc gain is negative, the phase starts out at 180°. Because of the RHP zero at 7 Hz, the phase decreases to 90° and eventually reaches -90° because of the complex pole pair in $\Delta(s)$. Since f_Δ is much greater than $\omega_{Z3}/2\pi$, the gain of F_{di} becomes very large in the region of f_Δ.

$$\omega_{Z3} = \frac{V_{BUS} - D R_{BUS} I_{Ls}}{V_{BUS} R_{BUS} C_{BUS}}.$$

A plot of this transfer function is shown in Fig. 4.3. As indicated by Eq. (4.3), depending on the operating conditions, the dc gain of F_{di} may be positive or negative. The low frequency dc gain is moderately high: 26 dB. Note that the location of ω_{Z3} may be either in the LHP or RHP, depending on the polarity of the dc gain. In Fig. 4.3, ω_{Z3} is a RHP zero at 7 Hz. Because the dc gain is negative, the phase starts out at 180°. Because of the RHP zero at 7 Hz, the phase decreases to 90° and eventually reaches -90° because of the complex pole pair in $\Delta(s)$. Since f_Δ is much greater than $\omega_{Z3}/2\pi$, the gain of F_{di} becomes very large in the region of f_Δ.

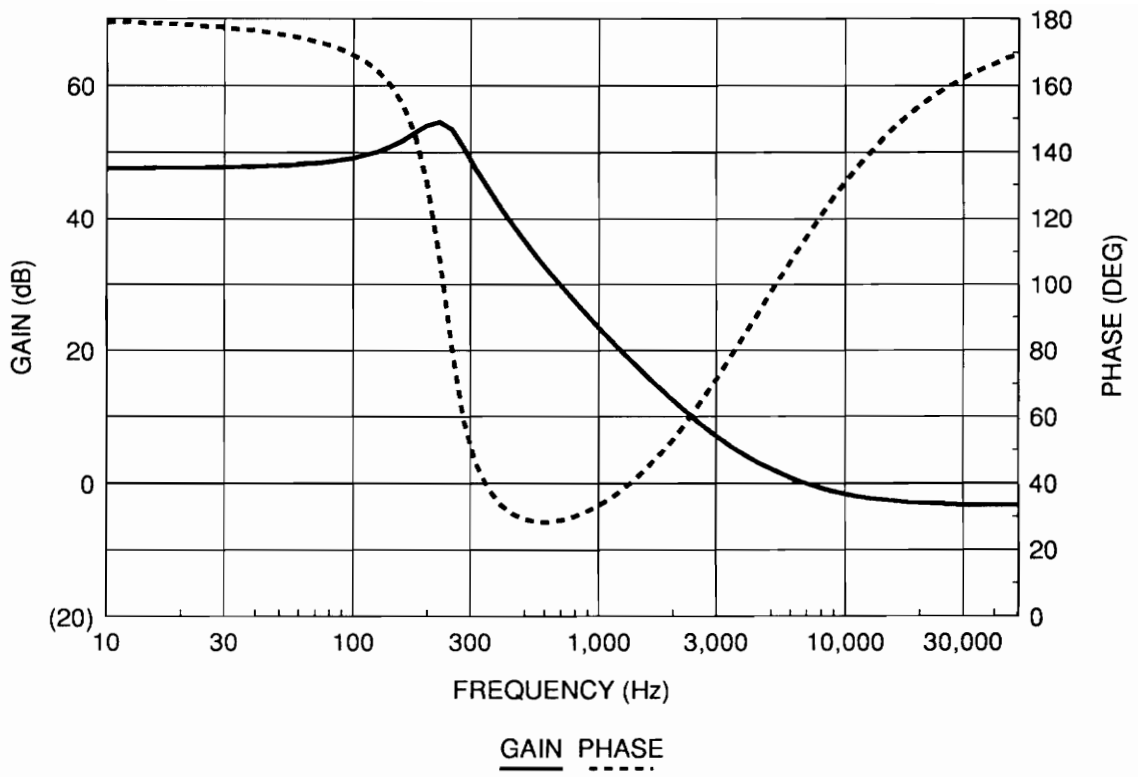


Fig. 4.2. Open-Loop CCM Duty Cycle-to-Bus Voltage Transfer Function

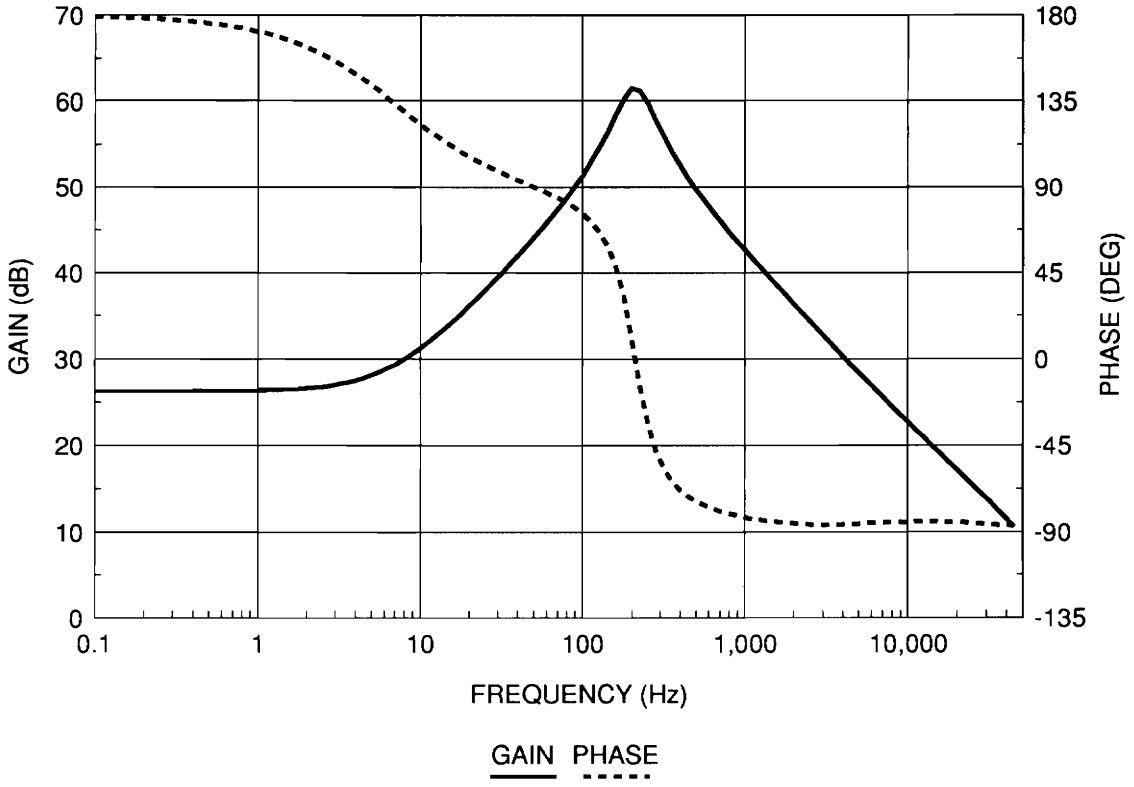


Fig. 4.3. Open-Loop CCM Duty Cycle-to-Inductor Current Transfer Function

4.3.2 Discontinuous Conduction Mode

As shown in [10] for DCM, the effects of current feedback are not present in the converter small-signal model. Therefore, the duty cycle-to-inductor current transfer function is not derived. Using the DCM model for the PWM switch, the open-loop DCM duty cycle-to-bus voltage transfer function is derived in [14]:

$$\frac{\hat{v}_{BUS}}{\hat{d}} = G_d \frac{\left(1+\frac{s}{\omega_Z}\right)(1+sR_1C_{BUS})}{\left(1+\frac{s}{\omega_{P1}}\right)\left(1+\frac{s}{\omega_{P2}}\right)}, \tag{4.4}$$

where, with some approximations,

$$G_d = \frac{-2V_{BUS}}{DR}\{R_{BUS} \parallel R(1-M)\},$$

$$R = \frac{V_{BUS}}{MI_{Ls}},$$

$$\omega_Z = \frac{RM^2(1-M)}{L_S(1-M+2M^2)},$$

$$\omega_{P1} = \frac{1}{C_{BUS}\{R_{BUS} \parallel R(1-M)\}},$$

$$\omega_{P2} = \frac{R(1-M)}{L_S}.$$

Both ω_Z and ω_{P2} are located at very high frequencies (above 30 KHz). Therefore, this zero and pole do not impact the design of the voltage feedback loop. The dominant pole of this transfer function is ω_{P1}, which occurs at low frequencies (around 1 Hz).

4.4 Feedback Loop Design

The design of the voltage feedback loop is shown in Fig. 4.4. The system output, the bus voltage, is sensed through the divider ratio, K_4. Since F_{dv}, the duty cycle-to-bus voltage transfer function, has a negative dc gain, positive feedback of v_{BUS} is necessary to obtain a stable system. The voltage error signal is amplified by the integrating error amplifier U12. The resulting control signal, v_c, is summed with negative feedback of the inductor current (i_{Ls}). The resulting signal, v_r, is compared against the external ramp to generate the duty cycle (d).

The control loop design begins with T_i, the gain of the current loop. This gain is easily found:

$$T_i = F_m F_{di} K_i H_e(s) K_2 .$$

The closed-loop control-to-bus voltage transfer function, F_v, is

$$F_v = \frac{\hat{v}_{BUS}}{\hat{v}_c} = \frac{(1+K_2)F_m F_{dv}}{1+T_i - F_m F_{dv} K_f K_2} .$$

As demonstrated in [14], with certain approximations, F_v in CCM can be greatly simplified:

$$F_v = G_x \frac{\left(1+\frac{s}{\omega_{z1}}\right)\left(1+\frac{s}{\omega_{z2}}\right)}{\left(1+\frac{s}{\omega_x}\right)\left(1+\frac{s}{\omega_n Q_p}+\frac{s^2}{\omega_n^2}\right)}, \tag{4.5}$$

where

$$G_x = \frac{-F_m V_{BUS}}{D(1+G_i)+K_f F_m V_{BUS}},$$

$$G_i = \frac{\left(\frac{V_{BUS}}{R_{BUS}} - D I_{Ls}\right)}{D^2} F_m K_i,$$

$$Q_p = \frac{1}{\pi(m_c D' - 0.5)},$$

$$m_c = 1 + \frac{S_E}{S_N}.$$

The dominant pole of F_v is ω_x which, with some approximations, can be shown to be equal to ω_{Z3} , the zero in the duty cycle-to-inductor current transfer function (F_{di}). Both ω_x and ω_{Z3} are located at low frequencies (<10 Hz), and both vary directly with the battery current. Under some conditions, the Space Platform consists largely of constant power loads, so R_{BUS} has a negative value. This causes ω_{Z3} to be a RHP zero, which in turn causes ω_x to be a RHP pole. It can be shown through a Nyquist plot that the voltage loop can be stable in the presence of this RHP pole if the loop gain is high enough [14]. The second order polynomial in the characteristic equation for F_v is resonant at half the charger switching frequency. If the external ramp is properly selected, the value of Q_p, the resonant damping factor, will be near unity. In this case, these complex resonant poles will have little effect on the charger dynamic behavior.

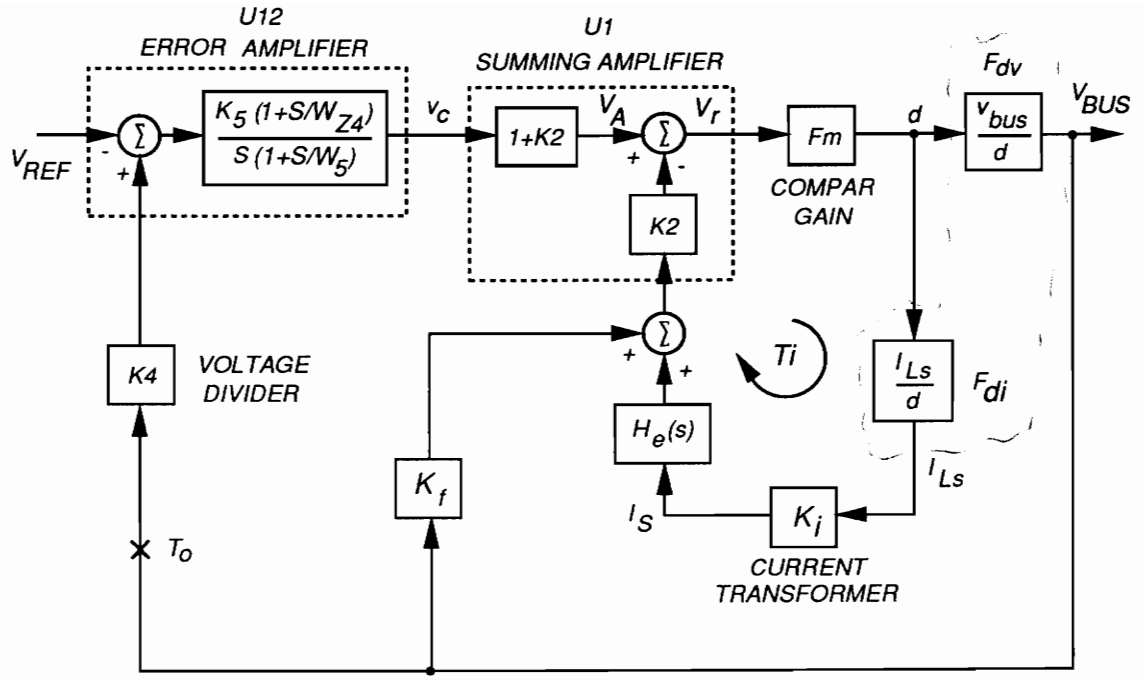


Fig. 4.4. Voltage Regulation Control System

The closed-loop control-to-bus voltage transfer function for DCM is derived in [14]:

$$F_{v,DCM} = \frac{\hat{v}_{BUS}}{\hat{d}} = F_m G_c \frac{\left(1+\frac{s}{\omega_Z}\right)(1+sR_1C_{BUS})}{\left(1+\frac{s}{\omega_{C1}}\right)\left(1+\frac{s}{\omega_{C2}}\right)}, \tag{4.6}$$

where

$$G_c = \frac{G_d}{1-K_f F_m G_d} < G_d,$$

$$|\omega_{C1}| < |\omega_{P1}|.$$

G_d is the dc gain and ω_{P1} is the dominant pole of the open-loop DCM duty cycle-to-bus voltage transfer function defined in Eq. (4.4). The closed-loop DCM control-to-bus voltage transfer function has a slightly lower dc gain and dominant pole. Since the value of K_f is normally very small, the following approximations can be made: $G_c = G_d$, and $\omega_{c1} = \omega_{P1}$.

The gain of the outer voltage loop (T_o) is

$$G_{vl} = F_v K_4 \frac{K_5\left(1+\frac{s}{\omega_{Z4}}\right)}{s\left(1+\frac{s}{\omega_5}\right)}. \tag{4.7}$$

To compensate this voltage loop, the error amplifier must be properly designed. The compensator pole, ω_5, is set at 9 KHz to attenuate the 90 KHz switching ripple. The dc gain, K_5, is designed to give a maximum loop gain crossover near 3 KHz so that the bus impedance can be minimized. This crossover frequency must not be pushed out to far since this would decrease the loop attenuation of the 90 KHz switching ripple. Since ω_{Z2}, a zero of F_{dv}, is inversely proportional to the battery current, care must be taken to

compensate for the movement of this zero. At minimum battery current, ω_{Z2} moves to a high frequency, so the compensating zero, ω_{Z4}, is placed low enough (700 Hz) to provide adequate phase margin. Placement of ω_{Z4} must not be too low, since this slows the speed of the voltage loop. Measured and predicted Bode plots for the voltage loop in CCM are shown in Fig. 4.5. The measured and predicted results agree well except for a difference in phase at higher frequencies. The loop gain crosses over at 2.1 KHz where the phase margin is 81 degrees. (For this plot, the battery voltage and current were 60 V and 11.5 A.)

Fig. 4.6 shows a Bode plot of the voltage loop in DCM obtained from a PSpice simulation. The PSpice charger circuit used the DCM model of the PWM switch [4]. As expected, the gain is lower, resulting in a lower crossover at 700 Hz where the phase margin is 50°. (For this plot, the battery voltage and current were 75 V and 1.2 A.) Superimposed on this plot are measured data points taken under the same conditions. The agreement between prediction and measurement is very good except for a divergence in the phase above 3 KHz. Measurement below 10 Hz was not possible because of test equipment limitations. Were it possible to measure the loop gain down to 0.01 Hz, the low frequency pole of the 741 op-amp would be apparent. The gain of the op-amp used in the PSpice simulation was high enough that the its low frequency pole was below 0.01 Hz. As Fig. 4.6 shows, the pole ω_x occurs at 0.4 Hz. The value of R_{BUS} in this case is positive, therefore, ω_x is located in the LHP where it causes -90° phase shift.

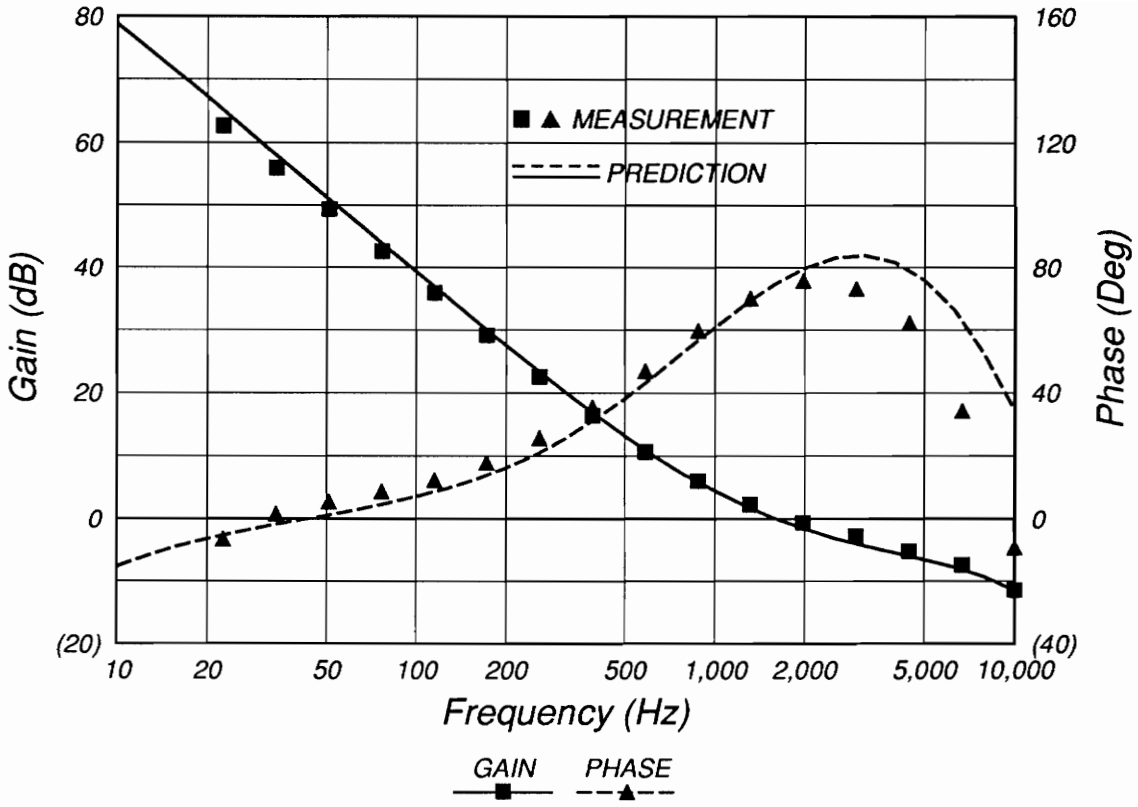


Fig. 4.5. Bode Plot of Voltage Loop (T_o) in CCM

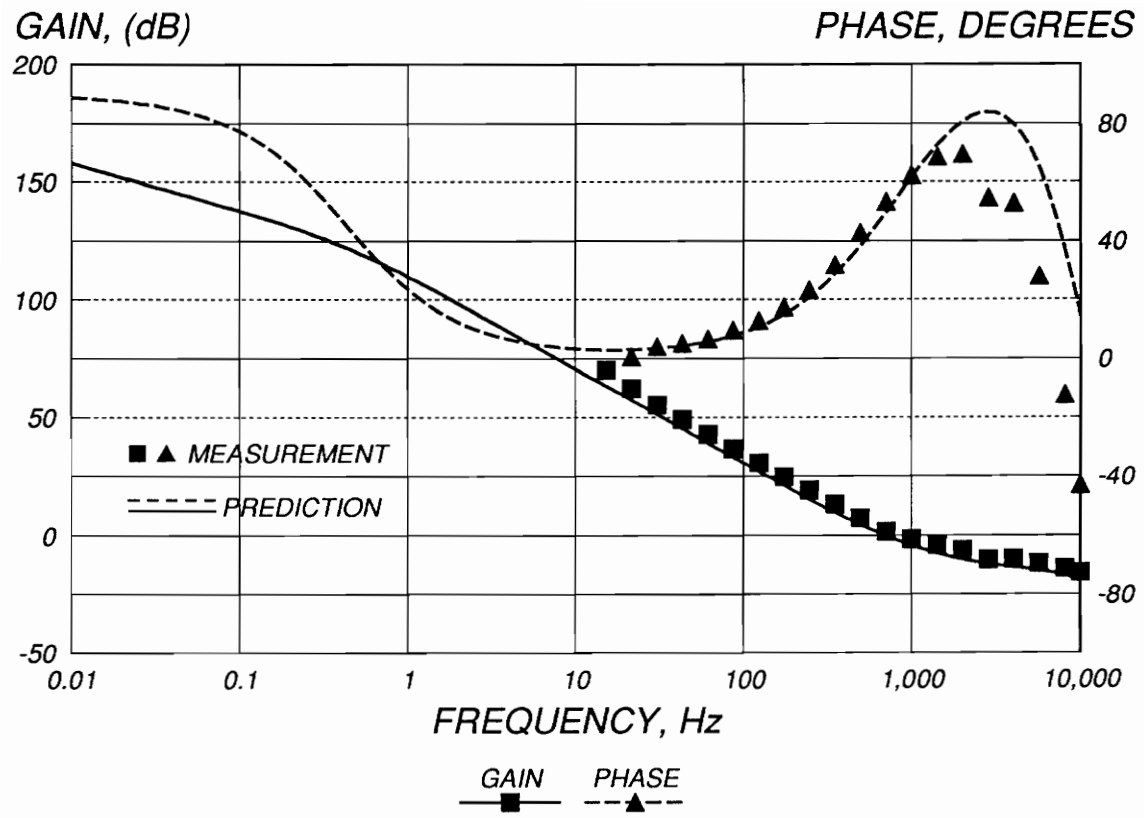


Fig. 4.6. Bode Plot of Voltage Loop (T_o) in DCM

4.5 Performance

To test the performance of the charger while it is in the bus voltage regulation mode, it was necessary to use a solar array simulator. For all tests on this prototype charger, a simple current source was used to simulate the solar array. The current source consisted of four parallel IRFP250 MOSFETs which were operated with a common gate-to-source bias voltage. The MOSFET current output was controlled by the manual adjustment of the dc gate bias voltage. The MOSFET drains were connected to a power supply producing a regulated voltage greater than 125 V. The MOSFET sources were directly connected to the 120 V bus in the test hardware setup.

To test the transient response of the voltage loop, the bus load current was stepped between two levels. As shown in Fig. 4.7, the bus load current was stepped between 5 and 10 A by driving a Dynaload which was in the external modulation mode. Since the Dynaload was operated as an active current source, the value of R_{BUS} was positive for this test. After a 75 mV overshoot lasting 1 mS, the charger maintains regulation of the bus voltage. To test the transient response in DCM, the bus load current was stepped between 0.5 and 1 A. For each condition of bus load current, the charger was in DCM. The resulting bus voltage transient is shown in Fig. 4.8. The voltage overshoot is 50 mV, and the transient lasts for 1 mS. The transient duration is a function of the location of the compensation zero, ω_{Z4}, which is 700 Hz.

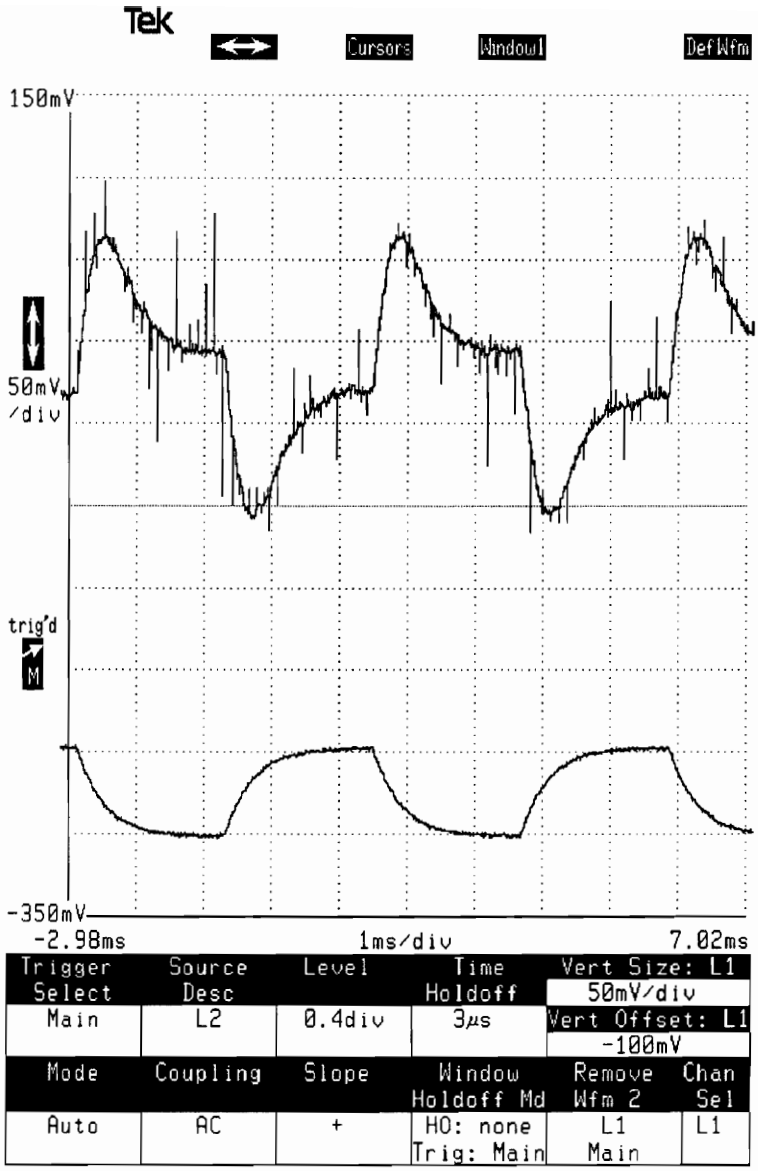
In order to provide a fast transient response with a low overshoot, the charger must have a low output impedance. This is also referred to as the bus impedance, since the charger regulates the bus voltage. Measured and predicted plots of the bus impedance in

CCM are shown in Fig. 4.9. The theoretical and measured results agree very closely. The bus impedance is low at lower frequencies because the feedback loop gain is high [9]. In the vicinity of the loop gain crossover point, the impedance reaches a maximum around 60 mΩ. The impedance then falls at a rate determined by the bus capacitance. The impedance eventually levels off at the value (40 mΩ) of the bus capacitor ESR. The DCM bus impedance is shown in Fig. 4.10. The DCM and CCM bus impedance curves are identical above 3 KHz since the feedback loop gain in each case is below unity. At lower frequencies, the DCM bus impedance is 9 dB higher than the CCM impedance since the feedback loop gain is that much lower.

The charger was also tested to determine its level of conducted emissions during the bus voltage regulation mode. To obtain the worst case conditions, this test was conducted under maximum charger current. The bus ac voltage was measured by sensing the ac current through the bus load resistance. This current was converted to voltage and then fed to a spectrum analyzer. The power spectrum of the charger's conducted emissions is shown in Fig. 4.11. The following formula is used to convert the results in Fig. 4.11 from dBmW to Vrms:

$$\text{Vrms} = 2.24 R_{BUS} \sqrt{10^{dBmW \times (0.1)}} .$$

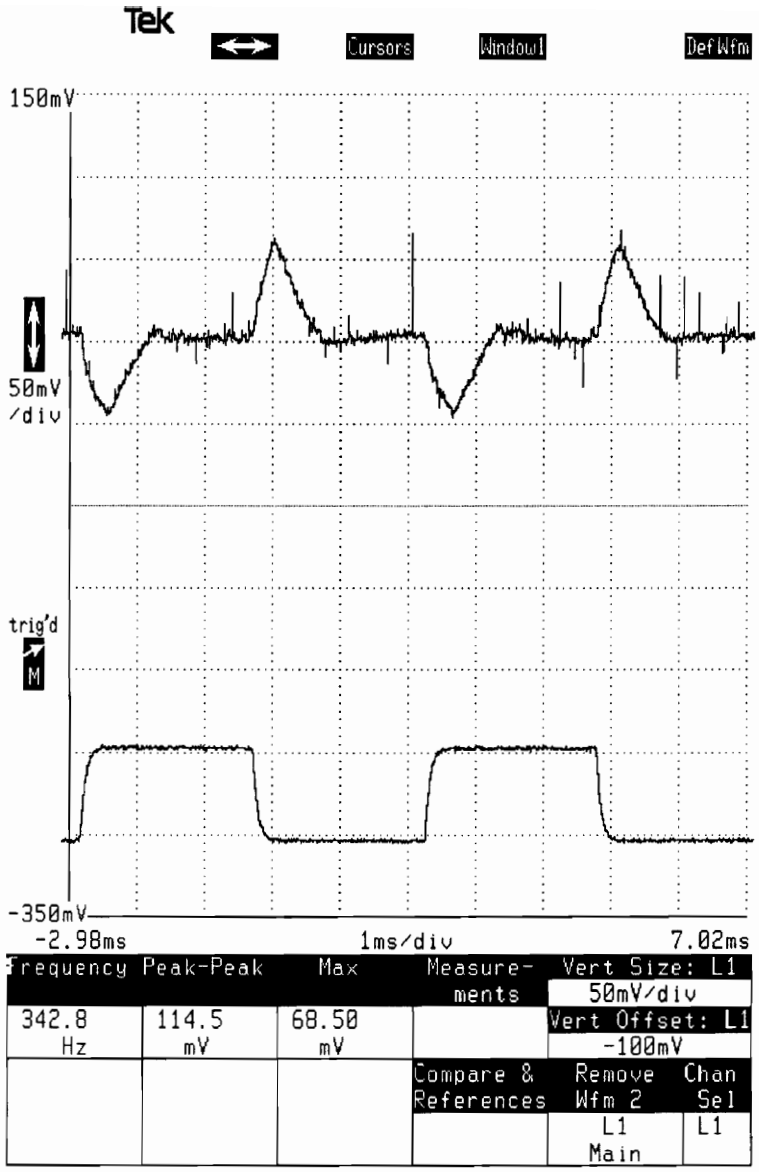
The peak current obviously occurs at the fundamental switching frequency (91.3 KHz) of the charger. At this frequency, the bus voltage ripple is found to be 35 mV p-p through the conversion formula. This level is well below the 200 mV p-p bus ripple specification. As can be seen in the spectrum, there are also numerous other peaks in the measurement. These are due to the 17 KHz switching components from the power supply used to simulate the solar array.



Top: Bus voltage transient, 50 mV/div, ac coupled

Bottom: Bus load current transient, 5 A/div

Fig. 4.7. Voltage Loop CCM Transient Response



Top: Bus voltage transient, 50 mV/div, ac coupled

Bottom: Bus load current transient, 0.5 A/div

Fig. 4.8. Voltage Loop DCM Transient Response

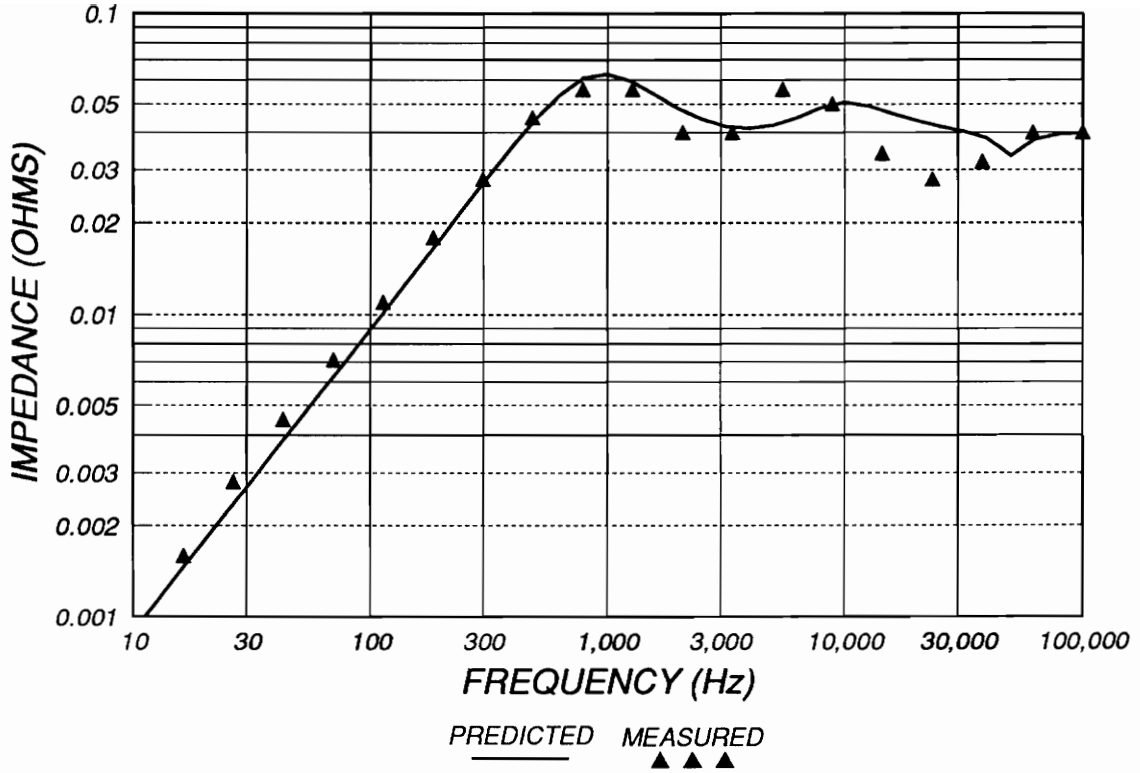


Fig. 4.9. CCM Bus Impedance

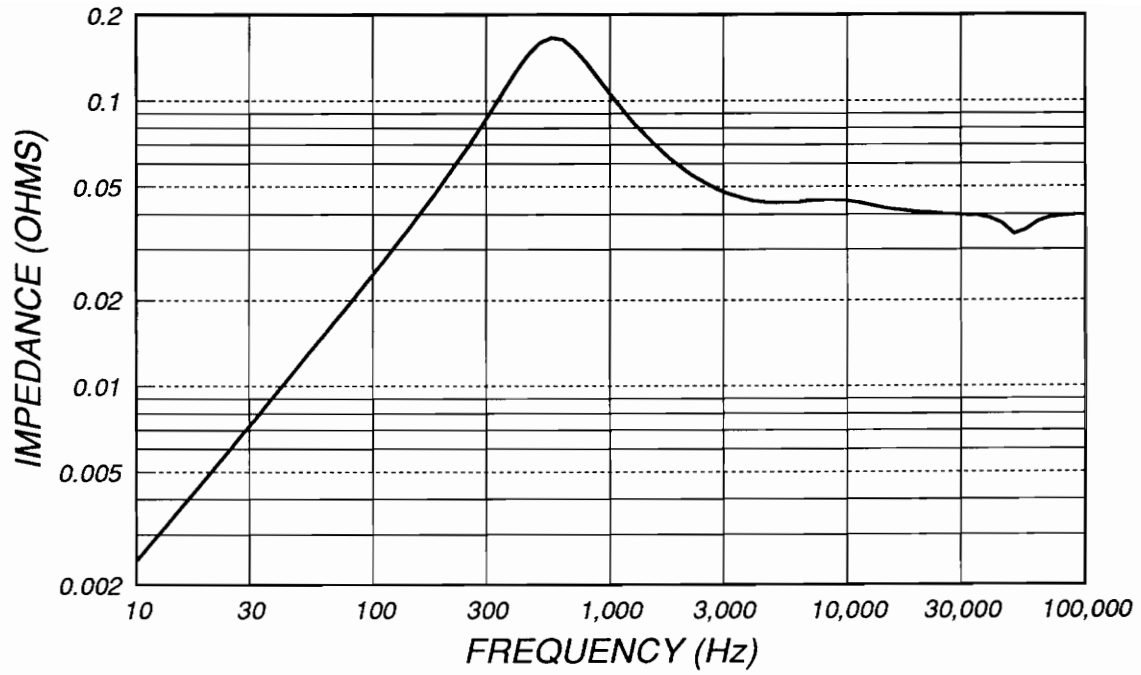


Fig. 4.10. DCM Bus Impedance

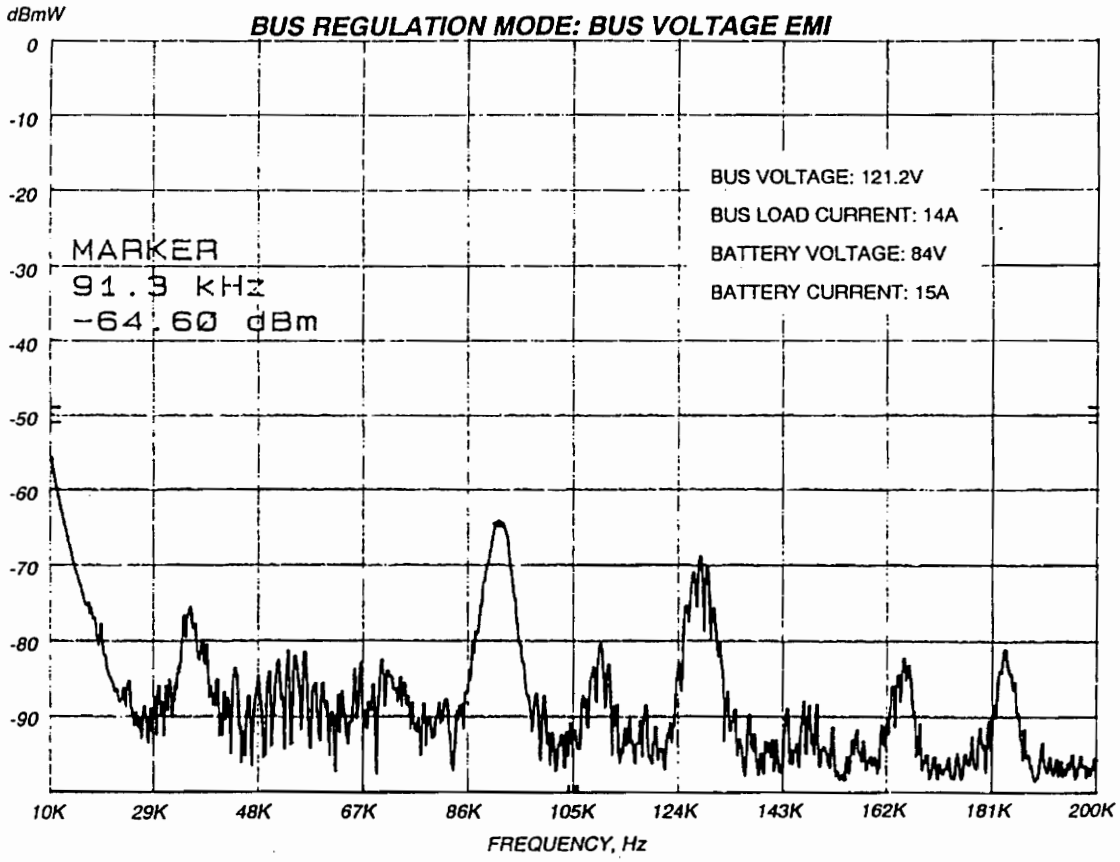


Fig. 4.11. Conducted Emission Measurement

4.6 Summary

The design of the bus voltage regulation circuitry has been presented. To improve the charger performance and to enable current sharing between battery ORUs, current mode control is implemented. The transfer functions from the duty cycle to the bus voltage and the inductor current were discussed for CCM and DCM. The predicted results agree well with the measurements of the voltage loop gain and bus impedance. The transient response measurements indicate a fast and stable bus voltage regulation loop. The conducted emission measurement verifies that the EMI from the charger is within specification.

5. Conclusions

A prototype battery charger for the NASA EOS Space Platform has been designed, built, and tested. The results from this thesis along with work on the battery discharger will be useful in the actual design of the Space Platform power system.

The design of the charger power stage was driven by mass and efficiency constraints. The nominal efficiency achieved for the charger is 96%, and the power stage mass is 309 g. The mass was minimized by the use of a high power conversion frequency (90 KHz) and the use of a Metglas core for the main energy storage inductor. The efficiency was boosted by the paralleling of four power MOSFETs and the maximum usage of the winding area of the filter inductors. A unique gate drive circuit was designed to simultaneously switch the four power MOSFETs. To reduce the battery current ripple below 1% (230 mA), a two-stage output filter was designed. The input and output filters were carefully damped to obtain a low Q.

Several useful design tools were employed in the modelling and design of the battery charger. The PWM switch model was instrumental in deriving the charger transfer functions and in designing the feedback loops. The new continuous-time model for current-mode control was also used to obtain accurate results in the feedback loop design. The validity of these design tools was demonstrated by the comparison of measurements to the model predictions. In most cases the agreement was very close.

Since the Space Platform power system consists of parallel battery modules, the charger must be designed in a manner to allow module current sharing. Therefore, all charger control loops are designed with current-mode control. The charger performance is also enhanced by current-mode control since instantaneous current limiting is inherently provided, and the differences in charger behavior between CCM and DCM are minimized.

To regulate the dc battery current, average current-mode control is used. A dual current transformer circuit is used to accurately sense the battery current, and the sensing error is less than 1% (230 mA). Both the charge current and the V/T control circuits are designed to be operated by digital command. Since the control-to-inductor current transfer function is effectively single-order in the current regulation mode, the design of the feedback loop is straightforward. The system loop gain crosses over at 3 KHz where there is a large phase margin (83°). Measurements indicate a fast (100 μS) and stable transient response.

One of the more interesting aspects of the charger design is the bus voltage regulation. The charger is designed to sense and regulate the bus voltage during the transition between eclipse and sunlight. In this mode, the charger dynamics are effectively transformed from a buck to a boost converter. The control-to-inductor current transfer function is unique in that the polarity of the dc gain is dependent upon the charger dc operating conditions. For example, when the bus load resistance (R_{BUS}) varies from a large to a small value, the dc gain of this transfer function changes from negative to positive. Furthermore, when the dc gain reverses sign, the low frequency pole of this transfer function moves between the LHP and RHP. The closed-loop transfer functions are complex, but they can be simplified considerably. The control-to-bus voltage transfer

function has a low frequency pole which corresponds to the dominant pole of the control-to-inductor transfer function. The transfer functions are different between CCM and DCM. However, the closed loop DCM and CCM control-to-bus voltage transfer functions are very similar due to the effect of current-mode control.

The voltage loop design is presented, and the gain typically crosses over at 2 KHz where the phase margin is 75°. The loop bandwidth varies because of a zero that is dependent on the battery current. The charger output impedance is measured and compared against a prediction from a PSpice model. The agreement is close, and the peak impedance is 60 mΩ, occuring at 1 KHz. The low output impedance corresponds to a fast voltage loop transient response. Measurements indicate a fast response with minimal overshoot when the bus load current is stepped. As the conducted emissions measurements reveal, the EMI from the charger is well within specification.

Appendix A - PSpice Modeling

The PSpice circuit models used to generate the transfer functions, Bode plots, and impedance plots for the battery charger are presented in this appendix for CCM and DCM. These small-signal models give accurate results out to one half the charger switching frequency. For simplicity, the dc sources including the battery are shorted out. The comparator gain and the parameters in the PWM switch model are adjusted depending on the dc operating conditions of the charger. In the CCM PWM switch model, the dc transformer is formed by the dependent sources FT and ET. The gain of these two sources is D, the steady-state duty cycle. The source ESUM is dependent on the charger input and output voltages through the gains K_f and K_r. The impedance of the 20 ft. power cable is modelled by LCAB and RCAB. The output impedance of the battery discharger is modelled by CDAN and RDAN.

The CCM PSpice circuit model and listing are presented in Fig. A.1 and Table A.1. Similarly, the DCM PSpice circuit model and listing are presented in Fig. A.2 and Table A.2. If analysis of the current regulation mode is needed, then the summing amplifier E3823 is made dependent on the voltage at node 26. The bus capacitor and load must be removed, so node 1 is grounded. The inductor current is sensed by HCS through the 0 V dc source VET. The current error signal is amplified by EIR. To measure the current loop gain, an ac voltage is injected by VACI through the coupling capacitor CY. This capacitor value is large enough so that the loop measurement is not affected. To close the loop, inductor LY is used. The value of this inductor is large enough to effectively open the loop in the span of frequencies needed for analysis.

If analysis of the voltage regulation mode is needed, then the summing amplifier E3823 is made dependent on the voltage at node 37. The bus voltage is sensed by EVS, and the voltage error signal is amplified by EVR. The attenuation of the differential amplifier (U2) is provided by RDA and CDA. A similar signal injection method for measurement of the voltage loop is used.

To model the sampling gain, $H_e(s)$, the source EHI and its feedback network are used [10]. The values of RS2, CS2, LS, and CS1 are calculated to give a pair of LHP complex zeros at one half the charger switching frequency:

$$CS2 = LS = CS1 = \frac{1}{\pi f_S},$$

and

$$RS2 = \frac{-\pi}{2}.$$

The sampled current feedback signal at node 22 is added to either the voltage or current error signal by the dependent source E3823.

In DCM, the current sampling has no effect, so the $H_e(s)$ circuit model is deleted. To simplify the model, the E3823 summing amplifier is deleted. To compensate for this, the dependent gain of the source ESUM is adjusted for either the voltage or current loop.

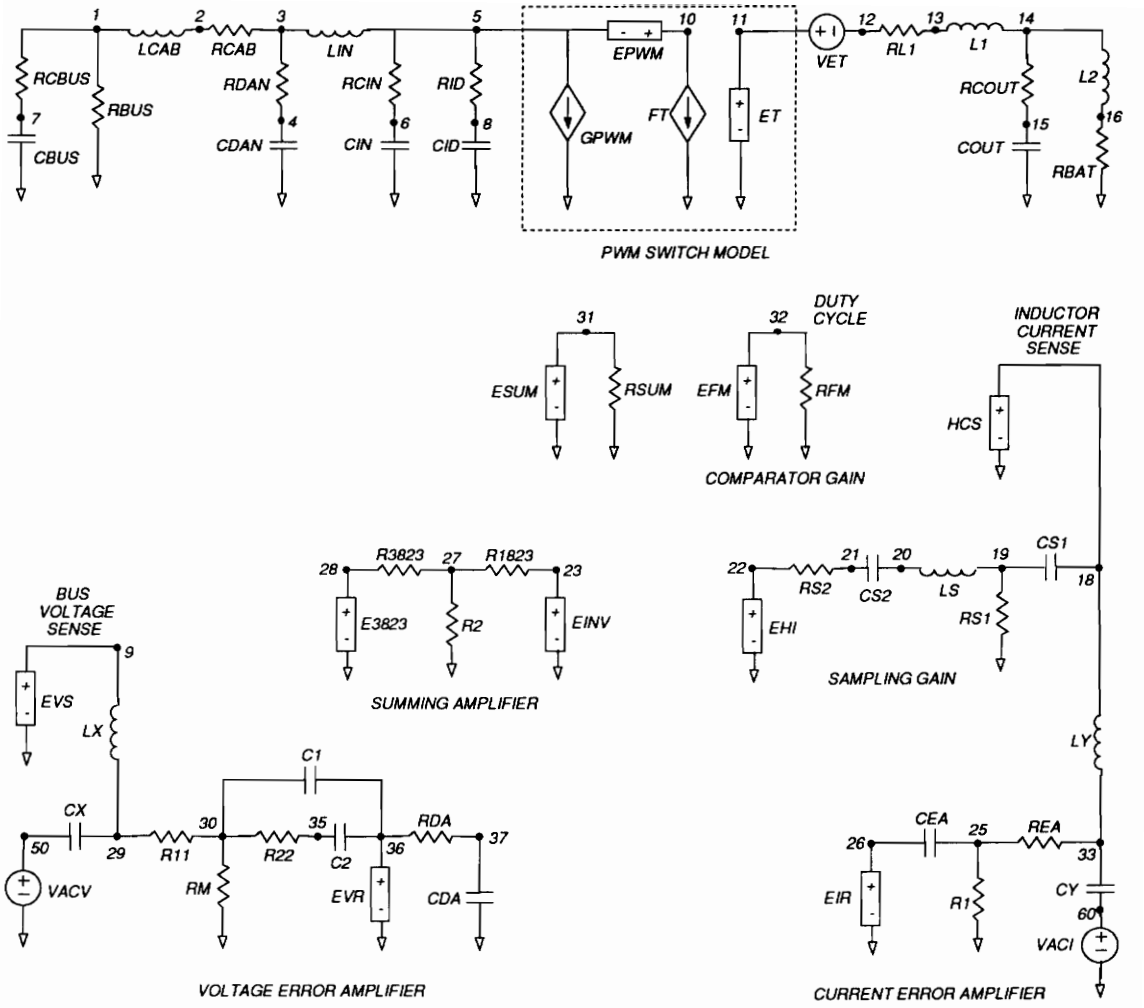


Fig. A.1. PSpice CCM Model Circuit

Table A.1. PSpice CCM Model Listing

```
*          BUS INPUT
RBUS   1 0  10000
RCBUS  1 7  .04
CBUS   7 0  .0017
LCAB   1 2  2.2U
RCAB   2 3  .2
*          INPUT FILTER
CDAN   4 0  5U
RDAN   4 3  11m
LIN    3 5  13U
CIN    6 0  20U
RCIN   6 5  8m
RID    5 8  .5
CID    8 0  220U
*          POWER STAGE
GPWM   5 0  32 0  11.5
EPWM   10 5  32 0  240
FT     10 0  VET   .5
ET     11 0  10 0  .5
VET    11 12 DC    0
*          OUTPUT FILTER
RL1    12 13 .01
L1     13 14 58U
RCOUT  14 15 .28
COUT   15 0  40U
L2     14 16 7.5U
RBAT   16 0  .03
*          SAMPLING GAIN
HCS    18 0  VET   .1
CS1    18 19 3.54U
RS1    19 0  1G
LS     19 20 3.54U
CS2    20 21 3.54U
RS2    21 22 -1.57
EHI    22 0  19 0  -1G
*    CURRENT ERROR AMP
LY     18 33 1G
CY     33 60 1G
VACI   60 0  AC  0
REA    33 25 33K
R1     25 0  1G
CEA    25 26 3300P
EIR    26 0  25 0  -1G
*              VOLTAGE ERROR AMP
EVS    9  0  1  0   1
LX     9  29 1G
CX     50 29 1G
VACV   50 0  AC  1
R11    29 30 20K
RM     30 0  1G
C1     30 36 560P
R22    30 35 33K
C2     35 36 6800P
EVR    36 0  30 0   -1G
RDA    36 37 10K
CDA    37 0  100P
*              3823 SUMMING AMP
EINV   23 0  22 0   -1
R1823  23 27 20K
R2     27 0  1G
R3823  27 28 20K
E3823  28 0  POLY(2) 37,0 27,0  0  -1G -1G
*              COMPARATOR GAIN
ESUM   31 0 POLY(3) 5,0 14,0 28,0  0  -6.3m  8.4m  1
RSUM   31 0  1K
EFM    32 0  31 0   .48
RFM    32 0  1K
*              CONTROL STATEMENTS
.ac dec   10    .1  100k
.probe
.PRINT AC VDB(9) VP(9)
.END
```

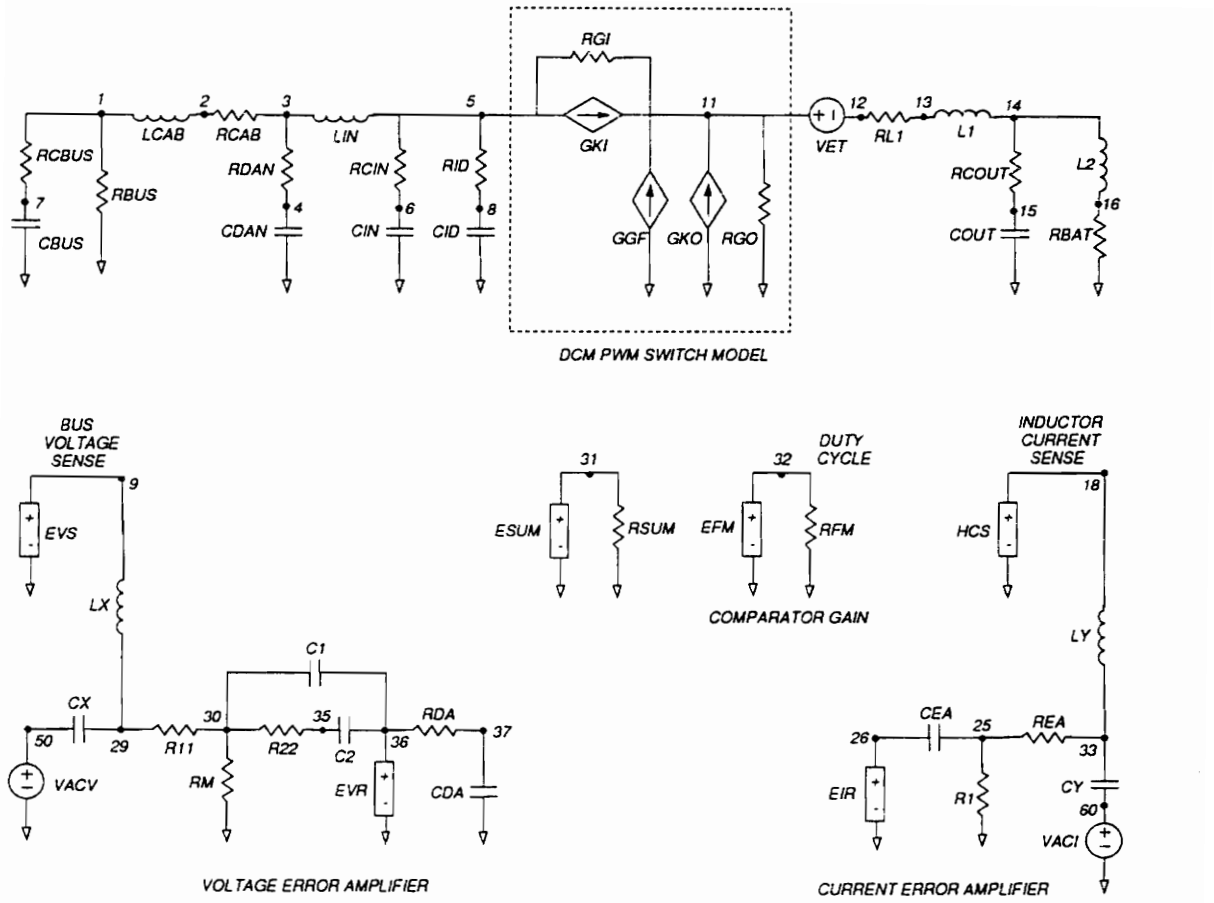


Fig. A.2. PSpice DCM Model Circuit

Table A.2. PSpice DCM Model Listing

```
*          BUS INPUT
RBUS   1 0  10000
RCBUS  1 7  .04
CBUS   7 0  .0017
LCAB   1 2  2.2U
RCAB   2 3  .2
*          INPUT FILTER
CDAN   4 0  5U
RDAN   4 3  11m
LIN    3 5  13U
CIN    6 0  20U
RCIN   6 5  8m
RID    5 8  .8
CID    8 0  220U
*          POWER STAGE
GKI    5  11   32 0   3.37
RGI    5  11   61.8
GGF    0  11   5 12   .0198
GKO    0  11   32 0   2.07
RGO    0  11   164
VET    11 12   DC   0
*          OUTPUT FILTER
RL1    12 13  .01
L1     13 14  58U
RCOUT  14 15  .28
COUT   15 0   40U
L2     14 16  7.5U
RBAT   16 0   .03
*       CURRENT ERROR AMP
HCS    18 0  VET  .1
LY     18 33  1G
CY     33 60  1G
VACI   60 0   AC   0
REA    33 25  33K
R1     25 0   1G
CEA    25 26  3300P
EIR    26 0   25 0   -1G
*              VOLTAGE ERROR AMP
EVS    9  0  1  0    1
LX     9  29  1G
CX     50 29  1G
VACV   50 0   AC  1
R11    29 30  20K
RM     30 0   1G
C1     30 36  560P
R22    30 35  33K
C2     35 36  6800P
EVR    36 0   30,0   -1G
RDA    36 37  10K
CDA    37 0   100P
*              SUMMING AND COMPARATOR GAIN
ESUM   31 0   POLY(2)  1,0   37,0   0   -.0057   -2
RSUM   31 0   1K
EFM    32 0   31 0    .57
RFM    32 0   1K
*              CONTROL STATEMENTS
.ac dec   20    .01  10k
.probe
.PRINT AC VDB(1) VP(1)
.END
```

Appendix B - Control Circuit Schematic

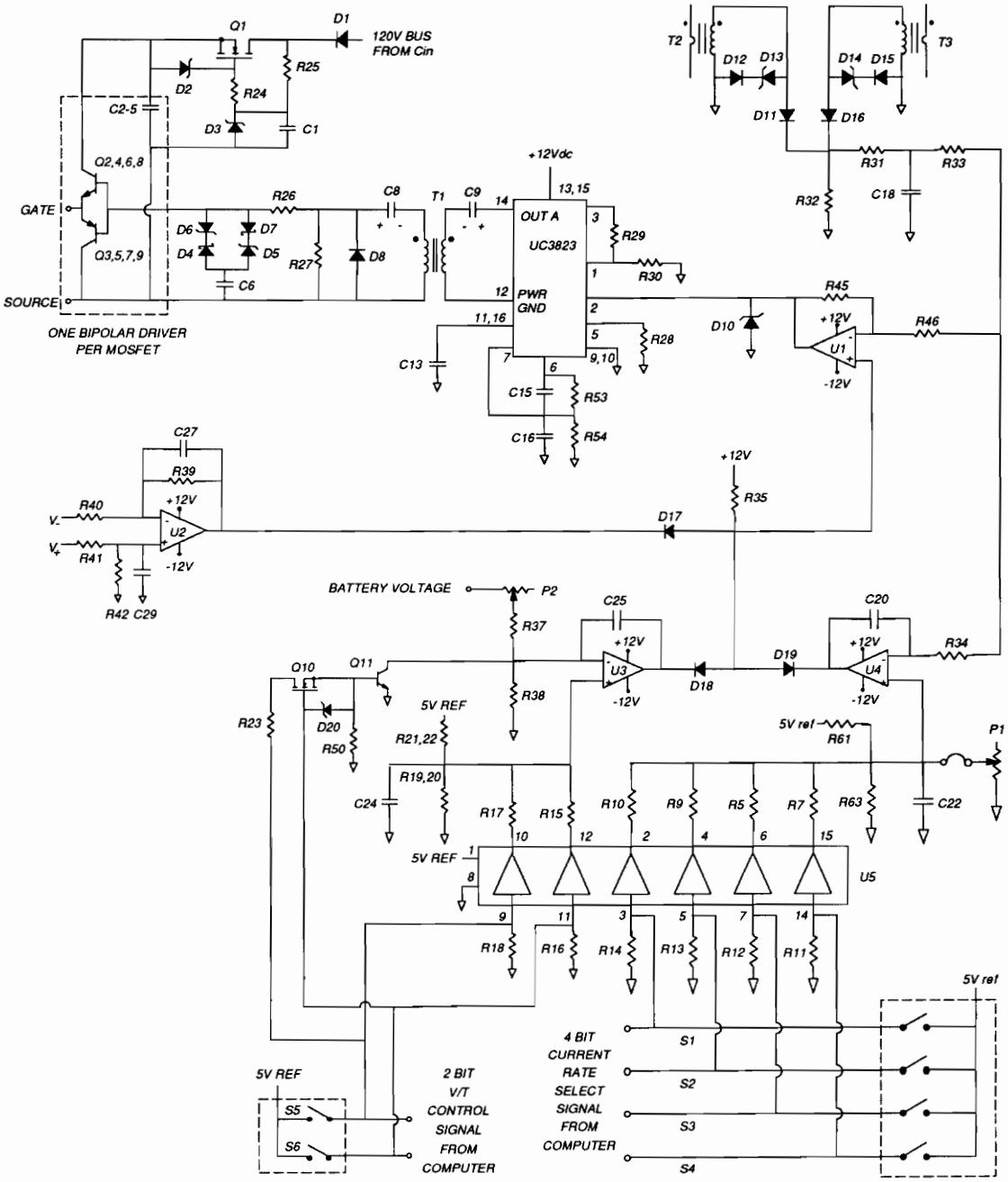


Fig. B.1. Composite Charger Control Circuit

Appendix C - Photograph of Charger

Shown below in Fig. C.1 is a photograph of the prototype battery charger. To obtain a sense of scale, note that the actual dimensions of the control printed circuit board are 5 inches by 3.25 inches.

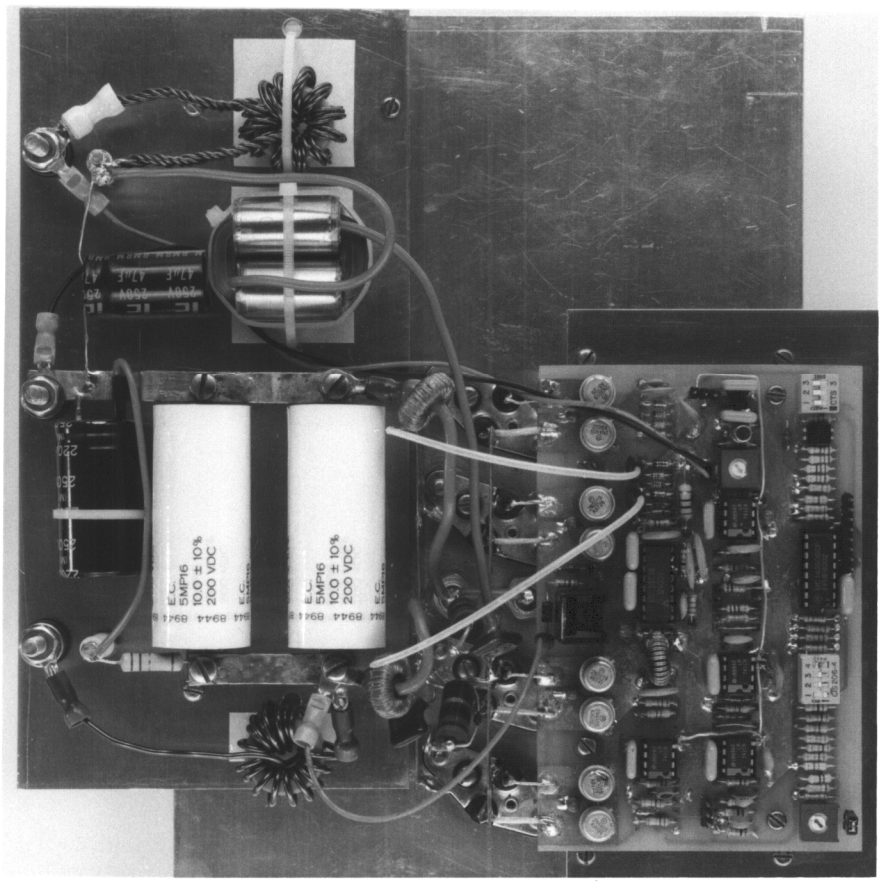


Fig. C.1. Photograph of Prototype Battery Charger

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Vita

Tom Sizemore was born in South Boston, Virginia on March 24, 1956. He obtained his BS degree in Electrical Engineering from Virginia Tech in June 1979. During his undergraduate years, he was a cooperative education student with General Electric and Westinghouse.

From July 1979 to December 1980, he worked for Appalachian Power Co. in Pulaski, Virginia in the field of ac power distribution.

From December 1980 to January 1988, he was a Member of the Technical Staff at COMSAT Laboratories in Clarksburg, Maryland where he designed and analyzed spacecraft power electronics and systems.

From January 1988 to August 1989 he was a Senior Engineer at Fairchild Space Co. in Germantown, Maryland where he designed spacecraft dc/dc converters.

In August 1989 he joined the Virginia Power Electronics Center where he performed research on the NASA Space Platform power system while pursuing his Masters degree in Electrical Engineering.

After graduation, he plans to continue working in aerospace power electronics while spending more time with his son, Cameron.

Tom Sizemore