Design of a High-Efficiency, High-Performance Zero-Voltage-Switched Battery Charger-Discharger for the NASA EOS Space Platform

by

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Thesis submitted to the faculty of the Virginia Polytechnic Institute and State University in partial fulfillment of the requirements for the degree of Master of Science in Electrical Engineering

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Committee Chairman: Dr. F.C. Lee
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(ABSTRACT)

The integration of two Zero-Voltage-Switched Bidirectional Battery Charger-Discharger (ZVS-BBCD) units into a space power system is shown. A robust design featuring four interleaved phases, commandable charge rates, overcurrent protection, overvoltage protection, soft starting, reliable gate drive circuitry, high efficiency, and good dynamics is demonstrated. The ZVS-BBCD is compared to separate hard-switched multi-module charge and discharge units in weight and efficiency and is found to be significantly lighter with comparable losses. The ZVS-BBCD has similar characteristics in discharge and in charge bus regulation modes and allows the use of a common control design for both modes. The two ZVS-BBCDs are integrated into the NASA power system testbed built at the Virginia Power Electronics Center (VPEC) to test their dynamics. The result shows good characteristics including low bus impedance and fast transient response.
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1. Introduction

1.1 Overview

This thesis describes the design of a high-efficiency, high-performance Zero-Voltage-Switched Bidirectional-Battery-Charger-Discharger (ZVS-BBCDs). The technical feasibility of integrating two ZVS-BBCDs into a spacecraft power system is analyzed. A robust design featuring:

- commandable charge rates,
- overcurrent protection,
- overvoltage protection,
- soft starting,
- reliable gate drive circuitry,
- high efficiency, and
- good dynamics

is demonstrated.
The two ZVS-BBCDs were designed, built and then tested in a testbed for the NASA EOS satellite built by the Virginia Power Electronics Center (VPEC). A block diagram of the testbed is shown in fig. 1.1. It consists of two battery simulators, two ZVS-BBCDs, a solar array simulator, a Shunt Switching Unit (SSU), a load simulator, and a Power Control Unit (PCU). During the eclipse portion of the orbit when no power is available from the solar arrays, the SSU is inactive. The spacecraft load is supplied by the batteries through the ZVS-BBCDs which regulate the spacecraft bus at 120 VDC. As the spacecraft comes out of eclipse the solar arrays begin to supply the load and charge the batteries. For a short period of time, the solar array has inadequate power to charge the batteries at their commanded charge rate. During this mode, known as charge bus regulation, the ZVS-BBCDs regulate the bus by cutting back on the charge rate. During the sunlight portion of the orbit the 12 kW solar arrays are the main source of power. These supply power to the spacecraft loads and charge the batteries at a commanded constant charge rate through the ZVS-BBCDs. The main bus of the system is regulated at 121 VDC by the SSU. This last mode is known as charge current regulation since the ZVS-BBCDs no longer regulate the bus but rather the battery charge current. The one volt dead band between modes ensures the SSU is not activated until the ZVS-BBCDs are charging the batteries to the commanded rate.

The two ZVS-BBCDs replace separate charge and discharge units in the testbed. A comparison of size and loss breakdowns is provided.
Fig. 1.1 Block diagram of the NASA testbed at VPEC.
1.2 Design Specifications

The following design specifications for the ZVS-BBCD during all modes of operation:

Battery Voltage = 53 - 84 VDC (64 - 84 VDC nominal),

Charge Current Levels = 0.85 -23 ADC (in 16 charge rates),

Battery Ripple Current = 230 mA pk-pk,

Bus Voltage = 120 VDC±4%,

Bus Ripple Voltage = 200 mV pk-pk,

Bus Voltage Transient = ±4.8 V pk-pk,

Bus Voltage Transient Settling Time < 10 mS (full to no-load)

Processed Power = 1930 W pk,

Nominal Efficiency = 95%, and

Switching Frequency = 100 kHz, and

Output Impedance ≤ 0.15 Ω.

The batteries are made up of a series of 54 nickel-hydrogen cells which have a nominal charge of 1.5 VDC each. Nominally the batteries do not go below 64 VDC.
Under certain abnormalities the batteries can reach 53 VDC which corresponds to less than 1 VDC per cell. The ZVS-BBCD is designed for this abnormal condition. During battery charging the current to the batteries must have a low ripple. The specified peak to peak ripple is 1% of full charge current or 230 mA.

The bus voltage needs to be regulated by the ZVS-BBCD at 120 VDC during discharge, and charge-bus regulation modes (eclipse and transition). The maximum peak to peak voltage ripple on the bus is 200 mV. Load transients should not disturb the quality of the bus voltage and this imposes a quick response time on the ZVS-BBCD.

Power losses should be kept at less than 96 W during peak power processing. A high efficiency reduces heatsink weight and increases converter reliability. A 100 kHz switching frequency is selected to reduce filter components weight and size.

1.3 Thesis Outline

Chapter 2 presents the operation, and loss breakdown for the ZVS-BBCD circuit. The efficiency and weight of the ZVS-BBCD circuit is then compared to the separate battery charger-discharger units. The ZVS-BBCD has equal efficiency with a significant decrease in weight.

Chapter 3 discusses the power stage design of the converter. A comparison between an 8 MOSFET converter and a 16 MOSFET converter is presented. The 16 MOSFET power stage is found to be more efficient. The PWM circuitry for a four-
module interleaved ZVS-BBCD is designed along with the gate drive. A detailed discussion of all the protection circuitry is given that includes bus over-voltage, battery under-voltage, and over-current. The design and discussion of the bus filter and battery filter is given.

The control and performance of the ZVS-BBCD units in discharge-mode is shown in chapter 4. The converters only operate in CCM due to their bidirectional nature. The converters use current-mode control to ensure current sharing. The converters are integrated into the testbed and show fast transient response times and low output impedance.

Charge-mode bus regulation and charge regulation controls are covered in chapter 5. Current mode control is also used in charge-mode. This presents some interesting control characteristics that could make the converters conditionally stable. Performance characteristics show very similar results to those in discharge mode.

The two ZVS-BBCD are identical and therefore their operation, loss breakdown and power stage design are the same. For this reason chapters 2 and 3 deal with a single converter. Chapters 4 and 5 show the control of the converters in discharge and charge modes respectively. The performance results are measured by integrating two ZVS-BBCDs into the NASA testbed.
Conclusions are given in chapter 6. A brief discussion of the main results of this work are discussed.
2. Converter Operation And Trade-Off Analysis

2.1 Introduction

The zero-voltage-switched (ZVS) operation of the BBCD is explained in this chapter. By using ZVS the need for blocking diodes on the switches and of fast recovery anti-parallel external diodes is eliminated. Fig. 2.1 shows a conventional bidirectional converter were it is necessary to add external diodes to avoid switch failure due to the slow reverse recovery time of the body diode.

This chapter also presents a comparison of weight and loss breakdown between the ZVS-BBCDs and separate charge and discharge units. The improved small signal characteristics of the ZVS-BBCD allow a smaller bus capacitance to be used. This significantly reduces the overall weight of the system.

2.2 Converter Operation

ZVS is made possible by forcing the main inductor to resonate with the switches’ drain to source capacitances. The resonant process occurs after the turn-off of either switch and before the turn on of the complimentary switch. Figs. 2.2 and 2.3 explain the resonant process. At time $t_0$ the boost switch is on and the buck switch drain to source
Fig. 2.1 Conventional Bidirectional converter.
Fig. 2.2 ZVS bidirectional converter and main waveforms.
t0 boost switch is on. Junction capacitance of buck switch at VBus.

VBus

R_L

I_SA

i_L

Batt.

VBus

R_L

I_SA

i_L

Batt.

VBus

R_L

I_SA

i_L

Batt.

VBus

R_L

I_SA

i_L

Batt.

Fig. 2.3 Resonant process.

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capacitance is charged to the bus voltage. At \( t_1 \) the boost switch is turned off and the buck body diode begins to conduct and discharges the buck switch drain to source capacitance with the inductor energy. At the same instant the boost capacitance is charged to the bus voltage. At \( t_2 \) the resonant process finishes and the buck switch is tuned on with zero-voltage. At time \( t_3 \) the buck switch is turned off and the body diode of the boost switch turns on and discharges the drain to source capacitance of the switch. The buck switch capacitance is then charged to the bus voltage and the resonant process is over for one switching cycle.

Two design parameters must be taken into account in order to ensure that ZVS occurs. The energy stored in the main inductor during the resonant process must be enough to discharge the drain to source capacitances of the MOSFETs [1]. This can be defined as:

\[
\frac{1}{2} L I_{\text{off}} > C_{ds} V_{\text{bus}}^2
\]  

(1)

where \( L \) is the main energy transfer inductor, \( I_{\text{off}} \) is the inductor current during off time, \( C_{ds} \) is the drain to source capacitance and \( V_{\text{bus}} \) is the bus voltage. This condition must be met twice during each switching cycle described above. The resonant process also requires a finite time to occur which is satisfied by the following requirement [1]:

\[
T_d = \sqrt{\frac{2C_{ds} L}{4}}
\]  

(2)

2. Converter Operation and Trade-Off Analysis 12
which is one fourth of the resonant time period. This delay must be implemented in the control of the converter by implementing fast turn-off and slow turn-on of the devices.

2.3 Trade-Off Analysis

Extensive work has been done on the testbed to compare different topologies for chargers [2] and for dischargers [3], [4]. Two separate multi-module charger [2] and two separate multi-module discharger units [3] were used in the NASA EOS testbed from 1991 to the present. To continue the task on the testbed two multi-module ZVS-BBCDs units have replaced the separate units. This section demonstrates the feasibility of replacing separate units with bidirectional units. The trade-offs presented will compare efficiency and weight.

2.3.1 Efficiency

Optimized designs of multi-module charger and discharger circuits are given in [2] and [3] respectively and will not be repeated here. For comparison purposes only the results of those designs along with a detailed loss analysis for the ZVS BBCD converter will be given. The ZVS-BBCD power stage design used for this comparison is shown in Fig. 2.4. It consists of four interleaved phases each with two MOSFETs and one energy transfer inductor. This design will be referred to as the 8 MOSFET power stage.

The first component of losses are semiconductor losses. These include conduction and switching losses. Due to the operation of the ZVS bidirectional converter the turn on
switching losses are completely eliminated, but turn off losses are still present. To simplify the analysis turn-off losses will be approximated to be 1% of the losses at full load or approximately 18 W.

The conduction losses are given by:

\[ P_Q = I_{rms}^2 \cdot R_{on} \]  \hspace{1cm} (3)

Where \( R_{on} \) is the on-state resistance of the MOSFETs and \( I_{rms} \) is the RMS current through the MOSFETs. The ZVS-BBCD can use synchronous rectification if the voltage drop across the MOSFET channel is lower than the body diode drop. For the MOSFETs used in this analysis (IRFP250 with \( R_{dson} = 0.085 \, \Omega \)) the maximum voltage drop occurs at full load and is 1.7 V while for the body diode it is of 2 V. It can therefore be assumed that the current will only flow through the channel of the MOSFETs. In order to determine the RMS current an approximation needs to be made. The current waveform through the inductor is a continuous waveform with instantaneous positive and negative peaks as shown in fig. 2.4. The conduction losses for the buck and boost can be calculated separately. This becomes a geometric problem if the inductor current waveform is approximated as a perfect triangle. The first problem is to determine the peak inductor current in discharge mode. The peak to peak change in inductor current is given by:

\[ I_{pk-pk} = \frac{V_{batt}}{L} \cdot D \cdot T_s. \]  \hspace{1cm} (4)
Defining;

\[
\tan(\alpha) = \frac{I_{pk} - pk}{D \cdot T_s},
\]

(5)

\[
\tan(\beta) = \frac{I_{pk} - pk}{D' \cdot T_s},
\]

(6)

\[
I_{\text{phase}} = \frac{I_{\text{batt}}}{4}
\]

(7)

and

\[
\lambda = \frac{\left(\frac{I_{\text{pos}}}{\tan(\alpha)} + \frac{I_{\text{pos}}}{\tan(\beta)}\right)}{T_s}
\]

(8)

allows one to solve for \(I_{\text{pos}}\) from the following function

\[
f(I_{\text{pos}}) = \left[\frac{I_{\text{pos}}}{2} \cdot \lambda - \left[\frac{I_{pk} - pk - I_{pos}}{2} \cdot [1 - \lambda]\right]\right] - I_{\text{phase}}.
\]

(9)
Fig. 2.4 Schematic of 8 MOSFET power stage.
Fig. 2.5 Ideal inductor waveform.
Then negative peak can be defined from (2) and (7) as:

\[ I_{\text{neg}} = I_{\text{pk-pk}} - I_{\text{pos}}. \]  \hspace{1cm} (10)

Knowing the positive and negative peaks allows calculation of the RMS currents through both the buck and boost switches separately. First the time during which the positive and negative peaks occur can be defined using fig. 2.4 as:

\[ t_1 = \frac{I_{\text{pk-pk}}}{D \cdot T_s}, \quad t_2 = \frac{I_{\text{pk-pk}}}{D' \cdot T_s}. \]  \hspace{1cm} (11)

Therefore the RMS currents for the boost and buck switches respectively become:

\[ I_{\text{rmsbst}} = I_{\text{pos}} \cdot \sqrt{\frac{t_1}{3 \cdot T_s}} + I_{\text{neg}} \cdot \sqrt{\frac{(D \cdot T_s - t_1)}{3 \cdot T_s}} \]  \hspace{1cm} (12)

and

\[ I_{\text{rmsbk}} = I_{\text{pos}} \cdot \sqrt{\frac{t_2}{3 \cdot T_s}} + I_{\text{neg}} \cdot \sqrt{\frac{(D' \cdot T_s - t_2)}{3 \cdot T_s}}. \]  \hspace{1cm} (13)
The inductor will also contribute considerable losses. The selection procedure for the core and wire is given in chapter 3. The inductors for the bidirectional converter are wound on MPP55550 cores with 130/35 Litz wire. It is necessary to use Litz wire due to the high RMS current in the inductor. The core losses of the inductor are calculated using manufacturer supplied data for MPP cores:[5]

\[ P_{core} = 0.0655 \cdot \left( \frac{l}{T_s \cdot 1000} \right)^{1.37} \cdot \left( \frac{B}{1000} \right)^{2.18} \] (14)

where \( B \) is the flux density in the inductor and \( T_s \) is the switching period. The conduction loss of the inductor winding can be calculated by the following formula:

\[ P_{cond} = R_cu \cdot I_{batt}^2 \cdot F_{ac} \] (15)

where \( R_cu \) is the dc resistance of the coil, \( I_{batt} \) is the battery current and \( F_{ac} \) is the ac resistivity obtained using Dowell curves. [6]

Table 2.1 shows a breakdown of losses between the discharge and charge modes of the ZVS BBCD converter and the discharger-charger units. The ZVS-BBCD exhibits considerable turn-off losses due to the increased peak current in each MOSFET. Inductor losses are increased since there is a large flux swing on the inductor core due to the large peak to peak current necessary to maintain ZVS. The discharge losses are taken at full load, 15 A, while the charge losses are taken at a 23 A battery charge rate.
2.4.2 Weight

The weight comparison takes into account magnetics, semiconductors, and bus capacitors. The superior small signal characteristics of the ZVS-BBCD allow the use of a smaller bus capacitance. The size of the bus capacitance necessary for two ZVS-BBCDs is 500 \( \mu F \) while for separate charger-discharger units is of 2000 \( \mu F \). The capacitors used in the comparison are made up of 20 \( \mu F \) metallized polypropylene capacitors placed in parallel. The semiconductor weight used for the MOSFETs is that of the IRFP250 MOSFETs in a TO-247 plastic package. All the inductors are wound on MPP cores from Magnetics [5]. Table 2.2 summarizes the weight comparison between a system composed of different charger-discharger units and a system composed of a ZVS-BBCD unit. The weight savings is considerable. The main difference is found in the magnetic components and the bus capacitor.

2.4 Conclusions

This chapter has presented the operation of the ZVS-BBCD converter and a trade-off analysis between a separate charger-discharger system and a ZVS-BBCD system. The operation of the ZVS-BBCD has two main characteristics. One is that it provides ZVS for both switches. This decreases turn on stresses on the switching devices. The second is that
to ensure ZVS a large peak to peak current ripple on the main energy transfer inductor is necessary which increases core losses.

The trade-off analysis has shown approximate equal efficiencies between separate charger-discharger units and the ZVS BBCD converter. The main difference is in the weight and size of the different charger-discharger systems. The ZVS BBCD converter system reduces the number of magnetic components in half. This reduction along with a smaller bus capacitance provide a significant decrease in the overall system weight.
Table 2.1 Loss Comparison.

<table>
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<th>Charge Mode</th>
<th>Discharge Mode</th>
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<tr>
<td></td>
<td>ZVS-BBCD</td>
<td>Present Charger</td>
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<tr>
<td>MOSFET Conduction</td>
<td>27.6</td>
<td>6.0</td>
</tr>
<tr>
<td>Diode Conduction</td>
<td>-</td>
<td>20.0</td>
</tr>
<tr>
<td>MOSFET Switching</td>
<td>18</td>
<td>9.7</td>
</tr>
<tr>
<td>Diode Switching</td>
<td>-</td>
<td>9.6</td>
</tr>
<tr>
<td>Inductor Conduction</td>
<td>1.6</td>
<td>2.8</td>
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<tr>
<td>Inductor Core</td>
<td>11.8</td>
<td>2.8</td>
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<tr>
<td>Total (watts)</td>
<td>59.0</td>
<td>50.9</td>
</tr>
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Table 2.2 Weight Comparison (all weights in gms).

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<thead>
<tr>
<th></th>
<th>ZVS-BBCD</th>
<th>Present Charger</th>
<th>Present Discharger</th>
</tr>
</thead>
<tbody>
<tr>
<td>Battery</td>
<td>20</td>
<td>20</td>
<td>20</td>
</tr>
<tr>
<td>Inductor</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Battery</td>
<td>20</td>
<td>60</td>
<td>60</td>
</tr>
<tr>
<td>Capacitor</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MOSFETs</td>
<td>13.6</td>
<td>6.8</td>
<td>6.8</td>
</tr>
<tr>
<td>Diodes</td>
<td>-</td>
<td>28</td>
<td>28</td>
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<tr>
<td>Main Inductor</td>
<td>240</td>
<td>566</td>
<td>240</td>
</tr>
<tr>
<td>Bus Capacitor</td>
<td>1500</td>
<td></td>
<td>6000</td>
</tr>
<tr>
<td>System total (gms)</td>
<td>1793.6</td>
<td></td>
<td>7007.6</td>
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</table>
3. Power Stage Design

3.1 Introduction

The circuit diagram of the bidirectional converter power stage is shown in Fig. 3.1. The four stages are tied at the bus capacitor and at the battery. The stages are phase shifted by 90° and theoretically provide very low voltage and current ripple[2], [3]. This chapter will present the power stage design for the ZVS-BBCD. The complete design is presented including power switches, PWM circuitry, gate drives, protection, and filtering.

3.2 Power Switches

The switches consist of two bidirectional switches for each phase. Each phase must handle one fourth of the power processed. Each switch must be rated to handle the total bus voltage, including derating, and one fourth of the current. Care must be taken when choosing appropriate devices since due to the small value of the energy transfer inductor the RMS currents are relatively high. Chapter 2 presented the operation of the converter and the energy equation was used to ensure ZVS. This equation is repeated here for convenience:

\[ \frac{1}{2}L_{\text{off}}I_{\text{off}}^2 > C_{\text{ds}}V_{\text{bus}}^2 \]  

(16)
Fig. 3.1 ZVS-BBCD power stage (not including secondary bus filter).
The inductor current at turn off will depend on the inductance, the switching frequency, along with the duty cycle. Taking all these variables into account one can find the peak rise in the inductor current

\[ I_{pk\text{max}} = \frac{V_{bat}}{L} \cdot D \cdot T_s \quad (17) \]

where \( V_{bat} \) is the battery voltage, \( L \) is the inductance, \( D \) the duty cycle, and \( T_s \) the period. Assuming the inductor waveform can be approximated as a perfect triangle (chapter 2) the relationship between the peak positive and peak negative currents can be found. \( I_{off} \) can then be found to be:

\[ I_{off} = I_{pk\text{max}} - I_{pk\text{pos}} \quad (18) \]

where \( I_{pk\text{pos}} \) is the maximum rise in current in the discharge direction. With a knowledge of \( I_{off} \) the minimum inductance necessary for ZVS can be found by knowing \( C_{ds} \). The value of \( C_{ds} \) is dependent on the voltage applied to the pn-junction of the MOSFET and it varies with the following relationship [7]:

\[ C_{ds} = \frac{C_{\text{test}}}{\sqrt{\frac{V_{pn}}{V_{\text{test}}}}} \quad (19) \]
where $C_{test}$ is the pn-junction capacitance measured at the $V_{test}$ voltage and $V_{pn}$ is the voltage applied to the junction. By using several MOSFETs in parallel the total $R_{ds(on)}$ decreases reducing conduction losses. At the same time this causes an increase in $C_{ds}$. A larger $C_{ds}$ value requires a smaller inductance for ZVS. This leads to larger AC current ripple and to larger inductor core losses. For this analysis paralleling more than two MOSFETs per switch was considered pointless due to layout difficulties, increase in weight, and increase in cost. The tradeoff analysis to follow was made between an 8 MOSFET power stage and a 16 MOSFET power stage. The analysis was done using the IRFP250 MOSFETs which have:

- $R_{ds(on)}=0.085 \ \Omega,$
- $V_{ds}=200 \ \text{V},$
- $I_{dmax}=30 \ \text{A (continuous)},$ and
- $C_{test}=2800 \ \text{pF}.$

Table 3.1 shows the loss breakdown for both the eight MOSFET design and the sixteen MOSFET design neglecting switching losses. The conditions are at full load 64 V battery using MPP cores for the inductors wound with 25 and 24 turns respectively of 130/35 Litz wire. The stresses on the MOSFETs are greater for the eight MOSFET design although the core losses on the inductor are lowered. For reliability purposes it is more important to run the semiconductor devices with as low stress as possible this makes the
Table 3.1. Breakdown of losses for 8 and 16 MOSFET designs.

<table>
<thead>
<tr>
<th></th>
<th>8 MOSFET</th>
<th>16 MOSFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>MOSFET conduction losses</td>
<td>25.3 W</td>
<td>13.9 W</td>
</tr>
<tr>
<td>Inductor core losses</td>
<td>10.8 W</td>
<td>11.8 W</td>
</tr>
<tr>
<td>Inductor conduction losses</td>
<td>1.7 W</td>
<td>1.8 W</td>
</tr>
<tr>
<td>Number of semiconductors</td>
<td>8</td>
<td>16</td>
</tr>
</tbody>
</table>
16 MOSFET design more attractive. Fig. 3.2 shows the theoretical efficiency for 64 V and 84 V battery. The efficiency in both cases is improved with the sixteen MOSFET design with the greatest improvement at light loads.

### 3.3 PWM Circuitry

A discrete PWM design approach was used. This gives the design higher noise immunity, more flexibility in designing the slope for CIC control, and more accurate current sharing between interleaved modules [2], [3]. The basic scheme is shown in figs. 3.3 and 3.4.

The 555 timer is operated astable at a frequency of 400 kHz. This generates the clock signal for the CD4017 decade counter. Outputs 3, 2, 4, 7, 10 generate signals $\phi_0$, $\phi_1$, $\phi_2$, $\phi_3$, and $\phi_4$ respectively with a 90º phase shift between each sequential output. Each phase is then a 100 kHz signal with a 25% duty cycle. $\phi_4$ generates the set/reset signal for the counter with the CD4001 logic. $\phi_0$ - $\phi_3$ are used to generate the external ramps for each phase.

Fig. 3.4 shows the PWM generator and timing diagram for $\phi_0$. The resulting ramp is added to the current sense signal and then compared to the error voltage to generate the PWM signal. The CD14013 acts as a latch and prevents multiple triggering. The output of
Fig. 3.2 Theoretical efficiency for eight and sixteen MOSFET designs.
Fig. 3.3 Clock generator.
Fig. 3.4 PWM circuitry and timing diagram.
the latch is nored with the corresponding $\phi$ signal to limit duty cycle at 75% for the boost switches.

The buck switches receive the complimentary PWM signal and therefore a different duty cycle limiting scheme must be used. Fig. 3.4 shows the timing diagram of the PWM signals for $\phi_0$. Note that $\phi_1$ is equal to $\phi_0 + 90^\circ$ and is therefore equivalent to the complement of the buck 75% duty cycle signal. This signal can be applied directly to the buck gate driver inhibit pin to shut it down when the 75% duty cycle limit is reached. This scheme requires no additional circuitry since all the signals are already generated by the PWM circuitry.

### 3.4 MOSFET Gate Drives

Several aspects need to be taken into account when designing the gate drive circuitry.

1. The gate drives should be able to implement the time delay between the turn on of one switch and the turn off of the complimentary to ensure zero-voltage-switching. This should be done without relying on MOSFET parasitics (such as gate capacitance).

2. The IC drivers must provide dual outputs to ensure proper current sharing between paralleled devices.
3. The IC drivers must have an inverting input to provide a complimentary output from the control PWM signal for the buck switches.

4. The IC drivers should provide a logic level inhibit input to limit the duty cycle on the buck switches as described in the PWM circuitry section.

3.4.1 Boost Gate Drives

The circuit diagram of the boost gate drive is shown in fig. 3.5. The turn on delay time is applied at the input of the IC driver. The RCD combination provides a fast turn-off of the MOSFET with a slow turn-on. The time delay is set by proper selection of resistor $R_s$ and capacitor $C_s$. From (2) the time delay necessary using $C_{ds}=55$ pF and $L=17 \ \mu$H is of 21.5 ns. This delay can be set by using $R_s=215 \ \Omega$ and $C_s=1000 \ \text{pF}$. Additional delay time will be added by propagation in the circuit and by the gate turn on time. By ensuring the minimum dead time necessary at the input of the IC driver zero-voltage switching can be assured. The IC drivers used are Unitrode 3707 which have dual inputs and dual outputs to ensure proper current sharing between paralleled devices.

3.4.2 Buck Gate Drives

The circuit diagram of the buck gate drives is shown in fig. 3.6. The design of these gate drives is challenging since the buck switches are floating and require isolated drivers. The Unitrode 3707 IC drivers are also used but by using their inverting inputs. The PWM control signal from the complimentary boost switch is inverted and the
Fig. 3.5 Boost gate drives.
Fig. 3.6 Buck gate drives.
resulting output signal is the complement of the input PWM signal. The time delay is set according to the same guidelines as with the boost switch. In this case the RCD combination is used to slow down the falling edge of the PWM signal (slow turn on) and speed up the rising edge (fast turn off). The delay for these switches is set at 21.5 ns with the same RC combination used for the boost gate drives.

The drive transformer is essentially a pulse transformer. The primary is ac coupled through a capacitor which eliminates any dc bias. This requires dc restoration components in the secondary. These components are an RC combination which must have a slower time constant than the switching frequency to prevent a droop in the gate drive signal. The capacitor is placed in series with the gate while the resistor is placed directly in parallel. The resistor also provides a low impedance path for the magnetizing current of the transformer. If this path is not provided the magnetizing current of the transformer would flow back in to the IC driver during turn-off and damage the IC. The time constant of the RC combination was set at 750 µs (R=750, C=1 µF) and was considered sufficiently larger than the 10 µs period of the switching frequency.

The design of the transformer requires that the magnetizing current be small to avoid unnecessary stress on the IC driver. A high permeability material is desirable so that a small number of turns can be used to achieve the required magnetizing current. The small number of turns will also lower the size of the leakage inductance. The material chosen was the H5C2 from TDK. The maximum flux density of this material is 4000 G with and initial permeability of 10000 ± 30%. The core chosen was the T5-10-2.5 toroidal
core ($A_e=0.0601$ cm$^2$, $l_e=2.18$ cm). The number of turns selected was 22 to ensure low flux excursion while at the same time providing large magnetizing inductance with low leakage. The maximum flux density is calculated with:[6]

$$B_m = \frac{V_p \cdot t_{on} \cdot 10^8}{N_p \cdot A_e}$$  \hspace{1cm} (20)

where $V_p$ is the peak voltage applied to the primary, $N_p$ is the number of turns and $t_{on}$ is the maximum time during which $V_p$ is applied.

$$t_{on} = D_{max} \cdot T_s$$  \hspace{1cm} (21)

$D_{max}$ is the maximum duty cycle (75%) and $T_s$ is the switching period (10 µs). Due to ac coupling on the transformer $V_p$ is the peak output voltage of the IC driver minus the average voltage of the drive waveform.

$$V_p = 5 \, V.$$  \hspace{1cm} (22)

Using (20), (21) and (22):

$$B_m = 2.8 \, kG.$$  \hspace{1cm} (23)
With this result the magnetizing current can be calculated by first calculating the value of the magnetizing inductance \( L_m \). By knowing the inductance coefficient, \( A_L \), and the number of turns, \( N_p \):

\[
L_m = A_L \cdot N^2 .
\]

(24)

For this core

\[
L_m = 1.63 \, mH .
\]

(25)

With the magnetizing inductance value it is possible to find the value of the peak to peak magnetizing current:

\[
i_m = \frac{V_o \cdot t_{on}}{L_m} .
\]

\[
i_m = 69 \, mA
\]

(26)

This level can be easily handled by the UC3707 driver IC which sources 1.5 A.

### 3.4 Protection

The ZVS-bidirectional converter must implement protection circuitry during all modes of operation (discharge, bus-regulation charge, and constant current charge). Voltage protection should include bus over-voltage, and battery under-voltage with soft-
start capability. Over-current protection should independently be applied to each phase and must ensure that ZVS is always maintained.

### 3.4.1 Voltage Protection

Proper voltage protection will ensure that failure of a different unit in the spacecraft power system or of the bidirectional control circuitry will not damage the MOSFETs of the power stage. Over-voltage protection is implemented as shown in fig. 3.7(a). The implementation of the LM339 comparator is that of a Schmitt trigger. The bus voltage is sensed and compared to the protection reference $V_{zp}$ through resistor divider $R_1$ and $R_2$. $V_{zp}$ is a common reference signal for all protection circuitry and it is set at 3.3 V. By properly selecting $R_1$ and $R_2$ the off voltage, $V_{off}$ is set:

$$V_{off} = \frac{R_1 + R_2}{R_1} \cdot V_{zp}.$$  \hfill (27)

Feedback resistor $R_3$ sets the level of the reset, $V_{on}$. This value is set at:

$$V_{on} = \left( V_{zp} - \frac{R_1}{R_1 + R_3} \cdot V_{cc} \right) \cdot \frac{R_1 + R_2}{R_1}. \hfill (28)$$

For this circuit $V_{on} = 136$ V and $V_{off} = 141$ V.

For undervoltage and soft-start the circuit shown in fig. 3.7(b) is used. The circuit must be able to keep the PWM signal low until the battery voltage is at 53 V. At this point
Fig. 3.7 (a) Overvoltage and (b) undervoltage protection.
the comparator will go open collector and the capacitor will charge first through resistor $R_5$ until $D_1$ is back-biased and then through $R_6$. The PWM signal will rise slowly and switching in the power stage begins. To avoid comparator chatter the comparator is operated as a Schmitt trigger with the PWM on voltage set at 53 V and the PWM off voltage set at 40 V. Component selection for the Schmitt trigger follows the same design procedure as the overvoltage circuit.

Due to the implementation of the PWM circuitry the soft start scheme does not account for the buck switches. A low PWM signal will keep the buck switches at 75% duty cycle. Analyzing fig. 3.8 (a) it is evident that when two converters are paralleled together, as in the case of the NASA EOS testbed, it is not desirable to have the buck switches at 75% when the battery voltage is low. As $V_{batt1}$ rises and reaches its soft-start voltage a large charge current will flow from battery 1 to battery 2. Converter #2 will begin operating as a buck converter at 75% duty cycle but, since the boost switch is off, the slow recovery body diode of the boost switch would cause a failure and damage the boost switch.

Undervoltage protection for the buck switch must prevent it from modulating until after the PWM signal has soft-started. This is done by using a third comparator circuit that will maintain the buck switches off through the inhibit pin of the gate drives until a 55 V battery level is reached this scheme is shown in fig.3.8(b). When the boost switches begin modulating and the buck switches are still off and the converter will be operating in DCM.
Fig. 3.8 (a) Two ZVS-BBCD in parallel one regulating the second with the boost switch off and the buck switch at 75% duty cycle. (b) Extra comparator for buck shutdown.
mode. This will not affect converter operation since the buck switch body diode will be turning off with zero current.

3.4.2 Current Protection

Over-current protection serves two purposes. The first is to prevent the converter from losing ZVS. The second is to implement fuse blowing capability in the case of a short circuit in the load or at the battery. The scheme is shown in fig. 3.9. The current limit reference is set at the maximum load permissible that will still allow ZVS with the power stage inductance value. From (1), (2), (3), (4), and (5) the minimum peak of the inductor to ensure ZVS, assuming \( L = 17 \ \mu\text{H} \), is:

\[
I_{\text{off}} = 1.08 \ A. \quad (29)
\]

This value occurs at:

\[
I_o = 18.5 \ A \quad (30)
\]

Which corresponds to an approximate battery current at 64 V discharge of:

\[
I_{\text{batt}} = 35 \ A. \quad (31)
\]

Normal operating conditions limit battery current to 23 A. Therefore to protect the load and battery the current limit is set to 30 A battery which corresponds to 16.5 A load
Fig. 3.9 PWM circuitry with current limit added.
current at 64 V battery. This corresponds to a minimum peak inductor current of 2 A and ensures ZVS.

Over-current protection must take into account both discharge and charge modes of operation. The current sensing scheme must offer isolation, bidirectional capability and AC+DC information. Commercially available wide bandwidth Hall effect devices (FW Bell CL-50) offer the best alternative. These devices avoid the need of complex current sensing design and offer repeatability which is very important for current sharing. Using Hall effect devices requires that only the inductor current be sensed to retrieve AC+DC information for all modes of operation. For current protection the DC portion of the sensed waveform is important. The sensed waveform will replicate the inductor current including positive and negative peaks. This requires the use of an absolute value generator to ensure current protection in both discharge and charge modes. The schematic of the absolute value generator is shown in fig. 3.10. It is simply a full wave precision rectifier using wide-bandwidth operation amplifiers. High-slew rate is a desired characteristic of these operational amplifiers to avoid distortion of the inductor waveform and ensure reliable current protection. The National Semiconductor LF347 amplifiers have a wide-bandwidth with a slew rate of 13 V/µs. The peak to peak inductor waveform is given by (22) and at 64 V battery is 17.6 A. By setting the gain of the Hall effect devices to:

$$G_{he} = 0.2 \frac{V}{A}$$

(32)
Fig. 3.10 Absolute value generator.
the peak to peak voltage waveform of the output will be:

\[ V_{he} = G_{he} \cdot 17.6 \, A \]
\[ V_{he} = 3.52 \, V \]  

which with a 13 V\(\mu\)s slew rate operational amplifier corresponds to a response time of 0.3 \(\mu\)s. This is considered small compared to the switching period. Fig. 3.11 shows the performance of the absolute value generator.

3.5 Filters

3.5.1 Bus Output Filter

A second stage bus output filter serves two purposes. The first is to meet the required voltage ripple specifications. The second is to prevent interaction between two paralleled converters by representing a high input impedance from the bus capacitor.

The bus output filter serves as an output filter during discharge and bus-regulation charge modes. During constant charge current mode it is essentially an input filter. The voltage ripple specification at the bus is of 200 mV\(pp\) and should be met during all modes of operation. In discharge mode the converter is essentially a boost converter which has the characteristic of a large output voltage ripple. This same problem is seen during charge mode where a large pulsating current is drawn from the bus. The design to follow will use the CEO1 and CEO3 standards set by NASA for EMI emissions using the RMS current.
Fig. 3.11 Absolute value generator performance.
ripple [9]. By using these standards along with high quality capacitors the 200 mV specification should be met.

The RMS current ripple for a four-phase unit can be approximated by the following relationships:[3]

\[
I_{rms} = \frac{I_o}{1-D} \sqrt{D \cdot (1-D)} \quad 0 \leq D \leq 0.25
\]  \hspace{1cm} (34)

\[
I_{rms} = \frac{I_o}{1-D} \sqrt{-D^2 + \frac{3}{4} D - \frac{1}{8}} \quad 0.25 \leq D \leq 0.5
\]  \hspace{1cm} (35)

\[
I_{rms} = \frac{I_o}{1-D} \sqrt{-D^2 + \frac{5}{4} D - \frac{3}{8}} \quad 0.5 \leq D \leq 0.75
\]  \hspace{1cm} (36)

The peak ripple occurs at 72 V battery and is approximately 3.8 A. The voltage RMS ripple will depend on the value of the ESR of the capacitors.

At the fundamental component of the ripple current (400 kHz) the maximum allowable ripple is given by:

\[
I_{rms0} = 46 + 20 \cdot \log I_{odc}
\]  \hspace{1cm} (37)

where \(I_{odc}\) is the maximum dc output current. For a 14 A output current the maximum ripple becomes:
\[
IR_{rmsk} = 10^{6.89/20} \mu A = 2.8 mA. \quad (38)
\]

The attenuation necessary at 400 kHz is therefore:

\[
A_{400kHz} = 20 \cdot \log \frac{2.8mA}{3.8A} = -62.7 dB. \quad (39)
\]

Different secondary filter configurations can be used obtain this attenuation. Fig. 3.12 shows two possible configurations. The first is a stage with an RC damping branch. The damping capacitor shown \( C_D \) is made much larger than the output capacitor \( C_{bus} \). The requirement to use flight approved capacitors imposes that high quality polypropylene capacitors be used. These capacitors have a large size and would make the size of \( C_d \) prohibitively large. The selected topology is therefore the one with the parallel LR damping branch. Setting three restrictions:

\[
\frac{L_1}{L_2} = 10 \cdot L_2, \quad \frac{L_2}{R_d} > C_1 \cdot R_d, \quad \text{and} \quad \frac{R_d}{R_d} \leq 0.1. \quad (40)
\]

The current attenuation transfer function can be expressed as

\[
Tca(s) = \frac{1 + sL_1}{(1 + \frac{sL_1}{R_d})(1 + sC_2R_d)(1 + sL_2)(1 + sC_2R_d)}. \quad (41)
\]
3.8 A pk-pk

Fig. 3.12 Different filter configurations.
The asymptotic bode plot of the attenuation transfer function is shown in fig. 3.13. This allows the secondary resonance and Q to be approximated by

\[
\omega_o = \frac{l}{\sqrt{L_2 \cdot C_1}}, \quad \text{and} \\
Q = \frac{l}{\omega_o \cdot C_1 \cdot R_d}.
\]

(41)

This makes the secondary resonance independent of the bus capacitor and sets it far apart from the primary resonance. The primary resonance and Q are:

\[
\omega_p = \frac{l}{\sqrt{L_1 \cdot C_2}}, \quad \text{and} \\
Q_p = \frac{R_d}{\omega_o \cdot L_2}.
\]

(42)

In order to achieve the desired attenuation at 400 kHz the primary resonance is set at 3 kHz and the secondary resonance at 35 kHz. Selection of \( C_2 \) must ensure that it will be able to handle the RMS current. Also it is desirable to select \( C_1 < C_2 \) in order to make the converter insensitive to capacitive loading effects [9]. \( C_2 \) is the bus capacitor (500 \( \mu \)F) and \( C_1 \) is set to 40 \( \mu \)F. \( R_d = 0.1 \) \( \Omega \) results in a Q of approximately 1 for both resonances. The filter design is summarized:

\[
L_2 = 500 \text{ nH}, \quad L_1 = 5 \text{ \mu H} \\
C_1 = 40 \text{ \mu F}, \quad \text{and} \quad R_d = 0.1 \text{ \Omega}
\]

(43)
Fig. 3.13 Assymptotic bode diagram of current attenuation transfer function (41).
Fig. 3.14 (a) shows the resulting transfer function of the filter. It shows an attenuation of -65 dB at 400 kHz. Fig. 3.14 (b) shows the impedance, $Z_r$, of the filter seen from the bus capacitor as defined in fig. 3.12. It shows the importance of properly damping the secondary resonance. The impedance should be maximized to avoid any interaction with other loads on the bus.

Metallized polypropylene capacitors which have an ESR of about 6 mΩ are used for both the first stage capacitor and the bus capacitor. $L_1$ and $L_2$ were both wound on MPP cores. The core selected for $L_1$ was the 55350 with 7 turns of AWG #12 wire. The core was selected to minimize the number of turns required and therefore reduce the conduction losses without making the core size unnecessarily large. The losses are calculated by knowing the RMS current and winding resistance of the inductor. For #12 wire the resistance is [10]:

$$R_{#12} = 5.22 \frac{mΩ}{meter} \quad (44)$$

and the length/turn for a 40% winding factor is [5]:

$$l_{\text{turn}} = 3.34 \text{ cm}. \quad (45)$$

This results in a winding resistance of:
Fig. 3.14 (a) Output filter's transfer function and (b) Zi impedance.
\[ R_{dc} = R_{\#12} \cdot \frac{I_{\text{turn}}}{100} = 0.17 \text{ m}\Omega \]  \hspace{1cm} (46)

Neglecting the bus voltage ripple this results in a dissipation at maximum load of:

\[ P_{\text{c.l.f}} = I_{o_{\text{max}}}^2 \cdot R_{dc} = 33 \text{ mW}. \]  \hspace{1cm} (47)

This can be considered negligible at 1.8 kW full power.

Simulation results of the actual converter are shown in fig. 3.15. The peak to peak magnitude of the voltage ripple is only 0.5 mV which is well below the required level. The output filter configuration used in the simulation is shown in fig. 3.16. ESRs for both the bus and first stage capacitor were included along with the ESL for the bus capacitor.

It was very difficult to measure the actual ripple on the oscilloscope due to common mode noise from the power grounds. It was decided to measure the EMI spectrum instead by using an isolated current probe. The test set up is shown in fig. 3.17. The results are shown in fig. 3.18 for a 12 A load and 72 V battery for a single converter. The peak of the spectrum occurs at 100 kHz with a maximum voltage of 239 \( \mu \)V. This corresponds to a 24 mV ripple. This noise is due in part to the noise from the Sorensen power supplies and to different current sharing in the ZVS-BBCD phases. The spectrum at 370 kHz corresponds to the four paralleled phases of the converter and is equivalent to a 7 mV ripple at the load. This is considered very low and under the EMI
Fig. 3.15 Voltage ripple simulation results.
Fig. 3.16 Filter used in simulation.
Fig. 3.17 EMI noise measurement test set up.
Fig. 3.18 EMI measurement at 12 A load and 72 V battery for a single unit.
specifications. Fig. 3.19 shows the result for two paralleled devices. It is apparent that both converters have a slightly different switching frequency. The peak of the noise is still at 100 kHz and remains at the previous level. The spectrum at around 370 kHz shows two peaks which correspond to each converter. The noise has increased at 370 kHz. The maximum peak is of 10.5 mV but this level is still below the EMI noise standards.

3.5.2 Energy Transfer Inductor

The value of the input inductance is set by the energy equation given in (21). By knowing the drain to source capacitance of the MOSFETs found using (24), and selecting the valley inductor current full load current and 64 V \( L \) is calculated as:

\[
L = \frac{2 \cdot C_{ds} \cdot V_{bus}^2}{I_{off}^2}
\]  

(48)

The final value of \( L \) was set 17 \( \mu \)H. This gives from (22) and (23) a valley inductor current of 2.5 A at full load, 64 V.

The large ripple current on the inductors makes this inductor design rather challenging. A low permeability gapped core is desired for this inductance. Ferrite cores would give the lowest core losses but require a large air gap for 17 \( \mu \)H at 14 A. Large air gaps on ferrite cores cause the fringing flux to radiate substantial EMI and induce eddy currents in the windings [1]. The latter would have the effect of increasing inductor losses due to an increased AC resistance on the windings. A good choice for these cores would
Fig. 3.19 EMI measurement at 12 A load and 72 V battery for a two units.
be Molypermalloy powder cores (MPP). These have a distributed air gap and come in low permeabilities. Previous work on the ZVS-BBCD converter used an MPP 55550 core [1]. For this work a comparison with this and other cores was done using a spreadsheet program. It was found that the most suitable core was in fact the MPP55550 due to size and losses.

The inductance factor for this core is given in [5] and results in:

\[ N = \sqrt{\frac{0.017}{28}} \cdot 1000 \]  \hspace{1cm} (49)

This results in a flux swing of:

\[ B = \frac{V_{rms}10^8}{4.44A_eNf_s} \]  \hspace{1cm} (50)

and as calculated in chapter 2 in 11.8 W of core losses. For DC operation the bias level must be known in order to determine the loss of permeability and adjust the number of turns if necessary. Using Ampere's law:

\[ H = \frac{0.4\pi NI}{l} \]  \hspace{1cm} (51)
which from [5] results in a 2% reduction in permeability. This reduction is not considered substantial and no adjustment is necessary.

Along with a 14 ADC current level the wire used for the inductor winding must withstand the large ripple current. The losses due to skin and proximity effects on the wire [6] must be taken into account. A Dowell analysis was performed. For the wire selected a set of five parameters must be defined:

\[ d = 2 \cdot \sqrt{\frac{A_w}{\pi}}, \]  \hspace{1cm} (52)

\[ h = \frac{\sqrt{\pi}}{2} \cdot d, \]  \hspace{1cm} (53)

\[ b_w = d_{eq} \cdot \frac{\sqrt{\pi}}{2}, \]  \hspace{1cm} (54)

\[ F_1 = \frac{\sqrt{N_{lw}} \cdot h}{b_w}, \text{ and} \]  \hspace{1cm} (55)

\[ \phi = \frac{h \cdot \sqrt{F_1}}{\delta}. \]  \hspace{1cm} (56)

Where \( A_w \) is the area of a single strand of Litz wire, \( d \) is the diameter of a single strand with \( h \) being the effective conductor height. \( d_{eq} \) is the equivalent diameter of the bundled
strands of Litz wire and $b_w$ is the effective diameter of the bundled strands. $F_I$ is the copper factor and $N_{lw}$ is the equivalent number of turns per layer for Litz wire. $\delta$ is the skin depth at 100 kHz and $\phi$ is the ratio of conductor height to skin depth. Using $\phi$ the AC - DC resistance ratio $F_R$ is found from the Dowell diagrams. The selected Litz wire has 130 strands of AWG #35 wire. Using (52) - (56) the AC - DC resistance ratio is given as:

$$F_R = \frac{R_{AC}}{R_{DC}} = 1.38.$$ (57)

This value is considered close to optimum according to [6].

The equivalent AWG for the 130/35 Litz wire is #14. The wire used had a served single nylon, single polyurethane insulation giving it a total diameter of 1.68 mm. It is desirable to wind the inductor on a single layer on the core to reduce losses and make the AC - DC ratio calculation above valid. The total length available for the winding inside the core assuming a 100% utilization of the inner diameter is: [5]

$$l_{ic} = 60.6 \, mm.$$ (58)

For 25 turns the total necessary length is:

$$l_{25} = 1.68 \cdot 25 = 42 \, mm$$ (59)
which requires a 70% utilization. In practical terms this is a difficult number to achieve. It was found that 25 turns was close to the maximum possible, 26 turns would be questionable.

The copper losses estimated in chapter 2 for the inductor were 2.33 W. These were estimated using the above procedure and were found to be very close in experiments.

3.5.3 Battery Current Ripple

There was no secondary input filter designed. A 5 μF capacitor was placed at the input of the converter. This capacitor essentially formed a secondary LC filter with the inductance of the cable connecting the converter to the battery. The inductance of this cable was found to be of about 3 μH and set the secondary resonance frequency at 40kHz.

The results for the EMI measurements at 72 V battery and full charge current are shown in fig. 3.20. The peak occurs at 100 kHz and corresponds to 30 mA. At the 370kHz the ripple current is of 20 mA. Both of these are very much below the specified 230 mA peak ripple.

3.6 Efficiency

The efficiency results for the ZVS-BBCD circuit were measured during charge and discharge modes. Fig. 3.21 shows the efficiency results measured experimentally for 8 and
Fig. 3.20 EMI measurement at full charge current
Fig. 3.21 Efficiency of bidirectional converter.
16 MOSFET designs. Overall the efficiency of the 16 MOSFET power stage is considered good. At 64 V full load it reaches 97%, with a light load efficiency of about 91.5%. For a single battery voltage the core losses are essentially constant across the entire load range. For this reason core losses become predominant at low power levels. The need for the large AC ripple current for ZVS operation dictates that core losses are the limiting factor to further increase efficiency. For example at 64 V battery and 3 A load the inductor losses make up 40% of the total losses while at 64 V full load current only 24%.

3.7 Conclusions

The power stage design for the ZVS-BBCD have been presented. A detailed description of the switch design was shown. The results indicate that the efficiency of the converter will be improved by paralleling two MOSFETs for every switch. The design of the PWM circuitry has also been presented. The PWM circuitry limits the duty cycle of both the buck and the boost switch to 75%. The gate drive design for the MOSFETs has also been presented. Gate drive design must take into account the several aspects which were discussed in detail. The protection circuitry design is also presented. Bus over-voltage, battery under-voltage, and over-current protection have been implemented. The filter design at the bus has met the ripple specifications. The main energy transfer inductor design has been shown to be rather challenging due to the characteristics of the converter. Power stage efficiency results have been presented and shown to be excellent.
4. Discharge-Mode

4.1 Introduction

The control circuit diagram is shown in fig. 4.1. During discharge mode and charge bus regulation mode the converters are controlled by the same bus voltage loop with each phase employing an independent current injection control (CIC) loop. The bus voltage loop is ored together with the charge current regulation loop. During charge current regulation mode error amplifiers U3 and U4 keep the charge current at a constant commanded charge rate.

In discharge mode the circuit behaves as a boost regulator. The effects of the RHP zero in the control to output transfer function of the boost based topologies is well documented [12]-[13]. The ZVS-BBCD has a small energy transfer inductance and this places the RHP zero at very high frequencies making the small signal characteristics of this topology superior to those of conventional boost topologies.

This chapter will cover the design and analysis of the control circuit in discharge mode. The technique used to model the converter is presented in [14] and has shown good
Fig. 4.1 Control circuit diagram.
agreement with experiment up to half the switching frequency. The design will be based on two paralleled ZVS-BBCD units. It has been shown [17] that to correctly model paralleled converters the current sense network gain $R_{ip}$ for a single module must be divided by the number of paralleled modules. Each ZVS-BBCD unit has four interleaved modules making the total number of paralleled modules 8.

4.2 Current Sensing

In discharge mode the peak of the inductor current is sensed. During charge mode the negative peak or the charge valley inductor current is sensed. The magnitude of the valley inductor current can be small especially near full charge current. This requires special consideration on the sensing scheme used. If transformer sensing is used it must be ensured that the transformers of the different phases be precisely matched. If this is not the case then current mode control and current sharing will not be optimal. If it is possible to precisely sense the peak to peak inductor current in two polarities then the sensed waveform will practically be constant (considering ideal components and constant voltages). The waveform will only be offset in the positive direction (discharge mode) and the negative direction (charge mode).

Hall effect devices were considered an appropriate option. The devices used (F.W. Bell CL-50) have a bandwidth of 150 kHz and a turns ratio of 1000:1. The gain is set by an external discrete resistor and this allows for the use of potentiometers to precisely
match the four phase currents and ensure good current sharing. A 200 Ω resistor gives a gain of:

\[ K_a = \frac{200}{1000} = 0.2 \frac{V}{A}. \] (60)

The inductor current is sensed through the Hall devices and the resistor divider network shown in fig. 4.2. The gain \( R_{ip} \) per module is determined by

\[ R_{ip} = K_a \cdot \left( \frac{R_{sel}}{R_{sel} + R_{se2}} \right). \] (61)

Fig. 4.3 shows the four inductor currents at three different operating conditions. Good current sharing among the phases is seen. This is important for proper cancellation of the ripple current.

4. Discharge-Mode
Fig. 4.2 Current sense scheme.
Fig. 4.3 Inductor currents at (a) 10 A discharge, (b) 1 A discharge, and (c) 10 A charge.
4.3 Small Signal Modeling

Accurate description of the appropriate transfer functions is necessary in order to model the converter and identify the main characteristics. Fig. 4.4 shows a block diagram of the control model parameters. The operation of this converter is always in CCM and this simplifies the analysis. Using averaging techniques [13] the duty cycle to output voltage and duty cycle to inductor current transfer functions, \( F_2 \) and \( F_4 \) respectively, are given by:

\[
F_2(s) = \frac{V_g}{D^2 L_e C} \cdot \frac{(1 + s C R_e) \left( 1 - s \frac{L_e}{R_l} \right)}{\Delta} \tag{62}
\]

\[
F_4(s) = \frac{V_g}{D^3 L_e} \cdot \frac{s + \frac{2}{C \cdot R_l}}{\Delta} \tag{63}
\]

where \( V_g \) is the input or battery voltage, \( C \) is the bus capacitance, \( R_l \) is the load resistance, \( R_e \) is the bus capacitor ESR, and \( D' \) is the boost switch off duty ratio. The inductance \( L_e \) is the actual power stage inductance \( L \) in each module divided by four and is given by:

\[
L_e = \frac{L}{4 \cdot D'^2}. \tag{64}
\]
Fig. 4.4 Control model parameters.
\(\Delta\) is the system's transfer function denominator:

\[
\Delta = s^2 + s \left( \frac{R_{eq} + R_c}{L_e} + \frac{1}{CR_i} \right) + \frac{1}{L_e C}
\]  
(65)

where \(R_{eq}\) is the equivalent inductor series resistance:

\[
R_{eq} = \frac{R_{Is}}{D^2}.
\]  
(66)

From fig. 4.4 the current loop \(T_i\) is found to be:

\[
T_i = F_m R_i F_d(s) H_e(s)
\]  
(67)

where \(R_i\) is the gain of the current sense network divided by the number of paralleled modules, and \(F_m\) is the gain of the modulator dependent in current mode control on the inductor current waveform slope \(S_n\) the external ramp slope \(S_e\) and the switching frequency

\[
F_m = \frac{f_s}{S_n + S_e}.
\]  
(68)

\(H_e(s)\) is the double RHP zero added by the sampling gain network [14] and given as:
\[ H_e(s) = 1 + \frac{s}{\omega_n \Omega_z} + \frac{s^2}{\omega_n^2} \tag{69} \]

where

\[ \Omega_z = \frac{-2}{\pi} \tag{70} \]

and

\[ \omega_n = \pi f_s. \tag{71} \]

The sampled current is added to the control voltage along with the gains \( k_f \) and \( k_r \), which are the feedback gains of the input and output voltages defined as [14]:

\[ k_f = \frac{R_l}{2 f_s} \]

\[ k_r = \frac{D^2 R_l}{2 f_s L} \tag{72} \]

(68)-(72) are used to design and optimize the current loop.

The control to output transfer function is approximated by the following relationship [3]:

\[ \text{4. Discharge-Mode} \]
\[ F_{co}(s) \approx T_o(s)T_p(s) \frac{I}{H_e(s)}. \] (73)

The worst case RHP zero is given at low line full load. This frequency can be approximated as

\[ F_{rhpz} = \frac{R_l}{2\pi L_e}. \] (74)

Which as derived in [1] can be approximated as

\[ F_{rhpz} \approx \frac{F_s}{\pi D}. \] (75)

For this converter \( F_{rhpz} \) will always be beyond half of the switching frequency.

\( T_o(s) \) is defined as the power stage transfer function given by

\[ T_o(s) = \frac{F_mF_2(s)}{I + T_i(s)} \] (76)

and \( T_p(s) \) is the output filter double pole given in chapter 3 by (41).
4.3.1 Feedback Loop Design

It was shown in [14] that the Q of the double pole introduced by the sampling gain $H_e(s)$ can be damped by proper selection of the external ramp slope which is added to the current sense signal. Defining

$$m_c = 1 + \frac{S_e}{Sn}$$

(77)

and reintroducing $Q_z$ from $H_e(s)$ as

$$Q_z = \frac{1}{\pi(m_cD-0.5)}$$

(78)

it is possible to select an appropriate value for $Q_z$. For this converter $S_e$ was selected as $373.333 \times 10^3$ V/s. This resulted in a worst case $Q_z$ of 0.68.

The voltage feedback loop is defined as

$$T_v(s) = F_m F_v(s)F_2(s)$$

(79)

where $F_v(s)$ is the gain of the compensation network in the PCU of the system. The compensation network is shown in fig. 4.5 and provides a zero to obtain the necessary
Fig. 4.5 Compensation network.
phase boost in the loop gain, and a pole at DC to obtain tight regulation. A second pole is not necessary due to the high frequency locations of the ESR zero and the RHP zero. The gain of the integrator is selected in order to cross over 0 dB with acceptable gain and phase margins. The power control unit (PCU) contains the compensator for the voltage loop. The PCU is located away from the converter and its schematic is shown in fig. 4.6. The voltage is sensed via the resistor divider network $R_{s1}$ and $R_{s2}$ through a 4 foot long cable. Amplifier U1 has unity gain and its output is fed to the corresponding compensator network. The ZVS-BBCD network has its output connected to a second 4 foot cable which is connected to a differential amplifier on the converter. This voltage sensing scheme is necessary in order to separate the grounds of the converter and the PCU. The relative distance between both units could offset their grounds and cause measurement errors.

The outer loop gain

$$T_2(s) = \frac{T_0(s)}{1 + T_1(s)}$$

(80)

is used as the criterion to establish the stability margin of the converter [13]. The gain of $T_1(s)$ should not be made too large for it would limit the bandwidth of the system. If this gain is made too small it will decrease the effects of current mode control and create a single loop system which can also be caused by an excessively large external slope.
Fig. 4.6 PCU module diagram.
To model the ZVS-BBCD the PWM switch model for continuous conduction current mode control is used [14]. This technique was used in PSPICE to develop a model of the converter and optimize loop gain design. Fig. 4.7 shows the theoretical control to output response. The RHP zero is not evident and due to the external ramp the double pole from the modulator sampling gain is properly damped.

The outer loop gain responses are shown in fig. 4.8. There is excellent agreement with between the theoretical and experimental gains. The phase margin for the theoretical loop gain is of 55° while for the experimental it is of 53°. The crossover for both cases is at about 4 kHz.

4.5 Performance

The system is composed of two ZVS-BBCD units in parallel each with four interleaved modules. Stability must be ensured even when one battery fails. The system loop for a failed battery would be of a single converter. This would increase the gain of the current loop and decrease the overall bandwidth of the system. This will affect the system performance by reducing load transient response time and increasing the output impedance.
Fig. 4.7 Theoretical control to output function.
Fig. 4.8 Outer loop gain for two units in discharge mode.
Fig. 4.9 shows the outer loop gain for a single converter. The loop crossover frequency is reduced to about 2 kHz. The DC gain is also slightly reduced. The phase margin of the system is increased to 62°.

The transient response result is shown in fig. 4.10. The case is for two paralleled converters. The top trace is the bus voltage transient at 2 V/div. The center trace shows the current step response from 3 A to 12 A, while the bottom trace is for one of the converters' inductor current. The maximum peak is of about 750 mV with a settling time of 270 μs.

As given in [1] the peak output impedance can be approximated to be a function of the loop crossover frequency. This peak is given by

\[ Z_{opk} \approx \frac{1}{2\pi f_c \omega C_{bus}}. \]  

(81)

The expected output impedance for the single converter case will be higher than for the two converter case. The output impedance of the system is shown in fig. 4.11. This is for the two paralleled converter case. The peak is of about -22.5 dB with no peaking beyond the loop crossover up until 100 kHz. The single converter case is shown in fig. 4.12. The peak output impedance is of -18 dB which is still below the specifications.
Fig. 4.9 Outer loop gain for one unit in discharge.
Fig. 4.10 Transient response to an 8 A load step for two converters in discharge mode. Top trace is the load current at 5 A/div, middle trace is the bus voltage (ac coupled) at 1 V/div, and bottom trace is one of the inductor currents at 10 A/div.
Fig. 4.11 Output Impedance for two units in parallel.
Fig. 4.12 Output impedance for one unit in discharge mode.
5. Charge-Mode

5.1 Introduction

Charge-mode is divided into charge current regulation and bus voltage regulation modes. During bus voltage regulation mode the converters' small signal characteristics resemble those of the converters during discharge mode as was shown in [11]. There are two main differences one is that the RHP zero of the control to output transfer function is shifted to the left hand plane. The second is the possible appearance of a RHP pole in the control to output transfer function during some operating conditions. During charge current regulation mode the feedback variable no longer is the bus voltage but the charge current. A new system loop is necessary in order to regulate the converter. This chapter covers the small signal analysis of the converter along with the design of the feedback loops for both modes.

5.2 Current Regulation Mode

Each ZVS-BBCD has its own charge current regulation loop. For this reason it is only necessary to discuss the results for a single unit.
5.2.1 Charge Rate Selection

The implementation of the charge rate selection circuitry is covered in detail in [2]. The same scheme is used here with the exception that the charge current is sensed with a hall effect device, and this avoids the necessity of summing the different phase currents at the error amplifier. The implementation is shown in fig. 5.1. There are sixteen distinct charge rates between 0.85 A and 23 A. The reference can be set manually via dip switches or digitally via a computer. The digital signal coming from the PC or switches contains four bits which are converted to analog signals through the digital to analog circuit (DAC). The output of the DAC contains an analog voltage which sets the reference for the charge rate. The maximum error allowed for the charge currents is 2% of the maximum charge current or 0.46 A. Table 5.1 shows the resulting measurements along with the error. The maximum error, 0.27 A, occurs at the minimum charge rate (0.85 A), and this is due to the non linearities of the hall effect devices.

5.2.2 Feedback Loop Design

The block diagram in fig. 5.2 shows the charge current feedback loop. From the block diagram the following relationship is obtained

\[ F_i(s) = \frac{F_{in}F_{ic}(s)}{1+T_i(s)}. \]  

(82)
Fig. 5.1 Charge rate selection implementation.
## Table 5.1 Commanded and measured charge rates.

<table>
<thead>
<tr>
<th>Digital command</th>
<th>Commanded current</th>
<th>Measured current</th>
<th>Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000</td>
<td>0.85</td>
<td>0.58</td>
<td>-0.27</td>
</tr>
<tr>
<td>0001</td>
<td>2.33</td>
<td>2.09</td>
<td>-0.24</td>
</tr>
<tr>
<td>0010</td>
<td>3.80</td>
<td>3.60</td>
<td>-0.20</td>
</tr>
<tr>
<td>0011</td>
<td>5.28</td>
<td>5.10</td>
<td>-0.18</td>
</tr>
<tr>
<td>0100</td>
<td>6.76</td>
<td>6.64</td>
<td>-0.12</td>
</tr>
<tr>
<td>0101</td>
<td>8.23</td>
<td>8.13</td>
<td>-0.10</td>
</tr>
<tr>
<td>0110</td>
<td>9.71</td>
<td>9.64</td>
<td>-0.07</td>
</tr>
<tr>
<td>0111</td>
<td>11.19</td>
<td>11.14</td>
<td>-0.05</td>
</tr>
<tr>
<td>1000</td>
<td>12.66</td>
<td>12.76</td>
<td>0.10</td>
</tr>
<tr>
<td>1001</td>
<td>14.14</td>
<td>14.30</td>
<td>0.16</td>
</tr>
<tr>
<td>1010</td>
<td>15.62</td>
<td>15.82</td>
<td>0.20</td>
</tr>
<tr>
<td>1011</td>
<td>17.09</td>
<td>17.30</td>
<td>0.21</td>
</tr>
<tr>
<td>1100</td>
<td>18.57</td>
<td>18.78</td>
<td>0.21</td>
</tr>
<tr>
<td>1101</td>
<td>20.05</td>
<td>20.27</td>
<td>0.22</td>
</tr>
<tr>
<td>1110</td>
<td>21.52</td>
<td>21.73</td>
<td>0.21</td>
</tr>
<tr>
<td>1111</td>
<td>23.00</td>
<td>23.21</td>
<td>0.21</td>
</tr>
</tbody>
</table>
Fig. 5.2 Charge regulation control diagram.
$F_{ic}(s)$ is the control to charge current transfer function derived from fig. 5.3 and given exactly by

$$F_{ic}(s) = \frac{V_{bus} \left[ L_2 C_f s^2 + C_f (R_{batt} + R_{cf}) s + I \right]}{L L_2 C_f s^2 + C_f \left( L (R_{batt} + R_{cf}) + L_2 R_{cf} \right) s^2 + \left( L + R_{batt} R_{cf} C_f + L_2 \right) s + R_{batt}}.$$  (83)

Making the approximation, $R_{batt} \gg R_3$, and neglecting high order terms the following result is given:

$$F_{ic}(s) \approx \frac{V_{bus}}{R_{batt}} \left[ \frac{I}{l + s \left( \frac{L + L_2}{R_{batt}} \right)} \right].$$  (84)

$L$ is the equivalent multi-module inductance and $L_2$ is the inductance of the cable connecting the battery to the converter. This shows that the resulting transfer function can be approximated by a single order term. Fig. 5.4 shows (83) plotted with (84) overlaid. The plots agree up to 10 kHz were the high order terms begin to take effect. The design of the feedback loop is simplified tremendously by this approximation. The current loop is thus given as

$$T_i(s) = F_m F_{ic}(s) R_{iH}(s).$$  (85)
Fig. 5.3 Charge mode control parameters.
Fig. 5.4 Control to charge current transfer function.
At low frequencies where \( T_i(s) \gg 1 \) and the gain of \( H_e(s) \) is unity \( F_i(s) \) simply becomes

\[
F_i(s) = \frac{I}{R_i} \tag{86}
\]

and can be compensated with a simple integrator. The loop gain for charge current control is then

\[
T_{cc}(s) = K_{ic}(s)F_i(s)K_i. \tag{87}
\]

Where \( K_i \) is the gain of the charge current sense network. This result is very convenient for it indicates that the gain crossover frequency and phase margin of the system are practically only dependent on \( K_{ic}(s) \) which is an integrator transfer function with a gain given by

\[
K_{ic}(s) = \frac{s}{RC}. \tag{88}
\]

Fig. 5.5 shows the theoretical loop gain response. The constant -1 slope of the integrator is noted past the crossover frequency. The phase of the loop gain begins to roll-off at approximately 5 kHz indicative of the effects of higher order terms. The phase margin of the loop is practically 85° with a crossover frequency of 1.2 kHz.
Fig. 5.5 Theoretical loop gain response.
5.3 *Bus Voltage Regulation Mode*

Both units share a common bus regulation loop as shown in fig. 4.1. For this reason stability and performance needs to take into account both paralleled units.

### 5.3.1 Small Signal Analysis

Extensive analysis in this mode of operation is given in [11]. Verification of those results will only be given here. The small signal transfer functions in bus regulation mode resemble those in discharge mode given in chapter 4. In CCM the duty cycle to output voltage transfer function derived from fig. 5.3 becomes

\[
F_2(s) = \frac{-V_{bus}}{D} \frac{(1 + R_c C_{bus}) \left( i + s \frac{I_L}{V_{batt}} \right)}{\Delta(s)}
\]  

(89)

where

\[
\Delta(s) = s^2 \frac{LC_{bus}}{D^2} + s \left( \frac{R_{batt}}{D^2} + R_c \right) C_{bus} + \frac{L}{D^2 R_L} + 1, \text{ and}
\]  

(90)

\(L\) is the equivalent multi-module inductance. Both zeros in (89) are located at very high frequencies in the ZVS-BBCD. The ESR zero is located near half the switching frequency due to the low ESR of the polypropylene capacitors. The second zero corresponds to the
RHP zero in discharge mode and as explained in chapter 4 its location is high due to the four modules being in parallel and to the small size of the inductor.

The duty cycle to inductor current transfer function is

\[ F_4(s) = \left( V_{bus} - D R_{bus} I_L \right) \frac{\left( 1 + \frac{s}{\omega_z} \right)}{\Delta(s)} \]  \hspace{1cm} (91)

where

\[ \omega_z = \frac{V_{bus} - D R I_L}{V_{bus} R C_{bus}} \] \hspace{1cm} (92)

This shows a potential problem under some operating conditions. The DC gain of \( F_4(s) \) can be negative. This would cause the zero to shift into the RHP. The frequency of this pole is very low (< 100 Hz) and introduces a -90° phase lag.

5.3.2 Feedback Loop Design

The control designed in chapter 4 for discharge mode must also hold in charge bus regulation mode. This allows a single feedback loop design for both discharge and bus regulation charge modes.
It was shown in [11] that the control to output transfer function with the current loop closed can be approximated by

\[
F_{co}(s) = G_x \frac{(1 + \frac{s}{\omega_1})(1 + \frac{s}{\omega_2})}{(1 + \frac{s}{\omega_x})H_e(s)}
\]  

(93)

where

\[
G_x = \frac{-F_m V_{bus}}{D(1 + G_i) + K_f F_m V_{bus}},
\]

(94)

\[
G_i = \frac{\left(\frac{V_{bus}}{R_i} - DL \right)}{D^2} F_m R_i,
\]

(95)

\[
k_f = \frac{-DR_i}{L_f s} \left(1 - \frac{D}{2}\right),
\]

(96)

and \(H_e(s)\) is as given in chapter 4 with the compensated Q factor. \(\omega_x\) can become a RHP pole under some operating conditions. For large values of \(R_i\), this pole can be approximated to the zero in the duty cycle to inductor current transfer function. In the

5. Charge Mode
case of a multi-module converter $R_i$ is effectively small and so this is not true most of the
time. From [11] $\omega_x$ for this converter is given as

$$\omega_x \approx \frac{l + G_i + K_f F_m \frac{V_{bus}}{D}}{G_i} \frac{G_i}{\omega_z}$$

(97)

which largely depends on $\omega_z$ but is not at the same frequency. Fig. 5.6 shows the
theoretical worst case control to output transfer function at low frequencies. The plot was
made assuming the bus loads were constant power loads and the loads appeared as
negative resistances to the converter. The conditions were 64 V battery, full charge
current (23 A), and full load current with $R_f = -8.8 \Omega$. The plot shows no indication of the
RHP pole. $w_z$ has shifted to the RHP but closing the current loop causes $w_x$ to be in the
LHP due to the low gain of the current sense network $R_i$. A small $R_i$ makes the values of
$G_i$ and $k_f$ small ($< 1$) and negative. Since $w_z$ is negative $\omega_x$ will be positive.

The theoretical control to output transfer functions for a single converter in charge
and discharge modes are shown in fig. 5.7. Both functions match almost identically with a
higher DC gain in discharge mode. The functions are shown for worst case conditions (23 A
charge current and 14 A load current respectively at 64 V battery and an 8.8 $\Omega$ load).
Fig. 5.6 Theoretical control to output function at worst case showing no indication of RHP pole.
Fig. 5.7 Theoretical control to output transfer functions.
Since both zeros of the control to output transfer function are identical in charge and discharge modes the same compensator network can be used. An integrator is used for large DC gain and a zero is set to boost the phase.

Fig. 5.8 shows the loop gain at worst case for two converters paralleled. The system has a 62° phase margin and the theoretical and experimental results match very well.

### 5.4 Performance

As detailed in chapter 4 the gain of the current loop is decreased for two units in parallel. This causes an increase in the bandwidth of the overall system. In chapter four it was shown that the system would still be stable under the abnormal condition of one battery failing. The loop gain crossover was decreased although the phase margin was increased. This condition is normal in charge mode. It occurs when one converter is in constant current mode and the other is in bus regulation mode. The system loop gain becomes the loop gain of a single converter. The loop gain of the converter in constant current becomes an inner loop of the system loop. Stability in this mode is ensured by making both loop gains stable. Fig. 5.9 shows the loop gain for this condition. Superimposed is the loop gain of a single converter in discharge mode from chapter 4.
Fig. 5.8 Outer loop gain for two units in charge mode.
Fig. 5.9 Outer loop gain for one unit in charge bus regulation mode and one in current regulation. Superimposed is the case of one unit in discharge.
Both loop gains are very similar and indicate a stable system. A phase margin of 60° with a crossover frequency of 2 kHz is achieved.

Fig. 5.10 shows the transient response to a step load of 8 A. The top trace is the load current, the middle trace is the bus voltage, and the bottom trace is one of the inductor currents. The result is for both converters paralleled. The maximum transient if of about 700 mV with a settling time of 500 μs. These are very much below specifications. Fig. 5.11 shows the transient response when one converter is in constant current mode and one converter is in bus regulation mode. The transient is of 1 V with a 750 μs settling time. Fig. 5.12 shows the response time in cross-regulation for two paralleled converters between discharge and charge modes. At 10 A load current the units are in discharge mode. At 2 A load they are in charge mode. Both transient peaks show a 700mV peak with a 500 μs settling time.

Fig. 5.13 shows the output impedance for one converter in bus regulation mode and one converter in constant current. The peak output impedance is of -18 dB which is below the specifications. Fig. 5.14 shows the output impedance for two converters operating in bus regulation mode. The peak is of -23 dB. This lower output impedance is expected because of a larger loop gain bandwidth and a better transient response. The output impedance and the peak transient can be related by the following equation.
\[ Z_{opk} = \frac{V_{pk}}{I_{tran}} \]  \hspace{1cm} (98)

where \( I_{tran} \) is the peak transient of the load and \( V_{pk} \) is the peak voltage of the transient.

This equation predicts a peak output impedance of -23 dB for \( V_{pk} = 700 \) mV and \( I_{tran} = 10 \) A.
Fig. 5.10 Transient response to an 8 A load step for two converters in charge mode. Top trace is the load current at 5 A/div, middle trace is the bus voltage (ac coupled) at 1 V/div, and bottom trace is one of the inductor currents at 10 A/div.
Fig. 5.11 Transient response to an 8 A load step for one converter in bus regulation and one in constant charge. Top trace is the load current at 5 A/div, middle trace is the bus voltage (ac coupled) at 1 V/div, and bottom trace is one of the inductor currents at 10 A/div.
Fig. 5.12 Transient response to an 8 A load step in cross regulation mode. Top trace is the load current at 5 A/div, middle trace is the bus voltage (ac coupled) at 1 V/div, and bottom trace is one of the inductor currents at 10 A/div.
Fig. 5.13 Output Impedance for one unit bus regulation and one in charge regulation.
Fig. 5.14 Output Impedance for two units in charge mode.
6. Conclusions

This thesis has presented the design of two high performance, high efficiency ZVS-BBCD units. The efficiency of each unit is excellent. Voltage and current protection schemes make the units reliable and essentially immune to external failures. The gate drives implemented have shown good performance during all modes of operation. Performance results on the testbed have shown excellent dynamics.

The implementation of ZVS-BBCDs into the testbed also shows an overall reduction in weight with respect to separate charger and discharger units. The reduction is due to less magnetic components and a smaller bus capacitor.

The efficiency analysis shows that by using a 16 MOSFET design in the power stage it is possible to increase the light load efficiency compared to an 8 MOSFET design. The efficiency at light discharge load (3 A) and 64 V battery is of 92%. While the peak efficiency at full load, 84 V battery is 97.5%.

Performance characteristics in discharge and charge modes show good results. The output impedance specification is met by using a 500 µF capacitor as opposed to the 2000 µF required when using separate charger and discharger units. The same bus regulation loop
is used in both modes due to the similar small signal characteristics of the ZVS-BBCD during discharge and charge bus regulation.

The technical feasibility of integrating two ZVS-BBCDs into a spacecraft power system is demonstrated in this work. This thesis gives the designer of an actual spacecraft power system another viable alternative for the implementation of the battery charge-discharge circuitry.
References


Vita

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