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MAGAMP POST-REGULATOR APPLIED TO A QUASI-RESONANT CONVERTER AND MAGAMP OPERATION UNDER EXTREME LOAD CONDITION IN A PWM CONVERTER

by

John C. Lee

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APPROVED:

Dr. Dan Y. Chen, Chairman

Dr. Fred C. Lee

Dr. Aicha A. Elshabini-Riad

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(ABSTRACT)

Two issues pertinent to magamp post regulator are treated in this thesis.

One of the issues considered is the operation of a magamp under extreme loading conditions. Practical design equations are derived to allow magamp operation under extreme load conditions such as shutdown of output, foldback of output current and very light load (discontinuous operation).

The other issue considered concerns with magamp post regulation for a quasi-resonant converter. A magamp circuit is proposed, designed and tested for a zero current switching quasi-resonant forward converter. It demonstrates that output regulation in a quasi-resonant converter can be achieved with a fixed switching frequency operation. It also demonstrates the feasibility of multiple regulated output application of a quasi-resonant converter.

Acknowledgements

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I INTRODUCTION

Magamp post regulators have received renewal interest in recent years [1, 13]. The benefits of using a magamp, compared to other post regulator techniques, are numerous: lower parts count, more rugged, more efficient, considerably smaller EMI, and lower stress on the main inverter power inverter power switches. The recent development of low cost, high frequency, square-loop amorphous magnetic materials has made the magamp regulator a preferred solution to many multiple output applications for operating frequencies over 100 KHz.

In this thesis, two issues pertinent to magnetic amplifier post regulator are treated:

1. **Operation Under Extreme Loading Conditions**

The design procedures and equations for a magamp circuit operating under normal load conditions have been discussed in literature [5]. However, extreme load conditions must be taken into consideration in a practical magamp circuit design. Such information is lacking in literature. This issue is treated in this thesis. Practical design considerations and equations are given to allow magamp operation under

extreme load conditions such as shutdown of output, foldback of output current and operation under light load conditions for which the filter choke current is in discontinuous conduction mode. Design guidance and equations are provided for such operation conditions.

2. **Quasi-Resonant Magamp Post-Regulator**

Quasi-resonant DC-DC converters have received tremendous attention in recent years[12]. Because of the unique characteristic of either the zero voltage or the zero current switching of the transistor switch, the converter can be operated at very high frequency without incurring high switching loss. Reduction in physical size of the converter can therefore be achieved. This technology is receiving primary attention of R & D effort in recent years.

As part of the effort that leads to this thesis, a magamp post regulator is proposed and designed for a quasi-resonant forward converter circuit to demonstrate the feasibility of a multiple output quasi-resonant regulators. It is also demonstrated that output regulation of a quasi-resonant converter can be achieved with a fixed switching frequency which is an advantage over the variable frequency regulation scheme normally used in quasi-resonant converters.

In the thesis, Chapter II gives a brief review of magamp post regulator operation with a conventional pulse-width-modulated converter circuit. This serves as the basis for the description of Chapters III & IV. Chapter III provides the magamp design guideline and equations for magamp operations under extreme loading conditions. Chapter IV describes a magamp circuit operating with a quasi-resonant forward converter. Chapter V concludes the work and describes future work. Because of a

number of symbol involves, a glossary of symbol is listed in appendix B. Appendix A gives the derivation of the equations used in Chapter III.

II THEORY OF OPERATION OF MAGAMP

Fig. 2.1 shows a PWM-controlled forward converter with a magamp post regulator. The voltage of the main output V'_o is regulated by the duty cycle control of the main power switch Q. The voltage of the magamp output V_o is regulated through a magamp reset control circuit which controls the operation of the saturable reactor (S.R.). S.R. functions as a switch. At its high impedance state, input power is blocked from the output by the S.R. and the output current freewheels through diode D_2. At its low impedance state, input power transmits through S.R. to the output. L and C are used to smooth out the PWM waveform across D_2. By controlling the duty cycle of S.R., V_o can be regulated against load variation.

In this chapter, a detailed operation of magamp is described using a PWM-controlled forward converter circuit for illustration. In chapter IV, a quasi-resonant forward converter with a magamp output will be described.

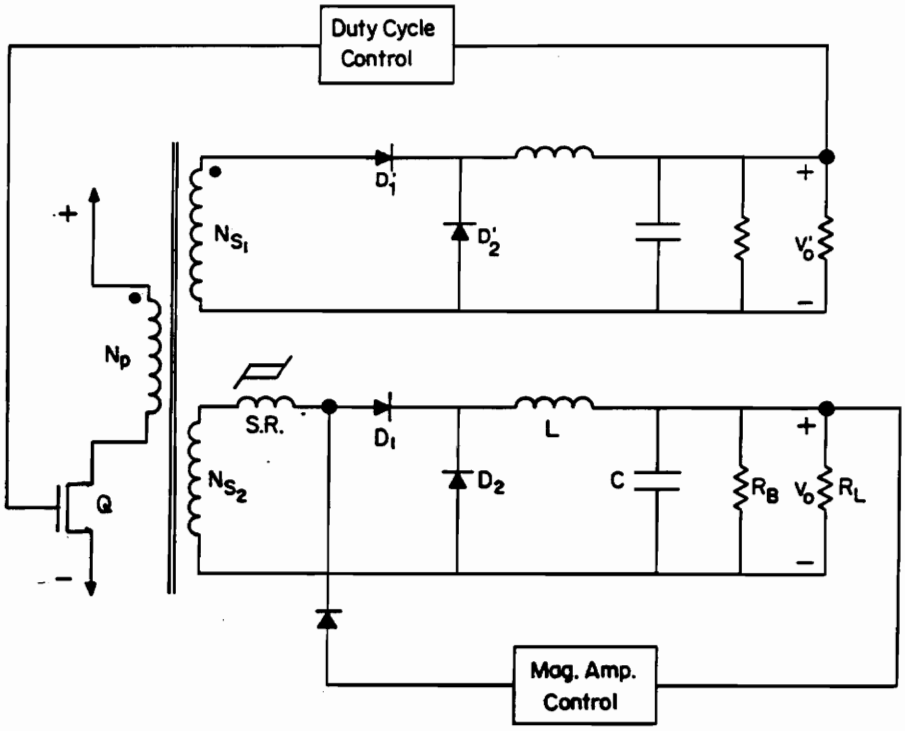


Fig.2.1 PWM Forward Converter with a Magamp Controlled Output.

2.1 Magamp Switching Cycles

To understand magamp circuit operation, attention should be focused on the operation of the S.R.. For the purpose of simplicity, the hysterisis loop of the S.R. is assumed nearly rectangular with large slope of the vertical portion as shown in Fig. 2.3. The switching cycle of the S.R. can be categorized into four intervals: (1) Blocking Interval (2) Conduction Interval (3) Reset Interval and (4) Under Excited Interval. The detail of each interval will be described below.

2.1.1 Blocking Interval

During this interval, the operating point is at the vertical portion of the S.R. dynamic loop (dynamic segment AB in Fig. 2.3). Because of the assumption of squareness of the loop, S.R. acts as an infinite inductor with very little leakage current. Therefore voltage across the secondary winding $V_{N_{S_2}}$ is dropped across S.R.. Diode D_2 freewheels with load current and the voltage across V_{D_2} in this period is therefore essentially zero (a diode voltage drop) and the input power is blocked from the output. The time interval of blocking state in Fig. 2.2 is governed by Farady's Law

$$t_x = \frac{N\Delta\phi}{V_{N_{S_2}}} \tag{2.1}$$

where N is the number of turns of magamp, $V_{N_{S_2}}$ is the voltage across secondary winding. $\Delta\phi$ is the total flux excursion between points B and A. By controlling point

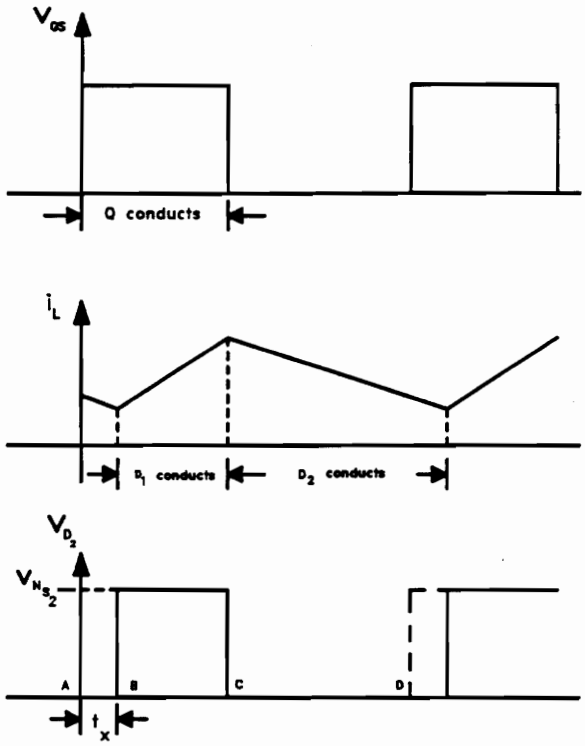


Fig. 2.2 Voltage Waveforms across Diode D_2

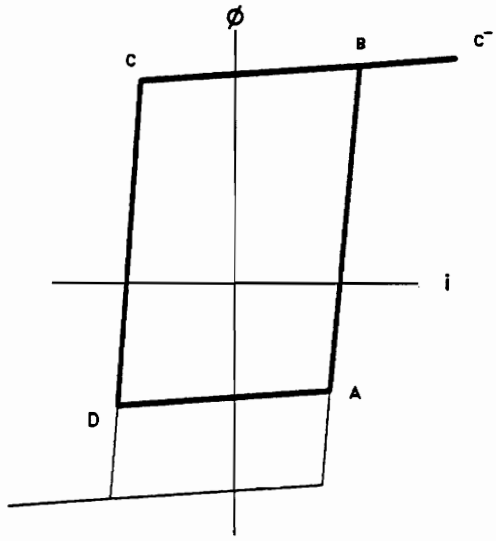


Fig. 2.3 Idealized Hysterisis Loop of S.R.

D through the reset circuit, t_x can be controlled and the output voltage V_O can be regulated.

2.1.2 Conduction Interval

Conduction interval is the period which the flux is at saturation value which corresponds to segment BC^- in Fig. 2.3. Since $\frac{d\phi}{dt}$ is zero at saturation, the voltage across S.R. is $V_{SR} = N\frac{d\phi}{dt} = 0$ which means the reactor is effectively a short circuit. Load current magnitude determines the position of point C^-. The saturation interval will last until the S.R. is reset by control circuit. During this period, diode D_1 conducts and diode D_2 cuts off. The voltage across D_2 is approximately $V_{N_{S_2}}$, neglecting diode voltage drop of D_1. Therefore the voltage across D_2 is a pulse-width modulated waveform as shown in Fig. 2.2. The output voltage V_O is the average of V_{D_2} waveform. Therefore, by controlling the blocking interval duration, the output voltage V_O can be regulated.

2.1.3 Reset Interval

At the end of conduction interval, Q_1 cuts off that forces D_1 "off" and D_2 "on". During this period (segments C^-BC and CD), the S.R. is reset to point D by the reset control circuit. The amount of current reset determines the flux level of point D which determines the duration of the next blocking interval. For a large reset current, the larger the flux reset is and the longer the blocking duration t_x is.

2.1.4 Under-Excited Interval

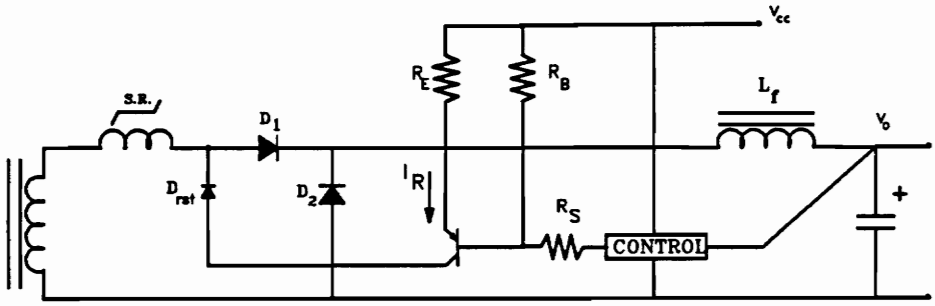
Under-excited interval is the period when the flux is at undersaturation value and the magnetizing force is smaller than the coercive force. The horizontal segment 'DA' in Fig. 2.3 represents this interval. The S.R. is also short circuit because of $\frac{d\phi}{dt}$ is zero. The interval will be ended when the voltage across S.R. is made non-zero. The response of the circuit in this period depends on other circuit elements in the magamp circuit.

2.2 Magamp Reset Circuits

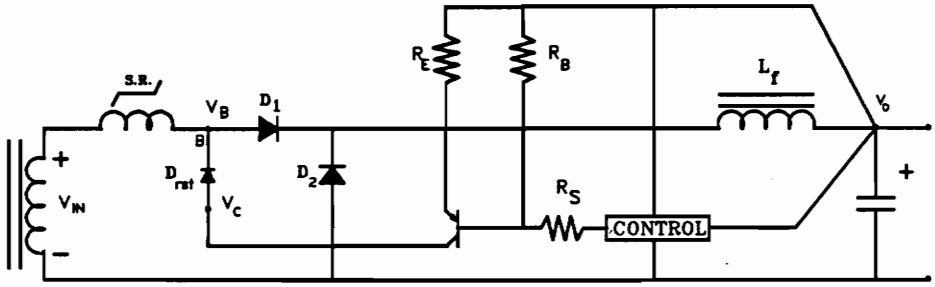
Reset circuit determines the flux reset level of the S.R. during each reset interval described earlier. Two commonly used reset circuitries are shown in Fig. 2.4, a voltage reset and a current reset circuit. Current reset approach is more common than a voltage reset since it introduce less phase delay than the voltage reset approach[14]. The operation of the two circuits are briefly explained in the following paragraphs.

2.2.1 Voltage Reset Circuit

In the voltage reset circuit, Fig.2.4(b), the voltage V_B is equal to $V_C - V_{D_{rst}}$ during the reset interval when diode D_{rst} is conducting. The flux reset, Fig. 2.5, can be expressed in terms of reactor parameters by using Faraday's Law



(a)



(b)

Fig. 2.4 Methods of Magamp Reset Circuits (a) Current Reset (b)Voltage Reset.

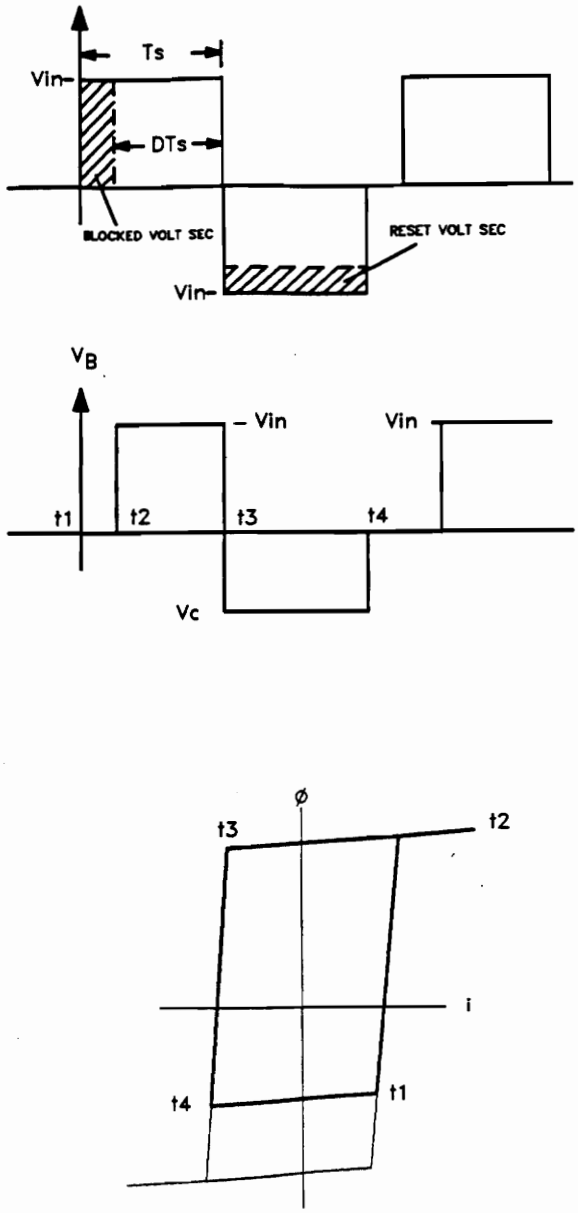


Fig. 2.5 Typical Waveforms for Voltage Reset Circuit.

$$(V_{IN} + V_C)T_S = NA_e\Delta B_{Down} \tag{2.2}$$

where

V_{IN} is secondary winding voltage

V_C is the control voltage

T_S is the switching period

N is winding turns

A_e is the cross section area of S.R.

ΔB_{Down} is the flux swing in reset period.

During the period of blocking, the whole secondary winding voltage V_{IN} is applied across the reactor. Therefore the flux change during this period ΔB_{UP}

$$\Delta B_{UP} = (t_2 - t_1)\frac{V_{IN}}{NA_e} \tag{2.3}$$

At steady state $\Delta B_{UP} = \Delta B_{DOWN}$. Since $V_O = DV_{IN}$, solve for D

$$D = \frac{(V_C - V_{D_{rst}})}{V_{IN}} \tag{2.4}$$

where $V_{D_{rst}}$ is the voltage drop across the reset diode.

The voltage regulation is accomplished through the automatic adjustment of D (duty ratio) of the reset circuit. Assuming a constant input voltage, if for some reason the output voltage is higher than the desired regulated voltage, then D should decrease from Eq.(2.4) which means the voltage at the point of V_B is higher in magnitude. A large voltage therefore drives the flux level down further which means the blocking interval in the next cycle is longer in duration and therefore reduces the

volt-second across the diode D_2. The average output voltage is therefore pulled down to the desired voltage level.

Feedforward Mechanism

If the input voltage V_I changes, the duty ratio D is changed automatically according to Eq.(2.1). If V_{IN} increases, D decreases but the volt-sec. of the voltage across diode D_2 remains the same and therefore the output voltage V_O is still regulated.

2.2.2 Current Reset Circuit

In the current reset circuit shown in Fig. 2.4(b), the reset current I_R is proportional to $V_O - V_{REF}$ as shown in Eq.(2.5)

$$I_R = K(V_O - V_{REF}) \tag{2.5}$$

where

I_R is the reset current

K is the error voltage to reset current gain

V_{REF} is the reference voltage in the compensator.

This relationship can be obtained by using the equivalent circuit shown in Fig. 2.4. It can be seen from this equation that as V_O increases, I_R increases in magnitude which forces the operating point in hysterisis loop further to the left as depicted in Fig. 2.3. This increases the blocking period in the next cycle and pulls down the average output voltage V_O. From this explanation, it can be seen that the incremental permeability of the saturable reactor core strongly affects the gain of the feedback loop.

The feedforward mechanism described in the voltage reset circuit section applies equally well in the current reset circuit. The main difference between the two reset circuit is during the reset interval. During the blocking interval, both circuits operates similarly, and feed forward action occurs during the blocking period.

III PRACTICAL DESIGN CONSIDERATIONS TO ALLOW OPERATION UNDER EXTREME LOADING CONDITIONS

3.1 Introduction

The design of the saturable reactor S.R. affects the circuits' performances such as the regulating range, the core losses of the saturable core, reactor magnetizing or resetting current and the size of the bleeder resistor,R_B. Use of a bleeder resistor is often necessary for the regulator to operate properly under light load conditions. The design equations and procedures for a normal operating mode under continuous-conduction conditions have been given in literature[5]. The objective of the present chapter is to establish practical design equations and guidelines to allow magamp operation under extreme loading conditions. Three conditions are considered:

1. Operation under light load conditions for which the current in the output choke is discontinuous but the output voltage is still regulated; the considerations of the design of the magamp for discontinuous mode are different.

2. Foldback of the output current (a current limit under an external short circuit which can occur deliberately during manufacturing tests or accidentally during system installation); in other applictions, one of the magamp outputs may need to be capable of limiting the output current when the load is shorted (Foldback of the Output Current).

3. Shutdown of output (output voltage deliberately shorted by an internal active switch and no power is delivered to the load); in some multiple output applications, one of the magamp outputs may need to be shut down while other outputs remain unchanged.

Each of these conditions will be discussed in this chapter. Of main concern in this chapter is the flux variation of the saturable reactor.

3.2 Magamp Operation Under Discontinuous Mode of Operation

Figure 3.1 shows the waveforms of the magamp circuit and the associated state of the reactor for both the continuous and discontinuous operation mode. In both cases, t_x is the time during which the magnetic switch is "OFF". The period during

which the magnetic switch is "ON" and the input to output power transfer occur is t_{on}. During the rest of the period (t_{off} in the case of continuous mode and $t_{off1} + t_{off2}$ in the case of continuous mode), diode D_1 is cut off and the magnetic switch is reset by the magamp feedback control.

Generally speaking, the greater the volt seconds needed by the reactor to block during the "OFF" state, the larger the reactor's size is. From the waveform, it is clear that in the case of total output shut down, the reactor must be capable of blocking the voltage across N_{S_2} for the entire duration of Q conduction time $t_{on,semi}$. It is also important to notice that under identical circuit conditions a discontinuous mode. This can be seen from Fig.3.1(a); the i_L waveform in which t_x during discontinuous mode is longer than a corresponding t_x during continuous mode.

3.2.1 Flux Density of Operating Saturable Reactor

A set of relationships exists in magamps that must regulate at light loads, in the region where the filter inductor current is discontinuous. Of particular interest is the dependence of ΔB upon the value of filter inductor L, the load output power P_o and the power dissipation of bleeder resistor P_B. Such a relationship is very useful in determining the trade off among the three design variables: saturable reactor core loss, filter inductance and the value of the bleeder resistor. These relationship are given in Eqs.(3.1), (3.2) and (3.3).

$$(\Delta B)_{cont} = \frac{V_x T}{N A_e} \left(\frac{t_{on,semi}}{T} - \frac{V_O + V_D}{V_X} \right) \times 10^8 \tag{3.1}$$

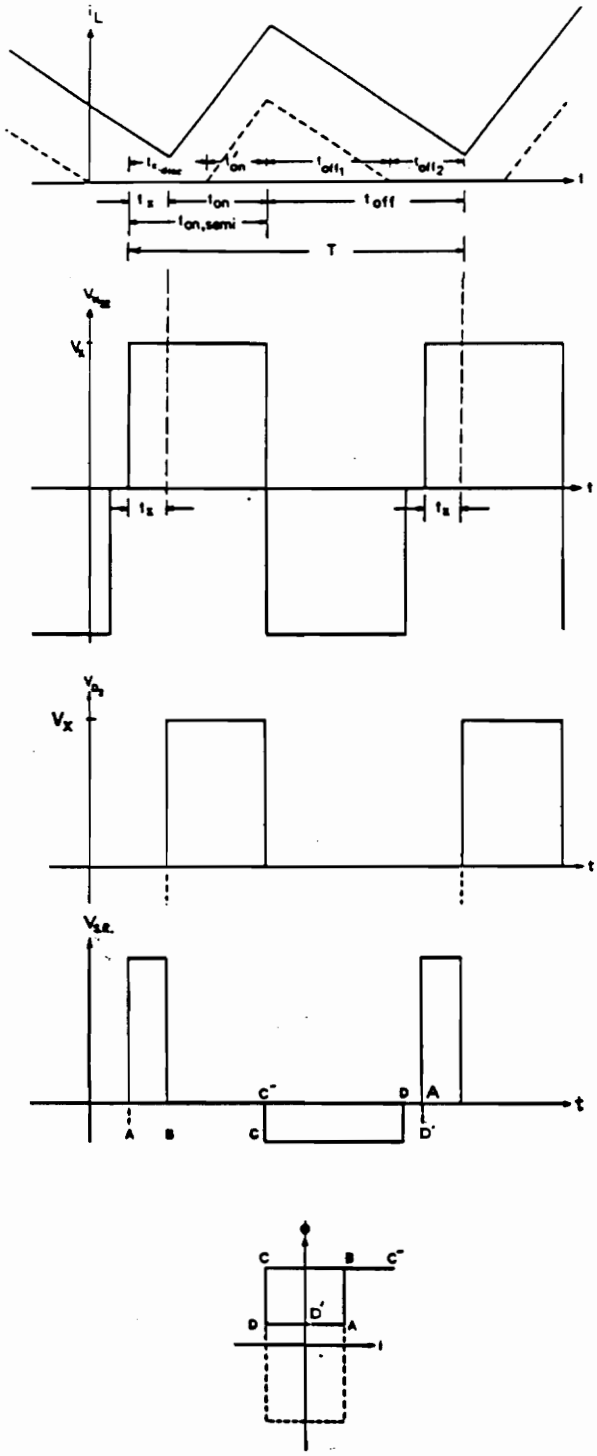
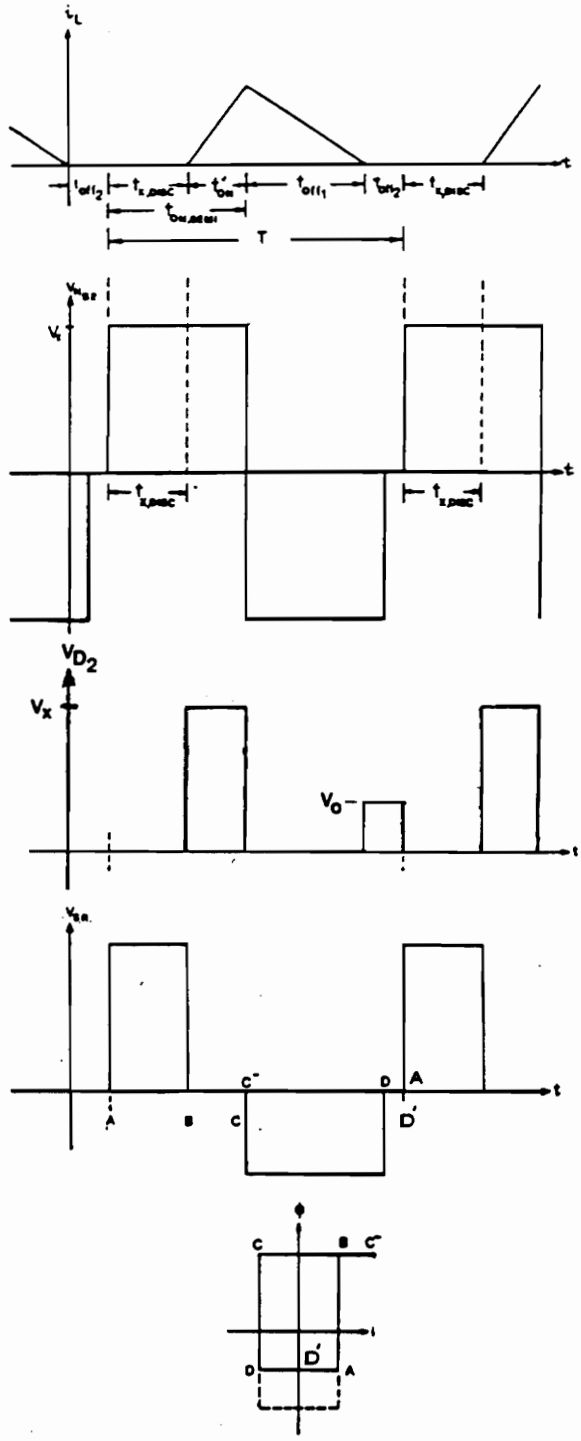


Fig.3.1 (a). Waveforms of the MagampCircuit for Continuous Mode of Operation. The Dotted Waveform for i_L is for Discontinuous Mode of Operation



(b). Waveforms of the Magamp Circuit for Discontinuous Mode of Operation

III PRACTICAL DESIGN CONSIDERATIONS TO ALLOW OPERATION UNDER EXTREME LOADING CONDITIONS

$$(\Delta B)_{disc} = \frac{V_X - V_O - V_D}{NA_e \times 10^{-8}} \left[\frac{V_O + V_D}{V_X} T - \sqrt{\frac{2LT(P_O + P_B)(V_O + V_D)}{V_O(V_X - V_O - V_D) - V_X}} \right] \tag{3.2}$$

$$(\Delta B)_{tot} = (\Delta B)_{cont} + (\Delta B)_{disc} \tag{3.3}$$

It is important to recognize how the three equations can be used. Eq. (3.1) can be used to calculate the flux swing of the reactor for a continuous mode operation. Eq. (3.2) can be used to calculate the additional flux density swing (on top of $(\Delta B)_{cont}$) required for a discontinuous mode operation. Therefore, to obtain the total reactor's flux density swing in a discontinuous mode of operation, Eq.(3.3) is needed. It can be seen from Eq. (3.2) that the use of a bleeder resistor reduces the flux swing, and therefore the power losses of the reactor. A practical way to determine if the filter inductor operates in discontinuous mode is to calculate the difference inside the brackets of Eq. (3.2). If the difference is a positive number, then the inductor is in discontinuous mode. In other words, if the following inequality is met, then the inductor is operated in discontinuous mode[8].

$$\left(\frac{V_O + V_D}{V_X}\right) T > \sqrt{\frac{2LT(P_O + P_B)(V_O + V_D)}{V_O(V_X - V_O - V_D) - V_X}} \tag{3.4}$$

A detailed derivation of Eqs. (3.1), (3.2) and (3.3) is given in the Appendix. Numerical examples will be given below to illustrate the use of these equations.

3.2.2 Design Considerations for Discontinuous Mode -- Numerical Example

Assume a 40V transformer secondary output is regulated at 12V by using a magamp in a 50 kHz forward converter. The saturable reactor is a Mag. Inc. 50B11-1D core with 30 turns. (Cross section is 0.038 cm^2 .) L is 300 μ H. Maximum allowable flux swing $(\Delta B)_{max}$ is 12,000 G. The main power transistor's switching duty ratio is 0.4.

a) What bleeder resistor is needed if the output is to remain at 12V with no load?

b) If the minimum output power is 1 W and the output voltage is still regulated at 12V, is a bleeder resistor needed? If so, determine the bleeder resistance and power dissipation.

c) If the number of turns of the reactor is 24, repeat Question a).

Solution:

Using Eq. (3.1), calculate $(\Delta B)_{cont}$

$$(\Delta B)_{cont} = \frac{40 \times 2.0 \times 10^{-5}}{30 \times 0.038} \left(0.4 - \frac{13}{40}\right) \times 10^8$$

$$= 5088 \text{ G}$$

This is the minimum flux density swing required to regulate the output voltage at 12V whether the inductor operates in continuous or discontinuous mode. If it is the latter, additional flux swing is required.

a) At no load, $P_o = 0$. A bleeder resistor is needed for proper operation. If the bleeder resistance is relatively small, then the circuit may operate in continuous mode and the reactor flux density swing is unchanged at 5088 G. Otherwise, the circuit operates in discontinuous mode and additional flux swing is required. The maximum flux density left is 12000 - 5088 = 6912 G. Using Eq. (3.2) and setting $(\Delta B)_{disc}$ = 6912 G, solve for P_B.

Set

$$6912 = \frac{(40-12-1)\times 10^8}{30\times 0.038}\times$$

$$\left[\left(\frac{12+1}{40}\right)(2.0\times 10^{-5}) - \sqrt{\frac{2(300\times 10^{-6})(2.0\times 10^{-5})(0+P_B)(12+1)}{12\times 40\times(40-12-1)}}\right]$$

$P_B = 1.06\text{W}$

$R_B = 135.8\Omega$

b) Using Eq.(3.4) to check if the circuit operates in discontinuous mode.

L.H.S. of Eq.(3.4) $= \frac{12+1}{40}\times 2.0\times 10^{-5} = 6.5\times 10^{-6}$

R.H.S. of Eq. (3.4)

$$= \sqrt{\frac{2\times 300\times 10^{-6}(2.0\times 10^{-5})(1.0+0)\times(12+1)}{12\times(40-12-1)\times 40}}$$

$$= 1.2\times 10^{-11}$$

Since (L.H.S.) > (R.H.S.), Eq.(3.4) is met and, consequently, circuit is in discontinuous mode. Without using a bleeder resistor, (ΔB_{disc}) is calculated from Eq.(3.2) as follows.

$$(\Delta B)_{disc} = \frac{(40-12-1)\times 10^8}{30\times 0.38}\times$$

$$\left[\left(\frac{12+1}{40}\right)\times 2.0\times 10^{-5} - \sqrt{\frac{2\times 300\times 10^{-6}\times 2.0\times 10^{-5}\times 0\times(12+1)}{12\times(40-12-1)\times 40}}\right]$$

$$= 15395 \text{ Gauss} > 6912 \text{ Gauss}$$

Therefore, a bleeder resistor is needed if the maximum allowable flux density swing is 12000 G. To limit $(\Delta B)_{max}$ at 12000 G, P_B can be found by using Eq.(3.2) and setting $(\Delta B)_{disc}$ = 6912 G and P_O = 1

$$6912 = \frac{(40-12-1)\times 10^8}{30\times 0.38}\times$$

$$\left[\left(\frac{12+1}{40}\right)\times 2.0\times 10^{-5} - \sqrt{\frac{2\times 300\times 10^{-6}\times 2.0\times 10^{-5}(1+P_B)(12+1)}{12\times 40\times(40-12-1)}}\right]$$

P_B = 2.18W

$$R_B = \frac{12^2}{2.18} = 66.1\Omega$$

By following a similar procedure, one can see the design trade off by allowing $(\Delta B)_{max}$ and /or L to vary. A set of such designs is given in Table I for the case of Part a) (i.e., P_O = 0 watt) in which there is no load. It can be seen from the table that as the value of L or the bleeder wattage decreases, the reactor's core losses increase. The values of the reactor's core losses are calculated by using information given in Ref.[7]

c) If N = 24, then $(\Delta B)_{cont}$ = 6579 G. (From Eq.(3.1).) Following a similar procedure, a set of solutions are given in Table II.

A comparison of Table I and Table II shows that as N is reduced, the bleeder's power increases. In a practical design, N is also limited by other considerations such as core windability, reactor saturable inductance. Design interaction are needed to find the optimum N.

3.3 Foldback of the Output Current

A short circuit across the output could occur during manufacturing tests or accidentally during system installation. A current limit is therefore necessary to protect the circuit. A current limit can be via shutdown of the PWM control or foldback of the magamp. The discussion given here is for the latter case.

Since a short circuit is considered as abnormal condition, the temperature rise of the saturable reactor core can be greater than for output shut down conditions. Thus, in the design, the allowable flux swing for a short circuit can be made somewhat greater than that for shut down.

The flux swing for foldback of the output current is somewhat less than for total shutdown of the output. This is because a small current pulse width is needed to forward bias the output rectifier diode and freewheeling diode. There is also the effect of saturated inductance. A good guideline for the flux swing needed in the core of the saturable reactor to achieve short-circuit protection is

Table 3.1 Bleeder Resistances at $P_o = 0$ under different $(\Delta B)_{max}$; N = 30

$(\Delta B)_{max}$ (Gauss)	$(\Delta B)_{cont}$ (Gauss)	L (μH)	Core loss (Watt)	P_B (Watt)	R_B (Ohm)
6000	5088	300	0.43	3.18	45.3
9000	5088	300	0.92	2.01	71.6
12000	5088	300	1.25	1.11	129.8
14000	5088	300	1.98	0.66	219.6
6000	5088	200	0.43	4.77	30.2
9000	5088	200	0.92	3.02	47.7
12000	5088	200	1.25	0.98	86.5
14000	5088	200	1.98	0.98	146.3

Table 3.2 Bleeder Resistances($P_o = 0$) if N = 24

$(\Delta B)_{max}$ (Gauss)	$(\Delta B)_{cont}$ (Gauss)	L (μH)	Core lossses (Watt)	P_B (Watt)	R_B (ohm)
9000	6579	300	0.92	2.49	57.8
12000	6579	300	1.25	1.47	98.0
14000	6579	300	1.98	0.94	152.9

$$\Delta B \cong K \times \frac{\frac{N_{S_2}}{N_{S_1}}(V'_O + V_D) \times 10^8}{NA_e f_s} \tag{3.5}$$

where K ≅ 0.91 for a 12V magamp output, and

K ≅ 0.85 for a 5V magamp output.

3.4 Output Shut Down

In some power supplies, there may be a requirement to shut down only the magamp output. To achieve this operation, first, the saturable reactor must be converted into an "open" switch state via maximum reset current. If the output voltage is to be less than 0.4V (low level for TTL logic), then a low impedance path in shunt with the output must be provided for the reactors magnetizing current. The latter is easily accomplished by shorting the output with an active load Q_L as shown in Fig. 3.2.

Two design considerations are important in this operation. These are the power losses of the reactor and the power loss associated with the active load Q_L due to the magnetizing current flow of the reactor during blocking. Each will be discussed in the following:

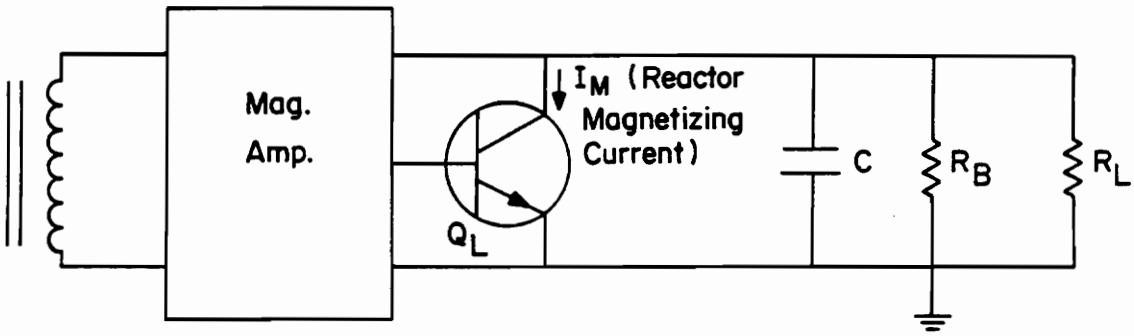


Fig.3.2 Output Shut Down by Using an Active Load Q_L.

3.4.1 Reactor's Flux Swing For Shut Down Condition

In a shut down operation, the reactor must block the entire voltage pulse from the secondary of the power transformer. Using Faraday's law, the following equation can be found

$$NA_e\Delta B = V_x \times t_{on,semi} \times 10^8 \tag{3.6}$$

It can also be written in terms of turns ratio and PWM main output voltage V'_o as follows

$$NA_e\Delta B = \frac{(V'_O + V_D)}{f_s} \times \frac{N_{S_2}}{N_{S_1}} \times 10^8 \tag{3.7}$$

For a given circuit condition, $NA_e\Delta B$ can be calculated from the right hand side of either Eq.(3.6) or (3.7), depending on the known variables. Once the required $NA_e\Delta B$ product has been calculated, some iteration and judgement calls are needed to completely determine N, A_e and ΔB . Normally for a given material and operating frequency, ΔB is limited to a maximum flux swing to avoid large power loss and over heating of the core. Therefore, for a given core and a predetermined ΔB value, N can be found. However, the calculated value of N must be checked with other considerations such as core windability, saturated inductance and reactor's magnetizing current which is to be discussed in the next section. Iteration is therefore needed to design a reactor for output shutdown conditions.

3.4.2 Power Dissipation Requirement of Active Load

When the magnetic switch is "OFF", a magnetizing current exists. Since this current flows through active load Q_L, proper care must be taken to ensure Q_L is capable of handling the power dissipation. The average leakage current, I_{IAVE}, can be calculated by using the following two equations[6].

$$I_{IAVE} \cong K_I H_{RC} \times \frac{L_e}{0.4\pi N} \tag{3.8}$$

$$H_{RC} \cong \frac{K_C \times (Watts/pound\ loss) \times 10^6}{\Delta B \times f_s} \tag{3.9}$$

where K_I is the conduction duty cycle of the main power semiconductor switch Q; H_{RC} is the reset coercive force, and K_c is a constant. For permalloy, $K_c = 1.2$ and for Metglas 2714A, $K_c = 1.05$.

It should be noted that in this discussion, it is assumed that output capacitor C has been discharged before Q_L is turned on. Otherwise, a small resistor in series with Q_L may be required to absorb the transient power. Furthermore, in certain types of magamp reset circuit, the reset current must flow through Q_L under shut down condition. This current must be taken into consideration in determining the total current and the power dissipation of Q_L.

3.4.3 Magamp Design Considerations Under Shut Down Condition--Numerical Example

Assume a 50 kHz forward converter with 9 turns on the power transformer for the 12V magamp output and 3 turns for the PWM controlled 5V output. The conduction duty cycle of the main semiconductor switch is 0.4.

a) What is the minimum turns needed on a Mag. Inc. 50B10-1D core to limit the flux swing at shut down to be less than 10,000 G? Core data: $A_e = 0.076cm^2$, $l_e = 6.18cm$ permalloy.

b) What is the minimum average current bleed through load Q_L for shut down of the output?

Solution:

a) From Eq.(3.7),

$$N = \frac{\frac{N_{S_2}}{N_{S_1}} \times (V'_O + V_D) \times 10^8}{\Delta B \times A_e \times f_s}$$

$$= \frac{\frac{9}{3} \times 6 \times 10^8}{10{,}000 \times 0.076 \times 50{,}000}$$

$$= 47.4$$

Use 48 turns.

b) From the core loss data given in Ref[7], at 50 kHz, and a flux density magnitude of $\frac{10000}{2}$ = 5000 G, there are 110 w/lb loss. From Eqs.(3.8) and (3.9)

$$H_{RC} = 1.2 \times 10^6 \times \frac{110(Watts/pound)}{10{,}000G} \times 50{,}000Hz$$

$$= 0.265 \text{ Oe}$$

and

$$I_{IAVE} \cong 0.4 \times \frac{H_{RC} \times l_e}{0.4\pi N} = \frac{0.4 \times 0.264 \times 6.1}{1.26 \times 48}$$

$$= 10.8 \text{ mA}$$

Average power dissipation is approximately 10.8 mA x 0.2V = 25 mW. A T092 package is adequate to handle the power. In certain types of reset circuits, additional current is provided to the reset circuit, typically in the range of 25mA. This should be added to the I_{IAVE} calculated above if this type of circuit os used.

3.5 Summary

In this chapter, some of the practical design trade-offs encountered in the use of the magamp for extreme operating conditions have been illustrated. Three extreme conditions were considered: discontinuous mode of operation, foldback into output short circuit and output shutdown.

Design equations are derived for the three extreme operations. The use of the equations is illustrated in numerical examples. The design equations provide the

designers with tools for parameter trade offs. Although not done in this chapter the design equations lend themselves to computer search design procedure.

IV Magamp Post Regulator in A Quasi-Resonant Converter

4.1 Introduction

Quasi-resonant converters have received considerable attention for high frequency switching power supply applications [12,15,16]. EMI reduction, fast response and high power density are among the advantages in using such converters. Two types of quasi-resonant converters are classified according to the nature of the transistor switching operation -- zero current switching converter and zero voltage switching converter. In each class of converter, there are two different operation to regulate the output voltage-- full wave operation and half wave operation. In either case, frequency modulation is used to regulate the output. Therefore, conversion switching frequency varies with circuit operating condition. Variable frequency operation is not desirable because the filter components of the converter are not opti-

mized. The filter component size is mainly determined by the lowest frequency of operation.

In this chapter, magamp regulation technique described in Chapter II is applied to a quasi-resonant zero current forward converter. Fig. 4.1 shows the circuit diagram. In the circuit operation, both the switching frequency and the duty cycle of the main transistor Q are fixed by a gate drive circuit. The output voltage regulation is achieved by magamp control. In other words, the pulse-width modulation is accomplished by the "switching" of the S.R. between high impedance state and low impedance state similar to what was described in Chap. II. Referring to Fig. 4.2, V_{D2} waveform is a high-frequency truncated half-wave sinusoidal. The output filter L_f and C_f smoothens out the high frequency ripple. By controlling the duty cycle of the truncated waveform, output DC voltage can be regulated. As a comparison, in a conventional PWM forward converter, the V_{D2} waveform(Fig. 2.2) is a pulse-width-modulated high -frequency square wave.

4.2 Mode of Operation

In this section, operation of the circuit will be described according to the state of the saturable reactor. Fig. 4.2 shows the waveforms and the B-H curve of the saturable reactor. Referring to the figure, operation will be described for five periods that are from T_1 to T_5

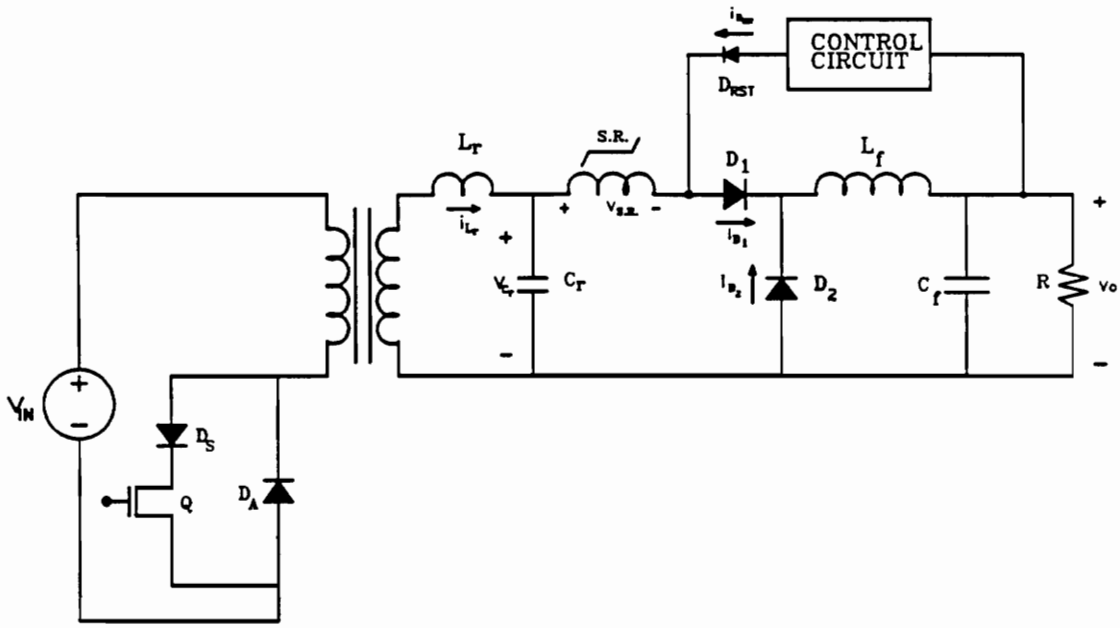


Fig. 4.1 Magamp Applied to Forward Quasi-Resonant Converter.

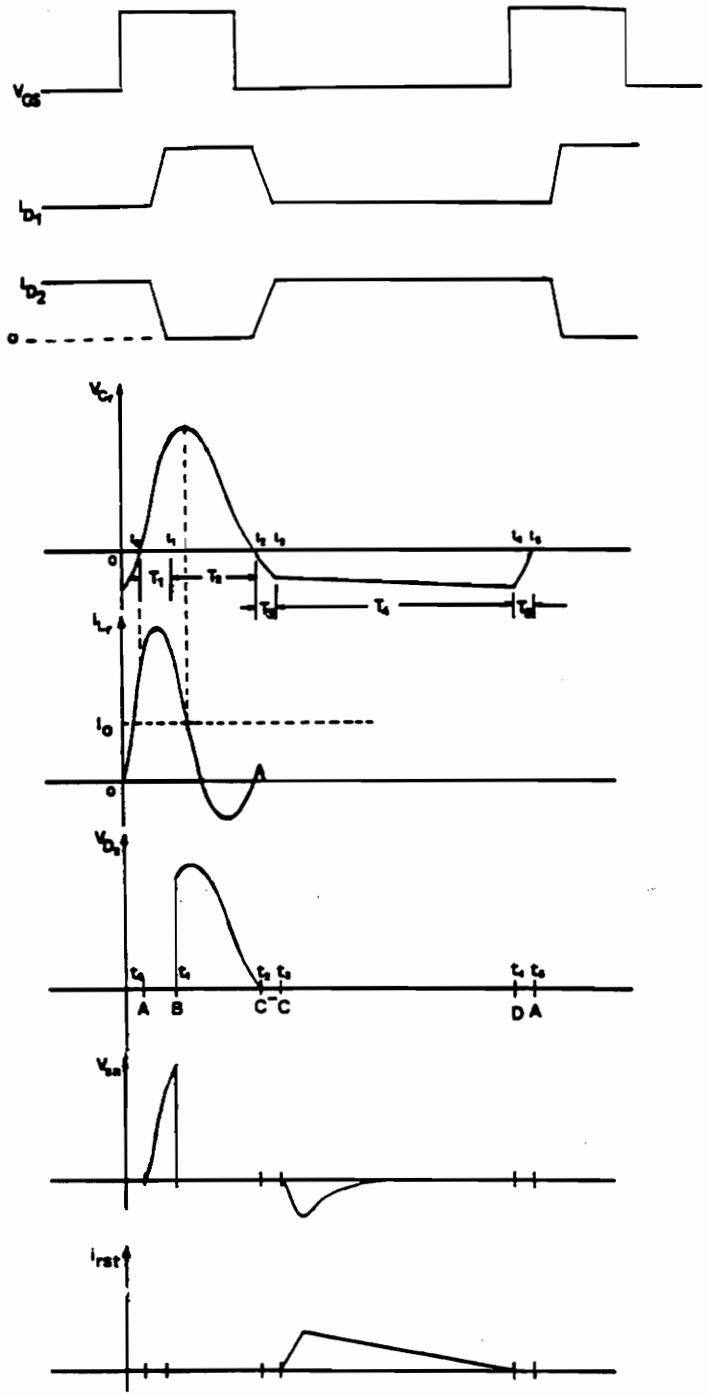


Fig.4.2 (a) Circuit Waveforms of Magamp Controlled Forward Quasi- Resonant Converter.

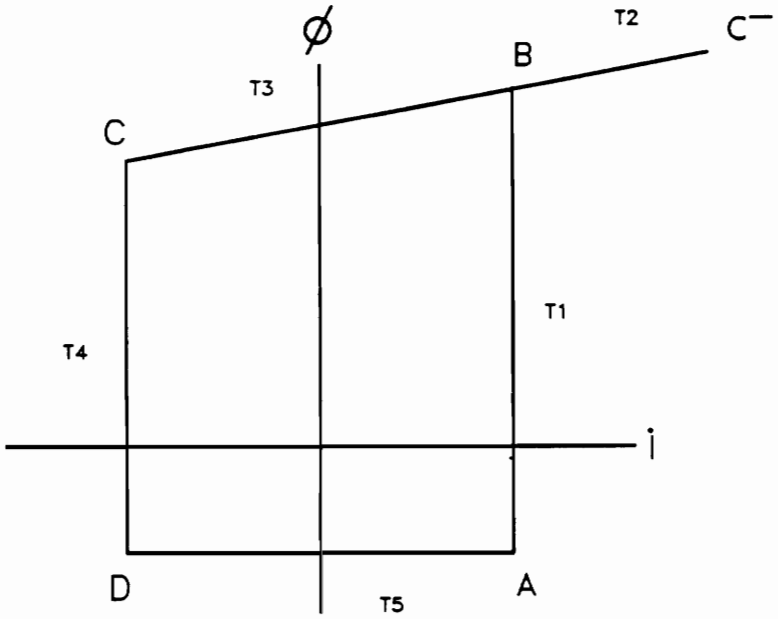


Fig. 4.2(b) Idealized Hysterisis Loop of Magamp Operation in Forward Converter.

4.2.1 Stage T1

During this period, diode D_1 is at 'OFF' state, D_2 is at 'ON' state. Transistor is at 'ON' state. Fig. 4.3 shows the equivalent circuit. The L_r,C_r in resonance and the capacitor voltage V_{cr} is positive. The saturable reactor is at blocking state as indicated by the B-H curve segment DAB shown in Fig. 4.3 (b). The voltage across V_{D_2} is, therefore, zero during this period. The duration of the blocking state T1 is governed by the Faraday's Law and is expressed as followed.

$$\int_0^T V_{Cr} dt = NA_e(B_B - B_A) \tag{4.1}$$

where

V_{cr} is the resonant capacitor voltage,

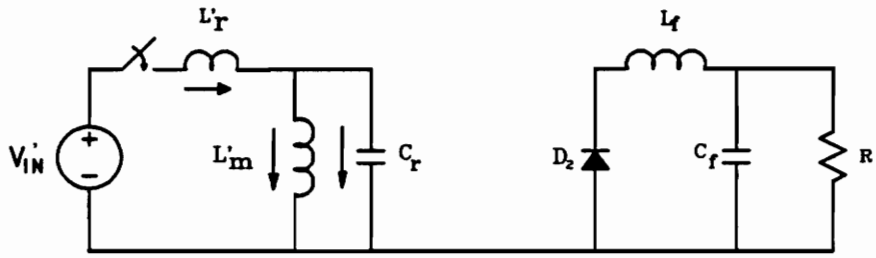
N is the winding turns of S.R.,

B_B is the flux density at point B,

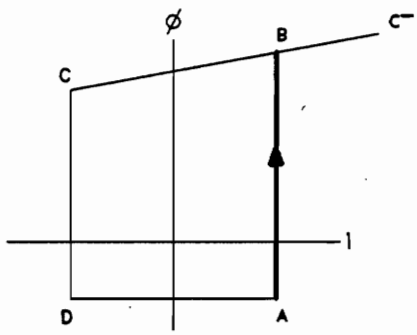
B_A is the flux density at point A.

4.2.2 Stage T2

At the end of T_1, S.R. is forced into saturation as shown in Fig. 4.4(b). Stage T_2 covers the whole period in which flux moves from point B to point C^-. In this period, diode D_1 conducts and D_2 cuts off. Transistor Q_1 is at 'ON' state. Fig. 4.4 shows the equivalent circuit during this period. Capacitor voltage V_{cr} is positive for the whole period. Point C^- is determined by the magnitude of the load current

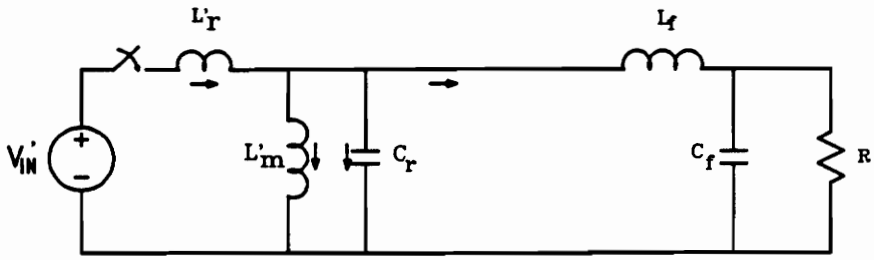


(a)

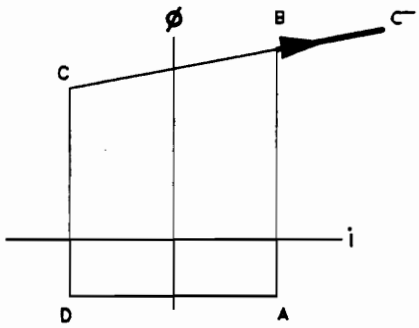


(b)

Fig. 4.3 (a) Equivalent Circuit of Stage T1. (b) Magamp Behavior in Dynamic Hysterisis Loop at Stage T1.



(a)



(b)

Fig. 4.4 (a) Equivalent Circuit of Stage T2. (b) Magamp Behavior in Dynamic Hysterisis Loop at Stage T2.

$(H_{c^-} = \frac{Ni_{load}}{L})$. No reset current is applied through D_{rst} to S.R. during this period.

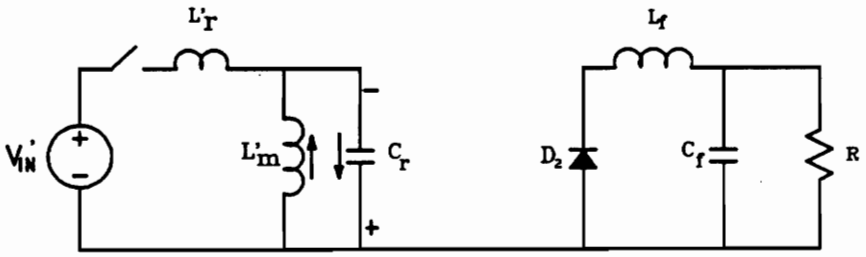
4.2.3 Stage T3

At the end of T_2, V_{cr} starts to become negative which force D_1 to cut off and D_2 to conduct. Fig. 4.5 shows the equivalent circuit. Capacitor is charged to the negative polarity by the magnetizing inductance of the transformer. The flux moves from C^- to C_o.

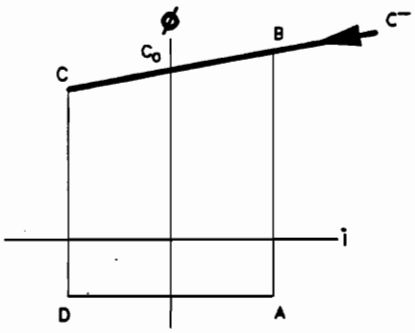
The action of magamp from C^- to C is induced by the decreasing current of i_{D_1}, which makes the voltage across the magamp negative while the decreasing current flows through magamp.

4.2.4 Stage T4

During this period, S.R. is reset through the feedback current i_{rst}. The operating point moves from C_o to D in the B-H characteristics. The amount of reset depends on the magnitude of reset current which depends on the difference between the output voltage V_o and the reference voltage V_R. Fig. 4.6 shows the equivalent circuit. Capacitor voltage V_{cr} is charged to higher negative value by the magnetizing inductance of the transformer. This continues until the transistor turns on again which forces L_r, C_r resonance. Capacitor voltage starts to rise.

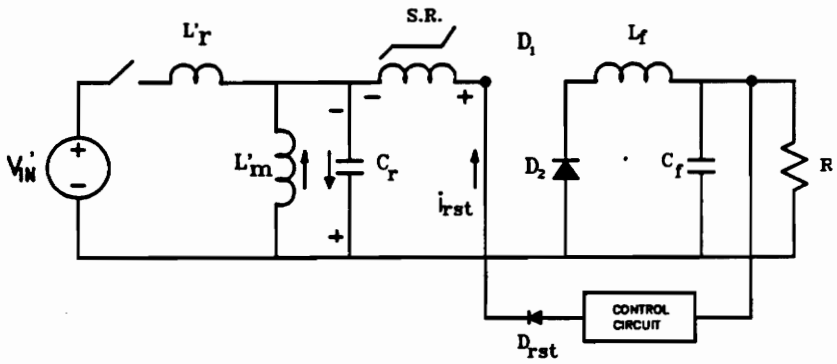


(a)

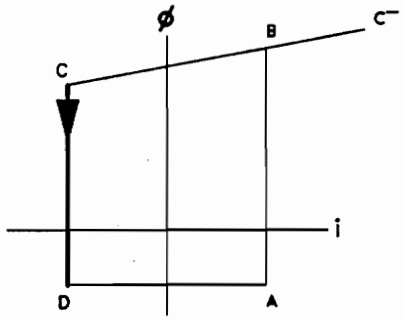


(b)

Fig. 4.5 (a) Equivalent Circuit of Stage T3. (b) Magamp Behavior in Dynamic Hysterisis Loop at Stage T3.



(a)



(b)

Fig. 4.6 (a) Equivalent Circuit of Stage T4. (b) Magamp Behavior in Dynamic Hysterisis Loop at Stage T4.

4.2.5 Stage T5

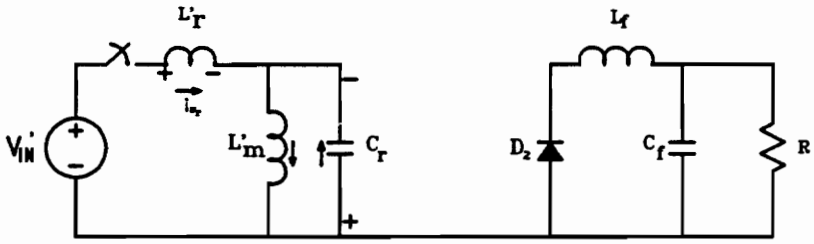
At this stage the switch is on. V_{C_r} is still negative but the current flowing through the resonant capacitor is positive, which means the energy of C_r is dumped to magnetizing inductance of the transformer as shown in Fig. 4.7. The reset current and $V_{S.R.}$ of magamp are zero. The magamp action in B-H loop will be in segment DA. It could stay anywhere in between point D and point A depending the load current through the magamp.

4.3 Quasi-Resonant Converter Circuits Using Magamp Regulation Scheme

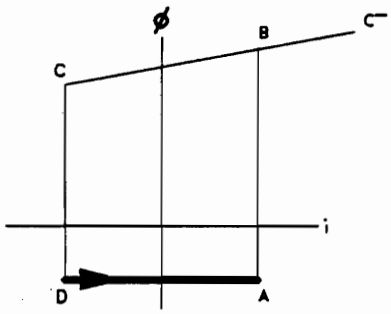
In this section experimental results are given for two circuits. One is the single-output forward quasi-resonant converter. The other circuit is a multiple-output forward quasi-resonant converter.

4.3.1 Single Output Forward Quasi-Resonant Converter Using Magamp Regulator

Fig. 4.8. shows the circuit diagram and the parts number of a single-output

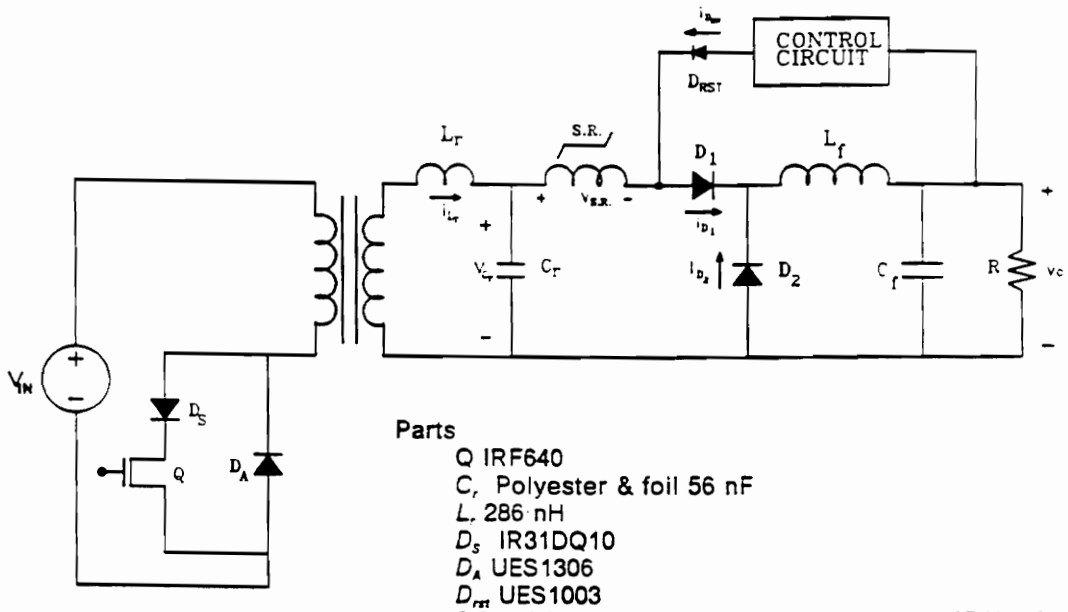


(a)



(b)

Fig. 4.7 (a) Equivalent Circuit of Stage T5. (b) Magamp Behavior in Dynamic Hysterisis Loop at Stage T5.



Parts

Q IRF640
C_r Polyester & foil 56 nF
L_r 286 nH
D_S IR31DQ10
D_A UES1306
D_{rst} UES1003
S.R.1 8 Turns Toshiba Amorphous Core MB15x10x4.5
D_1,D_2 IR31DQ10
Control Circuit UC3838
L_f MPP core 6.7μH
C_f Polyropylene 8.5 μF
Transformer 8/3T TDK H7C4 5901

Fig.4.8 Application of Magamp to Single Output Forward Quasi- Resonant Converter.

quasi-resonant forward converter with magamp as the regulator. The main power circuit is a full-wave zero current forward quasi-resonant converter which is operated at a fixed frequency of 500kHz. The duty cycle of the main power MOSFET Q is fixed at approximately 30%. The output voltage is regulated at 5V by a magamp post regulator. In using this regulation scheme, the quasi-resonant converter can be operated in a constant frequency mode. Fig. 4.9 shows the experimental waveforms.

4.3.1.1 Description of Control Circuit

Unitrode chip UC3838 was used in the control circuit. This chip contains two high-gain op amps and a high-gain PNP-equivalent current source which can deliver up to 100mA of reset current. Fig.4.10 shows a typical application of this chip in a circuit using PWM control scheme. The op amp with C/L is for current limit which was not used in this experiment. Only the op amp with E/R was used for voltage regulation. Application of this chip to quasi-resonant circuit is similar.

4.3.1.2 Design of Saturable Reactor S.R.

The design of saturable reactor for magamp application to a PWM converter has been reported[5].

$$\Delta B = \frac{T(V_s - (V_O + V_d))x10^8}{NA_e} \tag{4.2}$$

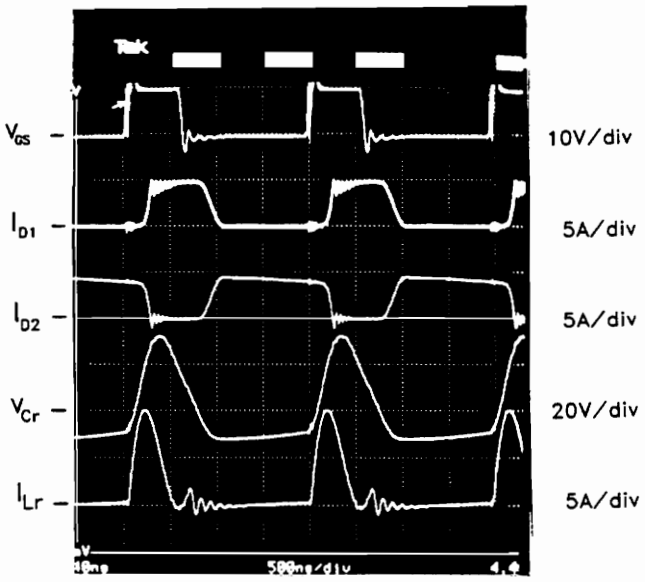


Fig.4.9 Experimental Waveforms of i_{Lr}, I_{D1}, I_{D2} and V_{Cr}.

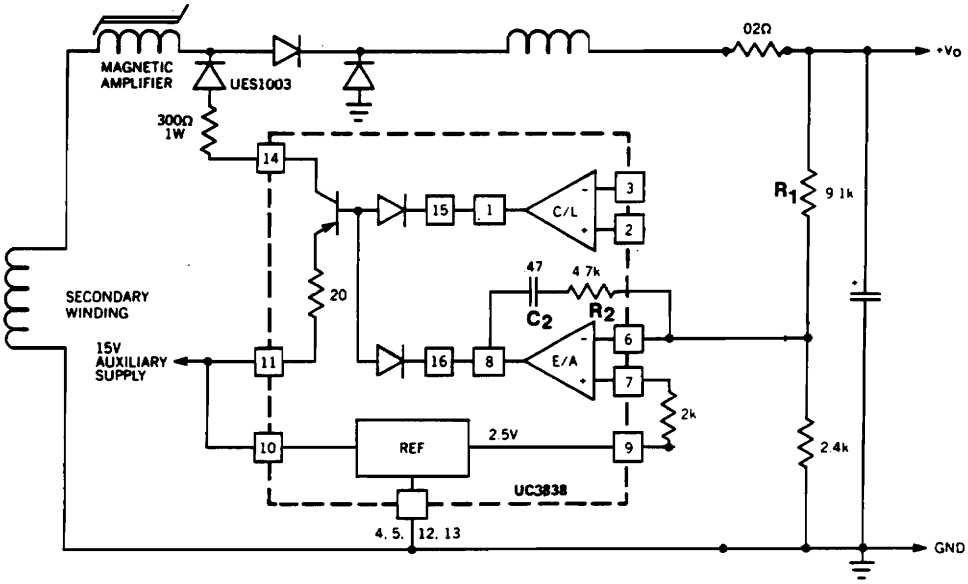


Fig.4.10 Application of UC3838 to Regulating Secondary Output.

Basically Eq.(4.2) relates the flux density of the core to circuit input and output condition. The same equation can be used to design the S.R. for a magamp used in a quasi-resonant forward converter. This will be explained below.

The key question can be more specifically stated as follows:

If

$$V_{O_{PWM}} = V_{O_{QRC}}$$

$$V_{I_{PWM}} = V_{I_{QRC}}$$

$$P_{O_{PWM}} = P_{O_{QRC}}$$

$$f_{S_{PWM}} = f_{S_{QRC}},$$

is the S.R. used in QRC converter under heavier stresses than the S.R. used in a conventional PWM converter? This question can be answered by comparing the flux swing in the S.R. and the rms current of the winding:

Flux swing: flux swing ΔB should be the same.

This is explained below. Referring to Fig. 4.11, V_{D2} waveforms for both QRC and PWM converters. V_O is the average of the total volt-second over the entire period. Since $V_{O_{QRC}}$ is assumed to be the same as $V_{O_{PWM}}$ it is concluded that the

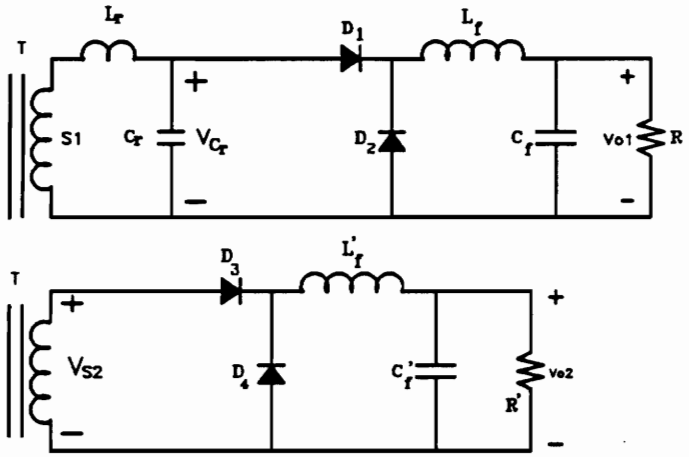
(total volt-second of $V_{D2_{QRC}}$) = (volt-second of $V_{D2_{PWM}}$)

which means

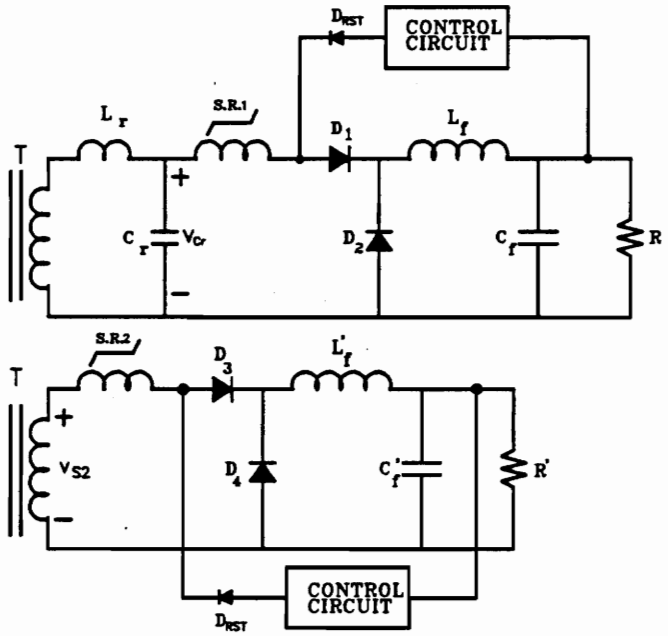
(volt-second of V_{Cr} (positive going part of QRC)) = (volt-second of V_{S2} (PWM))

If the saturable reactor is inserted as shown in Fig.4.11(b), then the "volt-sec" S.R. blocks in each cycle should be equal to the difference of the volt-sec between waveforms in part Fig.4.12 (b) and (c). In other words,

volt-sec of S.R. in QRC = (volt-sec of "+" part of V_{Cr})- (volt-sec of V_{D2} (QRC))



(a)



(b)

Fig. 4.11 Secondary Side of Forward QRC and Forward PWM Converter (a) Without Magamp (b) With Magamp.

and

(volt-sec of S.R. in PWM) = (Volt-sec of V_{S2}) - (volt-sec of V_{D2} (PWM))

Since the first term

volt-sec of V_{Cr} = volt-sec of V_{S2}

and

volt-sec of V_{D2}(QRC) = volt-sec of V_{D2}(PWM)

therefore,

Volt-Sec of S.R. in PWM = Volt-Sec of S.R. in QRC

From the argument given above, the same design equation and design procedure developed for PWM is applicable to QRC case.

In this design, a Toshiba amorphous core MB15x10x4.5 was used.

4.3.1.3 Measurement Results of Regulation of Single Output

Regulation against Input Voltage Variation

The results below showed the regulated output voltages of 5V with different loads at fixed input voltages of 70V and 80V respectively. Table 4.1 and Table 4.2 showed the results of regulation. Only those results within $\pm$5% change of the reference output voltage of 5V were recorded.

The regulation range was from 5A to 70mA for input voltage of 70V. Those for 80V input voltage the regulation range was from 5A to 65mA.

Regulation against Output Load Variation

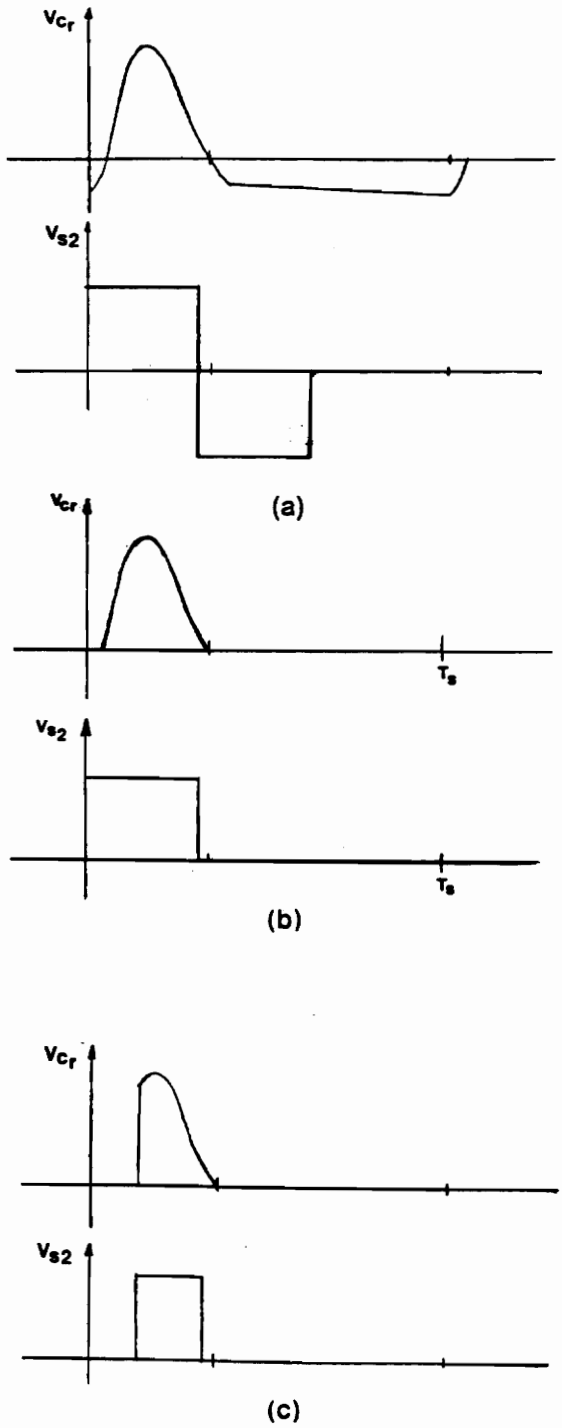


Fig.4.12 Waveforms of (a)V_{Cr} and V_{S2} without magamp (b) Positive V_{D2} and V_{S2} without magamp (c) V_{D2} and V_{S2} with magamp added.

Table 4.1 Regulation Against Load Change ($V_{in} = 70V, V_{Oref} = 5V$)

Regulation Range (Amp)	Output Voltage (Volts)	Load Resistance (Ohm)	± % Change
5.000	5.00	1	0.0
1.004	5.02	5	0.4
0.566	5.09	9	1.8
0.269	5.11	19	2.2
0.174	5.05	29	1.0
0.099	4.88	49	-2.4
0.070	4.89	69	-2.2

Table 4.2 Regulation Against Load Change ($V_{in} = 80V, V_{Oref} = 5V$)

Regulation Range (Amp)	Output Voltage (Volts)	Load Resistance (Ohm)	± % Change
5.000	5.00	1	0.0
1.010	5.05	5	1.0
0.568	5.11	9	2.2
0.270	5.14	19	2.8
0.126	4.92	39	-1.6
0.083	4.92	59	-1.6
0.071	4.95	69	-1.0

The results below showed the regulated output voltage when the loads were 1Ω, 5Ω and 16Ω as shown in Table 4.3, Table 4.4 and Table 4.5. When the fixed load increased in each case, the input voltage range dropped because the energy pumped to the output decreased.

4.3.1.4 Measurement Results of Step Change of Load

Fig.4.13 shows the measured control to output Bode plot. A crossover frequency of 23kHz(4.6% f_s) was chosen. A PI controller with zero at 15kHz and a gain of -5.7dB were used in the compensator.

The step response of the output to a step load change of 3.2A(64% change out of 5A) is shown in Fig. 4.14. The settling time is approximately 300 μs with a 300mV voltage change.

The reason of using PI controller is that the regulation of output is easy to achieve. But it has a disadvantage that the input voltage range or the load range for the output to be stable is small. This is because the crossover is at -2 slope which means the phase margin is very small at crossover frequency.

4.3.1.5 Measurement of Efficiency

The efficiency of the quasi-resonant forward converter with magamp control is measured at full load and half load. At full load the efficiency of the circuit is 77.3% ($V_{in}xI_{in}$ =60.7V x 0.52A = 31.56W, V_oxI_o = 4.94Vx4.94A = 24.4W). At half load the efficiency of the circuit is 60.2% ($V_{in}xI_{in}$ =55.0V x 0.37A = 20.3W, V_oxI_o = 4.94Vx2.47A =

Table 4.3 Regulation Against Input Voltage (R = 1 Ω)

Input Voltage (Volts)	Output Voltage (Volts)	± % Change
60.0	4.99	-0.2
66.0	5.00	0.0
70.0	5.00	0.0
74.5	5.00	0.0
80.0	5.01	0.2
90.0	5.02	0.4

Table 4.4 Regulation Against Input Voltage ($R_1 = 5\Omega$).

Input Voltage (Volts)	Output Voltage (Volts)	± % Change
44.0	4.98	-0.4
46.0	5.05	1.0
48.0	5.08	1.6
52.0	5.11	2.2
60.0	5.11	2.2
65.0	5.08	1.6

Table 4.5 Regulation Against Input Voltage($R_1 = 16\Omega$)

Input Voltage (Volts)	Output Voltage (Volts)	± % Change
41.0	4.98	-0.4
46.0	5.09	1.8
50.0	5.11	2.2
55.0	5.12	2.4
60.0	5.13	2.6
65.0	5.14	2.8

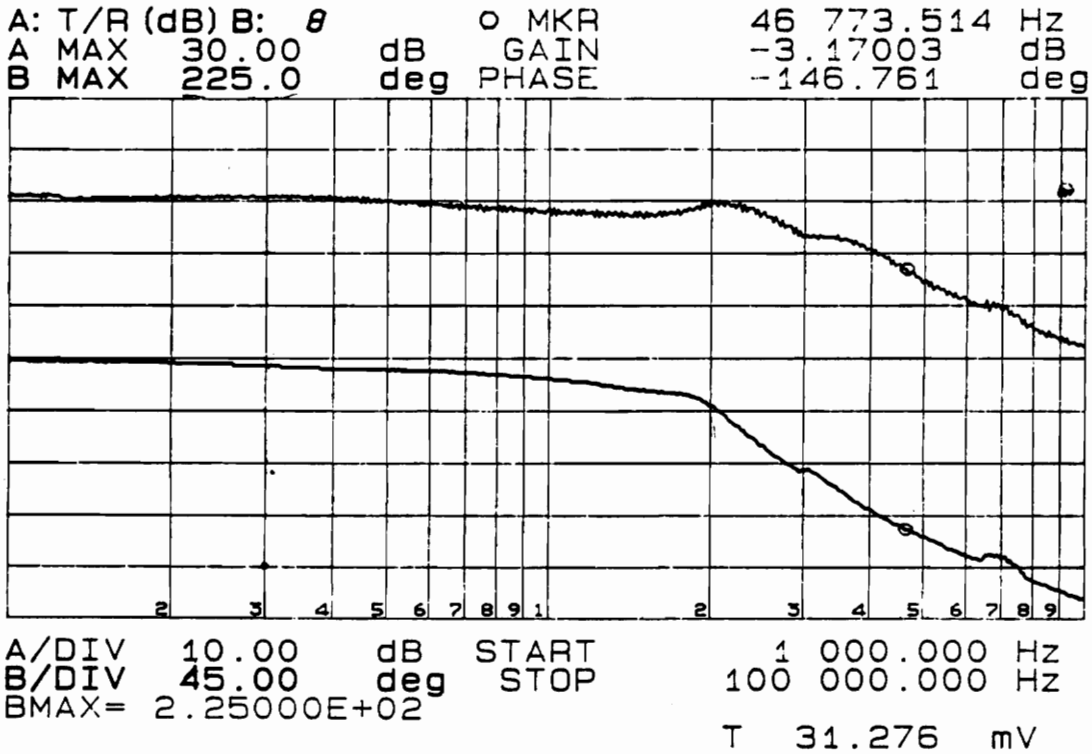


Fig.4.13 Measured Control to Output ($\frac{\hat{v}_o}{\hat{d}}$) Bode Plot.

12.2W). The low efficiency is caused by the use of capacitor with relatively large ESR of 115m Ω . The efficiency can be improved to have a value of 85%(increase of 2.52W) if a low ESR ceramic capacitor with an ESR value of .001 Ω is used.

4.3.2 Measurement of Results of Multiple-Output Quasi-Resonant Converter with Magamp Control

Fig. 4.15 shows the circuit diagram for a multiple-output forward QRC using magamp regulator. The main circuit is a forward zero-current QRC. Lr and Cr are the resonant elements which were used to shape the switching current waveform in the device Q. The other secondary is a regular PWM forward secondary.

The operation of the main circuit is very similar to that described in section 4.2 while the other one is similar to a PWM forward converter. Because another secondary output is added, the leakage inductance of the other secondary will affect the switching waveform of the device Q. Fig. 4.16(a) shows the experimental waveform of V_{D4}, I_{rst2}, and$V_{S.R.2}$ anf Fig. 4.16(b) shows waveforms of V_{D2} and I_{Lr} and V_{D4}.

A UC3838 was used for the regulation of second output which was regulated at 12V. Current reset scheme can be used in this chip. A PI controller similar to the main circuit was used in the second output(f_z = 75Hz, gain=-5.7dB).

Table 4.6 shows the test results of the regulated outputs V_{O1} andV_{O2} at 5V and 12V respectively when the load resistances R_1 andR_2 are fixed and the input voltages change. Table 4.7 and 4.8 show the regulatd output at 5V and 12V when only one of the load resistances changes while the other is fixed. Only those results within 5%

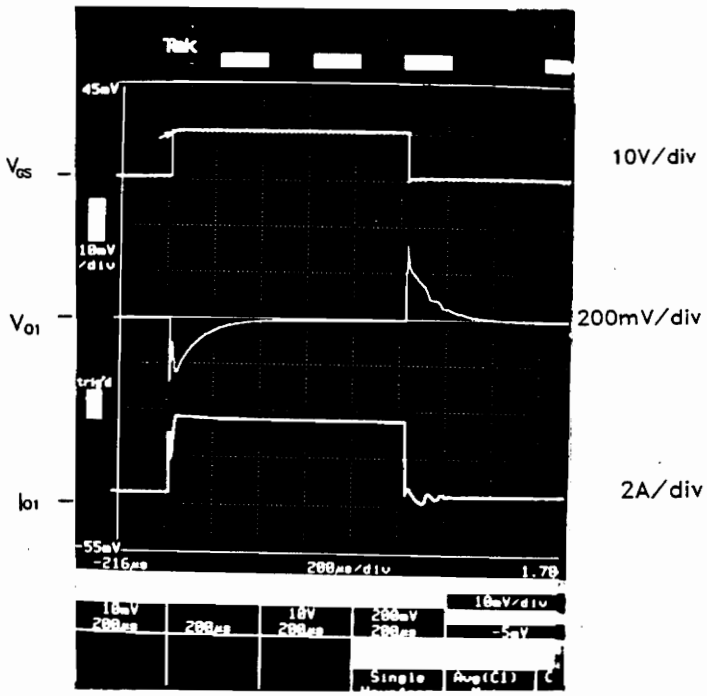
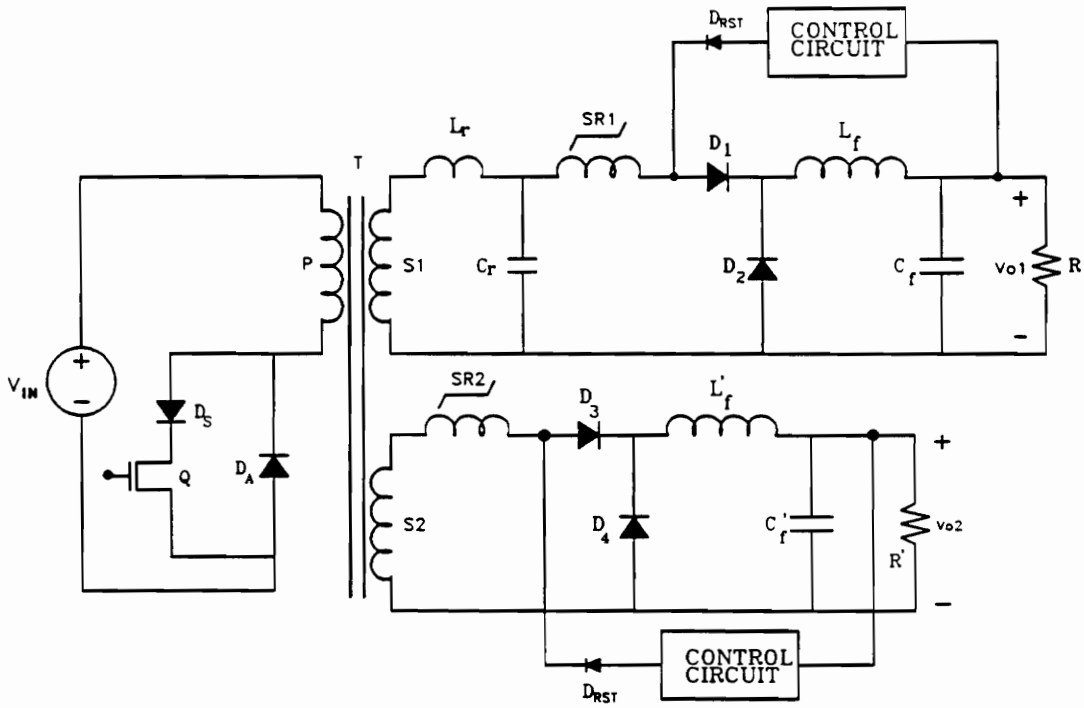


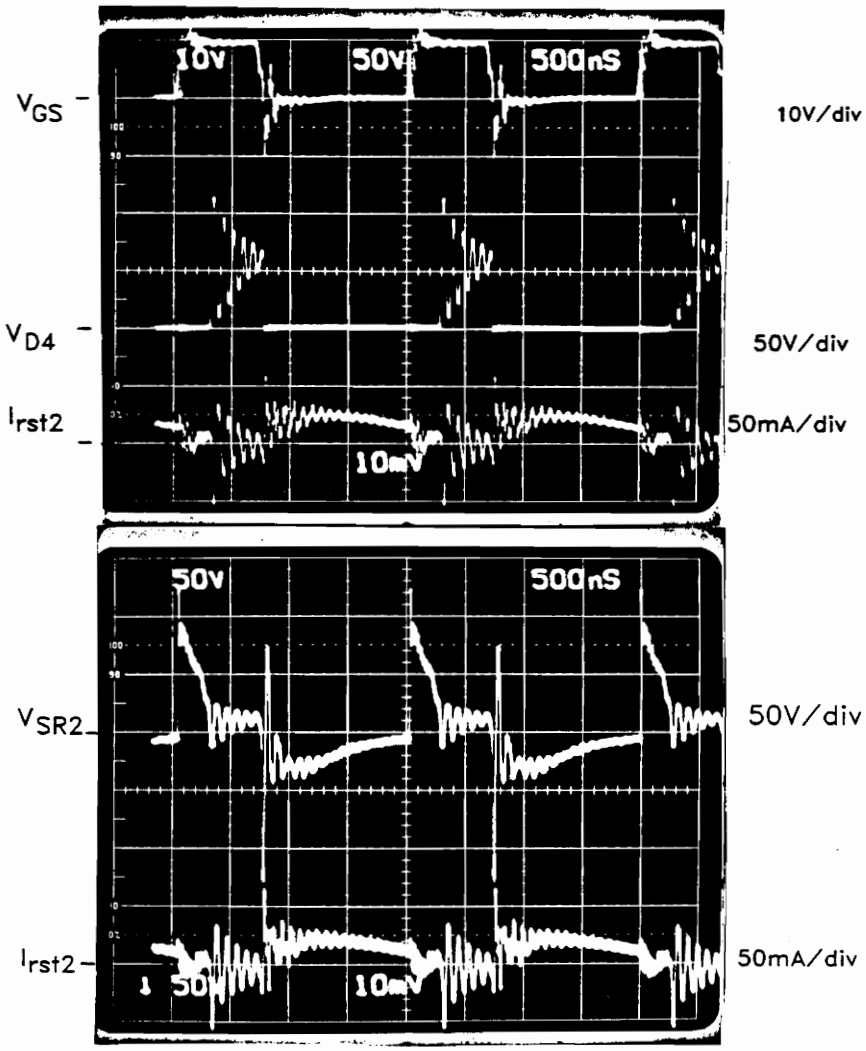
Fig.4.14 Step Response of Single Output to A Step Load Change of 3.2A.



Parts

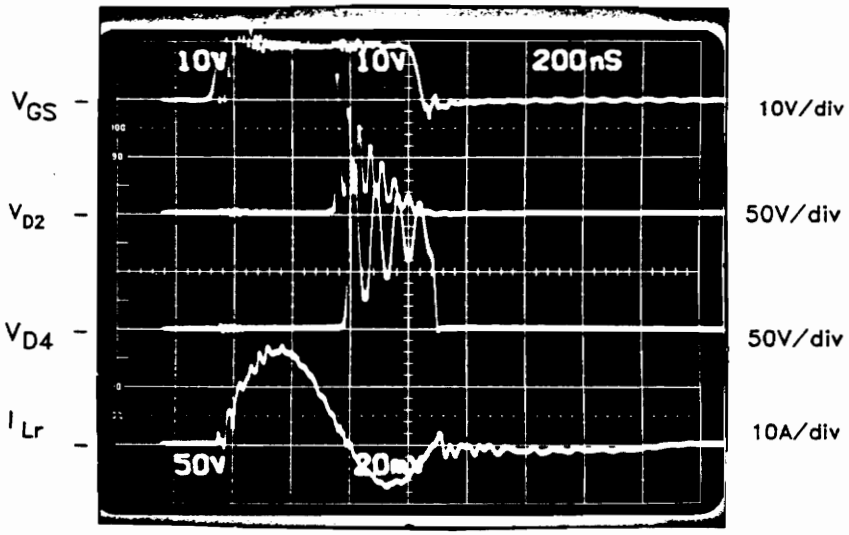
Q IRF640
C_r Polyester & foil 56nF
L_r 286nH
D_S IR31DQ10
D_A UES1306
D_{rst} UES1003
S.R.1, S.R.2 8 Turns Toshiba Amorphous Core MB15x10x4.5
D_1,D_2 IR31DQ10
D_3,D_4 IR31DQ10
Control Circuit UC3838
L_f MPP core 6.7μH
C_f Polyropylene 8.5 μF
Transformer 8/3/6T TDK H7C4 5901
L'_f MPP core 38 μH
C'_f Polyropylene 2.5 μF

Fig.4.15 Multiple-Output Forward Quasi-Resonant Converter Using Magamp Regulator.



(a)

Fig.4.16 Experimental Waveforms of Post Regulator.



(b)

Fig.4.16 Experimental Waveforms of Post Regulator.

Table 4.6 Regulation Against Input Voltage Variation for Multiple Output Quasi-Resonant Converter.

Input Voltage	Output Voltage(volts)	
(Volts)	$V_{01}(R_1 = 1\Omega)$	$V_{02}(R_2 = 6\Omega)$
58.0	5.00	12.02
63.0	5.02	12.08
72.0	5.01	12.15
78.0	4.99	12.15
85.0	4.98	12.14

Table 4.7 Regulation and Cross-Regulation Against the Variation of Load R_2 of a Multiple-Output Forward Quasi-Resonant Converter.

Input Voltage	Output Voltage(volts)		
$V_{in} = 60V$	$V_{01}(R_1 = 1\Omega)$	$V_{02}(volts)$	$R_2(\Omega)$
	5.0	12.23	6
	5.0	12.25	16
	5.0	12.31	46
	5.0	12.32	86
	5.0	12.29	116
$V_{in} = 70V$	5.01	12.13	6
	5.02	12.18	16
	5.02	12.18	26
	5.02	12.18	66
	5.02	12.33	116
$V_{in} = 80V$	4.95	12.28	6
	4.95	12.25	16
	4.95	12.25	26
	4.94	12.26	56
	4.94	12.02	116

Table 4.8 Regulation and Cross Regulation of a Multiple-Output Forward Quasi-Resonant Converter against Load Variation of R_1.

Input Voltage	Output Voltage(volts)		
$V_{in}=60V$	$V_{O1}(volts)$	$R_1(\Omega)$	$V_{O2}(R_2=6\Omega)$
	5.00	1	11.99
	5.04	5	12.02
	5.09	9	12.03
	5.11	19	12.03
	5.14	39	12.02
	5.17	59	12.03
	5.05	99	12.03
$V_{in}=70V$	5.00	1	11.98
	5.02	5	11.98
	5.09	9	11.98
	5.11	19	11.98
	5.05	29	11.98
	4.88	49	11.98
	4.89	69	11.98
$V_{in}=80V$	5.00	1	12.26
	5.05	5	12.26
	5.11	9	12.25
	5.14	19	12.24
	4.92	39	12.24
	4.92	59	12.24
	4.95	69	12.24

change were recorded. It can be seen that with magamp the cross regulation is well controlled.

V CONCLUSIONS AND SUGGESTIONS FOR FUTURE WORK

5.1 Conclusions

Design equations and some practical design considerations were presented for magamp post regulations in a conventional PWM converters under extreme magamp load conditions. Three load conditions were considered: discontinuous mode of operation, shut down of output and foldback of current. In each of these load conditions, the design of the saturable reactor plays an important role in determining the reactor core losses and the size of the bleeder resistor. The design equations given in Chapter III correlates the various circuit parameters, circuit conditions and reactor parameters in a closed analytical form. The equations make the trade-off between reactor core losses and bleeder resistor loss much easier to do. These equations are amendable to computer aided design even though this is not done in the thesis.

The concept of using magamp regulator to achieve a constant frequency quasi-resonant converter was proved feasible. A 500kHz 5V, 25 Watt-quasi-resonant full-wave forward converter was designed and tested using this concept. An efficiency of 77.3% was measured at 5A load current under 60V input voltage. This approach provides several advantages: constant switching frequency operation which makes it easier to optimize the filter component sizes, control loop is totally isolated from the primary side of the converter which simplifies the isolation problem normally associated with the control loop. There are disadvantages associated with this approach, however.

In the applications in which input voltage varies with large range, the size of the saturable reactor becomes too large. Another disadvantage is that the commercially available reactor core is hard pressed in going to frequency operation higher than 1MHz. The characteristics of the core loss, the squareness of the B-H loop and the increase of coercive force all become unsuitable for magamp applications.

5.2 Suggestions for Future Work

1. Implement the design equations developed for extreme load conditions in a computer aided procedure. This should drastically reduces the effort for the design of the saturable reactor and the choice of the bleeder resistor.

2. Develops the design equations for the saturable reactor under extreme loading condition for quasi-resonant converters. The results obtained in Chapter III are

for PWM converter. Extension of the same concept to quasi-resonant converter make it easier to design the saturable reactor under extreme loading condition for the magamp regulated quasi-resonant converter presented in Chapter IV.

3. Investigation of high frequency limitation of magamp regulator. It was pointed out in Chapter IV several limitation of high frequency operation of magamp but in a qualitative terms. Especially, the core characteristics of amorphous magnetic material at frequency above 1MHz is not available from the manufacturer. An experimental investigation of the material with regard to loss characteristics, B-H loop squareness, and increase of coercive force should provide further insight into the frequency limitation of magamp post regulator.

4. Control loop design optimization. In the circuit, control loop was not designed to take full advantage of constant frequency operation of the converter. The cross-over frequency implemented in the circuit was much too low. Future work to raise the cross over frequency to improve the dynamic response should be beneficial.

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Appendix A.

Derivation of Equations (3.1), (3.2) and (3.7)

Derivation of Eq. (3.2)

From Eq. (3.6)

$$NA_e\Delta B = V_X t_{on,semi} \times 10^8 \qquad (A.1)$$

Referring to Fig. 2.1, the average voltge across D'_2 is V'_O . Therefore,

$$(\frac{N_{S_1}}{N_P} \times V_I - V'_{D_1}) \times \frac{t_{on,semi}}{T} - V'_{D_2} \times (1 - \frac{t_{on,semi}}{T}) = V'_O$$

where V_I is the source voltage. Assume the two diode drops are the same, i.e., $V'_{D1} = V'_{D2} = V_D$ and solve for $t_{on,semi}$

$$t_{on,semi} = \frac{V'_O T}{(\frac{N_{S1}}{N_P}) \times V_I} \tag{A.2}$$

Substituting (A.2) and $V_x = V_I \times \frac{N_{S_2}}{N_P}$ into (A.1), Eq.(3.2) is obtained.

Derivation of Eq. (3.1)

From Fig. (3.1) (a) and using Farady's Law,

$$(\Delta B)_{cont} = \frac{V_x}{NA_e}(t_{on,semi} - t_{on}) \times 10^8 (Gauss)$$

t_{on} can be expressed in terms of T as follows.

$$t_{on} = \frac{V_O + V_D}{V_X} \times T$$

$$(\Delta B)_{cont} = \frac{V_X T}{NA_e}(\frac{t_{on,semi}}{T} - \frac{V_O + V_D}{V_X}) \times 10^8 (Gauss)$$

Derivation of Eq. (3.2)

$(\Delta B)_{disc}$ is the flux density in addition to $(\Delta B)_{cont}$ when the choke operates in discontinuous mode. From Fig. (3.1) (a), $(\Delta B)_{disc}$ is the flux density travelled during the period of time $(t_{on} - t'_{on})$. During this period of time, the voltage across the reactor is $V_x - V_o - V_{D1}$. Using Farady's Law,

$$(\Delta B)_{disc} = \frac{V_X - V_O - V_D}{NA_e} \times (t_{on} - t'_{on}) \times 10^8$$

t_{on} is related to T by Eq. (A.3) for a buck configuration as in the case

$$t_{on} = \frac{V_O + V_D}{V_X} \times T \tag{A.3}$$

And t'_{on} can be related to T, P_o , L etc. by Eq.(A.4). (See Eq.(CV, 27) of Ref.[8])

$$t'_{on} = \sqrt{\frac{2L(P_L + P_B)(V_O + V_D)}{V_O(V_X - V_O - V_D)V_X}} \tag{A.4}$$

By substituting Eqs. (A.3), (A.4) into (A.1), Eq. (3.2) is obtained.

Appendix B.

GLOSSARY SYMBOLS

A_e:	Cross sectional area of Magamp core (cm^2).
$(\Delta B)_{cont}$:	Flux density swing (in saturable reactor) required to regulate output voltage when the filter inductor is operated in continuous–conduction mode (Gauss).
$(\Delta B)_{disc}$:	Additional flux density swing required to regulate output voltage when the filter inductor is operated in the discontinuous mode (Gauss).
H_{RC}:	Reset coercive force.
i_L:	Filter inductor current.
L:	Inductance of the filter inductor (Henry).
l_e :	Effective magnetic path length.
L.H.S.:	Left hand side of an equation.
N:	Number of turns of the saturable reactor.

N_P:	Number of turns of the transformer's primary winding.
N_{S_1}:	Number of turns of secondary winding of the main output.
N_{S_2}:	Number of turns of secondary winding of post regulator.
P_B:	Bleeder power (W).
P_O:	Load power (W).
Q:	Power Semiconductor switch.
Q_L:	Active load for shutting down the output.
R.H.S.:	Right hand side of an equation.
R_B:	Bleeder resistance.(Ohm)
S.R.:	Saturable reactor.
T:	Period of the forward converter's switching frequency. (Sec)
$t_{on,semi}$:	Conduction time of the semiconductor switch of the converter. (Sec)
t_{on}:	Time duration when both the semiconductor power switch and magnetic switch are at "ON" state for continuous mode.(Sec)
t'_{on}:	Time duration when both the semiconductor power switch and magnetic switch are at "ON" state for discontinuous mode.(Sec)
$t_{x,disc}$:	Time duration when the magnetic switch blocks voltage.(Sec)
V_D:	Diode voltage drop. (V)
V_{D1}:	Voltage drop of diode D_1.
V_{D2}:	Voltage drop of diode D_2.

V_I:	Source voltage.
V_L:	Filter inductor voltage.
V_O:	Magamp output voltage. (V)
V_O':	Main output voltage. (V)
V_x:	Secondary winding voltage of the transformer of the forward converter when the power semiconductor switch is conducting (V).
$I_{l,\ AVE}$:	Average leakage current of the saturable reactor.(Amp)

Vita

The author was born in Ping Tung, Taiwan in 1953. He received his bachelor of science in Civil Engineering from Chung Shing University, Taiwan. He worked for Taiwan Power Company as an engineer for two years before he came to Virginia Tech. He then received his Master of Science in Civil Engineering from Virginia Tech in 1982. After that he worked for two years as a manager in S. S. Galveston Hotel , TX. He came back to Virginia Tech to study Electrical Engineering in 1984. He joined the group of Virginia Power Electronics Center in 1986 working toward his master degree in the field of power electronics.

The author has published three papers

1. A Simple Model Predicts Small Signal Control Loop Behavior of Magamp Post Regulator. High Frequency Power Conversion, May 1988, San Diego, CA
2. Magamp Post Regulators--Practical Design Considerations To Allow Operation Under Extreme Loading Conditions. Applied Power Electronic Conference, Feb.

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John C. Lee