Electrical Studies on Ion-Etched n-GaAs(100) Surfaces

by

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(ABSTRACT)

The major objective of this thesis was to evaluate electrically the damage caused by a low energy (< 4keV) Ar^+ bombardment on n-GaAs(100) surfaces. Electrical measurements were performed on Schottky diodes formed on the virgin and the ion-etched surfaces.

The I-V measurements show deterioration of diode parameters by ion etching. The ion-etched diodes have a strong component of surface leakage current. The high frequency capacitance of ion-etched diodes is less than that of the virgin diodes. The low frequency capacitance of ion-etched diodes was found to be frequency dispersive. The extent of frequency dispersion diminishes at low temperatures and at low reverse biases. Virgin diode capacitance, on the other hand, was found to be independent of frequency.

The electrical characteristics of ion-etched diodes are explained by means of an amorphous layer and a donor-like damaged layer formed as a result of ion etching. The depth of the top amorphous layer increases with etch energy. The damaged layer containing the ion induced traps superimposes over the amorphous layer and extends deep into the bulk semiconductor. The density of such traps is very bias sensitive and also temperature dependent.

A possible equivalent circuit model for the ion-etched material is proposed. Low temperature isochronal annealing (< 450°C, 10mins.) was not found effective in causing complete recovery of the ion-damaged surface.

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Chapter I: Introduction

1.1 Material

Gallium arsenide (GaAs) is a compound semiconductor combining group III (Ga) and group V (As) elements from the same row of the periodic table. It has a zinc blende crystal structure being composed of two fcc sublattices (Ga and As) separated from each other by half the diagonal of a fcc cube. A significant amount of research has been directed towards GaAs because of its application in high speed electronics. It has received serious attention as a competitor to Si in logic circuitry. Accordingly, numerous efforts were made to develop improved fabrication processes as well as devices and circuit structures for use in GaAs.

Principal advantages of GaAs over Si are its higher mobility (about six times), saturated drift velocity, and its ready availability in semi-insulating form. These advantages enable GaAs devices to work at higher frequencies (several GHz), and allows the construction of true monolithic integrated circuits (good device isolation and less parasitic capacitances). The direct band structure of GaAs makes it a good material for the fabrication of optoelectronic devices (LEDs,lasers etc). In addition, GaAs is epitaxially compatible with another semiconductor (e.g. AlAs), and can be used in making of hetrojunction lasers.

GaAs, however, has the disadvantage of not having a suitable native oxide (like SiO_2 on Si) that can cause passivation. Therefore GaAs circuit technology is largely based on MESFETs. GaAs is chemically less stable than Si and so the processing methods are restricted to low temperatures to avoid decomposition (As loss above 650°C).

Metal-GaAs Schottky barrier contacts form an important component of many semiconductor devices. It is a majority carrier device and does not exhibit appreciable minority carrier effects (e.g., diffusion capacitance, long reverse recovery time, etc.). Schottky diodes find wide spread application in microwave FETs, varactors, RF detectors, IMPATT diodes, mixers, solar cells, etc. The fabrication design of a Schottky barrier junction depends to a great extent on its application.

1.2 Ion Etching

Ion etching is a dry processing technique used in device fabrication for surface cleaning and/or etching. During ion etching, a low energy (<a few keV) ion beam sputters away material from the sample surface as a result of momentum transfer by ion impact. This technique has the ability to produce anisotropic etch profiles and hence is a promising technique for selective thinning of active layers. However, ion bombardment on GaAs has been observed to introduce crystal damage and cause subsequent degradation in the electrical performance of the devices[1,2]. Low energy beams undergo strong interaction with the semiconducting target and cause modification in its surface and bulk characteristics. For successful use of ion induced etching in device fabrication, it is very essential to understand the nature and extent of ion damage and ways to reduce its effect.

1.3 Research Objectives

Studies on the effect of low energy ion bombardment on GaAs are few, although reports have been made on ion milling as a fabrication technique. It is important to investigate the detailed electrical behaviour of ion-etched GaAs Schottky diodes as a step towards understanding the damage or device degradation caused by ion etching. The intent of this study is to characterize electrically the Si doped, LEC (Liquid Encapsulated Czochralski) grown, GaAs (100) surfaces. Two types of surfaces were investigated for this purpose. One is as received and chemically cleaned (to be referred as "virgin"); the other being subjected to low Ar^+ energy (< 4kev) bombardment following chemical cleaning (to be referred as "ion-etched"). Efforts were also made to study the effect of isochronal annealing on the electrical properties of ion damaged surfaces. Several questions related to these objectives were addressed :

1) How does ion etching affect current transport in Schottky diodes?

2) What is the influence of Ar^+ ion bombardment on the Schottky junction capacitance?

3) How the does electrical behavior of diodes compare for different etch energies?

4) What could be a possible equivalent electrical and structural model that can explain the observed behavior of ion-etched diodes?

5) Can low temperature annealing, partially or completely, heal the ion-damage?

It is felt that by answering such questions, significant information about the nature and extent of ion-damage can be deciphered. Experimental and analytical techniques used to address these questions are discussed in greater detail later.

Chapter II: Theoretical Background

Metal-Semiconductor (M-S) contacts can either be rectifying (Schottky contact) or non rectifying (ohmic contact). The advent of GaAs MESFETs and integrated circuits has placed stringent requirements on quality of Schottky and ohmic contacts. Ohmic contacts are expected to have contact resistance less than 10^{-6} ohm-cm^2, while Schottky barrier height tolerance of ± 0.01 V is desirable.

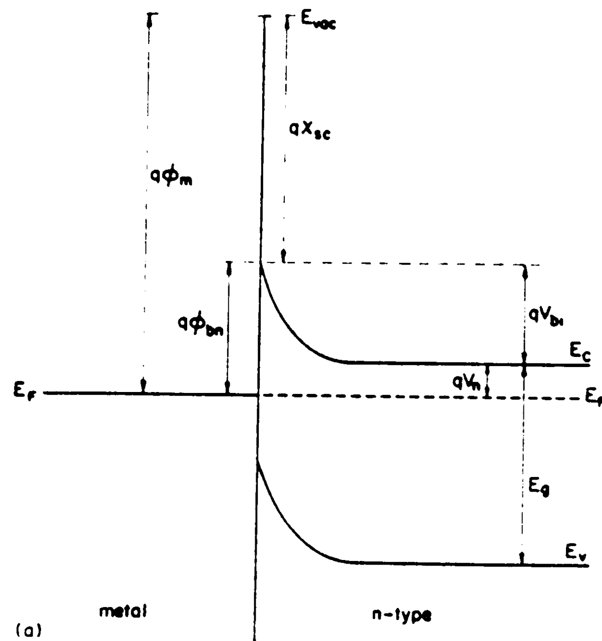
2.1 Ideal M-S Contact

Metal contacting an extrinsic semiconductor causes band bending in the semiconductor due to Fermi level equalization. For an ideal contact, there are no appreciable surface or interface states. An energy band diagram of an ideal metal n-type semiconductor junction is shown in Fig. (1a).

The Schottky barrier height for n type semiconductor is given as

$$\phi_{bn} = \phi_m - \chi_{sc} \tag{2.1}$$

while for a p-type semiconductor



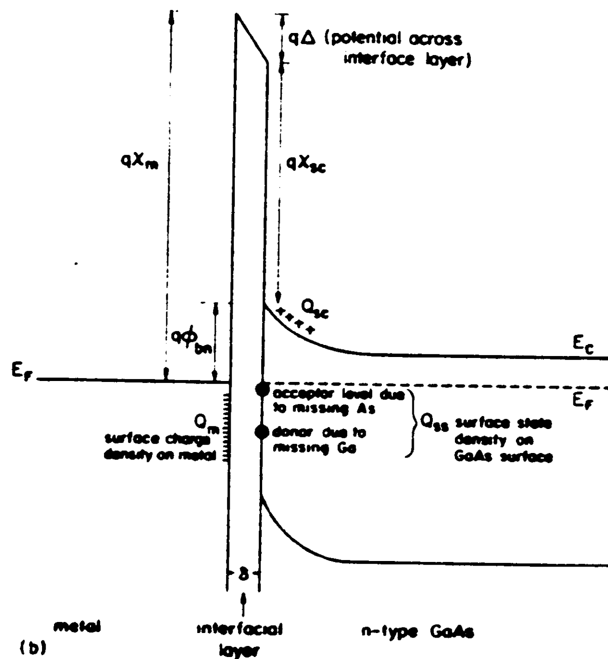


Figure 1. Energy band diagram for metal-n type semiconductor contacts: (a) ideal Schottky contacts (b) real Schottky contacts (after Howes[47]).

$$\phi_{bp} = \frac{E_g}{q} + \chi_{sc} - \phi_m \qquad (2.2)$$

where $\phi_m \equiv$ metal work function

$\chi_{sc} \equiv$ semiconductor electron affinity

$E_g \equiv$ band gap

$q \equiv$ electronic charge

For an n-type semiconductor, a Schottky junction is formed if $\phi_m > \chi_{sc}$ while the condition $\phi_m \leq \chi_{sc}$, results in an ohmic contact. If eqns. (2.1) and (2.2) were true then ϕ_b (barrier height) would be a strong function of ϕ_m (metal work function). In reality, ϕ_b values are determined by the surface states and are essentially independent of metal work function. The barrier height of metal-GaAs junctions lie close to 0.8 eV because of Fermi level pinning at the surface.

2.2 Real Metal-GaAs Contact

GaAs has a large density of surface states and so the band diagram for a Schottky contact would be similar to Fig. (1b). Numerous mechanisms have been proposed to explain the phenomenon of Fermi level pinning. One of the mechanisms due to Spicer [3] , appears to give a satisfactory explanation. According to this theory, Fermi level pinning on GaAs can be attributed to dangling bonds associated with surface antisite defects (As on Ga site and Ga on As site). However, this model does not account well for the behavior observed on a (110) GaAs surface. This surface is known to have negligible intrinsic surface states[7] and the Fermi level pinning on such a surface is explained in terms of introduction of foreign atoms, either adsorbed or deposited, during the formation of a Schottky barrier. It should be noted; however, that there is not yet a definitive theory which can uniquely explain the Fermi level pinning observed on various GaAs surfaces.

Mead [4] pointed out that the surface Fermi level of GaAs is pinned at $\sim 1/3E_g$, as measured from the valence band edge. Typical surface state density on a (100) GaAs is $\simeq 10^{14}\,cm^{-2}\,eV^{-1}$. The surface state density is found to be higher on a cleaved surface than on an etched surface [5]. Consequently, ϕ_b depends on the method used to prepare the surface.

2.3 Current Transport Mechanisms

Current transport through a metal/n-GaAs junction is governed by the following basic processes :

- emission of electrons from semiconductor to metal over the potential barrier, (a)
- quantum-mechanical tunnelling through the barrier, (b)
- recombination-generation in the space charge, (c)
- hole injection from metal or recombination in the neutral region, (d).

The transport mechanisms are schematically illustrated in Fig. 2. In addition to the above, edge leakage current and/or interface current may contribute to total current. The edge leakage arises from a high electric field at the contact periphery while the interface current is due to the traps at the metal n-GaAs interface. The description of the above current transport processes has been excellently treated by Rhoderick[5].

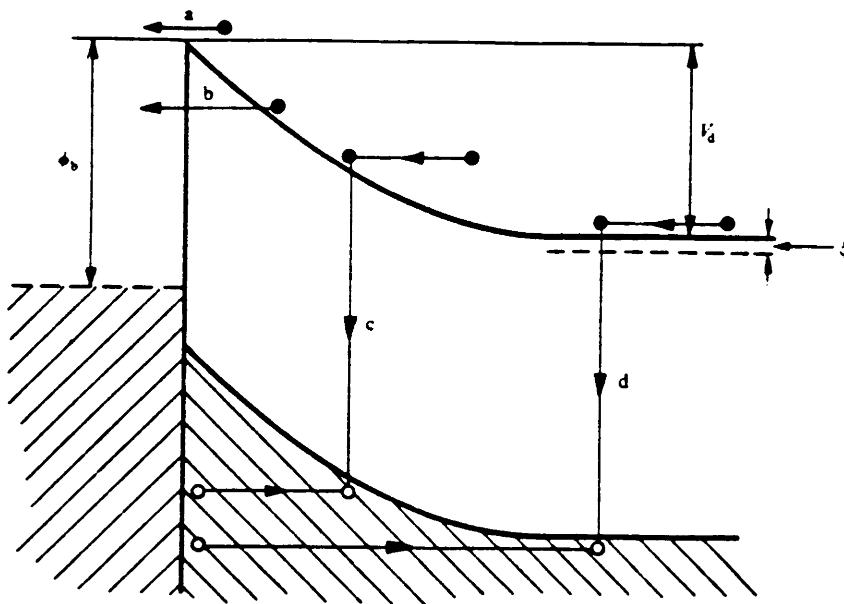


Figure 2. Transport processes of Schottky barrier under forward bias: (after Rhoderick[5]).

2.3.1 Electron Emission over Potential Barrier

The electron transfer across a M-S interface is limited by the thermionic emission. This is the most important transport mechanism in a good Schottky contact. According to this mechanism the current-voltage (I-V) characteristic of a Schottky diode is expressed by

$$I = I_0 (e^{qV/kT} - 1) \tag{2.3}$$

where $V \equiv$ applied bias

$T \equiv$ diode temperature

$k \equiv$ Boltzman constant

and $I_o \equiv$ reverse saturation current, of the form

$$I_o = AA^* T^2 e^{(\frac{-q\phi_b}{kT})} \tag{2.4}$$

where A is the diode area, A^* is the effective Richardson constant, being expressed as

$$A^* = 1.2 \times 10^6 (m^*/m)$$

where m^*/m denotes effective to free electron mass ratio.

The barrier height ϕ_b is found to be bias dependent either because of image force lowering or due to the presence of an interfacial layer. The bias dependence of ϕ_b and the current component due to tunnelling and/or space charge recombination causes the I-V relationship to take the form

$$I = I_0 e^{(qV/nkT)} (1 - e^{(-qV/kT)}) \tag{2.5}$$

where n is the ideality factor representing departure from an ideal Schottky junction (n = 1).

For $V > 3kT/q$ eqn. (2.5) can be expressed as

$$I = I_0 e^{(qV/nkT - 1)} \tag{2.6}$$

The ideality factor n can be determined from the slope of forward ln(I)-V plot. It is observed to be closer to unity at low doping levels and at high temperatures. Reverse saturation current (I_0) is obtained by extrapolating the linear portion of the forward ln(I)-V plot to zero bias. I_0 increases with the doping concentration and with the temperature.

Refined thermionic emission theory: Crowell and Sze [8] have considered the effect of quantum mechanical reflection and phonon scattering which causes a finite probability of the electrons emitted into the metal to return. This consideration would replace A^* by A^{**} (modified Richardson constant) in eqn. (2.4). The complete expression of I-V characteristics is then given as

$$I = AA^{**}T^2 e^{\left(\frac{-q\phi_b}{kT}\right)}\left(e^{\left(\frac{qV}{nkT}\right)} - 1\right) \tag{2.7}$$

Parameters, A^{**} and ϕ_b, can be experimentally determined from a Richardson plot of ln (I_0/T^2) *vs.* $1/T$. However, Rhoderick[5] points out that ϕ_b is not clearly defined for diodes with a high value of n (> 1.2) or with a non-linear forward ln(I)-V relationship. The modified Richardson constant A^{**} of GaAs is found to be $\simeq 8.6 \times 10^4 \frac{A}{m^2K^2}$. The barrier height ϕ_b, as obtained from the Richardson plot, is at 0°K. ϕ_b, to a first approximation is a linearly decreasing function of temperature[5].

The deviation of ideality factor n from unity is believed to be caused by a singular or by the combined effects of the following

- image force lowering
- presence of interfacial layer
- tunnelling
- recombination in the depletion region.

All of the above phenomena tend to increase the value of n. The presence of an interfacial layer has the strongest effect on n. It would modulate the I-V characteristics in such a way that the turn-on voltage would increase, while the barrier height and the modified Richardson constant would decrease. ϕ_b is then bias dependent and this is manifested as a diode with a non saturating reverse current (soft reverse characteristics).

2.3.2 Tunnelling

Quantum mechanical tunnelling can either occur via field emission or via thermionic field emission processes. The tunnelling by field emission (FE) is favored for a heavily doped semiconductor (degenerate) and/or at low temperatures. If the temperature is raised, electrons see thinner barrier, and the transport probability by thermionic field emission (TFE) increases. Under reverse bias, tunnelling can occur at much lower doping because the bias makes the barrier thin anyway. The I-V relationship (except at low forward bias) due to tunnelling can be expressed as

$$I = I_0 \, e^{(\frac{V}{E_0})}$$

where $E_0 = E_{00} \coth\,(qE_{00}/kT)$, $E_{00} = \frac{\hbar}{2}(\frac{N_d}{m^* \varepsilon_s})^{1/2}$, N_d being the doping density, ε_s is the semiconductor permittivity, and m^* denotes the effective electron mass. At low temperatures, i,e. in the FE regime, $E_0 \sim E_{00}$ and the slope of ln(I) *vs.* V plot is temperature independent. The TFE regime, however, has the temperature dependent slopes corresponding to different activation energies.

At contact edges, due to crowding of the field lines, the barrier height is reduced. Under such a situation, the tunnelling transport mechanism is important. This is known as the 'edge effect'. It influences the diode breakdown characteristics. The edge effect can be minimised by use of guard rings or mesa etched structures.

Ohmic Contact: The principal concept employed in an ohmic contact is to dope the semiconductor surface sufficiently high enough to assure that the dominant transport mechanism is by field emission. For n-GaAs, the structure at an ohmic interface is n^+-n. The quality of an ohmic contact is judged by its specific contact resistance(R_c). It can be represented as[24]

$$R_c \sim \exp\left[\frac{2\sqrt{m^* \varepsilon_s}}{\hbar} \left(\frac{\phi_b}{\sqrt{N_d}} \right) \right]$$

The above expression indicates that a low ϕ_b, and a high surface doping concentration (N_d) result in a low value of R_c .

2.3.3 Generation-Recombination in Space Charge

Under reverse bias, e-h pairs are generated and are swept away by the electric field resulting in a reverse current. The generation current density(J_g) is given by

$$g = \frac{q n_i W}{2\tau_r}$$

where n_i is the intrinsic carrier concentration, W is the depletion width and τ_r is the carrier life-time. The generation current is important at low temperatures and for low life-time materials.

The recombination of e-h pairs under forward bias is usually assisted by the localized centers lying within the band gap. Recombination current is higher for low minority carrier life-time materials. It makes a significant contribution at low temperatures, low forward biases and in large barrier height contacts. The carrier life-times in Si and GaAs are typically $\sim 2.5 \times 10^{-3}$ and $\sim 10^{-8}$ seconds respectively. Accordingly, the recombination-generation current is of more significance in GaAs than in Si devices.

2.3.4 Hole Injection

Hole injection constitutes the minority carrier current in a metal/n-GaAs Schottky contact. Since the Schottky diode is a majority carrier device, there is negligible contribution of hole injection to the total current. This component may be noticeable at low dopings, high current densities, and for large barrier height contacts.

2.4 Reverse Breakdown

The importance of this parameter lies in setting power limitation to GaAs MESFETs. The mechanism of a Schottky junction breakdown is via avalanche multiplication or impact ionization. For a planar structure, the breakdown voltage is inversely proportional to the product of doping density and the active layer thickness under the Schottky metal[9].

Breakdown is closely related to the electric field configuration. It is strongly influenced by the surface effects, which could modify the field configuration especially under the contact edges. In actual devices, the breakdown is very sensitive to processing details. The exact role of surface effects on the breakdown mechanism is not well understood.

2.5 Schottky Barrier Capacitance

Metal contact to an extrinsic semiconductor results in the formation of a depletion region in the portion of the semiconductor beneath the metal. The depletion region resembles a parallel plate capacitor. The depletion capacitance is bias dependent because of the variation of the depletion layer width (W) with bias. Capacitance-voltage (C-V) measurements can reveal information related to the dopant density (N_d) and the barrier diffusion potential (V_d).

The depletion layer capacitance (C) is expressed as

$$C = \frac{dQ}{dV} = \frac{\varepsilon_S A}{W} \qquad (2.8)$$

where W is related to the applied bias (V_a) as

$$W^2 = \frac{2\varepsilon_S}{qN_d}\left(V_d - V_a - \frac{kT}{q}\right) \qquad (2.9)$$

The values of N_d and V_d can be found from eqns. (2.8) and (2.9). The slope of the C^{-2} *vs.* V plot is used to evaluate the dopant density at the depletion layer edge. The diffusion potential is obtained from the intercept on the abcissa of the same plot. The barrier height can then be estimated as

$$\phi_b = V_d + V_n + \frac{kT}{q} \qquad (2.10)$$

where V_n is the separation between the Fermi level and the conduction band edge in the semiconductor bulk. For a non-degenerate semiconductor, V_n can be expressed as

$$V_n = \frac{kT}{q} \ln\left(\frac{N_c}{N_d}\right) \qquad (2.11)$$

where N_c is the effective density of states in the conduction band. GaAs has a value of $N_c \sim 4.7 \times 10^{17}\ cm^{-3}$ at room temperature.

2.5.1 Assumptions on Deducing Dopant Density and Barrier Height

Impurity profiling, from C-V measurements, is considered to be reliable if the diode has a near unity ideality factor. The above treatment is based on the assumption that the charge in the depletion layer is solely due to the uncompensated donors (for n-type) or the acceptors (for p-type). The basic concept in C-V method is to apply a dc bias (to create a depletion layer

width) with a superimposed ac signal (for differential capacitance). The amplitude of the ac test signal is much smaller than the dc bias and hence does not alter the depletion layer width appreciably. Traps often contribute to capacitance, as they may replete or deplete in response to the ac signal. For the purpose of C-V profiling, test signal frequency is usually at 1MHz. This frequency is too rapid for the traps to follow. A circuit model[10] of a typical Schottky diode is shown in Fig. 3(a). Capacitance meters typically measure parameters C_p and G_p in parallel mode as shown in Fig. 3(b). It has been discussed by Goodman[11] that a reliable capacitance measurement is possible if $\frac{G_p^2}{\omega^2 C_p^2} << 1$ (i,e. low parallel conductance), where ω is the angular measuring frequency.

The C-V method, unlike the I-V, estimates the flat band barrier height. The presence of an interfacial layer, responding surface state charges, and/or traps contribute to the non-linearity of a C^{-2} *vs.* V plot. Such a non-linear plot makes the doping density and the barrier height estimation difficult.

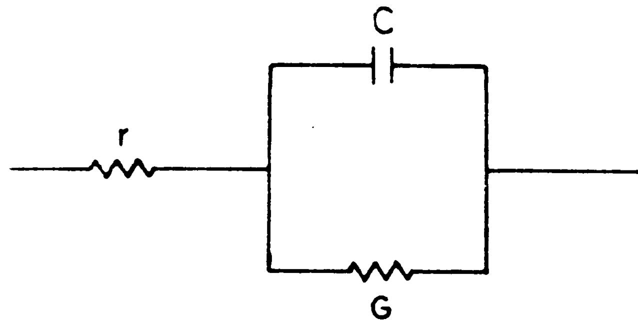
Effect of interfacial insulating layer: An interfacial layer acts in series with the space charge capacitance and modifies the bias dependence of the depletion layer width. If the layer is thin ($\leq 30\text{Å}$), semiconductor surface states can communicate well with the metal and its occupation will be decided by the metal Fermi level. Under such a situation, interface states make no direct contribution to the capacitance. However, if the interfacial layer is thicker, surface states are at least in partial equilibrium with the semiconductor[11]. These surface states, if able to follow the bias signal, can potentially contribute to the capacitance and render the C^{-2} *vs.* V plot non-linear.

The relationship between the interfacial (insulating) film thickness (t) and the effective barrier height (ϕ_b') to a first approximation can be given as [12,13]

$$\phi_b' = \phi_b + Dt$$

where D is a constant and ϕ_b is the zero film thickness barrier height.

(a) CIRCUIT MODEL OF SCHOTTKY DIODE



(b) PARALLEL CIRCUIT

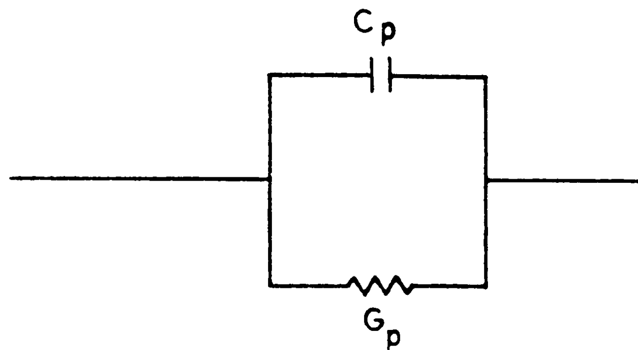


Figure 3. Eqivalent circuit model of Schottky diode: (a) actual circuit (b) circuit measured by bridge (after Neunman *et al.*[10]).

2.6 Trap Parameter Estimation

Schibli and Milnes[48] have studied the effect of deep impurities on the capacitance of a Si n^+-p junction . The total capacitance (C) is considered to be a series connection of C_{dc} (dc capacitance) and C_f (frequency dependent capacitance) such that

$$\frac{1}{C} = \frac{1}{C_{dc}} + \frac{1}{C_f}$$

The capacitance C_{dc} is bias dependent, while the capacitance C_f is frequency dependent and bias independent. At a very low frequency, deep traps contribute to capacitance and so C_f approaches infinity. The capacitance C_f decreases as the frequency is raised and so does the total capacitance C. When the density of deep traps (N_T) exceeds the density of shallow level impurities, C_f can be represented as[48]

$$C_f = \left(\frac{2\varepsilon_s q^2}{k\,T} N_T \frac{\omega_1}{\omega}\right)^{1/2} \qquad (2.12)$$

where ω is the angular measuring frequency, ε_s is the semiconductor permittivity, and ω_1 is expressed as

$$\omega_1 = c_n N_c \exp\left(\frac{-\,q\,E_T}{k\,T}\right) = \left(\frac{k\,T}{q}\right)\left(\frac{\omega_b}{4\,V_d}\right) \qquad (2.13)$$

where c_n denotes the electron capture probability, E_T is the trap depth and ω_b is the frequency at which $C_{dc} = C_f$.

Eqns. (2.12) and (2.13) together yield information about the trap parameters. The logarithmic relationship between C_f *vs.* ω yields N_T. The trap depth E_T can be determined from the slope of the plot of $\ln(C_f)$ against 1/T. The C_f axis intercept of the plot is related to the capture probability c_n. The trap capture cross-section (σ_T) is determined by

$$\sigma_T = \frac{c_n}{v_{th}}$$

where $v_{th} = 10^7\, cm/\sec$, the electron thermal velocity. If the deep trap concentration is less than that of the shallow dopants then the frequency effect is negligible and no closed form of C_f, as in eqn. (2.12), can be obtained.

2.7 Material Behavior under Alternating Field

In Fourier space, electric polarization P(ω) is related to the driving electric field E(ω) as

$$P(\omega) = \varepsilon_0\, \chi(\omega)\, E(\omega)$$

where $\chi(\omega)$ denotes the dielectric susceptibility and is a measure of the dielectric response to a harmonic excitation at angular frequency, ω. It can be expressed as

$$\chi(\omega) = \chi'(\omega) - i\chi''(\omega)$$

The imaginary component of the susceptibility is a measure of the dielectric loss, while the real part corresponds to the energy stored at the peak of the polarization cycle. The dielectric displacement D(ω) is related to the driving field E(ω) as

$$D(\omega) = \varepsilon_0 [\, 1 + \chi(\omega)\, E(\omega)] = \varepsilon(\omega)\, E(\omega)$$

where $\varepsilon(\omega) = \varepsilon_0\, \varepsilon_r = \varepsilon_0[1 + \chi(\omega)]$, $\varepsilon(\omega)$ is the complex dielectric permittivity of the form

$$\varepsilon(\omega) = \varepsilon'(\omega) - i\varepsilon''(\omega)$$

When dc conductivity (σ_0) is taken into consideration; this becomes[14] :

$$\varepsilon(\omega) = \varepsilon_0[1 + \chi'(\omega) - i(\chi''(\omega) + \frac{\sigma_0}{\varepsilon_0\, \omega})] \qquad (2.14)$$

The above equation implies that if $\varepsilon'' \sim \frac{1}{\omega}$ and $\varepsilon' \sim$ constant as $\omega \rightarrow 0$, then the dominant process is direct conduction in the measured frequency range.

When the measuring signal is alternating, the total capacitance (C_c) is a complex quantity. The real and imaginary parts of the complex capacitance are directly related to the real and imaginary parts of the dielectric permittivity as follows :

$$C_c(\omega) = C'(\omega) - iC''(\omega) = (\frac{A}{W})\{\varepsilon'(\omega) - i\varepsilon''(\omega)\} \qquad (2.15)$$

where $C'(\omega)$ corresponds to ordinary capacitance, $C''(\omega)$ is the dielectric loss, A is the cross-sectional area, and W is the capacitor thickness. The imaginary part of the capacitance $C''(\omega)$ is related to the effective conductance ($G(\omega)$) by the following :

$$C''(\omega) = \frac{G(\omega)}{\omega} \qquad (2.16)$$

The merit of a dielectric material is measured by the loss angle δ, and can be represented as

$$\tan\delta = \frac{C''(\omega)}{C'(\omega)}$$

2.7.1 Universal Capacitor

Ideal Debye response resulting from identical but non interacting dipoles or charges is seldom found because in most situations materials exhibit strong many-body interactions. More often capacitance follows power law frequency dependence as given by :

$$C_n(\omega) = B(i\omega)^{n-1} \qquad (2.17)$$

where $C_n(\omega) = C(\omega) - C(\infty)$, B is a constant, n is an exponent which defines the frequency dependence and can vary from 0 to 1. Details of dielectric relaxation and its measurement have been very well discussed by Joschner[14].

2.8 Complex Impedance and Admittance

A Complex Impedance and/or Admittance plot can be used to predict the equivalent circuit model and to estimate the circuit parameters[15]. Complex Impedance ($Z(\omega)$) and Admittance ($Y(\omega)$) can be represented as

$$Z(\omega) = R(\omega) + iX(\omega) \qquad (2.18)$$

and

$$Y(\omega) = [\,Z(\omega)\,]^{-1} = G(\omega) + iB(\omega) \qquad (2.19)$$

where R represents resistance, G is conductance, X and B are reactance and susceptance, respectively. A semicircle in the admittance or in the impedance plane corresponds to a lumped R-C series or a parallel model, respectively. A quarter circle indicates the presence of distributed R-C elements.

Chapter III: Literature Review

3.1 Introduction

Ion etching, also known as ion milling, is a physical process making use of the inert gas ions to sputter materials from a target. A general configuration of an ion etching system is shown in Fig. 4. Use of inert gas would presumably avoid any kind of chemical reaction between the bombarding ions and the target materials. Principal advantages of ion beam etching (IBE) lie in the complete absence of undercutting and its ability to produce submicrometer structures on a semiconducting substrate. Ion etching energies usually vary from 100eV - 1keV and the etch rate is a strong function of ion energy, ion current density, and beam angle. Figures 5(a) and 5(b) show the dependence of ion-etch rate on the accelerating voltage and the beam current density, respectively.

Ion etching, apart from the radiation damage, has few other disadvantages. There is a good possibility of redeposition of sputtered materials and also of trenching into the substrate material at the bottom of a masking pattern(16) . When an energetic ion beam strikes a GaAs substrate, the energy is released in sputtering and lattice disorder. The degree of disorder is dependent on the energy and the dose of incident ions. Complicated radiation damage is introduced even at low energy of incident ions.

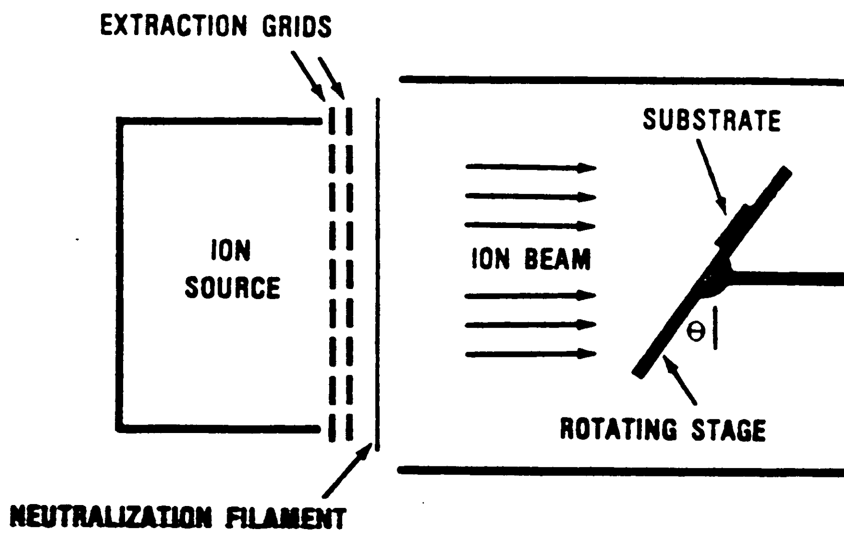
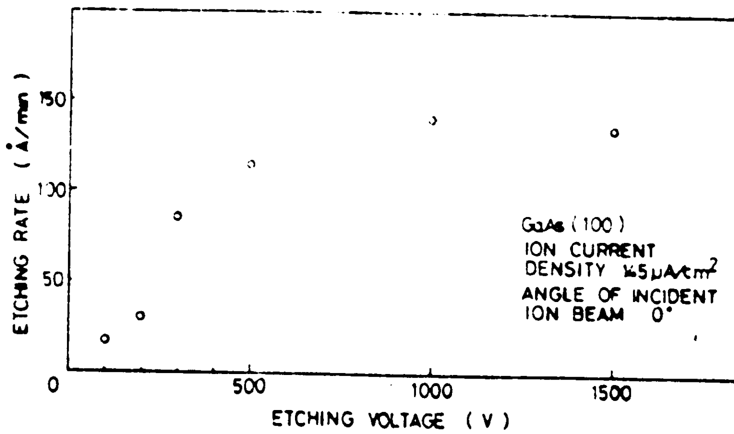
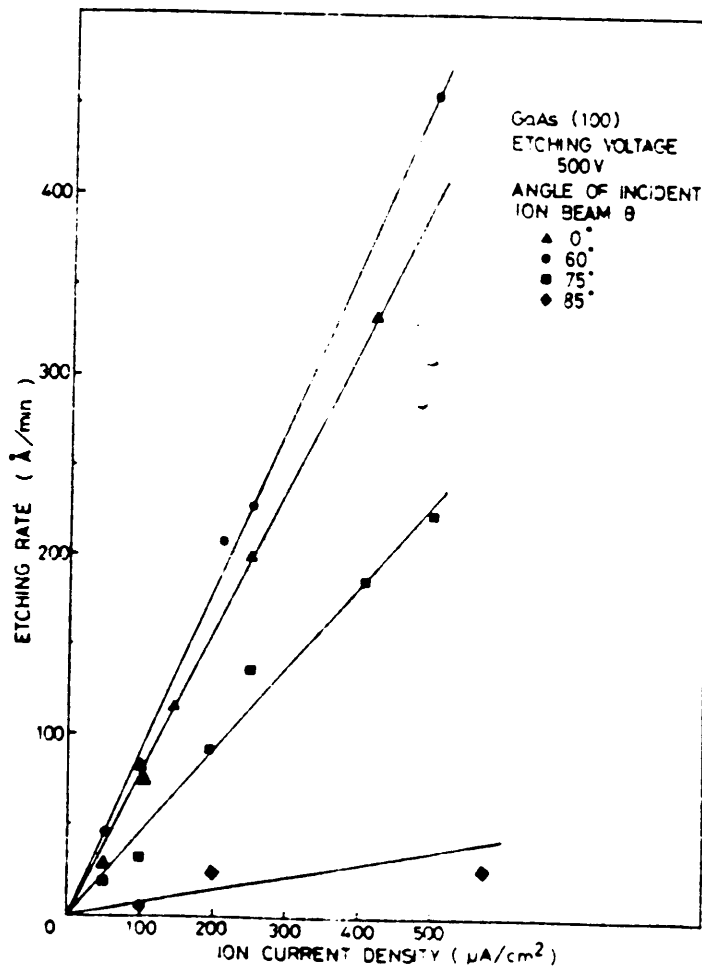


Figure 4. General configuration of an ion etching machine: (after Williams[16]).



(a)



(b)

Figure 5. Dependence of etching rate: on a) ion energy b) ion current density (after Kawabe *et al.* [11]).

IBE induces damage to the following properties :

- Crystal structure
- Chemical composition
- Electrical characteristics

3.2 Structural Damage

LEED (Low Energy Electron Diffraction), RBS (Rutherford Back Scattering), photoluminescence spectra, etc. are some of the commonly used tools for obtaining structural information. Amith and Mark[7] have studied the structural degradation due to the influence of 500eV Ar^+ bombardment on a (110) n-GaAs surface. The sharp LEED pattern, which is a characteristic of a chemically cleaned virgin sample, was completely lost with a 15 minutes exposure to a 500eV ion beam. The change in LEED pattern is attributed to the formation of a disordered (amorphous) surface layer of $\sim$ 15 - 20 Å thickness.

Kawabe *et al.*[1] evaluated the ion-damage layer on a LEC grown undoped (100)GaAs by means of photoluminescence spectra. They report that an ion-etched surface consists of roughly two layers. The first layer is a heavily damaged amorphous layer. The thickness of this layer was found to be 23 and 72 Å for Ar^+ ion energies of 100eV and 2keV, respectively. The second layer is a damage diffused layer and can be thicker than the top amorphous layer by one or more orders of magnitude. It extended as deep as 2000 Å for etching energies between 500eV - 2000eV. The defects in the damaged second layer can potentially participate as recombination centers during current transport. The intensity of the photoluminescence peak was found to decrease with increase in degradation caused by higher etch energy.

Ultraviolet reflectivity spectra on Ar^+ bombarded GaAs (100) surfaces are shown in Fig. 6[8]. The curves indicate that the spectra begin to resemble those of amorphous GaAs at

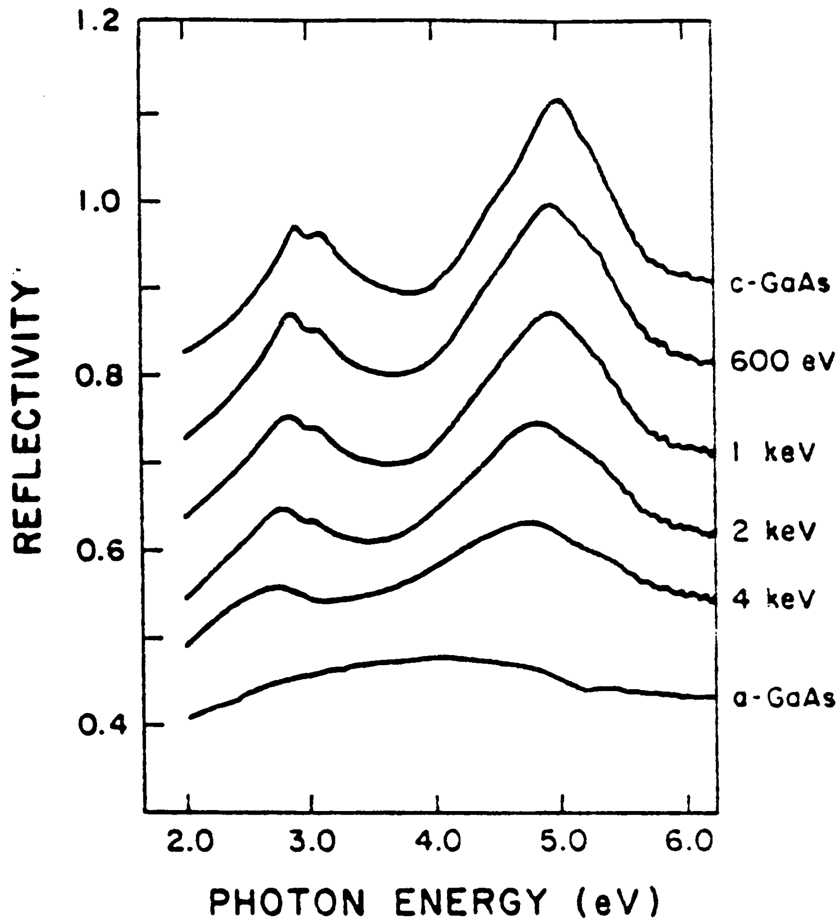


Figure 6. Ultraviolet reflectivity spectrum for different etch energies: (after Feng *et al.*[6]).

higher etch energies. At 4keV, about 45% of the surface region transforms into the amorphous form. Pang[18] also reports the presence of an amorphous layer on an ion-etched surface. This layer contains defects in the form of vacancy-complexes, dislocation loops, bubbles, implanted ions, etc.. The depth of ion-damage is greater than the projected ion range because of phenomena such as channeling, vacancy migration, enhanced diffusion etc..

Structural degradation by ion etching induces a high density of interface states[19]. Pang *et al.*[19] have investigated the ion-damage on a Si surface and found that the interface state density can be reduced to the pre-etched value, if the damage layer of about 500 Å is chemically removed.

3.3 Stoichiometric Disorder

Chemical conditons on a GaAs surface are usually monitored by means of AES (Auger Electron Spetroscopy), XPS (X-ray Photoelectron Spectroscopy), etc.. Wang and Holloway[20] have studied the effect of Ar^+ ions on the interface chemistry of (100)n-GaAs. The AES spectra shown in Fig. 7 indicate that the relative intensities of As and Ga peaks are changed due to sputtering. The spectra reveal the ion induced loss of arsenic (As) along with the removal of oxides and carbon contaminants. The spectra also indicate that the native oxide on GaAs is essentially gallium (Ga) rich while a chemically cleaned surface is As rich ($\frac{X_{As}}{X_{Ga}} \sim 1.2$).

The preferential sputtering of As by Ar^+ ions has also been reported by other investigators[6,7,18,21]. The depletion of As takes place at energies as low as 100eV but gets severe at higher etch energies. The depletion depth of As increases with ion energy. This correlation, for a 15° beam angle[20], is shown in Table 1.

Chiang and Pearson[23] have proposed that an As vacancy has a donor-like character. Accordingly, numerous investigators have reported the creation of a donor-like damage layer due to sputtering[2,19,20,21,27] . The depleted arsenic layer extends several tens of Å below the surface. The density of ion-induced donor-like traps depends on the etch rate and the etching

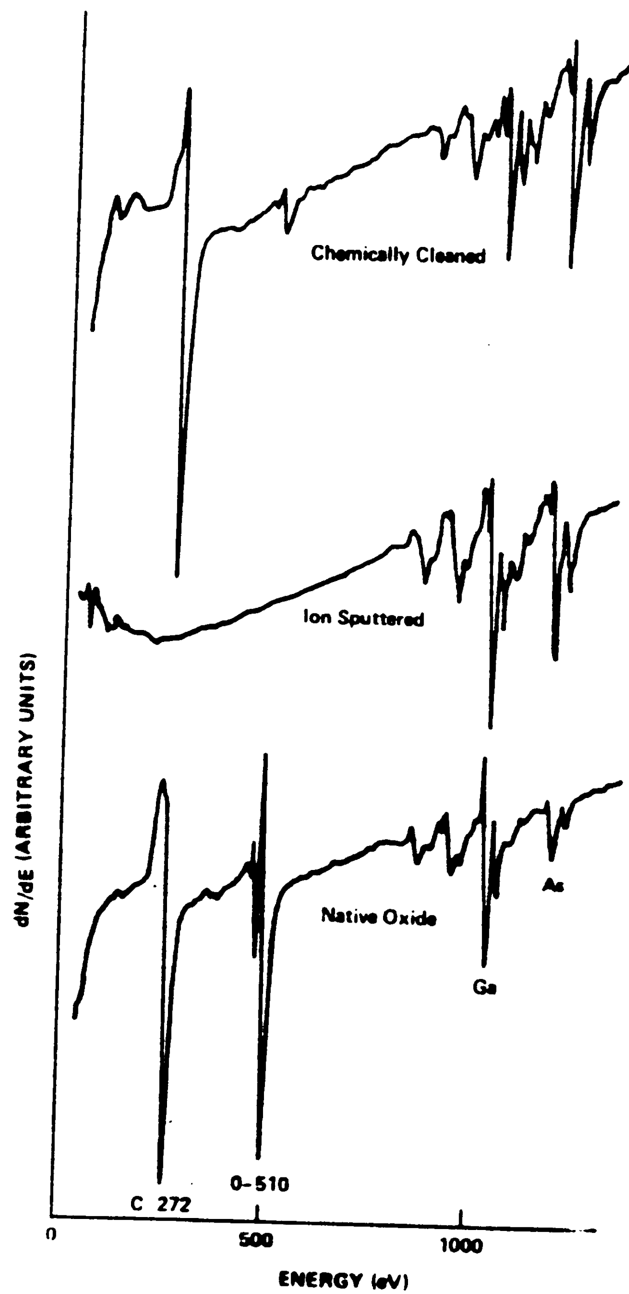


Figure 7. AES spectra for GaAs with native oxide, ion cleaned, and chemically cleaned surfaces: (after Wang and Holloway[20]).

Table 1. Effect of etch energy on As depletion depth.

Energy (keV)	**As depletion depth** (Å)
1	20
3	60
>4	>120

time. The As vacancies dominate the damage layer and the electric field in the layer is high. In addition to As vacancies, the damage layer also contains defect such as Ga vacancies, As and Ga antisites, interstitials, etc.. These defects form deep levels and have a lesser pronounced effect than the As vacancies on subsequent behavior of IBE diodes.

Muller and Brunschweiler[25] have proposed a model of donor-like damage layer on an ion sputtered Mo-Si interface. The distribution of donor-like trap states (N_t) from the surface is represented as

$$N_t = N_{ts} \exp\left(-\frac{X}{L} \right) \qquad (3.1)$$

where N_{ts} is the trap density at the surface and L is the characteristic length. L increases linearly with sputtering voltage while N_{ts} varies logarithmically with sputtering time at a fixed accelerating voltage[25].

Contamination: There is always a good possibility that the materials sputtered from any part of the etching chamber or from a dielectric or polymer layer on the substrate top can be redeposited on the etched surface. Traces of foreign atom deposition were observed during ion cleaning of Si[28]. The deposited atoms are believed to be creating deep levels at the interface.

3.4 Electrical Damage

Electrical damage is evaluated by electrically characterizing Schottky doides fabricated on the ion-etched surfaces. The damage discussed above strongly influences the electrical behavior of the IBE diodes. The principal effects of radiation damage are the reduced effective carrier concentration, the mobility degradation, and the reduced carrier life-time. These changes in material parameters have a significant effect on subsequent diode characteristics.

3.4.1 Current-voltage (I-V) Characteristics

Current transport across a metal-semiconductor barrier is very sensitive to ion-etch induced inhomogeneities at the interface. The I-V measurements exhibit the most dramatic difference between the behavior of virgin and ion-etched diodes. The IBE diodes are found to have anomalous rectifying behavior.

The Schottky barrier diodes built on an ion-etched surface have a high ideality factor (n) and high surface leakage current[18,21,31,36]. The top amorphous layer is presumed to be providing an effective lateral leakage path. The increase in ideality factor n is attributed to large number of donor-like surface states at the interface[30]. The forward characteristics of ion-etched diodes usually have a non-linear log(I) *vs.* V relationship. This non-linear relation makes the ideality factor bias dependent. A high ideality factor ($n \geq 2$) is indicative of trap assisted tunnelling effects[7,21]. Figure 8 shows the effect of 500eV Ar IBE (at 0.5 mA/cm^2) on forward I-V characteristic of a Ti-Au/n-GaAs Schottky diode[18]. The figure also indicates the importance of chlorine flux (as in ion beam assisted etching) in minimizing the ion-damage.

The reverse saturation current (I_0) increases with ion etching[7,21,32,33]. For $n >> 1$, direct extrapolation of the log(I)-V plot does not give true I_0; instead it gives an effective value[21]. The large reverse current in an ion-etched diode is explained in terms of higher tunnelling probability through the donor-like damage layer[20].

Borrego and Gutmann[33] have shown that the reverse current in an irradiated Au-nGaAs diode is neither due to the conventional generation in the depletion layer (as in an unirradiated p-n junction) nor is due to the thermionic emission (as in a virgin Schottky barrier). They observed a strong dependence of reverse current on voltage and a relatively weak dependence on temperature for neutron irradiated n-GaAs Schottky diodes. This behavior is attributed to the enhanced field emission from the bombardment induced traps.

Forward characteristics of ion-etched diodes can be better represented as[11]

$$I_F \propto V_F^m$$

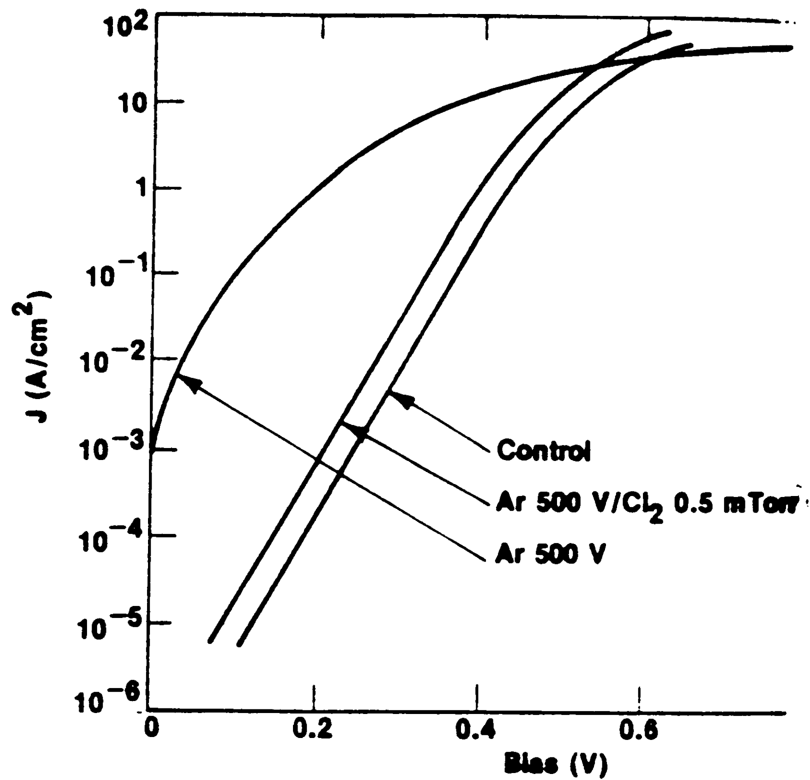


Figure 8. Semilog plot of current as a function of forward voltage: (after Pang[18]).

where m ~ 1.3 over the voltage range of 0.02 - 0.2 V. A similar observation, on GaAs subjected to boron ion implantation at 80keV, was made by Taylor and Morgan(39).

The effective barrier height (ϕ_b') is found to decrease with ion milling(2,11,17,19,20,27). The true barrier height (ϕ_b) on (110) n-GaAs, as obtained from the internal photoemission method, remains unchanged even after ion bombardment(7). The photoemission method gives a measure of true ϕ_b and unlike the I-V and the C-V method, is insensitive to spatial inhomogeneities at the interface. The effective barrier height ϕ_b' is an important parameter for diodes with high trap densities at the interface. ϕ_b' is dependent on the applied bias and the distribution of surface states(35) . The barrier height reduction of ion milled Si diodes has also been reported(25,28) . A model of donor-like damage layer was put forward to explain this behavior.

Berg *et al.*(36) have proposed that for a very high surface trap density (similar to ion cleaned diodes), the main contribution of current comes from an energy level E_{00} that is smaller than ϕ_b. At low surface trap density, $E_{00} \simeq \phi_b$. E_{00} decreases as the sputtering voltage and/or the sputtering time is increased(36) .

Wang and Holloway(20) have noticed that the barrier height is not a monotonic decreasing function of increasing ion energy. The barrier height for 3keV sputtering was found to be higher than that for 1keV. This anomaly is explained in terms of the As to Ga ratio which is found to be closer to stoichiometric for the 3keV than for the 1keV etched surfaces. The barrier height reduction is found to be more for a greater As depletion or for an excess of Ga at the Schottky interface(37,38). This model directly leads to Wang and Holloway's explanation to their barrier height anomaly of the 3keV etched diodes.

The ion-etched diodes exhibit soft reverse characteristics and lower breakdown voltages(18,19). Surface disorder and Ar ion inclusions are believed to be responsible for this behavior. Wu *et al.*(27) have investigated the effect of IBE after Schottky metallization. In this case the active layer was protected by a $ErSi_2$ layer. The breakdown voltage and the barrier height of an $ErSi_2$/n-GaAs diode decreased because of the the intensification of edge effect by ion etching.

3.4.2 Capacitance-voltage (C-V) Measurements

C-V measurements probe the depletion edge at equilibrium, and with reverse bias probe the region away from the interface. Few investigators have reported the distortion of C^{-2} against V plot by ion beam etching[20,31]. A downward concavity in the plot is due to the bias dependent charge on surface states or deep bulk states that may be electrically active or inactive. Wang and Holloway[20] report that for diodes etched with energies > 1keV, the interfacial damage distorts the C^{-2} *vs.* V plot in such a way that the data reduction scheme for obtaining dopant density (N_d) and barrier height (ϕ_b) is no longer valid.

Studies of 500eV ion bombardment on n-GaAs (100) have shown that the slope of C^{-2} *vs.* V plot remains unchanged but the intercept on the voltage axis is increased[7]. The zero bias capacitance C(0) is higher for IBE diodes. This is due to a decrease in depletion layer width by the presence of a high density of surface states.

Pang *et al.*[19] have noticed an increase in the effective doping concentration due to 250eV ion bombardment on n-GaAs at a beam current density of 0.25 mA/cm^2. Chemical etching of 250 Å could restore the virgin I-V characteristics. To restore the C-V characteristics a layer of ~ 750 Å had to be removed. This indicates that the C-V measurement is very sensitive to semiconductor trap concentration and/or insulating layer build up at the interface. The ion-damage layer was accordingly estimated to be ~ 750 Å thick and was found to be the same for ion energies between 250eV to 1keV[19].

In another study Kwan *et al.*[21] report that for 400eV, C(0) rises drastically but at higher energies it drops steadily and tends to approach C(0) of the virgin sample. It has been reasoned that the donor-like damage layer penetrates deeper into the crystal at higher energies, and so C(0) drops.

Neutron irradiated (3.6×10^{14} neutron/cm^2 at 100 keV) diodes show an apparent decrease in the carrier concentration[33]. The reduction in capacitance and in effective donor concentration (N_d') was observed for GaAs diodes that were subjected to dislocation-induced mechanical deformation[41] . GaAs MIS Schottky diodes also show similar trends[40]. For a thick

interfacial layer (> 30 Å), the surface states are in equilibrium with semiconductor and the effective doping concentration (N_d') is given by[42]

$$N_d' = \left[\frac{N_d}{(1 + \alpha')}\right]$$

where α' is a constant and is proportional to density of interface states.

Boron ion implantation at 80keV on GaAs is reported to create a compensated layer that dominates the capacitance at low reverse bias[39]. The compensated layer reduces the overall capacitance and renders the C^{-2} *vs.* V plot non-linear. At high reverse bias, the damaged layer does not form a significant portion of the depletion layer, and so the slope $(\frac{dC^{-2}}{dV})$ remains almost unchanged.

3.5 Annealing

Annealing of an ion-damaged (500eV Ar^+) surface appears to create an intrinsic layer while ordering the surface[7]. It neither eradicates defects or spatial inhomogeneities, nor does it drastically alter the electronic properties of an IBE diode. Amith and Mark[7] propose that the ion-induced As vacancies remain and get spatially redistributed by annealing. They observed that for an annealing temperature > 550°C, additional donor-like As vaccancies are created and the electron concentration in the sputter damaged layer is enhanced.

In a separate study, annealing of a 100eV ion-etched diode (at 450°C for 10 minutes under hydrogen) almost completely recovered the photoluminescence spectrum[1]. Similar behavior after annealing was also observed on a rf-sputter etched GaAs surface[44]. Annealing, however, could not completely heal the degradation on diodes etched by Ar^+ of energies more than 500eV.

Kwan *et al.*[21] have studied the effect of post Schottky metallization anneal on ion-etched GaAs (100) surfaces. The annealing temperature was restricted below 400°C because of

possible inter-diffusion effects. Recovery to a large extent is possible by annealing if the ion energy is ≤ 100eV. Such annealed samples had diode characteristics very close to that of the virgin ones. Samples damaged at ion energies ≥ 400eV became progressively worse with annealing.

Results of the study by Pang *et al.*[19] on VPE (Vapor phase epitaxy) grown n-GaAs indicate that thermal annealing (550°C for 30 mins under N_2) after Schottky metallization could partially recover the barrier height and the breakdown voltage of 250eV IBE diodes. Annealing at ~ 550°C was not found to be effective in improving the I-V characteristic of diodes etched between 500eV-1000eV. In such an ion energy range, the degree of lattice disorder is such that a higher thermal energy is possibly required for damage recovery.

Post ion etch (500eV, 0.5 mA/cm^2) annealing of $ErSi_2$/n-GaAs diodes at 300-375°C (under forming gas for 25 mins.) could recover the barrier height and the breakdown voltage to its initial value[27]. Yamasaki *et al.*[2] have studied the recovery behavior of barrier height on ion sputtered n-GaAs (100) surface. Figure 9 shows the barrier height dependence on annealing temperature. The barrier height increases linearly with anneal temperature above a certain threshold that depends largely on the sputter etching conditions. A higher threshold temperature is required for diodes etched at higher energies.

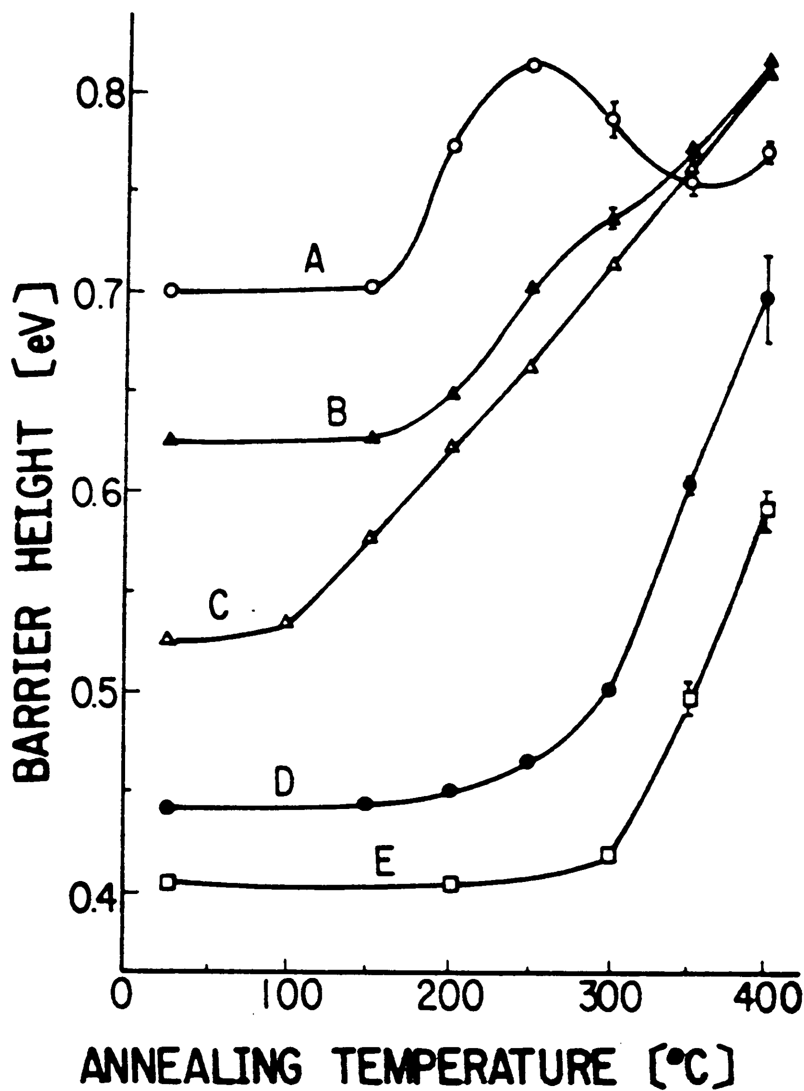


Figure 9. Barrier height variation with anneal temperature a) no sputter etch, sputter etch at b) 50W, 6 mins c) 50 W, 10 mins d) 100W, 10 mins e) 200W, 10mins: (after Yamasaki *et al.*[2]).

Chapter IV: Experimental Techniques

4.1 Wafers

GaAs wafers of two inch diameter were obtained from two sources. All wafers were Si doped (n-type) and LEC grown with (100) as the polished face. Airtron supplied wafers had a dopant concentration $N_d \sim 3 \times 10^{15}\,cm^{-3}$ while those supplied by Morgan had $N_d \sim 6.46 \times 10^{16}\,cm^{-3}$. Thicknesses of as received wafers were $\sim 20 \pm 1$ mils. The specified mobilities of Morgan and Airtron samples were $4280\,cm^2/(volt-\mathrm{sec})$ and $4320\,cm^2/(volt-\mathrm{sec})$, respectively. The wafers were diced into 0.5″ x 0.5″ chip size by means of a diamond scriber.

4.2 Sample Preparations

Schottky diodes were formed by the following sequential processes :

4.2.1 Chemical Cleaning

Prior to ohmic contact formation, all the chips were subjected to following chemical treatment

a. 10 minutes in boiling tetrachloroethylene

b. 10 minutes in warm methanol

c. rinse in de-ionized (DI) water

d. 10 minutes in 1:1 (by vol.) diluted HCl

e. rinse in DI water

f. 4 minutes in 8:1:1 H_2SO_4 : 30% H_2O_2 : H_2O (by vol.) solution contained in a rotating beaker (rotation speed $\sim$ 22 rpm).

g. rinse in DI water and kim-wipe dried.

The chips subsequent to above cleaning were ready for ohmic evaporation.

4.2.2 Evaporation

Thermal evaporation for Schottky and ohmic contact formations were carried out in a DENTON-503 high vacuum evaporating unit. A tungsten (W) boat containing the source material was resistance heated under vacuum. Following are the evaporation details maintained for each deposition cycle :

- pressure before evaporation $\sim 4 \times 10^{-6}$ torr

- substrate temperature at the end of an evaporation $\sim$ 150 °C

- heating current $\sim$ 200 amps

- voltage across the boat $\sim$ 8 V

A quartz crystal thickness monitor (Kronos model-311) and a rotating shutter were used in conjunction to control the thickness of the deposited film.

4.2.3 Ohmic Metal Deposition

The chemically cleaned chips were located between the slots on an Al base and a stainless steel shadow mask. The mask was held tightly over the chips by means of a top holder plate as shown in Fig. 10. The entire unit was clamped to a circular Al plate having three guiding holes near its outer edge. This plate was then positioned through the guiding pins in such a way that the masked chips were directly facing the evaporating source underneath. The distance between the source and substrate was maintained at $\sim$ 11 inches.

Au-Ge (88%-12%) alloy was used as an ohmic material. A piece of the alloy was evaporated upwards from a resistance heated W boat. The pressure maintained during evaporation was $\sim 4 \times 10^{-6}$ torr and the rate of deposition was $\sim$ 400Å/ min. The Au-Ge contacts had a circular geometry of 1/16″ in diameter, with a film thickness of $\sim$ 2000Å.

Following the Au-Ge evaporation, Ni was deposited over the Au-Ge layer. A layer of Ni is necessary for protective capping and to prevent "balling up" of the Au-Ge layer during subsequent ohmic annealing. The Ni layer had a thickness of $\sim$ 600Å.

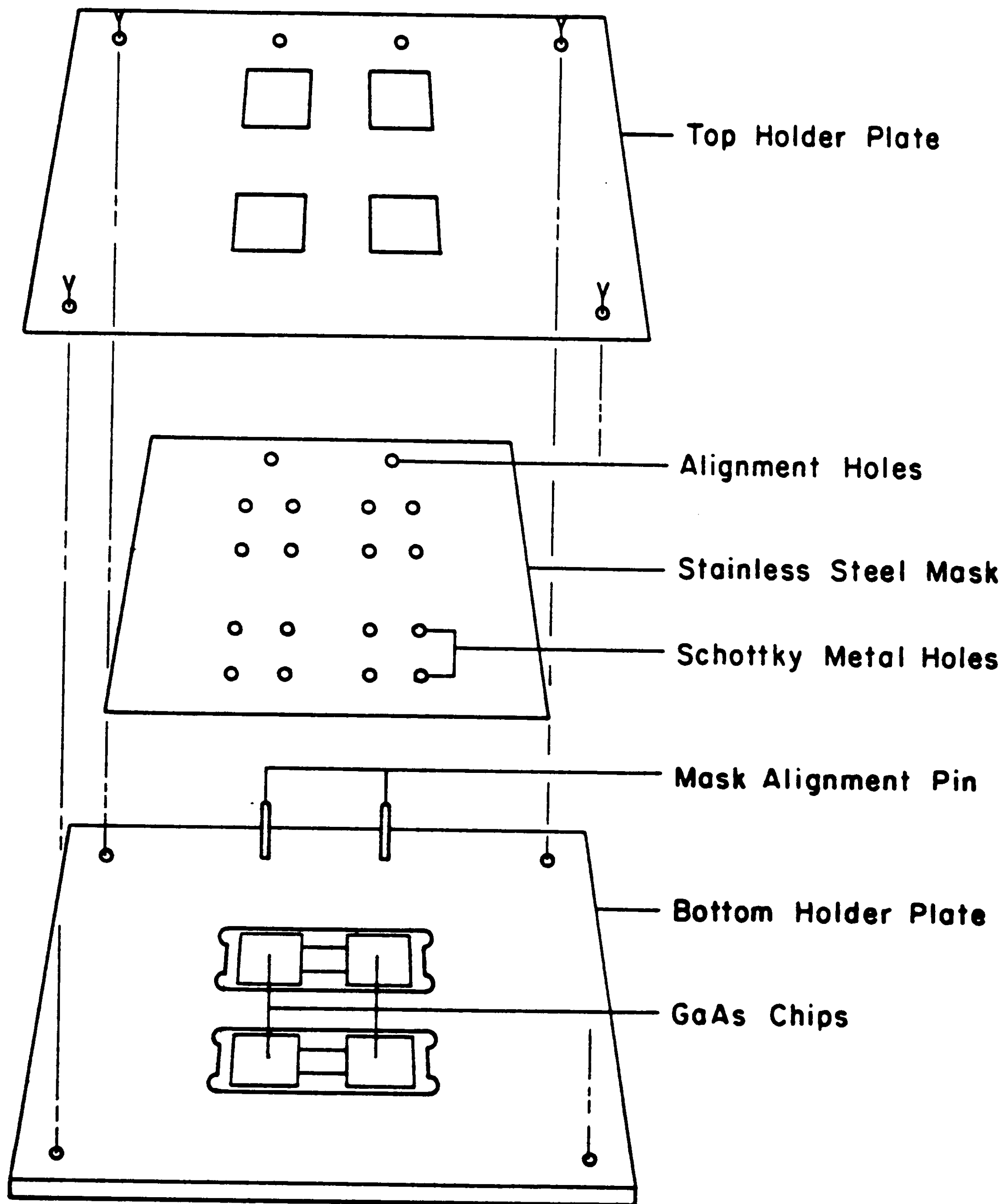


Figure 10. Substrate clamping arrangement during evaporation.

4.2.4 *Ohmic Annealing*

This step is necessary to develop ohmicity to Au-Ge/Ni layer. Annealing ensures that Ge diffuses into the GaAs substrate to form a low resistance n^+ region under the contact. The chips were individually annealed in a Thermolyne (Type 21100) tube furnace at 440°C for 2 minutes under forming gas ($90\%N_2$ + $10\%H_2$) ambient. An Omega temperature controller controlled the annealing zone temperature while a Matheson flowmeter controlled the forming gas flow.

4.2.5 *Intermediate Chemical Cleaning*

The GaAs substrates with ohmic contacts on them were subjected to 8 : 1 : 1 H_2SO_4 : 30% H_2O_2 : H_2O (by vol.) solution for $\simeq$ 4 mins and subsequently rinsed in DI water and dried. This etching step was found necessary to produce good quality diodes from Morgan wafers. Airtron samples bypassed this etching step. The intention to include this etch is to remove a possible damage layer, if any, formed during ohmic annealing. The ohmic anneal damaged layer is thought to be responsible for subsequent poor diode quality which was observed on a large number of diodes made out of Morgan wafers. Samples were then etched in 1 : 1 (by vol.) diluted HCl solution for 10 minutes. The aim of this etching step is to remove any surface oxides that may be present. The virgin samples, following this step, would be processed for Schottky metal deposition while the rest would be subjected to Ar ion bombardment.

4.2.6 *Ion Beam Etching*

Argon ion (Ar^+) beam etching was carried out in a Perkin-Elmer Phi 5300 X-ray Photoelectron Spectrometer in the Chemistry Department. The ion etching parameters used to introduce ion-damage on GaAs substrates are listed below :

- ion energies : 1keV, 3keV
- fluence : 10^{17} Ar^{+}/cm^{2}
- beam current : 38 μA
- chamber pressure before ion etching : 2×10^{-8} torr
- chamber pressure during ion etching : 1×10^{-7} torr
- beam angle w.r.t. surface normal : 45°
- beam area : 1 cm^2

4.2.7 Schottky Metal Deposition

The virgin and the ion-etched substrates were reloaded into the vacuum evaporator to define Schottky contacts. Aluminum (Al) was used as a Schottky metal because of its popularity as a gate metal in GaAs FETs. Its choice is due to its ease of evaporation, low resistivity, minimal inter-diffusion with GaAs, and forms an electrically stable Schottky barrier. A separate stainless steel mask was used to form 1/32″ diameter Schottky contacts. The Schottky films had a thickness of ~ 2000 Å. For the purpose of diode area study (effect of Schottky area on current transport), three different Al dot sizes (1/32″, 1/16″, 1/8″ in dia) were defined through a separate mask. At the initial stages of evaporation, the deposition rate was ~ 60-100 Å/ min. The rate was increased (~ 400 Å/ min) at a later stage when around 500Å of Al layer

had already been deposited. A pressure of 5×10^{-6} torr was maintained during Al evaporations.

Some samples were subjected to post ion-etch annealing prior to Schottky metallization. Low temperature annealing ($\leq$ 450°C) was done isochronally (for 10 mins) at different temperatures in a Thermolyne tube furnace under forming gas ambient.

4.3 Electrical Measurements

Electrical techniques used to evaluate diode properties are as follows :

- ▲ Current-voltage (I-V) characteristics with temperature as a parameter,
- ▲ Capacitance-voltage (C-V) characteristics with temperature as a parameter,
- ▲ Frequency dependence of capacitance at various biases and temperatures,
- ▲ Conductance-frequency (C-f) characteristics at different temperatures, and
- ▲ Complex impedance analysis.

Electrical measurements for all temperature runs were carried out in a MMR cryogenic microminiature refrigerator (model K 2205). The system is equipped with a K-77 temperature controller/indicator. The temperature control is achieved by a silicon diode and a resistor heater located at the device mounting stage. The temperature in the cryostat can be varied from -190 °C to 75 °C. with a variation of $\pm$0.5 °C. The system is cooled via high purity nitrogen gas. The gas flows under a pressure of $\simeq$ 1800 psi through a fine capillary. The refrigerator unit is shown in Fig. 11.

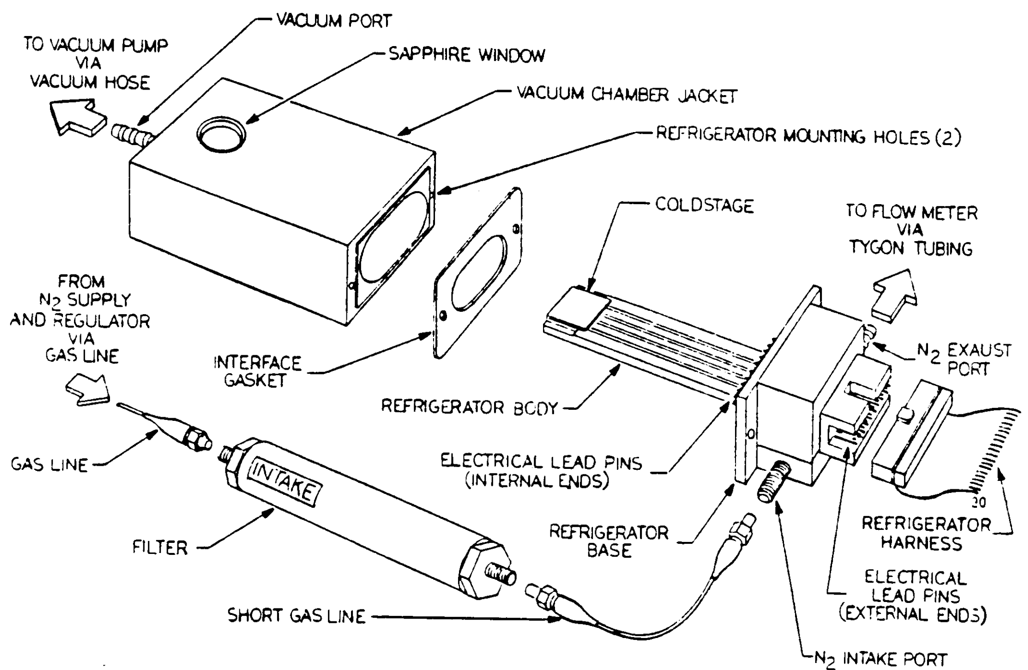


Figure 11. Refrigerator system IIB assembly.

For the pupose of electrical measurements, a thermally conductive grease was used to glue the diode to an alumina substrate and also to mount the substrate (with the diode) over the cold stage of the refrigerator. Figure 12 shows the schematic of a mounted doide on the cold stage. The mounted diode was connected to the end pads of the substrate by 1 mil thick gold wires. The gold wires were bonded by EPO-TEK H20E conductive epoxy and the epoxy cure was done at 65°C for 12 hrs. Figure 13 shows the layout of the electrical set up used for performing measurements.

Current-voltage and capacitance-voltage measurements were done using a Hewlett-Packard 4140B pA/voltage source meter and 4280A 1MHz C meter, respectively. The experimentation and the data collection were performed by means of Medusa[45] (name for an automated electrical analysis system for device characterization) through an IBM PC-AT. The temperature was however set manually through the K-77 controller.

Capacitance-frequency (C-f) and conductance-frequency (G-f) measurements were performed by means of Hewlett-Packard 4192 LF Impedance Analyzer. It was also used to perform complex impedance measurements. The experimental parameter setting and data collection for these measurements were done manually at various biases and temperatures. The errors involved in the electrical measurements are approximately within $\pm 5\%$. These errors are mainly due to the parasitic resistance and capacitance effects of the leads and contacts in the measuring circuit. Every effort was taken, during the course of experimentation, to minimize the effects of the parasitic components.

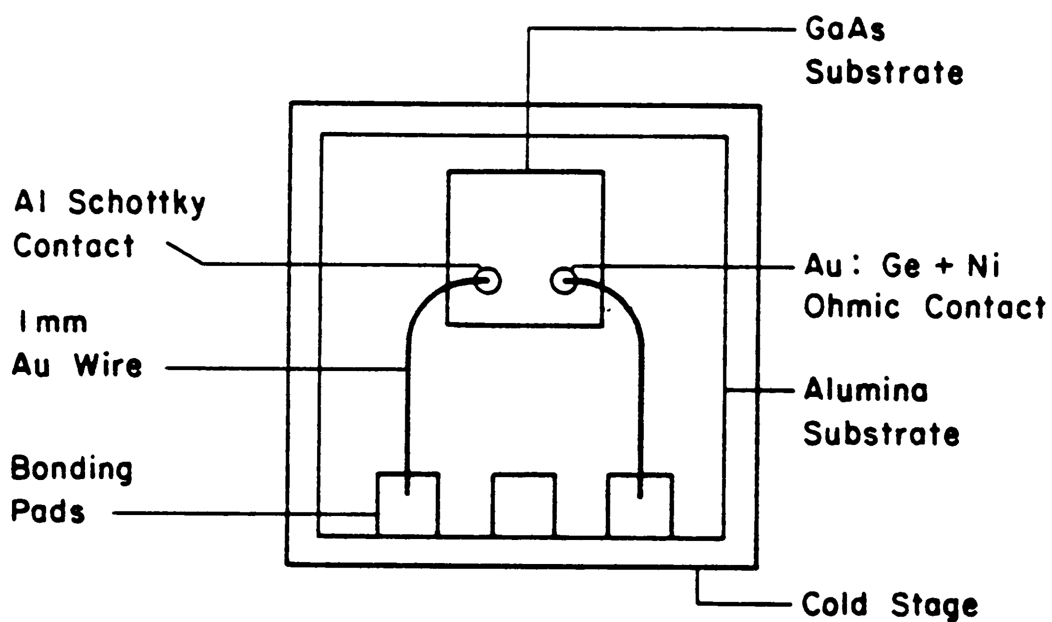


Figure 12. Schematic diagram for a mounted diode.

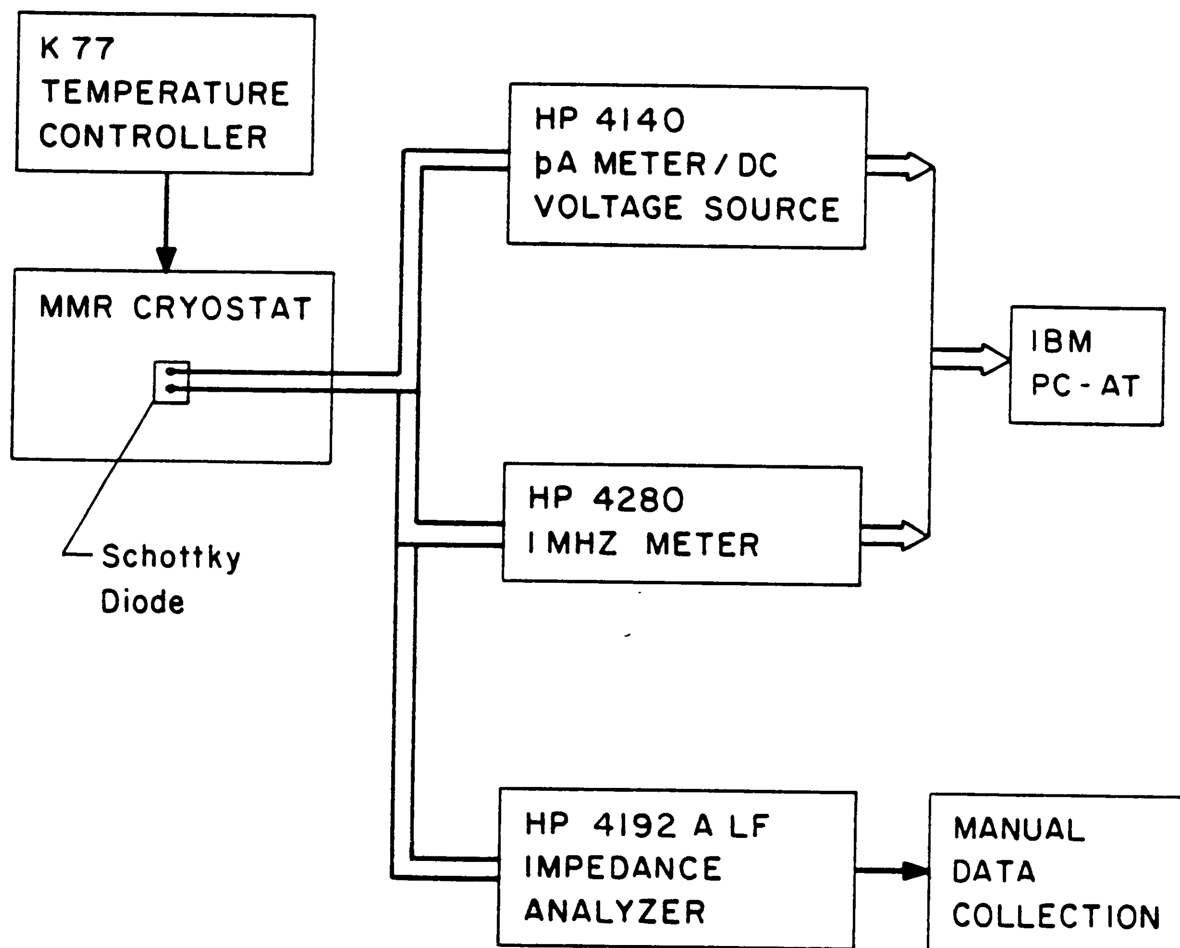


Figure 13. Schematic layout of electrical measurements on Schottky diodes.

Chapter V: Results and Discussion

5.1 Current-voltage (I-V) Measurements

a) Room temperature measurements :

Room temperature I-V measurements on virgin and IBE diodes are shown in Fig. 14. It is evident that the ion beam etched (IBE) diodes have soft reverse characteristics. Forward turn-on and reverse breakdown voltages increase with ion-etch energy. Forward characteristics, as shown in Fig. 15, reflect severe distortion of the IBE diode parameters. The diode parameters listed in Table 2 indicate an increase in ideality factor (n) and reverse saturation current (I_0) by ion etching. The increase in I_0 is, however, not monotonic with etch energy. Diodes with a 1keV etch exhibit higher reverse saturation than those with a 3keV etch. Reverse characteristics of virgin and IBE diodes are shown in Fig. 16. It is evident from this figure that the ion etching makes diodes "leaky". The I-V measurements on Airtron samples [Figs. 17 and 18] also show degradation of the ion-etched diode properties in the same manner as the Morgan samples.

The degradation of IBE diode parameters can be explained by means of a damage layer formed by ion bombardment. The increase in ideality factor n is related to the ion induced damage at the interface, being higher for a thicker interfacial damage layer. The factor n for

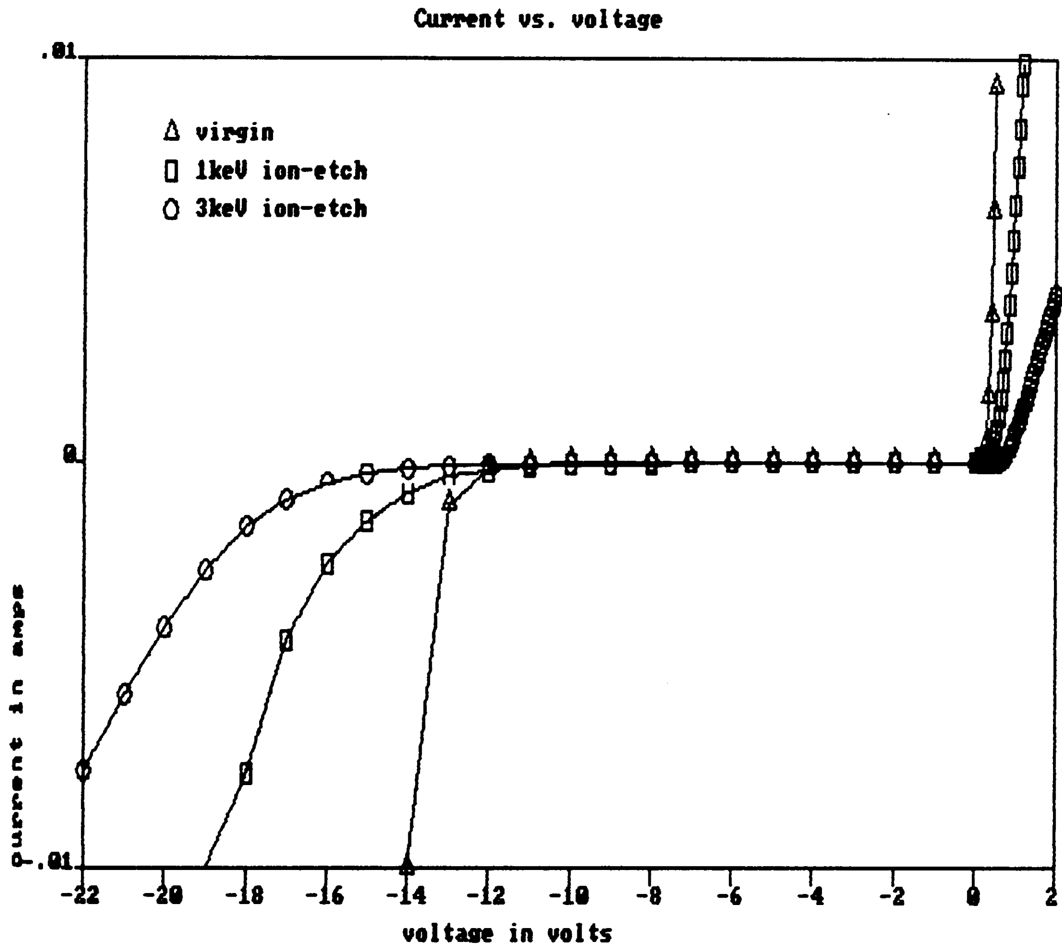


Figure 14. Room temperature I-V relationship: (Morgan samples).

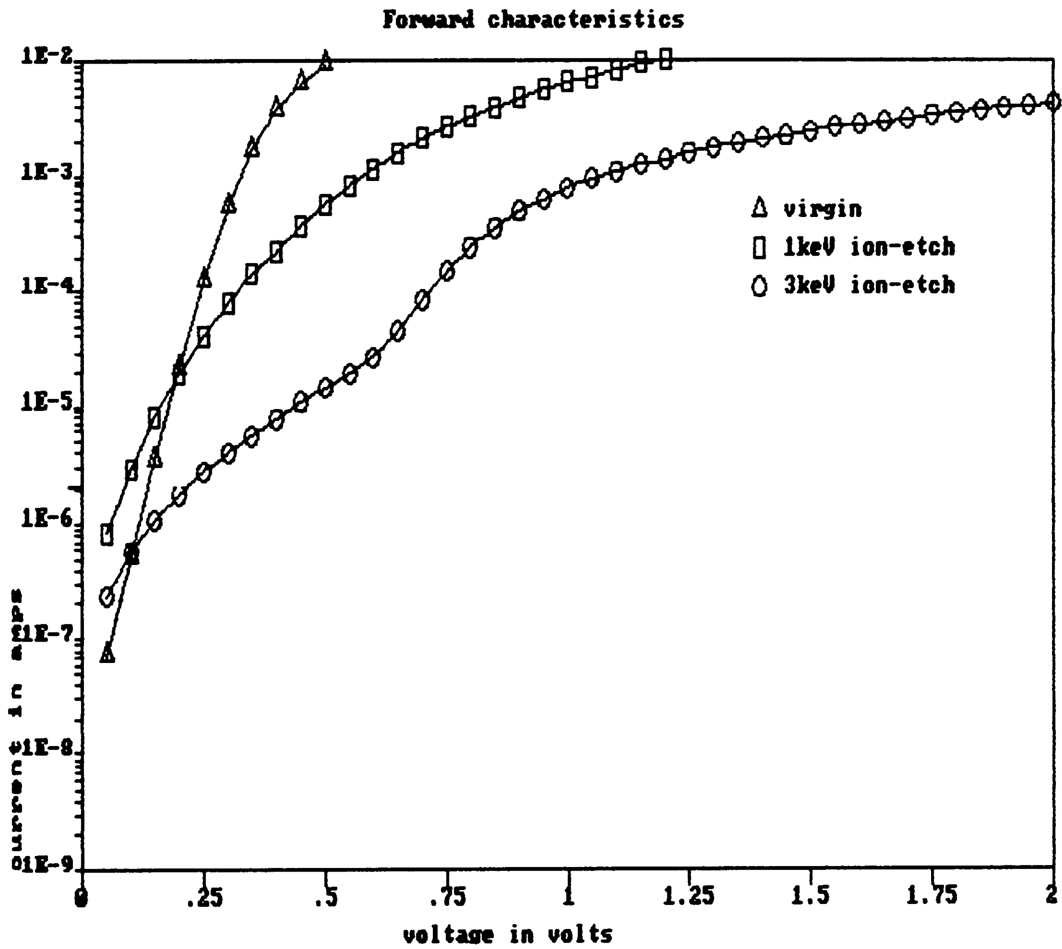


Figure 15. Forward diode characteristics at room temperature: (Morgan samples).

Table 2. Effect of ion-etch energy on diode parameters.

Samples	**n**	I_0 (amps)
virgin	1.09	1.49×10^{-8}
1keV	2.45	7.52×10^{-7}
3keV	4.23	2.6×10^{-7}

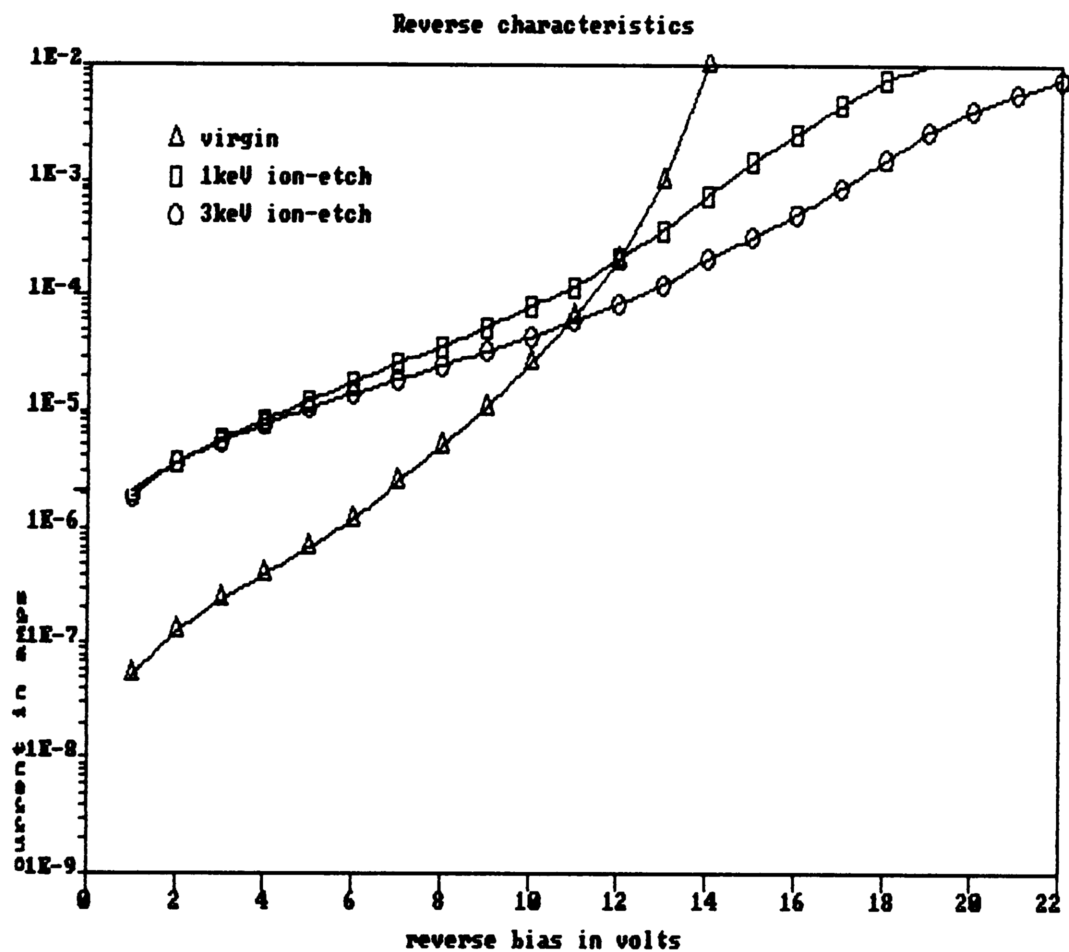


Figure 16. Reverse diode characteristics at room temperature: (Morgan samples).

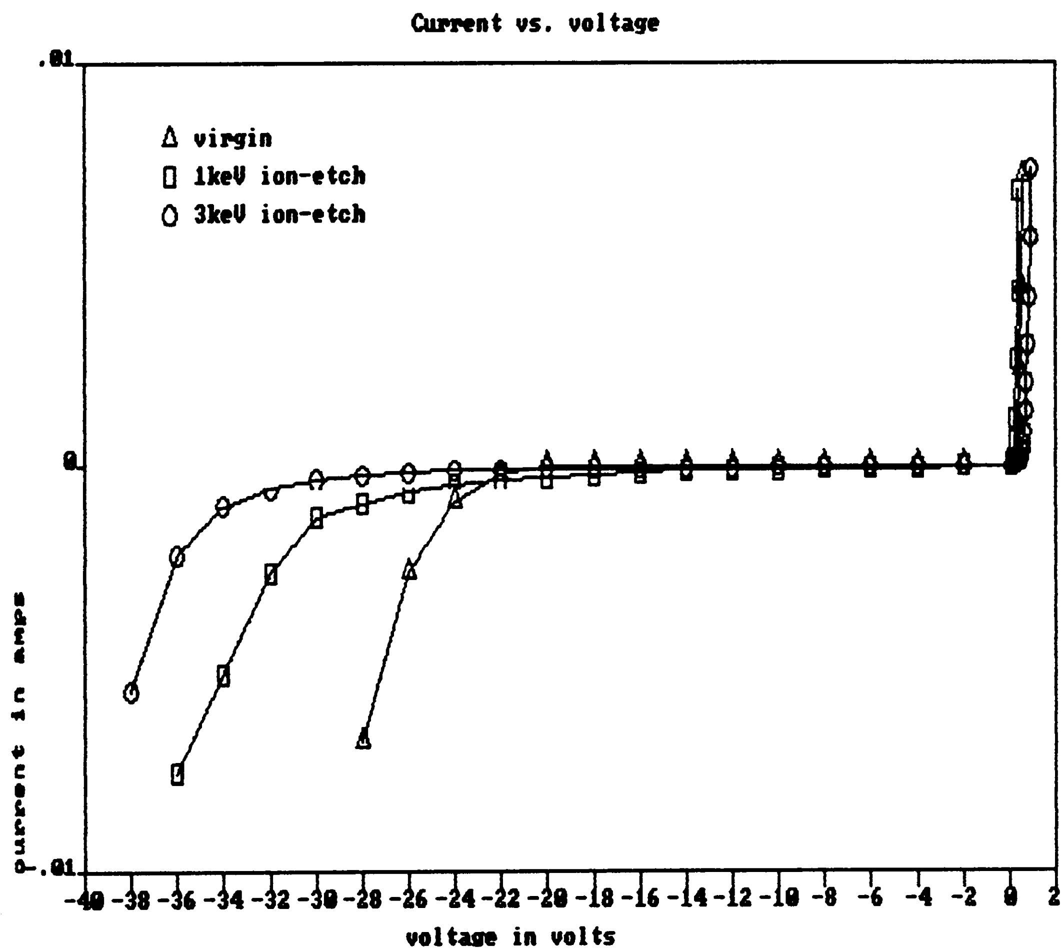


Figure 17. Room temperature I-V relationship: (Airtron samples).

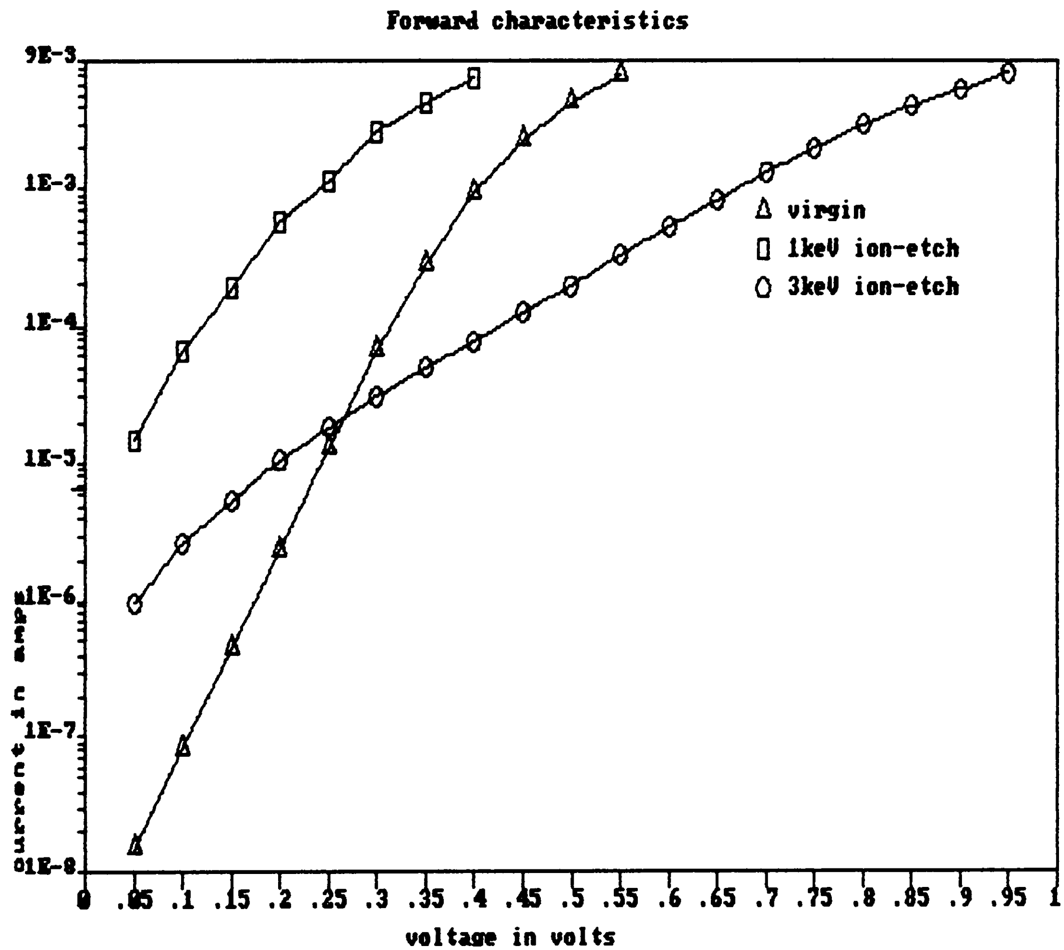


Figure 18. Room temperature forward characteristics: (Airtron samples).

a 3keV etched diode is affected the most [see Table 2]. This is presumably because of the formation of a thicker amorphous-like layer on top. The increase in I_0 is due to defect states, surface or bulk, that are introduced by ion etching. Figures 15 and 18 show that at low forward bias, the IBE diodes carry more current than the virgin diodes. This excess current in IBE diodes is attributable to trap assisted tunnelling transport.

The lower reverse saturation current in the 3keV etched diodes versus the 1keV etched diodes is likely to be due to a smaller number of ion-induced traps on the surface of the former. This appears to be consistent with Wang and Holloway's[20] finding of a lesser number of As vacancy related traps on a 3keV etched surface. Another possible explanation of lower I_0 on a 3keV etched diode as compared to a 1keV diode may be due to the damage saturation. It has been discussed by Ranbir Singh *et al.*[50] that an increase in I_0 on a Si bombarded surface depends on the modification of the surface layer, the extent of modification being dependent on the mass and energy of the incident ions. They propose that for 1keV, the surface layer is already conducting and a further increase in ion energy would result in more amorphicity and a decrease in conductivity. Similarly for GaAs, the extent of amorphicity and the defect assisted conductivity of the surface layer seem to compete with each other. Beyond a certain ion energy threshold, the number of ion-induced defects may get saturated and current transport through the surface layer is dominated by the extent of amorphicity. The phenomenon of higher reverse current in the 1keV etched diodes will be addressed later in sections 5.6 and 5.7.

The phenomena responsible for the increase in breakdown voltage in IBE diodes are not very clear. Few reports in the literature, on the contrary, indicate lowering of the breakdown voltage by ion sputtering[18,19]. The observed breakdown behavior can possibly be explained by a top amorphous layer and/or a compensated layer, if any, formed on the etched surface. In the absence of complete details, it is not possible to comment on reasons contributing to the increase in the breakdown voltage of IBE diodes.

b) Temperature dependent measurements :

Forward and reverse I-V characteristics of a virgin diode at various temperatures are shown in Figs. 19 and 20 repectively. The noticeable trend of increasing current with temperature agrees well with the theory. The virgin diode parameters, n and I_0, at different measuring temperatures are listed in Table 3.

It is evident from Table 3 that the ideality factor (n) increases at low temperatures. At such temperatures, the increase in n is due to the deviation from the true thermionic emission process. The Richardson plot [Fig. 21] yields a barrier height (ϕ_b) of 0.67eV and a modified Richardson constant (A^{**}) of $7.99 \times 10^4 \frac{A}{m^2K^2}$. The fact that the Richardson plot of a virgin diode is a straight line with a single activation energy indicates that the forward current is due to thermionic emission and that no significant generation-recombination and/or tunnelling current is present in the temperature range of -75°C to 50°C.

Figures 22 and 23 show the respective forward I-V characteristics of the 1keV and the 3keV IBE diodes at different temperatures. The plots, unlike those of virgin diodes, are far from being linear. The 3keV etched diodes have an N-shaped forward characteristic while the 1keV etched diodes exhibit similar features at low temperatures. The N-shaped anomaly in ln I-V plots of IBE diodes is indicative of the existence of multiple barriers at the Al-GaAs interface[48]. The flattening of the ln I-V plots at high forward bias is due to the series resistance effect.

Owing to the non-linear nature of the ln I-V plot, n and I_0 of an IBE diode are bias dependent and are thus difficult to estimate. Non-linearity of the plot is suggestive of the fact that the current transport is far from being controlled by the thermionic emission process. Under such a situation, data reduction methods for obtaining diode parameters are no longer valid. The IBE diode parameters n and I_0, shown in Table 2, are deduced from the best possible linear portion of plots in Fig. 15 and are thus likely to be error prone.

At first glance, however, one might conclude that the barrier height is lowered by ion etching because of an increase in reverse saturation current. The barrier height determined in this way for a non-thermionic nature of current transport is suspect, and hence unreliable. Therefore, no attempt has been made to compute ϕ_b of the IBE diodes by the I-V method.

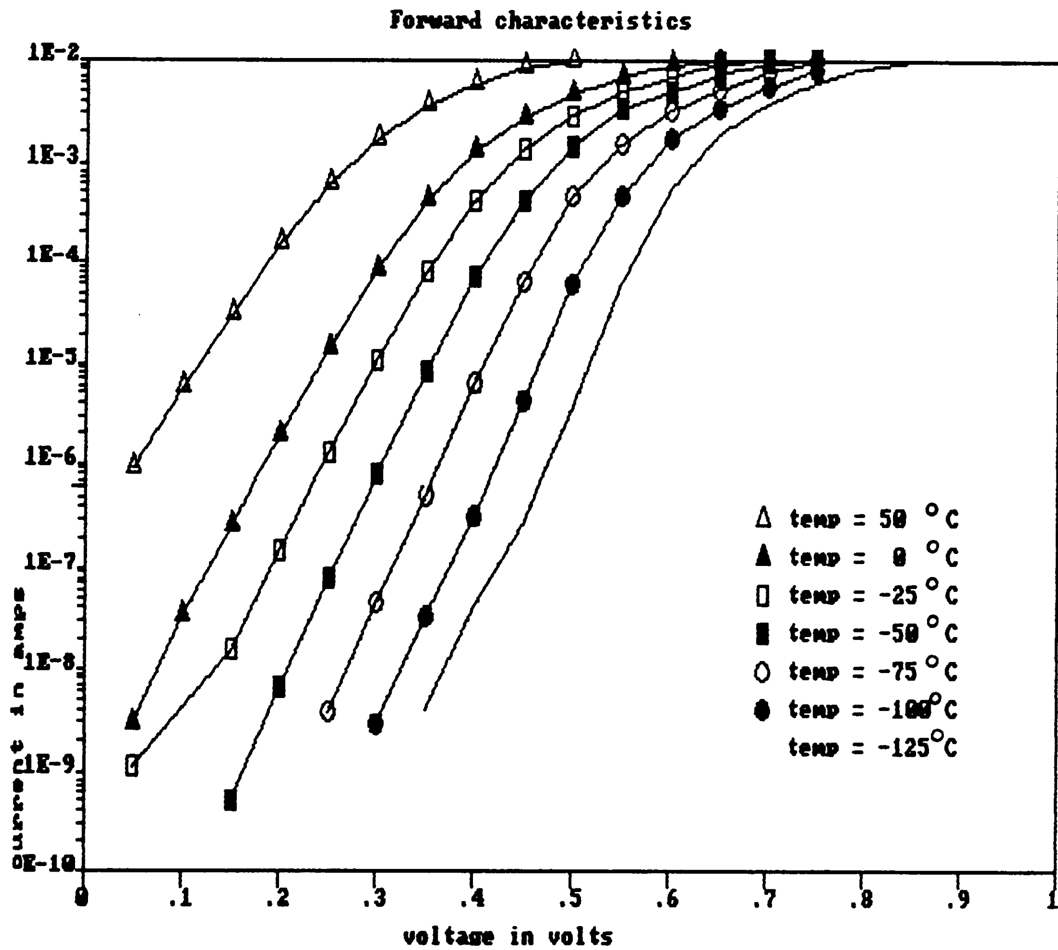


Figure 19. Forward I-V characteristics of a virgin diode.

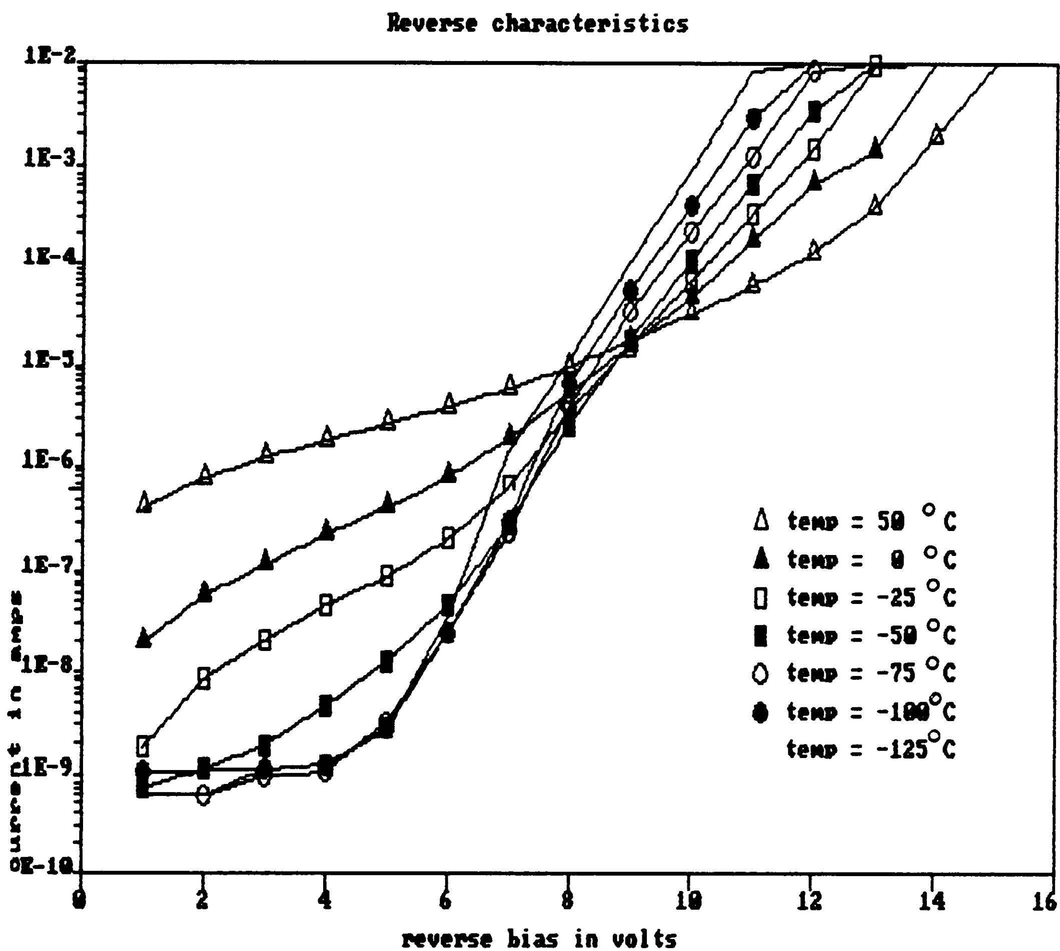


Figure 20. Reverse I-V characteristics of a virgin diode.

Table 3. Effect of temperature on virgin diode parameters.

Temperature (°C)	n	I_0 (amps)
-125	1.38	1.67×10^{-18}
-100	1.34	6.90×10^{-16}
-75	1.21	2.33×10^{-14}
-50	1.12	6.84×10^{-13}
-25	1.11	3.66×10^{-11}
0.0	1.06	6.20×10^{-10}
21.0	1.09	1.49×10^{-8}
50.0	1.09	2.10×10^{-7}
75.0	1.20	1.26×10^{-6}

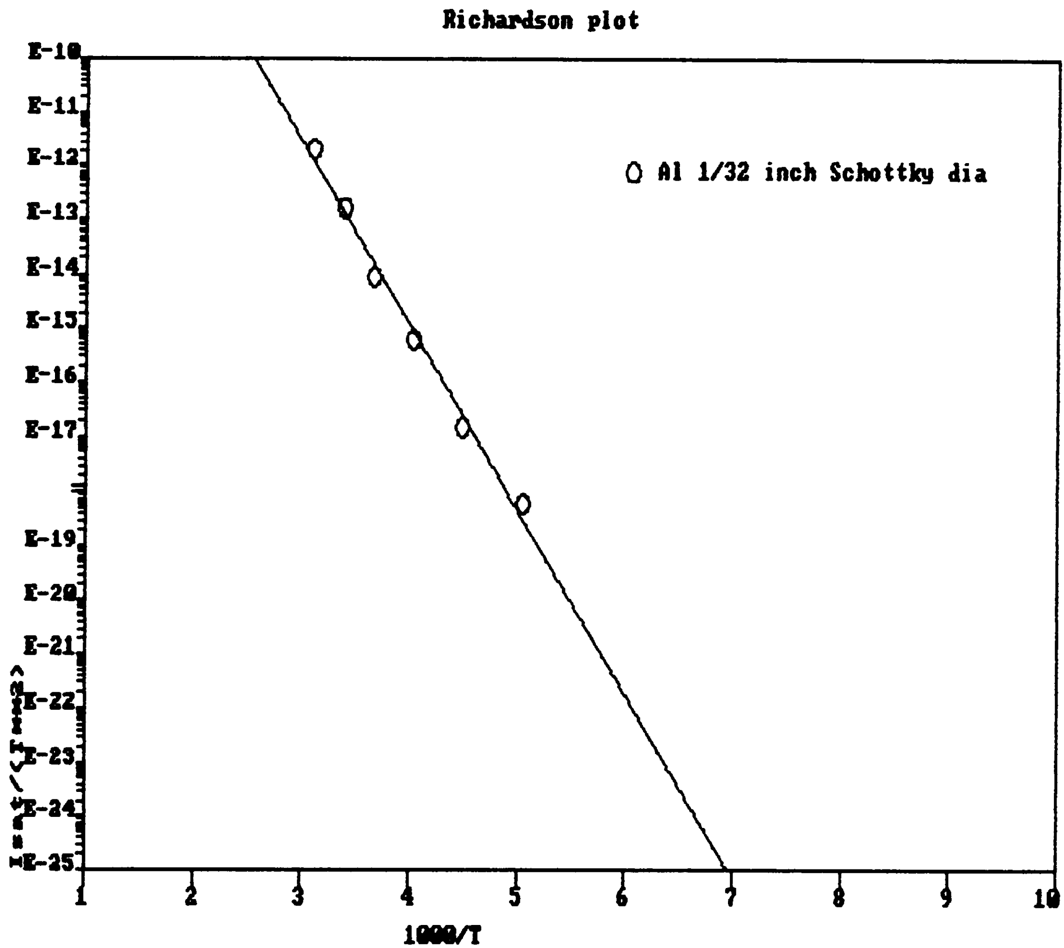


Figure 21. Richardson or activation energy plot of a virgin diode.

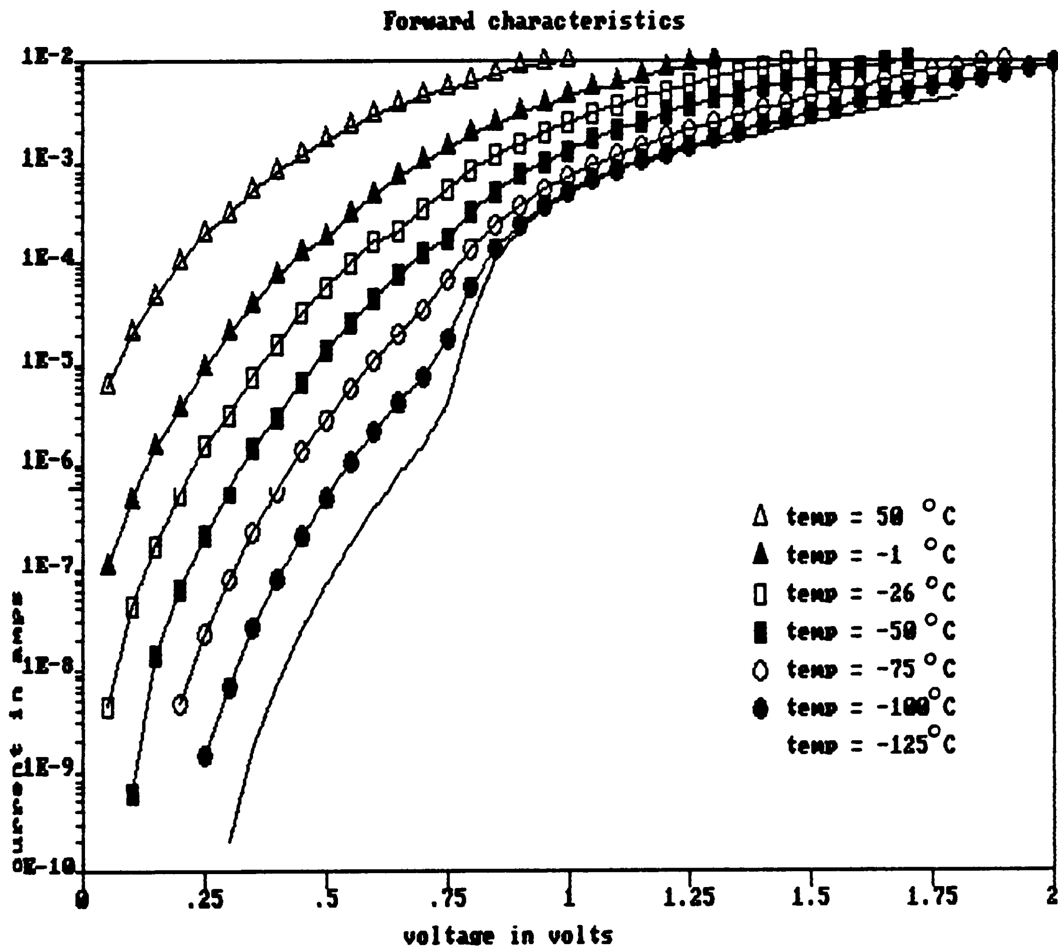


Figure 22. Forward characteristics of a 1keV etched diode at various temperatures.

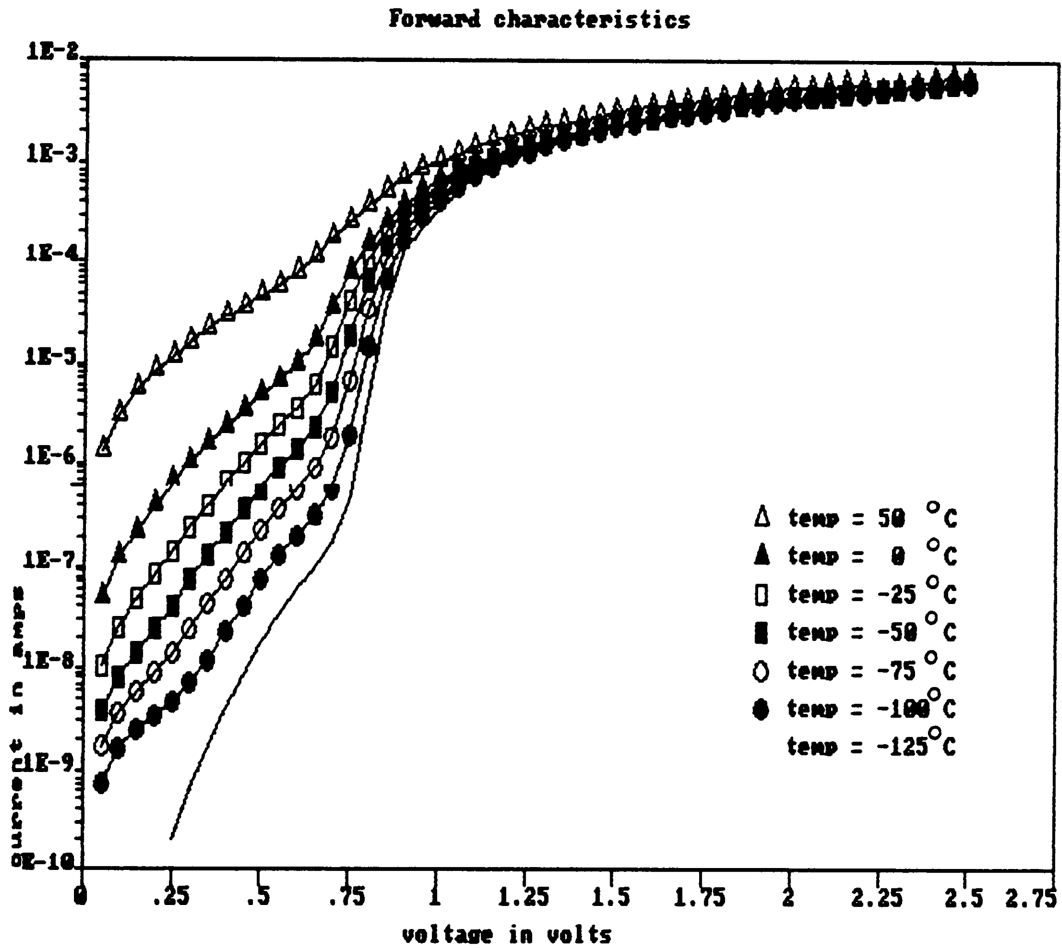


Figure 23. Forward characteristics of a 3keV etched diode at various temperatures.

5.2 I-V measurements on Schottky Diodes of Different Area

Diode area studies were performed to investigate the role of ion etching on surface leakage. Diodes of varying diameter (d) of 1/32", 1/16", and 1/8" were formed over virgin and ion beam etched surfaces with the objective to identify the dominant path of current flow. Figure 24 shows typical I-V relationships for three different diode diameters on a virgin surface.

For bulk controlled current transport, current through different diode geometries varies with the diode area ($I \sim d^2$). Currents, however, vary with the diode diameter for a total periphery controlled transport ($I \sim d$). Table 4 illustrates such variation in current on diodes formed on the virgin and the ion-etched surfaces. It is seen that for a virgin diode, current ratios are closer to the ratios of diode area (1 : 4 : 16), while in IBE diodes, current ratios decrease and are closer to the ratios of diode diameter (1 : 2 : 4). These results indicate the presence of a strong periphery component of current in ion-etched diodes. Ion etching therefore, creates a low resistance surface layer that partly shunts the depletion layer. The low resistance surface layer is indicative of the creation of a large number of ion-induced surface defect states. The diode area study performed on Airtron wafers showed similar trends and thus reinforces the finding on Morgan samples.

5.3 Capacitance-voltage (C-V) Measurements

The room temperature C^{-2} *vs.* reverse bias (V_R) relationships for virgin and IBE diodes of different Schottky diameters are shown in Figs. 25 and 26. Figure 25 shows the behavior observed on a 1/16" diameter Schottky diode, while Fig. 26 corresponds to that observed on a 1/32" diode diameter. Both figures indicate that, except near zero bias, the high frequency (1MHz) C^{-2} *vs.* V_R characteristics essentially remain unchanged after ion bombardment. The

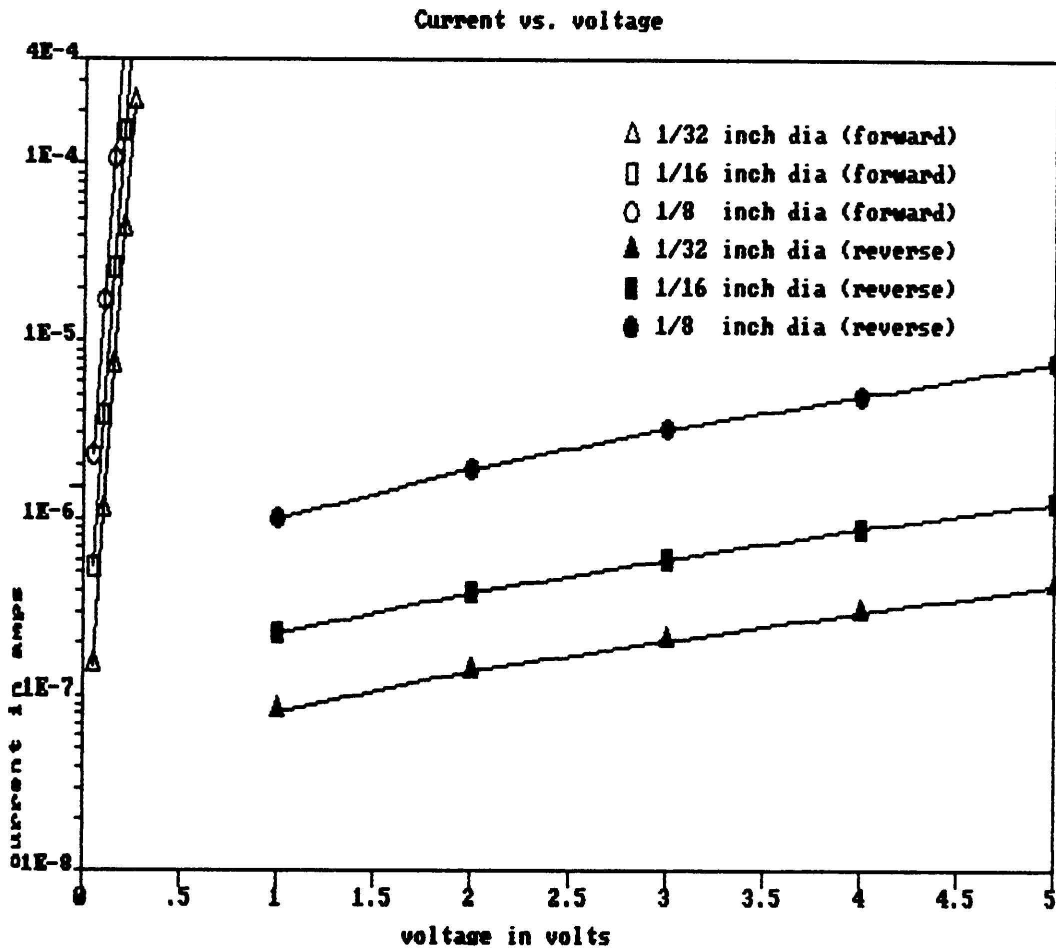


Figure 24. Effect of Schottky dia on current transport on a virgin surface: (Morgan samples).

Table 4. Effect of Schottky diameter on current ratios (Morgan samples).

Diode dot dia / samples	1/32″	1/16″	1/8″
virgin	1	3.2-5.3	11.85-16.85
1keV	1	3.0-3.2	6.8-8.8
3keV	1	2.3-3.6	4.9-9.0

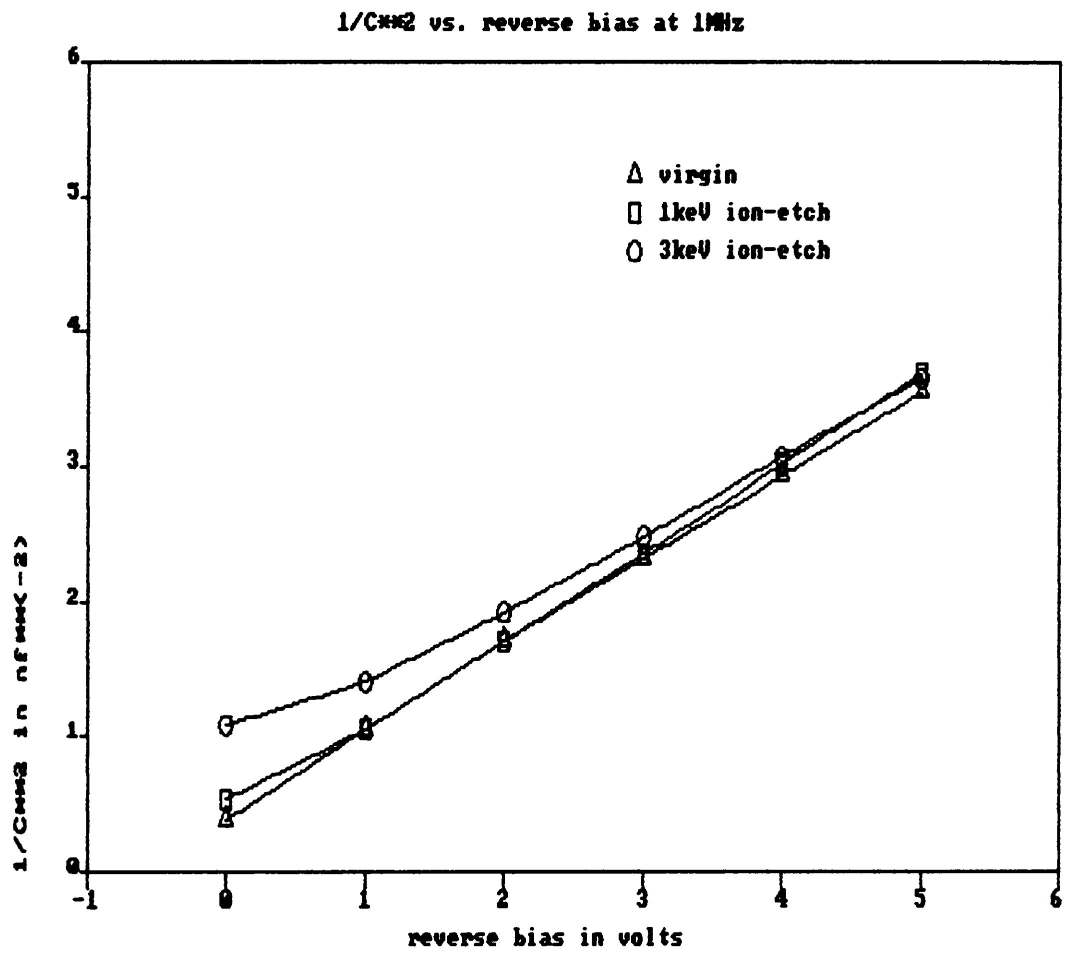


Figure 25. Room temperature C-V relationship: (Morgan, 1/16" dot dia).

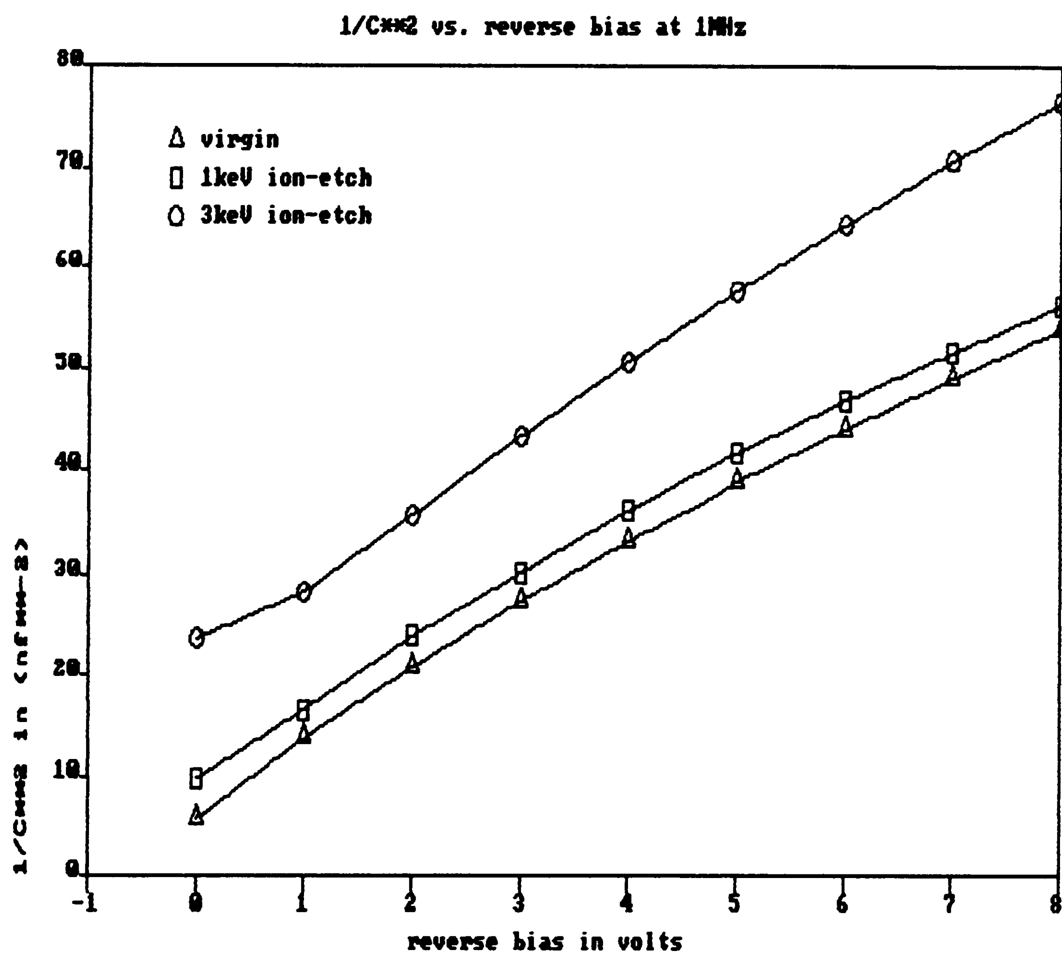


Figure 26. Room temperature C-V relationship: (Morgan, 1/32" dot dia).

decrease in high frequency capacitance with ion energy is noteworthy. Similar trends in $C^{-2} - V_R$ characteristics were observed for Airtron diodes.

C-V measurements performed at different temperatures for diodes fabricated over virgin, 1keV, and 3keV etched Morgan surfaces are shown in Figs. 27-29, respectively. Dopant density (N_d) and diffusion potential (V_d) at different temperatures are deduced by using eqns. (2.8) and (2.9). These values are listed in Table 5.

It is seen from Table 5 that a virgin surface has a room temperature doping density of $6.38 \times 10^{16} cm^{-3}$. This value compares well with the manufacturer specification of $6.46 \times 10^{16} cm^{-3}$. The table also indicates that the active dopant concentration remains practically unchanged after IBE. The variations observed in the values of N_d may well lie within the scope of experimental error. Figures 25 and 26 indicate that at a higher reverse bias, the slopes of the C^{-2} *vs.* V_R plots of the virgin and the IBE diodes tend to equalize. This is due to the fact that the C-V measurements, at high reverse bias probe deep inside the crystal, which in all likelihood is unharmed by the Ar^+ ions. As a weak approximation, the depth of the ion-damage is the depth of the space charge edge at that level of reverse bias where the slopes of C^{-2} *vs.* V_R plots of the virgin and the IBE diodes become nearly equal. Accordingly, it can be predicted [from Figs. 25 and 26] that the ion-damage depth for a 1keV surface extends to at least $\sim$ 1950Å (i,e. the depletion edge depth at 1 V reverse bias), while for a 3keV surface, the depths extend to at least $\sim$ 2200Å (i,e. the depletion edge depth at 1.5 V reverse bias).

A decrease in the C^{-2} *vs.* V_R slope of an ion-etched diode near zero bias [see Figs. 25, 26] is indicative of an increase in effective donor concentration in the ion-damage layer. This is in agreement with reports found in the literature about the formation of a donor-like damage layer by ion etching[2,19,20,21,27]. Reduction in the high frequency capacitance of an IBE diode is attributable to the formation of an amorphous-like surface layer. The amorphous layer capacitance (C_A) acts in series with the depletion layer capacitance (C_d) and thus lowers the overall capacitance (C). The capacitance C of the IBE diodes decreases with increase in ion energy. This directly implies the formation of a thicker amorphous layer at higher etch energies.

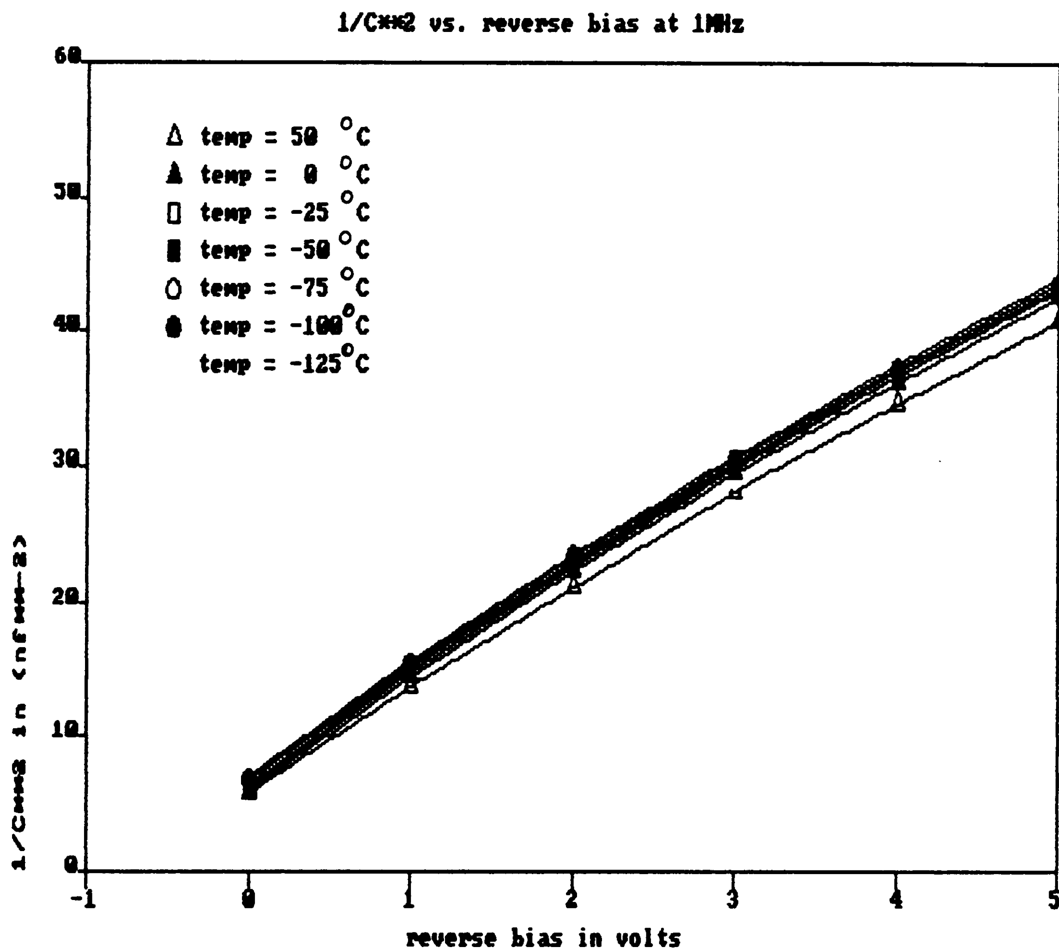


Figure 27. C-V relationship of a virgin diode at various temperatures.

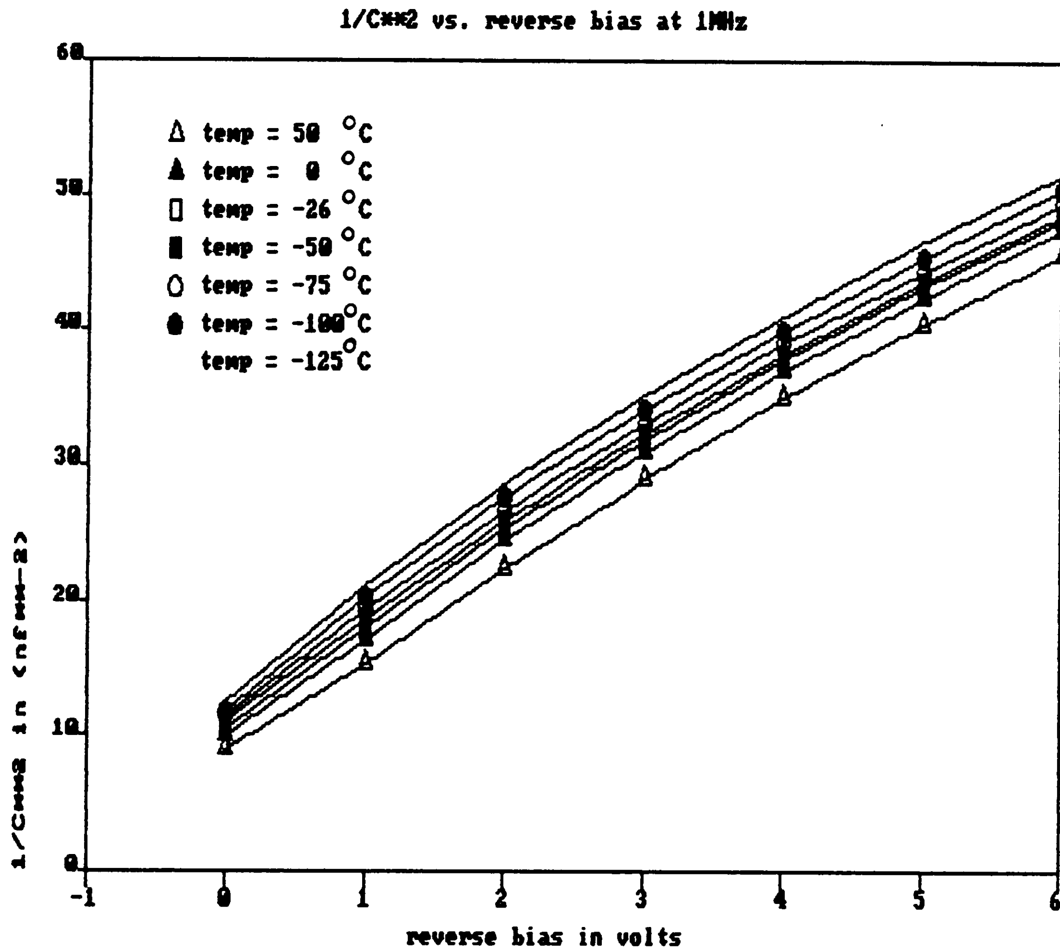


Figure 28. C-V relationship of a 1keV etched diode at various temperatures.

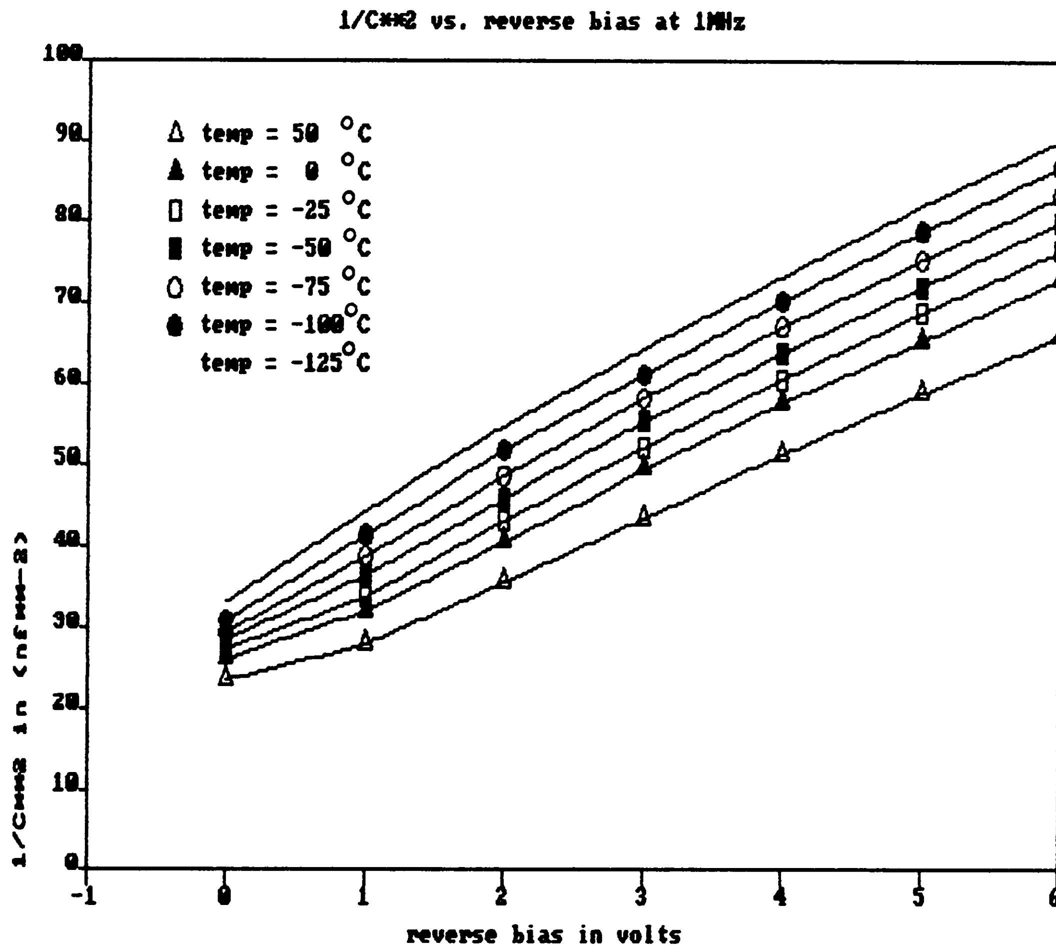


Figure 29. C-V relationship of a 3keV etched diode at various temperatures.

Table 5. N_d, V_d of virgin and IBE diodes at different temperatures.

conditon / Temp °C	virgin		1keV		3keV	
	$N_d \times 10^{16}$ (cm^{-3})	V_d (V)	$N_d \times 10^{16}$ (cm^{-3})	V_d (V)	$N_d \times 10^{16}$ (cm^{-3})	V_d (V)
-150	5.77	.966	6.20	1.9		
-125	5.80	.946	6.13	1.75	4.75	3.63
-100	5.80	.923	6.20	1.68	4.77	3.34
-75	5.84	.897	6.38	1.64	4.85	3.13
-50	5.80	.869	6.45	1.59	4.99	2.98
-25	5.80	.837	6.40	1.52	5.13	2.81
0.0	5.80	.813	6.57	1.46	5.35	2.74
21.0	6.38	.827	6.65	1.39	6.13	2.78
50.0	6.06	.769	6.80	1.33	5.90	2.58
75.0	6.16	.757	6.80	1.27	6.00	3.00

The room temperature barrier height (ϕ_b), computed by the C-V method, of a virgin diode is ~ 0.90eV. The difference in ϕ_b values found by I-V and C-V methods is possibly because each method probes a different portion of the interface region. Forward I-V probes the region of the depletion edge at equilibrium to the region near the metal-GaAs interface. C-V measurement on the other hand, probes the depletion edge in bulk and away from the interface. The C-V method, in presence of a thick interfacial damage layer, gives an unreliable estimate of V_d and ϕ_b. This is reflected in unusually high values of V_d for the IBE diodes [see Table 5]. Accordingly no attempt has been made to deduce the barrier height of IBE diodes by the C-V method. One final comment can be made about the sensitivity of C-V measurements. It is observed that, except at low reverse bias, there is not much damage information available from the rest of C^{-2} *vs.* V_R plot. High frequency (1MHz) C-V measurements, unlike I-V measurements, are thus relatively insensitive to the effects of surface damage by ion bombardment in the ion energy range of 1-3 keV.

5.4 Capacitance-frequency (C-f) Measurements

C-f measurements were performed over a wide range of temperature and bias. The effect of frequency on the room temperature diode capacitance is shown in Figs. 30 and 31. The plot in Fig. 30 shows the C-f behavior of a 1/32 inch diameter diode made from a Morgan wafer, while Fig. 31 shows the same behavior of a 1/16 inch diameter diode formed from an Airtron wafer. Both figures reveal a strong frequency dependence of the IBE diode capacitance. At low frequencies (<1kHz), the capacitance of the IBE diode rises sharply. Virgin diodes, on the contrary, exhibit a frequency independent capacitive behavior in the measured frequency range of 100Hz - 1MHz. The low frequency capacitance structure in the case of IBE diodes is attributed to the presence of a large number of ion-induced defect states in the damage layer. These defect states or traps have a finite time constant (τ) associated with charging and discharging. They contribute to junction capacitance at a signal frequency less than the inverse

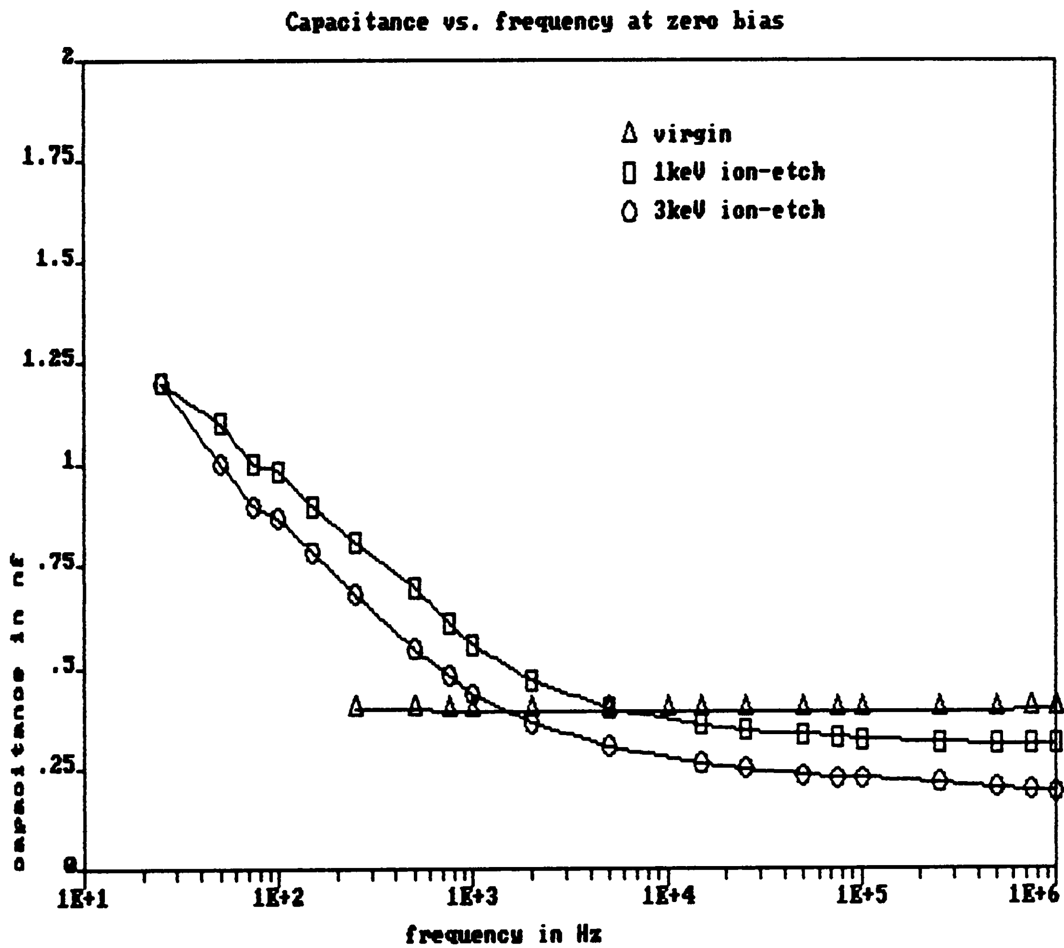


Figure 30. Effect of frequency on room temperature diode capacitance: (Morgan samples).

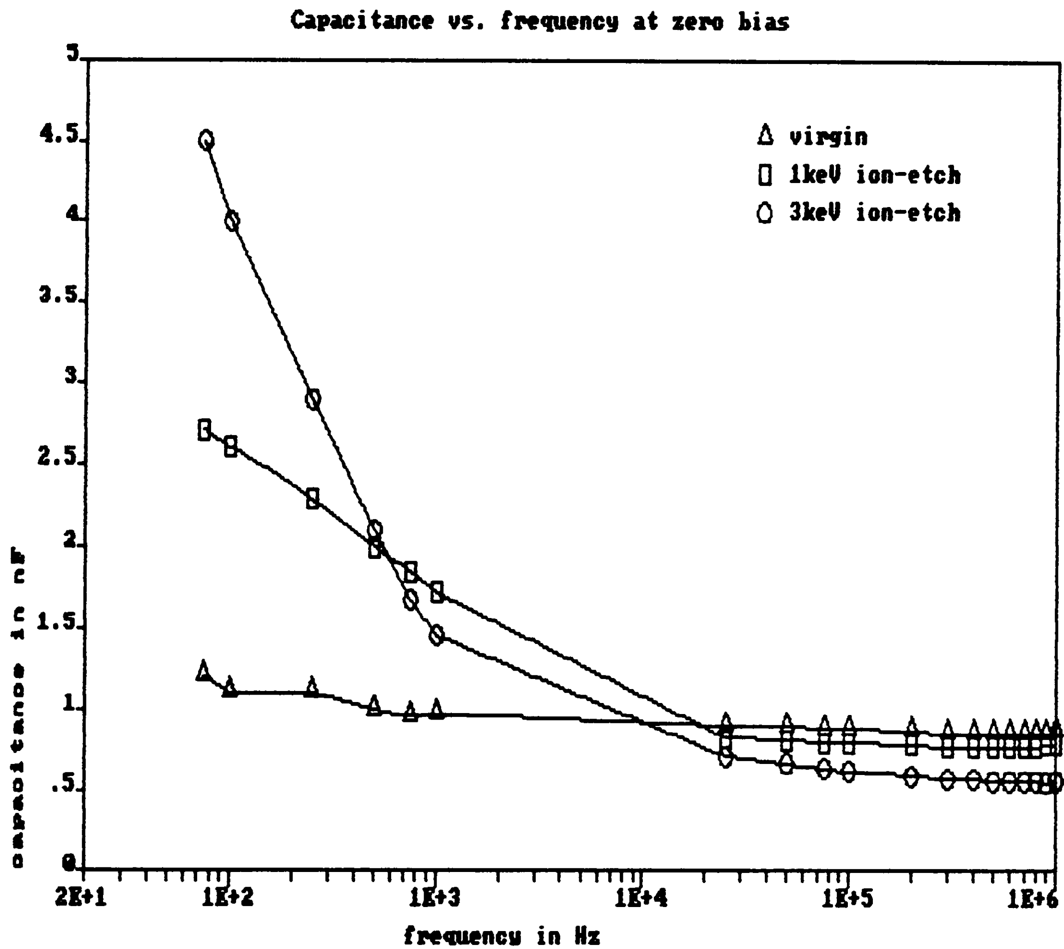


Figure 31. Effect of frequency on room temperature diode capacitance: (Airtron samples).

of their time constant. The rise in capacitance, or the capacitance "tail" at low frequencies, is suggestive of the creation of donor-like traps in the damage layer. The trap concentration at room temperature is high enough to effectively "clamp" and reduce the zero bias depletion width at low frequencies. The capacitance due to these traps (C_t), at low frequencies, dominates and superimposes on the shallow donor capacitance (C_d) and the amorphous layer capacitance (C_A). The high frequency capacitance, on the other hand, is solely due to the series combination of C_d and C_A.

The low frequency capacitance "tail" can be varied by modulating temperature and/or bias. The "tail" size depends strongly on the density of defect states and their activation energy (or energy level). The low frequency capacitance "tail" gets bigger with increase in the ion-induced trap density. For traps located deeper in the band gap, the response and hence the "tail" appears at lower frequencies.

The effects of temperature on the C-f relationship of diodes formed on virgin, 1keV, and 3keV etched surfaces are shown in Figs. 32, 33, and 34 respectively. Virgin diodes showed no frequency dispersive capacitance in the measured temperature range (-100 to 50 °C). This is indicative of the fact that the capacitance in virgin diodes, in all probabilty, is due to shallow donors only. In the case of the ion-etched surfaces, temperature has a strong influence on the low frequency capacitance behavior. The rise in low frequency capacitance, as can be seen from Figs. 33 and 34, diminishes at low temperatures. The "tail" practically disappears at a temperature of $\sim$ -25°C for both the 1keV and the 3keV etched diodes. The strong temperature dependence of low frequency capacitance of the IBE diodes is associated with the charge state of the ion-induced traps. At low measuring temperature, the traps are presumably frozen and consequently the electron density in the top damage layer decreases considerably. Traps or the deep levels can contribute to the capacitance only beyond a certain temperature threshold, which depends primarily on their energy levels. The temperature threshold being higher for traps that are located deeper from the conduction band edge.

Figures 35, 36, and 37 show the effect of reverse bias on diodes formed on the virgin, 1keV, and 3keV etched surfaces. The virgin diode retains the frequency independent

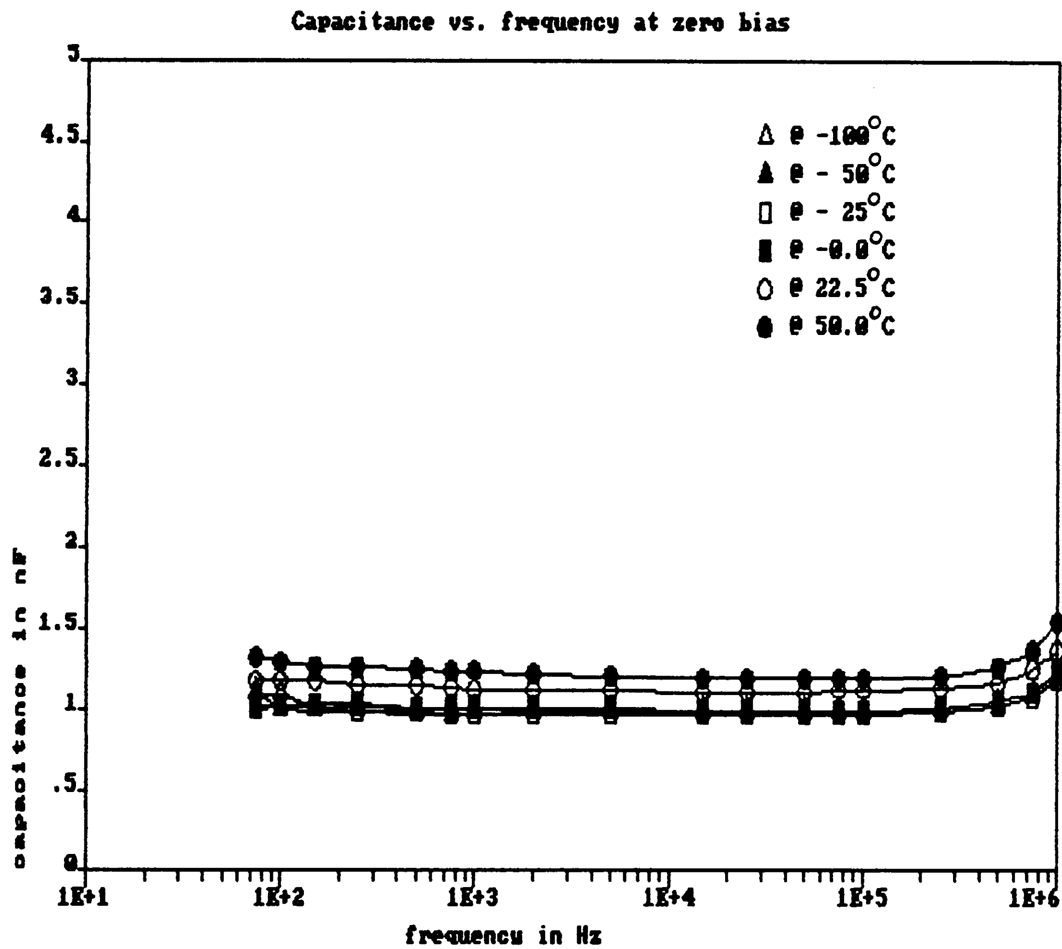


Figure 32. Effect of temperature on C-f relationship of a virgin diode.

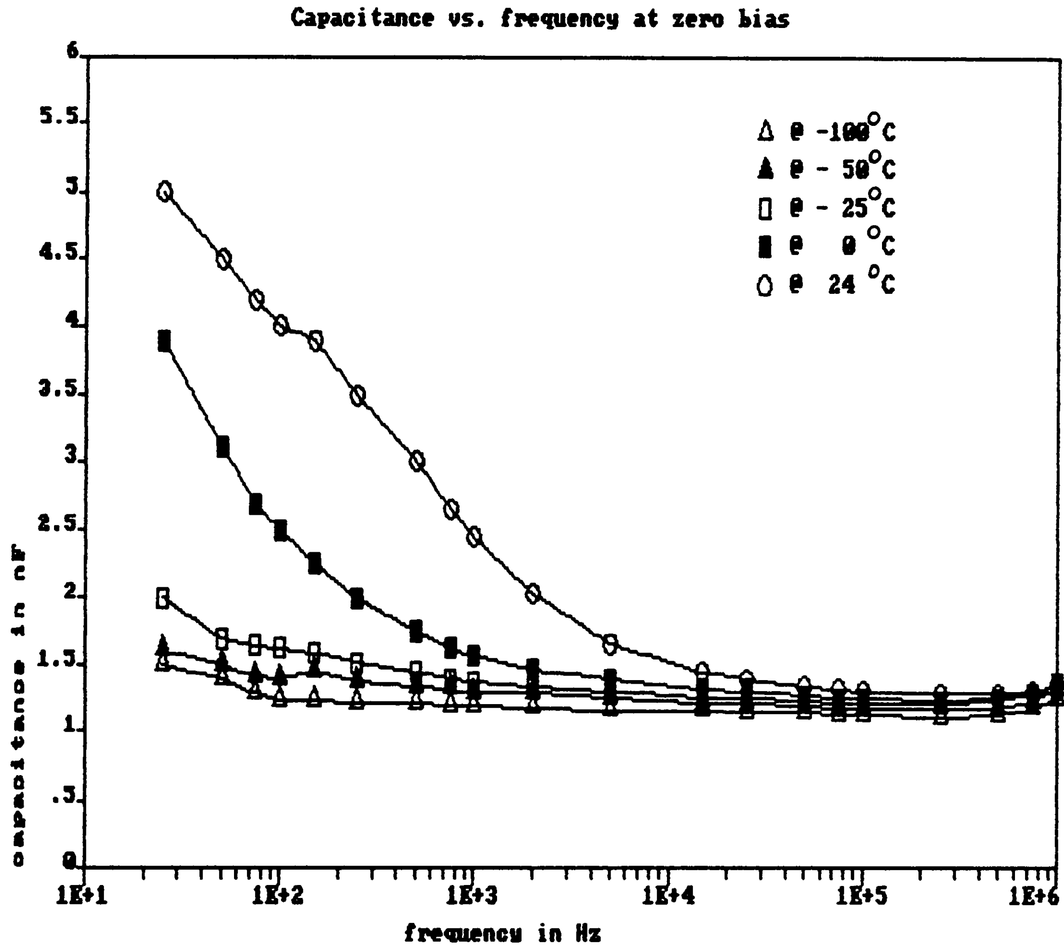


Figure 33. Effect of temperature on C-f relationship of a 1keV etched diode.

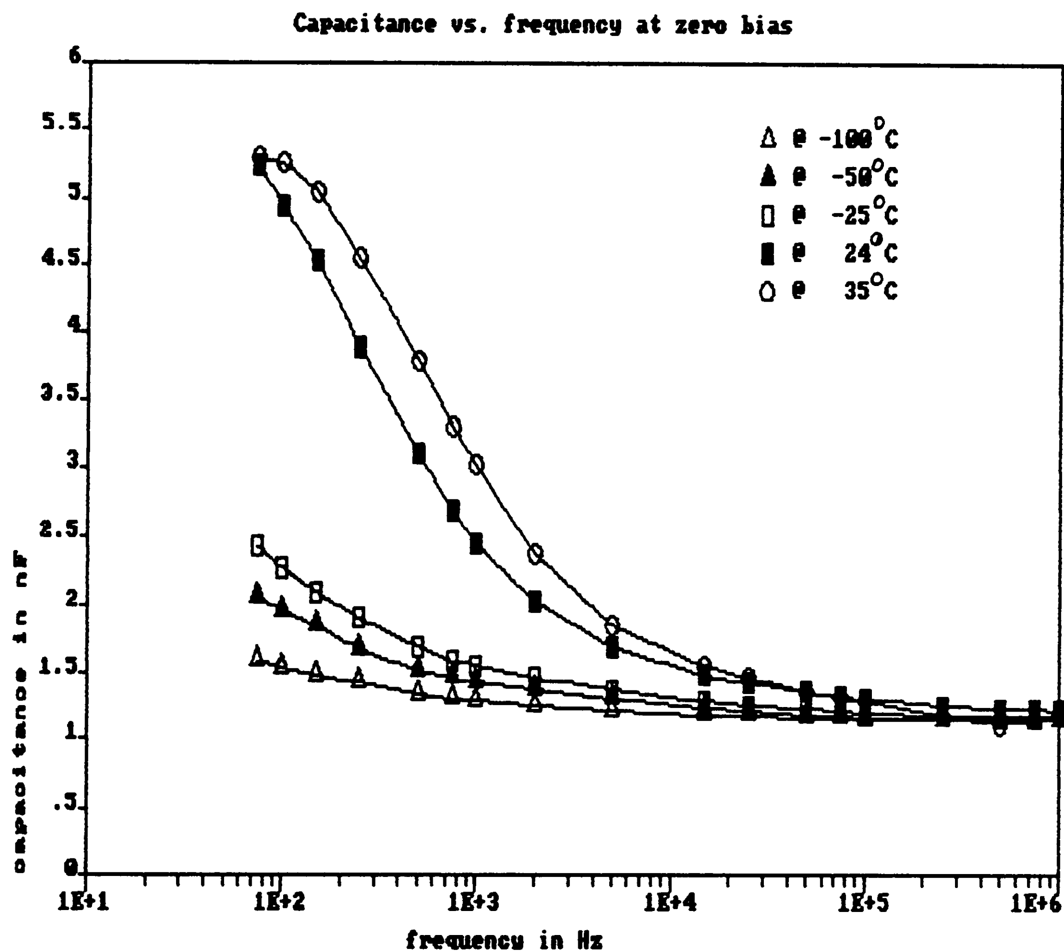


Figure 34. Effect of temperature on C-f relationship of a 3keV etched diode.

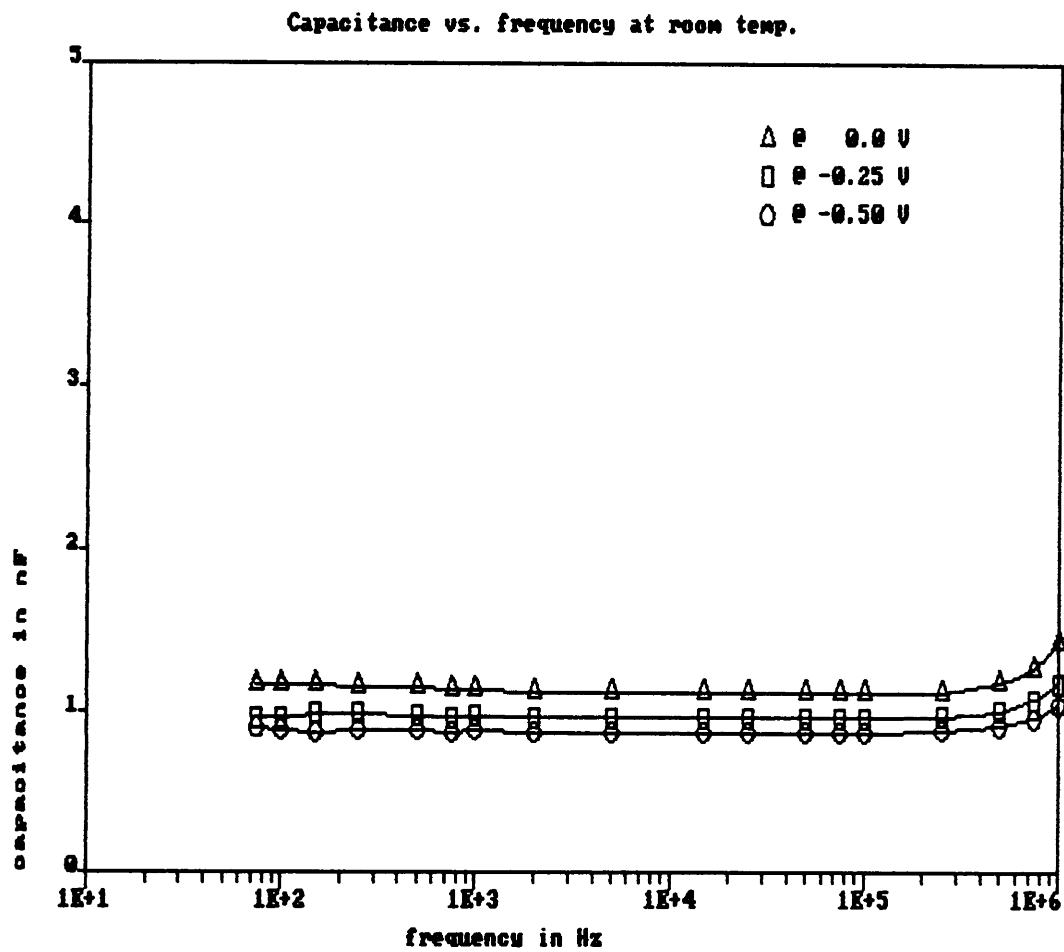


Figure 35. Effect of reverse bias on C-f relationship of a virgin diode: (Morgan sample).

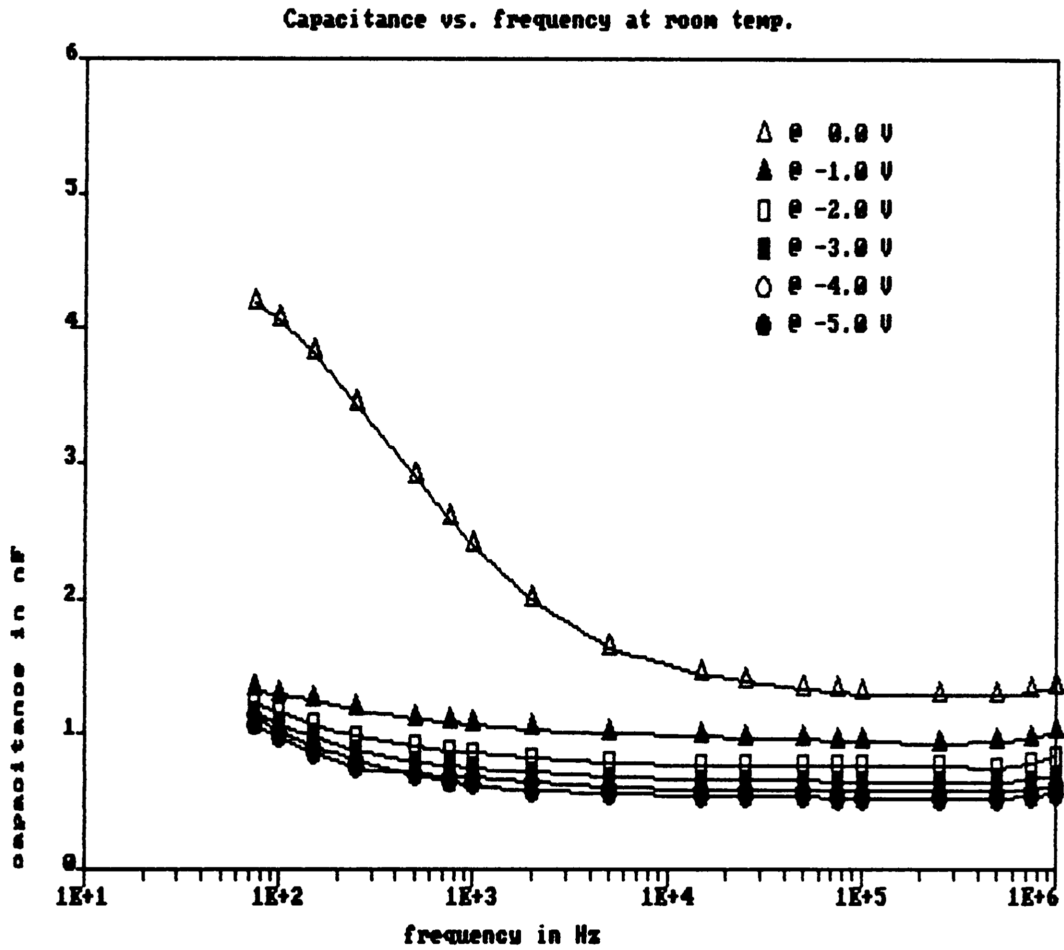


Figure 36. Effect of reverse bias on C-f relationship of a 1keV etched diode: (Morgan sample).

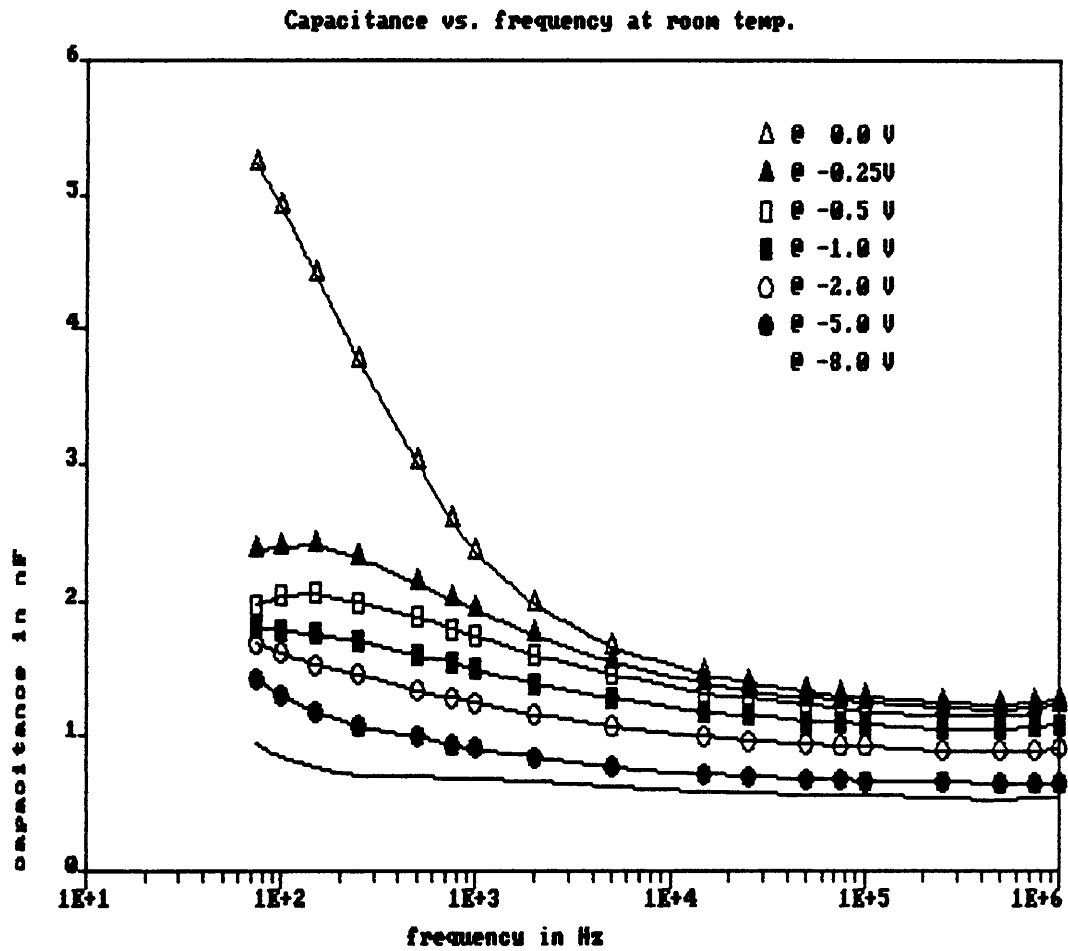


Figure 37. Effect of reverse bias on C-f relationship of a 3keV etched diode: (Morgan sample).

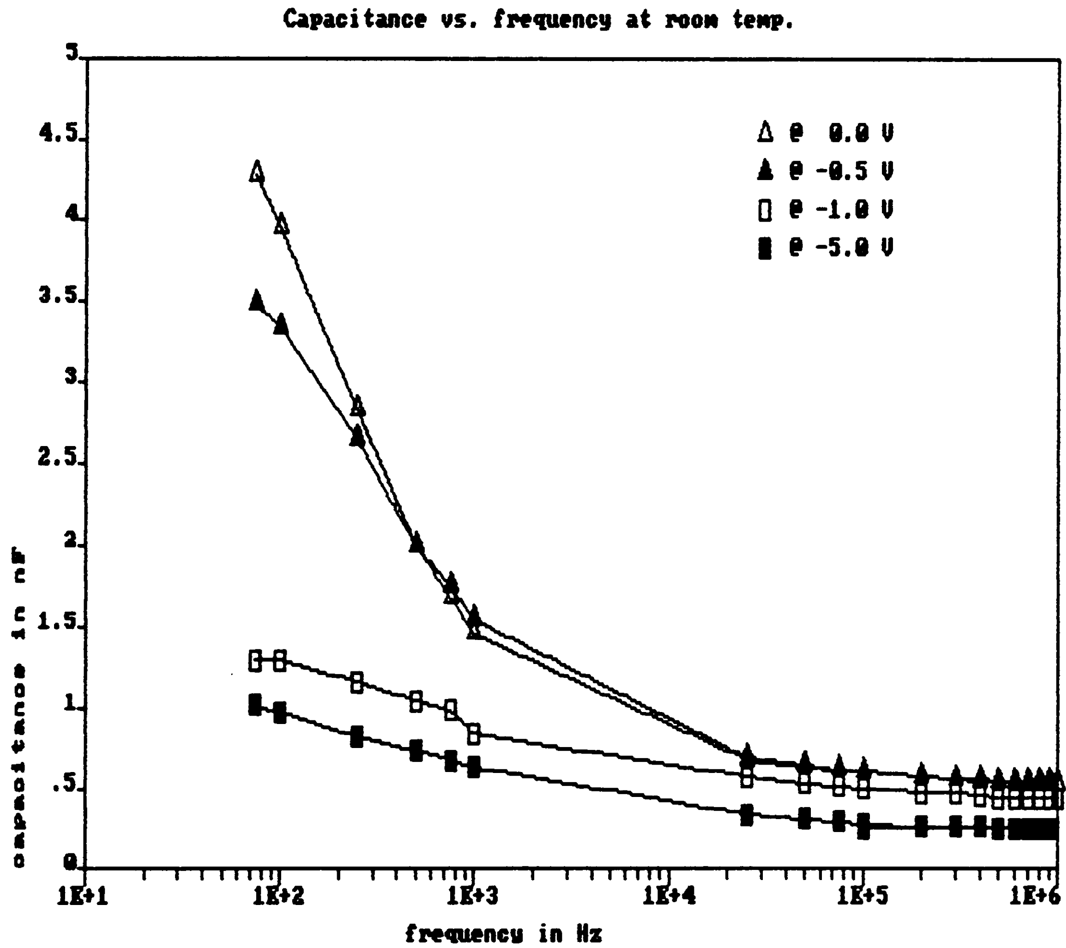


Figure 38. Effect of reverse bias on C-f relationship of a 3keV etched diode: (Airtron sample).

capacitance characterictics at reverse biases, as shown in Fig. 35. The decrease in capacitance with increase in reverse bias is uniform in the entire frequency range of 100Hz to 1MHz. Figures 36 and 37 reveal that the low frequency capacitance rise of the IBE diodes reduces drastically at low reverse bias of approximately 0.5 to 1 V. A similar effect of reverse bias was found on a 3keV etched diode made out of an Airtron wafer. This is illustrated in Fig. 38.

Although the frequency dispersion effect is expected to be weaker at large reverse bias[48,49], the experimental results indicate that the capacitance "tail" is somewhat more sensitive to reverse bias than that expected from the theory. The near disappearance of the "tail" at small reverse bias ($\sim$ 1 V) is suggestive of the fact that the high trap density ($>$ donor density) damage is likely to be confined to the top amorphous-like layer (around a few hundreds of angstroms thick) and a very narrow portion of the damage diffused layer. The reverse bias of $\sim$ 1 V is sufficient enough to shift the space charge region to a less damaged region where the ion-induced trap density is lower than the dopant concentration, and accordingly traps have no effect on the subsequent C-f relationship of the ion-etched diodes. This result is partly in concordance with that of the C-V measurements (see section 5.3, where at about 1 V reverse bias, the C-V characteristics of the IBE diodes and virgin diodes are nearly similar). The sudden disappearance of the frequency effect at low reverse bias will be addressed in greater detail in section 5.5.

5.5 Trap Analysis

Frequency dispersion of the capacitance of IBE diodes, and its dependence on temperature, can be used to estimate the ion-induced trap parameters. The low frequency capacitance rise, near zero bias, was explained in the previous section by proposing a parallel model of C_T (due to the traps) and C_D (due to the dopants and the amorphous layer

capacitances in series). Accordingly, the total capacitance C of an IBE diode can be expressed as :

$$C = C_D + C_t \tag{5.1}$$

At high frequencies, C approaches C_D because of the inability of the traps to follow the measuring signal. At low frequencies, the additive effect of C_t is manifested in the form of the capacitance "tail".

The trap analysis makes use of two assumptions in order to express C_t in the form of eqn. (2.12). The assumptions under which C_t can be expressed in such a closed form are listed below[46] :

a. Deep trap density exceeds that of the shallow level density.

b. Deep traps have discrete energy levels.

It is not known if the IBE diodes conform completely to the above conditions. However, they may be assumed true as a first approximation in obtaining trap parameters.

The frequency dependence of C_t, as obtained by using C-f data and eqn. (5.1), for 1keV and 3keV etched diodes, is shown in Figs. 39 and 40, respectively. Equation (2.12) suggest that the C_t dependence on measuring frequency would be of the form, $C_t \sim f^{-0.5}$. Experimentally, C_t of the IBE diodes was found to have frequency dependence of the form varying between $f^{-0.5}$ to $f^{-0.6}$ [see Figs. 39, 40.]. This implies that the slope of the logarithmic plot of C_t *vs. f* for the ion-etched diodes is fairly close to that of the theoretical prediction of -0.5. The trap density (N_T) is inferred from the intercept on the log C_t axis. The trap density values so deduced for the 1keV and the 3keV etched diodes, at room temperature, are $4.6 \times 10^{17}\,cm^{-3}$ and $1.28 \times 10^{17}\,cm^{-3}$ respectively. It is interesting that, for the Morgan material, the 3keV etched diodes appear to have a smaller trap density than the 1keV etched diodes. This is indicated by the larger low-frequency dispersion for the 1keV case (Fig. 30).

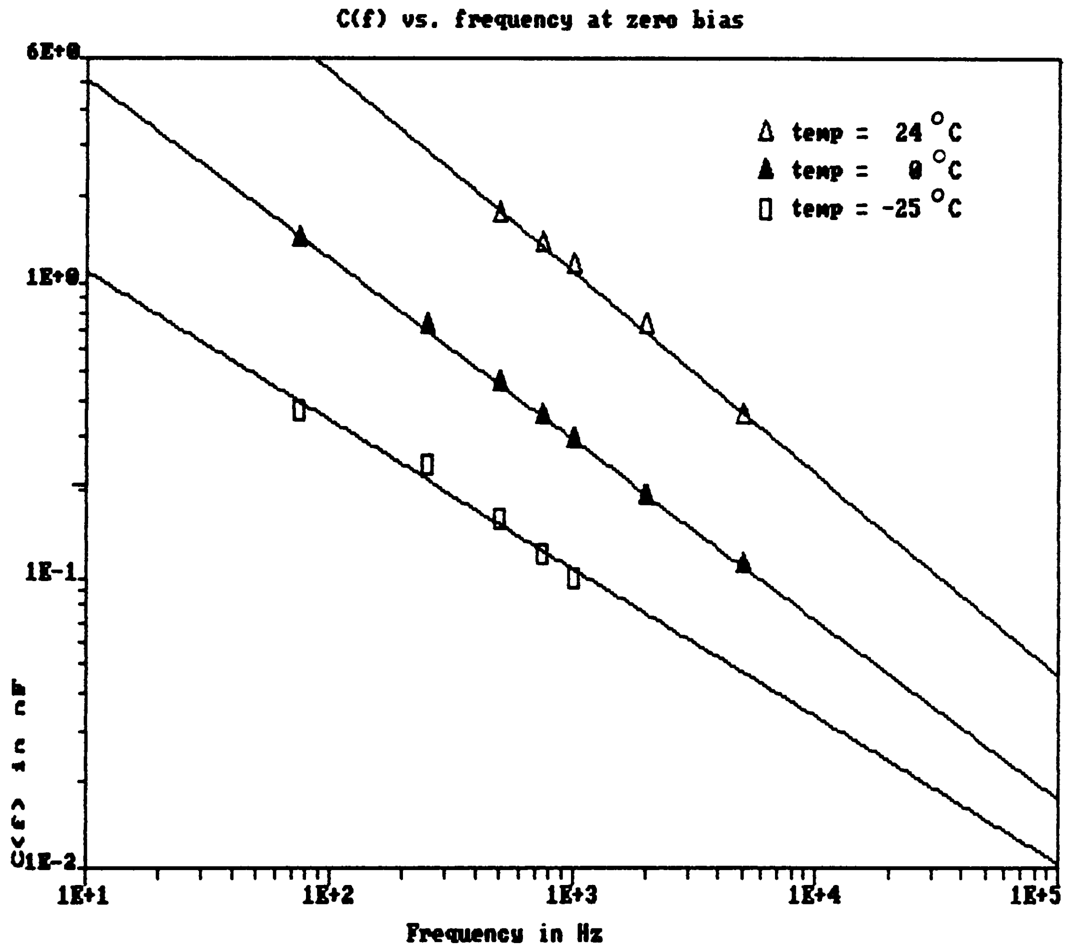


Figure 39. Frequency dependence of C_f of a 1keV diode at zero bias: (Morgan sample).

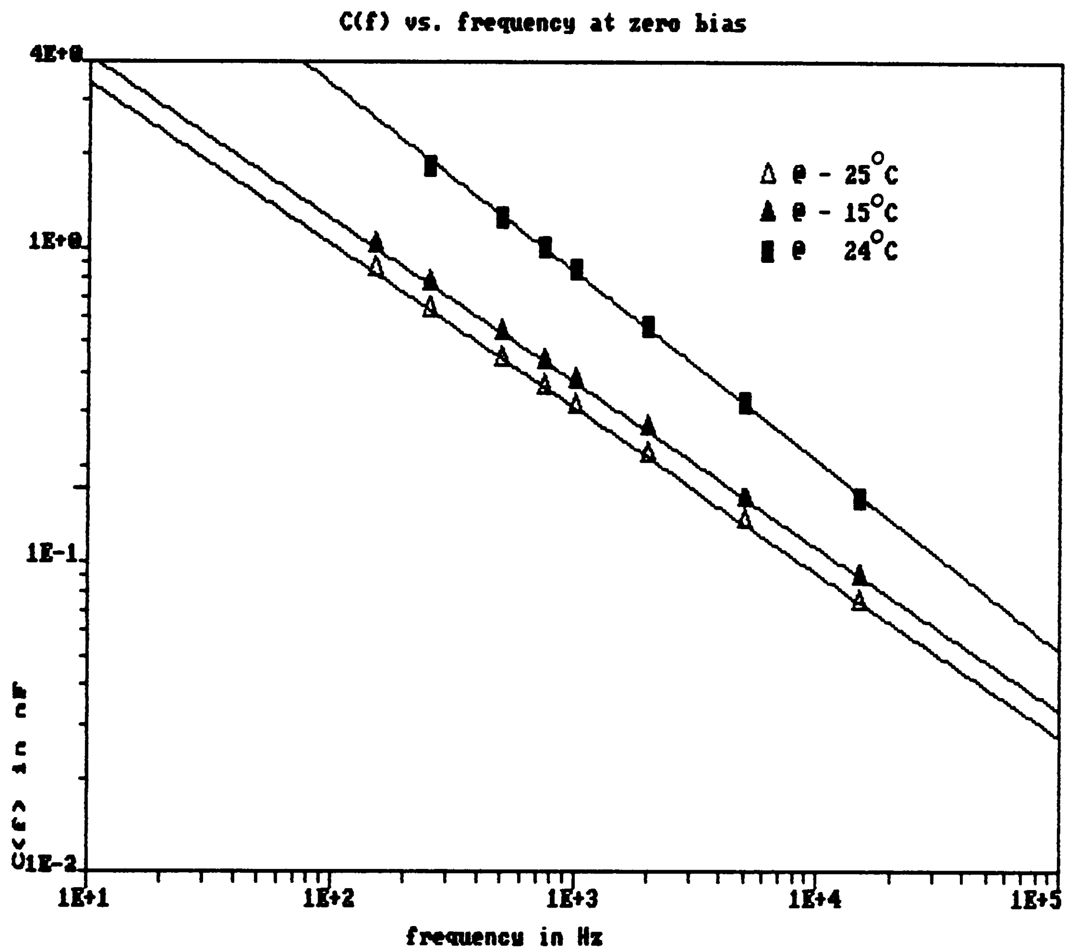


Figure 40. Frequency dependence of C_f of a 3keV diode at zero bias: (Morgan sample).

The trap depth (E_T) is found from the slope of the semilog plot of C_f *vs.* 1/T. Each linear portion of the semilog plot corresponds to traps with a fixed E_T or activation energy . The ion-induced traps are located below the conduction band edge at 0.5-0.6 eV for the 1keV and at 0.3-0.4 eV for the 3keV etched diodes. A shallow level of 0.15-0.17 eV was found in both 1keV and 3keV etched diodes. It is hard to rely too much on these trap depth values because of the aforementioned assumptions. There is no clear evidence as to why the amorphous damage layer should satisfy assumption b, above.

Earlier researches[25] have shown that the sputter induced defects are exponentially distributed from the surface and are of the form given by eqn. (3.1). It has also been mentioned that the frequency dispersion effect of the capacitance is weaker if the trap concentration (N_T) falls below the dopant concentration (N_d). Accordingly, the sudden disappearance of the low frequency capacitance "tail" at a mild reverse bias ($\sim$ 1 V) may possibly be explained by means of an unique trap distribution. It is proposed that the ion-damage defect states are distributed in such a way that the trap concentration N_T, abruptly goes below N_d at a reverse bias as low as 0.5 to 1 V. Such a type of trap distribution, though seeming very coincidental, appears to explain the observed effects of reverse bias on the capacitance "tail". The large electron concentration in the thin damaged layer clamps the depletion layer thickness, as long as frequency is low enough and temperature high enough so the traps can respond. Under reverse bias, the space charge region spreads rapidly into the less damaged, lower carrier concentration region, and capacitance decreases[52].

Another possible mechanism that can account for the high sensitivity of C-f measurements on reverse bias is related to the 'field effects'. Arsenic ions, even at room temperature, might diffuse to the arsenic depleted ion-etched surface and thereby cause a modification in the electric field behavior beneath the interface. Exact modification and the role of the electric field is not yet known. It is felt that such a modified field may potentially explain the anomalous effect of reverse bias on the C-f relationship of IBE diodes.

5.6 Conductance-frequency (G-f) Measurements

The G-f relationship of virgin and IBE diodes made from Morgan and Airtron wafers are shown in Figs. 41 and 42, respectively. It is clearly evident from both the figures that the zero bias conductance of the IBE diodes is higher than that of the virgin diodes. The difference is more striking at lower frequencies where the deep traps are likely to participate in current transport. Also noticeable is the higher conductance of the 1keV over the 3keV etched diodes. These results are consistent with those found in section 5.1. Higher diode conductance for the 1keV etched surface is attributable to a greater number of surface defect states that are likely to provide conduits to charge flow.

The temperature effect on G-f relationship of the virgin and the 3keV etched diodes is shown in Figs. 43 and 44, respectively. The virgin diodes exhibit near temperature independent conductance in the measured frequency range (100Hz-1MHz). On the contrary, the 3keV etched diodes, especially at low frequencies show a strongly temperature dependent conductance (G). At high frequencies ($\sim$ 1MHz), however, the temperature effect on G is similar to that observed on virgin diodes. This behavior of G on temperature is as expected. The increase in conductance of the IBE diodes at higher temperatures is because of the greater number of the ion-induced traps participating in electrical transport.

5.7 Complex impedance measurement

The real part ($R(\omega)$) and the imaginary part ($X(\omega)$) of the complex impedance ($Z(\omega)$) were measured at room temperature in the frequency range of 25Hz to 1MHz. The complex impedance plot of a virgin and an ion-etched diode made from a Morgan wafer are shown in Figs. 45 and 46, respectively. The virgin diode plot in Fig. 45 does not conform to a full semi-circle because of the measuring limitation of the impedance analyzer. The linear logarithmic

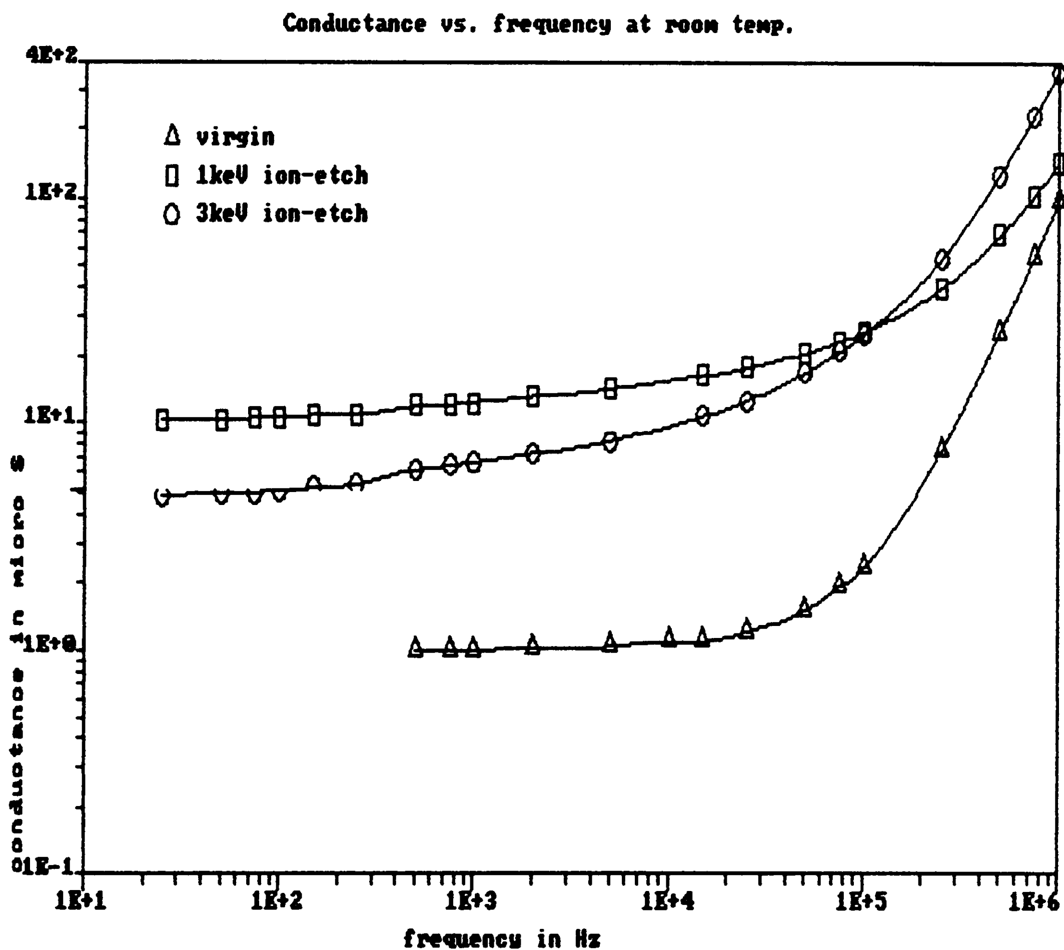


Figure 41. Frequency dependence of zero bias conductance: (1/32 in. Schottky dia, Morgan samples).

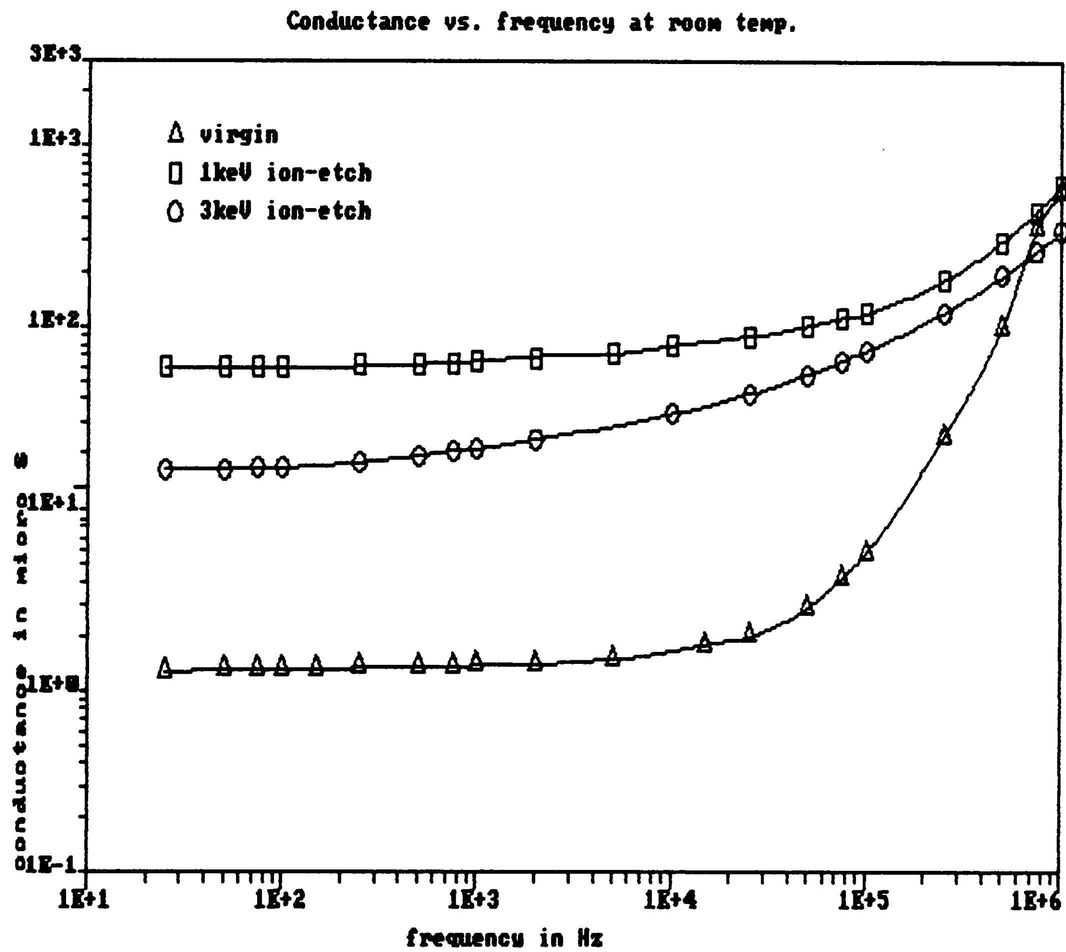


Figure 42. Frequency dependence of zero bias conductance: (1/16 in. Schottky dia, Airtron samples).

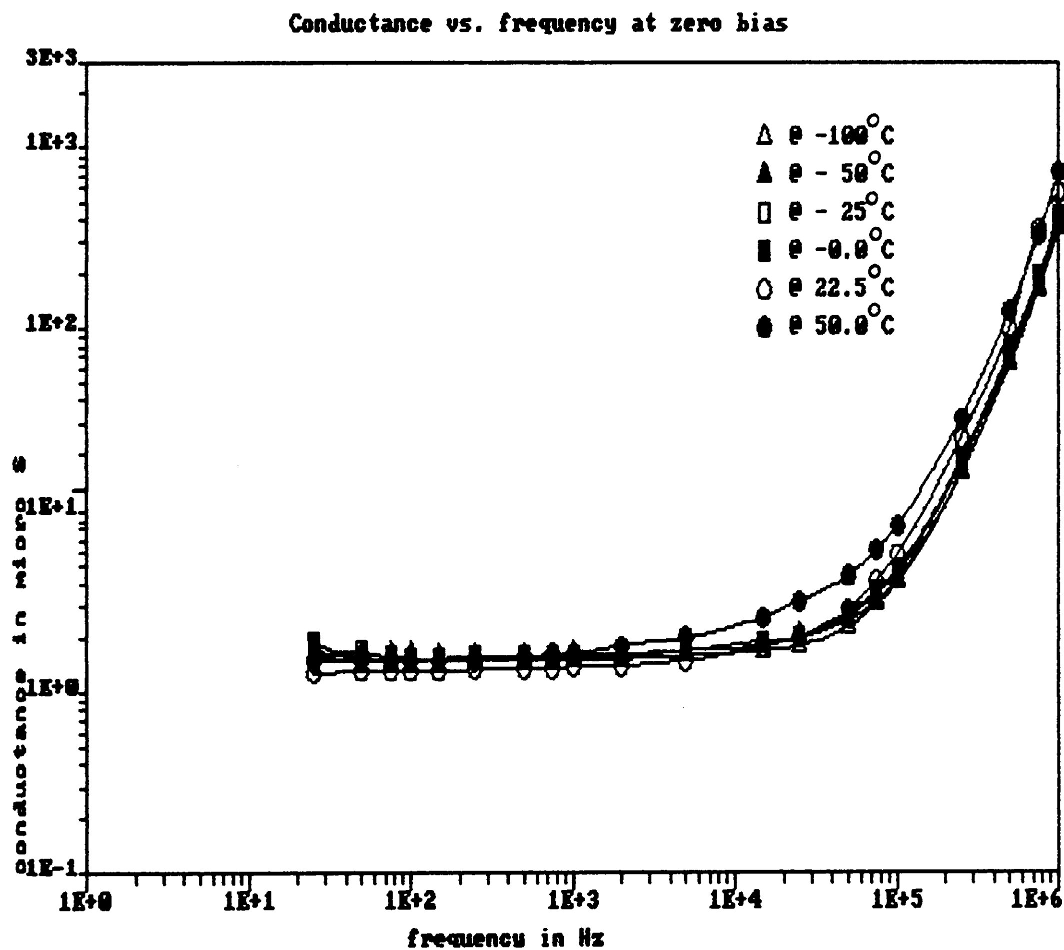


Figure 43. Effect of temperature on G-f relationship of a virgin diode.

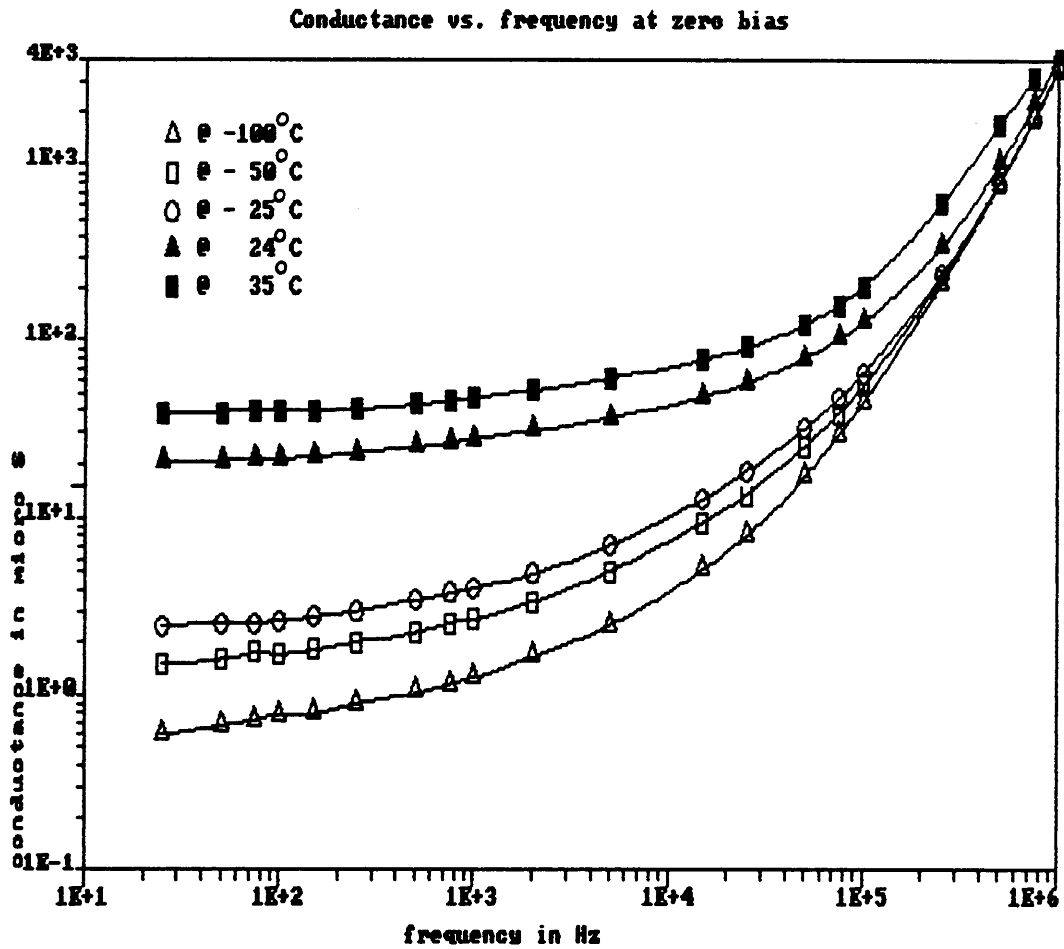


Figure 44. Effect of temperature on G-f relationship of a 3keV etched diode.

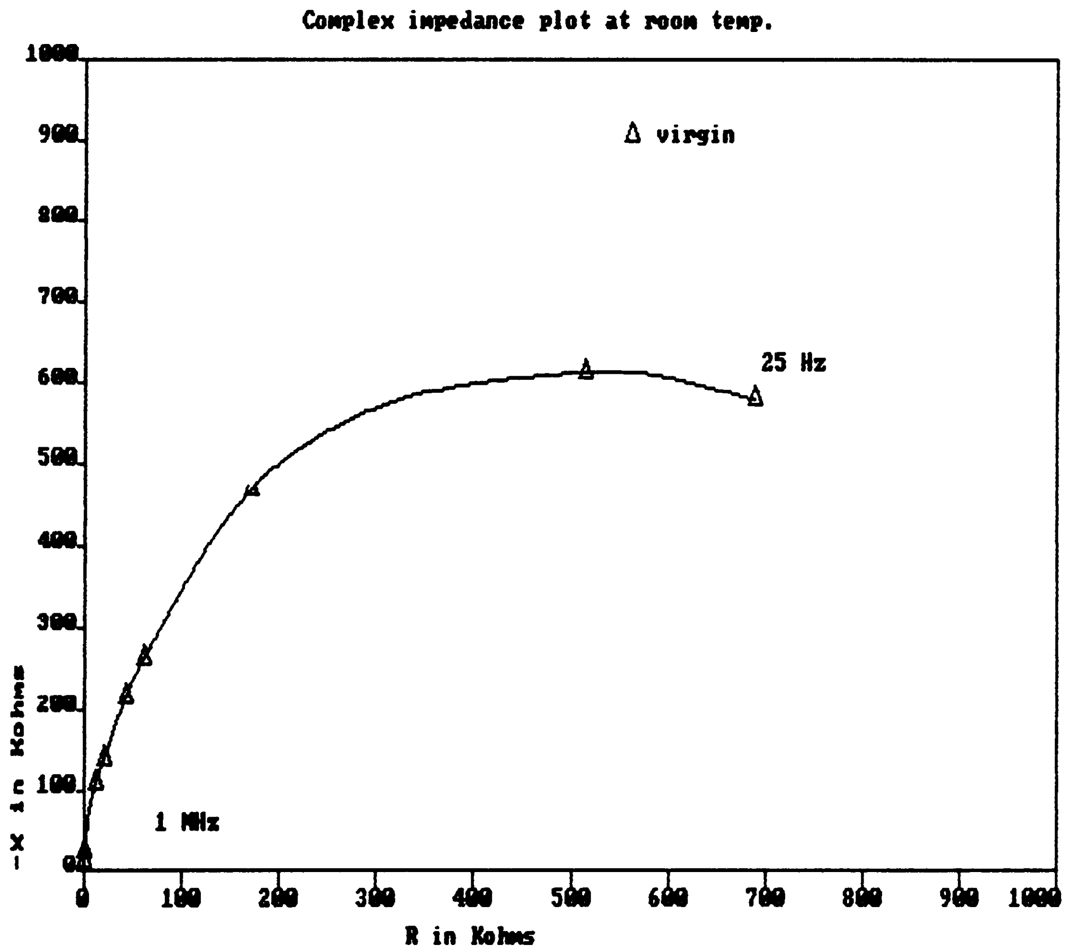


Figure 45. Complex impedance plot of a virgin diode: (Morgan sample).

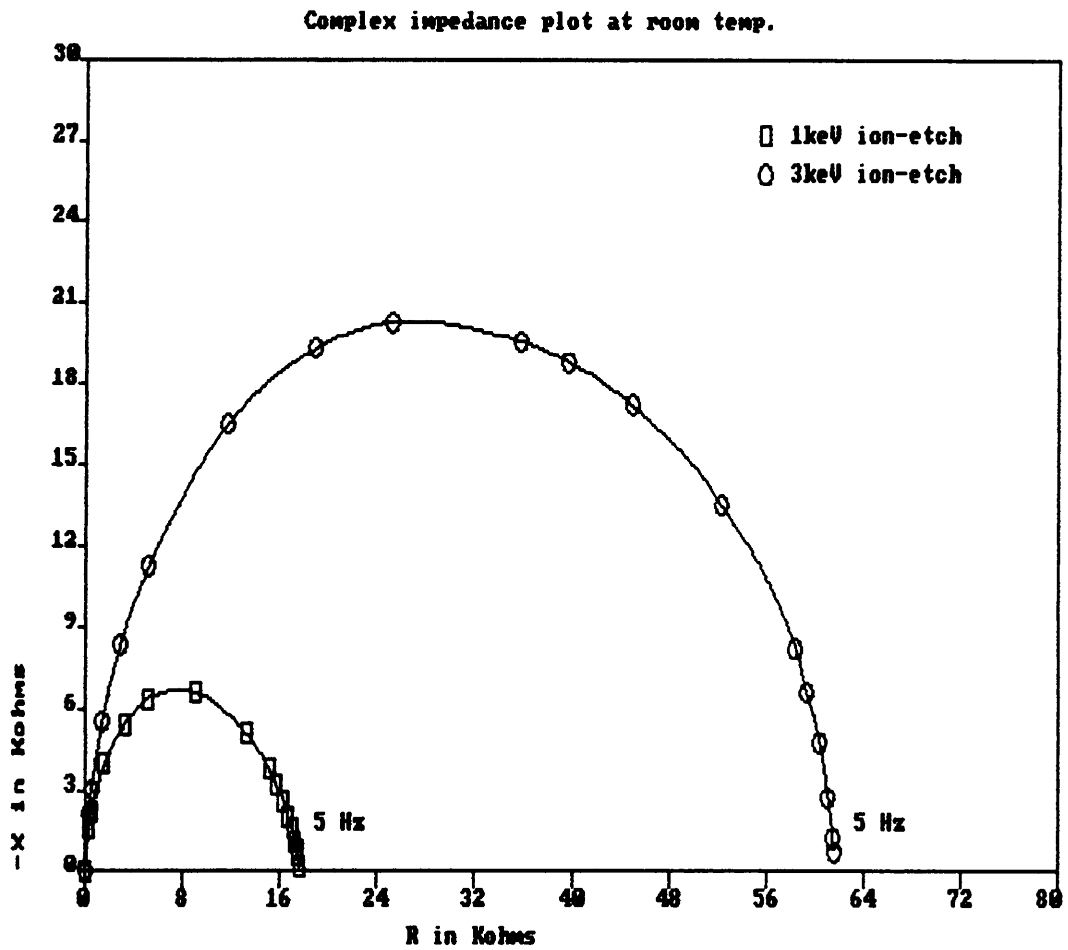


Figure 46. Complex impedance plot of ion etched diodes: (Morgan samples).

plot of $R(\omega)$ *vs.* $X(\omega)$ of a virgin diode had slope of 0.55 (the plot not shown). This slope is very close to the slope of 0.5, which would be obtained for a perfect semicircular impedance plot.

For the case of the IBE diodes the semicircle-like pattern traverses more completely. The plots, as shown in Fig. 46 for IBE diodes, are neither perfect semicircles nor are there any kind of distinct structure visible. There appear to be a strong overlapping of semicircles with each semicircle corresponding to a lumped parallel R-C combination. The details of a possible equivalent circuit model are discussed in section 5.10.

The overall diode resistance (found from the intercept on the real axis in Figs. 45 and 46) is lowered by ion etching. The resistances as obtained from the impedance plots are $\sim$ 17KΩ and 63KΩ for the 1keV and the 3keV etched diodes, respectively. These values are reasonably close to those obtained from the slope of I-V curve near zero bias (17.4KΩ for 1keV and 79.8KΩ for 3keV etched diodes). These results are in agreement with the findings of the I-V and G-f measurements discussed previously.

5.8 Chemical Etch Study

In an effort to study the effect of ion etching on surface leakage, a completed Au Schottky diode was subjected to 4keV Ar^+ bombardment. Au, in all likelihood, would protect the interface from being damaged by the incident ions. The ion-damage would then take place around the Schottky contact, while the junction, where all the electrical evaluations were done, would reamain intact.

The damage layer removal was done sequentially by treating the above diode in a $H_2SO_4 : H_2O_2 : H_2O$ (1:1:100 by vol.) solution for different lengths of time. The etch rate of the etchant is $\sim$ 600Å/min[51]. The I-V measurements were performed after each successive removal of the damaged layer.

The reverse I-V characteristics in Fig. 47 indicate that with progressive chemical etching, the leakage current reduces and the characteristics tend to approach those of the virgin diode.

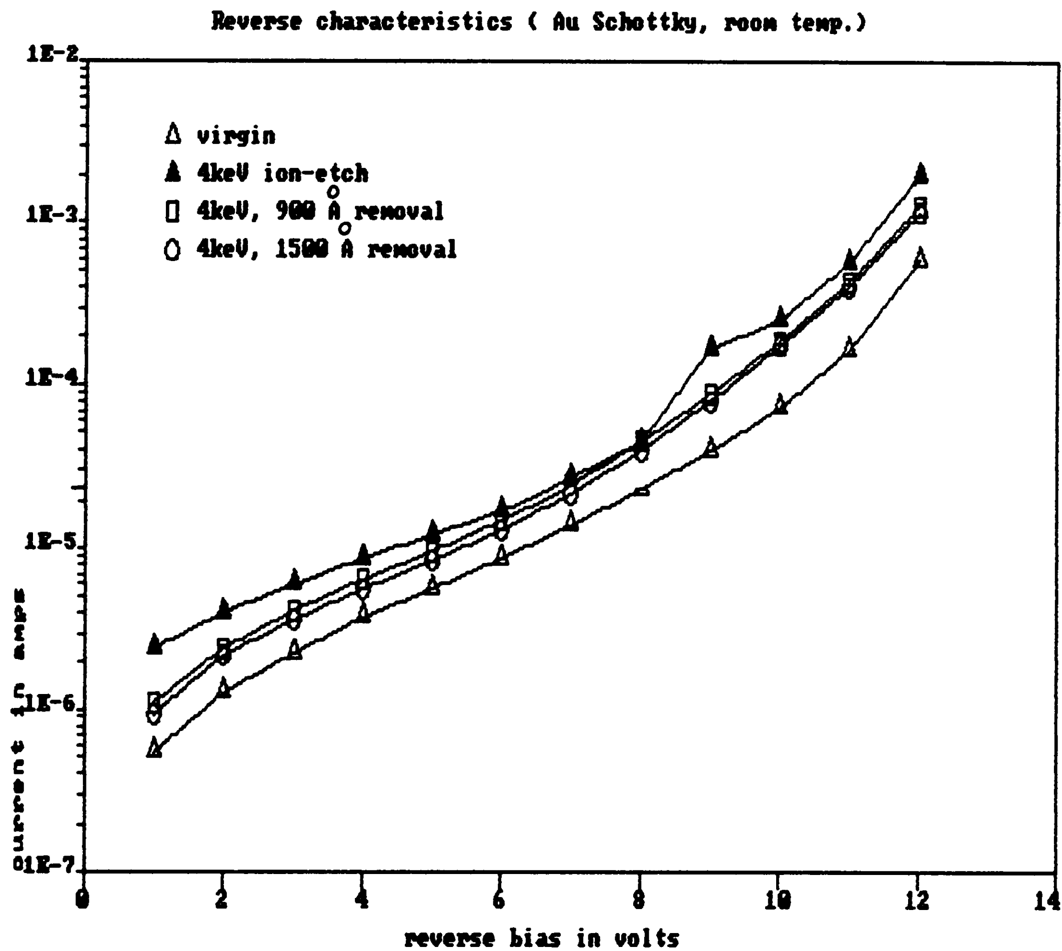


Figure 47. Comparision of reverse characteristics of an IBE and a subsequent chemically etched surface: (Morgan sample).

The results of this study reveal that the damage is at least ~ 1500Å deep for the 4keV bombarded surface. The important point to note; however, is that these reults are in agreement with the results of the area study [see section 5.2] and confirm the existence of a surface leakage path on the IBE diodes.

5.9 Structural Damage Model

The top amorphous layer (discussed earlier for IBE diodes) would probably be a random mixture of oxides, metal, and semiconductor atoms. The ion bombarded top surface of GaAs is expected to have a strong reactivity because of its amorphous nature. Accordingly, the presence of compounds such as AlAs, $Al_xGa_{1-x}As$ etc. at the ion-etched interface are quite likely. The propensity of oxide formation on an ion-etched surface is higher than that on a virgin surface(8) . This condition is more appropriate in the present study where the ion etching and the Schottky metallization processes were not done *in situ*.

In addition to the above, damage in the form of vacancies, interstitials etc. are capable of diffusing into the bulk even at room temperature. Such ion-induced defects give rise to a damage diffused layer(1) beneath the top amorphous layer. Taking all these into consideration, a possible Schottky barrier structural model of an ion-etched surface is shown in Fig. 48. The damage region may not be so distinctly separated as shown in the figure. It is very likely that the separate portions of the damage may in part superimpose on one another over a certain region.

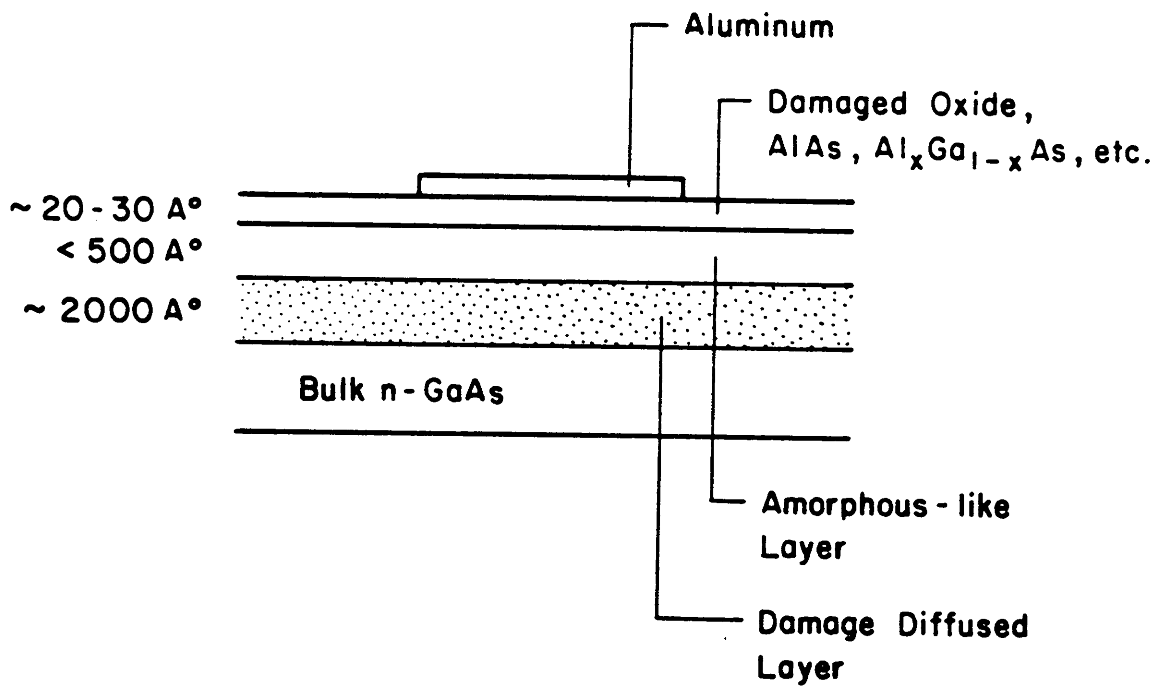


Figure 48. Structural model of an IBE diode.

5.10 Equivalent Circuit Model

Based on the results of electrical measurements and the above physical model, an attempt will be made in this section to model electrically the Schottky junctions of virgin and ion beam etched diodes.

5.10.1 Virgin diode

The dependence of the room temperature dielectric loss (C'') on measuring frequency (ω) of a virgin diode is shown in Fig. 49. C'' for this plot is evaluated by means of eqn. (2.16). The figure reveals the frequency dependence of C'' as $\omega^{-0.85}$. This is fairly close to the theoretical dependence of ω^{-1}. The admittance components G(ω) and C(ω) of the virgin diode, as seen from Figs. 32 and 43, respectively, are practically constant in the measured frequency range.

The frequency dependence of C(ω), G(ω), and $C''(\omega)$ and also the near semicircular nature of the complex impedance plot [see Fig. 45] prompts one to visualize a virgin diode to be comprised of a frequency independent junction or barrier capacitance (C_d) in parallel with a frequency independent conductance (G_d). The parallel $C_d - G_d$ combination is then in series with the bulk region of resistance R_s. The equivalent circuit model of a virgin diode is shown in Fig. 50(a).

5.10.2 Ion beam etched diode

Ion etching introduces additional resistor and capacitor elements on the virgin Schottky diode model. The surface leakage in IBE diodes would give rise to a conductance (G_L) in parallel with the barrier ($C_d - G_d$) and the bulk resistance (R_s).

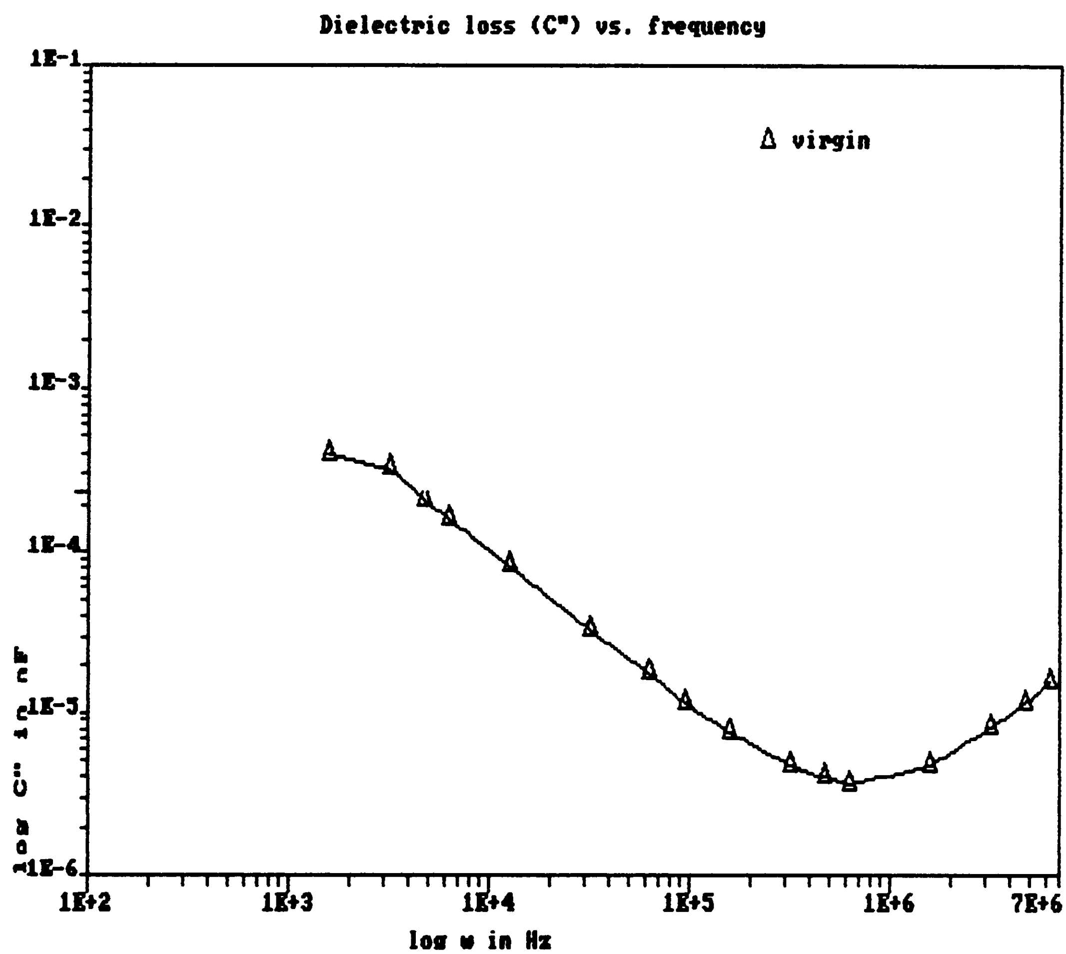
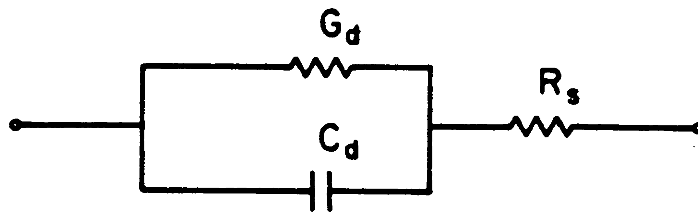


Figure 49. Effect of frequency on dielectric loss of a virgin diode.

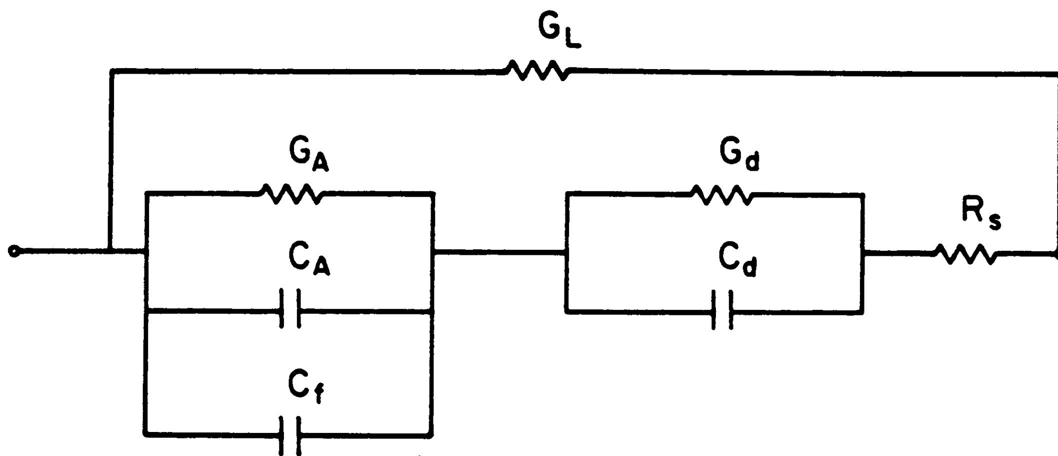
The decrease in high frequency capacitance of IBE diodes [section 5.3] was attributed to an amorphous layer capacitance (C_A) in series with the junction capacitance (C_d). The amorphous layer, by itself, can be treated as a parallel combination of frequency independent C_A and a frequency independent G_A (conductance). The possibility of different lumped parrallel R-C combinations was also discussed in section 5.7. The presence of G_A is because of the fact that the amorphous layer capacitor, like the virgin capacitor, would invariably have some associated dielectric loss (i,e. a non-ideal capacitor).

The C-f measurements in section 5.4 and subsequent trap analysis in section 5.5 have together explained the frequency dispersive capacitance behavior of the IBE diodes. A damage layer capacitance (C_f) due to the high density ion-induced traps was proposed to be in parrallel with the top amorphous layer capacitance (C_A). The capacitance C_f is strongly frequency dependent and adds up to the total capacitance only at low frequencies. The zero bias depletion width at low frequencies is essentally determined by the ion-induced traps in the top damage layer. The capacitance C_f is very bias sensitive and its effect is nearly non existent at reverse biases greater than 1 V. It has also been mentioned in section 5.4 that the traps contributing to the capacitance C_f are donor in nature.

On the basis of the above arguments, a possible equivalent circuit model of an IBE diode is shown in Fig. 50(b). The model may not be necessarily complete by itself. It is a model that is capable of accounting for most of the observed experimental results on the IBE diodes. The phenomenon of increase in breakdown voltage by ion etching is still not appropriately explained. More experimental details are therefore needed to comment on such behavior of the IBE diodes.



(a)



(b)

Figure 50. Equivalent circuit model: of a (a) virgin diode (b) IBE diode.

5.11 Annealing

In an effort to heal the ion-damage, IBE diodes were subjected to annealing at temperatures of 250, 350, and 450°C for 10 mins. each. Annealing effects under two conditions - before and after Schottky metallization - were considered.

The effects of post Schottky metallization anneal is shown in Fig. 51. The diodes continue to have a poor ideality factor and higher reverse saturation current even after all types of annealing treatment under consideration. In the case of annealing, after Schottky metallization, it is extremely difficult to exclusively discern the effect of anneal because of a possible masking effect by the inter-diffusion between Al and GaAs at anneal temperatures. The end result being the inability of this type of anneal to reduce ion-induced defects and/or damage.

The effects of anneal, prior to Schottky metal depositon, on I-V characteristics of a 3keV etched diode are shown in Figs. 52 and 53. The reverse saturation current increases and the turn-on voltage decreases with increase in annealing temperature. The leakage current in reverse characteristic is quite prominent and it becomes severe at higher annealing temperatures. The diode parameters after different isochronal annealing treatments are shown in Table 6.

The above results indicate that annealing prior to Schottky metallization does not distinctly improve the diode characteristics. At annealing temperature of around 450°C, the device performance is severely degraded and the diode characteristic is somewhat quasi-omhic. The annealing done at 350°C appear to cause improvement in n and I_0 parameters [see Table 6]. The annealed diode parameters are, however, still far deteriorated from those of the virgin diodes. These results indicate that ion-damage is present even after the 350°C (10 mins.) annealing treatment. The results of C-f measurements on annealed diodes are shown in Fig. 54. The presence of a low frequency capacitance "tail" is clearly evident in the annealed samples. The "tail" size is , however, considerably reduced after 350°C anneal. The result

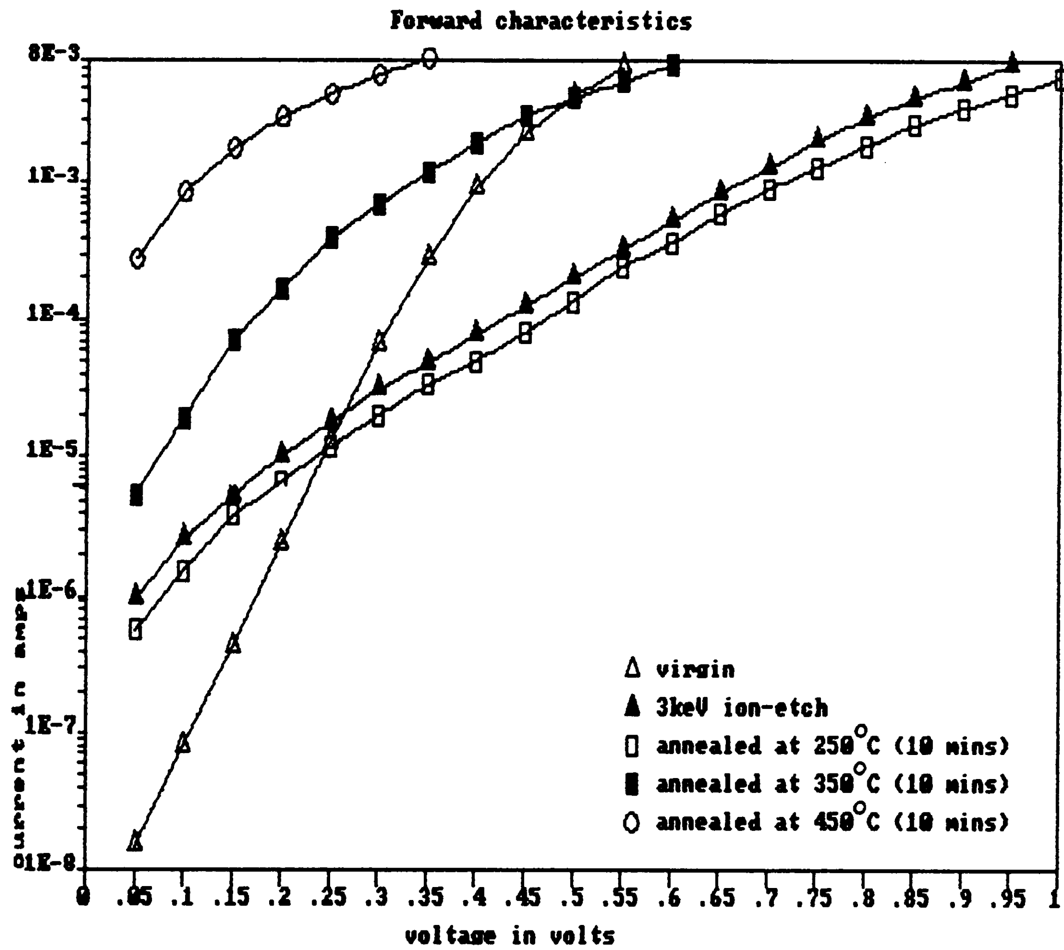


Figure 51. Effect of post Schottky metallization anneal on diode forward characteristics: (Airtron sample).

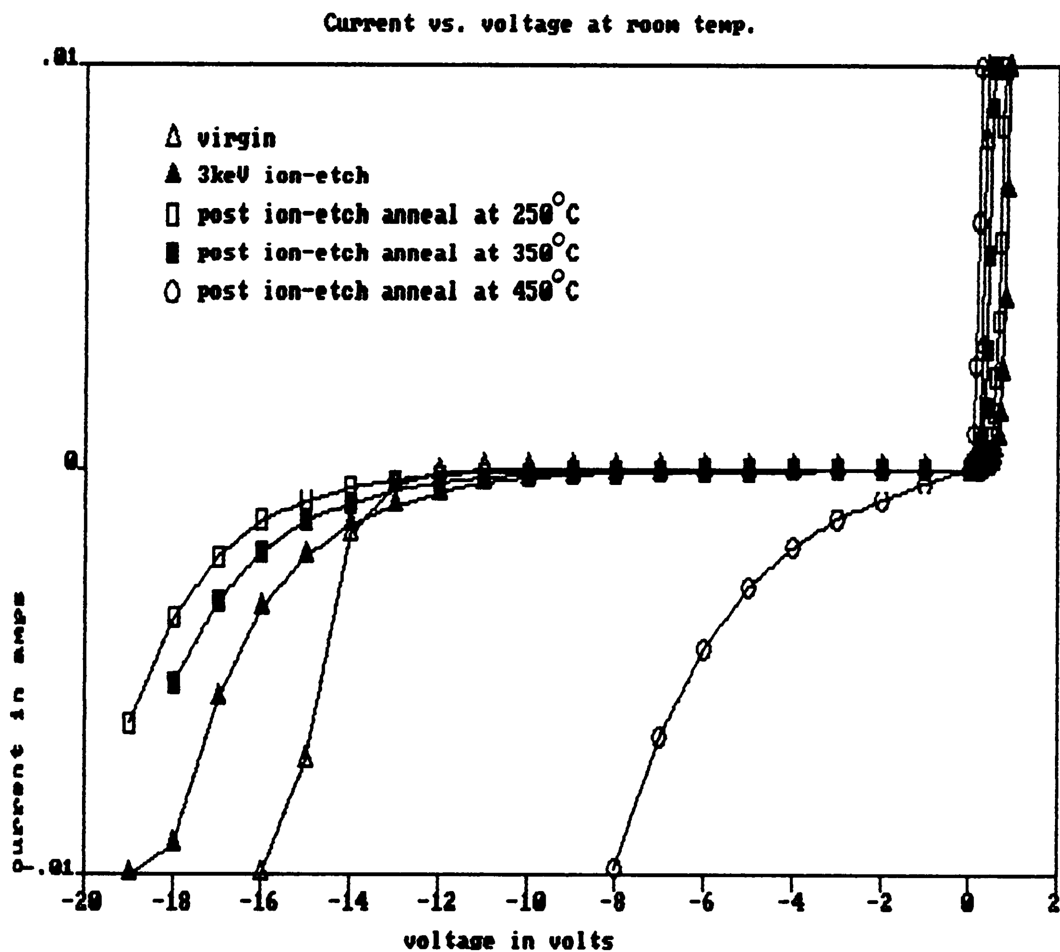


Figure 52. Effect of pre-metallization annealing on I-V relationship of 3keV etched diodes: (Morgan samples).

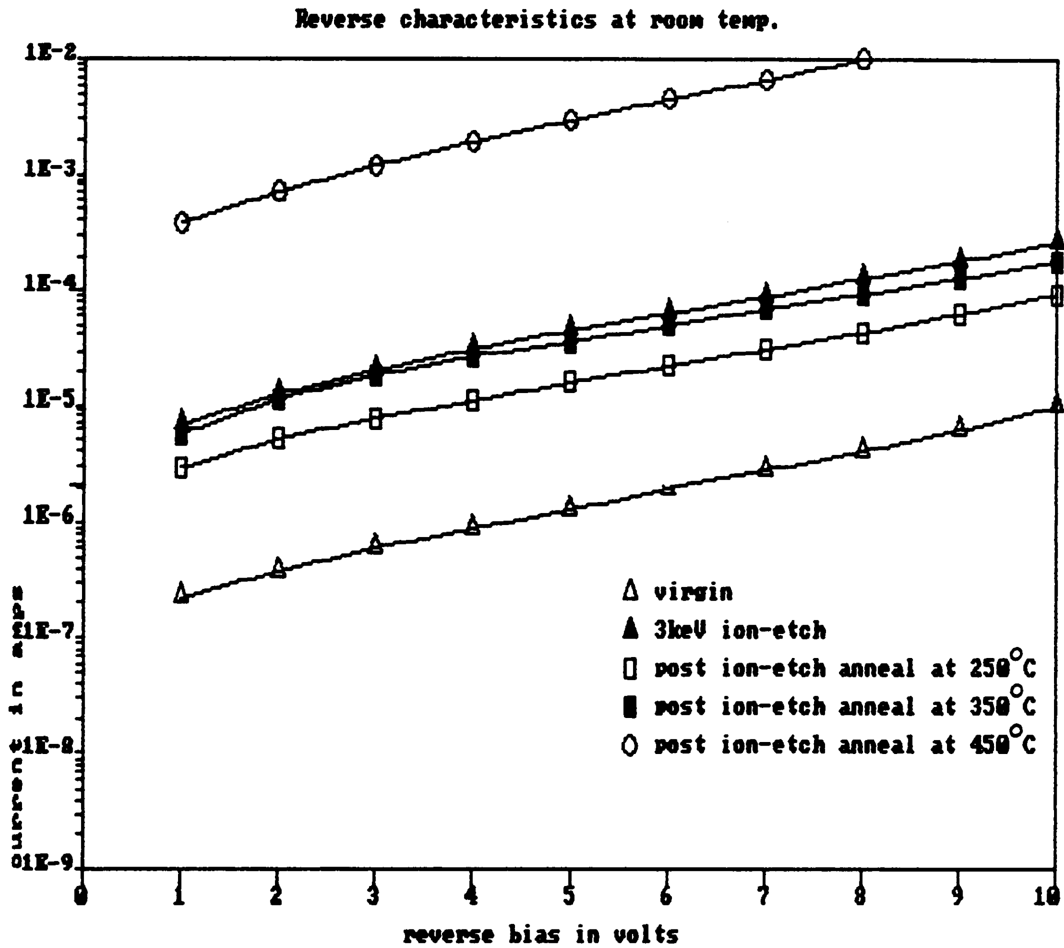


Figure 53. Effect of pre-metallization annealing on reverse characteristics of 3keV etched diodes: (Morgan samples).

Table 6. Effect of annealing on a 3keV etched diode parameters.

parameters / condition	n	I_0 (amps)
virgin	1.14	1.61×10^{-7}
3keV	3.28	9.8×10^{-7}
3keV + 250°C anneal	2.31	6.6×10^{-7}
3keV + 350°C anneal	1.79	1.34×10^{-6}
3keV + 450°C anneal	3.09	3.5×10^{-4}

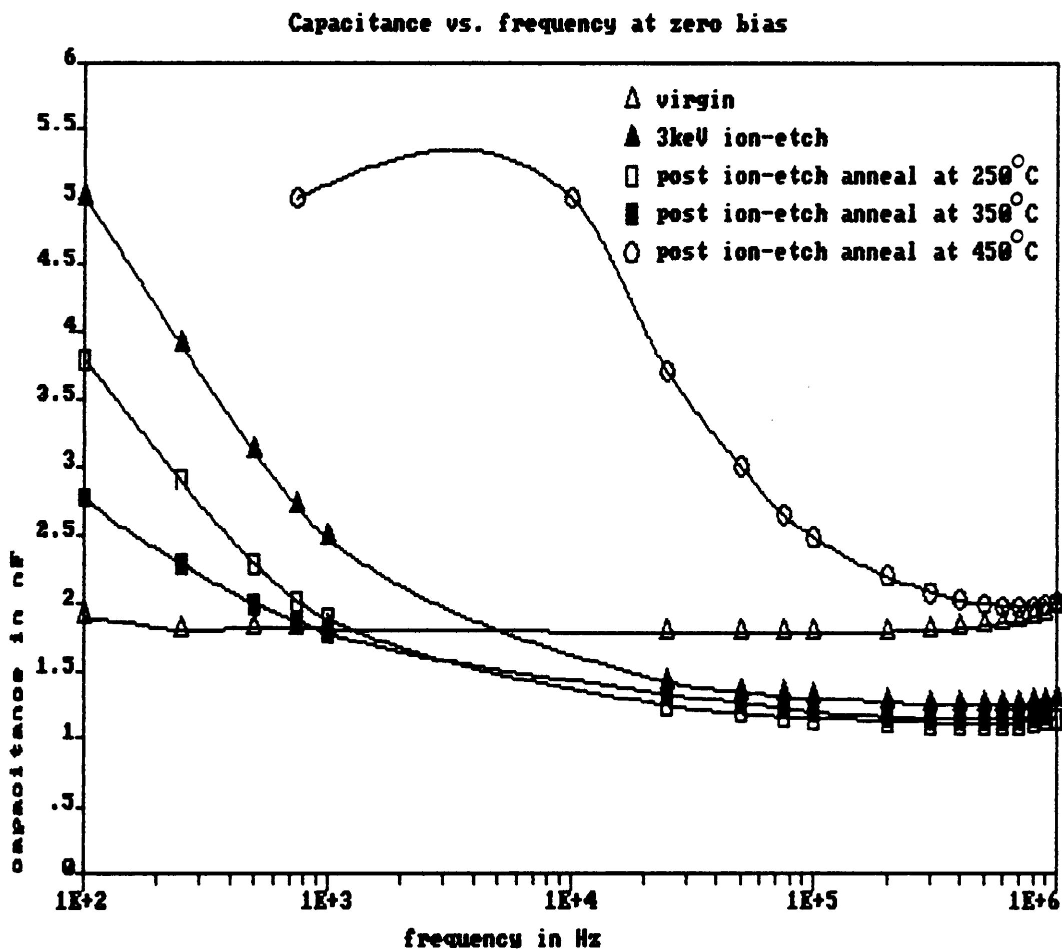


Figure 54. Effect of pre Schottky metallization anneal on C-f behavior of a 3keV etched diode: (Morgan sample).

suggest a possible anneal-induced recovery of the ion-damaged surface. The annealing time (10 mins.) was probably not enough to anneal out the ion-damage completely. The capacitance "tail" appears at a higher frequency for the 450°C annealed diode. The presence of "tail" indicates that the ion-induced surface defects continue to exist on an annealed surface and thus the diode characteristics still remain degraded.

It appears from the above results that annealing in the chosen time-temperature cycle is not effective in restoring the ion-induced disturbed surface stoichiometry. Annealing at 350°C, for a longer duration (> 10 mins.) might be effective in healing the ion-damage. Annealing, by itself, is believed to introduce additional defects in the form of As vacancies(7) at elevated temperature (≥ 450°C). The presence of such anneal induced defects in the damage layer, if any, would furthur complicate and worsen the ion-damage.

Chapter VI: Conclusions

Several questions related to the objectives of the research were addressed. The effects of ion-etch damage on the electrical behaviour of Schottky diodes were analyzed. The key results of the electrical studies on the virgin and the ion-etched n-GaAs Schottky diodes are summarized below:

1. The ion-etched diodes, as opposed to the virgin diodes, have severely degraded diode parameters. The diodes become "leaky" after ion etching.

2. The current transport in ion-etched diodes, unlike virgin diodes, is far from being governed by the thermionic emission process. The forward I-V characteristics of the ion-etched diodes reveal the possibility of the existence of multiple barriers at the Al-GaAs interface. Alternately, the barrier height of an ion-etched diode is not clearly defined.

3. Ion etching creates a low resistance surface layer that shunts the depletion layer. This is due to the ion-induced traps that provide effective surface leakage paths for current transport. The surface layer resistance of the 1keV etched diodes is less than that of the 3keV etched diodes.

4. The high frequency (1MHz) capacitance of ion-etched diodes is lower than that of the virgin diodes. The lowering of capacitance increases with increase in etch energy. This is due to the creation of a thicker amorphous layer on the surface at higher ion energies.

5. Ion etching creates a damage layer (thicker than the amorphous layer) that contains donor-like traps. The density of traps near the surface is higher for the 1keV etched than for the 3keV etched diodes. The traps in the damage layer cause the capacitance of the ion-etched diodes to be frequency dispersive. The virgin diode capacitance, on the contrary, is frequency independent.

6. Trap ionization is temperature dependent, and the resulting capacitance is very sensitive to reverse bias. The effective density of active traps decreases at low temperature, and at high value of reverse bias. The traps are distributed geometrically in such a way that a reverse bias of 0.5 to 1 V can make the trap density at the depletion layer edge lower than that of the dopant density. Under this condition, the frequency dispersion effect of the IBE diode capacitance is almost negligible.

7. A possible equivalent circuit model of an ion-etched diode consists of two lumped R-C elements in series, which are in parallel to a resistor that represents surface leakage. The equivalent circuit models of virgin and ion-etched diodes were shown in Fig. 52.

8. Low temperature annealing ($\leq$ 450°C) for a duration of 10 minutes under forming gas is not effective in healing the 3keV ion-damage. A longer annealing ($\geq$ 10 mins.) at $\sim$ 350°C is likely to heal the ion-damage to a considerable extent.

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