

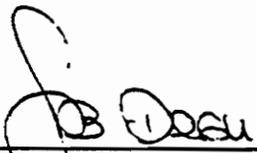
**ELECTRICAL CHARACTERIZATION OF FERROELECTRIC
CAPACITORS FOR NON-VOLATILE MEMORY APPLICATIONS**

by

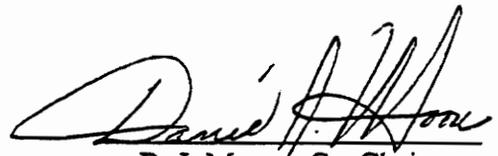
Chai-Liang Thio

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MASTER OF SCIENCE
in
Electrical Engineering

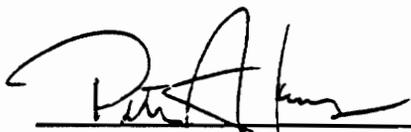
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ELECTRICAL CHARACTERIZATION OF FERROELECTRIC CAPACITORS FOR NON-VOLATILE MEMORY APPLICATIONS

by

Chai-Liang Thio

Committee Co-Chairmen: Seshu B. Desu and Daniel J. Moore

Department of Electrical Engineering

(ABSTRACT)

Ferroelectric materials show a spontaneous electrical polarization that can be reversed in sense by an applied external electric field. It should, therefore, be feasible to build a ferroelectric memory device that can store information in digital form.

Ascertaining the suitability of a ferroelectric material for use in memory devices requires an understanding of electrical properties of the thin-film capacitor. There are a number of electrical characterization methods which can be used to investigate these electrical properties. The polarization mechanism can be studied by the most fundamental characterization technique for ferroelectrics, the hysteresis loop, which is derived by plotting polarization against applied field. Fatigue, retention and imprint, which are specific ferroelectric lifetime characterization methods, are employed to determine the rate of capacitor degradation as well as the mechanisms responsible for it. The DC conductivity characterization techniques, including leakage current, resistivity degradation and time dependent dielectric breakdown (TDDB) are used to study the electrical current properties and charge transport mechanism in memory applications. Finally, the AC conductivity (complex impedance) characterization method, introduced here for the first

time for ferroelectric capacitors, permits further understanding of the charge transport mechanism of ferroelectric materials. However, this characterization method is not directly used to evaluate the application of ferroelectrics in memory devices, but it can provide a further physical understanding of ferroelectric capacitors, such as the understanding of fatigue.

$\text{PbZr}_x\text{Ti}_{1-x}\text{O}_3$ (PZT), a ferroelectric material with a pseudo-cubic perovskite-type structure, has been the material of choice in all major ferroelectric random access memory (FRAM) development programs to date. However, degradation problems such as fatigue and imprint that affect the lifetime of ferroelectric capacitors have moderated the progress of using PZT in commercial ferroelectric memories. Recently, $\text{SrBi}_2\text{Ta}_2\text{O}_9$ (SBT), a ferroelectric material that crystallizes in a layered structure, has been identified as a promising candidate for FRAM applications as a result of its fatigue-free behavior. In this research, the performance of PZT and SBT as ferroelectric memory materials is compared by using the aforementioned electrical characterization methods.

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Without the love and support from my lovely wife, Claire, I could not continue and have finished my education in Virginia Tech. Not only does she provide me warmth in my family life, but also help me in the research by encouraging in deep discussion and preparing the samples used in this work. Thank you, Claire. But I know I am not able to express my appreciation to her completely in words.

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Chapter 1

Introduction

In the race to produce memory chips with higher and higher densities, manufacturers abandoned the idea of flat integrated circuits several years ago. Modern memory chips are distinctly three-dimensional, with deep trenches and stacked layers that are used simply to increase the surface area. The capacitance of a flat layer is proportional to the product of its area and its dielectric constant (ϵ_r):

$$C = \epsilon_r \epsilon_0 \text{ Area/Thickness.}$$

If a way could be found to increase the dielectric constant of the material by a factor of 50, the size of the capacitor could be reduced correspondingly, and trenching and stacking could perhaps be eliminated altogether. This would make memories quicker and potentially cheaper to produce, as designs would be simpler and would need fewer production stages.

Until recently the capacitor material in dynamic random access memories (DRAMs) was generally silicon dioxide, which has a small dielectric constant. As a matter of fact, the need for further reduction in capacitor area in the state-of-the-art 1 Gbit DRAMs requires materials with much greater dielectric constants. This need has focused attention on ferroelectrics - a class of crystalline materials whose low symmetry permits them to have a net electric dipole in a certain direction, which can be reversed by an applied voltage.

Ferroelectrics have a couple of properties that make them attractive in memory devices. First, they possess a specific characteristic, called spontaneous polarization. Spontaneous polarization means that electrical dipoles in the material align themselves along electrical field lines when an electric field is applied to a specimen and remain in the

aligned position even if the field is subsequently removed, i.e. it provides non-volatile operation. Applying the opposite polarity cause the dipoles to switch and align in the opposite direction. Because ferroelectric materials exhibit two stable states that can be switched "up" or "down" as the storage of "1" or "0" - that is, they can be used as the memory element itself. Second, ferroelectrics have very large dielectric constants, a hundred times or so greater than that of silicon dioxide. These two outstanding qualities are not closely related, and most devices are based on just one of these properties [1-2].

In order to meet the requirements for these memory applications, the ferroelectric capacitors should have small size, low coercive field, high remanent polarization, low fatigue rate, good retention, less imprint and low leakage current. The most studied ferroelectric materials for these memory applications at present are lead zirconate titanates, $\text{PbZr}_x\text{Ti}_{1-x}\text{O}_3$ (PZT). This is due to the fact that such PZT films have promising electrical properties such as large remanent polarization and low switching fields. Furthermore, it has been shown that its processing can be done in combination with standard integrated circuit processing [3-4]. However, this perovskite ferroelectric, in general, is known to suffer from serious degradation problems such as fatigue, imprint and leakage current that affect the lifetime of the devices [5-6]. Recently, it has been found that ferroelectric bismuth-layered structure oxides such as $\text{SrBi}_2(\text{Ta}_x\text{Nb}_{2-x})\text{O}_9$ (SBTN) films are good candidates for fatigue-free ferroelectric random access memory (FRAM) applications on Pt electrodes [7]. In this study, several electrical characterization methods will be used to study the feasibility and compare the performance of PZT and $\text{SrBi}_2\text{Ta}_2\text{O}_9$ (SBT) as the materials for FRAM applications.

Accompanying the investigation of PZT and SBT as candidate FRAM materials, the characterization concepts, methods and possible mechanisms for several electrical properties of materials suitable for FRAM applications will be introduced in this study.

The most basic characterization is the hysteresis loop. Study of the hysteresis behavior is very important because it provides critical information regarding the ferroelectric such as saturation field, switchable polarization, spontaneous polarization, and remanent polarization. Furthermore, since the hysteresis properties change when ferroelectrics are degraded, this might also suggest that comprehensive understanding of the hysteresis properties is required to improve the reliability of ferroelectric capacitors. In this study, we will review two methods of characterizing the hysteresis properties. Basically, the measurements are based on the Sawyer-Tower circuit [8].

Fatigue, retention and imprint will be introduced to characterize the lifetime of ferroelectrics. By employing these characterization techniques, the degradation mechanisms of ferroelectrics can be understood. Fatigue is the decrease of switchable polarization of a ferroelectric capacitor to a value that is too low to distinguish between the polarization states (digital value of "1" or "0"). Space charge development at the interface between the electrodes and ferroelectric thin films will be used to explain the fatigue mechanism. Retention measurements characterize the polarization loss with time after writing a pulse into the ferroelectric capacitor, while imprint characterizes the retention loss rate difference between state "1" and "0" of a ferroelectric capacitor. Compared with the fatigue studies, there are not so much of studies of retention and imprint. As a matter of fact, imprint has just recently defined as a tendency of the poled ferroelectric capacitor to have a preferred polarization state after applying external stress, leading to misreading of the stored data. Since the imprint effect is contained in the conventional retention measurement, in this study a new characterization technique is introduced to draw out and provide quantitatively the imprint effect distinct from the retention measurement.

DC conductivity not only can provide the leakage current, resistivity degradation and TDDB (time dependence dielectric breakdown) data, which is very important for DRAM operation, but also could provide the conductivity behavior which could explain and clarify the ferroelectric capacitor behavior, particularly at the interface between film and electrode. I will introduce the programmable leakage current measurement and how to derive the required data from the measurement. In this part, I have successfully applied statistical method in a C-language program to manipulate the data and pick up the true leakage current of the ferroelectric capacitor.

For another conductivity study, the ac conductivity, we use complex impedance (Impedance Spectroscopy) analysis to define the ionic conductivity of the materials. Since Impedance Spectroscopy is introduced for the first time for ferroelectric capacitors and is not directly used to evaluate the application of ferroelectrics in memory devices, a separate chapter is devoted to this characterization technique. Using the fatigue model we suggest, the ionic conductivity could elucidate the fatigue behavior by comparing the fatigue-prone perovskite structure and the fatigue-free bismuth layered structure ferroelectric materials.

Chapter 2

Background

It was widely recognized that the existence of robust, chemically stable, and relatively inert ferroelectric crystals offered an electrically switchable, two-state device. With such a device one could encode the 1 and 0 states required for the Boolean algebra of binary computer memories. Their high speed, nonvolatility, and light weight, combined with low power requirements, physical robustness, and progressively improved memory density, suggested that they would rapidly replace core memories as the nonvolatile memory of choice for most applications. Nonvolatile memory is an essential requirement for all computer systems. It is especially important for military systems where vital information has to be stored in some type of a nonvolatile memory -- memory that does not forget when power is lost in a hostile environment. This chapter will review the history of ferroelectric memory devices, as well as ferroelectricity, the applications of ferroelectric memory devices, and the materials and processes involved in their fabrication.

2.1. Memory devices

The digital memories range from the slow, inexpensive devices (tape or disk) used for archival storage to the fast but expensive SRAM and the slightly slower DRAMs, whose availability in high-density chips has permitted them to become dominant in the computer memory market. The more expensive devices (plated wire, CMOS with battery backup, magnetic bubble memory, EEPROMs, and core) generally have some combination of attributes required for specific applications, particularly including nonvolatility and

radiation hardness. The projected memory market will be greatly simplified in a few years, however, if ferroelectric RAMs (FRAMs) become commercially available in high-density devices with satisfactory operating characteristics and lifetimes. The intrinsic nonvolatility and radiation hardness of FRAMs may greatly simplify the existing collection of computer memories, which will still include tape and disk systems for archival storage, as well as inexpensive high-density DRAMs and ultrafast SRAMs; however, most of the other memory devices now in use may be rendered obsolete.

The major advantage of ferroelectric devices in the memory world is their nonvolatility. Nonvolatile literally means that the stored information cannot "evaporate" -- if the power to a DRAM is interrupted, it "forgets" the information stored in it; a nonvolatile memory, such as magnetic core, retains information if the power is cut off. The initial idea using ferroelectric nonvolatility was to use a ferroelectric thin film, which can be permanently polarized by an electric voltage pulse, as the gate dielectric of a transistor. However, read errors might occur in such a memory cell due to the absence of a well defined threshold voltage for polarization. In 1987, a new concept of ferroelectric memory was introduced. The key idea was to use a ferroelectric thin film as the dielectric in the capacitor of a DRAM cell. Due to the fact that such a cell is refreshed every time it is read, READ disturbances could be avoided. If extreme endurance (10^{16} write/read cycles) and good data retention could be achieved, this could be the ideal memory. FRAM can potentially match DRAM in WRITE and READ speed and beat DRAM in cell size, with nonvolatility offered as a bonus.

Key characteristics of some of the current and future nonvolatile memory technologies are listed in Table I. The principal characteristics compared are density, speed, write time and endurance. The low density versions of FRAMs can compete with both EEPROMs and battery-backed SRAMs. When compared to EEPROM, FRAM has a

Table 1. Key characteristics of candidate nonvolatility memory technologies. Adapted from a table of Bob Peters published in *Defense Electronics*, October 1991, p.82.

FEATURE	EPROM	NAND EEPROM	Full-Featured EEPROM	Flash EEPROM	Stepped-Gate Flash	MNOS (SNOS)	Ferroelectric	Battery-Backed DRAM	Battery-Backed SRAM
Density	4Mbytes	4Mbytes	1Mbyte	1Mbyte	1Mbyte	64K	16K	16 Mbytes (Pro)	256K
Die Size (mm ²)	83.4	163	91.5	38	51	25	25	N/A	N/A
Cell Size (μm ²)	11.9	12.9	30.4	15.2	24.6	120	270	3.4	N/A
Elements/Cell	1	1.25	2	1	1.5	2	2	2	6
Lithography (μm)	1	0.5	1	1	1	2	1.5	0.5	1.2
Typ. Access Time (nsec)	90	1600	110	90	150	200	100	1000	45
Current Consumption									
Operating (mA)	20	20	66	8	N/A	30	5	5	120
Standby (μA)	10	10	100	4	N/A	10	10	.5	1
Write/Erase Voltage	12.5/-	22/17	16/16	12/12	21/21	15/15	5/5	1.5/1.5	5(3 hold)
Charge Pump	No	Yes	Yes	No	No	Yes	Not Nec.	Not Nec.	Not Nec.
Write Speed (μsec/byte)	.5	4000	2000	10	.5	5000	.2	1	.045
Erase Speed (sec)	1200/mem	.01/4 Kbyte	.002/bit	.9/mem	5/mem	.005/mem	1e-7/bit	1e-6/bit	45e-9bit
Max Write/Erase Cycles	1e2 to 1e3	1e4 to 1e5	1e4 to 1e5	1e5	1e2 to 1e3	1e5	1e10	Infinity	Infinity
Min Erase Block Size	All bits	4 Kbytes	1 bit	All bits	128 bytes	32 bytes	1 bit	1 bit	1 bit
Radiation Tolerance (Rads)	1e5	1e5	1e5	N/A	N/A	1e6	1e7 to 1e8	0	Low
Retention (Years)	>10	>10	>10	>10	>10	>10	>10	5@2AH Battery	4@35mAH Battery
Manufacturer	Intel	Toshiba	Mitsubishi	Intel	Seeq	Hitachi	Ramtron	Hitachi	Dallas Semi

much faster write cycle time (200 ns/byte) and longer write endurance (10^{10} maximum write/erase cycles versus $10^4\sim 10^5$). The erase, write and access times are essentially equal. This is important for those applications that are not read-mostly, like SRAM applications. EEPROM is a good read-mostly memory, but it cannot perform well as a read/write memory. Compared to SRAMs, FRAMs have similar read/write cycle times, but FRAMs are nonvolatile without a battery. A very high density FRAM processed with cell size similar to DRAM is going to be developed soon. (Note that a 256 Kbit $\text{SrBi}_2\text{Ta}_2\text{O}_9$ FRAM has been developed at this time.) These parts can compete with DRAMs and ferromagnetic disk memories. Scalability should not be a problem -- in fact FRAM cells should turn out to be more scalable than DRAM cells because the ferroelectric capacitors have a much higher dielectric constant (>1000) than CMOS SiO_2 capacitors. Thus only a very small capacitor area, perhaps the area of a contact via, is sufficient for storage purposes. In short, when one considers all the selection requirements for a nonvolatile memory, namely fast read/write, radiation hardness, cost effectiveness due to compatibility with currently used IC processing technology, high endurance and retention, and nondestructive readout (NDRO) capability, the ferroelectric memory stands out as the logical choice for all applications where submicrosecond operation is needed.[15]

2.2 Ferroelectric

2.2.1 Ferroelectric Properties

A ferroelectric material is a material that exhibits, over some range of temperature, a spontaneous electric polarization that can be reversed or reoriented by application of an electric field. This spontaneous polarization (P_s) must be nonvanishing when the electric field is removed and P_s must be able to reorient itself in an electric field. The P_s has two or

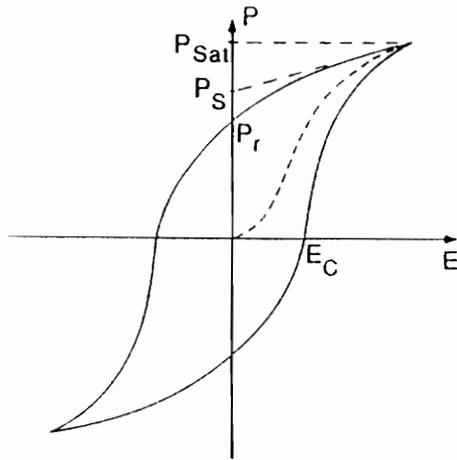
more possible orientation states in the absence of an electric field, and it can be switched between these states by applying appropriate electric fields.

One of the best-known features of ferroelectric materials is the response of the polarization to external electric fields, which is often referred to as simply the hysteresis loop [Fig. 1 (a)]. In a ceramic sample, the average displacement charge density D at low fields, is related to the polarization through the equation:

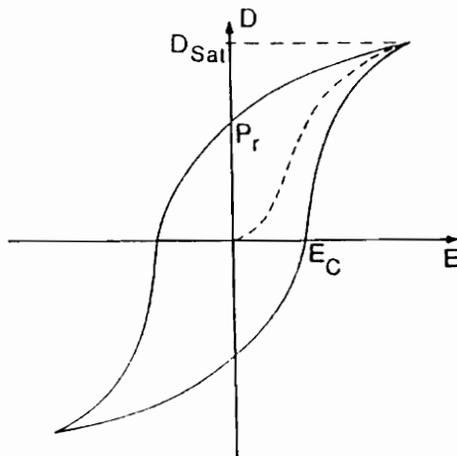
$$D_i = P_i + \epsilon_0 E_i$$

where ϵ_0 is the permittivity of free space. In most cases the $\epsilon_0 E_i$ is much smaller than the P_i term, so hysteresis plots of D versus E and P versus E (i.e., at high fields) become almost equivalent [Fig. 1 (b)]. The small signal relative permittivity, ϵ_r , is equal to the ratio ϵ/ϵ_0 . The ϵ term is found (in a macroscopic view) by measuring the capacitance of the metal-ferroelectric-metal unit. It is important to keep the field or voltage of the measurement as small as possible to prevent ferroelectric domains from reorienting and contributing to the permittivity.

The spontaneous polarization P_i is defined as the magnitude of the polarization within a single ferroelectric domain in the absence of an external electric field. If an electric field is applied, the domains that are closest to being parallel to the field grow while the others shrink. The macroscopic polarization with an external field applied is composed of the aligned spontaneous polarization, as well as electronic and additional ionic polarization generated by the external field. At a characteristic field, a maximum alignment of the spontaneous polarization occurs and the hysteresis curve saturates at P_{sat} because additional electronic and ionic polarization produced by an increase in the field is typically quite small compared to the spontaneous polarization. When the electric field is removed, the ionic and electronic polarization decrease to zero. The remanent -- remaining -- polarization P_r is the spontaneous polarization that remains aligned with the previously



(a)



(b)

Figure 1. Curves showing typical relationships between (a) polarization vs. electrical field, and (b) displacement charge vs. electric field for a ferroelectric dielectric are similar.

applied field. It can assume both positive and negative values. This polarization is what gives rise to the possibility of making nonvolatile ferroelectric memories.

In the hysteresis curve, the magnitude for the reverse electric field which decreases the net polarization to zero is called the coercive field E_C . At this point the net polarization reverses polarity if the reverse applied field is increased further. This E_C is also called the nominal threshold, above which the polarization changes sign. The two zero-field values $\pm P_r$ are equally stable. Thus, no applied field or voltage is required to maintain the memory, which is why the device is termed “nonvolatile.” This bistable operation may be contrasted with the operation of silicon DRAMs, which require a “refresh” voltage many times per second to maintain their stored information.

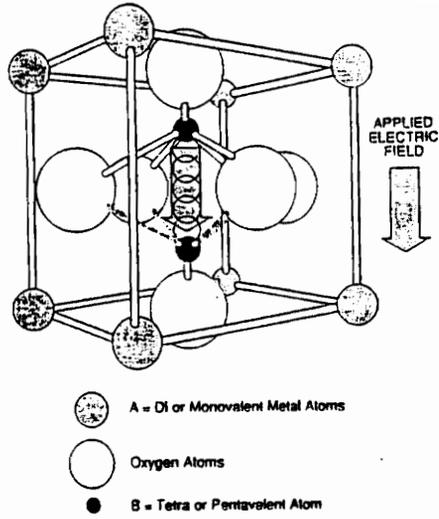
2.2.2 Ferroelectric Materials

2.2.2.1 Perovskite Structure

$\text{PbZr}_x\text{Ti}_{1-x}\text{O}_3$ (PZT) is the most popular ferroelectric material under investigation for nonvolatile memory applications. These ferroelectrics need to be crystallized in the perovskite phase (ABO_3) for them to exhibit ferroelectric behavior. In the tetragonal perovskite structure, the A^{2+} ions occupy the corners of the unit cell and the smaller B^{4+} ions are located at the body center. The oxygen ions (O^{2-}) are positioned at the face centers [Figure 2 (a)].

In the ferroelectric phase, the perovskite structure usually assumes one of three structural formations: tetragonal, orthorhombic or rhombohedral. In the tetragonal symmetry, a cubic cell stretches along one side (the “c-axis”) and shrinks along the other two sides (“a-axis”) forming a rectangular prism. The spontaneous polarization aligns itself parallel to the longest side. The orthorhombic structure is formed by stretching a

(a)



(b)

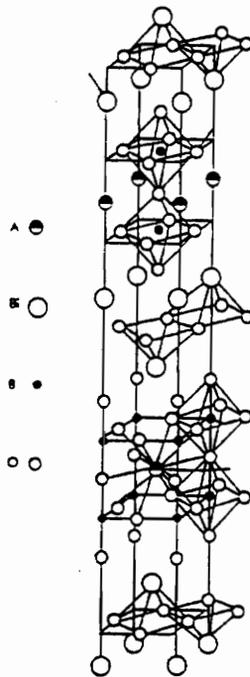


Figure 2. The lattice structure of ferroelectric materials: (a) Perovskite structure ABO_3 : Displacement of central atom B causes dipole moment; (b) Bismuth layered structure of $ABi_2B_2O_9$.

cube along a face diagonal along which the spontaneous polarization aligns itself. In a rhombohedral structure a cube is stretched along a body diagonal and the spontaneous polarization aligns in the direction of the stretched body diagonal.

A ferroelectric crystal of the tetragonal perovskite structure has two polarization states. In PbTiO_3 , for example, the Ti^{4+} ions occupy the centers of each cube; the Pb^{2+} ions are located at the corners; and O^{2-} ions are centered on each face of the undistorted lattice. In the distorted ferroelectric phase that is stable at room temperature, there is a net dipole (spontaneous polarization, P_S) of a few tens of microcoulombs per square centimeter produced primarily by the displacement up or down of the Ti^{4+} ions with respect to the other ions. In a crystal of PbTiO_3 that has not been specially prepared, we might expect to find regions in which the polarization is up and regions in which it is down, called “ferroelectric domains.” On application of an electric field greater than E_c , all the domains switch to orient themselves in the same direction [14].

However, these perovskite ferroelectrics, in general, are known to suffer from serious degradation problems such as fatigue (loss of switchable polarization with increasing reversal of polarization), aging, imprint and leakage current that affect the lifetime of the devices [6, 20, 23].

2.2.2.2 Layer Structure

Mixed bismuth oxide layer-structure ferroelectrics have the general form $(\text{Bi}_2\text{O}_2)^{2+}(\text{M}_{n-1}\text{R}_n\text{O}_{3n+1})^{2-}$, where $M = \text{Ba, Pb, Sr, Bi, K, or Na}$; $n = 2, 4, \text{ or } 5$; and $R = \text{Ti, Nb or Ta}$. These compounds have a pseudo-tetragonal symmetry and the structure is comprised of stacks of n perovskite-like units of nominal composition MRO_3 between Bi_2O_2 layers along the pseudo-tetragonal c -axis [10~13].

Recently, it has been found that $\text{SrBi}_2(\text{Ta}_x\text{Nb}_{1-x})_2\text{O}_9$ (SBTN) films, where $0 < x < 1$, are good candidates for fatigue-free FRAM applications on platinum electrodes [7]. The layered structure SBTN compounds consist of continuous solid solutions of $\text{SrBi}_2\text{Ta}_2\text{O}_9$ and $\text{SrBi}_2\text{Nb}_2\text{O}_9$. Their crystal lattices are orthorhombic and consist of two connected layers of TaO_6 (or NbO_6) octahedral, which are perovskite-like layers, separated by Bi_2O_2 layers as shown in Figure 2 (b). The perovskite-like units are continuous only in the planes perpendicular to the c -axis; along the c -axis, they are broken in their continuity by the presence of Bi_2O_2 layers. The presence of perovskite-like layers leads to spontaneous polarization in the plane of these layers. Spontaneous polarization is also known to occur along the c -axis where discontinuity of perovskite layers occurs. This indicates that the Bi_2O_2 layers also take part in the cooperative phenomenon that is responsible for ferroelectricity in these materials. Due to their layered superlattice structure, SBTN materials have unique ferroelectric properties.

2.3 Memory Applications

2.3.1 Basic Operation

For memory applications, we can switch the polarization of the entire ferroelectric crystal from up to down by reversing the applied field. In a large single crystal this would require voltages of several kilovolts. It would be impractical for a commercial device; but for a thin film of order 100 nm thick, it requires only a few volts. To understand how the nonvolatile ferroelectric memory works, we refer to the hysteresis curve. If a positive electric field greater than E_C is applied to the ferroelectric capacitor, then the film is polarized in the positive direction with a polarization value of P_S . Once the electric field is removed from the capacitor, the polarization relaxes slightly to the value P_T . We arbitrarily

call this positive polarization a "zero". If a negative voltage is applied to the ferroelectric film, the resulting polarization is in the negative direction at $-P_S$. This is called a "one". Again, when the voltage is removed, the polarization relaxes to the value $-P_T$. Thus we have two stable states at zero voltage which have been arbitrarily defined as "zero" and "one". This is a nonvolatile storage element since the data is present when the voltage is removed.

To read this storage element, we apply a positive voltage to the capacitor. If the stored data were a "zero", a small current equal to the increase in polarization from P_T to P_S is observed. If a "one" were stored, then the current is created by the change in polarization from $-P_T$ to P_S . The difference between these two currents is sensed to give the output from the memory. Obviously, the greater the difference between $dP(1)$ and $dP(0)$, the greater is the noise margin of the memory output. In a typical digital system, this noise margin must allow the determination of either one or zero to a probability of 0.999 [51]. Generally, the memory is destructively read since all data are now in the "zero" state. If we had stored a "one", it is required that we reverse the voltage and rewrite the negative polarization. This can be easily designed into the circuit.

Generally, the storage element of a ferroelectric memory cell consists of a ferroelectric film sandwiched between two electrodes. For memory applications this ferroelectric capacitor should comply with a number of device oriented requirements. These will influence the final memory characteristics and organization. Typically for reliable detection a switching polarization larger than $10 \text{ fC}/\mu\text{m}^2$ is needed. This level has to be reached after a short time ($<10 \text{ ns}$) and preferably with switching voltages below the standard supply voltages for memories. Today a nominal supply voltage of 5V is generally accepted, but there is a tendency to move to a nominal value of 3.3V. These requirements can only be met with thin films ($<500 \text{ nm}$) of materials with relatively small coercive field

strengths. For non-volatile memory applications the number of allowed reversal operations has to be large ($10^{14}\sim 10^{15}$) and the stability of the poled layers has to be very good (10 years retention) [16].

2.3.2 Ferroelectric memory types

Ferroelectric memories can be made in different processes and with different memory cell structures. Each of these parameters will not only influence the final memory characteristics but also the requirements for the ferroelectric layers. The basic type of integration scheme is destructive read-out (DRO) type where information must be rewritten after every read operation.

The ferroelectric shadow memory cell shown in Figure 3 (a) consists of two parts: a SRAM cell, that can be a full CMOS cell or an NMOS cell with polysilicon resistor loads, and two ferroelectric capacitors for non-volatile data storage. These capacitors are isolated from the SRAM cell by MOS transistors. In the normal mode these transistors which are connected to the "STORE" line are off and the SRAM cell is operated without affecting the ferroelectric capacitors. Only during STORE and RECALL operations (e.g. before and after a power removal, respectively) are these transistors on. During a STORE operation the data in the SRAM cell is written in the ferroelectric capacitors by switching their polarization in the appropriate direction. During a RECALL operation this polarization sets the SRAM back in the original state. Since these operations will be performed a limited number of times, the endurance requirements on the ferroelectric capacitors are modest. This memory concept is therefore safe but has the drawback of its large cell size and it is thus only suitable for memories with a limited number of bytes.

Much higher densities can be realized with the cell shown in Figure 3 (b). Here the ferroelectric capacitor forms an integral part of the memory cell. In fact, this cell is a

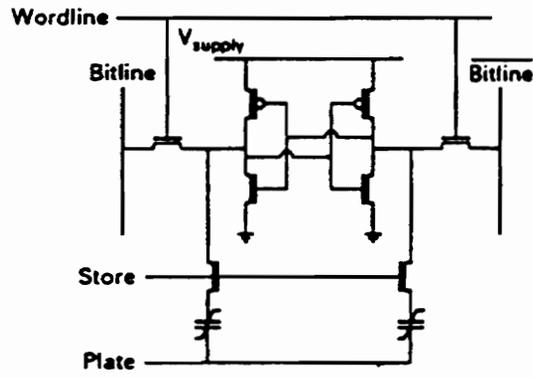


Figure 3 (a). Ferroelectric shadow memory cell

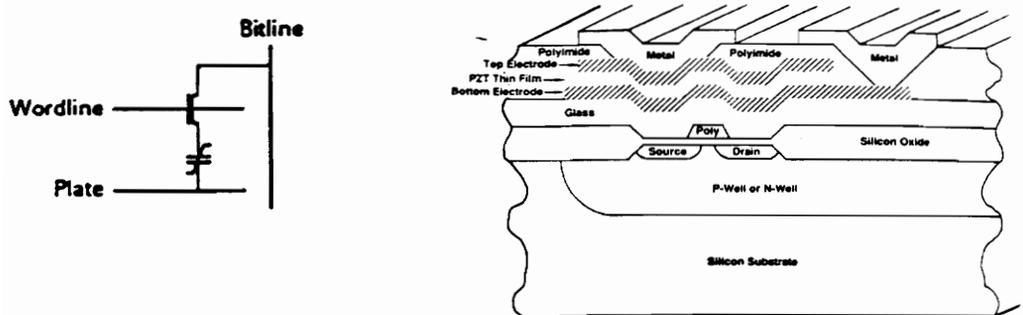


Figure 3 (b). DRAM type ferroelectric non-volatile cell.

DRAM cell with a thin ferroelectric film as the capacitor insulator. Since the dielectric constant of this material is high, this cell can also be used as a normal DRAM cell, for which data as charge has to be refreshed regularly. For a non-volatile memory the data in the cell will be stored by the directional polarization of the ferroelectric layer which also eliminates the need for a refresh operation. This cell which allows very high densities puts rather stringent requirements on the ferroelectric layers, especially with respect to the endurance. The polarization of the ferroelectric layer has to be switched for reading as well as for writing. Therefore a large number of polarization reversals has to be guaranteed. Memories that allow the selection of either the DRAM mode of operation or the non-volatile mode are very useful if a limited endurance is to be specified. The detection of the written data in a memory cell is commonly done via a comparison with a reference cell. This reference cell will be accessible to all the cells or else other detection principles have to be implemented. Mostly these will increase the access time. Reference cell problems can be avoided by using two memory cells for storing one bit. In one cell the data and in the other one the inverted data are stored. The detection of the written data (reading the cell) is done via a comparison of the contents of both cells. Now both cells are always accessed together and the reading is done in a differential way so that the absolute values are not so important. The two memory cells per bit concept is also often used to increase the read speed of the memory. Of course this is achieved at the expense of the memory density [16].

Another variation of the FRAM uses silicon bipolar transistor technology. This FRAM design requires pulsing a large common ferroelectric electrode at high speed, utilizing the high current capability of bipolar transistors. Second, bipolar technology provides a faster, more sensitive sense amplifier. Another type of FRAM using GaAs

JFET technology is being developed. This FRAM utilizes the ultrahigh circuit speed of GaAs and the radiation hardness associated with the JFET configuration.

2.4 Ferroelectric thin film process and integration

Recently developed techniques for the deposition of ferroelectric thin films are Metal Organic Deposition (MOD) and sol-gel processes. Most of the samples used in this study employed these techniques for deposition. With these processes the ferroelectric film is formed by the thermal decomposition of a solution of organo metallic compounds which are spun onto the substrate. The subsequent drying, firing and annealing processes of the film strongly influences the morphology and ferroelectric properties of the film. Thicker films can be obtained by repeating the spinning, drying and firing sequence. The main advantage of these processes is the ease by which complex oxide thin films can be prepared.

A very promising technique for ferroelectric thin films deposition, which still is in the exploratory phase, is Organo Metallic Chemical Vapor Deposition (OMCVD). This technique which offers advantages such as good step coverage, high deposition rate and low temperature deposition could be a very suitable way to increase the ferroelectric memory density and its performance. Other methods for the preparation of ferroelectric thin films include Pulse Laser Deposition (PLD) and Molecular Beam Epitaxy (MBE), but these currently do not comply with the requirements of IC production processes (large wafers, high throughput). Note that the thin film samples for complex impedance analysis in this study were prepared by using PLD.

The integration of ferroelectric thin films into a standard silicon IC process can basically be divided into three phases (Fig. 4). In the first phase the transistor is processed in a standard MOS process up to the passivation layer before contact hole etching. In the

second phase the ferroelectric stack is deposited by the aforementioned deposition techniques and the capacitor is fabricated. Finally, the back-end processing including the deposition of the isolation layer surrounding the capacitor is again done by standard processing [19].

Since ferroelectric processing involves reactive materials that are not common in silicon processing, special precautions have to be taken to prevent the ferroelectric processing from influencing the standard devices as well as to avoid the back-end processing destroying the ferroelectric characteristics. Solutions to these problems can range from the addition of suitable barrier layers, like TiO_2 , and adaptations in the ferroelectric capacitor processing to modifications in the back-end processing.

2.5 Memory design considerations

Several factors are of critical importance to the memory designer. The first of these is the location of the memory capacitor in relation to the access transistor. The initial design used by most researchers currently is the placement of the capacitor alongside the transistor structure as shown in Figure 5 (a). This arrangement allows the transistor manufacture to be completed after the ferroelectric capacitor is deposited. Thus the temperature sensitive steps of contact metal deposition and dopant diffusion can be performed after the high temperature annealing of the ferroelectric film. The latter process flow is essential for the GaAs-based memories at present. Figure 5 (b) shows the capacitor on top of the transistor and represents the ultimate in density since the memory cell dimensions are minimized. This configuration requires the transistor to be completely fabricated before the ferroelectric thin film is deposited and therefore presents severe processing constraints [51].

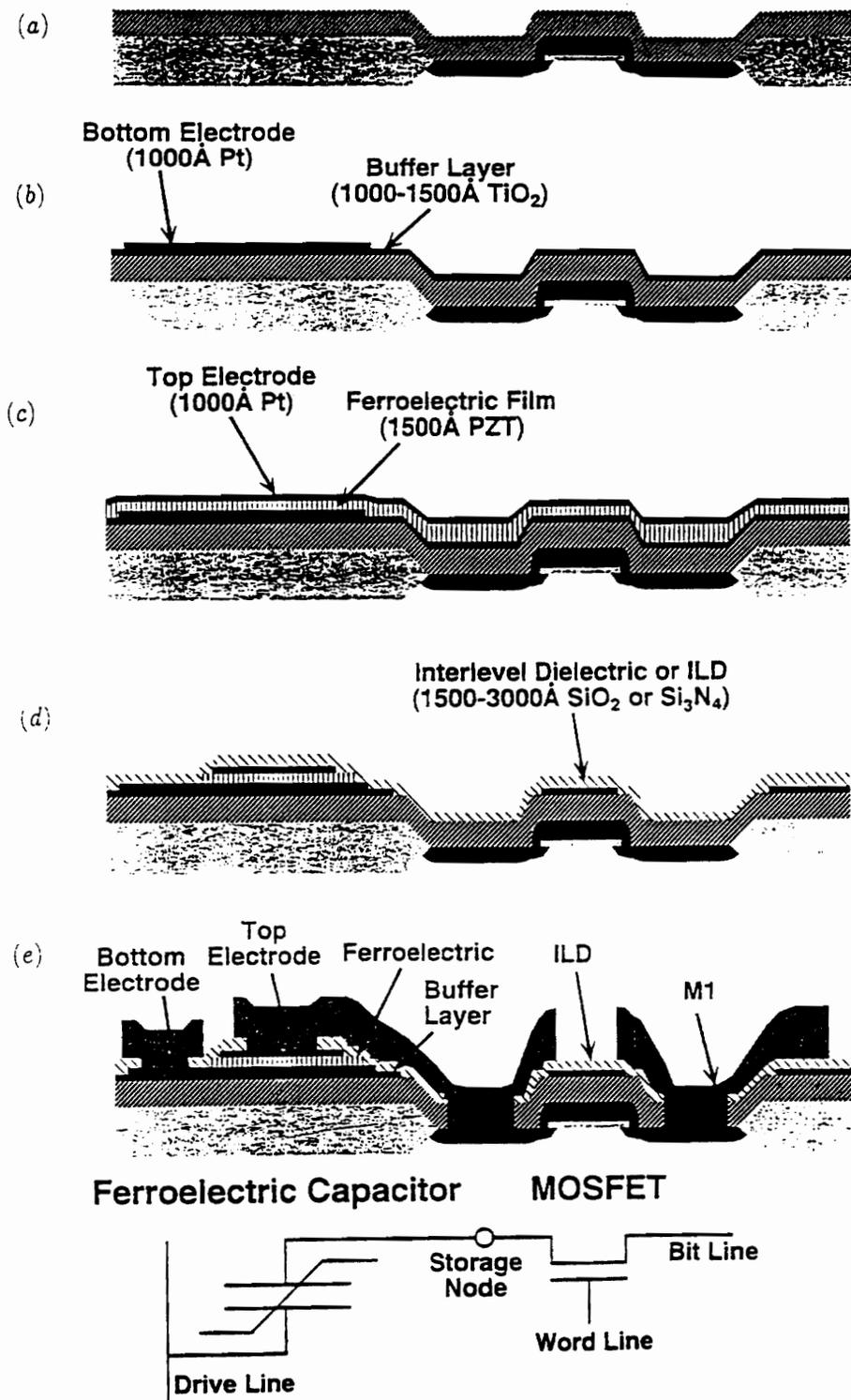


Figure 4. The ferroelectric capacitor process module is inserted in the CMOS process flow immediately prior to contact hole formation.

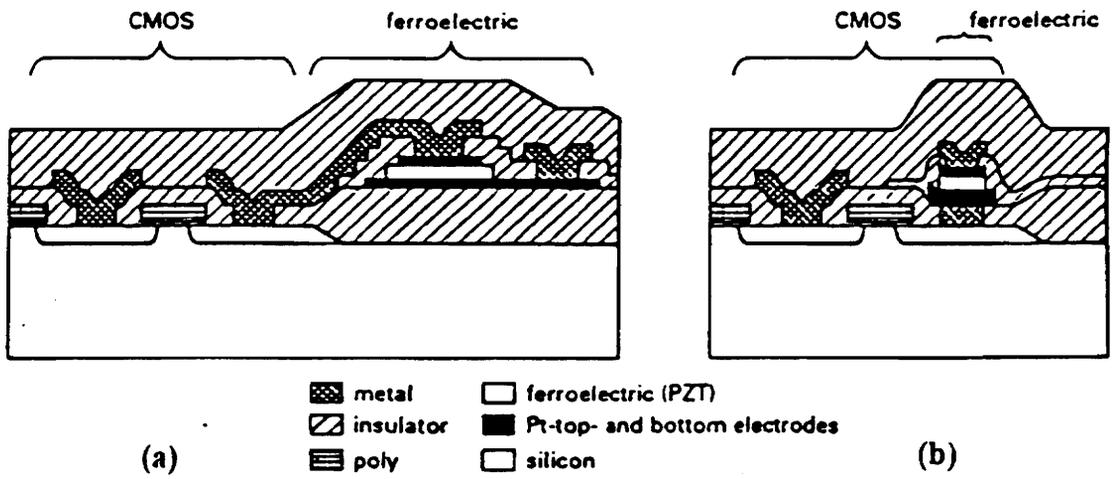


Figure 5. Cross sectional view of ferroelectric capacitors integrated with MOS transistors: (a) side-configuration and (b) stack-configuration.

The second major factor is the organization of the memory. Is the data stored as a single bit where a reference capacitor is used for sensing, or is the data stored as the bit and its complement where two storage elements are used and then the outputs compared? The two methods are shown in Figures 6 (a) and (b). The obvious advantage of the single storage element is a two fold increase in memory capacity for the same chip area. Dual storage, on the other hand, provides for a smaller remanent polarization before the data cannot be recognized. Figure 7 presents the circuit for a memory that is externally switchable from the single storage element to the dual storage. The capacity is 4-kbits if single element and 2-kbits if dual storage. The reference capacitors are ignored when the dual option is selected. Figure 7 also shows the automatic rewrite circuitry needed for the DRO (destructive read-out) design. This feature is essential for a practical memory [51].

The physical size of the capacitor and its compatibility with the semiconductor process used are major limitations to developing a practical commercial memory. The capacitor must have a coercive voltage below the standard operating voltage of the semiconductor process to insure compatibility. This means that the coercive voltage should be one volt or less for most processes. In practice, this limits the film thickness to the range of 100 to 200 nm. Other electrical parameters of importance are the saturated and remanent polarization values and the symmetry of the hysteresis loop. To insure compatibility with the underlying semiconductor process, both silicon and GaAs, the processing temperature of the ferroelectric film should be as low as possible with 550°C the maximum for most processes. This will allow the capacitor on top of the transistor. To make practical memory circuits with commercial yields, the uniformity of the ferroelectric properties of the thin film must be maintained over the area of the chip and over the entire wafer area. A uniformity of 1% within the chip area and 5% over the wafer are desirable [17].

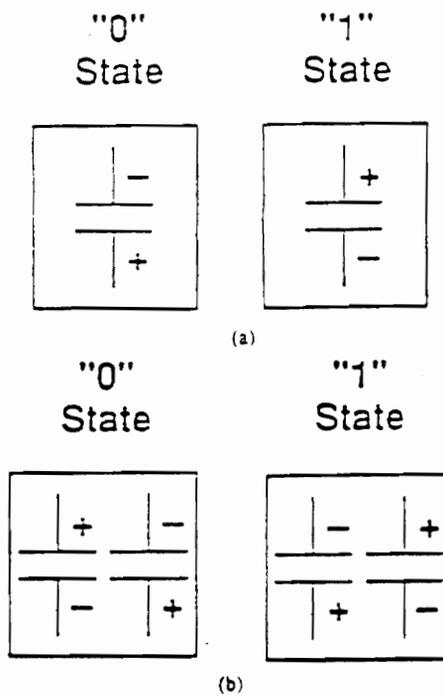


Figure 6. FRAM cell configurations. (a) 1-capacitor/cell -- small cell size, reduced interconnect. (b) 2-capacitor/cell -- separate reference not needed, provides larger difference to sense amplifier.

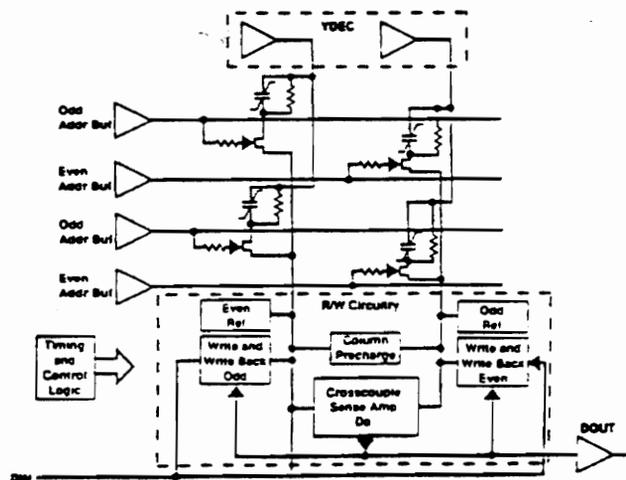


Figure 7. 4K-bit FRAM (512X8) [17].

Chapter 3

Electrical Characterizations (I)

3.1 Hysteresis

A number of electrical characterization methods are used to determine the suitability of ferroelectric thin films for specific applications. Hysteresis loop, fatigue, retention, imprint, leakage current, etc. are some typical examples of these characterization techniques. Hysteresis loop is the most basic ferroelectric characterization technique that provides very useful information concerning ferroelectricity, such as the saturation field, coercive field, switchable polarization, spontaneous polarization and remnant polarization.

3.1.1 Sawyer-Tower circuit

The most frequently used test set-up to characterize the hysteresis of ferroelectrics is the Sawyer-Tower circuit as shown in Figure 8 [8]. In the Sawyer-Tower circuit an integrating (linear dielectric) capacitor C_i (sensing capacitor) is connected in series with the ferroelectric capacitor. The application of a sine wave of +/- 5V and 100 Hz frequency to the ferroelectric capacitor and Channel 1 of the oscilloscope (Tektronix TDS 520 used in this study) is supplied by a pulse/function generator (HP8116A) with low output impedance (50Ω). The value of C_i is chosen to be large enough (40 nF) such that most of the voltage drop in the circuit occurs across the ferroelectric capacitor. Thus, the voltage at x is a close approximation to the voltage across the ferroelectric capacitor. The voltage developed across C_i is given by $\int i dt / C_i$ and hence the voltage at point y is proportional to the charge q flowing through the ferroelectric capacitor. By connecting points x and y

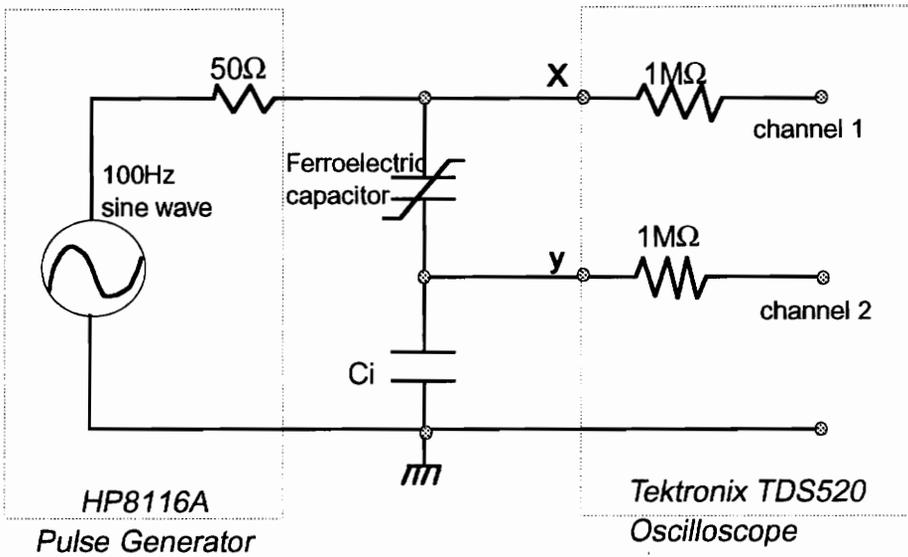


Figure 8. The set-up of Sawyer-Tower circuit.

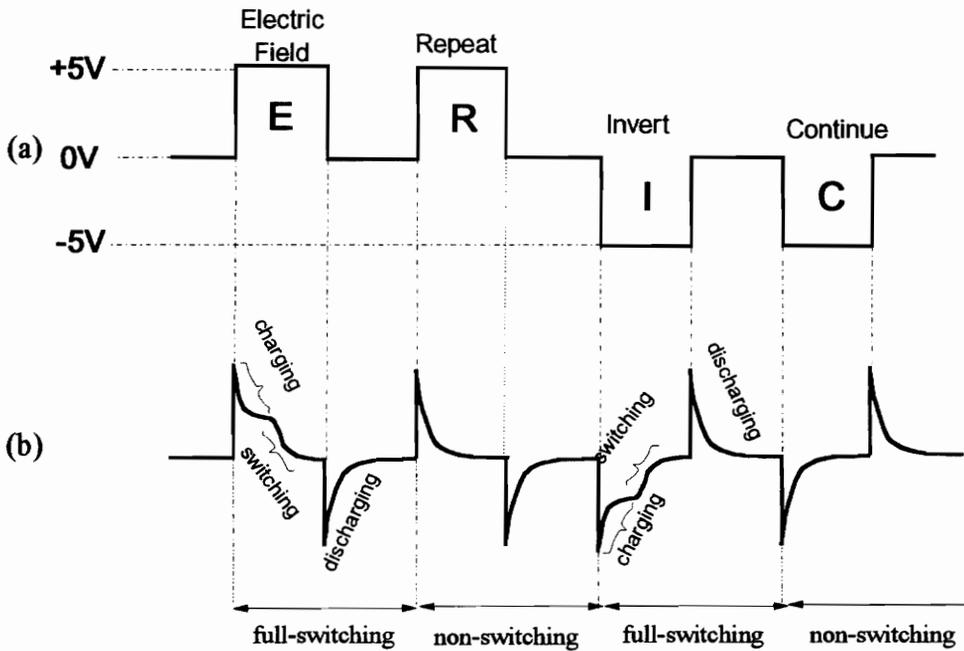


Figure 9. Pulse switching measurement with (a) input (voltage) pulse train [ERIC] and (b) output (current) response.

respectively to the Channels 1 and 2 of the oscilloscope with high input impedance setting (of 1 M Ω), one can obtain the q versus V characteristic of the ferroelectric capacitor. It is customary to calibrate the vertical axis of the plot in terms of polarization P ($\mu\text{C}/\text{cm}^2$) rather than q , where $P = q/\text{Area}$. Three parameters are usually measured from the hysteresis loop: (a) the coercive field E_c defined by the horizontal intercept, (b) the remanant polarization P_r defined by the vertical intercept and (c) the saturation polarization P_s classically defined by the intercept on the polarization axis of the extrapolation of the linear extremum of the loop. The loop parameters are a function of the frequency at which the hysteresis loop is traversed. In particular, the values of P_r and P_s decrease as the frequency increases. In most materials at frequencies above 100 kHz, the loop parameters have decreased to less than 0.1 of their DC value. This is due primarily to the basic limitation on the speed at which the domains can switch. The loop parameters are also a function of temperature.

For ferroelectric switching applications (memory device in computer architecture), electrical sensing of the cell polarization state performed by pulse measurement is required. The drive signals to the ferroelectric capacitor are in the pulse sequence (ERIC) with sufficient magnitude and duration of voltage shown in Figure 9 (a). The Sawyer-Tower circuit mentioned above need to have a small resistor in place of the C_i . The resistor is chosen to be small enough ($<10\text{ K}\Omega$) that most of the voltage drop occurs across the ferroelectric capacitor. This modification can be done by just taking out C_i from the circuit and setting both Channel 1 and 2 input impedance of the oscilloscope to 50 Ω . Since the voltage developed across the resistor in Channel 2 is proportional to the current flowing in the circuit, the displacement current from the ferroelectric capacitor can be monitored in Channel 2 of the oscilloscope [Fig. 9 (b)]. If the voltage pulse reverses the polarization of the ferroelectric that was previously polarized in the opposite direction, the

resulting displacement or full switching (f_s) current transient is illustrated as Curves 1 and 3 in Figure 9 (b). An initial spike is due to the charging of the linear dielectric component followed by a smooth humped curve due to the switching of the non-linear dielectric component. The area under these curves is given by:

$$\int^{f_s} i(t) dt = A (P_s + P_r + \epsilon_0 \epsilon_r E)$$

where A is the electrode area, E is the electric field, P_r is the remanant polarization, P_s is the saturation polarization (for a given E), ϵ_0 is the permittivity of free space, and ϵ_r is the small signal relative permittivity of the ferroelectric capacitor. Conversely, non-switching (n_s) current transients [Curves 2 and 4 in Fig. 9 (b)] result if the applied voltage pulse is in the same direction as the previously polarized state. The area under these curves is given by:

$$\int^{n_s} i(t) dt = A (P_s - P_r + \epsilon_0 \epsilon_r E)$$

Thus, the previous polarization state of the ferroelectric capacitor may be sensed, although in a manner which disturbs the cell state during the f_s transient. Consequently, the cell must be refreshed after being read.

To determine quantitatively the field and time dependence of polarization reversal, the difference between the areas of f_s and n_s transients gives the switchable component of the polarization (P_r):[18]

$$\int^{f_s} i(t) dt - \int^{n_s} i(t) dt = 2P_r A.$$

Due to its simplicity and low cost, the Sawyer-Tower circuit is the common method for characterizing ferroelectric devices. However, it is susceptible to significant errors from parasitic elements (particularly associated with the sense capacitor C_i) and is limited by the accuracy to which the sense capacitor value is known. Consequently, it may be difficult to calibrate and to compare results from different test setups.

3.1.2 RT66A Standardized Ferroelectric Test System [9]

In our study, we use a RT66A standardized ferroelectric test system from Radiant Technology to characterize the hysteresis loop more efficiently. Figure 10 shows the basic block diagram of this system. This system has another alternative testing mode, Virtual Ground, in addition to the Sawyer-Tower mode. The Virtual Ground mode (Fig. 10) measures the charge stored in the ferroelectric capacitor by integrating the current required to maintain one terminal of the sample at zero volts -- hence the term "virtual" ground. By eliminating the external sense capacitor, this circuit drastically reduces the effects of parasitic elements. The precision capacitor used as the feedback element in the current integrator is now a key element in obtaining high accuracy with this technique. The current amplifier and integrator stages of the virtual ground circuit can be designed and constructed to minimize gain and offset errors. They can also be calibrated in order to standardize measurements and be re-calibrated as needed to compensate for drift or changes during test set up in the RT66A system. In summary, the Virtual Ground mode allows device characterization with improved accuracy and allows results obtained from different test set ups to be compared with confidence.

Almost all the hysteresis characterization in this study were performed with the CHARGE program of RT66A system. The system not only provides an accurate, standardized and software controlled measurement, it also performs the corresponding pulse response and bipolar resistivity measurement simultaneously in hysteresis measurement with CHARGE program.

In the CHARGE program, the system generates a single triangular wave beginning at 0 volt and stepping in discrete voltage intervals to the assigned V_{max} (+/-5V), then back to 0 volt, then to $-V_{max}$, and then back to 0 volt. The integrating capacitor in the test unit is shorted before the hysteresis test is run. One hysteresis is run to preset the

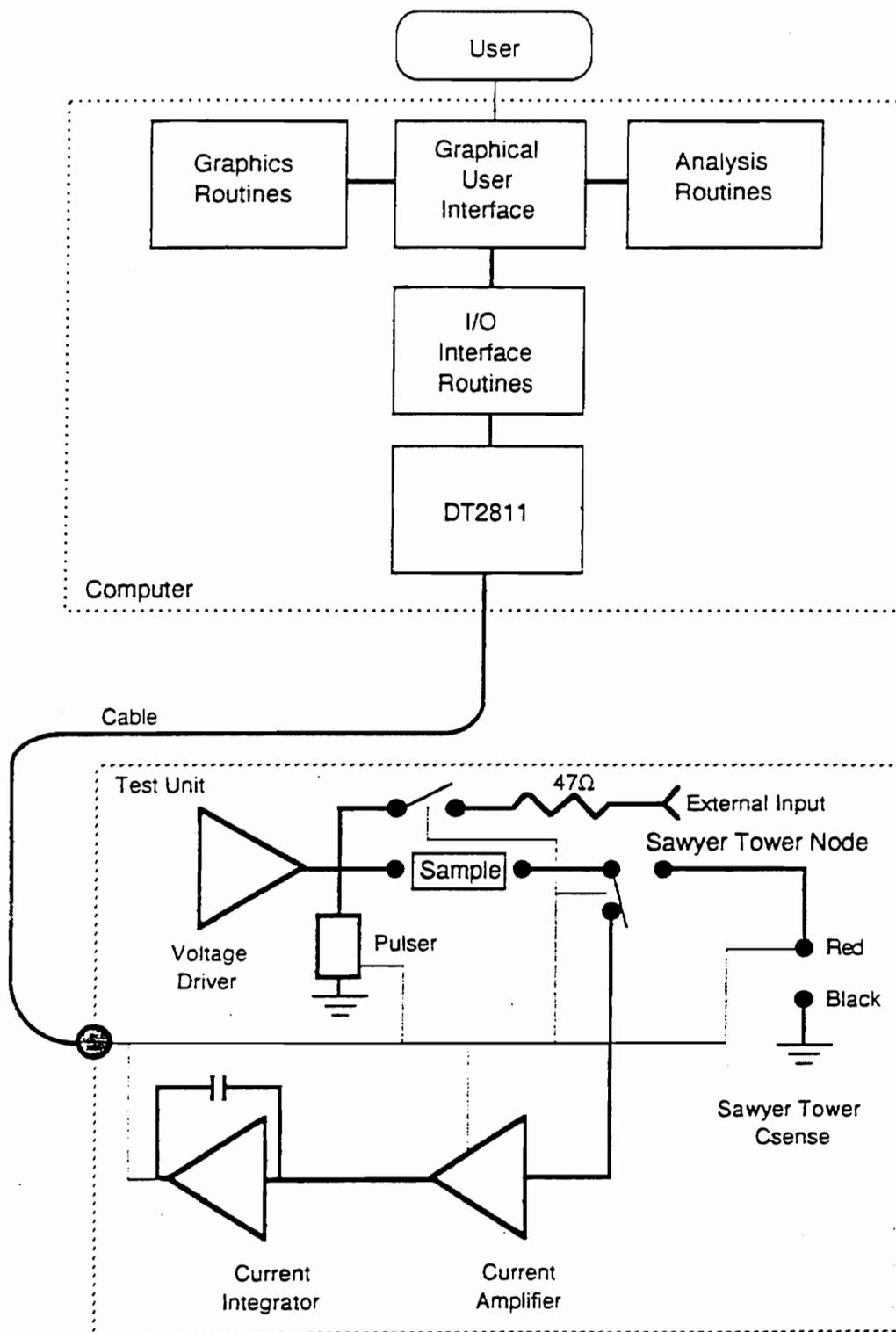


Figure 10. RT66A test unit block diagram.

ferroelectric capacitor to the appropriate remanant polarization. After a 1 second waiting time, a second hysteresis sequence is run while the integrating capacitor collects charge from the virtual ground. The voltage at the output of the integrating capacitor is measured by an A/D converter after each voltage step.

In an actual memory circuit, the READ and WRITE operations are carried out by voltage pulses applied across the ferroelectric capacitor. During the READ operation, switching and non-switching currents obtained by the application of appropriate pulses as mentioned in previous section are converted into voltage and are used for sensing the stored data. In order to simulate the actual read/write operations and to estimate the resulting switched and unswitched polarization, a pulse measurement is adopted. As mentioned before, the pulse measurement is also carried out simultaneously in CHARGE program during hysteresis measurement.

The pulsed polarization test consists of a sequence of five triangular pulses in RT66A system, each pulse being separated from the previous one by 1 second. The polarity of the various pulses is determined by a user defined quantity, V_{max} . The first pulse presets the ferroelectric capacitor to $Pr(-V_{max})$. For the next four pulses, the integrating capacitor is zeroed out prior to each pulse. The voltage across the integrating capacitor is measured at the top and bottom of each pulse. The parameters measured at each point are listed below (Fig. 11):

- (i) $Pr(X)$ = remanant polarization state at zero volt after application of X volt.
- (ii) $Ps(X)$ = the polarization state at X volts.
- (iii) $P^* = Ps(V_{max}) - Pr(-V_{max})$, the polarization transferred out of the capacitor traversing from zero to V_{max} volt when the capacitor starts at $Pr(-V_{max})$.

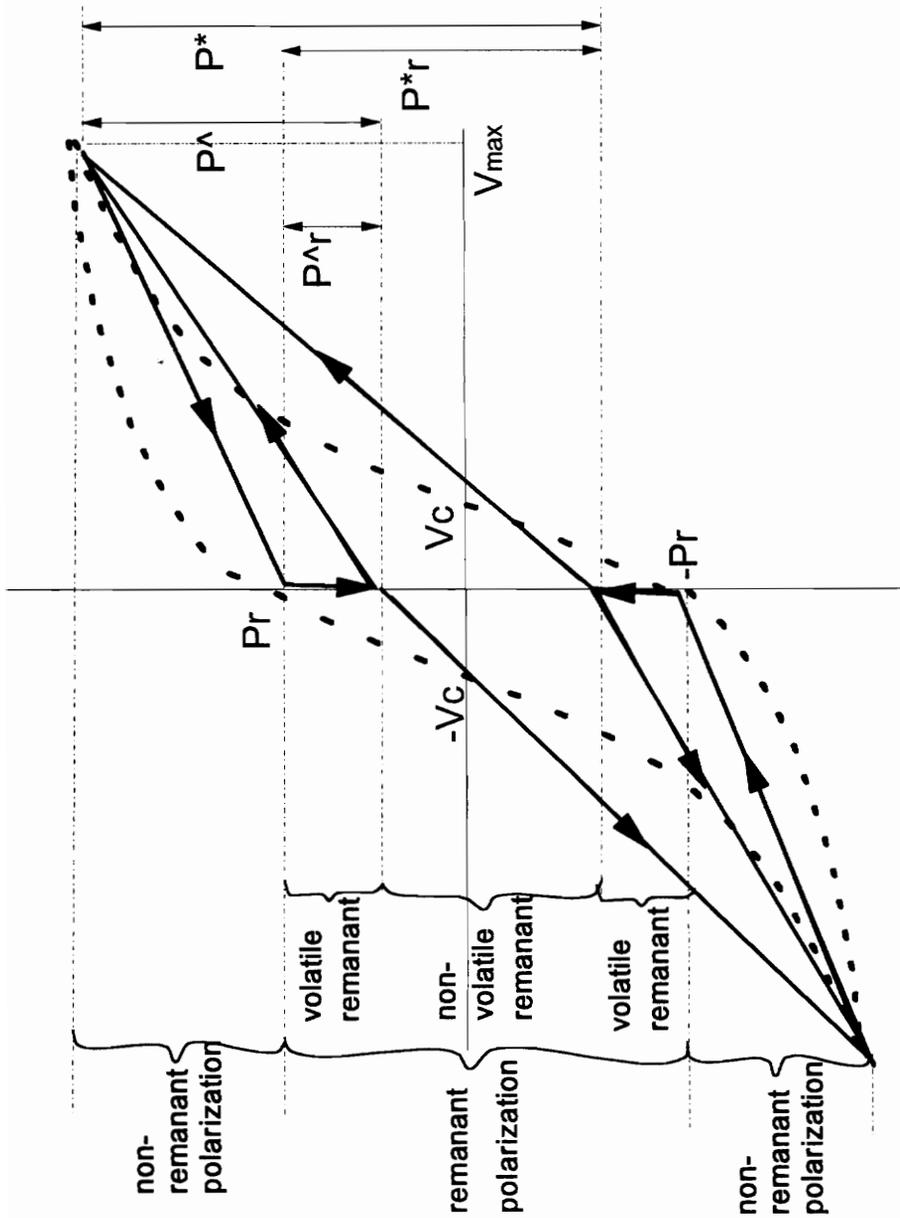


Figure 11. An ideal ferroelectric hysteresis loop (dashed line) exhibits two polarization components: the non-remnant and remnant polarization. The hysteresis loop of real ferroelectric capacitor is tracked as solid lines showed parameter terms defined in pulse measurement.

- (iv) $P^*r = Pr(V_{max}) - Pr(-V_{max})$, the polarization remaining out of the sample capacitor after returning to zero volt from V_{max} , when the capacitor starts at $Pr(-V_{max})$.
- (v) $P^\wedge = Px(V_{max}) - Pr(V_{max})$, the polarization transferred out of the capacitor traversing from zero to V_{max} volt when the capacitor starts at $Pr(V_{max})$.
- (vi) $P^\rceil = Pr(V_{max}) - Pr(V_{max})$, the polarization remaining out of the ferroelectric capacitor after returning to zero volts from V_{max} , when the capacitor starts at $Pr(V_{max})$.

These parameters need to be determined to observe the polarization relaxation (discussed in following section) of a ferroelectric capacitor qualitatively and quantitatively, and thereby understand the reliability of a ferroelectric capacitor as a memory device.

3.1.3 Polarization relaxation

An ideal ferroelectric hysteresis loop is shown in the dashed line of Figure 11. The polarization consists of non-remnant and remnant components. A non-remnant component $[(P^* - P^*r) \text{ or } (P^\wedge - P^\rceil)]$ which is suitable for ferroelectric DRAM but is undesirable for non-volatile memory is caused by non-ferroelectric ionic and electronic polarizability as well as field-induced spontaneous ferroelectric domain wall motion. The remnant component which represents the non-volatile memory signal margin is induced by ferroelectric domain switching. Any real ferroelectric capacitor exhibits polarization relaxation as demonstrated by the track of solid lines in Figure 11. This relaxation process is manifested in a logarithmic time-domain decay of the remnant polarization and commences immediately after the removal of an applied field. Therefore, the remnant polarization of a real ferroelectric capacitor is divided into a "volatile" component $(P^\wedge - P^\rceil)$ which relaxes completely within microseconds of the removal of an applied field and a "nonvolatile" component $(P^*r - P^\rceil)$ which remains after all relaxation processes are complete.

There are several important implications of remanant polarization relaxation for ferroelectric non-volatile memory operations. First, any relaxation directly reduces the device signal margin since it shrinks the polarization margins of each corresponding logic signal. In addition, since the magnitude of relaxation depends on how often an individual bit is accessed, sufficient margins for sensing are necessary to account for the different signal margins obtained for unrelaxed, partially relaxed and completely relaxed bits. Finally, polarization relaxation degrades the ferroelectric reliability as discussed in fatigue, retention and imprint sections [19].

3.1.4 PZT vs SBT

For perovskite structure ferroelectric, sol gel derived PZT was spin coated on the Pt/Ti/SiO₂/Si substrate with Pt layer as the bottom electrode of the capacitor. The PZT precursors were prepared from a metallorganic solution of lead acetate, zirconium n-propoxide, and titanium isopropoxide dissolved in acetic acid and n-propanol. The solution was hydrolyzed to form the precursor. Ten percent excess lead was added to the solutions to compensate for the loss of lead during high temperature processing. Precursors of different compositions were prepared by varying the ratios of Zr/Ti content. The coated films were then annealed at 650°C for 30 min in air. Finally, top electrodes Pt were deposited onto the films through a shadow mask by r.f. sputtering.

This study has concentrated on the 53/47 (Zr/Ti) composition because this composition is close to morphotropic phase boundary (MPB) in the PZT phase diagram [20]. At compositions close to MPB, both tetragonal and rhombohedral phases coexist. The tetragonal phase has six polarization directions and the rhombohedral phase has eight. The MPB composition has all fourteen polarization directions, therefore there are a higher number of polarization directions that can be used for domain switching. The hysteresis

loop obtained from this sample by using RT66A system is shown in Figure 12 (a). The value of $P_r = 22.8 \sim 25.6 \mu\text{C}/\text{cm}^2$ and $E_c = 26.3 \sim 37.3 \text{ kV}/\text{cm}$ was observed, which are well within the requirements for nonvolatile memory applications.

For bismuth layered structure ferroelectric $\text{SrBi}_2\text{Ta}_2\text{O}_9$ (SBT) thin films were chosen and fabricated by metalorganic deposition (MOD). A suitable organic precursor, dissolved in solution, was dispensed onto the Pt/Ti/SiO₂/Si substrate for spin coating with Pt layer as the bottom electrode. In this study, SBT films were prepared by varying the organic with different excess bismuth content. Six samples with 0%, 10%, 30%, 50%, 70% and 100% excess bismuth content were prepared. The soft metalorganic film was then pyrolyzed in air, oxygen, nitrogen, or other suitable atmospheres to convert the metalorganic precursors to their constituent elements, oxides, or other compounds. The annealing treatments were typically carried out at 700°C for 3 hours in oxygen atmosphere. Top Pt electrodes were deposited onto the films through a shadow mask by rf sputtering. The second annealing was done at 750°C for one after top electrode deposition in order to achieve the same heat treatment for top and bottom electrodes, to improve the asymmetry in hysteresis loop.

The hysteresis loops of the SBT samples were characterized by the RT66A system as shown in Figure 12 (b). By observing the hysteresis properties of the samples, the optimum range of excess bismuth content was determined to be 30% to 50%. The studies of phase formation found that SBT and bismuth oxide (Bi_2O_3) could form limited solid solution $(\text{Sr}_{1-x}\text{Bi}_x)\text{Bi}_2(\text{Ta}_{2-x/2}\text{Bi}_{x/2})\text{O}_9$ for $0 \leq x \leq 0.4$. With increasing Bi excess, the phase formation temperature of SBT decreased significantly by about 50 ~ 100°C, the grain size of SBT films increased from 0.08 to 0.2 μ , and the density of the films also increased. On the other hand, the SBT films exhibit a and b axis preferred orientation with increasing Bi excess. For these reasons, the polarizations of the hysteresis loop also increased with

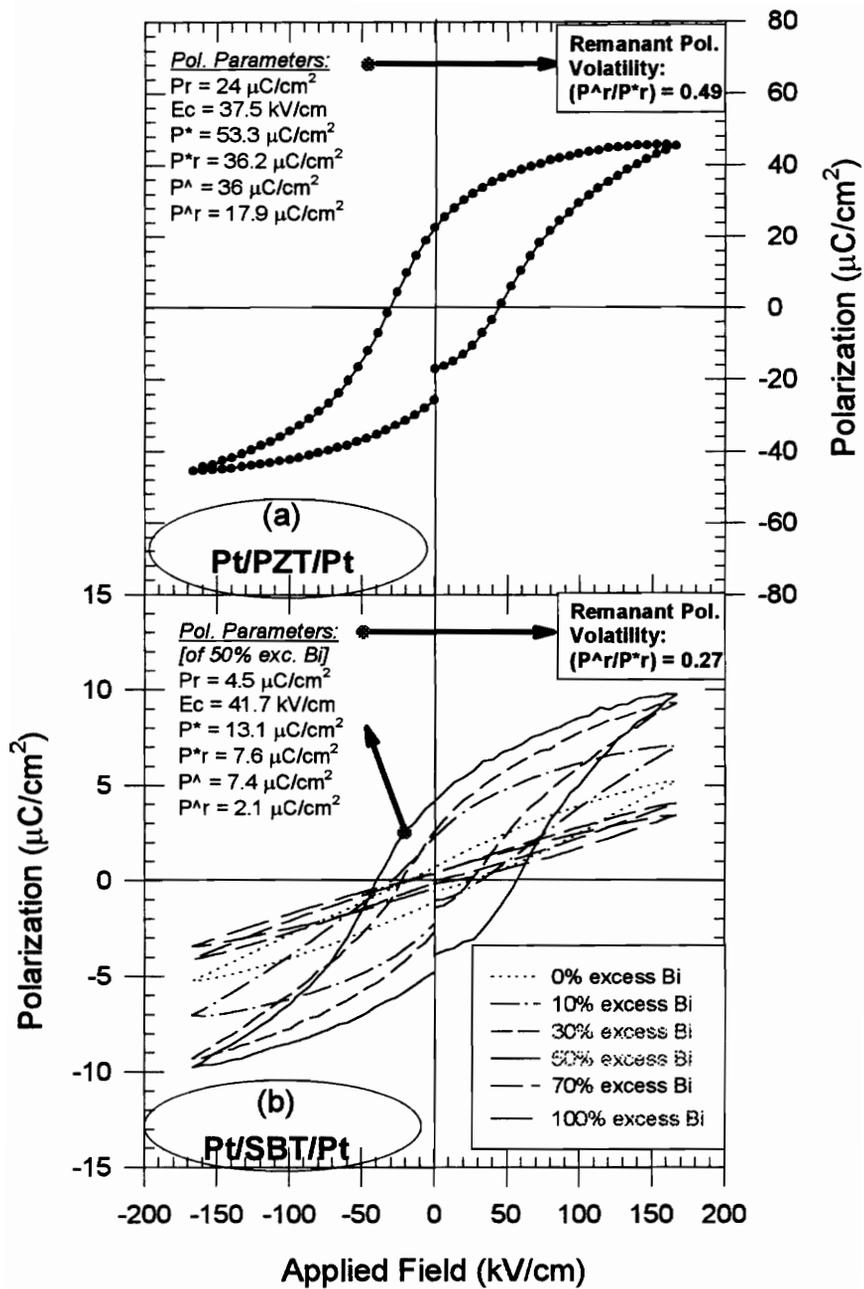


Figure 12. (a) Typical hysteresis loop of Pt/PZT/Pt
 (b) Excess bismuth dependent hysteresis loops of Pt/SBT/Pt.

increasing Bi excess content. However, for $x > 0.4$, Bi_2O_3 occurred as a second phase resulting in the worsening of the hysteresis properties [21].

In comparison, the PZT films exhibit a far higher polarization than SBT films. The polarizations in SBT films might be hindered by the existence of Bi_2O_3 layer, because its presence interrupts the continuity of perovskite-like layers along c-axis. However, SBT films with $P_r = 4.2 \sim 4.7 \mu\text{C}/\text{cm}^2$ and $E_c = 40.3 \sim 56.7 \text{ kV}/\text{cm}$ are still eligible for nonvolatile memory applications. Besides, the polarization relaxation of PZT films are more severe than that of SBT films. This can be seen by observing the volatility percentage of remanant polarization (the percentage ratio of $P^{\wedge}r$ to P^*r), 49% of PZT compared to 27% of SBT. The higher volatility of remanant polarization of PZT films make them susceptible to reliability problems of nonvolatile memory applications, such as retention and imprint problems discussed Section 3.4. This is also the primary problem that hinders PZT materials from extensive commercial usage in nonvolatile memory devices.

3.2 Fatigue

A principal drawback to early ferroelectric memories was the fact that the amount of switched charge decreased with use. Typically, early FRAMs (PZT as the material) degraded to 50% of its initial value after 10^6 read/write cycles. This is a profound problem for non-volatile FRAM because it is normally designed with destructive read-out (DRO). If FRAM is to become competitive with other non-volatile memory, like EEPROM (permits 10^5 write but 10^{15} read operations) [1], either it must be improved to withstand at least 10^{12} read/write operations or must have qualitatively different nondestructive read operations. The phenomena responsible for this failure is fatigue, which is unique to ferroelectric technology. Fatigue manifests itself as the gradual loss of detectable remanant

polarization following many polarization reversals. In a memory, the signal margin is observed to deteriorate after a bit is accessed many times. Since non-volatile FRAM has DRO operation, fatigue limits both the read and write endurance.

3.2.1 Test setup

A fatigue test is performed by subjecting the ferroelectric capacitor to a bipolar pulse train with known frequency and amplitude. An applied maximum frequency of the pulses should be ensured to eliminate the possibility of partial switching. If partial switching occurs, the switched charge will diminish and the fatigue results will be incorrect.

Principally, the fatigue test can be carried out using Sawyer-Tower circuit shown in Figure 8. However, in order to load the pulse stress into the ferroelectric capacitor the sensing capacitor should be taken out and the oscilloscope's input impedance of Channel 2 should be set to a low value of 50Ω . The fatigue cycles are provided by pulse generator HP8116A with chosen frequency (<500 kHz), amplitude (5V) and elapse time (cycle). Before continuing the test, full switching of the ferroelectric capacitor should be confirmed for a chosen frequency by evaluating the switching output response in Channel 2. After each fatigue cycle period, a pulse measurement mentioned in Section 3.1.1 is performed to obtain the switched polarization. The polarization switched charge is calculated by subtracting the measured non-switching (n_s) from the full switching (f_s) charge. Finally, a comparison of switched polarizations is evaluated between the initial state and after each fatigue cycle period.

However, similar to hysteresis measurement, RT66A system also provides a computerized fatigue test program called FATIGUE. We use this system with Virtual Ground mode typically for our study. The user may specify the voltage (5V) used to

fatigue the sample, the pulse format (external), and the pulse width (frequency). A sequential profile of up to 16 fatigue periods with chosen fatigue cycles for each period may be specified. The internally generated pulses of the system is limited to an applied frequency of ~14 kHz. In order to acquire fatigue information within a reasonable period of time, the applied pulses are supplied by an external pulse generator HP8116A with chosen frequency (<500 kHz), amplitude (5V) and time (cycle) via "external input" shown in Figure 10. A pulse response measurement is taken after each fatigue period. The switched polarizations ($+/-dPr = +/-P^*r - +/-P^{\wedge}r$) for each fatigue period are taken from the result. The fatigue cycles of each period should be multiplied with the set frequency of the pulse generator to obtain the real fatigue cycles.

3.2.2 Fatigue mechanism

Fatigue in ferroelectrics is thought to arise from three different microscopic causes:

- (i) Stress relaxation of 90° domains in pseudocubic crystals (such as PZT); there the orthogonal domains slowly relax back to 180° configurations as mechanical stresses are released internally, and in doing so reorient and reduce the net polarization. The "pinning" of 180° domains by stress or charged defects is a related fatigue mechanism [22].
- (ii) "Poling" of charged defect pairs, such as lead-vacancy, oxygen-vacancy neighbors; these dipoles become aligned with repetitive application of large electric fields and are very slow to reverse, thus reducing or canceling some switched lattice polarization [23].
- (iii) Space-charge accumulation at or near the electrode-ferroelectric interface; this compensates for the applied voltage and acts as a detrimental screening of external fields [24].

Desu and Yoo have proposed a fatigue mechanism model Based on space charges as fatigue sources [25, 26]. According to the model, when intrinsic defects such as vacancies and mobile impurity ions exist in ferroelectric films, they can migrate under an electric field. This electric field is the local field (E_L) and consists of external applied field (E_A) and internal field (E_i) caused by polarization at the electrode-ferroelectric interface with relationship: $E_L = E_A - E_i$. The fatigue test under the applied alternating field (E_A) [Fig. 13 (a)] moves the defects back and forth as illustrated in Figure 13 (b).

When defects arrive at the grain boundaries, domain boundaries, and electrode-ferroelectric interfaces, they will be trapped because of the chemical instability at these boundaries and interfaces. These boundaries or interfaces provide low potential energy sites for the defects as a result of their large interfacial energy. The entrapped defects can either cause domain pinning or structural damage to the electrode-ferroelectric interface, resulting in polarization loss. The polarization loss will occur continuously under alternating pulses and the polarization value produced by the each polarity and next opposite polarity will be different. Because of this asymmetric polarization, the net flux density is determined by the internal field difference. As the internal field decreases due to polarization loss, the local field becomes larger resulting in increased moving distance of defects. Therefore, effective unidirectional migration of defects will occur as in Figure 13 (c), which demonstrates the defects moving closer to the interfaces with the increase of test cycling. Eventually by the test cycling, the entrapped defects accumulate gradually at the interfaces followed by the gradual loss of polarization during each cycle.

3.2.3 Fatigue in PZT vs SBT

Figure 14 shows the fatigue results of Pt/PZT/Pt versus Pt/SBT/Pt with 50% excess Bi (all other SBTs with 0%, 10%, 30%, 70%.and 100% excess Bi had the same

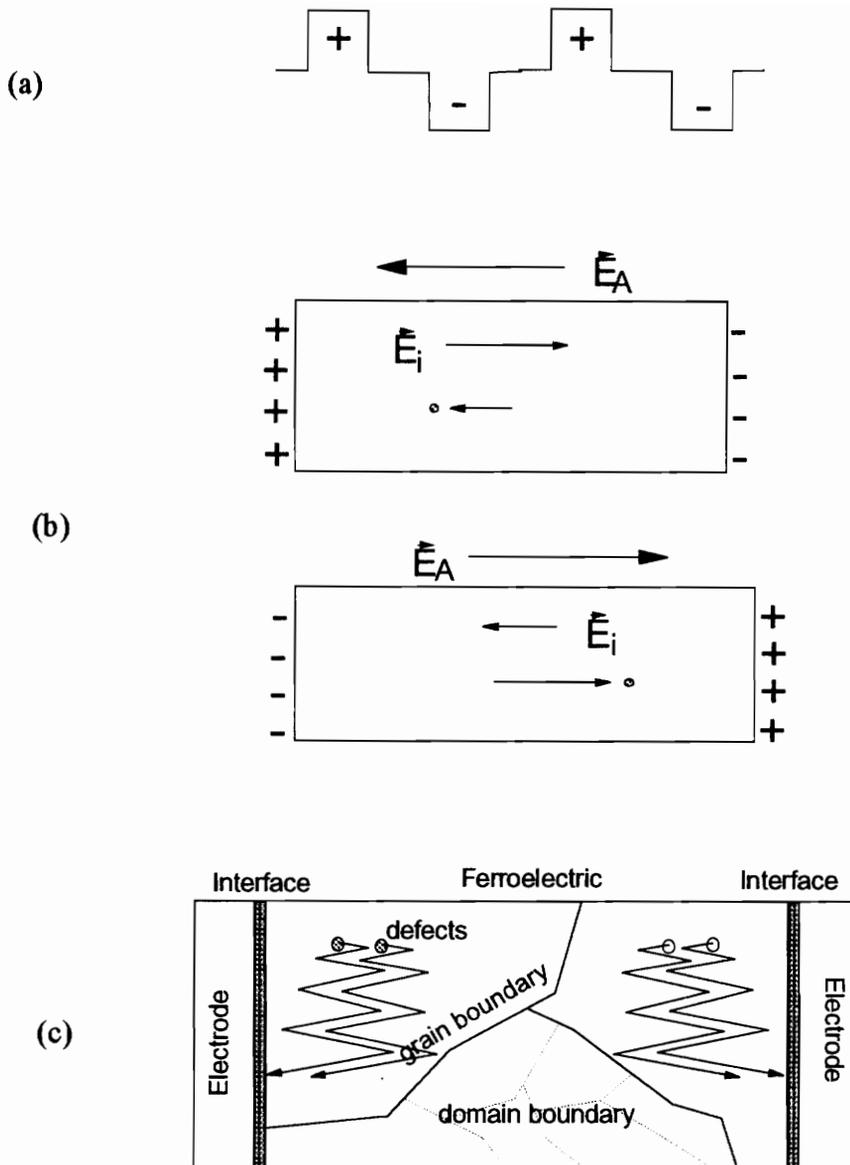


Figure13. Fatigue model: (a) input (voltage) stresses, (b) defect movement by local electric field, (c) effective unidirectional movement of defects under AC field.

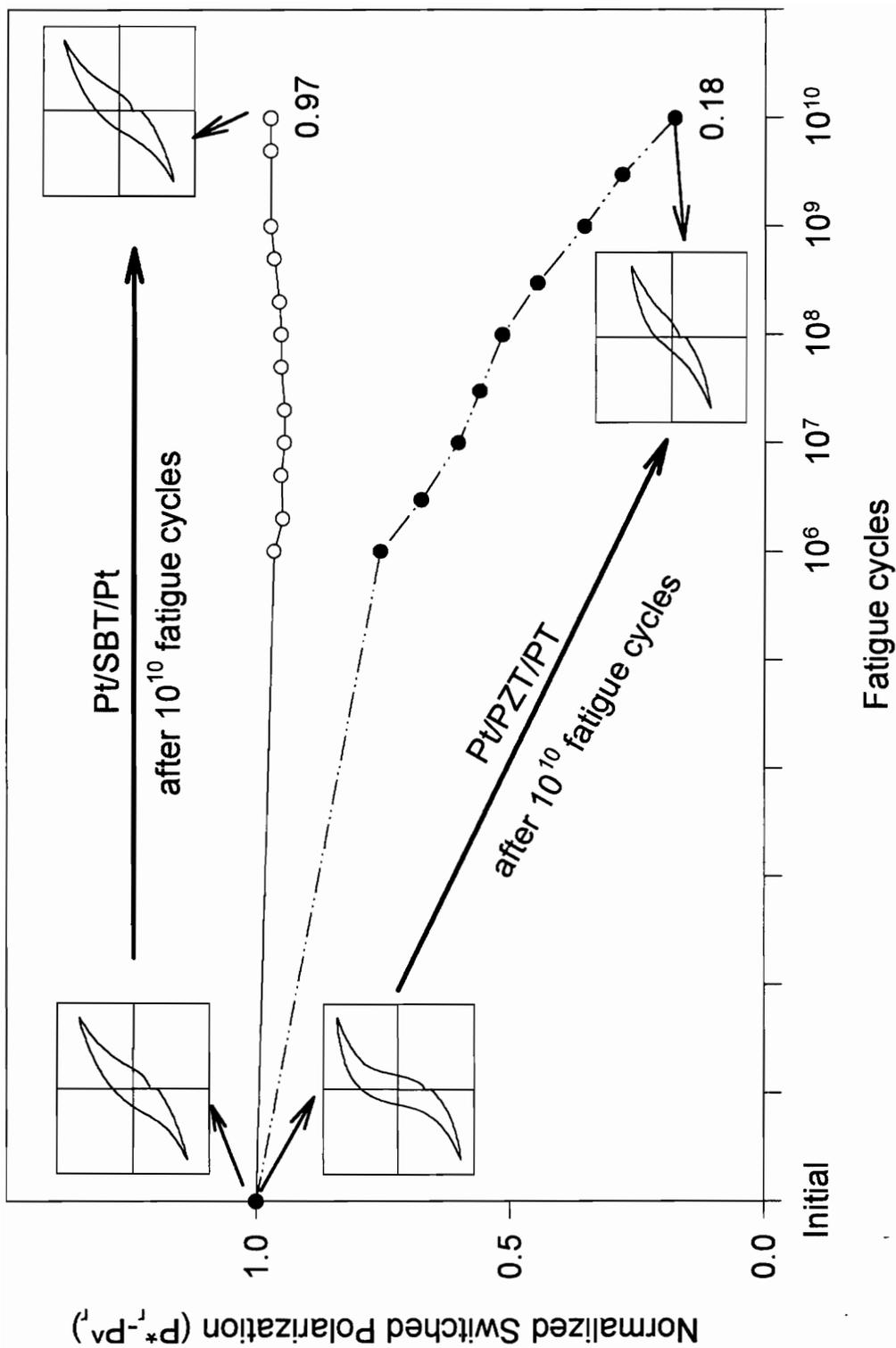


Figure 14. The fatigue spectrum comparison of PZT and SBT thin film capacitor captioned with their changes of hysteresis properties before and after fatigue.

performance as of 50% excess Bi). The applied voltage was 5V and frequency was 500 kHz. The fatigue profile was set as x-axis of Figure 14. The switched polarization (dPr) was plotted against the fatigue periods. Pt/PZT/Pt started fatiguing very early at $\sim 10^6$ cycles. On the other hand, all Pt/SBT/Pt with different excess Bi content performed well and were almost fatigue-free up to 10^{10} cycles. Because of the time consideration, 10^{10} cycles fatigue is the maximum time we used to test, but we believe that Pt/SBT/Pt should not degrade (fatigue) beyond 10^{10} cycles.

In the case of PZT, a processing temperature of at least 600°C is required to form the ferroelectric perovskite phase, which is responsible for polarization. However the PbO component begins evaporating at temperatures as low as 550°C, resulting in the formation of oxygen and lead vacancies. According to the discussed fatigue model, these oxygen or lead vacancies are the intrinsic defects entrapped in the Pt/PZT interface, which physically induces the polarization loss (fatigue). In the other case, SBT does not contain any volatile components in its sublattice responsible for the ferroelectric properties [7, 21]. Therefore, processing of SBT should not generate vacancies due to volatilization which is confirmed by the almost fatigue-free performance for all samples with various percentages of excess Bi. In fact, SBT was chosen based on the guidelines provided by the discussed fatigue model to minimize the degradation problem. If the relative movement of oxygen vacancies and their entrapment at the electrode-ferroelectric interface and/or at the domain boundaries and grain boundaries are the factors contributing to fatigue, then the possible solutions to overcome the problem include: reducing the tendency for defect entrapment by controlling the interface state and controlling the defect density. The first one has been achieved by using ceramic electrodes such as RuO₂ instead of conventional Pt metal electrodes for PZT thin films [20]. However, the leakage currents in RuO₂/PZT/RuO₂ capacitors are unacceptably high. The second option is to choose a ferroelectric material

that has high defect formation energies and/or material that does not contain any components which are volatile at the processing temperatures. A careful analysis of the fatigue model reveals that it is not presence of point defects in the lattice of the ferroelectric as a whole that is responsible for fatigue; it is only the formation of defects in the sublattice exhibiting ferroelectric properties that cause fatigue. Thus, another alternative is to use a material like SBTN, which has no volatile component in its ferroelectric sublattice. However, the reason for low fatigue of SBTN is not clearly known. Chapter 4 will discuss the likely inference of SBTN's low fatigue.

3.2.4 Experiment and result

There is sufficient experimental evidence to indicate that accumulation of oxygen vacancies at the Pt/PZT interfaces has a direct effect on the fatigue properties of Pt/PZT/Pt. Scott et al found that the oxygen concentration drop off near the electrodes after fatigue indicating increased accumulation of oxygen vacancies near the Pt/PZT interface [27]. Kwok and Desu found that the Pt/PZT/Pt films processed under a low partial pressure of oxygen in the processing ambient (i.e., higher oxygen vacancy concentration in the films showed a relatively higher rate of fatigue for a given number of cycles [28]. Another proof of oxygen vacancies pile-up at the fatigued Pt/PZT interface will be given in the following experiment. The objective of this experiment is to provide experimental evidence for the discussed fatigue model.

The equivalent capacitance (C_m) of Pt/PZT/Pt capacitor is composed of three capacitors in series: a capacitor representing the bulk material (C_B) and two representing the interfaces (C_i), as illustrated in the inset of Figure 15 (a). The capacitance value of the sample can be formulated as:

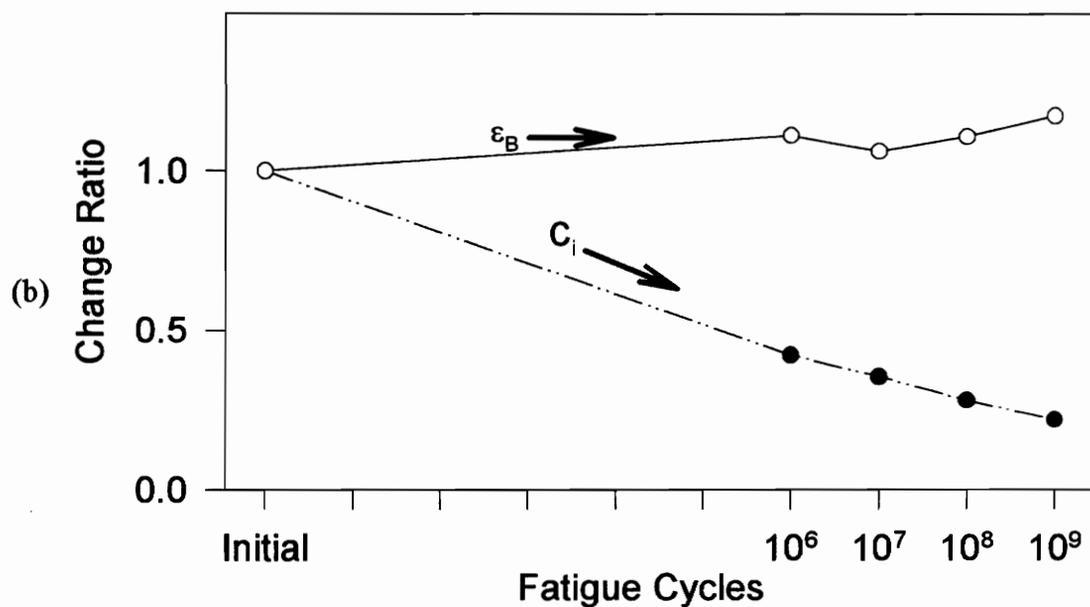
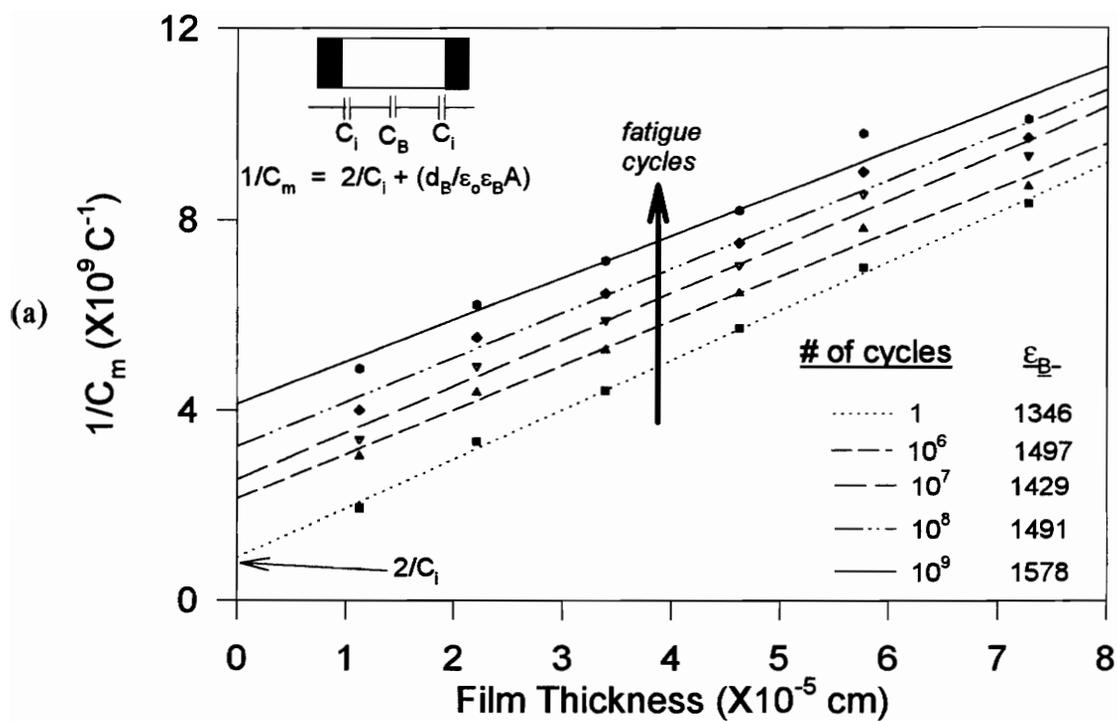


Figure 15. (a) Film thickness dependence of capacitance (C_m) for each fatigue cycle. (b) The change ratio comparison between C_i and ϵ_B .

$$\frac{1}{C_m} = \frac{1}{C_B} + \frac{2}{C_i}$$

$$\frac{d_m}{\epsilon_r \epsilon_0 A} = \frac{d_B}{\epsilon_B \epsilon_0 A} + \frac{2d_i}{\epsilon_i \epsilon_0 A}$$

where d_m and ϵ_r are total sample thickness and dielectric constant respectively; d_B and ϵ_B are bulk thickness and dielectric constant respectively; d_i and ϵ_i are interfacial layer thickness and dielectric constant respectively; ϵ_0 is the permittivity of free space; and A is the sample area. The interfacial layer thickness (d_i) has been estimated $\sim 200\text{\AA}$ [29], which is much thinner than the film thickness (d_m). Therefore, $d_B \approx d_m$ and the equation can be approximated by:

$$\frac{1}{C_m} = \frac{d_m}{\epsilon_B \epsilon_0 A} + \frac{2}{C_i}$$

Thus, a plot of $1/C_m$ versus d_m yields $2/C_i$ from the y-axis intercept and ϵ_B from the slope.

Pt/PZT/Pt samples were fabricated by MOD with six different films thicknesses (from 0.11 to 0.73 μm) while Pt/SBT/Pt with 0.21 μm thickness were fabricated by PLD. The fatigue tests were performed using RT66A system with frequency 500 kHz as mentioned in the previous section. Following each of the fatigue periods, low field dielectric properties were measured by using a multifrequency HP9192A impedance analyzer with an oscillation level of 50 mV and frequency of 10 kHz. Figure 15 (a) illustrates the thickness dependence of measured capacitance (C_m) of Pt/PZT/Pt samples. The plot provides the C_i value derived from intercept on the $1/C_m$ axis of extrapolation of each fatigue period line along with its corresponding ϵ_B . Hence, it can distinguish the factors of interfacial capacitance (C_i) and bulk dielectric constant (ϵ_B) for each period of fatigue cycling. The almost parallel lines among all the fatigue periods implied that ϵ_B was constant and C_i was decreasing as the fatigue progressed. The phenomenon is illustrated in Figure 15 (b), the change ratio of ϵ_B and C_i for the various fatigue periods.

The most probable candidate for the mobile defect in PZT is the oxygen vacancy. According to the discussed fatigue model, this oxygen vacancy can be entrapped at ferroelectric-electrode interfaces. Note that the oxygen vacancy concentration at ferroelectric-electrode interfaces for the fatigued PZT capacitor could be higher than that of the fresh sample. Interestingly, the observed data (ϵ_B constant, C_i decreasing) in this study also indicates that a higher concentration of oxygen vacancies was introduced at the Pt / PZT interfaces as the fatigue progressed.

By observing Figure 15 (a), the effective dielectric permittivity (ϵ_T) of Pt/PZT/Pt decreases with decreasing film thickness and with increasing fatigue cycles. Lee et al. found that the formation of a low ϵ_T Schottky depletion layer at the Pt/PZT contact lowers the effective ϵ_T for thin PZT films [30]. The Schottky depletion layer exhibited a lower ϵ_T due to the dielectric saturation and piezoelectric compression. The energy-band diagram of Pt/PZT/Pt capacitor shows band bending associated with the Schottky contacts, which induce a higher slope near the contacts and a lower slope near the bulk of the PZT film. For the energy-band diagram of fatigued PZT capacitors with Pt/PZT/Pt structure, higher concentration and higher total amount of oxygen vacancy can induce a deeper band bending and a higher effective interfacial layer thickness (d_j), respectively, at the Pt/PZT interfaces. The former results in a higher interfacial electric field and consequently a lower ϵ_T at the interfaces. These two effects (i.e., low ϵ_T and high d_j) keeps lowering the interfacial capacitance (C_i) and effective ϵ_T of the PZT capacitor as fatigue progresses.

In summary, more fatigue of a Pt/PZT/Pt capacitor resulted in a wider depletion width at the interface but the bulk dielectric permittivity was almost constant. Note that the internal electric field in the bulk PZT thin film is diminished as the oxygen vacancy moves toward the interfaces, explaining the slightly increase in ϵ_B with increasing fatigue period in Figure 15 (b).

For experiments similar to the Pt/PZT/Pt capacitor, a relative constant ϵ_r was determined as a function of fatigue cycles for Pt/SBT/Pt capacitors. Figure 16 provides the comparison of ϵ_r between Pt/PZT/Pt and Pt/SBT/Pt with the same film thickness as a function of fatigue cycles. The relative constant ϵ_r clearly indicates that oxygen vacancies do not accumulate at Pt/SBT interfaces during fatigue cycling. This could be due to the inherently low defect oxygen vacancy concentration in SBT crystal structure and/or the blocking of oxygen vacancies by Bi_2O_3 layers in the layered crystal structure from propagation during the course of fatigue. Band bending in band-diagram is not observed at the Pt/SBT Schottky contact due to the low defect concentration of SBT films. Therefore, no high-field induced low- ϵ_r interfacial layer was observed for these films.

3.3 Leakage current

It is anticipated that at least up to 1 Gbit DRAM design the traditional one transistor-one capacitor (1T-1C) cell structure will be used. In general, each new generation of DRAM offers a four-times increase in density, a three-times reduction in cell area and a 1.4 times reduction in minimum feature size [32]. However, the amount of charge stored on the capacitor must remain relatively constant for all designs in order to maintain a reasonable signal-to-noise ratio. Therefore, one of the challenges for developing ultra-dense DRAM is maintaining the minimum charge level on the capacitor despite the decreases in the cell area. In this respect, high dielectric materials, like ferroelectrics, offer a very promising solution. Although ferroelectric has a crucial fatigue problem, this endurance does not limit its usage as a DRAM capacitor film because of no polarization reversal switching of ferroelectric capacitor in DRAM operation, i.e. the P_{\max} at maximum applied voltage and P_r at zero voltage of ferroelectric capacitor are used as the logic states in DRAM. However, low leakage current is another limiting factor for

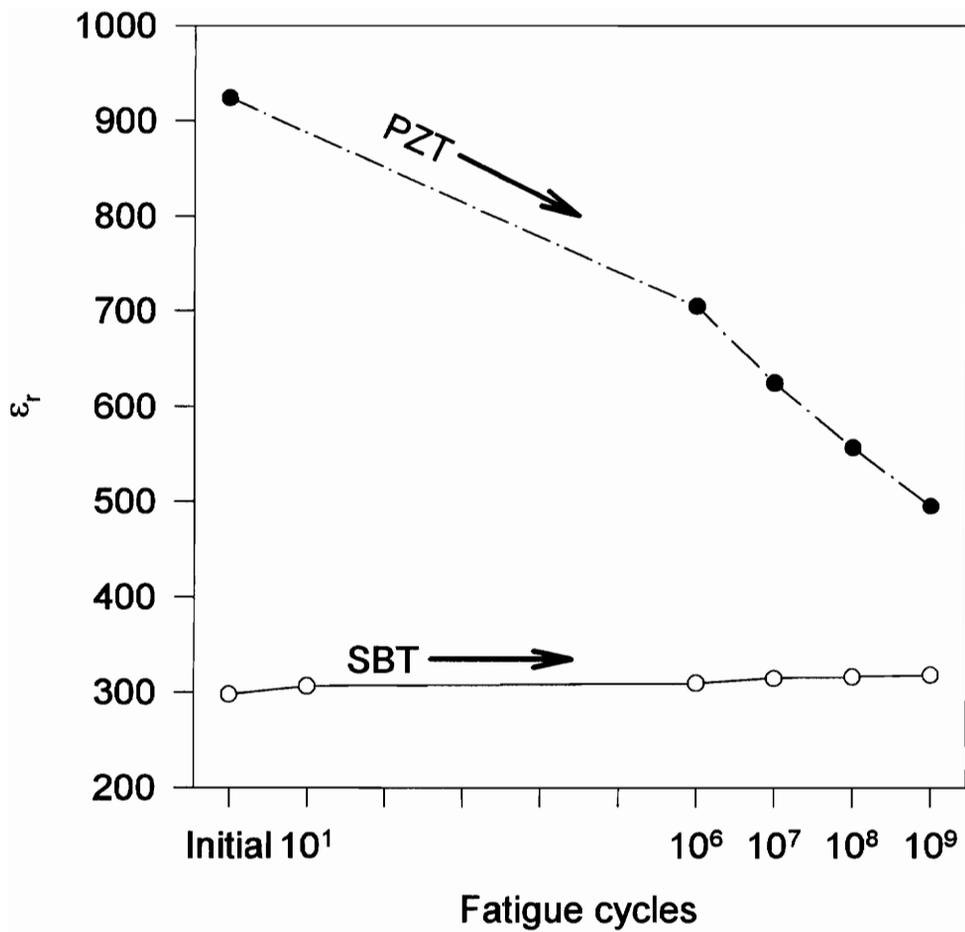


Figure 16. Dielectric constant vs fatigue cycles; decreasing in PZT films, almost constant in SBT films.

applications in DRAM. It has been estimated that 1 Gbit DRAM capacitor needs a minimum of $10 \mu\text{C}/\text{cm}^2$ charge storage density and a maximum of $5 \times 10^{-6} \text{ A}/\text{cm}^2$ [31].

Since the 1T-1C type of DRAM cell does not retain its stored charge in the "1" state, it must periodically be refreshed. This gradual loss of charge is typically due to the leakage current from the junction (field-induced or natural) in the silicon at the storage node. High leakage currents are deleterious to operation of DRAM since the cells require more frequent refreshing, use more power, and limit the maximum field that may be applied across the device. The memory cell is refreshed periodically at a time interval called the refresh time. The total leakage current of the cell must be low enough that the cell does not discharge and change its memory state between refreshes. A reasonable guideline is to allow a 20% degradation in the charged state.

3.3.1 DC Conductivity

When a DC field is applied to a dielectric material, the current relationship with time as well as the applied field is called DC conductivity. Charging current, switching current, leakage current, resistivity degradation and time dependent dielectric breakdown (TDDB) are all the issues in DC conductivity. These issues can be studied from the current response of a ferroelectric capacitor for an applied DC voltage, shown in Figure 17, as three regions in the time spectrum with possible conduction mechanism [32]. The three regions are transitory, steady state, and resistivity degradation and/or dielectric breakdown regions.

Three different types of current exist in this transitory time domain: (i) ferroelectric switching current which causes a switching current peak and is usually finished in about 100 ns or less; (ii) Electric charging current in measurement circuit; (iii) Electrical charge hopping and/or space charge polarization [33]. In this region, the current I after removal

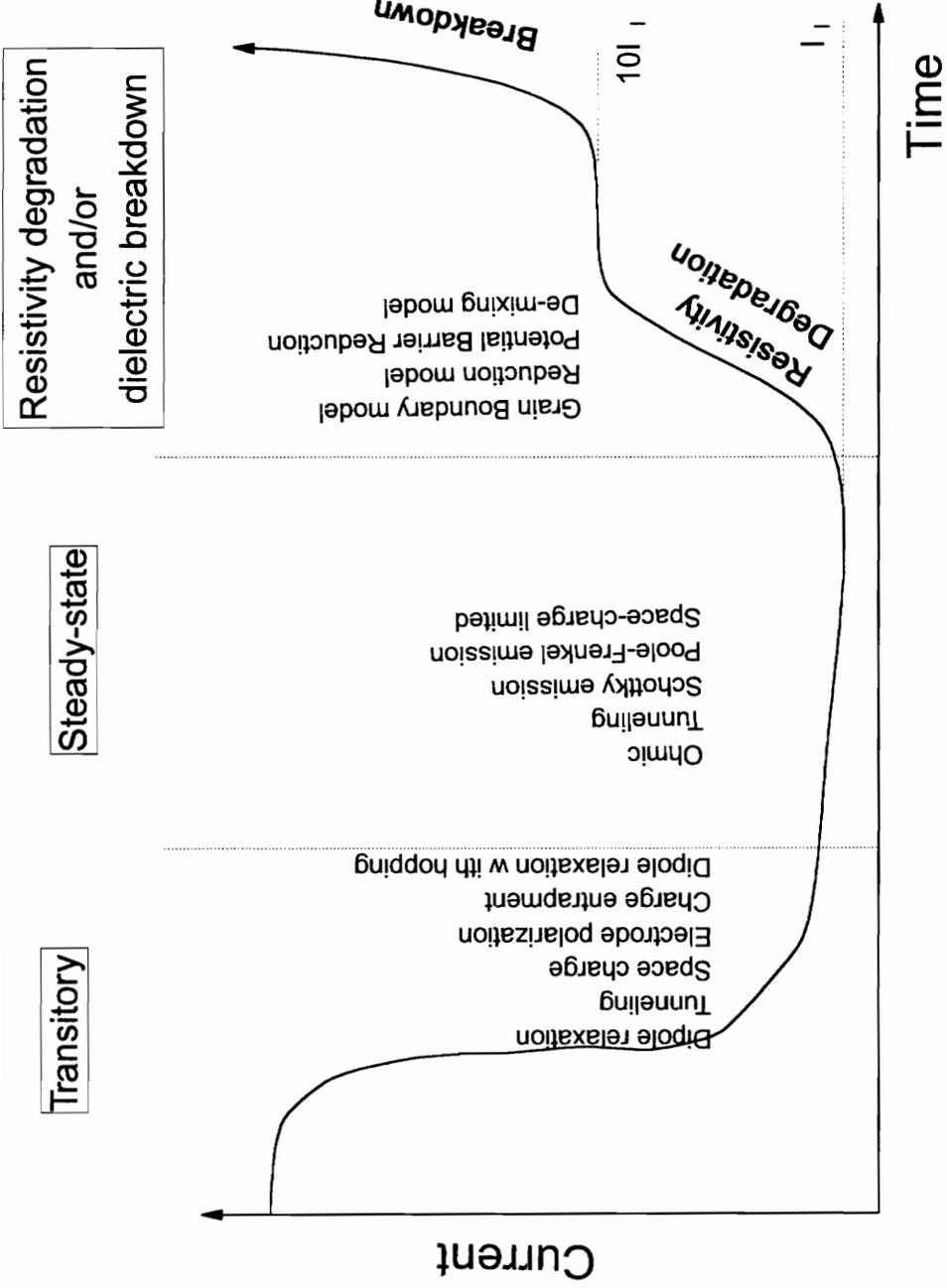


Figure 17. Current response of a ferroelectric capacitor on an applied DC voltage.

of the steady state current (leakage current) had been reported in terms of dielectric relaxation current ("Curie-von Schweidler law"): $I = I_0 t^{-\gamma}$. This current reflects an increase in time of the bound charge on the capacitor electrodes. This extra charge compensates for the gradual increase in time of the ferroelectric polarization at constant voltage. Electrical charge hopping with many-body interaction was used to explain this behavior [34].

In the steady state region, the measured current after stabilization represents true leakage current, flowing from one electrode of the ferroelectric capacitor to the other. This current must be electronic, otherwise, the electrical current would not be constant and non-zero because of the blocking by the electrode to charge carriers. The possible mechanism of leakage current for ferroelectric capacitors will be discussed later in this study.

When a voltage is applied for a period of time, the current begins to increase in the resistivity degradation and/or dielectric breakdown region, and this may or may not lead to dielectric breakdown. A gradual increase of leakage current after stabilization under an applied electric field stress is known as resistivity degradation. The dielectric breakdown, defined as time dependence dielectric breakdown (TDDB), however, is the abrupt increase of leakage current after stabilization and/or resistivity degradation. Many researchers, when investigating TDDB, establish a breakdown criterion, e.g. one or two orders of magnitude increase in current relative to the lowest current before the breakdown. In terms of mechanisms, resistivity degradation must be separated from TDDB. They are considered as two independent processes for the following reasons: (i) TDDB in ferroelectric films is usually destructive, i.e. it causes the film capacitor to short. However, resistivity degradation is non-destructive. After removing the high voltage, the leakage conductivity at low voltage is still small; (ii) Resistivity degradation does not necessarily lead to breakdown. TDDB can take place during resistivity degradation or before

establishment of the degradation. However, in terms of device failure, the two processes have the same consequence, i.e. excessive leakage. Since the resistivity degradation usually occurs earlier than TDDB, and it can also occur at very low voltages, it is likely to be more important than TDDB in determining the device reliability [35].

3.3.2 Leakage current measurement

The immediate implication of Figure 17 is that since the conduction mechanism of each region may be different, it is important to know in what region the current is measured during I-V measurement. It is suggested that one should measure I-t prior to I-V measurement to ensure that the current measured at the various voltages are in the same region. Special care must be taken to prevent at least two effects from interfering with the detecting of the true leakage current from I-t Curve of a ferroelectric capacitor. One is the polarization effect, which prevails at low electric fields before the polarization reaches saturation; the other is the resistivity degradation effect, which is particularly pronounced in thin films under high electric fields.

Ferroelectrics are highly polarizable materials whose polarization mainly consists of two parts in nature: ferroelectric and dielectric. Thus, there is a considerable amount of charging current through the measurement circuit when a voltage is applied to the specimen. To get the true leakage current, one usually has to collect readings from the I-t Curves after they reach steady states. Actually, ferroelectric polarization results from domain switching with itself would hardly be observable from the I-t Curve. The majority of the domain switching is completed in 1 ns to 1 μ s, and is much faster than the response time of the instruments used for conventional conductivity measurement. Therefore, one does not worry about the effect of ferroelectric polarization in regard to the time needed to read the steady-state current. Unlike ferroelectric polarization, dielectric polarization in

ferroelectric films is much slower, and thus the I-t responses take rather a long time to reach steady states. The differences between the initial transient current and steady-state current are significant. However, long-term readings do not give a better result in high voltage region, where resistivity degradation and/or TDDB comes into effect.

Considering all above facts, the leakage currents in the study were determined as follows:

- (i) conditioning the sample to a certain polarization state (the samples were measured their hysteresis by RT66A system prior to measurement in this study, i.e. top electrodes were negatively polarized).
- (ii) choosing the polarity of the top/bottom electrodes for applying the DC field (applying positive field to the top electrode was defined as "top-high" and to bottom electrode was defined as "top-low" in this study).
- (iii) measuring the I-V response from the I-t of each voltage step in programmable step mode and holding time (in this study, the low voltage segments measurement were programmed in a longer holding time but for high voltage segments were in a shorter holding time).

The DC electrical current was measured by using a Keithley 617 Programmable Electrometer with a built in voltage source. An IBM PC was employed to control the electrometer with a Turbo-C language program called "IVTHIN12" via IEEE 488 interface. The program IVTHIN12 is listed in the appendix of this thesis. The input source is a stair-like voltage with user-programmed flexible voltage steps and holding time (set with minimum and maximum time) for each voltage step. The other programmable parameters are the time-interval of measuring points (0.4s is the fastest time-interval for this system), the sample sizes for the calculation of standard deviation and the allowable relative standard deviation.

The current of each voltage step is measured at each measuring point. The time of current measurement for each voltage step is scheduled by at least "minimum time" and at most "maximum time". Statistical method is employed to decide termination of measurement of each voltage step. After collecting a number of measuring points (sample sizes) set by the user for each voltage step, the standard deviation of this group of data is calculated. This procedure is continuously taken for each consecutive group of data. After collecting data for the "minimum time" and before the "maximum time" of each voltage step, the standard deviation of each group of data is evaluated by the qualified bar decided by +/- setting relative standard deviation. When the standard deviation of last group of data lies within the qualified bar, the current measurement of each voltage is accomplished and the measurement skips to the next voltage step. In other words, the measured currents were stabilized and therefore are the "true" leakage currents. The average of the last group of data is taken as the leakage current of each voltage step. The program continues until the last voltage step. Then, I-V Curve can be obtained. The data of I-t at each voltage step and I-V are stored in two separate data files. The input and output of this program are demonstrated in Figure 18.

3.3.3 PZT vs SBT

Figure 19 plots the $\ln(J)-E^{1/2}$ Curve (J is the measured leakage current density and E is the applied DC electric field) from the I-V and leakage current measurement of RuO₂/PZT/RuO₂, Pt/PZT/Pt and Pt/SBT/Pt. The last two have applied DC field with positive polarity both on top (top-high) and bottom (top-low) electrodes of the samples. The leakage current measurement have followed the procedures mentioned in Section 3.3.2. The RuO₂/PZT/RuO₂ samples were measured to show the electrode effects on the leakage current of PZT thin film capacitor as compared to the Pt/PZT/Pt samples. The

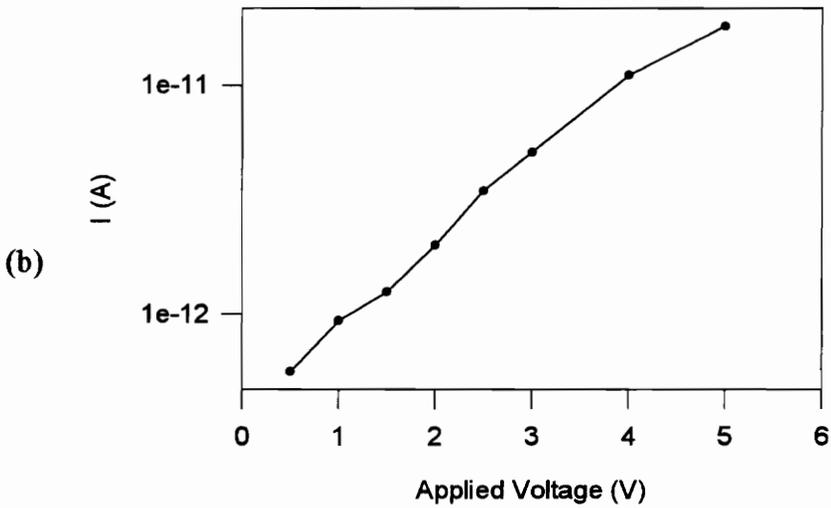
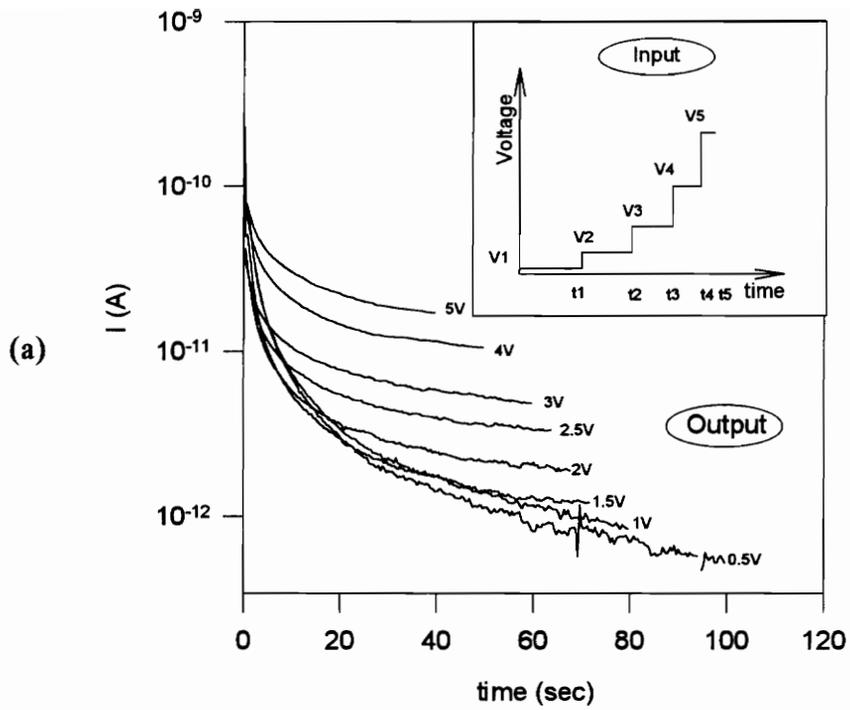


Figure 18. (a) Input of stair-step voltage (inset) and output response (I-t) for each voltage step. (b) I-V curve derived from the I-t data.

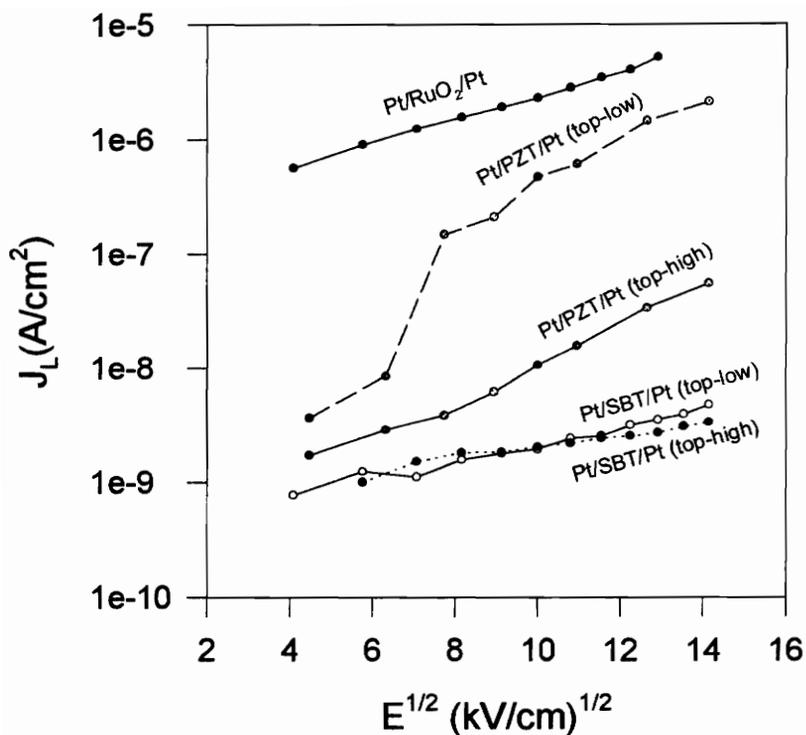


Figure 19. $\ln(J)-V^{1/2}$ relationship of Pt/PZT/Pt, $\text{RuO}_2/\text{PZT}/\text{RuO}_2$, and Pt/SBT/Pt.

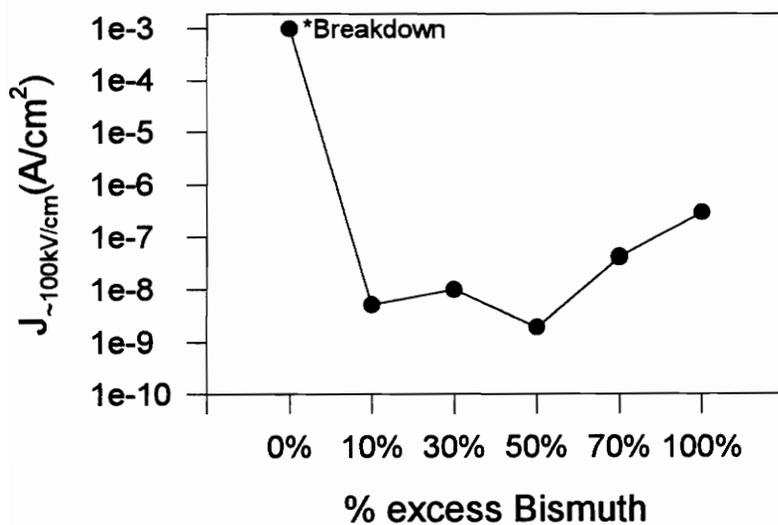


Figure 20. % excess bismuth dependence of Pt/SBT/Pt leakage current density at 100kV/cm applied field.

leakage current mechanism of ferroelectric thin film capacitors is discussed by comparing the leakage current of PZT and SBT samples.

There are several types of leakage current mechanisms in insulators. Ohmic behavior is observed at low fields. Under high electric fields, where devices exhibit non-ohmic characteristics, electrical behavior is governed by oxygen vacancy diffusion, space charge limited current (SCLC) injection, grain boundary potential barrier, tunneling, Schottky emission, or Poole-Frenkel emission. SCLC injection occurs under fields on the order of 1-10 kV/cm, and Schottky emission, under fields on the order of 0.1 MV/cm. Tunneling is observed under fields on the order of 100 MV/cm. I-V characteristics of ferroelectric capacitors did not show ionic type conduction at temperatures lower than 150°C. It is hard to believe that leakage current of ferroelectric capacitors is controlled by grain boundary potential barrier because there exists little chance for the thin film to form grains across electrodes as long as film thickness is of the order of thousand angstroms. Therefore, the likely leakage current mechanism may be Schottky emission or Poole-Frenkel emission. Schottky emission occurs at the insulator-electrode contact as a result of barrier lowering due to the applied field and the image force, i.e. interface-controlled. The latter is associated with field-enhanced thermal excitation of charge carriers from traps in the bulk, i.e. bulk-controlled. These two transport mechanisms are very similar. Both predict a I-V relationship of $J \sim \exp(E^{1/2})$, except that in the Poole-Frenkel mechanism the barrier lowering is twice as large as in the Schottky mechanism due to the fact that the positively charged trap in the Poole-Frenkel mechanism is immobile and the interaction between the electron and the charged trap is twice as large as the image force in the Schottky mechanism [36].

Both Pt/PZT/Pt and Pt/SBT/Pt I-V fit well with $\ln(J) \sim E^{1/2}$ relationship in Figure 19. Therefore, Schottky emission or Poole-Frenkel emission can be employed for their

leakage current mechanism. Since polarity dependence of leakage current is a strong indication of interface-controlled leakage, i.e. Schottky emission process, the asymmetric I-V of Pt/PZT/Pt samples in Figure 19 could conclude that their leakage mechanism attributes to Schottky emission. In another view, the leakage mechanism of Pt/SBT/Pt could attribute to the Poole-Frenkel emission due to their polarity independence of I-V. Another interface-controlled proof of Schottky mechanism in PZT capacitors is the significant different I-V between samples with RuO₂ electrodes and Pt electrodes. However, the high leakage in RuO₂/PZT/RuO₂ samples may be ascribed to conductive paths which are probably secondary phases (pyrochlore phase). The PZT films grown on RuO₂ electrodes always had a second non-ferroelectric phase [37].

In Figure 20, the leakage currents of SBT films with various excess Bi content are shown. Again, the 30% and 50% excess Bi samples perform better than others, the same performance as of their hysteresis properties. The higher leakage of 70% and 100% excess Bi samples are ascribed to the conductive paths in secondary phases, discussed in Section 3.1. The early breakdown of 0% excess Bi content is unknown. In another view, for the lower field leakage currents, the 0% excess Bi content samples have higher leakage currents. It seems that the increase of films grain size and compact density by the increase of % excess Bi might be the reasons that 50% excess Bi samples have the lowest leakage currents.

3.4 Retention and imprint

There is little consistency in the literature on the imprint measurement procedure. In this study, a simple characterization technique which consists of four measurement pulses to differentiate the retention and imprint effects is demonstrated. Thus, a

quantitative imprinted charge can be obtained. The retention and imprint properties of bismuth-layered ferroelectric thin films are also reported for the first time. Additionally, probable retention and imprint mechanisms are proposed on the basis of the observed data.

3.4.1 Definition and characterization

In order to make accurate retention and imprint measurements, one must define these two effects. The discontinuity in a hysteresis loop in Figure 21 (a) at zero voltage is due to the designed waiting period and where retention and imprint take place. The retention, imprint and retained charge are defined as:

- **Retention:** Loss of polarization with time after write. The magnitude of the polarization loss is state independent.
- **Imprint:** The increase in rate of retention loss in one state and decrease in the other for an imprinted capacitor. In other words, there is a preferred polarization state, leading to misreading of the stored data, by applying an external imprint stress on a poled capacitor.
- **Retained charge:** The polarization difference between state "1" and "0" with time after write. This charge is determined by both retention and imprint effects.

The defined items illustrated in Figure 21 (a) are elucidated as follows. $\overline{\Delta 1}$ and $\overline{\Delta 0}$ are vectors of polarization loss, $\overline{\Delta 1}$ being a negative vector and $\overline{\Delta 0}$ a positive one. The magnitudes of $\overline{\Delta 1}$ and $\overline{\Delta 0}$ are determined by both imprint and retention effects on ferroelectrics. The polarization losses at the two "stable" states due to retention effects (R) have the same magnitude but opposite directions, i.e., both losses point to the center of the hysteresis loop. The polarization loss (or gain) in states "1" and "0" due to imprint, however, are only in one direction and their corresponding magnitudes (I_1 and I_0) could

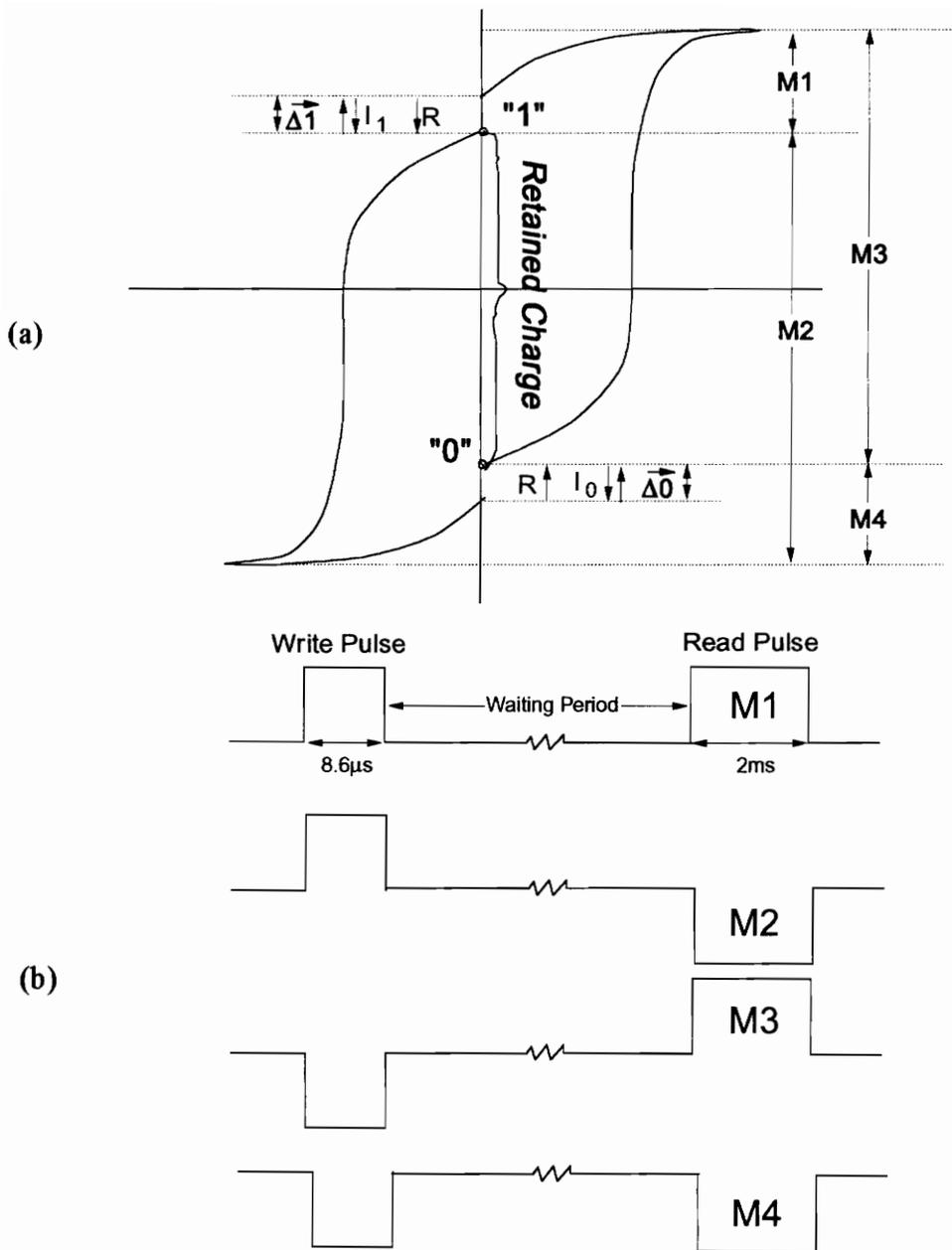


Figure 21 (a) A typical hysteresis loop with defined characterization parameters; the discontinuity at 0V is due to the designed waiting period where the retention and imprint processes take place.

(b) Four characterization pulses for the measurement of $M1$, $M2$, $M3$ and $M4$.

be different. If the magnitudes of I_1 and I_0 are equal, the effective retained charge is only determined by the retention.

M1, M2, M3 and M4 represent charges at different parts of the hysteresis loop. The magnitude of the retained charge equals $0.5[(M2 - M4) + (M3 - M1)]$, while the magnitude of imprinted charge ($|\overline{\Delta 1} + \overline{\Delta 0}|$) equals $0.5[(M2 - M1) - (M3 - M4)]$. Therefore, the retained and imprinted charges can be characterized by measurement of M1, M2, M3 and M4. Since the polarization loss due to retention can be obtained only if I_1 equals I_0 , pre-imprinted samples with $I_1 = I_0 = 0$ were chosen in this study to characterize the polarization loss due to retention. These samples also prevent the *process induced imprint effect* [38] that the fresh sample has the same imprint effect due to the improper process on the integration of ferroelectric capacitors. Usually, ferroelectric capacitors with symmetric hysteresis loops fulfill the requirement of $I_1 = I_0 = 0$ as discussed later.

Figure 21 (b) illustrates the characterization pulses for the measurement of M1, M2, M3 and M4. The RT66A system was used to perform these four measurements. However, its non-flexible system design is limiting the measurement ability. The delay time between write / read pulses must be longer than one second, thus no information on polarization loss within one second after write can be obtained. The writing and reading times in Figure 21 (b) were maintained at $8.6 \mu\text{s}$ and 2 ms , respectively. The capacitor was DC shorted after writing.

3.4.2 Experiments

Ferroelectric thin films with compositions of PZT and SBT were deposited by either the MOD or PLD. The substrates for the ferroelectric thin films were Pt/Ti/SiO₂/Si, RuO₂/SiO₂/Si and Pt(100)/MgO(100). The thicknesses of PZT and SBT thin films were

0.33 μm and 0.20~0.25 μm , respectively. *C*-axis oriented SBT films were deposited onto Pt(100) / MgO(100) substrates.

The absolute retained charge in a ferroelectric capacitor is the amount of polarization available for a memory circuit to detect (noise margin); it must be high enough to differentiate the states "1" and "0". In order to compare the retention properties for different capacitors, the normalized retained charge is presented. The normalized value is obtained by dividing the retained charge using the initial $2P_T$ value, measured from the Sawyer-Tower circuit for each capacitor. Figure 22 illustrates the time dependence of normalized retained charge for ferroelectric capacitors with structures of Pt/PZT/Pt (MOD), RuO₂/PZT/RuO₂ (MOD), Pt/SBT/Pt (PLD), Pt/SBT/Pt (MOD) and Pt/SBT/Pt/MgO (PLD). All samples show a dramatic drop in retained charge within the first second after writing and relatively constant retained charge thereafter. The PZT thin film with Pt electrodes showed the worst (~55% drop) retention while the *c*-axis oriented SBT thin film on Pt(100)/MgO(100) exhibited only an ~18% drop in retained charge. In general, the layered ferroelectric capacitors exhibit better retention properties than perovskite PZT capacitors.

SBT films prepared by MOD were selected for the imprint study. Figure 23 illustrates the retention and imprint properties of a Pt/SBT/Pt capacitor. The capacitor was written by a +5V pulse (8.6 μs) and then imprinted by a thermal stress of 100 °C for 100 minutes. The time dependence of retained charge for the imprinted capacitor was similar to that of the fresh capacitor as shown in Figure 23 (a). The individual polarization loss in the two memory states (i.e., $\overline{\Delta 1}$ and $\overline{\Delta 0}$) was derived by following equations:

$$(3.1) \quad \overline{\Delta 0} + \overline{\Delta 1} = \frac{1}{2} [(M2 - M1) - (M3 - M4)]$$

$$(3.2) \quad \overline{\Delta 0} - \overline{\Delta 1} = 2 P_r - \frac{1}{2} [(M2 - M4) + (M3 - M1)]$$

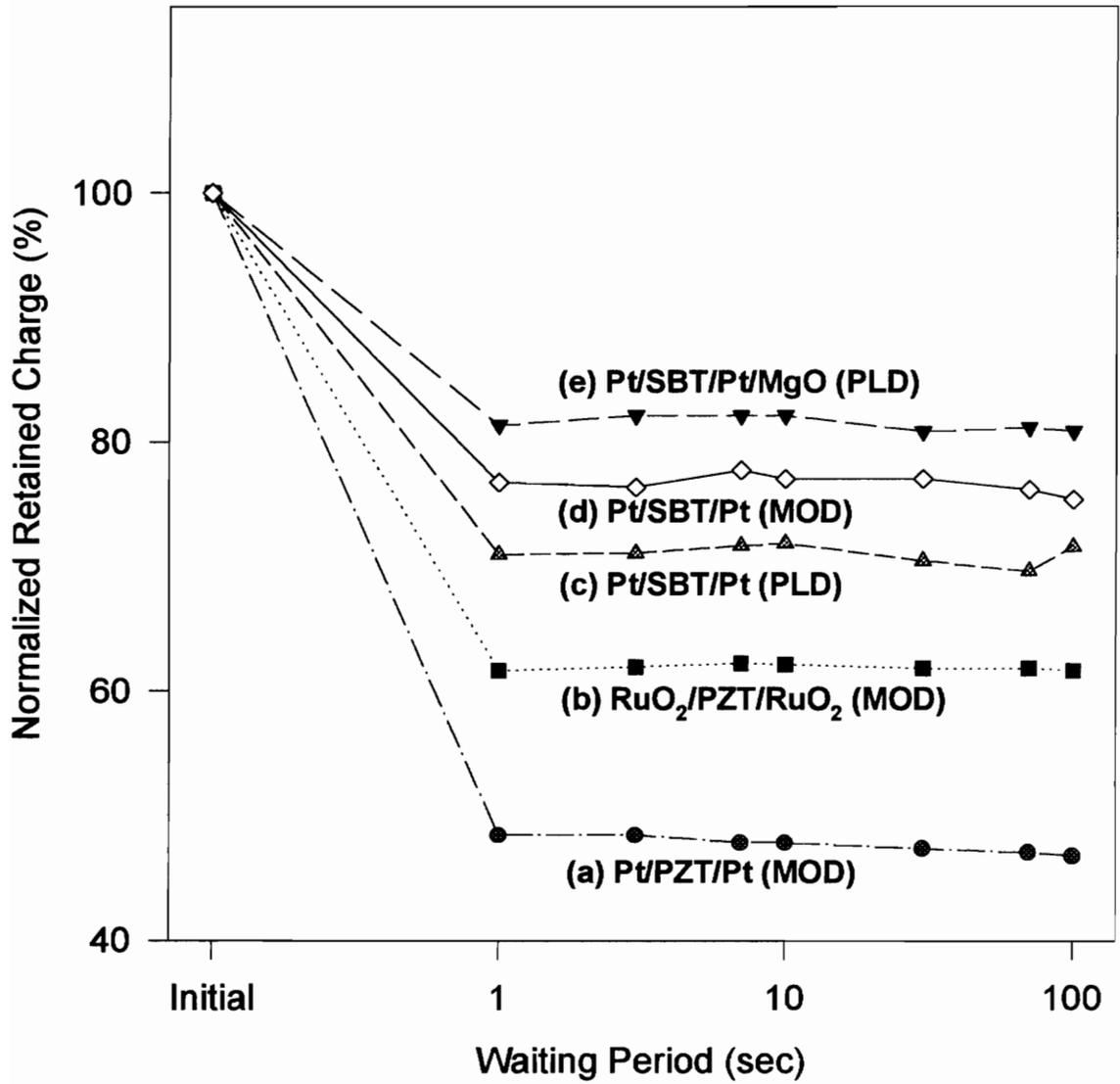


Figure 22. Time dependent retention properties on capacitors with structure: (a) Pt/PZT/Pt (MOD), (b) RuO₂/PZT/RuO₂ (MOD), (c) Pt/SBT/Pt (PLD), (d) Pt/SBT/Pt (MOD) and (e) Pt/SBT/Pt/MgO (PLD).

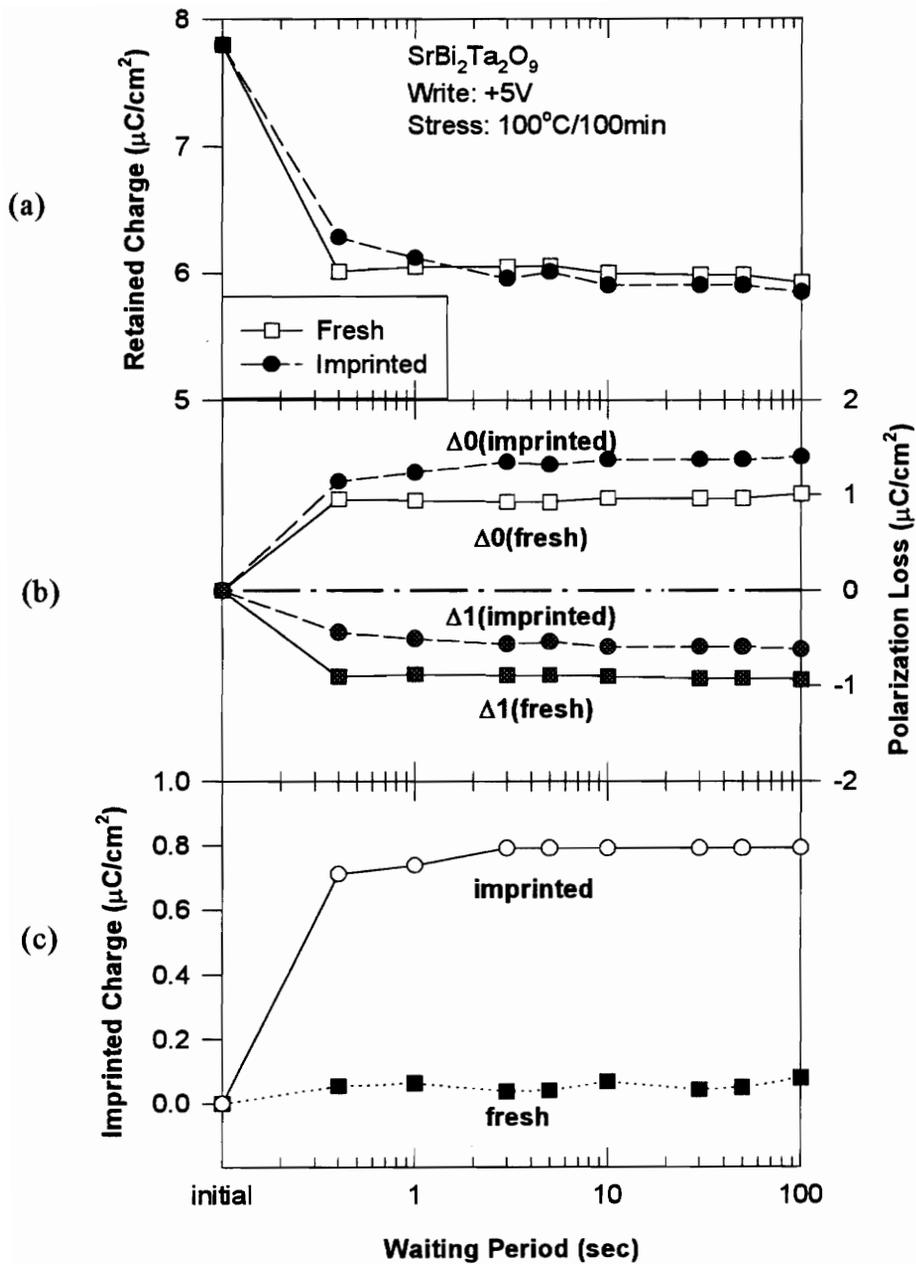


Figure 23. Time dependent (a) retained charge, (b) polarization loss, and (c) imprinted charge on fresh and imprinted (write: +5V, stress: 100°C/100min) SBT capacitors.

Figure 23 (b) shows that the polarization losses of fresh sample in both states (i.e., $\Delta 1$ and $\Delta 0$) are similar ($\sim 0.9 \mu\text{C}/\text{cm}^2$), whereas the polarization loss of imprinted sample in state "0" ($\Delta 0 \approx 1.35 \mu\text{C}/\text{cm}^2$) is higher than that in state "1" ($\Delta 1 \approx 0.58 \mu\text{C}/\text{cm}^2$). The imprinted charge was calculated by $\overline{\Delta 1} + \overline{\Delta 0} = \Delta 0 - \Delta 1 = I_1 + I_0 \approx 0.8 \mu\text{C}/\text{cm}^2$ [Fig. 23 (c)]. Since $I_1 \approx I_0 \approx 0$ for the fresh sample, the net polarization loss is attributed solely to retention effect. Since $I_1 \approx 0.32$ and $I_0 \approx 0.45 \mu\text{C}/\text{cm}^2$ for the imprinted sample, both retention and imprint contributed to the polarization loss. As in the case of retention, the polarization decay due to imprint is a fast process (< 1 sec).

Interestingly, the imprint process also changes the symmetry of the hysteresis loops [Fig. 24 (a)]. The hysteresis loop is measured using a continuous triangular signal where no delay is allowed between two measurement points, excepting the starting point. Therefore, no polarization loss due to retention and imprint can be observed in the course of continuous hysteresis loop measurement. The discontinuity between the starting and ending points is due to the one second delay after the capacitor is polarized to the negative state. The observed asymmetric hysteresis loop of the imprinted capacitor indicates that the imprint process builds up an internal bias within the ferroelectric thin film.

The polarization losses due to retention and imprint effects for the samples with same imprint stress (100 °C for 100 minutes) but opposite writing condition (-5V pulse for 8.6 μs) are shown in Figure 25. As expected, the polarization loss of imprinted sample in state "0" ($\Delta 0$) is lower than that in state "1" ($\Delta 1$). The imprinted charge of $0.9 \mu\text{C}/\text{cm}^2$ [Fig. 25 (c)] is almost the same as of the previous case in the opposite direction. Figure 24 (b) illustrates that the hysteresis loop of this imprinted capacitor shifts to the "positive" direction, opposite with Figure 24 (a).

Figure 26 shows the imprint tests on SBT films with various voltage stresses, i.e., unipolar pulses and bipolar pulses (fatigue). The fatigued sample ($\pm 5\text{V}$, 10^9 cycles)

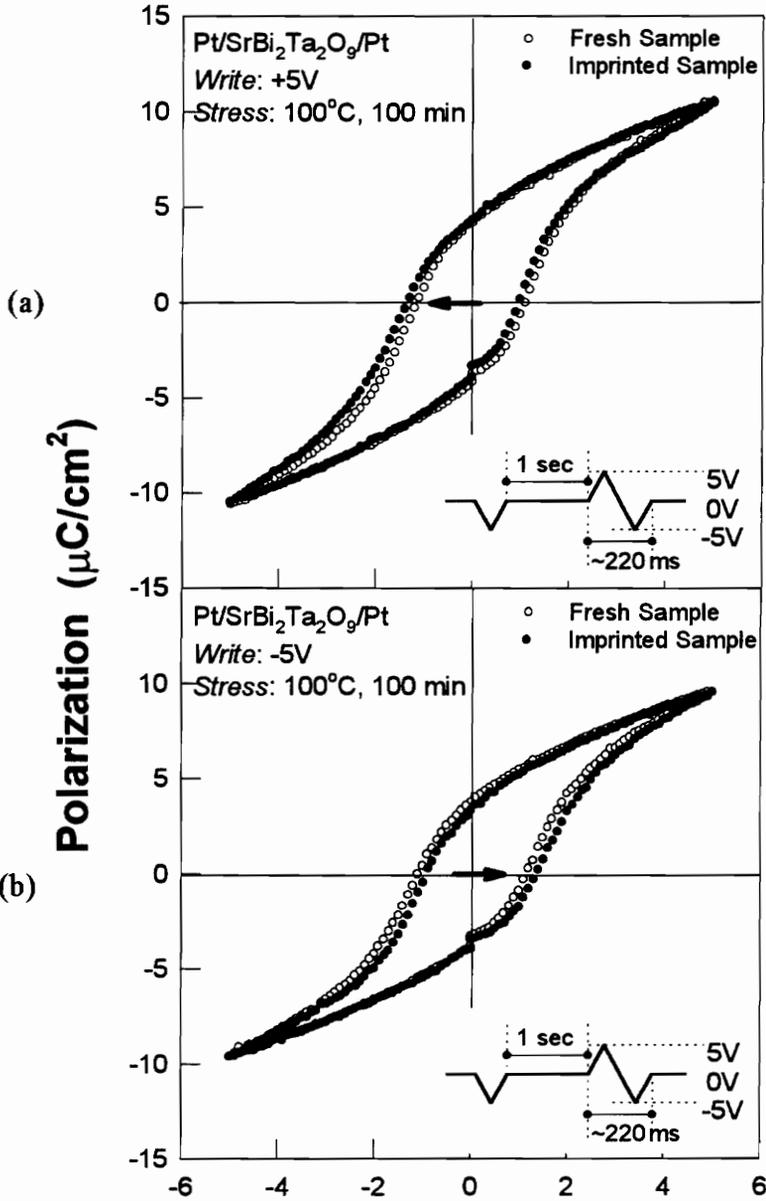


Figure 24. The hysteresis loop shifts (a) to "negative" for an imprinted (write: +5V, stress: 100°C/100min) SBT capacitor; (b) to "positive" for an imprinted (write: -5V, stress: 100°C/100min) SBT capacitor.

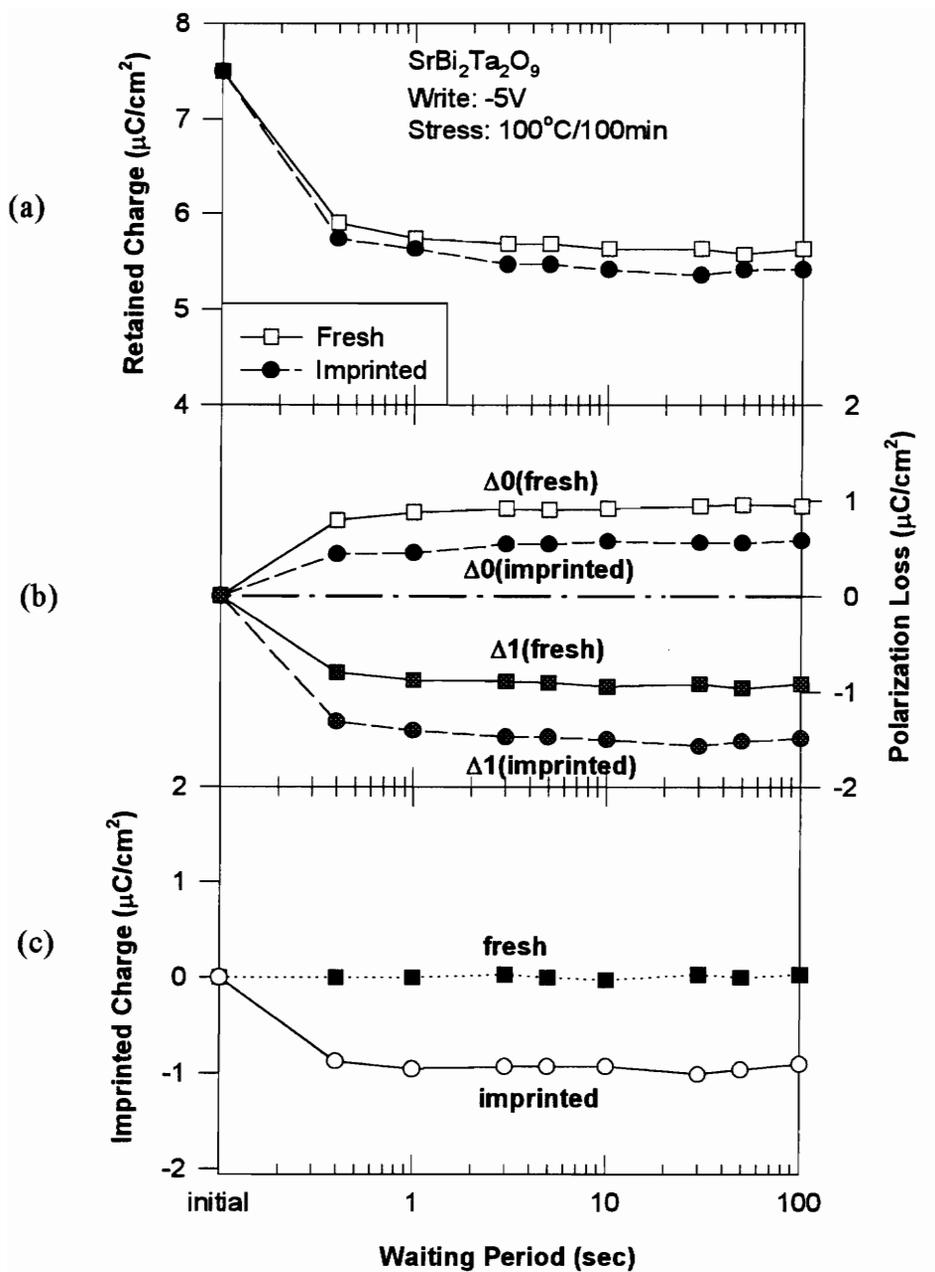


Figure 25. Time dependent (a) retained charge, (b) polarization loss, and (c) imprinted charge on fresh and imprinted (write: -5V, stress: 100°C/100min) SBT capacitors.

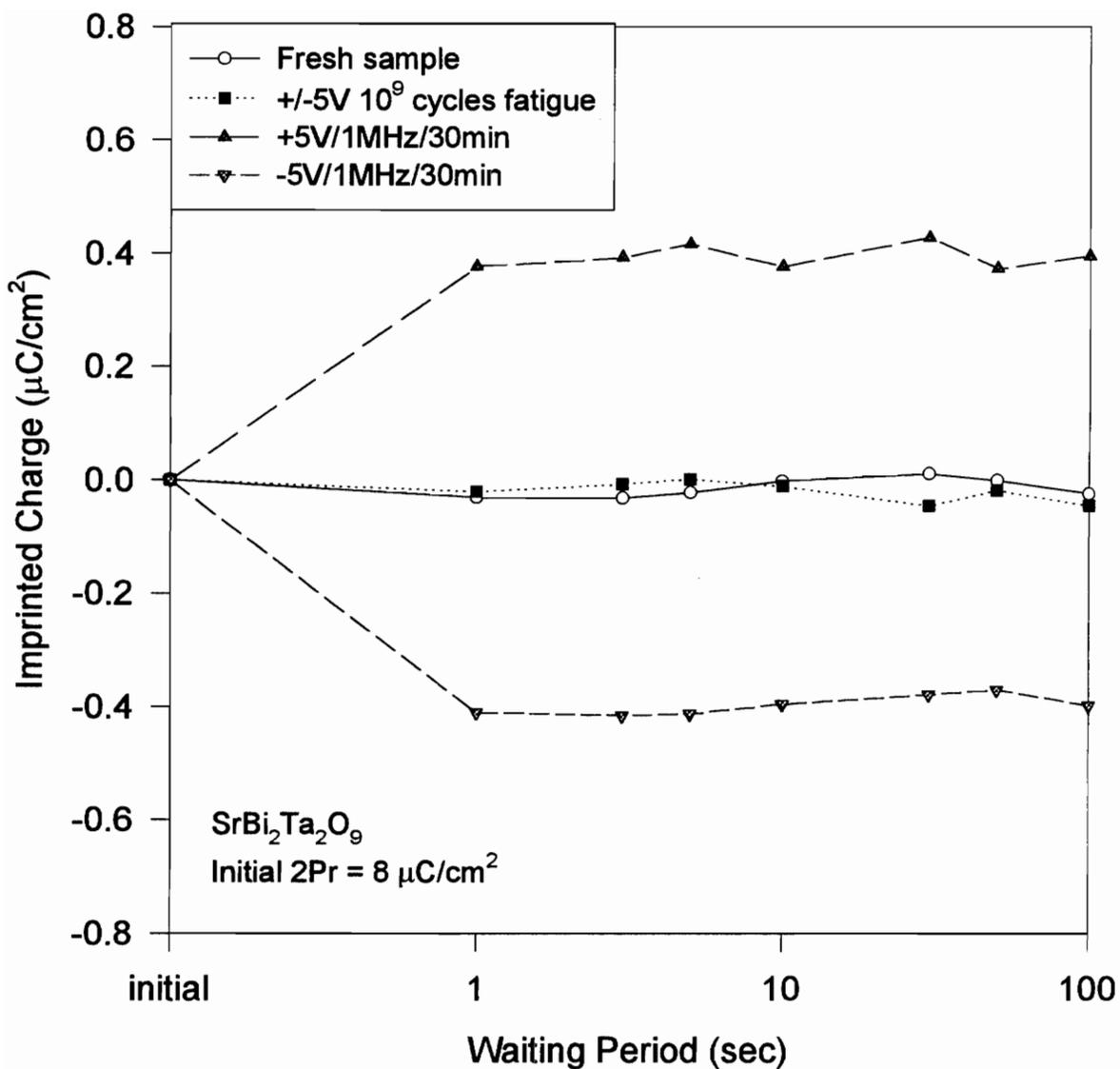


Figure 26. Time dependent imprinted charges of SBT capacitors with various stresses of bipolar pulses (fatigue) and unipolar pulses.

showed no imprinted charge buildup during the bipolar stress test. However, the positive and negative unipolar pulses (1 MHz, 30 minutes), simulating read pulses on the same logic state, result in the imprinted charge ($\sim 0.4 \mu\text{C}/\text{cm}^2$) in the positive and negative directions, respectively. Similarly, the positive and negative unipolar pulses also induce the shift of hysteresis loops in the negative and positive directions, respectively.

3.4.3 Retention mechanism

The ferroelectric retention problem is the loss of polarization as a function of time from a given poled state. Depolarization fields generated by the surface space-charge as well as ferroelastic effects have been proposed as mechanisms for this polarization loss. For the short-circuit condition during the retention test, the compensation charge in electrodes is such that the polarization charge is not completely canceled. This results in a nonvanishing electric field inside the ferroelectric that is opposite to the polarization. In the ideal case, where only electrode space-charge is considered, Mehta et. al. [49] calculated the depolarization field as:

$$E_{dep} = -\frac{P}{\epsilon_f} \left(\frac{2\epsilon_f / \ell}{2\epsilon_f / \ell + \epsilon_e / \ell_s} \right)$$

where P is polarization, ϵ_f and ϵ_e are the dielectric permittivity of ferroelectric and electrode, respectively, ℓ is the ferroelectric film thickness, and ℓ_s is the screening length characterized by the space-charge extent in the electrode. In the limit as $\ell \rightarrow \infty$ or $\ell_s \rightarrow 0$, the depolarization field vanishes. Therefore, very thin ferroelectrics coupled with long electrode screening lengths result in significant depolarization fields.

For a non-ideal case where a space-charge layer exists between the electrode and ferroelectric, this space-charge layer leads to the formation of a stronger depolarization field in the ferroelectric capacitor [39]. This is due to the charge defects (e.g., electrons,

holes, or ions) within the ferroelectric screen the spontaneous polarization and result in increasing the screening length ℓ_S . The space-charge layer between the electrode and PZT thin film consists of oxygen vacancies. These oxygen vacancies screen the spontaneous polarization internally and, therefore, ℓ_S in PZT capacitors should extend into the PZT film, i.e., ℓ_S is longer than the ideal case. Since fatigue-free SBT thin film implies a much lower space charge concentration within the film, no space-charge layer exists between the Pt and SBT film as discussed in fatigue section. Hence, an ideal ℓ_S could be used for capacitors with Pt/SBT/Pt structure. In short, higher depolarization fields are observed in PZT capacitors due to their higher oxygen vacancies and longer ℓ_S .

Ferroelastic effect is the behavior of domain reorientation in order to relax the internal strains. This effect can be observed in tetragonal crystal structures through 90° domains and observed in orthorhombic and rhombohedral structures through 90° and 60° , and 70.5° domains, respectively. This is due to the lattice distortion occurring during the reversal of 90° , 60° , and 70.5° domains. For the case of 180° domains, no lattice distortion is observed when the polarization direction is switched by 180° . Upon removal of the electric field, all 180° domains remain in their newly switched, stable positions. Hence, films with only 180° domains that are non-ferroelastic could reduce retention problems.

For a parallel-plate thin-film capacitor with a bismuth-layered ferroelectric, the domain wall movements for the a -axis and c -axis oriented thin films are different during reversal of the electric field. For an a -axis oriented thin film, the perovskite-like layers are perpendicular to the substrate and consist of 90° (i.e., a - a) and 180° domain walls that can move during the electric field reversal. The 90° and 180° domain walls are inclined at 45° and 90° to the substrate, respectively. In contrast, the c -axis oriented thin film has the perovskite-like layers parallel to the substrate and contains only moveable 180° domain

walls. These domain walls are parallel to the c -axis and perpendicular to the substrate. Based on the above analysis, the c -axis preferred oriented SBT thin films have the highest concentration of 180° domain walls and should have the best retention. The data indeed indicate that the c -axis preferred oriented SBT thin film on Pt(100)/MgO(100) exhibit better retention properties than random oriented SBT thin films on polycrystalline Pt electrodes (Pt/SBT/Pt). In summary, a preferred oriented ferroelectric thin film with only moveable 180° domain walls coupled with low concentration of space charge should have the best retention properties.

3.4.4 Imprint mechanism

Mihara et. al. [40] proposed that the rotation of new 90° domains at high temperatures as well as internal fields caused by charge trapping in the space charge layers are the imprint mechanisms. However, higher values of remanant polarization in hysteresis loops due to newly activated 90° domains have not been observed for the imprinted capacitor; therefore, it appears that internal field buildup by charge trapping in the space charge layer is the only possible imprint mechanism. Usually, the positive and negative mobile charges are drifting parallel and antiparallel, respectively, to the polarization direction, thereby building an internal field that opposes the polarization field. Consequently, the shift of hysteresis loop towards the positive or negative directions are expected. The conflicting data observed in Figures 24 (a) and (b), however, indicate that the explanation of charge movement as well as the charge trapping have to be modified.

For an ideal parallel-plate ferroelectric capacitor, the screening of spontaneous polarization at the surface of the ferroelectric is usually achieved by the charge within the electrodes. However, the screening can be internal for a non-ideal ferroelectric that contains free electrons, holes or ions. In fact, the internal screening of the spontaneous

polarization is thermodynamically favorable [39]. Before the imprint stress, these mobile charges could only affect the screen process slightly. This will not result in any effective internal field because they are reversibly following the electric field. Upon poling the ferroelectric in one direction and stressing it at high temperature for some time, however, these mobile charge move to the surface and become permanently trapped. Now these charges are partially screening the spontaneous polarization and thus result in an internal field which has the same direction as the poling direction. This explains the shift of hysteresis loop towards the "negative" or "positive" direction in Figure 24. Additionally, the internal field results in a preferential state wherein the polarization loss with time is smaller than in another state.

CHAPTER 4

Electrical Characterizations (II): Complex Impedance

4.1 Background

It is well understood that space charges are the source of fatigue. It is believed that the fatigue of PZT-based thin films is due to space charge accumulation and resorption at electrode-ferroelectric interfaces as mentioned in Section 3.2. The fatigue model in Section 3.2 is based on effective one-directional movement of defects due to asymmetric polarization under alternating pulses, and defect entrapment at the electrode-ferroelectric interface (and/or grain and domain boundaries). The entrapment of defects creates space charges at the electrode-ferroelectric interface. In this case the defects were oxygen vacancies.

Another class of materials, layered bismuth oxides with perovskite-like structure, have been identified as fatigue free materials showing almost no change (less than 5%) in remanant polarization up to 10^{12} switching cycles. However, it is still unknown why bismuth layered oxide materials have high resistance to fatigue. In order to understand the fatigue characteristics of bismuth layered oxides, the fatigue model in this study is assumed to be based on the movement of oxygen vacancies and is evaluated by the ionic conductivity of the materials. Also, the absolute value of the ionic conductivity is required for an understanding of the process of resistivity degradation. The newly introduced impedance spectroscopy is applied to obtain the ionic conductivity of the materials.

The use of complex impedance for the analysis of electrochemical reactions was introduced by Sluyters [41]. This method has subsequently found many applications. The

complex impedance presentation represents the most basic form of information about the dielectric properties of a substance and they form the basis of most interpretational analysis of experimental data, i.e. the presence of inhomogeneities in separate regions characterized by different dielectric properties. As pointed out by Bauerle [42], this technique allows the separation of several contributions to the total cell impedance, arising from bulk conduction and interfacial phenomena, as polarization effects at the electrode-electrolyte interfaces.

The successful separation of intergranular from bulk phenomena depends ultimately on the choice of an appropriate equivalent circuit to represent the electrolyte properties. Armstrong et al.[43] have used model equivalent circuits in complex impedance plane to simulate the effects of blocking electrodes, grain boundaries, etc., and have shown that this method of circuit analysis can be applied to practical systems. There are several models, some examples are illustrated in Figure 27. In these models, the terms blocking, non-blocking and absorption have to be defined. These terms are applied to electrodes and they describe the degree to which the mobile ions in the electrolyte can penetrate the electrode material. A completely blocking electrode is one in which no penetration of the mobile ions can occur. An example of a blocking situation is that of platinum electrodes on PZT. In this case, the mobile oxygen anion vacancies in PZT cannot cross the electrode-ferroelectric interfaces. The equivalent circuit and predicted complex impedance plane of this case are illustrated as Figure 27 (a), where C_g is a geometric capacitance of electrolyte, R_b is its bulk resistance, ω_1^* is equal to $(R_b C_g)^{-1}$, and C_{dl} is the capacitance which arises from the effect of mobile ions blocked by electrodes at electrode-electrolyte interfaces.

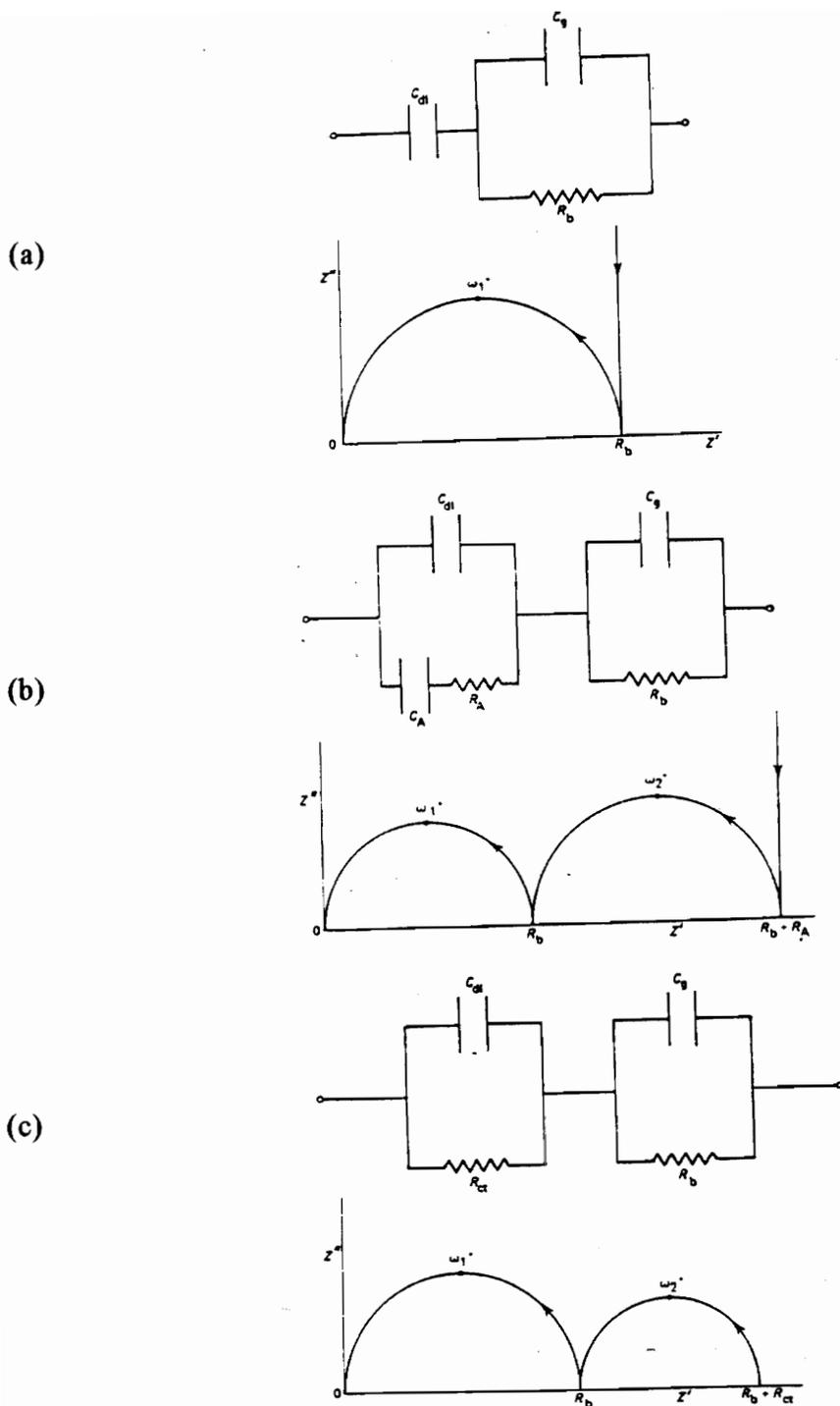


Figure 27. Equivalent circuits and predicted complex-plane impedance spectra for the cases of (a) blocking electrodes without specific absorption, (b) blocking electrodes with specific absorption, and (c) non-blocking electrodes [50].

The opposite situation is that involving non-blocking electrodes; the equivalent circuit model is shown in Figure 27 (c). A typical example is a metal oxide electrode (such as RuO_2) on PZT. In this case, the mobile oxygen vacancies from PZT bulk can discharge at a high rate at the electrode by crossing the ferroelectric/electrode interface and penetrating the electrode. Here, R_{ct} is a charge transfer resistance between the electrode and electrolyte and ω_2^* is equal to $(C_{dl}R_{ct})^{-1}$. For the case when charge transfer resistance for mobile ion transfer between the electrode and electrolyte is less than that between adjacent layers in the bulk of the electrolyte, the interfacial impedance becomes negligible and the equivalent circuit reduces to R_b in parallel with C_g . The case of absorption, as shown in Figure 27 (b), is because some abnormal positions of the proximity of electrode surface become possible for the mobile ions and lead to the entrapment of these mobile ions. In this case, C_A is a capacitance which arises from the specific adsorption of the mobile ions and ω_2^* here is equal to $(C_{dl}R_A)^{-1}$.

For the above cases, the parameter R_b , which represents bulk resistance of electrolyte, is the resistance of ion migration in the bulk electrolyte. The inverse of R_b represents the ionic conductance. Therefore, the ionic conductivity can be obtained by multiplying a geometric factor.

4.2 Sample preparation and measurement

The bulk samples, $\text{SrBi}_2\text{Nb}_2\text{O}_9$, were made starting from mixing the metal oxide powder to get the mixed powder by calcinating at 1050°C for 2 hours. A pellet can be made from the mixed powder. The pellets were sintered at 1280°C for 3 hours. The electrodes were sputtered with platinum onto both sides of the pellet to form external contacts. Then, a platinum lead attached on the electrodes with platinum paste.

For thin film samples, Pt/SrBi₂Ta₂O₉/Pt was grown on single crystal MgO substrates using pulsed laser ablation. Pt has the same lattice constant as that reported for SBT films ($a = 0.389$ nm). This indicates for favorable growth of SBT films along the c-axis, the underlying Pt films need to be grown with a (100) preferred orientation. Then, MgO(100) provides the necessary template for (100) texture in platinum. The Pt films were sputtered on single crystal MgO(100) substrates. The films were deposited at three different substrate temperatures - room temperature, 600°C and 700°C. As expected, the room temperature deposited films showed a strong (111) texture. With increasing deposition temperature, additional reflections were gathered from the (200) diffraction planes until at a deposition temperature of 700°C the Pt films were almost completely oriented with the (100) planes parallel to the substrate surface. SrBi₂Ta₂O₉ films were then deposited by pulsed laser ablation on these platinum coated MgO substrates. The SBT films deposited on the (111) textured Pt films are randomly polycrystalline. However, the films deposited on MgO(100)/Pt(100) substrates show a strong (001) texture. For the intermediate case of the films deposited on substrates containing both (100) and (111) oriented Pt films. In effect, these results indicate that simply by increasing the deposition temperature of Pt bottom electrode, the degree of c-axis orientation in the ferroelectric can be increased [44].

The samples were measured with an HP4192A impedance analyzer with a four terminal-shielded two terminal extension configuration. The applied frequency was scanned from 10 Hz to 1M Hz with no bias voltage applied. A very small (50 mV) oscillating amplitude was applied for each measurement. An IBM PC via IEEE 488 interface was used to control the measurement and collect the data points. For bulk samples, the heat treatment was carried out in a stand-alone oven controlled by OMEGA mode CN9000 temperature controller while for thin film samples it was carried out on a

hot plate controlled by a MDC-490 temperature controller. However, the heat treatment for thin films is imperfect because of a maximum 300°C from the MDC-490 controller and unstable surface temperatures. The applicability of the impedance spectroscopy is limited only by the accuracy and range of the laboratory impedance analyzer. HP4192A can measure impedance in the frequency range of 5 Hz to 13 MHz. The upper limit of the measured impedance value is approximately 1.3 MΩ. This value can prove to be the most important limitation in the application of impedance spectroscopy.

4.3 Fatigue-free Hypothesis

As mentioned before, the occurrence of fatigue in perovskite type ceramics is mostly from space charges created at electrode-ferroelectric interfaces. These space charges create dipoles at the interfaces with opposite direction to the polarization in the bulk. In most ferroelectric ceramics, oxygen vacancies form to preserve local charge balance. These defects are known to be very mobile and responsible for the ionic conductivity [45]. Under an applied electric field, these highly mobile oxygen vacancies can move across the bulk ferroelectrics and reach the electrode interfaces. According to the well established fatigue model [25, 26] for perovskite type ferroelectrics, several requirements have to be satisfied for the occurrence of fatigue. Generally, there should be a high oxygen vacancy concentration in the materials; and these oxygen vacancies should have sufficient mobility to migrate under an applied electric field. In addition to the concentration and mobility, there should be trap sites in the cell, i.e., in electrode-ferroelectric interfaces. By applying an electric field, these oxygen vacancies will move in one direction towards the electrode and are blocked by the electrode (Pt-electrode) so that these defects cannot cross the interface to the metal side. By changing the applied field

direction, those oxygen vacancies which have already reached the interface are trapped by some abnormal positions at the interface and are not able to move back to the bulk. In Pt/PZT/Pt, this entrapment is due to the defects moving into the position with lower energy level at the electrode interface. In other words, the high energy barrier at the interface prevents the defects from going back to the bulk. As a result, these trapped oxygen vacancies create the space charges at the electrode-ferroelectric interface and fatigue occurs.

For bismuth layer oxides having perovskite-like layer type structure, there are several possible reasons leading to the high lifetime for these materials. The first possibility is low oxygen vacancy concentration in the materials. Therefore, the amount of oxygen vacancy pile-up at electrode interfaces is very little. The space charges created in this case are not significant, so no fatigue is observed. Consequently, the ionic conductivity due to oxygen vacancy movement should be low compared to perovskite-type titanates.

The second possibility is the oxygen vacancy concentration in bismuth layered oxides is high, but have low mobility to reach the electrode interfaces in a limited time. Consequently, no defects pile up at electrode-ferroelectric interfaces, so fatigue does not occur. Since the conductivity is proportional to the charge mobility, the ionic conductivity in this case is expected to be low.

The third possibility is that the oxygen vacancies have high concentration as well as high mobility. The defects could probably reach the electrode-ferroelectric interface in a limited time but are blocked by the electrode. In this case, the most likely reason for low fatigue is the energy barrier at electrode-ferroelectric interface is low, so the oxygen vacancies are not trapped at the interface. Upon switching the applied electrical field, these defects can move back to the bulk ferroelectric. Because of no vacancy pile-up, there are

no space charges created at the interface; therefore it increases the resistance in fatigue. The ionic conductivity in this case is expected to be higher than the other two cases.

In this study, the above three hypotheses are proposed to explain the low fatigue in bismuth layered oxides. In order to decide the most possible model, ionic conductivities of the materials are measured by complex impedance plane and compared with the ionic conductivity of perovskite structure materials in literature.

4.4 Modified Debye model

The ac response of an electrolyte or electrochemical cell can be expressed in any of four basic formalisms as below:

- The complex admittance, $Y^* = (R_p)^{-1} + j\omega C_p$
- The complex impedance, $Z^* = (Y^*)^{-1} = R_s - j/\omega C_s$
- The complex permittivity, $\epsilon^* = \epsilon' - j\epsilon''$
- The complex modulus, $M^* = (\epsilon^*)^{-1} = M' + jM''$

where the subscripts p and s refer to the equivalent parallel and series circuit components respectively. These functions are also related as:

$$Y^* = j\omega C_0 \epsilon^* \quad \text{and} \quad M^* = j\omega C_0 Z^*$$

where C_0 is the vacuum capacitance of the cell.

For a series combination of an ideal capacitor and a resistor, the complex permittivity plot approximates a semicircle if materials behave in a manner close to Debye behavior. The corresponding complex permittivity plot has been widely used and is known as a Cole-Cole plot [46]. The ideal Debye behavior gives the complex relation as:

$$\epsilon^*(\omega) = \epsilon_\infty + \frac{\epsilon_s - \epsilon_\infty}{1 + (i\omega / \omega_D)}$$

where ϵ_s is the static permittivity, ϵ_∞ is the permittivity at infinitely high frequencies, and ω_D is the Debye relaxation frequency.

The Debye equation is based on the assumption that transient polarization can be represented by a simple exponential with a single relaxation time. For most materials, however, the experimental data are not well described by the Debye equations. Actually, most dielectric materials depart in varying degrees from the Debye response and it becomes necessary to modify the empirical expression representing the Cole-Cole plot. One such modification was proposed by Cole and Cole [46] and it is given by

$$\epsilon^*(\omega) = \epsilon_\infty + \frac{\epsilon_s - \epsilon_\infty}{1 + (i\omega / \omega_D)^{1-\alpha}} \quad (4.1)$$

where graphically, the parameter α represents the tilting angle ($\alpha\pi/2$) of the circular arc from the real axis.

Another modification needs to be added for ionic conductors [47]. Since ionic conductivity is determined by the mobility of ions as well as their concentration, and the mobility is dependent on ion hopping rate, the total expression becomes:

$$\epsilon^*(\omega) = \epsilon_\infty + \frac{\epsilon_s - \epsilon_\infty}{1 + (i\omega / \omega_D)^m} + \left\{ \frac{\sigma_0}{\epsilon_0 \omega} \left[1 + \left(\frac{i\omega}{\omega_I} \right)^n \right] \right\} \quad (4.2)$$

where $m = 1-\alpha$, n is a constant between 0 to 1, σ_0 is the dc conductivity, and ω_I is ionic hopping frequency. The complex permittivity can be decomposed as

$$\epsilon' = \epsilon_\infty + \frac{(\epsilon_s - \epsilon_\infty) \left[1 + \left(\frac{\omega}{\omega_D} \right)^m \cos\left(\frac{m\pi}{2}\right) \right]}{1 + 2\left(\frac{\omega}{\omega_D}\right)^m \cos\left(\frac{m\pi}{2}\right) + \left(\frac{\omega}{\omega_D}\right)^{2m}} + \frac{\sigma_0}{\epsilon_0 \omega} \left(\frac{\omega}{\omega_I} \right)^n \sin\left(\frac{n\pi}{2}\right) \quad (4.3)$$

$$\epsilon'' = \frac{(\epsilon_s - \epsilon_\infty) \left(\frac{\omega}{\omega_D} \right)^m \sin\left(\frac{m\pi}{2}\right)}{1 + 2\left(\frac{\omega}{\omega_D}\right)^m \cos\left(\frac{m\pi}{2}\right) + \left(\frac{\omega}{\omega_D}\right)^{2m}} + \frac{\sigma_0}{\epsilon_0 \omega} \left[1 + \left(\frac{\omega}{\omega_I} \right)^n \cos\left(\frac{n\pi}{2}\right) \right] \quad (4.4)$$

By fitting the experimental data, the parameters σ_0 , m , n , ω_D , ω_I , ϵ_s and ϵ_∞ can be obtained.

4.5 Experimental results

4.5.1 SrBi₂Nb₂O₉ (SBN) bulk ceramics with Pt-electrodes

The complex impedance planes of SBN ceramics were plotted as a function of temperature from room temperature to 800°C. Figures 28 (a) and (b) show typical examples at 100°C and 520°C. According to the results, at temperatures below 400°C, the complex impedance only showed one simple semicircle with an inclined spike at low frequencies, as shown in Figure 28 (a). However, at temperatures above 420°C, another broader arc appeared at low frequencies as shown in Figure 28 (b).

Impedance data such as Figure 28 can be analyzed in term of equivalent circuits, comprised of networks of resistance and capacitance elements like Figure 27. The main problem in data analysis is to identify an equivalent circuit that matches the general form of the complex impedance plots. Once this has been done, extraction of values for the components R and C are relatively straightforward. To a first approximation, the data showed in Figure 28 (a) can be represented by the equivalent circuit as the inset of the Figure, which is composed of a parallel RC (R_b and C_g) circuit in conjunction with a blocking capacitor C_{dl} . According to the impedance results and the equivalent circuit model, the semicircle shown in Figure 28 (a) represents the bulk response of the sample. The calculated value of bulk resistivity given by the intersection of the arc with x-axis is about $3.29 \times 10^6 \Omega\text{-cm}$. The inclined spike observed at low frequencies is represented by the blocking capacitor in the equivalent circuit. As mentioned by Bauerle [42], this spike at low frequencies is attributed to polarization at electrode-electrolyte interface and arises if the charge carrier is mobile ions, i.e. oxygen vacancies. In this case, the bulk resistivity obtained from the semicircle turns out to be ionic conductivity with the value of about

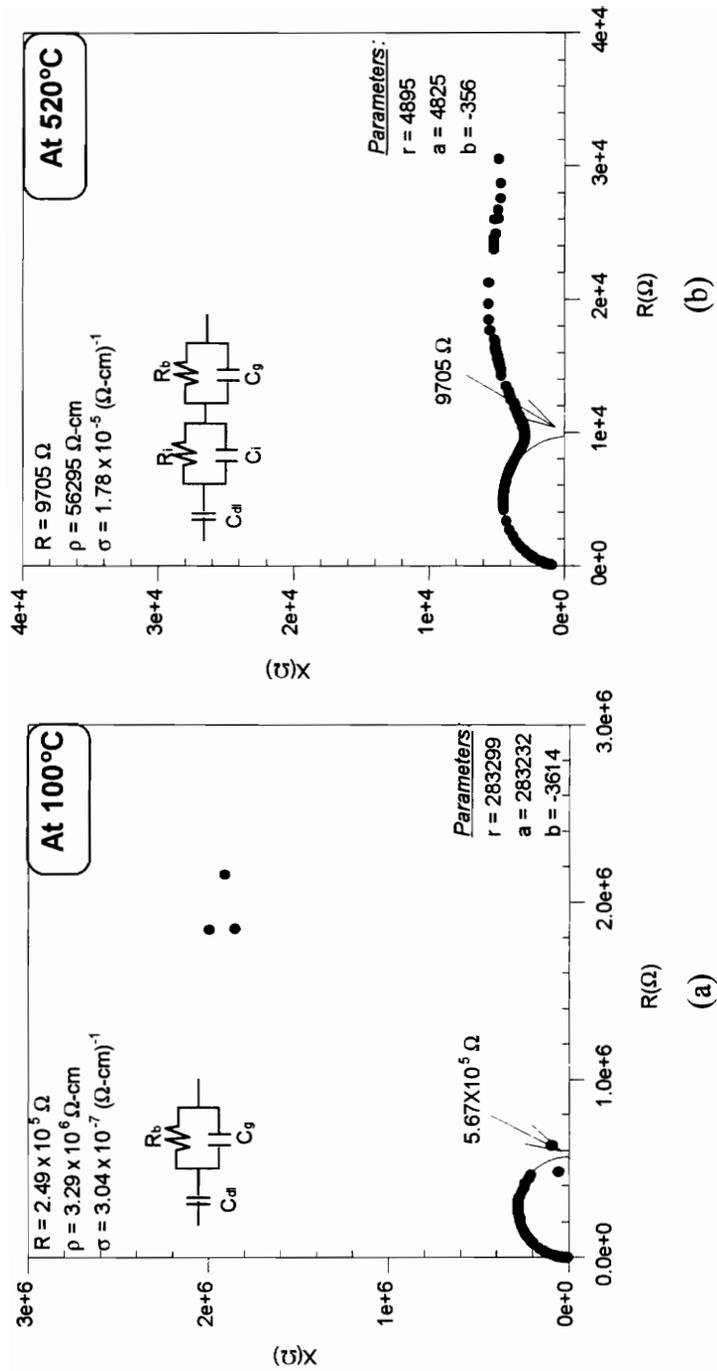


Figure 28. The complex impedance planes of SBN ceramics with Pt electrodes measured at (a) 100°C, and (b) 520°C; and their equivalent circuits shown as inset.

3×10^{-7} S/cm. This value is found to be much larger than the value for perovskite structure cases which is about 10^{-11} - 10^{-10} S/cm at 100°C [45, 48].

For high temperature representation such as Figure 28 (b), the equivalent circuit is shown in the inset of the figure. This model contains two parallel RC circuit elements in series with a blocking capacitor. In Figure 28 (b), the semicircle observed at high frequencies again represents the bulk performance of the sample. At the low frequencies end, a small spike is observed and indicates ion transportation. Therefore, the calculated bulk ionic conductivity of SBN was about 1.8×10^{-5} S/cm. However, at moderate frequencies, the broader arc could be attributed to the effects of grain boundaries or electrode-ferroelectric interfaces or be both. At this moment, we are not able to identify the cause of this broader arc yet.

Figure 29 shows the bulk conductivity of SBN as a function of temperature. The values of bulk conductivities were calculated from the complex impedance planes at various temperatures. The data shows that, at temperature below 300°C , there is no obvious change in bulk conductivity. However, for the temperature above 300°C , the bulk conductivities increased exponentially with increasing temperature. The activation energy at high temperatures represented the energy for ion hopping in the bulk and was calculated as about 0.86 eV.

Another way of presenting complex impedance, impedance spectroscopy, was also studied as functions of frequencies at various temperatures. Figure 30 (a) and (b) show the typical examples measured at 100°C and 520°C . From the results, at low temperature, the SBN ceramics have dielectric properties very close to Debye behavior as shown in Figure 30 (a). The Debye relaxation frequency was obtained from the peaks of reactance (X) spectra and was about 2.2×10^4 s⁻¹ at 100°C . However, as temperature increased, the materials departed from ideal Debye behavior. The peaks of the reactance (X) spectra

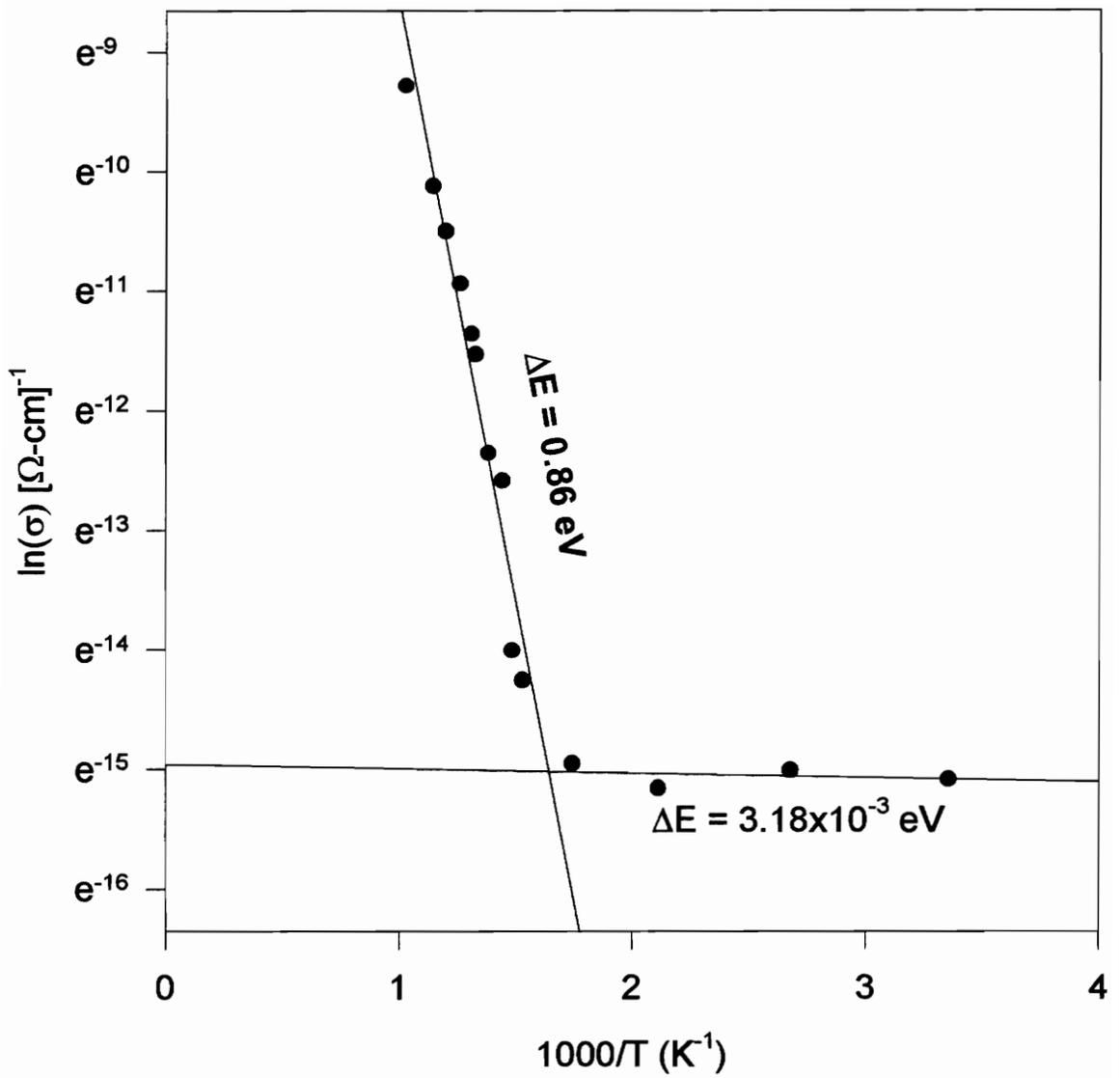


Figure 29. The bulk conductivity derived from complex impedance planes of SBN at various temperatures.

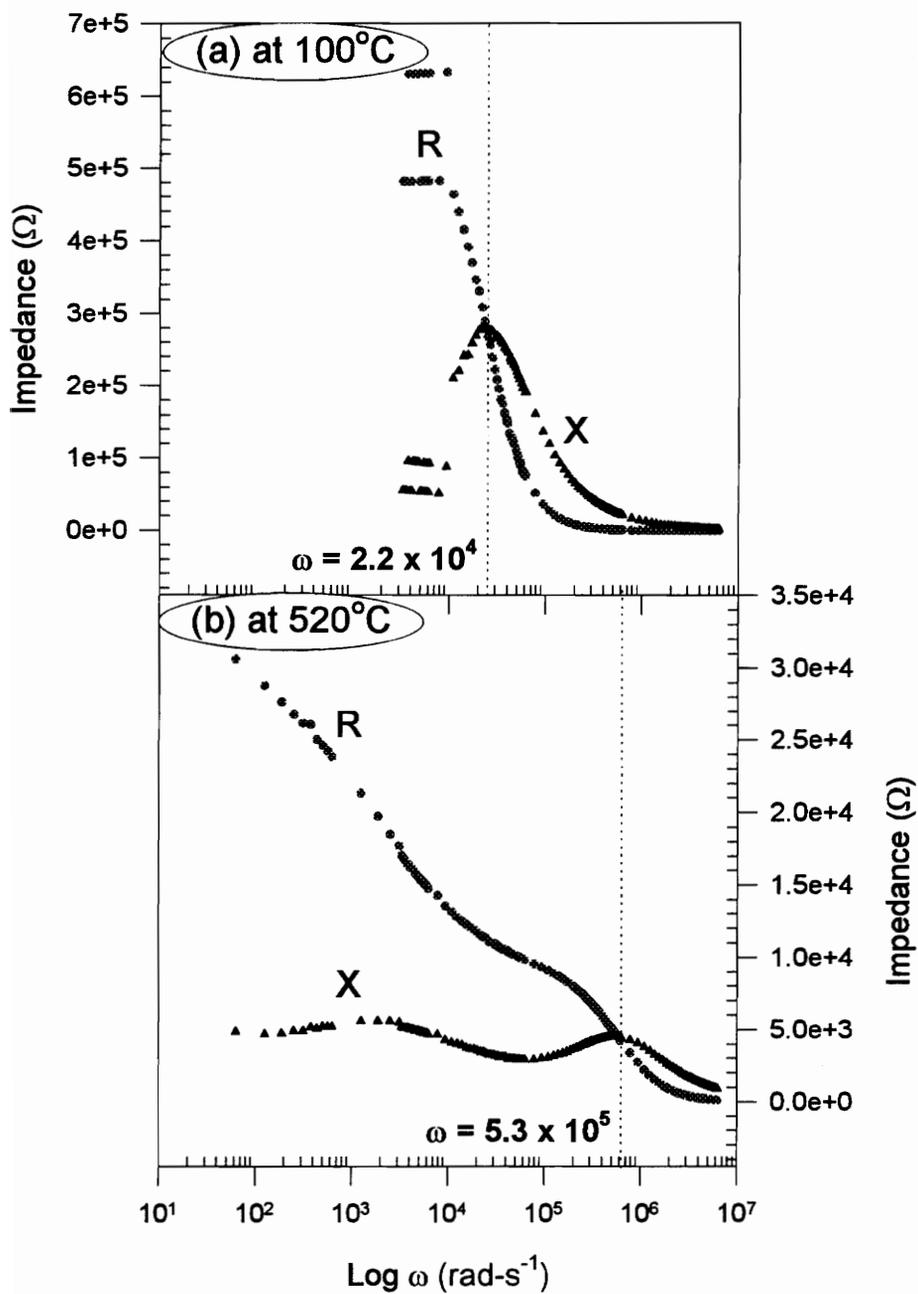


Figure 30. The impedance spectroscopies of SBN with Pt-electrodes measured at (a) 100°C, and (b) 520°C.

became broader at high temperatures, which indicated non-Debye behavior. The assumption of single relaxation time is no longer valid, hence Equation 4.1 made the correction of the distribution of relaxation times. At high temperatures as Figure 30 (b), two peaks of reactance spectra were observed and were in accordance with those two arcs showed in complex impedance planes. Therefore, the peak at high frequencies represented the bulk dielectric properties of the samples.

The permittivity spectra of SBN ceramics were also plotted with two typical examples shown in Figure 31. It has been mentioned before that the materials have the dielectric properties of non-Debye materials and the main current is due to ion transport. Therefore, the Equation 4.3 and 4.4 were applied to fit the experimental permittivity spectra. Among these parameters, constants m and dielectric constants at infinite frequencies, ϵ_{∞} , were fixed. The constants m were calculated from the tilting angles of the complex impedance semicircles from the real-axis and ϵ_{∞} , was calculated from the permittivity measurements. The fitted parameters are listed in Table 2.

4.5.2. $\text{SrBi}_2\text{Ta}_2\text{O}_9$ thin films

Structurally, the bismuth layered ferroelectrics are highly anisotropic and therefore the ferroelectric properties are strongly dependent on the orientation of the films with respect to the substrates. The complex impedance of Pt/SBT/Pt thin films made by PLD was studied in terms of orientation effects. Figure 32 shows complex impedance planes for three different orientations: polycrystalline, partial c-oriented and complete c-oriented. At temperature below 200°C, all the complex impedance showed a simple semicircle with a spike at low frequencies, just like the cases of SBN bulk ceramics. The equivalent circuit of Figure 27 (a) can also be applied in this case. Generally, the charge transport is by mobile ions, regardless of lattice orientation. Due to the limitations of the equipment,

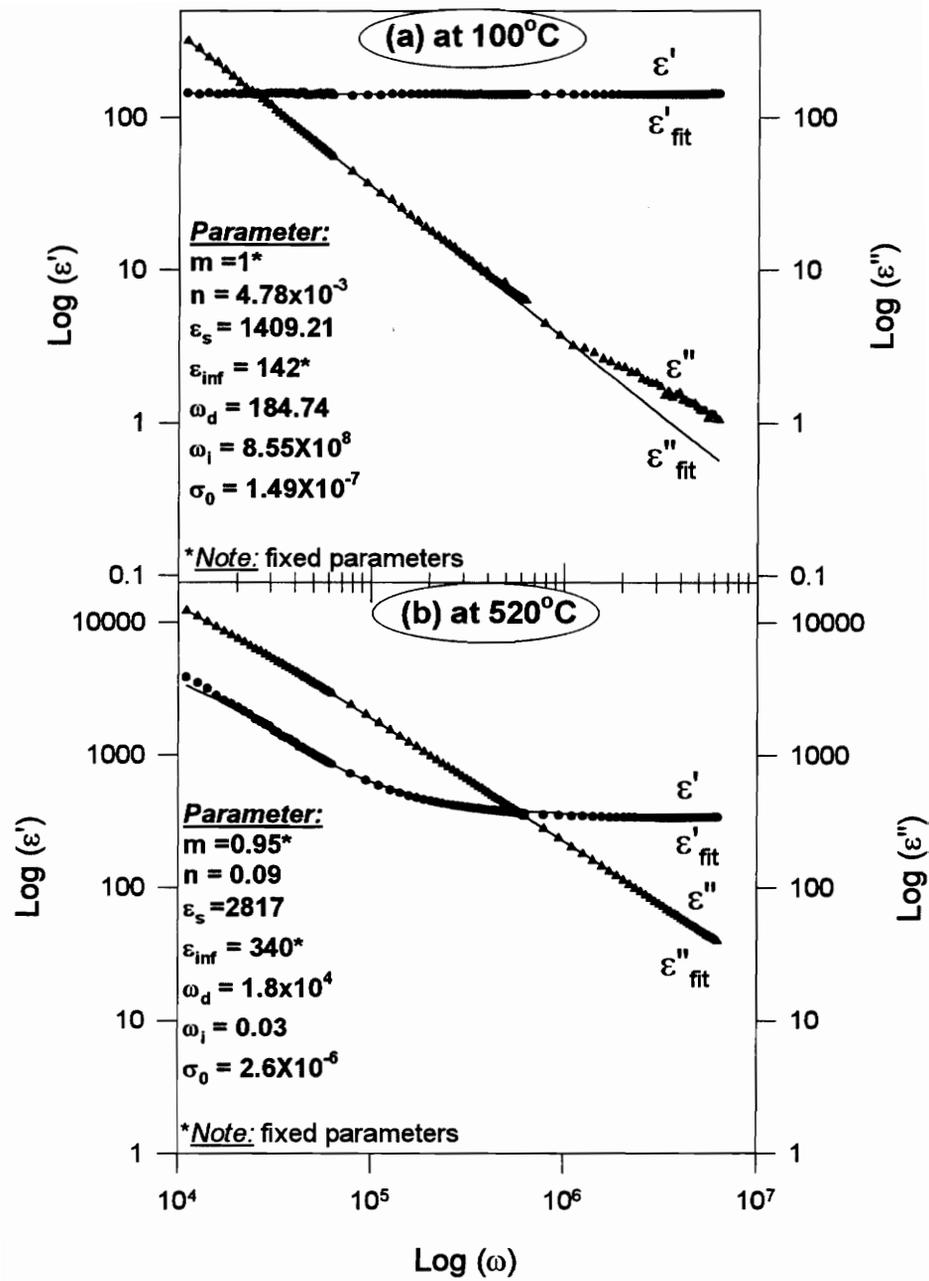


Figure 31. Permittivity spectra of SBN ceramics measured at (a) 100°C, and (b) 520°C; the data fitted as solid lines.

Table 2. Modified Debye parameters of SrBi₂Nb₂O₉ dielectric properties measured at various temperatures.

Parameters							
Temperature	m	n	ϵ_s	ϵ_{∞}	ω_d	ω_j	σ_0
25°C	1	0.017	1081	141	398	8.54X10 ⁸	1.36X10 ⁻⁷
100°C	1	0.005	1409	142	184.7	8.55X10 ⁸	1.49X10 ⁻⁷
200°C	1	0.009	1014	160	236	8.58X10 ⁸	1.27X10 ⁻⁷
300°C	1	0.58	1720	195	262.8	1.02X10 ⁶	2.77X10 ⁻⁷
400°C	0.88	0.52	33228	286	117	3.40X10 ⁵	5.40X10 ⁻⁷
420°C	0.94	0.27	27602	366	225.9	1.60X10 ⁵	1.70X10 ⁻⁶
480°C	0.94	0.09	3004	441	9646	0.006	1.46X10 ⁻⁶
520°C	0.95	0.09	2817	340	1.8X10 ⁴	0.03	2.60X10 ⁻⁶

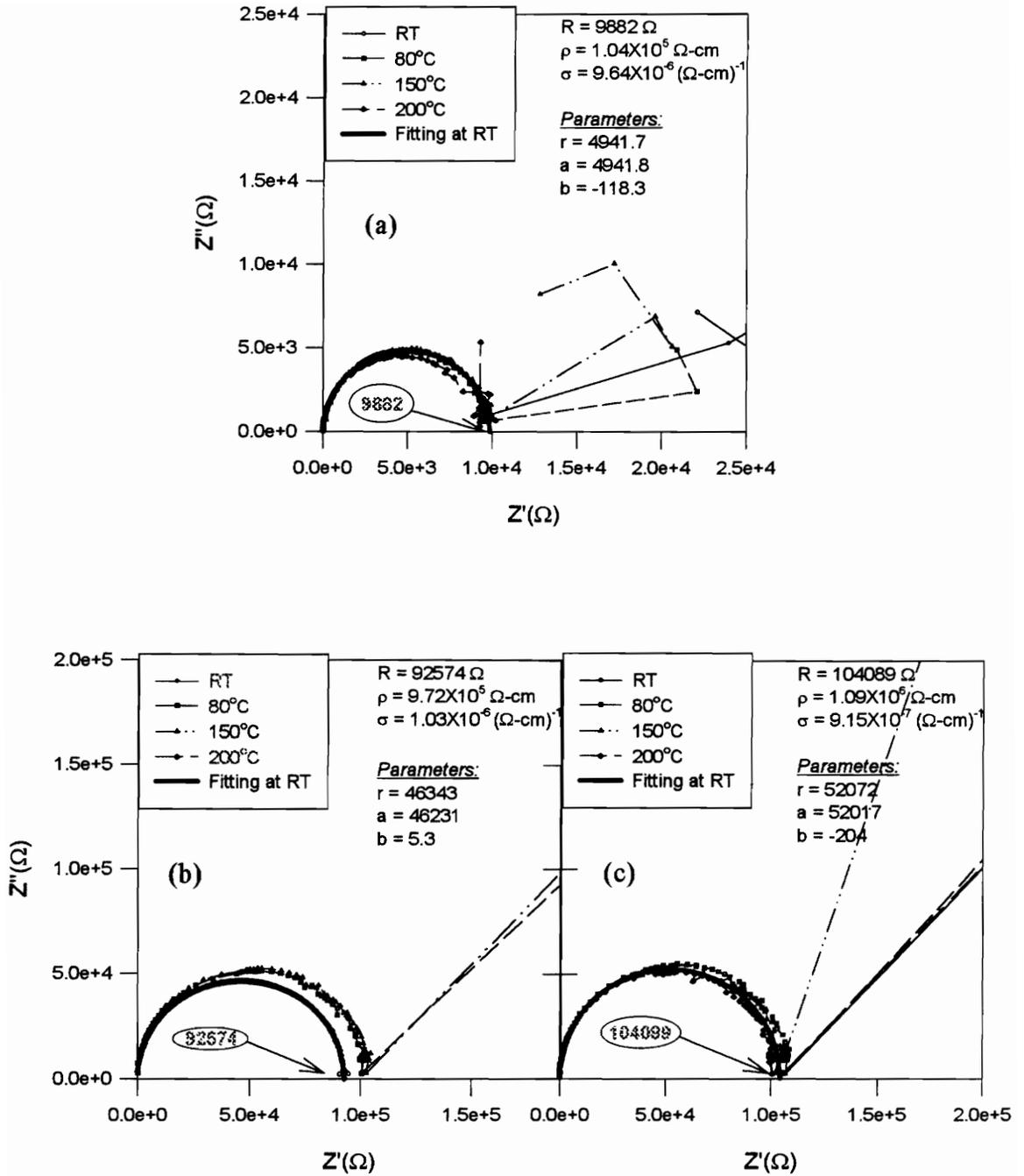


Figure 32. The complex impedance planes of (a) polycrystalline, (b) partial c-oriented and (c) complete c-oriented SBT thin films.

measurements were carried out up to 200°C. There were no significant differences in the measured resistivities in this temperature range for all the samples, identical with the results of SBN bulk ceramics shown in Figure 29. On the other hand, the results showed the bulk resistivity increased with increasing *c*-orientation ratio. In other words, the bulk conductivities of SBT thin films decreased with increasing *c*-orientation ratio. From the lower ionic conductivity for *c*-oriented SBT films, it can be concluded that the ion transport along the *c*-axis is slower than in the *a-b* plane. This might explain the phenomenon of high leakage current in the *a-b* plane for bismuth layered oxides.

4.6 Conclusion

From the preliminary results, both bulk ceramics and thin films of bismuth layered structure ferroelectrics possess much higher ionic conductivities than of perovskite structures. Because high ionic conductivity was found in bismuth layered oxides, the models which presume either low conductivity and low defect concentration or high defect concentration but low ion mobility are dismissed. Ultimately, the most likely model to explain high resistance in fatigue for bismuth layered oxides assumes a low energy barrier at electrode-ferroelectric interfaces. Even though high ionic conductivities are observed in the materials, which implies high defects concentration and mobility, those mobile defects will not be trapped at the electrode-ferroelectric interfaces because of low energy barrier at the interfaces. In another view, the study of the orientation effects on bulk conductivity showed that the ion transport is slower along the *c*-axis than in the *a-b* plane.

Chapter 5

Summary

5.1 SBTN vs PZT

For the application of FRAM, PZT ferroelectric capacitors are well known for their high remanant polarization ($\sim 25 \mu\text{C}/\text{cm}^2$), wide operating temperature range and stability under a wide range of operating conditions. However, the degradation problems of PZT capacitors, such as fatigue, retention and imprint problems observed in this study, are hampering the development of this material in commercial FRAM devices. On the other hand, SBTN ferroelectric capacitors have been evaluated using the electrical characterizations in this study as excellent candidates to replace PZT capacitors as FRAM devices. Although the SBTN capacitors have the remanant polarization of $\sim 10 \mu\text{C}/\text{cm}^2$, this value is well within the requirements for FRAM devices. The most advantageous characteristic of SBTN capacitors for PZT replacement are their high resistance in fatigue (more than 10^{10} cycles), their good retention properties and their failure to imprint.

However, the high dielectric properties of PZT films (~ 1000 dielectric constant) make them favorable in the applications of DRAM rather than SBTN films do, which have dielectric constants of only 100~300. A limiting factor for any potential DRAM capacitor is leakage current. High leakage currents are deleterious to operation since the cells require more frequent refreshing, use more power, and limit the maximum field that may be applied across the device. Even though the leakage current of PZT films is higher than typical specifications for $\text{SiO}_2/\text{Si}_3\text{N}_4$ films, the high storage capacity of PZT films reduces the required capacitor area and increases the allowable leakage current such that the films satisfy a refresh specification.

5.2 Complex Impedance

Both bulk ceramics and thin films of bismuth layered structure ferroelectrics possess much higher ionic conductivity, measured by using complex impedance method, than of perovskite structure. Because high ionic conductivity was found in bismuth layered oxides, the most possible model to explain high resistance in fatigue for bismuth layered oxides is of low energy barrier at electrode-ferroelectric interfaces. Even though high ionic conductivity is observed in the materials, which implies high defect concentration and mobility, those mobile defects will not be trapped at the electrode-ferroelectric interfaces because of low energy barrier at the interfaces.

The applications of complex impedance are not limited to obtaining the ionic conductivity. It also can identify the presence of inhomogeneities at separate regions characterized by different dielectric properties, allow the separation of several contributions to the total cell impedance, arising from bulk conduction and interfacial phenomena, as polarization effects at the electrode-electrolyte interfaces. However, because of limitations in our current equipment, intensive study of complex impedance is limited. The HP4192A impedance analyzer can measure impedance only in the frequency range of 5 Hz to 13 MHz and the upper limit of the measured impedance value is approximately 1.3 M Ω . The former range made it impossible to observe the impedances in the ultra low and high frequency. The latter range restricts the impedance measurement in PZT films, which have far higher impedance. The hot plate and MDC 490 temperature controller setup used for thin films also limits the breadth of our complex impedance study in thin films.

5.3 Future work

- (i) Measure the complex impedance of ferroelectric capacitors (like PZT) at the low- and high-ends of the frequency range with better equipment (sufficient frequency range and high impedance) in order to have a more complete observation of the cell impedance, especially for the observation of interfacial phenomena.
- (ii) Since the fatigue, resistivity degradation and time dependent dielectric breakdown (TDDB) characterizations are time-consuming, it may be useful to develop accelerated test methods with appropriate stressors, such as high temperature, high field, etc. If appropriate models can be developed for the degradation mechanisms under accelerated stresses, one may be able to determine the behavior of the ferroelectric device under normal operating conditions.
- (iii) If ferroelectric memories are commercialized, there will be a necessity to program the ferroelectric capacitor as an element in modelling programs such as SPICE. Therefore, ferroelectric memories could be used extensively in integrated circuit design.

APPENDIX: "IVTHIN12" PROGRAM

```
#include <graphics.h>
#include <math.h>
#include <string.h>
#include <chplib.h>
#include <cfunc.h>
#include <dos.h>
#include <stdio.h>
#include <conio.h>
#include <stdlib.h>

void scancon(int *output, int e);
void scancons(char taxi[], int e);
void checkerror(int error, char *routine);
void hpiptalk(void);
void parameters(void);
void drawscreens(void);
void graphpoints(float sdev, int count);
void graphpointsl(float sdev, int count);
void values(char idivch[], char tdivch[], float sdev, int count);
void changeparam(void);
void stdev(float *dev, float x[], int numx, int count);
void ivtcurve(void);

struct data{
    float reading;
    int time;
} *measurement[3000];

struct data2{
    float current;
    float voltage;
    int temperature;
} *ivdata[3000];

int mx, my, timinc, icount=0;
int lstmsmts; /* the least times of measurments */
int maxmsmts; /* the maximum times of measurments */
int lnomsmts; /* the last numbers of measurements taken for sdev */
int initemp=25, inctemp, fintemp=25, curtemp=25;
float avg, volt, voltinc, voltfin;
float samarea, samthic, efield;
float curval, curtim, readings[2];
```

```

float maxi, mini, maxt, mint, maxi2, mini2, maxv2, minv2;
float allsdv;
char samname[12], title[30];
char idivch[12], tdivch[12];
char oper[15], datafile[30], shortfile[30], voltage[12];

void main(void)
{
    int graphmode, graphdriver;

    textmode(3);
    parameters();

    detectgraph(&graphdriver, &graphmode);
    initgraph(&graphdriver, &graphmode, "c:\\tc");
    mx = getmaxx(); my = getmaxy();

    drawscreen();
    hpibtalk();
    getch();
    closegraph();
    exit(0);
}
/*****
**/
void parameters(void)
{
    int choice, numrep;
    char c;
do
    {
        clrscr();
        gotoxy(5, 4);
        printf("This is HP-IB interface to Model 617 Programmable Electrometer");
        gotoxy(5,5);
        printf("for Measurment of Leakage Current");
        gotoxy(20,6);
        printf("The Thin Films Lab, VT, Jan, 1995");
        gotoxy(15,8);
        printf("Enter beginning voltage (in volts > 0) ");
        gotoxy(55,8);
        scanf("%f",&volt);
        gcvt(volt,5,voltage);

        gotoxy(15,9);

```

```

printf("Enter voltage increment (in volts > 0) ");
gotoxy(55,9);
scanf("%f",&voltinc);

gotoxy(15,10);
printf("Enter final voltage (in volts) ");
gotoxy(55,10);
scanf("%f",&voltfin);

gotoxy(15,11);
printf("Enter time interval (millisecond)");
gotoxy(55,11);
scanf("%d",&timinc);

gotoxy(15,12);
printf("Enter Data File (no ext.)");
gotoxy(55,12);
scanf("%s",datafile);
strcpy(shortfile,datafile);
strcat(shortfile, ".fin");
strcat(datafile, ".dat");

gotoxy(15,13);
printf("Enter Sample Area (cm^2)");
gotoxy(55,13);
scanf("%f",&samarea);

gotoxy(15,14);
printf("Enter Sample Thickness (microns)");
gotoxy(55,14);
scanf("%f",&samthic);

gotoxy(15,15);
printf("Enter Sample Name ");
gotoxy(55,15);
scancons(samname,0);

gotoxy(15,16);
printf("Enter Title of Graph ");
gotoxy(55,16);
scancons(title, 0);
strcat(title, " Leakage Curve");
/*
gotoxy(15,17);
printf("Enter Beginning Temp ");

```

```

gotoxy(55,17);
scanf("%f",&initemp);

gotoxy(15,18);
printf("Enter Temp Increment ");
gotoxy(55,18);
scanf("%f",&inctemp);

gotoxy(15,19);
printf("Enter Final Temp  ");
gotoxy(55,19);
scanf("%f",&fintemp);printf("%f",fintemp);
*/
gotoxy(15,18);
printf("Enter The Last Times of Measurments Taken for sdev");
gotoxy(68,18);
scanf("%d",&lnomsmts);

gotoxy(15,19);
printf("Enter The Least Times of Measurments");
gotoxy(68,19);
scanf("%d",&lstmsmts);

gotoxy(15,20);
printf("Enter The Maximum Times of Measurments");
gotoxy(68,20);
scanf("%d",&maxmsmts);

gotoxy(15,21);
printf("Enter Allowable SDV(1 -- 5)");
gotoxy(60,21);
scanf("%f", &allsdv);

gotoxy(25,23);
printf("Any changes (Y) ");
c = getche();

} while( c == 89 || c == 121);
}
/*****
***/
void drawscreen(void)
{
int width, height, count;
char c[10] ; char csdv[5];

```

```

int dec;
setviewport(0,0,mx,my,1);
setfillstyle(INTERLEAVE_FILL,BLUE);
bar(0,0,mx/40,my);
bar(mx-mx/40,0,mx,my);
bar(0,my - my/40, mx,my);
bar(0,0,mx,my/40);

    settextstyle(TRIPLEX_FONT,HORIZ_DIR,2);
/* settextstyle(DEFAULT_FONT,HORIZ_DIR,2);
*/  setusercharsize(2,3,3,4);
width = textwidth(title);
height = textheight(title);
outtextxy(410-width/2,14,title);

settextstyle(TRIPLEX_FONT,HORIZ_DIR,1);
/* x - axis */
line(240,380,570,380);
for(count = 240; count < 570; count+= 20)
    line(count,382,count,378);

/* x - label */
outtextxy(576,371,"t");

/* y - axis */
line(240,60,240,390);
for(count = 380; count > 60; count -= 16)
    line(238,count,242,count);

/* y -label */
outtextxy(240,38,"Log I");

/* settextstyle(DEFAULT_FONT,HORIZ_DIR,1);

height = textheight("V");
width = textwidth("Output File1 = ");

outtextxy(250,350, "Output File1 = ");
outtextxy(250+width,350,datafile);

outtextxy(250,350+1.5*height,"Output File2 = ");
outtextxy(250+width,350+1.5*height,shortfile);

outtextxy(250,350+3*height,"Sample Name = ");

```

```

    outtextxy(250+width,350+3*height,samname);
*/

/* bottom right window */
rectangle(240,405,623,457);
rectangle(242,407,621,455);

/* top left window */
rectangle(18,14,230,200);
rectangle(20,16,228,198);

/* middle left window */
rectangle(18,202,230,389);
rectangle(20,204,228,387);

/* bottom left window */
rectangle(18,391,230,457);
rectangle(20,393,228,455);

/* Constant values for bottom right window */
setviewport(244,409,619,453,1);
clearviewport();
settextstyle(DEFAULT_FONT,HORIZ_DIR,1);

height = textheight("V");
width = textwidth ("Volt i = ");

outtextxy(6,6, "Volt i = ");
outtextxy(6+width,6,voltage);

outtextxy(6,6+1.5*height, "V Inc. = ");
outtextxy(6+width,6+1.5*height,gcvt(voltinc,5,c));

outtextxy(6,6+3*height, "Volt f = ");
outtextxy(6+width,6+3*height,gcvt(voltfin,5,c));

outtextxy(129,6, "Temp.i = ");
outtextxy(129+width,6,gcvt(temptemp,5,c));

outtextxy(129,6+1.5*height,"T Inc. = ");
outtextxy(129+width,6+1.5*height,gcvt(inctemp,5,c));

outtextxy(129,6+3*height, "Temp.f = ");
outtextxy(129+width,6+3*height,gcvt(finctemp,5,c));

```

```

width = textwidth("Thick = ");
outtextxy(253,6, "Thick = ");
outtextxy(253+width,6,gcvt(samthic,5,c));

outtextxy(253,6+1.5*height,"Area = ");
outtextxy(253+width,6+1.5*height,gcvt(samarea,5,c));

outtextxy(253,6+3*height, "Emax = ");
if(atof(voltage)==0) efield = 0;
else efield = voltfin/samthic;
outtextxy(253+width,6+3*height,gcvt(efield,5,c));

/* constant values for bottom left window */
setviewport(22,395,226,453,1);
clearviewport();
width = textwidth( "Output File = ");

outtextxy(6,6, "Allow SDV = ");
outtextxy(6+width,6, gcvt(allsdv,5,c));

outtextxy(6,6+1.5*height, "Last Msmts = ");
outtextxy(6+width,6+1.5*height,gcvt(lnomsmts,5,c));

outtextxy(6,6+3*height, "Lst Msmts = ");
outtextxy(6+width,6+3*height,gcvt(lstmsmts,5,c));

outtextxy(6,6+4.5*height,"Max Msmts = ");
outtextxy(6+width,6+4.5*height,gcvt(maxmsmts,5,c));

/* titles for top left window */
setviewport(22,18,70,196,1);
clearviewport();
width = textwidth( "Ymax = ");
outtextxy(8,8, "Ymax = ");
outtextxy(8,8+1.5*height, "Ymin = ");
outtextxy(8,8+3*height, "Xmax = ");
outtextxy(8,8+4.5*height, "Xmin = ");

outtextxy(8,8+7.5*height, "Xdiv = ");
outtextxy(8,8+9*height, "Ydiv = ");

outtextxy(8,8+12*height, "CurX = ");
outtextxy(8,8+13.5*height,"CurY = ");

```

```

outtextxy(8,8+16.5*height,"SDev = ");
outtextxy(8,8+18*height, "Volt = ");

/* return viewport to entire screen */
setviewport(0,0,mx,my,1);
}
/*****
*/
void hpibtalk(void)

{
char cmd[20];
char in[2], *bitmap;
int length, error=0, elements;
int height, count2, count3, num;
int count, timer, kb;
float recentx[100], sdev = 5;
double timeout_val;
FILE *fp;

fp = fopen(shortfile,"w");
fclose(fp);
fp = fopen(datafile,"w");
fclose(fp);

/*
* Clear the device and check for errors.
*/

IOCLEAR (528L);

/* set timeout value to 10 seconds */
timeout_val = 10;
error = IOTIMEOUT(5L,timeout_val);
checkerror (error, "IOTIMEOUT");

count = timer = 0;

do {

/* set electrometer to voltage */
strcpy(cmd, "D1V");
strcat(cmd,voltage);

```

```

strcat(cmd,"O1X");
length = strlen(cmd);
error = IOOUTPUTS(528L,cmd,length);
checkerror (error, "IOOUTPUTS");

/* set el to read amps          */
strcpy(cmd,"F1X");
length = strlen(cmd);
error = IOOUTPUTS(528L,cmd,length);
checkerror (error, "IOOUTPUTS");

/* Enable data                  */
strcpy(cmd, "B0XG2X");
length = strlen(cmd);
error = IOOUTPUTS(528L,cmd,length);
checkerror(error,"IOOUTPUTS");

do {
    fp = fopen(datafile,"a");

    kb = kbhit();

    /* Get reading                */
    elements = 2;
    error = IOENTERA(528L, readings, &elements);
    checkerror(error,"IOENTERA");

/*    readings[0] =(10+random(100000))*1.0e-11; */
/*    readings[0] = 5.0; */
    /* print readings to file */
    fprintf(fp,"%s %e %d \n",voltage,readings[0],timer);
    fclose(fp);

    measurement[count] = (struct data *)malloc(sizeof(struct data));
    measurement[count]->reading = readings[0];
    measurement[count]->time   = timer;
    curval = readings[0];
    curtim = timer;

/*    graphpoints(sdev, count); */ /* first time thru sdev = 5.0 */
    graphpointsl(sdev, count);
    timer += timinc;

    if(kb != 0)
    { bitmap = malloc(imagesize(200,160,479,319));

```

```

getimage(200,160,479,319,bitmap);
setviewport(201,161,478,318,1);
clearviewport();
rectangle(1,1,215,140);
rectangle(3,3,213,137);
rectangle(5,5,211,135);

getch(); /* this clears the buffer of the pressed key */

settextstyle(DEFAULT_FONT,HORIZ_DIR,1);
height = textheight("User");
outtextxy(8,50," User Interrupt....");

height = textheight("Enter");
outtextxy(30,100,"Enter new voltage");
outtextxy(35,100+1.5*height," (<q> to quit)");
scancons(voltage,1);
if(voltage[0] == 81 || voltage[0] == 113)
    { closegraph();
      exit(0); }

clearviewport();
setviewport(0,0,mx,my,1);
putimage(200,160,bitmap,COPY_PUT);
free(bitmap);
/* set electrometer to voltage */
strcpy(cmd, "D1V");
strcat(cmd,voltage);
strcat(cmd,"O1X");
length = strlen(cmd);
error = IOOUTPUTS(528L,cmd,length);
checkerror (error, "IOOUTPUTS");

/* set el to read amps */
strcpy(cmd,"F1X");
length = strlen(cmd);
error = IOOUTPUTS(528L,cmd,length);
checkerror (error, "IOOUTPUTS");

/* Enable data */
strcpy(cmd, "B0XG2X");
length = strlen(cmd);
error = IOOUTPUTS(528L,cmd,length);
checkerror(error,"IOOUTPUTS");

```

```

}

if(count > 2)
{
    num = 0;
    for(count3 = count; count3 > 1; count3--)
        { recentx[num] = measurement[count3]->reading;
          num++;
          if (num > lnomsmts) break;
        }
    stdev(&sdev, recentx, num, count);
}
if(count > maxmsmts)
{ fp = fopen(shortfile,"a");
  fprintf(fp,"measurment times = %d, %s, %e\n", count, voltage, avg);
  fclose(fp);
  goto max1;
}
count++;
delay(timinc); /* in millisecond */
/* delay(timinc*1000);
*/
} while (fabs(avg-readings[0]) > allsdv*sdev || count < lstmsmts);
max1:

sdev = 5;
count = timer = 0;

ivtcurve();
volt += voltinc;
gcvv(volt,5,voltage);
} while(volt <= voltfin);
fclose(fp);
}

/*****
**/
void stdev(float *dev, float x[], int numx, int count)
{
    float sum1 = 0.0, sum2 = 0.0;
    int count2;
    FILE *fp;

    for(count2 = 0; count2 < numx; count2++)

```

```

        sum1 += x[count2];

    avg = sum1/(numx);

    for(count2 = 0; count2 < numx; count2++)
        sum2 += (x[count2]-avg)*(x[count2]-avg);
    if(numx == 1) numx =2;
    *dev = sqrt((sum2)/(numx-1));

    /* if about to change to next voltage, write data to short file */
    if(fabs(avg-readings[0]) < *dev*allsdv && count > lstmsmts-2)
    {
        fp = fopen(shortfile,"a");
        fprintf(fp,"%s, %e\n",voltage,avg);
        fclose(fp);
    }
}

/***** GRAPHPOINTS GRAPHS INCOMING DATA
*****/

void graphpoints(float sdev, int count)
{
    float idiv, tdiv;
    int count2, xc=0, yc=0, x0, y0;
    int numpoints;
    double xdiv, ydiv;

    if(count == 0) maxi = mini = measurement[0]->reading*1.5;

    mint = 0; maxt = 10;

    if(measurement[count]->reading > maxi)
        maxi = measurement[count]->reading;

    if(measurement[count]->reading < mini)
        mini = measurement[count]->reading;

    if(measurement[count]->time > maxt)
        maxt = measurement[count]->time;

    if(measurement[count]->time < mint)
        mint = measurement[count]->time;

    numpoints = count+1; /* numpoints is needed when points are plotted*/

```

```

/* y-axis */
if(mini < 0 && mini*(-1) > maxi) idiv = ((mini*(-1))/165)*20;
else idiv = (maxi/165) * 20; if(idiv < 1.0e-20) idiv = 20.;
/* x-axis */
tdiv = (maxt/330) * 20; if(tdiv < 1.0e-20) tdiv = 20.;

gcvrt(idiv,5,idivch);
gcvrt(tdiv,5,tdivch);

setviewport(241,60,575,389,1);
/* setviewport(241,60,575,349,1); */ /* for data file name */
clearviewport();
setviewport(0,0,mx,my,1);

/* x - axis */
line(240,225,570,225);
for(count2 = 240; count2 < 570; count2 += 20)
{
    line(count2,223,count2,227);
}

setviewport(241,60,575,389,1);

for(count2 = 0; count2 < numpoints; count2++)
{
    if(count2 > 0) { x0 = xc; y0 = yc;}
    xc = measurement[count2]->time/(tdiv/20);
    yc = 165 - measurement[count2]->reading/(idiv/20);
    if(numpoints < 70)
        circle(xc,yc,2);
    else putpixel(xc,yc,1);

    if(count2 > 0) line(xc,yc,x0,y0);
}
    circle(0,165,4);
values(idivch, tdivch, sdev, count);

setviewport(0,0,mx,my,1);
}
/***** GRAPHPOINTS GRAPHS INCOMING DATA in log way in W0
window ***/

void graphpointsl(float sdev, int count)
{

```

```

float idiv, tdiv;
int count2, xc=0, yc=0, x0, y0; int numpoints;
double xdiv, ydiv;

maxi = 1.0; mini = 1.0e-20;
mint = 0; maxt = 10;

if(measurement[count]->reading < 1.0e-20 )
    measurement[count]->reading = 1.0e-20;

if(measurement[count]->time > maxt) maxt = measurement[count]->time;
if(measurement[count]->time < mint) mint = measurement[count]->time;

numpoints = count+1;
                /* numpoints is needed when points are plotted */

/* y-axis */

idiv = 320/(ceil(log10(maxi)) - ceil(log10(mini)));

/* x-axis */
tdiv = (maxt/330) * 20; if(tdiv < 1.0e-20) tdiv = 20.;

gcvt(idiv,5,idivch); gcvt(tdiv,5,tdivch);

setviewport(241,60,575,389,1);
/* setviewport(241,60,575,349,1); */ /* for data file name */
clearviewport(); setviewport(0,0,mx,my,1);

/* x - axis */
/* line(240,225,570,225); */
line(240,380,570,380);
for(count2 = 240; count2 < 570; count2 += 20)
{   line(count2,382,count2,378);
}

setviewport(241,60,575,389,1);
/* draw the reference points */
    xc=0;
    yc = - ceil(log10(1.0e-5))*idiv;
    line(xc,yc,xc+10,yc); outtextxy(xc+15, yc, "1.0e-5");
    line(320,yc,330,yc);

    yc = - ceil(log10(1.0e-10))*idiv;

```

```

    line(xc,yc,xc+10,yc); outtextxy(xc+15, yc,"1.0e-10");
    line(320,yc,330,yc);

    yc = - ceil(log10(1.0e-15))*idiv;
    line(xc,yc,xc+10,yc); outtextxy(xc+15, yc,"1.0e-15");
    line(320,yc,330,yc);
/* draw the measurements points */
for(count2 = 0; count2 < numpoints; count2++)
{   iff(count2 > 0) { x0 = xc; y0 = yc;}
    xc = measurement[count2]->time/(tdiv/20);
    yc = - log10(measurement[count2]->reading)*idiv;
    iff(numpoints < 70)
        circle(xc,yc,2);
    else putpixel(xc,yc,1);

    iff(count2 > 0) line(xc,yc,x0,y0);
}
    circle(0,320,4);

values(idivch, tdivch, sdev, count);

setviewport(0,0,mx,my,1);
}

/*****
**/

void checkerror(int error, char *routine)
{
char ch;
iff(error != 0)

    {printf("\n Error %d %s \n", error, errstr(error));
    printf(" in call to HP-IB function %s \n\n",routine);
    printf("Press Enter to continue: ");
    scanf("%c",&ch);
    }
    routine = 0;
}

/*****
**/
void values(char idivch[], char tdivch[], float sdev, int count)
{
    int height, width;

```

```

char c[12], c1[12];

/* update values in upper left window */
setviewport(72,18,226,196,0);
clearviewport();
height = textheight("J");

outtextxy(3,8,          gcvt(maxi,5,c));
outtextxy(3,8+1.5*height,  gcvt(mini,5,c));
outtextxy(3,8+3*height,   gcvt(maxt,5,c));
outtextxy(3,8+4.5*height, gcvt(mint,5,c));
outtextxy(3,8+7.5*height,   tdivch);
/* outtextxy(3,8+9*height,   idivch); */
outtextxy(3,8+9*height,   "*10");

gcvt((curtim/timinc),5,c);
gcvt(timinc,5,c1);
strcat(c, " * ");
strcat(c, c1);
/* outtextxy(3,8+12*height, gcvt(curtim,3,c));
*/ outtextxy(3,8+12*height,c);

outtextxy(3,8+13.5*height, gcvt(curval,5,c));

if(count > 3)
outtextxy(3,8+16.5*height,gcvt(sdev,5,c));
outtextxy(3,8+18*height,  gcvt(volt,5,c));
}

/*****
****/
void scancons(char taxi[], int e)
{
int counter = 0, length;
char temp;

/* strcpy(taxi,""); initialize string */

if(e == 1) /* if e = 1 then no echo to the screen */
{ do
{ temp = getch(); /* get a character */

```

```

    if(temp == 13) break;      /* 13 = carriage return */
    if(temp == 8) {counter -=1; taxi[counter] = 32; continue;}
    taxi[counter] =temp;      /* 32 = space */
    counter++;
} while(temp != 13);        /* end while */
taxi[counter] = '\0';      /* end string */
} /* end if */

else /* if e != 0 then echo to the screen */
{ do
{ temp = getche();
  if(temp == 13) break;
  if(temp == 8) {counter -=1; taxi[counter] = 32; continue;}
  taxi[counter] = temp;
  counter++;
} while(temp != 13);      /* end while */
taxi[counter] = '\0';    /* end string */
} /* end if */

if(counter == 0) taxi[counter] = 90;

}
/*****
**/
void scancon(int *output, int e)
{
  char begin[5], c[5];
  int counter;

  if(e == 1) /* if e = 1 then no echo to the screen */
  { for(counter=0;counter<5;counter++)
    { c[counter] = getch(); /* get a character */
      if(c[counter] == 13) break; /* 13 = carriage return*/
      else begin[counter] = c[counter];
      if(c[counter] == 8) counter-=2; /* 8 = backspace */
    }
    strcat(begin,"\0");
  }

  else /* if e != 1 then echo to the screen */
  { for(counter = 0; counter<5; counter++)
    { c[counter] = getche();
      if(c[counter] == 13) break; /* 13 = carriage return */
      else begin[counter] = c[counter];
      if(c[counter] == 8) counter -=2; /* 8 = backspace */
    }
  }
}

```

```

}
strcat(begin, "\0");
}

if(begin[0] != 13)
    *output = atoi(begin);

else *output = -999;
}

/***** IVTCURVE GRAPHS INCOMING DATA
*****/

void ivtcurve(void)
{
    float idiv2, tdiv2, vdiv2;
    int realx=0, realy=0, width, height;
    int count2, xc=0, yc=0, zc=0, x0, y0, xa, ya;
    double xdiv2, ydiv2;
    char idiv2ch[15], vdiv2ch[15], tdiv2ch[15];
    char c[15];

    setviewport(22,206,226,385,1);
    clearviewport();

    /* draw 3d axes */

    /* x - axis */
    line(50,104,190,104);
    for(count2 = 50; count2 < 190; count2 += 10)
        line(count2,104,count2,106);

    /* x - label */
    outtextxy(192,100,"V");

    /* y - axis */
    line(120,34,120,174);
    for(count2 = 104; count2 > 34; count2 -= 10)
        line(120,count2,122,count2);

    for(count2 = 104; count2 < 174; count2 += 10)
        line(120,count2,122,count2);

    /* y - label */
    outtextxy(122,30,"I");

```

```

/* z - axis */
/* line(120,74,190,144);
xa = 130; ya = 84;
do {
    line(xa-2, ya, xa+2, ya);
    xa += 10;
    ya += 10;
} while(xa < 190);
*/
/* z - label */
/* outtextxy(190,142,"T");
*/
/***** NOW BEGIN TO GRAPH DATA *****/
ivdata[icount] = (struct data2 *)malloc(sizeof(struct data2));
ivdata[icount]->current = avg;
ivdata[icount]->voltage = volt;
ivdata[icount]->temperature = curtemp;

if(icount == 0)
{
    maxi2 = mini2 = avg*1.5;
    minv2 = maxv2 = volt*1.5;
}

if(ivdata[icount]->current > maxi2)
    maxi2 = ivdata[icount]->current;

if(ivdata[icount]->current < mini2)
    mini2 = ivdata[icount]->current;

if(ivdata[icount]->voltage > maxv2)
    maxv2 = ivdata[icount]->voltage;

if(ivdata[icount]->voltage < minv2)
    minv2 = ivdata[icount]->voltage;

/* y-axis divisions */
if(mini2 < 0 && mini2*(-1) > maxi2) idiv2 = (mini2*(-1))/7;
else idiv2 = (maxi2/70) * 10;
if(idiv2 < 1.0e-20) idiv2=10.0;
/* x-axis divisions */
if(minv2 < 0 && minv2*(-1) > maxv2) vdiv2 = (minv2*(-1))/7;
else vdiv2 = (maxv2/70) * 10;
if(vdiv2 < 1.0e-20) vdiv2=10.0;
/* z-axis divisions */

```

```

/* tdiv2 = (300/98)*10; */

gcvrt(idiv2,10,idiv2ch);
gcvrt(vdiv2,10,vdiv2ch);
/* gcvrt(tdiv2,5,tdiv2ch); */

for(count2 = 0; count2 < icount+1; count2++)
{
    /* the 120 and 74 are the offset factors for the viewport */
    iff(count2 > 0) { x0 = realx; y0 = realy;}
    xc = 120 + ivdata[count2]->voltage/(vdiv2/10);
    yc = 104 - ivdata[count2]->current/(idiv2/10);
/*    zc = -25 + ivdata[count2]->temperature/(300/98);
*/

    zc=0;
    realx = xc + (.7071068)*zc;
    realy = yc + (.7071068)*zc;

    iff(icontains < 70)
        circle(realx,realy,2);
    else putpixel(realx,realy,1);

    iff(count2 > 0) line(realx,realy,x0,y0);
}

    circle(120,104,5);
/* test the center point */
/* settextstyle(SMALL_FONT,HORIZ_DIR,2);
*/
height = textheight("I");
width = textwidth("Idv = ");

outtextxy(5,5, "Idv = ");
outtextxy(5+width,5,idiv2ch);

outtextxy(5,5+1.5*height,"Vdv = ");
outtextxy(5+width,5+1.5*height,vdiv2ch);

/* outtextxy(5,5+3*height,"Tdv = ");
outtextxy(5+width,3*height,tdiv2ch);
*/
setviewport(0,0,639,479,1);
icontains++;
settextstyle(DEFAULT_FONT,HORIZ_DIR,1);
}

```

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