

Draft 09/01/2009

(Questions? Concerns? Contact Gail McMillan, Director of the Digital Library and Archives at Virginia Tech's University Libraries: gailmac@vt.edu)

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Name: Wenwei Zha

Description of item under review for fair use: Figure 2.2 A Simplified FPGA Architecture. Figure 2.3 The Simplified Block Diagram of the Xilinx XC4000 CLB. Figure 2.4 The Programmable Interconnect of the Xilinx XC4000 Device. XC4000E and XC4000X Series Field Programmable Gate Arrays Produce Specification, [Online]. Available: http://www.xilinx.com/support/documentation/data_sheets/4000.pdf.

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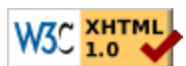
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Description of item under review for fair use: Figure 2.6 A Typical Model of the FPGA Routing Problem. Jayaraman, Rajeev. "Physical design for FPGAs." In Proceedings of the 2001 international symposium on Physical design, pp. 214-221. ACM, 2001.

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Description of item under review for fair use: Figure 2.7 A Simplified FPGA Routing Graph. Betz, Vaughn, Jonathan Rose, and Alexander Marquardt. Architecture and CAD for deep-submicron FPGAs. Kluwer Academic Publishers, 1999.

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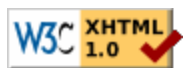
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Description of item under review for fair use: Figure 4.2 How to Divide a 32-bit Frame Address into Six Fields. Figure 4.3 The Top/Bottom Bit and the Raw Address in Xilinx FPGA. Figure 4.4 The Assignment of Major Addresses in a Major Row. Virtex-5 FPGA Configuration User Guide [online]. Available: http://www.xilinx.com/support/documentation/user_guides/ug191.pdf.

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