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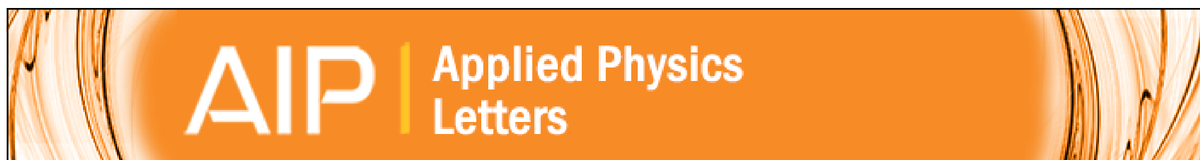

Novel high temperature multilayer electrode-barrier structure for high-density ferroelectric memories

H. D. Bhatt, S. B. Desu, D. P. Vijay, Y. S. Hwang, X. Zhang, M. Nagata, and A. Grill

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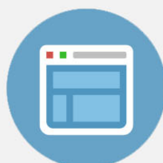
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Novel high temperature multilayer electrode-barrier structure for high-density ferroelectric memories

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This has been accomplished in the past using four/five separate electrode- and diffusion-barrier layers. In this letter, we report a novel Pt–Rh–O_x/Pt–Rh/Pt–Rh–O_x electrode-barrier structure which acts as an electrode as well as a diffusion barrier for integration of the ferroelectric capacitors directly onto silicon deposited using an *in situ* reactive rf sputtering process. The electrodes have a smooth and fine grained microstructure and are excellent diffusion barriers between the $PbZr_{0.53}Ti_{0.47}O_3$ (PZT) and Si substrate and exhibit good thermal stability up to very high processing temperatures of 700 °C. The ferroelectric (PZT) test capacitors using these electrode barriers grown directly on Si, show well saturated hysteresis loops with P_r and E_c of 16 μC/cm^2 and 30–40 kV/cm, respectively. The capacitors exhibit no significant fatigue loss (<5%) up to 10^{11} cycles and have low leakage currents (2×10^{-8} A/cm^2 at 100 kV/cm). These electrode barriers can be used to directly integrate the thin film capacitors on the source/drain of the transistors of the memory cell structure for accomplishing large scale integration. © *1997 American Institute of Physics.*
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Dielectric and ferroelectric thin film capacitors have generated considerable interest due to their potential in applications involving dynamic random access memories (DRAMs) and nonvolatile random access memories (NvRAMs).[1,2] A one transistor-one capacitor (1T-1C) memory cell structure has been proposed to accomplish very large scale integration of ferroelectric memory devices.[3] This requires the bottom electrode of the capacitor to be in direct electrical contact with the source/drain of the transistor of the memory cell. A few structures investigated for this purpose as shown in Fig. 1(a) require the deposition of separate electrode and barrier layers. The electrode consists of two layers, metal (Pt,Ir,Ru) and conducting oxide (LSCO, YBCO, RuO_2, IrO_2) to improve the degradation properties of $PbZr_{0.53}Ti_{0.47}O_3$ (PZT) ferroelectric capacitors.[4–6] The diffusion barrier can include up to three different layers [TiN/(Ti,Ta)/($TiSi_2$,$TaSi_2$)] due to constraints of diffusion, oxidation resistance as well as adhesion.[7] These structures are complicated, require the deposition of four/five different layers and also suffer from problems of adhesion as well as oxidation of the TiN layer for processing temperatures greater than 500 °C.

In this letter, we report a novel multilayer electrode-barrier structure which has good electrical conductivity, high temperature stability, acts as an excellent diffusion barrier up to high processing temperatures (~700 °C), provides excellent adhesion with the ferroelectric/substrate, significantly reduces the degradation problems of fatigue and leakage current associated with PZT thin film capacitors and has tremendous potential for integration in the high-density memory cell structure. Figure 1(b) shows the schematic of the multilayer electrode structure. The electrode structure consists of a bottom platinum-rhodium-oxide layer (Pt–Rh–O_x) in contact with the substrate, an intermediate Pt–Rh metal layer and a top Pt–Rh–O_x layer in contact with the ferroelectric layer. The three layers of the electrode barriers are deposited using an *in situ* sputtering process consisting of sputtering the bottom oxide layer in Ar+O_2 ambient, the metal layer in pure Ar atmosphere and finally the top oxide layer in the Ar+O_2 ambient. Specifically, the electrode deposition conditions were as follows: The electrodes were deposited in a rf sputter system (Cooke Vacuum Products) using a Pt-10% Rh alloy target (2 in. diam/0.125 in. thick). The electrodes were deposited at a substrate temperature of 450 °C and at rf power of 50 W. The gas pressure used was 5 mTorr for pure Ar and 7 mT for Ar+O_2. The Ar/O_2 ratio was kept constant at 20:4 sccm. The deposition times were 3,

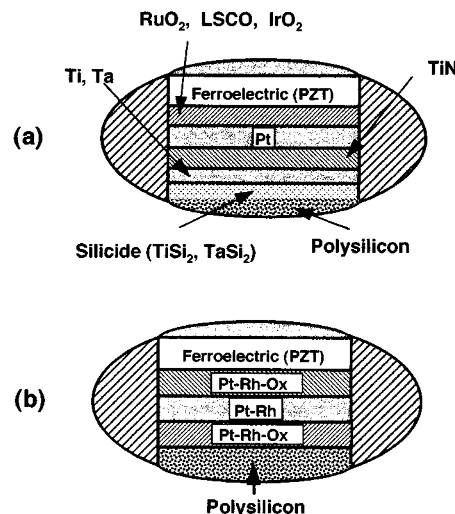

FIG. 1. Schematic of the magnified view of the capacitor on the source/drain of the transistor in the 1T-1C structure for (a) structure using separate electrode and barrier layers and (b) proposed novel electrode-barrier structure.

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17, and 6 min for the top, intermediate, and bottom layers, respectively. The electrodes were deposited directly on single crystal n^+ Si(100) and n^+ polycrystalline(poly)silicon/SiO_2/Si substrates. The substrates were cleaned and degreased and the surface H-passivated by using a HF acid treatment. The substrates were then immediately transferred to the sputter chamber to minimize any native oxide formation. Following the bottom electrode deposition, MOD derived PZT film of the composition $PbZr_{0.53}Ti_{0.47}O_3$ was deposited from a metallorganic precursor, preparation details of which are described elsewhere.[8] The thickness of the PZT film was determined by spectroscopic ellipsometry to be approximately 3000 °A. The films were then annealed at 650 °C for 30 min in a quartz tube furnace under flowing oxygen to accomplish crystallization of the perovskite phase in the PZT film. Next, the top electrodes were deposited through a shadow mask by sputtering, having identical structure and deposition conditions as the bottom electrodes and the specimens were then annealed at 600 °C for 30 min. The top electrode area was approximately $3.0\sim10^{-4}$ cm^2.

The composition and thickness of the electrode films was determined using the Rutherford backscattering spectroscopy (RBS) technique. The phase formation and orientation in the PZT film was studied using x-ray diffraction (XRD). The morphology of the films was examined using atomic force microscopy (AFM). The ferroelectric properties (hysteresis and fatigue) of the capacitor structures were determined by using the RT66A ferroelectric tester from Radiant Technologies (Albuquerque, NM). The dc leakage current of these capacitors was determined using the Kiethley 617 programmable electrometer.

Results of the RBS studies on the as-deposited electrode films confirmed the oxide layer formation at the surface (top) and the electrode/substrate interface (bottom) due to reactive sputtering. The RBS simulation results indicate that there are three distinct layers in the deposited films, as expected. The bottom layer adjacent to the substrate is an oxide layer having the atomic composition Pt:Rh:O=66:14:20, the intermediate layer is a metallic layer of composition Pt:Rh=87:13 and the top oxide layer having the composition Pt:Rh:O =50:20:30. The thickness of these layers corresponding to the deposition times of 3, 17, and 6 min was determined to be 15, 50, and 30 nm, respectively. Based on the compositional results we cannot conclude conclusively whether the film is a complete mixed oxide film or a mixture of metallic and oxide components. The resistivity of the multilayer electrode-barrier films measured using the four-point probe was determined to be in the range of 18–24 $\mu\Omega$ cm, indicating that the multilayer electrodes had comparable resistivities to the metallic films.

Figure 2 shows the RBS spectra of the multilayer electrode film as well as Pt film on n^+ Si substrate after annealing at 700 °C for 60 min in flowing O_2. The results clearly demonstrate that there is no significant interdiffusion between the Pt–Rh and Si as compared to the Pt/Si case (both the Pt and Si edges have shifted considerably). This indicates that the Pt–Rh–O_x layer acts as a very good diffusion/reaction barrier up to processing temperatures of 700 °C. The XRD data for the multilayer electrode films deposited on Si substrate did not show any new peaks as compared to Pt corresponding to Pt/Rh silicides after annealing at 650 °C demonstrating the barrier effect of the Pt–Rh–O_x layer. Morphological examination of the electrodes using the AFM showed that the electrodes have a uniform and a very fine grained structure with an average grain size of approximately 400 °A. In addition, no hillock formation was observed for these electrodes after annealing at 650 °C and the average surface roughness R_a determined from the AFM data was only 0.68 nm. Figure 3 shows the XRD pattern for the PZT film deposited on the bottom electrode/Si (100) structure and annealed at 650 °C for 30 min in O_2 atmosphere. As observed from the XRD pattern, it appears that the films have predominantly crystallized in the ferroelectric perovskite phase. The films do not appear to have any preferred orientation. The PZT films have an average grain size of approximately 800 °A as observed from the AFM micrographs. An important point to note here is the extreme smoothness of the PZT films which have an average roughness R_a value of only 1.31 nm due to the smooth and fine grained textured of the underlying electrodes (R_a=0.62 nm), as compared to films deposited on Pt electrodes due to the hillock formation problem of the underlying Pt electrodes.[9] Therefore the multilayer electrodes have a significant advantage when used for thinner films of PZT as compared to the Pt electrodes.

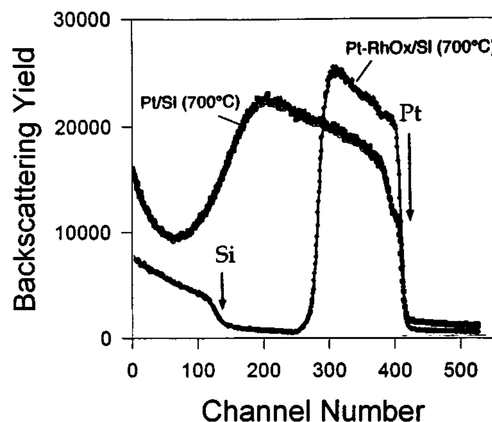

FIG. 2. RBS spectra of the multilayer electrode-barrier film and Pt film on n^+ Si (100) after annealing at 700 °C for 60 min in O_2.

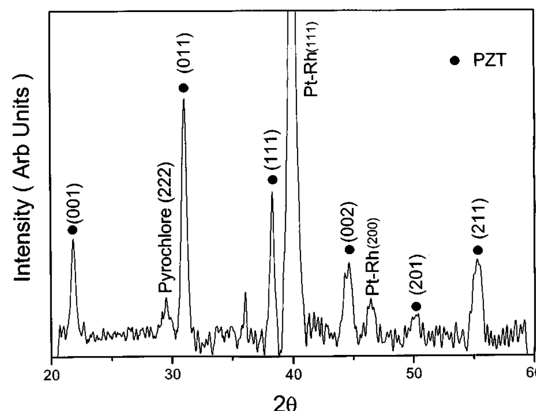

FIG. 3. XRD pattern of the PZT film deposited on the electrode-barrier/n^+ Si (100) structure and annealed at 650 °C for 30 min in O_2.

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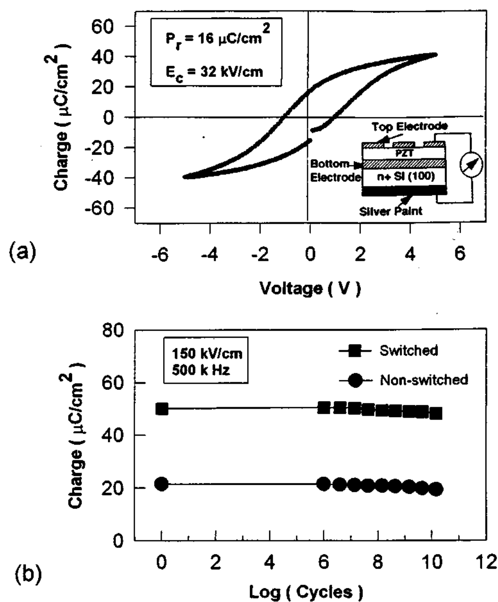

FIG. 4. Hysteresis curve (a) and fatigue behavior (b) of test capacitors with PZT on electrode-barrier structures deposited directly on n^+ Si (100).

Figures 4(a) and 4(b) show the typical hysteresis curve and the fatigue behavior of the top electrode ($Pt-Rh-O_x/Pt-Rh/Pt-Rh-O_x$)/PZT/bottom electrode ($Pt-Rh-O_x/Pt-Rh/Pt-Rh-O_x$) test structures deposited directly on n^+ Si(100) substrate annealed at 650 °C for 30 min in O_2. The electrical measurements were made through the n^+ Si(100) layer between the top electrodes and the conducting silver paint applied at the bottom of the substrate as depicted in the test structure shown in the inset of Fig. 4(a). The hysteresis loop for these test structures is well saturated and shows the remnant polarization P_r value of around 16 $\mu C/cm^2$. The coercive field E_c is also low and falls in the range of 30–40 kV/cm. The P_r and E_c values for the capacitors deposited on n^+ poly $Si/SiO_2/Si$ and SiO_2/Si structures fall within the same range. The P_r values for PZT films deposited on the multilayer electrodes are lower than the films deposited on Pt electrodes possibly due to the smaller grain size of PZT. Fatigue tests were performed using an externally generated square wave with an amplitude of ± 5 V and a frequency of 500 KHz. In Fig. 4(b), the switched as well as unswitched charge is plotted as a function of log cycles applied to the capacitors. Results of the fatigue testing show that there is no significant fatigue (polarization loss <5%) up to 10^{11} cycles. Figure 5 shows the dependence of the dc leakage current on applied voltage and polarity [top electrode (+) or bottom electrode (+)] for the test structures on n^+ Si (100) substrate. The leakage current increases very slightly up to applied field of 100 kV/cm which is followed by a linear increase up to applied fields of 500 kV/cm (log J v/s $E^{0.5}$ dependence). This behavior is indicative of either a Poole–Frankel or Schottky Barrier controlled mechanism. However, different values of the leakage current with respect to a polarity change during measurement implies that the Schottky barrier is the dominant leakage current mechanism. The leakage current at applied field of 100 kV/cm (3 V) has a low value of 2×10^{-8} A/cm^2 and is comparable to PZT on Pt electrodes.

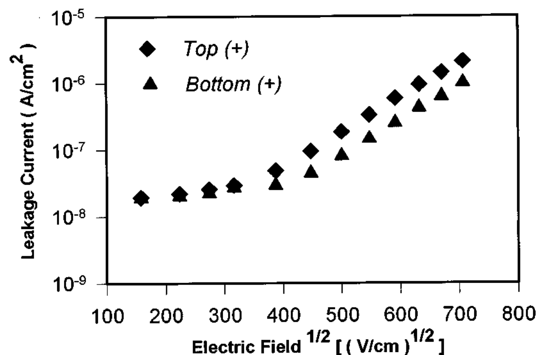

FIG. 5. Dependence of dc leakage current on root applied electric field $E^{0.5}$ and polarity for the test capacitors on electrode-barrier structures deposited directly on n^+ Si (100).

In conclusion, we have successfully fabricated ferroelectric (PZT) test capacitor structures directly on Si [n^+ Si (100) and n^+ poly Si] using $Pt-Rh-O_x/Pt-Rh/Pt-Rh-O_x$ multilayer electrode barriers with excellent ferroelectric and fatigue characteristics. The test capacitors show well saturated hysteresis loops with P_r and E_c of 16 $\mu C/cm^2$ and 30–40 kV/cm, respectively. The capacitors exhibit no significant fatigue loss up to 10^{11} cycles and have low leakage currents (2×10^{-8} at 100 kV/cm). The multilayer electrode structure acts as an excellent barrier between the ferroelectric film and the Si substrate up to high processing temperatures of 700 °C and also significantly improves the degradation properties of these capacitors. The barrier properties of this multilayer electrode structure should make it possible to integrate ferroelectric [PZT, $SrBi_2Ta_2O_9$ (SBT), etc.] or high dielectric constant paraelectric [$Ba_{1-x}Sr_xTiO_3$ (BST), etc.] capacitors in the large scale integrated memory (NvRAM and DRAM) cell structures.

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