Passive Component Weight Reduction for Three Phase Power Converters

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Abstract

Over the past ten years, there has been increased use of electronic power processing in alternative, sustainable, and distributed energy sources, as well as energy storage systems, transportation systems, and the power grid. Three-phase voltage source converters (VSCs) have become the converter of choice in many ac medium- and high-power applications due to their many advantages, such as high efficiency and fast response. For transportation applications, high power density is the key design target, since increasing power density can reduce fuel consumption and increase the total system efficiency. While power electronics devices have greatly improved the efficiency, overall performance and power density of power converters, using power electronic devices also introduces EMI issues to the system, which means filters are inevitable in those systems, and they make up a significant portion of the total system size and cost. Thus, designing for high power density for both power converters and passive components, especially filters, becomes the key issue for three-phase converters.

This dissertation explores two different approaches to reducing the EMI filter size. One approach focuses on the EMI filters itself, including using advanced EMI filter structures to improve filter performance and modifying the EMI filter design method to avoid overdesign. The second approach focuses on reducing the EMI noise generated from

the converter using a three-level and/or interleaving topology and changing the modulation and control methods to reduce the noise source and reduce the weight and size of the filters.

This dissertation is divided into five chapters. Chapter 1 describes the motivations and objectives of this research. After an examination of the surveyed results from the literature, the challenges in this research area are addressed. Chapter 2 studies system-level EMI modeling and EMI filter design methods for voltage source converters. Filter-design-oriented EMI modeling methods are proposed to predict the EMI noise analytically. Based on these models, filter design procedures are improved to avoid overdesign using in-circuit attenuation (ICA) of the filters. The noise propagation path impedance is taken into consideration as part of a detailed discussion of the interaction between EMI filters, and the key design constraints of inductor implementation are presented. Based on the modeling, design and implementation methods, the impact of the switching frequency on EMI filter weight design is also examined. A two-level dc-fed motor drive system is used as an example, but the modeling and design methods can also be applied to other power converter systems.

Chapter 3 presents the impact of the interleaving technique on reducing the system passive weight. Taking into consideration the system propagation path impedance, small-angle interleaving is studied, and an analytical calculation method is proposed to minimize the inductor value for interleaved systems. The design and integration of interphase inductors are also analyzed, and the analysis and design methods are verified on a 2 kW interleaved two-level (2L) motor drive system. Chapter 4 studies noise reduction techniques in multi-level converters. Nearest three space vector (NTSV) modulation, common-mode reduction (CMR) modulation, and common-mode elimination (CME) modulation are studied and compared in terms of EMI performance, neutral point voltage

balancing, and semiconductor losses. In order to reduce the impact of dead time on CME modulation, the two solutions of improving CME modulation and compensating dead time are proposed. To verify the validity of the proposed methods for high-power applications, a 100 kW dc-fed motor drive system with EMI filters for both the AC and DC sides is designed, implemented and tested. This topology gains benefits from both interleaving and multilevel topologies, which can reduce the noise and filter size significantly. The trade-offs of system passive component design are discussed, and a detailed implementation method and real system full-power test results are presented to verify the validity of this study in higher-power converter systems. Finally, Chapter 5 summarizes the contributions of this dissertation and discusses some potential improvements for future work.

To MY FAMILY

My Wife: *Songze Li*

My Parents: *Hui Zhang and Hongying Zhao*

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Chapter 1 Introduction

This chapter starts with an introduction to the motivation and objective of this research, the design and optimization of passive components in power converter systems. After that, the existing research activities in this area are reviewed, which helps to formulate the work in this dissertation and identify its originality. The challenges and the major results to solve the corresponding issues including system-level EMI modeling, EMI filter design, multilevel and interleaving topology analysis are then presented, followed by an explanation of the structure of the dissertation and brief summary of the main contributions of this work.

1.1 Background and Motivations

With pressing demand and limited production of chemical energy resources, such as petroleum and natural gas, energy problems have become more urgent, and have become a focus of people around the world [1]. With a recent emphasis on environmental concerns, there has been an increasing demand for lower fuel consumption in modern transportation applications such as vehicle, aviation and marine [2]. Over the past ten years, there has been increased incorporation of electronic power processing into alternative, sustainable, and distributed energy sources, as well as energy storage systems, transportation systems, and the power grid.

As shown in Figure 1-1 , electrical power is utilized more and more in electric vehicle applications for propulsion purposes. Also, a greater degree of utilization for assistance purposes in aircraft applications is being realized than in previous aircraft generations. For

solar and wind power generation as shown in Figure 1-2, power converters are the key units to process the energy harvested in order to connect with the grid or other loads.

Tesla Pure Electric Car

More electrical aircraft: Boeing 787

Figure 1-1 Electrically intensive transportation applications, www. teslamotors.com, www. boeing.com, 2014, used under fair use, 2014

(a) Solar panel

(b) Wind turbine

Figure 1-2 Solar and wind renewable energy, D. Dong, "Modeling and Control Design of a Bidirectional PWM Converter for Single-phase Energy Systems" Master thesis, Electrical and Computer Engineering, Virginia Tech, Blacksburg, 2009. Used under fair use, 2014

Power electronic converters are trending to replace the traditional mechanical and hydraulic systems. The goals have been to reduce the size, weight, maintenance and operational costs of these power systems, while increasing overall energy efficiency, safety, and reliability. For all the more electrical transportation applications such as vehicle [5,6], aviation [6-8] and marine [10,11], power density becomes the key issue because of the limited space and carrier capability. For the renewable energy applications, power density is also desirable for portability and easy installation for house or building equipment. Even

for renewable energy power plant applications, higher power density means fewer material needed which means a lower cost for the same power generation.

Power electronics has revolutionized the way we process power to meet the growing energy need of our society. The introduction of fast switching power semiconductor devices has greatly improved the dynamic response, efficiency and overall performance of the power converters. Moreover the fast switching power semiconductor devices also provides the opportunity to reduce the size of the power converters and the energy storage components, in other words, reduce system weight/size and increase the power density of the system [12]. The common objectives in the design of these converters are size reduction and increased energy efficiency. While the energy efficiency is mostly being pursued through system-level power management and converter integration [13]-[15], the power density is being addressed by the use of new materials, increased levels of integration, and innovative circuit designs [16]-[24]. Recently increased availability of silicon carbide (SiC) and gallium nitride (GaN) devices has opened new opportunities for designing power converters that operate at increased switching frequencies with higher voltages and lower losses to reduce the size/weight of the passive components for energy storage. Several studies [25]-[28] have shown that using these advanced devices can push the switching frequency of the converters to several mega-hertz for kilowatt level converters. With improved module integration and packaging technologies that reduce parasitics, the power density of the power converters can be improved significantly. However, switching devices bring the electromagnetic interference (EMI) problems into the system [29]. The generated noise current, called conducted EMI noise, travel along the input and output power lines and cause interference with other electronic systems [31]. In order to avoid the inference

between different systems, the EMI noise emissions from the power converters need to be limited and compliance with certain electromagnetic compatibility (EMC) standards is regularly required. EMI filters are inevitable parts in power electronics systems to provide attenuation for the EMI noise. These passive components take a significant portion of the total volume and weight of the converter. In some applications, filters are needed for both input and output of the converter, and the additional EMI filter weight may reduce the benefits of the power electronic converters over traditional systems and even make the total weight/size bigger[32-34]. Moreover, with the increase of the switching speed of the emerging advanced semiconductor devices, the dv/dt and di/dt transitions during the device switching become much higher than in traditional silicon (Si) devices. Hence, the switching energy is moved to higher frequencies, and both conducted and radiated noise emissions become higher than in Si systems, which aggravates the EMI problems [35]. Therefore, it is a big challenge for modern power electronic systems to design and integrate the power converter and EMI filter together to minimize total weight/size and thus improve system power density.

1.2 Conducted EMI Noise and EMI Filters

Conducted emissions are the EMI noise that circulates between the concerned system (power converter in this case) and the external network via the physical connections between them. [36]. The work presented in this dissertation is limited to conducted emissions only, the other type of EMI noise (Radiated EMI noise) will not be included in this dissertation. Although the radiated EMI may be of higher importance. This is often justified in the engineering practice because in many cases a properly shielded power

converter that meets conducted EMI requirements also meets the corresponding radiated EMI requirement.

The production of EMI noise is an inherent problem with power inverters, as has been reported and is a by-product of the method by which ac voltages are synthesized from a dc voltage by force-commutated switches. During the modulation and switching, other than the energy generated at needed frequency, different harmonics will also generated at different frequencies that can interfere with other equipment through the physical connections and become the conducted EMI noise.

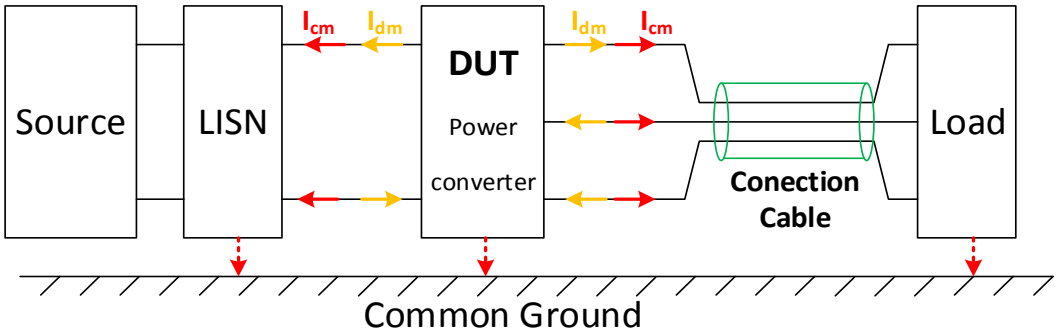


Figure 1-3 EMI noise propagation path in a DC/AC System

Figure 1-3 shows the noise propagation in a power converter (DC/AC) system. Power converter (the device under test (DUT)) is used to process the energy from source to the load, the source could be a dc power supply, dc voltage bus or an active front end and etc., and the load could be a motor or grid and etc. The LISN stands for the line-impedance-stabilization-network which is required to measure and fairly compare the EMI noise per all conducted emissions standards. To analyze the EMI noise and design EMI filters, one can separate the conducted emissions into two types: common-mode (CM) and differential mode (DM). The DM noise (I_{dm} shown in Figure 1-3) flows between the power ports of the converters and The CM noise (I_{cm} shown in Figure 1-3) flows in same direction and then returns via ground connection.

To control the EMI pollution of the system, EMI standards are usually enforce at the input and output of the DUT. For many application, the load is a standalone equipment such as a motor, a resistor or an inductor which has a high noise immunity, the EMI standard is only enforce at the source side to make sure the converter will not influence the working condition of the source or pollute the bus voltage. However, for many other applications, when the connection cable is long, for example, in aircrafts and electric vehicles. The converter will be connected to the load motor with a long cable. The cable will behave as an antenna and the conductive noise will generate radiated noise. Moreover, for renewable energy applications, if the converter is a grid tied converter then the load will be the AC grid or other noise sensitive equipment. Thus, certain conductive EMI standard is also needed between the converter and load [37].

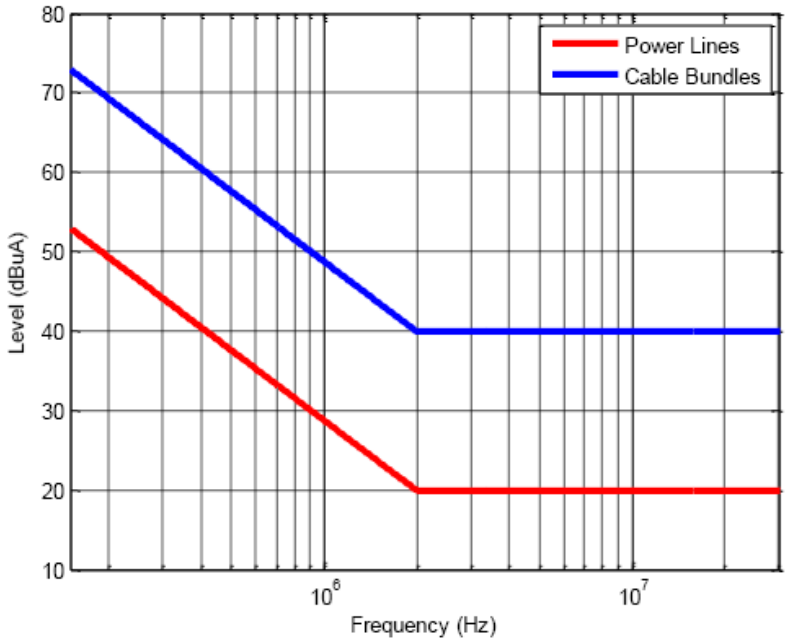


Figure 1-4 Conducted emission limits in DO-160E (Section 21) for L, M &H categories

There are numerous EMI standards for different applications. In this dissertation, the DO-160 standard [37], for conducted emissions in aerospace application (as shown in Figure 1-4) is selected for filter design and analysis. It is based on the total noise current in

one wire, in other words the current noise measured in one wire must not exceed the given limits within 150 kHz to 30 MHz.

To reduce the EMI noise generated from the system and meet EMI standards, EMI filters are effective solutions and inevitable parts in a power converter system[38] . Figure 1-5 shows the system connection for a DC/AC power converter system when EMI filter are needed for both AC and DC sides.

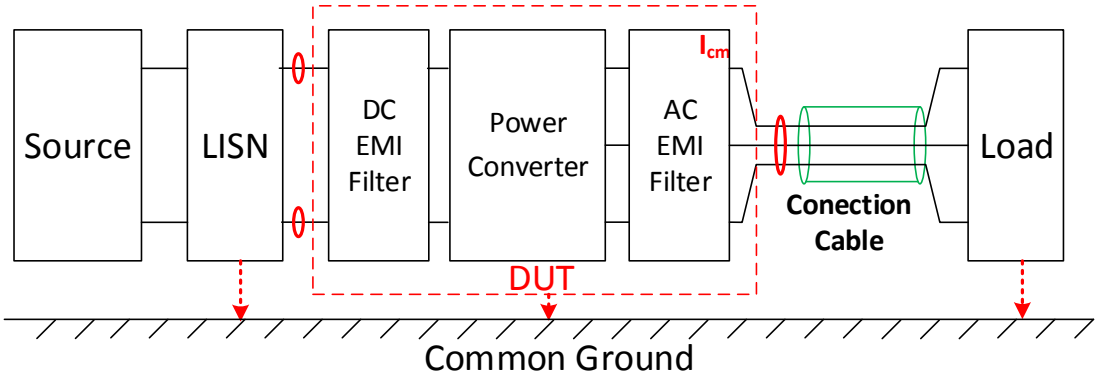


Figure 1-5 DC-AC power converter system with EMI filters

Typical EMI filters are composed with one or several stages of inductors and capacitors to create the impedance mismatch between the power converter and load/source to block and bypass the EMI noise, thus it can reduce the EMI noise propagated to the source and load. However, passive components especially the inductors are heavy and bulky, which make the EMI filter weight take a big portion of the total system weight. For example, for a motor drive system with EMI filter added to both AC and DC sides, the EMI filter weight can take more than 30% to even 50% of the total system weight [39]. Although, electrical power systems can help to reduce the system weight compare with traditional mechanical or hydraulic systems. Due to the special EMI issues, the size and weight of EMI filters must be considered to the system and the size and weight of the total system including power stage and EMI filters is comparable or even bigger if system EMI

problem is not well analyze or EMI filters are not designed properly. Thus how to reduce the EMI noise generated from the system and design EMI filters properly in order to reduce the total system weight and size is a key issue in the power converter design.

1.3 Literature Review

There are mainly two different approaches to reduce the size of EMI filters. One approach focus on the EMI filters itself, including using advance EMI filter structures to improve filter performance and improving the EMI filter design method to accurately predict the performance of the EMI filter and avoid over design of the filters. The other approach is trying to reduce the EMI noise generated from switching of the devices. By changing the switching sequence and the switching behavior of the devices, the converter can generate less noise, thus the attenuation needed from the EMI filters is smaller and the weight and size of the EMI filters can be reduced. This section will first summarize the state-of-the-art in these techniques. The unsolved problems of these techniques are also addressed. Based on the addressed problems, the challenges and objectives of this research are proposed.

1.3.1 System Level EMI Modeling

Design of EMI filters, in principle, should start with a good model of the power converter that is accurate in the EMI frequency range and can be used for predicting EMI noise under different input/output conditions. However extracting such models is not a trivial task as the measured noise levels are sensitive to the geometry of the design and the final geometry will not take shape until at least one prototype of the converter is laid down. Thus design of EMI filters for power converters has been traditionally done using trial-

and-error methods which cannot ensure the optimal EMI filter design. However over the last few decades, several modeling methodologies have been published for extracting EMI models of power converters. They can be classified into two broad categories: detailed lumped-circuit modeling and behavioral modeling.

Detailed lumped circuit modeling in time and frequency domain

The detailed lumped circuit modeling approach is based on the physics of the circuit and is the classical way to model any electronic circuits. It can be done in both time domain and frequency domain. For time domain simulation, every parts of the system can be modeled separately and simulated together using simulation software such as SABER or MATLab/SIMULINK to get the prediction results. For simple converters, such model may be suitable and could provide the most versatile solutions for EMI predictions [40]. The main benefits of lumped circuit models are adaptability and scalability as everything is based on physics. The accuracy of such models for complicated topologies has been found to be good only up to around 10 MHz [41]. However it gets very complex with the increase in number of semiconductor devices and the highest frequency of interest. Figure 1-6 shows an example of the detailed switching model for a three phase motor drive system with only first order resonance modeling.

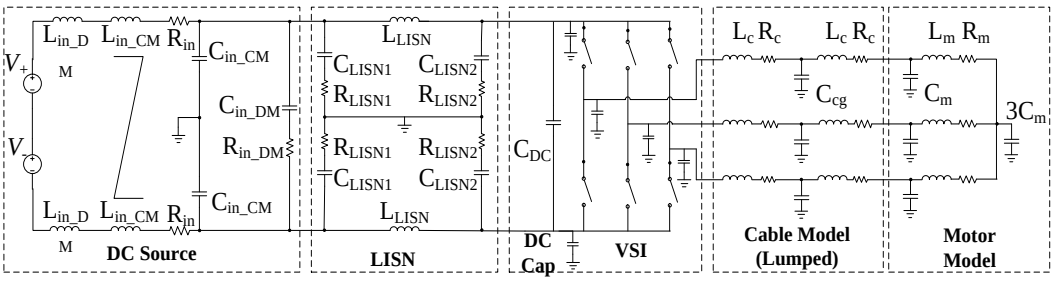


Figure 1-6 Detailed switching model for a three phase motor drive system

The model is very complex and the time domain simulation is also time-consuming. Even with all the details, the model may not work as the simulator can have convergence

issues. [43], which make it less practical for designing EMI filters that may involve numerous simulations. In order to simplify the extraction processes and increase model robustness, engineers started using reduced order models. In such models the devices are replaced by voltage or current sources. Since the devices are used as switches, the voltage across them has an approximately squared shape. However it has been shown that such approximation is not accurate and finite rise/fall time must be included for the better representation of the switched voltage (or current) [45]-[48]. The robustness of such models has been demonstrated in handling complex systems [49]-[52] however it is seen that the accuracy is only good up to several mega-hertz. Reference [44] shows that the approximation of the voltage (or current) switching characteristics with a trapezoidal waveform may not be very accurate either. Attempts have been made to use piece wise linear approximation of the voltage and current though the devices [53]. However, this kind of modeling then becomes specific to the device in use and the accuracy was not seen to be any better than the previous models. Simplified models of IGBT for EMI analysis has also been developed in[54][55]. Here the IGBT is modeled with an ideal switch, an ON resistance and a few capacitances. The accuracy of results was found to good up to only several MHz, most likely because of the limitations of other lumped circuit models that were used to model the system. The reduced order modeling can also be realized in frequency domain. The time domain simulation of the converter, including all the parasitic and noise sources are included in [40][48]. The noise spectrum is then obtained by computing the FFT of the resulting currents. When converter modulation method and operation conditions are known double Fourier integral transformation (DFIT) method can be applied to calculate the frequency domain noise source analytically [56]. This approach

gives good results as long as the switches and circuit models are very close to the real physical devices. This approach provides a simply method for EMI filter design where the noise can be calculated analytically. It is much faster than the time domain simulation which make it a preferred method for EMI filter design where numerous noise prediction processes are involved.

Behavior modeling approaches

Behavior modeling approaches is developed for doing system level EMI predictions. Simulating several converters with detailed lumped circuit equivalents would require large computational resources and time, not to mention that the chances of convergence get severely diminished. Behavior modeling approaches model the whole power converters using a one-port or a two-port network with independent sources[57-59]. With the assumption that the linearity of the converter is still high in EMI range, frequency domain Thevenin (or Norton) equivalents can be derived out of the circuit. Thus the whole circuit is modeled as several noise source with several noise impedances [60][61] (as shown in Figure 1-7).

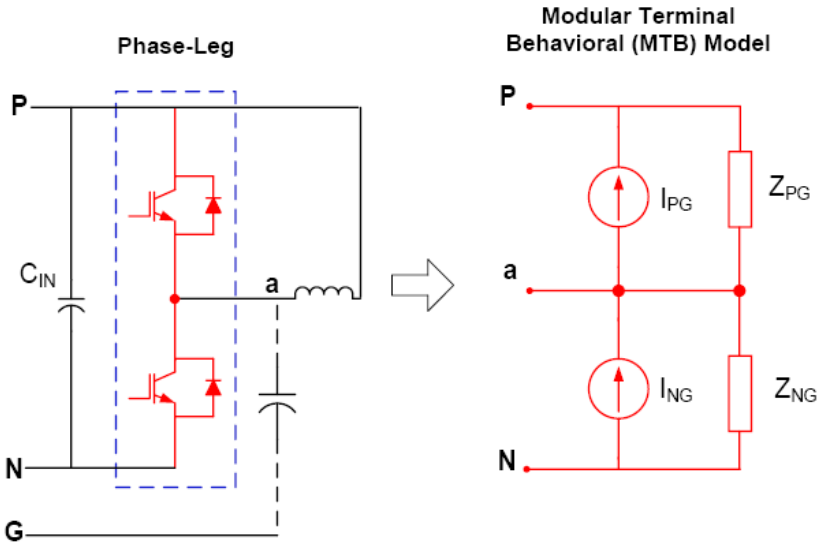


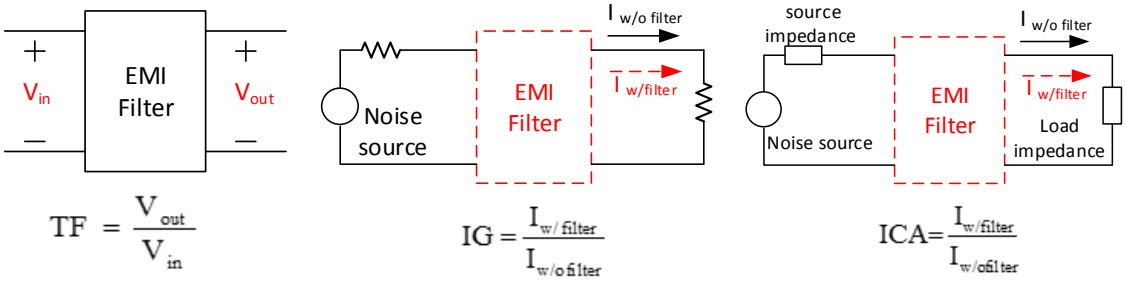
Figure 1-7 Behavioral Modeling for A Two-Level Phase Leg

To derive such models, several measurements are needed for the existing hardware to calculate the noise source and corresponding impedances and numerical optimization may be needed to increase the accuracy of the model. The behavior modeling approach has been applied to phase leg [62], dc/dc converter [63] and three phase dc/ac converters [64]. All the results shows that with proper measurement and numerical optimization algorithms, the accuracy of the model can be achieved up to 50MHz which is good enough for conductive EMI analysis. However, this method need the power converter hardware for measurement to derive an accurate model which make it hard to use for the design and size/weight optimization for the converter and filter together as a whole system since the filter need to be designed before the converter implementation in order to get a minimum weight/size for the power stage and filters together.

1.3.2 EMI Filter Design and Optimization

The EMI filter design methods are evolving with the development of system-level EMI modeling. Without accurate system EMI modeling, design of EMI filters for power converters has been traditionally done using trial-and-error methods which cannot ensure the optimal EMI filters design. Reference [65] proposed a EMI filter design method using the filter transfer gain(TF) (as shown in Figure 1-8(a)) to estimate the filter in circuit attenuation(ICA) (as shown in Figure 1-8(c)) with the assumption that the impedance mismatch has been achieved between the filter input/output impedance and the source/load impedance. This method has been used widely as a practical EMI filter design method. However, due to the existence of resonance source/load impedance and the EMI filter parasitic parameters, the assumption of impedance mismatching cannot be ensured in real system. Thus certain margin is always needed for this design method which cannot provide

the optimal filter design and make the filter over-designed to attenuate the noise effectively. To verify filter attenuation, the insertion gain of the filter (as shown in Figure 1-8(b)) can be measure using a network analyzer [66]. However, this still cannot accurately predict the in-circuit-attenuation of the filter, since the load and source impedance will not be 50Ω constant in the real circuits. Based on the frequency domain modeling of the system such as behavior modeling or reduced order frequency domain modeling, the source and load impedance can be included in the predicting circuit for filter attenuation, and filter in-circuit-attenuation can be predicted and used in filter design to avoid the filter over-design.



(a) Transfer Gain (TF) **(b) Insertion Gain(IG)** **(C) In Circuit Attenuation(ICA)**

Figure 1-8 Different attenuations for EMI filters

However, the filter design method shown above only gives the optimized value for L and C in the filter. To get the real weight/size of the filters, the physical implementation of each component needs to be consider. There are two main issues during the implementation of filters: saturation of inductors and parasitic parameters of EMI filters. To make inductor maintain the inductance during system operation, inductors must be designed to avoid saturation. Volt-second applied on the inductors is the main reason for inductor saturation. With the consideration of volt-second generated in the system, sometimes the optimized inductor and capacitor value cannot guarantee an optimized filter weight [69]. Component parasitic parameters are also very importance for filter high frequency performance [70]-[73]. Many studies has been presented to either estimate the parasitic parameters of

inductors and capacitors [71]-[75] or to cancel them using circuit theories [77]. All the studies showed that the parasitic components must be controlled during the implementation of EMI filters to ensure high frequency performance.

Although many research have be conducted to systematically study the impact of the EMI filter on the power density of three-phase PWM converters, and the design method for a high density EMI filters [77]. The filter design method still follows the process of getting the "optimized" filter parameters first then design and implement the "optimized" filter based on the "optimized" filter parameters. However, as the volt-second issues discus above, sometimes the optimized inductor and capacitor value cannot guarantee an optimized filter weight. To get the global optimum weight/size of the EMI filter, the design method should consider the parameter selection and physical implementation together.

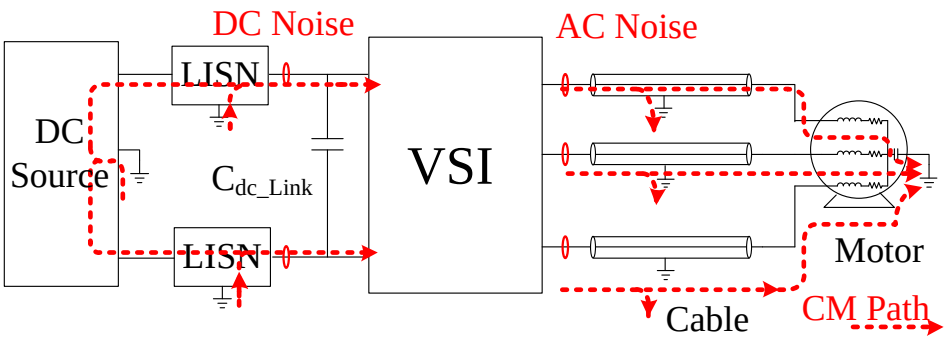


Figure 1-9 CM noise propagation path for dc-fed motor drive system

Moreover, previous works only focus on EMI filter design method for one side of the converter. For application that need EMI filters for both AC and DC sides, the interaction between AC and DC EMI filters must be considered, especially for CM noise as shown in Figure 1-9. Certain design sequence is needed to ensure that adding another filter into one side of the system will not make the noise on the other side worse and fail the filter design for the other side. How to design the filter properly to ensure effective attenuation for both AC and DC sides is a key issue for motor derives or grid tied converters.

1.3.3 Noise Reduction Using Active Devices.

The reduction of EMI filter weight/size can also be achieved by reducing the noise generated from the system using active devices. These approaches can be divided into two types. One is using auxiliary circuit to inject the noise with the opposite direction according to system noise to compensate the noise generated from the system [78]-[81] . The auxiliary circuits is only for noise reduction, thus it is lower power and smaller size and behave as an active filter. However the active filters still take a portion of system weight and the reliability and fault tolerance of active filters is still a key issue in system design [82]. Another approach to reduce EMI noise generated from the system using active devices is to change the topology and modulation scheme of the power converters to reduce certain types of EMI noise, such as adding an additional phase leg to cancel CM noise generated from the system [83], using multilevel converters that can reduce the voltage step during each switching to reduce both CM and DM noise [84][85]and use parallel and interleaving topology to cancel certain order noise harmonics[87]- [91]. Since this dissertation is aiming at the application power level is from several kW to hundreds of kW, multilevel and interleaving topology is studied in detail for system passive weight reduction.

Multilevel converters

EMI noise is a by-product of the method by which ac voltages are synthesized from a dc voltage by force-commutated switches. It is highly related with the dv/dt during device switching, thus reduce the voltage steps can reduce both CM and DM noise generated from the system. This is the main ideal of using multilevel converters to reduce EMI noise. There has been many of well-established multilevel converter topologies, such as the neutral point clamped (NPC), cascaded H-bridge(CHB), and flying capacitor (FC). In the power level

on several kW to hundreds of kW, three level NPC voltage source converter (as shown in Figure 1-10) is widely used [93] .

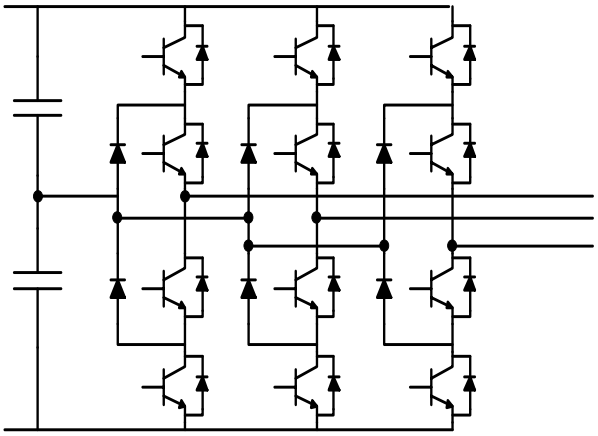


Figure 1-10 3L DNPC Topology

In a NPC 3L inverters, since each phase leg have three output voltage level: $+V_{dc}/2$ (P), 0 (O), $-V_{dc}/2$ (N), there are totally 27 switching states and 18 different output voltage vectors as shown in Figure 1-11.

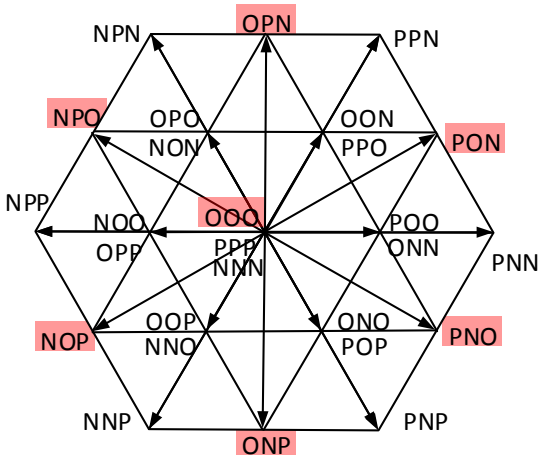


Figure 1-11 Switching states in 3L DNPC VSI

There have been many publications about the modulation methods for NPC 3L inverters, different optimization goals such as minimum loss, minimum CM voltage generation or minimum harmonic distortion can be achieved by using the redundant switching states. Previous work has demonstrated how the additional choices in switching states of the NPC converter provide many opportunities for optimizing a system to get low

differential mode harmonic performance, minimum dc-link ripple current, known as nearest three space vectors (NTSV) modulation [94]. To reduce the EMI filter size, the additional choices in switching states of the NPC converter also provide the options to reduce the common mode (CM) output voltage generation known as common mode reduction (CMR) modulation [95][96] and also can theoretically eliminate the common mode voltage referred as common mode elimination (CME) modulation [97]. Although those modulation methods are widely used to reduce filter size, no comprehensive comparison was presented in the previous literatures to evaluate the performance of these three modulation methods on EMI performance, neutral point voltage ripple and system loss . Reference [98] compared NTSV modulation and CME modulation in the aspect of CM voltage generation. However, the comparison was only done in time domain and low frequency range and the EMI performances are not compared.

By selecting the switching states properly in 3L DNPC converters, reference [97]specifically proposed a modulation method that can theoretically eliminate the CM voltage; namely the common-mode elimination (CME) modulation. However the benefits of CM noise elimination can only be achieved with the assumption that the device is ideal. However, when this technique is implemented, due to the need to apply a dead time (DT) period to the gate drive of complementary IGBTs in a phase-leg to avoid shoot-through faults, the final benefit of this modulation technique is quite limited, which on top of the penalty of limiting the voltage utilization ratio of the converter by 15 %, and the loss of neutral-point (NP) voltage balancing capability. All these drawbacks make this modulation method less attractive and less practical for real implementation. Similar with the dead time compensation ideal for 2L converters [99], reference [100]proposed a dead time

compensation method that can be applied for all different modulation method however the compensation focusing on time domain aspects to reduce the output current distortion instead of CM noise reduction. So far, very few initiatives have been conducted or reported to determine the impact of DT on CME modulation. Only a brief compensation method was proposed in [103] however the compensation still focused on time domain aspect and consequently did not exploring the impact on the EMI frequency range. In order to make CME modulation more practical in real system, it is necessary to study the compensation method or explore other modulation methods to reduce the impact of DT on system CM noise reduction in CME modulation.

Interleaving Topology

The use of paralleled three-phase PWM converters dates back to the late 1980s in motor drives [104]and uninterruptable power supply (UPS) applications[105][106]. Although almost 30 years have passed, paralleling with interleaving continues to have many benefits and being used widely. However, most paralleling applications with interleaving are still for dc/dc converters only. Until recently, interleaving operation was not a common practice in paralleling three-phase power conversion. Instead, the paralleled three-phase VSCs are usually controlled in phase, avoiding any phase-shifting in carrier waveforms. This is because there are still some issues not resolved, prohibiting the widespread application of interleaving in the paralleling three phase power conversion. The interleaving concept comes starts from dc/dc application in order to achieve current ripple reduction to reduce the size of the inductor and capacitors. Similar to the analysis of interleaving in dc/dc applications [107][108], the impact of interleaving in a three-phase VSC system is usually analyzed in time domain [114][115]. It is easy to see a ripple current

cancellation effect of interleaving in time domain, but the analysis in time domain lacks insight. Recently, people started to study the impact of interleaving on a paralleled three phase VSCs system in frequency domain [88-91][109][110]where both AC and DC are non-isolated to reduce the weight of isolation inductors. Figure 1-12 show a system connection of interleaving 3P converters with both common AC and common DC sides.

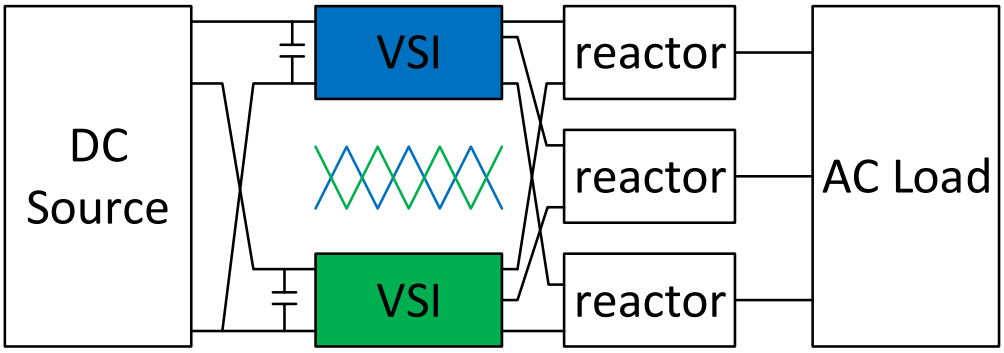


Figure 1-12. Interleaved three phase converters with both common AC and common DC sides

Using the double integral Fourier analysis method [111], the output ac harmonic currents cancellation effect of interleaving for N parallel three-phase VSCs system has been analyzed and verified theoretically [112]. The impact of the non-conventional interleaving is also discussed in [88-91] [110]and used in [113].Considering system EMI filter design, asymmetric interleaving has been proposed to reduce system EMI noise [116]. However, the optimal interleaving angle is selected on a sweeping method rather than analytical analysis and during the analysis, interleaving angle is selected to get minimum inductor value rather than EMI filter weight, where the trade-off between noise reduction and system volt-second reduction is not considered.

By phase shifting the voltage output of the converter, circulating current will be generated if no impedance appears between the two converters. Traditionally, an isolation method is used to block such circulating current. Separate ac or dc power supplies [117]-[120]or a transformer-isolated ac-side [121]-[124] is configured. With this approach, the

overall paralleling system is bulky and expensive because of the additional power supplies or the ac line-frequency transformer. Another choice of passive component is a high impedance reactor as shown in Figure 1-12. Many works have dealt with the low frequency circulating currents [125]-[130] and proved that the low frequency circulating current is fully controllable for either continuous or discontinuous PWM .Inter-phase inductor and CM inductor are often used to provide high impedance in the loop of circulating current [131]-[134]. When interleaving is used, a high frequency CM circulating current will be introduced which may increase the size of such reactor. Reference [88] discussed and compared different types of interphase inductors such as coupling inductors and CM chokes which showed that reverse coupled inductors or inter-phase inductors are more effective for high frequency circulating current suppression than CM chokes. However, those reactors are still heavy and bulky compared with other components in the paralleling system, it is very important to design the structure of such a reactor carefully to limit the circulating current efficiently and make them as small and light as possible. Previous papers has already analyzed some design and optimization for such coupled inductors [88],[135], however the analysis is mainly focus on the design and optimization of interphase inductor alone or the integration of interphase inductor and boost inductor. For some applications that needs EMI filters, how to integrate coupled inductor with DM or CM filter inductors and how to reduce the total weight is very importation for improving system power density.

Interleaving and multilevel topologies have different impact on system EMI noise reduction. Multilevel converters can reduce voltage step during devices switching and reduce EMI noise for the whole frequency range. However, by selecting different

interleaving angles, interleaving topology can reduce or cancel certain order harmonics. Thus if combining three level and interleaving topology together, there will be more freedom to control system noise source and reduce filter weight. Previous studies were mainly focused on dc/dc or single phase interleaved three level topologies [136][137] and the analysis were also focused on time domain ripple reduction, there has been no study focused on three phase three level interleaving topologies and the impact on system noise reduction and filter weight reduction is not clear.

1.4 Challenges and Objectives

The target of this dissertation is to analyze and compare different topologies and control methods using active devices to reduce system EMI noise source. Meanwhile develop a systematical EMI filter design method to reduce the weight and size of passive components for voltage source converters with EMI filters for both AC and DC sides. As discussed above in this section, there are many unsolved issues existing in this area. The most challenging works are summarized below in three different aspects:

(1) System-Level EMI modeling and filter design methods

Many system-level EMI modeling methods were proposed for system EMI noise prediction, however, those models either need a converter designed and built before EMI filter design process or they are too complex to use for designing EMI filters. An easy and fast modeling method is needed for EMI filter design and performance estimation before the power stage implementation. Moreover, practical EMI filter design methods either use transfer gain or insertion gain of the filters to predict performance, however, none of them can really get the accurate prediction results. With the load and source impedance information, a systematical EMI filter design method is needed using the filter in circuit

attenuation to accurately predict the performance of the filters to avoid overdesign. For some applications that need filter for both input and output sides, different filters will interact with each other. Adding filters will change the performance of the filters that have already been designed. Thus, the design method for both input and output sides is needed with the consideration of the interaction between EMI filters.

(2) Noise reduction methods in three level neutral point clamping voltage source converter

Due to the increase of available voltage vectors in 3L NPC VSI, different optimization goals can be achieved by selecting different redundant voltage vectors. However, most of the modulations methods focus on just one aspect of the optimization and not really on system EMI performance, there is no comprehensive comparison of the modulations methods for three level NPC VSI. Moreover, CME modulation provides a promising reduction on system CM noise reduction, however, the benefit is highly related with the dead time added to the system, which make this modulation less practical in real system. Since dead time is necessary for the safety operation of the system. Improvement is needed to reduce the impact of DT on system CM noise reduction for CME modulation.

(3) Impact of interleaving on system EMI filter weight reduction

Previous literatures studies the impact of interleaving on energy storage components in power converter systems. Although some literature also showed some benefits on system EMI filter reduction using small angle interleaving, the optimal angle selection methods is not clear. Moreover, since the interleaving introduce circulating current in the system, larger boost inductors or additional inductors are needed to limit the circulating current. Such penalty may cost all the benefits on EMI filter weight reduction and make

interleaved system even heavier than non-interleaved system. However, the analysis for such penalties is missing, thus it is important to explore the boundary of the benefit of interleaving system to show the limitation under which interleaving is beneficial to total system weight and size.

1.5 Dissertation Layout

This research report is organized as follows:

Chapter 2 studies the system-level EMI modeling methods and EMI filter design methods for a two level dc-fed motor drive system. First a filter design oriented system-level EMI frequency domain modeling method is proposed where the source and load impedance in the model can be calculated from the detailed switching model or measured directly from the system. The frequency domain noise sources can be calculated analytically using double Fourier integral transformation (DFIT) method. Based on this model, the interaction between AC and DC EMI filters are analyzed in detail. With this consideration, A EMI filter design method using predicted in-circuit-attenuation (ICA) is proposed for designing both AC and DC side EMI filters together. Then, a new filter structure is proposed which connects the AC and DC neutral points to attenuate both AC-side and DC-side noise at the same time. Moreover, based on the EMI noise prediction model and filter design methods, the impact of the noise propagation impedance and converter switching frequency on EMI filter weight/size is discussed in detail. A 1.5kW two level three phase voltage source inverter is developed to verify the analysis and proposed design methods.

Chapter 3 presents the impact of interleaving technique on system passive weight reduction. Starting from a DC/DC high power PV converters, the benefit of interleaving

on input inductor weight reduction is analyzed in detail. Then, analysis is focused on the impact of interleaving on system passive weight reduction for three phase converters. The analysis is presented in frequency domain using DFIT method. The impact of interleaving on system voltage noise source spectrum is calculated analytically and its impact on EMI filter design is presented. Since system propagation path impedance dominate the shape of EMI noise thus it has significant impact on EMI filter design, small angle interleaving is proposed to reduce the noise source according to the system impedance resonance in EMI range to reduce the attenuation needed for EMI filters. Since interleaving creates the circulating current problems that need additional interphase inductors. The design and integration method of interphase inductors are also analyzed in detail. A 3kW two level three phase interleaved voltage source inverter is developed to verify the proposed design methods and analysis.

Chapter 4 studies the noise reduction methods in multi-level converter. The three level (3L) diode neutral point clamped (DNPC) voltage source inverter (VSI) is analyzed in detail. Different modulation methods (nearest three space vector (NTSV) modulation, common mode reduction (CMR) modulation, common mode elimination (CME) modulation) are studied and compared in the aspect of system EMI performance (especially on system CM noise emission), neutral point voltage ripple and semiconductor losses. The neutral point voltage balancing methods are discussed in detail. The results show that with ideal switches, CME modulation can reduce the CM noise more than 20dB up to 2MHz. However, the reduction is highly dependent on the dead time added to the system. Which make the CME modulation less practical in real implementation. The DT compensation method is proposed to solve this problem, which can reduce the impact of DT on CM noise

emission significantly. Moreover, an improve CME modulation is also proposed to reduce the impact of DT. A 3kW three level three phase voltage source inverter is developed to verify the proposed design methods and analysis.

Based on the analysis and design results of chapter 2, 3, 4. A 100 kW dc-fed motor drive system with EMI filters for both input and output sides are designed, implemented and tested. Since interleaving and three level topologies have different impacts on system noise source reduction, they have different benefits on passive weight reduction when system operation condition is different. Combining the analysis of three level and interleaving topology, a three level interleaved system with two 3L DNPC VSIs interleaving topology is selected as the power stage. The detailed design and implementation results along with the real system 100 kW test results are shown in Chapter 4 which verifies the proposed analysis and design for higher power systems.

Chapter 5 concludes the entire dissertation, summaries the main contributions and discusses some ideas for future work.

Chapter 2 System-level EMI Modelling and Filter Design Methods

2.1 Introduction

Electronic power processing technologies that are being developed now have a potential to revolutionize the way electricity is generated, distributed, and used. However, switching devices bring the electromagnetic interference (EMI) problems into the system. The generated noise currents, called conducted EMI noise, travel along the input and output power lines and may, in turn, cause interference with other electronic systems. In order to avoid the inference between different systems, the EMI noise emissions from the power converters need to be limited and certain electromagnetic compatibility (EMC) standards is regularly required. EMI filters are inevitable parts in power electronics systems to provide attenuation for the EMI noise. These passive components take a significant portion of the total volume and weight of converters. In some applications, filters are needed for both the input and output sides of the converter, and the additional EMI filter weight may reduce the benefits of the power electronic converters over traditional systems and even make the total weight/size bigger [31, 32]. Therefore, it is a big challenge for modern power electronic systems to design the power converter and EMI filter together to minimize total weight/size and improve system power density.

This chapter presents a detailed analysis of the system-level EMI modeling and filter design methods for three phase power converters. A filter design oriented frequency domain system-level EMI modeling method is proposed for EMI noise prediction before system implementation, where the source and load impedance in the model can be

calculated from the detailed switching model or measured directly from the system and the frequency domain noise sources can be calculated analytically using double Fourier integral transformation (DFIT) method.

With this model, the impact of propagation path impedance on EMI noise emission is analyzed in detail. An improved filter design method using filter in circuit attenuation rather than transfer function is proposed to improve the design accuracy and avoid overdesign.

Based on the proposed model, the interaction between ac and dc EMI filters is also analyzed in detail. With this consideration. A EMI filter design method using predicted in-circuit-attenuation (ICA) is proposed for designing both ac-side and dc-side EMI filters together. Then, a new filter structure is proposed which connects the ac and dc neutral points to attenuate both ac-side and dc-side noise at the same time.

Moreover, based on the EMI noise prediction model and the filter design method, the impact of the noise propagation impedance and converter switching frequency on EMI filter weight/size is discussed in detail. A 1.5kW two level three phase voltage source inverter is developed as an example to verify the theoretical analysis and proposed modeling and design methods.

2.2 Filter Design Oriented System Level EMI Modeling in Frequency Domain

To improve the power density of the whole system, EMI filter design should be considered before the implementation of the power stage. Detailed time-domain switching model is usually used to predict the EMI emissions. However, simulation of detailed switching models usually use small simulation time step to ensure the accuracy of the

simulation results in EMI frequency range which makes the simulation of detail switching usually problematic on convergence and simulation time. Several frequency-domain prediction models have been proposed to solve those problems. However, the noise sources (especially CM noise source) were not defined completely in previous work, which give hard time on accurate EMI prediction. Moreover, because all conducted EMI standards start at frequencies below 1 MHz, and practically all power converters generate the strongest EMI noise components in the same low-frequency range, the EMI filter must be designed to provide the necessary attenuation in this range. Fortunately most converter components have relatively simple linear characteristics in at these frequencies, and many circuit waveforms can be derived analytically with relatively high accuracy. In order to estimate EMI filters weight before the implementation of the power stage to consider the system weight including filter and power stage weight together, models for design purposes are needed. Thus, to improve the power density of the whole system, a simple EMI prediction model that has enough accuracy in low frequency (up to MHz) is needed to design the EMI filters before the system being built.

This section proposes a simple frequency-domain model to predict the EMI noise emissions in motor drive systems for designing EMI filter before the system being built. Double Fourier Integral Transformation (DFIT) method is used to identify the DM and CM noise sources. When system topology, modulation scheme and modulation index are fixed, system EMI noise can be calculated in frequency domain, which is much faster than switching model simulation. Verifications are carried out through simulation and experiment system by comparing the calculated EMI spectrums with simulated and measured EMI spectrums.

2.2.1 Analytical Derivation of the Equivalent Circuits for a Single Phase Leg

The frequency domain equivalent circuit of a power converter for system level EMI analysis can be analytically derived from the time domain operation of the system with certain simplifications. Figure 2-1 shows the lumped model of a half bridge DC-AC converter where L and R represents the load inductor and load resistor, C represents the dc link capacitor, V_{dc} represents the dc source and R_{dc} represents the resistance of the dc source, two switch S_1 and S_2 will switch with a complementary pattern under a sinusoidal modulation and output the AC voltage in the output side.

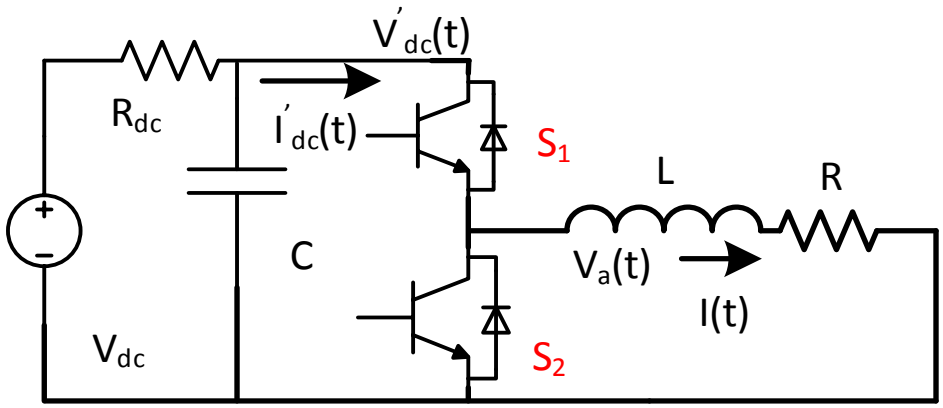


Figure 2-1. Lumped model of a half bridge DC-AC converter

Assuming the switch action happens instantaneously, the circuit operation can be modeled using the switching function of the phase leg, thus, the circuit can be modeled as shown in Figure 2-2.

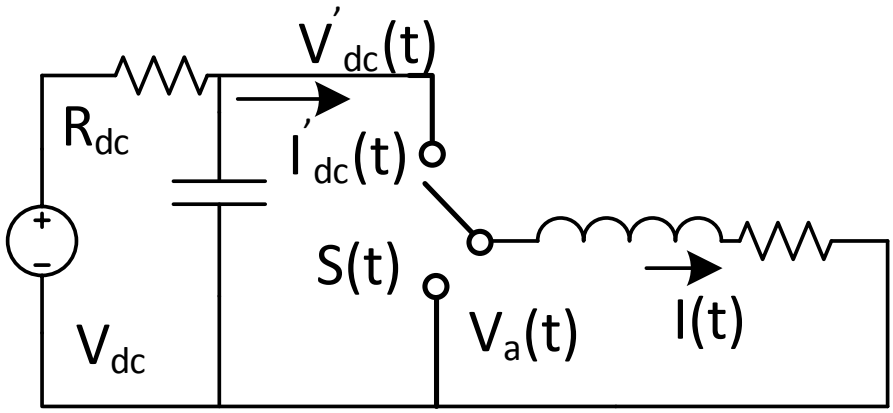


Figure 2-2 A half bridge DC-AC converter with switching functions

The switching function of the phase leg is defined as

$$s(t)=\begin{cases}0 & \text{when } S_1 \text{is open and } S_2 \text{ is close}\\ 1 & \text{when } S_1 \text{is close and } S_2 \text{ is open}\end{cases} \tag{2-1}$$

Thus, at any time the voltage and current relations between AC and DC sides can be expressed by using the switching function S(t) as shown in (2-2),

$$\begin{cases} i_{dc}(t) = s(t)i(t) \\ v_a(t) = s(t)v_{dc}'(t) \end{cases} \tag{2-2}$$

The remaining circuits can be modeled as shown in (2-3)

$$\begin{cases} v_a(t) = i(t)R + L\dfrac{di(t)}{dt} \\ \dfrac{V_{dc} - v_{dc}'(t)}{R_{dc}} - C\dfrac{dv_{dc}'(t)}{dt} = i_{dc}(t) \end{cases} \tag{2-3}$$

Take equation (2-2) into (2-3). The time domain mathematical model of the whole converter can be derived as shown in (2-4), and this mathematical model holds for any time during the operation of the converter.

$$\begin{cases} s(t)v_{dc}'(t) = i(t)R + L\dfrac{di(t)}{dt} \\ \dfrac{V_{dc} - v_{dc}'(t)}{R_{dc}} - C\dfrac{dv_{dc}'(t)}{dt} = s(t)i(t) \end{cases} \tag{2-3}$$

Convert the mathematical model into frequency domain using Laplace Transformation, then the frequency domain mathematical model is shown in (2-4), where represents the convolution operation in frequency domain

$$\begin{cases} S(s)\otimes V_{dc}'(s) = I(s)R + sLI(s) \\ \dfrac{V_{dc} - V_{dc}'(s)}{R_{dc}} - sCV_{dc}'(s) = S(s)\otimes I(s) \end{cases} \tag{2-4}$$

From (2-4) one can solve the equation and get the relationship between AC and DC sides as shown in (2-5)

$$S(s)\otimes\left[\frac{V_{dc} - R_{dc}\cdot S(s)\otimes I(s)}{1+sRC}\right] = I(s)R + sLI(s) \tag{2-5}$$

Equation (2-5) represents the equivalent circuit of the half bridge DC-AC converter in frequency domain as shown in Figure 2-3 where V_{source} represents the noise source in the system, sL and R is the impedance of load inductor and resistor, I(s) is the AC side steady state current in frequency domain. This equivalent circuit can be used to calculate the steady state operation status (including EMI noise) of the system.

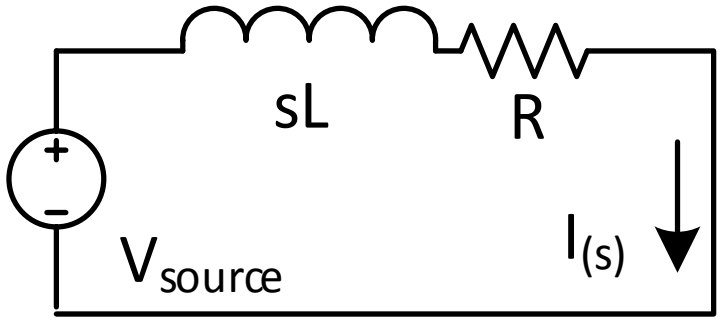


Figure 2-3. Equivalent circuit of the half bridge DC-AC converter in frequency domain

The noise source in the model can be calculated analytically using (2-6) which shows that the noise source is determined by the switching function of the phase leg and the dc link voltage of the phase leg.

$$V_{source} = S(s) \otimes \left[\frac{V_{dc} - R_{dc} \cdot S(s) \otimes I(s)}{1 + sRC} \right] \tag{2-6}$$

The convolution operation involves massive calculations since both switching function and the dc link voltage of the phase leg includes multiple harmonics due to the switching. It is also notice that the dc link voltage expression include a low pass term ($\frac{1}{1+\mathrm{sRC}}$) due to the existence of the dc link capacitor and this low pass filter will attenuate the switching order harmonics of the dc link capacitor to be much lower than DC component. Thus, when the dc link capacitor is big enough, the calculation of noise source in the frequency domain model can be simplified as shown in (2-7)

$$V_{source} = S(s) \otimes \left[\frac{V_{dc} - R_{dc} \cdot S(s) \otimes I(s)}{1 + sRC} \right] \approx S(s) \otimes V_{dc} = S(s) \times V_{dc} \tag{2-7}$$

Where the convolution operation is replaced by a product operation and the dc link voltage is replaced with dc source voltage where all the harmonics are not considered. Then the frequency domain model for AC side noise analysis is simplified as shown in Figure 2-4.

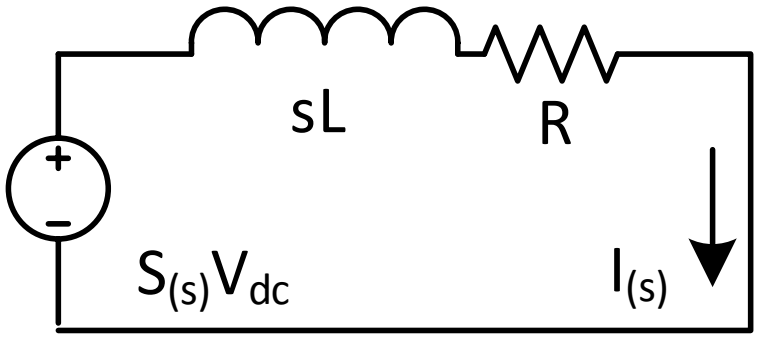


Figure 2-4 Simplified equivalent circuit of the half bridge dc-ac converter in frequency domain

This simplification reduces the complexity and the calculation time of the frequency domain model significantly. It will reduce the accuracy of the model in very high frequency, however if the dc link capacitor is big enough and provide enough attenuation for the dc link voltage harmonics that is required for a normal operation of the converter, the

accuracy is still enough for EMI filter estimation, which will be verified in the following section.

As for the three phase converters, similar derivation can be applied. For a three phase voltage source converter (VSC) system shown as Figure 2-5, the voltage relations between AC and DC side can be expressed by using the switching function S_i of each phase leg and the DC link voltage, as shown in (2-8),

$$V_i = S_i V_{dc\_Link}, i = a, b, c \tag{2-8}$$

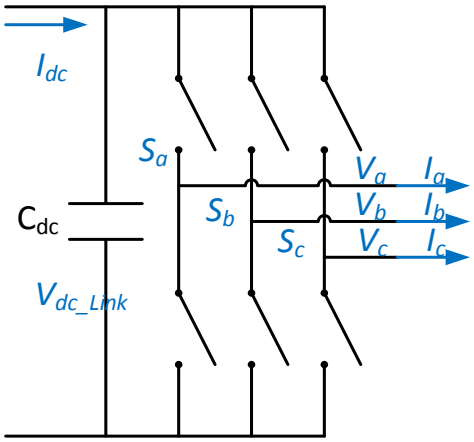


Figure 2-5 Three phase voltage source converter

It is hard to calculate the noise sources in time domain with the switching functions. To get the spectrum of phase voltage, convert (2-8) into frequency domain as (2-9),

$$FFT(V_i) = FFT(S_i) \otimes FFT(V_{dc\_Link}), i = a, b, c \tag{2-9}$$

Applying the same derivation method as shown for half bridge converters, the three phase system can also be modeled in frequency domain. Figure 2-6 shows a simplified time domain model of a three phase voltage source inverter with grounding capacitors.

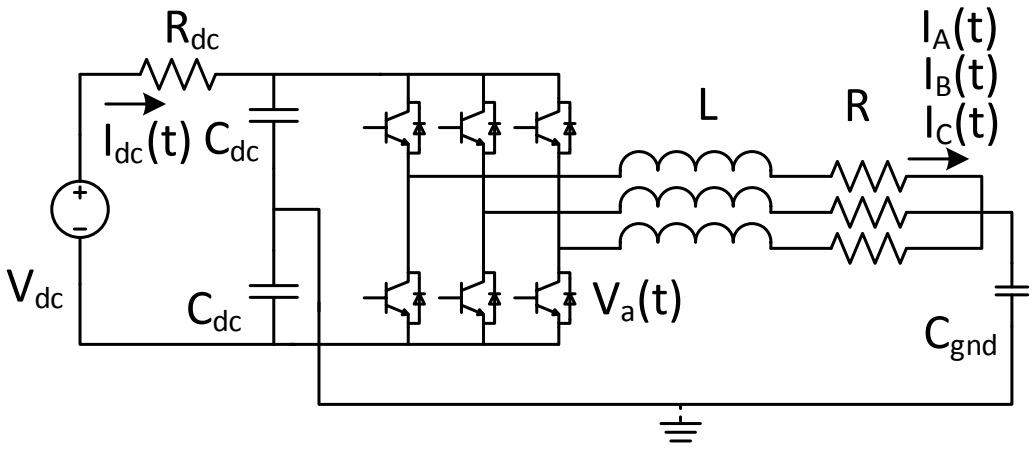
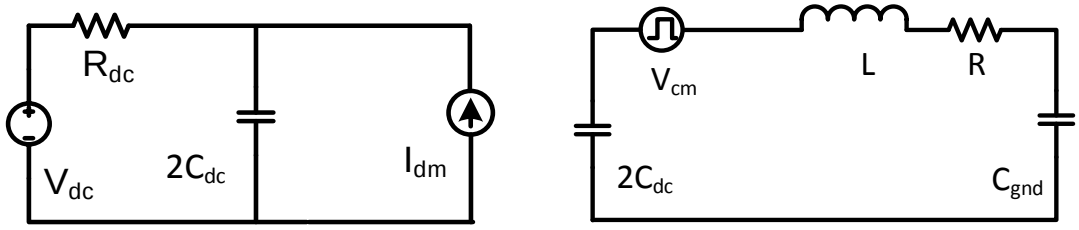


Figure 2-6 Simplified time domain model of a three phase VSI with grounding capacitors

Considering the voltage and current relationship between ac and dc sides, the steady state operation status of the system can also be calculated in frequency domain. Equation (2-10) shows the calculation results of the dc side current in frequency domain

$$I_{dc}(s)=\frac{s\frac{C_{dc}}{2}V_{dc}-\frac{1}{2}\sum_{k=a,b,c}I_k(s)+\sum_{k=a,b,c}S(s)\otimes I_k(s)}{1+s\frac{C_{dc}}{2}R_{dc}} \tag{2-10}$$

It is clear that there is also a low pass filter in the circuit due to the existence of the dc link capacitor, thus the model can be simplified similarly with single phase converter as shown in Figure 2-7(a). Similarly the CM model can also be derived as shown in Figure 2-7(b) and the noise source for the equivalent circuits are shown as (2-11) and (2-12) respectively.



(a) DC DM equivalent circuit **(b) CM equivalent circuit**

Figure 2-7 Frequency domain equivalent circuits

$$V_{CM} \approx \frac{V_{dc} \times \sum_{k=a,b,c}(2S_k(s)-1)}{3} \tag{2-11}$$

$$I_{dm} = \frac{1}{2}\sum_{k=a,b,c} I_k(s) + \sum_{k=a,b,c} S(s) \otimes I_k(s) \tag{2-12}$$

With similar approaches, the frequency domain models can be derived for very complex system. For example, Figure 2-8 shows the lumped model of a dc fed motor drive system with long cables for EMI analysis. The DM and CM equivalent circuits of the system in frequency domain is shown in Figure 2-9 (a) and (b) respectively.

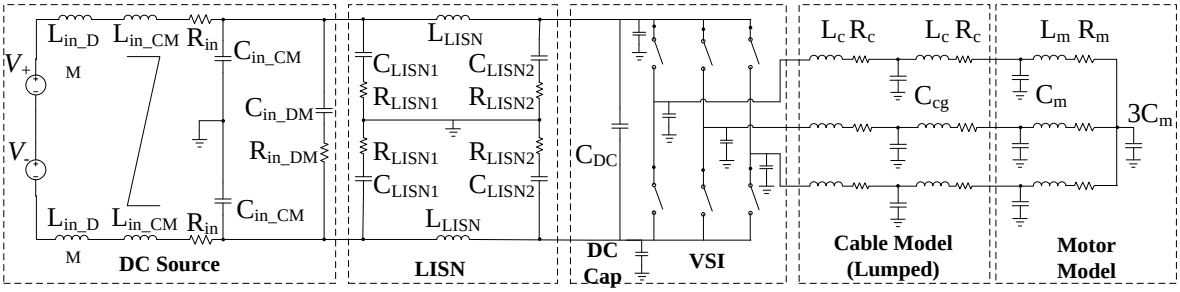
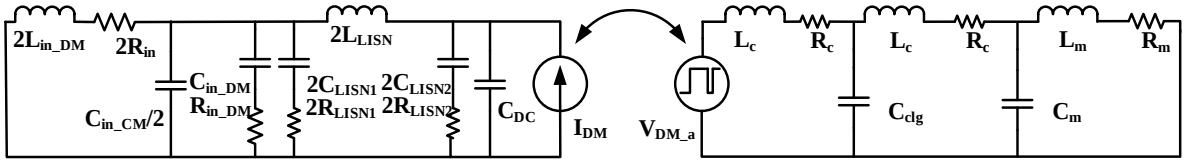
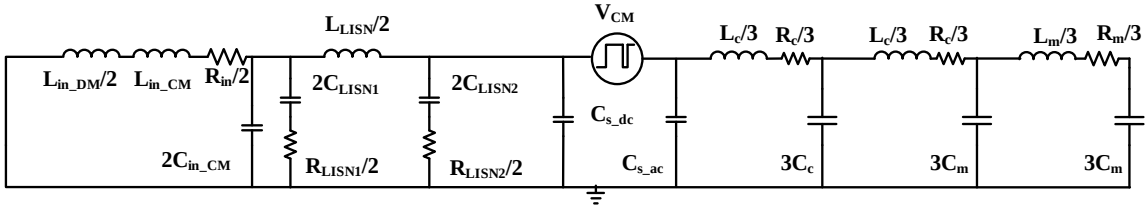


Figure 2-8 Lumped model of a dc fed motor drive system with long cables



(a) DM Equivalent Circuit



(b) CM Equivalent Circuit

Figure 2-9 Frequency domain models of a dc fed motor drive system with long cables

The model shows that for DM noise, due to the presence of the big dc-link capacitor, the ac and dc sides are decoupled for low frequency EMI analysis and the equivalent circuit can be separated for ac and dc sides at certain operation point where the noise source is

determined by the working condition. However, for CM noise, there is no such low impedance path as the dc link capacitor in DM propagation path, the equivalent circuit includes both AC-side and DC-side propagation path impedance and the noise source is also related with the working condition and dc link voltage ripple of the system.

It should be noticed that the propagation path impedance in this modeling technique can be derived from the time domain detailed switching model of the system if there is one, or else it can also be directly measured from the system if the load and source are already available for measurement, which can increase the noise prediction process significantly compared with time domain modeling methods.

2.2.2 Noise Source Calculation Using Double Fourier Integral Transformation

When the propagation path impedance in the frequency domain is derived or measured from the system. The noise source need to be calculated based on the operation condition of the converter (such as switching frequency, modulation scheme and modulation index). When the ratio between device state transition time (turn-on and turn-off time) and the steady state time (on and off time) is relatively small. It can be assumed that devices turn on and off instantaneously, then the voltage changing at the output of the phase leg can be shown as a square waveform. With such assumptions, Reference [56] shows that the spectrum of switching function S_i in frequency domain can be can be decomposed into different harmonics. The frequencies of harmonic components can be expressed as ($m\omega_c$+ $n\omega_0$), where ω_c is the angular frequency of the carrier wave, ω_0 is the fundamental line frequency, and m and n are the carrier and baseband integer index respectively. When the modulation scheme and modulation index of the converter are fixed, based on the double

Fourier integral transformation (DFIT) approach, the harmonic component for voltage v_{A1N} corresponding to frequency ($m\omega_c + n\omega_0$) can be expressed as in (2-13) [56]:

$$S_A(m,n)(t) = C_{mn}\cos\left[(m\omega_c + n\omega_0)t + m\theta_c + n\theta_0 + \theta_{mn}\right] \tag{2-13}$$

where C_{mn} is the harmonic amplitude, θ_c and θ_0 are the initial angles of the carrier and reference waves, and θ_{mn} is a constant value depending on PWM scheme and operation condition. C_{mn} and θ_{mn} can be obtained as in (2-14) from the double integral Fourier analysis. Note that C_{mn} is only a function of PWM scheme and modulation index M. An example for central aligned space vector modulation (SVM) is given in Table 2-1. Assuming the same carrier and symmetrical reference (with 120˚ apart) for the three phases, its phase B and C voltage harmonic v_{B1N}(m,n), v_{C1N}(m,n) will be similar to (2-13) with identical C_{mn} and θ_{mn} but θ_0 will be displaced by 120˚.

$$C_{mn} = A_{mn} + jB_{mn} = \frac{1}{2\pi^2}\int_{y_r}^{y_f}\int_{x_r}^{x_f} e^{j(m\omega_s t + n\omega_0 t)}d(\omega_s t)d(\omega_0 t) \tag{2-14}$$

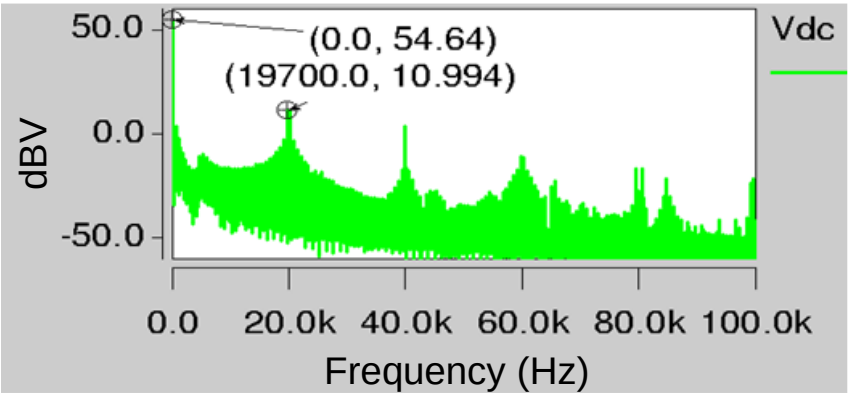
Table 2-1 Double Fourier integral limits for SVM (Phase A)

y	x_r (rising edge)	x_f (falling edge)
$0<y<\frac{\pi}{3}$	$-\frac{\pi}{2}[1+\frac{\sqrt{3}}{2}M\cos(y-\frac{\pi}{6})]$	$\frac{\pi}{2}[1+\frac{\sqrt{3}}{2}M\cos(y-\frac{\pi}{6})]$
$\frac{\pi}{3}<y<\frac{2\pi}{3}$	$-\frac{\pi}{2}[1+\frac{3}{2}M\cos y]$	$\frac{\pi}{2}[1+\frac{3}{2}M\cos y]$
$\frac{2\pi}{3}<y<\pi$	$-\frac{\pi}{2}[1+\frac{\sqrt{3}}{2}M\cos(y+\frac{\pi}{6})]$	$\frac{\pi}{2}[1+\frac{\sqrt{3}}{2}M\cos(y+\frac{\pi}{6})]$
$-\frac{\pi}{3}<y<0$	$-\frac{\pi}{2}[1+\frac{\sqrt{3}}{2}M\cos(y+\frac{\pi}{6})]$	$\frac{\pi}{2}[1+\frac{\sqrt{3}}{2}M\cos(y+\frac{\pi}{6})]$
$-\frac{2}{3}\pi<y<-\frac{\pi}{3}$	$-\frac{\pi}{2}[1+\frac{3}{2}M\cos y]$	$\frac{\pi}{2}[1+\frac{3}{2}M\cos y]$
$-\pi<y<-\frac{2}{3}\pi$	$-\frac{\pi}{2}[1+\frac{\sqrt{3}}{2}M\cos(y-\frac{\pi}{6})]$	$\frac{\pi}{2}[1+\frac{\sqrt{3}}{2}M\cos(y-\frac{\pi}{6})]$

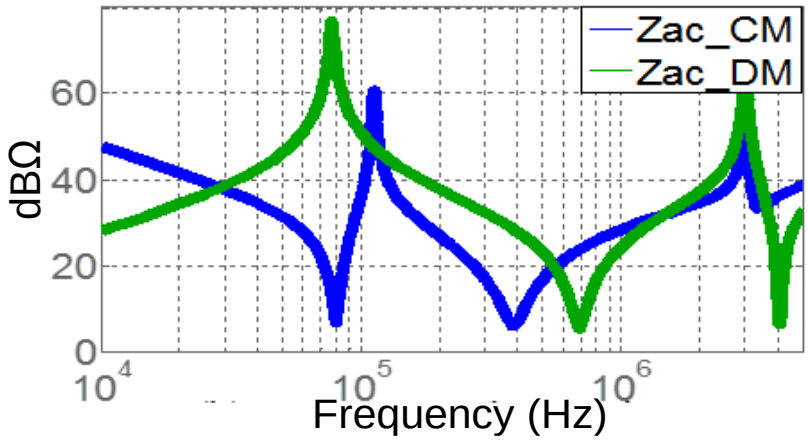
When both noise source and propagation path impedance in the frequency domain model are calculated correctly, the EMI noise can be predicted without the implementation of the system. The experimental verification and accuracy of the proposed modeling methods will be shown in the following section.

2.2.3 Simulation Results and Experimental Verification

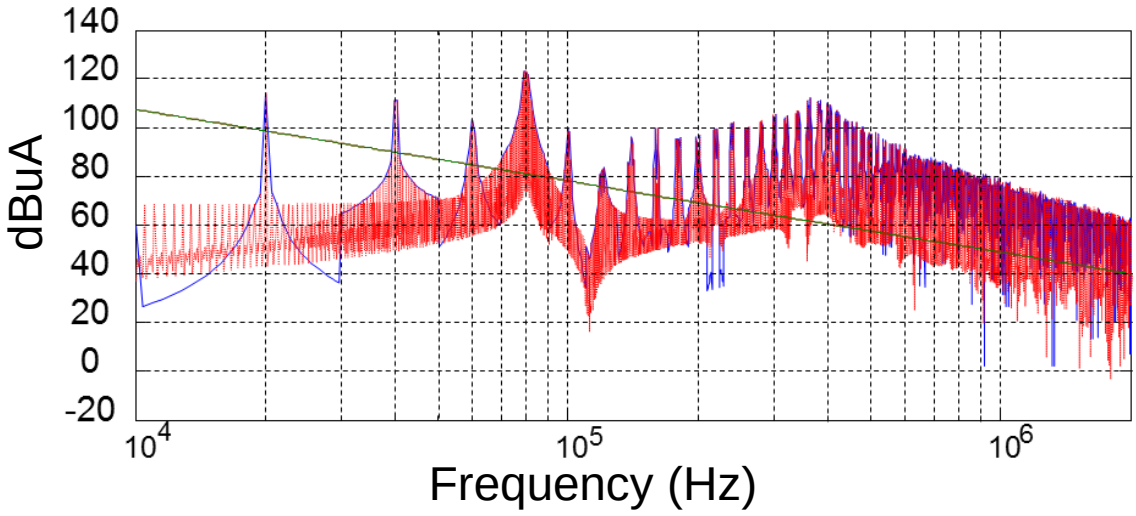
To verify the analysis above, a DC fed motor drive system with long cables shown as in Figure 2-8 is studied. The simulation results of the system detailed time domain switching model by using SABER and the calculation results of the equivalent circuits proposed are compared. The system output power is 100kW, line frequency is 100Hz, and switching frequency is selected to be 20 kHz.



(a) DC link voltage



(b) EMI noise equivalent impedances (DM path: green & CM path: blue)

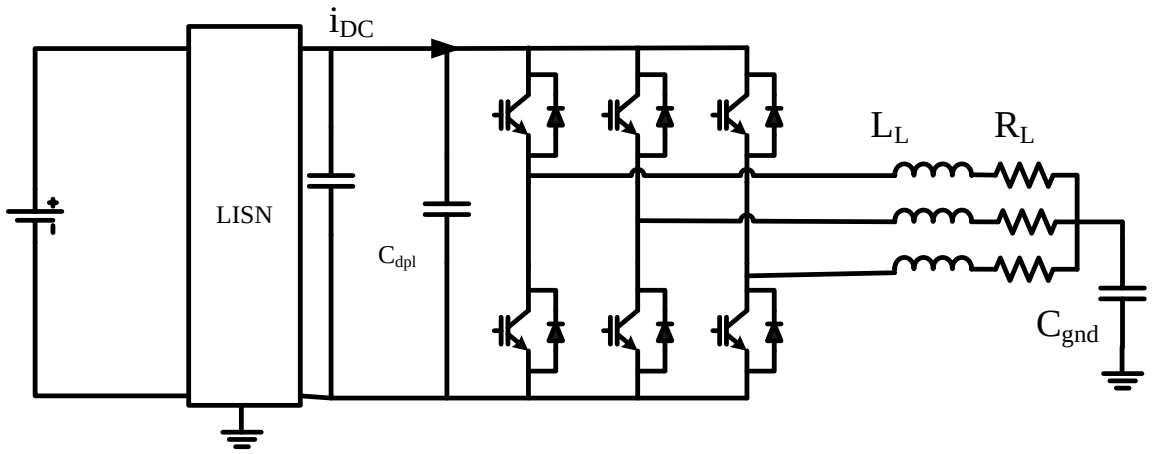


(c) ACCM noise comparison (Simulated: red and Calculated: blue)

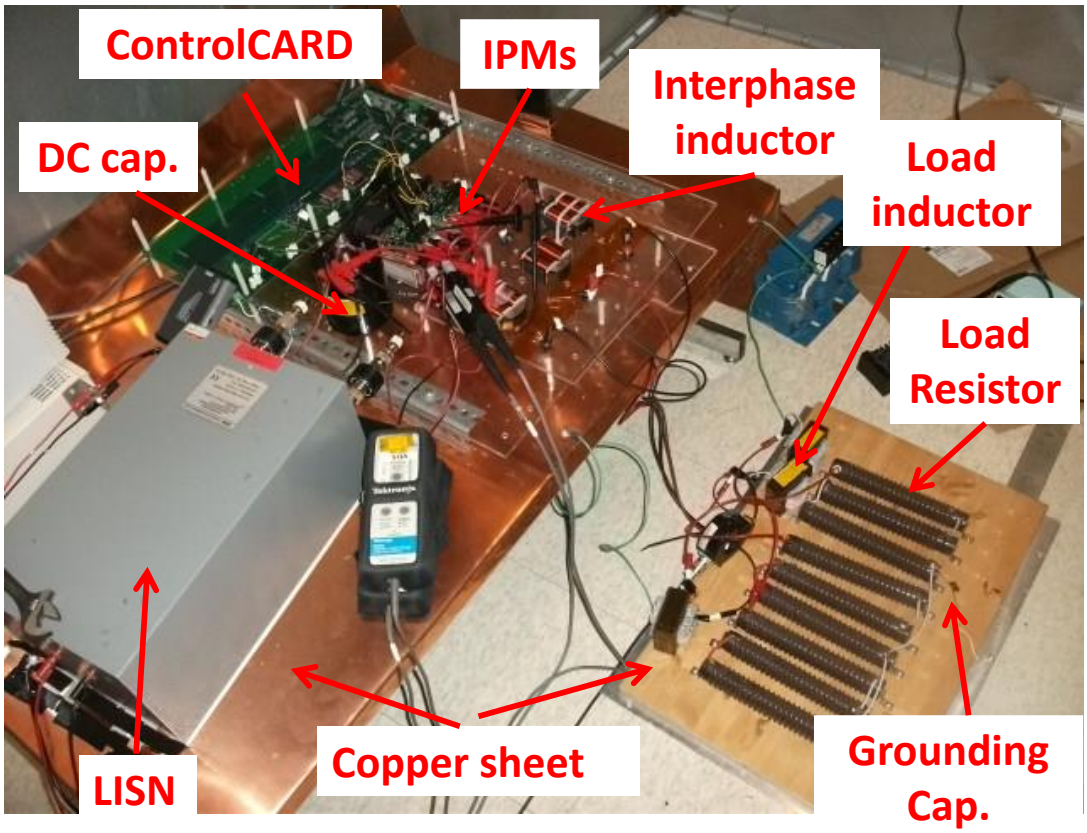
Figure 2-10 Simulation results of noise prediction

Figure 2-10 shows the comparison results between simulation and calculation. Figure 2-10 a) shows that the harmonic component of DC link voltage is more than 40dB smaller than the dc component when the system is work at rated condition, which ensure the assumption that using the product instead of convolution of the spectrum of switching function S_i and dc components of DC link voltage during the calculation of noise sources in the equivalent circuit in a lower frequency range, while in higher frequency range, the harmonics will also contribute to the EMI noise source which make the prediction accuracy reduced. Figure 2-10(b) shows the resonances existed in both CM and DM noise propagation paths. Since there is no LISN on AC side, the AC impedance will influence the impedance of the propagation path of noises and created resonances. Since for DM noise, AC and DC sides are decoupled by the DC link capacitor, the resonant points of AC DM impedance are determined mainly by the AC impedance, however, for CM noise, AC and DC sides are coupled together, both AC and DC impedance will influence the impedance of CM propagation path and determine the resonant points of CM impedance.

Figure 2-10(c) shows the comparison between the simulated result of AC side CM noise and the calculated result of AC side CM noise using proposed EMI prediction model. The noise spectrums show that the resonant points of noise propagation path impedance match well with the peaks and dips in the current noise spectrum, which indicates that the resonant points of the noise propagation path determine the location of the peaks of the EMI spectrum and this will further influence the EMI filter design for the system. The comparison shows that the resonant points of the current noise match well between the calculated result and the experimental result, which validates the modeling of noise propagation path. Moreover the spectrum comparison between calculated and simulated AC CM noises also shows that the prediction of the spectrum matches well with the simulation results, which validates the modeling of noise sources. The error is within 1dB when the frequency is up to 5MHz.



(a) Experimental system structure



(b) Experimental system setup

Figure 2-11 Two Level dc-fed VSI experimental system

Experimental verification is carried outon a scale down 1.5kW VSI system. A RL load with an additional ground capacitor is used to control and change the propagation path impedance easily. The experimental system structure is shown in Figure 2-11(a) and the system setup is shown in Figure 2-11(b).

Figure 2-12 shows the measured propagation path impedance for CM and DM noise which is used in the model to predict EMI noise. A grounding capacitor is added to the circuit to simulate the grounding capacitor of a motor, which create an anti-resonance dip at 270 kHz in the CM impedance. This will result in a resonance in the CM noise and determine the CM EMI filter design.

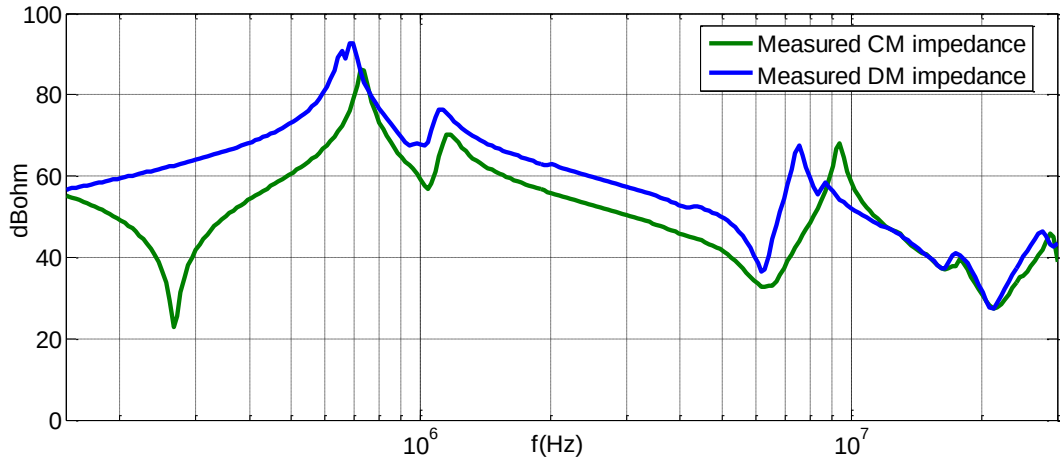
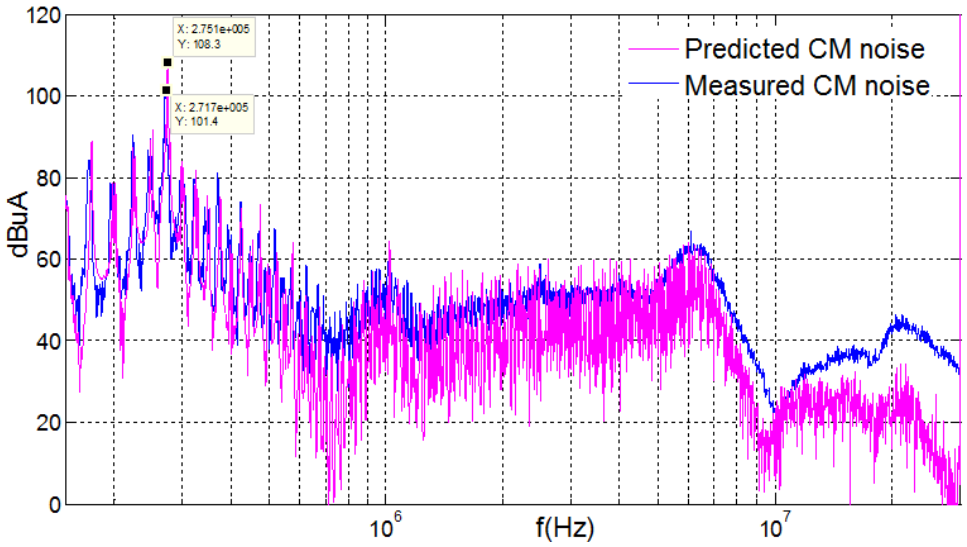
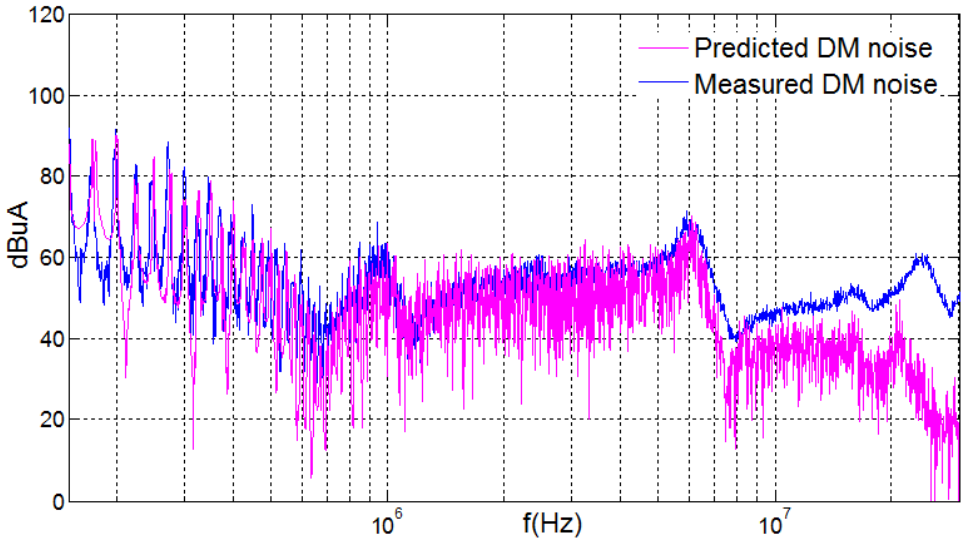


Figure 2-12 Measured noise propagation path impedance

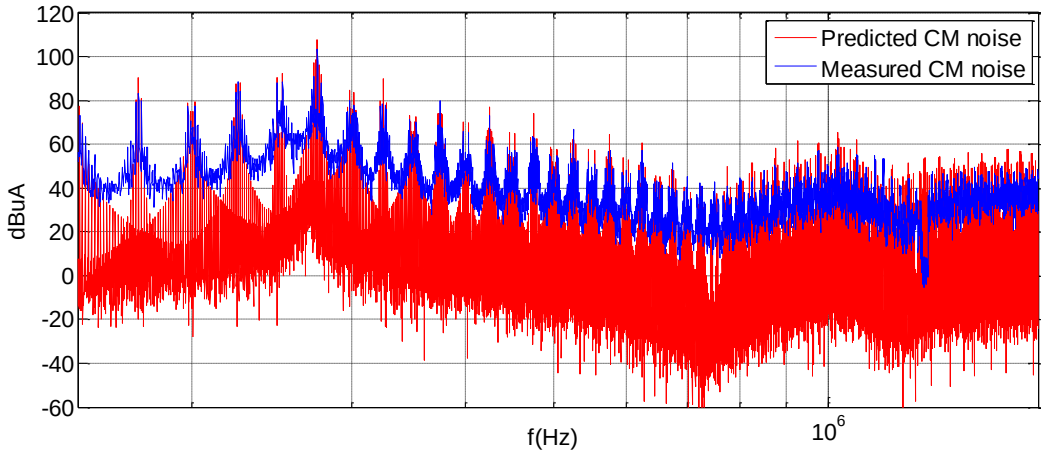
(DM:blue and CM:green)



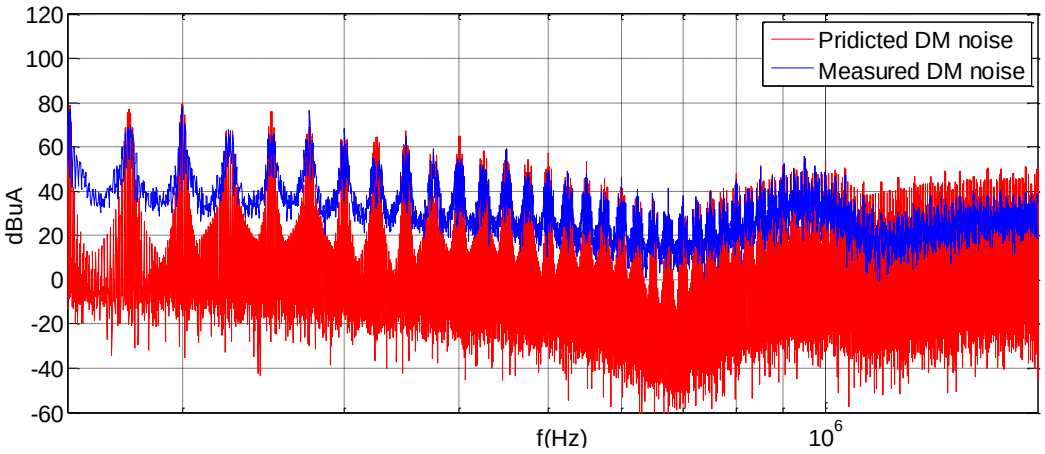
(a) CM noise comparison with standard measurement (predicted: pink and Measured: blue)



(b) DM noise comparison with standard measurement (predicted: pink and Measured: blue)



(c) CM noise comparison with high measurement resolution (predicted: red and Measured: blue)



(d) DM noise comparison with high measurement resolution (predicted: red and Measured: blue)

Figure 2-13 Experimental results of noise prediction

The comparison results between predicted and measured EMI noise are shown in Figure 2-13. Figure 2-13(a) and Figure 2-13 (b) show the comparison in 150 kHz to 30 MHz range. The measurement is performed using the method specified in DO160 standard. It shows that the prediction results match with the measured results for both CM and DM noise up to 7MHz. The error is within 10dB below7MHz which is enough for an EMI filter design. The predicted noise deviates with the measured noise from 7MHz, where the switching behavior (turn-on, turn-off time and ringing during switching) and the impact of the dc link harmonics impacts will appear in the measurement and is not considered in the prediction model. Detailed comparison results with higher resolution for CM and DM noise is shown in Figure 2-13(c) and Figure 2-13(d) at 150 kHz to 2 MHz range, which shows that the prediction model has higher accuracy at lower frequency and at lower frequency (<5MHz), the error is small enough for designing EMI filters based on practical EMI filter design procedure.

2.2.4 Summary and Discussion

In this section, a simple frequency-domain model is proposed to predict the EMI noise emissions for three phase power converters to design EMI filter before the system being built. Double Fourier Integral Transformation (DFIT) method is used to identify the DM and CM noise sources. When system topology, modulation scheme and modulation index are fixed, system EMI noise can be calculated in frequency domain, which is much faster than switching model simulation. Verifications are carried out through simulation and experimental system by comparing the calculated EMI spectrums with the simulated and measured EMI spectrums. In this modeling method, the noise source is calculated under two main assumptions: 1) the dc link voltage and output current harmonics are assumed to

be much smaller than the fundamental components due to the existence of the inherent low pass filter in the system (dc link capacitor and output inductor) and are not considered in the calculation to improve the calculation speed. This will introduce the errors into the calculation of higher frequency harmonics and the error is related with the low pass filter performance in the system (the impedance of dc link capacitor and output inductor at higher frequency). 2) The devices are simplified as ideal switches and the switching behavior (turn-on, turn-off time and ringing during switching) of the devices is not considered. This will also introduce the errors into the calculation of higher frequency harmonics and make the predicted noise source lower than the real system. Thus this modeling method will not provide high accuracy at very high frequency (above 10MHz). If high accuracy at very high frequency is needed, other modeling methods such as behavior modeling methods is preferred. [64] The behavior modelling method model the converter based on the EMI noise measurement results of the real hardware and have good accuracy up to 30MHz. However it need the real hardware of the converter thus cannot be used in the design process. Considering that all conducted EMI standards start at frequencies below 1 MHz, and practically all power converters generate the strongest EMI noise components in the same low-frequency range, the EMI filter must be designed to provide the necessary attenuation in this range and the main weight and size of the EMI filters are determined by the noise within this frequency range. Fortunately most converter components have relatively simple linear characteristics in at these frequencies, and many circuit waveforms can be derived analytically with relatively high accuracy. The proposed methods can provide enough accuracy in this frequency range for EMI filter weight estimation before the implementing the real hardware.

2.3 Filter Design Method Considering Source and Load Impedance

The proposed filter design oriented EMI modeling method can provide enough accuracy in lower EMI frequency range. With the predicted EMI noise and system models, the EMI filter can be designed to suppress EMI noise effectively. The EMI filter design methods are evolving with the development of system EMI modeling. Without accurate system EMI modeling, design of EMI filters for power converters has been traditionally done using trial-and-error methods which cannot ensure the optimal EMI filters design. In order to reduce filter weight and improve system power density, the overdesign of EMI filters need to be avoid. This section will discuss the appropriate EMI filter design method for three phase power converters considering source and load impedance to improve the design accuracy of EMI filters.

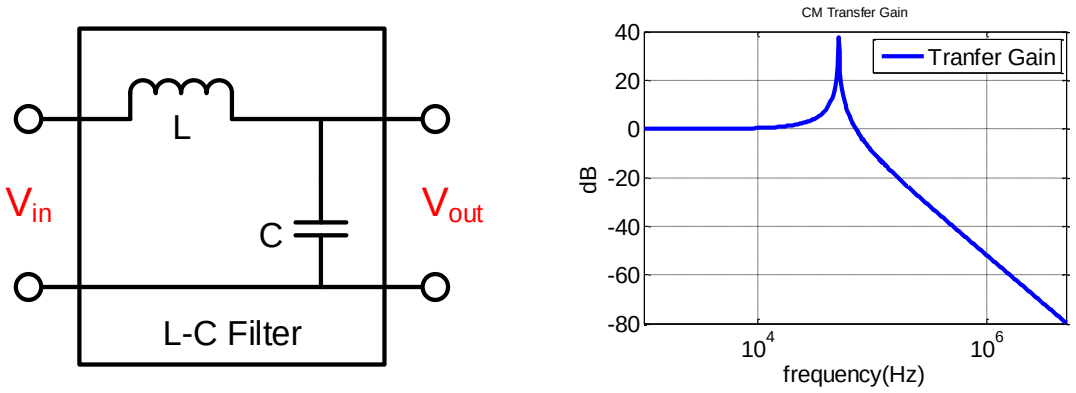
2.3.1 Impact of Load and Source Impedance on Filter Attenuation

Before the analysis of filter design methods, some basic characteristics of the filter need to be clarified. The EMI filters discussed in this work is the passive filter which usually consist of the combination of passive components such as inductors and capacitors. A simple L-C structure filter is taken as an example as shown in Figure 2-14, where one inductor and one capacitor create a two-port network. When the filter is inserted into the circuit, with the increase of frequency, the impedance of the inductor will increase that can increase propagation path impedance to block EMI noise emission and the impedance of capacitor will decrease which can bypass the EMI noise and reduce the EMI noise at the output port. The transfer gain defined as the ratio between the output V_{out} and the input

voltage V_{in} in frequency domain (as shown in (2-15)) is usually used to describe the characteristics of the EMI filter.

$$TF = \frac{V_{out}(s)}{V_{in}(s)} = \frac{1}{1+s^2LC} \tag{2-15}$$

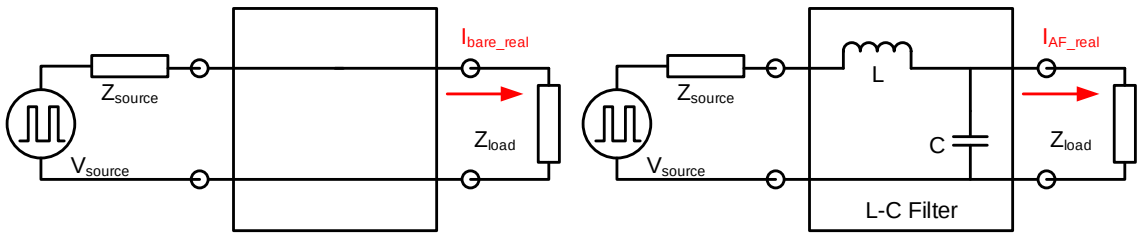
Figure 2-14 shows the bode plot of the transfer gain of the filters with 1mH inductor and 10 nF capacitor with some self-parasitic parameters. It is noticed that after the corner frequency ($\omega_c = \frac{1}{\sqrt{LC}}$) of the filter, the transfer gain show a -40dB/dec attenuation between the input and output voltage, the resonant peak at corner frequency is determined by the resistance in the filter loop at resonant frequency which is related with the damping in the system.



(a) L-C structure filter **(b) Bode plot of filter transfer gain**

Figure 2-14 Structure and bode plot of a L-C filter

In order to get the attenuation for the noise, the EMI filters need to be connected with the system. A successful filter design will make sure the noise after the EMI filter is below the standard. Thus, the real attenuation one can get from the filters is the in circuit attenuation, defined as the ratio between the noise after adding EMI filter (I_{AF_real}) and the bare noise (I_{bare_real}) in the real system as shown in Figure 2-15.



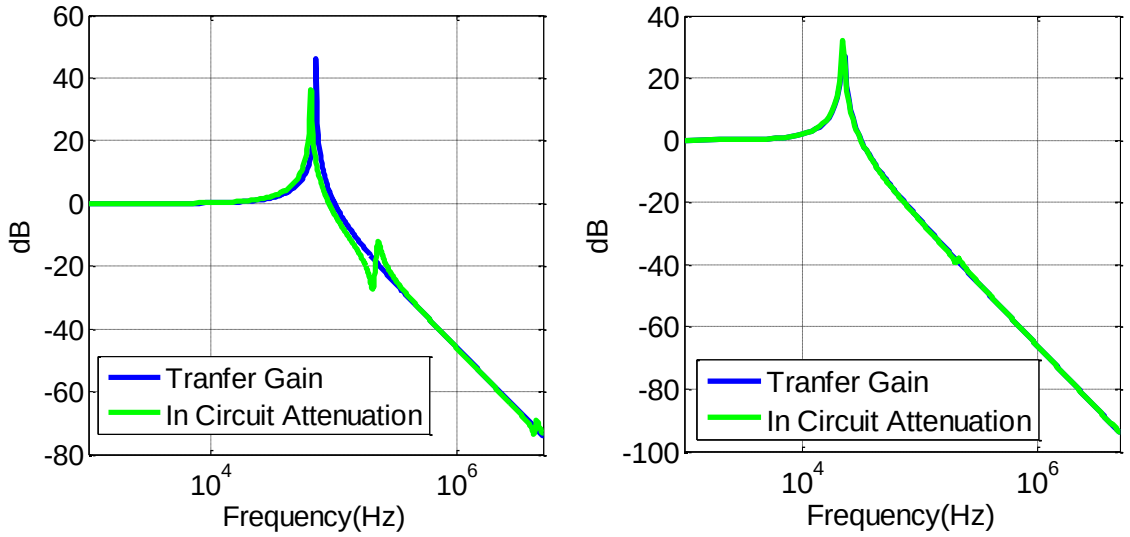
(a) without filter **(b) with filter**

Figure 2-15 Filter in-circuit-attenuation

Thus, the filter in circuit attenuation can be calculated as (2-16)

$$TF = \frac{I_{AF\_real}}{I_{bare\_real}} = \frac{Z_{source} + Z_{Load}}{(1 + sCZ_{load})(Z_{source} + sL) + Z_{load}} \tag{2-16}$$

It is clear that the real in circuit attenuation is determined by both the filter parameters and system propagation path impedance and it is different from the transfer gain when Z_{source} and Z_{load} are considered. However, it is also shown that if the impedance of the inductor is much larger that the source impedance and the impedance of the capacitor is much smaller than the load impedance, (2-16) can be simplified to (2-15), if such cases which is defined as the impedance mismatching is satisfied , transfer gain can approximately represent the in circuit attenuation. Figure 2-16(a) shows the comparison between the filter transfer gain and in circuit attenuation of a 1mH + 10nF L-C structure filter in the experimental system shown in chapter 2.2, due to the existence of load and source impedance, it is clear that the real in circuit attenuation and filter transfer gain are different. It can be notice that there is a big difference between the two plots at around 300kHz where the load impedance has a resonant and the impedance is smaller than the impedance of the capacitor.



(a) Without impedance mismatching **(b) With impedance mismatching**

Figure 2-16 Comparison between transfer gain and in circuit attenuation

Figure 2-16(b) shows the comparison between the filter transfer gain and in circuit attenuation when the filter capacitor is increased to 50nF. It is clear that when the impedance of the capacitor is smaller than the load impedance or the impedance mismatching is achieved, transfer gain can be used to represent the in circuit attenuation.

2.3.2 Practical Design Methods

The main target of EMI filter design is to find the proper L and C combination to provide enough attenuation for the noise source to meet the standard and also gives the minimum weight of the filter. Reference [77] proposed an EMI filter design method using the transfer gain (TF) of filter to estimate the filter in circuit attenuation (ICA) with the assumption that the impedance mismatching has been achieved between filter input/output impedance and source/load impedance as shown in Figure 2-17. This method has been used widely as a practical EMI filter design methods. However, due to the existence of resonance source/load impedance and the EMI filter parasitic parameters, the assumption of impedance mismatch cannot be ensured in real system. In three phase power converters,

usually there are limitation of the grounding capacitance from safety requirements. And also if there is a long connection cable, the cable impedance and the grounding capacitance of the load will create multiple resonance on the propagation path impedance making it hard to achieve the impedance mismatching, moreover, the self parasitics of the inductor and capacitor will also change the impedance at higher frequency which make it even harder for maintaining impedance mismatching in the system. Thus certain margin is always needed for this design method which cannot give the optimal filter design and make the filter over-designed to attenuate the noise effectively.

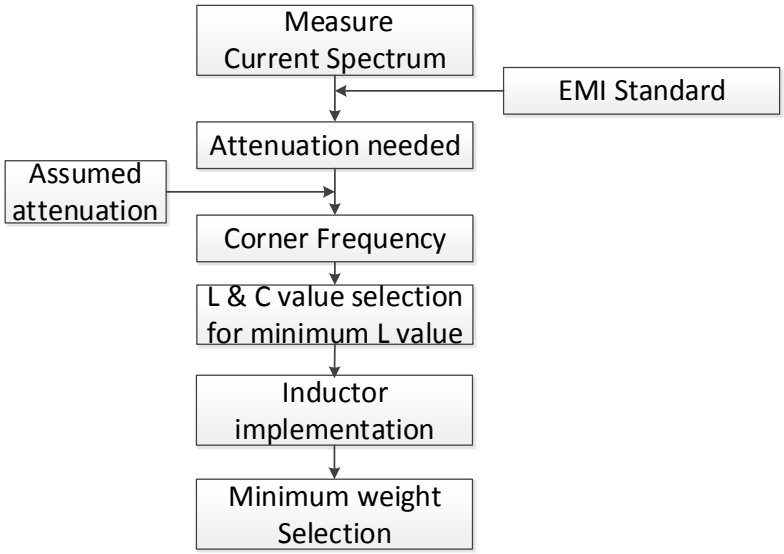
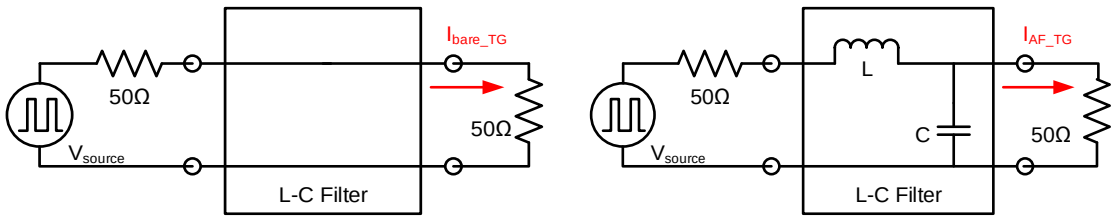


Figure 2-17 Practical EMI filter design method

To verify filter attenuation, the insertion gain of the filters can be measure using a network analyzer and checked as the in circuit attenuation. There will be an inherent 50 Ω resistance added as the load and source impedance during the measurement. the insertion gain is define as the the ratio between the noise after adding EMI filter (I_{AF_TG}) and the bare noise (I_{bare_TG}) with the 50 Ω load and source impedance as shown in Figure 2-18.



(a) Without filter **(b) With filter**

Figure 2-18 Insertion gain measurement

However, this still cannot accurately predict the in-circuit-attenuation of the filters, since the load and source impedance will not be 50Ω constant in the real circuit. Figure 2-19 shows the comparison of the transfer gain, the insertion gain and the in circuit attenuation when impedance mismatching is achieved. It is clear the transfer gain cannot indicate the real in circuit attenuation and should not be used to check the filter design.

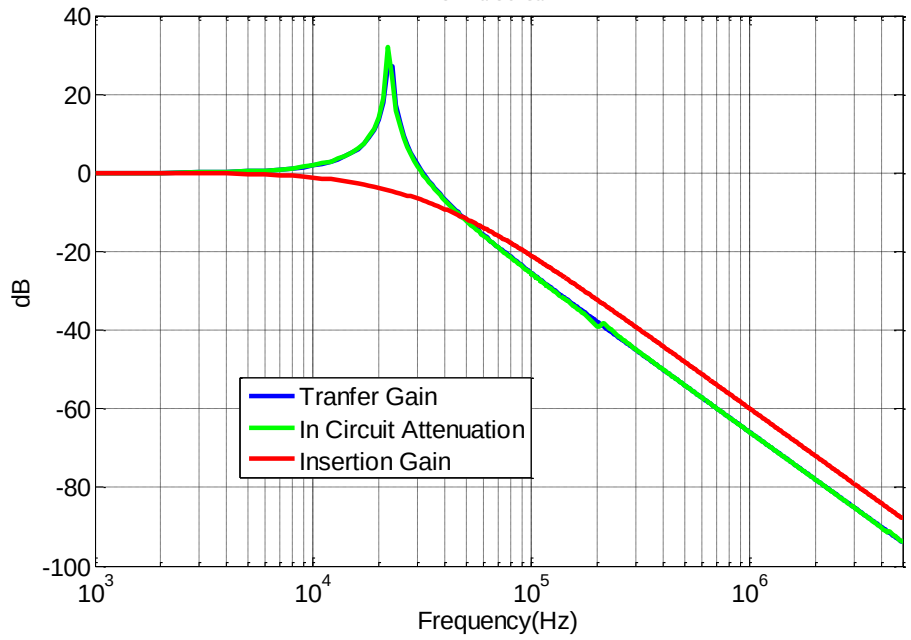


Figure 2-19 Comparison of transfer gain, in circuit attenuation and insertion gain

Another problem in the practical filter design method is that it designs the filter values without the consideration of the filter implementations but assuming that the minimum value can give a minimum weight of the filter, however, filter weight is not only determined by the values, other considerations such as the volt-second on the inductor also determines

the filter weight which should be considered with the filter parameter selection for the optimized filter design.

Moreover, this practical design method need to measure the current spectrum, thus it need the implementation of the power stage before the filter design, as what has been discussed above, it cannot ensure the optimized design of total system weight minimization.

2.3.3 Improved Filter Design Methods Considering Source and Load Impedance

Based on the frequency domain modeling of the system, EMI noise can be predicted when the system working condition is determined. Moreover, the system source and load impedance can be included in the predict circuit for filter attenuation, and filter in-circuit-attenuation can be predicted and used in filter design to avoid over-design of filters.

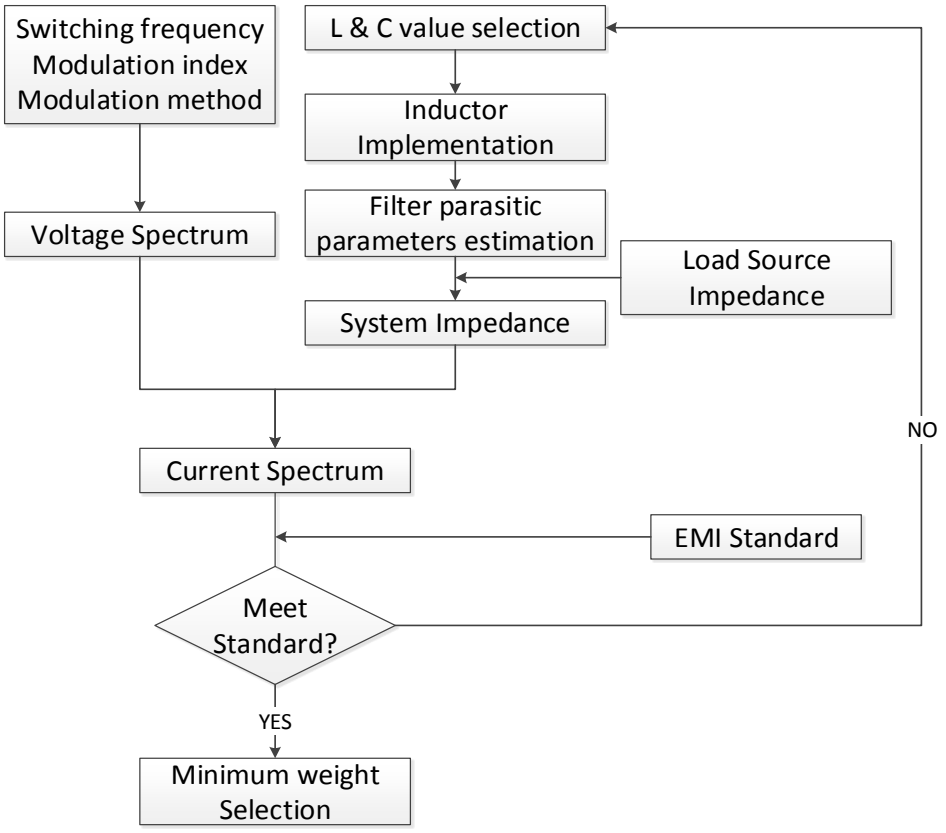


Figure 2-20 Propose filter design method considering load and source impedance

To improve the system power density, the weight of EMI filters should be minimized which require the estimation of inductor and capacitor working condition during filter design process. The filter design and weight minimization method is shown in Figure 2-20, where the filter is designed by sweeping all possible L&C values and compare the filter attenuation with required attenuation at each frequency to get an applicable filter parameter space. Within this applicable filter parameter space, a filter weight optimization algorithm is used with the target function as filter weight minimization while the boundary conditions are selected to meet inductance limitation, filter physical fitness, temperature rise limit, and saturation limit and so on, the detailed analysis will be shown in section 2.5. The parasitic parameters (EPR and EPC) are included in the optimization process that are calculated after the design of the inductor, then the inductor and capacitor model will be added to the equivalent circuit to predict the EMI noise after adding the EMI filters to check the EMI filter performance. Since this design method use the real in circuit attenuation and considers the parasitic parameters, it can ensure the performance of the filter in the real application. When impedance mismatching cannot be achieved in the system, this method will provide a more accurate design result compared with the practical design method. One problems with this method is that it involves multiple design processes of the implementation of inductors which take a significant time. Thus, the whole design process is time consuming. When impedance mismatching can be achieved, a simplified design method is shown in Figure 2-21.

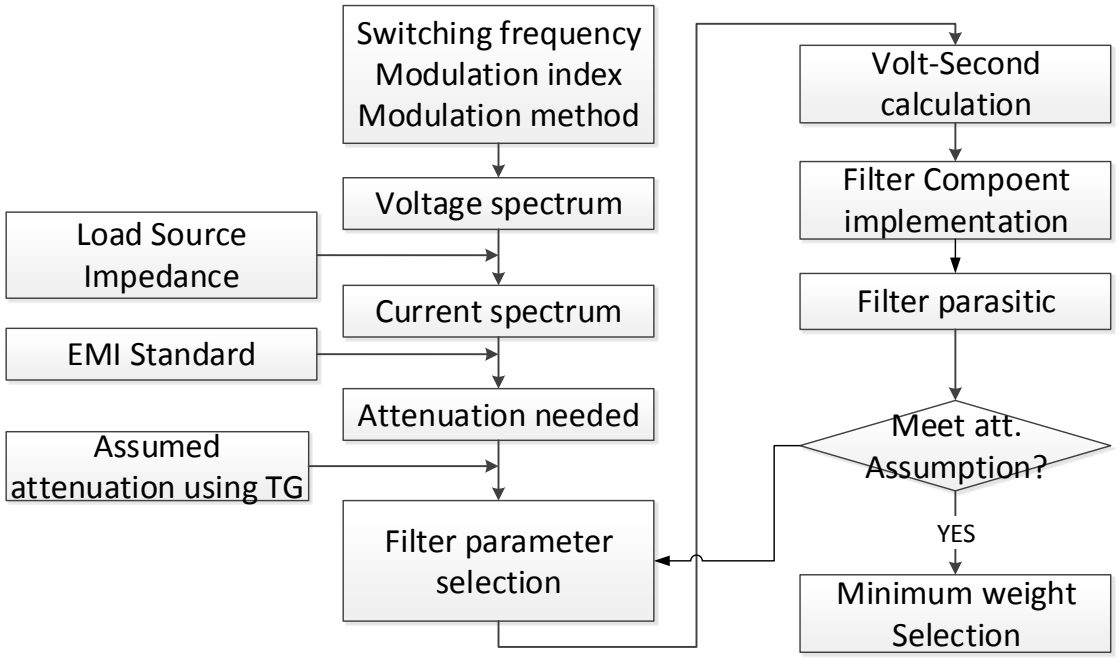


Figure 2-21 Simplified filter design method with impedance mismatching

This method is based on the proposed system level EMI modeling, when converter switching frequency, modulation method and modulation index is known, the noise source can be calculated using DFIT method, then the current noise spectrum can be calculated from the model with the propagation path impedance. The transfer gain is used as the approximated attenuation to design filter parameters. The volt-second on the inductor is calculated from the proposed system level EMI model and then filter components are design and implemented with the estimation of filter parasitic parameters, then the in circuit attenuation of the whole filter is calculated with the proposed system level EMI model again to verified the performance, if the implementation does not meet the requirement, then the filter parameter selection will be revised. Finally, a minimum weight selection process is done to get the design result of the EMI filter with minimum weight and enough attenuation. It need to be noticed that the transfer gain is used in this design method to estimate the in circuit attenuation, thus the assumption of the impedance mismatching must be tested, if impedance mismatching cannot be achieved, then the previous proposed

method is preferred. Moreover, it is necessary to check the filter attenuation after the implementation of filter components to ensure the proper performance. With this proposed filter design method, the filter can be designed with required attenuation and the over design can be avoid.

2.4 Filter Design Methods for Both Input and Output Sides

The EMI filter design method can ensure a successful EMI filter design that can effectively attenuate one type of the EMI noise (such as AC CM or DC DM noise) in the system. However, the EMI standards is usually defined for the total noise that include both CM and DM noise. Adding filter to the system will change the propagation path of the noise. Since the performance of the filter is related with the propagation path impedance. Adding new filter in the circuit will change the performance of the existing filters. The interaction between different types of filters need to be considered for a successful EMI filter design. Moreover, in some applications such as motor drive system with long connection cables or converters that bridges two buses, EMI standards are defined for both input and output of the power converter. For such applications, EMI filters are required for both input and output sides. Due to the interaction between AC and DC side, adding EMI filters on one side will influence the EMI noise level on the other side. If this interaction is not considered in the filter design procedures, even though one can design an optimized filter for one side to meet the standard, adding filters on the other side will make the noise worse on this side and finally fail to meet the standard.

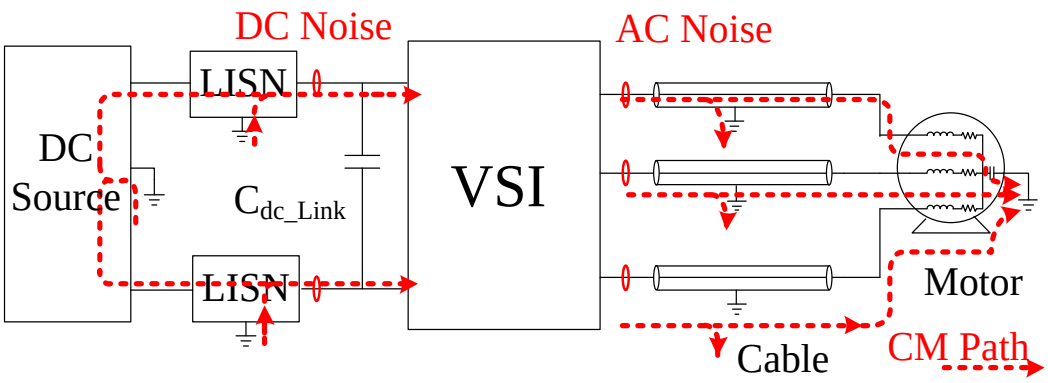


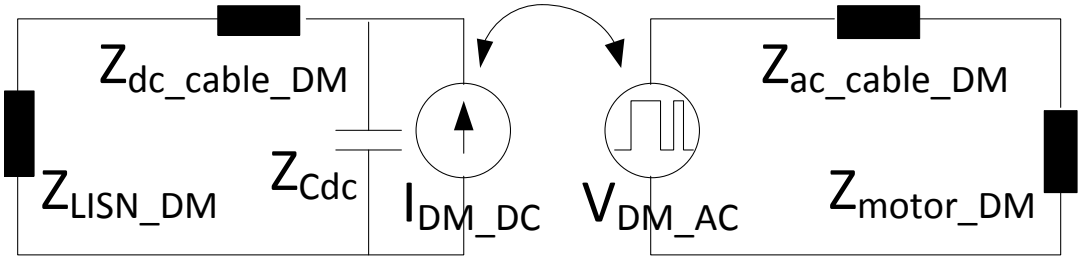
Figure 2-22 Dc-fed motor drive system with long connection cables

In this section, a dc-fed motor drive system with long connection cables as shown in Figure 2-22 is taken as an example, based on the common mode (CM) and differential mode (DM) EMI noise equivalent circuits, the relationship of system EMI noise between AC and DC sides are investigated, which shows the interaction between DM and CM noises and the interaction between adding ac-side and dc-side filters. With these considerations, an EMI filter design procedure to design CM and DM filters for both AC and DC sides is proposed. To minimize the impact on the EMI noise of one side caused by adding filter on the other side, certain order must be followed to design AC and DC CM and DM filters. Simulation and experimental results verify the interaction between AC and DC filters and show that EMI filters can be designed to suppress both AC and DC CM and DM EMI noise to meet the standard with the proposed EMI filter design method. These design methods can be applied also for other applications where EMI filters are needed for both sides of the power converters.

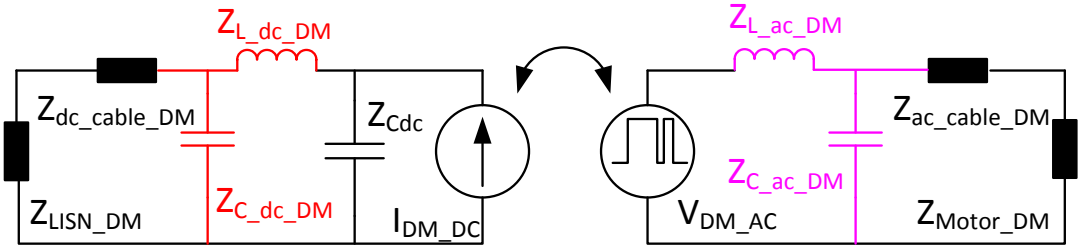
2.4.1 Interaction between EMI Filters

It has been shown in the system level EMI modelling section that AC-side and DC-side DM noise are decoupled due to the existence of the dc link capacitor as shown in Figure 2-23. Thus, Adding filter on one side will not change the propagation path

impedance of the other side and the performance of the EMI filter will not change by adding EMI filter to the other side.



(a): DM equivalent circuit



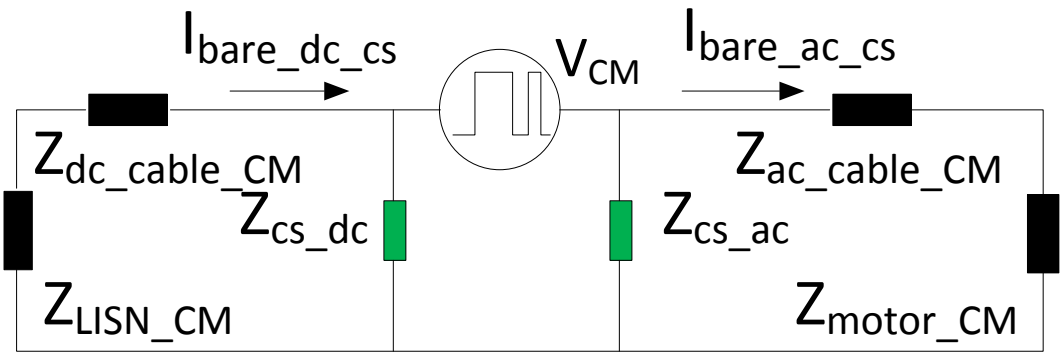
(b): DM equivalent circuit with DM filter

Figure 2-23 Equivalent circuits for DM filter analysis

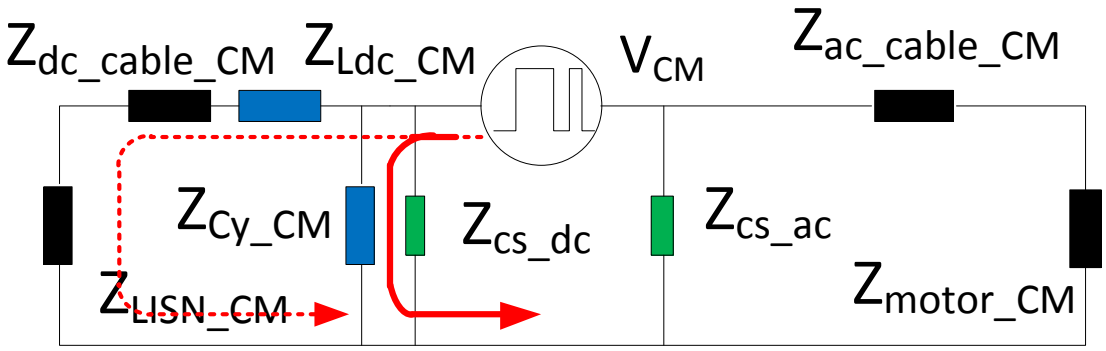
However, the noise source of AC side is related with the voltage harmonics on the DC link capacitor and the noise source of DC side is related with the harmonics of output AC current. Adding filters on one side will change those harmonics and change the noise source of the other side, thus there is still interaction between AC and DC DM filters. Usually AC side DM filter will use L-C structure and DC side DM filter will use C-L structure (Figure 2-23(b)) to provide enough attenuation for DM noises [71]. After adding DC DM filters, the changes of the dc link voltage will be limited due to the existence of dc link capacitor. However, for motor drive system, adding L-C filter on AC side will change the resonant frequency of AC load and change the output harmonics significantly, which will change the noise source on DC side. Thus, the impact on changing the dc-side noise source by adding DM filter to ac side is more significant than the impact on changing the ac-side noise source by adding DM filter to dc side. However, in rectifier applications, since the

AC side EMI filters are added after the boost inductor, the impact is related with the final filter parameter selected.

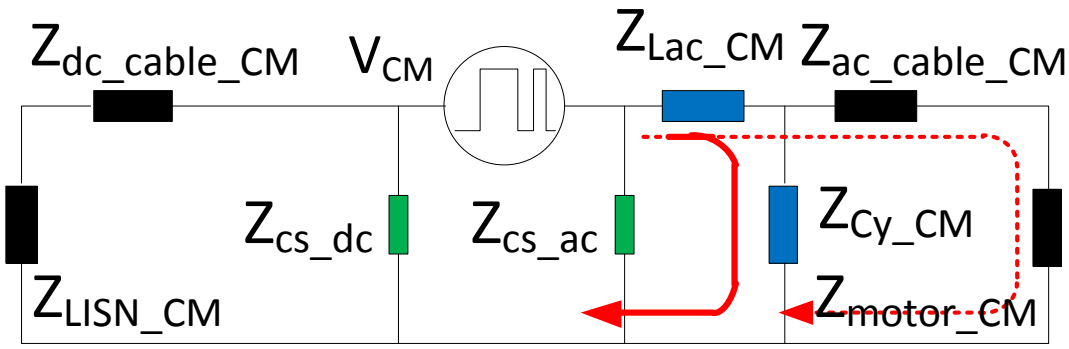
Considering the CM noise propagation path through both AC and DC sides, since there is no such big low impedance path as the dc link capacitor in DM propagation path, the equivalent circuit (Figure 2-24(a)) includes the interaction between AC and DC side for CM noise, where the noise source is also determined by the working condition and dc link voltage ripple of the system.



(a) CM equivalent circuit



(b) CM equivalent circuit with DC CM filter



(c) CM equivalent circuit with AC CM filter

Figure 2-24 Equivalent circuits for CM filter analysis

Therefore, for CM noise, adding filter on one side will influence the propagation path impedance of both AC and DC sides and change the performance of the filter on the other side. In practical EMI filter design method, C-L filter is a common choice for DC side EMI filtering (Figure 2-24((b)) because C_y capacitors can bypass the CM noise that reduce the inductor value needed for a given attenuation and also provide a voltage divider to reduces the CM volt-second across the CM inductor and makes the inductor smaller[71]. However, the C_y capacitors will create a low impedance path for CM noise (as shown in Figure 2-24(b)), which will go through the AC side and amplify the AC CM noise. It is also true that adding AC L-C CM Filter (as shown in Figure 2-24((c)) will amplify the DC CM noise since the AC C_y capacitors also provide a low impedance path for DC CM noise. For motor drive system, when considering both AC and DC CM noise, connecting C_y capacitors to ground will help the filter design for one side, while make it harder to design the EMI filter for the other side, since the C_y capacitor will provide an additional low propagation path for the EMI noise of the other side. Thus, certain orders need to be followed to minimize the interaction between AC CM and DC CM filters.

The equivalent circuits also show that DM inductors will show in CM model and CM capacitors will show in DM model, thus there is also interaction between CM and DM

filters. Usually L-C topology is used for DM filter to provide enough attenuation for DM noises. Adding L-C filter will change the current harmonics of the converter, which will change the CM noise source in the equivalent circuit. Moreover, considering the influence on the system impedance between CM and DM filters, the DM filter inductor will appear in CM equivalent circuit and provide attenuation for CM noises, which is also true for CM filter capacitors that can influence the DM noises. However, due to the limitation in the standard, the value of CM filter capacitor is usually much smaller than DM filter capacitors, thus DM filters should be designed before CM filters to assure the accuracy of CM noise measurement and avoid overdesign.

In order to verify the interaction between EMI filters, A SABER simulation is established based on a 2 kW 300 V DC-fed 3phase motor drive systems with RL load shown as Figure 2-25, where a grounding CM capacitor is added to control the CM propagation path impedance. Detail switched simulation model is used to analyze the interaction between AC and DC sides and study the EMI filter performance, ideal switches are used in the model and the load and source impedance model are built based on the measurement of the real system.

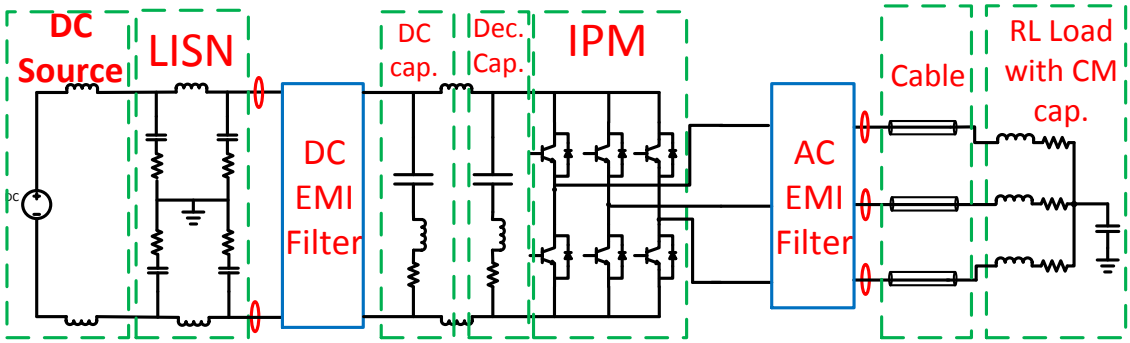
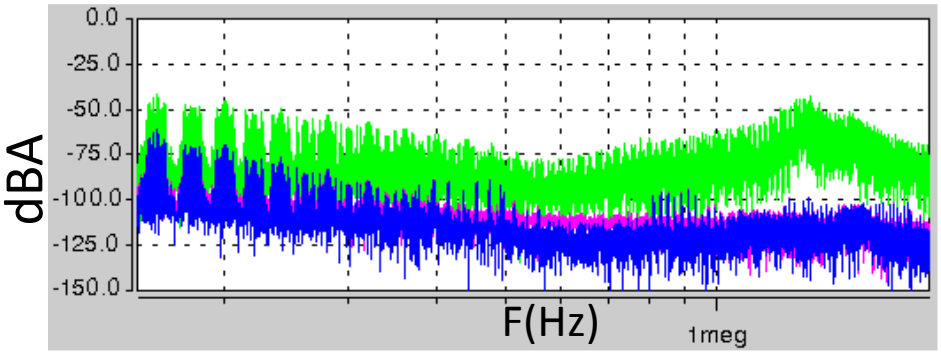


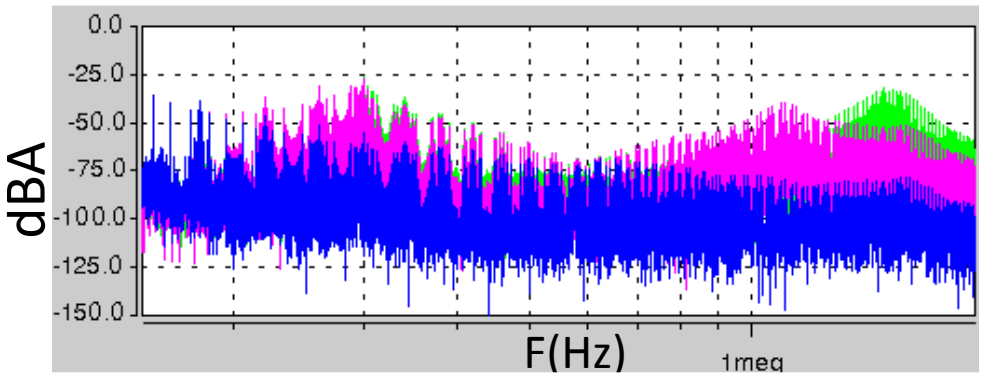
Figure 2-25 Experimental system for the verification of filter interaction

AC EMI filters (including a L-C structure CM and a L-C structure DM filter) are added to the circuit as an example in the simulation to test the noise change on both sides and

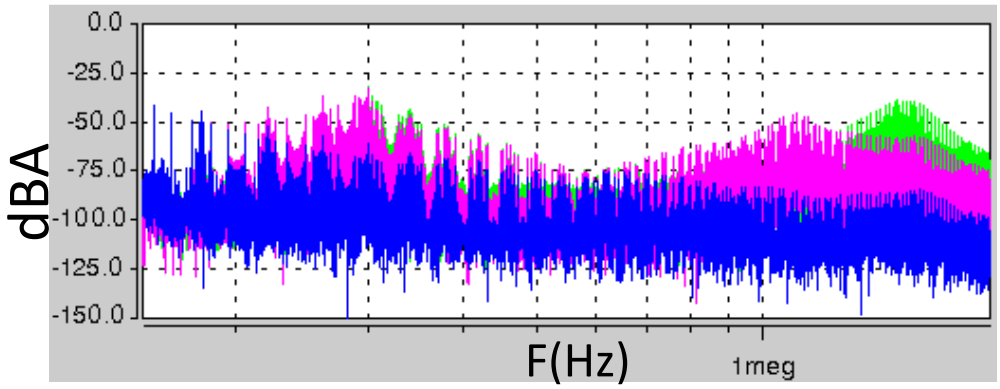
verify the interaction between EMI filters. Figure 2-26 shows the simulation results of AC and DC side CM and DM noise before and after adding AC side EMI filters.



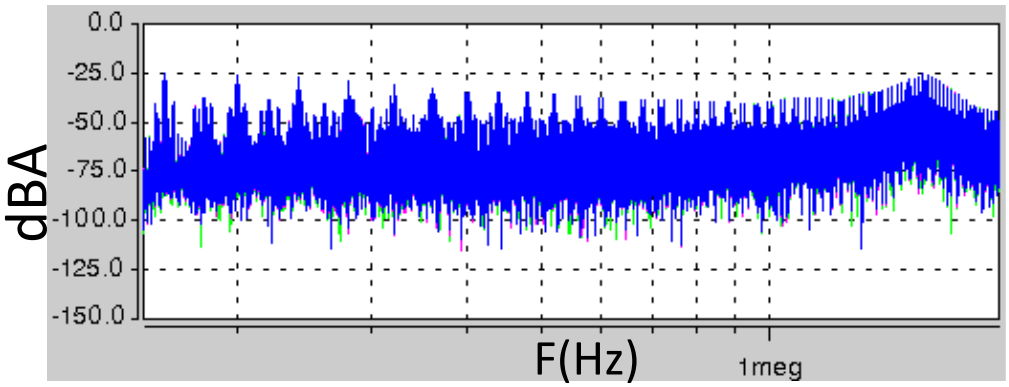
(a) AC DM noise (bare noise: green; with ACDM filter addded: pink, with AC DM and CM filter added: blue)



(b) AC CM noise (bare noise: green; with ACDM filter addded: pink, with AC DM and CM filter added: blue)



(c) DC CM noise (bare noise: green; with ACDM filter addded: pink, with AC DM and CM filter added: blue)



(d) DC DM noise (bare noise: green; with ACDM filter added: pink, with AC DM and CM filter added: blue)

Figure 2-26 Simulation results of EMI noise with both input and output filters

It is clear that adding AC DM filter will reduce the DM noise on AC side effectively and it will also help to reduce the CM noise on both sides since the inductance of DM filter inductor will appear in the CM noise propagation path which will increase the CM propagation path impedance and reduce the CM noises in high frequency. Moreover, the results also show that adding AC DM filter will change the DC CM noise, which indicates the coupling between AC and DC CM noise. Meanwhile, there is no significant change on DC DM noise, which verifies the decoupling of DM noises of AC and DC sides. Only CM choke inductor are used as the CM filter to reduce the impact of C_y capacitors on CM noises, thus adding CM choke inductor on AC side will increase the propagation path impedance for both AC and DC noises and adding ACCM filter will reduce both AC and DC CM noises. However, it has limited impact on both AC and DC DM noise, which also verifies the previous analysis.

2.4.2 Floating Filters for Noise Containment

Considering the interaction between AC and DC sides for CM noise, instead of connecting Cy capacitors to the ground which will provide additional low impedance

propagation path for the noise of the other side, a capacitor can be connected across the noise source to confine the noise within the converter and suppress both AC and DC noise. For motor drive system, usually a DM filter is designed before the CM filter since the DM inductor will help reduce the CM noise and DM capacitors will not influence CM noise. To obtain more attenuation and utilize the DM capacitors to reduce CM noise, the mid-point of AC DM capacitors and DC link capacitors can be connected as shown in Figure 2-27. The equivalent circuit of this connection is shown in Figure 2-28, where a capacitor is connected across the noise source. One can also directly connect the mid-point of the input and output side together, however, it may increase the DM current ripple significantly. The connection with an extra capacitor can limit the increase of current switching harmonics through the output DM filter and also provide more freedom to control the noise attenuation for high frequency, the capacitor provides a low impedance path to bypass the noise and limit the noise within the converter, thereby suppressing both AC and DC noise.

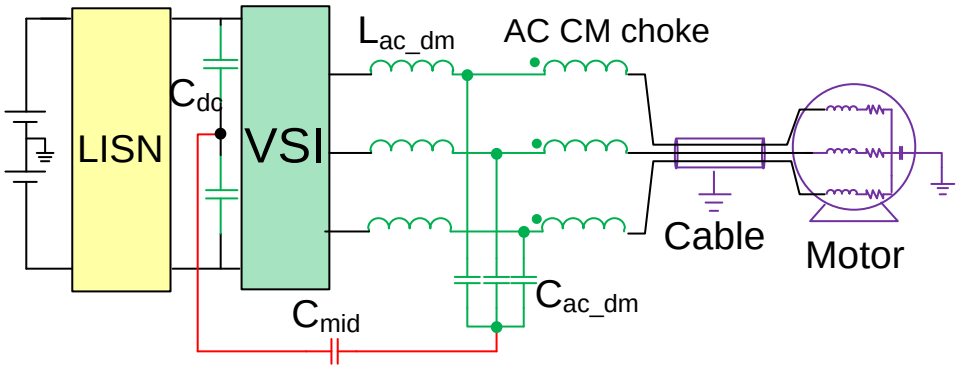
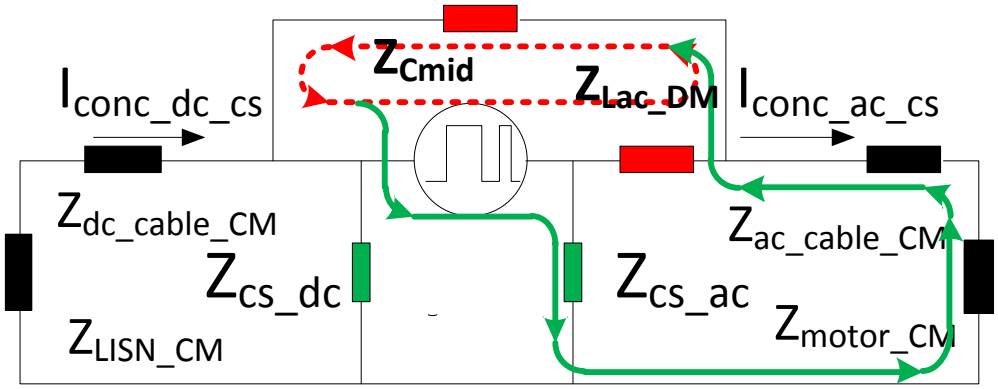
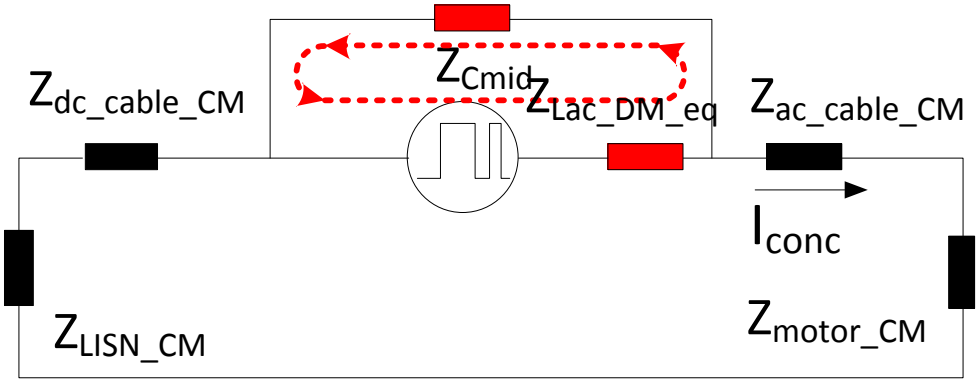


Figure 2-27 Floating filter topology



(a) CM equivalent circuit considering device stray capacitor



(b) Simplified CM equivalent circuit

Figure 2-28 Equivalent circuit for floating filter analysis

When analyzing the impact of connecting the mid-point, the stray capacitances between device and common ground Zcs in equivalent circuit are ignored first, since the influence of those capacitances only appears in high frequency and will be analyzed later. From the simplified equivalent circuit (Figure 2-28(b)); the bare noise and noise after adding DM filter and connecting mid-point can be calculated as shown in (2-17) and (2-18) respectively.

$$I_{bare} = \frac{V_{CM}}{Z_{dc\_CM} + Z_{ac\_CM}}, \text{ where } \begin{matrix} Z_{dc\_CM} = Z_{LISN\_CM} + Z_{dc\_cable\_CM} \\ Z_{ac\_CM} = Z_{motor\_CM} + Z_{ac\_cable\_CM} \end{matrix} \quad (2\text{-}17)$$

$$I_{conc} = \frac{\frac{V_{CM}}{Z_{Lac\_DM\_eq} + Z_{Cmid}} Z_{Cmid}}{Z_{dc\_CM} + Z_{ac\_CM} + Z_{Lac\_DM\_eq} // Z_{Cmid}} \quad (2\text{-}18)$$

The DM inductor L_{ac_DM} and capacitors $C_{mid}+3C_{ac\_DM}$ create a voltage divider that reduces the noise source for both AC and DC side. Equation (2-19) shows the in circuit attenuation (ICA) of connecting the mid-point compared with the bare noise.

$$ICA_{noCs}=\frac{I_{ConC}}{I_{bare}}=\frac{1}{1+\frac{Z_{Lac\_DM\_eq}}{Z_{Cmid}}+\frac{Z_{Lac\_DM\_eq}}{Z_{dc\_CM}+Z_{ac\_CM}}} \tag{2-19}$$

In EMI frequency range (150kHz~30MHz), when Zc is much smaller than Zac+Zdc and Zdm. Both AC and DC CM noise can be attenuated.

When high frequency performance of the filter is considered, stray capacitors of the device to ground C_{s_ac},C_{s_dc} need to be included in the analysis. The bare noise of ac side and the noise of ac side after connecting mid-point can be calculated as shown in (2-20) and (2-21) respectively.

$$I_{bare\_ac\_cs}=\frac{V_{CM}}{Z_{dc\_CM}//Z_{cs\_dc}+Z_{ac\_CM}//Z_{cs\_ac}}\frac{Z_{cs\_ac}}{Z_{ac\_CM}+Z_{cs\_ac}} \tag{2-20}$$

$$I_{ConC\_ac\_cs}=\frac{V_{CM}\left(\frac{Z_{cs\_ac}}{Z_{cs\_ac}+Z_{cs\_dc}//Z_{dc\_CM}}-\frac{Z_{Lac\_DM\_eq}}{Z_{Lac\_DM\_eq}+Z_{Cmid}}\right)}{Z_{dc\_CM}//Z_{cs\_dc}//Z_{cs\_ac}+Z_{Lac\_DM\_eq}//Z_{Cmid}+Z_{ac\_CM}} \tag{2-21}$$

At certain high frequency, connecting the mid-point will bring a low impedance loop (green loop in Figure 2-28(a)) for the noise and high frequency attenuation is limited as the calculation results shows in Figure 2-29.

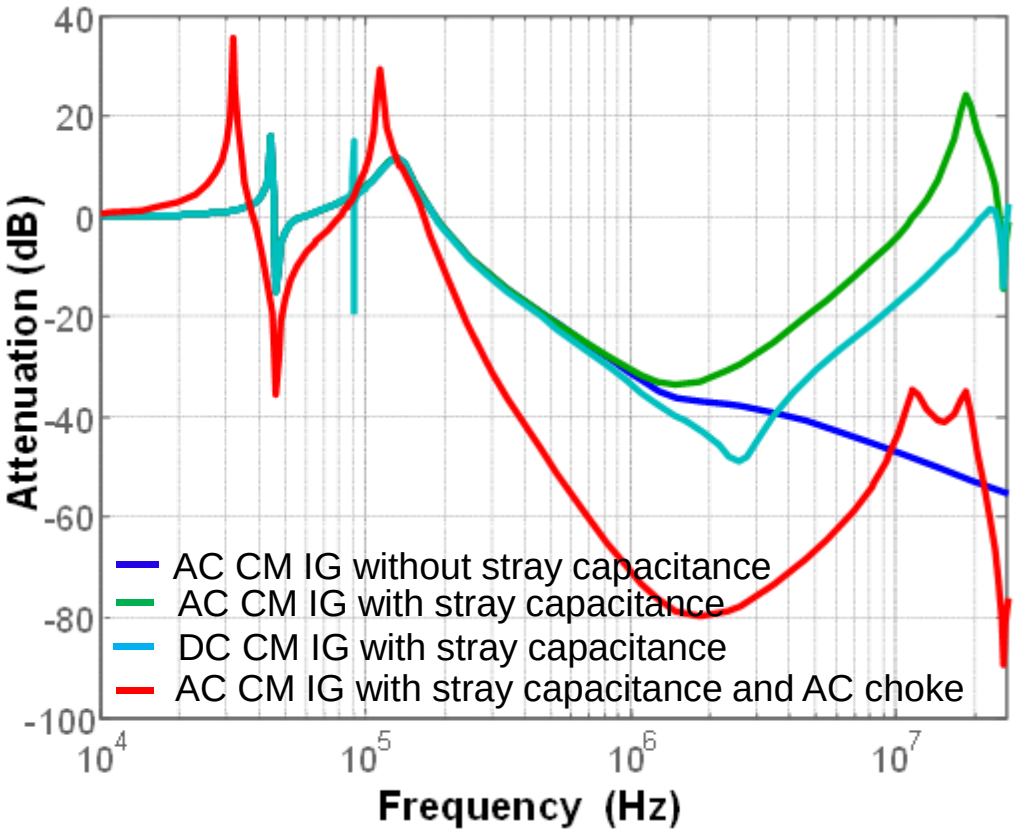


Figure 2-29 In-circuit-attenuation calculation results of floating filters

For AC noise in circuit attenuation, bigger L and C value will increase the low frequency attenuation while the high frequency attenuation is mainly determined by the stray capacitance C_{s_dc} and C_{s_ac}, by increasing the ground impedance of heatsink can help to reduce these stray capacitances and increase the attenuation in high frequency of the proposed filter, however it will bring the safety issues to the system. To increase the high frequency attenuation, a CM choke can be added after the DM filter to block the low impedance loop at high frequency and a small capacitor can also be added to further increase the attenuation at higher frequency. Moreover the capacitors should be connected to the mid-point of dc link capacitors instead of connecting to the CM ground as shown in Fig. 4d to avoid low impedance path which will amplify the dc-side noise, then the high frequency attenuation can be improved as shown in Figure 2-3029.

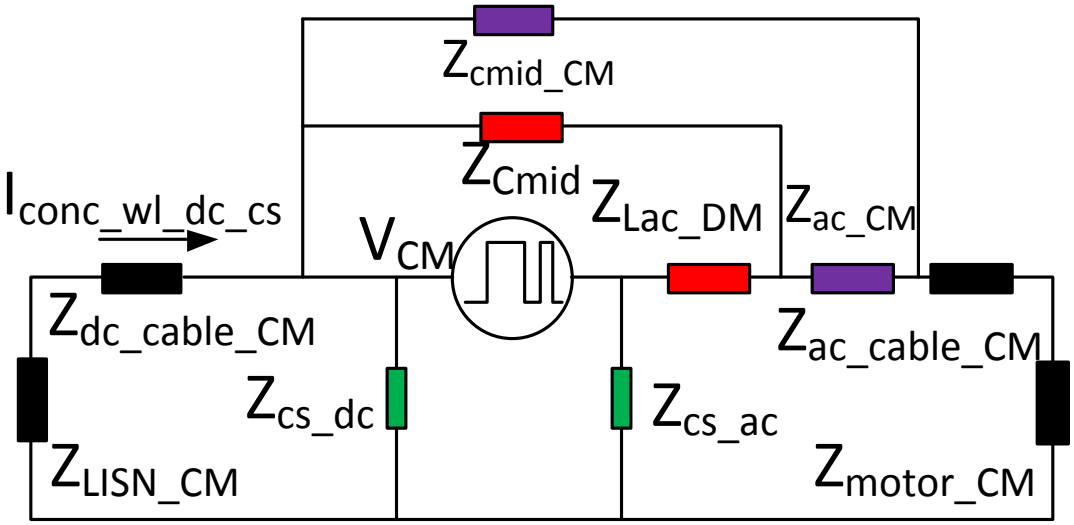
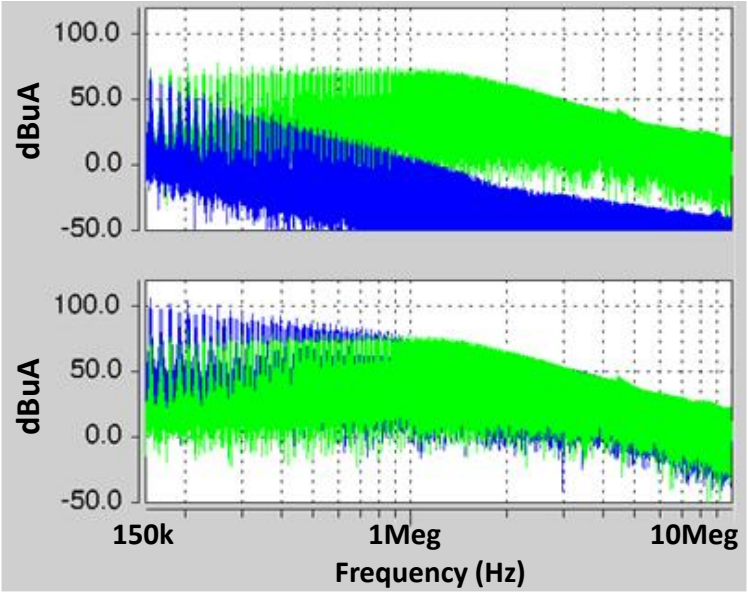


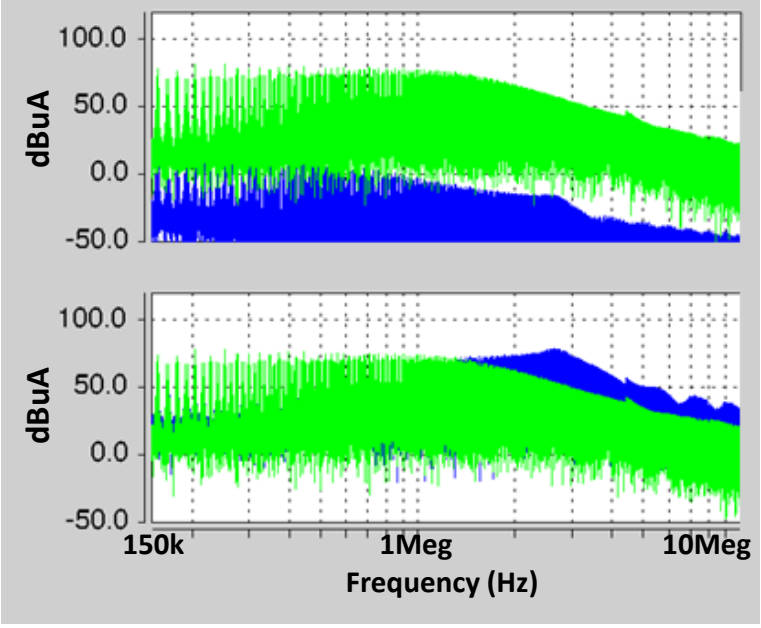
Figure 2-30 Additional L and C with floating filter for high frequency attenuation

The penalty of this topology is that there is an additional CM current added to the DM current through the DM inductors. This current is determined by the CM noise source and the impedance of $Z_{cmid}+Z_{Lacdm}$. For a given corner frequency, larger L and smaller C_{mid} will give a smaller current, while the voltage drop on L will be increased which need to be considered for a real filter design. In a motor drive system, the corner frequency of AC DM filter is usually high, which makes the additional CM current is high frequency and much smaller than DM current, and the design of DM inductor will not be influenced much, only inductor core loss will increase due to this high frequency circulating current.

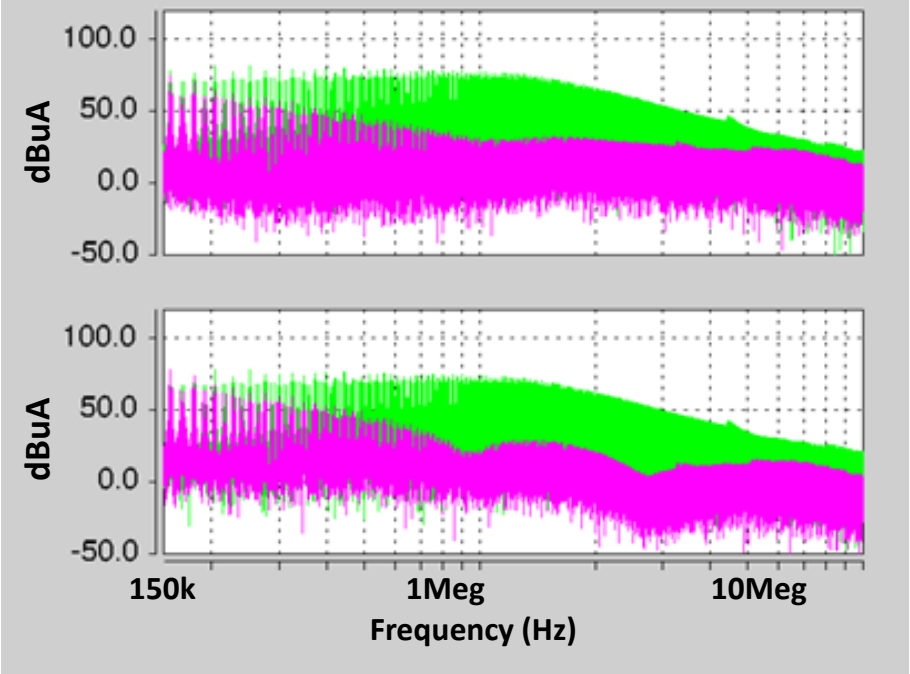
A SABER simulation was established based on a 5 kW 300 V DC-fed 3phase motor drive experimental system with a 12 meter cable.



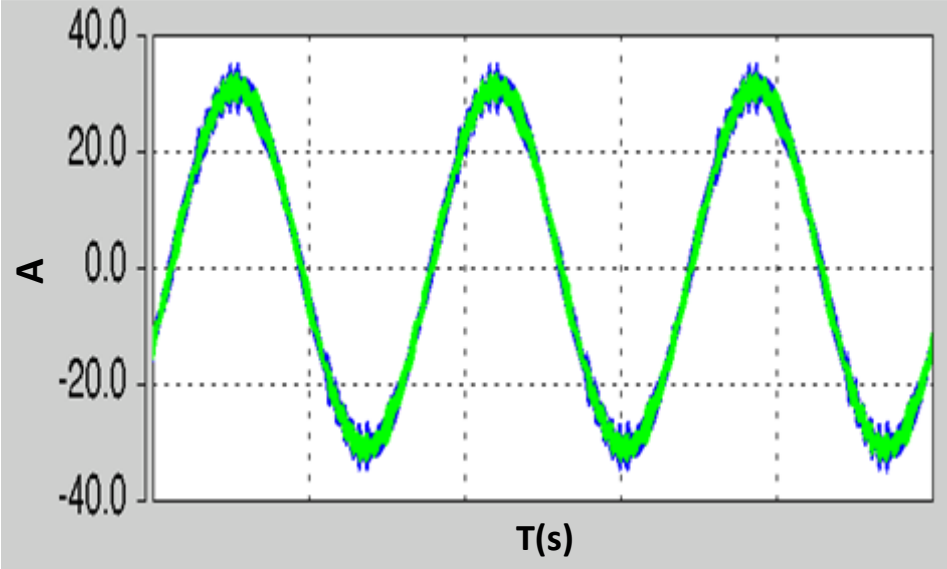
(a) top: AC CM noise with AC CM filter (blue) and without AC CM filter(green); bottom: DC CM noise with AC CM filter (blue) and without AC CM filter (green)



(b) top: DC CM noise with DC CM filter (blue) and without DC CM filter(green); bottom: AC CM noise with DC CM filter (blue) and without DC CM filter (green)



(c) top: AC CM noise with proposed (blue) and without proposed filter(green); bottom: DC CM noise with proposed filter (blue) and without proposed filter (green)



(d) AC DM inductor current with proposed filter (blue)and without proposed filter (green)

Figure 2-31 Simulation results of adding floating filters

Figure 2-31(a) shows the simulation results of AC and DC CM noise before and after adding AC side L-C EMI filter with Cy capacitor connected to ground. The results shows that if connecting Cy capacitor to ground, with AC EMI filter, the AC side EMI noise is

well attenuated while the DC side EMI noise increases. Figure 2-31(b)b shows the simulation results of AC and DC CM noise before and after adding DC side C-L EMI filter with Cy capacitor connected to ground, which shows the similar result with adding AC EMI filter if connecting Cy capacitor to ground, when the noise on one side is suppressed, the noise on the other side is amplified. Figure 2-31(c) shows the simulation results of AC and DC CM noise before and after adding proposed EMI filter which illustrates that both AC and DC CM noise is attenuated with the proposed topology. Figure 2-31(d) shows the comparison of the current through DM inductor before and after adding the proposed filter. It is clear that due to the high corner frequency of the DM EMI filter, the impedance of $Z_{cmid}+Z_{Lacdm}$ is very big and the additional CM current is high frequency and the amplitude is relatively small than the DM current which will not influence the design of DM inductor.

The proposed EMI filter is also verified through an experimental setup based on a 5 kW 300 V DC-fed 3phase motor drive system with a 40 feet cable. Figure 2-32 shows the setup of the system and test results of EMI noise and filter attenuations are shown in Figure 2-33.

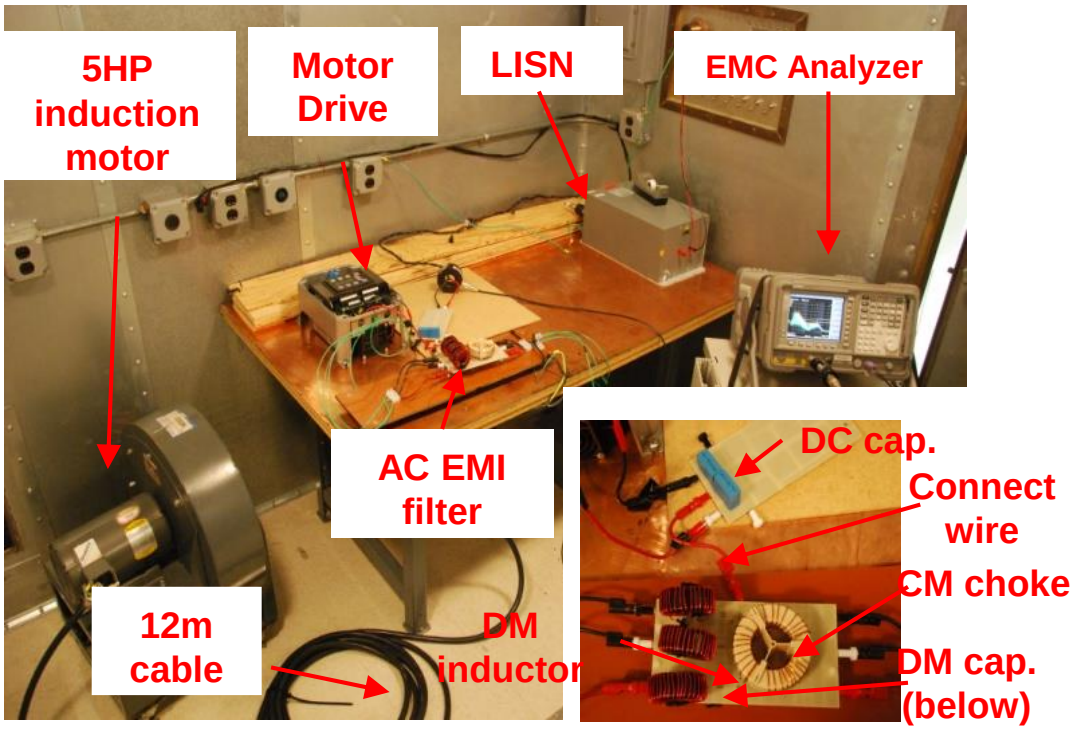
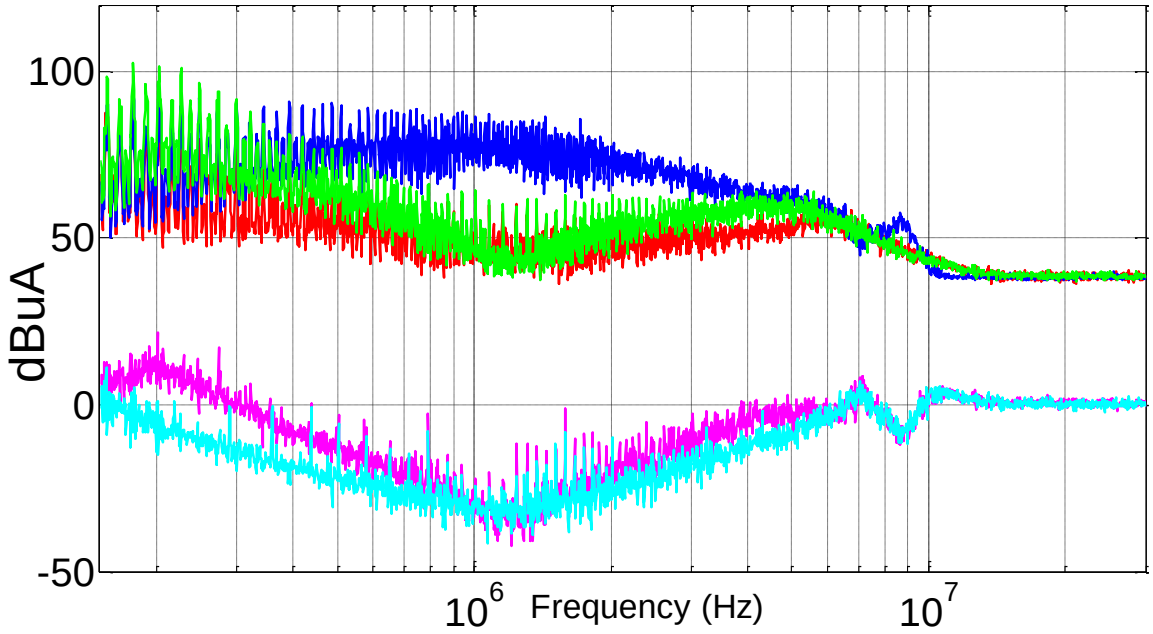
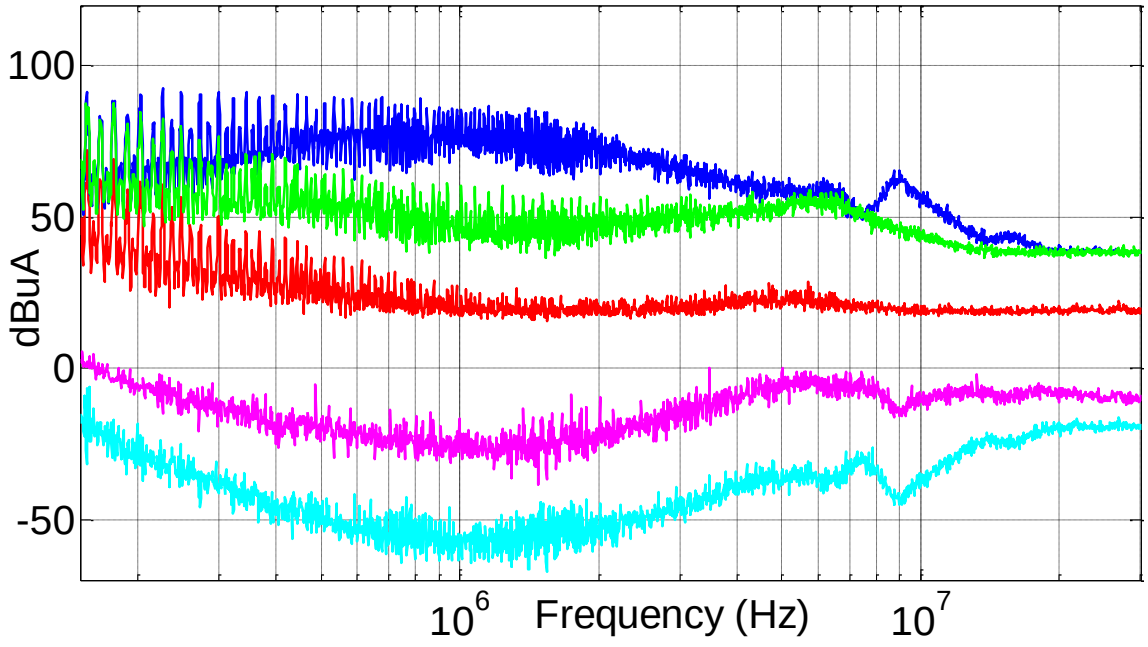


Figure 2-32 Dc-fed motor drive systems with proposed EMI filter structure



(a) DC CM EMI noise and attenuation experimental result: DC CM noise without filter (blue); DC CM noise with AC DM filter added (green), DC CM noise with proposed filter added (red); DC CM attenuation with AC DM filter added (pink); DC CM attenuation with proposed filter added (light blue)



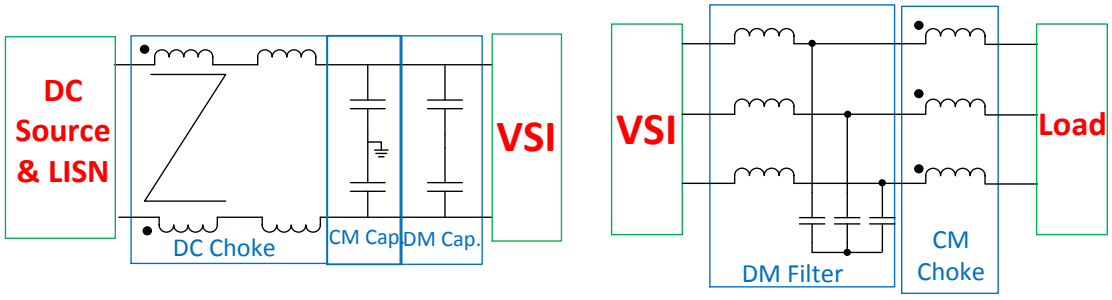
(b) AC CM EMI noise and attenuation experimental result: AC CM noise without filter (blue); AC CM noise with AC DM filter added (green), AC CM noise with proposed filter added (red); AC CM attenuation with AC DM filter added (pink); AC CM attenuation with proposed filter added (light blue)

Figure 2-33 Experimental Results of the floating filter

The experiment results show that by adding AC DM filter, since the DM inductor will increase the CM noise propagation path impedance for both AC and DC sides, the CM EMI noise of both sides are attenuated, which proves the interaction between AC and DC CM EMI noises. Moreover, by connecting AC and DC capacitors mid-point, additional attenuation is got for both AC and DC CM noise at low frequency while at high frequency, the benefit is limited due to the existence of device stray capacitances. To attenuate the high frequency noise, an AC CM choke is added after DM filter, and the results show that high frequency AC CM noise is well attenuated by adding the proposed filter.

2.4.3 EMI Filter Design Methods for Both AC and DC Sides

The proposed floating filter can confine the EMI noise within the system and reduce the EMI noise emission from the power converter effectively. However, the analytical analysis shows that the performance of the filter is highly related with the load and souce impedance of the converters which make it difficult for the accurate design of the filter parameters. Thus, traditional L-C filters are still necessary for precisely control the filter attenuation and well attenuate the noise below the standard. Considering the interaction between AC-side and DC-side filters and between CM and DM filters, certain order must be followed to minimize the impact of adding new filters into the circuit and ensure a successful filter design. A practical filter structures for ac and dc sides are shown in Figure 2-34 where LC structures are selected for AC DM filter and CL structures are selected for DC DM filter to get enough attenuation. For CM filters, since connecting C_y capacitors to ground will make it harder to design the EMI filter for the other side, only L structure is selected for both AC DC CM filter. However, CL structure is used for DC CM filter to get enough attenuation. The DC DM inductor is integrated with DC CM choke to reduce the weight of the EMI filter.



(a) DC EMI filter **(b) AC EMI filter**

Figure 2-34 Implemented AC and DC EMI filter structures

Considering the interactions between CM and DM filter, since DM filter inductor will appear in CM equivalent circuit and provide attenuation for CM noises and CM filter

capacitors are usually small which has a negligible impact on DM noises, DM filters should be designed before the CM filters to assure the accuracy of CM noise measurement and avoid overdesign. Moreover, since AC side has more harmonic components that can be easily affected by adding LC filters, AC filters should be designed before the DC filters. Thus, a filter design sequence is proposed as shown in Figure 2-35 where AC DM filter is designed at first and after AC DM noise meeting the EMI standard, DC DM noise is measured with AC DM added to the circuit to include the DM noise changing by adding AC DM filters.

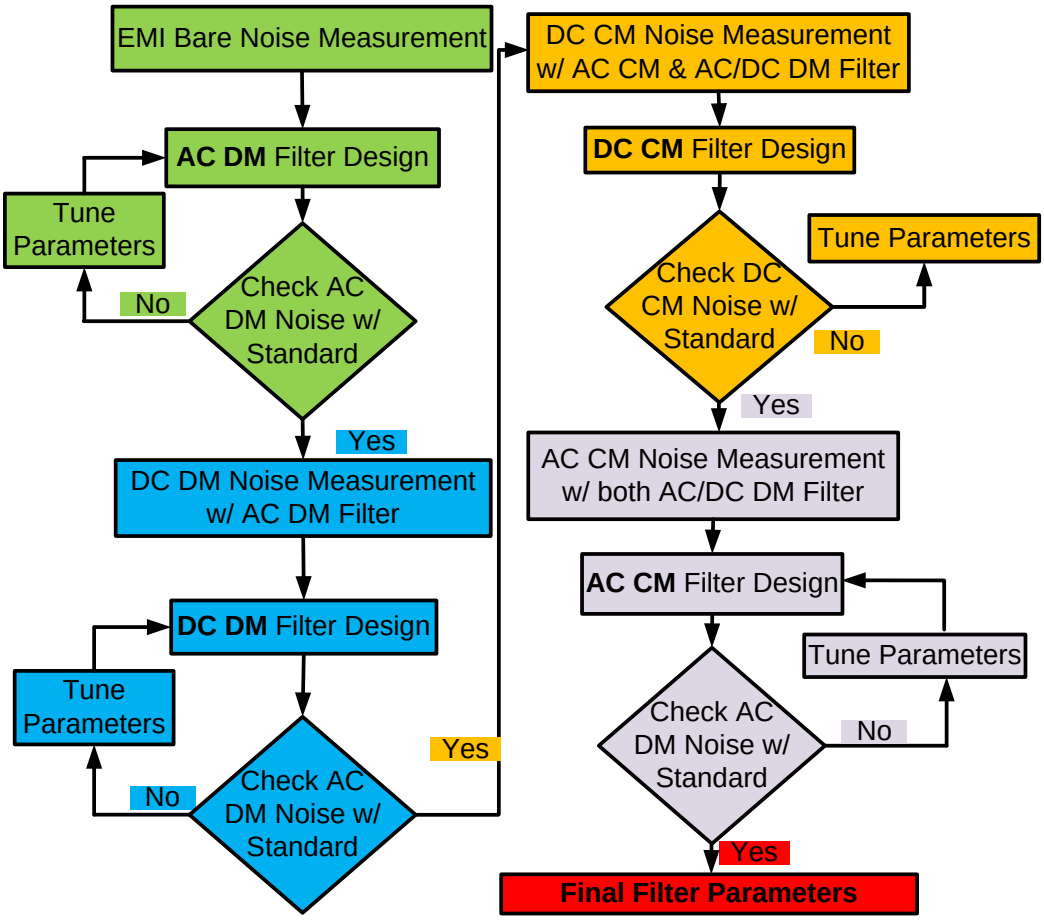


Figure 2-35 EMI filter design sequence for both AC and DC sides

CM filters are designed based on the CM noise measurement with DM filter added to the circuit in order to include the CM noise and propagation path impedance changed due to adding the DM filters. In the standard, DM side has a stricter requirement than AC side and usually DC CM noise is higher than AC CM noise in the measurement, thus DM side usually need more attenuation than AC side. Thus, CL structure is selected in the design. L structure is selected for AC CM filter to reduce the impact of connecting C_y capacitor to the ground which will make DC CM noise worse. For this system, DC CM impedance and AC CM impedance are comparable in EMI frequency range (150 kHz to 30 MHz) without any CM filter added as shown in Figure 2-36.

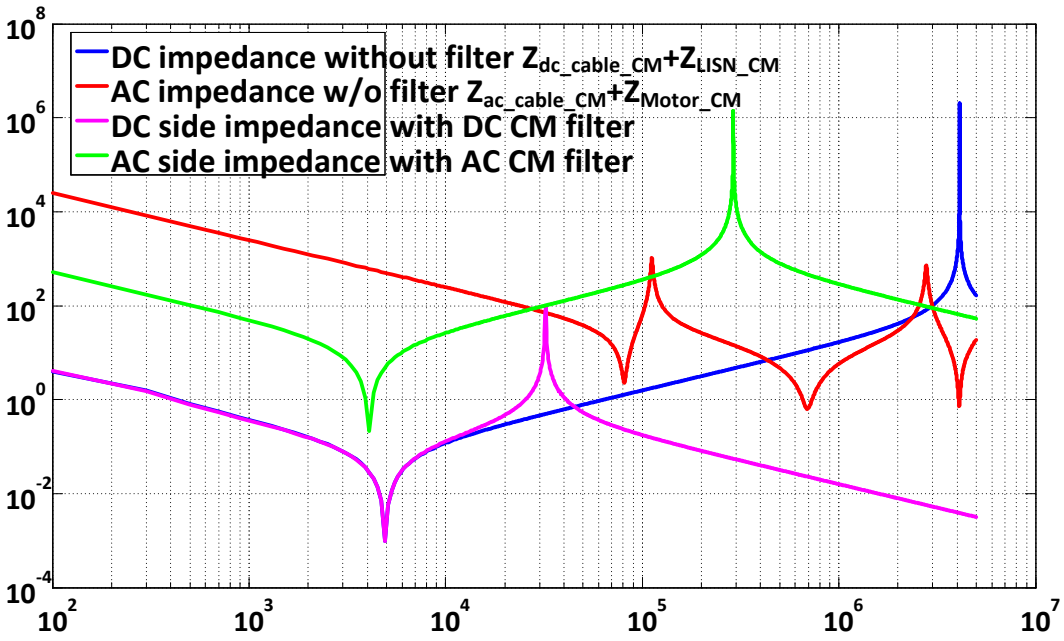


Figure 2-36 CM impedance changing with and without EMI filters
(DC CM impedance without filter : blue, AC CM impedance without filter : red,
DC CM impedance with filter : pink, AC CM impedance with filter : green).

Thus, adding filter on one side will change the propagation path impedance of both sides, which shows the interaction of CM filters. However, after adding a CL filter to dc side, the dc side equivalent impedance that is seen from AC side will be reduced and AC side impedance become dominant. In this case, tuning DC EMI filter parameters will not

change the AC side EMI noise level and DC side EMI filter is decoupled from AC side, then DC CM filter should be designed before AC side filter. After tuning of the EMI filter parameter to make DC CM noise meet the standard, AC filter can be designed based on the noise measurement after adding DC filter to the circuit. Since AC side filter is only a CM choke, adding filter to the circuit will increase the equivalent impedance seen from DC side. Thus, adding AC filter will further reduce DC noise except for some resonant points need to be checked after AC CM filter design.

2.4.4 Experimental Verification of Filter Design Methods for Both sides

Experimental verifications are carried on a 2kW 300V dc-fed motor drive system with 30 feet cables as shown in Figure 2-37. The system detailed structure is shown in Figure 2-25, where a RL load with a grounding capacitor is used to stimulate a motor load. The grounding capacitance is selected to make the system CM propagation path impedance has a resonant frequency at around 350kHz. System switching frequency is 25kHz and system fundamental frequency is 200Hz. Both AC and DC CM and DM noises are measured to verify the analysis of the interaction of EMI noise and EMI filter design and both AC and DC side EMI filters are designed to make the EMI noise meet the standard.

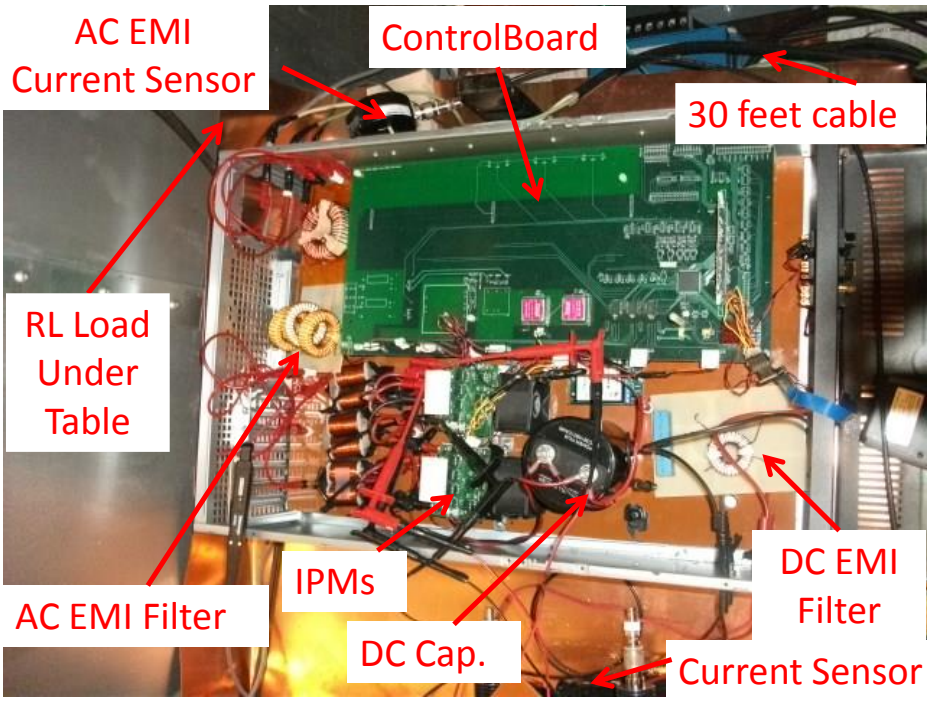
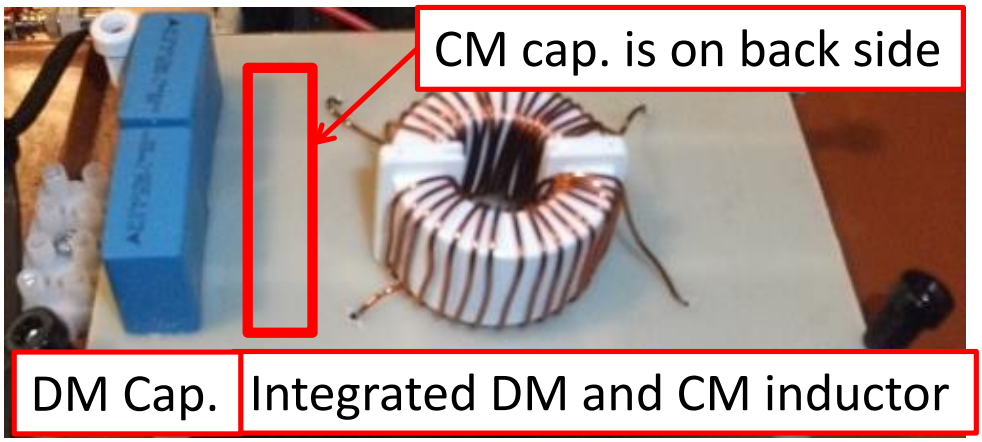
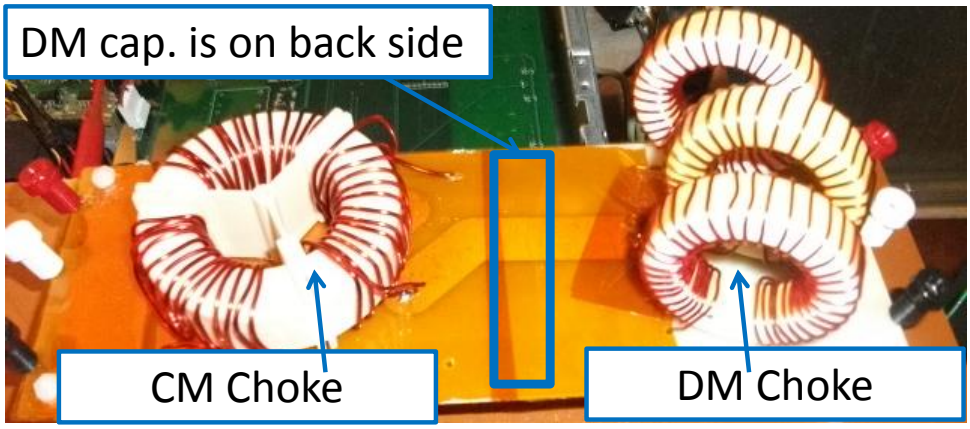


Figure 2-37 Experimental system setup for EMI filter design methods



(a) DC EMI filter



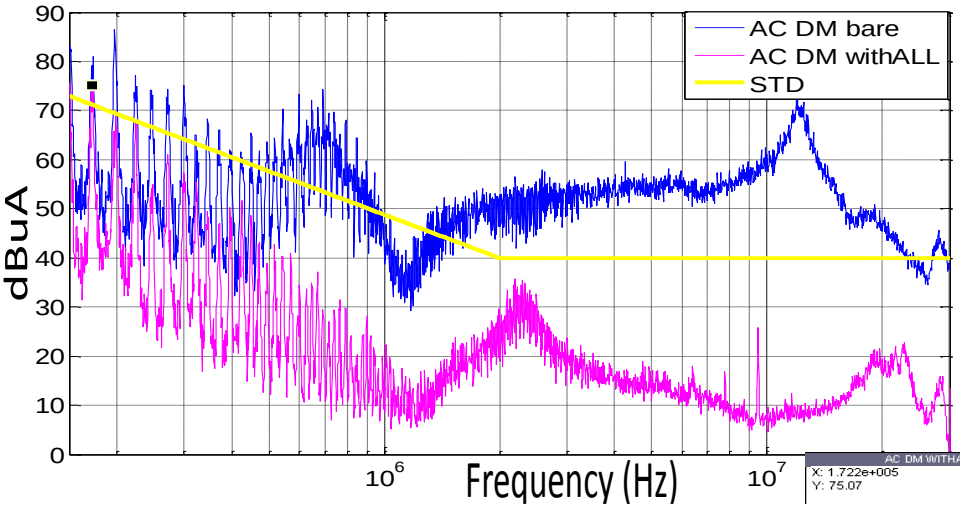
(b) AC EMI filter

Figure 2-38 Implemented EMI filters

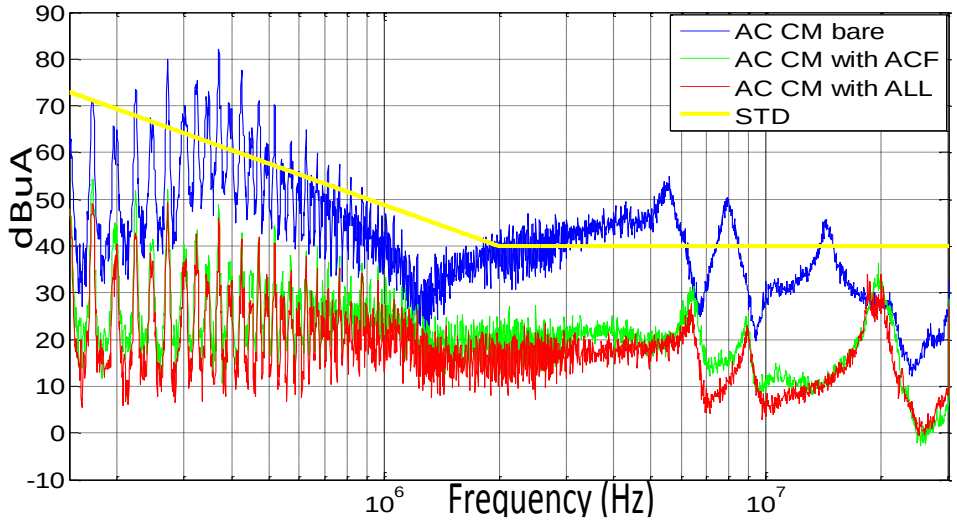
Figure 2-38 shows the EMI filters designed for AC and DC sides following the design and optimization method shown in previous chapter, where the filter structure is shown as in Figure 2-34. The component selection and EMI filter weight optimization methods are shown in Figure 2-35 and the final value selection and weight measurement for AC and DC side EMI filters are shown in Table 2-2 EMI filter design results It is noticed that the weight of the inductors are the dominant part, which takes more than 90% of the total weight of the EMI filter.

Table 2-2 EMI filter design results

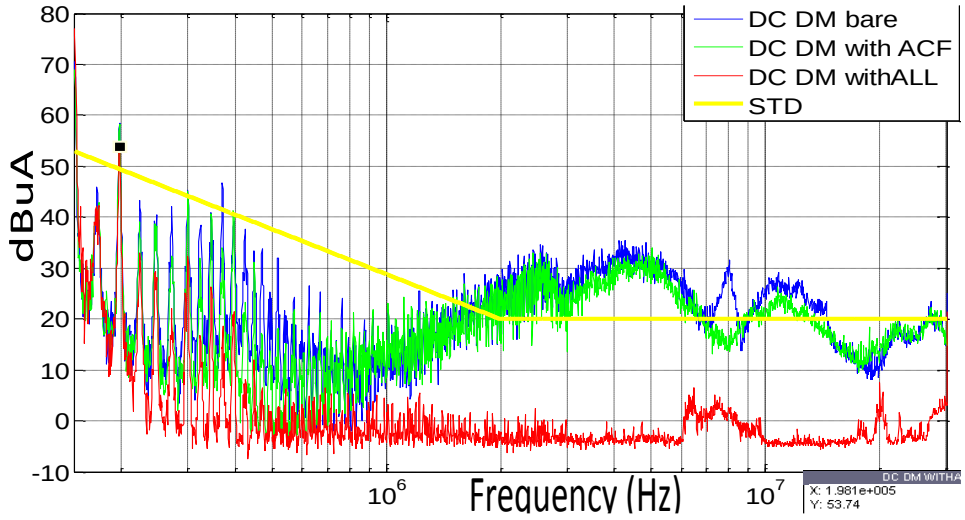
	DC-side EMI Filter			AC-side EMI Filter		
	Integrated Choke	CM capacitor	DM capacitor	CM Choke	DM inductor	DM capacitor
Value	CM:1.2mH DM:10uH	1nF	3uF	CM: 2.7mH DM: 2uH	130uH	3*5nF
Weight	180g	3g	30g	500g	270g	9g



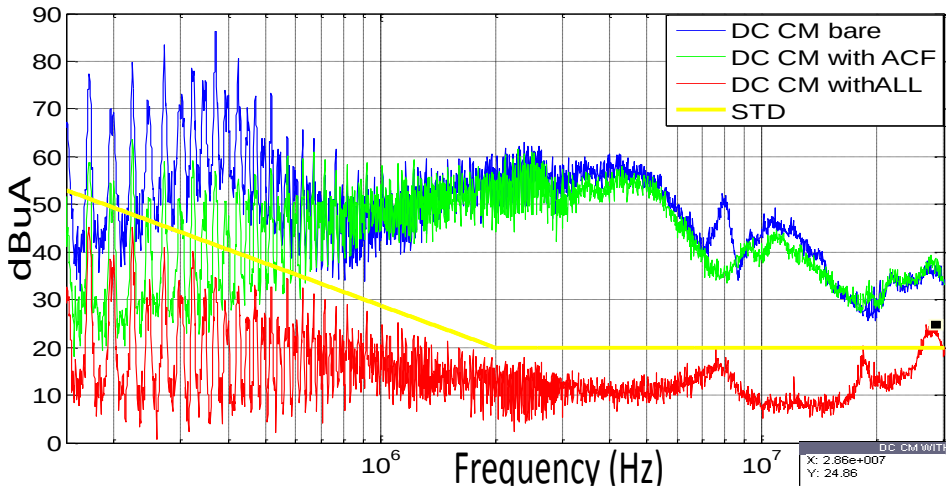
(a) AC DM EMI noise: bare noise: blue; with AC&DC filter: pink



(b) AC CM: bare noise: blue; w/ AC filter: green; w/ AC&DC filter: red



(c) DC DM: bare noise: blue; w/ AC filter: green; w/ AC&DC filter: red



(d) DC CM: bare noise: blue; w/ AC filter: green; w/ AC&DC filter: red

Figure 2-39 EMI test results of the experimental system

Measurement of EMI noise before and after adding EMI filters are shown in Figure 2-39. It is clear that both AC and DC noise meet the EMI standards by adding the designed EMI filter following the proposed design and optimization method, which verifies the validity of the proposed EMI filter design method. Moreover, the results show that both AC and DC CM noise will be changed after adding AC CM filters, which verified the interaction between AC and DC sides. Meanwhile, adding AC DM filters will attenuate AC DM noise effectively but also change DC DM noise, which indicate the interaction between AC and DC sides. Besides, both ac-side and dc-side CM noise is reduced after adding AC DM filter on AC side which verified the CM noise source change by adding DM filters on the AC side.

2.4.5 Summary and Discussion

In this section, the interaction between EMI filters are analyzed in detail for the applications where EMI filters are needed for both input and output sides of the power converter, the results show that input and output DM noise is decoupled due to the existence of the dc link capacitor and the impact of adding filters mainly happens when it change the

noise source for the other side. Meanwhile, the interaction between CM filters is more significant since the input and output sides share the same propagation path, adding CM filters on one side will change the propagation path impedance and change the performance of the EMI filter on the other side. For conventionally designed filter that is designed for only one side, usually C_y capacitors are connected to the ground which will introduce a low impedance path for the CM noise of the other side and when the noise on one side is suppressed, the noise on the other side is amplified. With this consideration, an improved filter topology for dc fed motor drive system is proposed where both input and output filters are needed. By connecting the mid-point of AC side DM capacitors and the mid-point of DC link capacitor in motor drive system, the huge DM capacitors can help to limit the CM noise within converter and provide significant attenuation compared with conventional design for both input and output noise. An analytical model is proposed for evaluating the attenuation of the proposed structure in frequency domain. Both simulations and experiments verified this proposed improved method. The proposed method gives potential to reduce conventional design filter weight or volume to realize the same EMI attenuation.

Moreover, a design and optimization method for EMI filters on both input and output side is proposed. To minimize the impact on the EMI noise of one side caused by adding filter on the other side, certain design order must be followed to design AC and DC CM and DM filters. Simulation and experimental results verify the interaction between AC and DC filters and show that EMI filters can be designed to suppress both AC and DC EMI noise to meet the standard with the proposed EMI filter design method.

2.5 Implementation and Weight Minimization of EMI Filters

Successful EMI filter designs can provide engineers with different combinations of inductor (L) and capacitor (C) values that can effectively suppress the noise along with the working condition of the corresponding L and C. With the desired value and the estimated working conditions, a good EMI filter implementation method can ensure a successful hardware implementation with proper design of L and C to ensure an effective noise suppression in real EMI measurement with the minimum weight/size of the filter.

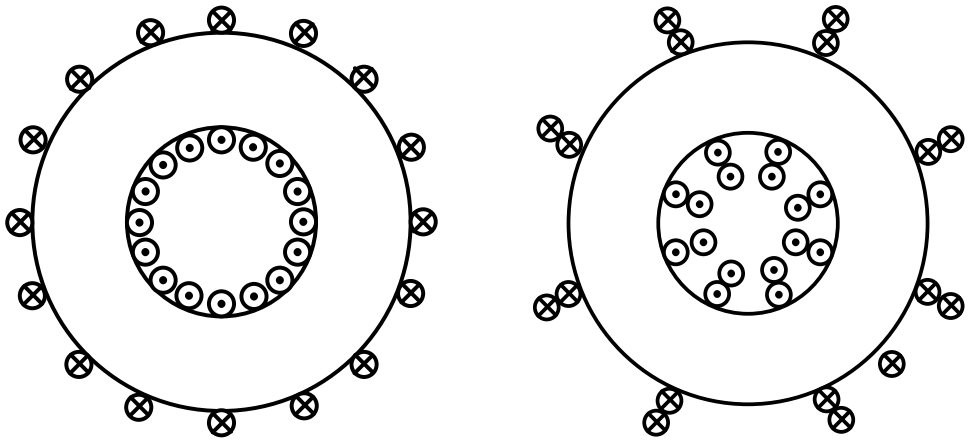
In EMI filters, capacitors are in parallel with the power circuits, thus the current through capacitors is limited and the weight/size of the capacitors are relatively small. As shown in the experimental system in the previous section, capacitors takes less than 10% of the total passive component weight in the system. Meanwhile, most of the capacitors are selected from commercial products unless implementing certain material and process for customized capacitors such as LTCC capacitors [81]. Once the value and working condition (mainly current/voltage stress) of the capacitors are fixed, the size and weight of the capacitor are usually fixed and there is little freedom to optimize the weight of capacitors. However, most of the inductors are in series with system power circuits, thus the current through inductor is relatively big which increase the loss of the filter, meanwhile the energy density of inductor is lower than capacitor from weight point of view, thus, the size/weight of the inductors take a big portion of the total EMI filter. Moreover, the inductor usually are customized or semi-customized from certain magnetic material and core shape. One can select and optimize the design variables such as materials, core shapes, wire gauges, turn numbers and etc. to get an optimized inductor with required characteristic

and minimum size/weight. Thus, the filter weight minimization will focus on the weight minimization of inductors.

2.5.1 Constraints of Minimum Weight Optimization during Filter Implementation

During the optimized inductor implementation, different constraints should be considered for a successful mini-mum size/weight inductor implementation. These constraints include:

1) Physical fitness; for the inductors that are used for power storage, multiple layer (as shown in Figure 2-40(a)) winding structures can be used to maximize the utilization ratio of the winding area (increasing the filling factor), however, multi-layer structure will increase the parasitic capacitance (EPC) of the inductor and make filter lose the attenuation at higher frequency. For EMI filters, due to the limitation of parasitic capacitance (EPC) of the inductors, single layer structure winding is preferred (as shown in Figure 2-40(b)).



(a) Multi-layer winding **(b) Single layer winding**

Figure 2-40 Single layer and multi-layer winding structure

Although single layer structure will reduce the filling factor of the inductor and may make the inductor bigger if the physical fitness constraint become the strict

constraint during optimization process, it is necessary to keep the single layer winding structure for parasitic capacitance minimization if high attenuation is needed from the filter at higher frequency.

2) Limitation of the maximum magnetic flux density (B_{max}) to avoid core saturation; the maximum allowable magnetic flux density (B_{sat}) on a core is limited by the characteristics of the core material. If the magnetic flux density is higher than B_{sat}, the core will be saturated and the inductance will be reduced significantly. This will make the filter lose its functionality and may damage the system, thus the maximum magnetic flux density (B_{max}) should be limited according to the B_{sat} of the core material and certain margin is necessary to avoid saturation during some transient of the circuit. The magnetic flux density is determined by the volt-second (VS) added on the inductor, core area(A_c) and turn numbers(N_{turn}) as shown in (2-22).

$$B_{max} = \frac{VS_{max}}{N_{tum} A_C} \tag{2-22}$$

When VS is high, the inductor should be enlarged or turn number will be increased to limit the flux density on the core which make the inductor heavier. VS on the inductor is determined by the impedance of the system and the L and C values selected during the filter design process. Thus inductor value cannot directly indicate the size of the inductor [93]. The VS on the inductor should also be considered in the filter design process to avoid certain design regions that create resonance in the circuit and result in a huge inductor implementation. Figure 2-41shows an design example of AC CM L-C filter for the 2kW demo system shown in section 2.4 with a 20nF CM capacitor, which shows that smaller

inductance will not ensure a smaller inductor weight, since the volt-second determines the filter weight in this case.

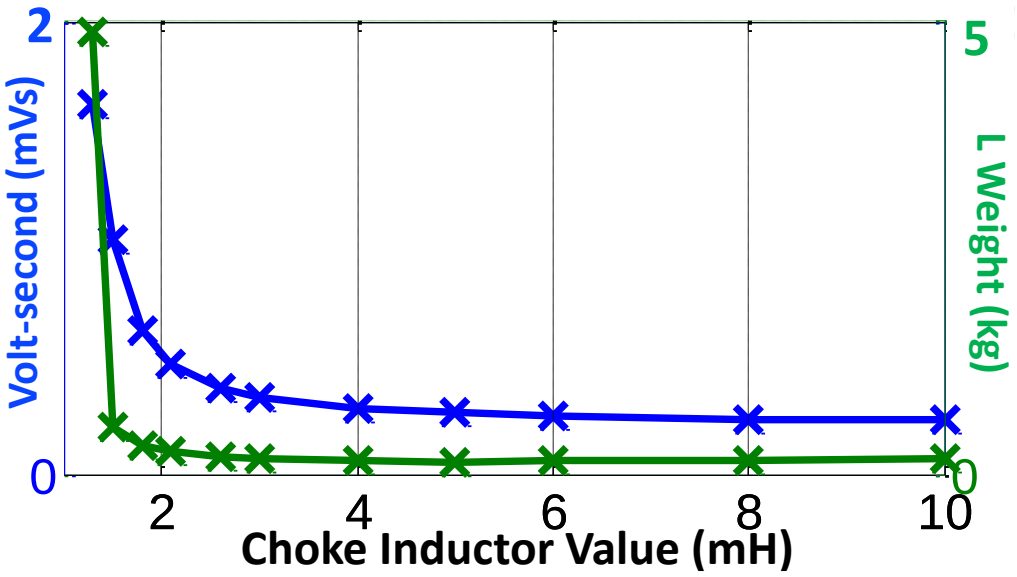


Figure 2-41 Inductor design results with different inductance

3) Inductor value requirements for enough attenuation for EMI noise, the filter design process will provide the minimum inductor value needed for adequate attenuation, larger inductance will provide higher attenuation in theory, however, larger inductance will change volt-second sharing in the system and change the whole inductor design. Moreover, larger inductors have larger parasitic parameters and may make the HF attenuation of the filter worse. With higher turn numbers the inductance at lower frequency is higher, but the higher frequency impedance will be reduced and may result in the filter design failure if higher attenuation is needed for high frequency range.

4) Limitation of inductor parasitic parameters for high frequency attenuation; Due to the parasitic parameters of the inductor and capacitor, the filter attenuation will be lost at higher frequency. Thus, when high-frequency attenuation is require from the design process, the corresponding limitation of parasitic parameters also need to be

considered. The limitation can be got from the filter design process using filter insertion gain which is prosed in section 2.3. The parasitic capacitance of the inductor can be predicted using analytical methods based on the winding and core structures.[81] and the parasitic resistance of the inductor is related with the core loss and winding loss of the inductor, with a model for inductor loss, the parasitic resistance can also be modelled. Besides, fine element analysis (FEA) method can also be applied for inductor modelling as shown in many works. [81].

5) Limitation of filter loss and system efficiency; since the inductor current is system full current with switching frequency ripples, the skin effect and proximity effect make the equivalent conducting area smaller and the winding loss on the inductor are not negligible. Moreover, the core loss on the EMI filters especially on CM filters also need to be considered. Inductor core loss is related with the VS excitation on the inductor. Originally, Steinmetz equation is used for core loss estimation, however, since core loss generation in magnetic materials is complicated and none linear, different improved Steinmetz equations are proposed to improve the model accuracy of the inductor core loss under different excitations and different experimental measuring methods are also studied for accurate core loss measurement. In this work, the core loss calculation is based on the Steinmetz equation method. When certain filter is added into the system, the current through the inductor can be calculated in frequency domain from the equivalent circuit shown in section 2.2 and then the magnitude of different order of switching harmonics is known.

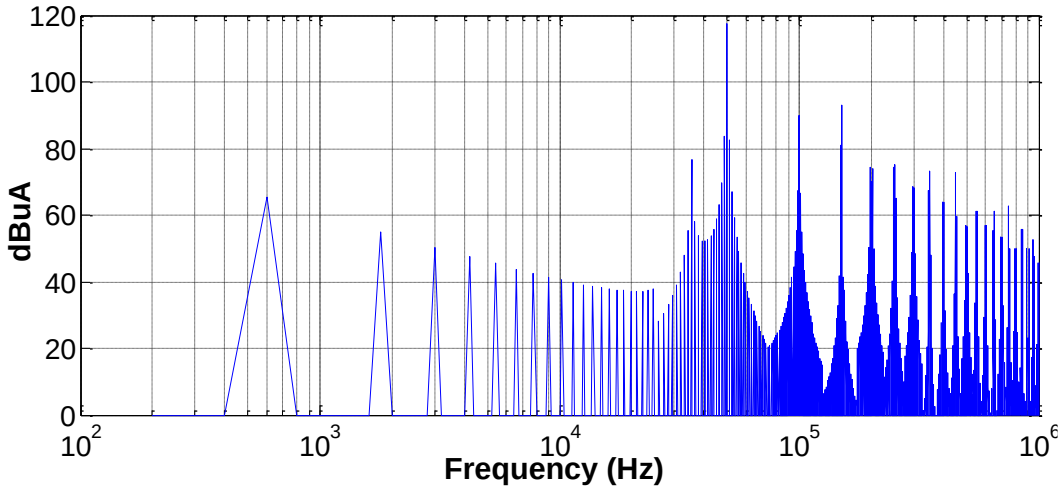


Figure 2-42 Frequency domain calculation results of the current through CM inductor

Figure 2-42 shows the frequency domain calculation result of the current through CM inductor with the design CM filter added to the circuit. The higher harmonics are identified with the frequency and the magnitude of the harmonic, then the core loss on the inductor is calculated as shown in (2-23)

$$P_{Loss} = \sum_i \left(a \left(\frac{LI_{max\_i}}{A_C N_{turn}} \right)^c \left(f_{max\_i} \right)^d V_c \right) \tag{2-23}$$

where, a,c,d is the core loss coefficients that can be calculated from material datasheet, L is the inductance added in the circuit, I_{max_i} is the magnitude of the i^{th} order harmonics, Ac is the core area, N_{turn} is the turn number, f_{max_i} is the frequency of the i^{th} order harmonics, V_c is the core volume of the designed inductor. With (2-23) the core loss can be estimated and be used in the optimization process. This core loss estimation method assumes that the core loss generation in the core can be linearized to the frequency of the VS excitation applied on the core. Previous studies has shown that this assumption will introduce errors in the core loss estimation and the error depends on the material type of the cores. For metal based materials such as FINEMET or Amorphous materials which is widely used in

medium power applications, eddy current is the main reason of core loss. The error is relatively small. However, for ferrite materials that is widely used in low power applications with higher switching frequencies, hysteresis loss will dominant in the core loss distribution, then this method will have big error and not valid for such applications.

6) Limitation of inductor temperature rise. Due to the winding and core loss generated during operation, both winding and core temperature will increase. Limited by the material characteristics (Curie temperature of the magnetic cores or maximum temperature for insulating materials of windings), the temperature rise of the core and windings is limited. The temperature is determined by the loss, core shape and cooling conditions.[106]. There are many studies that provide the thermal models based on Fine Element Analysis (FEA) or simplified thermal circuit models that can estimate and consider the temperature during the design process.

With the consideration of these design constraints and accurate models, a mathematical model can be developed for the optimization of inductors for minimum weight/size implementation. Different optimization methods such as enumeration method or Lagrange method can be applied to solve the model and design the optimized inductors.

2.5.2 Inductor Implementation with Weight Minimization

With the consideration of all the constraints above, when the required inductor value and working condition of the inductors are known from the filter design procedure, the minimum weight implementation can be achieved following the optimization procedure shown in Figure 2-43.

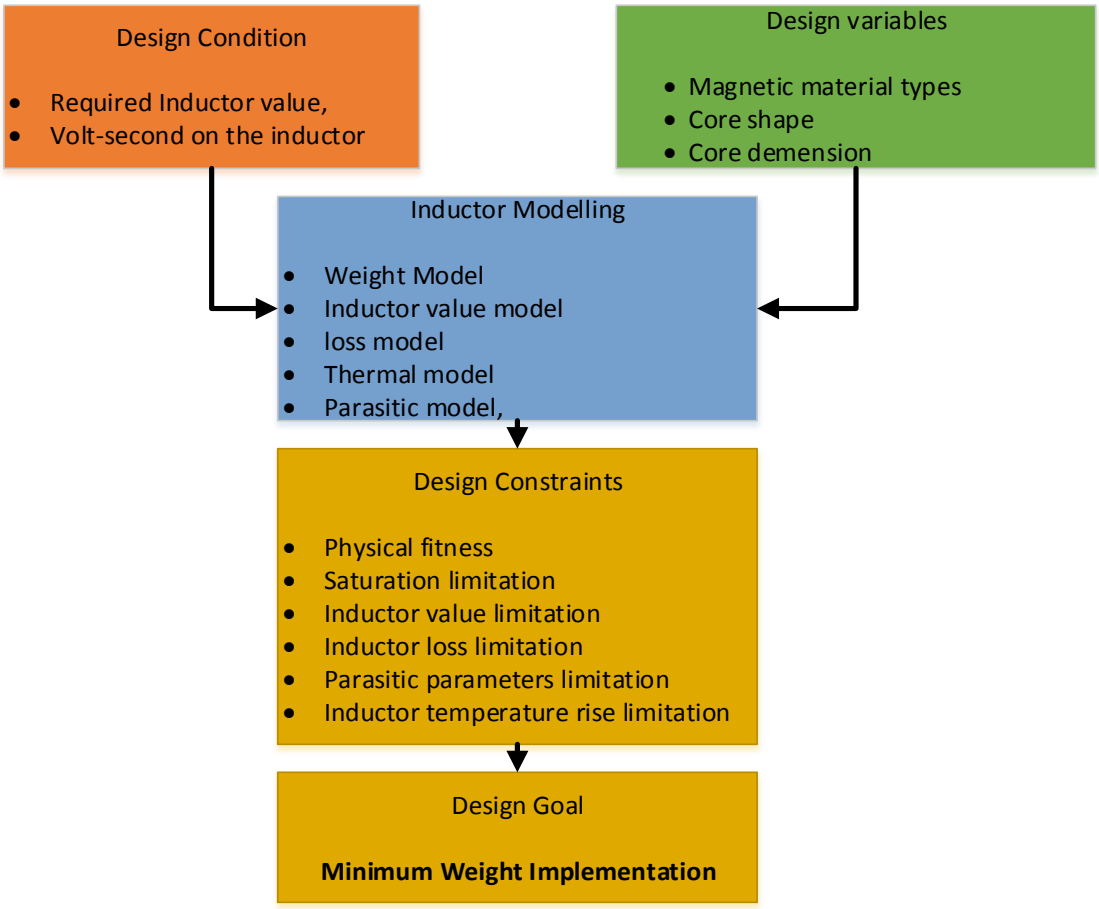


Figure 2-43 Inductor weight minimization procedure

With the proposed design procedure, a minimum weight implementation of the inductor can be insured, however, due to the limitation of the accuracy of the system level EMI analysis model at high frequency, adjustment may still be necessary for enough attenuation at higher frequency to ensure a successful EMI filter design.

2.5.3 Summary and Discussion

In this section, the minimum weight filter implementation method is discussed in detail. Several constraints that need to be considered during the minimum weight optimization for filter implementation is presented. With a required inductance and estimated working condition of the inductors, the minimum weight should be optimized with the constraints including physical fitness, saturation limitations, inductor value

limitations, inductor loss limitations, parasitic parameter limitations, inductor temperature rise limitations and so on. Different inductor models such as loss models, parasitic models are present to design the inductor according to these constraints. The accuracy of the final optimization result is highly related with the accuracy of the models used for the constraints. Inaccurate models may introduce errors to the absolute optimization results, however, it is still reasonable to relatively compare different design conditions such as different topology or modulation methods using the same models and design procedures. The relative compare results can still justify the benefit or drawback of these design conditions on filter weight reduction.

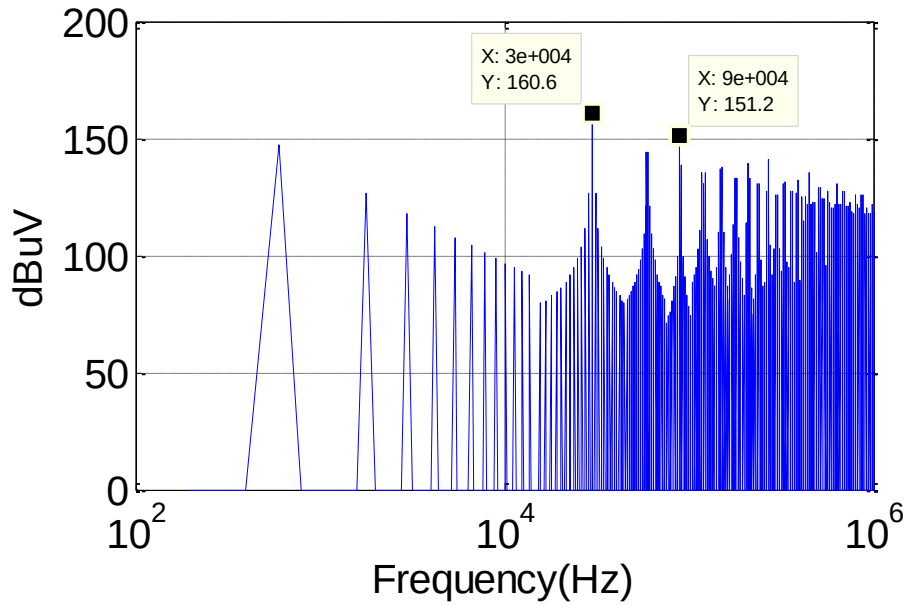
2.6 Impact of Switching Frequency on EMI Filter Design

The switching frequency of the power devices in a power converter is a very important design parameter. It determines the power losses on the semiconductors and directly related with the weight and size of the heat sinks or cold plates. Switching frequency also determines the design of the passive component that used for energy storage purpose such as the dc link capacitors and boost inductors. Usually increasing the switching frequency will decrease the energy needed to be stored in the passive components, thus the passive components that used for energy storage purpose such as the dc link capacitors and boost inductors can be reduced. Changing switching frequency will also change system EMI noise source. Since the EMI standards usually does not start from zero, the impact of switching frequency on the weight and size of EMI filter is not the same as the energy storage components. Moreover, since the current noise is determined by both the noise sources and the propagation path impedance, changing switching frequency will only change the noise source. This section will present a systematical design method to select

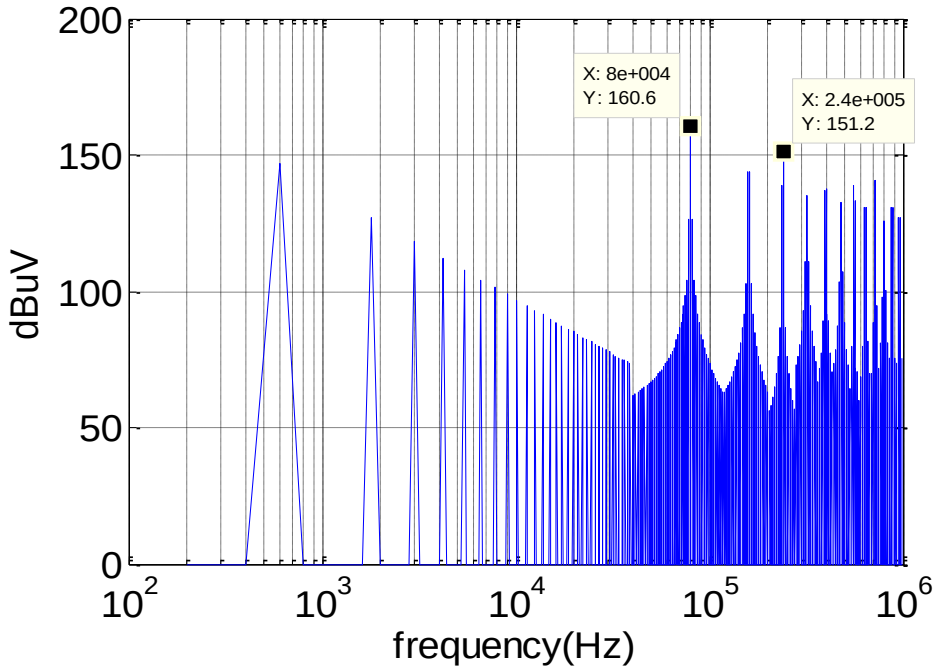
the optimized switching frequency to get the minimum EMI filter weight using the proposed system modeling and filter design methods. The two level system presented in section 2.4 will be taken as an example. System EMI models are built using the proposed modeling methods, the noise source is calculated using DFIT method with different switching frequencies. Then, considering the propagation path impedance, EMI filters are designed for converters with different switching frequencies but the same propagation path impedance. Finally, the weight of the EMI filters are estimated using the proposed filter implementation methods to show the real impact of system switching frequency on the size and weight of the EMI filters.

2.6.1 Impact of Switching Frequency on Noise Spectrum

Device switching will generate noise in the system, thus change switching frequency will change the noise source in the system. The proposed design-oriented EMI modeling method shows that the noise source can be calculate using DFIT method, when the modulation scheme, switching frequency and modulation index are fixed. Figure 2-44 shows the calculation results of the CM noise voltage source in the equivalent model with 30 kHz and 80 kHz switching frequency and 200Hz fundamental frequency. It is clear that the peak points of the EMI noise are different switching harmonics. Changing switching frequency will change the frequencies of these harmonics but the magnitude of the voltage harmonics will keep the same. For instance, the magnitude of the third order harmonics of 30 kHz converter (located at 90 kHz) is the same with the magnitude of the third order harmonics of 80 kHz converter (located at 240 kHz). In other words, increasing switching frequency will expand the voltage noise source spectrum and push the switching energy to higher frequency.



(a) Switching frequency fs= 30 kHz



(b) Switching frequency fs= 80 kHz

Figure 2-44 AC CM noise source calculation results with different switching frequency

The proposed modeling method also shows that the EMI noise is determined by both the noise source and propagation path impedance, even though magnitude of the third order harmonics are the same, since the propagate path impedance will be different since the frequency is different, the current spectrum is not the same as the voltage spectrum. Figure

2-45 show the propagation path impedance of the system and the calculated CM current spectrum is shown in Figure 2-46. Since there is a resonance in the CM propagation path at around 240 kHz, if there is also a voltage excitation near 240 kHz, there will be a peak in the current spectrum. Since the third order harmonics of the 80 kHz converter is located at 240 kHz, both of the current spectrums shows the resonant peak at around 240 kHz. This is also true for 30 kHz conditions, since the 7th, 8th and 9th order switching harmonics are all located near the e frequency range with low impedance, the current spectrum shows multiple peaks. Since the magnitude of 8th order harmonics is lower that 3rd harmonics, the magnitude of the current noise peak if lower in 30 kHz converter than it in 80 kHz converter.

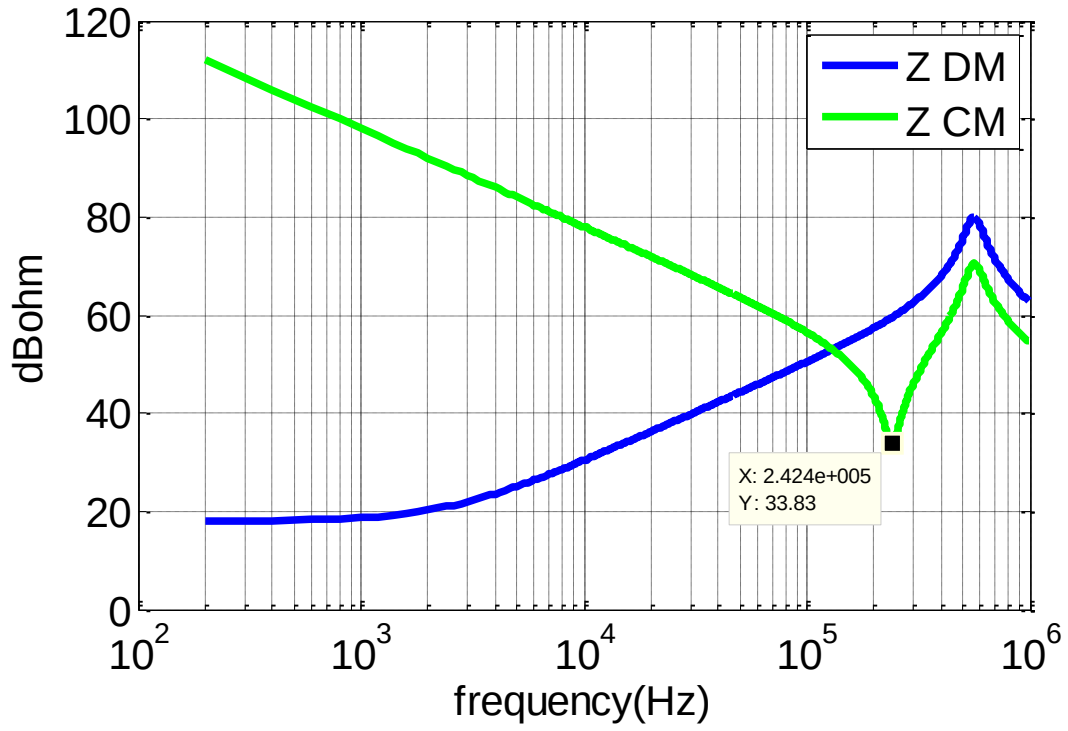
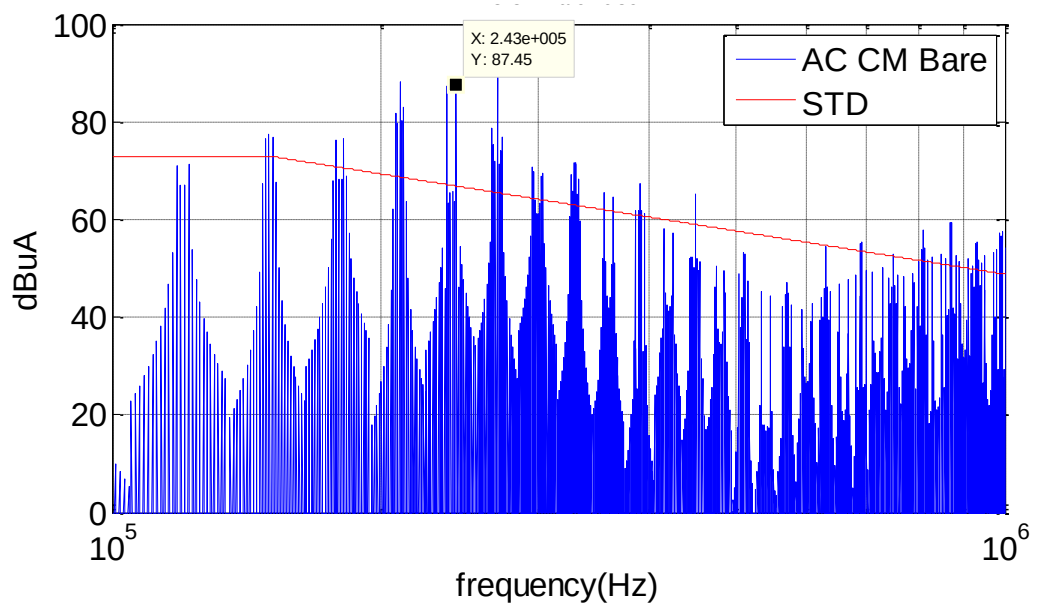
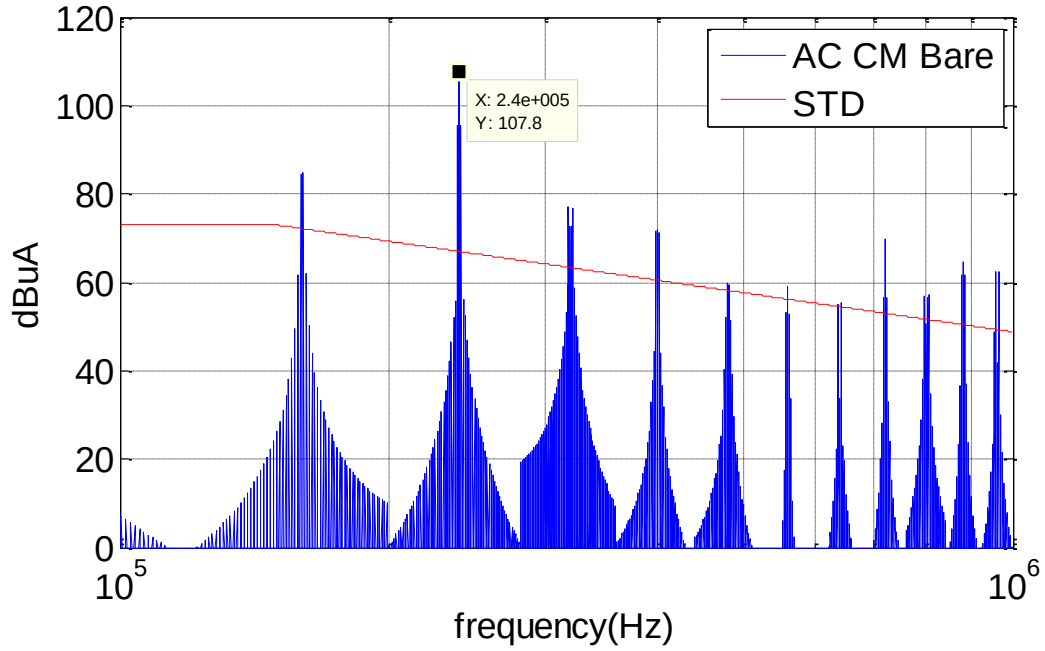


Figure 2-45 Propagation path impedance



(a) Switching frequency fs= 30 kHz



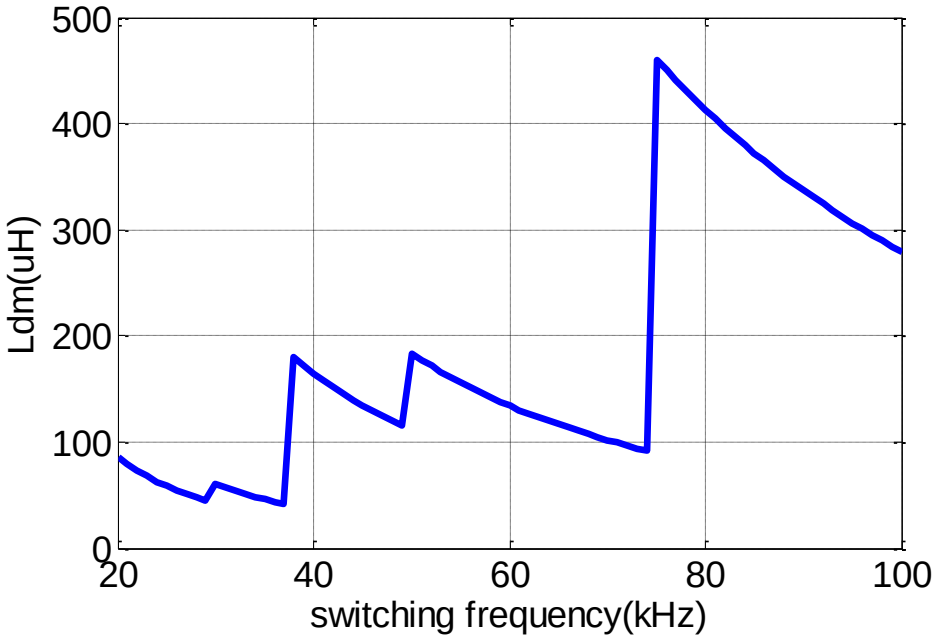
(b) Switching frequency fs= 80 kHz

Figure 2-46 Calculated AC CM current noise spectrum

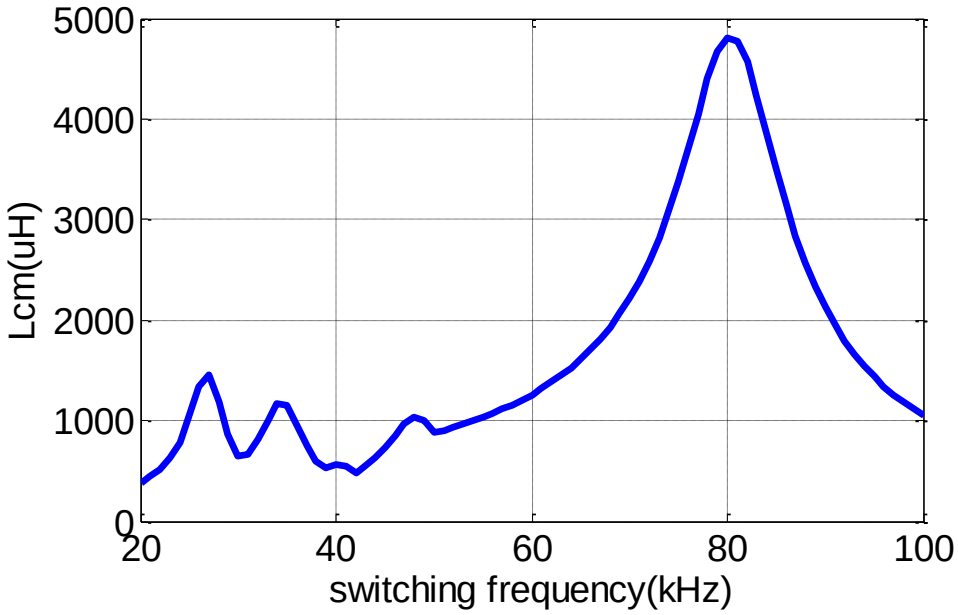
2.6.2 Impact of Switching Frequency on Filter Parameter Selection

With the information of system current noise, the EMI filters can be designed following the proposed design method for power converter systems. Figure 2-47 shows the

sweeping results of designed minimum inductor values versus the switching frequencies of the converter for CM and DM filters respectively.



(a) DM inductance VS switching frequency



(b) CM inductance VS switching frequency

Figure 2-47 Sweeping results of inductor value versus the switching frequency

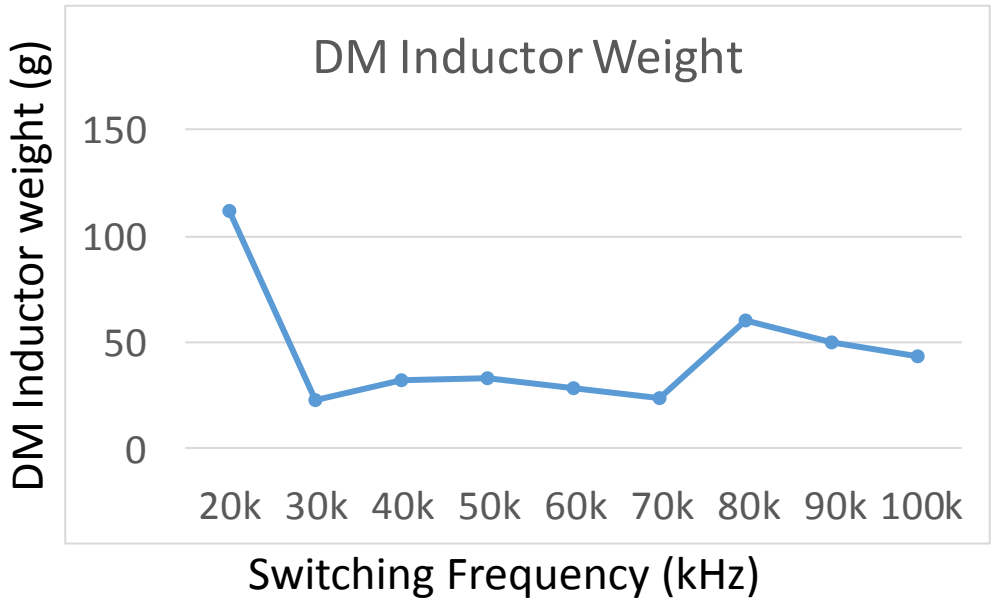
With the increasing of the converter switching frequency, the voltage harmonics that determine the EMI filter design will be pushed to a higher frequency, if system impedance

do not have resonant peaks and keep flat or increase as the DM impedance in the system, the critical frequency that determines the EMI filter design will be push to higher frequency with small increase of the attenuation due to the standard, the impedance needed will decrease until the lower order harmonics enter the EMI range and determine EMI filter design, then the inductance needed will become bigger, thus a "zig-zag" curve will be got as shown in Figure 2-47(a). It need to be noticed that the "zig-zag" curve is only for certain propagation path impedance. If the propagation path impedance has resonances as the CM impedance in the system, then increasing switching frequency will not change the critical point significantly, the filter design is always determined by the attenuation needed at the resonant frequency, in such case there will be no "zig-zag" shape of the relationship between inductor value and corner frequency. The curve will show similar shape as what is shown in Figure 2-47(b). Large inductance will be needed at several frequencies will since the voltage harmonics under such frequencies will match with the impedance resonance. The current peak will be amplified and larger inductance is needed for higher attenuation.

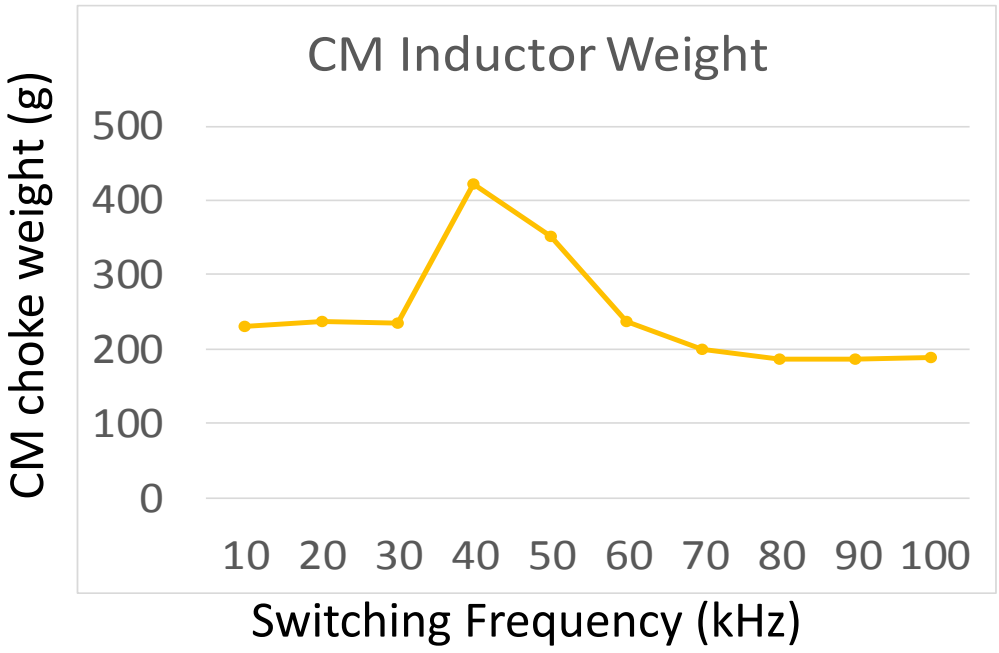
2.6.3 Impact of Switching Frequency on Filter Weight

It has been discussed in section 2.5 that the weight of inductor is not only determined by the inductor value, under certain design conditions, it is also related with the volt-second on the inductor. Figure 2-48 shows the implementation design results of the inductor weight with different switching frequencies. For the DM inductor design, the inductor weight is limited by the inductor value since the high frequency volt-second is relatively low. Thus the inductor weight is consistent with the inductor value. When inductor value is higher under certain switching frequency, the inductor weight is also higher, except when

the switching frequency is very low, the filter corner frequency will located at certain frequency where the voltage excitation is also high, then the voltage ripple is high which make the inductor weight higher without damping.



(a) DM inductor weight



(b) CM inductor weight

Figure 2-48 Inductor weight design results with different switching frequency

However, the design results for the CM inductors are different, it is noticed that the inductor value is highest with 80 kHz converter switching frequency however, the weight design results show a maximum point weigh 40 kHz, and this is because the weight is limited by the volt-second on the inductor instead of inductor value for CM chokes. With 40kHz switching frequency, the resonant frequency of the designed CM filter is also located at around 40kHz, thus the volt-second is amplified for 40 kHz design condition, and the inductor is bigger. With higher switching frequencies, the inductor value will be larger and the resonant frequency is lower, since there is not voltage excitation at the resonant frequency, the volt-second on the inductor is relatively small and the inductor weight is smaller. It need to be noticed that with higher switching frequency, the gap between different order of harmonics is larger which provide more freedom for choosing inductor values to make the resonant frequency of the EMI filter located at the frequency with small voltage excitations to avoid high volt-second.

2.6.4 Summary and Discussion

Using the proposed EMI prediction models and inductor implementation methods, this section presented a detailed analysis on the impact of switching frequency on the weight of EMI filters. The results show that increasing switching frequency will expand the voltage noise source spectrum and push the switching energy to higher frequency. However, the EMI is determined by both the noise source and propagation path impedance. The experimental system shown in section 2.2 is taken as an example and filters are design using the proposed design method. The results show that the relationship between the filter inductor value and the switching frequency is related with the propagation path impedance. If there is no resonance of propagation path impedance in EMI range, the relationship will

show a "zig-zag" behavior, several optimal points exist for smaller inductor values. However, if there are resonances of propagation path impedance in EMI range which determines the EMI filter design, there is no such a "zig-zag" behavior and some points need to be avoid that give a bigger inductor value. Moreover, this section also shows the weight design results for the experimental system, which show that the DM inductor weight is limited by inductor value and CM inductor weight is limited by the volt-second on the inductor. Moreover, with higher switching frequency, the gaps between the switching harmonics are larger which provides more freedom for choosing inductor values to make the resonant frequency of the EMI filter located at the frequency with small voltage excitations to avoid high volt-second.

2.7 Summary

This chapter presents a detailed analysis of the system level EMI modeling and filter design method for three phase power converters which provides the approaches to accurately estimate the filter weight before the implementation of the power stage and enable the optimal design of filter and power stage together.

A filter design oriented frequency domain system-level EMI modeling method is proposed for EMI noise prediction before system implementation, where the source and load impedance in the model can be calculated from the detailed switching model or measured directly from the system and the frequency domain noise sources can be calculated analytically using double Fourier integral transformation (DFIT) method.

With this model, the impact of propagation path impedance on system EMI noise emission is analyzed in detail. An improved filter design method using filter in circuit

attenuation rather than filter transfer function is proposed to improve the design accuracy and avoid overdesign.

Based on the proposed model, the interaction between AC and DC EMI filters is also analyzed in detail. With this consideration, an EMI filter design method using predicted in-circuit-attenuation (ICA) is proposed for designing both ac-side and dc-side EMI filters together. Then, a new filter structure is proposed which connects between AC and DC neutral points to attenuate ac-side and dc-side EMI noise at the same time.

Moreover, based on the EMI noise prediction model and filter design methods, the impact of the noise propagation path impedance and converter switching frequency on EMI filter weight/size is discussed in detail, which shows that the optimal switching frequency for minimum filter weight is highly related with the impedance of the system. A 1.5kW two level three phase voltage source inverter is developed as an example to verify the theoretical analysis and proposed modeling and design methods.

Chapter 3 Impact of Interleaving on Passive Component Weight Reduction

3.1 Introduction

In ac medium and high power applications, three-phase PWM VSCs are very popular because of their many advantages, such as low harmonics, high power factor, and high efficiency [88]. The parallel operation of VSCs has also become a popular choice in order to achieve ever increasing power ratings [92]. In addition, interleaving can further improve the benefits of paralleling VSCs. This PWM technique interleaves or phase-shifts the converter switching cycles, which is done by phase shifting the gate control signals of the converters. To represent such phase-shifted switching cycles, the interleaving angle α ($0 \le \alpha \le 2\pi$, or $0° \le \alpha \le 360°$) is defined in Figure 3-1. In the case of carrier-based PWM, this is done by the actual phase shifting of the carrier signals for each converter, or in the case of space vector modulation (SVM) by interleaving their switching cycle clock. As a result, interleaving has the main benefit the reduction of harmonic currents at the input and output terminals of the converters, i.e., at the dc capacitor and ac boost inductors.

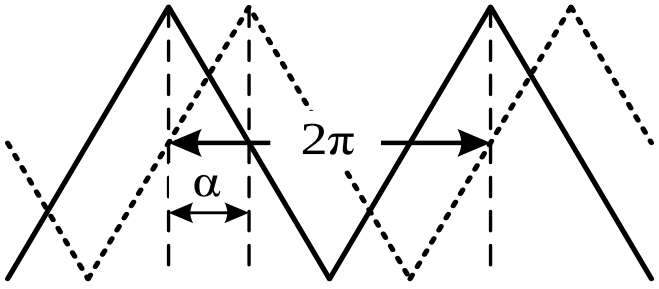


Figure 3-1. Definition of interleaving angle (α).

Furthering the past work, this chapter presents a detail analysis of the impact of interleaving on the passive components weight reduction for three phase power converters. the operation principle of interleaving topology, the design considerations and interleaving

angle selection method for minimum filter weight will be discussed in detail. To reduce the passive component weight of the system, the integration of interphase inductor is also studied in detail. As the principle study and preparation for the three phase power converters, section 3.2 will focus on the study of the impact of interleaving on input passive components weight reduction for dc-dc boost converters; section 3.3 will present the detail analysis of the impact of interleaving on filter weight reduction for three phase dc-ac power converters. In interleaving topologies, additional interphase inductor (or coupled inductors) are needed in order to limit the circulating current generated by interleaving which may reduce the benefit of interleaving and make the total passive component heavier, it is preferred to integrate the interphase inductor with other inductors together to reduce the total system weight. Section3.4 will present a detail analysis on the integration of interphase inductors for three phase dc-ac power converters. All of these analyses are verified with experimental results based on a demo system.

3.2 Impact of Interleaving on Input Passive Components of High Power Paralleled DC-DC Converters

3.2.1 Introduction

As the principle study and preparation for the three phase power converters, this section presents a detail analysis of the impact of interleaving on the input passive components weight reduction for dc-dc converters. A 2MW DC-DC boost converter for PV systems is taken as a design example. In high power PV farm applications, the centralized structure is always the choice where a high power DC/AC converter is needed to transfer the electric power to the grid. Two stage structure shown in Figure 3-2 is one common implementation of the high power DC/AC converter where the dc-dc boost

converter is used to achieve MPPT of the PV panel and the dc-ac converter is used to regulated DC link voltage and realize the grid connection.

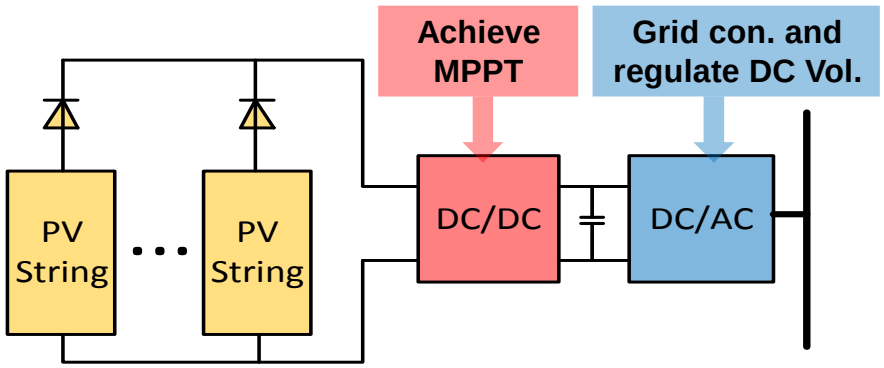


Figure 3-2 Typical PV converter configuration

In the dc-dc converter, a huge and expensive input filter is needed to meet the strict requirement of the PV panels. Due to the high power level, only silicon based devices (usually IGBTs and IGCTs) can be used and the switching frequency is relatively low (<1 kHz). Therefore a huge filter is needed between the PV strings and DC/DC converter to meet the strict requirements (such as 1% voltage ripple) for making PV panels work properly. Moreover, in high power application, due to the limitation of manufacturing capability and the cost consideration for the huge inductors, the core material type is also limited (for example, usually silicon steel is used instead of other advanced magnetic materials that are used in low power applications). All those limitations make the input filter extremely huge, a baseline filter design is done for a 2MW dc/dc converter with 1 kHz switching frequency and the results show that the inductors and capacitors are huge and especially the inductor is more than 2000kg, which takes a significant portion of system size and cost. In order to reduce the input inductor weight and cost, interleaving topology is studied in detail. A detailed ripple reduction analysis of interleaving topology and inductor design method is provided for the high power application. To reduce the circulating current, a coupled inductor is added to the circuit with interleaving topology.

The analysis model and design method for the coupled inductor is presented for dc-dc applications. The results show that adding coupled inductor can significantly reduce the size of the non-coupled inductor part. As for the additional coupled inductor, since the size is relatively small, advanced magnetic materials such as Amorphous can be used and the total input inductor size and loss can be reduced significantly. In order to get the minimum cost design point, asymmetric interleaving is also proposed to control the weight of coupled inductors and non-coupled inductors by changing the interleaving angle of the paralleled converters. All these ideas will be also used in three phase dc-ac system to minimize the total passive component weight. The analysis and design methods for dc-dc systems and three phase dc-ac systems are similar, however, since the operation conditions, design considerations and design optimization targets are different, the final design and optimization results are different which will be presented in the following sections.

3.2.2 Principle Analysis

A two phase interleaved DC/DC boost converter topology is shown in Figure 3-3, where the carrier of the second converter is phase shifted by 180 °. With the phase-shifting of the gate signals, the current ripple of each converter is also phase-shifted, and the total current ripple is reduced and the frequency is doubled due to the cancellation of the two converters.

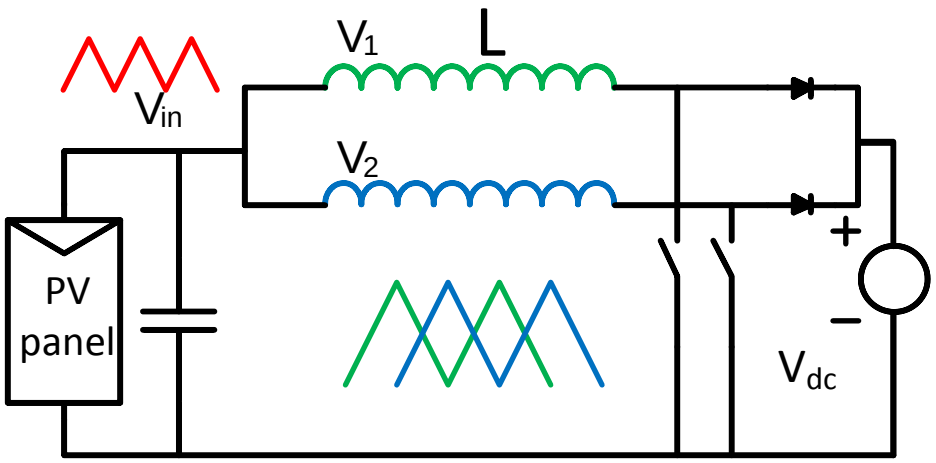


Figure 3-3 Two phase interleaved DC/DC PV converter

The total current ripple can be calculated as

$$\frac{\Delta I_{L\_all}}{\Delta I_L} = \frac{2D'-1}{D'} \tag{3-1}$$

If maintaining the total current ripple at the input side to be the same then the value of each inductor can be reduced as

$$Ratio = \frac{L_{interleaving}}{L_{nointerleaving}} = \frac{2D'-1}{D'} \tag{3-2}$$

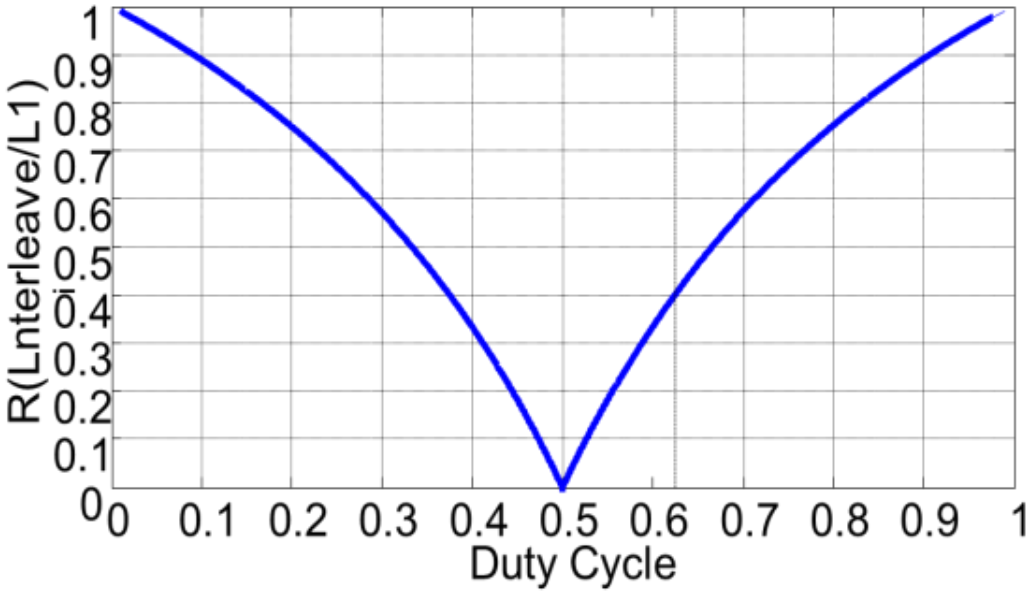
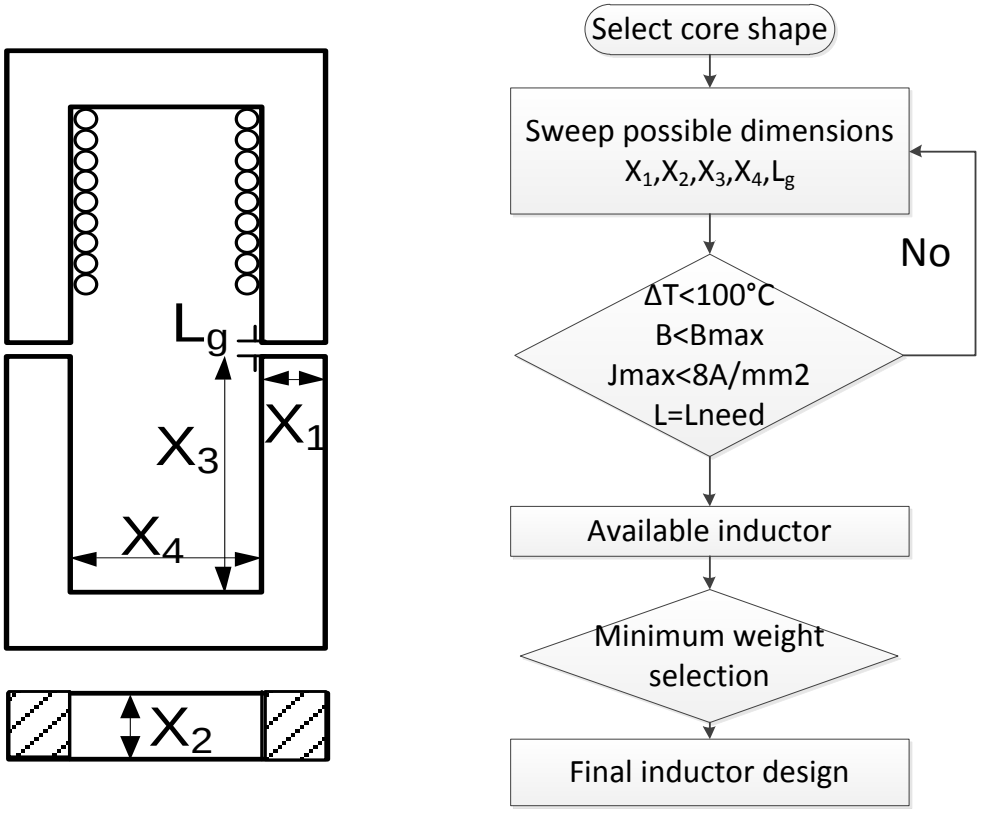


Figure 3-4 Current ripple reduction ratio of two phase interleaving topology

It is clear that the reduction ratio is related with the duty cycle of each converter, the relationship is shown in Figure 3-4. By using symmetric interleaving, if maintain the input current ripple, the inductor value needed for each inductor is reduced which provide the possibility to reduce inductor weight, while the current ripple through each inductor is increased.

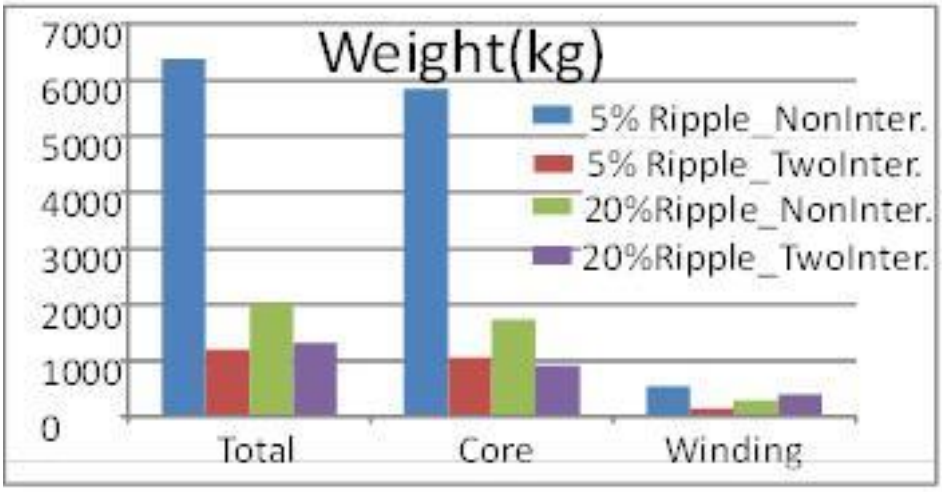
A minimum weight targeted inductor design method is shown in Figure 3-5, by sweeping all the possible dimensions of the core and designing inductors to meet the value, saturation and thermal limitation, a minimum inductor weight design result can be got. Due to the high power level, the filter design result is huge, which make the silicon steel the only valid core material for the inductor.



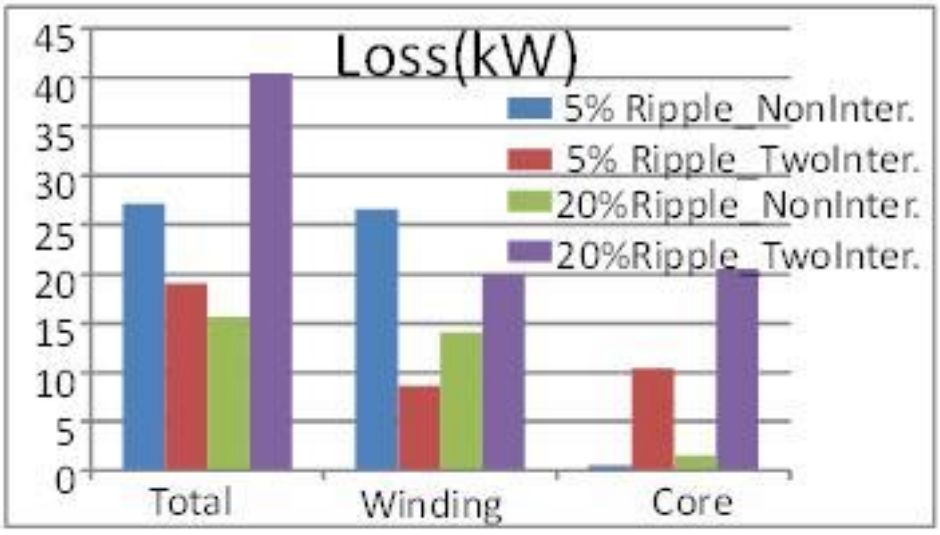
(a) Inductor Shape **(b) Inductor weight optimization**

Figure 3-5 Implementation method for energy storage inductors

The comparison (shown in Figure 3-6) is brought as an example to show the benefit of interleaving on inductor weight reduction when maintaining the total current ripple be 5% and 20% and using silicon steel materials. The result shows that if maintaining the same total current ripple, interleaving topology can help to reduce the inductor weight, however, it will increase the inductor loss (especially core loss) significantly.



(a) Weight comparison



(b) Loss comparison

Figure 3-6 Comparison of inductor design results for 2 MW PV converter (5% ripple requirement without interleaving: blue, 5% ripple requirement with two phase interleaving: red, 20% ripple requirement without interleaving: green,20% ripple requirement with two phase interleaving: purple)

If maintaining the total current ripple, interleaving can reduce the weight of passive component, while it will increase the current ripple through each inductor and the current through each active device is also changed. When current ripple is bigger, the turn-off loss will increase and the turn-on and reverse recovery loss will decrease and the conduction loss will also increase. An active component loss comparison result is shown in Figure 3-7. It is clear that by using interleaving, the total conduction loss will increase while the total switching loss is reduced and the total active component loss will increase which makes the system efficiency reduced.

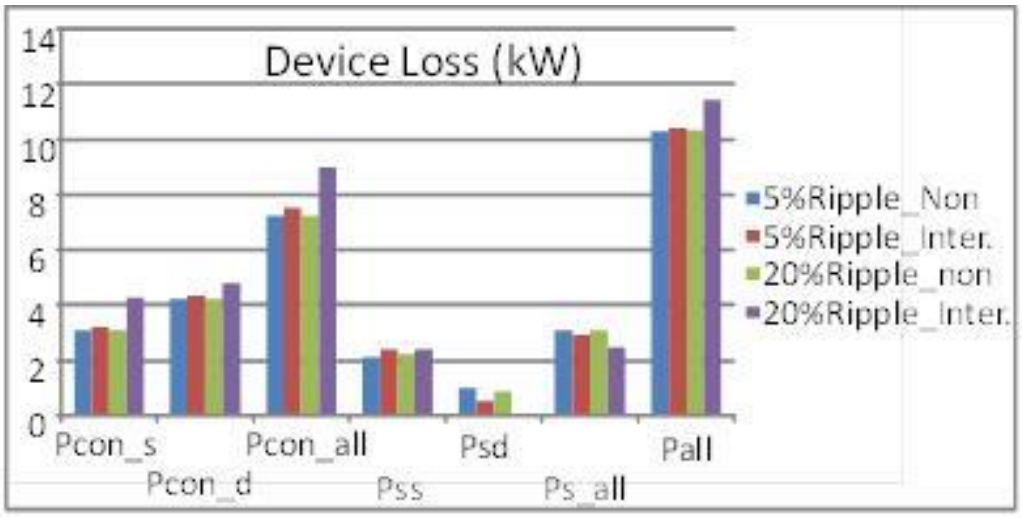


Figure 3-7 Semiconductor loss comparison
(switch conduction loss: Pcon_s, diode conduction loss: Pcon_d, total conduction loss: Pcon_all, switch switching loss: Pss, diode reverse recovery loss: Psd, total switching loss: Ps_all and total loss: Pall)

Moreover, when each inductor current ripple is bigger the current stress on IGBT, which is defined as $\text{C.S.} = \frac{I_{IGBT\_peak}}{I_{IGBT\_RMS}}$, will increase as shown in Figure 3-8. This will make the device safety margin smaller or even higher rating devices are needed.

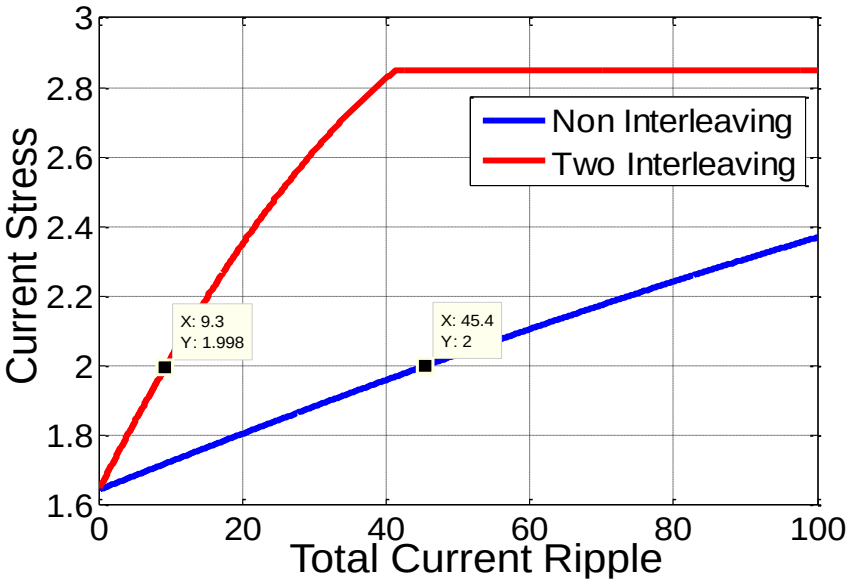


Figure 3-8 Current stress on IGBT comparison

For a real PV system, the input current ripple requirement is an inner system requirement and should not be used as the inductor selection criteria. In high power PV applications, high power level IGBT is usually used as the active component where the maximum peak current is always about twice of the RMS current due to the thermal limitation and latch up problems. When comparing the benefit of interleaving topology, the inductor value should be selected to maintain the same current stress through each IGBT, and the selection and the cost of IGBTs will not be increased. Due to the existence of circulating current that generated by interleaving topology, if maintaining the current stress on IGBT, each input inductor value is twice the value of non-interleaved topology. Figure 3-9 shows the weight and loss comparison of the input inductor in the two topologies. It is clear that if maintaining the current stress on IGBT, two phase interleaving will increase both the weight and loss of input inductor, while the input capacitor can be reduced since the total current ripple in input side will be reduced.

Figure 3-9 Inductor design comparison with IGBT current stress =2

3.2.3 Design of Coupling Inductors

To reduce the circulating current, instead of adding two independent input inductors, one additional reverse coupled inductor can be used. A two phase interleaving with reverse coupled inductor topology is shown in Figure 3-10. The inductors are separated as the non-coupled inductor L and ideal coupled inductor M. When the two converters is coupled together, the current through each inductor can be separated as output current I_{dm} and circulating current $I_{cir.}$ The simulation results (shown in Figure 3-11) show that adding ideal reverse coupled inductor will only reduce the circulating current and IGBT current stress while the output current remains the same.

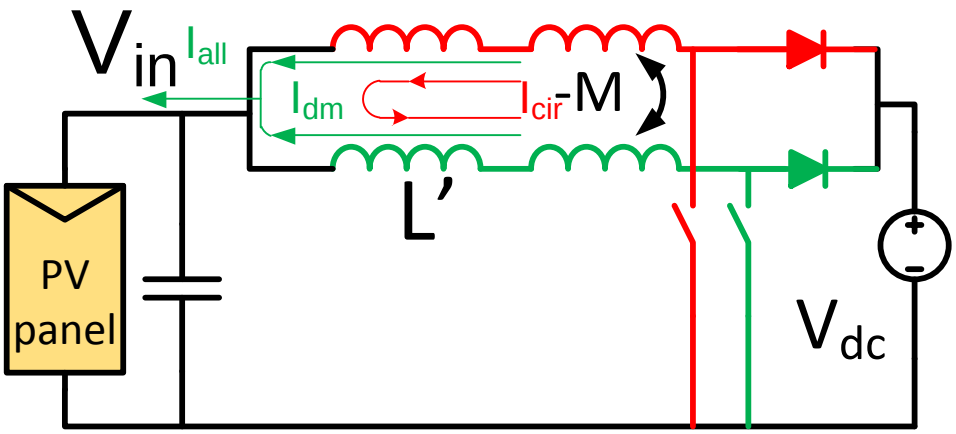


Figure 3-10 Two phase interleaving with ideal reverse coupled inductor

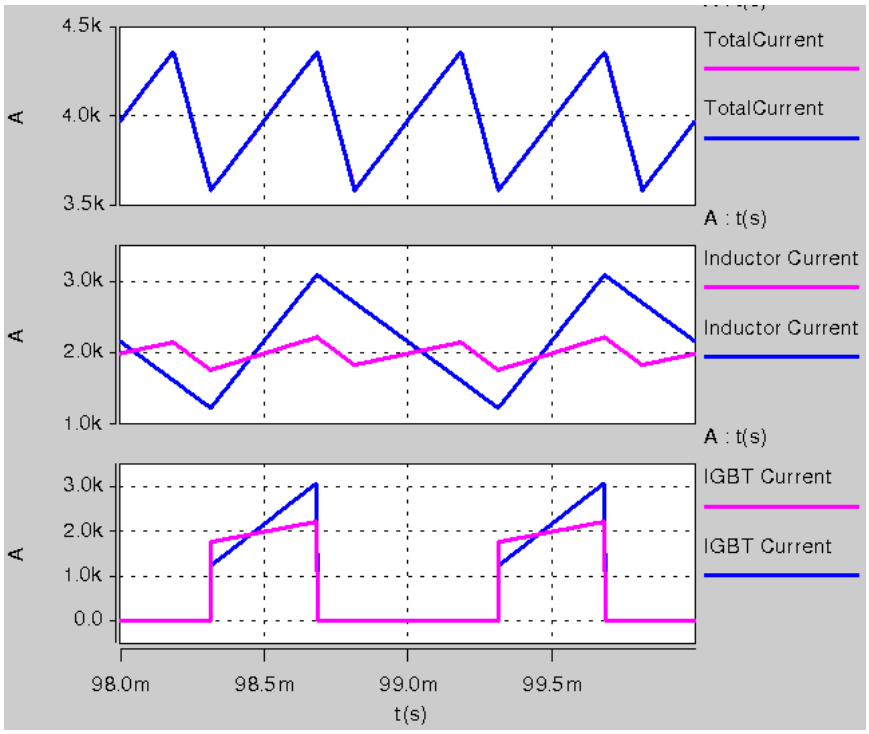


Figure 3-11 Simulation results with coupling inductors

(without coupled inductor: blue and adding 1mH coupled inductor: pink)

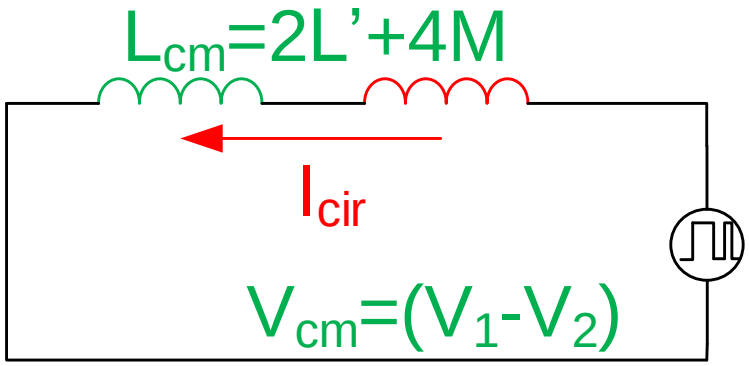


Figure 3-12 Equivalent circuit for circulating current

The equivalent circuit for circulating current is shown in Figure 3-12, which shows that circulating current is determined by the voltage different between two phases and the interphase inductance added to the circuit. when interphase inductor value is big enough, the circulating current can be well attenuated, thus the current stress on IGBT will be reduced. Figure 3-13 shows the reduction of IGBT current stress when different coupled inductor is added.

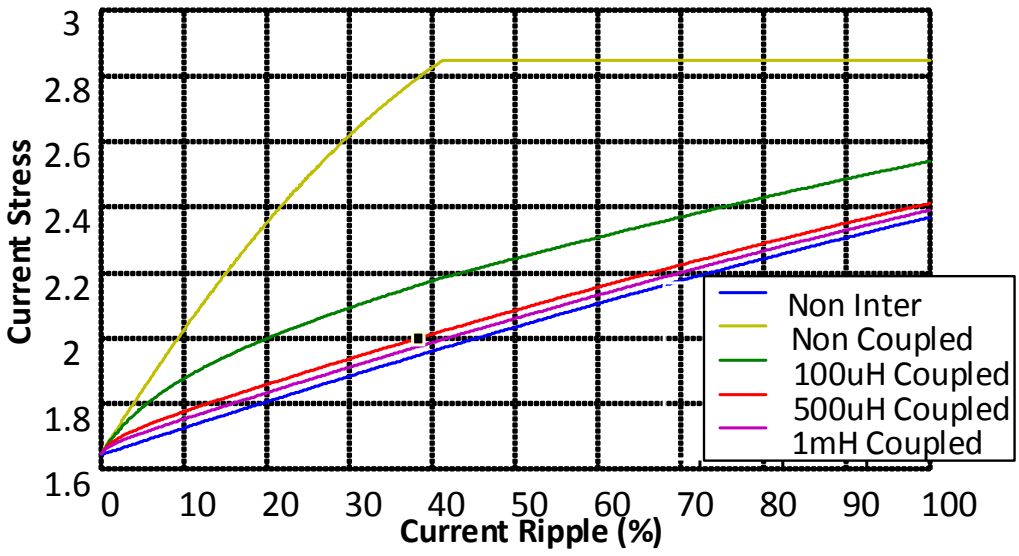
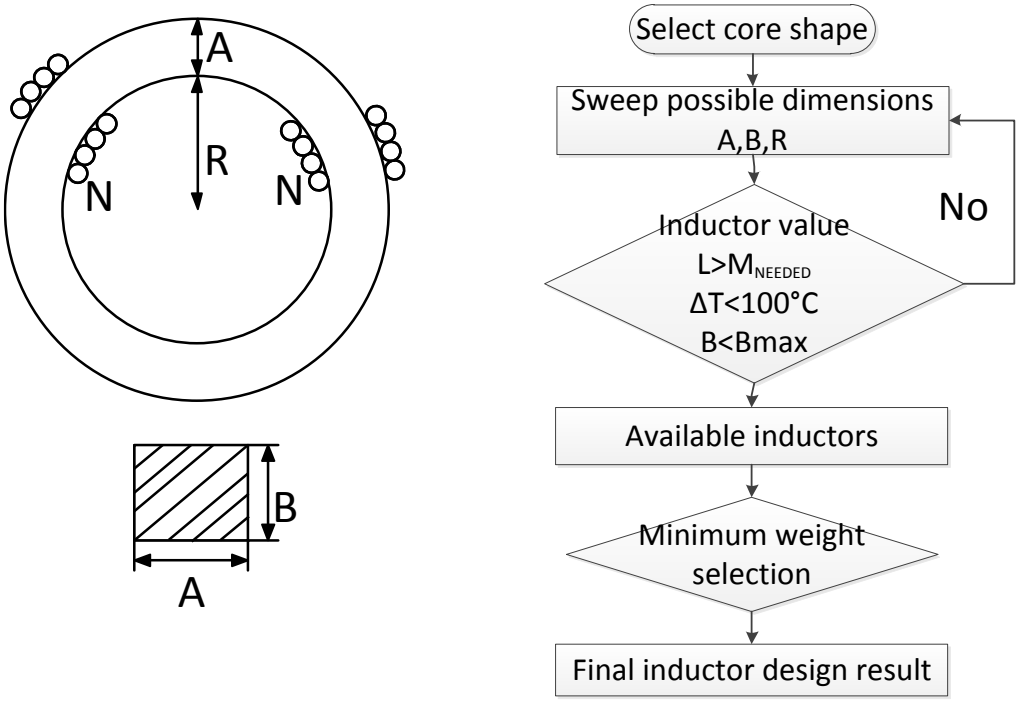


Figure 3-13 IGBT current stress comparison

Moreover, the equivalent circuit also shows that the volt-sec on the coupled inductor is determined by the voltage difference of the two converters, which make it possible to

implement the coupled inductor using a choke without air gap to get a big inductance value. Figure 3-14 shows the coupled inductor minimum weight design method.



(a) Interphase inductor core shape **(b) minimum weight design**

Figure 3-14 Coupled inductor design method

Since the design result of the coupled inductor is relatively small, it is also possible to use amorphous material to reduce the core loss which makes the coupled inductor even smaller. When the current ripple of each inductor is smaller, the non-coupled inductor size can be reduced significantly. Figure 3-15 shows the normalized inductor design comparison result which indicates that when maintaining the IGBT current stress, by adding coupled inductor, both weight and loss of the inductor can be reduced significantly.

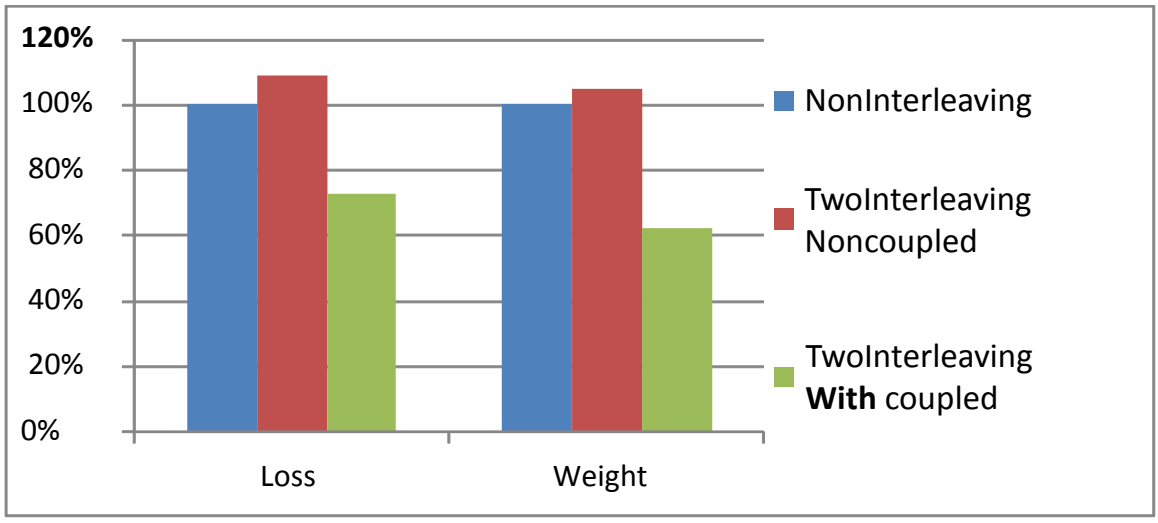


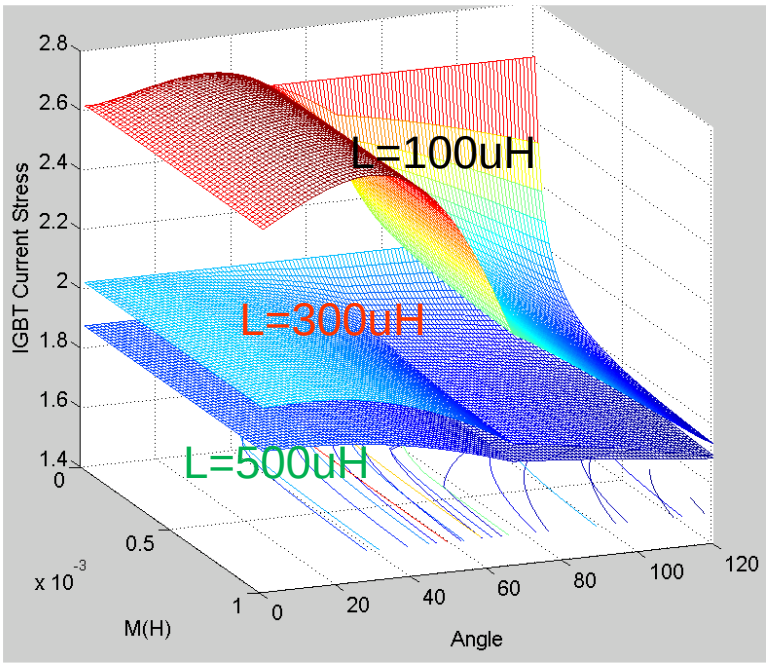
Figure 3-15 Inductor design comparison (normalized value)

3.2.4 Asymmetric Interleaving

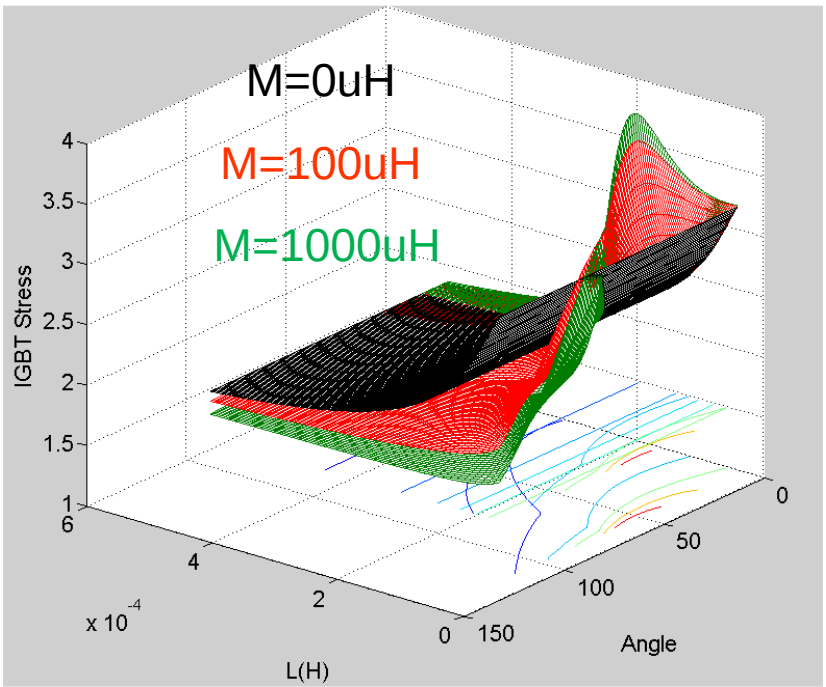
Interleaving topology with coupled inductors can reduce the weight and loss of the input inductor, however, the cost of using amorphous material is much higher than the silicon steel material, so when the inductor weight is the smallest, the cost may not be the optimal point. In the implementation of the coupled inductor, it is shown that the coupled inductor size is determined by volt-sec on itself which is directly related with the interleaving angle we select. Using smaller interleaving angle can help to reduce the coupled inductor weight which can reduce the cost of amorphous material. However it will increase the non-coupled inductor value needed for maintaining the IGBT current stress, which means that it will increase the cost of silicon steel material.

Since coupled inductor do not change the total current ripple, the total current ripple is determined by the converter duty cycle (D), non-coupled inductor value (L) and interleaving angle(α) $\Delta I_{all} = f_1(D, L, \alpha)$, and for IGBT current stress, the IGBT current stress is determined by the converter duty cycle, non-coupled inductor value, interleaving

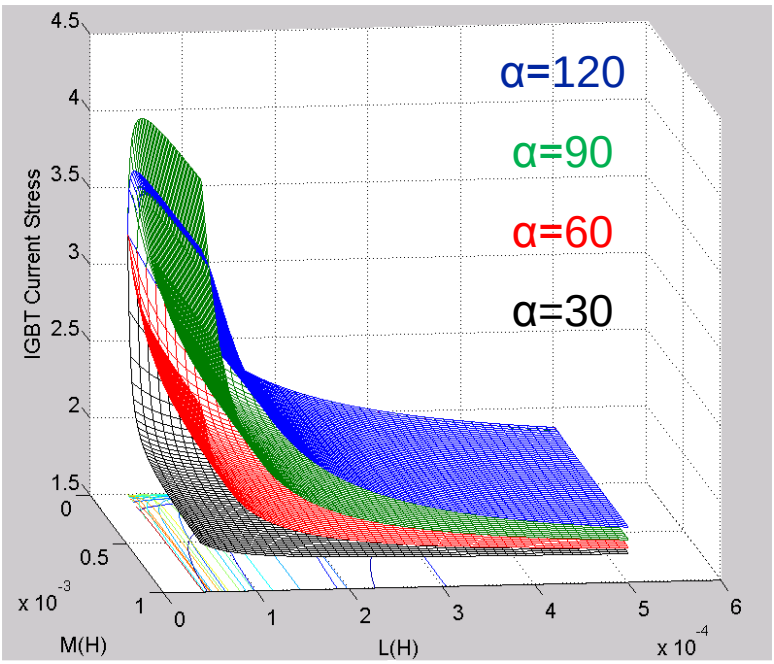
angle and also the coupled inductor value (M): $\frac{I_{peak\_IGBT}}{I_{RMS\_IGBT}} = f_2(D, L, \alpha, M)$, the 3-D sweeping results shown in Figure 3-16 show the impact of different variables on IGBT current stress.



(a) Fixed non-coupled inductor value (L)



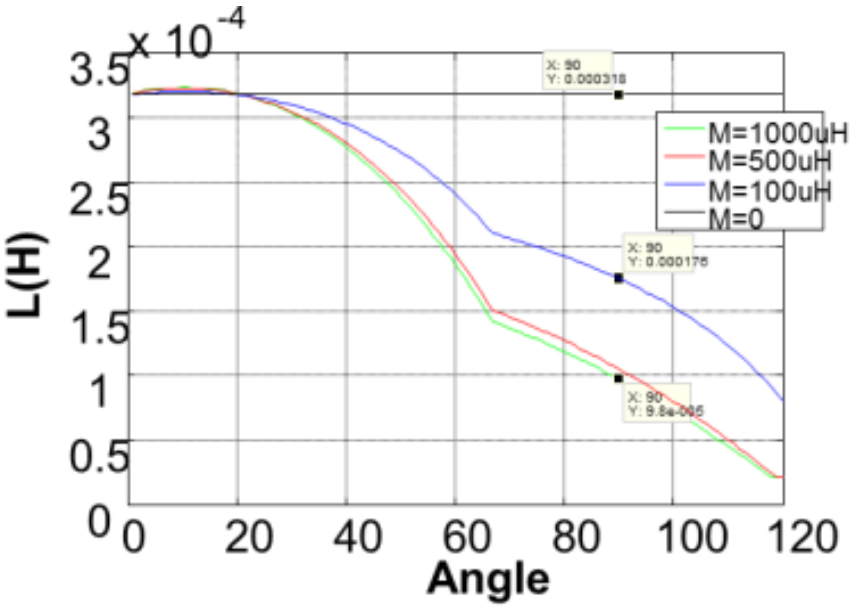
(b) Fixed coupled inductor value (M)



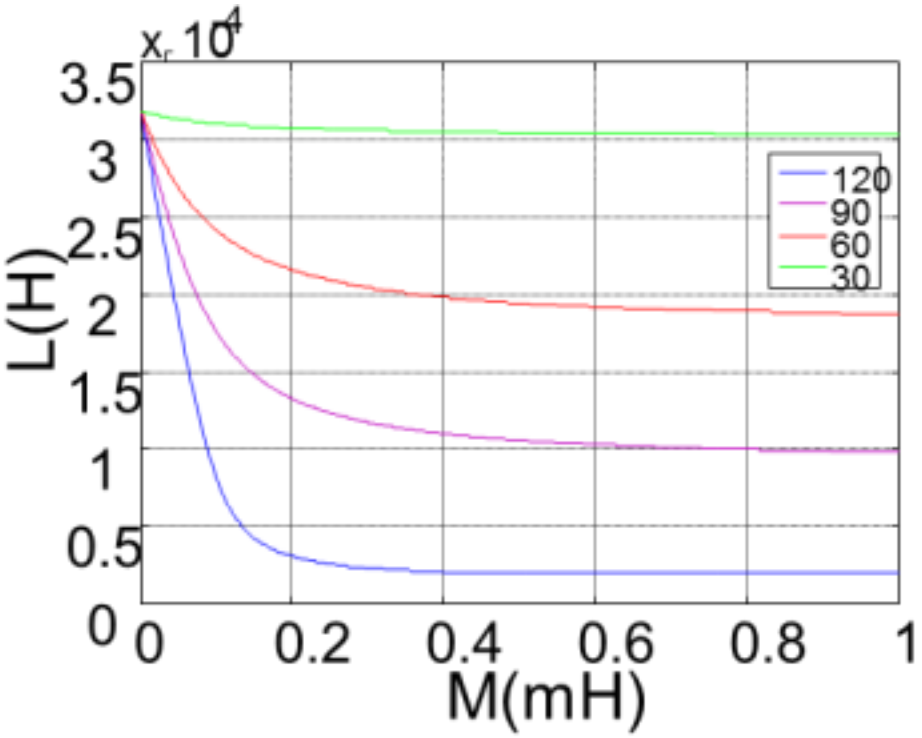
(c) Fixed interleaving angle

Figure 3-16 Impact of asymmetric interleaving with coupled inductor on IGBT current stress

When the design requirement is maintaining the IGBT current stress, the selection of interleaving angle, non-coupled inductor (L) and coupled inductor value (M) is shown in Figure 3-17, the result shows that, with a fixed interleaving angle, increasing coupled inductor value can reduce the non-coupled inductor value, however, if M is big enough (>1mH), the benefit of further increasing M will be limited. Moreover, with a fixed M value, smaller interleaving angle need a bigger non-coupled inductor value to maintain the IGBT current stress.



(a) Interleaving angle vs. L (with different coupled inductor value: 1mH: green, 500uH: red, 100uH: blue, 0uH: black)



(b) M vs L (with different interleaving angle: 120°: blue, 0°: purple, 60°: red, 30°: green)

Figure 3-17 Parameter selection when IGBT current stress=2

3.2.5 Weight Design Summary and Discussion

Figure 3-18 shows the inductor weight design result with different interleaving with the coupled inductor value equal to 1mH. It is clear that by using small interleaving angle, the coupled inductor (Amorphous) weight will be reduced while the non-coupled inductor (Silicon Steel) weight will increase.

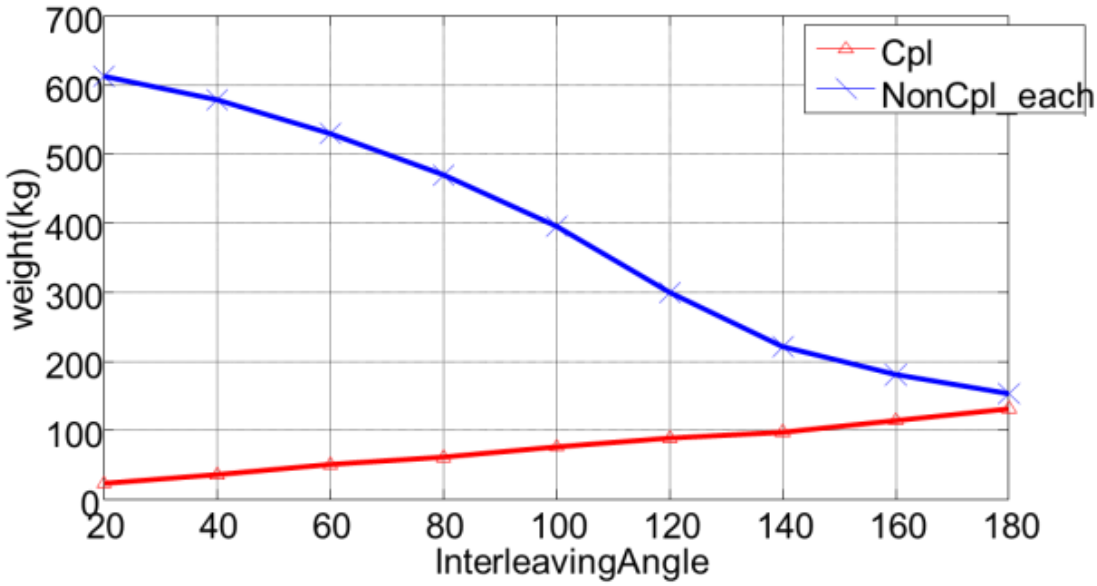


Figure 3-18 Inductor design results for asymmetric interleaving

(Coupled inductor: red, non-coupled inductor: blue)

If the design target is the minimum cost for the passive components, one can collect the ratio between the price of coupled inductor (Amorphous) and the price of non-coupled inductor (Silicon Steel), and then the total cost will change according to the interleaving angle selected in the design, thus, the optimal interleaving angle is selected according to the minimum cost for the input inductors..

This section presents a detail analysis on the impact of interleaving on input passive components of paralleled dc/dc converter for high power PV applications. The design result shows that if maintaining active component current stress, both the weight and the loss of input inductor will increase. To reduce the circulating current, a coupled inductor is added

to the circuit which can reduce the current ripple through the non-coupled inductor and reduce the size significantly. Moreover, amorphous material can be used to implement the coupled inductor which makes the coupled inductor small , thus, the overall size and loss can be reduced significantly. Asymmetric interleaving is also proposed to balance the cost of silicon steel and amorphous material to get the optimal design point for minimum system passive component cost. The analysis and design methods for dc-dc converters and three phase dc-ac converters are similar, however, since the operation conditions, design considerations and design optimization targets are different, the final design and optimization results are different which will be presented in the following sections.

3.3 Impact of Interleaving on Filter Weight Reduction for Three Phase Power Converters

Interleaving has the main benefit the reduction of harmonic currents at the input and output terminals of the converters, for example, at the dc capacitor and ac boost inductors. Furthering the past work, this section presents a complete analysis of the impact of interleaving on system filter weight reduction for three phase power converters. A dc-fed motor drive system with paralleled three-phase voltage-source converters as shown in Figure 3-19 is taken as an example. The system contains two VSIs working in an interleaved mode to reduce system noise, and three interphase inductors ($L_{inter1\sim3}$) are added to reduce the circulating current that is generated by the output voltage differences.

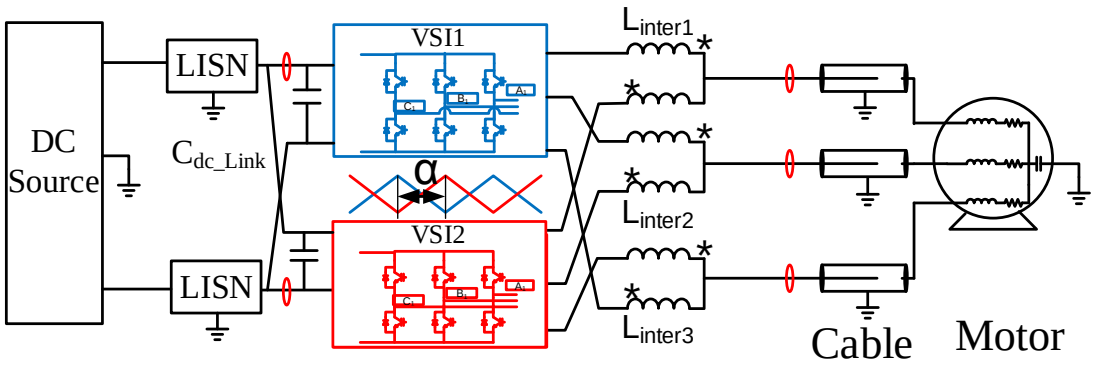
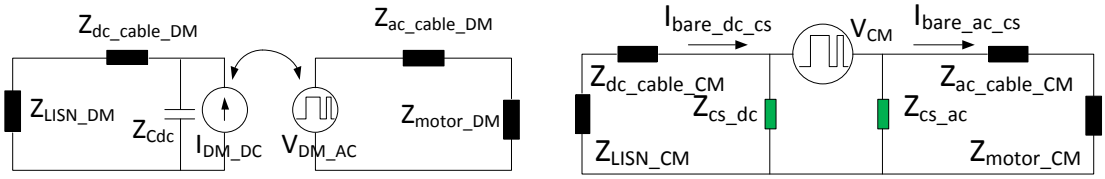


Figure 3-19 Interleaved two level VSI DC-fed motor drive system.

A systematic design method for selecting the interleaving angle to reduce the EMI noise in the system is proposed. First the equivalent circuits for EMI noise analysis for this interleaved dc-fed motor drive system is provided and double Fourier integral analysis is used to analyze the impact of interleaving on system EMI noise sources. The detailed analysis about the interleaving angle selection for EMI noise reduction with the consideration of system EMI noise propagation path impedance is presented in section 3.3.2. Considering the real implementation of the filters, section 3.3.3 presents the analysis of the passive component weight reduction for interleaved three phase converters. All the analysis is verified through both simulations and experiments. Since the CM filters takes a big portion of the total passive component weight in dc-fed motor drive system with long connecting cables, the analysis is focused on CM noise reduction and CM filter weight minimization, however, all the design procedures and methods can also be applied for DM noise analysis.

3.3.1 Principle of Interleaving for Three Phase Power Converters

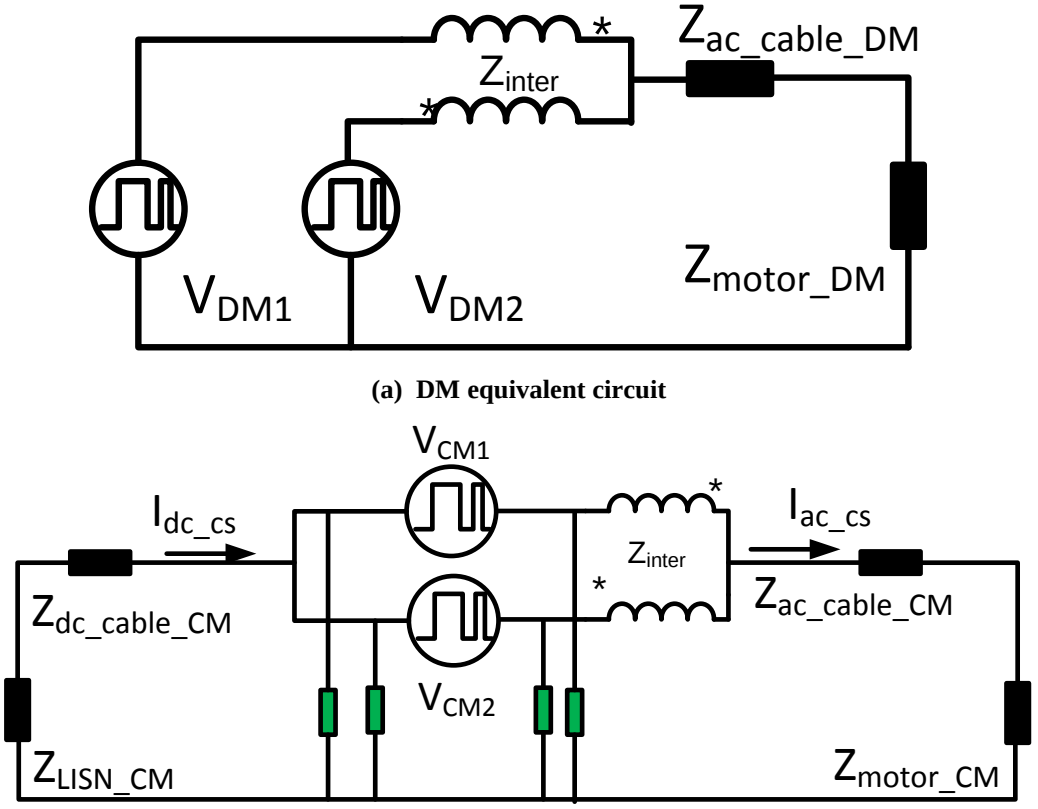
From the system level EMI modelling method shown in section 2.2, it is noticed that, in a motor drive system, due to the existence of impedance of both DC and AC sides, they will interact and influence the noises on both sides. However, there usually is a big value of DC link capacitor (C_{DC}) to meet the harmonic requirement for a typical VSI system. Due to the low impedance of the DC link capacitor, the AC and DC side DM noise is decoupled at relative low frequency (several MHz) and the equivalent circuit for DM noise analysis is shown in Figure 3-20(a). Since there is no such low impedance path for CM noise, the AC and DC side CM noises are coupled as shown in Fig.1, then the CM equivalent circuit should include both AC and DC side impedance as shown in Figure 3-20(b). In the circuit, V_{DM_AC} and V_{CM} represent the equivalent noise sources in frequency domain and all the impedances can be got from the detail switching model or directly measured from the system.



(a) DM equivalent circuit **(b) CM equivalent circuit**

Figure 3-20 EMI noise equivalent circuits without interleaving.

For the interleaved two-level VSI DC-fed motor drive system shown as Figure 3-19, the CM and DM equivalent circuits are shown as Figure 3-21. Since the carrier of VSI 2 is phase shifted with VSI 1, the noise sources of the two converters are also different. The interphase inductor is also included in the equivalent circuit which is used to limit the circulating current that is generated by the voltage difference between the two noise sources.

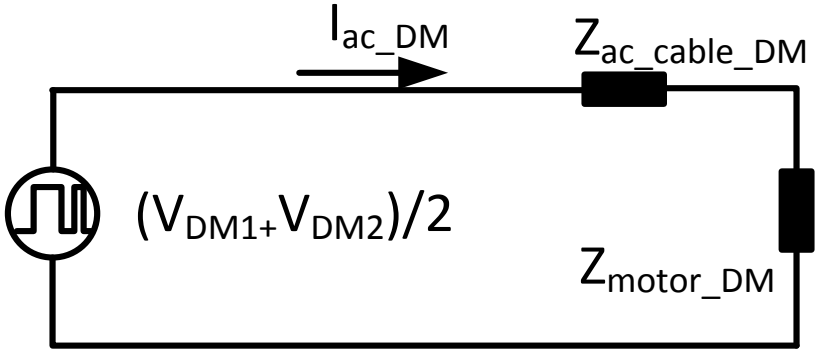


(a) DM equivalent circuit

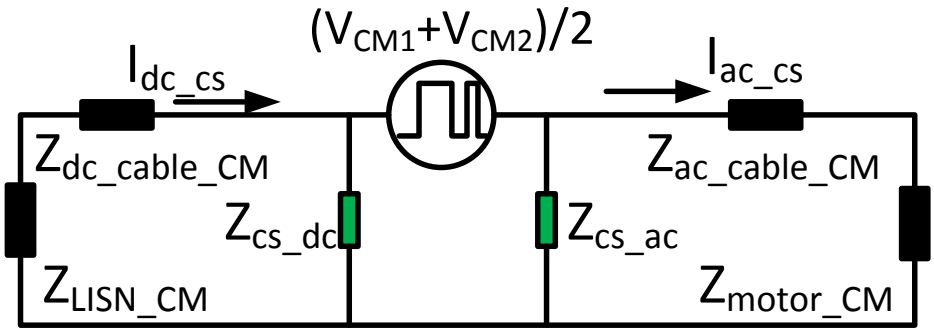
(b) CM equivalent circuit

Figure 3-21 DM and CM noise equivalent circuit of dc-fed system with interleaving

However, the EMI standard only limited the EMI noise at the output of the interleaved converter and the circulating current is only inside the interleaved converter and have no impact on the output noise, thus the equivalent circuit can be simplified as shown in Figure 3-22 if only the output noise of the converter is analyzed.



(a) DM equivalent circuit



(b) CM equivalent circuit

Figure 3-22 Equivalent circuits for converter output noise with interleaving

The equivalent circuits show that the interleaving will only change the noise source in the system and the impact of interleaving on the noise source can be calculated analytically using the double Fourier integral transformation (DFIT) method. As shown in section 2.2, the noise source of each converter in the equivalent circuit can be analytically calculated with some reasonable simplification when the system operation condition is known. The switched phase-leg output voltage between ac terminal (e.g. point A_1) and dc link mid-point (N), v_{A1N}, can be decomposed into different harmonics. The frequencies of harmonic voltage components can be expressed as $(m\omega_c + n\omega_0)$, where ω_c is the angular frequency of the carrier wave, ω_0 is the fundamental line frequency, and m and n are the carrier and baseband integer index respectively. Based on the double Fourier integral analysis approach, the harmonic component for voltage v_{A1N} corresponding to frequency $(m\omega_c + n\omega_0)$ can be expressed as in (2-13). Moreover, the magnitude and phase information of each harmonic can be obtained as in (2-14) from the double Fourier integral analysis. Note that C_{mn} is only a function of PWM scheme and modulation index M.

For the group 2 converter VSC2, without interleaving (i.e., with identical carrier wave as group 1 converter), v_{A2N} will be identical to v_{A1N}. In general, for the example system in Fig. 2, the harmonic currents in i_A are determined by the summation of harmonic currents

in i_{A1} and i_{A2}, which are in turn determined by the harmonic voltages in v_{A1N} and v_{A2N} respectively, assuming the inductances L_1 and L_2 are balanced and equal, the harmonic current in i_A corresponding to frequency $(m\omega_c+ n\omega_0)$ will be determined by the average value of v_{A1N} (m,n) and v_{A2N} (m,n), or $v_{AN\text{-}avg}$ (m,n). Without interleaving, the amplitude of $v_{AN\text{-}avg}$ (m,n) remains the same as C_{mn}, i.e.

$$C_{mn\_ave} = 0.5(C_{mn1} + C_{mn2}) = C_{mn} \tag{3-3}$$

Interleaving phase shifts the carrier waves between VSC1 and VSC2. As a result, for the harmonic components at frequency $(m\omega_c+ n\omega_0)$ in v_{A1N} and v_{A2N}, their amplitudes will remain the same, but the angle will be different. Specifically, an angle shift of α by the VSC2 carrier will result in $\Delta\theta_c= m\alpha$ angle shift for θ_c of v_{A2N} (m,n). Consequently, the amplitude of $v_{AN\text{-}avg}$ (m,n) with interleaving angle κ will become

$$C'_{mn\_ave} = 0.5\left|\left(C_{mn1} + C_{mn2}e^{jm\alpha}\right)\right| = C_{mn}\cos(m\alpha/2) \tag{3-4}$$

The sweeping result of the voltage noise source magnitude reduction ratio on different order harmonics of interleaving with different interleaving angle is shown in Figure 3-23 and a 2D drawing of the magnitude reduction ratio on different order harmonics is shown in Figure 3-24.

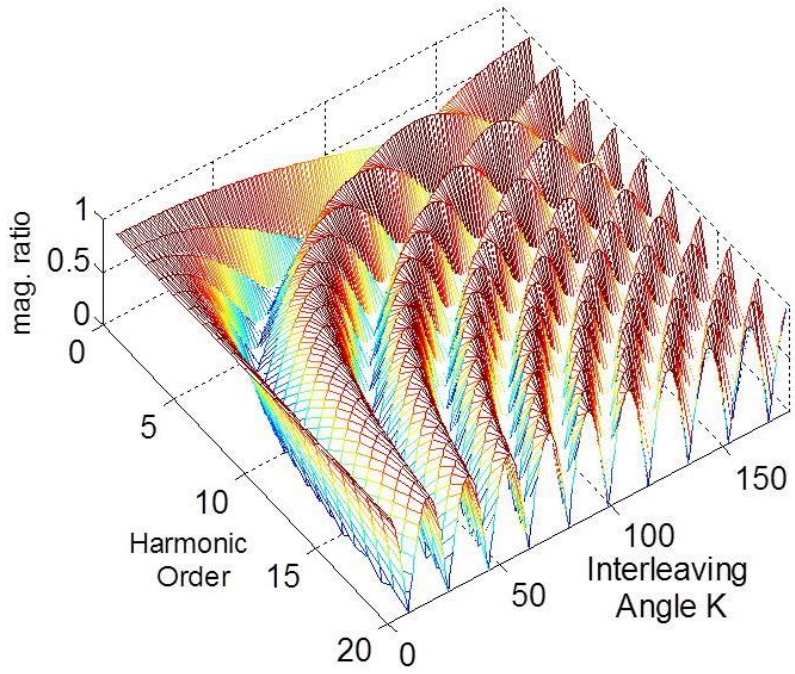


Figure 3-23 Voltage noise source magnitude reduction ratio on different order harmonics with different interleaving angle

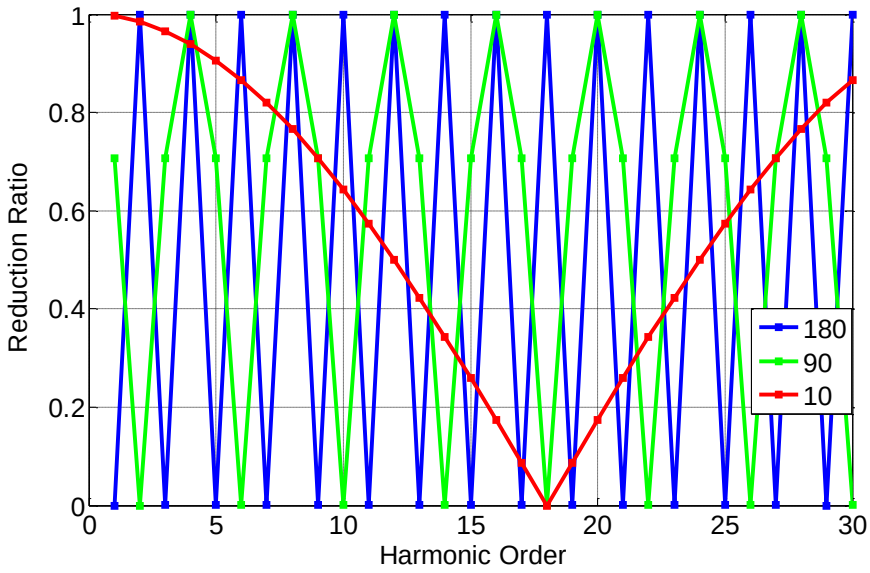


Figure 3-24 Voltage magnitude reduction ratio on different order harmonics of interleaving (180°: blue; 90°: green; 10°: red)

The results show that if α is set to be π/m, i.e., interleaving the carrier wave of VSC2 by 1/m switching cycle and keeping the carrier wave of VSC1 unchanged, C'_{mn_avg} will be zero. Especially, for the sample system shown in Fig. 2, phase-shifting π can eliminate all odd order switching frequency harmonics and not affect the even order switching

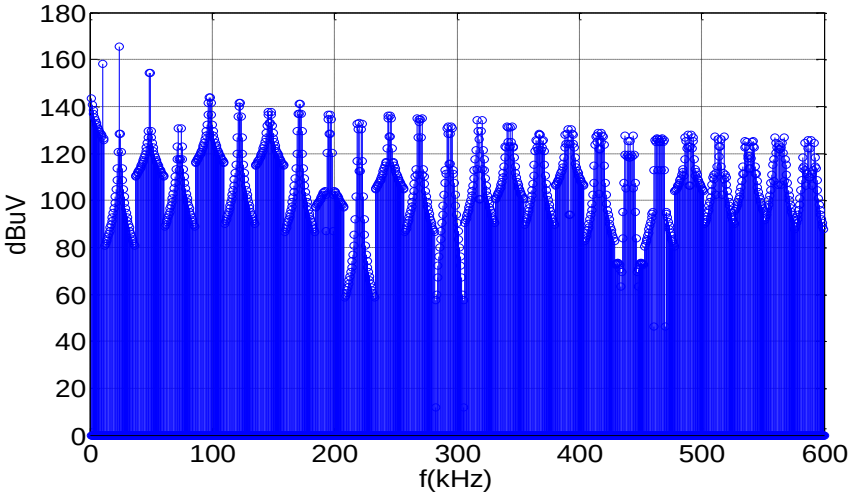
frequency harmonics. And phase-shifting π/2 will eliminate harmonics when m is (4k+2), such as 2, 6 and 10, reduce the harmonics by 30% (i.e. $1/\sqrt{2}$ of the original) when m is odd, and not affect other even order harmonics. Moreover, interleaving can reduce the amplitude of harmonic currents at the output port, because part of the harmonic currents in each converter is changed into circulating current not flowing into the ac source. Such circulating current can be determined by the difference of DM harmonic voltage in v_{A1N} and v_{A2N} as in (3-5) and the impedance in the circulating current loop.

$$C'_{mn\_diff} = C_{mn}\sin(m\kappa/2) \tag{3-5}$$

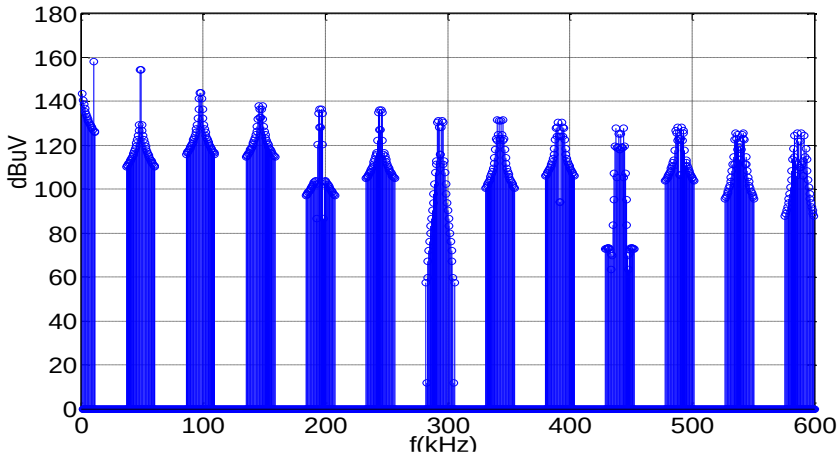
In order to limit the circulating current, additional interphase inductors are necessary for motor drive system, which adds additional weight to the system. It is clear from (3-5) that with a smaller interleaving angle, the voltage difference of the two converters is smaller so the volt-sec on the interphase inductor is also smaller, thus the size of the interphase inductor can be reduced. The detailed design and trade-off of interphase inductors will be presented in section 3.4.

3.3.2 Impact of Interleaving on EMI Noise Reduction

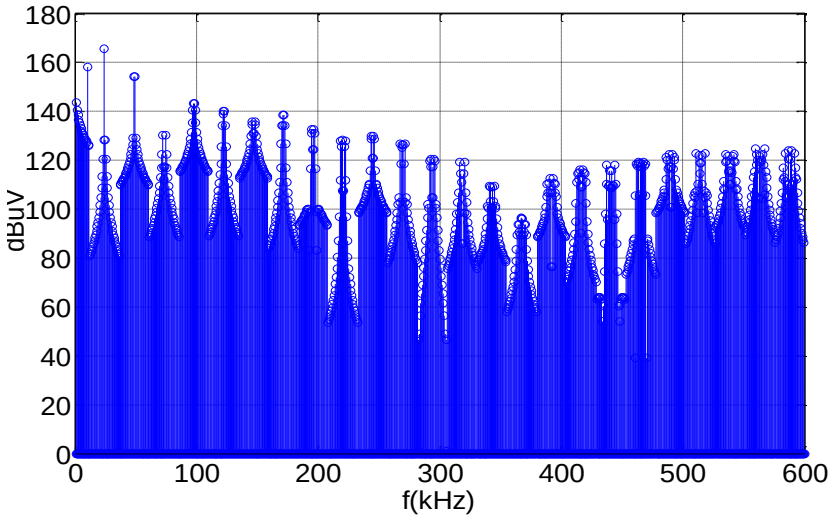
In interleaving topology, different switching frequency harmonics of the total noise source can be attenuated with different interleaving angles. With DFIT method, when system modulation scheme and modulation index is fixed, the impact of different interleaving angles on noise source reduction can be calculated analytically. Figure 3-25 shows the calculated CM noise voltage source with different interleaving angles. It is clear that bigger interleaving angle can eliminate certain order of harmonics while small angle interleaving can attenuate the noise source in a wide range.



(a) non-interleaving



(b) 180 °interleaving



(c) 12 °interleaving

Figure 3-25 CM noise source calculation results

From the system-level EMI model of the system, it is clear that the current EMI noise spectrum is determine by both the noise source and noise propagation path impedance. Changing interleaving angle can change the noise source while the noise propagation path impedance remains the same. Figure 3-26 shows the EMI propagation path impedances of the studied motor drive system. Due to resonance between the cable inductance and motor grounding capacitance, the CM propagation impedance has an anti-resonance at around 370 kHz, which considering the converter switching frequency is 24.5kHz (to avoid 150kHz harmonic) will create a resonance on the CM current noise spectrum at 367.5kHz.

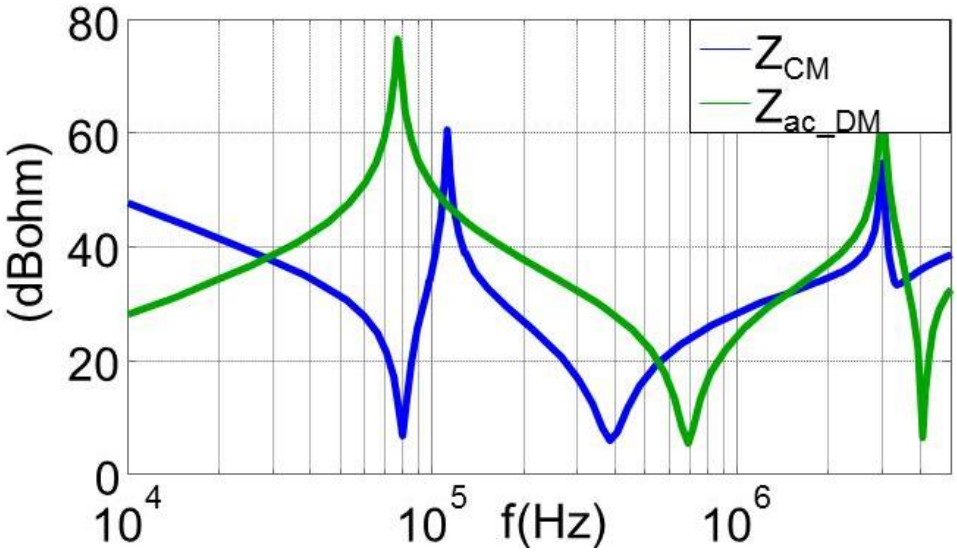


Figure 3-26 EMI propagation path impedances

(DM: green & CM: blue)

If following the practical EMI filter design procedure shown in section 2.3, the EMI filter corner frequency will be determined by this resonant peak. If 180 °interleaving is used then the resonant peak at 367.5kHz (15th order switching frequency harmonic) will be eliminated (as shown in Figure 3-25(b)) however the harmonics at 392kHz (16th order switching frequency harmonic)will remain the same and determine the EMI filter design, which make the benefit on filter size reduction limited. Instead of using 180 °interleaving,

a small interleaving angle can be used to attenuate all the harmonics near the resonant frequency and create anti-resonance at the same frequency range, thus it can reduce the current noise near the whole resonant frequency range and help to increase the corner frequency of EMI filter significantly. Figure 3-25(c) shows the calculated voltage harmonics result with a 12 °interleaving angle. It is clear that using this small interleaving angle can attenuate all the harmonics near 370 kHz. Based on the calculated voltage spectrum and system impedance, the current noise spectrum can be calculated. Following the practical EMI filter design procedure, a sweeping result of different interleaving angle for EMI filter corner frequency is shown in Figure 3-27, which shows that 12.6 °and 35.8 ° are some optimized interleaving angle for a smaller EMI filter size.

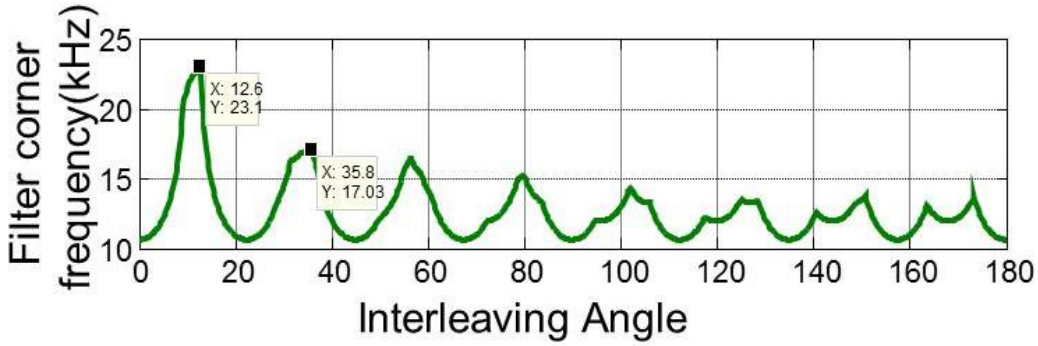


Figure 3-27 Interleaving angle sweeping result for ACCM EMI filter corner frequency

These angles can also be calculated analytically using DFIT method. It is clear that if α is set to be π/m, C'mn_avg will be zero, in other word mth order switching frequency harmonics will be eliminated, thus considering the system impedance resonant frequency f_{res} (or mth order harmonic $m=f_{res}/f_s$), to reduce the voltage harmonics at this frequency, the interleaving angle should be calculated as shown in (6)

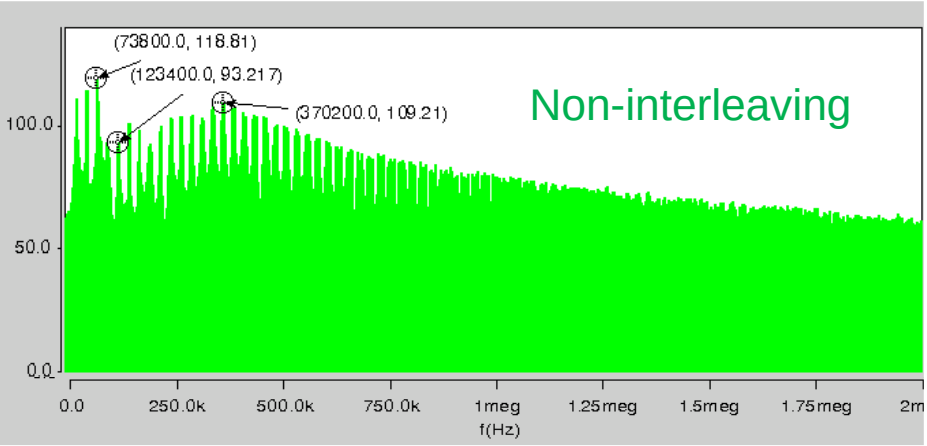
$$\kappa = \pi \frac{f_s}{f_{res}} \tag{3-6}$$

Notice the any odd number times this interleaving angle can also cancel the voltage harmonics at f_{res}, thus the final optimal interleaving angle should be calculated as (3-7)

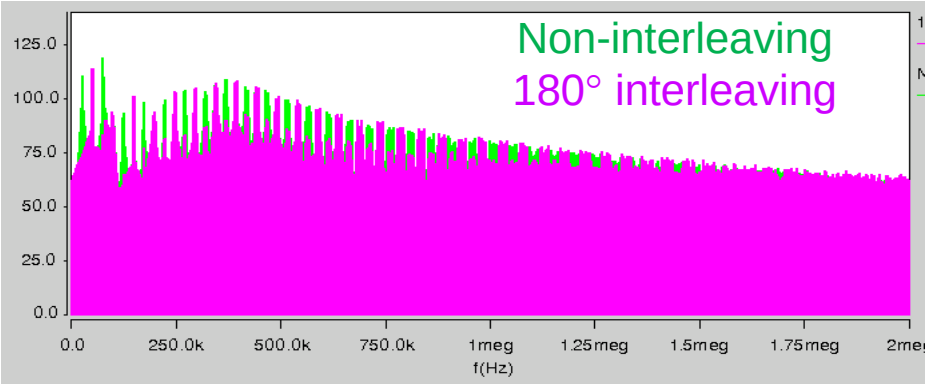
$$\kappa = (2N+1)\pi \frac{f_s}{f_{res}} \tag{3-7}$$

To get the attenuation at a wider range around the resonant frequency, smaller interleaving angle is preferred.

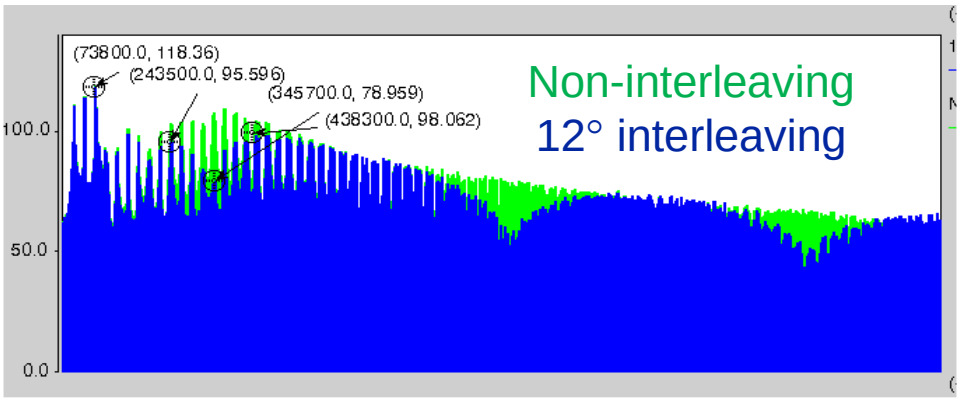
To verify the analysis above, a DC fed motor drive system with long cables shown as Figure 3-19 is studied. The time domain switching model simulation is carried out in SABER and the simulated current spectrum comparison result is shown in Figure 3-28.



(a) Simulated AC CM noise without interleaving (green)



(b) Simulated AC CM noise (without interleaving: green; with 180 °interleaving: maroon)



(c) Simulated AC CM noise (without interleaving: green; with 12 °interleaving: blue)

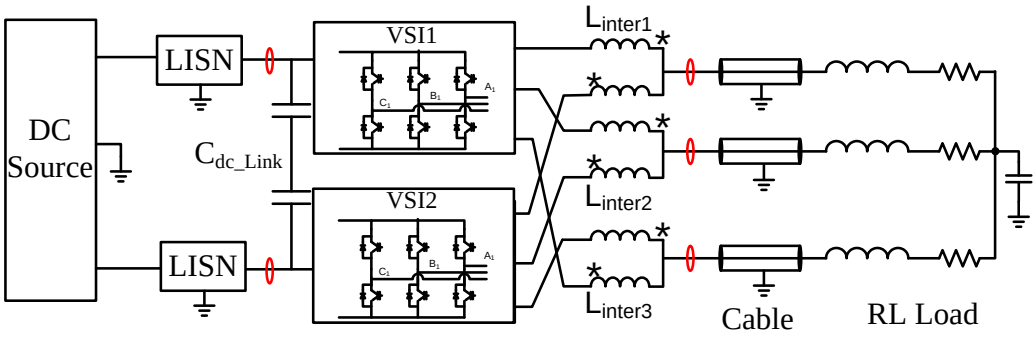
Figure 3-28 ACCM current EMI noise spectrum simulation results

The simulated system output power is 100kW with 540V dc link voltage, line frequency is 100Hz, and switching frequency is selected to be 24.5 kHz. Due to the resonance between the cable inductance and motor grounding capacitance, the CM propagation impedance has an anti–resonance at around 370 kHz, which will create a resonance on the CM current noise spectrum at the same frequency. The simulated results show that due to the anti–resonance of CM propagation path, the CM current noise spectrum has a resonance at the same frequency which will determine the EMI filter design. With 180 °interleaving odd-order switching frequency harmonics will be canceled which has a significant benefit on the harmonic filter design since it will eliminate the first switching frequency harmonics and make the equivalent switching frequency doubled. However for the EMI filter design, since the standard start from 150 kHz (based on DO160), if following the design procedure shown in Fig. 9, the critical point for designing the filter is only pushed to 393 kHz (which is an even-order harmonics and remains the same with 180 °interleaving) with similar attenuation needed and the increase of EMI filter corner frequency is limited. However, with 12 °interleaving, the voltage harmonic at 370 kHz is attenuated and the harmonics around this frequency are also attenuated, which make

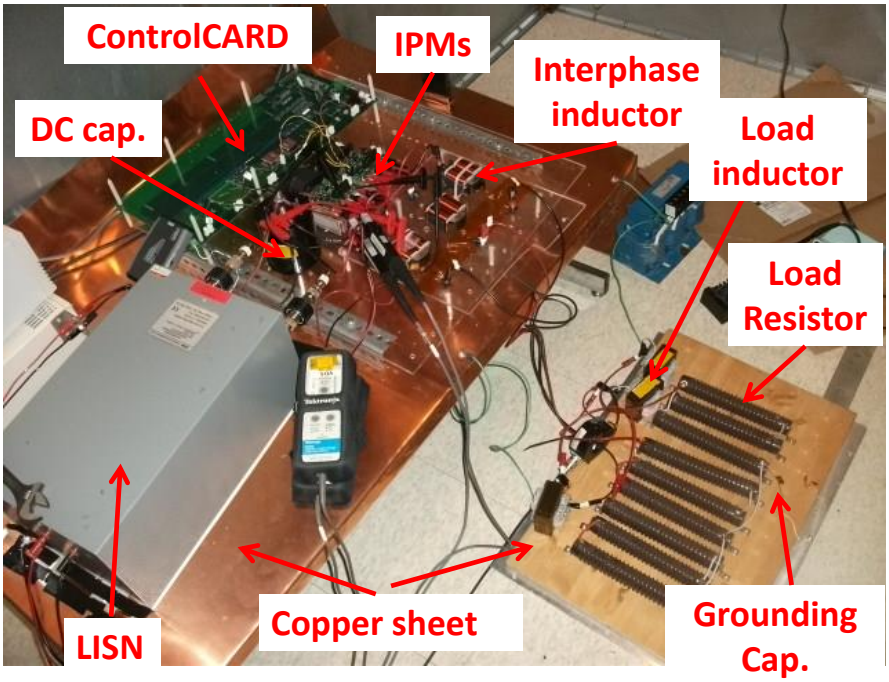
the critical point to designing the filter is changed to 170 kHz with a small attenuation, thus the corner frequency is increased significantly as shown in Table 3-1.

Table 3-1 EMI filter design comparison with different interleaving angles

Inter. angle	Fcri(Hz)	Att_need	Fc(Hz)
0 °	373.2k	53.3dB	16.8k
180 °	393.5k	53.8dB	17.7k
12 °	170.6k	29.9dB	30.5k



(a) Experimental system structure



(b) Experimental system setup

Figure 3-29 2kW interleaved 2L VSI experimental system

Experimental verification is carried on a scale down 2kW interleaved VSI system with 300V dc link voltage, 30 kHz switching frequency and 200Hz line frequency. A RL load with an additional ground capacitor is used to control and change the propagation path impedance easily. The Experimental system structure is shown in Figure 3-29(a) and the system setup is shown in Figure 3-29(b). From previous analysis shown above, it is clear that the spectrum of the EMI noise current is determined by the noise source and the propagation path impedance. Figure 3-30 shows the measure propagation path impedance for CM noise. Due to the resonance between the load inductor and grounding capacitor, there is anti-resonance on system CM propagation path at around 260 kHz which create the resonance on CM noise at the same frequency as shown in the results.

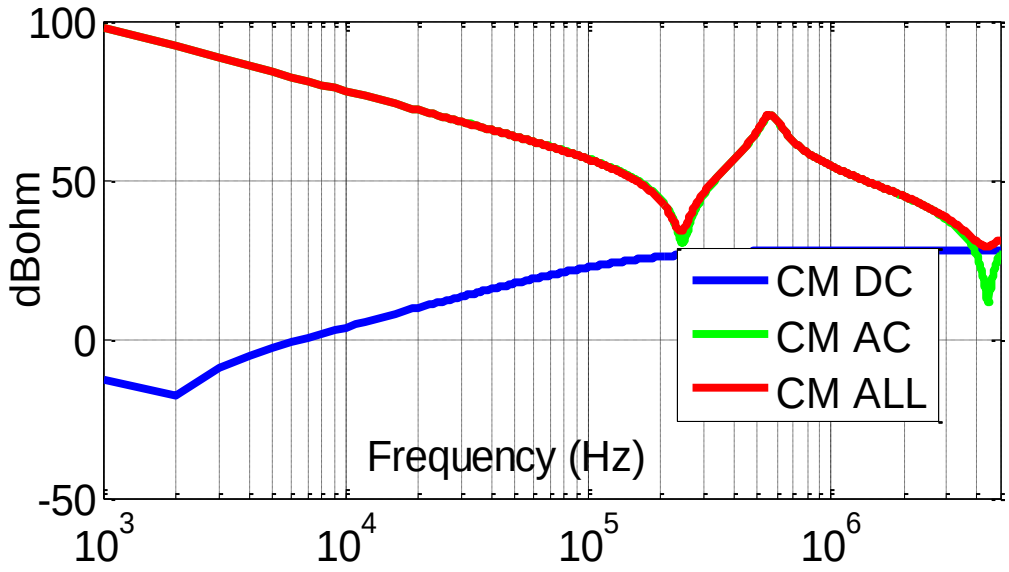


Figure 3-30 Measurement Results of the noise propagation path impedance

(DC CM: blue, AC CM: green; ALL CM: red)

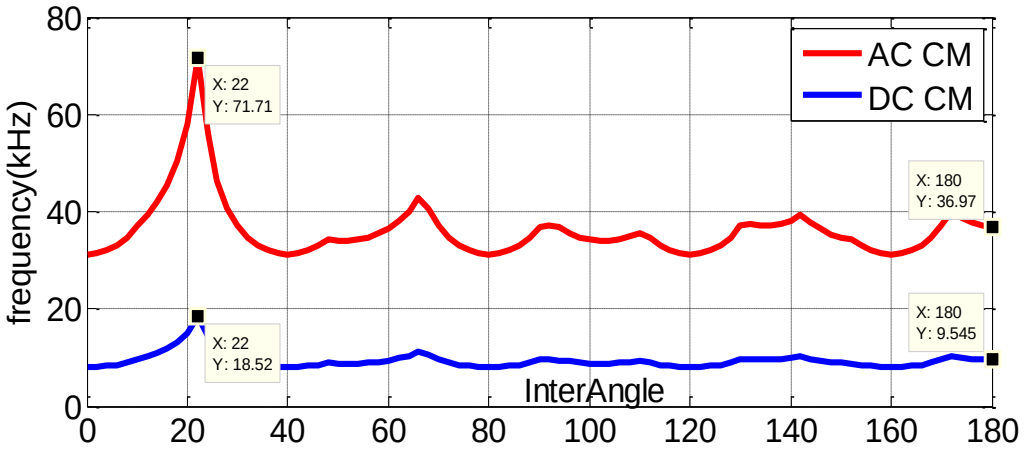
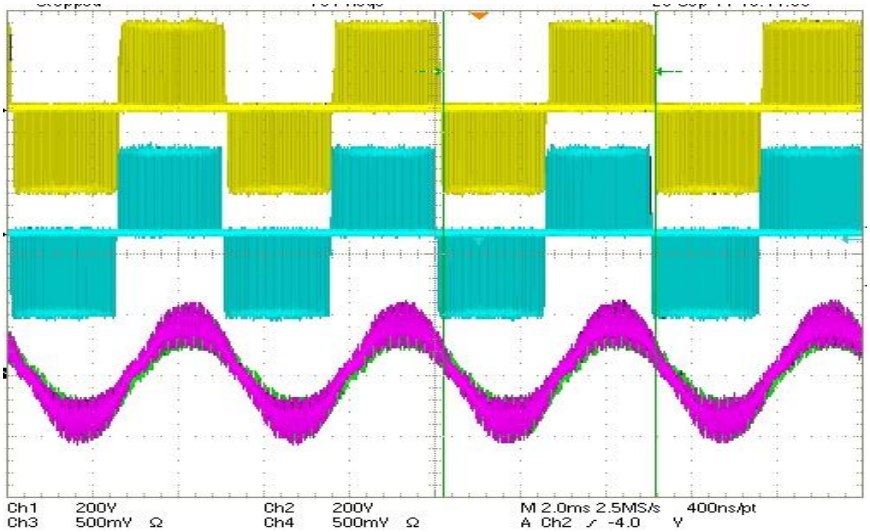
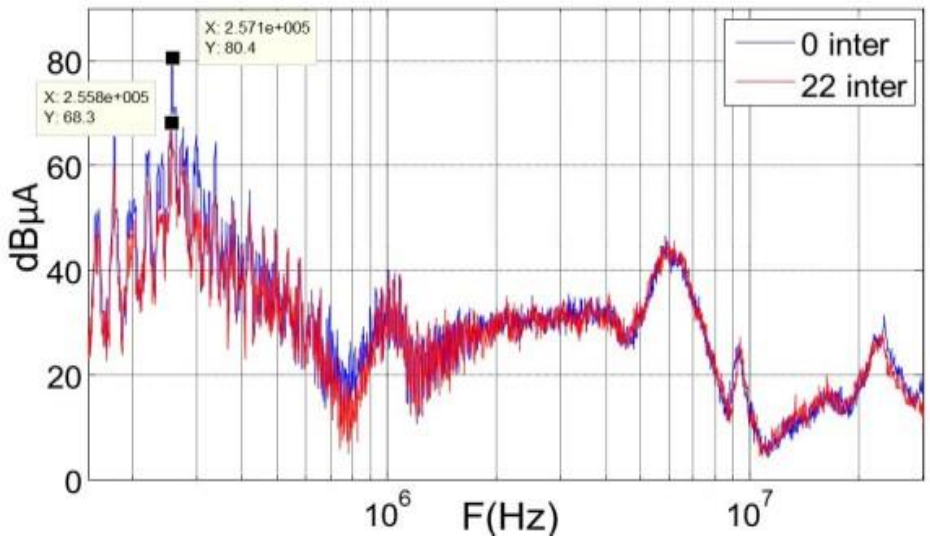


Figure 3-31 Optimized corner frequency with different interleaving angle

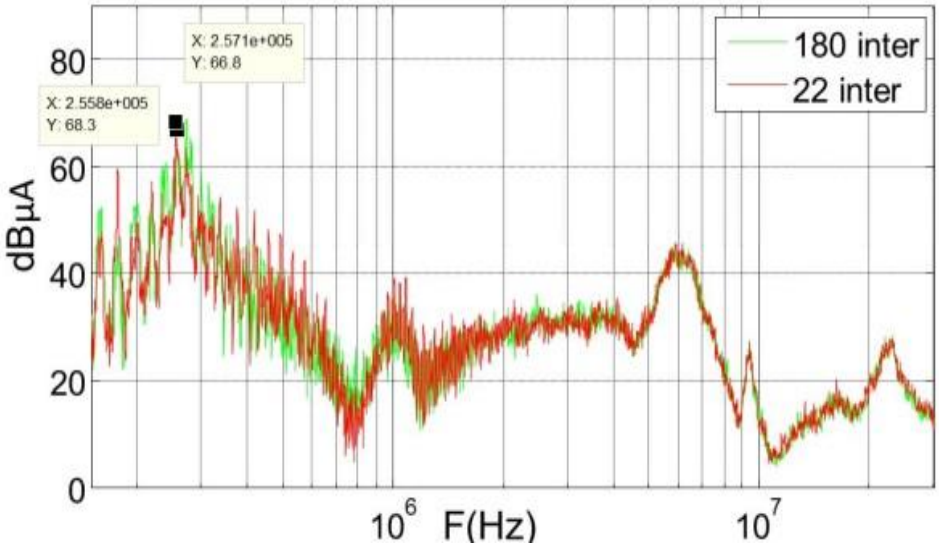
Based on this resonant frequency and system switching frequency, a 22 °interleaving angle is chosen using equation (3-7). Figure 3-31 depicts the resultant optimized EMI filter corner frequency with varying interleaving angle for both AC and DC terminals for the experimental test system. Thus, the system AC CM noise is measured and compared as an example with 0 °, 180 °and 22 °interleaving angle and the results are shown in Figure 3-32.



(a) **Time domain test results: V_{out1}:yellow;V_{out2}:cyan; I_{out1}:pink; I_{out2}:green;**



(b) Experimental ACCM noise (non-interleaving: blue and 22 °interleaving: red)



(c) Experimental ACCM noise (180 °interleaving: green and 22 °interleaving: red)

Figure 3-32 ACCM current EMI spectrum experimental results

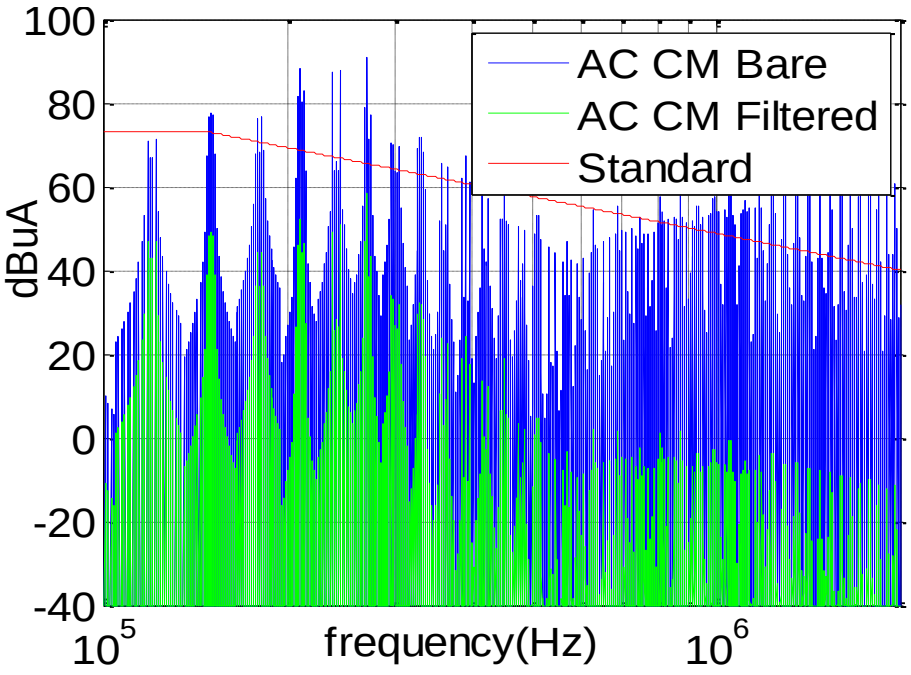
Comparing with the non-interleaved case, using 22 ° interleaving can attenuate the resonant peak at around 260 kHz by more than 12dB, which has a similar impact as 180 ° interleaving (as shown in Figure 3-32(b)), meanwhile it can also attenuate the harmonics near the resonant frequency which can reduce the total attenuation needed for EMI filter design and help to reduce the value of the inductor needed. However, as discussed above, small angle interleaving will have less reduction for the lower order switching harmonics

than symmetrical interleaving, thus it will have less benefit on the volt-second reduction on the inductor, since the weight of the inductor is determined by both the inductance and the volt-second on the inductor. The optimal interleaving angle for minimum inductor weight depends on the working condition of the power converter. The detailed trade-off will be discussed in the following section.

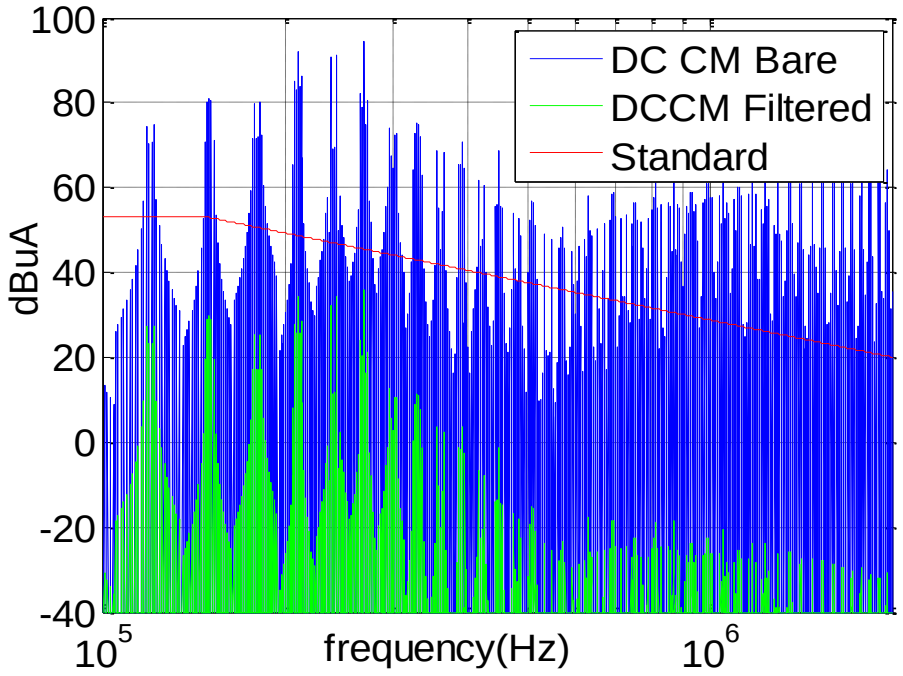
3.3.3 Passive Component Weight Minimization

Small angle interleaving will reduce noise at the resonant frequency thus it can reduce the attenuation from the system and the required inductor value for noise attenuation. However, smaller inductor value cannot ensure a smaller inductor weight, since the weight of the inductor is also determined by other design constraint such as saturation, loss and thermal performance during the real implementation. The weight of an inductor is not only determined by the inductance value, but is also determined by the volt-second value which has a significant impact on the saturation and core loss of the inductor. The impact of the volt-second on the inductor weight has been discussed in section 2.5.

In order to show an example of the impact of volt-second, CM EMI filters for the ac-side and dc- side terminals are designed separately following the proposed design method in section 2.3. The simulated system AC side spectrum before and after adding the EMI filters is shown in Figure 3-33(a), which shows that the EMI noise is effectively attenuated with the designed EMI filters within the EMI range. The DC side results are shown in Figure 3-33(b).



(a) AC CM noise (Bare noise: blue; filtered noise green)



(b) DC CM noise (Bare noise: blue; filtered noise green)

Figure 3-33 CM noise prediction results

The optimized corner frequency, L-C value and weight are given in Table 3-2. It is clear that due to the high frequency resonance (at around 250 kHz) in the EMI propagation impedance, the bare noise also has a resonant peak that will determine the EMI filter design

for both AC and DC sides. For the AC side filter, the corner frequency is located at 31 kHz, which means that the impedance of the L-C filter is nearly zero at this frequency. Further, since the converter switching frequency is also 30 kHz, the current is through L and C is large. Since the volt-second on the inductor equals to Lcm × Icm, which in this case is also large, the designed filter weight is more than 4 kg.

Table 3-2 Filter implementation results without interleaving

	AC	DC
Critical Frequency (kHz)	270	270
Attenuation Needed (dB)	37.5	61.1
Corner Frequency (kHz)	31.7	8.05
CM capacitance C_{CM} (nF)	20	100
CM inductance L_{CM} (mH)	1.3	3.9
Volt-second (Vs)	1.6m	8.5u
Weight (g)	4889	45.4

The results are quite different on the DC terminal since the standard is stricter than the AC side, thus, a higher attenuation is required translates into a much lower corner frequency of 8.05 kHz. The inductor value is consequently much larger, but, since the converter switching frequency is 30 kHz and the fundamental frequency 200 Hz, there is no voltage excitation at 8.05 kHz, which results in much smaller volt-seconds on the DC inductor when compared to its AC counterpart. Consequently, the DC inductor weight is also much smaller than that of the AC inductor.

Two methods can be used to reduce the volt-seconds on the AC inductor: 1) add damping, a lot of works has been conducted regarding the optimal damping in the filter, however, adding damping needs a big resistor value with associated high losses, thus, this

option is not considered in this work; 2) increase the inductance value to shift the corner frequency, which can significantly reduce the volt-seconds as shown in Figure 3-34.

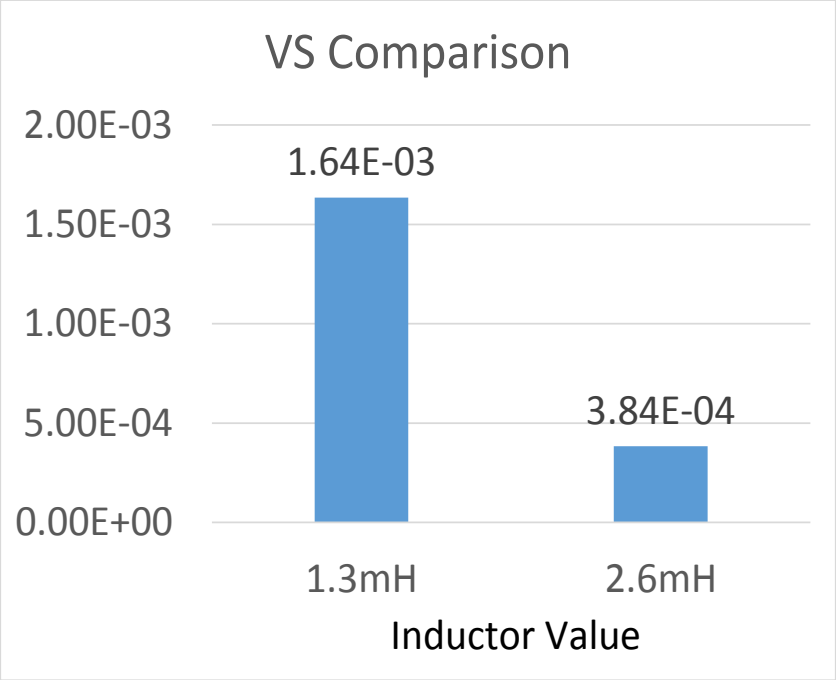


Figure 3-34 Volt-second on CM inductor with different inductor value

As seen, when the inductance is increased to 2.6 mH, the volt-seconds on the CM inductor are reduced by five times. The relationship between the inductor value and weight design results has already been shown in section 2.3 Figure 2-41 which illustrates how the optimized inductor value does not yield an optimized inductor weight. For AC side inductors, for instance, a larger value can help reduce the volt-second on the inductor, which can also reduce its weight when the design is limited by the saturation of the inductor. This evinces that to obtain a minimum filter weight, the inductor volt-seconds need to be considered. For DC side, since the volt-seconds are already small enough, and the inductor design is determined by its inductance value, the smallest inductance value give yield the smallest weight as normally presumed.

As for the interleaved system, the previous analysis shows that the use of different interleaving angles will attenuate different switching frequency harmonics of the total noise source, while the impedance of the propagation path will remain the same. The test results show that 22 °will give the highest corner frequency for both AC and DC sides, which will yield the smallest CM choke inductance; however, the volt-seconds on the CM choke will not be reduced significantly. Using 180 ° interleaving on the other hand will only reduce the CM choke inductance by a small amount, but it can reduce the volt-seconds significantly. Consequently, both 22 ° and 180 ° interleaving angles are selected to design EMI filters for the ac-side and dc-side filters. Table 3-3 summarizes the filter design results, verifying the analysis regarding the impact of interleaving on inductance value and volt-seconds reduction.

Table 3-3 Filter implementation results for different interleaving angles

	AC		DC	
Interleaving Angle	22	180	22	180
Critical Frequency (kHz)	210	243	210	243
Attenuation Needed (dB)	18.7	32.8	42.2	56.2
Corner Frequency (kHz)	71.7	37	18.5	9.54
CM capacitance C_{CM} (nF)	20	30	100	100
CM inductance L_{CM} (mH)	0.25	0.93	0.74	2.8
Volt-second (μVs)	172	44	9.1	2.6

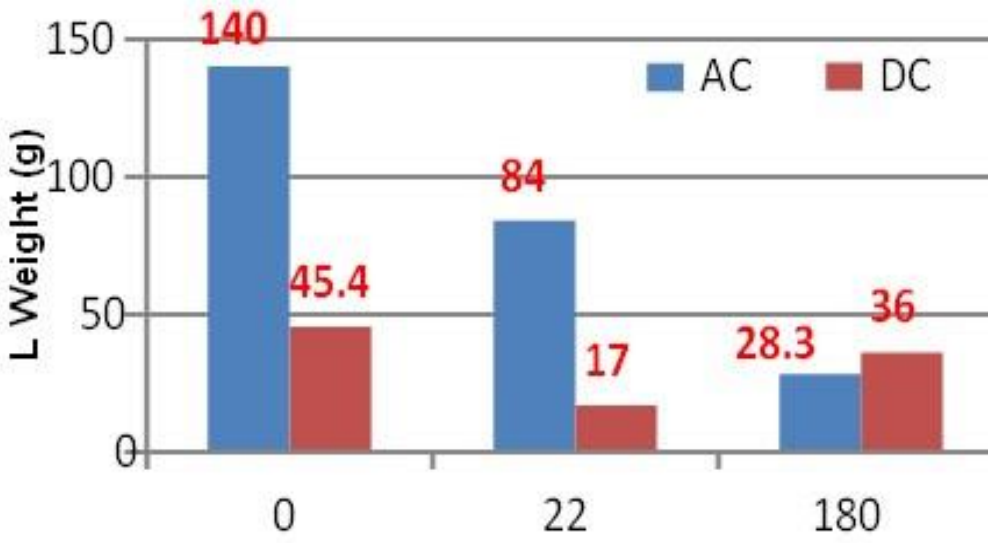


Figure 3-35 EMI filter weight comparison of AC and DC sides

Following the minimum weight implementation procedure for filters shown in section 2.5, the design of the physical implementation for filters are performed. The weight comparison results of AC-side and DC-side EMI filters are presented in Figure 3-35, which shows that both 22 ° and 180 ° interleaving angles can help reduce the weight of the CM choke inductor compared with non-interleaving case; However, since the dominating constraints for the weight of the choke inductors are different for AC and DC sides, the optimal points of the filter weight minimization are also different. In this system, since the dominating constraint for the weight of the AC CM choke inductor is the volt-seconds, 180 ° interleaving will attain a higher weight reduction for the AC CM filter. For the DC CM choke inductor on the other hand, as predicted, the inductance value is the main constraint that limit the design and weight reduction potential of the inductor; thus 22 ° interleaving will achieve a higher weight reduction.

3.3.4 Summary and Discussion

This section presents a complete analysis of the impact of interleaving on system filter weight reduction for three phase power converters. A motor drive system with an

interleaved three-phase voltage-source converter is taken as an example. The principle of interleaving operation is studied using the proposed equivalent circuits and the double Fourier integral transformation method. The analysis shows that changing interleaving angle will change the noise source in the system while the propagation path impedance will keep unchanged. With the consideration of the impact of propagation path impedance on system noise, a systematic design method for selecting the interleaving angle to reduce the EMI noise is proposed. The results show that symmetric interleaving can reduce the volt-second on the system more effectively, while the small angle interleaving can help to minimize the inductor value needed for noise attenuation. Considering the real implementation of the filters, the passive component weight reduction for interleaved three phase converters is analyzed in detail with different interleaving angles. All the analysis is verified through both simulation and experimental tests. The results show that by using calculated optimal interleaving angle based on the method proposed, the EMI noise can be reduced by 10~12dB in the impedance resonant frequency range. Moreover, since the determine factors for EMI filter weight is different for AC side and DC side, the optimal interleaving angle selections of the minimum filter weight of AC and DC sides are also different. For the experimental system, small angle interleaving achieves a higher weight reduction for DC CM filter while the symmetrical interleaving is better for AC CM filter weight reduction. The analysis is focused on CM noise reduction and CM filter weight minimization, since the CM filters takes a big portion of the total passive component weight in dc-fed motor drive system with long connecting cables, however, all the design procedures and methods can also be applied for DM noise analysis.

3.4 Design and Integration of Interphase Inductor

In interleaving topology, when the output voltages of the two converters are phase-shifted, there will be a voltage difference between the same phase of the two converters, thus, there will be circulating current generated between the two converters. Since the circulating current will increase device current stress and change system losses, certain interphase reactors is needed to limit the magnitude of the circulating current [88]. Previous studies has discussed the control method of circulating current and the impact on the passive component weight in rectifier applications. However, since the load inductor is inside the motor in motor drive applications. Additional inductors are necessary for circulating current suppression, these inductors are defined as the interphase inductor. Although it has been shown in the previous section that interleaving can help to reduce the weight of the filters, the additional weight of these interphase inductors will reduce the benefit of interleaving or even make the total weight of passive components heavier than non-interleaved system.

In order to reduce the weight penalty from the interphase inductors and reduce the total weight of passive components in interleaved converters, this section will present a detailed analysis of the design and implementation of the interphase inductors. First, the equivalent circuit for circulating current analysis is provided and the impact of circulating current on the loss distribution is analyzed in detail in section 3.4.1. Based on the equivalent circuits, the design and implementation method of interphase inductor is presented in 3.4.2. The interphase inductors are designed for the experimental system used in the previous section and the design results show that interleaving will increase the total weight of the passive component if ideal coupled inductors are used. In order to reduce the penalty of the

additional weight from interphase inductors, section 3.4.3 presents a detailed analysis of the integration of the interphase inductors that can fully utilize the magnetic core. Finally, section 3.4.4 shows that experimental verification of the analysis using the 2kW dc-fed motor drive system.

3.4.1 Circulating Current in Interleaving Topology

In interleaving topology, when certain interleaving angle is selected, the output voltage of the two converters will be phase shifted and there will be a voltage difference between the same phase leg of the two converters as shown in Figure 3-36.

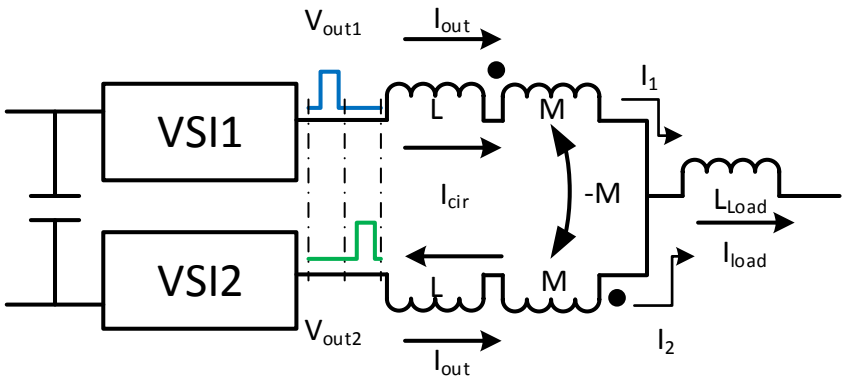


Figure 3-36 Interphase inductor and circulating current

This voltage difference will generate the circulating current that propagate between the same phase of the two converters and make the total current through each converter different. The current through each phase can be decomposed as shown in (3-8)

$$\begin{cases} I_1 = I_{out} + I_{cir} \\ I_2 = I_{out} - I_{cir} \end{cases} \tag{3-8}$$

where, I_{cir} represents the circulating current that propagates the same phase of the two converters, I_{out} represents the remaining current which is the same on the two

converters and contribute to the load current. Since $I_1+I_2=I_{Load}$, it can be calculated that $I_{cir}=\frac{I_1-I_2}{2}$ and $I_{out}=\frac{I_1+I_2}{2}$.

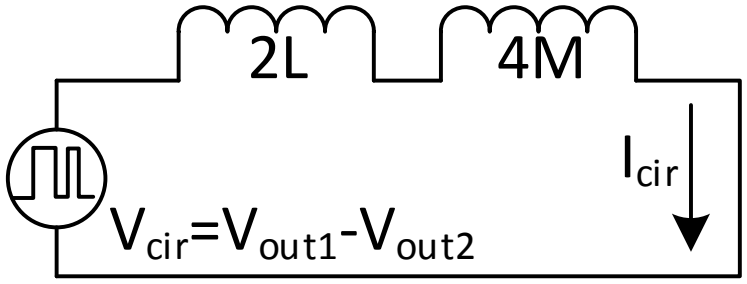


Figure 3-37 Equivalent circuit for circulating current analysis

The equivalent circuit for circulating current analysis is shown in Figure 3-37. It is clear that the circulating current is only related with the voltage difference between the two phases and the total inductance (L_{cir}) in the circulating loop which is the determined by the DM fitter inductance and the addition interphase inductance. When the interleaving angle is determined, the circulating current can be calculated as shown in (3-10).

$$I_{cir}=\frac{V_{cir}}{L_{cir}},\ \text{where VS}=\begin{cases}V_{dc}DT_s & D<\frac{\kappa}{360}\\ V_{dc}\frac{\kappa}{360} & \frac{\kappa}{360}<D<1-\frac{\kappa}{360}\\ V_{dc}(1-D)T_s & D>1-\frac{\kappa}{360}\end{cases} \tag{3-10}$$

Figure 3-38 shows the simulating results of the voltage difference between the two converters and the circulating current, which verifies the equivalent circuit for circulating current analysis.

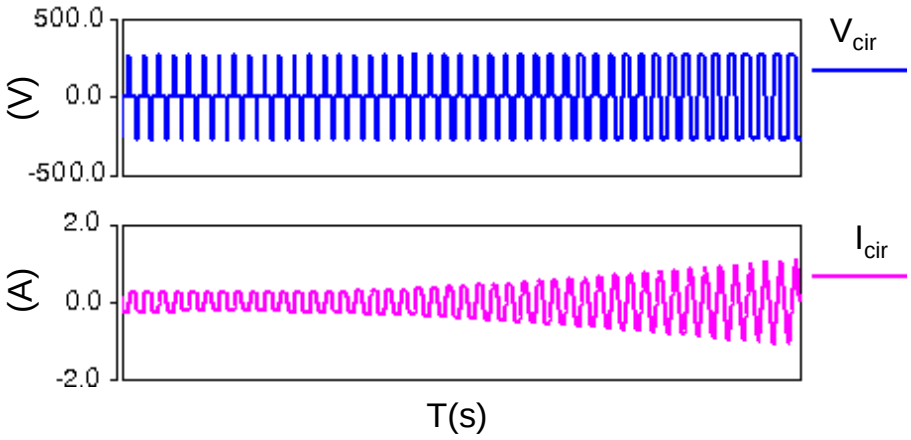


Figure 3-38 Simulating results of the voltage difference and the circulating current

Since the circulating current is an additional current generated by interleaving, it will change the current waveform through each devices and change the loss distribution in the converter. Figure 3-39 shows the device current during switching with interleaving and without interleaving, it shows that the turn-on current is reduced and turn-off current is increased due to the existence of circulating current.

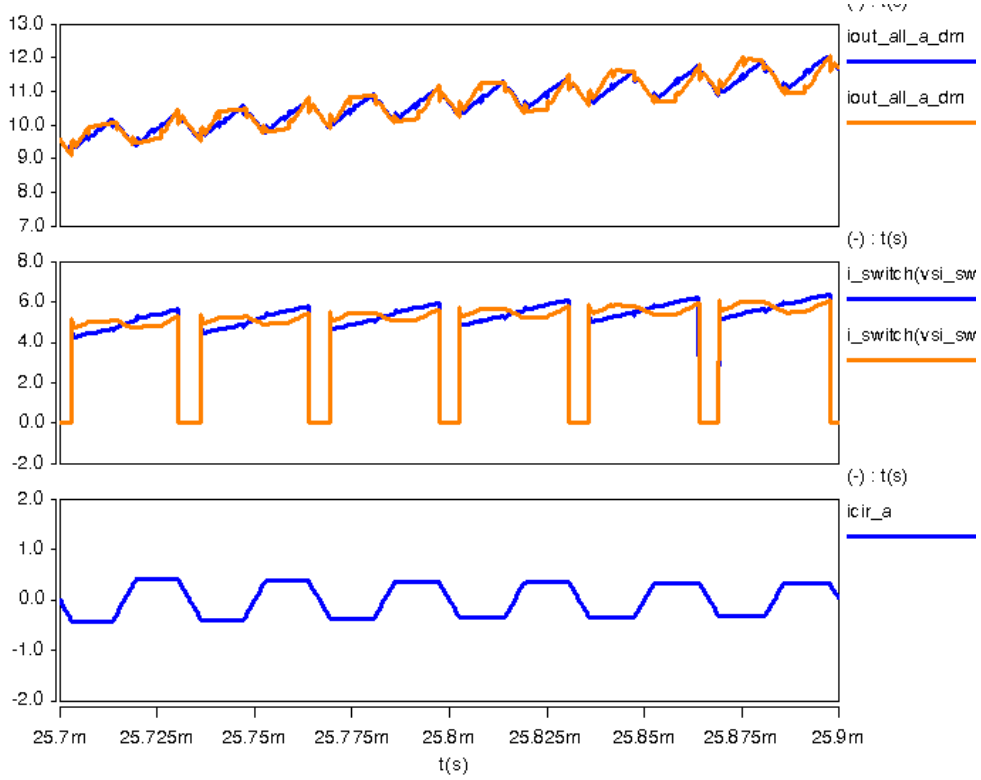


Figure 3-39 Simulation results of device current during switching

The impact of circulating current on converter loss distribution can be calculated analytically. Assuming output current ripple is small and carrier ratio (defined as the ratio between switching frequency and fundamental frequency) is high, one can assume that the current through devices during each switching period is constant without interleaving as shown in Figure 3-40.

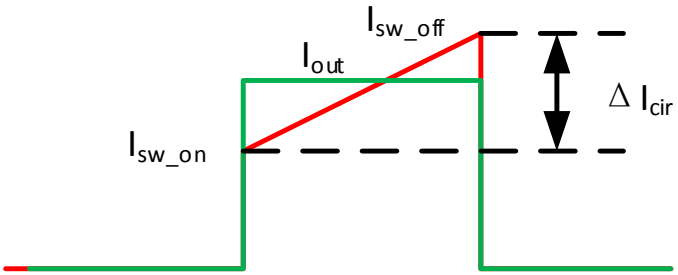


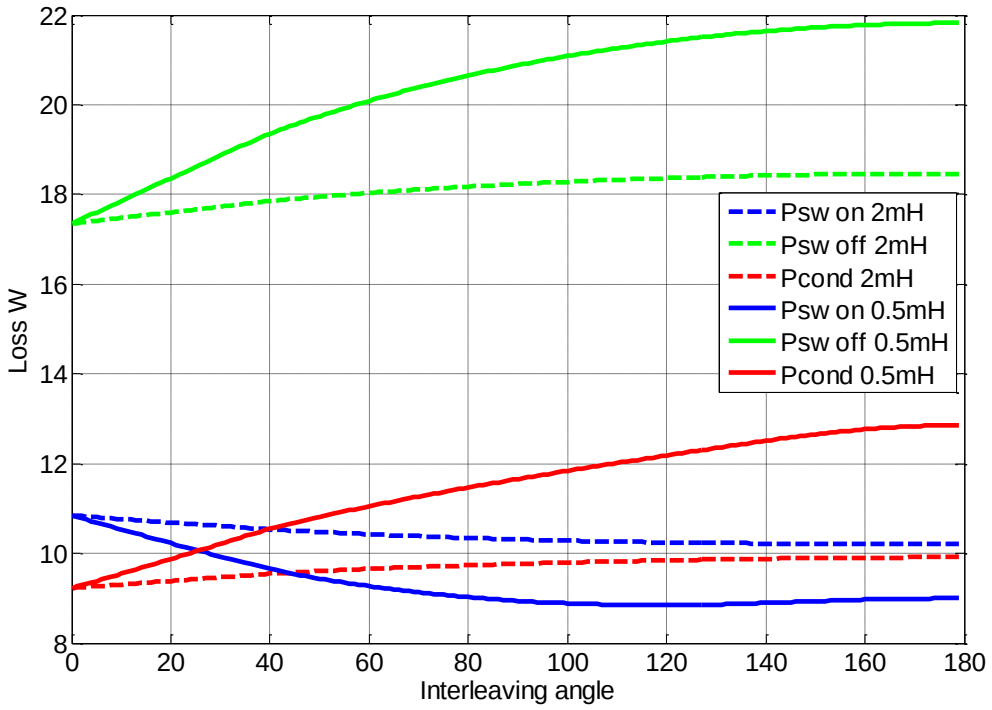
Figure 3-40 Impact of circulating current on semiconductor power losses

With interleaving, the circulating current will be added to the output current, the changes during each switching period can be calculated with (3-10), then the current changes during each switching cycle can be calculated separately. Then conduction energy (E_{cond}), turn-on energy (E_{on}), turn-off energy (E_{off}) and reverse recovery energy (E_{rr}) can be calculated based on the measurement results at rated switching condition which can be got from device datasheet as shown in (3-11).

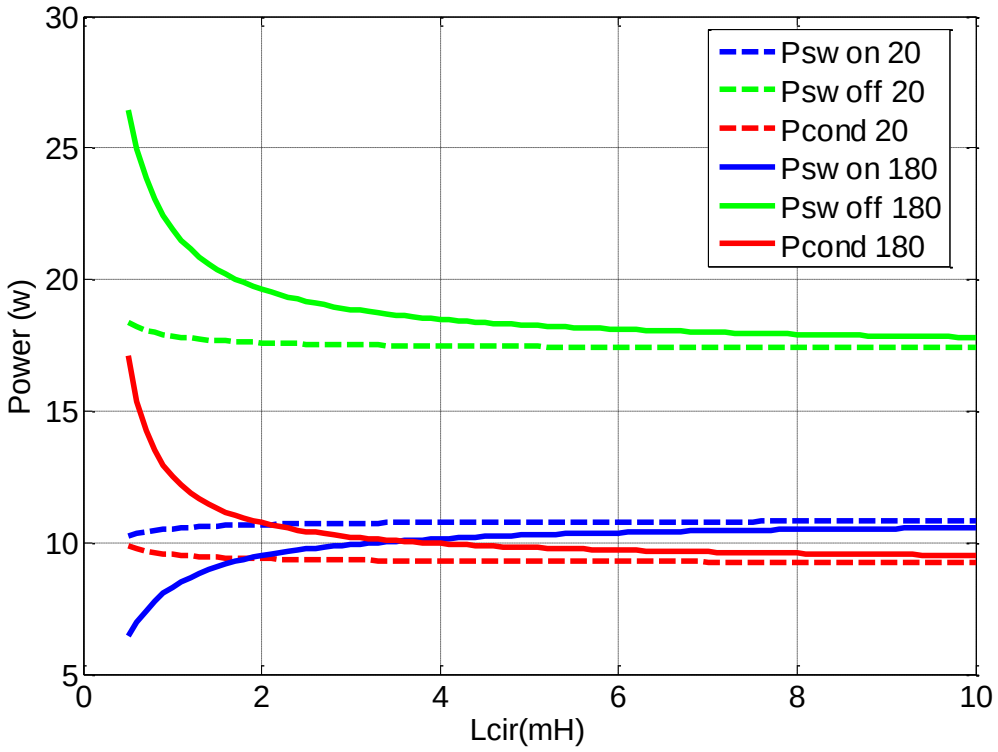
$$\begin{cases} E_{cond} = \int i_s V_{s\_cond} dt = \sum (I_{sw\_on} + kn\Delta t) \times (R_{on} \times (I_{sw\_on} + kn\Delta t) + V_{on}) \Delta t \\ E_{on} = \dfrac{I_s V_s}{I_{rated} V_{rated}} E_{on\_rated} \\ E_{off} = \dfrac{I_s V_s}{I_{rated} V_{rated}} E_{off\_rated} \\ E_{rr} = \dfrac{I_s V_s}{I_{rated} V_{rated}} E_{rr\_rated} \end{cases} \tag{3-11}$$

In order to show the impact of circulating current on system loss distribution. A loss calculation was conducted on the experimental system with different configurations, the device loss data was obtained from the datasheet of the IPM modules used in the

experimental system with different configuration as an example. Figure 3-41(a) shows the loss changing versus the interleaving angles when different interphase inductors were added into the system. The results indicate that increasing interleaving angle will reduce the turn on loss but increase the turn-off loss and reverse-recovery loss since it will increase the circulating current in the system. In terms of the impact of circulating current on system total loss, it depends on the characteristics of the devices. In some systems where turn-on loss is dominant, increasing the circulating current may help to reduce the total loss. Figure 3-41(b) shows the loss change versus the inductance in the circulation loop with different interleaving angles. It shows that increasing the inductance in the circulating loop can reduce the impact of interleaving since it can reduce the circulating current in the system. The results also indicate that when the inductance in the circulating loop is big enough, further increasing the inductance will have less impact since the circulating current is already small enough and the impact is not significant anymore.



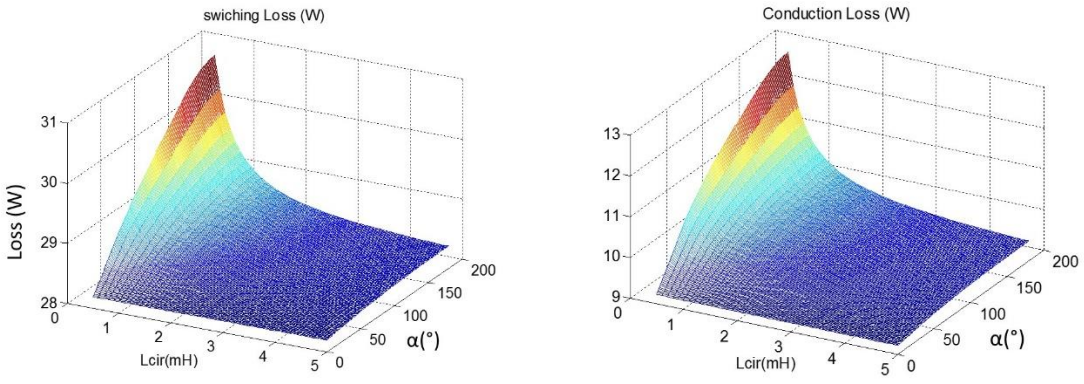
(a) Calculation results of loss change with interleaving angle under different interphase inductance



(b) Calculation results of loss change with inductance under different interleaving angles

Figure 3-41 Calculation results of loss change with inductance and interleaving angles

Figure 3-42 shows the 3-D plot of relationship of the loss changing, interleaving angle and the interphase inductor value in the circulating loop. It is clear that when interleaving angle is bigger (near 180 °) and inductance is smaller, both switching loss and conduction loss will be larger since the circulating current is larger, this results depends on the characteristics of the power device. In some system total switching loss may decrease when circulating current is bigger, but the condition loss will also increase when circulating current is bigger since it will increase RMS current through the power device.



(a) Switching loss **(b) Conduction Loss**

Figure 3-42 3-D plot of the relationship of the loss changing, interleaving angle and the interphase inductance

It need to be noticed that the circulating current is an inner design constraint, the limitation should be selected to avoid the voltage overshoot on the power devices during switching and loss limitation of the system (efficiency and thermal design), when the requirement for the circulating current is determined, the additional interphase inductor value can be calculated from (3-10) and physical implantation can be designed based on the value and the working condition of the inductor.

3.4.2 Design and Implementation of the Interphase Inductors

From the previous analysis, it is clear that the circulating current need to be limited in interleaving system to reduce systems loss and ensure a normal working condition. The equivalent circuits indicate that the circulating current is determined by the voltage difference between the two converters and the inductance in the circulating loop. When interleaving angle is determined the voltage difference between the two converters is also fixed. Thus the inductance in the circulating loop need to be designed to limit the circulating current. In rectifier applications, the boost inductors can be split and served as the interphase inductors. However, the value of the boost inductor is designed based on the current ripple requirement, if it is not enough for the circulating current limitation, then

additional reverse coupled inductors are needed. For motor drive applications, since the load inductor is inside the motor, the only inductor that can be used as interphase inductor is the AC DM inductor in the filters which usually have a small inductance (usually several μH, thus adding reversed coupled inductor is an effective method to limit circulating current. From the equivalent circuit for circulating current analysis, it is clear that minimum inductance needed in the system can be calculated from (3-10) when the requirement for the circulating current is known. When the inductance of the coupled inductor is calculated, the physical implantation can be designed based on the value and the working condition of the inductor.

It need to be noticed that the circulating current only propagate between the two converters and it will not influence the EMI noise emission from the system. The equivalent circuits also indicate that adding ideal reverse coupled inductor into the system will not only change the impedance of the circulating loop and it only works for circulating current suppression, thus adding ideal reverse coupled inductor will not change the EMI noise emission in the system. However, the AC DM inductors will show in the circulating loop and change the circulating current, thus, the design of the additional interphase inductor should be done after the design of the EMI filter with the consideration of the DM inductors in the analysis.

Since coupled inductors are additional components added to the system. It need to be designed carefully to reduce the total weight of the passive components. Toroidal cores are implemented for the reverse coupled inductors and bifilar winding structure is used to reduce the leakage inductance as shown in Figure 3-43.

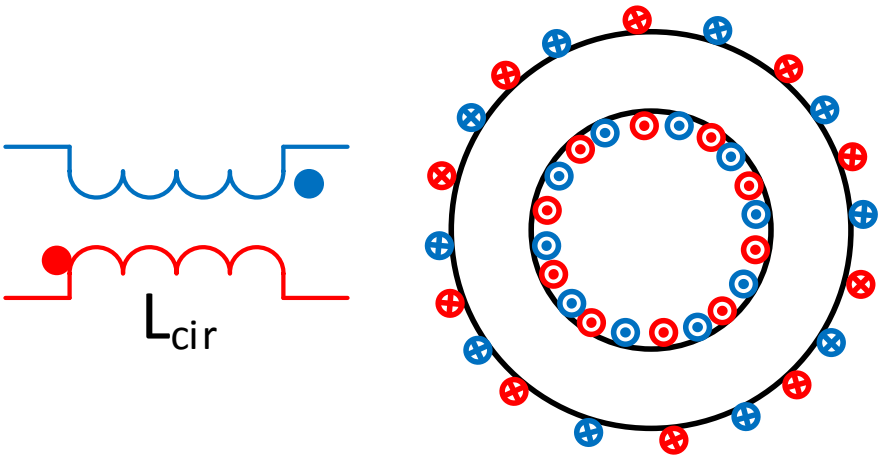


Figure 3-43 Interphase inductor with reduced leakage inductance

With a relatively small leakage inductance, the volt-second on the interphase inductor can be calculated from the equivalent circuit and it is only determined by the voltage difference between the two converters that is related with the interleaving angle. With the information of inductor value, volt-second on the inductor and the current through the inductor, the inductor can be optimized for the minimum inductor weight. In order to get the minimum weight of the coupled inductor, all of the possible dimensions of the toroidal core are swept under the constraints of physical fit, core saturation and core temperature rise. These constraints are similar with the design of choke inductors for EMI filters as shown in section 2.5. However, there is a difference between the two procedures, in the design of choke inductors for EMI filters, the volt-second on the inductor is related with inductor value, thus the inductance of the CM choke also need to be within a range to ensure the accurate estimation of the volt-second. However, the volt-second on interphase inductor is fixed when the interleaving angle is fixed, thus the limitation from the circulating current requirement only define the minimum required value for the inductor, during the optimization process the final value can be much bigger than the required value as long as it can give smallest inductor weight.

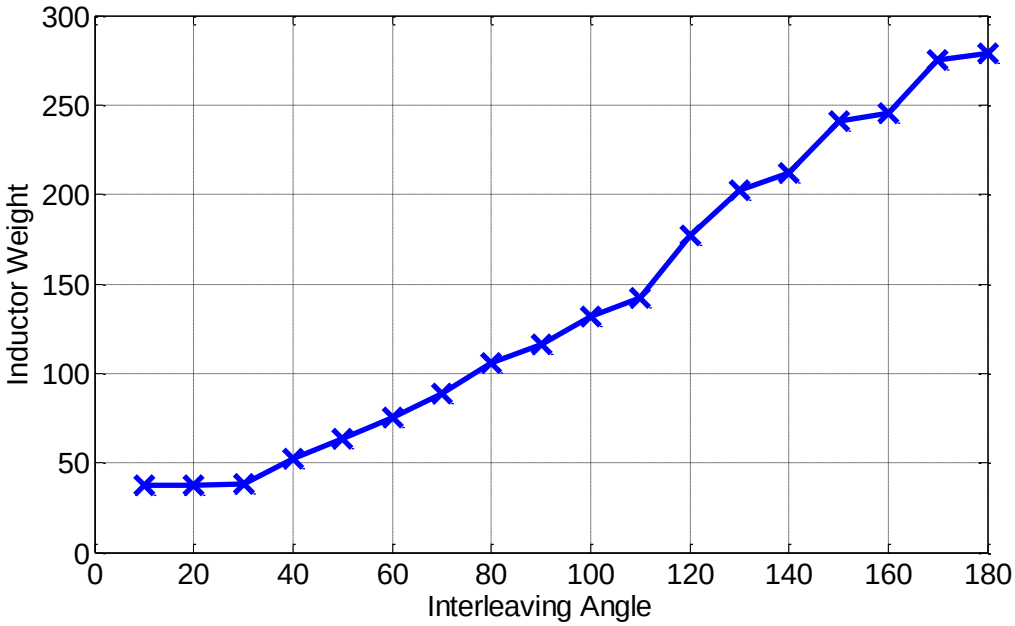


Figure 3-44 Coupled inductor weights VS interleaving angles

Figure 3-44 shows the design results of the weight of the coupled inductors VS interleaving angles for the experimental system. It is clear that the weight of the reversed coupled inductor highly depends on the interleaving angle. When interleaving angle is small, the coupled inductor is also small and vice versa. This is because the optimization results are determined by the volt-second on the inductor other than the inductor value, thus when interleaving angle is smaller, the volt-second is smaller and the coupled inductor is also smaller. Moreover, since the voltage on the interphase inductor is switching frequency excitation, the core loss is relatively high. It is clear that the inductor weight is determined by the temperature rise of the inductor, which make the coupled inductor heavy.

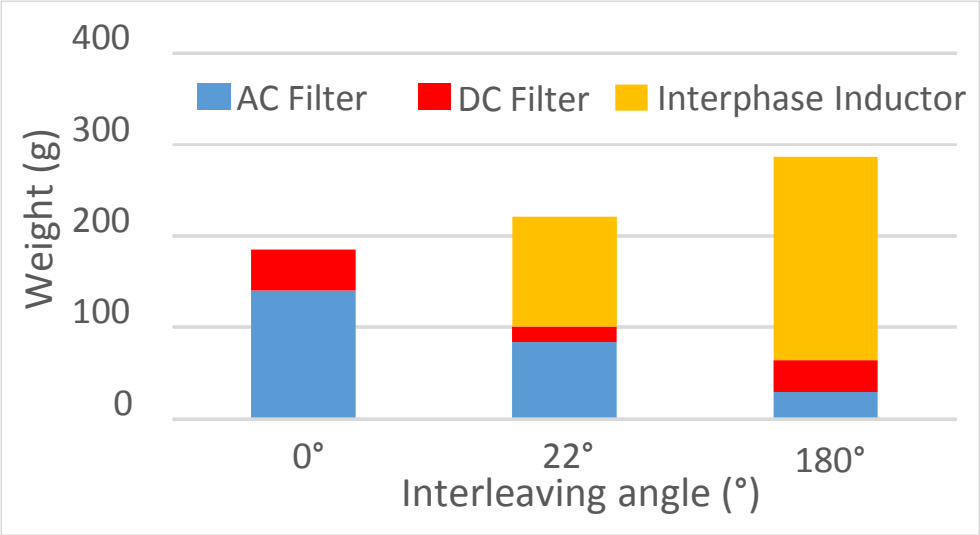


Figure 3-45 Total passive component weight comparison with different interleaving angle

In motor drive system, three additional interphase inductors are necessary for the circulating current suppression. Since the coupled inductors are additional passive components of the system, Figure 3-45 shows the total passive component weight comparison with different interleaving angles. It shows that the increase of the additional coupled inductor weight is more than the EMI filter weight reduction, thus interleaving will increase the passive component weight regardless of the interleaving angle for motor drive system with the ideal reverse coupled inductors added in the system.

3.4.3 Integration of Interphase Inductors

The optimization results of the coupled inductor shows that the weight is determined by the temperature rise of the inductor, Table 3-4 shows the optimized inductor design results. It shows that the designed inductor value (0.54H) is much larger than required value (2mH) and the flux density (0.3T) is lower than the saturation limitation (1T), thus the core is not fully utilized. In order to further reduce the total weight of the system the coupled inductor can be integrated with other inductors in the system to fully utilize the core.

Table 3-4 Design results of interphase inductors with 180 interleaving

Total Weight (g)	73.16
Total Volume Net (cm^3)	9.45
L (H)	0.5428
B (T)	0.32
Core Loss(W)	3.22
WireLoss(W)	2.35
Trise(°C)	99.5

In motor drive system, the interphase inductor can be integrated with the AC DM filter inductor. Instead of twisting the wire of the coupled inductor, the two windings can be separated as shown in Figure 3-46 to increase the leakage inductance which can perform as the AC DM filter inductors (L_{DM}).

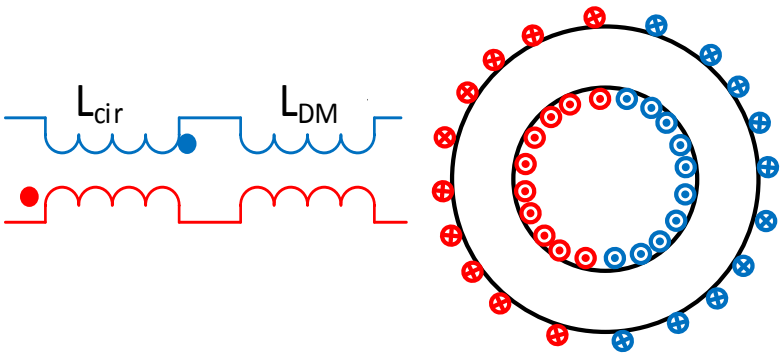


Figure 3-46 Integrated interphase inductor

Adding L_{DM} will introduce additional volt-second from the output current (I_{out}) and the new total volt-second can be calculated as shown in equation (3-12).

$$VS_{Total} = L_{DM} I_{out} + VS_{cir} \tag{3-12}$$

Where VS_{cir} is the volt-second generated due to the voltage difference between the two converters by interleaving. $L_{DM}I_{out}$ is the volt-second generated by adding the leakage inductance and it is proportional to output current. Moreover adding L_{DM} will also increase the core loss as shown in equation (3).

$$P_{fs} = \sum_{n=1..CR}\left(a\left(\frac{VS_n}{NA_c}\right)^c (f_s)^d V\times Ts\right),$$
$$P_{f1} = a\left(\frac{L_{DM}I_{out}}{NA_c}\right)^c (f_1)^d V\times Ts\times f_1, \quad (3\text{-}13)$$
$$P_{Loss\_core} = P_{fs} + P_{f1}$$

Where P_{fs} is the core loss generated due to the voltage difference of the two converters that is related with switching frequency and P_{f1} is the additional core loss due to the leakage inductance that is relate with fundamental frequency. For motor drive system f1<<fs, Thus P_{f1}<<P_{fs}, which means that adding L_{DM} will increase the volt-second on the interphase inductor that is low frequency, thus the additional loss is negligible. Since the coupled inductor weight is determined by temperature rise, adding leakage inductance will not increase the inductor weight if the total volt-second do not exceed the saturation limit. The integrated interphase inductor design result is shown in Figure 3-47 for different interleaving angles and different leakage inductances.

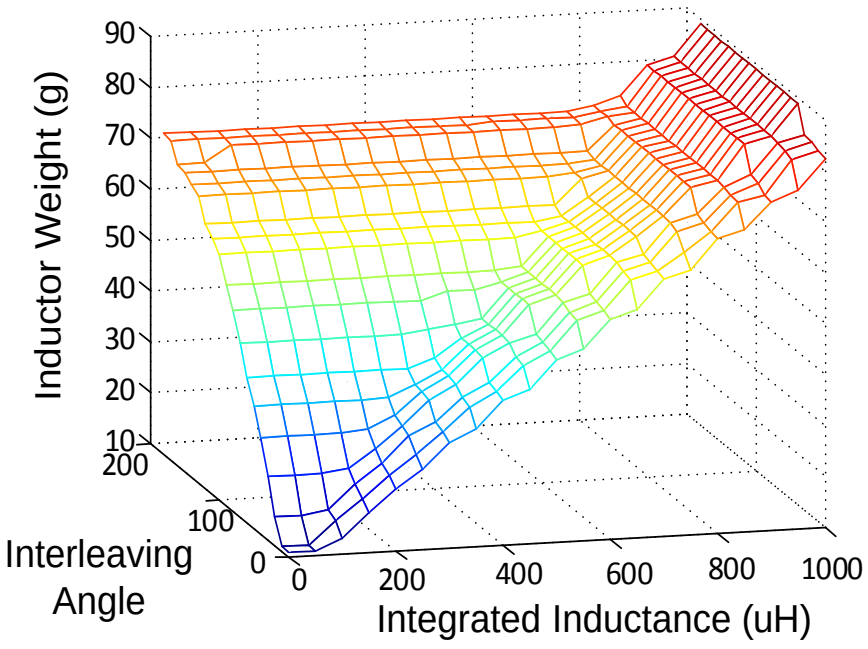


Figure 3-47 Integrated inductor design results with different interleaving angle

The design results show that adding leakage inductance will not increase the inductor weight until the volt-second determines inductor weight. Thus, the AC DM inductor is implemented with no weight increase of the interphase inductor. When interleaving angle is large, the maximum allowable DM inductance without increasing the weight of the coupled inductor is bigger. However, for small angle interleaving condition, since the volt-second introduced by interleaving is relatively small, the maximum allowable DM inductance for integration is smaller, since the addition volt-second will become dominant and determines the weight of the coupled inductor.

In motor drive system, the DM inductor value in EMI filter is relatively small and DM inductor weight is not dominant in the total passive component weight. Thus, integrating the coupling inductors with DM inductor for motor drive system can help to reduce the total passive component weight, but the benefit is limit. Interleaving will still increase the total passive component weight compared with non-interleaving topology.

The same integration ideal can also be implemented in the rectifier application, where the coupled inductor can be integrated with the boost inductor. Since boost inductor is the main energy storage component in rectifier, it take a significant portion of the total passive component weight. Moreover, in such applications, the boost inductor is determined by the current ripple requirement, the inductance need to be controlled and the volt-second on the inductor is mainly introduced by fundamental frequency current. During the design of boost inductors, the weight is usually determined by the saturation limitation while the core loss and temperature rise is relatively small. In other words the core is not fully utilized either. Then, the integration can be reversed to integrate the coupled inductor with the boost inductor. In order to accurately control the value of the boost inductor, the “EE” shape core

structure as shown in Figure 3-48 will be used, where the air gap L_2 can be adjusted to control the inductance value of the boost inductor while L1 can be adjusted to control the inductance value of the coupled inductor separately.

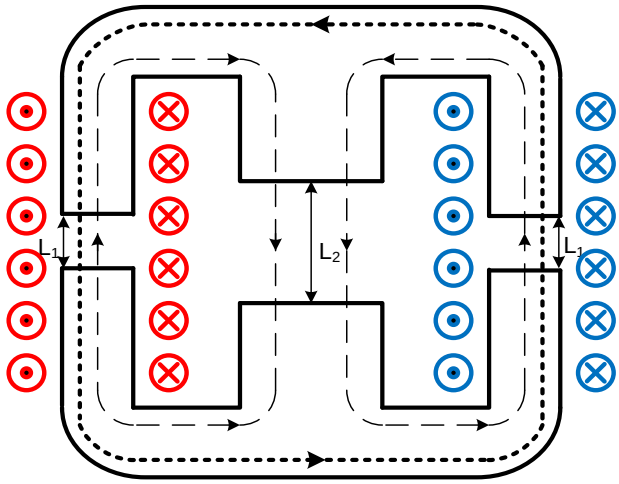


Figure 3-48 EE shape core for integrated interphase inductor implementation

In this case, the integrated coupled inductor will introduce a high frequency volt-second that will increase the core loss while almost keep the maximum volt-second the same. Since the boost inductor weight is dominant by the saturation limitation which is related with the maximum volt-second, increasing core loss will not change the design for the boost inductor, thus the coupled inductance is obtain at no cost of weight increasing. Figure 3-49 shows a design example of a 1mH boost inductor with coupled inductor integrated using EE core under different interleaving angle operations. The results include both the temperature rise of the inductor and the weight of the inductor, it is clear that increasing interleaving angle will increase the high frequency volt-second in the core thus the inductor temperature rise (Trise) will increase, before it hit the design limitation (100 ℃), the boost inductor weight will not increase since it is determined by the saturation limitation. When Trise reach the design limitation, the inductor will be bigger, however, even with 180 interleaving the total weight only increase less than 30%, considering the

weight reduction of EMI filters by interleaving the two converters. Interleaving topology is preferred for rectifier application where the boost or output inductors is included in the system, then interleaving can really reduce the total passive component weight.

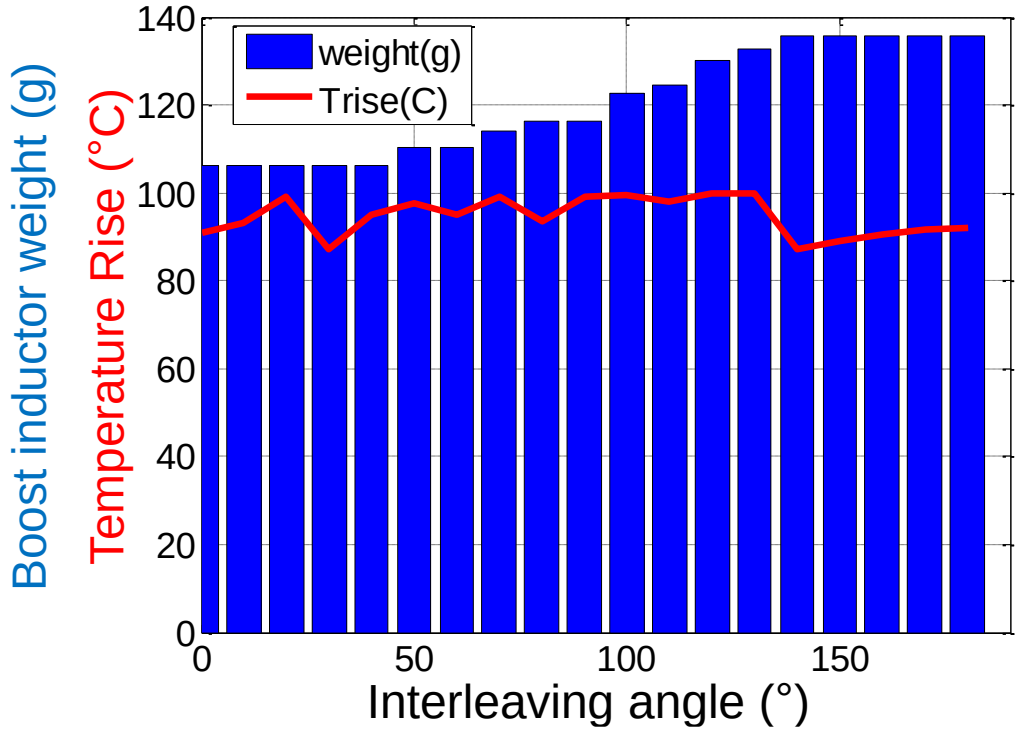


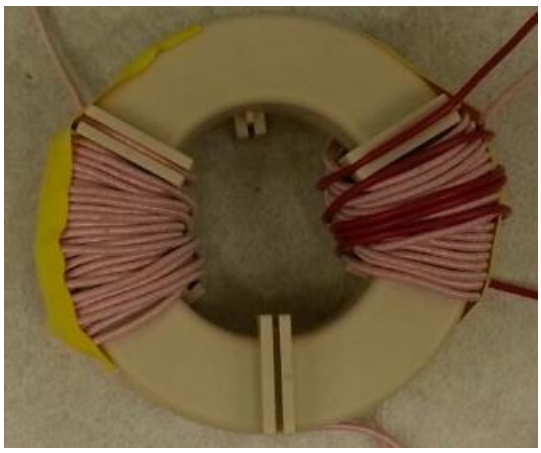
Figure 3-49 Design results of a 1mH boost inductor with coupled inductor integrated under different interleaving angle

3.4.4 Experimental Verification

To verify the analysis, two kinds of interphase inductor are built using nano-crystaline material with L_{cir}=20mH: one with twisted winding to reduce leakage inductance with L_{DM}=1uH as shown in Figure 3-50(a);one with separately winding to increase the leakage inductance with L_{DM}=60uH as shown in Figure 3-50(b). Additional open ended five turns is added to show the flux changing by measuring the voltage (V_{ext}) on the extra winding.

Both inductors are tested in the experimental systems as shown in Figure 3-29 with 2kW output power and 30 °interleaving angle.

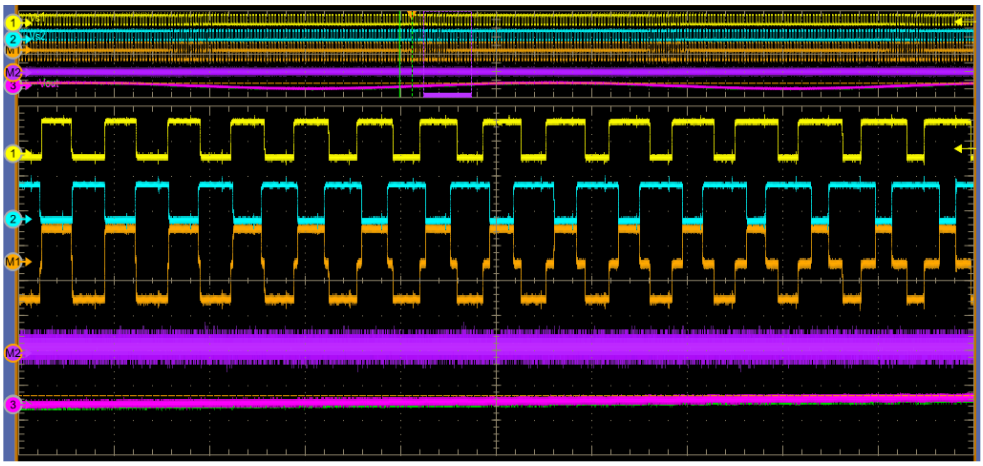
(a) Reduced leakage inductance



(b) Increased leakage inductance

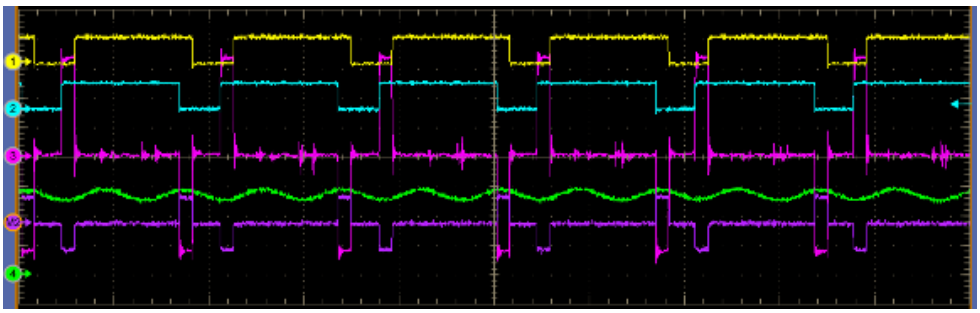
Figure 3-50 Implemented interphase inductor

The test results of the interphase inductors are shown in Figure 3-51. Since the interphase inductance is very big, the circulating current is well suppressed, thus the currents through two converters are almost the identical. It is clear that the output voltage of the two converters are phase-shifted. With the low leakage inductance, V_{ext} is the same with the voltage difference between the two converters, which shows that the volt-second in the core is determined by the voltage difference. However, for the inductor with high leakage inductance, there are more ringing on V_{ext} due to the leakage inductance added, and the integration of V_{ext} is larger than the results with low leakage inductance, which show the increase of the volt-second. Moreover, since the ringing will hardly change the magnitude of the switching frequency voltage excitation. The increase of core loss will be negligible.

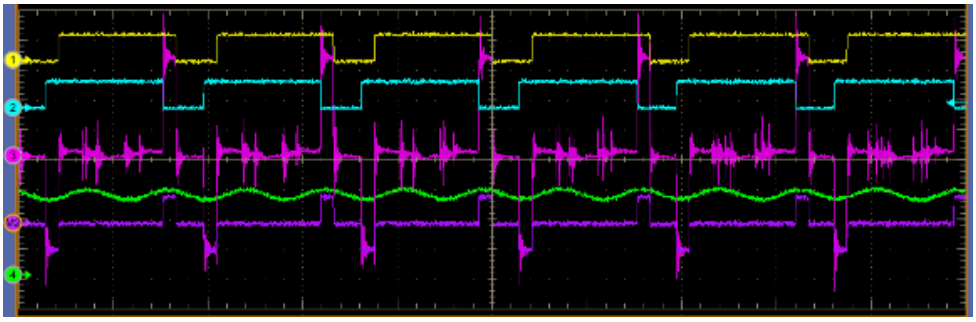


(a) Time domain result of circulating current

(V_{out1}:yellow;V_{out2}:cyan; V_{out1}-V_{out2}:orange; I_{out1}:green; I_{out2}: pink; I_{out1}-I_{out2}: purple)



(b) Results of adding interphase inductor with low leakage inductance (V_{out1}:yellow;V_{out2}:cyan; V_{ext}:pink; I_{out}:green; V_{out1}-V_{out2}: purple)



(c) Results of adding interphase inductor with high leakage inductance (V_{out1}:yellow;V_{out2}:cyan; V_{ext}:pink; I_{out}:green; V_{out1}-V_{out2}: purple)

Figure 3-51 Interphase Inductor test results

3.4.5 Summary and Discussion

This section presents a detailed analysis on the design and integration of interphase inductor for interleaved three phase VSI for three phase power converters. A dc-fed three phase motor drive system is studied as an example. The benefits and penalties of

interleaving on system passive weight reduction are analyzed in detail. The results show that interleaving will increase the total passive weight due to the additional weight of interphase inductors for motor drive systems. To solve this problem, a design method to integrate the interphase inductor with the AC DM inductor is proposed and analyzed in detail. All the analysis is verified through a 2kW prototype. The results show that certain value of AC DM inductance can be integrated with interphase inductor with negligible increase on the weight and the maximum integrated inductance is related with interleaving angle. In motor drive system, the DM inductor value in EMI filter is relatively small and DM inductor weight is not dominant in the total passive component weight. Thus, integrating the coupled inductor with DM inductor for motor drive system can help to reduce the total passive component weight, but the benefit is limit. The same integration ideal can also be implemented in the rectifier application, where the coupled inductor can be integrated with the boost inductor. Since boost inductor is the main energy storage component in rectifier, it take a significant portion of the total passive component weight which make interleaving topology preferred for rectifier application where the boost or inductors is included in the system.

3.5 Summary

This chapter presented a detailed analysis of the impact of interleaving on the passive components weight reduction for three phase power converters. The operation principle of interleaving topology, the design considerations and interleaving angle selection method for minimum filter weight were discussed in detail. To reduce the passive component weight of the system, the integration of interphase inductor was also studied in detail. As the principle study and preparation for the three phase power converters, this chapter first

presented the study of the impact of interleaving on input passive components weight reduction for high power dc-dc boost converters, which shows the design trade-off and how one can reduce the inductor weight by using interleaving technique and using different materials.

Extending the analysis to three phase systems, this chapter also provided the detail analysis of the impact of interleaving on filter weight reduction for three phase dc-ac power converters. Small angle interleaving selection method according to system propagation path impedance are proposed for filter value minimization. Filters were designed for AC and DC sides, which showed that the optimal interleaving angle selection is related with the design conditions.

In interleaving topologies, additional interphase inductor (or coupled inductors) are necessary to limit the circulating current generated by interleaving, The design and implementation methods of interphase inductors were studied in detail, the design results showed that interleaving will increase system passive component weight due to the penalty of additional interphase inductors in motor drive applications. It is preferred to integrate the interphase inductor with other inductors together to reduce the total system weight. Thus, this chapter also presented a detail analysis on the integration of interphase inductors for three phase dc-ac power converters. All of these analyses were verified by experimental results based on an interleaved two-level VSI demo system.

Chapter 4 Noise Reduction in Three Level Voltage Source Converters

4.1 Introduction

Voltage-source pulse-width modulation (PWM) inverters have made a significant contribution in the achievement of energy conservation as well as in improving system performance and productivity in many applications; among others variable frequency motor drives, uninterruptible power supplies and renewable energy integration. In such systems, certain interface standards must be met including those that govern electromagnetic interference (EMI), power quality, and transient performance. Filters are invariably needed in this case, which can end up representing a significant portion of the total size and cost of the power converters in question.

Compared with two-level voltage source converters, three-level (3L) neutral-point-clamped (NPC) converters can achieve better performance in terms of ripple, harmonics and EMI noise emission [84]. Figure 4-1shows a three-level NPC voltage-source inverter working as a dc-fed motor drive system, which will be studied in this chapter as an example. In three-level voltage source converters, each phase leg have three output voltage levels: $+V_{dc}/2$ (P), 0 (O), $-V_{dc}/2$ (N), there are totally 27 switching states and 18 different output voltage vectors. more output voltage levels means a smaller voltage step which can help to reduce the noise source compared with two-level converters, thus the ripple is smaller for three-level converters and the EMI performance are better. Moreover, there are more available output voltage vectors and even redundant vectors (27 switching states and 18 different output voltage vectors) in three-level converters compared with two-level

converters (8 switching states and 7 different output voltage vectors), which provide more freedom for different optimization goals, such as minimum loss, minimum CM voltage, and minimum harmonic distortion.

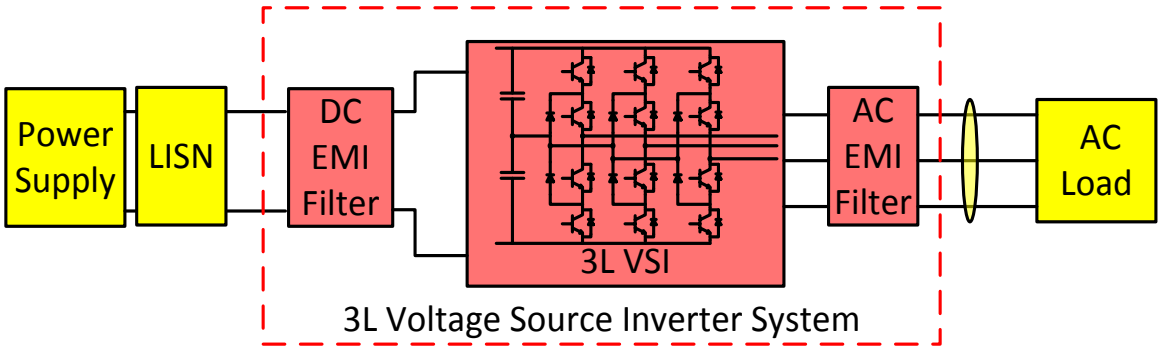


Figure 4-1 Diagram of three-level NPC voltage-source inverter system.

Previous work have presented numerous modulation methods that demonstrated how the additional choices in switching states of the NPC converter intrinsically provide many opportunities for the optimization of a system. The nearest three space vector (NTSV) modulation scheme, for instance, achieves low differential-mode (DM) harmonic distortion, and minimum dc-link ripple current which can help to reduce the size of the boost inductors or load inductors and widely used for three-level converters, this modulation method also provide the freedom for neutral point voltage balancing, which is a very important aspect to maintain the normal working of three-level converters. Similar with two level converters, discontinuous PWM modulation method can also be applied to reduce the switching loss and optimize system efficiency. Since this modulation method also have the potential to reduce the common-mode (CM) voltage generated by the converter, it is also defined as as the common mode reduction (CMR) modulation. To reduce the EMI filter size, especially, the CM filter size for motor drive system, , the additional choices in switching states of the NPC converter can even fully eliminate the CM voltage by proper selection of switching states which is referred as common mode

elimination (CME) technique. Although these modulation schemes have been widely used to reduce the filter size of NPC inverters, so far no detailed evaluation has been presented studying their specific performance regarding EMI mitigation, neutral-point (NP) voltage ripple, and system losses. Addressing this shortcoming, this chapter will first conducts an in-depth analysis of the EMI performance, NP voltage ripple, and system losses of these modulation methods with the detailed comparison results through simulations and experiments in section 4.2. The results show that the CME modulation method can effectively reduce the CM noise emission from the system, however, the performance is highly sensitive to the dead time added in the system, which make this modulation method less practical. To address this problem, section 4.3 will present a detailed analysis on the impact of dead time on system EMI noise emission for CME modulation. Based on the analysis, two methods are proposed to reduce the impact of dead time for CME modulation: dead time compensation and improved CME modulation. All the analyses are experimentally verified through a 2.5kW laboratory prototype. Finally, in order to verify the validation of the proposed methods for high power applications, a 100 kW dc-fed motor drive system with EMI filters for both AC and DC sides was designed, implemented and tested. The design and implantation details were presented along with the full power test results.

4.2 Evaluation of Alternative Modulation Schemes for Three-Level Topology

In 3L-NPC inverters, since each phase-leg has three output voltage levels: $+V_{dc}/2$ (P), 0 (O), $-V_{dc}/2$ (N), there are totally 27 switching states and 18 different output voltage vectors as shown in Figure 4-2.

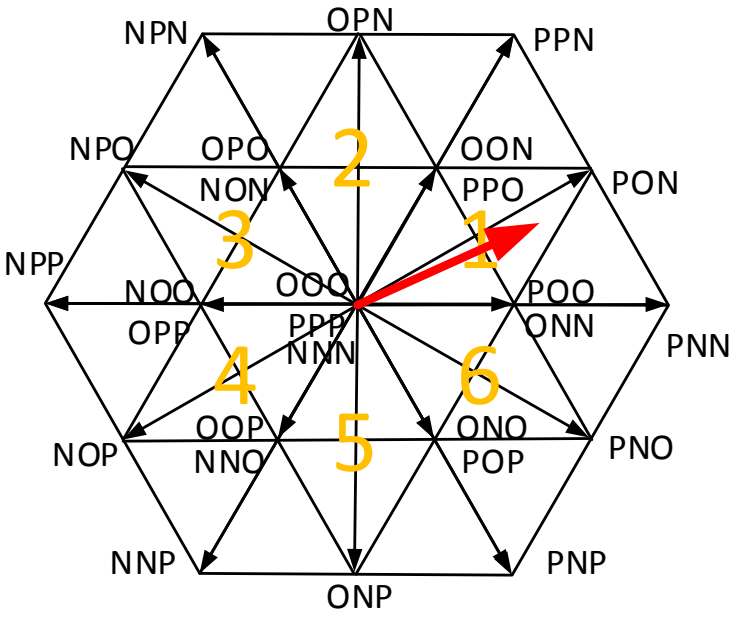


Figure 4-2 Switching states and voltage vectors in 3L topology

Previous work have demonstrated how the additional choices in switching states of the NPC converter intrinsically provide many opportunities for the optimization of a system. The nearest three space vector (NTSV) modulation scheme for instance achieves low differential-mode (DM) harmonic distortion, and minimum dc-link ripple current. Similar with two level converters, discontinuous PWM modulation method can also be applied to reduce the switching loss and optimize system efficiency. Since this modulation method also have the potential to reduce the common-mode (CM) voltage generated by the converter, it is also defined as the common mode reduction (CMR) modulation. To reduce the EMI filter size, especially, the CM filter size for motor drive systems, the additional

choices in switching states of the NPC converter can even fully eliminate the CM voltage by proper selection of switching states which is referred as CM elimination (CME) modulation.

Although these modulation schemes have been widely used to reduce the filter size of NPC inverters, so far no detailed evaluation has been presented studying their specific performance in what regards EMI mitigation, neutral-point (NP) voltage ripple, and system losses. Reference [98] seems to be the only work addressing these topics, where a comparison of CM voltage generation between NTSV and CME modulation was presented; however it limited its analysis to the time domain focusing only on the low frequency range.

Addressing this shortcoming, and based on the three-level NPC inverter system (3L-NPC) shown in Figure 4-1, this section presents a comprehensive evaluation of the NTSV, CMR and CME modulation techniques. Specifically, analyzing the space vector sequences used and the respective dwelling times of these schemes, this section conducts an in-depth analysis of their EMI performance, of their NP voltage ripple, and of their system losses. Simulations results obtained with a detailed switching model developed in SABER, as well as experimental results obtained with a 2.5 kW laboratory prototype are used to verify the theoretical findings of this work.

4.2.1 Implementation of different modulation methods

This section will present how thanks to the many degrees of freedom that the available space vectors provide—especially the redundant space vectors, many different modulation schemes with distinct optimization goals, such as minimum loss, minimum CM voltage,

and minimum harmonic distortion have been developed so far. Specifically the NTSV, CMR and CME modulation schemes will be briefly described in what follows.

A. Neatest Three Space Vectors Modulation

The NTSV modulation scheme uses all 27 switching states available in the 3L-NPC inverter. It is commonly used to achieve minimal harmonic distortion and NP voltage balancing. Under this modulation scheme, the three space vectors that is the closest to the reference vector are used to synthesize the reference voltage vector. For instance, when the reference vector lies in the small triangular region within sector '1' as shown in Fig.2, the nearest three vectors and their respective redundant states are: PON, OON/PPO and POO/ONN as shown in Figure 4-3.

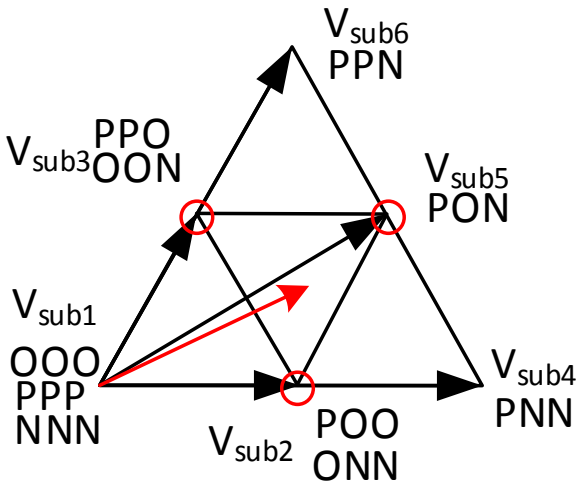


Figure 4-3 The nearest three vectors used in NTSV modulation

The dwelling time of each vector to generate the vector reference are then calculated using (4-1),

$$\begin{aligned} &\vec{V}_{sub2}T_2 + \vec{V}_{sub3}T_3 + \vec{V}_{sub5}T_5 = \vec{V}_{ref}T_s \\ &T_2 + T_3 + T_5 = T_s \end{aligned} \tag{4-1}$$

where V_{sub2} V_{sub3} and V_{sub5} represents the voltage sector POO/ONN, OON/PPO and PON respectively, T_2, T_3 and T_5 correspond to the dwelling time of V_{sub2} V_{sub3} and V_{sub5}, and T_s to the switching period.

This modulation scheme uses both redundant state realizations for each small vector within switching cycles, allowing it to achieve a low harmonic distortion while maintaining the capability to balance the dc bus NP voltage. For example, both POO and ONN state realization are used for small vector V_{sub2} in Figure 4-3. Further, to ensure that each phase-leg commutates only once within a switching cycle, as well as to maintain current symmetry, the space vector sequence and dwelling time distribution shown in Table 4-1 is used when the reference vector lies in sector 1 and sub-sector 3.

Table 4-1 Vector sequence and dwell time for NTSV modulation

Dwell Time	$T_2/4$	$T_3/2$	$T_5/2$	$T_2/2$	$T_5/2$	$T_3/2$	$T_2/4$
Phase A	O	O	P	P	P	O	O
Phase B	N	O	O	O	O	O	N
Phase C	N	N	N	O	N	N	N

From here the switching sequence for other regions can be easily determined. Since all small vector realizations are used in NTSV on a switching cycle basis, this modulation scheme has the capability to regulate the NP voltage by adjusting the conduction time ratio between redundant space vectors. Additionally, since the sequence used is split into seven segments to synthesize the reference voltage vector, the switching ripple generated is also small. The main drawback of this scheme is the relatively high CM voltage generated by the converter.

B. Common-Mode Reduction Modulation

Common Mode (CM) voltage is the sum of the three-phase voltages produced by a power converter measured with respect to a common point, usually the ground. The

generation of CM voltage is an inherent problem of converters, as it is a by-product of the method by which ac voltages are synthesized from a dc voltage source, i.e., pulse-width modulation.

In the case of 3L-NPC inverters, it is clear that the redundant state realizations of small vectors produce different CM voltage. For example, for sub-vector V_{sub2}, POO generates a CM voltage equal to $+V_{dc}/6$, while its counterpart ONN generates a CM voltage equal to $-V_{dc}/3$. Similarly all middle vectors generate zero CM voltage, large vectors generate a CM voltage equal to $\pm V_{dc}/3$, and the zero vectors generate a CM voltage equal to $\pm V_{dc}$ and zero. Consequently, to reduce the CM voltage generated by the converter, one can limit the switching states used in the modulation scheme to employ the ones that generate a CM voltage equal to or lesser than $\pm V_{dc}/6$. This specific scheme is known as CMR modulation.

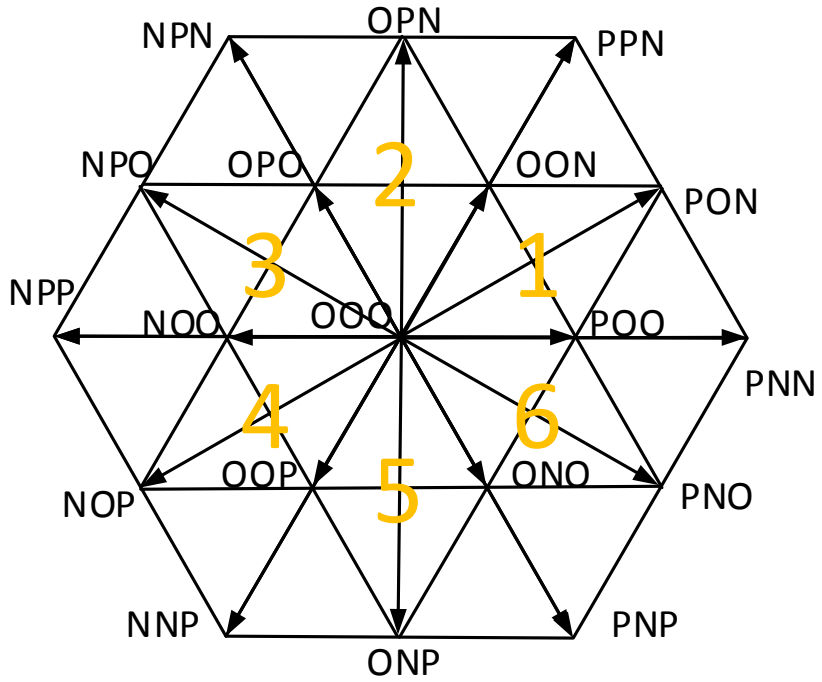


Figure 4-4 Voltage vectors of CMR modulation scheme

The restrained set of space vectors available are displayed in Figure 4-4, and the space vector sequence when the voltage reference voltage lies in sector 1 and sub sector 3 is

shown in Table 4-2. The dwelling time calculation for the space vectors used is the same as with NTSV, and can be determined using (1).

Table 4-2 Vector sequence and dwell time for CMR modulation

Dwell time	$T_5/4$	T_2	$T_5/2$	T_3	$T_5/4$
Phase A	P	O	P	P	P
Phase B	O	O	O	O	O
Phase C	N	N	N	O	N

As seen, this modulation method can effectively limit the CM voltage produced by the converter by avoiding the use of vectors with a CM voltage higher than $\pm V_{dc}/6$. The apparent downside of this approach, as shown in Fig. 3, is that only one switching state realization is available for the small vectors, with which CMR modulation forfeits the freedom to regulate the dc bus NP voltage. On the other hand, since in every sector there is always one phase-leg that does not commutate within switching cycles, the switching losses generated by this modulation scheme are significantly reduced with respect to NTSV. If the optimal design target is to minimize the switching loss, one can also select the vectors to make sure no switching happens on the phase leg that conduct the highest current, this modulation is the minimum loss modulation, however, since in this modulation, the CM noise is not optimized, it will have relatively high CM noise emission, thus it is not discussed in the work.

C. Common-Mode Elimination Modulation

In 3L-NPC inverters, it is also possible to completely eliminate the CM voltage produced by the converter by further limiting the set of available space vectors to conduct the high frequency synthesis of the voltage reference vector. This is known as CME modulation. The switching states used in this scheme are shown in Figure 4-5, where it is

apparent that only the vectors that generate zero CM voltage are used, that is, the middle vectors.

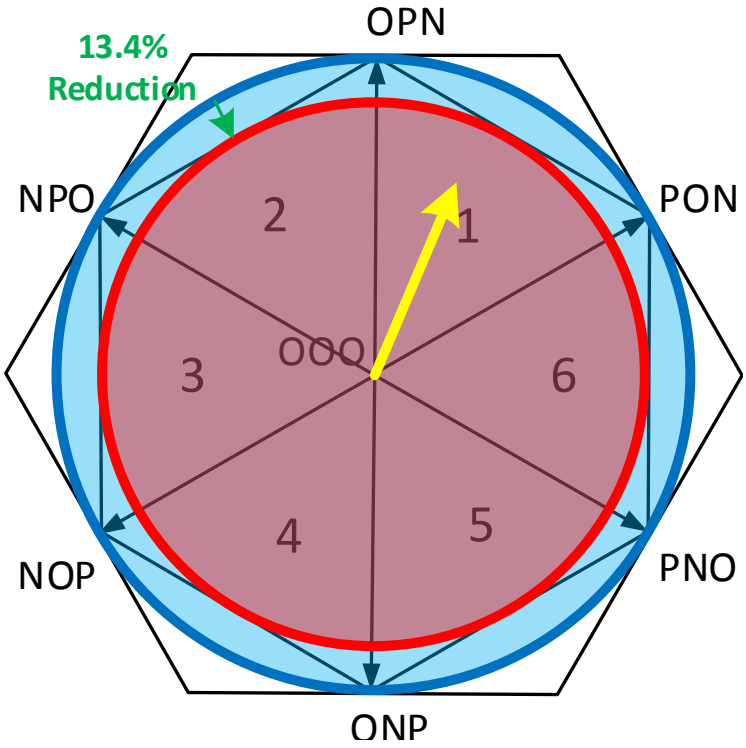


Figure 4-5 Voltage vectors of CME modulation scheme

As observed, the remaining space vector diagram is similar to those of two-level voltage-source converters, where one fundamental period can be divided into six regions as illustrated, and where the dwelling time calculation when the reference voltage lies in region 1 is given by (4-2),

$$\begin{aligned} T_1 &= \left(\frac{2}{\sqrt{3}} m\cos\beta + \frac{2}{3} m\sin\beta \right) \times T_s \\ T_2 &= \frac{4}{3} m\sin\beta \times T_s \\ T_0 &= T_s - T_1 - T_2 \end{aligned} \tag{4-2}$$

and where T_0, T_1 and T_2 represent the dwelling times of vectors OOO, PON and OPN respectively, β is the reference vector angle, and m is the modulation index.

Table 4-3 Vector sequence and dwell time for CME modulation

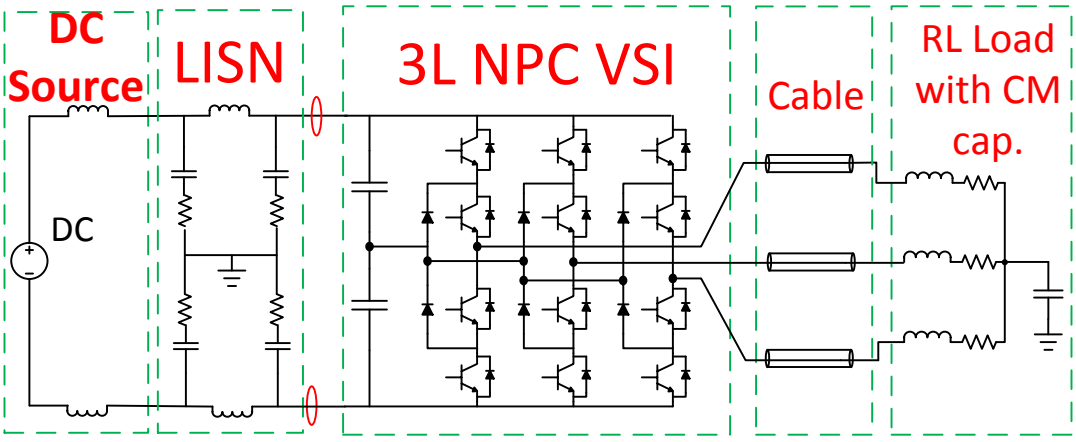
Dwell time	$T_0/2$	T_1	T_2	$T_0/2$
Phase A	O	P	O	O
Phase B	O	O	P	O
Phase C	O	N	N	O

Similarly to the previous modulation schemes, in order to ensure that each phase-leg commutates only once during a switching cycle, the vector sequence and dwelling time distribution shown in Table 4-3 can be used for the case when the reference voltage vector lies in sector 1. Other sequences for the remaining sectors can be easily derived. By observing this sequence, it can be noticed that there are always two phases switching at the same time, and that the two switching phases are always with voltage of opposite polarity. In consequence, CME modulation can in principle avoid the generation of CM voltage and help reduce the size of the converter CM filter significantly. The penalty of this approach, as observed in Figure 4-5, is a 13.4 % smaller voltage utilization ratio and the loss of the converter capability to balance its NP voltage.

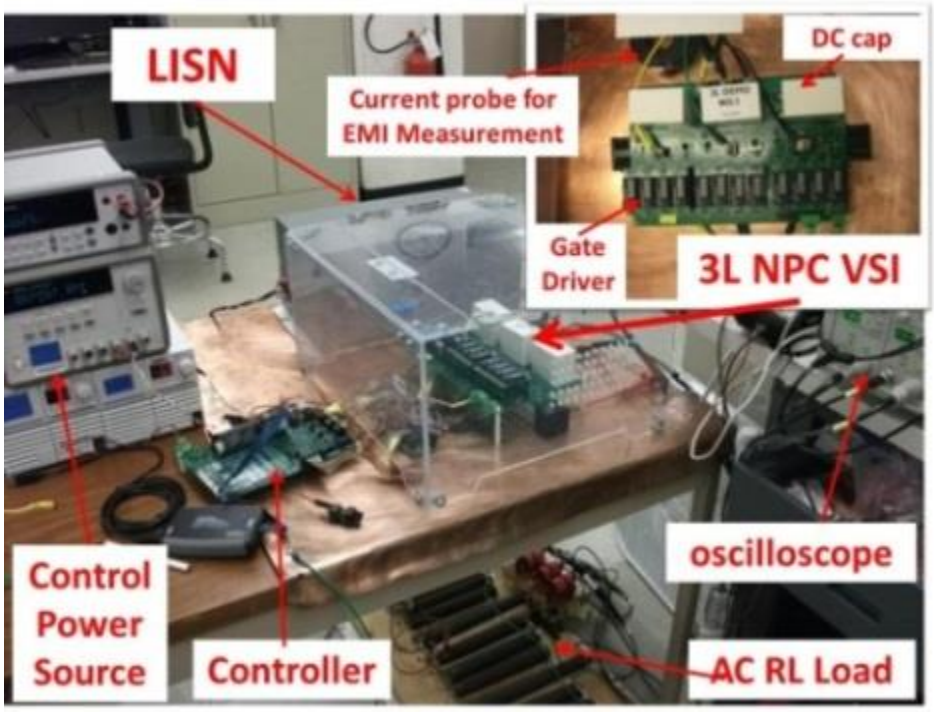
4.2.2 EMI Performance Comparison

To compare the performance of the three modulation scheme under study, both simulation and experimental results were obtained on a 3L-NPC VSI system as the one shown in Figure 4-1. A detailed switching model was developed in SABER for this purpose. The experimental setup employed is shown in Figure 4-6, where the AC load was replaced by an RL load with a grounding capacitor to emulate the CM coupling to ground

typical of industrial applications. The converter power rating is 2.5 kW, the switching frequency 30 kHz (f_s), and its fundamental frequency 200 Hz (f_1).



(a) Experimental system structure.



(b) Experimental system setup

Figure 4-6 Schematic and setup of the experimental system

CM voltage is a key contributor to the generation of bearing currents in electrical motors and of conducted EMI in electrical systems, for which EMI filters represent an effective means of mitigation. However, to attain sufficient attenuation, CM filters are

oftentimes of large size representing a significant part of the total physical system and ultimately of its cost too. To reduce the filter size, a preferred approach has then been to use advanced filter configurations while using most judicious design methods to avoid the over design of the filters.

An alternative, as discussed so far, is to reduce the CM voltage produced by the converter, which in a more direct way simply reduces the filtering needs of the system in order to reduce the actual size of the filters. This is accomplished by using optimized PWM schemes that selectively apply electrical states of the converter with reduced CM voltage. Among the modulation techniques under study, NTSV produces the highest CM voltage since all available switching states are used to synthesize the reference voltage vector—without pursuing any CM voltage reduction; hence the range of discrete CM voltage values is relatively large. For modulation indexes larger than 0.5, the CM voltage varies between $\pm V_{dc}/3$ as shown in Figure 4-7. In CMR modulation, since the switching states that generate CM voltage equal to $\pm V_{dc}/3$ are not used, the CM voltage range is constrained to $\pm V_{dc}/6$. This represents a significant reduction that can aid in the EMI filter design minimization.

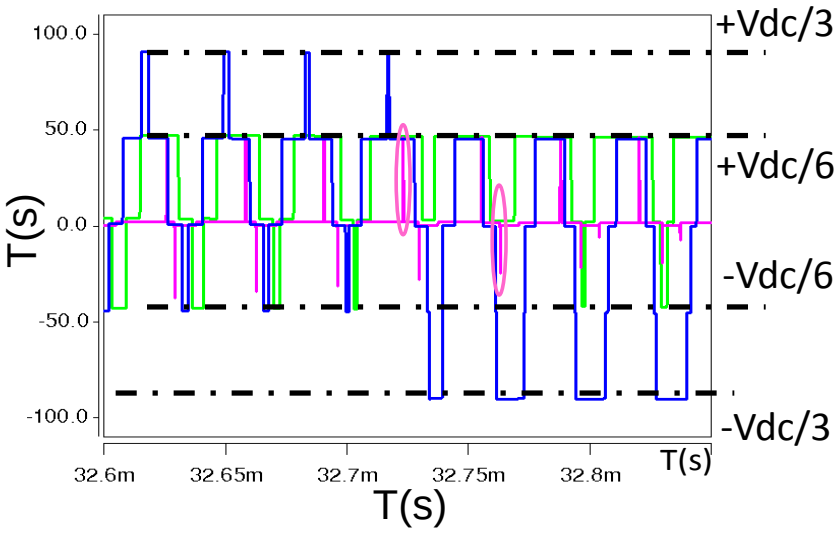
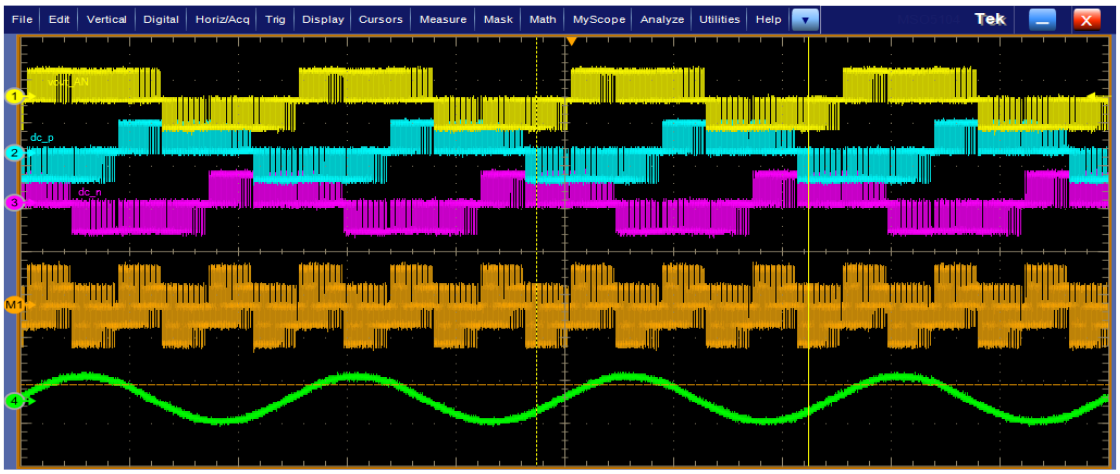


Figure 4-7 Simulated CM voltage for different modulation schemes

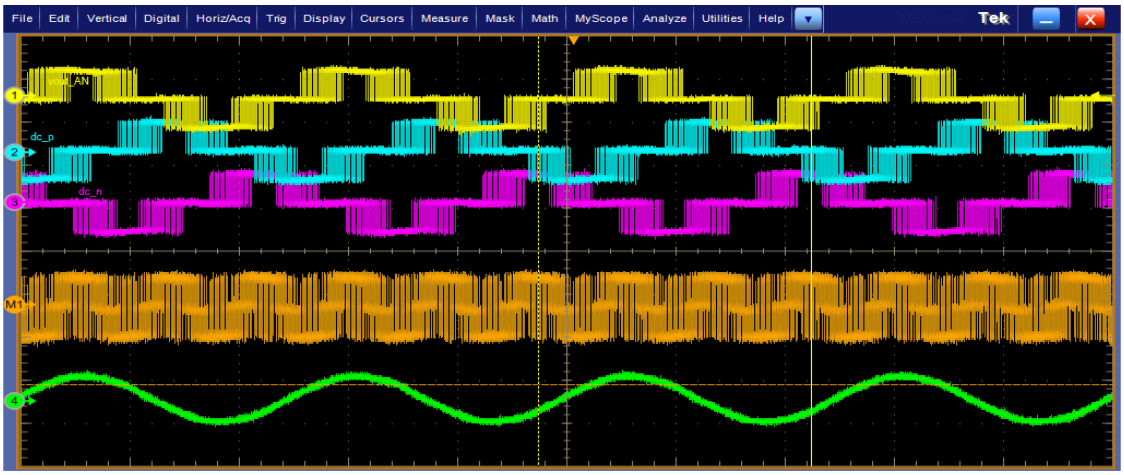
(NTSV: blue, CMR: green, and CME: purple)

Lastly, CME modulation is the most aggressive in these terms as it only employs switching states with zero CM, theoretically eliminating CM voltage. The effectiveness of this modulation scheme however is severely limited and dependent on the amount of dead-time (DT) needed by the converter gating signals. As a result, the CM voltage is not eliminated but some peaks will remain as shown in Figure 4-7. Nonetheless, the CM voltage produced is still smaller than that produced by CME and CMR methods for relatively small DT.

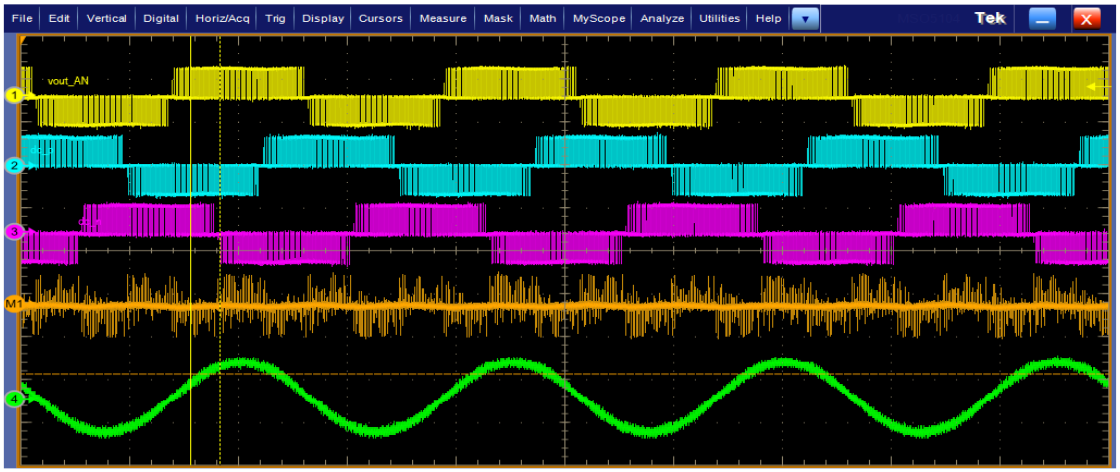
The time-domain test results of the experimental prototype are shown in Figure 4-8. From Figure 4-8 (a-b) it is apparent that with CMR modulation the effective span of the converter CM voltage is limited compared to NTSV modulation. Furthermore, CME modulation shows how an additional CM voltage reduction can be achieved with respect to CMR and NTSV, but only when small DT periods are used. This is depicted in Figure 4-8 (c), which shows how in this case only some peaks are generated by the converter. However, when larger DT periods are used, the CM voltage produced by this technique increases significantly as shown in Figure 4-8(d). Special compensation methods can be used to correct this unwanted behavior.



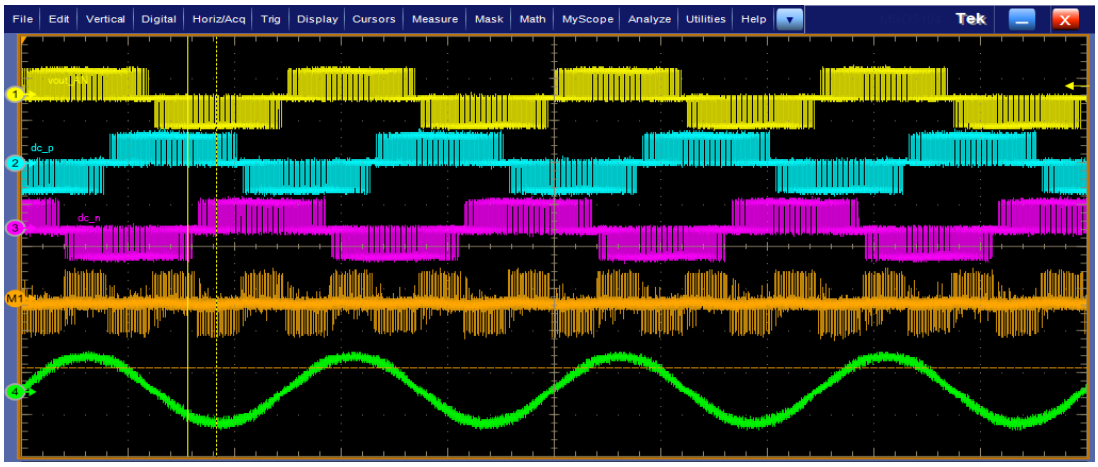
(a) **NTSV Modulation with 0.5 μs dead-time.**



(b) **CMR Modulation with 0.5 μs dead-time.**



(c) CME modulation with 0.5 μs dead-time.

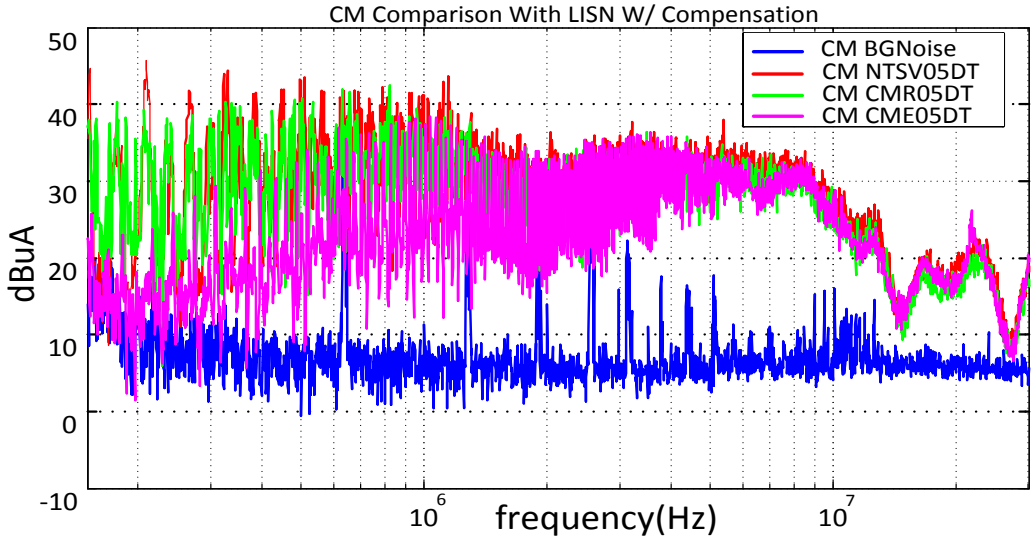


(d) **CME modulation with 1 μs dead-time**

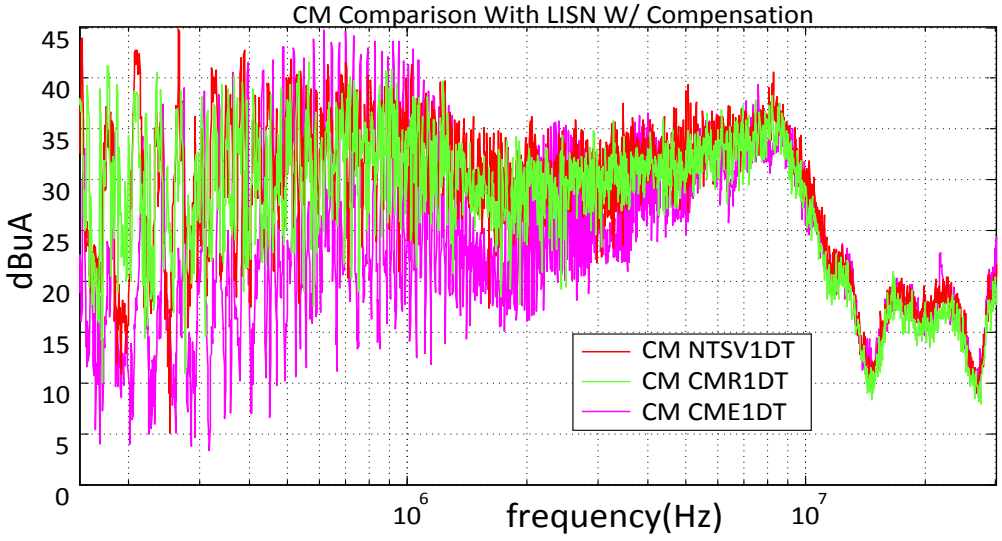
Figure 4-8 Experimental results depicting CM voltage generation.

(Van: yellow, Vbn: cyan, Vcn: purple, Vcm orange, and Ia: green.)

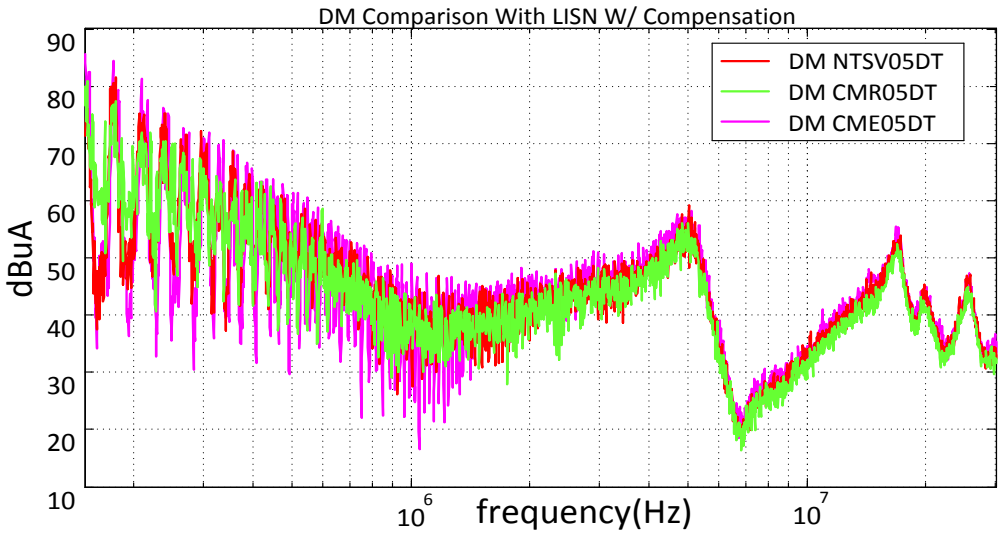
Since EMI standards delimit the magnitude of the CM voltage frequency components, frequency domain analysis is more suitable to evaluate the EMI performance and filtering requirements of the different modulation schemes. Of special interest are the current measurements conducted with the 3L-NPC inverter experimental prototype. Figure 4-9 shows the EMI test results of the inverter CM and DM output currents from 150 kHz to 30 MHz, using a test setup as specified by the DO160E standard.



(a) **CM noise comparison with 0.5 μs dead-time.**



(b) **CM noise comparison with 1 μs dead-time.**



(c) DM noise comparison with 0.5 μs dead-time.

Figure 4-9 CM and DM noise measurements with different modulation methods

(NTSV: red, CMR: green, and CME: pink)

Figure 4-9(a) demonstrates how CME modulation can effectively reduce CM noise in the low frequency range (150 kHz~2MHz) when the DT used in the converter is small (0.5 μs). In the high frequency range (> 2 MHz), the impact of DT is in any case negligible since the EMI content in this range is primarily determined by the switching behavior of the switching devices. Figure 4-9(b) on the other hand illustrates how for larger DT values, 1 μs in this case, the CM voltage cancellation effect is not effective and the resultant CM noise under CME modulation increases beyond even the noise produced by NTSV. The results achieved by CMR modulation are more systematic when compared to CME, as its CM noise is around 6 dB lower than NTSV throughout the frequency spectrum regardless of the DT value employed. In terms of DM noise, CME modulation uses the fewest voltage vectors, which consequently translates into the highest DM noise among the three modulation schemes. CMR and NTSV on the other had featured a comparable DM noise composition, which is similar to the differences of discontinuous and continuous PWM schemes in two-level voltage-source converters.

4.2.3 Neutral-Point Voltage Ripple Comparison

In CMR and CME modulation, since a subgroup or none of the small vectors are used in the voltage reference synthesis, these schemes have no capability to compensate the NP voltage ripple. Accordingly, the DC bus capacitance needs to be increased in order to limit the NP voltage ripple, which invariably increases the size of this capacitor bank. From a power density standpoint, there is hence a design tradeoff between the EMI filter and the DC bus capacitance.

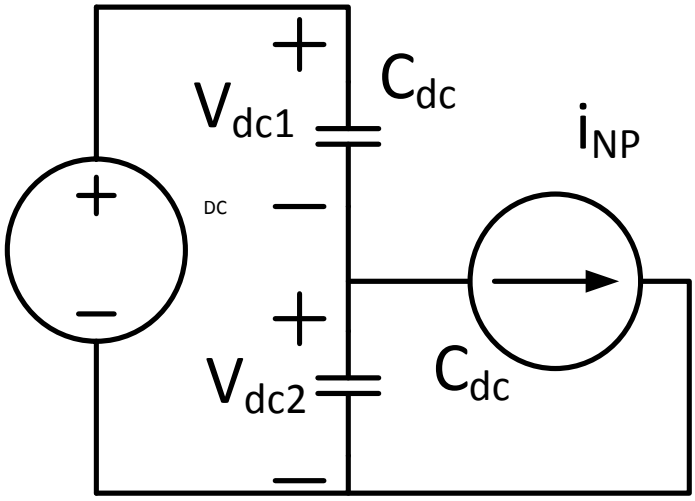


Figure 4-10 Equivalent circuit for neutral-point voltage ripple

Considering an NPC converter phase-leg, it is clear that the NP voltage can only change when there is current flowing through it; thus the equivalent circuit shown in Figure 4-10 can be used to analyze the NP voltage ripple, where C_{dc} corresponds to the dc bus capacitance and $i_{NP\text{-}k}$ (k=A,B,C) to one of the phase-leg currents flowing through the neutral point. The latter are determined by the active space vector realization at any given time. When the phase-leg output voltage state is P or N, I_{np_k}=0, and when the output state is O, $I_{np\_k} = I_{out\_k}$.

In space vector modulation several voltage vectors are activated within any given switching cycle depending on the specific vector sequence in use. For this reason it is

reasonable to assume that the phase current remains constant during a switching period when operating under high sampling and switching frequencies. Under this assumption the NP voltage changes within the n^{th} switching period can be calculated as follows:

$$\Delta V(nT_s) = \frac{\sum_m \left(T_m \sum_{k=A,B,C} i_{np\_k} \right)}{2C_{dc}} \tag{4-3}$$

where m represents the voltage vector and T_m represents the vector dwelling time. Notice that $\sum_m T_m = T_s$ Based on the NP voltage changes within a switching cycle, the NP voltage ripple can be calculated as:

$$V_{NP\_ripple} = \max\left(\int_t \Delta V(nT_s)dt \right) - \min\left(\int_t \Delta V(nT_s)dt \right) \tag{4-4}$$

As observed, the NP voltage ripple is determined by both the active switching states of the converter and by its given operating condition, which includes modulation index, power factor, and dc bus capacitance. Figure 4-11 depicts the relationships between NP voltage ripple and the converter modulation index and power factor under the three modulation schemes in consideration.

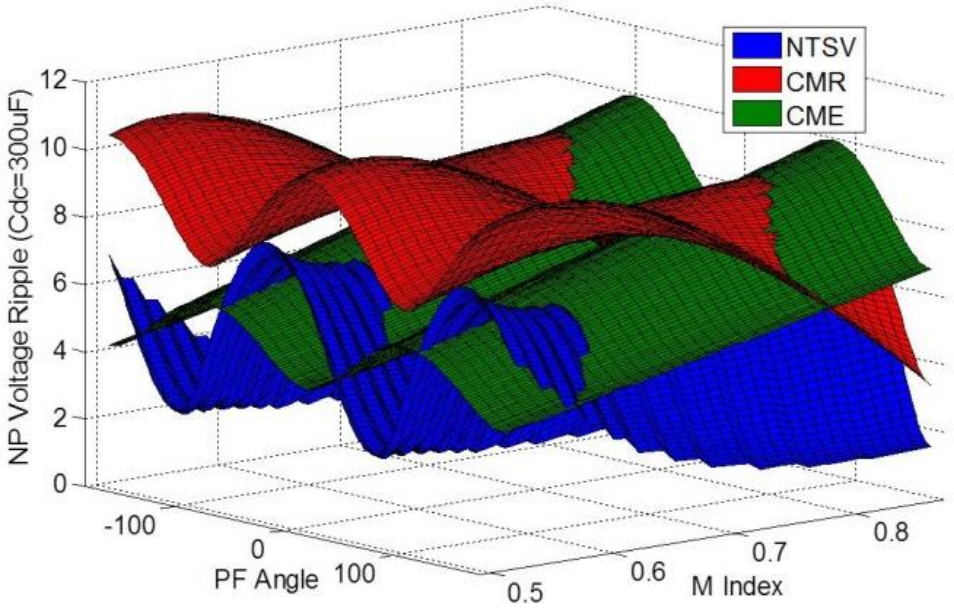
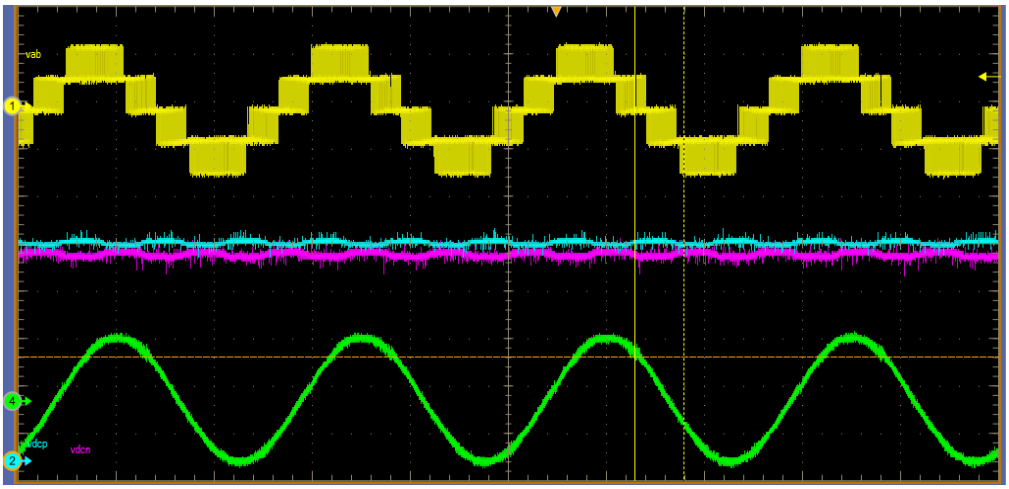
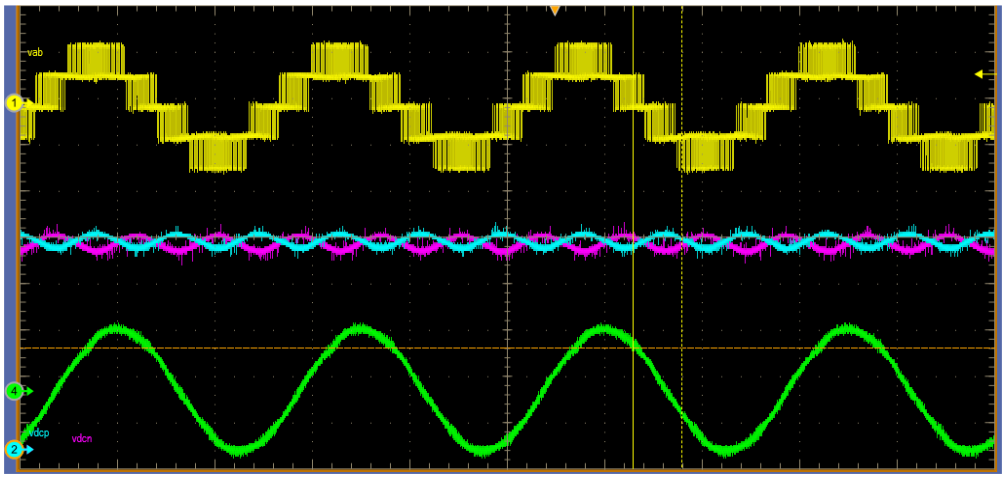


Figure 4-11 Neutral-point voltage ripple comparison of different modulation schemes

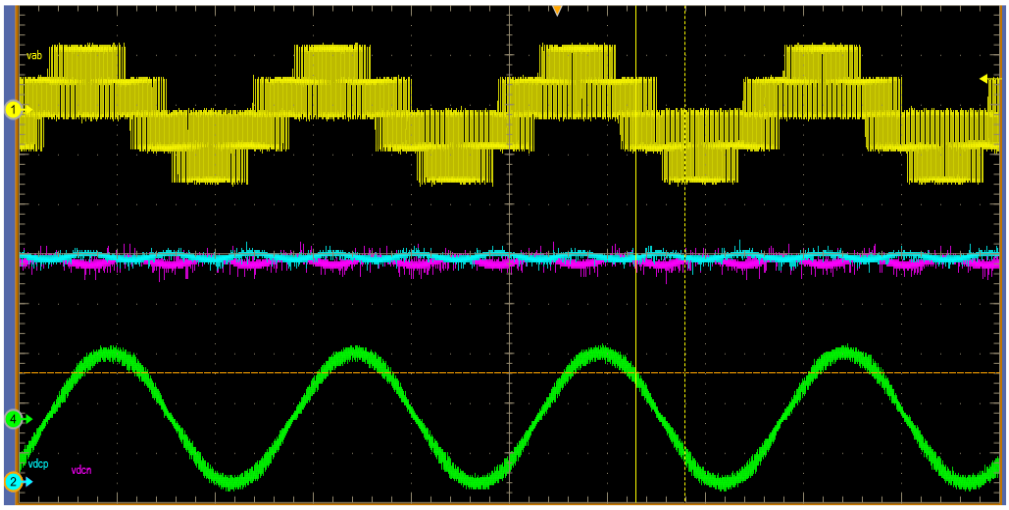
From this plot it is clear that the CMR scheme is always inferior in terms of NP voltage ripple with respect to the NTSV scheme, while in the case of CME modulation the scheme with superior performance truly depends on specific working conditions. For instance, for low modulation index and near zero power factor angle CME featured the smallest NP voltage ripple. On the contrary, for high modulation index and near 90° power factor angle CME has the largest ripple. In order to verify the previous analysis, experimental results are presented in Figure 4-12 evaluating the three modulation schemes in question. The specific operating point used for this test is M = 0.7 and PF Angle = 10 °.



(a) NTSV modulation scheme.



(b) CMR modulation scheme.



(c) CME modulation scheme.

Figure 4-12 Experimental results of NP voltage ripple

(Vab: yellow, Vpo: blue, Von: purple, and Ia: green.)

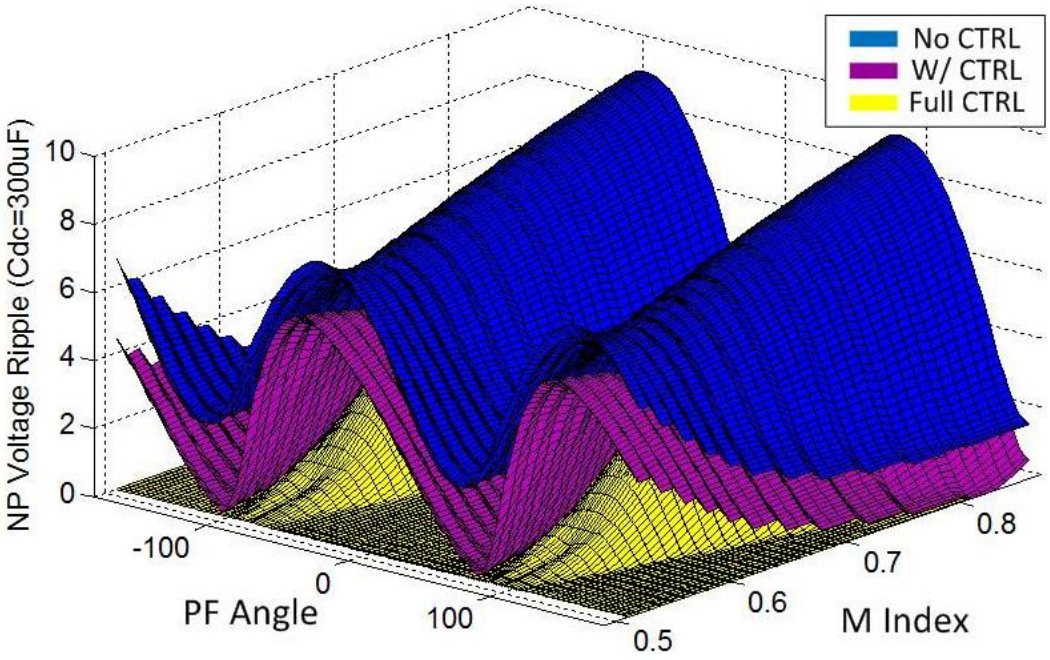


Figure 4-13 NP voltage ripple comparison with different compensation methods (without NP voltage control: blue; with NP voltage control: purple; with full NP voltage control: yellow)

These plots show that the CMR scheme suffers from the largest NP voltage ripple and that the NTSV scheme exhibits the smallest one. The latter was expected since NTSV modulation can make use of all redundant vectors to help aid in the NP voltage balancing task. However, even under this modulation scheme the NP voltage ripple is not fully controlled since in some of the sub-sectors only three out of the four state realizations of the two small vectors are used. To achieve full control of the NP voltage ripple all four state realizations of the small vectors should be used. This is verified in Figure 4-13, which illustrates how the NP voltage ripple can be fully eliminated within a limited region where full control can be attained in the case of NTSV modulation. As expected neither CMR nor CME modulation can achieve this operating condition.

4.2.4 Semiconductor Loss Comparison

In power converter design, the semiconductor losses is also an important design aspect, since it directly determined the efficiency of the system and the weight of the heat sinks. Semiconductor losses include conduction and switching losses. The semiconductor calculation methods has been analyzed in section 3.4. The loss calculation method in three level topologies is similar with the method used in two-level topologies. To calculate the conduction losses both IGBT and diode can be modelled as a voltage source in series with a resistor. Accordingly, while the devices conduct their losses can be calculated as follows:

$$P_{cond} = V_{on} \times i \ + i^2 \times R_{on} \tag{4-5}$$

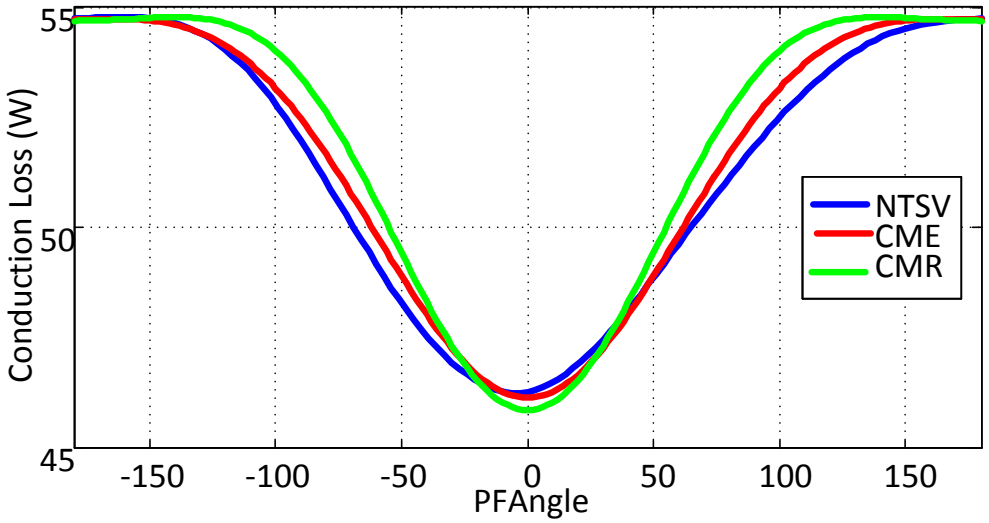
Where V_{on} and R_{on} represent the voltage drop and the on-state resistance of the devices. These parameters can be easily extracted from the device forward characteristics in the datasheet.

Switching losses are generated by the dissipation of energy in the device during the momentary voltage and current overlap across its terminals—the commutation period. Typically switching energy (E_{ss_rated}) is given in the device datasheet for a given voltage (V_{rated}) and current (I_{rated}), from where linear interpolation can be used to calculate the switching energy (E_{SS}) under a desired operating point ($V_{SS,}$ I_{SS}). The total switching losses ($P_{switching}$) within one fundamental period can then be calculated as shown in (4-6), where f_1 and f_{sw} correspond to the fundamental and switching frequency respectively.

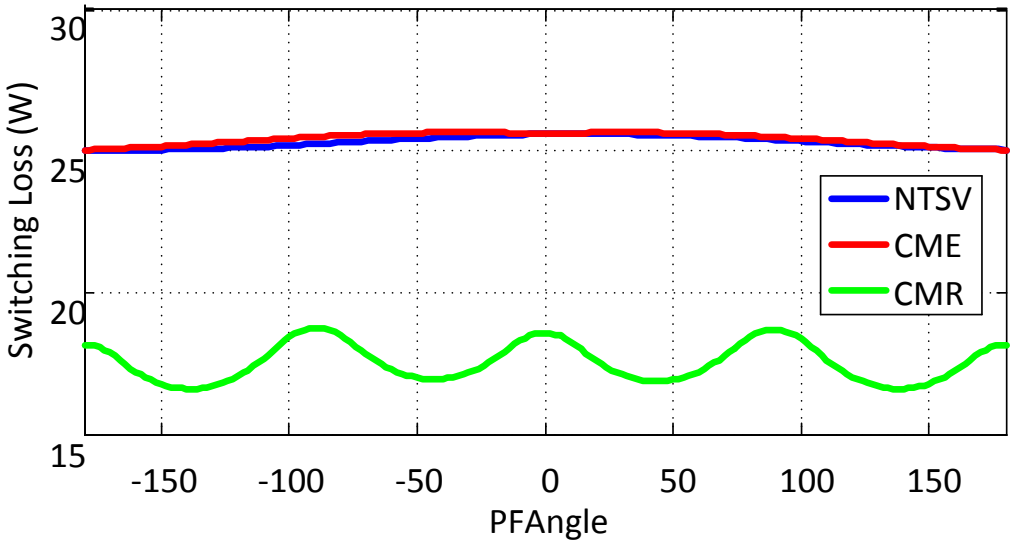
$$P_{switching} = f_1 \times \sum_{k=1}^{f_{sw}/f_1} E_{ss\_rated} \frac{V_{SS\_k} I_{SS\_k}}{V_{rated} I_{rated}} \tag{4-6}$$

For high carrier ratios, it is normally sufficient to assume that the line current is constant during the switching cycle, which simplifies the use of (4-6).

To evaluate the three modulation schemes in question, their respective switching and conduction losses were calculated as described above. Figure 4-14 shows the results obtained where the respective power losses are plotted versus the power factor angle of the converter. This is necessary since under different voltage and current phase-shift the current flow in the converter will alter its path, with which both conduction and switching losses change.



(a) Conduction losses



(b) Switching losses

Figure 4-14 Evaluation of conduction and switching losses under different modulation schemes.

As seen in this figure, all three modulation methods feature very similar conduction losses. This due to the fact that the dwelling times of space vectors are determined by the same voltage reference vector in the modulation process. Switching losses on the other hand exhibit some difference between the three modulation schemes. Specifically, since CMR modulation only switches two phase-legs on a switching cycle basis, its losses are approximately 30 % lower than those of the NTSV and CME modulations schemes. The latter two methods have very similar losses as they both feature the same number of commutations per switching cycle.

4.2.5 Summary and Discussion

This section presented a detailed evaluation of the NTSV, CMR and CME modulation schemes for 3L-NPC inverters, addressing their EMI performance, NP voltage ripple, and switching and conduction losses. Both simulation and experimental results were used to study EMI under these schemes in both time and frequency domains, showing that CMR modulation can help reduce both DM and CM noise in the EMI range when compared to NTSV modulation, and that CME modulation increases DM noise but can help reduce CM noise significantly when using relatively small dead-time in the gate-driving of devices. The latter point revealed the strong dependence on dead-time of the CME modulation scheme, which saw its effectiveness disappear with increasing dead-time periods, to the point where it significantly worsened the converter CM noise, even beyond the NTSV modulation scheme. To make this modulation method more practical, the impact of DT on system CM EMI noise emission is analyzed and will be presented in the next section with improving methods proposed and verified.

The impact on NP voltage ripple was also analyzed in detail using an equivalent circuit and the calculation method are also presented. The results obtained showed the intrinsic relationship between the NP voltage ripple and the converter operating condition; namely modulation index and power factor. In relative terms, it was shown that NTSV modulation has always a lower ripple than the CMR scheme, but that its comparison to CME modulation depended on the specific operating point.

Lastly, in what regards loss generation, all three modulation schemes were shown to feature similar conduction losses, but the CMR modulation scheme attained a 30 % switching loss reduction with respect to NTSV and CME. This is due to the discontinuous switching pattern. If the optimal design target is to minimize the switching loss, one can also select the vectors to make sure no switching happens on the phase leg that conduct the highest current, this modulation is the minimum loss modulation, however, since in this modulation, the CM noise is not optimized, it will have relatively high CM noise emission, thus it is not discussed in the work.

4.3 Impact of Dead Time on CME Modulation

Considering the vector sequence used for CME modulation, it can be observed that there are always two phases that commutate at the same time, and also that their respective voltages have opposite polarity. This is precisely what enables CME modulation, theoretically at least, to generate zero CM voltage. Although this feature could greatly impact the size of EMI filters, it comes at the cost of a smaller voltage utilization ratio and the loss of the capability to balance the NP voltage of the converter. Furthermore, for CME to work properly, ideal commutations are necessary to ensure that the converter phase-legs

indeed switch simultaneously. This explains why under larger DT periods CME becomes less and less effective and less practical as a modulation technique.

Voltage-source PWM inverters have made a significant contribution in energy conservation as well improving system performance and productivity in many applications, such as variable frequency motor drives, uninterruptible power supplies, and renewable energy systems. In such systems, certain interface standards must be met which include those that govern the electromagnetic interference (EMI), power quality, and transient performance. Filters are hence inevitably required in these systems representing a big portion of the size and cost of PWM inverters.

Reference [97] specifically proposed a modulation method that can theoretically eliminate the CM voltage; namely the common-mode elimination (CME) modulation. Its practical implementation and CM voltage reduction however are severely limited by the dead-time (DT) period needed to ensure the safe switching of complementary IGBTs within phase-legs. Additionally, this technique suffers from a 15 % reduction in voltage utilization, and the loss of neutral-point (NP) voltage balancing capability, making it overall less attractive for the applications at hand.

So far, very few initiatives have been conducted or reported to determine the impact of DT on CME modulation. Only a brief compensation method was proposed, focusing on time domain aspects of the technique, and consequently not exploring the impact on the EMI frequency range. Addressing this problem, but focused on a 3L-NPC inverter system as that shown in Fig. 1, this section proposes an improved CME modulation method with DT compensation and performs the detailed analysis of the impact of DT on the converter EMI performance under this modulation scheme. Both time domain and frequency domain

simulations are presented to verify the study, and experimental results conducted with a 2.5 kW 3L-NPC inverter prototype are used to validate the theoretical findings.

4.3.1 Dead Time in Power Converters

Since semiconductor devices are not ideal switches, switching cannot happen instantaneously; hence DT is necessary to avoid shoot-through faults. Just like in two-level converters, DT introduces a volt-second unbalance in the voltage waveforms that induces current distortion in three-level converters. For 3L-NPC inverters however, the effect is slightly more involved as explained in what follows.

Considering the 3L-NPC phase-leg in Figure 4-15, and the output voltage transition O→P, where the gate signals for the four switches are respectively 0110 (O) and 1100 (P). Figure 4-15(a) and (c) show these two voltage-state conditions that do not depend on the current direction. However, it is not safe for power converters to make the phase leg transiting from 0110 (O) directly to 1100 (P), since the device is not ideal, it need certain time to get to completely turn-on and turn-off. If the phase leg transit from 0110 (O) directly to 1100 (P), it is possible that both S1 and S3 are ON, then there will be a short circuit for the top capacitor and create a shoot-through error which will damage the device. In order to avoid this error, S1 need to be turned off completely before S3 turn on. This is implemented in the modulation stage where a small delay time is added between S1 turning on and S3 turning off. This delay time is defined as the dead time (DT) in the system. The duration of the dead time is related with the switching speed and delay characteristics of the power semiconductor, it may varies from several nanoseconds for low power application to tens of microseconds for high power applications.

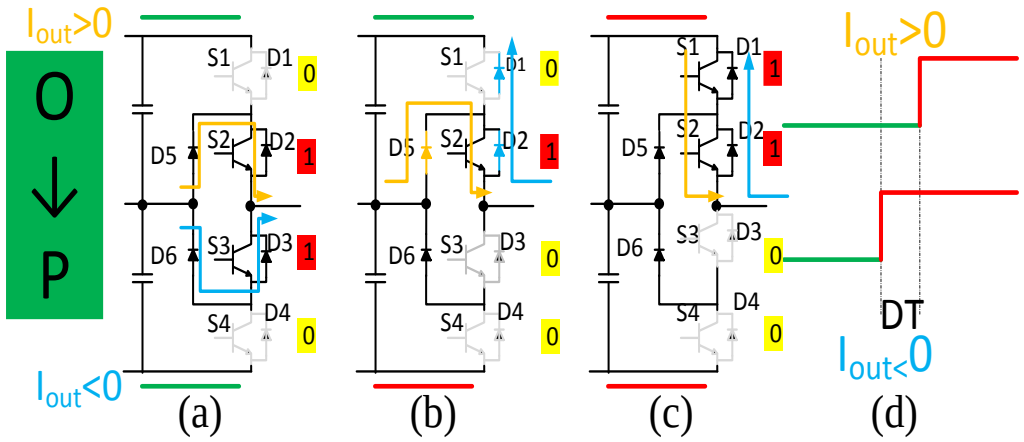


Figure 4-15 Phase leg status during O→P transition

(a) steady state V_{out}=O, (b) during dead time, (c) steady state V_{out}=P, (d) output voltage waveform with different current direction (I_{out}>0:orange, I_{out}<0:blue).

During the DT instant however, when switch S3 remains open before S1 is closed, there is a mid-state condition shown in Figure 4-15(b), where the voltage polarity does depend on the current direction. Specifically, if the current flows out of the converter (Iout>0) during this period, the output voltage is O, and if it flows into the converter (I_{out}<0) the output voltage is P. This is summarized in Figure 4-15(d), showing that the output voltage transition and its instantaneous value depends on the output current direction.

4.3.2 Impact of Dead Time on CM Voltage

In what regards CME modulation, this technique requires that two phases switch simultaneously and in opposite voltage direction at every voltage vector transition in order to maintain zero CM voltage. The ability to accomplish this precise timing in the switching action is hence highly dependent on DT and on the current direction of the two phases. This is illustrated in Figure 4-16 where phases A and C are shown to receive simultaneous gate commands.

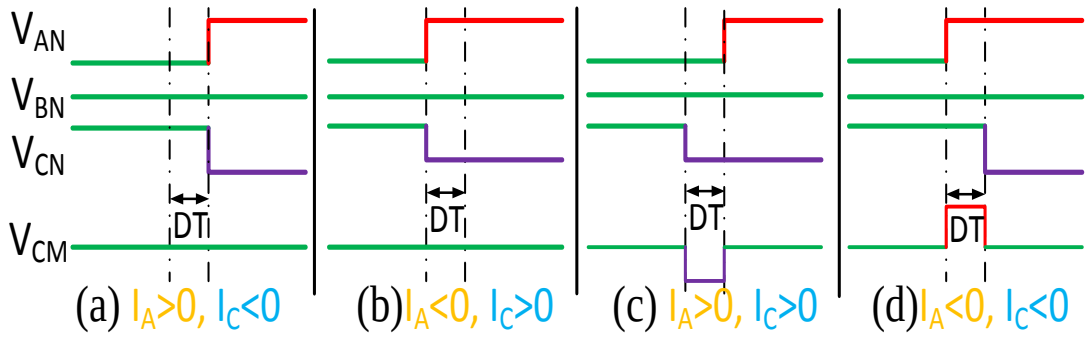


Figure 4-16 Impact of DT on CM voltage generation.

It is clear from this figure that when the two phases have different current direction the effect of DT on each phase is identical, and the resulting CM voltage is zero. But, when the two phases have the same current direction, a notch appears in the converter CM voltage with a pulse width equal to DT and a polarity opposite to that of the current. In CME modulation, since $i_A + i_B + i_C = 0$, two phases will always have different current direction while one will have the same current direction. In consequence, the converter CM voltage will generate a single pulse per switching cycle with a duration of DT seconds, with its relative position determined by the modulation index and the current direction itself. The latter in turn depends on the relative phase between the converter ac voltages and currents.

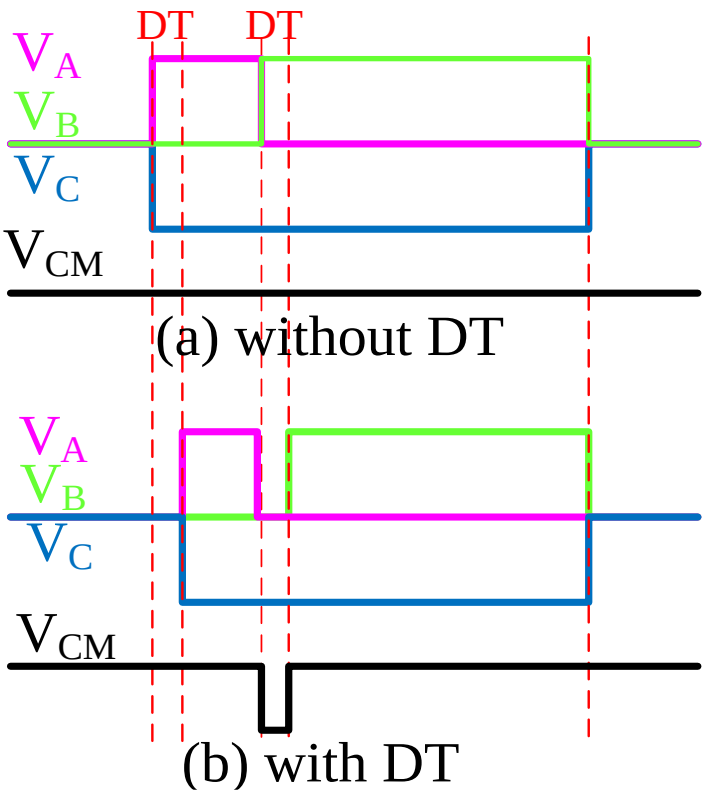


Figure 4-17 Impact of DT on CM voltage during a switching cycle with CME modulation.

Specifically, the polarity of the CM pulse during the switching cycle will depend on the two phases with the same current direction as shown in Figure 4-17(b). From the above, it is clear that the frequency spectrum of the resultant CM current will have switching frequency components, and that their magnitude will depend on the ratio between DT and the switching period. Furthermore, their magnitude will also depend on the phase angle between the converter voltage and current, that is, the converter power factor. Consequently, the CM voltage waveform can be effectively predicted enabling its post-processing using FFT to calculate analytically the impact of DT on the converter CM current spectrum.

4.3.3 Experimental Verification

An experimental verification was carried on the 2.5kW laboratory prototype as shown in the previous section, the time domain results of CME modulation with 0.5μs and 1μs is shown in section 4.2. Figure 4-18 shows the zoomed-in results to illustrate how with basic CME modulation the converter CM voltage consists as predicted of a single pulse per switching cycle with a pulse width equal to the DT period used.

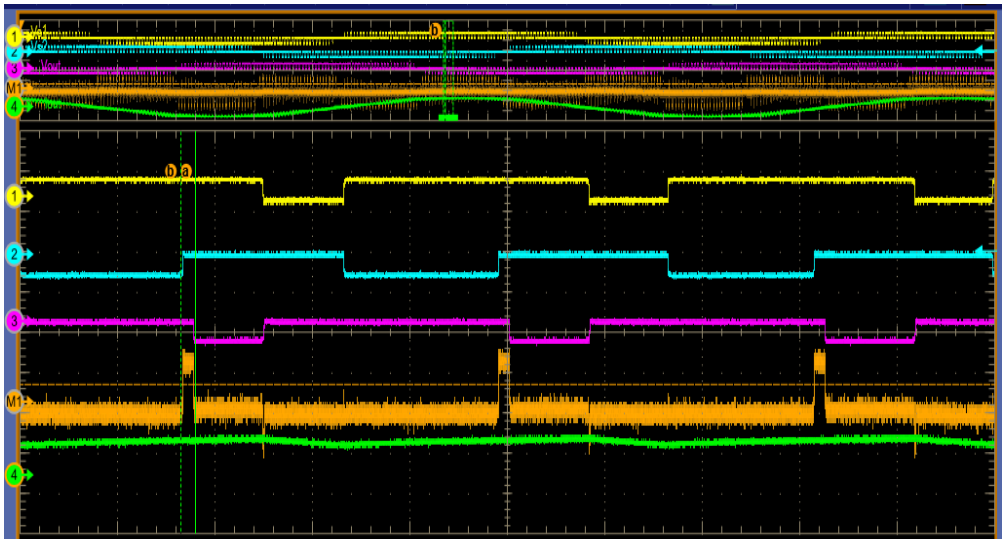


Figure 4-18 1 μs DT test results with CME modulation (Zoomed)

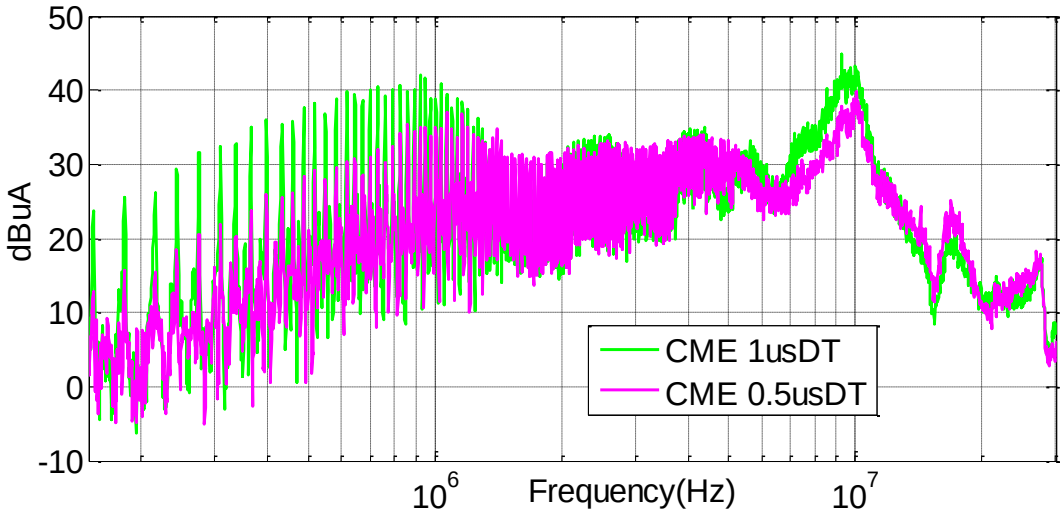


Figure 4-19 AC CM noise comparison of CME modulation

0.5usDT : pink, 1usDT: green

The frequency spectra of the ac terminal CM current measured for the different modulation schemes is shown in Figure 4-19, which shows how for larger DT (1 μs) the CM current spectrum increases significantly, illustrating this modulation scheme loses effectiveness becoming a poor choice for larger DT, if additionally its reduced voltage utilization ratio and loss of NP voltage balancing control penalties are considered.

4.4 Improved CME Modulation and DT Compensation

The impact of dead time on CM voltage can be reduced with some improvements. This section will present two improved methods to solve this problem: improved CME modulation (ICME) and dead time compensation for CME modulation. The detailed implementation methods are presented, ICME modulation change the vector sequence according to the phase current to ensure the impacts of dead time on the two switching phases are the same thus the switching will still happen at the same time and the CM voltage can be canceled. On the other hand, the dead time compensation method for CME modulation use the compensation principle that compensate the dead time on the gate signal of the power semiconductors to compensate the impact of dead time on each phase leg and still make the two phases switch at the same time to reduce the impact of dead time on common mode noise emission for CME modulation. All the analysis are experimentally verified with the 2.5kW laboratory prototype.

4.4.1 Improved CME Modulation

In the original CME modulation scheme, there are always three different voltage changes within one switching cycle. For example, when the reference voltage vector is located in the first sector, the three different voltage changes are: (1) phase A:O→P, phase

C: O→N; (2) phase A: P→O, phase B: O→P; and (3) phase B: P→O, phase C: N→O. Accordingly, since $i_A + i_B + i_C = 0$, and based on the impact of DT on the phase output voltages analyzed in the previous section, a single CM voltage pulse per switching cycle will be generated as a result of the three-phase voltage transitions. Consequently, modifying the vector sequence in this switching pattern will not eliminate the impact of DT on the converter CM voltage.

On the other hand, if no commutations occur among the two phases that have the same current direction then the generated CM voltage will be zero on a switching cycle basis. For example, if the vector sequence is changed to be OOO→PON→OPN→PON→OOO as shown in Figure 4-20(a), where there are four voltage transitions within one switching cycle: (1) phase A: O→P, phase C: O→N; (2) phase A: P→O, phase B: O→P; (3) phase B: P→O, phase A: O→P; and (4) phase A: P→O, phase C: N→O, it is clear that the simultaneous commutations only involve phases A-B and phases A-C. Further, if the current direction of phase A is different from that of phases B and C, the DT effect on the two phases will always be the same during the entire switching period and the CM voltage will remain zero as shown in Figure 4-20(b).

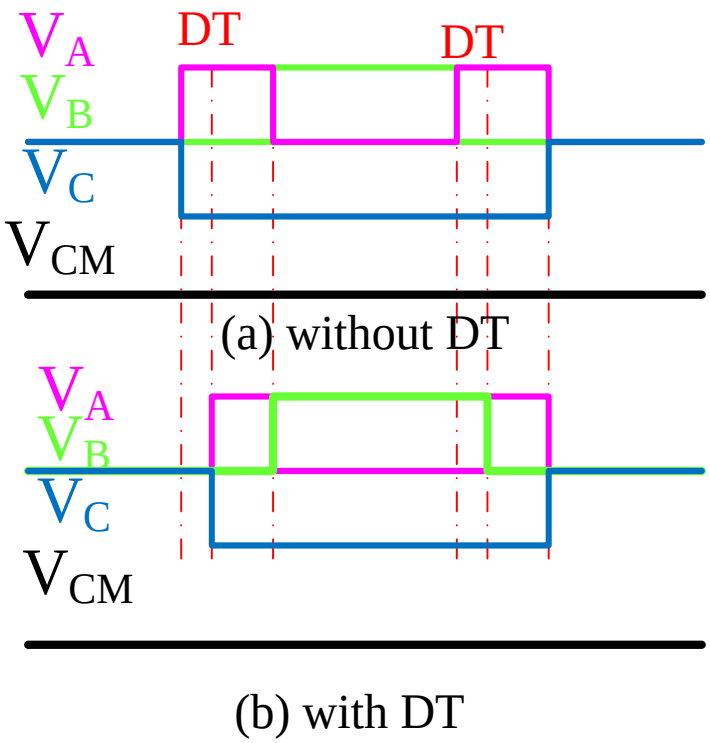


Figure 4-20 Impact of DT on CM voltage with ICME modulation

The above shows that by selecting a different space vector sequence, based on the current direction relationship between the three phases, the effect of DT on this modulation scheme can be effectively eliminated. The vector sequence selection of the improved common mode elimination (ICME) modulation technique is shown in Table 1 for sector 1. To determine the relationship between the phase current directions the product of two phase currents can be compared with zero.

$$i_A i_B < 0 \text{ and } i_A i_c < 0 \tag{4-7}$$

For example, if (4-7) is true then the current direction of phase A is different from phase B and phase C, and the vector sequence in sector 1 can be selected based on Table 4-4. As observed, with this modulation method the unwanted effect of DT is fully eliminated.

Table 4-4 Voltage vector sequence and dwell time for ICME modulation when reference vector lies in sector 1

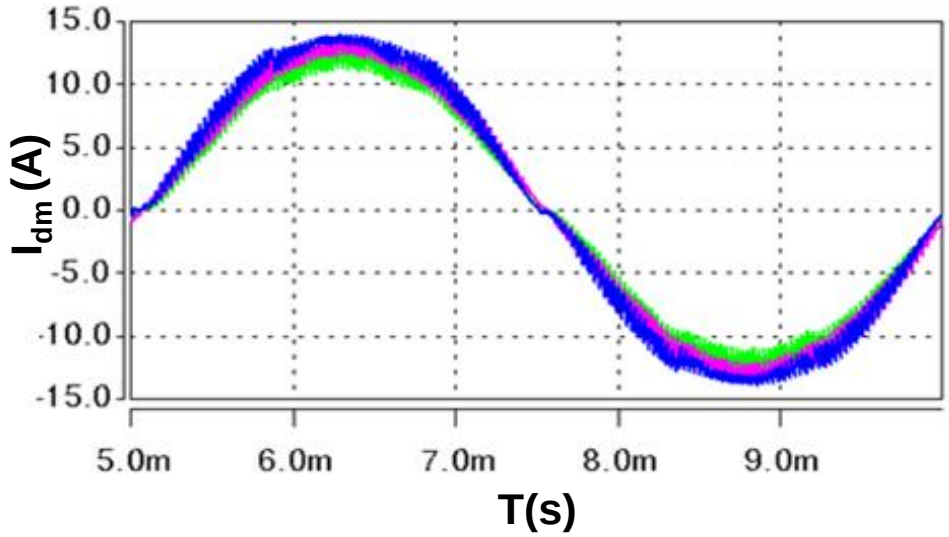
when Iout direction of phase A, C is different with Phase B						
Dwell time	T0/2	T1/2	T2/2	T2/2	T1/2	T0/2
A	O	O	P	P	O	O
B	O	P	O	O	P	O
C	O	N	N	N	N	O
when Iout direction of phase B, C is different with Phase A						
Dwell time	T0/2	T2/2	T1/2	T1/2	T2/2	T0/2
A	O	P	O	O	P	O
B	O	O	P	P	O	O
C	O	N	N	N	N	O
when I_{out} direction of phase BC is different with Phase C						
Dwell time	$T_1/2$	$T_0/2$	$T_2/2$	$T_2/2$	$T_1/2$	$T_0/2$
A	O	O	P	P	O	O
B	P	O	O	O	O	P
C	N	O	N	N	O	N

One drawback of this modulation method is that it will increase the switching losses of the converter. It is clear that there is always one phase that switches twice in one switching period and that the current direction of this phase is the opposite of the other two phases. Since the sum of the three phase currents is always zero, this specific current will be the largest one among the three phases, which results in an increase of up to 50 % in switching loss when compared to the basic CME modulation scheme. Conduction losses

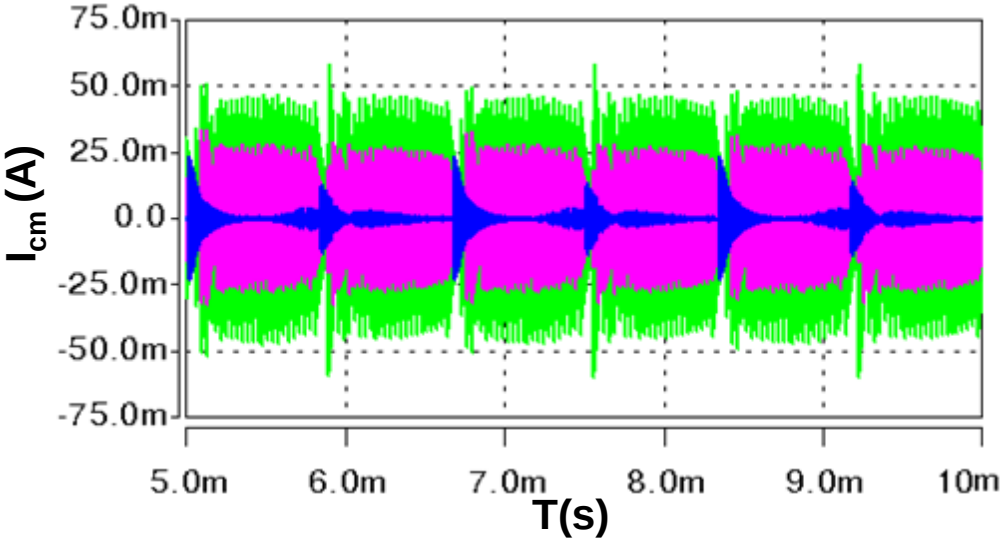
on the other hand will remain unchanged, since the total dwell time of the different vectors is the same within the switching period. The increase of switching loss can be calculated using an analytical method based on the device datasheet as presented in the previous section.

4.4.2 Verification for ICME Modulation

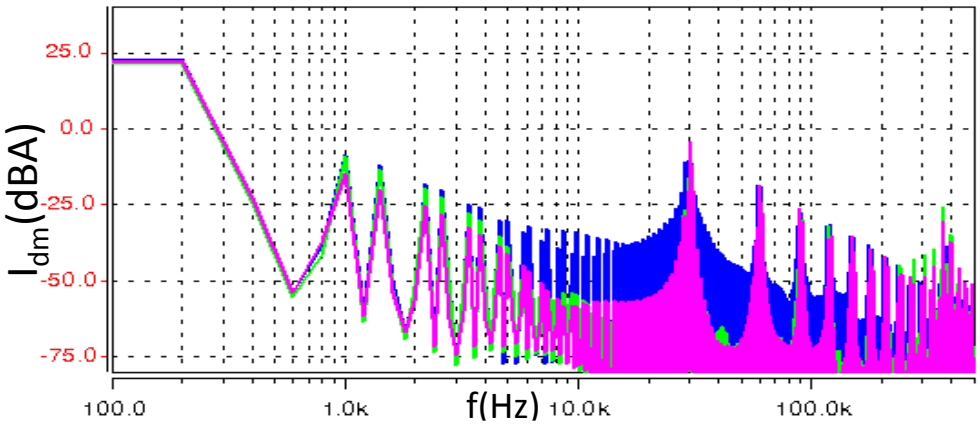
To verify the analysis and the proposed compensation method, both simulations and experimental tests were conducted based on the 2.5kW 3L-NPC prototype. A detailed switching model of the converter was built in SABER to analyze the impact of DT and to verify the compensation method developed. Time and frequency domain simulation results showing the ac terminal CM and DM currents are shown in Figure 4-21. These indicate that under standard CME modulation the current distortion increases for larger DT periods as shown in Figure 4-21(a), and also that fundamental frequency harmonics of the DM current, such as 5^{th} and 7^{th} components, have larger magnitude, whereas switching harmonics are comparable with the smaller DT cases as shown in Figure 4-21(c). Lastly, it is also apparent in Figure 4-21(b) and (d) how bigger DT increases the CM current since all switching frequency harmonics increase more than 15 dB.



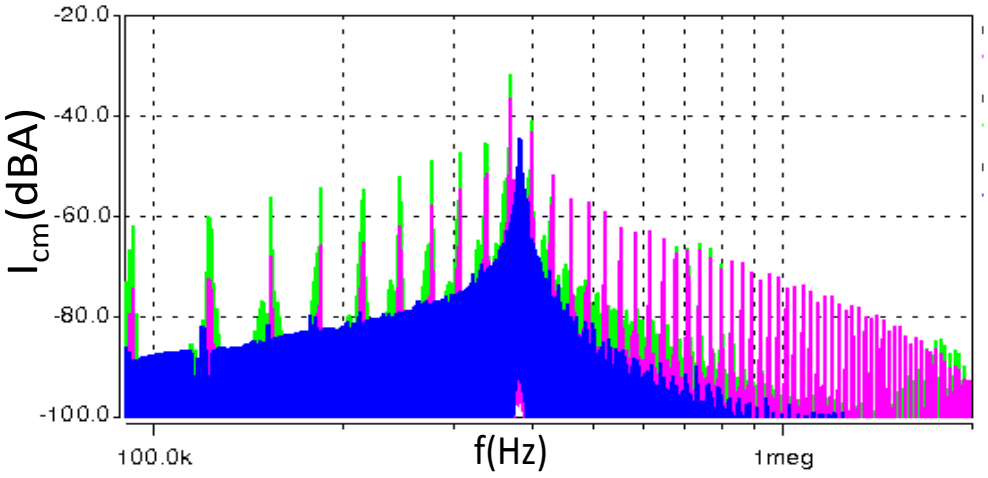
(a) AC DM current



(b) AC CM Current



(c) AC DM spectrum



(d) AC CM spectrum

Figure 4-21 System simulation results for ICME modulation

with 0.5 μs DT: pink; with 1 μs DT: green, with 1 μs DT and ICME: blue

With ICME modulation on the other hand, the CM noise is reduced significantly as shown in Figure 4-21(d). Further, Figure 4-21(c) shows that using ICME modulation does not change the fundamental frequency harmonics compared to standard CME modulation; however it does reduce the peak value of the switching harmonics. Lastly, it can be observed that the side bands of the switching frequency harmonics are higher in the ICME case; whether this is worse or better for the DM filter design will depend on the final system specifications.

Experimental test results are shown in Figure 4-22 to illustrate that with ICME modulation the converter CM voltage is free of any pulse generation related with dead time and is indeed kept at zero, since the impact of DT is effectively canceled out by only switching the phase-legs with equal DT effect. It can also be observed how during the switching period phase A has twice the switching frequency compared to phases B and C, which verifies switching loss increase of the proposed modulation method.

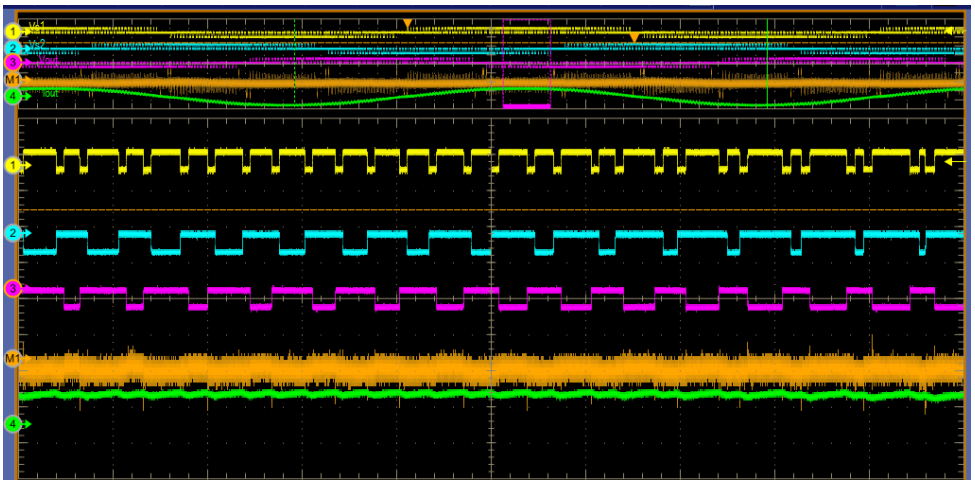


Figure 4-22 1 μs DT test results with ICME modulation (zoomed)

Waveforms depicted are: V_{an}: yellow (200V/div), V_{bn}: cyan (200V/div), V_{cn}: purple (200V/div), V_{cm}: orange (100V/div), and I_{out}: green (15A/div).

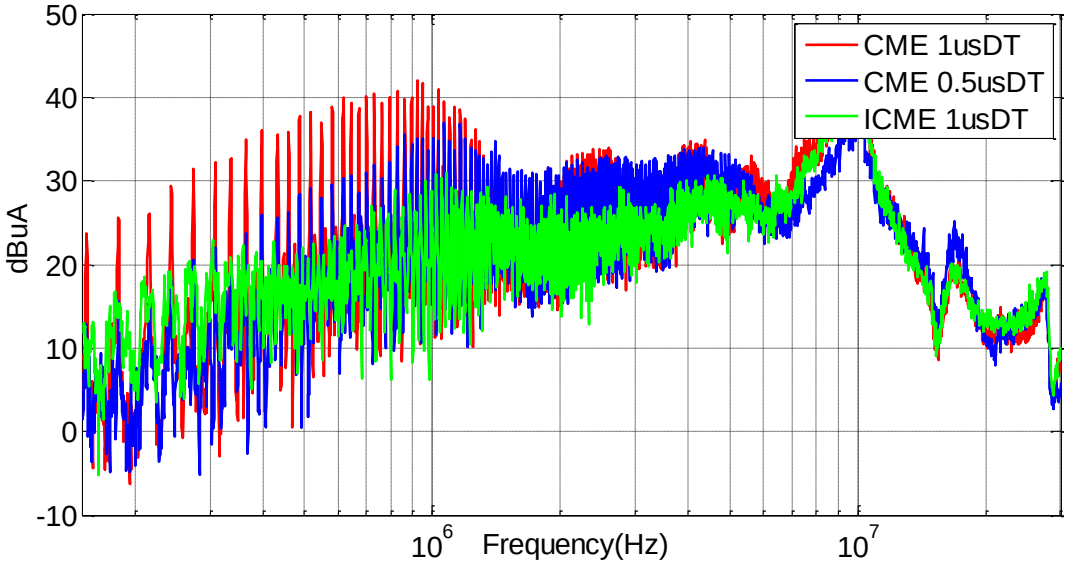


Figure 4-23 CM noise comparisons for ICME modulation

CME modulation with 1 μs DT: red, CME modulation with 0.5 μsDT: blue,

ICME modulation with 1 μsDT : green

The frequency spectra of the ac terminal CM current measured for the different modulation schemes is shown in Figure 4-23. It is apparent that the proposed ICME modulation can effectively contribute to reducing CM EMI noise even under the use of large DT. In fact, its cancellation is such that the resultant CM noise under ICME for 1 μs DT is lower than the CM noise generated under CME modulation with a DT of 05 μs. This

is so since with CME the converter CM voltage still consists of, although narrow, a 0.5 μs pulse per switching cycle, while with ICME the converter CM voltage is effectively zero, and is so regardless of the DT amount used.

4.4.3 DT Compensation for Minimum EMI

The impact of dead time for CME modulation can also be reduced by implementing the dead time compensation. In two level inverter applications, adding dead-time to the system will create the problem of output current distortion and compensation methods are used to solve this problem [99]. The same problem exists in three-level inverter applications and similar compensation methods can be used to reduce the output current distortion due to DT [100]. Considering the impact of DT on CM voltage generation, a similar DT compensation idea can be devised; however, the position of the compensating pulses needs to be considered carefully to ensure that the phases switch at the same time.

For the three-level topology, one phase-leg can output three different voltage levels, P, O and N. Considering the voltage sequence used in CME modulation one phase-leg can only switch on and off once within a switching period, and the voltage transition can only be of two kinds: O→P→O and O→N→O. Then the impact of DT on CM voltage during one switching period is as shown in Figure 4-24.

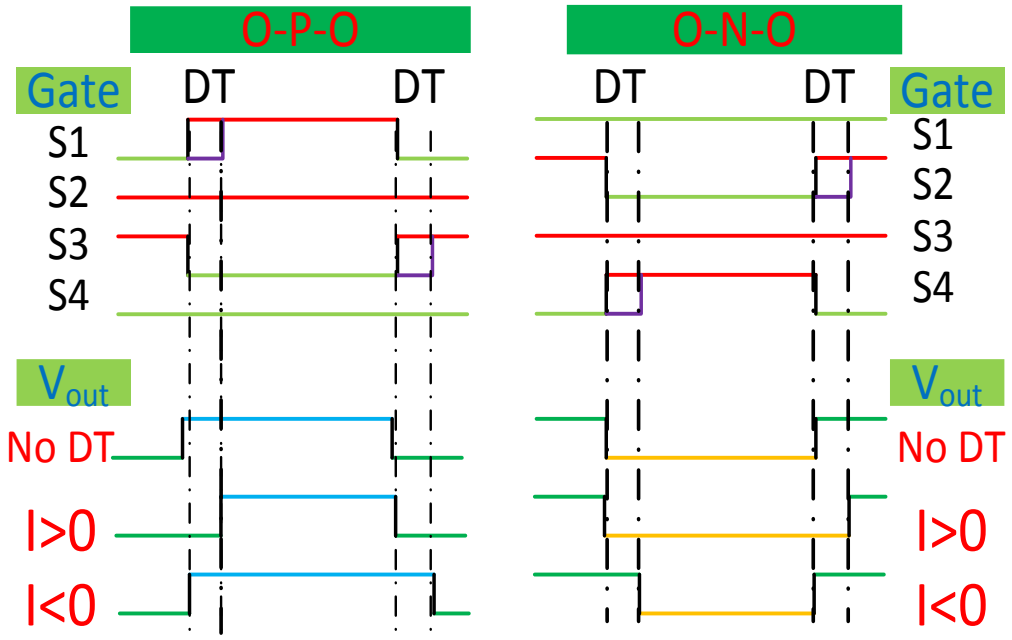
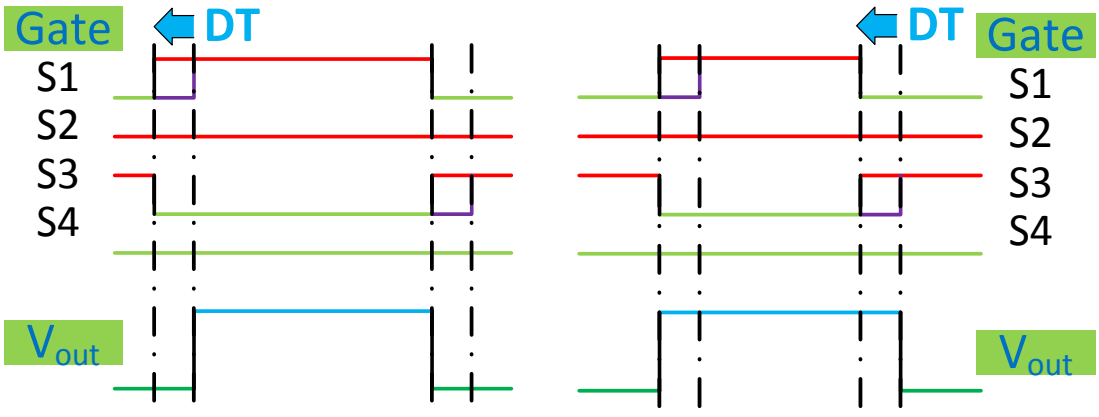


Figure 4-24 Impact of DT on CM voltage generating during one switching period

For the voltage transition that is O→P→O, there will be one period of DT length removed at the beginning of the output voltage when Iout>0, and there will be one DT period added at the beginning of the output voltage when Iout<0. When the voltage transition is O→N→O, the procedure is the opposite. This error can be compensated from the gate signal of the power devices. Figure 4-25 shows the compensation used for the voltage transition O→P→O with different current directions.



(a) I>0 Increase at the beginning **(b) I<0 Reduce in the end**

Figure 4-25 Compensation of DT to reduce CM voltage

Table 4-5 Dead time compensation algorithm for CME modulation

Voltage Transition	Compensation	
	phase current i>0	phase current i<0
O→P→O	Add DT at the beginning of S1,S3	Reduce DT in the end of S1,S3
O→N→O	Reduce DT in the end of S2,S4	Add DT at the beginning of S2,S4

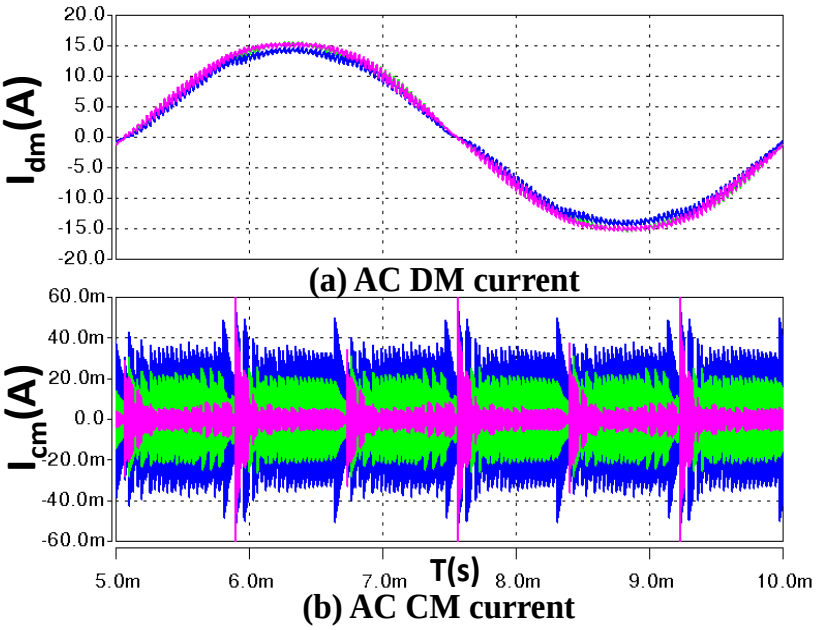
To compensate the impact of DT on current distortion, one can reduce the additional period of time or add the removed period of time to the calculated duty cycle. However, to compensate the impact of DT on CM voltage reduction, the position of the compensated DT needs to be considered. Since in the original PWM signals two phases switch simultaneously, after the compensation of DT the output voltages also need to switch at the same time. So, if the impact of the DT is to reduce the period of time at the beginning of the pulse, the compensation should add the DT time at the beginning of the pulse too (Figure 4-25). The DT compensation algorithm for CM voltage reduction in 3L topologies is shown in Table 4-5.

4.4.4 Verification of the Proposed DT Compensation Method

To verify the previous analysis and the proposed compensation method, both simulation and experimental testing were conducted based on the 3L-NPC prototype. A detailed switching model of the system was built in SABER to verify the DT compensation method.

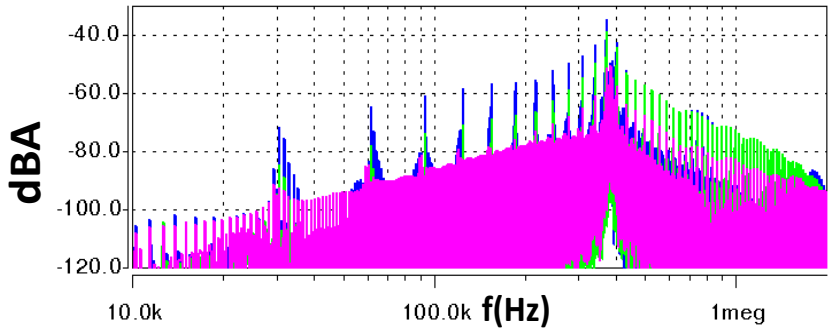
The AC CM, and AC DM current time domain simulation results and AC CM current spectrum simulation results are shown in Figure 4-26, which indicate that with a larger DT

added to the system, without compensation, the output current distortion is larger, while with the compensation, the distortion can be reduced and the current is more sinusoidal (Figure 4-26(a)). Moreover, increasing DT will also increase the CM current, whereas with compensation, the CM current can be reduced significantly as shown in Figure 4-26(b). Figure 4-26(c) indicates that the CM current shows a 30 kHz switching behaviour, which verified that within one switching period there is only one pulse generated due to the dead-time. Besides, when the system DT increases from 0.5 μs to 1 μs, all the CM current switching harmonics increase about 20 dB below 500 kHz, which requires more attenuation from the EMI filters making the filter size bigger. With DT compensation implemented, the switching harmonics were reduced significantly and the CM current spectrum of 1 μs with DT compensation condition is even lower than the 0.5 μs case without DT compensation, which can help reduce the CM EMI filter size significantly.



(a) AC DM current

(b) AC CM current



(c) AC CM current spectrum

Figure 4-26 AC CM and AC DM current time domain simulation results

0.5us DT no compensation: green, 1us DT no compensation blue, 1us DT with compensation pink

The experimental verifications was also carried on the 2.5 kW 3L-NPC prototype. Figure 4-27and Figure 4-28 show the experimental test results.

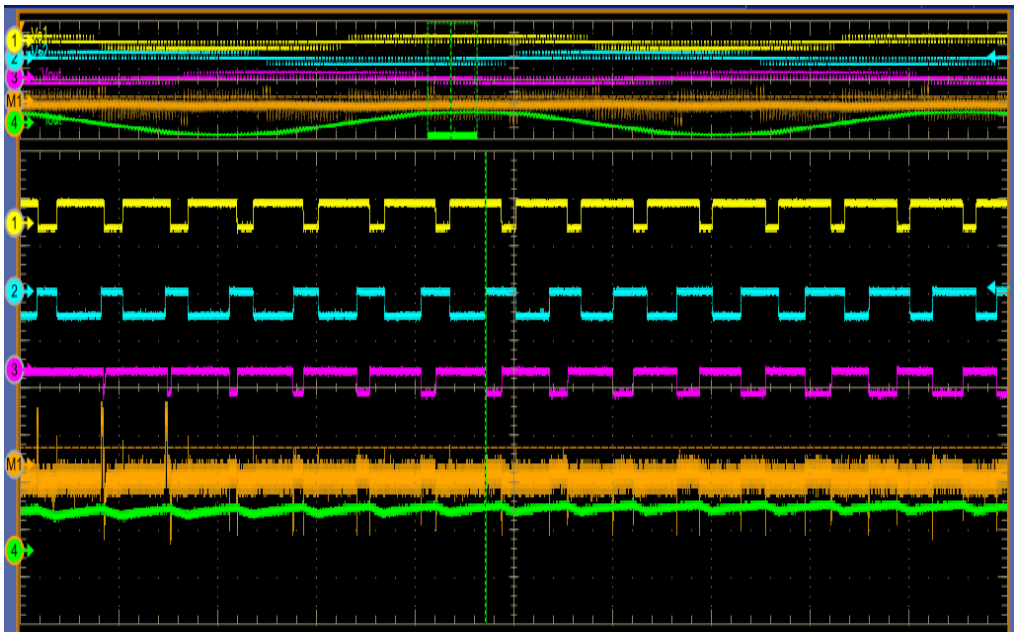


Figure 4-27 Time domain test result with CME modulation with DT compensation with 1us deadtime

V_{an} :yellow (200V/div), V_{bn}: cyan (200V/div); V_{cn} : purple (200V/div); V_{cm}: orange (200V/div), I_{out}: green (15A/div)

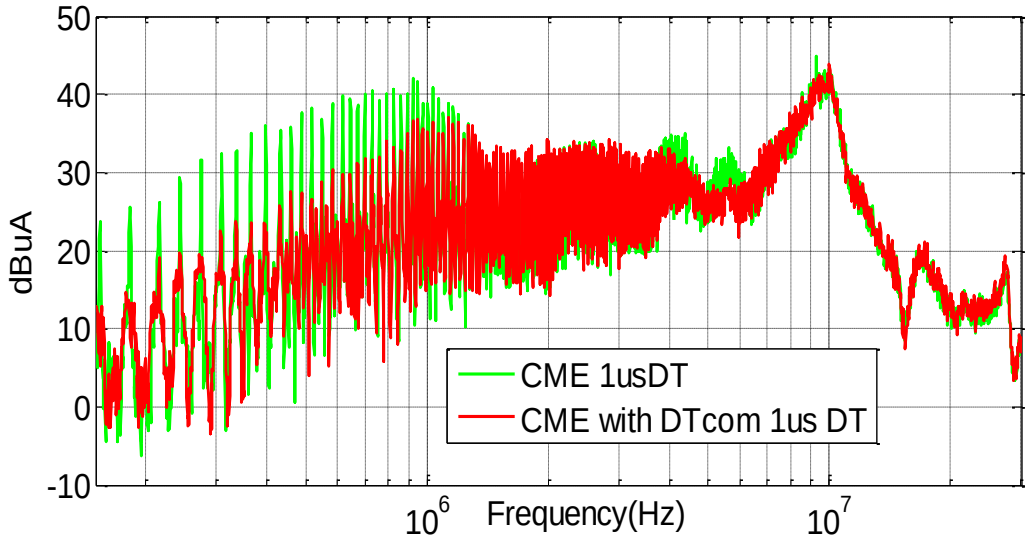


Figure 4-28 Measured AC CM noise comparisons with 1us DT

CME modulation without DT compensation: green, CME modulation with DT compensation: red

From the time domain results, it is clear the proposed dead time compensation method can reduce the impact of dead time on the CM voltage generation. Compared with the regular CME modulation without DT compensation, there is no such error pulses related with the dead time on CM voltage. For the implementation of DT compensation, since the performance of the IGBT devices are dependent with system operation point, the real compensated DT value in the system should be tuned to make the best CM voltage elimination. A look-up table can be used to select the compensation value based on system operation condition. With the DT compensation method the impact of DT can be reduced as shown in Figure 4-27. When phase current direction is correct, the error pulse on CM voltage generated due to DT can be eliminated. While the phase current is approaching zero, the sensing circuit has errors on current direction detection, in that case adding a wrong DT compensation will make the CM noise worse, thus during this period, no compensation was used and the error pulse still exist. The frequency domain AC CM current are measured based on DO160E standard, which show the effectiveness of the proposed compensation method. CME modulation can reduce the CM noise significantly

compared to NTSV when DT is small. With the proposed DT compensation method implemented with CME modulation, the impact of DT can be reduced significantly. The CM current noise can be reduced up to 20 dB compared with CME modulation without DT compensation and the noise level is not sensitive with DT added to the system.

4.4.5 Summary and Discussion

This section has presented a detailed analysis on the impact of dead-time on the EMI performance of 3-L NPC inverters using CM voltage elimination modulation techniques and proposed two solutions to reduce this effect. By analyzing the switching steps and electrical states of a single phase-leg, the impact of dead time on system CM voltage cancelation is studied in detail to explain why the effectiveness of its CM voltage cancellation capability is severely hindered and strongly dependent on the amount of dead-time used to gate the switching devices of the converter. Based on these analysis, two methods are proposed to solve this issue by two different approaches. The improved CM voltage elimination modulation scheme can effectively desensitized the modulation technique from the impact of dead-time, where a new space vector sequence was developed taking the current direction of the three phases into consideration, ensuring that only the two phases with the same dead-time effect during the switching period could commutate. Simulation and experimental results verified the analysis conducted and the proposed method, showing additionally how the conventional CME modulation could only reduce CM voltage with respect to NTSV when using short dead-time periods, and that it would actually increase CM voltage with respect to NTSV when using larger dead-time. The proposed ICME modulation on the other hand was shown to effectively mitigate CM voltage and to fully eliminate its dependence on DT.A dead time compensation method for

CME modulation was proposed to reduce the impact of DT on CM voltage generation. To achieve both CM voltage reduction and current distortion minimization, the position of the compensated pulses was shown to be of high importance. For verification purposes, simulation and experimental results were also carried out on a 2.5 kW NPC 3L VSI prototype. The results showed that the impact of DT on CME modulation was reduced with the proposed DT compensation method. In effect, the CM current noise could be reduced up to 20 dB compared with CME modulation without DT compensation. Additionally, the noise level was shown to be not sensitive to DT, making CME modulation a more practical scheme.

Comparing the improved CME modulation and dead time compensation for CME modulation, both of them will need the current information from the system to effectively reduce the impact of dead time on CM voltage generation. However, for dead time compensation method, since the device characteristics are different under different conducting current, thus the real dead time on the system is different with the programed dead time applied on device gate signal and it is changed with different working conditions. Thus given a fixed compensation value cannot ensure a good cancellation over the whole fundamental period even when the current information is correct, there will always be some small errors during the compensation unless the compensation time is tuned online with different working conditions. While, for improved CME modulation, the dead time will always have the same impact on the two phases that switch at the same time, thus, when current information is correct, improved CME modulation method will have a better performance than dead time compensation method. However, the main penalty of ICME modulation is that the one phase will have twice the switching frequency of the other two

phases, the switching loss will be increase by up to 50%. Since dead time compensation method does not change the vector sequence, it will not change the semiconductor losses in the system.

4.5 100kW Interleaved Three Level System Design and Test Results

4.5.1 System Requirements and Baseline Design Results

In order to verify the validation of the proposed methods for high power applications, a 100kW dc-fed motor drive system with EMI filters for both AC and DC sides was designed, implemented and tested. The design requirements are shown in Table 4-6. The main design target is to reduce the system weight and improve power density. Since the system have 90 feet output cables, both AC-side and DC-side EMI noise need to be well suppressed according to DO160-E standard, thus EMI filters are needed for both AC and DC sides. A baseline design was performed on a tradition 2L VSI running at 10 kHz, the weight breakdown is shown in Figure 4-30. It is clear that the EMI filters takes more than 75% of the total system weight, thus reducing EMI filter weight is the main design goal.

Table 4-6 Design requirements for 100 kW motor drive system

Nominal Power	DC input voltage	Ac output voltage	Output frequency	Cooling method	Output cable	Standards
100kW	± 270 V (ATRU supplied)	180 V_{LN_RMS}	Up to 1200Hz	Liquid cooling	90 feet	DO160 for both input and output

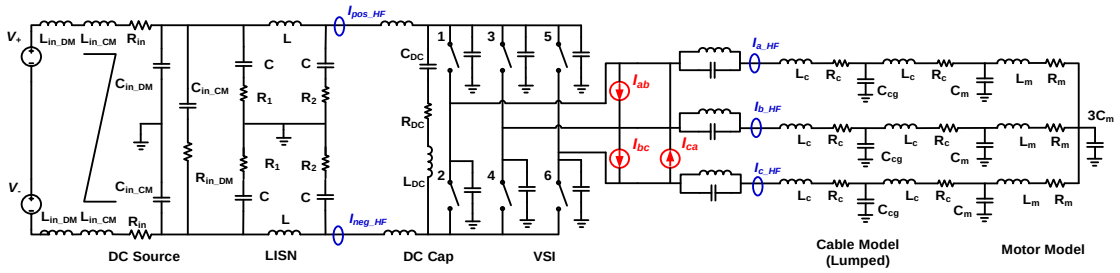


Figure 4-29: System Structure of the baseline system

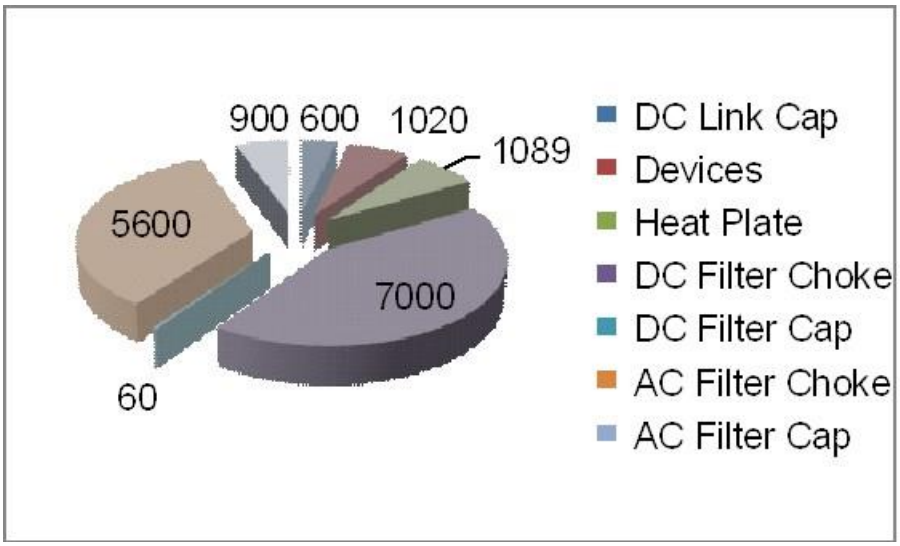


Figure 4-30 100kW system weight breakdown of baseline design

4.5.2 Topology Selection and Design Summary

The previous analysis shows that the impact of interleaving and three level topology on system EMI noise generation is different. Both of them can help to reduce the EMI noise in the system. However, in interleaving topology, the interleaving angles can be selected to either reduce the volt-second or to shape the voltage noise source according to the impedance resonance and reduce the attenuated needed from the filter to reduce the inductance needed in the filter. However, the three level topology can help to reduce the output voltage step, thus it can reduce the volt-second and also reduce the EMI noise emission for the whole range compared with two level topology. Moreover, different modulation methods can be applied for different optimization targets. Since the 100 kW motor drive system is intended to be used with different loads and sources, thus the

propagation path impedance of the system will be changeable. Since the benefit of interleaving and three level topology will be different with different load and source impedance, there is not a universal optimized topology for all the design conditions. With this consideration, an interleaved three level voltage source inverter is designed and implemented as the power stage of the system.

Figure 4-31 shows the structure of the implemented system. The power stage consist of two three-level voltage source inverters working at interleaved or non-interleaved configuration. Each converter can be designed to handle 50kW power and the switching frequency is pushed to the highest limitation. The system is reconfigurable, it can run as two level topology, two level interleaved topology, three level topology and three level interleaved topology. With different system connection and different propagation path impedance, different topology with different modulation methods can be applied and tested to find the real optimal topology for minimum weight of the filters. The interleaving operation is more suitable when there is resonance peak in the propagation path that determines the EMI filter design since there is the freedom of changing interleaving angles to achieve inductor value minimization and/or volt-second reduction. However, the interphase inductor is necessary when interleaving technique is used since the load inductor is inside the motor for motor drive system. Each converter can be operated as either three level or two level topologies with different modulation schemes. Thus the benefit of using three level topologies can be verified through the high power system. For three level topology, different modulation methods can also be applied to verify the previous analysis via a higher power system.

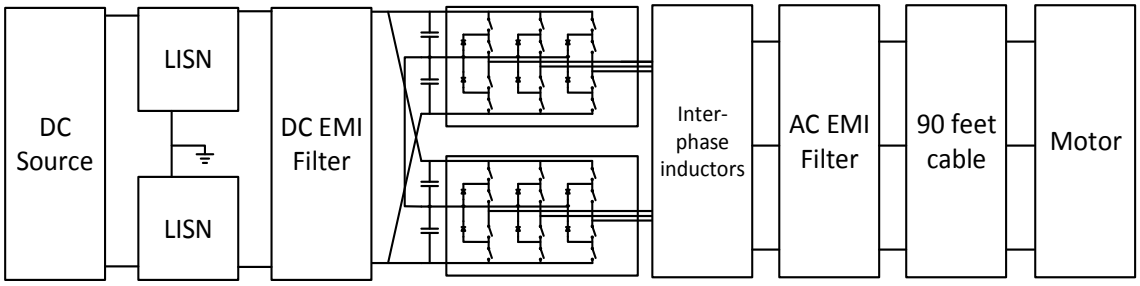


Figure 4-31 Structure of the implemented 100kW system

With the proposed interleaved three level topology, the power converters are designed according to the design requirement. Table 4-7 shows the weight summary of interleaved three-level converter and Figure 4-32 shows the weight breakdown of the power stage. Each part of the system was designed and optimized for the minimum weight of the system. Due to the limitation of device availability, the three level phase leg was built by using three individual IGBTs with 2L phase leg configuration. Since the power devices are commercial devices, the weight and size is relatively big, thus the weight of the device and the cold plate take a big portion of the system and make the total weight relatively big.

Table 4-7 Weight summary of interleaved three-level converter

Device	Cold plate	Gate driver	Interface board	Busbar	DC capacitors	Total
2790g	5570g	810g	434g	540g	1020g	11164g

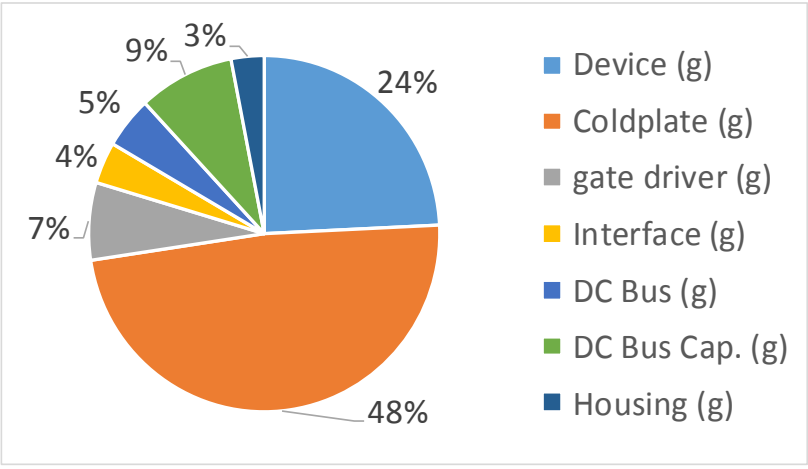


Figure 4-32 Weight breakdown of the implemented 100kW power stage

With the power stage topology and system propagation path impedance information, the filters are designed and implemented for both AC and DC sides using the proposed filter design and implementation methods presented in chapter 2. Figure 4-33 shows the filter topology

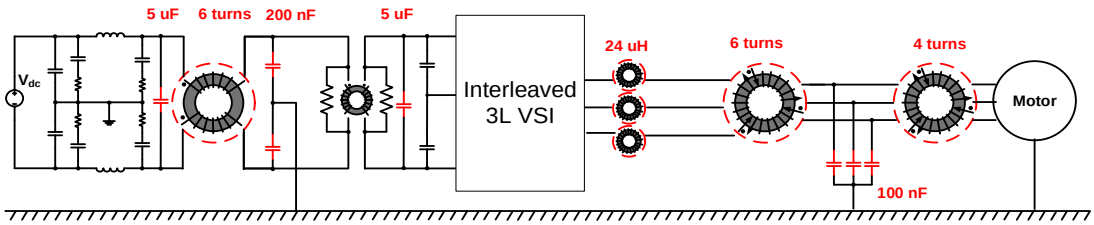


Figure 4-33 Filter structure in the implemented 100kW system

For AC side, A L-C-L structure filters are selected to effectively attenuate the noise, the first stage L can maintain the impedance mismatching between the CM noise source and input of the filter. Moreover, it can increase the propagation path impedance for the DC side to avoid the noise boosted by connecting the grounding capacitors. The second stage L maintain the impedance mismatching between the output of the filter and the load impedance including the cable and motor. An L-C structure is selected for the AC DM filter, L can maintain the impedance mismatching between the DM noise source and input of the filter, C can maintain the impedance mismatching between the output of the filter and the load impedance. Since the load inductance is inside the motor and the DM inductance is relatively small, the DM capacitance is limited to avoid large current ripple at the output of the converter. Similarly, for dc side, a C-L-C structure is selected to provide enough attenuation for DC DM noise and a C-L structure is selected to effectively attenuate DC CM noise.

Following the filter weight minimization method proposed in section 2, the filters are design for the system to attenuate both AC-side and DC-side EMI noise below the standards, the EMI filter weight design result is shown in Figure 4-34. The design of the

filter was done by Jing Xue in CURENT lab in University of Tennessee, Knoxville. Detailed design methods can be found in Reference [138][139].

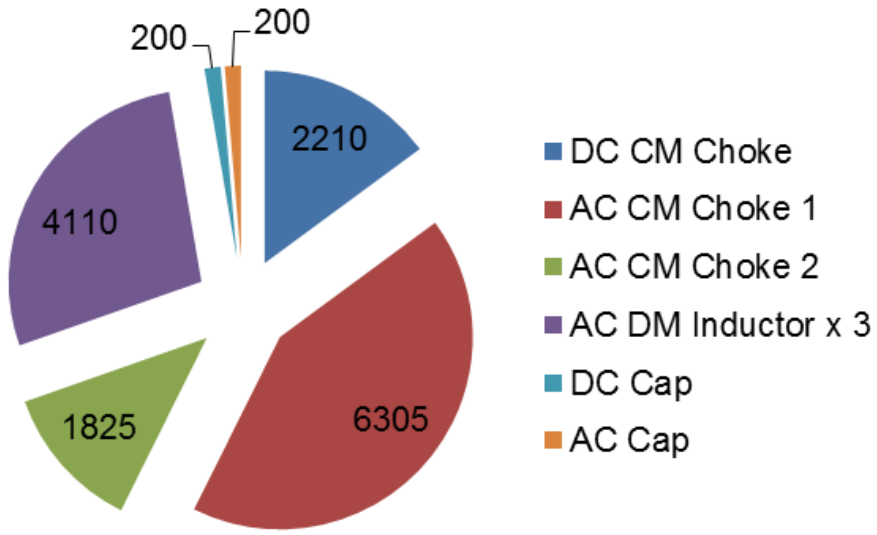


Figure 4-34 EMI filter weight design result

4.5.3 Hardware Implementation and Test Results

The power stage is implemented and tested in the lab. Figure 4-35 shows the two implemented three level voltage source inverters working in the interleaved mode in the test setup with RL load. Figure 4-36 show the test result of the system with two converters running at 100kW output power with RL Load with 180 interleaving. The results shows the normal operation of the system and validate the design process.

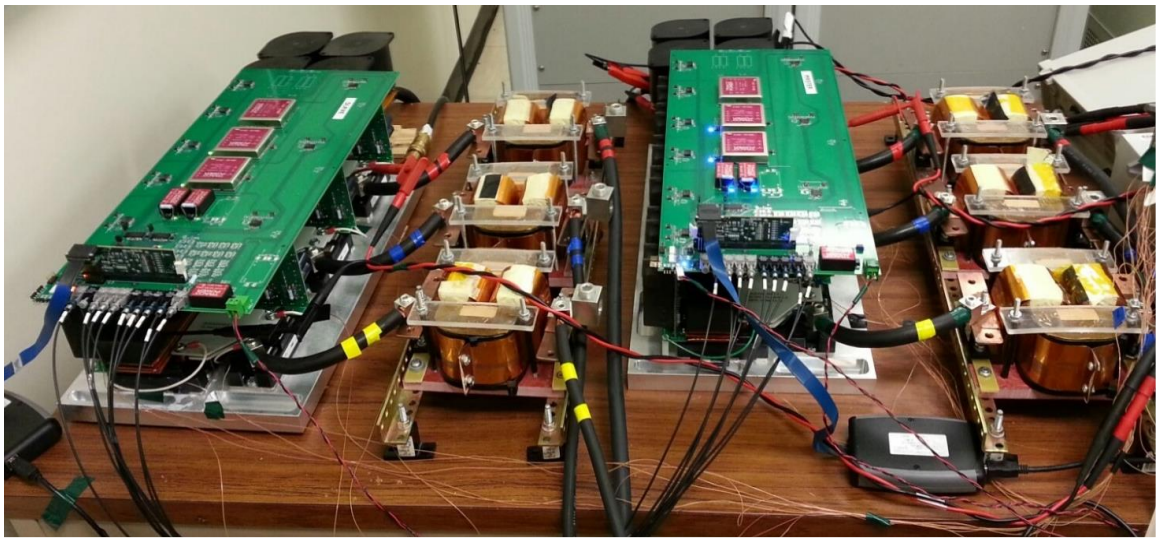


Figure 4-35 100 kW interleaved three level power stage hardware

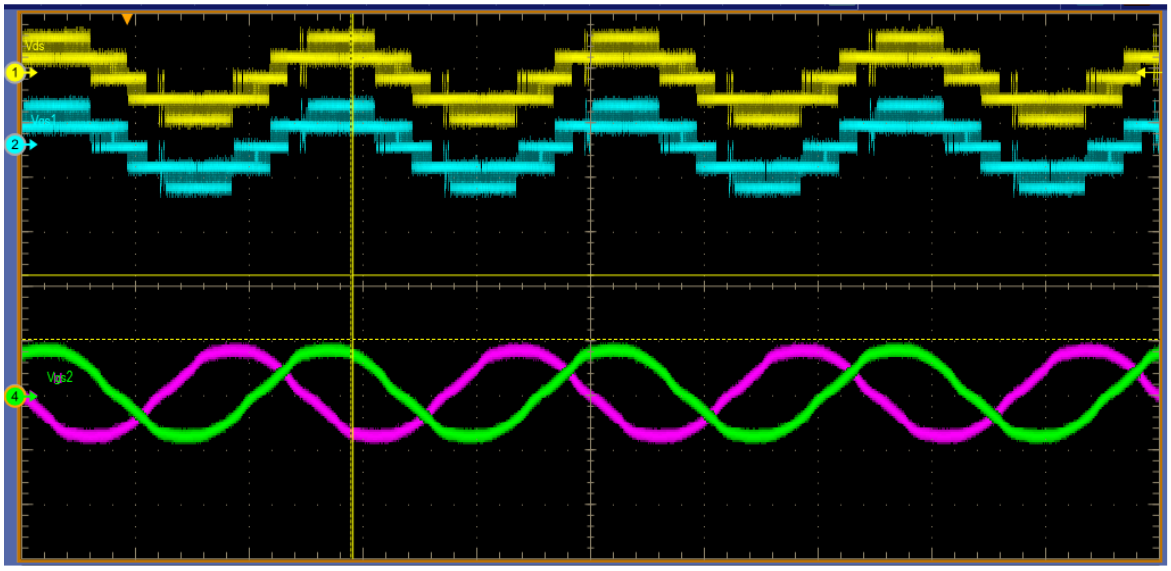


Figure 4-36 Time domain test result of the implemented 100kW power stage

The frequency domain measurement results of system CM noise is shown in Figure 4-37 with 180 interleaving angle and non-interleaving operation, which showed the effective attenuation of system EMI noise by using 180 ^{o} interleaving and verified the analysis of interleaving topology in chapter 4.

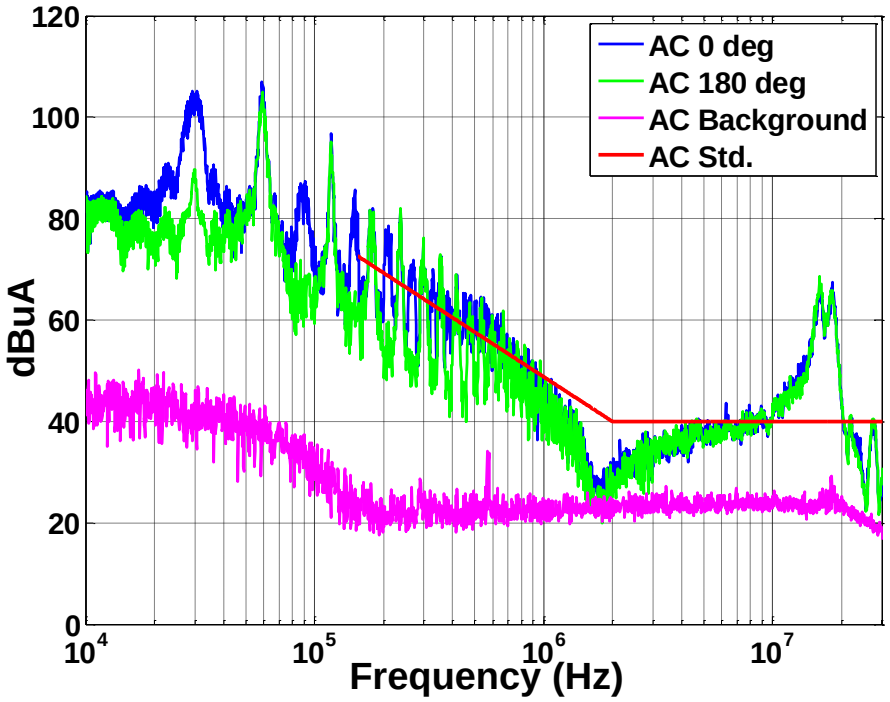
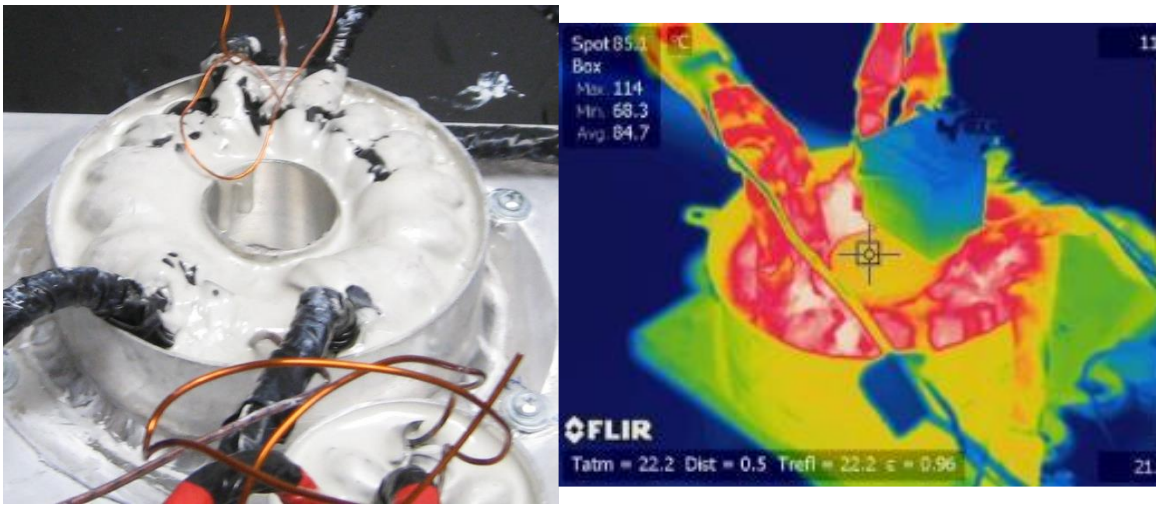


Figure 4-37 AC line bare noise measurement results

With the designed parameters and estimated working conditions, the filters are also implemented in the lab and tested for thermal and EMI performance, Figure 4-38 shows the implemented AC side second stage CM choke and its thermal test result. The filter implementation was done by Jing in University of Tennessee, Knoxville. Detailed implementation methods can be found in Reference [138].



Implemented CM choke **Thermal test result**

Figure 4-38 High power inductor implementation

Finally, the complete system with both power stage and EMI filters was packaged, delivered and tested on site. Figure 4-39 shows the picture of the packaged system which include the power stage, EMI filters, cooling system and the control systems.

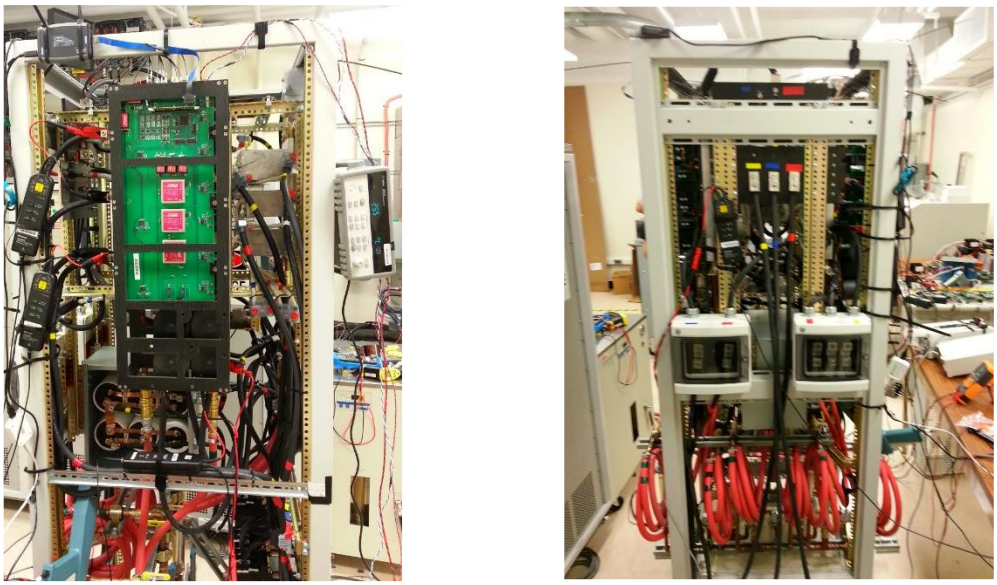


Figure 4-39 Packaged 100 kW motor drive system with EMI filters

Figure 4-40 shows the on-site test result of the complete system with motor load in time domain, which verified the normal operation of the system. Figure 4-41 shows the EMI test result of the system following DO160-E standard, which shows that the AC-side line noise was well attenuated with the implemented power stage and the designed EMI

filter. The dc side EMI noise is also attenuate, the results shows that it meet the standard except for two peaks at 2 MHz and 8MHz respectively. These noise can be attenuate by adding high frequency CM bead in the system without big penalty on system weight.

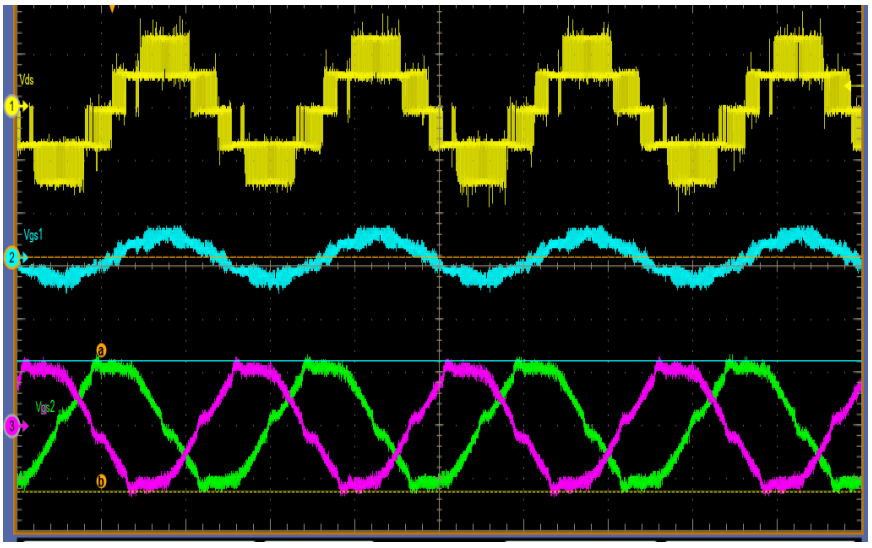
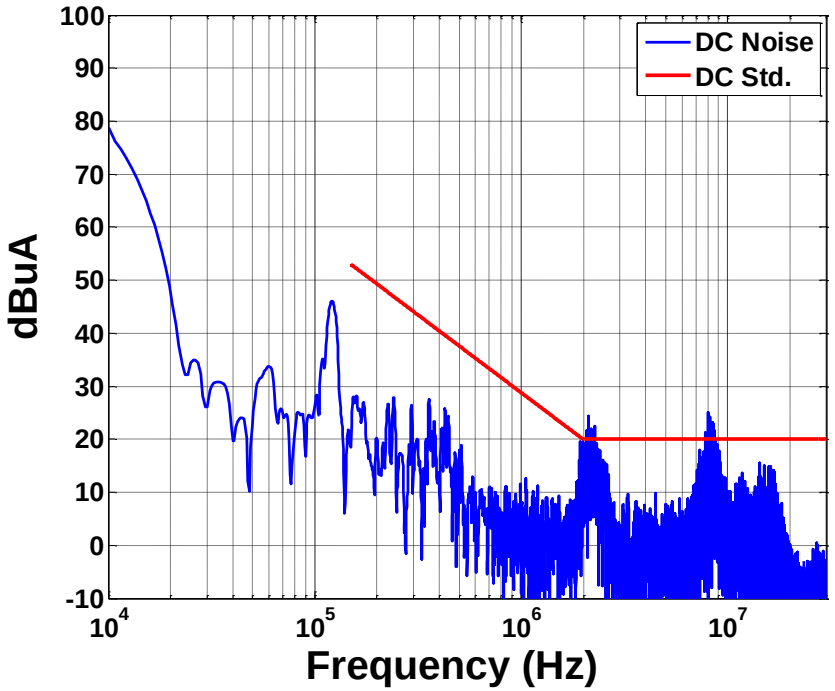
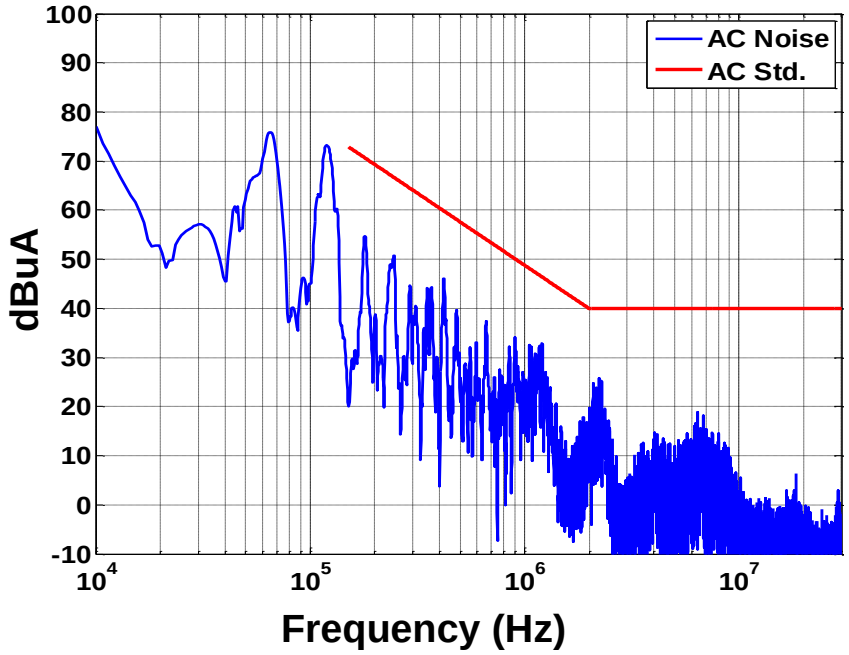


Figure 4-40 Time domain measurement result of 100kW system with motor load

($V_{out\_before\ filter}$: yellow;$V_{out\_after\ filter}$:cyan; I_{out1}:pink; I_{out2}:green)



(a) DC line noise



(b) AC line noise

Figure 4-41 EMI noise measurement result of 100kW system with motor load

4.6 Summary

This chapter presented a systematical analysis on the noise reduction techniques for three level neutral point clamped voltage source converters. First, an in-depth analysis of different modulation methods (NTSV, CMR and CME) is conducted from the aspects of EMI performance, NP voltage ripple, and system losses with the detailed comparison results through simulations and experiments. The results show that the NTSV have the best performance on harmonics reduction and it provides the freedom for neutral point voltage balancing; CMR modulation can help to reduce system CM noise and reduce the switching losses on the semiconductors; CME modulation method can effectively reduce the CM noise emission from the system.

However, the performance of CME modulation is highly sensitive to the dead time added in the system, which make this modulation method less practical. To address this

problem, this chapter presented a detailed analysis on the impact of dead time on system EMI noise emission for CME modulation. Based on the analysis, two methods are proposed to reduce the impact of dead time for CME modulation: dead time compensation and improved CME modulation. Both methods are provided with detailed theoretical analysis with the verification through both simulation and experiments. All the analyses are experimentally verified through a 2.5kW laboratory prototype.

Finally, in order to verify the validation of the proposed methods for high power applications, a 100 kW dc-fed motor drive system with EMI filters for both AC and DC sides was designed, implemented and tested. The design and implantation details were presented along with the full power test results, which proved the normal operation of the 100 kW system and verified the applicability of the proposed methods for high power applications.

Chapter 5 Conclusions

In this dissertation, a systematic methodology to analyze, design and reduce the passive component weight in three phase power converters is developed. All the analysis and proposed design methods are investigated with the goal of estimating and minimizing filters before power stage implementation so that the filters and power stage can be optimized for total system weight minimization.

Firstly, this dissertation studies the system level EMI modeling and filter design methods for a two level dc-fed motor drive system. A filter design oriented system-level EMI frequency domain modeling method is proposed where the source and load impedance in the model can be calculated from the detailed switching model or measured directly from the system and the frequency domain noise sources can be calculated using double Fourier integral transformation (DFIT) method. Based on this model, the interaction between AC and DC EMI filters are analyzed in detail. With this consideration, A EMI filter design method using predicted in-circuit-attenuation (ICA) is proposed for designing both ac-side and dc-side EMI filters together. Moreover, a new filter structure are proposed along with the design and analyzing methods that confine the EMI noise in the system to attenuate both input and output EMI noise. Moreover, based on the EMI noise prediction model and filter design methods, the impact of the noise propagation impedance and converter switching frequency on EMI filter weight/size is discussed in detail. A 1.5kW two level three phase voltage source inverter is developed to verify the proposed design methods and analysis.

Secondly, in order to reduce the system EMI noise, the impact of interleaving technique on system passive weight reduction is studied. Starting from a DC/DC high

power PV converters, the benefits of interleaving on input inductor weight reduction are analyzed in detail. Then, the analysis is focused on the impact of interleaving on system passive weight reduction for three phase converters. The impact of interleaving on system voltage noise source spectrum is studied with the consideration of system propagation path impedance. An analytical calculation method of optimal interleaving angles for minimal inductor value is proposed and verified through an experimental system. With the proposed filter design and weight minimization methods, a complete analysis on passive component weight optimization in interleaved two level systems is presented which shows that the optimal interleaving angle for EMI filter weight minimization is highly related with the propagation path impedance. Since interleaving creates the circulating current problems which need additional interphase inductors, the design and integration for interphase inductor are also analyzed in detail. The results show that interleaving topology will increase the total passive component weight for motor drive system due to the penalty on the additional weight of interphase inductor. A two level three phase interleaved voltage source inverter with complete control and hardware implementation is developed to verify the proposed design methods and analysis.

Thirdly, the noise reduction modulation methods are explored for three-level neutral point clamped VSI system. The evaluation of three modulations methods (NTSV, CMR, CME) are performed in the aspect of EMI noise emission, neutral point balancing and semiconductor losses through a three level VSI system developed in the lab. The results show that with ideal switches, CME modulation can reduce the CM noise more than 20dB up to 2MHz. However, the reduction is highly dependent on the dead time (DT) added to the system, which make the CME modulation less practical in real implementation. The

DT compensation method is proposed to solve this problem, which can reduce the impact of DT significantly. Moreover, an improve CME modulation is also proposed to reduce the impact of DT. A 3kW three level three phase voltage source inverter is developed to verify the proposed design methods and analysis.

Finally, based on the analysis and the proposed design and weight minimization methods, a 100 kW dc-fed motor drive system with EMI filters for both input and output sides are designed, implemented and tested. . Since interleaving and three level topologies have different impacts on system noise source reduction, they have different benefits on passive weight reduction when system operation condition is different. Combining the analysis of three level and interleaving topology, a three level interleaved system with two 3L DNPC VSIs working in paralleled and interleaved mode is selected as the power stage. The detailed design and implementation results along with the real system 100 kW test results are presented that verified the applicability of the analysis and proposed methodology for high power applications.

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