# Transformer Shielding Technique for Common Mode Noise Reduction in Switch Mode Power Supplies

Yuchen Yang

Thesis submitted to the Faculty of the Virginia Polytechnic Institute and State University in partial fulfillment of the requirements for the degree of

> Master of Science in Electrical Engineering

Fred C. Lee, Chair Qiang Li Rolando Burgos

May 9<sup>th</sup>, 2014 Blacksburg, Virginia

Keywords: EMI, Common mode noise, Shielding technique, Balance concept

© 2014, Yuchen Yang

# Transformer Shielding Technique for Common Mode Noise Reduction in Switch Mode Power Supplies

Yuchen Yang

### (Abstract)

Switch mode power supplies are widely used in different applications. High efficiency and high power density are two driving forces for power supply systems. However, high *dv/dt* and *di/dt* in switch mode power supplies will cause severe EMI noise issue. In a typical front-end converter, the EMI filter usually occupies 1/3 to 1/4 volume of total converter. Hence, reducing the EMI noise of power converter can help reduce the volume of EMI filter and improving the total power density of the converter.

For off-line switch mode power supplies, DM noise is dominated by PFC converter. CM noise is a more complicated issue. It is contributed by both PFC converter and DC/DC converter. While many researches have focused on reducing CM noise for PFC converter, the CM noise of DC/DC converter still remains a challenge. The main objective of this thesis is provide a solution to have best CM noise reduction for DC/DC converters. The shielding concept and balance concept are combined to propose a novel balance double shielding technique. This method can have an effective CM noise reduction in the circuit level. In addition it is easy to design and implement in the real production. The balance condition is easily controlled and guarantees effective CM noise reduction in mass production. Then, a novel one-layer shielding method for PCB winding transformer is provided. This shielding technique can block CM noise from primary side and also cancel the CM noise from secondary side. In addition, shielding does not increase the loss of converter too much. Furthermore, this shielding technique can be applied to matrix transformer structure. For matrix transformer LLC converter, the inter-winding capacitor is very large and will cause severe CM noise problem. By adding shielding layer, CM noise has been greatly reduced. In addition, by modifying the secondary winding, the loss on shielding layer is minimized and experiments show that the total efficiency of converter has almost no impact.

Furthermore, although this thesis uses flyback and LLC resonant converter as example to demonstrate the concept, the novel shielding technique can also be applied to other topologies that have similar transformer structure.

## Acknowledgments

First I would like to express my sincere gratitude to my advisor, Dr. Fred C. Lee, for his guidance, encouragement, and patience. It is him who guided me to the field of power electronics. It is his extensive knowledge, his rigorous attitude towards research, and his scientific thinking to solve problems that enlightens me as to what makes a superior researcher. Having the opportunity to study with him has been a great honor.

I am also grateful to Dr. Qiang Li, who shares a great amount of knowledge, suggestions, and experience with me. I appreciate his generous help and encouragement. I would like to thank Dr. Rolando Burgos for his valuable guidance during my research.

I would also like to thank all the great staff in CPES: Ms. Teresa Shaw, Ms. Linda Gallagher, Ms. Marianne Hawthorne, Ms. Teresa Rose, Ms. Linda Long, Mr. David Gilham, and Dr. Wenli Zhang.

It is a great pleasure to work with the talented colleagues in the Center for Power Electronics Systems (CPES). Without your help, this work cannot be accomplished. I would like to thank Dr. Dianbo Fu, Dr. Pengju Kong, Dr. David Reusch, Dr. Mingkai Mu, Dr. Yingyi Yan, Dr. Daocheng Huang, Mr. Chanwit Prasantanakorn, Mr. Shu Ji, Mr. Zijian Wang, Mr. Haoran Wu, Mr. Sizhao Lu, Mr. Syed Bari, Mr. Zhongsheng Cao, Mr. Xuebing Chen, Mr. Chao Fei, Dr. Dongbin Hou, Mr. Xiucheng Huang, Mr.Yang Jiao, Mr. Pei-Hsin Liu, Mr. Zhengyang Liu, Ms. Yincan Mao, Mr. Yipeng Su, Mr. Shuilin Tian, Mr. Wei Zhang. I cherish the wonderful time together and the great friendship. With much love and gratitude, I want to thank my parents: my mother Ying Lu and my father Shijun Yang for their endless love, encouragement, and support throughout twenty years of school.

Finally and most importantly, I must thank my wife Zhuxuan Li, whom I love deeply. Your love and encouragement has been the most valuable thing in my life.

Special thanks go out to the CPES PMC mini-consortium members for the funding of my research: Chicony Power, CSR Zhuzhou Institute Co., Ltd., Delta Electronics, Huawei Technologies, International Rectifier, Linear Technology, Macroblock, Inc., Murata Manufacturing Co., Ltd., NEC TOKIN Corporation, NXP Semiconductors, Richtek Technology, Texas Instruments.

# **Table of Contents**

Chapter	1. Introduction1
1.1	Introduction to EMI and EMC1
1.2	EMI measurement
1.3	Conducted EMI noise in switch mode power supplies6
1.4	CM noise reduction methods for switch mode power supplies9
1.5	Thesis outline
Chapter	2. CM noise reduction using balance concept22
2.1	Introduction to balance technique
2.2	CM noise model of flyback converter27
2.3	Double shielding technique using balance concept
2.4	Experimental results
2.5	Summary
Chapter	3. CM noise reduction for resonant converter41
3.1	Introduction41
3.2	Shielding technique for PCB winding transformer to reduce CM noise
3.3	Experimental results
3.4	LLC resonant converter with matrix transformer54
3.5	Shielding technique for matrix transformer57
3.6	Loss analysis of matrix transformer with shielding61
3.7	Summary

Chapter	4. Summary and Future Work	66
4.1	Summary	66
4.2	Future Work	68

Reference 69

# **List of Figures**

Fig. 1.1 EMI standard EN55022 Class B for conducted noise	2
Fig. 1.2 FCC measurement setup	3
Fig. 1.3 Internal circuit of a LISN	4
Fig. 1.4 Practical noise measurement circuit	4
Fig. 1.5 Decision tree for peak detector measurements	5
Fig. 1.6 Structure of low power laptop adapter	6
Fig. 1.7 Front-end converter for server and telecom	7
Fig. 1.8 State-of-the-art front end converter	7
Fig. 1.9 DM noise propagation path	8
Fig. 1.10 CM noise propagation path	8
Fig. 1.11 Topology of flyback converter	
Fig. 1.12 CM Noise source and propagation path of flyback converter	
Fig. 1.13 1:1 transformer to reduce CM noise	
Fig. 1.14 Voltage distribution of primary winding and secondary winding	
Fig. 1.15 Misalignment between primary and secondary windings	
Fig. 1.16 Transformer structure for a flyback adapter	
Fig. 1.17 Voltage distribution of primary winding P3 and secondary winding	
Fig. 1.18 Series Shielding method	
Fig. 1.19 Voltage distribution of P3 and S	
Fig. 1.20 Two layers of shielding in the transformer	
Fig. 1.21 Partial shielding method	
Fig. 2.1 Boost converter with symmetry technique	23
Fig. 2.2 Balanced boost PFC converter	24
Fig. 2.3 Replace the MOSFET with a voltage source	25

Fig. 2.4 CM noise model of balanced boost PFC converter	25
Fig. 2.5 Wheatstone bridge structure	26
Fig. 2.6 Topology of flyback converter	27
Fig. 2.7 Replace the switches by voltage sources	
Fig. 2.8 Parasitic capacitor between drain of MOSFET and ground	29
Fig. 2.9 Transformer structure	
Fig. 2.10 Voltage distribution of primary winding P3 and secondary winding	31
Fig. 2.11 CM noise model of flyback converter	
Fig. 2.12 Double shielding using balance concept	
Fig. 2.13 CM noise model of flyback converter with balance double shielding technique	
Fig. 2.14 Bridge circuit form of CM noise model	
Fig. 2.15 3D structure of transformer with balance double shielding	35
Fig. 2.16 CM noise measurement result for original transformer	
Fig. 2.17 CM noise measurement results with two-layer complete shielding	
Fig. 2.18 CM noise measurement result with balance double shielding	
Fig. 3.1 Topology of LLC resonant converter	
Fig. 3.2 Waveform of v <sub>3</sub>	43
Fig. 3.3 Waveform of v <sub>2</sub>	43
Fig. 3.4 Waveform of v <sub>1</sub>	44
Fig. 3.5 LLC resonant converter with PCB winding on secondary	45
Fig. 3.6 Adding shielding layer between primary and secondary winding	46
Fig. 3.7 Shielding in PCB winding transformer	47
Fig. 3.8 3D structure of shielding and secondary winding	49
Fig. 3.9 Voltage distribution of shielding and secondary winding	49
Fig. 3.10 Shielding cannot block CM noise when connecting wrong point	50
Fig. 3.11 Shielding has 90 °rotation with secondary winding	51

Fig. 3.12 Shielding has 270 °rotation with secondary winding	
Fig. 3.13 CM noise measurement result with shielding	53
Fig. 3.14 Converter efficiency with shielding	54
Fig. 3.15 LLC resonant with matrix transformer	56
Fig. 3.16 Matrix transformer structure	56
Fig. 3.17 Mount secondary devices and output capacitors on top of secondary winding	56
Fig. 3.18 CM noise measurement result for LLC resonant converter with matrix transformer	57
Fig. 3.19 Adding shielding into matrix transformer	58
Fig. 3.20 Transformer structure with shielding	58
Fig. 3.21 3D structure of secondary winding and shielding	60
Fig. 3.22 Voltage distribution of shielding and secondary winding	60
Fig. 3.23 CM noise measurement result for matrix transformer with shielding	61
Fig. 3.24 Current distribution from FEA software	62
Fig. 3.25 Current crowding around gap area	63
Fig. 3.26 Reduce the loss on shielding by adding more capacitor on secondary winding	64
Fig. 3.27 Efficiency comparison between shielding version and original version	64

## **Chapter 1. Introduction**

#### **1.1 Introduction to EMI and EMC**

In a world full of electronic devices, it is very important that these devices can work properly in a complicated electromagnetic environment. Thus, electromagnetic compatibility (EMC) is a significant characteristic of electronic devices. The definition of EMC according to International Electrotechnical Commission (IEC) is "The ability of an equipment or system to function satisfactorily in its electromagnetic environment without introducing intolerable electromagnetic disturbances to anything in that environment."[1]. Nowadays, EMC is becoming more and more important. First, more and more applications are going to be electrified, such as automobile, ship, and aircraft. Every devices in these applications must work properly to assure safety. In addition, recent years have seen a dramatically growth of personal electronic devices. We are facing a more complicated electromagnetic environment that we have never met before. Second, modern electronic devices are more susceptible to electromagnetic disturbances. The lower supply voltage is more easily affected by noises. Higher switching frequency is introducing severe disturbances. Furthermore, the pursuing of power density is making electronic devices closer to each other.

Electromagnetic interference is defined as "degradation of the performance of an equipment, transmission channel or system caused by an electromagnetic disturbance" [2]. There are four methods that the electromagnetic interference can propagate from the noise source to the victim:

- (1) Conducted interference;
- (2) Radiated interference;

(3) Inductive interference;

(4) Capacitive interference.

The conducted interference means the noise propagates through conductors. Radiated interference propagates through the radiation of electromagnetic field. The inductive and capacitive interference combined as the near field coupling propagates from the noise source to the victim.

EMI can cause malfunction of electronic devices, from the annoying cell phone interference to lethal failure of life support equipment in the hospital. In order to avoid those impacts, there are several EMI standards to limit both the conducted and radiated EMI noise, such as FCC part 15 in United States and CISPR 22 in Europe. Fig. 1.1 shows the EN55022 Class B standards for conducted EMI noise.



Fig. 1.1 EMI standard EN55022 Class B for conducted noise

#### **1.2 EMI measurement**

Because of the complexity of EMI propagation path, different measurement setup leads to different result. In order to get a constant measurement condition, EMI standards provide the specified measurement setup. The FCC measurement setup is shown in Fig. 1.2.



Fig. 1.2 FCC measurement setup

Line Impedance Stabilization Network (LISN) is used to guarantee constant measurement condition. Fig. 1.3 shows the internal circuit of a LISN. The main function of LISN is that it provide a stable loop impedance that can get repeatable measurements of the EMI noise. LISN works like a low-pass filter that it can block high frequency noise from the power source and allow low frequency power flow to the Equipment Under Test (EUT). In the real measurement setup, two LISNs are needed to connect between power source and EUT as shown in Fig. 1.4. A spectrum analyzer is connected to one LISN to pick up the total noise while a standard  $50\Omega$  terminator is connected to the other LISN.



Fig. 1.3 Internal circuit of a LISN



Fig. 1.4 Practical noise measurement circuit

There are three different methods to measure EMI noise: peak, average and quasi-peak. The peak detector picks the maximum amplitude of the noise signal for each frequency. The average detector takes an envelope-detected signal and passes it through a low-pass filter with a bandwidth

much less than the resolution bandwidth. The filter integrates (averages) the higher-frequency components such as noise. Quasi-peak detector is a weighted form of peak detection. The measured value of the quasi-peak detector drops as the repetition rate of the measured signal decreases [3].

Detecting average or quasi-peak noise is very time-consuming. To reduce the testing time, the peak detector may be used. Fig. 1.5 shows the decision tree used to determine a final pass/fail judgment [4].



Fig. 1.5 Decision tree for peak detector measurements

#### **1.3** Conducted EMI noise in switch mode power supplies

Switch mode power supplies are widely used in different applications, such as power supply for telecom and server, silver box for desktops, adapter for laptops and charger for personal mobile devices.

Switch mode power supplies is a complicated system and have different structures for different applications. Fig. 1.6 shows the structure of laptop adapter. Because the power is below 75W, it do not need a power factor correction (PFC) circuit. The diode bridge rectifies the AC input voltage to DC voltage. The isolated DC-DC converter converts the DC voltage to 20V DC bus voltage. Then the voltage regulator (VR) module converts the bus voltage to different load voltage and assures the required transient performance.



Fig. 1.6 Structure of low power laptop adapter

For the power supply for server and telecom system, the structure is a little different. Fig. 1.7 shows the structure of front-end converter for server and telecom system. First, the PFC converter rectifies the AC input voltage to 380V DC voltage. Second, the DC-DC converter converts the 380V DC voltage to a 48V/12V DC bus voltage. Then the voltage regulator module will take over.



Fig. 1.7 Front-end converter for server and telecom

Switch mode power supplies never stop pursuing high efficiency and high power density. In order to reach this goal, new semiconductor devices, such as GaN and SiC, are being developed. In addition, circuit topologies, structure and control method continue improving to help make switch mode power supplies smaller, lighter and more efficient.

However, high *dv/dt* and *di/dt* in switch mode power supplies will cause severe EMI noise issue. Hence, EMI filter is always needed in switch mode power supply to attenuate severe conducted EMI noise. Fig. 1.8 shows a state-of-the-art front-end converter for server system. It can be seen that the EMI filter takes about 1/4 to 1/3 volume of total converter. Reducing the noise of power converter can reduce the size and volume of EMI filter and help improving the power density of total converter.



Fig. 1.8 State-of-the-art front end converter

The conducted EMI noise is always decoupled to differential mode (DM) noise and common mode (CM) noise. Because the DM noise and CM noise have different propagation path, they need different attenuation method. Fig. 1.9 shows the propagation path of DM conducted noise. DM noise current  $i_{DM}$  flows between two power lines. Fig. 1.10 shows the propagation path of CM conducted noise. CM noise current  $i_{CM}$  flows between power lines and ground.



Fig. 1.9 DM noise propagation path



Fig. 1.10 CM noise propagation path

According to the EMI standard EN55022, the noise voltage on the 50 $\Omega$  resistor is limited:

$$\begin{cases} v_1 = 50(i_{DM} - i_{CM}) \\ v_2 = 50(-i_{DM} - i_{CM}) \end{cases}$$
(1.1)

 $v_1$  and  $v_2$  both can represent total EMI noise. In the measurement, the amplitudes of  $v_1$  and  $v_2$  are almost identical because  $i_{DM}$  and  $i_{CM}$  are high frequency AC currents [5].

DM noise voltage and CM noise voltage can then be represented as:

$$\begin{cases} v_{DM} = 50i_{DM} = \frac{v_1 - v_2}{2} \\ v_{CM} = -50i_{CM} = \frac{v_1 + v_2}{2} \end{cases}$$
(1.2)

For off-line switch mode power supplies, DM noise is dominated by PFC converter. CM noise is a more complicated issue. It is contributed by both PFC converter and DC/DC converter. A lot researches have been done to reduce the CM noise of PFC converter [6][7][8][9][10]. However, the CM noise of DC/DC converter still remains a challenge.

#### **1.4** CM noise reduction methods for switch mode power supplies

In order to reduce the CM noise filter size, many researches have been done to reduce the CM noise of DC/DC converters. To have a better understanding on the principle of these methods, CM noise sources and its propagation path should first be identified.

Flyback is the most widely used topology in adapter products. Fig. 1.11 shows the flyback topology and the parasitic capacitance that conducts CM noise. The switch performance of primary device can introduce severe voltage pulse dv/dt. The switching of secondary device can also introduce voltage pulse dv/dt. They can be modeled as two voltage sources. There is parasitic capacitance between the primary winding and secondary winding of transformer. It is one major CM noise path. The parasitic capacitance between the drain of primary MOSFET and ground is another CM noise path. The CM noise current is generated by voltage pulse dv/dt on the parasitic capacitance. Fig. 1.12 shows the CM noise source and propagation path of flyback converter.



Fig. 1.11 Topology of flyback converter



Fig. 1.12 CM Noise source and propagation path of flyback converter

The inter-winding capacitance between the primary winding and secondary winding of transformer is a major propagation path of CM noise current. Many researches have been focused on reducing the inter-winding capacitance to reduce the CM noise. In [11], CM noise cancellation is achieved by blocking the displacement current go between primary winding and secondary winding of transformer. Fig. 1.13 (b) shows the proposed transformer structure for a flyback

converter. The technology is described as "The primary winding and secondary winding have the same length, have the same number of turns of wire of the same diameter, and are concentrically disposed on the core in the same axial position. Their winding sense and connection to a primary circuit and a secondary circuit, respectively, are chosen so that correspondingly situated ends of these two coils carry alternating voltages of the same polarity in the operating condition [11]." Fig. 1.14 shows the voltage distribution of the primary and secondary windings. Assuming the voltage distributes linearly along the winding. It can be seen that for a specific point on the primary winding, it shares the same voltage potential as the corresponding point on the secondary winding. Consequently, there is no voltage difference between the primary winding and secondary winding and no displacement current can flow between the primary and secondary windings. Thus the CM noise current flowing through the transformer is blocked.



(a) Flyback circuit topology



(b) Transformer structure

Fig. 1.13 1:1 transformer to reduce CM noise



Fig. 1.14 Voltage distribution of primary winding and secondary winding

However, this method requires that the primary winding and secondary winding must be aligned perfectly. Fig. 1.15 shows that if there is a misalignment between primary winding and secondary winding, the voltage distribution will change. As shown in Fig. 1.15 (b), there will be voltage difference between the primary and secondary winding and this will lead to CM noise current flow through the transformer. The benefit of this technique will be diminished. Because of this, this method is not effective in mass production.



(a) Winding position when misalignment



(b) Voltage distribution of misalignment windings

Fig. 1.15 Misalignment between primary and secondary windings

Another limitation of this method is that it requires the primary and secondary winding using identical number of turns of wire of the same diameter. However, in practice, the turn ratio of the transformer can note be 1:1 in an adapter application. Meanwhile, since the primary and secondary winding have different RMS current flowing through, the diameter of primary and secondary windings should be different. Fig. 1.16 shows a practical design of a flyback converter. The primary winding has three layers and the secondary winding has one layer. The turns ratio is 36:5. There is displacement current between each layer of winding. However, the displacement current flows between primary windings does not contribute to the CM noise current because this current will circulating within the primary side. The CM noise current comes from the displacement current and lumped inter-winding capacitance can then be calculated.

In order to calculate displacement current and lumped inter-winding capacitance, the voltage distribution of primary winding P<sub>3</sub> and secondary winding need to be identified, as shown in Fig. 1.17. N<sub>P3</sub> stands for the number of turns of P<sub>3</sub> layer, N<sub>P</sub> stands for the total number of turns of primary winding and N<sub>S</sub> stands for the number of turns of secondary winding. C<sub>PS</sub> is the total capacitance between primary winding layer P<sub>3</sub> and secondary winding.



Fig. 1.16 Transformer structure for a flyback adapter



Fig. 1.17 Voltage distribution of primary winding P3 and secondary winding

The total displacement current flowing from primary winding to secondary winding can then be calculated as:

$$i = C_{PS} \frac{d}{dt} \frac{v_A}{2N_P} (N_{P3} - N_S)$$
(1.3)

In a practical transformer, there is a large amount displacement current flowing between the primary and secondary windings. This contributes large CM noise current. [12] provides a method to block the CM noise current when the primary winding has much more number of turns than the secondary winding. Fig. 1.18 shows the proposed transformer structure. In this figure, half core of the transformer is implemented into the circuit. The primary winding has three layers and secondary winding has one layer. Instead of using one complete wire as the primary winding, this method breaks the primary winding into two parts. One part is normally winded primary winding P1, P2. The other part P3 is a special winding that is identical with secondary winding but connected in series with the primary winding. The displacement current flows between primary windings does not contribute to the CM noise current because this current will circulating within the primary side. As shown in Fig. 1.19 there is no voltage difference between the special primary winding P3 and the secondary winding. Consequently, there is no CM noise current flowing through the transformer.



Fig. 1.18 Series Shielding method



Fig. 1.19 Voltage distribution of P3 and S

This method is an improvement of [11]. However, it shares the similar limitations with [11]. This method also requires that the special primary winding must be identical with secondary winding and two windings should be aligned perfectly. Hence, this method cannot be very effective in mass production. In [13], a shielding method is provided to better block the CM noise current flowing through the transformer. Fig. 1.20 shows its transformer structure. Two layers of copper shielding are added between the primary and secondary winding of transformer. One layer is connected to the primary ground and the other layer is connected to the secondary ground. The displacement current flowing from primary winding to Shielding 1 will be confined in the primary side. Similarly, the displacement current flowing from secondary winding to Shielding 2 will be confined in secondary side. These current will not cause CM noise issue. Also, there is no voltage difference between two copper shielding. Hence the CM noise current is blocked. And it is easy to make these two copper shielding layer identical in mass production.



Fig. 1.20 Two layers of shielding in the transformer

This method can effectively block the CM noise current flowing through the transformer. However, it has limitation too. As shown in Fig. 1.20, the parasitic capacitance  $C_{AG}$  provides another CM noise path. All the previous methods cannot reduce this part of CM noise. In [14], a shielding method is provided that can reduce CM noise flowing through both the transformer and parasitic capacitor  $C_{AG}$ . Fig. 1.21 shows its transformer structure. Instead of using a shielding that blocking the whole winding area, it reduces the shielding width and leaves a non-shielded area. In non-shielded area, the voltage of primary winding is higher than secondary winding. Displacement current  $i_1$  flows from primary to secondary. In the shielded area, the voltage of secondary winding is higher than shielding, so the displacement current  $i_2$  flows from secondary to primary. Also, there is another current  $i_3$  flows through parasitic capacitor  $C_{AG}$ . By controlling the width of shielding, the three current can cancel each other (1.4) that there is no net CM noise current.

$$i_1 + i_2 + i_3 = 0 \tag{1.4}$$



Fig. 1.21 Partial shielding method

However, in the real production, the optimal width of shielding is obtained by trial-and-error procedure and requires a lot effort. In addition, this method requires a precise control on the relative

position of windings and shielding. However, it is hard to guarantee this for every transformer in the real production and will diminish the effect on the CM noise reduction.

#### 1.5 Thesis outline

The main objective of this thesis is to analyze the CM noise characteristic for isolated DC/DC converters. Then provides a system approach to minimize the CM noise while not impacting circuit performance.

The first chapter introduces background knowledge of EMI related issues. In off-line applications, isolated DC/DC converter generates most CM noise. In order to attenuate the noise, large EMI filter is needed and this reduces the system power density. Then the review of previous CM noise reduction method for isolated DC/DC converters is provided. However, those method cannot achieve best CM noise reduction and its effect is diminished during mass production. The challenge for CM noise reduction is achieving good CM noise reduction for the whole frequency range and the parasitics should be easily controlled in real production to guarantee the enough CM noise reduction.

In Chapter 2, the general balance concept is introduced. The balance technique can effectively reduce the CM noise while not increasing the complexity of the circuit. Then, CM noise model of flyback converter, a popular topology for isolated DC/DC converter, is discussed. The main propagation paths of CM noise current are inter-winding capacitor of the transformer and parasitic capacitor between the drain of MOSFET and ground. Then, the double shielding technique using balance concept is provided to reduce CM noise. By using this method, the CM noise can be minimized in system level. Furthermore, this method is easy to design and implement in the real

production. The balance condition is easily controlled and guarantees effective CM noise reduction in mass production.

In Chapter 3, CM noise characteristic of resonant converter is discussed. Then a novel onelayer shielding method for PCB winding transformer is provided. After implementing the shielding layer, the primary and secondary windings of transformer is completely isolated and assures that no CM noise current will flow through the transformer. In addition, shielding does not impact the performance of the converter, the total efficiency is almost the same as the original version. Next, matrix transformer is introduced and a LLC converter using matrix transformer is used as an example. The shielding method is applied to the matrix transformer and have good CM noise reduction. After optimizing the winding structure, the loss on shielding can be minimized and total efficiency of the converter is not impacted by shielding layer.

Chapter 4 is conclusions with the summary and the future work.

### Chapter 2. CM noise reduction using balance concept

As shown in previous chapter, CM noise of DC/DC converter is a very serious problem. Many methods have been raised to reduce the CM noise of DC/DC converter. However, there is no solution that can reduce the CM noise for all important paths and still effective in mass production. In [7][8][9][10], balance technique is provided to solve CM noise issue for PFC converters. This chapter tries to combine the shielding technique and balance concept to provide a novel method that can effectively reduce CM noise for isolated DC/DC converter. CM noise model and shielding design consideration is provided. Experiment result verifies the validity of this method.

#### 2.1 Introduction to balance technique

CM noise current is formed by severe dv/dt on parasitic capacitance, as shown in (2.1). Before the balance technique was proposed, several methods had been provided to reduce CM noise by introducing another dv/dt source to cancel the previous one [15][16][17][18][19][20][21][22].

$$i_{CM} = C_{para} \frac{dv}{dt} \tag{2.1}$$

In [22], CM noise is cancelled by achieving symmetrical circuit topology. Fig. 2.1 demonstrates the symmetrical boost topology versus a conventional boost topology [22]. The original boost inductor L is split into two identical coupled inductor L<sub>1</sub> and L<sub>2</sub>. In addition, another diode D2 is introduced. Thus, another dv/dt source is introduced and it has the same amplitude and opposite polarity with node A. The parasitic capacitor C<sub>d1</sub> and C<sub>d2</sub> is controlled to be the same value. Hence, the CM noise current flowing through C<sub>d1</sub> and C<sub>d2</sub> has the same amplitude but out-

of-phase. Consequently, there is no net CM noise current flowing to the ground and CM noise has been cancelled.



(a) Conventional boost converter



(b) Symmetrical boost converter

Fig. 2.1 Boost converter with symmetry technique

Although the experiment shows significant CM noise reduction, symmetry technique has its own limitation. Most popular topologies are not symmetrical structure. In order to achieve symmetry, additional components is required to be added in the circuit, such as diodes, power switches and windings. This will make the converter more complicated and introduces extra loss and higher cost. It sacrifices too much to reduce CM noise, which is not applicable in commercial products. In order to have good CM noise reduction without extra loss, balance technique is provided [7]. As shown in Fig. 2.2, the inductor is split in to L1 and L2, but there is no need to add another diode into the converter.  $C_d$  is the parasitic capacitance between MOSFET drain and ground.  $C_a$  is the parasitic capacitance between the cathode of diode D, large area of output traces, load and the ground.  $C_c$  is the parasitic capacitance between load, large area of output traces and the ground.



Fig. 2.2 Balanced boost PFC converter

According to the substitution theorem, if the MOSFET branch is substituted by a voltage source  $V_{AC}$  having the same voltage as the original branch, the circuit behavior keeps the same. Hence, the MOSFET can be replaced by a voltage source  $V_{AC}$ , as shown in Fig. 2.3.



Fig. 2.3 Replace the MOSFET with a voltage source

In the CM noise frequency range, the input and output capacitor can be treated as short circuit. In addition, the diode bridge can also be treated as short circuit since it is always conducting current. Thus, the CM noise model of this boost PFC converter is shown in Fig. 2.4.



Fig. 2.4 CM noise model of balanced boost PFC converter

It can be seen that this CM noise model is a Wheatstone bridge circuit. In a general Wheatstone bridge structure shown in Fig. 2.5, if the balance equation (2.2) is satisfied, point B and point D have identical voltage and there is no current going outside this circuit.



Fig. 2.5 Wheatstone bridge structure

$$\frac{Z_1}{Z_2} = \frac{Z_3}{Z_4}$$
 (2.2)

Thus, for the CM noise model of boost PFC converter in Fig. 2.4, as long as the balance equation (2.3) is satisfied, there is no CM noise current generated by converter going through LISN.

$$\frac{Z_{L1}}{Z_{L2}} = \frac{Z_{Cd}}{Z_{Ca+Cc}} \tag{2.3}$$

In contrast to the symmetry technique, this ratio in the balance technique do not need to be only 1:1. The impedance ratio can be any value as long as the balance condition is satisfied, CM noise can be cancelled. Hence, the balance technique offers additional freedom to the designer to choose the impedance ratio according to the converter design. Furthermore, balance technique do not require additional components in the circuit. This will not increase the complexity of the
converter and will not increase the cost and loss while has significant CM noise reduction, which is preferred in the commercial products.

# 2.2 CM noise model of flyback converter

According to previous analysis, a valid CM noise model is prerequisite for developing an effective CM noise reduction method. Flyback is a very popular topology for the DC/DC converter in off-line applications. In this chapter, flyback converter is used as an example to illustrate the novel CM noise reduction method.

Fig. 2.6 shows the topology of flyback converter. It has only one switch and one diode. Due to its simplicity, flyback converter is widely used as isolated DC/DC converter in low power switching mode power supplies. Because the CM noise is generated by voltage pulse dv/dt on the parasitic capacitance, it is necessary to first identify the noise sources in flyback converter. The switching performance of primary power switch can generate severe voltage pulse dv/dt. The primary power switch can then be modeled as a voltage source. Similarly, secondary diode can also be modeled as a voltage source since it generate voltage pulse dv/dt on the secondary side.



Fig. 2.6 Topology of flyback converter

As shown in Fig, the switch components have been replaced by voltage sources, next step is to identify the CM noise path, which is the parasitic capacitance that conduct CM noise current. One major CM noise current path is the parasitic capacitance between the drain of MOSFET and ground. As shown in Fig. 2.8, there is parasitic capacitor between the drain pad of MOSFET and the heat sink attached to it. Because the heat sink is connected to ground, this parasitic capacitor is becoming a major path of CM noise current.



Fig. 2.7 Replace the switches by voltage sources



Fig. 2.8 Parasitic capacitor between drain of MOSFET and ground

Another important CM noise current path is the inter-winding capacitance between the primary winding and secondary winding of transformer. Through this inter-winding capacitor, the CM noise current can be transferred from the primary side to secondary side and go to ground. However, the inter-winding capacitor is discrete stray capacitance, it is inconvenience to directly use it in the CM noise model. Hence, a lumped capacitor is required to represent the original discrete capacitor.

The basic idea of lumped capacitor is getting a lumped capacitor that the displacement current flowing from primary side to secondary side through the lumped capacitor is identical with the displacement current flowing from primary winding to secondary winding through original discrete stray capacitor. The lumped capacitor value is highly depended on the transformer structure.

Fig. 2.9 shows a typical transformer structure. The primary winding has three layers, secondary winding has one layer. Both primary and secondary windings are winded by wires. There is parasitic capacitance between each layer of the transformer. Because the voltage is

different between each layer, there will be displacement current flowing between different layers. However, the displacement current flows between primary winding layers does not contribute to CM noise current because this current is confined in primary side. Only the displacement current flowing between primary winding and secondary winding contributes CM noise current.



Fig. 2.9 Transformer structure

In order to get the lumped capacitor between primary and secondary side, the total displacement current flowing between primary and secondary windings should first be calculated. Voltage distribution of primary winding  $P_3$  and secondary winding is identified in Fig. 2.10.  $N_{P3}$  stands for the number of turns of  $P_3$  layer,  $N_P$  stands for the total number of turns of primary winding and  $N_S$  stands for the number of turns of secondary winding.  $C_{PS}$  is the total discrete stray capacitance between primary winding layer  $P_3$  and secondary winding.



Fig. 2.10 Voltage distribution of primary winding P3 and secondary winding

The total displacement flowing from primary winding to secondary winding can then be calculated as:

$$i = C_{PS} \frac{d}{dt} \frac{v_A}{2N_P} (N_{P3} - N_S)$$
(2.4)

The lumped inter-winding capacitance can be derived as:

$$C_{AC} = \frac{N_{P3} - N_S}{2N_P} C_{PS} \tag{2.5}$$

Fig. 2.11 shows the CM noise model of flyback converter with lumped capacitor. The current will flow from primary side through  $C_{AC}$  and  $C_{AG}$  to secondary side. This current will cause CM noise issue. In order to reduce CM noise using balance technique, another capacitor  $C_{BD}$  is needed.



Fig. 2.11 CM noise model of flyback converter

## 2.3 Double shielding technique using balance concept

Balance technique is widely used in reducing CM noise for PFC converters. This technique can also be applied to isolated DC/DC converters to reduce CM noise. As shown in Fig. 2.11, the CM noise model of flyback converter does not look like a bridge circuit. It only has one branch of the bridge. In order to form a Wheatstone bridge circuit, another capacitor is needed to connect point B and point D. This can be achieved by adding the proposed shielding between primary winding and secondary winding of transformer.

Fig. 2.12 shows the proposed shielding structure. Two layers of shielding is added between the primary winding and secondary winding of transformer. Each shielding has been divided into two parts, the upper part and the lower part. For the left layer of shielding, the upper part is connected to point A, the lower part is connected to point B. the right layer of shielding, the upper part is connected to point C and the lower part is connected to point D. Thus the upper part of shielding forms a capacitor connecting point A and point C. The lower part of shielding forms a capacitor connecting point B and point D. The CM noise model is shown in Fig. 2.13.



Fig. 2.12 Double shielding using balance concept



Fig. 2.13 CM noise model of flyback converter with balance double shielding technique

This CM noise model can be redrawn as the bridge circuit shown in Fig. 2.14. However, this is not the typical Wheatstone bridge structure. It has voltage sources in the branches. Although it

cannot achieve impedance balance, it is possible to achieve a more general balance condition in the voltage sense. That is, the voltage potential of point X and point Y should be identical. Thus there is no net CM noise current flowing outside the circuit.



Fig. 2.14 Bridge circuit form of CM noise model

The balance condition is derived in (2.6). In order to achieve the balance condition, the value of  $C_{BD}$  and  $C_{AC}$  need to be controlled.

$$\frac{dv_A/dt}{dv_D/dt} = \frac{C_{BD}}{C_{AC} + C_{AG}}$$
(2.6)

The 3D structure of the transformer with balance double shielding is shown in Fig. 2.15.  $C_{BD}$  and  $C_{AC}$  is formed by two shielding layers. They can be treated as coaxial cylinder capacitor, as shown in Fig. 2.15. The capacitance can then be calculated as:

$$C_{BD} = \frac{2\pi\varepsilon l_1}{\ln(R_2/R_1)} \tag{2.7}$$

$$C_{AC} = \frac{2\pi\varepsilon l_2}{\ln(R_2/R_1)} \tag{2.8}$$



Fig. 2.15 3D structure of transformer with balance double shielding

Furthermore, if the distance between two shielding layers are much smaller than the radius of the shielding:  $d = R_2 - R_1 \ll R_1$ ,  $R_2$ . Then,

$$ln\frac{R_2}{R_1} = \ln(1 + \frac{d}{R_1}) \approx \frac{d}{R_1}$$
(2.9)

The capacitance can then be derived as

$$C_{BD} \approx \frac{2\pi\varepsilon l_1 R_1}{d} = \frac{\varepsilon S_1}{d}$$
(2.10)

$$C_{AC} \approx \frac{2\pi\varepsilon l_2 R_1}{d} = \frac{\varepsilon S_2}{d}$$
(2.11)

 $C_{BD}$  and  $C_{AC}$  can then be treated as parallel-plate capacitors. This further simplifies the calculation. For a specific transformer, the total length and the perimeter of the shielding is fixed. In order to adjust the capacitance of  $C_{BD}$  and  $C_{AC}$ , the distance between two shielding layers and the position of the gap between the upper shielding and lower shielding can be controlled.

In the real implementation, flexible printed circuit board material can be used to build the two shielding layers. One type of flexible printed circuit board material is polyimide double sided copper clad laminate. It is easy to cut or etch the gap on the copper layers while keep the insulation layer complete. Thus the total two shielding layers is formed in one piece flexible printed circuit board material and it is easy to implement the shielding into the transformer.

One benefit of this novel shielding technique is that the capacitance of  $C_{AC}$  and  $C_{BD}$  is easy to be calculated and controlled since  $C_{AC}$  and  $C_{BD}$  is formed by two layers of copper. In addition, once the shielding is built by flexible printed circuit board material, the relative position of each part of shielding is fixed. It assures that this method is still valid in mass production since the tolerance can easily be controlled. Another benefit of this shielding technique is that it is independent of the transformer structure. The capacitance of  $C_{AC}$  and  $C_{BD}$  is only controlled by the shielding structure. The deviation of the transformer winding production cannot impact the effectiveness of balance technique.

### 2.4 Experimental results

A 65W flyback adapter is used to verify the proposed balance shielding method. The measurement is done in the EMI chamber with 110V AC input and full load condition. According to the standard EN55022, LISN is connected to the input of the converter and Agilent EMC 7402A EMC analyzer is used to measure the EMI. The CM noise is separated from the total EMI noise using the noise separator proposed in [23]. The CM noise is measured in peak mode.

The original CM noise of flyback converter is first measured. There is no shielding or other CM noise reduction method applied to the original converter. The measured CM noise is shown in Fig. 2.16. It has a relatively high CM noise level in the 150kHz to 30MHz frequency range.



Fig. 2.16 CM noise measurement result for original transformer

The two layer complete shielding method [13] is first applied to the transformer to set a bench mark. The result of this method is shown in Fig. 2.17. The CM noise has been effectively reduced by 30dB.



Fig. 2.17 CM noise measurement results with two-layer complete shielding

Then the balanced double shielding method is applied in the transformer. The CM noise measurement result is shown in Fig. 2.18. The CM noise is reduced by almost 50dB. The balanced double shielding method has more CM noise reduction than two layer complete shielding method. It is because for the two layer complete shielding, it can only block the CM noise through the transformer and it cannot reduce the CM noise through parasitic capacitor  $C_{AG}$ . While for the balance double shielding method, it can cancel the CM noise both flowing through the transformer and flowing through parasitic capacitor  $C_{AG}$ . The experiment verifies the effectiveness of the proposed shielding method.



Fig. 2.18 CM noise measurement result with balance double shielding

## 2.5 Summary

This chapter introduces the balance technique for PFC converter. Then the shielding concept and balance concept are combined to propose a novel double shielding technique. This method can have an effective CM noise reduction in the circuit level. In addition, by using this method, the parasitic capacitance which impact CM noise is easy to be calculated and controlled. It makes this method suitable to real mass production that the tolerance of the parasitics can be controlled and the error on transformer winding production will not impact the balance condition. Although this chapter uses flyback converter to illustrate the proposed shielding method, the balanced double shielding technique can be applied to different converter topologies. By using this method, the bridge circuit can always be build and the balance condition can be achieved by adjust the shielding structure. Hence, this method has a very wide range of applications.

# Chapter 3. CM noise reduction for resonant converter 3.1 Introduction

People always want the power supply to be smaller and more efficient. That makes the power density and efficiency are the two major driving forces for power supply systems [24][25].

Pulse-width modulation (PWM) converters is widely used in front-end DC/DC converters. However, because of the hard switching performance, the switching loss is large in PWM converters. This limits the efficiency of PWM converters and impedes the converter going to high switching frequency. Hence, it is hard for PWM converter to achieve high power density and high efficiency. Soft switching technique can make PWM converter achieve zero voltage switching (ZVS). So the switching loss of PWM converter can be reduced and it has the ability to go to high switching frequency to improve power density. However, another disadvantage of PWM converter still limits its performance. For the computing electronic systems, such as desktop, laptop, server and telecom applications, certain hold-up time is required to assure data security. Normal PWM converters require bulky hold up capacitors to guarantee the hold-up time. Thus the power density of PWM converters are still limited.

LLC resonant converter, as shown in Fig. 3.1, is becoming more and more popular because of the high efficiency and high power density [26][27][28][29][30][31][32][33]. LLC resonant converter can achieve ZVS for primary side switches from zero to full load range. Meanwhile, the secondary side synchronous rectifier (SR) can achieve zero current switching (ZCS). Because of this, the switching loss of LLC resonant converter can be minimized and high efficiency can be achieved. In addition, low switching loss provides the LLC resonant converter the ability to achieve high switching frequency. This can continue reduce the size of passive components and

improve power density. Furthermore, it is easy to integrate magnetic components into the transformer to further reduce size and cost of LLC resonant converter. In addition, the voltage gain characteristic of LLC resonant converter makes it have good hold-up capability to reduce the volume of hold-up capacitor. In summary, LLC resonant converter is becoming dominant in off line power supply systems.



Fig. 3.1 Topology of LLC resonant converter

In order to study the CM noise of LLC resonant converter, the noise source and propagation path should first be identified. As shown in Fig. 3.1, there are three dv/dt sources in the primary side:  $v_1$ ,  $v_2$  and  $v_3$ ; two dv/dt sources in the secondary side:  $v_{51}$  and  $v_{52}$ . Same as other isolated DC/DC converters, the inter-winding capacitor between primary winding and secondary winding of the transformer is the major CM noise path and will lead to high CM noise current. The secondary noise sources  $v_{51}$  and  $v_{52}$  has identical amplitude with opposite direction. Hence the CM noise current generated by  $v_{51}$  and  $v_{52}$  will cancel each and  $v_{51}$  and  $v_{52}$  together will not cause CM noise problem.

The dominant CM noise source is  $v_3$ , its waveform is shown in Fig. 3.2. It has very short rising and falling time and ringing. This will introduce severe dv/dt over the inter-winding capacitance and leads to large CM noise current.



Fig. 3.2 Waveform of v<sub>3</sub>

However, if Lr is integrated into the transformer as leakage inductance, the dominant CM noise source becomes  $v_2$ . The waveform of  $v_2$  is shown in Fig. 3.3. It is the sum of  $v_1$  and capacitor voltage  $v_{Cr}$ . The waveform of  $v_1$  is shown in Fig. 3.4. It is generated by the switching performance of primary side switches. Because of the ZVS of primary switches,  $v_1$  has slower rising and falling time without overshoot and ringing. And the voltage on Cr is sine wave. Hence  $v_2$  has slow rising and falling time and no ringing. This will reduce the high frequency CM noise of the converter.



Fig. 3.3 Waveform of v<sub>2</sub>



Fig. 3.4 Waveform of v<sub>1</sub>

As mentioned before, the inter-winding capacitance is the major CM noise current path and its value determines the amplitude of CM noise. In high frequency, high power density LLC resonant converter, PCB winding transformer is widely used. The PCB winding transformer is easily built in an automatic manufacturing process [34]. In addition, the PCB winding transformer can achieve high power density and low profile. Thus, the PCB winding transformer has a large area of copper winding and will have large inter-winding capacitance. This will leads to severe CM noise problem for converter has PCB winding transformer.

#### 3.2 Shielding technique for PCB winding transformer to reduce CM noise

One design of LLC converter using PCB winding transformer is shown in Fig. 3.5. Primary winding has two series connected winding Pri1 and Pri2 using litz wire. Secondary winding is implemented by four-layer PCB board. For each half of the center-tap structure, the secondary winding has two one turn PCB windings in parallel. The four-layer PCB secondary winding is in the middle layers and two primary windings are on the outer layers, which forms an interleaving structure. This can reduce leakage inductance and AC winding resistance.



(a) LLC resonant converter structure



(b) Cross section view of transformer structure

Fig. 3.5 LLC resonant converter with PCB winding on secondary

However, good interleaving between primary and secondary windings will introduce large inter-winding capacitance and severe CM noise current. In order to reduce the CM noise, a shielding method is provided for PCB winding transformers.

As shown in Fig. 3.6, because of the interleaving structure, shielding layers Shielding1 and Shielding2 are added between Pri1 and Sec1, Pri2 and Sec2. Shielding1 and Shielding2 also form a center tap structure and both connected to primary ground. Because of this, CM noise current

flowing between primary winding and shielding layer will be confined in primary side and will not contribute to CM noise.



(a) Circuit structure with shielding



(b) Transformer structure with shielding

Fig. 3.6 Adding shielding layer between primary and secondary winding

As shown in Fig. 3.7, the primary side is on the left part of converter and secondary side is on the right part of converter. Shielding layer, which is made by copper foil, is rotated 180 ° with secondary winding to have an easy connection with primary ground. Thus, there will be voltage

difference between shielding layer and secondary winding. However, this voltage difference will not diminish shield effect and introduce CM noise current.



(b) Shielding has a 180 ° rotation with secondary winding

Fig. 3.7 Shielding in PCB winding transformer

Fig. 3.8 shows 3D structure of shielding and secondary winding. Point C, E, C' and E' are marked in Fig. 3.6 (a), and point E' on shielding layer is connected to primary ground. In order to

analyze the displacement current flowing between shielding layer and secondary winding, the voltage distribution needs to be described. Shielding layer can be treated as a one-turn winding. There will be voltage induced on the shielding layer according to Faraday's Law. An X-Y coordinate system is built to analyze the voltage distribution of shielding layer and secondary winding. Zero point is set between point C and point E on secondary winding. The X axis is built along the winding and representing the position of certain point on the winding. The Y axis indicates the voltage potential of certain point. Fig. 3.9 shows the voltage distribution of shielding layer and secondary winding. One assumption is made that the voltage is linearly distributed along the winding. For secondary winding, from point C to point E the voltage decreases from V to 0. For shielding layer, because the zero point is set in the middle of shielding, at zero point, the voltage on shielding is V/2. First, the voltage on shielding decreases linearly from V/2 to 0. Then, at point C', the voltage is V and decreases to V/2. It can be seen that on one half, the voltage of secondary winding is higher than shielding. The displacement current flows from secondary winding to shielding. On the other half, the voltage of shielding is higher than secondary winding. The displacement current flows from shielding to secondary winding. Those two currents have same amplitude and opposite direction. Thus, there is no net CM noise current flowing out of the transformer. In summary, the function of shielding is: (1) it blocks the displacement current from primary side; (2) the displacement current between shielding and secondary winding will not generate CM noise current.



Fig. 3.8 3D structure of shielding and secondary winding



Fig. 3.9 Voltage distribution of shielding and secondary winding

However, if point C' on the shielding layer is connected to primary ground, the shielding technique cannot have CM noise reduction effect. As shown in Fig. 3.10, the voltage induced on shielding layer is always negative. Hence, the voltage on secondary winding is always higher than shielding layer. There will be severe CM noise current flowing from secondary winding to shielding and then going to primary side. Thus, shielding cannot block CM noise current in the transformer.



(c) Voltage distribution of shielding and secondary winding

Fig. 3.10 Shielding cannot block CM noise when connecting wrong point

The rotation angle between shielding layer and secondary winding do not need to exactly 180 °. Fig. 3.11 and Fig. 3.12 demonstrate the 90 ° rotation and 270 ° rotation respectively. As shown in Fig. 3.11, the shielding layer has a 90 ° rotation with secondary winding. The same X-Y coordinate is built. Same as previous analysis, from point C to point E, the voltage on secondary winding linearly decreases from V to 0. However, at zero point, the voltage on shielding is 3/4 V and decreases to 0. Then, from point C', the voltage decreases from V to 3/4 V. The amount of current flowing from secondary winding to shielding layer can be calculated as (3.1). C<sub>ssh</sub> is the total capacitance between secondary winding and shielding. L is the length of winding. Similarly, the amount of current flowing from shielding layer to secondary winding can be calculated as (3.2). Those two current are equal to each other. Hence there is no net CM noise current flowing out of the transformer. It is the same with 270 °rotation condition.

$$i_1 = \int_0^{3/4} \frac{C_{ssh}}{L} \frac{d(\frac{1}{4}v)}{dt} dl = \frac{3}{16} C_{ssh} \frac{dv}{dt}$$
(3.1)

$$i_2 = \int_{3/4}^1 \frac{C_{ssh}}{L} \frac{d(\frac{3}{4}v)}{dt} dl = \frac{3}{16} C_{ssh} \frac{dv}{dt}$$
(3.2)



(a) 3D structure of shielding and secondary winding



(b) Voltage distribution of shielding and secondary winding

Fig. 3.11 Shielding has 90 °rotation with secondary winding



(a) 3D structure of shielding and secondary winding



(b) Voltage distribution of shielding and secondary winding

Fig. 3.12 Shielding has 270 °rotation with secondary winding

The rotation angle does not impact the effectiveness of CM noise reduction. Hence in a specific design, the rotation angle can be selected according to the PCB layout. This gives the designer more freedom in designing the transformer.

## **3.3 Experimental results**

A 300W, 400V to 12V LLC resonant converter is used as an example to verify the theory. Shielding is added between primary and secondary winding using thin copper foil. The measurement CM noise comparison is shown in Fig. 3.13. It can be seen that the proposed shielding technique has good CM noise reduction and it is still effective at high frequency range.



Fig. 3.13 CM noise measurement result with shielding

However, it is a concern that shielding may introduce extra loss and reduce the efficiency of the converter. Fig. 3.14 shows the efficiency comparison between shielding version and non-shielded version. After adding shielding layers, the efficiency of converter drops less than 0.5%, it is almost the same with the original non-shielded version. In summary, the shielding technique has good CM noise reduction result while little sacrifice of efficiency.



Fig. 3.14 Converter efficiency with shielding

#### **3.4** LLC resonant converter with matrix transformer

The matrix transformer is defined as an array of elements interwired so that the whole functions as a single transformer [35][36]. Each element being a single transformer that contains a set turns ratio, i.e. 1:1, 2:1 ....n:1. The desired turns ratio is obtained by connecting the primary windings of the elements in series and the secondary's in parallel. For the high current design cases only a single turn secondary will be considered. The benefits of the matrix transformer are that it can split current between secondary windings connected in parallel, reduce leakage inductance by lowering the N<sup>2</sup> value of the secondary loop inductance, and improve thermal performance by distributing the power loss throughout the elements [37]. In addition, the matrix transformer structure also can effectively reduce the magnetomotive force (MMF) of the windings, especially for the PCB winding. That also means a reduction in leakage inductance and winding AC

resistance [38]. This makes the matrix transformer a very attractive structure for high current, high switching frequency applications.

Fig. 3.15 shows a design of 400V/12V, 1kW LLC resonant converter with matrix transformer [38]. The switching frequency of this converter is 1MHz. It uses GaN devices as primary switches to reduce switching related loss [39][40]. By utilizing flux cancellation method [34], this converter uses two U-I cores for four sets of transformers. Comparing with normal design, this can reduce the core loss and core size by more than 30% [38]. For each small cell of transformer, the primary winding has four turns and secondary winding has two one-turn center-tap structure. The primary windings are in series and secondary windings are in parallel. Hence, the total turns ratio is 16:1. As shown in Fig. 3.16, by using matrix transformer structure, four-layer PCB can achieve 16:1 turns ratio. Primary windings are at the two middle layers and secondary windings are at top and bottom layers. Thus, secondary SR devices and output capacitors can be directed mounted on top of the secondary winding, as shown in Fig. 3.17. By doing this, there is no extra termination loss. The primary and secondary windings are exactly overlapped.

This LLC resonant converter can achieve more than 95% efficiency and 710W/in<sup>3</sup> power density, which is comparable with the state-of-the-art industry product.



Fig. 3.15 LLC resonant with matrix transformer



Fig. 3.16 Matrix transformer structure



Fig. 3.17 Mount secondary devices and output capacitors on top of secondary winding

## 3.5 Shielding technique for matrix transformer

Matrix transformer brings a lot of benefits. However, there is always a price to pay. In the matrix transformer, the winding area is large, which can introduce large inter-winding capacitance. Furthermore, because of the interleaving structure, the inter-winding capacitance is further increased. This large inter-winding capacitance between primary and secondary windings will bring large CM noise current. As shown in Fig. 3.18, the measured CM noise of LLC converter is way above the EMI standard. Large CM noise filter is needed to achieve the required EMI noise level. The high power density may be diminished by huge CM noise filter.



Fig. 3.18 CM noise measurement result for LLC resonant converter with matrix transformer

In this section, a shielding method is provided for matrix transformer to reduce CM noise. Fig. 3.19 shows the circuit structure after adding shielding layers between primary and secondary windings. Fig. 3.20 shows the cross section view of transformer with shielding layers. Shielding

layer is added between each primary-secondary cell. Thus, the transformer need six layers of PCB after adding shielding. It can be seen from Fig. 3.19 that all shieldings are connected to the primary ground. Thus, the noise current coming from primary side will be blocked by shielding and confined in the primary side. This noise current will not cause CM noise.



Fig. 3.19 Adding shielding into matrix transformer



Fig. 3.20 Transformer structure with shielding

However shielding, treated as a one-turn winding, becomes another voltage pulse source. Therefore the shielding need to be carefully designed otherwise there will be CM noise current between shielding and secondary winding. One shielding-Sec. winding is used as an example to illustrate the shielding design. As shown in Fig. 3.21, Secondary winding is on top of the shielding, and node A, B, A', B' is noted in Fig. 3.19. Shielding is rotated 180 degree with secondary winding to have an easy connection to primary ground. Assuming voltage is distributed linearly along the winding, Fig. 3.22 Voltage distribution of shielding and secondary winding shows the voltage distribution of shielding and sec. winding. The coordinate is build: set zero on point A and the xaxis is along the winding; y-axis is the voltage of each point on the winding. For secondary winding, node A is the dv/dt point and node B is connected to the ground. Hence from A to B, the voltage distributes from V to 0. For shielding, node B' is connected to ground, and the zero point of the axis is at the middle point of shielding. Hence the voltage of shielding first distributes from V/2 to 0, then jump to V (node A') and decrease to V/2. It can be seen that on one half, the voltage of secondary winding is higher than shielding. There is displacement current go from secondary winding to shielding. On the other half, the voltage of shielding is higher than secondary winding. There is displacement current go from shielding to secondary winding. These two current are at the same magnitude but has opposite direction. Therefore, displacement current is circulating within shielding and secondary winding. Therefore, the shielding is designed to not only block the primary noise source, but also block the noise from secondary side.



Fig. 3.21 3D structure of secondary winding and shielding



Fig. 3.22 Voltage distribution of shielding and secondary winding

The experiment result is shown in Fig. 3.23. For an easy observation, the peak points are connected as the envelope. It can be seen that the proposed shielding technique can have a 23dB reduction at 1MHz. Further, the shielding is still effective at very high frequency range.



Fig. 3.23 CM noise measurement result for matrix transformer with shielding

## 3.6 Loss analysis of matrix transformer with shielding

Again, loss is still a concern after shielding layers are implemented in the transformer. In this section, Finite Element Analysis (FEA) software is used to study the loss of matrix transformer with shielding.

At first, shielding layer uses 4oz copper as other transformer windings. However, the FEA simulation shows that the winding loss has a 13% increase, from 9.18W to 10.39W. Since shielding do not need to conduct large amount of current, to reduce the extra loss, shielding layer is reduced to 1oz copper. The total winding loss reduces to 9.70W. However, from the current density distribution Fig. 3.24, there is severe current crowding in the shielding layer. Because the symmetrical structure, only top three layers of the transformer is shown. The severe current crowding will cause significant loss on shielding layer.



Fig. 3.24 Current distribution from FEA software

Fig. 3.25 explains the reason that current crowds in shielding layer. Generally, the on lower part of secondary winding, current flows from left to right. Meanwhile, on lower part of primary winding, current flows from right to left. The flux generated by these two opposite direction current will cancel each other so that there is no eddy current in the shielding layer. However, as shown in Fig. 3.25, two gaps occurred in the lower part of secondary winding. The current flows vertically
near the gap area. Thus, the flux generated by secondary winding and primary winding cannot be cancelled on the shielding. The flux on the shielding layer will generate eddy current and will bring extra loss.



Fig. 3.25 Current crowding around gap area

One solution to this problem is adding more capacitors on the secondary winding to fill the gap. As shown in Fig. 3.26, several capacitors are added to the secondary winding to fill the left gap. The simulation results shows that the current crowding has been reduced a lot in the circled area, which is corresponded to the left gap. After filling the gap, the current on the secondary winding will flow from left to right. Thus, the flux can be cancelled on the shielding layer and reduce the eddy current. The simulation result shows that after modification on the secondary winding, the total winding loss is 9.24W, which is very close to without shielding version (9.18W).



Fig. 3.26 Reduce the loss on shielding by adding more capacitor on secondary winding

The efficiency comparison is shown in Fig. 3.27. It can be seen that less than 0.5% efficiency difference between shielding version and original design. In summary, the shielding technique has good CM noise reduction result while little sacrifice of efficiency.



Fig. 3.27 Efficiency comparison between shielding version and original version

#### 3.7 Summary

In this chapter, the CM noise characteristic of resonant converter is introduced. The CM noise sources of resonant converter is analyzed. The method to improve high frequency performance and reduce high frequency CM noise is discussed. Then the one-layer shielding method for PCB winding transformer is provided. This shielding technique can block CM noise from primary side and also cancel the CM noise from secondary side. Thus the primary and secondary side of the transformer is completely isolated. There is no CM noise current can flow through the transformer. And CM noise reduction is achieved. In addition, shielding does not increase the loss of converter too much. In the experiment, the results shows that the total efficiency only drops less than 0.5%. Thus, this shielding technique can effectively reduce CM noise and has almost no impact on the converter performance.

Furthermore, this shielding technique can be applied to matrix transformer structure. For matrix transformer LLC converter, the inter-winding capacitor is very large and will cause severe CM noise problem. After implementing the shielding technique, the CM noise has a 23dB reduction. In addition, by modifying the secondary winding, the loss on shielding layer is minimized and experiments show that the total efficiency of converter has almost no impact.

Although this chapter uses LLC resonant converter as an example to illustrate the concept, the new shielding technique can be applied to other topologies that use PCB winding transformer.

# **Chapter 4.** Summary and Future Work

#### 4.1 Summary

Switch mode power supplies are widely used in different applications, such as power supply for telecom and server, silver box for desktops, adapter for laptops and charger for personal mobile devices. High efficiency and high power density are two driving forces for power supply systems. New semiconductor devices, circuit topologies and control methods are being developed to help make switch mode power supply systems smaller, lighter and more efficient.

However, high dv/dt and di/dt in switch mode power supplies will cause severe EMI noise issue. In a typical front-end converter, the EMI filter usually occupies 1/3 to 1/4 volume of total converter. Hence, reducing the EMI noise of power converter can help reduce the volume of EMI filter and improving the total power density of the converter.

For off-line switch mode power supplies, DM noise is dominated by PFC converter. CM noise is a more complicated issue. It is contributed by both PFC converter and DC/DC converter. A lot researches have been done to reduce the CM noise of PFC converter [6][7][8][9][10]. However, the CM noise of DC/DC converter still remains a challenge. Several methods have been provided to help reduce CM noise of DC/DC converter. However, those method cannot achieve best CM noise reduction and its effect is diminished during mass production. The main objective of this thesis is provide a solution to have best CM noise reduction for DC/DC converters.

The CM noise model of flyback converter is discussed. The major propagation paths are interwinding capacitor between primary and secondary winding of the transformer and parasitic capacitor between the drain of primary switch device and ground. Then the balance concept and shielding concept is combined to provide a novel double shielding method to reduce CM noise. This method can have an effective CM noise reduction in the circuit level. In addition, by using this method, the parasitic capacitance which impact CM noise is easy to be calculated and controlled. It makes this method suitable to real mass production that the tolerance of the parasitics can be controlled and the error on transformer winding production will not impact the balance condition.

Next, the CM noise characteristic of resonant converter is discussed. A novel one-layer shielding technique is proposed to reduce CM noise for PCB winding transformer. After implementing the shielding, the primary winding and secondary winding are completely isolated so that there is no CM noise current can flow through the transformer. The experiment shows that CM noise has been effectively reduced. In addition, the total efficiency of the converter is almost the same as the original non-shielded version. In addition, the benefit of matrix transformer is discussed. However, the matrix transformer has greatly increased the inter-winding capacitor between the primary winding and secondary winding. Thus, it has severe CM noise issue. Shielding method is also applied to matrix transformer and can greatly reduce the CM noise for whole frequency range. The loss on the shielding layer is analyzed using FEA simulation tool. One method is provided to reduce the extra shielding loss. After optimization, the efficiency of converter is almost as high as the original circuit.

Although this thesis uses flyback and LLC resonant converter as example to demonstrate the concept, the novel shielding technique can also be applied to other topologies that have similar transformer structure.

### 4.2 Future Work

Although the shielding technique is effective for the whole frequency range, the high frequency CM noise is still relatively large. The reason of large high frequency noise is still not very clear. In order to analyze the high frequency noise, a more accurate CM noise model is need and the parasitic parameters need to be considered. This can help to continue reduce the noise at high frequency range.

In addition, the CM noise reduction impact on the EMI filter need to be studied. In the future, improving the filter performance and reduce the filter size to increase the power density is an important work.

## Reference

- [1] International Electrotechnical Vocabulary IEV 161-01-07.
- [2] International Electrotechnical Vocabulary IEV 161-01-06.
- [3] Agilent Technologies: "AN150 Spectrum Analysis Basics".
- [4] EN55022: Information Technology Equipment Radio Disturbance Characteristics Limits and Methods of Measurements.
- [5] Wang S. Characterization and Cancellation of High-Frequency Parasitics for EMI Filters and Noise Separators in Power Electronics Applications [Ph.D. Dissertation]. Blacksburg: Department of Electrical and Computer Engineering, Virginia Tech, 2005.
- [6] Shuo Wang; Lee, F.C., "Common-Mode Noise Reduction for Power Factor Correction Circuit With Parasitic Capacitance Cancellation," *Electromagnetic Compatibility, IEEE Transactions on*, vol.49, no.3, pp.537,542, Aug. 2007.
- [7] Shuo Wang; Pengju Kong; Lee, F.C., "Common Mode Noise Reduction for Boost Converters Using General Balance Technique," *Power Electronics, IEEE Transactions on*, vol.22, no.4, pp.1410,1416, July 2007.
- [8] Pengju Kong; Shuo Wang; Lee, F.C., "Improving balance technique for high frequency common mode noise reduction in boost PFC converters," *Power Electronics Specialists Conference, 2008. PESC 2008. IEEE*, vol., no., pp.2941,2947, 15-19 June 2008.
- [9] Pengju Kong; Shuo Wang; Lee, F.C., "Common Mode EMI Noise Suppression for Bridgeless PFC Converters," *Power Electronics, IEEE Transactions on*, vol.23, no.1, pp.291,297, Jan. 2008.
- [10] Pengju Kong; Shuo Wang; Lee, F.C.; Chuanyun Wang, "Common-Mode EMI Study and Reduction Technique for the Interleaved Multichannel PFC Converter," *Power Electronics, IEEE Transactions on*, vol.23, no.5, pp.2576,2584, Sept. 2008.
- [11] Johannes A. C. Misdom, "Interference free, pulse type transformer," U.S. Patent 5107411 A, 1992.

- [12] Chan Woong Park, "Method and apparatus for substantially reducing electrical earth displacement current flow generated by wound components without requiring additional windings," U.S. Patent 7109836 B2, 2006.
- [13] Lassi Pentti Olavi Hyvönen, "Electrically decoupled integrated transformer having at least one grounded electric shield," U.S. Patent US7733205 B2, 2010
- [14] S. Lin, M. Zhou, W. Chen, and J. Ying, "Novel methods to reduce common-mode noise based on noise balance," in Proc. 2006 IEEE Power Electron. Spec. Conf., pp. 2728–2733.
- [15] Rockhill A, Lipo T A, Julian A L. High Voltage Buck Converter Topology for Common Mode Voltage Reduction. Proceedings of IEEE APEC 1998:940-943.
- [16] Crebier J, Ferrieux J. PFC Full Bridge Rectifiers EMI Modeling and Analysis-common Mode Disturbance Reduction. IEEE Transactions on Power Electronics 2004,19(2):378-387.
- [17] Wu H, Chen X, Zhou M, Zeng J, Ying J. A Novel Control Method of Interleaved Two-Transistor Forward Converter. Proceedings of IEEE PESC 2007:2812-2818.
- [18] Wu X, Poon F, Lee C M, Pong M H, Qian Z. A Study of Common Mode Noise in Switching Power Supply from a Current Balancing Viewpoint. Proceedings of IEEE PEDS 1999(2):621-625.
- [19] Hofsajer I W, Fricker K, Crosato M O. Reduction of EMI in Planer Transformers by Charge Balancing. IEEE Electronics Letters 2002,38(25):1712-1714.
- [20] Cochrane D, Chen D, Boroyevic D. Passive Cancellation of Common-mode Noise in Power Electronic Circuits. IEEE Transactions on Power Electronics 2003,18(3):756-763.
- [21] Crosato M O, Hofsajer I W. Minimising Conducted Common Mode EMI by Charge Balancing in a Nonisolated DC-DC Converter. Proceedings of IEEE PESC 2004(4):3146-3151.
- [22] Shoyama M, Li G, Ninomiya T. Balanced Switching Converter to Reduce Common-Mode Conducted Noise. IEEE Transactions on Industrial Electronics 2003,50(6):1095-1099.

- [23] Shuo Wang; Lee, F.C.; Odendaal, W.G., "Characterization, evaluation, and design of noise Separator for conducted EMI noise diagnosis," *Power Electronics, IEEE Transactions on*, vol.20, no.4, pp.974,982, July 2005.
- [24] Lee, F.C.; Barbosa, P.; Peng Xu; Jindong Zhang; Yang, B.; Canales, Francisco, "Topologies and design considerations for distributed power system applications," *Proceedings of the IEEE*, vol.89, no.6, pp.939,950, Jun 2001.
- [25] M. M. Jovanovic "Technology drivers and trends in power supplies for computer/telecom", *Proc. APEC*, 2006.
- [26] G. Huang, A. J. Zhang, and Y. Gu, "LLC series resonant DC-to-DC converter," U.S. Patent 6 344 979, Feb. 5, 2002.
- [27] B. Yang, Y. Ren and F. C. Lee "Integrated magnetic for LLC resonant converter", *Proc. IEEE APEC*, pp.346-351 2002.
- [28] B. Yang, F. C. Lee, A. J. Zhang and G. Huang "LLC resonant converter for front end dc/dc conversion", *Proc. IEEE APEC*, pp.1108 -1112 2002.
- [29] Bo Yang, "Topology investigation for front end DC/DC power conversion for distributed power system," Ph.D. dissertation, Dept. ECE, Virginia Tech, Blacksburg, VA, USA, 2003.
- [30] Y. Gu, Z. Lu, L. Hang, Z. Qian and G. Huang "Three-level LLC series resonant DC/DC converter", *IEEE Trans. Power Electron.*, vol. 20, no. 4, pp.781-789 2005.
- [31] D. Fu, Y. Liu, F. C. Lee and M. Xu "A novel driving scheme for synchronous rectifiers in LLC resonant converters", *IEEE Trans. Power Electron.*, vol. 24, no. 5, pp.1321 -1329 2009.
- [32] Xinke Wu, Guichao Hua, Junming Zhang, and Zhaoming Qian, "A new current-driven synchronous rectifier for series-parallel resonant (LLC) DC-DC converter," IEEE Trans. Ind. Electron., vol. 58, no. 1, pp. 289–297, Jan. 2011.
- [33] Xinke Wu, Chen Hu, Junming Zhang, and Chen Zhao, "Series-parallel autoregulated charge-balancing rectifier for multioutput light-emitting diode driver," IEEE Trans. Ind. Electron., vol. 61, no. 3, pp. 1262–1268, Mar.2014.

- [34] N. Dai and F. C. Lee "Edge effect analysis in a high-frequency transformer", Proc. 25th Annu. IEEE Power Electron. Spec. Conf., Rec., pp.850-855 1994.
- [35] Edward Herbert, "Design and Application of Matrix Transformers and Symmetrical Converters," a tutorial presented at the High Frequency Power Conversion Conference '90, Santa Clara, CA, May 11, 1990.
- [36] K. Kit Sum, D. Trevor Holmes, "Novel Low Profile Matrix Transformers for High Density Power Conversion," Power Conversion and Intelligent Motion, September, 1988.
- [37] D. Reusch and F. C Lee "High frequency bus converter with low loss integrated matrix transformer", *Proc. IEEE APEC 2012*, pp.1392 -1397.
- [38] Daocheng Huang; Shu Ji; Lee, F.C., "LLC Resonant Converter With Matrix Transformer," *Power Electronics, IEEE Transactions on*, vol.29, no.8, pp.4339,4347, Aug. 2014.
- [39] International Rectifier. (Feb. 2010). GaNpowIR—An introduction [On-line]. Available: http://www.IRF.com.
- [40] Efficient Power Conversion. EPC1015—Enhancement mode power transistor [Online]. Available: www.EPC.com.