Design and Characterization of Liquid Metal Flip Chip Interconnections for Heterogeneous Microwave Assemblies

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(ABSTRACT)

Flip chip interconnections have superior performance for microwave applications compared to wire bond interconnections because of their reduced parasitics, more compact architecture, and flexibility in laying out flip chip bond pads. Reduction in interconnect parasitics enables these interconnects to support broadband signals, therefore increasing the bandwidth capabilities of flip chip-assembled systems. Traditional flip chip designs provide mechanical and electrical connections from a top chip to a carrier substrate with rigid solder joints. For heterogeneous assemblies, flip chip connections suffer from thermo-mechanical failures caused by coefficient of thermal expansion mismatches. As an alternative, flexible flip chip interconnections incorporating a metal, which is liquid at room temperature, mitigates the possibility of such thermo-mechanical failures. Additionally, liquid metal, flip chip interconnections allow for room temperature assembly, simplifying assembly and rework processes.

This dissertation focuses on the design and characterization of liquid metal interconnections, specifically using Galinstan, an alloy of gallium indium and tin, for the heterogeneous assembly of active monolithic microwave integrated circuits (MMICs) onto a CTE mismatched substrate. Carrier substrates designed for liquid metal transitions were fabricated on high resistivity Si and on three dimensional copper structures. The three dimensional copper structures were fabricated in the PolyStrata^{TM} process. Individual MMIC chips were post-processed to mate with carrier substrates in a liquid metal, flip chip configuration. S-parameter measurements of prototype MMIC assemblies with liquid metal, flip chip interconnections showed an average transition loss of 0.7dB over the MMIC's frequency of operation (4.9 - 8.5 GHz). Passive assemblies were also fabricated to characterize

the power and temperature performance of liquid metal transitions. Liquid metal interconnections show excellent power handling, maintaining consistent RF performance while transmitting 100W of continuous wave power for an hour. Liquid metal interconnections were also tested following 200 temperature cycles over the -140°C - 125°C range. A comparison of S parameter measurements taken before and after temperature cycling, over a frequency range of 10MHz - 40GHz showed no significant changes in performance. These passive assemblies were also used to develop a lumped element model of the interconnection which is useful for the verification the interconnections performance and for comparison of liquid metal interconnection parasitic to wire bond and flip chip interconnect parasitics.

The experimental results presented in this dissertation confirm that liquid metal interconnect are viable for wider use in military and commercial applications. In the future, additional environmental testing and further refinement of the processing flow, such as improved contact metallurgy, are needed to make this interconnect approach more viable for large volume manufacturing.

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Chapter 1

Introduction

The purpose of this dissertation is to introduce the concept of a flexible liquid metal, flipped chip RF interconnect technology, outline the fabrication steps utilized to build these interconnects including integration with monolithic microwave/mm-wave integrated circuits (MMICs), and present the measured RF results of proof of concept interconnects. In this introductory chapter, conventional methods of integrated circuit and package interconnection are presented, and the advantages and disadvantages of these interconnection technologies are examined, in particular focusing on RF/microwave performance. Additionally, the basic liquid metal, flipped chip concept is introduced and the potential of this technology to advance integrated circuit packaging reliability is considered.

1.1 Electronic Packaging

Nearly all components involved in the generation, transmission, and utilization of electrical signals are packaged in some way. With the development and commercialization of the first transistors in the 1950s came the advent of a new field of electronic packaging in order to effectively interface high performance electronic components such as integrated circuits

(ICs) to the outside world. A broad definition of electronic packaging is "the portion of an electronic structure that serves to protect electrical elements from the environment, protect the environment from electrical elements, as well as allow for complete testing of the packaged device and a high-yield method of assembly to the next level of integration" [1]. The rapid pace of IC technology advancement has also driven packaging technology, and has, in many ways, outpaced packaging technology. Consequently, the performance of electronic systems is often limited by parasitics associated with the package housing electronic components. Therefore, it has become a primary objective of package designers to maximize the performance of ICs by minimizing the effect of the package on electrical signal integrity.

The requirements for electronic packages are often very complex. The microchip package functions as the mechanical support and protection for the chip, the means by which heat is removed from the chip, and the interface for signal and power access to and from the chip. These functions must be accomplished while taking into account and optimizing such factors as the electrical, thermal, and mechanical design, packaging manufacturability, testability, reliability, serviceability, cost, size, and weight. With such a wide range of requirements, the various types of ICs to be packaged, and the differing design priorities (such as RF and microwave performance vs. analog and/or digital signal performance) of each IC, a wide range of packaging technologies are now utilized by the electronics industry. The following subsections are a description of the packaging technologies which are most relevant to the work in this dissertation.

1.1.1 Packaging Hierarchy

A complete electronic system typically has multiple levels of packaging, each having its own characteristic interconnection approach. These levels of packaging can be described as follows:

- **Level 0** Transistor-to-transistor interconnection on a monolithic semiconductor chip

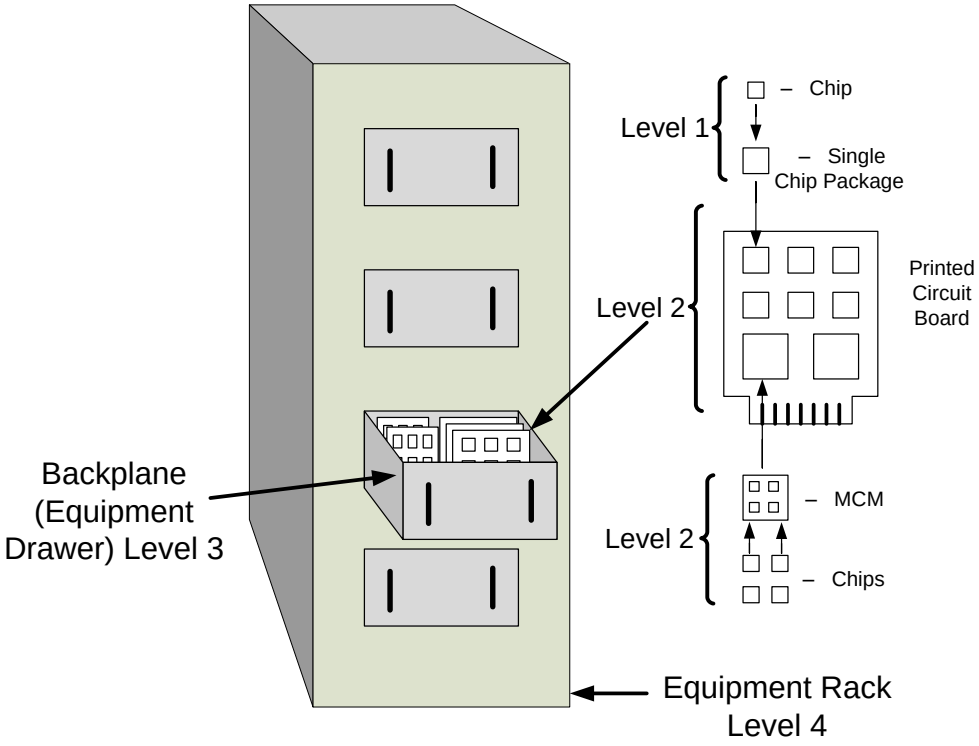

Figure 1.1: Hierarchy of electronic packages [1]. Connections between racks represent level 5 packaging.

- **Level 1** Packaging of semiconductor chips into lead frames, small outline integrated circuits (SOICs), or multichip modules
- **Level 2** Printed wiring boards or printed circuit boards (PCBs) with packaged chips or multi chip modules (MCMs), discrete components, edge connectors for off-the-board interconnection, etc.
- **Level 3** Connection between PCBs to form subassembiles
- **Level 4** Connection between two or more subassemblies to form a system
- **Level 5** Connection between separate systems

Figure 1.1 shows packaging of levels 1 through 4; connections between two or more system racks would represent "Level 5" packaging.

The level of packaging that is most pertinent to this dissertation work is level 1, particularly the packaging of semiconductor chips in multichip modules. However, there are certain packaging technologies, such as system-on-package (SOP), that blur the lines between level 1 and level 2 packaging and would also reap benefits of the type of flexible, flip chip technology to be presented in this work.

1.1.2 Level 1 Electronic Packaging

As noted previously, level 1 packaging refers to the interconnection of individual semiconductor ICs to the next level of an electronic system (e.g., a PCB). Some of the first standardized IC connection techniques were lead frames, which interconnect the IC chips via wirebond to a larger, more robust set of leads that can be soldered to a printed circuit board (PCB) without adversely affecting the microchip itself. Lead frames are still used today. These configurations are typically encased in some form of a chip carrier. Examples of chip carriers are dual in-line packages (DIPs), small outline ICs (SOICs), quad flat packs (QFPs), and ball grid array (BGA) packages (Figure 1.2). Figure 1.3a shows a single chip packaged in a DIP carrier.

With each generation of new chip carriers, the electronic packages have become smaller and lower profile. Reducing the overall size of IC packaging not only reduces size and weight of the overall system, but it also intuitively means there is a reduction in signal delay, noise propagation, and parasitics. The highest signal performance package is essentially having no package at all. The development of chip scale packages (CSPs) in the late 1990s utilized the flip chip, BGA concept; packages which consist of an array of solder balls on the bottom side of the package which bond with PCBs, to create essentially "ruggedized" ICs for ease of handling, testing, and assembly. CSPs are defined as packages that are equal to or smaller than 1.2 times the bare die size, and have contributed significantly to reducing size and weight

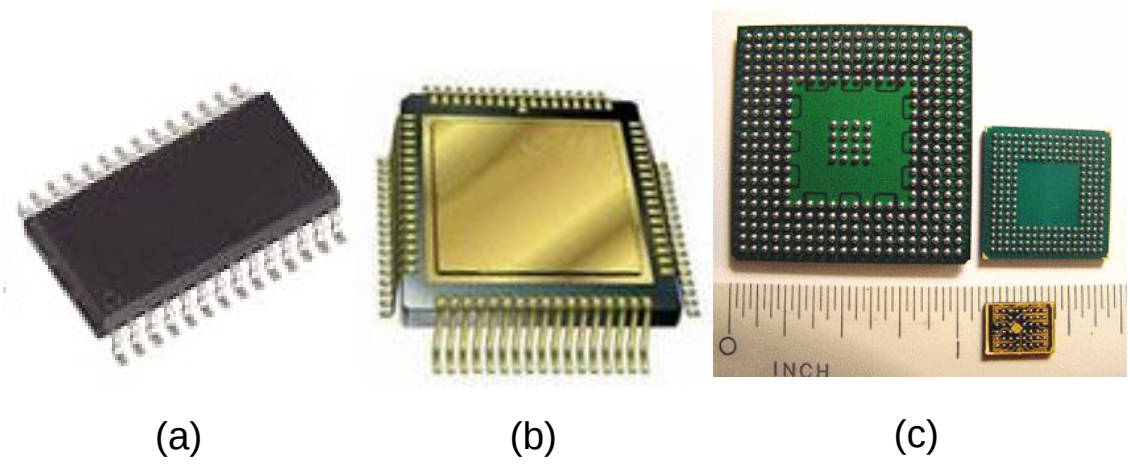

Figure 1.2: Examples of (a) SOIC, (b) QFP, and (c) BGA packages. [2, 3]

of electronics such as cellular phones, while also increasing performance of these electronics. Some of the most recent packaging efforts avoided level 1 packaging altogether and place bare die directly onto printed circuit board - an appealing idea, but one which still presents some problems where full functionality and reliability testing are concerned.

With continued advancements in silicon fabrication and design, system on chip (SOC) implementations appeared. While it is possible to integrate large amounts of functionality on a single silicon chip, cost and performance requirements of single-chip electronic systems can be prohibitive [4]. For example, fabrication of DRAM is relatively cheap compared to the requirements of processor chip fabrication, often making it impractical to design and build entire computing systems on a single chip.

A different approach to reducing the footprint of chip packaging is to have multiple chips in a single package. Multichip packaging strategies, such as multichip modules (MCMs) and hybrid modules, consist of a custom substrate which provides mechanical support to several ICs. The substrate has multiple layers of conductors which provide short length signal connections between chips, the integrated circuit chips are directly connected to the substrate using wire bonding or flip chip bonding. Compared to the signal paths of individually packaged chips, MCMs can have chip-to-chip connection lengths that are many times shorter,

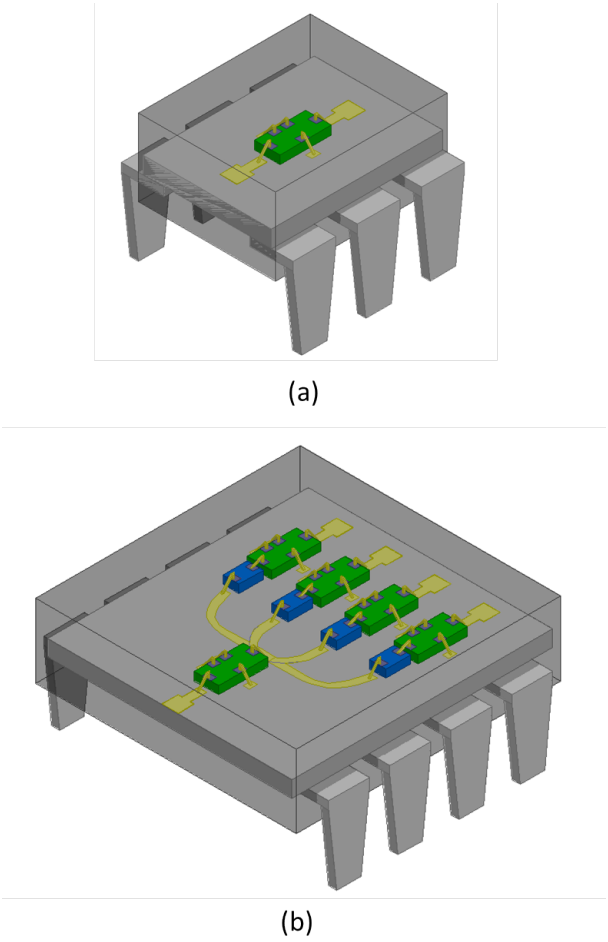

Figure 1.3: (a) An example of a single chip in a DIP package. (b) An example of a multichip module in a DIP package. Custom, multichip modules take up significantly less space and require less signal routing compared to single chip packages.

yielding a system that is smaller, has reduced transmission loss, wider bandwidth capabilities, and is more robust [5]. Figure 1.3 compares single chip packaging with a mulitchip module.

MCM technology was first utilized as early as the 1958 during the development of the first integrated circuits [6]. The military and aerospace industry drove the development of more mature MCM technology with their need of small, light, and high performance electronic platforms for aircraft and missiles. Performance gains of multichip packaging, particularly the reductions parasitics resulting from reduced interconnection lengths, make

MCMs invaluable to high frequency, broadband electronics applications.

Several innovative packaging techniques have further reduced the footprint of MCMs and made them an even more versatile. Some of these technologies include wafer thinning, which allows designers to stack chips, and improved bare die testing which increases the yield of fully assembled MCMs [7, 8, 9, 10, 11]. These innovations have enabled advances in system in package (SiP) and system on a package (SOP) technologies. SiP and SOP technologies are basically more advanced multi functional package approaches which integrate various types of components (passive components, ICs, optoelectronics, MEMS, ect.) onto very high density, single substrates. One adaptation of this configuration is to have chip dies stacked vertically on a substrate, interconnected with wire bonds or with flip chip bonds, yielding higher packaging density. SiP and SOP designs tend to be more compact and simpler than MCMs, and more easily integrated onto a printed circuit board. The subtle difference between SiP and SOP is the broader functionality that a SOP design can have; for example, RF, digital, and optoelectronic devices integrated for mixed signal applications, including passives that can be integrated into the package itself, whereas SiP is typically applied in a single functional domain (e.g., digital) [12].

1.1.3 Level 1 Packaging Technologies

Wirebonding and flip chip bonding have already been mentioned as chip interconnection methods utilized for level 1 packaging. A third, less common form of chip connection is referred to as tape-automated bonding (TAB). These three chip interconnection methods are discussed in more detail below.

Wire bond Interconnects

Wire bonded interconnects are the original and most common form of chip connection. Considered the most cost effective and flexible interconnect technology, wire bonding consists

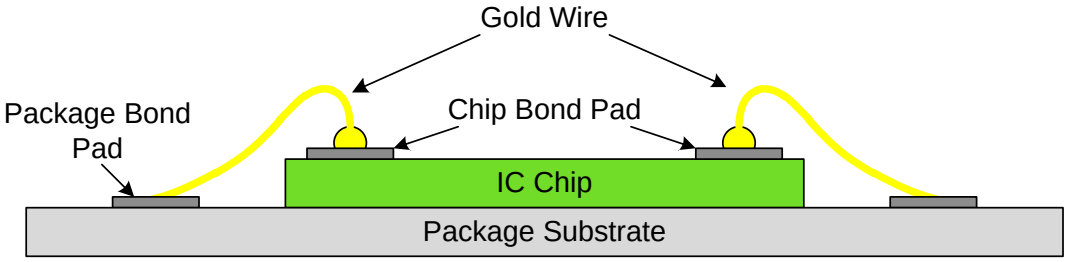

Figure 1.4: A wire bond cross section.

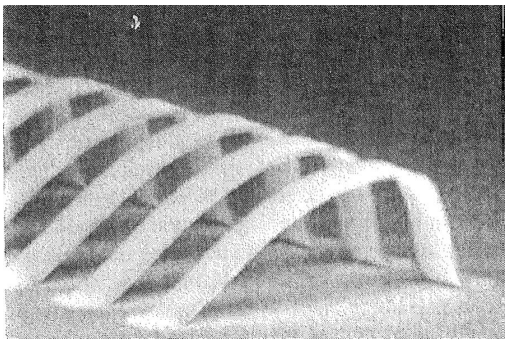

Figure 1.5: SEM of ribbon wire bonds [1]. ©by IEEE. All rights and reserved.

of a fine piece of wire electrically connecting the bond pads of a chip to contact points on an individual chip package or multichip module, as shown in figure 1.4. The chip is mounted on the package face up, allowing backside vias to ground the chip in the case of RF and microwave ICs. Integrated circuits designed for wire bond connections typically have their bond pads laid out at the outer edges of the chip in order to keep wire bonds organized, so they do not cross over one another, and minimize their length.

The wire used in wire bonding can be copper, gold, aluminum, or sometimes silver, and wire diameters can be as small as 15 μm. Ribbon bonds (Figure 1.5) are often used in microwave frequency packaging because the ribbon's rectangular shape reduces inductance and skin effect losses of the wire bond, which can be particularly detrimental to microwave performance.

There are three techniques utilized to form the bond: thermocompression, ultrasonic, and

thermosonic bonding. Thermocompression bonding uses heat, typically about 250°C, and pressure to fuse the wire to the surface of the bond pad and then to the packaging lead frame. Ultrasonic bonding presses the wire to the pad/frame and then applies ultrasonic vibration to the bond site; the pressure/force combination causes a localized temperature increase, creating a weld. Thermosonic wire bonding uses a combination of heat and ultrasonic vibration to create the bond as seen in Figure 1.6a. Thermosonic bonding typically requires less heat than thermocompression bonding; consequently thermosonic and ultrasonic bonding are much more prevalent compared to thermocompression bonding.

Some of the issues with wire bonding include restrictions placed on the bond pad locations, both because the bond pads are required to be placed at the edge of an IC and because the minimum spacing of the bond wires from each other to allow for tooling clearances (Figure 1.6b). Signal delay, crosstalk between adjacent wires, and wire bond parasitics are also issues, particularly for high frequency ICs.

Flip Chip Interconnects

Flip chip interconnects were first demonstrated at the production level by IBM with the introduction of their controlled-collapsed chip connection (C4) technology in the 1960s [13]. Figure 1.7 shows typical cross sections of flip chip structures. The integrated circuit chip is mounted face down with solder bumps providing electrical and mechanical connections. Flip chip technology was revolutionary for its ability to provide high I/O density, uniform power distribution, and high reliability. Additional benefits of the technology include reduced and more controlled parasitics, reduced assembly footprint and die size, improved signal performance, and potentially reduced production cost.

Solder is most commonly employed in the flip chip process by first depositing it on the bond pads of the IC, referred to as solder bumping. Bumping is categorized into two types: regular bumping and redistribution bumping. Regular bumping is a process that is performed at the wafer level during IC fabrication for chips that have been specifically designed for flip-

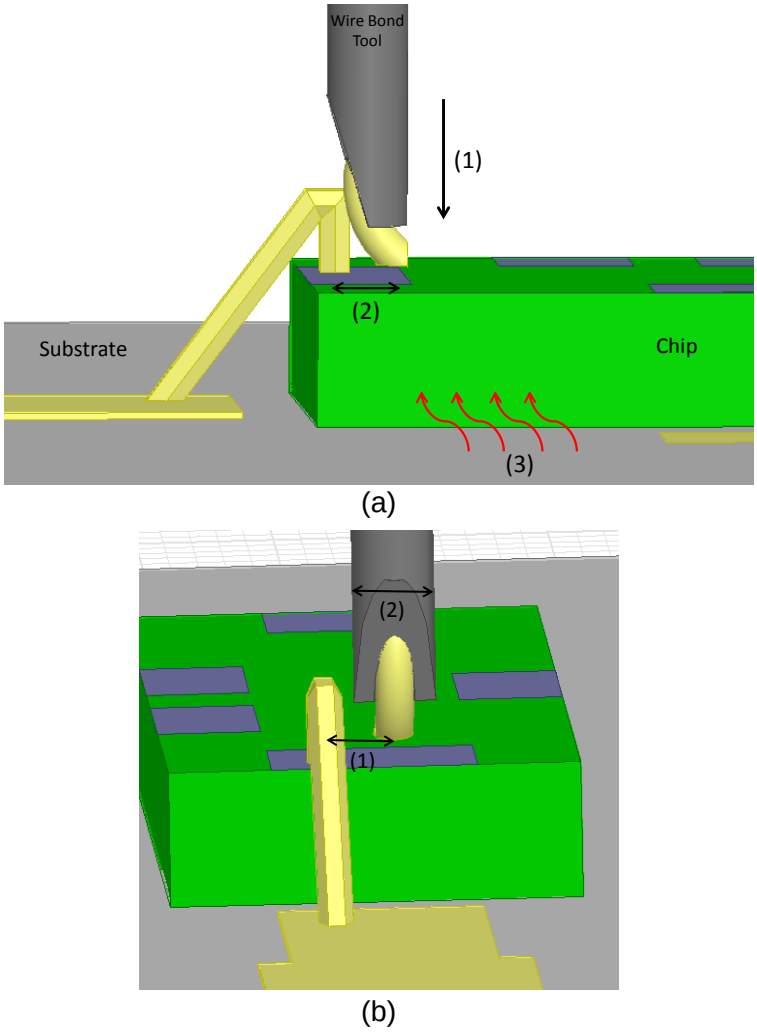

Figure 1.6: (a) A thermosonic bond is achieved by applying (1) downward force, (2) Ultrasonic scrubbing in the horizontal axis, and (3) heat. The use of all three actions enables the magnitude of each action to be minimized. (b) Spacing of wire bonds (1) will ultimately be limited by the dimensions of the wire bond tooling (b).

chip applications. Redistribution bumping refers to converting a chip that was originally designed for wire bond assembly to a chip that can be assembled via flip chip connection, typically by redistributing the layout of bond pads of the chip without redesigning the underlying IC. The bond pads are moved, post fabrication, from the perimeter of the chip to be distributed across the chip; additional ground bond pads are added to the IC since a flip

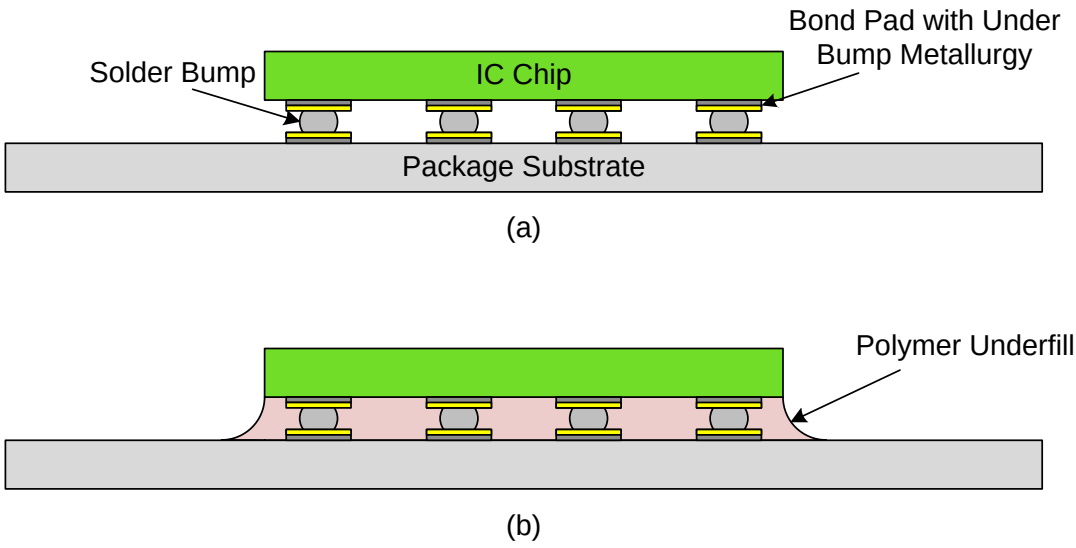

Figure 1.7: A flip chip cross section (a) without and (b) with polymer underfill.

chip structure no longer has backside ground. The post-fabrication solder pad distribution is done by adding a thin polymer layer to the surface of the chip and etching back openings over metal traces which are suitable for bond pad locations. For both regular bumping and redistribution bumping it is important to deposit under bump metallurgy (UBM) onto the IC bond pads. The UBM is usually comprised of multiple layers of metal that both provide both a good wetting layer for the solder to adhere to, and a barrier layer to keep solder metallics from diffusing into the underlying chip layers. Some examples of UBM layers are Cr/Cu/Au or Ni/Au, where in both cases Au is the topmost, bonding metal layer.

There are several different techniques employed to deposit the solder bumps on the surface of the IC. Using solder paste or conductive epoxies, solder bumps can be stenciled onto the surface of a chip and reflowed (or cured) to form solid bumps with reasonably high aspect ratio. Figure 1.8 shows the sequence of solder stenciling steps. The pitch of such bumps can be as small as 200 μm with bump heights on the order of 100 μm [1]. Stud bumping is another technology that is commonly employed, adhering a gold stud to the chip's bond pad. The tip of a gold wire is melted and joined to the surface of a bond pad; the wire is

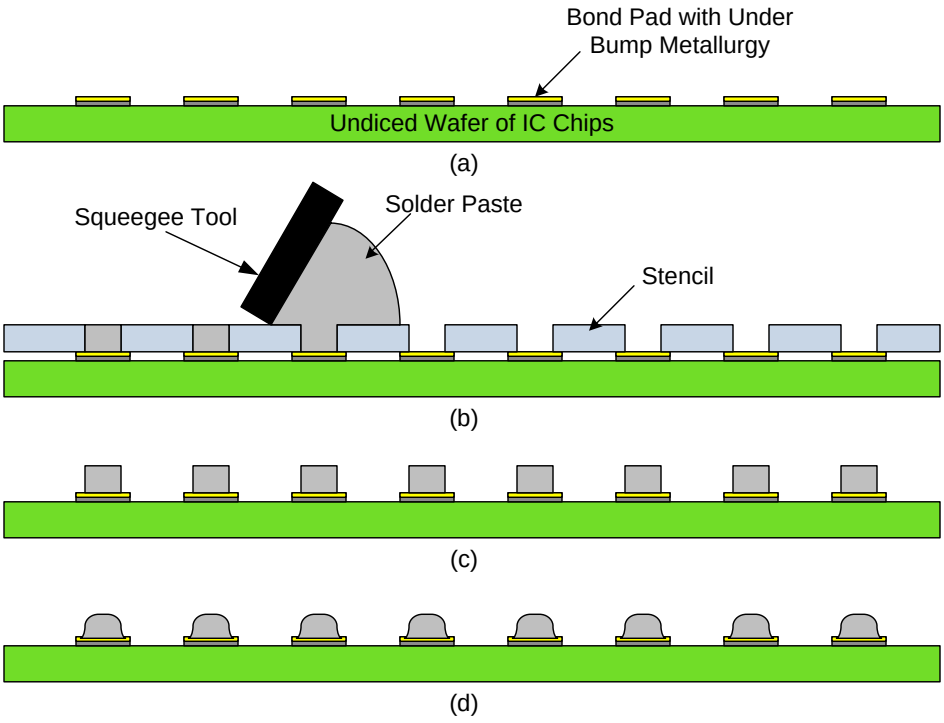

Figure 1.8: Cross section of a stencil solder deposition process. (a) Starting with a wafer with under bump metallurgy already on the wafer surface, (b) place stencil on surface and squeegee solder paste into the stencil openings. (c) Remove stencil and (d) reflow solder.

then cut and sometimes planarized for more reliable flip chip bonding [14].

Although more expensive to fabricate, plated solder bumps provide the smallest solder bump pitch of any current technology. Specifically, the state-of-the-art pitch and highest performing bumps have been demonstrated using the copper pillar bump process [15, 16]. As shown in figure 1.9, copper posts are plated up at the wafer level using a standard "lithography, electroplating, and molding" (LIGA) process; thick photoresist is used as a mold and copper is selectively plated in openings in the photoresist. These posts are typically 60 to 70 μm tall, and 20 to 35 μm of solder is subsequently applied to the top of the post. Copper pillars do not compress on contact as solder bumps would, allowing even tighter pitch bond pads and an improved height-to-diameter ratio. Because the majority of the bump is

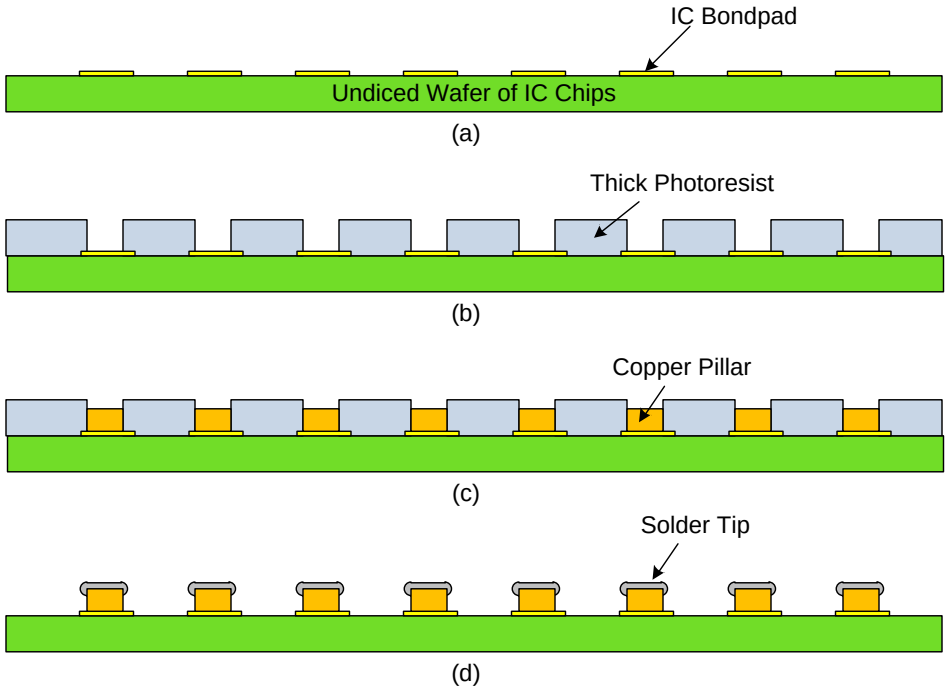

Figure 1.9: Cross section of a copper pillar fabrication process. (a) Starting with a wafer with bond pads prepped for copper plating, (b) deposit and pattern thick photoresist on the surface of the wafer. (c)Plate copper on the surface of the wafer and (d) remove the thick photoresist and tip the copper bumps with solder.

made of copper, these bumps also have better current handling capabilities and reduced risk of electromigration and related failure modes.

Once a chip has been bumped, flux is applied to its surface immediately before the chip is joined with a substrate. During solder reflow, flux helps remove oxide from the surface of the solder, ensuring good mechanical and electrical contact of all soldered connections. The viscosity and tackiness of flux also assists in holding the chip in place during reflow. Dipping, brushing, or spraying are different ways that flux is dispensed onto the solder surface. The chip is then aligned and mated to its substrate; then reflow is performed. A reflow temperature profile is used to heat up the entire assembly to an activation temperature, which is just below the reflow temperature of the solder. This is followed by a brief elevation in temperature beyond the solder melting point to ensure a consistent reflow. During reflow,

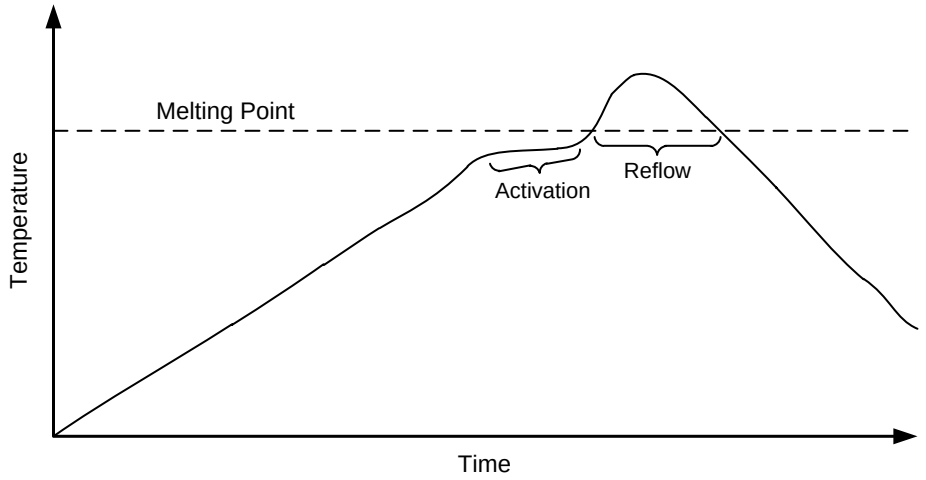

Figure 1.10: A generic temperature profile for solder reflow.

intermetallics form between the Sn contained in the solder and the metal on the bond pad surface. The chip is then cooled. The entire reflow process lasts around 3 to 4 minutes. Figure 1.10 is an example of a solder reflow profile for eutectic SnAgCu solder, often referred to as SAC solder [17].

Once an IC is mounted to a substrate, underfill is often injected into to the space beneath the underside of the chip and the carrier. Underfill is typically a thermosetting polymer which fills the gaps between the die and substrate. Figure 1.7b shows an example of a flip chip assembly with underfill. Underfill gives the flip chip assembly mechanical robustness, can reduce stress caused by thermal mismatch, and keeps reflowed solder in a state of compression. Unfortunately, curing of underfill is often a time consuming process that limits the throughput of the flip chip assembly process. The dielectric effects of underfill can also be detrimental to the performance of an integrated circuit, particularly for high frequency and high speed ICs.

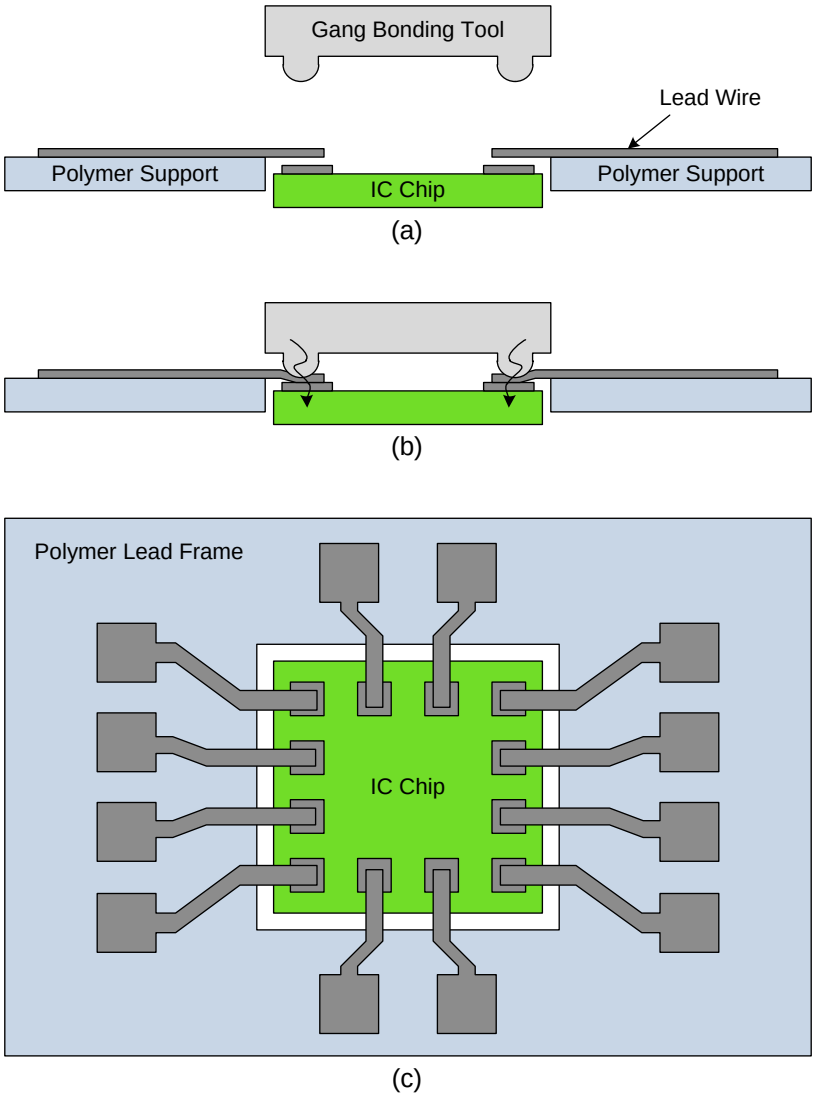

Figure 1.11: The tape automated bonding process. (a) The IC chip is aligned to the leads of the TAB frame. (b) The gang bond tool clamps onto the dangling leads and heats up, bonding the leads to the bond pads of the IC. (c) A top view of TAB assembly, the larger, outer bond pads of the TAB frame can now be used to test the IC before bonding the final assembly to a package.

Tape Automated Bonding

Tape automated bonding (TAB) was originally introduced in the 1960s because it offered significantly tighter pitch, lower profile, lower inductance, and a smaller overall footprint

compared to the wire bonding capabilities at the time [18]. Since then, however, wire bonding technology has advanced such that these advantages no longer hold true. However, one notable advantage TAB has over other forms of chip assembly is the ability to test chips before they are fully assembled to a substrate. This is a significant advantage when building expensive multichip modules.

TAB technology starts with a custom made polymer "lead frame" which has copper leads on its surface defined lithographically from metal laminate, as shown in Figure 1.11a. The lead frame is aligned and bonded to the IC all at once in a process referred to as inner lead "gang bonding". The copper leads on the polymer lead frame overhang the polymer support and overlap with the chip's bond pads (Figure 1.11b). A compression head then clamps the chip to these leads and heats up to form the bonds. Once the chip is attached to the polymer lead frame, the intermediate assembly can be tested to ensure both the quality of the bond and the proper functionality of the chip before the outer leads are bonded to the chip package.

The shape of these lead interconnects and the fact that they are formed from high conductance copper still gives this form of interconnect better performance compared to wire bonding, and gang bonding is a faster process, making TAB a desirable bonding method for chips with large I/O requirements. However, TAB is still a less economical option, requiring additional lithography and metallurgy to create the lead frame and then solder bumping the frame.

1.2 An Introduction to Microwave Frequency Package Design

Microwave and millimeter wave (mm-wave) systems operate at frequencies ranging from approximately 3 GHz to 300 GHz, with corresponding wavelengths in free space ranging from

100 millimeters to 1 millimeter. The signal wavelength is what distinguishes microwave/mm-wave frequency circuits from low frequency analog/RF circuits; the size of circuits or circuit elements of a microwave system start to become a more significant fraction of the wavelength of interest. Because of this fact, designers must take into consideration the distributed electromagnetic effects in the system rather than relying on basic lumped element circuit theory.

Despite the design challenges, operation at microwave/mm-wave frequencies has important advantages. Certain ranges of microwave frequency signals can be transmitted through the atmosphere more effectively than other frequencies. Various remote sensing applications, such as radar, operate best in the microwave range, 100MHz to 36GHz and sometimes as high as 240GHz [19]. Higher frequency signals also enable larger data bandwidths compared to low frequency carriers. Perhaps most importantly, antennas typically have optimal efficiency transmitting and receiving signals with wavelengths that are on the order of the antenna's size, and therefore higher frequency antennas will be more compact/less cumbersome than lower frequency antennas [20, 21].

Two of the major design differences between high frequency and low frequency packaging are rooted in impedance and insertion loss control. For low frequency circuitry, signal degradation is primary caused by resistive losses. Dielectric and radiative losses typically do not need to be taken into consideration at low frequencies, but at microwave and mm-wave frequencies they are often the predominant forms of signal loss. At low frequencies, parasitics of an interconnect will generate switching noise, which reduces a circuit's efficiency and the maximum switching frequency of digital systems. At high frequencies, interconnect parasitics produce switching noise, but they will also affect the characteristic impedance of an interconnection. Conjugate, matched impedances at source/load terminations result in maximum power transfer and the voltage standing wave ratio (VSWR) of the circuit will be 1. It is therefore very important to not only understand the sources of parasitic impedance in a microwave package, but also to minimize and/or compensate for these parasitic impedances.

Most monolithic microwave and mm-wave frequency chips are designed with input and output loads of 50Ω. For a level 1 package, it is important to design interconnects with characteristic impedances that reduce signal reflection and maximize power transfer to and from the IC chip. Figure 1.12a shows a simplified network model with a voltage source, V_S, and source impedance, Z_S, driving a chip load, Z_L. The source-to-load interconnect is modeled as a transmission line with characteristic impedance, Z_0. The reflection coefficient of a network represents the fraction of an incident voltage wave on a transmission line that is reflected at a transition. The equation for reflection coefficient at a load is

$$\Gamma_L = \frac{V_L^-}{V_L^+} = \frac{Z_L - Z_0}{Z_L + Z_0}. \tag{1.1}$$

Note that Z_0 and Z_L can be complex values. When Z_0 equals Z_L, Γ equals 0 and there is no reflected voltage at the transition. This is the most desired situation for the package designers, but is difficult to achieve over wide bandwidths.

Scattering parameters (S parameters) are commonly used to describe the response of high frequency, N-port networks. For this 2-port network the S parameters can be described with

$$\begin{bmatrix} V_{in}^- \\ V_L^- \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} V_{in}^+ \\ V_L^+ \end{bmatrix}. \tag{1.2}$$

Therefore, in a passive, lossless network which is used to model basic transmission lines

$$S_{11} = \Gamma_{in} = \frac{V_{in}^-}{V_{in}^+} = 1 - S_{21} \tag{1.3}$$

$$S_{22} = \Gamma_L = \frac{V_L^-}{V_L^+} = 1 - S_{12} \tag{1.4}$$

In the case of where $Z_0 = Z_L = Z_S$, the reflection coefficients at both transition points

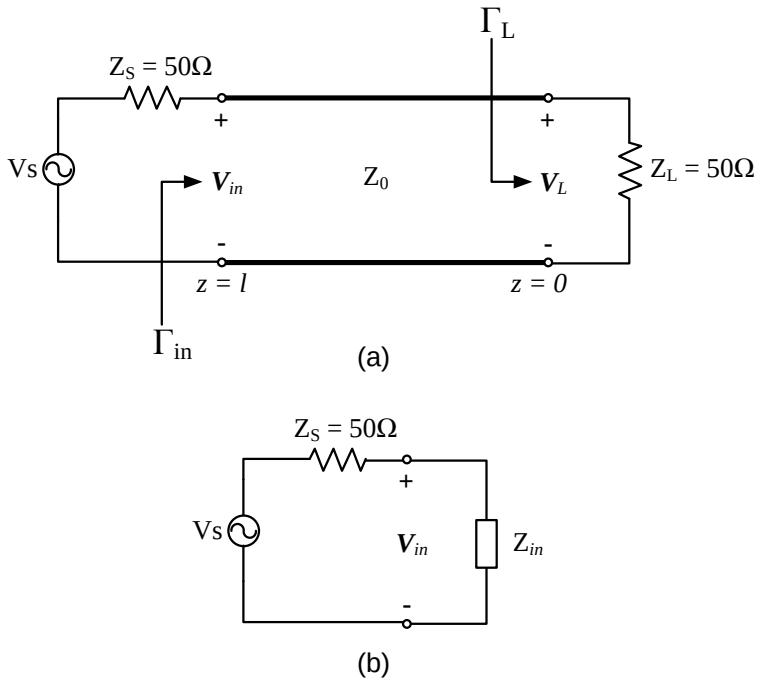

Figure 1.12: (a) Basic network where the transmission line with characteristic impedance, Z_0, represents a package interconnect between a voltage source and an on-chip load. (b) Reduced equivalent circuit with impedance, Z_{in}.

are both 0, $\Gamma_{in} = \Gamma_L = 0$. The insertion loss of the interconnect, given by

$$IL = -20log|S_{21}|dB \tag{1.5}$$

is therefore zero.

Before interconnect parasitics can be adequately understood it is important to introduce transmission lines, which are a fundamental building block to a microwave network. The following sections give a brief overview of transmission lines, the most prevalent forms of transmission line, and then cover some the major design aspects of interconnect parasitics that impact impedance control in a level 1 package interconnection.

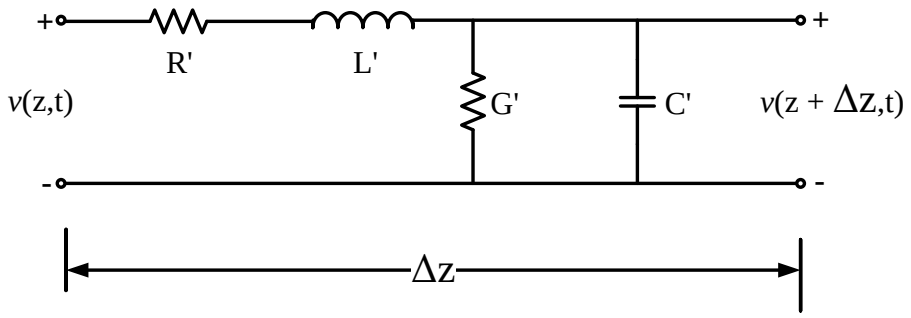

Figure 1.13: Lumped model of a transmission line with unit length, Δz.

1.2.1 Transmission Lines

Transmission line is a distributed-parameter network where voltages and currents can vary in both magnitude and phase over the line's length. The short wavelengths of microwave and mm-wave frequencies mean that most signal routing must be modeled with transmission line analysis. Transmission lines can be modeled as a lumped element circuit as seen in Figure 1.13, where, per unit length, there is an equivalent resistance, R$'$, admittance, G$'$, inductance, L$'$, and capacitance, C$'$. For an infinitely long section of transmission line characteristic impedance is the ratio of voltage and current that occur on the transmission line and is given by equation [22]

$$Z_0 = \sqrt{\frac{R' + j\omega L'}{G' + j\omega C'}}. \tag{1.6}$$

Even though resistance, R$'$, and admittance, G$'$, are always present on real transmission lines, their effects on the characteristic impedance are generally minor and they are often neglected. This results in a reduced transmission line model and the simplified equation for characteristic impedance:

$$Z_0 = \sqrt{\frac{L'}{C'}}. \tag{1.7}$$

There are many different kinds of transmission lines that are used for signal routing in the

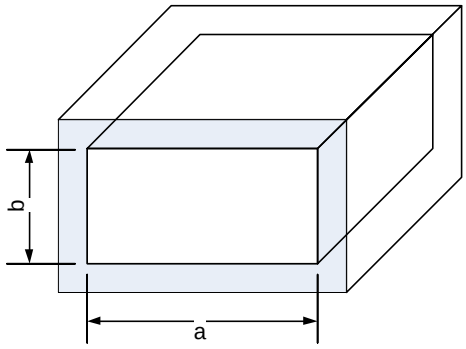

Figure 1.14: Basic cross section of rectangular waveguide.

microwave spectrum. Some of the more common transmission line structures include coaxial line, microstrip line, coplanar waveguide, and rectangular waveguide. Each are described briefly in the subsections below.

Rectangular Waveguide

Waveguide is the lowest loss transmission structure available, because waves travel through a typically air dielectric tube, as seen in Figure 1.14. This property also gives waveguide excellent power handling capability. Standard waveguide is rectangular, and dimensions of this rectangular structure constrain the range of frequencies which will propagate through the waveguide. In practice, cavity dimension, a, in Figure 1.14 is always twice as large as dimension b. Waveguide can propagate many modes, for this waveguide configuration described in Figure 1.14 the lowest frequency mode that can propagate in waveguide is the TE01 mode, referred to as the lower cutoff frequency and is calculated as [23]

$$f_c = \frac{1}{2a\sqrt{\mu\epsilon}} \tag{1.8}$$

where μ and ϵ are the permeability and permittivity of the dielectric material filling the waveguide. Typically, the lower operating frequency of a waveguide is set to be 125% to 189% of the TE01 cutoff frequency [24]. The upper cutoff frequency is defined by the

propagation of higher order modes in the waveguide, specifically TE02 in this case.

The characteristic impedance of waveguide is given as

$$Z_0 = \frac{k\eta}{\beta}, \tag{1.9}$$

where η is the characteristic impedance of free space, k is the wavenumber, and β is the propagation constant,

$$k = \omega\sqrt{\mu\epsilon}, \tag{1.10}$$

$$\beta = \sqrt{k^2 - (\pi/a)^2}. \tag{1.11}$$

Common applications for waveguide include connecting large transmit/receive modules to antennas for high power applications such as radar. However, waveguide is a bulky technology at microwave frequencies which makes it impractical for level 1 packaging. Dispersion is another characteristic of waveguide that is undesirable. Higher frequency waves propagate through waveguide slower than lower frequency waves, meaning components of a broadband module using waveguide will become distorted after the signal travels through a long enough section of waveguide. Designers must often compensate for this problem when designing wide band systems.

Coaxial Line

Coaxial transmission line, shown in Fgure 1.15a, is a transverse electromagnetic (TEM) transmission line, meaning that the electric and magnetic field lines are entirely transverse to the direction of propagation (Figure 1.15b). Electric signals propagate down the center conductor, isolated from the outer ground conductor with a dielectric region. Analysis of TEM transmission lines is relatively straightforward. Unlike waveguide, there is no lower

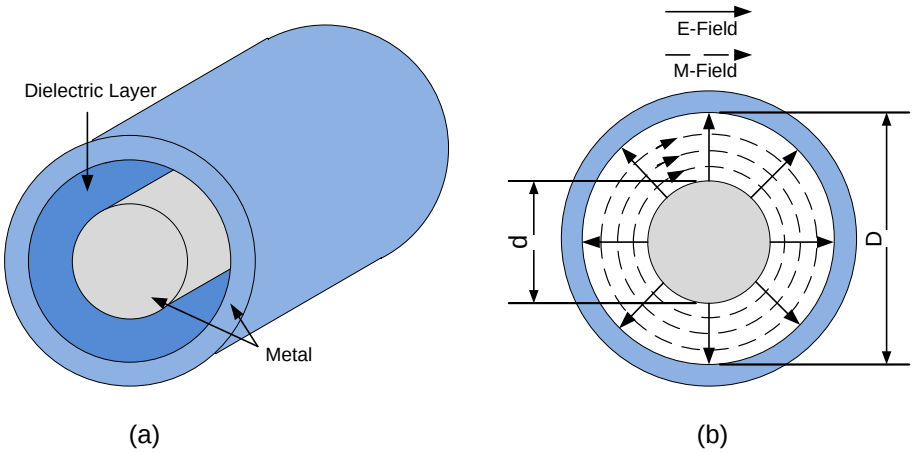

Figure 1.15: (a) Structure of a basic coaxial line. A dielectric layer isolates the center signal line from the outer grounding shield. (b) The electric and magnetic fields of a coaxial line are both perpendicular to the direction of propagation, which is into the page.

cut off frequency and there is ideally no dispersion in a TEM transmission line. A coaxial line's upper operating frequency is determined by moding caused by discontinuities in the coaxial line and circular waveguide moding, and is a function of the dielectric midpoint circumference [24]

$$f_c = \frac{c}{\lambda_c} \tag{1.12}$$

where

$$\lambda_c = \pi \left(\frac{D+d}{2} \right) \sqrt{\mu_r \epsilon_r \epsilon_0}, \tag{1.13}$$

where μ_r is the relative magnetic permeability of the dielectric, ϵ_r is the relative dielectric constant, D is the outer diameter of the dielectric layer, and d is the inner diameter of the dielectric layer. The characteristic impedance of coaxial line is given as

$$Z_0 = \frac{1}{2\pi} \sqrt{\frac{\mu_0 \mu_r}{\epsilon_0 \epsilon_r}} ln \left(\frac{D}{d} \right). \tag{1.14}$$

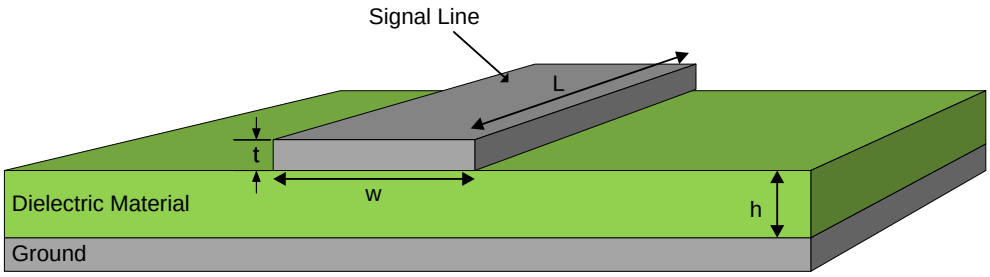

Figure 1.16: A diagram of microstrip labeling the basic parameters needed to quantify characteristic impedance.

Coaxial transmission lines are typically used in cabling, where relatively long lengths of transmission line are required, on the order of meters rather than centimeters or millimeters. Coaxial line has very high isolation and very low radiative losses. Using low loss dielectrics and tightly controlled fabrication tolerances, broadband signal integrity can be maintained for long distances. Most coaxial transmission lines are relatively bulky and expensive, however, making them impractical for many high frequency level 1 interconnection applications. An exception to this traditional thinking is PolyStrata^{TM} rectangular coax; a form of micro coaxial transmission line which is fabricated using on wafer, lithographic processing. These transmission lines are introduced in more detail in the introduction of Chapter3.

Microstrip Line

Planar transmission lines, are the standard choice for interconnecting chips and components in MCM or SOP technologies. The most common planar transmission line is microstrip: a conductor of width, w, printed on a dielectric material of thickness, h, separating the conductor from a ground plane.

Because the electric field lines going from signal to ground travel through both the dielectric layer and air, there is an effective dielectric constant which will be less than ϵ_r of the dielectric material. The effective dielectric constant is largely dependent on the geometry of the microstrip line and is empirically found to be [25]

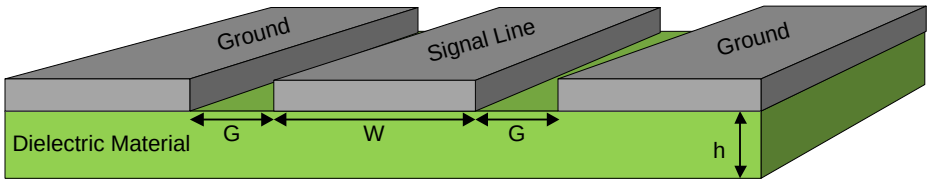

Figure 1.17: A diagram of coplanar waveguide labeling the basic parameters needed to quantify resistance.

$$\epsilon_e = \begin{cases} \frac{\epsilon_r+1}{2} + \frac{\epsilon_r-1}{2}\left[\left(1+\frac{12h}{w}\right)^{\frac{1}{2}} + 0.04\left(1-\left(\frac{w}{h}\right)\right)^2\right] & \text{when } \frac{w}{T} < 1 \\ \frac{\epsilon_r+1}{2} + \frac{\epsilon_r-1}{2}\left(1+\frac{12h}{w}\right)^{\frac{-1}{2}} & \text{when } \frac{w}{h} \geq 1. \end{cases} \tag{1.15}$$

The characteristic impedance of microstrip line can be calculated as

$$Z_0 = \begin{cases} \frac{60}{\sqrt{\epsilon_e}} ln\left(\frac{8h}{w} + \frac{w}{4h}\right) & \text{when } \frac{w}{h} < 1 \\ \frac{120\pi}{\sqrt{\epsilon_e}[w/h+1.393+0.667ln(w/h+1.444)]} & \text{when } \frac{w}{h} \geq 1. \end{cases} \tag{1.16}$$

As can be seen from equations 1.15 and 1.16, effective dielectric constant and characteristic impedance are strongly affected by the $\frac{w}{h}$ ratio. For a given characteristic impedance value, decreasing the thickness of a substrate decreases the required width of the conductor, increasing the resistive losses of the microstrip. Meanwhile, as a general rule of thumb, microstrip substrate thickness should be not thicker than 10% of the wavelength of operation to prevent higher order moding [24]. Therefore microstrip lines on thin, high frequency MMIC chips and package substrates will lead to high resistive losses because the conductor widths must be scaled down to narrow widths to achieve desired impedance widths. Resistive effects are discussed in more detail later. Additionally, because microstrip line is unshielded on three sides, it will have poor isolation with neighboring microstrip lines. Sometimes additional shielding structures must be integrated into the substrate to prevent this.

Coplanar Waveguide

Coplanar waveguide (CPW) is a planar transmission line configuration where the signal line of width, W, resides in between two ground planes with a gaps, G, between the signal and ground planes (Figure 1.17). Coplanar waveguide has some characteristics that make it well suited for certain applications compared to microstrip. CPW has better isolation than microstrip because the ground plane is in the same plane as the signal line. Additionally, MMICs that are designed with CPW transmission line rather than microstrip no longer require expensive backside vias to a bottom ground plane and have greater versatility for the design of signal lines for a given characteristics impedance. MMICs designed with CPW are also better suited for flip chip assembly.

Calculating the impedance of CPW is not always a straightforward process. This is partially because there are several variations of CPW; some can have a backside ground (CPWG), some can have finite ground planes, etc. For the most ideal form of CPW, the metal traces are printed on an infinitely thick dielectric. This is not a realistic scenario, but when the thickness of the dielectric is significantly larger than W+2G it can be assumed that the dielectric thickness is approximately infinite [26]. Under this condition characteristic impedance can be calculated as [27]

$$Z_0 = \frac{30\pi}{\sqrt{(\epsilon_r + 1)/2}} \frac{K(k')}{K(k)} \tag{1.17}$$

where K(k) and K(k′) are the complete elliptic integrals of

$$k = \frac{W}{W + 2G}, and \tag{1.18}$$

$$k' = \sqrt{1 - k^2}. \tag{1.19}$$

As with microstrip, the ratio of trace width, W, and signal to ground gap, G, influence the

CPW's characteristic impedance. Therefore, if designers want tight signal routing spacing, the signal conductor metal must be scaled down to very small widths. In general, this causes CPW transmission lines to have even higher resistive losses compared to a similar microstrip configuration. However, when high signal isolation is a requirement, this may be a compromise that designers may be willing to make.

Another problem with CPW is that asymmetry or discontinuities in CPW can cause slot line moding to occur [28, 29]. Certain design strategies can help prevent this, such as creating air bridges over the signal trace to better connect the two ground planes, but this only adds complication and additional processing to the the overall fabrication of CPW traces.

1.2.2 Packaging Parasitics

Transmission lines route electric signals to the bond pads which interact with the wirebond, flipchip, or TAB transition. In order to design well matched systems, it is important to have an understanding of how the geometry of the transmission lines and packaging interconnections affect the the impedance of the overall network connection. The following gives a brief introduction to these parasitics: resistance, capacitance, and inductance.

Resistance

The most apparent effect of interconnect resistance is power dissipation, $P_{loss} = I^2R$. Power dissipation not only degrades the quality of an integrated circuit's signal performance, but also creates unwanted heat. There are many high frequency, high power, applications, such as aerospace applications, where thermal management is a major design challenge because size and weight of the circuit system must also be minimized. Generally, elaborate cooling systems will reduce the available payload of an aircraft or spacecraft.

Consequently, conductor material selection for high performance packages is often limited to metals with very high conductivity. Table 1.1 gives the bulk resistivity, ρ, of several

Table 1.1: Bulk resistivity of common metal conductors commonly used in packaging at 300K [30].

Metal	**Resistivity (ρ)**
Aluminum	2.73×10^{-6}
Copper	1.73×10^{-6}
Gold	2.27×10^{-6}
Silver	1.63×10^{-6}

different materials commonly used in the packaging of high frequency electronics.

Figure 1.16 shows a cross section of microstrip transmission line. DC and low frequency resistance can be described with the basic equation

$$R = \frac{\rho L}{A} = \frac{\rho L}{wt} ohms. \tag{1.20}$$

Essentially, resistance is directly proportional to the bulk resistivity of the signal line material and length of propagation, and inversely proportional to the cross sectional area of the signal line. It has already been mentioned how the small widths of these lines on thin MMIC chips can result in high resistive losses. Meanwhile, at higher signal frequencies, current begins to concentrate on the surface of a conductor with current density decreasing exponentially as a function of distance into the conductor. Skin depth, δ_S, describes this phenomenon and is defined as the distance into the conductor where the current density is 37% of the current density at the conductor surface. It can be quantified with the equation

$$\delta_S = \sqrt{\frac{\rho}{f\pi\mu}} \tag{1.21}$$

where f is the frequency of the signal and μ is the magnetic permeability of the conductor material. Figure 1.18 is a graph of skin depth as a function of frequency. This skin effect

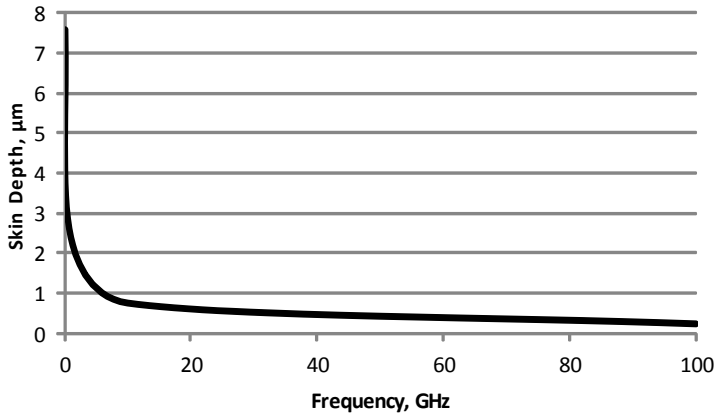

Figure 1.18: Skin depth into gold as a function of frequency.

causes significant increases in series resistance once the skin depth becomes smaller than half the signal line thickness. For the microstrip configuration shown in Figure 1.16 the skin-effect resistance is given by [31]

$$R_\delta = \frac{L\sqrt{f\pi\mu\rho}}{2(w+h)}, \tag{1.22}$$

where h is the thickness of the dielectric layer. We see that for microwave frequency circuits, the thickness of the signal trace is no longer a significant factor; signals flow along the surface of the trace and therefore resistance is largely determined by the trace's width.

As thickness of metal conductors scale down to small thicknesses, where $t << \delta$, the resistivity of the metal is no longer constant, but increases logarithmically as the metal gets thinner [32]. This property is utilized when making thin film resistors, but can be troublesome for signal routing very thin layers of metals on MMICs and planar substrates.

Capacitance

A first order equation to describe capacitance between two parallel plates with large surface area relative to their spacing from one another (Figure 1.19a), is

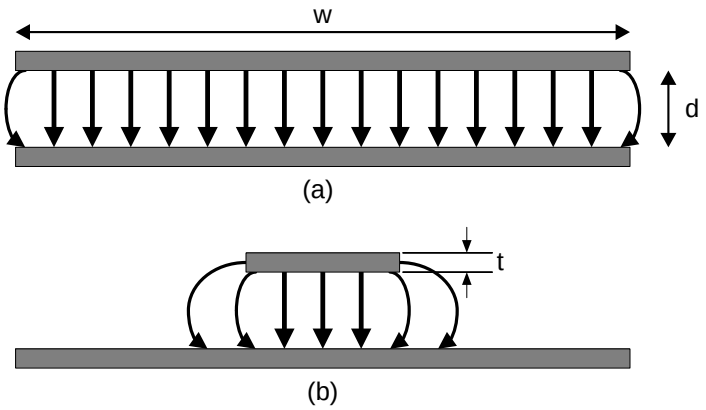

Figure 1.19: Examples of fringe fields for (a) infinitively large parallel plate capacitors and (b) finite parallel plate capacitors.

$$C = \frac{\epsilon_o \epsilon_r w L}{d} \; farads, \tag{1.23}$$

where w is the width of the interconnect, d is thickness of the dielectric material between the two conductors, and L is length. Essentially, capacitance is directly proportional to dielectric constant and the coupling surface area, and inversely proportional to the thickness of the dielectric material.

This relationship becomes inaccurate as the width of one or both of the conductors becomes on the same order as the distance, d, between the two conductors (small w/d ratio). In this case, the electric field fringing effects, shown in Figure 1.19b, become significant and increase the overall capacitance to values that exceed that of the expected values from equation 1.23. This fringing effect will cause the microstrip lines or wire bonds suspended over a ground plane to have a larger than expected parasitic capacitance. There are several approximate equations which attempt to capture the true capacitance of small conductors over ground planes; some of the most accurate approximations are empirically derived [33, 34, 35]. A good overall equation which can accurately estimate capacitance for both large w/d ratios (typically the case for microstrip and bond pad capacitance) and small w/d ratios (typically the case for capacitance of a wirebond over a ground plane) is given by

$$C \approx \epsilon_o \epsilon_r L \left[\frac{w}{d} + 0.77 + 1.06 \left[\left(\frac{w}{d} \right)^{0.25} + \left(\frac{t}{d} \right)^{0.5} \right] \right] \tag{1.24}$$

where t is the thickness of the wire bond. Wire bonds connected to an IC package will often have parasitic capacitances on the order of 1 pF [1].

Inductance

Wire bond inductance is typically the most predominant and detrimental parasitic when interconnecting an RF IC to its package. The two forms of inductance are self-inductance and mutual inductance. Self inductance of a current carrying conductor can be defined as

$$L_s = \frac{N\Phi}{I} \; henrys \tag{1.25}$$

where N is the number of turns in the conductor, ϕ is the flux density, and I is the magnitude of the current. For a cylindrical, straight conductor, as shown in Figure 1.20a, the self inductance of this conductor in nanohenries is determined to be [36]

$$L_s = 0.00508L \left[ln \left(\frac{4L}{r} \right) - 1 \right], \tag{1.26}$$

where r is the radius of the conductor and L is the length of the conductor, both expressed in units of milli-inches (mils). Note that inductance is directly proportional to length of a conductor, but not dependent on the magnitude of current flowing through it. Additionally, the smaller the radius of a conductor, the larger its self inductance. And no matter how close the chip's bond pad is to a package bond pad, the length of the wire bond does not decrease linearly, because of the required bond wire loop height as can be seen in Figure 1.20b [37]. The minimum wire bond length that can realistically be achieved is approximately 100 μm, or 4 mils in length. For a bond wire diameter of 1 mil, the expected inductance of such a bond is still greater than 0.05nH. At increasing frequencies, the parasitic impedance of this wire

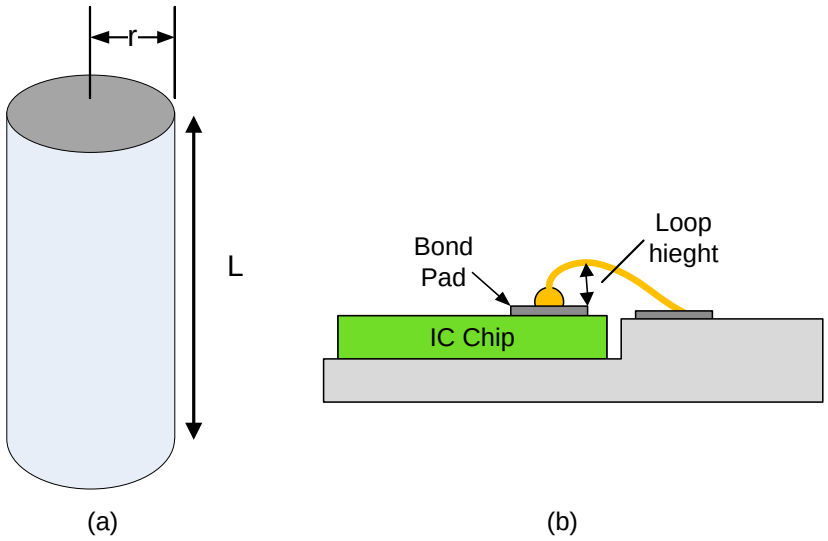

Figure 1.20: (a) Current carrying conductor labeling the parameters used in inductance calculations. (b) The loop of a wire bond extends the total length of the wire bond, but the radius of this loop is large enough that it can be accurately modeled as a straight, current carrying conductor.

bond inductance becomes more significant and thus more detrimental to the performance of the assembly.

Meanwhile, coupling between by the magnetic fields of two nearby conductors, creates mutual inductance. Assuming that the dielectric medium between the conductors is air, and applying Biot-Savart law and Maxwell's equations, mutual inductance can be described with [1]

$$L_M = \frac{\mu_0 L}{2\pi}\left[ln\left(\frac{L}{d}+\sqrt{1+\left(\frac{L}{d}\right)^2}\right)-\sqrt{1+\left(\frac{d}{L}\right)^2}+\frac{d}{l}\right], \tag{1.27}$$

where L is the length of the conductors, d is distance between the two conductors, and μ_0 is the permeability of free space. In general, mutual inductance is much smaller than self-inductance, but cross talk in neighboring wire bonds is still a design issue that must be addressed when laying out the bond pads of a chip.

1.2.3 The Case for Flip Chip Interconnects

A perfectly matched, broadband network is nearly impossible to design and build. In the case of wire bond transitions, the characteristic impedance of typical wire bonds is very hard to match to 50Ω. Models have been developed to account for the electrical effects of wire bonds and are given as [38, 39, 40]

$$Z_0 = \frac{\eta_0 u_0}{2\pi\sqrt{\epsilon_w}} \tag{1.28}$$

where η_0 is the characteristic impedance of free space and ϵ_w is the effective dielectric constant of the wire bond, given by

$$\epsilon_w \approx \left[1 - \frac{k_0}{u_0}\left(\frac{\epsilon_r - 1}{\epsilon_r}\right)\right]^{-1/2}, \tag{1.29}$$

$$u_0 = ln\left(\frac{h}{r_w} + \sqrt{\left(\frac{h}{r_w}\right)^2 - 1}\right), \tag{1.30}$$

$$k_0 = ln\left(\frac{\sqrt{(h/r_w)^2 - 1} + h_s/r_w}{\sqrt{(h/r_w)^2 - 1} - h_s/r_w}\right). \tag{1.31}$$

Where, h_s is the thickness of the chip, h is the height of the bond wire loop over the ground plane, and r_w is the radius of the bond wire. So the characteristic impedance of a wire bond to a $100\mu m$ thick GaAs chip with a maximum loop height of $150\mu m$ above the ground plane and a radius of $25\mu m$ will have a characteristic impedance of about 118Ω. Reducing the bond wire height and using wider ribbon bonds can bring down the characteristic impedance of the wire bond, but it is not possible to get wire bond impedances down to 50Ω in general.

In such cases where the interconnect impedance does not match the rest of its network, the voltage source will see an impedance at the position, $z = l$, as shown in Figure 1.12b. This value of Z_{in} is given as [22]

$$Z_{in} = Z_0 \left(\frac{Z_L + \jmath Z_0 \tan \beta l}{Z_0 + \jmath Z_L \tan \beta l} \right) \tag{1.32}$$

where β is the the phase constant,

$$\beta = \omega \sqrt{L'C'}. \tag{1.33}$$

If the characteristic impedance of the interconnect is not well matched to the source and load impedance, a way to at least minimize the effects of the interconnect is to reduce the βl term in equation 1.32 to nearly zero. This can be done by reducing the length of the interconnect and/or reducing the values of L' and C'. Wire bond inductances are intrinsically larger and their interconnect lengths are longer than that of flip chips, so this will not often be a practical solution with wire bonding. Even when a package design is tightly controlled, a wire bond connection will be at least hundreds of micrometers in length while typical flip chip connections can be as short as 25 μm and rarely longer than 100 μm in length.

The inductances of wire bonds can be now be reasonably well controlled with automated, repeatable wire bonding and therefore compensated with capacitances added on or off chip. This is the typical way designers deal with the high impedances of wire bonds; however the resulting LC-networks will reduce the bandwidth of a chip.

Bandwidth reduction can be quantitatively understood by examining the quality factor of a circuit, Q. Quality factor has different, but equivalent, definitions; for this discussion it can described as the ratio of reactance to resistance of a network. Quality factor is inversely proportional to the circuit's bandwidth [41]. For a series RLC network, this can be described in equation form as

$$Q = \frac{f_0}{B} = \frac{\omega_0 L}{R}, \tag{1.34}$$

where f_0 is frequency, ω_0 is angular frequency, B is bandwidth, R is the circuit resistance,

and L is the circuit inductance. It can therefore be concluded that

$$B = \frac{R}{2\pi L}. \tag{1.35}$$

This shows that broadband circuitry is extremely limited by high series inductances introduced by wire bond packaging. Scaling up to microwave frequency applications, particularly at frequencies exceeding 40GHz, wire bond packaging quickly becomes impractical and very limiting to circuit design. Typical inductive and capacitative parasitics of flip chip designs are on the order of 10 pH and 10 fF whereas wirebond inductance is generally greater than 1 nH and 1 pF. In these cases flip chip connections, as described in Section 1.1.3 become a much more attractive level 1 interconnect option.

1.3 Flip Chip Failure Modes and Issues: A Case for Liquid Metal Interconnects

The advantages of flip chip connections for level 1 packaging were discussed above, but there are also several problems that come with this form of interconnect. Intuitively, a very small connection point which is to provide both mechanical and electrical continuity between two materials can be a point of failure for a system. Solder joints have been scaled down to dimensions as small as 50 μm in diameter and 25 μm tall [12]. Reducing the size of these rigid connection points subjects flip chip connections to potential mechanical and electrical failures which create packaging reliability issues.

There are a number of failure modes that can be experienced by flip chip solder connections can experience. The following subsections briefly discuss some of these flip chip packaging issues.

1.3.1 Lead-Free Solders

Japan was the first country to begin phasing out lead based solder from consumer electronics in the late 1990s [42]. In 2006 the European Union's Restriction of Hazardous Substances (RoHS) Directive (2002/95/EC) went into effect [43]. Similar restrictions have taken effect in China and South Korea in 2007. With a few minor exceptions, these RoHS regulate the concentration of lead in the majority of consumer grade products to be no greater than 0.1% by weight.

The vast majority of flip chip interconnections are created with solder bonding. As mentioned previously, conductive epoxies can possibly be used to replace solder. This is rarely done because of conductive epoxy's inferior thermal, mechanical, and electrical properties compared with solder [44]. Thermosonic bonding of stud bumped ICs is another solder free way of joining these two surfaces, however such bonding requires reasonably high downward forces applied to the chip in order to ensure adequate bonding of each stud, approximately 100 grams force per stud bond compared to a few grams of force per bond when using solder [45]. These levels of mechanical compression applied to III-V semiconductor materials can cause significant damage to an IC chip, making thermosonic bonding unrealistic for many high frequency chip interconnections where there are more than a few connections points from chip to substrate.

Before the aforementioned restrictions were scheduled to take effect, the majority of all soldering was performed with PbSn solder. There are several metallic compounds that have been proposed to replace lead-based solder; nearly all of these are Sn-based. Table 1.2 gives a brief summary of some of these more prevalent compounds.

Even though lead free solders have now been used in industry for several years there are several process-related problems that have not been resolved and will not likely be resolved in the near future. For instance, as seen from table 1.2, there are no current solders in the industry that have a reflow temperature near the reflow temperature of PbSn solder. The compound with the closest reflow temperature is SnZn. However, zinc readily forms stable

Table 1.2: Pb-free eutectic solders [12].

Compound	Reflow Temp. (°C)	Eutectic Composition (wt%)
Sn-Cu	227	0.7
Sn-Ag	221	3.5
Sn-Au	217	10
Sn-Ag-Cu	217	4.2
Sn-Zn	198.5	9
Sn-Pb	183	38.1
Sn-Bi	139	57
Sn-In	120	51

oxides causing it to have very poor wetting behavior during reflow. Because of this, SnZn is rarely utilized.

The solder with the next closest reflow temperature is SnAgCu (SAC), which is the most common lead-free solder available. This compound wets well to copper and gold and has better thermomechanical properties compared to PbSn. Nonetheless, the reflow temperature of SnAgCu is greater than 30°C higher than that of PbSn. Because flux has not yet been optimized for the reflow temperatures of SAC solder, this lead free solder paste produces many more residue voids in the solder joints than PbSn paste [42] increasing the probability of mechanical fatigue failures. The higher reflow temperature also presents a problem when solder forms a bond with the UBM on a IC's bond pad. Higher reflow temperatures mean unwanted intermetallics are more likely to form between layers of the bond pad metalization and even within the molten solder, creating brittle areas and eventually leading to fracture failure of the joint.

In solder, Sn is the active element which forms an intermetallic bond during reflow with the surface metal of the bond pad. The high concentration of Sn in these newer, lead free

solders limits the number of reflows that a solder joint can withstand before the solder joint reduces the entire bond pad to a Sn based intermetallic. For multistage assemblies, or assemblies that may require rework, this can be problematic. If UBM adhesion layers, which attach the bond pad metal to the IC or package substrate, begin to form intermetallic with the Sn the mechanical strength of the bond is significantly deteriorated and the solder bump is prone to cracking from the surface of the IC or the package substrate. This phenomenon is referred to as spalling [46, 47].

High concentrations of Sn in lead free solder also creates an environment where Sn whiskers can form [48, 49]. Sn whiskers will freely grow in regions of internal stress of matte Sn finishes, and have become a widely recognized reliability issue. Such whiskers can grow several hundred micrometers in length, causing shorts between neighboring connections. An example of a Sn whisker is shown in figure 1.21.

It has taken intensive research and development to refine processes which provide the repeatable performance of lead based, flip chip soldering to reliably form many bonds during a single reflow step and subsequently withstand additional heat cycling without chemical and mechanical deterioration. It will take similar levels of effort to do the same with lead free solders. However, in the near term, lead free solders are experiencing significant reliability issues.

1.3.2 Flip Chip Rework

In expensive multichip modules it is often desirable to replace a single chip which has failed rather than replace the entire module. In these cases the module must undergo rework. With flip chip interconnects this is a fairly time consuming process. The solder must first be reflowed to remove the bad chip. Then residual solder must be removed from the surface of the module substrate so that a clean and planar bonding surface remains for the replacement chip to bond with. Finally a new chip is then aligned to the substrate and bonded with temperature cycling.

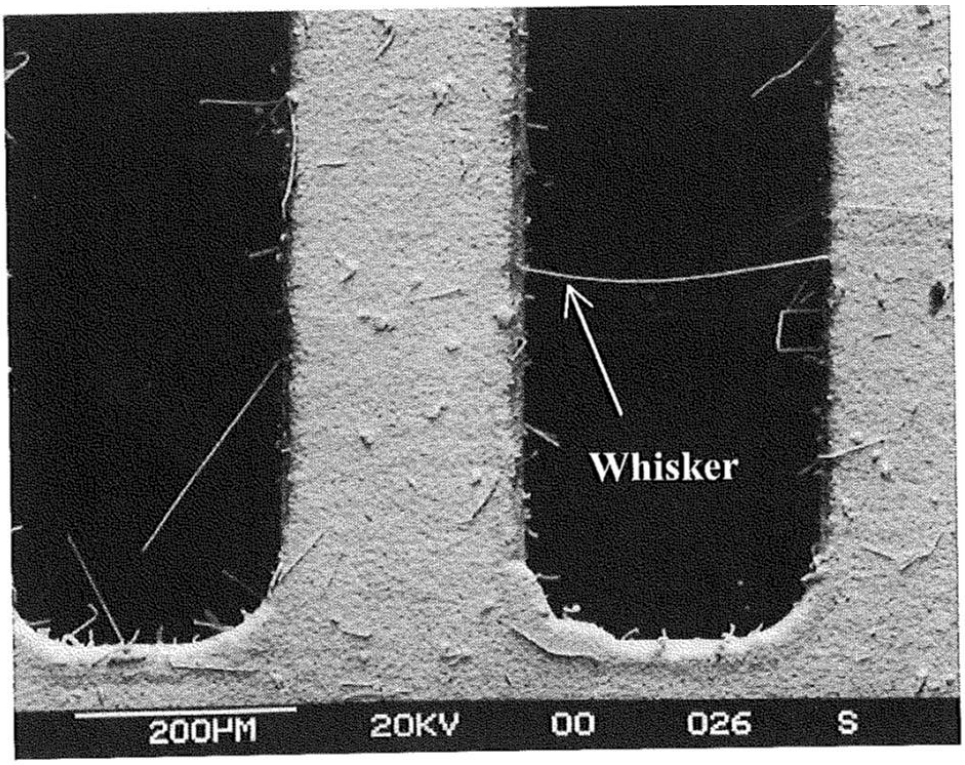

Figure 1.21: An SEM image of a Sn whisker forming a short between two legs of a lead frame [12]. ©by Springer Series in Material Science. All rights and reserves.

All of these steps take time, and each time the module is subjected to applied heat for solder reflow. There is a risk of damage to the solder pad on the substrate and also risk of reflowing the solder bumps of chips in close proximity, or damaging any neighboring components on the substrate which are temperature sensitive. Plastic connectors or electrolytic capacitors (which can explode if they are overheated) should be protected with thermal tape or a heat sinking device if they too close to the area of rework [42].

During the assembly of a new IC chip onto the substrate, controlling the temperature of the substrate is more difficult because the module is now fully built. It is important to closely monitor the temperature of the local substrate where the chip is being connected and neighboring components that will be may become compromised by high temperatures.

The use of lead free solders only exacerbates these problems since the reflow temperature

of this solder is higher than lead based solder. Additionally, as mentioned in the previous section, subjecting the substrate bond pad to multiple solder reflows increases the probability of spalling at the substrate/solder interface.

All of these factors make module rework a challenging process which does not guarantee the module can be salvaged.

1.3.3 Thermo-Mechanical Stresses

Both during assembly of a single chip package or module, and during the standard operation of the finished package or module, the chip will undergo temperature variations. Since materials have varying coefficients of thermal expansion (CTEs) and many ICs will experience temperature differences between the chip its package/substrate, solder joints will undergo some amount of shear strain throughout the package's life cycle.

Solder joints are under stress as soon as they connect two heterogeneous surfaces. Solder reflow elevates the temperature of the entire assembly, causing expansion of both the substrate and the integrated circuit. This reflow cycle is shown in Figure 1.22. The chip and substrate are aligned before the reflow process begins (Figure 1.22a). Most substrates will expand at a higher rate since they usually have larger CTEs than semiconductor ICs, as seen in Figure 1.22b. Depending on the rigidity of the substrate and the IC, once the entire assembly cools back down to room temperature, either the solder joints will prohibit the substrate from shrinking back to its original size, or the solder joints will deform to match to the room temperature dimensions of the assembly (Figure 1.22c).

A basic analytical model which describes the shear strain solder joints experience during temperature variations is:

$$\epsilon = \frac{L}{h}\left(\alpha_{sub}\Delta T_{sub} - \alpha_{IC}\Delta T_{IC}\right) \tag{1.36}$$

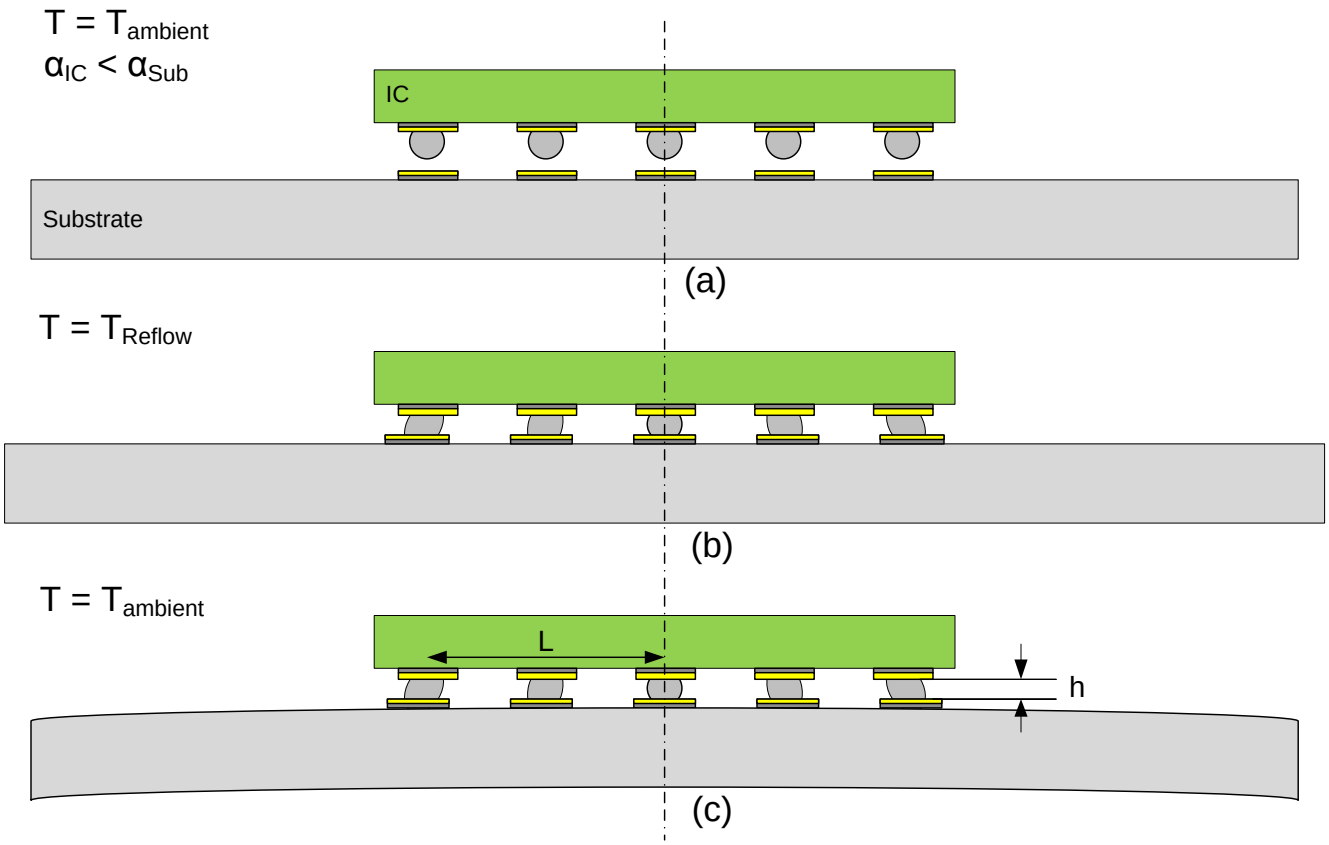

Figure 1.22: (a) There is no thermal stress in a solder joint before joining. (b) During reflow the substrate will expand at a higher rate than the IC chip, deforming the solder bumps slightly. (c) Once the assembly is cooled back down to room temperature the solder joints left are under shear strain.

where α_{IC} and α_{sub} represent the coefficients of thermal expansion of the IC and the substrate respectively, ΔT represents the assembly's deviation from the "stress free" temperature, L represents the distance the center of the solder joint resides from the neutral position of the assembly (the dashed line in Figure 1.22), and h is the height of the solder joint [50].

The strain behavior of solder can be broken out into three distinct parts; elastic strain (ϵ_e), time-independent plastic strain (ϵ_p), and time-dependent creep strain (ϵ_c). Figure 1.23 is a simple model of a solder's response to a step load showing these three forms of strain. That portion of the total strain that gets allocated to each of these three forms of strain is

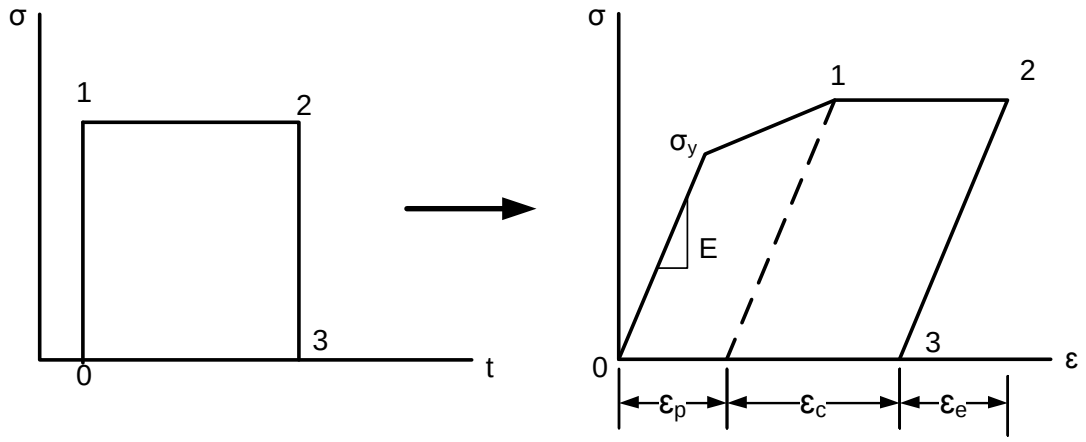

Figure 1.23: Strain response of solder with an applied step stress load showing the three forms of strain.

dependent on the material properties of the solder, the temperature of the solder bump, and the applied stress's magnitude and rate of application.

Elastic strain represents the recoverable flexing that a solder bump can withstand and follows Hooke's Law,

$$\epsilon_e = \frac{\sigma}{E} \tag{1.37}$$

where σ is the applied stress in MPa and E is the Young's Modulus in MPa. Young's Modulus is a temperature dependent property for solders.

Time-independent plastic strain is the non-recoverable deformation experienced by a solder bump. There are several different models that can be used to analyze plastic strain, solders are best modeled with a nonlinear hardening model which is often described with the Ramgood-Osgood equation [50],

$$\sigma = H(\epsilon_p)^n, \tag{1.38}$$

where H is a material constant typically set to be the stress value σ_y, and n is a material

constant referred to as the strain hardening exponent.

Creep strain is a time dependent, non-recoverable form of strain. It can be observed in metal structures when the metal's homologous temperature (the ratio of the metal's melting temperature, T_m, in Kelvin, to the metal's actual temperature) is greater than $0.5T_m$. At room temperature, standard PbSn solder has a homologous temperature of 0.65, while SnAgCu solder has a homologous temperature of 0.61. During temperature cycling of a flip chip assembly, the rate of deformation is very small, on the order of 10^{-4}/s. In slow strain rate scenarios creep effects are important. A common equation that models creep is

$$\dot{\epsilon} = A_0 \sigma^n e^{\frac{-Q}{R_G T}} \tag{1.39}$$

where A_0 and n are creep specific constants, Q is the activation energy of dislocation motion in the solder, T is absolute temperature, and R_G is the universal gas constant.

These different forms of deformation all become a factor in the deformation of solder bumps as they yield to stress induced by CTE mismatch, but creep strains plays the most prominent role solder deformation and subsequent interconnect failure. Chapter 6 further investigates the limitations of heterogeneous assemblies caused by CTE mismatch.

1.4 State of the Art Microwave Assemblies and Liquid Metal Interconnects

In the previous sections it has been pointed out that shorter path lengths, in addition to reducing signal delay, improve the performance of transitions and transmission lines, particularly when sections of transmission line have mismatched characteristic impedances. Therefore a clear strategy for the microwave frequency package designer is to reduce the overall electrical size of the package. The smaller form factor of a microwave system, the shorter the transmission line lengths, and the higher performance of the overall system,

and the greater capabilities a microwave system can achieve. The goal of shorter overall transmission lines gave rise to the original MCM concept, as pointed out in section 1.1.2, integrating level 1 and level 2 packaging. System on chip (SoC) is the ultimate extension of level 1 and level 2 integration; essentially eliminating level packaging all together by bringing all required functionality of a system into a single chip.

It was previously mentioned that SoC is not always a cost effective solution for many applications. However, for many state-of-the-art high frequency designs, particularly for military applications, cost of a system is not the limiting factor; rather it is achieving very stringent performance parameters. So the subsequent question which could be asked for these applications is: why not invest into developing entire systems on single chips? The short answer to this question is that the highest performance RF/microwave systems cannot (currently) be built on a single, homogeneous chip. While state-of-the-art digital processing and lower-frequency RF functions can be integrated in silicon, designers of high-performance microwave systems rarely have the luxury of finding a single semiconductor technology that provides optimal solutions for all functions of a high frequency system module.

For instance, for mm-wave frequency bands, low noise amplifiers with the most ideal performance capabilities may be in an indium phosphide design technology, but the best performing power amplifier available may be in a gallium nitride technology. And of course, the digital functions of a module will most likely be optimally designed in a Si CMOS based technology.

Not only are different semiconductor technologies optimal for specific active stages within a high frequency module, but materials with low dielectric loss (specifically, varieties of ceramics or polymer substrates) provide the best platform for certain passive functionality, such as baluns, power combiners, and particularly filters and high Q inductors [51].

Rather than a fully SoC design approach, system on package (SoP) designs may be a more flexible strategy for realizing cutting-edge microwave modules. Designers can select the best MMIC technology for each function and integrate those MMICs with high performance

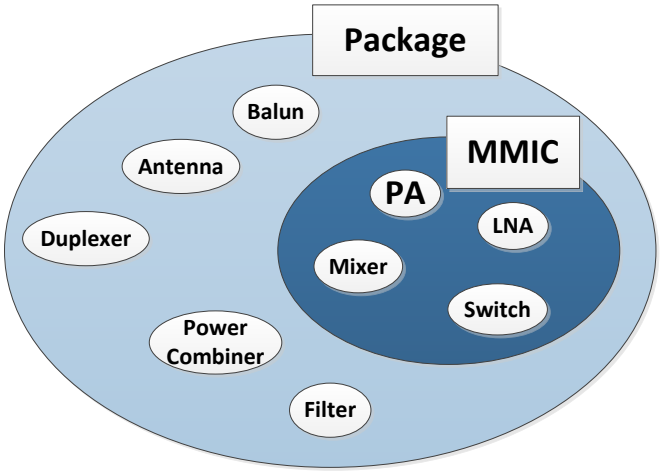

Figure 1.24: System on package design approach for microwave systems.

passive structures built into the package itself [52]. Figure 1.24 depicts this design strategy for high frequency modules. LTCC is one of the potential technologies used for SoP architectures. Another potential SoP technology that can be used in high frequency applications is PolyStrata, which is introduced in Chapter 3.

Meanwhile, significant effort is underway to utilize 3DIC fabrication and assembly strategies to break down the limitations of 2D modules. 3DIC fabrication can be thought of as integrated circuit fabrication which builds active circuitry both laterally and vertically, scaling down total transmission line lengths because the overall footprint is significantly reduced, as seen in Figure 1.25. 3DIC extends the SiP and SoP, chip stacking technology a step farther because for both SiP and SoP technology, chips in package still communicate with each other using off-chip signaling. The goal of 3DIC technology is ultimately to design a system as a single 3D chip.

Technology that has been developed to achieve 3DIC circuit fabrication includes wafer and die bonding strategies, as well as exploiting SOI processes. Advances in thru silicon vias have made stacking of several wafers or die possible [54]. Also, low temperature deposition of silicon layers on top of active circuitry has enabled sequential techniques for layering active circuitry on a single chip without wafer or die bonding.

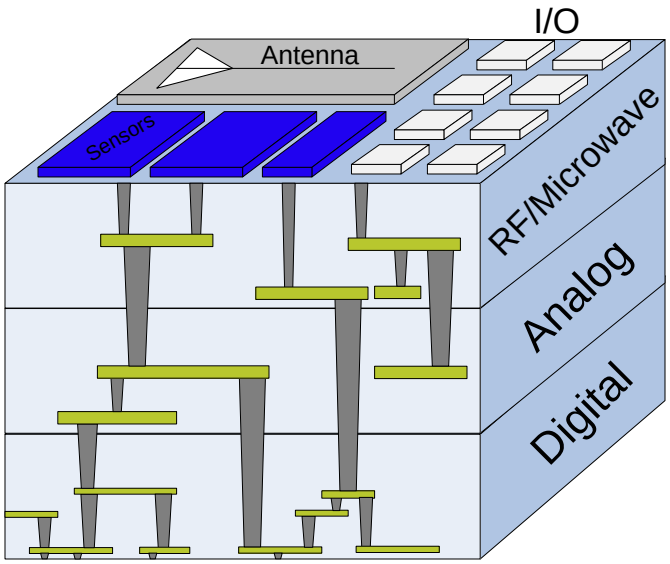

Figure 1.25: Schematic of a 3D IC consisting of three layers of functionality [53].

3DIC technology has significant potential for microwave systems. Research efforts are underway to develop heterogeneous chip integration; the stacking of differing semiconductor layers, allowing designers the flexibility to utilize the optimal active design technology for specific functionality within the complete system "chip". For example, the COSMOS program, funded by DARPA, successfully demonstrated the integration InP and GaN semiconductor devices onto Si CMOS. The integration of high speed InP transistors onto silicon ICs enables design of state of the art mixed-signal ICs such as digital-to-analog converters [55].

SoP and 3DIC are both heavily reliant on innovative level 1 packaging strategies. One of the more challenging assembly issues is how to alleviate stresses induced in these heterogeneous assemblies from coefficient of thermal expansion mismatch. Solder based flip chip interconnections are a step in the right direction for SoP and 3DIC design but the issues that flip chip interconnects have with respect to CTE and rework make it a high risk assembly strategy for many state of the art architectures. As the line between level 1 and level 2 packaging blurs, packaging problems like CTE mismatch and rework become a more pronounced issue, requiring even more careful and complex design and fabrication [56].

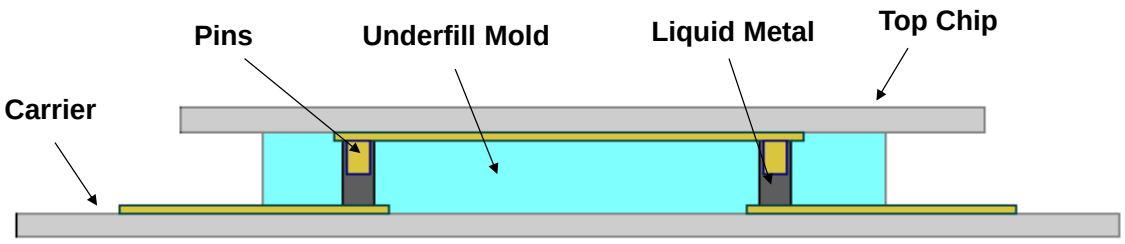

Figure 1.26: Cross section of a basic, liquid metal assembly.

In this dissertation, we explore the use of liquid metal for vertical, flip-chip interconnects in heterogeneous, RF/microwave assemblies. The concept of using liquid metal in integrated circuitry is not an entirely new idea. Other research groups have experimented using liquid metals in chip cooling, MEMS switches, and RF MEMS resonators [57, 58, 59].

A liquid metal flip chip connection utilizes a "pin" and "socket" approach to establishing electrical connections, where the socket is filled with the liquid metal prior to assembly. An underfill mold material creates the socket for the liquid metal to reside in. This pin and socket structure replace a solder bump connection. Figure 1.26 is a basic cross section of a liquid metal interconnection. This assembly configuration accomplishes the same desirable qualities of a flip chip interconnect while also potentially alleviating thermo-mechanical stress problems because it is a flexible interconnect. Additionally, because the electrical connection in this configuration is liquid at room temperature, assembly can also be performed at room temperature. This makes rework potentially much less complicated.

Preliminary work has been performed that demonstrated liquid metal interconnects for passive Si chips onto a Si carrier substrate [60]. The current research described in this dissertation focuses on developing interconnects for active MMIC chips and heterogeneous structures. The following chapters describe this research and outline future work for this research project.

1.5 Dissertation Organization

This introduction has given a detailed background on level 1 electronics packaging and the motivation for developing liquid metal, flip chip interconnections. The remaining chapters of this dissertation are organized as follows.

In Chapter 2, preliminary experiments to interconnect an active device with liquid metal, flip chip interconnections is described. The connection substrate is a high resistivity silicon wafer with CPW transmission lines fabricated on its surface. The design of the assembly, fabrication steps, and the resulting measurements are described in detail.

In Chapter 3, PolyStrata fabrication and design is introduced. A PolyStrata substrate is designed and fabricated to accept both a passive, "through" structure and an active MMIC chip. The results from completed assemblies are compared with simulated results and directly probed MMIC chips.

In Chapter 4, a single liquid metal transition is presented, which has been modeled and designed in HFSS electromagnetic finite element method solver, fabricated in the PolyStrata sequential machining process, and then assembled for testing. S-parameter testing leads to the development of a lumped element model.

In Chapter 5, the power handling capabilities of liquid metal interconnects are tested and verified. Power test assemblies are designed and fabricated and a high power test setup is utilized to apply high power while simultaneously monitoring the liquid metal interconnect performance.

In Chapter 6, thermal testing is performed to verify the mechanical and electrical robustness of this transition. Liquid metal transitions experience temperature cycling, and then are RF tested to verify that they can maintain their electrical performance after being subject to extreme temperatures. Additionally, the electrical performance of a liquid metal transition is monitored as the temperature of the transition is varied; examining the performance of a liquid metal interconnection during the liquid metal's phase change from solid to liquid.

In the final chapter, Chapter 6, conclusions and the recommendations for further research and development work are presented.

Chapter 2

Heterogeneous Liquid Metal Flip Chip Connections: GaAs MMIC onto High Resistivity Silicon Coplanar Waveguide

2.1 Introduction

An initial demonstration of a liquid metal interconnect performed by Wood, et al. [60], was a purely passive assembly, shown in Figure 2.1a. Coplanar waveguide traces were fabricated on high resistivity silicon substrates and the pin and liquid metal socket features were implemented using high-aspect ratio resist (SU-8) structures. The top CPW chip was diced out so that it could be aligned and interconnected to the bottom carrier, simulating a flip chip MMIC. This assembly was tested before and after undergoing thermal cycles ranging from $-10°C$ to $125°C$. The measured results from this thermal cycling demonstration, shown in Figure 2.1b, indicated that liquid metal flip chip interconnects could survive standard

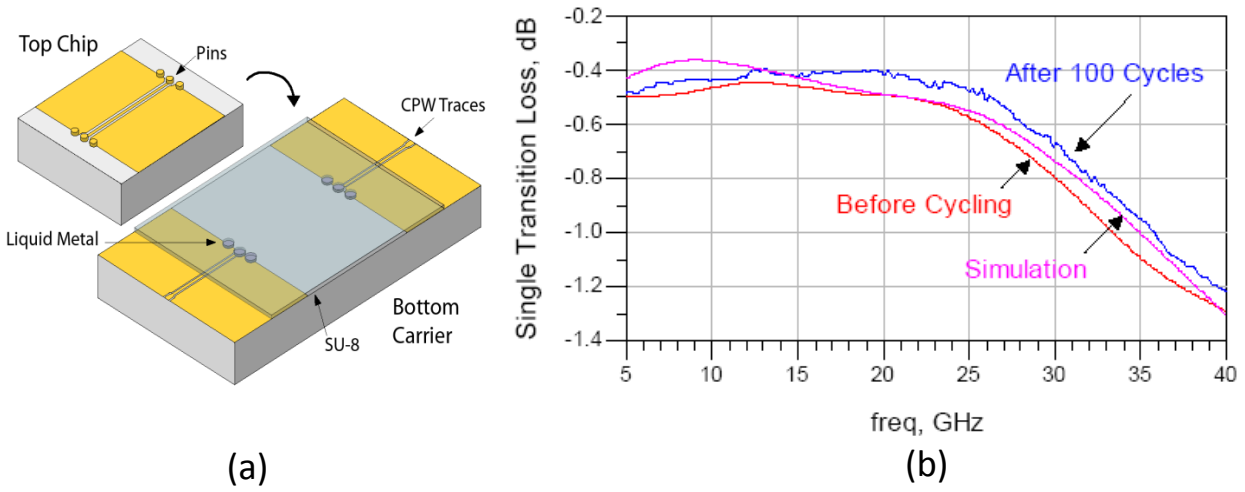

Figure 2.1: (a) 3D view of a simple, liquid metal assembly. (b) Graph showing the simulated and tested transmission loss of the liquid metal assembly.

temperature variations experienced by electronic systems.

The work discussed in this chapter represents the next milestone in the development of liquid metal interconnect assemblies; demonstrating the interconnection of an active, GaAs MMIC to a Si carrier substrate. This heterogeneous assembly exhibits a severe CTE mismatch between the two semiconductor materials (5.8 10^{-6}/°C for GaAs and 3.0 10^{-6}/°C for Si) that would put an otherwise rigid assembly under stress during temperature variations. This work also shows how the liquid metal flip chip connection effects the performance of an active MMIC chip.

2.1.1 Material Selection

This section briefly introduces each of the key materials utilized to realize the demonstrator liquid metal assembly.

Galinstan

There is a limited range of metallic materials to choose from when selecting a liquid metal for level 1 electronic interconnections. There are only two elements that are liquid at room temperature, mercury and bromine, and of these only mercury is an electrically conductive material. Also, both of these elements are toxic. There are other elements that melt close to room temperature: francium, cesium, rubidium, and gallium. Francium is a radioactive material, and cesium and rubidium will violently react with water, making these materials inappropriate for electronic assembly [61].

Gallium is a metal that melts at 30°C, but it can be combined with other low melting point metals to reduce its overall melting point. The most prevalent material, Galinstan, is a gallium based eutectic composed of a combination of gallium, indium, and tin that has a melting point which ranges from $10°C$ to $-19°C$ depending on its percent composition. Compared to mercury it is relatively non toxic and Galistan will readily wet to most surfaces. Galinstan has very low thermal resistance and good electrical resistance. For this research the selected eutectic composition is $Ga_{62}In_{22}Sn_{16}$ (62%Ga, 22%In, 16%Sn) by weight, which has a melting point of $10.7°C$.

Unfortunately, gallium does react with many other metals. It can diffuse into the lattice structure of other metals and create a brittle compound. For example, gallium will corrode aluminum very quickly; it is important that aluminum not be used in the same package as Galinstan. This fact makes the material selection for the pins critical. Some materials that gallium will not react with include nickel, molybdenum, and tungsten [62].

SU-8

Figures 1.26 and 2.1a show the liquid metal deposited into a socket that is formed by an underfill mold. The material selected to serve as this underfill mold in this work is MicroChem's SU-8. SU-8 is a negative, epoxy based photoresist that can form thermally and chemically

stable, permanent layers [63]. It is capable of very high aspect ratios and can be deposited in thickness which range from $0.5\mu m$ to $200\mu m$ in a single spin coat. These qualities have made it a popular material selected for micromachining, microelectronics, and MEMS applications and a good underfill material for the proposed vertical liquid metal interconnect structure.

KMPR

Creating high aspect ratio pins requires using a LIGA process, much like one used for copper pillar bumping, as shown in Figure 1.9. This process requires a temporary, thick photoresist that serves as a mold for metal electroplating (Figure 1.9b and 1.9c). The photoresist that is used for this step is MicroChem's KMPR. This photoresist has very similar properties to SU-8; it is also a thick, negative photoresist which is thermally and chemically stable once it has been developed. It has the same high aspect ratio qualities and can create layers as thick as $120\mu m$ in a single spin [64]. The predominant difference between SU-8 and KMPR is that, once deposited and patterned, KMPR can easily be removed with strong solvents where as SU-8 must be dry etched for complete removal. This makes KMPR an ideal photoresist for temporary molds high aspect ratio.

2.1.2 GaAs MMIC

The GaAs MMIC used in these demonstrations is a M/A-COM MAAM-007523 three-stage driver amplifier chip, shown in Figure 2.2. The MMIC's input and output ports are matched on chip to 50Ω. There are two drain supply voltage pads, one that accepts an eight volt input and the other for a five volt input, and there is an on-chip bias network for generating V_{GS} [65]. This chip has a specified bandwidth of 4.9-8.5 GHz and a small signal gain of 23 dB.

Figure 2.2 shows the bond pad locations on the chip and the overall chip dimensions. The final thickness of the chip is $100\mu m$ and it has a backside ground plane which connects

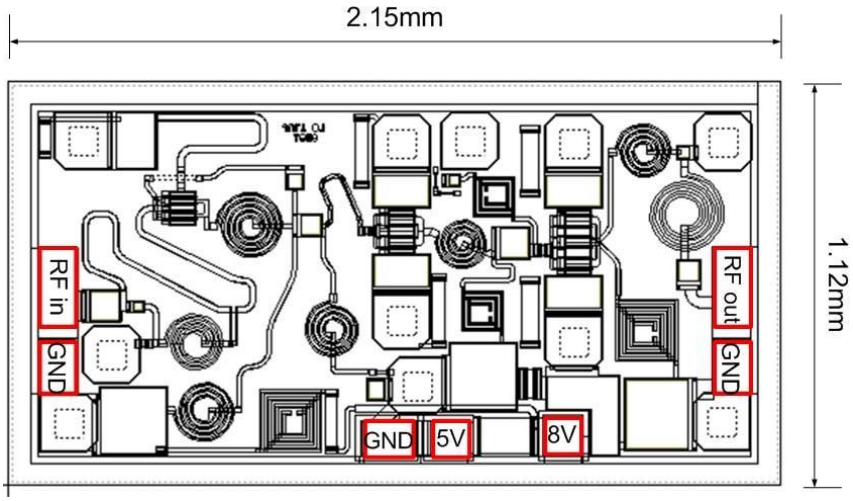

Figure 2.2: Drawing of MAAM-007523 with labeled bond pads [65].

with the top surface of the chip with backside vias. There is a $4\mu m$ thick layer of polyimide that uniformly covers the top surface of the chip, aside from the bond pads. The polyimide acts as a protective coating against chemical and mechanical damage. It should be noted that the chip has ground pads on its top surface for ease of test and verification of individual MMICs. These ground pads are leveraged in this work for the flip chip configuration.

There are two fabrication approaches that were pursued in this research: fabricating pins on the Si substrate with the liquid metal sockets on the GaAs MMIC, the "pins-on-Si" assembly; and fabricating the liquid metal sockets on the Si substrate with the pins on the GaAs MMIC, the "pins-on-MMIC" assembly. The following sections describe the fabrication steps taken to realize these structures and the measured results acquired from completed assemblies.

2.2 Pins-on-Silicon Substrate Assembly

This approach to liquid metal connection flip-chip of an active MMIC to transmission lines on a Si substrate has the pins electroplated onto the surface of the Si substrate wafer and

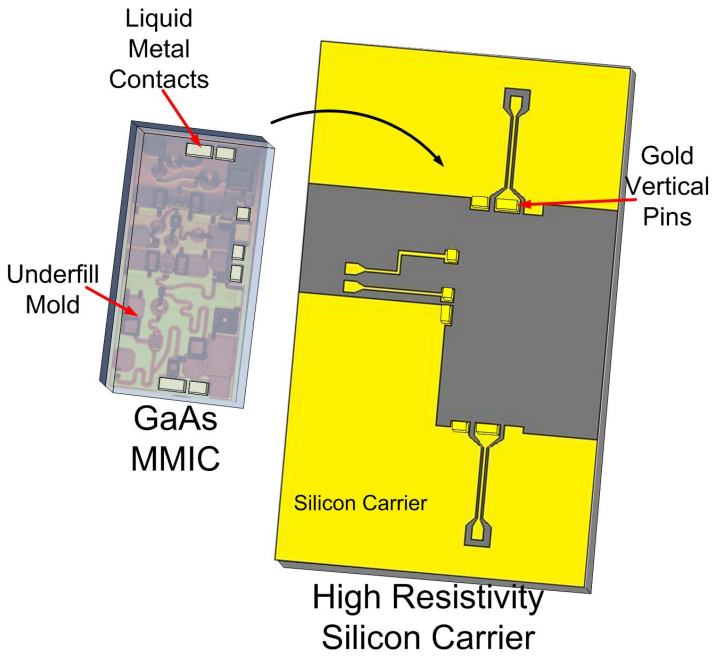

Figure 2.3: Liquid metal, flip chip assembly of MMIC onto a Si substrate. The assembly pins are on the Si substrate and the liquid metal sockets are on the GaAs MMIC.

the liquid metal sockets added to the top surface of the GaAs MMIC. Figure 2.3 depicts both the substrate and GaAs chip with their respective socket and pin configuration. This section covers the process steps that are required to build such an assembly.

2.2.1 Fabrication of Pins On Silicon Substrate

Figure 2.4 presents the major process steps for preparing the Si carrier substrate. These steps are as follows:

(a) Deposit a seed layer of titanium on the surface of a silicon wafer.

(b) Using a liftoff process, pattern Au signal traces on the surface of the Ti layer.

(c) Deposit and pattern KMPR onto the wafer surface.

(d) Electroplate gold pins in exposed regions of the wafer.

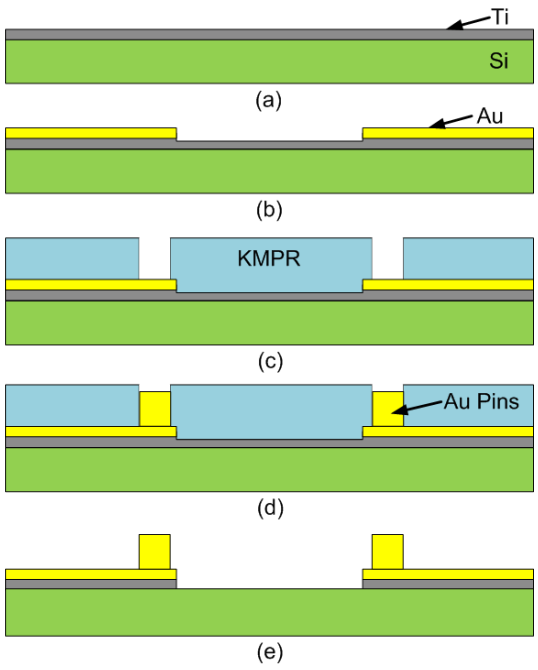

Figure 2.4: Cross section of process steps used to create the silicon carrier substrate with gold pins.

(e) Remove KMPR and etch back Ti seed layer.

The Si carrier substrate incorporates two DC lines which connect to the drain supply voltage pads of the MMIC, two RF CPW traces which connect to the MMIC's RF input and output, and a ground plane which connects to three ground pads on the MMIC (Figure 2.5). The gap and width (G and W) dimensions of the CPW are $16\mu m$ and $30\mu m$ respectively. The CPW traces were designed using Sonnet, a high frequency full wave electromagnetic software which simulates planar microwave components very well. The CPW traces are designed to have a characteristic impedance of 50Ω and the terminating probe pads are designed for ground-signal-ground (GSG), $150\mu m$ pitch probes. The DC probe pads also have a pitch of $150\mu m$.

The Si wafer processing starts with an $80nm$ thick Ti layer that is e-beam evaporated onto the surface of a high resistivity wafer using a Kurt J Lesker 250-PVD. This thin flim

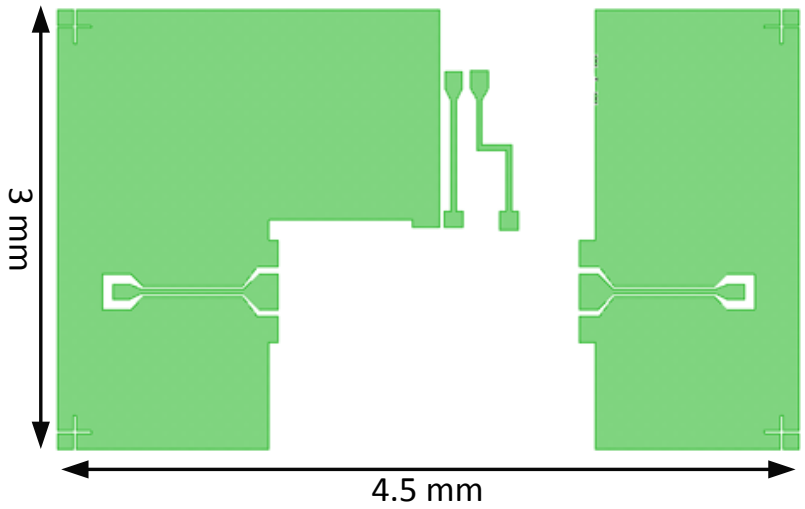

Figure 2.5: Mask layout of signal and ground pattern which is deposited in gold on the high resistivity Si substrate.

of Ti is a seed layer for electroplating. It is important to deposit this seed layer before patterning the signal lines because in order to perform uniform, wafer scale electroplating there needs to be electrical continuity on the surface of the wafer. If there is a significant resistance across the wafer's surface, there will be a significant voltage potential across the surface of the wafer during electroplating, causing inconsistent plating heights and plating quality.

An image reversal photoresist, AZ5214, is deposited and patterned on the surface of the wafer. This photoresist creates a negative of the image shown in Figure 2.5, remaining in areas where gold is not desired. This photoresist has a negative wall profile; the cross section of the photoresist pattern appears undercut. Appendix A contains the processing parameters used for the deposition and development of AZ5214 photoresist.

With the AZ5214 pattern on the wafer, another Ti layer, $20nm$ thick, is deposited to promote good adhesion between the Ti/Au layer. Before breaking vacuum in the e-beam chamber, a $400nm$ thick Au layer is also deposited. Since e-beam evaporators deposit materials in a line-of-sight mode, the undercut photoresist edges do not get coated with the Ti/Au layer. Soaking the wafer in acetone and applying ultrasonic agitation will remove the

photoresist, lifting off metal layers that were evaporated onto the photoresist, and leaving a patterned, gold surface behind.

The KMPR photoresist spin deposition is controlled so that its final thickness is approximately $50\mu m$. These process parameters can be found in Appendix A. Openings in the KMPR pattern define the location and area of the gold pins. After developing KMPR it is important to perform an O_2 plasma etch to remove residual resist that remains on the surface of opening in the KMPR. If this step is not performed, good adhesion will not be obtained between the CPW's gold surface and electroplated gold pins. However, the parameters of the plasma etch are critical because if the surface is etched too much, the surface energy of the exposed gold will become high enough to cause some gold to evaporate and redeposit on the sidewalls of the KMPR mold. Figure 2.6 shows two gold pins electroplated with the same plating parameters, but different plasma etch parameters. The gold pin on the left underwent an 100 W etch for 2 minutes while the pin on the right underwent a 50 W etch for 1 min. The higher energy etch redeposited gold on the sidewalls of the KMPR. Subsequently, during plating, these sidewalls plated up gold, creating a taller, but less physically robust gold structure.

Electroplating wax is applied to the back of the Si wafer to prevent plating from occurring on the backside of the wafer. All gold electroplating was conducted with Technic gold plating solution, RG-25. This is a non-cyanide based electroplating solution that is compatible with most photoresists. Plating parameters are given in Appendix A. The gold pins were plated to a height of approximately $30\mu m$.

Immediately after the plating is completed the electroplating wax is peeled off and then the KMPR is dissolved in solvent. The exposed Ti seed layer is then removed in dilute hydrofluoric acid. The Si carrier substrate is then ready for liquid metal, flip chip assembly of the GaAs MMIC.

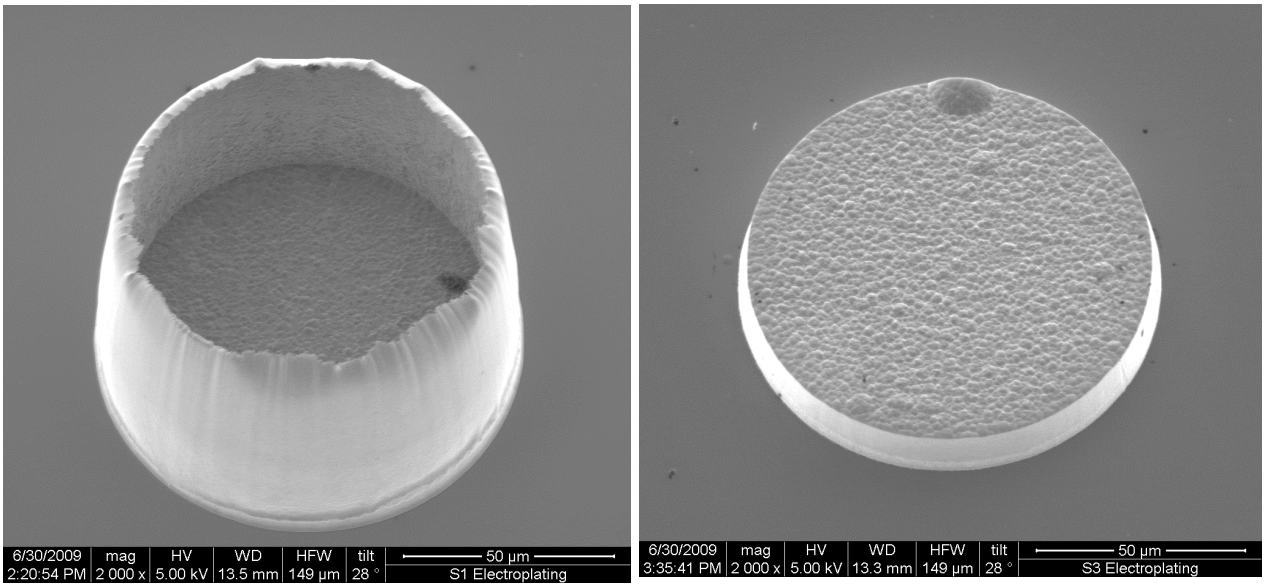

Figure 2.6: The image on the left is a gold pin that was electroplated after a 100 W, 2 min O_2 plasma etch. The image on the right is a gold pin electroplated with the same plating parameters but a 50 W, 1 min O_2 plasma etch.

2.2.2 Fabrication of Liquid Metal Sockets on GaAs MMIC

The major process steps for fabricating the liquid metal sockets onto the GaAs MMIC are shown in Figure 2.7. A basic description of each step is as follows:

(a) Place GaAs MMIC into cavity which has been anisotropically etched into a Si handle wafer with a DRIE to create a near planar surface across tops of MMIC and the Si wafer.

(b) Deposit and pattern SU-8 sockets over MMIC bond pads.

(c) Deposit liquid metal into SU-8 sockets.

(d) Remove MMIC from Si cavity.

(e) Flip chip align MMIC sockets with Si carrier substrate pins.

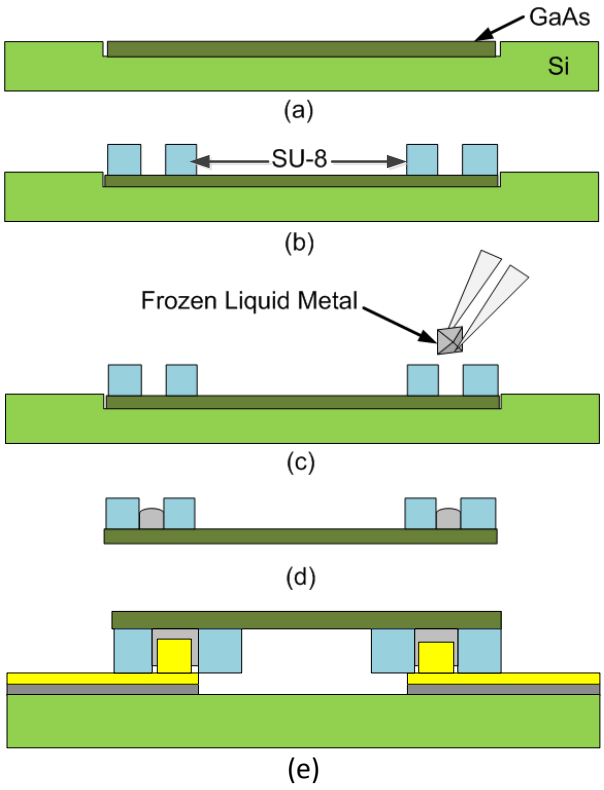

Figure 2.7: Cross section of process steps used to create liquid metal sockets on a MMIC chip.

Because processing must be performed on individual GaAs chips rather than an undiced wafer, a sacrificial Si wafer is used as a handling platform. High aspect ratio cavities are etched in the sacrificial wafer using an Alcatel Deep Reactive Ion Etcher, DRIE. The cavities are micromachined such that the chip tightly fits inside the cavity and the surface of the MMIC is approximately in the same plane as the surface of the Si wafer, allowing for photoresist continuity when the resist is spun onto the Si wafer surface.

SU-8 photoresist is deposited with a layer thickness of approximately $50\mu m$. Process parameters for the SU-8 deposition and patterning can be found in Appendix A. The SU-8 uniformly covers the surface of the MMIC, and is patterned to have openings at the bond pads. Figure 2.8 shows microscope images of these sockets on the MMIC.

Depositing liquid metal into the SU-8 sockets is a challenging step. Originally it was performed by masking out all but the socket openings on the chip using S1813 photoresist,

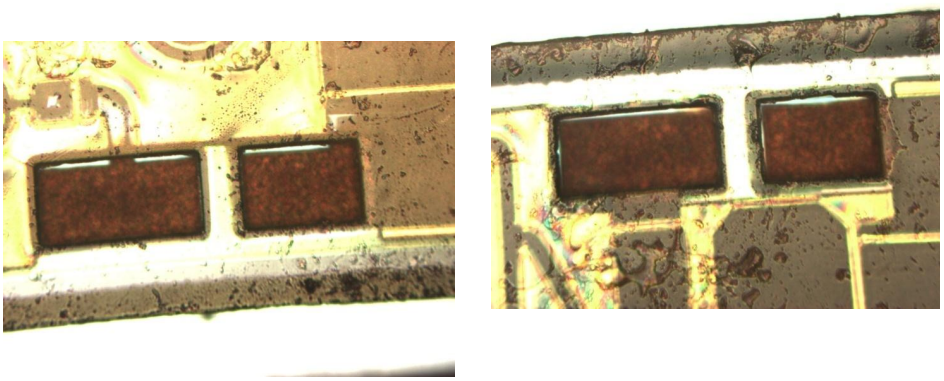

Figure 2.8: Microscope images of SU-8 sockets on the GaAs MMIC chip's signal input and output bond pads.

depositing the liquid metal over the surface of the chip such that it fills the sockets (Figure 2.9a), and then using a "squeegee" to remove excess liquid metal (Figure 2.9b). This method was simple but messy, and because galinstan has such high surface tension it did not consistently deposit uniform volumes of liquid metal in the different MMIC sockets. Figure 2.10 shows pictures of some of the sockets after such depositions.

Consequently an improved process was developed which uses an intermediate mold made of anisotropically etched silicon. Figure 2.11 shows a cross section of the steps required to make this mold. Starting with a type (100) Si wafer with a layer of SiO_2 grown on its surface (Figure 2.11a), photoresist is deposited and patterned on the surface of the chip (Figure 2.11b). The SiO_2 is etched back (Figure 2.11c) and then the Si wafer is etched TMAH (Figure 2.11d). Because TMAH does not etch Si in the $< 111 >$ plane, the volume of the cavity anisotropically formed in Si by TMAH can easily be controlled by adjusting the area of the opening in SiO_2 [66]. The surfaces of the Si cavities are smooth and they are sloped at an angle of 54.7°, making it easy for Galinstan to flow into and fill them with a squeegee (Figure 2.11e). Once liquid metal is deposited into the Si cavities, the wafer is exposed to dry ice, dropping the liquid metal's temperature to $-78°C$ and freezing it (Figure 2.11f). In a solid state, the liquid metal is easy to handle, it can be picked up with small tweezers or a DC probe and placed in the MMIC's SU-8 sockets.

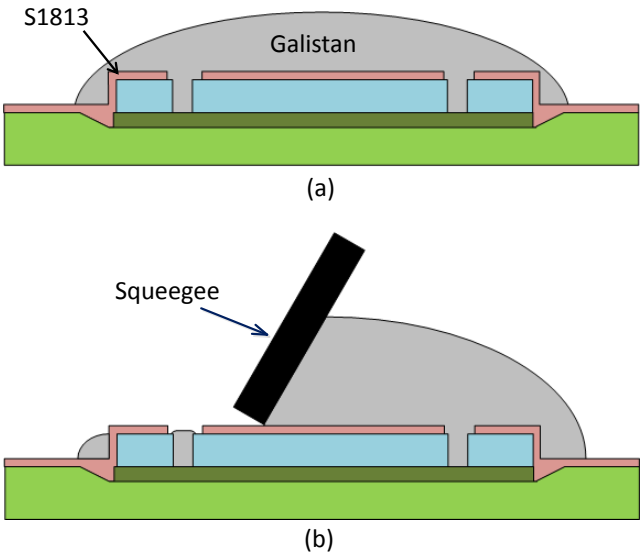

Figure 2.9: Squeegee method for depositing liquid metal. (a) Photoresist S1813 is used to mask surfaces of the chip and galistan is deposited over the chip. (b) A squeegee removes the excess liquid metal.

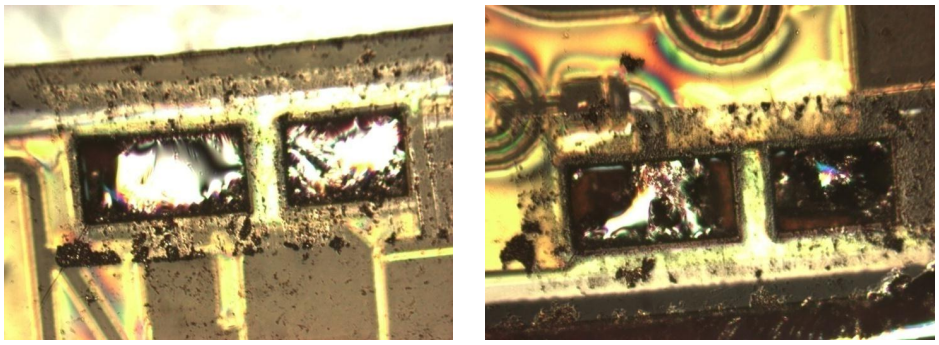

Figure 2.10: Microscope images of SU-8 sockets with liquid metal deposited via squeegee method.

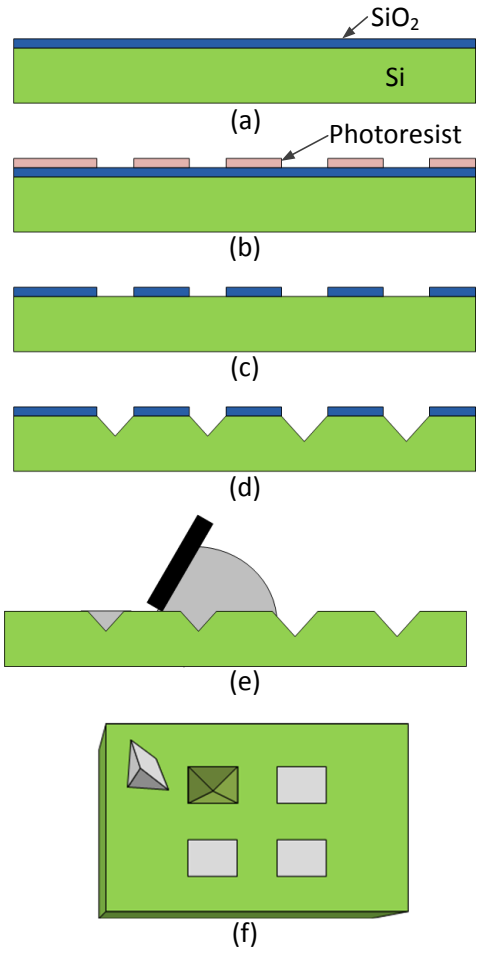

Figure 2.11: Cross section of process steps used to make liquid metal stencil.

Once liquid metal is in the liquid metal sockets, the MMIC chip is aligned and mounted on to the Si substrate using a Finetech Lambda Flip Chip Bonder. This tool uses split optics to perform the chip alignment, allowing the operator to see the top surface of the chip and the top surface of the substrate simultaneously before bonding. 1 micron alignment accuracy can be achieved with the Lambda Bonder, exceeding the alignment requirements of this assembly. Elevated temperature cycling is not needed for this assembly, and minimal pressure is required to bring the chip and substrate together. The Lambda bonder applies a minimum pressure of about 0.5 Newtons. Figure 2.12 is an image of a completed flip chip assembly on the silicon carrier.

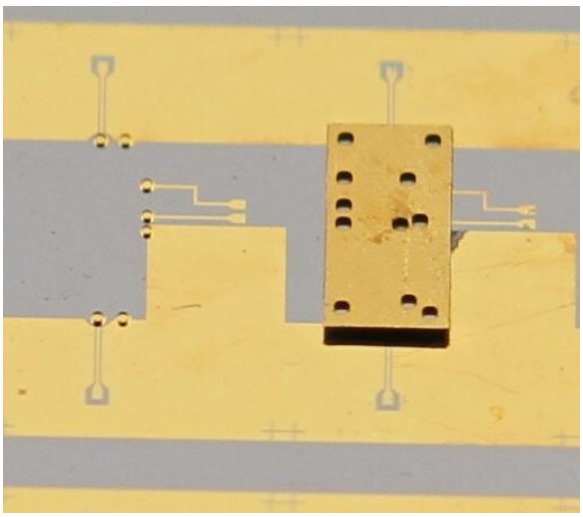

Figure 2.12: MMIC chip sitting face down Si substrate.

2.2.3 Measured Results and Discussion

RF measurements were taken with an Agilent 8364B Vector Network Analyzer and Cascade Air Coplanar GSG probes with pitch of 150μm. The VNA, cables, and probes were calibrated with a standard, SOLT calibration over a frequency range of 1 - 15 GHz. The reference plane of the measurement is at the probe tips.

The results from initial liquid metal, flip chip assemblies had severe peaks in the band of interest, indicative of oscillations (red traces in Figure 2.13). After further investigation it was determined that the grounding planes of the Si substrate were not sufficiently connected. Consequently, strips of gold ribbon wire were used to better connect the two ground planes (Figure 2.14), resulting in improved performance without significant oscillations, as indicated by the blue traces in Figure 2.13. Both measurements had an applied V_{DD} of 5V and current, I_{DQ}, of 150mA. These substantial differences in post assembly performance highlight the importance of proper grounding.

Using thru lines included on the Si substrate, insertion loss caused by the probe pad contacts and CPW lines was measured and is shown in Figure 2.15. Dembedding the losses

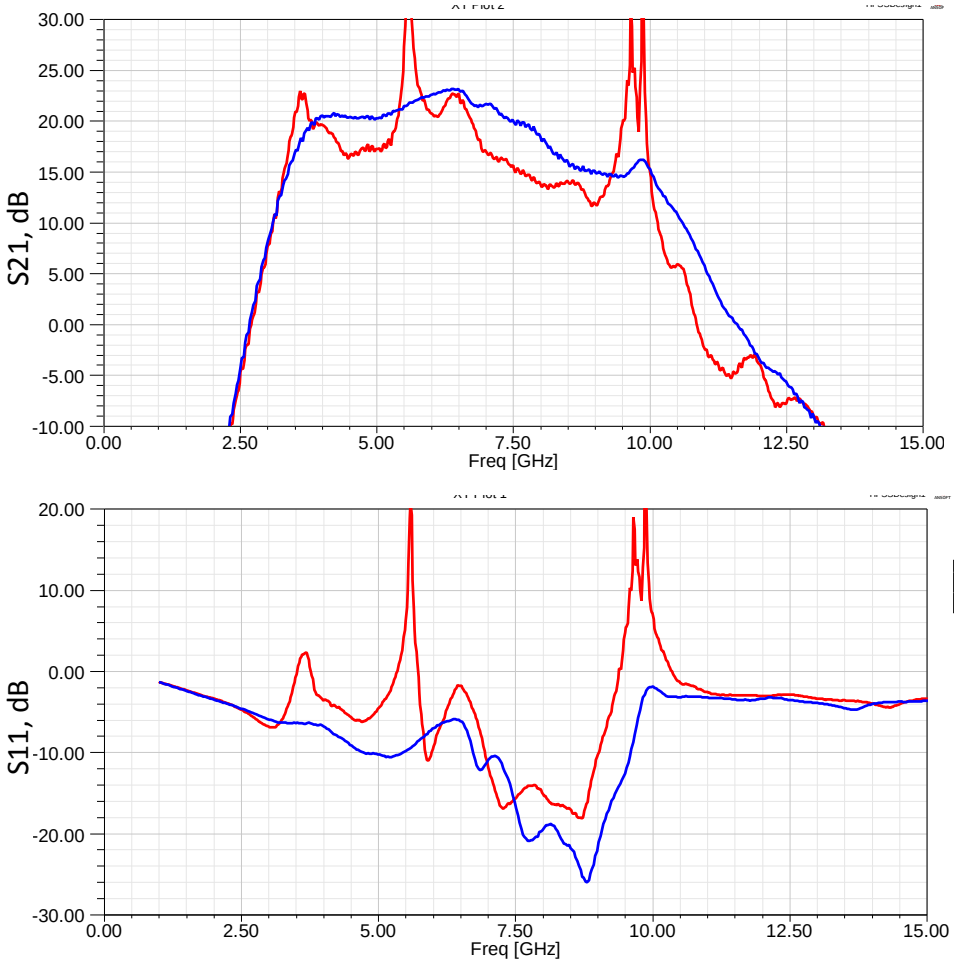

Figure 2.13: (a) S21 and (b) S11 data from MMIC driver chip probed via liquid metal interconnects. The red lines are measurements from an initial, poorly grounded chip, and the blue lines are measurements from a chip with improved grounding.

caused by these thru lines by subtracting their S-parameter data using Equation 2.1 gives a more accurate measure of the overall performance of the assembly.

$$S_{21assembly} = 10log\left(\frac{\mid S_{21measured} \mid^2}{1- \mid S_{21measured} \mid^2}\right) - 10log\left(\frac{\mid S_{21thru} \mid^2}{1- \mid S_{21thru} \mid^2}\right) \tag{2.1}$$

Figure 2.16 gives a comparison of directly probed MMIC measurements and measurements of the liquid metal transition assembly.

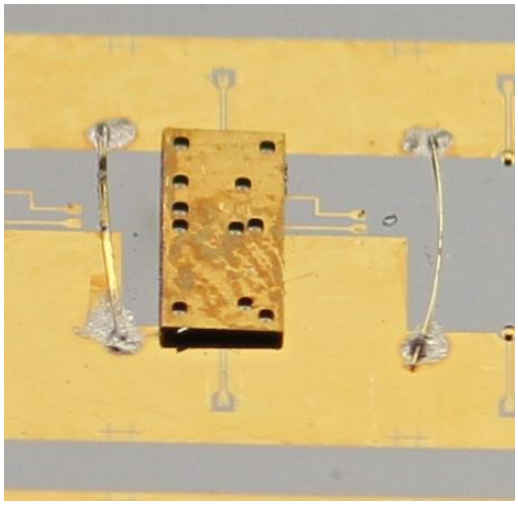

Figure 2.14: MMIC chip mounted to Si substrate with gold ribbon wires connecting the grounding planes.

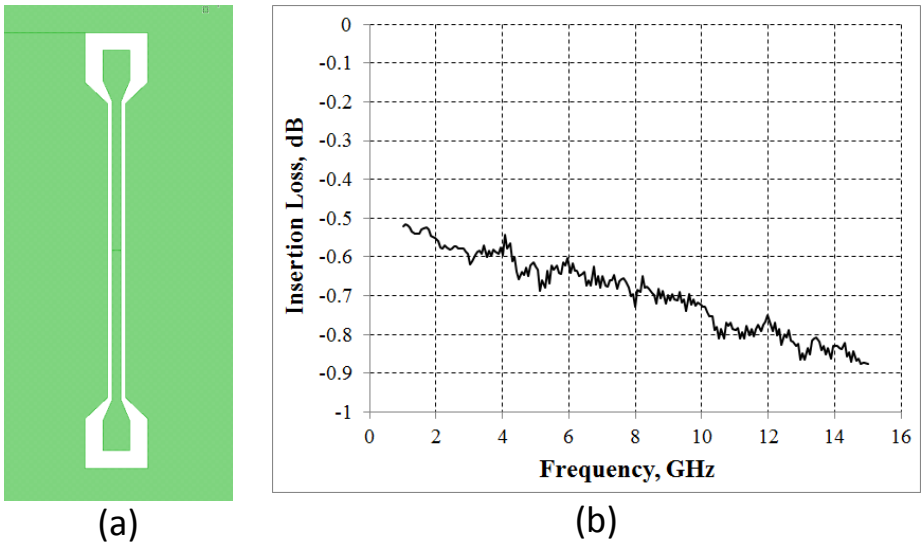

Figure 2.15: Si CPW thru line (a) layout and (b) insertion loss.

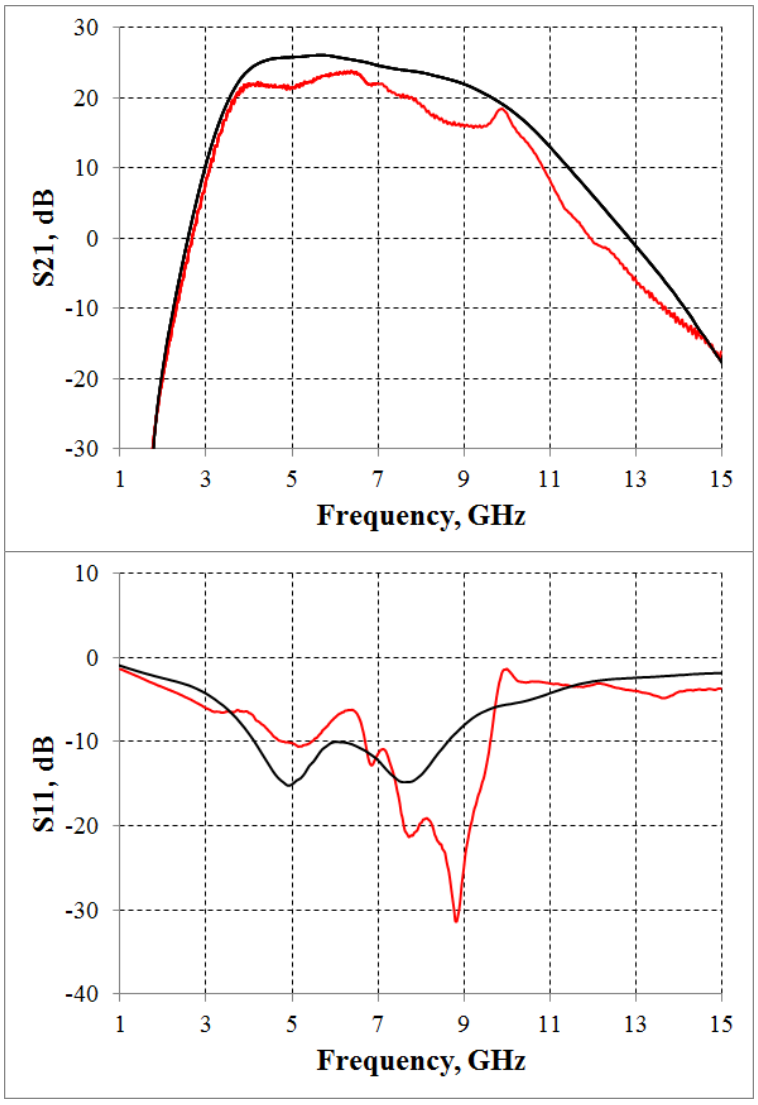

Figure 2.16: Comparison of MMIC driver chip's directly probed performance (black traces) to the performance of a MMIC assembled at a Si substrate with liquid metal interconnects (red traces).

Discussion

The results shown in Figure 2.16 show that the vertical liquid metal interconnects perform reasonably well at microwave frequencies. There are discrepancies in the return loss compared to the directly probed device. The loss per transition, calculated using

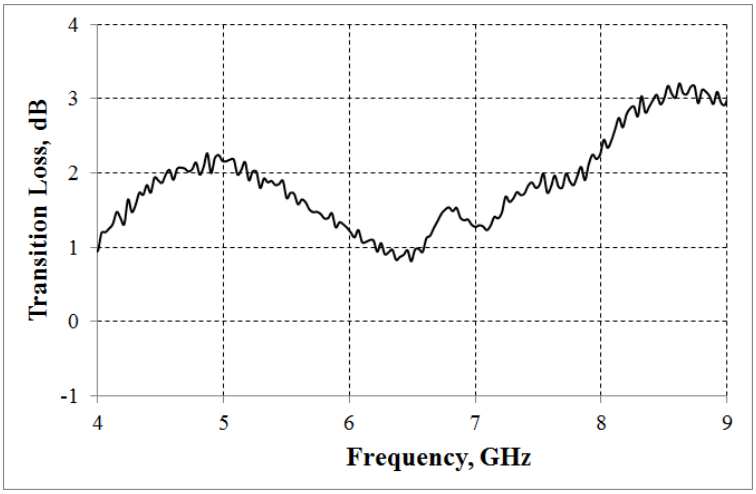

Figure 2.17: The loss of the liquid metal interconnect assembly, per transition.

$$IL(dB) = \frac{1}{2}\left(10log\left(\frac{\mid S_{21probed}\mid^2}{1-\mid S_{11probed}\mid^2}\right) - 10log\left(\frac{\mid S_{21measured}\mid^2}{1-\mid S_{11measured}\mid^2}\right) - 10log\left(\frac{\mid S_{21thru}\mid^2}{1-\mid S_{11thru}\mid^2}\right)\right) \tag{2.2}$$

is shown in Figure 2.17. The assembly has an average insertion loss value of 1.8dB over the frequency band of the MMIC. While some of the transition loss can be attributed to resistive losses of the liquid metal transition and impedance mismatch at the transition, there are several other factors that likely degrade the performance of the flip-chipped MMIC and therefore negatively effect the assembly's overall performance.

One factor that has already been mentioned is grounding. This chip was designed for wirebond assembly and has a backside ground plane which would typically ground the chip to its package substrate. In this flip-chip configuration, the backside ground is only connected through vias and the liquid metal contacts to the CPW carrier ground plane. Any voltage difference between the chip's ground path and the Si substrate will cause the MMIC's transistors to shift from their ideal design Q points. Figure 2.13 shows in impact of improving the Si substrate ground plane on the performance of the overall assembly; better on-chip grounding would likely also yield significant improvements to the chip's return loss.

Heat dissipation is another potential problem. When this driver chip is operating withing

its specification, it is dissipating over 0.5 Watts of power. In this flip chip configuration, nearly all the heat is carried away from the chip through the pin/socket transitions, despite the thermal conductivity of Galinstan being high compared to most metals. If this is causing the chip's temperature to exceed its rated temperature, it could be degrading its overall performance.

Another factor that likely degraded the chip's performance is the presence of the SU-8 on the MMIC's surface. SU-8 has a dielectric constant of approximately 4.1 and a dielectric loss tangent of 0.015 [67]. This will increase the dielectric losses of the microstrip lines on the MMIC, and may also change the impedance of these microstrip lines and the Q of the MMIC's inductors.

Complete MMIC assemblies as presented in this chapter were exposed to thermal cycling after initial measurements were taken. These assemblies did not survive thermal cycling; measurements made after thermal cycling showed lack of chip connection to the CPW lines on the Si substrate. This could be due to diffusion of the gallium in Galinstan into the gold pins, causing the pins to brittle and then break. Future work resolves this issue by coating the pins with metals which are resistant to gallium diffusion.

2.3 Pins-on-MMIC Assembly

A liquid metal interconnect assembly with the socket structure on the substrate rather than on the chip is a more desirable configuration for several reasons. Firstly, adding a pin feature to an IC chip (chip "bumping") is already a common, wafer level process, whereas adding thick polymer features to the surface of an IC and inserting liquid metal in these features is not. Therefore it would be easier for a designer of custom multichip modules or SiPs to acquire MMICs designed for flip chip assembly and then build an in-house custom substrate with liquid metal connections.

Additionally, SU-8 is a polymer that needs to be hard baked in order for it to fully cross

link. Complete cross linking will stabilize the electrical characteristics, dielectric constant and loss tangent, of SU-8. This means exposing SU-8 to high temperatures for an extended cycle, typically $150°C$ for 30 minutes [67]. It may not be acceptable to expose certain MMICs to such elevated temperatures for extended periods of time.

However, an assembly that has the pin side of the connection on the MMIC rather than the substrate is a much more challenging to fabricate because, for this demonstration, the processing must be performed on individual chips rather than whole wafers. There are two industry standard ways that metal, non-solder, pins can be applied to a wafer's surface; LIGA electroplating as described previously in this chapter and gold stud bumping as mentioned in Section 1.1.3. Since the author did not have access to equipment that could manually apply stud bumps, the only approach to this task is to electroplate the bumps onto the GaAs MMIC's surface. The following describes the processing steps required to build this assembly.

2.3.1 Fabrication of Liquid Metal Socket onto Si Substrate

Figure 2.18 depicts the Si substrate with liquid metal sockets fabricated on the surface. Several design changes were made to improve the performance of the liquid metal, flip chip interconnect. The substrate layout contains CPW lines for input and output signals and DC bias lines, but the CPW ground plane has been extended to improve the assembly's grounding. Additionally, the SU-8 underfill is designed to have minimal surface overlap with the MMIC, reducing the SU-8 dielectric effects on the performance of the chip. The fabrication steps are shown in Figure 2.19, are summarized as follows:

(a) The Ti/Au signal traces and ground plane are deposited on the surface, using a liftoff etch process.

(b) Deposit and pattern SU-8 sockets over substrate transition pads.

(c) Place frozen liquid metal into SU-8 sockets.

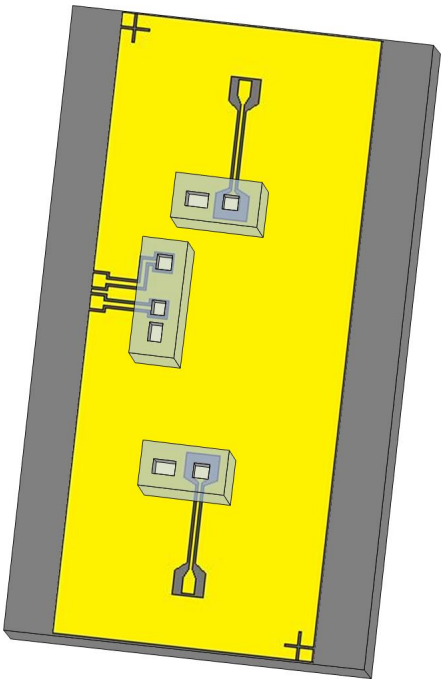

Figure 2.18: Si substrate with liquid metal sockets.

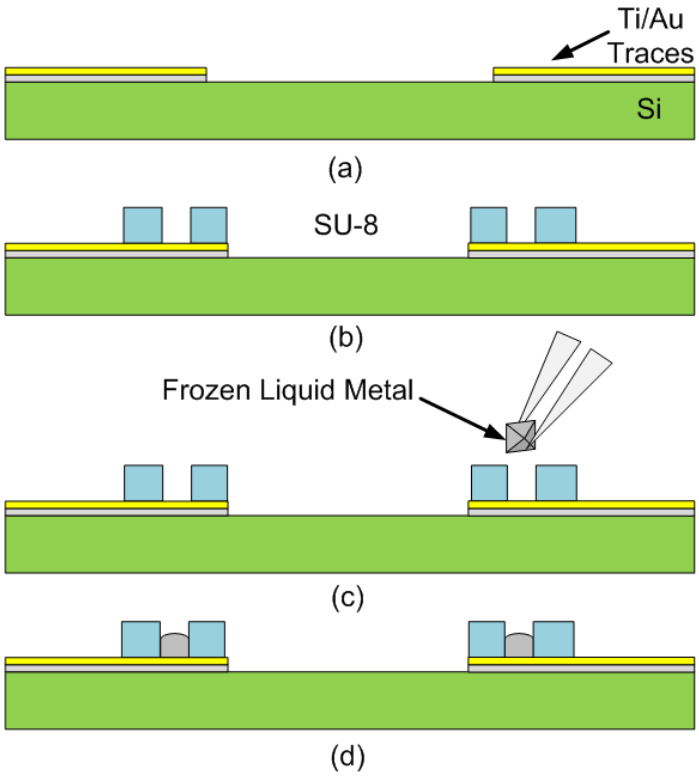

Figure 2.19: Cross section of process steps used to create liquid metal sockets on Si substrate.

(d) Substrate is ready for MMIC alignment.

The process steps to prepare the Si substrate for liquid metal, flip chip assembly have already been established when processing the pins-on-Si substrate assembly, described in Section 2.2.2. AZ5214 photoresist is used in the liftoff etch to define the substrate traces, SU-8 is processed to have a final thickness of approximately $50\mu m$ on the wafer, and the liquid metal is deposited in the sockets using the same Si mold to freeze and place the liquid metal in sockets.

2.3.2 Fabrication of Pin onto GaAs MMIC

Figure 2.20 shows the fabrication steps for growing pins on the surface of individual MMIC chips. The processing requires more steps, as follows:

(a) Place GaAs MMIC into cavity which has been anisotropically etched into a Si handle wafer with a DRIE.

(b) Deposit and pattern AZ9260 photoresist on Si surface.

(c) Hard bake the AZ9260.

(d) Deposit a seed layer of Ti/Au on the Si surface.

(e) Deposit and pattern KMPR for the pin electroplating mold.

(f) Electroplate copper pins onto the surface of the MMIC chip.

(g) Remove the KMPR and AZ9240 from the surface of the chip. Coat pins with ENEPIG (electroless nickel, electroless palladium, immersion gold) surface finish. Chip is now ready for flip chip assembly.

This process begins with etching 6 cavities in a Si handle wafer. The smallest cavity has overall dimensions of 2.15mm by 1.12mm and the largest cavity has dimensions of 2.225mm

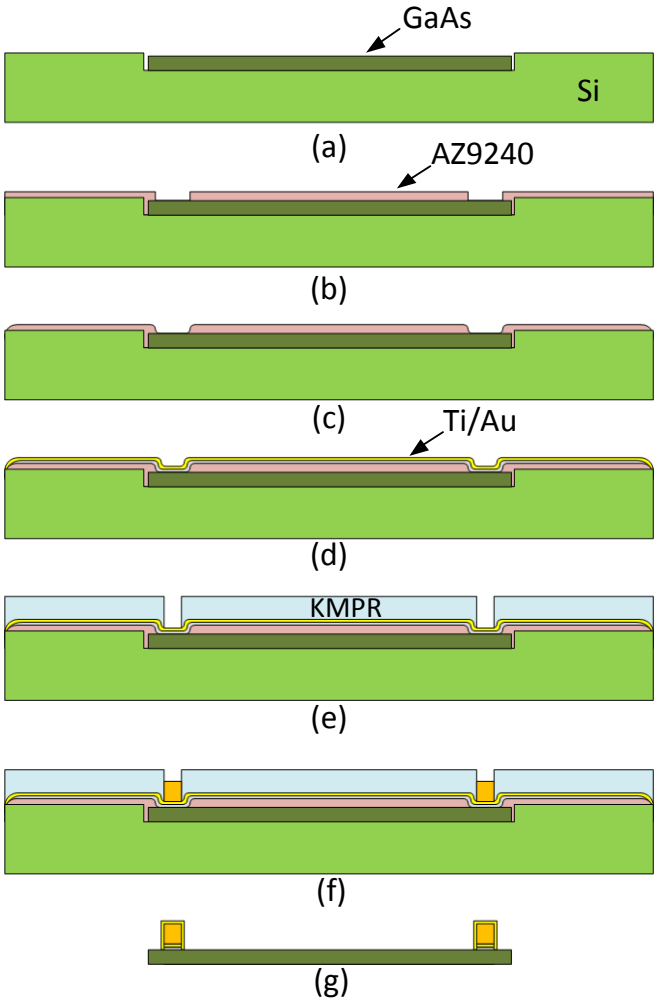

Figure 2.20: Cross section of process steps used to create liquid metal sockets on Si substrate.

by 1.195mm. The MMIC chip is placed in smallest cavity that it will fit into. By doing this, the gap between the edge of the MMIC and the Si cavity is minimized, increasing the continuity of the AZ9260 photoresist when it is deposited over the entire surface.

The AZ9260 photoresist pattern should provide complete coverage of the MMICs surface except at the bond pads where the pins will be electroplated. For this purpose, it would be more desirable to use a negative photoresist rather than a positive photoresist because the required alignment is very challenging. The properties of positive photoresist dictate that the only openings in the chrome photo mask should be for the bond pads. However, negative photoresist generally has bad step coverage, making it a poor choice as an intermediate

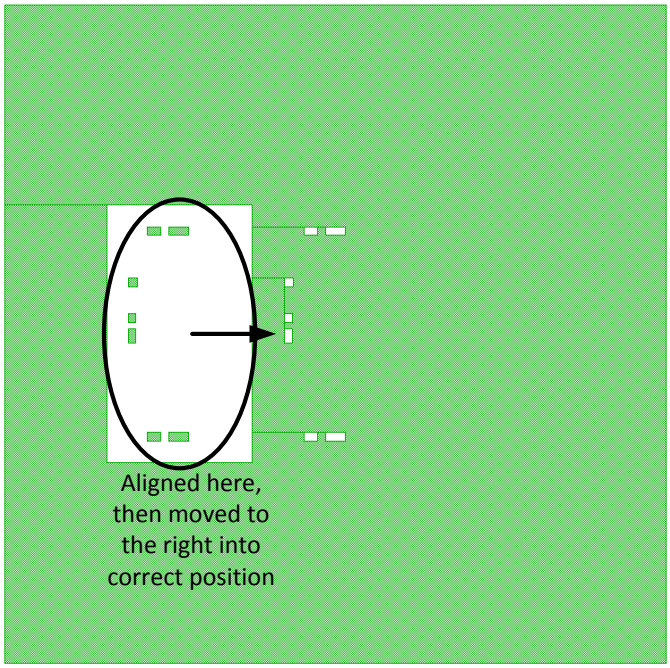

Figure 2.21: The AZ9260 mask used to align the MMIC bond pads.

layer to provide surface continuity [66]. Therefore, positive photoresist must be used. Good alignment is achieved by first aligning the chip near the mask pattern used to expose the MMIC surface and then moving the chip into position. Figure 2.21 shows this mask layout. The green pattern represents the areas of chrome on the mask. The chip is aligned to the features on the left side of the mask and then the chip is moved in the X direction to the features immediately to the right. The small openings in the chrome represent the openings in the photoresist for the bond pads so that there will be seed layer continuity to all pads.

AZ9260 photoresist is a positive, high resolution thick photoresist that can have layer thicknesses ranging from 4 - 24μm [68]. For this application, the resist has a thickness of approximately 6μm, process steps are included in Appendix A. This is thick enough to provide good step coverage over the cavity and MMIC edges, but also thin enough that the seed layer still has good continuity over patterned openings in the resist. Another good property of AZ9260 resist is its ability to develop rounded edges when it is hard baked after pattern development. Figure 2.22 shows micrographs of AZ9260 photoresist before and after

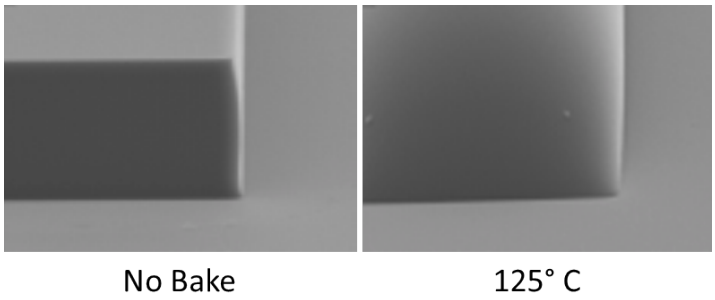

Figure 2.22: Pictures showing sidewalls of AZ9260 photoresist before and after a 120 second hard bake at 120°C [68].

a hard bake of 125°C for 120 seconds. This hard bake also removes any remaining solvents from the photoresist. This is important because, if the photoresist out gases after the Ti/Au seed layer has been deposited, the seed layer will wrinkle and crack.

The Kurt Lesker PVD-250 is again used to evaporate the Ti/Au seed layer over the surface of the Si wafer. Approximately 200nm of Ti and the 50nm of Au are deposited. The evaporation rate is kept very low for this deposition, no more than 2 Angstroms per second, in order to keep the surface of the Si wafer and the MMIC chip at a reasonably low temperature. It also keeps the photoresist from expanding too much during metal deposition so that it will not contract significantly once it cools off, which would cause the seed layer to wrinkle and crack.

The thicker layer of Ti deposited on the surface of the Si and MMIC chip creates a protective layer between the AZ9260 photoresist and the KMPR. This keeps the AZ9260 from reabsorbing solvents from the KMPR which would cause the AZ9260 the swell and crack, again compromising the seed layer.

The KMPR is deposited to have a thickness of approximately $50\mu m$. The MMIC chip has a rough gold surface on its bond pads to enhance the compatibility of their surfaces with ultrasonic wirebonding. During the UV exposure of the KMPR, this rough surface will reflect UV light at random angles, reflecting some of the light underneath the unexposed

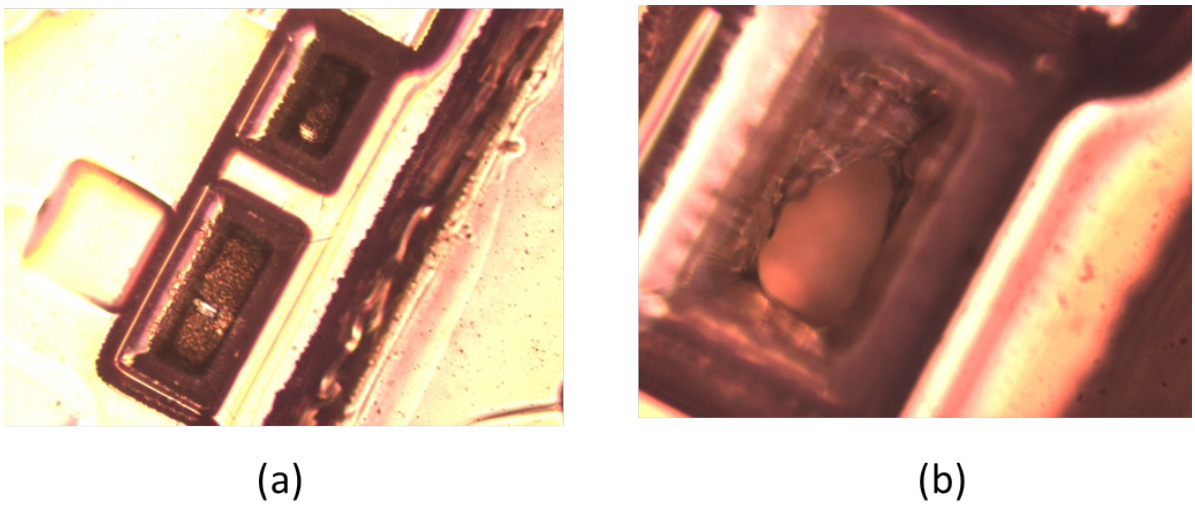

Figure 2.23: (a) KMPR bridging can be seen in the upper opening over the bond pad, the lower bond pad has no bridging. (b) A closer look at KMPR bridging.

portions of the mask. This causes partial development of the KMPR, referred to as bridging. In Figure 2.23a the lower bond pad has no bridging, but the smaller, upper bond pad does show bridged KMPR. Figure 2.23b is a zoomed in picture of this bridging. In order to avoid this problem, the minimum exposure energy is used to develop the the KMPR, no more than $1000 mJ/cm^2$.

Once the KMPR is patterned and the Si substrate has undergone an O_2 plasma clean, the chip is electroplated with copper pins. Previously, gold pins were plated on the surface of the chip. Gold is a good exterior surface because of its corrosion resistance, but as mentioned in the introduction of this chapter, gallium readily diffuses into many metals, including gold. This could compromise the reliability of a liquid metal assembly because the gallium will embrittle the gold pins. Additionally, with the rising cost of gold, electroplating high profile layers of gold on the surface of chips is not an economical approach. Therefore copper pins are plated instead. A copper sulfate electroplating bath was prepared in house. Appendix A contains the electroplating bath preparation and electroplating steps.

Copper pins are electroplated onto the surface of the chip, and once the KMPR and AZ9260 are removed from the MMIC's surface, an ENEPIG surface treatment is used to deposit a series of metals that will protect the pin's surface and the overall physical integrity of the copper pin. ENEPIG is a thin film deposition of electroless nickel, electroless palladium, and then immersion gold. It is used to prepare circuits for both solder joints and wire bonding, and is cheaper than many alternative under bump metalization processes [69]. Nickel is a good barrier layer, keeping the tin component of solder from diffusing away from a solder pad. In this application it keeps gallium from diffusing into the copper. The palladium helps keep the pin copper from diffusing into the surface gold. Therefore plating copper and then treating the copper surfarce with this ENEPIG process is more economical and more reliable alternative to plating gold pins on the MMIC's bond pads.

The chip is then aligned and attached to the Si substrate using the Finetech Lambda bonder, as with the pins-on-Si substrate assembly.

2.3.3 Results

Unfortunately, this process was unsuccessful at yielding consistent results, mainly because the positive photoresist, AZ9260, does not undergo cross linking during lithography. When the KMPR is deposited on its surface, the AZ9260 reacts to the solvents in the KMPR causing the AZ9260 to wrinkle and thus ruining the continuity of the Ti/Au seed layer on its surface.

Compared to using AZ9260 for the continuity layer, a negative photoresist would not have this problem. However, negative photoresists inherently have an undercut profile, and this undercut profile would keep the Ti/Au seed layer from being continuous. A sputter deposition system has the capability of depositing continuous metal seed layers onto surfaces with these discontinuity steps, however access to sputtering systems was limited during these experiments and therefore this demonstration was not completed.

2.4 Conclusions

In conclusion, the pins-on-silicon demonstration using liquid metal interconnections between an active integrated circuit and a carrier substrate further demonstrates the feasibility of liquid metal interconnects for MMIC applications. Utilizing a silicon handle wafer allowed individual MMIC chips to be further processed with thick polymer sockets for the liquid metal. Room temperature assembly onto a Si carrier substrate could then be achieved using a manual flip chip bonder. Although this demonstrator assembly had a high transition loss of 1.8dB, there are several design factors of this assembly which degraded the MMIC's overall performance. These performance degradations are embedded in the transition loss value.

As discussed in Section 2.2.3, the transition loss of prototype, passive structures assembled with liquid metal interconnections (shown in Figure 2.1b), was considerably less than the transition loss of the active assembly, shown in Figure 2.17. It was concluded that the relatively higher loss of these first active assemblies was due to the fact that the MMIC used in these demonstrations was not designed for flip chip assembly. The specific MMIC's backside ground was designed to be directly connected to the package ground, and the active circuits were affected by the presence of dielectric materials near passive structures, making it difficult to design a high performing flip chip assembly. A MMIC chip specifically designed for flip chip assembly would yield better performance in the liquid metal flip chip configuration; however wire bonding is the accepted standard in high frequency packaging, and flip chip MMICs are that still not common despite the improved interconnect performance of flip chip designs.

Subsequent iterations of the liquid metal flip chip design sought to reduce these effects; improving the Si substrate ground plane and reducing the MMIC's contact with SU-8. Changing the plating process and coating the pins with protective metal layers reduces the cost of processing and will also likely increase the reliability of the the assembly. However, processing difficulties prevented a direct demonstration of the effectiveness of these changes in this dissertation work.

Chapter 3

Heterogeneous Liquid Metal Flip Chip Connection onto PolyStrata^{TM}

Chapter 2 highlighted the challenges of integrating a MMIC in a flip chip configuration onto a carrier when the MMIC is designed for wire bond interconnects. PolyStrata^{TM} technology is a 3D micromachining technology that offers the flexibility to design individual chip sockets to receive single MMICs or integrate whole hybrid module sub-systems. Design and fabrication of a PolyStrata based, three dimensional, flip chip carrier substrates can better compensate for MMIC wire bond design dependencies. The following sections introduce PolyStrata technology, discuss a Polystrata based, liquid metal flip chip assembly design, and present measured results of a completed assembly.

3.1 Introduction to PolyStrata

PolyStrata is a sequential surface micromachining fabrication technique that is capable of building very small and accurate three dimensional copper structures. This process is patented and exclusively held by Nuvotronics, LLC. The versatility of this technology allows

designers to create unique passive structure designs for microwave and mm-wave applications. The cornerstone of PolyStrata's functionality and superior performance is its capability to fabricate micro-rectangular coaxial transmission lines, referred to as recta-coax, with an air dielectric. Dielectric losses are a major loss mechanism in standard coaxial line, particularly at mm-waves, so air dielectric coax is an ideal form of coaxial line.

The cross section of PolyStrata recta-coax is much smaller compared to standard that of high frequency coaxial cables, allowing them to be utilized at even higher frequencies. The smallest cable standard currently available is for 1mm cables; the circular coax line outer conductor diameter is 1mm. These cables operate at frequencies as high as 110 GHz. The largest outer conductor dimension of typical PolyStrata, recta-coax designs is $300\mu m$, enabling PolyStrata design at frequencies well above W-band. Additionally, because of the PolyStrata design flexibility, this technology can be integrated with many other standard microwave and mm-wave technologies, including MMICs, discrete passives, and MEMS devices.

A brief discussion of PolyStrata fabrication and a summary of the technology's performance follow.

3.1.1 PolyStrata Fabrication

PolyStrata fabrication is a wafer level process that consists of a sequence of lithography and plating steps [70]. Figure 3.1 shows these basic steps for the fabrication of recta-coax. Layers of thick photoresist are sequentially deposited and patterned; the photoresist remains through plating steps and is subsequently released all at once. The specific photoresist used was originally designed by Rohm and Haas; Nuvotronics now owns the patent for its formula.

The thick photoresist is deposited and patterned on a wafer (Figure 3.1a) and copper is plated in the openings of the photoresist (Figure 3.1b). The surface of the wafer is then planarized and the lithography, plating, and planarizing steps are repeated (Figure 3.1c and

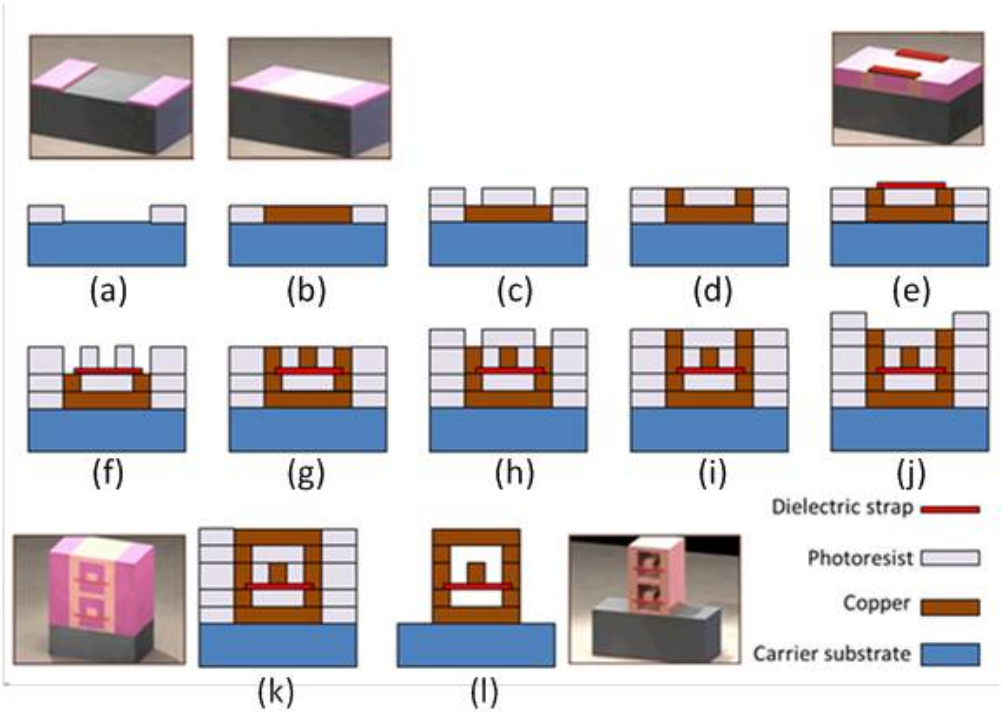

Figure 3.1: Cross sections of process steps to create PolyStrata^{TM} rectangular coaxial transmission lines [70]. ©by IEEE. All rights and reserved.

Figure 3.1d). Each copper plating step is referred to as a "strata". Permanent dielectric straps are added to suspend the center conductors of the recta-coax (Figure 3.1e). Copper is plated above and below the permanent dielectric strap layer to lock the dielectric into place.

Once all strata have been deposited on the surface of the wafer (Figures 3.1f through 3.1k), the photoresist is removed (Figure 3.1l), releasing signal lines which are now isolated from ground shielding by an air dielectric. The permanent dielectric straps occupy approximately 0.2% of the volume between the signal line and the ground shielding, introducing minimal dielectric losses [71].

Copper PolyStrata structures are built on alumina or silicon wafers of 150 mm diameter, therefore each build yields more than 150 cm^2 of design area for fabrication. Completed PolyStrata designs can remain on the substrate as rigid stand alone systems, or can be detached from the substrate to be integrated into larger architectures. The thickness of each

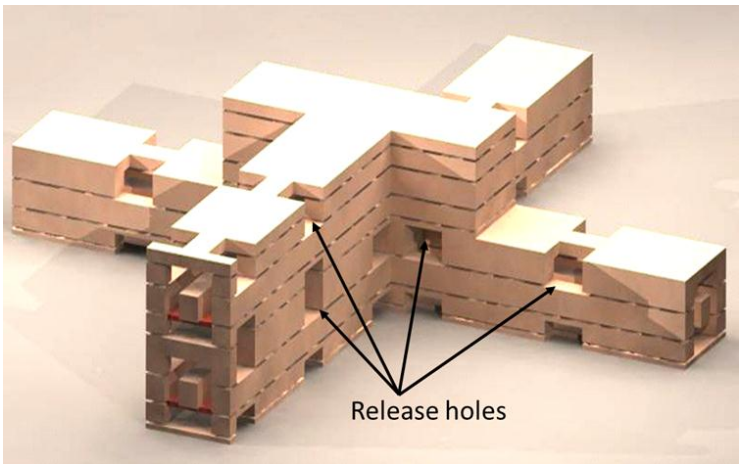

Figure 3.2: Rendered image of recta-coax transmission lines stacked on top of one another.

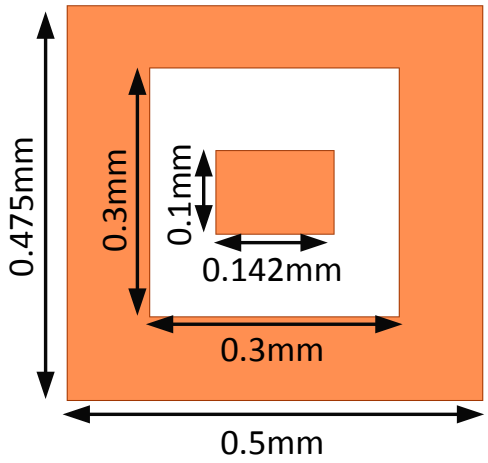

Figure 3.3: Cross section of 50 PolyStrata recta coax showing its dimensions.

strata can vary anywhere from $10\mu m$ to $100\mu m$, with photoresist aspect ratios of as much as 1:1. The lithography steps are high precision, with horizontal and vertical tolerances of each strata on the order of $1\mu m$ or less. This enables designers of microwave and mm-wave devices to design structures in CAD based, electro-magnetic software that very closely match the fabricated structures [72].

Figure 3.2 is a rendering of recta-coax lines that demonstrates some of the basic characteristics of a PolyStrata build and Figure 3.3 show the dimensions of a typical 50Ω cross section of PolyStrata. Standard PolyStrata recta-coax is built in 6 strata layers, and up to

15 strata layers can be processed, allowing for two levels of recta-coax lines to be built on top of one another. Intermediate ground shielding keeps these lines isolated from one another. Low loss, 90° bends are easily realized in PolyStrata fabrication. Release holes are indicated in Figure 3.2 which allow the photoresist within recta-coax to be removed during the release process.

The ability for recta-coax transmission lines to be routed close to one another and over top of one another in 3D adds to the versatility of microwave and mm-wave structures designed in PolyStrata. PolyStrata builds can be stacked on top on one another, utilizing flip chip style interconnections, for more complex signal routing.

3.1.2 PolyStrata Performance

Advantages and disadvantages of standard transmission lines were reviewed in Section 1.2.1. High performance circular coaxial transmission lines are limited by their high cost and relatively large size. A single, high frequency cable that functions in the mm-wave frequency range (30 GHz and higher) can cost thousands of dollars. Micromachining processes for the fabrication of coaxial transmission lines can scale down the size of these coaxial transmission lines and may facilitate cost effective integration of discrete microwave elements or whole microwave module systems.

Planar transmission lines, such as microstrip and CPW, are the typical choices of module designers for signal routing. Compared to these technologies, recta-coax offers a groundbreaking combination of low loss and high isolation, as shown in Figure 3.4. 3D routing and high isolation allows for compact, high performance signal routing, reducing this overall footprint of microwave elements.

In addition to these significant advantages, many other three dimensional passive microwave and mm-wave structures can be realized in PolyStrata. The precision and versatility of PolyStrata fabrication enables an increase in performace and reduction in size and weight

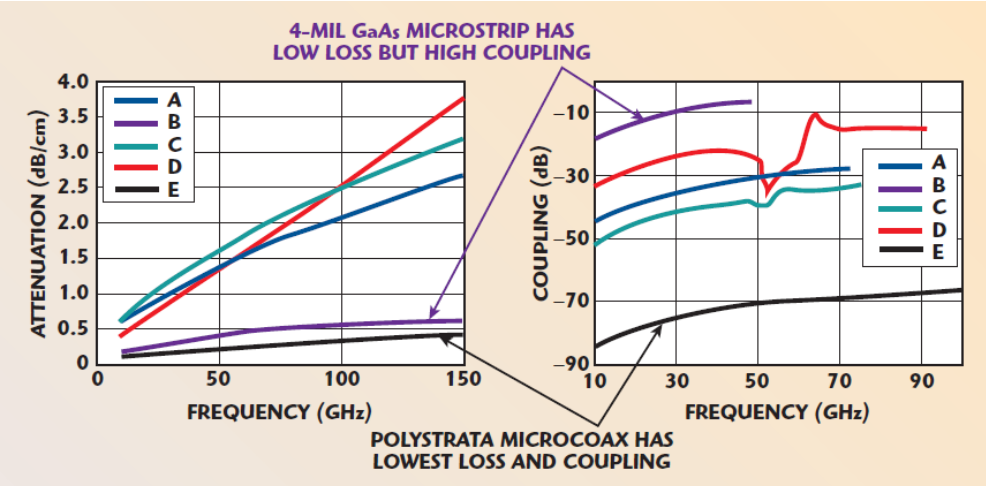

Figure 3.4: Graphs comparing the attenuation and coupling of typical planar signal routing technologies to PolyStrata. (A) microstrip on 50μm GaAs, (B) microstrip on 200μm GaAs, (C) CPW on 125μm GaAs, (D) CPW on 200μm alumina, and (E) PolyStrata 250μm recta-coax lines [70].

of many high frequency components such as antennas, dividers/combiners, filters, baluns, and resonators [73, 74, 75]. Integration of PolyStrata structures into larger microwave systems has been demonstrated with wirebond interconnections, flip chip interconnections and waveguide transitions (Figure 3.5) [76, 77].

These beneficial properties of PolyStrata make it an ideal technology to demonstrate liquid metal interconnections. The 3 dimensional fabrication process is well suited to receive MMICs in a flip chip configuration, with pin structures fabricated on the PolyStrata frame.

3.2 Polystrata Frame and GaAs MMIC

Before discussing the liquid metal, flip chip assembly onto a PolyStrata frame, the frame and MMIC chip design used in the assembly are introduced in this section.

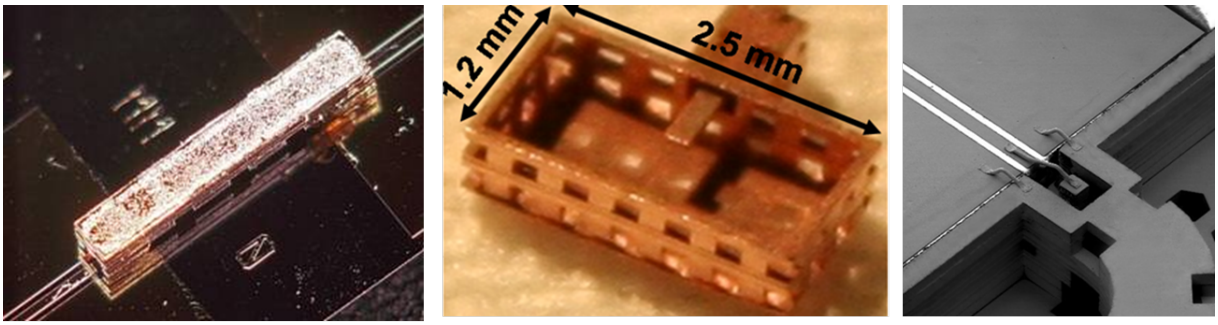

Figure 3.5: Examples of PolyStrata's integration capabillities; (a) flip chip configuration onto CPW, (b) PolyStrata waveguide transition, and (c) wire bonding to CPW.

3.2.1 PolyStrata Frame

Figure 3.6 shows two exploded views of the PolyStrata assembly. The frame has pins, corresponding to RF and DC pads on the MMIC chip, having the dimensions of $75\mu m \times 75\mu m \times 75\mu m$. The RF probe pads are designed to be measured with $250\mu m$ pitch GSG probes, and the DC probe pads have a pitch of $150\mu m$. The recta coax transmission lines have a characteristic impedance of 50Ω; a cross section of this recta coax is shown in Figure 3.3.

The PolyStrata frame supports the MMIC around the vertical transitions and the outer edge of the chip. The remaining portion of the frame is open, so that the chip surface faces primarily air. The MMIC's SU-8 sockets fit over these PolyStrata frame pins, with the liquid metal intended to create electrical continuity between the two structures. The MMIC is supported by a copper backplane, also fabricated in the PolyStrata process. This backplane serves primarily to connect the backside ground of the MMIC chip with a conductive ground layer the PolyStrata frame sits on. The use of this backplane is an artifact of the MMIC not being designed for a flip chip configuration. It also helps create a path for heat to be removed from the chip and makes the MMIC chip easier to handle during assembly.

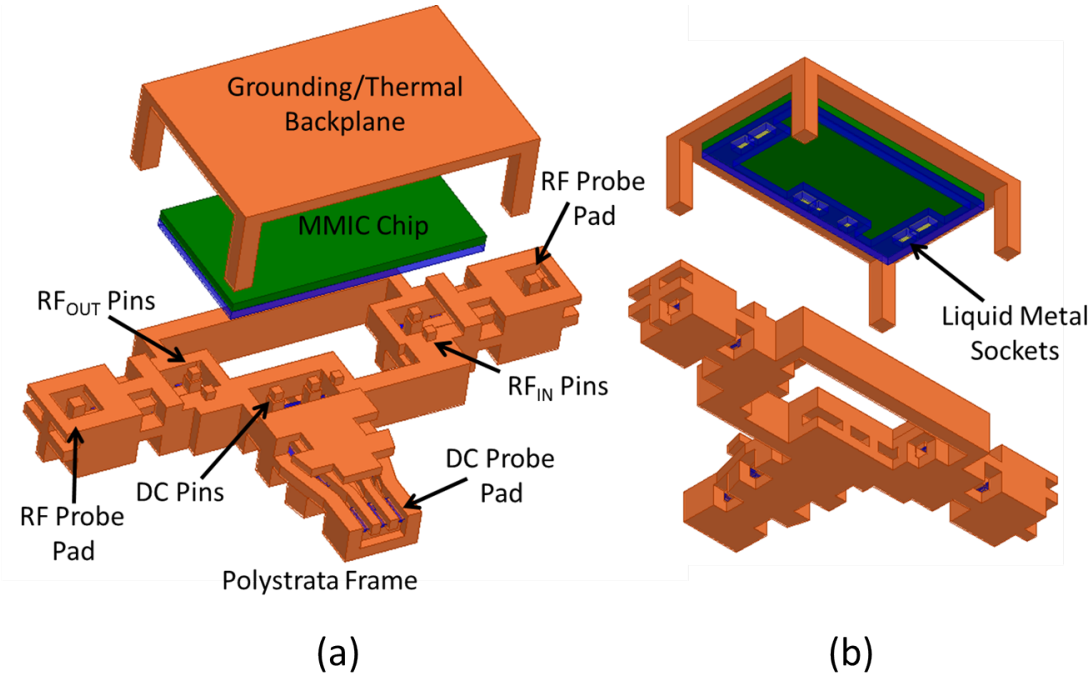

Figure 3.6: CAD rendering of the PolyStrata liquid metal, flip chip assembly: (a) an exploded view of all major parts; (b) an angled view showing the MMIC with its border of SU-8, creating the socket feature at the MMICs bond pads.

3.2.2 GaAs MMIC

The GaAs MMIC used in this PolyStrata assembly demonstration is very similar to the MMIC described in Section 2.1.2, with some differences which are explained in the following subsection.

The MMIC chip used, MA/COM part number 1629, is a two stage driver amplifier (Figure 3.7). It has many of the same characteristics as the MAAM-007523 that was used in the Chapter 2 assemblies. This chip is the same size as the MAAM-007523 chip; the bond pads are located in the same positions on the chip, the operating frequency is the same, and the input and output impedance is still matched on-chip to a 50Ω system. The primary difference is that the MAAM-007523 chip is a three stage amplifier chip, with an average small signal gain of 23 dB, and the gain of chip 1629 is only about 18 dB. With an applied

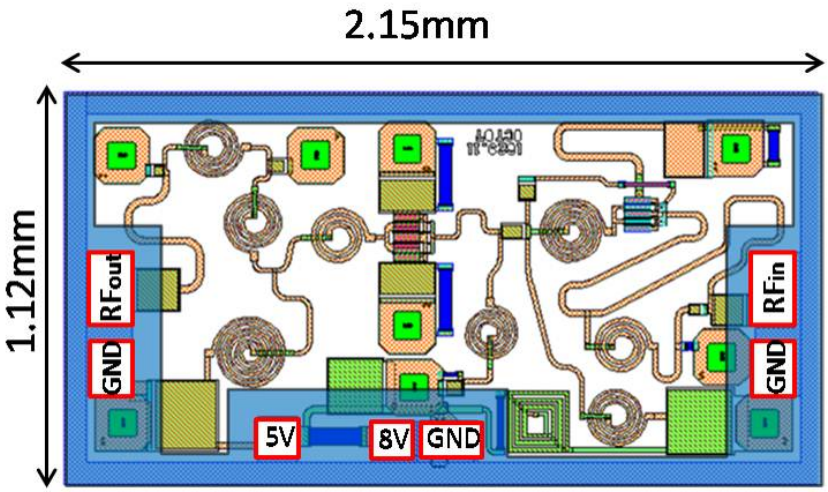

Figure 3.7: CAD drawing of MA/COM amplifier chip used in this demonstration. The blue shading on the surface of the chip outlines the area of SU-8 coverage.

V_{DD} of 5V, the chip is expected to draw 62 mA.

3.3 PolyStrata Frame and Jumper Assembly

A passive "jumper" piece was also designed and built in PolyStrata to enable characterization of the transition performance of liquid metal, flip chip assembly on PolyStrata (Figure 3.8). The jumper is a section of PolyStrata recta coax transmission line that is the same length as the MMIC chip. The jumper has SU-8 sockets at it's vertical transition points which connect the RF input and output pins on the frame via liquid metal interconnects. Fabrication of this connection and a comparison of modeled data verses measured results are provided below.

3.3.1 Fabrication of PolyStrata Jumper Assembly

The frame and jumper are both fabricated in the same PolyStrata run at the Nuvotronics facility in Radford, VA. The frame and jumper designs are grouped together on a wafer layout

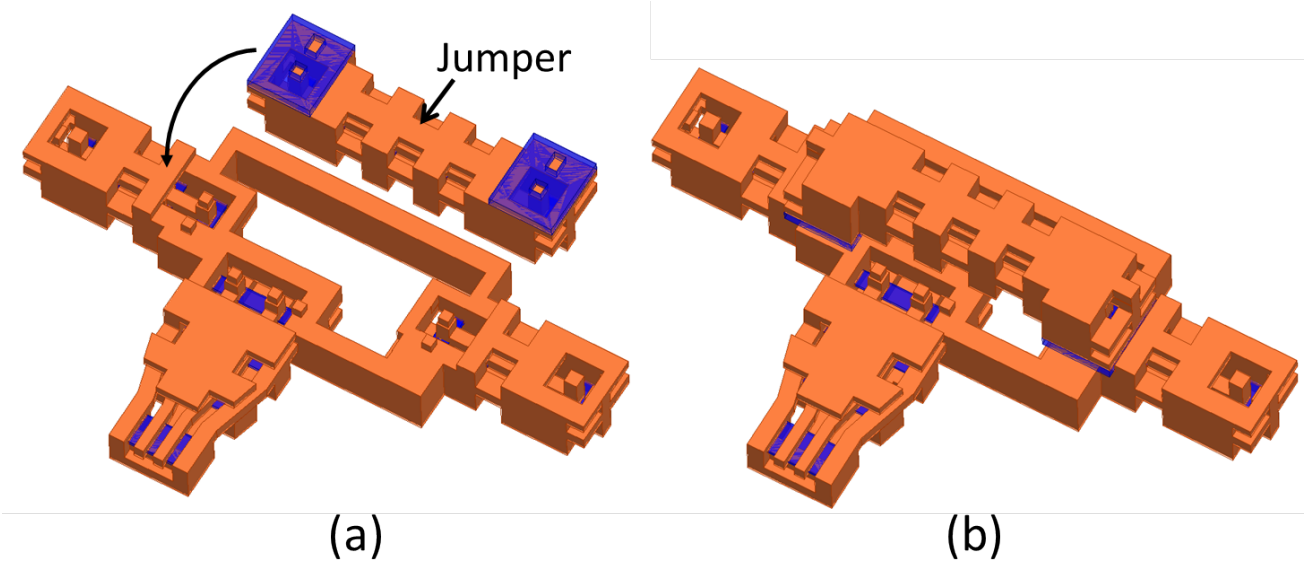

Figure 3.8: The passive, "through" liquid metal, flip chip jumper assembly, (a) showing both the PolyStrata frame and the PolyStrata jumper face up (b) a view of the final assembly.

Figure 3.9: Photograph of PolyStrata reticle containing the PolyStrata frames and jumpers.

in reticles, and once the fabrication of the wafer is completed these reticles are separated by dicing of the wafer. Figure 3.9 is a Photograph of one of the frame and jumper reticles.

The SU-8 sockets on the recta-coax jumper piece shown in Figure 3.8a must be added to the surface of the jumper after wafer scale fabrication is completed. The top surface of these socket and jumper pieces reside on the top surface of the PolyStrata reticle. Originally, the SU-8 socket features were planned to be fabricated on the surface of jumpers before the jumpers were released from the photoresist. Then the reticles would be stripped of their photoresist and the SU-8 sockets would remain on the surface of the jumpers. It had been previously determined that SU-8 is not mechanically or chemically affected by the solvents used to strip PolyStrata photoresist. However, the adhesion of the SU-8 to the surface of the PolyStrata jumpers was not sufficient for the SU-8 to remain on the surface of the jumpers during resist removal.

Alternatively, the SU-8 sockets were glued to the surface of the jumper parts post-release. To make stand-alone SU-8 features, a thin film layer of gold is deposited on the surface of a silicon wafer and the SU-8 features are developed on top of the gold layer. The entire wafer is then immersed in Rohm and Haas's Super Stripper gold etch solution, a cyanide based etch solution that does not adversely effect the polymers like SU-8, and the wafer is left in the solution for at least eight hours. The gold is subsequently etched from the surface of the wafer, under-etching the SU-8 sockets and releasing them from the surface of the wafer. Figure 3.10a shows some of these released SU-8 parts. The parts can be handled with relative ease, and are glued to the surface of the jumpers with non-conductive epoxy (Figure 3.10b). Even relatively large SU-8 features can be released and manipulated, such as SU-8 sockets glued to the surface of a PolyStrata frame (Figure 3.10c).

Frozen liquid metal is then placed in the sockets in the same manner described in Chapter 2, and the PolyStrata frame and jumper are aligned and connected using the Finetech Lambda flip chip bonder. Figure 3.11 is an image of the completed passive, through "jumper" assembly.

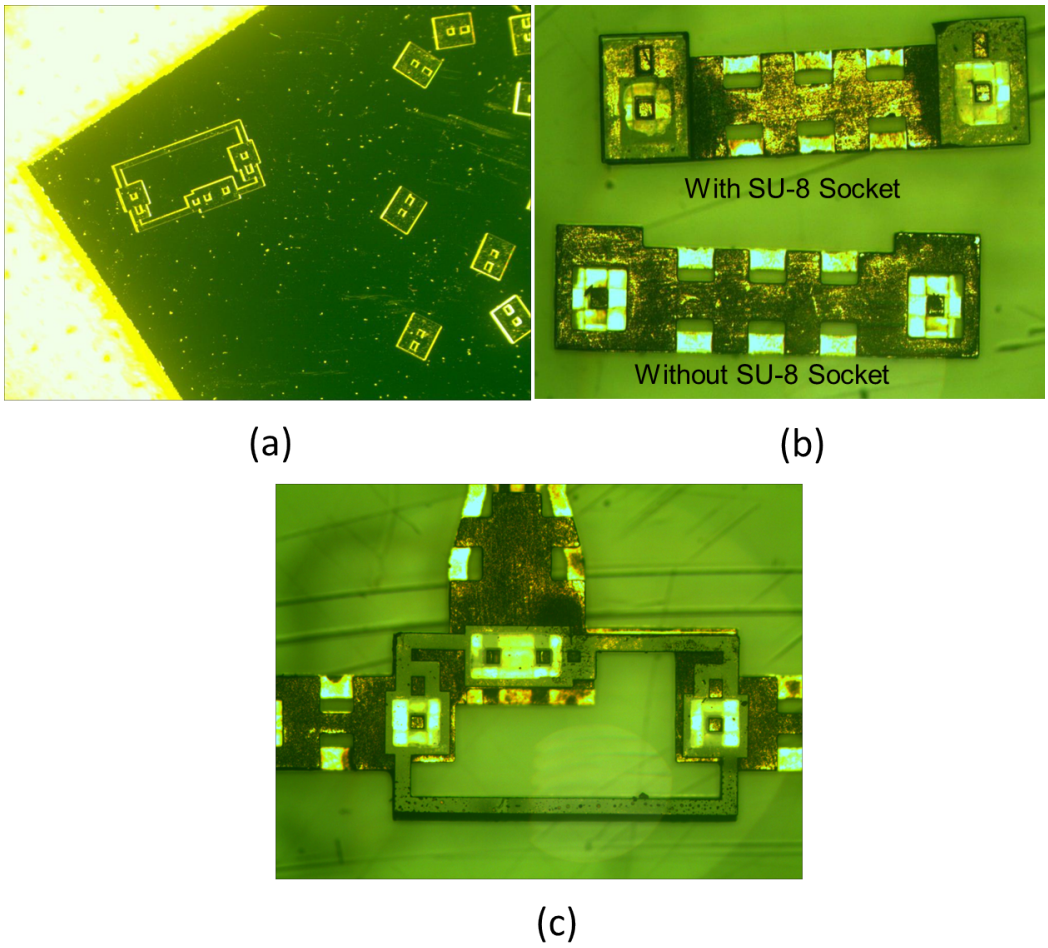

Figure 3.10: Micrographs of SU-8 sockets (a) after being released from the surface of a silicon wafer, (b) glued to the surface of a jumper, and (c) glued to the surface of a PolyStrata frame.

3.3.2 Jumper Assembly Simulation and Measurements

The performance of the passive liquid metal, flip chip jumper assembly was simulated in Ansoft HFSS, a CAD based software that can preform full wave electromagnetic field analysis of 3 dimensional structures. The measured results were made with Picoprobe model 40A, GSG, 250μm pitch probes. An SOLT calibration was used to calibrate the measurement setup to the probe tips. These simulated results (red) are compared with the measured results (blue) of the passive assembly in Figure 3.12. In a lossy, passive network the insertion

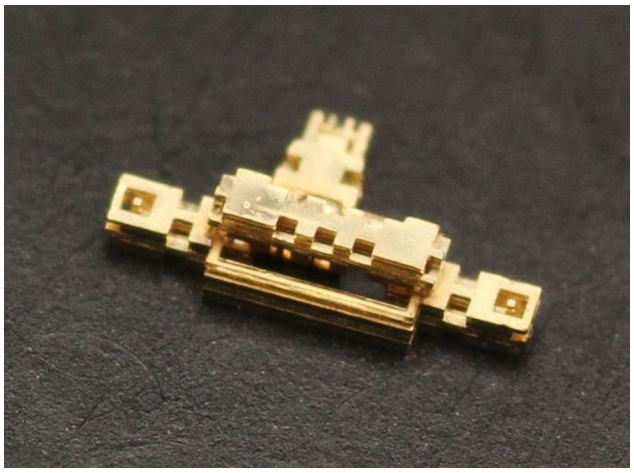

Figure 3.11: Complete PolyStrata through "jumper" assembly.

loss (the relative amount of power dissipated within the network) can be calculated by deembedding the magnitude of reflected power from the magnitude of transmitted power. Using s-parameters, the transition losses of this passive assembly is found using the equation,

$$2 \times transitionloss = -10log\left(\frac{\mid S_{21} \mid^2}{1- \mid S_{11} \mid^2}\right), \tag{3.1}$$

and is presented in Figure 3.13.

An limited set of thermal cycling data was taken after acquiring the initial set of RF measurements. The PolyStrata through assembly was placed in a thermal cycler and the temperature was cycled 40 times from -40°C to 125°C. S-parameter data was then taken again after the thermal cycling, and the results are shown in Figure 3.14.

Discussion

Referring to S11 and S21 data shown in Figure 3.12, the simulated and measured responses of the "jumper" assembly match reasonably well over the 40GHZ range. At lower frequencies the jumper assembly's match is better than expected. On the other hand, the liquid metal interconnection experiences higher loss than expected at higher frequencies. The model of

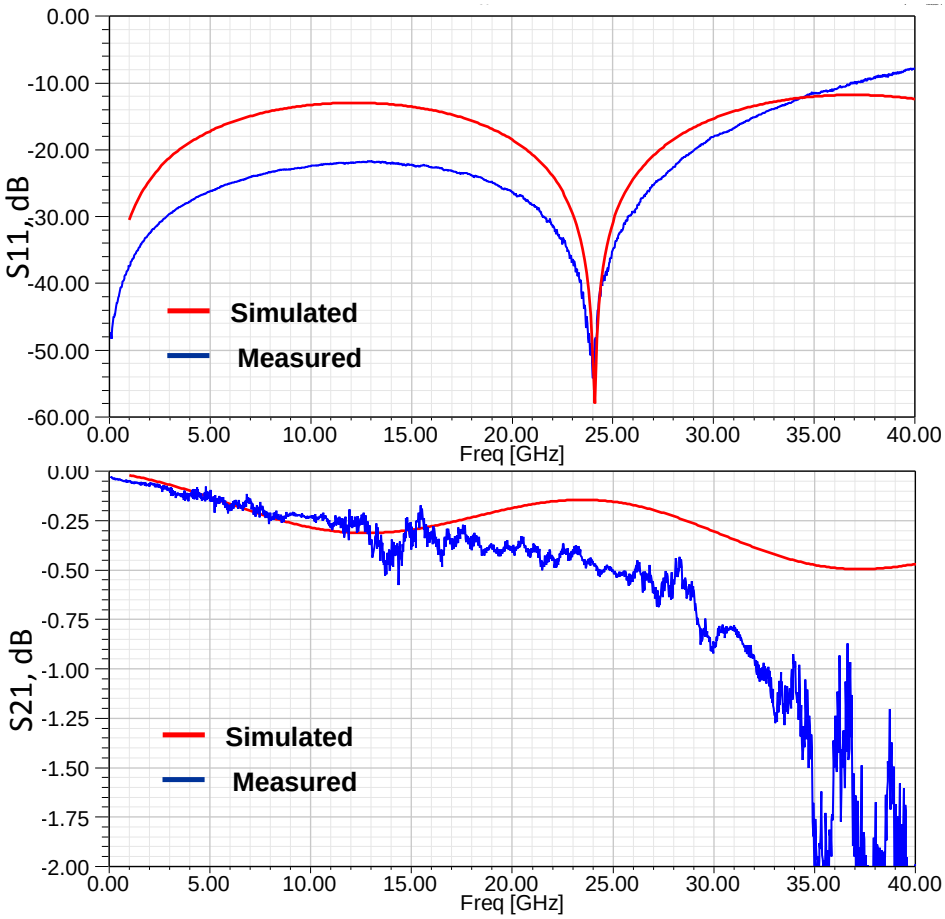

Figure 3.12: Comparison of the PolyStrata through assembly simulated (red) and measured (blue) s-parameters.

the liquid metal interface is very likely an incomplete model of pin/liquid metal interface. Insufficient wetting of the liquid metal to the pin or nonuniform pin/liquid metal contact likely effect the response of this passive assembly and are currently not taken into account in the simulated model.

The average loss per transition is found to be 0.19dB. The losses at frequencies exceeding 30GHz are sharply higher; the average loss over the 1629 MMIC's frequency band of operation (4.9 - 8.5 GHz) is only 0.08dB per transition. This is a conservative loss measurement,

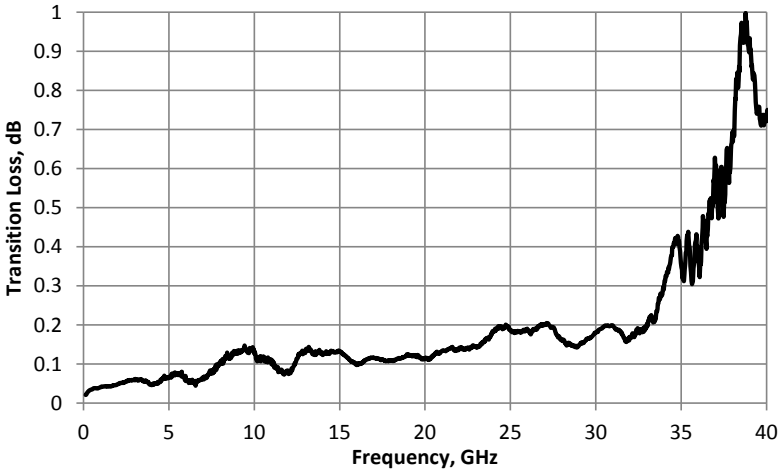

Figure 3.13: Loss per transition of the PolyStrata through "jumper" assembly.

because this loss value includes losses incurred in the PolyStrata frame and jumper recta-coax.

A factor that likely accounts for higher loss in the PolyStrata "jumper" assembly, particularly at frequencies exceeding 30GHz, is that the SOLT calibration used to de-embed the probe tips is not an ideal calibration for PolyStrata structures. The planar "short", "load", and "thru" structures on a SOLT calibration substrate are very different from the surface of the PolyStrata probe points, which results in calibration errors at the probe/PolyStrata transition. Incorporating TRL structures for future PolyStrata designs will eliminate error contribution and allow deembing of any losses in the PolyStrata frame recta coax lines.

The thermal cycling data in Figure 3.14 shows that the resonant frequency of the assembly shifted up by about 2GHz after 40 thermal cycles. The resonant frequency of a circuit is the frequency where the capacitive and inductive components of the circuit cancel each other out, and is given by:

$$f = \frac{1}{2\pi\sqrt{LC}}. \tag{3.2}$$

Therefore reduction in the liquid metal interconnection's inductance or capacitance would

cause a shift up in the resonance of the circuit. Based on this, two possible scenarios are suggested to be occurring either independently or in parallel with each other.

The first is that the dielectric properties of SU-8 may change slightly during temperature cycling. It has been found cross linking of SU-8 affects the value of its dielectric constant [78, 79]. Exposing SU-8 to elevated temperatures exceeding 100°C further cross links the polymer and reduces its dielectric constant. Cited values of dielectric constant vary from 4.1 to 2.85; however a dielectric constant value of 4.1 was presumed for simulations. The SU-8 sockets were not hard baked before they were glued to the jumper transmission lines,

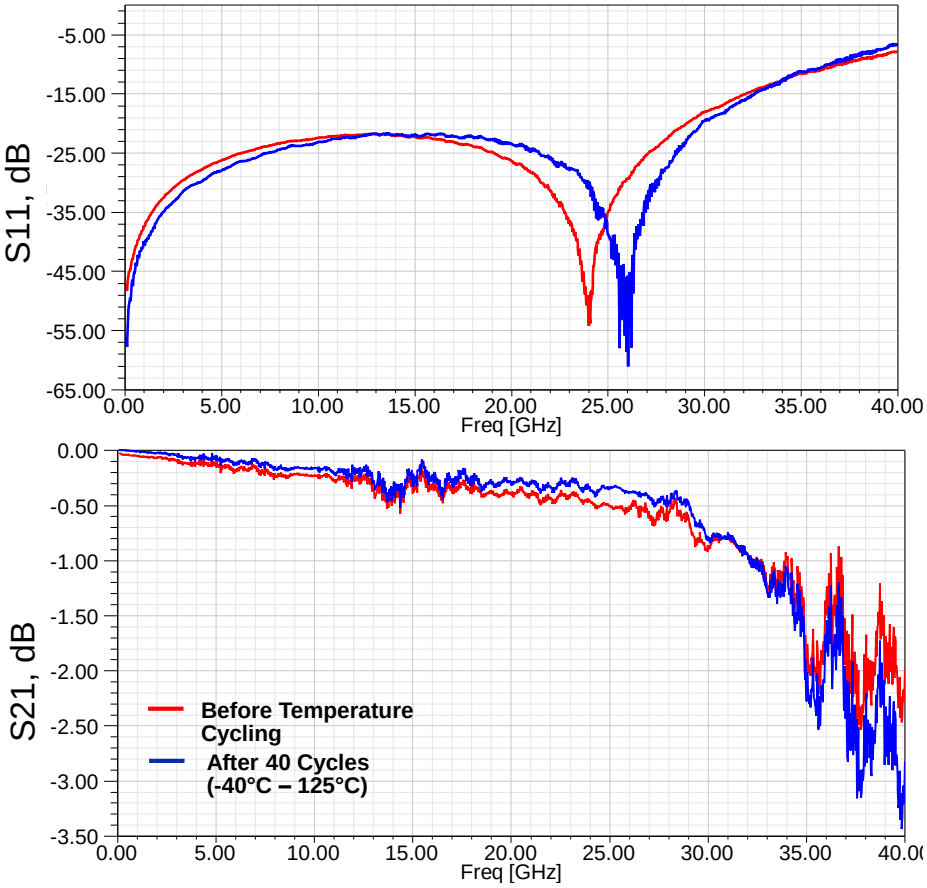

Figure 3.14: Measured response of PolyStrata through "jumper" assembly before (red) and after (blue) thermal cycling.

therefore the SU-8 could have continued to cross link during the temperature cycling. The cross linking caused the dielectric constant of the SU-8 to decrease, reducing the capacitance of the interconnect, and shifting the resonance of the assembly up.

Another explanation for the shift in resonance is the temperature cycling caused the surface of the interconnect's pin to better wet with the liquid metal. This would reduce the resistance of the interconnect, which could explain a slight reduction in the insertion loss shown in Figure 3.14. Improved electrical path would also decrease the inductance of the interconnection, shifting the resonance up.

It is believed that the electrical performance of the assembly would reach a steady state after being exposed to a sufficient number of temperature cycles. Further testing will be performed in the future to confirm this and to understand at what point the liquid metal interconnect's electrical properties reach a steady state.

Overall, this through assembly testing suggests that the PolyStrata frame with liquid metal, flip chip interconnections should perform very well for an active, MMIC chip assembly.

3.4 Polystrata Frame and MMIC Assembly

The following section describes the steps taken to assemble an active MMIC onto the PolyStrata frame and presents the measured data collected from the prototype structure.

3.4.1 Fabrication of MMIC to PolyStrata Frame

The steps used to assemble the MMIC interconnect configuration are shown in Figure 3.15:

(a) Place MMIC chip in DRIE-etched Si cavity.

(b) Deposit and pattern SU-8 sockets over MMIC bond pads.

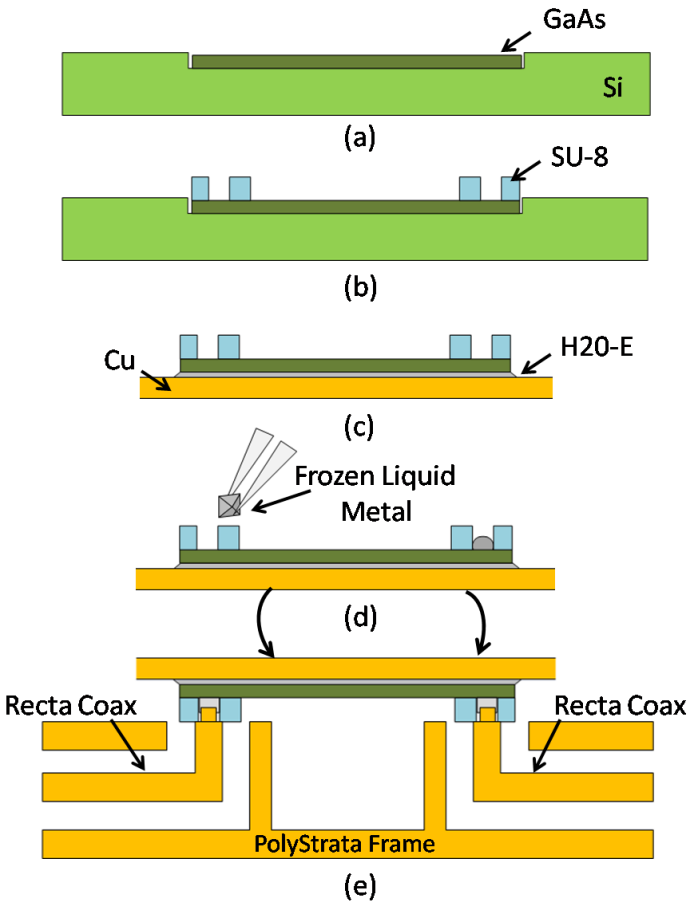

Figure 3.15: Cross section of process steps used to flip chip connect a MMIC to a PolyStrata frame.

(c) Remove chip from Si cavity and bond to copper backplane with H20-E conductive epoxy.

(d) Place frozen liquid metal into SU-8 sockets.

(e) Flip chip connect to PolyStrata frame.

Steps (a) and (b) are described in Section 2.2.2. The SU-8 is deposited on the MMIC chip to a thickness of $100\mu m$. The conductive epoxy that is used to attach the MMIC to the copper backplane, H20-E, is a common conductive epoxy utilized for chip bonding. It has volume electrical resistance of 0.0004Ω-cm, and the thickness of the epoxy layer is

approximately $20\mu m$ [44]. Figure 3.16a shows a picture of the MMIC chip epoxied to the copper backplane.

Before the final connection step is performed, the PolyStrata frame is also bonded to a conductive carrier substrate with H20-E. When the assembly is complete, the legs of the backplane are also mechanically and electrically connected to the conductive substrate with H20-E, giving the backside ground plane on the MMIC a direct path to a common ground. This a is necessary for MMIC chips designed for wire bond connections only; a flip chip IC design would not need this additional grounding. Figure 3.16b is a picture of a complete assembly.

3.4.2 MMIC Assembly Measurements

The completed MMIC assembly was measured with the same measurement setup used to measure the PolyStrata through "jumper" assembly. 8 volts was applied to the DC bias input, drawing a current of 55 mA, which closely matches the designed operating point of the amplifier. A comparison of the measured results with the directly probed measurements are shown in Figure 3.17.

Discussion

The measured S11 data shown in Figure 3.17 from the liquid metal assembly matches the directly probed MMIC measurements very well. The integration with of the PolyStrata assembly has greatly improved the overall liquid metal, flip chip performance. However, the gain of the PolyStrata assembly is still notably less than the gain of the directly probed measurement. The loss of the PolyStrata through measurement was less than 0.1dB per transition over the range of the MMIC chip's operation, the loss of the MMIC assembly is about 0.7dB per transition. Additionally, it appears that the bandwidth of the chip is about 200MHz lower than the directly probed measurement.

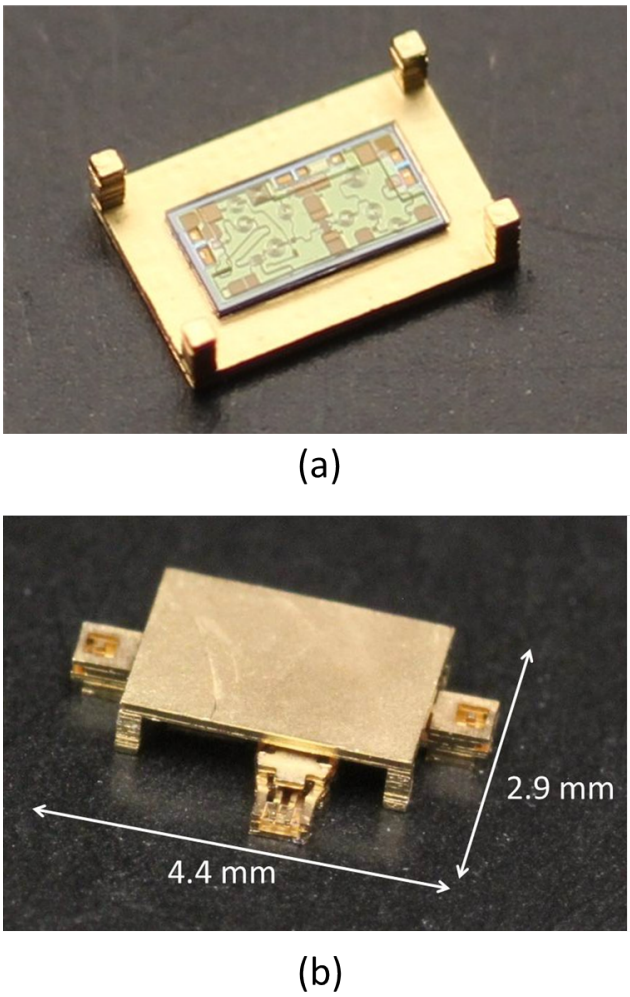

Figure 3.16: (a) MMIC chip on the copper backplane. (b) A completed assembly of a MMIC on the PolyStrata frame.

These issues maybe caused in part by the the effects of SU-8 on some of the passive components on the MMIC. Figure 3.18 shows an image of the MMIC chip with the SU-8's coverage on the chip outlined in blue. Some of the inductors and microstrip lines which maybe affected by the presence of the SU-8 are framed in red boxes. These components are part of the interstage matching networks and transistor biasing networks, and changes in their impedance values could be adversely affecting the performance of the amplifier.

Reducing the coverage of the SU-8 on the surface of the chip and avoiding areas electrically

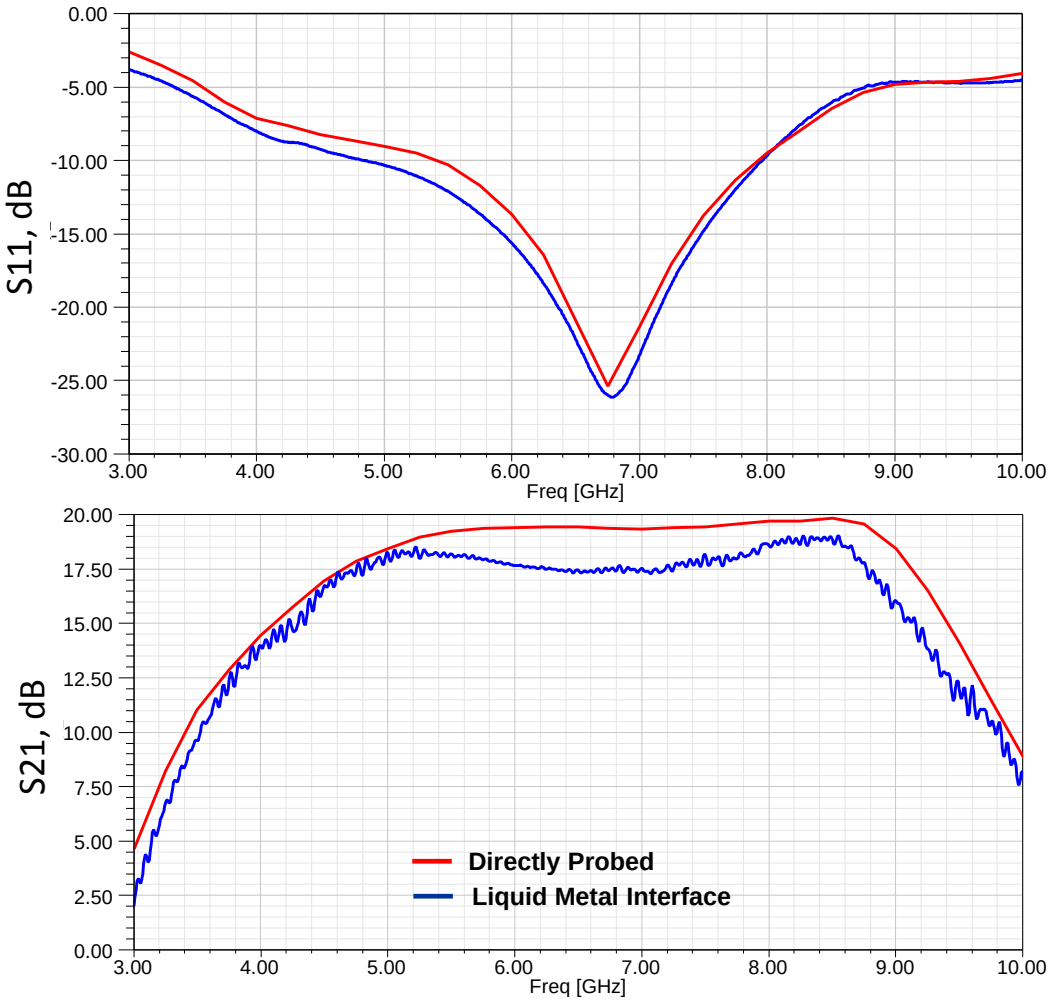

Figure 3.17: A comparison of the directly probed MMIC performance to the performance of a MMIC in a PolyStrata, liquid metal, flip chip assembly.

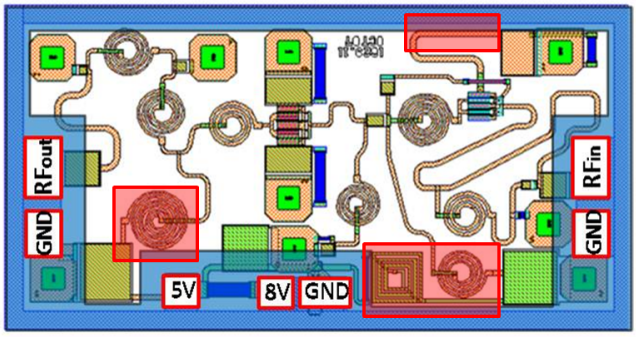

Figure 3.18: Image of MMIC chip with SU-8 coverage outlined in blue and some of the affected passive components outlined in red.

close to microstrip and inductors would help this problem. Hard baking the SU-8 to better cross link the polymer and reduce its dielectric constant would reduce some of SU-8's effects on the chip's performance. Also, designing the MMICs for this liquid metal interconnect approach at the outset, and compensating for these dielectric effects would improve the performance of the overall assembly.

3.5 Summary

Despite the greater than expected loss of this PolyStrata, flip chip assembly, the performance of the MMIC chip in this assembly was reasonable. The MMIC chip is expected to maintain a gain of 17-18 dB fully assembled in a typical wire bonded configuration [80]. In the PolyStrata demonstration, the gain never drops below 17.5 dB over the chip's frequency band. This not only indicates that a liquid metal, flip chip interconnection can be competitive with standard connection technology but it can even be utilized for chips which are not initially designed for flip chip assembly.

The PolyStrata through assembly was used to verify the efficiency of the flip chip, liquid metal assembly. It also shed some light on properties of a liquid metal assembly that were not captured in initial simulations. Further modeling work and temperature testing will be performed to better understand these properties and make the design of liquid metal interconnections more reliable and predictable.

Chapter 4

Modeling of Liquid Metal, Flip Chip Transitions on PolyStrata

Developing a lumped element model for liquid metal transitions is an important step in characterizing the transition's performance. This modeling not only allows for a quantifiable comparison of liquid metal transitions to traditional forms of level 1 interconnection technology, but is also important for designing and simulating circuits using such interconnects. For example, optimal performance of a power amplifier MMIC can only be achieved with suitable impedance matching at the input and output of the chip.

The following chapter introduces a single-transition test assembly designed for model extraction measurements, presents and analyzes the data taken from the model assembly, and discusses the lumped element model that is extracted from this data.

4.1 PolyStrata Single Transition Assembly

Creating a structure for directly measuring the response of a single liquid metal transition can be realized by utilizing the 3D design flexibility of PolyStata technology. As discussed in

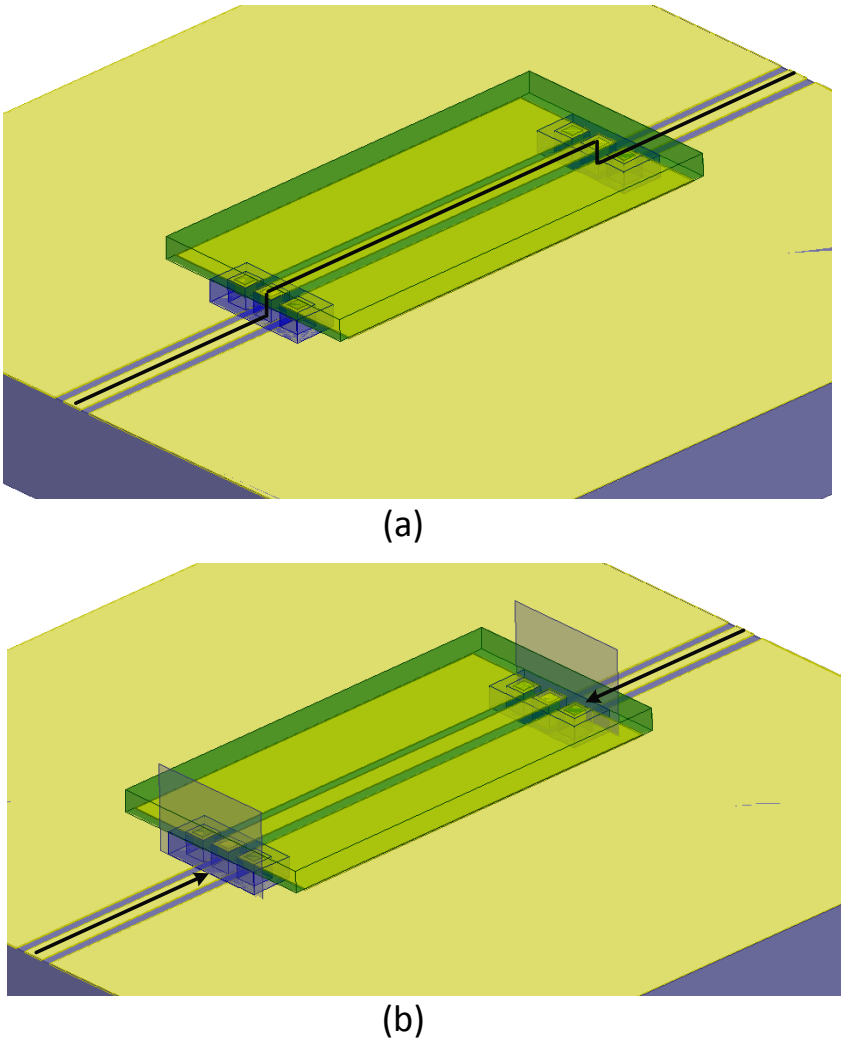

Figure 4.1: Liquid metal, flip chip assembly on planar CPW transmission line (a) showing the signal path (b) the shifted reference plane that can be achieved with a TRL calibration.

Chapter 2, designing passive transmission line structures on planar semiconductor substrate or printed circuit board surfaces (Figure 4.1a) requires an assembly architecture where the measurement signal must transition up to a top chip and then back down to the substrate surface (Figure 4.1b). Thru, Reflect, Line (TRL) calibration structures on the substrate can only deembed the input and output transmission lines to the location of the vertical transitions (Figure 4.1b); however the effects of the top chip transmission line will be included

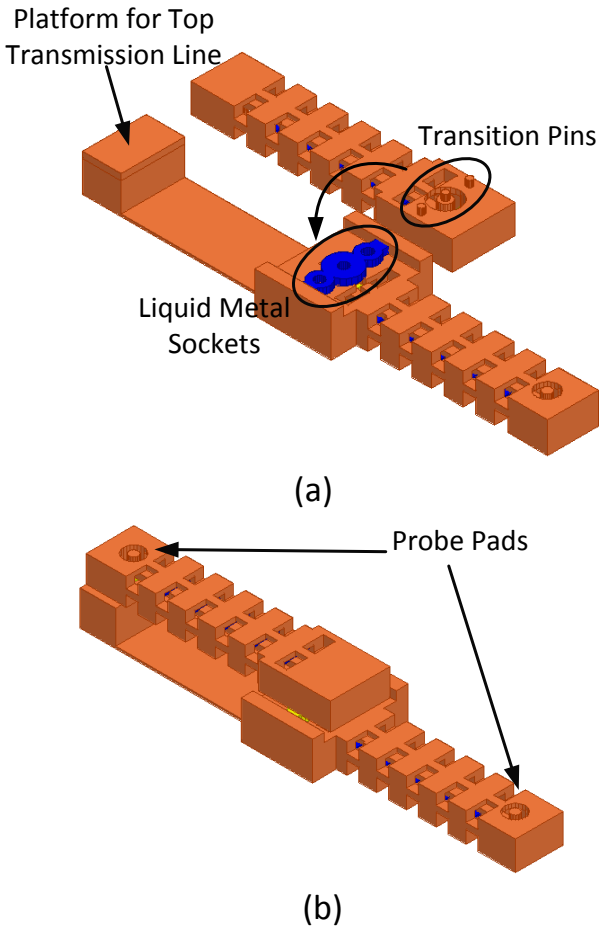

Figure 4.2: 3D renderings of a single PolyStrata liquid metal transition, (a) prior to assembly, showing the PolyStrata pins and (b) after assembly.

in the measurement.

On the other hand, the 3D design capabilities of PolyStrata enable straightforward design of a liquid metal assembly transition which can fully deembed the effects of the RF probe points and transmission lines leading up to the vertical transition. Figure 4.2a shows the two components of a single transition assembly. The base portion of the assembly connects the liquid metal transition socket to RF probe points via a recta coax transmission line and is fabricated so that it remains attached to an alumina carrier substrate. The top portion of the assembly contains the pin feature of the liquid metal transition and is flip chipped onto the base. A "platform" attached to the base mechanically supports the top portion

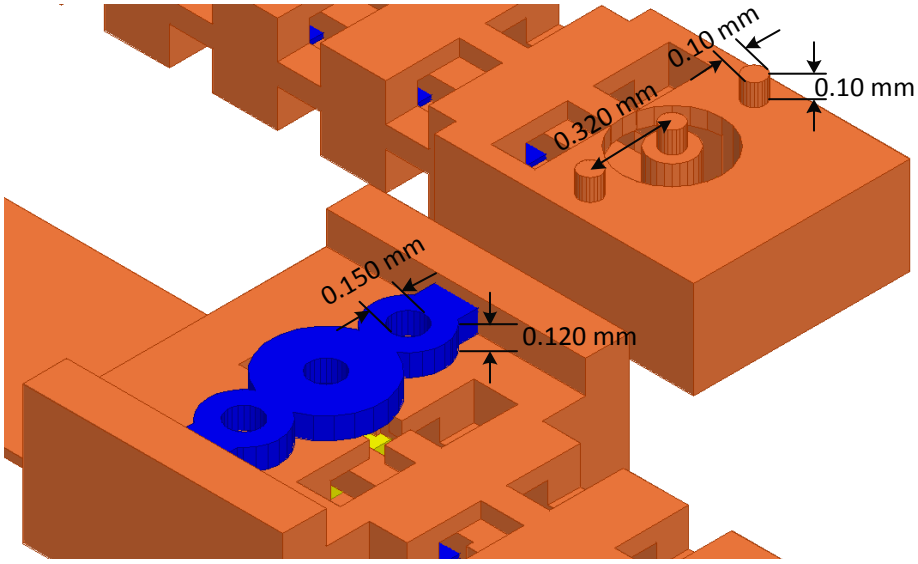

Figure 4.3: The critical dimensions of the PolyStrata liquid metal vertical transition.

of transmission line under the probe pad. The RF probe on the top section of recta coax is opposite to the liquid metal pins (Figure 4.2b), allowing for direct probing of this single transition. Both sections of rectacoax transmission line are 3.3mm in length and are designed to have a characteristic impedance of 50Ω.

The single interconnection assembly was designed and simulated in HFSS and then fabricated in the PolyStrata process. Figure 4.3 is a close up of the two interconnecting PolyStrata parts, displaying the critical dimensions of the liquid metal transition. Both the top and bottom sections of transmission line were coated with ENIPEG passivation before assembly. The SU-8 sockets (blue) are glued to the surface of the PolyStrata structure in the same manner as described in Section 3.3.1. During assembly of this interconnect test structure, liquid metal is placed in sockets of the base structure, and then conductive epoxy is placed on the mechanical support platform. The top section of transmission line is then aligned and mated to the bottom structure using a Finetech Fineplacer lambda bonder. The lambda bonder has temperature cycling capabilities; while the assembly is on the bonder it is heated for five minutes at a temperature of 150°C to cure the conductive epoxy. Figure 4.4 shows an image of a completed assembly on an alumina substrate.

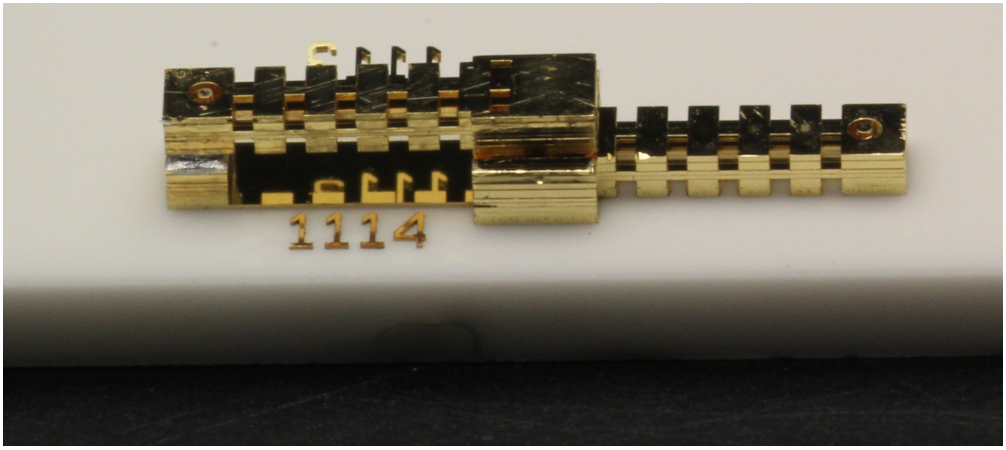

Figure 4.4: A picture of a complete single transition assembly on an alumina substrate.

4.2 Single Transition Measurement and Discussion

Figure 4.5 shows a rendering of the TRL structure used to calibrate the RF cabling, probes, and pads to a rectacoax reference plane prior to measurement of the the single transition assembly. The "thru" transmission line has a total length of 4.9mm and there are three delay line structures that are 1.1mm, 2.5mm, and 5.5mm between the reference planes. The frequencies covered by these lines cover are 25 - 110 GHz, 10 - 50 GHz, and 4 - 23 GHz, respectively. Measurements of this assembly were taken with 250μm pitch GGB Industries Picoprobe, 2.92mm GSG probes. The 2.92mm probes are designed to operate out to a frequency of 40 GHz, therefore calibration data was only taken over a frequency range of 5 - 40 GHz.

Post calibration measured S-parameter data from the single transition assembly is shown in Figure 4.6 (red traces). The single transition assembly was simulated in HFSS before layout and fabrication of the parts. This simulation response is represented with the blue traces. The Figure 4.7 is a lumped element model of the liquid metal transition. This basic circuit is typical for flip chip interconnections [1, 81], with the exception of the series resistor, R, which is added to account for the resistance of Galinstan and its surface oxide.

Table 4.1 gives the values for R, L, and C which are extracted from the single transition

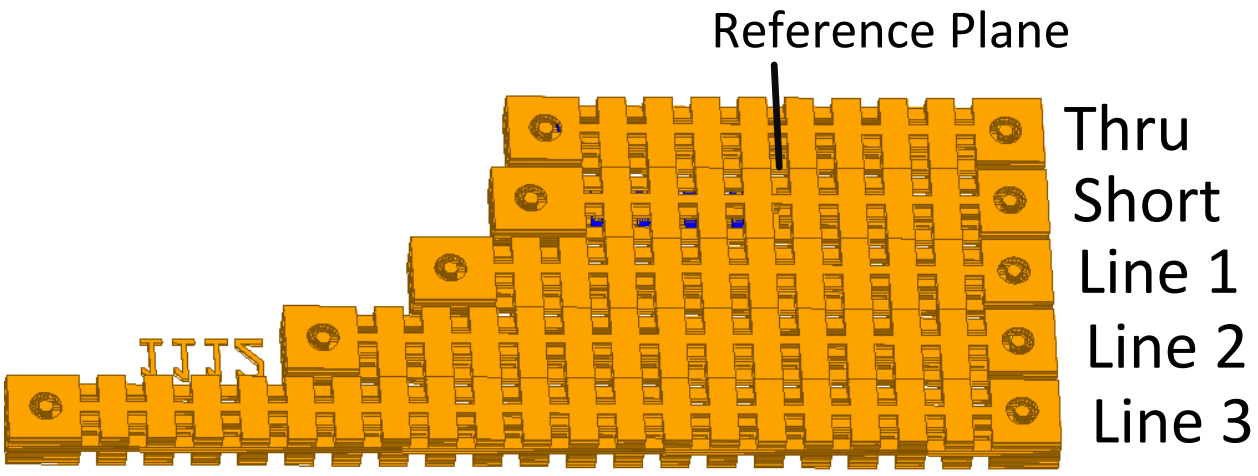

Figure 4.5: Rendering of TRL structure which was used for deembedding the probe points and transmission line features of the single transition assembly.

measurement. Typical values of capacitance and inductance for a flip chip assembly are 10pH and 10fF, respectively[1, 81]. Therefore the values of capacitance and inductance of a liquid metal, flip chip connection are predicted to be higher than that of typical, rigid flip chip assemblies. The simulated response of the lumped element model is represented with the black traces in Figure 4.6.

Higher capacitance is caused by several factors: larger bond pad area of the single transition assembly compared to the bond pad area of typical flip chip assemblies (0.0177 mm^2 compared to 0.01 mm^2 - 0.0025mm^2) and higher dielectric constant of SU-8 ($\epsilon_r = 4.1$) compared to a flip chip assembly with no underfill. The higher bond pad areas are dictated by the design constraints of PolyStrata fabrication; the pin features of the top section of transmission line are fabricated on an 100μm strata layer. The height to lateral dimension aspect ratio is 1:1, which constrains the dimension of the circular pins to 100μm in diameter. Smaller bond pad dimensions are certainly feasible for PolyStrata liquid metal fabrication, but would require a more complex vertical transition design or a change to the standard PolyStrata stack up. Reducing the diameter of the circular pins to approximately 50μm in diameter would allow for bond pad sizes which are comparable to flip chip bond pads.

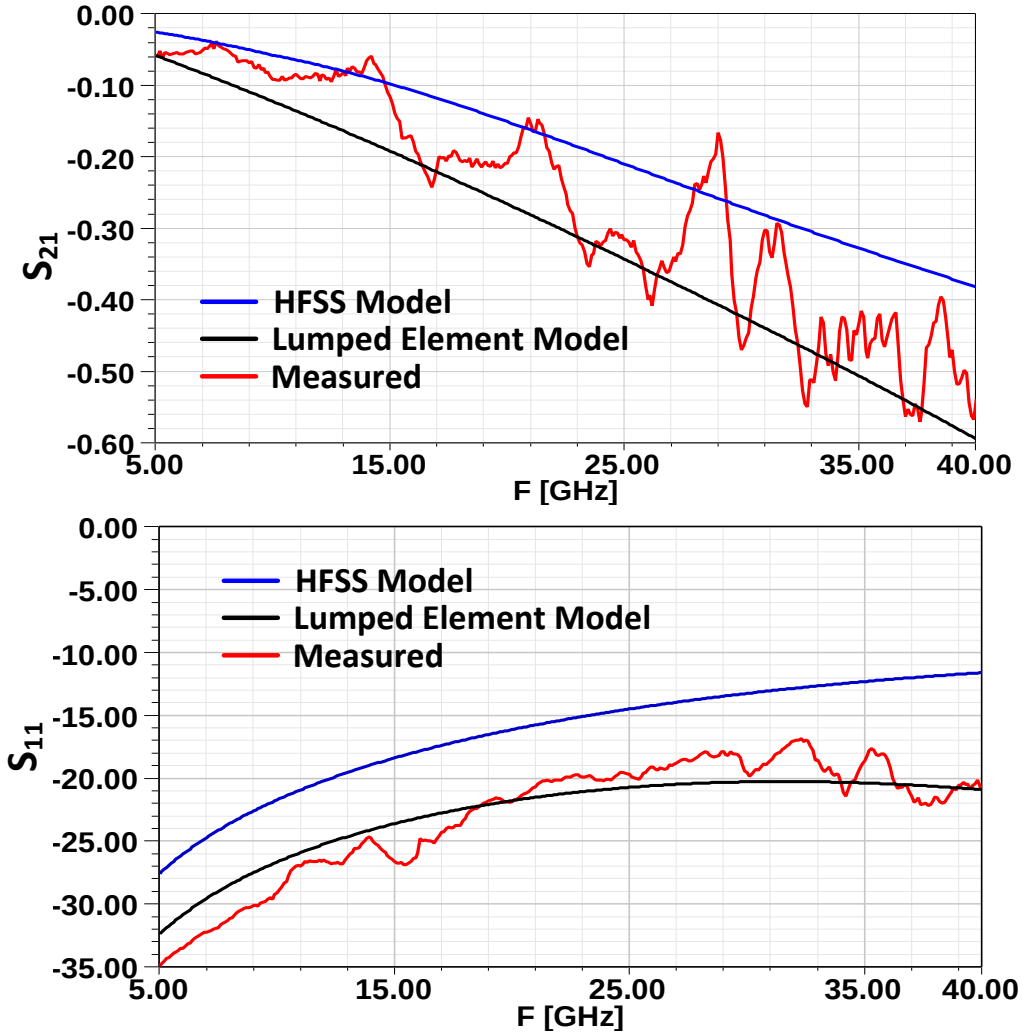

Figure 4.6: A comparison of a single liquid metal interconnect assembly measured results with HFSS simulation results and simulations of the extracted lumped element model of the assembly.

The value for inductance found in this demonstration is a more drastic deviation from the expected results. It is greater than an order of magnitude higher than typical flip chip inductances. Higher inductances are in part due to the high standoff of this liquid metal flip chip connection; typical flip chip solder bumps are on the order of 25μm - 50μm in height. The length of the transition is directly proportional to the value of inductance as explained in Section 1.2.2.

Table 4.1: Lumped Element Values for Liquid Metal Interconnect

Element	**C (fF)**	**L (pH)**	**R (Ω)**
Value	45	150	0.3+0.1*f(GHz)

Another aspect of this liquid metal transition that very likely increases its parasitic inductance is the non conformal contact between the liquid metal and the surface of the PolyStrata transition area. Galinstan's high surface tension, about 535 mN/m, creates a high contact angle between Galinstan and contact surfaces [82]. The ENIPIG passivation layer used on PolyStrata parts has a roughness of approximately 60-70 nm [83]. This surface roughness enhances the wirebondability of PolyStrata parts. However, these two aspects also cause the PolyStrata/Galinstan contact to be non uniform, limiting the area of contact and therefore increasing the resistance and inductance of the liquid metal transition. Figure 4.8 depicts this phenomenon.

Resistance of this liquid metal transition is high not only because of reduced contact area, but also because of a gallium oxide layer that readily forms on Galinstan surfaces when exposed to oxygen. This oxide layer forms when Galinstan is exposed to greater than 0.5ppm of oxygen. The oxide layer is amorphous Ga_2O_3, which stabilizes to a thickness of about $5\mathring{A}$ even when exposed to elevated levels of oxygen and heat [82, 84]. Figure 4.9 shows small volume drops of Galinstan with non spherical shape; this is an effect of the oxide layer which is rigid enough to make small volumes of Galinstan to behave like a gel rather than a liquid.

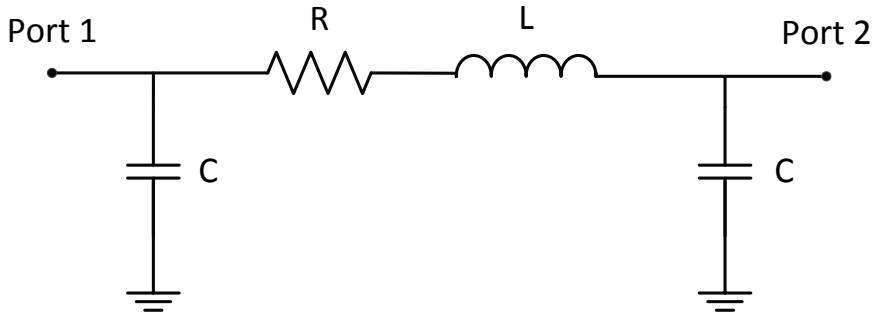

Figure 4.7: Lumped model of liquid metal flip chip transition.

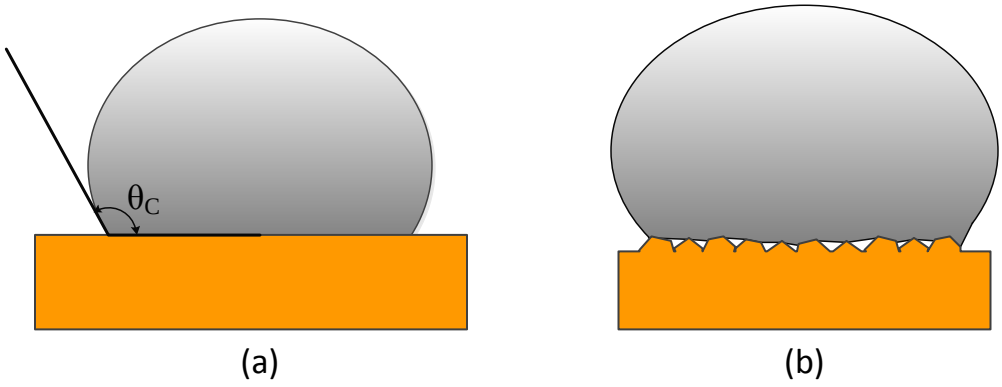

Figure 4.8: Renderings of galinstan droplets on various surfaces. (a) The contact angle of Galinstan is high; the advancing and receding contact angles have been measured to be 146.8° and 121.5°, respectively [82]. (b) On rough surfaces, high surface tension and contact angle cause limited and nonuniform surface contact.

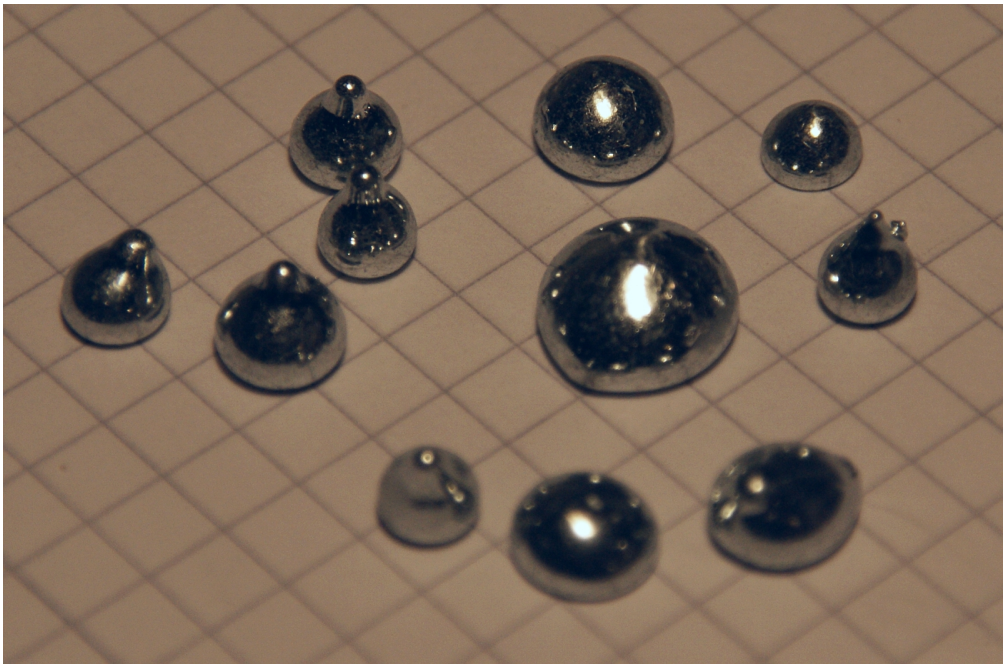

Figure 4.9: Droplets of Galinstan with gallium oxide skin on surface. The rigidity of the skin layer will cause small droplets to behave more like a gel than a liquid, as can be seen by some of the non spherical shapes these droplets have formed.

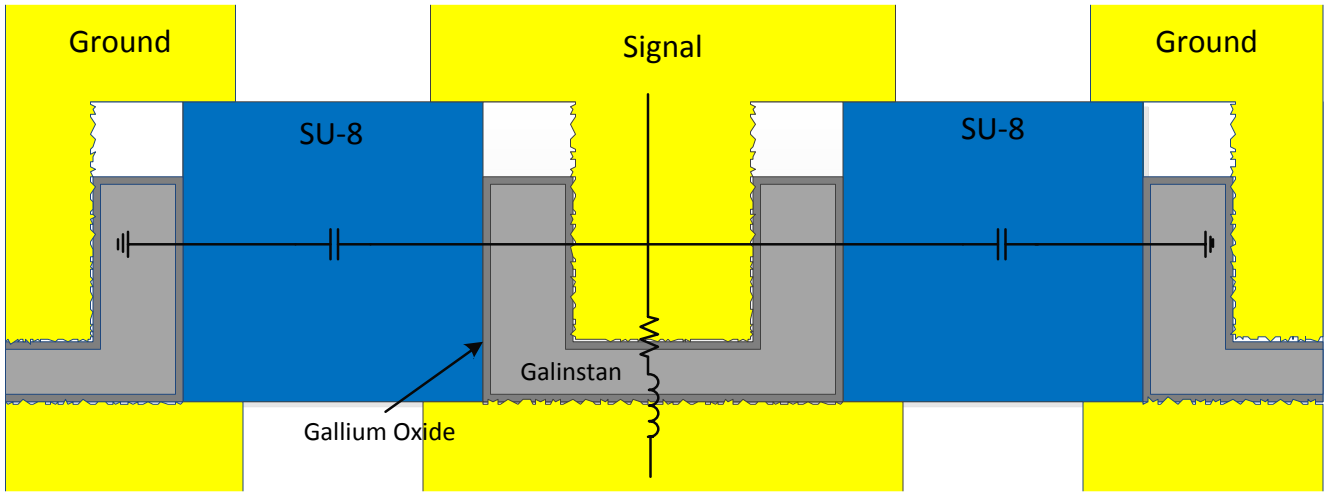

Figure 4.10: Image of a PolyStrata liquid metal cross section, highlighting the parasitic components of the interconnect; shunt capacitance through SU-8 sockets, series inductance and resistance through the pin and rough gold surface contact areas.

4.3 Conclusions

Figure 4.10 shows a cross section of a PolyStrata liquid metal connection which depicts the parasitic elements of a liquid metal transition. Despite the higher values of parasitics of this transition as compared to a standard flip chip connection, these values of capacitance and, most importantly inductance, are still significantly less than typical wirebond values. Wirebond inductance is typically 5 times larger than the inductance derived above [24].

Additionally, there are several means to optimize this liquid metal transition. Depositing a smooth and more uniform gold finish would reduce surface roughness and reduce resistance and inductance of the finished part. An optimized vertical transition design would have smaller pins and bond pad areas, and the standoff height of the transition could be reduced. For maximally reduced resistance, the assembly could be performed in a nitrogen environment, impeding the development of the gallium oxide skin in on the surface of the Galinstan. Such an assembly would also likely require hermetic packaging to keep such an oxide layer from forming on its surface post-assembly.

Overall, this demonstration yielded valuable physical insights, and a preliminary lumped element model was derived that can be used to aid future liquid metal vertical transition integration into microwave system designs.

Chapter 5

Power Handling and Temperature Testing of Liquid Metal Interconnections

Two critical areas of testing which are required to qualify the proposed liquid metal interconnections are power and temperature based testing. Temperature testing is important for two reasons: liquid metal interconnects will transition from liquid to solid when operating at low temperatures, and thermomechanical robustness is a key figure of merit for the proposed liquid metal interconnection. Power handling testing verifies that sufficient levels of high frequency current can be carried by liquid metal interconnections with minimal deterioration in performance, validating that the interface between the liquid metal and pad/pin surfaces is conformal and stable enough for high current conditions.

5.1 Power Handling Testing of Liquid Metal Interconnections

The goal of power handling testing is to confirm that the high frequency power and current levels a liquid metal interconnect can handle are comparable to more standard wirebond and solder based flip chip assemblies. The following sections review the capabilities of wirebond and flip chip technology and describe the testing performed to verify the capabilities of liquid metal flip chip assemblies.

5.1.1 Wirebond and Rigid Flip Chip Capabilities

As a general rule of thumb, the upper current handling limit for a wirebond made with 1 mil wire is approximately 1 amp at DC [85]. The small cross sectional area of wirebonds causes high resistive losses in wirebond connections and limits the power handling capabilities of wirebonds. There are also a limited number of wirebonds that can be attached to a given bond pad area; as a general rule of thumb one wirebond connection can be made for a 0.1 mm$\times$0.1 mm (100μm $\times$100μm), or 0.01mm^2, bond pad [85].

Wirebond failure caused by the application of too much current is an abrupt failure, much like the failure of a fuse when the applied current exceeds the rated current. On the other hand, solder bump connections generally have a significantly higher cross sectional area compared to wirebond connections and in general have higher power handling capabilities. However, there are degenerative failure modes that occur in flip chip solder connections which are caused by high current density through the connections, referred to as electro migration and thermal migration.

Electromigration, the movement of metal particles, due to high current density, electron "wind", in IC metal traces and solder bumps is an issue for many microelectronics designers. In aluminum and copper traces, however, electromigration does not occur until the current

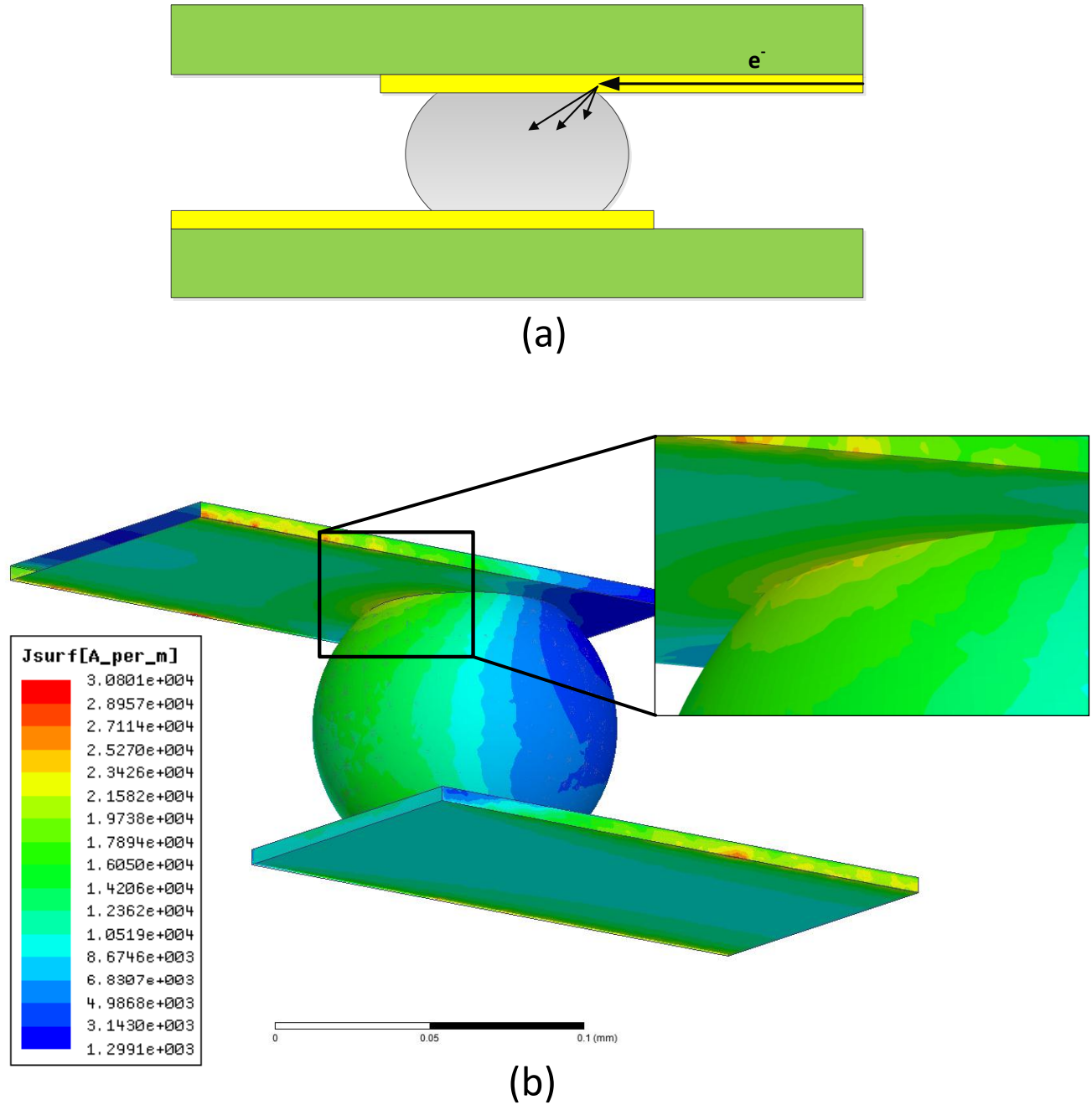

Figure 5.1: (a) Current will crowd at corners and discontinuities of flip chip connections, (b) a simulation of a solder bump with a 50μm cross section and 1 W of applied power quantifies how current concentrates at flip chip solder discontinutes.

density is on the order of 10^6 A/cm^2. Solder joints experience electromigation at current densities on the order of 10^4 A/cm^2 [86]. Current crowding at corners of the signal path in a solder joint increases the current densities at these corners (Figure 5.1), lowering the allowable current through a solder joint. Electromigration will cause voiding and cracking in solder joints which will eventually propagate and lead to complete disconnection of solder joints and open circuiting at this interface. Voids will begin to propagate at these solder joint locations where current density is the greatest, as highlighted in Figure 5.1b. The voiding creates greater discontinuities to current as it flows through the solder bump, inducing an even higher current density around the newly formed void; complete failure of the solder bump typically occurs soon after evidence of voiding is observed.

In Section 1.3.1 it was briefly mentioned how multiple reflow cycles of a solder bump can eventually lead to the deterioration of the solder joint's mechanical characteristics, an effect referred to as spalling. In addition to electromigration, current crowding will cause joule heating of solder bumps to a point where the solder bumps can remelt. If ambient temperature of a solder joint is 100° C, applied current density exceeding 1.6×10^4 A/cm^2 will cause a PbSn solder bump to remelt, and current density exceeding 5×10^4 A/cm^2 will cause a AuSn solder bump to remelt [12]. Remelting only a few times will ruin the electrical connection because the tin in solder slowly absorbs the UBM adhesion metal, allowing the solder bump to easily shear from the surface.

This spalling effect is problematic for high current assemblies or assemblies that require multiple reflow cycles. Copper pillar bumping, discussed in Section 1.1.3, is one way to alleviate the electromigration problem because one side of the flip chip interconnection is a pure copper pillar rather than solder. However, this only alleviates the problem for one direction of current flow; if high current is flowing both into and out of a flip chip assembly, the flip chip interconnection is still susceptible to this spalling effect.

5.1.2 High Power Test Fixture and Setup

High power testing was performed to confirm that liquid metal interconnections can achieve power handling performance that is comparable to the performance of wirebond or flip chip solder connection at RF frequencies. The testing was performed at a continuous wave (CW) frequency of 2 GHz. Using standard, 50Ω loads in a power test set up, at least an average of 1 A of current is needed to verify that liquid metal interconnections can handle at least as much current as a singe wirebond. Power can be quantified with the following relationship;

$$P_{ave} = (I_{RMS})^2 \times R. \tag{5.1}$$

Therefore a minimum of 50 W of average power is required to exceed the power handling of a standard wirebond.

Applying power levels of 50 W and higher with standard RF probes is not practical so, rather than constructing a liquid metal power test structure which requires direct RF probing, a test fixture was designed that is connectorized with SMA connectors for power test via SMA cables. Figure 5.2 shows a rendering of the test fixture. The top and bottom sections of transmission lines are composed of PolyStrata (Figure 5.2a); the bottom section of the PolyStrata transmission line is attached to an alumina base. The dimensions of the liquid metal pin/socket transitions are identical to the dimensions of the single transition pin/socket configuration, discussed in Section 4.1.

Once the PolyStrata transmission lines are interconnected with liquid metal, the alumina base is mounted onto to an aluminum base plate. This aluminum base plate also has CPW transmission line sections, printed on Duroid material, mounted to its surface which transition to Southwest Microwave SMA edge connectors. The center conductors of the CPW and the PolyStrata are interconnected with two wirebonds per transition. Several of these PolyStrata sections of transmission lines are laid out in a row to enable simple transfer to a neighboring transmission line in the event that the tested line fails and is no longer testable.

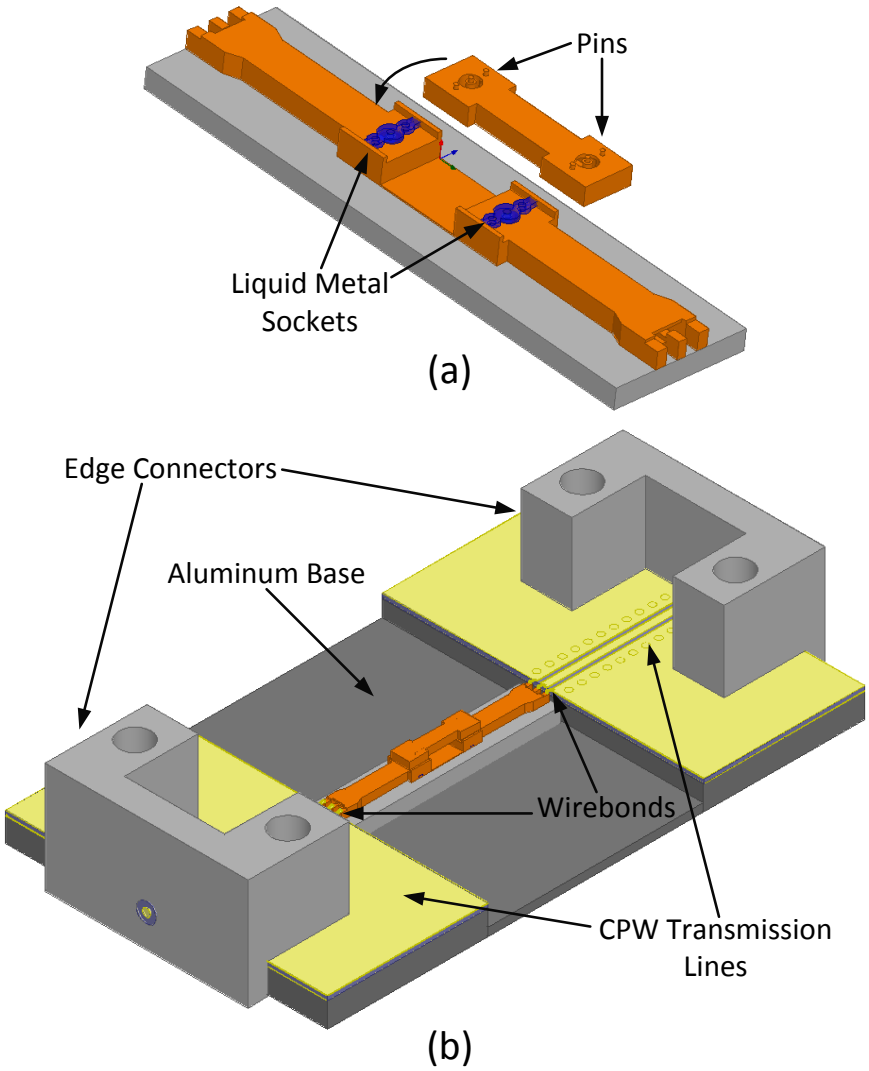

Figure 5.2: Renderings of (a) the high power PolyStrata liquid metal test transmission line, and (b) the completed high power test fixture.

Figure 5.3 shows the completed liquid metal power test fixture.

Continuous wave (CW) power testing was performed at a frequency of 2GHz, and all parts of the test fixture were tested individually at this frequency to confirm their operation at high power.

- The SMA connectors are rated to operate at as high as 400 W of power.
- There is a "thru" transmission line sections that confirms the operation of the Rogers Duroid CPW transmission lines and wirebonds at as high as 200 W of power (Fig-

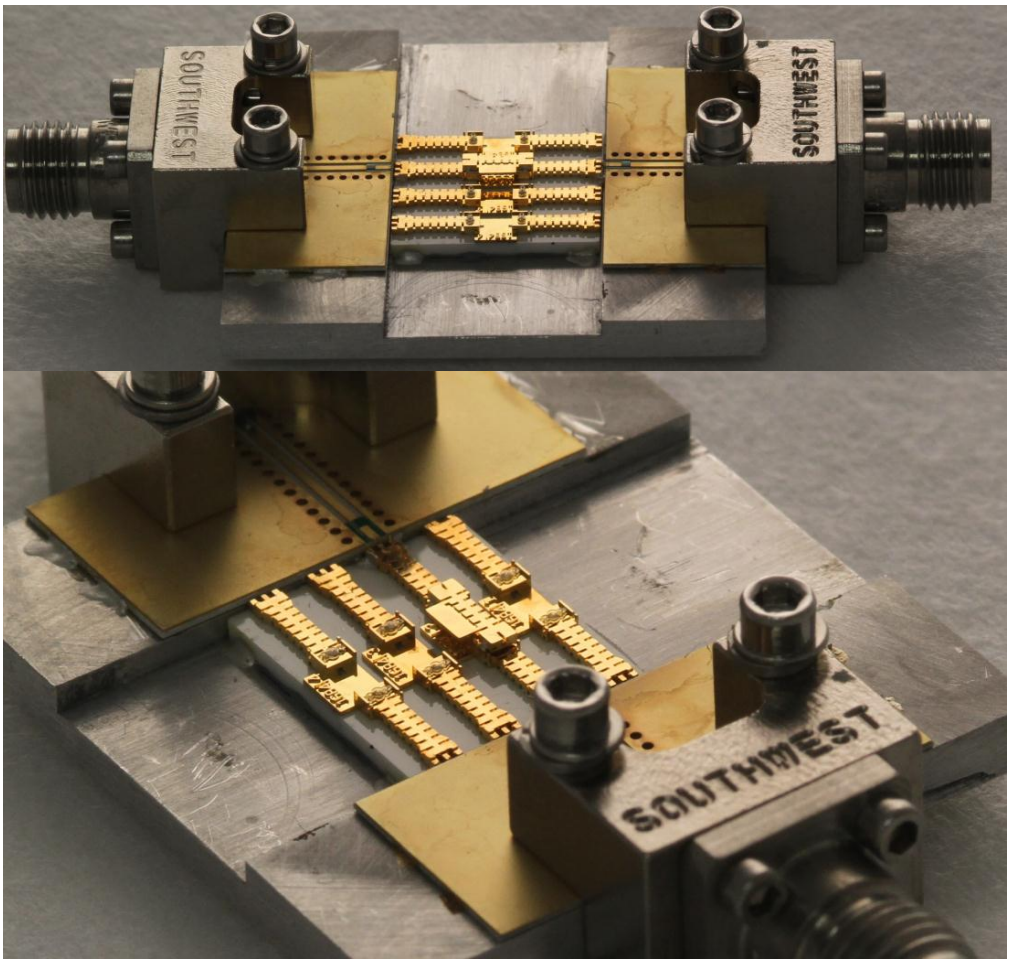

Figure 5.3: Images of the complete power test fixture assembly.

ure 5.4a).

- Two wirebonds are used to for each connection of the PolyStrata transmission line center conductor to Rogers Duroid CPW signal line to ensure robust connection (Figure 5.4b).

- Standard PolyStrata transmission lines without vertical liquid metal interconnections were assembled and tested with applied power as high as 200 W (Figure 5.4c).

- Solid vertical transitions, connected with SAC solder, were tested in PolyStrata out to 80W (Figure 5.4d).

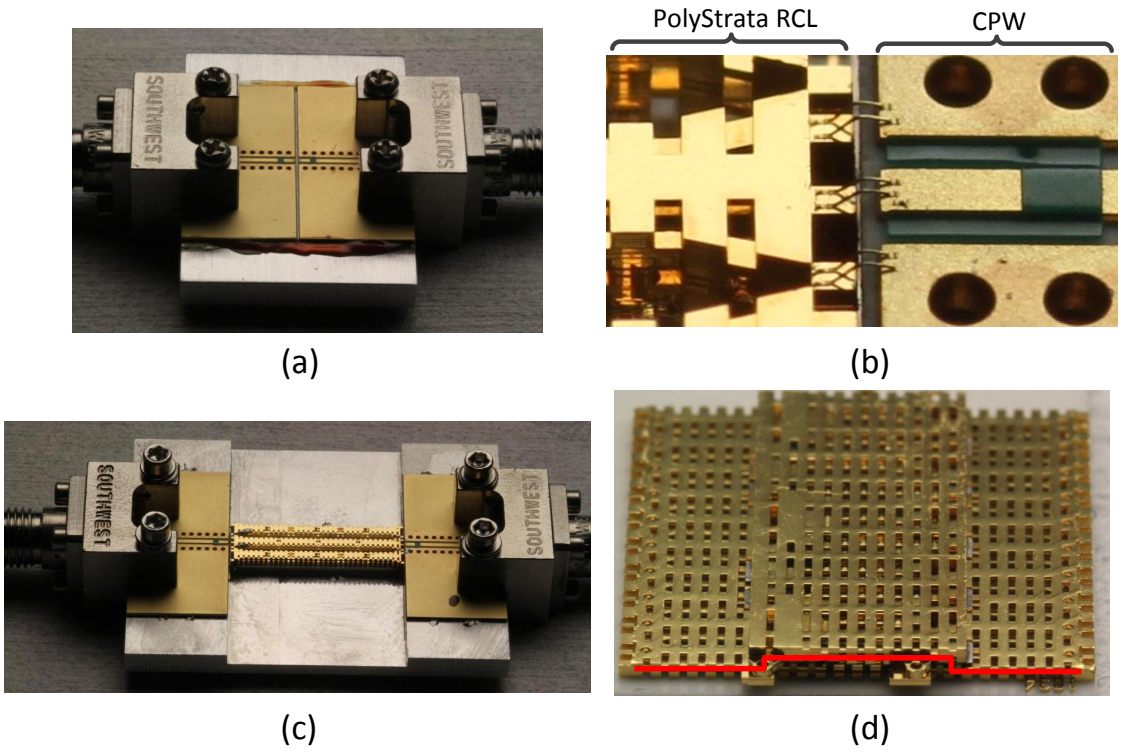

Figure 5.4: Test fixtures for verification of power performance of individual fixture components; (a) a "thru" line with only the CPW and wirebond connections; (b) a close up of the wirebond connections from PolyStrata to CPW; (c) a fixture which tests standard PolyStrata recta coax; and (d) a fixture which tests rigid, solder based vertical transitions (red line highlights the transmission path).

A rendering of the PolyStrata vertical transitions is shown in Figure 5.5. Ten sets of PolyStrata transmission lines, laid out in a row, were connected simultaneously using mechanical features that are a part of the assembly. A more detailed description of the solid (non-liquid) metal based power assemblies and verification of their power performance was reported in reference [87].

Figure 5.6 is a block diagram of the entire high power test set up. A Hittite HMC-T2000 signal generator provides the 2 GHz CW signal which is amplified by an Ethercomm solid state power amplifier. The signal goes through a circulator which protects the power amplifier from reflected power in the case of device failure; the high power signal is diverted

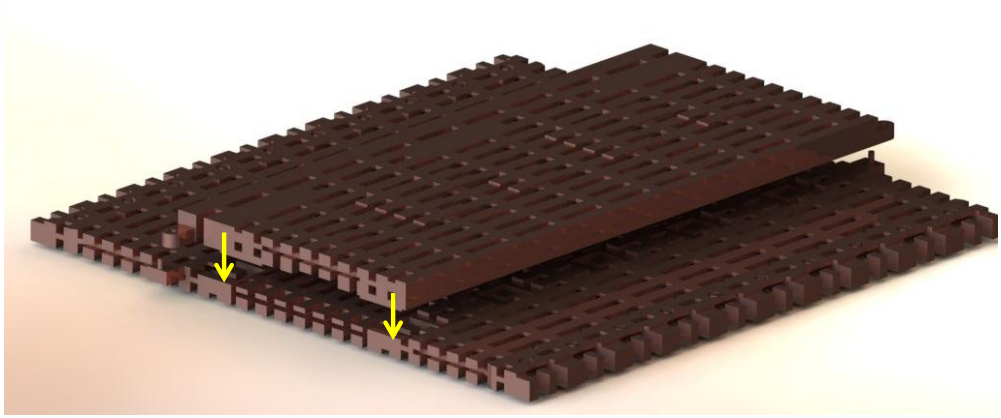

Figure 5.5: Rendering of the vertical assembly test piece

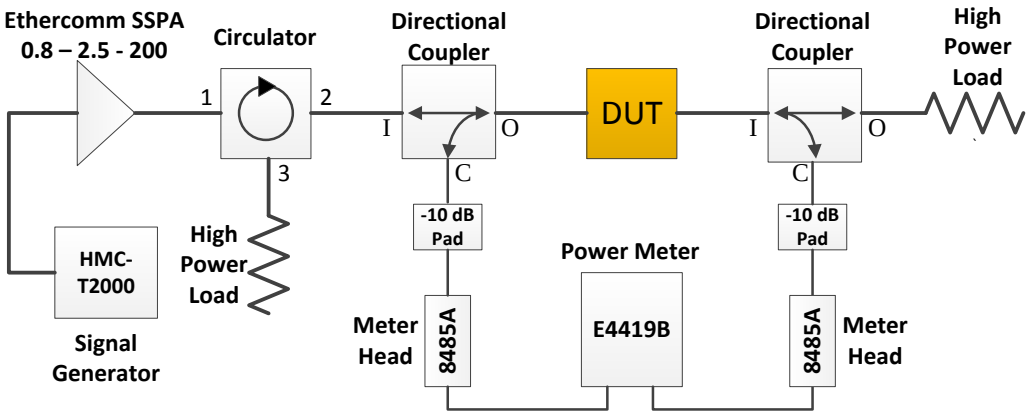

Figure 5.6: Block diagram for power test setup.

to a high power load at port 3 in such a situation. Throughout testing, a power meter is used to monitor power at both the input and the output of the device under test using two Pasternack directional couplers, allowing the user to monitor against catastrophic failure or any slow deterioration of the test fixture's performance. The directional couplers provide 30dB of attenuation at port C, but an additional 10dB attenuator is placed in the path of the power meters so power into the meter does not exceed its maximum allowable input. Figure 5.7 is a picture of the high power test setup at the lab bench.

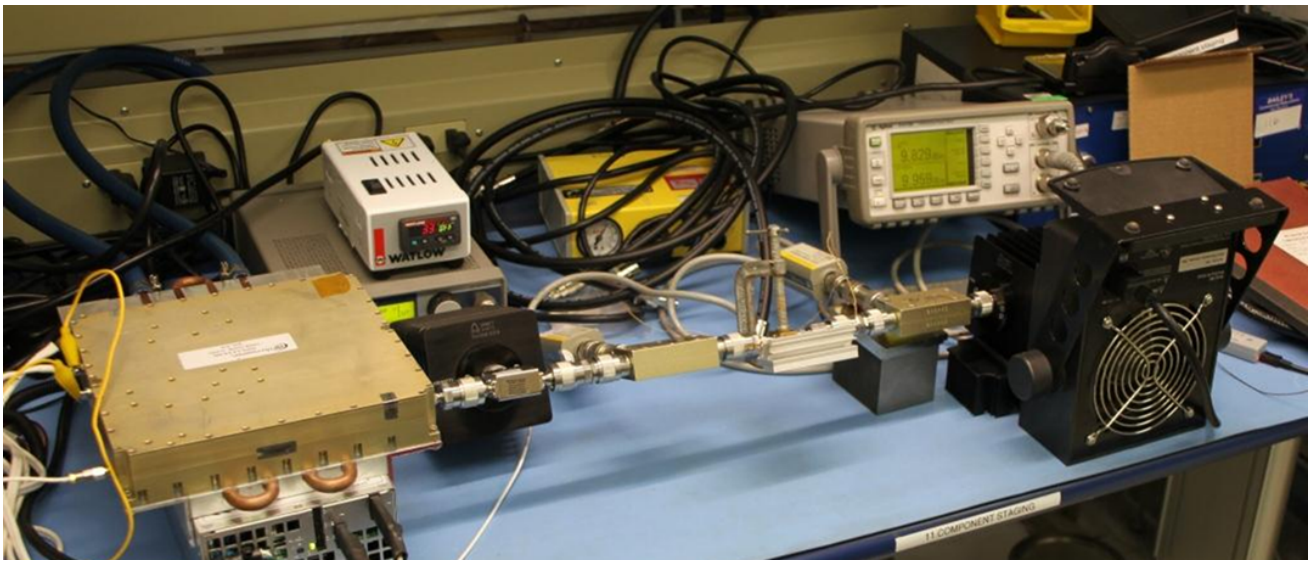

Figure 5.7: Photograph of power test setup.

5.1.3 High Power Test Procedure and Results

Once the test fixture was assembled and ready for high power testing, it first was connected to a network analyzer and small signal S parameter data is taken to obtain the fixture's baseline performance. The network analyzer was calibrated with a 3.5mm coaxial SOLT calibration set before data collection. After capturing baseline RF data, the liquid metal interconnect test fixture was then connected to the high power test setup shown in Figure 5.7 and the applied power manually ramped up to 50W at 2 GHz. The 50W condition was maintained for 1 hour and then the high power is switched off. During power ramp up and the one hour of testing, the power meters which monitor input and output power of the DUT displayed a 0.7dB difference between input and output power. The stability of this measurement throughout testing confirms that there is no notable increase in transmission losses as the fixture heats up during testing.

After high power testing, small signal S parameter data was again collected and compared to the original baseline performance. The test fixture was then reconnected to high power test setup, this time applying 100W of CW power at 2GHz for an hour. After one hour, the

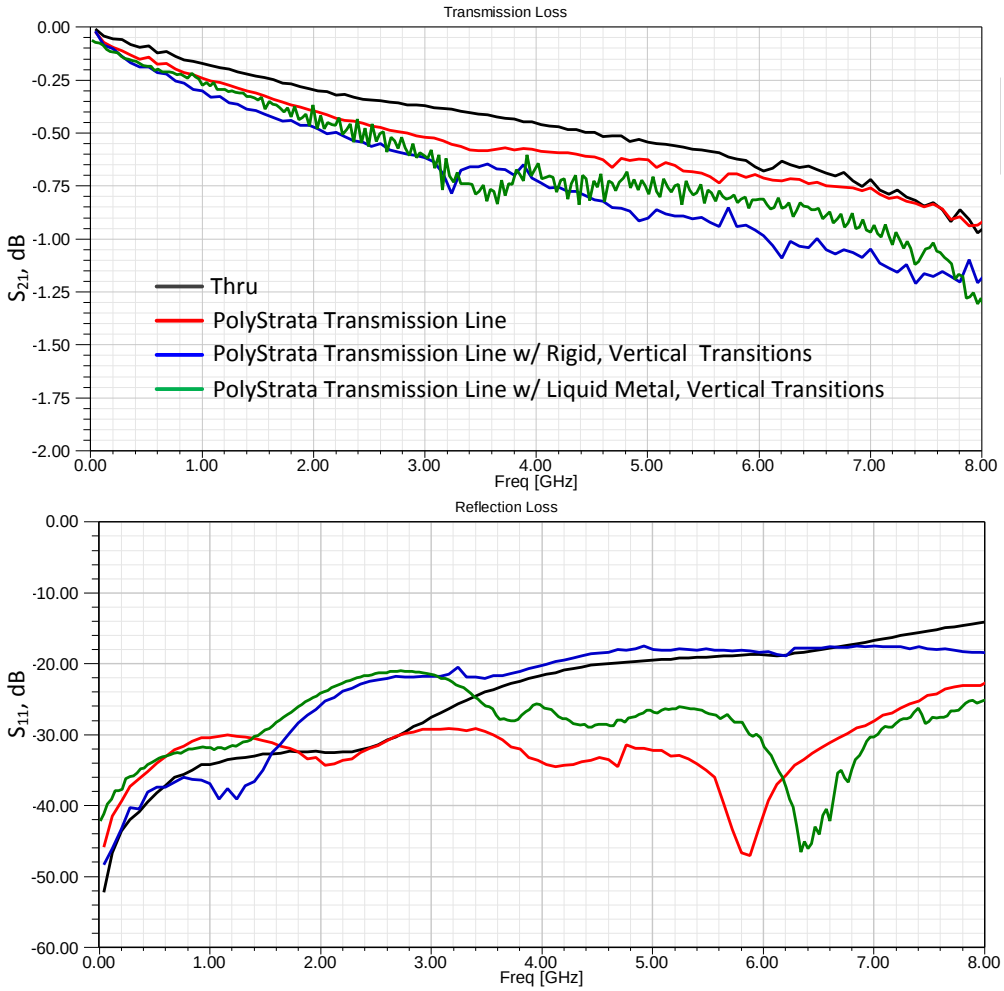

Figure 5.8: Measured small-signal S parameter data for different test fixtures before high power testing.

text fixture was removed and small signal S parameter data was once again recorded.

The "thru" test fixture and other PolyStrata based test fixtures all underwent the same test steps as the liquid metal test fixture; the results of these other power tests are reported in reference [87]. Figure 5.8 compares the S parameter data of four different test fixture configurations before each of these configurations was power tested: the "thru" test fixture shown in Figure 5.4a (black line); the test fixture containing PolyStrata recta coax (red line); the test fixture containing two rigid PolyStrata vertical transitions (blue line); and the test

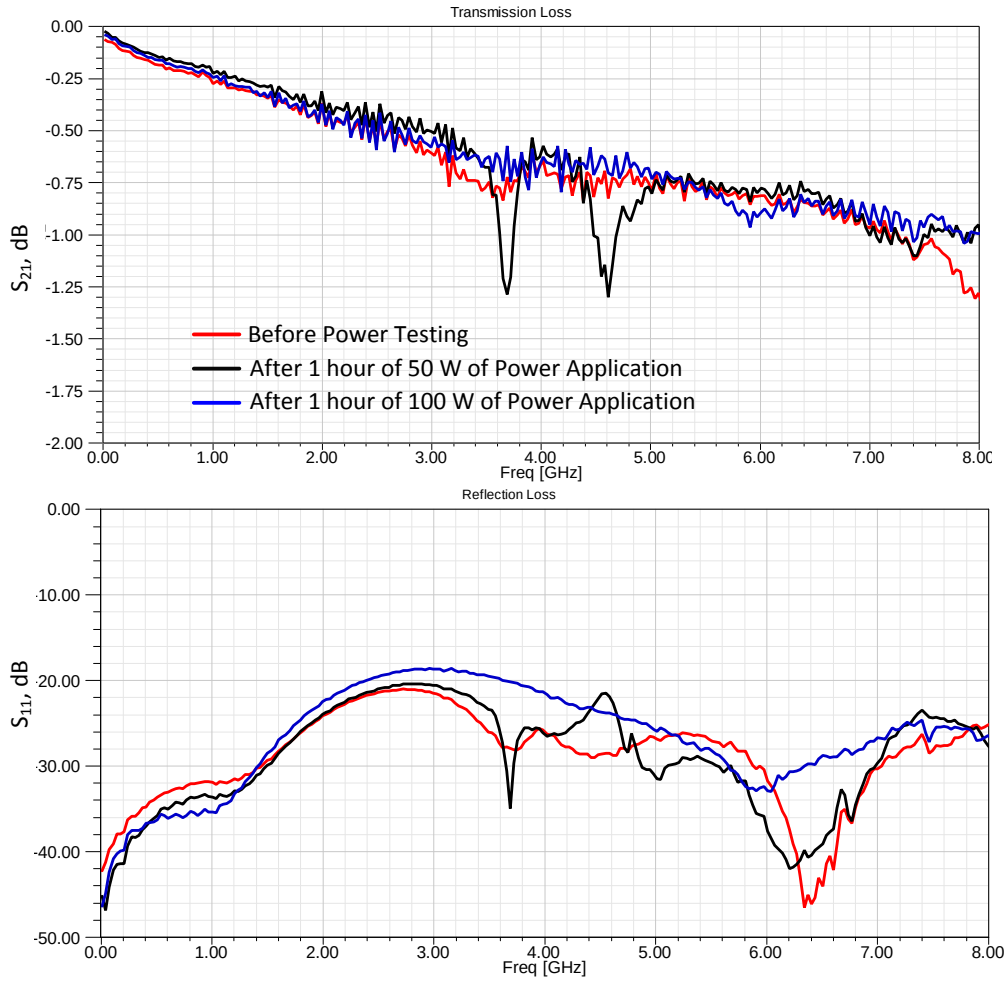

Figure 5.9: S parameter data of the liquid metal test fixture before and after high power testing.

fixture containing two liquid metal PolyStrata transitions (green line). Figure 5.9 compares the baseline data for the liquid metal test fixture to data taken after applying 50 and 100 W of power at 2 GHz for 1 hour each to this fixture.

5.1.4 High Power Testing Discussion

Considering the data shown in Figure 5.8, the transmission loss of the thru test fixture at 8GHz is about 0.9dB, whereas the transmission losses of both the solid vertical transition assembly and the liquid metal vertical transition assembly are close to 1.2dB. Therefore

approximately 90% of transmission loss incurred in these test fixtures comes from the edge connectors and the CPW; additional transmission losses in the PolyStrata based test fixtures are small. Variations in return loss could be due to variations in the quality of the grounding of each fixture.

As seen in Figure 5.9 changes in the overall performance of the liquid metal interconnect test structure after high power testing were small. Average transmission loss for each measurement varies from 0.65dB for the baseline measurement to 0.62dB for the measurement taken after applying 100 W of power to the liquid metal test fixture. The small dips in transmission loss in the 50W data set at 3.7 GHz and 4.6 GHz are likely due to the movements in the cable assembly creating slight resonances. These measurements verify that this fixture can withstand at least 100 W of CW power at 2 GHz; these results are significant when compared to the capabilities of wirebond and solder bump interconnect technology.

Based on equation 5.1, with 100 W of power applied to the test fixture there is 1.4 A of current flowing through these liquid metal transitions. At least two wirebonds would be required to safely carry the same magnitude of 2 GHz current, requiring a bond pad area of approximately $0.02mm^2$. The bond pad area of the liquid metal transition is less than $0.018mm^2$, therefore this amount of current density capability is very competitive with that of wirebond transitions.

Compared to solder bump technology, liquid metal interconnections do not have the temperature limitations of soldered, flip chip interconnects. The intermetallics which create mechanically robust solder joints become a detriment once the temperature of the solder joint approaches or exceeds the solder's melting point, and the continued formation of intermetallics depletes bond pad surface gold. Because liquid metal interconnections do not form intermetallics when contacts are made, high power related failure modes which are caused by joule heating, should not occur. As long as there is good surface wetting between the liquid metal and the pin/bond pad to make a low resistance connection, high current can freely flow through this type of interconnection without deteriorating the integrity of the

interconnection.

5.2 Thermomechanical Analysis of Solid and Liquid Flip Chip Interconnections

This section provides an analysis of solid solder bumps for flip chip interconnections which highlights the size limitations of MMICs that are assembled with rigid solder bumps in a stacked, heterogeneous structure. The result of this analysis is then compared with measured S parameter data from temperature cycling tests conducted on liquid metal interconnections.

5.2.1 Limitations of Solid Solder Bumps

Understanding and predicting the reliability of solder bumps is very difficult and is an area of focused research. There are many variables that affect solder joint robustness. For instance, it is a challenge to isolate creep behavior in stress tests so that elastic and plastic properties can be accurately derived [88, 89]. Also, tensile properties which describe the general stress/strain behavior can be affected by the temperature profile used to reflow the solder bump, the geometry of the solder bump, and the temperature conditioning which occurs before cyclic testing begins. Thus, developing a general model that can accurately predict when fatigue failure (when solder bump cracks/shears from one of the substrates) will occur for a wide variation of flip chip configurations is not realistic.

Very general models can be used to give rough, order of magnitude estimates for specific applied strain rates. By using basic tensile properties for PdSn and SAC solder, an understanding of the limits of flip chip solder bumps can be established for a variety of MMIC/substrate configurations.

Failure due to thermomechanical stresses was briefly discussed in Section 1.3.3. The three forms of strain (elastic, plastic, and creep strain) were introduced. As previously

mentioned, creep strain is a significant contributor to solder fatigue models because of solder's low melting point. The standard which establishes the robustness of electronics going into military equipment, MIL-STD-883, specifies in method 1010.8 that electronics must survive temperature cycle testing to verify thermal robustness [90]. A typical standard that is applied to military standard electronics, condition B, stipulates that electronics need to survive temperature range of -55° C to 125° C. For qualification of these electronics, it is recommended that the electronics survive a minimum of 1000 cycles [91].

With respect to the -55° C − 125° C test temperature range, the homologous temperature (ratio of ambient temperature in degrees Kelvin to melting point temperature, T_m, in degrees Kelvin) range of PbSn solder, which has a melting point of 183° C (456 K), is $0.48T_m$ to $0.87T_m$. For SAC solder, which has a melting point of 217° C (490 K), the homologous temperature range is $0.45T_m$ to $0.81T_m$. Creep deformation becomes significant whenever homologous temperature is above the value of $0.5T_m$; therefore, creep deformation plays a major role in flip chip solder bump failures during temperature qualification of these parts.

A widely recognized fatigue model used to predict failure in metals is the Coffin Mason model, which was developed in the 1950s and is described by the following equation [92]

$$\Delta\gamma N_f^{\alpha} = \Theta \tag{5.2}$$

where N_f is the number of cycles to failure, $\Delta\gamma$ is the plastic strain range, α is the fatigue exponent, and Θ is a material specific constant. Plastic strain range is a ratio of displacement caused by applied forces versus height, as depicted in Figure 5.10, and is given by

$$\Delta\gamma = \frac{\Delta L}{h}. \tag{5.3}$$

For PbSn solder the values for α and Θ are -1.96 and 1.29, respectively, and for SAC solder these values are -0.913 and 26.3 respectively [88, 93].

This model works for stress/strain cycles that are less than 0.3Hz, a frequency fast enough

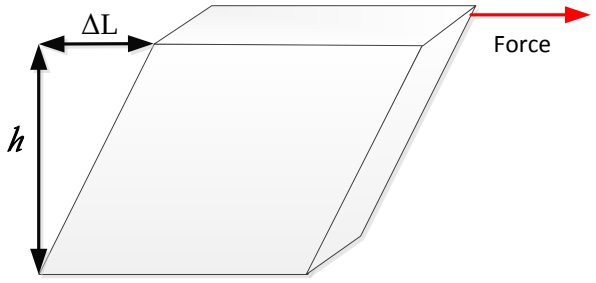

Figure 5.10: Shear stain.

that time dependent, creep deformation plays a negligible role. However for typical electronic systems, with on/off cycle rates that can be minutes, hours, or even days, the frequency of thermomechanical stress/strain cycles are significantly lower than 0.3Hz [94]. Therefore, this fatigue model is not applicable. A better model, which represents typical temperature cycling a solder bump experiences is described as

$$N_f = \frac{1}{2}\left(\frac{\Delta\gamma}{2\epsilon'_f}\right)^{\frac{1}{c}} \tag{5.4}$$

where ϵ_f is fatigue ductility coefficient and c is fatigue ductility exponent, given by

$$c = c_0 + c_1 T_s + c_2 ln(1+f) \tag{5.5}$$

where T_s is average temperature and f is cyclic frequency, 1≤f≤1000 cycles/day. Table 5.1 gives the model parameters for PbSn, SAC, and SnAg solder.

As mentioned previously, qualification of electronics typically requires 1000 temperature cycles over a specified temperature range. A common temperature cycle used for qualification (-55 to 125° C) is based on MIL-STD-883 1010.8, condition B. If an assembly is expected to survive 1000 temperature cycles, then a reasonably conservative value for N_f is 1500. Also established in MIL-STD-883, the period of each cycle is approximately 20 minutes in length, making f of this model 72 cycles per day. Based on these parameters, Table 5.1 gives the maximum value of shear strain that several types of solder can withstand in order to survive

Table 5.1: Low Cycle Fatigue Properties of Common Solders and Max Shear Strain,$\Delta\gamma$, When $N_f = 1500$, $T_s = 35°$ C, and f = 72 cycles/day for a 100μm Tall Solder Bump [94, 95]

Solder	c_0	c_1	c_2	$2\epsilon'_f$	$\Delta\gamma$ **(μm)**
PbSn	-0.442	-6.00×10^{-4}	0.0174	0.65	5.58
SAC	-0.347	-1.74×10^{-3}	7.83×10^{-3}	0.29	3.27
AuSn	-0.416	-2.10×10^{-3}	0.0142	0.49	3.33

this qualification test.

Tables 5.2, 5.3, and 5.4 then show the upper limit of parameter L_{T0}, the maximum distance between two flip chip solder connections at ambient temperature (Figure 5.11), for a wide variety of semiconductor and substrate materials [96, 97, 98]. Because this model largely captures time dependent, creep deformation, additional rigidity provided by the intermediate solder bumps is small, and has very little effect in reducing the total strain experienced by the outer most solder bumps. Therefore the effects of the inter-spaced bumps are not taken into account in this model. The height of the solder bumps is assumed to be 100μm, a typical solder bump height for flip chip assembly. The maximum value of ΔL of a bump is found by solving the following equation

$$\Delta L = \Delta\mathrm{T} \times L_{T0} \left(CTE_{chip} - CTE_{substrate}\right), \tag{5.6}$$

where ΔT is the absolute temperature range (180° C for MIL-STD-883 conditions), and CTE_{chip} and $CTE_{substrate}$ are the different CTE values for the semiconductor/substrate materials, respectively.

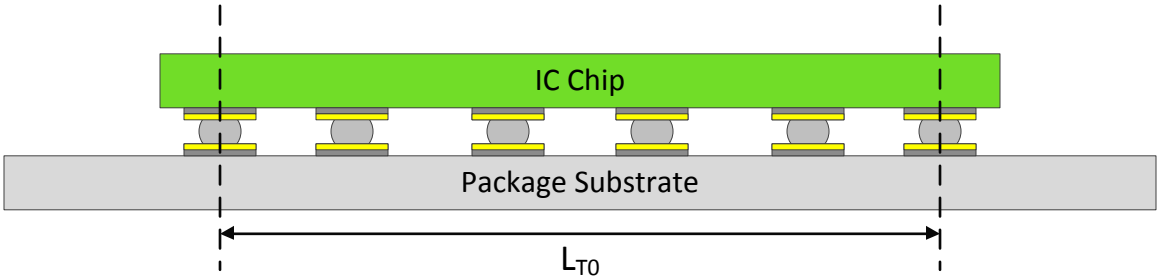

Figure 5.11: Image depicting parameter, L; the maximum distance between two solder interconnects in a flip chip assembly.

Table 5.2: Maximum Length, L_{TO}, Between Two **PbSn** Flip Chip Solder Joints Connecting the Following Materials, in Units of Millimeters

Substrate / MMIC material (CTE ppm)	**Alumina** (6.50)	**FR-4** (15.5)	**GaAs** (6.86)	**GaN** (5.60)	**InP** (4.75)	**Rogers RO 4003C** (14.5)	**Si** (2.60)
FR-4 (15.5)	6.88	–	–	–	–	–	–
GaAs (6.86)	172	7.17	–	–	–	–	–
GaN (5.60)	68.9	6.26	49.2	–	–	–	–
InP (4.75)	35.4	5.76	29.4	72.9	–	–	–
Rogers RO 4003C (14.5)	8.26	41.3	8.68	7.38	6.70	–	–
Si(2.60)	15.9	4.80	14.6	20.7	28.8	5.44	–
SiGe (3.90)	23.8	5.34	20.9	36.5	72.9	6.14	47.7

Table 5.3: Maximum Length, L_{TO}, Between Two **SAC** Flip Chip Solder Joints Connecting the Following Materials, in Units of Millimeters

Substrate / MMIC material (CTE ppm)	**Alumina** (6.50)	**FR-4** (15.5)	**GaAs** (6.86)	**GaN** (5.60)	**InP** (4.75)	**Rogers RO 4003C** (14.5)	**Si** (2.60)
FR-4 (15.5)	4.03	–	–	–	–	–	–
GaAs (6.86)	101	4.20	–	–	–	–	–
GaN (5.60)	40.3	3.67	28.8	–	–	–	–
InP (4.75)	20.8	3.38	17.2	42.7	–	–	–
Rogers RO 4003C (14.5)	4.84	24.2	5.09	4.32	3.93	–	–
Si(2.60)	9.31	2.81	8.52	12.1	16.9	3.18	–
SiGe (3.90)	14.0	3.13	12.3	21.4	42.7	3.59	27.9

Table 5.4: Maximum Length, L_{TO}, Between Two **AuSn** Flip Chip Solder Joints Connecting the Following Materials, in Units of Millimeters

Substrate / MMIC material (CTE ppm)	**Alumina** (6.50)	**FR-4** (15.5)	**GaAs** (6.86)	**GaN** (5.60)	**InP** (4.75)	**Rogers RO 4003C** (14.5)	**Si** (2.60)
FR-4 (15.5)	4.11	–	–	–	–	–	–
GaAs (6.86)	103	4.29	–	–	–	–	–
GaN (5.60)	41.1	3.74	29.4	–	–	–	–
InP (4.75)	21.2	3.44	17.6	43.6	–	–	–
Rogers RO 4003C (14.5)	4.94	24.7	5.19	4.41	4.00	–	–
Si(2.60)	9.49	2.87	8.69	12.3	17.2	3.25	–
SiGe (3.90)	14.2	3.19	12.5	21.8	43.6	3.67	28.5

For many cases, values of L_{T0} are large enough that a flip chip assembly would not likely be limited by CTE induced thermomechanical constraints. Many semiconductor materials have CTE properties that are reasonably close to one another. But, when assembling MMIC chips directly on FR-4 material, or high frequency board material, such as Rogers RO 4003C material, CTE mismatch will limit the size of chips which can be used. There are also many other substrate materials which have comparable CTE to these substrates (on the order of 10 - 20 ppm) including copper, with a CTE of approximately 16.7 ppm.

Solder bumps have a limited aspect ratio; the ratio of height versus diameter of a solder bump is typically less than 1:1 [1]. Therefore, it is often desirable to reduce the height of the solder bump because this will also reduce the size of the bond pad required and allow for a more dense concentration of interconnections and smaller bond pad parasitics. However, L_{T0}, directly scales with the height of the solder bump, h, because $\Delta\gamma$ is inversely proportional to h as seen from Equation 5.3. Therefore, scaling down to smaller solder bumps also directly drives down the thermo mechanical robustness of the entire flip chip assembly. So, for example, if a designer chooses to stack a GaN chip onto a Si chip, using 25μm tall AgSn solder bump (rather than an 100μm tall solder bump), L_{T0} is reduced from a 12.3mm to about 3.1mm. GaN technology is an excellent technology for RF/microwave power amplifier design [24]. Because typical power amplifier MMIC design consists of several transistor stages which require die area for layout, the dimensions of a power amplifier MMIC chip will often exceed 3.1mm, making many GaN power amplifiers unusable in such a scenario.

5.2.2 Verification of Flip Chip Liquid Metal Interconnect Thermal Robustness: Temperature Cycling

The single liquid metal interconnection assembly presented in Section 4.1 was also used for temperature cycling testing. After baseline, small-signal S parameters of the assembly shown in Figure 4.6 were measured from 10MHz - 40GHz, this assembly was placed in an FTS System Turbo Jet temperature cycle chamber, where it was exposed to temperature

cycles ranging from -40° C to 125° C. Each cycle took 20 minutes to complete, as per MIL-STD-883 1010.8. The lower limit of the temperature cycle was 15° higher than the range specified in MIL-STD-883 1010.8 Condition B, due to limited temperature programs available at the time the temperature testing was conducted. The assembly was taken out after 100 cycles, visually inspected, and small-signal S parameter data was again taken from the part. The assembly was then returned to the chamber for another 100 temperature cycles and remeasured once the second set of 100 temperature cycles completed. Figure 5.12 shows the small signal S parameter data of these three measurements.

As can be seen, the performance of the single transition assembly is basically unchanged after as many as 200 cycles. Each sequence of 100 cycles took over a day to complete, causing the network analyzer to require recalibration prior to each measurement. The slight variations between data sets is likely due to variations in these calibrations. Even though this assembly is fabricated in the PolyStrata process, and both the top and bottom transmission lines are composed entirely of copper, the bottom section of transmission line is attached to an alumina substrate, which physically constrains the bottom transmission line to the thermal expansion of the alumina (6ppm/°C). Meanwhile, the top transmission line is mechanically constrained,at one end by its epoxy attachment to the base platform. Therefore the expansion of the structure is constrained to one direction, as shown in Figure 5.13. The total length of the top transmission line is 3.3mm. Using Equation 5.6 and solving for $\Delta\gamma$, the expansion of the top transmission line, relative to the bottom transmission line is 5.8μm over the temperature range of -40°C - 125°C.

Based on the fatigue model given in Equation 5.4, solid solder bumps would also survive 200 temperature cycles with the same distance of strain flex applied during the temperature cycling, but the applied strain is approaching the limits of what a standard solder bump can handle; with N_f equal to 200, a PbSn solder bump's maximum strain is 13μm and a SAC solder bump's maximum strain is 7.2μm. Based on the design of the liquid metal interconnections used in this experiment, it is conservative to predict that more applied strain would not have caused the liquid metal interconnections to fail; their flexible architecture allow

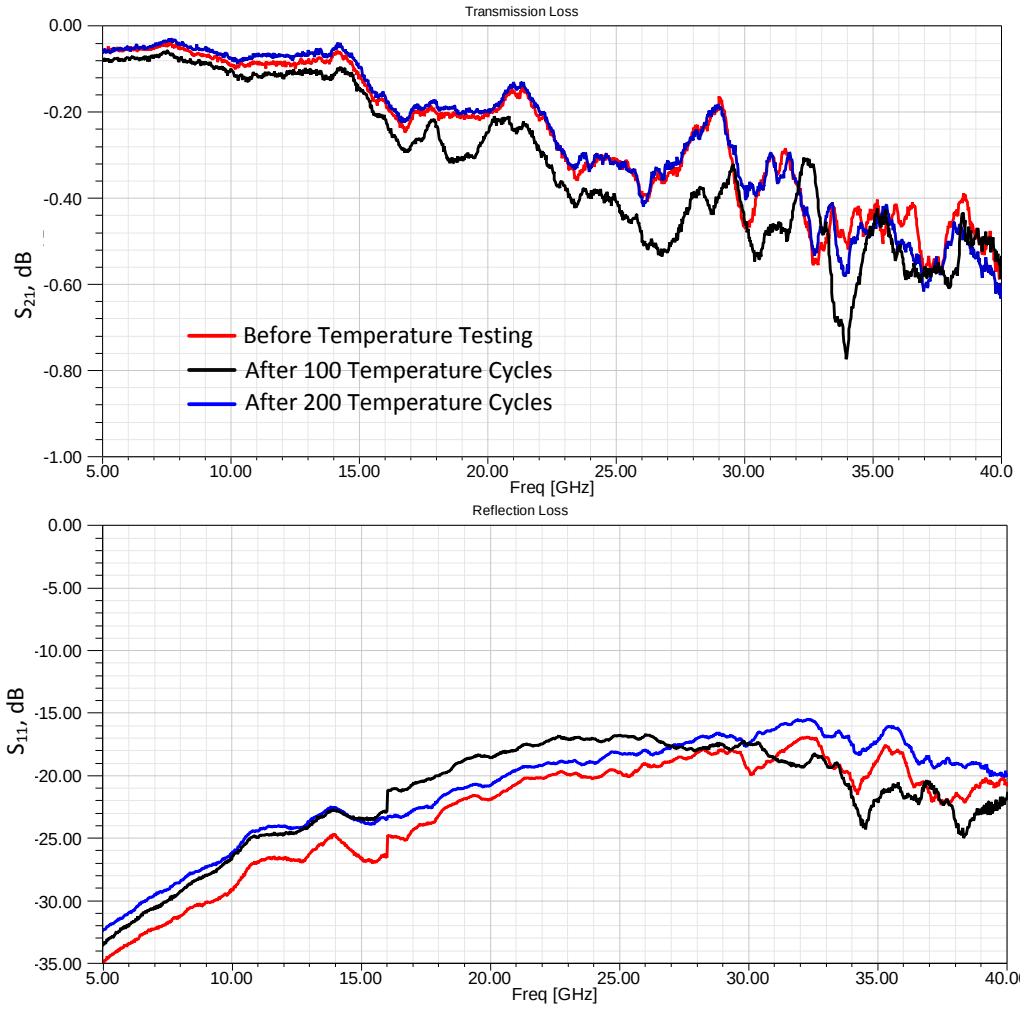

Figure 5.12: A comparison of the single transition assembly s parameter data before and after temperature cycling.

for strain values that far exceed the limitations of PbSn and SAC solder. This experiment proves that liquid metal interconnections have the thermal robustness to survive at least 200 cycles of extreme temperature cycles.

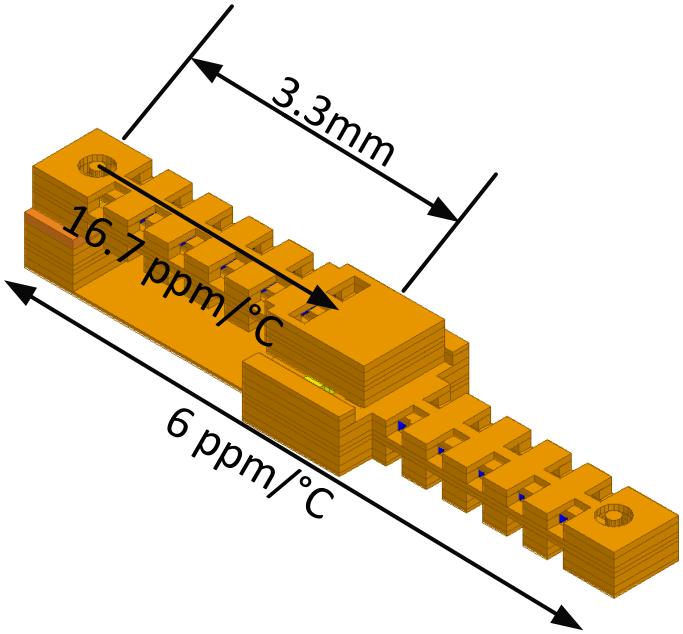

Figure 5.13: Image showing the expansion of top and bottom sections of the single vertical transition assembly.

5.2.3 Liquid Metal Interconnect Performance at Extreme Temperatures

The melting point of the galinstan eutectic chosen for this experiment is 10° C, which means during temperature cycling the phase of the interconnect actually transitions from liquid to solid and then back to liquid multiple times. Therefore, determining if there is significant deterioration in electrical performance over a wide range of temperatures, specifically low temperatures where the liquid metal is near its freezing temperature, is necessary for to the verification of this style of interconnection.

Directly probing the single interconnection transition and recording S parameter data during temperature cycling would be an ideal way to perform this experiment. Unfortunately, a temperature controlled probe station was not available to perform such tests. In lieu of this, the existing test fixture used to verify the power handling performance of liquid metal interconnections, shown in Figure 5.3, is used for this test. This set-up allows for connectorized testing rather than direct probing, and safe cycling of the assembly temperature

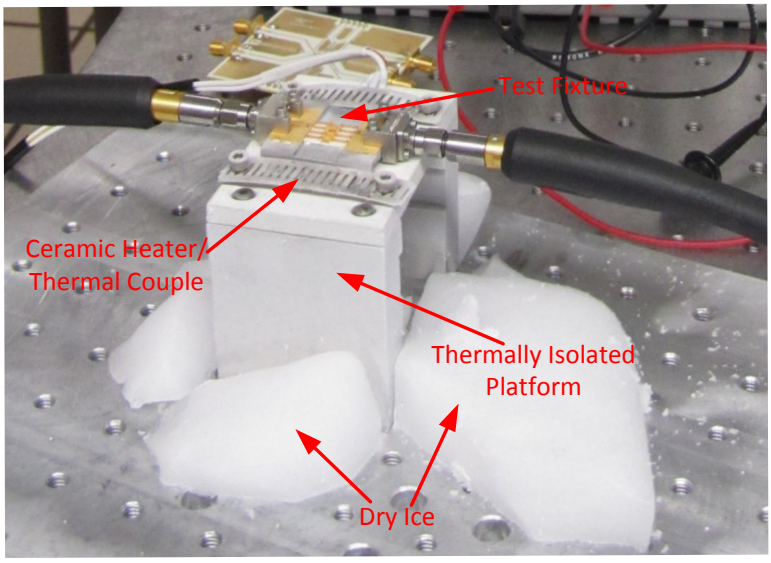

Figure 5.14: Picture of the power test fixture on the thermally isolated table, using dry ice for low temperature testing.

without exposing expensive, high precision equipment to the same temperature variations. As mentioned previously, the dimensions of the pin/hole connections are the same as the dimensions of the single liquid metal transition assembly, shown in Figure 4.3. Electrical signals are routed onto the PolyStrata structures via an SMA edge connector to a CPW transition on Rogers soft board material. The CPW then transitions to PolyStrata via a wirebond connection, as shown in Figure 5.2. The SMA edge connectors maintain good performance out to approximately 18 GHz, therefore the range of data recorded ranges from 10MHz to 18 GHz.

This assembly is placed directly on a small ceramic heater attached to a thermally isolating platform. The heater, which has heating capabilities that range from 0°C to 300°C, has a built-in thermocouple so that temperature of the ceramic is always known. The temperature of the thermally isolating platform, the ceramic heater, and the assembly can also be lowered by introducing dry ice around the platform and then insulating the test station with a Styrofoam box. Figure 5.14 shows a picture of this test set up under cooling with dry ice.

This method allows the temperature of the liquid metal assembly to reach a steady state temperature as low as -25° C. Once at this temperature, the condition is maintained for 10 minutes before the dry ice is removed from the test fixture and the interconnect assembly is then allowed to warm to 0° C. After the temperature of the assembly exceeds 0° C, the ceramic heater is used to control the ramp up of temperature, until the assembly has reached a temperature of 125° C. Small signal S parameter data is recorded every time the temperature of the assembly increases by 10 - 15°C during this testing.

The measured data recorded reveals some interesting behavior of metals that are under strain while approaching their melting point. The temperature of the assembly was brought down to -25° C quickly, and while at this temperature, the S parameter data changed little. In fact, the overall transmission loss of the assembly was reduced slightly, which is expected since resistive properties of metal are directly proportional to metal's temperature over the ranges of temperature studied here. However, as the temperature is slowly raised to a value close to Galinstan's melting point, creep deformation becomes more and more of a factor. Figure 5.15 compares the difference in transmission loss of the assembly at various temperature relative to the transmission loss of a room temperature assembly. As the assembly warms to 0° C, the performance of the assembly drops off dramatically.

Examining a generic creep curve shown in Figure 5.16, creep strain has three stages: primary creep, secondary creep and tertiary creep. Once a metal has transitioned into the tertiary creep stage, fatigue failure is often imminent,as depicted in Figure 5.16. What is likely being observed in the measurements shown in Figure 5.15, is that while the assembly's temperature is cooler than Galinstan's freezing temperature, the Galinstan material is under shear strain because the top copper transmission line shrinks at a faster rate than the bottom transmission line that is mechanically constrained by the alumina substrate it is attached to. When the assembly temperature stabilizes around -25° C, the Galinstan is likely undergoing secondary creep. Then as the Galinstan slowly warms, it becomes more and more malleable, and the tensile properties of this material decline at a dramatic rate. The creep deformation exceeds its secondary creep stage and goes into tertiary creep, and the interconnection

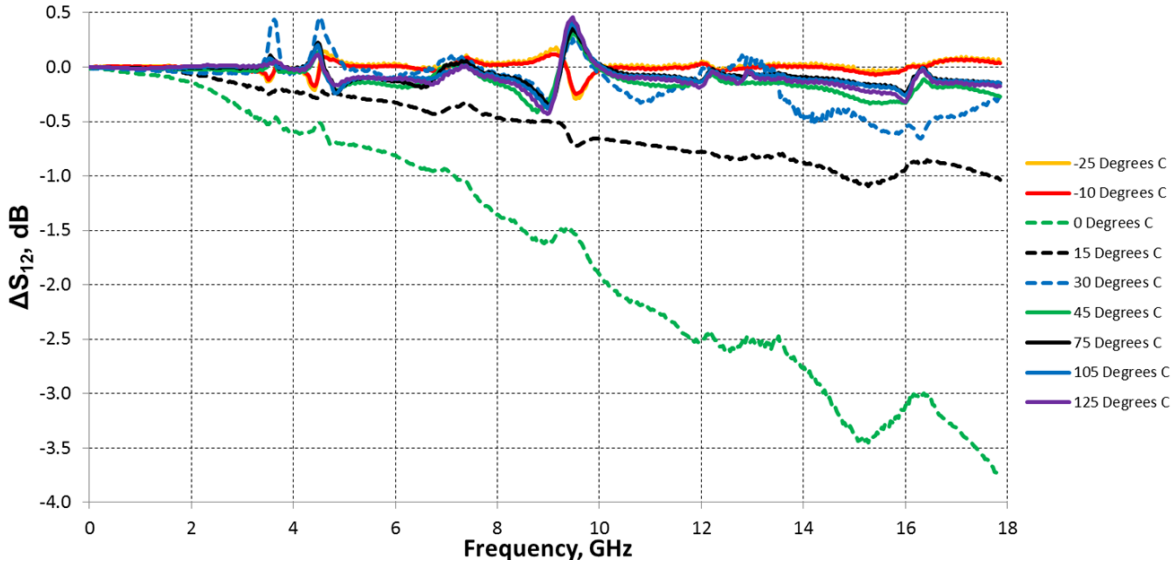

Figure 5.15: A comparison of the liquid metal assembly's transmission loss at different temperatures, normalized to the performance of a liquid metal assembly at room temperature.

undergoes cracking/delamination from the surface of the pin and/or the surface of the bond pad area, significantly deteriorating the performance of the interconnection.

This kind of performance would typically be unacceptable for a rigid configuration. However, the liquid metal interconnect quickly recovers from the observed performance deterioration soon after the temperature of the assembly exceeds the melting point of the connection and the liquid metal re-wets to all surfaces, as can be observed in the data of Figure 5.15. The liquid metal interconnect nearly recovers its original performance once the temperature of the assembly returns to room temperature. This experiment was repeated two more times and each time the outcome was very similar, with the performance of the assembly falling off as its temperature exceeded -10° C but then quickly recovering as the assembly temperature approached room temperature.

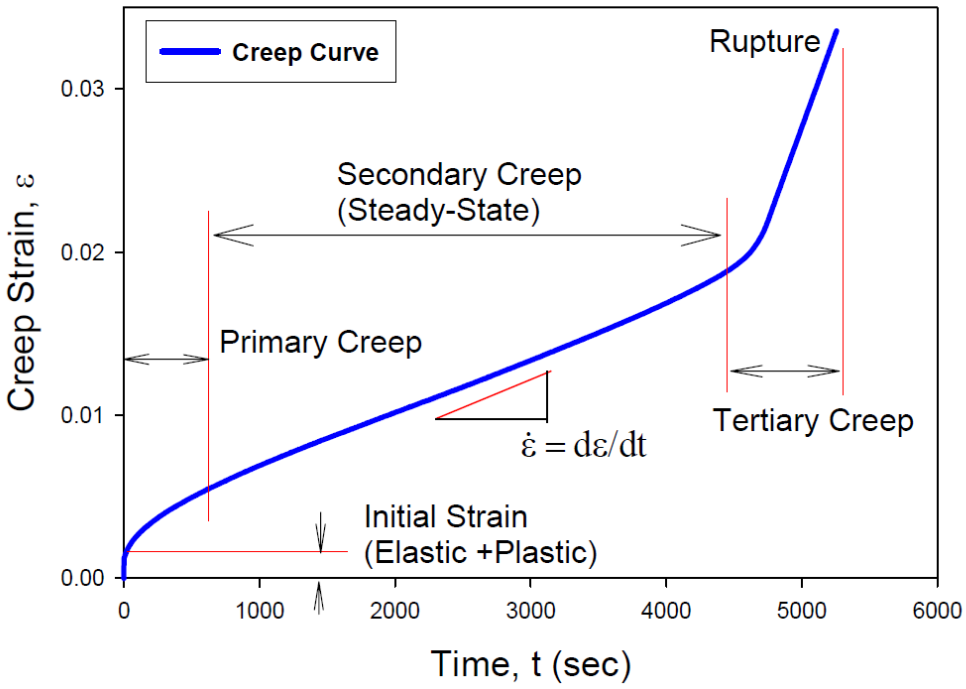

Figure 5.16: Generic creep strain curve for metal deformation.

5.2.4 Temperature Testing Discussion

S parameter testing vs. temperature discussed in the previous section shows that operation of liquid metal interconnections is non linear once the liquid metal transitions into a solid phase, but this non linear behavior is consistent and predictable. Deterioration in performance of the interconnect, while the liquid metal is in its solid phase, is recovered once the Galinstan remelts and rewets to all surfaces. As presented in Section 5.2.2, a single liquid metal interconnection survives as many as 200 temperature cycles from -40° C to 125° C, verifying that the freeze/thaw cycling of liquid metal interconnections do not cause long term performance deterioration.

Performance deterioration of liquid metal connections while the metal is in a solid phase could potentially be a serious problem for applications that have "cold start" requirements. One solution that would alleviate this issue is the utilization of a liquid metal that has a lower melting point. The composition of the Galinstan variant used in these experiments was

$Ga_{62}In_{22}Sn_{16}$ which melts at approximately 10° C. However, there are other compositions that melt at lower temperatures, such as $Ga_{68.5}In_{21.5}Sn_{10}$ which melts at -19° C. Additionally, mercury, which has a melting point of -39° C, could also be a possible alternative for liquid metal interconnections in very cold environments albeit having toxicity issues. Using a lower melting point liquid metal reduces the operating temperature limitations of such a interconnect, however, if an IC assembly is required to perform at temperatures lower than -19° C; in this case a more thorough investigation of the Galinstan's tensile properties while the material is in its solid phase would be necessary to determine what levels of shear strain liquid metal interconnections can safely withstand below their freezing point.

5.3 Summary

This chapter has presented testing of liquid metal interconnections to verify both their power handling capabilities and their performance when subject to temperature extremes. High power testing confirmed that liquid metal interconnections are suitable for high RF current assemblies. Furthermore, based on the limitations and issues of wirebonding and solid solder based interconnections, it is suggested that liquid metal interconnections can exceed the capabilities of more traditional, level 1 packaging. Temperature testing confirms that extreme temperature cycling does not deteriorate the performance of liquid metal connections. However the performance of liquid metal interconnections at low temperatures, when the interconnect material is in its solid phase, becomes non linear. Using a Galinstan eutectic with a lower freezing point would partially alleviate this problem, but this approach would need further study to fully understand the limitations of liquid metal interconnection performance at very low temperatures.

Chapter 6

Conclusions and Future Work

6.1 Conclusions and Contributions

This dissertation has presented new approaches and results for the design, fabrication, and analysis of liquid metal vertical interconnections. The following contributions to the advancement of liquid metal, flip chip interconnetions have been made:

- MMIC chip post processing techniques which establish permanent layers of polymer, SU-8, on surface of individual ICs for liquid metal interconnect structures.
- Design and characterization of a heterogeneous liquid metal flip chip assembly for active, integrated circuit onto planar and 3 dimensional carriers.
- Modeling and analysis of individual, flip chip liquid metal RF transitions and their parasitics.
- Verification of the power handling capabilities of vertical liquid metal interconnects.
- Verification of the thermal robustness of vertical liquid metal interconnects.

These contributions are discussed further below.

Using a DRIE process to pattern the surface of a sacrificial Si wafer with cavities for planarization to the wafer surface, individual MMIC chips can be post processed with high aspect ratio sockets made from SU-8. The high aspect ratio of the SU-8 allows for minimal SU-8 footprints to achieve effective sockets and thus minimizes the polymer's effect on the MMIC's performance.

Power amplifier MMICs that were interfaced to CPW and PolyStrata substrates with flip chip, liquid metal interconnections showed encouraging results over C-band frequencies. In the first heterogeneous integration approach developed, the MMIC was flip=chip integrated onto high resistivity Si with CPW traces. A conformal SU-8 layer was deposited on the surface of the MMIC as discussed above, with sockets at the bond pad locations and pins plated onto the CPW lines. Liquid metal was squeegeed into the MMIC sockets and the MMIC was flip chip bonded. The response of the MMIC (return loss, and gain) closely matched the MMIC data sheet performance, with an average insertion loss of each transition at the chip's passband of about 1.8dB. Plating of gold pins onto the surface of MMIC chips was also attempted to simplify the process with inconsistent results.

The second heterogeneous approach integrated a MMIC onto PolyStrata recta coax transmission lines. For this design the areas of SU-8 on the surface of the MMIC was made more limited, only depositing SU-8 around the bond pad locations. In addition, a cleaner, more controlled, "pick-and-place" method was developed to deposit the liquid metal. Additionally, the MMIC backside ground plane and thermal connection was improved using a copper baseplate which was also made in PolyStrata. The resulting assembly performed significantly better that the previous design with insertion loss of each transition averaging around 0.7dB over the MMIC passband.

Single transitions were also designed and fabricated in PolyStrata in order to develop a lumped element model of a liquid metal transition for future design establishment and to confirm the parasitics of the liquid metal are competitive with wire bond and solid flip chip designs. The extracted lumped element model of this assembly indicated that the

liquid metal transition has a capacitance of 45fF, an inductance of 150pH and a frequency dependent resistance of $(0.3 + 0.1\times10^{-9} * f)\Omega$. These values of capacitance and inductance are smaller than typical capacitance and inductance of wirebond interconnections (on the order of 1pF and 1nH) but still higher than typical flip chip connections (on the order of 10pH and 10fF).

Power handling testing verified that liquid metal interconnections are capable of handling continuous wave RF power of 100W for at least an hour without deterioration of the interconnections RF performance. Power handling of solder and wirebond connections is limited, so the potential of liquid metal interconnections for high power operation and long term reliability is a significant reason to continue pursuing this method of connection.

Temperature cycling testing shows that liquid metal interconnections maintain good RF performance after 200 temperature cycles, ranging from -40°C to 125°C, a good indicator that the thermal robustness of liquid metal interconnects is at least competitive with traditional, solid flip chip interconnections. S parameter measurements of liquid metal interconnections were taken over a wide range of temperatures, from -25°C to 125°C. Data from this demonstration shows non-linear performance of the liquid metal interconnection while the assembly is transitioning below the liquid metal's freezing temperature. Further investigation of this phenomena would be important for integration into extreme environment applications.

The design, fabrication, and measurement work described in this dissertation document was performed by the author with the following exceptions. The first, passive liquid metal, flip chip assembly described in Figure 2.1 was designed and fabricated by a previous Virginia Tech graduate student, Joe Wood. MMICs used in these demonstration were provided by M/A-COM and Cobham. PolyStrata structures were fabricated and plated using the ENEPIG process at the Nuvotronics facility in Radford, VA. Post processing and assembly with the PolyStrata structures was performed by the author.

6.2 Future Work

This section discusses suggested future research directions and experiments which would further the development of liquid metal interconnections for wider use, in both commercial and military applications.

6.2.1 Verification of Liquid Metal Interconnects for Commercial and Military Assemblies

The work described in this dissertation includes initial experiments indicating the viability of liquid metal interconnections for production scale assemblies. It was shown that liquid metal RF and DC connections can be effectively integrated into heterogeneous, MMIC assemblies. Preliminary RF power handling and temperature cycling testing was performed with encouraging results. However, there are significant additional verification experiments that must be conducted before this style of level 1 IC packaging can assembly could be integrated into production commercial or military assemblies.

MIL-STD-883 details the standard tests that a packaged microelectronic device must undergo before it can be used within military and aerospace electronic systems, and is a good reference for future environmental testing that would need to be performed on devices with liquid metal interconnections. The following is a list of all the environmental testing specifications provided in this standard. Many of the tests specified on this table evaluate and verify the exterior packaging of a microelectronics device, the quality and reliability of the microelectronics' assembly, or the robustness of the packaged IC to failure testing. Tests that would subject interconnections to environmental stress have a brief description of their test standard. Therefore testing liquid metal interconnections to these standards will be a significant step in proving that pervasive use of liquid metal, flip chip interconnections is feasible.

Test Standard Number	**Test Standard Name**	**Description**
1001	Barometric pressure, reduced (altitude operation)	Test microelectronics assembly at reduced pressures; most extreme case the test pressure is set to 9.436×10^{-8}
1003	Insulation resistance	Tests exterior packaging of assembly
1004.7	Moisture resistance	Tests exterior packaging of assembly
1005.9	Steady state life	Tests the longevity of the microelectronics assembly; assemblies must survive 1000 hours of operation at an ambient temperature set at 125°C
1006	Intermittent life	Tests the microelectronics to abrupt on/off power cycling; assemblies must survive 1000 hours of operation at an ambient temperature set at 125°C with microelectronics powered off an on at a frequency specified by the microelectronic's application
1007	Agree life	Tests the microelectronics resistance to shock and vibration testing which simulates environmental conditions that the microelectronics would be subject to in its application, these conditions are specified under MIL-STD-781
1008.2	Stabilization bake	Exposes the microelectronics to high temperature, 150°C for 24 hours before the assembly is tested

1009.8	Salt atmosphere	Tests exterior packaging of assembly
1010.8	Temperature cycling	Tests the microelectronics to temperature cycling; a typical test condition, condition B, exposes the an assembly to temperature ranging from -155°C - 125°C
1011.9	Thermal shock	Tests the microelectronics to abrupt temperature changes, for condition B the assemblies temperature shall go from -155°C - 125°C in no more than 10 seconds.
1012.1	Thermal characteristics	Tests exterior packaging of assembly
1013	Dew point	Tests exterior packaging of assembly
1014.13	Seal	Tests exterior packaging of assembly
1015.10	Burn-in test	Tests the quality and reliability of the microelectronics assembly
1016.2	Life/reliability characterization tests	Tests the quality and reliability of the microelectronics assembly
1017.2	Neutron irradiation	Tests the robustness of the IC to environmental conditions
1018.6	Internal gas analysis	Tests the quality and reliability of the microelectronics assembly
1019.8	Ionizing radiation (total dose) test procedure	Tests the robustness of the IC to environmental conditions
1020.1	Dose rate induced latchup test procedure	Tests the robustness of the IC to environmental conditions
1021.3	Dose rate upset testing of digital microcircuits	Tests the robustness of the IC to environmental conditions

1022	Mosfet threshold voltage	Tests the robustness of the IC to environmental conditions
1023.3	Dose rate response of linear microcircuits	Tests the robustness of the IC to environmental conditions
1030.2	Preseal burn-in	Tests the quality and reliability of the microelectronics assembly
1031	Thin film corrosion test	Tests exterior packaging of assembly
1032.1	Package induced soft error test procedure	Tests the robustness of the IC to environmental conditions
1033	Endurance life test	Tests the robustness of the IC to environmental conditions
1034.1	Die penetrant test	Tests exterior packaging of assembly

Table 6.1: Table of MIL-STD-883 Environmental Test Standards

Preliminary temperature testing of liquid metal connections in this work suggests that liquid metal connections would survive temperature cycling and temperature shock testing. As mentioned in Section 5.2.4, more work needs to be done to evaluate the tensile properties of the Galinstan material in its solid state in order to understand the limitations of liquid metal to "cold start" conditions.

Galinstan has a very low vapor pressure, less than 10^{-8} Torr [62], which indicates that barometric testing will not likely cause failures in liquid metal interconnections, even in the most extreme pressure condition MIL-STD-883 outlines, 9.436 $\times 10^{-8}$ Torr.

Confirming the performance of liquid metal connections under shock and vibration conditions is important because shock and vibration conditions could pose potential problems for this non-rigid connection. During the testing presented in this dissertation, the high surface tension liquid metal was always sufficient to hold assemblies together, even when the

assembly was held upside down. However, during shock and vibration testing, significant changes in an assembly's inertia could disrupt the continuity of the electrical connection. If problems arise during shock and vibration testing, MMIC chips that are integrated into a larger electronic assembly with liquid metal connections may need some additional structural support for satisfactory shock and vibration performance.

Test standards which demonstrate the longevity of a connection under specific conditions (steady state life testing, intermittent life testing, and stabilization back testing) should be pursued after designing and building assemblies that have the highest likelihood of long term success. Specifically, fabricating ICs and assembly substrates with finishing metals which will not react to Galinstan liquid metal will be needed. As mentioned in Section 2.1.1 the gallium in Galinstan is a volatile metal which reacts with many other metals. However, there are several metals which gallium does not react with, such as nickel and tungsten. On the other hand, most top surface, finishing metals used on bond pads of ICs and assembly substrates are typically gold, silver, or copper [99]. Flip chip connections almost exclusively use gold for bond pad finishes because of gold's corrosion resistance and because it readily wets with the tin in solders. Gold surfaces were present on all assembly pin and bond pad contacts described in this dissertation, and while these assemblies performed satisfactorily, gold and gallium will react with one another and form intermetallics after prolonged, intimate exposure, especially at elevated temperatures [100]. Depleting the surface gold of a bond pad and having it diffuse into the eutectic liquid metal could degrade the conductivity of this bond pad and/or deteriorate the performance of the liquid metal (increase its melting point, increase the metal's resistivity, decreased wettablity to surfaces, etc.).

Nickel plating is already a well established process on ICs and various substrate materials because it is typically used as an intermediate metal between surface gold of a bond pad and the interconnect metal of many ICs in order to keep gold atoms from migrating into the semiconductor material [69]. Tungsten has also been integrated into IC processing and performs well as an IC contact metal because of its good adherence to semiconductor materials, its low CTE which matches well to that of the semiconductor substrates, low resistivity compared

to nickel, and the fact that it does not self diffuse into other materials [101]. Thus, altering MMIC and carrier processing to have nickel or tungsten surface metal for liquid metal, flip chip assemblies would not likely be a substantial process challenge, creating contacts which will not form intermetallics over time and provide reliable, long term performance.

6.2.2 Manufacturability of Liquid Metal Flip Chip Assemblies

All liquid metal assemblies described in this dissertation were fabricated in a research and development lab environment. Developing processing techniques for larger scale manufacturing is another essential step in making this type of interconnect a practical alternative to wirebonding or flip chip bonding. This section briefly discuss some of the challenges and opportunities that present themselves for large scale manufacturing of liquid metal interconnections in level 1 packaging environments.

Plating or Bumping Copper Pillars onto MMICs

As discussed in Section 2.3, the pin and socket configuration of liquid metal flip chip assemblies is more functional with the pin structure on the top, MMIC portion of the assembly. In this dissertation, plating these pins directly onto individual chips was attempted, but a consistent process was not achieved.

Despite the aforementioned setbacks, there are several other paths to successful "pins-on-chip" design. Plating copper pillars onto entire IC wafers is already a standard process for copper pillar bump, flip chip assemblies, and several MMIC foundries have begun adding copper post plating to their fabrication processes [15, 16, 102]. If a MMIC chip is not fabricated with copper pillars, stud bumping machines are capable of depositing posts on MMIC's bond pads. These posts are adhered to bond pads in the same way a thermosonic wirebonder bonds wire to bond pads, as described in Section 1.1.3 [1]. Stud bumping would allow for more custom assemblies to be fabricated without significant post processing of

MMICs.

Surface Finishing

As mentioned in the previous section, liquid metal interconnections which use Galinstan will need to have the surface of their pins and bond pads prepared with nickel or tungsten. Both materials are used in IC fabrication and both can be deposited on surfaces using an electroless plating process [69, 103]. Therefore these metals can be added to the surface of MMICs, either during wafer scale processing or as chip level process.

Injection of Liquid Metal Into Sockets

Integrating liquid metal into the bond pad sockets was carried out in this work using two different strategies; individual placement of frozen liquid metal into the sockets, as described in Section 2.2.2 or a squeegee process which selectively deposits liquid metal into all sockets. A pick and place strategy could easily be automated for fast transfer of frozen liquid metal into each socket of an assembly; there are may companies which already supply electronics manufacturers with similar machines for surface mount assembly.

A squeegee deposition process would deposit liquid metal into all sockets in parallel, making it a more manufacturable strategy for high interconnection or high volume assemblies. Squeegee deposition is readily used in many flip chip assembly processes for depositing solder bumps, as seen in Figure 1.8, therefore the development of this proposed process would not be a significant departure from current practice. Studies would need to be performed to understand forces required during stencil deposition, limitations stencil hole size, and surface preparation for squeegee deposition in order to cleanly and consistently deposit controllable volumes of liquid metal into sockets of varying sizes. Figure 6.1 shows a cross section of this proposed process.

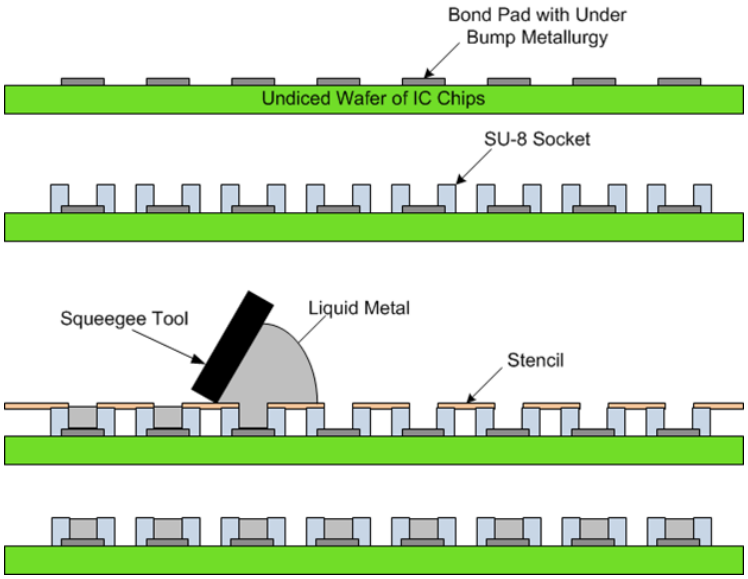

Figure 6.1: Cross sectional step depicting a squeegee process flow for depositing liquid metal.

6.3 Comparative Summary of Liquid Metal Interconnections to Typical Level 1 Packaging

In summary, Table 6.3 compares the figures of merit of liquid metal, flip chip designs to wirebond and solid flip chip designs, indicating the potential for liquid metal interconnections to resolve some of the issues faced by current flip chip technology, and enabling greater integration of heterogeneous technology for RF and microwave frequency applications.

Table 6.2: Comparison of liquid metal assemblies to wirebond and flip chip assemblies

	Wirebonding	**Solder Based Flip Chip**	**Liquid Metal Based Flip Chip**
Footprint	Size of MMIC plus the substrate bondpads; approximatly twice the size of the MMIC	Size of the MMIC	Size of the MMIC
Parasitics	High; on the order of 1nH of inductance and 1pF of capacitance	Low; on the order of 10pH of inductance and 10fF of capacitance	Moderate; initial modeling gives an inductance on the order 100pH and capacitance of 50pF. Better liquid metal contact would likely improve inductance values.
Thermo-mechanical Stress	Not an issue for wirebond connections	CTE mismatch can cause connection failures for heterogeneous assemblies	CTE mismatch can cause poor "cold start" performance when liquid metal is in the solid phase
Underfill	Not required	Underfill can alleviate some CTE mismatch stresses and increase reliability however dielectric constant of underfill must be taken into consideration during the design phase of the MMIC. Underfill will make the MMIC more lossy and effect the performance of planar transmission lines and on chip inductors.	Socket material can be selectively deposited at pad locations and MMIC design can account for the changes in dielectric constant at those locations.

Table 6.3: Comparison of liquid metal assemblies to wirebond and flip chip assemblies continued

	Wirebonding	**Solder Based Flip Chip**	**Liquid Metal Based Flip Chip**
Power limitations	Power limited to the size and number of wirebonds made per connection.	Limited by the electromigration phenomena and joule heating that can cause degradation and failure in a solder connection.	Has very good power properties, no known power limitations other than resistive heating limitations.
Preparation and Assembly	Bond pads prepared with soft, malleable surface finish. Wirebonds must be made one at a time during assembly, often requiring assembly heating.	Bond pads prepared with under bump metallurgy, including a gold surface finish, and solder is deposited and reflowed on one side of the connection. Solder reflow requires MMIC and substrate heating and makes all connections at once.	MMIC bond bad prepared with metal pillar and assembly surfaces are finished with nickel or tungsten. SU-8 patterned on substrate surface and liquid metal is inserted in sockets all at once with squeegee process or one at at time with a pick and place process. Assembly connected all at once, heat is not required.
Rework	Moderately difficult, requiring breaking and reapplying wirebonds, which is time consuming and requires skilled labor.	Very difficult, if underfill is used in assembly it is likely impossible. There are a limited number of times solder can reflow on bond pads.	Easy, assembly does not need to be reheated and connections can be made and broken many times.

Appendix A

Fabrication Steps for Specific Processes

A.1 Photolithography Recipe for AZ9214 Photoresist

The following process yields a $2\mu m$ thick layer, negative pattern of AZ9214.

1. Clean wafer; dip into hydrofloric acid (HF) for 15 seconds, then rinse in deionized (DI) water. On spinner, spray wafer 5 seconds with acetone, 5 seconds with methanol, followed by 5 seconds with isopropanol (IPA), then spin dry for 1 additional minute.
2. Bake at 120°C for 1 minutes to dehydrate.
3. Ensure that photoresist is at room temperature.
4. With wafer on spinner, pour photoresist in center of wafer to cover 1/3 of wafer.
5. Spin wafer at 2000 RPM for 35 seconds. Set acceleration to 20.
6. Soft bake for 65 seconds at 95°C.

7. Align in mask aligner and expose to 85 mJ/cm^2 of ultraviolet (UV) energy.
8. Post expose bake for 60 seconds at 115°C.
9. Flood expose to 1100 mJ/cm^2 of UV energy.
10. Develop for 40 seconds in 1 part AZ400K, 4 parts DI water.
11. Rinse wafer DI water and blow dry with nitrogen.

A.2 Photolithography Recipe for KMPR 1050

The following process yields a 50μm thick layer of patterned KMPR.

1. Ensure photoresist has reach room temperature.
2. Pour photoresist from bottle onto wafer, covering 1/3 of wafer.
3. Spin wafer 15 seconds at 500 RPM and 30 seconds at 3000 RPM.
4. Set wafer on hotplate, ramp hotplate to 65°C, at 65°C wait 3 minutes.
5. Ramp hotplate to 100°C, at 100°C wait 15 minutes.
6. Turn off hot plate and allow wafer to cool to room temperature.
7. Align in mask aligner and expose to 1000 mJ/cm^2 of UV energy.
8. Set wafer on hotplate, ramp hotplate to 65°C, at 65°C wait 1 minute.
9. Ramp hotplate to 100°C, at 100°C wait 4 minutes.
10. Turn off hot plate and allow wafer to cool to room temperature.
11. Develop in SU-8 developer for 6 minutes, for last 2 minutes of development use ultra sonic agitation.

12. Perform de-scum cycle in reactive ion etcher (RIE); 50W of ICP power for 1 minute in 10 sccm O_2.

A.3 Photolithography Recipe for SU-8 2050

The following process yields a $50\mu m$ thick layer of patterned SU-8.

1. Ensure photoresist has reach room temperature.
2. Pour photoresist from bottle onto wafer, covering 1/3 of wafer.
3. Spin wafer 15 seconds at 500 RPM and 30 seconds at 3000 RPM.
4. Set wafer on hotplate, ramp hotplate to 65°C, at 65°C wait 3 minutes.
5. Ramp hotplate to 100°C, at 100°C wait 8 minutes.
6. Turn off hot plate and allow wafer to cool to room temperature.
7. Align in mask aligner and expose to 300 mJ/cm^2 of UV energy.
8. Set wafer on hotplate, ramp hotplate to 65°C, at 65°C wait 1 minute.
9. Ramp hotplate to 100°C, at 100°C wait 6 minutes.
10. Turn off hot plate and allow wafer to cool to room temperature.
11. Develop in SU-8 developer for 6 minutes, for last 2 minutes of development use ultra sonic agitation.

A.4 Photolithography Recipe for AZ9260

The following process yields a $6\mu m$ thick layer of patterned AZ9260.

1. Ensure that photoresist is at room temperature.
2. With wafer on spinner, pour photoresist in center of wafer to cover 1/3 of wafer.
3. Spin wafer 15 seconds at 500 RPM and 60 seconds at 2000 RPM.
4. Allow wafer to sit for 15 minutes.
5. Soft bake for 3minutes at 110°C.
6. Align in mask aligner and expose to 600 mJ/cm^2 of UV energy.
7. Allow wafer to rest for several minutes.
8. Develop for 85 seconds in 1 part AZ400K, 3 parts DI water.
9. Rinse wafer DI water and blow dry with nitrogen.

A.5 Recipe for TMAH Wet Etching

1. Pour 25% TMAH solution into a large beaker.
2. Heat solution on hotplate to 90°C.
3. Agitate solution with stir bar set to spin at least 250 RPM.
4. Immerse wafer into solution. Ensure good flow reaches the surface to be etched.
5. Wait desired time based on 0.5μm/minute etch rate.
6. Rinse sample in DI water.

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