CCM Totem-Pole Bridgeless PFC with Ultra-Fast IGBT

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(ABSTRACT)

The totem pole PFC suffers from the Mosfet body diode reverse recovery issue which limits this topology adopted in the CCM high power condition. As the ultra-fast IGBT which is capable of providing 100 kHz switching frequency is available in the market, it is possible to apply the totem pole PFC in CCM high power condition. The thesis provides a method by implementing the ultra-fast IGBT and SiC diode to replace the MOSFET in this topology.

To verify the method, a universal 1.5kW CCM totem pole PFC is designed and tested. The design adopts the ADP1048 programmable digital PFC controller by adding external logic gate for totem-pole PFC. ADP1048 greatly simplifies the design process and satisfies the design requirements. The experiment results verify that the totem-pole PFC can be applied into CCM high power condition by using the method. The DC output voltage is well regulated. The power factor is higher than 0.98 when the load is above 400W. The measured efficiency can achieve up to 96.7% at low line and 98.2% at high line condition with switching frequency 80 kHz.

Keywords: Totem Pole PFC, ADP1048, Ultra-fast IGBT, CCM

To my Parents
Mingxue Zhou and Min Wang

To my wife
Zheng Zhao

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Chapter 1:
Introduction

1.1 Background and Research Objective

Power factor correction technology is an essential part of power electronic products to meet environmental protection requirements. With all types of electrical appliances drawing power from the grid and more and more stringent power quality norms required by international organizations, power factor correction has become the focus of the development of the power electronics industry. If the input current to the grid has a displacement and large harmonic distortion, it will result in low power factor. The low power factor will cause the energy wasted. The distorted current will cause harmonic and pollute the grid. On one hand, the current flowing through the line impedance causes a voltage drop, which in turn makes the grid distortion occurred; on the other hand, it has an harmful impact on the other electrical equipment connecting to the grid, such as instrument measurement error, protection equipment malfunction, lines and distribution transformers overheating etc. The main design target of implementing power factor correction in the power supplies is to meet the international standards for power factor and harmonic content requirements. For example, some countries impose EN61000-3-2 standards [1-5].

With the development of PFC technology and semiconductor technology, how to improve the PFC efficiency has become a hot topic. For a conventional boost PFC, the loss in the rectifier bridge is significant especially in low voltage high current case [6-12].

In order to reduce the conduction losses in the rectifier bridge, some bridgeless PFC topologies are proposed. For high-power bridgeless PFC, how to improve the efficiency and reduce the size, cost, ease of design is the direction for the designers.

Compared with semi-bridgeless Boost PFC, totem-pole PFC has fewer components, more efficient advantages. However, due to the internal MOSFET body diode reverse recovery problems, the totem-pole PFC is not applicable in CCM high power applications [8][13-16]. In the past, the limited switching frequency of IGBT results in it is not realistic to use IGBT in totem-pole PFC. However in nowadays, with advanced semiconductor technologies, there have been IGBTs which can be switched more than 100 kHz, such as Infineon's ultra-fast IGBT [17-19]. With the fast IGBT appearance, it is possible to apply CCM totem-pole PFC in high power condition. Thus research of how to apply fast IGBT and SiC diode in totem-pole PFC also provides an alternation for high-power bridgeless PFC application.

In addition, how to choose the controller chip that is easy to implement and can shorten the product design cycle is also one of the important factors engineers take into consideration. As the first digital programmable PFC chip, ADP1048 meets the needs of PFC design [40]. ADP1048 can convert all signals to the digital domain and allow the adjustment of one PMBUS through the interface and the report all the parameters, including accurate measurement of the input voltage, current and power. Compared with DSP, ADP1048 is less expensive and easier to use. ADP1048 also provides an intuitive graphical user interface (GUI), which help designers optimize PFC systems without the need of programming and compiling the complex code in DSP. This is also helpful in avoiding the code verification time in industry. However, bridgeless PFC mode in

ADP1048 is designed for semi-bridgeless boost bridgeless PFC, some external circuits are required to apply it in totem-pole PFC topology. Based on the above discussion, it is very interesting and promising to apply ADP1048 in totem pole PFC design.

1.2 Thesis Outline

The thesis focuses on designing a universal CCM high power totem pole PFC by implementing ADP1048 programmable digital PFC controller. Chapter 1 introduces the research background and motivation. Chapter 2 reviews different bridgeless boost PFC topologies and control methodologies. Chapter 3 discusses the method for applying the totem pole PFC in CCM high power condition and analyzes the operation modes and simulates it in PSIM. Chapter 4 describes the design process of the power stage component selection and ADP1048 control setting. Chapter 5 shows the experiment results, including efficiency and THD. Chapter 6 presents the summary of this work and outlooks the future work.

Chapter 2:

Power Factor Correction

2.1 Power Factor Definition

In electrical area, the power factor is defined as the utilization rate of the power from grid. It is the ratio of real power (P) to the apparent power ($|S|$).

$$PF = \frac{Real\ Power}{Apparent\ Power} \tag{2.1}$$

The power factor equation can be shown in **Figure 2.1**:

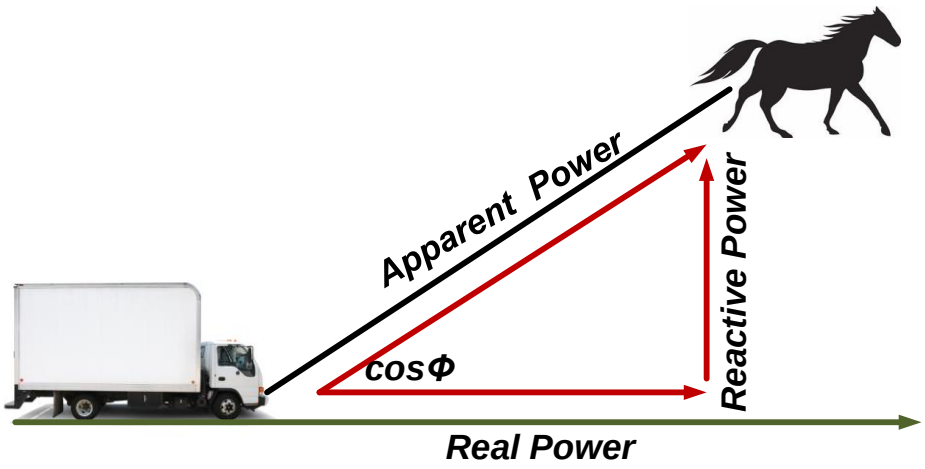


Figure 2.1 Illustration of Power Factor

If the voltage and current are ideal sinusoidal waveform, the PF=cosϕ. But for the sinusoidal voltage and non-sinusoidal current, the PF should be equal to:

$$PF = \frac{V_{rms} \cdot I_{rms\_1}}{V_{rms} \cdot I_{rms}} \cdot \cos\phi = K_d \cdot \cos\phi \tag{2.2}$$

K_d is the ratio of the fundamental of line current RMS value to the total line current RMS value.

$$K_d = \frac{I_{rms\_1}}{\sqrt{I^2_{rms\_1} + I^2_{rms\_2} + ... + I^2_{rms\_n}}} \tag{2.3}$$

n is the nth order of harmonic current.

Define the total harmonic distortion (THD) as:

$$THD = \frac{I_h}{I_{rms\_1}} = \frac{\sqrt{I^2_{rms\_2} + I^2_{rms\_3} + ... + I^2_{rms\_n}}}{I_{rms\_1}} \tag{2.4}$$

I_h is the sum of total harmonic current RMS values.

Thus the distortion factor K_d equals to:

$$K_d = \frac{1}{\sqrt{1 + THD^2}} \tag{2.5}$$

The power factor can be represented as:

$$PF = \frac{\cos\phi}{\sqrt{1 + THD^2}} \tag{2.6}$$

From the power factor expression, the reasons leading to poor power factor are line current has large amount of high order harmonic and the different phase between input voltage and current. Therefore, to improve the power factor, the line current should keep the same phase with the sinusoidal line voltage and attenuate the line current harmonics [20].

2.2 Active Power Factor Correction Control Methods

The active power factor correction (APFC) uses active switch device associating with passive component to shape the input current waveform and control the output voltage. Proper control method can make the power factor approximated to unity PF [20].

The APFC always adopts boost, buck, buck-boost, Cuk, sepic or flyback topologies based on the inductor and switch positions in the circuit [20]. Boost converter as shown in

Figure 2.2 is the most popular topology for PFC application. The boost inductor is in series with the input line terminal which is easy to implement average current control and achieve smaller current ripple. The switch in boost PFC is not floating, which is another benefit that makes the driver circuit easy to design. The boost PFC also has low current stress [2-24].

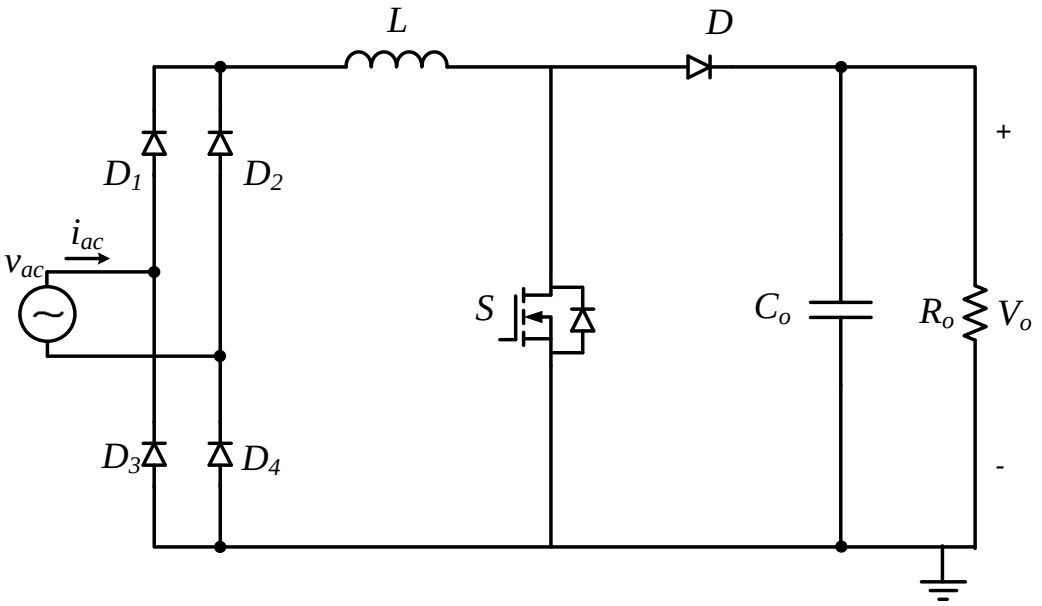


Figure 2.2 Traditional Boost PFC Topology

Based on the different PFC power level, the active PFC operation mode can be categorized as DCM (Discontinued Current Mode), CRM (Critical Conduction Mode) and CCM (Continuous Current Mode). The DCM PFC adopts voltage follower control method which has simple control circuit (only one voltage loop) and the inductor is working at DCM making the boost diode avoid the reverse recovery problem. But the DCM current is discontinuous, so the input needs bigger size filter and switch current RMS value is higher than CCM which increases the switch conduction loss. The DCM is only suitable for low power level condition. Because the inductor current is continuous, the CCM control is suitable for high power level. The CCM control method, including the Hysteresis Current Control, Peak Current Control, Average Current Control, is based on the multiplier approach control theory [25-30].

2.2.1 Peak Current Control Method

The peak current control scheme is shown in Figure 2.3. The current reference is generated from the output of the voltage loop error amplifier multiplying the rectifier input voltage. The switch is turned on keeping steps with the constant clock trigger and is turned off when the sensing switch current touches the current reference.

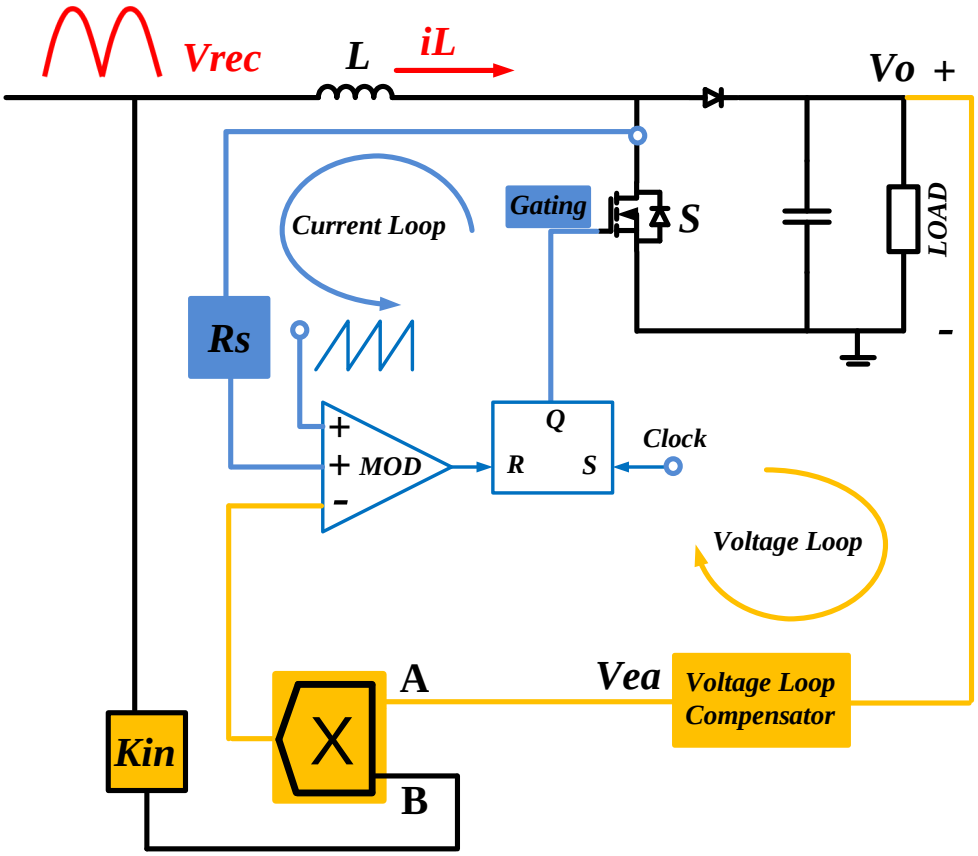


Figure 2.3 Peak Current Mode Control Scheme

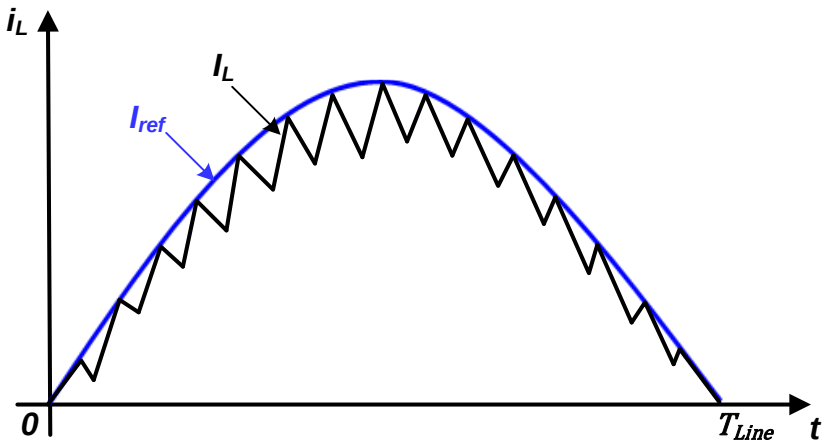


Figure 2.4 Peak Current Mode Control Waveform

When the inductor current rising slope Sn is higher than falling slope which means the duty D<0.5, the current perturbation will decay after several switching cycles.

When the inductor current rising slope Sn is lower than falling slope which means the duty D>0.5, the current perturbation will grows and the system will lose stability [23]. The constant frequency peak current mode inherited instability issue is shown in Figure 2.5.

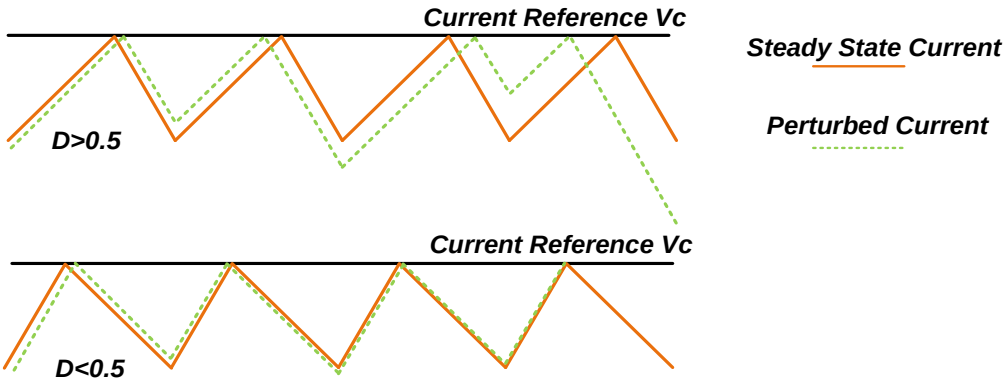


Figure 2.5 Peak Current Mode Control Current Perturbation

An external ramp is needed to add for keeping the system stable when the D>0.5. But adding external ramp increase the difficulty of design. The peak current control is simple for design but the disadvantages are the current loop gain is low at low frequency, current THD is higher than average current control and the sub-harmonic issue is serious even with the external ramp. The disadvantages of the peak current mode control limit the application in CCM control method.

2.2.2 Hysteresis Current Control Method

The hysteresis current control scheme is shown in Figure 2.6. There are two current references: upper limit threshold I_{ref_up} and lower limit threshold I_{ref_down}. When the current touches the lower threshold current reference, the switch is turned on and inductor current will increase. When the current touches the upper threshold current

reference, the switch is turned off and current will decrease. The current is limited in the hysteresis band and the power switch gating signal is depended on the two current references.

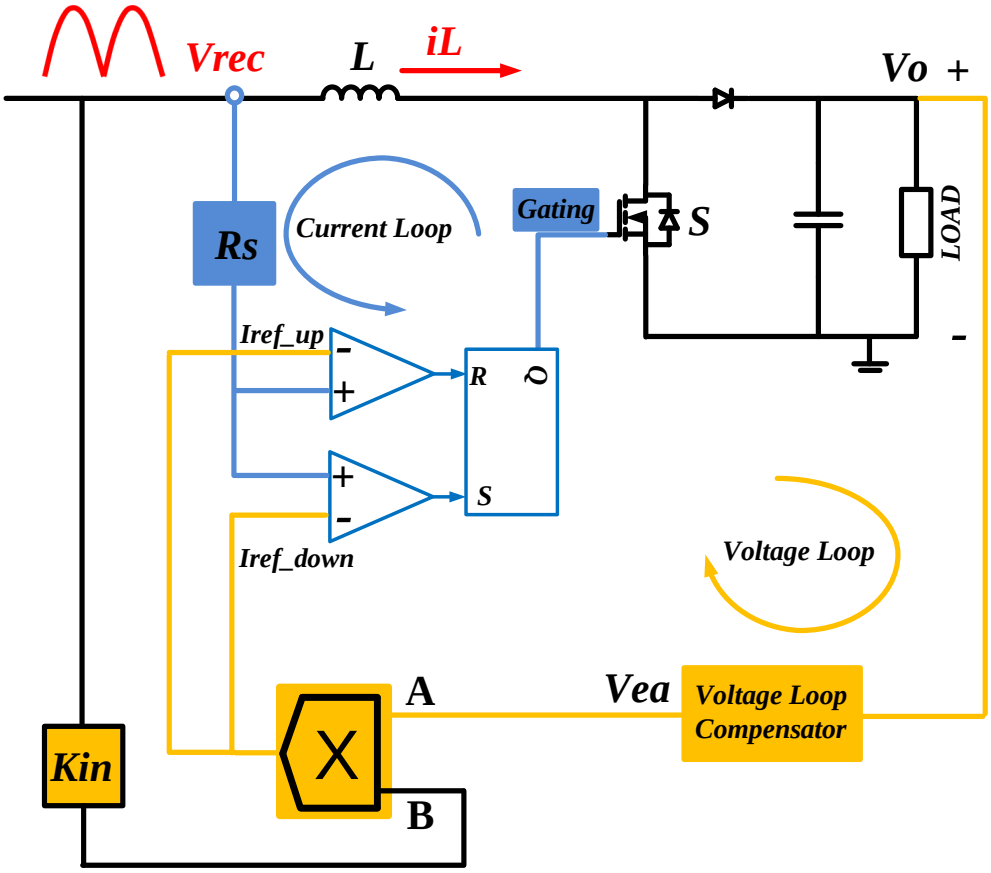


Figure 2.6 Hysteresis Current Mode Control Scheme

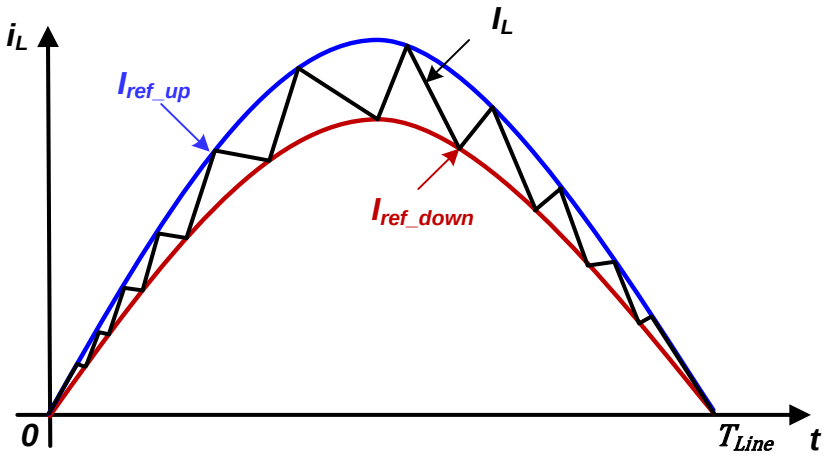


Figure 2.7 Hysteresis Current Mode Control Waveform

The hysteresis current method can control the hysteresis band range to decrease the inductor current ripple. But in this method, switching frequency is variable and the load impact the switching frequency great causing the filter circuit difficult to design.

2.2.3 Average Current Control Method

The average current control scheme is shown in Figure 2.8. The controller multiplies the sensed input voltage with the power reference generated from the output of voltage loop compensator, and divided by the square of input voltage RMS value to get the input current reference. The current error amplifier compensates the error between sensed current and current reference. The output of the current compensator drives the PWM modulator to generate the gating signals for helping line current to track the input voltage waveform and get the desired output voltage.

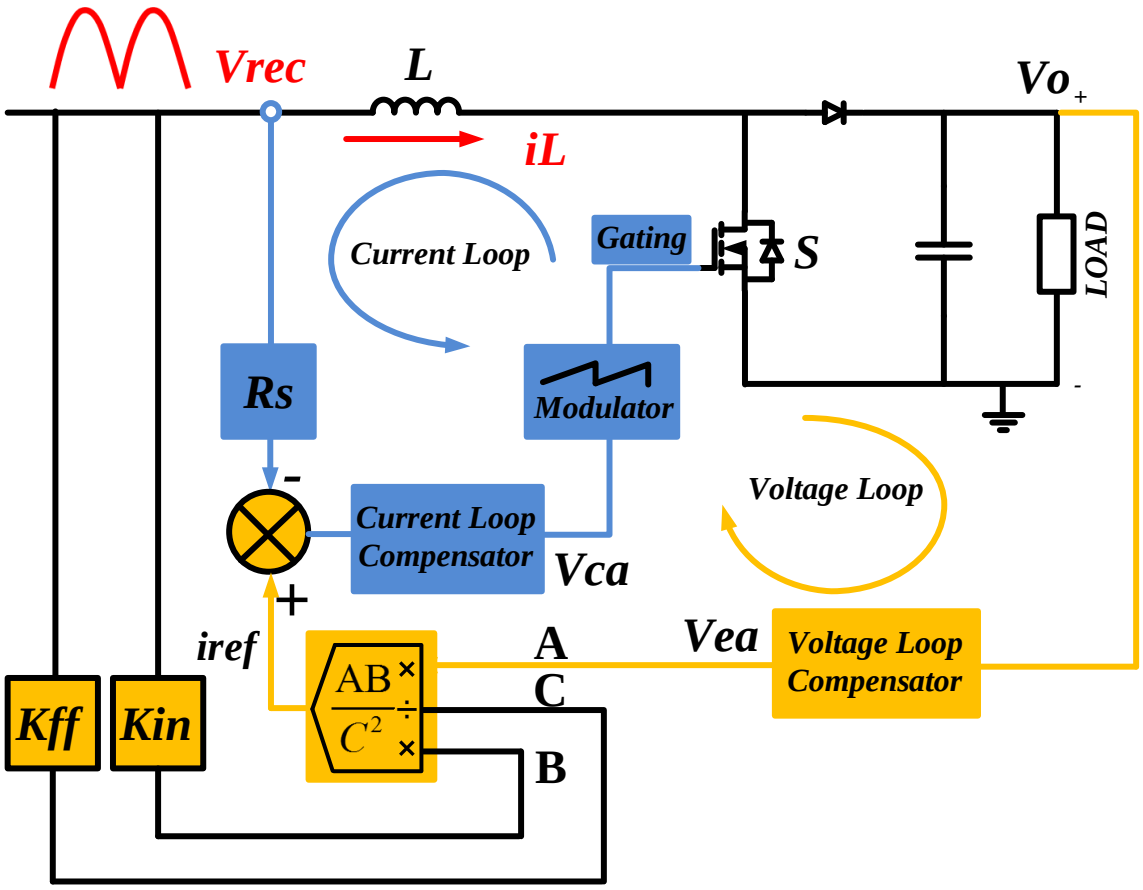


Figure 2.8 Average Current Mode Control Scheme

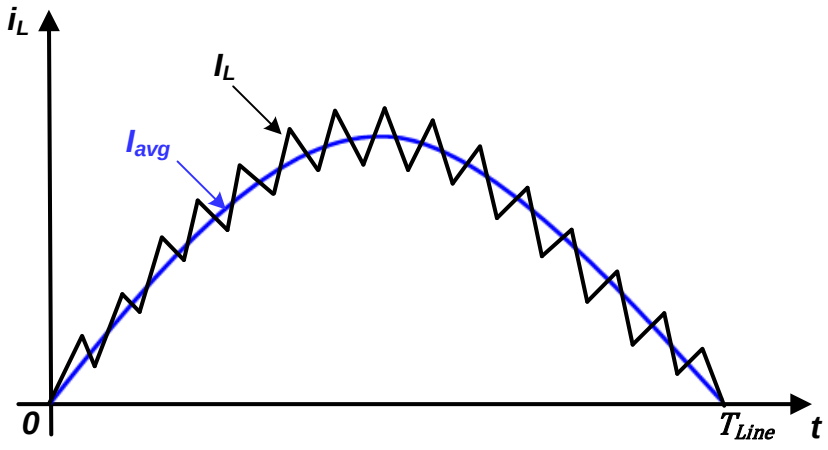


Figure 2.9 Average Current Mode Control Scheme

The average current control is most widely used method for boost PFC converter especially in high power level. It can achieve low THD, accuracy current tracking and low EMI.

2.3 Bridgeless Boost PFC Topology Overview

The electronics devices such as laptops, cell phone, panel computer, workstations, and data severs increasingly challenge AC/DC power supplies for higher efficiency requirements. The environment organization and government regulations are forcing designers to look for any possible opportunity to minimize power losses [31-32]. Although the conventional boost PFC is the most popular topology among the AC/DC converter, the conduction loss from line bridge rectifier is significant and limits to enhance the efficiency of the whole circuit. To solve this problem, Bridgeless Boost PFC is proposed and attracts wide range attention. It is effective to reduce the number of devices on the current path to reduce considerable conduction loss and improve the total efficiency. Generally, the bridgeless PFC can cut down the number of devices and improve the efficiency and power density [7-12].

So far, many boost bridgeless topologies have been proposed. Researches on bridgeless topologies become to a hot spot in power electronic area. In this section, some simple and usually implemented structures are reviewed.

2.3.1 Traditional Boost Bridgeless PFC

The configuration of traditional boost bridgeless PFC is shown in Figure 2.10. The current only flows through two semiconductor devices at every moment, whereas the number for traditional boost PFC shown in

Figure 2.2 is three. The power switch MOSFET instinct body diodes are used to replace two slow diodes and provide the return path. The topology is not only beneficial in reducing the number of semiconductor devices in the whole circuit and conduction loss, but also solves the heat dissipation of the input rectifier bridge problem.

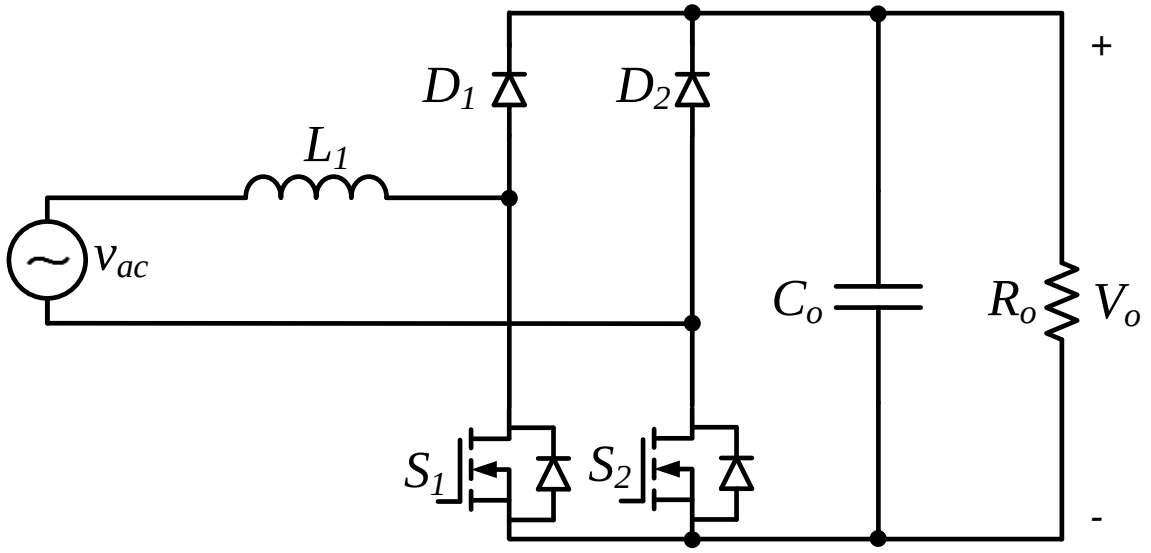


Figure 2.10 Dual Boost Bridgeless PFC Topology

However, the implementation of traditional boost bridgeless PFC is limited by the high common-mode noise problem which caused by the high frequency switches S_1 and S_2.

In the traditional boost PFC, the output ground is always connected to the input ac source through the input rectifier bridge whenever the positive or negative half-line cycle.

For the traditional boost bridgeless PFC, during the positive half-line cycle, the output ground is always connected to the ac source through the power switch S_2 body diode, but during the negative half-line cycle, the output ground has high frequency pulsating and the amplitude is equal to output voltage. This high frequency pulsating voltage source charge and discharge the equivalent parasitic capacitance between the output ground and the ac line, causing a significantly increased common-mode noise. To solve the serious common mode noise, a larger EMI filter is needed. The inherent drawback of the traditional boost bridgeless topology limits the implementations for the PFC design.

2.3.2 Semi-Bridgeless Boost PFC

To reduce the high common-mode noise, the semi-boost bridgeless PFC is modified by adding two slow diodes and second inductor to supply a LF path between the output ground and ac source. This derivative topology is presented in Figure 2.11.

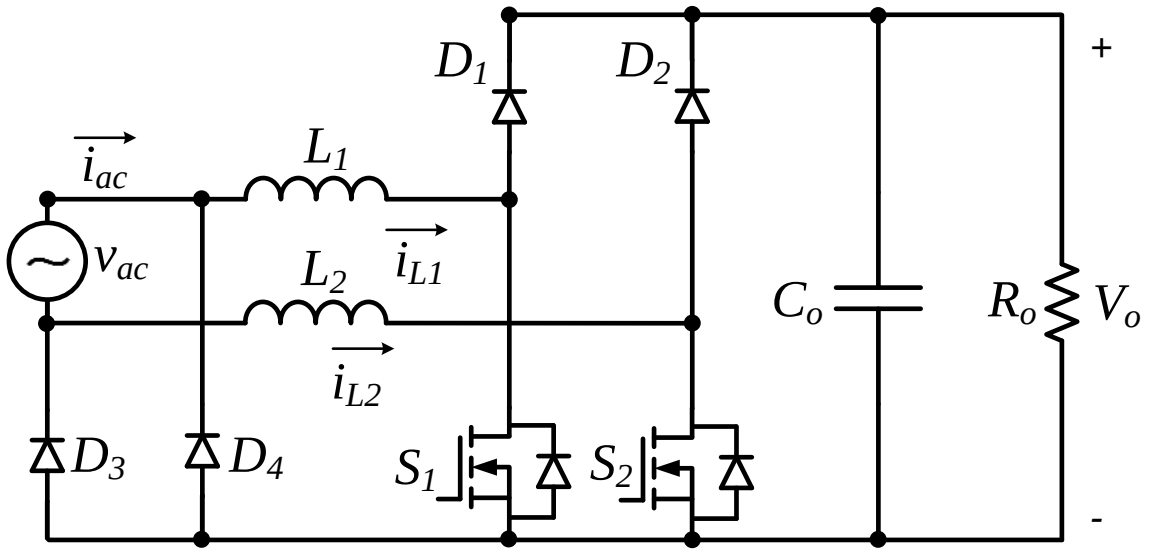


Figure 2.11 Semi-Boost Bridgeless PFC

This topology consists of two DC/DC boost converter. During the positive half-line cycle, the output ground is connected to the ac source through the slow diode D3. During the negative half-line cycle, the output ground is connecting to the ac source through the slow diode D_4. The symmetric inductors also can be expected as a common-mode filter to reduce the common-mode. This topology can achieve the common-mode noise as the same level as the traditional boost PFC. However, the major drawback of this topology is low components utilized rate and high cost of the design product.

2.3.3 Dual Boost Bridgeless PFC with Bidirectional Switch

Another modified topology based on the basic bridgeless PFC is shown in Figure 2.12. This topology can also survive from the common-mode noise problem by adding two diodes. During the positive half-line cycle, the output ground is connected to the ac source through the diode D_4. During the negative half-line cycle, the positive output bus is connected to the ac source through the diode D_1. So the output voltage is no longer in a floating status.

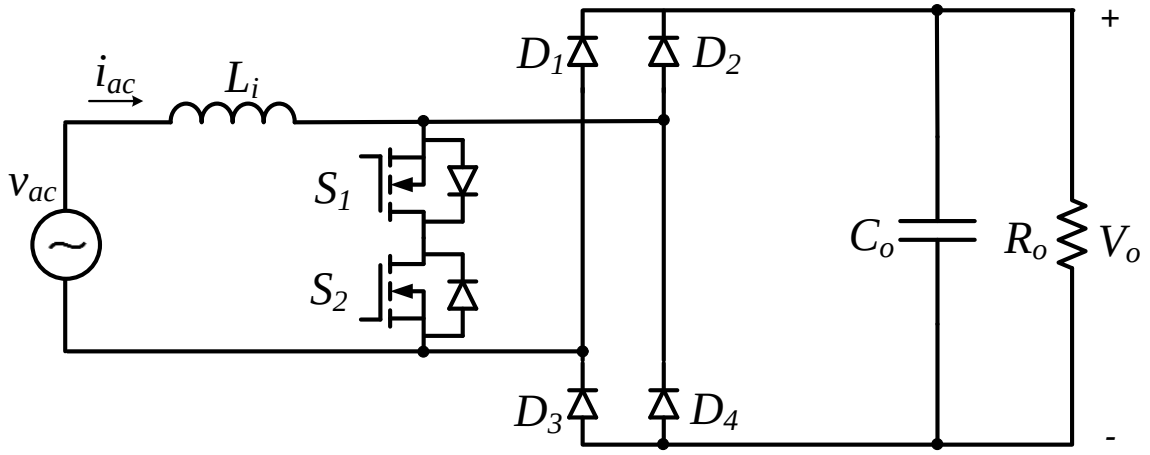


Figure 2.12 Dual Boost Bridgeless PFC with bidirectional switch

The major drawback of the topology is that the gate voltage for each switch is different and requires isolated gate drive transformer which makes the drive circuit design difficult. Besides when the switch is off, the current flows through two high frequency diodes which increase the conduction loss significantly.

2.3.4 Pseudo Totem-Pole Bridgeless PFC Topology

Figure 2.13 presents another variation topology of dual boost bridgeless PFC. Based on the location of two switches, this topology is named as pseudo totem-pole bridgeless PFC. This topology does not suffer from the common-mode noise problem as does the basic bridgeless boost PFC.

During the positive half-line cycle, the output ground is connected to the ac source through the slow diode D_3. During the negative half-line cycle, the output voltage bus connects to the ac source through the slow diode D_4.

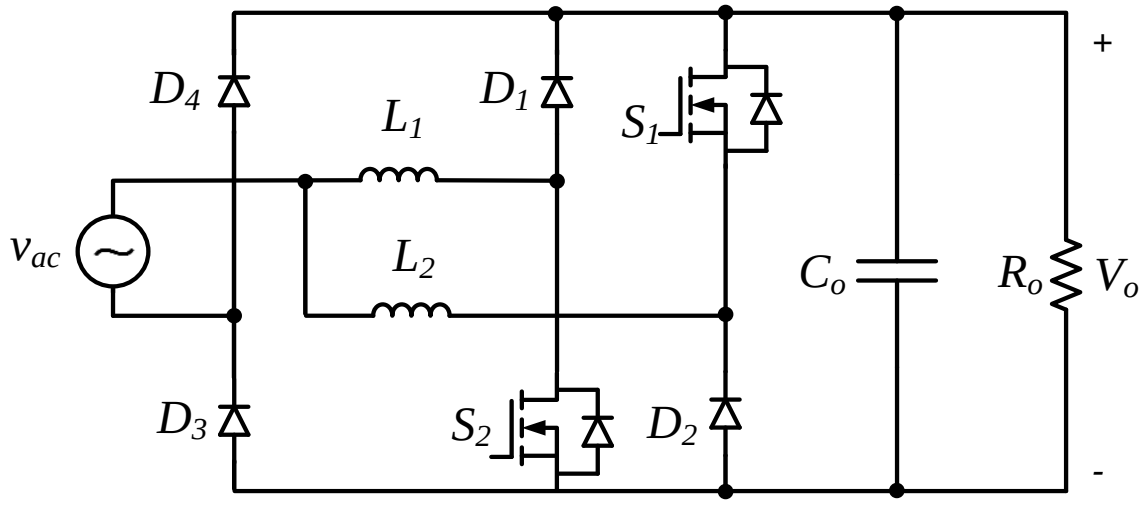


Figure 2.13 Pseudo Totem-Pole Bridgeless PFC Topology

The two switches need to be driven with different PWM signals and isolated gate drivers. This topology practical implementation is also limited by the difficult control and driver circuit design.

2.3.5 Totem-Pole Bridgeless Boost PFC Topology

The topologies shown in above either have the common-mode noise problems or have to add the extra components to reduce the common mode noise. Compared with these topologies, the totem-pole Bridgeless PFC shown in Figure 2.14 seems attractive for implementation, because it has the advantage of the simple structure and lowest components cost same as the basic bridgeless PFC, but also does not create large common-mode noise.

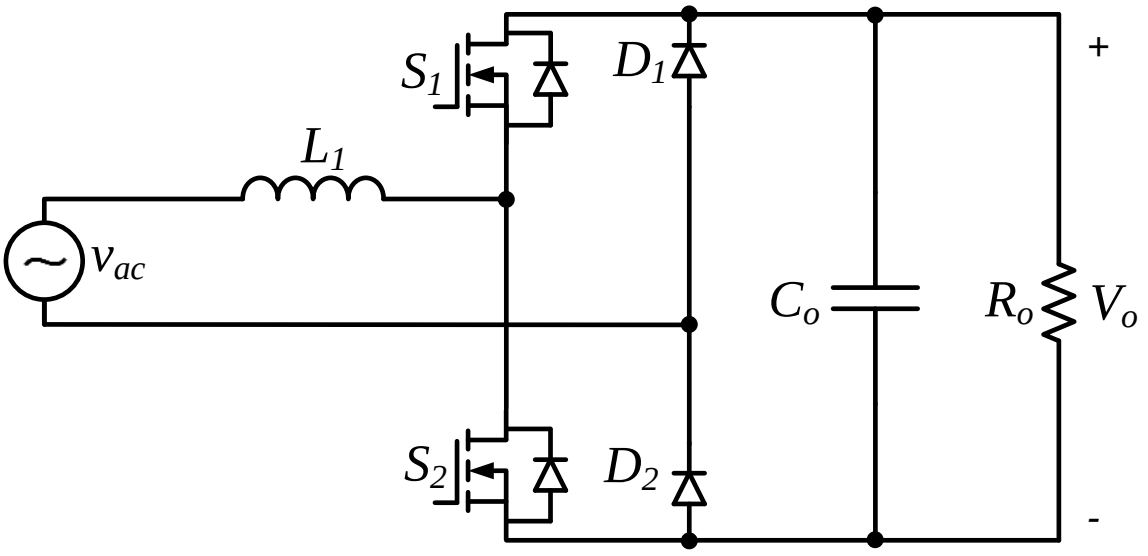


Figure 2.14 Totem-Pole Bridgeless Boost PFC Topology

The totem-pole PFC successfully suppresses the common-mode noise by changing the semiconductors positions of the basic bridgeless boost PFC shown in Figure 2.10. During in the positive half-line cycle, the output ground is connected the ac source

through the D_2, and during the negative half-line cycle, the positive terminal of the output voltage is connected the ac source through the D_1.

Although the totem-pole PFC has more advantages than other topologies, it has not attracted widespread implementation in practical. Because the slow recovery body diode of the MOSFET make the totem-pole PFC only suitable for Discontinuous Current Mode(DCM) or Critical Mode operation. The body diodes of the switches in the totem-pole PFC play the same effect as the traditional boost PFC fast-recovery diode. For example, as shown in Figure 2.15, in CCM operation mode, during switch S_2 off, the switch S_2 body diode works as the fast diode and provide a current path for the input current. At the moment of the switch S_2 is turning on, the current through the switch S1 include the input current and the S_1 body diode's reverse recovery current. This phenomenon will cause the severely high losses and even make device damaged by the potential overshoot issue.

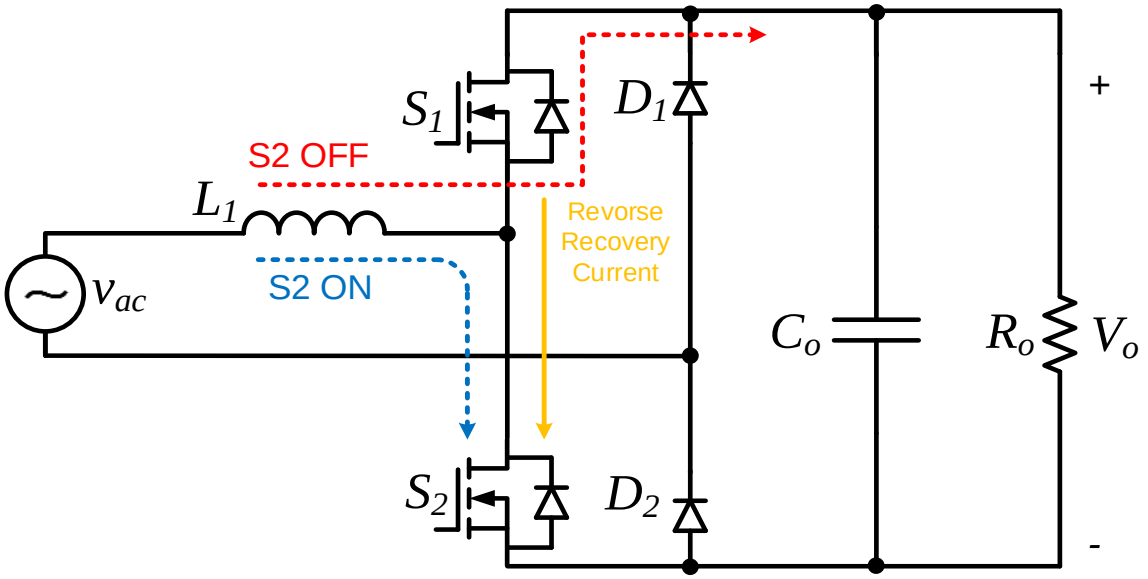


Figure 2.15 Reverse Recovery Issue in Totem-pole PFC

Therefore, the instinct issue makes the totem-pole PFC applications with mosfet switch limited with the DCM or Critical Mode operation. Some ZVS control methods are proposed to reduce the reverse recovery of the diode, but extra components need to be added to achieve the CCM operation mode. Besides the cost increase, the power range, complicated current sense and control are other drawbacks for these soft-switching methods.

IGBT parallels with a *SiC* diode can replace the MOSFET in the totem-pole, and the *SiC* diode does not have the reverse recovery issue. This method is workable in theoretically, but it is impractically by considering the conventional IGBT working frequency is usually around 30 kHz [33]. Under this frequency, the size of inductor is huge and the power density decreases. So the conventional IGBT used in totem-pole PFC is also impractical. In general, although the totem-pole PFC has the apparent advantages, the conventional switches characteristic cannot make the topology accepted in wide range.

2.3.6 Bridgeless PFC topologies comparison

Table 2.1 shows the number of components, CM noises, and applicable operation mode comparison during these bridgeless PFC topologies.

Table 2.1 Comparisons of different bridgeless PFC topologies.

Topology	Traditional Boost PFC	Traditional BLPFC	Semi-Boost BLPFC	Bidirectional BLPFC	Pseudo BLPFC	Totem-pole BLPFC
Switches	1	2	2	2	2	2
Slow Diode	4	0	2	0	2	2
Fast Diode	1	2	2	4	2	0
Freewheeling diode	0	2	2	2	2	2
Input Inductor	1	1	2	1	2	1
Output Cap	1	1	1	1	1	1
Total Number	8	8	11	10	11	8
Driver Circuit	Easy	Easy	Easy	Complex	Complex	Complex
CM Noise	Small	Large	Small	Small	Small	Small
Operation Mode	CCM DCM CRM	CCM DCM CRM	CCM DCM CRM	CCM DCM CRM	CCM DCM CRM	DCM CRM

Chapter 3:

A Method for CCM Totem-Pole PFC

3.1 Ultra-Fast IGBT Implemented in CCM Totem-Pole PFC

3.1.1 Ultra-Fast IGBT Introduction

The conventional IGBTs are usually adopted in low switching frequency and high current applications. As the requirement of higher switching frequency in power converter field, the application range of IGBT is limited. However, the IGBT technology achieves extraordinary progress recently. Such as Infineon, it launched the breakthrough technology called as TRENCHSTOP 5 and released the H5/F5 ultra-fast IGBT with switching frequency up to 100 kHz [33]. The TRENCHSTOP IGBT technology achieves the high switching speed while remaining the IGBT intrinsic features such as low conduction loss, high voltage rate, high current density, low cost [34-35]. The new generation ultra-fast IGBT has the high possibility of replacing the MOSFET in high frequency and high power switch power supply applications.

3.1.2 Ultra-fast IGBT and *SiC* Diode in Totem-pole PFC

The totem-pole PFC with MOSFET is not workable in CCM operation because of the MOSFETs' instinct body diode reverse recovery. The combination of ultra-fast IGBTs and *SiC* diode replacing the MOSFET in the totem-pole PFC makes the topology possible to be used in CCM operation, because the ultra-fast IGBTs are capable of

switching above 100 kHz and the *SiC* diode can provide the current path when switch IGBT is off without the reverse recovery current. This method will be verified in experiments in later Chapter 5.

3.2 Totem-Pole PFC Circuit Structure

The totem-pole PFC based on the ultra-fast IGBT diagram is shown in Figure 3.1. The ultra-fast IGBTs offer the high efficiency in hard switching, low Q_g, low conduction loss and high switching frequency. The characteristics of the ultra-fast IGBTs and *SiC* diodes enable the high switching frequency PFC under CCM operation. The totem-pole PFC based on the ultra-fast IGBT diagrams are shown in Figure 3.1.

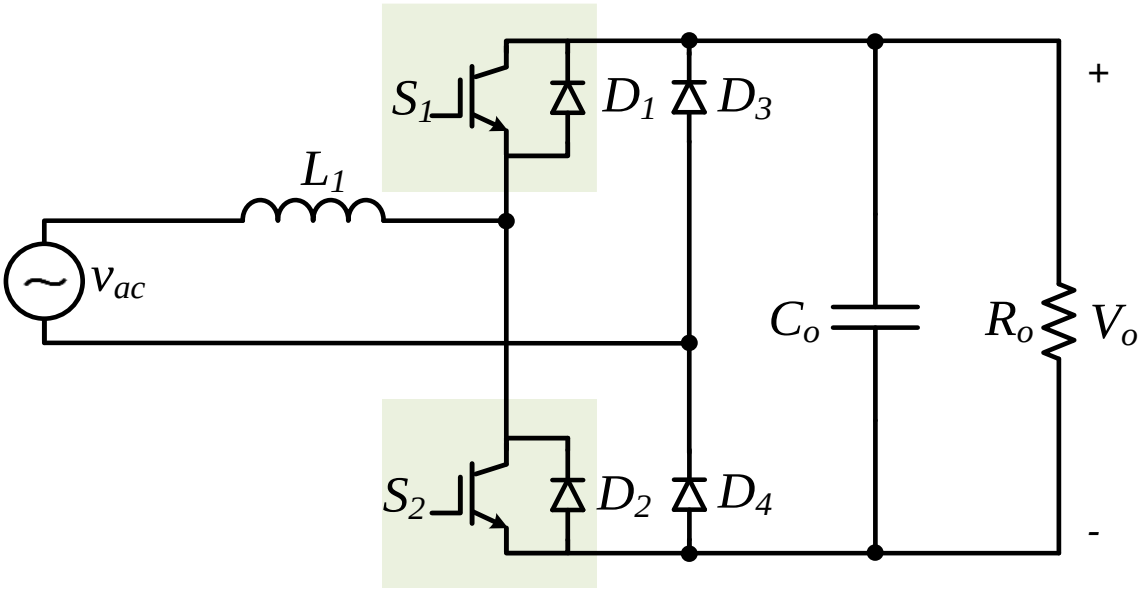


Figure 3.1 Totem-pole PFC with ultra-fast IGBT and Diode Line Rectification

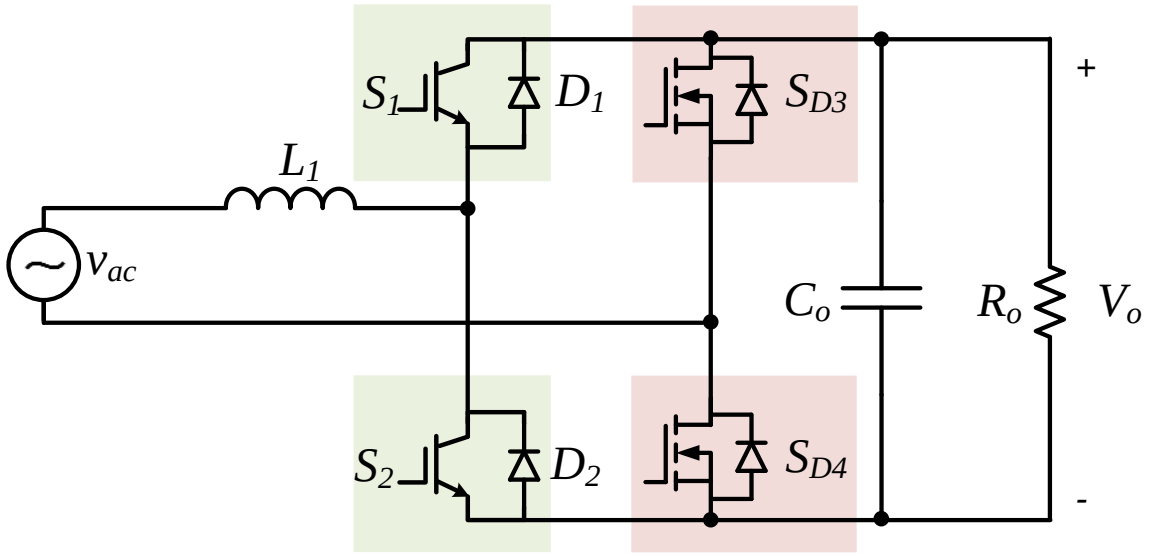


Figure 3.2 Totem-pole PFC with ultra-fast IGBT and MOSFET Line Rectification

Figure 3.1 includes two slow diodes D_3 and D_4 which are used for line rectification. For further boosting the efficiency, the line rectification diode can be replaced by the low R_{dson} MOSFETs. Figure 3.2 diagram shows the totem-pole PFC with MOSFET line rectification. The new topology only replaces the line rectifiers D_3 and D_4 with MOSFETs S_{D3} and S_{D4} which are controlled by two additional PWM signals synchronizing with the half line cycle.

3.3 Operation Mode Analysis

3.3.1 Positive Half Line Cycle Operation

The positive half line cycle operation of the totem-pole PFC is shown in Figure 3.3 and Figure 3.4. There are only two semiconductors in the current path. When the switch S_2 is on, the ac source charges the inductor L_1 and the output capacitor supplies the energy for load. The MOFET S_{D4} is conducting current and connecting the ac source to the output ground.

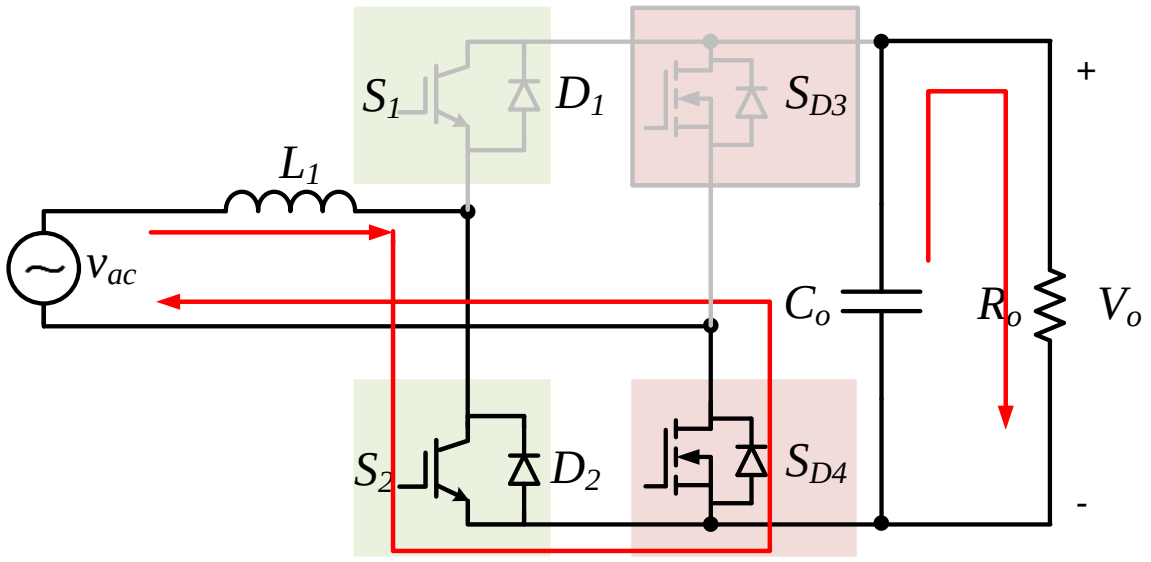


Figure 3.3 Totem-pole PFC Positive line cycle when switch is ON

When the switch S_2 is off, the inductor L_1 discharges the energy to the output and the *SiC* D_1 freewheels the inductor current. The Mosfet S_{D4} is conducting current and connecting the ac source to the output ground.

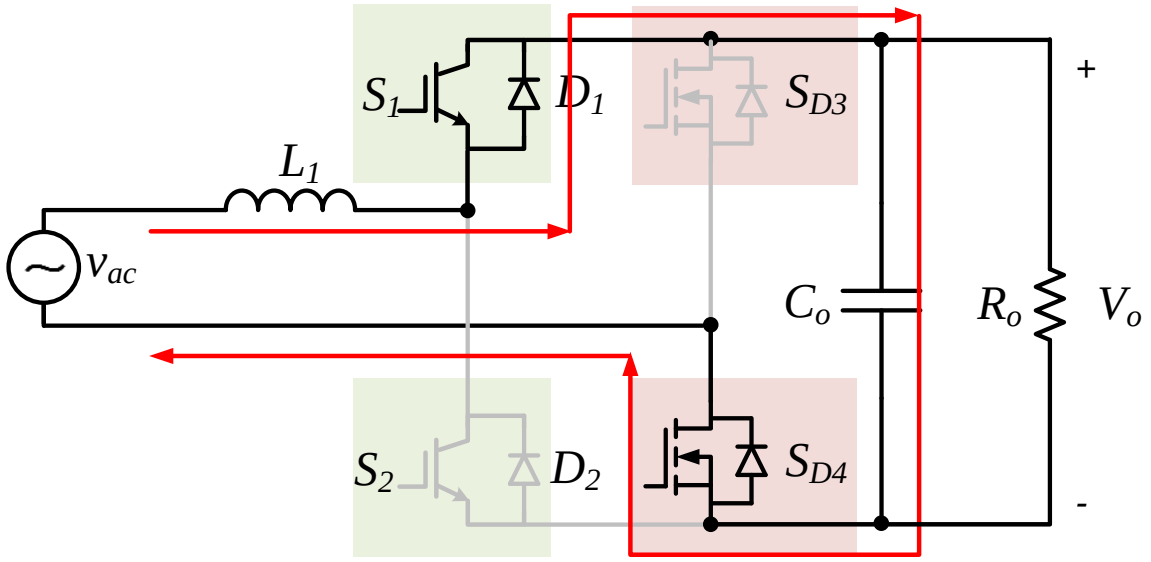


Figure 3.4 Totem-pole PFC Positive line cycle when switch is OFF

3.3.2 Negative Half Line Cycle Operation

The negative half line cycle operation of the totem-pole PFC is shown in Figure 3.5 and Figure 3.6. There are only two semiconductors in the current path. Similarly to the positive half line cycle, when the switch S_1 is on, the ac source charges the inductor L_1 and the output capacitor supplies the energy for load. The MOSFET S_{D3} is conducting current and connecting the ac source to the positive terminal output.

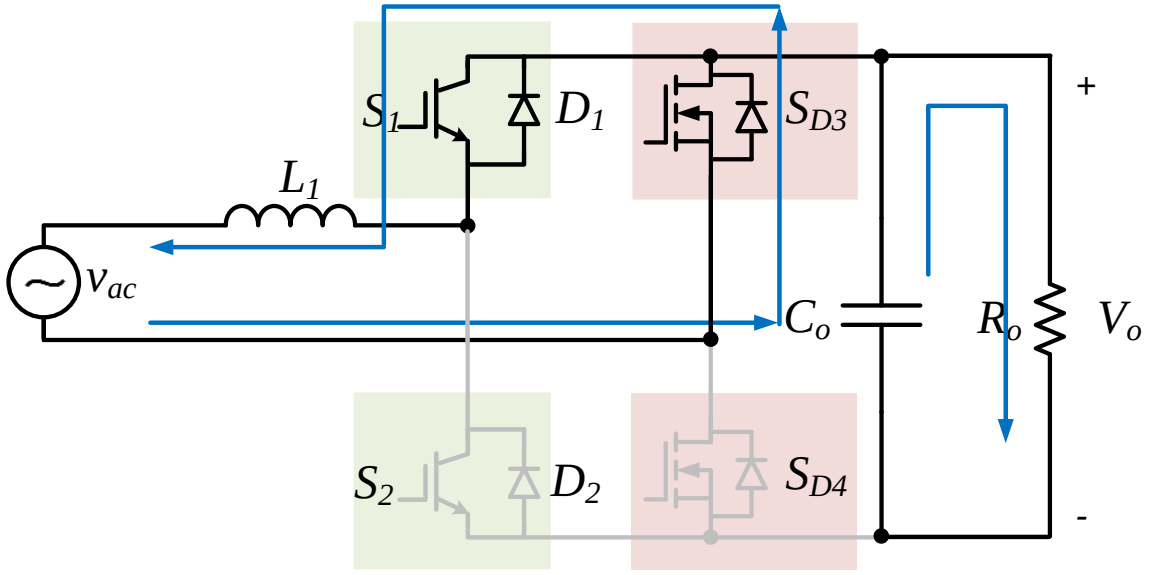


Figure 3.5 Totem-pole PFC Negative line cycle When Switch is On

When the switch S_1 is off, the inductor L_1 discharges the energy to the output and the *SiC* D_2 freewheels the inductor current. The MOSFET S_{D3} is conducting current and connecting the ac source to the positive terminal output.

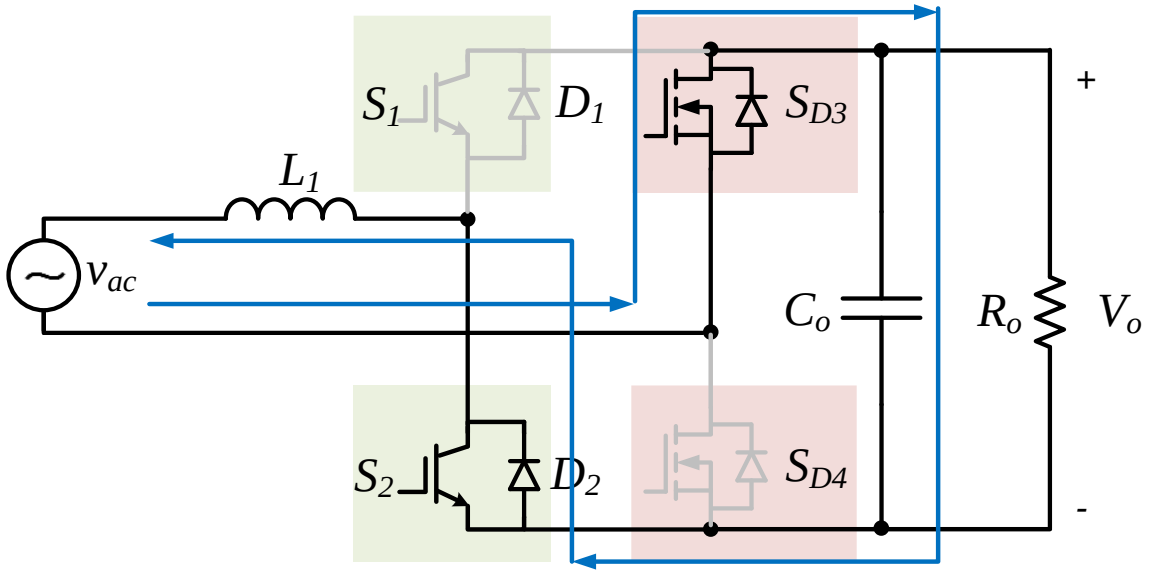


Figure 3.6 Totem-pole PFC Negative line cycle When Switch is off

Based on the analysis for the Totem-Pole PFC operation modes, the switch S_1 and S_2 PWM signal should be working as:

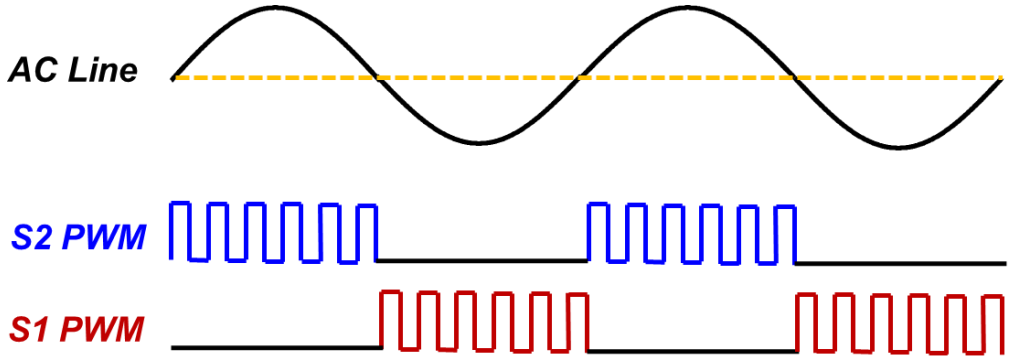


Figure 3.7 Totem-pole PFC Switching Signal

3.4 Zero Crossing Ring Issue with Mosfet Rectification

For further boosting the efficiency, two low R_{dson} MOSFETs can replace the bridge diodes. But there is a serious voltage ring across the MOSFET from drain to

source if the IGBT and MOSFET turn on at the same time. The testing waveform is shown in Figure 3.8 which presents the problem.

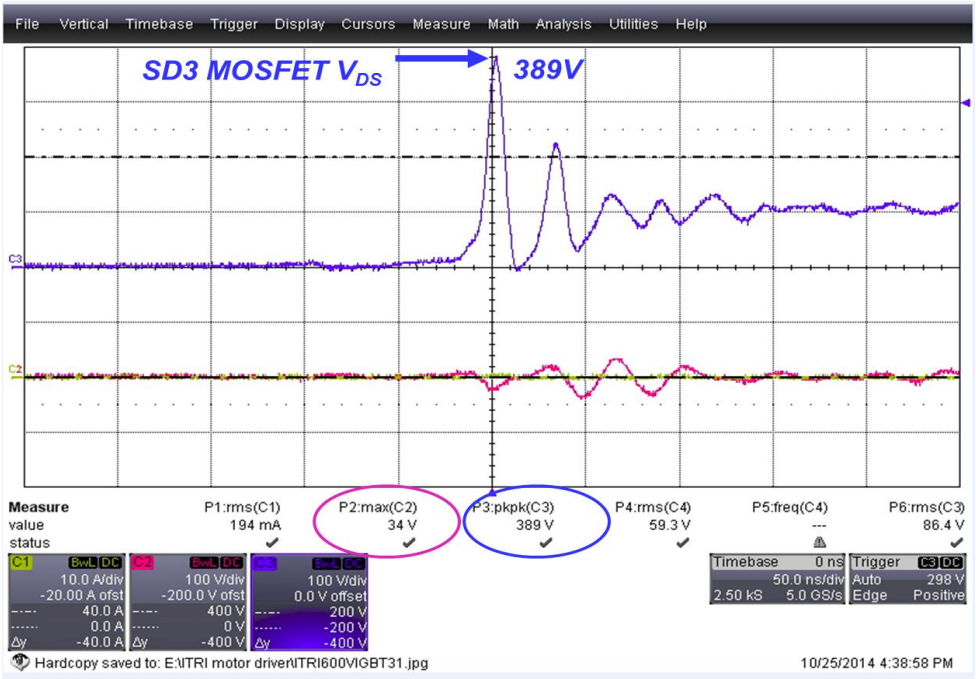


Figure 3.8 Drain to Source Voltage Ring Waveform

From the waveform, during the zero crossing stage, there is a huge voltage ring on the MOSFET SD3. The input voltage is only 34V but the V_{DS} on the MOSFET is almost 390V. This phenomenon can be explained in Figure 3.9.

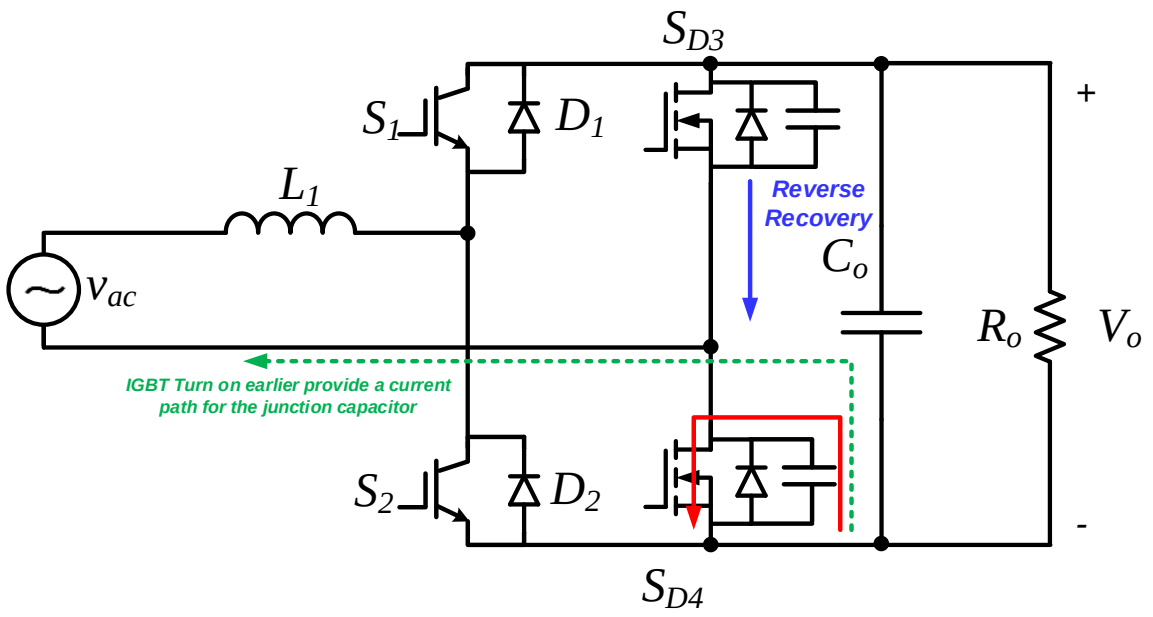


Figure 3.9 Zero Crossing Voltage Ring Issue Analysis

When the line voltage crosses the zero from negative to positive, the S_{D4} takes up most of the output voltage. If the MOSFET S_{D4} with IGBT S_2 turns on at same time, because the S_2 current path has an inductor, the switch S_2 cannot provide a very fast current path for the S_{D4} junction capacitor to outpour the energy. The current from the S_{D4} junction capacitor will go through the S_{D4} channel and the *di/dt* is very high. The voltage on the S_{D3} also increase very fast which makes a reverse recovery current also go through the S_{D4}. This is the reason the huge ring on the MOSFET appears while line rectification MOSFET and switch IGBT turn on at same time.

To solve this problem, the line rectification MOSFET should be turned on later than the switch IGBT for several switching cycles. If the IGBT S_2 start switching before the SD4 turning on, the established inductor current will discharge the junction capacitor ensuring ZVS for SD4. The body diode reverse recovery of SD3 also can be avoided.

There is no large *di/dt*, so the voltage ring will be minimized. The waveform is shown in Figure 3.10.

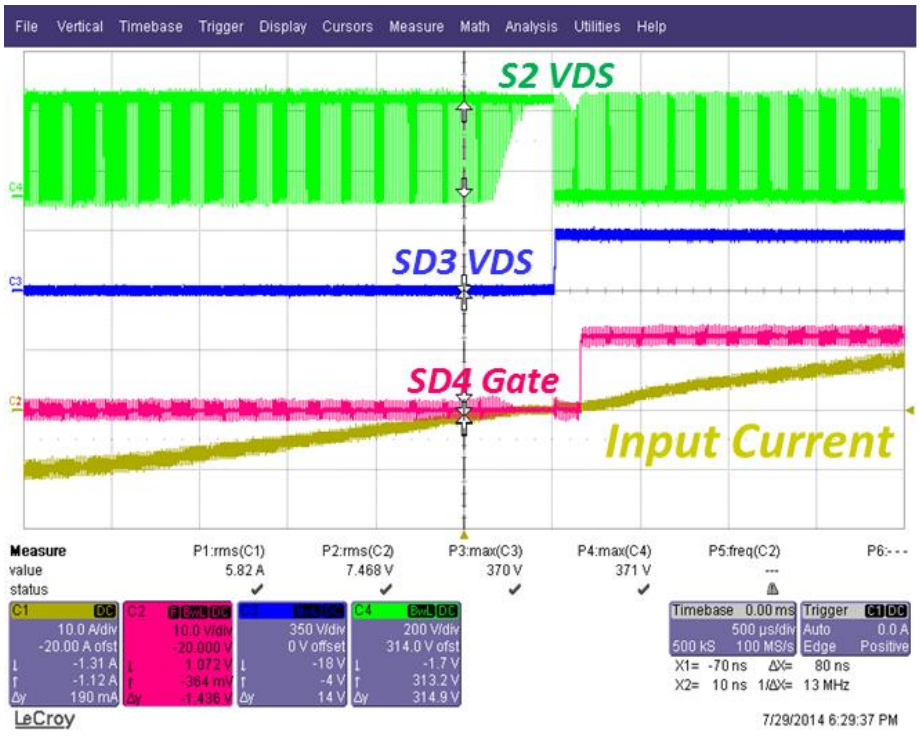


Figure 3.10 Zero Crossing Voltage Ring Issue Analysis

Based on the zero crossing issue, when the totem pole PFC implements the MOSFET as the line rectification, the switch and line rectification MOSFET PWM signal should act as the Figure 3.11.

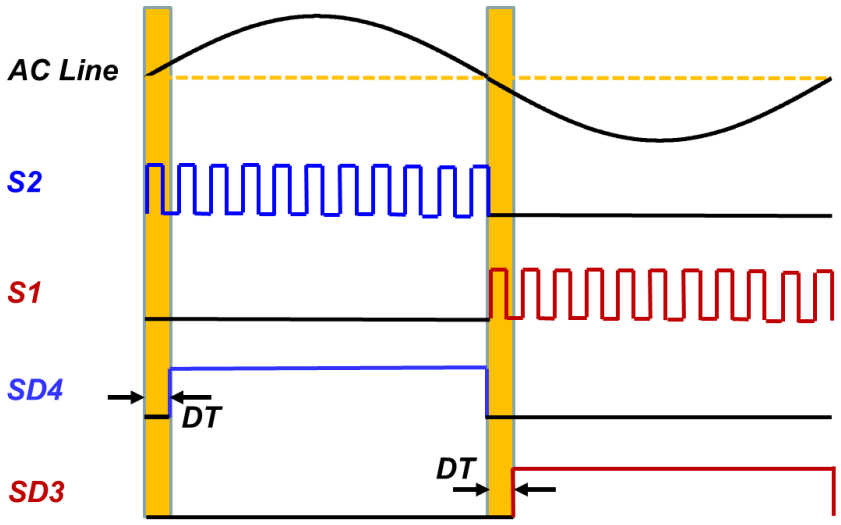


Figure 3.11 MOSFET Line Rectification PWM Signal

3.5 CCM Totem-Pole PFC Control Loop Design

3.5.1 PFC Control Method

Since the totem-pole PFC is working as a boost converter during each half line cycle, the control method is same as the traditional CCM boost PFC. As mentioned in the Chapter 2, the high power CCM boost PFC always use the average current control method. The average current control diagram of boost PFC is shown in Figure 3.12.

The target of the PFC is to make the input current proportional to the input voltage and this causes the input impedance to be a resistive load to the input power as shown in (3.1):

$$\frac{V_{in}(t)}{I_{in}(t)} = R_{in} \tag{3.1}$$

Assume $P_{in} = P_{out}$ thus:

$$\frac{V_{in\_RMS}^{\ 2}}{R_{in}} = P_{in} = P_{out} \tag{3.2}$$

Substitute the R_{in}, and get the input current shown in (3.3):

$$I_{in}(t) = \frac{P_{out} \times V_{in}(t)}{V_{in\_RMS}^{\ 2}} \tag{3.3}$$

(3.3) shows that the controller multiplies the sensed input voltage signal **B** with the power reference **A** generated from the output of voltage loop compensator, and divided by the square of input voltage RMS value **C** to get the input current reference. The theory is also presented in the Figure 3.12.

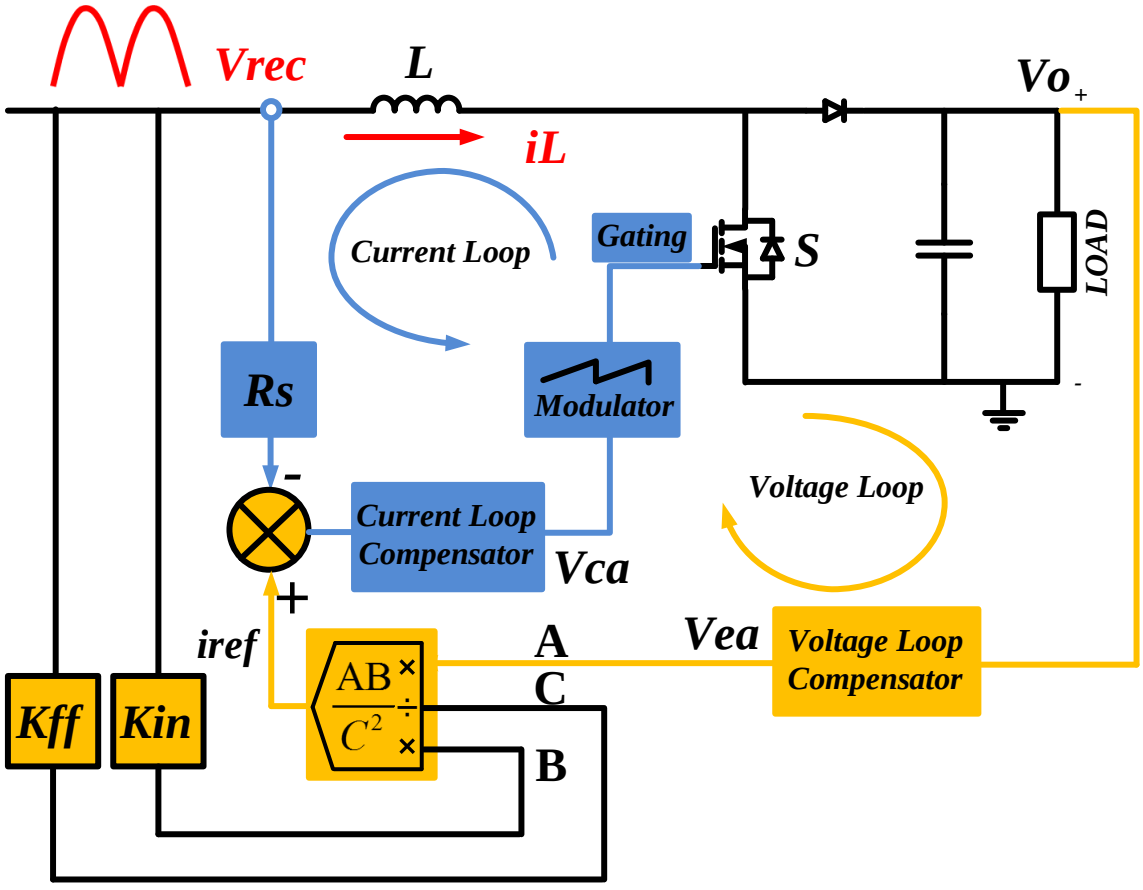


Figure 3.12 Boost PFC Average Current Control Diagram

The average current PFC control system includes a fast current loop, a slow voltage loop and an input voltage feedforward loop. The fast current loop is used to force the input current to be proportional to the input voltage, which seeks the PF equal to 1. The voltage loop regulates the bus voltage at 380-400V. The input voltage feedforward loop is used to balance the input voltage variation for the voltage loop. The voltage loop and current loop have different bandwidth and need to design the loop independently. The current bandwidth should be well above the line frequency usually 2 kHz to 10 kHz to track the current well and decrease the distortion around the zero crossing [24]. Because the switching frequency is much higher than the line frequency, the input voltage can be regarded as a constant voltage during several switching cycles. The small signal model block for the PFC is shown in Figure 3.13.

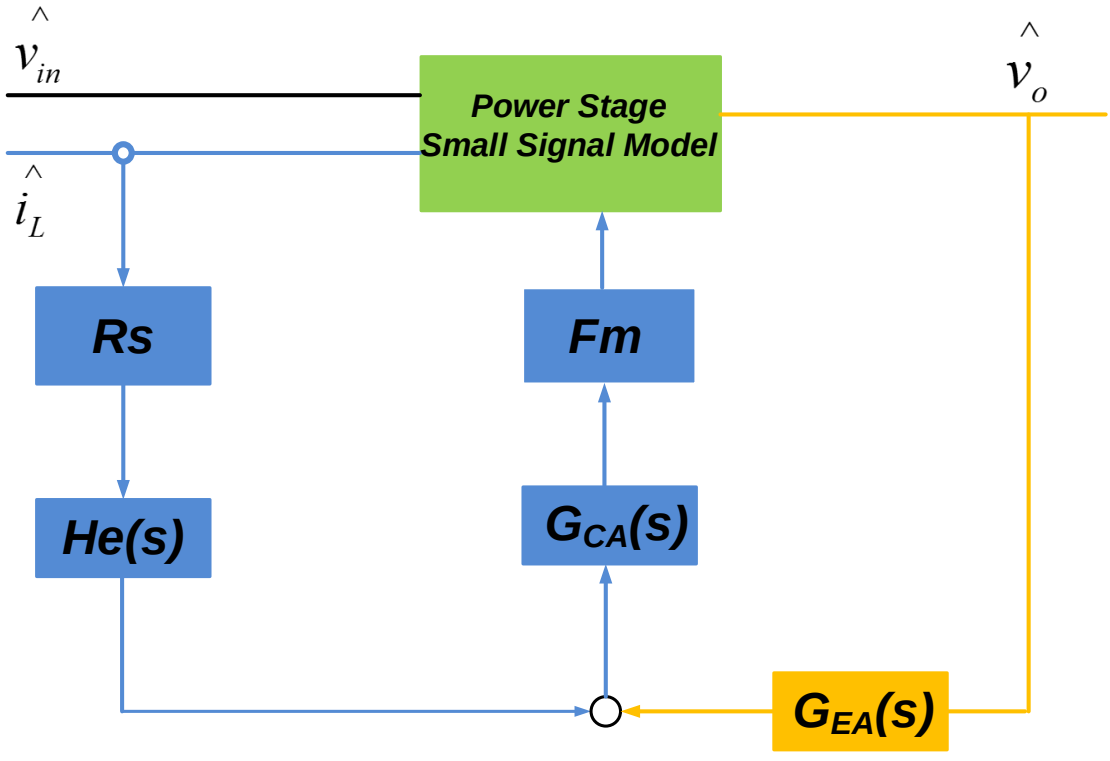


Figure 3.13 PFC Small Signal Model Block Diagram

For frequency between line frequency and half of the switching frequency ($f_L \leq f \leq f_s/2$), the sampling-effect $H_e(s)$ is approximately equal to 1[30]. Therefore, the inner current loop is simplified as:

$$T_{current} = F_m \cdot R_s \cdot G_{CA}(\mathrm{s}) \cdot G_{id}(\mathrm{s}) \tag{3.4}$$

3.5.2 Inner Current Loop Design

Because the switching frequency is much higher than the line frequency, the input voltage can be regarded as the constant voltage during several switching cycles. PWM three terminal model can be used to establish the power stage small signal model [23]. Ignoring the capacitor and inductor series resistance, the power stage control to current small signal model is shown in Figure 3.14.

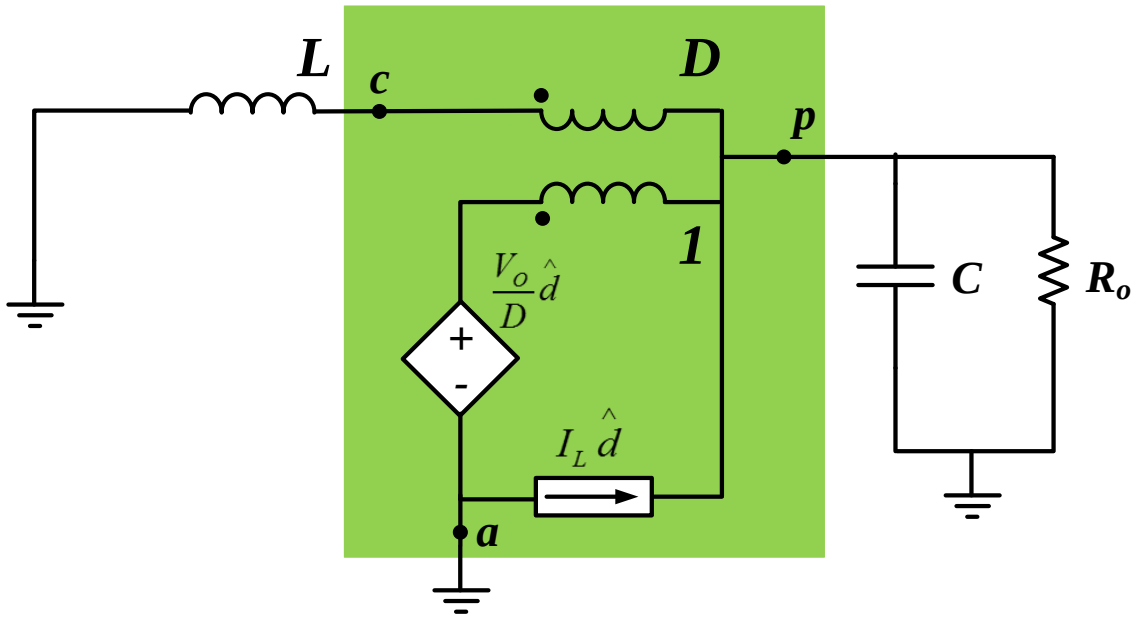


Figure 3.14 power stage control to current small signal model

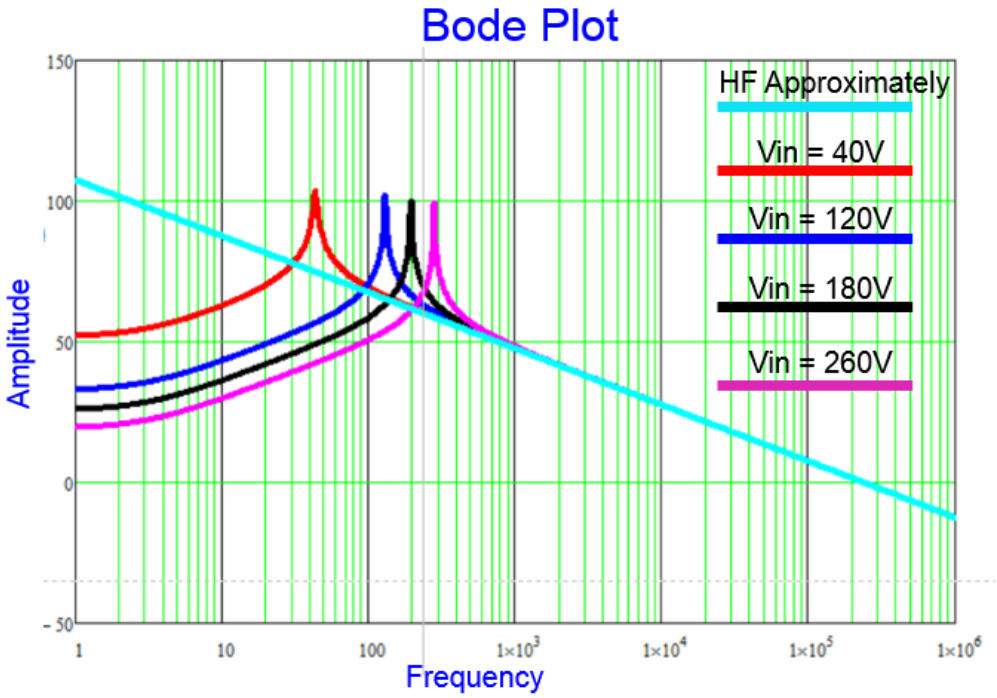
Based on the circuitry, the control to current transfer function can be derived as:

$$G_{id}(s) = \frac{\hat{i}}{\hat{d}} = \frac{2V_o}{R_L(1-D)^2} \cdot \frac{1+\frac{R_L Cs}{2}}{1+\frac{Ls}{R_L(1-D)^2}+\frac{LCs^2}{(1-D)^2}} \tag{3.5}$$

The capacitor impedance is *1/sC*, so at high frequency range the impedance is approximately equal to zero. The control to current transfer function can be simplified as:

$$G_{id}(s) = \frac{\hat{i}}{\hat{d}} = \frac{V_o}{sL} \tag{3.6}$$

Based on the design parameter value for the 1.5 KW PFC, the bode plot of the control to current transfer function $G_{id}(s)$ is shown in Figure 3.15.



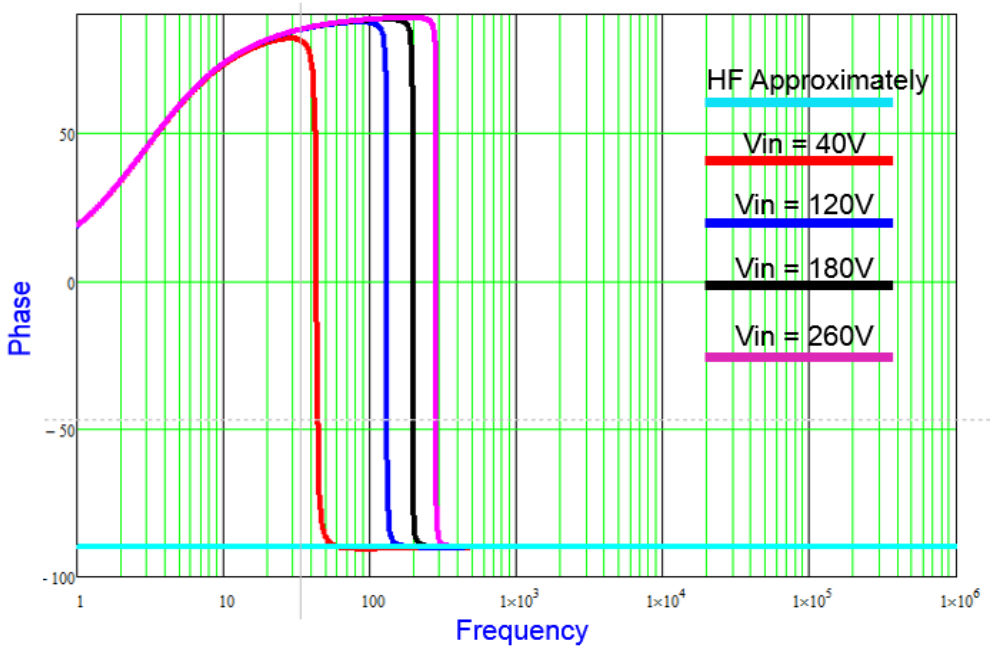


Figure 3.15 Control to Current $G_{id}(s)$ Bode Plot

From the bode plot, different input voltage and load decide the $G_{id}(s)$ low frequency gain value. However the curves of different input voltage are overlapped at the high frequency range. The current loop bandwidth is always higher than 2 kHz so the simplified $G_{id}(s)$ transfer function can be used for the current loop design.

Use the integral and lead-lag compensation to achieve current loop stable. The integrator is used to boost the low frequency gain and the zero is required to make sure the sufficient phase margin. For this design, the current compensation includes one integrator, one zero at 1kHz and one pole at 40 kHz. The compensator loop bode plots are shown as Figure 3.16:

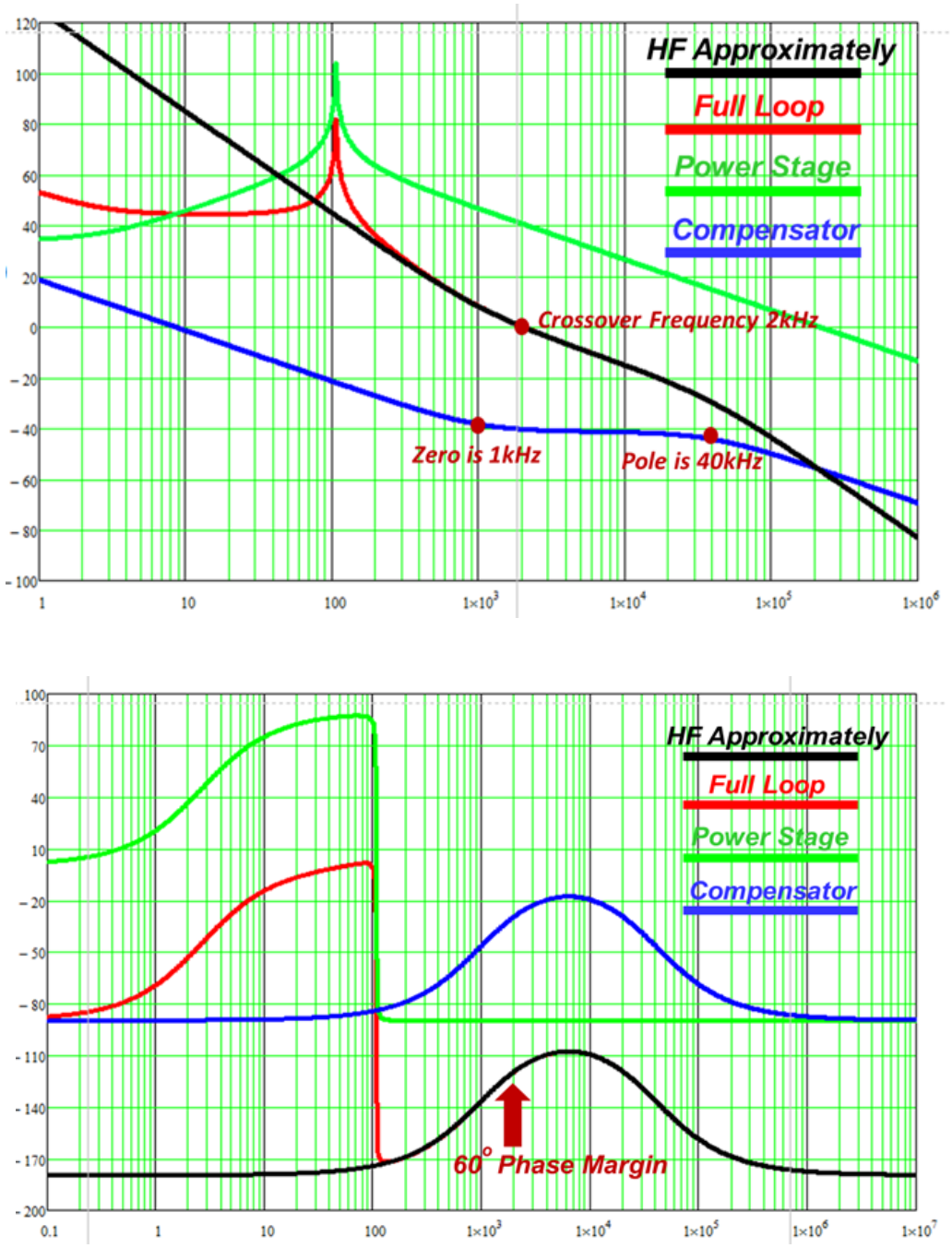


Figure 3.16 Current Loop Compensation Bode Plot

From the compensated current loop, the low frequency gain is enough to track the current reference. The crossover frequency is 2kHz and phase margin is 60^{o} which make the current loop stable enough.

3.5.3 Outer Voltage Loop Design

The voltage loop compensation is independent to the compensated current loop. Based on the small signal model diagram Figure 3.13, the voltage loop diagram can be simplified as Figure 3.17:

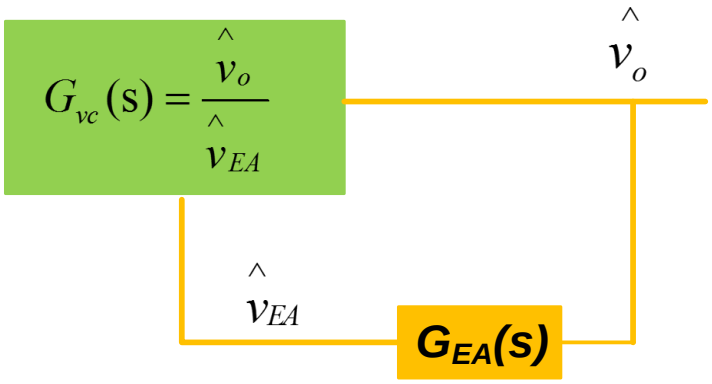


Figure 3.17 Simplified Voltage Loop Diagram

The voltage loop control to output small signal model can be derived by using the power balance equation. Based on the average current control diagram Figure 3.12, when the input current track the input voltage well, the current reference is:

$$i_{in} = \frac{K_{in}}{K_{ff}^{\ 2} v_{in}^{\ 2}} v_{in} v_{EA} \tag{3.7}$$

Assuming efficiency is 100%, based on the power balance $P_{in}=P_{out}$, so the equation is:

$$i_{in} v_{in} = i_{out} v_{out} \tag{3.8}$$

Substitute (3.7) into (3.8), then get:

$$\frac{K_{in}v_{in}}{K_{ff}^{\ 2}v_{in}^{\ 2}}v_{in}v_{EA}=i_o v_o \tag{3.9}$$

Adding perturbation to the equation and assume input voltage without perturbation, the equation can be derived as:

$$\frac{K_{in}v_{in}}{K_{ff}^{\ 2}v_{in}^{\ 2}}v_{in}(v_{EA}+\hat{v}_{EA})=(i_o+\hat{i}_o)(v_o+\hat{v}_o) \tag{3.10}$$

Neglect the nonlinear term, then (3.10) can be derived to:

$$\hat{i}_o=\frac{K_{in}}{K_{ff}^{\ 2}v_{out}}\hat{v}_{EA}-\frac{i_o}{v_o}\hat{v}_o \tag{3.11}$$

Based on the equation, a small signal model diagram is shown below:

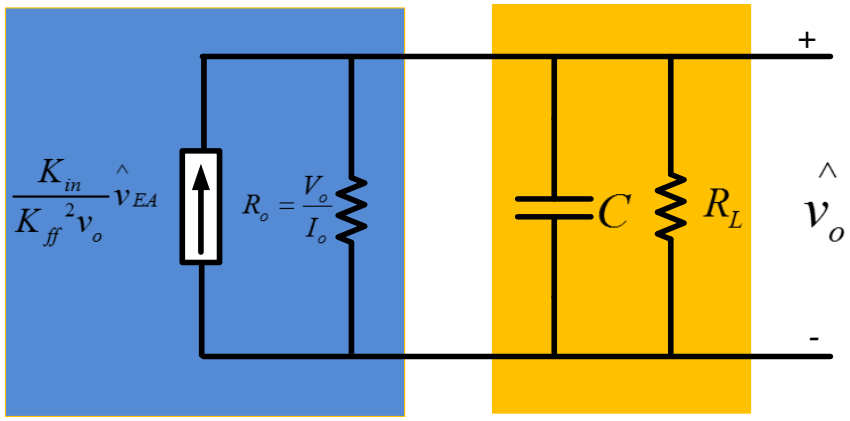


Figure 3.18 Low Frequency Voltage Loop Small Signal Model

Assume the load power is constant, we can get the:

$$dP_o=dV_o I_o+dI_o V_o=0 \tag{3.12}$$

From the Eq. 3.12, we can get:

$$R_o = \frac{dV_o}{dI_o} = -\frac{V_o}{I_o} = -R_L \tag{3.13}$$

So the small signal model diagram for the constant power is shown as Figure 3.19:

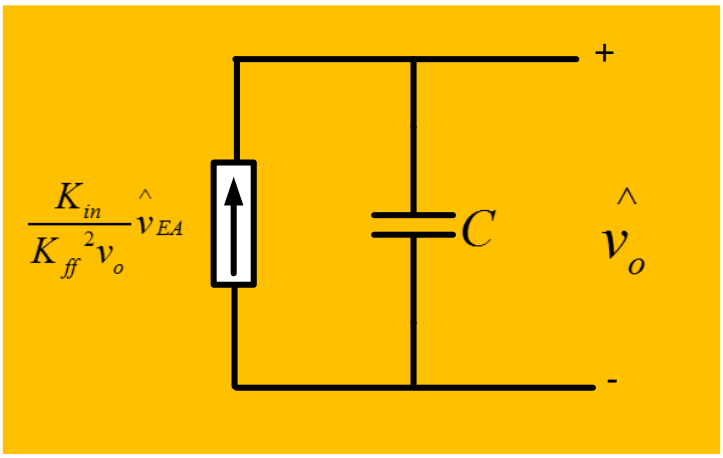


Figure 3.19 Low Frequency Voltage Loop Small Signal Model for Constant Power

Based on the constant power condition, the control to output voltage loop transfer function is shown as:

$$G_{vc}(s) = \frac{\hat{v}_o}{\hat{v}_{EA}} = \frac{K_{in}}{K_{ff}^2 V_o C s} \tag{3.14}$$

The output voltage have inherited second harmonic ripple and this will import the second harmonic component into the voltage loop. The current reference will be affected and make the input current distortion. Therefore, the voltage bandwidth should be well below the 120 Hz to alleviate the second harmonic component at the output of the voltage compensator. For the design requirement, the bandwidth of the voltage loop usually should be chosen at 10 -20 Hz and phase margin is 50º. Based on the 1.5 kW PFC with ADP1048 design parameter, the transfer function Bode plot is shown in Figure 3.20:

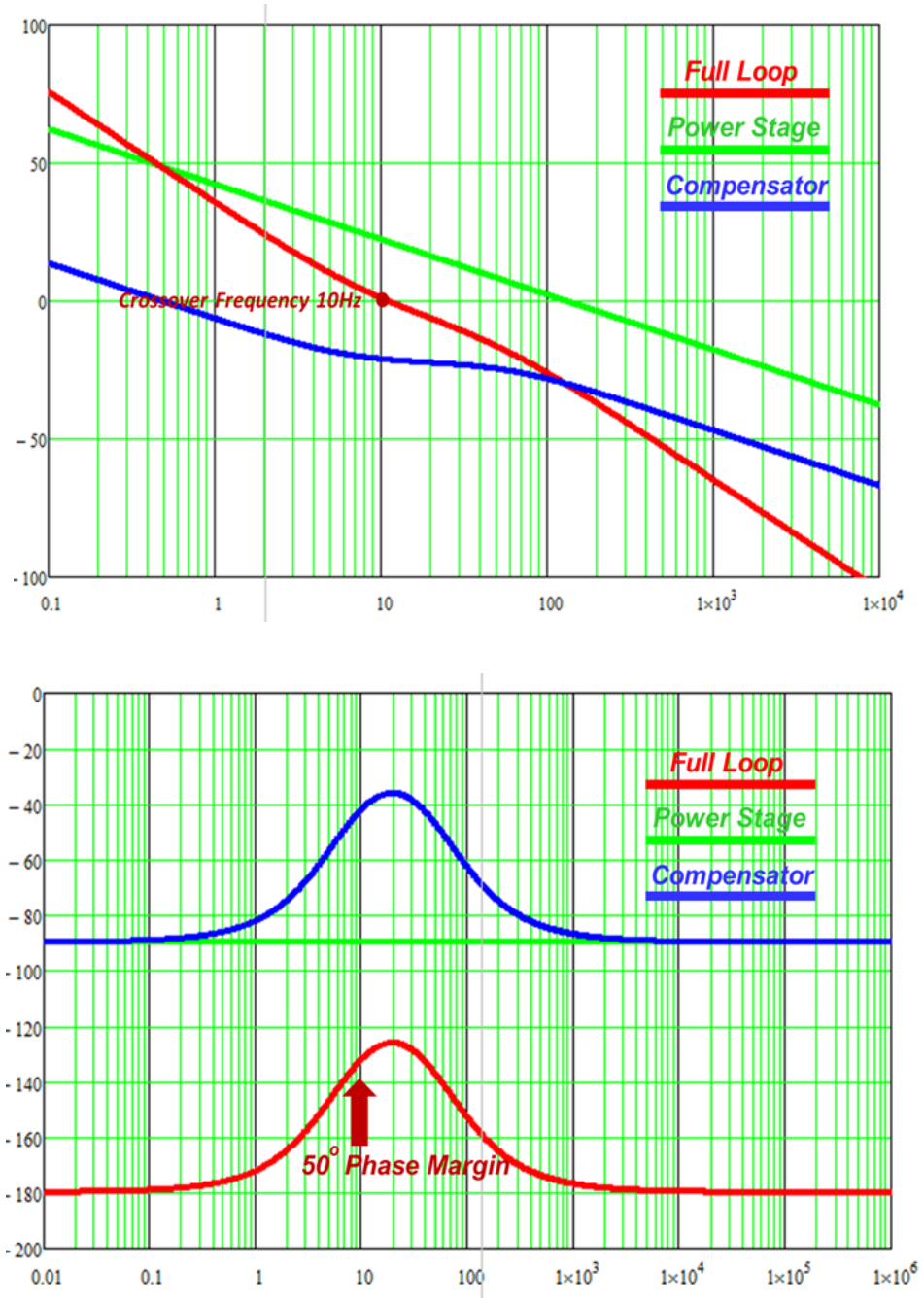


Figure 3.20 Voltage Loop Compensation Bode Plot

3.5.4 Simulation Results

The simulation is designed for the totem-pole PFC topology. The simulation power stage parameters values are all depended on the hardware design in the Chapter 4.

The control loop compensator is designed the same as the previous sections. The simulation adopts the same compensator at different power level. The simulation circuit is shown as Figure 3.21

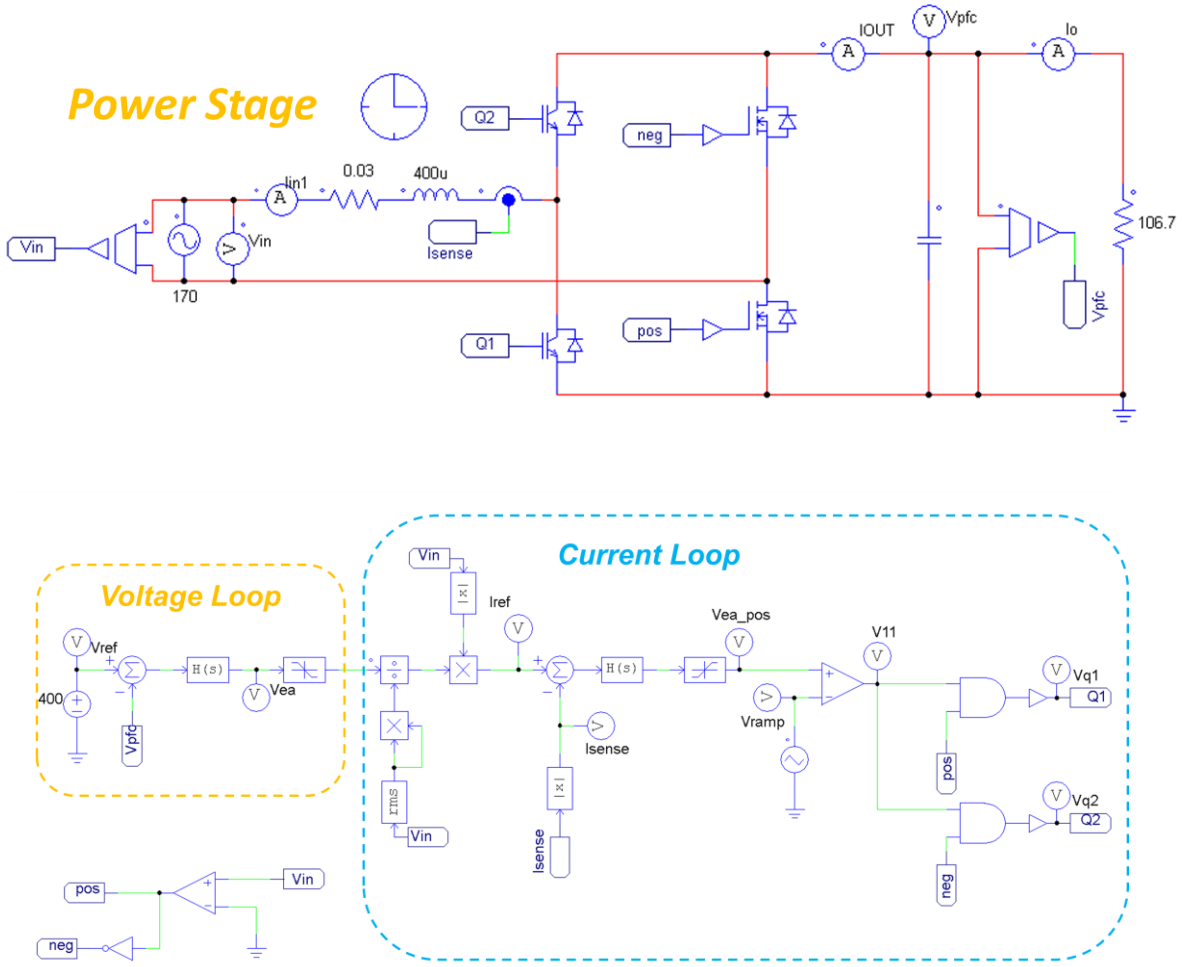
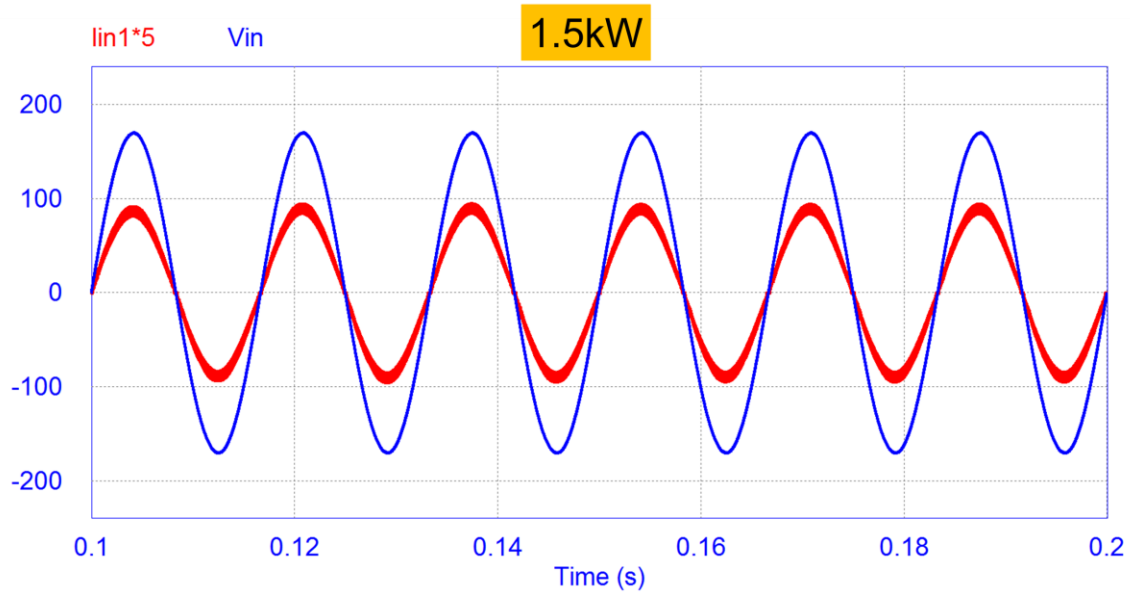
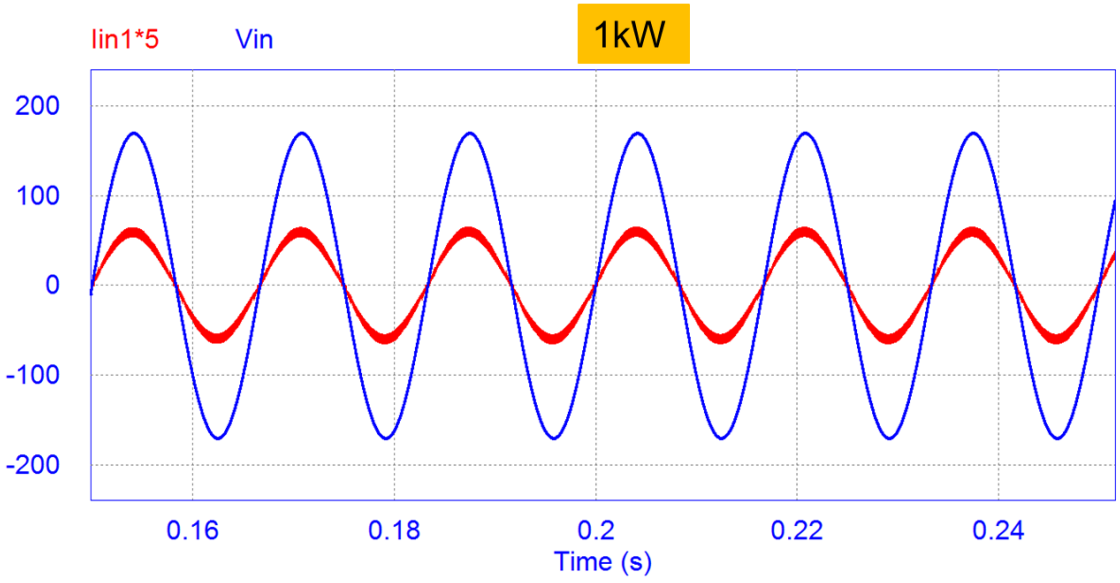


Figure 3.21 Totem-pole PFC Simulation Circuit

Figure 3.22 shows the simulation results with different power level:


1.5kW
Iin1*5
Vin
200
100
0
-100
-200
0.1
0.12
0.14
0.16
0.18
0.2
Time (s)


1kW
Iin1*5
Vin
200
100
0
-100
-200
0.16
0.18
0.2
0.22
0.24
Time (s)

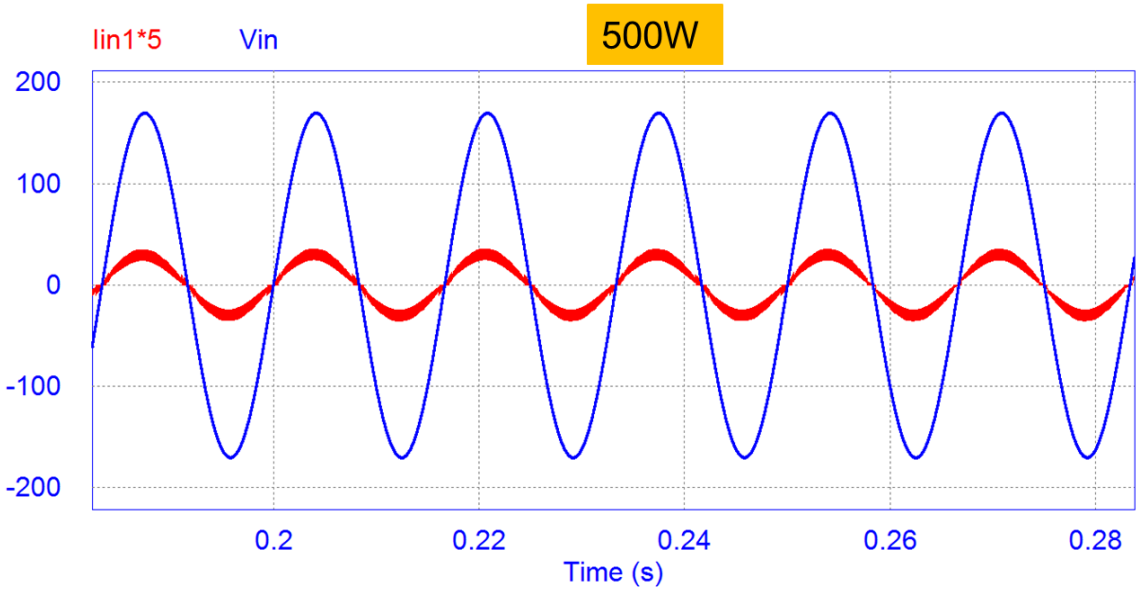


Figure 3.22 Totem-pole PFC Simulation Results with Different Levels

From the waveforms, the input current tracks the line voltage well at different power level. The results present the control loop design is qualified for the power stage parameters.

Chapter 4:

Implement ADP1048 Controller for CCM Totem-Pole PFC Design

This Chapter introduces the design of a totem-pole PFC with ADP1048 controller. The general features and pins functions of ADP1048 are presented. After that is the design of the power stage components, control method design process and the related circuits to finally accomplish the proposed 1.5 kW totem-pole PFC design.

The simplified design circuit is shown in Figure 4.1.

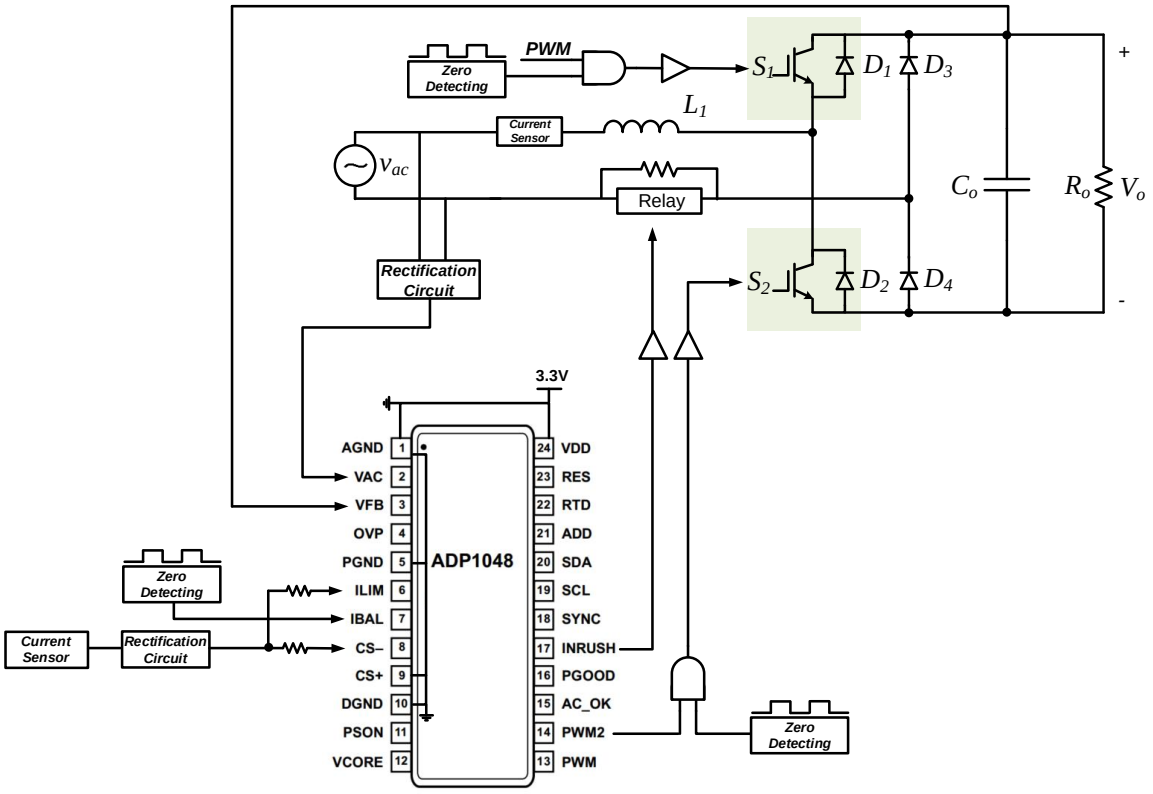


Figure 4.1 Control Diagram with ADP1048 in Totem-Pole PFC Circuit

4.1 ADP1048 Introduction

ADP1048 is a flexible digital PFC controller which has more advantages than the DSP and analog controller. There is no any complex programming required and all the parameters can be written or adjusted through an easy-to-use GUI. It has enough functions to serve as a PFC controller and its cost is cheaper than the DSP. Comparing to the analog PFC controller, the advantages such as easier design process and more flexible functions attract the engineers.

The ADP1048 controller has interleaved and bridgeless PFC operation mode. The digital PFC function is based on the boost PFC with average current control method. The sensing signals are converted into the digital domain to provide maximum flexibility. The design parameter setting and programmed values can be stored into the internal EEPROM allowing standalone control without a microcontroller. ADP1048 can provide accurate input voltage, current and power RMS value. The inrush current signal for soft start can reduce components amounts without complicated design optimization. This controller also has enhanced dynamic response, smart frequency for efficiency optimization, multiple programmable fault detections and protections, digital EMI reduction, external frequency synchronization advanced features [37].

The ADP1048 pin configurations are shown in Figure 4.2:

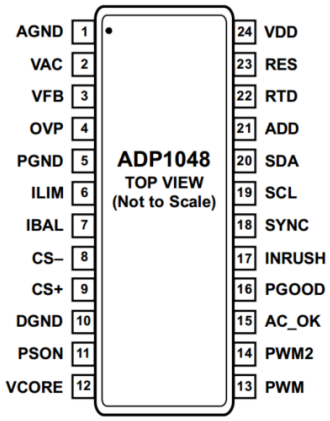


Figure 4.2 ADP1048 Pins Configuration, Analog Devices, "ADP1047/ADP1048 Digital Power Factor Correction Controller with Accurate AC Power Metering" Datasheet. Used under fair use, 2014.

The Pin function descriptions are shown as Table 4.1

Table 4.1 ADP1048 pin function description Analog Devices, "ADP1047/ADP1048 Digital Power Factor Correction Controller with Accurate AC Power Metering" Datasheet. Used under fair use, 2014.

Pin1(AGND)	Analog Ground
Pin2(VAC)	Input Line Voltage Sense
Pin3(VPB)	Feedback Voltage Sense
Pin4(OVP)	Overvoltage Protection
Pin5(PGND)	Power Ground
Pin6(ILIM)	Fast Current Limiting
Pin7(IBAL)	Detect ac Line Phase and Zero Crossings
Pin8(CS-)	Differential Current Sense Negative Input
Pin9(CS+)	Differential Current Sense Positive Input
Pin10(DGND)	Digital Ground
Pin11(PSON)	Power Supply Enable Signal
Pin12(VCORE)	Output of 2.5V Regulator
Pin13(PWM)	PWM Output for PFC Regulation
Pin14(PWM2)	Interleaved/Bridgeless PWM Output
Pin15(AC_OK)	Open-Drain Output
Pin16(PGOOD)	Open-Drain Output
Pin17(INRUSH)	Inrush Current Control Signal to an Eternal Inrush Driver
Pin18(SYNC)	Parallel PFC Controller to synchronize to reduce interference
Pin19(SCL)	I2C Serial Clock Input
Pin20(SDA)	I2C Serial Data Input and Output
Pin21(ADD)	Address Select Input
Pin22(RTD)	Thermistor Input
Pin23(RES)	Internal Voltage Reference
Pin24(VDD)	Positive Supply Input

The controller functional Block Diagram is shown as Figure 4.3

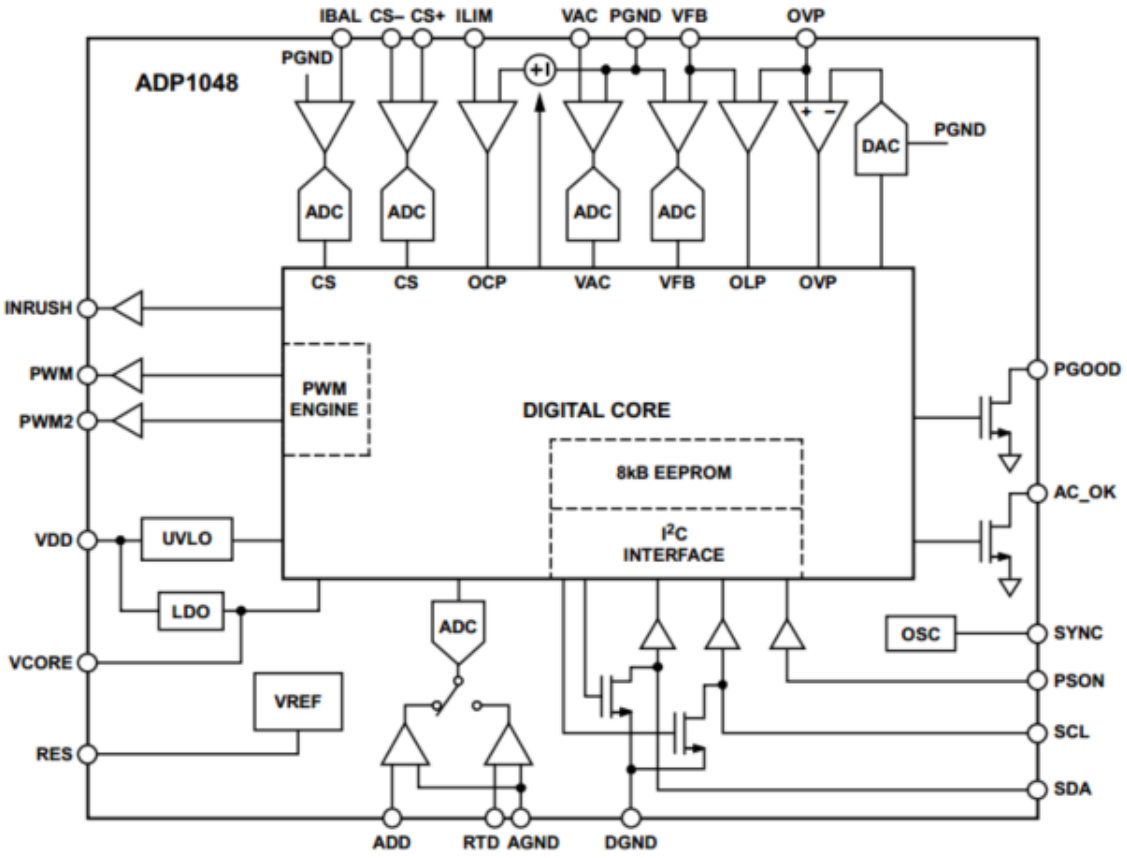


Figure 4.3 ADP1048 Functional Block Diagram, Analog Devices, "ADP1047/ADP1048 Digital Power Factor Correction Controller with Accurate AC Power Metering" Datasheet. Used under fair use, 2014.

4.2 1.5kW Totem-Pole PFC Design Specification

To verify the proposed method in CCM totem-pole PFC, a 1.5 kW Bridgeless PFC is designed. Because this is a high power PFC in CCM mode, average current mode is used as the control method. To apply this proposed method in wide range, digital and

analog controllers are both implemented in the circuit. The specification is shown in Table 4.2.

Table 4.2 1.5KW Totem-Pole PFC Design Specification

Input Voltage (Vin)	90-265Vrms
Output Voltage(Vout)	400V
Maximum Output Power	1.5 kW
Switching Frequency	80kHz
Line Frequency	60Hz
Inductor Current Ripple	20%
Output Voltage Ripple	5%

The boost converter suffers the highest current stress and losses at the low line voltage, so the calculation of design is based on the low line voltage condition. The totem-pole PFC can be regarded as two boost converters working respectively during each half line cycle. The two boost converters share one inductor and same capacitors.

4.3 Power Stage Component Design

4.3.1 Inductor Design

The inductor current is same as the input current which is shown in Figure 4.4(a). Because the switching frequency is much higher than the line frequency, so the inductor current change can be neglected during one switching cycle. The current ripple means peak to peak shown in Figure 4.4(b).

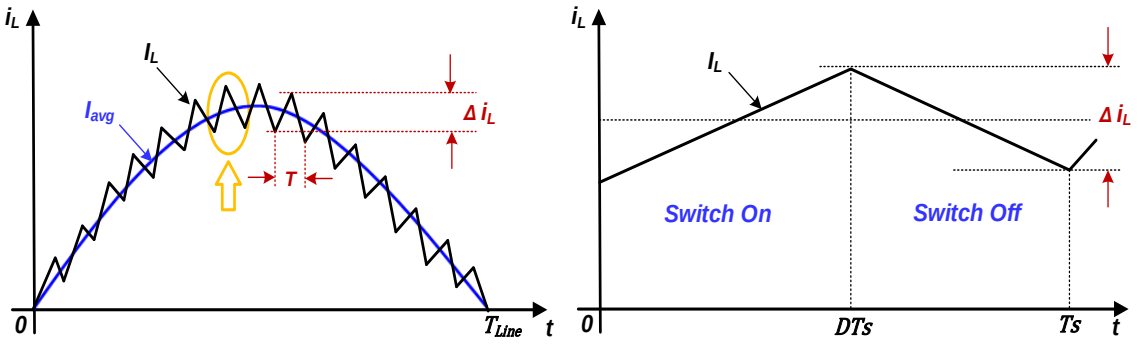


Figure 4.4 Inductor Current (a) Half Line Cycle (b) One Switching Cycle

The maximum peak line current is calculated at the lowest input line voltage condition:

$$I_{in\_pk} = \sqrt{2} \cdot \frac{P_{out}}{V_{in\_\min}} = \sqrt{2} \cdot \frac{1500}{90} \approx 23.6\text{A} \tag{4.1}$$

The current ripple should be reasonable value. If the ripple is too small, the inductance value is high and the size of the magnetic core is big. If the ripple is too high, the DCM period is long. The current ripple ratio is usually in the range of 20% ~30% of the maximum peak input current.

For this design, set the peak to peak current ripple as 20% of the peak current:

$$\Delta I_{pk\_pk} = 0.2 \cdot I_{in\_pk} = 0.2 \times 23.6 = 4.72\text{A} \tag{4.2}$$

The maximum current that the inductor needs to carry is the maximum peak line current value plus the switching frequency ripple current. The maximum inductor current is:

$$I_{L\_\text{pk}} = I_{in\_pk} + \frac{\Delta I_{pk\_pk}}{2} = 23.6 + \frac{4.72}{2} = 25.9\text{A} \tag{4.3}$$

The inductance value must be:

$$L \geq \frac{V_{in\_\min}}{\Delta I_{pk\_pk}} \cdot DT_s \tag{4.4}$$

Boost duty cycle is equal to: $D = \frac{V_{out} - V_{in\_\min}}{V_{out}}$ (4.5)

Substitute (4.5) into (4.4) to replace the D, then:

$$L \geq \frac{D \cdot (1-D)}{\Delta I_{pk\_pk} \cdot f_{sw}} \cdot V_{out} \tag{4.6}$$

When D=0.5, the above equation will generate maximum value. So the value of inductance is:

$$L \geq \frac{0.5 \cdot (1-0.5)}{4.72 \times 80 \times 10^3} \cdot 400 = 264.8uH \tag{4.7}$$

Set the inductance value *L = 300uH*

4.3.2 Capacitor Design

The output voltage ripple and holdup time has to be considered when calculating the bulk capacitance value.

Because the instantaneous input power brings the double line frequency ripple to the output, the PFC converter need bulk capacitor to control the ripple value.

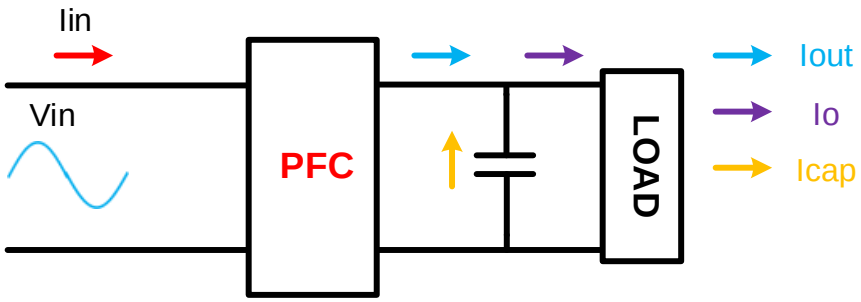


Figure 4.5 PFC diagram

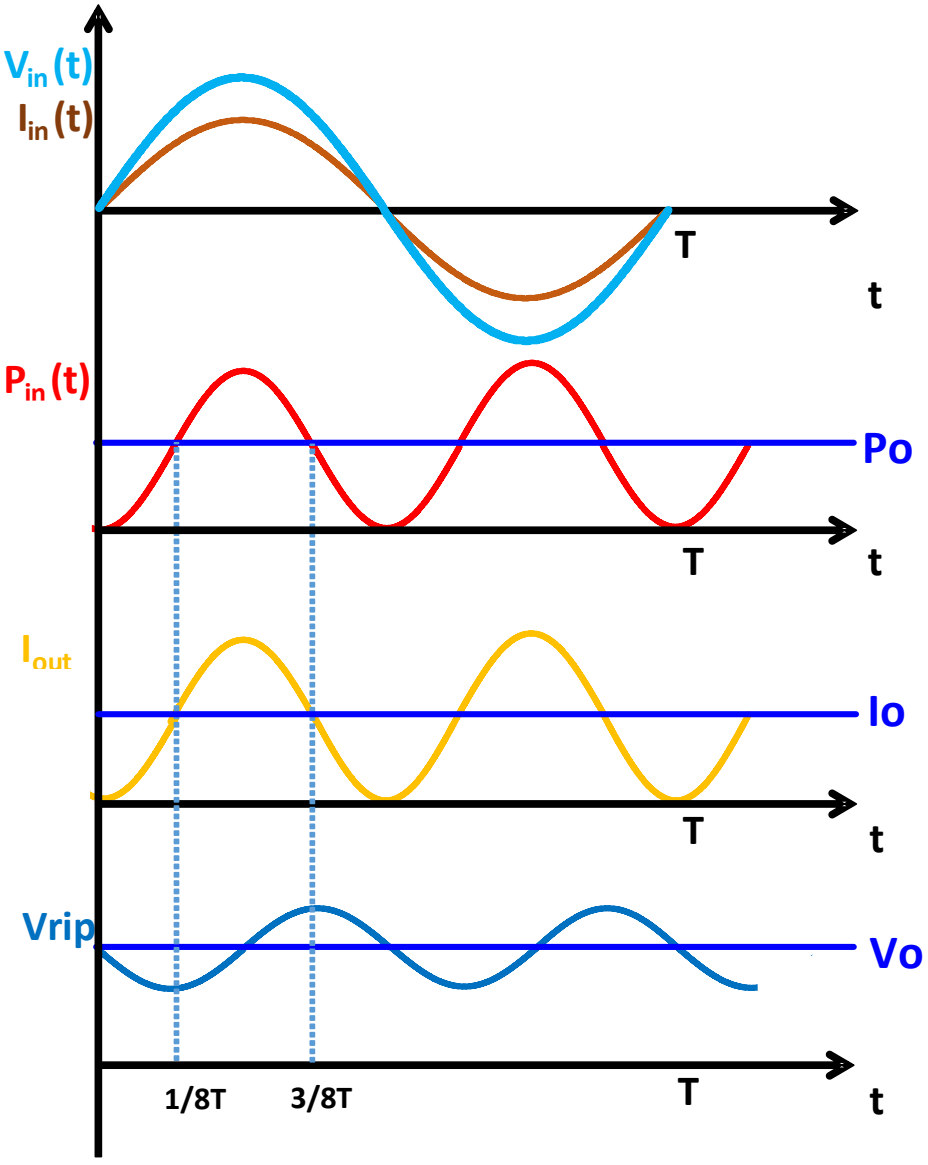


Figure 4.6 Output Voltage Ripple Waveform

From Figure 4.6, the rectifier input voltage is:

$$v_{in}(\mathrm{t}) = \sqrt{2}V_{in}\sin\omega t \tag{4.8}$$

The rectifier current is:

$$i_{in}(\mathrm{t}) = \sqrt{2}I_{in}\sin\omega t \tag{4.9}$$

So the instantaneous input power is:

$$p_{in}(\mathrm{t}) = \sqrt{2}V_{in}\sin\omega t\cdot\sqrt{2}I_{in}\sin\omega t = V_{in}I_{in}\left(1-\cos 2\omega t\right) \tag{4.10}$$

And $$p_{in}(\mathrm{t}) = V_o i_{out}(\mathrm{t}) \tag{4.11}$$

From the (4.11) and (4.12), the $i_{out}(t)$ is equal to:

$$i_{out}(\mathrm{t}) = \frac{V_{in}I_{in}}{V_o}(1-\cos 2\omega\,\mathrm{t}) \tag{4.12}$$

Use the $i_{out}(t)$ subtract the load current, then get the bulk capacitor current is:

$$i_{cap}(\mathrm{t}) = i_{out}(\mathrm{t}) - I_o = \frac{V_{in}I_{in}}{V_o}(1-\cos 2\omega\,\mathrm{t}) - \frac{V_{in}I_{in}}{V_o} = -\frac{V_{in}I_{in}}{V_o}\cos 2\omega\,\mathrm{t} \tag{4.13}$$

The bulk capacitor current is shown in Figure 4.6, and the impedance of the bulk capacitor is: $\dfrac{1}{\omega C_{out}}$

So the voltage ripple equal to:

$$V_{ripple} = \frac{V_{in}I_{in}}{2V_o\omega C_{out}} \tag{4.14}$$

From the equation, the bulk capacitor value determines the output voltage ripple. Usually set the peak to peak ripple is 5% of the output voltage. And the capacitance should be more than the calculation value:

$$C_{out} \geq \frac{V_{in}I_{in}}{V_o} \cdot \frac{1}{2\omega V_{ripple}} = \frac{V_{in}I_{in}}{V_o} \cdot \frac{1}{2\pi \cdot f_{Line}V_{ripple}} = \frac{1500}{400} \cdot \frac{1}{2\pi \times 60 \times 10} = 995uF \qquad (4.15)$$

The holdup time means when line voltage interruption or fault happens, the output voltage can still keep in a normal operation range. Generally, the holdup time is equal to one line voltage cycle. If the minimum normal operation output voltage is 300V, the output capacitance is:

$$C_{out} \geq \frac{P_{out} \cdot t_{holdup}}{\frac{V_{out}{}^2 - V_{out\_\min}{}^2}{2}} = \frac{1500 \cdot \frac{1}{60}}{\frac{400^2 - 300^2}{2}} = 714uF \qquad (4.16)$$

The design selects the higher capacitance value to fulfill two requirements. Based on the real capacitor rating, two 560 *uF* electrolytic capacitors are selected.

4.3.3 Power Switch Selection

Considering the power switch design requirement, the peak current under full power and minimum input voltage condition is needed to be calculated. The safety margin coefficient *Q=1.3* also should be included.

$$I_{SW-PK} = 1.3\left(\frac{\sqrt{2}P_{out}}{V_{\min}} + \frac{\Delta i_L}{2}\right) = 33.7\,\text{A} \qquad (4.17)$$

The ultra-fast IGBT *IGW40N65H5* is selected as the power switch.

The boost diode should have low forward voltage, fast reverse recovery and suitable voltage and current rating values. The average current of the boost diode in this design is:

$$i_{in}(t) = \mathrm{I}_{PK\_MAX} \left|\sin(2\pi f_{Line} t \cdot T_{sw})\right| \qquad \frac{f_{sw}}{2 f_{Line}} = 666 \qquad t = 0,1...666 \tag{4.18}$$

$$i_{DB\_AVG}(t) = (1 - D(t)) \cdot i(t) \tag{4.19}$$

$$i_{DB-AVG} = \frac{\sum_{t=1}^{833} (i_{DB\_AVG}(t) \cdot T_{sw})}{T_{Line} / 2} = 5.68\,\mathrm{A} \tag{4.20}$$

The Infineon *IDK10G65C5* (1.5V forward voltage, 650V voltage rating and 10A current rating) is selected as the boost diode. This *SiC* schottky diode has low forward voltage and no reverse recovery feature which is suitable for the proposed design.

4.4 Control Design with ADP1048

4.4.1 Modified ADP1048 PWM Signal for Totem-Pole PFC

The ADP1048 can support bridgeless PFC operation mode but the PWM signals are not suitable for totem-pole PFC. The schematic of dual boost bridgeless PFC controlled by ADP1048 is shown as Figure 4.7 :

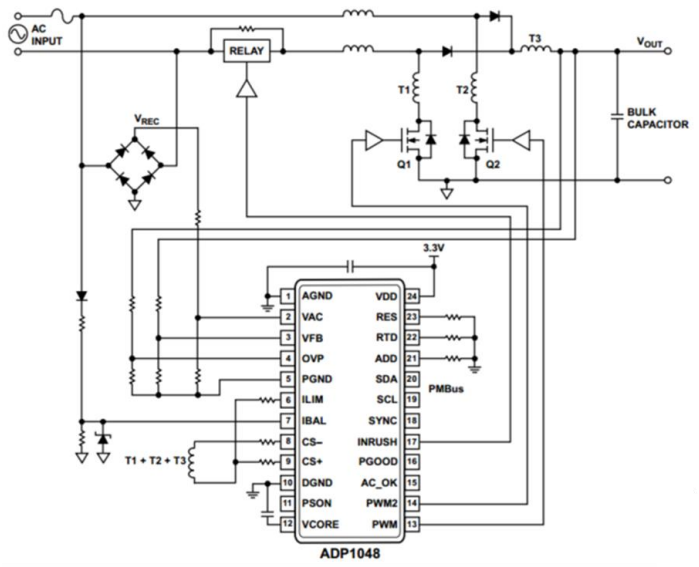


Figure 4.7 Schematic of Dual Boost Bridgeless PFC Circuit with ADP1048, Analog Devices, "ADP1047/ADP1048 Digital Power Factor Correction Controller with Accurate AC Power Metering" Datasheet. Used under fair use, 2014.

During the positive ac line, the Q2 is active switch, and Q1 is always on. During the negative ac line, the Q1 is active switch and Q2 is always on. The PWM signal generated from ADP1048 is shown as:

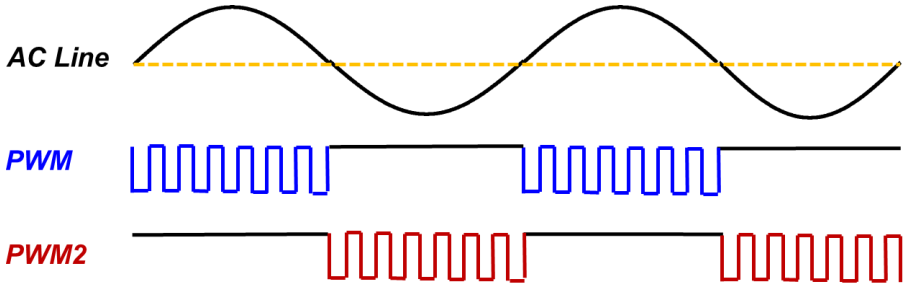


Figure 4.8 ADP1048 Bridgeless Mode PWM Signal

The PWM signals are needed to be modified to serve for the totem-pole PFC. Based on the proposed totem-pole PFC operation mode, when during one half line cycle, one switch is active, the other should be always off. So using AND gate logic is

necessary to achieve the desired PWM signals. The modified ADP1048 PWM signal diagram is shown as Figure 4.9:

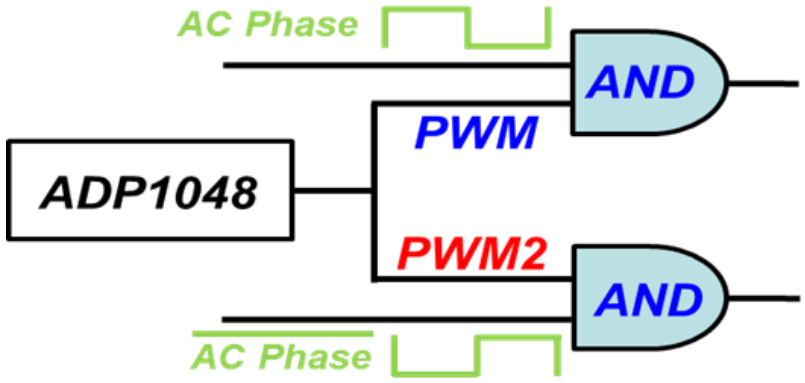


Figure 4.9 Modified ADP1048 PWM Signal Diagram

4.4.2 Input Voltage Sensing Design

LEM voltage sensor is implemented for sensing input voltage. The output of the voltage sensor is ac current signal so measuring resistance and accurate rectifier circuit are needed for satisfying the VAC pin 0V-1.6V operating input range [37]. The input voltage sensing circuit diagram is shown as Figure 4.10.

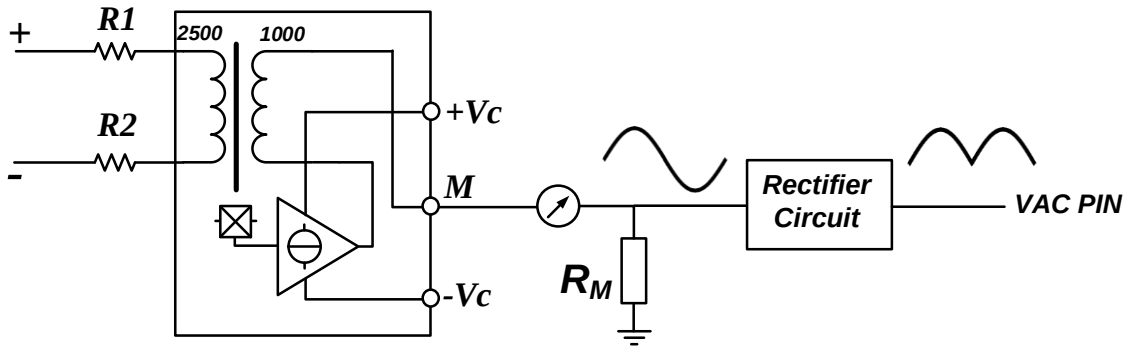


Figure 4.10. Input Sensing Circuit Diagram

The voltage sensor primary side RMS current is 10mA, for the design in low line condition, select R1 = R2 = 12.5 kΩ. Considering the operating range for the VAC pin, the design chooses R_M = 190 Ω. So the input voltage scale down ratio is:

$$Ratio\_vac = \frac{2.5}{R1+R2} \cdot R_M = \frac{1}{197} \tag{4.21}$$

4.4.3 Output Voltage Sensing Design

Based on the ADP1048 datasheet, the VFB pin is used for control, protection and observation of the output voltage. The operating output voltage range for VFB pin is 0V-1.6V. Because of the output voltage design target is 400V, so selecting a reasonable output voltage scale down ratio is: 0.0027.

4.4.4 Input Current Sensing Design

LEM current sensor is implemented for sensing input current. Because the output of the current sensor is ac current signal and current reference is rectified signal, the rectifier circuit and measuring resistance are needed. The maximum operating range between the current sensing pins CS+ and CS- is 200mV [39], so the rectified input current signal should be scaled down. The input current sensing circuit diagram for ADP1048 is shown as Figure 4.11.

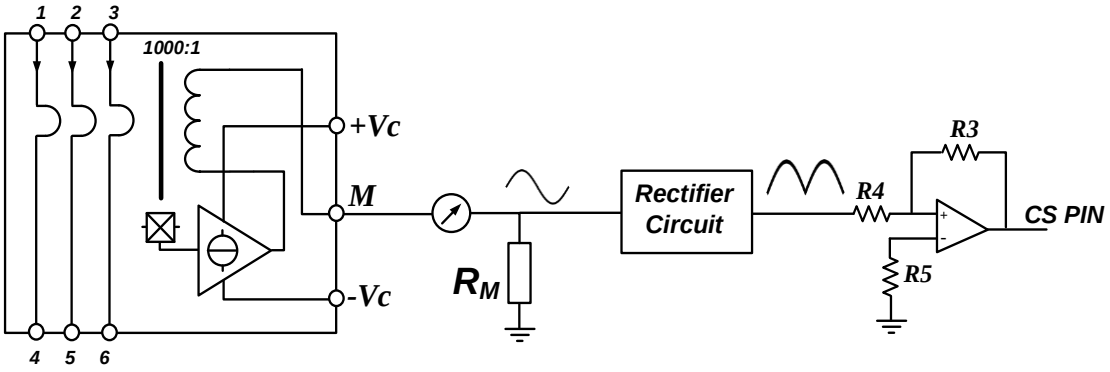


Figure 4.11 Input Current Sensing Circuit Diagram

The current sensor conversion ratio is 1000:1. Considering the operating range for the VAC pin, select R_M=190Ω, R3=10kΩ, R4=150kΩ. So the input current scale down ratio can be regarded as sensing resistor value:

$$R_{sense} = \frac{1}{1000} \cdot R_M \cdot \frac{R3}{R4} = 0.013 \tag{4.22}$$

4.4.5 ADP1048 Control Setting

An easy-to-use graphical user interface (GUI) is provided for programming and configuring the ADP1048. All the necessary parameters for the PFC control can be set up through the interface which dramatically reduces the power supply design and development time [38]. The ADP1048 communicates with the GUI software using the I2C bus. The APD1048 stores all its settings in the EEPROM. When the ADP1048 is connected to the USB adapter the LDO powers the I.C. and the GUI downloads the settings from the register of the ADP1048 so that the state of the part is known [37]. The GUI main interface window is shown as Figure 4.12

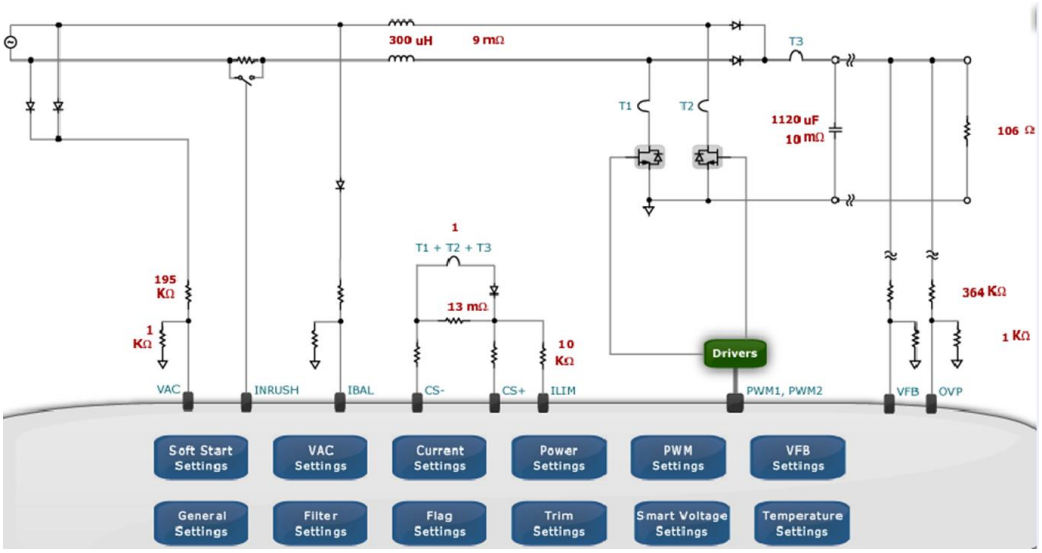


Figure 4.12 GUI Main Interface Window

There are two parts on the main interface that are boarding settings and register settings. The board setting contains all the information about the power board, such as sensing ratio, output capacitor and inductor values [37]. The 1.5 kW totem-pole PFC design parameter values are all shown in the board setting parts in Figure 4.12. The register setting contains the information that governs the functionality of the part such as the over power, voltage and current limits, soft start timing, PWM settings, fault response etc [37].

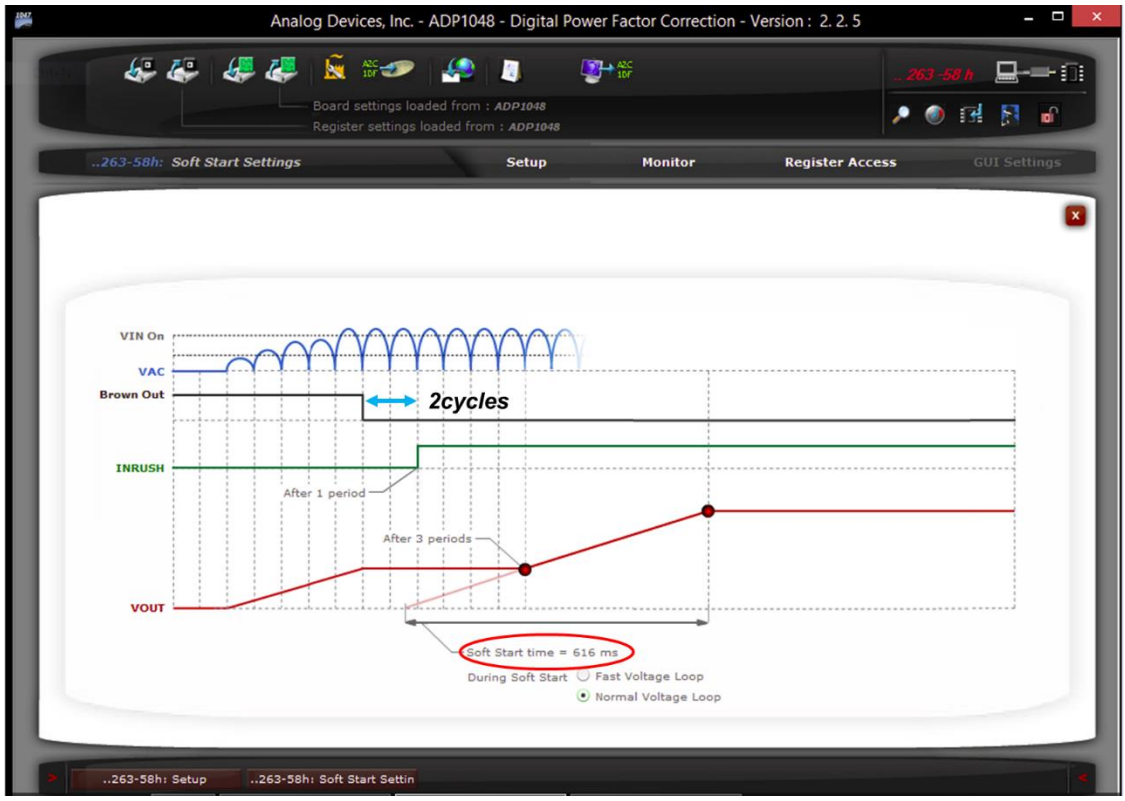


Figure 4.13 Soft Start Setting in GUI

When V_{ac} is higher than the *VIN_ON* value, the BROWN_OUT is set to low. After two cycles, an inrush signal sends to the relays. After the soft start time, the output is ramped up according to the setting. In this 1.5kW totem-pole PFC design, the soft start time is 616ms. The soft start setting is shown in Figure 4.13.

The ADP1048 has the over current, voltage and power limit protection. The controller responses to protect the system once the limit values are touched. All the responses during faults happened can be set through the flag settings part. The current limit setting is shown in Figure 4.14. The voltage limit setting is shown in Figure 4.15. The power setting is shown in Figure 4.16. The flag setting is shown in Figure 4.17.

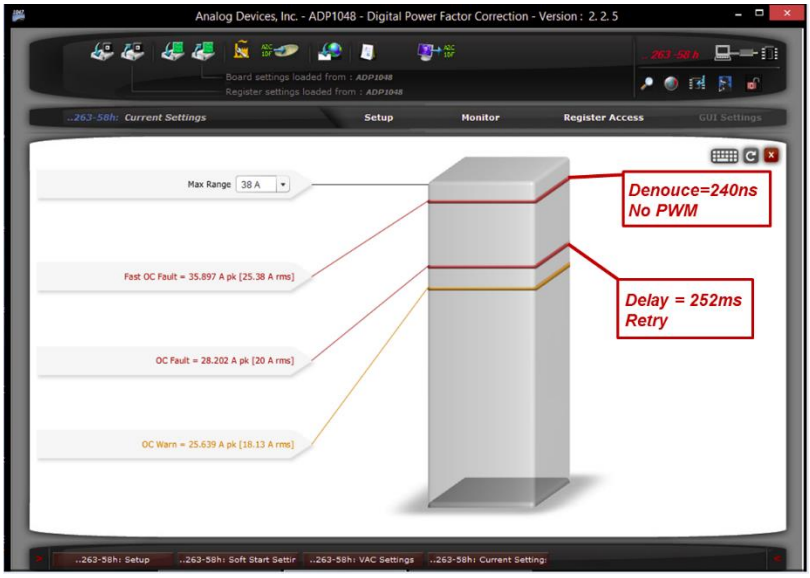


Figure 4.14 Current Limit Setting in GUI

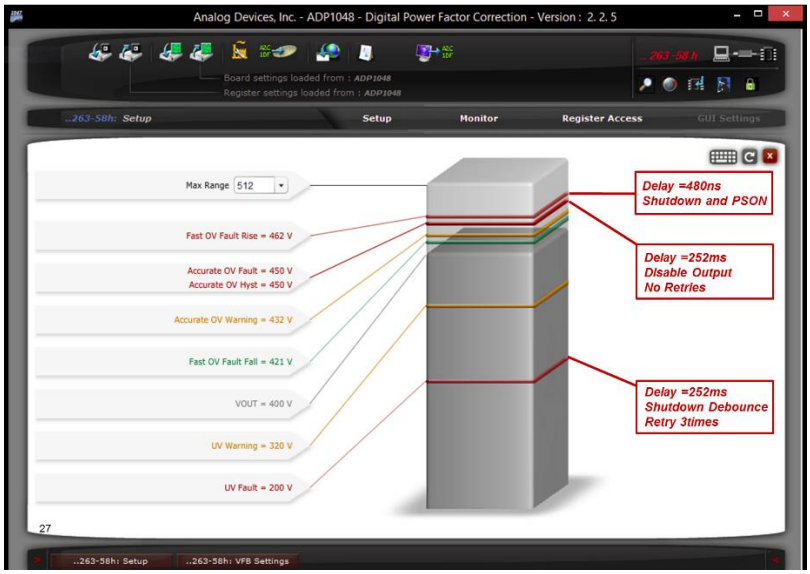


Figure 4.15 Voltage Limit Setting in GUI

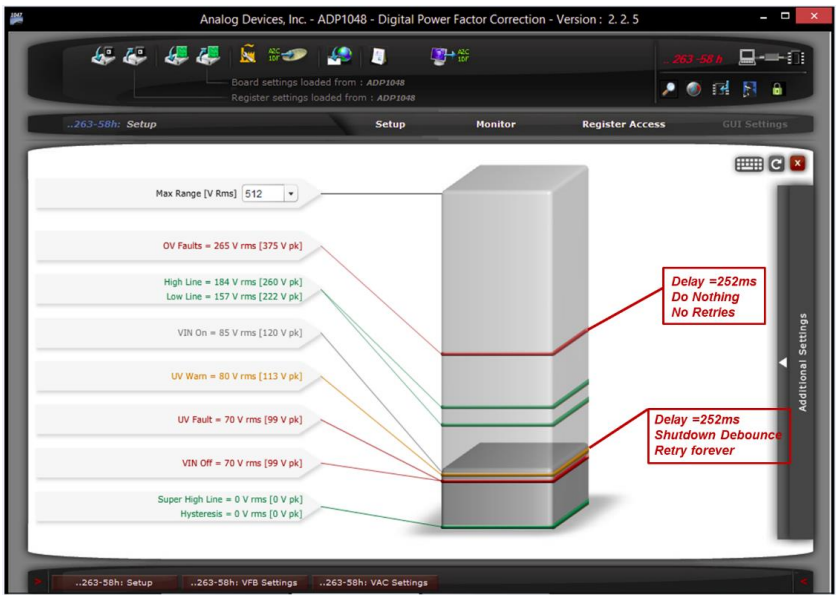


Figure 4.16 Power Setting in GUI

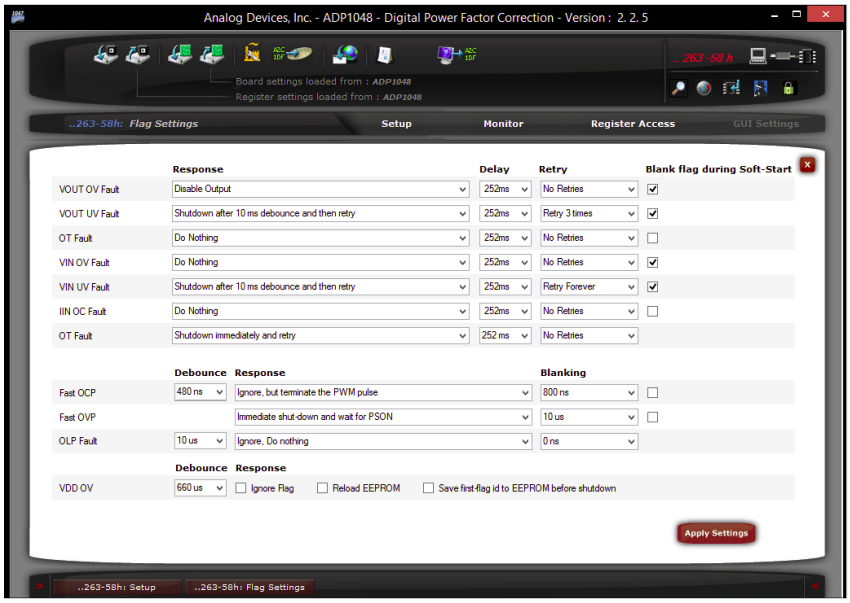


Figure 4.17 Flag Setting in GUI

The current and voltage loop compensator design is set at the filter settings part. The implementation of the loop is digital, and all the signals are converted from analog to digital before they are processed by the control loop. In this design, 2kHz crossover frequency and 60^{o} phase margin for low line in Figure 4.18 is settled which is almost same as the simulation design. For high line input voltage, the plant DC gain is lower, so

higher bandwidth is needed. The compensator for high line is shown in Figure 4.19. The voltage loop compensator setting is shown in Figure 4.20.

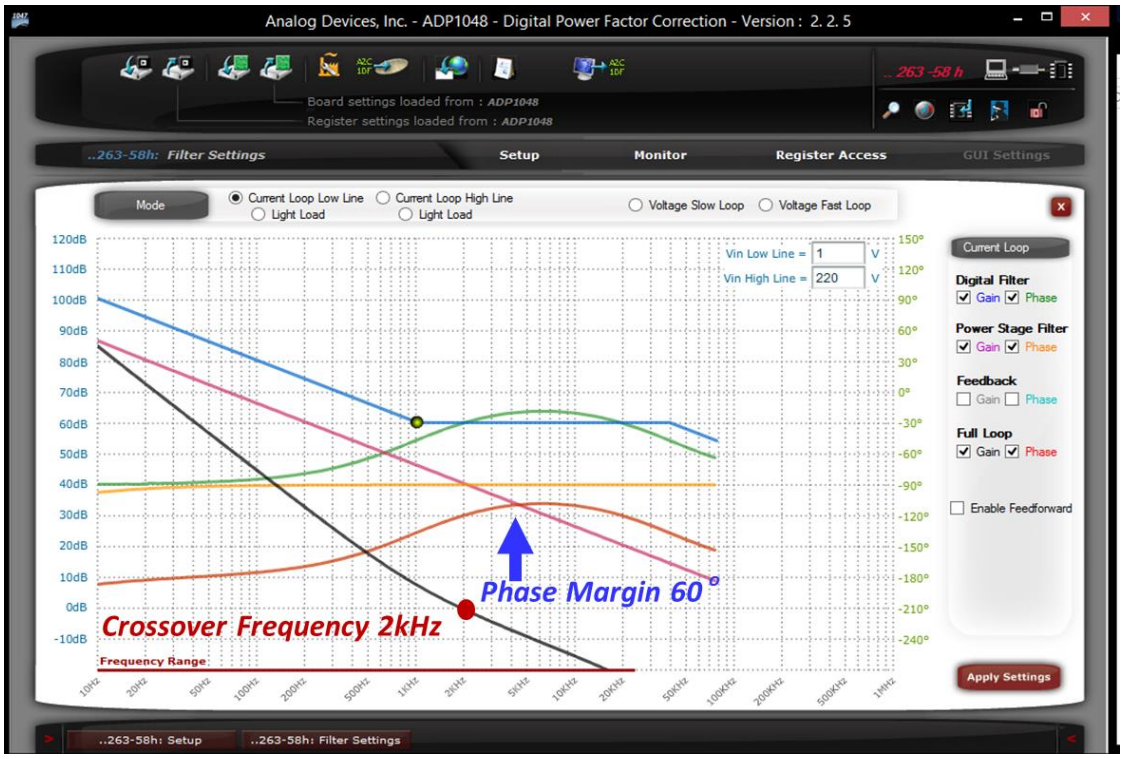


Figure 4.18 Current Loop Compensator Design for Low Line

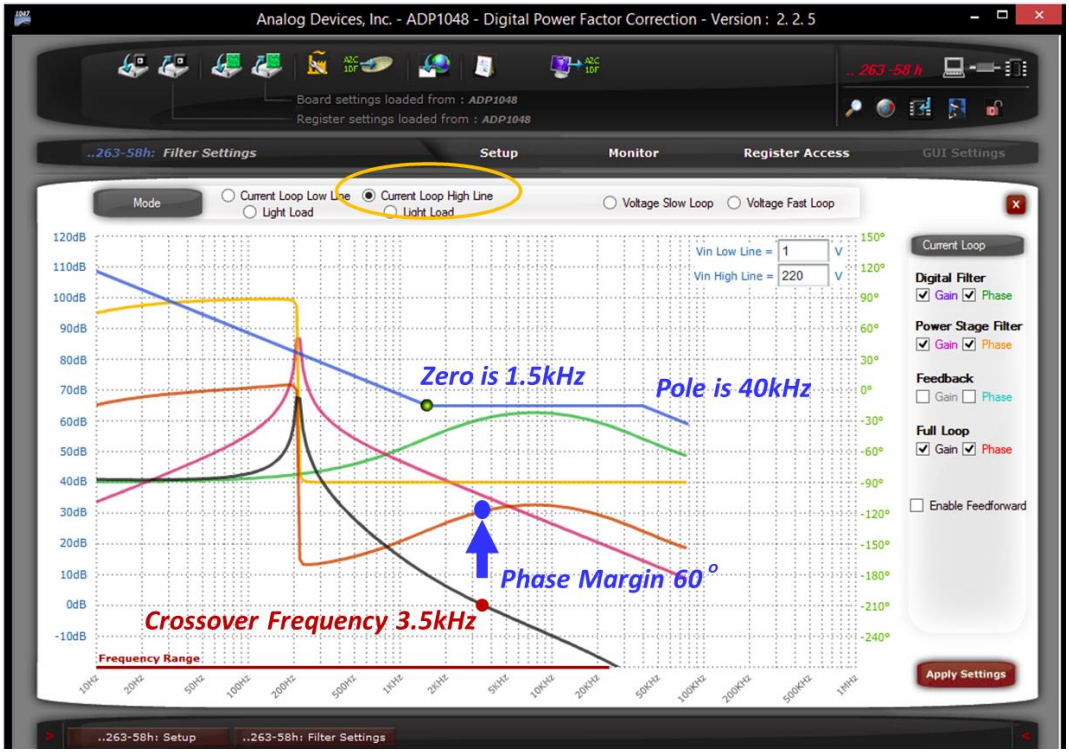


Figure 4.19 Current Loop Compensator Design for High Line

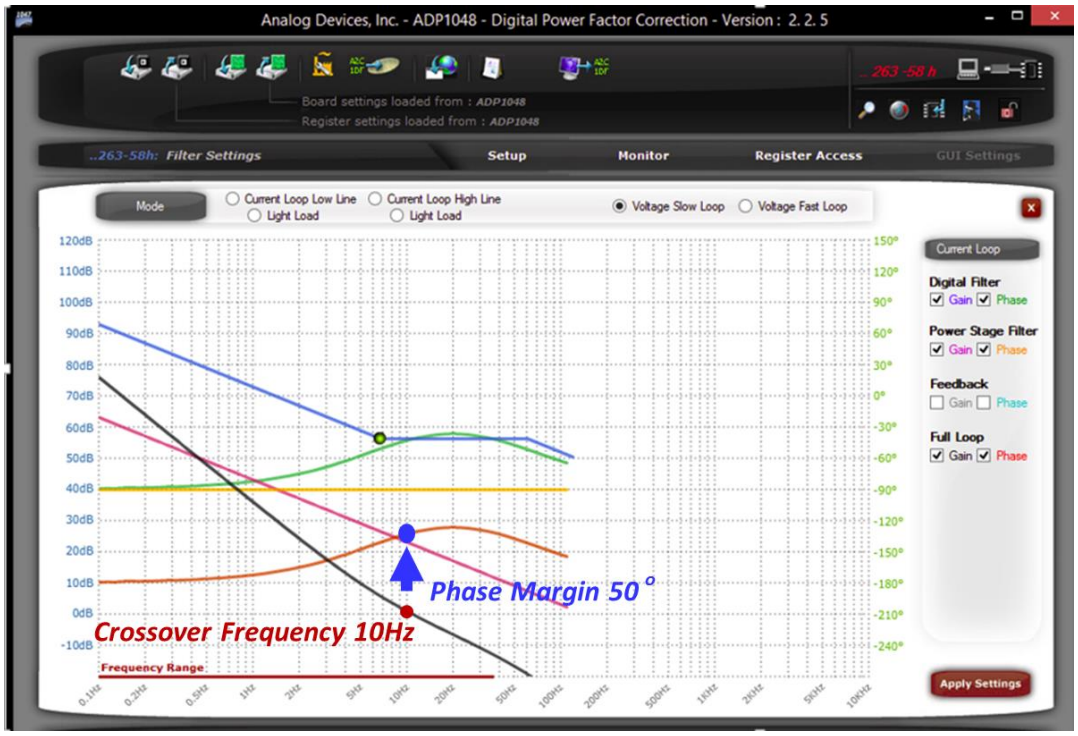


Figure 4.20 Voltage Loop Compensator Design

Chapter 5:

Experiment Setup and Results

5.1 Experiment Setup

The 1.5 kW totem-pole PFC prototype based on ADP1048 controller is shown in Figure 5.1. The major components in the prototype are selected as shown in Table 5.1. The testing condition is 110V low line input voltage at 60Hz line frequency as shown in

Table 5.2. The test results include input voltage and current waveform, PF values, efficiency, harmonic and THD.

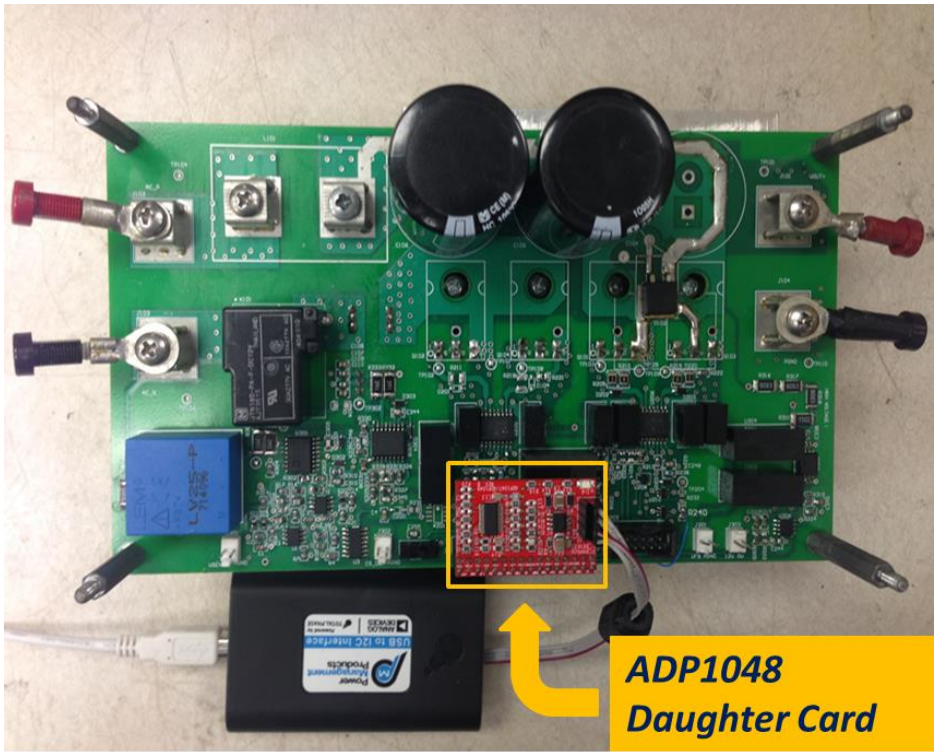


Figure 5.1 Test-bed hardware prototype.

Table 5.1 Experiment Major Components

Components	Model Number/Value	Quantity
SiC Schottky Diode	IDK10G65C5	2
Power Switch	IGW40N65H5	2
Bridge Diode	FFH60UP60S3	2
(or)Bridge MOSFET	IPW65R019C7	2
Inductor	58195A2	3
Capacitor	560uF/450V	2
Controller	ADP1048	1
Driver	Si8233	2
Current Sensor	LAH25-NP	1
Voltage Sensor	LV25-P	1

Table 5.2 Testing Conditions

Rated Power	1.5 kW
Grid Voltage	110 *V/220V*
Grid frequency	60 Hz
Onput Voltage	400 V
Switching frequency	80 kHz

The test equipment are listed in Table 5.3:

Table 5.3 Experiment Equipment

Equipment	Model
Oscilloscope	Lecroy 104Mxs-B
DC Electronic Load	BK Precision 8526
Digital Power Meter	Yokogawa WT1600

5.2 Measurement Data

The output power versus the efficiency curve is shown in Figure 5.2.

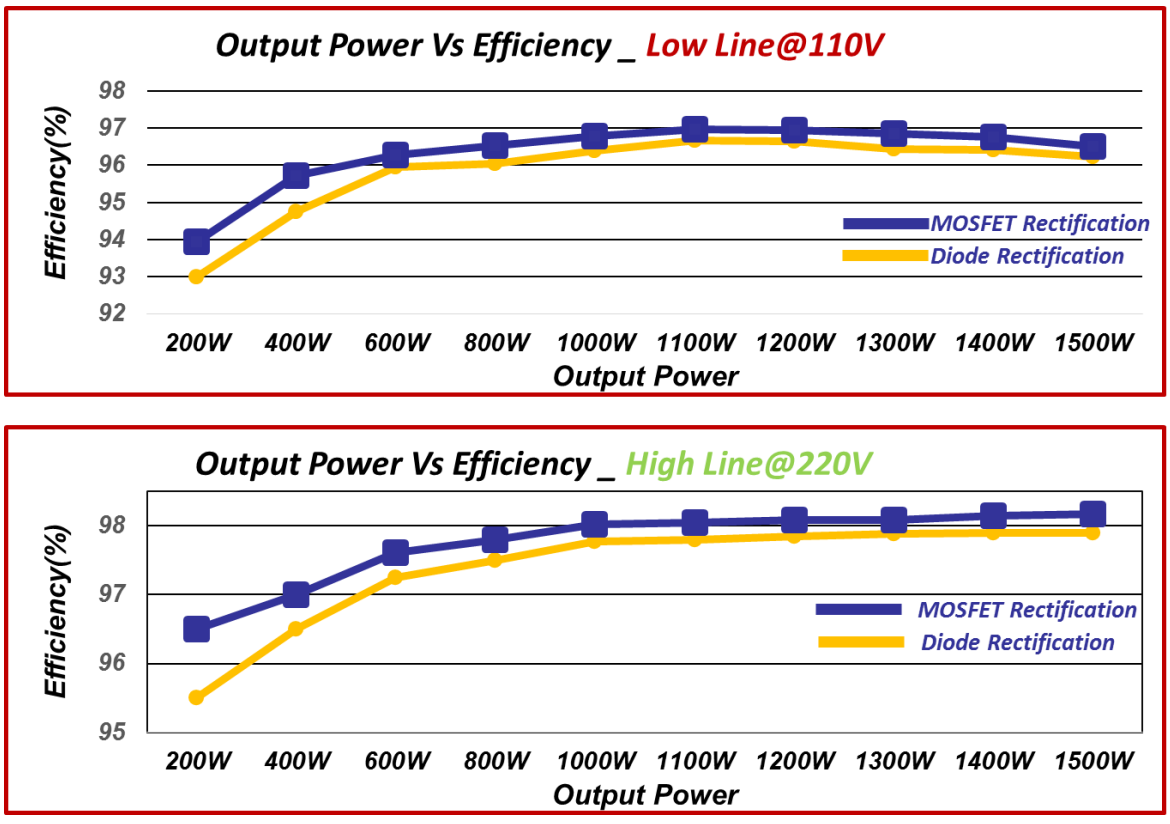


Figure 5.2 Output Power Vs Efficiency Curve

The Figure 5.3 shows the output power versus the power factor. At high power level, the power factor almost equal to 1.

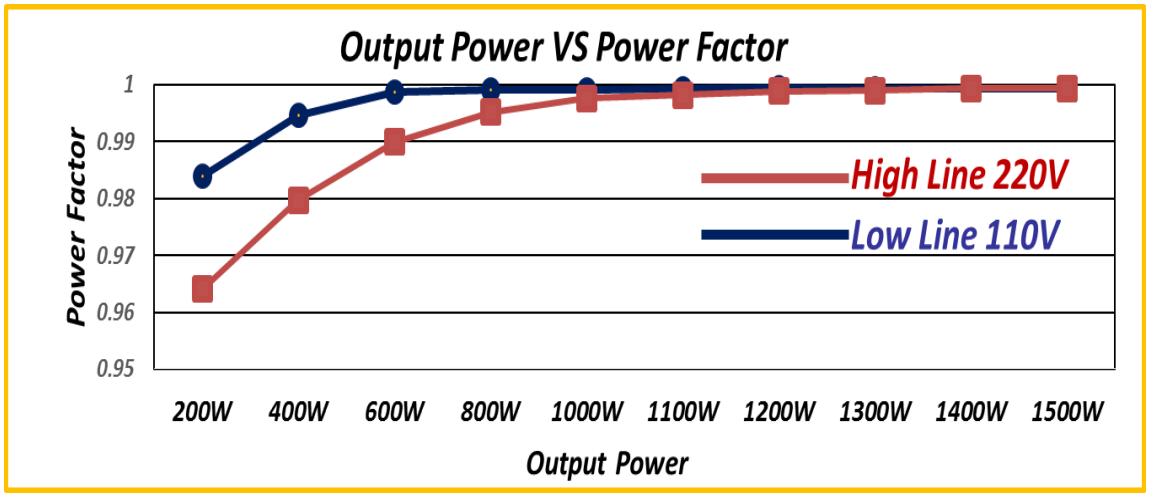


Figure 5.3 Output Power Vs Power Factor Curve

PF and input current harmonic and THD value are the major reference for evaluating the current quality. When the power level is lower which means the input current is smaller, the sensing current signal has higher error with the current reference. This will cause higher THD value. Figure 5.4 shows the THD versus different power level. Figure 5.5 shows the THD analysis based on Yogakawa digital power meter WT1600. Figure 5.6 shows the 1.5kW output power condition 3rd order to 13rd harmonic compared to the EN61000-3-2 class A level [40].

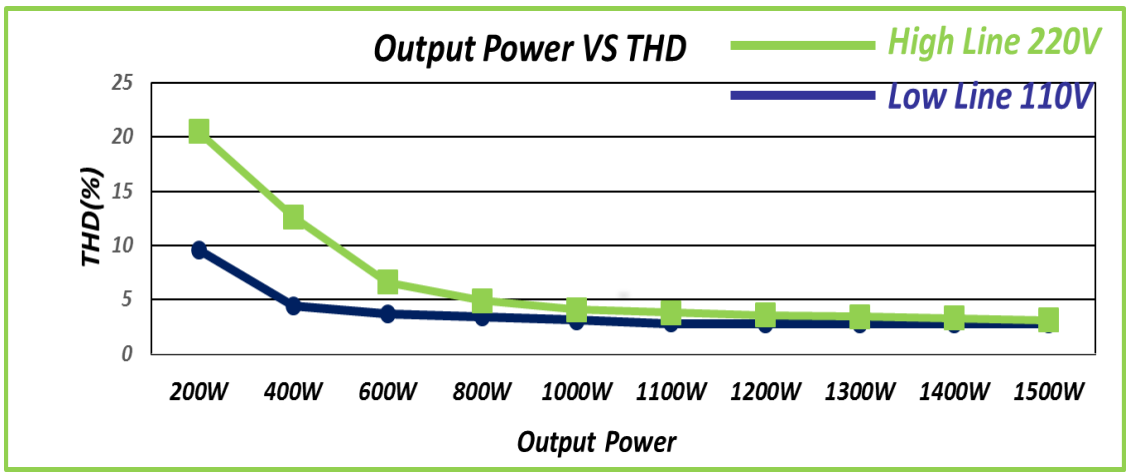
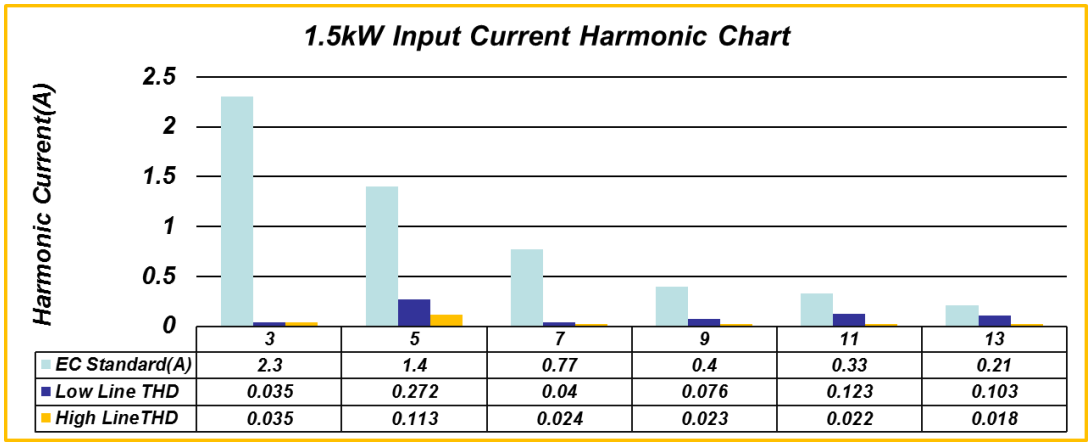


Figure 5.4 THD under different power level

Figure 5.5 THD shown in Yogakawa digital power meter



	3	5	7	9	11	13
EC Standard(A)	2.3	1.4	0.77	0.4	0.33	0.21
Low Line THD	0.035	0.272	0.04	0.076	0.123	0.103
High LineTHD	0.035	0.113	0.024	0.023	0.022	0.018

Figure 5.6 1.5 kW Input Current Harmonic

Figure 5.7 shows the ADP1048 Monitor Interface providing real-time working status.

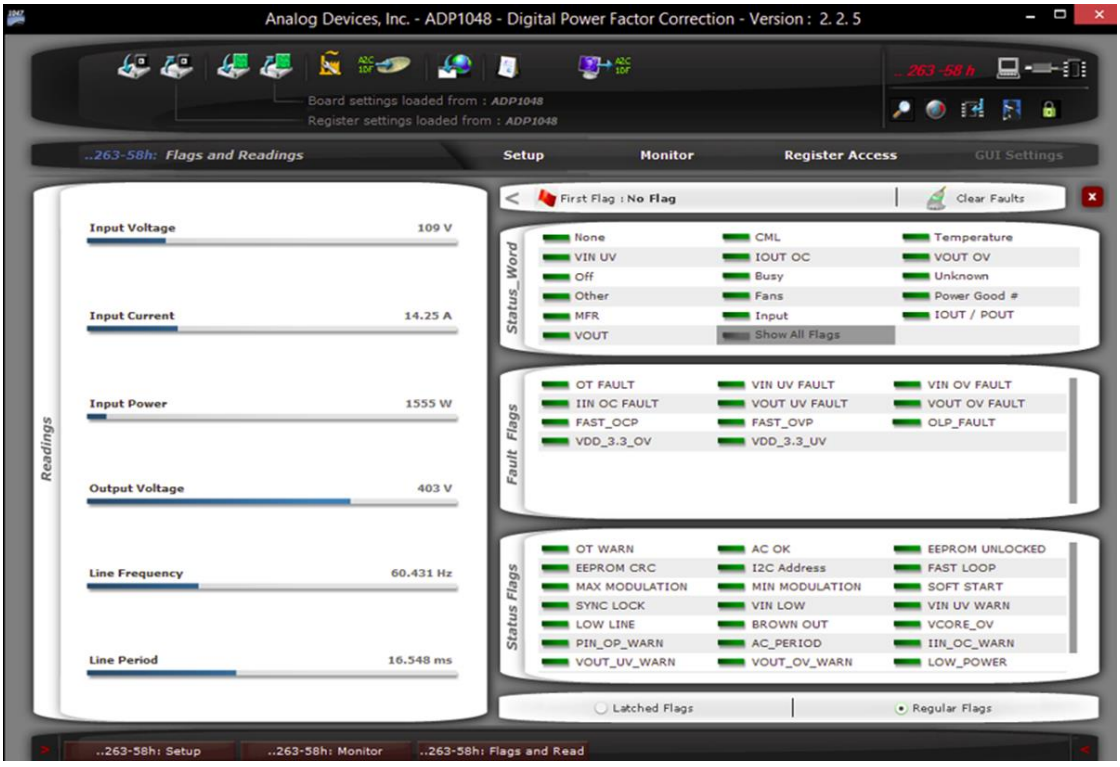


Figure 5.7 1500W Testing ADP1048 Monitor at 110V input

Figure 5.8, Figure 5.9 and Figure 5.10 are input voltage and input current waveforms at 1500W, 1000W and 500W power level with 110V input voltage.

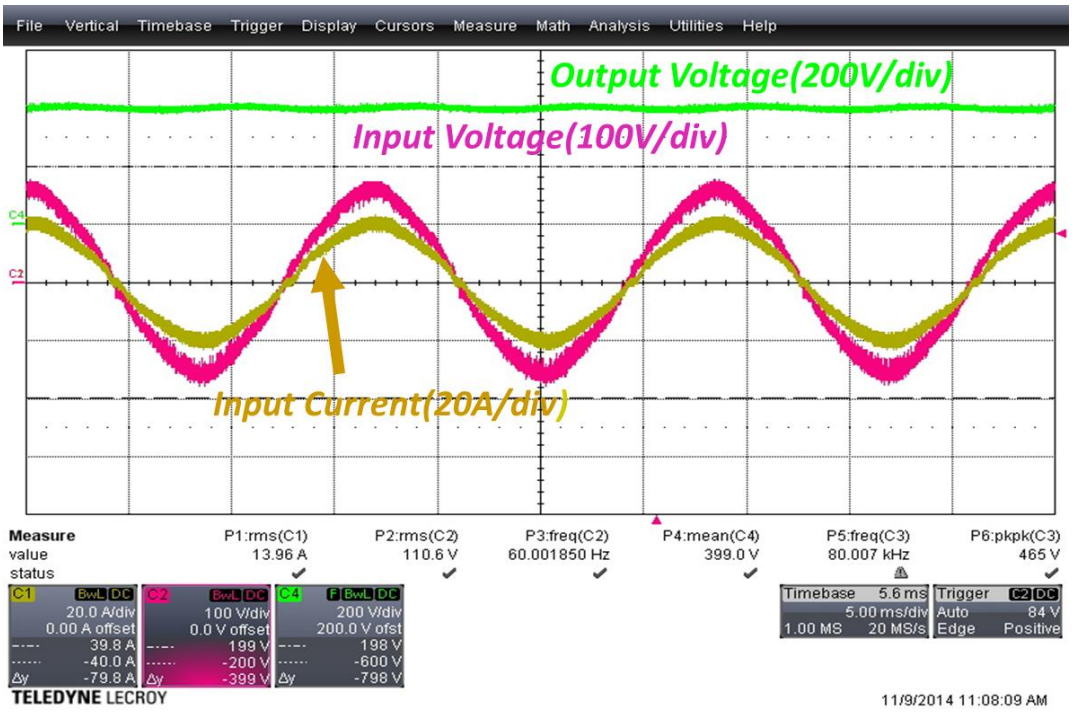


Figure 5.8 1500W Testing Waveform at 110V input

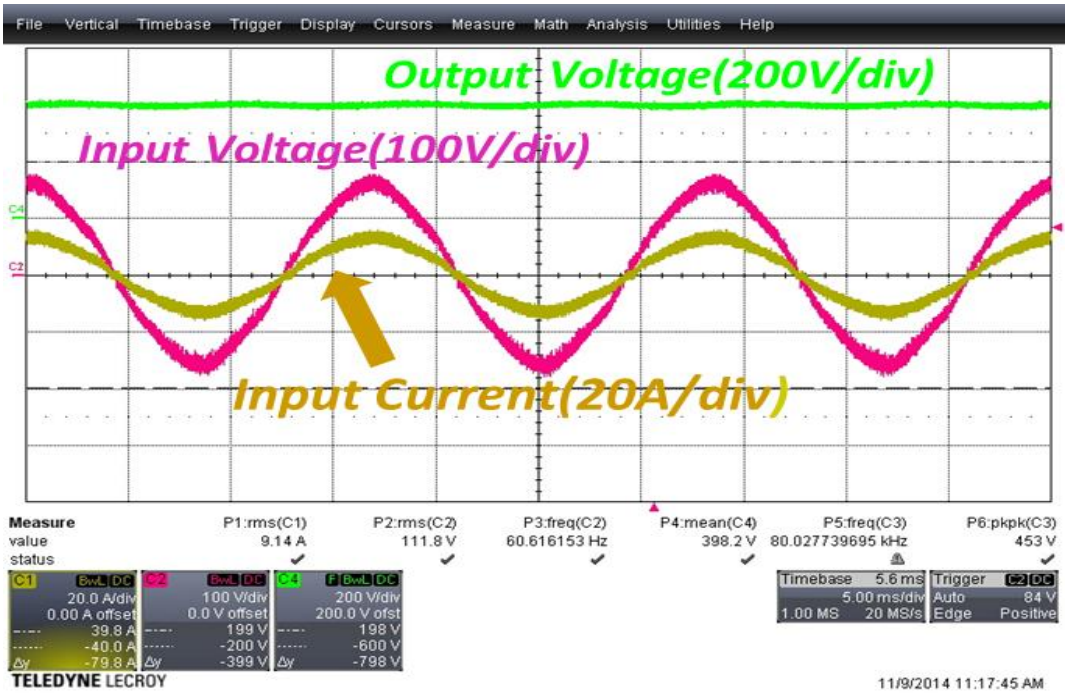


Figure 5.9 1000W Testing Waveform at 110V input

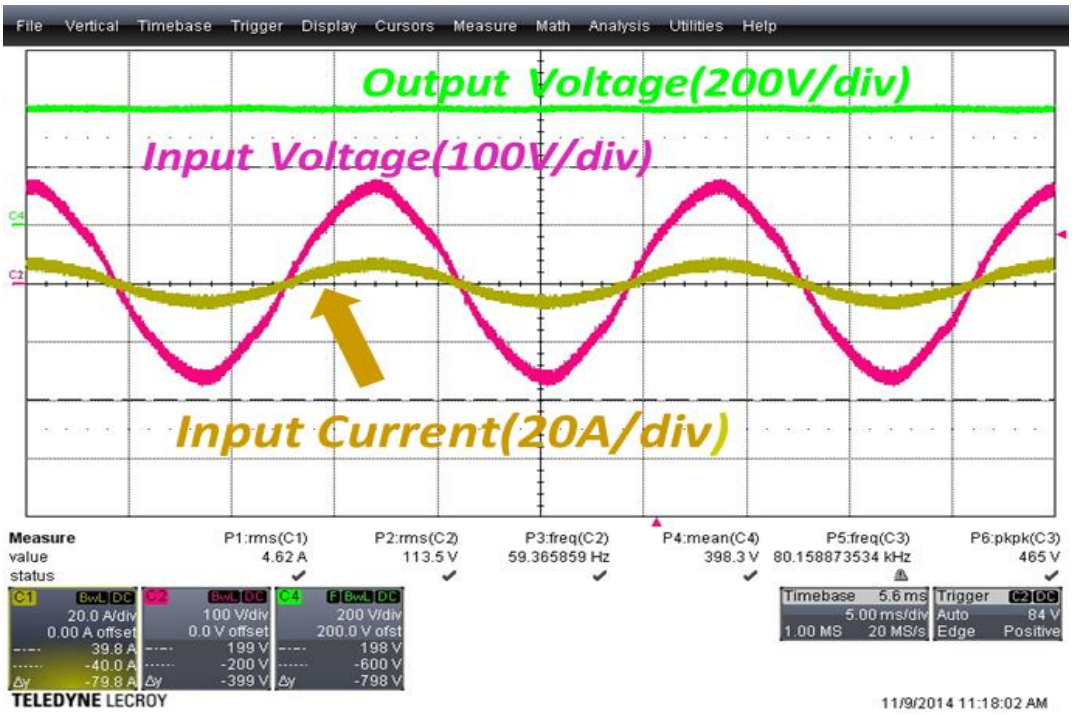


Figure 5.10 500W Testing Waveform at 110V input

Figure 5.11, Figure 5.12 and Figure 5.13 are input voltage and input current waveforms at 1500W, 1000W and 500W power level with 220V input voltage. All the three different power level waveforms use the same current and voltage loop compensator. When high line low power, the current is very small and the error between sensing current and current reference is larger. Therefore, the high line low power has high THD results and current waveform is not good as high power condition.

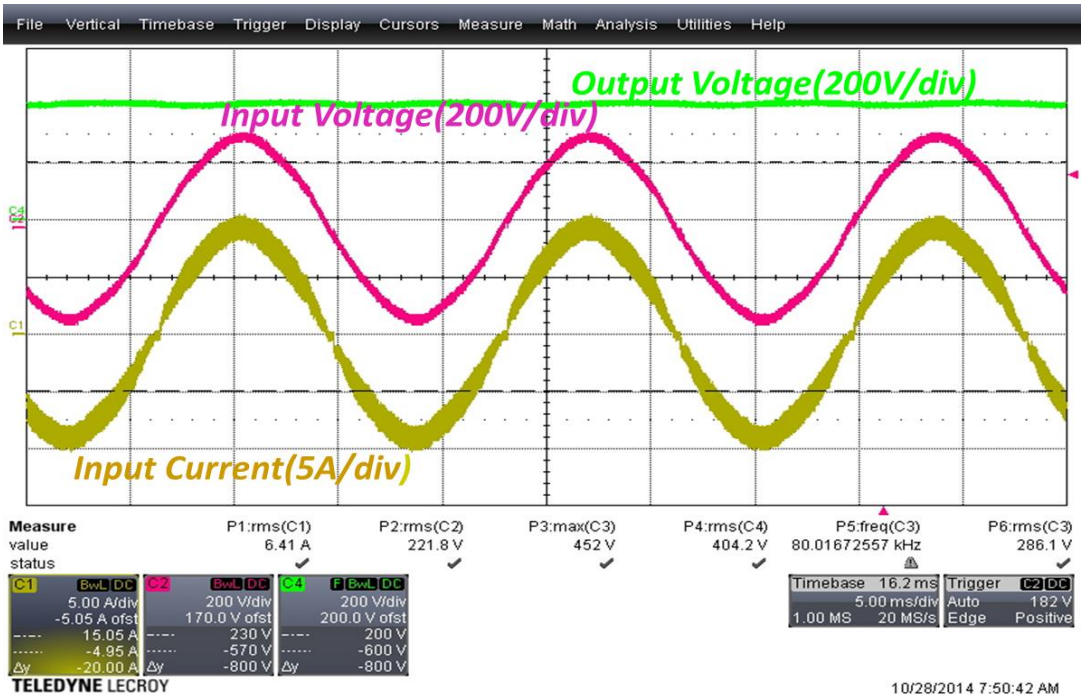


Figure 5.11 1500W Testing Waveform at 220V input

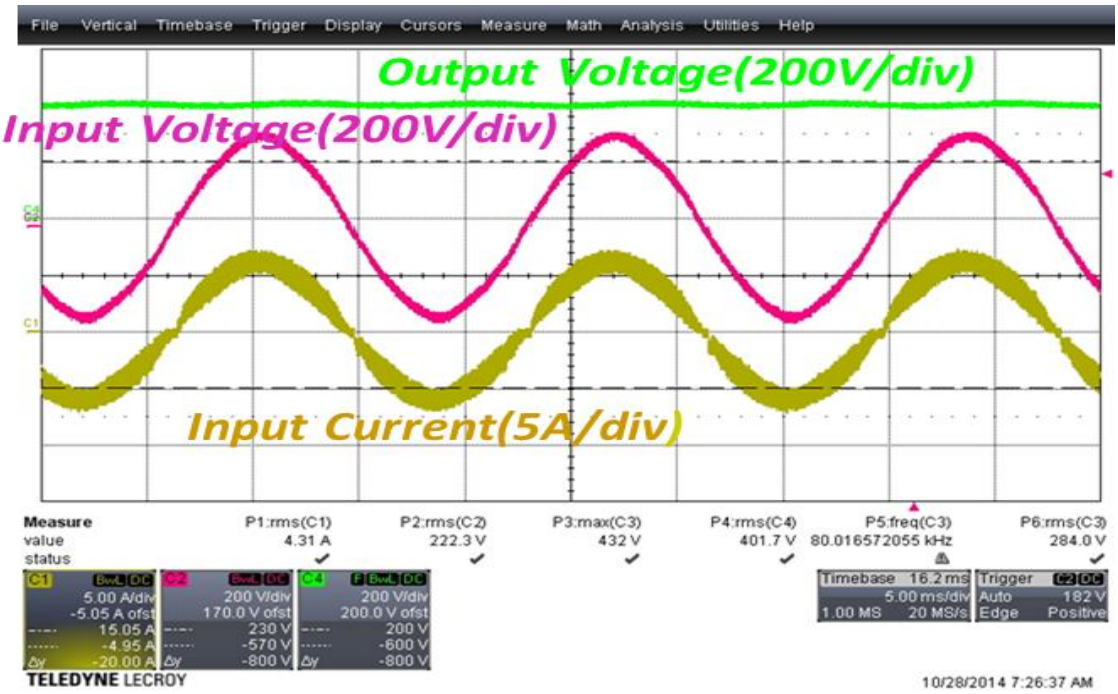


Figure 5.12 1000W Testing Waveform at 220V input

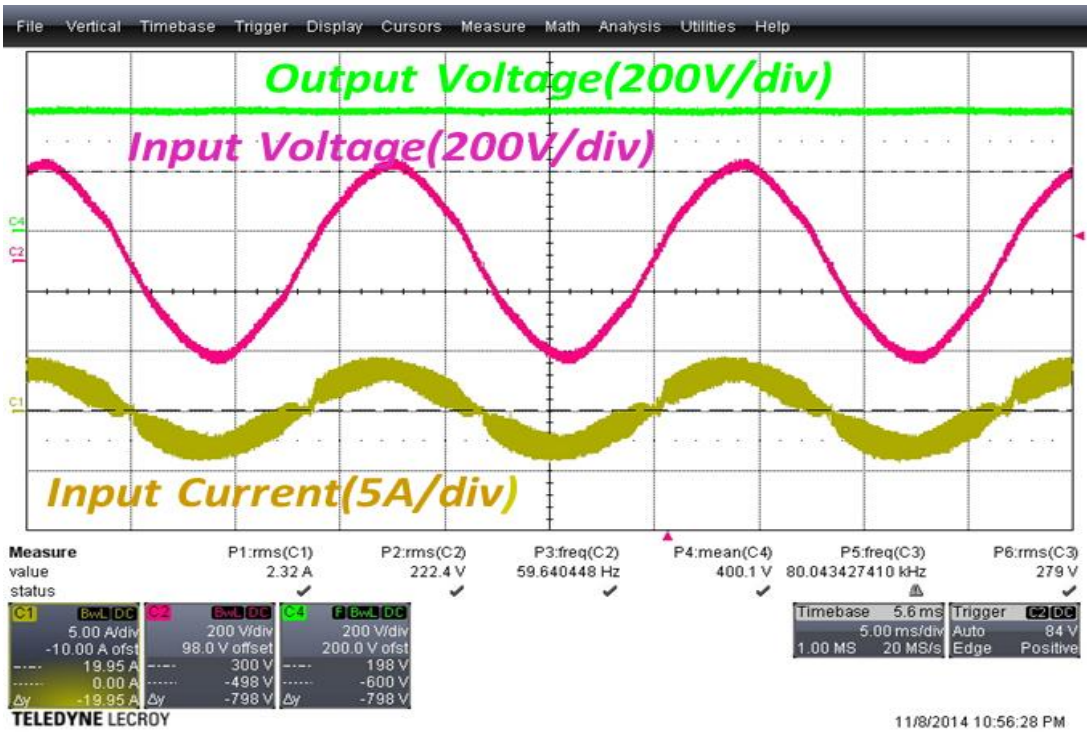


Figure 5.13 500W Testing Waveform at 220V input

Chapter 6:

Summary and Future Work

6.1 Summary

The thesis first introduces the basic knowledge of PFC and compares the characteristics of different bridgeless boost PFC. After discussing the inherited limitation of the totem pole PFC, the method of using ultra-fast IGBT combined with *SiC* diode to replace MOSFETs is discussed.

The operation modes for the CCM totem- pole PFC are analyzed. For the high power PFC, average current control method is implemented. Based on the average current control theory, the current loop and voltage loop compensator is designed and verified by simulation.

In order to further boost the efficiency, the slow diode are replaced by the MOSFET. However they introduce a huge ring on the MOSFET from drain to source during the zero crossing if IGBT and MOSFETs are turned on at same time. The phenomenon is analyzed and the issued is solved by turning on MOSFETs later than IGBT for several switching cycles.

To verify the method for the CCM totem-pole PFC, a 1.5 kW PFC with ADP1048 control is designed and tested. Some external circuits are designed to make the PWM signals from ADP1048 are suitable for totem-pole PFC. The GUI design of ADP is friendly and simple, which help reduces the design cycle for engineers.

Both high line and low line input voltages at 60Hz line frequency are tested with 400V output voltage. The maximum load current is 3.75A and the efficiency at low line achieves 96.7% and high line at 98.2%.

The PFC is working with good performance which has very low THD, unity PF value and high efficiency. The testing results verify the method for totem-pole PFC is suitable for high power CCM condition with ADP1048 digital controller.

6.2 Novelty of Work

- A method using ultra-fast IGBT and SiC diode to replace the mosfet for solving CCM Totem-pole PFC reverse recovery issue is verified
- Provide a method to solve mosfet rectification voltage ring issue at zero crossing
- Implement ADP1048 in totem pole PFC application by adding circuit

6.3 Future Work

- Optimize the design to achieve higher efficiency
- Extend this totem-pole topology to bidirectional EV charger application

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