Stability Analysis of Three-phase AC Power Systems Based on Measured D-Q Frame Impedances

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ABSTRACT

Small-signal stability is of great concern for distributed power systems with a large number of regulated power converters. These converters are constant-power loads (CPLs) exhibit a negative incremental input resistance within the output voltage regulation bandwidth. In the case of dc systems, design requirements for impedances that guarantee stability have been previously developed and are used in the design and specification of these systems. In terms of three-phase ac systems, a mathematical framework based on the generalized Nyquist stability criterion (GNC), reference frame theory, and multivariable control is set forth for stability assessment. However, this approach relies on the actual measurement of these impedances, which up to now has severely hindered its applicability. Addressing this shortcoming, this research investigates the small-signal stability of three-phase ac systems using measured *d-q* frame impedances. Prior to this research, negative incremental resistance is only found in CPLs as a results of output voltage regulation. In this research, negative incremental resistance is discovered in grid-tied inverters as a consequence of grid synchronization and current injection, where the bandwidth of the phase-locked loop determines the frequency range of the negative incremental resistance behavior, and the power rating of inverter determines the magnitude of the resistance. Prior to this research, grid synchronization stability issue and sub-synchronous oscillations between grid-tied inverter and its nearby rectifier under weak grid condition are reported and analyzed using characteristic equation of the system. This research proposes a more design oriented analysis approach based on the negative incremental resistance concept of grid-tied inverters. Grid synchronization stability issues are well explained under the framework of GNC. Although stability and its margin of ac system can be addressed using source and load impedances in *d-q* frame, method to specify the shape of load impedances to assure system stability is not reported. This research finds out that under unity power factor condition, three-phase ac system is decoupled. It can be simplified to two dc systems. Load impedances can be then specified to guarantee system stability and less conservative design.

To Prof. Dr. Jinjun Liu

To China Scholarship Council

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Chapter 1 Introduction

1.1 Background

Instability was found in aircraft dc power system in the 1950's. There have been occasions when energizing a particular inverter has produced an unstable system [1]. In the 1960's, instability was found in the 400 Hz electric power system on board US aircraft carries. A large number of line voltage regulatgors were installed at the aircraft electric service stations to eliminate voltage losses due to long cables. Upon energization of all the regulators, the ship power system went into unstable condition [3]. It was found that the instability is from negative incremental input resistance at power input port of switching-mode regulator, amplifier, dc-dc converter, or dc-ac inverter [5]. Instability can be avoid by reducing the regulation bandwidth of the voltage regulator to decrease the effect of the negative incremental input resistance. From that time, the designers of distributed power system (DPS) with ac and dc subsystems, as shown in Fig. 1-1, on various platforms, such as spacecraft [6], space station [7]–[10], more electric aircraft [11]–[14], automotive system [15], ships [16]–[18], and microgrid [19]–[23], have all paid close attention to the negative incremental input resistance of regulated converter loads and its effect on system stability.

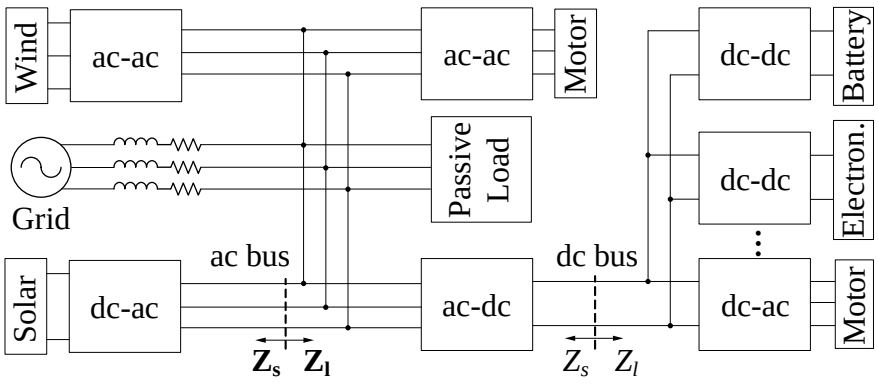


Fig. 1-1. Hybrid ac/dc distributed power system.

Negative incremental resistance is usually believed due to constant power loads (CPLs) behavior of power converters. The fast progress of power semiconductors, especially the wide-bandgap devices [24], [26], [27], enables high switching frequency (over MHz) and high efficiency[25]–[27] (over 99%) power conversion techniques. With high switching frequency, regulation bandwidth of power converters can easily reach 1 to 100 kHz range. With a constant output current, high-bandwidth voltage regulation leads to constant output power. When combined with high conversion efficiency, this results constant input power characteristic. These converters are then called CPLs. There input impedances freatures negative incremental resistance [28].

The stability of power systems nonetheless is often analyzed using eigenvalues, which are extracted from the system matrix "A" of the canonical state space model representation of the system in question [29]. This approach requires the use of full dynamic models for all the elements in the system, including physical and control parameters. As such, DPS integrators need to manage an enormous amount of information to derive these models; from converter topologies, to circuit parameters, to control strategies, information that must also be updated every time any of the components changes in the system. Naturally, the system model needs to be derived again too. Using this approach, the sharing of proprietary information from different system component vendors is not feasible, ultimately impeding the proper modeling of the system.

Loop gain is also a useful stability analysis tool for analog circuit with feedback control system [32]–[34]. When the phase margin of the loop gain is positive, then the feedback system is stable. Moreover, increasing the phase margin (could be more than 60 °) causes the system transient response to be better behaved, with less overshoot and ringing. Loop gain can be measured.

However, both eigenvalue and loop gain based stability analysis need information of components' inner physical structure and parameters which usually are not available for system integrator. When components in the system are acquired as "black boxes" for use

in bigger electrical system to deliver power from source to load, it may be found that the system oscillates or becomes unstable because the particular source or load impedances were not foreseen by the components' designers; or, the components may have inadequate input or output filters, so the system integrator has to provide external filters which in turn may cause the system to oscillate. Under such condition, it is difficult to use eigenvalue and loop gain based analysis.

As a more practical alternative to the above methods, impedance-based stability analysis as previously mentioned has been successfully used in dc systems for a long time [31], where the stability at each interface is determined using measured impedances and Nyquist stability criterion. The main advantage of this approach is that the measured impedances intrinsically model all circuit components, including physical components and control systems. Stability criteria can be formulated then by establishing forbidden regions in the complex plane where the locus of possible source and load impedance ratios cannot reside thus ensuring a stable operation [35]–[38]. This allows for new loads to be added to the system easily without knowing their internal parameters and without requiring the re-modeling of the whole system to assess its impact on the system stability. This approach is widely used in design of various dc DPSs, such as spacecraft [6], space station [7]–[10], more electric aircraft [13], automotive system [15], ships [16]–[18], and dc microgrid [21].

In terms of three-phase ac systems, negative incremental resistance of CPLs are also found at the input port of ac-dc converters [3], [39]. Similar impedance-based stability analysis are formulated in a mathematical framework based on the generalized Nyquist stability criterion (GNC), reference frame theory, and multivariable control is set forth for stability assessment [3].

1.1.1 Impedance-based dc system stability analysis

The negative input resistance can be shown to be the result of two properties of power converters, namely the high regulation bandwidth and high efficiency. It is assumed that

the output voltage v_o of the dc-dc converter shown in Fig. 1-2 is maintained constant by the feedback regulator. If the load current does not change, then P_o is constant. With the high efficiency of dc-dc converter, P_i is also constant, even if the input voltage v_{dc} varies. It follows that if v_{dc} increases, i_{dc} must decrease. Consequenctly, the regulator exhibits a negative incremental input resistance as show in Fig. 1-3. Incombination with the input filter or the source converter, the negative input resistance can under certain condition constitute a negative resistance oscillator, and is the origin of the system potential instability.

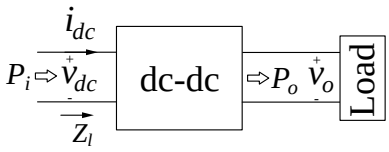


Fig. 1-2. Dc-dc converter.

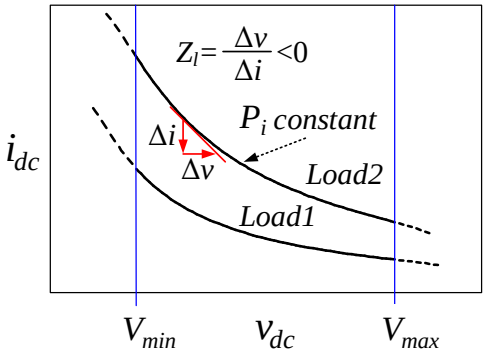


Fig. 1-3. Static input characteristic of dc-dc converter.

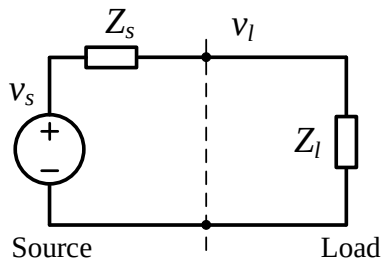
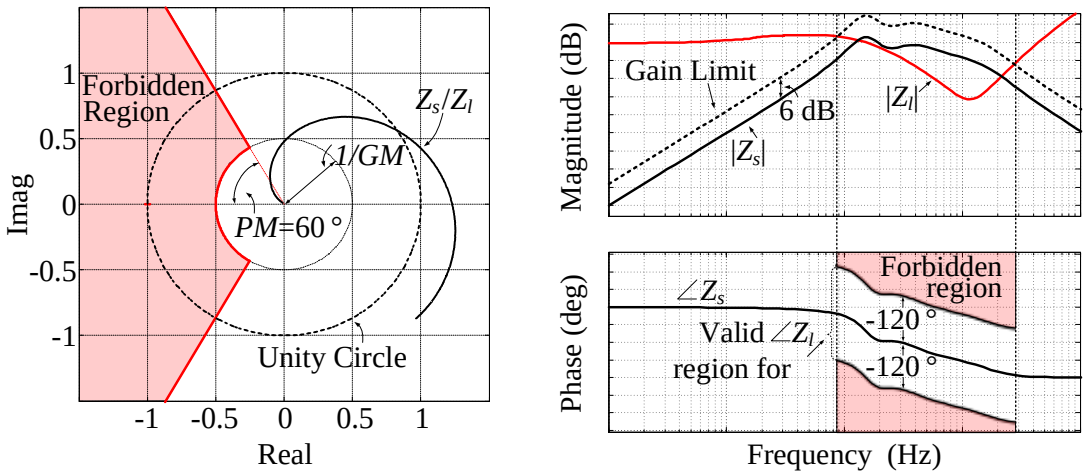


Fig. 1-4. Small-signal representation of a dc system.

For dc system, once the system is partitioned to source and load subsystems at an interface (see Fig. 1-4), stability of the system can be predicted by applying Nyquist stability criteria to the minor loop-gain ($L=Z_s/Z_l$) [28] that is defined by output impedance (Z_s) of the source subsystem and the input impedance (Z_l) of load subsystem. Using this concept, one possible design procedure for the dc subsystem in DPS shown in Fig. 1-1 is to design the source converter (ac-dc converter in Fig. 1-1) using an unterminated modeling approach [40]. Then, based on the output impedance characteristics of the source converter, specification for the input impedance of load subsystem can be defined to ensure the system stability. Ref. [31] proposes to keep the minor loop-gain loci inside the unity circle on the complex plane, so that it never encircles the critical point (-1,0), and the system is stable (if there's no right half plane (RHP) pole). Transform to impedance of the system, this concept force the magnitude of the input impedance of the load subsystem to be larger than the magnitude of the output impedance of the source subsystem [31]. However, this concept leads to too conservative impedance specification and bulky input filter for the load subsystem.

To know how stable the system is or how much uncertainty the system design can take, phase margin (PM) and gain margin (GM) are defined as pointed out in Fig. 1-5 (a). Ref. [35] proposes a forbidden region concept based on desired PM and GM, as shown in Fig. 1-5 (a), on the complex plane out of which the minor loop-gain shall stay. (Actually, concept from Ref. [31] is also a forbidden region concept that is the region outside the unity circle.) The forbidden region shown in Fig. 1-5 (a) can be also transformed to load impedances (Z_l) specification on the Bode plot. As shown in Fig. 1-5 (b), under the

frequency range where the magnitude of the load impedance ($|Z_l|$) is higher than the Gain Limit, which is magnitude of source impedance ($|Z_s|$) plus the GM, there will be no limitation for the phase of load impedance ($\angle Z_l$). However, $\angle Z_l$ should stay inside its valid region (see Fig. 1-5 (b)) in the frequency range where $|Z_l|$ is smaller than the Gain Limit. Compare with the concept proposed by Ref. [31], this forbidden region concept is less conservative. It allows minor loop-gain loci goes to the outside of unity circle, which means $|Z_l|$ is bigger than $|Z_s|$, but ensure the system stability with certain margin. Since then, different forbidden region concepts were proposed [36]–[38], and they can be transformed to certain load impedance specifications. This is a convenient and useful tool for DPS integrators. Based on the output impedance of source converter, shapes of the input impedance of load converters can be specified for the suppliers. In this way, not only the information from suppliers can be protected, but also the system stability can be assured when source and load are connected by the integrator. This also allows new loads to be added to the system easily without knowing their internal parameters and without requiring the re-modeling of the whole system to assess its impact on the system stability.



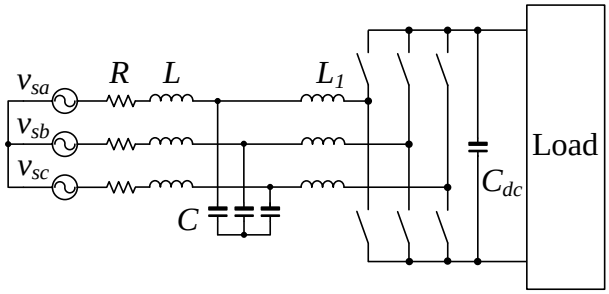
(a) (b)

Fig. 1-5. (a) Polar plot of minor loop-gain; (b) Bode plot of source and load impedances.

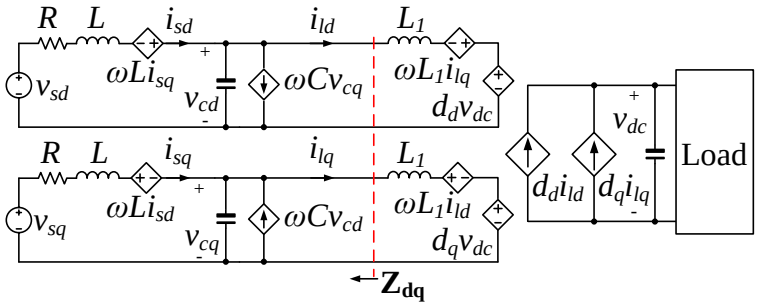
1.1.2 Impedance-based ac system stability analysis

Impedance-based small-signal stability analysis for three-phase ac system is usually carried out in *d-q* frame by doing transformation (Eq. (1-1)) from stationary (*abc*) frame [3], [41]. This is because, in *abc* frame, there is no equilibrium point exits for small-signal linearization. In *d-q* frame, balanced three-phase ac system (see Fig. 1-6 (a), in which three-phase boost rectifier is used as an example) becomes two coupled dc systems (see Fig. 1-6 (b)). Small-signal model of the system can be extracted using traditional linearization method.

$$\begin{bmatrix} x_d \\ x_q \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos(\theta) & \cos\left(\theta - \frac{2}{3}\pi\right) & \cos\left(\theta + \frac{2}{3}\pi\right) \\ -\sin(\theta) & -\sin\left(\theta - \frac{2}{3}\pi\right) & \sin\left(\theta + \frac{2}{3}\pi\right) \end{bmatrix} \cdot \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \tag{1-1}$$



(a) Three-phase boost rectifier in *abc* frame.



(b) Average model of boost rectifier in d-q frame.

Fig. 1-6. Average models of boost rectifier.

Different from impedances of dc-dc converters, impedances of three-phase ac converters are 2×2 matrices as shown by Eq. (1-2). This is due to the coupling effect between *d*-axis and *q*-axis.

$$\mathbf{Z}_{\mathbf{dq}}(s)=\begin{bmatrix} Z_{dd}(s) & Z_{dq}(s) \\ Z_{qd}(s) & Z_{qq}(s) \end{bmatrix} \tag{1-2}$$

In ac system, the negative resistor behavior is observed in the Z_{dd} element of the rectifier (Fig. 1-6 (b)) input impedance that also acts as a constant power load [39], as a result of which instability can be induced in the ac system due to the negative resistance of Z_{dd}.

Similar to dc system, the balanced three-phase ac system can be then presented by source and load subsystems as shown in Fig. 1-7.

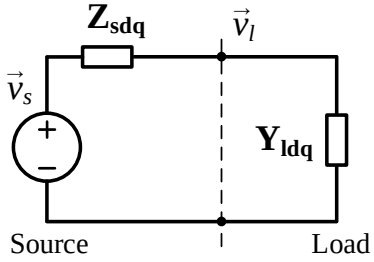


Fig. 1-7. Small-signal representation of a balanced three-phase system in *d*-*q* frame.

Similar to dc system, the interface voltage ($\vec{v}_l$) can be derived as Eq. (1-3). Minor loop-gain is defined as Eq. (1-4), which is the ratio between source and load impedances in *d*-*q* frame.

$$\vec{v}_l(s)=\left[\mathbf{I}+\mathbf{Z}_{\mathbf{sdq}}(s)\mathbf{Y}_{\mathbf{ldq}}(s)\right]^{-1}\vec{v}_s(s) \tag{1-3}$$

$$\mathbf{L}(s)=\mathbf{Z}_{\mathbf{sdq}}(s)\mathbf{Y}_{\mathbf{ldq}}(s) \tag{1-4}$$

As reported by Ref. [3], the condition for balanced three-phase ac system stability can be determined by applying generalized Nyquist stability criterion (GNC) [42] or generalized inverse Nyquist stability criterion (GINC) [43] to the minor loop-gain **L**(*s*).

Let $\{l_1(s), l_2(s),\ldots,l_m(s)\}$ be the set of frequency-dependent eigenvalues of **L**(*s*), which can be find using Eq. (1-5) to (1-7). Thses eigenvalues trace in the complex plane the characteristic loci of matrix **L**(*s*) as the variable *s* traverses the standard Nyquist contour in the clockwise direction. Then the generalized Nyquist stability criterion can be formulated as:

"Let the multivariable system shown in Fig. 1-7 have no open-loop unobservable or uncontrollable modes whose corresponding characteristic frequencies lie in the right-half plane. Then the system will be closed-loop stable if and only if the net sum of anticlockwise encirclements of the critical point (–1+j0) by the set of characteristic loci of **L**(*s*) is equal to the total number of right-half plane poles of $\mathbf{Z}_{\mathbf{sdq}}(s)$ and $\mathbf{Y}_{\mathbf{ldq}}(s)$."

The generalized inverse Nyquist stability criterion can be formulated as:

"Let the multivariable system shown in Fig. 1-7 have no open-loop unobservable or uncontrollable modes whose corresponding characteristic frequencies lie in the right-half plane. Then the system will be closed-loop stable if and only if the net sum of anticlockwise encirclements of the critical point (–1+j0) by the set of inverse characteristic loci (reciprocal of each of the numbers $\{l_1(s), l_2(s),\ldots,l_m(s)\}$ in the complex plane) of **L**(*s*) is equal to the total number of right-half plane zeros of $\mathbf{Z}_{\mathbf{sdq}}(s)$ and $\mathbf{Y}_{\mathbf{ldq}}(s)$."

$$\mathbf{L}(s)=\mathbf{Z}_{\mathbf{sdq}}(s)\cdot\mathbf{Y}_{\mathbf{ldq}}(s)=\begin{bmatrix} Z_{sdd}(s) & Z_{sdq}(s) \\ Z_{sqd}(s) & Z_{sqq}(s) \end{bmatrix}\cdot\begin{bmatrix} Y_{ldd}(s) & Y_{ldq}(s) \\ Y_{lqd}(s) & Y_{lqq}(s) \end{bmatrix} \tag{1-5}$$

$$\mathbf{L}(s)=\begin{bmatrix} Z_{sdd}(s)Y_{ldd}(s)+Z_{sdq}(s)Y_{lqd}(s) & Z_{sdd}(s)Y_{ldq}(s)+Z_{sdq}(s)Y_{lqq}(s) \\ Z_{sqd}(s)Y_{ldd}(s)+Z_{sqq}(s)Y_{lqd}(s) & Z_{sqd}(s)Y_{ldq}(s)+Z_{sqq}(s)Y_{lqq}(s) \end{bmatrix} \tag{1-6}$$

$$\mathbf{C}(s)\cdot\mathbf{L}(s)\cdot\mathbf{C}^{-1}(s)=\begin{bmatrix} \lambda_1(s) & 0 \\ 0 & \lambda_2(s) \end{bmatrix} \tag{1-7}$$

1.2 Motivation and Objective

Prior to this research, the impedance-based stability analysis has been mainly reported using computer simulation using either average or switching models. None of the references discussed above has verified its results using actual *d-q* frame measured impedances because of the difficulty associated with this procedure. Consequently, a significant effort has been devoted to solve this problem; by using current or voltage injection in order to characterize the frequency response of the system [44]–[47], or by investigating the transient response to shorten the measurement process [48], [49]. Ref. [44] is interesting in the sense that it discussed the stability of a three-phase motor drive system; however did it at the interface between the inverter and a resistive load, plotting several frequency points of the generalized Nyquist diagram for this stable case. Stability analysis of ac system with CPLs using measured *d-q* frame impedances has not been reported.

Moreover, synchronism stability issues are not well addressed in the original impedance-based method using GNC [3], [44]. The method is mainly used in the analysis of DPS in aircraft and marine vessels, which only have one or two sources and synchronism issues arise only in certain isolated cases [3]. Historically, ac systems were largely studied for frequency stability especially in the utility industry [50]. A power grid may have hundreds of generators operating at same frequency and therefore synchronism is of utmost importance. Nowadays, More and more voltage source converters (VSCs) are installed to modern power systems. VSCs not only can improve the power utilization efficiency but also are key components to integrate renewable energy sources [51]–[62].

VSCs should also synchronize with the grid. Phase-locked loops (PLLs) [63], [64] are standard techniques for synchronization. Some literatures have reported that PLL has a negative impact mainly in the inverter mode [65]–[67]. Synchronism issues between parallel-connected VSCs with weak grid are also reported [68]. However, influence of PLL on impedances of VSCs is not well discussed, and the synchronism issues caused by PLL is not analyzed using impedance-based method.

Although GNC utilizes minor loop-gain $\mathbf{L}(s)$ defined by source and load impedances matrices. Elements of $\mathbf{L}(s)$ are functions of both self-channel and cross-channel impedances ratios as show in Eq. (1-5) and (1-6). Plus, stability condition is finally judged by eigenvalues of $\mathbf{L}(s)$. If $\mathbf{L}(s)$ is non-diagonal, finding eigenvalues for non-diagonal matrix will involve complicated computation, which makes indirect relationship between system stability condition and impedances. This is the roadblock of doing load impedance specification for ac system in *d-q* frame. Based on the relationship between a matrix's eigenvalues and its singular values, Ref. [69] proposes to limit the minimum singular value of load input impedance matrix to be smaller than the maximum singular value of the source output impedance. This concept is similar as the one in Ref. [28] for dc system, which leads to conservative design. Load impedances specification, which can greatly help system integration, in ac system that allows impedance interaction but still keep the system stable with certain margin is not reported yet.

Addressing these unexplored issues, this research investigates the small-signal stability of three-phase ac systems with CPLs using measured *d-q* frame impedances. Prior to this research, negative incremental resistance is only found in CPLs as a results of output voltage regulation. In this research, negative incremental resistance is discovered in grid-tied inverters as a consequence of grid synchronization. Based on the negative incremental resistance concept of grid-tied inverters, grid synchronization stability issues are well explained under the framework of GNC. Moreover, this research finds out that under unity power factor condition, three-phase ac system is diagonal. It can be simplified to two decoupled dc systems. Load impedances can be then specificed to guarantee system stability and less conservative design.

1.3 Disseration Outline and Summary of Contributions

Three-phase VSCs are basic building blocks for many DPS. Stability issues discussed in this dissertation happen between different types of VSCs. Chapter 2 discusses the small-signal models for different VSCs, such as inverters and rectifiers. Impedances matrices in *d-q* frame are derived based on the results in the literature. Some VSCs need PLL to synchronize with the ac bus, basic PLL structures and models for grid-tied VSCs are also discussed in this chapter.

Chapter 3 presents, for the first time, the small-signal stability analysis of a balanced three-phase ac system with constant power loads based on the GNC and measured impedances in *d-q* frame. The results obtained show how the stability at the ac interface can be easily and readily predicted using the measured impedances and the GNC; thus illustrating the practicality of the approach, and validating the use of ac impedances as a valuable dynamic analysis tool for ac system integration.

Chapter 4 proposes a full analytical model for the output impedance of the three-phase grid-tied VSCs considering the effect of PLL. The result unveils an interesting and important feature of three-phase grid-tied VSCs, namely that its *q-q* channel impedance (Z_{qq}) behaves as a negative incremental resistor for inverter and a positive incremental resistor for rectifier. Moreover, this behavior is a consequence of grid synchronization, where the bandwidth of the PLL determines the frequency range of the incremental resistor behavior, and the power rating of VSCs determines the magnitude of the resistor. In addition, PLL-based active frequency drift islanding detection (AFD) function makes phase of Z_{qq} of grid-tied inverter drops below -180 °, which has worse impact than the negative resistance in the system stability point of view.

Chapter 5 discusses the stability issues caused by PLL dynamics. Due to the PLL dynamics, parallel connected VSCs could lose synchronization under weak grid condition. This issue is well studied in this chapter within the frame work of impedance-based analysis using GNC.

Chapter 6 presented an impedance-based analysis for active frequency drift islanding detection methods. The output impedance of a grid-tied inverter was modeled with PLL-based AFD method. With big feed forward gain N for islanding detection, the phase of Z_{qq} is shown to drop below –180 °. Under islanding condition, the inverter system became unstable with a frequency drift away from steady-state. Based on the impedance of the inverter, it could be concluded that the grid-tied inverter with AFD islanding method has the potential to destabilize the grid-connected inverter system when the grid is weak.

Chapter 7 proposes impedances specification for balanced three-phase ac DPSs. Under unity power factor condition, three-phase ac system is diagonal. It can be simplified to two decoupled dc systems. Load impedances can be then specificed to guarantee system stability and less conservative design.

The last chapter summarizes the work and discusses some possible future work.

Chapter 2 Modeling of Voltage Source Converters

More and more voltage source converters (VSCs) are installed to modern power systems. VSCs not only can improve the power utilization efficiency but also are key components to integrate new energy sources. For example, in the power distribution system with high penetration of power electronics and renewable energy, as shown in Fig. 1-1, three-phase pulse-width modulated (PWM) rectifiers, as shown in Fig. 2-1, which have better efficiency and power quality performance [51], [52], are installed working as active front end (AFE) to replace conventional line-commutated converters for motor drives. Three-phase voltage source inverters (VSIs) with output voltage control, as shown in Fig. 2-2, are installed to provide power to the factory and building when the grid is gone. Grid-tied VSIs with only current controllers are used to delivery power from wind turbines or solar panels to the grid [62].

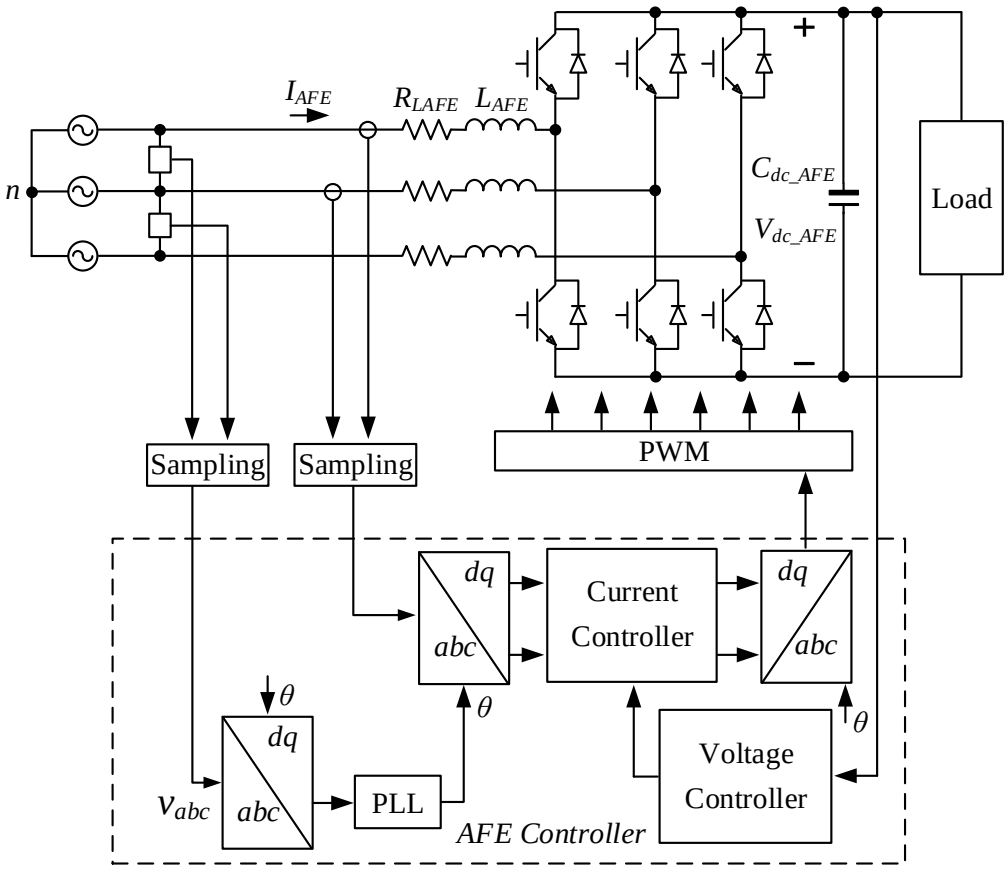


Fig. 2-1. Three-phase boost rectifier.

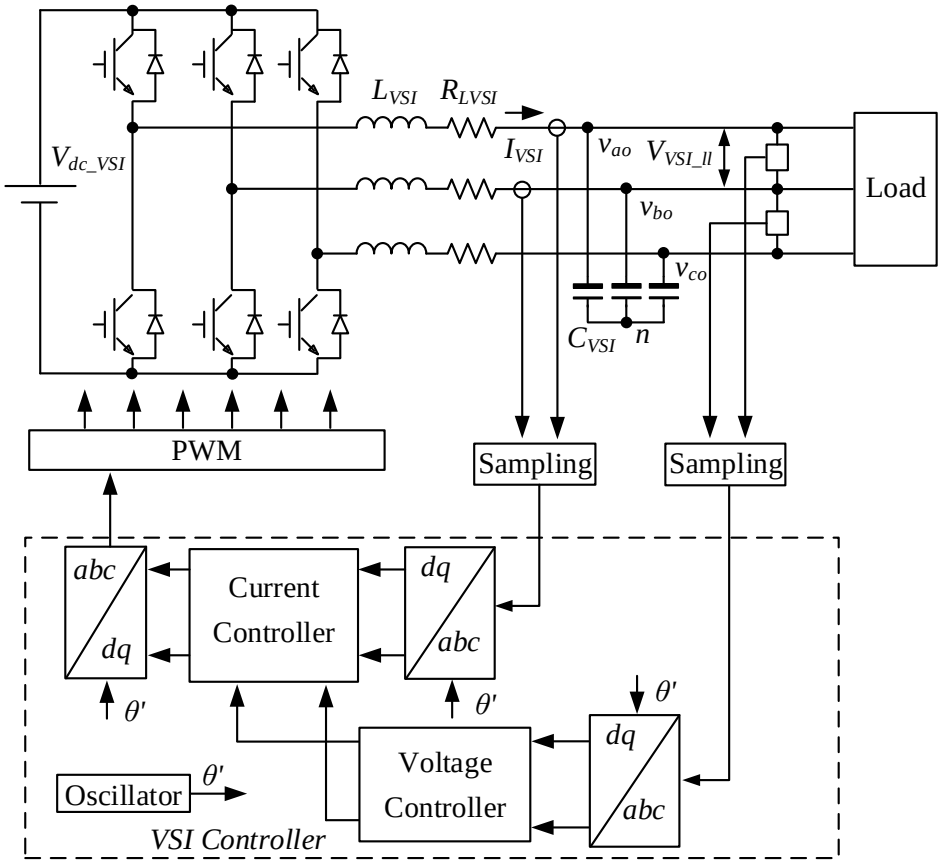


Fig. 2-2. Three-phase VSI with LC filter.

VSCs are time-varing non-linear systems. The stability critera discussed in chapter 1 are tools for linear systems. The task of this chapter is to develop linear models for VSCs, especially output impedances of VSI and input impedances of AFE in *d-q* frame. Some other information which will be referred in the rest of the dissertation, will also be discussed, such as *d-q* impedances measurement and Phase-locked Loop (PLL).

2.1 Small-signal Models of VSCs

Both AFE and VSI consist of a switching network, filtering componetns and feedback control systems. Development of the small-signal models of VSCs begins from the switching network [54].

Switches in Fig. 2-1 and Fig. 2-2 are Insulated-Gate Bipolar Transistor (IGBT) paralleled with diode. For control design and stability analysis, they can be simplified as ideal switches as shown in Fig. 2-3.

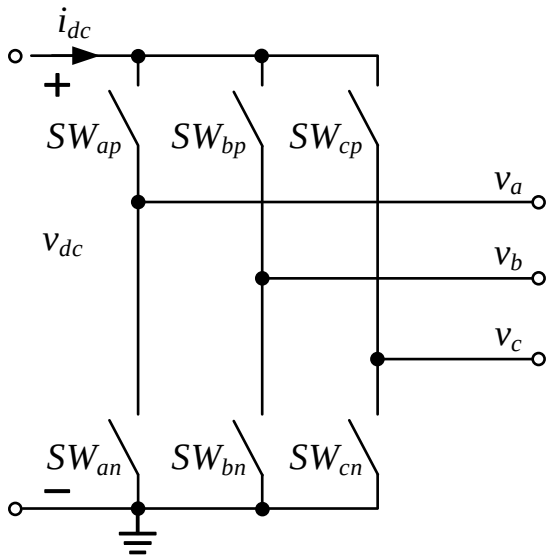


Fig. 2-3. Switching network with ideal swtiches.

For the switching network, a path for the inductor currents must always be provided, while the terminal voltage sources should never be shorted. If the switching function of a switch SW_{jk} in Fig. 2-3 is defined as:

$$s_{jk} = \begin{cases} 1, SW_{jk} closed \\ 0, SW_{jk} open \end{cases}; j = \{a,b,c\}, k = \{p,n\} \tag{2-1}$$

And,

$$s_{jp} + s_{jn} = 1, j = \{a,b,c\} \tag{2-2}$$

The switching network can be simplified as switching network with three single-pole double-throw switches shown in Fig. 2-4. From Fig. 2-4, the three-phase output voltages are given by:

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} s_a \\ s_b \\ s_c \end{bmatrix} \cdot v_{dc} \tag{2-3}$$

The dc side current is:

$$i_{dc} = \begin{bmatrix} s_a & s_b & s_c \end{bmatrix} \cdot \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{2-4}$$

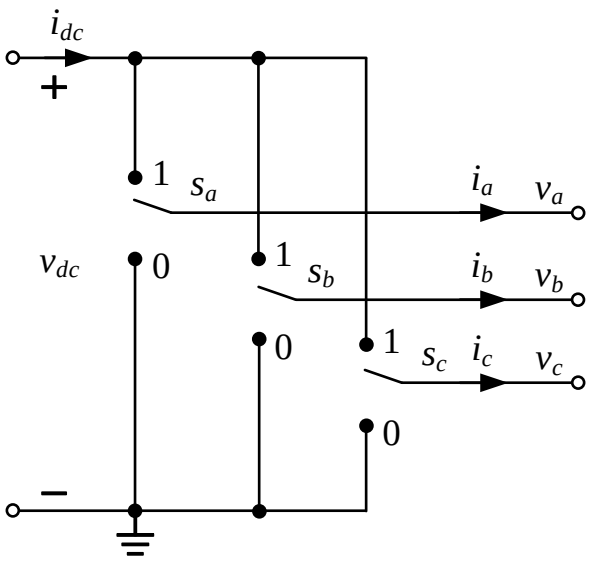


Fig. 2-4. Switching network with single-pole double-throw switches.

At frequencies significantly lower than the switching freuqeny, the operation of the network can be modeled by an average model. The average value of the switching function s_{jk} is the duty cycle of the switch SW_{jk} and is denoted by d_{jk}. Then the average equivalents of Eq. (2-3) and (2-4) are:

$$\vec{\bar{v}}_{ph} = \vec{d}_{ph} \cdot \bar{v}_{dc} \tag{2-5}$$

$$\bar{i}_{dc} = \vec{d}'_{ph} \cdot \vec{\bar{i}}_{ph} \tag{2-6}$$

Eq. (2-5) and (2-6) can be represented by the equivalent circuit shown in Fig. 2-5.

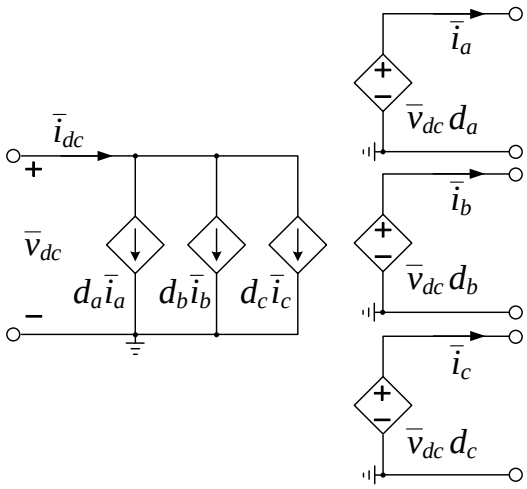


Fig. 2-5. Average model of the switching network.

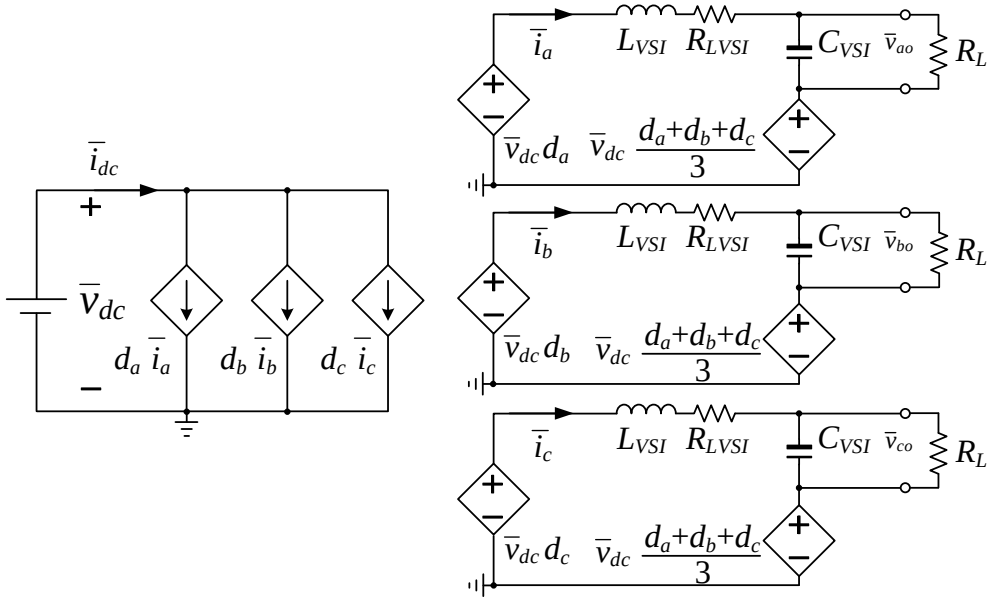


Fig. 2-6. Average model of the power stage of VSI.

To get the average model of VSCs' power stage, just connect the average model of switching network with the filters as shown in Fig. 2-6 for the case of VSI. In Fig. 2-6, the neutral point voltage is modeled as:

$$\bar{v}_n = \frac{\bar{v}_a + \bar{v}_b + \bar{v}_c}{3} = \frac{1}{3}\left(d_a + d_b + d_c\right)\cdot \bar{v}_{dc} \tag{2-7}$$

The state-space equations of Fig. 2-6 are:

$$L_{VSI}\frac{d\vec{\bar{i}}_{ph}}{dt}+R_{LVSI}\vec{\bar{i}}_{ph}=\bar{v}_{dc}\vec{d}_{ph}-\frac{\bar{v}_{dc}}{3}\begin{bmatrix}1&1&1\\1&1&1\\1&1&1\end{bmatrix}\vec{d}_{ph}-\vec{\bar{v}}_{pho} \tag{2-8}$$

$$C_{VSI}\frac{d\vec{\bar{v}}_{pho}}{dt}=\vec{\bar{i}}_{ph}-\frac{1}{R_L}\vec{\bar{v}}_{pho} \tag{2-9}$$

$$\bar{i}_{dc}=\vec{d}_{ph}\cdot\vec{\bar{i}}_{ph} \tag{2-10}$$

For a three-phase ac system, no dc equilibrium point exits in the stationary frame. By doing a transformation from the stationary frame (Eq. (2-31)) to the synchronous reference (*d*-*q*) frame, a three-phase ac system becomes two coupled dc systems [41] as shown in Fig. 2-7.

$$\mathbf{T}_{dq/abc}=\frac{2}{3}\begin{bmatrix}\cos(\theta)&\cos\left(\theta-\frac{2}{3}\pi\right)&\cos\left(\theta+\frac{2}{3}\pi\right)\\-\sin(\theta)&-\sin\left(\theta-\frac{2}{3}\pi\right)&\sin\left(\theta+\frac{2}{3}\pi\right)\end{bmatrix} \tag{2-11}$$

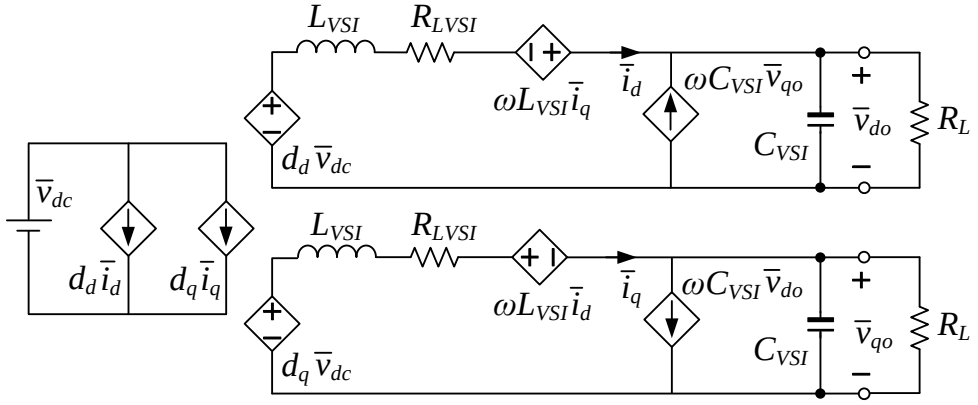


Fig. 2-7. Average equivalent circuit model of VSI.

$$L_{VSI}\frac{d\vec{\bar{i}}}{dt}+R_{LVSI}\vec{\bar{i}}=\bar{v}_{dc}\vec{d}-L_{VSI}\begin{bmatrix}0&-\omega\\\omega&0\end{bmatrix}\vec{\bar{i}}-\vec{\bar{v}}_o \tag{2-12}$$

$$C_{VSI}\frac{d\vec{\bar{v}}_o}{dt}=\vec{\bar{i}}-\frac{1}{R_L}\vec{\bar{v}}_o-C_{VSI}\begin{bmatrix}0 & -\omega\\ \omega & 0\end{bmatrix}\vec{\bar{v}}_o \tag{2-13}$$

$$\vec{\bar{i}}_{dc}=\vec{d}\cdot\vec{\bar{i}} \tag{2-14}$$

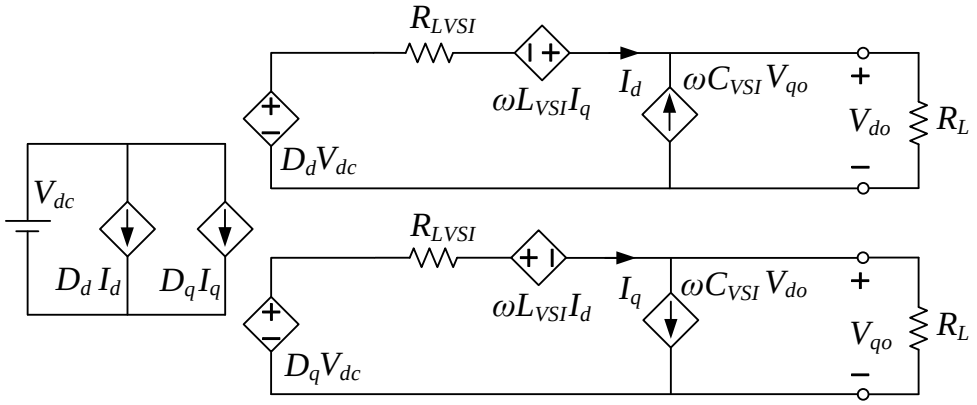


Fig. 2-8. Equivalent circuits of VSI in *d-q* frame for equilibrium point calculation.

Small-signal models of VSCs are obtained by linearization of the large-signal averge models at the equilibrium point. The small-signal of VSI is shown in Fig. 2-9 where the symbol ~ denotes perturbed variables, and the upper-case letters denote the equilibrium point values.

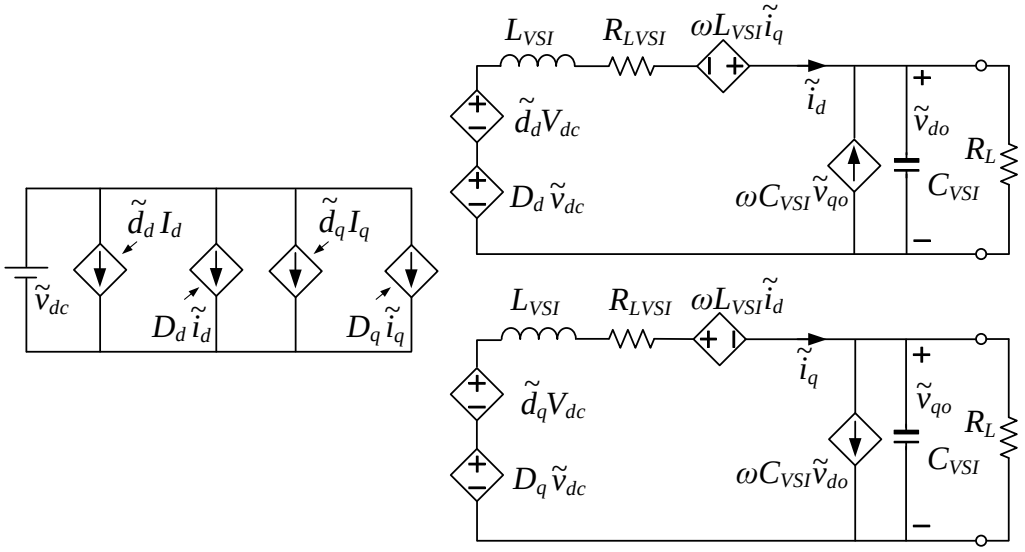


Fig. 2-9. Small-signal equivalent circuits model of VSI in *d-q* frame.

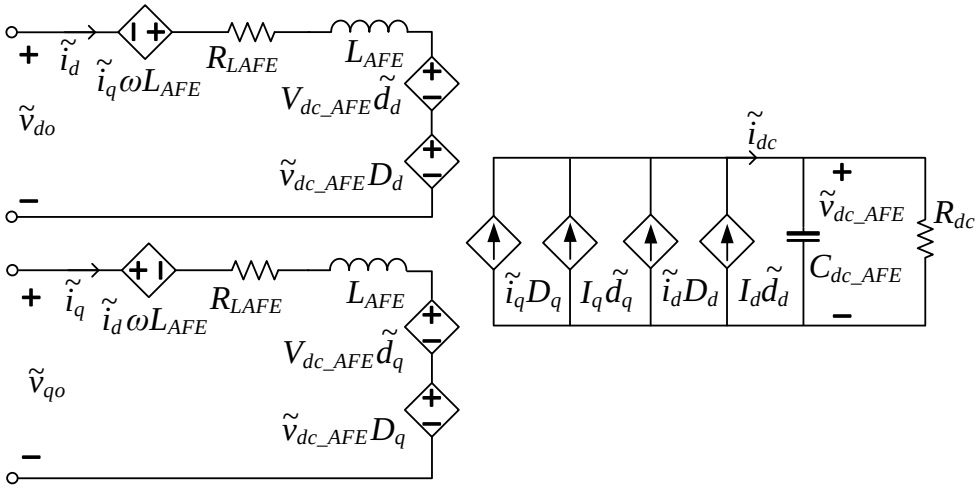


Fig. 2-10. Small-signal equivalent circuits model of AFE in *d*-*q* frame.

2.2 Design of feedback control system for VSCs

Small-signal models of VSCs can be used to design their feedback control systems. Feedback control algorithms for VSCs are usually realized using Digital Signal Processor (DSP). DSP runs the main function just to wait PWM unit to give interrupt signal, which happens every switching period. When the interrupt signal is detected, interrupt function will be triggered. Fig. 2-10 shows the flow chart of interrupt function in which the VSI control algorithm is realized. There are four steps in the interrupt function:

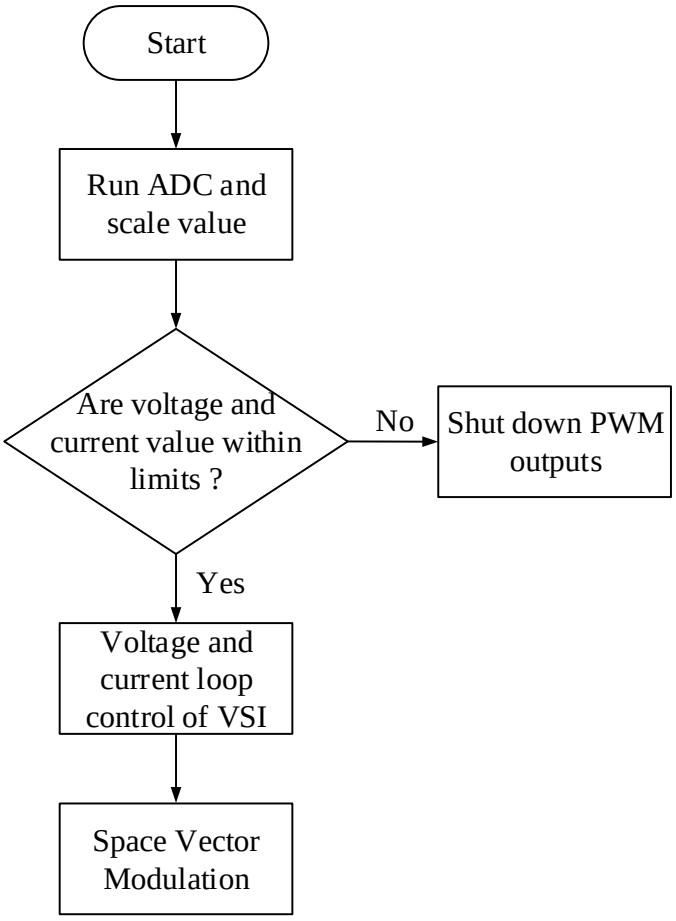


Fig. 2-11. Flow chart of interrupt function for VSI feedback control.

First, run ADC control code to get signals from ADC, scale the signals' values for control.

Second, compare current and voltage values with their limitation for protection purpose, if one signal hits the limits, PWM outputs will be shut down to both converters, if not, go for next step.

Third step is to run VSI voltage and current control.

The final step is to run space vector modulation (SVM) [53]. The calculated duty cycles are being put to the modulator at the next interrupt instant. This digital control algorithm introduces one switching cycle delay. As Fig. 2-12 shows, at the begin instant of k^{th} switching period, power stage voltage and current signals are collected by sensor and ADC, it will take a period of

time for ADC to finish conversion. The digital processor then take some time to run the feedback control and SVM algorithm, the results of the computation will be updated to the modulator's registers at the beginning of $(k+1)^{th}$ switching period. In this process, the computation results of k^{th} switching instant is update at the $(k+1)^{th}$ switching instant, this yields a switching period delay. The triangular-carrier modulation is used as being shows in Fig. 2-13. The modulator will introduce additional half switching cycle (T_{sw}) delay according to [55].

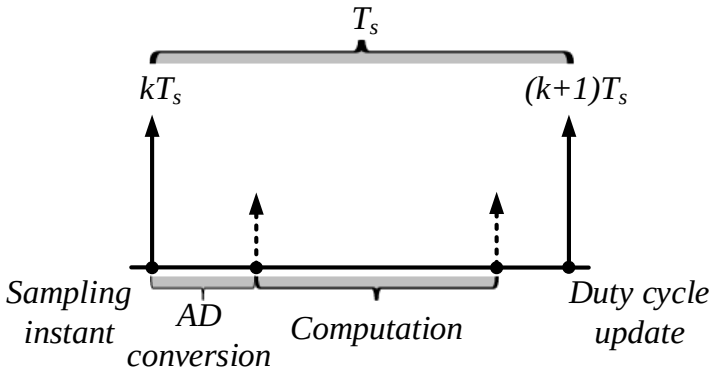


Fig. 2-12. Digital delay caused by digital control algorithm

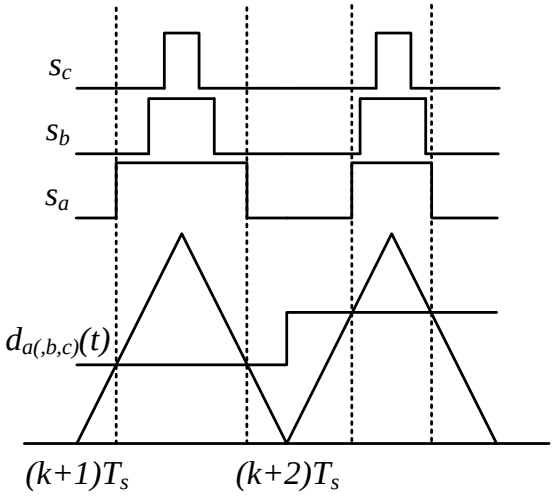


Fig. 2-13. Triangular-carrier modulation

The small-signal of the delay caused by digitial controller and PWM can be model as Eq. (2-15) [56].

$$\mathbf{G_{del}} = \begin{bmatrix} \dfrac{1-0.5T_{del}s}{1+0.5T_{del}s} & 0 \\ 0 & \dfrac{1-0.5T_{del}s}{1+0.5T_{del}s} \end{bmatrix} \tag{2-15}$$

$$T_{del} = 1.5T_{sw} \tag{2-16}$$

In order to do feedback control, filter inductor currents and capacitor voltages are sampled back to DSP. On the path of feedback signals, signal conditioning filters are used for noise rejection. They are been built using operational amplifiers. The circuit diagram is shown in Fig. 2-14. The designed filter model in *d-q* frame is shown in Eq. (2-17).

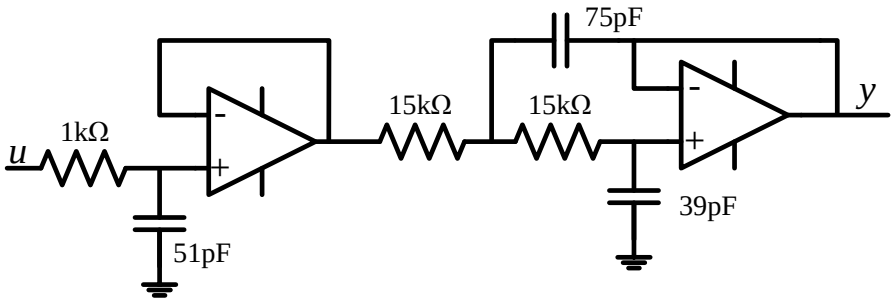


Fig. 2-14. Circuit diagram of on board signal conditioning filter.

$$\mathbf{K} = \begin{bmatrix} \dfrac{\omega_n^2}{s^2+2\zeta\omega_n s+\omega_n^2} & 0 \\ 0 & \dfrac{\omega_n^2}{s^2+2\zeta\omega_n s+\omega_n^2} \end{bmatrix} \tag{2-17}$$

In order to design the feedback controller for inductor current of VSI, the transfer functions from duty cycle to inductor current should be studied. They can be either derived using the small-signal model of VSI power stage considering the digital delay and signal conditioning filer as shown in Fig. 2-15, or measured using VSI hardware and network analyzer as shown in Fig. 2-16.

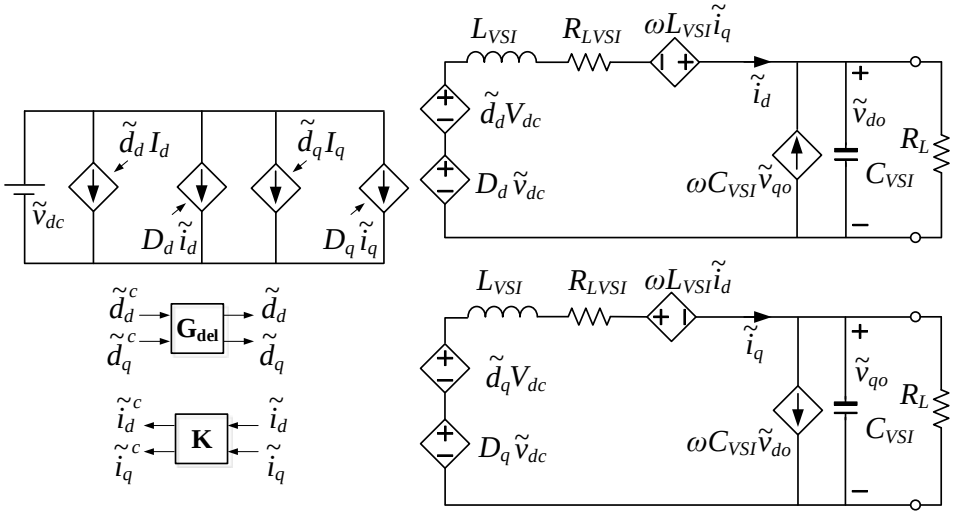


Fig. 2-15. Average model of VSI considering delay and signal conditioning filters.

Fig. 2-16 shows the measurement setups of VSI *d* channel duty cycle (d_d) to d channel current (i_d) transfer function. Network analyzer 4395A is being used for this measurement. First, 4395A generate small signal perturbation, this perturbation is connected to digital controller, which is used to control power stage of VSI, after analog to digital conversion, and the perturbation is added to *d* channel duty cycle reference D_{ref}. Duty ratios in *d-q* frame are then transferred to *α-β* frame for SVM. Small-signal perturbation propagates to gate commands for the power module and further to the voltage generated by the power module at the each phase-leg middle point. When the perturbed voltage applied to the output *LC* filter and resistor load, the current of the inductors are perturbed. These currents are collected back to digital processor and transferred to *d-q* frame. The perturbed *d* channel duty ratio and d channel current are sent back to network analyzer by digital to analog converter. Network analyzer then measures the transfer function from d_d to i_d. To measure the transfer function from d_q to i_q, same procedure can be followed. The only change is to apply the perturbation to D_{qref} and collect perturbed d_q and i_q back to network analyzer.

Table 2-1. VSI power stage parameters

Symbol	Description	Value
V_{dc}	VSI input dc voltage	270 V
V_{VSI_ll}	VSI output line-line rms voltage	99.6 V
f	VSI output voltage frequency	400 Hz
L_{VSI}	Inductance of VSI output inductor	970 μH
R_{LVSI}	Output inductor self-resistor	120 mΩ
C_{VSI}	VSI output capacitor	32 μF
f_{sw}	Switching frequency	20 kHz
R_L	Load resistor	15 Ω
T_{del}	Control and PWM delay	$1.5/f_{sw}$
ω_n	Natural frequency of signal conditioning filter	1.23e6 rad/s
ζ	Damping factor of signal conditioning filter	4.74e-13
D_{dref}	D channel duty cycle reference	0.2996
D_{qref}	Q channel duty cycle reference	0.0662

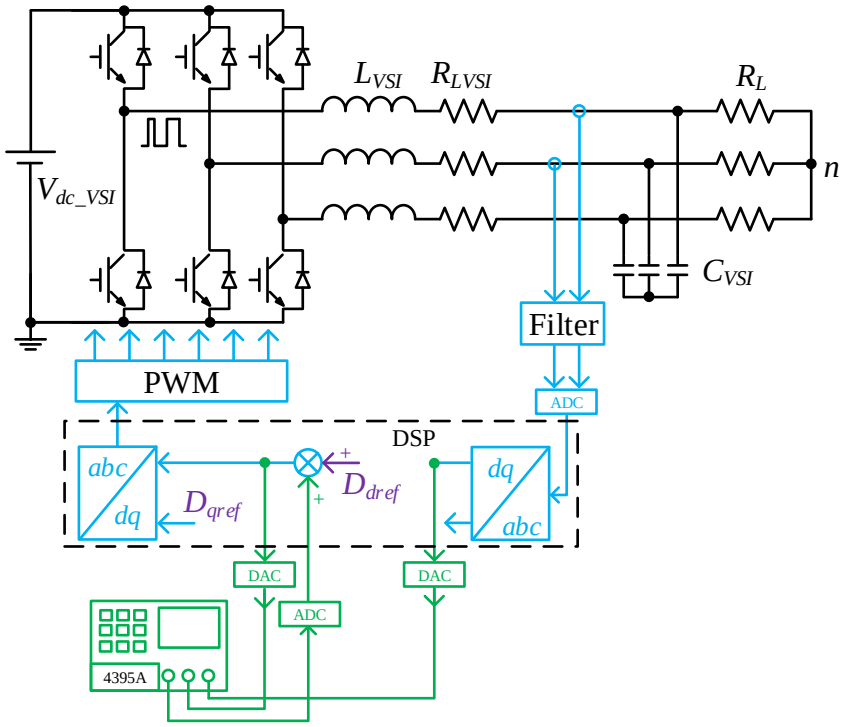


Fig. 2-16. Measurement setup transfer function from d_d to i_d.

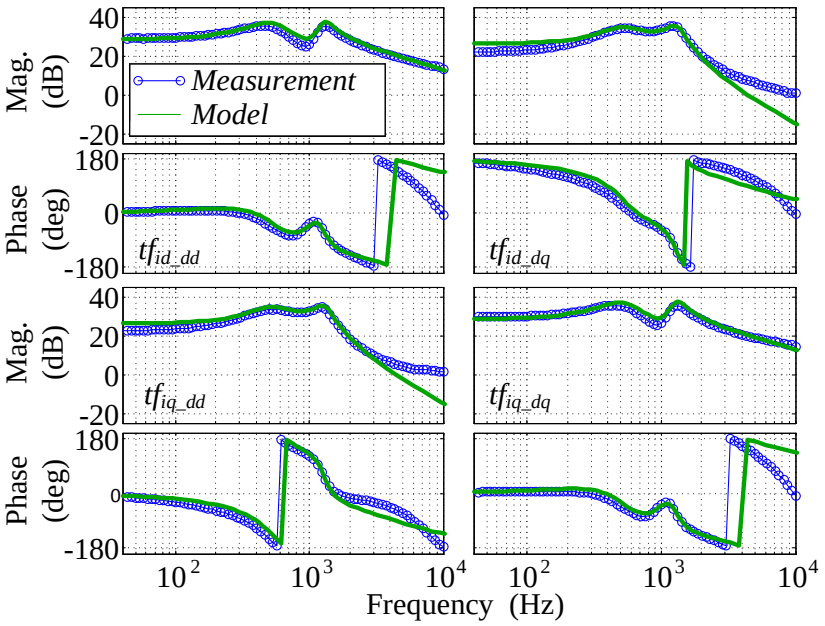


Fig. 2-17. Model and measurement results for open loop transfer functions.

Using the VSI parameters list in Table 2-1, transfer functions from duty cycle to inductor currents are calculated using the model discussed before. Also, they are measured using the method described in Fig. 2-16. Comparison between results from small-signal model and measured are shown in Fig. 2-17. They match with each other with good accuracy.

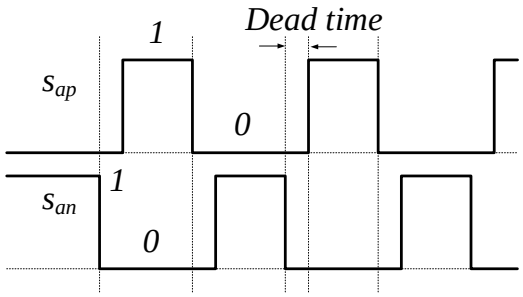


Fig. 2-18. Dead time for the switching network.

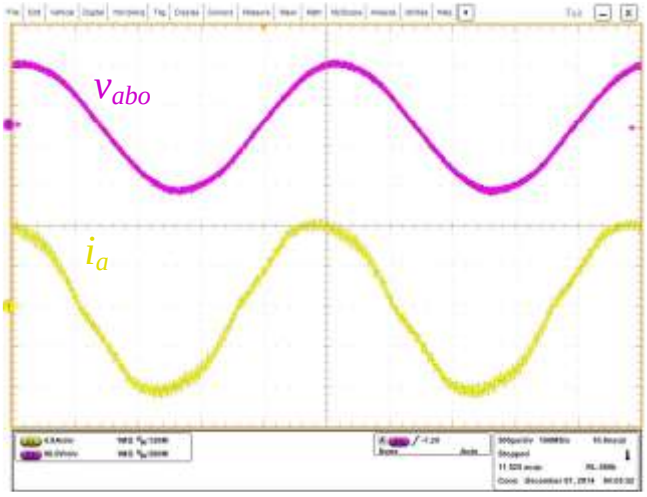


Fig. 2-19. Output voltage and inductor current with 2 μs dead time.

Although for the switching network, the swiching function should fulfill Eq. (2-2). Considering the rising and falling time of the real switches (IGBT and Diode) as well as the delay of the gate signal, dead time, as shown in Fig. 2-8, should be implemented to prevent the shoot through of the top and bottome switches. Dead time will casue the lose of duty cycle and distortion on the inductor current [57], [58] as shown in Fig. 2-19. Dead time also influence the transfer functions from duty cycle to inductor current as shown in Fig. 2-21. Specifically, deat time will introduce damping to these transfer functions. Before doing the feedback control, dead

time should be compensated [57] to improve the quality of inductor current as well as the output voltages. Fig. 2-20 shows the inductor current and output voltage waveforms with dead time compensation. Comparing with Fig. 2-19, both waveforms are improved.

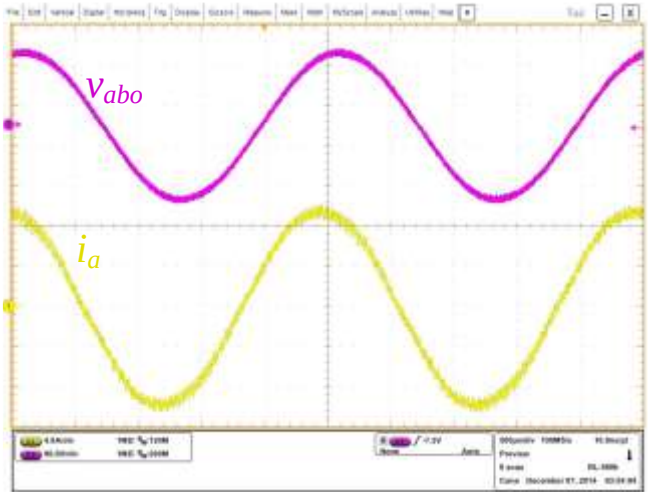


Fig. 2-20. Output voltage and inductor current with 1 μs dead time and compensation.

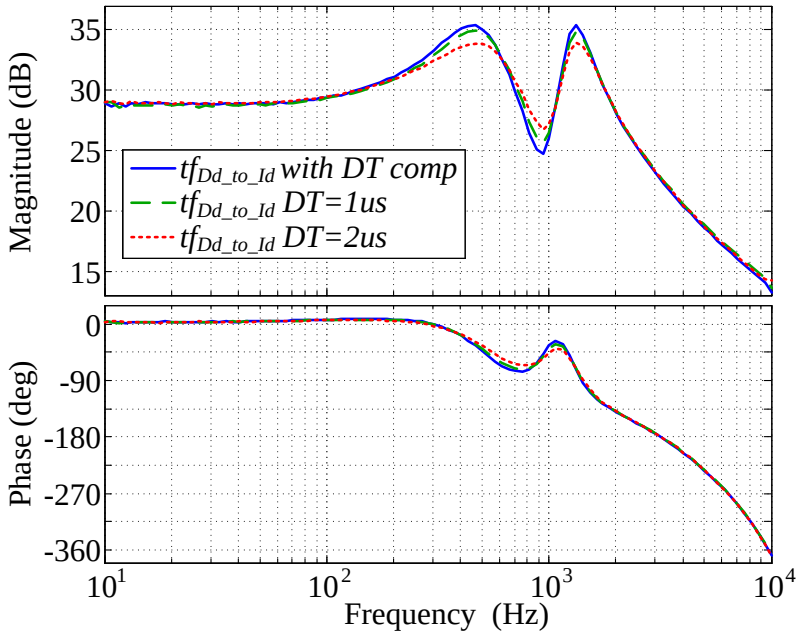


Fig. 2-21. Influence of dead time to open loop transfer function.

Based on the transfer functions been measured, PI controller (k_{pi} = 0.0465; k_{ii} = 121.01) is designed. Fig. 2-22 shows the *d* channel current feedback control loop-gain measurement setup. Current loop-gain is measured by breaking the feedback control loop and injecting perturbation using network analyzer. The breaking point is chosen at the feedback signal i_d, the signals before and after adding perturbation are sent out to network analyzer to measure the loop-gain. Fig. 2-23 shows the small-signal model and measurement results of *d* and *q* channel current loop-gains. The comparison shows the simulation results match the measurement results very well.

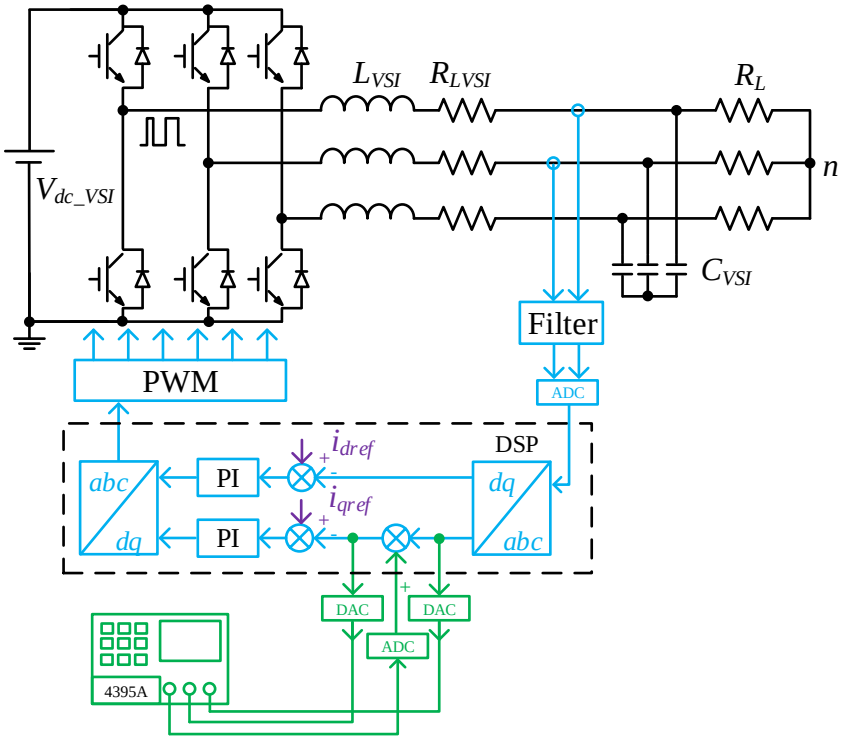


Fig. 2-22. Current loop-gain measurement setup.

Notice that the current loop-gains in Fig. 2-23 have 2k Hz bandwidth (BW) and 21 ° phase margin (PM). This design has small PM which is not enough for typical feedback control loop. The inductor current can be distorted because of the small PM as shown in Fig. 2-24. To reduce the resonance in the inductor current and improve the quality of the waveform, a current regulator with high PM can help.

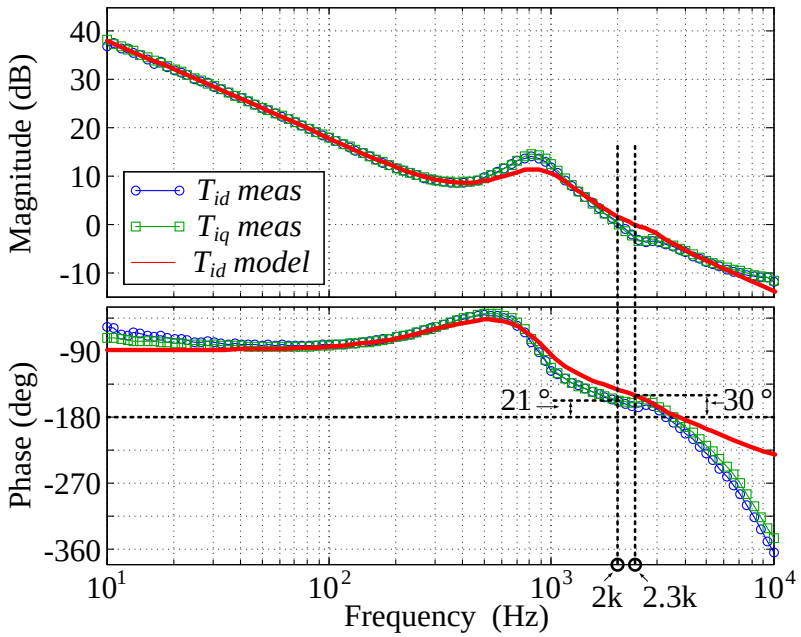


Fig. 2-23. Current loop-gains with high BW low PM.

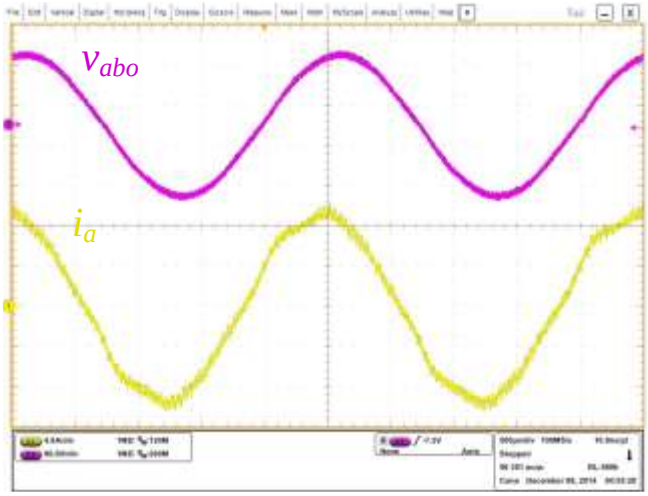


Fig. 2-24. Output voltage and inductor current with high BW low PM current loop.

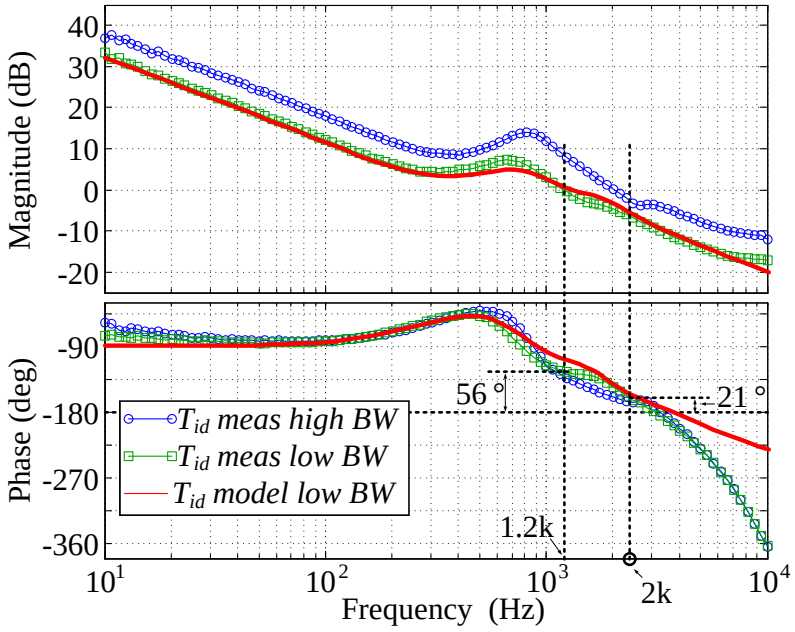


Fig. 2-25. Current loop-gains with low BW high PM.

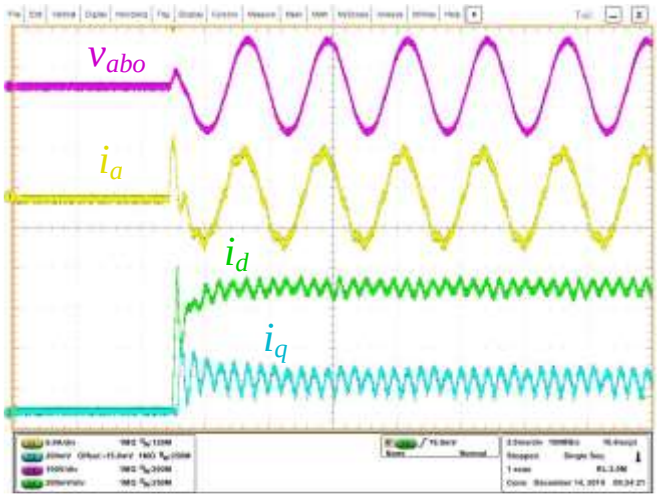


Fig. 2-26. Current reference step responses with high BW low PM.

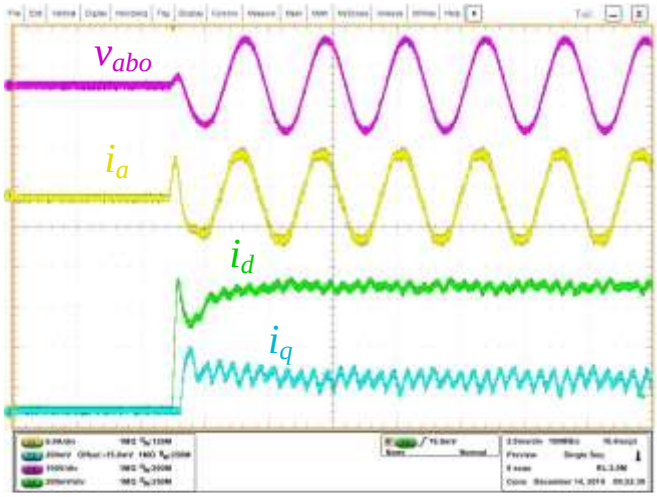


Fig. 2-27. Current reference step responses with low BW high PM.

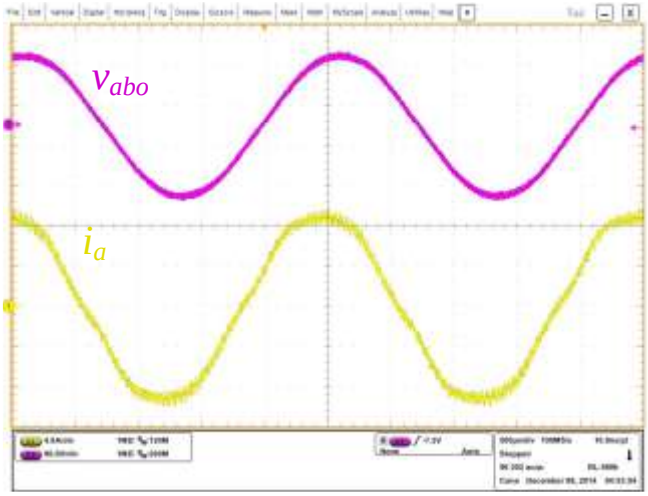


Fig. 2-28. Output voltage and inductor current with low BW high PM current loop.

By reducing the value of current loop PI controller by half, the PM of the loop-gains can be increased as shown in Fig. 2-25. In Fig. 2-25, the BW is still around 1k Hz, the PM is increased to 56°. With this design, the current loop has more robustness and the quality of the current waveform is improved as shown in Fig. 2-27 and Fig. 2-28.

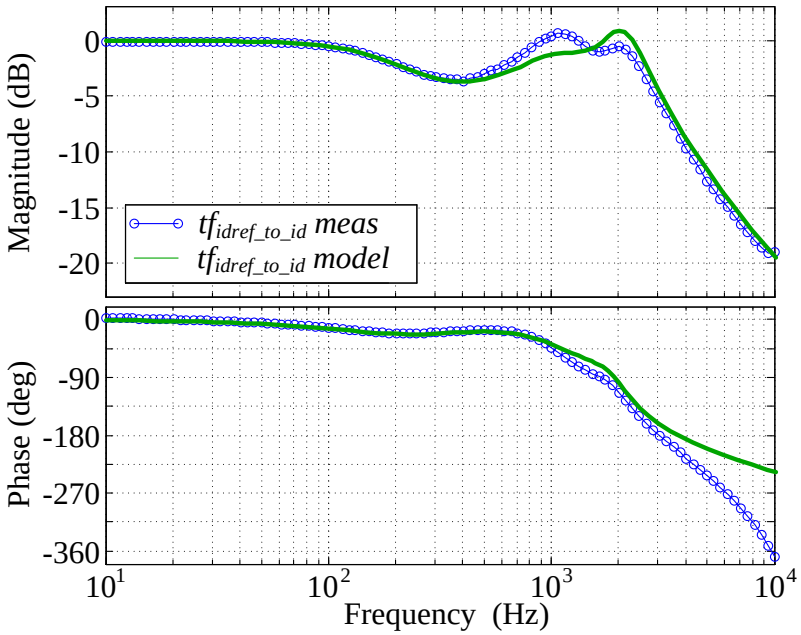


Fig. 2-29. Transfer function from i_{dref} to i_d.

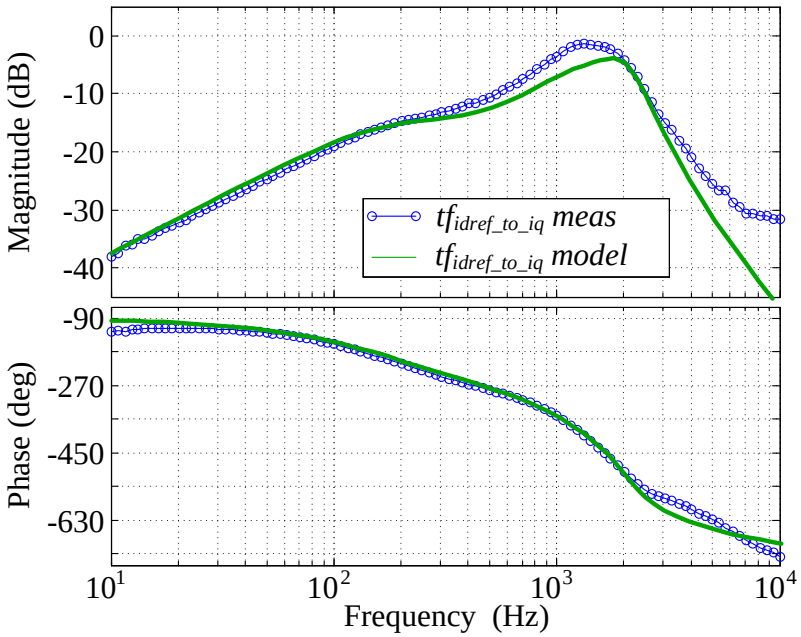


Fig. 2-30. Transfer function from i_{dref} to i_q.

Fig. 2-29 shows the closed-loop transfer function of *d*-channel current loop, it shows the tracking performance of *d*-channel current (i_d) to its reference (i_{dref}). Fig. 2-30 shows the transfer

function from i_{dref} to i_q. As discussed before, in d-channel and q-channel are coupled i_d is the perturbation for i_q. Fig. 2-30 reflects the attenuation of i_{dref} to i_q. As indicated by Fig. 2-30, perturbation from i_{dref} is well attenuated at the low and high frequency range. The gain from i_{dref} to i_q are nearly 1 at the resonant frequency of LC filter.

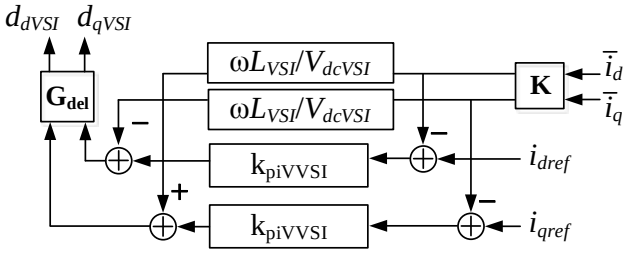


Fig. 2-31. Current controller with decoupling for VSI.

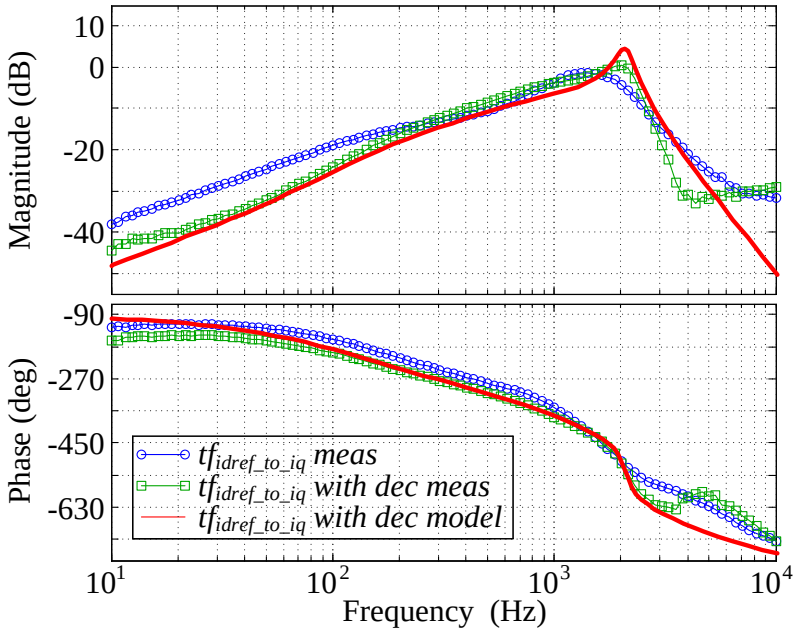


Fig. 2-32. Effects of current loop decoupoing control.

As shown in the small-signal model, the coupling of one channel is coming from other channel current. Decoupling control scheme shown in Fig. 2-31 can be used to further reduce the coupling effect. Fig. 2-32 shows the effects of current loop decoupling control. At low frequency, the coupling effect is further decreased by around 10dB. At the resonant frequency of

the filter, the coupling effect is increased because of the control delay. Advanced decoupling schemes [60], [61] should be applied to handle this issue.

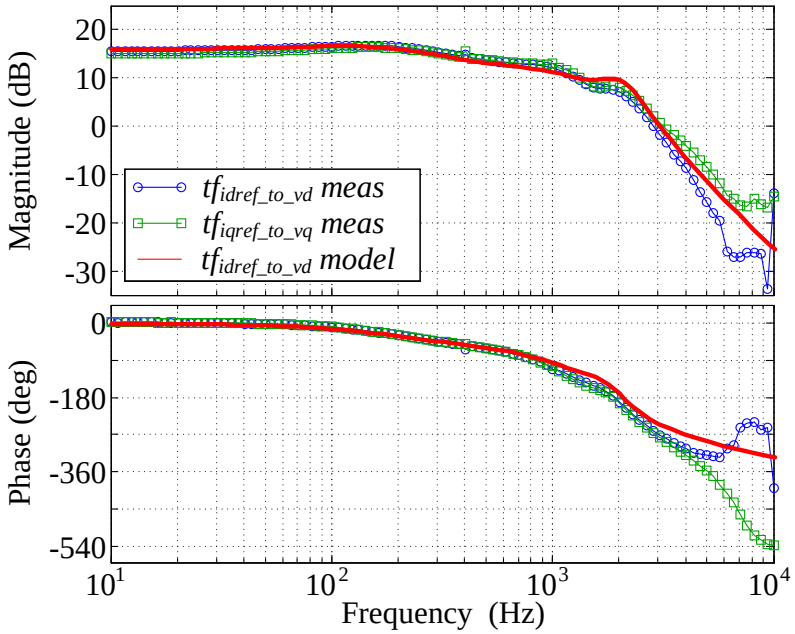


Fig. 2-33. Transfer function from i_{dref} to v_d.

To design the voltage feedback control loop, transfer functions from current references to output voltages are modeled and measured as the transfer functions from duty cycles to inductor currents have been done for current loops. Fig. 2-33 shows the transfer functions from i_{dref} to v_d obtained from small-signal model and measurement. Fig. 2-34 shows the voltage loop-gains, with the PI controller (k_{pv} = 0.0297; k_{iv} = 78.54), which shows the voltage loop has 100Hz BW with 62 °PM. Fig. 2-35 shows the output voltage and inductor current when both current and voltage loops are closed. Fig. 2-37 shows the *d* channel voltage tracking performance. Fig. 2-38 shows the voltage loop decoupling control scheme. Fig. 2-39 shows the transfer functions from v_{dref} to v_q with and without voltage decopling control scheme. Similar issue regarding the decoupling control for output voltage can also be observed.

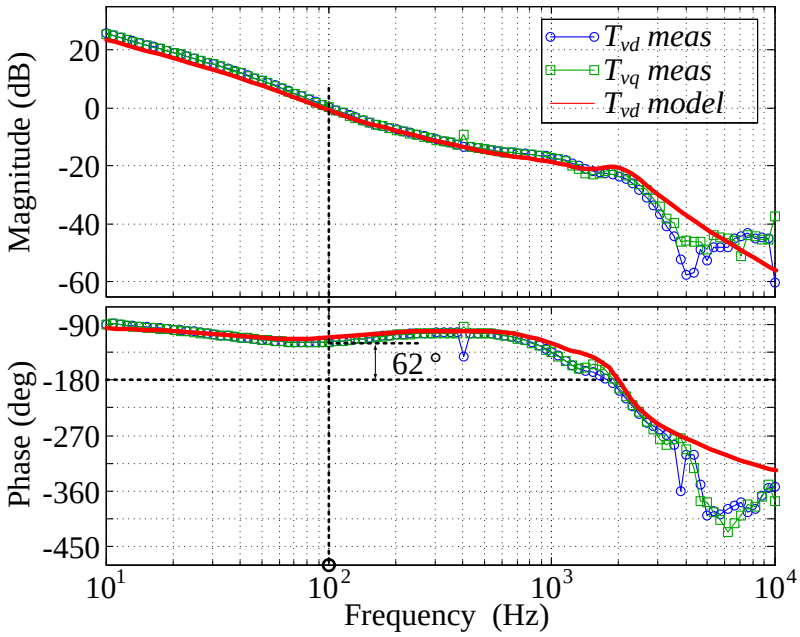


Fig. 2-34. Voltage loop-gain.

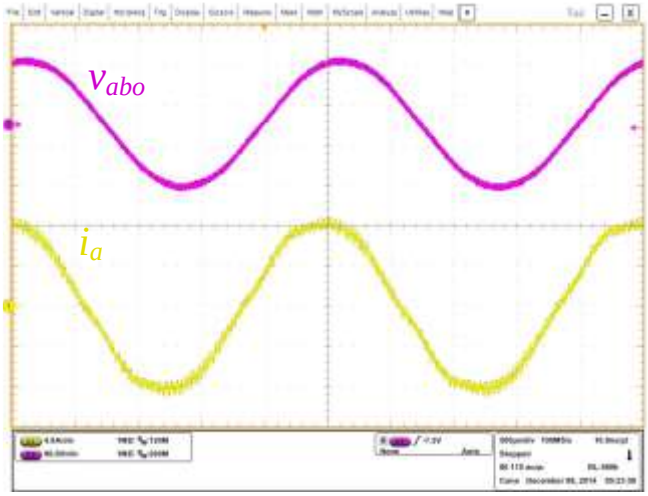


Fig. 2-35. Output voltage and inductor with both current and voltage loops.

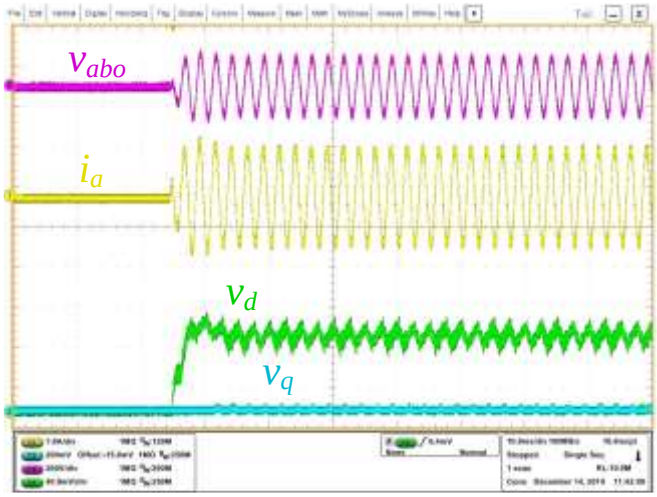


Fig. 2-36. Voltage reference step responses with both current and voltage loops.

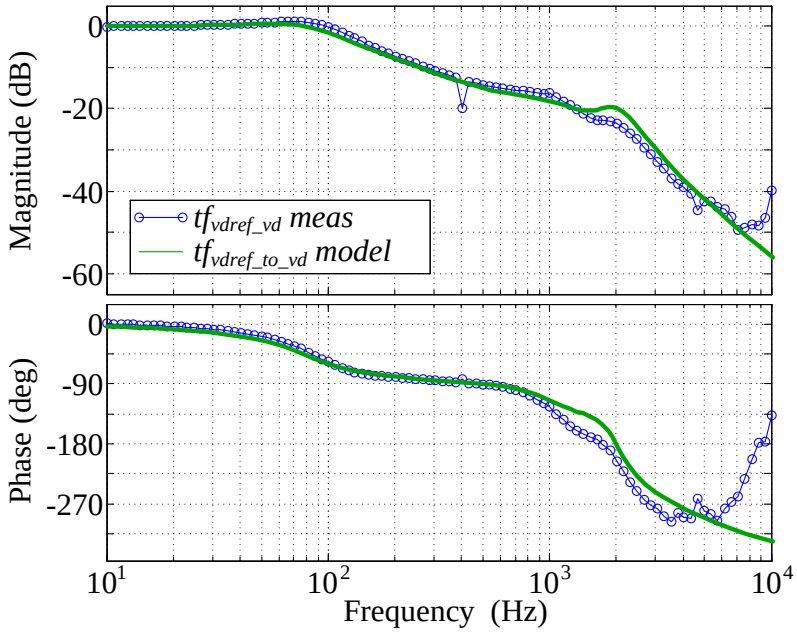


Fig. 2-37. Transfer function from v_{dref} to v_d.

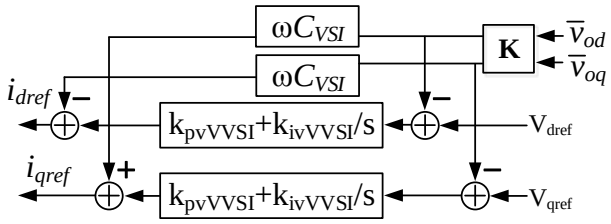


Fig. 2-38. Voltage controller with decoupling for VSI.

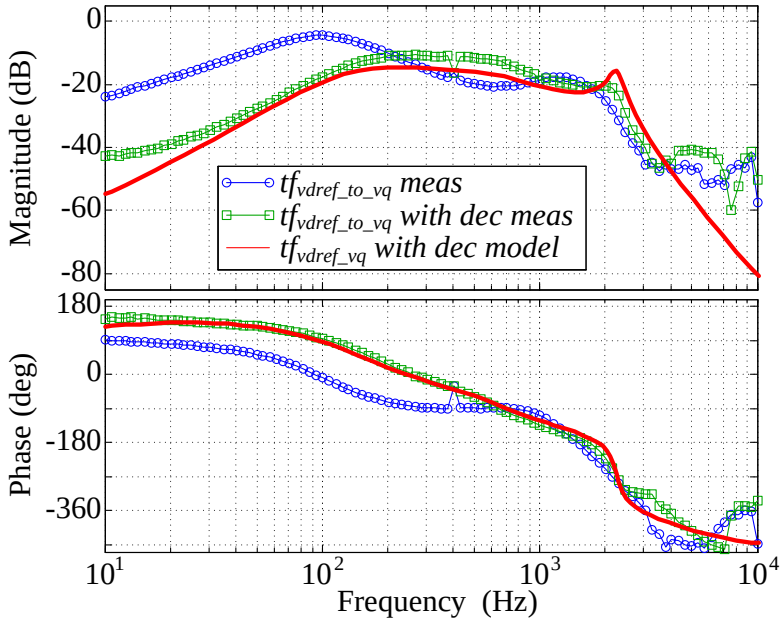


Fig. 2-39. Effects of voltage loop decouping control.

2.3 Input and output impedance of VSCs

GNC is an method to predict stability at ac interface using source and load impedances matrix ratio in the *d-q* frame. Understanding the input and output impedances of AFE and VSI are critical for stability analysis of the ac system consist of VSCs.

Small-signal impedance is derived by linearizing the average model around a dc operation point. By doing *d-q* transformation, three-phase inverter circuit becomes dc circuit with two coupled channels as been discussed in last section. The impedance in *d-q* frame is a 2×2 matrix, perturbation on output current of one channel produces response from itself and the cross-

coupling channel [41]. Using the small-signal discussed in las section, this section will discuss the modeling process of output impedance of VSI. The average model of VSI with feedback control is shown in Fig. 2-40. The modeling process follows the steps of modeling the output impedance of inverter power stage in *d-q* frame, the influence of current feedback control, and the influence of voltage feedback control.

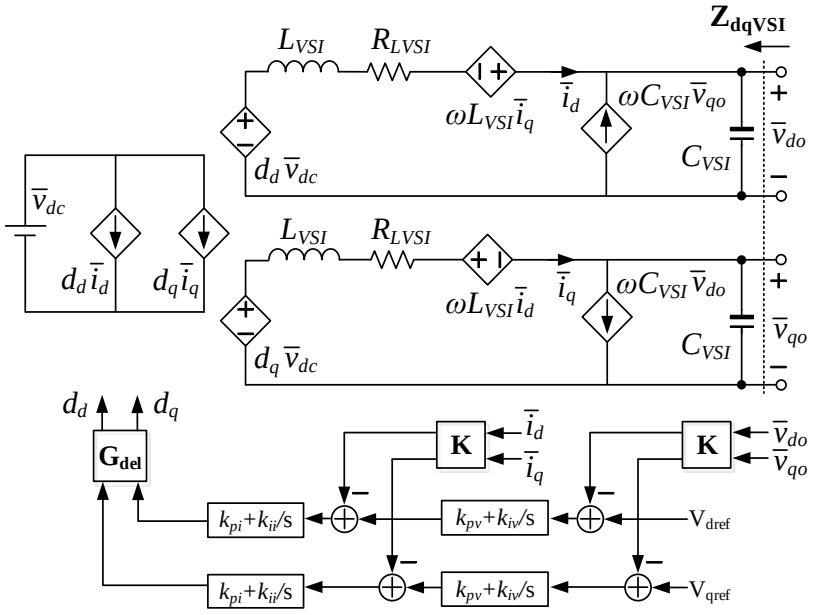


Fig. 2-40. Average model of VSI in *d-q* frame with feedback control.

2.3.1 Open loop output impedances of VSI

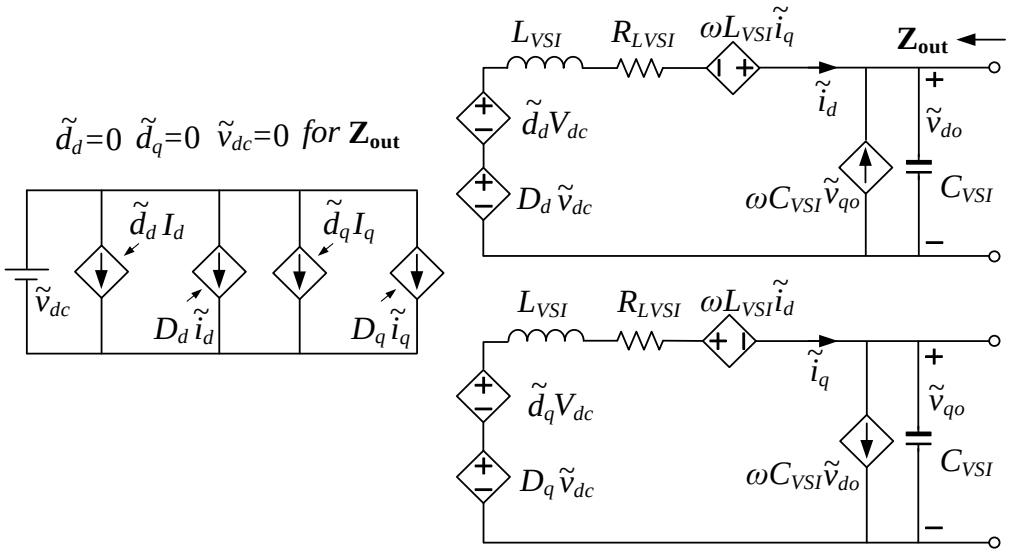


Fig. 2-41. Small-signal circuit model of VSI power stage.

Fig. 2-41 shows the small-signal model of the VSI power stage. Assume the input of the inverter is supplied by a stiff dc source which could be a battery or dc-dc converter. Then, the dynamic from dc input can be neglected. The small-signal circuit model then can be represented by the transfer function matrix flow chart shown in Fig. 2-42. $\mathbf{G_{vd}}$ is the transfer function matrix from duty ratio vector $\vec{\tilde{d}}$ to output voltage vector $\vec{\tilde{v}}_o$; $\mathbf{Z_{out}}$ is the open loop output impedance; $\mathbf{G_{id}}$ is the transfer function matrix from duty ratio vector $\vec{\tilde{d}}$ to inductor current vector $\vec{\tilde{i}}$; $\mathbf{G_{ii}}$ is the transfer function matrix from output current vector $\vec{\tilde{i}}_o$ to inductor current vector $\vec{\tilde{i}}$.

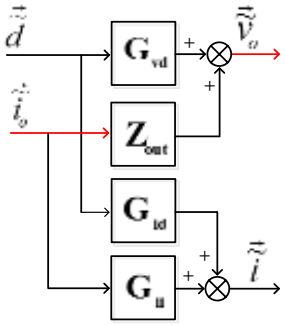


Fig. 2-42. VSI power stage small-signal model.

The output impedance can be derived by forcing perturbations of the duty ratio and dc voltage to zero as shown in Fig. 2-41. The expression of open loop output impedance is:

$$\mathbf{Z_{out}} = \begin{bmatrix} Z_{dd} & Z_{dq} \\ Z_{qd} & Z_{qq} \end{bmatrix} = -\frac{1}{3}\begin{bmatrix} \frac{num_{11}}{den} & \frac{num_{12}}{den} \\ \frac{num_{21}}{den} & \frac{num_{22}}{den} \end{bmatrix} \tag{2-18}$$

Where,

$$den = (-3^2\omega^2 {L_{VSI}}^2 C_{VSI} s - G_L^2 C_{VSI} s - G_L)^2 + (3^2\omega^3 {L_{VSI}}^2 C_{VSI} - 3\omega L_{VSI} + G_L^2 \omega C_{VSI})^2 \tag{2-19}$$

$$num_{11} = -(3^2\omega^2 {L_{VSI}}^2 + G_L^2)\cdot (3^2\omega^2 {L_{VSI}}^2 C_{VSI} s + G_L^2 C_{VSI} s + G_L) \tag{2-20}$$

$$num_{12} = -(3^2\omega^2 {L_{VSI}}^2 + G_L^2)\cdot (3^2\omega^3 {L_{VSI}}^2 C_{VSI} - 3\omega L_{VSI} + G_L^2 \omega C_{VSI}) \tag{2-21}$$

$$num_{21} = -num_{12}\,, num_{22} = num_{11} \tag{2-22}$$

$$G_L = 3L_{VSI} s + 3R_{LVSI} \tag{2-23}$$

Other transfer function matrix can be derived using the same methodology.

Table 2-1 shows the parameters of a 400 Hz VSI prototype system. Using these parameters and the model shown above, the inverter open loop output impedance is plotted. Fig. 2-43 shows the open-loop *d-q* frame output impedance of the VSI superimposed over the impedance of the output *LC* filter in the *abc*-frame. As observed, due to the modulation effect of the *d-q* frame transformation, the VSI impedance in the *d-q* frame has two resonant frequencies, which correspond to the transformed *abc*-frame impedance of the *LC* filter. These two resonant frequencies are consequently separated by two-times the line frequency around the *LC* filter resonant frequency. Fig. 2-43 depicts this phenomenon where the *LC* resonant frequency at 900 Hz is clearly seen, as well as the two corresponding resonant peaks at 500 Hz and 1.3 kHz respectively for the VSI impedance in the *d-q* frame given the 400 Hz line frequency employed.

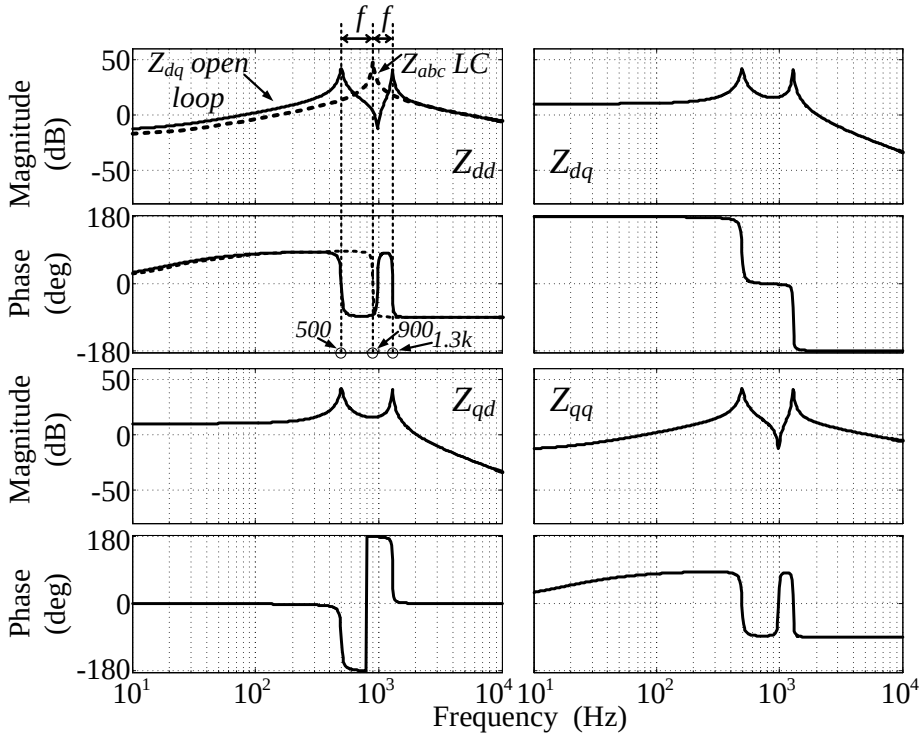


Fig. 2-43. Open loop output impedance of VSI.

2.3.2 VSI Impedance with current feedback control

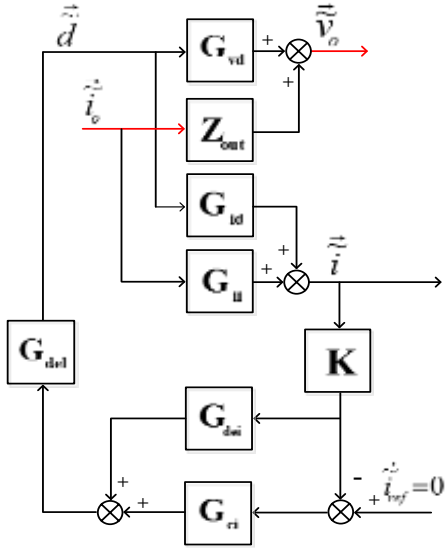


Fig. 2-44. VSI small-signal model with current feedback control.

Current controller can be implemented in either synchronous frame or stationary frame. Stationary frame current regulators can be transformed to synchronous frame using the transformation provided by [91]. Modeling of the impedance of voltage source converter with stationary frame current regulator is shown in [92]. Influence of different current regulators will not be elaborated, only current controller in synchronous frame is considered in this study. Fig. 2-44 shows the small-signal model of inverter with current feedback control. **K** is the filter transfer The current controller matrix is $\mathbf{G_{ci}}$ (k_{pi} = 0.0465; k_{ii} = 121.01). $\mathbf{G_{dei}}$ is the decoupling term:

$$\mathbf{G_{ci}} = \begin{bmatrix} k_{pi} + \dfrac{k_{ii}}{s} & 0 \\ 0 & k_{pi} + \dfrac{k_{ii}}{s} \end{bmatrix} \tag{2-24}$$

$$\mathbf{G_{dei}} = \begin{bmatrix} 0 & -\dfrac{3\omega L_{ac}}{V_{dc}} \\ \dfrac{3\omega L_{ac}}{V_{dc}} & 0 \end{bmatrix} \tag{2-25}$$

By forcing the current reference signal $\vec{\tilde{i}}_{L\_ref}$ to zero, one can derive the VSI output impedance with current feedback control by solving the equations shown in Eq. (2-26). The analytical expression of inverter output impedance with inductor current feedback control is given by Eq. (2-27).

$$\begin{cases} \vec{\tilde{d}} = \mathbf{G_{del}}\left(\mathbf{G_{dei}} - \mathbf{G_{ci}}\right)\mathbf{K}\vec{\tilde{i}}_L \\ \vec{\tilde{i}}_L = \mathbf{G_{id}}\vec{\tilde{d}} + \mathbf{G_{ii}}\vec{\tilde{i}}_o \\ \vec{\tilde{v}}_o = \mathbf{G_{vd}}\vec{\tilde{d}} + \mathbf{Z_{out}}\vec{\tilde{i}}_o \end{cases} \tag{2-26}$$

$$\mathbf{Z_{il}} = \mathbf{G_{vd}}\left(\left(\mathbf{I} + \mathbf{G_{del}}\left(\mathbf{G_{ci}} - \mathbf{G_{dei}}\right)\mathbf{K}\mathbf{G_{id}}\right)^{-1} \cdot \mathbf{G_{del}}\left(-\mathbf{G_{ci}} + \mathbf{G_{dei}}\right)\mathbf{K}\mathbf{G_{ii}}\right) + \mathbf{Z_{out}} \tag{2-27}$$

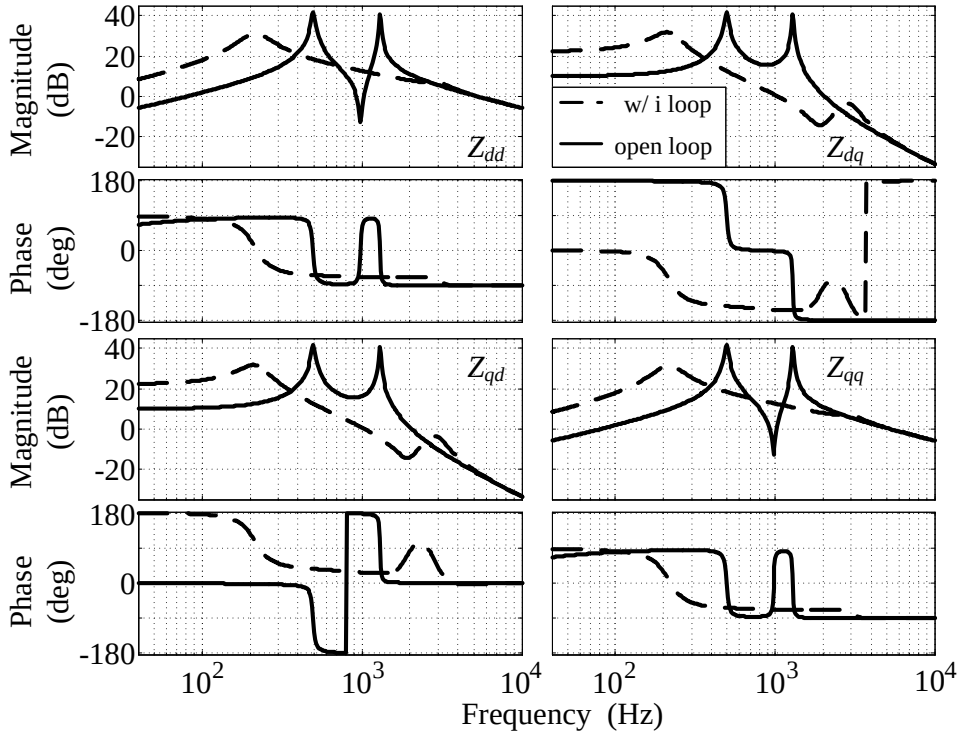


Fig. 2-45. Inverter output impedance with and without feedback control.

The most prominent feature in this case is that these *LC* resonances are effectively smoothed out by the converter current loop. This shows the inductor current feedback control works as a damper of the L-C resonances.

2.3.3 VSI Impedance with current and voltage feedback control

Fig. 2-46 shows the small-signal model of inverter with both current and voltage feedback control loops, in which $\mathbf{G_{cv}}$ is the voltage controller:

$$\mathbf{G_{cv}} = \begin{bmatrix} k_{pv} + \dfrac{k_{iv}}{s} & 0 \\ 0 & k_{pv} + \dfrac{k_{iv}}{s} \end{bmatrix} \tag{2-28}$$

By forcing the voltage reference signal $\tilde{\vec{v}}_{o\_ref}$ to zero, one can derive the VSI output impedance with both current and voltage feedback control by solving the equations shown in (2-29. The analytical expression of VSI output impedance with both current and voltage loop control is given by Eq. (2-30).

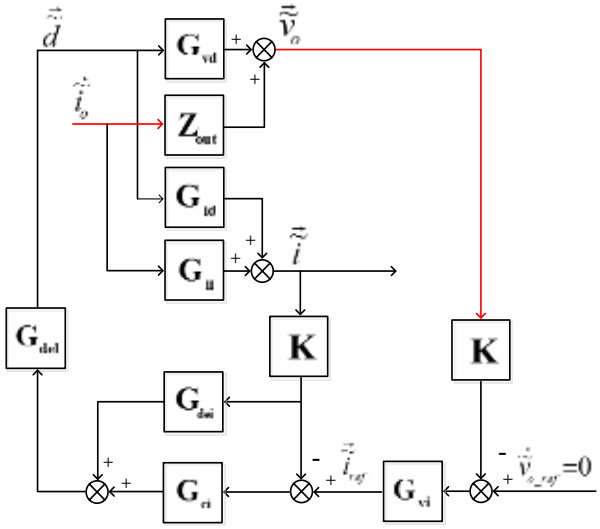


Fig. 2-46. VSI small-signal model with both current and voltage feedback control loops.

$$\begin{cases} \tilde{\vec{d}} = \mathbf{G_{del}}\left(\mathbf{G_{dei}}\mathbf{K_i}\tilde{\vec{i}}_L + \mathbf{G_{ci}}\left(\tilde{\vec{i}}_{L\_ref} - \mathbf{K_i}\tilde{\vec{i}}_L\right)\right) \\ \tilde{\vec{i}}_L = \mathbf{G_{id}}\tilde{\vec{d}} + \mathbf{G_{ii}}\tilde{\vec{i}}_o \\ \tilde{\vec{i}}_{L\_ref} = -\mathbf{G_{cv}}\mathbf{K_v}\tilde{\vec{v}}_o \\ \tilde{\vec{v}}_o = \mathbf{G_{vd}}\tilde{\vec{d}} + \mathbf{Z_o}\tilde{\vec{i}}_o \end{cases} \tag{2-29}$$

$$\mathbf{Z_{vil}} = \left(\mathbf{I} + \mathbf{G_{vd}} \left(\begin{matrix} \left(\mathbf{I} + \mathbf{G_{del}}\left(\mathbf{G_{ci}} - \mathbf{G_{dei}}\right)\mathbf{K_i}\mathbf{G_{id}}\right)^{-1} \\ \cdot \mathbf{G_{del}}\mathbf{G_{ci}}\mathbf{G_{cv}}\mathbf{K_v} \end{matrix} \right) \right)^{-1} \cdot \left(\begin{matrix} \mathbf{G_{vd}}\left(\mathbf{I} + \mathbf{G_{del}}\left(\mathbf{G_{ci}} - \mathbf{G_{dei}}\right)\mathbf{K_i}\mathbf{G_{id}}\right)^{-1} \cdot \\ \mathbf{G_{del}}\left(-\mathbf{G_{ci}} + \mathbf{G_{dei}}\right)\mathbf{K_i}\mathbf{G_{ii}} + \mathbf{Z_o} \end{matrix} \right) \qquad (2\text{-}30)$$

Fig. 2-47 shows comparison between inverter impedance with only current control loop (dashed lines) and with both current and voltage control loops (solid lines). Voltage controller reduces the impedance within its bandwidth, especially Z_{dq} and Z_{qd} are greatly reduced. This shows the voltage control loop reduces the cross coupling between *d*-channel and *q*-channel a lot. Bandwidth of the voltage controller influence the inverter output impedances. Fig. 2-48 shows three different voltage controller designs. The corresponding inverter output impedance is shown in Fig. 2-49 which shows the higher the voltage loop bandwidth is, the lower the output impedance is.

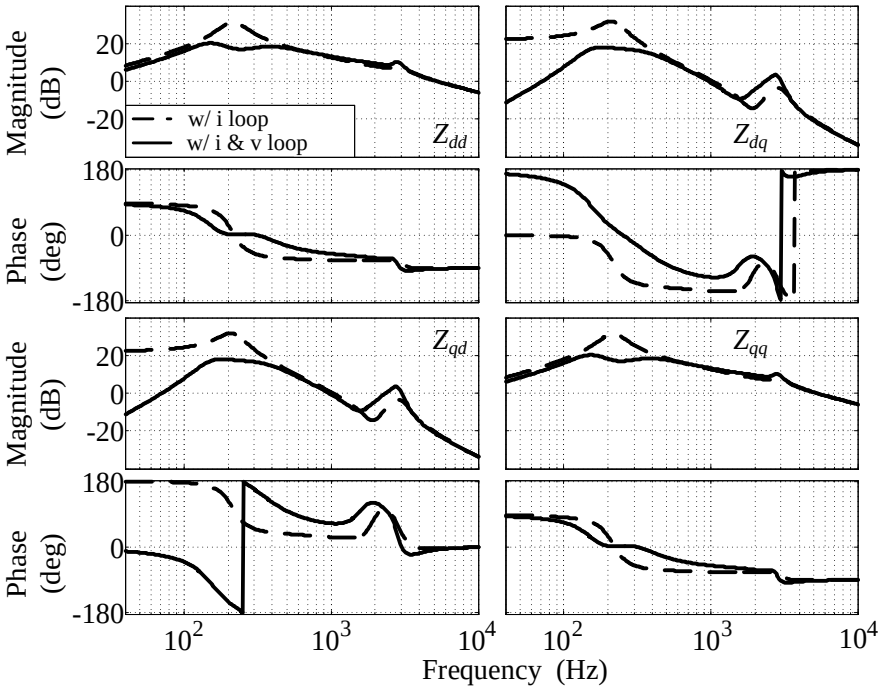


Fig. 2-47. VSI output impedance with single and multiple feedback control loops.

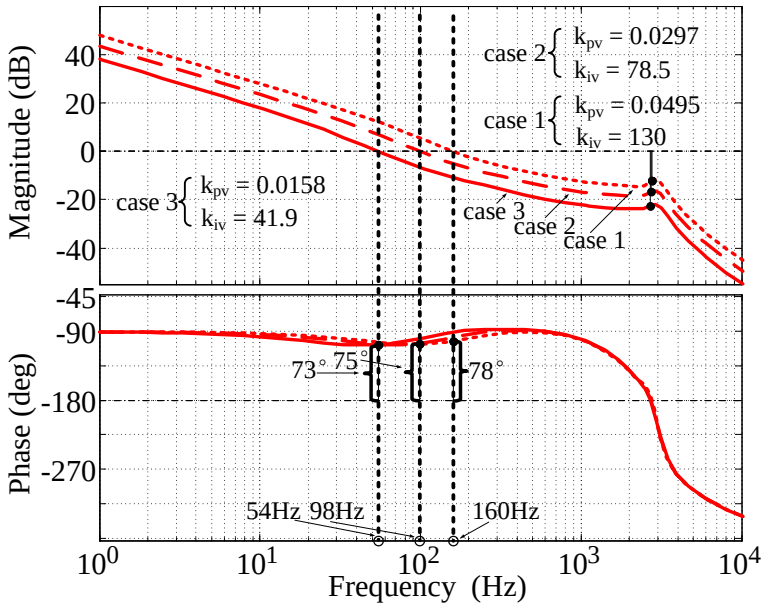


Fig. 2-48. Different voltage control loop designs.

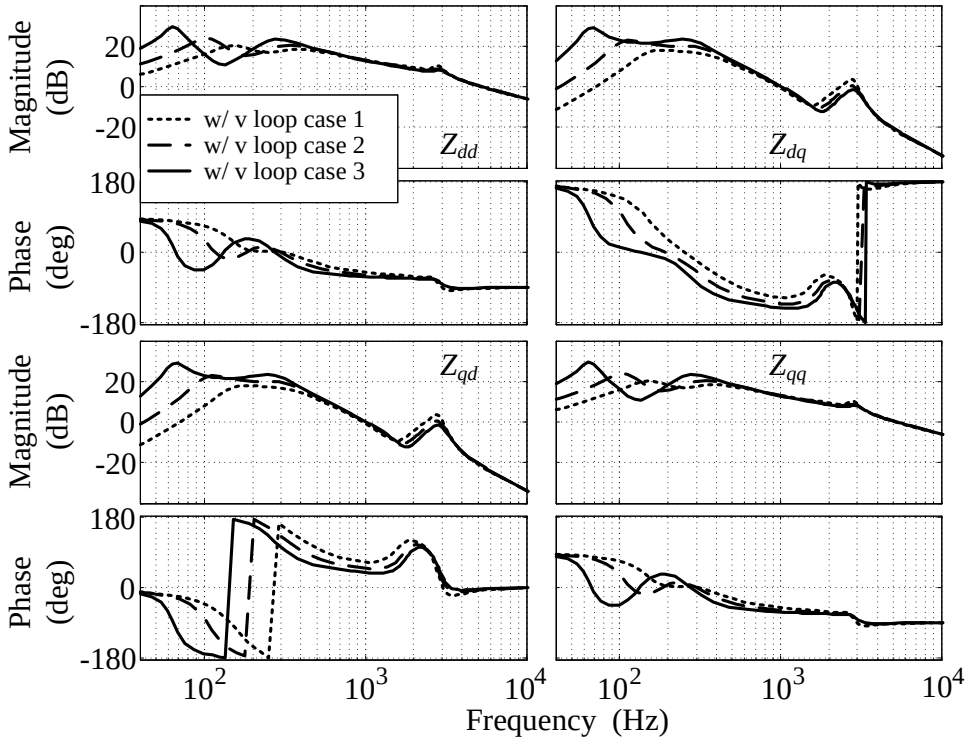


Fig. 2-49. VSI output impedances with different voltage controllers.

2.3.4 AFE input impedances

Same *d-q* impedances modeling approach discussed for VSI can be used for three-phase AFE. Fig. 2-50 shows the average model with feedback control. In this model, $\mathbf{T}_{\Delta\theta}$ is the *d-q* transformation.

$$\mathbf{T}_{\Delta\theta} = \begin{bmatrix} \cos(\Delta\theta) & \sin(\Delta\theta) \\ -\sin(\Delta\theta) & \cos(\Delta\theta) \end{bmatrix} \tag{2-31}$$

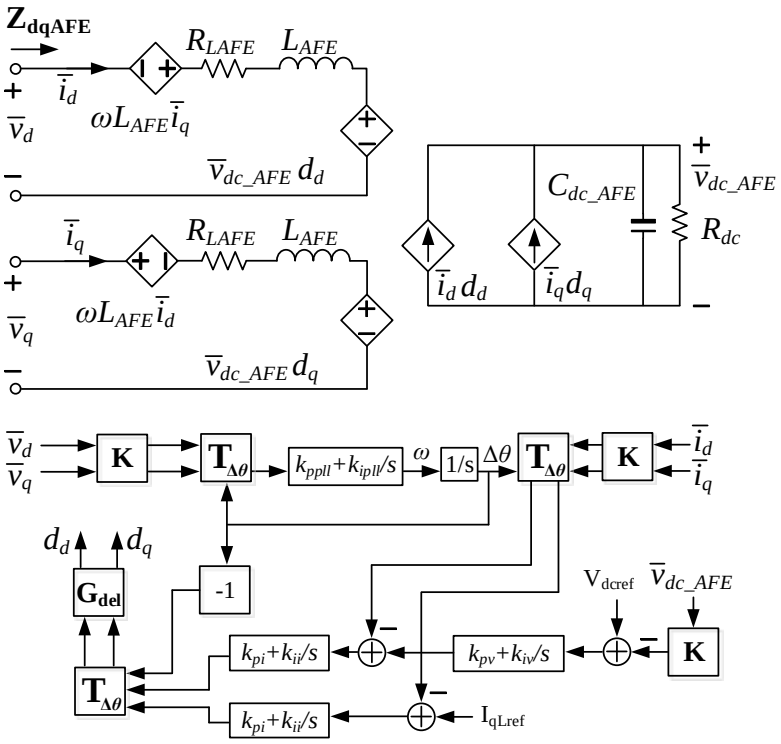


Fig. 2-50. Small-signal model of AFE.

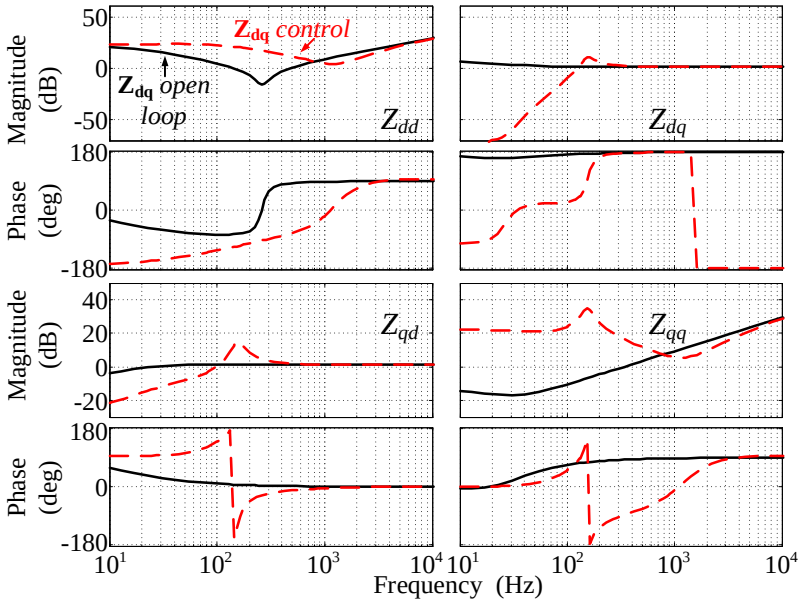


Fig. 2-51. AFE input impedance in *d-q* frame.

Fig. 2-51 shows the open-loop (black solid line) and closed-loop (red dash line) *d-q* frame input impedance of the VSC. As it can be observed, the open-loop impedance is a combination of the ac side inductor impedance (at high frequency) and the dc side impedance of capacitor and resistor (at low frequency) weighted by *d* channel and *q* channel duty ratios. After the closed-loop control (unity power factor control in this paper) is applied, the negative resistor impedance effect can be observed in the *d* channel impedance Z_{dd}, which is the main feature of the AFE input impedance, a direct result of its constant power load dynamics. In this case the higher the control bandwidth of the AFE voltage loop is, the wider the frequency range of the negative resistor is.When dc voltage is controlled, with certain load, AFE is a constant power load [39]. In the feedback control system shown in Fig. 2-50, output of dc voltage control loop gives the reference of *d* channel current. Then, dc side power is delivered through *d* channel from ac side. Eq. (2-32) reflects this relationship. After small-signal linearization process (Eq. (2-32) to Eq. (2-34)), Eq. (2-34) shows that Z_{dd} is a negative incremental resistor.

$$\frac{V_{dcAFE}^2}{R_{dc}} = I_d^s \cdot V_d^s = \left(I_d^s + \tilde{i}_d^s\right) \cdot \left(V_d^s + \tilde{v}_d^s\right) \tag{2-32}$$

$$I_d^s \cdot V_d^s = I_d^s \cdot V_d^s + I_d^s \tilde{v}_d^s + \tilde{i}_d^s V_d^s + \tilde{i}_d^s \tilde{v}_d^s \tag{2-33}$$

$$Z_{dd}\big|_{j\omega=0} = \frac{\tilde{v}_d^s}{\tilde{i}_d^s} = -\frac{V_d^s}{I_d^s} \tag{2-34}$$

2.4 D-Q Frame Impedance Measurement

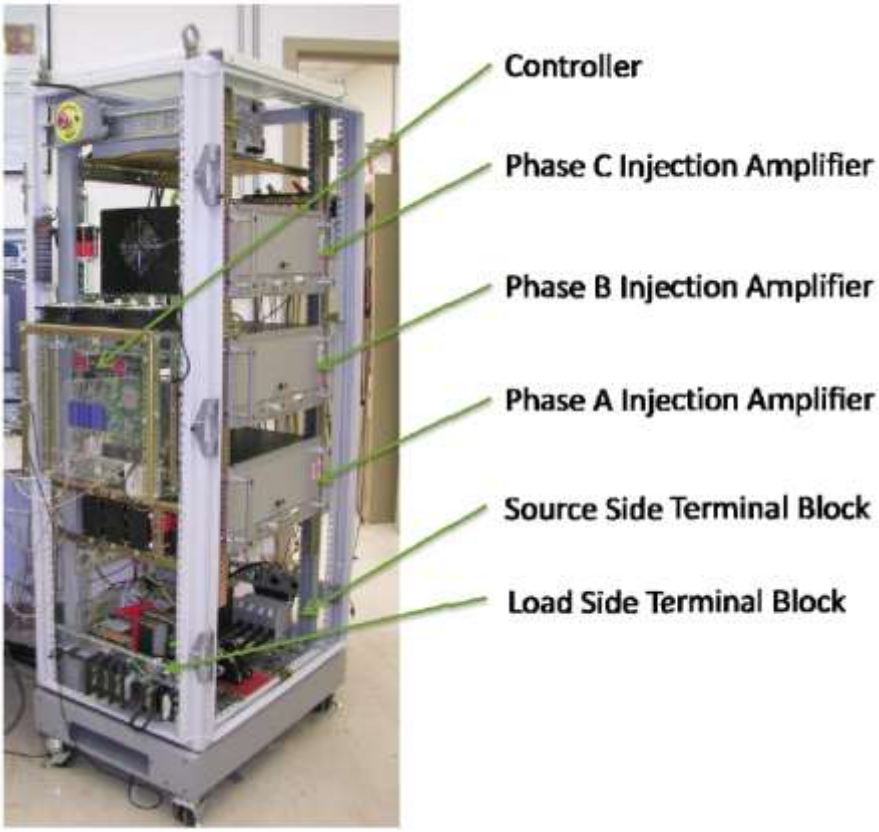


Fig. 2-52. *D-q* frame impedance tester.

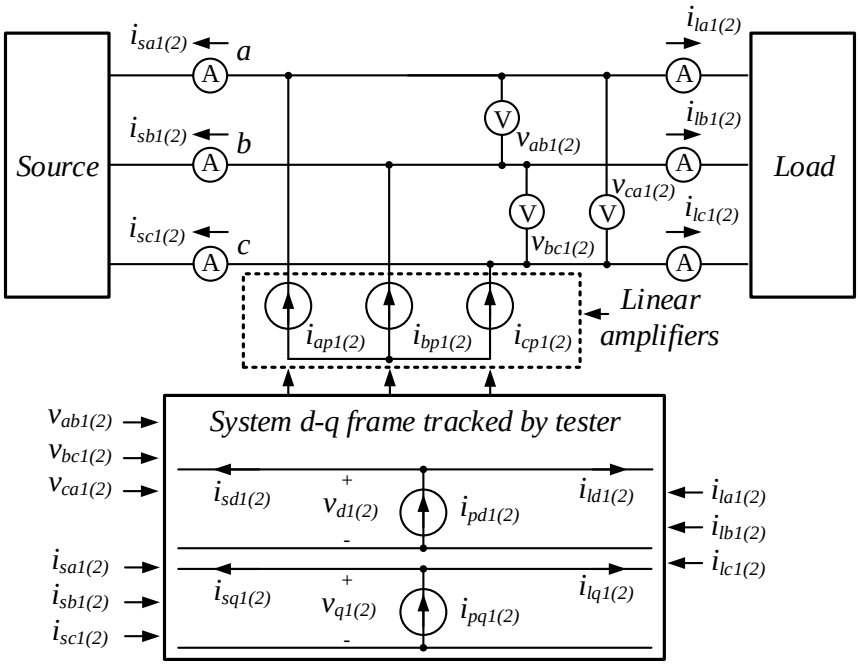


Fig. 2-53. *D-q* frame impedance measurement.

2.4.1 Algorithm

The measurement of impedances in the *d-q* frame needs special algorithms and equipment. This paper uses the impedance tester developed in [46] (see Fig. 2-52) to measure the source and load impedances in the *d-q* frame. As shown in Fig. 2-53, the tester first tracks the system angle in order to align with the system *d-q* frame, then a sinusoidal perturbation signal with certain frequency is generated on the *d*-axis (i_{pd1}) while keeping the *q*-axis perturbation null (i_{pq1}=0), and then converted into the *abc*-frame by a real-time micro-controller. Three linear amplifiers, controlled by the same real-time micro-controller, act as current injection devices and inject the current perturbations into the system at the ac interface. The system responses, namely the interface voltage and the currents of both source and load sides are measured and converted back into the *d-q* frame by the micro-controller. A second perturbation sequence is carried out then but perturbing the *q*-axis instead (i_{pq2}), with the d-axis components being zero (i_{pd2} = 0), which completes a set of two system response signals in the *d-q* frame. These are:

$$\begin{bmatrix} v_{d1} \\ v_{q1} \end{bmatrix}, \begin{bmatrix} i_{ld1} \\ i_{lq1} \end{bmatrix}, \begin{bmatrix} i_{sd1} \\ i_{sq1} \end{bmatrix}; \begin{bmatrix} v_{d2} \\ v_{q2} \end{bmatrix}, \begin{bmatrix} i_{ld2} \\ i_{lq2} \end{bmatrix}, \begin{bmatrix} i_{sd2} \\ i_{sq2} \end{bmatrix} \tag{2-35}$$

$$\mathbf{Z_{ldq}} = \begin{bmatrix} Z_{ldd} & Z_{ldq} \\ Z_{lqd} & Z_{lqq} \end{bmatrix} \tag{2-36}$$

$$\mathbf{Z_{sdq}} = \begin{bmatrix} Z_{sdd} & Z_{sdq} \\ Z_{sqd} & Z_{sqq} \end{bmatrix} \tag{2-37}$$

Let the subscripts 1 and 2 denote the variables measured during the two independent perturbations, and let (2-36) and (2-37) be the definition of the load and source impedance in the *d-q* frame. Then when measuring the load impedance $\mathbf{Z_{ldq}}$, the two perturbations yield:

$$\begin{bmatrix} v_{d1} \\ v_{q1} \end{bmatrix} = \begin{bmatrix} Z_{ldd} & Z_{ldq} \\ Z_{lqd} & Z_{lqq} \end{bmatrix} . \begin{bmatrix} i_{ld1} \\ i_{lq1} \end{bmatrix} \tag{2-38}$$

$$\begin{bmatrix} v_{d2} \\ v_{q2} \end{bmatrix} = \begin{bmatrix} Z_{ldd} & Z_{ldq} \\ Z_{lqd} & Z_{lqq} \end{bmatrix} . \begin{bmatrix} i_{ld2} \\ i_{lq2} \end{bmatrix} \tag{2-39}$$

Notice that since the system is the same, the impedance must remain unchanged. Then equations (2-38) and (2-39) containing v_{d1} and v_{d2} can be regrouped as in (2-40), and the equations containing v_{q1} and v_{q2} can be regrouped as in (2-41).

$$\begin{bmatrix} v_{d1} \\ v_{d2} \end{bmatrix} = \begin{bmatrix} i_{ld1} & i_{lq1} \\ i_{ld2} & i_{lq2} \end{bmatrix} . \begin{bmatrix} Z_{ldd} \\ Z_{ldq} \end{bmatrix} \tag{2-40}$$

$$\begin{bmatrix} v_{q1} \\ v_{q2} \end{bmatrix} = \begin{bmatrix} i_{ld1} & i_{lq1} \\ i_{ld2} & i_{lq2} \end{bmatrix} . \begin{bmatrix} Z_{lqd} \\ Z_{lqq} \end{bmatrix} \tag{2-41}$$

Eq. (2-40) and (2-41) in turn can similarly be regrouped as:

$$\begin{bmatrix} v_{d1} & v_{d2} \\ v_{q1} & v_{q2} \end{bmatrix} = \begin{bmatrix} Z_{ldd} & Z_{ldq} \\ Z_{lqd} & Z_{lqq} \end{bmatrix} . \begin{bmatrix} i_{ld1} & i_{ld2} \\ i_{lq1} & i_{lq2} \end{bmatrix} \tag{2-42}$$

Then the load impedance can be calculated as (2-43). A similar process is followed to derive the source impedance $\mathbf{Z_{sdq}}$ in (2-44).

$$\begin{bmatrix} Z_{ldd} & Z_{ldq} \\ Z_{lqd} & Z_{lqq} \end{bmatrix} = \begin{bmatrix} v_{d1} & v_{d2} \\ v_{q1} & v_{q2} \end{bmatrix} \cdot \begin{bmatrix} i_{ld1} & i_{ld2} \\ i_{lq1} & i_{lq2} \end{bmatrix}^{-1} \tag{2-43}$$

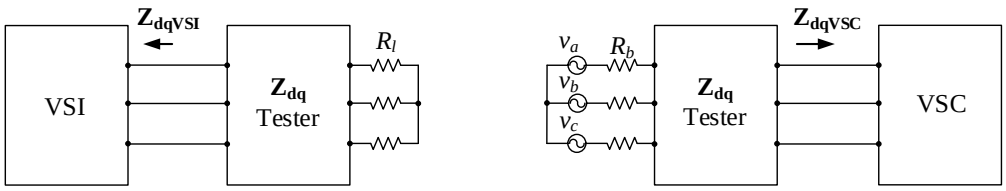
$$\begin{bmatrix} Z_{sdd} & Z_{sdq} \\ Z_{sqd} & Z_{sqq} \end{bmatrix} = \begin{bmatrix} v_{d1} & v_{d2} \\ v_{q1} & v_{q2} \end{bmatrix} \cdot \begin{bmatrix} i_{sd1} & i_{sd2} \\ i_{sq1} & i_{sq2} \end{bmatrix}^{-1} \tag{2-44}$$

2.4.2 Measurement Setup

To measure the output impedance of the VSI, its load is replaced by a three-phase resistor (R_l) of equal power as shown in Fig. 2-54 (a). The *d-q* impedance tester is then inserted in between the VSI and the three-phase resistors. The setup for the AFE input impedance measurement is shown in Fig. 2-54 (b), where in this case its source is replaced by a three-phase voltage source. A 0.5 Ω three-phase resistor (R_b) is additionally connected between the impedance tester and this voltage source in order to increase its total output impedance, which improves the measurement results. This is so since the voltage response (measurement) at the interface is larger when the impedance of the system is increased. The voltage source amplitude is then adjusted to make the VSC input voltage the same as when the source is the VSI. Actually, for system integration, impedances of source and load equipment are usually tested by suppliers separately using resistive load (for source converter) an ideal voltage source (for load converter) to check the system stability before they are connected by system integrator.

In this discussion, both the VSI output impedance and the AFE input impedance in the *d-q* frame were measured from 40 Hz to 10 kHz with 100 frequency points [46]. Because of frequency of instability in the electrical system under study, the measurement frequency range is chosen as such. The system line frequency is 400 Hz. Frequency of instability in the system under study is between 40 Hz to 10 kHz. For other applications, for example, 60 Hz system, instability could happen below 1 Hz, corresponding impedance testers should have the ability to measure impedance lower than 1 Hz. Upper limit of impedance measurement is chosen as half

switching frequency of converters in the system, where the small-signal model extract from the system is still a good linear approximation of the system. In this paper the switching frequencies of VSI and VSC are 20 kHz, 10 kHz is set to be the upper limit of impedance measurement. For different application, switching frequency of power converter is different. For 60 Hz system where power rating could be megawatt and several kilo hertz could be the switching frequencies of most power converters. Then, impedance measurement up to 1 kHz is sufficient. For transportation electrical system, high switching frequency (over 20 kHz) is preferred to reduce the size of magnetic components, impedance measurement can be higher than 10 kHz.



(a) (b)

Fig. 2-54. Measurement setups: (a) output impedances, (b) input impedances.

2.4.3 Experimental Results

The *d-q* impedance tester is used to verify the output impedances model of VSI. Fig. 2-55 shows the comparison of analytical results (green lines) and the experimental measurement results (blue lines) for VSI output impedance for open loop with paramters in Table 2-1. Fig. 2-56 shows the results with current feedback control (k_{pi} = 0.0465; k_{ii} = 121.01). Fig. 2-57 shows the comparison of analytical results (green lines) and the experimental measurement results (blue lines) for VSI output impedance with both current and voltage feedback (k_{pv} = 0.0297; k_{iv} = 78.54) control. All the measurement results match with the results predicted by the model very well.

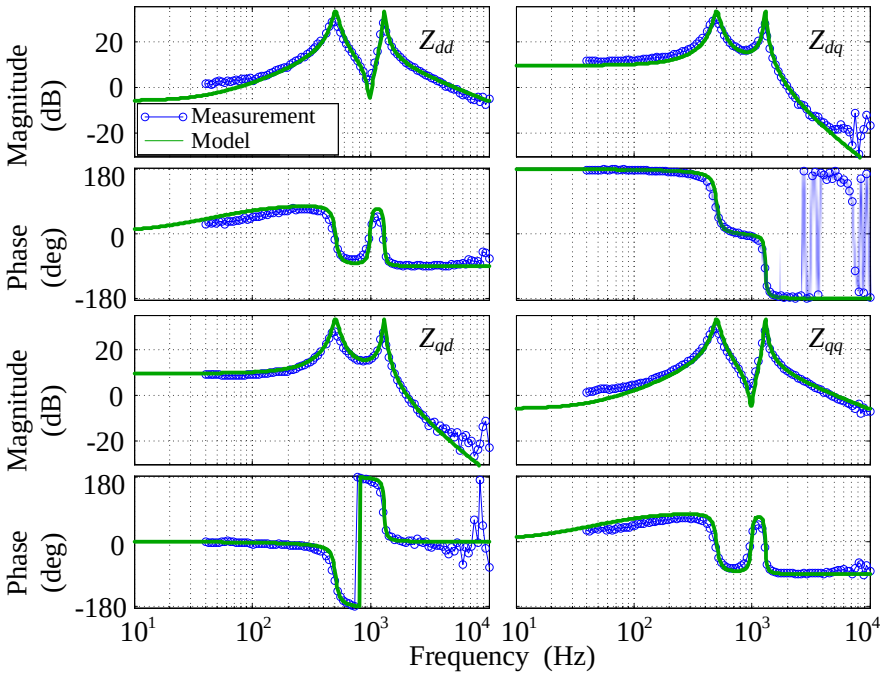


Fig. 2-55. Measurement results compare with model for open loop.

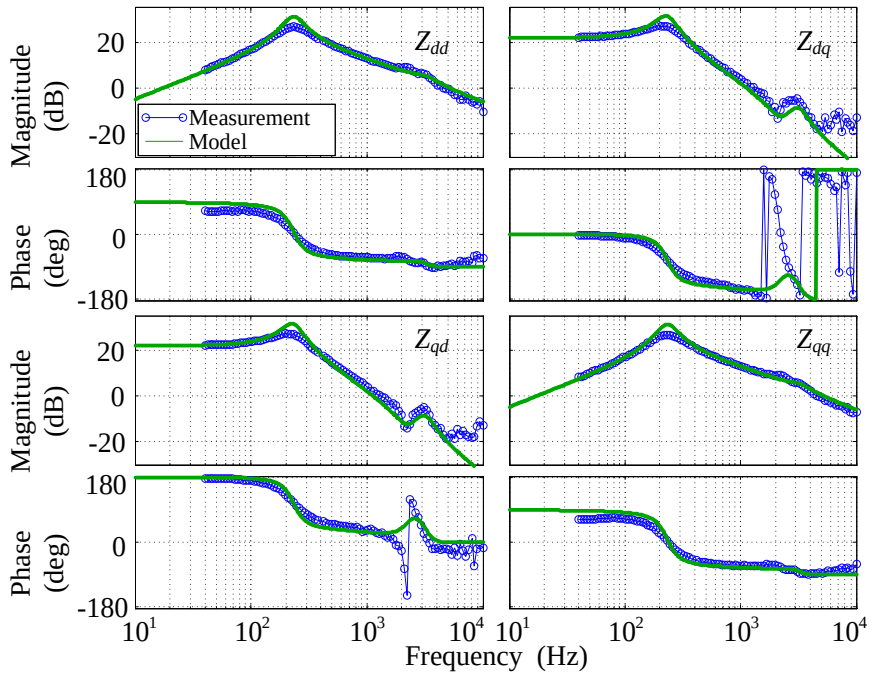


Fig. 2-56. Measurement results compare with model for current loop control.

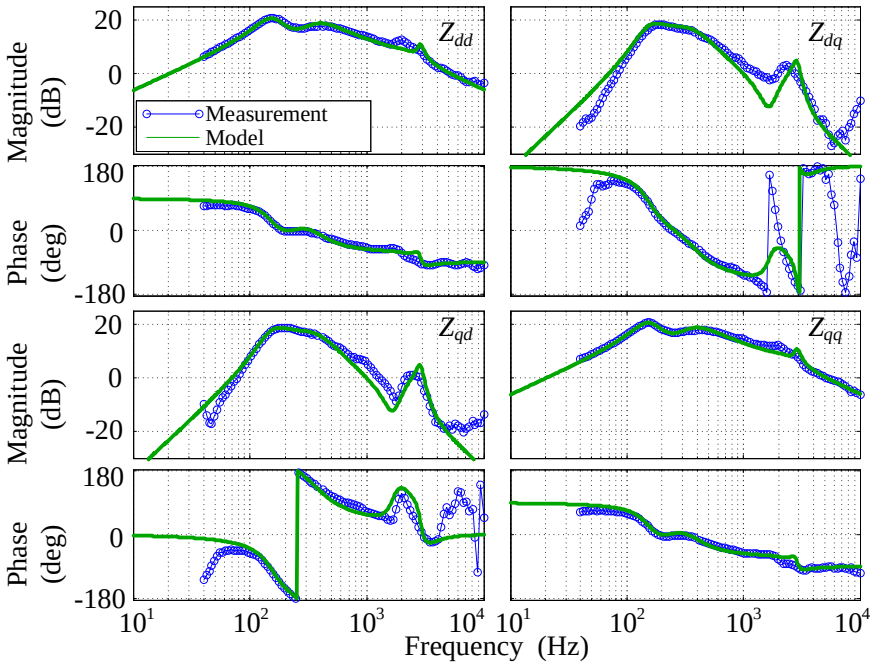


Fig. 2-57. Measurement results compare with model for voltage control.

2.5 Phase-Locked Loop

As discussed in the beginning of this chapter, AFE needs synchronously work with the ac bus which it is connected to. So does the grid-tied inverter. PLL technique is currently the most adopted solution [63], [64]. One of the big part of this disseratoin is to discuss the influence of PLL to the impedances of AFE and grid-tied inverter. It is necessary to give brief discussion of the basics of PLL. Synchronous-reference frame (SRF) PLL, as shown in Fig. 2-58 is a very basic solution [63], [64] in three-phase applications, and many advanced PLLs are derived from it. It is considered firstly. The SRF transformation matrix is shown in Eq. (2-45).

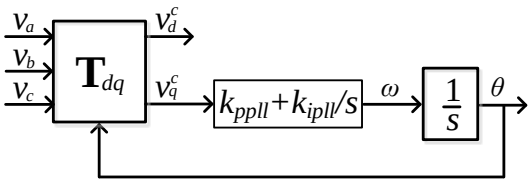


Fig. 2-58. SRF PLL.

$$\mathbf{T}_{dq} = \frac{2}{3}\begin{bmatrix} \cos(\theta) & \cos\left(\theta - \frac{2}{3}\pi\right) & \cos\left(\theta + \frac{2}{3}\pi\right) \\ -\sin(\theta) & -\sin\left(\theta - \frac{2}{3}\pi\right) & \sin\left(\theta + \frac{2}{3}\pi\right) \end{bmatrix} \tag{2-45}$$

In *d-q* frame, the average model of PLL is shown in Fig. 2-59, where $\mathbf{T}_{\Delta\theta}$ is shown in Eq. (2-31). Small-signal model shown in Fig. 2-60 is utilized to design the loop filter [94].

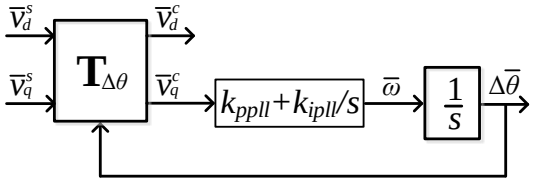


Fig. 2-59. Average model of SRF PLL.

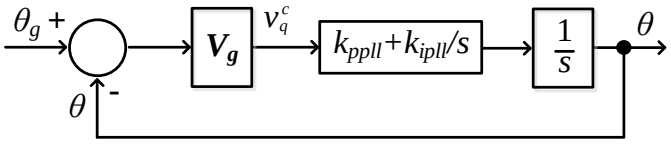


Fig. 2-60. Small-signal model of SRF PLL with ideal grid.

One important issue in PLL design is the double line frequency ripple caused by three-phase unbalance. Decoupled Double SRF (DDSRF) [89], as shown in Fig. 2-61, is an effective strategy to migrate the double line frequency ripple. The dynamic of decoupling term is modeled as transfer function matrix **H** in Fig. 2-62. The expression of **H** can be found in [90], and it is shown from Eq. (2-46) to (2-50).

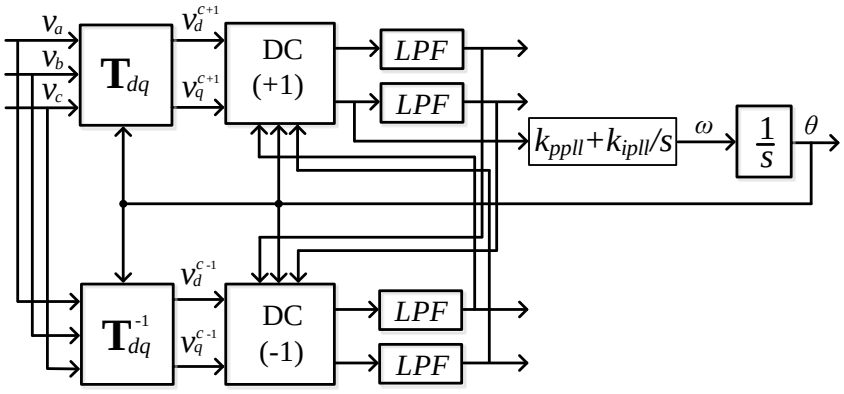


Fig. 2-61. DDSRF PLL.

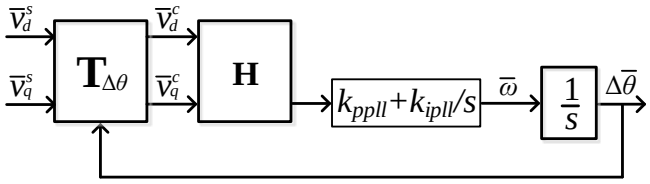


Fig. 2-62. Average model of DDSRF PLL.

$$\mathbf{H}=\begin{bmatrix} H_{11} & H_{12} \\ H_{21} & H_{22} \end{bmatrix} \tag{2-46}$$

Where,

$$H_{11}=H\left(s^3+2\omega_f s^2+4\omega^2 s+4\omega_f\omega^2\right) \tag{2-47}$$

$$H_{22}=H_{11}\frac{s+\omega_f}{\omega_f} \tag{2-48}$$

$$H_{12}=-H_{21}=-H(2\omega_f\omega s) \tag{2-49}$$

$$H=\frac{\omega_f}{s^4+4\omega_f s^3+4\left(\omega_f^2+\omega^2\right)s^2+8\omega_f\omega^2 s+4\omega_f^2\omega^2} \tag{2-50}$$

The Low-Pass Filter (LPF) in Fig. 2-61 is:

$$LPF = \frac{\omega_f}{s + \omega_f} \tag{2-51}$$

Chapter 3 Small-signal Stability in the Presence of Constant Power Load

3.1 Introduction

This chapter presents, for the first time, the small-signal stability analysis of a balanced three-phase ac system with constant power loads based on the GNC and measured impedances in *d-q* frame. To this end, three experiments are shown for stable, critical stable, and unstable conditions, demonstrating the stability prediction accuracy of the approach. Furthermore, results in the time and frequency domains are put side-by-side to show the effectiveness of the stability analysis based on the measured impedances. This also validates the assumptions previously made to study the stability of ac systems using the GNC and simulation-based analysis. Specifically, using the *d-q* impedance measurement algorithm and equipment developed in [46], this paper studies the small-signal stability of an ac system comprised of a voltage source inverter (VSI) feeding a boost rectifier or voltage source converter (VSC) in this chapter, in what is regarded a very generic system configuration. In effect, it could represent many applications, for example, an uninterruptable power supply feeding an active load in a building, or an ac subsystem within a microgrid as shown in Fig. 3-1. Accordingly, the analysis presented is kept as generic as possible to be representative of any such ac system interface. Stable and unstable conditions then are created by adjusting the voltage control bandwidth of the VSI, where by measuring the source (VSI) output impedance and the load (VSC) input impedance the GNC is applied characterizing the stability conditions at the ac interface.

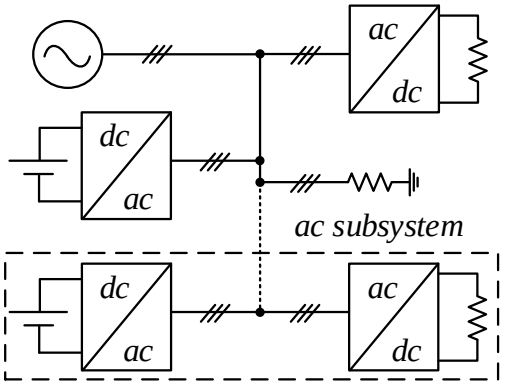


Fig. 3-1. Experimental ac system used for stability analysis.

3.2 System Setup and Parameters

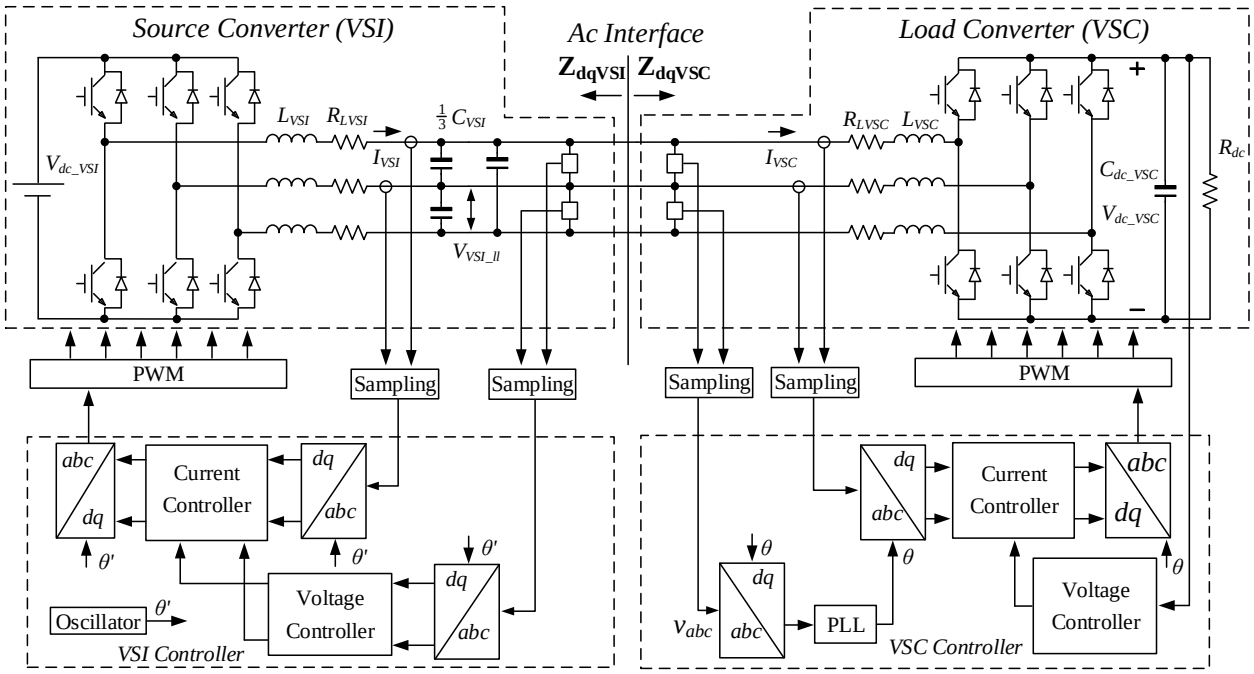


Fig. 3-2. Experimental system setup and control scheme.

Fig. 3-2 shows the circuit schematic and control system block diagram of the experimental setup where the VSI, VSC, and ac interface of interest are clearly identified. At this interface, the VSI closes its outer control loop regulating the ac bus voltage V_{VSI_ll}, from where the VSC draws its current I_{VSC}. As such, the VSI output impedance $\mathbf{Z_{dqVSI}}$ and the VSC input impedance $\mathbf{Z_{dqVSC}}$

seen at this interface are solely of each converter's parameters and do not depend on each other's components and control systems. Also, when performing the measurements this interface is a common coupling point fully accessible from the exterior of the VSI and VSC cabinets.

The parameters of this system are listed in Table 3-1.

Table 3-1. Experimental system parameters.

Symbol	Description	Value
V_{dc_VSI}	VSI input dc voltage	270 V
V_{VSI_ll}	VSI output line-line rms voltage	99.6 V
f	VSI output voltage frequency	400 Hz
L_{VSI}	Inductance of VSI output inductor	970 μH
R_{LVSI}	Resistance of VSI output inductor self-resistor	120 mΩ
C_{VSI}	Capacitance of VSI output capacitor	31.8 μF
L_{VSC}	Inductance of VSC boost inductor	470 μH
R_{LVSC}	Resistance of VSC boost inductor self-resistor	90 mΩ
V_{dc_VSC}	VSC output dc voltage	270 V
C_{dc_VSC}	Capacitance of VSC output capacitor	100 μF
R_{dc}	Resistance of VSC load resistor	96 Ω
R_l	Resistances of resistor load for VSI output impedance test	13 Ω
R_b	Resistances of resistor for VSC input impedance test	0.5 Ω

As seen, the control systems of both converters are implemented in the *d-q* frame. For the VSI, the inductor currents are measured in the inner current control-loop, and the capacitor voltages are measured in the outer voltage control-loop. For the VSC, the input terminal voltages are measured by the Phase-Locked Loop (PLL) in order to estimate the phase of the ac bus voltage and synchronize the converter operation. The PLL scheme implemented is based on the positive-sequence *d-q* frame transformation [64]. The boost inductor currents are measured in the inner current control-loop, and the output capacitor voltage is measured in the outer voltage control-loop. All the regulators employed use a Proportional and Integral (PI) structure, and no

dynamic decoupling schemes were implemented between *d-q* axis variables. Both control systems are run on a single Digital Signal Processor (DSP) control board, at a sampling rate of 20 kHz. All analog signals are previously conditioned via a second-order Sallen-Key low pass Butterworth filter with a 200 kHz cutoff frequency. Continuous Space Vector Modulation (SVM) was used as Pulse Width Modulation (PWM) scheme for both converters [73].

3.3 Description Of Experimental Tests Conducted

The most intuitive way of making the system unstable is to increase the VSI output impedance, which can be accomplished by decreasing the bandwidth of its output voltage control-loop. In this study accordingly, the VSC control parameters were kept constant, and only the VSI voltage controller is adjusted to create stable and unstable conditions. Specifically, feedback controllers of VSI and VSC are list in

Table 3-2. Using the average models of VSI and VSC together with their controllers, three cases are considered as shown in Fig. 3-3, which are bode plots of VSI output impedances and VSC input impedance. As list in

Table 3-2, from case 1 to case 3, parameters of PI controller in VSI voltage control loop are decreased. As a result, output impedance of VSI increases from case 1 to case 3. Input impedance of VCS is kept unchanged from case 1 to case3. Using the simulated *d-q* impedances, characteristic loci ($\lambda_{1\_case1\_sim}$, $\lambda_{2\_case1\_sim}$) of return ratio ($\mathbf{Z}_{\_VSI\_case1\_sim}*(\mathbf{Z}_{\_VSC\_sim})^{-1}$) which are shown in Fig. 3-4 indicate the system is stable. Time domain response of interface voltage when VSI is loaded by VSC in *d-q* frame, which is shown in Fig. 3-5 (a), indicates the prediction of GNC is correct. In case 2, the loci indicate the system is still stable, but $\lambda_{1\_case2\_sim}$ is very close to the critical point, it intersects with the unit cycle at 83 Hz. This means there is a damped oscillation with 83 Hz in the system, and this is shown in the time domain simulation results in Fig. 3-5 (b). Case 3 is an unstable case. $\lambda_{1\_case3\_sim}$ encircles the critical point, it intersects with the unit cycle at 53 Hz. this means the time domain response has an intensified oscillation with 53 Hz. This is verified by simulation results in Fig. 3-5 (c).

Table 3-2. Feedback controller parameters for VSI and VSC.

	VSI		**VSC**	
	Voltage loop	Current loop	Voltage loop	Current loop
Case 1	0.0495 + 130/s	0.0465 + 121/s	0.0462 + 4.58/s	0.0116 + 46.5/s
Case 2	0.0297 + 78.5/s			
Case 3	0.0158 + 41.9/s			

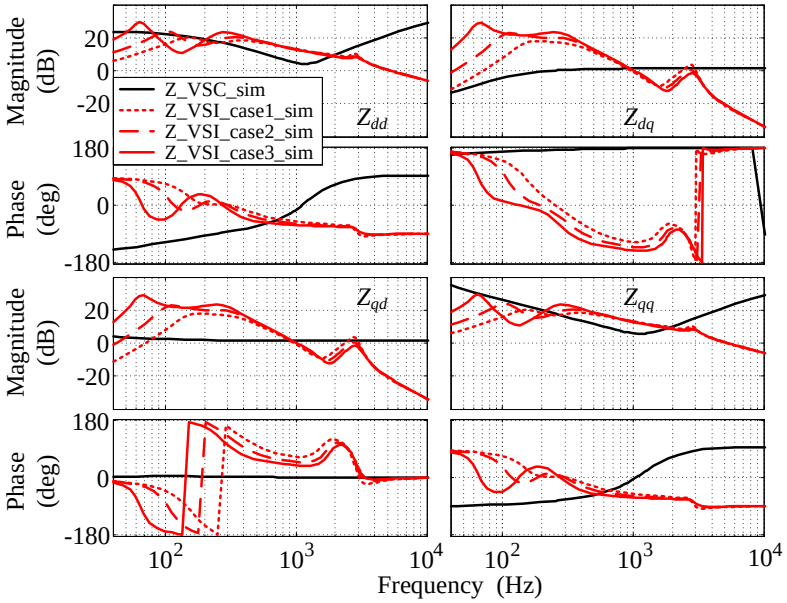


Fig. 3-3. Impedances of VSI and VSC for three cases from average model simulation.

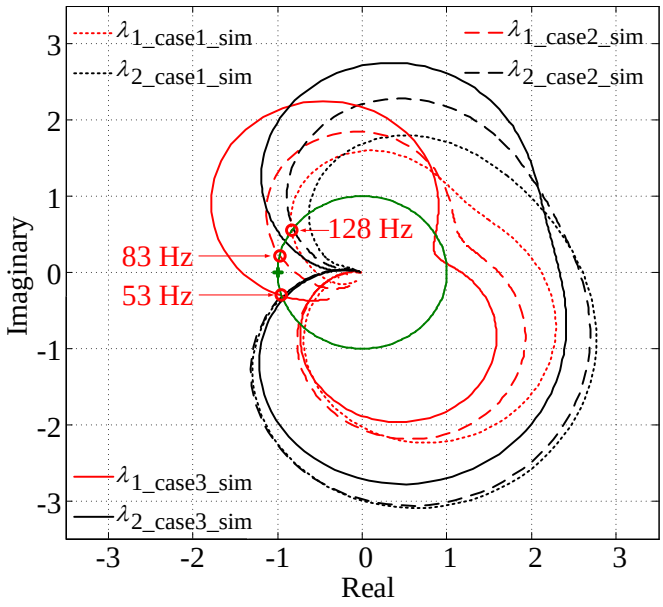
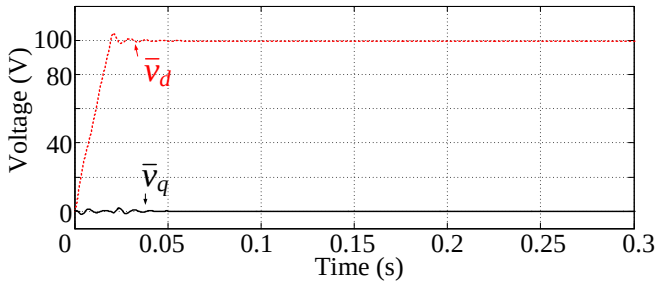
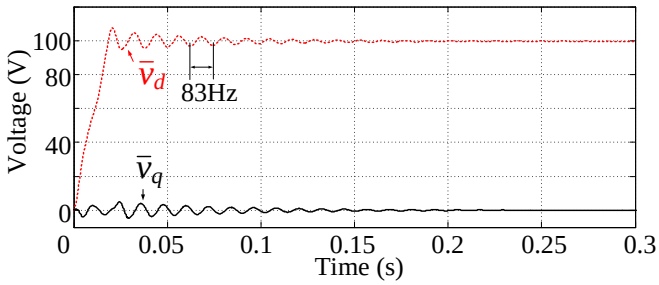


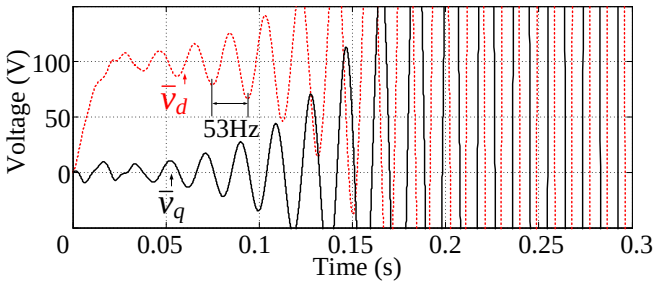
Fig. 3-4. Characteristic loci of three cases using simulated impedance from average model.



(a) case 1.



(b) case 2.



(c) case 3.

Fig. 3-5. Time domain simulation of interface voltage in *d-q* frame.

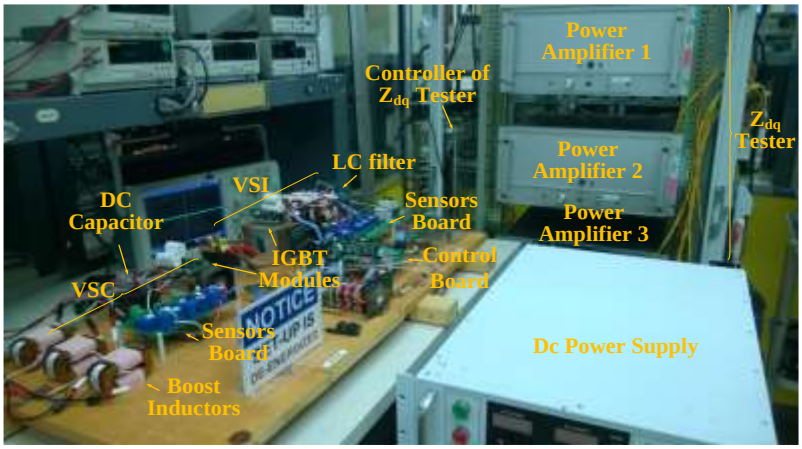


Fig. 3-6. Test-bed hardware prototype for experimental system.

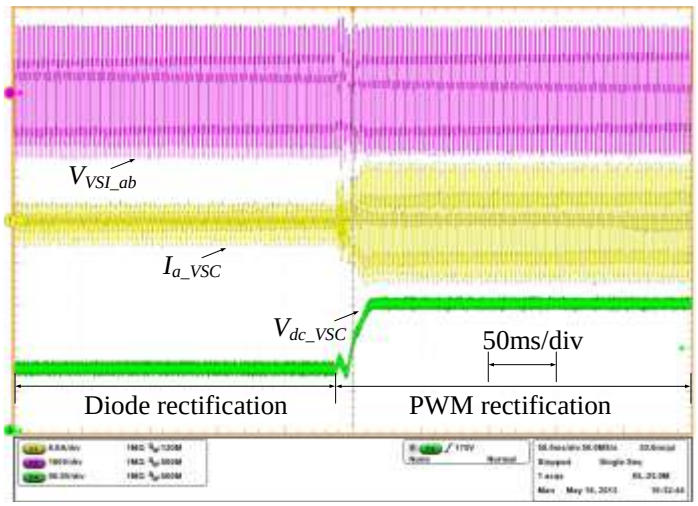
3.4 Experimental Results

Using the test-bed hardware prototype shown in Fig. 3-6, experimental results of three cases discussed before are shown in this section. Fig. 3-7 shows the measurement results of case 1, the stable case. Specifically, Fig. 3-7 (a) shows the time domain waveforms showing the rectifier starting up until it reaches steady state. Fig. 3-7 (b) is the zoomed in view of the steady state waveforms. Fig. 3-7 (c) shows the Bode plot of the impedance matrices, where it is clear that the *d-d* channel impedance (Z_{dd}) of the VSC is negative at lower frequencies. Using the measured impedances, the return-ratio matrix ($\mathbf{Z_{sdq}}\,\mathbf{Y_{ldq}}$) is calculated and its characteristic loci is obtained as shown in Fig. 3-7 (d). As evinced, none of the loci encircles the critical point (–1+j0) indicating that the system is stable.

The second test corresponds to case 2, the critical stable condition. Specifically, when the PI parameters of VSI voltage control loop are decreased, the system becomes less stable as it can be observed from the time domain waveforms shown in Fig. 3-8 (a). In effect, when the PWM control of the VSC starts, a damped oscillation with a frequency of 80 Hz can be found in the system. This was not observable in case 1. Nonetheless, the system is still stable according to the characteristic loci plot shown in Fig. 3-8 (d), but the distance between the critical point (–1+j0) and the loci is less than that seen in case 1. Further, one of the characteristic loci, $\lambda_{1\_case2\_exp}$, intersects the unit circle at 81.7 Hz approximately, which corresponds to the damped oscillation observed in time domain waveforms.

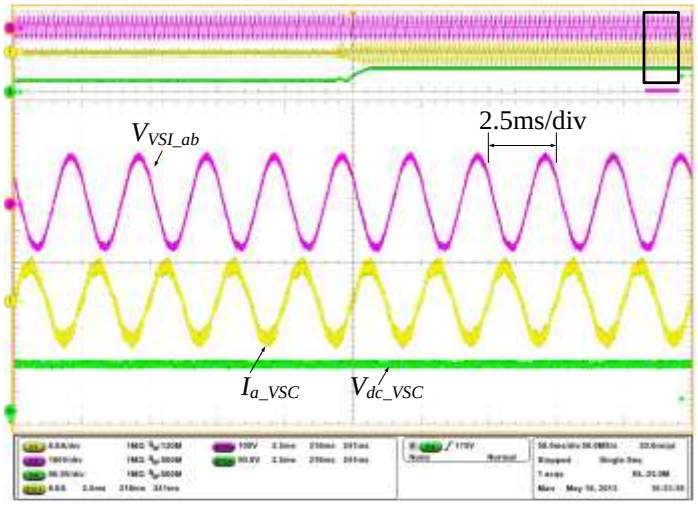
Lastly, in case 3, the unstable condition, the PI parameters of VSI voltage control loop are further decreased. As shown in Fig. 3-9 (a) the system becomes unstable as soon as the PWM control of the VSC starts. The characteristic loci plot in Fig. 3-9 (d) agrees with this conclusion. In effect, when the PWM control of the VSC starts an unstable oscillation with frequency of 50 Hz appears in the system, which can be verified by the loci shown in Fig. 3-9 (d), as the loci of $\lambda_{1\_case2\_exp}$ intersects the unit circle around 49.8 Hz.

As seen, the experimental results obtained from both time domain and frequency domain show that the stability analysis based on measured impedances has good accuracy, which can be observed both in the impedance Bode plots and in the characteristic loci of the return-ratio matrix eigenvalues.

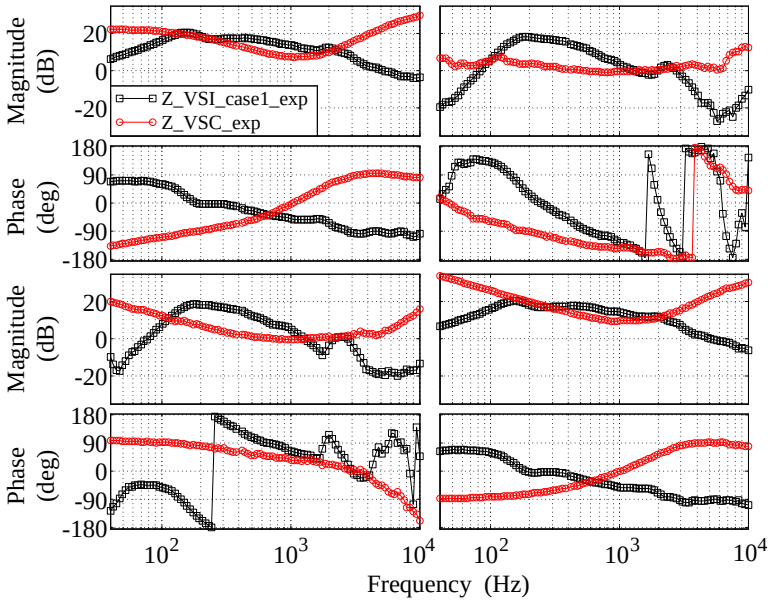


(a) Time domain results.

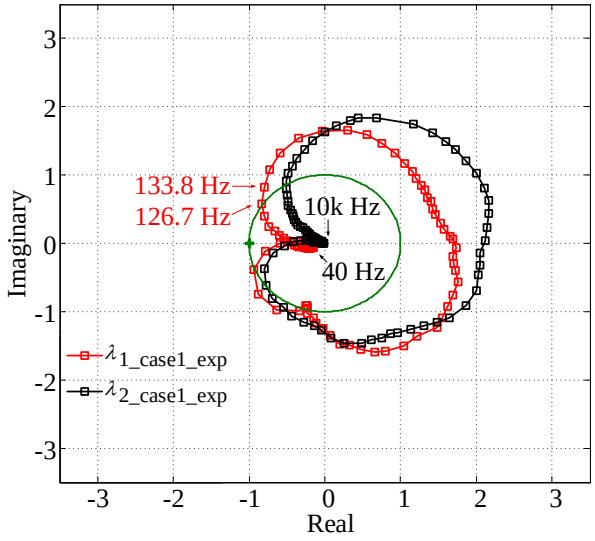
Interface a to b voltage (V_{VSI_ab}) (purple) [100 V/div], VSC phase a current (I_{a_VSC}) (yellow) [6 A/div], VSC output voltage (V_{dc_VSC}) (green) [90 V/div]



(b) Zoomed in time domain results.

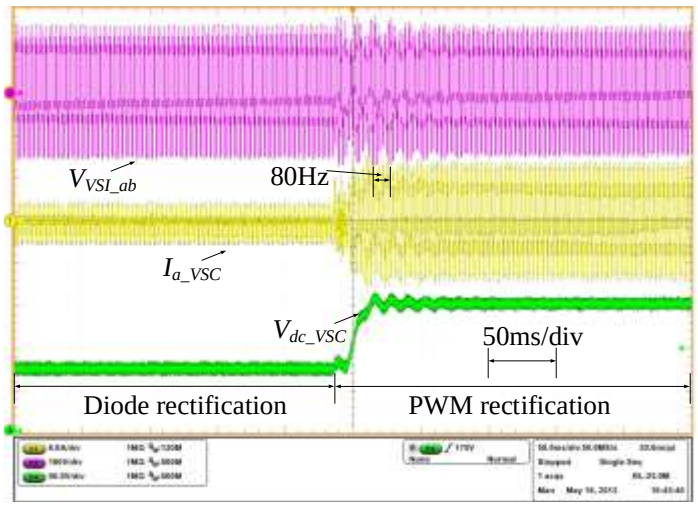


(c) VSI and VSC *d*-*q* impedance.



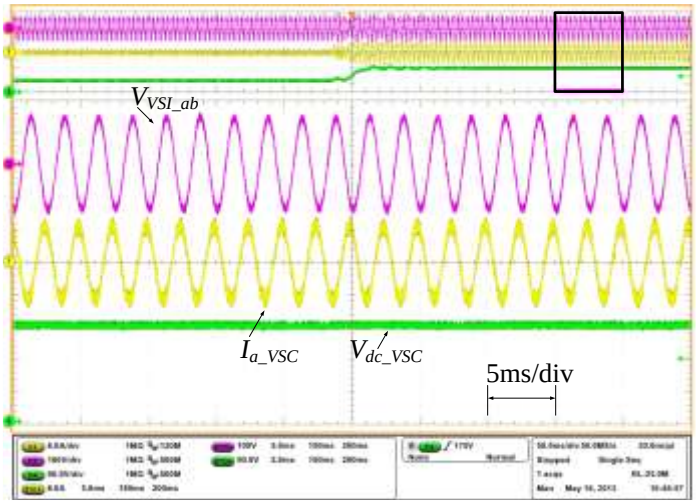
(d) Characteristic loci plot.

Fig. 3-7. Measurement results of case 1.

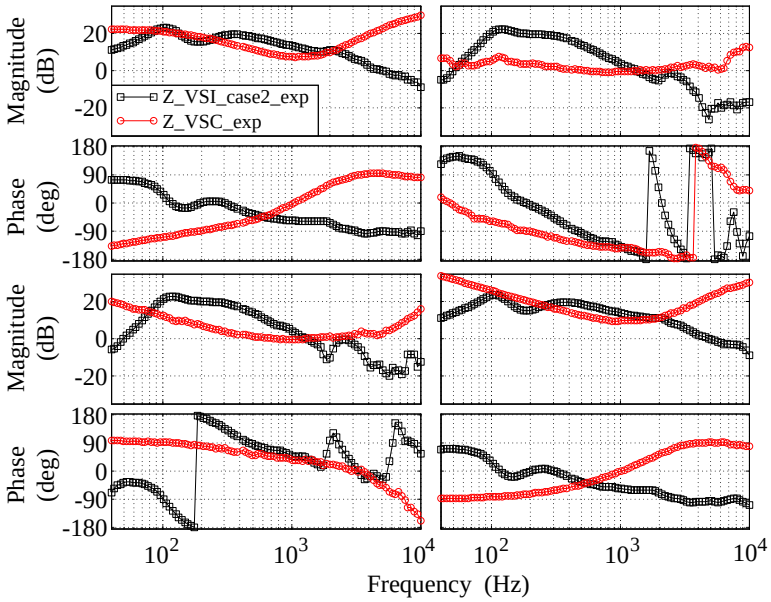


(a) Time domain results.

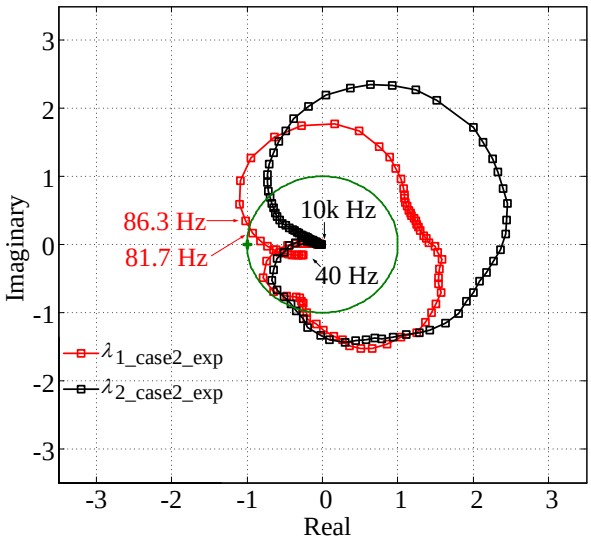
Interface a to b voltage (V_{VSI_ab}) (purple) [100 V/div], VSC phase a current (I_{a_VSC}) (yellow) [6 A/div], VSC output voltage (V_{dc_VSC}) (green) [90 V/div]



(b) Zoomed in time domain results.

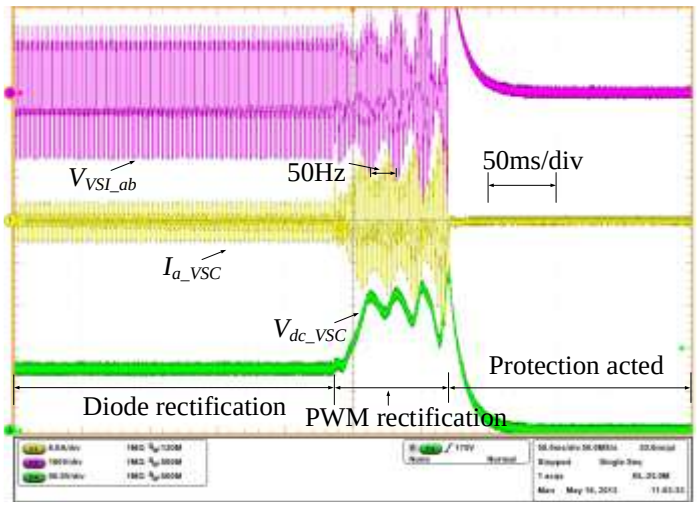


(c) VSI and VSC *d*-*q* impedance.



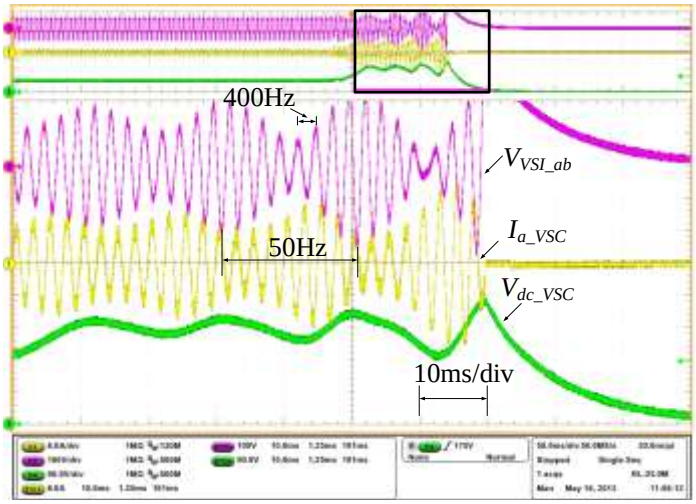
(d) Characteristic loci plot.

Fig. 3-8. Measurement results of case 2.

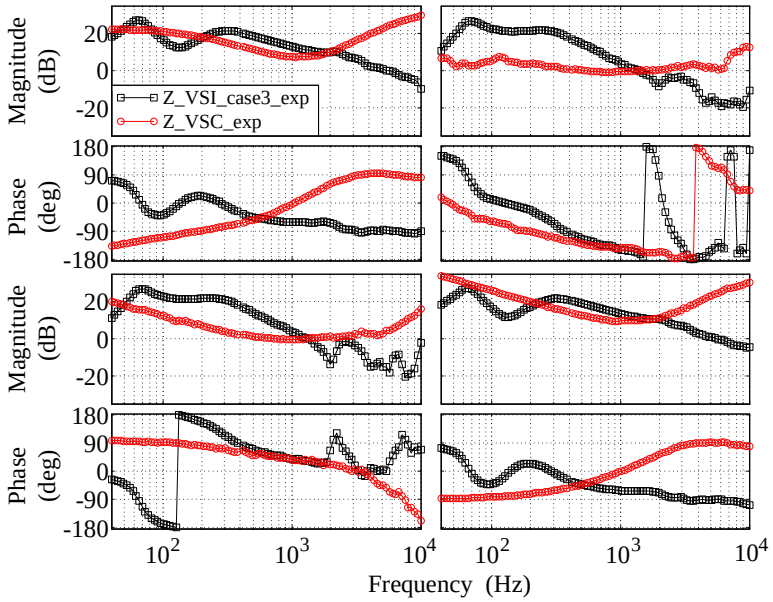


(a) Time domain results.

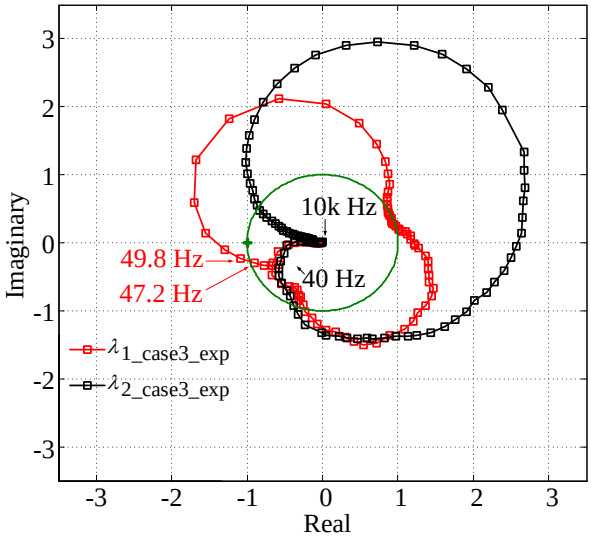
Interface a to b voltage (V_{VSI_ab}) (purple) [100 V/div], VSC phase a current (I_{a_VSC}) (yellow) [6 A/div], VSC output voltage (V_{dc_VSC}) (green) [90 V/div]



(b) Zoomed in time domain results.



(c) VSI and VSC *d-q* impedance.



(d) Characteristic loci plot

Fig. 3-9. Measurement results of case 3.

3.5 Discussion

In section 3.3, impedances extracted from average models can predict system stability accurately in simulation. This is shown by Fig. 3-3 and Fig. 3-4 in frequency domain and

verified by Fig. 3-5 in time domain both in *d-q* frame. These results represent the original theory of stability analysis using GNC for balanced three-phase ac system. However, it has been observed that in practice, a lot of uncertainties exit which can influence the robustness of the analysis. GNC-based small-signal stability analysis for three-phase ac system requires: first, the three-phase ac system is balanced, second, *d-q* impedances of the practical system are measured accurately. Three is no ideal balanced three-phase ac system in practice. On the other hand, *d-q* impedance tester relays on PLL to track the system *d-q* frame and measure impedances. The accuracy of phase tracking influence the measurement accuracy of impedances and further the stability analysis.

Unbalance of the experimental system in this paper is kept less than 1%. PLL bandwidth of *d-q* impedance tester utilized in this paper is 1 Hz to assure a good phase tracking accuracy. Under such condition, stability prediction using GNC in experiments shows very good accuracy for the system under study. Still the paper does not study the robustness of the stability analysis using GNC, it is an important topic to be explored in the future.

When comparing the simulation results with experimental results, it can be found that, although they give same conclusion on the stability condition of the system under study, the oscillation frequencies of the system are different in the two studies. When comparing impedances of the system in high frequency, there are more differences between simulation and experimental results. In order to achieve such agreement between simulation and experimental results, a lot of model verification and validation work have been done. Model validation needs measurement of from real hardware. This paper presents for the first time, the small-signal stability analysis of three-phase ac system in the presence of constant power loads based on measured *d-q* frame impedances. This work not only demonstrates the feasibility of using GNC in practice, but also opens the door of model validation for stability analysis using GNC in three-phase ac system.

The experimental results also demonstrate that three-phase PWM rectifiers with output voltage control are constant power loads, when the source impedance is high, they can make the system unstable. From the experimental study, simple design guidance can be provided regarding

ac system with controlled PWM rectifiers. First, in order to make the system stable, source impedance should be kept small. This can be achieved by increasing the voltage control bandwidth of the source as shown in this paper. Also, reducing the output voltage control bandwidth of the rectifier could also stabilized the system. Weak output voltage control reduces the frequency range of constant power load behavior of three-phase PWM rectifier which consequently stabilizes the system.

Stability analysis using GNC relies on plotting characteristic loci of the system. Characteristic loci are calculated from impedances of source and load. Stability cannot be judged intuitively from impedances interaction as what has been done in dc system. Although some initial work has been reported to simplify stability analysis using GNC for three-phase system [72] under certain condition, more efforts are needed before simple design guidance can be provided based on impedances.

Chapter 4 Modeling of Voltage Source Converters Including Phase-locked Loop

4.1 Introduction

As discussed in the previous chapter, grid-tied VSCs need PLL to synchroniously work with the grid. These VSCs can be broadly divided as grid-tied inverter and acitive front-end (AFE) rectifeirs.

Grid-tied inverters are the key components which deliver renewable energy to the grid [62], [74]. They are typically controlled as current sources injecting current to the grid. With the increasing penetration of renewable energy resources, power quality and stability issues induced by grid-tied inverters becomes more and more important [75]–[79]. Harmonic pollution could happen due to the interaction between inverter and grid impedance [75], [77], [79]. Large grid impedance could destabilize the inverter system [66], [76]. In order to deliver power to the grid, frequency and phase angle of inverter output current should synchronize with grid voltage which is usually served by PLL [63], [64]. Some recent literatures discovered that PLL has negative impact to the system stability [66], [80]–[84].

Both harmonic and stability issue can be studied using inverter small-signal impedance. Small-signal impedances of power converters are the linearization around their dc operation points. For three-phase ac system, no dc operation point exits in stationary frame. By doing transformation from stationary frame to synchronous reference (*d-q*) frame, three-phase ac system becomes two coupled dc system. Small-signal impedances in *d-q* frame can then be derived by doing traditional linearization [66], [39], [41], [81]. Different from impedances of dc-dc converters, impedances of three-phase ac converters are 2-by-2 matrices. Measurement techniques and devices for *d-q* frame impedances are also developed [44]–[48]. Small-signal stability of three-phase ac system can then be analysis based on *d-q* impedances and generalized Nyquist Criterion. Recently, small-signal impedances and stability analysis of three-phase converters are also developed in stationary frame using harmonic linearization on ac signals [67],

[77], [71], [82]. This paper focuses on the traditional *d-q* impedance analysis in synchronous reference frame.

D-q small-signal impedance analysis of three-phase grid-tied converters have been reported for rectifiers without considering the effect of PLL [41], [39]. Ref. [66] models the effect of PLL by introducing system and converter *d-q* frames. It shows that high bandwidth PLL increases the negative real part of inverter output impedance which could destabilize the system [66], [67]. Ref. [81] models the influence of PLL on the input impedance of three-phase boost rectifier. Ref. [81] gives the full impedance model of grid-tied inverter considering current feedback control and PLL in *d-q* frame. The model shows that PLL shapes *q-q* channel output impedance of grid-tied inverter as a negative resistor within its bandwidth. Later on, Ref. [85] also shows the same conclusion using model which ignores the coupling effect between *d*-channel and *q*-channel. This model predicts the inverter impedances well for unity power factor application where coupling effect can be ignored. However, for three-phase system with reactive power, coupling effect between *d* and *q* channels is significant, this model cannot predict the impedance under this condition.

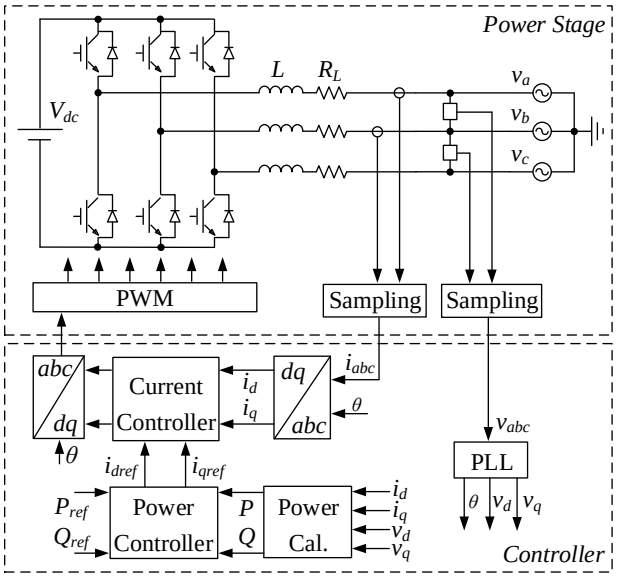


Fig. 4-1. Grid-tied inverter with feedback control and PLL.

Differently, this chapter proposes a full analytical model for the output impedance of the three-phase grid-tied inverter in the *d-q* frame considering the effect of PLL, and feedback control as shown in Fig. 4-1. Traditional PLL and feedback control of grid-tied inverter are formulated also in *d-q* frame. Recently, other synchronization and feedback control strategies are also developed, such as power synchronization [86], controller in stationary frame and even control grid-tied inverter as synchronous generator [87]. These topics are out of the scope of this disseration.

Using the proposed model, inverter small-signal impedances are characterized with different control strategies. Impedance value are shown in the form of Bode plots which clearly demonstrate the negative incremental resistor behavior of the impedance in *q* channel. Analytical expression for the negative resistance is given. The model shows that higher PLL bandwidth will produce a wider frequency range of negative resistor, and higher power rating of inverter will result lower magnitude of the negative resistor. The model is verified by measured impedance.

4.2 Power Stage Small-Signal Model

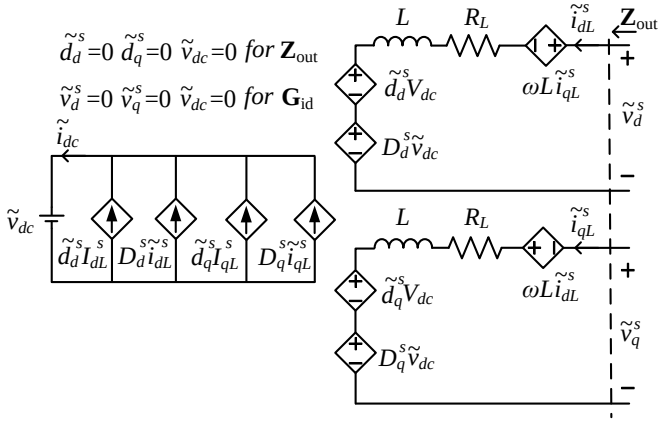


Fig. 4-2. Small-signal circuit model of grid-tied inverter in system *d-q* frame.

Fig. 4-2 shows the small-signal circuit model of the grid-tied inverter power stage in the system *d-q* frame [41], [39]. Assume the input of the grid-tied inverter is supplied by a stiff dc source which could be a dc-dc converter for solar application or ac-dc converter for wind

application. Then, the dynamic from dc input can be neglected. The small-signal circuit model then can be represented by the transfer function matrix flow chart shown in Fig. 4-3. $\mathbf{G}_{\mathbf{id}}$ is the transfer function matrix from duty ratio vector $\tilde{\vec{d}}^{s}$ to inductor current vector $\tilde{\vec{i}}_{L}^{s}$, $\mathbf{Z}_{\mathbf{out}}$ is the output impedance of power stage.

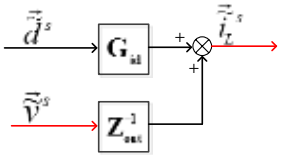


Fig. 4-3. Power stage small-signal model.

The output impedance can be derived by forcing perturbations of the duty ratio and dc voltage to zero as shown in Fig. 4-3. The expression of power stage output impedance is:

$$\mathbf{Z}_{\mathbf{out}} = \begin{bmatrix} Z_{dd} & Z_{dq} \\ Z_{qd} & Z_{qq} \end{bmatrix} = \begin{bmatrix} Ls + R_L & -\omega L \\ \omega L & Ls + R_L \end{bmatrix} \tag{4-1}$$

Notice that, impedance of three-phase converter in *d*-*q* frame is a 2-by-2 matrix. Z_{dd} represents the voltage response in *d* channel when *d* channel current is perturbed. Z_{qq} represents the *q* channel voltage response when *q* channel current is perturbed. Eq. (4-1) shows that Z_{dd} and Z_{qq} are the same as the impedance of inverter ac inductor. Z_{dq} and Z_{qd} represent the coupling effect between *d* and *q* channel.

Transfer function matrix between duty ratio vector and inductor current vector can be derived by forcing perturbations of grid and dc voltage to zero as shown in Fig. 3-2. The expression of $\mathbf{G}_{\mathbf{id}}$ is:

$$\mathbf{G}_{\mathbf{id}} = \frac{-V_{dc}}{(Ls + R_L)^2 + (\omega L)^2} \begin{bmatrix} Ls + R_L & \omega L \\ -\omega L & Ls + R_L \end{bmatrix} \tag{4-2}$$

4.3 Influence of PLL

Output impedance of dc-dc converter is influenced by its power stage parameters and feedback controller [29]. Different from dc-dc converter, grid-tied converter usually needs PLL to synchronize with the grid [64]. Because of PLL, the inverter system has two *d-q* frames, one is system *d-q* frame, and another is the controller *d-q* frame [66] as shown in Fig. 4-4. Grid voltage defines the system *d-q* frame. Controller *d-q* frame is defined by the PLL, which estimates the frequency and angle of grid voltage to find the position of system *d-q* frame. In steady state, controller *d-q* frame is aligned with the system *d-q* frame. When small-signal perturbations are added to the grid voltage, the position of system *d-q* frame is changed. The controller *d-q* frame is no longer aligned with system *d-q* frame because of the PLL dynamics (PI regulator of PLL). The angle between two *d-q* frames is $\Delta\theta$ as shown in Fig. 4-4. Voltage and current vectors in system *d-q* frame are rotated to controller *d-q* frame for feedback control by matrix $\mathbf{T}_{\Delta\theta}$. The duty cycle commands generated by feedback control are then rotated to system *d-q* frame by the inverse of matrix $\mathbf{T}_{\Delta\theta}$ to control the power semiconductors.

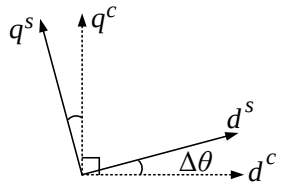


Fig. 4-4. System and controller d-q frames.

$$\mathbf{T}_{\Delta\theta} = \begin{bmatrix} \cos(\Delta\theta) & \sin(\Delta\theta) \\ -\sin(\Delta\theta) & \cos(\Delta\theta) \end{bmatrix} \tag{4-3}$$

$$\vec{v}^{\,c} = \mathbf{T}_{\Delta\theta}\vec{v}^{\,s},\ \vec{i}^{\,c} = \mathbf{T}_{\Delta\theta}\vec{i}^{\,s}, \vec{d}^{\,s} = \mathbf{T}_{\Delta\theta}^{-1}\vec{d}^{\,c} \tag{4-4}$$

Small-signal perturbations of the system voltage propagate to the PLL output angle, and further to the current and duty ratio vector in controller *d-q* frame. Perturbations then go to the voltage generated by the inverter power stage and finally to the output current of the inverter [81]. This means PLL dynamic influences the output impedance of grid-tied inverter.

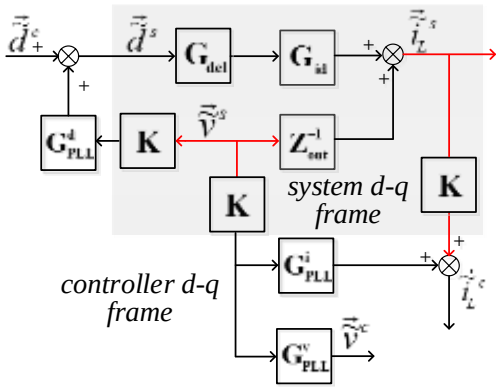


Fig. 4-5. Small-signal model with PLL.

In order to model the small-signal propagation path through PLL, transfer function matrices $\mathbf{G}^{\mathrm{v}}_{\mathrm{PLL}}$, $\mathbf{G}^{\mathrm{d}}_{\mathrm{PLL}}$ and $\mathbf{G}^{\mathrm{i}}_{\mathrm{PLL}}$ are defined. $\mathbf{G}^{\mathrm{v}}_{\mathrm{PLL}}$ models the small-signal perturbation path from system voltage to voltage in controller *d-q* frame. $\mathbf{G}^{\mathrm{d}}_{\mathrm{PLL}}$ models the small-signal perturbation path from system voltage to duty cycle in controller *d-q* frame. $\mathbf{G}^{\mathrm{i}}_{\mathrm{PLL}}$ models the small-signal perturbation path from system voltage to current in controller *d-q* frame. Fig. 4-5 shows the transfer function matrix flow chart representation of grid-tied inverter small-signal model with PLL. $\mathbf{K}$ is the filter transfer function matrix for voltage and current signals conditioning. $\mathbf{G}_{\mathrm{del}}$ represents the time delay (T_{del}) due to digital control and PWM [88]. Notice that, in the model shown in Fig. 4-5, adding $\mathbf{G}^{\mathrm{d}}_{\mathrm{PLL}}$ is the major difference to the model shown in Ref. [66].

To derive $\mathbf{G}^{\mathrm{v}}_{\mathrm{PLL}}$, $\mathbf{G}^{\mathrm{d}}_{\mathrm{PLL}}$, and $\mathbf{G}^{\mathrm{i}}_{\mathrm{PLL}}$, the PLL strategy in the synchronous reference (*d-q*) frame (SRF) [63] shown in Chapter 2.

$$\vec{V}^c = \vec{V}^s,\ \vec{I}^c = \vec{I}^s, \vec{D}^s = \vec{D}^c \tag{4-5}$$

Eq. (4-5) indicates that the angle between vectors in controller frame and the vector in system frame is 0, using the rotation matrix $\mathbf{T}_{\Delta\theta}$, Eq. (4-5) can be rewritten as:

$$\vec{V}^c = \begin{bmatrix} \cos(0) & \sin(0) \\ -\sin(0) & \cos(0) \end{bmatrix} \vec{V}^s,\ \vec{I}^c = \begin{bmatrix} \cos(0) & \sin(0) \\ -\sin(0) & \cos(0) \end{bmatrix} \vec{I}^s,$$
$$\vec{D}^s = \begin{bmatrix} \cos(0) & -\sin(0) \\ \sin(0) & \cos(0) \end{bmatrix} \vec{D}^c \tag{4-6}$$

Add small-signal perturbation to Eq. (4-6):

$$\begin{bmatrix} V_d^c + \tilde{v}_d^c \\ V_q^c + \tilde{v}_q^c \end{bmatrix} = \begin{bmatrix} \cos(0 + \Delta\tilde{\theta}) & \sin(0 + \Delta\tilde{\theta}) \\ -\sin(0 + \Delta\tilde{\theta}) & \cos(0 + \Delta\tilde{\theta}) \end{bmatrix} \begin{bmatrix} V_d^s + \tilde{v}_d^s \\ V_q^s + \tilde{v}_q^s \end{bmatrix} \tag{4-7}$$

By doing approximation of trigonometric functions, and canceling the steady state values, relationship between voltage vectors in controller frame, system frame and PLL output angle can be derived as:

$$\begin{bmatrix} V_d^c + \tilde{v}_d^c \\ V_q^c + \tilde{v}_q^c \end{bmatrix} \approx \begin{bmatrix} 1 & \Delta\tilde{\theta} \\ -\Delta\tilde{\theta} & 1 \end{bmatrix} \cdot \begin{bmatrix} V_d^s + \tilde{v}_d^s \\ V_q^s + \tilde{v}_q^s \end{bmatrix} \tag{4-8}$$

$$\begin{bmatrix} \tilde{v}_d^c \\ \tilde{v}_q^c \end{bmatrix} \approx \begin{bmatrix} \tilde{v}_d^s + V_q^s \Delta\tilde{\theta} \\ -V_d^s \Delta\tilde{\theta} + \tilde{v}_q^s \end{bmatrix} \tag{4-9}$$

Recall that PLL output angle is:

$$\Delta\tilde{\theta} = \tilde{v}_q^c \cdot tf_{PLL} \cdot \frac{1}{s} \tag{4-10}$$

Where,

$$tf_{PLL} = k_{ppll} + k_{ipll} \frac{1}{s} \tag{4-11}$$

Substitute Eq. (4-10) to (4-9), Eq. (4-12) shows the equation represent the relation between PLL output angle and *q* channel voltage.

$$\Delta\tilde{\theta} = \frac{tf_{PLL}}{s + V_d^s tf_{PLL}} \tilde{v}_q^s \tag{4-12}$$

Define G_{PLL} as:

$$G_{PLL} = \frac{tf_{PLL}}{s + V_d^s tf_{PLL}} \tag{4-13}$$

Then,

$$\Delta\tilde{\theta} = G_{PLL}\tilde{v}_q^s \tag{4-14}$$

For voltage,

$$\begin{bmatrix} \tilde{v}_d^c \\ \tilde{v}_q^c \end{bmatrix} \approx \begin{bmatrix} \tilde{v}_d^s + V_q^s G_{PLL}\tilde{v}_q^s \\ -V_d^s G_{PLL}\tilde{v}_q^s + \tilde{v}_q^s \end{bmatrix} = \begin{bmatrix} 1 & V_q^s G_{PLL} \\ 0 & 1 - V_d^s G_{PLL} \end{bmatrix} \cdot \begin{bmatrix} \tilde{v}_d^s \\ \tilde{v}_q^s \end{bmatrix} \tag{4-15}$$

Then, $\mathbf{G_{PLL}^v}$ is defined as:

$$\mathbf{G_{PLL}^v} = \begin{bmatrix} 1 & V_q^s G_{PLL} \\ 0 & 1 - V_d^s G_{PLL} \end{bmatrix} \tag{4-16}$$

For duty ratio, similar small-single analysis can be done which yields:

$$\begin{bmatrix} \tilde{d}_d^s \\ \tilde{d}_q^s \end{bmatrix} \approx \begin{bmatrix} 0 & -D_q^s G_{PLL} \\ 0 & D_d^s G_{PLL} \end{bmatrix} \cdot \begin{bmatrix} \tilde{v}_d^s \\ \tilde{v}_q^s \end{bmatrix} + \begin{bmatrix} \tilde{d}_d^c \\ \tilde{d}_q^c \end{bmatrix} \tag{4-17}$$

Then, $\mathbf{G_{PLL}^d}$ is defined as:

$$\mathbf{G_{PLL}^d} = \begin{bmatrix} 0 & -D_q^s G_{PLL} \\ 0 & D_d^s G_{PLL} \end{bmatrix} \tag{4-18}$$

Similar equation can be derived for inductor current as shown in (4-19):

$$\begin{bmatrix} \tilde{i}_d^c \\ \tilde{i}_q^c \end{bmatrix} \approx \begin{bmatrix} 0 & I_q^s G_{PLL} \\ 0 & -I_d^s G_{PLL} \end{bmatrix} \cdot \begin{bmatrix} \tilde{v}_d^s \\ \tilde{v}_q^s \end{bmatrix} + \begin{bmatrix} \tilde{i}_d^s \\ \tilde{i}_q^s \end{bmatrix} \tag{4-19}$$

$\mathbf{G_{PLL}^i}$ is defined as:

$$\mathbf{G}_{\mathbf{PLL}}^{\mathbf{i}} = \begin{bmatrix} 0 & I_q^s G_{PLL} \\ 0 & -I_d^s G_{PLL} \end{bmatrix} \tag{4-20}$$

Solving the equations represented by Fig. 4-5, the output impedance of inverter with PLL working on open loop is:

$$\mathbf{Z}_{\mathbf{out\_ol\_PLL}} = \left(\mathbf{Z}_{\mathbf{out}}^{-1} + \mathbf{G}_{\mathbf{id}}\mathbf{G}_{\mathbf{del}}\mathbf{G}_{\mathbf{PLL}}^{\mathbf{d}}\mathbf{K}\right)^{-1} \tag{4-21}$$

With DDSRF, the relation between PLL output angle and grid voltage is:

$$\Delta\tilde{\theta} = G_{PLL1}\tilde{v}_d^s + G_{PLL2}\tilde{v}_q^s \tag{4-22}$$

Where,

$$G_{PLL1} = \frac{tf_{PLL}H_{21}}{s + tf_{PLL}\left(V_d^s H_{22} - V_q^s H_{21}\right)} \tag{4-23}$$

$$G_{PLL2} = \frac{tf_{PLL}H_{22}}{s + tf_{PLL}\left(V_d^s H_{22} - V_q^s H_{21}\right)} \tag{4-24}$$

Then $\mathbf{G}_{\mathbf{PLL}}^{\mathbf{v}}$, $\mathbf{G}_{\mathbf{PLL}}^{\mathbf{d}}$, and $\mathbf{G}_{\mathbf{PLL}}^{\mathbf{i}}$ become $\mathbf{G}_{\mathbf{DDPLL}}^{\mathbf{v}}$, $\mathbf{G}_{\mathbf{DDPLL}}^{\mathbf{d}}$, and $\mathbf{G}_{\mathbf{DDPLL}}^{\mathbf{i}}$ with DDSRF PLL, and they are:

$$\mathbf{G}_{\mathbf{DDPLL}}^{\mathbf{v}} = \begin{bmatrix} 1+V_q^s G_{PLL1} & V_q^s G_{PLL2} \\ -V_d^s G_{PLL1} & 1-V_d^s G_{PLL2} \end{bmatrix} \tag{4-25}$$

$$\mathbf{G}_{\mathbf{DDPLL}}^{\mathbf{d}} = \begin{bmatrix} -D_q^s G_{PLL1} & -D_q^s G_{PLL2} \\ D_d^s G_{PLL1} & D_d^s G_{PLL2} \end{bmatrix} \tag{4-26}$$

$$\mathbf{G}_{\mathbf{DDPLL}}^{\mathbf{i}} = \begin{bmatrix} I_q^s G_{PLL1} & I_q^s G_{PLL2} \\ -I_d^s G_{PLL1} & -I_d^s G_{PLL2} \end{bmatrix} \tag{4-27}$$

When DDSRF PLL is used, $\mathbf{G}_{\mathbf{PLL}}^{\mathbf{d}}$ is replaced by $\mathbf{G}_{\mathbf{DDPLL}}^{\mathbf{d}}$ in Eq. (4-21).

4.4 Impedance with Current Control and PLL

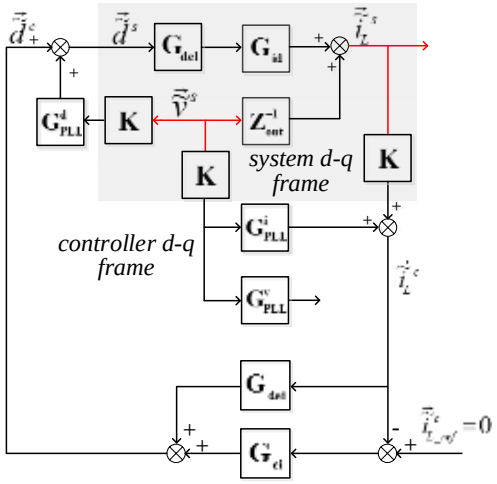


Fig. 4-6. Small-signal model with PLL and current feedback control.

Current controller can be implemented in either synchronous frame or stationary frame. Stationary frame current regulators can be transformed to synchronous frame using the transformation provided by [91]. Modeling of the impedance of voltage source converter with stationary frame current regulator is shown in [92]. Influence of different current regulators will not be elaborated, only current controller in synchronous frame is considered in this paper. Fig. 4-6 shows the small-signal model of grid-tied inverter with current feedback control. The current controller matrix is $\mathbf{G_{ci}}$. $\mathbf{G_{dei}}$ is the decoupling term.

$$\mathbf{G_{ci}} = \begin{bmatrix} k_{pi} + \dfrac{k_{ii}}{s} & 0 \\ 0 & k_{pi} + \dfrac{k_{ii}}{s} \end{bmatrix} \tag{4-28}$$

$$\mathbf{G_{dei}} = \begin{bmatrix} 0 & -\dfrac{3\omega L_{ac}}{V_{dc}} \\ \dfrac{3\omega L_{ac}}{V_{dc}} & 0 \end{bmatrix} \tag{4-29}$$

Solving the equations represented by Fig. 4-6, the output impedance of grid-tied inverter system with PLL working under closed-loop condition is:

$$\mathbf{Z}_{\mathbf{out\_il\_PLL}} = \left(\mathbf{Z}_{\mathbf{out}}^{-1} + \mathbf{G}_{\mathbf{id}}\mathbf{G}_{\mathbf{del}}\left(\left(-\mathbf{G}_{\mathbf{ci}} + \mathbf{G}_{\mathbf{dei}}\right)\mathbf{G}_{\mathbf{PLL}}^{\mathbf{i}} + \mathbf{G}_{\mathbf{PLL}}^{\mathbf{d}}\right)\mathbf{K}\right)^{-1} \cdot \left(\mathbf{I} + \mathbf{G}_{\mathbf{id}}\mathbf{G}_{\mathbf{del}}\left(\mathbf{G}_{\mathbf{ci}} - \mathbf{G}_{\mathbf{dei}}\right)\mathbf{K}\right) \tag{4-30}$$

When DDSRF PLL is used, $\mathbf{G}_{\mathbf{PLL}}^{\mathbf{d}}$ is replaced by $\mathbf{G}_{\mathbf{DDPLL}}^{\mathbf{d}}$ and $\mathbf{G}_{\mathbf{PLL}}^{\mathbf{i}}$ is replaced by $\mathbf{G}_{\mathbf{DDPLL}}^{\mathbf{i}}$ in Eq. (4-30).

Table 4-1. Parameters of Grid-Tied Inverter Prototype

Symbol	Description	Value
V_{dc}	Inverter input dc voltage	270 V
V^s_d	D channel grid voltage	99.6 V
V^s_q	Q channel grid voltage	0 V
i_{dref}	D channel current reference	-11 A
i_{qref}	Q channel current reference	0 A
ω	Line frequency	$2\pi\times400$ Hz
L	Inductance of inverter output inductor	970 μH
R_L	Resistance of inverter output inductor self-resistor	120 mΩ
f_{sw}	Switching frequency	20 kHz
k_{pi}	Proportional gain of current controller	0.023
k_{ii}	Integrator gain of current controller	25.59
ω_n	Natural frequency of signal conditioning filter	1.23e6 rad/s
ζ	Damping factor of signal conditioning filter	4.74e-13
T_{del}	Time delay due to digital control and PWM	$1.5/f_{sw}$
ω_f	Cut off frequency of LPF in DDSRF PLL	1777 rad/s
k_{ppll}	Proportional gain of inverter PLL	
k_{ipll}	Integral gain of inverter PLL	

Table 4-1 in shows the parameters of inverter prototype system. Using these parameters and Eq. (4-30), Fig. 4-7 shows the Bode plot of inverter output impedances with current feedback

control and different PLL designs. The impedances are calculated up to half switching frequency where it is valid.

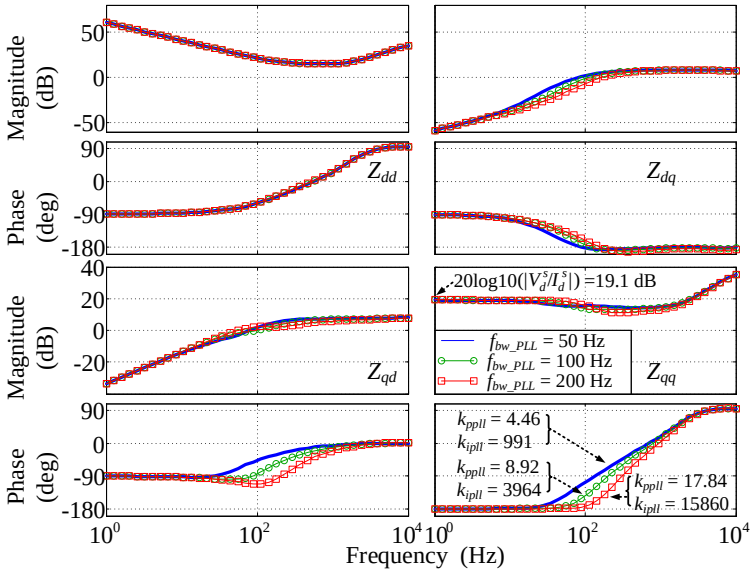


Fig. 4-7. Impedance with current control and different PLL bandwidth.

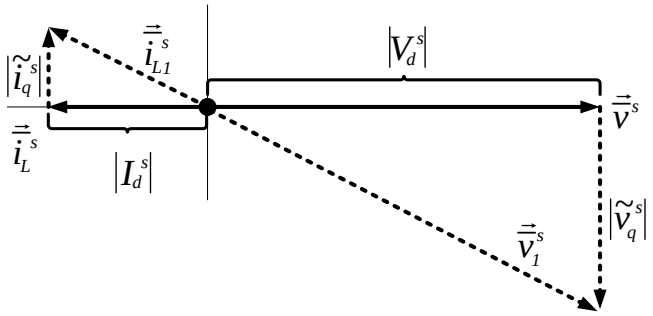


Fig. 4-8. Phasor diagram interpretation of negative resistor behavior of Z_{qq}.

$$Z_{qq} = -\frac{|\tilde{v}_q^s|}{|\tilde{i}_q^s|} = -\frac{|V_d^s|}{|I_d^s|} \tag{4-31}$$

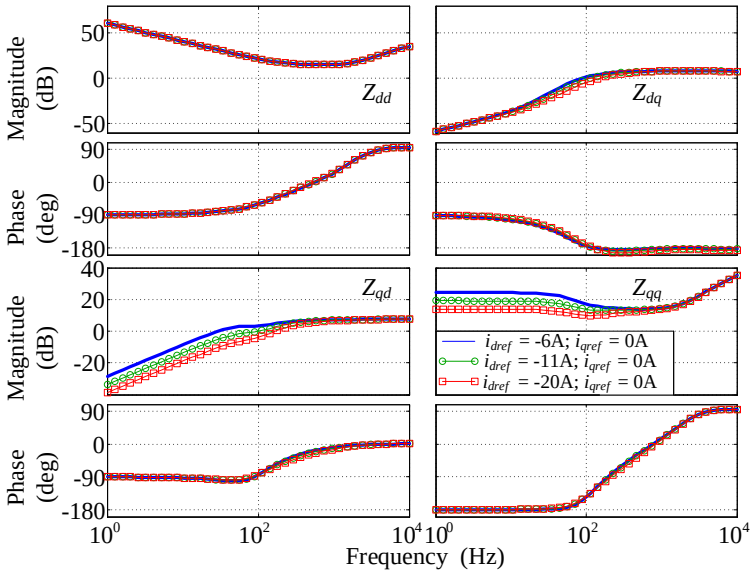


Fig. 4-9. Impedance with current control and different current ratings.

As it can be observed in Fig. 4-7, Z_{dd} shows the current source behavior. In low frequency range, it is shaped by current controller integrator; in high frequency range, Z_{dd} is the impedance of ac inductor. Z_{dq} and Z_{qd} are very small within current controller bandwidth, because of unity power factor control. In high frequency range, they behave as the power stage impedance value as shown in Eq. (4-1). Z_{qq} behaves as negative incremental resistance within PLL bandwidth. Three different PLL designs which bandwidth (f_{bw_PLL}) varies from 50 Hz to 200 Hz (line frequency is set to be 400 Hz in order to allow a wide range of PLL bandwidth) are chosen to show the influence of PLL. The results shows that higher PLL bandwidth case yields wider frequency range of negative resistance behavior. The magnitude of the resistance related to power rating of the inverter. Especially, as shown in Fig. 4-8, current vector of the inverter is synchronized with grid voltage vector which is aligned in *d* channel to inject real power to the grid. When voltage disturbance happens in *q* channel, the voltage vector $\vec{\bar{v}}^{s}$ becomes $\vec{\bar{v}}_1^{s}$. Because of PLL, current vector will rotate to keep the synchronization with voltage vector. Meanwhile, current controller keeps current magnitude in *d* channel unchanged. Then, current vector $\vec{\bar{i}}_L^{s}$ becomes $\vec{\bar{i}}_{L1}^{s}$ due to the *q* channel voltage perturbation. Notice that small-signal response of *q* channel current is in the opposite direction of *q* channel voltage perturbation, so, from Fig. 4-8,

Z_{qq} can be calculated by Eq. (4-31) within the bandwidth of PLL. This conclusion is also verified by the magnitude of Z_{qq} in low frequency shown in Fig. 4-7. According to Eq. (4-31), inverter with high current rating has low impedance in *q*-*q* channel, this is shown by Fig. 4-9 in which impedances with three different *d* channel current references are plotted.

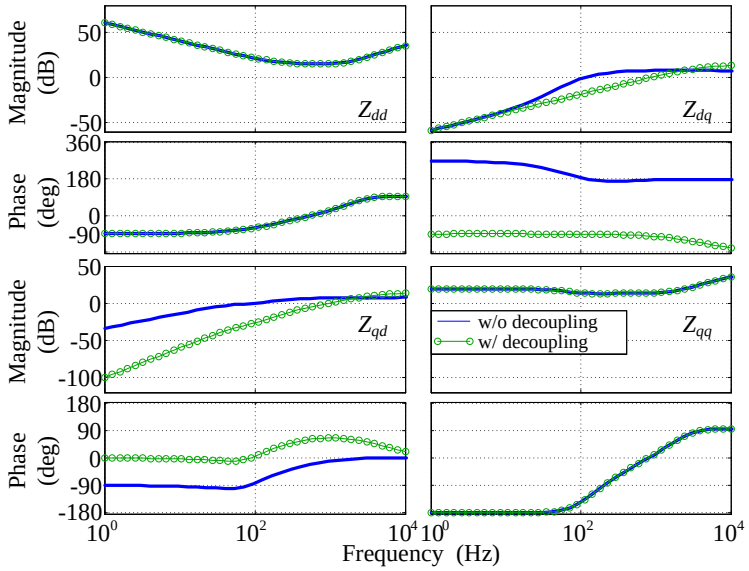


Fig. 4-10. Impedance with and without decoupling control.

Fig. 4-10 shows the impedances of inverter with and without decoupling control. With decoupling control, Z_{dq} and Z_{qd} are reduced. This is expected, because decoupling control reduces the coupling between *d* and *q* channel which is reflected by Z_{dq} and Z_{qd}. Using of decoupling control does not change the negative resistance behavior of Z_{qq}.

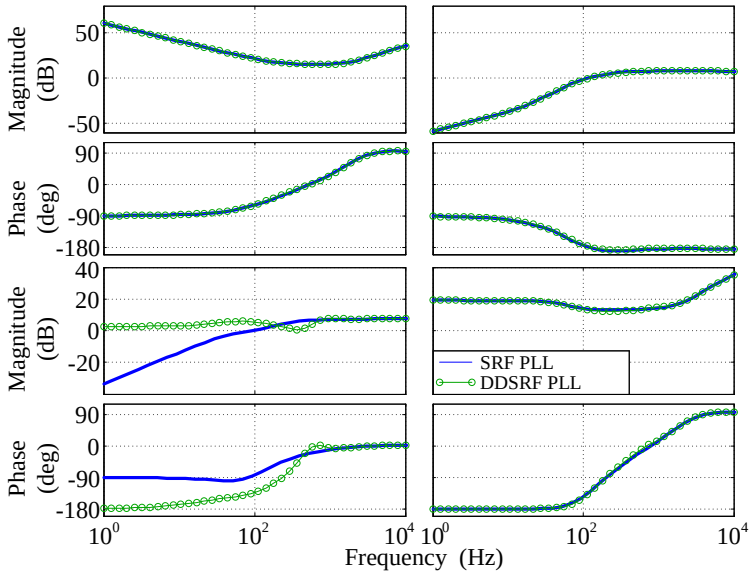


Fig. 4-11. Impedance with current control and different PLL strategies.

Fig. 4-11 shows the impedance with different PLL strategies which indicates that using of DDSRF PLL does not change the negative resistance behavior of Z_{qq}.

Grid-tied inverter can inject reactive current to support the grid. Fig. 4-12 shows the impedance of grid-tied inverter with different reactive power injections. Blue line shows the impedance of capacitive power injection case; the green line shows the impedance of no reactive power injection, and the red line shows the inductive power injection case. Notice that reactive power injection will increase the impedance of cross coupling term Z_{dq}, the rest impedances are the same with unit power factor case. The negative resistance feature remains unchanged when grid-tied inverter injects reactive power to the grid.

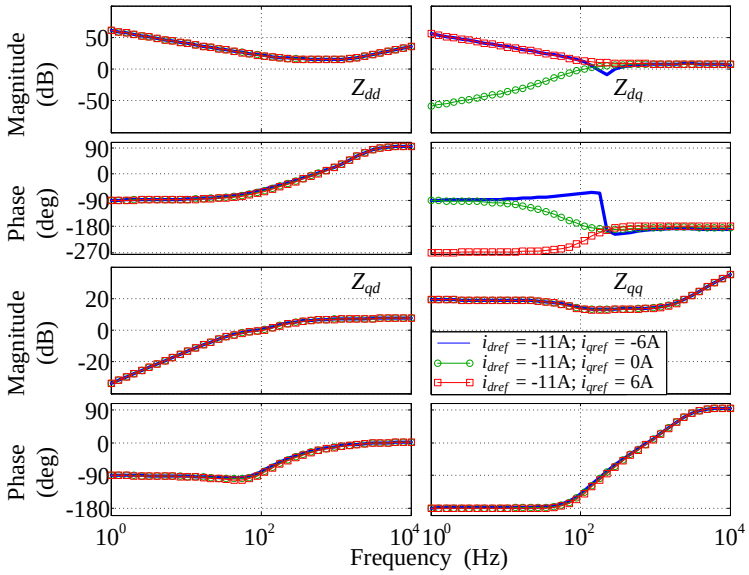


Fig. 4-12. Impedance with different reactive current injections.

4.5 Influence of Power Flow Control Loop

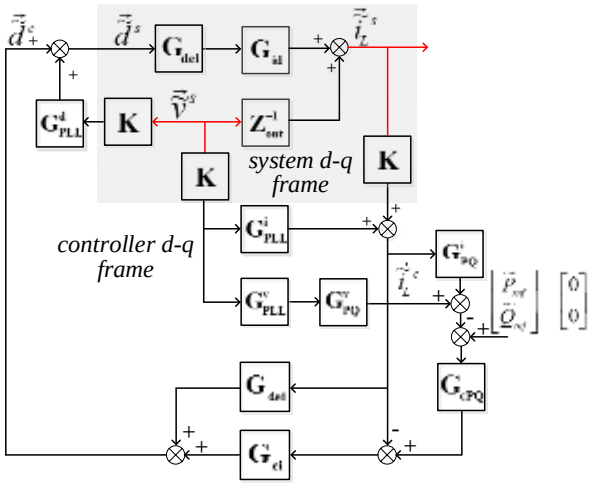


Fig. 4-13. Small-signal model with PLL, current and power feedback control.

On top of current controller, power flow controller can be added to control the real and reactive power generated by inverter accurately. The small-signal model is shown in Fig. 4-13 for power flow control case. $\mathbf{G}_{cPQ}$ is the transfer function matrix of power flow controller:

$$\mathbf{G}_{\mathbf{cPQ}} = \begin{bmatrix} k_{pPQ} + \dfrac{k_{iPQ}}{s} & 0 \\ 0 & k_{pPQ} + \dfrac{k_{iPQ}}{s} \end{bmatrix} \tag{4-32}$$

$\mathbf{G}^{\mathbf{i}}_{\mathbf{PQ}}$ and $\mathbf{G}^{\mathbf{v}}_{\mathbf{PQ}}$ are small-signal transfer function matrices of power calculation in *d-q* frame:

$$\begin{cases} P = i_d^c v_d^c + i_q^c v_q^c \\ Q = -i_d^c v_q^c + i_q^c v_d^c \end{cases} \tag{4-33}$$

By doing linearization to Eq. (4-33), $\mathbf{G}^{\mathbf{i}}_{\mathbf{PQ}}$ and $\mathbf{G}^{\mathbf{v}}_{\mathbf{PQ}}$ are derived:

$$\mathbf{G}^{\mathbf{i}}_{\mathbf{PQ}} = \begin{bmatrix} V_d^s & V_q^s \\ -V_q^s & V_d^s \end{bmatrix} \tag{4-34}$$

$$\mathbf{G}^{\mathbf{v}}_{\mathbf{PQ}} = \begin{bmatrix} I_d^s & I_q^s \\ I_q^s & -I_d^s \end{bmatrix} \tag{4-35}$$

Solving the equations represented by Fig. 4-13, the output impedance of grid-tied inverter system with PLL and power feedback control is:

$$\begin{aligned} &\mathbf{Z}_{\mathbf{out\_PQ\_il\_PLL}} = \\ &\left(\mathbf{Z}_{\mathbf{out}}^{-1} + \mathbf{G}_{\mathbf{id}}\mathbf{G}_{\mathbf{del}}\left(\left(-\mathbf{G}_{\mathbf{ci}}\mathbf{G}_{\mathbf{cPQ}}\mathbf{G}^{\mathbf{i}}_{\mathbf{PQ}} - \mathbf{G}_{\mathbf{ci}} + \mathbf{G}_{\mathbf{dei}}\right)\mathbf{G}^{\mathbf{i}}_{\mathbf{PLL}} + \mathbf{G}^{\mathbf{d}}_{\mathbf{PLL}} - \mathbf{G}_{\mathbf{ci}}\mathbf{G}_{\mathbf{cPQ}}\mathbf{G}^{\mathbf{v}}_{\mathbf{PQ}}\mathbf{G}^{\mathbf{v}}_{\mathbf{PLL}}\right)\mathbf{K}\right)^{-1} \cdot \\ &\left(\mathbf{I} + \mathbf{G}_{\mathbf{id}}\mathbf{G}_{\mathbf{del}}\left(\mathbf{G}_{\mathbf{ci}}\mathbf{G}_{\mathbf{cPQ}}\mathbf{G}^{\mathbf{i}}_{\mathbf{PQ}} + \mathbf{G}_{\mathbf{ci}} - \mathbf{G}_{\mathbf{dei}}\right)\mathbf{K}\right) \end{aligned} \tag{4-36}$$

When DDSRF PLL is used, $\mathbf{G}^{\mathbf{d}}_{\mathbf{PLL}}$ is replaced by $\mathbf{G}^{\mathbf{d}}_{\mathbf{DDPLL}}$, $\mathbf{G}^{\mathbf{i}}_{\mathbf{PLL}}$ is replaced by $\mathbf{G}^{\mathbf{i}}_{\mathbf{DDPLL}}$, and $\mathbf{G}^{\mathbf{v}}_{\mathbf{PLL}}$ is replaced by $\mathbf{G}^{\mathbf{v}}_{\mathbf{DDPLL}}$ in Eq. (4-36).

Fig. 4-14 shows the impedance of inverter prototype with power feedback control using inverter power stage parameters list in Table 4-1 and the controller parameters list in Table 4-2. Notice that, integrator gain of current controller in Table 4-2 is increased comparing to what is shown in Table 4-1, in order to close the power feedback control loop. Once the power flow controller is applied, within its bandwidth, Z_{dd} becomes a positive resistance, and Z_{qq} is still a

negative resistance. PLL bandwidth still influences the frequency range of negative resistance behavior of Z_{qq} as shown in Fig. 4-14. Z_{dq} and Z_{qd} is still low in the low frequency because of the unity power factor control.

Table 4-2. Parameters of Current and Power Feedback Controller

Symbol	Description	Value
k_{pi}	Proportional gain of current controller	0.023
k_{ii}	Integrator gain of current controller	51.18
k_{pPQ}	Proportional gain of power controller	0.0028
k_{iPQ}	Integrator gain of power controller	7
P_{ref}	Real power reference	-1150 W
Q_{ref}	Reactive power reference	0 Var

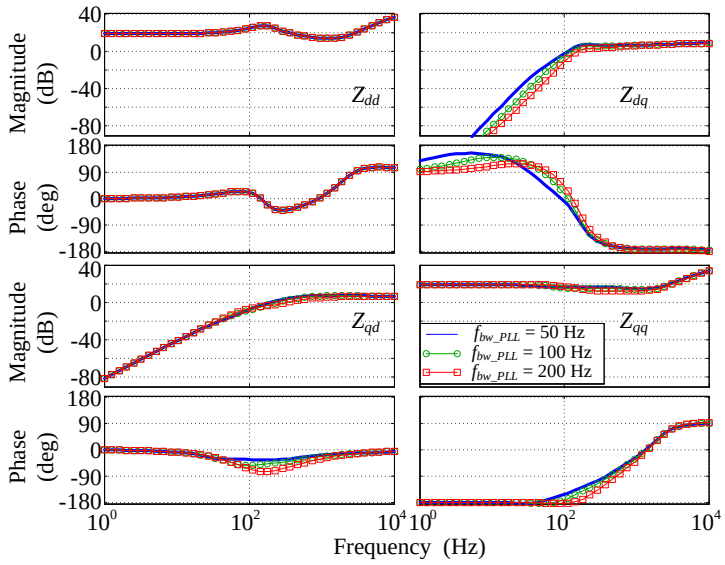


Fig. 4-14. Impedance with PLL and power feedback control.

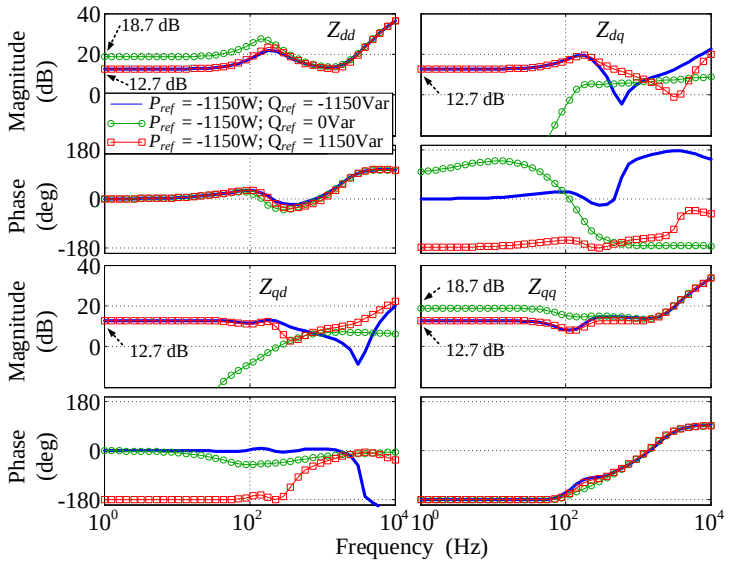


Fig. 4-15. Impedance with power feedback control and different reactive power injections.

When injecting reactive power into the grid, all four impedances changes along with real and reactive power rating as shown in Fig. 4-15. In order to understand the impedance matrix when power controller is applied, or, in another word, to understand the impedance feature of constant power source, the following derivation are shown [64]:

$$\begin{cases} P = i_d^s v_d^s + i_q^s v_q^s \\ Q = -i_d^s v_q^s + i_q^s v_d^s \end{cases} \tag{4-37}$$

Eq. (4-37) is a good approximation at the frequencies that are below the power regulation bandwidth where P and Q are constant. Then voltage vector can be derived as Eq. (4-38) from Eq. (4-37). It can be linearized using two-variable Taylor series up to the second term as shown in Eq. (4-39). Then, impedance matrix is shown in Eq. (4-40). Eq. (4-40) can be verified by comparing its results with the value shown in Fig. 4-15 for different reactive injection conditions.

$$\vec{v}_{dq}^{\,s} = \begin{bmatrix} \dfrac{i_d^s P + i_q^s Q}{\left(i_d^s\right)^2 + \left(i_q^s\right)^2} \\ \dfrac{-i_d^s Q + i_q^s P}{\left(i_d^s\right)^2 + \left(i_q^s\right)^2} \end{bmatrix} \tag{4-38}$$

$$\vec{v}_{dq}^{\,s} = \mathrm{F}\left(\vec{i}_{dq}^{\,s}\right) \approx \mathrm{F}\left(\vec{i}_{dq}^{\,s}\right)\Big|_{\vec{I}_{dq}^{\,s}} + \mathrm{OF}\left(\vec{i}_{dq}^{\,s}\right)\Big|_{\vec{I}_{dq}^{\,s}} \tilde{\vec{i}}_{dq}^{\,s} = \vec{V}_{dq}^{\,s} + \mathbf{Z_{dq}} \tilde{\vec{i}}_{dq}^{\,s} \tag{4-39}$$

$$\mathbf{Z_{dq}} = \begin{bmatrix} \dfrac{P}{\left(I_d^s\right)^2 + \left(I_q^s\right)^2} - \dfrac{2I_d^s\left(I_d^s P + I_q^s Q\right)}{\left(\left(I_d^s\right)^2 + \left(I_q^s\right)^2\right)^2} & \dfrac{Q}{\left(I_d^s\right)^2 + \left(I_q^s\right)^2} - \dfrac{2I_q^s\left(I_d^s P + I_q^s Q\right)}{\left(\left(I_d^s\right)^2 + \left(I_q^s\right)^2\right)^2} \\ -\dfrac{Q}{\left(I_d^s\right)^2 + \left(I_q^s\right)^2} - \dfrac{2I_d^s\left(I_q^s P - I_d^s Q\right)}{\left(\left(I_d^s\right)^2 + \left(I_q^s\right)^2\right)^2} & \dfrac{P}{\left(I_d^s\right)^2 + \left(I_q^s\right)^2} - \dfrac{2I_q^s\left(I_q^s P - I_d^s Q\right)}{\left(\left(I_d^s\right)^2 + \left(I_q^s\right)^2\right)^2} \end{bmatrix} \tag{4-40}$$

4.6 Influence of PLL on Input Impedance of AFE

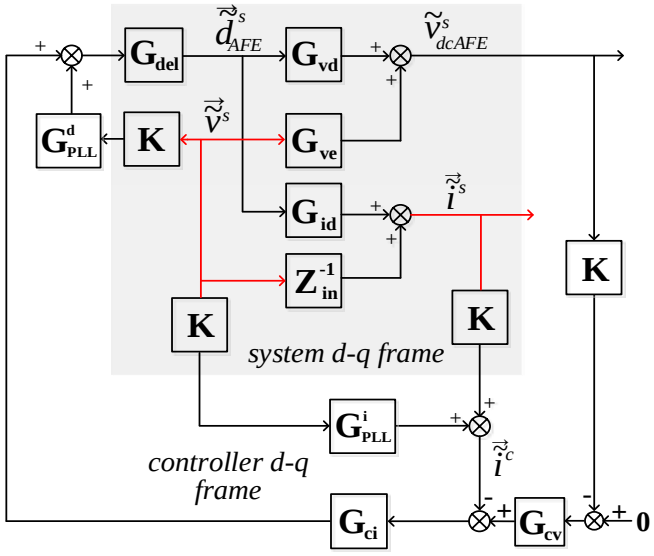


Fig. 4-16. Small-signal model of AFE.

Together with the feedback control system, the small-signal circuit model of AFE can be represented by the transfer function matrix flow chart shown in Fig. 4-16. $\mathbf{G_{vd}}$ is the transfer

function matrix from duty ratio vector $\tilde{\vec{d}}^{s}_{AFE}$ to output dc voltage $\tilde{v}^{s}_{dcAFE}$; $\mathbf{G_{ve}}$ is the transfer function matrix from PCC voltage vector $\tilde{\vec{v}}^{s}$ to output dc voltage $\tilde{v}^{s}_{dcAFE}$; $\mathbf{G_{id}}$ is the transfer function matrix from duty ratio vector $\tilde{\vec{d}}^{s}_{AFE}$ to inductor current vector $\tilde{\vec{i}}^{s}$, $\mathbf{Z_{in}}$ is the output impedance of power stage. $\mathbf{G^{d}_{PLL}}$ is the transfer function matrix from system voltage $\tilde{\vec{v}}^{s}$ to system *d-q* frame duty ratio vector $\tilde{\vec{d}}^{s}_{AFE}$; $\mathbf{G^{i}_{PLL}}$ is the transfer function matrix from system voltage $\tilde{\vec{v}}^{s}$ to controller *d-q* frame current vector $\tilde{\vec{i}}^{c}$. From Fig. 4-16, Eq. (4-45) can be derived to calculate the input impedance of AFE with feedback control.

$$\mathbf{G^{d}_{PLL}} = \begin{bmatrix} 0 & -D^{s}_{qAFE}G_{PLL} \\ 0 & D^{s}_{dAFE}G_{PLL} \end{bmatrix} \tag{4-41}$$

$$\mathbf{G^{i}_{PLL}} = \begin{bmatrix} 0 & -I^{s}_{q}G_{PLL} \\ 0 & I^{s}_{d}G_{PLL} \end{bmatrix} \tag{4-42}$$

$$G_{PLL} = \frac{tf_{PLL}}{s + V^{s}_{d}tf_{PLL}} \tag{4-43}$$

$$tf_{PLL} = k_{ppllAFE} + k_{ipllAFE}/s \tag{4-44}$$

$$\mathbf{Z_{AFEdq}} = \left[\begin{matrix} \mathbf{Z_{in}^{-1}} + \mathbf{G_{id}}\left(\mathbf{I} + \mathbf{G_{del}G_{ci}G_{cv}KG_{vd}}\right)^{-1}\mathbf{G_{del}} \cdot \\ \left[-\mathbf{G_{ci}G^{i}_{PLL}K} - \mathbf{G_{ci}G_{cv}KG_{ve}} + \mathbf{G^{d}_{PLL}K}\right] \end{matrix}\right]^{-1} \cdot \left(\mathbf{I} + \mathbf{G_{id}}\left(\mathbf{I} + \mathbf{G_{del}G_{ci}G_{cv}KG_{vd}}\right)^{-1}\mathbf{G_{del}} \cdot \mathbf{G_{ci}K}\right) \tag{4-45}$$

Using the parameters in Table 5-1, input impedances of AFE are plotted in Fig. 4-17.

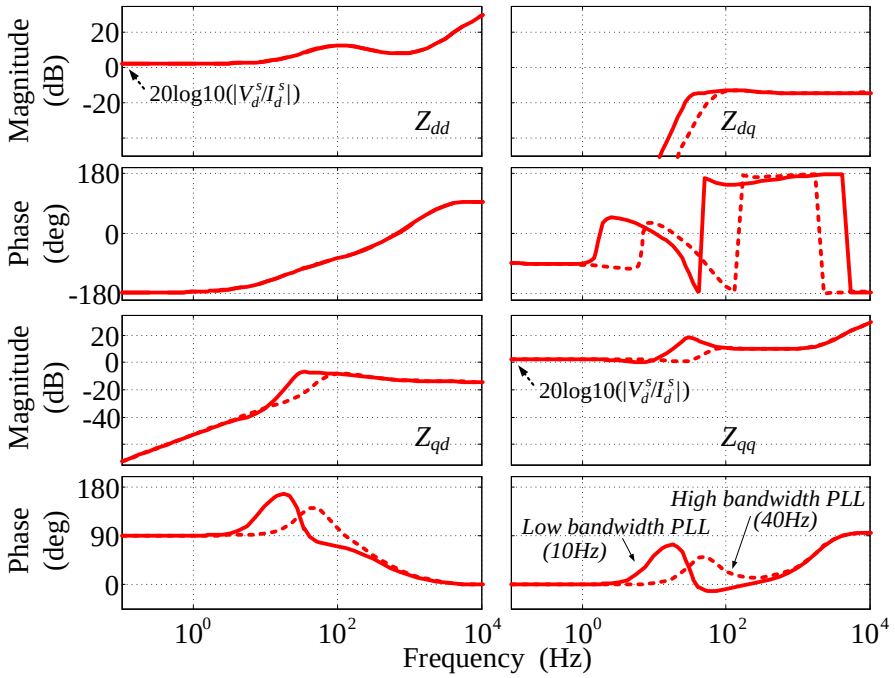


Fig. 4-17. AFE input impedance with different PLL bandwidth.

For Z_{qq}, it behaves as a positive incremental resistance due to PLL as shown in Fig. 4-17. The magnitude of the resistance related to power rating of the inverter. Especially, as shown in Fig. 4-18, current vector of the AFE is synchronized with PCC voltage vector that is aligned in *d* channel to get real power from the grid. When voltage disturbance happens in *q* channel, the voltage vector $\vec{\bar{v}}^s$ becomes $\vec{\bar{v}}_1^s$. Because of PLL, current vector will rotate to keep the synchronization with PCC voltage. Meanwhile, current controller keeps current magnitude in *d* channel unchanged. Then, current vector $\vec{\bar{i}}^s$ becomes $\vec{\bar{i}}_1^s$ due to the *q* channel voltage perturbation. Notice that small-signal response of *q* channel current is in the same direction of *q* channel voltage perturbation, so, from Fig. 4-18, Z_{qq} can be calculated by Eq. (4-46) within the bandwidth of PLL.

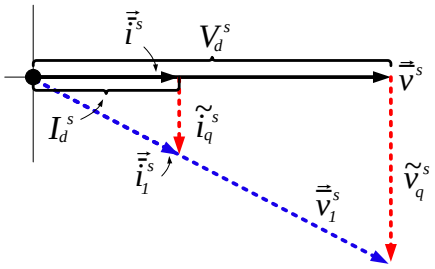


Fig. 4-18. Phasor diagram illustration of AFE $Z_{qq}(0)$.

$$Z_{qq}\Big|_{j\omega=0} = \frac{\tilde{v}_q^s}{\tilde{i}_q^s} = \frac{V_d^s}{I_d^s} \tag{4-46}$$

When working under unity power factor condition, Z_{dq} and Z_{qd} are kept small by d and q channel current controllers [39].

4.7 Stability Analysis using the Proposed Model

4.7.1 Grid-tied inverter system

Although this paper focus on impedance analysis of three-phase grid-tied inverter, this section gives a brief discussion of stability analysis using the proposed model. This example also shows that increasing PLL bandwidth could cause instability of the grid-tied inverter system under weak grid condition.

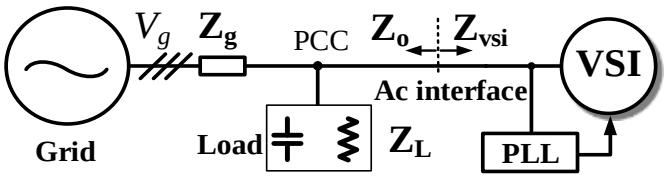


Fig. 4-19. One line diagram of three-phase grid-tied inverter system with local load.

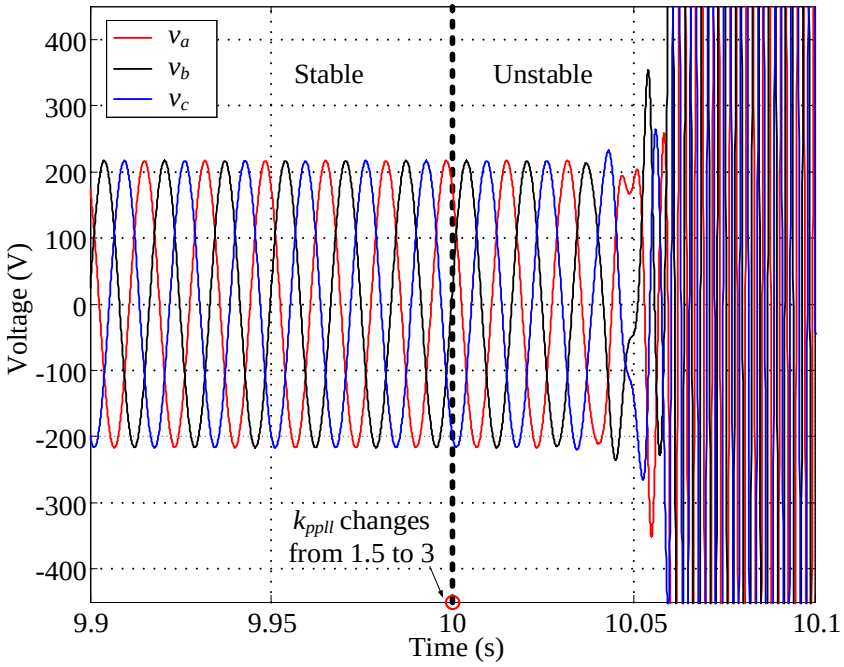
One line diagram representation of the inverter system under study is shown in Fig. 4-19. In this system, three-phase inverter is connected to the point of common coupling (PCC) together with three-phase passive load. This inverter is synchronized with PCC voltage by SRF PLL.

Only current feedback control is applied to control the amount of power injection to PCC. Each phase of the passive load consist of parallel connected resistor and capacitor. Grid is connected to PCC through impedance consist of inductor and resistor. The detailed parameter of this system is shown in Table 4-3.

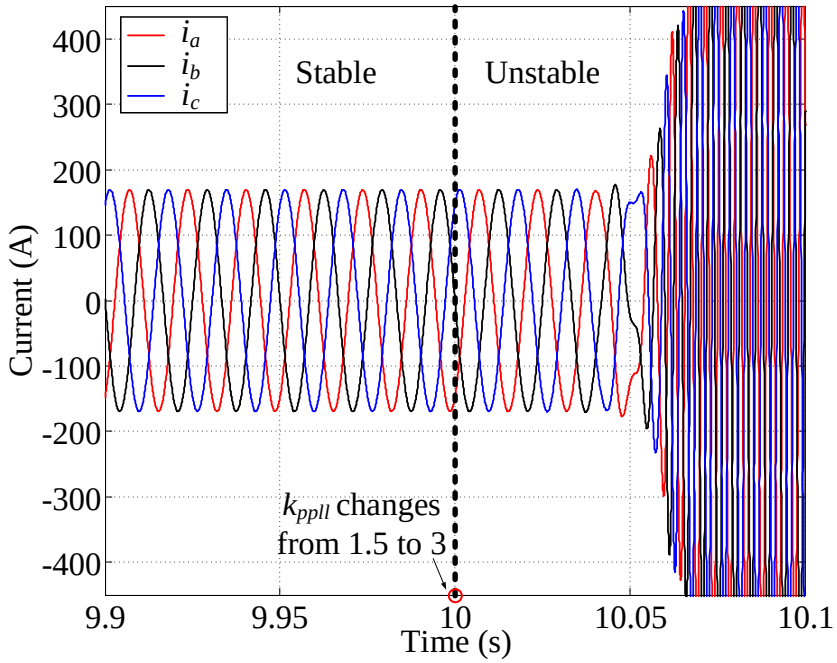
Table 4-3. Parameters of Inverter System for Stability Analysis

Symbol	Description	Value
V_g	Grid line-line peak voltage	$120\sqrt{6}$ V
ω_g	Grid voltage frequency	$2\pi\times60$ Hz
L	Inductance of inverter	1 mH
V_{dc}	Inverter dc voltage	600 V
f_{sw}	Switching frequency of inverter	20 kHz
I_{dref}	*d* channel current of inverter	-190 A
I_{qref}	*q* channel current of inverter	0 A
k_{pi}	Proportional gain of inverter current controller	0.0105
k_{ii}	Integrator gain of inverter current controller	1.1519
k_{ppll}	Proportional gain of inverter PLL	1.5 (stable); 3 (unstable)
k_{ipll}	Integral gain of inverter PLL	3.2
Z_L	Local passive load	R_{Load}: 10 Ω; C_{Load}: 250 μF
Z_g	Grid impedance	R_g: 0.2 Ω; L_g: 2 mH
f_{pll}	PLL output frequency of inverter	

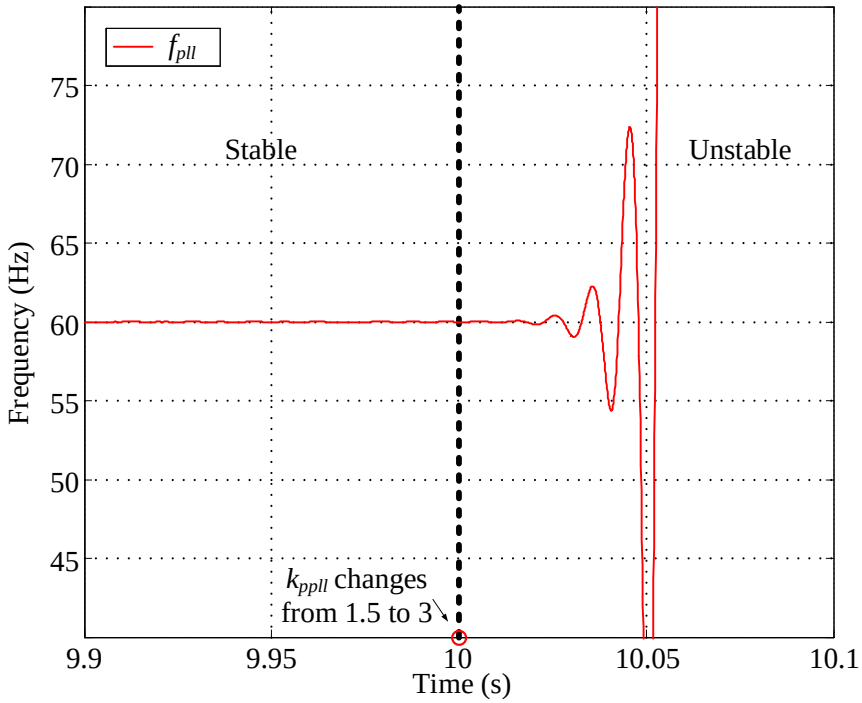
Fig. 4-20 shows the time domain simulation results of the inverter system. In the simulation, within the time range from 0 to 10 second, the system is running under stable condition. At 10 second, proportional gain (k_{ppll}) of PLL PI regulator is increased from 1.5 to 3, both PCC voltage as shown in part (a) of Fig. 4-20 and PLL output frequency of VSI as shown in part (b) of Fig. 4-20 start to oscillate. The whole system becomes unstable.



(a)



(b)



(b)

Fig. 4-20. (a) PCC voltages; (b) output current of VSI; (c) PLL output frequency of VSI.

In order to predict stable and unstable condition of the system using impedance-based method, an ac interface is found at the terminal of inverter as shown in Fig. 4-19. As reported by Ref. [79], when using impedance-based stability analysis for grid-tied inverter system, the inverter should be treated as load, Nyquist stability criterion should be applied to the impedance ratio between grid side impedance and inverter impedance as shown in Eq. (4-47).

$$\mathbf{L} = \mathbf{Z}_{\mathbf{o}} \cdot \mathbf{Z}_{\mathbf{vsi}}^{-1} \tag{4-47}$$

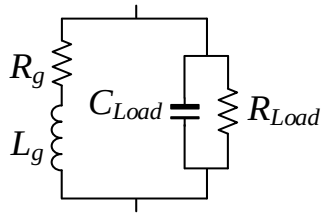
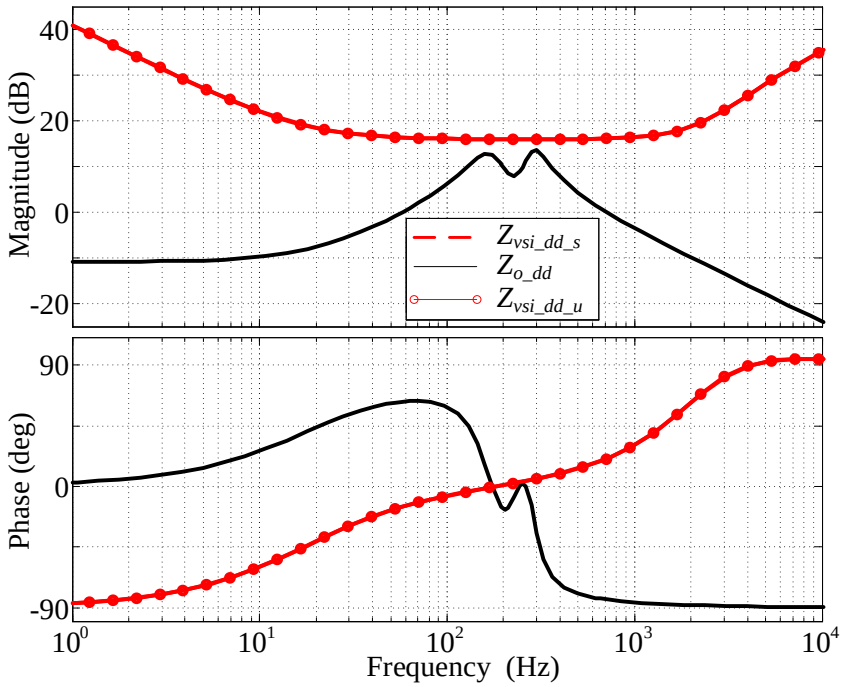
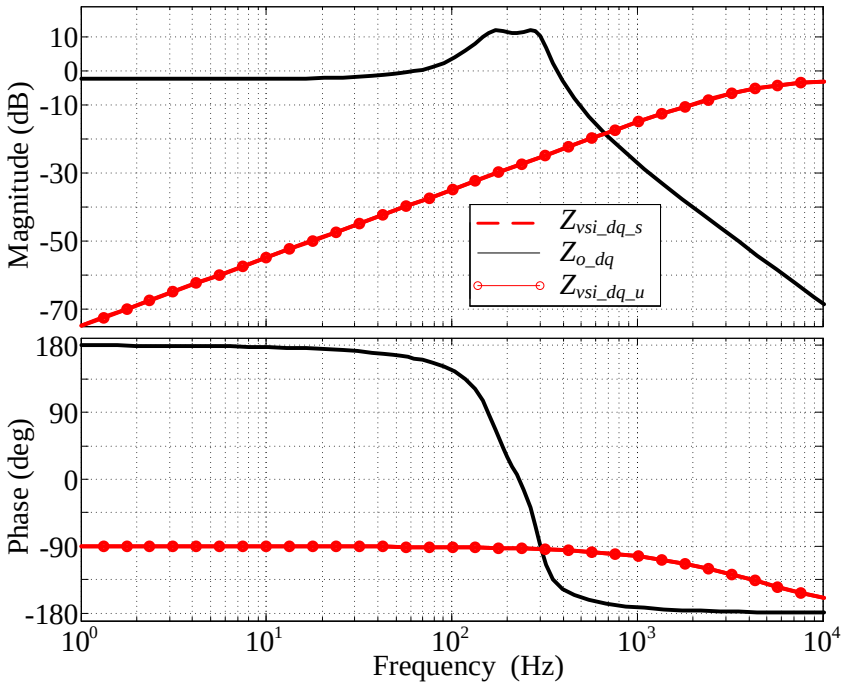


Fig. 4-21. One phase diagram of $\mathbf{Z_o}$ in stationary frame.

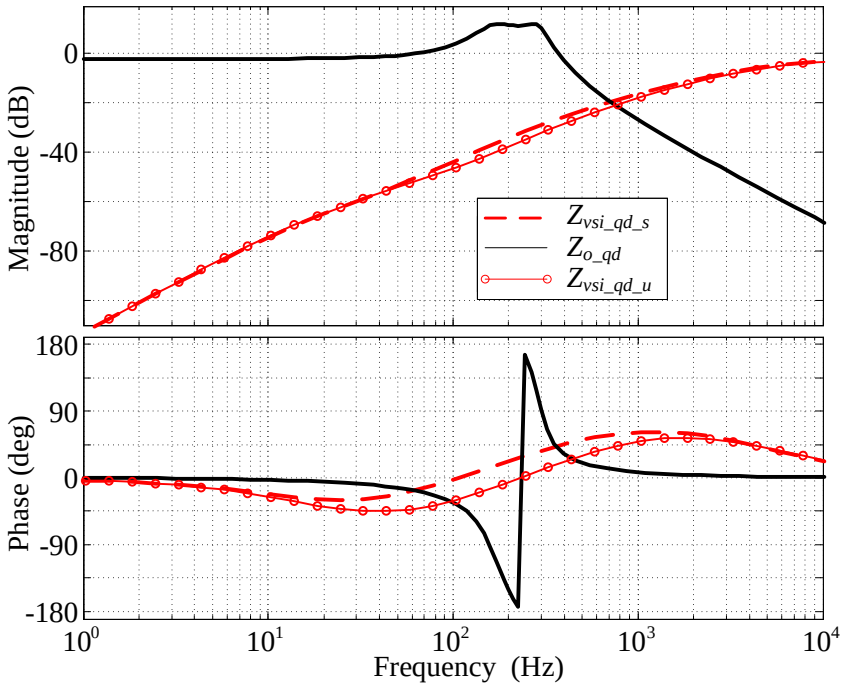
From small-signal point of view, $\mathbf{Z_o}$ is the parallel of grid impedance $\mathbf{Z_g}$ and load impedance $\mathbf{Z_L}$. One phase diagram of $\mathbf{Z_o}$ in stationary frame is shown in Fig. 4-21. Derivation of $\mathbf{Z_o}$ in *d-q* frame is discussed in Ref. [69], using the parameters listed in Table 4-3, $\mathbf{Z_o}$ in *d-q* frame is plotted in Fig. 4-22 as solid black line.



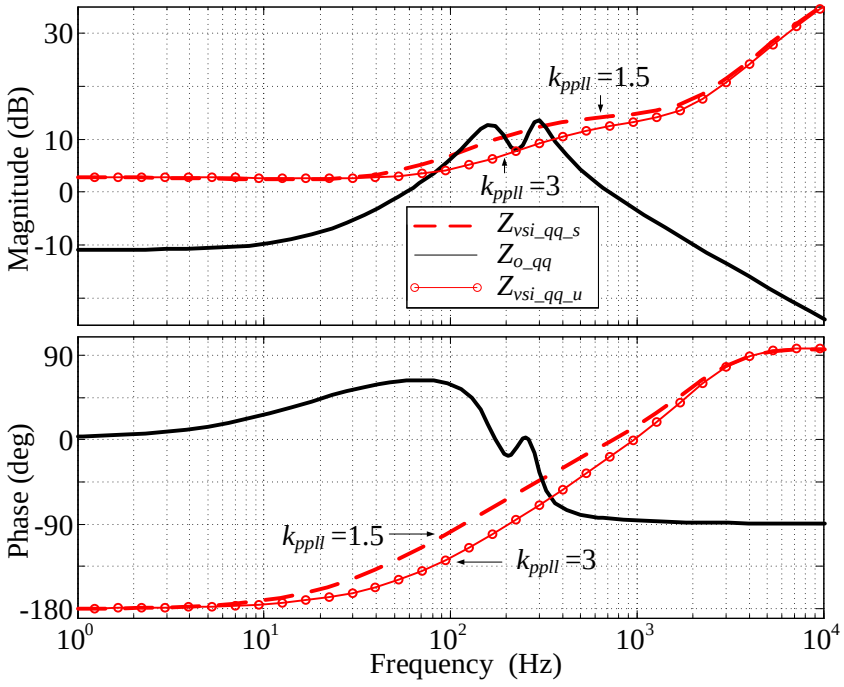
(a) Z_{dd} of grid side and VSI.



(b) Z_{dq} of grid side and VSI.



(c) Z_{qd} of grid side and VSI.

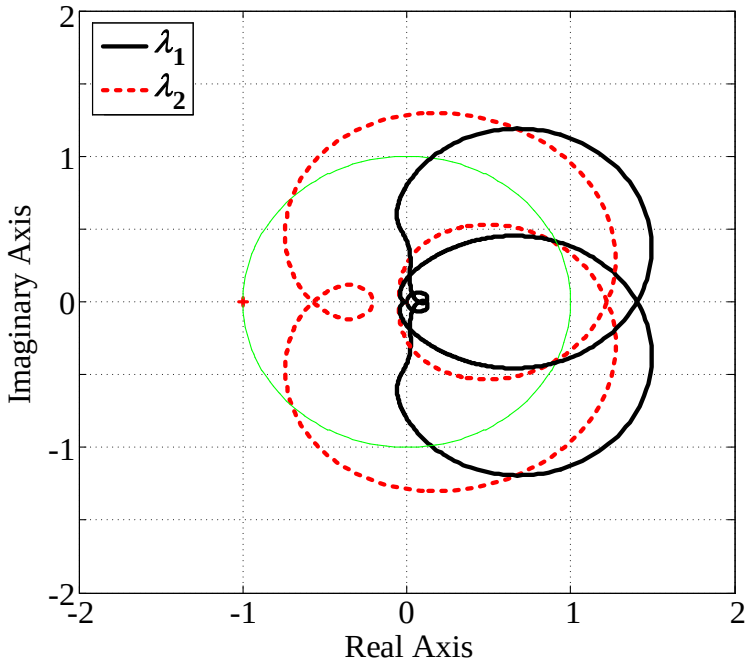


(d) Z_{qq} of grid side and VSI.

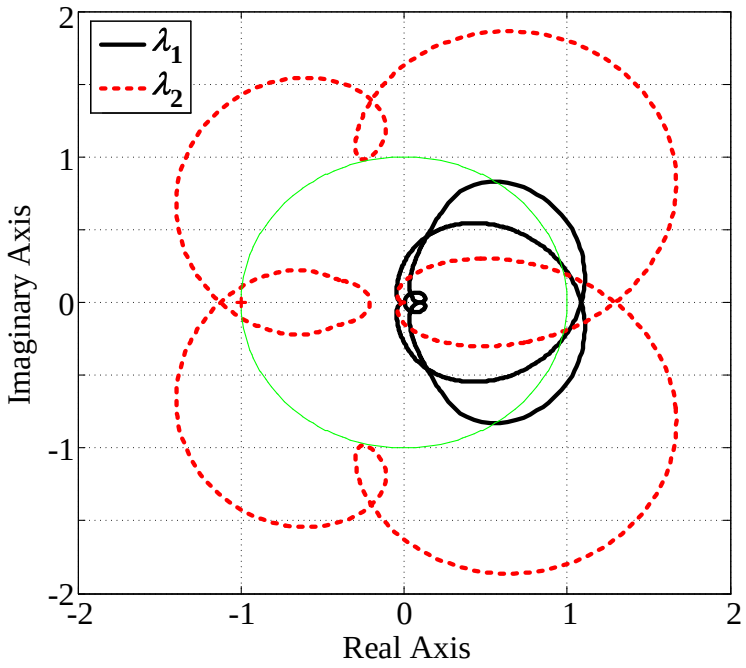
Fig. 4-22. Impedances of the source and load.

Using Eq. (4-30) and inverter parameters listed in Table 4-3, Z_{vsi} is calculated and plotted in Fig. 4-22 as a dashed red line for stable condition (k_{ppll} = 1.5) and a solid red line with a circle marker for unstable conditions (k_{ppll} = 3). The change of PLL design does not change Z_{vsi_dd} in Fig. 4-22 (a). Significant change has been introduced in Z_{vsi_qq}. There are small variation on Z_{vsi_dq} and Z_{vsi_qd}, but compare to Z_{vsi_qq}, these variation can be ignored, since they are over 30dB smaller than Z_{vsi_qq}. With bigger value of k_{ppll}, frequency range of negative resistor of Z_{vsi_qq} is extended. Instability is caused by Z_{vsi_qq}.

Using Z_o and Z_{vsi} and applying generalized Nyquist criterion (GNC) to impedance ratio L, stability conditions of the example system can be predicted correctly as shown in Fig. 4-23. In part (a) of Fig. 4-23, when k_{ppll} is 1.5, none of the system's characteristic loci encircles the critical point (-1, 0), and the system is stable. In part (b) of Fig. 4-23, when k_{ppll} is 3, one of the system's characteristic loci (λ_2) encircles the critical point, which indicates the system is unstable.



(a)



(b)

Fig. 4-23. GNC plots: (a) stable case (k_{pll} = 1.5); (b) unstable case (k_{pll} = 3).

In this example, grid-tied inverter is controlled with current controller, the negative resistor is only observed on Z_{qq}, not Z_{dd}. Z_{dq} and Z_{qd} are controlled with very small magnitude under unity power factor. Instability of the system is mainly due to Z_{qq}. When the inverter injects reactive power, magnitude of Z_{dq} becomes significant, but it is still not negative resistor. When power controllers are added and inverter injects reactive power, Z_{dq} and Z_{qd} could also behave as negative resistor as shown in Fig. 4-15. The impacts of Z_{dq} and Z_{qd} on system stability under these condition need more discussion in the future.

4.8 Experimental Verification

4.8.1 Grid-tied inverter system

In order to verify the proposed model, low power prototype of three-phase grid-tied inverter and *d-q* impedance measurement equipment [46] are built as shown in Fig. 4-24.

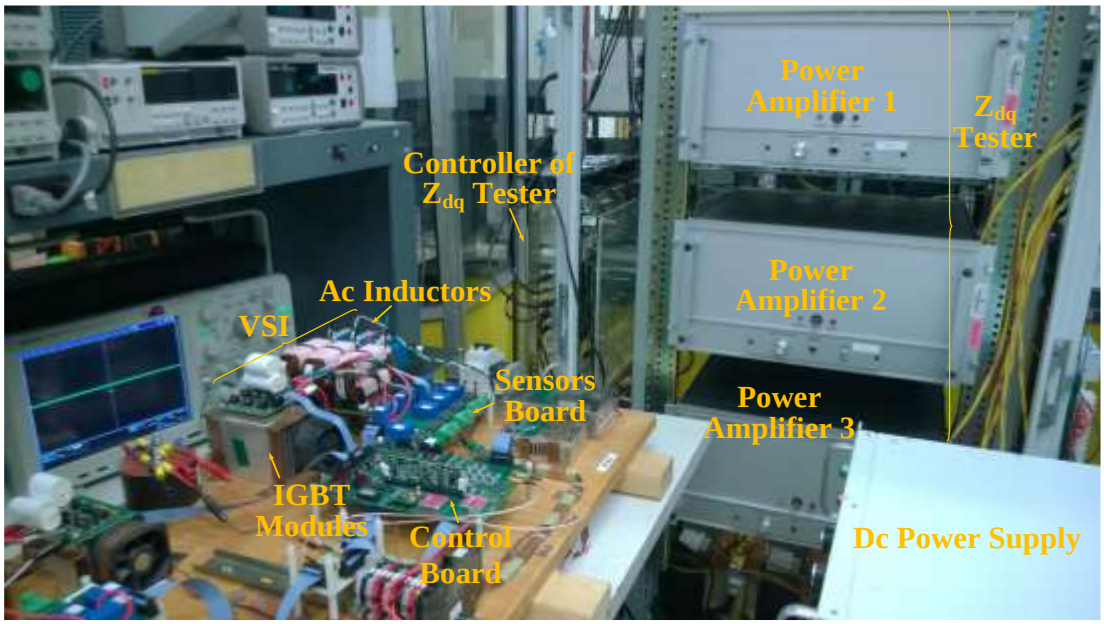
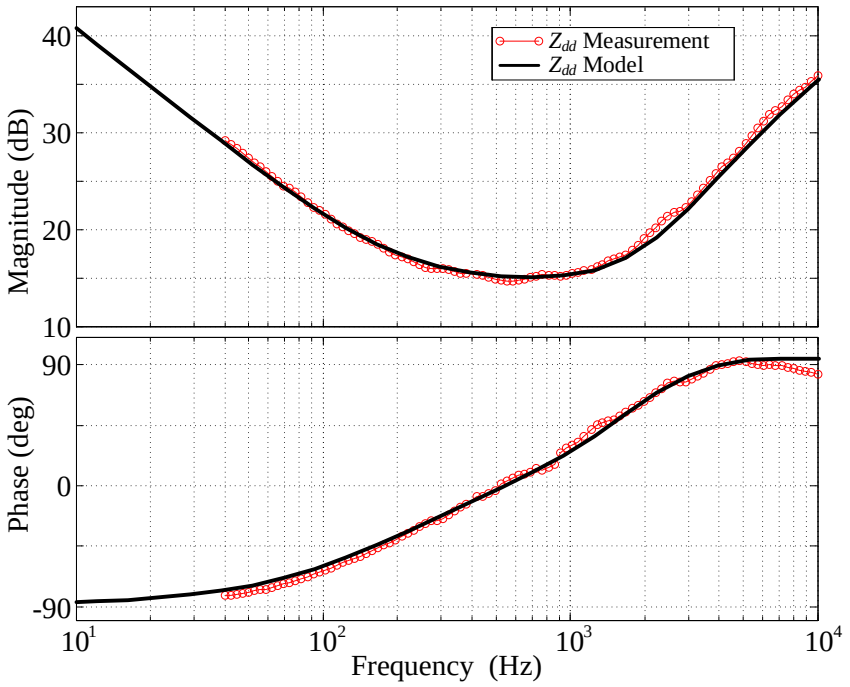


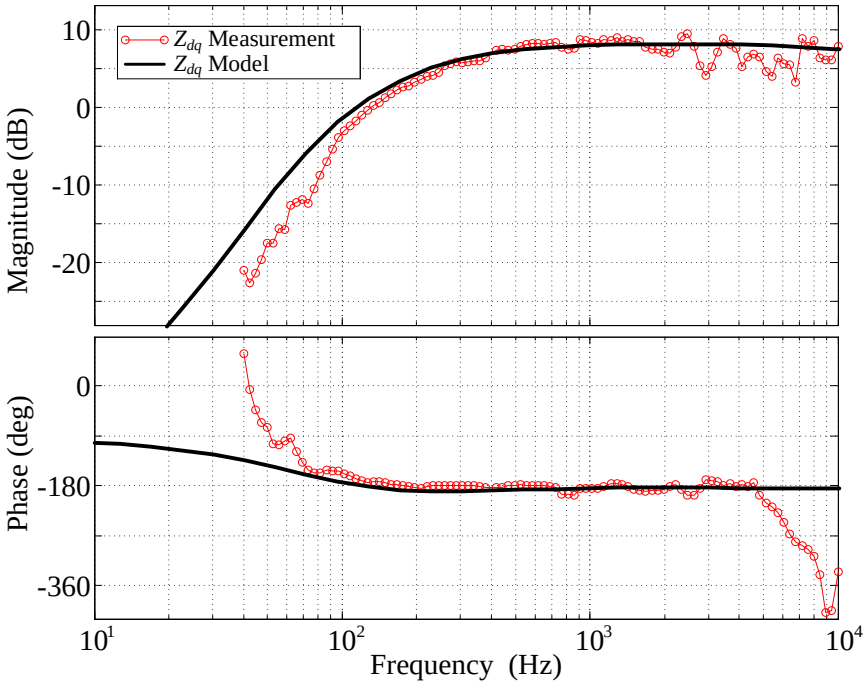
Fig. 4-24. Experimental system.

All the impedance were measured from 40 Hz to 10 kHz (half switching frequency of the inverter) with 100 points. For the cases with current feedback control and SRF PLL, inverter prototype with parameters list in Table 4-1 is used for measurement. For the cases with power feedback control and SRF PLL, parameters list in Table 4-2 is used for measurement.

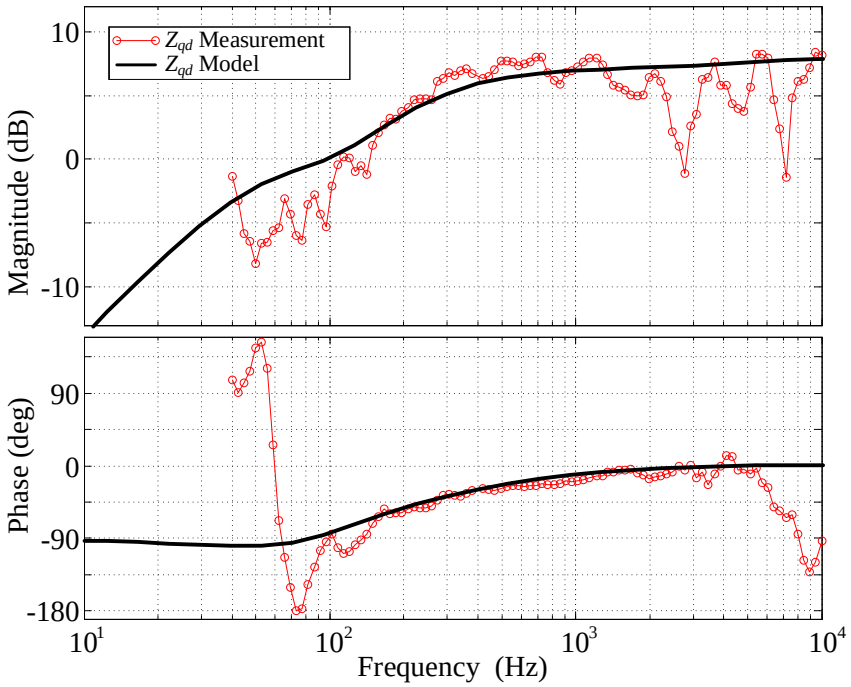
Fig. 4-25 shows the measured impedance over plotted with results calculated using proposed Eq. (4-30) for unit power factor control, where *d* channel current reference is -11 A and the SRF PLL bandwidth is 100 Hz. The results shows good accuracy of the proposed model. Fig. 4-26 shows Z_{qq} with different SRF PLL bandwidth. The measurement results clearly show the negative impedance behavior of Z_{qq} and its variation along with PLL bandwidth. Fig. 4-27 and Fig. 4-28 shows the measurement results with inductive and capacitive reactive power under current feedback control with 100 Hz SRF PLL bandwidth. Fig. 4-29 shows the measurement results with power feedback control where P_{ref} is -1150 W and Q_{ref} is 0 Var. All the measurement results match with the results predicted by the model very well.


Z_{dd} Measurement
Z_{dd} Model
Magnitude (dB)
40
30
20
10
Phase (deg)
90
0
-90
10^1
10^2
10^3
10^4
Frequency (Hz)

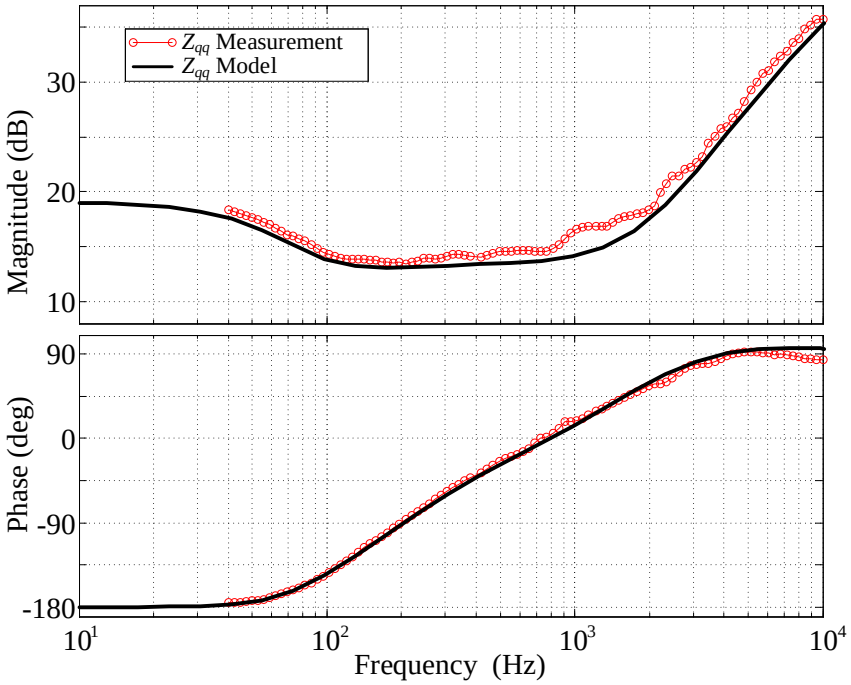
(a)


Z_{dq} Measurement
Z_{dq} Model
Magnitude (dB)
10
0
-10
-20
Phase (deg)
0
-180
-360
10^1
10^2
10^3
10^4
Frequency (Hz)

(b)


Z_{qd} Measurement
Z_{qd} Model
Magnitude (dB)
10
0
-10
Phase (deg)
90
0
-90
-180
10^1
10^2
10^3
10^4
Frequency (Hz)

(c)


Z_{qq} Measurement
Z_{qq} Model
Magnitude (dB)
30
20
10
Phase (deg)
90
0
-90
-180
10^1
10^2
10^3
10^4
Frequency (Hz)

(d)

Fig. 4-25. Model validation results for i_{dref} = -11.A, i_{qref} = 0 A, f_{bw_PLL} = 100 Hz.

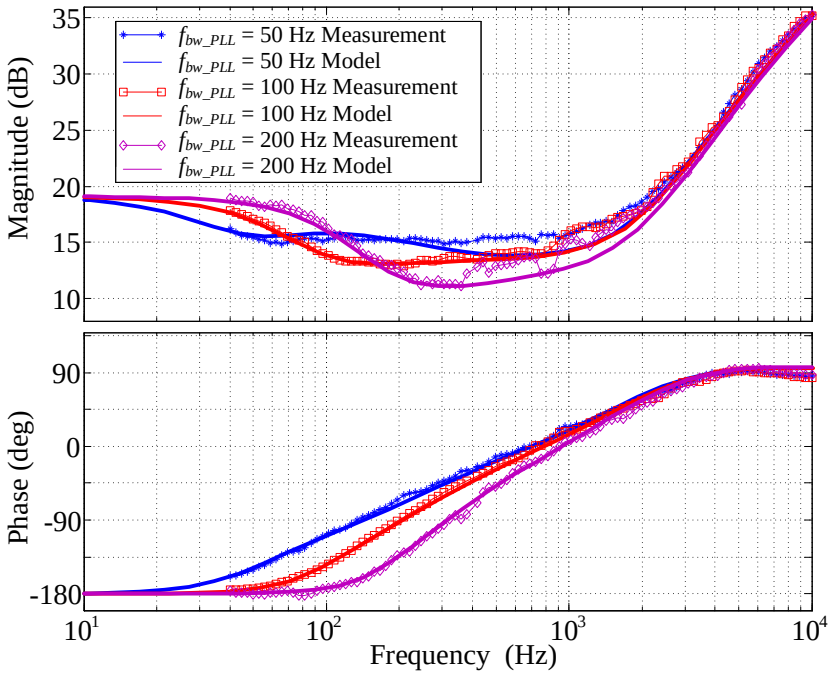
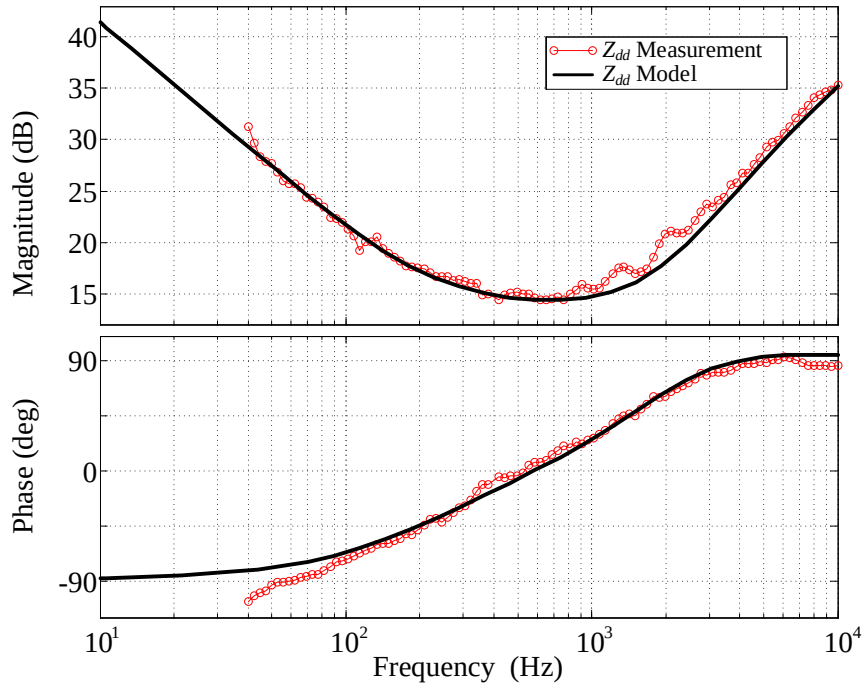
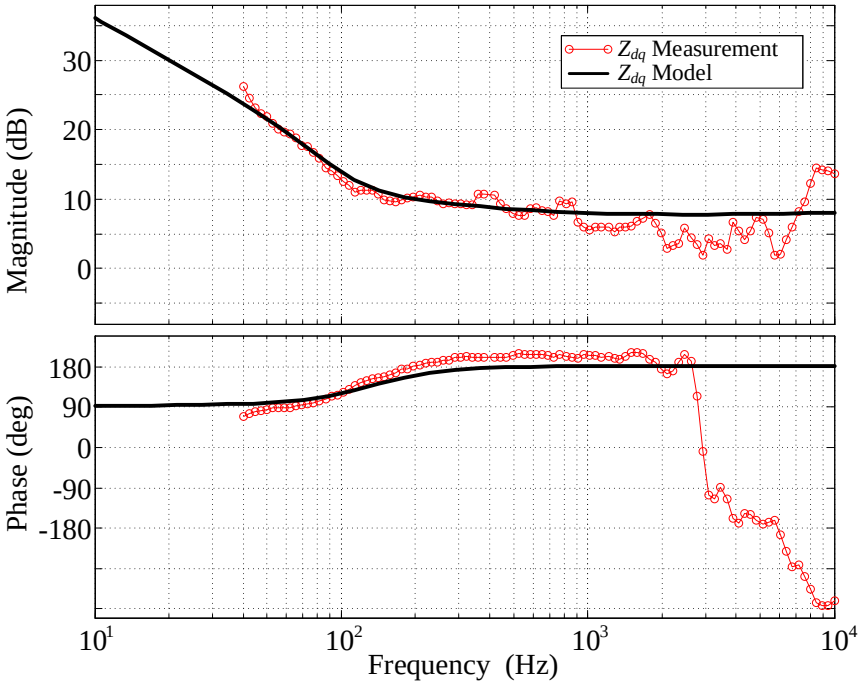


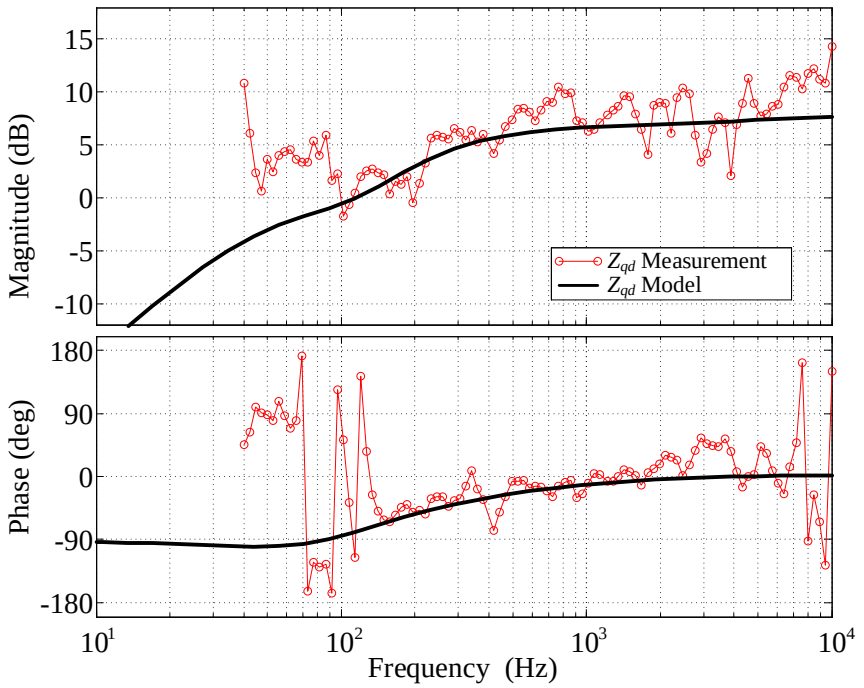
Fig. 4-26. Model validation results for i_{dref} = -11.A, i_{qref} = 0 A.



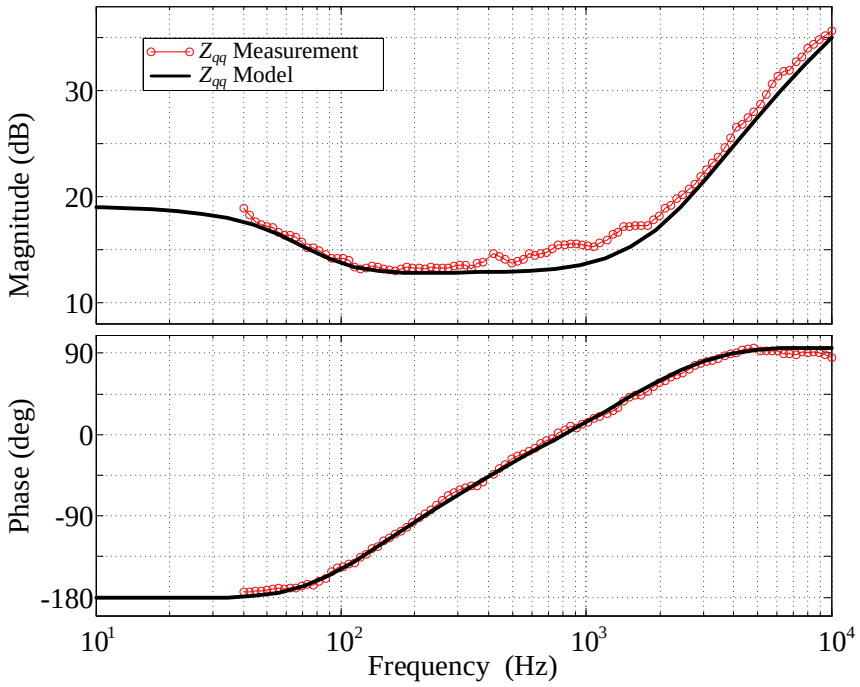
(a)


Z_{dq} Measurement
Z_{dq} Model
Magnitude (dB)
30
20
10
0
Phase (deg)
180
90
0
-90
-180
10^1
10^2
10^3
10^4
Frequency (Hz)

(b)

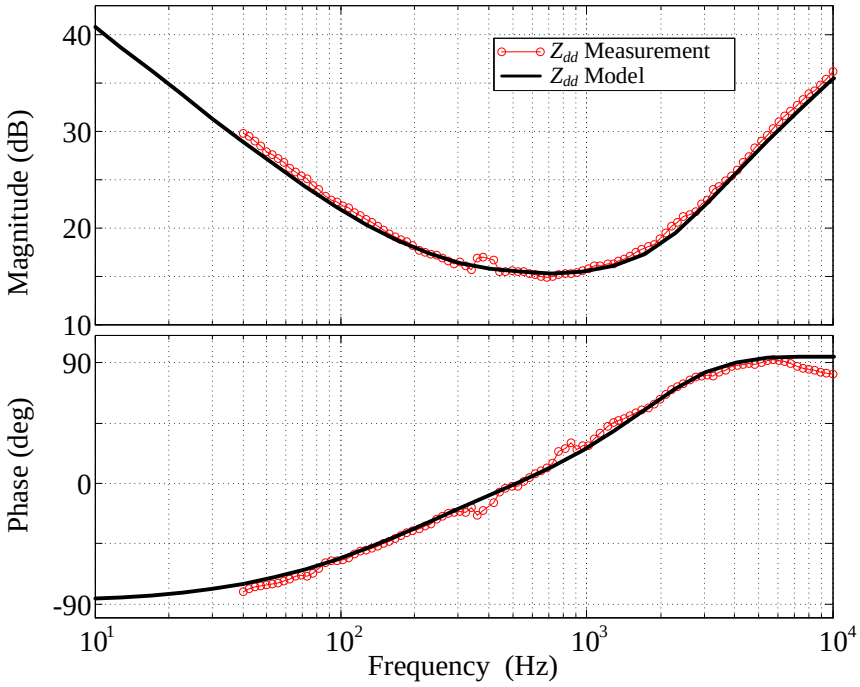

Z_{qd} Measurement
Z_{qd} Model
Magnitude (dB)
15
10
5
0
-5
-10
Phase (deg)
180
90
0
-90
-180
10^1
10^2
10^3
10^4
Frequency (Hz)

(c)

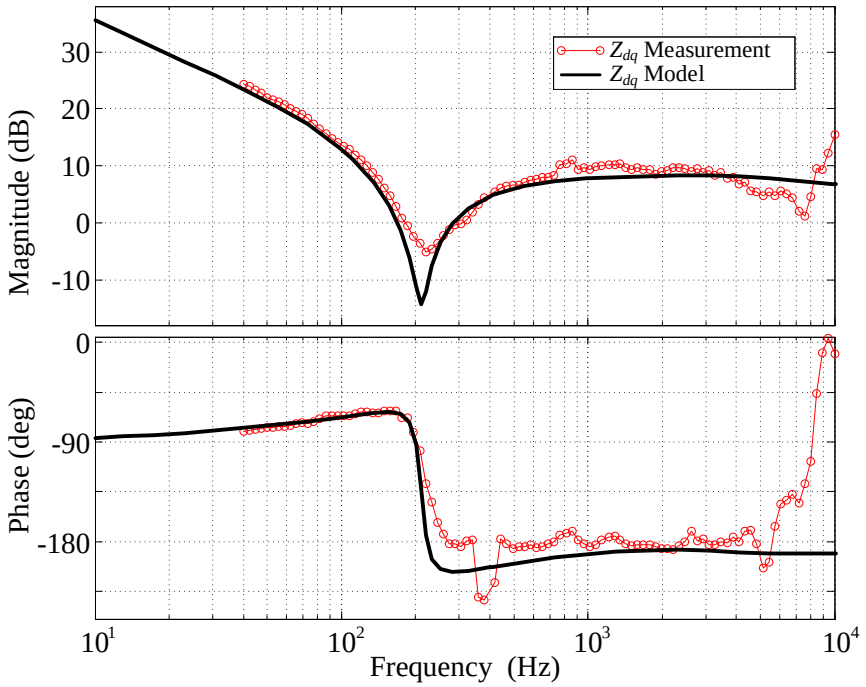


(d)

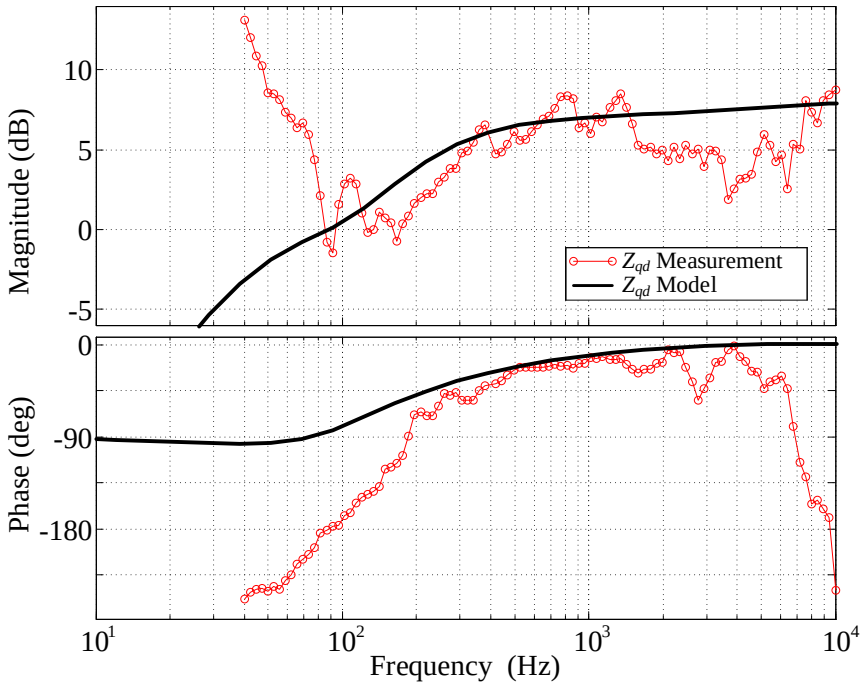
Fig. 4-27. Model validation results for i_{dref} = -11.A, i_{qref} = 6 A, f_{bw_PLL} = 100 Hz.



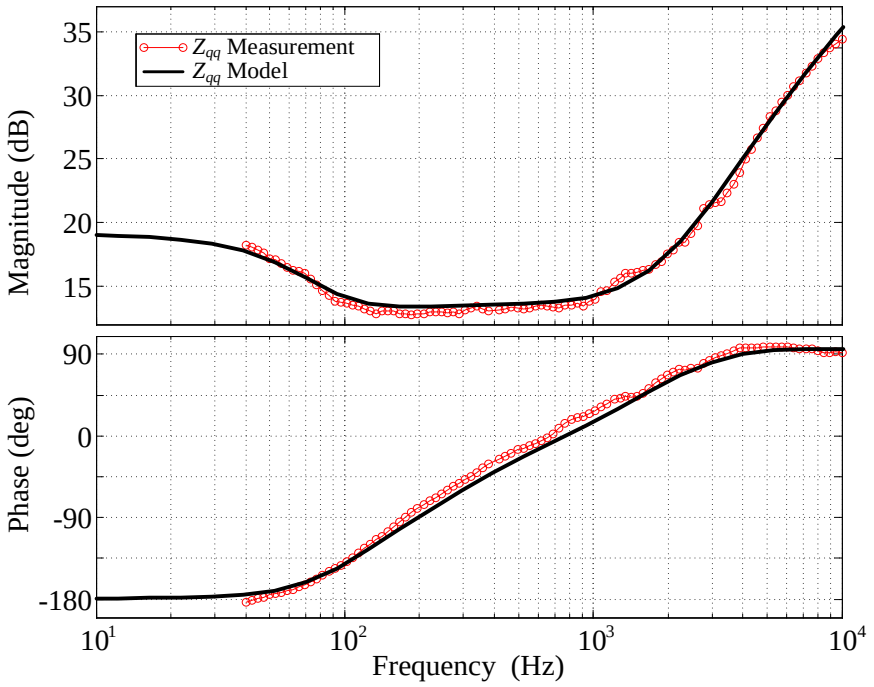
(a)


Z_{dq} Measurement
Z_{dq} Model
Magnitude (dB)
30
20
10
0
-10
Phase (deg)
0
-90
-180
10^1
10^2
10^3
10^4
Frequency (Hz)

(b)

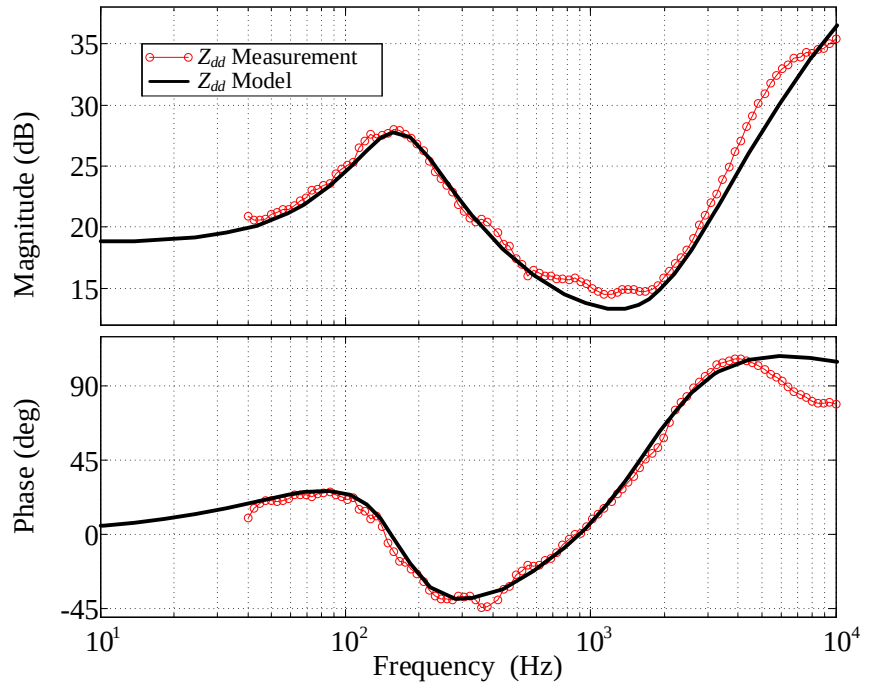

Z_{qd} Measurement
Z_{qd} Model
Magnitude (dB)
10
5
0
-5
Phase (deg)
0
-90
-180
10^1
10^2
10^3
10^4
Frequency (Hz)

(c)

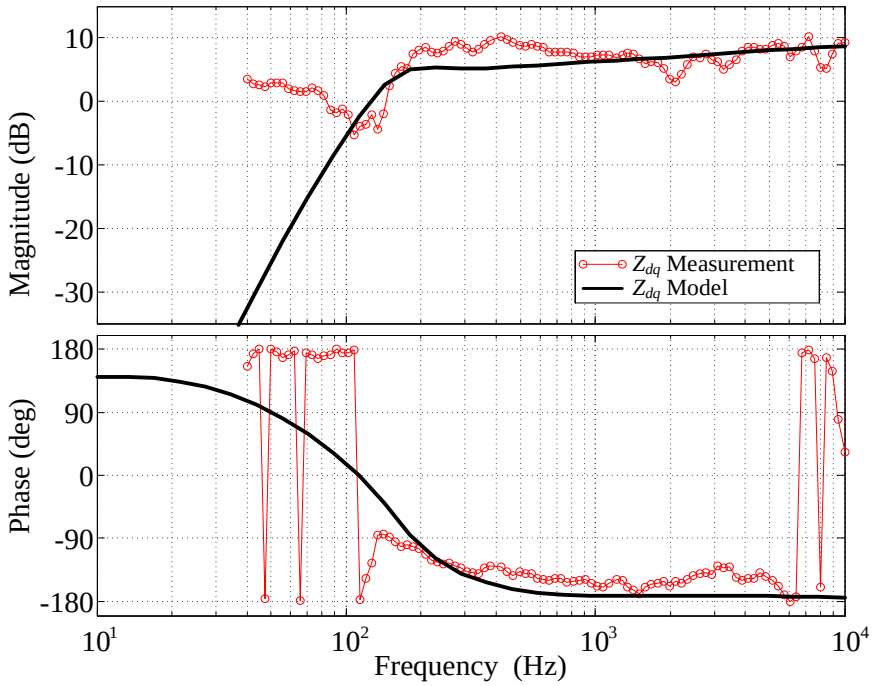


(d)

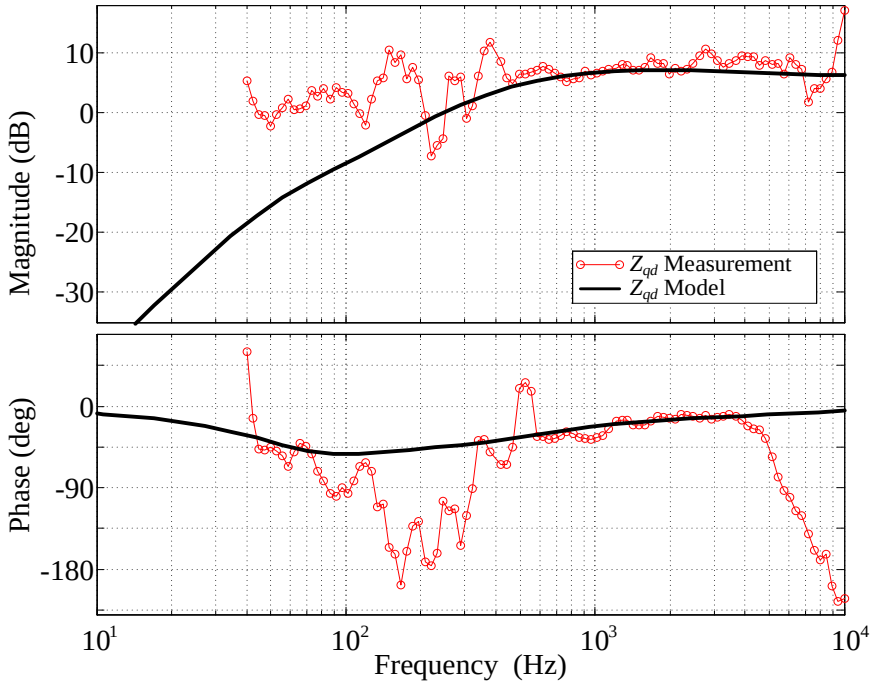
Fig. 4-28. Model validation results for i_{dref} = -11.A, i_{qref} = -6 A, f_{bw_PLL} = 100 Hz.



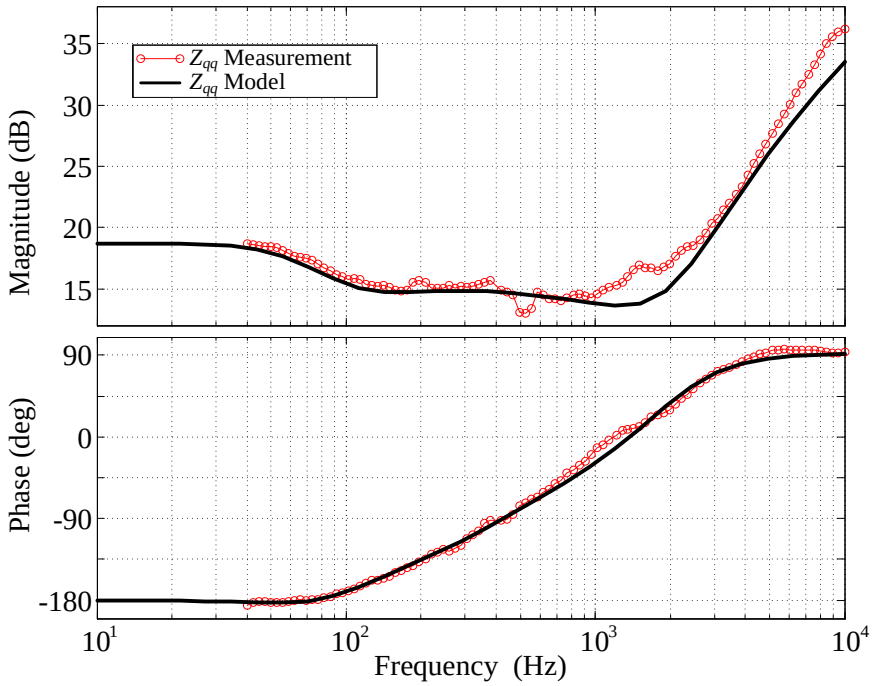
(a)


Magnitude (dB)
10
0
-10
-20
-30
Z_{dq} Measurement
Z_{dq} Model
Phase (deg)
180
90
0
-90
-180
10^1
10^2
10^3
10^4
Frequency (Hz)

(b)


Magnitude (dB)
10
0
-10
-20
-30
Z_{qd} Measurement
Z_{qd} Model
Phase (deg)
0
-90
-180
10^1
10^2
10^3
10^4
Frequency (Hz)

(c)



(d)

Fig. 4-29. Model validation results for P_{dref} = -1150 W, Q_{qref} = 0 Var, f_{bw_PLL} = 100 Hz.

4.8.2 AFE

To verify the proposed input impedance model for AFE, measurements are carried out on the built test-bed with the parameters list in Table 4-4. The results are shown in Fig. 4-30 for impedances and Fig. 4-31 for admittances. Fig. 4-32 shows the Z_{qq} of AFE with different PLL bandwidth. All the results show good agreement between model and measurement.

Table 4-4. Parameters of AFE system for measurement

Symbol	Description	Value
V_{ll}	Grid line-line peak voltage	$57.5\sqrt{6}$ V
f_g	Grid voltage frequency	60 Hz
f_{sw}	Switching frequency of AFE	20 kHz
L_{AFE}	Inductance of AFE	0.47 mH
C_{dc}	Dc link capacitor of AFE	100 μF
R_{dc}	Load resistor of AFE	96 Ω
V_{dcAFE}	Dc voltage of AFE	270 V
k_{piAFE}	Proportional gain of AFE current controller	0.0116
k_{iiAFE}	Integrator gain of AFE current controller	23.2711
k_{pvAFE}	Proportional gain of AFE voltage controller	0.0628
k_{ivAFE}	Integrator gain of AFE voltage controller	3.2725
$k_{ppllAFE}$	Proportional gain of AFE PLL	0.8921
$k_{ipllAFE}$	Integral gain AFE of PLL	39.64

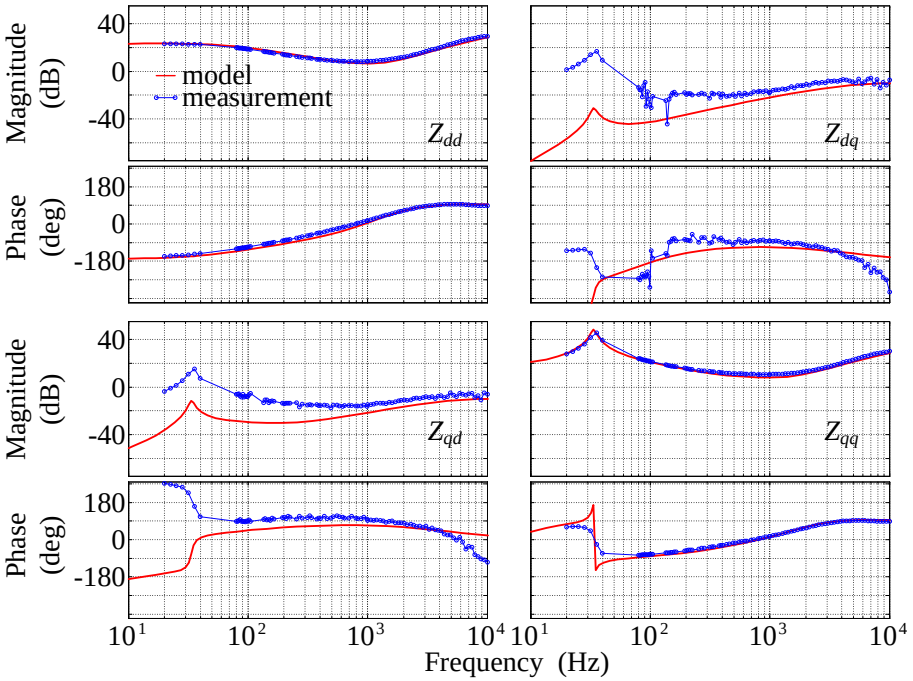


Fig. 4-30. Model validation results for $\mathbf{Z_{dqAFE}}$.

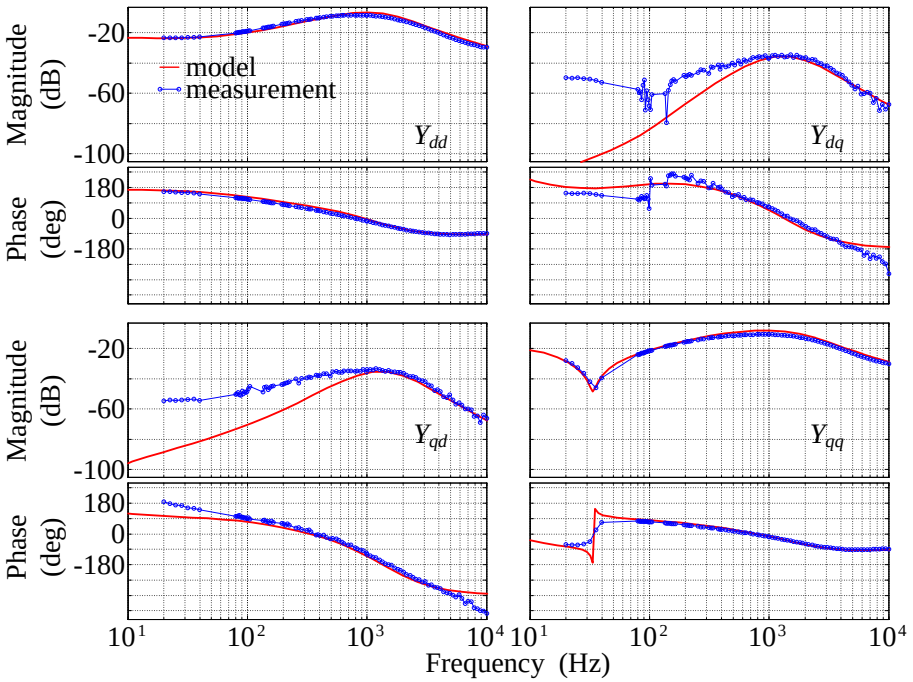


Fig. 4-31. Model validation results for $\mathbf{Y_{dqAFE}}$

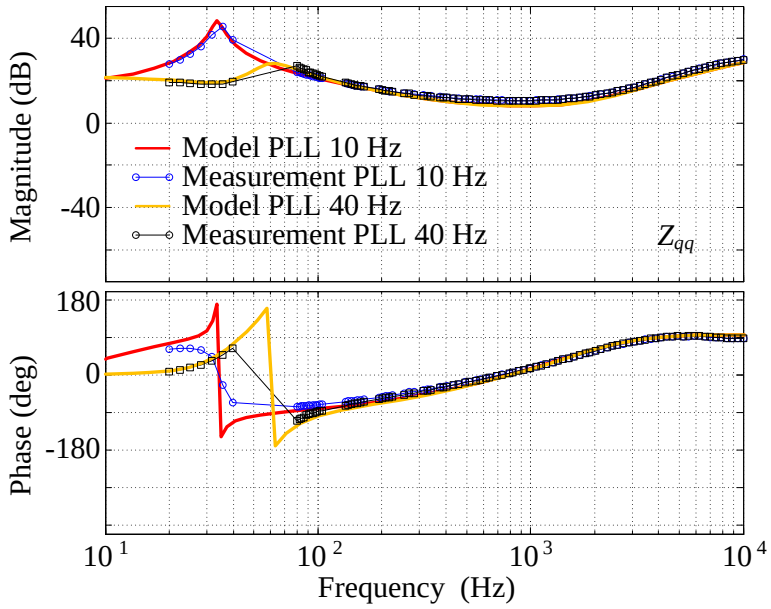


Fig. 4-32. Model validation results with different PLL bandwidth.

In both Fig. 4-30 and Fig. 4-31, there are significant errors in the off diagonal terms of the matrices. The author thinks the errors are not just due to measurement. There could be some dynamics which are not modeled. Further research are need to find out the reason.

Chapter 5 Synchronization Stability Issues Caused by PLL Dynamics

5.1 Introduction

More and more VSCs are installed to modern power systems. VSCs not only can improve the power utilization efficiency but also are key components to integrate new energy sources The systems like which has been shown in Fig. 5-1 have superior features to build the modern power grids, including controllability, sustainability, and the improved efficiency. However, many stability issues are reported regarding this system.

Interactions between VSCs and grid could make the system unstable. AFE can destabilize the system due to its constant power load (CPL) behavior as discussed in chapter 3. PLLs are needed for VSCs to synchronize with the grid. Chapter 4 shows that PLL shapes Z_{qq} of grid-tied inverter as negative increamental resistor within its bandwidth. Together with large grid side impedances, this negative resistor could destabilize the inverter system. PLL shapes Z_{qq} of AFE as positive increamental resistor within its bandwidth. Changing PLL bandwidth could also lead the AFE system in to instability when the source side output impedance is high.

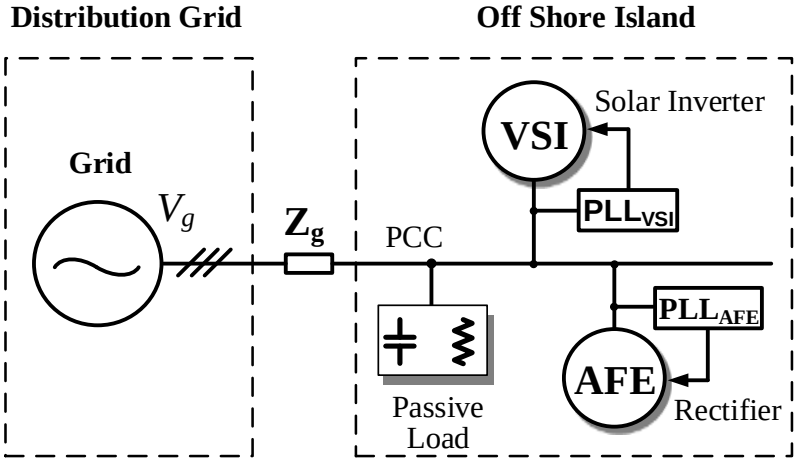


Fig. 5-1. Distribution system with high penetration of VSCs.

Designs of PLL for VSI and AFE usually consider the grid impedance is zero. When PLLs are designed to be stable with certain margin by checking the loop gains of PLLs, VSI and AFE should synchronize with the ideal grid. Due to the parallel connection, VSI and AFE utilize the same voltage information at the point of common coupling (PCC) to do synchronization. Under weak grid condition, grid impedance cannot be ignored. PCC voltage is then not only determined by the grid voltage, but also grid impedance $\mathbf{Z_g}$ and current injected by VSI and AFE. In this way, PLLs of VSI and AFE couple with each other. With certain grid side impedance $\mathbf{Z_g}$, these PLLs could be unstable which eventually makes the whole system lose synchronization and collapse [68], although they are designed to be stable under the assumption that grid impedance is zero. Ref. [68] proposes a PLL small-signal model including grid side impedances. The model gives deep insight of the coupling nature of grid-connected VSCs through their PLLs. Synchronization instability issue caused by PLL can be predicted using the model. However, the proposed analysis uses characteristic equation of PLLs which involves control parameters of every converter. For system integration, converters in the system are usually acquired as "black boxes". It may be found that the system oscillates or becomes unstable because the particular grid or load impedances were not foreseen by the converters' designers. Under such condition, design specifications for each converter to avoid instability cannot be defined easily using characteristic equation based method.

On the other hand, the impedance-based method, which does not need converters' internal design information, applies Nyquist stability criteria to the ratio between output impedance of the source and the load input impedance for the stability analysis. Such method is well established for converter-filter or general source-load interaction problems in dc electronic power conversion systems [28], [35]–[37]. It is preferred by system integrator for the reason that stability issue can be predicted based on measured impedances of the source and load [10].

In the case of three-phase ac systems, the impedance-based stability can be formulated using the synchronous *d-q* frame source and load impedances, where the generalized Nyquist stability criterion (GNC) or generalized inverse Nyquist stability criterion (GINC) is applied to return-ratio matrix defined by the product of the source impedance and load admittance [2]–[43]. This method was used to study the stability of a hybrid ac/dc system in Ref. [3], and the resonances

between input filter and three-phase converters in Ref. [69]. Although impedance-based analysis is also proposed to study the stability of grid-connected inverter systems [79]. Such analysis is not reported to analyze the synchronization stability issue between parallel connected VSCs and the grid as discussed above. To fill this gap, this paper proposes to use impedance-based analysis in the *d-q* frame for such instability issue. Furthermore, this synchronization instability is found to be caused by the interaction between negative incremental resistor behavior of VSI and positive incremental resistor behavior of AFE in *q* channel. Instability can be migrated simply by changing the PLL design of each converter.

5.2 Synchronization Instability between Parallele-Connected Three-Phase VSCs

The synchronization instability between parallel-connected three-phase VSCs is discussed in this section using the example system shown in . The instability is caused by a small change of VSI's PLL design.

5.2.1 Components in the system and their parameters

There are four components in the system shown in Fig. 5-1, including VSI, AFE, passive load and the grid. Parameter of this system is shown in Table 5-1.

Fig. 5-2 shows the circuit and control systems' diagram of VSI. Power stage of VSI is a two-level full bridge inverter with ac inductors. PCC voltages are measured by PLL in order to estimate the phase of the ac bus voltage and synchronize the operation of inverter with the grid. Inductor currents are measured in the current feedback control-loop. VSI is then controlled as a current source injecting power to the ac bus.

Power stage of AFE is a two-level three-phase boost rectifier as shown in Fig. 5-3. PCC voltages are measured for PLL to do grid-synchronization for AFE. Boost inductor currents and output voltage are measured by inner current and outer voltage feedback control-loops. All control systems of VSI and AFE are implemented in *d-q* frame [41].

Table 5-1. Parameters of simulation system

Symbol	Description	Value
V_g	Grid phase-neutral peak voltage	$120\sqrt{2}$ V
f_g	Grid frequency	60 Hz
ω_g	Grid angular frequency	$2\pi \times f_g$
L_{VSI}	Inductance of inverter	1 mH
V_{dcVSI}	Inverter dc voltage	600 V
f_{sw}	Switching frequency of VSI and AFE	20 kHz
$I_{drefVSI}$	*d* channel current of VSI	140 A
$I_{qrefVSI}$	*q* channel current of VSI	0 A
k_{piVSI}	Proportional gain of VSI current controller	0.0105
k_{iiVSI}	Integrator gain of VSI current controller	1.1519
$k_{ppllVSI}$	Proportional gain of VSI PLL	0.1
$k_{ipllVSI}$	Integral gain of VSI PLL	3.2 (unstable);0.32 (stable)
L_{AFE}	Inductance of AFE	0.5 mH
C_{dcAFE}	Dc link capacitor of AFE	100 μF
R_{dc}	Load resistor of AFE	13.825 Ω
V_{dcAFE}	Dc voltage of AFE	600 V
k_{piAFE}	Proportional gain of AFE current controller	0.0052
k_{iiAFE}	Integrator gain of AFE current controller	1.152
k_{pvAFE}	Proportional gain of AFE voltage controller	0.0628
k_{ivAFE}	Integrator gain of AFE voltage controller	45.45
$k_{ppllAFE}$	Proportional gain of AFE PLL	0.05
$k_{ipllAFE}$	Integral gain AFE of PLL	0.5
Z_L	Local passive load	R_{Load}: 10 Ω; C_{Load}: 250 μF
Z_g	Grid impedance	R_g: 1.1 Ω; L_g: 200 μH
ω_n	Natural frequency of signal conditioning filter	1.23e6 rad/s
ζ	Damping factor of signal conditioning filter	4.74e-13
T_{del}	Time delay due to digital control and PWM	$1.5/f_{sw}$

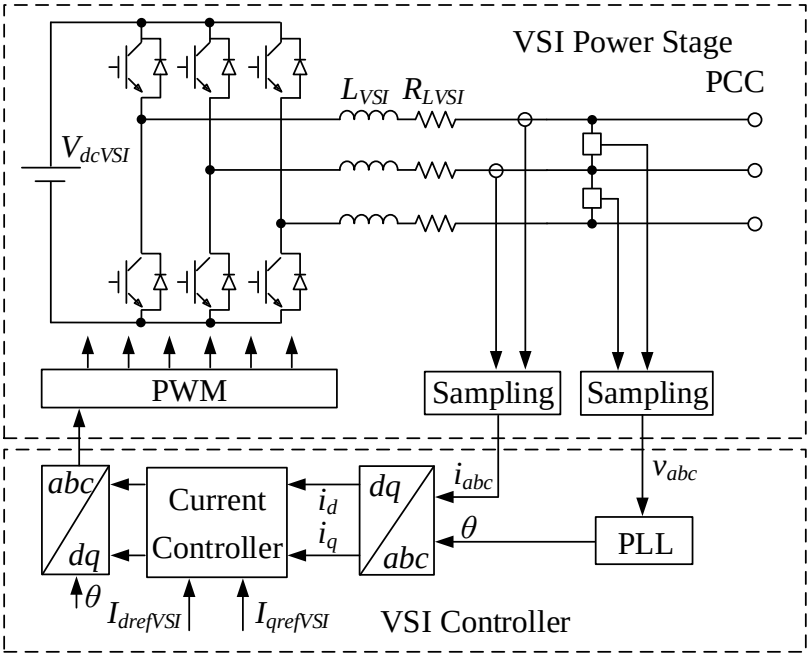


Fig. 5-2. Power stage and control system of VSI.

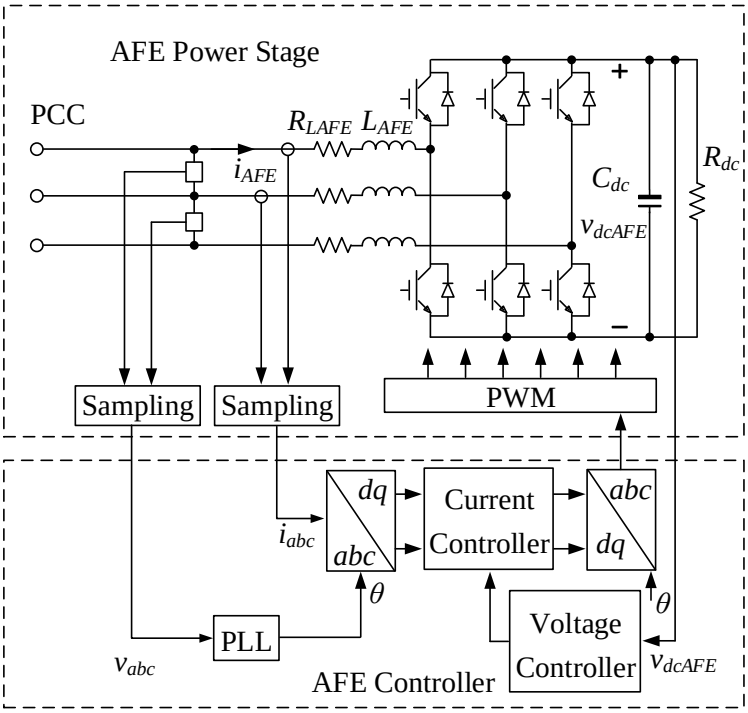
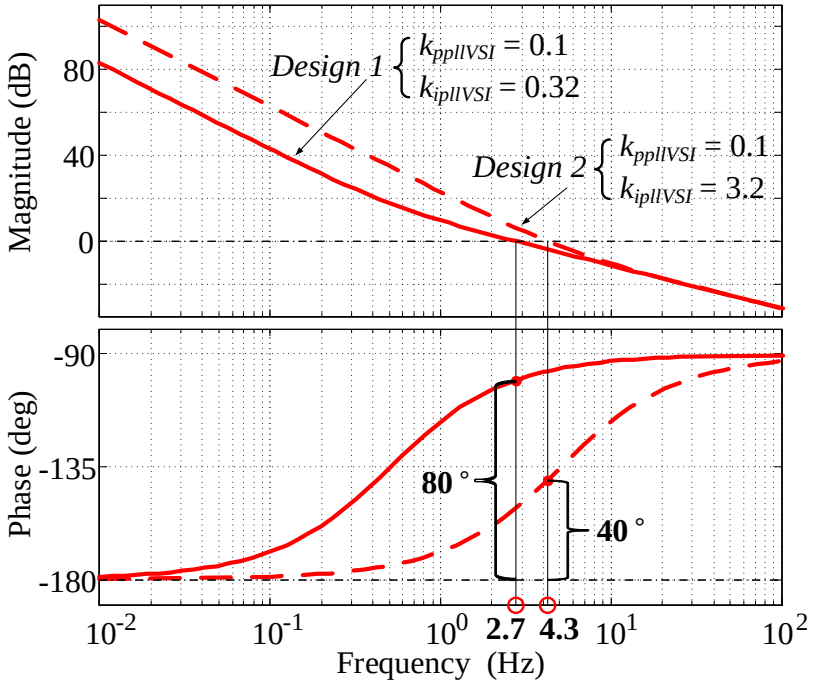
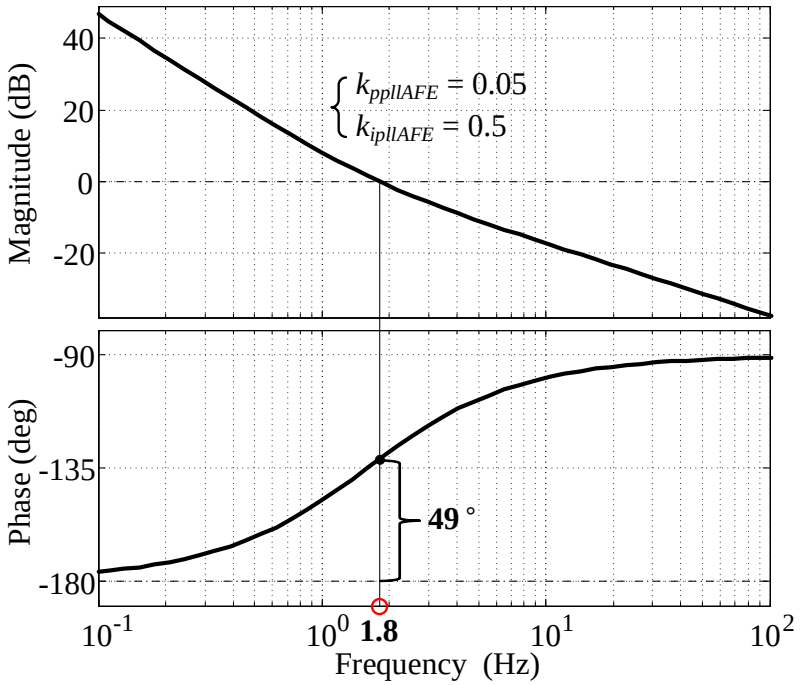


Fig. 5-3. Power stage and control system of AFE.

Both VSI and AFE use the synchronous reference (*d-q*) frame (SRF) PLL [63] strategy as shown in Fig. 2-58. Typical PLL design assumes zero impedance in the grid side. In Fig. 5-4 (a), loop gains of two PLL designs for VSI are shown, both designs are stable with bandwidth less than 5 Hz and phase margin over 40 °with ideal grid. Fig. 5-4 (b) shows the loop gain of AFE's PLL under the zero grid impedance assumption.



(a) VSI.



(b) AFE.

Fig. 5-4. PLL loop-gains for VSI and AFE with ideal grid.

Grid and load impedances are shown in Fig. 5-5.

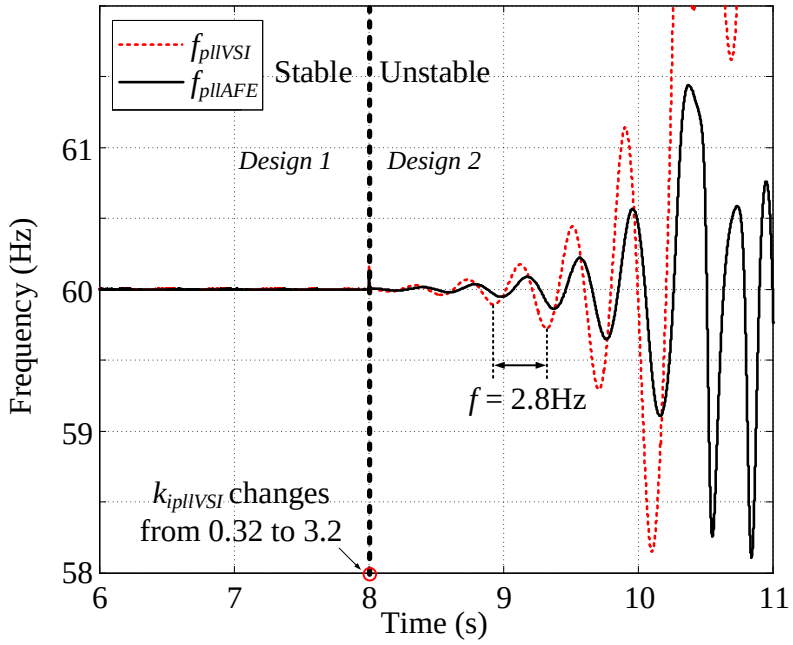
(a) (b)

Fig. 5-5. (a) Grid impedance $\mathbf{Z_g}$; (b) Load impedance $\mathbf{Z_L}$.

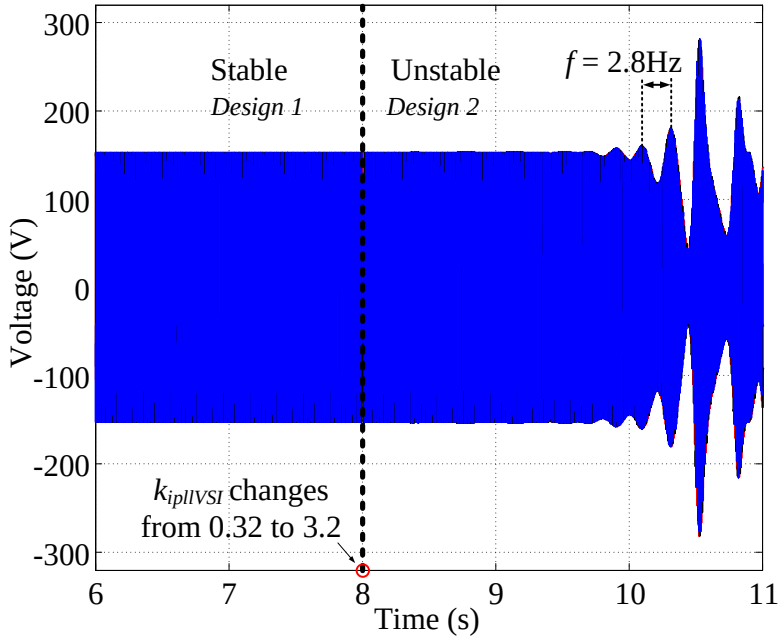
5.2.2 Synchronization instability

Fig. 5-6 shows the time domain simulation results of the system. In the simulation, within the time range from 0 to 8 second, the system is running under stable condition. At 8 second, integral gain ($k_{ipllVSI}$) of PI regulator in VSI's PLL is increased from 0.32 (*Design 1*) to 3.2 (*Design 2*), PLL output frequencies of VSI and AFE start to oscillate as shown in Fig. 5-6 (a). Fig. 5-6 (b)

shows the PCC three-phase voltages which indicates the whole system becomes unstable with a small change of PLL parameters. When VSI uses PLL *Design 1*, multi-converter system shown in Fig. 5-1 is stable. When VSI uses PLL *Design 2*, VSI and AFE in the multi-converter system lose synchronization and system is unstable.



(a)

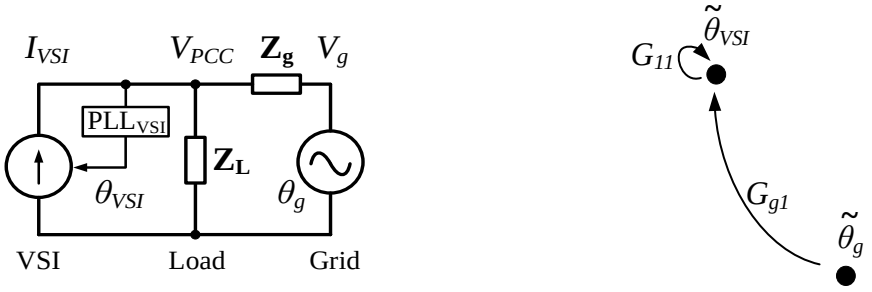


(b)

Fig. 5-6. (a) PLLs' output frequencies; (b) PCC voltages.

5.3 PLL-Based Stability Analysis

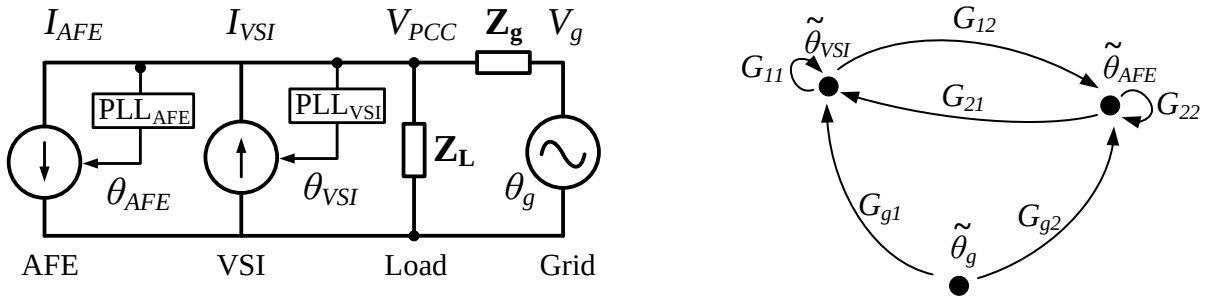
The low frequency synchronization instability as shown in section 5.2 can be analyzed using PLLs' small-signal model [68]. This method is briefly summarized here.



(a) Single line circuit. (b) SFG.

Fig. 5-7. Representations of VSI with local load connecting to the grid.

Fig. 5-7 (a) shows the single line representation of VSI connecting to the grid with local load and grid impedance. As shown in Fig. 5-2, VSI is controlled as current source. Within the current control bandwidth, which usually is much higher than line frequency, VSI can be modeled as a controlled current source which frequency and angle is commanded by PLL. PLL collects PCC voltages to work synchronously with grid. As illustrated by Fig. 5-7 (a), PCC voltages are determined not only by the grid voltage, but also by the current injected from VSI to the impedance network formed by $\mathbf{Z_L}$ and $\mathbf{Z_g}$. This means, VSI not only synchronizes with the grid, but also with itself. If grid voltage phase θ_g, and VSI current phase θ_{VSI}, which is the output of VSI's PLL, are chosen as state variables, small-signal model of PLL in the grid-tied inverter system shown in Fig. 5-7 (a) can be represented using signal-flow-graph (SFG) shown in Fig. 5-7 (b). In Fig. 5-7 (b), transfer function G_{11} represents the self-synchronization dynamic of PLL, transfer function G_{g1} represents the grid-synchronization dynamic.



(a) Single line circuit. (b) SFG.

Fig. 5-8. Representations of VSI and AFE with local load connecting to the grid.

When AFE is also connected to PCC, PCC voltages are formed by grid voltage, the current injected by VSI and AFE as shown in Fig. 5-8 (a). Each converter in the system not only has grid synchronization, self-synchronization, but also cross synchronization (G_{12} and G_{21}) with other converter as shown in Fig. 5-8 (b).

Ref. [68] reports that the multiple grid-tied VSCs system synchronization stability can be predicted by PLL's closed-loop transfer function of each VSC. For example, Eq. (5-1) shows the transfer function of VSI in the system shown in Fig. 5-8 (a), when the transfer function has right-

half plane pole (RHP), low frequency synchronization instability discussed in section 5.2 happens. Detailed analysis can be found in Ref. [68].

$$\frac{\tilde{\theta}_{VSI}}{\tilde{\theta}_g} = \frac{G_{g1}(1-G_{22})+G_{g2}G_{21}}{1-(G_{12}G_{21}+G_{11}+G_{22})+G_{11}G_{22}} = \frac{N(s)}{D(s)} \tag{5-1}$$

This PLL small-signal model based analysis gives a deep insight to the PLL interaction between grid and converters. On the other hand, this method needs not only the impedance of grid, the impedance of local passive load, but also the parameters of every converter's PLL which may not available to system integrator. SFG of two-converter system is not simple already. The scale of SFG will increase exponentially when number of converters increases. Then, to find the model of the system is not easy. In addition, from this method, design specification for each converter cannot be made to guarantee system synchronization stability.

5.4 Impedance-Based Analysis

Impedance-based small-signal stability analysis, first proposed by Ref. [28] for filter and dc-dc converter system, models the system into two subsystem as shown in Fig. 5-9. The source subsystem is modeled by its Thevenin equivalent circuit, which consists of an ideal voltage source (v_s) in series with an output impedance (Z_s). Load subsystem is modeled by its input impedance. Then the interface voltage (v_l) can be derived as Eq. (5-2). If the minor loop gain, or return ratio [3], is defined as Eq. (5-3), which is the ratio between source and load impedances, the condition for system stability can be determined by checking whether the minor loop gain ($L(s)$) satisfies the Nyquist stability criterion or not.

$$v_l(s) = \left[1 + Z_s(s)Z_l^{-1}(s)\right]^{-1} v_s(s) \tag{5-2}$$

$$L(s) = Z_s(s)Z_l^{-1}(s) \tag{5-3}$$

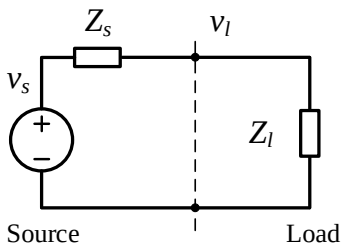


Fig. 5-9. Small-signal representation of a dc system.

Small-signal impedances of power converters are the linearization of nonlinear circuits around their equilibrium points. For three-phase ac system, no equilibrium point exits in stationary (*abc*) frame. By doing transformation (see Eq. (5-4)) from stationary frame to synchronous reference (*d*-*q*) frame, balanced three-phase ac system becomes two coupled dc systems. Small-signal impedances in *d*-*q* frame can then be derived by doing traditional linearization. Similar to dc system, the balanced three-phase ac system can be then presented by source and load subsystems as shown in Fig. 5-10.

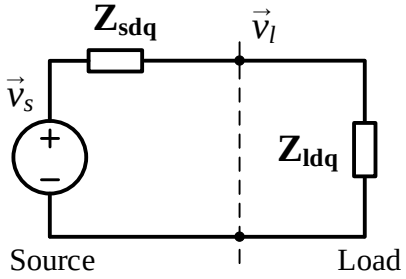


Fig. 5-10. Small-signal representation of a balanced three-phase system in *d*-*q* frame.

$$\mathbf{T}_{dq/abc} = \sqrt{\frac{2}{3}}\begin{bmatrix} \cos(\theta) & \cos\left(\theta-\frac{2}{3}\pi\right) & \cos\left(\theta+\frac{2}{3}\pi\right) \\ -\sin(\theta) & -\sin\left(\theta-\frac{2}{3}\pi\right) & \sin\left(\theta+\frac{2}{3}\pi\right) \end{bmatrix} \tag{5-4}$$

Different from impedances of dc-dc converters, impedances of three-phase ac converters are 2-by-2 matrices as shown by Eq. (5-5). This is due to the coupling effect between *d*-axis and *q*-axis.

$$\mathbf{Z}_{\mathbf{dq}}(s)=\begin{bmatrix} Z_{dd}(s) & Z_{dq}(s) \\ Z_{qd}(s) & Z_{qq}(s) \end{bmatrix} \tag{5-5}$$

Similar to dc system, the interface voltage ($\mathbf{v_{ldq}}$) can be derived as Eq. (5-6). Minor loop gain is defined as Eq. (5-7), which is the ratio between source and load impedances in *d-q* frame.

$$\vec{v}_l(s)=\left[\mathbf{I}+\mathbf{Z}_{\mathbf{sdq}}(s)\mathbf{Z}_{\mathbf{ldq}}^{-1}(s)\right]^{-1}\vec{v}_s(s) \tag{5-6}$$

$$\mathbf{L}(s)=\mathbf{Z}_{\mathbf{sdq}}(s)\mathbf{Z}_{\mathbf{ldq}}^{-1}(s) \tag{5-7}$$

As reported by Ref. [3], the condition for balanced three-phase ac system stability can be determined by applying generalized Nyquist stability criterion (GNC) [4] or generalized inverse Nyquist criterion (GINC) [43] to the minor loop gain $\mathbf{L}(s)$.

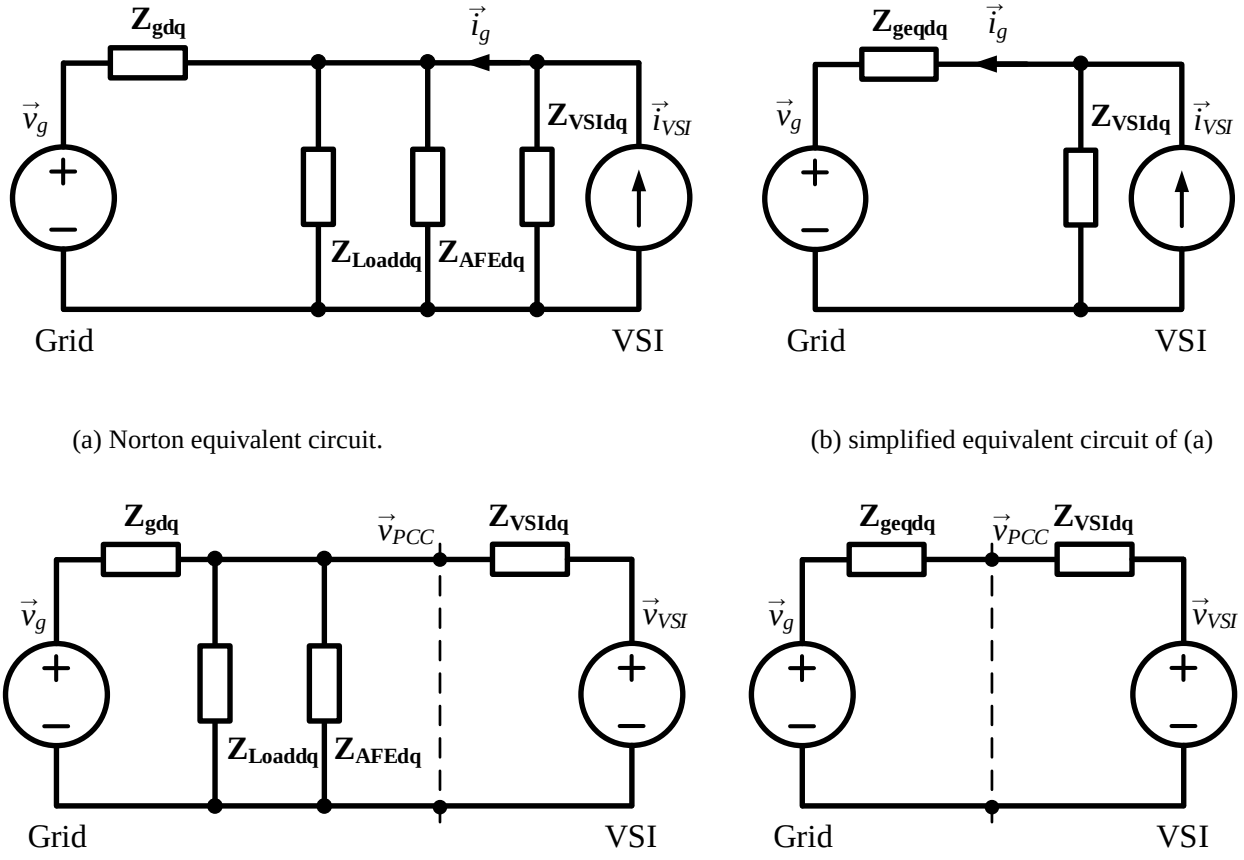
Let $\{l_1(s), l_2(s),\ldots,l_m(s)\}$ be the set of frequency-dependent eigenvalues of $\mathbf{L}(s)$, which trace in the complex plane the characteristic loci of matrix $\mathbf{L}(s)$ as the variable s traverses the standard Nyquist contour in the clockwise direction. Then the generalized Nyquist stability criterion can be formulated as:

"Let the multivariable system shown in Fig. 5-10 have no open-loop unobservable or uncontrollable modes whose corresponding characteristic frequencies lie in the right-half plane. Then the system will be closed-loop stable if and only if the net sum of anticlockwise encirclements of the critical point (–1+j0) by the set of characteristic loci of $\mathbf{L}(s)$ is equal to the total number of right-half plane poles of $\mathbf{Z}_{\mathbf{sdq}}(s)$ and $\mathbf{Z}_{\mathbf{ldq}}^{-1}(s)$."

The generalized inverse Nyquist stability criterion can be formulated as:

"Let the multivariable system shown in Fig. 5-10 have no open-loop unobservable or uncontrollable modes whose corresponding characteristic frequencies lie in the right-half plane. Then the system will be closed-loop stable if and only if the net sum of anticlockwise encirclements of the critical point (–1+j0) by the set of inverse characteristic loci (reciprocal of

each of the numbers $\{l_1(s), l_2(s),\ldots,l_m(s)\}$ in the complex plane) of $\mathbf{L}(s)$ is equal to the total number of right-half plane zeros of $\mathbf{Z}_{sdq}(s)$ and $\mathbf{Z}_{ldq}^{-1}(s)$."



(a) Norton equivalent circuit.

(b) simplified equivalent circuit of (a)

(c) Thévenin equivalent circuit.

(d) simplified equivalent circuit of (c)

Fig. 5-11. Small-signal representation of the system under study.

Impedance based stability analysis using GNC is verified by experiments to be an effective method to study the stability issue of balanced three-phase ac power system. In this paper, this analysis is implemented to study the low frequency synchronization instability shown in Fig. 5-6.

The system under study includes VSI working as current source. The most common equivalent circuit of VSI is an ideal current source parallel with its output impedance, as shown in Fig. 5-11 (a). Based on Fig. 5-11 (b), the output current of VSI is:

$$\vec{i}_g(s) = \mathbf{Z}_{\mathbf{geqdq}}^{-1}(s)\cdot\left(\mathbf{Z}_{\mathbf{VSIdq}}^{-1}(s)+\mathbf{Z}_{\mathbf{geqdq}}^{-1}(s)\right)^{-1}\cdot\vec{i}_{VSI}(s) - \left(\mathbf{Z}_{\mathbf{VSIdq}}(s)+\mathbf{Z}_{\mathbf{geqdq}}(s)\right)^{-1}\cdot\vec{v}_g(s) \tag{5-8}$$

and,

$$\mathbf{Z}_{\mathbf{geqdq}}(s) = \left(\mathbf{Z}_{\mathbf{Loaddq}}^{-1}(s)+\mathbf{Z}_{\mathbf{AFEdq}}^{-1}(s)+\mathbf{Z}_{\mathbf{gdq}}^{-1}(s)\right)^{-1} \tag{5-9}$$

Eq. (5-8) can be rearranged as:

$$\vec{i}_g(s) = \left(\mathbf{I}+\mathbf{Z}_{\mathbf{VSIdq}}^{-1}(s)\mathbf{Z}_{\mathbf{geqdq}}(s)\right)^{-1}\cdot\left(\vec{i}_{VSI}(s)-\mathbf{Z}_{\mathbf{VSIdq}}^{-1}(s)\cdot\vec{v}_g(s)\right) \tag{5-10}$$

$$\mathbf{L}_1(s) = \mathbf{Z}_{\mathbf{VSIdq}}^{-1}(s)\mathbf{Z}_{\mathbf{geqdq}}(s) \tag{5-11}$$

The condition for system stability can be determined by applying GNC or GINC to the minor loop gain $\mathbf{L_1}$.

Since any linear circuit can be also modeled using its Thévenin equivalent circuit, then VSI can also be modeled as ideal voltage source in series with its output impedances as shown in Fig. 5-11 (c). Based on Fig. 5-11 (d), the PCC voltage is:

$$\vec{v}_{PCC}(s) = \left(\mathbf{I}+\mathbf{Z}_{\mathbf{geqdq}}(s)\mathbf{Z}_{\mathbf{VSIdq}}^{-1}(s)\right)^{-1}\cdot\vec{v}_g(s) + \left(\mathbf{Z}_{\mathbf{VSIdq}}(s)\mathbf{Z}_{\mathbf{geqdq}}^{-1}(s)+\mathbf{I}\right)^{-1}\cdot\vec{v}_{VSI}(s) \tag{5-12}$$

$$\mathbf{L}_2(s) = \mathbf{Z}_{\mathbf{geqdq}}(s)\mathbf{Z}_{\mathbf{VSIdq}}^{-1}(s) \tag{5-13}$$

$$\mathbf{L}_3(s) = \mathbf{Z}_{\mathbf{VSIdq}}(s)\mathbf{Z}_{\mathbf{geqdq}}^{-1}(s) \tag{5-14}$$

The condition for system stability can be determined by applying GNC or GINC to the minor loop gain $\mathbf{L_2}$ and $\mathbf{L_3}$.

Since the eigenvalues of $\mathbf{L_1}$ are the eigenvalues of $\mathbf{L_2}$, then stability tests based on $\mathbf{L_1}$ and $\mathbf{L_2}$ are equivalent.

One can find that $\mathbf{L_2}$ is the inverse matrix of $\mathbf{L_3}$. Then eigenvalues of $\mathbf{L_2}$ are reciprocals of eigenvalues of $\mathbf{L_3}$. Since poles of $\mathbf{Z}_{\mathbf{geqdq}}$ are equal to the zeros of $\mathbf{Z}_{\mathbf{geqdq}}^{-1}$ [95], and same for $\mathbf{Z}_{\mathbf{VSIdq}}^{-1}$,

then system stability condition tested by applying GNC or GINC to $\mathbf{L_2}$ is the same by applying GINC or GNC to $\mathbf{L_3}$. Then stability tests base on $\mathbf{L_2}$ and $\mathbf{L_3}$ are equivalent.

5.4.1 Impedance of each components

i) Grid and passive load impedances

In this paper, the grid impedance is simply modeled as series-connected three-phase inductor and resistor. The grid impedance in *abc* frame is:

$$\begin{bmatrix} sL_g + R_g & 0 & 0 \\ 0 & sL_g + R_g & 0 \\ 0 & 0 & sL_g + R_g \end{bmatrix} \tag{5-15}$$

Let the grid angular frequency is ω_g, then in *d-q* frame the grid impedance is:

$$\mathbf{Z_{gdq}} = \begin{bmatrix} sL_g + R_g & -\omega_g L_g \\ \omega_g L_g & sL_g + R_g \end{bmatrix} \tag{5-16}$$

The passive load consists of parallel-connected three-phase capacitor and resistor. The capacitor impedance in *abc* frame is:

$$\begin{bmatrix} sC_{Load} & 0 & 0 \\ 0 & sC_{Load} & 0 \\ 0 & 0 & sC_{Load} \end{bmatrix} \tag{5-17}$$

In *d-q* frame the capacitor impedance is:

$$\mathbf{Z_{Cdq}} = \begin{bmatrix} sC_{Load} & -\omega_g C_{Load} \\ \omega_g C_{Load} & sC_{Load} \end{bmatrix}^{-1} \tag{5-18}$$

The load resistor impedance in *abc* frame is:

$$\begin{bmatrix} R_{Load} & 0 & 0 \\ 0 & R_{Load} & 0 \\ 0 & 0 & R_{Load} \end{bmatrix} \tag{5-19}$$

In *d-q* frame the resistor impedance is:

$$\mathbf{Z}_{\mathbf{Rdq}} = \begin{bmatrix} R_{Load} & 0 \\ 0 & R_{Load} \end{bmatrix} \tag{5-20}$$

The impedance of resistor parallel with capacitor is:

$$\mathbf{Z}_{\mathbf{Loaddq}} = \left(\mathbf{Z}_{\mathbf{Rdq}}^{-1} + \mathbf{Z}_{\mathbf{Cdq}}^{-1}\right)^{-1} \tag{5-21}$$

ii) AFE input impedances

Please check section 4.6 in chapter 4.

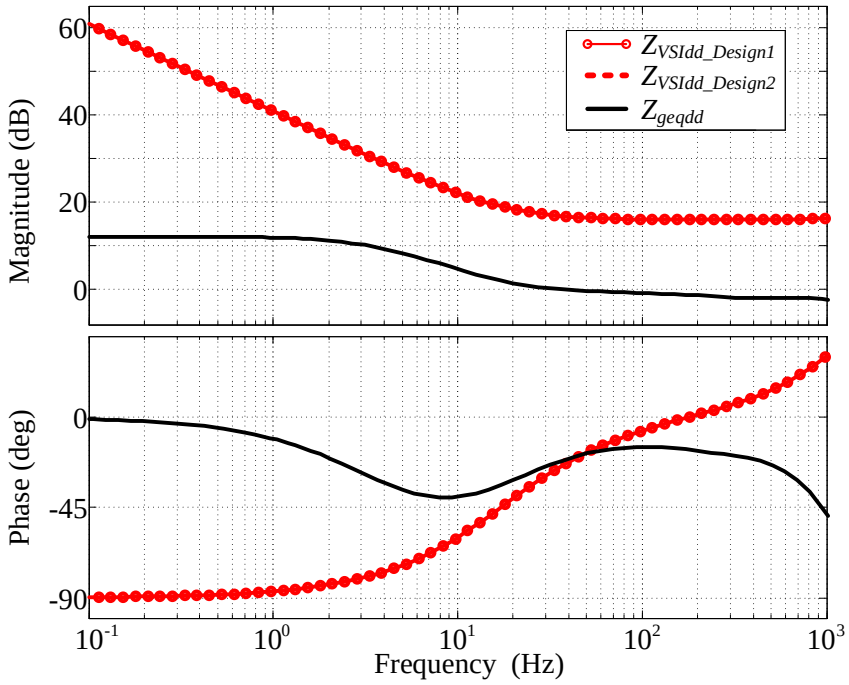
iii) VSI output impedances

Please check section 4.4 in chapter 4.

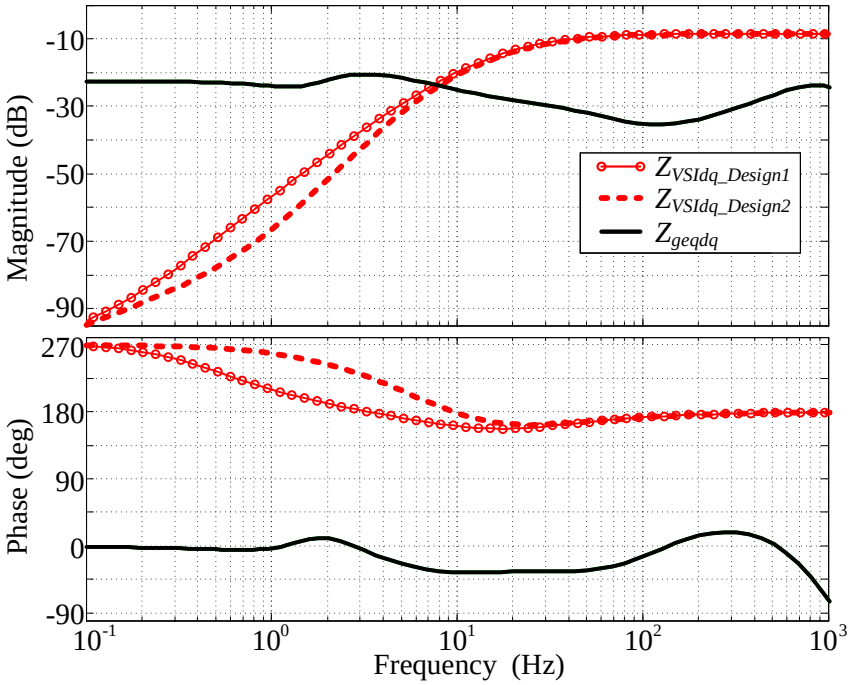
5.4.2 Stability analysis

In this section, system stability condition will be judged by applying GNC or GINC to $\mathbf{L_2}$ and $\mathbf{L_3}$. Both $\mathbf{L_2}$ and $\mathbf{L_3}$ are defined by $\mathbf{Z_{geqdq}}$ and $\mathbf{Z_{VSIdq}}$, they are calculated using the models discussed before and the system parameters in Table 5-1. Fig. 5-12 shows the Bode plots of $\mathbf{Z_{geqdq}}$ and $\mathbf{Z_{VSIdq}}$ for stable and unstable cases. From stable case to unstable case, the only change is VSI's PLL parameters. For stable case, VSI uses PLL *Design 1* as shown in Fig. 5-4 (a); for unstable case, VSI uses PLL *Design 2* in Fig. 5-4 (a). As a result, Z_{dd} of VSI for both cases are the same, they are over 10 dB bigger than the grid side equivalent impedance. Z_{qq} of VSI is shaped as negative resistance at low frequency. Since VSI uses PLL *Design 2* that has higher bandwidth than *Design 1* as indicated by Fig. 5-4 (a) in unstable case, Z_{qq} of VSI for unstable case ($Z_{VSIqq\_Design2}$) has wider frequency range of negative resistance behavior. On the other hand, PLL *Design 2* has less phase margin than *Design 1* (see Fig. 5-4 (a)), $Z_{VSIqq\_Design2}$ has a resonance between 1Hz to 10 Hz that makes $Z_{VSIqq\_Design2}$ interacting with grid side impedance Z_{geqqq} and the phase difference over 180 °, which makes the system unstable. Although different PLL parameters make changes on Z_{dq} and Z_{qd} for VSI, these changes can be ignored. This is because for both VSI and grid side impedances, Z_{dq} and Z_{qd} are more than 10 dB smaller compare to Z_{dd} and Z_{qq}, the system under study is diagonal dominant. Eigenvalues of minor loop-

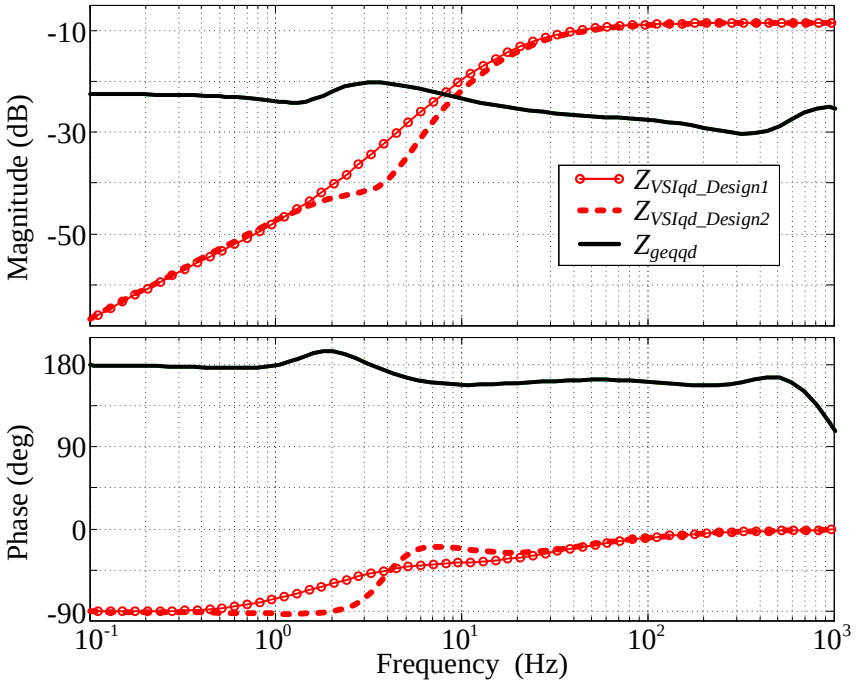
gains ($\mathbf{L}_2$ and $\mathbf{L}_3$) are mainly determined by impedance ratios of *d* channel (Z_{geqdd}/Z_{VSIdd}) and *q* channel (Z_{geqqq}/Z_{VSIqq}) [72] [43].



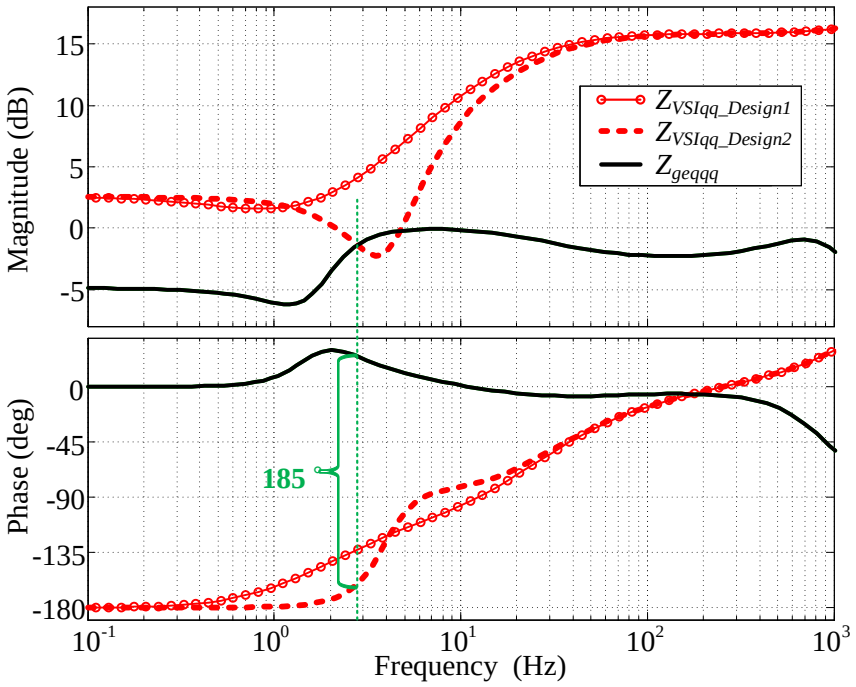
(a)



(b)


Magnitude (dB)
-10
-30
-50
$Z_{VSIqd\_Design1}$
$Z_{VSIqd\_Design2}$
Z_{geqqd}
Phase (deg)
180
90
0
-90
10^{-1}
10^{0}
10^{1}
10^{2}
10^{3}
Frequency (Hz)

(c)


Magnitude (dB)
15
10
5
0
-5
$Z_{VSIqq\_Design1}$
$Z_{VSIqq\_Design2}$
Z_{geqqq}
Phase (deg)
0
-45
-90
-135
-180
185
10^{-1}
10^{0}
10^{1}
10^{2}
10^{3}
Frequency (Hz)

(d)

Fig. 5-12. Grid and VSI impedances for PLL *Design 1* and *Design 2*.

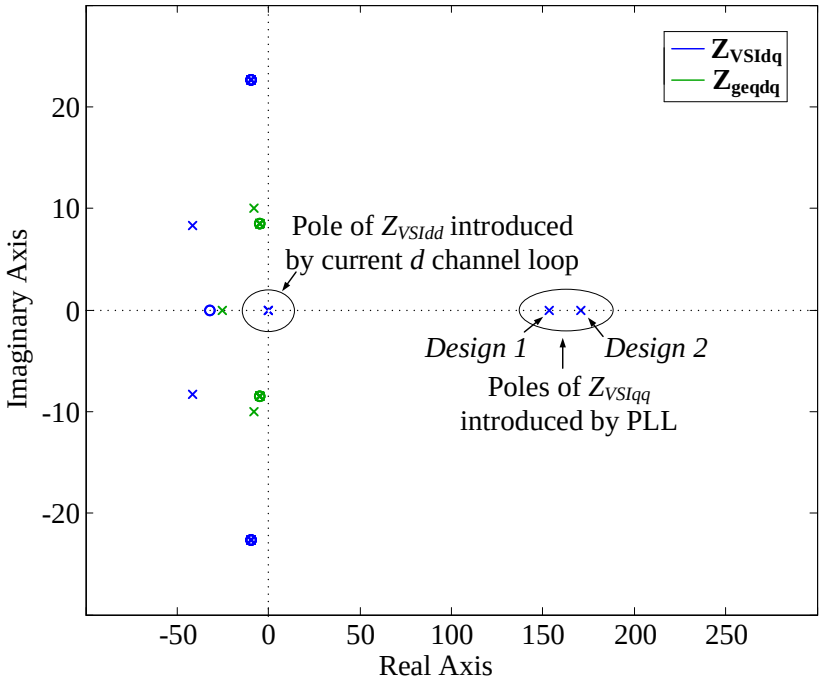


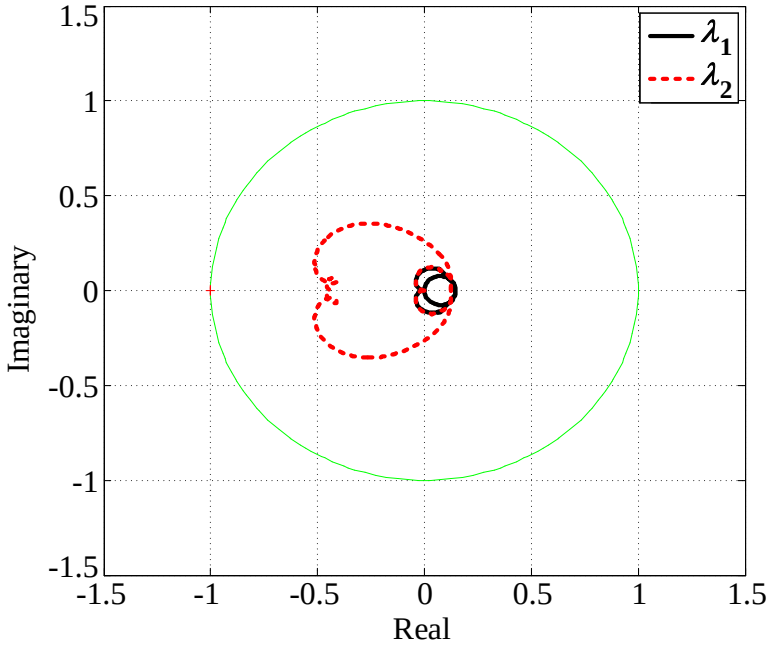
Fig. 5-13. Pole-zero map of VSI ($\mathbf{Z_{VSIdq}}$) and grid side impedances ($\mathbf{Z_{geqdq}}$).

Before applying GNC to study the stability of the system, it is necessary to check the poles and zeros of grid and VSI impedances, since stability condition of the system also rely on the number of poles and zeros on the right-half plane (RHP).

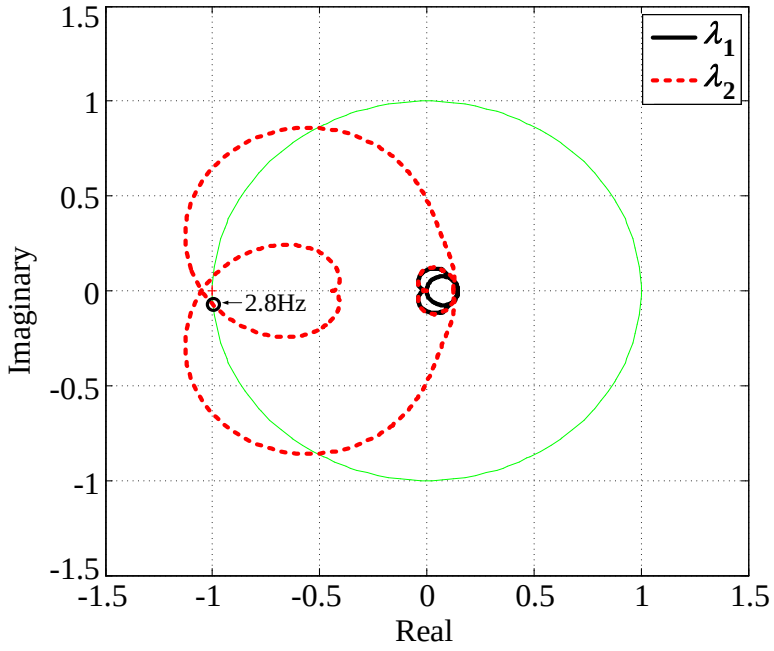
Fig. 5-13 is the pole-zero map of VSI and grid side impedances, which shows that there is no pole and zero of grid side impedance ($\mathbf{Z_{geqdq}}$) locates on RHP. For VSI impedances, there is one pole at the origin and one pole on the positive real axis. The pole at the origin is introduced by the *d* channel current feedback control. Reflecting to the Bode plot of Z_{VSIdd}, this pole gives 20dB/dec decreasing of magnitude and -90 °phase (see Fig. 5-12 (a)). PLL of VSI introduces the pole on the positive real axis. Reflecting to the Bode plot of Z_{VSIqq}, this pole makes the magnitude decreasing while the phase increasing at the low frequency range (see Fig. 5-12 (d)).

As discussed before, the condition for system stability can be determined by applying GNC or GINC to the minor loop gain $\mathbf{L_2}$ and $\mathbf{L_3}$. For $\mathbf{L_2}$, which is defined by $\mathbf{Z}_{\mathbf{geqdq}}$ and $\mathbf{Z}^{-1}_{\mathbf{VSIdq}}$, it is easier to test stability by applying GNC rather than GINC. Because there is no pole from $\mathbf{Z_{geqdq}}$ locates

on RHP, and the same for $\mathbf{Z}_{VSIdq}^{-1}$, since all the poles of $\mathbf{Z}_{VSIdq}$ will become zeros of $\mathbf{Z}_{VSIdq}^{-1}$ [43]. To judge the stability condition of the system, one can simply find whether the eigenvalue loci of $\mathbf{L_2}$ encircles the critical point (-1 + j0) or not. Fig. 5-14 shows the characteristic loci of $\mathbf{L_2}$, When VSI uses PLL *Design 1*, characteristic loci of $\mathbf{L_2}$ do not encircle (-1 + j0) point, the system is stable. When VSI uses PLL *Design 2*, characteristic loci of $\mathbf{L_2}$ encircle (-1 + j0) point, the system is unstable. These conclusions matches with the time domain simulations results shown in Fig. 5-6.

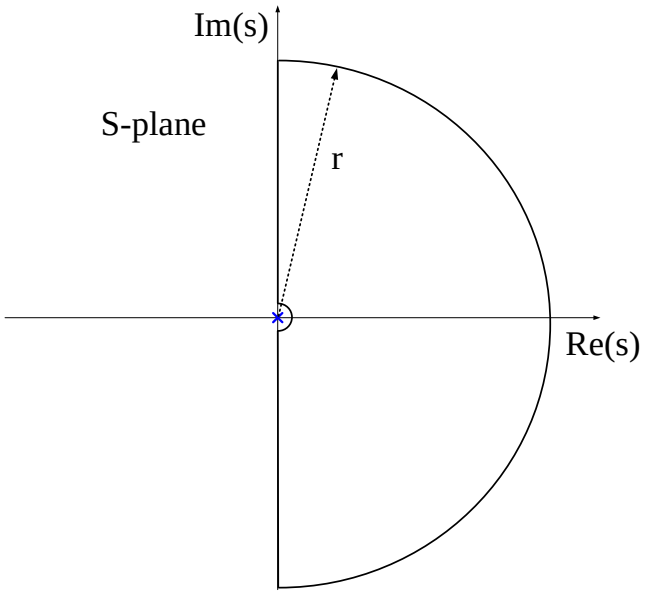


(a)

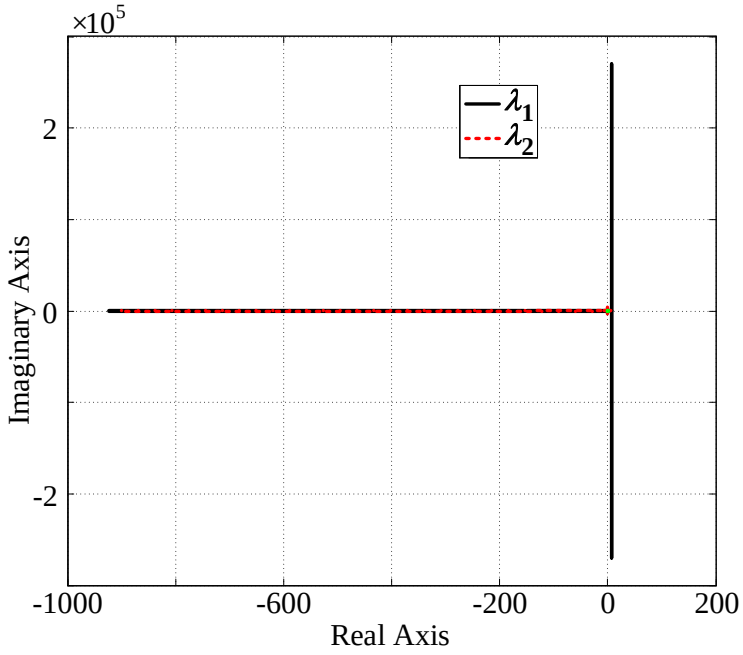


(b)

Fig. 5-14. Characteristic loci of $\mathbf{L}_2$ (a) VSI with *Design 1*; (b) VSI with *Design 2*.



(a)



(b)

Fig. 5-15. (a) Standard D contour for $\mathbf{L_3}$; (b):Characteristic loci of $\mathbf{L_3}$.

For $\mathbf{L_3}$, which is defined by $\mathbf{Z}_{\mathbf{VSIdq}}$ and $\mathbf{Z}_{\mathbf{geqdq}}^{-1}$, it is easier to test stability by applying GINC rather than GNC. Since, although there is no pole from $\mathbf{Z}_{\mathbf{geqdq}}^{-1}$ locates on RHP, $\mathbf{Z}_{\mathbf{VSIdq}}$ has one pole at the origin and one pole on the RHP as discussed before. Standard contour for s must avoid the pole at origin, which makes the eigenvalue loci travels to infinity (see Fig. 5-15). On the other hand, because of the RHP pole, one have to count the number of encirclement of the (-1 + j0) point by the eigenvalue loci. All these features make the use of GNC to $\mathbf{L_3}$ difficult. Notice that, there is no RHP zero from the system, the stability condition of the system can be simply judged by checking whether the inverse characteristic loci of $\mathbf{L_3}$ encircles the critical point (-1 + j0) or not. Recall that inverse characteristic loci of $\mathbf{L_3}$ are the reciprocal of eigenvalue loci of $\mathbf{L_3}$, which are also the characteristic loci of $\mathbf{L_2}$ since $\mathbf{L_3}$ is the inverse matrix of $\mathbf{L_2}$. Then Fig. 5-14 is also the inverse characteristic loci plots of $\mathbf{L_3}$. The stability conclusions from using GINC to $\mathbf{L_3}$ also matches from the time domain simulation, which also proved the equivalence of using $\mathbf{L_2}$ and $\mathbf{L_3}$ for system stability study.

5.4.3 Migration of synchronization instability

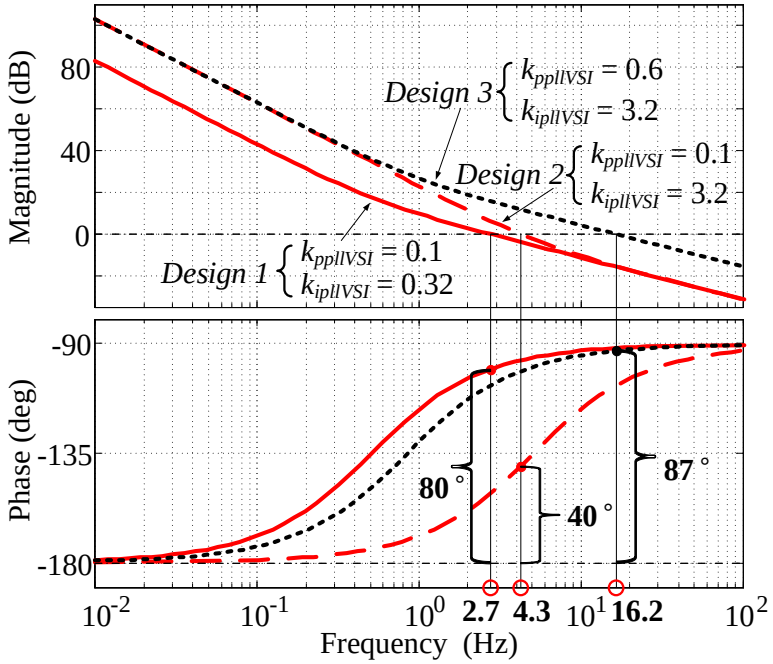
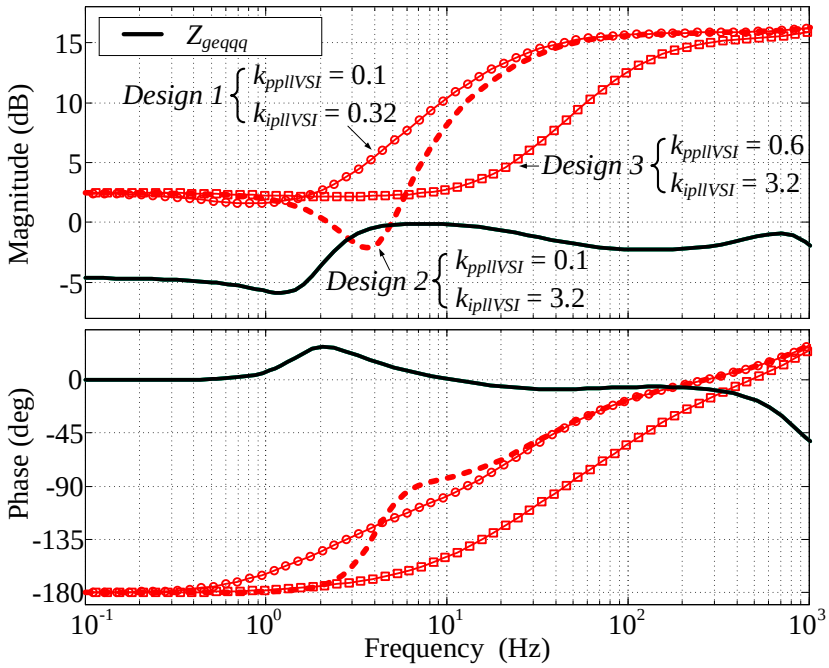
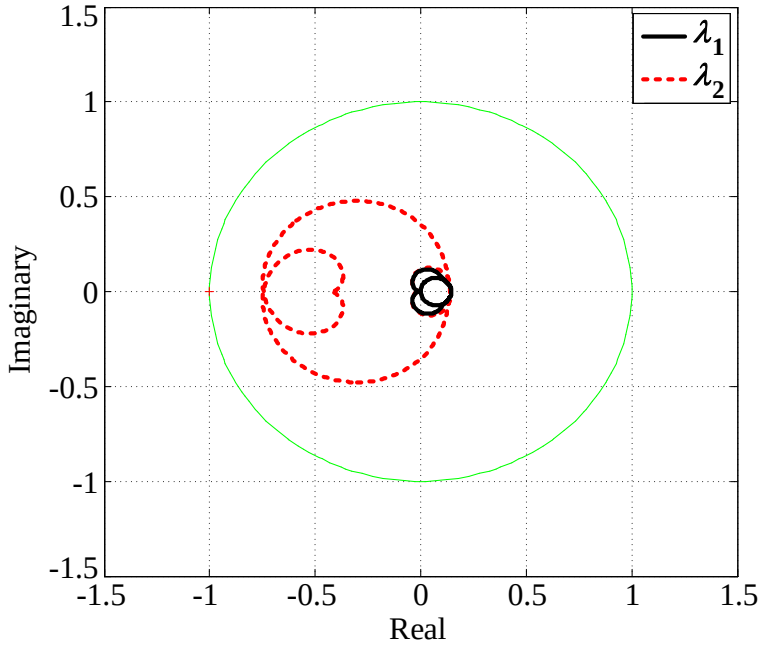


Fig. 5-16. VSI PLL loop gains with different PI parameters and ideal grid.

As discussed in the stability analysis section, when VSI uses PLL *Design 2*, which has bigger bandwidth and less phase margin comparing to *Design 1*, Z_{qq} of VSI (Z_{VSIqq}) and the grid (Z_{geqqq}) interacts with each other and the phase difference is over 180 °(see Fig. 5-12 (d)), and system is unstable. In order to migrate the instability, one can simply reduce the PLL bandwidth and adopt *Design 1*, which makes no interaction between Z_{VSIqq} and Z_{geqqq}. However, instability can also be migrated by increasing the phase margin of PLL while still keep higher bandwidth, for example using PLL *Design 3* as shown in Fig. 5-16. Fig. 5-17 (a) shows the Z_{qq} of VSI using three PLL designs. Same as using *Design 1*, Z_{VSIqq} using PLL *Design 3* do not interact with the grid side impedance. Fig. 5-17 (b) shows the characteristic loci of $\mathbf{L}_2$ when VSI uses PLL *Design 3*, which indicate the system is stable with VSI using PLL *Design 3*. Simulation results in time domain shown in Fig. 5-18 also verify the conclusion.

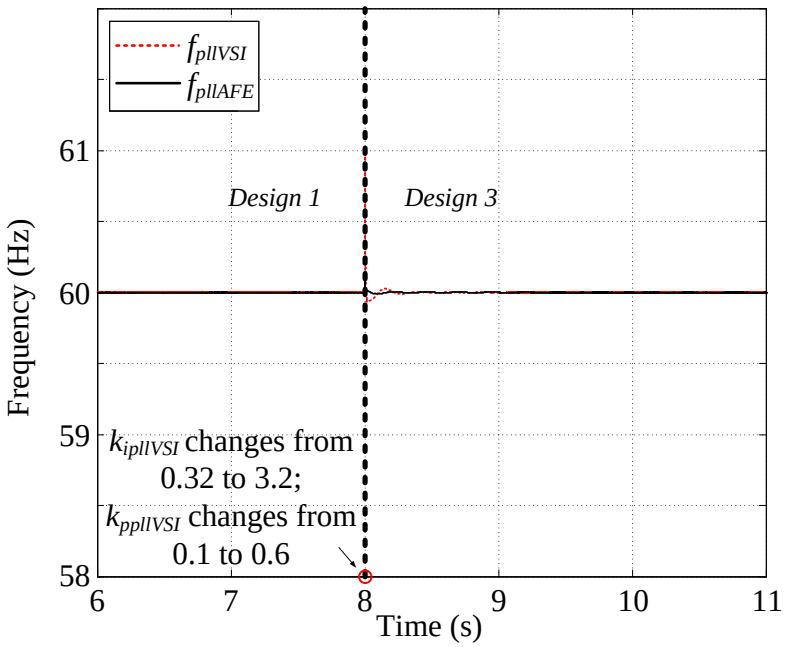


(a)

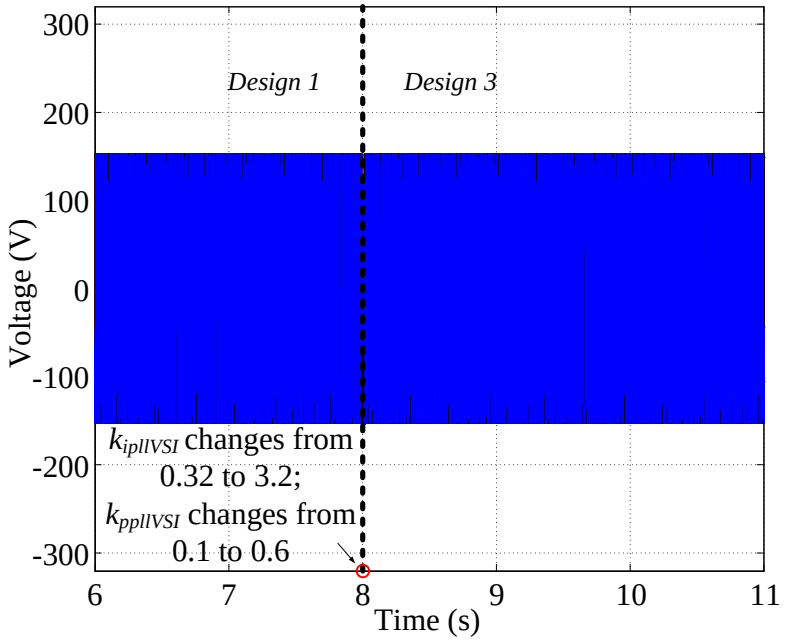


(b)

Fig. 5-17. (a) Z_{qq} of grid side and VSI; (b) characteristic loci of $\mathbf{L}_2$ with *Design 3*.



(a)



(b)

Fig. 5-18. (a) PLLs' output frequencies with *Design 3*; (b) PCC voltages with *Design 3*.

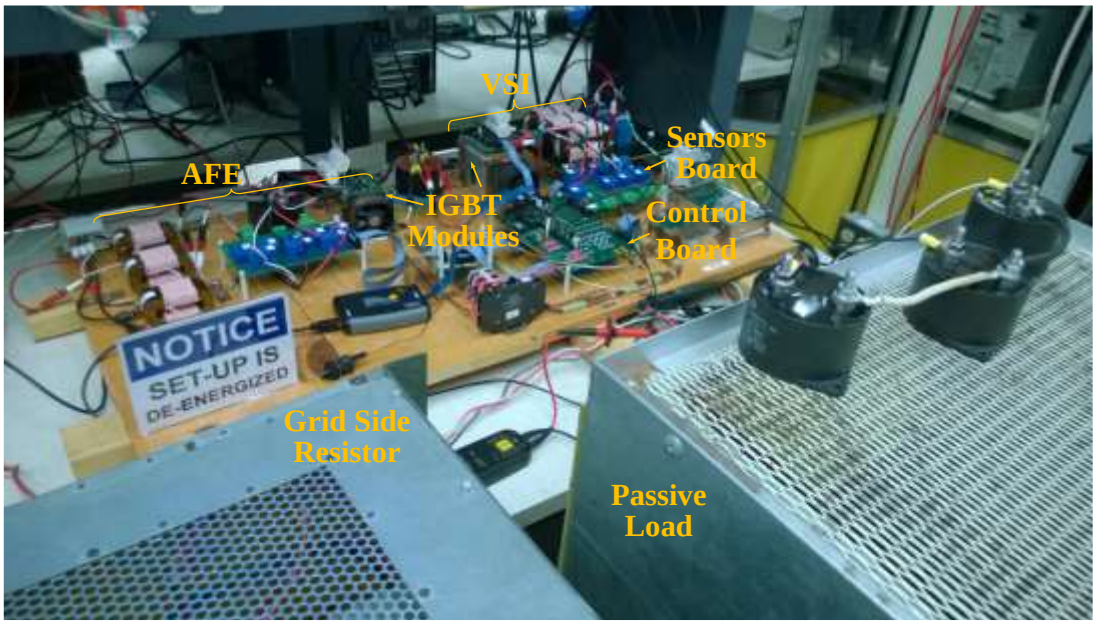
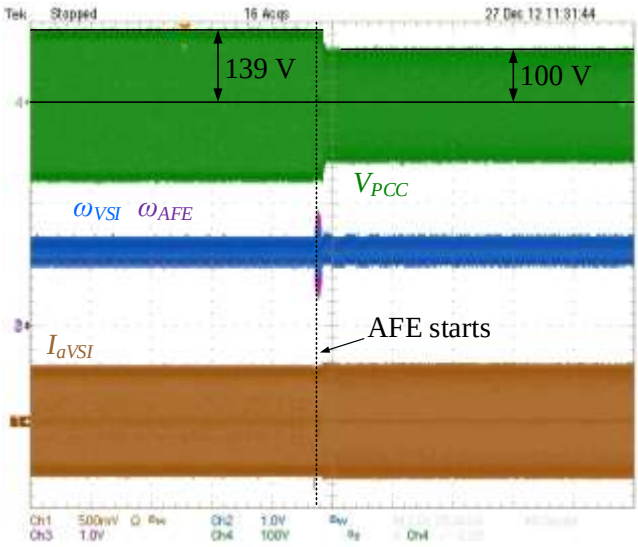


Fig. 5-19. Test-bed hardware prototype for experimental system

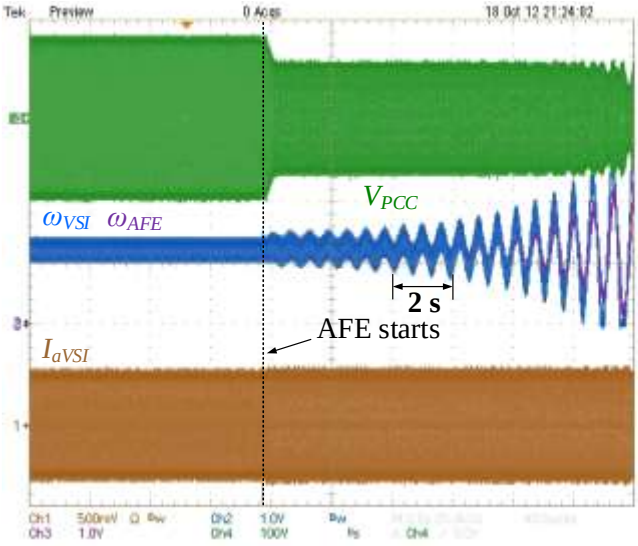
5.5 Experimental Results

A low power test-bed hardware prototype (Fig. 5-19) of system shown in Fig. 5-1 is built in the laboratory to verify the proposed analysis. Table 5-2 gives the parameters of the test-bed hardware.

In the experiment, VSI is started first, and then AFE is started. Two experiments are shown. In the first experiment, VSI and AFE work stably with the weak grid and passive load (Fig. 5-20 (a)). In the second one, the system is unstable (Fig. 5-20 (b)). From stable to unstable test, only PLL parameters of VSI and AFE are changed.

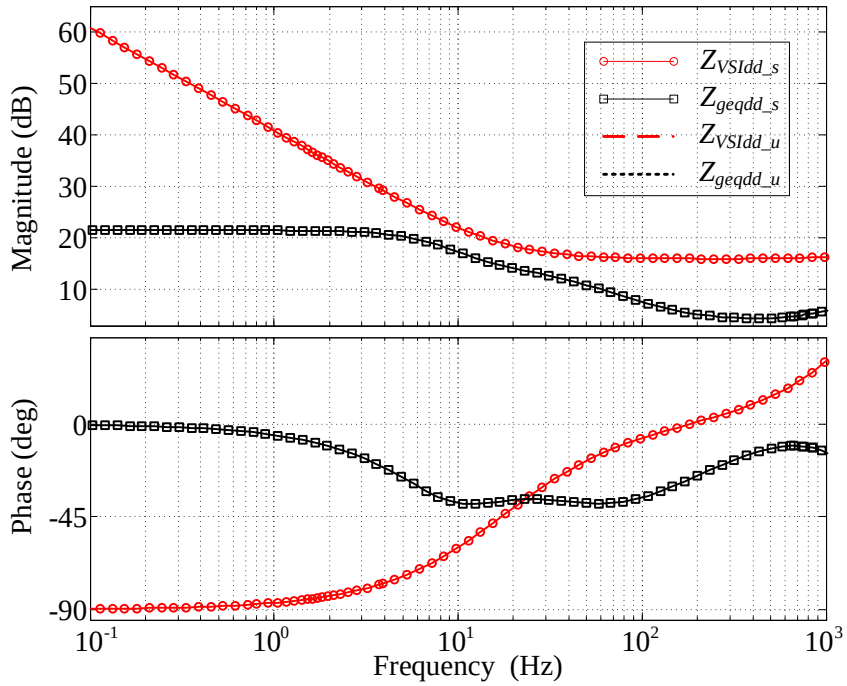


(a) Stable case. V_{PCC} [100 V/DIV], I_{aVSI} [10 A/DIV], ω_{VSI}, ω_{AFE} [0.05 Hz/DIV]

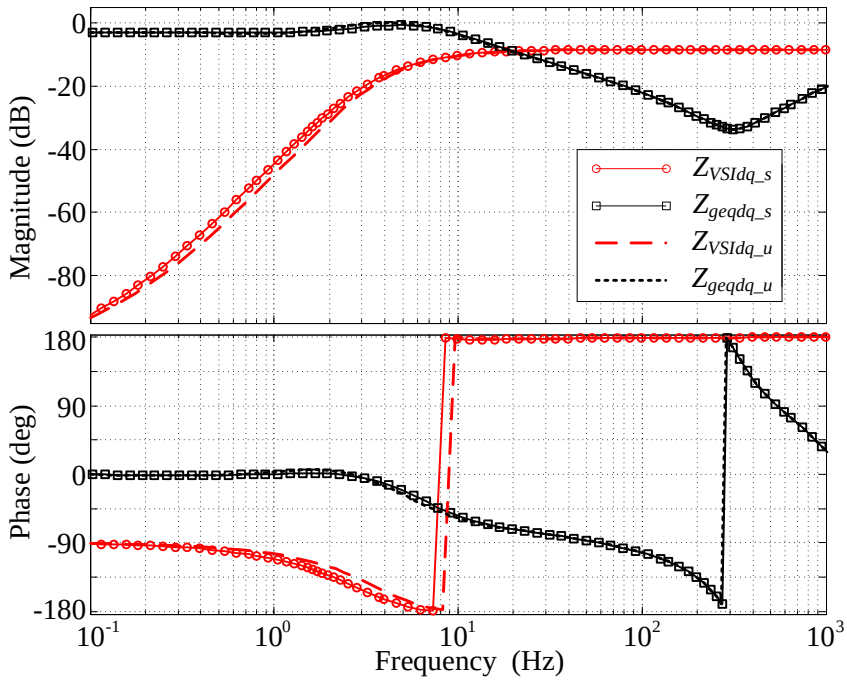


(b) Unstable case. V_{PCC} [100 V/DIV], I_{aVSI} [10 A/DIV], ω_{VSI}, ω_{AFE} [0.05 Hz/DIV]

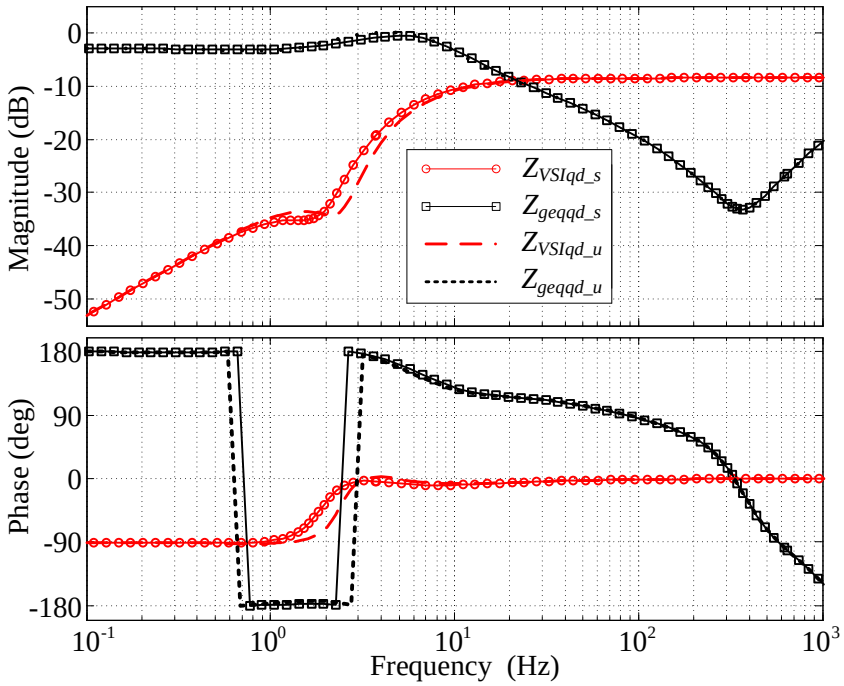
Fig. 5-20. Experimental test results.


Magnitude (dB)
60
50
40
30
20
10
Z_{VSIdd_s}
Z_{geqdd_s}
Z_{VSIdd_u}
Z_{geqdd_u}
Phase (deg)
0
-45
-90
10^{-1}
10^{0}
10^{1}
10^{2}
10^{3}
Frequency (Hz)

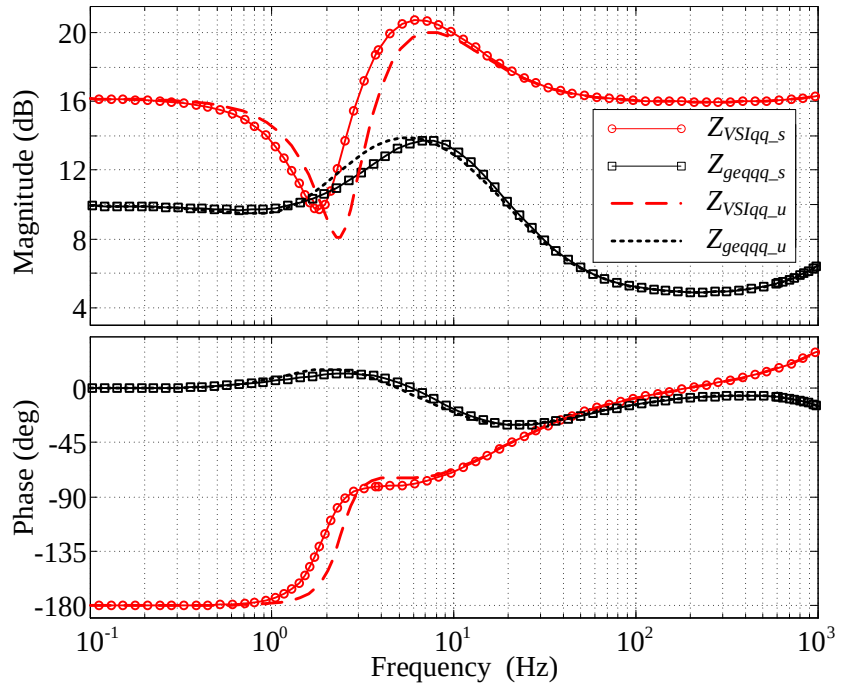
(a)


Magnitude (dB)
0
-20
-40
-60
-80
Z_{VSIdq_s}
Z_{geqdq_s}
Z_{VSIdq_u}
Z_{geqdq_u}
Phase (deg)
180
90
0
-90
-180
10^{-1}
10^{0}
10^{1}
10^{2}
10^{3}
Frequency (Hz)

(b)



(a)



(d)

Fig. 5-21. Grid and VSI impedances for stable and unstable cases.

Using the models in section 5.4 and the parameters in Table 5-2, impedances of VSI and grid are calculated for the experimental systems. They are shown in Fig. 5-21. As a result, the experimental system is diagonal dominant. Because, for both VSI and grid side impedances, Z_{dq} and Z_{qd} are more than 10 dB smaller compare to Z_{dd} and Z_{qq}. Eigenvalues of minor loop-gains (**L**$_2$ and **L**$_3$) are mainly determined by impedance ratios of *d* channel (Z_{geqdd}/Z_{VSIdd}) and *q* channel (Z_{geqqq}/Z_{VSIqq}), Z_{dq} and Z_{qd} can be ignored. Changes of PLL parameters changes Z_{qq}. As Fig. 5-22 shows, although for both stable and unstable condition, Z_{VSIqq} interacts with Z_{geqqq}, stable case has nearly 30 °phase margin while the unstable case has no phase margin.

Table 5-2. Parameters of experimental system

Symbol	Description	Value
V_g	Grid phase-neutral peak voltage	$60\sqrt{2}$ V
f_g	Grid voltage frequency	60 Hz
L_{VSI}	Inductance of inverter	1 mH
V_{dcVSI}	Inverter dc voltage	270 V
f_{sw}	Switching frequency of VSI and AFE	20 kHz
$I_{drefVSI}$	*d* channel current of VSI	11 A
$I_{qrefVSI}$	*q* channel current of VSI	0 A
k_{piVSI}	Proportional gain of VSI current controller	0.0233
k_{iiVSI}	Integrator gain of VSI current controller	2.560
$k_{ppllVSI}$	Proportional gain of VSI PLL	0.1
$k_{ipllVSI}$	Integral gain of VSI PLL	3.2 (unstable); 2 (stable)
L_{AFE}	Inductance of AFE	0.5 mH
C_{dcAFE}	Dc link capacitor of AFE	100 μF
R_{dc}	Load resistor of AFE	96 Ω
V_{dcAFE}	Dc voltage of AFE	231 V
k_{piAFE}	Proportional gain of AFE current controller	0.0116
k_{iiAFE}	Integrator gain of AFE current controller	2.5598
k_{pvAFE}	Proportional gain of AFE voltage controller	0.0628
k_{ivAFE}	Integrator gain of AFE voltage controller	6.9813

$k_{ppllAFE}$	Proportional gain of AFE PLL	0.2 (unstable); 0.3 (stable)
$k_{ipllAFE}$	Integral gain AFE of PLL	1
Z_L	Local passive load	R_{Load}: 10 Ω; C_{Load}: 50 μF
Z_g	Grid impedance	10 Ω

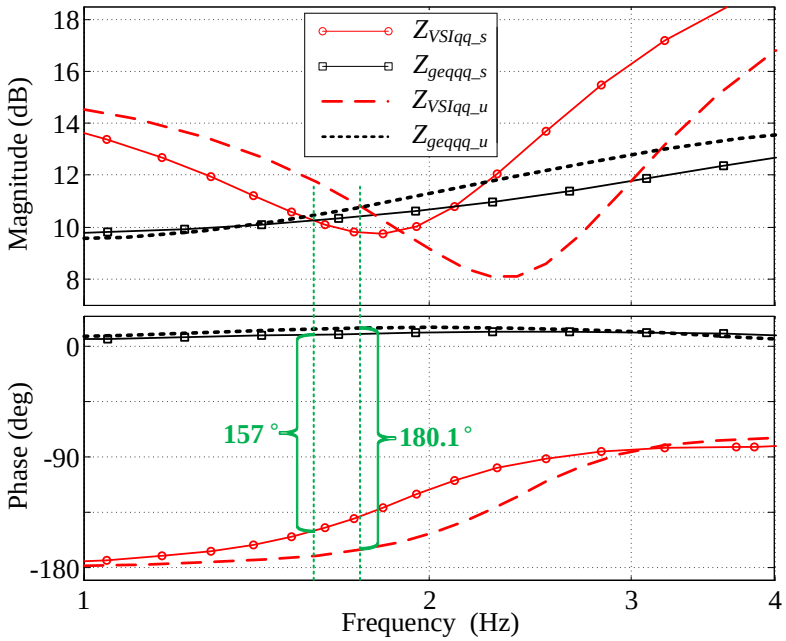
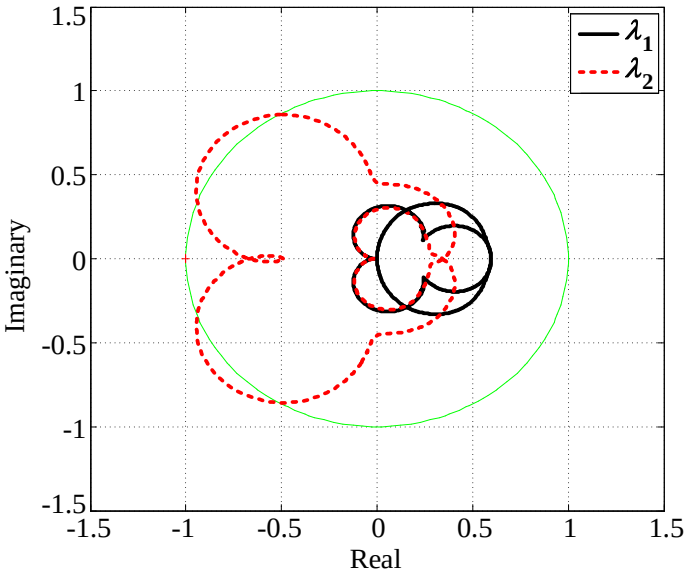
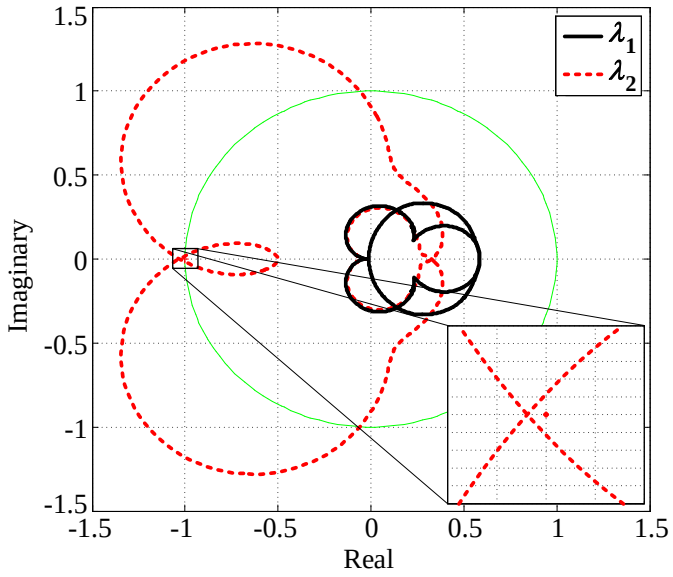


Fig. 5-22. Z_{qq} of grid and VSI for stable and unstable cases.



(a)



(b)

Fig. 5-23. Characteristic loci of $\mathbf{L}_2$ (a) VSI with *Design 1*; (b) VSI with *Design 2*.

Fig. 5-23 shows the characteristic loci of $\mathbf{L}_2$ which defined by the impedances of experimental system. By applying GNC to $\mathbf{L}_2$, stability condition of the experimental system can be predicted accurately.

This paper proposes an impedance-based analysis method to analyze the grid-synchronization stability issue in paralleled three-phase converter systems including grid-tied inverter, active front end rectifier, local passive load, and grid impedance. The proposed method shows that the multi-variable generalized Nyquist stability criterion (GNC) and generalized inverse Nyquist stability criterion (GINC) can be used to predict the system stability based on the grid and inverter impedances in the synchronous *d-q* frame. Furthermore, the instability is found to be caused by *qq* channel impedance interaction. Experimental results verify the analysis and the proposed method.

Chapter 6 Impedance-based Analysis of Islanding Dection for Grid-tied Inverter Systems

Islanding detection is an important function of distributed generation units because of the requirement of grid code compliance [96]. On the other hand, islanding detection function gives distributed generation unit the capability of adjusting its operation mode according to grid condition. For example, the three-phase inverter, as shown in Fig. 6-1, can work as a current source when it is connected to the grid. It can work as a voltage source to feed the local load (islanding mode) when it is disconnected with grid because of grid faults.

Many islanding detection methods have been developed. Methods that rely on monitoring the changes of grid parameters are defined as passive methods. For example, over/under voltage or frequency detection. Methods generate small perturbations to force the change of grid parameters are defined as active methods. For example, active frequency drift (AFD) islanding detection method forces frequency drifts enough to activate over/under frequency protection when islanding condition happens. Other active methods include grid impedance estimation and negative sequence detection [90]. Among them, AFD methods are popular because of their simplicity, small non-detection zone, and low impact on system power quality. Most AFD methods generate a frequency positive feedback, such as the Sandia frequency shift (SFS) method, which drives the converter system frequency away from the steady-state and detects the islanding event [97]–[101]. Other methods are based on the analysis of PLL small-signal stability [102].

Different from traditional analysis of AFD method, this paper proposes an impedance-based analysis which unveils that frequency drift is the consequence of interaction between inverter output impedance and the impedance of local loads. Moreover, impedance-based analysis also shows that, AFD method has the potential to destabilize the grid-connected inverter system when the grid is week or the size of inverter is large.

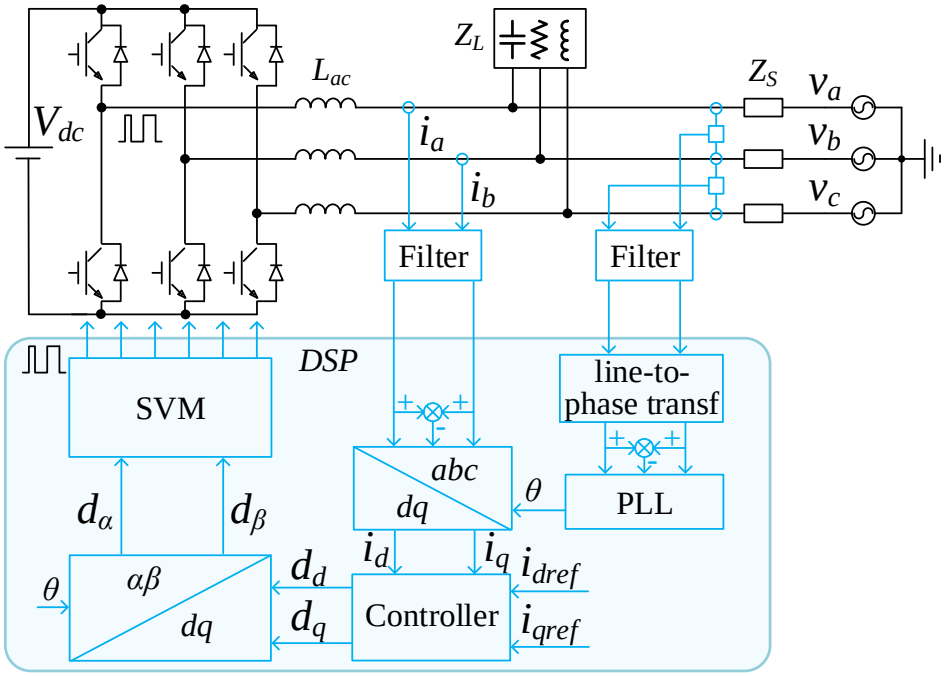


Fig. 6-1. Three-phase grid-tied PWM inverter system.

6.1 AFD Islanding Detection Methods

In this section, the principles of two AFD islanding detection methods are discussed.

6.1.1 PLL-Based Method

The PLL-based AFD islanding detection method [102] is shown in Fig. 6-2. This method uses a typical rotating reference frame PLL scheme with a small-signal feed-forward loop.

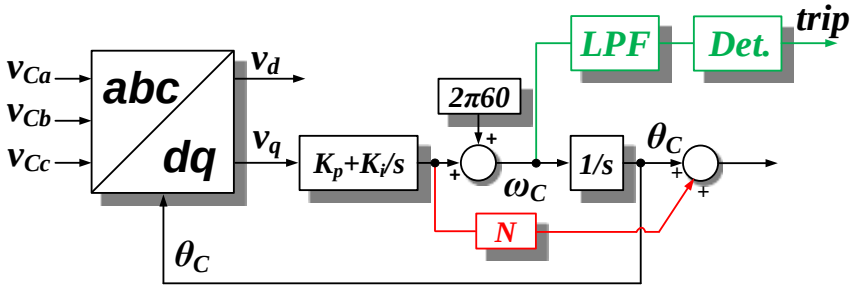


Fig. 6-2. PLL-based AFD islanding detection method.

Under islanding condition, inverter is controlled as a current source feeding to the local load, as shown in Fig. 6-3. The terminal voltage v_c of inverter is determined by the current injected to the load and the impedance of the load. This voltage is collected by inverter for PLL to generate frequency and angle to do current control, as shown in Fig. 6-4. In another word, under islanding condition, inverter is synchronized with the voltage generated by itself. By adjusting the value of N, the pole of PLL can be moved from left half plane to right half plane. When PLL has right half plane pole, it becomes unstable, the output frequency drift away from steady-state value, the bigger the N value is the faster the drift speed is. Islanding event can be detected by over or under frequency detection function of the inverter. Detailed analysis can be found in [102]. This method features a small impact to the inverter system operation as well as an easy implementation.

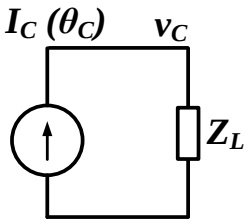


Fig. 6-3. One line circuit of inverter system under islanding condition.

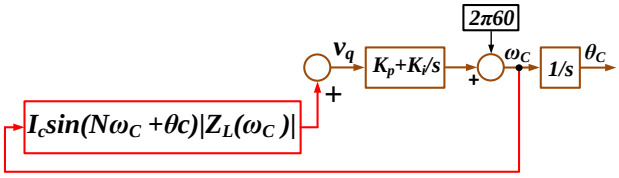


Fig. 6-4.PLL model under islanding condition.

6.1.2 SFS Method

SFS method is one of the positive feedback anti-islanding method. The details of the SFS method can be found from [102], [103] where the inverter reference currents i_{dref} and i_{qref} are processed by a phase angle transformation block to get the new current reference settings i^*_{dref} and i^*_{qref}. The definition of the transformation and the phase angle are:

$$\begin{bmatrix} i^*_{dref} \\ i^*_{qref} \end{bmatrix} = \begin{bmatrix} \cos\theta_f & -\sin\theta_f \\ \sin\theta_f & \cos\theta_f \end{bmatrix} \cdot \begin{bmatrix} i_{dref} \\ i_{qref} \end{bmatrix} \tag{6-1}$$

$$\theta_f = \frac{\pi}{2}\left(cf_0 + K(\omega - \omega_0)\right) \tag{6-2}$$

The angle θ_f used in the transformation block is calculated from the SFS control, in which ω is the inverter terminal voltage frequency, ω_0 is the grid nominal frequency, K is the positive feedback gain, and cf_0 is the initial chopping factor. [9]

Positive feedback always tries to perturb the grid-tied inverter system. When the grid is connected, the system is operated stably. However, when islanding event happens, the system is destabilized so that the frequency drift detection unit is tripped.

6.2 Impedance-Based Analysis of Inverter System AFD Methods

Unlike most analyses for AFD islanding detection methods, this paper presents an impedance-based analysis which uses the terminal characteristics of inverter and loads. The advantages of impedance-based analysis is that impedance can be measured, no internal parameters of the inverter are need, and it is easier to address compatibility issue between inverter and the grid by using impedances and Nyquist stability criteria.

Grid-tied inverter can be modeled as a voltage source in series with an output impedance as shown in Fig. 6-5. Impedance-based analysis studies the islanding event by the interaction between the output impedance of inverter and the input impedance of local load. When the system is connected to the grid, the grid impedance should be considered too; for a stiff grid, the impedance is small, for a weak grid, the impedance is big.

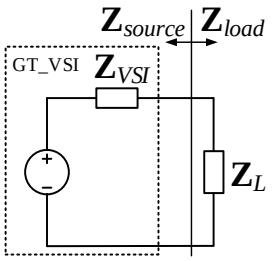


Fig. 6-5. Impedance-based analysis of inverter system under islanding condition.

6.2.1 Impedance of local load

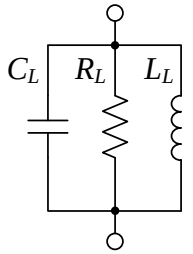


Fig. 6-6. Load configuration for unintentional islanding test.

Fig. 6-6 shows the local load configuration (for one line) for unintentional islanding test defined by [96], R_L is equal to 1 pu value of the inverter, which means the real power needed by the resistor is provided only by the inverter. The Q factor of the circuit is equal to 1.0 ± 0.05, when it is equal to 1, the reactive power needed by L_L and C_L are equal to real power provide by the inverter.

6.2.2 Output impedance of inverter with AFD method

Fig. 6-7 shows the average model of grid-tied inverter with PLL-based AFD method discussed in section 6.1. Notice that the inverter system is divided into two parts, one is in the system *d-q* domain, and one is in the converter or control system *d-q* domain. The system domain is defined by the grid voltage, while the converter domain is defined by the PLL, which tracks the frequency and angle of the grid voltage to find the position of system domain. In steady-state, the converter domain is aligned with the system domain. When the grid voltage

contains small-signal perturbations, which means the system domain is changing, the converter domain is no longer aligned with the system domain because of the PLL dynamics (PI of PLL).

In effect, small-signal perturbations of the system voltage propagate to the PLL output angle, and further to the converter domain current. Through the current controller, the perturbation propagates to the duty ratio and the voltage generated by the inverter power stage and finally to the output current of the inverter. This analysis indicates that the PLL has an impact on the output impedance of the grid-tied inverter.

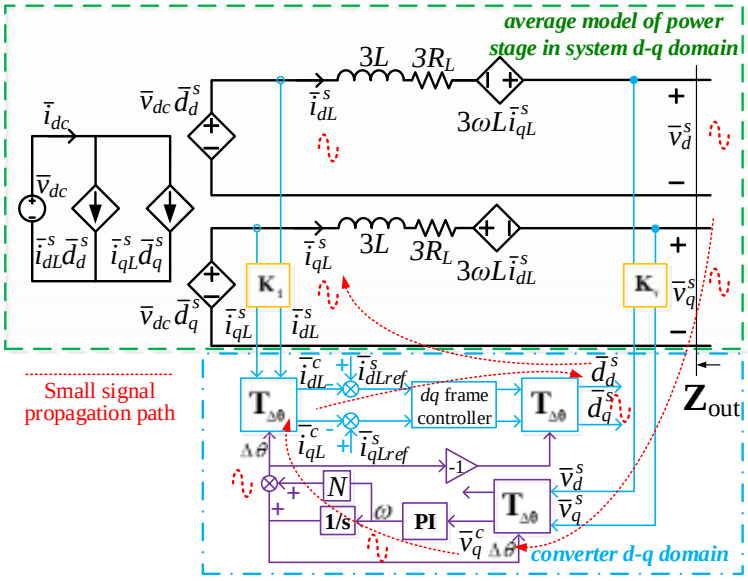


Fig. 6-7. Average model of grid-tied inverter with AFD method.

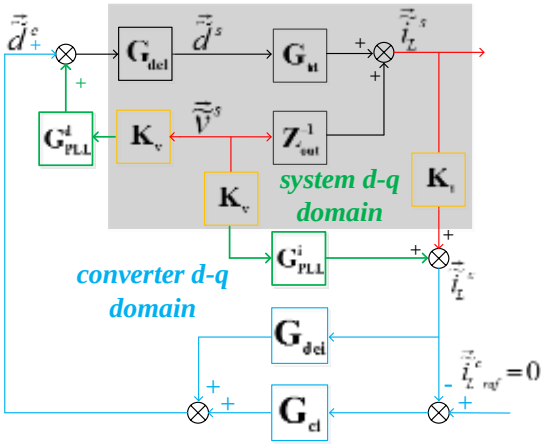


Fig. 6-8. Inverter small-signal model with PLL-based AFD method.

Fig. 6-8 shows the transfer function matrix flow chart representation of grid-tied inverter small-signal model with PLL-based AFD method and current feedback control. $\mathbf{G}_{\mathbf{id}}$ is the transfer function matrix from duty ratio $\tilde{\vec{d}}^{\,s}$ to inductor current $\tilde{\vec{i}}_L^{\,s}$, $\mathbf{Z}_{\mathbf{out}}$ is the open loop output impedance which can be derived using the small-signal circuit shown in Fig. 6-9, and the expression is:

$$\mathbf{Z}_{\mathbf{out}} = \begin{bmatrix} Z_{dd} & Z_{dq} \\ Z_{qd} & Z_{qq} \end{bmatrix} = \begin{bmatrix} 3Ls + 3R_L & -3\omega L \\ 3\omega L & 3Ls + 3R_L \end{bmatrix} \tag{6-3}$$

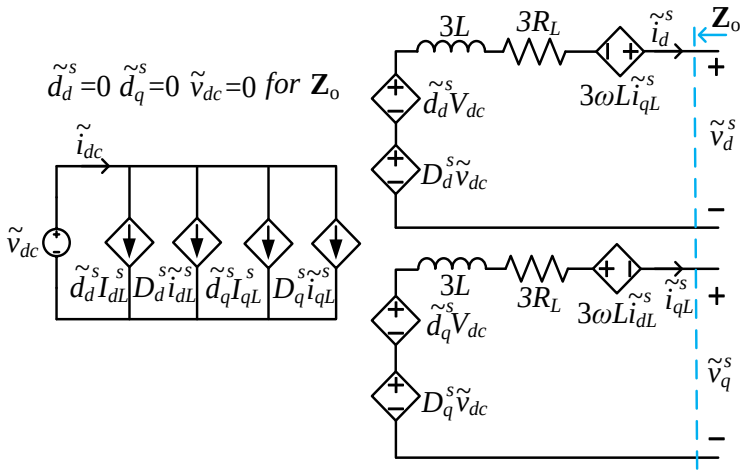


Fig. 6-9. Average model of grid-tied inverter with AFD method.

In order to model the small-signal propagation path through PLL, transfer function matrices $\mathbf{G}^{\mathbf{i}}_{\mathbf{PLL}}$ and $\mathbf{G}^{\mathbf{d}}_{\mathbf{PLL}}$ are defined. $\mathbf{G}^{\mathbf{i}}_{\mathbf{PLL}}$ models the path from system voltage to current in converter domain. $\mathbf{G}^{\mathbf{d}}_{\mathbf{PLL}}$ models the path from system voltage to duty cycle in converter domain. $\mathbf{K}_{\mathbf{v}}$ is the filter for voltage signals and $\mathbf{K}_{\mathbf{i}}$ is for current signals.

Once the power stage is modeled to SRF, the average model of PLL becomes Fig. 6-10, which shows that PLL is an estimator of system domain voltage vector v_d^s and v_q^s. $T_{\Delta\theta}$ is the rotation matrix shown in (6-4). $T_{\Delta\theta*}$ is the matrix used for duty cycle and current vectors rotation shown in (6-5).

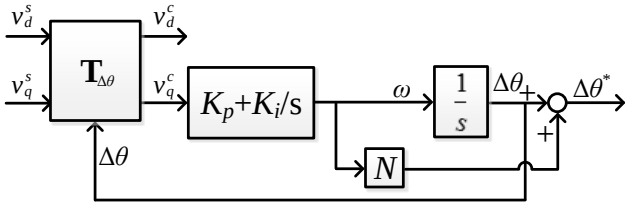


Fig. 6-10. Average model of SRF PLL.

$$\mathbf{T}_{\Delta\theta} = \begin{bmatrix} \cos(\Delta\theta) & \sin(\Delta\theta) \\ -\sin(\Delta\theta) & \cos(\Delta\theta) \end{bmatrix} \tag{6-4}$$

$$\mathbf{T}_{\Delta\theta*} = \begin{bmatrix} \cos(\Delta\theta^*) & \sin(\Delta\theta^*) \\ -\sin(\Delta\theta^*) & \cos(\Delta\theta^*) \end{bmatrix} \tag{6-5}$$

Let

$$tf_{PLL} = K_p + K_i / s \tag{6-6}$$

Actually, in the grid-tied inverter system, voltage and current vectors are firstly rotated from system domain to converter domain for feedback control, and then duty cycle vector is rotated from converter domain to system domain to give converter power stage command. Their relationship are:

$$\vec{D}^c = \mathbf{T}_{\Delta\theta^*}\vec{D}^s,\ \vec{V}^c = \mathbf{T}_{\Delta\theta}\vec{V}^s,\ \vec{I}^c = \mathbf{T}_{\Delta\theta^*}\vec{I}^s \tag{6-7}$$

Under steady state the angle between vectors in two domains is zero:

$$\vec{D}^c = \begin{bmatrix} \cos(0) & \sin(0) \\ -\sin(0) & \cos(0) \end{bmatrix}\vec{D}^s \tag{6-8}$$

Small signal perturbation can be added to (6-8) to get:

$$\begin{bmatrix} D_d^c + \tilde{d}_d^c \\ D_q^c + \tilde{d}_q^c \end{bmatrix} = \begin{bmatrix} \cos(0+\tilde{\theta}^*) & \sin(0+\tilde{\theta}^*) \\ -\sin(0+\tilde{\theta}^*) & \cos(0+\tilde{\theta}^*) \end{bmatrix} \cdot \begin{bmatrix} D_d^s + \tilde{d}_d^s \\ D_q^s + \tilde{d}_q^s \end{bmatrix} \tag{6-9}$$

By doing approximation of trigonometric functions, and cancel the steady state values. Relationship between converter domain duty cycle and system domain duty cycle can be derived as:

$$\begin{bmatrix} D_d^c + \tilde{d}_d^c \\ D_q^c + \tilde{d}_q^c \end{bmatrix} = \begin{bmatrix} 1 & \tilde{\theta}^* \\ \tilde{\theta}^* & 1 \end{bmatrix} \cdot \begin{bmatrix} D_d^s + \tilde{d}_d^s \\ D_q^s + \tilde{d}_q^s \end{bmatrix} \tag{6-10}$$

$$\begin{bmatrix} \tilde{d}_d^c \\ \tilde{d}_q^c \end{bmatrix} \approx \begin{bmatrix} \tilde{d}_d^s + D_q^s\tilde{\theta}^* \\ -D_d^s\tilde{\theta}^* + \tilde{d}_q^s \end{bmatrix} \tag{6-11}$$

Since,

$$\tilde{\theta}^* = \tilde{\theta} + N \cdot tf_{PLL} \cdot \tilde{v}_q^c \tag{6-12}$$

Then,

$$\begin{bmatrix} \tilde{d}_d^c \\ \tilde{d}_q^c \end{bmatrix} \approx \begin{bmatrix} \tilde{d}_d^s + D_q^s\left(\tilde{\theta} + N \cdot tf_{PLL} \cdot \tilde{v}_q^c\right) \\ -D_d^s\left(\tilde{\theta} + N \cdot tf_{PLL} \cdot \tilde{v}_q^c\right) + \tilde{d}_q^s \end{bmatrix} \tag{6-13}$$

By doing similar small signal analysis as above for voltage vectors, relation between PLL output angle and q axis voltage can be derive as [11]:

$$\tilde{v}_q^c = -V_d^s \tilde{\theta} + \tilde{v}_q^s \tag{6-14}$$

$$\tilde{\theta} = \frac{tf_{PLL}}{s + V_d^s tf_{PLL}} \tilde{v}_q^s = G_{PLL} \tilde{v}_q^s \tag{6-15}$$

Substitute (6-14) and (6-15) to (6-13):

$$\begin{bmatrix} \tilde{d}_d^c \\ \tilde{d}_q^c \end{bmatrix} \approx \begin{bmatrix} \tilde{d}_d^s \\ \tilde{d}_q^s \end{bmatrix} + \begin{bmatrix} 0 & D_q^s \left[\left(1 - Ntf_{PLL} V_d^s\right) G_{PLL} + Ntf_{PLL} \right] \\ 0 & -D_d^s \left[\left(1 - Ntf_{PLL} V_d^s\right) G_{PLL} + Ntf_{PLL} \right] \end{bmatrix} \begin{bmatrix} \tilde{v}_d^s \\ \tilde{v}_q^s \end{bmatrix} \tag{6-16}$$

Then:

$$\mathbf{G_{PLL}^d} = \begin{bmatrix} 0 & -D_q^s \left[\left(1 - Ntf_{PLL} V_d^s\right) G_{PLL} + Ntf_{PLL} \right] \\ 0 & D_d^s \left[\left(1 - Ntf_{PLL} V_d^s\right) G_{PLL} + Ntf_{PLL} \right] \end{bmatrix} \tag{6-17}$$

Using similar approach, $\mathbf{G_{PLL}^i}$ can be derived as:

$$\mathbf{G_{PLL}^i} = \begin{bmatrix} 0 & I_q^s \left[\left(1 - Ntf_{PLL} V_d^s\right) G_{PLL} + Ntf_{PLL} \right] \\ 0 & -I_d^s \left[\left(1 - Ntf_{PLL} V_d^s\right) G_{PLL} + Ntf_{PLL} \right] \end{bmatrix} \tag{6-18}$$

Solving the equations represented by Fig. 6-8, the output impedance of grid-tied inverter system with PLL-based AFD is:

$$\begin{aligned} \mathbf{Z_{out\_il\_PLL}} = & \left(\mathbf{Z_{out}^{-1}} - \mathbf{G_{id}} \mathbf{G_{del}} \left(\left(\mathbf{G_{ci}} - \mathbf{G_{dei}} \right) \mathbf{G_{PLL}^i} - \mathbf{G_{PLL}^d} \right) \mathbf{K_v} \right)^{-1} \cdot \\ & \left(\mathbf{I} + \mathbf{G_{id}} \mathbf{G_{del}} \left(\mathbf{G_{ci}} - \mathbf{G_{dei}} \right) \mathbf{K_i} \right) \end{aligned} \tag{6-19}$$

Table 6-1. Parameters for simulation and Calculation

Symbol	Description	Value
V_{dc} (V)	Dc voltage	270
V^s_d (V)	D channel source voltage	99.6
V^s_q (V)	Q channel source voltage	0
f (Hz)	Line frequency	60

L_{ac} (mH)	Ac inductor	1
R_{Lac} (mΩ)	Ac inductor ESR	110
I_{dref} (A)	D channel current reference	-10
I_{qref} (A)	Q channel current reference	0
K_{pi}	Current controller proportional gain	0.0233
K_{ii}	Current controller integral gain	2.5598
K_p	PLL proportional gain	1
K_i	PLL integral gain	2
f_{sw} (kHz)	Switching frequency	20
R_L (Ω)	Load resistor	10
L_L (mH)	Load inductor	17.4
C_L (μF)	Load capacitor	400

Using the parameters in Table 6-1, Fig. 6-11 shows the Bode plot of grid-tied inverter output impedance. The results shows that the *q-q* channel dc impedance is a negative incremental resistance. The magnitude of Z_{qq} equals to the per unit value of inverter system. A higher power rating of the inverter will result in a lower magnitude negative resistance as shown in the Z_{qq}.

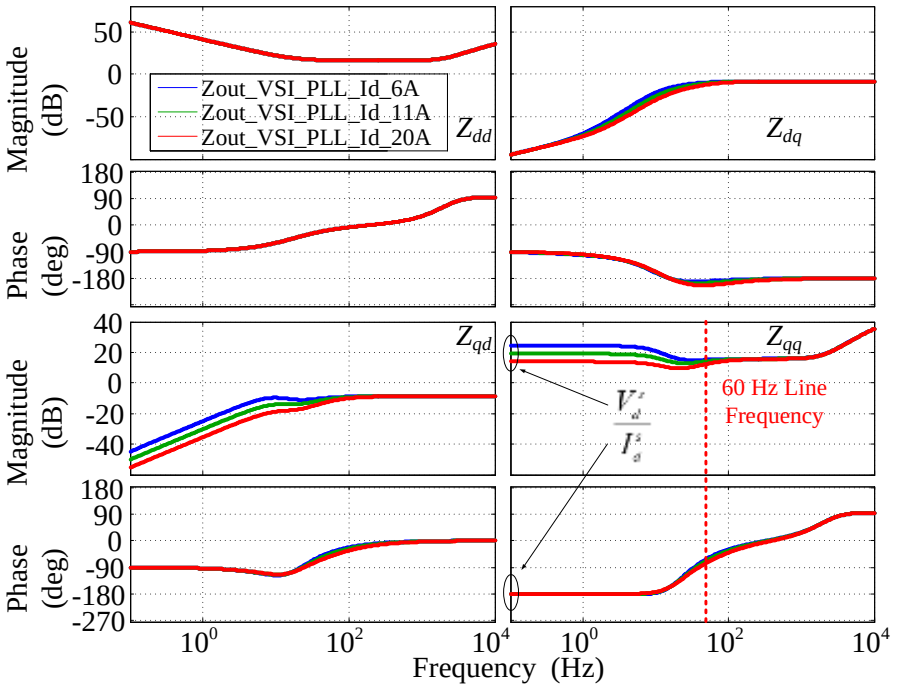


Fig. 6-11. Output impedance of grid-tied inverter without PLL-based AFD method.

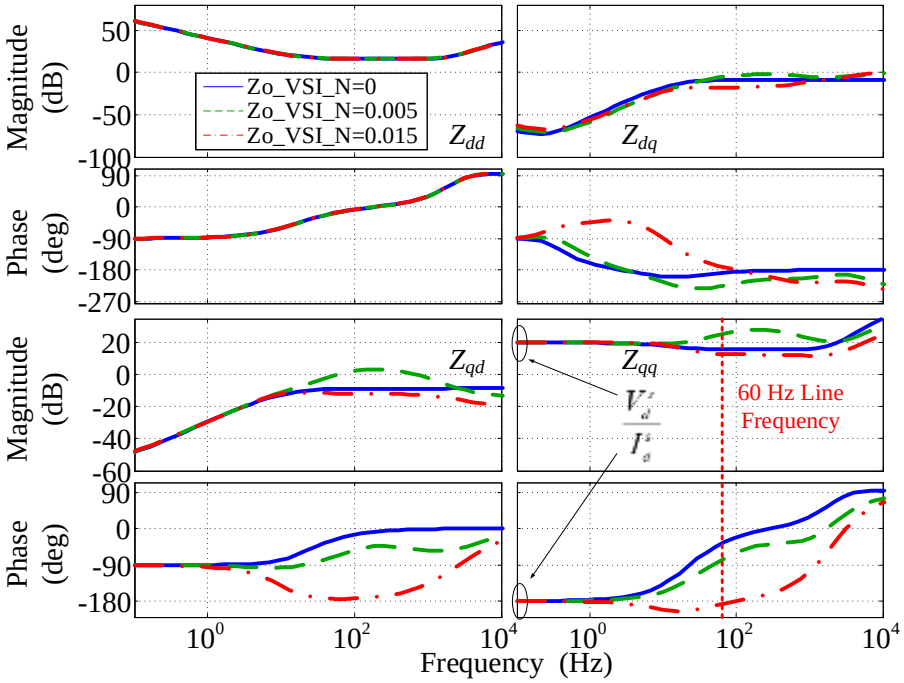


Fig. 6-12. Output impedance of grid-tied inverter with PLL-based AFD method.

Fig. 6-12 shows the output impedance of the grid-tied inverter with different feed forward gain N in the PLL-based AFD method. Because of the feed forward loop, the phase of Z_{qq} drops below -180 °. The bigger feed forward gain is, the lower the phase of Z_{qq} is.

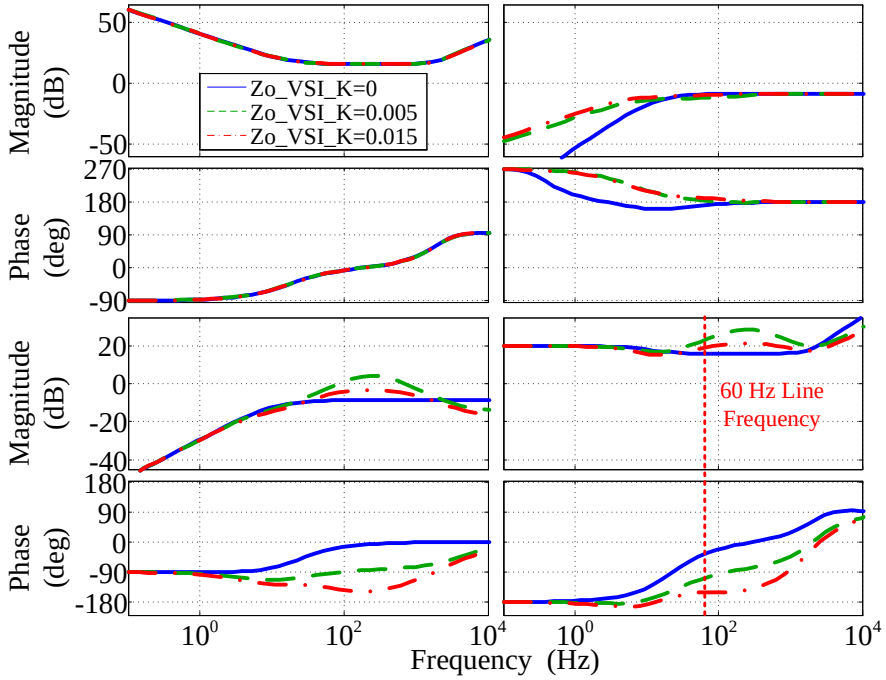


Fig. 6-13. Output impedance of grid-tied inverter with SFS AFD method.

Fig. 6-13 shows the output impedance of the grid-tied inverter with different positive feedback gain K in the SFS AFD method. Similar phenomenon can be found that the phase of Z_{qq} drops below -180 °. The bigger positive feedback gain K is, the lower the phase of Z_{qq} is.

6.2.3 Impedance-based analysis

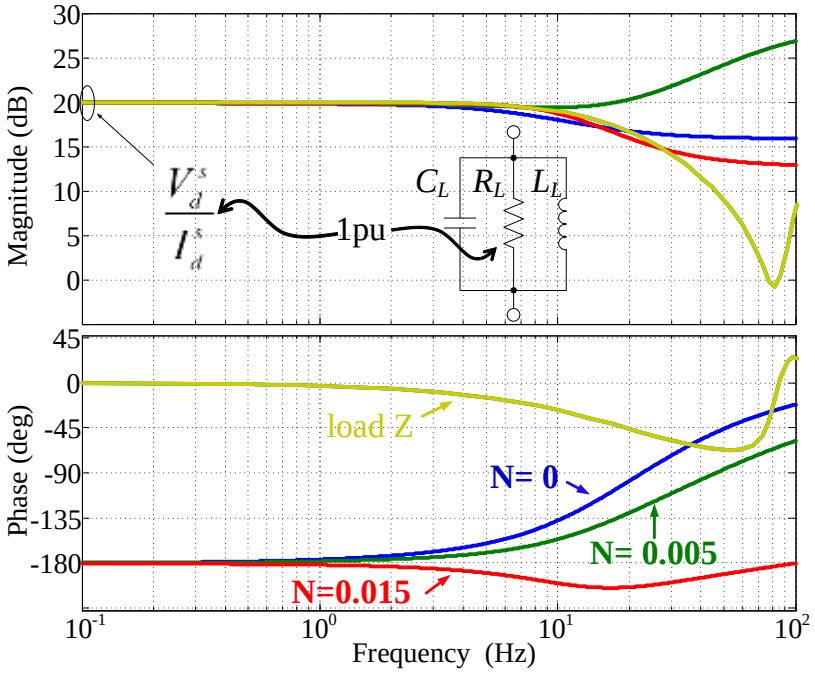


Fig. 6-14. Impedance interaction in *qq* channel.

When the output impedance of the grid-tied inverter and the impedance of local load are put together, an impedance interaction is found. As shown in Fig. 6-14, the dc impedance of the inverter is equal to the dc impedance of the local load. With feed forward gain N = 0, the phase difference is 180 °; with N bigger than 0.015, the system becomes unstable due to lack of phase margin.

As been reported in [12], grid-tied inverter output impedance has RHP pole. If it is treated as source converter, it is better to use generalized inverse Nyquist (GINC) criteria to study the system stability. Fig. 6-15 shows the characteristic loci of system return ratio reciprocal which indicates that the system is destabilized with bigger feed forward gain N.

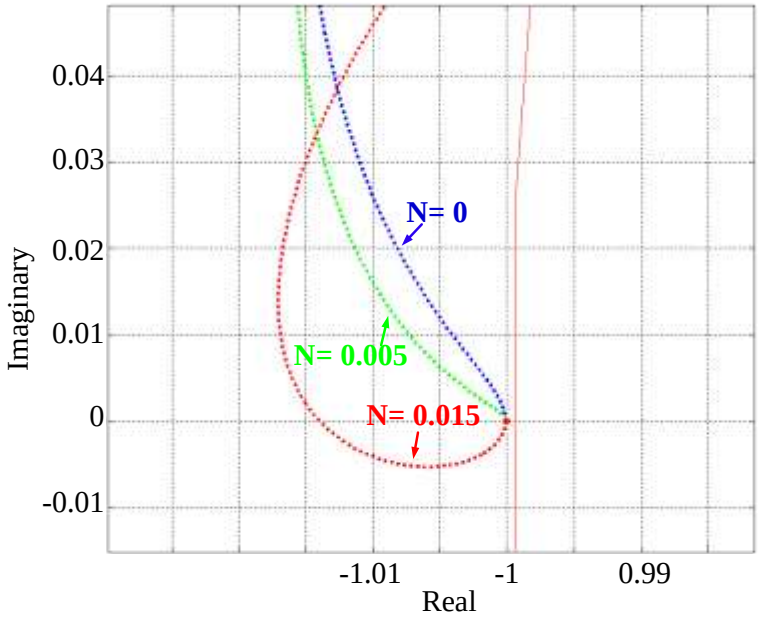


Fig. 6-15. Characteristic loci of inverter system.

6.3 Experimental Results of Islanding Detection

In order to verify the proposed model and analysis, output impedances of a three-phase grid-tied inverter with PLL-based and SFS AFD islanding detection methods are measured with different parameters which is listed in Table 6-2. According to the analysis above, the critical dynamics locates at low frequency range (0.1~10Hz) which the impedance analyzer [13] in the lab cannot measure. In order to show the interesting dynamics, the line frequency is changed to 400 Hz, the bandwidth of PLL is also increased as shown in Table 6-2.

Table 6-2. Parameters for Experimental Verification

Symbol	Description	Value
f (Hz)	Line frequency	400
K_p	PLL proportional gain	8.921
K_i	PLL integral gain	3964

Fig. 6-16 shows the comparison between measurement results and model calculation results for Z_{qq} of grid-tied inverter with and without PLL-based AFD method. Fig. 6-17 shows the corresponding comparison for SFS AFD method.

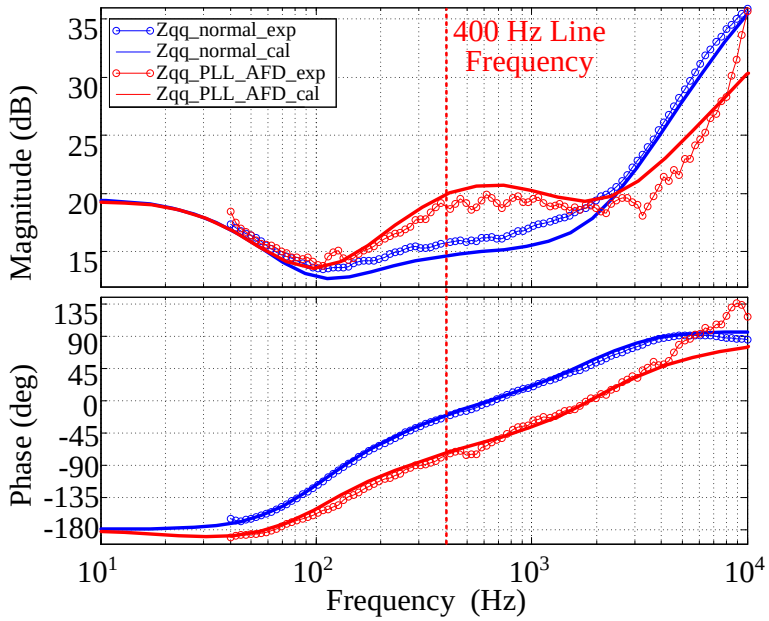


Fig. 6-16 Measurement of Z_{qq} for PLL-based AFD method with N = 0.0005.

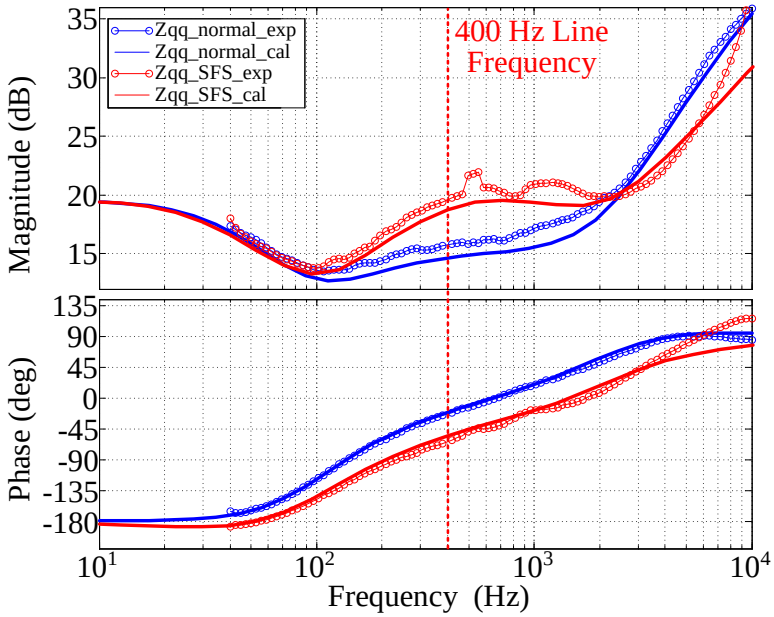
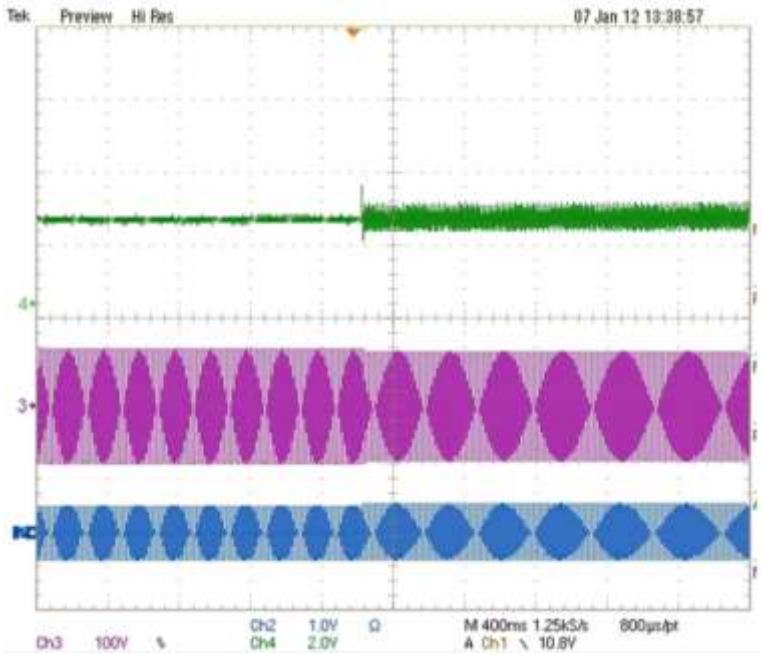


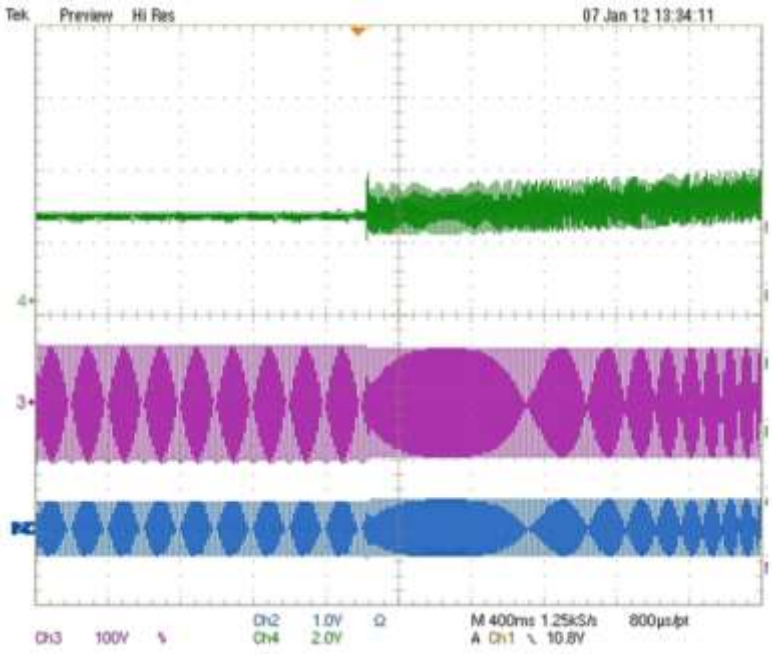
Fig. 6-17. Measurement of Z_{qq} for SFS AFD method with K = 0.0008.

The time domain experiments are carried out using parameters in Table 6-1. Fig. 6-18 shows the islanding event with feed forward gain N = 0. It shows that the PLL stays at it steady-state value, the system is stable. Both voltage and current does not change due to the matched load condition. Fig. 6-19 shows the islanding event with N = 0.015. It can be seen that PLL output frequency starts to drift when islanding event happens, the system is unstable.



Terminal voltage (purple) [100 V/DIV], inverter current (blue) [20A/DIV], ωc (green) [5 Hz/DIV]

Fig. 6-18. Islanding event (PLL with feed forward gain N = 0).



Terminal voltage (purple) [100 V/DIV], inverter current (blue) [20A/DIV], ωc (green) [5 Hz/DIV]

Fig. 6-19. PLL with feed forward gain N = 0.015 when islanding event happens.

Chapter 7 Impedances Specification for Balanced Distributed Power Systems

7.1 Introduction

Although many results demonstrate the stability at the ac interface can be easily and readily predicted using the measured impedances and the GNC in *d-q* frame for ac system, similar load impedances specifications, as they are done in dc system (see Section 1.1.1 in Chapter 1), is not reported. To fill this gap, this chapter discusses the challenges of stability analysis and load impedance specification in three-phase ac system, namely its coupled multi-input multi-output (MIMO) nature. Then a method to do load impedance specification in *d-q* frame is proposed. Condition and limitation of the proposed method are discussed. Simulation and measurement verify the analysis.

7.2 Ac System Small-Signal Stability Analysis in *d-q* Frame

Small-signal stability analysis for three-phase ac system can be analyzed in *d-q* frame by applying GNC or GINC to the minor loop-gain $\mathbf{L}(s)$ as defined by Eq. (7-1). The stability condition of the system under study is deterimined by eigenvalues of $\mathbf{L}(s)$ as shown in Eq. (7-3).

$$\mathbf{L}(s)=\mathbf{Z}_{\mathbf{sdq}}(s)\cdot\mathbf{Y}_{\mathbf{ldq}}(s)=\begin{bmatrix} Z_{sdd}(s) & Z_{sdq}(s) \\ Z_{sqd}(s) & Z_{sqq}(s) \end{bmatrix}\cdot\begin{bmatrix} Y_{ldd}(s) & Y_{ldq}(s) \\ Y_{lqd}(s) & Y_{lqq}(s) \end{bmatrix} \tag{7-1}$$

$$\mathbf{L}(s)=\begin{bmatrix} Z_{sdd}(s)Y_{ldd}(s)+Z_{sdq}(s)Y_{lqd}(s) & Z_{sdd}(s)Y_{ldq}(s)+Z_{sdq}(s)Y_{lqq}(s) \\ Z_{sqd}(s)Y_{ldd}(s)+Z_{sqq}(s)Y_{lqd}(s) & Z_{sqd}(s)Y_{ldq}(s)+Z_{sqq}(s)Y_{lqq}(s) \end{bmatrix} \tag{7-2}$$

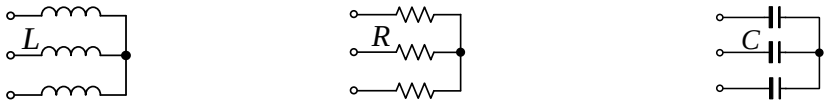
$$\mathbf{C}(s)\cdot\mathbf{L}(s)\cdot\mathbf{C}^{-1}(s)=\begin{bmatrix} \lambda_1(s) & 0 \\ 0 & \lambda_2(s) \end{bmatrix} \tag{7-3}$$

It seems the method of using of GNC in *d-q* frame to study small-signal stability of three-phase ac system is a dualism of the one for dc system. However, the essential difference between

three-phase ac system and dc system is that the ac system is a coupled multi-input and multi-output system. Perturbation in one channel induces response not only in the same channel but also the cross channel. Although GNC utilizes minor loop-gain defined by these impedance matrices. Elements of minor loop-gain matrix are functions of both self-channel and cross-channel impedances ratios as show in Eq. (7-1) and (7-2). Plus, stability condition is finally judged by eigenvalues of **L**(*s*). If **L**(*s*) is non-diagonal, finding eigenvalues for non-diagonal matrix will involve complicated computation, which makes indirect relationship between system stability condition and impedances. This is the roadblock to do load impedances specification for ac system in *d-q* frame. Based on the relationship between a matrix's eigenvalues and its singular values, Ref. [69] proposes to limit the minimum singular value of load input impedance matrix to be smaller than the maximum singular value of the source output impedances matrix. This concept is similar as the one in Ref. [28] for dc system, which leads to conservative design. Load impedances specification in ac system that allows impedance interaction but still keep the system stable with certain margin is not reported yet.

7.3 Load Impedance Specification for Unity Power Factor Systems

As shown in the discussion above, the difficulty of doing load impedance specification of three-phase ac system is because of its' coupled MIMO system nature. Let us take time to see where dose the coupling come from. Eq.(7-1)–(7-4) list the admittances matrix (which is the inverse of impedance matrix) expression of three-phase resistive, inductive, and capacitive loads. Clearly, *d-q* admittances (and impedances) matrix (Eq. (7-5)) of resistor is diagonal. Admittance matrices of inductor and capacitor are not.



(a) (b) (c)

Fig. 7-1. Small-signal representation of a balanced three-phase system in d-q frame.

$$\mathbf{Y}_{\mathbf{Ldq}} = \begin{bmatrix} \dfrac{s}{Ls^2 + L\omega^2} & \dfrac{\omega}{Ls^2 + L\omega^2} \\ -\dfrac{\omega}{Ls^2 + L\omega^2} & \dfrac{s}{Ls^2 + L\omega^2} \end{bmatrix} \tag{7-4}$$

$$\mathbf{Y}_{\mathbf{Rdq}} = \begin{bmatrix} R^{-1} & 0 \\ 0 & R^{-1} \end{bmatrix} = \begin{bmatrix} R & 0 \\ 0 & R \end{bmatrix}^{-1} = \mathbf{Z}_{\mathbf{Rdq}}^{-1} \tag{7-5}$$

$$\mathbf{Y}_{\mathbf{Cdq}} = \begin{bmatrix} sC & -\omega C \\ \omega C & sC \end{bmatrix} \tag{7-6}$$

7.3.1 Simplified stability analysis and load impedance specification for ac system

The structure of admittances matrix of three-phase resistor gives hint that if the source output impedances matrix $\mathbf{Z_{sdq}}$ and load admittances matrix $\mathbf{Y_{ldq}}$ are diagonal, then the minor loop-gain **L** is diagonal as shown in Eq. (7-7), eigenvalues of **L** are *d* channel and *q* channel source and load impedances ratios as shown in Eq. (7-8). System stability condition is directly judged by source and load impedances ratios in *d* and *q* channel. Three-phase ac system becomes two decoupled dc systems. Impedance specification methods that are developed in dc system can be applied to these two dc systems separately. In this way, system stability are ensured with certain GM and PM while still allows impedances interaction, which gives less conservative design compare to the singular value based approach in Ref. [3] and [69].

$$\begin{aligned} \mathbf{L}(s) &= \mathbf{Z}_{\mathbf{sdq}}(s) \cdot \mathbf{Y}_{\mathbf{ldq}}(s) = \begin{bmatrix} Z_{sdd}(s) & 0 \\ 0 & Z_{sqq}(s) \end{bmatrix} \cdot \begin{bmatrix} Y_{ldd}(s) & 0 \\ 0 & Y_{lqq}(s) \end{bmatrix} \\ &= \begin{bmatrix} Z_{sdd}(s) \cdot Z_{ldd}^{-1}(s) & 0 \\ 0 & Z_{sqq}(s) \cdot Z_{lqq}^{-1}(s) \end{bmatrix} \end{aligned} \tag{7-7}$$

$$\mathbf{C}(s) \cdot \mathbf{L}(s) \cdot \mathbf{C}^{-1}(s) = \begin{bmatrix} \lambda_1(s) & 0 \\ 0 & \lambda_2(s) \end{bmatrix} = \begin{bmatrix} Z_{sdd}(s) \cdot Z_{ldd}^{-1}(s) & 0 \\ 0 & Z_{sqq}(s) \cdot Z_{lqq}^{-1}(s) \end{bmatrix} \tag{7-8}$$

The simplification shown above relies on source and load impedance matrices with diagonal structure. Impedance matrices' structure of typical dc-ac and ac-dc converters in ac DPS should

be studied to verify this precondition. Typical dc-ac converters are voltage source inverters (VSIs). They work as voltage source in ac DPS. Typical ac-dc converters are different rectifiers, they work as active front-ends (AFEs) interfacing different loads or dc buses. In this paper boost rectifier is chosen as an example.

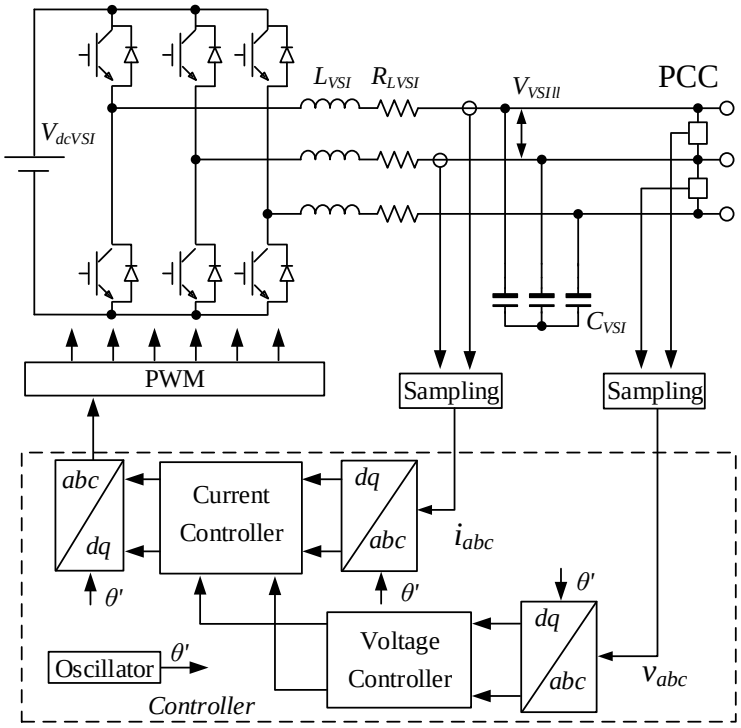


Fig. 7-2. Power stage and control system of VSI.

7.3.2 Output impedance of VSI

VSI, as shown in Fig. 7-2, is the typical voltage source in the DPS. If output impedances of VSIs are not designed low enough, with certain loads, the whole DPS could be unstable . In this section, the output impedances matrix of VSI is analyzed to show that it can be shaped to be diagonal by feedback controller. Small-signal impedance is derived by linearizing the average model around an equilibrium point. The average model in *d-q* frame of VSI with feedback controllers is shown in Fig. 7-3.

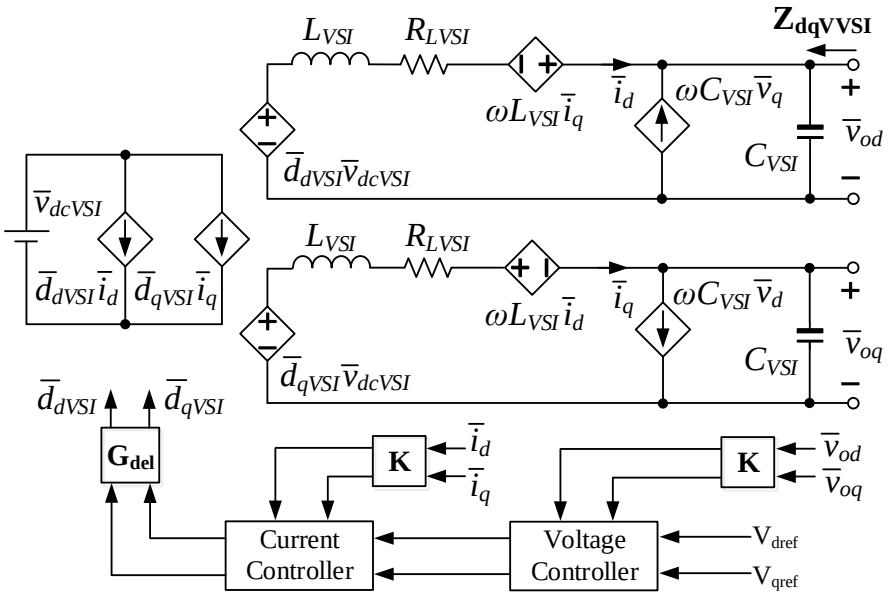


Fig. 7-3. Average model of VSI in d-q frame with feedback control.

As discussed in chapter 2, both power stage and the feedback controller influences the output impedances matrix ($\mathbf{Z}_{\mathbf{dqVSI}}$). Open-loop output impedances of VSI are determined by output *LC* filter and line frequency. They are independent of VSI duty-ratio steady state value ($\vec{D}_{VSI}$).

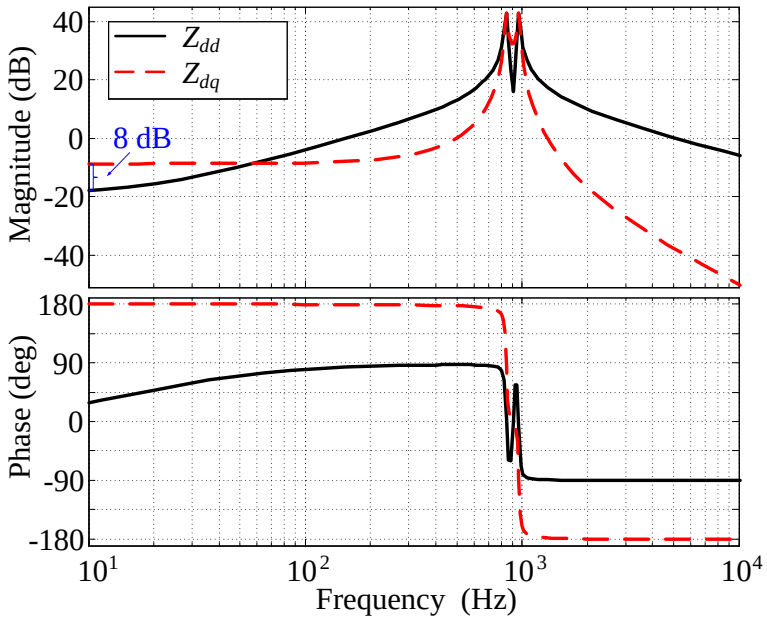


Fig. 7-4. Non-diagonal feature of impedances matrix of VSI.

With parameters shown in Table 7-1, Fig. 7-4 shows the non-diagonal feature of impedances matrix of VSI. At low frequency up to 50Hz, Z_{dq} is bigger than Z_{dd}. At the resonant frequency, magnitude of Z_{dq} is the same as the one of Z_{dd}. Open loop impedances matrix of VSI is non-diagonal. This is due to the coupling between *d* and *q* channel inductor currents and capacitor voltages.

Table 7-1. Parameters of simulation system

Symbol	Description	Value
V_{ll}	Grid line-line peak voltage	$57.5\sqrt{6}$ V
f_g	Grid voltage frequency	60 Hz
L_{VSI}	Inductance of inverter	0.97 mH
V_{dcVSI}	Inverter dc voltage	270 V
f_{sw}	Switching frequency of VSI and AFE	20 kHz
$I_{drefVSI}$	*d* channel current of inverter	11 A
$I_{qrefVSI}$	*q* channel current of inverter	0 A
k_{piVSI}	Proportional gain of current controller	0.0041
k_{iiVSI}	Integrator gain of current controller	0
k_{pvVSI}	Proportional gain of voltage controller	0.029
k_{ivVSI}	Integral gain of voltage controller	78.5398
L_{AFE}	Inductance of AFE	0.47 mH
C_{dc}	Dc link capacitor of AFE	100 μF
R_{dc}	Load resistor of AFE	96 Ω
V_{dcAFE}	Dc voltage of AFE	270 V
k_{piAFE}	Proportional gain of AFE current controller	0.0116
k_{iiAFE}	Integrator gain of AFE current controller	23.2711
k_{pvAFE}	Proportional gain of AFE voltage controller	0.0628
k_{ivAFE}	Integrator gain of AFE voltage controller	3.2725
$k_{ppllAFE}$	Proportional gain of AFE PLL	0.8921
$k_{ipllAFE}$	Integral gain AFE of PLL	39.64
L_f	Inductance of AFE input filter	120 μH
C_f	Capacitance of AFE input filter	10 μF

Many techniques can be used to decouple the VSI system. Damping [109], [110] can reduce the *LC* filter resonance and help to decouple the system at the resonant frequency. For example, adding a damping resistor with 1% impedance of the capacitor at the line frequency as shown in

Fig. 7-5, open-loop impedances Z_{dq} and Z_{qd} can be reduced with 4 dB less than Z_{dd} and Z_{qq} as shown in Fig. 7-6.

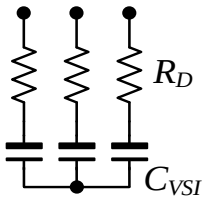


Fig. 7-5. Capacitor with 1% damping resistor.

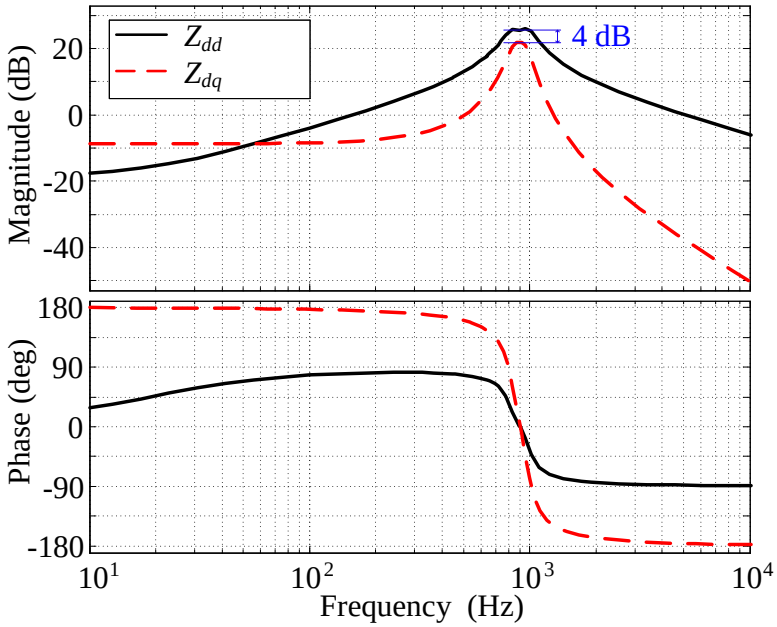


Fig. 7-6. VSI open-loop impedances with damping resistor

Feedback control can also help reducing the coupling between two channels, since current or voltage on one channel are disturbances to another channel. Feedback control can reject disturbance. On top of feedback control, various decoupling methods [108], [111], [112] are developed to further reduce the cross coupling effect. In this paper, most common feedback control with decoupling methods are adopted to show that they are capable to shape the output impedances matrix of VSI diagonal. Fig. 7-7 shows the proportional (P) current controller with decoupling technique [108]. Fig. 7-8 shows the proportional-integral (PI) voltage controller with decoupling.

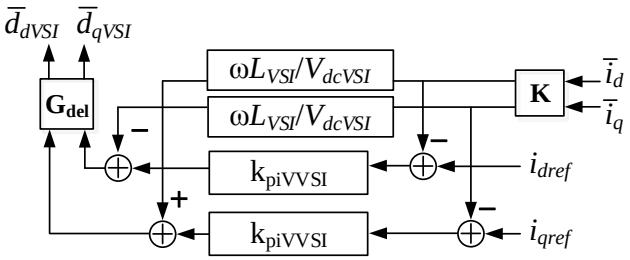


Fig. 7-7. Current controller with decoupling for VSI.

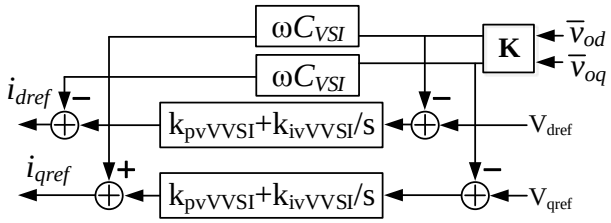


Fig. 7-8. Voltage controller with decoupling for VSI.

Together with the power stage small-signal model, Fig. 7-9 shows the whole model of VSI, in which $\mathbf{G_{ciV}}$ is current controller matrix; $\mathbf{G_{dei}}$ is the decoupling matrix for current controller; $\mathbf{G_{cvV}}$ is the voltage controller matrix; $\mathbf{G_{dev}}$ is the decoupling matrix for voltage controller.

$$\mathbf{G_{ciV}} = \begin{bmatrix} k_{piVVSI} & 0 \\ 0 & k_{piVVSI} \end{bmatrix} \tag{7-9}$$

$$\mathbf{G_{dei}} = \begin{bmatrix} 0 & -\dfrac{\omega L_{VSI}}{V_{dc\_VSI}} \\ \dfrac{\omega L_{VSI}}{V_{dc\_VSI}} & 0 \end{bmatrix} \tag{7-10}$$

$$\mathbf{G_{ciV}} = \begin{bmatrix} k_{piVVSI} & 0 \\ 0 & k_{piVVSI} \end{bmatrix} \tag{7-11}$$

$$\mathbf{G_{dev}} = \begin{bmatrix} 0 & -\omega C_{VSI} \\ \omega C_{VSI} & 0 \end{bmatrix} \tag{7-12}$$

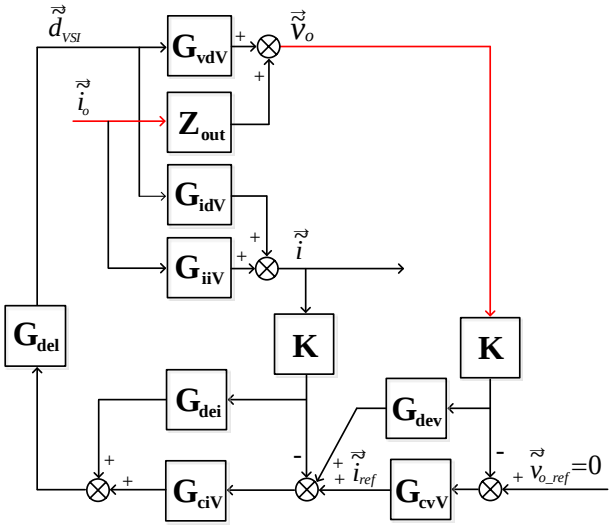


Fig. 7-9. VSI small-signal model with feedback control.

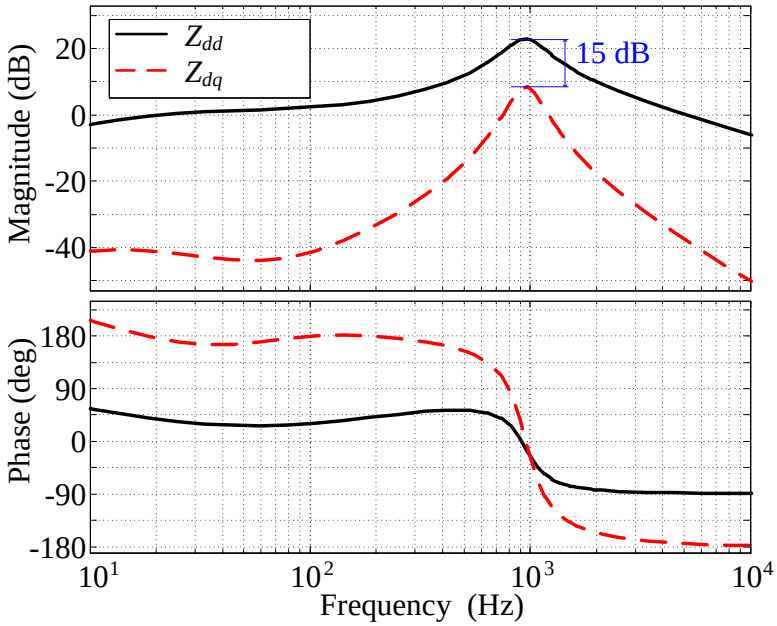


Fig. 7-10. Output impedances of VSI with and feedback decoupling control.

Fig. 7-10 shows Z_{dd} and Z_{dq} of VSI with voltage and current feedback decoupling control. At low frequency, Z_{dq} is greatly reduced by decoupling terms in current and voltage controllers. Even at the *LC* filter resonant frequency, Z_{dq} is 15 dB less than Z_{dd}, which means with feedback decoupling control the output impedances matrix $\mathbf{Z}_{\mathbf{dqVVSI}}$ of VSI is diagonal dominant.

By checking the model shown in Fig. 7-9, none of the transfer function matrices is a function of VSI steady state values of duty-ratio ($\vec{D}_{VSI}$), output voltage ($\vec{V}_o$) and output current ($\vec{I}_o$). This indicates that output impedances matrix $\mathbf{Z}_{\mathbf{dqVVSI}}$ is independent of operation point of voltage-controlled VSI (although some matrices are influenced by V_{dcVSI}, V_{dcVSI} is fixed for most of the operation), it is only influence by power stage and feedback controllers' parameters.

The analysis in this section can be simply concluded that output impedances matrix of VSI can be easily shaped as diagonal dominant matrix, and it is not influenced by operation point of VSI.

7.3.3 Admittance of AFE

Fig. 7-11 shows the power stage and control system of AFE. The power stage is a two-level three-phase boost rectifier. PCC voltages are measured for PLL to do grid-synchronization. SRF PLL strategy is used. Boost inductor currents and output voltages are measured by inner current and outer voltage feedback control-loops.

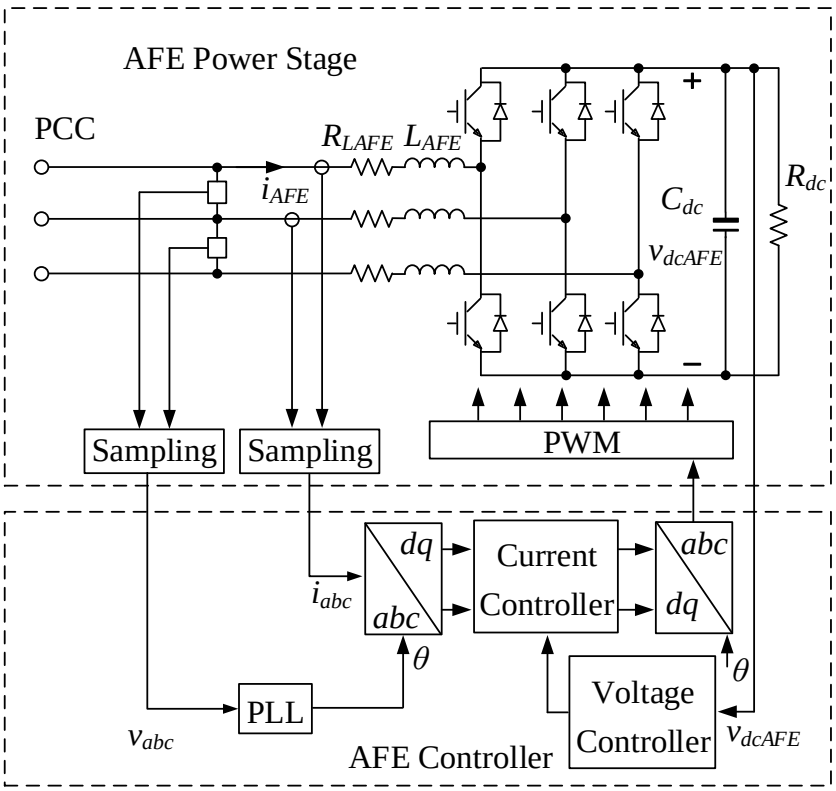
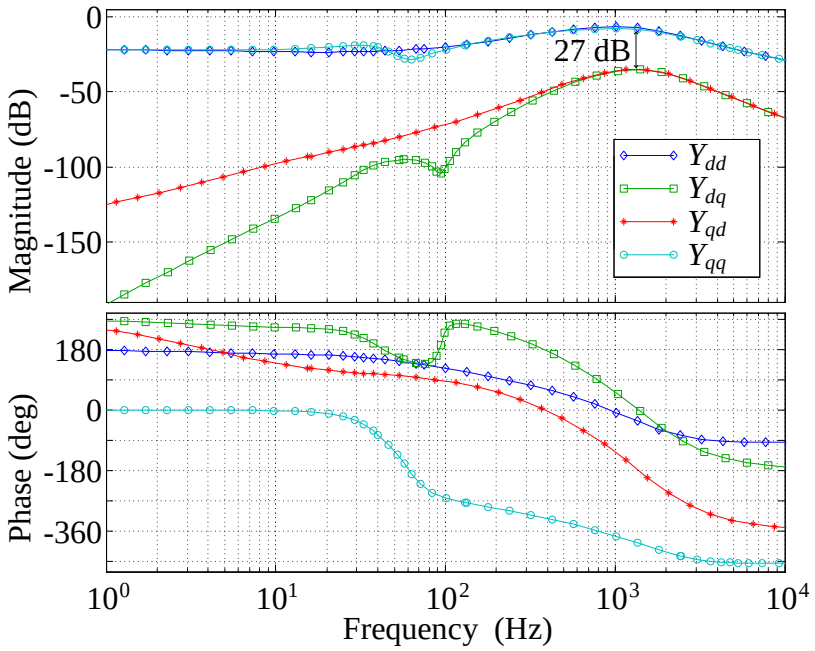
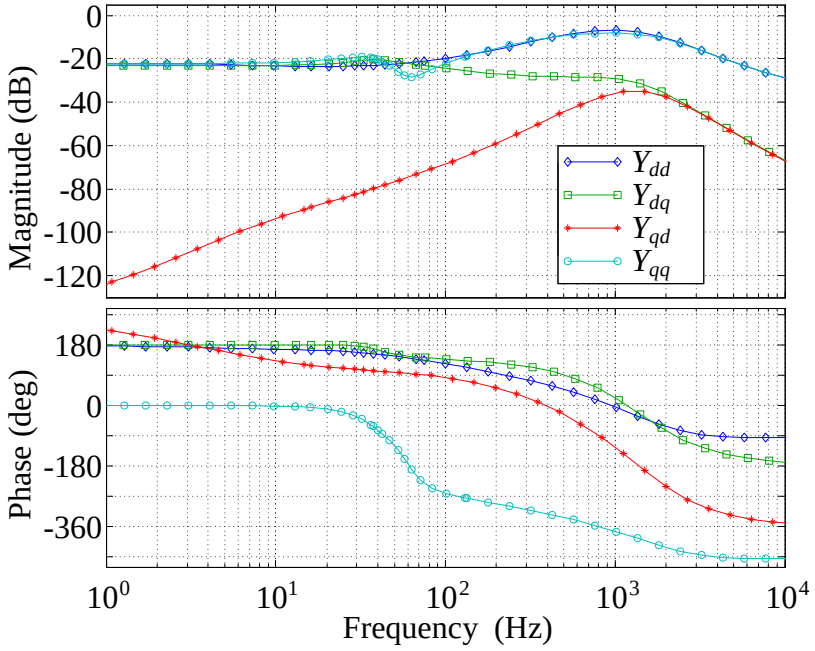


Fig. 7-11. Power stage and control system of AFE.

The discussion in chapter 2 shows that the input admittances of AFE power stage is related to the steady state values of duty-ratio ($\vec{D}^s_{AFE}$). Moreover, in chapter 4 shows that, PLL dynamics also influence input admittance of AFE. $\mathbf{G}^{\mathbf{d}}_{\mathbf{PLL}}$ (Eq. (4-7)) is a function of AFE steady state values of duty-ratio ($\vec{D}^s_{AFE}$), and $\mathbf{G}^{\mathbf{i}}_{\mathbf{PLL}}$ (Eq. (4-8)) is a function of steady state values of output current ($\vec{I}^{\,s}$). This indicates that input admittance matrix $\mathbf{Y}_{\mathbf{dqAFE}}$ is related to the operation point of AFE, with different output current, $\mathbf{Y}_{\mathbf{dqAFE}}$ is different. When AFE is working under unity power factor condition, I^s_{qAFE} is 0, $\mathbf{G}^{\mathbf{i}}_{\mathbf{PLL}}$ is diagonal, $\mathbf{G}^{\mathbf{d}}_{\mathbf{PLL}}$ is diagonal dominant. Feedback decoupling control shapes $\mathbf{Y}_{\mathbf{dqAFE}}$ as diagonal dominant as shown in Fig. 7-12 (a). When VSI injects reactive current to the PCC, I^s_{qAFE} could be bigger than I^s_{dAFE}, $\mathbf{G}^{\mathbf{i}}_{\mathbf{PLL}}$ is non-diagonal, consequently, $\mathbf{Y}_{\mathbf{dqAFE}}$ is non-diagonal as shown in Fig. 7-12 (b).



(a)



(b)

Fig. 7-12. AFE input admittances with different PLL bandwidth.

7.3.4 Influence of filter

In the discussion above, it has been proved that output impedances matrix of VSI can be designed as diagonal by feedback decoupling control. For AFE, under unity power factor condition, its input admittance can also be designed as diagonal by feedback decoupling control. For voltage-controlled VSI, no output filter is needed in addition to its own *LC* filter. For AFEs, since they are connected to the PCC, additional filters are needed to reduce the harmonics generated by them as shown in Fig. 7-13. Influence of filter to the diagonal features of the admittance matrices of AFE should be considered.

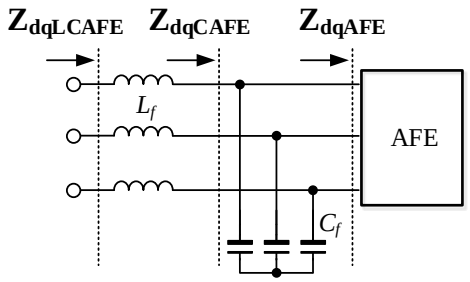


Fig. 7-13. AFE with input filter.

Assume the filter is a single-stage *LC* filter as shown in Fig. 7-13. Multi-stage filter can be simplified to single-stage filter [109].

There are certain design constraints that set up the boundary for the value of L_f and C_f in Fig. 7-13. The tolerable reactive power consumption by C_f is typically set to 2%~5% of the active power of the converter [90].

$$\left(V_d^s\right)^2 \omega C_f = 5\% V_d^s I_d^s \tag{7-13}$$

$$C_f = \frac{5\%}{\omega R} \tag{7-14}$$

R is the base impedance of the converter system.

$$R = \frac{V_d^s}{I_d^s} \tag{7-15}$$

Base on the discussion on the input impedances of AFE, within the bandwidth of feedback control, its input impedance can be assumed as (here, impedances matrix is used for easy derivation. It is easy to see that for 2×2 matrix, if impedance matrix is diagonal dominant, then admittance matrix is also diagonal dominant):

$$\mathbf{Z}_{\mathbf{dq}AFE} = \begin{bmatrix} -R & 0 \\ 0 & R \end{bmatrix} \tag{7-16}$$

Then,

$$\begin{aligned} \mathbf{Z}_{\mathbf{dqCAFE}} &= \left(\left(\mathbf{Z}_{\mathbf{dqCf}}\right)^{-1} + \left(\mathbf{Z}_{\mathbf{dqAFE}}\right)^{-1}\right)^{-1} = \begin{bmatrix} Z_{dd} & Z_{dq} \\ Z_{qd} & Z_{qq} \end{bmatrix} \\ &= \begin{bmatrix} \dfrac{20R\omega(s+20\omega)}{s^2-399\omega^2} & \dfrac{20R\omega^2}{s^2-399\omega^2} \\ -\dfrac{20R\omega^2}{s^2-399\omega^2} & \dfrac{20R\omega(s-20\omega)}{s^2-399\omega^2} \end{bmatrix} \end{aligned} \tag{7-17}$$

$\mathbf{Z}_{\mathbf{dqCAFE}}$ is diagonal dominant, since:

$$\left|\frac{Z_{dd}}{Z_{dq}}\right| = \left|\frac{Z_{dd}}{Z_{qd}}\right| = \left|\frac{20R\omega(s+20\omega)}{20R\omega^2}\right| = \left|\frac{s+20\omega}{\omega}\right| \geq 20 \tag{7-18}$$

$$\left|\frac{Z_{qq}}{Z_{dq}}\right| = \left|\frac{Z_{qq}}{Z_{qd}}\right| = \left|\frac{20R\omega(s-20\omega)}{20R\omega^2}\right| \geq 20 \tag{7-19}$$

AFE input impedance matrix with input *LC* filter is:

$$\begin{aligned}\mathbf{Z}_{\mathbf{dqLCAFE}} &= \mathbf{Z}_{\mathbf{dqLf}} + \mathbf{Z}_{\mathbf{dqCAFE}} \\ &= \begin{bmatrix} \dfrac{20R\omega(s+20\omega)}{s^2-399\omega^2} + L_f s & -L_f\omega \\ L_f\omega & \dfrac{20R\omega(s-20\omega)}{s^2-399\omega^2} + L_f s \end{bmatrix}\end{aligned} \tag{7-20}$$

Consider the frequencies that are less and equal to line frequency, $L_f s$ can be ignored, since

$$L_f s < L_f \omega \tag{7-21}$$

Then,

$$\left|\frac{Z_{dd}}{Z_{dq}}\right| = \left|\frac{Z_{dd}}{Z_{qd}}\right| = \left|\frac{20R\omega(s+20\omega)}{s^2-399\omega^2}\times\frac{1}{L_f\omega}\right| \approx \frac{20R\omega(20\omega)}{399\omega^2}\times\frac{1}{L_f\omega} = \frac{400R}{399L_f\omega} \tag{7-22}$$

$$\left|\frac{Z_{qq}}{Z_{qd}}\right| = \left|\frac{Z_{qq}}{Z_{dq}}\right| = \left|\frac{20R\omega(s-20\omega)}{s^2-399\omega^2}\times\frac{1}{L_f\omega}\right| \approx \frac{20R\omega(20\omega)}{399\omega^2}\times\frac{1}{L_f\omega} = \frac{400R}{399L_f\omega} \tag{7-23}$$

Design of L_f depends on the attenuation of harmonics, but impedances of L_f at line frequency is typically less than 20% of converter system base impedances R, then:

$$\left|\frac{Z_{dd}}{Z_{dq}}\right| > 5 \tag{7-24}$$

$\mathbf{Z}_{\mathbf{dqLCAFE}}$ is diagonal dominant within the line frequency range.

Above line frequency,

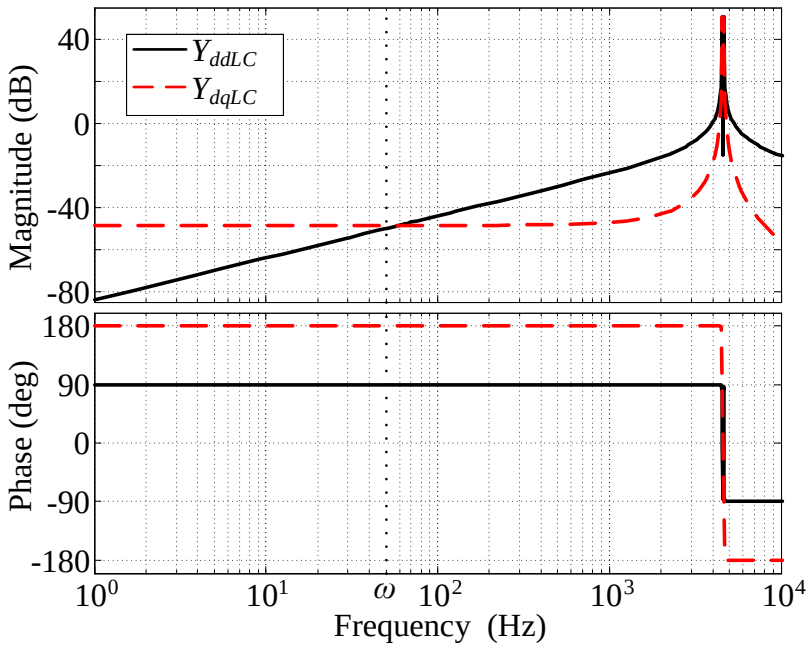
$$L_f s > L_f \omega \tag{7-25}$$

Obviously, $\mathbf{Z}_{\mathbf{dqLCAFE}}$ is diagonal dominant, then, $Y_{\mathbf{dqLCAFE}}$ is also diagonal dominant.

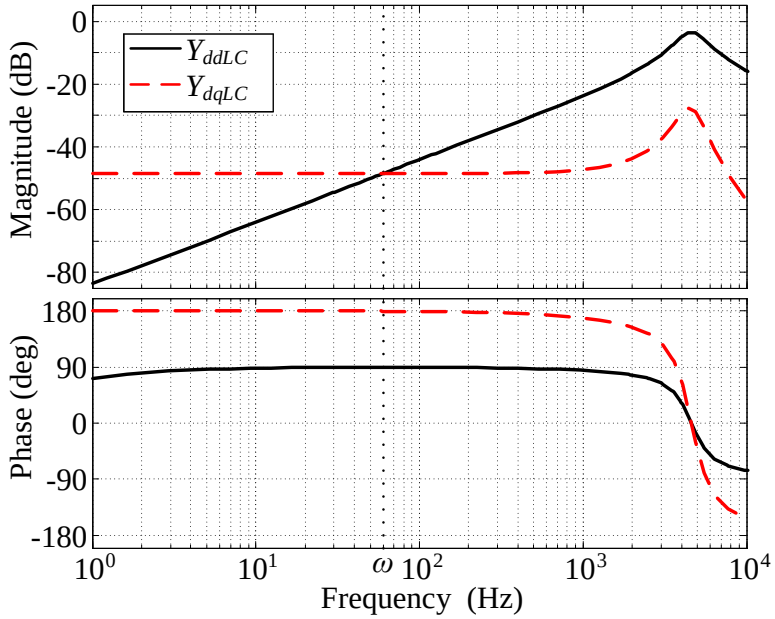
At high frequency, which bigger than 10 times of line frequency, the input admittance is determined by the admittance of *LC* filter. Similar to the discussion in the VSI section, the input admittances matrix is non-diagonal at the resonant frequency as shown in Fig. 7-14 (a). If series

damping resistor is added to the capacitor, the admittances matrix is shaped as diagonal dominant above the line frequency as shown in Fig. 7-14 (b).

Finally, Fig. 7-15 shows the magnitude of AFE input impedance with input filter and unity power factor. It shows that with input filter, $\mathbf{Y}_{\mathbf{dqLCAFE}}$ can be designed as diagonal dominant.



(a) Without damping.



(b) With damping

Fig. 7-14. *LC* filter input admittance.

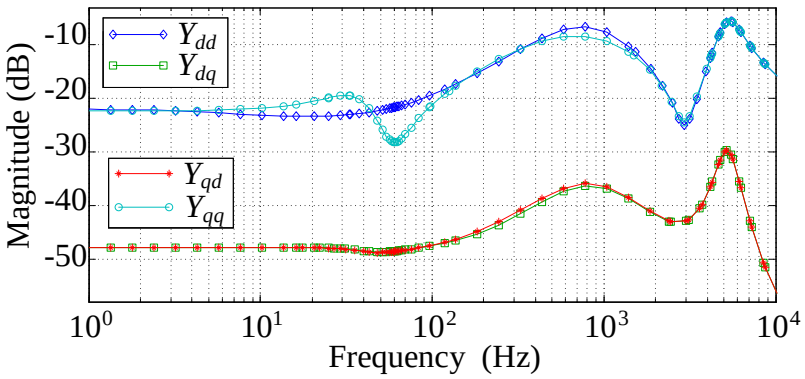


Fig. 7-15. AFE input impedance with input filter and unity power factor.

7.4 Experimental Results

Fig. 7-16 shows the circuit schematic and control system block diagram of the experimental setup where the VSI, AFE, and ac interface of interest are clearly identified. At this interface, the VSI closes its outer control loop regulating the ac bus voltage V_{VSI_ll}, from where the AFE draws

its current I_{AFE}. As such, the VSI output impedance $\mathbf{Z_{dqVVSI}}$ and the AFE input admittance $\mathbf{Y_{dqAFE}}$ seen at this interface are solely of each converter's parameters and do not depend on each other's components and control systems. Also, when performing the measurements this interface is a common coupling point fully accessible from the exterior of the VSI and AFE cabinets. The parameters of the system is list in Table 7-1 in the appendix.

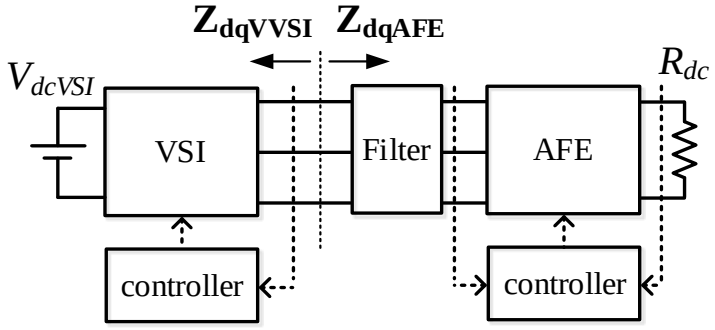


Fig. 7-16. Experimental system setup and control scheme.

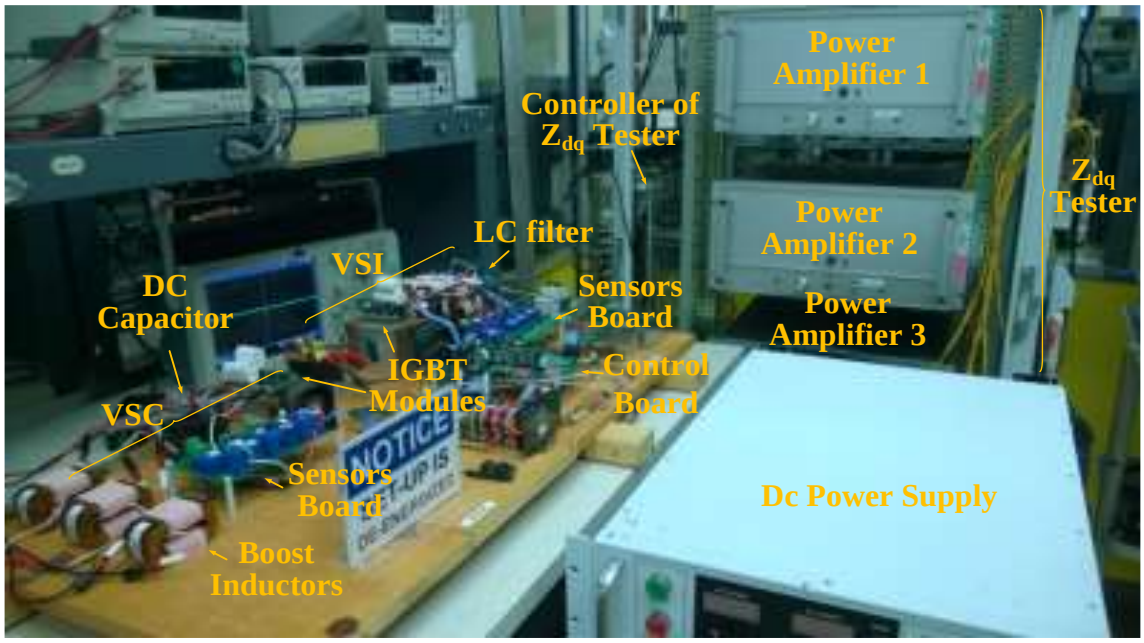


Fig. 7-17. Test-bed hardware prototype for experimental system

Using the test-bed hardware prototype shown in Fig. 7-17, experimental results of three cases are shown in this section.

The first experiments is VSI feeding AFE working under unity power factor condition. Fig. 7-18 shows the time domain test results, which indicates the system is stable. Fig. 7-19 shows the measured VSI output impedances, which shows the impedances matrix is diagonal. Fig. 7-20 shows the measured AFE input admittances, which shows the admittances matrix is diagonal. Fig. 7-21 shows the eigenvalue loci of minor loop-gain of the VSI feeding AFE system over plotted with *d* and *q* channel impedance ratios. Clearly, the first eigenvalue loci is equal to the *d* channel impedance ratio between VSI and AFE, the second loci is equal to the *q* channel impedance ratio between VSI and AFE.

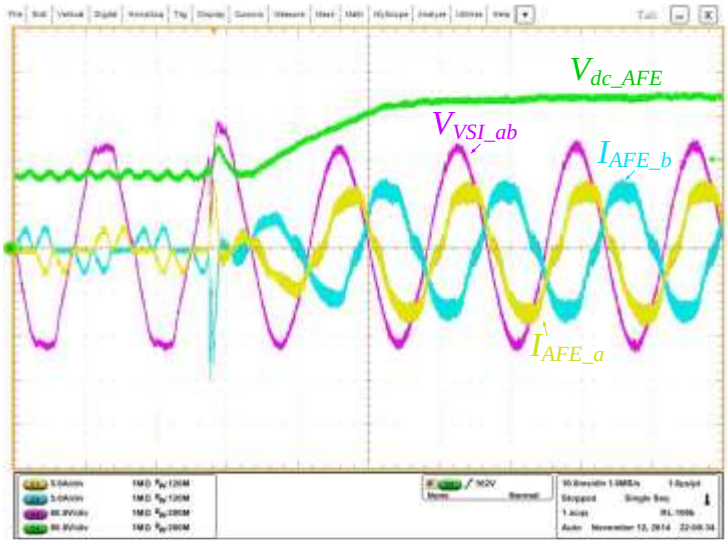


Fig. 7-18. Time domain test results of VSI feeding AFE with unity power factor.

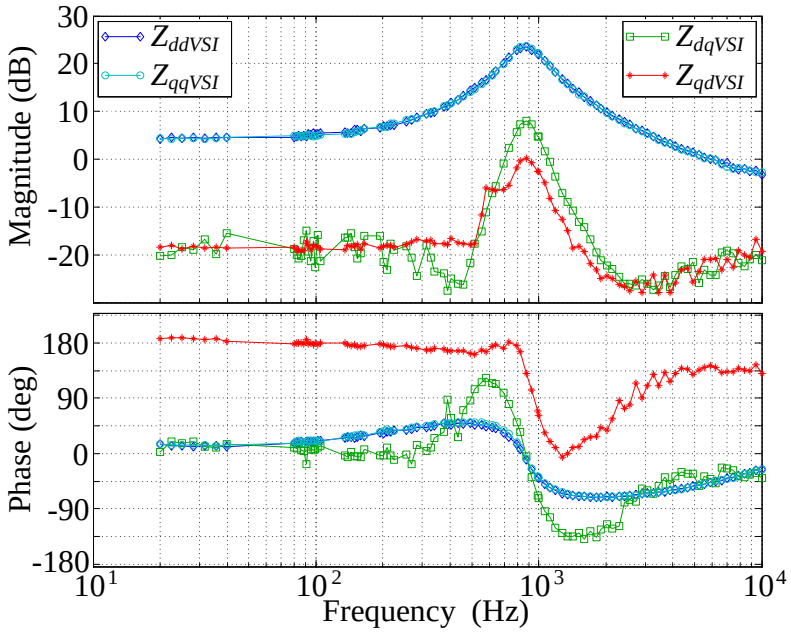


Fig. 7-19. Meausred VSI output impedances.

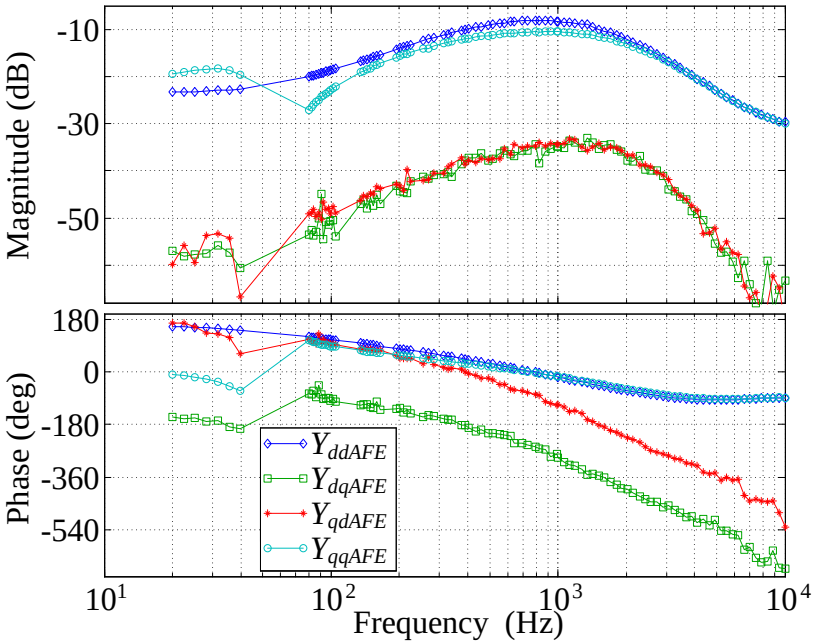


Fig. 7-20. Measured AFE input admittances with unity power factor.

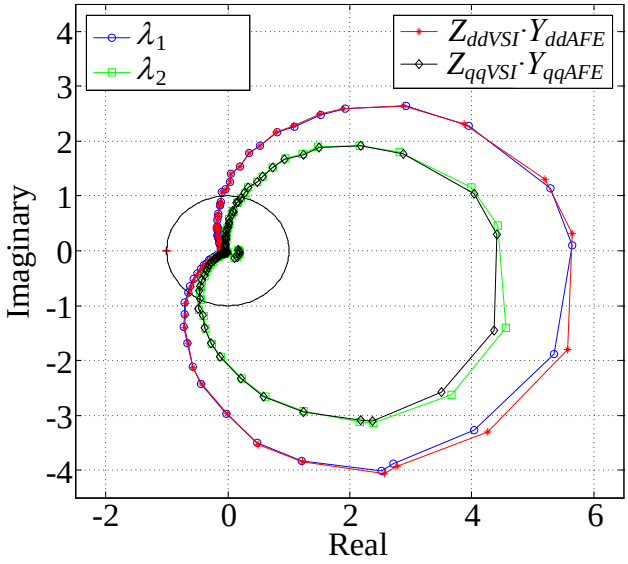


Fig. 7-21. Eigenvalue loci over plotted with impedance ratios.

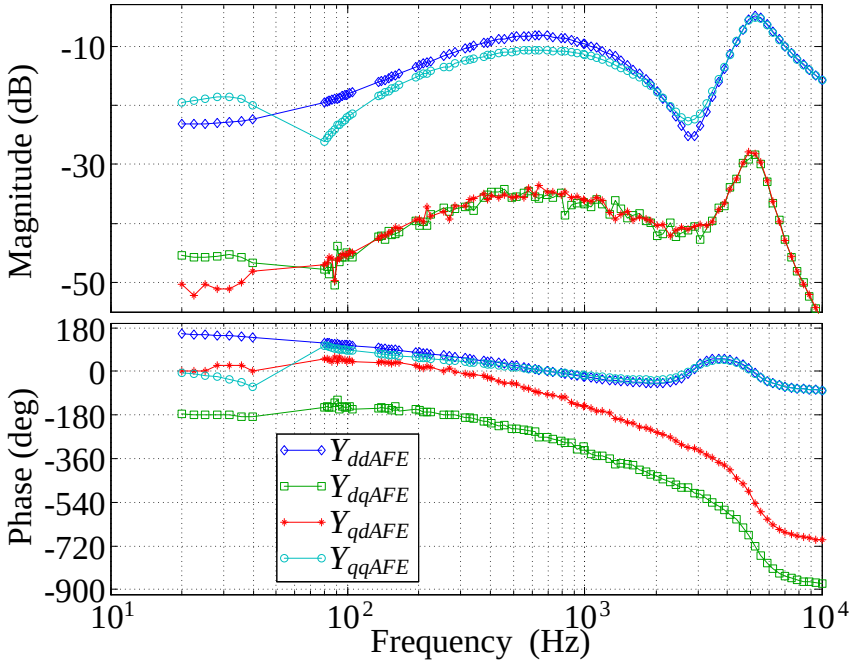


Fig. 7-22. Measured $\mathbf{Y_{dqAFE}}$ with input filter.

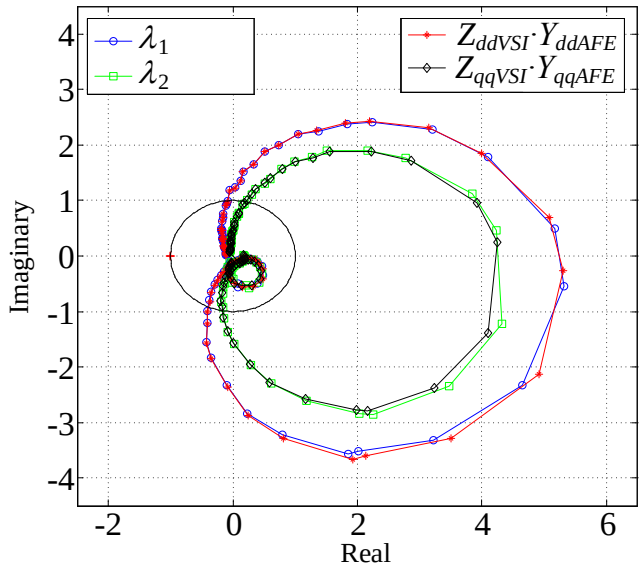


Fig. 7-23. Eigenvalue loci over plotted with impedance ratios with input filter.

The second test is AFE with input filter working under unity power factor condition.

Fig. 7-22 shows the measured AFE input admittances with input filter, which shows the system is also diagonal. Fig. 7-23 shows the eigenvalue loci of system minor loop-gain and *d* and *q* channel impedance ratios. The results also verify the analysis. These results indicate that when AFE working under unity power factor, system stability condition is directly judged by source and load impedances ratios in *d* and *q* channel. Three-phase ac system becomes two decoupled dc systems. Impedance specification methods that are developed in dc system can be applied to these two dc systems separately.

The third test is AFE working under non-unity power factor condition with I_q=90%I_d. Fig. 7-24 shows the measured input admittance of AFE, it shows the admittance matrix is not diagonal. Consequently, the eigenvalue loci of system minor loop-gain no longer equal to *d* and *q* channel impedance ratios. These results verify the proposed analysis in another direction.

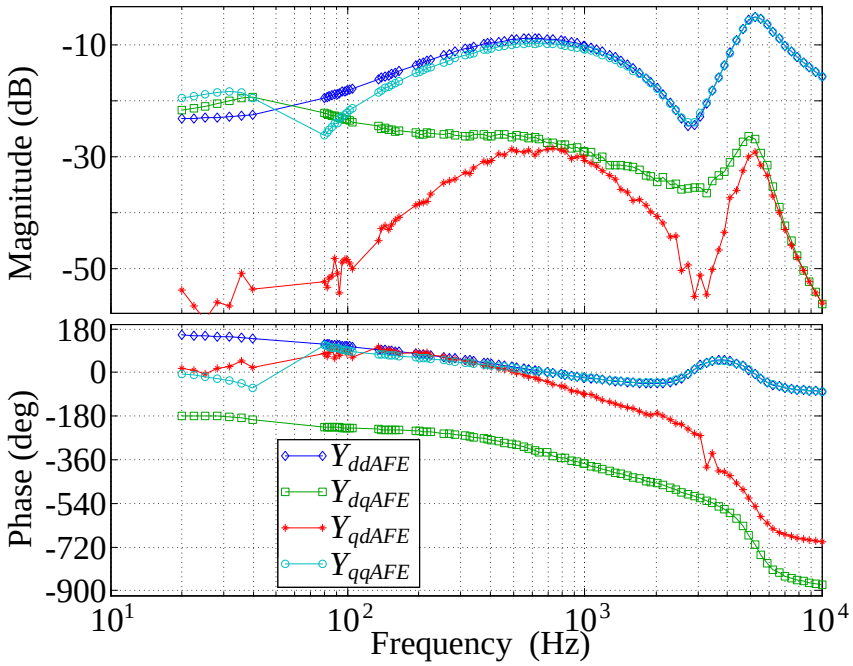


Fig. 7-24. Measured $\mathbf{Y_{dqAFE}}$ (I_q = 90%I_d).

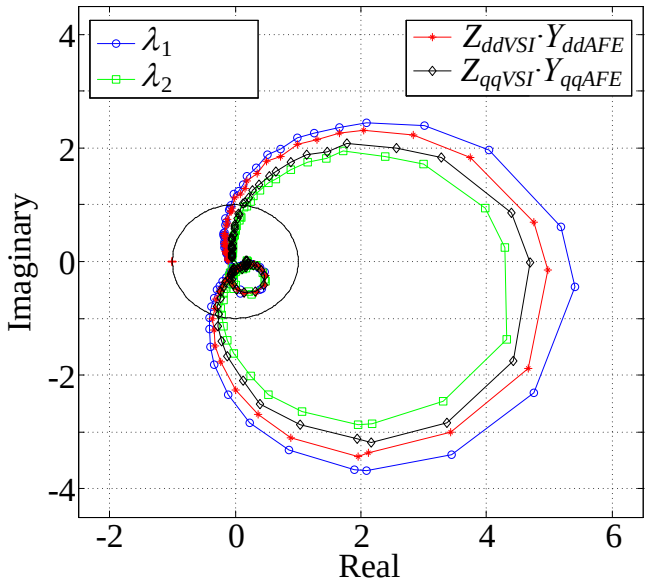


Fig. 7-25. Eigenvalue loci over plotted with impedance ratios (I_q = 90% I_d).

The fourth test is AFE working with more load and higher voltage control bandwidth, which makes the system less stable. The output voltage of AFE is increased to 320 V, the feedback controller parameters are also increased as shown in Table 7-2. shows the measured input

admittance of AFE with 320 V output voltage and higher voltage control bandwidth. The input admittance matrix is still diagonal. Y_{dd} shows extended range of negative resistance behavior compare to Test 1, which indicates the system Fig. 7-26 is less stable (with oscillation of 319 Hz) as shown in Fig. 7-27. As shown in Fig. 7-28, impedance ratio in *d* channel (Z_{ddVSI}*Y_{ddAFE}) indicates that system in Test 4 has less margin comparing with system in Test 1. These results validate the effectiveness and accuracy of using impedance ratios in *d* and *q* channel to predicate system stability condition.

Table 7-2. Parameters of Test System

Symbol	Description	Value
V_{dcAFE}	Dc voltage of AFE	320 V
k_{piAFE}	Proportional gain of AFE current controller	0.0098
k_{iiAFE}	Integrator gain of AFE current controller	19.635
k_{pvAFE}	Proportional gain of AFE voltage controller	0.2827
k_{ivAFE}	Integrator gain of AFE voltage controller	14.7262

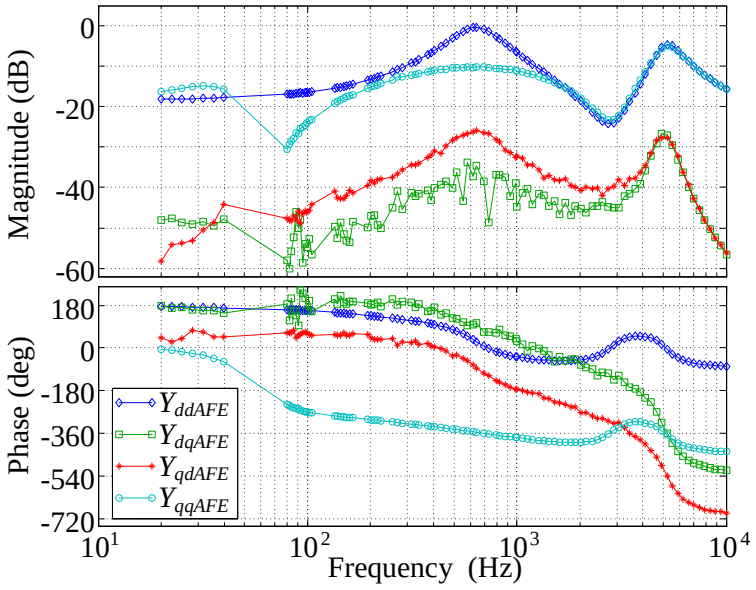


Fig. 7-26. Measured $\mathbf{Y_{dqAFE}}$ with V_{dc_AFE} = 320 V.

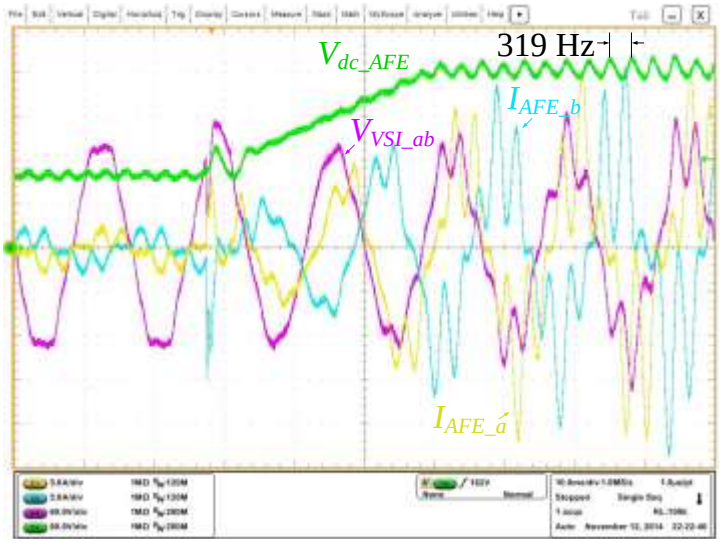


Fig. 7-27. Time domain test results of the system with V_{dc_AFE} = 320 V.

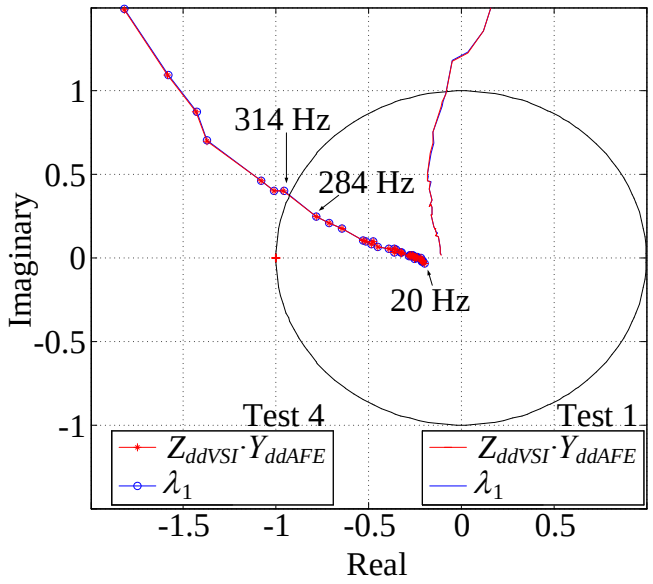


Fig. 7-28. Eigenvalue loci over plotted with impedance ratios for Test 1 and 4.

Chapter 8 Conclusions and Future Work

The impedance-based stability analysis has now been used for over 20 years in dc systems, having become an essential component of their design and integration. In effect, by using this method, system integrators can easily specify valid ranges for the impedance of components in order to ensure the system stability when using equipment from different suppliers. For ac systems however, this method is still not common practice. Accordingly, this research has strived to demonstrate the experimental accuracy of stability prediction in both frequency domain and time domain that can be attained in ac systems when using this approach. This has the potential to enable the use of impedance specification as a design tool for future ac systems. To this end, an experimental setup comprised of a voltage source inverter acting as ac source, and a three-phase boost rectifier acting as constant power load, was built. Three experiments were then conducted and analyzed, showing stable, critical stable, and unstable conditions by adjusting the control bandwidth of the source converter—modifying its output impedance. The corresponding ac impedances in the *d-q* frame of both source and load subsystems were then measured, and the Generalized Nyquist stability Criterion (GNC) was applied, showing how both stable and unstable conditions could be effectively predicted and verified using this approach. Time domain and frequency domain waveforms and plots were used to illustrate this.

This research also presents an analysis of grid-tied inverter small-signal impedance in *d-q* frame under different control strategies. Influences of PLL, current and power feedback control to the inverter impedance are discussed. Some important features of inverter impedance are discussed. These features indicates that grid-tied inverter working as current source could destabilize the system due to the negative incremental resistor of Z_{qq}. This negative incremental resistor behavior is a results of PLL. Increasing of PLL bandwidth extends the frequency range of this behavior. Increasing of inverter power level decreases the absolute value of the resistor. A brief simulation example shows that under weak grid condition, a small increase of the PLL bandwidth could lead the system to unstable condition. The example also shows how the proposed model can be used to predict such instability. Hardware measurements verify the proposed model. The model gives insight of the grid-tied inverter behavior in the grid. Harmonic

resonance and instability issues reported in the literature can be analyzed using the characterized impedance model.

Then this research proposes an impedance-based analysis method to analyze the grid-synchronization stability issue in paralleled three-phase converter systems including grid-tied inverter, active front end rectifier, local passive load, and grid impedance. The proposed method shows that the multi-variable GNC and GINC can be used to predict the system stability based on the grid and inverter impedances in the synchronous *d-q* frame. Furthermore, the instability is found to be caused by *q* channel impedance interaction. Experimental results verify the analysis and the proposed method.

Impedance-based analysis for active frequency drift islanding detection methods is also discussed in this disseration. To do the analysis, the output impedance of a grid-tied inverter was modeled with PLL-based AFD method. The Z_{qq} of the grid-tied inverter output impedance features a negative incremental impedance. Since a grid-tied inverter *q* channel impedance magnitude is equal to the dc impedance magnitude of the local load, impedance interaction happens when islanding event happens. With big feed forward gain *N* for islanding detection, the phase of Z_{qq} is shown to drop below $-180\,°$. Under islanding condition, the inverter system became unstable with a frequency drift away from steady-state. Based on the impedance of the inverter, it could be concluded that the grid-tied inverter with AFD islanding method has the potential to destabilize the grid-connected inverter system when the grid is weak. Experimental results verified the analysis.

Finally, an attempt to do load impedance specification for three-phase ac system is presentated. The research first reviewed impedance-based small-signal stability analysis of dc distributed power system. It is well known that stability margin and forbidden region can be defined for dc system to ensure small-signal stability. Load impedance specification can also be defined which greatly helps the system integration for dc system. Small-signal stability of balanced three-phase ac system can be predicted using source and load impedance in *d-q* frame, similar stability margin and load impedance specification cannot be done because of the MIMO system coupling in three-phase ac system. This research found that when three-phase ac system

working under high power factor condition, which is the case for power electronics interfaced distributed power system for micro-grid, more electric aircraft and ship, system could be decoupled in *d*-*q* frame. Then ac system becomes two independent dc systems. Load impedance specification can be done separately for *d* and *q* channel as two dc systems. Limitation of the proposed method is system should working under nearly unity power factor condition. Simulation and measurement are used to verify the analysis.

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