Heterogeneous Integration of III-V Multijunction Solar Cells on Si Substrate: Cell Design & Modeling, Epitaxial Growth & Fabrication

Nikhil Jain

Dissertation submitted to the faculty of the Virginia Polytechnic Institute and State University in partial fulfillment of the requirements for the degree of

Doctor of Philosophy
In
Electrical Engineering

Mantu K. Hudait, Chair
Luke F. Lester
Marius K. Orlowski
Jean J. Heremans
Paul E. Plassmann

March 27, 2015
Blacksburg, VA

Keywords: III–V-on-Si solar cells, multijunction solar cells, heterogeneous integration, solar cell modeling, GaAs-on-Si epitaxy, Ge-on-Si epitaxy.

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ABSTRACT

Achieving high efficiency solar cells and concurrently driving down the cell cost has been among the key objectives for photovoltaic researchers to attain a lower levelized cost of energy (LCOE). While the performance of silicon (Si) based solar cells have almost saturated at an efficiency of ~25%, III-V compound semiconductor based solar cells have steadily shown performance improvement at approximately 1% (absolute) increase per year, with a recent record efficiency of 46%. However, the expensive cost has made it challenging for the high efficiency III-V solar cells to compete with the mainstream Si technology. Novel approaches to lower down the cost per watt for III-V solar cells will position them to be among the key contenders in the renewable energy sector. Integration of such high-efficiency III-V multijunction solar cells on significantly cheaper and large area Si substrate has the potential to address the future LCOE roadmaps by unifying the high-efficiency merits of III-V materials with low-cost and abundance of Si. However, the 4% lattice mismatch, thermal mismatch polar-on-nonpolar epitaxy makes the direct growth of GaAs on Si challenging, rendering the metamorphic cell sensitive to dislocations.

The focus of this dissertation is to systematically investigate heterogeneously integrated III-V multijunction solar cells on Si substrate. Utilizing a combination of comprehensive solar cell modeling and experimental techniques, we seek to better understand the material properties and correlate them to improve the device performance, with simulation providing a very valuable feedback loop. Key technical design considerations and optimal performance projections are discussed for integrating metamorphic III-V multijunction solar cells on Si substrates for 1-sun and concentrated photovoltaics. Key factors limiting the “GaAs-on-Si” cell performance are identified, and novel approaches focused on minimizing threading dislocation density are discussed. Finally, we discuss a novel epitaxial growth path utilizing high-quality and thin epitaxial Ge layers directly grown on Si substrate to create virtual “Ge-on-Si” substrate for III-V-on-Si multijunction photovoltaics. With the plummeting price of Si solar cells accompanied with the tremendous headroom available for improving the III-V solar cell efficiencies, the future prospects for successful integration of III-V solar cell technology with Si substrate looks very promising to unlock an era of next generation of high-efficiency and low-cost photovoltaics.

Dedication:

1. My always inspiring and loving parents (Monica and Saurabh Jain) and my grandparents (Usha & R.B. Jain, Rani & Jagdish Jain).
2. My caring and beautiful wife, Apoorva Vasan, my brother and sister-in-law (Vinay & Megha Jain).
3. To my future children - I wish they can find the same curiosity, passion and love for a field as I had the fortune to experience.
4. To all the amazing people who share the dream for a better, cleaner, safer and a more peaceful tomorrow.

ACKNOWLEDGMENT

As I start to write my PhD dissertation, I look back in time and I'm reminded about my truly amazing experience at Virginia Tech over the last four and a half years. The graduate school journey has not only given me a solid academic foundation, but has also prepared me to face challenges across all the facets of life. The ability to think critically, working in teams on collaborative projects and dealing with experimental failure on numerous occasions have taught me the important skills of perseverance and determination. The journey has been truly worthwhile, both at the professional and personal front.

First and foremost, I would like to sincerely thank my adviser, Dr. Mantu Hudait for giving me the opportunity to pursue my PhD under his mentorship. We have been extremely fortunate as members of the ADSEL group to have Dr. Hudait available almost 24/7 to discuss our doubts and brainstorm new ideas. I am really thankful to him for giving me the freedom to explore and pursue new research directions. I would also like to thank the members on my committee: Prof. Luke Lester, Prof. Marius Orlowski, Prof. Jean Heremans and Prof. Paul Plassmann for their guidance and research direction.

Joining the ADSEL group as the first student and seeing the group grow and advance has been exciting. The challenges and learning that came being among the first students in the group has been really satisfying. The experience gained during setting-up the MBE growth facility, developing a dislocation-dependent modeling capability, installing the I-V/QE equipment and developing cleanroom fabrication process from scratch has been really rewarding. I want to express my sincerest thanks to all the ADSEL group members – Yan Zhu, Michael Clavel, Patrick Goley, Jheng-Sin Liu and Peter Nguyen for their help and support during this research. I specially thank Michael Clavel for giving me company during wafer fabrication and later for being my MBE growth companion and for putting in endless hours towards the end of my PhD to make sure my work is finished on time. Also, a special thanks to Yan for being my growth mentor in the initial days and Patrick Goley for helping out with TEM. I would also like to extend my sincere thanks to the following people -

1) Don Leber for his enormous help during MBE chamber installation and for cleanroom training.
2) The team at Nanoscale Characterization and Fabrication Lab - Jerry Hunter, Stephen McCartney, Andrew Giordani and Christopher Winkler for help with material characterization studies.
3) The Crosslight team for all their help and support during this research.
4) The MBE team at Veeeco Instruments, Inc. - John, McDonough, Rich Bresnahan and Dana Johnson.

5) Andy Jackson at MBE control solution.
6) Kathy, Melanie, Kim, Cindy and Becky at the ECE department for all the administrative help.
7) A special thanks to Matthew Meitl and John Wilson at Semprius for being excellent mentors during my internship in Fall 2012.
8) Prof. K.C. Hsieh at University of Illinois at Urbana Champaign for instilling the passion for semiconductor research and Prof. J.J. Coleman for giving me the opportunity to conduct hands-on research during my undergrad.

I gratefully acknowledge the funding support from the Institute for Critical Technology and Applied Sciences, Virginia Tech and Naval Air Warfare Center Weapons Division. I would also like to thank all my teachers, family and friends who have supported me all through these years and helped me grow into a better individual. Thanks to Yash, Rahul, Sagar, Harjas, Saransh, Sudharshan, Adrian, Pallavi, Karl, Natasha, Raman, Naureen, Jaspreet, Aditya, Ankit, Rikin, Arun, Akshay, Gurtej, Siddhant, Akrit, Harris, Teju and Sean and the Virginia Tech Cricket Club for allowing me to have a life in Blacksburg outside Whittemore Hall. My friends from high school at DPS Mathura Road and my undergrad friends at Manipal & UIUC also played an important role towards shaping my career. A special thanks to Kay Luttrel and the pathfinders group at Blacksburg Baptish Church for providing an extremely important dimension to my life during the time at Virginia Tech.

Lastly, I would like to extend my sincere thanks to my entire family for their unconditional support, love and encouragement. During the PhD years at Virginia Tech year, my family lost a very dear and close member, my grandmother, Usha Jain. When I had first made the decision to pursue a PhD, she was the most delighted person in my family and always encouraged me to dream big. I thank my father, Saurabh Jain for being extremely supportive and for his guidance along every facet of life and my mother, Monica Jain for teaching me to be humble and content, but at the same be always hungry to seek improvement. A special thanks to my brother, Vinay Jain and his wife, Megha Jain for their love and support and for keeping the family knitted together. I am also very grateful to my wife, Apoorva and the new Vasan family. I thank Apoorva for being my pillar of support and strength and for all the countless sacrifices she's made for our relationship. I have been fortunate to have her by my side as a constant source of encouragement.

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Chapter 1

INTRODUCTION

Publication for Section 1.2

N. Jain and M. K. Hudait (Invited Review), "III-V Multijunction Solar Cell Integration with Silicon: Present Status, Challenges & Future Outlook", *Energy Harvesting and Systems*, 1 (3-4), pp. 121-145, 2014.

In this chapter, we discuss the current progress in the development of III-V multijunction solar cell and towards their integration onto Si substrate. The current state-of-the-art for III-V-on-Si solar cells along with their theoretical performance projections are presented. Next, the key design criteria and the technical challenges associated with the integration of III-V multijunction solar cells on Si are reviewed. Different technological routes for integrating III-V solar cells on Si substrate through heteroepitaxial integration and via mechanical stacking approach are discussed. The key merits and technical challenges for all of the till-date available technologies are summarized. With the plummeting price of Si solar cells accompanied with the tremendous headroom available for improving the III-V solar cell efficiencies, the future prospects for successful integration of III-V solar cell technology onto Si substrate looks very promising to unlock an era of next generation of high-efficiency and low-cost photovoltaics.

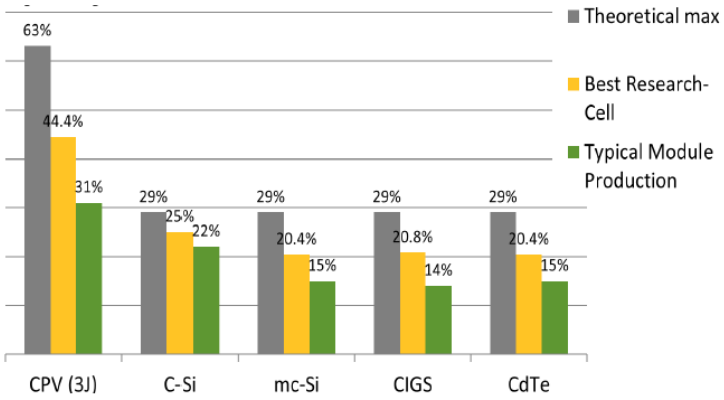

Fig. 1: Gap between theoretical and best research cell efficiencies along with the performance of commercially available modules for different solar cell technologies. The graph clearly indicates the headroom available to improve the performance of III-V based solar cells (CPV-3J) [**2**]. Used under fair use, 2015.

1.1 Overview of III-V Solar Cell Technology

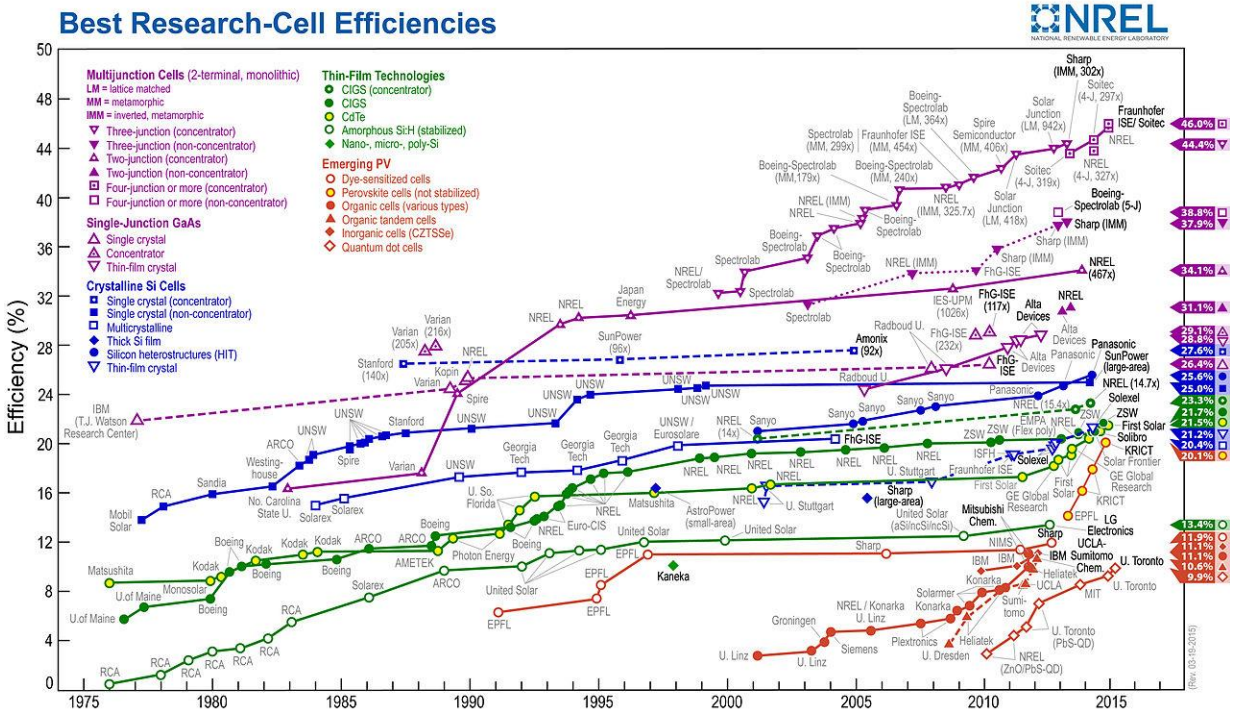

Fig. 2: The evolution of various solar cell technologies over the last 40 years [**1**]. Used under fair use, 2015.

III-V compound semiconductor based multijunction solar cells have been the most successful technology for delivering the highest photovoltaic conversion efficiency among all other competing photovoltaic technologies, as shown in **Fig. 1**. The gap between theoretical and best research cell efficiencies along with the performance of commercially available modules for different solar cell technologies is shown in **Fig. 1**. The graph clearly indicates a tremendous headroom available to further boost the performance of III-V based solar cells utilizing concentrated photovoltaic (CPV) technology. Unlike silicon, the III-V compound semiconductor materials provide the flexibility to realize multiple solar cells stacked on top of each other following same crystal lattice. The flexibility in band-gap selection for III-V materials provides an unprecedented degree of freedom in solar cell design through metamorphic or lattice-matched configurations based, allowing to achieve efficiencies reaching 46% in multijunction configuration under concentrated sunlight [**1**], while the performance of single-junction (1J) Si solar cells has saturated at ~25% and almost reaching the theoretical maximum as shown in **Fig. 2.** There has been almost 40-50% reduction in the PV system cost over the last 4-5 years and to be on track with the Department of Energy's SunShot goals beyond 2020, significant reduction in the PV system cost would be required to increase market share of renewable and clean solar energy, as shown in **Fig. 3**. With the performance of Si based solar cell almost

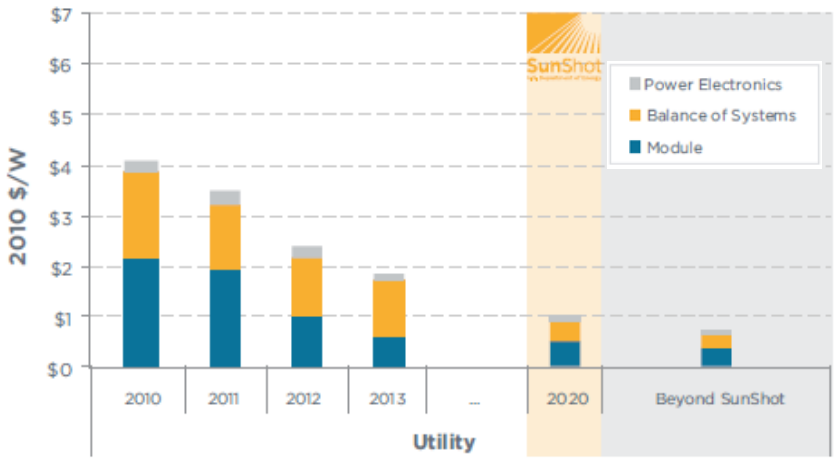

Fig. 3: The evolution of the PV system cost with component costs breakdown. The SunShot targets and beyond SunShot milestone are also indicated in the graph [**5**]. Used under fair use, 2015.

saturating, new avenues for high-efficiency solar cell technologies will be sought in the future (especially beyond 2020) to address the cost per watt. Thus, providing a remarkable opportunity for high-efficiency III-V solar cell technology. Novel approaches for reducing the cost of III-V solar cells with strong focus on economy of scale through higher production volume will be critical for III-V technology to compete with existing and new technologies.

The highest efficiency achieved from lattice-matched thin film 1J GaAs and 2J InGaP/GaAs solar cells are 28.8% and 31.1%, respectively at 1-sun [**1**]. A record efficiency of 34.1% at 467 suns has been demonstrated for the 2J InGaP/GaAs cell on GaAs substrate [**1**]. Utilizing Ge (band-gap = 0.67eV) as the bottom subcell in a lattice-matched 3J solar cell configuration, cell efficiency in excess of 40% was demonstrated for the first time by King et al [**3**]. In search for 1eV bottom subcell, the most commonly followed path initially was the integration of 1eV metamorphic InGaAs solar cell in the 3J solar cell configuration with lattice-matched InGaP and GaAs as the top two subcells [**4**]. To gain additional performance benefits, the InGaAs cell was grown the last in an inverted configuration and this approach is commonly known as inverted metamorphic or IMM approach [**4**]. This IMM approach lead to an efficiency of 40.8% which utilized two metamorphic InGaAs subcells with band-gaps of 1.34eV and 0.89eV as the bottom two subcells in the 3J solar cell configuration and such IMM 3J solar cells have now attained an efficiency of 44.4% at 302 suns, which stands the highest efficiency achieved using triple junction solar cells. [**1**]. With recent development in the dilute nitride based III-V materials, high quality 1eV InGaAsN alloys have been made possible by molecular beam epitaxy [**6**]. Dilute nitride based solar cells utilizing InGaP (1.9eV)/ GaAs (1.4eV)/ InGaAsN (1eV) cell architecture have reached record efficiency of 44% under concentrated sunlight of 947 suns [**6**]. Although, four-junction (4J) III-V based solar cells have been under research for a few years now,

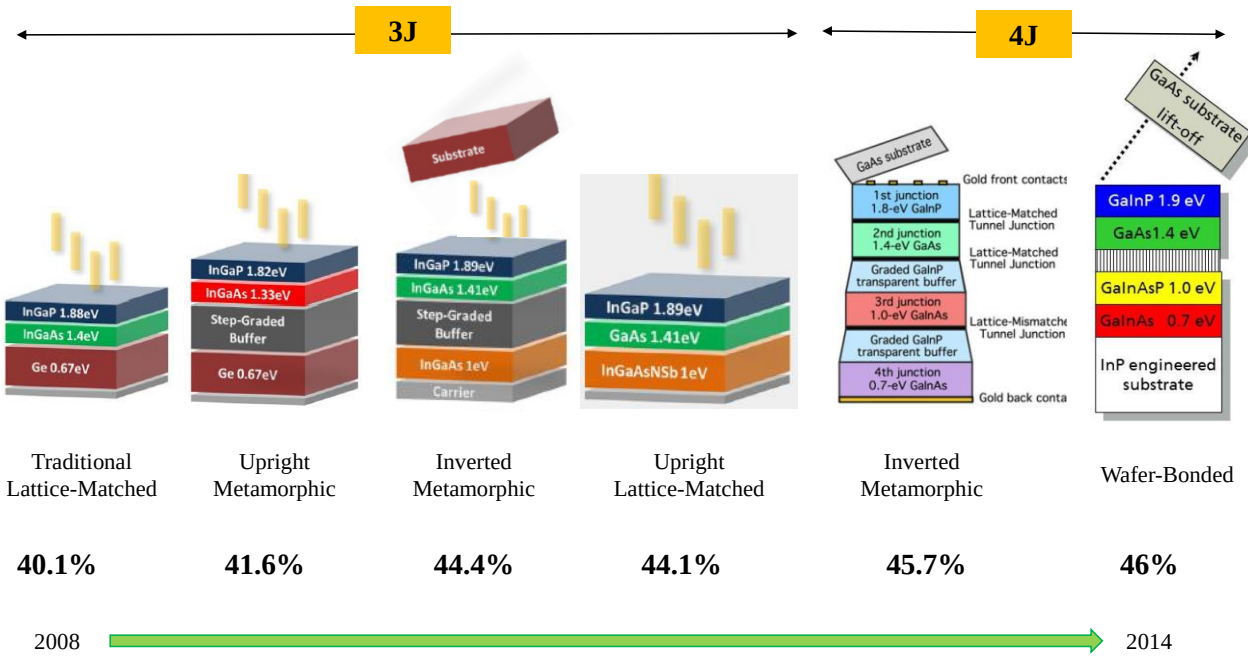

Fig. 4: Progress of III-V solar cell technology in the last 6 years [**1, 3, 7-10**]. [**1, 8, 10**] Used under fair use, 2015. [**3**] Used with permission from APL, 2007; [**7**] used with permissioned from Progress in Photovoltaics, 2015; [**9**] used with permission from IEEE, 2015.

only recently their true potential has become visible to surpass the performance of 3J solar cells. Four-junction solar cells become more challenging due to multiple metamorphic growths, tunnel-junctions and the ability to grow and connect high-quality individual four-junctions. Utilizing the IMM-approach, NREL has added an additional 0.7eV fourth junction (bottommost cell), which is grown last during the IMM solar cell growth. An efficiency of 45.7% under 234 suns was achieved using this approach utilizing GaInP (1.8eV)/ GaAs (1.4eV)/ GaInAs (1eV) / GaInAs (0.7eV) solar cells [**1**]. Researchers from Fraunhofer Institute leveraged almost similar band-gap combination but utilizing all lattice-matched growth. Dual-junction GaInP (1.88eV)/GaAs (1.42eV) solar cells grown on GaAs substrate were removed from the parent GaAs substrate and wafer-bonded onto dual-junction GaInAsP (1.12eV)/GaInAs (0.72eV) solar cells which were grown lattice-matched on InP substrate. Such wafer-bonded 4J solar cells hold the current world record among all kind of solar cells at 46% under 508 suns [**7**]. **Fig. 4** shows the progress of III-V solar cell technology in the last 6-7 years showing different approaches utilized to advance the state-of-the-art. Furthermore, it can also be inferred the technology is shifting from 3J solar cells to 4J solar cells to achieve further gain in performance. **Fig. 5** shows the performance dependence of multijunction solar cells with increasing number of junctions, indicating 4J efficiencies exceeding 50% should be achievable in the near future. In spite of achieving the highest conversion efficiency amongst all the competing photovoltaic technologies, their expensive cost has been the biggest impediment in their large scale deployment for

terrestrial applications. Thus, successful integration of III-V solar cells on Si substrate can offer a great promise for lowering the future levelized cost of energy by unifying the high efficiency merits of the III-V materials with the low-cost and abundance of the Si substrate.

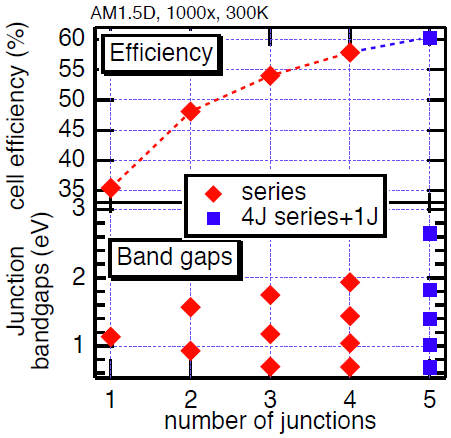

Fig. 5: Performance dependence of multijunction solar cells with increasing number of junctions, indicating efficiencies exceeding 50% should be achievable using four junctions [**11**]. Used under fair use, 2015.

1.2 Motivation for III-V-on-Si Solar Cells

III-V compound semiconductor based multijunction solar cells have been the most successful technology for delivering the highest photovoltaic conversion efficiency for space power applications. In spite of achieving the highest conversion efficiency amongst all the competing photovoltaic technologies, their expensive cost has been the biggest impediment in their large scale deployment for terrestrial applications. The performance of single-junction (1J) Si solar cells has almost saturated at ~25%, with the most recent accomplishment of 25.6% efficiency taking more than 15 years for an absolute 0.6% improvement in efficiency [**1**]. Interestingly, III-V solar cells have steadily shown performance improvement at approximately 1% (absolute) increase in efficiency per year [**2**], with the most recent world record efficiency of 44.7% at 297 suns for a four-junction III-V solar cell [**1**]. However, the dominance of silicon solar cells and their plummeting prices in the recent years have made it challenging for high efficiency III-V solar cells to make a strong commercial impact.

One of the most significant cost contributors to the bill of materials for III-V solar cells is the cost of the starting substrate. Typically, GaAs or Ge substrates are used for III-V multijunction solar cell growth, which are not only smaller in diameter, but are also significantly more expensive than the Si substrate. Successful integration of III-V solar cells on Si substrate can offer a great promise for lowering the future levelized cost of energy by unifying the high efficiency merits of the III-V materials with the low-cost and abundance of the Si substrate. In addition to the substantial cost benefits associated with the larger-area, and low-cost of Si substrate, Si also offers higher thermal conductivity and superior mechanical strength in comparison to GaAs or Ge substrates. III-V multijunction solar cell integration on Si substrate could potentially use the starting Si substrate as an active bottom subcell or perhaps just as an inactive starting template. With a bandgap of 1.12 eV, Si substrate is a better bottom cell candidate in comparison to Ge substrate (bandgap - 0.67 eV) for integration with standard dual junction (2J) InGaP/GaAs based multijunction solar cells in regards to current-matching [**4**]. Such triple-junction (3J) InGaP/GaAs//Si solar cells (monolithically or mechanically stacked) are likely to be the quickest path for high efficiency III-V-on-Si solar cells [**3**] with theoretically efficiency in excess of 40% at AM1.5g and AM1.5d [**4, 5**]. A recent study has revealed that transitioning from a 4" Ge substrate to an 8" Si substrate would correlate to about 60% reduction in cost for multijunction solar cells [**6**]. When utilizing Si as an inactive starting template, III-V-on-Si technology could leverage commercially available substrate re-use techniques such as spalling [**7**] and epitaxial lift-off [**8**] to explore additional cost savings schemes. The research on integrating III-V compound semiconductor materials on Si substrate for photovoltaic application was initiated in 1980s. However, the complexity associated with the material growth, reliability and reproducibility led to decline in the research for III-V-

on-Si solar cells in the late 1990s. In the last 5-6 years, III-V-on-Si solar cell research has re-gained attention pertaining to the research on new metamorphic buffer approaches, wafer bonding and mechanical stacking techniques. With the declining cost of Si combined with the impressive headroom available for improving the performance of III-V solar cells, future prospects for successful integration of III-V solar cell technology on Si substrate looks very promising.

1.3 Design Criteria & Integration Challenges for III-V-on-Si Solar Cells

There are two key approaches for integrating III-V multijunction solar cells on Si substrate: (i) heteroepitaxial growth (or monolithic) and (ii) mechanical stacking (and wafer-bonding). The terms mechanical stacking and wafer-bonding will be used interchangeably in this chapter. The following section reviews the key design criteria and technical challenges associated with both of these integration approaches.

1.3.1 Heteroepitaxial Integration

Heteroepitaxial integration approach is believed to be a very promising path to integrate high-efficiency III-V solar cells onto Si substrate owing to the utilization of single substrate and single epitaxial process. Lattice-matched 2J InGaP/GaAs solar cells have been the key building block for today's most efficient 3J and quadruple junction (4J) III-V solar cells, with GaAs being predominantly used as the starting substrate. Hence, integration of GaAs on Si substrate was the initial and the natural choice for realizing a "GaAs-on-Si" virtual platform for the subsequent multijunction solar cell growth [**9-11**]. More recently, approaches involving metamorphic graded buffers such as GaAsP and SiGe have gained a lot of attention for III-V/Si tandem solar cells [**12-16**]. Additional heteroepitaxial integration approaches, which in comparison to the previously mentioned techniques have been less extensively explored include – (i) lattice-matched dilute nitride (GaAsPN) solar cells on Si substrate [**17-19**] and (ii) lattice-mismatched InGaN based solar cells [**20-22**] on Si substrate. The most critical challenges associated with heteroepitaxial integration of III-V materials on Si substrate are highlighted below:

1.3.1.1 Growth of lattice-mismatched III-V materials on Si substrate

The 4% lattice-mismatch between GaAs and Si makes the direct epitaxy of GaAs on Si extremely challenging, resulting in the formation of defects and dislocations such as threading dislocations and misfit dislocations. Such defects and dislocations have a detrimental impact on the minority carrier lifetime and hence the solar cell performance. The most noteworthy techniques which have been employed for direct

GaAs epitaxy on Si to reduce the threading dislocation density (TDD) include (i) the thermal cycle annealing (TCA) [**23, 24**] and (ii) the low temperature and low growth rate process during the initial GaAs nucleation on Si [**9, 22-25**]. Growing thicker GaAs buffers have also been shown to facilitate dislocation reduction [**9**] but adds to the overall cost and time of the epitaxial process. Additionally, thin strained layers and superlattices introduced into the bulk GaAs buffer have been shown to facilitate the annihilation of TDs and minimize the dislocation propagation into the active layers of interest. Such an approach led to one of the highest efficiencies for heteroepitaxial 1J GaAs-on-Si solar cells [**42, 47**]. More recent approaches involve the growth of metamorphic graded buffers (e. g., SiGe, GaAsP) to bridge the lattice-constant between the Si and GaAs (or GaAsP) [**12-16**]. One of the most successful approaches in regards to dislocation reduction has been the utilization of graded SiGe buffers, however such buffers are very thick and their low bandgap precludes the use of the Si substrate as an active bottom cell. The larger bandgap of GaAsP buffers could circumvent the problem of utilizing the Si substrate as an active subcell. Among the various heteroepitaxial approaches employed for III-V-on-Si epitaxy, the SiGe graded buffer [**13**] and the direct GaAs on Si epitaxial approach involving strained layer superlattices [**23**] have reported the lowest TDD ~ $1x10^6$ cm^{-2}. Further dislocation reduction to ~ $1x10^5$ cm^{-2} would enable the GaAs-on-Si solar cells to compete with lattice-matched GaAs-on-GaAs solar cells.

1.3.1.2 Heteroepitaxy of polar III-V materials on non-polar Si substrate

Growth of compound semiconductors (e.g., GaAs) on monoatomic semiconductors (e.g., Si, Ge) results in the formation of antiphase domains (APDs) which are structural defects generated due to heteroepitaxy of polar material (GaAs) on non-polar materials (Ge or Si). The (001) surface of Si substrate consists of monoatomic steps in which Si atoms are arranged in the form of dimers oriented in perpendicular directions across two adjacent steps. During the initial stage of GaAs-on-Si growth, the arsenic dimers follow the dimer orientations of the underlying Si layer and orient themselves in perpendicular directions across the adjacent steps leading to the formation of As-As or subsequent Ga-Ga bonds, which initiates the formation of antiphase boundaries. Significant research has been devoted to minimize the formation of antiphase domains. Utilization of offcut Si substrates (4˚-6˚) with double-layer step formation with the adjacent Si-Si dimers in identical orientation facilitates similar trend for the subsequent GaAs, thus minimizing the formation of APDs [**25**].

1.3.1.3 Thermal-mismatch between III-V materials and Si substrate

The inherent difference in the thermal expansion coefficient ($5.73x10^{-6}$ $°C^{-1}$ for GaAs and $2.6x10^{-6}$ $°C^{-1}$ for Si) and the lattice-mismatch between GaAs and Si leads to residual strain in the films. This could lead to

the formation of defects and dislocations through lattice strain relaxation which could result in poor crystalline quality. The defects and dislocations are primarily categorized into antiphase domains, misfit and threading dislocations, twinning and stacking faults. One of the major concerns regarding the thermal mismatch is the generation of microcracks in the GaAs epitaxial layer which could pose serious problems related to solar cell reliability besides limiting the device area and performance. Faster sample cooling rate promotes microcrack formation, hence it is extremely important to control the cooling rate to minimize the microcrack density. Continued investigations to better understand the correlation between thermal mismatch and solar cell characteristics would be essential to validate the reliability and long-term robustness for GaAs-on-Si solar cells.

1.3.1.4 Buffer design – thickness, optical transparency, electrical conductivity & surface passivation.

An appropriate buffer selection is extremely critical for the success of III-V-on-Si solar cells. Optically transparent and thin buffer layers are desirable in order to utilize the starting Si substrate as an active cell, while the electrical conductivity of the buffer becomes more important for concentrated photovoltaic (CPV) to minimize series resistance. Most of the metamorphic graded buffer approaches utilize a thick buffer layer to bridge the lattice constant between the III-V's and Si. The lattice-matched dilute nitride buffers (GaAsPN) on Si and direct GaAs-on-Si buffers with strained layer superlattice are among the choices which could offer comparatively thinner heteroepitaxial buffers. In terms of optical transparency for active bottom Si substrate cell, wide bandgap GaAsP graded buffer would be a better choice than low bandgap SiGe buffers. Interestingly, the SiGe buffers could serve as active bottom subcell offering bandgap and lattice-constant tunability to allow integration with top GaAsP subcell for tandem cell designs [**15**]. An additional important buffer selection criteria is to utilize a layer which would provide a good surface passivation for the bottom Si subcell and serve as a window layer. Thus, there are important design trade-offs between the respective buffer selections in relation to minimizing the dislocation density while enabling thin and optically transparent buffers for utilizing Si substrate as an active solar cell.

1.3.2 Wafer Bonding & Mechanical Stacking

The approach of mechanical stacking for III-V-on-Si integration can accommodate large amount of lattice-mismatch and enable the integration of materials with ideal bandgap combination which are free from lattice-mismatch constraints unlike in heteroepitaxial growth approach. The most critical challenges associated with the mechanical stacking approach for integrating III-V materials and solar cell structures on Si substrate are highlighted below:

(i) Post-growth bonding approaches are favorable, otherwise the bond interface would go through the high temperature epitaxial growth process and could potentially suffer from thermal-mismatch between the III-V materials and Si leading to wafer bowing or cracking.

(ii) The bonding temperature must be compatible with the III-V materials and the Si substrate.

(iii) The bonding layer should be thin and optically transparent to allow the utilization of bottom Si substrate as an active subcell.

(iv) For two-terminal solar cell operation under concentrated sunlight, it is of critical importance to realize electrically conductive bond layers to avoid adding series resistance.

(v) The bonding interfaces should have low surface roughness and must be free from native oxides.

(vi) Viable III-V substrate removal and re-utilization process with high yield and high throughput.

In addition to the integration challenges associated with either the heterogeneous or the mechanical stacking approaches, the respective challenges for III-V and Si solar cell design are also very critical for successful III-V-on-Si integration.

1.3.3 III-V and Si Solar Cell Design Challenges

Si being an indirect bandgap semiconductor typically limits the overall current when integrated in tandem with conventional 2J InGaP/GaAs solar cells in 3J two-terminal configuration [**4, 5, 27, 28**]. Hence, the design of bottom Si subcell is extremely important for current-matching in tandem cell design. An additional important role of the initial III-V layer on Si is to serve as effective window layer, allowing sufficient optical transmission, surface passivation, majority carrier conduction and minority carrier reflection. Emitter formation in the Si substrate can be challenging and different approaches are being explored, such as in-situ epitaxial phosphorus diffusion [**28**], in-situ epitaxial growth of Si emitter [**29**], and ex-situ conventional diffusion. The in-situ phosphorus diffusion from the gas phase was found to be less intense for optimal junction formation in Si [**29**] translating to epitaxially grown or ex-situ diffused junctions being more efficient. Although, III-V/Si interface passivation is essential for subsequent III-V epitaxial growth, the influence of front surface recombination is not critical for multijunction designs, since the top III-V subcells would absorb most of the photons in the wavelength range which is affected by the III-V/Si interface, and only the high wavelength photons would reach the bottom Si subcell, hence a less severe impact on the short-circuit current density (J_{sc}) of Si solar cell. Thinner Si emitters are preferred to maximize both the open circuit voltage (V_{oc}) and J_{sc} when the interface recombination velocity (IRV) is low, however there is a strong trade-off between optimizing the V_{oc} and J_{sc} when the IRV is high [**31**]. For selecting the optimal doping in the emitter, lightly-doped Si emitter maximizes the V_{oc} when the IRV is low, while heavily doped emitter designs translate to higher V_{oc} when the IRV is high [**30**]. The most

important design criterion for utilizing Si as an active subcell with III-V subcells in a multijunction configuration, would be to engineer the backside of the Si substrate to enhance back surface reflection and achieve good surface passivation because Si subcell typically limits the current in III-V/Si tandem cell designs [**4, 27**]. Numerical simulations reveal that a silicon nitride passivation layer along with aluminum back reflector would provide substantial boost in quantum efficiency for higher wavelength regime of the spectrum and enable J_{sc} >14 mA/cm^2 in the bottom Si subcell for successful integration with III-V multijunction solar cells [**32**].

In terms of the III-V solar cell designs on Si, most crucial challenges are the reduction of TDDs and realization of high-quality solar cell materials with bandgap-voltage offset (W_{oc}) close to the radiative limit of 0.3-0.4 eV. The TDs act as recombination centers for minority carriers, thus degrading the minority carrier lifetimes. Higher dislocation density more adversely affects the V_{oc} than the J_{sc} in a solar cell. The major effect of TDs generated due to lattice-mismatch on the V_{oc} and fill-factor (FF) is attributed to the increased n = 2 reverse saturation current associated with bulk space-charge recombination due to the reduced minority carrier lifetime [**33, 37**]. Minimizing the lattice-mismatch induced defects and dislocations is expected to improve the minority carrier diffusion length and hence the overall solar cell performance. Realization of high quality tunnel-junction is also a major challenge for connecting new metamorphic solar cell materials such as SiGe, GaAsP, InGaP, GaAsPN, GaPN and InGaN for realizing tandem III-V/Si solar cells. An additional extremely important design aspect is the realization of the current-matching condition taking into account the impact of TDs in metamorphic multijunction solar cells. Careful consideration of all these design challenges would be very critical for the success of III-V multijunction solar cells on Si.

1.4 State-of-the-art III-V-on-Si Solar Cells

With the recent advancements in both heteroepitaxial and mechanical stacking integration approaches for III-V-on-Si solar cells, 3J GaInP/GaAs//Si solar cells have now achieved two-terminal efficiencies in excess of 27% (AM1.5d spectrum) under concentrated sunlight [**2**], with substantial headroom for further improvement. The best experimental results for III-V-on-Si solar cells are summarized in **Table I** along with the respective data for the solar cell figure-of-merits (efficiency (η), sun concentration, V_{oc}, J_{sc} and FF. Only two-terminal efficiencies are included in the **Table I**. A four-terminal GaAs-Si dual-junction solar cell with an efficiency of 31% under 347 suns AM1.5d was demonstrated in 1988 [**34**]. More recently, a spectral beam-splitting system utilizing independent 2J GaInP/GaAs, a Si and a GaSb solar cell achieved an efficiency of 34.3% under 1 sun AM1.5d [**35**].

The state-of-the-art results for III-V-on-Si solar cells are shown in **Fig. 6** along with the projected iso-efficiencies for series-connected 2J and 3J solar cells under respective incident solar spectrums. The projected efficiencies for 2J (yellow-dashes) and 3J (green-dashes) cells assume bandgaps of 1.7/1.1 eV and 1.8/1.4/1.1 eV, respectively [**36**]. Iso-efficiencies in **Fig. 6** were calculated assuming that the thickness of the top junction was optimized for each bandgap combination (Kurtz et al. 1990). The efficiency numbers in red represent results for III-V-on-Si mechanically stacked solar cells, while the numbers in blue represent the results for III-V-on-Si solar cells realized using heteroepitaxial integration. Although iso-efficiency results predict efficiencies in excess of 40% for 3J III-V on Si tandem solar cells [**4**], such analysis typically doesn't take into account the indirect bandgap of Si, the dislocation-dependent current-matching, dislocation dependent minority carrier lifetimes, surface recombination velocities and the tunnel junction design. Several groups have been investigating III-V-on-Si solar cell designs which provide more realistic performance projections taking into account the impact of dislocations and surface recombination velocities. Using finite element analysis, *Jain et. al.* showed that a 2J InGaP/GaAs solar cell on Si could achieve efficiency in excess of 29% (AM1.5g-1000 W/m^2, 1-sun) [**37**] and 33% (AM1.5d-900 W/m^2, 600 suns) [**38**] at a realistic TDD of 10^6 cm^{-2}. Using a similar finite element analysis modeling approach, *Brown et. al.* showed that an 2J InGaN/Si tandem cell could achieve an efficiency of 28.9% under AM1.5 illumination [**21**]. Triple-junction InGaP/GaAs//Si solar cells have also been numerically investigated as a function of TDD under 1-sun [**5, 26, 27**] and concentrated sunlight [**38**]. Efficiencies exceeding 33% seems

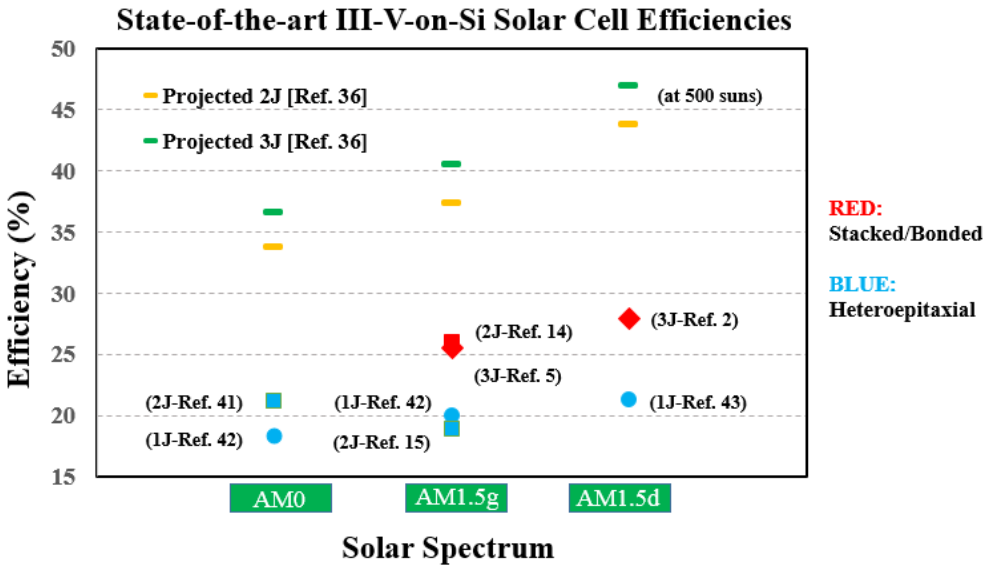

Fig. 6 Present state-of-the-art III-V-on-Si experimental solar cell results for AM0, AM1.5g and AM1.5d spectrum. The projected iso-efficiencies for 2J and 3J solar cells under the respective spectrums are shown in yellow and green, respectively. Results for both heteroepitaxial and mechanically stacked integration approaches are shown in blue and red, respectively. [**75**] Used with permission from EHS, 2014.

TABLE I

III-V on Si Solar Cells – State-of-the-art Experimental Results [**75**]. Used with permission from EHS, 2014.

	Group/Institution	η [%]	Suns	V_{oc} [V]	J_{sc} [mA/cm^2]	FF [%]	Spectrum	Remarks
3 J	Fraunhofer ISE [**2, 4**]	27.9	48	3.33	614	82.9	AM1.5d	Wafer-bonding (CPV)
		20.5	1	2.78	8.56	86.3	AM1.5d	Wafer-bonding
	McMaster University [**5**]	25.5	1	2.74	11.80	79	AM1.5g	Direct metal interconnect
2 J	Fraunhofer ISE [**14**]	26.0	1	2.385	12.70	85.9	AM1.5g	Wafer-bonding
	University of Tokyo [**44**]	25.2	1	1.55	27.9	58		Wafer-bonding
	Nagoya Institute [**41**]	21.2	1	1.57	23.6	77.2	AM0	GaAs/AlGaAs buffer
	Multiple [**15**]	18.9	1	1.45	18.1	72	AM1.5g	SiGe buffer
	Ohio State University [**45**]	16.8	1	2.18	10.48	73.3	AM1.5g	SiGe buffer
	Fraunhofer ISE [**14**]	16.4	1	1.94	11.20	75.3	AM1.5g	GaAsP buffer
1J	Spire / NREL [**43**]	21.3	200	-	-	-	AM1.5d	GaAs buffer (CPV)
	NTT Japan [**42**]	20.0	1				AM1.5g	Strained-layer superlattice & GaAs/AlGaAs buffer
		18.3	1	0.94	33.2mA	79.1	AM0	
	Ohio State University [**13**]	18.1	1	0.973	23.8	78.1	AM1.5g	10 µm SiGe buffer
	Spire / NREL [**46**]	17.6	1	0.891	25.5	77.7	AM1.5	7 µm GaAs buffer

feasible at a realistic TDD of 10^6 cm^{-2} under 200 suns AM1.5d (1000 W/m^2) spectrum [**38**]. Using areal current-matching, a 2J GaInP/GaAs connected onto an enlarged bottom Si subcell is predicted to have 3J efficiencies exceeding 43% under 1-sun AM1.5g spectrum [**5**]. Novel solar cell designs maybe feasible by employing Si as an intermediate subcell instead of the bottommost subcell, however, it is extremely challenging to experimentally realize such cell structures. *Connolly et. al.* have modelled 3J GaAs/Si/$In_{0.74}Ga_{0.26}As$ and 3J $GaAs_{0.77}P_{0.23}$ /Si/$In_{0.74}Ga_{0.26}As$ solar cells with efficiencies of 32.9% and 36.5%, respectively, under 1-sun AM1.5g spectrum [**39**]. 4J AlGaAs/GaAs/Si/InGaAs tandem solar cells utilizing Si as an intermediate subcell could achieve efficiencies exceeding of 45% [**40**]. Although achieving such milestones will be experimentally very challenging, these modeling results showcase a promising potential for III-V-on-Si solar cells.

1.5 Literature Review: Integration Approaches for III-V-on-Si Solar Cell

1.5.1 Heteroepitaxial Integration Approaches for III-V Solar Cells on Si

1.5.1.1 Direct GaAs-on-Si Epitaxy

Among various approaches being investigated for III-V-on-Si integration for solar cell applications, the direct GaAs-on-Si epitaxial approach was among the very first ones. For realizing high quality GaAs epitaxial layers on Si substrate, the use of TCA has been proven to be a very important step for dislocation reduction. The transmission electron microscopy (TEM) micrographs for GaAs directly grown on Si along with their respective TDDs using TCA only and TCA along with InGaAs strained layer are shown in **Fig. 7 (a) and (b)**, respectively [**48, 49**]. The insertion of a strained layer during the GaAs on Si growth relieves the need for high temperature TCA and multiple TCA iterations.

Spire Corporation utilized direct GaAs-on-Si epitaxy involving thick GaAs buffer layer to realize 1J GaAs solar cell on Si substrate for 1-sun and concentrated photovoltaic application using thermal-cycle growth (TCG) by metal organic chemical vapor deposition (MOCVD) technique [**9, 33, 43, 46**]. A low temperature GaAs nucleation layer was grown at 400˚C followed by the standard GaAs growth at 700˚C. Ellipsometry studies showed that the presence of arsine during the Si bakeout was one of the major sources of oxide formation [**9**]. For a 1J GaAs cell structure, a 7 µm thick n+ GaAs buffer was employed between the cell structure and the Si substrate. An efficiency of 17.6% (J_{sc}=25.5mA/cm^2, V_{oc}=0.891V and FF=77.7%) was reported for 1J GaAs solar cell on Si under AM1.5 at a TDD of ~$8x10^6$ cm^{-2} [**46**]. Utilizing a similar growth process with 2 µm GaAs buffer, 1J GaAs concentrator solar cell on Si with an efficiency of 21.3% under 200-suns (AM1.5d) were also reported [**43**].

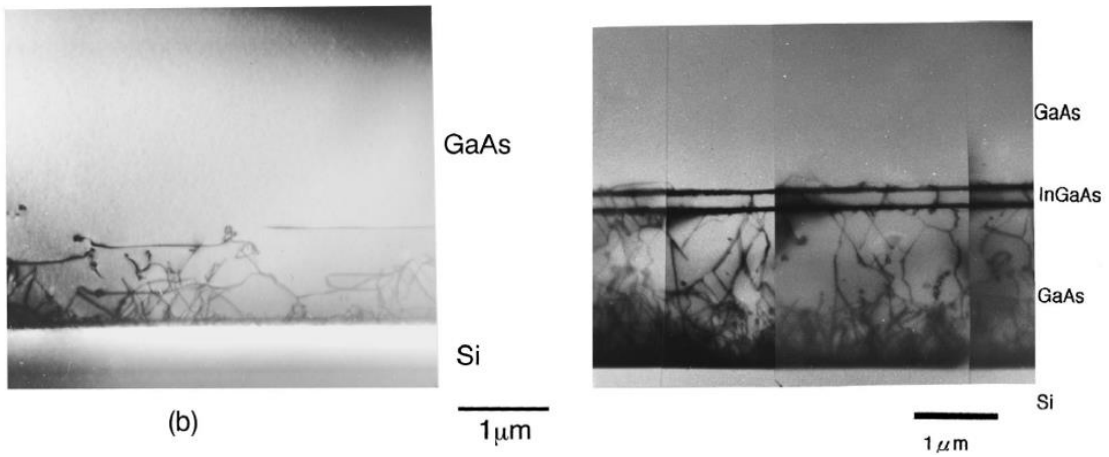

Fig. 7 Cross-sectional TEM image of heteroepitaxial GaAs grown on Si using (a) only thermal cycle annealing [**49**] and, (b) thermal cycle annealing along with $In_{0.07}Ga_{0.93}As$ strained-layer [**48**]. [**75**] Used with permission from EHS, 2014.

Soga et. al. utilized AlGaAs as an active solar cell material for integration with active Si substrate[**50**]. $Al_{0.22}Ga_{0.78}As$ with a bandgap of ~1.7 eV is one of the ideal candidates for 2J III-V/Si tandem solar cell. However, the growth of AlGaAs active solar cell material on Si becomes more complex and challenging with increased aluminum (Al) content as it incorporates more oxygen and forms deep level defects which can act as recombination centers for minority carriers and in turn degrade the minority carrier lifetime [**50**]. A 2.5 µm thick AlGaAs buffer was grown on (100) Si substrate with 2˚ offcut towards [110] using MOCVD utilizing five TCA iterations performed at 950˚C to realize a tandem p/n 2J $Al_{0.15}Ga_{0.85}As$/Si solar cell [**41**]. $Al_{0.15}Ga_{0.85}As$ (1.61 eV) solar cell material exhibited better quantum efficiency (QE) than $Al_{0.22}Ga_{0.78}As$ (1.7 eV) cell and was therefore better suited as the top-cell for current-matching with the bottom Si cell

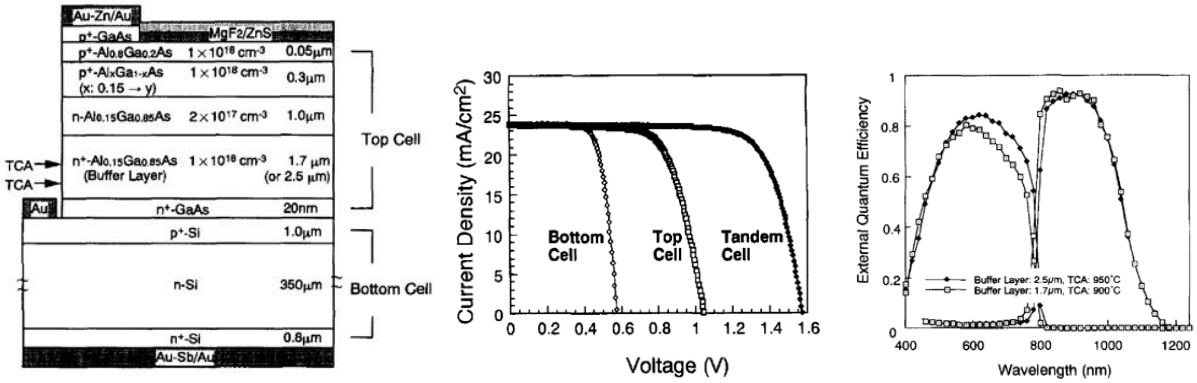

Fig. 8 (a) Cross-sectional schematic of 2J AlGaAs/Si solar cell structure, and the corresponding (b) J-V characteristic (AM0) and (c) QE plots [**41**]. [**75**] Used with permission from EHS, 2014.

[**50**]. A two-terminal 2J $Al_{0.15}Ga_{0.85}As$/Si solar cell efficiency of 21.2% was achieved under AM0 (J_{sc}=23.6mA/cm^2, V_{oc}=1.57V and FF=77.2%) [**41**], which is the highest efficiency reported for heteroepitaxial 2J III-V/Si tandem solar cell. The corresponding solar cell structure, I-V and QE plots are shown in **Fig. 8 (a), (b) and (c)**, respectively. Further improvement in the 2J AlGaAs/Si efficiency would require a superior quality and higher bandgap (Al-rich) top-cell (~1.7-1.8 eV), making it necessary to focus efforts on improving the minority carrier lifetime in Al-rich AlGaAs solar cell material [**41**], besides minimizing the TDs generated due to the lattice-mismatch with Si substrate.

Yamaguchi et. al. utilized $In_{0.1}Ga_{0.9}As$/GaAs strained layer superlattices (SLSs) in combination with TCA to significantly minimize the TDD to ~ 1-2x10^6 cm^{-2} for GaAs layers grown on (100) Si substrate by MOCVD [**23**]. For the growth of 1J GaAs solar cell on Si, (100) Si substrates with 2˚ offcut towards [110] were utilized [**42**]. An initial 10-15 nm thick low temperature GaAs was grown at 400˚C, followed by the subsequent growth of ~2 µm thick GaAs at 700˚C. Five iterations of TCA were performed at 900˚C, followed by the growth of 5 periods of $In_{0.1}Ga_{0.9}As$/GaAs (10nm/10nm) SLS and 5 periods of $Al_{0.6}Ga_{0.4}As$/GaAs (20nm/100nm) strained layer (SL), prior to the growth of 1J p/n GaAs solar cell structure [**42, 47**]. The 1J GaAs-on-Si solar cells realized using the combination of TCA, SLS and SL buffer demonstrated an efficiency of 20% under AM1.5g and 18.3% under AM0 conditions (at a TDD of ~4.5x10^6 cm^{-2}), both of which are the highest efficiencies reported for heteroepitaxial 1J GaAs-on-Si solar cells [**42, 47**]. The corresponding solar cell structure and the I-V curve are shown in **Fig. 9 (a) and (b)**, respectively. Further reduction in TDD < 1x10^6 cm^{-2}, improvement in minority carrier transport properties and thermal mismatch related issues would be essential to enable direct GaAs-on-Si solar cell performance to compete with lattice-matched GaAs-on-GaAs solar cells.

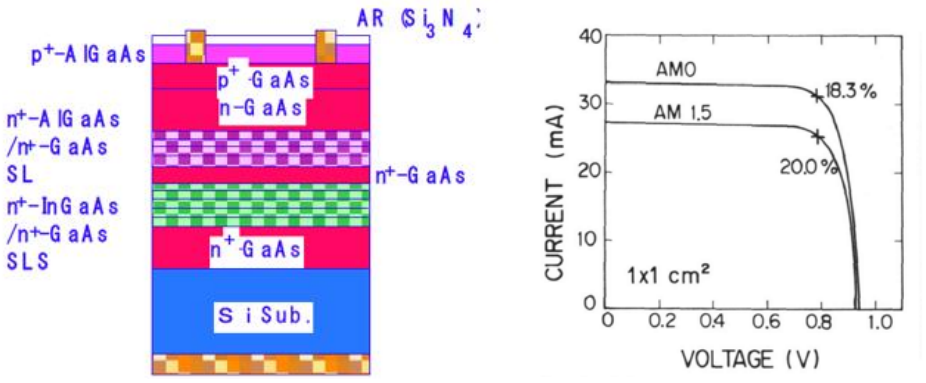

Fig. 9 (a) Cross-sectional schematic of 1J GaAs-on-Si solar cell using AlGaAs/GaAs SLs and InGaAs/GaAs SLS [**47**], and (b) the corresponding I–V curve for a 1 cm^2 solar cell [**42**]. [**75**] Used with permission from EHS, 2014.

1.5.1.2 Si_xGe_{1-x} Graded buffers

GaAs or Ge substrates are currently the conventional choice for commercial multijunction III-V solar cells. One of the inherent benefits of using step-graded Si_xGe_{1-x} buffer is the ability to realize high-quality, low TDD and relaxed Ge layers on Si substrate providing a "virtual" Ge platform for subsequent GaAs growth [**51**].

Most of the research on SiGe buffers for III-V solar cell integration on Si substrate has been carried out through collaborative research between Ohio State University (OSU) and Massachusetts Institute of Technology (MIT) using combination of growth techniques including ultrahigh vacuum chemical vapor deposition (UHV-CVD), molecular beam epitaxy (MBE) and MOCVD. Typically, the compositionally step-graded 12 µm thick SiGe buffers are grown by UHC-CVD on (100) Si with 6˚offcut towards <110> plane with final composition ending in 100% Ge [**13, 45**]. A TDD of ~$2.1x10^6$ cm^{-2} was reported for fully relaxed Ge layers grown on SiGe/Si substrate [**13, 45**]. For the III-V solar cell growth, an initial epitaxial Ge layer was grown by MBE followed by the growth of GaAs on Ge at an initial low growth temperature using migration-enhanced epitaxy, details of which can be found in reference **13, 52**. This process has been shown to suppress the formation of APDs due to the controlled nucleation at the GaAs/Ge interface, and etch-pit density of $5x10^5$ - $2x10^6$ cm^{-2} was reported for the GaAs layers grown on virtual Ge substrate [**52**].

Detailed investigation on the impact of TDs on the minority carrier lifetimes revealed superior dislocation tolerance for holes in n-type GaAs (τ_p~10 ns) in comparison to electrons in p-type GaAs (τ_n~1.5 ns) material for a similar dislocation density and doping concentration [**53, 54**]. The reduced electron lifetime was attributed to their higher mobility which translated to increased sensitivity towards the dislocations in GaAs

p^{++} GaAs contact layer (1000Å)	~$1x10^{19}$ cm^{-3}
p^+ $In_{0.49}Ga_{0.51}P$ window (500 Å)	~$1x10^{18}$ cm^{-3}
p^+ GaAs emitter (5000 Å)	~$2x10^{18}$ cm^{-3}
n GaAs base (2.0 µm)	~$1x10^{17}$ cm^{-3}
n^+ $In_{0.49}Ga_{0.51}P$ back surface field (1000 Å)	~$1x10^{18}$ cm^{-3}
n^+ GaAs buffer (1000 Å)	~$1x10^{18}$ cm^{-3}
low-temperature n^+ GaAs buffer (1000 Å)	~$2x10^{18}$ cm^{-3}
SSMBE Ge buffer layer (300 Å)	uid
Ge termination layer (~1.0 µm)	~$1x10^{18}$ cm^{-3}
n SiGe step graded buffer layers (~ 10 µm)	~$1x10^{18}$ cm^{-3}
n Si substrate	~0.5-2 $1x10^{18}$ cm^{-3}

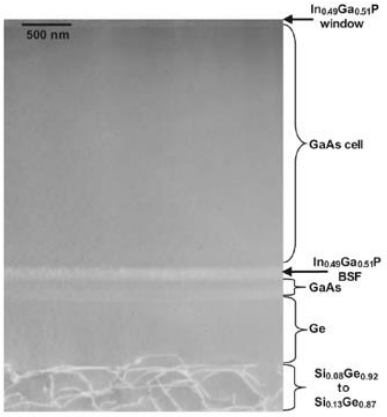

Fig. 10 (a) Cross-sectional schematic of 1J GaAs solar cell structure grown on Ge/SiGe/Si substrate, and (b) the corresponding cross-section TEM image showing most of the dislocations confined within the buffer layer [**13**]. [**75**] Used with permission from EHS, 2014.

layers grown on metamorphic SiGe buffers [**54**]. Such sensitivity of minority carrier lifetime in the metamorphic GaAs material on Ge/SiGe/Si substrates led to superior performance for p^+/n diodes over their n^+/p counterparts and hence the p/n solar cell showed higher V_{oc} compared to n/p solar cell (0.98 V vs. 0.88V) at a TDD ~ $1x10^6$ cm^{-2}, indicating device polarity dependence for metamorphic GaAs solar cells grown on SiGe substrates [**55, 56**]. Utilizing step-graded Si_xGe_{1-x} buffer, OSU and MIT teams demonstrated a 1J p/n GaAs solar cell (see **Fig. 10 (a)** and **(b)** for the cell structure and the corresponding cross-sectional TEM image) with an efficiency of 18.1% and 15.5% under AM1.5g and AM0 conditions, respectively (see **Fig. 11** for the J-V characteristics) [**13**]. Such 1J GaAs solar cells on SiGe substrate were demonstrated to exhibit similar performance virtually independent of the cell area, thereby addressing the concern of thermal mismatch related issues between the GaAs epilayers and the Si substrate [**13**]. Addtionally, *Lueck et. al.* reported a 2J GaInP/GaAs solar cell on similar Ge/SiGe/Si substrate with an efficiency of 16.8% under AM1.5 [**45**]. The overall performance of the 2J cell was limited by poor antireflection coating, large grid coverage area, significant absorption in the GaAs tunnel junction and due to a lower V_{oc} contribution from the top GaInP subcell (primarily due to a lower top cell bandgap) [**45**].

Utilizing a low bandgap SiGe metamorphic buffer eliminates the possibility of utilizing the bottom Si as a subcell since the SiGe buffer doesn't provide the optical transparency needed for the bottom Si subcell. Interestingly, *Diaz et. al.* have utilized an active Si_xGe_{1-x} cell on the graded SiGe buffer to realize III-V/SiGe tandem solar cell [**15**]. Both GaAsP and SiGe materials can be compositionally tuned to span a broad range of bandgaps opening possibility for multijunction cells with internal lattice-matching between GaAsP and SiGe. While the unconstrained two-terminal 2J ideal efficiency is 41.7% under AM1.5g for a bandgap combination of 1.73/1.13 eV, the predicted efficiency for 2J GaAsP/SiGe cell is 39.4% (AM1.5g) under lattice-matched conditions (with bandgaps of 1.54/0.84 eV) [**57**]. *Diaz et. al.* reported an efficiency of

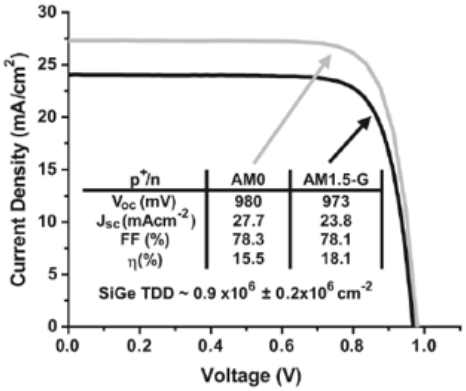

Fig. 11 J-V characteristic of 1J p/n GaAs solar cell on Ge/SiGe/Si substrate [**13**]. [**75**] Used with permission from EHS, 2014.

18.9% under AM 1.5g (J_{sc}=18.1mA/cm^2, V_{oc}=1.45V and FF=72%) for 2J $GaAs_{0.84}P_{0.16}$ /$Si_{0.18}Ge_{0.82}$ (1.67/0.86 eV) tandem solar cell grown on (100)/6˚ offcut Si substrate by a combination of reduced pressure chemical vapor deposition for SiGe buffer and MOCVD for III-V growth [**15**]. The solar cell structure and the corresponding cross-sectional SEM micrograph are shown in **Fig. 12 (a)** and **(b)**, respectively. The corresponding J-V and QE plots for the 2J GaAsP/SiGe tandem solar cell are shown in **Fig. 13 (a)** and **(b)**, respectively. The bottom SiGe subcell was found to be current-limiting with significant room for QE improvement in the higher wavelength regime. Further improvements from series resistance minimization, better current-matching and dislocation reduction in the top GaAsP subcell are expected to improve efficiency to ~25% [**15**]. Research efforts at 4Power LLC have led to GaAsP/SiGe tandem solar cells with an efficiency of ~20% (AM 1.5) at a TDD as low as 8x10^5 cm^{-2} indicating a promising future for GaAsP/SiGe based tandem solar cells on Si substrate [**58**].

1.5.1.3 $GaAs_xP_{1-x}$ Graded buffers

A tandem 2J solar cell with a top subcell having a bandgap of 1.7-1.8 eV ($GaAs_{0.7}P_{0.3}$ being one of the potential candidates) integrated onto a bottom 1.12 eV Si subcell is predicted to have efficiency exceeding of 40% under AM1.5g [**59**]. Furthermore, 3J InGaP/GaAsP//Si (2.0/1.5/1.1 eV) solar cells are expected to achieve > 45% efficiency under AM1.5g [**59**]. The large bandgap of $GaAs_xP_{1-x}$ buffer provides light transmission to the bottom Si subcell unlike the graded SiGe buffer approach. *Geisz et. al.* utilized a thin GaP nucleation layer, followed by the growth of lattice-matched $GaN_{0.02}P_{0.98}$ buffer layer which was compositionally graded using $GaAs_xP_{1-x}$ buffer to demonstrate a metamorphic $GaAs_{0.7}P_{0.3}$ (1.71 eV) solar cell on Si substrate for the first time [**60**]. 1J $GaAs_{0.7}P_{0.3}$ solar cell grown on Si substrate by MOCVD was reported with an efficiency of 9.8% (AM1.5g) without antireflection coating. The performance of the solar

$GaAs_{.84}P_{.16}$	Contact	1.67eV	n+
$In_{.35}Al_{.65}P$	Window	2.4eV	n
$GaAs_{.84}P_{.16}$	Emitter	1.67eV	n
$GaAs_{.84}P_{.16}$	Base	1.67eV	p
$Ga_{.59}In_{.41}P$	BSF	2eV	p
$GaAs_{.84}P_{.16}$	Buffer	1.67eV	p
$GaAs_{.84}P_{.16}$	TJ	1.67eV	p+/n+
$GaAs_{.84}P_{.16}$	Buffer	1.67eV	n
$Ga_{.59}In_{.41}P$	Nucleation	2eV	n
$Si_{.18}Ge_{.82}$	SiGe	0.86eV	i
$Si_{.18}Ge_{.82}$	Emitter	0.86eV	n
$Si_{.18}Ge_{.82}$	Base	0.86eV	p
$Si_{.18}Ge_{.82}$	Graded Buffer	1.1-0.86eV	p
	Si Substrate		p

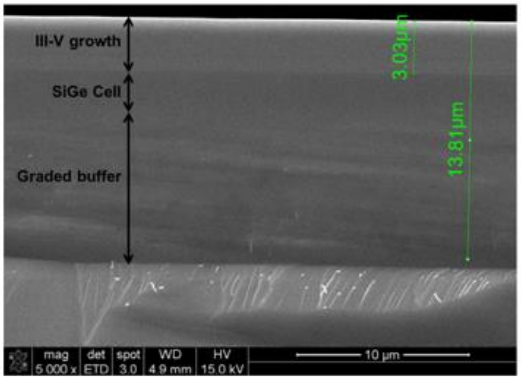

Fig. 12 (a) Cross-sectional schematic of 2J $GaAs_{0.84}P_{0.16}/Si_{0.18}Ge_{0.82}$ solar cell structure grown on Si substrate, and (b) the corresponding cross-section SEM image [**15**]. [**75**] Used with permission from EHS, 2014.

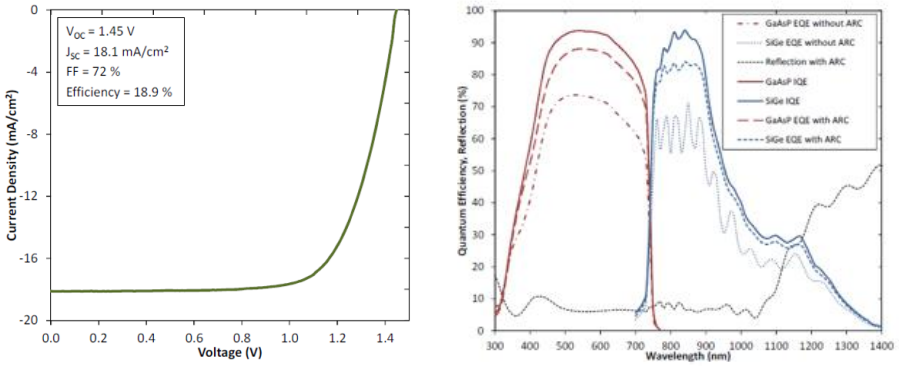

Fig. 13 (a) J-V characteristic (AM1.5g) and (b) QE plot of 2J $GaAs_{0.84}P_{0.16}/Si_{0.18}Ge_{0.82}$ solar cell structure grown on Si substrate [**15**]. [**75**] Used with permission from EHS, 2014.

cell was limited by the high TDD of $9.4x10^7$ cm^{-2}, which translated to a relatively high bandgap-voltage offset, W_{oc} of 0.73 eV [**60**].

Grassman et. al. have focused efforts on improving the quality of GaP/Si interface to minimize the heterovalent nucleation-related defects, including APDs, stacking faults and microtwins for structures grown by both MBE and MOCVD [**29, 62**]. Phosphorus diffusion during GaP-on-Si epitaxy was found to be inefficient in forming a diffused emitter to realize an active bottom Si subcell. Hence, n-doped epitaxial silicon emitter was proposed as a more promising alternative. GaP was shown to act as an effective window layer for bottom Si subcell and provided good front surface passivation and minority carrier reflection. **Fig. 14** shows the 2J GaAsP/Si solar cell structure along with the corresponding cross-sectional TEM image of the MOCVD grown $GaAs_{0.7}P_{0.3}$ on GaAsP/GaP/Si substrate. A prototype 2J $GaAs_{0.75}P_{0.25}$/Si solar cell

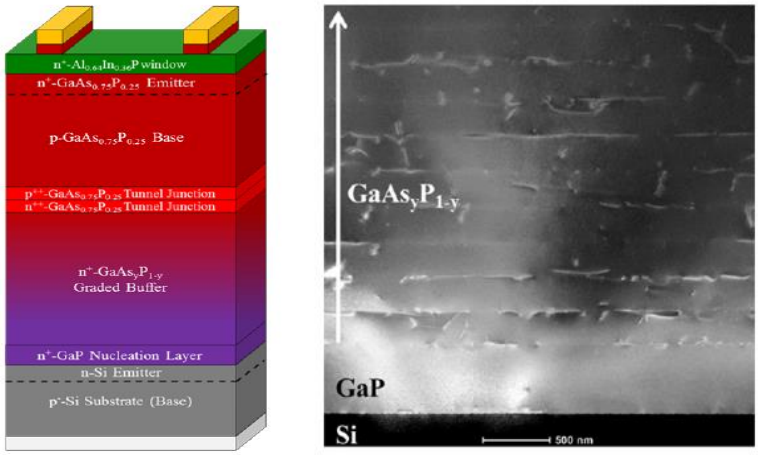

Fig. 14 (a) Cross-sectional schematic of 2J $GaAs_{0.84}P_{0.16}/Si_{0.18}Ge_{0.82}$ solar cell structure grown on Si substrate, and (b) the corresponding cross-section SEM image [**63**]. [**75**] Used with permission from EHS, 2014.

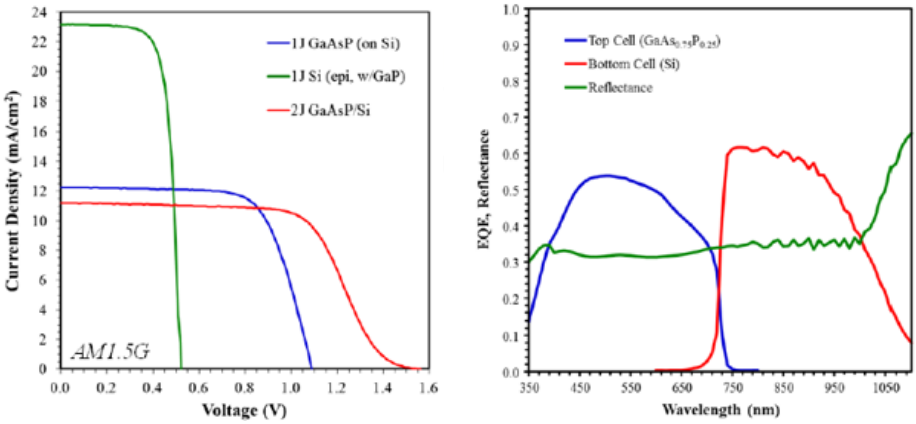

Fig. 15 (a) J-V characteristic (AM1.5g) and (b) QE plot of 2J $GaAs_{0.84}P_{0.16}/Si_{0.18}Ge_{0.82}$ solar cell structure grown on Si substrate [**63**]. [**75**] Used with permission from EHS, 2014.

exhibited an efficiency of ~10.65% under AM1.5g spectrum (J_{sc}=11.2 mA/cm^2, V_{oc}=1.56 V and FF=61%) without any anti-reflection coating [**63**]. The corresponding J-V and QE characteristics are shown in **Fig. 15 (a)** and **(b)**, respectively. The overall efficiency was limited by a low FF associated with the $GaAs_{0.75}P_{0.25}$ tunnel diode, which was inefficient in providing a lossless interconnection between the subcells [**63**].

More recently, *Yaung et. al.* have focused efforts on further optimizing the metamorphic GaAsP growth on GaP/Si templates by using MBE [**16**]. To promote strain relaxation in order to minimize TDD, GaAsP growth temperature was varied from 600 to 700˚C. Authors reported best optimization of rms roughness and TDD at a growth temperature of 600 - 640˚C. Consequently, improvement in the TDD translated to a low bandgap-voltage offset, W_{oc}~0.55 for $GaAs_{0.77}P_{0.23}$ (1.66 eV) on GaP/Si templates (TDD ~7.8x10^6 cm^{-2}) compared to a W_{oc}~0.53 on the GaP substrate. Such GaAsP material with W_{oc} approaching the 0.3-0.4 eV radiative limit represent good material quality for metamorphic 1J GaAsP grown on GaP/Si template. **Fig. 16 (a)** shows the cross-sectional schematic of 1J $GaAs_{0.77}P_{0.23}$ solar cell structure grown on GaP/Si substrate, and the corresponding J-V characteristic (AM1.5g) and the QE plot are shown in **Fig. 16 (b)** and **(c)**, respectively. In addition, identical W_{oc} values were reported for both n^+/p and p^+/n polarities for 1J GaAsP solar cells on GaP/Si template (unlike for the 1J GaAs solar cells on SiGe substrates), suggesting future work should focus efforts on n^+/p solar cell designs to take the advantage of GaP as an effective window layer for the bottom Si subcell [**61**]. With improvement in the tunnel junction designs, addition of optimal anti-reflection coating and further reduction in TDD in the metamorphic GaAsP cells, the future for graded GaAsP buffer approach for integrating III-V/Si tandem solar cell looks very promising.

Dimroth et. al. have utilized metamorphic $GaAs_xP_{1-x}$ buffer layer to bridge the lattice constant from Si to GaAs in order to realize conventional 2J GaInP/GaAs solar cells integrated onto inactive Si substrate [**14**].

A homoepitaxial silicon layer was first grown on (100) Si substrate with 6˚ offcut towards <1 -1 1>, followed by the growth of thin GaP nucleation layer. Next, the graded $GaAs_xP_{1-x}$ buffer with seven steps was grown at a growth temperatures of 640˚C using MOCVD, details of which can found in reference **14**. A TDD exceeding 10^8 cm^{-2} was observed; suggesting future research efforts should focus on utilizing slower grading and growth rates in addition to optimizing the growth temperature for metamorphic GaAsP buffer. An efficiency of 16.4% (J_{sc}=11.20 mA/cm^2, V_{oc}=1.94 V and FF=75.3%) was measured under AM1.5g for the 2J GaInP/GaAs solar cell grown on Si substrate, while the control 2J GaInP/GaAs solar cell grown on GaAs substrate exhibited an efficiency of 27.1%, suggesting that the high TDD was the performance limiting factor for the "on Si" solar cells. An additional important finding was that there was no indication of cracking due to differences in thermal expansion coefficient between Si and GaAs. The QE curve for the 16.4% efficient 2J GaInP/GaAs solar cells realized on GaAsP/GaP/Si substrate is shown in **Fig. 17**. The GaAs subcell was found to be current-limiting due to the reduced minority carrier lifetime associated with high TDD, resulting in inefficient carrier collection in the thick (1.9 µm) GaAs absorbers. Interestingly, the GaInP subcell was less impacted by dislocations due to two possible reasons: (i) additional thermal budget beyond the GaAs subcell growth helped in minimizing the propagation of the dislocations to the top GaInP subcell and (ii) lower thickness (0.79 µm) of the GaInP absorbers did not sufficiently impact the minority carrier collection in spite of a high TDD. Such finding is consistent with dislocation dependent modeling results for 2J InGaP/GaAs solar cells on Si, wherein the authors reported that lowering the GaInP subcell

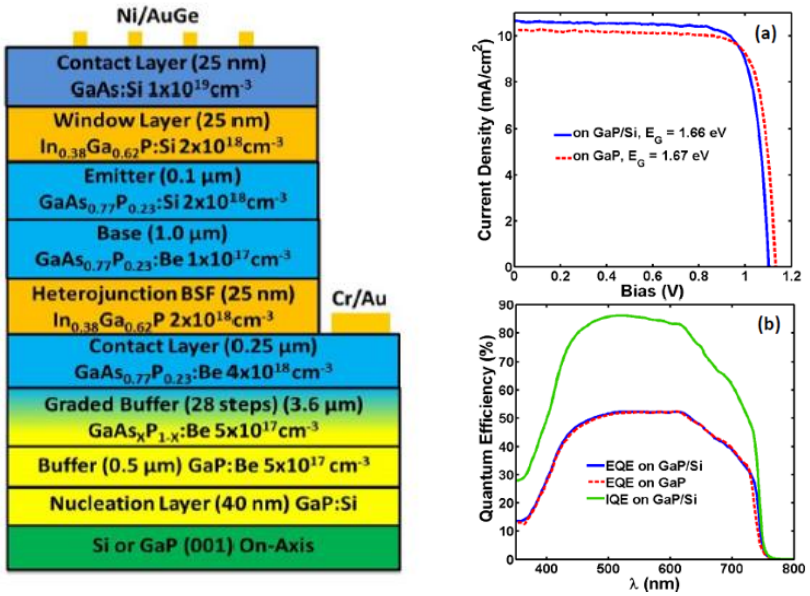

Fig. 16 (a) Cross-sectional schematic of 1J $GaAs_{0.77}P_{0.23}$ solar cell structure grown on GaP/Si substrate, and (b) the corresponding J-V characteristic (AM1.5g) and (c) the QE plot for the 1J $GaAs_{0.77}P_{0.23}$ solar cell structure grown on GaP vs. GaP/Si substrate [**16**]. [**75**] Used with permission from EHS, 2014.

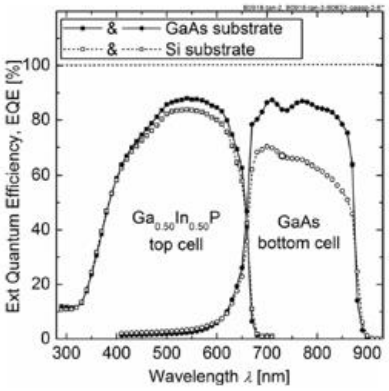

Fig. 17 QE plot for 2J InGaP/GaAs solar cell structure grown on GaAs/GaAsP/GaP/Si substrate indicating the bottom GaAs subcell limits the two-terminal current [**14**]. [**75**] Used with permission from EHS, 2014.

thickness, allowed increase in the photon flux penetration to the bottom current-limiting GaAs subcell for current-matching [**37**]. Such tandem 2J InGaP/GaAs solar cells on Si with efficiencies comparable to 2J InGaP/GaAs solar cells on GaAs substrate are possible if TDD lower than10^6 cm^{-2} can be achieved [**37**]. With this approach, 1-sun efficiency in excess of 30% would be realistic for 3J GaInP/GaAs//Si solar cells on Si substrate, offering one of the most promising short-term paths for III-V-on-Si solar cell integration.

1.5.1.4 Lattice-matched III-V-N Materials on Si

The biggest advantage of dilute nitride based III-V-N alloys is the ability to grow almost lattice-matched III-V materials on Si substrate for promising III-V/Si tandem solar cells. The quaternary compounds of $GaAs_xP_{1-x-y}N_y$ and $In_xGa_{1-x}P_yN_{1-y}$ are attractive options for lattice-matched top subcells in 2J III-V/Si tandem architecture [**18**]. For lattice-matched 3J consideration, the ideal material selection is $GaP_{0.98}N_{0.02}$ (2 eV)/ $GaAs_{0.20}P_{0.73}N_{0.07}$ (1.5 eV) // Si (1.1 eV) [**18**]. $GaAs_{0.09}P_{0.87}N_{0.04}$ alloy (bandgap of 1.81 eV) lattice-matched to Si substrate is an attractive top cell choice for 2J III-V/Si tandem solar cell [**18**]. Furthermore, from growth perspective, GaAsPN alloys are easier to grown in comparison to InGaPN due to the difficulties associated with InN and GaN solid-phase miscibility [**64-66**].

Geisz et. al. reported the first 2J $GaAs_{0.10}P_{0.86}N_{0.04}$ (1.80 eV)/Si tandems solar cell with an efficiency of 5.2% under AM1.5g (without an antireflective coating) utilizing an initial GaP nucleation layer, followed by the MOCVD growth of lattice-matched $GaN_{0.02}P_{0.98}$ layer [**17**]. The solar cell structure along with the corresponding I-V and QE characteristic for this tandem solar cell are shown in **Fig. 18 (a), (b)** and **(c)**, respectively. The GaNP layer had a TDD $<10^6$ cm^{-2} with most of the misfit dislocations being confined at the GaP/Si interface. The phosphorus diffusion during the initial GaP growth formed the n-emitter for the

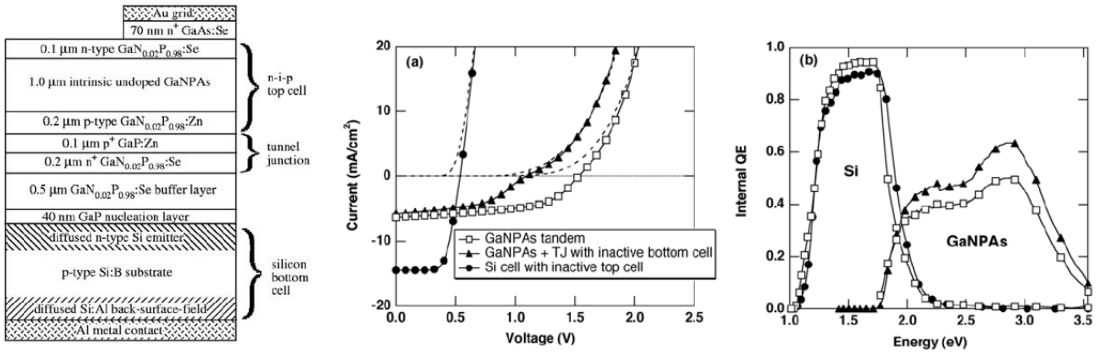

Fig. 18 (a) Cross-sectional schematic of lattice-matched 2J GaNPAs/Si solar cell structure grown on Si substrate, (b) J-V characteristic (AM1.5g), and (c) the QE plot of 2J $GaN_{0.04}P_{0.86}As_{0.1}$/Si solar cell grown on Si substrate, clearly indicating GaNPAs is the current limiting subcell [**17**]. [**75**] Used with permission from EHS, 2014.

p-Si substrate. Intuitively, one would expect the defects at the GaP/Si interface to influence the Si cell response near the front emitter region, however most of the blue light is captured by the top cell and therefore imperfect front passivation did not strongly degrade the J_{sc} of the Si bottom cell. The top GaAsPN subcell was found to be limiting the two-terminal current (5.7 mA/cm^2 for GaAsPN subcell vs. 14.5 mA/cm^2 for the bottom Si-subcell). Furthermore, the unintentional carbon and hydrogen impurities had a strong influence on the minority carrier lifetimes in GaAsPN, resulting in low structural quality of the top nitride subcell which translated to a low tandem cell efficiency. Improving the diffusion lengths in the dilute nitride solar cell material would be pivotal to improve the QE response and hence the overall tandem cell performance. Another important area of attention for the lattice-matched III-V solar cells on Si would be the development of tunnel-junction with abrupt interfaces and doping profiles and low series resistance, especially for CPV operation. Recent advancements in dilute nitride materials, GaAsPN/GaPN multiple quantum-well (MQW) structures, extensive research on GaP on Si epitaxy and the progress in lattice-matched GaNAsP based lasers on Si [**67**] present an exciting opportunity to further advance the research on III-V-N based lattice-matched materials on Si for solar cell integration.

1.5.1.5 Lattice-mismatched InGaN on Si

With its tunable and direct bandgap spanning the entire useful range of the solar spectrum (0.65 eV – 3.4 eV), InGaN material is one of the most well suited materials for multijunction solar cells. InGaN solar cell with a bandgap of ~1.8 eV would be an ideal candidate for 2J integration with an active 1.1 eV Si bottom subcell. An additional advantage of using InGaN top subcell with Si bottom subcell is the band-alignment of the n-InGaN conduction band with the p-Si valence band which exhibits same energy relative to vacuum,

opening a promising option for tunnel junction between the two subcells [**20**]. Using simple analytical simulations taking into account realistic diffusion lengths, an efficiency of ~30% (1-sun) is expected for 2J InGaN/Si p/n solar cell, while 3J InGaN (1.9 eV)/InGaN (1.5 eV)/Si solar cell are predicted to have an efficiency of ~35% (1-sun) [**65**]. The grading of the InGaN absorber layer close to the top heterointerface (p-GaN/n-InGaN) in a p/n InGaN/Si tandem solar cell is expected to boost the performance as it removes the barrier for hole transport [**21**].

The first experimental evidence of a tandem GaN/Si solar cell was demonstrated using GaN/AlN-buffer/ Si 2J p/n solar cell [**68**]. More recently, *Tran et. al*. demonstrated good quality $In_{0.4}Ga_{0.6}N$ films grown on GaN/AlN/Si(111) substrate with negligible phase separation using high-low-high-temperature AlN buffer layers by MOCVD [**22**]. Utilizing a similar growth approach, 1J n-$In_{0.4}Ga_{0.6}N$/p-Si hetero-structure solar cell with enhanced J_{sc} was demonstrated, attributed to the use of indium tin oxide as the top n-type contact [**22**]. A conversion efficiency of 7.12% under AM1.5g [**22**] was achieved, indicating a promising start for InGaN solar cells on Si substrate.

Poor structural quality of nitride materials (especially for InGaN material with >30% indium content) and the associated challenges for p-type doping have been the major impediments in the realization of high-efficiency InGaN solar cells. Large lattice-mismatch between InN and GaN causes a solid-phase miscibility gap due to the low solubility between these two materials [**65, 66**]. The difficulty in doping InN material with p-type dopant is presumably due to the compensation by native defects. Utilizing p-GaN/n-$In_xGa_{1-x}N$ heterojunction is one of the ways to avoid the use of p-doped $In_xGa_{1-x}N$ material, wherein the GaN layers also serves as a window layer and reduces the surface recombination [**21**]. However, theoretical efficiency of such GaN/InGaN heterojunction is limited to 11% for 1J devices due to the polarization effects, which impedes the carrier collection [**69**]. Hence, homojunction devices would be essential to achieve higher efficiencies because employing p-i-n structures could eliminate the polarization effects. Homojunction $In_{0.60}Ga_{0.40}N$ p-n junctions with optimal device designs are predicted to be 21.5% efficiency under AM1.5g conditions [**74**]. InGaN based p-i-n solar cells with InGaN as the intrinsic layer between GaN and with graded indium composition up to 50% could lead to theoretical efficiency of 18.53% under AM1.5 [**70**]. InGaN homojunctions with indium-rich, highly p-doped and thick bulk layers with no phase separation would be essential for the success of InGaN solar cells [**69**]. Utilizing metal modulated epitaxy (MME), wherein the metal shutters are modulated with a fixed duty cycle under constant nitrogen flux is a promising approach. This technique allows for control of the kinetics of Mg incorporation, while using low substrate temperature for growth, thus offering great potential to overcome both p-type doping and phase-separation limitations in In-rich InGaN. InGaN material with upto 66% In content, good crystallinity and rms

roughness of 0.76 nm were demonstrated using this MME growth approach [**69**]. Further development of high-quality In-rich InGaN material would be crucial for realizing InGaN/Si tandem solar cells in the future.

Table II summarizes the key merits and technological challenges for the respective heteroepitaxial integration approaches for III-V-on-Si solar cells.

1.5.2 Wafer Bonding & Mechanical Stacking Approach for Integrating III-V Materials on Si

1.5.2.1 Ion-implantation induced layer transfer for Ge/Si templates.

In the hydrogen-induced layer transfer technique, Ge wafers were implanted with H^+ ions and then bonded to Si substrate through a SiO_2 bond layer. The wafer bonding was done before starting the epitaxial cell growth. The bonded pair was then annealed to 250-350˚C under > 1MPa pressure to enable hydrogen-induced layer splitting which initiates the propagation of micro-cracks parallel to the Ge surface upon annealing [**71**].

Archer et. al. utilized such bonded templates fabricated with wafer bonding and ion implantation induced layer transfer technique to realize 2J GaInP/GaAs solar cells (grown by MOVPE) on Ge/Si template with comparable performance to those grown on epi-ready Ge substrate [**72**]. For the device grown on Ge/Si template, the J_{sc} was comparable to the control samples on bulk Ge substrate, however the V_{oc} was slightly lower (1.97-2.08 V vs. 2.16 V). The drop in V_{oc} translated to 2J GaInP/GaAs efficiency of 15.5%-15.7% (AM1.5d) on Ge/Si template compared to 17.2% - 19.9% on bulk Ge substrate. The authors attributed the decrease in GaInP bandgap (for the samples grown on Ge/Si template) as one of the main reasons for lower V_{oc}. The decrease in GaInP bandgap was believed to be due to the difference in the Ge substrate miscut used to make the Ge/Si template [**72**]. It is not trivial to decouple the contributions from the substrate miscut, the GaInP ordering effect and due to the growth conditions on Ge versus Ge/Si substrates and warrants further investigation. Nonetheless, a key advantage of this technique is its metal-free bonding approach enabling the possibility of subsequent upright epitaxial growths. Metal involved for bonding process could otherwise block light penetration in case an active subcell below the bond layer is desired. However the thermal-mismatch between Si, Ge, III-V materials and the bond layer could pose potential cracking issues in thin solar cell layers [**14**] during the subsequent post-bonding epitaxial growth

TABLE II

Summary of Heteroepitaxial III-V-on-Si Integration Approaches [**75**]. Used with permission from EHS, 2014.

PATH	MERITS	CHALLENGES	BEST EFFICIENCY
GaAsP Graded Buffer	• Start with lattice-matched GaP layer • GaP buffer could serve as a window layer for the bottom Si cell • Possibility for no N- or Al-containing alloys • Semi-transparent buffer for bottom Si cell	• Mixed anion As-P complex growth • Thick graded buffer	2J GaInP/GaAs - 16.4% (AM1.5g) [**14**]
SiGe Graded Buffer	• Low dislocation density • Possibility to use Ge or SiGe as subcell	• Non-transparent buffer, ruling out bottom-Si cell • Thick graded buffer • Ge poses severe thermal-mismatch concern	1J GaAs - 18.1% (AM1.5g) [**13**] & 2J GaAsP/SiGe - 18.9% (AM1.5g) [**15**]
InGaN-on-Si	• InGaN material composition can span the entire useful solar spectrum • Avoid the need for As, P or Al based materials • Semi-transparent buffer for bottom Si cell	• Large lattice-mismatch between InGaN and Si • Realization of In-rich InGaN bulk material (In>40%) challenging • Difficulty in p-doping of In-rich InGaN layers • Problem of phase separation in In-rich InGaN material and InN segregation.	1J InGaN//Si heterostructure – 7.12% (AM1.5g) [**22**]
GaAsPN-on-Si	• Only path for lattice-matched multi-junction III-V solar cells to Si • Transparent & relatively thinner buffers for bottom Si cell • GaP buffer could serve as a window layer for the bottom Si cell	• Poor diffusion lengths in dilute nitride materials • Challenging to control composition of quaternary alloys.	2J GaAsPN//Si- 5.2% (AM1.5g) – No ARC [**17**]
Direct GaAs-on-Si	• Direct route for realizing record efficient dilute-nitride based lattice-matched 3J cells on GaAs substrate • Path for conventional inverted metamorphic cells • Semi-transparent buffer for bottom Si • Lower dislocation density for SL approach	• High dislocation density • Might use thick buffers to minimize dislocations in some cases • Multiple thermal cycle anneals	2J AlGaAs//Si - 21.2% (AM0) [**41**] & 1J GaAs – 21.3% (AM1.5d, 200-suns) [**43**]
Strained-layers (SL) for GaAs-on-Si		• Growth could involves multiple super-lattice period • Shutter sequence during switching could be challenging (eg InGaAs/GaAsP)	1J GaAs – 20% (AM1.5g) & 18.3% (AM0) [**42**]

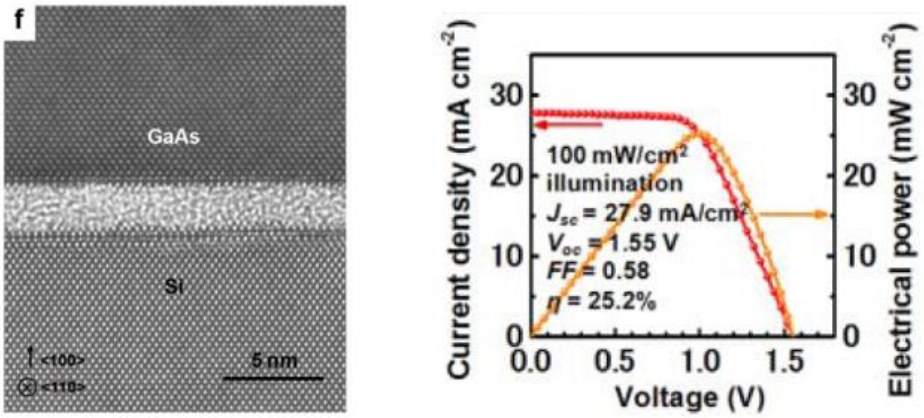

Fig. 19 (a) Cross-sectional TEM image of direct-bonded p^+-GaAs/p^+-Si heterointerface solar cell structure grown on Si substrate, and (b) J-V characteristic of the 2J $Al_{0.1}Ga_{0.9}As$/Si solar cell realized using direct-bonding [**44**]. [**75**] Used with permission from EHS, 2014.

process. Furthermore, rms roughness of films produced by this approach is ~ 25 nm and the ion implantation induced damage extends to ~200 nm into the film, requiring additional steps for damage recovery and polishing to reduce the surface roughness.

1.5.2.2 Direct Fusion Bonding

Tanabe et. al. demonstrated highly transparent and electrically conductive GaAs/Si heterojunctions using direct fusion bonding technique [**44**]. Heavily doped (degenerate) layers at both the GaAs and Si bond interface were found to be critical for realizing ohmic behavior. The p^+-GaAs/p^+-Si and p^+-GaAs/n^+-Si combination exhibited ohmic behavior for bonding temperatures as low as 300˚C in ambient air. However, when non-degenerate p-GaAs was used, non-ohmic behavior was observed even for samples bonded at 500˚C. Utilizing the direct-fusion bonding process, 2J $Al_{0.1}Ga_{0.9}As$/Si solar cells were fabricated, wherein the $Al_{0.1}Ga_{0.9}As$ subcell was grown on GaAs substrate by MBE and layer-transferred onto a Si subcell by means of p^+-GaAs/n^+-Si direct bonding at 300˚C. The p^+-GaAs/n^+-Si bond layer also served as the tunnel junction between the two n-on-p subcells. The bonding was followed by the subsequent removal of the GaAs substrate. **Fig. 19 (a)** shows the cross-sectional TEM image of a similar direct-bonded p^+-GaAs/p^+-Si heteointerface. The 2J solar cell demonstrated the highest efficiency for bonded 2J III-V/Si tandem solar cell with an active Si subcell. The performance parameters were η= 25.2%, J_{sc} = 27.9 mA/cm^2,V_{oc} = 1.55 V and FF = 58% under a 600nm peaked halogen white light source of 1-sun intensity (100 mW/cm^2). The corresponding J-V curve is shown in **Fig. 19 (b)**. One of the major challenge for this approach is the selection of interfacial layers with appropriate polarity and doping concentration which might restrict the design of solar cell polarity (n/p vs. p/n).

1.5.2.3 Surface Activated Direct Wafer Bonding

Dimroth et. al. and *Derendorf et. al*. from Fraunhofer ISE demonstrated the use of semiconductor wafer bonding to realize 2J GaInP/GaAs solar cells wafer bonded onto an inactive n-Si wafer as well as 3J GaInP/GaAs//Si solar cells bonded on an active Si solar cell, respectively [**4, 14**]. This approach is similar to the direct fusion bonding technique. One of the key advantages of this approach is the post-growth wafer bonding which to an extent circumvents the thermal stress caused by difference in thermal expansion coefficient between GaAs and Si, unlike the hydrogen-induced layer transfer technique to realize Ge on Si template [**72**].

The fast beam activated direct wafer bonding process was carried out in an Ayumi SAB-100 system. For the 2J GaInP/GaAs solar cells bonded onto Si substrate [**14**], the III-V solar cells were first grown inverted on a GaAs substrate. Thereafter, the GaAs substrate was removed by wet chemical etching and the bonding was performed at 120˚C. The Si substrate served as an inactive mechanical support and an electrical conductor. The bonded structure was then annealed for 1 min at 400˚C and processed into 4 cm^2 solar cells. This 2J GaInP/GaAs solar cell bonded onto inactive Si substrate demonstrated a conversion efficiency of 26.0% under AM1.5g spectrum with a V_{oc} = 2.39 V, J_{sc} = 12.7 mA/cm^2, and FF = 85.9% (see **Fig. 20** for the J-V characteristics). The top GaInP subcell was reported to be current-limiting (J_{sc} = 12.9 mA/cm^2 for GaInP subcell vs. 14.4 mA/cm^2 for the GaAs subcell). With improved current-matched designs, such an approach should be able to achieve greater than 30% efficiency in the future.

The 3J GaInP/GaAs//Si solar cells employing an active n-p junction Si solar cell were also realized by the same direct wafer bonding technique at room temperature under a vacuum pressure of 10^{-6} Pa. The III-V solar cells were grown upright on a GaAs substrate with a degenerately doped n-GaAs bonding layer. Thereafter, the epitaxial structure was stabilized on a sapphire wafer, the GaAs substrate was removed by

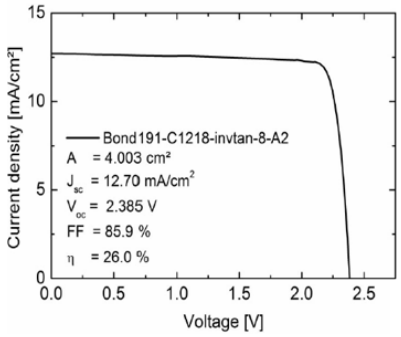

Fig. 20 J-V characteristic (AM1.5g) of 2J GaInP/GaAs solar cells wafer-bonded onto an in-active Si substrate [**14**]. [**75**] Used with permission from EHS, 2014.

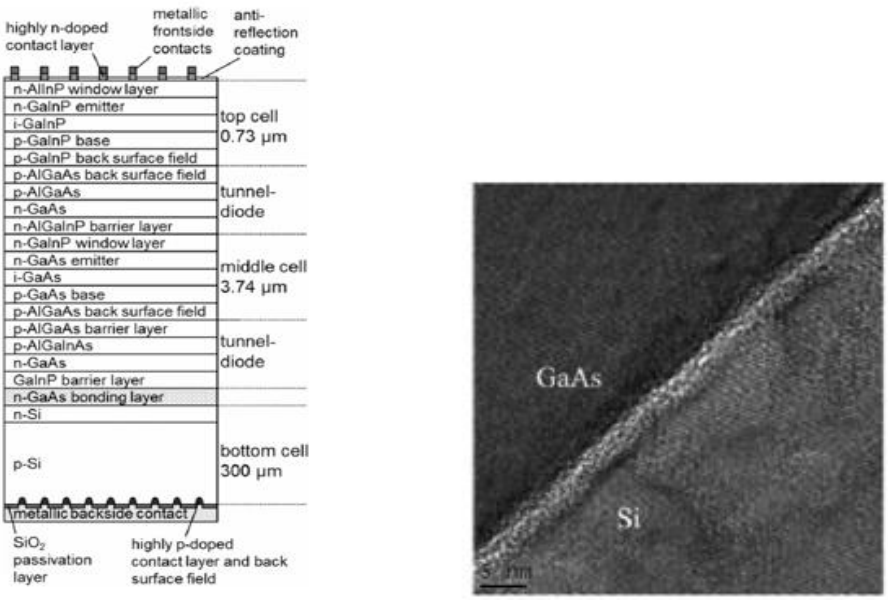

Fig. 21 (a) Cross-sectional schematic of 3J GaInP/GaAs//Si solar cell structure grown on Si substrate, and (b) the corresponding cross-section TEM image of the bonded GaAs/Si heterointerface [**4**]. [**75**] Used with permission from EHS, 2014.

selective etching and the cell stack was bonded to the n-doped emitter for the Si subcell. The bonding was initiated by applying a force of 5 kN for a minute. A 4-5-nm thin amorphous interface layer was formed by the argon fast atom beam treatment, nonetheless the photovoltaic activity of the Si subcell proved a high transparency of the bond interface. **Fig. 21 (a)** and **(b)** shows the cross-sectional schematic of the solar cell structure and cross-section TEM micrograph of the GaAs-Si bond layer interface showing the thin amorphous layer. The 3J GaInP/GaAs//Si solar cell was characterized under 1-sun AM1.5d spectrum and demonstrated an efficiency of 20.5% (J_{sc} = 8.56 mA/cm^2, V_{oc} = 2.78 V and FF = 86.3%). The performance of the 3J cell was limited by the low-current in the Si subcell due to the low absorption in the indirect bandgap Si substrate. Surface texturing at the back side of the Si substrate and reduction of the III-V layer thicknesses is expected to improve the current-response of the bottom Si subcell. The I-V and QE characteristic of this 3J solar cell are shown in **Fig. 22 (a) and (b)** respectively. Under concentrated sunlight, this 3J design demonstrated an efficiency of 23.6% under 71 suns [**2**]. At higher concentration, the significant influence of series resistance led to reduction of the fill-factor. The bond interface was attributed as the main contributor to the series resistance which led to the reduced FF under concentrated sunlight. Further optimization of the 3J GaInP/GaAs//Si solar cell has recently led to an efficiency of 27.9% (AM1.5d, 48 suns) [**2**] with headroom for further performance improvement, indicating efficiencies exceeding 30% could be attainable in the near future by employing such a wafer bonding technique for III-V-on-Si solar cell integration.

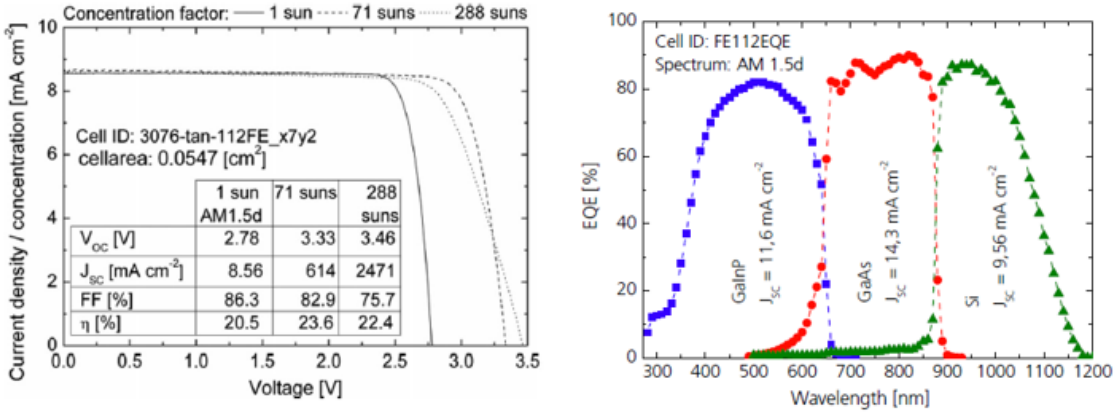

Fig. 22 (a) J-V characteristic (AM1.5d) of 3J GaInP/GaAs//Si solar cell under 1-sun and concentrated sunlight, and (b) the corresponding QE plot for the 3J GaInP/GaAs//Si solar cell realized using direct wafer bonding of III-V solar cells onto an active Si subcell [**4**]. [**75**] Used with permission from EHS, 2014.

1.5.2.4 Direct Metal Interconnect

The direct metal interconnect technique (DMI) is a novel approach where the subcells are fabricated in separate processes and joined mechanically and optically by a transparent epoxy, while the metal-to-metal interconnect provides the electrical contact [**5**]. In simple sense, the metal interconnection can be considered to perform the same function as tunnel junctions in conventional multijunction solar cells. DMI technique is capable of providing high tolerance to disparate materials with difference in lattice constants and thermal expansion coefficients, allowing for greater freedom in choosing the subcell materials with optimal bandgap combinations. *Yang et. al.* demonstrated a 3J GaInP/GaAs/Si solar cell using the DMI approach [**5**]. The 2J GaInP/GaAs cells were first grown on lattice-matched Ge substrate, thereafter the substrate was removed using epitaxial lift-off technique and the metallized front side of the 2J cell was attached to a transparent quartz wafer for support. The bottom side of the 2J solar cell was also metallized to form grid fingers. This structure was then connected to a larger area bottom Si subcell using the DMI technique such that the front grid fingers of the Si solar cell crossed over the bottom grid fingers of the 2J cell, forming a natural cross grid interconnections as shown in **Fig. 23.** An epoxy (Epo-Tek 301-2) covered the non-metallized area and a pressure of ~50kPa was applied, followed by a subsequent cure at 80˚C for 3 hours. The area of the bottom Si subcell was enlarged to allow sufficient light to reach the bottom Si-subcell which typically limits the current in such 3J GaInP/GaAs//Si solar cells. Additionally, in the DMI technique, due to the grid crossover

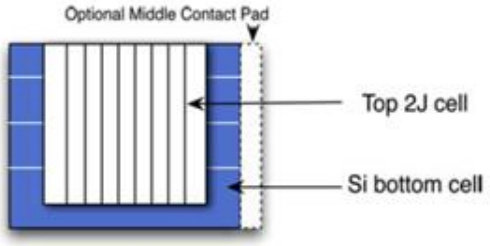

Fig. 23 Top-view of 2J GaInP/GaAs solar cell connected to the bottom Si subcell through direct metal interconnection, forming a natural cross grid interconnection [**5**]. [**75**] Used with permission from EHS, 2014.

interconnection scheme, the bottom Si subcell experiences significant shading and hence enlarged bottom Si subcell allows for realizing current-matching. *Yang et. al.* referred to this method of using large area for bottom Si substrate compared to the top III-V cells as areal current-matching (ACM). A 3J GaInP/GaAs/Si solar cell with a two-terminal 1-sun efficiency of 25.5% was reported under AM1.5g (J_{sc} = 11.8 mA/cm^2, V_{oc} = 2.74 V and FF = 79%) by employing the ACM technique for an areal Si-to-III-V ratio of 1.16. **Fig. 24 (a)** shows the I-V curve of this 3J GaInP/GaAs/Si solar cell. Utilizing the ACM technique, efficiencies exceeding 40% are feasible for 3J GaInP/GaAs/Si solar cells as shown in **Fig. 24 (b).** An additional advantage of such tandem cells employing ACM technique is their reduced sensitivity to temporal variations and light non-uniformity. Further improvement in such 3J cells would require antireflection coating at the back side of the III-V cells and alignment of the metal-interconnection between the III-V and Si cells to allow maximum light penetration to the bottom Si subcell. **Table III** summarizes the key merits and technological challenges for the respective mechanically stacked integration approaches for III-V-on-Si solar cells.

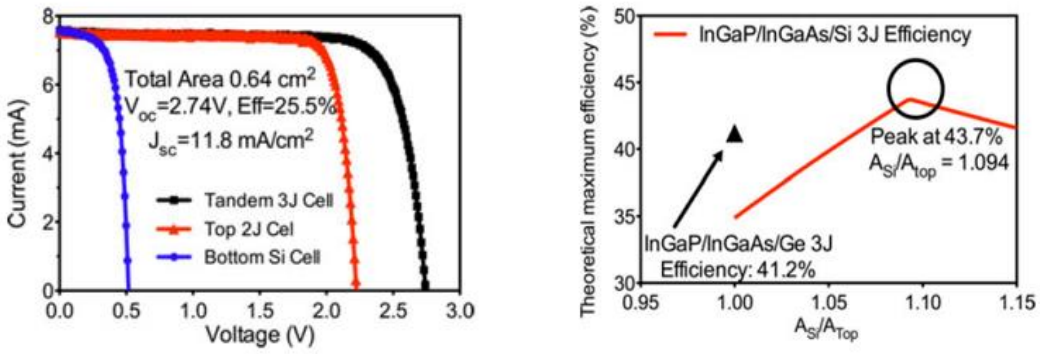

Fig. 24 (a) I-V characteristic of 3J GaInP/GaAs/Si solar cell realized using the areal current-matching technique, and (b) AM1.5g theoretical maximum efficiency for of 3J GaInP/GaAs/Si solar cell as function of the areal ratio of the bottom Si subcell with respect to the top two III-V subcells [**5**]. [**75**] Used with permission from EHS, 2014.

TABLE III

Summary of Mechanically Stacked III-V-on-Si Integration Approaches [**75**]. With permission from EHS, 2014.

PATH	MERITS	CHALLENGES	BEST EFFICIENCY
Ion-implantation induced layer transfer	• Metal free bonding allows for epitaxial growth post bonding • Post bonding growth precludes the use of expensive GaAs or Ge substrate	• Requires hydrogen ion-implantation and results in implantation damages • Pre-growth wafer bonding may impose micro-cracks issues due to thermal mismatch during high temperature growth • High rms roughness of the transfered layer • Ge layer would make the use of bottom Si subcell challenging.	2J GaInP/GaAs on Ge/Si template- 15.7% (AM1.5d) [**72**]
Direct Fusion Bonding	• Electrically conductive bond layer • Optically transparent bond layer • Post-growth wafer bonding minimizes the thermal stress	• Requires degenerate semiconductors at the bond interface with specific polarities • Relatively higher bonding temperatures • Formation of thin amorphous layer at the bonding interface	2J AlGaAs//Si- 25.2% (100 mW/cm2) [**44**]
Surface Activated Direct Wafer Bonding	• Post-growth wafer bonding minimizes the thermal stress • Low-temperature bonding process • Transparent bond-interface	• Formation of thin amorphous layer at the bonding interface due to Argon fast atom beam • Bond-layer resistance limits performance under high concentration of sunlight	2J GaInP/GaAs – 26% (AM1.5g) & 3J GaInP/GaAs//Si- 20.5% (AM1.5d, 1-sun) 27.9% (AM1.5d, 48-suns) [**14, 4, 2**]
Direct Metal Interconnect (DMI)	• Areal current matching allow for easier current matching • Low-temperature metal-metal interconnection process • Low interconnection resistance • Improved sensitivity to temporal variation and non-uniform illumination • Relieves the requirement for bonding epoxy to be conductive	• Metal interconnection in cross over grid pattern increases the shading for bottom cell • Alignment during the bonding process required for minimizing shading	3J GaInP/GaAs//Si- 25.5% (AM1.5g) [**5**]

1.6 Summary

In summary, III-V multijunction solar cells are regaining attention for integration with Si substrates as a potential solution to address the future levelized cost of energy and to unify the high-efficiency merits of III-V materials with the low-cost and abundance of Si. The current state-of-the-art results for III-V-on-Si solar cells are summarized along with the theoretical performance projections for III-V-on-Si solar cell technology. Several routes for integrating III-V materials with Si substrate are discussed. Important design criteria, challenges and trade-offs between the respective buffer schemes are reviewed in relation to minimizing the dislocation density while enabling thin and optically transparent buffers for realizing Si as an active bottom solar cell. Efficient utilization of the bottom Si substrate as an active subcell would require backside Si substrate engineering to enhance the Si subcell current-density to realize current-matching condition in III-V/Si tandem solar cells.

Among the heteroepitaxial integration approaches, the realization of virtual GaAs-on-Si templates is likely to be the most promising path to realize near-term high-efficiencies; however it is also one of the most challenging paths. Such direct GaAs-on-Si templates could leverage the current state-of-the-art 2J InGaP/GaAs (with active Si subcell) or 3J InGaP/GaAs/InGaAsNSb lattice-matched to GaAs. Although, the graded SiGe buffer choice is more effective in terms of dislocation reduction, such buffers are typically very thick and their smaller bandgap would preclude the use of an active bottom Si subcell. The graded GaAsP buffer approach, on the other hand, offers an optically transparent buffer for active bottom Si subcell with optimal bandgap selection for the top and the middle subcell to realize 3J InGaP/GaAsP/Si solar cells. An interesting path combining the SiGe and the GaAsP approach could utilize SiGe as an active subcell to realize 3J InGaP/GaAsP/SiGe solar cells. In the long-run, research on dilute nitride based lattice matched III-V-N materials on Si and lattice-mismatched InGaN based III-V alloys on Si could also be promising. Among the several mechanical stacking integration approaches, surface activated wafer bonding and direct metal interconnect techniques are the most promising for near-term success of III-V-on-Si mechanically stacked solar cells. However, one of the key challenges yet to be successfully addressed for mechanically stacked solar cells is the realization of bond layers which are not only optically transparent for an active bottom Si subcell, but are also electrically conductive to realize efficient two-terminal concentrated photovoltaic operation.

Careful consideration of all these design challenges would be very critical for the success of future high-efficiency and low-cost III-V multijunction solar cells on Si substrate. Combination of these different heteroepitaxial and mechanically stacked integration approaches has now opened a new range of

possibilities for novel III-V multijunction solar cell architectures on Si substrate. With the recent advancements in both the heteroepitaxial and mechanically stacked integration approaches, efficiencies exceeding 40% under concentrated sunlight seems achievable for III-V-on-Si multijunction solar cells, indicating a promising future for III-V-on-Si solar cell technology.

1.7 Dissertation Objective & Organization

The central focus of the dissertation is oriented towards more efficient design and experimental realization of heterogeneously integrated III-V multijunction solar cells on Si substrate utilizing thin buffer layer (< 2 µm). Integration of such III-V multijunction solar cells on significantly cheaper, more robust and large area Si substrates can address the future levelized cost of energy roadmaps by unifying the high-efficiency merits of III-V materials with low-cost and abundance of silicon. One of the key objective is to be able to better understand the material properties and correlate them to enhance the device performance. Simulation provided valuable aid in predicting more efficient cell designs and provided continuous feedback to improve the material quality and hence the device performance. **Fig. 25** shows this critical feedback loop involving iteration of simulation, epitaxial growth, material characterization, device fabrication and cell

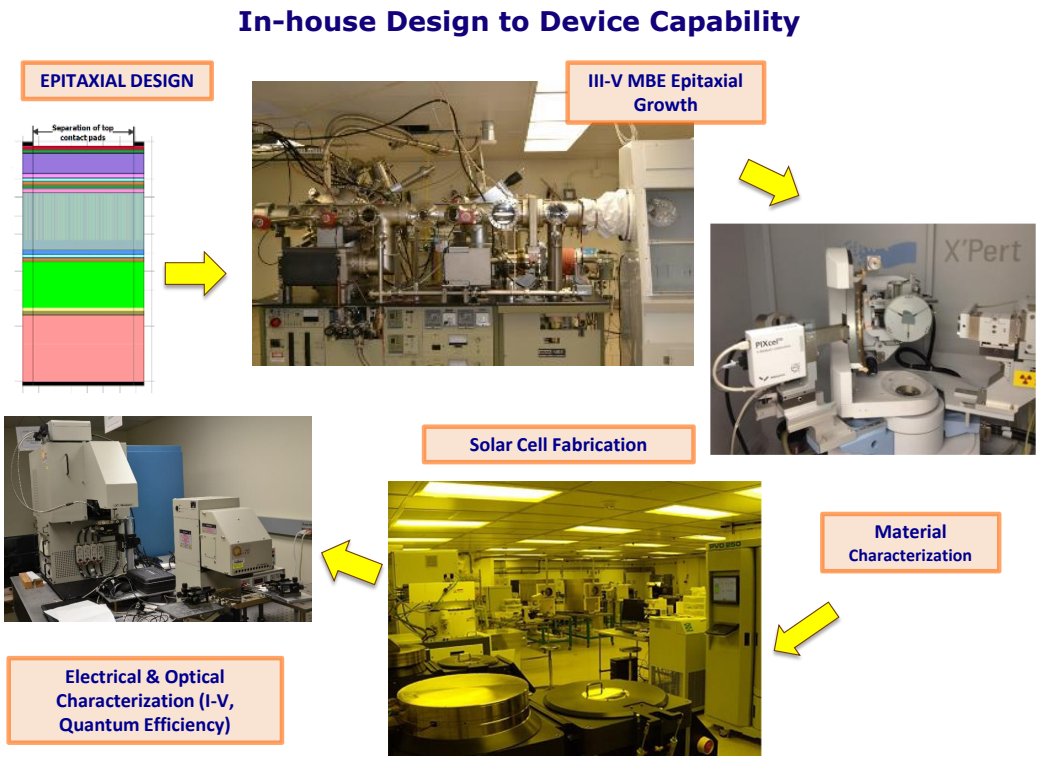

Fig. 25 Feedback loop for complete in-house device optimization, starting from epitaxial device design and simulation, material growth and characterization, solar cell fabrication and final solar cell electrical and optical testing.

testing with focus on correlating material properties to device performance in this disseration. The research encompasses the design of dual-junction (2J) InGaP/GaAs solar cells on Si substrate and triple-junction (3J) InGaP/GaAs//Si solar cells on an active Si substrate for both 1-sun and concentrated sunlight applications. Using comprehensive modeling designs coupled with realistic material parameters, we predicted the optimal performance of such 2J and 3J III-V solar cells on Si substrate taking into account the dislocation density. The findings will be prove to be very valuable for closing the performance gap between lattice-mismatched III-V solar cells on Si substrate and lattice-matched III-V solar cells on GaAs substrate. On the experimental front, the goal is to realize non-selective area and high-quality III-V compound semiconductors on Si using thin buffer layers and evaluate their quality using various material characterization techniques. Finally, fabricate III-V-on-Si solar cells using our in-house epitaxial material and investigate the solar cell performance.

The dissertation is organized into seven chapters. ***Chapter 1*** introduces to the motivation for III-V-on-Si solar cells research. An overview of the current state-of-the-art for III-V-on-Si solar cells is presented along with the theoretical performance projections for III-V-on-Si solar cell technology. Next, key design considerations and integration challenges associated with both heteroepitaxial approach and wafer-bonding approach are discussed, highlighting the key merits of each approach.

Chapter 2 focuses on the modeling and design aspect of dual-junction (2J) InGaP/GaAs solar cells on Si and triple-junction (3J) InGaP/GaAs//Si solar cells on Si for operation under 1-sun and concentrated sunlight. The objective is to understand if we could carefully engineer the cell design to close the gap between the performance of lattice-mismatched III-V solar cells on Si and lattice-matched III-V solar cells. Some of the questions addressed include - (i) how high dislocation density can metamorphic 2J and 3J III-V solar cells designs on Si tolerate without significant performance degradation; (ii) are the subcells with higher bandgap more sensitive to threading dislocations in comparison to subcells with lower bandgap; (iii) is the degradation in current (in comparison to the voltage), a bigger factor affecting the cell performance due to dislocation; (iv) how does the cell design alter for operation under concentrated sunlight; (v) what are the trade-offs in adding Si substrate as an active subcell below 2J InGaP/GaAs solar cells.

Chapter 3 presents the epitaxial growth of III-V compound semiconductors on Si substrate using molecular beam epitaxy (MBE). Epitaxy fundamentals and different growth modes are discussed. Next, we discuss the growth sequence for thin direct GaAs (< 2 μm) buffers on Si and the subsequent III-V solar cell growth on Si substrate. The key knobs (such as temperature, flux and V/III ratio) influencing the initial GaAs buffer growth are investigated. We also discuss the structural properties of 1J GaAs-on-Si solar cell structures realized by utilizing an intermediate GaAsSb single-strained layer. Material characterization results for

evaluating the structural properties of III-V-on-Si solar cell structures are discussed involving a combination of techniques including - (i) in-situ reflection high-energy electron diffraction (RHEED), (ii) X-ray diffraction (XRD) to investigate compositions and strain relaxation properties, (iii) transmission electron microscopy (TEM) to understand defects and dislocation propagation and gauge into the crystalline quality and (iv) atomic force microscopy (AFM) to characterize the surface morphology.

Chapter 4 concentrates on the fabrication process for III-V-on-Si solar cells. Correlating the structural properties to device performance, our motivation for introducing all front side metal contacts is presented. Key process integration challenges including the mesa-etching, grid-finger lithography optimization are discussed. Role of simulation in aiding the importance of critical fab steps, such as cap layer etching and design of anti-reflection coating is also discussed.

In ***chapter 5***, we present the electrical and optical characterization results of our fabricated III-V-on-Si solar cells to evaluate their performance under AM1.5g spectrum (1-sun). The light and dark I-V characteristics, quantum efficiency, reflectance and contact resistance analysis are discussed. The significance of utilizing both front-side metal contacts for III-V-on-Si solar cells is also highlighted. Key factors limiting the performance of "GaAs-on-Si" solar cells are identified, and on-going research efforts focused on minimizing threading dislocation density are discussed.

In ***chapter 6***, we present our preliminary results on a very promising alternate path for integrating III-V solar cells on Si substrate by utilizing high-quality and thin Ge layers grown directly on Si substrate. The goal is to leverage the virtual "Ge-on-Si" substrates for subsequent lattice-matched growth of GaAs to realize III-V-on-Si multijunction solar cells. Modeled 1-sun performance of 3J InGaP/GaAs/Si-Ge solar cells and the excellent material quality achieved for epitaxial Ge directly grown on Si substrate lays a strong foundation towards realizing virtual "Ge-on-Si" template, indicating a promising future for monolithically integrated, low-cost and high-efficiency III-V-on-Si photovoltaics.

Chapter 7 summarizes the key findings and accomplishments of this research. We also highlight important lessons learnt during this research. Potential research direction to pursue heterogeneous integration of III-V-on-Si solar cell research is presented. Finally, we conclude with the prospects, opportunities and future outlook towards further advancing the performance of III-V-on-Si multijunction solar cells.

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Chapter 2

III-V-on-Si Solar Cell Device Design and Modeling

Publication for Section 2.2

N. Jain, M. K. Hudait, “Design of metamorphic dual-junction InGaP/GaAs solar cell on Si with efficiency greater than 29% using finite element analysis,” in *Proc. 38th IEEE Photovoltaic Spec. Conf.*, pp. 002056-002060, 2012.

N. Jain, M. K. Hudait, “Impact of Threading Dislocations on the Design of GaAs and InGaP/GaAs Solar Cells on Si Using Finite Element Analysis,” *IEEE J. Photovoltaics*, vol. 3, pp. 528-534, 2013.

Publication for Section 2.3

N. Jain, and M.K. Hudait, "Design and Modeling of Metamorphic Dual Junction InGaP/GaAs Solar Cells on Si Substrate for Concentrated Photovoltaic Application," *IEEE J. Photovoltaics*, vol. 4, pp.1683-1689, 2014.

Publication for Section 2.4

N. Jain, Y. Zhu, M. Clavel, P. Goley, M. K. Hudait, "Performance Evaluation of Monolithically Integrated 3J InGaP/GaAs/Si Tandem Solar Cells for Concentrated Photovoltaics", *40th IEEE Photovoltaic Spec Conf.*, Denver, CO, USA, 8-13 June, pp. 1152-1157, 2014.

This chapter focuses on the modeling and design aspect of dual-junction (2J) InGaP/GaAs solar cells on Si and triple-junction (3J) InGaP/GaAs//Si solar cells on Si for operation under 1-sun and concentrated sunlight. The objective is to understand if we could carefully engineer the cell design to close the gap between the performance of lattice-mismatched III-V solar cells on Si and lattice-matched III-V solar cells. Some of the questions addressed include - (i) how high dislocation density can metamorphic 2J and 3J III-V solar cells designs on Si tolerate without significant performance degradation; (ii) are the subcells with higher bandgap more sensitive to threading dislocations in comparison to subcells with lower bandgap; (iii) is the degradation in current (in comparison to the voltage), a bigger factor affecting the cell performance due to dislocation; (iv) how does the cell design alter for operation under concentrated sunlight; (v) what are the trade-offs in adding Si substrate as an active subcell below 2J InGaP/GaAs solar cells.

2.1 Modeling Background

Finite element analysis is one of the preferred modeling approach for solar cells as this method allows the flexibility to vary multiple parameters simultaneously, namely – lifetime, surface recombination velocities, band-gaps, anti-reflective coating design, material compositions, doping-type, doping concentration, layer thicknesses etc. This numerical simulation platform enables the investigation of individual parameters as well as coupled parameters in a much faster environment compared to analytical solutions. The modeling process for optimizing our III-V multijunction solar cell designs was performed using the APSYS simulator, a general-purpose 2D/3D finite element analysis and modeling software for semiconductor devices. Finite-element method (FEM) is a numerical technique for finding the approximate solutions to boundary value problems. Analogous to the idea of connecting many tiny straight lines to form a circle, FEM combines many simple element equations over many small subdomains, named finite elements, to approximate a more complex equation over a larger domain. For solar cell modeling, 2D simulations were performed using the APSYS simulator, which solves several interwoven equations, including the Poisson's equation and the drift-diffusion equation for electron and holes using FEM. These finite elements are represented through mesh design in the device structures, wherein the density of mesh points and the spacing arrangement between various mesh points can be defined. For instance, the regions in a device which are more sensitive to the device performance can be assigned with more dense mesh design with mesh points closely spaced. In a solar cell, these high density mesh regions include most of the interfaces, the base layer and the tunnel junctions. The optical propagations in a solar cell, related to the electron-hole generation due to the incident light, are modeled with the transfer matrix method and/or ray tracing by taking into account the reflections at the interfaces. The tunnel junction models incorporate complex Zener-type tunneling

models. All important generation and recombination mechanisms, such as Shockley-Reed-Hall recombination (SRH), spontaneous and Auger recombination, were taken into account.

The most important equations solved by the simulator using FEM are the Poisson's equation and the continuity equation for electrons and holes. The Poisson's equation is as follows:

$$-\nabla.\left(\frac{\varepsilon_0\,\varepsilon_{dc}}{q}\ \nabla V\right) = -n + p + N_D(1 - f_D) - N_A\,f_A + \sum_j N_{tj}\,(\delta_j - f_{tj}) \qquad (2.1)$$

where V is the electric potential, ε_o vacuum dielectric constant, ε_{dc} relative DC or low frequency dielectric constant, q electronic charge, n electron concentration, p hole concentration, N_D the shallow donor density, N_A the shallow acceptor density, f_D occupancy of the donor level, f_A occupancy of the acceptor level, N_{tj} the density of the jth deep trap, f_{tj} the occupancy of the jth deep trap level, δ_j is 1 for donor-like traps and 0 for acceptor-like traps. The current continuity equation for electrons and holes are respectively expressed as:

$$\nabla.J_n - \sum_j R_n^{tj} - R_{sp} - R_{st} + R_{au} + G_{opt}(t) = \frac{\partial n}{\partial t} + N_D\,\frac{\partial f_D}{\partial t} \qquad (2.2)$$

$$\nabla.J_p + \sum_j R_p^{tj} + R_{sp} + R_{st} + R_{au} - G_{opt}(t) = -\frac{\partial p}{\partial t} + N_A\,\frac{\partial f_A}{\partial t} \qquad (2.3)$$

where J_n and J_p are electron and hole current flux density respectively. $R^{tj}{}_n$ and $R^{tj}{}_p$ are the electron and hole recombination rates per unit volume through the jth deep trap, respectively. G_{opt} is the optic generation rate, R_{sp}, R_{st}, and R_{au} are the spontaneous recombination rate, the stimulated recombination rate and the Auger recombination rate per unit volume, respectively.

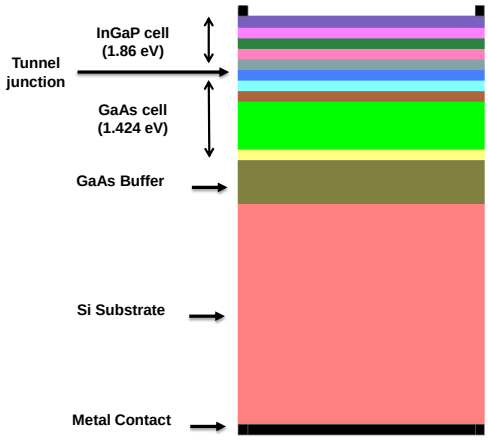

Fig. 1 LayerBuilder schematic of 2J InGaP/GaAs solar cell on Si substrate.

The most important files in a simulation project include: (i) layer file, (ii) sol file and the (iii) plt file. The device structure is defined in the layer file, which can also be set up in the LayerBuilder. The LayerBuilder schematic of our 2J InGaP/GaAs solar cell structure on Si is shown in **Fig. 1**. Multiple columns can be constructed which are useful in defining the metal contacts. The mesh design is defined in the layer file. Using the layer file, user can define the material composition, doping-type, doping concentration, layer thicknesses and metal contact (Schottky vs. Ohmic). The sol file or the main solver lets the user define material parameters such as the band-gaps, minority carrier lifetimes, surface recombination velocities, tunnel junction position, anti-reflecting coating design as well as the associated reflection/transmission properties and the incident solar spectrum. The simulation parameters in terms of the current/voltage sweep range and step size are also defined in the sol file. The simulator generates files for the mesh, material and doping from the layer file. The main solver for simulating the device utilizes all of these files. The plt file lets the user define the plot description, the axis range and also allows the extraction of important solar cell parameters such as the η, V_{oc} and J_{sc}. The complete modeling sequence is described through a flow chart, as shown in **Fig. 2**.

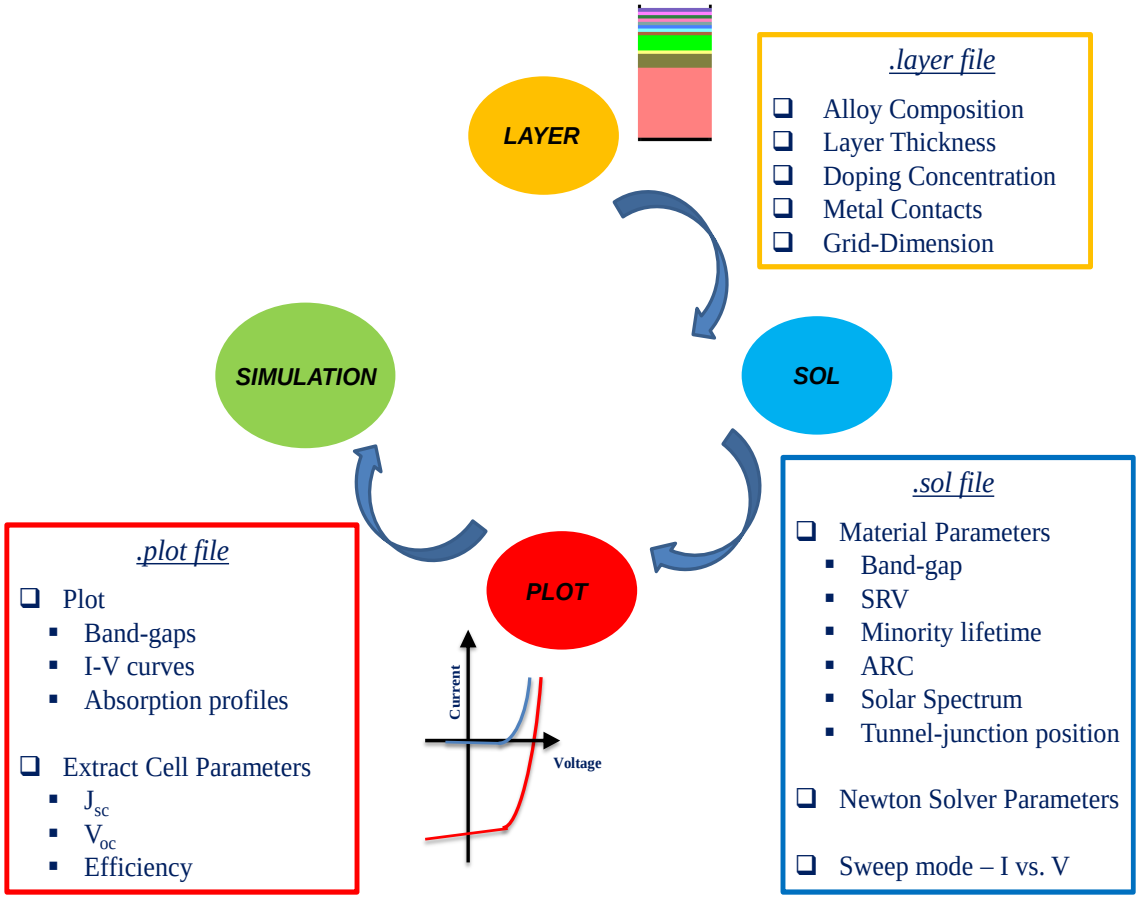

Fig. 2 Flow chart of the modeling sequence in APSYS.

2.2 Single-Junction GaAs & Dual-Junction InGaP/GaAs Solar Cell Design on Si for 1-Sun

Multijunction III-V solar cells are the dominant choice for space satellite power primarily due to their high efficiencies under concentrated sunlight [**1-4**]. Efficiencies as high as 43.5% have been demonstrated for GaInP/GaAs/GaInNAs III-V solar cells under 418x suns [**5**]. However, the higher cost of Ge and III-V substrates have restricted the widespread commercialization of III-V solar cells. Heteroepitaxy of III-V materials on large diameter, cheaper and readily available Si substrate can not only offer a path for low cost and high efficiency III-V cells, but also significantly increase their yield per die. Furthermore, implementation of III-V solar cells on Si in conjunction with substrate re-use technologies [**6, 7**] can lead to additional cost savings. However, viability of III-V InGaP/GaAs solar cells on Si relies on the ability to grow high quality GaAs on Si with careful lattice engineering and substrate treatment. The polar on non-polar epitaxy and the 4% lattice-mismatch between GaAs and Si may results in formation of various defects including dislocations. These dislocations can propagate into the photoactive cell region, significantly impede the minority carrier lifetime and hence the overall cell performance [**8-11**].

We provide a systematic study on the correlation of threading dislocation density (TDD) and minority carrier lifetime on the 1J and 2J cell figure-of-merits, namely, efficiency (η), open-circuit voltage (V_{oc}), short-circuit current density (J_{sc}) and fill factor (FF). The schematic of the 2J InGaP/GaAs cell structure investigated is shown in **Fig. 3**. As a starting point in our simulation, the base thicknesses in the GaAs and

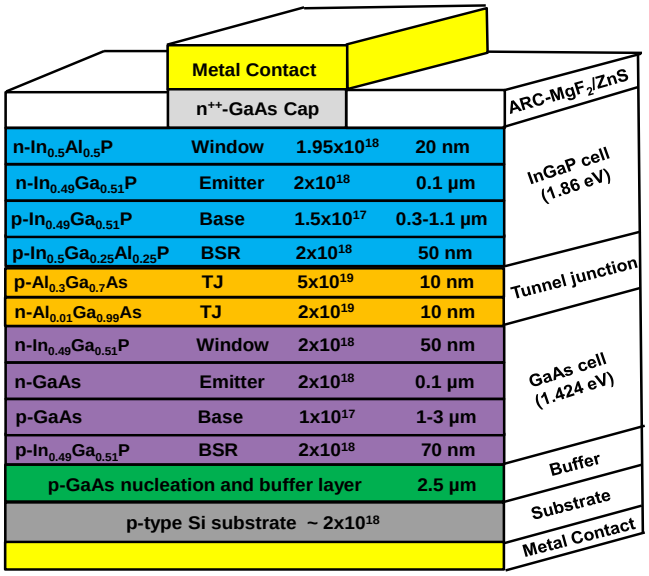

Fig. 3 Schematic of 2J InGaP/GaAs solar cell on Si [**30**]. Used with permission from IEEE, 2013.

InGaP cell were set to be 2.5 μm and 0.9 μm, respectively [**1**]. We then discuss our design methodology to engineer the metamorphic 2J InGaP/GaAs cell structure on Si to achieve the current-matching condition between the subcells at a TDD of 10^6 cm^{-2}. The results from our detailed cell modeling provide a quantitative assessment of solar cell figure-of-merits as a function of TDD, thus enabling more efficient cell design and prediction of the metamorphic 2J cell performance on Si.

The impact of TDD on cell performance has been previously investigated [**9-14**], however, their analysis was limited to only 1J GaAs cell on Si. For modeling the impact of TDD on $V_{oc,}$ J_{sc} was assumed to be independent of TDD [**13**]. In reality J_{sc} decreases with increase in TDD and may have a significant impact on the extraction of efficiency. Recently, the impact of minority carrier lifetime on cell performance was investigated for InGaN cells on Si [**15**]. Recently, the effect of dislocations in metamorphic III-V tandem cells was also investigated, but did not incorporate any substrate [**16**]. There has not been significant work done on the modeling-assisted design of metamorphic tandem solar cells incorporating the impact of TDD. We provide the first study on the modeling and the optimization of metamorphic 2J n^+/p InGaP/GaAs solar cell on Si at AM1.5g spectrum using finite element analysis without assuming a constant J_{sc}.

2.2.1 Simulation Model, Assumptions & Calibration

Minority carrier lifetime is one of the most important figure -of-merit for the design of metamorphic solar cells. Defects and dislocations generated at the III-V/Si heterointerface may serve as recombination centers and decrease the minority carrier lifetime and hence their diffusion length. The effective minority carrier lifetime (τ_n or τ_p) in a lattice-mismatched system varies as a function of TDD (f (τ_{TDD})) [**12, 24**] and is expressed as,

$$\frac{1}{\tau_{n,p}} = \frac{1}{\tau^0_{n,p}} + \frac{1}{\tau_{TDD}} \qquad (1)$$

where $\tau°_p$ and $\tau°_n$ are the minority carrier lifetime for a dislocation free material. The τ_{TDD} is the minority carrier lifetime associated with the recombination at dislocation and can be expressed as,

$$\tau_{TDD} = \frac{4}{\pi^3 (TDD) D} \qquad (2)$$

where D is the minority carrier diffusion coefficient and TDD is the threading dislocation density in cm^{-2}.

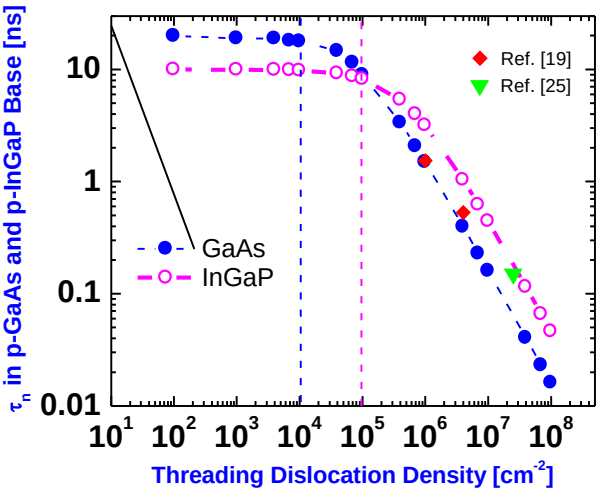

Fig. 4 Correlation of threading dislocation density on minority electron lifetime in p-GaAs and p-InGaP base [**30**]. Used with permission from IEEE, 2013.

Using the model described above, coupled with the material parameters summarized in **Table I**, we computed the impact of TDD on the minority electron lifetime in p-GaAs and p-InGaP base as shown in **Fig. 4**. Impact of TDD on minority carrier lifetime has been previously investigated in GaAs material [**13**]. From **Fig. 4**, it can be noted that for TDDs greater than 10^4 cm^{-2} in GaAs subcell, the minority electron lifetime significantly degraded. The onset of degradation in minority electron lifetime occurs at a higher TDD (10^5 cm^{-2}) in InGaP subcell compared to GaAs subcell due to the lower electron diffusion coefficient in p-InGaP material. By utilizing the minority electron lifetime variation as a function of increasing TDD, coupled with the material parameters incorporated from **Table I**, we simulated the impact of TDD on the performance of 1J GaAs and 2J InGaP/GaAs solar cell on Si [**23**]. The experimental lifetime values for p-GaAs (red) and p-InGaP (green) are included in this figure [**19, 25**], indicating an excellent agreement between the model and experiment.

In a solar cell, most of the light is absorbed in the thick base and the minority carriers generated far away from the junction should have sufficient lifetime to reach the junction before being recombined. Therefore, the variation of the minority electron lifetime in the base (τ_n) was found to have a significant impact on the cell performance. The minority hole lifetime (τ_p) in the thin emitter was considered to be constant. The surface recombination velocity (SRV) was set to 10^4 cm/s for both holes (S_p) and electrons (S_n) at InGaP base/back reflector interface and emitter/window interface. The corresponding S_n and S_p values were set to 10^6 cm/s at both the interfaces in the GaAs subcell. In our model, the mobility of minority carriers was

TABLE I

GaAs and InGaP material and transport parameters [**30**]. Used with permission from IEEE, 2013.

Parameters (Abbreviation, Units)	GaAs	InGaP
Band-gap (E_g, eV)	1.424	1.86
Minority electron mobility ($\mu_{e'}$, cm^2Vs)	3088.8	1074 [**20**]
Minority hole mobility ($\mu_{h'}$, cm^2/Vs)	100 [**17**]	40 [**20**]
Electron diffusion coefficient (D_n, cm^2/s)	80 [**18**]	27.816
Hole diffusion coefficient (D_p, cm^2/s)	2.59	1.036
Peak minority electron lifetime ($\tau°_n$, ns)	20 [**12, 19**]	10 [**21, 22**]
Minority hole lifetime ($\tau°_p$, ns)	2.5	1

assumed to be independent of TDD [**24**] and the effect of band-gap narrowing and grid-shadowing were not included. Therefore, the analysis discussed here provides an upper bound for the modeled cell results.

We calibrated our model with the 2J InGaP/GaAs cell structure in [**26, 27**]. A τ_n value of 5.2 ns in p-InGaP was reported in [**26**]. This value of lifetime corresponds to a TDD of $4x10^5$ cm^{-2} as shown in **Fig. 4**. Since, the value of τ_n in p-GaAs was not provided, a τ_n value of 3.3 ns was used from **Fig. 4**. The simulation results are compared to the experimental results in **Table II**. Overall, the simulated and the experimental values presented in **Table II** are in agreement, thus validating our model and the parameters utilized in the simulation.

The next section is divided into four subsections. First, the impact of minority carrier lifetime degradation on the performance of 1J GaAs cell on Si and 2J InGaP/GaAs cell on Si are discussed, respectively. Next, we describes our design methodology to engineer the 2J InGaP/GaAs cell structure on Si to realize current-matching between each subcell at a TDD of 10^6 cm^{-2}. Finally, we discuss the impact of surface recombination on the 2J cell performance.

TABLE II

Model calibration with 2J InGaP/GaAs experimental data [**30**]. Used with permission from IEEE, 2013.

	V_{oc} (V)	J_{sc} (mA/cm^2)	FF (%)	Efficiency (%)
Experiment [**26**]	2.48	14.22	85.6	30.28
Simulation	2.41	13.85	88.9	29.80
Experiment [**27**]	2.52	12.70	85.00	27.20
Simulation	2.58	12.53	85.19	27.64

2.2.2 Design of Single-Junction (1J) GaAs Solar Cell on Si

The p-GaAs base thickness in the 1J n^+/p GaAs cell on Si was set to 2.5 μm. The TDD in this GaAs cell was varied from 10^4 cm^{-2} to 10^8 cm^{-2}. At a TDD of 10^6 cm^{-2}, the minority electron lifetime in p-GaAs was calculated to be 1.49 ns, as shown in **Fig. 4**, consistent with the experimentally determined minority electron lifetime of 1.5 ns in p-GaAs [**19**].

Voltage at maximum power point, V_m and V_{oc} were plotted as a function of increasing TDD in the 1J GaAs cell on Si as shown in **Fig. 5(a)**. At lower TDD, the higher value of both V_{oc} and V_m was attributed to the higher minority electron lifetime in the p-GaAs base. TDD below 10^5 cm^{-2} had a negligible impact on the V_{oc}. However, beyond this TDD, V_{oc} started to degrade significantly. V_{oc} has a logarithmic dependence on reverse saturation current density, J_0 which is inversely proportional to the minority carrier lifetime. Thus, at higher TDD, significant degradation in both V_{oc} and V_m was attributed to the higher reverse saturation current density pertaining to the reduced minority electron lifetime.

Current density at maximum power point, J_m and J_{sc} were plotted as a function of TDD in the 1J GaAs cell on Si as shown in **Fig. 5(b)**. For a TDD below $4x10^5$ cm^{-2}, the minority electrons had sufficient lifetime to reach the junction before being recombined and hence, TDD below $4x10^5$ cm^{-2} had a negligible impact on the J_{sc}. For the 1J GaAs cell considered here, a τ_n value of at least 0.78 ns (at a TDD of $2x10^6$ cm^{-2}) was

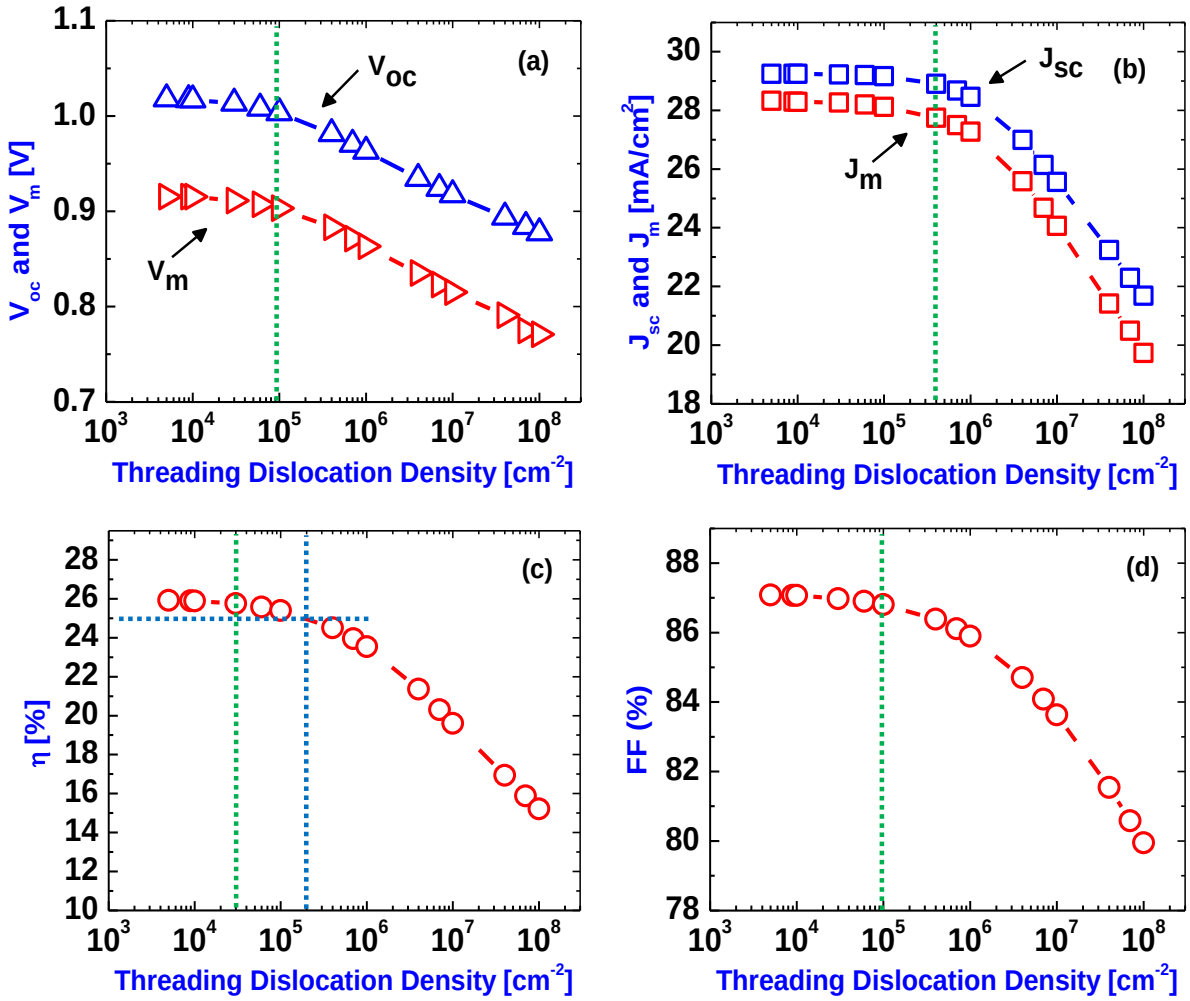

Fig. 5 Impact of threading dislocation density variation on 1J GaAs cell performance parameters: (a) V_{oc} and V_m, (b) J_{sc} and J_m, (c) η and (d) FF at AM1.5g spectrum [**30**]. Used with permission from IEEE, 2013.

necessary for the cell to function as a short diode. Beyond a TDD of $2x10^6$ cm^{-2}, the cell behaved like a long diode with the electron diffusion length becoming shorter than the GaAs base thickness. Thus, beyond a TDD of $2x10^6$ cm^{-2}, the degradation in both J_{sc} and J_m was attributed to the reduction in minority electron lifetime. Interestingly, from **Fig. 5(a)** and **5(b)**, it can be seen that the beginning of degradation in J_{sc} occurred at a higher TDD than V_{oc}, indicating J_{sc} being more tolerant to TDD in the 1J GaAs cell on Si.

Fig. 5(c) shows the degradation in efficiency of the 1J GaAs cell on Si as a function of increasing TDD. It can be seen that cell efficiency higher than 25% were attained for TDD below $2x10^5$ cm^{-2} (or τ_n greater than 5 ns). However, the cell efficiency significantly degraded beyond a TDD of ~10^5 cm^{-2} due to the reduction in both J_m and V_m, as discussed earlier. At an experimentally realistic TDD of 10^6 cm^{-2} [**28**], the

corresponding cell efficiency was found to be 23.54% while at a higher TDD of 10^7 cm^{-2}, the corresponding cell efficiency degraded to 19.61% due to the reduction in the minority electron lifetime.

The fill factor as a function of increase in TDD was plotted in **Fig. 5(d)**. There was almost negligible drop in fill factor below a TDD of 10^5 cm^{-2}. The percentage drop in both J_m and V_m from a TDD of 10^4 cm^{-2} to 10^8 cm^{-2} was greater than the percentage drop in J_{sc} and $V_{oc,}$ respectively, as can be see from **Fig. 5(a)** and **5(b)**. Thus, at higher TDD, a greater percentage drop in the J_m*V_m product compared to J_{sc}*V_{oc}, led to the degradation in FF.

2.2.3 Design of Dual-Junction (2J) InGaP/GaAs Solar Cell on Si

For the analysis of metamorphic 2J n^+/p InGaP/GaAs cell on Si, the base thicknesses in the GaAs and InGaP subcells were set to 2.5 μm and 0.9 μm, respectively. The TDD was varied from 10^5 to 10^8 cm^{-2} and it was assumed that all the threading dislocations in GaAs bottom subcell propagated to the top InGaP subcell.

Fig. 6(a) shows the degradation in both V_{oc} and V_m as a function of increasing TDD in the 2J InGaP/GaAs cell on Si. The primary reason for the decrease in V_{oc} was due to the strong dependence on the reverse saturation current density, J_{02}, associated with the depletion region recombination. The V_{oc} can be expressed as,

$$V_{oc} = \left(\frac{n_2 kT}{q} \right) \ln \left(\frac{J_{sc}}{J_{02}} \right) \quad (3)$$

where, J_{02} depends on the minority carrier base lifetime, τ_{base} and is expressed as,

$$J_{02} = \frac{q n_i W_D}{2} \left(\frac{1}{\tau_{base}} \right) \quad (4)$$

where, n_i is the intrinsic carrier concentration and W_D is the depletion layer width. At higher TDD, the value of J_{02} increased due to the reduction in minority electron lifetime. Thus, the increase in J_0 led to significant degradation in both V_{oc} and V_m with increasing TDD.

The J_{sc} and J_m in the 2J InGaP/GaAs cell were plotted as a function of increase in TDD in **Fig. 6(b)**. The degradation in both J_{sc} and J_m at higher TDD was due to the simultaneous reduction in the minority electron lifetime in both GaAs and InGaP base. The onset of degradation in J_{sc} in 2J cell configuration was also

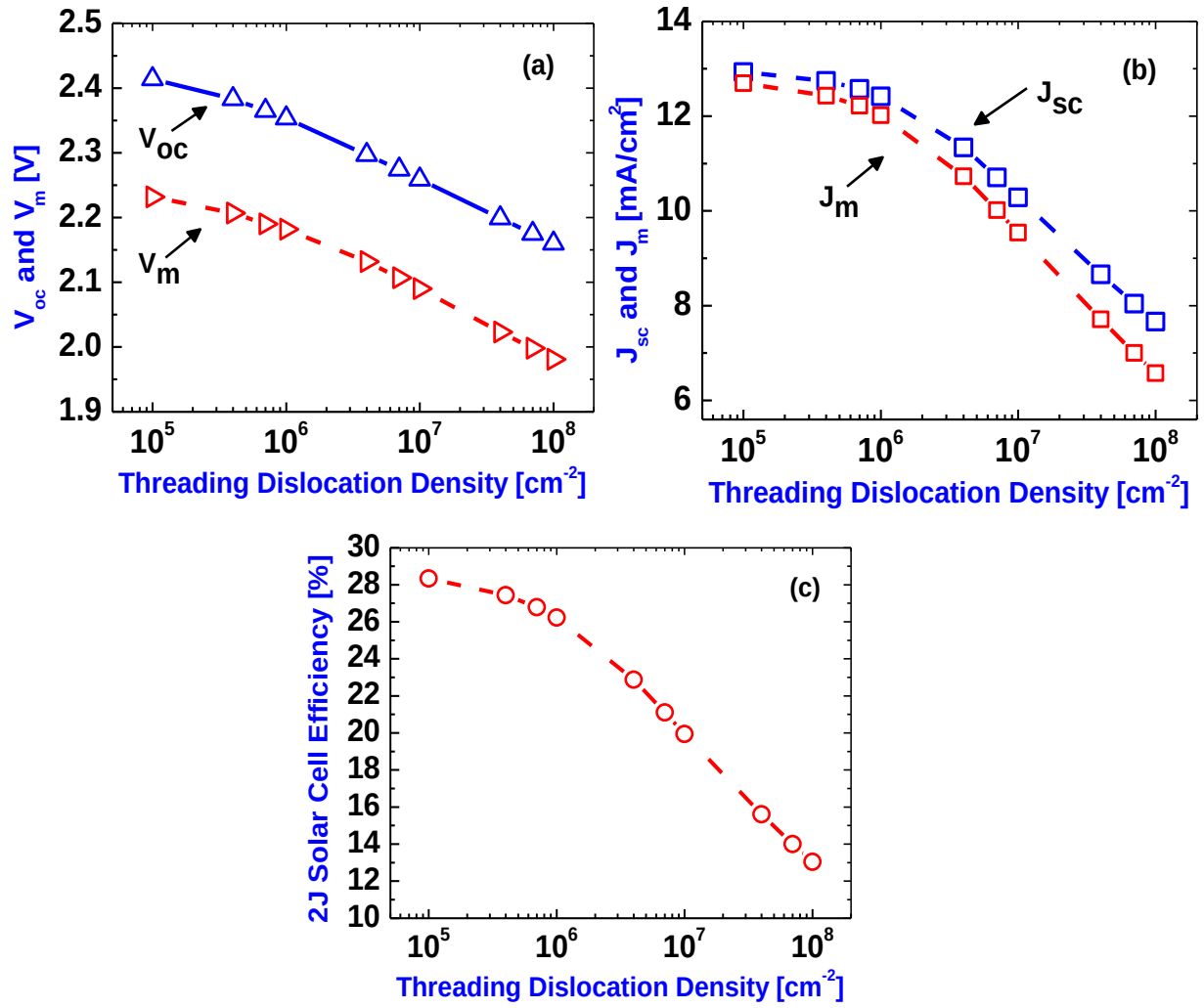

Fig. 6 Impact of threading dislocation density variation on 2J InGaP/GaAs cell performance parameters: (a) V_{oc} and V_m, (b) J_{sc} and J_m and (c) η at AM1.5g spectrum [**30**]. Used with permission from IEEE, 2013.

found to occur at higher TDD compared to V_{oc}, similar to the 1J GaAs cell which was discussed earlier. Thus, J_{sc} was more tolerant to TDD compared to V_{oc} for both 1J GaAs and 2J InGaP/GaAs cells on Si, consistent with prior work [**14**].

Fig. 6(c) shows the degradation of 2J InGaP/GaAs cell efficiency as a function of increasing TDD. At a TDD of 10^6 cm^{-2} in the 2J structure, the corresponding 2J cell efficiency was 26.22%. Beyond a TDD of 10^6 cm^{-2}, the degradation in minority electron lifetime in the p-GaAs significantly hindered the 2J InGaP/GaAs cell efficiency as p-GaAs material was found to be more sensitive to dislocations than the p-InGaP (see

Fig. 4). Above a TDD of 10^7 cm^{-2}, the 2J InGaP/GaAs cell efficiency degraded to that of 1J GaAs cell efficiency, thus, making the contribution of the top InGaP cell redundant.

The J-V characteristics of 2J InGaP/GaAs (red curve) cell, the GaAs subcell (blue curve) and the InGaP subcell (pink curve) were plotted in **Fig. 7** at a TDD of 10^6 cm^{-2}. It can be seen that the subcells were not current-matched and the bottom GaAs subcell limited the J_{sc} in the 2J cell configuration. In practice, it is challenging to improve the material quality of heteroepitaxial GaAs grown on Si to lower the TDD significantly below 10^6 cm^{-2}. Consequently, it becomes extremely important to optimize the metamorphic 2J InGaP/GaAs cell structure on Si at a realistic TDD of 10^6 cm^{-2} by tailoring the design of each subcell.

2.2.3.1 Current-matching in 2J InGaP/GaAs Cell on Si

In a multijunction cell, one of the most important design criteria is to achieve the current-matching between the subcells. Current-matching enables to extract the best performance from a multijunction cell. The cell with a higher band-gap provides a higher V_{oc} and lower J_{sc}. For achieving the current-matching condition, ideally J_m between each subcell should be matched. Here, we used J_{sc} for current-matching as J_{sc} is a directly measurable parameter during cell characterization and it has been widely used for current-matching analysis [**2, 29**].

The subcells in our 2J configuration were not current-matched as shown in **Fig. 7**. Therefore, appropriate design changes in our 2J cell structure were required to realize the current-matching condition between the subcells. In a solar cell, most of the light in absorbed in the thicker base layer and, hence, the minority carrier lifetime in the base plays a critical role in determining the current density contribution from a cell.

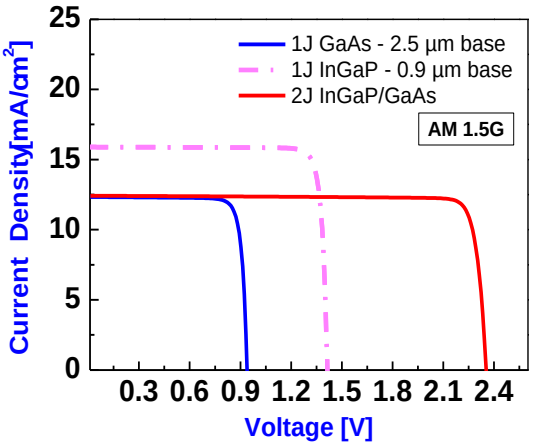

Fig. 7 J-V characteristic of 2J cell along with the InGaP and GaAs subcell before current-matching at a TDD of 10^6 cm^{-2} at AM 1.5g [**30**]. Used with permission from IEEE, 2013.

Thus, we optimized the base thicknesses in the GaAs and the InGaP subcells to achieve current-matching condition at an experimentally realistic TDD of 10^6 cm^{-2} [**28**]. At this TDD, the values of τ_n were 1.494 ns and 3.171 ns in the p-GaAs and the p-InGaP base, respectively, as calculated in **Fig. 6**.

We first varied the thickness of p-InGaP base from 1.1 μm to 0.3 μm in a 1J InGaP cell configuration. This is represented by the blue curve in the **Fig. 8(a)**. Then, in the 2J cell configuration, the thickness of p-InGaP base was again varied over the same range with the GaAs base thickness set to 1 μm (pink curve) as shown in **Fig. 8(a).** The same procedure was repeated for the GaAs base thickness of 2 μm (black curve) and 3 μm (red curve). The InGaP cell structure was the same in both the 1J InGaP and the 2J InGaP/GaAs cell configurations. It can be seen that thinning the base thickness in 1J InGaP cell lowered the J_{sc} due to reduction in the absorption depth for the photons to be absorbed in the p-InGaP base. Interestingly, thinning the InGaP base thickness in the 2J cell configuration allowed more photons through to the bottom GaAs subcell, resulting in an increase of J_{sc} from the GaAs subcell at the cost of reduction in J_{sc} from the InGaP subcell. This resulted in the overall increase in J_{sc} of 2J cell as the bottom GaAs subcell limited the J_{sc} in the 2J cell configuration. Furthermore, as the top cell base was being thinned, increasing the base thickness of the bottom GaAs subcell allowed for additional photons through to the GaAs subcell. This led to further improvement in the overall J_{sc} of the 2J cell. However, further increment in the GaAs base thickness beyond 2 μm did not result in significant improvement of J_{sc}. This was likely due to insignificant photocurrent contribution from the GaAs subcell beyond a base thickness of 2 μm.

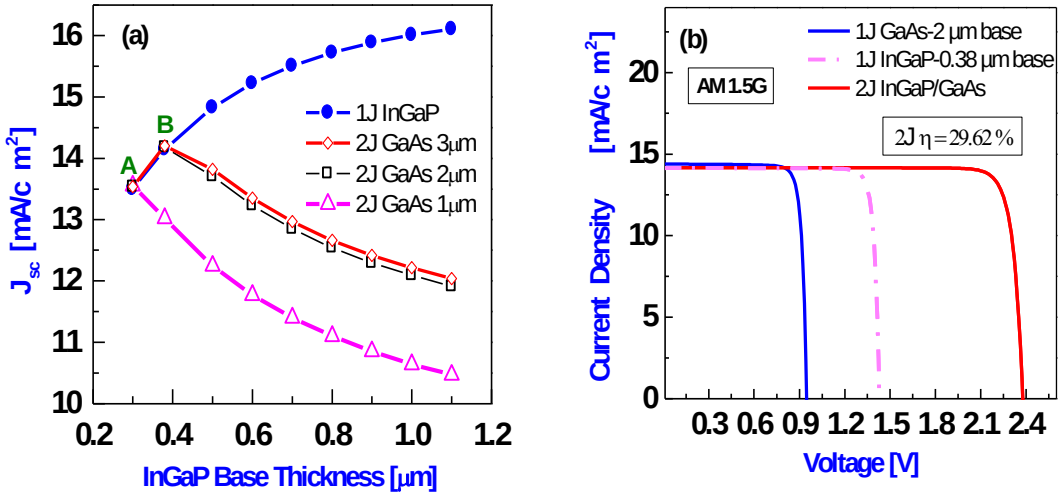

Fig. 8 (a) Short-circuit current density as a function of variation in the base thickness of the InGaP subcell to realize for current-matching, (b) Current-matched J-V characteristic of the 2J InGaP/GaAs cell on Si at AM 1.5g corresponding to the current-matched point B in **Fig. 8(a)** [**30**]. Used with permission from IEEE, 2013.

TABLE III

2J InGaP/GaAs cell parameters at AM 1.5g illumination [**30**]. Used with permission from IEEE, 2013.

2J cell (InGaP/GaAs base thickness in μm)	V_{oc} (V)	J_{sc} (mA/cm^2)	FF (%)	Efficiency (%)
Non-optimized (0.9/2.5)	2.35	12.41	89.73	26.22
Current-matched (0.38/2)	2.37	14.18	88.22	29.62

Utilizing the method discussed above, the current-matching condition was realized at point A (J_{sc}=13.5 mA/cm^2) and B (J_{sc}=14.18 mA/cm^2), as shown in **Fig. 8(a)**. The J-V characteristics of the 2J cell and the individual subcells corresponding to the point B were plotted in **Fig. 8(b)**. At point B, the 2J cell exhibited a conversion efficiency of 29.62% with a 2 μm and a 0.38 μm thick GaAs and InGaP base, respectively. The cell parameters extracted after achieving the current-matching condition between the two subcells at a TDD of 10^6 cm^{-2} were summarized in **Table III**. These results illustrate that even at a TDD of 10^6 cm^{-2}, an efficiency of greater than 29% can be realized for a metamorphic 2J InGaP/GaAs solar cell on Si by carefully engineering the cell design. To further verify the results from this simulation study, experimental work is underway.

2.2.3.2 Impact of Surface Recombination on 2J InGaP/GaAs Cell

Interface recombination could be a major factor limiting the performance of a tandem cell. Recombination at top cell interfaces was found to have the most detrimental impact [**20**]. In our design, the thickness of the top InGaP subcell was significantly reduced, hence, it was important to analyze the impact of SRV on the overall 2J cell performance. **Fig. 9** shows the impact of SRV at top InGaP subcell interfaces on the 2J cell η and J_{sc}. Initially, all the SRVs were set to 10^0 cm/s at all the interfaces in the GaAs and the InGaP subcells. Thereafter, the SRV was set to 10^6 cm/s in the GaAs subcell, while the SRV in the InGaP subcell was varied. It can be seen that the SRV, when below 10^4 cm/s in the InGaP subcell, had negligible impact on the efficiency of the 2J cell. However, the efficiency dropped to 27.35% at a SRV of 10^6 cm/s due to degradation

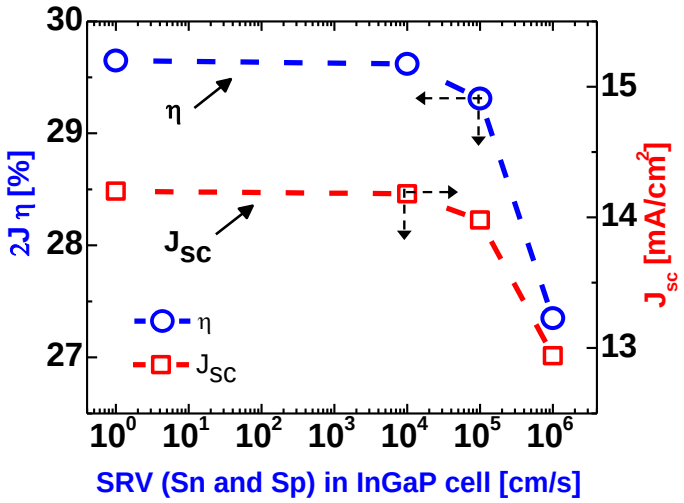

Fig. 9 2J InGaP/GaAs cell η and J_{sc} as a function of SRV in the top InGaP subcell [**30**]. Used with permission from IEEE, 2013.

in J_{sc}. Thus, it is important to restrict the SRV below 10^4 cm/s in the InGaP subcell to achieve high efficiency 2J InGaP/GaAs cell on Si.

Summary

We have investigated the impact of threading dislocation density on the performance of 1J n^+/p GaAs and 2J n^+/p InGaP/GaAs cell on Si at AM 1.5g spectrum. Using our calibrated model, simulation predicts an efficiency of greater than 23% for 1J GaAs cell on Si at AM1.5g spectrum at a threading dislocation density of 10^6 cm^{-2}. For both 1J and 2J cell configurations, the onset of degradation in V_{oc} was found to occur at a lower TDD than in J_{sc}, indicating that V_{oc} was more sensitive to threading dislocation density.

The 2J InGaP/GaAs cell at a TDD of 10^6 cm^{-2} exhibited an efficiency of 26.22% with a 2.5 μm and 0.9 μm thick GaAs and InGaP base, respectively. The design of the metamorphic 2J InGaP/GaAs cell on Si was optimized at a TDD of 10^6 cm^{-2} to achieve current-matching between the two subcells. By thinning the top InGaP cell from 0.9 μm to 0.38 μm, the 2J cell efficiency increased to 29.62% from 26.22%. Also, at the interfaces in the top InGaP subcell, the surface recombination velocities below 10^4 cm/s had negligible impact on the 2J cell performance. Thus, even in a lattice-mismatched 2J InGaP/GaAs cell on Si with TDD of 10^6 cm^{-2}, a theoretical conversion efficiency of greater than 29% at AM1.5g is achievable by tailoring the device design. Once experimentally realized, the III-V cell technology on Si would offer a new paradigm for the advancement of low cost III-V solar cells and foster innovative avenues for both space and terrestrial applications.

2.3 Dual-Junction InGaP/GaAs Solar Cell Design on Si for Concentrated Photovoltaics

Multijunction III-V compound semiconductor solar cells have been the dominant choice for space applications; however, their expensive cost has limited their application for the terrestrial sector. Concentrated photovoltaic (CPV) systems utilizing III-V multijunction cells provides a great promise for delivering electrical power at lower cost than traditional flat-plate systems [**1**]. Under high sun concentration, the concentrator begins to dominate the overall system cost as the cell size becomes much smaller and the economics becomes strongly influenced by the efficiency-concentration relationship. The relatively small cell size reduces the amount of material and consequently, the system cost.

Most of the III-V solar cells utilized in CPV systems are grown on either GaAs or Ge substrate, both of which are not only smaller in diameter, but are also more expensive than Si Direct integration of III-V semiconductors on large diameter, cheaper and readily available Si substrate is highly desirable for increased density, low-cost and lightweight photovoltaics. III-V integration on Si unifies the excellent optical properties of III-V materials with the volume manufacturability of Si, allowing a path for significantly driving down the cost. Furthermore, III-V on Si technology is also attractive for integration with commercially available substrate re-use techniques such as spalling [**2**] and epitaxial lift-off [**3-5**] to explore additional cost saving schemes. The approach of direct GaAs on Si epitaxy could be extended to record efficiency 3J solar cells that utilize dilute nitride cell [**6**] as well as with the state-of-the-art inverted metamorphic solar cells [**7**]. However, polar on non-polar epitaxy, thermal mismatch, and 4% lattice-mismatch makes the growth of GaAs on Si challenging, rendering the metamorphic solar cell sensitive to dislocations.

We have recently modeled a 2J InGaP/GaAs cell on Si with a theoretical efficiency greater than 29% (1-sun) at a threading dislocation density (TDD) of 10^6 cm^{-2} by carefully engineering the cell design and by realizing the current-matching condition taking into account the TDD [**8,9**]. Experimental 2J InGaP/(In)GaAs based solar cells have been an integral part of most of the high efficiency multijunction solar cells [**6,7,10,11**]. The highest 1-sun efficiency reported for monolithic 2J InGaP/GaAs cell on Si is 18.6% [**12**]. There has not been significant experimental or theoretical work done on the monolithic integration of 2J InGaP/GaAs solar cells on Si for operation under concentrated sunlight, which takes into account the impact of TDD. To the best of our knowledge, this is the first simulation study on the CPV performance of metamorphic 2J InGaP/GaAs solar cells on Si substrate which takes into account the impact of TDD using finite element analysis [**13**]. The results from our work will be useful for future design and optimization of metamorphic 3J and beyond III-V solar cells on Si substrate.

2.3.1 Theory and Modeling Process

In CPV systems, lenses focus the sunlight onto a small area cell, enabling higher efficiency under concentrated sunlight. Typically, the current density of a solar cell is proportional to the intensity of the incident light and inversely proportional to the cell area. The efficiency increases with the concentration until series resistance or cell heating begins to limit the performance. For lattice-matched 2J InGaP/GaAs cells, an absolute 4% drop in efficiency was observed for the cell operating at ~100°C compared to ~25°C [**14**]. However, extremely small 2J cells (0.36 mm^2) have been previously used under ~1000x concentration without employing heat sinks for passive cooling [**3**]. Since we have utilized small cell dimensions (≤ 0.25 mm^2) in our model, we neglected the cell heating under concentrated sunlight for our prototype cells.

2.3.1.1 CPV Design Consideration for Metamorphic III-V Solar Cells on Si

The most important design aspects for maximizing the CPV performance of multijunction solar cells includes the (i) realization of current-matching, (ii) optimization of the design trade-offs between the front metal shadowing and the series resistance, and (iii) proper tunnel-junction design. An additional aspect that becomes extremely important for designing metamorphic tandem cells for CPV is the optimization of all these parameters taking into account the impact of TDD.

We have utilized our calibrated model for 2J InGaP/GaAs cell on Si under AM1.5g [**9**] as the first step. The entire structure is metamorphic with respect to Si substrate; however, the III-V subcells are internally lattice matched. Although, the InGaP subcell was lattice-matched to the bottom GaAs subcell, all the threading dislocations (TDs) generated due to the mismatch between GaAs and Si were assumed to propagate into the top InGaP subcell. We utilized the same material and device parameters, namely, band gaps, minority carrier mobility and lifetimes, diffusion coefficients, and surface recombination velocities [**9,15-21**] to evaluate the CPV performance under AM1.5d (900 W/m^2). Utilizing an incident power density of 1000 W/m^2 would only alter the efficiency and not affect any of the other solar cell parameters. The schematic of the 2J InGaP/GaAs cell structure on Si is shown in **Fig. 10**. The grid finger-pitch was defined as the end-to-end distance between two adjacent fingers, each being 2μm wide.

2.3.1.2 Tunnel Junction Design under Concentrated Sunlight

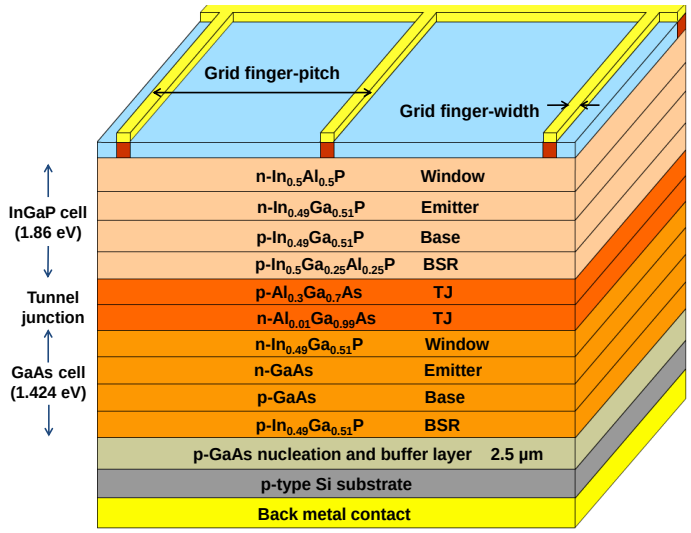

Fig. 10 Schematic depiction of 2J InGaP/GaAs solar cell on Si [**32**]. Used with permission from IEEE, 2014.

The tunnel junctions (TJs) may limit the overall performance if the current density of the solar cell exceeds the peak tunneling current density ($J_{T\text{-}Peak}$) of the TJ. However, it is extremely challenging to estimate the carrier lifetimes in the heavily doped TJs at a given TDD. Therefore, for the simplification of our analysis, the AlGaAs/GaAs TJ in our cell structure was assumed to be unaffected at a TDD of 10^6 cm^{-2}. The potential risk of reduction in $J_{T\text{-}Peak}$ due to TDD can be mitigated by utilizing AlGaAs/GaAs quantum-well TJs, which have $J_{T\text{-}Peak}$ over 300 A/cm^2, equivalent to operation under 20,000 suns [**22**].

2.3.1.3 Series Resistance Losses during Grid Design

Typically, the degradation in cell performance under high concentration due to series resistance is attributed to the (i) shadowing losses due to front grid obscuration, (ii) resistance of the epitaxial layers including the sheet resistance of the window-emitter layers, (iii) contact resistance at the metal-semiconductor interface, and (iv) resistivity of the metal gridlines. Selecting an appropriate metal stack and the annealing condition during the cell fabrication can minimize the contribution from the latter two factors. Major contributions to the power loss due to series resistance can be attributed to the shadowing of the metal fingers as well as the emitter sheet resistance [**23**]. The optimization of these specific parameters is therefore extensively addressed in this work.

There have been several methods proposed for characterizing the series resistance of a solar cell [**24-28**]. Most of the methods are based on computing slopes and may require current-voltage (I-V) measurements at multiple concentration [**27**] or both light and dark I-V measurements [**25-26**]. Although, the most

commonly used methods are based on computing the slope near the V_{oc}, these methods are sensitive to the point considered on the characteristic curve. To compute series resistance, we have utilized the method proposed in Ref. [**24**], where the overall contribution of the series resistance is considered as an effective series resistance, R_s and is calculated by evaluating numerically the area, A under the light I-V curve of the solar cell [**24**] using:

$$R_S = 2\left[\frac{V_{oc}}{I_{sc}} - \frac{A}{I_{sc}^2} - n\frac{kT}{q}\frac{1}{I_{sc}}\right] \quad (1)$$

where *n* is the effective ideality factor of the diode and *k* is the Boltzmann constant. This method of computing the area is superior to computing the slope as this method smoothens the experimental data errors rather than enhancing the noise.

2.3.2 Current-matching in 2J InGaP/GaAs Solar Cell on Si

In our device structure, owing to the lattice-mismatch between GaAs and Si, the TDs may propagate into the active junctions and serve as recombination centers for electron and holes, leading to degradation in the minority carrier lifetimes and thus the cell performance. In our model, the maximum minority electron lifetime (τ_n) in lattice-matched p-type GaAs and p-type InGaP base were considered to be 20ns [**15, 16**] and 10ns [**20,21**], respectively. Due to the lattice-mismatch between GaAs and Si, τ_n in p-type GaAs and p-type InGaP base were estimated to be 1.49ns and 3.17ns, respectively at a TDD of $10^6\,cm^{-2}$ [**9**]. Carefully taking into account the impact of these degraded lifetimes on the cell performance, we achieved the current-matching condition between the two subcells under AM1.5d spectrum utilizing a similar method as outlined earlier [**9**]. Owing to the spectral differences between AM1.5g and AM1.5d spectra, for the same current-matched design under AM1.5g (2μm thick p-GaAs and 0.38μm thick p-InGaP base), the J_{sc} in the GaAs subcell was found to be 7.66% higher than the top InGaP subcell under AM1.5d spectrum.

Our preliminary 2J InGaP/GaAs cell structure on Si employed a grid finger-pitch of 500μm. In order to maximize the J_{sc} of our 2J InGaP/GaAs cell and to achieve the current-matching condition under AM1.5d at a TDD of $10^6\,cm^{-2}$, the thicknesses of individual layers in both the subcells were optimized as shown in the **Fig. 11(a)**. The optimal p-GaAs base thickness was found to be 2.7μm, beyond which the minority carriers could not be efficiently collected as a consequence of the reduced electron lifetime owing to the dislocations in the p-GaAs base. The optimal thicknesses for the p-InGaP base was found to be 0.47μm, which allowed to extract the maximum current density from the bottom current-limiting GaAs subcell, while still maintaining the current-matching condition. This current-matched 2J InGaP/GaAs cell design

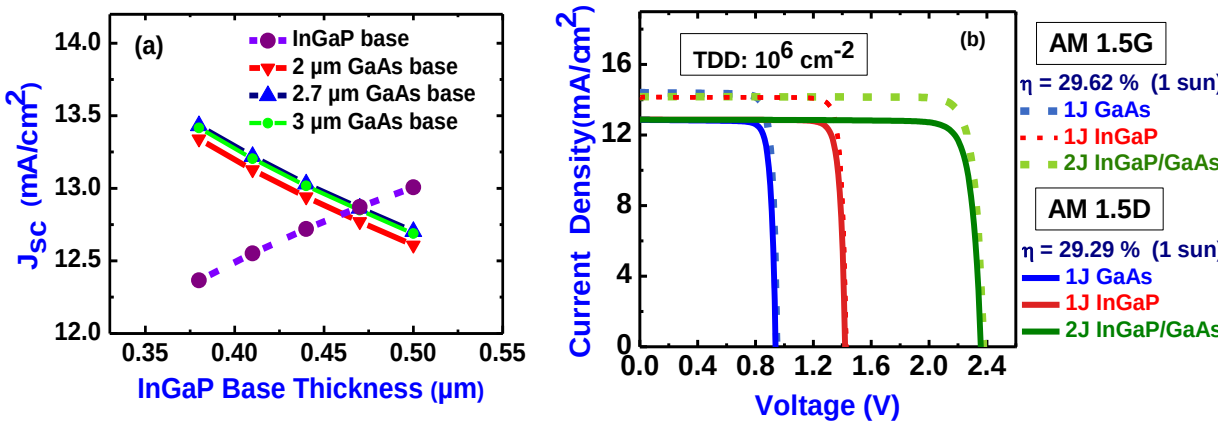

Fig. 11 (a) Short-circuit current density as function of variation in the base thickness of the InGaP subcell to realize current-matching at a TDD of 10^6 cm^{-2} under AM1.5d, (b) Current-matched J-V characteristic of 2J InGaP/GaAs solar cell on Si under AM1.5g (dashed curves) and AM1.5d (solid curves) spectrum [**32**]. Used with permission from IEEE, 2014.

on Si exhibited an efficiency of 29.29% under AM1.5d (1-sun) with a J_{sc} of 12.86 mA/cm^2 as indicated by the solid curves in **Fig. 11(b)**. The contribution of individual GaAs and InGaP subcells towards the 29.29% efficiency were 11.44% and 17.85%, respectively and the V_{oc} of the GaAs and InGaP subcells were 0.94V and 1.42V, respectively. The corresponding band gap-voltage offset, W_{oc} (=E_g/q-V_{oc}) for the GaAs and InGaP subcells were calculated to be 0.48V and 0.44V, respectively. These values of W_{oc} higher than the ideal W_{oc} value of ~0.4V [10] were indicative of the dominance of non-radiative recombination in the base of both the subcells owing to the TDs. A comparative assessment of 2J InGaP/GaAs on Si solar cell performance with varying TDD under AM1.5g and AM1.5d is presented in **Table IV**. The incident power density used was 1000 W/m^2 and 900 W/m^2 for AM1.5g and AM1.5d spectrum, respectively. Each efficiency data point represents a current-matched condition.

TABLE IV

Impact of TDD on the performance of 2J InGaP/GaAs solar cell on Si – AM1.5g vs. AM1.5d

TDD (cm^{-2})	1-sun AM 1.5g Efficiency (%)	1-sun AM 1.5d Efficiency (%)
No TDD	33.26	32.75
10^6	29.29	29.29
10^7	26.05	25.88

2.3.3 Optimization of Spacing between Grid Fingers

The performance of III-V solar cells for CPV operation can be significantly impacted if the front grid design is not optimized for a specific target concentration. Lowering the grid separation between the front gridlines (or increasing the grid shadowing) improves the I^2R resistive losses, but at the same time reduces the photon flux that reaches the cell and in turn limits the J_{sc}. Thus, there are design trade-offs between the shadowing effect and the series resistance which needs to be optimized to enable the best performance under a specific target concentration.

In order to optimize the losses due to shadowing effect and series resistance, we varied the grid finger-pitch from 500µm to 50µm to determine the optimal spacing for a cell design at a TDD of 10^6 cm^{-2}. The influence of variation in the grid finger-pitch on the efficiency (η), V_{oc}, fill-factor (FF) (inset shows J_{sc}) and voltage at maximum power point (V_m) with increasing concentration under AM1.5d were plotted in **Fig. 12(a), 12(b), 12(c)** and **12(d)**, respectively. It can be clearly seen that our preliminary cell with a grid finger-pitch of 500µm demonstrated the best performance under 1-sun. However, with increasing sun concentration the performance began to degrade with the peak efficiency of 31.71% occurring at merely 50 suns. Due to a wider grid finger-pitch of 500µm, the effect of series resistance was more pronounced at low concentrations,

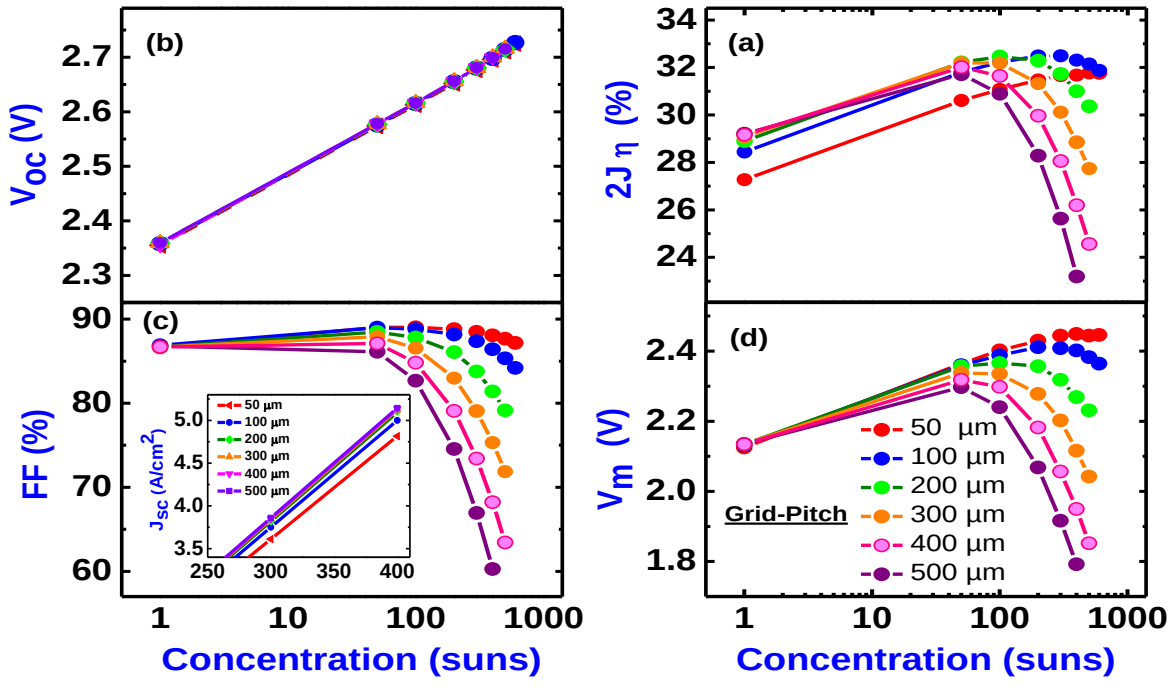

Fig. 12. Impact of concentration on the performance of 2J InGaP/GaAs cell on Si: (a) η, (b) V_{oc}, (c) FF (inset shows J_{sc}), and (d) V_m for various grid finger-pitches under AM1.5d spectrum at a TDD of 10^6 cm^{-2} [**32**]. Used with permission from IEEE, 2014.

thus limiting the peak performance to only 50 suns and rendering this cell design inefficient for CPV operation.

From **Fig. 12(a)**, one can clearly find that as the front grid spacing was reduced, the efficiency at 1-sun for the 50μm finger-pitch dropped significantly due to the lower photon flux reaching the cell as a result of increased grid shadowing. However, the advantage of reducing the front grid spacing was clearly seen at higher concentration, evident by the improvement in efficiency and the extension of peak performance to higher concentration. For the cell with a grid finger-pitch of 50μm, the low absorbed photon flux (and the corresponding low J_{sc}, as evident by the inset of **Fig. 12(c)**), overpowered the benefits gained by minimizing the I^2R resistive losses. The cell with a finger-pitch of 100μm exhibited the best performance at higher concentration (32.49% at 300 suns). The grid finger-pitch of 100μm reduced the resistive path, while allowing sufficient photon flux to reach the cell. Thus, underlining the importance of accurate grid design at an intended concentrated level. The resulting solar cell performance parameters are compared for the best grid finger-pitch of 100μm with the preliminary grid finger-pitch of 500μm in **Table V**. In addition, to get a clear insight on the dependency of cell performance on the TDD, we simulated 2J InGaP/GaAs solar cell on Si for CPV operation with TDD varying from 10^5 to 10^7 cm^{-2}, with subcells being current-matched at each respective TDD. The grid finger-pitch design at each respective TDD was optimized and the performance results obtained are summarized in **Table VI**.

From **Fig. 12(a)**, it is also worth noting that even for the optimized 100μm grid finger-pitch, the efficiency peaked at 300 suns and then eventually decreased thereafter. The solar cell performance parameters (J_{sc}, V_{oc}, J_m, V_m) were analyzed to investigate the root cause of the degradation in performance beyond 300 suns,

TABLE V

Dependence of 2J cell performance on finger-pitch at TDD ~10^6 cm^{-2}

Grid Finger-Pitch (μm)	V_{oc} (V)	J_{sc} (mA/cm^2)	FF (%)	Efficiency (%)
1-sun				
500 μm	2.356	12.86	86.87	29.29
100 μm	2.358	12.50	86.89	28.44
300-suns				
500 μm	2.681	3859.1	66.94	25.63
100 μm	2.679	3751.13	87.37	32.49

starting with J_{sc} first. It is evident from the inset of **Fig. 12(c)** that the J_{sc} continued to increase with sun concentration, irrespective of the finger-pitch and hence was not a performance limiting factor. From **Fig. 12(b)**, it can be inferred that the V_{oc} had a logarithmic dependence on the concentration. Assuming constant temperature, V_{oc} under concentrated sunlight can be expressed as [29],

$$V_{oc}^{X\,suns} = V_{oc}^{1\,sun} + n\frac{kT}{q} lnX \quad (2)$$

where *n* is the effective diode ideality factor, *k* is the Boltzman constant, *X* is the sun concentration and *q* is the elementary charge. From **Fig. 12(b)**, one can find that the V_{oc} continued to increase with the concentration and therefore was not a factor limiting the cell performance to increase beyond 300 suns. Using (2), the slope of V_{oc} vs. logarithmic of concentration was calculated to be ~ 2.21kT, close to the predicated value of 2*k*T for two series connected ideal diodes. The higher value of the ideality factor was attributed to the recombination within the base region of the subcells owing to the TDD. We utilized this ideality factor to compute the series resistance, which we discuss in the subsequent section. While J_{sc} and V_{oc} continued to increase with co ncentration, it is evident from **Fig. 12(c)** that the FF was adversely impacted, especially for the cells which had wider grid finger-pitch. The decrease in FF at higher concentration was attributed to the effect of series resistance associated with V_m. We next address in greater details the role of series resistance and the associated I^2R losses in limiting the cell performance at higher concentrations.

TABLE VI

Dependence of 2J cell efficiency on threading dislocation density [**32**]. Used with permission from IEEE, 2014.

TDD (cm^{-2})	1-sun AM 1.5d Efficiency (%)	Peak CPV Efficiency (%) (Peak Concentration) – Optimal Grid Finger-Pitch
10^5	30.73	33.84 (100x) - 200μm
10^6	29.29	32.49 (300x) - 100μm
10^7	25.88	29.12 (300x) - 100μm

2.3.4 Role of Series Resistance on the Cell Performance

Among the solar cell parameters (V_m, J_m, V_{oc}, J_{sc}) which influence the FF, we found that all of these parameters continued to increase with concentration, except V_m. Unlike V_{oc}, which increased logarithmically

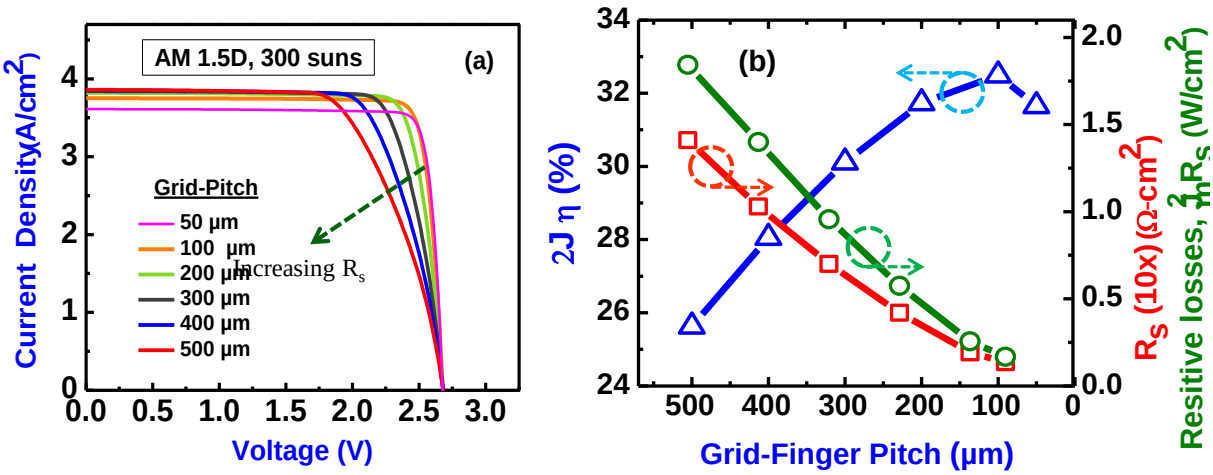

Fig. 13 (a) J-V characteristics of 2J InGaP/GaAs solar cell on Si (under AM1.5d, 300 suns) for various grid finger-pitches at a TDD of 10^6 cm^{-2}, (b) 2J cell η, R_s and $(J_m)^2R$ resistive losses as a function of grid-finger pitch at a TDD of 10^6 cm^{-2} [**32**]. Used with permission from IEEE, 2014.

with concentration; V_m had a nonlinear dependence as shown in **Fig. 12(d)**. Thus, the degradation in V_m with increasing concentration limited the cell efficiency to rise beyond a certain concentration due to the impact of both series and shunt resistance. With the increase in concentration, the degradation in V_m was found to be the less severe for narrower grid finger-pitch, as evident from **Fig. 12(d)**. This was attributed to the pronounced effect of series resistance for the widely spaced grid fingers owing to a longer resistive path for the electrons to travel before being collected in the gridlines. As a consequence of the degradation in V_m with increasing concentration, the efficiency was most severely impacted for the cell with wider grid finger-pitch, as shown in **Fig. 12(a)**. The resistive power losses increase with the square of current density, having a stronger impact at higher concentration. The enhanced effect of series resistance with increasing grid finger-pitch is illustrated in the J-V characteristics of the 2J InGaP/GaAs cell on Si at 300 suns at a TDD of 10^6 cm^{-2}, as shown in **Fig. 13(a)**. In order to gain quantitative insight into the design trade-offs for optimizing series resistance and shadowing losses at higher concentration, we evaluated the effective series resistance and the associated I^2R losses at 300 suns. The efficiency of the 2J InGaP/GaAs cell on Si at 300 suns, the R_s and the associated $(J_m)^2R_s$ losses are plotted as a function of the variation in grid finger-pitch **in Fig. 13(b)**. One can clearly see that both the R_s and $(J_m)^2R_s$ resistive losses decrease with the decrease in grid finger-pitch. This facilitated an increase in efficiency for the cells with narrower grid finger-pitch. However, this trend of increase in efficiency with decrease in grid finger-pitch was effective only until the shadowing losses began to dominate and limit the performance. This was evident in the cell with a grid finger-pitch of 50µm. Although, the $(J_m)^2R_s$ losses were minimized for grid finger-pitch of 50µm, the photon flux reaching the cell was significantly reduced due to the increased shadowing losses, thereby limiting the

cell performance. Thus, the design trade-offs between shadowing losses and series resistance for CPV operation were best optimized at a grid finger-pitch of 100μm.

2.3.5 Optimizing of the Doping in the Top Cell Window Layer

The conductivity of the top cell window-emitter layers play a significant role in extending the peak cell performance towards higher concentration, enabling more efficient design for economical CPV. In a typical n+/p solar cell, the electrons flow laterally in the top cell's window layer before they are collected at the gridlines. This lateral electron flow makes the optimization of the conductivity of the window-emitter layers

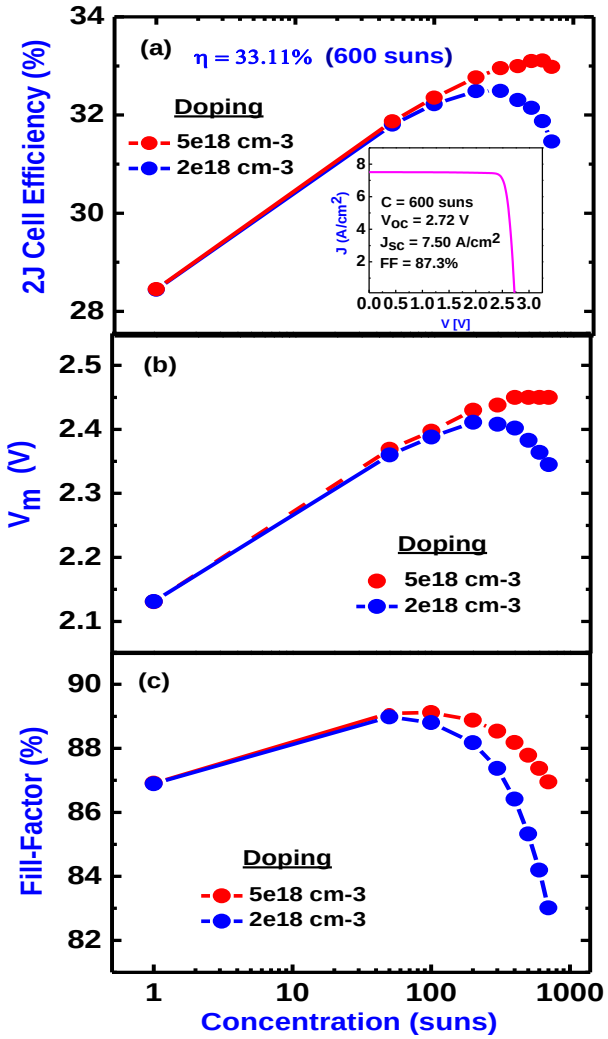

Fig. 14. Impact of doping concentration in the InAlP window layer on the performance of 2J InGaP/GaAs solar cell on Si at a TDD of 10^6 cm^{-2}: (a) η , (b) V_m, and (c) FF under AM1.5d. The inset in (a) shows the J-V characteristic of the optimized 2J InGaP/GaAs solar cell with grid finger-pitch of 100μm and window layer doping concentration of n=$5x10^{18}$ cm^{-3} at 600 suns [**32**]. Used with permission from IEEE, 2014.

TABLE VII

Dependence of 2J cell efficiency on the window layer doping [**32**]. Used with permission from IEEE, 2014.

Doping (cm^{-3})	1-sun Efficiency (%)	Peak Concentration (suns)	Peak Efficiency (%)
$2.00x10^{18}$	28.44	300	32.49
$3.50x10^{18}$	28.45	500	32.93
$5.00x10^{18}$	28.45	600	33.11
$8.00x10^{18}$	28.46	600	33.23

of key importance to minimize the I^2R resistive losses and indeed translate to substantial performance improvement.

Our optimized cell design with a grid finger-pitch of 100μm, utilized an $In_{0.5}Al_{0.5}P$ window layer with a doping concentration of $n=2x10^{18}$ cm^{-3}. In order to optimize the doping concentration in the window layer, we varied it from $n=2x10^{18}$ cm^{-3} to $n=8x10^{18}$ cm^{-3}, while keeping the grid finger-pitch fixed at 100μm and taking into account the impact of TDD. The influence of increasing sun concentration on the η, V_m, and FF for the 2J InGaP/GaAs cell on Si at two different window layer doping concentrations ($n=2x10^{18}$ cm^{-3} and $n=5x10^{18}$ cm^{-3}) is illustrated in **Fig. 14(a), 14(b) and 14(c)**, respectively and the key results are summarized in **Table VII**. It is worth noting that as the doping concentration in the window layer was increased, the peak cell efficiency continued to increase, with the best performance of 33.23% occurring at 600 suns for $n=8x10^{18}$ cm^{-3}. However, obtaining a high doping concentration of $n=8x10^{18}$ cm^{-3} in the InAlP window layer can be challenging during material growth. Therefore, we selected a more realistic and achievable doping concentration of $n=5x10^{18}$ cm^{-3}. From **Fig. 14(a)** we can see that by increasing the doping concentration from $n=2x10^{18}$ cm^{-3} to $n=5x10^{18}$ cm^{-3}, the peak performance of 32.49% at 300 suns was extended to 33.11% at 600 suns. This improvement in cell performance was attributed to the improvement in V_m and the FF (see **Fig. 14(b)** and **14(c)**) owing to the reduction in the I^2R resistive losses. Although, the gain in cell performance by increasing window layer doping concentration from $n=2x10^{18}$ cm^{-3} to $n=5x10^{18}$ cm^{-3} was only 0.62%, the shift in peak performance from 300 suns to 600 suns will allow to significantly scale down the cell size and contribute substantially towards cost reduction. The drop in cell performance beyond 600 suns was attributed to effect of series resistance, emanating from the bulk resistance of the epi-

layers. It was not due to the J_{sc} of the 2J cell exceeding the peak tunneling current density of the TJ at 600 suns since AlGaAs/GaAs based TJs have been previously demonstrated with peak tunneling current density in excess of 7.5 A/cm^2, the J_{sc} of our 2J InGaP/GaAs cell on Si at 600 suns [30], [31]. Performance prediction of ~33% for 2J InGaP/GaAs solar cells on Si is encouraging for future research and development of III-V solar cells on Si substrate for CPV application.

Summary

We have investigated the concentrated photovoltaic performance of metamorphic, monolithic InGaP/GaAs dual-junction (2J) solar cells on Si substrate under AM1.5d spectrum using finite element analysis. We have demonstrated a design methodology oriented towards maximizing the performance of 2J InGaP/GaAs solar cell on Si for concentrated photovoltaics, incorporating threading dislocations. The current-matching condition under AM1.5d was realized at TDD varying from 10^5 to 10^7 cm^{-2}, emanating from the mismatch between GaAs and Si substrate. A theoretical conversion efficiency of 29.29% at a realistic TDD of 10^6 cm^{-2} was achieved for the 2J InGaP/GaAs solar cell design on Si with a grid finger-pitch of 500 μm under 1-sun AM1.5d spectrum. The bottom GaAs subcell was found to limit the overall performance of the 2J InGaP/GaAs solar cell on Si.

The optimization of front grid spacing and sheet resistance of the window layer were the key design parameters taken into consideration for extending the peak performance towards higher concentrations. The design trade-offs between the losses due to grid shadowing and series resistance were optimized to maximize the performance under higher concentration. At a TDD of 10^6 cm^{-2}, the optimal grid finger-pitch was found to be 100 μm, demonstrating an efficiency of 32.49% at 300 suns. Increasing the window layer doping from n=2x10^{18} cm^{-3} to n=5x10^{18} cm^{-3} allowed to extend the peak performance to 600 suns, improving the conversion efficiency to 33.11%, a greater than absolute 3.5% performance improvement compared to 1-sun. We have demonstrated the importance of optimizing the cell design for a target concentration at a specific threading dislocation density. Our model predicts theoretical conversion efficiency in excess of 33% at 600 suns for 2J InGaP/GaAs solar cell on Si at a TDD of 10^6 cm^{-2}. The performance results are encouraging and show a promising future for integrating metamorphic III-V concentrator solar cells on Si substrate for CPV applications.

2.4 Triple-Junction (3J) InGaP/GaAs//Si Solar Cells for 1-sun and CPV

Attaining a lower levelized cost of energy (LCOE) is seen as one of the key success criteria for the competing solar technologies to gain a substantial share of the future global PV market. While the performance of Si based solar cells have almost saturated at an efficiency (η) of 25%, III-V compound semiconductor based solar cells have steadily shown performance improvement at approximately 1% (absolute) increase per year, with a recent record efficiency of 44.7%. Integration of such high-efficiency III-V solar cells on significantly cheaper and large area Si substrate has recently attracted immense interest to address the future LCOE roadmaps. A recently study reveals that transitioning from a 4" Ge to a 8" Si substrate would correlate to a 60% cost reduction in multijunction solar cells [**1**].

There are two key approaches for realizing multijunction solar cells: (i) by mechanical stacking and (ii) by monolithic (or heterogeneous) epitaxial growth. Several paths are being investigated to integrate III-V solar cells on Si, in which the Si substrate could be used as a passive template or as an active bottom subcell. Among the most notable approaches for integration of III-V solar cells on Si include the use of GaAsP buffer [**2-4**], SiGe buffer [**5, 6**], nitride based III-V solar cells on Si [**7, 8**], utilization of porous Si substrate for III-V solar cell integration [**1**] and wafer-bonding [**9, 10**]. The lattice-matched dual-junction InGaP/GaAs solar cell combination has been the key building block for today's high-efficiency 3J and beyond III-V solar cells. Although, ideal bottom junction material in a 3J configuration is a 1.0 eV solar cell, Si with a band-gap of 1.1eV would be a very promising candidate in addition to the larger area and significantly cheaper Si advantage. The iso-efficiency of an ideal 3J InGaP/GaAs/Si solar cell predicts a theoretical efficiency in excess of 50% under concentrated sunlight [**9**]. However, recently demonstrated 3J InGaP/GaAs/Si solar cell by direct wafer bonding approach precludes the efficient operation of such cells under CPV due to the bond interfacial layer [**9**]. The focus of this chapter is to investigate the performance of heterogeneously integrated 3J InGaP/GaAs/Si solar cells on Si substrate for CPV operation. Heterogeneous epitaxial growth approach employing a modestly doped buffer would provide a promising platform for III-V-on-Si solar cell operation for medium sun concentrations. In addition, direct epitaxial approach would enable a faster cell manufacturing process and would eliminate the probability of interfacial oxide layer formation during the wafer bonding process. We systematically investigate three key design challenges for successful heteroepitaxial integration of 3J InGaP/GaAs/Si solar cells on Si – (i) light management in the bottom Si subcell by taking into account the incident light absorption in the III-V/Si buffer layer, (ii) optimal buffer design in terms of ideal thickness and doping parameters by taking into account the impact of dislocations and (iii) performance evaluation of 3J InGaP/GaAs/Si under CPV as a function of threading dislocation density (TDD). To the best of our knowledge, this is the first study on the

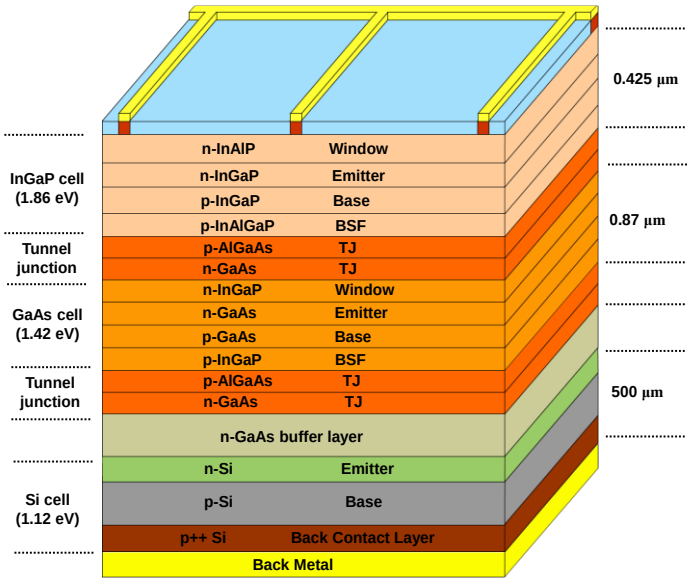

Fig. 15 Schematic depiction of tandem 3J InGaP/GaAs/Si solar cell employing Si active bottom cell [**13**]. Used with permission from IEEE, 2014.

design and performance prediction of heterogeneously integrated 3J InGaP/GaAs/Si solar cell for concentrated photovoltaic operation by taking into account the impact of dislocations in the buffer and the active III-V layers.

The numerical simulation of the proposed 3J InGaP/GaAs/Si solar cell were performed using the APSYS software. We have utilized our previously established methodology for dislocation dependent modeling of multijunction solar cells [**11, 12**]. The solar cell design and modeling was performed under AM1.5d spectrum (1000 W/m^2). The efficiency is expected to be higher if an incident power density of 900 W/m^2 is considered. A band-gap of 1.86 eV was utilized for the InGaP material. The schematic of the proposed 3J InGaP/GaAs/Si solar cell structure is shown in **Fig. 15**. A GaAs n-type buffer was selected to compliment the arsenic diffusion during the nucleation of III-V materials on the n-on-p Si solar cell. The band-diagram revealed that n-type GaAs would also act as an effective window layer for the Si subcell as it would an efficient minority hole reflector. A grid-finger width of 2µm and a grid-finger spacing of 496µm (grid-finger pitch of 500µm) was selected for the 1-sun design. To evaluate the performance under CPV operation, the grid-finger pitch was varied from 50 µm to 500 µm. An ideal anti-reflective coating design was considered. The detailed solar cell design parameters, namely, minority carrier mobility, diffusion coefficients and surface recombination velocities along with the model calibration were reported elsewhere [**11**]. The minority carrier lifetimes in the GaAs and the InGaP base at different TDDs are summarized in **Table VIII**.

TABLE VIII

Minority electron lifetime in GaAs and InGaP base with varying TDD [**13**]. Used with permission from IEEE, 2014.

TDD	Lifetime in GaAs (ns) (p=1e17cm-3)	Lifetime in InGaP (ns) (p=2e17cm-3)
No TDD	20	10
10^6	1.49	3.17
10^7	0.16	0.44

2.4.1 Buffer Architecture for III-V-on-Si Integration

One of the key challenges for designing 3J InGaP/GaAs/Si solar cell is the light management to allow sufficient photon flux to reach the bottom Si subcell. This is primarily due to the competition between the GaAs and Si subcell to absorb a shared regime of the incident solar spectrum. The direct band-gap in GaAs material allows the use of thinner active cell layers, however Si being an indirect band-gap material requires a thicker layer to maximize absorption for current-matching. In the 3J InGaP/GaAs/Si solar cell design, the indirect band-gap Si subcell was found to be the current-limiting one. Rigorous numerical iterations were performed to maximize the short-circuit current density (J_{sc}) in the Si subcell. By utilizing a heavily doped thin p-type Si layer beneath the base of the Si subcell, we were able to realize a J_{sc}=40mA/cm^2 for a stand-

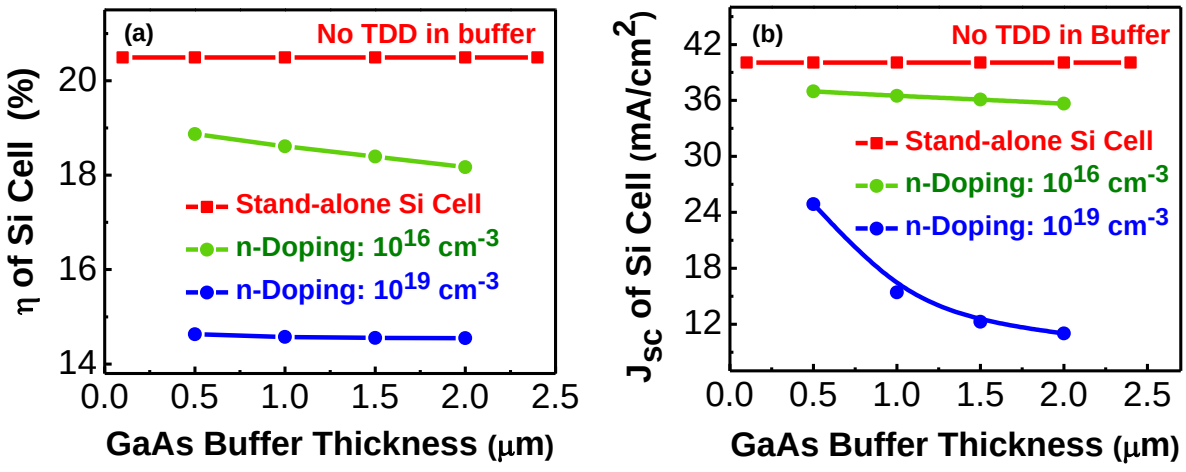

Fig. 16 Impact of GaAs buffer thickness on 1J Si solar cell [**13**]. Used with permission from IEEE, 2014.

alone Si cell. The impact of GaAs buffer layer grown above 1J Si solar cell was investigated next. The efficiency and the short-circuit current density of the Si subcell for different GaAs buffer thicknesses (see **Fig. 16(a),(b)**) and GaAs doping concentrations (see **Fig. 17(a),(b)**) were evaluated. The red line represents ideal stand-alone 1J Si solar cell efficiency. With increase in the GaAs buffer thickness, the light penetration to the bottom Si subcell was significantly hampered as evident by the decrease in J_{sc} as shown in **Fig. 16(b)**. Furthermore, for the heavily doped GaAs buffer, increasing the buffer thickness had a detrimental impact on the Si subcell performance. The decrease in J_{sc} indeed correlated to the decrease in Si cell performance (see **Fig. 16(a)**). The decrease in the J_{sc} was recognized as the key parameter degrading the Si subcell performance as the open-circuit voltage (V_{oc}) of the Si subcell reduced by less than 10% when the GaAs buffer thickness was increased from 0.5μm to 2μm. Thus, a thinner GaAs buffer would be preferable to maximize the Si subcell current response. Alternatively, materials with higher band-gap for buffer layer (such as InGaP and AlGaAs), though might be challenging to grow, would relieve some of the constraint on the buffer layer thickness for III-V-on-Si integration.

Next, we evaluated the influence of GaAs buffer doping on the Si subcell performance at a fixed GaAs buffer thickness of 0.5 μm. From **Fig. 17(a)**, it is evident that the performance of Si subcell was most severely impacted when the buffer was heavily doped. This was attributed to the band-gap narrowing in GaAs associated with the heavy doping effect. Thus, in order to maximize the light penetration to the bottom Si subcell, the n-type GaAs buffer should have doping concentration less than $n=1x10^{18}$ cm^{-3}.

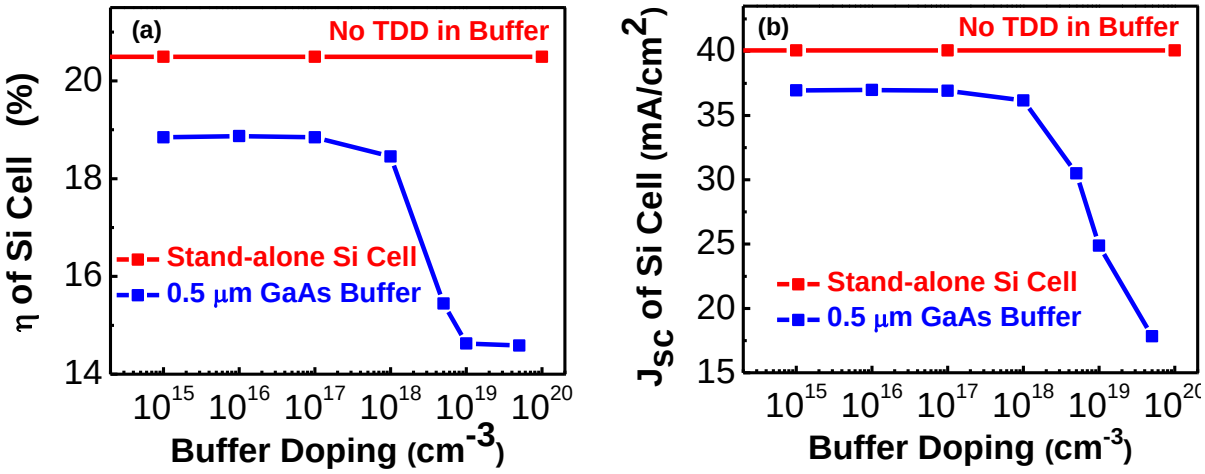

Fig. 17 Impact of GaAs buffer doping on 1J Si solar cell [**13**]. Used with permission from IEEE, 2014.

2.4.2 Impact of Dislocations in the Buffer on Cell Performance

We next investigated the impact of TDD in the GaAs buffer on the 1J Si solar cell efficiency (see **Fig. (18(a)**) and the short-circuit current density (see **Fig. 18(b)**). The TDDs in the buffer layer were varied by taking into account the degraded minority carrier lifetime in the n-GaAs buffer. From **Fig. 18(a)**, it is evident that the higher dislocation density in the GaAs buffer significantly degraded the Si subcell performance, primarily due to the poor minority hole transport across the n-type GaAs buffer. Thus, the incorporation of dislocations in the GaAs buffer makes the light management and carrier collection very challenging, demanding very careful attention to dislocation dependent current-matching in the 3J tandem cell configuration, which is addressed in the following subsection.

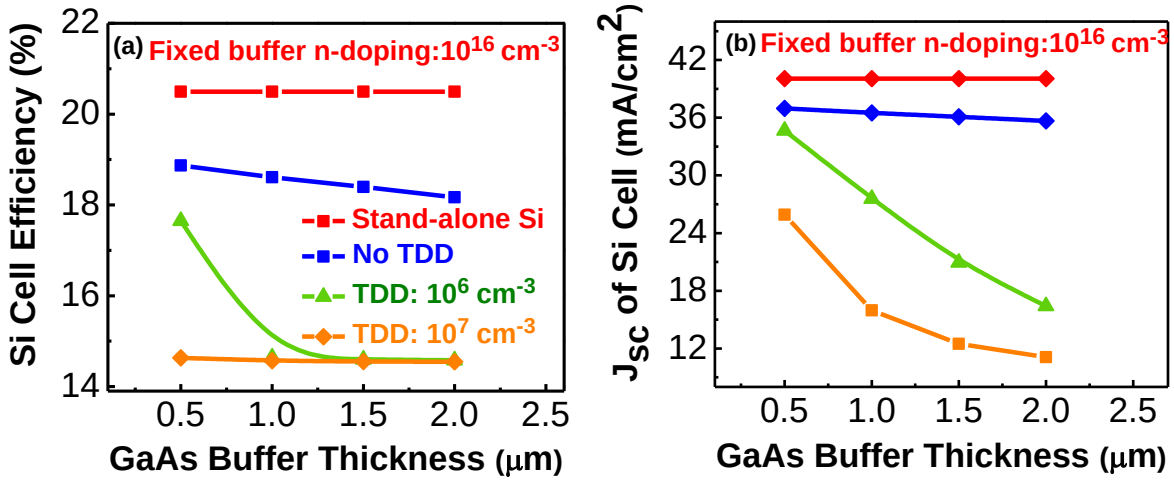

Fig. 18 Impact of dislocation in GaAs buffer on 1J Si solar cell [**13**]. Used with permission from IEEE, 2014.

2.4.3 3J 1-Sun Design

The dislocations generated at the III-V/Si interface could propagate through the buffer layer into the active III-V layers, thus rendering the task of current-matching as extremely challenging. Since, the Si bottom cell was the current-limiting one, the top InGaP and GaAs subcell thicknesses had to be significantly reduced to allow sufficient photon flux to reach the bottom cell. Interestingly, thinning the III-V active cell layers (mainly base) would imply that the minority carriers will have to travel shorter distance in the base to reach the junction, thus translating to 3J III-V solar cell designs on Si being less sensitive to TDDs. Based on our GaAs buffer design optimization, we utilized a 0.5 μm thick GaAs buffer with a doping concentration of n=5x16 cm^{-3} to evaluate the performance of 3J InGaP/GaAs/Si tandem solar cells under 1-sun and CPV conditions.

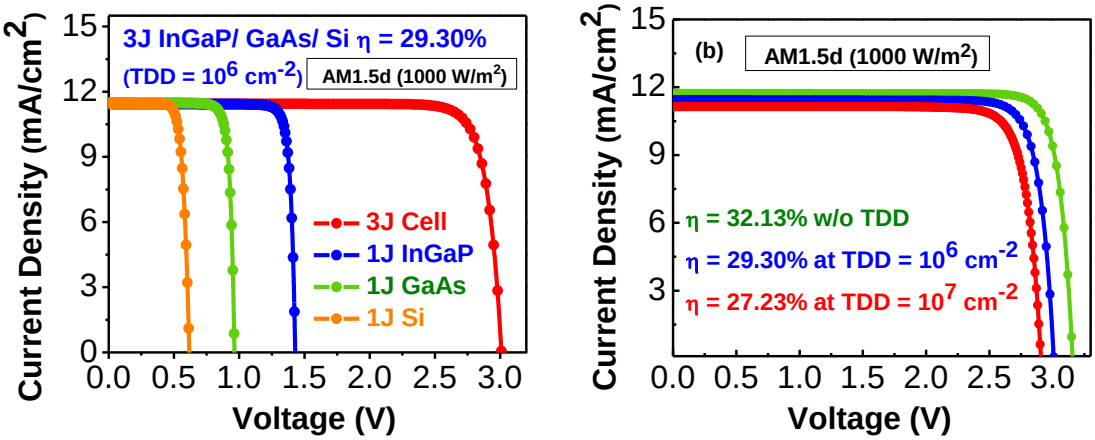

Fig. 19 (a) Current-matched J-V curve for 3J InGaP/GaAs/Si cell at TDD=1x10^6 cm^{-2} (b) J-V curves for 3J cell at different TDDs [**13**]. Used with permission from IEEE, 2014.

Fig. 19(a) shows the current-matched I-V characteristic of the 3J InGaP/GaAs/Si solar cell along with the I-V curves of the individual subcells at a realistic TDD of 10^6 cm^{-2}. The current-matched thickness of the top InGaP subcell (0.425 μm) and the middle GaAs subcell (0.87 μm) resulted in an efficiency of 29.30% (1-sun) under AM1.5d spectrum at a TDD of 10^6 cm^{-2}. The 3J design was also evaluated at a TDD of 10^7 cm^{-2} and exhibited an efficiency of 27.23% (AM1.5d) under current-matched condition, as shown in **Fig. 19(b)**. We also simulated the best-case scenario when no buffer was present between the GaAs subcell and the Si subcell and entire cell stack was assumed to be free of dislocations. The Si subcell was connected to the top two III-V subcells by a GaAs/AlGaAs tunnel junction. The ideal case 3J design exhibited an efficiency of 32.13% under AM1.5d (1-sun). The 3J design was also evaluated under AM1.5g spectrum to

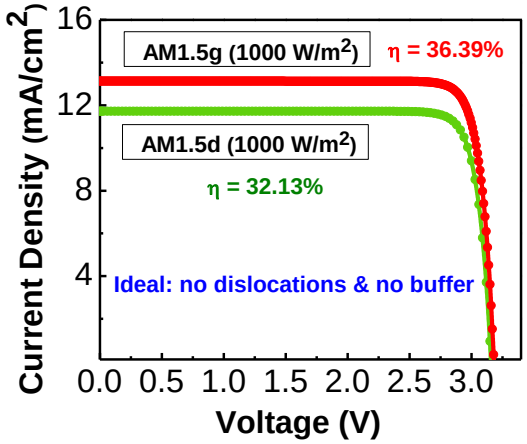

Fig. 20 Comparison of current-matched J-V characteristic of 3J InGaP/GaAs/Si solar cells under AM1.5d vs. AM1.5g spectrum for the ideal scenario when no dislocations propagate into the III-V layers. [**13**]. Used with permission from IEEE, 2014.

compare the spectral differences. The thicknesses of the individual subcells were redesigned for current-matching, yielding an efficiency of 36.39% under AM1.5g (1-sun) as shown in **Fig. 20**. **Table IX** summarizes the performance parameters for the 3J InGaP/GaAs/Si cell with TDD varied up to 10^7 cm^{-2}. It is noteworthy that even at a TDD of 10^7 cm^{-2}, careful current-matching enabled an efficiency of ~27% under 1-sun, emphasizing that such 3J III-V solar cells utilizing the Si as a bottom subcell would be feasible and provide a promising path for extending single-junction Si solar cell performance. Such direct integration schemes are also of key interest for approaches involving mechanically stacking, transfer-printing and wafer-bonding of III-V solar cells with Si solar cell.

TABLE IX

Performance dependence of 3J InGaP/GaAs/Si tandem solar cell on TDD at AM1.5d (1-sun) [**13**]. Used with permission from IEEE, 2014.

TDD	V_{oc} (V)	J_{sc} (mA/cm^2)	FF (%)	Efficiency (%)
No TDD	3.15	11.72	87.08	32.13
10^6	3.01	11.45	85.10	29.30
10^7	2.9	11.14	84.31	27.23

2.4.4 3J Concentrated Photovoltaic Design

The concentrated photovoltaic performance of the 3J InGaP/GaAs/Si solar cell at a realistic TDD density of 10^6 cm^{-2} was evaluated next. In order to mitigate the losses due to shadowing effect and series resistance, the front grid-pitch was varied from 500 μm to 50 μm to evaluate the optimal grid design for CPV. A doping concentration of $n=5x10^{18}$ cm^{-3} was utilized in the InAlP window layer to extend the peak performance towards higher sun concentration, as previously reported [**12**]. The solar cell performance parameters, namely efficiency, open-circuit voltage, fill-factor and peak voltage at maximum power point (V_m) are plotted as a function of concentration in the **Fig. 21(a), (b), (c)** and **(d)**, respectively. It can be clearly seen that with the reduction in the front grid-spacing, the 3J peak cell performance was extended to higher sun concentration. The design trade-offs between the losses due to the grid shadowing and the series resistance were best optimized at a grid-spacing of 200 μm, resulting in a conversion efficiency of 33.50% at 200 suns. Reducing the grid-spacing lower than 200 μm reduced the photon flux reaching the cell as result of

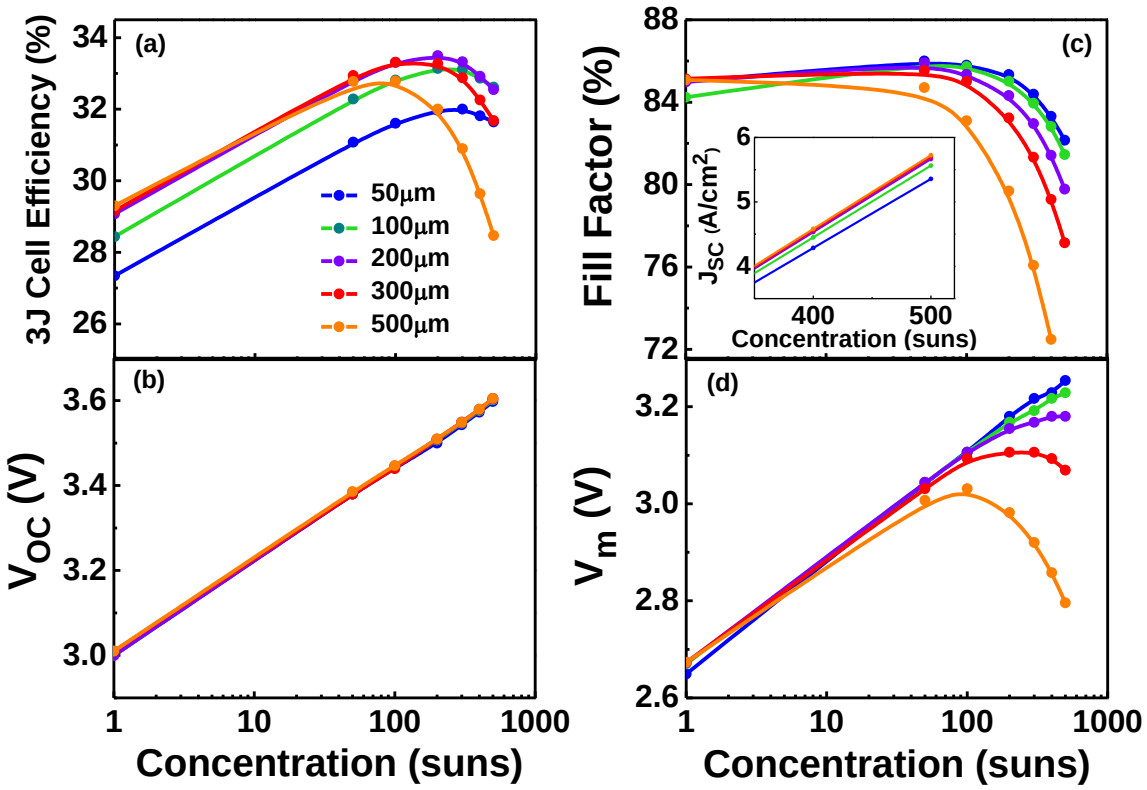

Fig. 21. CPV performance evaluation of 3J InGaP/GaAs/Si solar cell at a TDD of 1x10^6 cm^{-2}: (a) cell efficiency, (b) open-circuit voltage, (c) fill-factor (inset shows the short-circuit current-density), and (d) peak voltage at maximum power point [**13**]. Used with permission from IEEE, 2014.

increased grid-shadowing, thus overpowering the benefits gained by minimizing the resistive losses. The drop in cell performance beyond 200 suns was attributed to effect of series resistance, particularly emanating from the lightly doped and thick Si substrate. Results from our work on the heterogeneous III-V-on-Si solar cell integration employing an active bottom Si subcell will provide key design guidelines for the future optimization of 3J and beyond III-V-on-Si solar cells for 1-sun and CPV applications.

Summary

We have proposed a novel design for heterogeneous integration of 3J InGaP/GaAs/Si tandem solar cell with Si as an active subcell. We present key insight into the design of GaAs buffer architecture for the optimal down-selection of the buffer doping and thickness to maximize the photon flux penetration to the bottom Si subcell. Rigorous numerical simulations reveal the importance of a thin GaAs buffer architecture with doping concentration less than n=1x10^{18} cm^{-3} in order to allow maximum light penetration to the bottom current-limiting Si subcell. Current-matched 1-sun 3J cell efficiency of 32.13% and 36.39% was realized when no buffer layer was present between the III-V and Si subcell under AM1.5d and AM1.5g

spectra, respectively. When a 0.5 μm thick GaAs buffer layer was employed, the 1-sun efficiency (AM1.5d) dropped to 29.30% at a TDD of 10^6 cm^{-2} and to 27.23% at a TDD of 10^7 cm^{-2}. Efficiency in excess 27.23% at a TDD of 10^7 cm^{-2} suggests good tolerance of dislocations in our designed structure primarily due to reduced thickness of the III-V solar cell layer needed for current-matching. Finally, a novel 3J InGaP/GaAs/Si solar cell design at a TDD of 10^6 cm^{-2} is presented with theoretical efficiency in excess of 33% at 200 suns, suggesting a promising future for integrating III-V solar cells on Si substrate for concentrated photovoltaics.

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Chapter 3

Epitaxy & Material Characterization of III-V-on-Si Solar Cell Structures

This chapter presents the epitaxial growth of III-V compound semiconductors on Si substrate using molecular beam epitaxy (MBE). Epitaxy fundamentals and different growth modes are discussed. Next, we discuss the growth sequence for thin direct GaAs (< 2 µm) buffers on Si and the subsequent III-V solar cell growth on Si substrate. The key knobs (such as temperature, flux and V/III ratio) influencing the initial GaAs buffer growth are investigated. We also discuss the structural properties of 1J GaAs-on-Si solar cell structures realized by utilizing an intermediate GaAsSb single-strained layer. Material characterization results for evaluating the structural properties of III-V-on-Si solar cell structures are discussed involving a combination of techniques including - (i) in-situ reflection high-energy electron diffraction (RHEED), (ii) X-ray diffraction (XRD) to investigate compositions and strain relaxation properties, (iii) transmission electron microscopy (TEM) to understand defects and dislocation propagation and gauge into the crystalline quality and (iv) atomic force microscopy (AFM) to characterize the surface morphology.

3.1 Epitaxy Fundamentals and Growth Modes

Thermodynamically, growth regimes could typically be classified into mass transport limited regime or surface reaction rate limited regime depending on the growth (or deposition) temperature. Most common

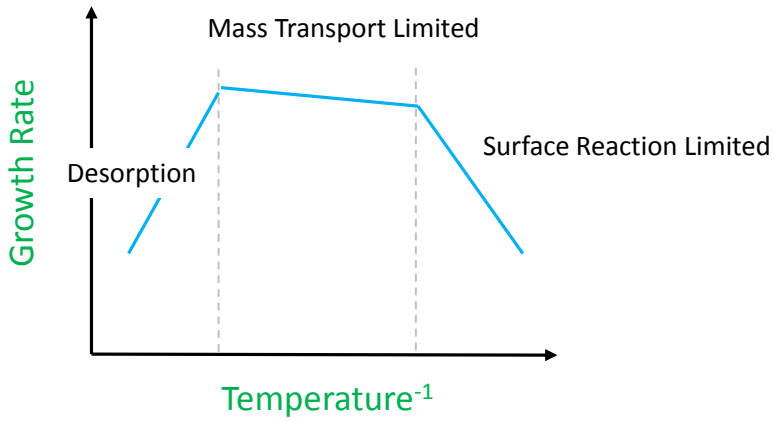

Fig. 1 Arrhenius plot for growth rate versus inverse temperature.

III-V epitaxy processes (MBE and MOCVD) fall under the mass transport regime, where the growth rate becomes almost independent of the growth temperature, providing a broader process window. The Arrhenius plot for growth rate versus temperature is shown in **Fig. 1**. Commonly used atomic layer deposition (ALD) technique for oxide depositions falls under the surface reaction limited regime, where the growth rate could be a strong function of the deposition temperature. While MBE and ALD techniques are non-equilibrium processes, MOCVD is a near-equilibrium process. The MBE growth process is a sublimation process and the growth rate is governed by the group-III element flux. In MOCVD, the growth rate has strong dependence on the group-III metalorganic cracking temperature. Much higher growth rates are achieved in MOCVD growth process in comparison to MBE. Hydride vapor phase epitaxy (HVPE) is another III-V growth technique in which extremely high growth rates (higher than MOCVD) could be achieved under almost atmospheric pressure. However, the low growth rate in MBE could be advantageous to have precise interface switching control, as in the case of quantum-wells and super-lattice structures. In comparison to MOCVD, MBE is an expensive growth technique primarily due to the ultra-high vacuum (UHV) requirements, expensive high purity precursors and due to the liquid nitrogen flow essential to keep the chamber walls extremely cold to prevent spurious fluxes of atomic and molecular species from the reactor walls.

During growth by MBE technique, a molecular beam of atoms or molecules is thermally evaporated from a solid or a liquid elemental source. The UHV deposition chamber ensures sufficient mean free path of the effused species, thus preventing their collision between the beam and the background vapor in the reactor. The growth duration and shutter sequencing allows to control the thickness and composition of respective layers. The substrate heaters allows for continuous substrate rotation to ensure growth uniformity. The substrate heater is equipped with an ion gauge on its opposite side and allows to measure and calibrated the beam-equivalent pressure (BEP) from individual sources [**1**]. Typically, most of the research MBE tools are equipped with an in-situ surface monitoring system - reflection high-energy electron diffraction (RHEED). Electron beams almost parallel to the growth surface are reflected on a phosphorous coated screening forming a surface reconstruction in the reciprocal space. Such RHEED patterns could be very valuable in providing information about the surface crystallography during oxide-desorption and to monitor the epitaxial growth process. A spotty RHEED pattern likely reflects non-smooth and island like growth, while a streaky RHEED pattern with long lines typically reflects smooth 2D layer-by-layer growth. RHEED tool is also very instrumental in precise determination of growth rates requiring on-axis substrates. The RHEED intensity oscillation frequency has a relation with the epitaxial monolayer thickness that allows to generate a linear relation between the growth rate and beam equivalent pressure.

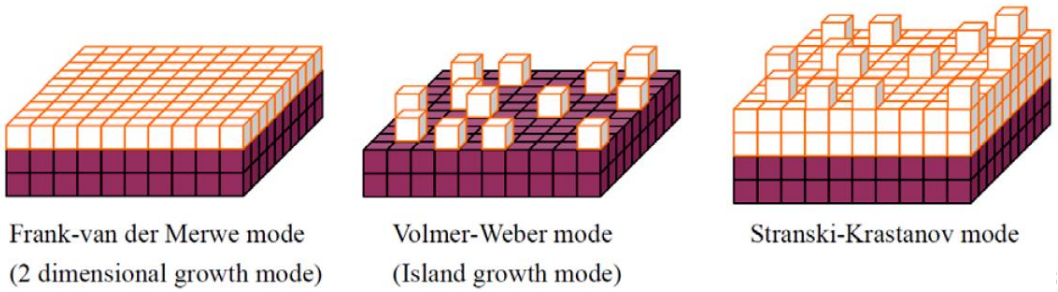

Fig. 2 Comparison between three thermodynamic growth modes [**3**]. Used under fair use, 2015.

Three mostly commonly observed thermodynamic epitaxial growth modes are discussed in the next section [**2, 3**]:

1. **Layer-by-layer Growth (Frank-van der Merwe)**

The film atoms are more strongly bound to the substrate than to each other, resulting in formation of 2D layer-by-layer growth. The adatom cohesive forces are weaker than the surface adhesive forces. Generally the crystalline quality is the highest for this growth mode. As the growth proceeds, the surface energy of the growing layer reduces, resulting in complete wetting of the surface and forming smooth layers.

2. **Island Growth (Volmer-Weber)**

The film atoms are more strongly bound to each other than to the substrate, resulting in formation of 3D islands. The adatom cohesive forces are stronger than the surface adhesive forces. As the growth proceeds, the surface energy of the growing layer and the interface increases, resulting in layer 3D balling-up on the substrate.

3. **Mixed Growth (Stranski-Krastanov)**

The growth initiates with layer-by-layer growth, but then forms 3D islands beyond crossing the critical thickness threshold. The initial first layers are able to wet the surface, but the subsequent layers are not able to. As the growth proceeds, the strain in the growing film, typically due misfit strain favors 3D growth. **Fig. 2** shows the comparison between the three thermodynamic growth modes.

3.2 III-V Buffers and Solar Cell Structures Directly Grown on Si

3.2.1 MBE Growth

All the epitaxial structures discussed in this dissertation were grown by molecular beam epitaxy. The Veeco Gen-II molecular beam epitaxy cluster tool with III-V and Ge MBE chambers connected via ultra-high vacuum transfer chamber with the ADSEL group is shown in **Fig. 3**. The group V element source equipped includes P (500 cc), As (500 cc), Sb (200 cc) with all three being valve crackers cell Mark V generation. Group three elemental sources included In, Ga and Al. The Ga cell used was a sumo cell. For the aluminum cell, unlike most of the other cells, the tip temperature was kept colder than the base.

The growth for "GaAs-on-Si" samples were performed on 3-inch diameter Si (100) substrates with a 4˚ off-cut towards <110> and on Si (100) substrates with a 6˚ off-cut towards <110>. The 4˚ off-cut Si wafers were boron-doped (resistivity- 1-5 ohm-cm) and the 6˚ off-cut Si wafers were arsenic-doped (resistivity- > 0.004 ohm-cm). Unless otherwise mentioned, the Si substrate referred in the entire dissertation is 4˚ off-cut. **Fig. 4** shows the current best three approaches for the highest heteroepitaxial 1J GaAs-on-Si solar cells utilizing a thick (7 µm) GaAs buffer (left), thick ~10 µm SiGe buffer (middle) and utilizing multiple super-lattice periods [**4, 5, 6**]. However, such thick buffers are very time consuming to grow, they typically require growth interruption for chemical mechanical polishing step to smoothen out the surface (in case of SiGe buffer), add significantly to the bill of materials, elevate the issue of thermal mismatch and furthermore eliminates the scope of leveraging the Si substrate as an active subcell due to significant absorption in the buffer. On the other, the strained-layer super-lattice structures are very complex to grow, requiring precise interface switching and composition control, making the approach not so attractive in terms of scalability.

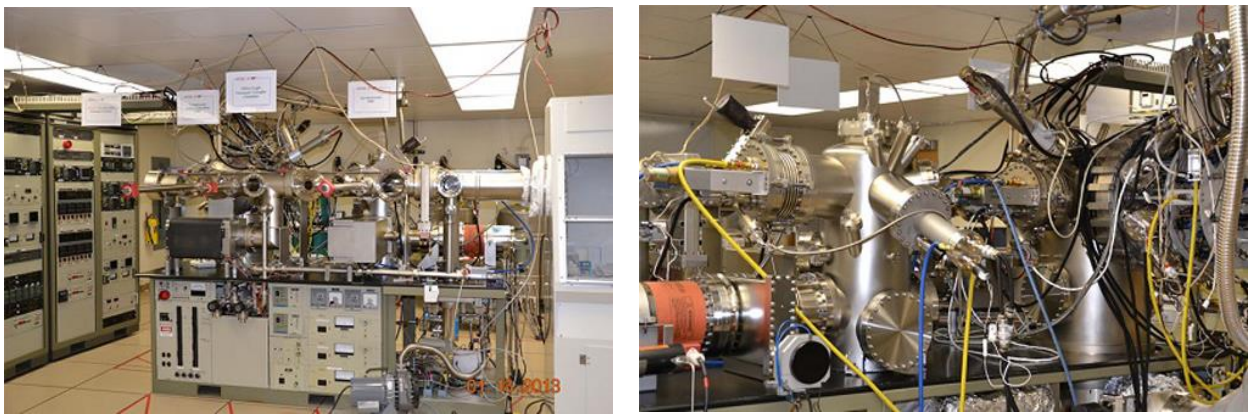

Fig. 3 Front and back view of Veeco Gen-II molecular beam epitaxy cluster tool with III-V and Ge MBE chambers connected via ultra-high vacuum transfer chamber (ADSEL Group, Virginia Tech).

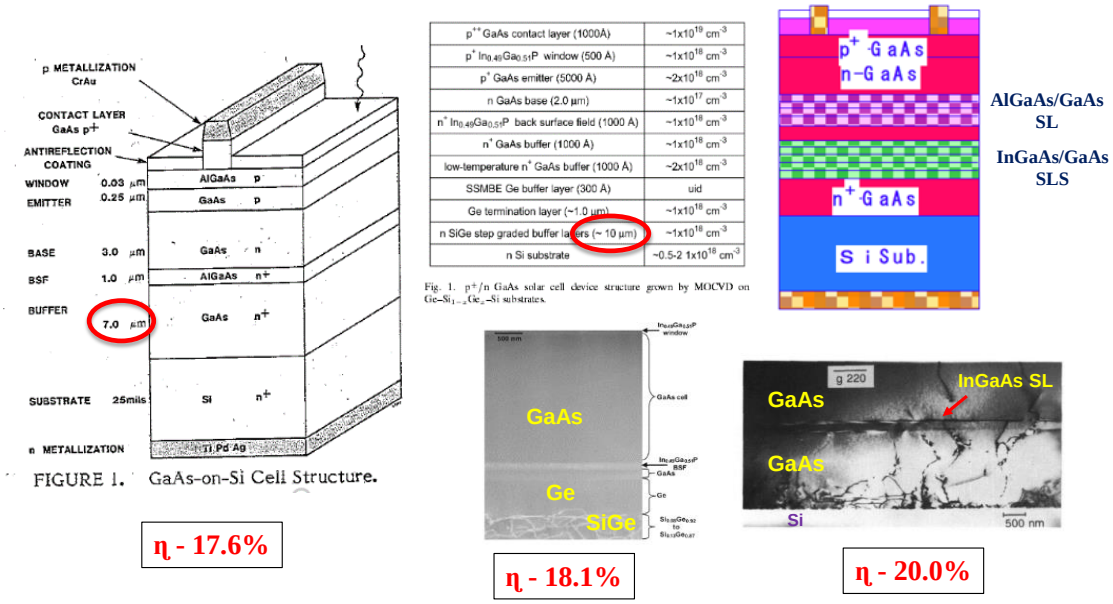

Fig. 4 Current best three approaches for highest 1J GaAs-on-Si solar cells utilizing a thick GaAs buffer (left), thick SiGe buffer (middle) and utilizing multiple super-lattice periods [**4,5,6**]. [**4**] Used with permission from IEEE, 1988; [**5**] used with permission from IEEE, 2005; [**6**] used with permission from MRS, 1988.

Thus, our approach is to utilize a GaAs buffer connecting the Si substrate and the active III-V solar cell with target thickness of ≤ 2 μm to achieve thin and low-cost buffer platforms for subsequent III-V solar cell growth which are easily scalable.

The direct GaAs epitaxial growth on Si substrate is initiated by a low-temperature, low-flux growth process followed by subsequent high-temperature and high-flux growth involving periodic high-temperature annealing schemes. The motivation for the initial low-temperature growth is to introduce misfit dislocations into a continuous psuedomoprhic film such that a continuous layer is created before structural defects are introduced allowing more area for defects to annihilate and glide. If an initial high-temperature GaAs growth is employed, the dislocations are introduced before the islands coalesce and propagate as the growth proceeds, as shown in **Fig. 5**. The two-step GaAs-on-Si growth was optimized with two key goals: (1) minimizing the dislocation density and (2) maintaining the thin buffer thickness to be less than 2 μm. All the temperatures for MBE related growth mentioned in this dissertation are thermocouple temperatures. The Si substrate was outgassed at 950˚C for oxide desorption under the absence of arsenic over pressure. The Si substrate was lowered to temperatures below 450˚C (thermocouple temperature) for the initial low-temperature and low growth rate GaAs growth. **Fig. 6** shows the growth sequence for growing 2 μm GaAs directly on Si using a series of 5 cycles of thermal annealing. During each high-temperature anneal cycle,

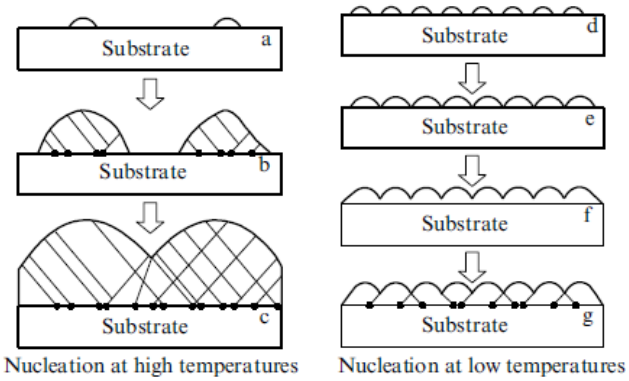

Fig. 5 The motivation for growing initial GaAs layer at low temperature. Left: dislocations and other structural defects are introduced before the islands coalesce. Right: MDs are introduced into a continuous pseudomorphic film [**22**]. Used under fair use, 2015.

the gallium cell temperature was lowered to minimize the coating on the shutter. After growing the 2 µm thick GaAs buffer on Si substrate, the 1J GaAs solar cell structure was grown next at 575˚C. A control 1J GaAs solar cell structure was also grown on GaAs substrate at a growth temperature of 650˚C. After the 2 µm GaAs buffer, a 1 µm thick, heavily p-doped (using Beryllium) lateral conduction layer was grown to serve as a high conductivity layer to realize bottom contact. Thereafter, the standard n-on-p configuration 1J GaAs solar cell structure was grown as shown in **Fig. 7** comprising of the $Al_{0.2}Ga_{0.8}As$ back surface reflector (BSF), GaAs base, GaAs emitter, $Al_{0.7}Ga_{0.3}As$ window layer and finally heavily doped GaAs cap layer. The entire solar cell structure was grown at a fixed GaAs growth rate of 0.5 µm/hr, except for the window and the cap layer that was grown a slower GaAs growth rate. A slower Ga growth rate for the AlGaAs window layer was chosen to restrict very high operating temperature of aluminum cell. A slow

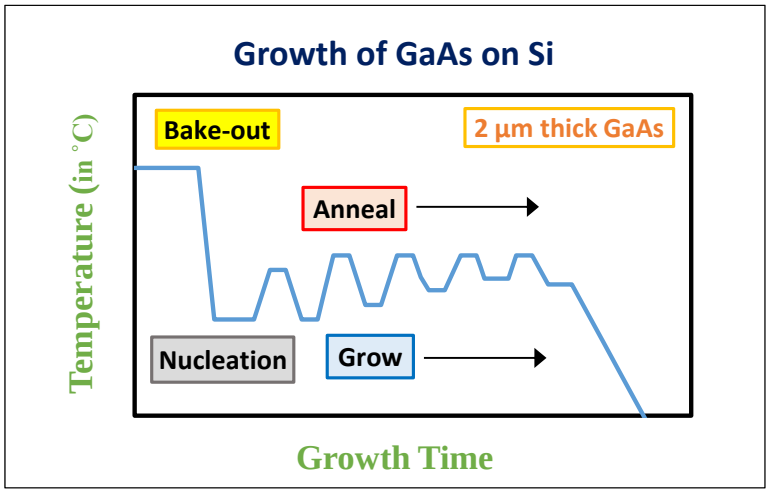

Fig. 6 Growth scheme for growing 2 µm GaAs directly on Si using multiple cycles of thermal annealing.

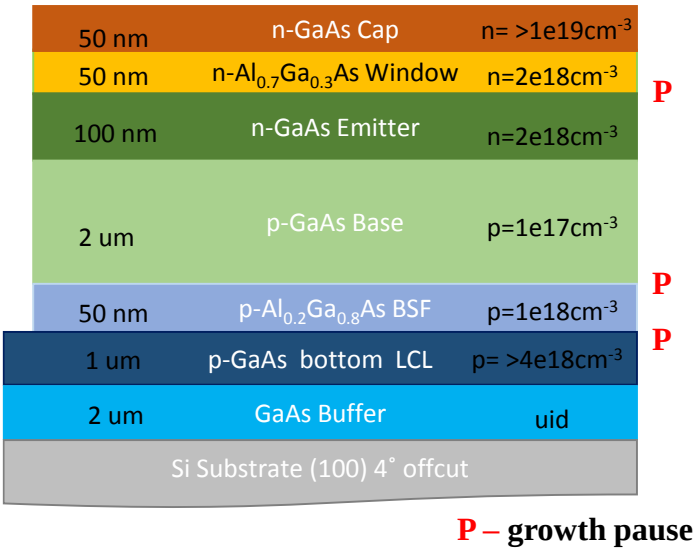

Fig. 7 Schematic of 1J GaAs solar cell structure grown directly on Si substrate using MBE.

growth rate for growing GaAs cap layer was chosen to be able to maximize Si dopant incorporation in the GaAs cap layer for minimizing the contact resistance.

Next, we discuss the material characterization techniques utilized to evaluate the quality of the GaAs solar cell structure grown on Si substrate.

3.2.2 Structural & Material Characterization

Comprehensive material characterization studies were performed to evaluate the quality of direct epitaxial GaAs and the GaAs solar cell structure grown on Si substrate in terms of crystalline quality, residual strain due to thermal mismatch, surface roughness and dislocations and defects formation. We performed material characterization spanning a series of experiments including X-ray diffraction (XRD), transmission electron microscope (TEM), atomic force microscope (AFM) and in-situ reflection high energy electron diffraction (RHEED) monitoring during epitaxial growth.

Following set of characterization tools for employed to evaluate the structural and material quality:

1) STAIB Instruments RHEED system for analyzing surface reconstruction and growth rate.
2) JOEL 2100 TEM for defects and dislocation analysis
3) PANalytical X-Pert Pro system for determining compositions and strain relaxation properties
4) Bruker Dimension Icon AFM system for surface morphology

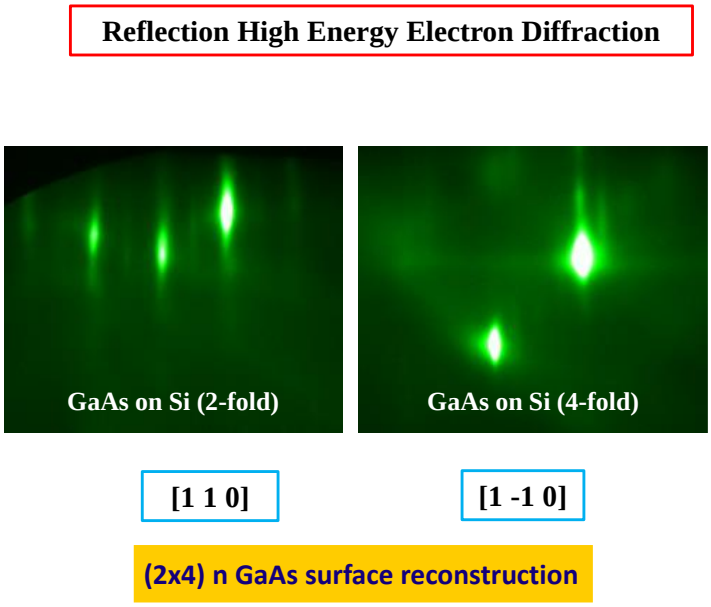

Fig. 8 RHEED patterns from the surface of (100) GaAs substrate exhibiting a streaky (2x4) surface reconstruction.

The surface reconstruction of GaAs grown on Si substrate was investigated using in-situ RHEED analysis. **Fig. 8** shows the RHEED patterns from the surface of (100) GaAs substrate for the in-plane [110] and [1-10] azimuths. The sharp and a streaky (2x4) surface reconstruction indicate a high quality for epitaxial GaAs structure directly grown on Si substrate.

Next, to investigate the dislocation propagation mechanism and the extent of dislocation propagation in the GaAs structures directly grown on Si substrate, we performed high-resolution TEM analysis. The electron transparent foils of thin film cross-sections were prepared by using standard polishing sequence involving mechanical grinding, followed by dimpling and temperature Ar ion beam milling. **Fig. 9** shows the cross-sectional TEM micrographs of (a) 1J GaAs solar cell grown on (100)Si substrate with 4˚ off-cut towards (110), (b) GaAs/Si (100) interface, (c) high-resolution (HR) TEM of GaAs/Si interface, (d) GaAs emitter/base layer with window & BSF, (e) HRTEM of AlGaAs window and the adjacent interfaces. The blue arrows indicate the growth direction. The corresponding high-resolution TEM micrograph in **Fig. 9 (b)** and **Fig. 9 (c)** reveal good crystal quality for direct epitaxial GaAs grown on Si. It can be clearly seen that a few dislocations propagate into the active cell area as seen in **Fig. 9 (d)**, while the majority have been confined with the initial 1 µm of the buffer. Almost negligible threading dislocations were observed to propagate and reach the top part of the cell (emitter, window and cap layer), suggesting the electrical

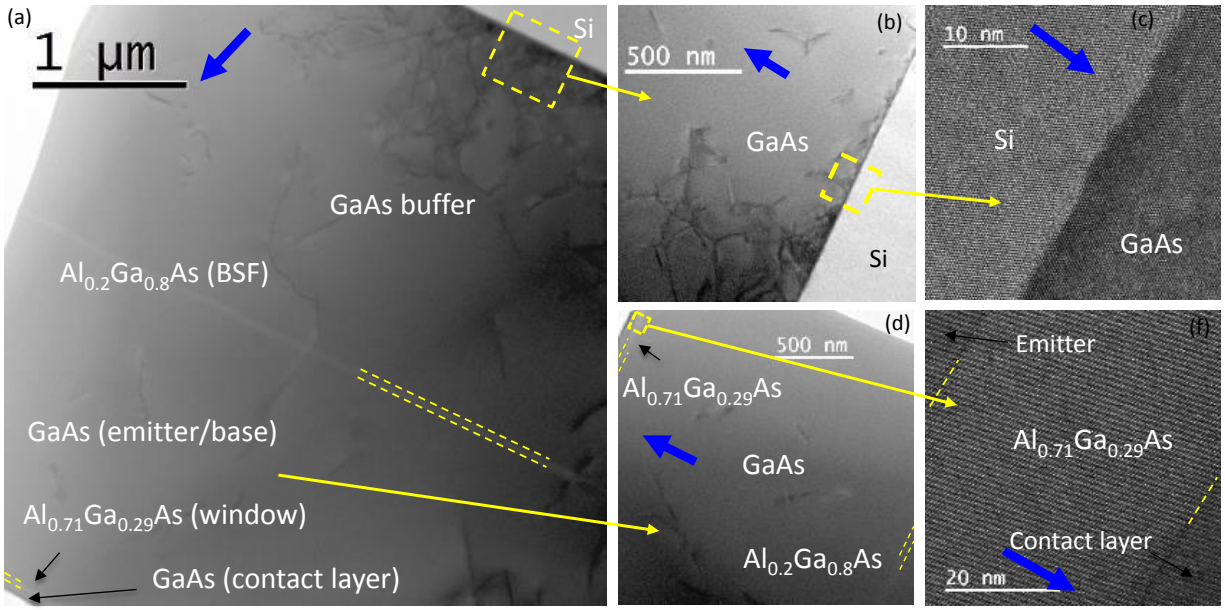

Fig. 9 XTEM micrographs of (a) 1J GaAs-on-Si solar cell, (b) GaAs/Si (100) interface, (c) HRTEM of GaAs/Si interface, (d) GaAs emitter/base layer with window & BSF, (e) HRTEM of AlGaAs window and the adjacent interfaces. The blue arrows indicate the growth direction.

performance of the solar cell should be comparatively less impacted by photon absorption in the emitter layer.

To quantitatively investigate the crystalline quality and strain relaxation properties of our GaAs on Si epi structure, we performed XRD analysis using Cu Kα-1 line-focused X-ray source. **Fig. 10** shows the ω/2θ XRD scan (004) for GaAs solar cell structure directly grown on Si utilizing a 2 µm GaAs buffer. The Si (004) ω peak position was noted to have a full with at half-maximum (FWHM) value of ~21 arcsec, while that corresponding FWHM value for the entire GaAs solar structure including the buffer layer and the lateral conduction layer (~ 5 µm) was ~36 arcsec, which is representative of excellent crystal quality, considering the 4% lattice-mismatch. Clearly, the good structural quality observed in the TEM micrographs is in accordance with the XRD analysis. The symmetric (004) and asymmetric (115) reciprocal space maps (RSMs) of GaAs solar cell structure directly grown on Si utilizing a 2 µm GaAs buffer are shown in **Fig. 11 (a)** and **Fig. 11 (b)**, respectively. It can be clearly seen from the symmetric (004) scan that the GaAs epitaxial film exhibited no observable lattice tilt and the film was almost fully relaxed with respect to the Si substrate, as seen from the asymmetric (115) RSM analysis.

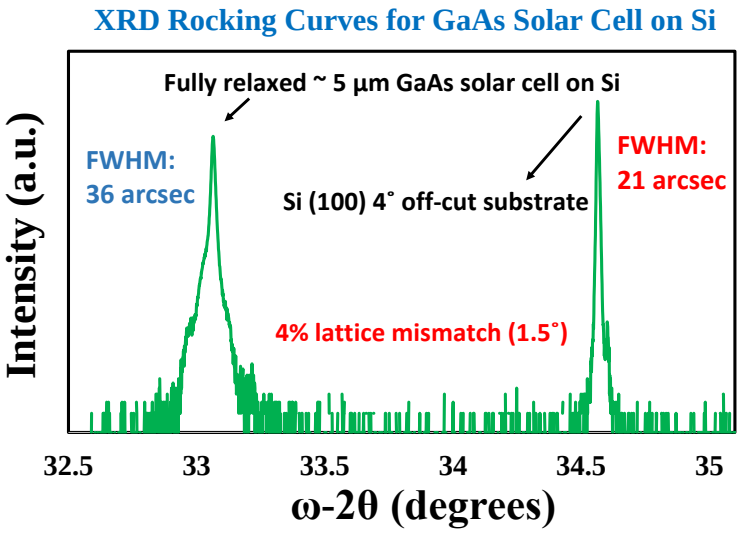

Fig. 10 ω/2θ XRD scan (004) for GaAs solar cell structure directly grown on Si utilizing a 2 µm thick GaAs buffer.

The characterization of surface morphology is important metric to evaluate the surface quality of metamorphic structures and analyze pin-holes and other surface defects. The surface morphology and roughness was investigated using atomic force microscope (AFM) in Scan Asyst Mode on Bruker

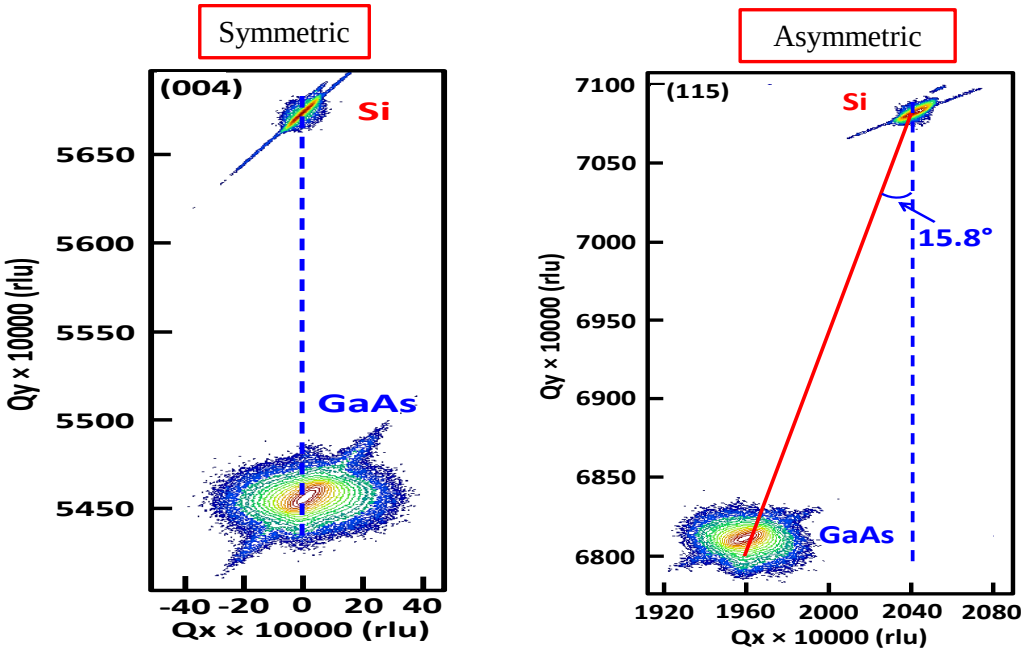

Fig. 11 a) Symmetric (004) and **(b)** asymmetric (115) RSMs of GaAs solar cell structure directly grown on Si utilizing a 2 µm GaAs buffer. The GaAs epitaxial film exhibited no observable lattice tilt and the film was almost fully relaxed.

Dimension Icon AFM system. Excellent surface morphology was achieved on lattice-matched GaAs solar cell structures grown on GaAs substrate with an RMS roughness of 0.32 nm for a 20 µm x 20 µm scan area, as shown in **Fig 12 (a)**. Furthermore, it was confirmed that the AlGaAs window layer with high aluminum content (70-75%) did not degrade the surface roughness on lattice-matched structures. The corresponding RMS roughness on our 2 µm thick GaAs buffers directly grown on Si substrate was ~ 1.76 nm for 20 µm x 20 µm scan area, as shown in **Fig. 12 (b)**. The quality of our GaAs-on-Si epitaxial films have greatly improved since starting the first few GaAs-on-Si runs. Key knobs which contributed to improving the quality of direct GaAs-on-Si growth included: (1) in-house developed modified RCA cleaning process of Si substrate in SC-1, SC-2 solution followed by oxide-strip in BOE, (ii) Si substrate oxide desorption in the absence of arsenic at temperatures ~ 950˚C thermocouple temperature, (iii) initial cold GaAs (< 450˚C) nucleation on Si substrate under low gallium flux and (iv) thermal anneal cycle to allow dislocation

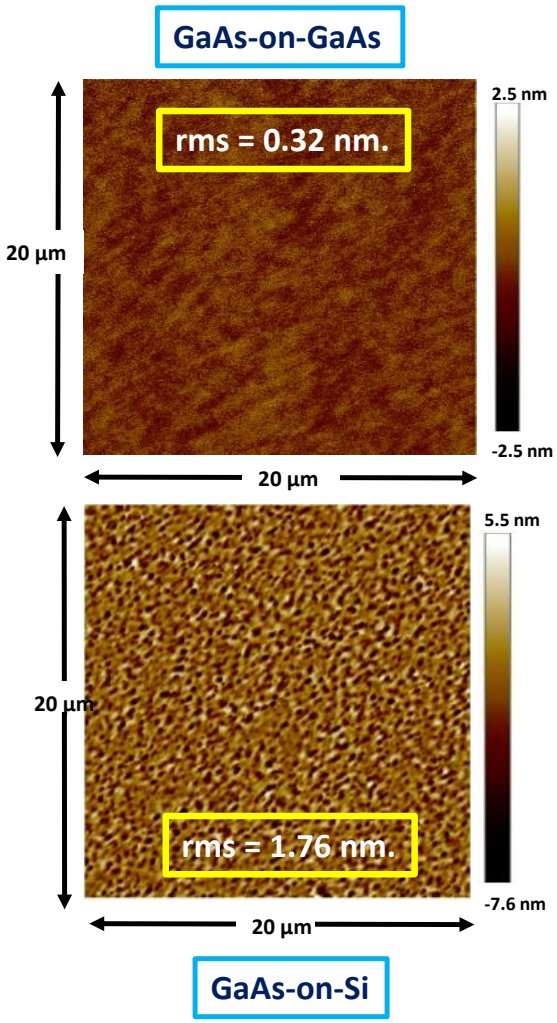

Fig. 12 AFM micrographs of (top) - the surface GaAs solar cell structure grown on GaAs substrate and (bottom) – surface of 2 µm thick GaAs buffer directly grown on Si substrate.

Fig. 13 Optical image showing epitaxial quality of GaAs grown directly on Si substrate by MBE. Left - initial direct GaAs-on-Si runs prior optimization, Right – surface quality of current optimized process-of-record (right) utilizing a sequence of LT/HT growth.

annihilation. **Fig 13** shows the optical image showing epitaxial quality of GaAs buffers grown directly on Si substrate by MBE. The image on the left shows the surface quality of our initial direct GaAs-on-Si runs prior optimization and the image on the right shows the surface quality of our current optimized process-of-record.

3.3 III-V Buffers and Solar Cell Structures Grown on Si with an Intermediate Single Strained-Layer

Utilization of multiple strained-layer super-lattice (SLS) structures has been shown to be an effective method for dislocation reduction in GaAs epitaxial layers grown on Si [**8-14**] *Yamaguchi et. al.* utilized $In_{0.1}Ga_{0.9}As$/GaAs SLS in combination with thermal cycle annealing to significantly minimize the TDD to ~ 1-2x10^6 cm^{-2} for GaAs layers grown on (100) Si substrate [**8**]. Researchers have also investigated dislocation reduction mechanism by utilizing SLS comprising of InGaAs/GaAsP multiple periods [**11**]. However, the precise ternary composition control, precursor switching sequence, especially during the growth of mixed-cation and mixed-anion super-lattice structures such InGaAs/GaAsP and multiple periods required for such structures renders this approach less attractive from scalability and reproducibility stand-point. Utilizing single strained-layer such as InGaAs has shown to be an effective technique to achieve

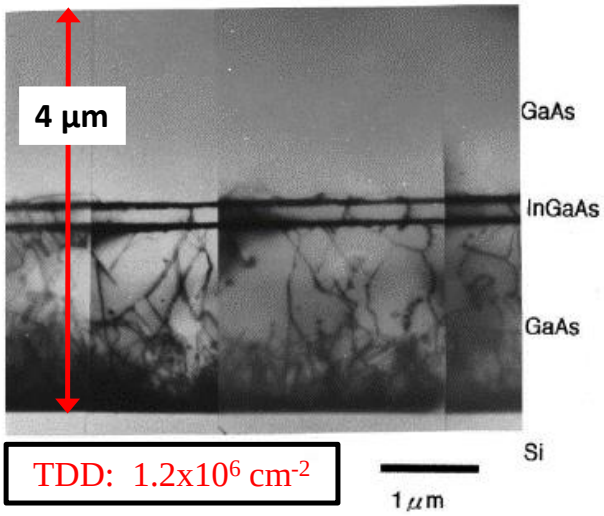

Fig. 14 Cross-sectional TEM micrograph of GaAs buffer grown on Si with an $In_{0.07}Ga_{0.93}As$ interlayer showing how the single strained layer is helping to bend the dislocation due to the misfit strain [**15**]. Used with permission from APL 1998.

threading dislocation density as low as $1.2x10^6$ cm^2 [**15]**. The thickness of the InGaAs interlayer, 200 nm was beyond the critical thickness and a relaxation of the InGaAs interlayer was found to be on the order of 70% by x-ray analysis [**15**]. The relaxation of the misfit strain in the InGaAs layer allowed the bending of threading dislocations in the epilayers near the surface, thus restricting their propagation into the active layer. **Fig. 14** shows the cross-sectional TEM micrograph of GaAs buffer grown on Si substrate with an $In_{0.07}Ga_{0.93}As$ interlayer showing how the single strained-layer is helping to bend the dislocation due to the misfit strain [**15**]. However, such an approach hasn't been given much attention for realizing III-V-on-Si solar cells. We propose to utilize GaAsSb as the single strained-layer to investigate the impact in reducing dislocation for GaAs grown on Si. Careful control of GaAsSb composition, placement in the buffer stack and thickness could prove to be a promising approach to bend the dislocation due to the relaxation of misfit strain associated with the different lattice constants. The GaAsSb path could further help minimize dislocation density since Sb would act as a surfactant and help glide dislocation density [**16**] better than In (for InGaAs case). The proposed 1J GaAs solar cell structure grown on Si substrate utilizing an intermediate 200 nm thick GaAsSb single strained-layer is shown in **Fig. 15**.

3.3.1 Calibration Sample for Antimony Composition

Valve cracker arsenic and antimony source was used to provide the As and Sb flux with each respective cracking zone temperature held constant at 900˚C. An antimony composition calibration sample was grown on (100)/2o off-cut GaAs substrate at fixed Ga growth rate of 0.3 µm/h. First an initial homoepitaxial GaAs

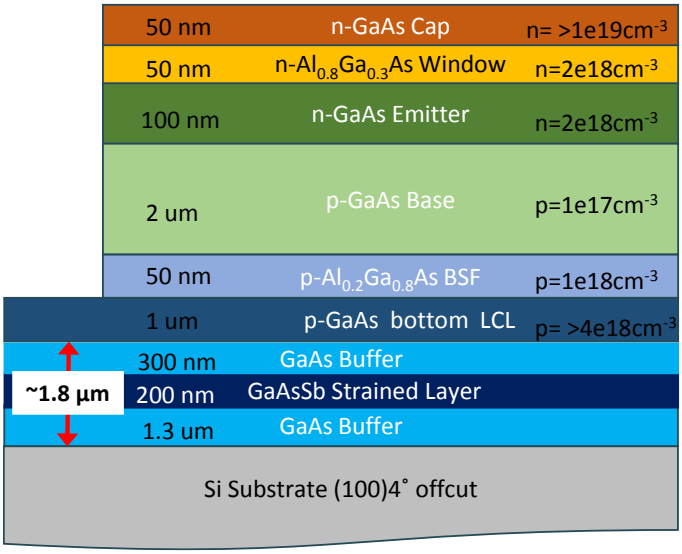

Fig. 15 Schematic of proposed 1J GaAs solar cell structure grown on Si substrate utilizing an intermediate 200 nm thick GaAsSb single strained-layer.

layer about 125 nm in thickness was grown on GaAs substrate at a substrate temperature of 450˚C, following the oxide desorption. Next, a 3-step graded $GaAs_xSb_{1-x}$ epitaxial layer structure was grown at a fixed substrate thermocouple temperature of 450˚C, starting with the lowest Sb composition layer first. The thickness of each layer grown was ~ 400 nm. The As/Ga and Sb/Ga ratio were varied for the three respective layers. First $GaAs_xSb_{1-x}$ layer was grown with ratios of As/Ga ~ 26 and Sb/Ga ~ 1, second $GaAs_xSb_{1-x}$ layer was grown with ratios of As/Ga ~ 16 and Sb/Ga ~ 1, and third second $GaAs_xSb_{1-x}$ layer was grown with ratios of As/Ga ~ 11 and Sb/Ga ~ 1.2, as shown in **Fig. 16(a)**. The alloy composition and strain relaxation properties of each $GaAs_xSb_{1-x}$ layer were characterized by high-resolution x-ray diffraction using both

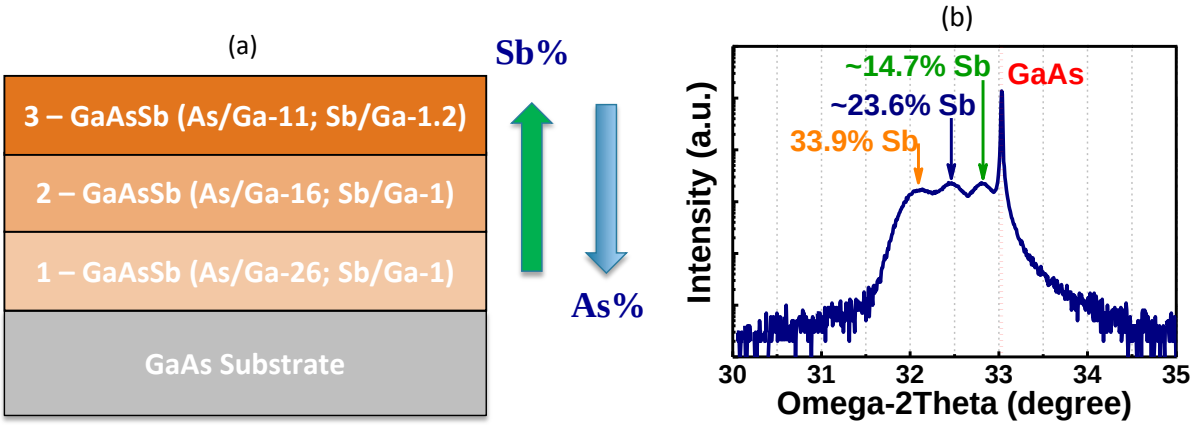

Fig. 16 (a) scematic growth structure and (b) ω/2θ XRD scan (004) for the step-graded $GaAs_xSb_{1-x}$ epitaxial layers grown on GaAs substrate for calibration of Sb composition and growth parameters using our new installed Sb cracker cell.

rocking curve (ω/2θ scan) and reciprocal space maps (RSMs). **Fig. 16(b)** shows the ω/2θ XRD scan (004) for the step-graded $GaAs_xSb_{1-x}$ epitaxial layers grown on GaAs substrate. The measured Sb composition in the respective $GaAs_xSb_{1-x}$ layers were found to be ~ 14.7%, 23.6%, and ~ 33.9%, respectively using the Vegard's law. The symmetric (004) and asymmetric (115) RSMs of the step-graded $GaAs_xSb_{1-x}$ epitaxial layers grown on GaAs substrate are shown in **Fig. 17 (a)** and **Fig. 17 (b)**, respectively. The measured Sb composition is indicated at each reciprocal lattice point taking into account the tilt component and relaxation. High Sb composition layer exhibits contour (RSM) and peak broadening (RC) likely due to the higher lattice-mismatch and only ~ 400 nm thickness to accommodate the dislocations and defects. Each respective layer was found to be almost fully relaxed with respect to the GaAs substrate from the asymmetric (115) analysis. From the extracted alloy compositions, it can be inferred that the Sb composition had a direct dependence on the As/Ga and the Sb/Ga ratio, consistent with prior observation [**17**]. We always investigated the surface morphology and root-mean-square (rms) roughness of the surface by atomic force microscopy in the Scan Asyst mode (similar to contact mode) to determine if Sb was forming clusters at the surface and making the surface rough. **Fig. 18** shows the AFM micrograph of the surface of $GaAs_{0.66}Sb_{0.34}$ grown on GaAs substrate utilizing a step-graded $GaAs_xSb_{1-x}$ buffer. A very weak cross-hatch pattern was observed, most likely suppressed due to the high Sb composition final layer. An RMS roughness of 2.29 nm for 20 µm x 20 µm scan area suggests very good surface morphology. Sb clustering during growth also appears likely, which could be contributing to the surface roughness over lower composition

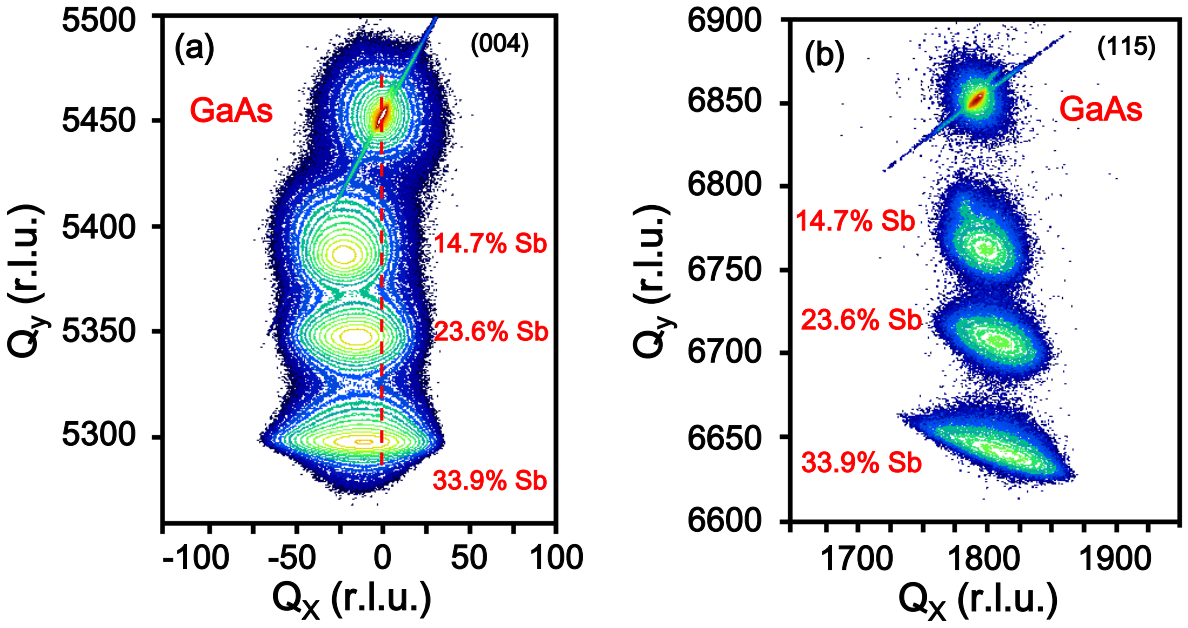

Fig. 17 a) Symmetric (004) and **(b)** asymmetric (115) RSMs the step-graded $GaAs_xSb_{1-x}$ epitaxial layers grown on GaAs substrate for calibration of Sb composition and growth parameters.

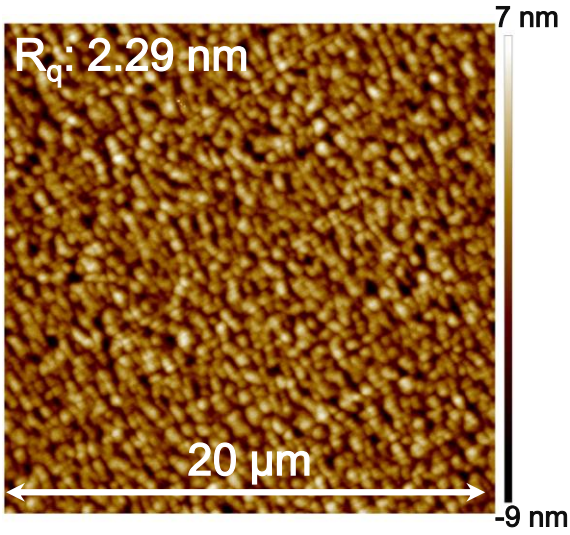

Fig. 18: AFM micrographs of the surface of $GaAs_{0.66}Sb_{0.34}$ grown on GaAs substrate utilizing a step-graded $GaAs_xSb_{1-x}$ buffer. The RMS roughness for scan area of 20 µm x 20 µm was 2.29 nm.

$GaAs_xSb_{1-x}$ grown on GaAs. Further optimization of the growth temperature could help achieve even smoother surfaces.

A good understanding of the modulation of Sb composition in ternary $GaAs_xSb_{1-x}$ layers was achieved using As/Ga and Sb/Ga as the key knob. Our next goal was to determine the Sb composition in the single strained $GaAs_xSb_{1-x}$ layer and realize high-quality GaAs-on-Si buffers and 1J GaAs-on-Si solar cell structures by utilizing an intermediate GaAsSb single-strained layer. It was found that the stress field associated with SLS has a shear component that forces the 60° dislocations to bend at the SLS interfaces and the individual layer thickness should be close to maximum critical layer thickness to maximize the gliding forces acting on the dislocations [**12**]. The number of bent-over threading dislocations in a given system depends critically on the total energy change (Δ.E) associated with the introduction of misfit dislocations segments. Generally, Δ.E is determined by the strained-layer thickness, h and the misfit strain, f between the strained layer and substrate [**14**]. The energy model by *El-Masry et. al* defines the minimum critical thickness as the thickness at which the threading dislocation will spontaneously bend along the strained interface [**14**]. The other models like the one by Matthews and Blakeslee, define it as the thickness above which bending can occur [**18-20**]. **Fig. 19** shows the comparison between the calculated minimum critical layer thickness versus the misfit strain calculated from mechanical equilibrium and the energy equilibrium model [**14**]. Our goal was to demonstrate a proof-of-concept and experimentally determine if a single strained-layer of $GaAs_xSb_{1-x}$ was effective in bending the dislocations and minimize the dislocation propagation during GaAs-on-Si growth. No attempts of optimization in terms of Sb composition, thickness and placement were

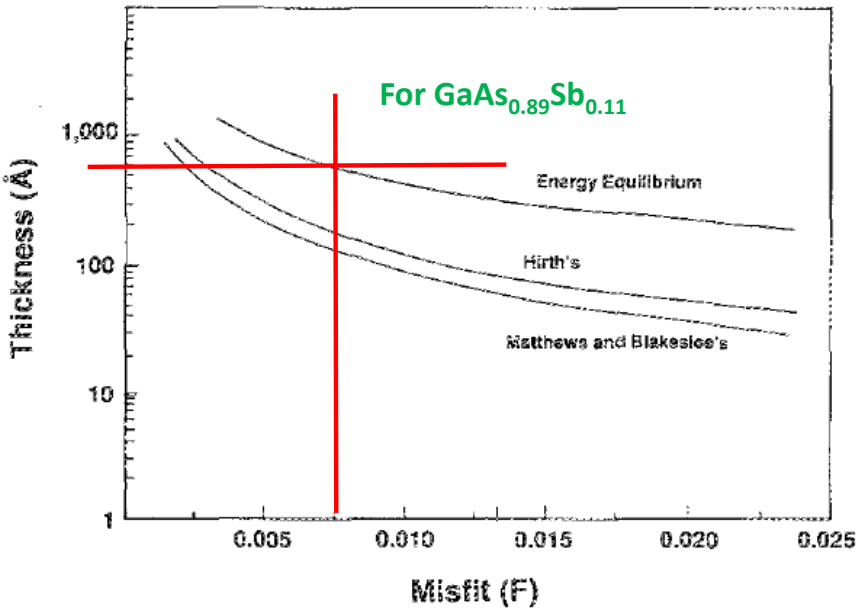

Fig. 19 Comparison between the calculated minimum critical layer thicknesses versus the misfit strain calculated from mechanical equilibrium and the energy equilibrium models [**14**]. Used with permission from APL 1989.

made in this dissertation. This could be an interesting subject for future research not only from material standpoint but also in implementing such buffer structures to realize III-V-on-Si devices. We chose an initial Sb composition of ~ 10% and fixed the thickness of $GaAs_xSb_{1-x}$ strained layer at 200 nm, higher than the proposed thickness by the energy equilibrium model from **Fig. 19** as a starting conservative approach to understand dislocation interaction at the $GaAs_xSb_{1-x}$ strained layer interfaces. Preliminary GaAs buffers (1.6 µm in thickness) were grown on n-type Si (100) substrate with 6˚off-cut towards <110> by utilizing an intermediate 200 nm thick GaAsSb single-strained layer. The GaAs buffer thickness below the GaAsSb

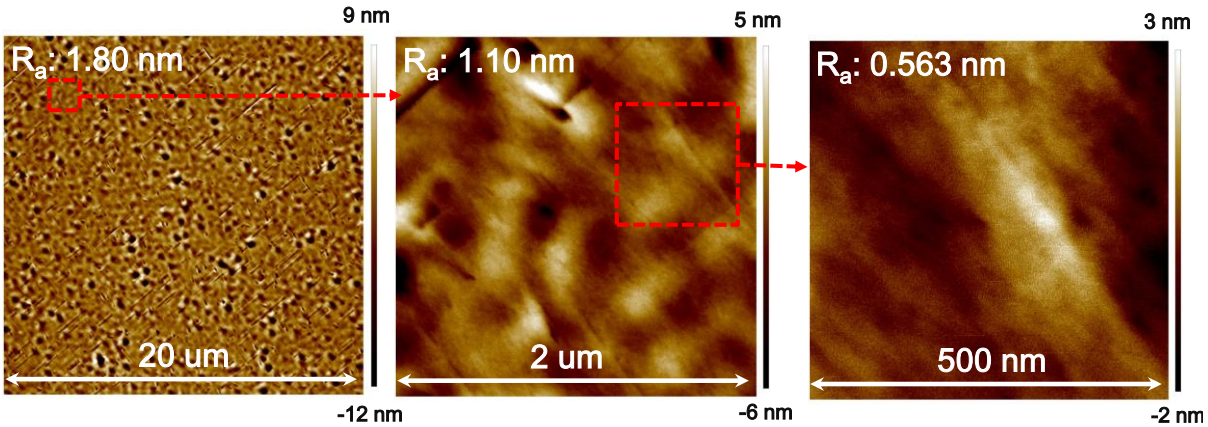

Fig. 20 AFM micrographs for GaAs buffer (1.6 µm) grown on Si substrate utilizing a GaAsSb single-strained layer. Scan areas are: (a) 20 µm x 20 µm, (b) 2 µm x 2 µm, and (c) 500 nm x 500 nm.

layer was 1.2 µm, and an additional 0.2 µm GaAs was grown above the GaAsSb strained layer. **Fig. 20** shows the AFM micrographs of the surface of GaAs buffer (1.6 µm) grown on Si substrate including an intermediate 200 nm thick GaAsSb single-strained layer (a) 20 µm x 20 µm, (b) 2 µm x 2 µm, and (c) 500 nm x 500 nm. An average roughness of ~ 1.80 nm was measured on 20 µm x 20 µm scan area, indicating excellent quality of lattice-mismatched GaAs grown on Si substrate utilizing the strained $GaAs_{0.84}Sb_{0.16}$ layer. Additionally, it can be inferred that the addition of $GaAs_{0.85}Sb_{0.15}$ layer does not degrade the surface roughness of the GaAs buffer (comparable to the roughness reported in the previous section for 2 µm thick GaAs buffer directly grown on Si substrate – **Fig. 12**).

Next, we discuss the growth of 1J GaAs-on-Si solar cell structures realized by utilizing an intermediate GaAsSb single-strained layer. The strain relaxation properties, surface morphology and defects and dislocation propagation in the epitaxial GaAs-on-Si solar cell structure are discussed.

3.3.2 Solar Cell Growth on Si and Structural Characterization

The epitaxial growth process for GaAs-on-Si solar cell structures with the intermediate GaAsSb single-strained layer was performed was very similar to the approach for 1J GaAs solar cells directly grown on Si substrate. Same growth conditions such as growth rate, thicknesses, doping densities and growth temperatures were utilized. The solar cells with the intermediate strained-layer samples were grown on 3-inch n-type Si (100) substrate with 6˚off-cut towards <110>. Our goal was to still target a buffer thickness of less than ≤ 2 µm below the start of the lateral conduction layer. The proposed 1J GaAs solar cell structure grown on Si substrate utilizing an intermediate 200 nm thick GaAsSb single strained-layer is shown in **Fig. 15**. The growth initiated in a similar fashion compromising of low-temperature, low-growth step followed by subsequent high-temperature and high growth-rate step. The temperature of the GaAs buffer layer was eventually bridged in small steps to reach the 575˚C temperature for solar cell growth. While, the entire solar cell structure was grown at a fixed substrate temperature of 575˚C (thermocouple temperature), the GaAsSb intermediate layer was grown at 450˚C to achieve a target Sb composition of 10% based on the findings from our calibration sample. The GaAs thickness below and above the GaAsSb strained layer was ~ 1.3 µm. The last 1 µm of GaAs thickness above the GaAsSb layer was very heavily doped p-type to realize the lateral conduction layer. We discuss the material characterization results to investigate the quality of such 1J GaAs solar cell structures grown on Si substrate utilizing an intermediate strained GaAsSb layer.

To gain further insight into the defect properties and structural quality of 1J GaAs solar cell structure grown on Si substrate utilizing a single strained GaAsSb layer, we performed cross-sectional TEM analysis. **Fig.**

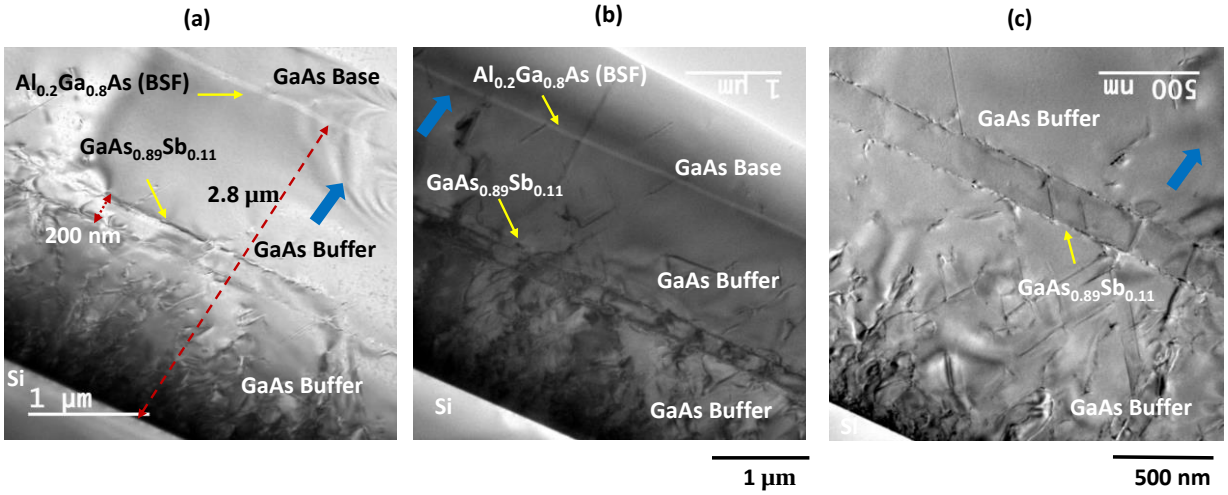

Fig. 21 (a), (b) XTEM micrographs of 1J GaAs-on-Si solar cell structure utilizing an intermediate GaAsSb single-strained layer and **Fig. 21 (c)** shows the high-resolution TEM micrograph of the GaAs buffer region. It can be seen that due to the misfit strain, the dislocation bend horizontally at the GaAsSb interfaces and only few threading dislocation propagate beyond the GaAsSb strained-layer.

21 (a) and **Fig. 21 (b)** shows the cross-sectional TEM micrographs of 1J GaAs-on-Si solar cell structure utilizing an intermediate GaAsSb single-strained layer and **Fig. 21 (c)** shows the high-resolution TEM micrograph of the GaAs buffer region. The respective thicknesses of each layer are marked in the figure. The fringes on the upper right hand side of **Fig. 21 (a)** are likely due to sample preparation related issue. It can be clearly seen from these TEM micrographs that the strained-layer is effective in minimizing the

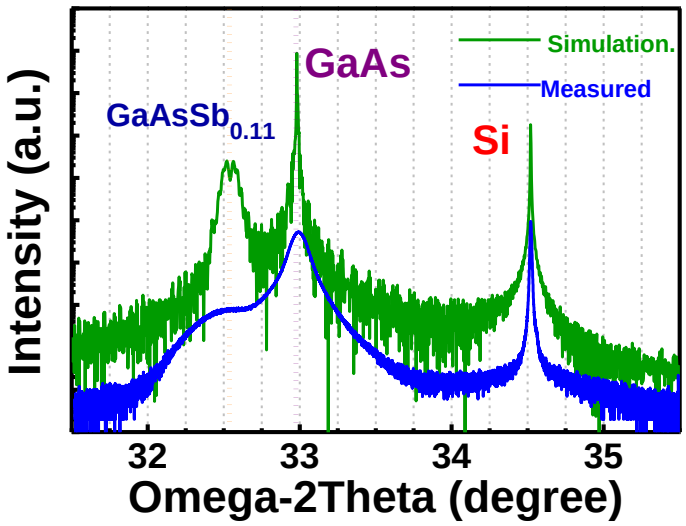

Fig. 22 ω/2θ XRD scan (004) for 1J GaAs solar cell structure grown on Si utilizing an intermediate 200 nm thick GaAsSb single strained-layer. By taking into account the strain relaxation in the GaAsSb layer, rock curve simulation was utilized to extract the Sb composition.

dislocation propagation beyond the strained-layer and very few dislocation propagate into the active GaAs base region. From these TEM micrographs, it is also evident that the strained-layer is also generating a few defects, which could like be attributed to some strain relief mechanism allowing partial relaxation of the film.

Next, we discuss the XRD composition analysis for the GaAsSb strained-layer and evaluate the strain relaxation properties of the entire solar cell structure as well as the GaAsSb strained-layer. **Fig. 22** shows the ω/2θ rocking curve (004) along with a simulated rocking curve to extract the Sb composition in the strained GaAsSb layer. The symmetric (004) and asymmetric (115) RSMs of 1J GaAs solar cell structure grown on Si substrate with a 1.8 µm thick buffer comprising of an intermediate 200 nm thick GaAsSb single-strained layer are shown in **Fig. 23 (a)** and **(b),** respectively. From the measured RSMs, the out-of-plane lattice constant, c (from (004) RSM), and the in-plane (in the growth plane) lattice constant, a (from (115) RSM), were determined. The relaxed lattice constant, a_r, and strain relaxation values were extracted from each RSM using the methods introduced in [**21**]. **Table I** shows the strain relaxation analysis of 1J GaAs solar cell structure grown on Si utilizing an intermediate 200 nm thick GaAsSb single strained-layer It can be clearly seen from the (115) RSM of **Fig. 23** that the GaAsSb layer was not fully relaxed, while the GaAs buffer and the cell structure was found to be almost fully relaxed with the reciprocal lattice points (RLPs) along the 15.8˚ full relaxation line. The relaxation in the GaAsSb film was found to 47% and the

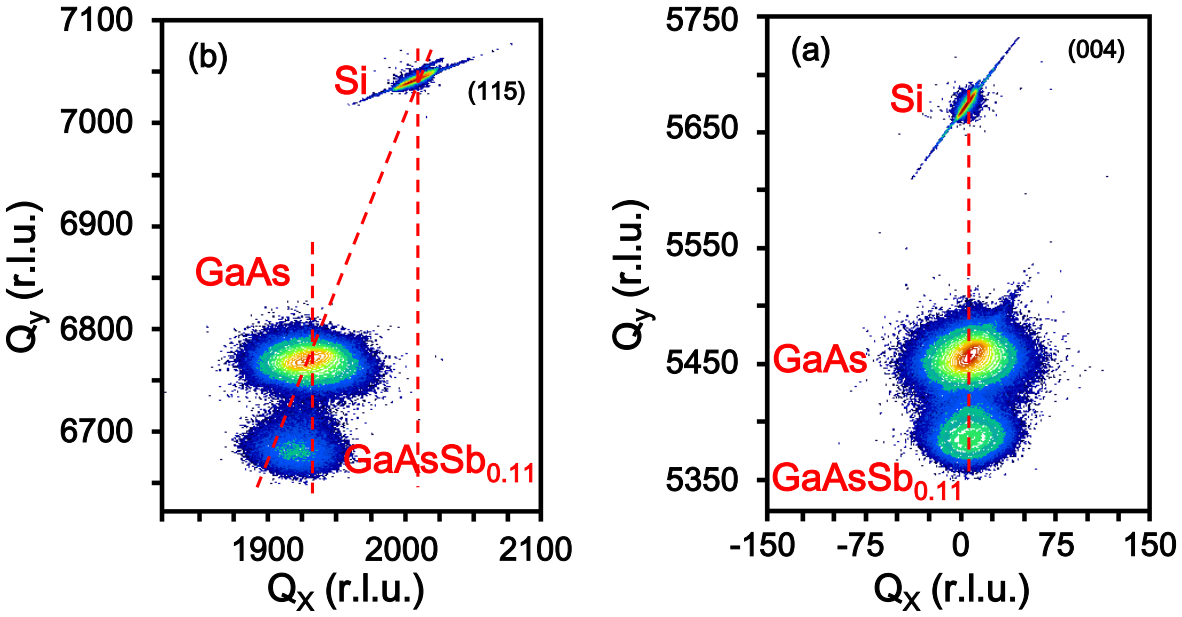

Fig. 23 a) Symmetric (004) and **(b)** asymmetric (115) RSMs of 1J GaAs solar cell structure grown on Si utilizing an intermediate 200 nm thick GaAsSb single strained-layer. A relaxation of 47% was calculated for the strained GaAsSb layer, while the GaAs buffer and the solar cell structure were almost fully relaxed.

Table I Strain relaxation analysis of 1J GaAs solar cell structure grown on Si utilizing an intermediate 200 nm thick GaAsSb single strained-layer

layer	hkl 004	lkl 115	c	a	a_r	GaSb MF	$\varepsilon_{//}$ [ppm]	ε_{perp} [ppm]	Relaxation (%)	Tilt (arcsec)	Strain (%, wrt substrate)
sub (GaAs)	0.6813	0.7080	5.6533	5.6533							
epi_1 (GaAsSb)	0.6724	0.6992	5.7282	5.6762	5.7022	11.1	4558	-4551	47%	18	0.87

associated Sb composition was about 11%. By fitting in the relaxation component of the GaAsSb layer, we confirmed the composition by overlaying rocking curve simulation with the experimental data, as shown in **Fig. 22**. It was due to this misfit strain from GaAsSb layer that allowed the bending of the threading dislocations horizontally instead of vertical propagation into the active device layers. However, this partial relaxation was expected since the 200 nm thickness of $GaAs_{0.89}Sb_{11}$ exceeded the critical layer thickness (~ 25 nm from Matthews and Blakeslee theory and ~ 60 nm from the energy equilibrium theory from **Fig. 19**). Thus, reducing the thickness of the GaAsSb would further help minimize the dislocation propagation, as observed in the cross-sectional TEM micrographs in **Fig. 21**. Nonetheless, the proof-of-concept and the effectiveness of utilizing a single strained GaAsSb layer has been demonstrated. No further attempts were made to optimize the parameters of the GaAsSb layers such as the composition, thickness, placement and growth temperature. This could be an interesting subject for future research not only from material standpoint but also to implement such buffer structures to realize III-V-on-Si devices.

3.4 Summary

The key technical challenge to improve the performance of "GaAs-on-Si" solar cell is to reduce the TDD. We have demonstrated a non-selective area, high-quality and thin (2 µm) epitaxial GaAs buffer directly grown on Si substrate. Si substrate cleaning, oxide desorption and initial low-temperature GaAs nucleation were found to be among the most critical components influencing the quality of GaAs-on-Si buffer.We have also demonstrated a novel proof-of-concept to reduce the TDD by leveraging the misfit strain from single-strained GaAsSb layer embedded in the direct GaAs buffer on Si. This is a promising path to bend the threading dislocations horizontally instead of allowing them to propagate vertically into the active device layers. Such an approach of a single strained-layer is a more scalable and controllable process in comparison to multiple strained layer super-lattice structures. Further investigation and optimization of the GaAsSb ternary layer in terms of Sb composition, layer thickness, and layer position and growth conditions could be exploited to achieve substantial reduction in dislocation density.

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Chapter 4

Solar Cell Fabrication & Process Integration Challenges

This chapter concentrates on the fabrication process for III-V-on-Si solar cells. Correlating the structural properties to device performance, our motivation for introducing all front side metal contacts is presented. Key process integration challenges including the contact resistance optimization, placement of bottom-metal on the front-side, anti-reflection coating design, mesa-etching and grid-finger swim-away are discussed. Role of simulation in aiding the importance of critical fab steps, such as cap layer etching and design of anti-reflection coating is also discussed.

4.1 Overview of Fabrication Process

The complete solar cell fabrication process was developed in-house at the Micro and Nano Fabrication Facility at Whittemore Hall, Virginia Tech. One of our key goals for III-V-on-Si solar cell fabrication was to achieve an all-front contact processed solar cell device. The motivation was to avoid the carriers from travelling through the highly-dislocated GaAs buffer connecting the III-V solar cell to the Si substrate. A 1 μm thick heavily doped GaAs lateral conduction layer was grown above the 2 μm thick GaAs buffer on Si for realizing the bottom contact. We also fabricated a few devices with conventional bottom-side metal on the back side of the substrate (Si and GaAs). A 4-level lithography process was developed and image-reversal IR) AZ 5214-IR photoresist was used. Initial developer we employed was AZ 400K, but now our process-of-record utilizes MF 319. The reasons for the switch in the developer are discussed in the subsequent section on process integration challenges. The cleanroom tools utilized for the solar cell fabrication process are listed below:

(1) Karl Suss MA-6 mask aligner
(2) KJ Lesker PVD-250 - E-beam metal deposition
(3) Trion PECVD - plasma enhanced chemical vapor deposition
(4) Filmetric
(5) Brucker Detak profilometer
(6) Acid and solvent bench
(7) Trion ICP-RIE Dry Etch tool
(8) In-house developed metal contact annealing furnace (with forming gas)

(9) LEO (Zeiss) 1550 field-emission SEM

(10) Woolam - Ellipsometer

4.1.1 Solar Cell Fabrication Process Flow: 1J GaAs-on-Si

The fabrication process sequence for 1J GaAs-on-Si solar cell is as follows:

(i) Native oxide clean in NH_4OH:DI water solution (1:1 by volume ratio)

(ii) Level I Lithography (*positive lithography*)

- Mesa-etch pad definition
- Wet mesa-etch for device isolation (phosphoric acid for GaAs cell)

(iii) Level II Lithography (*negative lithography*)

- Front grid-finger metal contact definition
- PVD metallization (Au/Ge/Au/Ni/Au alloys for n-GaAs terminal)
- Lift-off in acetone

(iv) Level III Lithography (*negative lithography*)

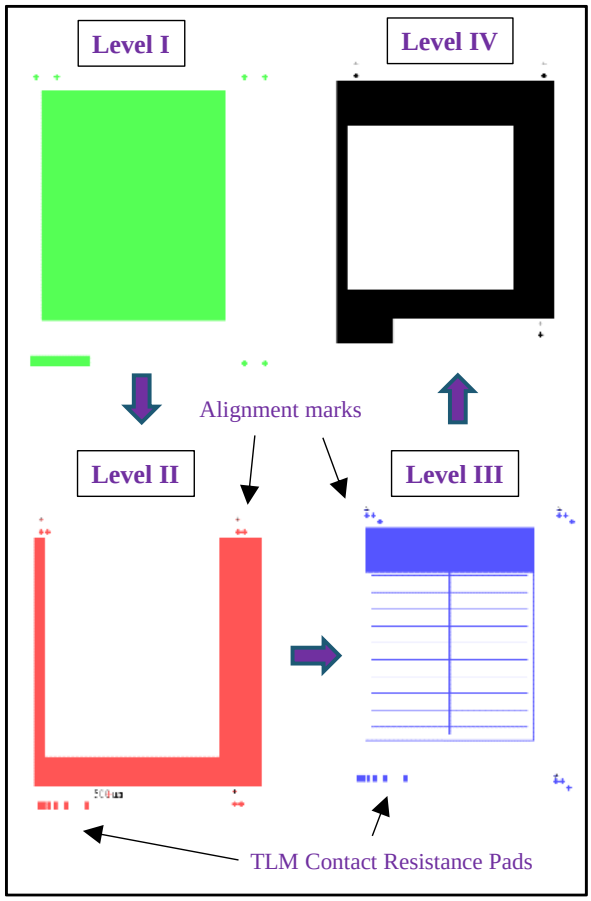

Fig. 1 Mask-set for the 4-level lithography process of 1J GaAs-on-Si solar cell fabrication

- Bottom-side metal contact definition
- PVD metallization (Ti/Pt/Au for p-GaAs terminal)
- Lift-off in acetone

(v) GaAs cap-layer selective wet-etch w.r.t AlGaAs window layer using citric acid

(vi) Level IV Lithography (*positive litho for ARC lift-off & negative litho for ARC etch*)

- Front and bottom metal contact probe-area definition
- ARC deposition (PVD for MgF_2/ZnS and PECVD for Si_xN_y)
- Lift-off in acetone

The L-EDIT mask layout design for the 4-level lithography process to fabricate 1J GaAs-on-Si solar cell is shown in **Fig. 1**. The contact pads for transfer length measurement to determine both front and bottom metal contact resistance are shown in the figure. The process sequence changes slightly depending upon if the anti-reflection coating layer is lifted-off or is etched. For the ARC lift-off process, the level-IV positive lithography is performed first, followed by the GaAs cap-etch just prior to loading into the PVD chamber for MgF_2/ZnS based ARC deposition. Thereafter, the ARC layer is lifted-off, opening front and bottom-metal areas for probing. For ARC-etch based process, the silicon nitride based ARC is deposited first, followed by level-IV negative lithography. This allows to etch the ARC-layer above the front and bottom-

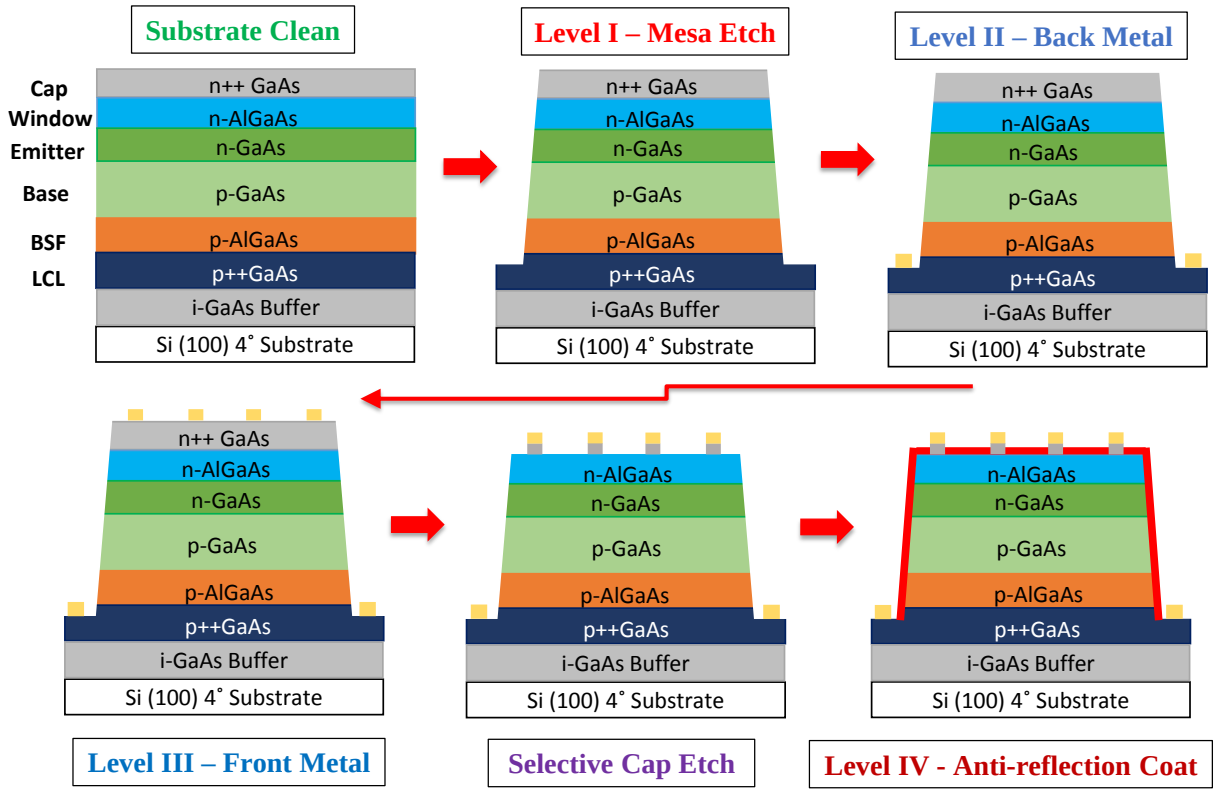

Fig. 2 Fabrication process flow for 1J GaAs-on-Si solar cell

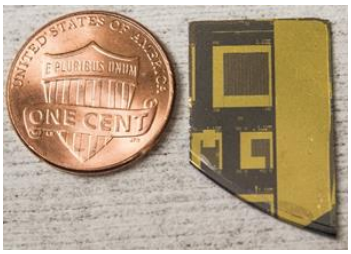

Fig. 3 Optical image of 0.5 cm^2 1J GaAs solar cell grown on Si substrate with both front-side metal contacts.

metal probe areas. The complete 4-level lithography process for fabricating 1J GaAs-on-Si is summarized in **Fig. 2** (ARC lift-off process). Our mask design had options of 3 different cell sizes – 1x1 cm^2, 0.5x0.5 cm^2 and 0.2x0.2 cm^2. An optical image of a processed 0.5x0.5 cm^2 1J GaAs-on-Si solar cell with both front-side metal contacts is shown in **Fig. 3**. A one cent coin is shown adjacent to the cell for size comparision. Various optical and SEM images were taken at specific regions of the cell to examine fine details of the processed device and understanding possible design changes which will improve the subsequent cell fabrication process flow. Some of these images are shown in **Fig. 4.**

4.2 Anti-Reflection Coating Design

Achieving low reflectance at the front surface of a solar cell is extremely important to be able to capture most of incident photons from the solar spectrum. It is very critical to careful bridge the refractive index of the air-medium to the III-V cap layer (GaAs in our case). For developing anti-reflection coating, we initially utilized a single layer silicon nitride as the ARC layer [**1**]. The Si_xN_y was deposited using PECVD process at a temperature of 250˚C to minimize the effects associated with the high-temperature exposure of the high Al-content AlGaAs window layer (>70%). The SiN coatings were processed using the ARC etch process as discussed in section 8.1 and both wet and dry etching were investigated. For wet-etching, buffer oxide etch was utilized, while the process gas for dry RIE-etching utilized was SF_6. We have now transitioned to a dual-layer MgF_2/ZnS based ARC layer as our current process of record, deposited using PVD at room temperature. The room temperature PVD process allows the possibility of MgF_2/ZnS ARC lift-off that was not possible when using SiN based ARC layer. The high temperature process involved in the PECVD process would not be compatible with the photoresist processing temperatures. Regardless of the ARC lift-off or ARC etch process, the GaAs cap layer was precisely etched before the ARC deposition (discussed in section 8.3). The importance of precise etching of GaAs cap-layer and an ideal ARC design for a prototype 1J GaAs solar cell is highlighted by the simulated performance results shown in **Fig. 5**. The Crosslight simulation results suggest that the absolute performance of 1J GaAs solar cell could exceed 25% by

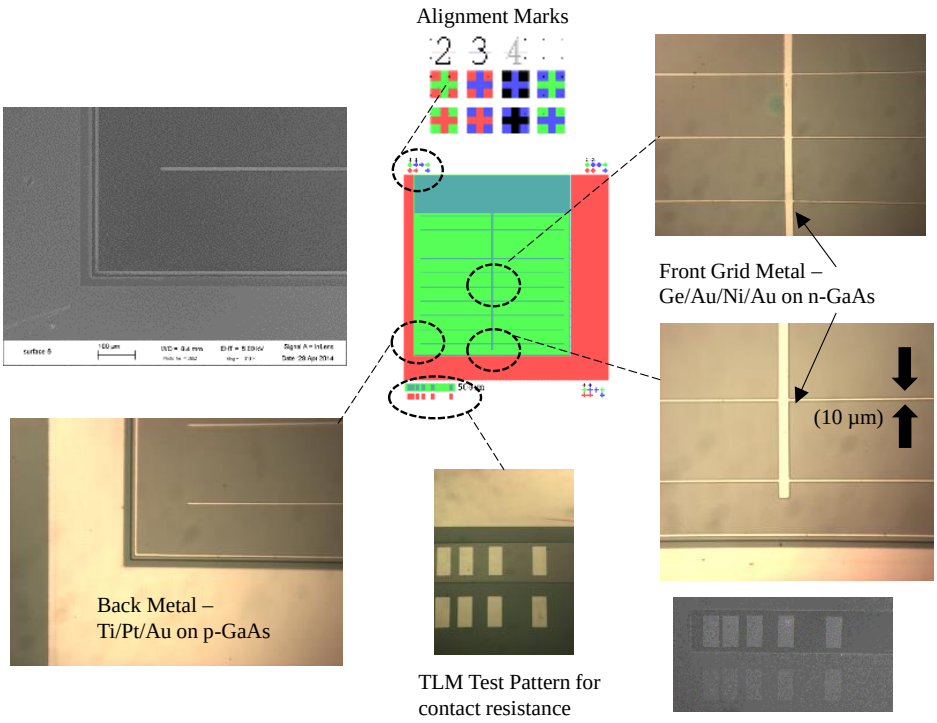

Fig. 4 Optical and SEM images of specific regions of a processed 1J GaAs-on-Si solar cell.

combining a well-controlled cap-etch process with an optimal ARC-design. We eventually plan to transition to a tri-layer $SiO_2/Si_xN_y/TiO_2$ which maintain excellent transmission over substantial range of the incident solar spectrum, necessary for multi-junction solar cell designs as evident from **Fig. 6.** It can be clearly seen that a tri-layer $SiO_2/Si_xN_y/ TiO_2$ anti-reflection coating design is more efficient and would outperform a bi-

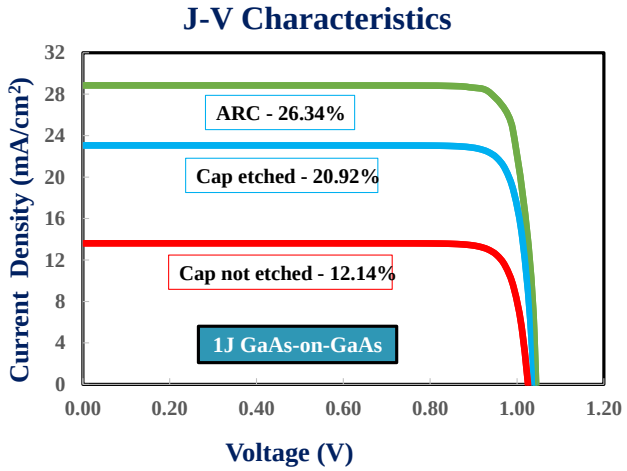

Fig. 5 1J GaAs-on-Si performance prediction using Crosslight simulation signifying the importance of GaAs cap-etch and an optimized ARC cell design (this result utilizes a bi-layer MgF_2/ZnS ARC layer).

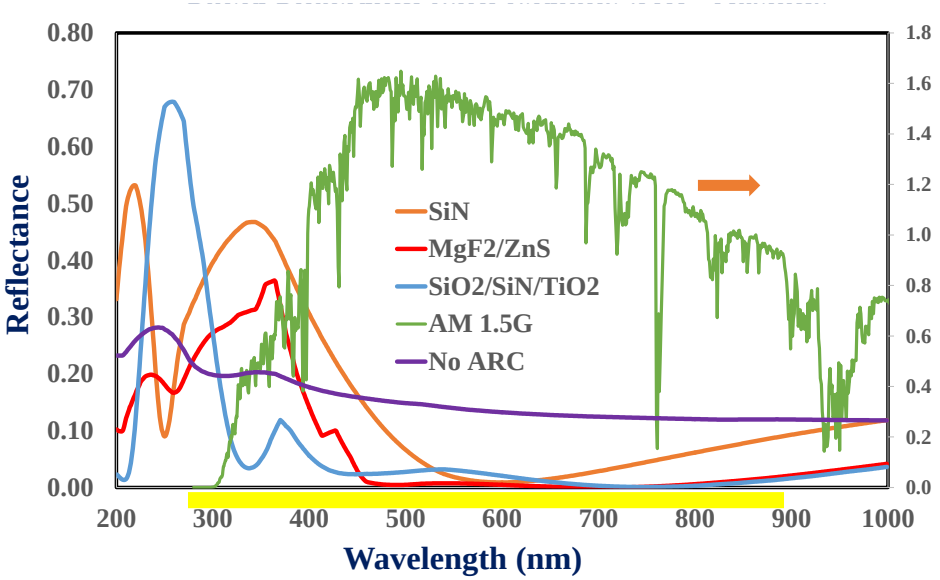

Fig. 6 Anti-reflection coating (ARC) designs: **purple** – bare III-V solar cells with no ARC; **orange** – single layer SiN ARC layer, **red –** bi-layer MgF_2/ZnS layer **blue –** tri-layer $SiO_2/Si_xN_y/ TiO_2$ layer, **green** – reference AM1.5g spectrum. It can be clearly seen tri-layer ARC serves as the best broadband layer.

layer MgF_2/ZnS stack for multijunction solar cells to span a wide range of the solar spectrum. The AM1.5g solar spectrum and reflection percentage for bare AlGaAs window layer is also included for reference.

4.3 Process Integration Challenges

Several complex process challenges were comprehensively investigated and addressed during this PhD work. Some of the key process related challenges faced includes: (1) realize positive sidewall slopes and no under-cut during mesa-etch process essential to realize both front side metal contacts – motivation was to prevent current from flowing through the GaAs buffer with high dislocation density, (2) precise control of the mesa-etch depth into the lateral conduction layer for bottom-metallization (under-etch would results in bottom metal positioned in the base or BSF of the cell), (3) un-even floor due to non-uniform etch across the four adjacent floors of the solar cells during mesa-etch process (dependent on how you hold the sample and sample size, (4) unclean mesa-etched streets due to post wet mesa-etch residue, 5) grid-fingers swim-away in the acetone bath during lift-off due to lithography issues, (6) selective etch of GaAs cap layer w.r.t to the AlGaAs window layer and minimizing the under-cut while using grid-finger lines as the wet cap-etch mask, (7) anneal sequence – do we anneal post cap-etch, prior to cap-etch or post ARC deposition. All these individual challenges were given great attention to fine-tune the process and develop a more robust and a repeatable fab process.

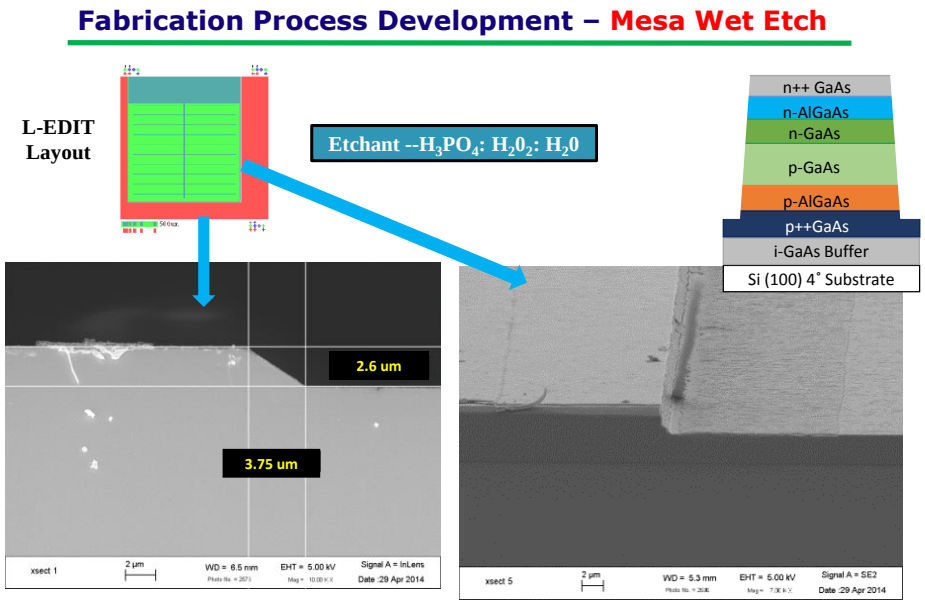

Fig. 7 Improvement in wet mesa-etch process: SEM micrograph suggesting positive-slopes attained across both cell edges to realize both front-side metal contacts to minimize carrier flow through highly-dislocated GaAs buffer connecting the III-V cell with the Si substrate.

Mesa-etching for GaAs cell isolation was initially performed using dry etching (ICP-RIE), but due to RIE chamber and repeatability issues we decided to use wet-etch process for GaAs mesa-etch using phosphoric acid based wet chemistry (H_3PO_4:H_2O_2:H_2O) [**2**]. The volume ratio of this chemistry was optimized to achieve a modest etch rate (~30 nm/s) to have a precise etch-depth control. A non-positive mesa-etch slope will block the deposition of the bottom metal. Such an approach of both front-side metal contacts is targeted to eliminate current flow through the GaAs buffer with high dislocation density and also minimize the resistive path, improving fill-factors. Using the optimal ratio for the phosphoric acid based wet chemistry, we were able to achieve positive side-walls across all the four edges of the cell in order to realize both metal contacts on the front side of the cell as shown in **Fig. 7**. The non-uniform etching across the perpendicular edges of the cell was addressed by using rectangular or square samples shapes such that the sample can sit flat on the sieve (with two of the sample edges almost parallel to the sieve floor). The sample was rotated 180˚ half-way through the etching to allow a more uniform-etch across all the four edges. After the mesa-etch, the samples were dipped in a 1:4 NH_4OH:DI for about 10s to remove the etch-residue and clean-up the mesa-etched streets between the cells.

Another challenging issue we encountered during the initial processing days was the grid-finger swim away during lift-off in acetone as shown in **Fig. 8**. This issue was attributed to rough grid-finger edges as shown in **Fig. 9** due to non-optimized lithography parameters. The positive exposure time was reduced for the

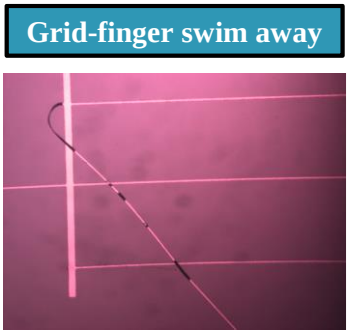

Fig. 8 Optical image showing solar cell grid-finger swim away during lift-off in acetone due to rough edges.

image reversal AZ 5214 resist (from 12s to ~ 6s), the flood exposure time and the bake time were also optimized which resulted in improving the rough edges and achieve more uniform grid-finger patterns as shown in **Fig. 9**. The improvement in the grid-finger lithography process almost completely eliminated grid-finger swim-away issues leading to a more robust and reproducible solar cell fabrication process and better yields.

For the AlGaAs window layer etch, a citric acid based chemistry was developed for selective wet-etching of GaAs contact layer from the AlGaAs window to minimize parasitic light absorption in the 1J GaAs solar cell. We used a 1:4 volume ratio of citric acid: DI water solution with an etch time of 20s for etching 50 nm GaAs cap. Over-etching was minimized to avoid severe grid-finger under-cuts that could also lead to grid-finger swim away.

Some of the key take-away points for fabrication are listed below:

(1) Periodically clean the mask with IPA and acetone and blow dry with nitrogen gas.

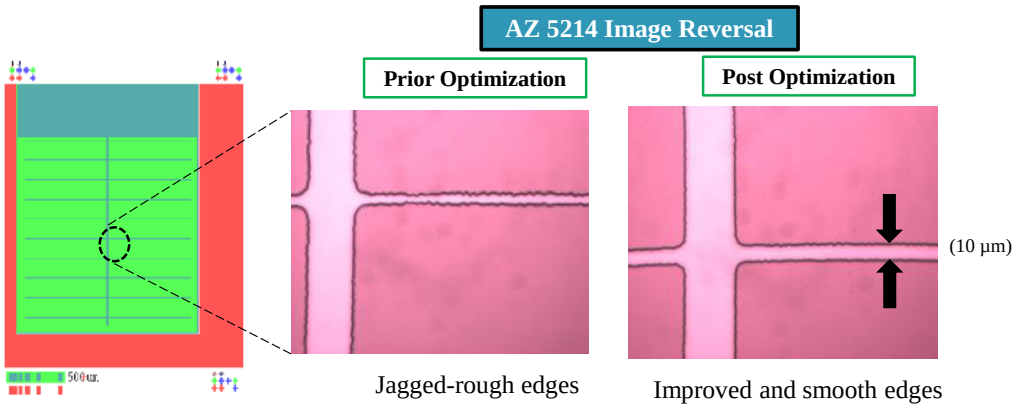

Fig. 9 Lithography process improvement targeted towards improving the rough grid-finger edges to minimize swim-away and improve yield, besides developing a more robust and repeatable process.

(2) Try cleaving square or rectangle shape for processing devices.

(3) Load PVD samples close to the center of the mounting plate, especially for ARC deposition

(4) Prior to metal/ARC deposition – a quick dilute $NH_4$0H clean helps clean up the surface and removes native oxide.

(5) Use of very dilute $NH_4$0H post mesa and cap-etches cleans up the surface.

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Chapter 5

Performance Analysis of GaAs-on-Si Solar Cells

In this chapter, we present the electrical and optical characterization results of our fabricated III-V-on-Si solar cells to evaluate their performance under AM1.5g spectrum (1-sun). . The significance of utilizing both front-side metal contacts for III-V-on-Si solar cells is discussed. The light and dark current-voltage (I-V) characteristics, quantum efficiency (QE), reflectance and contact resistance analysis are also discussed. Key factors limiting the performance of "GaAs-on-Si" solar cells are identified, and on-going research efforts focused on minimizing threading dislocation density are discussed.

5.1 Motivation for both Front-Side Metal Contacts

Conventional 1J GaAs solar cells and most 1J GaAs-on-Si solar cells utilize the back-side of the substrate as the bottom contact. In-order to circumvent the carrier flow through the highly dislocated GaAs buffer, we proposed to utilize our bottom-contact on the front-side of the wafer above the GaAs buffer. For a 1J

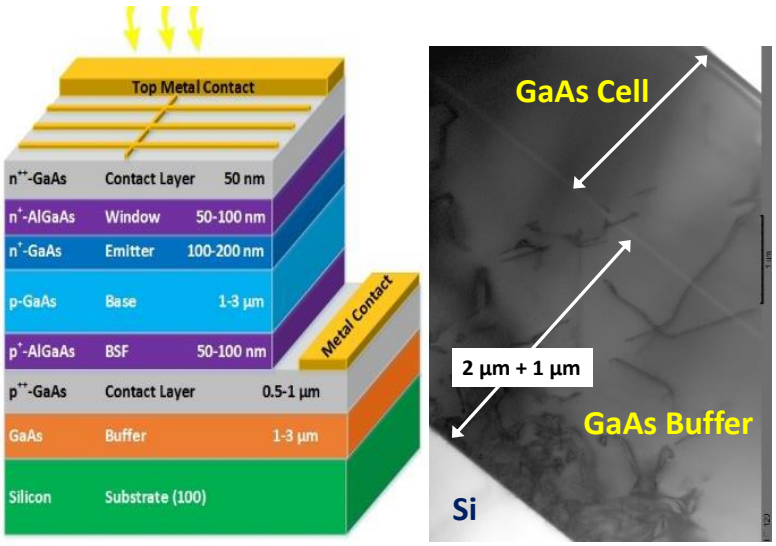

Fig. 1 1J GaAs solar cell structure grown directly on Si substrate using a 2µm GaAs buffer and the corresponding cross-sectional TEM micrograph, indicating some dislocations propagate into the active cell. To circumvent the carrier flow from the highly dislocated buffer, we employed both front-side contact scheme.

GaAs solar cell on Si substrate, researchers have previously employed a 7 µm thick n+ GaAs buffer between the cell structure and the Si substrate to achieve an efficiency of 17.6% (J_{sc}=25.5mA/cm^2, V_{oc}=0.891V and FF=77.7%) Si under AM1.5 at a TDD of ~8x10^6 cm^{-2} [**1**]. Such thick buffers are expected to result in lower dislocation density, attributed to the additional thermal budget associated with growing thicker films. However, such thick buffers not only significantly add to the overall growth time but also to the overall cost. Thus, it could be expected that our GaAs solar cell directly grown on Si substrate using only a 2 µm thick GaAs buffer would more than likely have higher dislocation density. **Fig. 1** shows 1J GaAs solar cell structure grown directly on Si substrate using a 2µm GaAs buffer and the corresponding cross-sectional TEM micrograph, indicating some dislocations propagate into the active cell. To circumvent the carrier flow path from the highly dislocated buffer, we proposed to employ both n- and p-terminal contacts on the front-side of the cell. Additional benefits could include eliminating the series resistance component from the bulk Si substrate if both contacts are used on the front side as shown in **Fig. 1**. A downside of this approach is losing the active front solar cell surface area, but our motivation was to investigate if there is a significant performance benefit which could potentially outweigh the front side area loss. A 1 µm thick heavily doped GaAs lateral conduction layer was grown above the 2 µm thick GaAs buffer on Si for realizing the bottom contact. We also fabricated a few devices with conventional bottom-side metal on the back side of the substrate (Si and GaAs). This particular Si substrate was doped p-type (boron doped) with resistivity in the range of 1-5 ohm-cm. **Fig. 2** shows the J-V characteristics of a prototype 1J GaAs-on-Si solar cell indicating the impact of both front side metal contacts in comparison to conventional one front top side contact and the bottom contact on the back-side of the wafer. This particular 1J GaAs-on-Si solar cell was chosen from the lot which had issues with one of the fabrication steps (likely bottom-contact

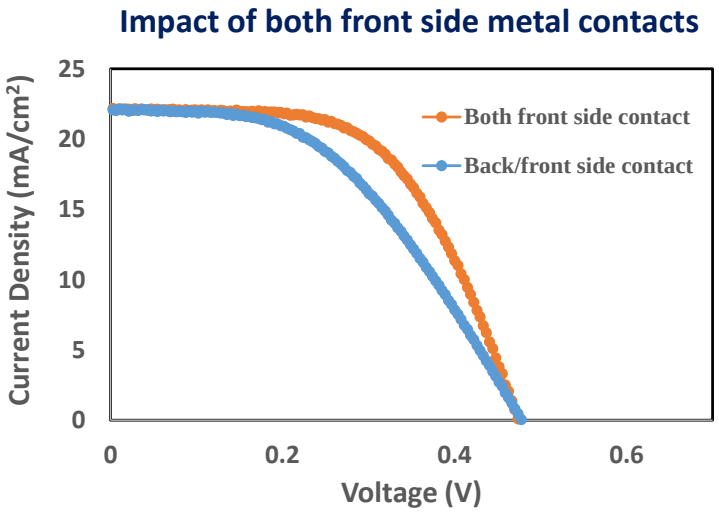

Fig. 2 J-V characteristics of a prototype GaAs-on-Si solar cell indicating the impact of both front side metal contacts.

alignment). The fill-factor drops from 57.58% to 46.56%, while the AM1.5g 1-sun efficiency drops from 6.043% to 4.91%, when conventional bottom contact on the wafer back-side is utilized. Utilizing bottom contact on the back-side of the unpolished Si wafer drastically affects the fill-factor as seen from the J-V characteristics. This was attributed to the cumulative effect of high dislocation density in the GaAs buffer and the series resistance contribution from the Si substrate. Thus, the performance benefits by utilizing both front side metal contacts are clearly evident from **Fig. 2**. Interestingly, there was no increment in the J_{sc} or V_{oc} when the conventional back-side contact on the bottom side of the Si wafer was utilized. Hence, it could be inferred that the arsenic exposure to Si wafer during initial growth was insufficient in forming an active Si junction on the p-type Si substrate.

5.2 Contact Resistance Analysis

Achieving low contact resistance is very important for optimizing the performance of solar cells, especially for operation under concentrated sunlight. The impact of high-contact resistance could affect the short-circuit current, the fill-factor and in-turn the cell performance. Improper metallization condition, non-optimized contact layer parameters (doping, composition and thickness), anneal conditions and appropriate pre-metal native oxide removal technique. The contact resistance of our n-type GaAs and p-type GaAs contacts was analyzed using the well-established linear transfer length method (TLM). For n-on-p solar cell configuration, the top contact above the window layer was a heavily doped (Si-doped) n-type GaAs layer, ~ 50 nm in thickness with a target concentration of $1x10^{19}$ cm^{-3}. For the p-type contact, a 1 µm thick lateral conduction layer was utilized below the BSF of the 1J GaAs solar cell as the bottom-contact layer. This

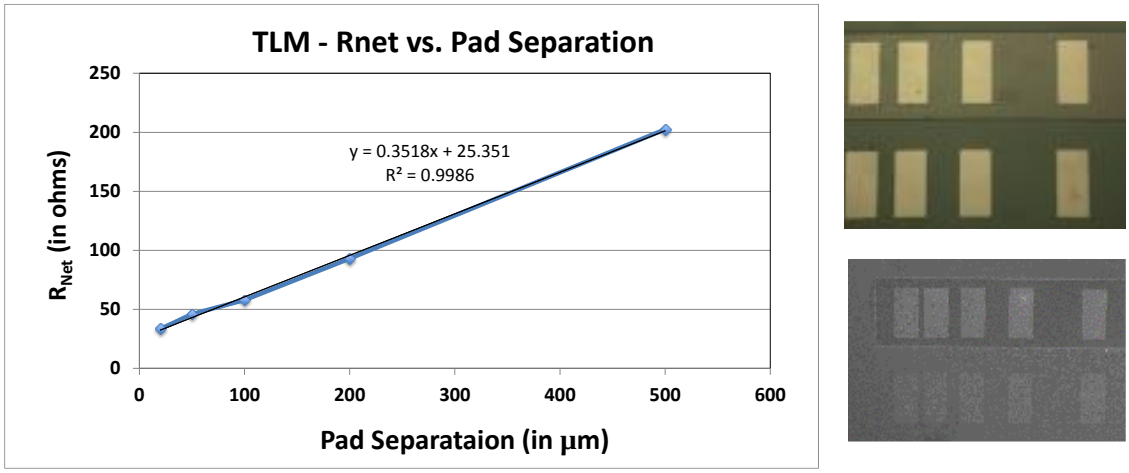

Fig. 3 Net resistance versus pad spacing for TLM contact resistance extraction using 4-probe I-V measurement for n-type GaAs (Si-doped) contacts. An optical and SEM image of the TLM pads is shown on the right. A specific contact resistance of $4.57x10^{-4}$ Ω-cm^2 was extracted for gate metal stack of Au/Ge/Au/Ni/Au.

layer was Be-doped with a target concentration of $8x10^{18}$ cm^{-3}. For n-type GaAs, a metal stack of Au/Ge/Au/Ni/Au was utilized, while for p-type GaAs, a metal stack of Ti/Pt/Au was utilized, with the top gold layer thickness of 150 nm for both contact types. Prior metallization, the patterned sample were dipped in 1:4 NH_4OH:DI solution for ~30s. Increasing the thickness of top gold layer or adding additional thickness of a very conductive metal layer is further expected to improve the series resistance. **Fig. 3** shows the net resistance versus pad spacing plot for TLM contact resistance extraction using 4-probe I-V measurement for n-type GaAs (Si-doped) contacts. An optical and SEM image of the TLM pads is shown on the right. A specific contact resistance of $4.57x10^{-4}$ Ω-cm^2 was extracted for the n-type GaAs gate metal stack of Au/Ge/Au/Ni/Au, while there is still room to optimize the p-GaAs contact.

5.3 Quantum Efficiency & Reflectance Analysis

Quantum efficiency analysis provides key insight into the cell design. Especially, for multijunction solar cells, short-circuit current density could be extracted from individual subcells using QE measurements and aid in current-matching. The QE and the I-V station set-up used for characterizing our in-house fabricated solar cells are shown in **Fig. 4**. The QE system (Newport IQE200 series) utilizes a xenon lamp and has the capability to measure the internal quantum efficiency (IQE), external quantum efficiency (EQE) and reflectance over the entire solar spectrum starting from 300 nm – 1800 nm using a Si/Ge detector. The system has specific filters and light biasing capability to do QE measurements on individual subcells in a multijunction solar cell. For QE measurements, the incident beam spot size was much smaller than the sample area, unlike I-V measurement where the incident beam area is bigger than the cell size. While, the QE measurements was performed using a 2-wire measurement, all the I-V measurements were performed using a 4-wire measurement set-up to minimize the influence of parasitic resistance. Some of the most important definitions and formulas used for the solar cell performance analysis in this chapter are highlighted below:

$$\textbf{External Quantum Efficiency, EQE}(\boldsymbol{\lambda}) = \frac{\#\ Electrons\ collected\ as\ photocurrent/s}{\#\ Photons\ incident\ /s} \quad (1)$$

$$\textbf{Internal Quantum Efficiency IQE}(\boldsymbol{\lambda}) = \frac{\#\ Electrons\ collected\ as\ photocurrent/s}{\#\ Photons\ aborbed\ /s} \quad (2)$$

$$\textbf{IQE} = \frac{EQE}{1-Reflectance} \quad (3)$$

$$\textbf{Spectral Response, SR}\left(\frac{\mathbf{A}}{\mathbf{W}}\right) = \frac{QE}{\lambda(nm)}.\ 1239.8 \quad (4)$$

$$\textbf{Short-circuit current density, } \boldsymbol{J_{sc}} = q \int b_s\ (E).QE(E).dE \quad (5)$$

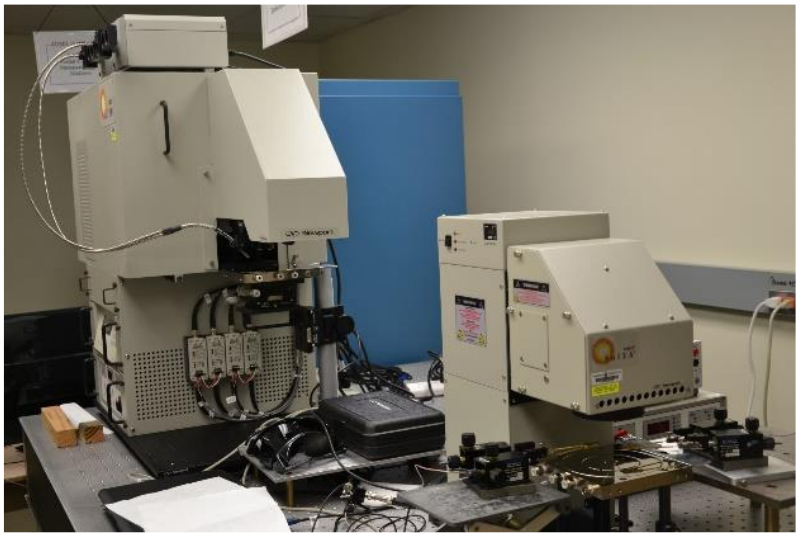

Fig. 4 Quantum efficiency and light/dark I-V measurement facility with the ADSEL group.

where λ is the incident wavelength and $b_s(E)$ is the incident photon flux density (# incident photons/ unit area/ unit time in the integral energy range from E to E+dE).

In the initial stages, to calibrate our system and investigate the quality of in-house GaAs solar cells, we performed QE measurements on a commercial space 3J solar cells from one of the leading solar cell manufacturer (in red) and compared its performance with our 1J GaAs solar cell grown lattice-matched on

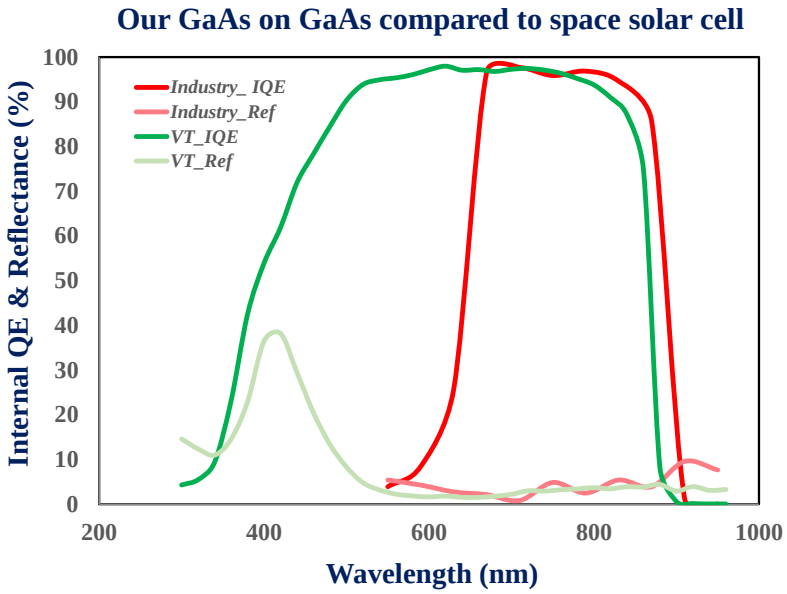

Fig. 5 Internal quantum efficiency (IQE) and reflectance plots for 1J GaAs solar cell. The plot in green is for our in-house 1J GaAs solar cell grown on GaAs substrate, while the plot in red is for a GaAs subcell in a 3J commercial space solar cell for validation.

GaAs substrate (in green), as shown in **Fig. 5**. The idea was to validate our epitaxal quality and our in-house developed solar cell fabrication process. The QE spectrum for commercial spectrum start from around 600 nm because the small wavelength is aborbed by the top subcell of the 3J solar cell, while our GaAs solar cell was a standalone 1J cell. Also, the shift in QE cut-off towards higher wavelength reflected smaller bandgap of the middle solar cell in the 3J configuration, likely due to the addition of indium to form an InGaAs subcell for better spectral-match. Nonetheless, comparable values for the IQE (> 90%) and the reflectance validate our epi and in-house fabrication process for GaAs solar cell. It is worth mentioning that, we utilized a bi-layer MgF_2/ZnS anti-reflection coating layer which might be different that the ARC layer on the commercial 3J solar cell. Furthermore, there is trenemdous scope of reflectance improvement for our cell in the low wavelength regime (300-500 nm).

Next, we evaluated the optical response of our 1J GaAs solar cell grown directly on Si substrate utilizing a 2 µm thick GaAs buffer. **Fig. 6** shows the IQE, EQE and reflectance plots for 1J GaAs solar cell directly grown on Si substrate (blue) versus 1J GaAs solar cell grown on GaAs substrate (green). High dislocation density degraded the carrier collection in the GaAs base, as can be interpreted from the QE response from 700 - 900 nm. The impact is less severe for the low wavelength regime (<650 nm) likely due to two reasons: (1) high-dislocation density doesn't drastically impact the carrier collection in the thin GaAs emitter, (2) While growing the cell structure, GaAs emitter is grown after growing a 2 µm thick GaAs base, therefore the additional thickness and thermal budget help annihilate dislocations and restrict their propagation in the

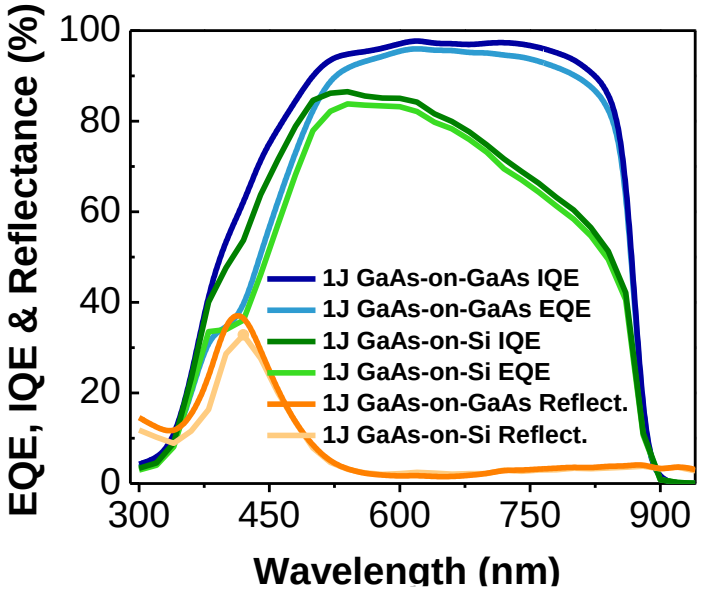

Fig. 6 Internal quantum efficiency (IQE), external quantum efficiency (EQE), and reflectance plots for 1J GaAs solar cell directly grown on Si substrate (blue) using a 2µm GaAs buffer versus 1J GaAs solar cell grown on GaAs substrate (green). High dislocation density degraded the carrier collection in the GaAs base.

direction of the growth, as evident from the cross-sectional TEM micrograph of **Fig. 1.** Further improvement in the QE response for the base region could be achieved by – (i) minimizing dislocation density propagation from the buffer layers into the active cell, and (ii) reducing the base thickness to allow better carrier-collection with the trade-off in reducing the absorption volume. Utilizing multiple periods of strained-layer super-lattice (SLs) have been once successful path to reduce the threading dislocation density [**2**], but the epitaxial growth is very challenging and not the ideal volume production route. Thus, novel techniques employing single strained layer (SL) such as InGaAs [**3**] and GaAsSb, with small percentage of In or Sb, would be promising to bend the dislocation due to the relaxation of misfit strain associated with the different lattice constants. The GaAsSb path could further help minimize dislocation density since Sb would act as a surfactant and help glide dislocation density.

5.4 Light and Dark I-V Characteristics

Light I-V measurement provides a direct tool for evaluating the sunlight to power conversion efficiency of a solar cell. Furthermore, the impact of series and shunt resistance could also be gauged into by I-V measurement analysis. On the other hand, dark I-V measurements are important as they help provide insight into the series and shunt resistance of the device and could help identify process induced shunt mechanisms (such as metal deposition providing a shunt path due to incorrect alignment across the mesa edge, defects and dislocations in the epitaxial layers etc.). Furthermore, we can extract the diode parameters such as the reverse saturation current (I_o), which is strongly dependent on the temperature; and ideality factor (n), which provides insight about various radiative & non-radiative recombination mechanisms. The I-V measurements were performed on Oriel SOL 2A 150W solar simulator equipped with AM1.5g filter. A calibrated Si reference solar cell was utilized to adjust the I-V station probing height to calibrate for precise 1-sun measurement. Important equations utilized during this analysis are highlighted below:

$$I_o = qA\left(\sqrt{\frac{D_P}{\tau_P}}.\frac{n_i^2}{N_D} + \sqrt{\frac{D_n}{\tau_n}}.\frac{n_i^2}{N_A}\right) \quad (6)$$

$$n_i^2 \propto T^3.\exp\left(\frac{-E_g}{kT}\right) \quad (7)$$

$$V_{oc} = \frac{nkT}{q} ln\left(\frac{I_{sc}}{I_0} + 1\right) \quad (8)$$

where n_i is the intrinsic carrier concentration, D_P and D_N are the diffusion coefficients, and N_A and N_D are doping concentrations. **Fig. 7** shows the dark I-V characteristic of 1J GaAs solar cell directly grown on Si

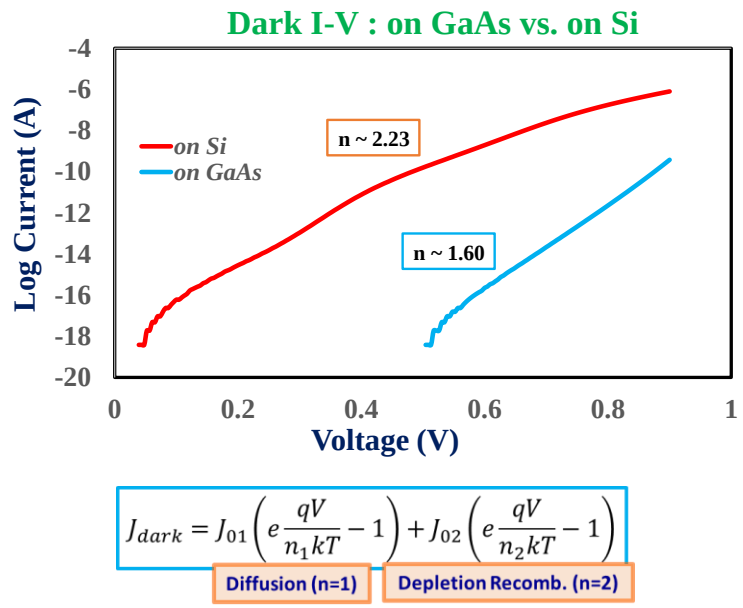

Fig. 7 Dark I-V characteristic of 1J GaAs solar cell directly grown on Si substrate (in red) using a 2µm GaAs buffer versus 1J GaAs solar cell grown on GaAs substrate (in blue). High dislocation density for "GaAs-on-Si" solar cell resulted in higher dark current due to increased recombination.

substrate (in red) using a 2µm GaAs buffer versus 1J GaAs solar cell grown on GaAs substrate (in blue). The extracted high value of the ideality factor is indicative of n=2 depletion region recombination process dominating over n=1 diffusion limited recombination process. As a result, much higher dark current was

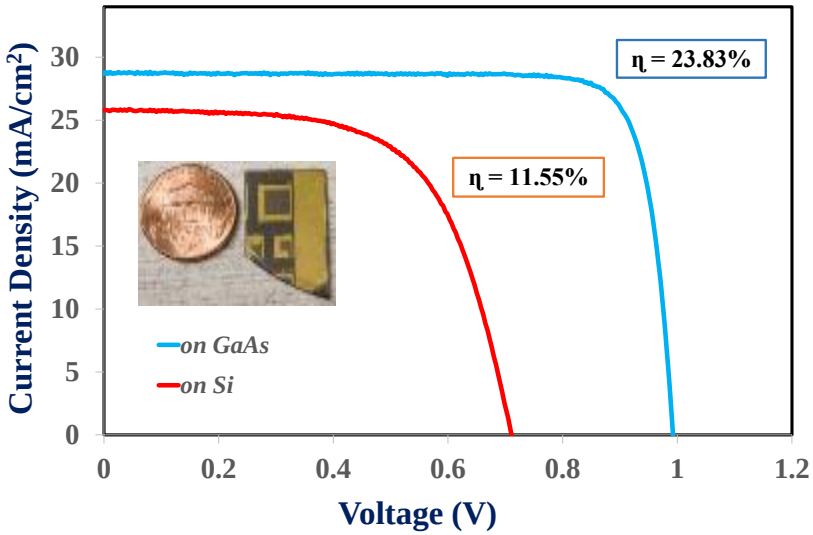

Fig. 8 Light J-V characteristics of 1J GaAs solar cell directly grown on Si (red) using a 2 µm GaAs buffer versus grown on GaAs substrate (blue) under AM1.5g spectrum (1000 W/m^2) for a cell area of 0.2 x 0.2 cm^2. High dislocation density impacts the V_{oc} drastically and limits the "GaAs-on-Si" cell performance.

TABLE I

Performance comparison of 1J GaAs solar cell (grown on GaAs vs. on Si substrate)

	On GaAs	on Si
V_{oc} [V]	0.99	0.71
J_{sc} [mA/cm^{-2}]	28.74	25.80
FF [%]	83.61	63.01
η [%]	**23.83**	**11.55**

measured for the "GaAs-on-Si" solar cell attributed to the high dislocation density, likely to be the main contributor to the recombination.

A direct consequence of the higher dark current for the 1J GaAs-on-Si solar cell can be seen in the light I-V characteristic. **Fig. 8** shows the light J-V characteristics of 1J GaAs solar cell directly grown on Si (red) using a 2µm GaAs buffer versus grown on GaAs substrate (blue) under AM1.5g spectrum (1000 W/m^2). The fabricated cells were of different size – 0.2 x 0.2 cm^2 and 0.5 x 0.5 cm^2. 1J GaAs-on-Si demonstrated an efficiency of 11.55% (cell area: 0.2 x 0.2 cm^2), while lattice-matched 1J GaAs solar cell on GaAs substrate (control sample) demonstrated a 23.55% under AM1.5g spectrum. The high dislocation density which degraded the carrier collection in the GaAs base as shown in the QE plot of **Fig. 6** was responsible for the degraded performance of the 1J GaAs-on-Si solar cell. The open-circuit voltage was found to be more impacted by dislocations than short-circuit current density, a finding inconsistent with our dislocation assisted solar cell modeling. The performance parameters are summarized in **Table 1** and our 1J GaAs-on-Si solar cell results are compared with 1J GaAs-on-Si solar cell results from Spire Corporation [**4**] in **Table II**, (both utilize same GaAs buffer thickness) suggesting that V_{oc} is strongly goverened by the dislocation

TABLE II

Performance comparison of 1J GaAs solar cell on Si (Spire Corporation vs. VT)

	Spire [4]	VT
V_{oc} [V]	0.69	0.71
J_{sc} [mA/cm^{-2}]	14.8	25.80
FF [%]	67.2	63.01
η [%]	**7**	**11.55**

density. Thus, the high dislocation density was identified as the key factor limiting the performance of "GaAs-on-Si" solar cell.

5.5 Role of Si Substrate Offcut

The growth for "GaAs-on-Si" solar cells was also performed on 3-inch diameter, arsenic-doped (resistivity-> 0.004 ohm-cm) Si (100) substrates with a 6˚ off-cut towards <110> (see **Section 3.2.1**). **Fig. 9** shows the light J-V characteristics of 1J GaAs solar cell directly grown on Si substrates with 4˚ (ADSEL0127) and 6˚ (ADSEL0144) offcut with a same buffer thickness of 2 µm. The J-V characteristic in **Fig. 9** are for cells processed only till level-III front metal lithography and prior to cap-etch and ARC depositions (hence the term PRE). Thus, lower J_{sc} was expected in these partially processed cells due to light absorption in the GaAs cap layer and due to the absence of ARC layer. The only other difference in the cell structure of these two samples was in the GaAs base thickness (ADSEL0127 -2 µm and ADSEL0144 -1.5 µm). Typically, for a 1J GaAs solar cell the J_{sc} saturates beyond a cell thickess of ~ 0.5 µm. It can be clearly seen that the FF and V_{oc} improved for ADSEL0144 likely due to reduction in dislocation density attributed to combination of greater Si substrate offcut, conducting substrate and thinner base.

To confirm the consistency in the improved V_{oc}, we also analyzed the performance of large area 1J GaAs solar cells grown on Si substrate. The fabricated cells were of size – 0.2 x 0.2 cm^2 (127-S and 144-S) and

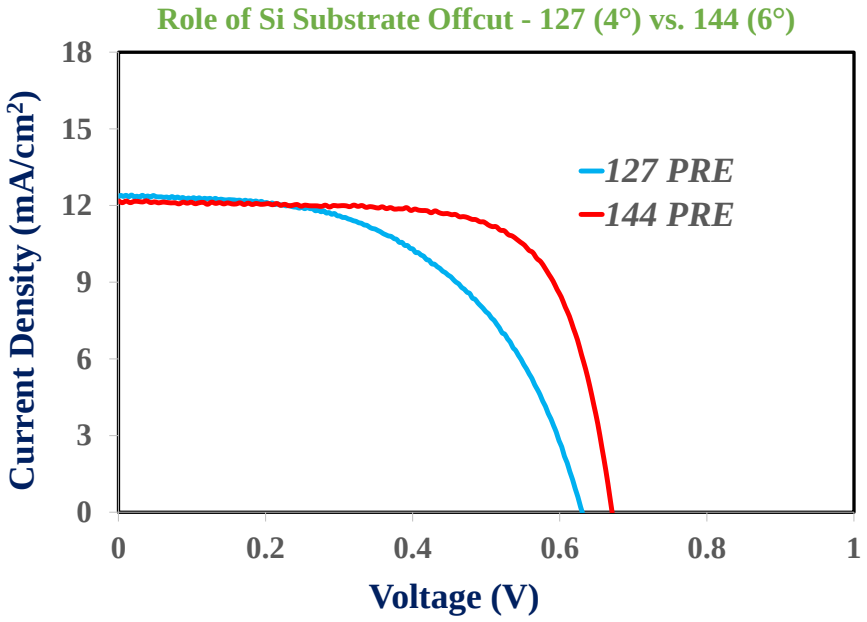

Fig. 9 Light J-V characteristics of 1J GaAs solar cell directly grown on Si with 4˚ (ADSEL0127) and 6˚ (ADSEL0144) offcut prior to GaAs cap-etch and ARC deposition. The buffer thickness was held constant at 2 µm and the cell area was 0.2 x 0.2 cm^2.

TABLE III

Dependance of 1J GaAs-on-Si Solar Cell Performance on Area

	127-S	144-S	144-B
V_{oc} [V]	0.63	0.67	0.669
J_{sc} [mA/cm^{-2}]	12.36	12.15	11.13
FF [%]	53.46	70.90	67.01
η [%]	**4.16**	**5.78**	**4.99**

0.5 x 0.5 cm^2 (144-B) processed together on the same wafer piece. **Table III** shows the dependence of 1J GaAs-on-Si solar cell performance on the area for sample ADSEL0127 (4˚) and ADSEL0144 (6˚) prior to GaAs cap-etch and ARC deposition. It can be clearly seen that there is almost no degradation in V_{oc} (144-B) for large area 1J GaAs-on-Si solar cell in comparision to smaller area cell (144-S). The reduction in J_{sc} and FF are likely due to increased series resistance contribution from the lateral conduction layer for the larger area cells. Small area solar cell 144-S was also analyzed after the GaAs cap-etch and ARC deposition. **Fig. 10** shows the light J-V characteristics of 144-S, demonstrating an efficiency of 12.77% under AM1.5g spectrum, the highest 1J GaAs-on-Si solar cell efficiency achieved during this PhD study. Further optimization of the growth condition and utilization of novel buffer schemes would be critical to minimize the dislocation density and improve the electrical performance of GaAs-on-Si solar cells.

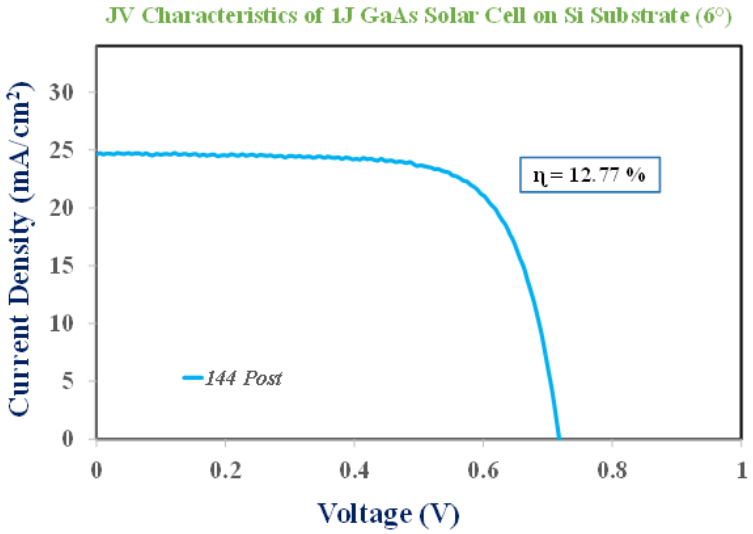

Fig. 10 Light J-V characteristics of 1J GaAs solar cell directly grown on Si with 6˚ (ADSEL0144) offcut after GaAs cap-etch and ARC deposition. The cell area was 0.2 x 0.2 cm^2.

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Chapter 6

Towards "Ge-on-Si" Virtual Substrates via Direct Epitaxy

N. Jain, et. al., "Towards a Monolithic, an All-Epitaxial and a Reusable-Substrate Design for III-V-on-Si Solar Cells," in *Proc. 42nd IEEE Photovoltaic Spec. Conf.*, 2015.

In this chapter, we present our preliminary results on a very promising alternate path for integrating III-V solar cells on Si substrate by utilizing high-quality and thin Ge layers grown directly on Si substrate. The goal is to leverage the virtual "Ge-on-Si" substrates for subsequent lattice-matched growth of GaAs to realize III-V-on-Si multijunction solar cells. Modeled 1-sun performance of 3J InGaP/GaAs/Si-Ge solar cells and the excellent material quality achieved for epitaxial Ge directly grown on Si substrate lays a strong foundation towards realizing virtual "Ge-on-Si" template, indicating a promising future for monolithically integrated, low-cost and high-efficiency III-V-on-Si photovoltaics.

6.1 Motivation and Approach

Integration of III-V multijunction solar cells on Si substrate can address the future levelized cost of energy by unifying the high-efficiency merits of III-V materials with the low-cost and abundance of Si. Achieving high-quality GaAs epitaxial layers on Si substrate is highly desirable for growing subsequent subcells to realize III-V multijunction solar cells. The 4% lattice-mismatch, the polar on non-polar material epitaxy and the thermal mismatch makes it really challenging to grow high-quality GaAs on Si substrate. While the efficiency of mainstream Si based solar cells has almost saturated at ~25%, III-V multijunction solar cells have steadily shown performance improvement, reaching a recent record efficiency of 46%. Integration of such III-V multijunction cells with Si can address the future levelized cost of energy by unifying the high-efficiency merits of III-V materials with low-cost and abundance of Si. Till date, efficiency of 3J III-V/Si tandem solar cells have merely exceed 25% even after employing non-monolithic techniques such as wafer-bonding [**1**] and areal current-matching [**2**]. Challenges associated with material growth, reliability and reproducibility have limited the success of III-V-on-Si technology. Thus, novel approaches are sought for realizing the potential of III-V-on-Si multijunction solar cells.

An alternate to this approach is to grow epitaxial Ge on Si substrate and create virtual "Ge-on-Si" substrate for subsequent lattice-matched GaAs epitaxy. Significant research has been devoted towards a similar approach but by employing graded Si_xGe_{1-x} buffers, however they utilize very thick (~10 µm) buffers [**3-**

5]. Single-junction GaAs solar cell with efficiency of 18.1% under AM1.5g spectrum have been demonstrated using the graded Si_xGe_{1-x} thick buffer approach [**3**]. However, such thick buffers are very time consuming to grow, they typically require growth interruption for chemical mechanical polishing step to smoothen out the surface, add significantly to the bill of materials, elevate the issue of thermal mismatch and furthermore eliminates the scope of leveraging the Si substrate as an active subcell due to the smaller bandgap of SiGe. Here, we proposed a novel approach to integrated GaAs on Si by utilizing direct epitaxial Ge-on-Si. Very thin epitaxial Ge layer could allow the option to utilize the bottom Si substrate as an active subcell. We investigate a Si-compatible monolithically integrated 3J InGaP/GaAs/Ge-Si solar cell design with a hybrid Ge-Si bottom cell. The intermediate Ge buffer layer forms the emitter for the bottom hybrid subcell and allows the de-coupling of key challenges for subsequent GaAs-on-Si growth: polar on non-polar epitaxy and lattice-mismatch epitaxy, thus allowing an all-epitaxial and diffusion-free process. High-quality virtual Ge-on-Si template would also find be very promising applications for transistors [**6-8**], LEDs [**9**], photodetectors [**10-12**] and solar cells [**13**]. Prior simulation studies have shown that efficiencies approaching 28% under AM 1.5g spectrum could be achieved using Si-Ge tandem solar cells [**13**]. For transistor application, III-V epitaxy on Ge-on-Si template could allow to realize high electron mobility III-V n-channel and high hole mobility p-channel Ge transistor heterogeneously integrated on Si substrate for high-speed and low-power CMOS applications [**8**]. Several groups are investigating the growth of III-V compounds on Ge-on-Si substrates **[8, 14-16**]. Unlike some of the prior reports on Ge integration on Si substrate using patterned and selective area epitaxy [**17, 18**], we focus on developing a non-selective area Ge-on-Si epitaxial process with a key goal of realizing thin epitaxial Ge layers allowing light penetration to the bottom Si substrate cell. Researchers have investigated several techniques for growing Ge on Si substrate including metalorganic chemical vapor deposition [**19**], ultra-high vacuum chemical vapor deposition (UHV-CVD) [**18, 20, 21**], rapid thermal chemical vapor deposition (RTCVD) [**22**], reduced pressure chemical vapor deposition (RPCVD) [**23, 24**], low-energy plasma-enhanced chemical vapor deposition (LEPECVD) [**12**], DC magnetron sputtering [**25**] and molecular beam epitaxy (MBE) **[9-11, 16, 26-28**]. However, most of these processes are CVD based and require relatively higher growth temperature and typically involving gaseous precursors containing hydrogen and carbon which could make the surface reactions relatively difficult to control. High-quality epitaxial Ge-on-Si was realized using gas-source MBE, but required precise admixture tuning of the gaseous precursor [**27**]. Solid-source MBE approach could not only allow ultra-low growth rates but also beam of high purity evaporated germanium source (unlike gaseous precursors) providing a better control over the substrate temperature and initial growth conditions. Thus, we focus our efforts on solid-source MBE for direct epitaxial Ge growth on Si substrate. Most of the approaches for direct epitaxial growth of Ge on Si using MBE utilize a very high intermediate annealing temperature (>800˚C) [**9, 10, 16**], a high growth temperature (>500˚C) [**26**] or would employ very thick

epitaxial Ge layers on Si [**16**]. A low-temperature process (< 600˚C) for Ge-on-Si could be extremely beneficial for Si-compatible CMOS applications. Additionally, a low-temperature process could also minimize the thermal mismatch induced tensile strain in epitaxial Ge, allowing almost fully-relaxed epitaxial Ge layers on Si substrate. Our goal is to achieve a high-quality, non-selective area, ultra-thin (< 200 nm) epitaxial Ge-on-Si virtual substrates under low thermal budget (< 600˚C). Using comprehensive simulation, we propose the preferred polarity for Ge-on-Si templates to realize III-V-on-Si multijunction solar cells and predict their ideal performance. Furthermore, using a combination of experimental material characterization techniques, we gauge the crystalline quality, surface roughness and inter-diffusion and transport properties for epitaxially grown direct Ge-on-Si samples.

Successful demonstration of virtual "Ge-on-Si" template could significantly reduce the cost per watt attributed to the large area and low cost of Si substrate. Interestingly, utilizing Ge intermediate layer de-couples two critical challenges for GaAs-on-Si growth: (i) polar on non-polar epitaxy and (ii) lattice-mismatch growth. Typically, Si subcell limits the current in 3J InGaP/GaAs//Si cell [**29, 30**], however that is not the case in 3J InGaP/GaAs/Ge-Si solar cell. Owing to a small bandgap, Ge layer absorbs a wide spectrum of the incident sunlight and therefore the hybrid Ge-Si subcell does not limit the current. The Ge intermediate layer approach for III-V-on-Si integration could be utilized (i) to create virtual "Ge-on-Si" template for subsequent GaAs growth (could involve active Ge subcell), (ii) solely as an ultra-thin buffer layer for connecting III-V cells to an active Si bottom subcell, and (ii) as the emitter layer for bottom Si base, forming a hybrid Ge-Si subcell. Utilizing a Si homojunction cell beneath the Ge buffer layer would likely require a diffusion process and a thicker Si substrate for current-matching in comparison to the hybrid

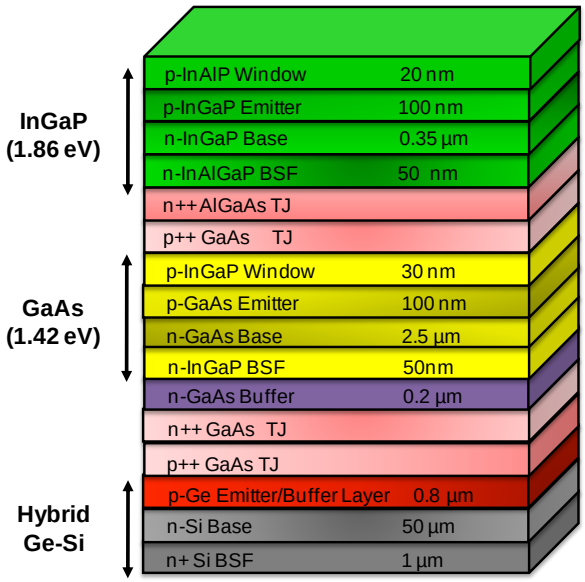

Fig. 1 Schematic depiction of 3J InGaP/GaAs/Ge-Si solar cell utilizing a hybrid Ge-Si bottom subcell.

Ge-Si approach. Furthermore, to allow sufficient light penetration to active Si subcell, extremely thin Ge buffer would be essential, rendering the subsequent GaAs growth very challenging. Thus, we focus on the design, modeling and epitaxial growth for hybrid Ge-Si bottom subcell, wherein the epitaxial Ge layer serves as a uniformly doped emitter for bottom subcell. This approach precludes the need for diffused Si junction, allowing an in-situ and an all-epitaxial process for subsequent III-V growth requiring very thin Si layers (< 60µm). Such 3J cells with very thin Si would also be very promising for CPV applications and could further benefit from additional cost savings by leveraging substrate re-use schemes utilizing amorphous Si (a-Si) as a release layer and seed layer for subsequent Si epitaxy [**31**].

6.2 Modeling of 3J InGaP/GaAs/Ge-Si Solar Cells

The numerical simulation of the proposed 3J InGaP/GaAs/Ge-Si solar cell structure and the band-alignment simulations were performed under AM1.5g spectrum using APSYS software and schematic of the proposed 3J solar cell structure which utilizes a hybrid Ge-Si bottom subcell is shown in **Fig. 1**. An ideal anti-reflective coating design was assumed for modeling. Most of the light absorption for bottom hybrid subcell occurs in the Ge emitter, thus adjusting the thickness of Ge layer allows for easy current-matching, while the direct Ge-on-Si virtual substrate provides template for subsequent GaAs growth. Typically, Si subcell limits the current in 3J InGaP/GaAs//Si cell [**29, 30**], however in 3J InGaP/GaAs/Ge-Si solar cell, middle GaAs subcell was found to be the current-limiting one. Since, V_{oc} is directly related to the bandgap, the V_{oc} from the hybrid Ge-Si subcell was found to be intermediate between that of Si and Ge homojunction cells. However, as mentioned the key advantage lies in the ability to utilize much lesser material and integration

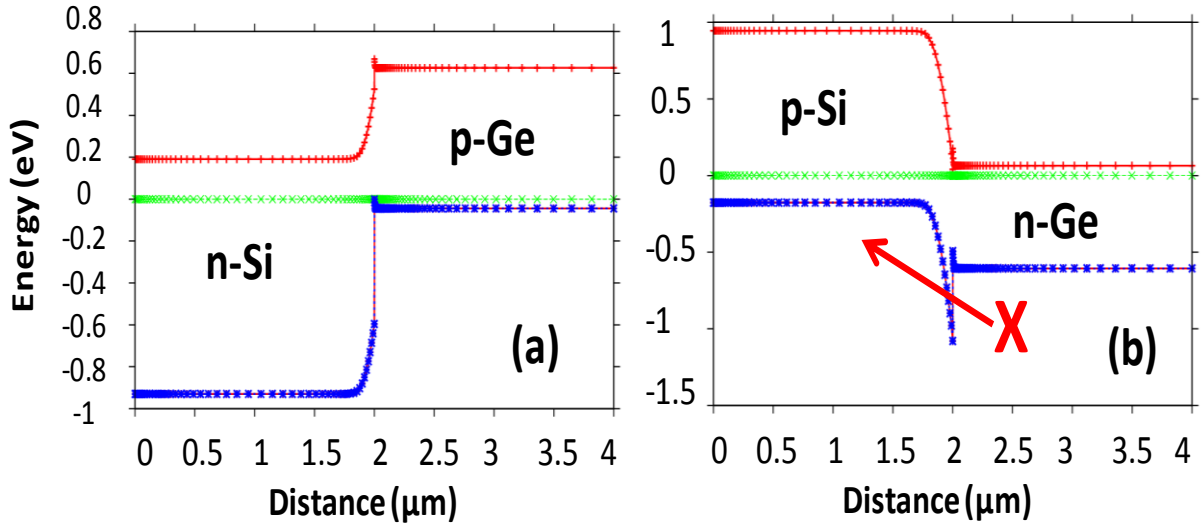

Fig. 2 Band-alignment at Ge/Si heterointerface: (a) p-Ge/n-Si, and (b) n-Ge/p-Si, indicating hole flow is restricted for case (b).

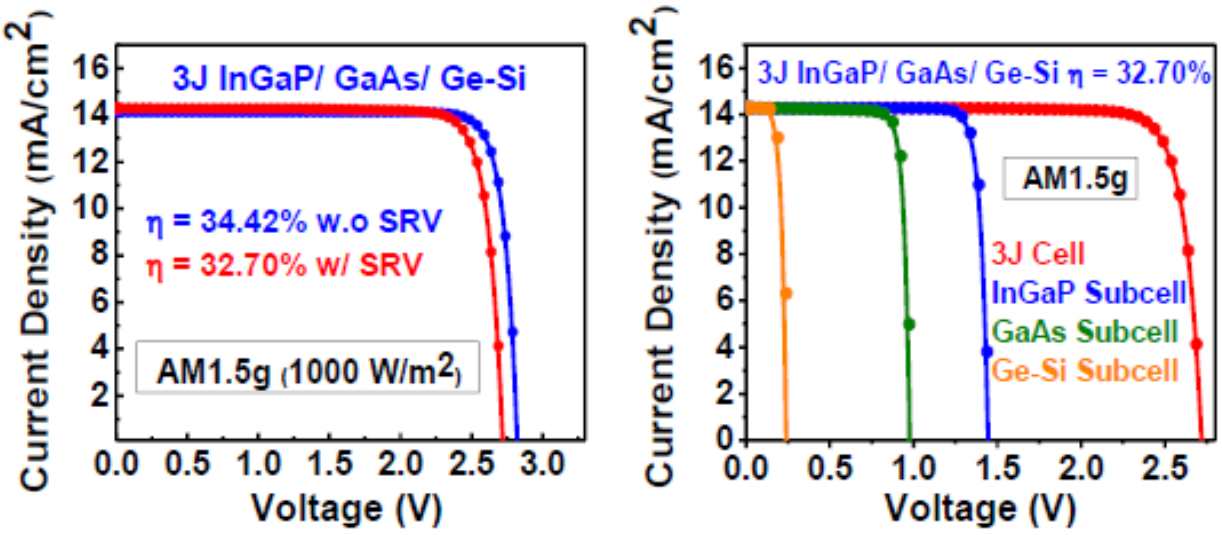

Fig. 3 Current-matched JV characteristic of 3J InGaP/GaAs/Ge-Si solar cells (a) with and without taking into account SRVs, (b) Current-matched JV characteristics for 3J InGaP/GaAs/Ge-Si and individual subcell staking into account SRV under AM1.5g, 1-sun.

through epitaxial Ge layer, allowing a lattice-matched platform for subsequent GaAs growth. For deciding the polarity of Ge and Si for realizing an active hybrid Ge-Si bottom subcell, we carried our band-alignment simulation at the Ge-Si heterointerface. **Fig. 2** shows the band-alignment at Ge/Si heterointerface for (a) p-Ge/n-Si heterostructure, and for (b) n-Ge/p-Si heterostructure. It is clear from these band diagrams that the flow of photo-generated holes in Ge is restricted into the p-side of the junction, as shown in **Fig. 2 (b).** Thus, comprehensive band-alignment assessment revealed the necessity of utilizing p-Ge with n-Si polarity to allow unrestricted carrier flow to enable an active bottom Si subcell. These band-alignment results are consisted with prior analysis for Ge-Si photodetectors [**12**].

Fig. 3 shows the current-matched I-V characteristic of 3J InGaP/GaAs/Ge-Si solar cell demonstrating an efficiency of 32.70% and 34.42%, respectively, with and without taking into account the surface recombination velocities. As can be seen from **Fig. 1**, only 50 μm thick Si was required with a 0.8 μm thick Ge emitter for current-matching. For Ge emitter thickness greater than 0.8 μm, Si base with ~ 10 μm thickness would be sufficient for current-matching. Thus, intermediate Ge buffer layer with thickness ≥ 0.8 μm would be ideal to minimize the Si base thickness, while at the same providing sufficient thickness for accommodating the dislocations due Ge/Si mismatch. Such cells utilizing thin Si could entirely be grown epitaxially and allow to release the 3J cell from the Si substrate using an a-Si release layer [**31**].

6.3 MBE Growth of Direct Ge-on-Si

The epitaxial Ge layers were grown directly on (100) Si substrate with 6° offcut towards the <110> direction in a dual-chamber molecular beam epitaxy (MBE) cluster tool. One of the chambers is solely dedicated for Ge epitaxy and is connected to a separate MBE chamber for III-V epitaxy via an *in-situ* ultra-high vacuum transfer chamber. This unique growth capability enables superior Ge epilayer quality with precise thickness control and minimal cross-contamination. The Si substrates were immediately loaded into the load lock of MBE chamber after RCA cleaning. Silicon oxide desorption was performed in the absence of arsenic over pressure at ~950°C in III-V growth chamber and was monitored in-situ using reflection high-energy electron diffraction (RHEED). The substrate was cooled to 150°C and then transferred via an ultra-high vacuum transfer chamber to the Ge MBE chamber. Three direct epitaxial Ge samples were grown on (100)Si substrates: (1) 1-step low-temperature (LT) 250°C epitaxial Ge (Sample A), (ii) 1-step high-temperature (HT) 400°C epitaxial Ge (Sample B), and (iii) two-step LT/HT epitaxial Ge ~ 135 nm thick (Sample C). A growth rate of ~0.025μm per hour was utilized for Ge epitaxy and following the Ge growth, the sample was slowly cooled down to prevent any thermal cracking.

6.4 Structural and Material Characterization

Comprehensive material characterization studies were performed to evaluate the quality of direct epitaxial Ge grown on Si in terms of crystalline quality, residual strain due to thermal mismatch, surface roughness, dislocations and defects formation, atomic inter-diffusion and electrical transport properties.

6.4.1 Surface Morphology – AFM

The surface morphology and roughness was investigated using atomic force microscope (AFM) in Scan Asyst Mode on Bruker Dimension Icon AFM system. For a scan size of 10x10 μm, the rms roughness of sample A (grown at 250°C) and sample B (grown at 400°C) were found to be 1.37 nm and 2.32 nm, respectively as shown in **Fig. 4(a)** and **(b)**, respectively. The film surface for sample grown at LT was smoother since the growth mode was more like Frank–van der Merwe (or layer-by-layer) growth. However, such a LT epitaxial Ge template would not be stable for subsequent HT GaAs growth. Hence, a combination of LT and HT growth sequence was utilized (sample C) resulting in an rms roughness of 1.91 nm, as shown in **Fig. 4(c)**.

6.4.2 Crystallinity and Strain Relaxation Properties – XRD

High-resolution triple-axis X-ray diffraction allowed insight into the crystal quality of the epitaxial Ge layer grown on Si. The XRD measurements were performed on a Panalytical X'pert Pro system. A full-width at half maxima (FWHM) of 250 arcsec for 135 nm thick Ge directly grown on Si substrate is representative

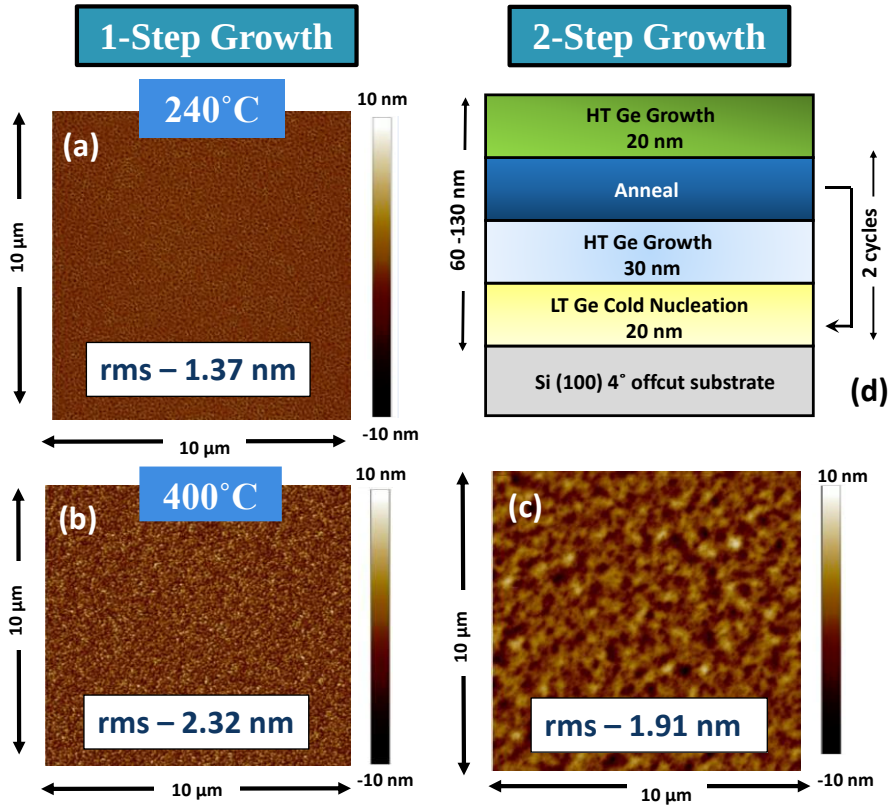

Fig. 4 AFM micrographs for (a) sample A, (b) sample B, and (c) sample C and (d) the growth sequence of sample C.

of excellent crystal quality for sample C as shown in **Fig. 5**. Furthermore, XRD measurements revealed no formation of SiGe compound, attributed to suspected diffusion during the initial growth of Ge on Si. Also,

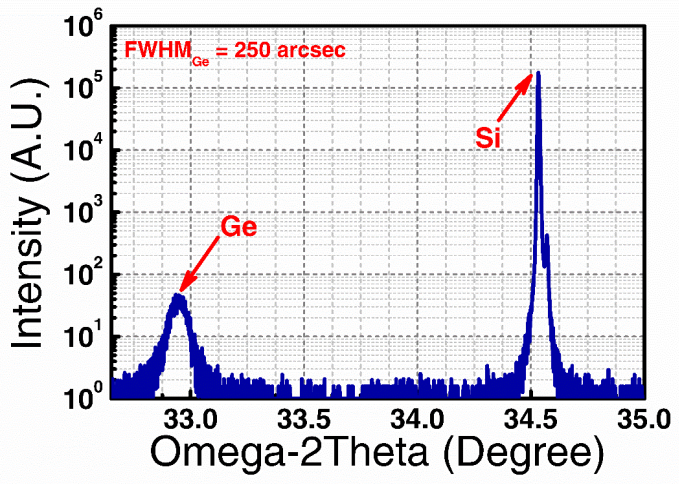

Fig. 5 XRD rocking curve for sample C, indicating an excellent FWHM~ 250 arcsec, with no formation of SiGe compound.

it is worth mentioning that, in spite of an initial low growth temperature of 250°C, a FWHM of 250 arcsec represents excellent crystalline quality of sample C.

6.4.3 Defects and Dislocations - TEM

High-resolution tunneling electron microscopy (HR-TEM) was performed on sample C using a JOEL 2100 microscope. The electron transparent foils of thin film cross-sections were prepared by using standard polishing sequence involving mechanical grinding, followed by dimpling and low temperature Ar ion beam milling. The TEM micrographs of **Fig. 6(a)** illustrates a uniform thickness of ~ 135 nm of epitaxial Ge grown directly on Si with a well-defined and an abrupt interface (sample C). The corresponding high-resolution TEM micrograph in **Fig. 6(b)** reveals good crystal quality for direct epitaxial Ge grown on Si. A few dislocations propagating into the Ge layer cancel out themselves, likely due to the thermal annealing during the growth as shown in **Fig. 6(b)**, while a few micro-twins, such as the one shown in **Fig. 6(c)** propagate towards the Ge surface. Further understanding of growth mechanism at the Ge-Si interface would be necessary to minimize such dislocation propagation.

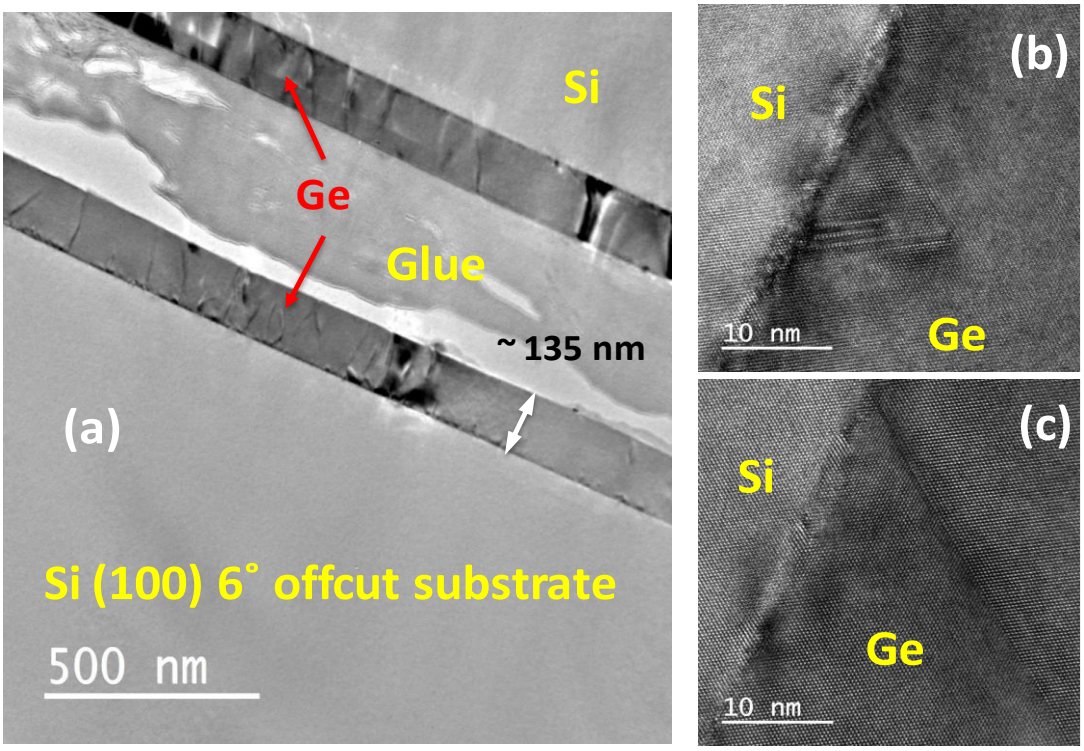

Fig. 6 (a) TEM micrographs for sample C, (b) HR-TEM micrographs indicating few dislocations cancel out themselves as shown in (b), while a few micro-twins propagate to the Ge surface, as shown in (c).

6.4.4 Raman Spectroscopy

Raman spectroscopy was performed to gauge the in-plane strain in Ge epilayers and to further evaluate the crystalline quality in relation to the peak broadening. The measurements were performed utilizing a JY Horiba LabRam HR800 system equipped with a 514.32 nm Laser Physics 100S-514 argon laser excitation source. **Fig. 7** shows the Raman spectroscopy plot for bulk Ge substrate and for directly grown epitaxial Ge-on-Si sample (sample C). The thermal expansion coefficient for Si, GaAs and Ge are - $\alpha(Si) = 2.6x10^{-6}\ ^{\circ}C^{-1}$, $\alpha(GaAs) = 5.7\ x10^{-6}\ ^{\circ}C^{-1}$ and $\alpha(Ge) = 5.9 \cdot 10\text{-}6\ ^{\circ}C^{-1}$ at 300 K, respectively. The peak located at 300.90 cm^{-1} is the Ge-Ge phonon mode from bulk Ge and the slightly shifted peak at 301.44 cm^{-1} is from the virtual Ge-on-Si substrate (sample C). The shift in wavenumber for the Ge-on-Si sample could be attributed to the minimal residual strain in the Ge epilayer induced during cooling of the sample after growth (thermal mismatch between Ge and Si). It is evident that the 135 nm epitaxial Ge grown directly on Si substrate is almost fully relaxed. It is well known that impurities, defects and dislocations could distort the lattice structure and attribute to the FWHM broadening. It is also worth noting that there is minimal change in peak broadening associated with the FWHM for Ge-on-Si sample in comparison to bulk Ge substrate, suggesting very good crystal quality of direct epitaxial Ge layer grown on Si substrate.

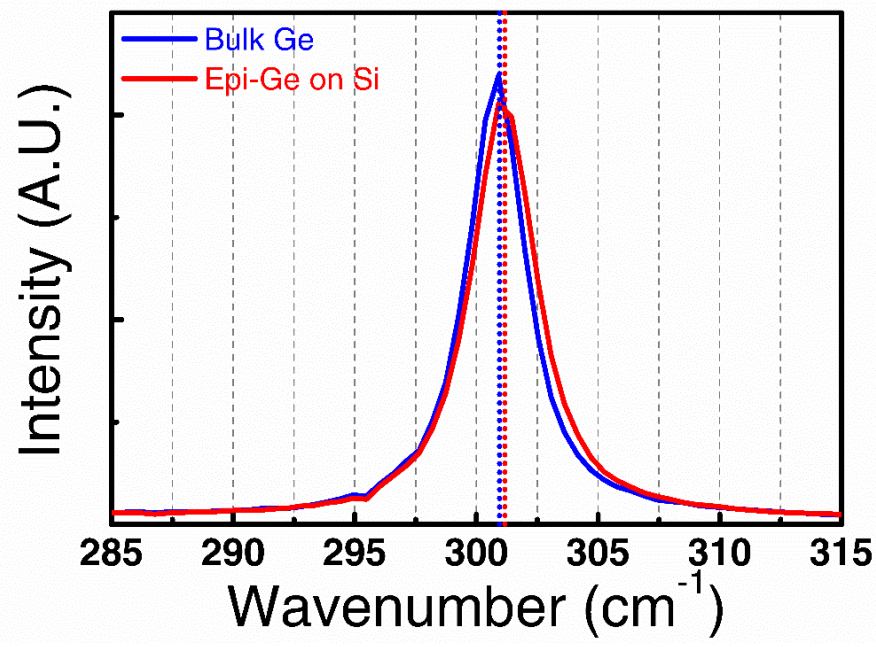

Fig. 7 Raman spectroscopic plot for bulk Ge substrate and for direct Ge grown on Si sample (sample C). Almost negligible FWHM associated peak broadening is observed for sample C in comparison to bulk Ge and almost no residual strain is induced in the direct epitaxial Ge-on-Si films.

6.4.5 Atomic Inter-diffusion - SIMS

Dynamic secondary ion mass spectrometry (D-SIMS) was used to profile the epitaxial Ge/Si interface and determine the extent of interdiffusion between layers. SIMS analysis was performed using a Cameca IMS-7f GEO utilizing a 5 kV Cs+ bombardment and molecular Cs ion detection (CsGe+ and CsSi+) in order to reduce matrix effects and minimize mass interference. Transmission electron microscopy measurements of the epitaxial Ge layer thickness were used to establish the depth scale within an estimated error margin of ~5%. The inter-diffusion between Ge and Si atoms across the heterointerface is shown in **Fig. 8**. Almost negligible inter-diffusion depth profiles of ~ 20-30 nm were observed for both Ge and Si, indicating very low level of intermixing between Si and Ge. The higher Si signal near the interface is likely attributed to the matrix transition effect. However, further experiments would be essential to probe into the reasoning for higher Si concentration towards the Ge surface.

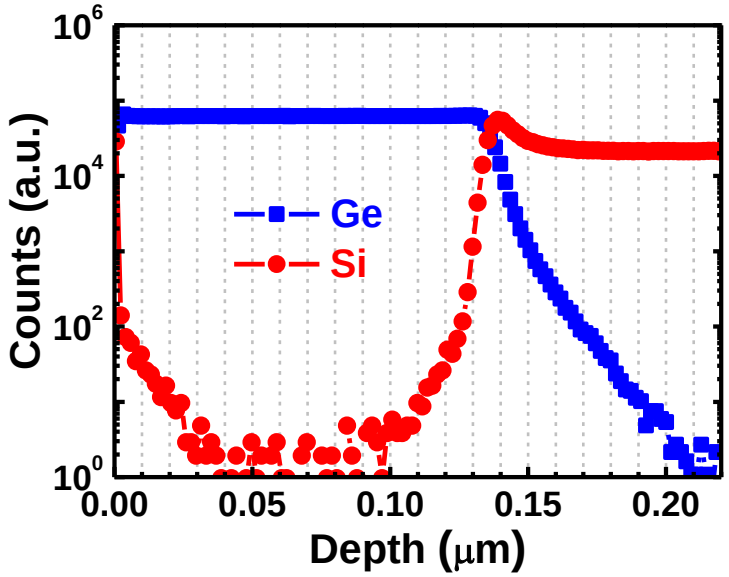

Fig. 8 Dynamic SIMS plot for sample C indicating negligible inter-diffusion at the Ge/Si heterointerface.

6.4.6 Temperature Dependent Hall Mobility

To investigate the electrical transport properties of epitaxial Ge layers directly grown on Si substrate (sample C), we measured the carrier mobility of Ge using Hall measurement by Van der Pauw method for a temperature range of 90 K to 315 K under a fixed magnetic field of 0.55T on Ecopia HMS5000 Hall measurement system. **Fig. 9** shows electron mobility and sheet carrier density measured as a function of

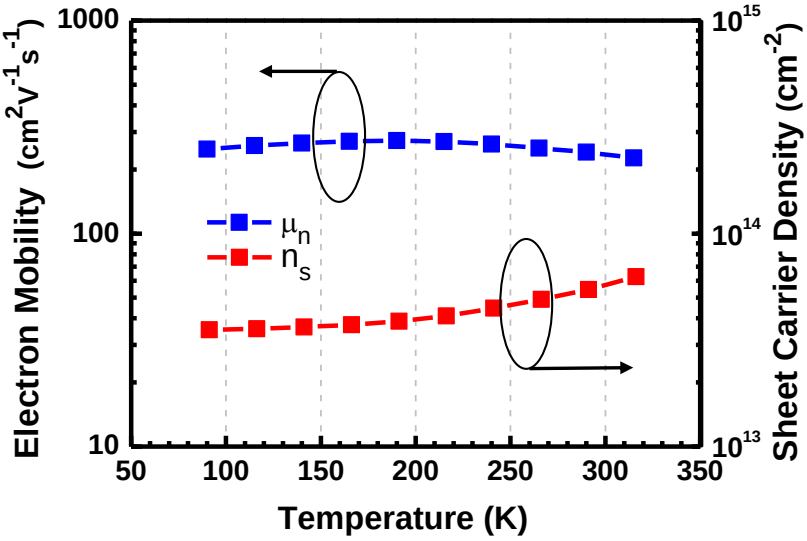

Fig. 9 Hall mobility and the sheet carrier density measured as a function of the temperature from 90 K to 315 K.

temperature. Room temperature electron mobility was measured to be 241 cm^2/Vs at 290 K at sheet carrier density, $n_s = 5.46x10^{13}$ cm^{-2}. At low temperature (90 K), the mobility was measured to be 249 cm^2/V at sheet carrier density, $n_s = 3.53x10^{13}$ cm^{-2} (donor concentration, $n_d = 4.55x10^{18}$ cm^{-3}), which suggests about a 35% carrier freeze-out in comparison to RT sheet carrier density, most likely due to the dislocations in the epitaxial Ge films grown on Si. Further reduction in dislocation density would be pivotal to improve the carrier mobility and minimize the carrier freeze-out.

6.5 Summary

We have proposed a novel design for monolithic integration of III-V multijunction solar cells on Si utilizing an intermediate Ge layer, serving both as an active layer and as a buffer layer to realize a hybrid Ge-Si bottom subcell. Comprehensive band-alignment assessment at the Ge/Si heterointerface revealed the importance of utilizing p-Ge on n-Si polarity to allow unrestricted carrier flow to enable an active bottom Si subcell. Due to high optical absorption, adjusting Ge thickness allows easy current-matching in 3J InGaP/GaAs/Ge-Si architecture, while minimizing the active Si thickness opens up avenues for releasing the bulk substrate for multiple reuses. Modeled 1-sun current-matched efficiency of 34.42% is demonstrated for an ideal 3J InGaP/GaAs/Ge-Si solar cell under AM1.5g, while a more realistic efficiency of 32.70% is expected when surface recombination is taken into account. Efficiency of such 3J solar cells under concentrated sunlight is expected to be over 40%, indicating a promising future for low-cost and high-efficiency III-V-on-Si photovoltaics. We also demonstrated heterogeneous integration of high-quality, and

thin epitaxial Ge directly grown on Si substrate using molecular beam epitaxy. Fig. 10 shows optical image of direct Ge-on-Si surface quality. Milky white surface was observed during our initial Ge-on-Si runs prior optimization (left-image). By employing a two-step growth scheme (LT/HT growth) in addition to an in-situ thermal annealing step, the surface quality improved drastically (right image). High-resolution TEM confirmed a sharp Ge/Si heterointerface with only few defects propagating towards the Ge surface. SIMS analysis revealed almost negligible inter-diffusion between the Ge and Si atoms, while XRD confirmed excellent crystal quality of 135 nm thin Ge directly grown on Si. Raman spectroscopy confirmed excellent crystalline quality and almost fully-relaxed nature of direct epitaxial Ge films on Si. RMS surface roughness as low as 1.37 nm were demonstrated for epitaxial Ge directly grown on Si, suggesting a promising step towards the realization of virtual "Ge-on-Si" substrates for monolithically integrated, low-cost and high-efficiency III-V-on-Si photovoltaics.

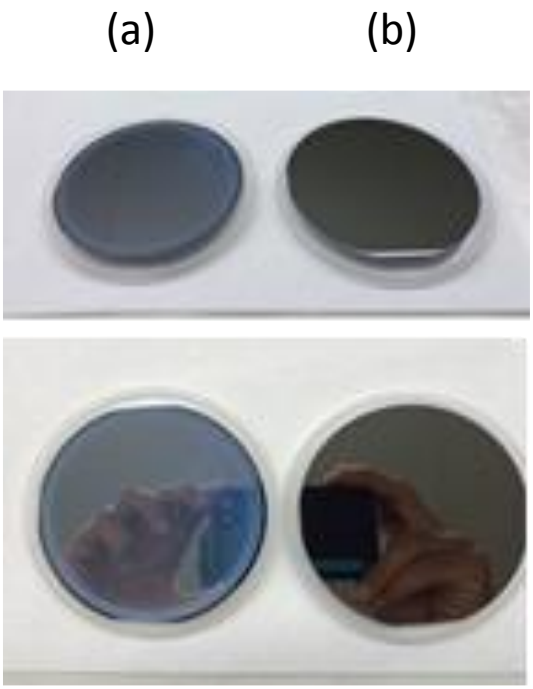

Fig. 10 Optical image of direct Ge-on-Si surface. **(a)** Initial Ge-on-Si run prior optimization, **(b)** current process-of-record for direct Ge-on-Si growth utilizing a sequence of LT/HT growth.

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Chapter 7

Conclusions & Future Outlook

Publication

N. Jain and M. K. Hudait (Invited Review), "III-V Multijunction Solar Cell Integration with Silicon: Present Status, Challenges & Future Outlook", *Energy Harvesting and Systems*, 1 (3-4), pp. 121-145, 2014.

This chapter summarizes the key findings and accomplishments of the research. Potential research directions to pursue heterogeneous integration of III-V-on-Si solar cell research and advance the-state-of-the-art are presented. Finally, we conclude with the prospects, opportunities and future outlook towards further advancing the performance of III-V-on-Si multijunction solar cells.

7.1 Key Accomplishments

1. Developed a comprehensive simulation platform for modeling & designing metamorphic III-V multi-junction solar cells on Si for 1-sun and concentrated photovoltaic operation incorporating threading dislocations. A guideline for dislocation tolerance for III-V-on-Si solar cells was presented.
2. The onset of degradation in open-circuit voltage was found to occur at a lower threading dislocation density (TDD) than in short-circuit current density, indicating that open-circuit voltage is more sensitive to TDs (simulation).
3. In the 2J InGaP/GaAs solar cells on Si substrate, the GaAs subcell was found to be the current-limiting one, while in 3J InGaP/GaAs//Si solar cells, the active Si substrate subcell was found to limit the overall current in two-terminal configuration (simulation).
4. We demonstrated that in spite of a TDD ~10^6 cm^{-2}, a theoretical conversion efficiency of greater than 29% (AM1.5g) could be achieved for lattice-mismatched 2J InGaP/GaAs solar cells on Si by realizing current-matching conditions taking into account TDD. Thus, suggesting comparable performance to lattice-matched GaAs solar cells (simulation).

5. Demonstrated that the optimization of front grid spacing and sheet resistance of the window layer were the key design parameters to extend the peak performance towards higher concentrations for CPV (simulation).
6. We demonstrated a theoretical conversion efficiency in excess of 33% at 600 suns for 2J InGaP/GaAs solar cell on Si at a TDD of 10^6 cm^{-2} and showed the importance of optimizing the cell design for a target concentration and for a specific TDD (simulation).
7. By adding an active Si subcell underneath a 2J InGaP/GaAs solar cell, an absolute 3% performance improvement to 32% (AM1.5g) could be expected at a TDD of 10^6 cm^{-2} (simulation).
8. Heterogeneous epitaxy of GaAs and Ge directly on Si substrate utilizing non-selective area epitaxy and thin buffers (2 μm for GaAs and < 150 nm for Ge).
9. Demonstrated that no unintentional Si junction is created during initial low temperature GaAs-on-Si growth during molecular beam epitaxy of GaAs directly on Si.
10. Led the entire development a four-level solar cell fabrication process for GaAs-on-Si solar cells with all front-side metal contacts to circumvent the carrier flow from dislocated buffer.
11. Successfully overcame grid-finger swim-away during lift-off and precise mesa etch slope and depth control for placement of both front-side metal contacts.
12. The high dislocation density was identified as the key factor limiting the performance of "GaAs-on-Si" solar cell, confirmed by the degradation in open-circuit voltage for 1J GaAs-on-Si solar cell.
13. 1J GaAs solar cell grown on Si substrate with a 6° offcut was found to exhibit a higher V_{oc} in comparison to a 4° offcut Si substrate.
14. A novel approach for III-V solar cell integration on Si substrate using direct and ultra-thin intermediate Ge buffer layer targeted towards high-efficiency and low-cost photovoltaic was developed.
15. We have also demonstrated a novel proof-of-concept to reduce the TDD by leveraging the misfit strain from single-strained GaAsSb layer embedded in the direct GaAs buffer on Si. This is a promising path to bend the threading dislocations horizontally instead of allowing them to propagate vertically into the active device layers.

7.2 Conclusions

The objective of this dissertation has been to systematically investigate heterogeneously integrated III-V multijunction solar cells on Si substrate. Utilizing a combination of comprehensive solar cell modeling and experimental techniques, we have been able to better understand the material properties and correlate them to improve the device performance. Key technical design considerations and optimal performance projections have been discussed for integrating metamorphic III-V multijunction solar cells on Si substrates for 1-sun and concentrated photovoltaics. Key factors limiting the "GaAs-on-Si" cell performance were

identified, and novel approaches focused on minimizing threading dislocation density were discussed. Finally, we proposed a novel epitaxial growth path utilizing high-quality and thin epitaxial Ge layers directly grown on Si substrate to create virtual "Ge-on-Si" substrate for III-V-on-Si multijunction photovoltaics. With the plummeting price of Si solar cells accompanied with the tremendous headroom available for improving the III-V solar cell efficiencies, the future prospects for successful integration of III-V solar cell technology with Si substrate looks very promising to unlock an era of next generation of high-efficiency and low-cost photovoltaics. The key findings of the dissertation are summarized below:

1. We have comprehensively investigated the impact of threading dislocations density (TDD) on the design and performance of 1J GaAs and 2J InGaP/GaAs solar cell on Si substrate for 1-sun and concentrated photovoltaic applications. Using comprehensive modeling designs coupled with realistic material parameters, we predicted the optimal performance of III-V solar cells on Si substrate taking into account the dislocation density. "GaAs-on-Si" solar cells with high dislocation density suffer from higher dark current associated with n=2 depletion region recombination. As a result, for both 1J and 2J cell configurations, the onset of degradation in V_{oc} was found to occur at a lower TDD than in J_{sc}, indicating that V_{oc} was more sensitive to TDD as compared to J_{sc}. In the 2J configuration, we found that the GaAs subcell was more sensitive to dislocations and hence limited the overall short-circuit current density in the 2J configuration. At the interfaces in the top InGaP subcell, the surface recombination velocities below 10^4 cm/s were found to have negligible impact on the 2J cell performance. Dislocation-dependent current-matching has been shown to be a powerful technique for maximizing the performance of metamorphic III-V-on-Si solar cells. The design of the 2J InGaP/GaAs cell on Si was optimized at a TDD of 10^6 cm^{-2} to achieve current-matching between the two subcells. By thinning the base thickness in the top InGaP subcell, the 2J cell efficiency increased to 29.62% under AM1.5g 1-sun condition, comparable to the record efficiency of 31.1% for 2J InGaP/GaAs solar cells on lattice-matched GaAs substrate (NREL). Thus, even in a lattice-mismatched 2J InGaP/GaAs cell on Si with TDD of 10^6 cm^{-2}, a theoretical conversion efficiency of greater than 29% at AM1.5g could be achieved by tailoring the device design, suggesting an optimistic future for direct integration of III-V solar cells on Si substrate. Once experimentally realized, this technology would offer a new paradigm for the advancement of low cost III-V solar cells and foster innovative avenues to harness the excellent energy conversion properties of III-V semiconductors with the volume manufacturability of Si.

2. We also demonstrated a design methodology oriented towards maximizing the performance of 2J InGaP/GaAs solar cell on Si for concentrated photovoltaics, incorporating threading dislocations. The current-matching condition under AM1.5d was realized at TDD varying from 10^5 to 10^7 cm^{-2}, emanating

from the mismatch between GaAs and Si substrate. The optimization of front grid spacing and sheet resistance of the window layer were the key design parameters taken into consideration for extending the peak performance towards higher concentrations. The design trade-offs between the losses due to grid shadowing and series resistance were optimized to maximize the performance under higher concentration. At a TDD of 10^6 cm^{-2}, the optimal grid finger-pitch was found to be 100 μm, demonstrating an efficiency of 32.49% at 300 suns. Increasing the window layer doping from $n=2x10^{18}$ cm^{-3} to $n=5x10^{18}$ cm^{-3} allowed to extend the peak performance to 600 suns, improving the conversion efficiency to 33.11%, a greater than absolute 3.5% performance improvement compared to 1-sun. We have demonstrated the importance of optimizing the cell design for a target concentration at a specific threading dislocation density. Our model predicts theoretical conversion efficiency in excess of 33% at 600 suns for 2J InGaP/GaAs solar cell on Si at a TDD of 10^6 cm^{-2}. The performance results are encouraging and show a promising future for integrating metamorphic III-V concentrator solar cells on Si substrate for CPV applications.

3. We have proposed a novel design for heterogeneous integration of 3J InGaP/GaAs//Si tandem solar cell with Si as an active subcell. We present key insight into the design of GaAs buffer architecture for the optimal down-selection of the buffer doping and thickness to maximize the photon flux penetration to the bottom Si subcell. Si subcell was found to be the current-limiting subcell even under ideal case scenario when no dislocation or a buffer between III-V and Si subcell was assumed. Thus, suggesting novel engineering schemes would be essential on the back-side of the Si substrate to leverage light management and reflection back into Si subcell. Rigorous numerical simulations reveal the importance of a thin GaAs buffer architecture with doping concentration less than $n=1x10^{18}$ cm^{-3} in order to allow maximum light penetration to the bottom current-limiting Si subcell. Current-matched 1-sun 3J cell efficiency of 32.13% and 36.39% was realized when no buffer layer was present between the III-V and Si subcell under AM1.5d and AM1.5g spectra, respectively. When a 0.5 μm thick GaAs buffer layer was employed, the 1-sun efficiency (AM1.5d) dropped to 29.30% at a TDD of 10^6 cm^{-2} and to 27.23% at a TDD of 10^7 cm^{-2}. Efficiency in excess 27.23% at a TDD of 10^7 cm^{-2} suggests good tolerance of dislocations in our designed structure primarily due to reduced thickness of the III-V solar cell layer needed for current-matching. Finally, a novel 3J InGaP/GaAs/Si solar cell design at a TDD of 10^6 cm^{-2} is presented with theoretical efficiency in excess of 33% at 200 suns, suggesting a promising future for integrating III-V solar cells on Si substrate for concentrated photovoltaics.

16. Utilizing a combination of comprehensive solar cell modeling and experimental techniques, we have been better able to understand the III-V-on-Si material properties and correlate them to device

performance. The key technical challenge to improve the performance of "GaAs-on-Si" solar cell is to reduce the TDD propagation into the active cell layers and the LCL, besides improving the material quality. We have demonstrated a non-selective area, high-quality and thin (2 µm) epitaxial GaAs buffer directly grown on Si substrate. Si substrate cleaning, oxide desorption and initial low-temperature GaAs nucleation were found to be among the most critical components influencing the quality of GaAs-on-Si buffer. 1J GaAs solar cells grown on Si substrate with a 6° offcut were found to exhibit a higher V_{oc} in comparision to 4° offcut Si substrate.We have also demonstrated a novel proof-of-concept to reduce the TDD by leveraging the misfit strain from single-strained GaAsSb layer embedded in the direct GaAs buffer on Si. This is a promising path to bend the threading dislocations horizontally instead of allowing them to propagate vertically into the active device layers. Such an approach of a single strained-layer is a more scalable and controllable process in comparison to multiple strained layer super-lattice structures.

4. We have successfully overcome several fabrication related process integration challenges including the issue of grid-finger swim-away during lift-off, precise mesa etch slope and depth control for placement of both front-side metal contacts. We have shown the performance benefits of utilizing both front-side metal contacts in comparison to the conventional approach of bottom contact on the back-side of the wafer. The dislocation density in the buffer and the series resistance from the bulk-substrate drastically affects the fill-factor. However no change in J_{sc} or V_{oc} was observed, suggesting that the arsenic diffusion into Si during initial GaAs growth was insufficient in creating a Si junction cell. Optical and electrical characterization of our in-house fabricated solar cells was carried out to investigate the solar cell performance. High dislocation density for the "GaAs-on-Si" solar cell degraded the carrier collection in the GaAs base, suggested by the quantum-efficiency measurement. From the dark I-V measurement, a high value of the ideality factor for "GaAs-on-Si" solar cell represented n=2 depletion region recombination process, resulting in much higher dark current attributed to the high dislocation density. Consequently, a 1J GaAs-on-Si demonstrated an efficiency of 11.55%, while lattice-matched 1J GaAs solar cell on GaAs substrate (control sample) demonstrated a 23.55% under AM1.5g spectrum. 1J GaAs solar cells grown on Si substrate with a 6° offcut were found to exhibit a higher V_{oc} in comparision to 4° offcut Si substrate. An efficiency of 12.77% was achieved for 1J GaAs solar cell directly grown on 6° offcut Si substrate, utilizing a 2 µm GaAs buffer. The open-circuit voltage was found to be more impacted by dislocations than short-circuit current density, a finding inconsistent with our dislocation assisted solar cell modeling. Thus, the high dislocation density was identified as the key factor limiting the performance of "GaAs-on-Si" solar cell.

5. We have proposed a novel approach for reducing the dislocation density in III-V-on-Si multijunction solar cells. A design for monolithic integration of III-V multijunction solar cells on Si utilizing an intermediate Ge layer, serving both as an active layer and as a buffer layer to realize a hybrid Ge-Si bottom subcell is presented. Comprehensive band-alignment assessment at the Ge/Si heterointerface revealed the importance of utilizing p-Ge on n-Si polarity to allow unrestricted carrier flow to enable an active bottom Si subcell. Due to high optical absorption, adjusting Ge thickness allows easy current-matching in 3J InGaP/GaAs/Ge-Si architecture, while minimizing the active Si thickness opens up avenues for releasing the bulk substrate for multiple reuses. Modeled 1-sun current-matched efficiency of 34.42% is demonstrated for an ideal 3J InGaP/GaAs/Ge-Si solar cell under AM1.5g, while a more realistic efficiency of 32.70% is expected when surface recombination is taken into account. Efficiency of such 3J solar cells under concentrated sunlight is expected to be over 40%, indicating a promising future for low-cost and high-efficiency III-V-on-Si photovoltaics. We also demonstrated heterogeneous integration of high-quality, and thin epitaxial Ge directly grown on Si substrate using molecular beam epitaxy. High-resolution TEM confirmed a sharp Ge/Si heterointerface with only few defects propagating towards the Ge surface. SIMS analysis revealed almost negligible inter-diffusion between the Ge and Si atoms, while XRD confirmed excellent crystal quality for the 135 nm thin Ge directly grown on Si. Raman spectroscopy confirmed high crystalline quality and almost fully-relaxed nature of direct epitaxial Ge films on Si. RMS surface roughness as low as 1.37 nm were demonstrated for epitaxial Ge directly grown on Si, suggesting a promising step towards the realization of virtual "Ge-on-Si" substrates as an alternate and promising route for monolithically integrated, low-cost and high-efficiency III-V-on-Si photovoltaics.

7.3 Prospects for Future Research

This research explores and evaluates the heterogeneous integration of III-V multijunction solar cells on Si substrate utilizing a combination of comprehensive solar cell modeling and experimental approach. Further investigations along the following prospective research directions could extend the current scope of the work to better understand the material properties and correlate them to improve the III-V-on-Si solar cell performance:

1. The key technical challenge to improve the performance of "GaAs-on-Si" solar cell is to reduce the threading dislocation density. We demonstrated the use of single-strained layer embedded in the direct GaAs buffer on Si as an interesting path to reduce the dislocation density by leveraging the misfit strain from GaAsSb layer to bending the threading dislocations horizontally instead of vertical propagation

into the active device layers. Such an approach of a single strained-layer is a more scalable and controllable process in comparison to multiple strained layer super-lattice structures. In addition, the surfactant property of "Sb" in GaAsSb is expected to aid in the dislocation glide. Further investigation and optimization of the GaAsSb ternary layer in terms of Sb composition, layer thickness, and layer position and growth conditions could be exploited to achieve substantial reduction in dislocation density. Interestingly, alternative single strained layers such an InGaAs or even GaAsP could be investigated in relation to exploiting schemes for further dislocation reduction.

2. Utilizing Si as an active junction has tremendous potential for III-V-on-Si multijunction solar cells. Si as an active subcell is likely to limit the current in conventional 3J InGaP/GaAs//Si multijunction. In this dissertation, triple-junction solar cell design with 1-sun efficiency exceeding 30% have been proposed based on III-V-on-Si solar cell technology utilizing GaAs buffer. As explored in this dissertation, one of the most critical challenges for incorporating an active Si junction involves novel schemes on the back-side of the Si substrate to enhance the short-circuit current density in the Si subcell. Additionally, utilizing large bandgap buffers such as AlGaAs or InGaP or even thinning down the GaAs buffer thickness are possible routes to increase the light penetration to the bottom Si subcell. Furthermore, would be interesting to evaluate the scope of in-situ arsenic diffusion during MBE growth in comparison to conventional Si diffusion. The findings will prove to be very valuable for closing the performance gap between lattice-mismatched III-V solar cells on Si substrate and lattice-matched III-V solar cells on GaAs substrate.

3. Our focus has been integrating GaAs solar cell on Si substrate since based on our simulation, a good quality GaAs subcell on Si substrate is the most critical component towards realizing high-efficiency multijunction solar cells. Research extending 1J cells towards multijunction solar cells would be an interesting avenue to explore, especially since based on our simulation results InGaP, the top subcell in a multijunction configuration, is expected to be less severely impacted by threading dislocations. Experimental results validating our current-matching dual-junction cell designs would be critical in providing design-to-material-to-device feedback. Experimental efficiency of dual-junction based III-V-on-Si solar cells have merely reached efficiencies in the vicinity of 20% under AM1.5g, while their predicted efficiencies are well above 30% under AM1.5g spectrum.

4. Exploring the proposed novel epitaxial route for integrating III-V multijunction solar cells utilizing ultra-thin and very high-quality direct "Ge-on-Si" virtual template has very promising prospects. In this dissertation, triple-junction solar cell design with 1-sun efficiency exceeding 30% has been proposed

based on III-V-on-Si solar cell technology utilizing Ge buffer. Although, it will be challenging to realize an active Si subcell using small bandgap Ge buffer, nonetheless virtual "Ge-on-Si" template could providing a promising platform for subsequent lattice-matched GaAs solar cell epitaxy. The direct "Ge-on-Si" growth could be further optimized by exploring combination of different growth temperatures, growth rates and annealing conditions to create virtual "Ge-on-Si" template for subsequent high-quality GaAs solar cell epitaxy.

5. The modeling frame presented in this dissertation provides a promising starting platform to extend the work towards integration 3J and beyond III-V based multijunction solar cells on Si substrate. The dislocation-dependent current-matching scheme could be explored to study metamorphic low bandgap InGaAs (1eV and 0.7eV) solar cells and better understand the role of threading dislocations on their performance. Furthermore, as new experimental data becomes available in the future for dislocation-dependent minority carrier lifetime and minority carrier mobility, the models proposed in this dissertation could be further strengthened and extended to bridge the gap between experimental and simulation results and could become an extremely valuable tool to design and predict the performance of lattice-mismatched III-V multijunction solar cell performance on Si substrate.

7.4 Scope & Future Outlook

One of the most promising near term routes for integration of III-V solar cells on Si substrate would be to create virtual "GaAs-on-Si" substrate for the subsequent growth of state-of-the-art 3J InGaP/GaAs/InGaAsNSb solar cells (which are 44% efficient under 947 suns when grown on GaAs substrate [**1**]) which are lattice-matched to GaAs as shown in **Fig. 1(a)**. Although, this approach would utilize the Si substrate as a passive template, such an approach could leverage commercially available GaAs substrate re-use techniques for additional cost reduction [**2, 3**]. However, very high quality GaAs-on-Si template would be essential which would not only require a low TDD, but also be negligibly impacted by thermal mismatch. Successful realization of such virtual GaAs-on-Si template can be very challenging and would require novel buffer architectures which might leverage a combination of existing buffer approaches, but not limited to: (i) direct GaAs growth on Si involving TCA and SLSs, (ii) direct Ge epitaxy on Si, (iii) graded GaAsP buffer, and (iv) graded SiGe buffer. Triple junction solar cells with GaInP/GaAsP/SiGe subcells on an inactive Si substrate utilizing SiGe graded buffer could also be an interesting future path to explore.

When utilizing Si substrate as an active bottom subcell for 3J designs, InGaP or AlGaAs would likely be the preferred top cell material choice, while GaAsP or GaAs would be the preferred middle cell material.

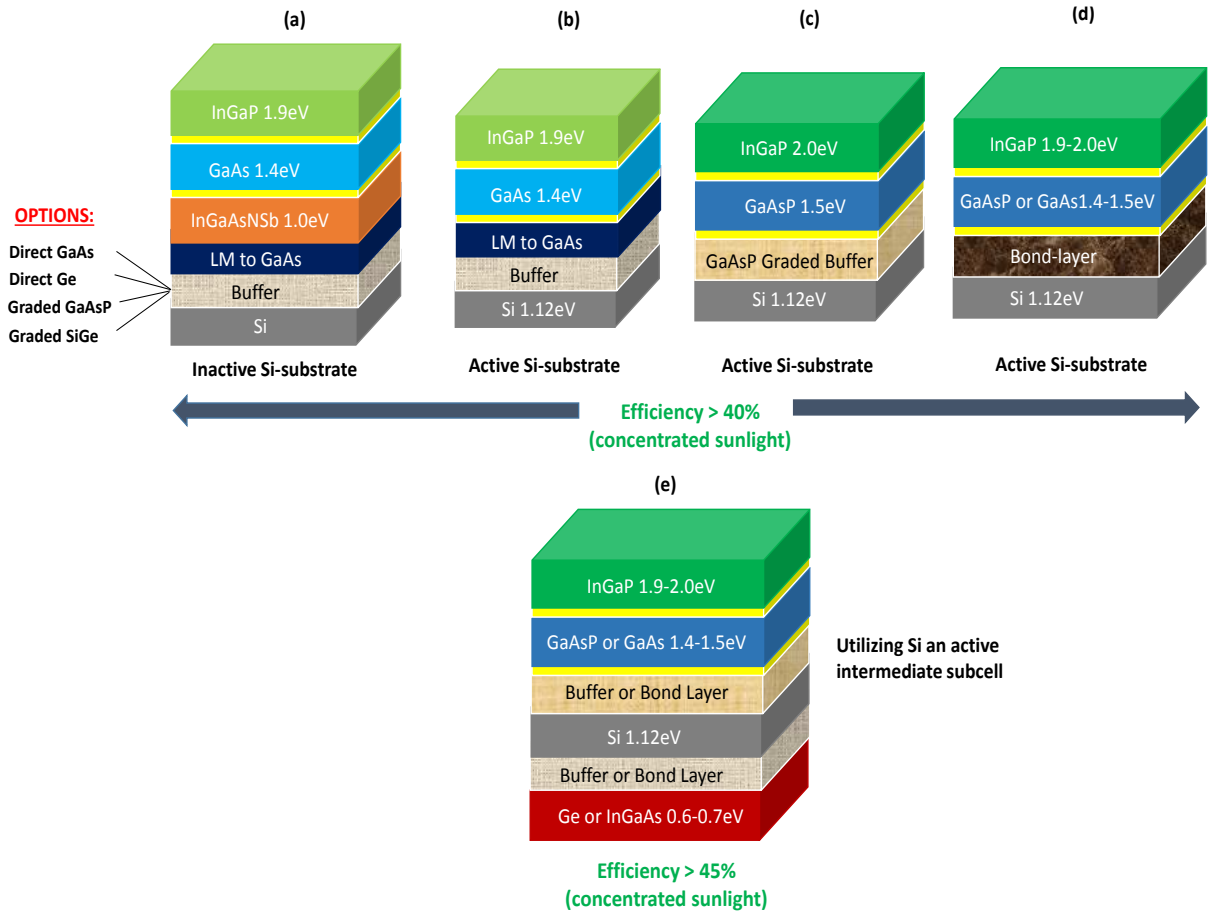

Fig. 1 Routes towards high-efficiency III-V-on-Si concentrator solar cells utilizing heteroepitaxial integration approaches are shown in (a), (b), (c) and through a combination of heteroepitaxial and mechanical stacking approaches are shown in (d) and (e). Fig. (a)-(d) represent the most likely path towards >40% efficiency under AM1.5d concentrated sunlight for 3J III-V-on-Si multijunction solar cells, while Fig. (e) represents the likely path for >45% efficiency utilizing 4J III-V-on-Si multijunction solar cells. Other possible route for high-efficiency III-V-on-Si solar cells could be based on the standard inverted metamorphic 3J or 4J cells on a GaAs-on-Si substrate (not shown in the figure) [**4**]. Used with permission from EHS, 2014.

The three most promising near-term routes for 3J III-V-on-Si solar cell with an active Si substrate include: (i) 1.9eV InGaP/1.4eV GaAs 2J solar cells epitaxially grown on a virtual GaAs-on-Si template with an active Si substrate (see **Fig. 1(b)**), (ii) more ideal bandgap combination could be realized using 2eV InGaP with 1.5eV GaAsP on Si using a metamorphic GaAsP buffer (see **Fig. 1(c)**), and (iii) mechanically-stacked or wafer bonded 2J InGaP/GaAsP solar cells onto an active bottom Si substrate (see **Fig. 1(d)**). In-order for such 3J III-V-on-Si solar cell designs to exceed 40% efficiency (under concentrated sunlight), careful attention needs to be given to dislocation and thermal-mismatch management for metamorphic materials on Si, proper tunnel-junction designs (especially for metamorphic GaAsP route), and appropriate bonding

layer with optical transparency and good electrical conductivity. Additionally, the bottom Si subcell is likely to be the current-limiting subcell in such designs and would therefore require novel backside substrate engineering to maximize the current density for successful multijunction designs. Utilizing III-V-on-Si integration approach, tandem solar cells with four junctions or more would be essential to push the efficiency beyond 45% under concentrated sunlight. If Si substrate were to be used as an active subcell, it would likely require a bottom subcell beneath the Si substrate with a bandgap of ~0.6-0.7eV (likely to be InGaAs or Ge) as shown in the **Fig. 1(e)**. Such 4J designs would likely involve a combination of metamorphic epitaxial growth and mechanical stacking.

In summary, direct integration of III-V solar cells on large diameter, cheaper and readily available Si substrate is highly desirable for increased density, low-cost, lightweight & high-efficiency photovoltaics. III-V integration on Si combines the excellent optical properties of compound semiconductors with the volume manufacturability of silicon allowing a path for significantly driving down the cell cost. III-V on Si technology is also attractive from the point of view of integration with commercially available substrate re -use techniques for additional cost savings such as the spalling [**2**] and the epitaxial lift-off techniques [**3**]. Furthermore, the direct GaAs on Si epitaxy would enable this approach to be easily extended and employed in conjunction with the current record efficient 3J solar cells utilizing dilute nitride bottom cell [**1**] as well as with the current state-of-the-art inverted metamorphic (IMM) triple junction solar cell production lines. Integration of such high-efficiency III-V multijunction solar cells on significantly cheaper and large area Si substrate has the potential to address the future LCOE roadmaps by unifying the high-efficiency merits of III-V materials with low-cost and abundance of Si. With the recent advancements in both the heteroepitaxial and mechanically stacked integration approaches and the tremendous headroom available for III-V solar cell performance improvement, efficiencies exceeding 35% and 40% under 1-sun and concentrated sunlight, respectively, seems achievable for III-V-on-Si multijunction solar cells, indicating a promising future for high-efficiency and low-cost III-V-on-Si photovoltaics. Novel, robust and scalable substrate re-usable techniques are expected to further lower the cost per watt for III-V solar cell technology.

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APPENDIX

(i) List of Publications at Virginia Tech

JOURNALS:

1. **N. Jain**, et. al., " Towards a Monolithic, an All-Epitaxial and Substrate-Reusable Design for III-V-on-Si Solar Cells," *IEEE J. Photovoltaics (in preparation, 2015).*
2. **N. Jain** and M. K. Hudait (Invited Review), "III-V Multijunction Solar Cell Integration with Silicon: Present Status, Challenges & Future Outlook", *Energy Harvesting and Systems* 1 (3-4): 121-145 (2014).
3. **N. Jain** and M. K. Hudait, "Design and Modelling of Metamorphic Dual Junction InGaP/GaAs Solar Cells on Si Substrate for Concentrated Photovoltaic Application", *IEEE J. Photovoltaics* 4: 1683-1689 (2014).
4. **N. Jain**, Y. Zhu, D. Maurya, R. Varghese, S. Priya, and M. K. Hudait,"Interfacial Band Alignment and Structural Properties of Nanoscale TiO2 High-k Gate Dielectric for Integration with Epitaxial Crystallographic Oriented Germanium", *J. Appl. Phys.* 115: 024303 (2014).
5. **N. Jain** and M. K. Hudait, "Impact of Threading Dislocations on the Design of GaAs and InGaP/GaAs Solar Cells on Si Using Finite Element Analysis", *IEEE J. Photovoltaics* 3: 528 (2013).
6. P. Goley, C. Winkler, M. Clavel, **N. Jain**, and M. K. Hudait,"Investigation of Tensile Strain Relief Mechanism in 3D Epitaxial Germanium", *Under Review* (2015).
7. M. Clavel, P. Goley, **N. Jain**, Y. Zhu, and M. K. Hudait, "Strain-Engineered Biaxial Tensile Epitaxial Germanium for High-Performance Ge/InGaAs Tunnel Field-Effect Transistors", *IEEE J. Electron Devices* Society 3: 1-10 (2015).
8. M. K. Hudait, Y. Zhu, P. Goley, M. Clavel, and **N. Jain**, "Mixed-anion GaAs1-ySby Graded Buffer Heterogeneously Integrated on Si by Molecular Beam Epitaxy", *Appl. Phys. Express* 8: 025501-025503 (2015).
9. N. Shehata, K. Meehan, M. K. Hudait, **N. Jain**, and S. Gaballah, "Study of Optical and Structural Characteristics of Ceria Nanoparticles Doped with Negative and Positive Association Lanthanide Elements", *J. Nanomaterials,* vol . 2014, 1-7 (2014).
10. M. K. Hudait, M. Clavel, P. Goley, **N. Jain**, and Y. Zhu, "Heterogeneous Integration of Epitaxial Ge on Si using AlAs/GaAs Buffer Architecture: Suitability for Low-power Fin Field-Effect Transistors", *Scientific Reports* 4: 6964-6969 (2014).

11. N. Shehata, K. Meehan, I. Hassounah, M. K. Hudait, **N. Jain**, M. Clavel, S. Elhelw Sarah, and N. Madi, "Reduced erbium-doped ceria nanoparticles: one nano-host applicable for simultaneous optical down- and up-conversions", *Nanoscale Research Lett.* 9: 231 (2014).
12. Y. Zhu, **N. Jain**, D. Maurya, R. Varghese, S. Priya, and M. K. Hudait,"X-ray photoelectron spectroscopy analysis and band offset determination of CeO2 deposited on epitaxial (100), (110) and (111)Ge", *J. Vacuum Science & Technology B* 32: 011217-1(2014).
13. M. K. Hudait, Y. Zhu, **N. Jain**, D. Maurya, Y. Zhou, R. Varghese, and S. Priya, "BaTiO3 Integration with Nanostructured Epitaxial (100), (110), and (111) Germanium for Multifunctional Devices", *ACS Applied Materials & Interfaces* 5: 11446-11452(2013).
14. M. K. Hudait, Y. Zhu, **N. Jain**, D. Maurya, Y. Zhou, and S. Priya, "Quasi-zero lattice mismatch and band alignment of BaTiO3 on epitaxial (110)Ge", *J. Appl. Phys*. 114: 024303-1-6 (2013).
15. Y. Zhu, **N. Jain**, D. K. Mohata, S. Datta, D. Lubyshev, J. M. Fastenau, Amy K. Liu, and M. K. Hudait,"Band offset determination of mixed As/Sb type-II staggered gap heterostructure for n-channel tunnel field effect transistor application", *J. Appl. Phys.* 113: 024319 (2013).
16. M. K. Hudait, Y. Zhu, **N. Jain**, and J. L. Hunter, Jr.,"Structural, morphological, and band alignment properties of GaAs/Ge/GaAs heterostructures on (100), (110) and (111)A GaAs substrates", *J. Vacuum Science & Technology* B 31: 011206 (2013).
17. Y. Zhu, **N. Jain**, S. Vijayaraghavan, D. K. Mohata, S. Datta, D. Lubyshev, J. M. Fastenau, and Amy K. Liu, N. Monsegue and M. K. Hudait,"Defect assistant band alignment transition from staggered to broken gap in mixed As/Sb tunnel field effect transistor heterostructure", *J. Appl. Phys.* 112: 094312 (2012).
18. N. A. Shehata, K. Meehan, **N. Jain**, and M. K. Hudait,"Control of oxygen vacancies and Ce+3 concentrations in doped ceria nanoparticles via the selection of lanthanide element", *J. of Nanoparticle Research*, 14: 1173 (2012).
19. Y. Zhu, **N. Jain**, D. K. Mohata, S. Datta, D. Lubyshev, J. M. Fastenau, A. W. K. Liu, and M. K. Hudait,"Structural properties and band offset determination of p-channel mixed As/Sb type-II staggered tunnel filed-effect transistor structure", *Appl. Phys. Lett.* 101: 112106 (2012).
20. M. K. Hudait, Y. Zhu, **N. Jain**, S. Vijayaraghavan, A. Saha, T. Merritt, and G. A. Khodaparast "In-situ grown Ge in an arsenic-free environment for GaAs/Ge/GaAs heterostructures on off-oriented (100)GaAs substrates using molecular beam epitaxy", *J. Vacuum Science & Technology B* 30(5): 051205 (2012).
21. Y. Zhu, **N. Jain**, S. Vijayaraghavan, D. K. Mohata, S. Datta, D. Lubyshev, J. M. Fastenau, A. W. K. Liu, N. Monsegue, and M. K. Hudait,"Role of InAs and GaAs terminated heterointerface at

source/channel on the mixed As-Sb staggered gap tunnel FET structures grown by molecular beam epitaxy", *J. Appl. Phys.* 112: 024306 (2012).

CONFERENCES:

1) **N. Jain**, et. al., " Towards a Monolithic, an All-Epitaxial and Substrate-Reusable Design for III-V-on-Si Solar Cells," *42nd IEEE Photovoltaic Spec. Conf.*, 2015, New Orleans, LA.
2) **N. Jain**, et. al., "Towards III-V Multi-junction Solar Cells on Si Substrate: Epitaxial GaAs-on-Si Characterization & Performance Modeling" *6th World Conf. Photovoltaic Energy Conversion*, 2014, Kyoto, Japan (Accepted).
3) **N. Jain**, et. al., "Performance Evaluation of Heterogeneously Integrated 3J InGaP/GaAs/Si Tandem Solar Cells for Concentrated Photovoltaics," *40th IEEE Photovoltaic Spec. Conf.*, 2014, Denver, Colorado.
4) **N. Jain**, and M.K. Hudait, "Design of Metamorphic Dual-Junction InGaP/GaAs Solar Cell on Si with Efficiency Greater than 29%," *38th IEEE Photovoltaic Spec. Conf.*, 2012, Austin, Texas (**finalist for best poster award).**

PATENTS & INVENTION DISCLOSURES:

(Inventors for all -- **N. Jain** and M. K. Hudait)

1) Highly Efficient & Low Cost/Watt, Monolithic Integrated Module (MIM) of III-V Solar Cells on Si (**VTIP:12-006).**
2) High Yield, Low Cost III-V Multi-Junction Solar Cells by Epitaxial Release from Si Substrate, (**VTIP:12-027**).
3) Monolithic Integration Module of Epitaxially Released III-V Tandem Solar Cells from Si Substrate, (**VTIP:12-028**).

(ii) List of Useful Links

1. Bandgap and lattice-constants for III-Vs.
   http://www.cleanroom.byu.edu/EW_ternary.phtml

2. Properties of III-V semiconductors
   http://www.semiconductors.co.uk/propiiiv5653.htm
   http://www.ioffe.rssi.ru/SVA/NSM/Semicond/GaAs/

3. Doping and resistivity conversion for Si
   http://www.cleanroom.byu.edu/ResistivityCal.phtml

4. Molecular beam epitaxy
   https://faebianbastiman.wordpress.com/category/mbe-fundamental-principles/

5. Etching
   http://en.wikibooks.org/wiki/Microtechnology/Etching_Processes
   http://terpconnect.umd.edu/~browns/wetetch.html
   http://www.cleanroom.byu.edu/wet_etch.phtml

6. Optical Constants and ARC Design
   http://www.filmetrics.com/reflectance-calculator
   http://refractiveindex.info/

7. Journal Abbreviations
   http://cassi.cas.org/search.jsp