Advanced Control Schemes for High-Bandwidth Multiphase Voltage Regulators

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ABSTRACT

Advances in transistor-integration technology and multi-core technology of the latest microprocessors have driven transient requirements to become more and more stringent. Rather than relying on the bulky output capacitors as energy-storage devices, increasing the control bandwidth (BW) of the multiphase voltage regulator (VR) is a more cost-effective and space-saving approach. However, it is found that the stability margin of current-mode control in high-BW design is very sensitive to operating conditions and component tolerance, depending on the performance of the current-sensing techniques, modulation schemes, and interleaving approaches. The primary objective of this dissertation is to investigate an advanced multiphase current-mode control, which provides accurate current sensing, enhances the stability margin in high-BW design, and adaptively compensates the parameter variations.

Firstly, an equivalent circuit model for generic current-mode controls using DCR current sensing is developed to analyze the impact of component tolerance in high-BW design. Then, the existing state-of-the-art auto-tuning method used to improve current-sensing accuracy is reviewed, and the deficiency of using this method in a multiphase VR is identified. After that, enlightened by the proposed model, a novel auto-tuning method is proposed. This novel method

features better tuning performance, noise-insensitivity, and simpler implementation than the state-of-the-art method.

Secondly, the current state-of-the-art adaptive current-mode control based on constant-frequency PWM is reviewed, and its inability to maintain adequate stability margin in high-BW design is recognized. Therefore, a new external ramp compensation technique is proposed to keep the stability margin insensitive to the operating conditions and component tolerance, so the proposed high-BW constant-frequency control can meet the transient requirement without the presence of bulky output capacitors. The control scheme is generic and can be used in various kinds of constant-frequency controls, such as peak-current-mode, valley-current-mode, and average-current-mode configurations.

Thirdly, an interleaving technique incorporating an adaptive PLL loop is presented, which enables the variable-frequency control to push the BW higher than proposed constant-frequency control, and avoids the beat-frequency input ripple. A generic small-signal model of the PLL loop is derived to investigate the stability issue caused by the parameter variations. Then, based on the proposed model, a simple adaptive control is developed to allow the BW of the PLL loop to be anchored at the highest phase margin. The adaptive PLL structure is applicable to different types of variable-frequency control, including constant on-time control and ramp pulse modulation.

Fourthly, a hybrid interleaving structure is explored to simplify the implementation of the adaptive PLL structure in an application with more phases. It combines the adaptive PLL loop

with a pulse-distribution technique to take the advantage of the high-BW design and fast transient response without adding a burden to the controller implementation.

As a conclusion, based on the proposed analytical models, effective control concepts, systematic optimization strategies, viable implementations are fully investigated for high-BW current-mode control using different modulation techniques. Moreover, all the modeling results and the system performance are verified through simulation with a practical output filter model and an advanced mixed-signal experimental platform based on the latest MHz VR design on the laptop motherboard. In consequence, the multiphase VRs in future computation systems can be scalable easier with proposed multiphase configurations, increase the system reliability with proposed adaptive loop compensation, and minimize the total system footprint of the VR with the superior transient performance.

To My Family

My mother and brother: Li-Hsiang Chou and Yung-Hsin Liu

My parents in law: Baishen Li and Lihua Gao

My wife: Meiyan Li

My son: Jayden Liu

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Chapter 1. Introduction

This chapter presents the motivations, objectives and an overview of this dissertation. The challenges of the state-of-the-art control schemes in high-bandwidth design are investigated to determine how they can fulfill the power delivery demand of future microprocessors. This chapter provides a review of this field, followed by the dissertation outline and the scope of research.

1.1 Research Background

1.1.1 Trend of Microprocessors

The central processing units (CPU) on a microprocessor are the heart of computation systems such as laptops, desktops, and servers. To achieve more powerful computation and data processing, more and more transistors are integrated, and higher clocking is performed in future microprocessors. Based on the historical data of transistor counts in Figure 1.1, the number of transistors on a microprocessors has grown exponentially from 2300 to 1 billion transistors between 1974 and 2013 [A.1][A.2][A.3]. Also, based on the historical data of clock frequency shown in Figure 1.2, the frequency has grown from 108kHz to over 3 GHz operation between 1974 and 2013 [A.1][A.2][A.3]. The approximate power consumption (P_{CPU}) of a CPU is proportional to the clocking frequency (f_{CLK}) and the square of the core voltage (V_{Core}) [A.4][A.5], which is:

$$P_{CPU} = C\ f_{CLK} V_{Core}^{\ 2} \tag{1.1}$$

where C is the lumped parasitic capacitance of the total logic gates. Based on the equation, more transistors and a higher f_{CLK} increase CPU power dissipation significantly, so the thermal issue will become a bottleneck for a high-performance CPU.

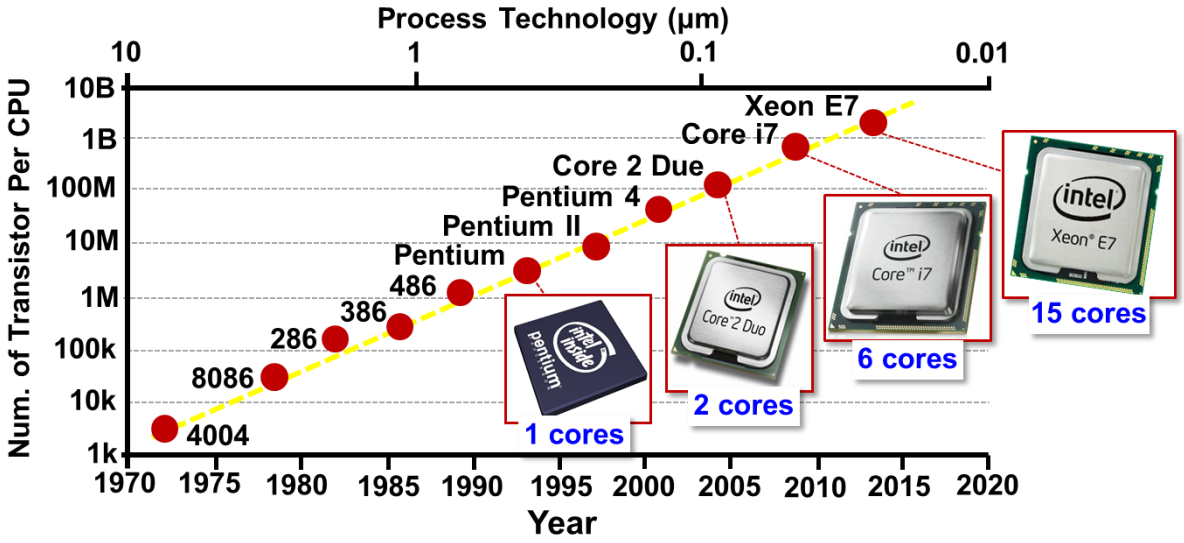


Figure 1.1 The trend in transistor integration on a microprocessor [A.1][A.2][A.3]

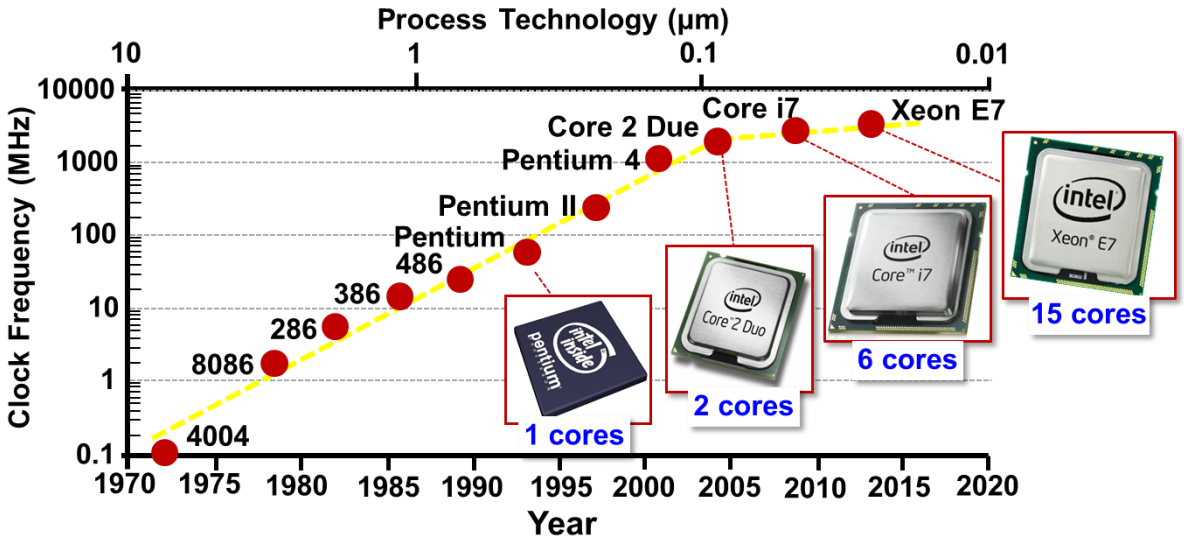


Figure 1.2 The trend in clock frequency of microprocessors [A.1][A.2][A.3]

Since 2005, the multi-core technology has been applied, so the CPU performance can be boosted without increasing f_{CLK} higher than 5GHz, as shown Figure 1.2. The reason is that a multi-core CPU can perform multitasking at the same time by utilizing all cores to run different application software. Recently, IBM introduced a 12-core POWER8 processor in 2014, while Intel announced a 15-core Xeon E7 processor in the same year. The core count will keep increasing every year due to the advance of silicon technology [A.6][A.7][A.8]. Moreover, f_{CLK} of each core can be adjusted based on its computation demand, so the growth rate of the power dissipation can be reduced, according to (1.1). Terminologically, the growth rate of thermal design power (TDP) of a CPU becomes slows. TDP is not the peak power of a CPU, but the maximum power which a CPU can draw for a thermally significant period while running software programs [A.5]. TDP is used for the thermal solution design target of microprocessors. For example, Intel's Core 2 Duo E8300 with 2.83GHz clocking and 2 cores consumes 65W TDP, but the consumption of the latest Xeon E7 processor with 3.8GHz clocking and 15 cores only increases to 150W TDP.

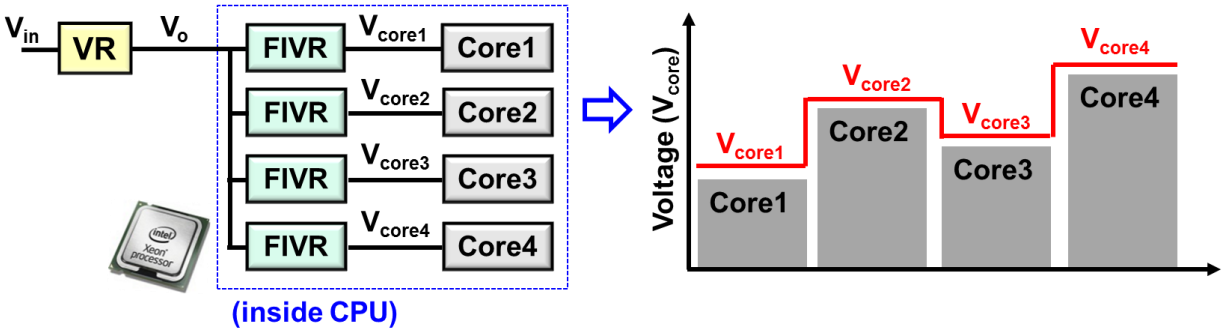
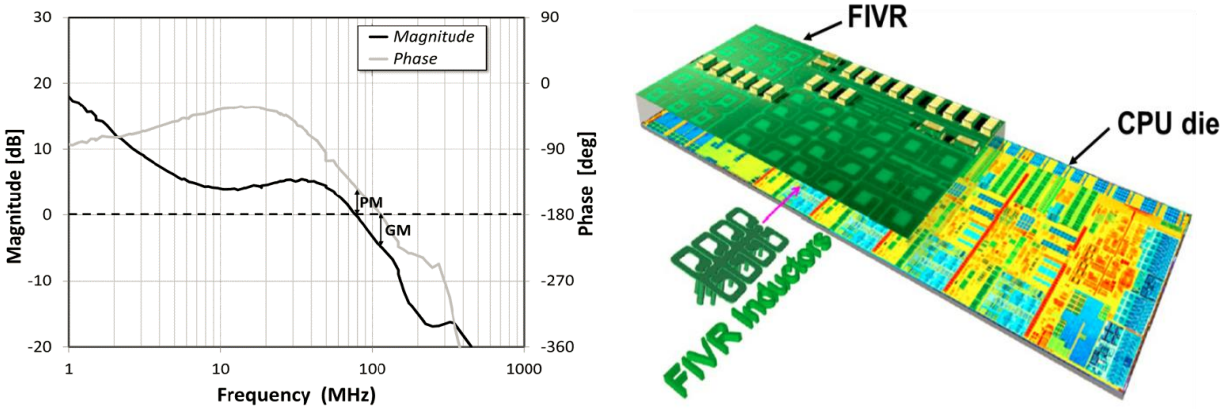


Figure 1.3 The VR platform for Haswell and Broadwell CPU [A.9][A.10]

In order to further minimize TDP, each core has been powered by an individual voltage rail since 2013, such that V_{core} can also be adjusted dynamically according to its computation

demand, as shown in Figure 1.3. The power delivery of the latest CPUs, such as the Haswell and Broadwell series, contains a two-stage VR: fully integrated voltage regulators (FIVR) to power each core in a CPU, and an external VR to power all FIVRs [A.9][A.10]. Higher switching frequency (f_{sw}) and higher control-loop bandwidth (BW) are the two critical design parameters to allow FIVR co-packing with a CPU die. Figure 1.4 demonstrates that the BW of a FIVR in Haswell CPU is designed at 80MHz for f_{sw}=140MHz, so the FIVR can provide faster transient response with a minimum number of output capacitors on the FIVR module [A.11].



(a) (b)

Figure 1.4 FIVR on the CPU die: (a) control loop design, and (b) chip micrograph [A.11]

However, the multicore technology impose a new challenge to the external VR design, since a multicore CPU can generate much higher transient current from the external VR during Turbo Boost mode [A.12][A.13][A.14]. As shown in Figure 1.5, Turbo Boost mode forces many cores in a CPU activated with higher f_{CLK} simultaneously for a short period of time, and the f_{CLK} can be even higher when fewer cores run in this mode [A.12]. The purpose is to boost the core performance under a heavy workload, such as video gaming and streaming. According to the instantaneous power demand example of Intel's latest CPU as Figure 1.6, the maximum power

during Turbo Boost mode can be two times higher than TDP at least [A.13]. For example, a Haswell CPU with TDP of 150W, the CPU takes only around 96A from its voltage regulator (VR) in TDP mode, but can sink around 200A in Turbo Boost mode for a short period of time [A.14]. Since activating Turbo Boost mode can generate a large load current change with a high current slew rate (di/dt), a powerful external VR with a very fast transient response is needed to meet the load current demand.

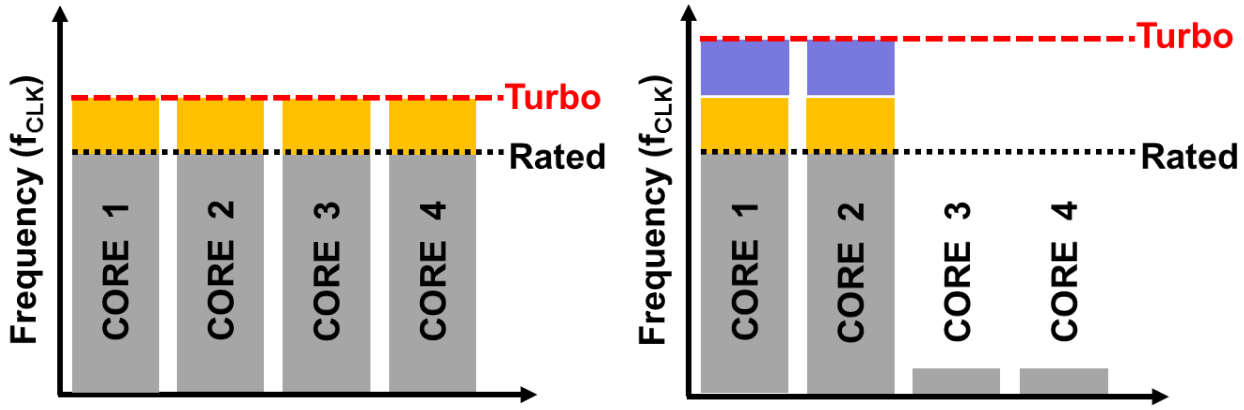


Figure 1.5 A quad-core CPU in Turbo Boost mode activated for: (a) all cores, and (b) fewer cores [A.12]

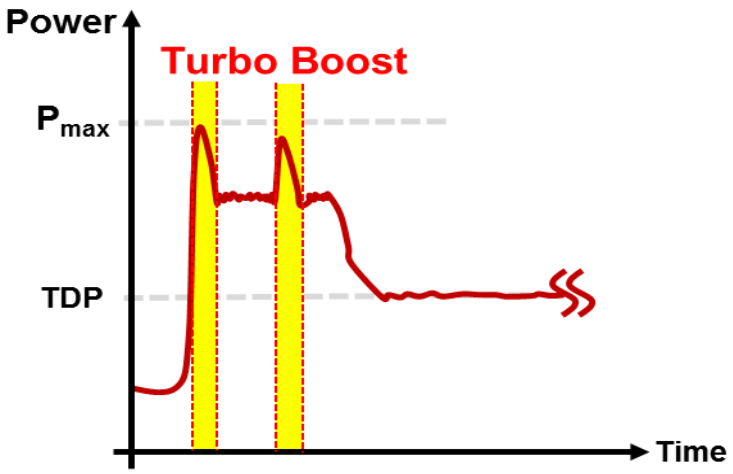


Figure 1.6 The instantaneous power demand in Turbo Boost mode [A.13]

1.1.2 Trend of High-Bandwidth Design for Voltage Regulators

The control loop design of the external VR is indispensable to meet the load-line regulation with a well-known control technique, called adaptive voltage position (AVP). When the load current (I_o) increases gradually, AVP control allows the output voltage (V_o) to reduce gradually with a predetermined slope, defined as the load line resistance (R_{LL}) [A.14][A.15]. Therefore, the steady-state V_o can be defined as:

$$V_o = VID - I_o R_{LL} \tag{1.2}$$

where the VID (voltage identification) is the reference output voltage command sent from the CPU to the VR controller.

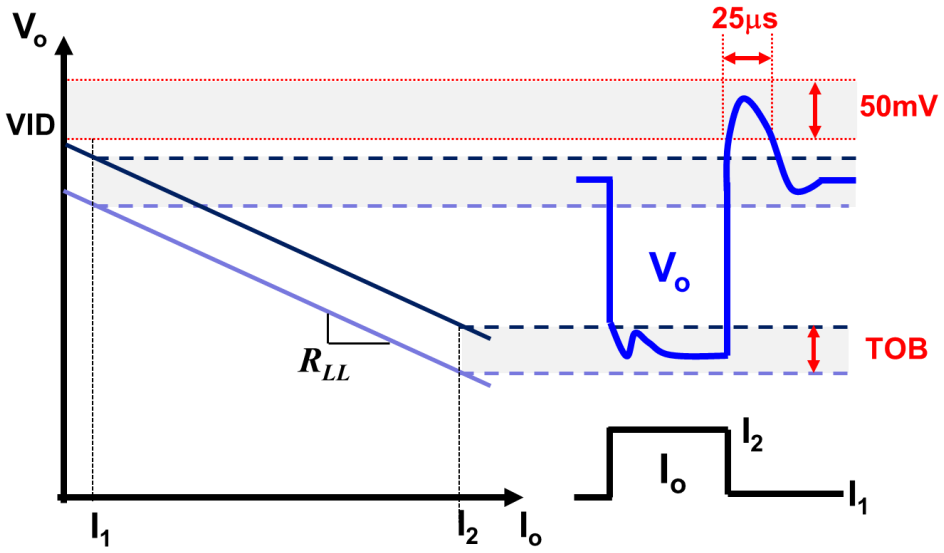


Figure 1.7 The relation between the load-line specification and the permitted load transient [A.14][A.15]

Figure 1.7 shows the relationship between the load-line specification and the transient waveform of V_o under the step load current change. For load step-up, V_o should step down and settle within the tolerance band (TOB) around +/-20mV. The voltage undershoot cannot be less

than the lower boundary, because a larger undershoot may cause system lock-up or data corruption. For load step-down, V_o should step up and settle within the TOB under a permitted short transient overshoot event, whose voltage cannot exceed the overshoot relief (VID+50mV) and duration is within 25uS. The larger overshoot may cause a higher processor operating temperature, which results in damage or a reduced processor life span [A.14][A.15].

To minimize the transient spike, there are different kinds of output capacitors of VR along the power delivery path, as shown in Figure 1.8. Figure 1.9 and Figure 1.10 show today's motherboards using Intel's quad-core i7 microprocessor for a desktop computer and for an Apple's laptop computer, respectively [A.16][A.17]. It is found that the external VR relies on many bulky output capacitors on the motherboards to meet the stringent AVP requirement, since the AVP response of the control loop is not fast enough; i.e., the control-loop BW is relatively low. The bulky capacitors not only occupy the precious motherboard space, but also increase the component cost. Since the trend of electronic devices suggests they will continue to become lighter and thinner in the future, the space for the CPU VR will be further squeezed. Therefore, the enabling technology of high-BW design is critical to remove the need for bulky capacitors.

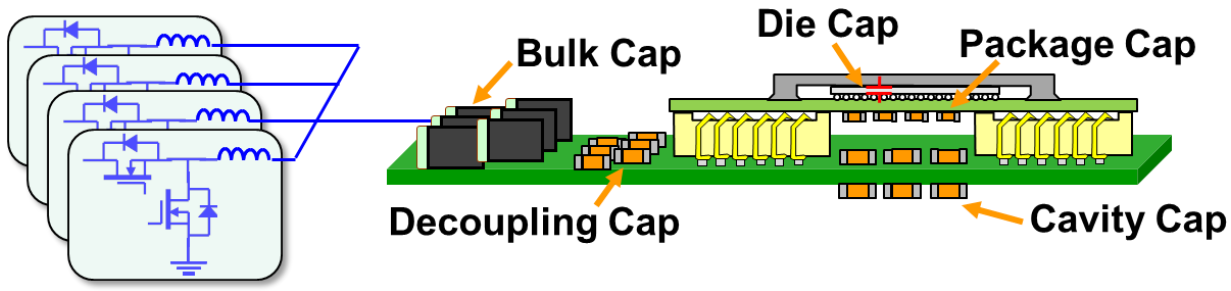


Figure 1.8 Output capacitors on the power delivery path between an external VR and a CPU

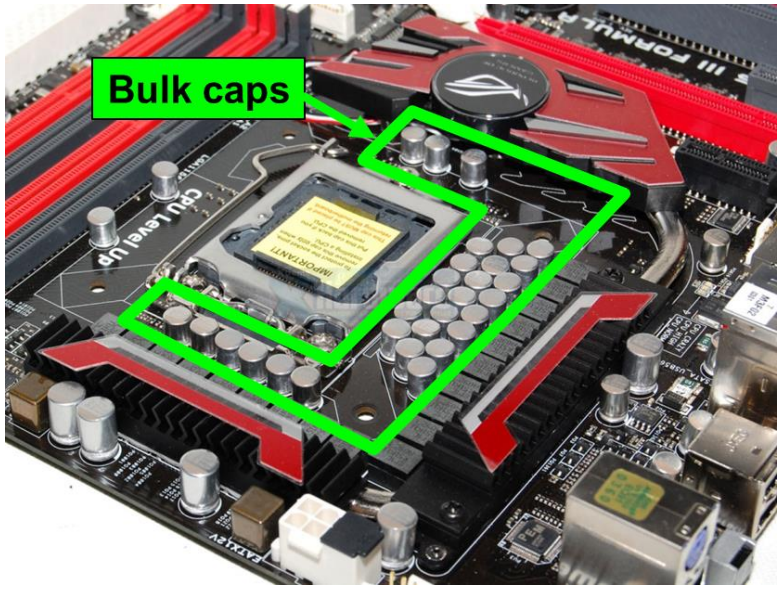


Figure 1.9 Motherboard of a desktop computer with an Intel i7 microprocessor [A.16]

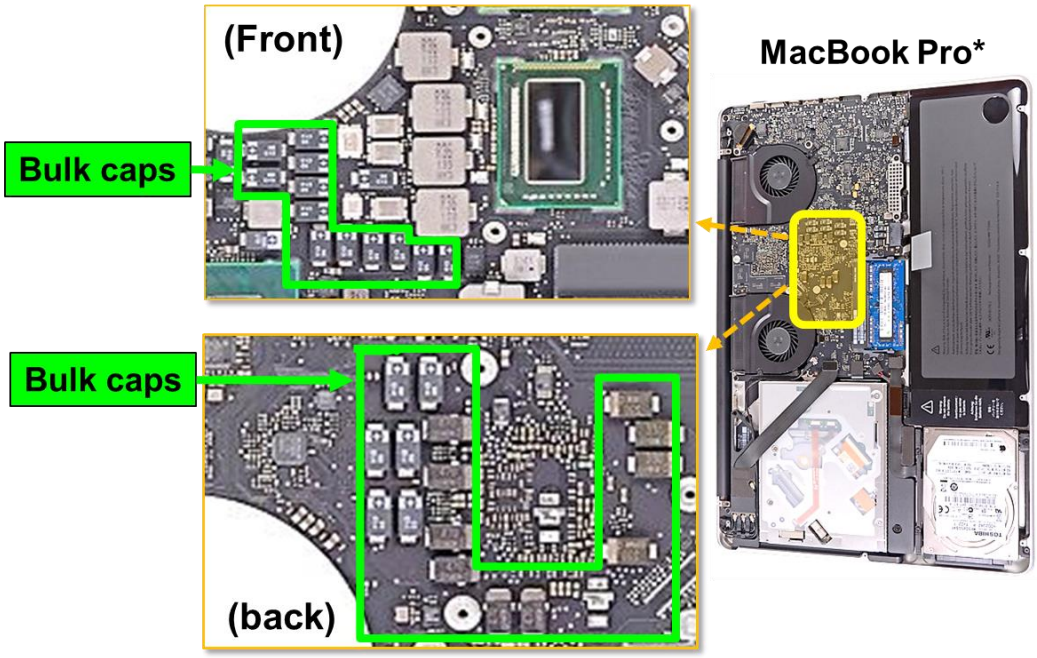
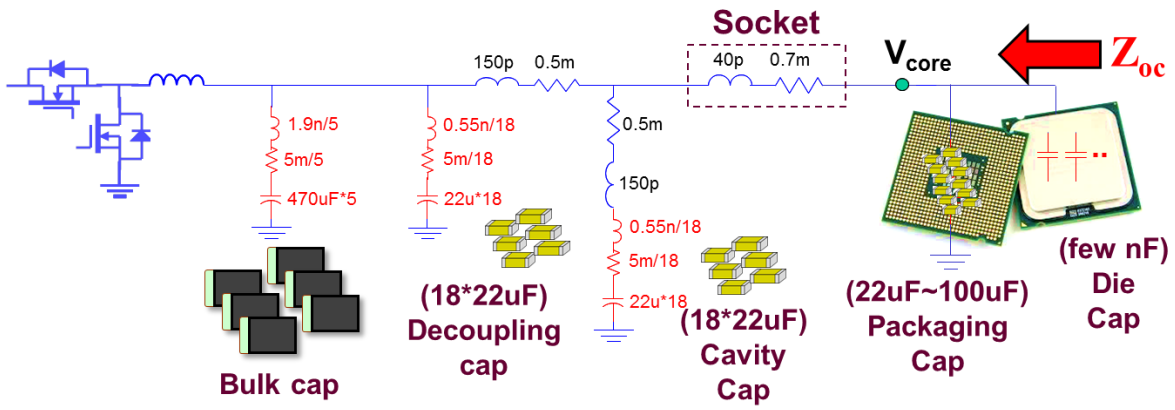


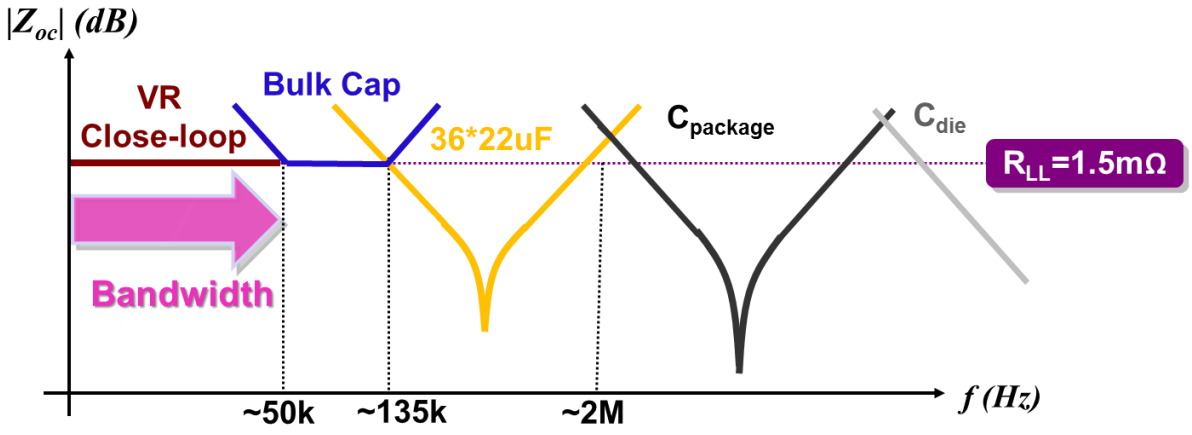
Figure 1.10 Motherboard of a laptop computer with an Intel i7 microprocessor [A.17]

To meet the stringent AVP requirement without any bulky capacitors, the target BW is identified as follows. Two design guidelines have been addressed to meet the AVP requirement:

the first is maintaining a sufficient phase margin higher than 60° at the control BW to avoid the peaking of closed-loop output impedance (Z_{oc}) to be higher than R_{LL}, and the second is that the output capacitors should be properly chosen to avoid Z_{oc} peaking for the frequency range higher than the control BW [A.14][A.15][A.18][A.19].



(a)



(b)

Figure 1.11 Output filter model of a CPU VR from a laptop: (a) parameters, and (b) Z_{oc}

Figure 1.11 shows an output filter model of a laptop CPU with an R_{LL} specification of 1.5mΩ. The bulk capacitor is an aluminum-polymer solid capacitor with large capacitance, high

equivalent series resistance (ESR), and high equivalent series inductance (ESL), so the impedance characteristic can cover the low-frequency range from 50kHz to 135kHz. Following the bulk capacitors, two branches of multi-layer ceramic capacitors (MLCCs) are used as the middle-frequency decoupling capacitors between 135kHz and 2MHz, where the first branch contains 22·22μF MLCC capacitors in an 0805 package placed around the CPU socket, and the second branch contains 22·22μF MLCC capacitors in an 0805 package mounted in the socket cavity, also called the "cavity cap". After these, there are packaging capacitors and die capacitors on the microprocessor, which serve as the high-frequency decoupling capacitors for the frequencies range higher than 2MHz.

In the previous VR11.1 specification, the BW is designed to be around 30kHz to 40kHz, due to the optimal switching frequency (f_{sw}) of 300kHz, to maintain good efficiency in the single-stage power delivery structure [A.15]. Recently, the optimal f_{sw} has increased to be around 600kHz to 800kHz, because of better switching devices. It may be possible to push the BW to 135kHz to eliminate bulk capacitors, and push even beyond to reduce more decoupling capacitors outside of the socket. Under the optimal f_{sw} range, the BW of 135kHz is around $f_{sw}/6$ and $f_{sw}/4$. Since the BW is designed to be much closer to $f_{sw}/2$, the impact of the aliasing effect from the control loop on the system stability margin has to be considered. In the VR12.5 specification, the control BW must be higher than 100kHz to minimize the use of bulk capacitors [A.20].

1.1.3 Trend of Power Delivery in Computation Systems

The original power delivery of VRs for CPUs directly steps down high input voltage (V_{in}) into low output voltage (V_o), so the duty cycle is narrow during normal operation. For server and desktop VRs, the 12V input from the AC/DC converter can range from 10.8V to 12.5V, so the duty cycle can vary from 0.04 to 0.15 considering the possible V_o scaling from 0.5V to 2V, as shown in Figure 1.12 [A.14][A.15][A.20]. However, the duty cycle range becomes even narrower for conventional laptop VRs, because of a higher V_{in} of 19V from the adaptor. Under such a narrow duty cycle range, it is very difficult to achieve good efficiency for switching frequencies higher than 300kHz.

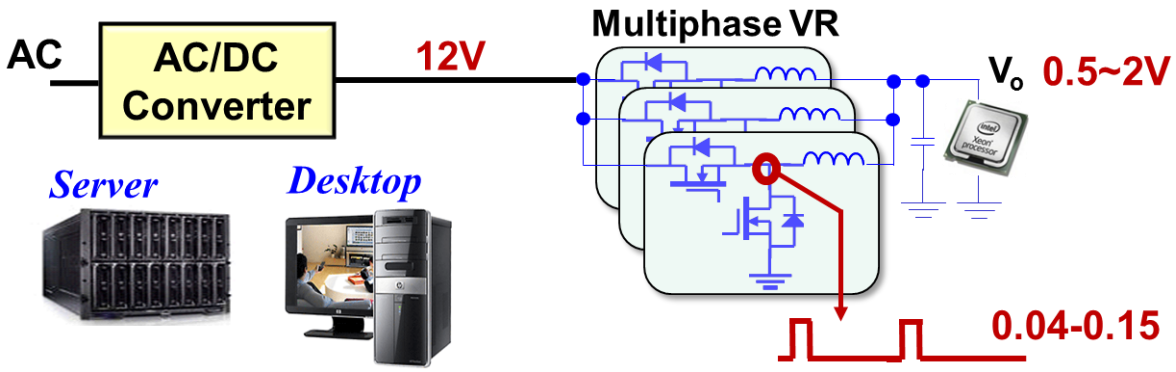


Figure 1.12 Power delivery structure for server and desktop computers

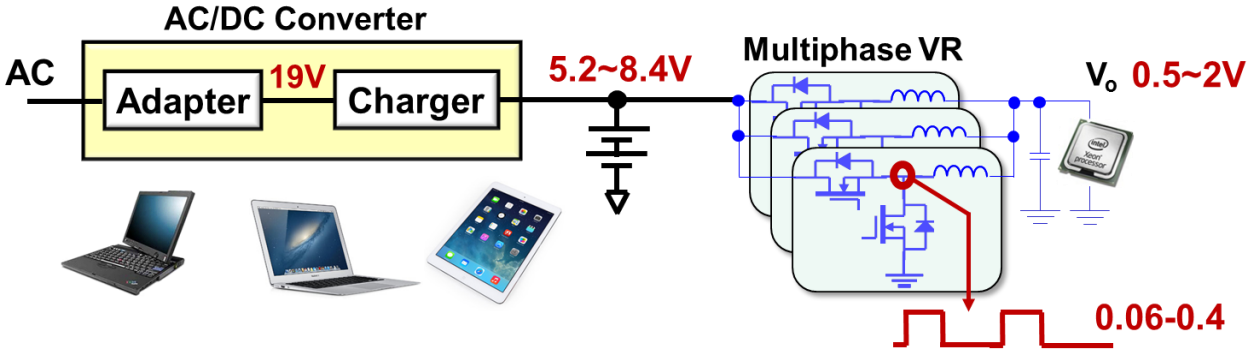


Figure 1.13 Power delivery structure for the latest battery-powered electronic devices

A two-stage power delivery architecture has been developed to boost the efficiency for higher f_{sw} operation [A.21][A.22][A.23][A.24]. Recently, a similar concept has been applied onto the latest laptop by utilizing the battery charger as the first-stage VR to step down 19V to a lower voltage, such that the duty cycle range of the second-stage VR becomes wider. The V_{in} range of the second-stage VR is between 5.2V to 8.4V, because two serially-connected battery cells are placed at the battery charger output [A.25][A.26][A.27][A.28]. The duty cycle can vary from 0.06 to 0.4, based on the possible V_o scaling from 0.5V to 2V, as shown in Figure 1.13. The efficiency improvement of the second-stage VR is demonstrated in Figure 1.14 under different load current conditions, in which L_s=0.36μH, f_{sw}=300kHz, V_o=1.8V, a top FET with BSZ065N03L, and a bottom FET with BSZ0901NSI [A.28].

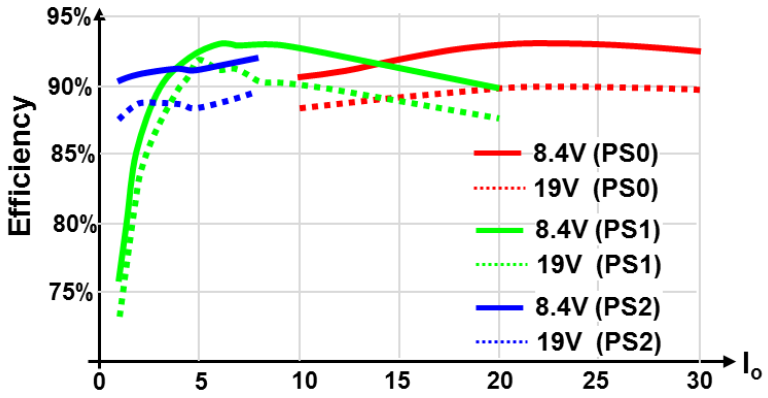


Figure 1.14 Efficiency improvement of the two-stage structure for a laptop VR [A.28]

It is necessary that the control loop design of the VR considers different V_{in} and V_o operating conditions of the latest power delivery structure, so the impacts of the duty cycle range on the state-of-the-art control schemes in high-BW design needs to be further investigated, such as the system stability and multiphase operation.

1.2 Challenges of State-of-the-Art Control Schemes

1.2.1 Accuracy of Inductor DCR Current Sensing

Calculating the correct load current information is essential to achieve AVP. The inductor DCR sensing technique has been widely used for low-voltage and high-current VR due to its lossless sensing and simple implementation. The DCR sensing method contains an R_sC_s network in parallel with the output inductor, and a differential current amplifier (A_i) to sense the voltage across C_s, as shown in Figure 1.15 [A.29][A.30][A.31][A.32][A.33][A.34]. The transfer function from inductor current (i_L) to output of the current sensor (V_i) is:

$$H_i(s) \equiv \frac{V_i(s)}{i_L(s)} = A_i R_{Ls} \frac{s\tau_{Ls}+1}{s\tau_{Cs}+1} \tag{1.3}$$

where τ_{Cs}, equal to $R_s \cdot C_s$, is the time constant of DCR sensing network, τ_{Ls}, equal to L_s/R_{Ls}, is the time constant of the output inductor, A_i is the amplification gain, and R_{Ls} is the DC winding resistance (DCR). Equation (1.3) shows a frequency-dependent term related with the two time constants, so V_i is proportional to the voltage across the inductor DCR only if $\tau_{Cs}=\tau_{Ls}$.

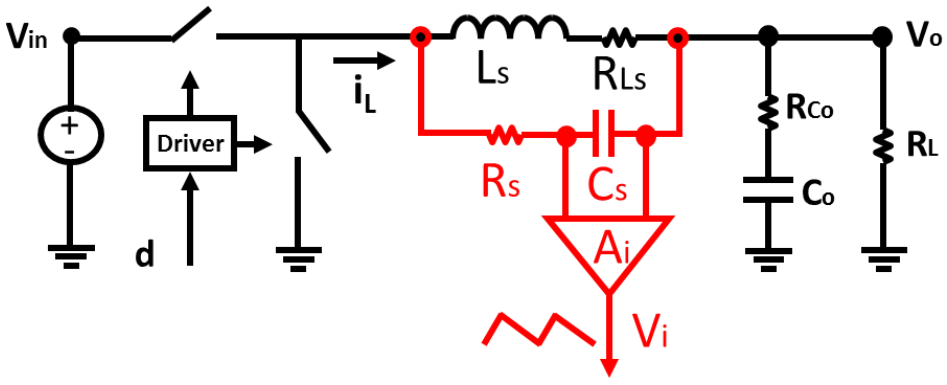


Figure 1.15 Block diagram of inductor DCR current sensing network

In reality, the two time constants are functions of component tolerances, so it is very difficult to make $\tau_{Cs}=\tau_{Ls}$. The actual L_s and C_s are highly dependent on the material, operating condition, aging effect, and manufacturing tolerance. Therefore, even though typical values of both are designed equally, τ_{Cs} can still be +/-40% away from τ_{Ls} in the worst case, where C_s tolerance for a ceramic capacitor of 0.1µF ranges between -28% and +15% (X7R M-type 0603 from Murata Inc.) and L_s tolerance for ferrite power inductor of 150nH ranges between -35% and +20% (NiZn-type in Cyntec Inc.).

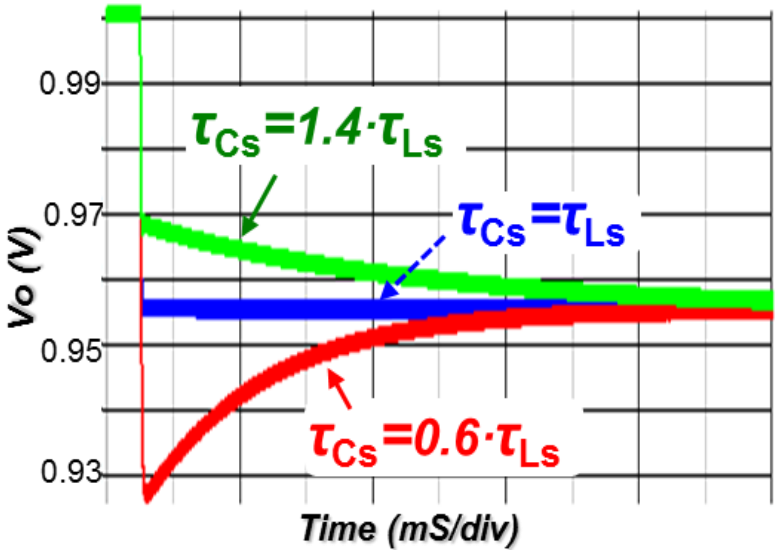


Figure 1.16 The effect of time constant mismatch on AVP response

When a time constant mismatch occurs, the AVP response could fail to meet the stringent requirements described in Section 1.1.2. Figure 1.16 shows a simulation example to highlight the issue under the worst-case mismatch condition. The simulation conditions are: V_{in}=12V, V_o=1V, C_o=36·22µF (ceramic), R_{LL}=1.5mΩ, and f_{sw}=800kHz. For the output inductor with L_s=150nH and R_{Ls}=0.5mΩ, the typical value of DCR current sensing network is C_s=0.1µF and R_s=3kΩ. The simulation results show that when τ_{Cs} is 40% less than τ_{Ls}, voltage undershoot occurs, so more

output capacitors may be needed to minimize it. On the other hand, when τ_{Cs} is 40% higher than τ_{Ls}, the slow AVP response takes long time to settle into steady state.

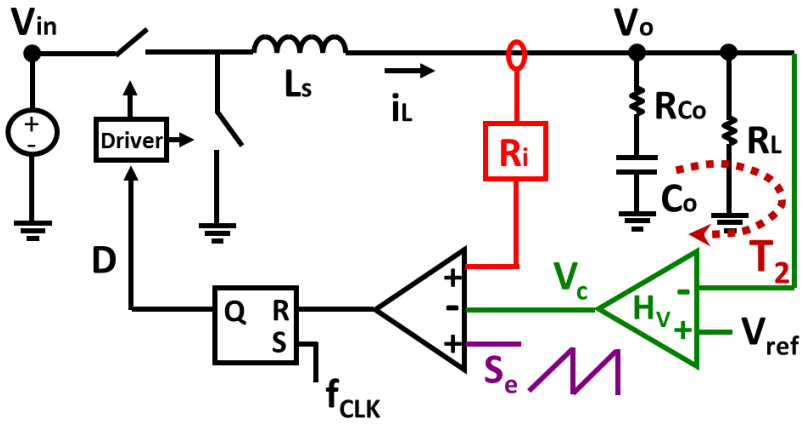
Therefore, it is found that the DCR current sensing is very sensitive to component tolerance, so it is necessary to analyze the impacts on the state-of-the-art control schemes in high-BW design. Also, it is advantageous to investigate an effective self-compensation scheme to correct the time-constant mismatch such that the output capacitor does not need to be overdesigned.

1.2.2 Constant-Frequency Control

Figure 1.17 shows the block diagram and the operation principle of constant-frequency peak-current mode control (PCM) [A.36][A.37][A.38]. The operation principle is that a fixed-frequency reference clock (f_{CLK}) initiates the turn-on instance, and then the inductor current feedback ($i_L \cdot R_i$) compares with the voltage difference of control voltage (V_c) and an external ramp (S_e) to determine the turn-off instance. Since the inner current loop directly feedbacks the inductor current, all high-frequency components are coupled to the modulator. When V_c generates a small-signal perturbation at frequency f_m to the modulator, the perturbed i_L contains many frequency components, including the fundamental component at f_m, the switching frequency component (f_{sw}), its harmonic (nf_{sw}), and the sideband components ($f_{sw} \pm f_p$, $nf_{sw} \pm f_p$), as shown in Figure 1.18.

It is found that when f_m moves toward $f_{sw}/2$, the primary sideband component ($f_{sw}-f_p$) also moves toward $f_{sw}/2$. When $f_m=f_{sw}/2$, the collision of two components causes an amplification effect of f_m at $f_{sw}/2$, so a double pole at $f_{sw}/2$ is formed on the transfer function of the open-loop gain with a closed current loop (T_2) [A.39][A.40][A.41]. Interestingly, the duty cycle change

affects the double-pole damping, as shown in Figure 1.19. When D is close to 0.5, the double pole is underdamped, and it is possible to cause secondary crossover without a sufficient phase margin for T_2 loop gain. In the case of a small D, the double pole can be over-damped, which lowers the phase margin. Therefore, the double pole at $f_{sw}/2$ becomes the bottleneck for high-BW design of constant-frequency control.



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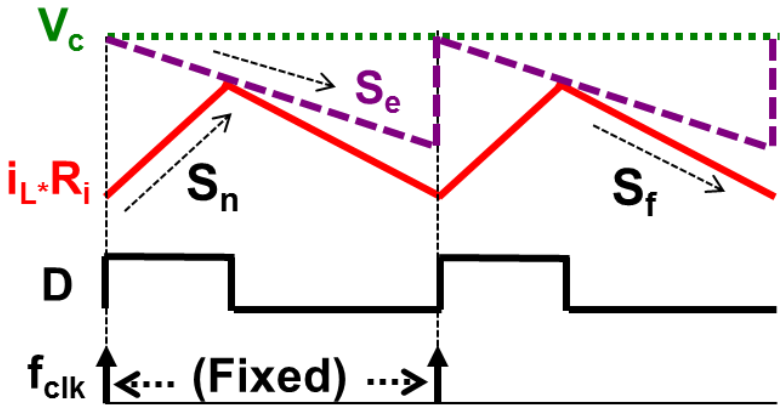
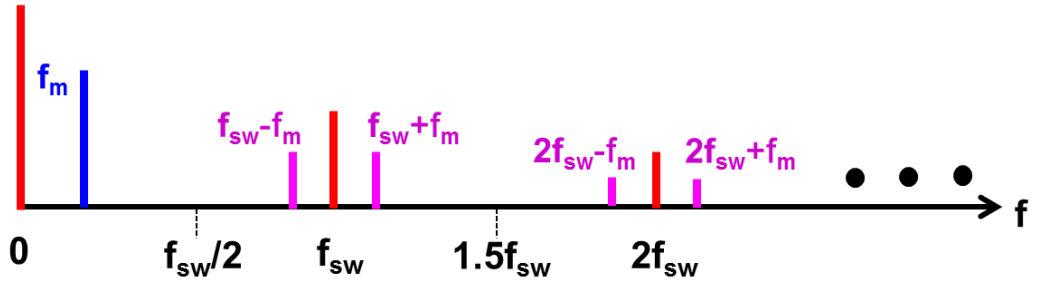
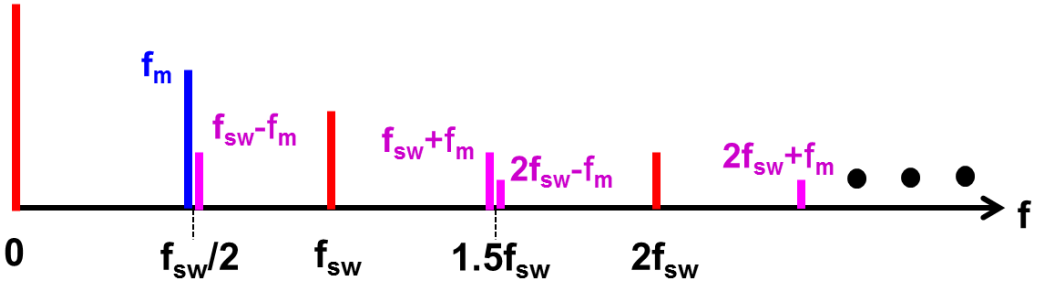


(b)

Figure 1.17 Implementation of PCM control: (a) control structure, and (b) operation principle



(a)



(b)

Figure 1.18 Spectrum of perturbed i_L in constant-frequency control: (a) $f_m << f_{sw}/2$, and (b) $f_m \approx f_{sw}/2$

There are still several advantages of constant-frequency control. The first benefit is that the efficiency and output filter can be optimized with a fixed f_{sw}. The second benefit is that f_{CLK} can be synchronized with other VRs to minimize the beat frequency ripple and possible switching noise coupling [A.42][A.43]. The third benefit is that it is easy to achieve interleaving by phase shifting the f_{CLK} of each phase [A.44]. The fourth benefit of PCM control is a faster step-down transient response due to the variable on-time. Figure 1.20 shows a simulation example to demonstrate that V_o overshoot can be minimized in high-BW design, if the stability margin of the PCM control is enhanced. The simulation conditions are: V_{in}=8.4V, V_o=1.8V, ΔI_o=27A under a slew rate of 100A/uS, f_{sw}=800kHz, L_s=180nH, R_{LL}=1.5mΩ, C_o=22μF·36 (ceramic capacitors), and PM=60° under a T_2 BW of 135kHz. A higher BW allows V_c to change faster, so

the on-time of D can be truncated more quickly. Therefore, it is still worthwhile to investigate improved constant-frequency control to overcome the sideband effect.

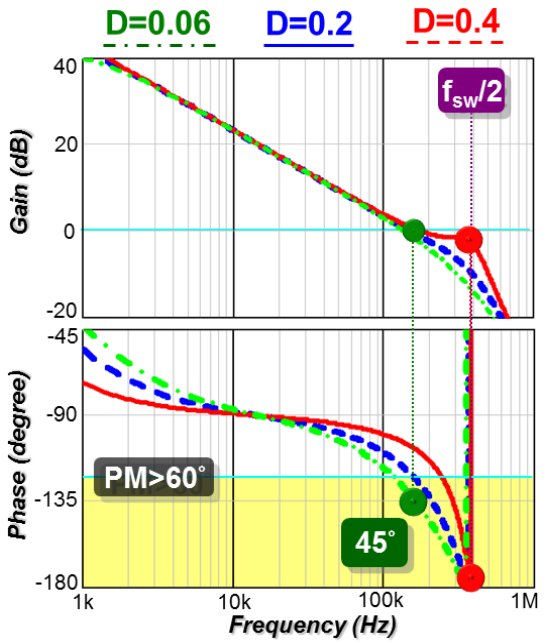


Figure 1.19 Effect of the side-band component on T_2 of PCM control in high-BW design

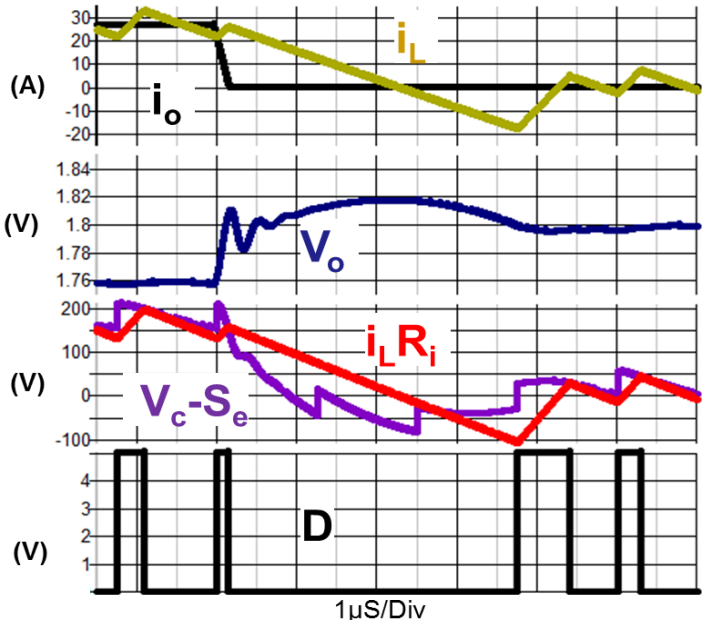
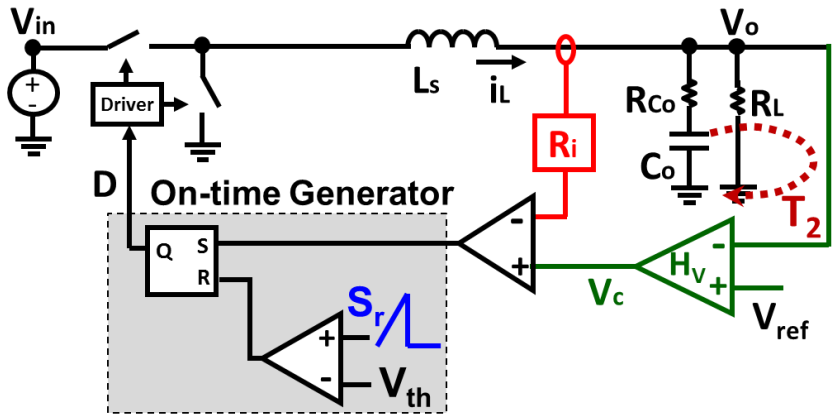


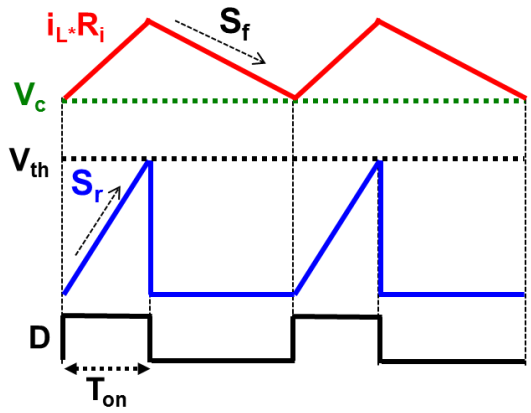
Figure 1.20 Step-down load transient response of PCM control

1.2.3 Variable-Frequency Control

Figure 1.21 shows the block diagram of current mode control with constant on-time modulation (COT) [A.45][A.46][A.47]. The operation principle is that V_c is compared with the inductor current feedback to determine the turn-on instance, and then the fixed on-time pulse is generated by comparing a fixed threshold voltage (V_{th}) with a fixed ramp in the on-time generator (S_r).



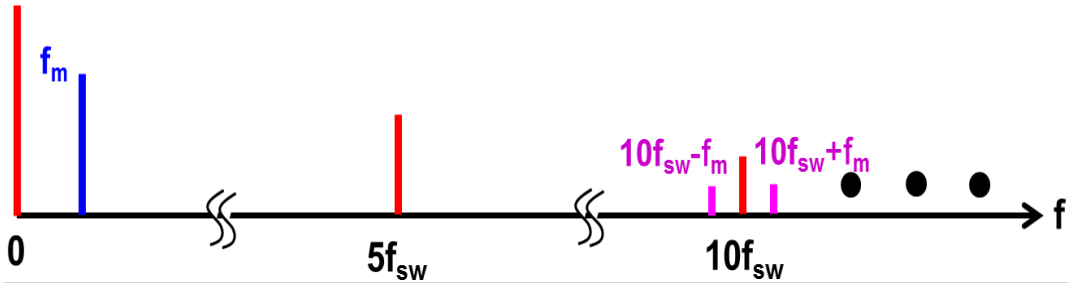
(a)



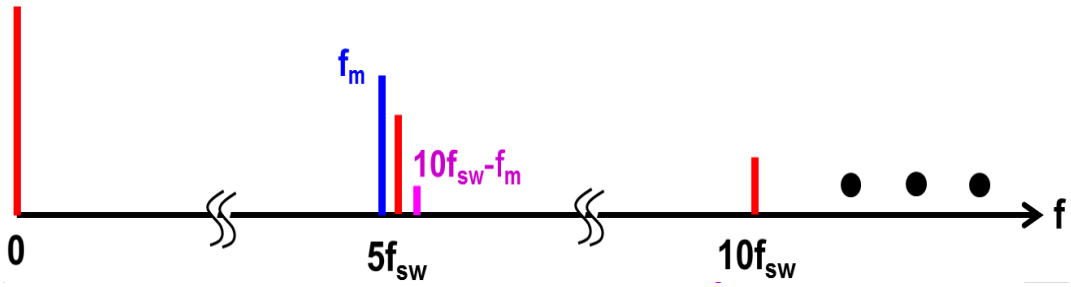
(b)

Figure 1.21 COT current-mode control: (a) control structure, and (b) operation principle

Based on the unified three-terminal switch model in [A.39][A.40][A.41], the current loop also contributes a double pole on T_2 loop gain, but it is pushed away from $f_{sw}/2$ and the quality factor is always constant. This indicates that the amplification effect of the V_c perturbation signal and the primary side band component happens at very high frequencies. When D=0.1, the V_c perturbation signal and the primary side band component collide at $5 \cdot f_{sw}$, as shown in Figure 1.22. The duty cycle change doesn't affect damping, but shifts the double-pole frequency. Therefore, the phase delay effect is almost negligible in the case of a small D. When D=0.4, PM is still higher than 60° at a BW of $f_{sw}/4$, as shown in Figure 1.23. Therefore, COT control can push BW design higher than constant-frequency control.



(a)



(b)

Figure 1.22 Spectrum of perturbed i_L in COT control: (a) $f_m << 5 \cdot f_{sw}$, and (b) $f_m \approx 5 \cdot f_{sw}$

Another advantage of COT control is that it is easier to improve light-load efficiency than when using constant-frequency control. Since COT control is a valley-current mode control, f_{sw} drops naturally with the load decreasing without additional effort, when the inductor current falls into discontinuous conduction mode (DCM) [A.45][A.47]. As for constant-frequency control, an additional constant on-time loop or a pulse-skipping loop is needed to improve light-load efficiency [A.37][A.48].

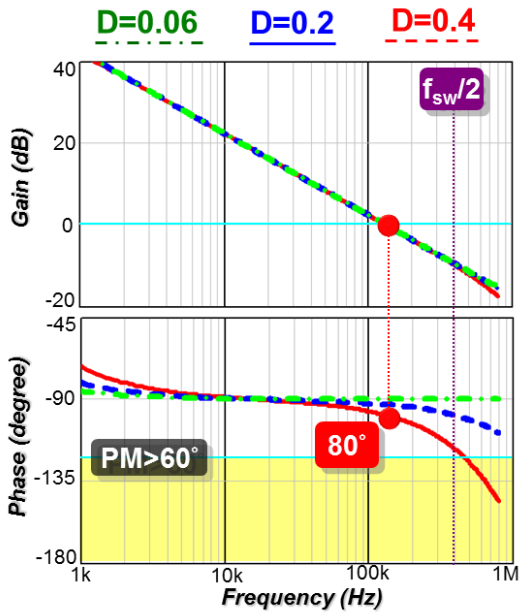


Figure 1.23 Effect of the side-band component on T_2 of COT control in high BW design

However, there are several design challenges for COT control. First is the fact that the steady-state f_{sw} can vary widely under V_{in} and V_o changes if T_{on} is fixed. For example, if f_{sw} is 800kHz when D=0.06, f_{sw} goes to 5.3MHz when D=0.4. Such a wide f_{sw} change creates excessive power loss and makes the output inductor difficult to design. Then, the second challenge is interleaving for multiphase operation, since there is no reference clock to generate correct interleaving angles. The third challenge is the inability of synchronization with other VRs

to minimize the beat-frequency ripple and noise coupling. The fourth issue is the presence of a higher V_o overshoot for load step-down transient than there is with constant-frequency control. Figure 1.24 shows a simulation example to compare V_o overshoot in Figure 1.20 under the same conditions. When the step-down load transient occurs at the beginning of the fixed on-time, D cannot be saturated immediately, in contrast with constant-frequency control, so the T_{on} delay builds more charge to the output capacitor and then creates a higher voltage overshoot.

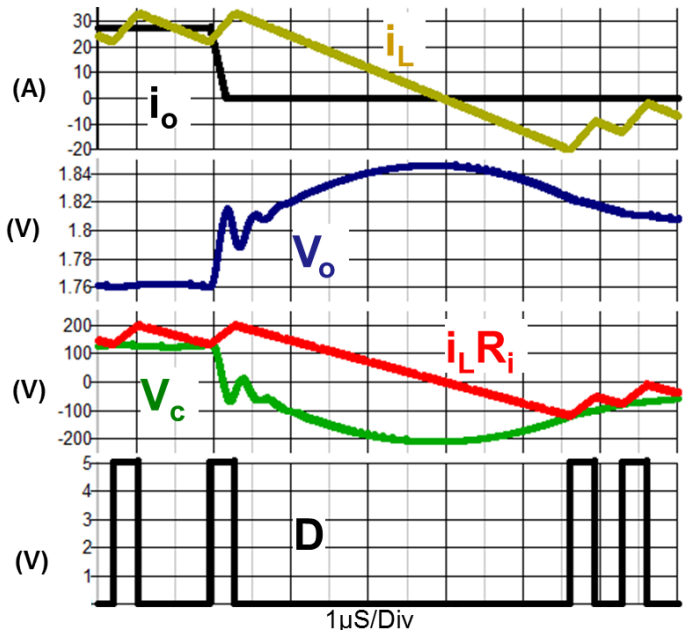
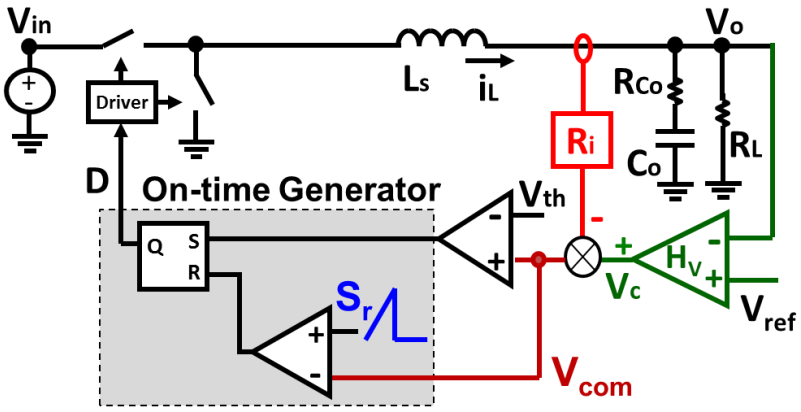


Figure 1.24 Step-down load transient response of COT control

To improve the transient response of COT control, ramp pulse modulation (RPM) has been proposed, and the block diagram for this is shown in Figure 1.25(a) [A.49][A.50][A.51][A.52]. Both the on-time and off-time of RPM control are modulated with V_{com}, which is the voltage difference of V_c and the inductor current feedback ($i_L \cdot R_i$). The turn-on instance of D is determined by comparing V_{com} with a fixed V_{th}, where the V_{com} slope in the T_{off} period comes from the falling slope (S_f) of $i_L \cdot R_i$, which is $V_o/L_s \cdot R_i$. Then, the turn-off instance of D is

determined by comparing V_{com} with a fixed ramp (S_r) in the on-time generator, where the V_{com} slope in the T_{on} period comes from the rising slope (S_n) of $i_L \cdot R_i$, which is $(V_{in}-V_o)/L_s \cdot R_i$. Figure 1.25 can be degenerated into COT control, when S_r is compared with a fixed V_{th} threshold instead of V_{com}.



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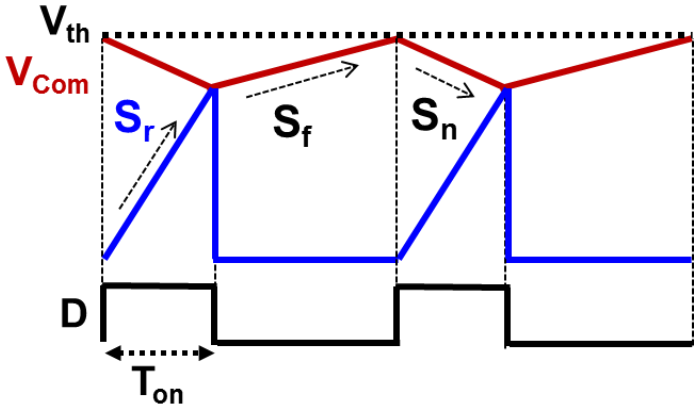


(b)

Figure 1.25 RPM current-mode control: (a) control structure, and (b) operation principle

The small circuit difference actually improves the transient response significantly. Since T_{on} can be adjusted by V_{com}, RPM control results in less of a V_o spike. As shown in Figure 1.26,

when a step-down load occurs at the rising edge of D, V_{com} intersects with S_r earlier to truncate the T_{on} pulse, so the V_o overshoot becomes smaller. In a similar manner, RPM minimizes the V_o undershoot with a native T_{on} extension. Therefore, RPM control can save more output capacitors than COT control.

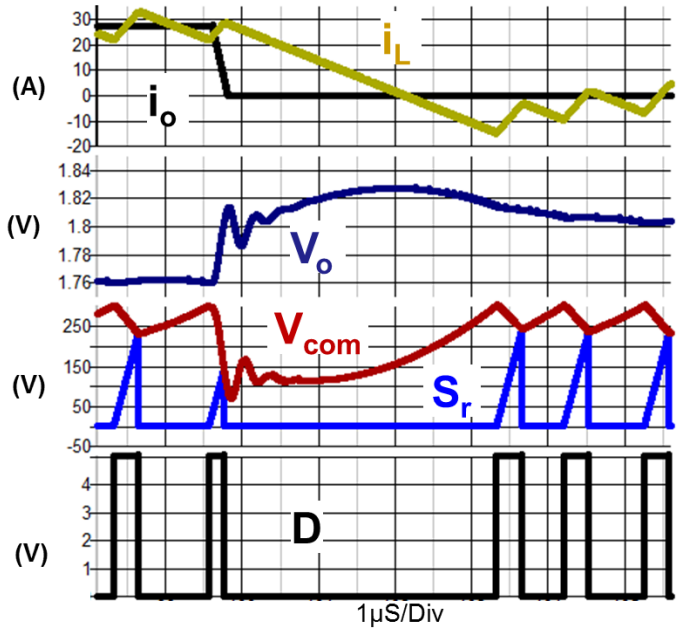


Figure 1.26 Step-down load transient of RPM current-mode control

However, while RPM control solves the transient limitation of COT control, other issues still remain. Therefore, it is desirable to investigate better variable-frequency control with constant steady-state f_{sw} over possible parameter variations, simple interleaving for multiphase systems, and easy synchronization with other VRs.

1.3 Dissertation Outline

This dissertation is organized into five chapters.

Chapter 1 is the introduction of the research background. Current-mode control has been widely used to achieve AVP for powering microprocessors. Current-sensing accuracy and constant impedance design are the two key factors to meet AVP requirements. The inductor DCR current-sensing technique is widely used, but the accuracy of the current sensing is very sensitive to component tolerance. Moreover, high-BW design has become a critical specification to reduce output capacitors used in a multiphase VR. For constant-frequency control, the vicinity effect of a double pole at $f_{sw}/2$ is the bottleneck of high-BW design. Comparatively, variable-frequency control natively pushes the double pole away from $f_{sw}/2$ to enable higher BW design. However, f_{sw} variation, interleaving, and beat frequency ripple become obstructions for wide adoption. Therefore, the research goal is to discover a new adaptive current-mode control scheme equipped with the following features: (1) auto-compensation of the sensing error from the DCR current-sensing network; (2) higher-BW design considering parametric variations; (3) constant steady-state f_{sw} under different operating conditions; (4) a simple interleaving structure with quick response to fast load transient; (5) easy synchronization with other VRs to eliminate the beat frequency ripple.

In Chapter 2, the impact of DCR current-sensing error is analyzed with the proposed equivalent circuit model, and the sensing error is compensated with the proposed auto-tuning method. The accuracy of DCR current sensing relies on the time constant matching between the output inductor and the current-sensing network. Due to component tolerance, time constant mismatch causes the BW to be shifted to lower frequency, so high peaking of output impedance

appears. The issue impacts both constant-frequency control and variable-frequency control, so it needs to be tackled at the beginning. Therefore, a non-ideal voltage-controlled current source model is proposed to predict the effect of time constant mismatch on current mode control. Then, a simple auto-tuning technique based on a unique pole-zero compensation is presented to correct the mismatch, so the output capacitor does not be overdesigned for the worst case.

In Chapter 3, a novel adaptive control for external ramp compensation is proposed to solve the BW limitation of constant-frequency control. The proposed control scheme maintains a peak phase margin in high-BW design by controlling constant damping of the double pole at $f_{sw}/2$. Both analog and digital implementations are provided with the circuit design guidelines. Then, two multiphase configurations are developed, an individual-control structure and a pulse-distribution structure, using which a trade-off between circuit simplicity and performance is discussed.

In Chapter 4, a frequency-regulation loop with adaptive phase-lock loop (PLL) is proposed to solve the design challenges of variable-frequency control. The PLL loop achieves constant f_{sw}, interleaving, and frequency synchronization. However, a stability issue of the PLL loop is encountered with certain parameter variations, which make loop compensation difficult. Therefore, the PLL is modeled based on a describing function such that the stability criteria can be identified. Then, enlightened by the proposed model, a simple adaptive control is proposed to make the stability margin of PLL loop insensitive to the parameter changes. Next, the benefit of natural overlapping feature is introduced for variable-frequency control interleaving with the proposed PLL, and the issue in the circuit complexity is addressed.

In Chapter 5, a hybrid interleaving structure is explored to simplify the implementation in multiphase operation. At the beginning, an alternative interleaving without using PLL, called a pulse distribution structure, is reviewed, and the limitation in multiphase operation is discussed. Then, it is found that combining adaptive PLL with pulse distribution structure can obtain balanced performance of the two. Basically, not only can the number of adaptive PLL loop and the related compensation network be significantly reduced, but the proposed structure also has a comparable transient response and high-BW design.

Chapter 6 provides conclusions of the work with the summary of actions taken and the directions for future work.

Chapter 2. Improving Accuracy of Inductor DCR Current Sensing

Current sensing accuracy is the key precondition of every control scheme to meet the stringent AVP requirements. Although lossless DCR current sensing has been widely used, it is very sensitive to component tolerance. Therefore, this chapter introduces a novel auto-tuning technique to compensate the effect of tolerance on AVP response. The beginning of this chapter identifies the design issues associated with current-mode control with DCR current sensing, based on proposed equivalent circuit model. Then, enlightened by the proposed model, an auto-tuning method is proposed. Finally, the auto-tuning system is designed and verified with simulations and hardware experiments.

2.1 Design Challenges Associate with DCR Current Sensing

The effect of a time constant mismatch has been observed in the time domain [A.35], but it is not clear how the mismatch impacts the small-signal property in high-BW design. A small-signal model for peak-current-mode control with DCR current sensing has also been investigated [B.1][B.2], which is based on the modified average model of R. Ridley [B.3]. However, it is found that Ridley's model cannot be justified for variable-frequency current-mode control, so a generic non-ideal voltage-control current source model has been proposed in [A.40] and [A.41]. Unfortunately, the model is derived based on ideal current sensing. Therefore, the extension of the model into DCR current sensing is investigated below.

2.1.1 Proposed Equivalent Circuit Model to Analyze DCR Current Sensing

For modeling purposes, the transfer function of H_i from the inductor current (i_L) to the output of the current sensor (V_i) is mathematically broken down into two terms as:

$$H_i(s) = R_{ip} + R_{ik} \cdot \frac{1}{s\tau_{Cs} + 1} \tag{2.1}$$

where $R_{ip}=A_iR_{Ls}\bullet(\tau_{Ls}/\tau_{Cs})$, and $R_{ik}=A_iR_{Ls}\bullet(1-\tau_{Ls}/\tau_{Cs})$. The first term ($R_{ip}$) is a pure gain. The second term is a low-pass filter with a gain of R_{ik} and the corner frequency at $1/\tau_{Cs}$. Based on this understanding, the DCR sensing network in Figure 2.1 can be redrawn as the alternative representation in Figure 2.2. R_{ip} represents the proportional feedback of the inductor current, while the second term represents the filtered inductor current feedback.

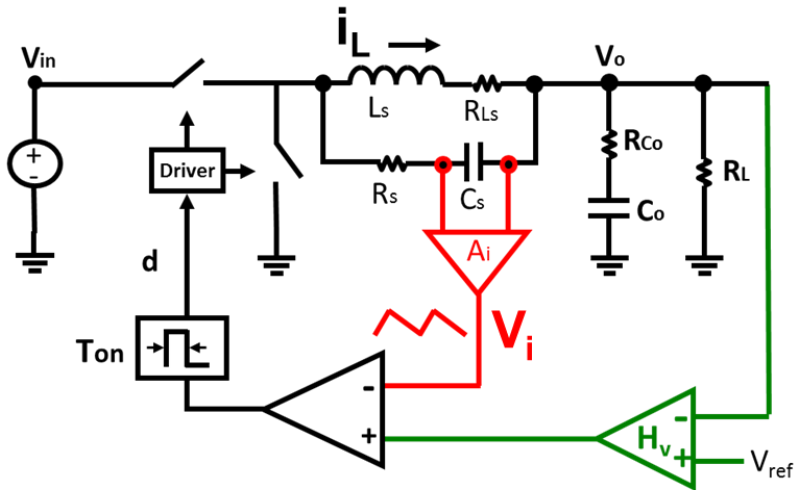


Figure 2.1 The DCR sensing network in current mode control

The proportional feedback loop passes all the sideband frequency components of i_L, but the low-pass filter loop provides strong attenuation to the sideband components, because the pole of τ_{Cs} in H_i is at very low frequency for practical design. For example, the pole is located at 267Hz,

when the power inductor SLC1175 from Coilcraft is used with L_s=150nH and R_{Ls}=0.252mΩ. As a result, the proportional feedback loop contributes to the effect of the sideband components, while it is reasonable to consider only the fundamental frequency for the low-pass filter loop.

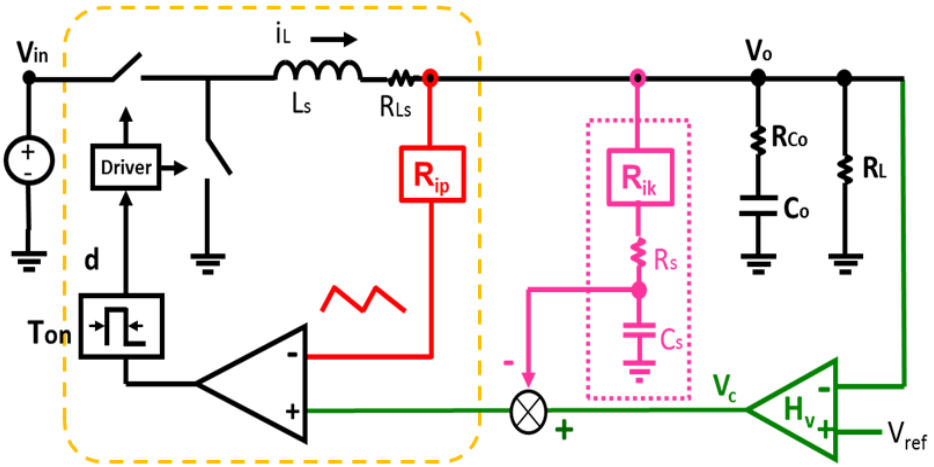


Figure 2.2 The alternative circuit representation of DCR sensing network

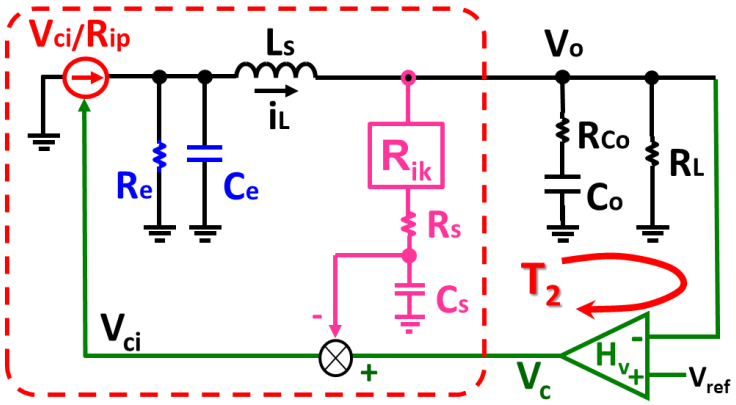


Figure 2.3 Proposed equivalent circuit model for current-mode control with DCR sensing

It is clear that the proportional feedback loop highlighted with the yellow dashed line is the same as the current-mode control with ideal current sensing, so the proportional feedback loop and switches can be substituted with the original non-ideal current source model. Then, the complete equivalent circuit model for current-mode control using DCR current sensing is

obtained, as shown in Figure 2.3. The $R_eC_eL_s$ resonant tank represents the effect of the sideband components on the i_L feedback though the DCR current sensor, while the low-pass filter loop represents the low-frequency effect of the DCR current sensing. Since the current gain becomes R_{ip}, the rising and falling current slopes on V_i for a buck converter are modified into:

$$s_{ni} = R_{ip}\frac{V_{in}-V_o}{L_s} = A_i\frac{V_{in}-V_o}{\tau_{Cs}} \tag{2.2}$$

$$s_{fi} = R_{ip}\frac{V_o}{L_s} = A_i\frac{V_o}{\tau_{Cs}} \tag{2.3}$$

Also, R_e and C_e are modified into the expressions in Table I.

Table 1 Parameters of proposed equivalent circuit model for DCR sensing

Modulation	R_e	C_e
Constant On-time Current Mode	$\frac{2L_s}{T_{on}}$	$\frac{T_{on}^2}{L_s\pi^2}$
Constant Off-time Current Mode	$\frac{2L_s}{T_{off}}$	$\frac{T_{off}^2}{L_s\pi^2}$
Constant-Frequency Peak Current Mode	$\frac{L_s}{T_{sw}\left[\frac{s_e+s_{ni}}{s_{ni}+s_{fi}}-0.5\right]}$	$\frac{T_{sw}^2}{L_s\pi^2}$
Constant-Frequency Valley Current Mode	$\frac{L_s}{T_{sw}\left[\frac{s_e+s_{fi}}{s_{ni}+s_{fi}}-0.5\right]}$	$\frac{T_{sw}^2}{L_s\pi^2}$

SIMPLIS simulation is performed to verify the proposed model for COT control. The parameters of the buck converter are as follows: V_{in}=12V, V_o=1.8V, f_{sw}=800kHz, L_s=150nH,

R_{Ls}=0.5mΩ, A_i=12, R_s=3kΩ, C_s=0.1μF, and C_o=36·22μF (ceramic). The control-to-output-voltage transfer function is plotted with the simulation results, when τ_{Cs} is +/-40% away from τ_{Ls}. As shown in Figure 2.4, proposed model accurately predicts the time constant mismatch effect.

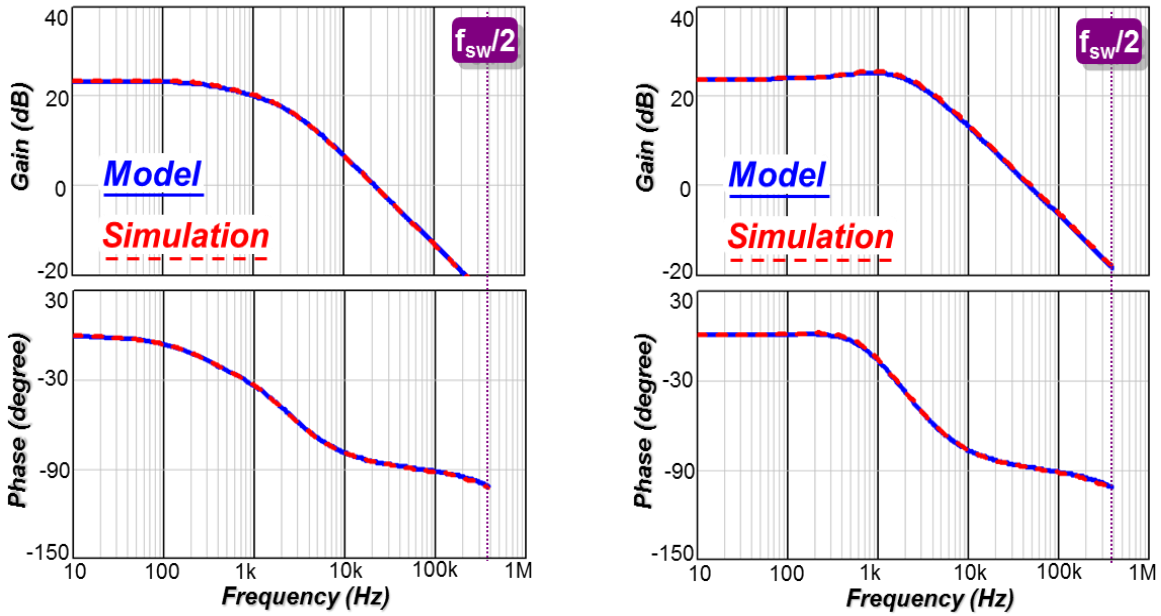


Figure 2.4 Control-to-output transfer function comparison: (a) τ_{Cs}=0.6·τ_{Ls}, and (b) τ_{Cs}=1.4·τ_{Ls}

2.1.2 The Impact of Time Constant Mismatch on Constant On-Time Control

Based on the proposed equivalent circuit model, the control-to-output-voltage transfer function of constant on-time current mode (COT) control is calculated as:

$$\frac{V_o(s)}{V_c(s)} \approx \frac{R_L}{A_i R_{Ls}} \frac{s\tau_{Cs}+1}{s\tau_{Ls}+1} \frac{R_{Co}C_o s+1}{R_L C_o s+1} \frac{1}{1+s/(\omega_1 Q_1)+s^2/\omega_1^2} \tag{2.4}$$

where A_i is current sensing amplifier, R_{Ls} is inductor DCR, R_L is the load resistor, C_o is the capacitance of the output capacitor, R_{Co} is the equivalent-series resistance (ESR) of the output capacitor, $\omega_1 = \pi/T_{on}$, and $Q_1 = 2/\pi$.

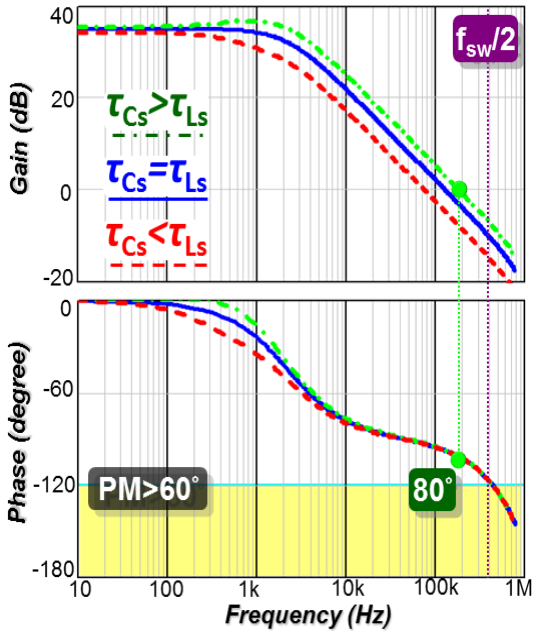


Figure 2.5 Effect of time constant mismatch on T_2 of COT control

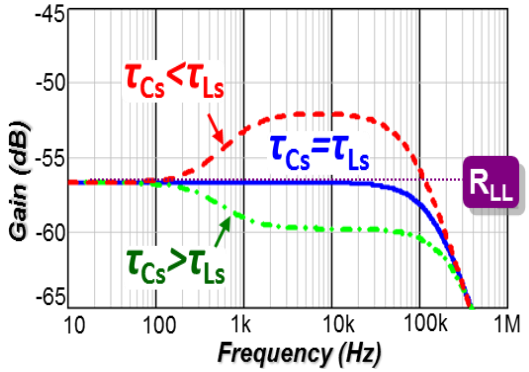


Figure 2.6 Effect of time constant mismatch on Z_{oc} of COT control

Equation (2.4) shows that the time constant mismatch does not affect the double pole characteristic of COT control, but only the pole-zero pair of H_i is inversed and appears in (2.4).

In small D operation, the double pole is located much higher than $f_{sw}/2$, so the effect on V_o/V_c can be neglected. In addition, T_2 is the product of V_o/V_c and the outer-loop compensation (H_v). Conceptually, to achieve AVP in current-mode control, the H_v compensation is a low-pass filter with finite-gain (K_v) and the corner frequency at the ESR zero of the output capacitor [A.41], which is expressed as:

$$H_v(\mathrm{s}) = K_v \frac{1}{1+R_{Co}C_o s} \tag{2.5}$$

As shown in Figure 2.5, the Bode plot of T_2 shows the pole-zero pair shifts the BW, when there is a time constant mismatch. It is possible for the BW to be moved less than the minimum requirement of 100kHz in the VR12.5 specification [A.20]. For example, when τ_{Cs} is 40% less than τ_{Ls}, the BW is shifted from 135kHz to 70kHz.

Next, to understand the effect of BW shifting on the AVP response, the output impedance (Z_{oc}) with both current and voltage feedback loops closed is calculated as:

$$Z_{oc}(\mathrm{s}) = \frac{Z_{oi}(\mathrm{s})}{1+T_2(\mathrm{s})} \tag{2.6}$$

where Z_{oi} is the output impedance with a closed current feedback loop. Z_{oi} can be expressed as:

$$Z_{oi}(\mathrm{s}) \approx \frac{R_L(R_{Co}C_o s+1)}{1+R_L C_o s} \tag{2.7}$$

By substituting (2.4) and (2.5) into (2.6), the Z_{oc} expression in low-frequency approximation can be simplified as:

$$Z_{oc}(\mathrm{s}) \approx \frac{A_i R_{Ls}}{K_v}\left(\frac{s\tau_{Ls}+1}{s\tau_{Cs}+1}\right) \tag{2.8}$$

First of all, the model indicates that the ratio between A_iR_{Ls} and K_v should be equal to R_{LL}, such that the low frequency property of Z_{oc} can be equal to R_{LL}. Secondly, it shows that the pole-zero pair of H_i is not inverted in the Z_{oc} expression, but is inverted in the T_2 expression. Therefore, when $\tau_{Cs}<\tau_{Ls}$, the gain of T_2 in Figure 2.5 is shifted lower, but Z_{oc} in Figure 2.6 is shifted higher than R_{LL} which causes transient overshoot and undershoot. Then, the output capacitors have to be overdesigned to minimize the transient spike. On the other hand, when $\tau_{Cs}>\tau_{Ls}$, Z_{oc} shifting lower than R_{LL} causes a long settling time in AVP response, because τ_{Cs} determines the dominant-pole frequency in the Z_{oc} expression.

2.1.3 The Impact of Time Constant Mismatch on Constant-Frequency Control

Based on the proposed equivalent circuit model, the control-to-output-voltage transfer function for peak-current mode (PCM) control is derived as:

$$\frac{V_o(\mathrm{s})}{V_c(\mathrm{s})} \approx \frac{R_L}{A_i R_{Ls}}\frac{s\tau_{Cs}+1}{s\tau_{Ls}+1}\frac{R_{Co}C_o s+1}{R_L C_o s+1}\frac{1}{1+s/(\omega_2 Q_2)+s^2/\omega_2^2} \tag{2.9}$$

where $\omega_2=\pi/T_{sw}$, and $Q_2=1/\{\pi[(S_{ni}+S_e)/(S_{ni}+S_{fi})-0.5]\}$. The double pole ($\omega_2$) is always located at $f_{sw}/2$, but the quality factor (Q_2) is affected by τ_{Cs} tolerance because S_{ni} and S_{fi} are inverse proportional to τ_{Cs}.

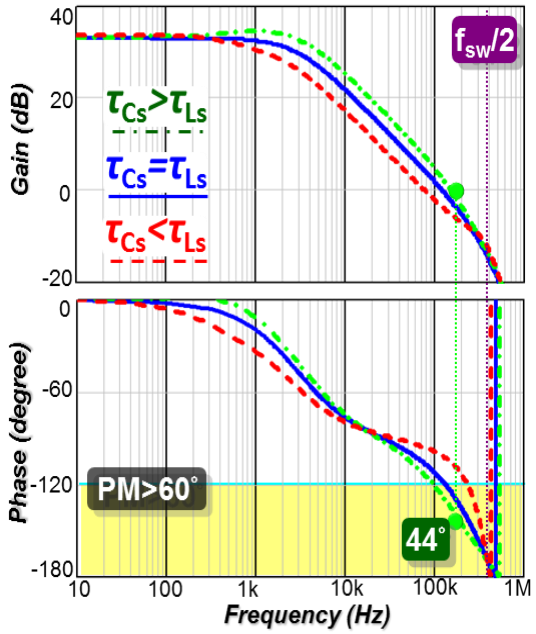


Figure 2.7 Effect of time constant mismatch on T_2 of PCM control

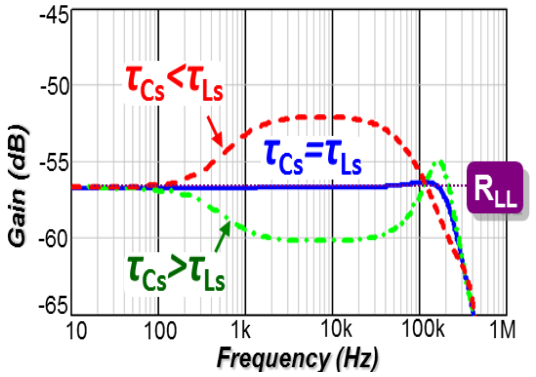


Figure 2.8 Effect of time constant mismatch on Z_{oc} of PCM control

Compared with COT control, the time constant mismatch in PCM control not only introduces an additional pole-zero pair from H_i, but also changes Q_2 of its double pole. As shown in Figure 2.7, when τ_{Cs} is 40% less than τ_{Ls}, the BW is shifted less than 100kHz, and the PM increases with higher Q_2. When τ_{Cs} is 40% larger than τ_{Ls}, BW is shifted higher, and PM drops with lower Q_2. The Bode plot of Z_{oc} in Figure 2.8 shows the impedance peaking appears in both

mismatch cases. When $\tau_{Cs}<\tau_{Ls}$, Z_{oc} peaking appears, because of the pole-zero pair. When $\tau_{Cs}>\tau_{Ls}$, Z_{oc} peaking appears at the crossover frequency, because Q_2 reduction causes PM<60°.

2.2 Review of State-of-the-Art DCR Current Sensing

The concept of tuning τ_{Cs} to approach actual τ_{Ls} has been proposed to correct the time constant mismatch such that the τ_{Cs} pole cancels the τ_{Ls} zero [B.4][B.5][B.6][B.7]. The mismatch condition is identified by detecting the slope of V_i (dV_i/dt) with an analog-to-digital converter (ADC), and then τ_{Cs} is tuned gradually till dV_i/dt is close to zero, as shown in Figure 2.9.

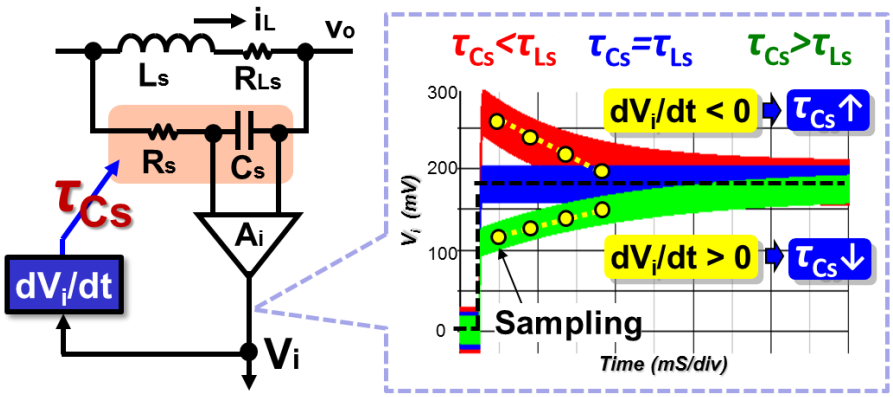
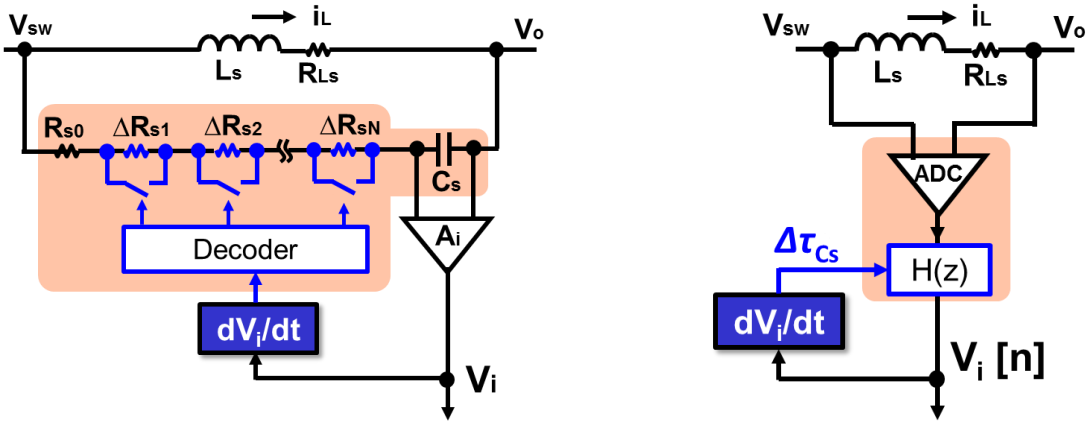


Figure 2.9 Block diagram of state-of-the-art auto-tuning for DCR current sensing

In a mixed-signal implementation, a switched-resistor bank is used as a variable R_s to tune τ_{Cs} of each phase, as shown in Figure 2.10(a) [B.4][B.5][B.6]. The polarity of dV_i/dt determines the change of equivalent R_s. There are four drawbacks that make monolithic integration difficult and complex for a multiphase VR: First, the tuning resolution can change a lot depending on the tolerance of the integrated resistor [B.8], so the sensed dV_i/dt is difficult to converge close to zero. Second, multiple resistor banks are required for a multiphase VR, so the bulky resistors occupies a great deal of the die size. Third, careful isolation between the resistor bank and other

noise-sensitive circuits is required to avoid noise coupling from multiple high-dV/dt nodes among the resistor interconnections, since those resistors are connected to the switching node of the DC/DC converter (V_{sw}). Fourth, multiple ADCs in a multiphase VR are required to sense the V_i slope of each DCR sensor separately.

In a fully digital implementation, an ADC and a digital H(z) filter are used to replace the bulky and noisy switched-resistor bank into a digital control algorithm, so tuning τ_{Cs} becomes simpler, as shown in Figure 2.10(b) [B.7]. The polarity of dV_i/dt determines the change of the τ_{Cs} parameter in the digital filter. However, there are two drawbacks which limit the AVP response: First, multiple high-resolution ADCs are required to ensure the accuracy of load-line regulation for a multiphase VR. Second, the sampling-rate of ADC limits the control BW and AVP response [B.9]. In addition, it is only applicable for digital current-mode controllers.



(a) (b)

Figure 2.10 Implementation of the tunable actuator: (a) analog version, and (b) digital version

2.3 Proposed Auto-Tuning to Correct Time Constant Mismatch

2.3.1 Operating Principle

A new auto-tuning method is proposed based on the impedance compensation technique to maintain good AVP response under any mismatch condition. Enlightened by the proposed model in (2.8), a simple tunable compensator (H_{Com}) is used to create another pole-zero pair to make the product of the two pole-zero pairs close to 1 such that the resultant Z_{oc} is close to R_{LL}.

$$Z_{oc} \approx R_{LL}\left(\frac{s\tau_{Ls}+1}{s\tau_{Cs}+1}\right)H_{Com} \tag{2.10}$$

The block diagram of the proposed auto-tuning system is shown in Figure 2.11. H_{Com} is placed at the output of the DCR sensor. Inside H_{Com}, a high-pass RC filter and a variable-gain amplifier (A) generate an internal compensation signal which shapes original current feedback signal (V_i). Then, V_i plus the compensation signal becomes a modified current feedback signal (V_i'). The transfer function of H_{Com} can be expressed as follows:

$$H_{Com} = \frac{sRC(1+\mathrm{A})+1}{sRC+1} \tag{2.11}$$

The pole position is predetermined by R and C, while the zero position is made variable by changing A. When A=0, H_{Com} does not affect Z_{oc}. When A increases, the compensation zero moves to a lower frequency, so H_{Com} keeps shaping Z_{oc} close to R_{LL}. A is adjusted gradually based on the polarity of dV_o/dt, because a Z_{oc} characteristic can be estimated by sensing dV_o/dt. As shown Figure 2.11, when $Z_{oc}<R_{LL}$, the slow response makes $dV_o/dt<0$. When $Z_{oc}>R_{LL}$, the V_o

undershoot makes $dV_o/dt>0$. The dV_o/dt calculation is initiated when a step-up load transient is detected though V_i'.

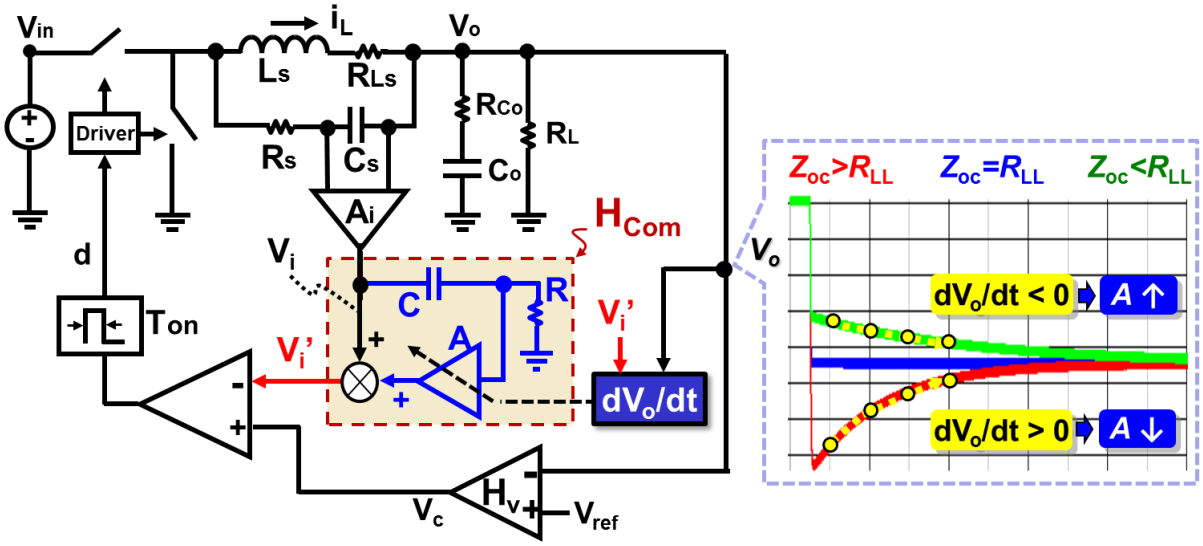
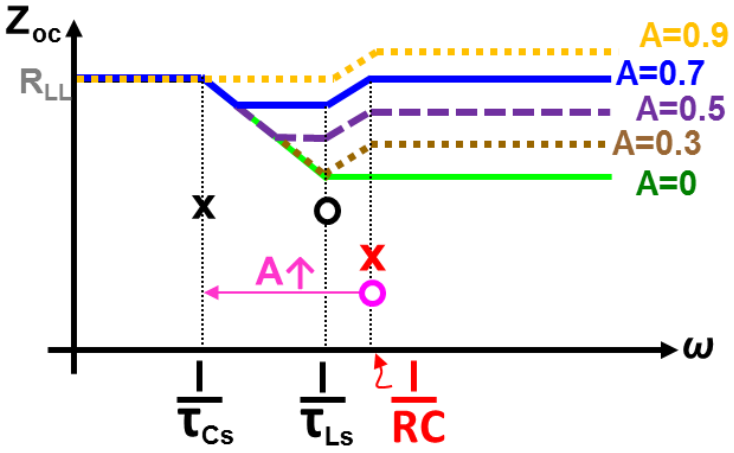


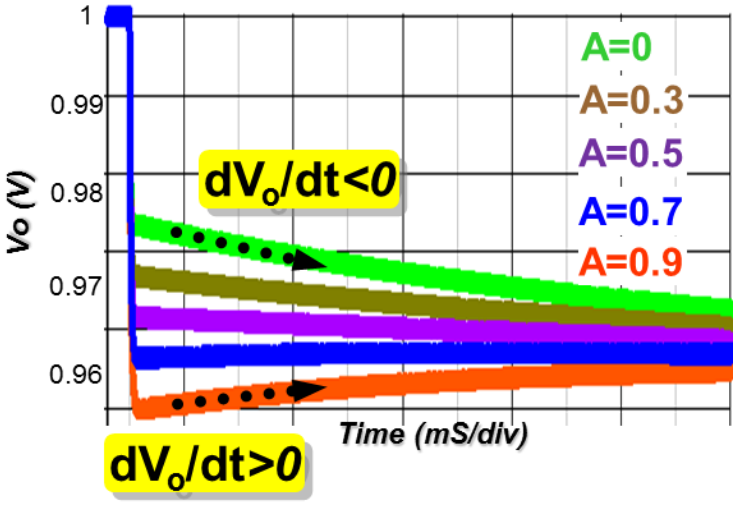
Figure 2.11 The block diagram of the proposed auto-tuning for DCR current sensing

The compensation principle is explained by the asymptotic Bode plot of Z_{oc} in Figure 2.12(a) as well as the V_o waveform during the step-up load transient in Figure 2.12(b). Firstly, to prevent undershoot at the beginning of the tuning process, τ_{Cs} is purposely designed to be higher than τ_{Ls}, so the worst-case Z_{oc} at A=0 is less than R_{LL}. Secondly, the time constant of RC in H_{Com} is chosen within the τ_{Ls} tolerance range. Thirdly, when dV_o/dt is negative in every step-up load transient, A increases a bit to move the compensation zero toward the pole of τ_{Cs}, so Z_{oc} approaches R_{LL}. When A increases to 0.7, Z_{oc} in most frequency ranges has been compensated to R_{LL} except for a small dip on Z_{oc} between the τ_{Cs} pole and the compensation pole (1/RC), because the two pole-zero pairs are not in full cancellation. When A=0.7, dV_o/dt is close to zero but is still negative, so A keeps increasing to 0.9. When A=0.9, Z_{oc} peaking occurs, and the positive dV_o/dt provides an indication of overcompensation. Fourthly, when dV_o/dt becomes

positive, A reduces back to 0.7 and the tuning is finished. Tuning will be initiated again if dV_o/dt turns into positive slope.



(a)



(b)

Figure 2.12 Effect of H_{Com} on: (a) Z_{oc}, and (b) AVP response in step-up load

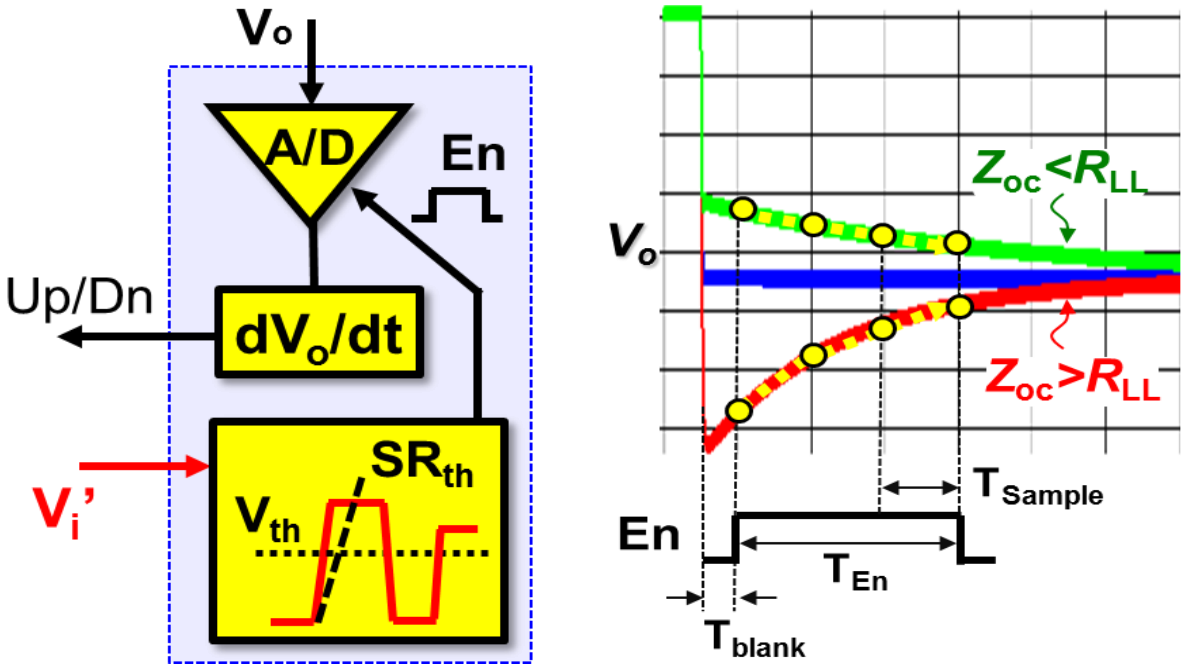
The first benefit of the proposed method is that Z_{oc} can be compensated to be close to R_{LL} without perfect cancellation, since the AVP response in A=0.7 is fast enough to meet the transient requirement. Even though there are component tolerances of R and C in H_{Com}, A will

always increase to a point at which $dV_o/dt \approx 0$. The second benefit is the simplicity of the compensation network, since the variable-gain amplifier is more accurate and occupies less of the die size than the switched resistor bank. The third benefit of this method is that it solves the noise issue of the current state-of-the-art method, since the compensation is performed at the output of DCR sensing. The fourth benefit is the simplicity of mismatch detection, since only one detection circuit is needed to calculate dV_o/dt, instead of detecting dV_i/dt in each phase.

2.3.2 Circuit Design Consideration

There are two simple implementations of a variable-gain amplifier which are suitable for the proposed auto-tuning. One uses a simple switched-current mirror bank to adjust the output stage of an operational trans-conductance amplifier (OTA) [B.10][B.11]. Another uses a simple switched-current mirror bank to adjust the bias current of the differential pair in the input stage of an OTA [B.12]. In addition, the frequency response of the amplifier that is higher than T_2 BW is enough to compensate the mismatch effect, so the cost of the variable-gain amplifier can be reduced.

An example implementation of the slope detector is shown in Figure 2.13(a). When a step-up transient event is identified at V_i' whose magnitude is larger than V_{th} and slew rate is higher than SR_{th}, an enable signal (En) held in a predetermined period (T_{En}) is sent to an ADC to trigger dV_o/dt calculation after the blanking time of T_{blank}. The simulation of the sampling sequence in Figure 2.13(b) shows T_{blank} avoids an initial voltage spike, and then several samples of V_o are taken by ADC in the T_{En} period. If another transient event occurs before the end of the T_{En} period, the dV_o/dt calculation result will be discarded, and A will not change.

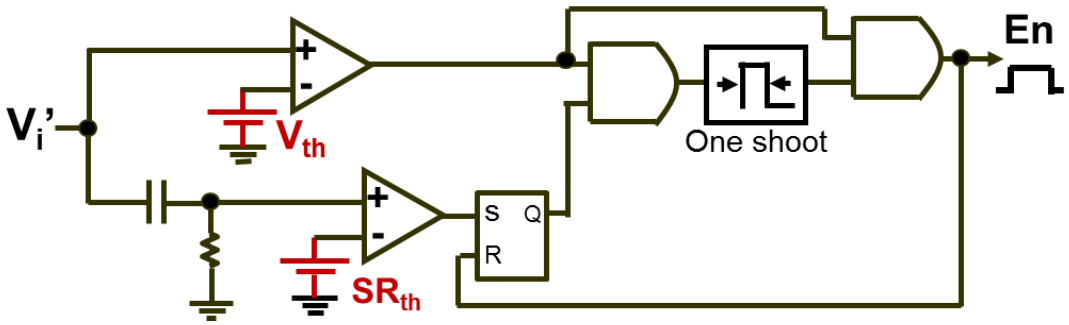


(a) (b)

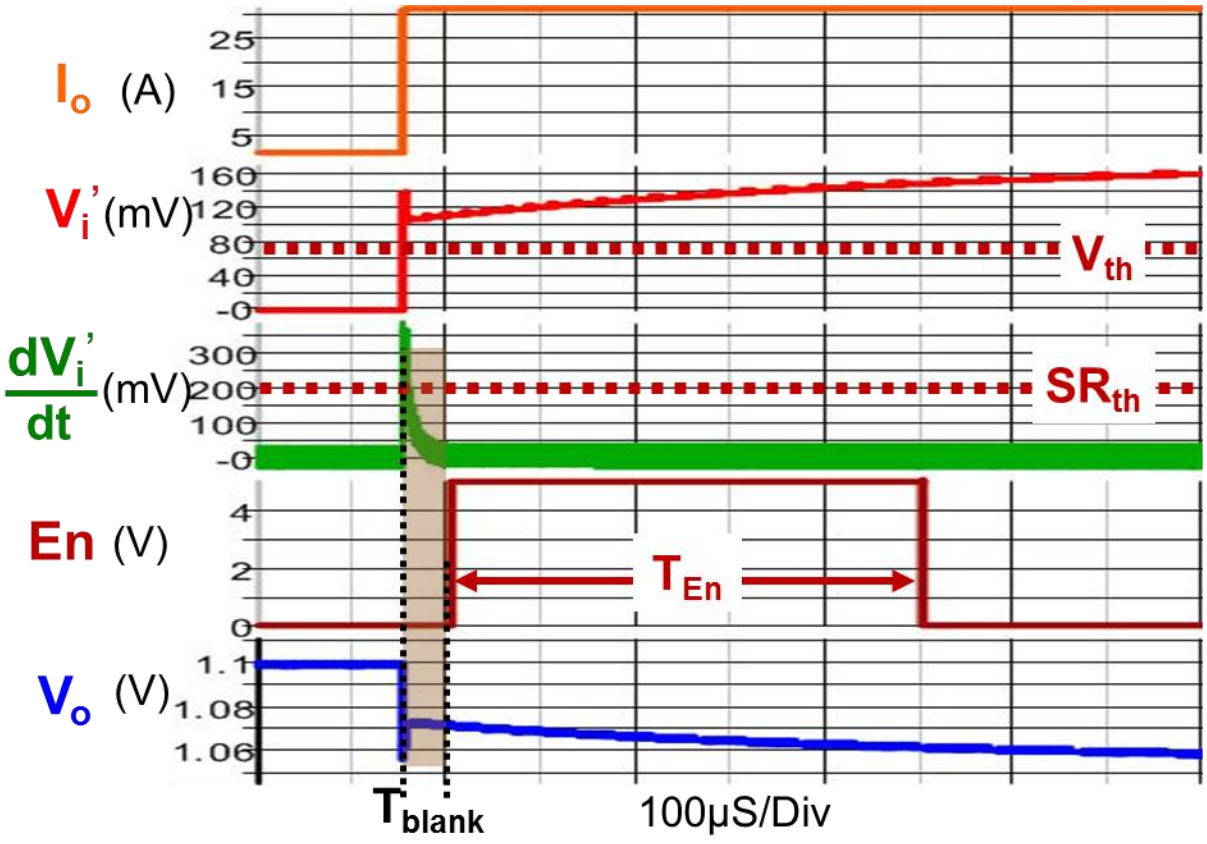
Figure 2.13 Implementation of the slope detector: (a) block diagram, and (b) sampling sequence

In the slope detector, the step-up transient is identified from V_i' by the simple circuit in Figure 2.14(a) which contains two comparators: one to check the magnitude change, another to check the slew rate. The simulation of the identification sequence in Figure 2.14(b) shows the En signal is high only when the change in V_i' exceeds the two threshold values. For multiphase operation, V_i' can be connected to ether the current feedback of one phase or the summed current feedback signal of all phases. T_{En} is set by the one-shot pulse generator in Figure 2.14(a). Since τ_{Cs} is the dominant pole of Z_{oc}, $T_{En} \geq \tau_{Cs}/2$ is suggested to more easily catch the slope change. For example, when R_s=3kΩ and C_s=0.1μF, $T_{En} \geq 150\mu S$ and $T_{Sample} \geq 30\mu S$. According to the VR12.5 specifications in [A.14][A.20], the frequency range of the CPU repetitive load transient is

between 300Hz to 1MHz, which means the timing of load step-up event T_H lasts between 1.6mS to 0.5μS, so $T_{En} \geq 150\mu S$ is practical.



(a)



(b)

Figure 2.14 The identification of step-up load transient: (a) circuit diagram, and (b) simulation results

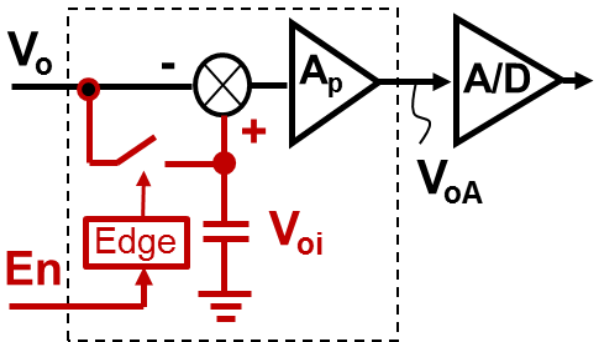
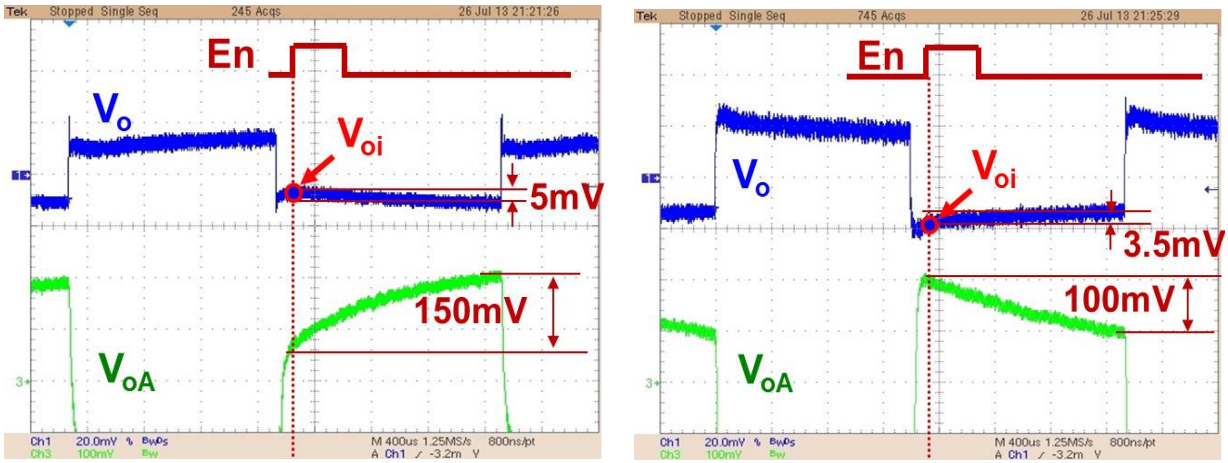


Figure 2.15 Circuit diagram of proposed preconditioning for V_o sampling



(a) (b)

Figure 2.16 The measurement results of preconditioned V_o: (a) $Z_{oc}<R_{LL}$, and (b) $Z_{oc}>R_{LL}$

To avoid using high-resolution ADC for sampling the V_o waveform, signal preconditioning at the first stage of the ADC before quantization is useful. A simple and useful preconditioning circuit is proposed, which allows using an 8-bit ADC to perform V_o sample. The circuit diagram is shown in Figure 2.15. First, a switched-capacitor stores the initial value V_{oi} in step-up load transient, triggered by the rising edge of En. Then, the value is subtracted with the V_o waveform to cancel the bias. After that, the difference voltage is scaled by the error amplifier, A_p. The measurement result in Figure 2.16 shows that even though there is only 5mV difference in the V_o

transient waveform under a slight time-constant mismatch, the magnitude of preconditioned signal V_{oi} is still large enough, at 150mV when A_P=30. Therefore, an eight-bit ADC is enough to identify the polarity of dV_o/dt.

2.3.3 Verification

The inductor current of one phase in a desktop VR is measured, and the results are as shown in Figure 2.17. It is found that the pattern of the step-up load transient is unsymmetrical with different current levels and repetition frequencies. Some step-up load transients last more than 150μS after the CPU is powered on for 6 sec. Therefore, a simulation of the auto-tuning process is demonstrated based on the unsymmetrical load transient event, as shown in Figure 2.18. The simulation conditions are: V_{in}=12V, V_o=1V, R_{LL}=1.5mΩ, C_o=36·22μF (Ceramic capacitor), and f_{sw}=800kHz. The DCR sensing network is designed for $\tau_{Cs}>\tau_{Ls}$, where L=150nH, R_{Ls}=0.5mΩ, C_s=0.1μF, and R_s=5.3kΩ. The RC of H_{Com} is designed at a typ. value of τ_{Ls}, so C=680pF and R=440kΩ.

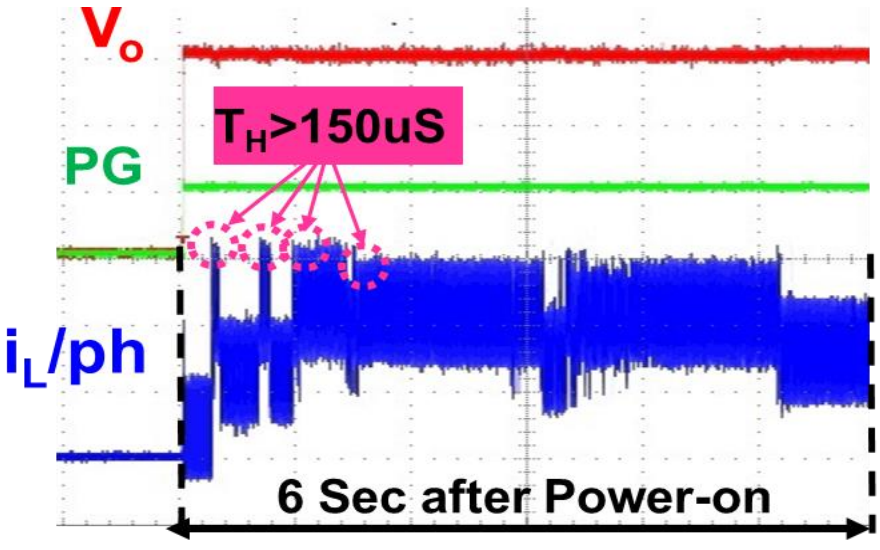


Figure 2.17 Load transient pattern of a desktop VR after V_o startup

(A) SIMPLIS simulation

The simulation starts with a worst-case component tolerance where the pole/zero pair of the DCR sensor is the farthest away from the pole/zero pair of H_{Com}: with τ_{Cs} increasing 15% and with τ_{Ls} increasing 20%. The variable A range of H_{Com} is 0~1.5 with an incremental change of 0.2. When the low-frequency load transient appears, the enable signal lasts 150μS and the initial $dV_o/dt<0$, so A increases gradually. When a high-frequency load transient appears, the enable signal lasts less than 150μS which is not long enough to identify dV_o/dt, so A does not change. Then, when A increases to 0.9 which makes $dV_o/dt>0$, A will decrease back to 0.7 and then the auto-tuning process is finished.

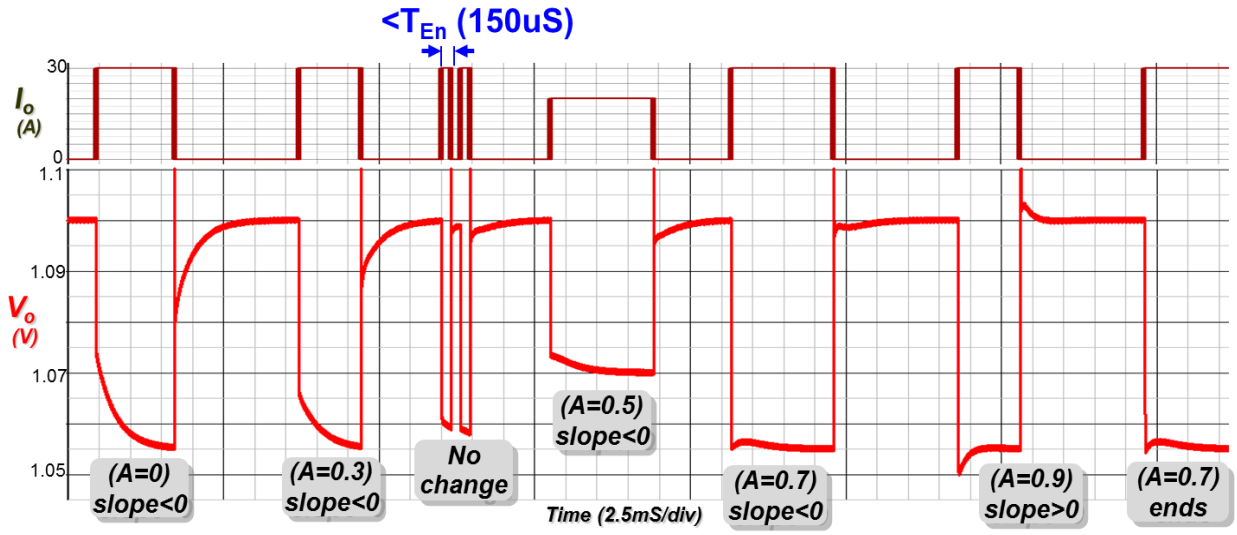
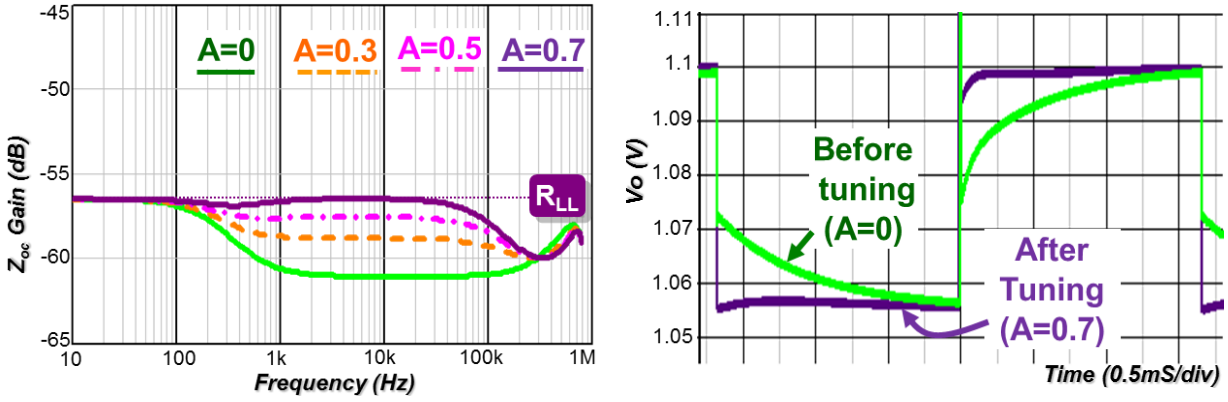


Figure 2.18 The simulation of auto-tuning process with unsymmetrical load transients

The simulation result in Figure 2.19 demonstrates that the proposed method maintains constant Z_{oc} and a fast AVP response under the worst mismatch conditions. Additionally, the reason of Z_{oc} dipping at A=0.7 is that the two pole-zero pairs in (2.10) are not completely

canceled. The dipping effect on Z_{oc} only introduces a small dynamic on the transient response with 2mV, which is acceptable within the tolerance band spec of +/-20mV in Figure 1.7.



(a) (b)

Figure 2.19 The simulation of auto-tuning performance on: (a) Z_{oc}, and (b) AVP response

(B) Experimental verification

As shown in Figure 2.20, the experimental platform includes a constant on-time controlled buck converter on the power board, a H_{Com} circuit on an analog control card, and a digital slope detector implemented on a Xilinx Spartan-3E FPGA board. The test conditions are: V_{in}=12V, V_o=1V, R_{LL}=1.9mΩ, f_{sw}=300kHz, and ΔI_o=15A. The DCR sensing network is designed for $\tau_{Cs}>\tau_{Ls}$, where L=360nH, R_{Ls}=0.825mΩ, C_s=33nF (X7R), and R_s=28kΩ. The RC of H_{Com} is designed at Typ. value of τ_{Ls}, so C=680pF (C0G) and R=640kΩ. The test result in Figure 2.21 shows that the proposed auto-tuning corrects the slow AVP response into fast settling time during several transient events after V_o startup. The comparison result in Figure 2.22 highlights the effectiveness of the proposed auto-tuning method.

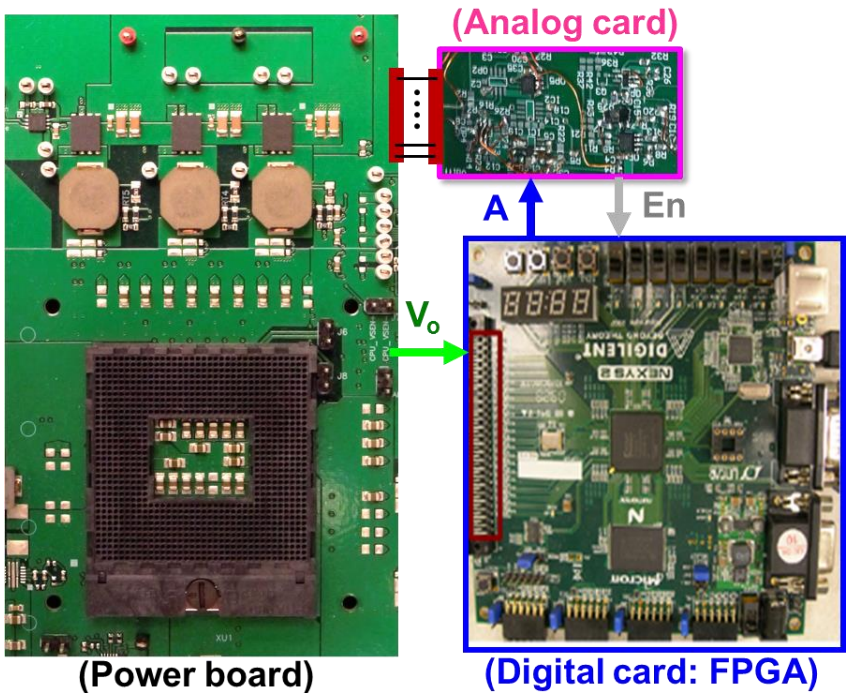


Figure 2.20 The experimental platform.

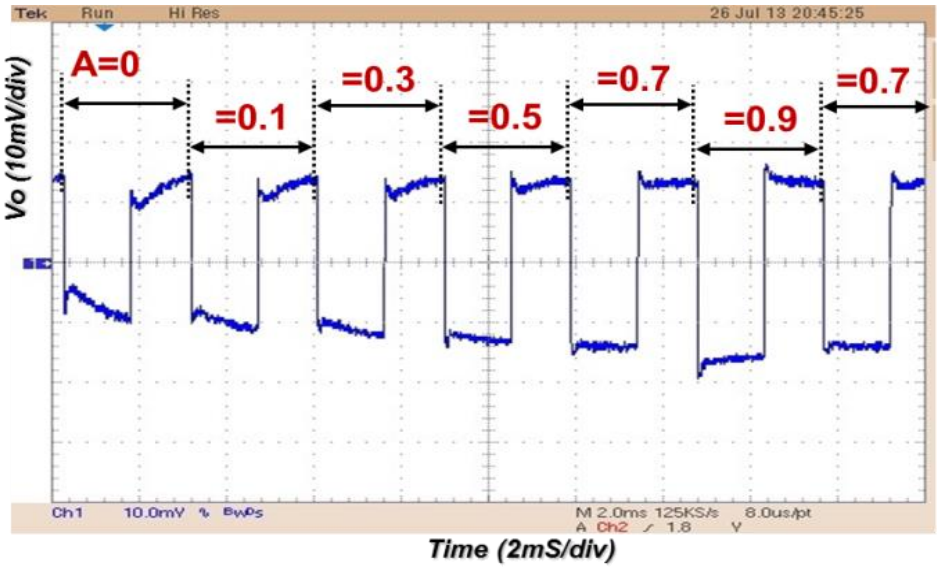


Figure 2.21 The measurement result of the auto-tuning process after V_o start-up

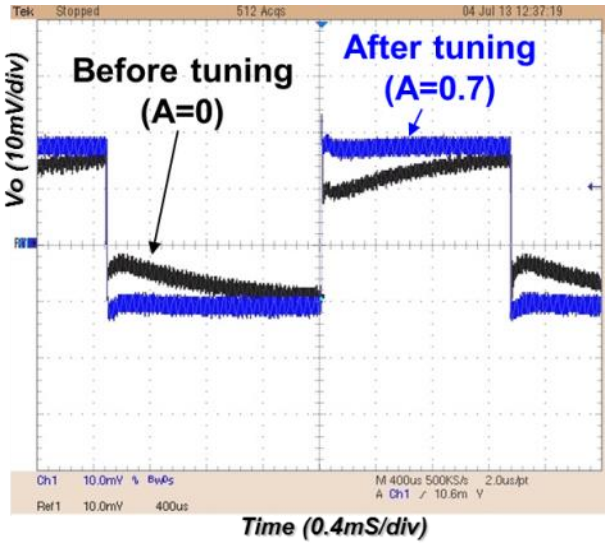


Figure 2.22 The measurement result of the auto-tuning performance

2.4 Summary

A time constant mismatch of DCR sensing impairs the AVP response. Based on conventional design guidelines for a DCR current sensor, more output capacitors may be needed to avoid a transient spike under the worst-case component tolerance. Therefore, a modified equivalent circuit model is proposed to predict the mismatch effect on loop gain and output impedance. Then, using this model, an impedance shaping technique is developed to solve the mismatch issue. Compared with the state-of-the-art auto-tuning method, the proposed method features easier tuning, better tuning performance, noise-free operation, and simpler implementation for monolithic integration. In the end, this method saves output capacitors and enables high BW design, while minimizing the circuit complexity. The improvement of current sensing accuracy is verified by both simulation and experimental results.

Chapter 3. Adaptive High-Bandwidth Constant-Frequency Control

As mentioned in Chapter 1, the damping effect of the double pole at $f_{sw}/2$ is the major bottleneck of constant-frequency control. At the beginning of this chapter, the current state-of-the-art ramp compensation techniques are reviewed and their limitations are identified. After that, a new method of adaptive current-mode control with unique external ramp compensation is proposed, which maintains a sufficient phase margin for high-BW design under various possible parameter variations. Finally, the system is modeled, designed, and verified with simulations and hardware experiments.

3.1 Review of State-of-the-Art Constant-Frequency Control

Since the issue of DCR current sensing is resolved in Chapter 2, the following analysis of the other issues in high-BW constant-frequency control is based on ideal current sensing. The equivalent circuit model in Chapter 2 can be simplified to Figure 3.1 [A.39][A.40][A.41]. The simplified T_2 loop gain is obtained by:

$$T_2(\mathrm{s}) \approx \frac{R_L}{R_i} \frac{\mathrm{R}_{Co}\mathrm{C}_o\mathrm{s}+1}{\mathrm{R}_L\mathrm{C}_o\mathrm{s}+1} \frac{H_v(\mathrm{s})}{1+\dfrac{s}{\omega_2 Q_2}+\dfrac{s^2}{\omega_2^{\,2}}} \tag{3.1}$$

where $\omega_2=\pi/T_{sw}$, and Q_2 is the quality factor of the double pole.

The Q_2 for peak current-mode (PCM) control is expressed as:

$$Q_2 = \frac{1}{\pi\left(\frac{s_n + s_e}{s_n + s_f} - 0.5\right)} \tag{3.2}$$

where $S_n=(V_{in}-V_o)R_i/L_s$ and $S_f=V_oR_i/L_s$ for a buck converter.

It is found that Q_2 is a critical design parameter for high-BW design. The T_2 characteristic with different Q_2 is plotted in Figure 3.2. If $Q_2>1$, the double pole peaking at $f_{sw}/2$ causes the secondary crossover without sufficient PM. On the other hand, if $Q_2<1$, the PM is also reduced, because of over-damping. However, (3.2) indicates there are several parameters that can affect Q_2: external ramp compensation (S_e), operating conditions (V_{in} and V_o), and component variations (R_i and L_s).

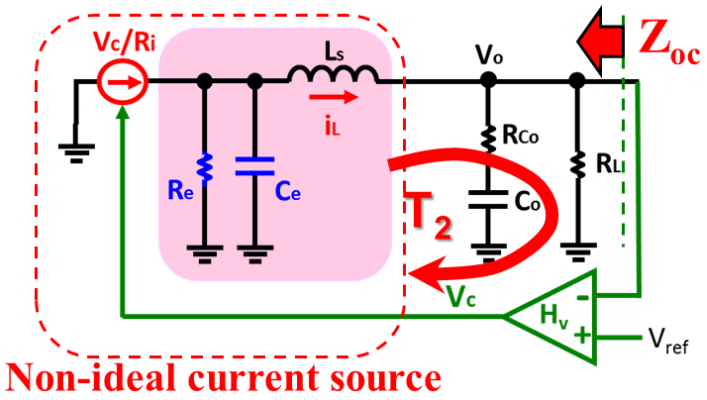


Figure 3.1 Equivalent circuit model of constant-frequency control with ideal current sensing [A.40]

S_e is the only design possibility for the control loop to affect Q_2. Figure 3.3(a) highlights the importance of S_e design at $D\approx0.4$ ($V_{in}=5.2V$ and $V_o=2V$), where a small S_e results in a high double-pole peaking, and a large S_e results in poor PM. Unfortunately, it is very difficult to

design a fixed S_e for different operating conditions, since Q_2 varies when V_{in} and V_o change. Assuming that the fixed S_e is equal to $0.9 \cdot S_f$ when D=0.2, Q_2 jumps higher than 1 when D=0.4, and Q_2 drops lower than 0.6 when D=0.06. It is impossible to anchor T_2 BW at $f_{sw}/6$, as shown in Figure 3.3(b). Therefore, it is critical to adaptively adjust S_e to optimize the loop compensation.

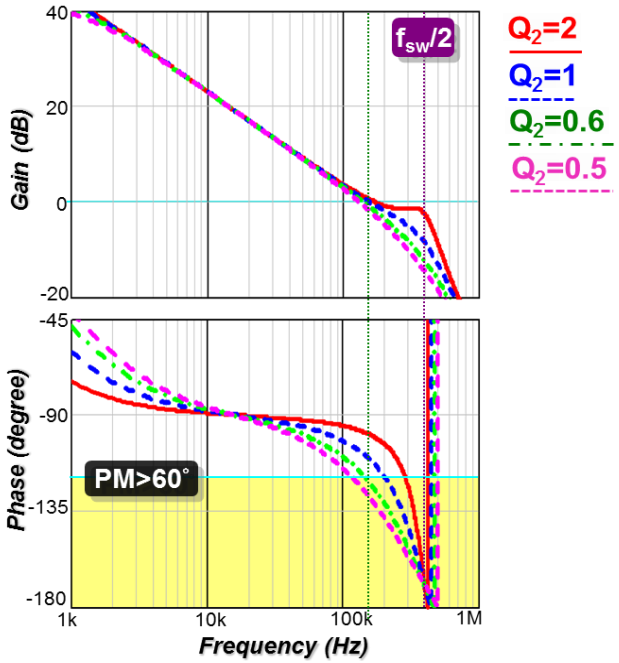
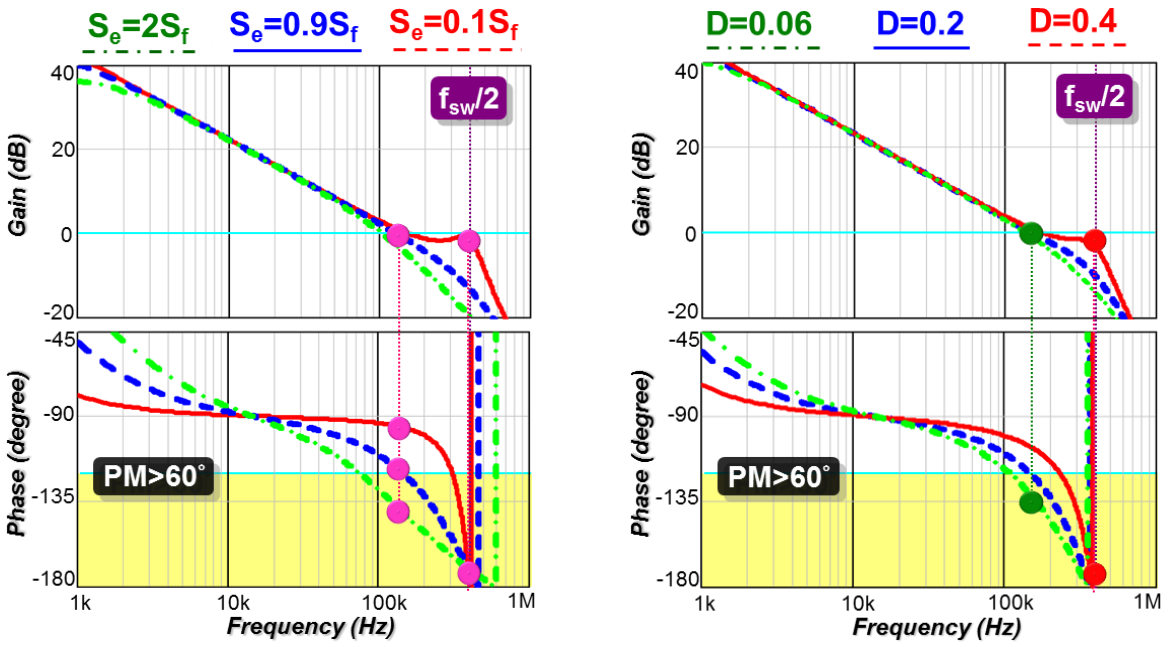


Figure 3.2 Effect of different Q_2 values on T_2 characteristic when BW≈$f_{sw}/6$

Currently, many publications suggest S_e should follow a V_o change such that be S_e tracks with S_f changes [C.1][C.2][C.3][C.4][C.4][C.5]. An example implementation for this is shown in Figure 3.4 [C.1][C.2][C.3]. The predetermined V_o feedback gain (K_e) must be equal to R_i/L_s such that $S_e=S_f$, since $S_f=V_o \cdot R_i/L_s$. The other two implementations in [C.4] and [C.5] are also based on the assumption. However, it is found that making $S_e=S_f$ does not improve high-BW design, since the double pole is over-damped. According to (3.2), Q_2 is equal to $2/\pi$ (≈0.64) if $S_e=S_f$, so it is still too low to maintain a PM>60° for a BW of $f_{sw}/6$, as shown in Figure 3.5(a). Unfortunately, considering the possibility of tracking errors, the over-damping issue of the

adaptive control becomes worse. Since R_i and L_s are highly dependent on the converter design and component tolerance, it is impossible to rely on a fixed K_e to maintain S_e=S_f.



(a) (b)

Figure 3.3 Effect of fixed S_e on T_2: (a) different S_e designs, and (b) different D ranges

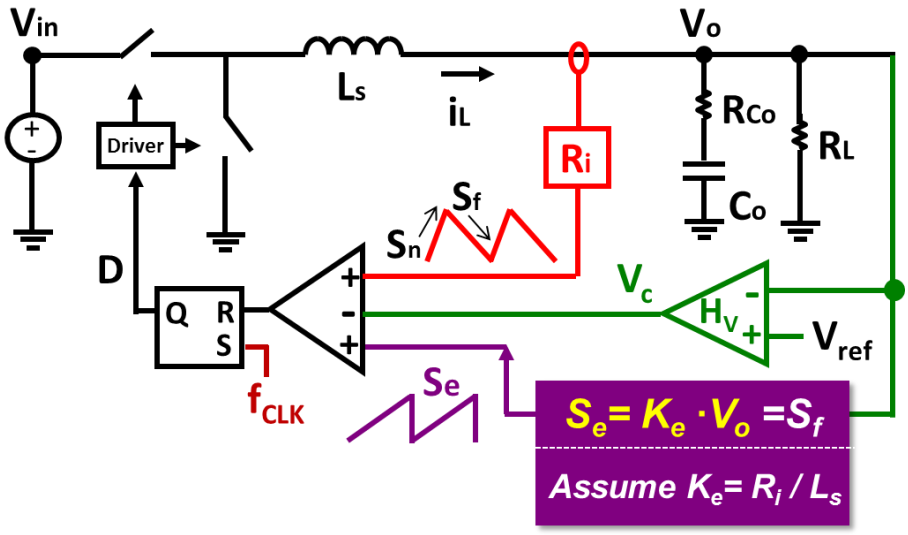
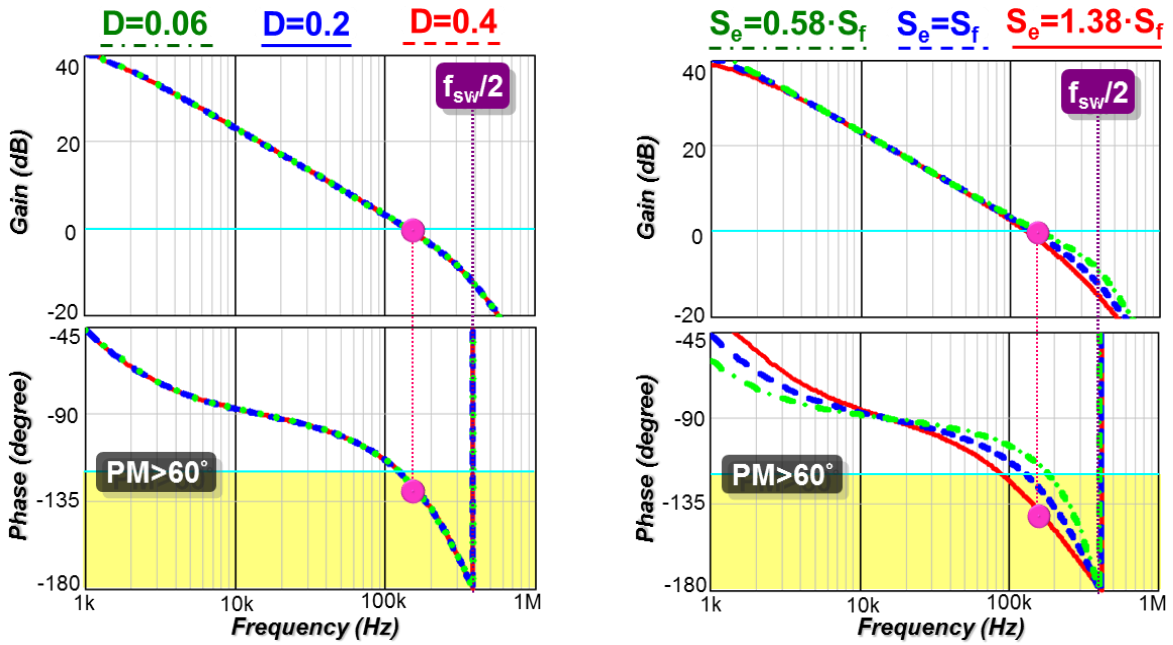
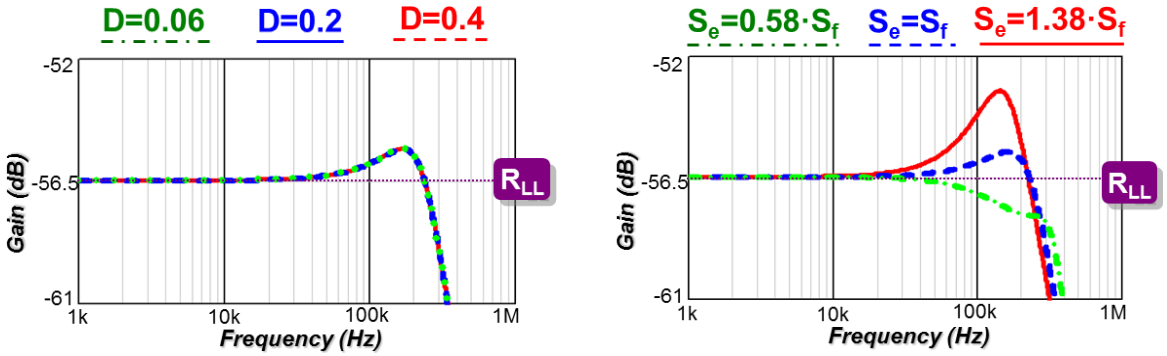


Figure 3.4 The block diagram of state-of-the-art constant-frequency control



(a) (b)

Figure 3.5 T_2 loop gain of the state-of-the-art control scheme: (a) ideal case, and (b) worst case.



(a) (b)

Figure 3.6 Z_{oc} of the state-of-the-art control scheme: (a) ideal case, and (b) worst case.

The impact of tolerance change on the adaptive control scheme is revealed in Figure 3.5(b). According the specifications of the ADP1853 controller from Analog Devices, the R_i tolerance is +/-13% [C.6]. Also, according to the specifications of the powder core inductor (FCUL1040-H-

R36M) from TOKO Inc., the L_s tolerance ranges between -35% and +20% [C.7]. In total, S_e can be +38% higher or -42% less than the actual S_f. When S_e is +38% higher than S_f, it is found that PM drops even lower. In the end, regardless of whether the tracking error is small or large, Z_{oc} peaking always occurs, as shown in Figure 3.6.

3.2 Proposed Adaptive Ramp Compensation to Enhance Stability Margin

3.2.1 Operating Principle

New adaptive ramp compensation is proposed to fix Q_2 under any possible parameter variations, so the stability margin can be maximized for high-BW design. Another goal is that the Q_2 value can be chosen to be higher than $2/\pi$ (0.64) to enhance a higher PM. The proposed auto-tuning concept is that S_e is adjusted based on the real current slope change, S_n and S_f, to control Q_2 value. All possible variations are reflected in the current-slope change, regardless of whether the variations come from the V_{in}, V_o, R_i or L_s tolerances. Based on (3.2), the proposed S_e control law for PCM control is derived as:

$$S_e = \left(\frac{1}{Q_2\pi} + 0.5\right)\cdot S_f + \left(\frac{1}{Q_2\pi} - 0.5\right)\cdot S_n \tag{3.3}$$

where the sensed S_n and S_f values are multiplied with two constants respectively and then summed together. For example, if Q_2=1 is desired, $S_e \approx 0.82\cdot S_f - 0.18\cdot S_n$.

Figure 3.7 shows the block diagram of a PCM-controlled buck converter that includes the proposed auto-tuning idea. First, the triangular current feedback signal ($i_L\cdot R_i$) is differentiated into a square waveform. Then, the value of the two slopes is obtained by a sample-and-hold

(S/H) circuit triggered by the turn-on and turn-off instance of D. After that, a scaling circuit performs multiplication and summing of (3.3). Finally, a ramp generator outputs the desired S_e slope.

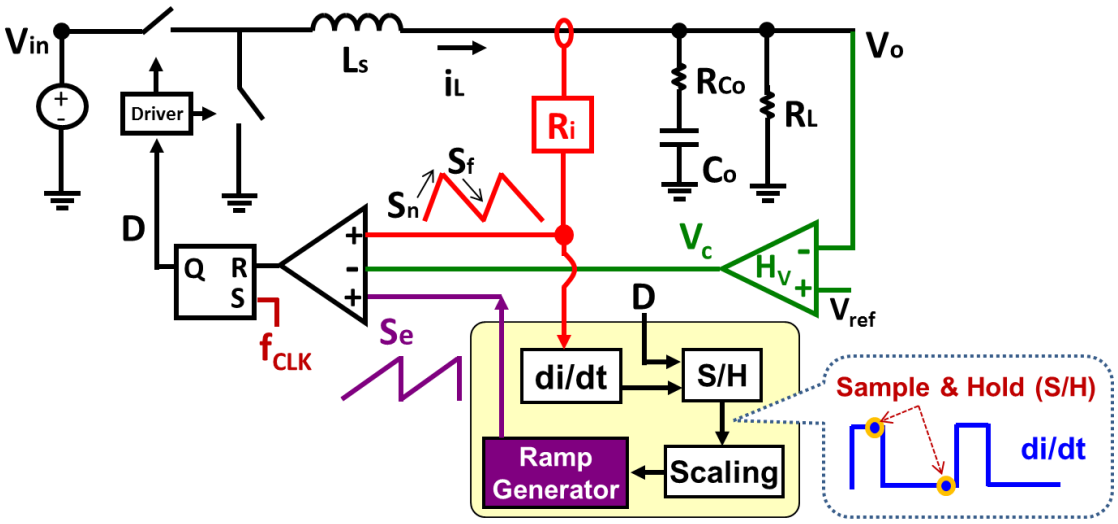


Figure 3.7 The block diagram of proposed adaptive constant-frequency PCM control

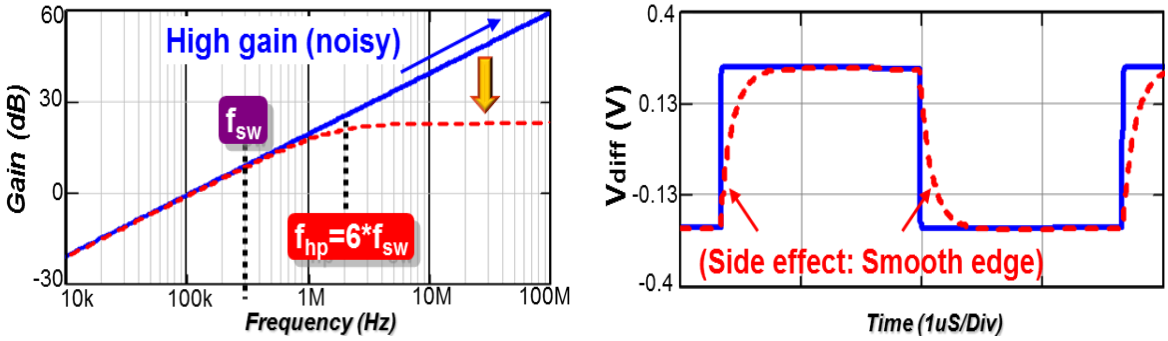
3.2.2 Circuit Design Considerations

As shown in Figure 3.8(a), since the high-frequency gain of an ideal differential is high, the amplified high-frequency noise of the current feedback signal distorts the differentiated waveform. Therefore, the differentiator should be designed with a high-frequency pole at the corner frequency (f_{hp}) to limit the high-frequency gain. The transfer function of the suggested differentiator is expressed as:

$$H_{diff}(s) = \frac{sK_d}{s/\omega_{hp} + 1} \tag{3.4}$$

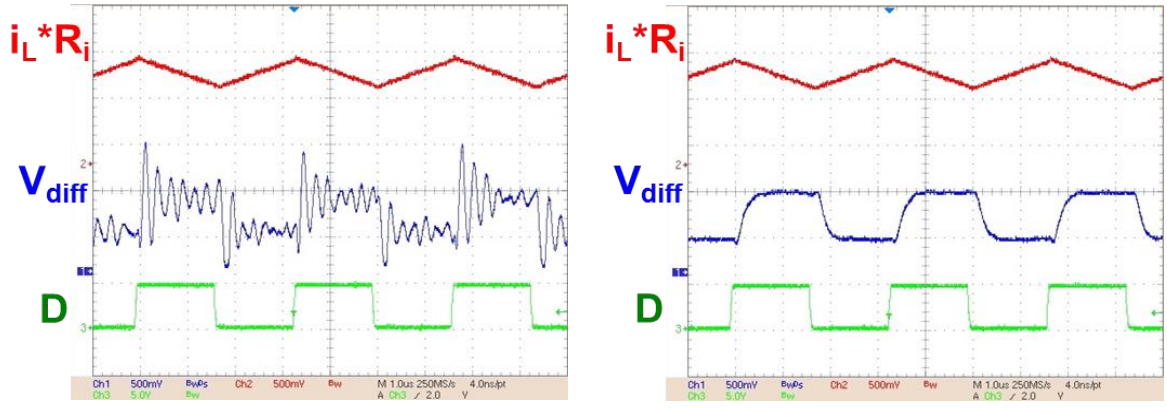
where K_d is the gain of the differentiator and $\omega_p = 2\pi f_{hp}$.

In Figure 3.8(b), the two levels of the differentiated waveform can be calculated as $S_n \cdot K_d$ and $-S_f \cdot K_d$. The figure also indicates the side effect of lowering f_{hp}: the rising and falling edges of the square waveform (t_r, t_f) are smoothed out. Fortunately, this effect can be overcome by either sample-and-holding the two settled slope values before the duty cycle transition or blanking the smooth edge before sampling. The experimental result in Figure 3.9 demonstrates that the differentiation waveform (V_{diff}) is clean enough to identify the slope information, when f_{hp} is designed at $6 \cdot f_{sw}$.



(a) (b)

Figure 3.8 Effect of high-frequency pole in the differentiator: (a) frequency domain, and (b) time domain.



(a) (b)

Figure 3.9 The experimental results of the differentiator: (a) f_{ph}>100MHz, and (b) f_{ph}=1.8MHz ($6 \cdot f_{sw}$).

Figure 3.10 shows the analog auto-tuning circuit for analog PCM controllers: First, a differentiator is connected to the analog current feedback signal ($i_L \cdot R_i$). Then, two sample-and-hold circuits are connected to the differentiator in order to sense the two current slopes, $S_n \cdot K_d$ and $-S_f \cdot K_d$, where $K_d = R_d C_d A_d$. After that, two trans-conductance amplifiers, g_{m1} and g_{m2}, scale the two sampled slope values with different trans-conductance values based on the Q_2 selection. Finally, the outputs of the two amplifiers are serially connected to form a summing node, and the summed current signal (I_R) charges C_R to generate an analog external ramp slope.

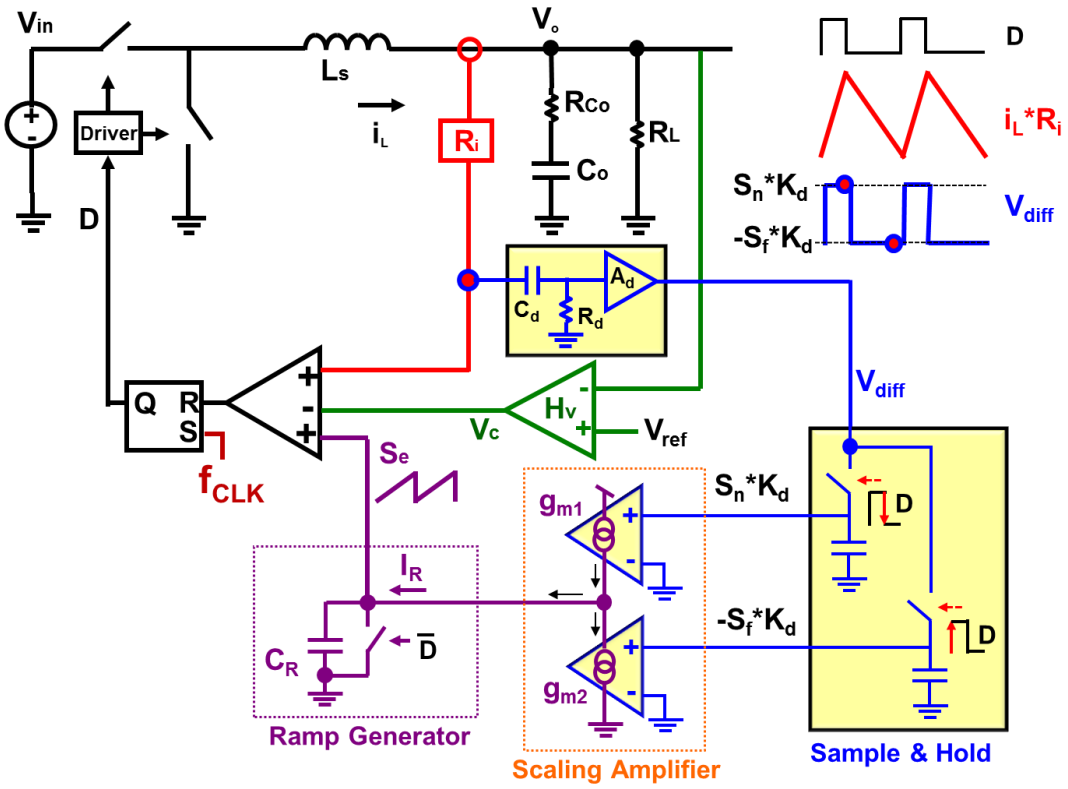


Figure 3.10 The analog implementation of proposed S_e auto-tuning concept.

The value for S_e based on the circuit arrangement is derived as:

$$S_e = [A_d g_{m2} R_d \frac{C_d}{C_R}] \cdot S_f + [A_d g_{m1} R_d \frac{C_d}{C_R}] \cdot S_n \tag{3.5}$$

Though the S_e calculation relies on several analog components, the tolerance can be mutually compensated as long as they are in the same control chip. For example, the tolerance of C_d and C_R can be compensated, because two integrated capacitors have similar variations and make the ratio change of C_d/C_R small. Moreover, the variation of g_{m1} and g_{m2} is inversely proportional to the variation in R_d, so the variation of $R_d \cdot g_{m1}$ and $R_d \cdot g_{m2}$ can also be controlled.

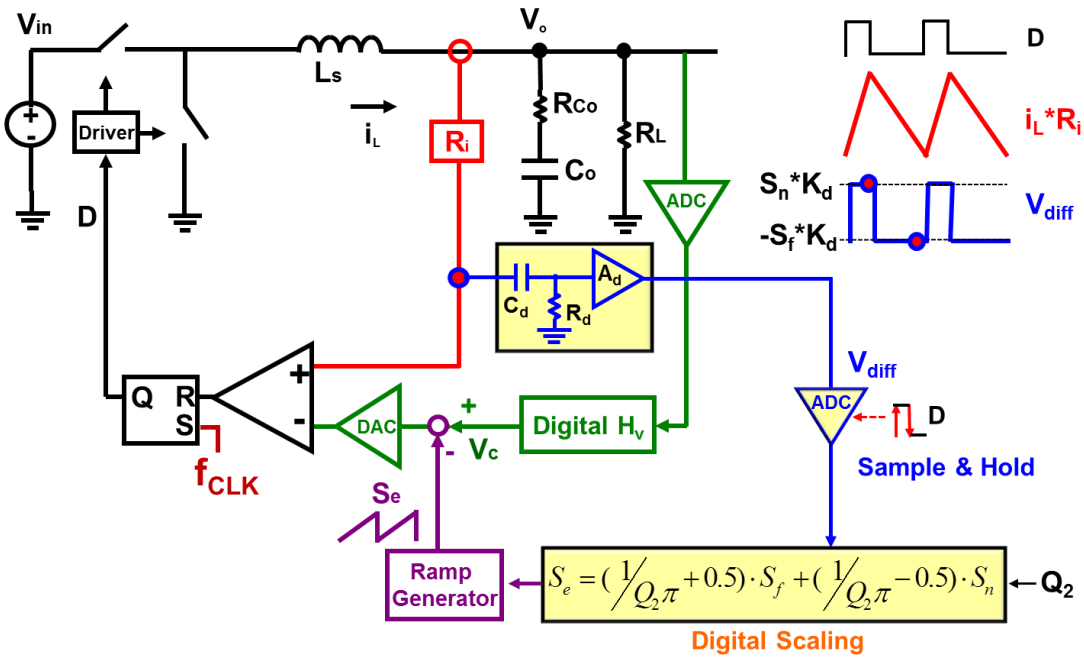


Figure 3.11 The digital implementation of the proposed S_e auto-tuning concept.

Figure 3.11 shows the digital auto-tuning circuit for mixed-signal PCM controllers: First, one ADC inside the controller is triggered by the rising and falling edge of the duty cycle to sense the two current slopes. Next, digital scaling is performed to obtain the desired S_e based on the Q_2 selection, and finally a digital ramp is generated. The advantage of digital scaling over analog implementation is that the slope calculation is insensitive to component tolerance from the auto-tuning circuit.

3.2.3 Extension to Other Types of Constant-Frequency Control

This method can be easily extended to valley current-mode control (VCM) and average current-mode control (ACM). Based on [A.41], the quality factor expression of VCM is calculated as:

$$Q_2 = \frac{1}{\pi(\frac{s_e + s_f}{s_n + s_f} - 0.5)} \tag{3.6}$$

Therefore, the proposed S_e control law for VCM is derived as:

$$S_e = (\frac{1}{Q_2\pi} - 0.5)\cdot S_f + (\frac{1}{Q_2\pi} + 0.5)\cdot S_n \tag{3.7}$$

where the only difference in implementation is the coefficient for S_n and S_f. For example, if Q_2=1 is desired, $S_e \approx -0.18\cdot S_f + 0.82\cdot S_n$.

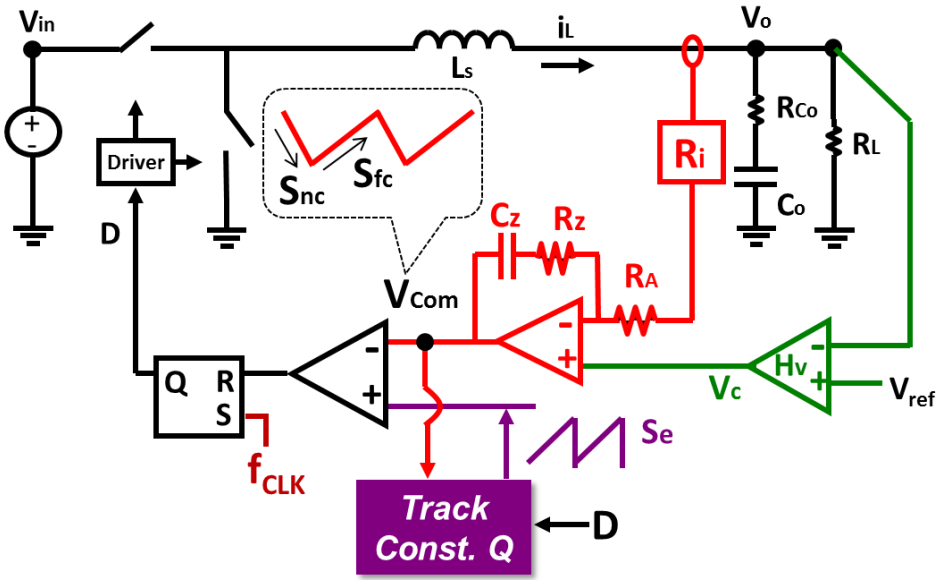


Figure 3.12 Proposed adaptive constant-frequency ACM control.

For the ACM configuration in Figure 3.12, since the current-loop compensator exhibits a proportional gain of R_Z/R_A in the high-frequency range, the triangular inductor current waveform is amplified with R_Z/R_A onto V_{Com}. According to [C.8], the quality factor expression of ACM is calculated as:

$$Q_2 = \frac{1}{\pi(\frac{s_e + s_{nc}}{s_{nc} + s_{fc}} - 0.5)} \tag{3.8}$$

where S_{nc} and S_{fc} represent the amplified slope at V_{Com} i.e. $S_{nc}=(R_Z/R_A)\cdot S_n$ and $S_{fc}=(R_Z/R_A)\cdot S_f$. Therefore, the proposed S_e control law for ACM is derived as:

$$S_e = (\frac{1}{Q_2\pi} + 0.5)\cdot S_{fc} + (\frac{1}{Q_2\pi} - 0.5)\cdot S_{nc} \tag{3.9}$$

Based on this understanding, the differentiator for ACM should be placed at V_{Com} to sample S_{nc} and S_{fc}, as shown in Figure 3.12.

3.3 Extension to Multiphase VRs

Figure 3.13 shows one implementation of the proposed two-phase auto-tuning configuration. The control voltage (V_c) is compared with the inductor current and external ramp of each phase to determine the off-time instance of each PWM signal. Based on the equivalent circuit model in [A.41], the T_2 loop gain can be expressed as:

$$T_2(s) \approx \frac{H_v(s)}{R_i C_o s}(\frac{1}{1 + \frac{s}{\omega_2 Q_{ph1}} + \frac{s^2}{\omega_2^2}} + \frac{1}{1 + \frac{s}{\omega_2 Q_{ph2}} + \frac{s^2}{\omega_2^2}}) \tag{3.10}$$

where Q_{ph1} and Q_{ph2} represent the quality factor of the two double poles at $f_{sw}/2$. The equation indicates that the high-frequency property is determined by the combination effect of the two double poles from the two separated current feedback loops. Therefore, the auto-tuning circuit is added in each phase to individually control Q_{ph1} and Q_{ph2} to be constant. The slopes of S_{e1} and S_{e2} can be different depending on the parameter change in the Q_{ph1} and Q_{ph2} expressions. The limitation of this implementation is that the number of auto-tuning circuits increases with a higher phase number, so the circuit complexity increases.

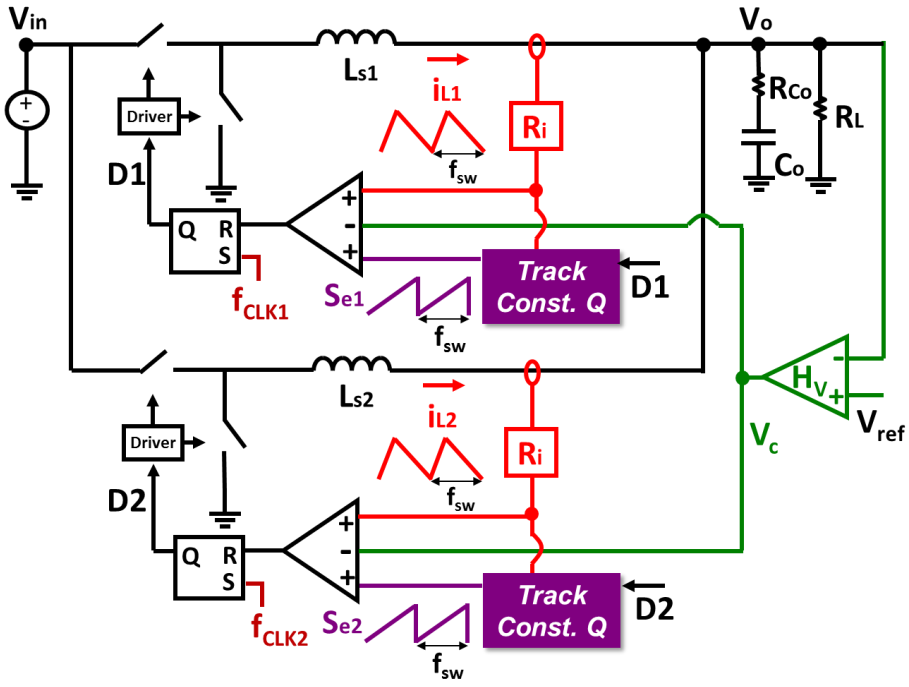


Figure 3.13 The two-phase configuration with the individually-controlled S_e auto-tuning

To minimize the circuit complexity, another implementation of the proposed two-phase auto-tuning configuration is presented in Figure 3.14. The modulation is determined by the intersection between V_c and a current loop, which is formed from the summation of the individual phase currents (i_{sum}). Figure 3.15 shows the operation principle: V_c is compared with

i_{sum} and S_{e1} to determine off-time instance of D_1, while V_c is compared with i_{sum} and S_{e2} to determine the turn-off instance of D_2. The slope and frequency of S_{e1} and S_{e2} are the same but the phase shift is 180°.

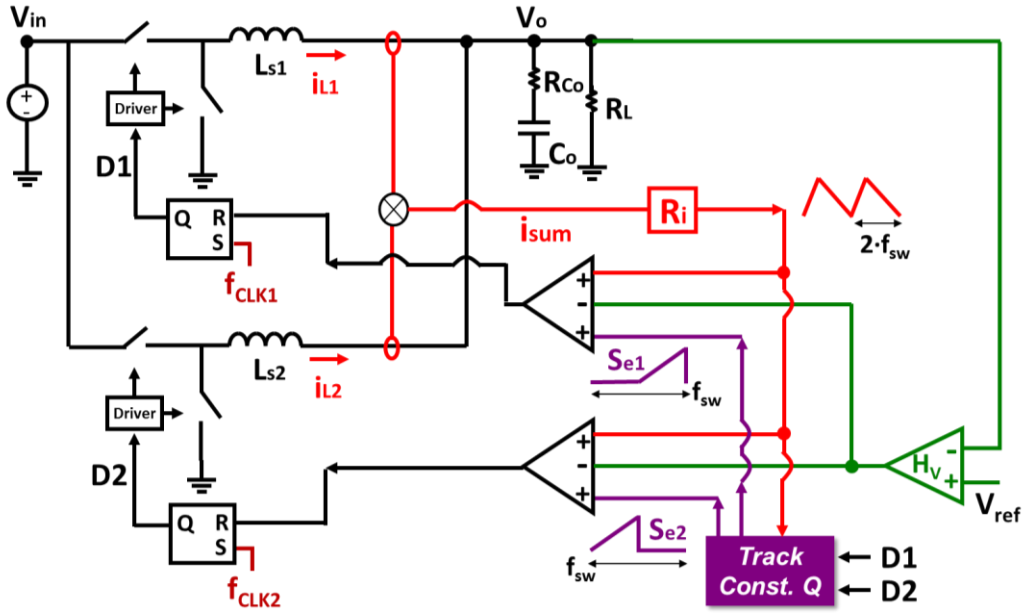


Figure 3.14 The two-phase configuration with the centralized-controlled S_e auto-tuning

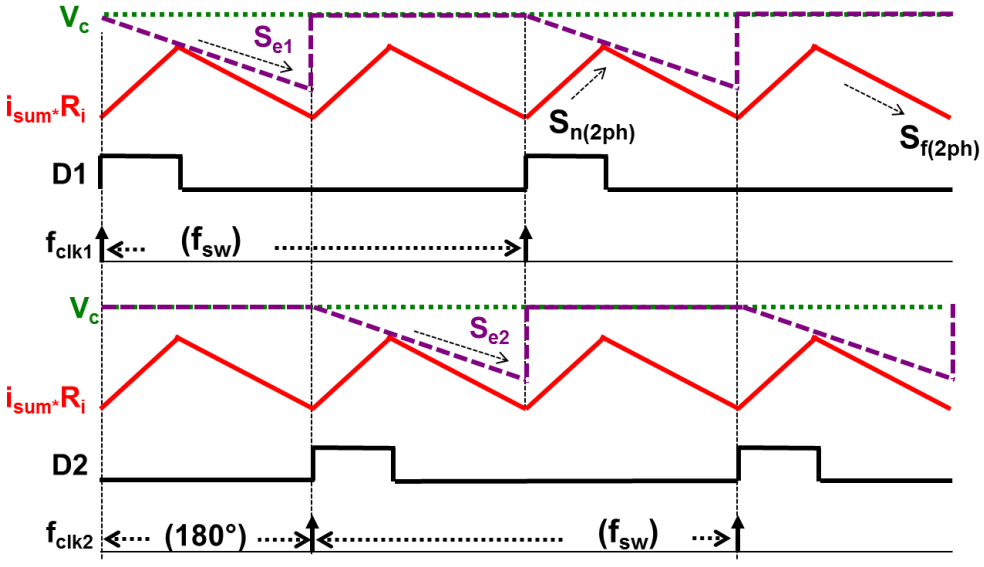


Figure 3.15 Operation principle of the PWM modulation with summed inductor current

Since there is only one i_{sum} current loop, the T_2 loop gain only contains a double pole, and can be expressed as:

$$T_2(s) \approx \frac{H_v(s)}{R_i C_o s}\left(\frac{1}{1+\frac{s}{\omega_{2(2\text{ph})}Q_{2(2ph)}}+\frac{s^2}{\omega_{2(2ph)}^{\ 2}}}\right) \tag{3.11}$$

where $\omega_{2(ph)}=2\pi/T_{sw}$ because the frequency of i_{sum} is $2\cdot f_{sw}$. Also, $Q_{2(2ph)}$ of PCM control is expressed as:

$$Q_{2(2ph)} = \frac{1}{\pi\left(\frac{s_e + s_{n(2\text{ph})}}{s_{n(2\text{ph})} + s_{f(2\text{ph})}} - 0.5\right)} \tag{3.12}$$

where S_e is the slope of S_{e1} as well as S_{e2}, $S_{n(2ph)}=R_i(V_{in}-2V_o)/L_s$, and $S_{f(2ph)}=2R_iV_o/L_s$ for a two-phase buck converter running with D<0.5.

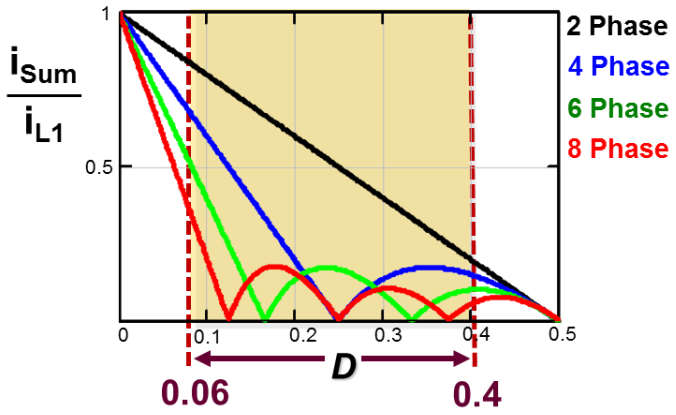


Figure 3.16 The ripple cancellation effect of i_{sum}

Equations (3.11) and (3.12) indicate that the high-frequency property is determined by the double pole from the summed current feedback loop. Therefore, the first benefit of the proposed

control method is simpler implementation, because using only one auto-tuning circuit is adequate to control $Q_{2(2ph)}$. The second benefit is higher BW design, because the double pole is located at f_{sw} for two phase operation. However, the drawback is that the maximum D range and maximum phase number are limited by the ripple cancellation effect of i_{sum}. In Figure 3.16, the i_{sum} ripple in four-phase operation is gone when D is close to 0.25, so the S_e tuning can no longer find the slope information. A hybrid interleaving technique is introduced in Chapter 5 to overcome the ripple cancellation effect of i_{sum}, where the current feedback signals of every two phases are summed together for wide D range application of a multiphase VR.

3.4 Verification

(A) SIMPLIS simulation

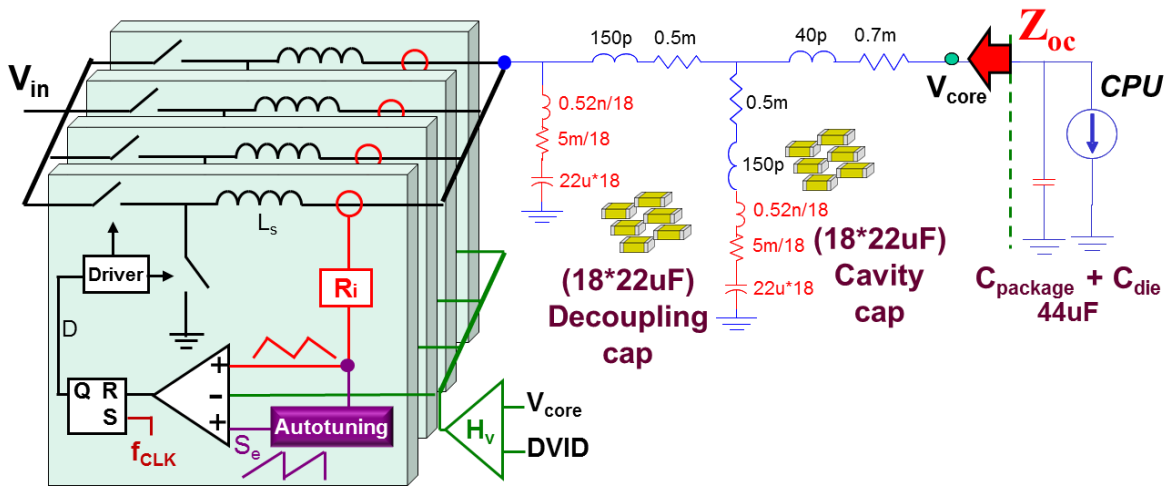
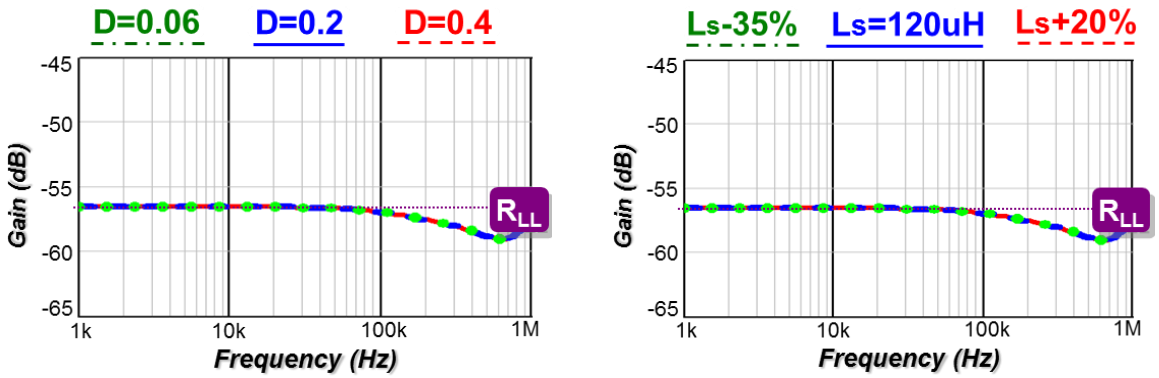


Figure 3.17 The simulation diagram for proposed four-phase PCM control

The proposed control scheme is verified using the design example of a four-phase buck converter where V_{in}=5.2~8.4V, V_o=0.5~2V, L_s=150nH (-35%~20%), f_{CLK}=800kHz, R_i=18mΩ, R_{LL}=1.5mΩ, and no bulk capacitors. As shown in Figure 3.17, the filter only contains decoupling

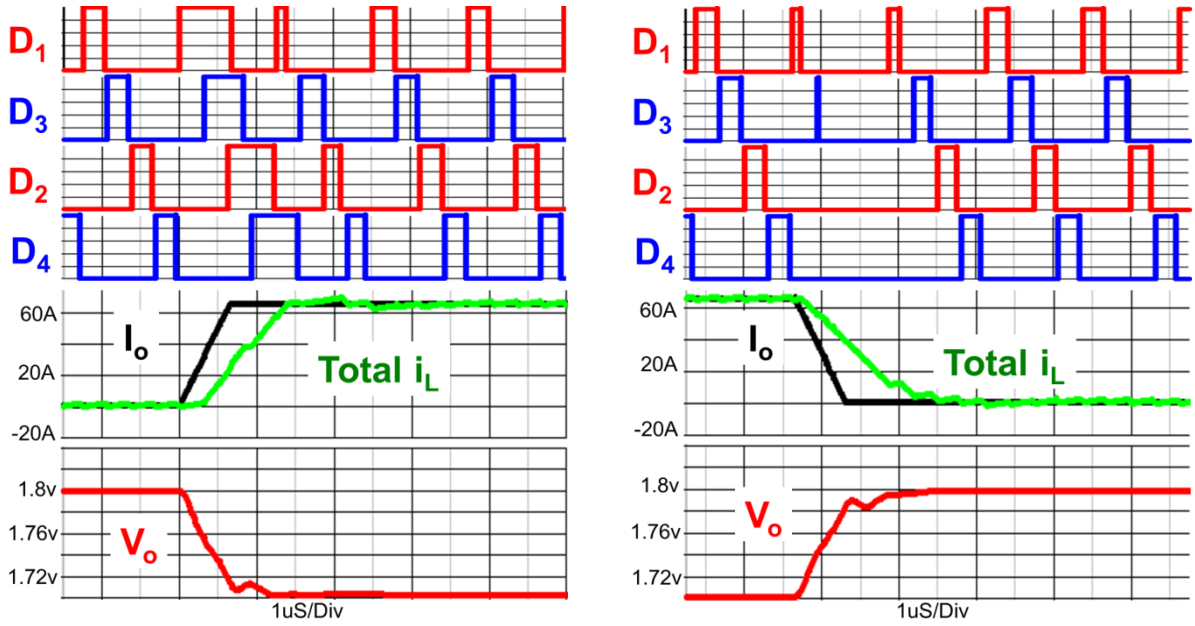
capacitors outside of a CPU socket with 18·22μF and cavity capacitors with 18·22μF. The multiphase configuration uses the individually-controlled S_e auto-tuning, and the tuning circuit uses the analog implementation to track Q_2=1. The H_v compensator contains finite gain of 3, a zero at 530kHz, and a pole at 2MHz.

Firstly, the closed-loop output impedance (Z_{oc}) is simulated under the D range of interest and the worst inductance variation of L_s. The results in Figure 3.18 show that no impedance peaking is observed, considering those parameter changes. Next, the transient response is simulated under V_{in}=8.4V, V_o=1.8V, L_s=150nH, and a step load change between 1A and 66A with a slew rate of 100A/μS. The load transient simulations in Figure 3.19 show no voltage spike for both step-up and step-down load transients, because the high-BW property allows the PWM signals to change the on-time rapidly.



(a) (b)

Figure 3.18 Z_{oc} simulation of the proposed control scheme: (a) in wide D range, and (b) in L_s tolerance.



(a) (b)

Figure 3.19 Transient simulations of proposed control scheme to: (a) load step-up, and (b) load step-down

(B) Experimental verification

An experimental platform for the analog S_e auto-tuning circuit is built on a control board with an analog peak-current-mode controller, UC3842, as shown in Figure 3.20. The S_e auto-tuning loop is implemented with an AD783 from Analog Devices as the sample-and-hold amplifier, and an AD8062 as the scaling amplifier with current-source output to charge a ramp capacitor. The power board contains a single-phase buck converter controlled by the circuity on the control board. The test parameters are V_{in}=4V~13V, V_o=1.2~3.3V (D=0.1~0.8), L_s=600nH±30%, R_i=40mΩ, C_d=390pF, R_d=256Ω, A_d=-13, f_{sw}=300kHz, and the target Q_2=1. Figure 3.21 demonstrates that the measurement results of $V_o(s)/V_c(s)$ are insensitive to variations over a wide D change from 0.1 to 0.8 and ±30% of inductance change, so the effectiveness of proposed analog implementation is verified.

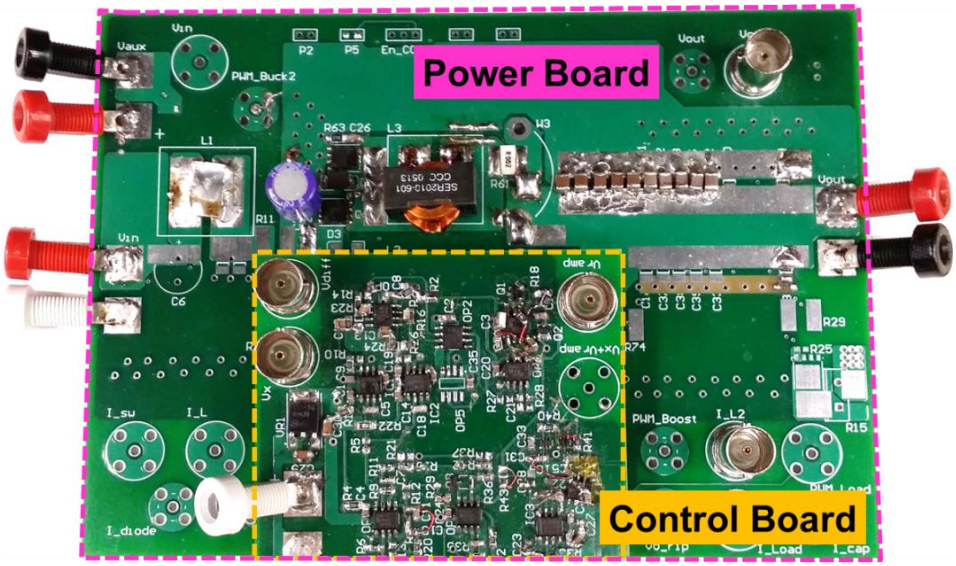
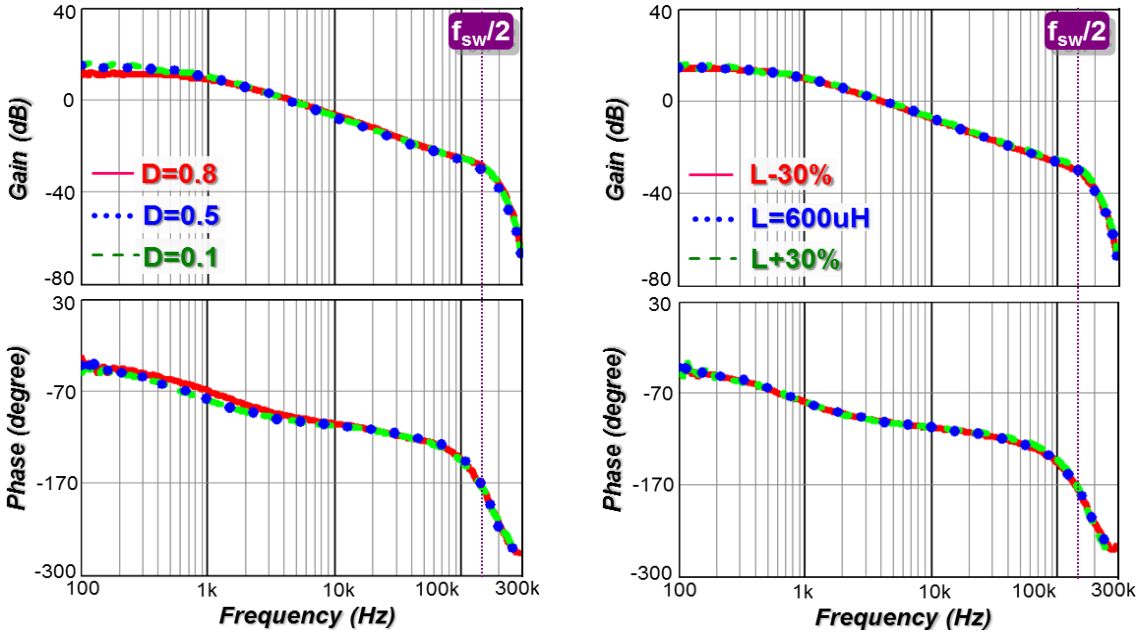


Figure 3.20 Hardware of an analog PCM controller using proposed analog S_e auto-tuning



(a) (b)

Figure 3.21 V_o/V_c measurements using analog tuning: (a) in a wide D range, and (b) in L_s tolerance

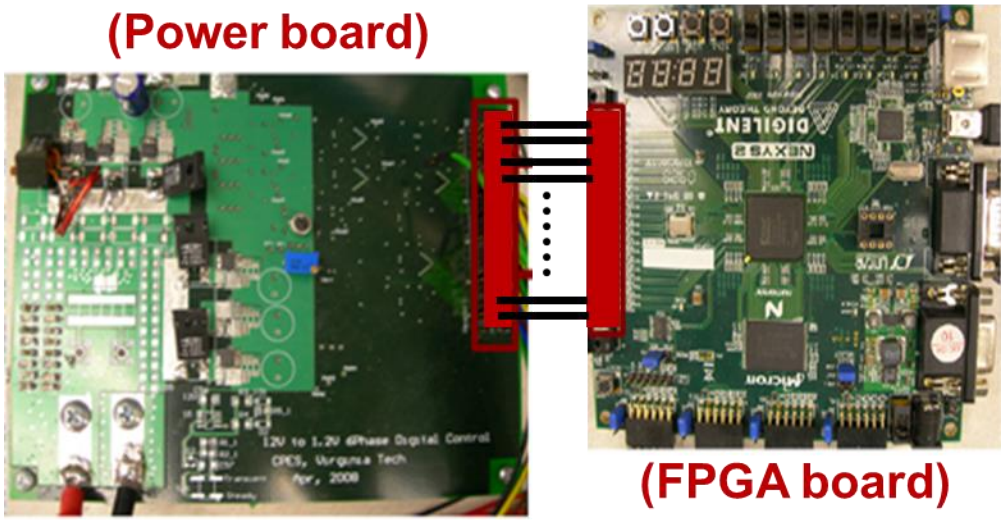
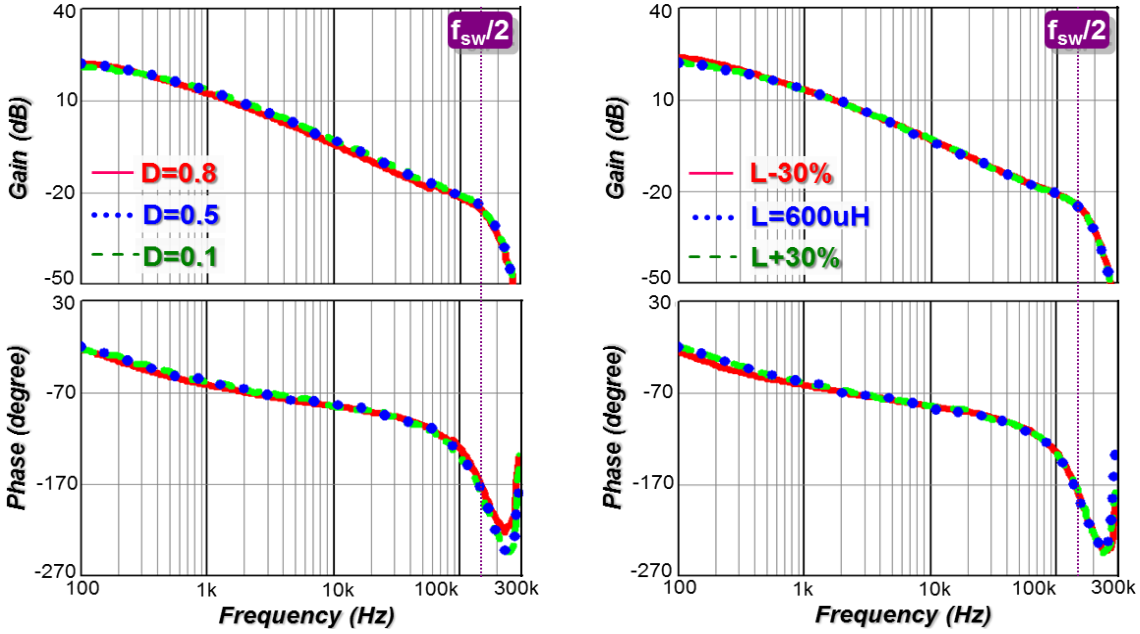


Figure 3.22 Hardware of a mixed-signal PCM controller with proposed digital S_e auto-tuning



(a) (b)

Figure 3.23 V_o/V_c measurements using digital tuning: (a) in a wide D range, and (b) in L_s tolerance

Figure 3.22 shows an FPGA-based experimental platform for the digital S_e auto-tuning circuit built on a mixed-signal PCM controller to track Q_2=1. The digital outer-loop compensator

and S_e auto-tuning loop are implemented with a Xilinx Spartan-3E FPGA with a 50MHz system clock rate and a 10-bit data converter with 2mV resolution. The power board contains a single-phase buck converter controlled by the FPGA control board. The test condition is the same as the analog implementation. Figure 3.23 demonstrates the measurement results of $V_o(s)/V_c(s)$ are fixed over D=0.1~0.8 and L_s±30%, because the proposed S_e auto-tuning is able to fix the Q_2 successfully.

3.5 Summary

The system BW of the reviewed adaptive S_e compensation is limited, because the Q_2 of the $f_{sw}/2$ double pole alters the plant characteristic and introduces significant phase delay. To solve this issue, a novel adaptive current-mode control is proposed to maintain a stationary high-frequency property by controlling constant Q_2 with a new S_e compensation technique. The T_2 BW can push higher than 135kHz with 800kHz switching to remove the need for bulk capacitors under the vicinity of the $f_{sw}/2$ double pole without impedance peaking. Then, two simple implementations and circuit design guidelines are provided to realize proposed control in various types of constant-frequency current-mode controllers, such as peak current mode, valley current mode, and average current mode operations. After that, two multiphase configurations are developed, and the design trade-offs are discussed. Finally, the simulation and experimental results verify that the proposed control scheme can meet the latest AVP requirement without bulk capacitors even considering wide V_{in}, V_o, and L_s variations.

Chapter 4. Adaptive High-Bandwidth Variable-Frequency Control

As mentioned in Chapter 1, although variable-frequency control performs with a higher-bandwidth design than constant-frequency PWM, there are several design challenges to be solved, such as frequency variation, interleaving, and clock synchronization. Therefore, this chapter introduces a novel variable-frequency control scheme with an adaptive PLL loop to resolve the problems. In the beginning, the stability issues using a PLL loop in variable frequency control are identified. Then, a generic PLL loop model is derived to provide the loop compensation guideline. After that, a generic adaptive PLL loop is proposed to simplify loop compensation. Finally, the proposed model and control scheme are verified with simulation and experimental results.

4.1 Review of State-of-the-Art Variable-Frequency Control

Based on the output filter model of CPU VR in Chapter 1, if BW can be pushed close to 200kHz, the VR design can not only eliminate bulk capacitors but also further reduce the decoupling capacitors outside of the CPU socket from 22·22μF to 8·22μF. For f_{sw} of 800kHz, the target BW is around $f_{sw}/4$. In Chapter 3, the proposed adaptive constant-frequency PWM control is able to push the control BW to $f_{sw}/5$. However, the BW of $f_{sw}/4$ is not easy to achieve, because the vicinity effect of the double pole at $f_{sw}/2$ introduces a significant phase delay. Therefore, an alternative high-BW control scheme needs to be further investigated.

Recently, variable-frequency control has been widely used, because it not only improves light-load efficiency, but also pushes BW design higher than using constant-frequency PWM [A.39]. Constant on-time control (COT) and ramp pulse modulation (RPM) control are the two widely-used variable-frequency controls. Based on the equivalent circuit model in [A.41], the simplified T_2 loop gain of COT control with ideal current sensing is:

$$T_2(s) \approx \frac{R_L}{R_i} \frac{R_{Co}C_o s+1}{R_L C_o s+1} \frac{H_v(s)}{1+\frac{s}{\omega_1 Q_1}+\frac{s^2}{\omega_1^2}} \tag{4.1}$$

where $Q_1=2/\pi$, $\omega_1=\pi/T_{on}$, and T_{on} is the fixed on-time. It indicates that the double pole is located much higher than $f_{sw}/2$ and Q_1 is always constant. With constant Q_1, external ramp compensation is not required. In the case of small duty cycle ($D\approx 0.1$), the double pole is located at $5\cdot f_{sw}$ and can be negligible, so the equivalent circuit model behaves like an ideal voltage-controlled current source, as plotted in Figure 4.1. In contrast with the PCM control in which $Q_2=2/\pi$, COT control enables the T_2 BW toward $f_{sw}/4$ with PM>60°, as shown in Figure 4.2.

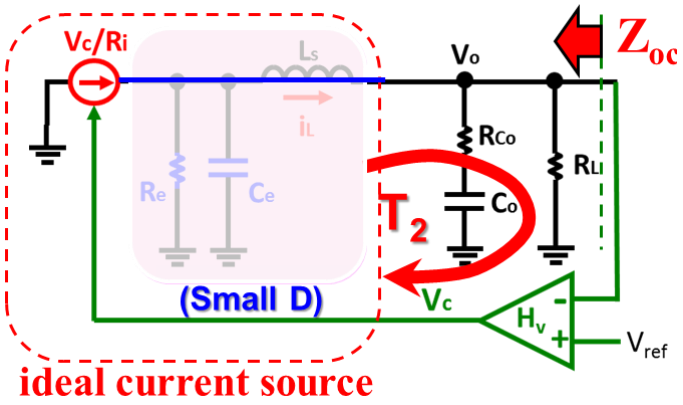


Figure 4.1 Equivalent circuit model of COT current-mode control [A.41]

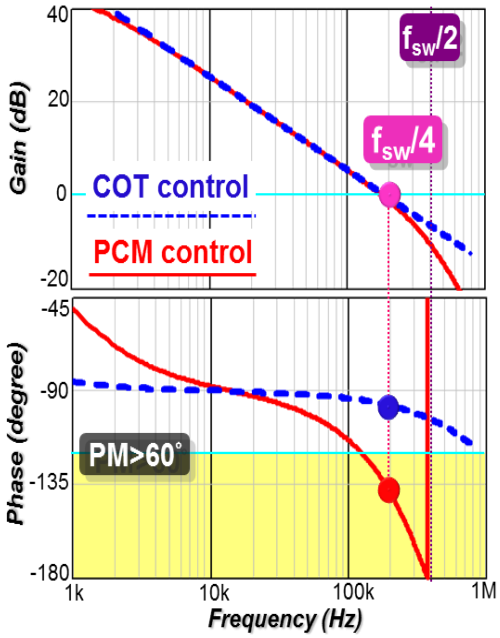
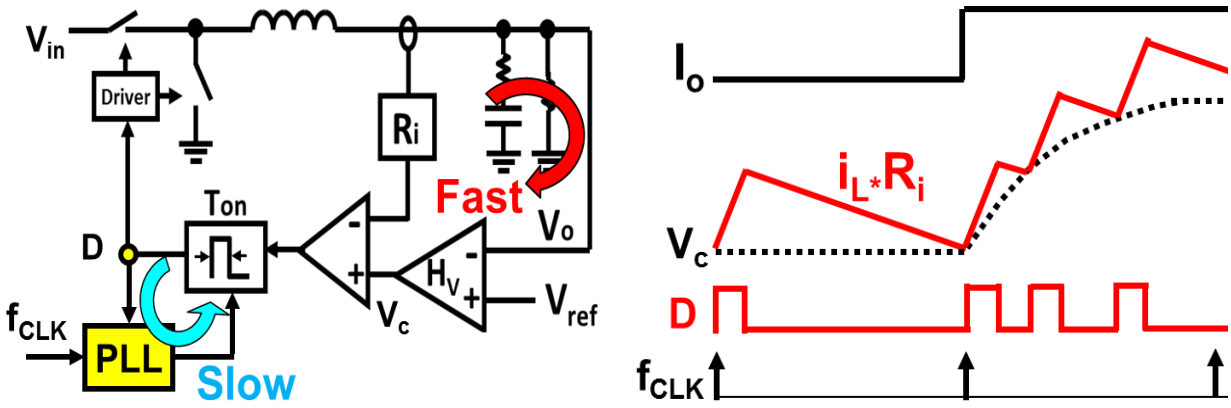


Figure 4.2 Comparison of T_2 loop gain for D=0.1 case

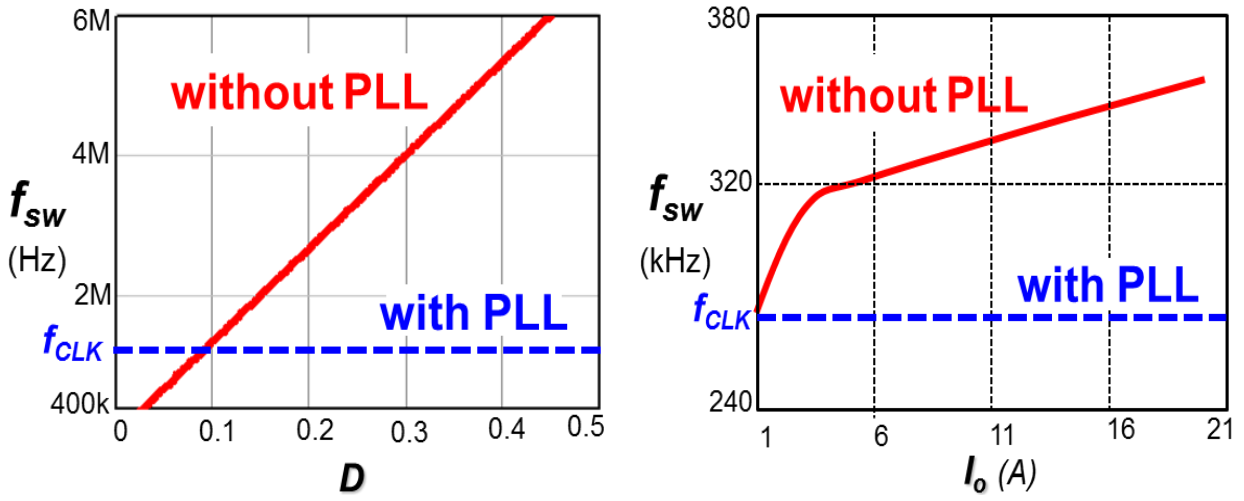


(a) (b)

Figure 4.3 Concept of COT control with PLL loop: (a) block diagram, and (b) transient response

However, to make the variation-frequency control for practical use in a multiphase VR, it is important to investigate a simple solution, which is capable of minimizing f_{sw} variation, achieving interleaving, and synchronizing the clock with other VRs. Recently, COT control with a Phase-Lock Loop (PLL) was proposed to meet these demands [D.1][D.2][D.3]. Figure 4.3(a)

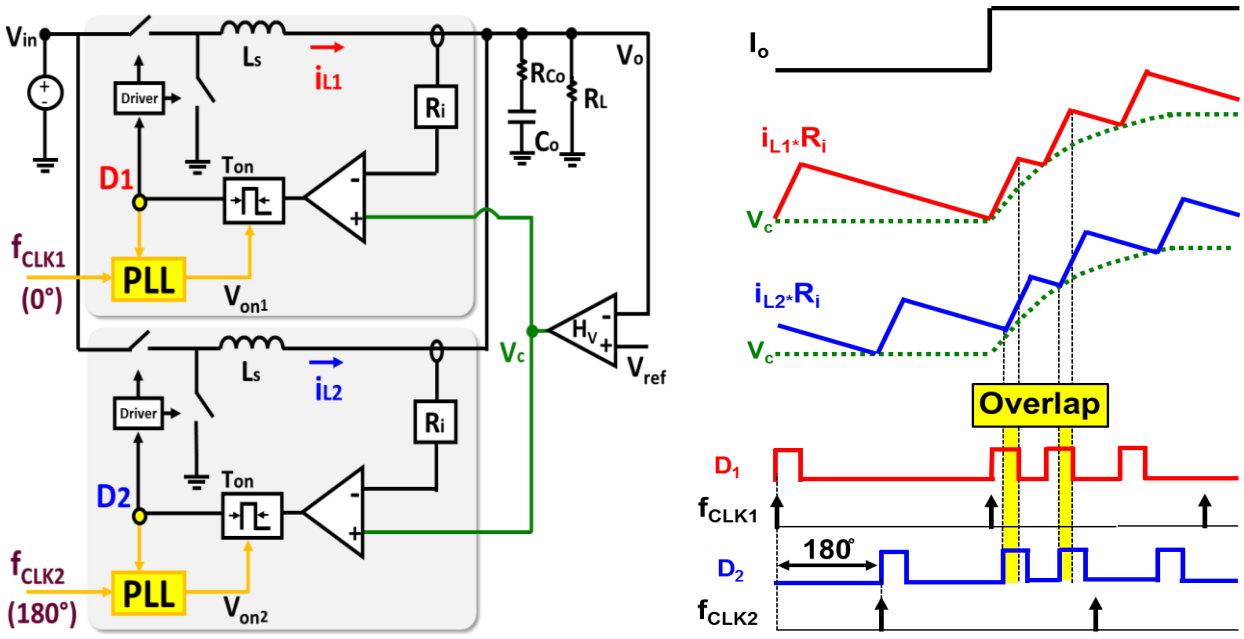
shows the block diagram, where the PLL forces D to follow with a fix-frequency reference clocks (f_{CLK}) through adjusting T_{on}. Since the PLL loop response is purposely designed to be much slower than the main control loop, D loses tracking with f_{clk} during a load transient, as shown in Figure 4.3(b). Then, the transient response still behaves like original COT control.



(a) (b)

Figure 4.4 PLL Loop for solving the frequency variation to: (a) D changes, and (b) I_o changes [D.1]

The benefits of a PLL loop are explained as follows. Firstly, the steady-state f_{sw} is locked with f_{CLK}, so it becomes insensitive to V_{in}, V_o or steady-state load current (I_o), as shown in Figure 4.4. Then, the efficiency can be optimized and the output filter design is easier [D.1]. Secondly, interleaving is achieved by phase-shifting the two clock signals of two phases in 180^o, as shown in Figure 4.5(a). Thirdly, V_c is compared with the inductor current of each phase, so D_1 and D_2 can be naturally overlapped to improve the step-up load transient. Also, the overlapping area is dependent on the magnitude of the load change, so there is no ring-back problem in the smaller load transient, in contrast with the multiphase VR which uses force duty-cycle saturation [D.4].



(a) (b)

Figure 4.5 Interleaving with PLLs for COT control: (a) block diagram, and (b) step-up load transient

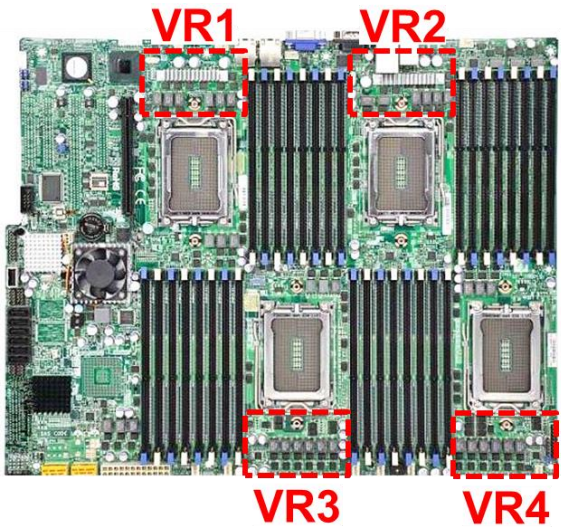


Figure 4.6 Multiple VRs on the motherboard of a four-processor server [D.5]

From the viewpoint of a system design, the fourth benefit is that the clocks of the VR controllers can be synchronized, so the beat-frequency input ripple can be eliminated for multiple

VRs sharing the same input-voltage rail, such as a server motherboard with multiple microprocessors in Figure 4.6 [D.5]. As shown in Figure 4.7, the common clock signal with a proper interleaving angle is sent to the PLL of each VR controller. Without a beat-frequency ripple, the conduction loss of the power delivery path is reduced, a smaller input filter can be used, and the interference to the load is avoided [D.6][D.7][D.8][D.9].

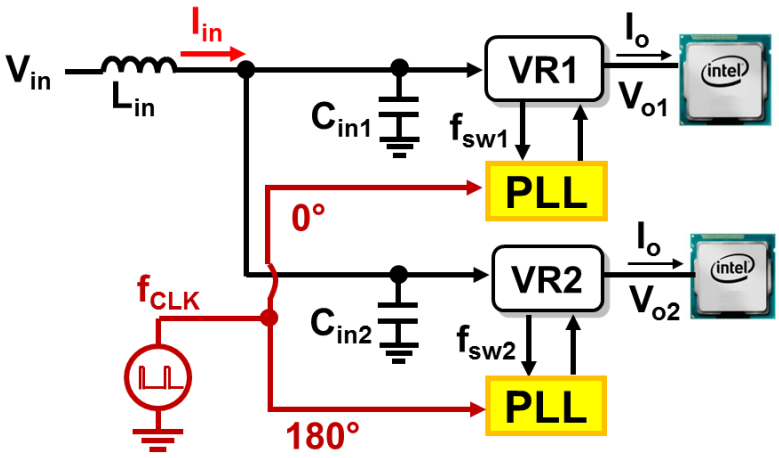


Figure 4.7 PLL Loop for synchronizing the switching frequency of multiple VRs in a system

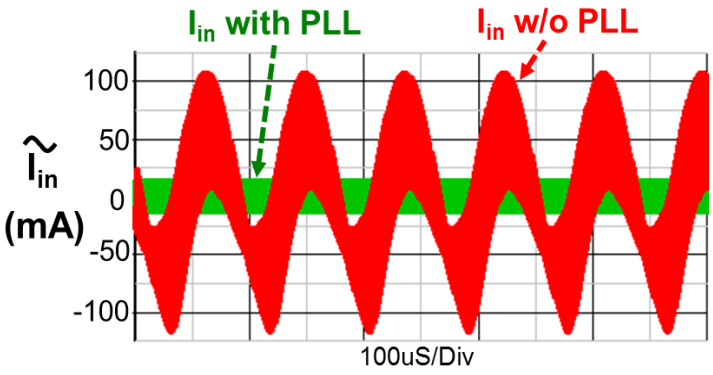


Figure 4.8 Simulation of input current ripple from two VRs sharing a common input rail

Figure 4.8 shows a simulation example to demonstrate the effectiveness of using PLL loop to eliminate the beat-frequency input current ripple from two COT-controlled VRs. The power stage parameters of the two VRs are: V_{in}=8.4V, V_o=1.8V, f_{clk}=800kHz, I_o=27A, L_s=150nH,

C_o=22μF·36 (ceramic cap), L_{in}=0.5μH, C_{in}=470μF·1 (OSCON cap) // 10μF·4 (ceramic cap), and single-phase operation per VR. Without PLL, when f_{sw1}=800kHz and f_{sw2}=790kHz, there is a large 10kHz ripple superimposed on the switching ripple. When the PLL is applied to each VR, the 10kHz ripple is gone, so the total ripple magnitude becomes ten-times smaller.

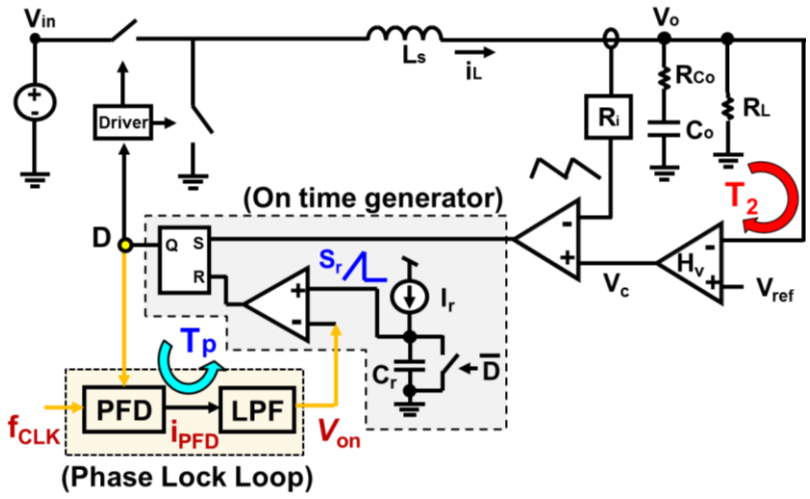


Figure 4.9 The state-of-art COT control with a PLL loop [D.1][D.2]

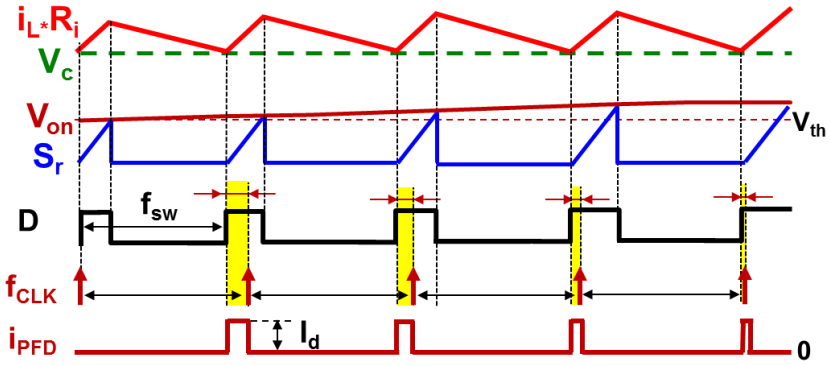


Figure 4.10 The operation principle of the PLL loop in COT control

The operation principle of two PLL-loop implementations is explained as follows. Figure 4.9 shows the block diagram of the first implementation [D.1][D.2]. The PLL contains a phase frequency detector (PFD) and a low-pass filter (LPF). The PFD is to detect the phase and

frequency difference between f_{sw} and f_{CLK}, and then generates a pulsating current signal (i_{PFD}) where its pulse width is equal to the time difference between the rising edges of two signals. The LPF is to smooth out the digital pulsating i_{PFD} into an analog V_{on} signal, and is also to ensure the PLL loop stability. Figure 4.10 demonstrates that when initial $f_{sw}>f_{CLK}$, the rising edge of D is leading the one of f_{CLK}, so the PFD output (i_{PFD}) generates a positive current pulse, which magnitude is equal to I_d, and then the LPF smoothens out the pulsating signal into an incremental V_{on} change. A higher V_{on} raises the ramp amplitude of S_r, so T_{on} increases and f_{sw} reduces.

Figure 4.11 shows the block diagram of the second implementation. The major difference is that the PLL loop controls T_{on} by changing S_r through a trans-conductance amplifier (g_{mr}) [D.3]. The operating principle is shown in Figure 4.12. When the rising edge of D is leading the f_{CLK}, the PFD generates a negative pulse of i_{PFD}. Then, the LPF smoothens out the pulsating signal into a shallower S_r change to extend T_{on}, thereby reducing f_{sw}.

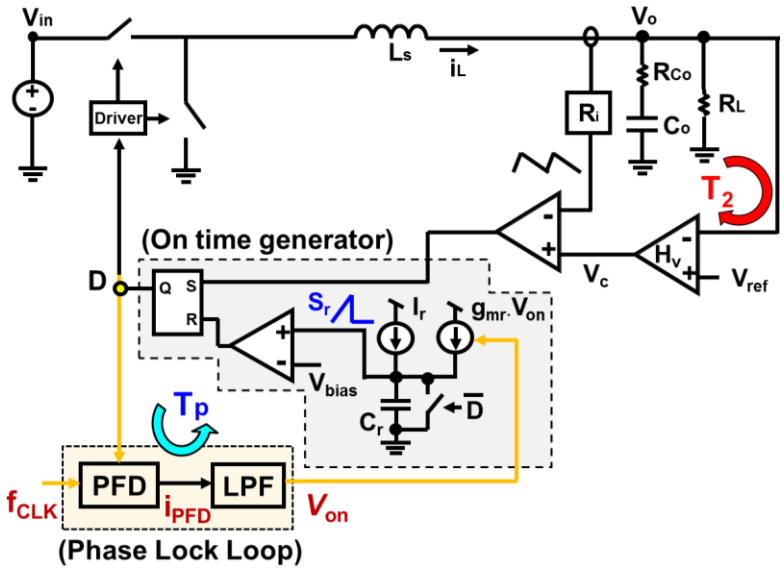


Figure 4.11 Alternative PLL loop design in COT control [D.3]

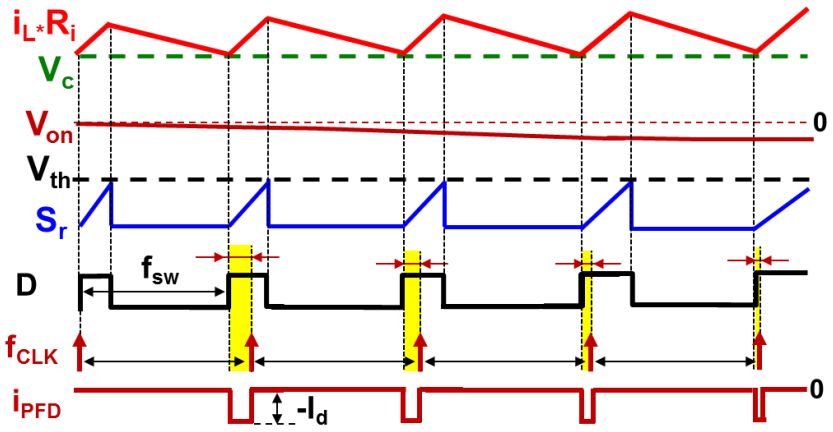


Figure 4.12 The operation principle of the alternative PLL loop design in COT control

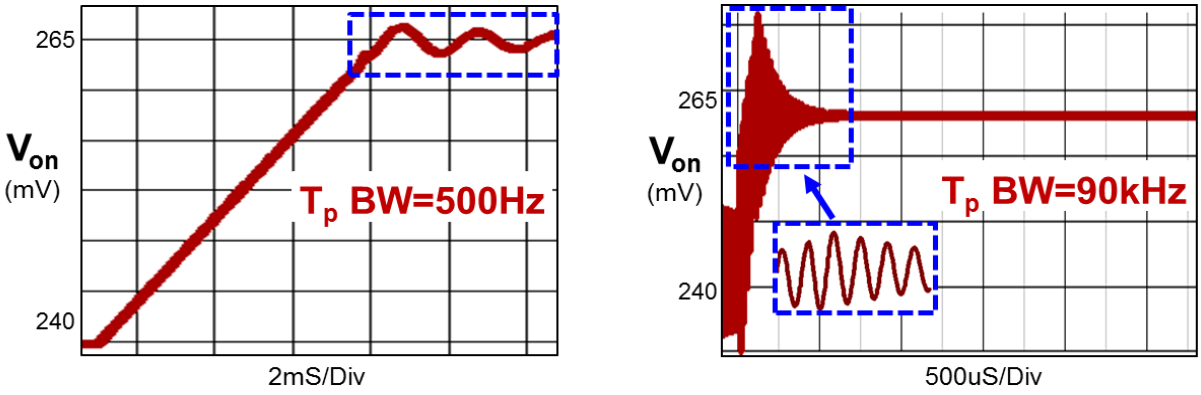


Figure 4.13 Stability issue of the PLL loop in COT control

The speed of the V_{on} change is dependent on the control BW design of the open-loop gain (T_p). The compensation of the PLL loop is difficult, however, because T_p BW can affect both its loop stability and the system performance. Figure 4.13 shows a simulation example to highlight the potential stability issue of a PLL loop in COT control. The simulation conditions are: V_{in}=12V, V_{ref} scales from 1.7V to 1.8V, f_{sw}=800kHz, and T_2 BW is 135kHz. The simulation results demonstrate that the PLL output (V_{on}) exhibits an oscillatory response when T_p BW is designed either too high or too low. Conceptually, in order to avoid the confliction with the T_2 loop, T_p BW should be designed to be as low as possible, but the observation shows that a low T_p

BW results in instability. The oscillation can result in duty-cycle jittering, higher output-voltage ripple, and can even cause lost tracking to f_{clk}. In the end, all the benefits using a PLL loop are lost with an unstable PLL loop. Unfortunately, there is no design guideline from previous literature to avoid the stability issue. Therefore, it would be advantageous to derive a small-signal model and investigate a better PLL loop structure to solve the stability issue.

4.2 Proposed Constant On-Time Control with Adaptive PLL Loop

4.2.1 Modeling and Design of PLL Loop

The small signal model is built based on the describing function (DF) method, because there are several non-linear components along the PLL loop, which include the PFD, the comparator of inductor current feedback, and the on-time generator. Modeling with the DF method, those non-linear components are treated as a single entity, and then the transfer function from the v_{on} to i_{PFD} is derived.

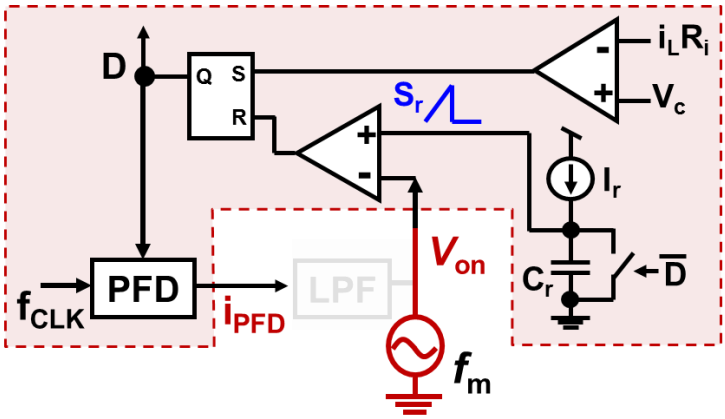


Figure 4.14 Proposed modeling methodology for a PLL loop in COT control

For the first PLL loop implementation in Figure 4.9, the small-signal model is derived as follows. As shown in Figure 4.14, a sinusoidal perturbation with a small magnitude at the frequency f_m is injected through the control signal v_{on}, when the LPF is disconnected. Then, based on the perturbed i_{PFD} waveform, the DF from v_{on} to i_{PFD} can be obtained. Three assumptions are made before applying the DF method: (i) the magnitude of the inductor current slopes during the on-period and the off-period remains constant; (ii) the magnitude of the perturbation signal is very small; and (iii) the perturbation frequency (f_m) and the clock frequency (f_{CLK}) are commensurable, which means that $N \times f_{CLK} = M \times f_m$, where N and M are positive integers [D.10][D.11]. The T_{off} and T_{on} are modulated by the perturbation signal: $v_{on}(t)=V_{th}+\hat{r}\sin(2\pi f_m \cdot t+\theta)$, where V_{th} is the steady state value, $\hat{r}$ is the perturbation magnitude, and θ is the initial angle.

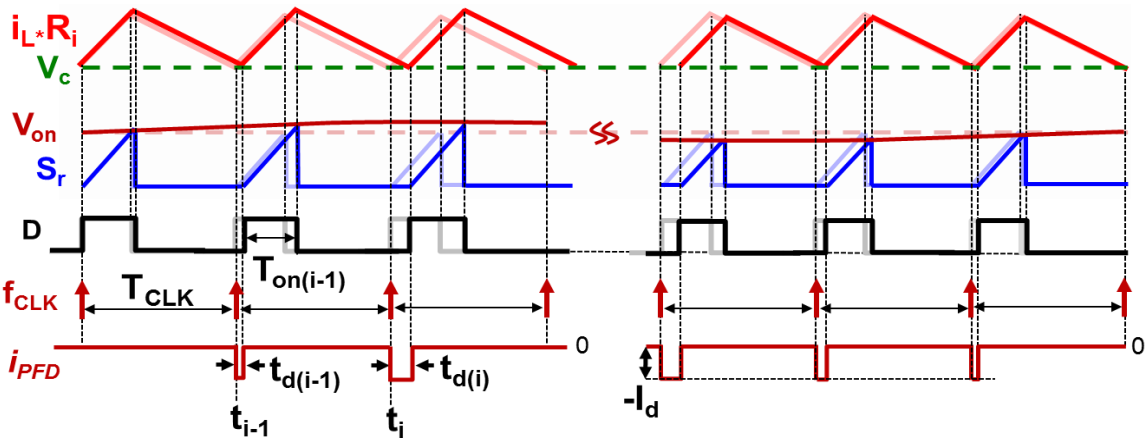


Figure 4.15 Key perturbed waveforms of the PLL loop in COT control

The modulated duty cycle and the perturbed i_{PFD} waveform are shown in Figure 4.15. Based on the modulation law, it is found that:

$$v_c + s_n T_{on(i-1)} = v_c + s_f [t_{d(i)} + (T_{CLK} - t_{d(i-1)} - T_{on(i-1)})] \tag{4.2}$$

$$T_{on(\mathrm{i}-1)} = v_{on}(\mathrm{t}_{i-1} + t_{d(i-1)} + T_{on(\mathrm{i}-1)}) / s_r \tag{4.3}$$

where $t_d(i)$ is the i^{th} cycle of i_{PFD} on-time, $T_{on}(i)$ is the i^{th} cycle of on-time of the duty cycle (D), $S_n=R_i(V_{in}-V_o)/L_s$, $S_f=R_iV_o/L_s$, L_s is the inductance of the output inductor, and R_i is the current feedback gain. t_i can be calculated as: $t_i=(i-1)T_{CLK}$.

Next, by substituting (4.3) into (4.2), it is found that:

$$t_{d(i)} - t_{d(\mathrm{i}-1)} = \frac{V_{in}\hat{r}\sin[2\pi f_m \cdot (\mathrm{t}_{i-1} + t_{d(i-1)} + T_{on(\mathrm{i}-1)}) + \theta]}{s_r V_o} \tag{4.4}$$

Then, the perturbed inductor current $i_{PFD}(t)$ can be expressed by:

$$i_{PFD}(t)\Big|_{0\le t\le t_M + T_{CLK}} = -I_d \cdot \sum_{i=1}^{M}[u(t-t_i) - u(t-t_i-t_{d(i)})] \tag{4.5}$$

where u(t)=1 when t>0, and I_d is the magnitude of $i_{PFD}(t)$.

After that, Fourier analysis can be performed on the $i_{PFD}(t)$ as:

$$c_m = j\frac{2f_m}{N}\int_0^{t_M + T_{CLK}} i_{PFD}(t)\cdot e^{-j2\pi f_m t}dt \tag{4.6}$$

where c_m is the Fourier coefficient of $i_{PFD}(t)$ at the perturbation frequency f_m.

By substituting (4.4) and (4.5) into (4.6), the coefficient can be calculated as:

$$c_m = \frac{-I_d}{s_r D T_{CLK}} \frac{e^{-j2\pi f_m(1-\mathrm{D})T_{CLK}}}{(1-e^{-j2\pi f_m T_{CLK}})} (\hat{r}\, e^{j\theta}) \tag{4.7}$$

Since the Fourier coefficient of v_{on} is $\hat{r}e^{j\theta}$, the describing function of v_{on}-to-i_{PFD} transfer function in the s-domain can be calculated as:

$$\frac{i_{PFD}(s)}{v_{on}(s)} = \frac{-I_d}{s_r D T_{CLK}} \frac{e^{-s(1-D)T_{CLK}}}{1-e^{-sT_{CLK}}} \tag{4.8}$$

The exponential term, $e^{-sT_{CLK}}$, can be simplified by using the Pade' approximation:

$$e^{-sT_{CLK}} = 1 - \frac{sT_{CLK}}{1 + \frac{s}{Q_3\omega_3} + \frac{s^2}{\omega_3^2}} \tag{4.9}$$

where $\omega_3=\pi/T_{CLK}$ and $Q_3=2/\pi$. This approximation is valid up to the frequency of $1/(2T_{CLK})$. Since the PLL loop is practically in a low BW design, the low-frequency approximation of (4.8) can be further simplified as:

$$\frac{i_{PFD}(s)}{v_{on}(s)} \approx \frac{-I_d}{s_r D T_{CLK}^2} \frac{1}{s} \tag{4.10}$$

For detail derivation, refer to Appendix A. Furthermore, the minus sign of (4.10) means that the transfer function includes the summing node sign for the error control signal between sensed f_{sw} and f_{clk} reference. Therefore, the open-loop gain of PLL loop (T_p) is represented as

$$T_p(s) = \left(-\frac{i_{PFD}(s)}{v_{on}(s)}\right) \cdot LPF(s) \tag{4.11}$$

LPF(s) is suggested to include an integrator to seize the i_{PFD} error signal, and a low-frequency zero (ω_z) to boost phase, and a high-frequency pole (ω_p) to filter pulsating i_{PFD} signal.

Since the PFD output is a current source, the LPF can be implemented with three passive components, as shown in Figure 4.16.

$$LPF(s) = \frac{A}{s}\frac{(s/\omega_Z + 1)}{(s/\omega_P + 1)} \tag{4.12}$$

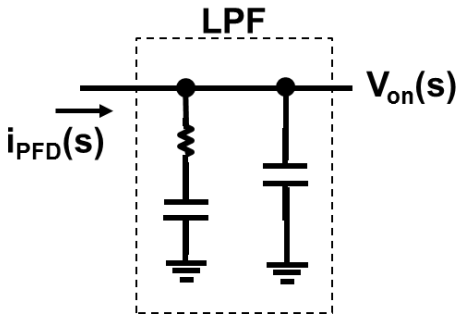
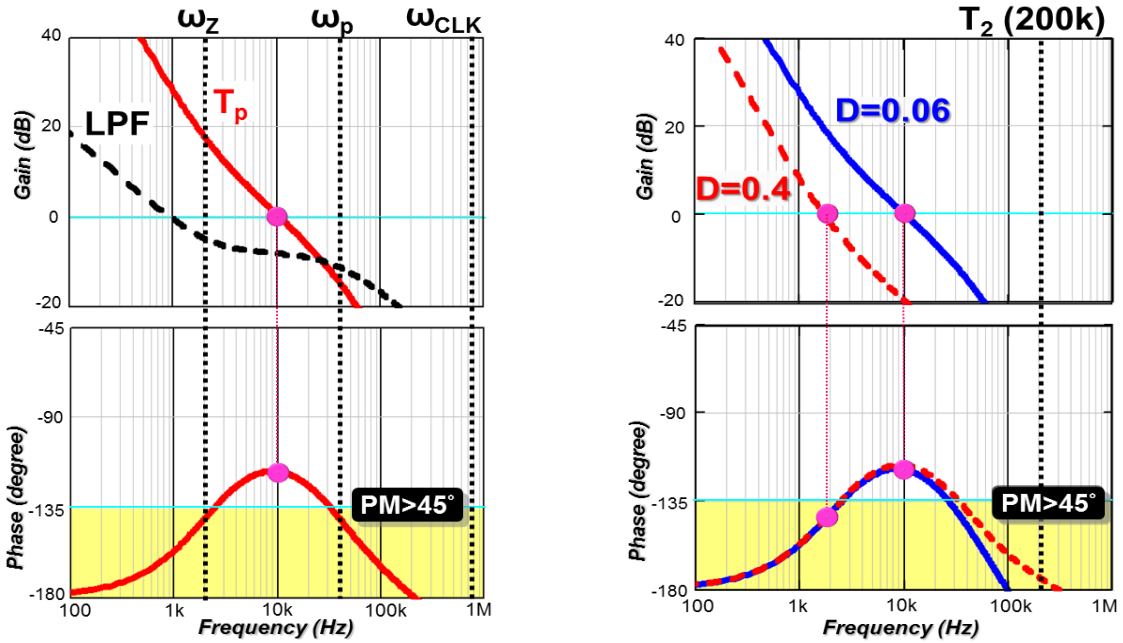


Figure 4.16 Recommended implementation of the LPF



(a) (b)

Figure 4.17 Challenges of T_p compensation: (a) design guideline of LPF, and (b) sensitivity to D change

Since both v_{on}-to-i_{PFD} transfer function and LPF(s) contain an original pole, the phase characteristic of T_p starts at -180°, then becomes larger than -135° after $\omega>\omega_z$, and finally drops below -135° again after $\omega>\omega_p$. Therefore, the model suggests T_p BW should crossover between ω_z and ω_p to remain a sufficient PM>45°, as shown in Figure 4.17(a). Besides, the exact model contains a delay term related with D, $e^{-s(1-D)T_{CLK}}$, so the additional phase delay needs to be considered if T_p BW pushes higher in a small D operation. Most importantly, the model explains the oscillatory response, which is observed in Figure 4.13, since the unique T_p characteristic only provides a limited region with sufficient PM.

The model also shows that the gain characteristic of T_p is inversely proportional to D, so T_P BW shifts when V_{in} or V_o changes. For the normal operation range of a laptop VR with D=0.06~0.4, when T_p BW is designed at 10kHz for D=0.06, T_p BW drops to less than 2kHz for D=0.4, as revealed in Figure 4.17(b). For a worst-case operation, such as a V_o start-up, the D range can be wider than at normal operation, so the BW shifting of T_p becomes more severe. This points out another complexity of the LPF compensation, because the gain change makes PM easily to slide below 45°.

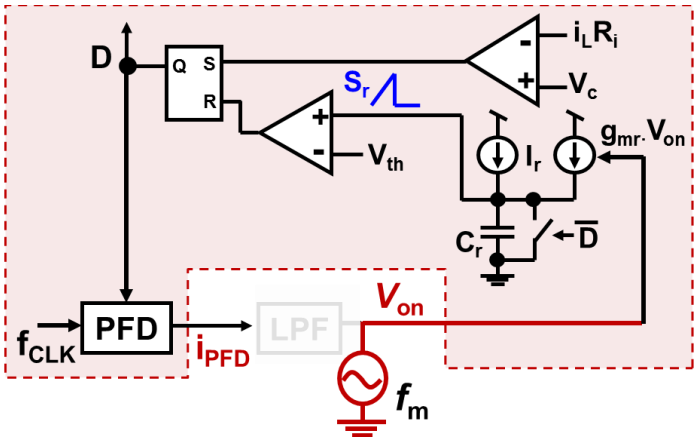


Figure 4.18 Proposed modeling methodology for the alternative PLL loop design in COT control

For the alternative PLL loop implementation in Figure 4.11, the small-signal model is derived as follows. Figure 4.18 shows that after LPF is disconnected, a sinusoidal perturbation with a small magnitude at the frequency f_m is injected through the control signal v_{on}. Under the perturbation signal, $v_{on}(t)=0+\hat{r}\sin(2\pi f_m \cdot t+\theta)$, the modulated duty cycle and the perturbed i_{PFD} waveform are shown in Figure 4.19.

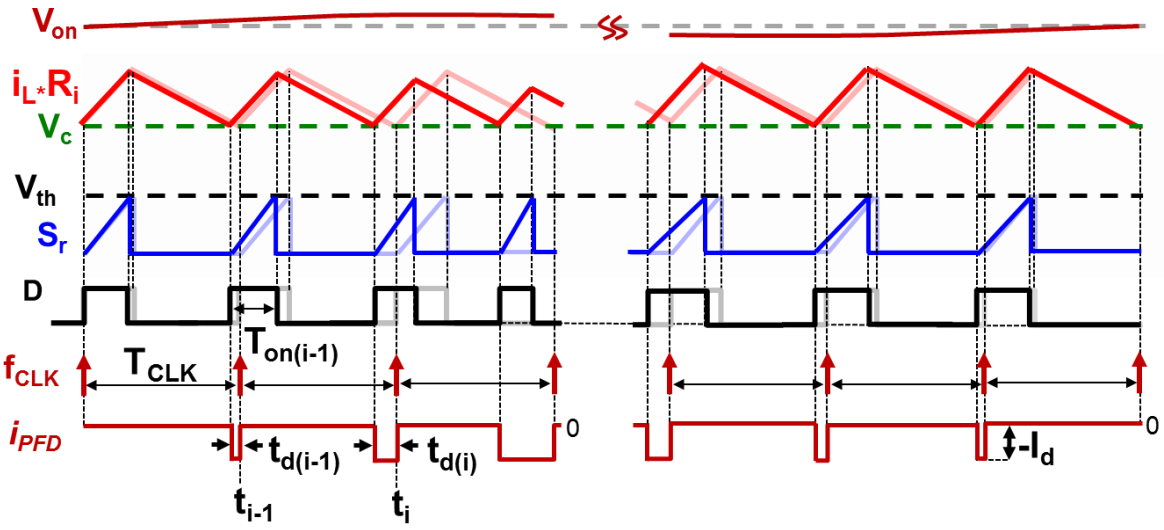


Figure 4.19 Key perturbed waveforms of the alternative PLL loop design in COT control

Based on the modulation law, it is found that:

$$v_c + s_n T_{on(i-1)} = v_c + s_f (T_{CLK} - t_{d(i)} - T_{on(i-1)} + t_{d(i-1)}) \tag{4.13}$$

$$s_r (t_{i-1} + T_{on(i-1)} - t_{d(i-1)}) = \frac{I_r + g_{mr} \cdot v_{on}(t_{i-1} + T_{on(i-1)} - t_{d(i-1)})}{C_r} \tag{4.14}$$

$$T_{on(i-1)} = V_{th} / s_r (t_{i-1} + T_{on(i-1)} - t_{d(i-1)}) \tag{4.15}$$

Next, by substituting (4.14) and (4.15) into (4.13), it is found that:

$$t_{d(i)} - t_{d(\mathrm{i}-1)} = \frac{V_{in} V_{th} C_r g_{mr} \cdot \hat{r} \sin[2\pi f_m \cdot (\mathrm{t}_{i-1} + T_{on(\mathrm{i}-1)} - t_{d(i-1)}) + \theta]}{V_o I_r \{I_r + g_{mr} \cdot \hat{r} \sin[2\pi f_m \cdot (\mathrm{t}_{i-1} + T_{on(\mathrm{i}-1)} - t_{d(i-1)}) + \theta]\}} \tag{4.16}$$

Since $I_r >> g_{mr} \cdot \hat{r} \sin[2\pi f_m \cdot (\mathrm{t}_{i-1} + T_{on(\mathrm{i}-1)} - t_{d(i-1)}) + \theta]$, (4.16) can be simplified as:

$$t_{d(i)} - t_{d(\mathrm{i}-1)} \approx \frac{V_{in} V_{th} C_r g_{mr} \cdot \hat{r} \sin[2\pi f_m \cdot (\mathrm{t}_{i-1} + T_{on(\mathrm{i}-1)} - t_{d(i-1)}) + \theta]}{V_o {I_r}^2} \tag{4.17}$$

Then, the perturbed inductor current $i_{PFD}(t)$ can be expressed by:

$$i_{PFD}(t)\Big|_{0 \le t \le t_M + T_{CLK}} = -I_d \cdot \sum_{i=1}^{M} [u(t - t_i) - u(t - t_i - t_{d(i)})] \tag{4.18}$$

After that, after Fourier analysis can be performed on $i_{PFD}(t)$, the coefficient is calculated as:

$$c_m = \frac{-I_d V_{th} C_r g_{mr}}{{I_r}^2 D T_{CLK}} \frac{e^{-j2\pi f_m (1-\mathrm{D}) T_{CLK}}}{(1 - e^{-j2\pi f_m T_{CLK}})} (\hat{r} e^{j\theta}) \tag{4.19}$$

Since the Fourier coefficient of v_{on} is $\hat{r}e^{j\theta}$, the describing function of v_{on}-to-i_{PFD} transfer function in the s-domain can be calculated as:

$$\frac{i_{PFD}(\mathrm{s})}{v_{on}(\mathrm{s})} = \frac{-I_d V_{th} C_r g_{mr}}{{I_r}^2 D T_{CLK}} \frac{e^{-s(1-D)\mathrm{T}_{CLK}}}{1 - e^{-s\mathrm{T}_{CLK}}} \tag{4.20}$$

Finally, the low-frequency approximation of (4.20) is derived as:

$$\frac{i_{PFD}(\mathrm{s})}{v_{on}(\mathrm{s})} \approx \frac{-I_d V_{th} C_r g_{mr}}{{I_r}^2 D {T_{CLK}}^2} \frac{1}{s} \tag{4.21}$$

For detail derivation, refer to Appendix A. Furthermore, as the v_{on}-to-i_{PFD} transfer function also contains an original pole, the compensation guideline of LPF is the same as the first PLL implementations of COT control. Moreover, because the gain is also inversely proportional to D, the issue of BW shifting appears considering the V_{in} and V_o changes.

4.2.2 Enhancement of Stability Margin with Adaptive PLL

The proposed model indicates that the two current PLL-loop implementations are difficult to compensate for, because of the limited stability region, and the BW shifting to V_{in} and V_o changes. The purpose of the proposed adaptive PLL loop is to auto-tune the gain of T_p to be constant, so that the compensation becomes simple and the PLL loop response can be easily optimized. With constant gain, Figure 4.20 demonstrates T_p BW can be anchored at peak PM, so the LPF compensation is universal with different operating conditions of VR. Also, it guarantees that T_p BW is far away from T_2 BW, such that the system still exhibits like COT control during a load transient event.

Enlightened by the proposed model in (4.10), an adaptive control is developed to improve the first PLL implementation in Figure 4.9. The goal is to fix the gain of $I_d/(S_r \cdot D)$. To achieve this, two viable circuit modifications are found. The first strategy tunes I_d/S_r to be proportional to D, i.e., I_d is proportional to V_o and S_r is proportional to V_{in}. Figure 4.21 shows the first circuit modification, where the magnitude of the internal current charge pump of the PFD is controlled by V_{ref} feed-forward through a simple current mirror with K_2 gain, and S_r is adjusted by V_{in} feed-forward through connecting a current mirror with K_1 gain to the current source I_r.

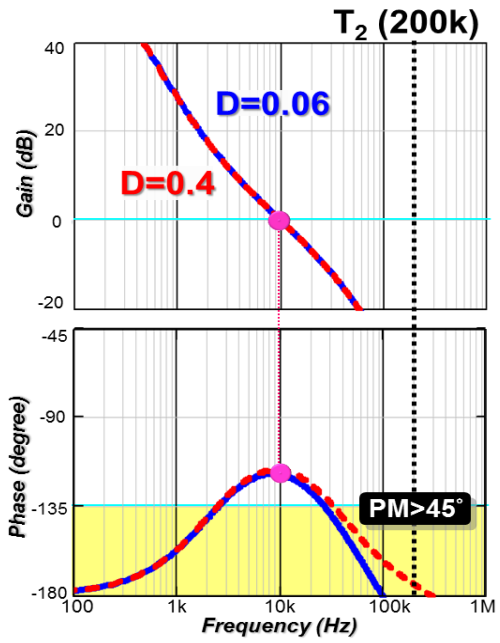


Figure 4.20 The concept of the proposed adaptive PLL loop

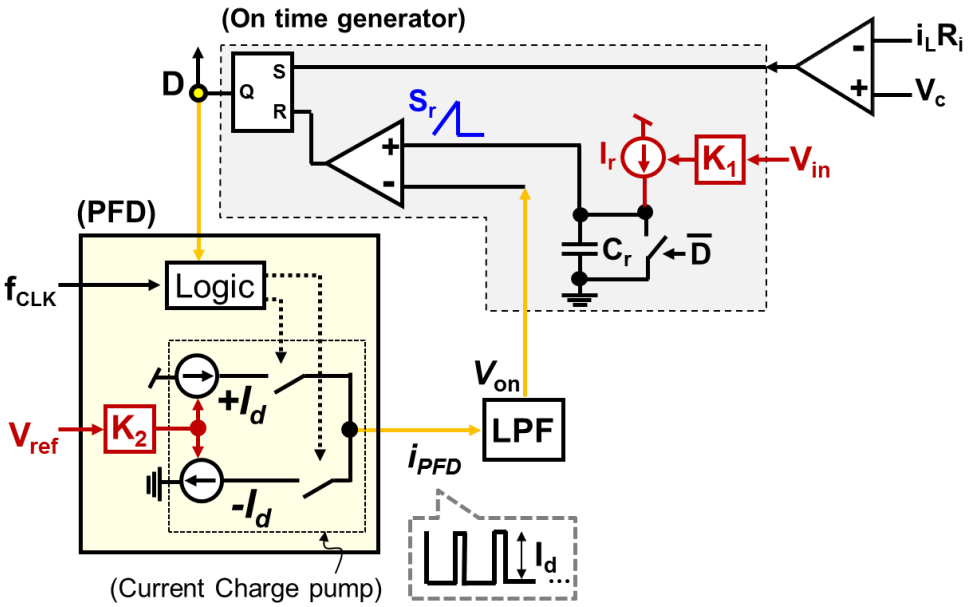


Figure 4.21 Adaptive PLL Loop with V_{in} and V_o feed-forward for COT control

Moreover, the second strategy is to fix I_d but tune S_r to be inversely proportionate to D, i.e., S_r becomes a piecewise linear ramp. Figure 4.22 shows the second circuit modification to allow

S_r to gradually reduce as D increases, where a simple switched current-mirror bank gradually reduces the current level of I_r based on the on-time length. The design of the current-mirror bank is based on the curve-fitting of the following ramp function to meet $S_r=K_1/D$:

$$V_{Sr}(t) = \int_{t=0}^{t} \frac{K_1}{t \cdot T_{CLK}} dt = \frac{K_1}{T_{CLK}} \ln(t) \tag{4.22}$$

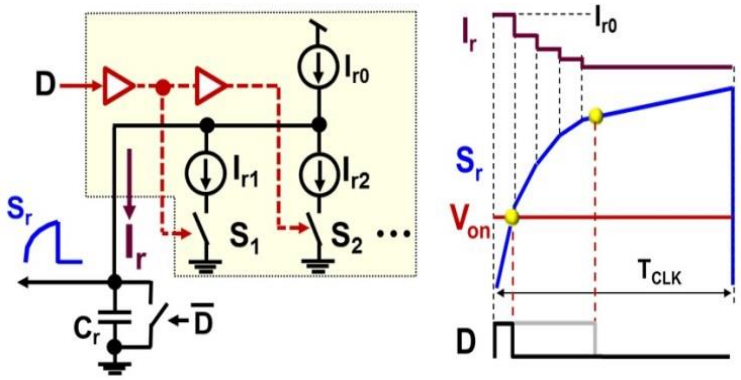


Figure 4.22 Adaptive PLL Loop with a piecewise linear ramp for COT control

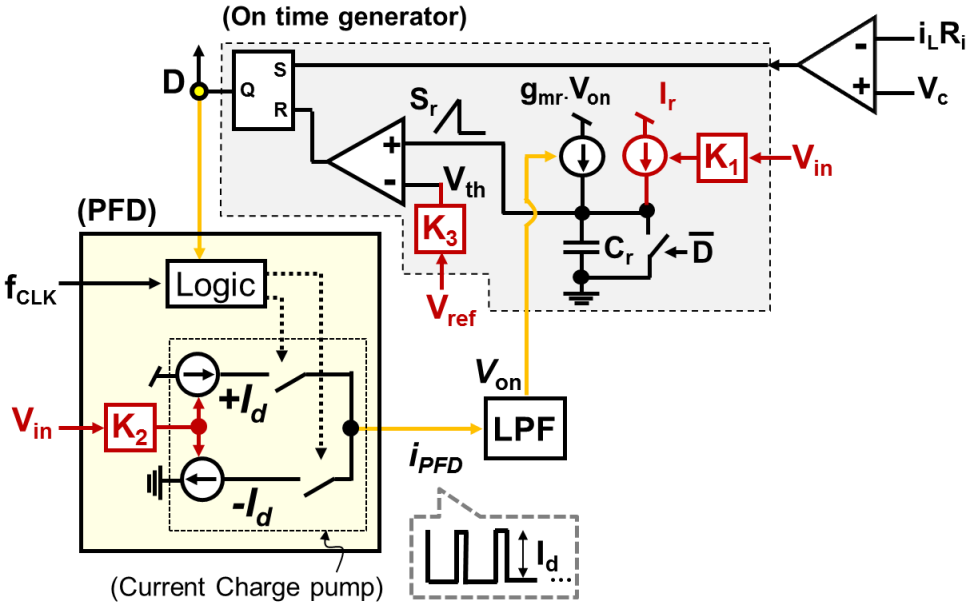
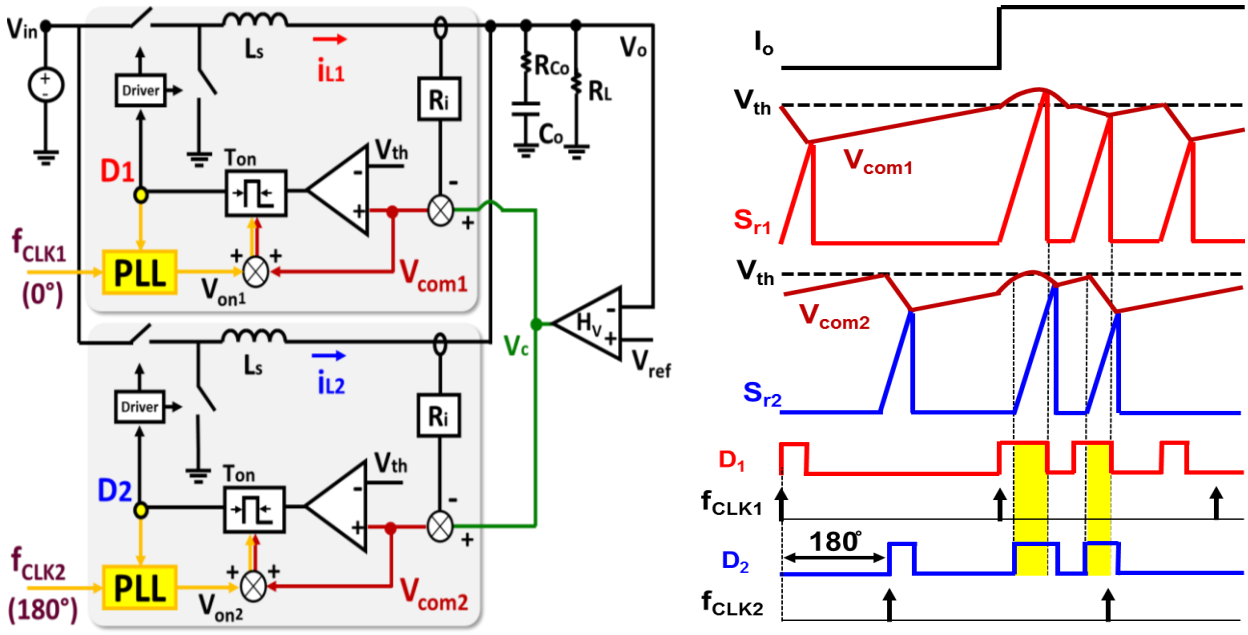


Figure 4.23 Alternative adaptive PLL loop implementation for COT control

The same methodology can be applied to the alternative PLL implementation in Figure 4.11. Based on the proposed model in (4.21), the auto-tuning objective is to fix the gain, $I_d \cdot V_{th}/(I_r^2 \cdot D)$. Specifically, I_d and I_r are proportional to V_{in}, while V_{th} is proportional to V_o. In the example implementation (Figure 4.23), the current charge pump is controlled by V_{in} feed-forward through a current mirror with K_2 gain; V_{th} is connected to V_{ref} through a voltage divider with K_3 gain; I_r is adjusted by V_{in} feed-forward through a current mirror with K_1.

4.3 Proposed Ramp Pulse Modulation with Adaptive PLL Loop

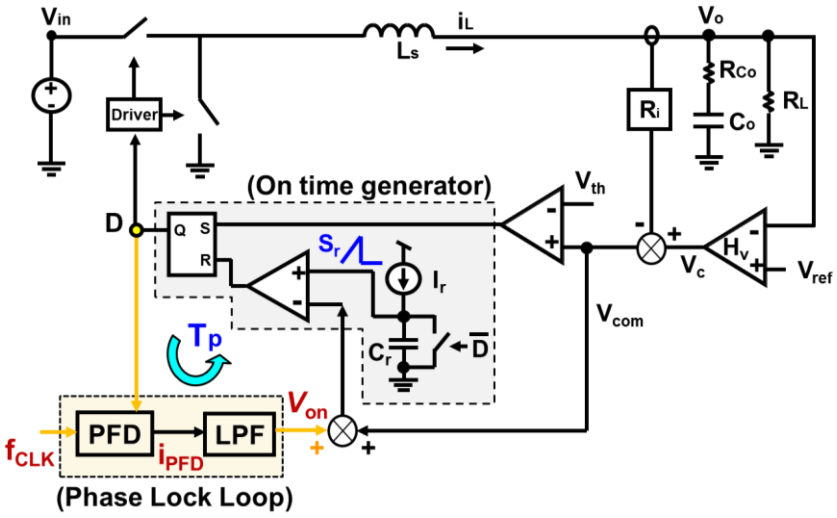
As mentioned in Chapter 1, RPM control can further improve the transient response of COT control because of the variable on-time and off-time during transient. It is worthwhile to investigate how to extend the concept of the proposed adaptive PLL loop to multiphase RPM.



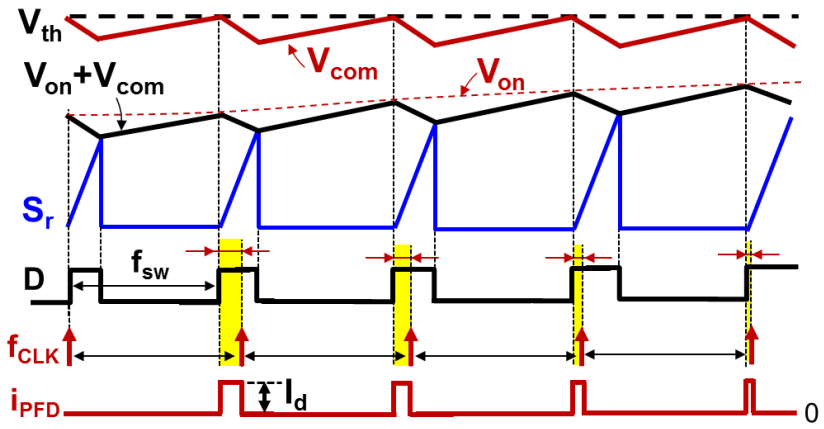
(a) (b)

Figure 4.24 Interleaving with PLL for RPM control: (a) block diagram, and (b) step-up load transient

Figure 4.24(a) shows a proposed two-phase configuration where the two PLL outputs are summed with V_{com} to change T_{on} of each phase such that D_1 and D_2 follow f_{CLK1} and f_{CLK2} respectively. Figure 4.24(b) demonstrates that this multiphase configuration can utilize the on-time extension feature of RPM control to create a more overlapping area. Therefore, the step-up load transient response is also better than the multiphase COT control.



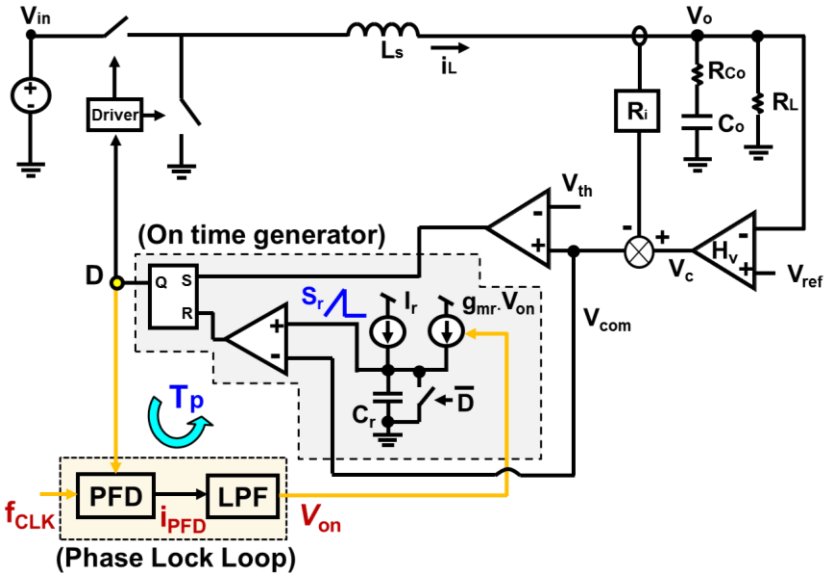
(a)



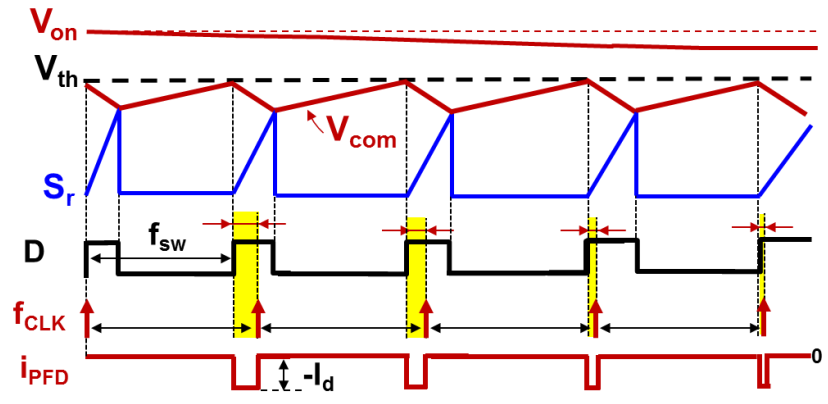
(b)

Figure 4.25 Extension of PLL loop to RPM control: (a) block diagram, and (b) operation principle

There are also two possible PLL loop implementations for RPM control. The first implementation is that V_{on} from a PLL output is summed with V_{com} to change T_{on} such that f_{sw} locks with f_{CLK}, as shown in Figure 4.25. The second implementation is that PLL loop controls T_{on} through changing S_r, as shown in Figure 4.26. Both operation principles are similar with COT control.



(a)



(b)

Figure 4.26 Alternative PLL design of RPM control: (a) block diagram, and (b) operating principle

4.3.1 Modeling and Design of PLL Loop

The modeling strategy in Section 4.2 can be very easily applied to model the PLL loop of RPM control. Along the PLL loop, the non-linear modulator consists of the PFD, the comparators, and the on-time generator. Following the same methodology, all of them are treated as a single entity, and then the transfer function from the v_{on} to i_{PFD} is derived.

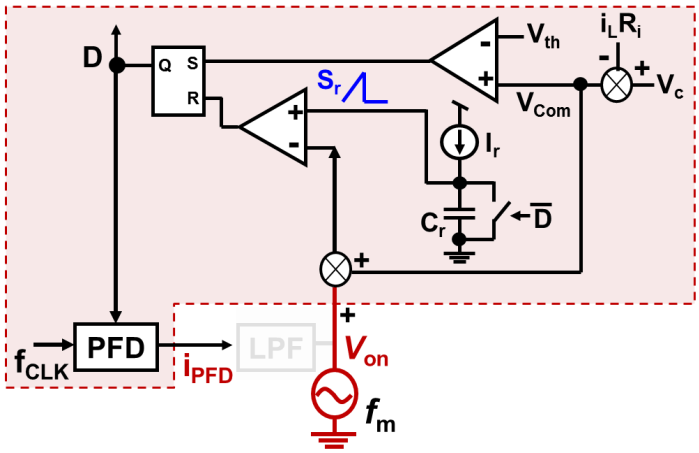


Figure 4.27 Proposed modeling methodology for PLL loop of RPM control

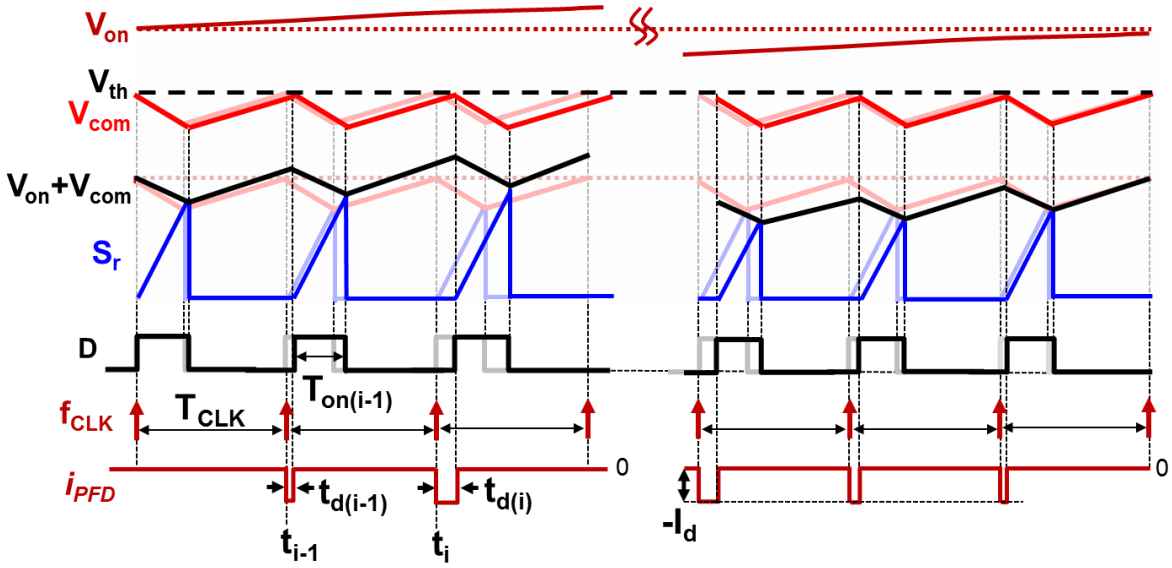


Figure 4.28 Key perturbed waveforms of the PLL loop in RPM control

For the PLL-loop implementation in Figure 4.25, the small-signal model is derived as follows. Figure 4.27 shows that after LPF is disconnected, a sinusoidal perturbation with a small magnitude at the frequency f_m is injected through the control signal v_{on}. Under the perturbation signal, $v_{on}(t)=V_{th}+\hat{r}\sin(2\pi f_m \cdot t+\theta)$, the modulated duty cycle and the perturbed i_{PFD} waveform are shown in Figure 4.28. Based on the modulation law, it is found that:

$$V_{th}-[v_c - s_n T_{on(i-1)}] = V_{th} - \{v_c - s_f [t_{d(i)} + (T_{CLK} - t_{d(i-1)} - T_{on(i-1)})]\} \tag{4.23}$$

$$T_{on(i-1)} = v_{on}(t_{i-1} + t_{d(i-1)} + T_{on(i-1)}) / (s_r + s_n) \tag{4.24}$$

Next, by substituting (4.24) into (4.23), it is found that:

$$t_{d(i)} - t_{d(i-1)} = \frac{V_{in}\hat{r}\sin[2\pi f_m \cdot (t_{i-1} + t_{d(i-1)} + T_{on(i-1)}) + \theta]}{(s_r + s_n)V_o} \tag{4.25}$$

Then, the perturbed inductor current $i_{PFD}(t)$ can be expressed by:

$$i_{PFD}(t)\Big|_{0\le t\le t_M + T_{CLK}} = -I_d \cdot \sum_{i=1}^{M} [u(t-t_i) - u(t-t_i-t_{d(i)})] \tag{4.26}$$

After Fourier analysis is performed on the i_{PFD} expression, the transfer function of v_{on}-to-i_{PFD} of RPM control can be calculated as:

$$\frac{i_{PFD}(s)}{v_{on}(s)} = \frac{-I_d}{(s_r + s_n)DT_{CLK}} \frac{e^{-s(1-D)T_{CLK}}}{1-e^{-sT_{CLK}}} \tag{4.27}$$

Finally, the low-frequency approximation of (4.27) is derived as:

$$\frac{i_{PFD}(s)}{v_{on}(s)} \approx \frac{-I_d}{(s_r + s_n)DT_{CLK}^{\ 2}} \frac{1}{s} \tag{4.28}$$

For detail derivation, refer to Appendix A.

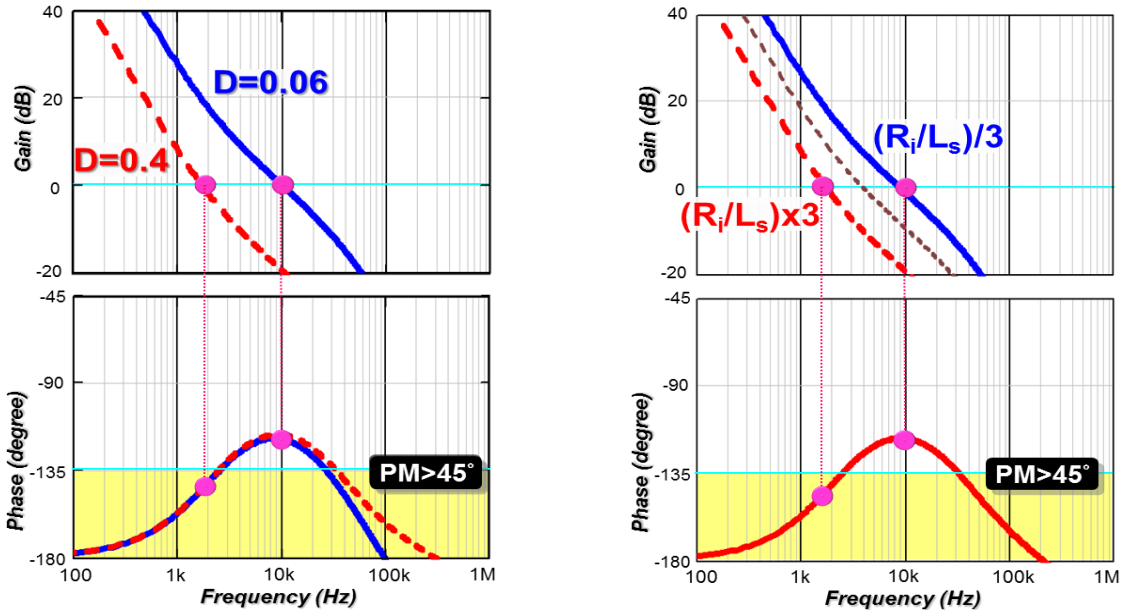


Figure 4.29 Sensitivity of T_p for RPM Control to: (a) D change, and (b) R_i/L_s variations

The similarity with COT control is that the T_p gain is inversely proportional to D, so the BW is also shifted with V_{in} and V_o changes, as shown in Figure 4.29(a). Furthermore, the major difference from the model of COT control is that the gain is inversely proportional to the sum of S_r and S_n instead of S_r only. It is found that the additional S_n term makes compensations even more complex, since S_n is a function of several parameters. Using a buck converter as example, $S_n=(V_{in}-V_o)R_i/L_s$, so T_p gain becomes dependent on R_i and L_s parameters, whose values are

highly dependent on the converter design. As Figure 4.29(b) reveals, when S_r is designed five times less than the typical S_n value, T_p BW varies between 10kHz and 1.8kHz, if R_i/L_s varies three times away for the predetermined value. Based on the above analysis, it is found that the PLL loop of RPM control is difficult to stabilize with a predetermined compensation of LPF.

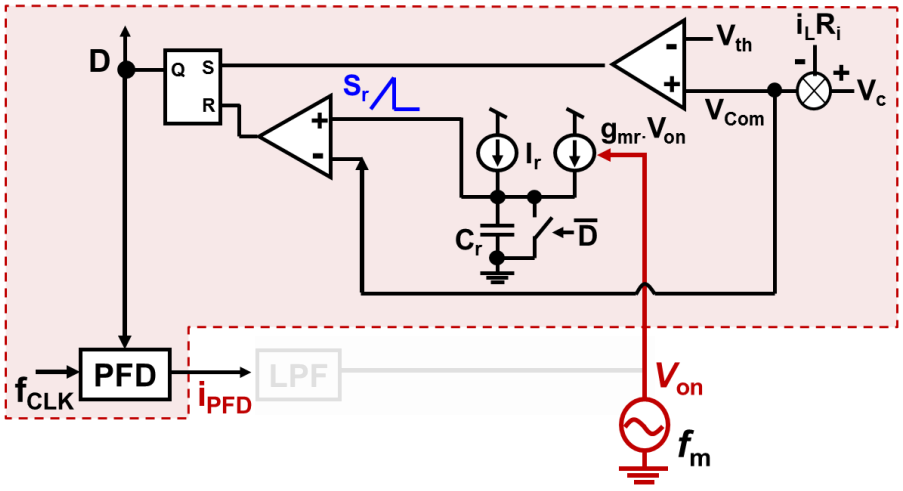


Figure 4.30 Proposed modeling methodology for the alternative PLL loop of RPM control

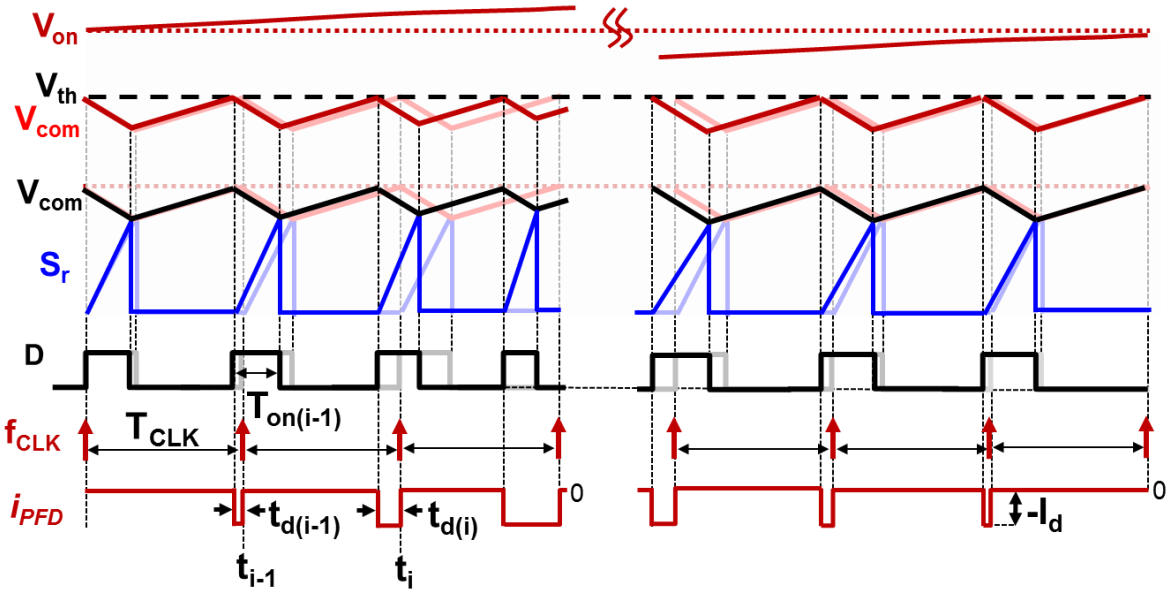


Figure 4.31 Key perturbed waveforms of the alternative PLL loop design in RPM control

For the alternative PLL loop implementation in Figure 4.26, the small-signal model is derived as follows. Figure 4.30 shows that a sinusoidal perturbation signal $v_{on}(t)=0+\hat{r}\sin(2\pi f_m \cdot t+\theta)$ is injected at the PLL output. The modulated duty cycle and the perturbed i_{PFD} waveform are shown in Figure 4.31. Based on the modulation law, it is found that:

$$V_{th}-[v_c - s_n T_{on(i-1)}] = V_{th} - \{v_c - s_f [T_{CLK} - t_{d(i)} - T_{on(i-1)} + t_{d(i-1)}]\} \tag{4.29}$$

$$s_r(t_{i-1} + T_{on(i-1)} - t_{d(i-1)}) = \frac{I_r + g_{mr} \cdot v_{on}(t_{i-1} + T_{on(i-1)} - t_{d(i-1)})}{C_r} \tag{4.30}$$

$$T_{on(i-1)} = V_{th} / [s_r(t_{i-1} + T_{on(i-1)} - t_{d(i-1)}) + s_n] \tag{4.31}$$

Next, by substituting (4.30) and (4.31) into (4.29), it is found that:

$$t_{d(i)} - t_{d(i-1)} = \frac{V_{in} V_{th} C_r g_{mr} \cdot \hat{r} \sin[2\pi f_m \cdot (t_{i-1} + T_{on(i-1)} - t_{d(i-1)}) + \theta]}{V_o (I_r + s_n C_r) \cdot \{I_r + s_n C_r + g_{mr} \cdot \hat{r} \sin[2\pi f_m \cdot (t_{i-1} + T_{on(i-1)} - t_{d(i-1)}) + \theta]\}} \tag{4.32}$$

Since $I_r + S_n C_r >> g_{mr} \cdot \hat{r} \sin[2\pi f_m \cdot (t_{i-1} + T_{on(i-1)} - t_{d(i-1)}) + \theta]$, (4.32) can be simplified as

$$t_{d(i)} - t_{d(i-1)} \approx \frac{V_{in} V_{th} C_r g_{mr} \cdot \hat{r} \sin[2\pi f_m \cdot (t_{i-1} + T_{on(i-1)} - t_{d(i-1)}) + \theta]}{V_o (I_r + s_n C_r)^2} \tag{4.33}$$

Then, the perturbed inductor current $i_{PFD}(t)$ can be expressed by:

$$i_{PFD}(t)\Big|_{0 \le t \le t_M + T_{CLK}} = -I_d \cdot \sum_{i=1}^{M} [u(t - t_i) - u(t - t_i - t_{d(i)})] \tag{4.34}$$

After that, after Fourier analysis can be performed on $i_{PFD}(t)$, the coefficient is calculated as:

$$c_m = \frac{-I_d V_{th} C_r g_{mr}}{(I_r + s_n \mathrm{C}_r)^2 D T_{CLK}} \frac{e^{-j2\pi f_m (1-\mathrm{D}) T_{CLK}}}{(1-e^{-j2\pi f_m T_{CLK}})} (\hat{r} e^{j\theta}) \tag{4.35}$$

Since the Fourier coefficient of v_{on} is $\hat{r}e^{j\theta}$, the describing function of v_{on}-to-i_{PFD} transfer function in the s-domain can be calculated as:

$$\frac{i_{PFD}(\mathrm{s})}{v_{on}(\mathrm{s})} = \frac{-I_d V_{th} C_r g_{mr}}{(I_r + s_n \mathrm{C}_r)^2 D T_{CLK}} \frac{e^{-s(1-D)\mathrm{T}_{CLK}}}{1-e^{-s\mathrm{T}_{CLK}}} \tag{4.36}$$

Finally, the low-frequency approximation of (4.36) is derived as:

$$\frac{i_{PFD}(\mathrm{s})}{v_{on}(\mathrm{s})} \approx \frac{-I_d V_{th} C_r g_{mr}}{(I_r + s_n \mathrm{C}_r)^2 D T_{CLK}^{\ 2}} \frac{1}{s} \tag{4.37}$$

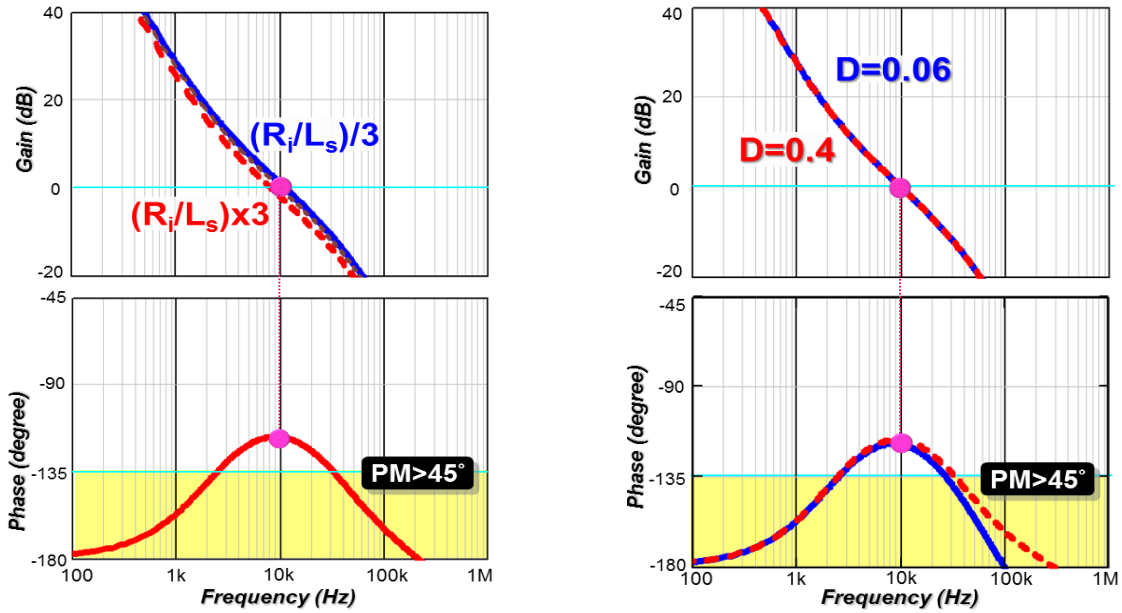
For detail derivation, refer to Appendix A. Furthermore, the model indicates that the gain is not only inversely proportional to D, but also inversely proportional to the sum of I_r and S_nC_r. Therefore, the model highlights that the BW of the PLL-loop implementation is also very sensitive to the V_{in}, V_o, R_i, and L_s variations.

4.3.2 Enhancement of Stability Margin with Adaptive PLL

Based on the knowledge of (4.28), the adaptive control for the PLL loop in Figure 4.25 is fixing the gain, $I_d/[(S_r+S_n)\cdot D]$. The first step is to design $S_r >> S_n$ so as to minimize the R_i and L_s impact. Figure 4.32(a) shows that T_p BW becomes less sensitive to R_i/L_s, when S_r is designed to be five times higher than S_n. Then, the second step is to make I_d proportional to V_o, and S_r

proportional to V_{in}, so $I_d/[(S_r+S_n)\cdot D]$ is almost a constant gain, as shown in Figure 4.32(b). Finally, the overall circuit implementation is plotted in Figure 4.33.

For the alternative PLL implementation in Figure 4.26, the model in (4.37) provides the answer to fix the gain, $I_d\cdot V_{th}/[(I_r+S_nC_r)^2\cdot D]$. The first step is to design $I_r>>S_nC_r$ to minimize the R_i and L_s impact from the S_nC_r term. Then, the second step is to design I_d and I_r proportional to V_{in}, and V_{th} proportional to V_o, as shown in Figure 4.34.



(a) (b)

Figure 4.32 T_p of the adaptive PLL loop for RPM Control to: (a) R_i/L_s variations, and (b) D changes

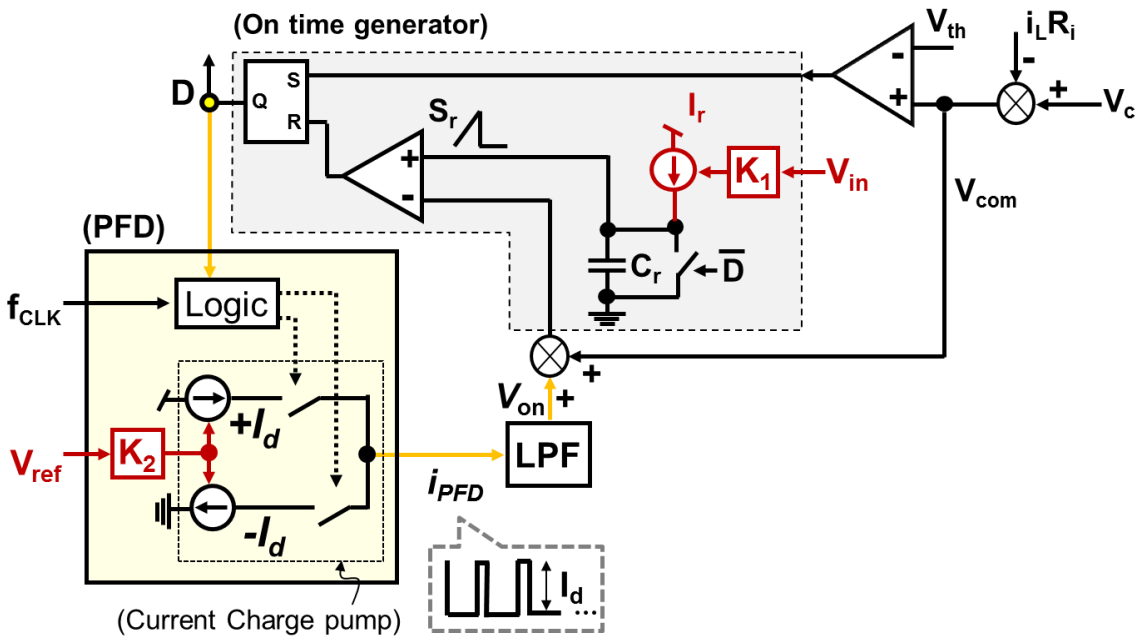


Figure 4.33 The adaptive PLL loop implementations for RPM control

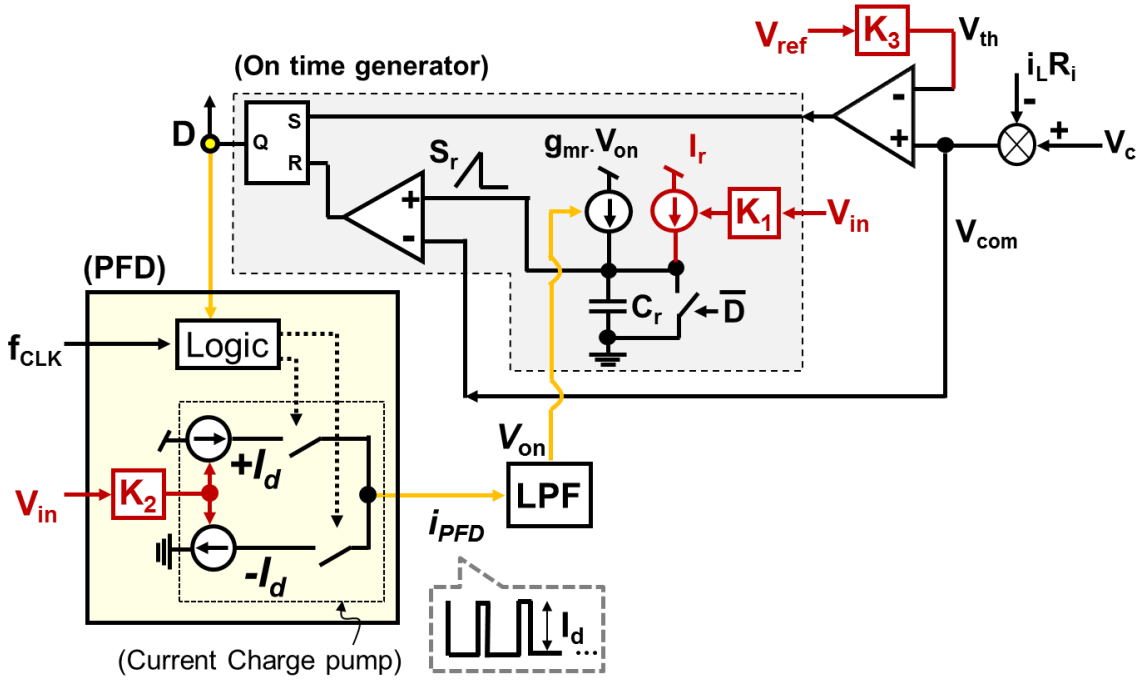
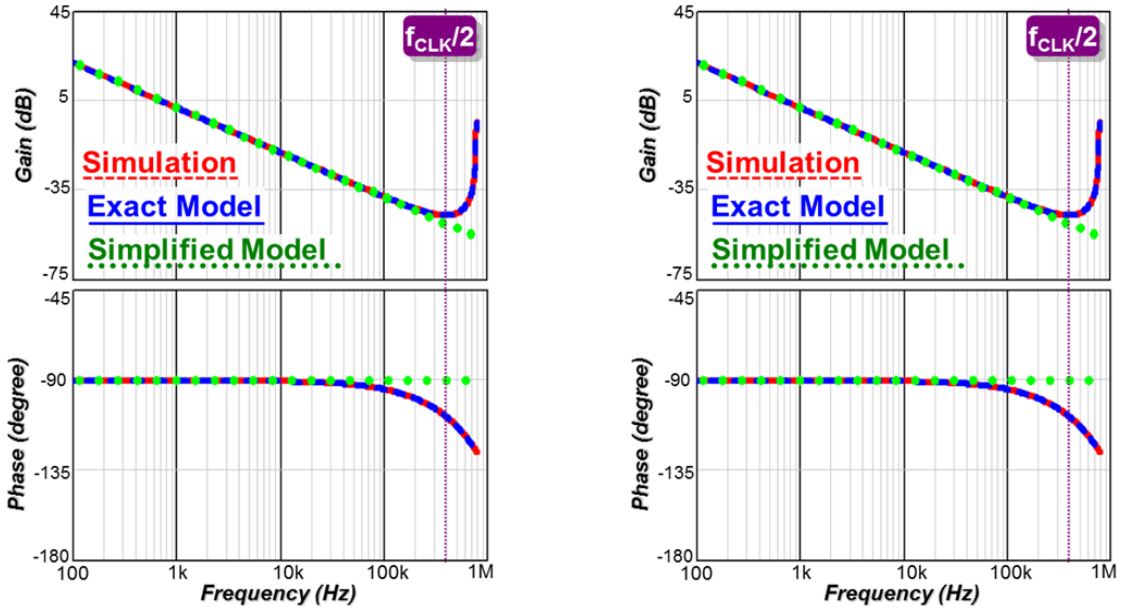


Figure 4.34 Alternative adaptive PLL loop implementation for RPM control

4.4 Verification

The adaptive PLL loop is verified on the design example of a single-phase buck converter: V_{in}=5.2V~8.4V, V_o=0.5V~2V, L_s=120nH, f_{CLK}=800kHz, R_{LL}=1.5mΩ, T_2 BW≈120kHz, and a state-of-the-art output filter without bulk capacitors, which only contains a decoupling capacitor bank outside of a CPU socket with 18·22μF and a cavity capacitor bank with 18·22μF. The simulation platform is built on SIMPLIS software.



(a) (b)

Figure 4.35 Model verification of v_{on}-to-i_{PFD} transfer function (a) COT control, and (b) RPM control

As shown in Figure 4.35, the simulation comparisons of v_{on}-to-i_{PFD} transfer function indicates that the exact model is accurate beyond $f_{CLK}/2$ for both COT control and RPM control. The peaking around f_{CLK} represents the switching component of pulsating i_{PFD}. The simulation results also verify the reasonable approximation of the simplified model up to $f_{CLK}/10$ which is useful enough for T_p design.

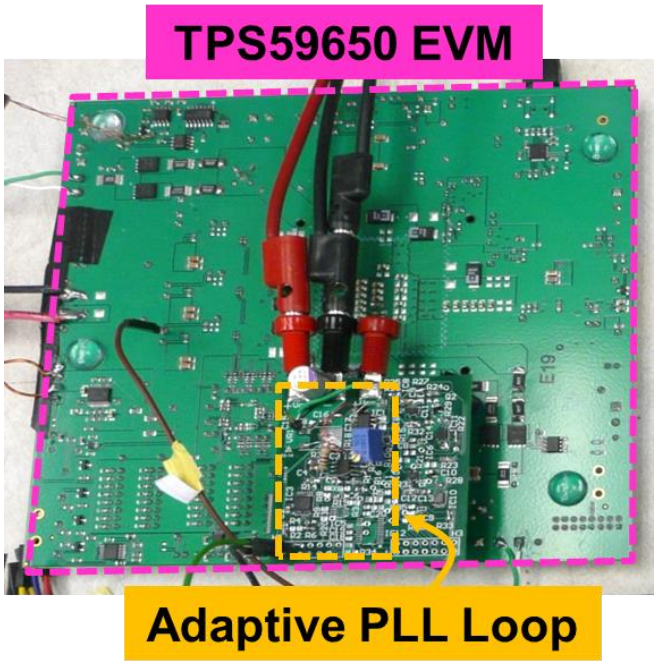
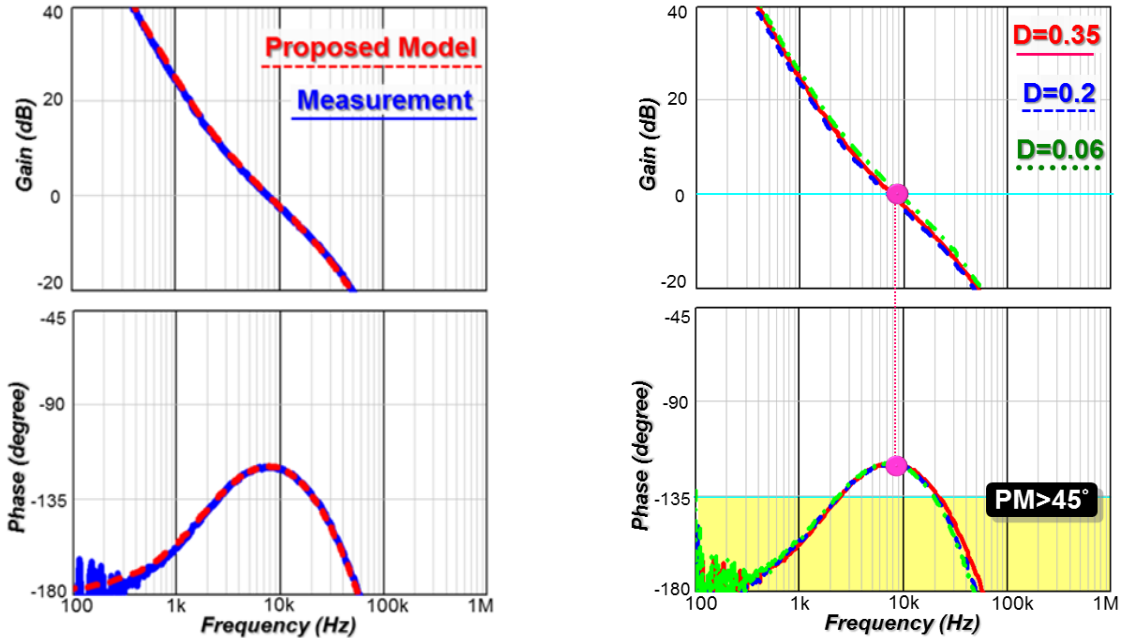


Figure 4.36 Hardware of a COT-controlled VR with proposed adaptive PLL Loop

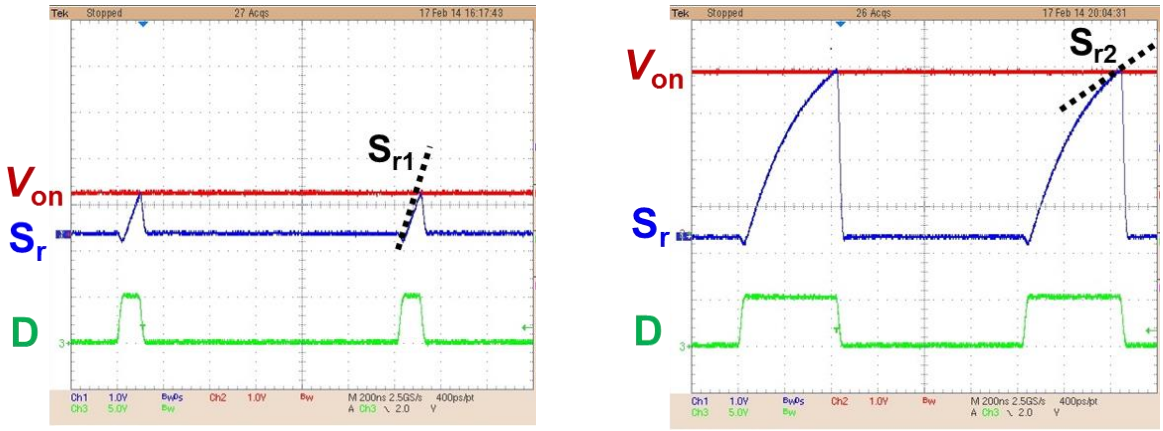
The experimental platform for the adaptive PLL loop is built with a COT-controlled VR, as shown in Figure 4.36. The adaptive PLL is implemented on a control board, which contains a PFD using TLC2932, an operational amplifier AD8062 used in LPF, and an on-time generator using a piecewise linear ramp. The LPF contains an original pole, a zero at 2kHz, a pole at 40kHz, and another pole at 100kHz. The additional pole is to enhance the attenuation to the pulsating voltage signal of 5V from the voltage charge pump inside TLC2932. The evaluation board (EVM) contains a single-phase buck converter and a COT controller, TPS59650, whose on-time is adjusted by the control board. Figure 4.37(a) is tested at V_{in}=7V and V_o=1.2V. It indicates the experimental result of T_p loop gain matches with the model, so the proposed model can accurately predict to loop response. The test results in Figure 4.37(b) confirms the effectiveness of the proposed adaptive PLL loop, which anchors BW of 9kHz at a peak stability

margin of 60° and maintains an optimal constant BW over a wide D range. The adaptive PLL loop is implemented with a piecewise linear ramp, as shown in in Figure 4.38.



(a) (b)

Figure 4.37 T_p of adaptive PLL loop: (a) model verification, and (b) Sensitivity to different D



(a) (b)

Figure 4.38 Piecewise linear ramp in adaptive PLL loop: (a) D=0.06, and (b) D=0.35

4.5 Summary

A variable-frequency control with a PLL loop not only takes advantage of a high-BW design, but also can fix the steady-state switching frequency and achieve interleaving. In this chapter, a generic small-signal model of PLL loop is proposed for two widely-used variable frequency controls, and it is found that the challenges of PLL loop compensation come from the unique loop gain characteristic. Then, enlightened by the proposed model, a simple adaptive PLL loop is developed to enhance the stability margin automatically even under parameter variations. The auto-tuning concept and example implementations are applicable to COT and RPM control. Finally, the effectiveness of the adaptive PLL loop is verified with the simulation and experimental results.

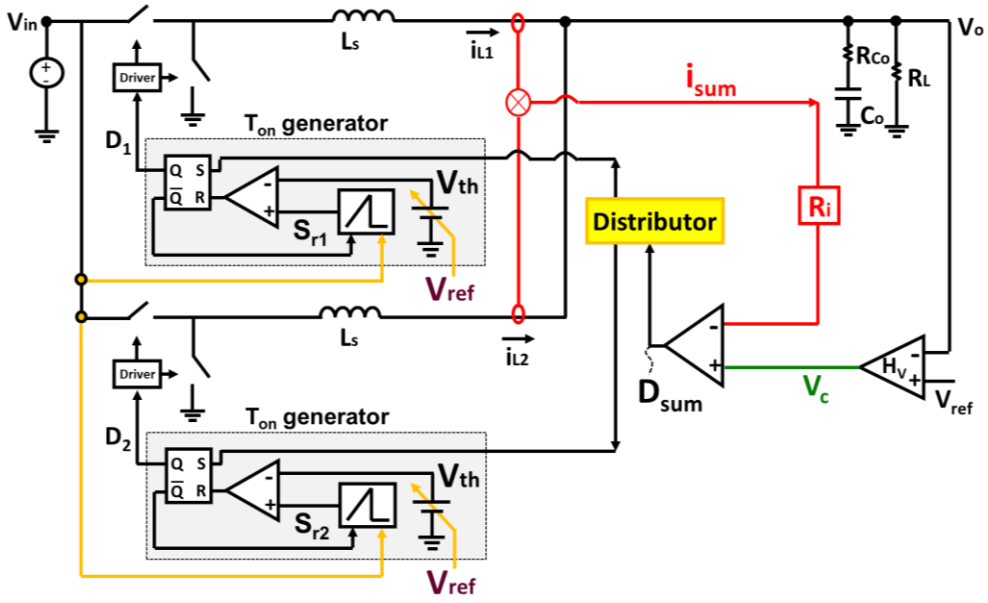
Chapter 5. Extension of Proposed Control Schemes to Multiphase VRs

Research shows that the variable-frequency control with the adaptive PLL loop mentioned in Chapter 4 can push BW design higher, and improve the transient response of multiphase VRs with natural pulse overlapping feature. However, the number of adaptive PLL loop in each phase becomes a barrier for high-current VRs with a high phase number. At the beginning, a simpler interleaving structure with no PLL loop is reviewed and the limitations in multiphase VRs are discussed. Then, a new hybrid interleaving structure is developed to solve both limitations by combining the two structures. Finally, the effectiveness is verified with simulation and experimental results.

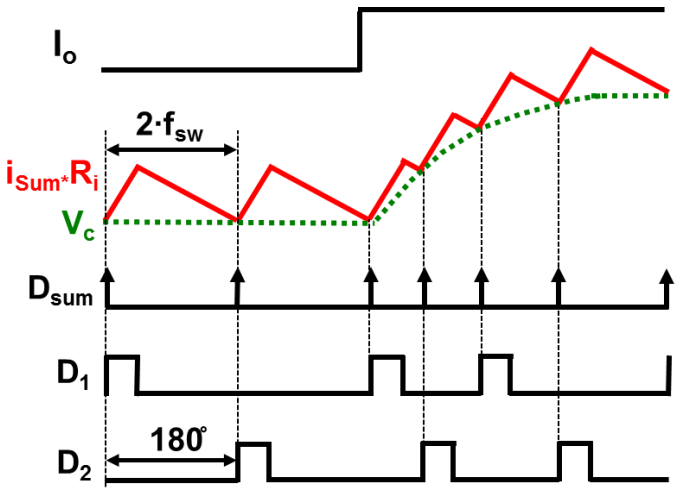
5.1 Review of State-of-the-Art Interleaving Structure

An alternative interleaving method for variable-frequency control is called a pulse distribution structure [E.1][E.2][E.3][E.4][E.5][E.6][E.7]. It has been widely used in the latest COT controllers, such as TI's TPS59650, Richtek's RT8859M, and Maxim's MAX15569. Figure 5.1(a) shows the two-phase configuration of the COT control, and Figure 5.1(b) explains the operation principle [E.1][E.2][E.3][E.4][E.5][E.6]. The modulation of D_{sum} pulse is determined by the intersection between the summed inductor current ripple (i_{sum}) and the control voltage (V_c). A pulse distributor (which is also named as a phase manger or a phase splitter) then spreads the sequential D_{sum} pulse to the on-time generator of each phase one by one. The distributed D_{sum} pulse initiates the rising edge of D_1 and D_2, while the T_{on} period is

predetermined by the on-time generator. Since the frequency of i_{sum} ripple and D_{sum} is $2 \cdot f_{sw}$, a 180° phase shift is automatically achieved after D_{sum} is distributed.

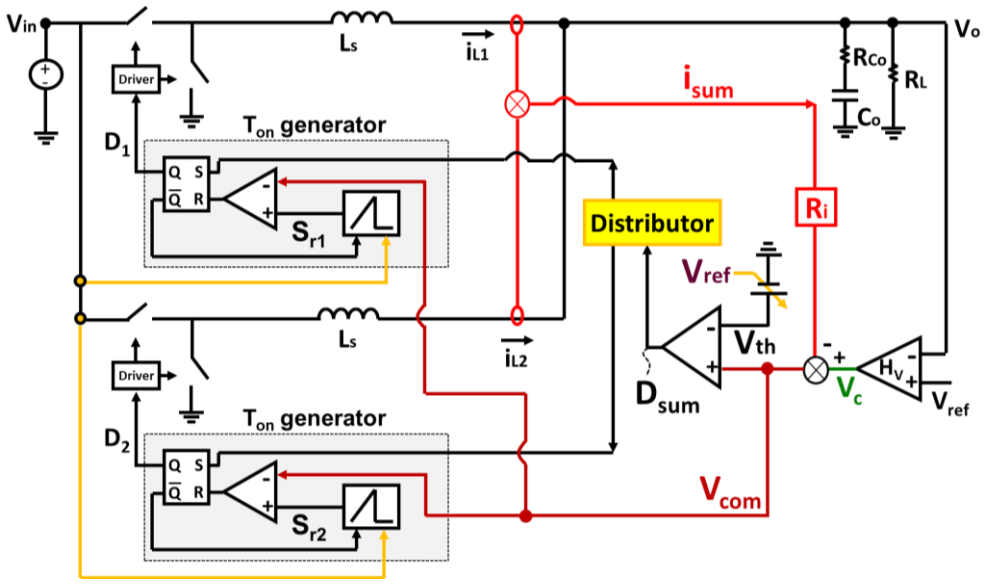


(a)

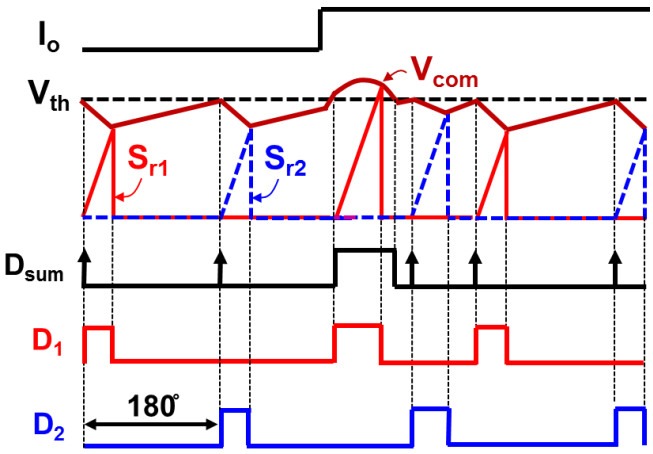


(b)

Figure 5.1 Pulse distribution structure for COT control: (a) block diagram, and (b) step-up load transient



(a)



(b)

Figure 5.2 Pulse distribution structure for RPM control: (a) block diagram, and (b) step-up load transient

Similarly, the pulse distribution structure is also applied to multiphase RPM control, as shown in Figure 5.2(a), and Figure 5.2(b) explains the operation principle [E.7]. The D_{sum} pulse is generated by comparing V_{com} with V_{th}, and a pulse distributor then spreads D_{sum} pulse to each phase one by one, so the rising edge of D_1 and D_2 is obtained. The T_{on} period of D_1 and D_2 is

determined by comparing V_{com} with individual S_r in the on-time generator of each phase, i.e. S_{r1} for on time of D_1 and S_{r2} for on time of D_2. Since the V_{com} ripple is $2 \cdot f_{sw}$, a 180° phase shift is automatically achieved, after the D_{sum} pulse is distributed.

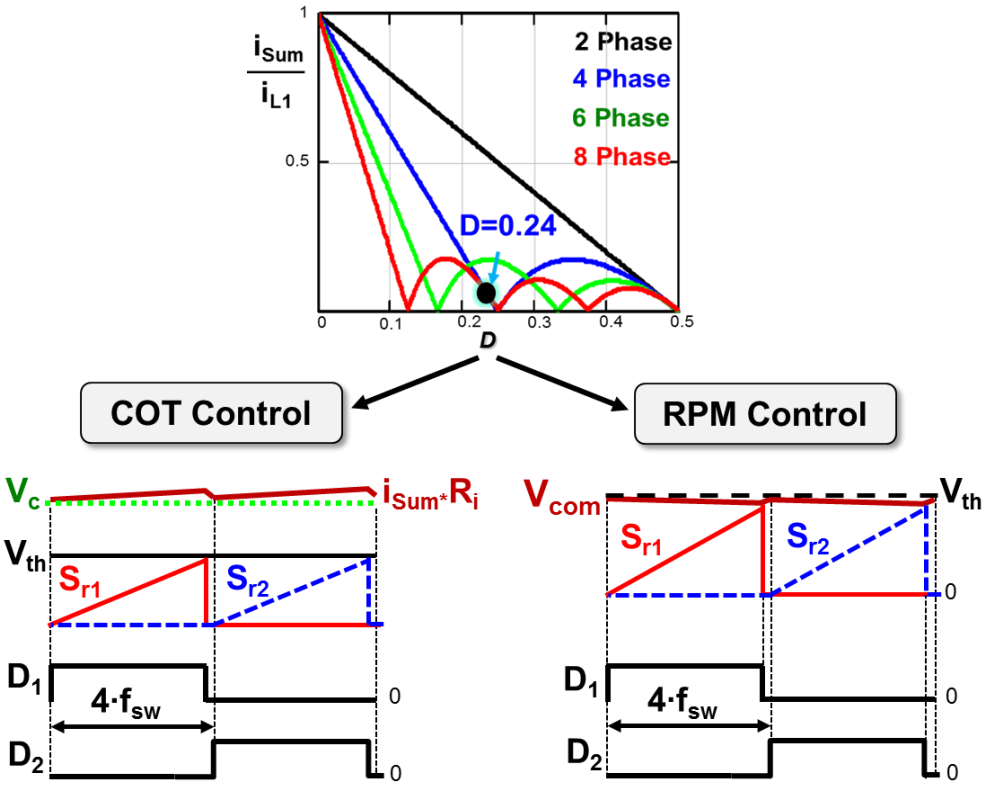
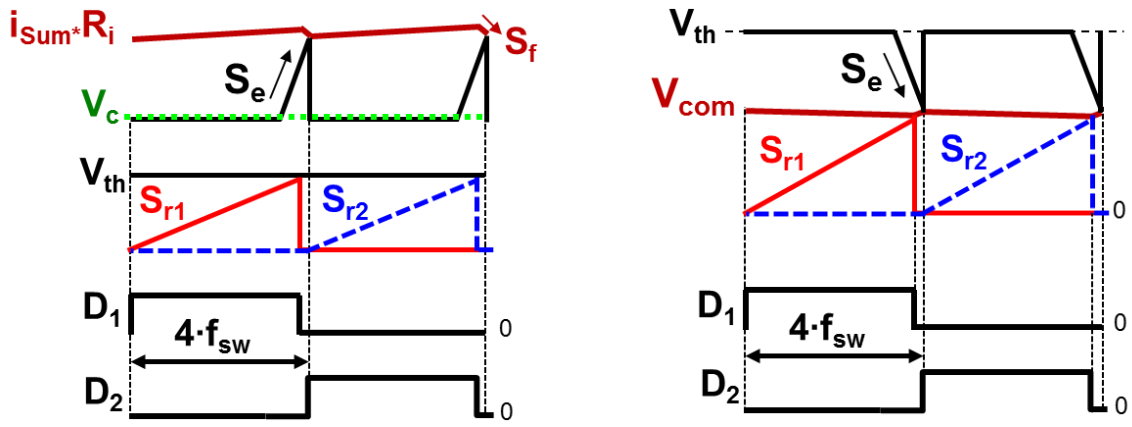


Figure 5.3 The ripple cancellation effect of i_{sum} on variable-frequency control

Although the pulse distribution structure achieves interleaving easily without using PLL loops, the step-up load transient response is worse than the proposed adaptive PLL structure. Since the pulse distributor only allows one phase to turn ON one at a time, D_1 and D_2 cannot be synchronized during step-up load transient, as shown in Figure 5.1(b) and Figure 5.2(b). In the end, more output capacitors may be needed to minimize the V_o undershoot. The second issue is that the ripple cancellation effect of i_{sum} makes the system noise-sensitive. As shown in Figure 5.3, when the i_{sum} ripple is almost gone at D≈0.24 in four-phase operation, any small amount of

noise changes the timing of D_1 and D_2, so severe duty cycle jittering occurs in steady state [E.3]. Then, it is possible to lose interleaving during jittering, so the V_o ripple becomes much higher and the transient response can be degraded.



(a) (b)

Figure 5.4 Se compensation for multiphase operation: (a) COT control [E.3], and (b) RPM control [E.7]

As shown in Figure 5.4, some literature suggests adding an external ramp (S_e) to keep enough off-time ripple to produce for less jittering [E.3][E.5][E.7][E.8]. However, from a system stability point of view, the external ramp compensation is not necessary for variable-frequency control [A.39][A.40][A.41]. Additional S_e introduces a significant phase delay, so the third issue is to limit BW for a wide D range [E.3][E.8]. Since i_{sum} ripple disappears around a cancellation point, a small amount of S_e can easily over-compensate the current loop causing the benefit of current mode control to diminish. Using COT control with S_e compensation as an example, the equivalent circuit model is no longer an ideal voltage-controlled current source as Figure 4.1. Instead, the dynamic of the S_e compensation creates an additional impedance branch which is formed by R_{e2} and L_{e2} in the current source, as shown in Figure 5.5 [E.8].

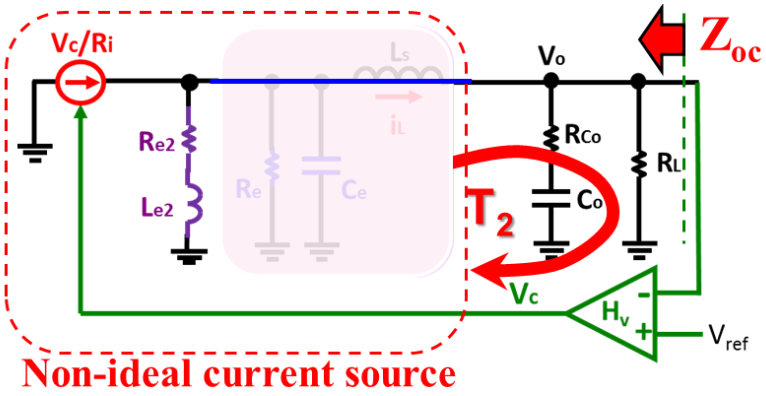
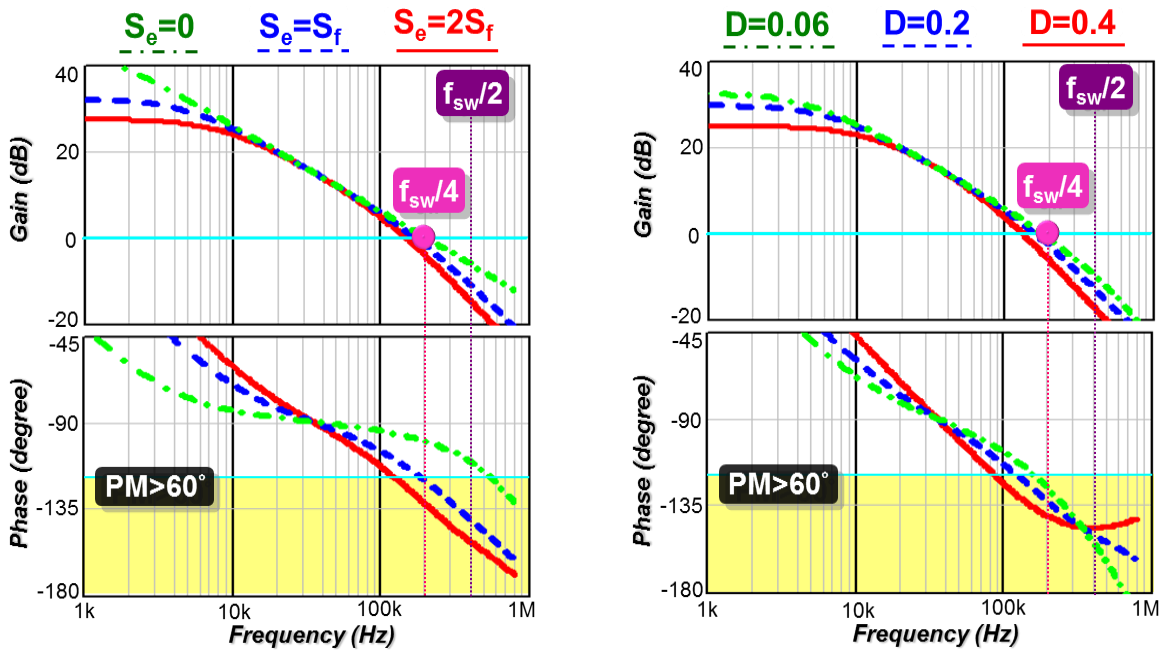


Figure 5.5 The equivalent circuit model of COT control with S_e compensation [E.8]

Based on the equivalent circuit model, the simplified T_2 loop gain of COT control with external ramp compensation is:

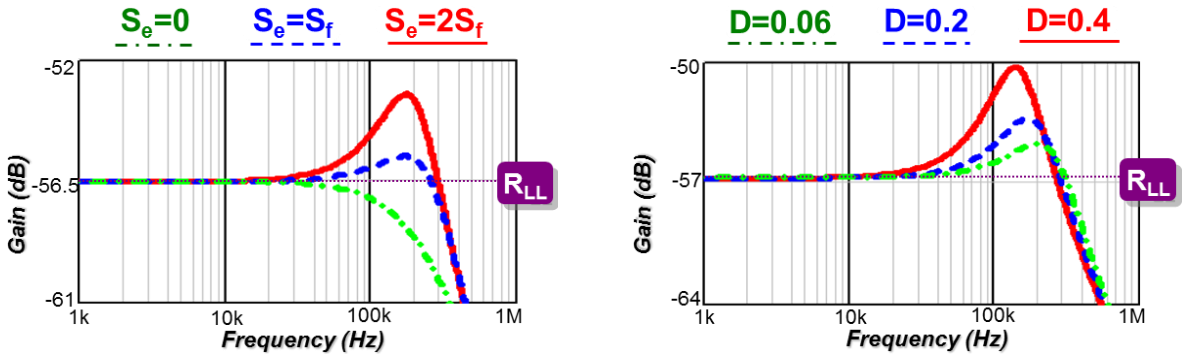
$$T_2(s) \approx \frac{R_L}{R_i}\frac{R_{Co}C_o s+1}{R_L C_o s+1}\frac{1+\frac{T_{sw}}{2}s}{1+\left(\frac{s_e}{s_f}+\frac{1}{2}\right)T_{sw}s}\frac{H_v(s)}{1+\frac{s}{\omega_1 Q_1}+\frac{s^2}{\omega_1^2}} \tag{5.1}$$

The model indicates that the branch introduces an additional pole-zero pair on the control-to-output-voltage transfer function, where the stationary zero is located at f_{sw}/π but the pole can move from f_{sw}/π toward a lower frequency as S_e increases [E.8]. Since the pole introduces significant phase delay, Figure 5.6(a) demonstrates that adding S_e results in a poor PM for a high-BW design close to $f_{sw}/4$, when D=0.2. Moreover, Figure 5.6(b) shows the effect of a fixed S_e design on T_2 under wide D range, when S_e=S_f at D=0.4. It is found that D change makes the pole further moved to a lower frequency, so a high-BW design becomes more difficult. In the end, S_e causes a detrimental effect on output impedance characteristic, as shown in Figure 5.7.



(a) (b)

Figure 5.6 Effect of S_e on T_2 of COT control: (a) different S_e design, and (b) different D range



(a) (b)

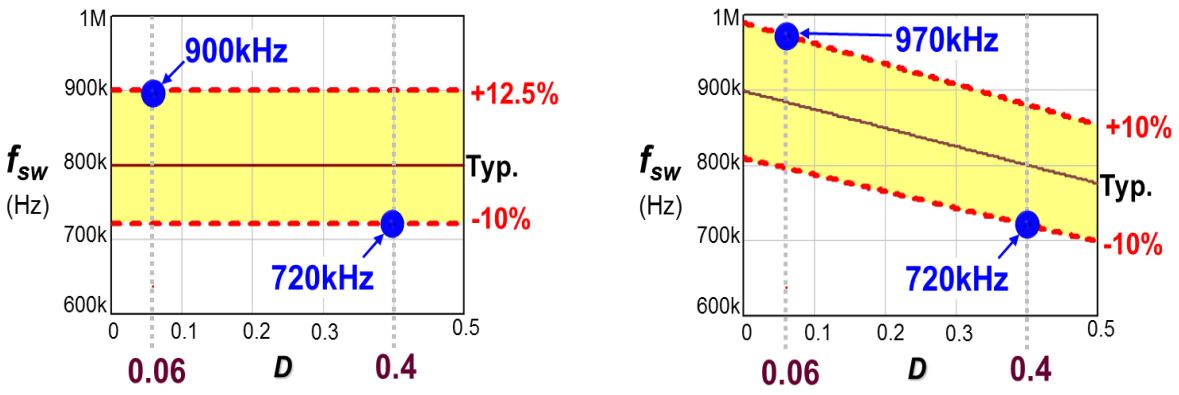
Figure 5.7 Effect of S_e on Z_{oc} of COT control: (a) different S_e design, and (b) different D range

The fourth issue is that the variation of steady-state f_{sw} makes the converter operating away from the optimized design point. For example, if f_{sw} is higher than expected, the switching loss increases. On the contrary, if f_{sw} is lower than expected, the highest control BW is limited by the

lowest f_{sw}. In a pulse distribution structure, V_{in} and V_o feedforward to the on-time generator such that the f_{sw} variation can be minimized. Based on the on-time generator design of COT control in Figure 5.1(a), the steady-state f_{sw} can be derived as:

$$f_{sw} \approx \frac{V_o}{V_{in}} \frac{S_r}{V_{th}} \tag{5.2}$$

Since S_r is proportional to V_{in} and V_{th} is proportional to V_{ref}, f_{sw} becomes less sensitive to V_{in} and V_o changes. However, the analog T_{on} generation scheme cannot guarantee f_{sw} to be the expected value due to S_r tolerance, V_{th} tolerance, and even the effect of load dependence [D.1]. According to the T_{on} tolerance in the specification of industry products, the f_{sw} variation of TI's TPS59650 is between -10% to 12.5%, the f_{sw} variation of Richtek's RT8859M is between -11% to 9%, and the f_{sw} variation of Maxim's MAX15569 is between -12% to 9.6% [E.4][E.5][E.6]. Figure 5.8(a) highlights the worst f_{sw} variation range under different D conditions, when typical f_{sw} is 800kHz.



(a) (b)

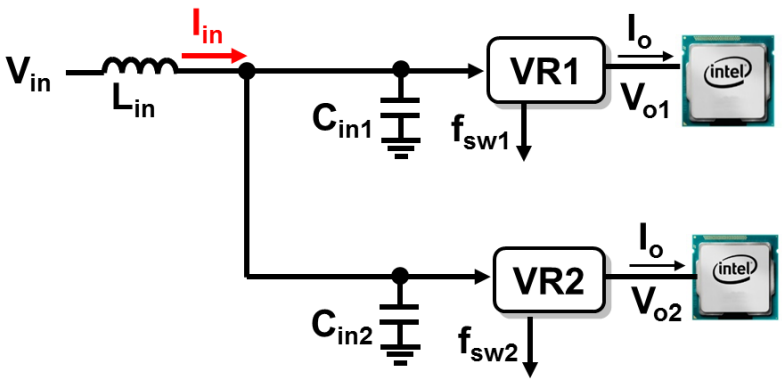
Figure 5.8 f_{sw} variation of pulse distribution structure: (a) COT control, and (b) RPM control

Based on the on-time generator design of the RPM control in Figure 5.2(a), the steady-state f_{sw} can be derived as:

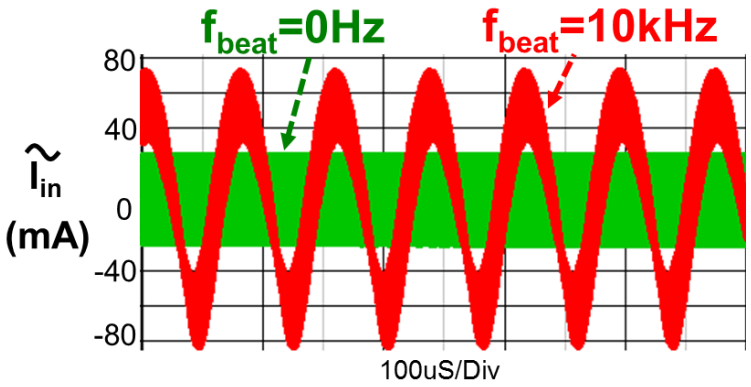
$$f_{sw} \approx \frac{V_o}{V_{in}} \frac{S_r + S_n}{V_{th}} \tag{5.3}$$

where S_r is proportional to V_{in}, V_{th} is proportional to V_{ref}, and S_n is on-time slope of V_{com}, which is equal to $(V_{in}-V_o)R_i/L_s$. Unlike (5.2), (5.3) indicates S_r and V_{th} cannot fully cancel the V_o/V_{in} term due to the existence of S_n, so the f_{sw} variation becomes worse than the COT control. Moreover, the T_{on} tolerance of the RPM controller contributes to even more variation. According to the V_{th} tolerance of On-Semiconductor's ADP3212, f_{sw} tolerance is +/-10% [E.9]. Then, Figure 5.8(b) highlights the worst f_{sw} variation range under different D range, when typical f_{sw} of 800kHz is designed at D=0.4.

The fifth issue is that the variation of the steady-state f_{sw} in Figure 5.8 generates undesired beat-frequency ripple in the system with multiple VRs, so the structure causes a higher conduction loss, a larger size of input filter, and the stronger low-frequency interference to the load. Figure 5.9 shows a simulation example to demonstrate the severity of the beat-frequency ripple from two VRs sharing same input voltage, where each VR applies a two-phase pulse distribution structure. The power stage parameters of the two VRs are as following: f_{sw1}=800kHz, f_{sw2}=790kHz, V_{in}=8.4V, V_o=1.8V, I_o=40A, L_s=150nH, C_o=22μF·36 (ceramic cap), L_{in}=0.5μH, C_{in}=470μF·1 (OSCON cap) // 10μF·4 (ceramic cap), and two-phase operation per VR. More low-frequency components would be superimposed on the input current ripple, when more VRs are connected to the input source.



(a)



(b)

Figure 5.9 Two VRs using pulse distribution structure: (a) block diagram, and (b) beat-frequency ripple

Based on the above studies, although the pulse distribution structure completely discards the PLL loops to simplify the interleaving, but the system performance suffers significantly. The poor transient response and inability to achieve high BW design may make the bulk output capacitors unable to be fully eliminated on the motherboard. Also, the f_{sw} variation can affect efficiency, and the beat frequency oscillation appears for a system with multiple VRs.

5.2 Proposed Hybrid Interleaving Structure

A hybrid interleaving structure is proposed to solve the circuit complexity of the adaptive PLL structure by combining with the pulse distribution structure. The basic concept is properly choosing the number of phases to sum the inductor current according to a no ripple cancellation point in interested duty cycle range. By doing this, the number of PLL loops and comparators can be minimized without suffering the issue of pulse distribution structure.

5.2.1 Application to Constant On-Time Control

A four-phase VR with proposed hybrid interleaving structure for wide D range is shown in Figure 5.10. Using the laptop VR with D=0.06~0.4 as an example, the magnitude ratio of i_{sum} to i_{L1} in Figure 5.3 shows that there is no ripple cancellation point within this D range for two phases, but one exists for four phases at D=0.25. Therefore, a pulse distribution structure is applied for every two phases, such that phase angles between the first and second phases as well as between the third and fourth phases are in 180° phase shift respectively. Then, two PLL loops can be used where one PLL loop forces the first phase to follow f_{clk1} with 0° by adjusting T_{on} on the first and second phases together, and another forces the third phase to follow f_{clk2} with 90° by adjusting T_{on} on the third and fourth phases. f_{clk1} and f_{clk2} can be either generated from a clock generator inside the controller or from an external system clock which synchronizes f_{sw} of multiple VRs in a system. Compared to the entire PLL structure, the hybrid interleaving structure eliminates two PLL loops and two current-loop comparators.

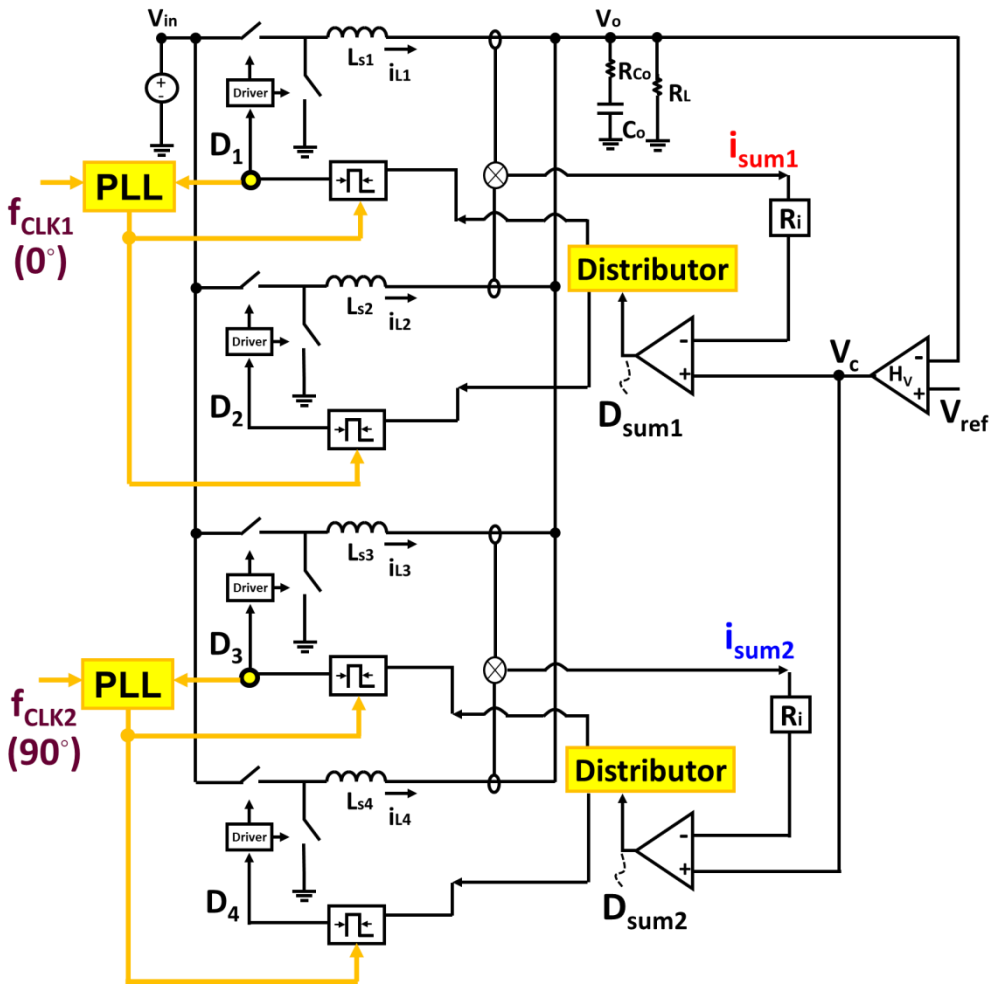


Figure 5.10 Hybrid interleaving structure of COT control for wide D range

Furthermore, if the f_{sw} variation or the beat-frequency ripple could be tolerated in certain VR designs, one more PLL loop can be removed as Figure 5.11. A delay-line circuit delays the D_1 in $T_{sw}/4$ as a reference clock of the PLL loop. The single PLL loop is only used to ensure D_1 and D_3 in a 90° phase shift by forcing the third phase to follow the delayed reference clock. Meanwhile, each on-time generator senses V_{in} and V_{ref} to minimize f_{sw} error.

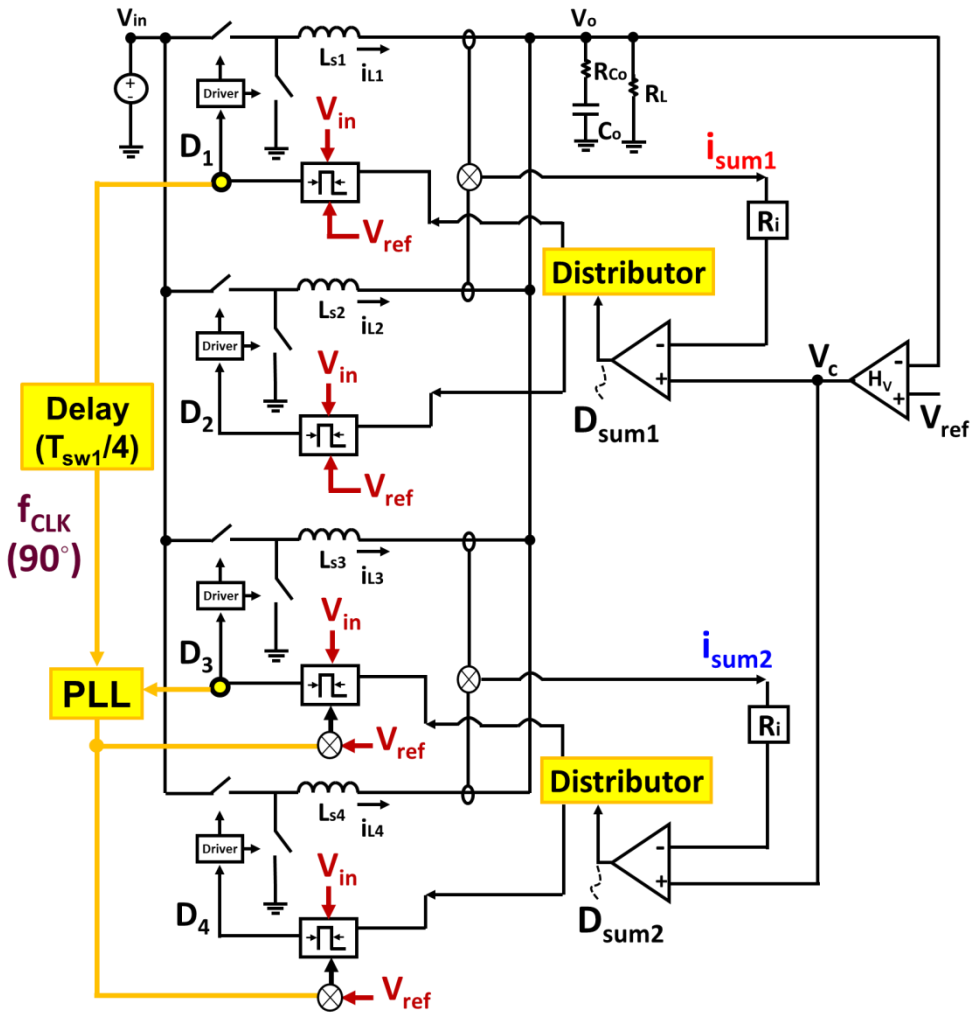


Figure 5.11 Simplified hybrid interleaving structure of COT control for wide D range

For a narrower D range application, the hybrid interleaving can eliminate even more PLL loops and related components. Using a desktop/server VR with D=0.06~0.15 (V_{in}=12, V_o=0.5~2V) as an example, the magnitude ratio of i_{sum} to i_{L1} shows that there is no ripple cancellation point up to the five-phase operation. For an eight-phase VR design of a server, the pulse distribution structure is applied to every four phases as shown in Figure 5.12, such that the phase angles among first to fourth phases as well as among fifth to eighth phases are in 90° respectively. Then, two PLL loops are used where one PLL loop forces the first phase to follow

f_{clk1} with 0° by adjusting T_{on} among the first to fourth phases together, and another PLL forces the fifth phase to follow a f_{clk2} with 45° by adjusting T_{on} among the fifth to eighth phases. Compared to the entire PLL structure, six PLL loops and six current-loop comparators are removed. Besides, one of the two PLL loops can be removed if the f_{sw} variation and the beat frequency can be tolerated.

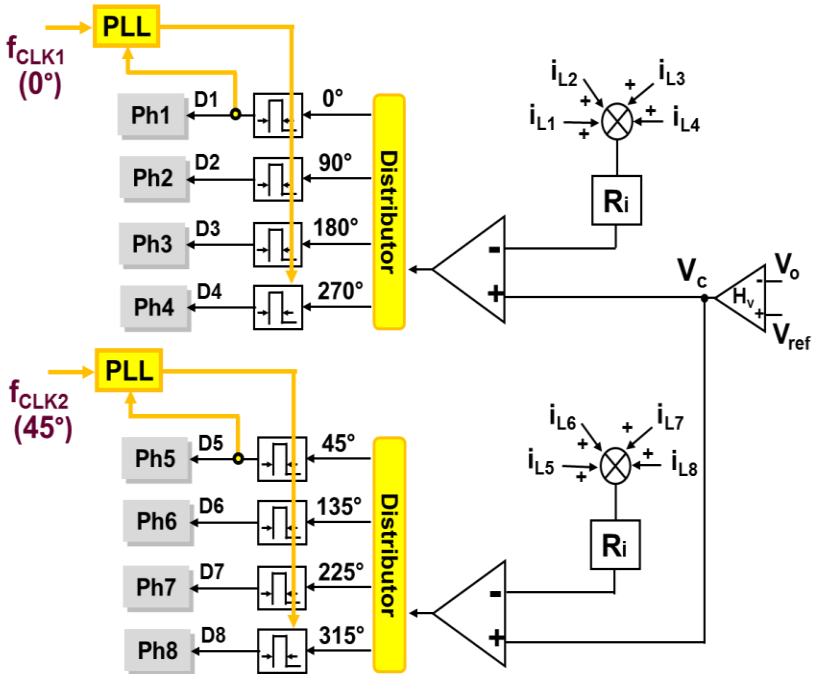


Figure 5.12 Hybrid interleaving structure of COT control for narrow D range

The hybrid interleaving preserves the natural overlapping feature of the adaptive PLL structure. Figure 5.13 illustrates that the gate signals between the two pulse-distribution groups can be overlapped naturally, because the summed current signals of the two groups compare with the V_c individually, and the two adaptive PLL loops in low BW design allow the gate signal lost tracking with clock signals during transient. The overlapping areas are automatically increased on demand, when load transient event becomes more severe.

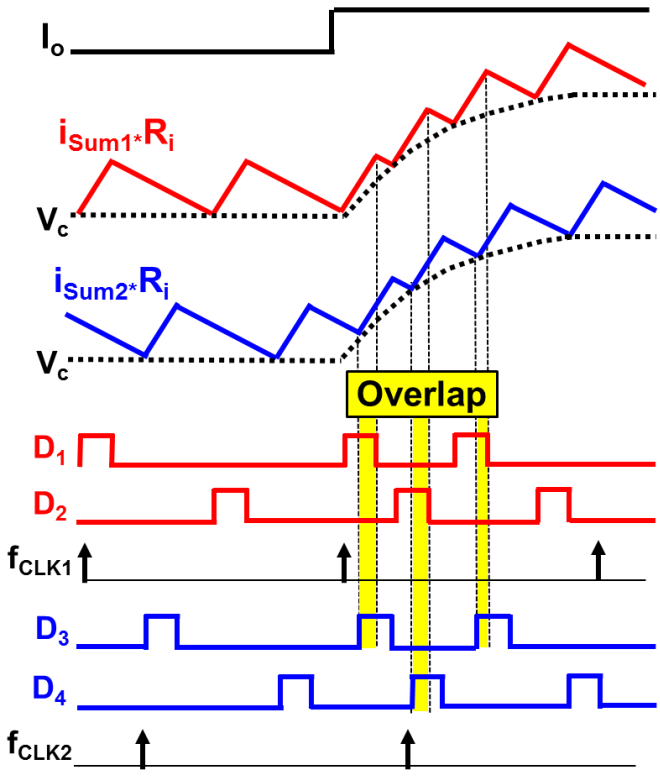


Figure 5.13 Step-up load transient of hybrid interleaving structure using COT control

5.2.2 Application to Ramp Pulse Modulation

The same methodology applies to the RPM control. The hybrid interleaving structure for the wide D range is shown in Figure 5.14. Since V_{com} of RPM control contains i_{sum} ripple, the magnitude ratio of i_{sum} to i_{L1} in Figure 5.3 also represents the ripple ratio of V_{com} to i_{L1}. To avoid a ripple cancellation point for the wide D range, a pulse distribution structure is applied for every two phases. Then, the two PLL loops can be used to force D_1 to follow f_{clk1} with 0° and D_3 to follow f_{clk2} with 90°. Besides, for a narrow D range application, more phase current can group together to further minimize the number of PLL loops and comparators, as shown in Figure 5.15.

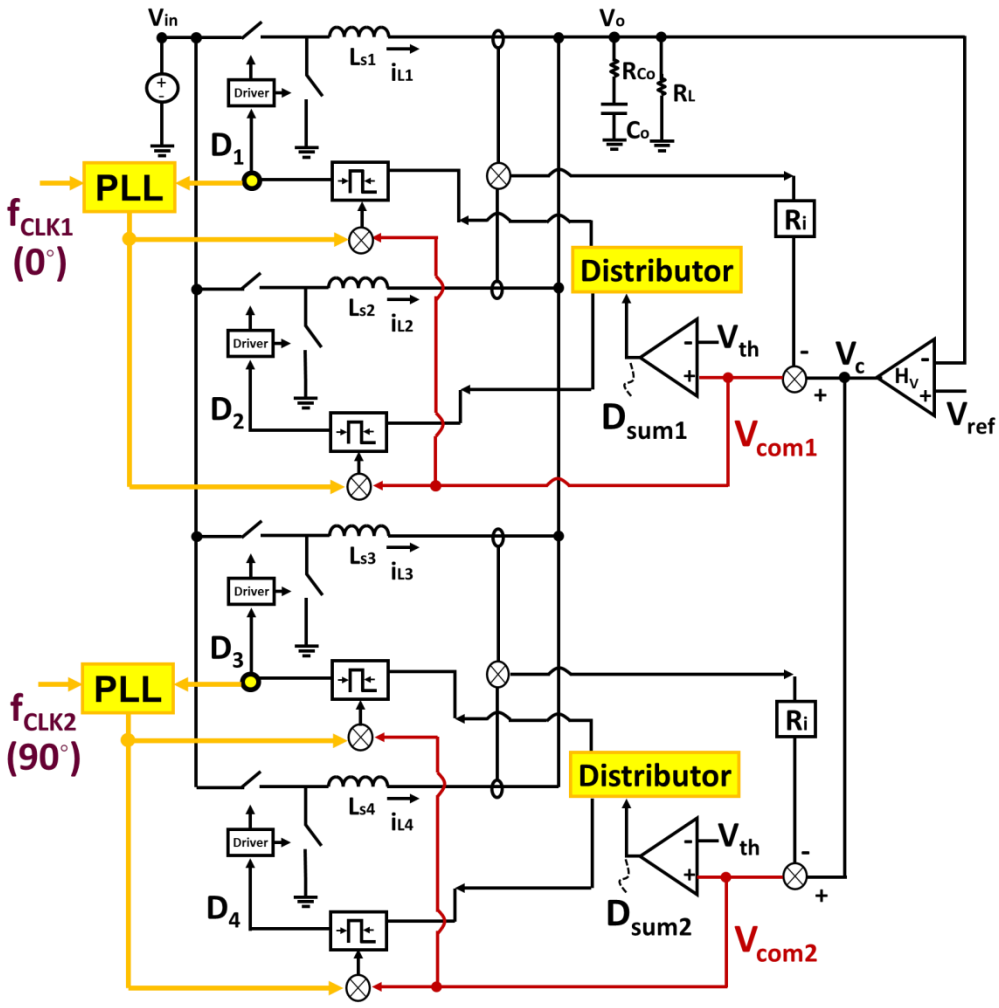


Figure 5.14 Hybrid interleaving structure of RPM control for wide D range

Furthermore, Figure 5.16 demonstrates that the hybrid interleaving takes the advantage of the RPM control with on-time extension to enlarge the overlapping region among phases naturally. When V_{com1} and V_{com2} rise during a step-up load transient, S_r of each phase takes longer time to intersect with, so the on-time can be extended automatically. The incremental changes of both on-time width and overlapping area dependent to the magnitude of load transient event, so the ring-back issue can be avoided.

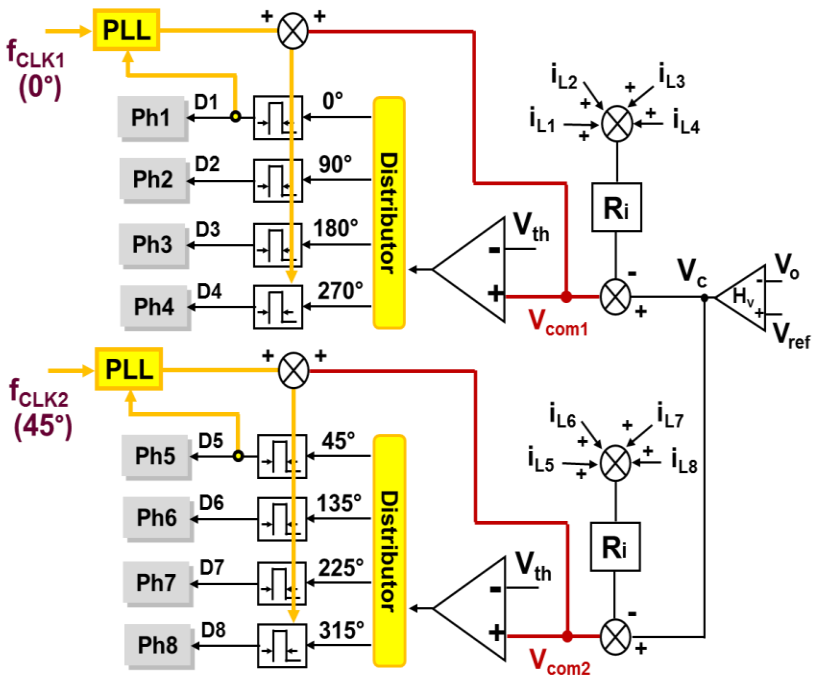


Figure 5.15 Hybrid interleaving structure of RPM control for narrow D range

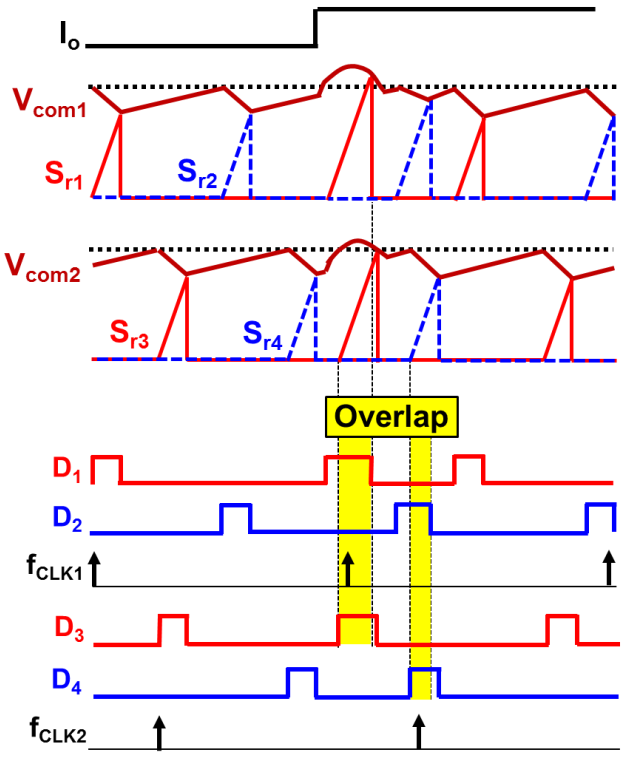


Figure 5.16 Step-up load transient of hybrid interleaving structure using RPM control

5.3 Verification

The goal is to demonstrate the proposed control scheme is capable of achieving both a higher BW design and a faster transient response to minimize output capacitors. Based on the output filter model in Chapter 1, when the target T_2 BW is designed close to 200kHz ($f_{sw}/4$), it is possible to save more output capacitors, including not only all bulk capacitors but also some of the decoupling capacitors outside of the CPU socket.

A. SIMPLIS simulation using proposed COT control

The proposed control scheme is verified on the design example of a four-phase buck converter: V_{in}=5.2~8.4V, V_o=0.5~2V, L_s=150nH (-35%~20%), f_{CLK}=800kHz, and R_{LL}=1.5mΩ. The proposed COT control with hybrid interleaving is built on SIMPLIS simulation, and the filter only contains a decoupling capacitor bank outside of a CPU socket with 8·22μF and a cavity capacitor bank with 18·22μF, as shown in Figure 5.17.

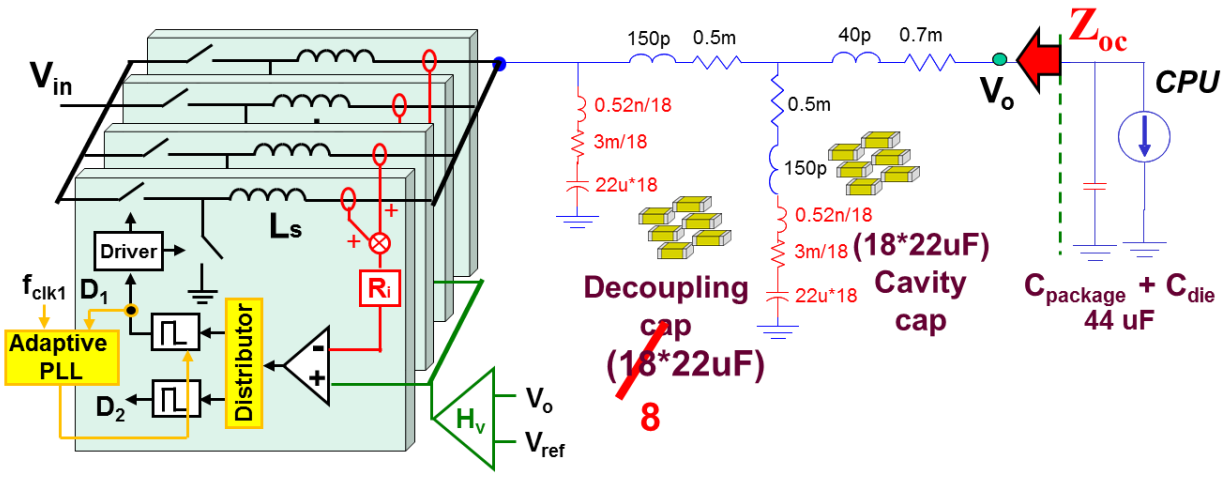
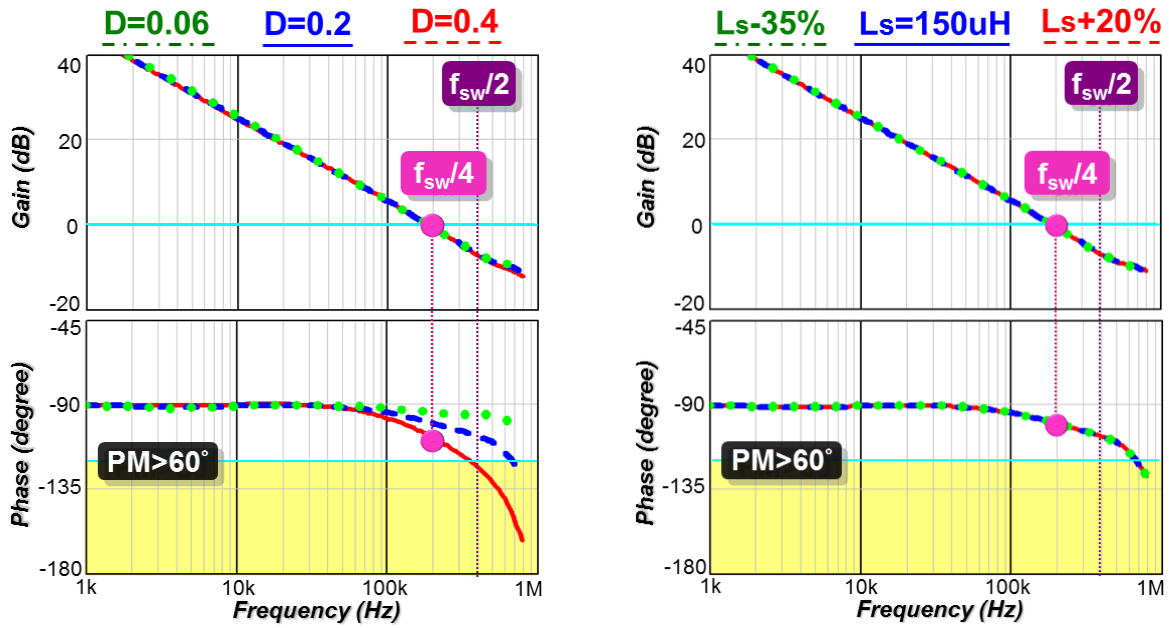


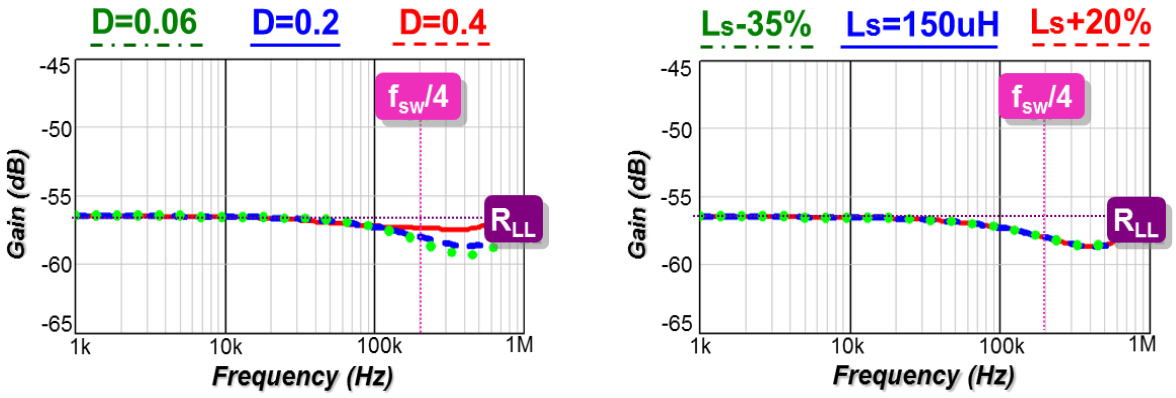
Figure 5.17 The simulation diagram for proposed four-phase COT control.

Firstly, since the hybrid interleaving structure does not need additional external ramp compensation, it preserves sufficient PM at $f_{sw}/4$ under the interested D range and worst L_s variation, as shown in Figure 5.18. Therefore, the simulation results in Figure 5.19 indicate no output-impedance peaking is observed, considering those parameter changes. Next, the transient response is simulated under V_{in}=8.4V, V_o=1.8V, L_s=150nH, and a step load change between 1A and 66A with a slew rate of 100A/μS. Figure 5.20(a) highlights that the natural overlapping feature minimizes V_o undershoot for the step-up load transient. Figure 5.20(b) points out that the COT control cannot truncate the gates signals and results in the V_o overshoot of 35mV. It is within the VR12.5 Specification of 50mV, but the design margin is only 15mV.



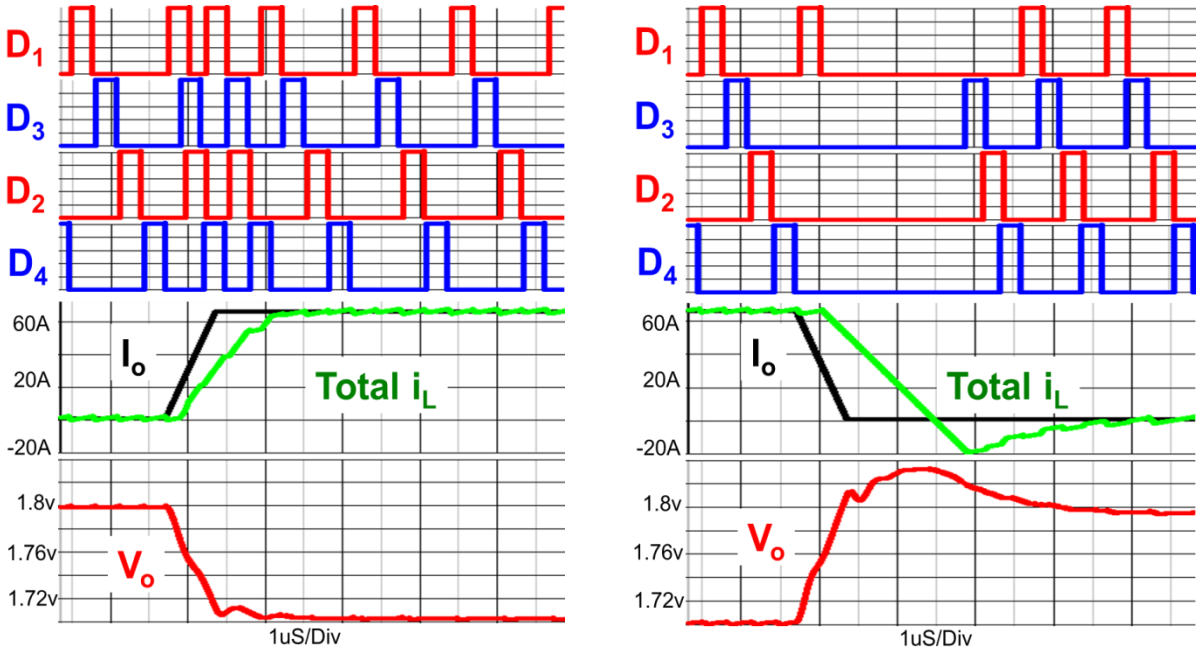
(a) (b)

Figure 5.18 T_2 simulation of proposed COT control: (a) D change, and (b) L_s variation



(a) (b)

Figure 5.19 Z_{oc} simulations of proposed COT control to: (a) D change, and (b) L_s variation



(a) (b)

Figure 5.20 Transient simulations of proposed COT control to: (a) load step-up, and (b) load step-down

B. SIMPLIS simulation using proposed RPM control

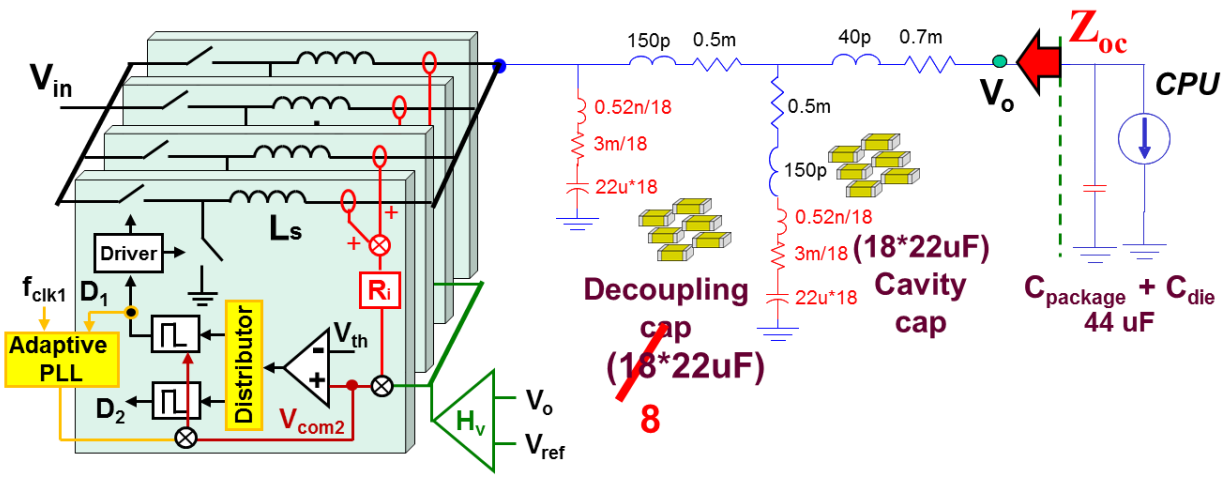
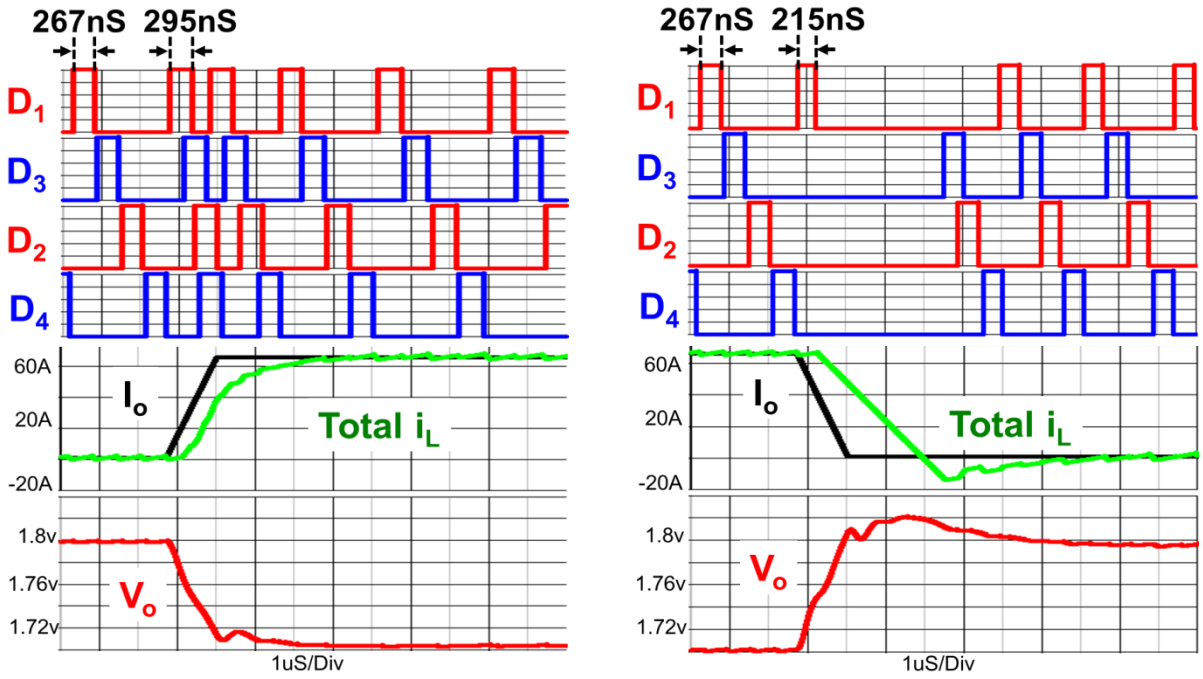


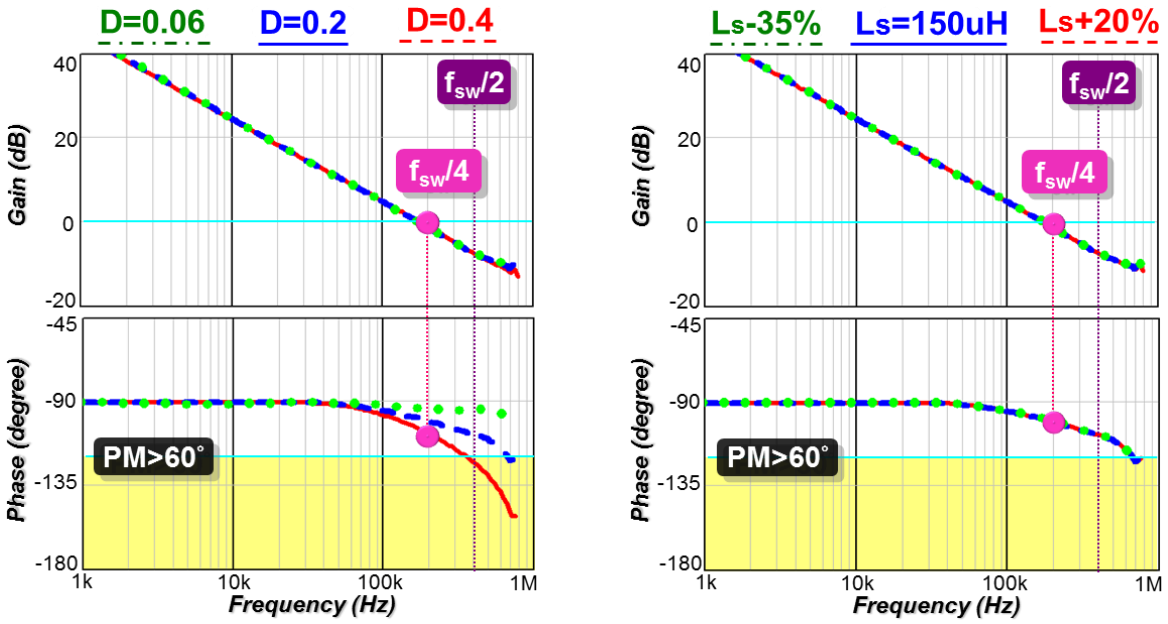
Figure 5.21 The simulation diagram for proposed four-phase RPM control

The simulation on the proposed RPM control with hybrid interleaving is then performed to show further improvement on the transient response. With the same number of output capacitors, the simulation setup of the proposed RPM control is shown in Figure 5.21. Figure 5.22(a) highlights the benefit of natural on-time extension and natural overlapping feature enables a faster step-up load transient response. Moreover, Figure 5.22(b) indicates that the ability of on-time truncation reduces V_o overshoot from 35mV to 20mV, so a 30mV design margin is available for 50mV Spec. Furthermore, with a similar small-signal property as the COT control, a proposed RPM control is also capable of providing sufficient PM at $f_{sw}/4$ under the interested D range and worst L_s variation, as shown in Figure 5.23. Therefore, constant output impedance is achieved with all ceramic output capacitors, as shown in Figure 5.24.



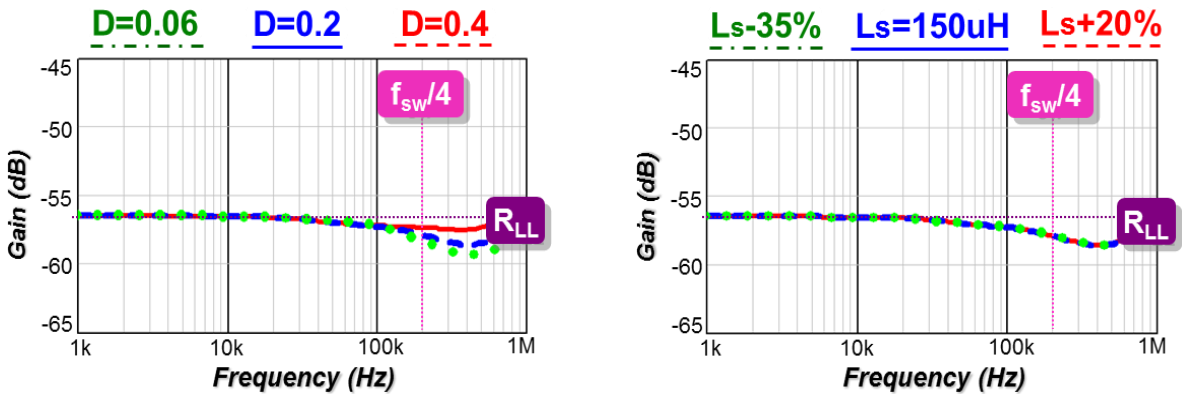
(a) (b)

Figure 5.22 Transient simulations of proposed RPM control to: (a) load step-up, and (b) load step-down



(a) (b)

Figure 5.23 T_2 simulation of proposed RPM control: (a) D change, and (b) L_s variation



(a) (b)

Figure 5.24 Z_{oc} simulations of proposed RPM control to: (a) D change, and (b) L_s variation

C. Experimental verification

A mixed-signal experimental hardware is built to provide an advance evaluation platform for a high-frequency and high-bandwidth multiphase VR, as shown in Figure 5.25. The power-board layout is built based on the stack-up of a laptop motherboard. A four-phase VR is mounted on it to power a laptop CPU using a rPGA947 socket. The VR utilizes the latest DrMOS from On-semiconductor, NCP5368, to perform higher switching frequency up to 5MHz. The output capacitor bank on the power board consists of 18 decoupling capacitors outside of a CPU socket (22µF X5R ceramic capacitor in 0805 size), and 18 cavity capacitors (22µF X5R ceramic capacitor in 0805 size). Next to the power board, a mixed-signal control board is connected to the power board with a socket, which contains an analog control card to implement proposed high-BW control scheme, and an optional digital FPGA control card to support auto-tuning algorithm.

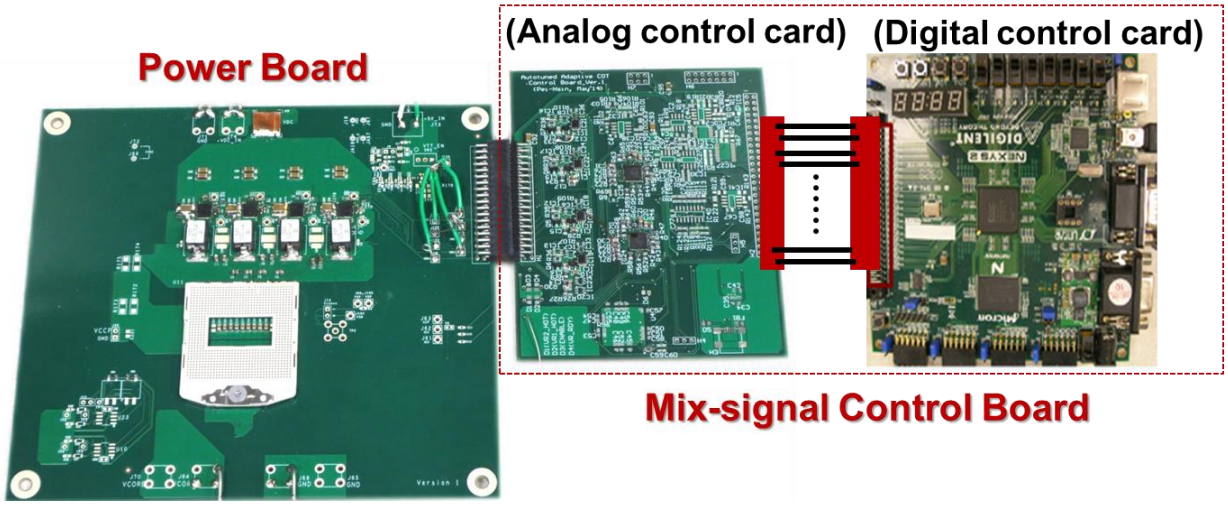


Figure 5.25 The mixed-signal experimental platform for a multiphase VR in MHz switching

On the analog control card, the proposed COT control with hybrid interleaving is constructed with two constant on-time controllers using a pulse distribution structure, TPS59650 from Texas instrument, as well as an adaptive PLL loop. TLC2932 is used as the phase frequency detector of the PLL loops. The low-pass filter of the PLL loops contains an original pole, a zero at 2kHz, a pole at 40kHz, and another pole at 100kHz. The adaptive control of the PLL loops is based on a piecewise linear ramp method to anchor the PLL BW at 9kHz, as mentioned in Chapter 4.

Figure 5.26 shows the test setup for time-domain and frequency-domain measurements. Mounted on the rPGA947 socket of the power board, a CPU emulator (Gen 4 VTT tool from Intel) generates a high di/dt load transient event. The V_o waveform is measured with a specified differential probe on the test point of the emulator. Firstly, the test data in Figure 5.27 is to demonstrate the steady-state gates signals and output voltage ripple at a ripple cancellation point. The test condition is V_{in}=6V, V_o=1.5V, L_s=100nH, f_{CLK}=1MHz, I_o=1A, and R_{LL}=1.5mΩ. The measurement result reveals that the proposed method performs at a correct interleaving angle and

has a stable gate signals at D≈0.25, which is the ripple cancelation point in a four-phase operation. Therefore, the functional interleaving maintains the low output ripple of 15mV, which is within the tolerance band of VR12.5 specification.

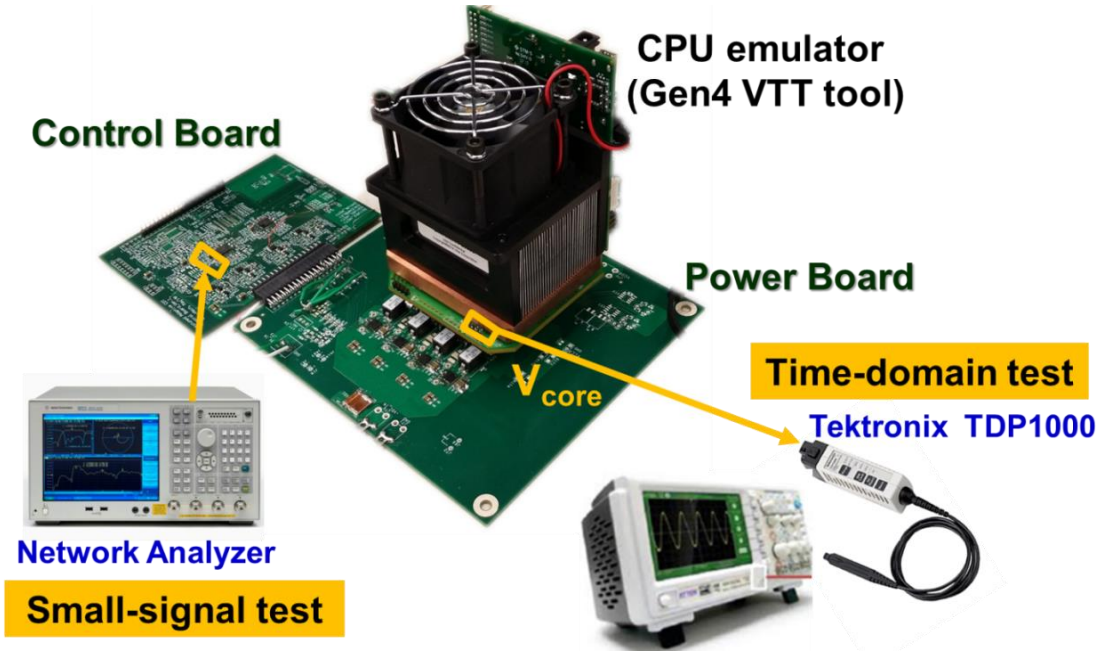
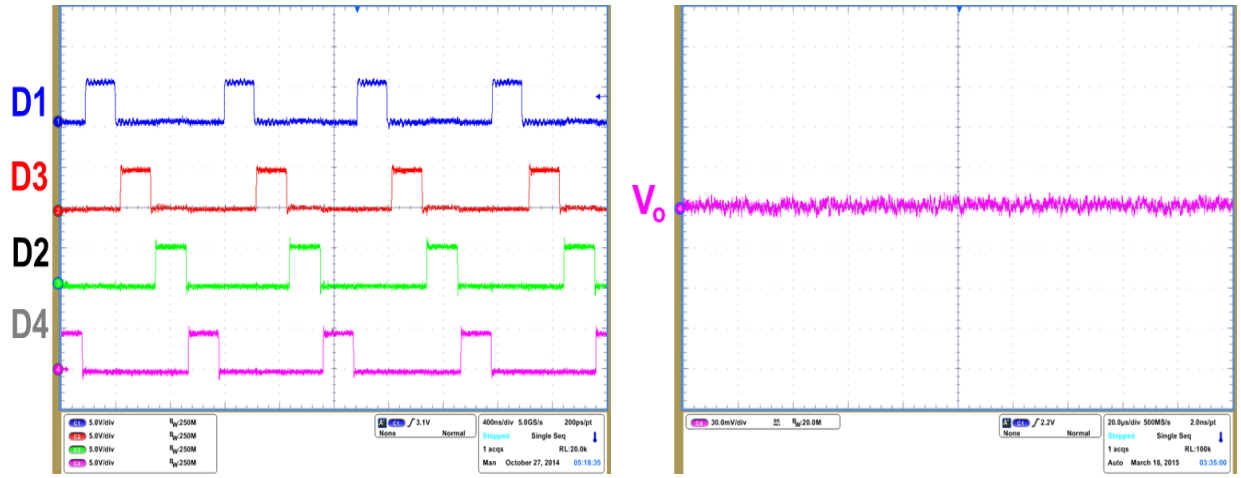
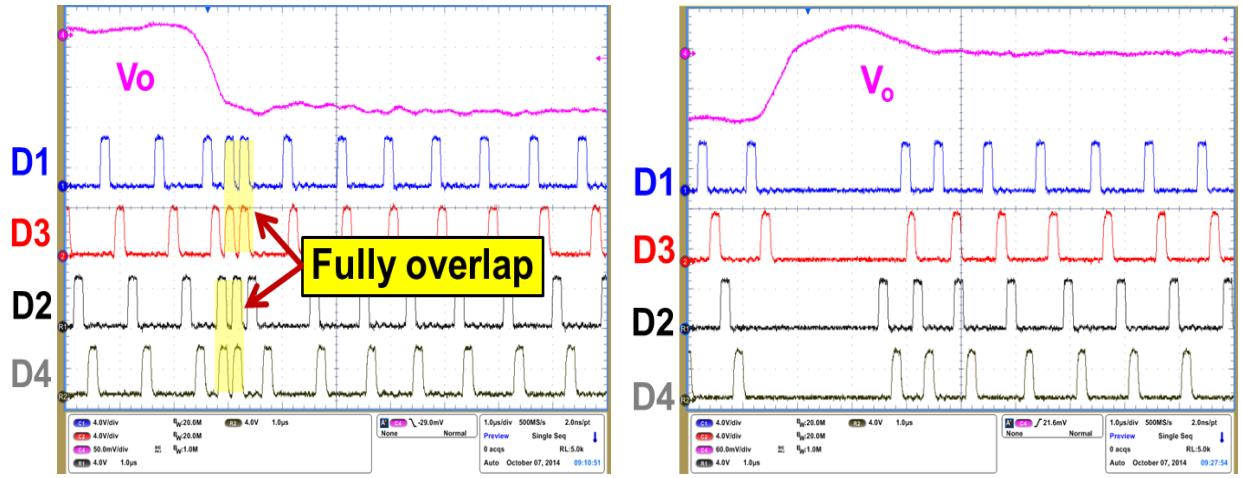


Figure 5.26 Test setup



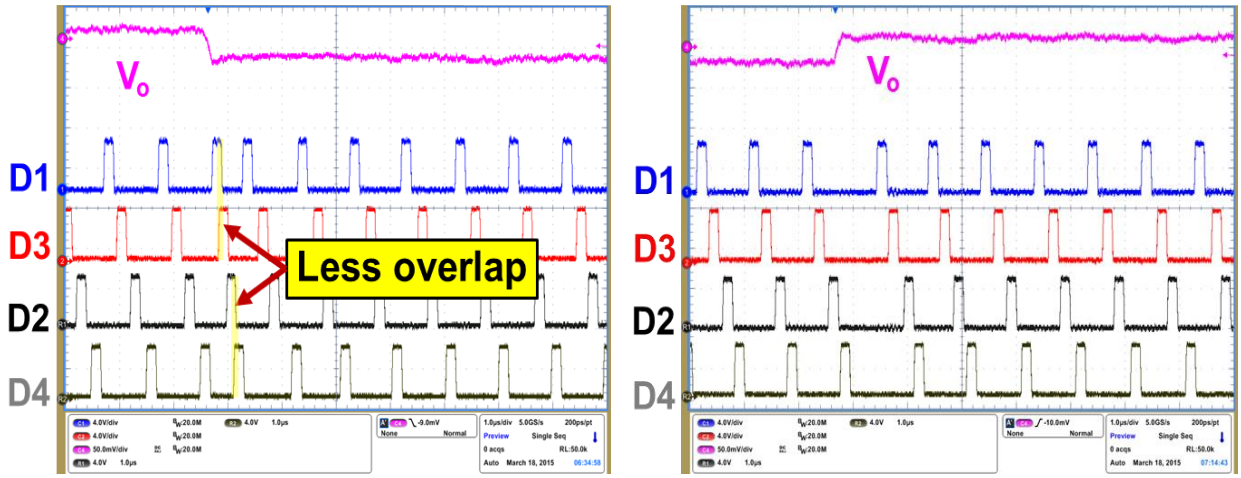
(a) (b)

Figure 5.27 Steady-state measurement results on: (a) gate signals, and (b) V_o ripple



(a) (b)

Figure 5.28 Transient measurement results to: (a) heavy step-up load, and (b) heavy step-down load

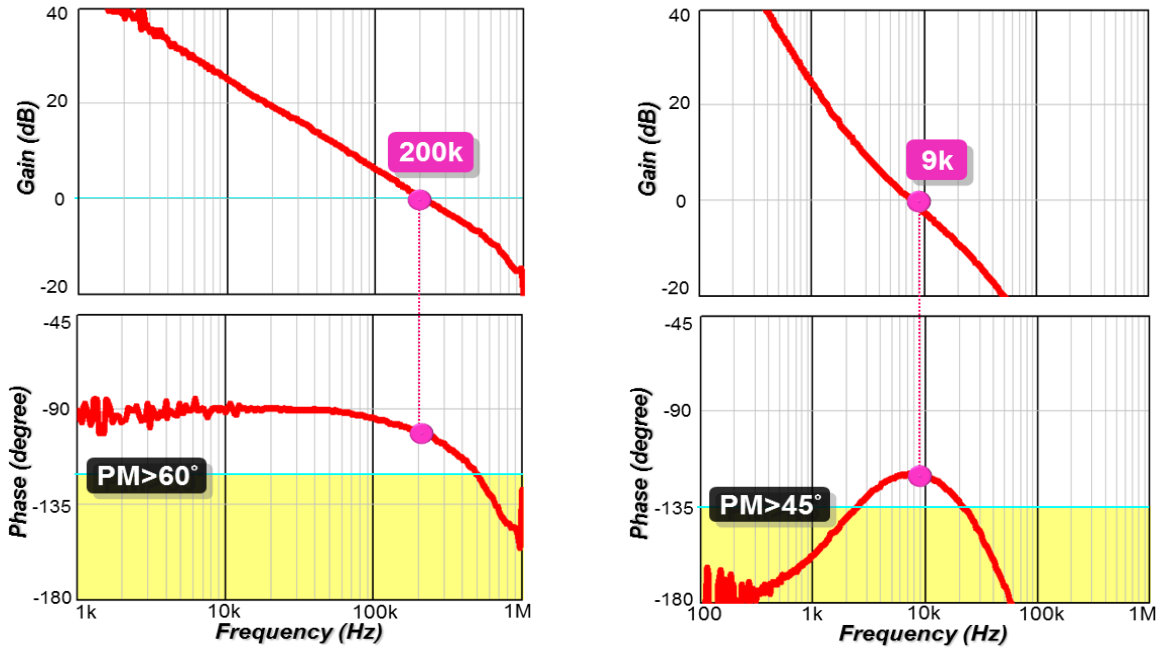


(a) (b)

Figure 5.29 Transient measurement results to: (a) light step-up load, and (b) light step-down load

Next, the test data in Figure 5.28 displays the transient performance. The test condition is V_{in}=8.4V, V_o=1.5V, L_s=100nH, f_{CLK}=1MHz, R_{LL}=1.5mΩ, and the step load change between 1A and 66A with a slew rate of 100A/uS. Figure 5.28(a) indicates the gates signals are overlapped automatically during a step-up load transient, so no V_o undershoot is observed. Figure 5.28(b)

indicates the V_o overshoot is 36mV which is within the 50mV Spec. It is possible to reduce overshoot by using proposed RPM control. After that, a lighter step-load transient condition between 1A and 21A is tested to prove the overlapping feature can be adaptive to different load conditions. Figure 5.29(a) indicates the overlapping area shrinks naturally for a smaller step-up load, so there is no ringing-back phenomenon on V_o waveform.



(a) (b)

Figure 5.30 Small-signal measurements on: (a) T_2, and (b) T_p

Moreover, the small-signal property is measured. Figure 5.30(a) shows that proposed interleaving preserves sufficient PM for T_2 BW design at 200kHz, and it is possible to push higher for a more aggressive design. Figure 5.30(b) shows that the proposed adaptive PLL loop in the hybrid interleaving ensures the stability margin for a T_p BW design at 9kHz.

5.4 Summary

This chapter aims to simplify the implementation of the proposed interleaving with adaptive PLL loops for a multiphase VR. The adaptive PLL structure mentioned in Chapter 4 enables a high-BW design, and a fast transient response, however the tradeoff comes with the circuit complexity of the multiple adaptive PLL loops. In the beginning, an alternative interleaving method that does not use PLL is reviewed, and the limitations in multiphase are analyzed. Then, a novel hybrid interleaving structure is proposed, whose property combines with the pulse distribution structure and adaptive PLL structure to solve the issues. After that, a SIMPLIS simulation is performed based on the state-of-the-art output filter model. Finally, an advance experimental platform is built to evaluate the performance for the cutting-edge MHz VR with minimum output capacitors.

Chapter 6. Conclusion

6.1 Summary

The current-mode control architecture has been an indispensable technique to fulfill the AVP requirement for multiphase VRs to power microprocessors. In the future, more critical transient requirements of multi-core microprocessors and higher power-density demands of VRs will impose a new challenge on the multiphase VR with higher BW design and a minimum number of output capacitors. However, when the system BW approaches half of switching frequency, the stability margin becomes very sensitive to operating conditions and component tolerance, because of the nonlinearity of the direct inductor current feedback. The current-sensing accuracy, modulation schemes, and interleaving approaches play important roles in maintaining a sufficient stability margin.

The inductor DCR current sensing technique is simple and widely used, but its poor accuracy in the time-constant mismatch can cause BW limitations and overdesign of output capacitors. Moreover, the stability margin of the current-mode control using constant-frequency modulation is sensitive to both operating conditions and component tolerance, so a high-BW design is challenging. Furthermore, the stability margin with variable-frequency modulation can also be affected by parameter variations, when a pulse-distribution approach is used for interleaving. Those BW limitations become technology barriers of minimizing the output capacitors. In addition, the switching-frequency variation of the variable-frequency control not

only influences the system efficiency, but also introduces a beat-frequency input ripple which may result in larger input filter size.

Chapter 2 focuses on improving the current-sensing accuracy using inductor DCR current sensing. At the beginning, an equivalent circuit model for generic current-mode controls using DCR current sensing is developed to analyze the impacts of component tolerance in high-BW design. Next, the state-of-the-art auto-tuning method that improves the current sensing accuracy is reviewed, and its deficiency in a multiphase VR is identified. After that, enlightened by the proposed model, a novel auto-tuning method is proposed, which features better tuning performance, noise-free operation, and simpler implementation than the state-of-the-art method.

Chapter 3 explores a new solution to overcome the BW limitation of constant-frequency control. First, the current state-of-the-art adaptive control is reviewed, and the analysis shows that its BW limitation comes from the inability to minimize the quality factor change of the $f_{sw}/2$ double pole. Therefore, adaptive external-ramp compensation is proposed to maintain the highest stability margin for high-BW design by controlling the quality factor to be constant. The design guidelines and multiphase configurations of the adaptive control scheme are discussed in detail. Also, an extension technique to various kinds of constant-frequency controls is presented.

Chapter 4 covers the modeling and design of the proposed adaptive PLL loop for multiphase variable-frequency control. It is found that interleaving with the adaptive PLL loop enables the variable-frequency control to push the BW of output voltage feedback loop higher, speed up the load transient response, maintain constant steady-state switching frequency, and avoid the beat-frequency ripple. A generic small-signal model of the PLL loop is derived to investigate the

stability issue caused by the parameter variations. Then, inspired by the proposed model, a simple adaptive control is developed to allow the BW of the PLL loop to be anchored at the highest phase margin. The adaptive PLL structure is applicable to different types of variable-frequency control, including COT control and RPM control.

Chapter 5 introduces a hybrid interleaving structure to simplify the implementation of multiphase VRs using the proposed adaptive PLL loop for applications with more phases. At the beginning, an alternative interleaving approach without PLL loops, called the pulse distribution structure, is reviewed, and the design trade-offs among the system BW, transient response, and beat-frequency ripple are explained. Then, a novel interleaving strategy is proposed which simplifies the circuitry of multiphase VR controllers without compromising the system performance by combining the adaptive PLLs with the pulse distribution structure.

As a conclusion, based on the proposed analytical models, effective control concepts, systematic optimization strategies, viable implementations are fully investigated for high-BW current-mode control using different modulation techniques. Moreover, all the modeling results and the system performance are verified through simulation with a practical output filter model and an advanced mixed-signal experimental platform based on the latest MHz VR design on the laptop motherboard. In consequence, the multiphase VRs in future computation systems can be scalable easier with proposed multiphase configurations, increase the system reliability with proposed adaptive loop compensation, and minimize the total system footprint of the VR with the superior transient performance.

6.2 Future Work

The simulation comparison indicates the similarity of the small-signal property between COT control and RPM control. It could be interesting to derive the small-signal model of the RPM control based on describing function method, such that more rigorous understanding may be obtained. Also, the mathematical model of RPM control could be turn into an equivalent circuit model, so the circuit representation could provide more physical and simple interpretations on the dynamic of the current-loop with RPM control.

Appendix A. Describing Function Derivation

The appendix provides the detail derivation for the describing function used in the PLL loop implementations of COT and RPM controls.

A.1 Derivation for the PLL Loop of Constant On-Time Control

(A) The PLL Implementation which Adjusts V_{th} to Control T_{on}

The following derivation is to model the small-signal property of the PLL-loop implementation in Figure 4.9. As shown in Figure A.1, a sinusoidal perturbation with a small magnitude at the frequency f_m is injected through the on-time control signal v_{on}, when the LPF is disconnected. Then, based on the perturbed i_{PFD} waveform, the describing function from the on-time control signal v_{on} to the PLL output signal i_{PFD} can be found by mathematical derivation.

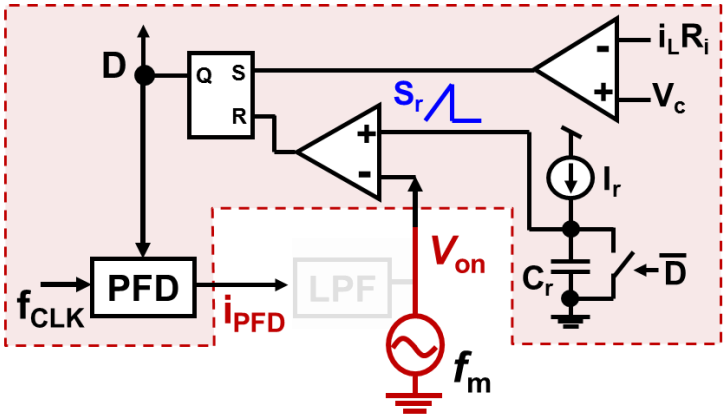


Figure A.1 Modeling for the first PLL-loop implementation of COT control

The T_{off} and T_{on} are modulated by the perturbation signal: $v_{on}(t)=V_{th}+\hat{r}\sin(2\pi f_m \cdot t+\theta)$, where V_{th} is the steady state value, $\hat{r}$ is the perturbation magnitude, and θ is the initial angle. Based on the modulation law, it is found that:

$$v_c + s_n T_{on(i-1)} = v_c + s_f [t_{d(i)} + (T_{CLK} - t_{d(i-1)} - T_{on(i-1)})] \tag{A.1}$$

$$T_{on(i-1)} = v_{on}(t_{i-1} + t_{d(i-1)} + T_{on(i-1)}) / s_r \tag{A.2}$$

where $t_d(i)$ is the i^{th} cycle of i_{PFD} on-time, $T_{on}(i)$ is the i^{th} cycle of on-time of the D signal, $S_n=R_i(V_{in}-V_o)/L_s$, $S_f=R_iV_o/L_s$, L_s is the inductance of the output inductor, and R_i is the current feedback gain. t_i can be calculated as: $t_i=(i-1)T_{CLK}$.

By substituting (A.2) into (A.1), it is found that:

$$\begin{aligned} t_{d(i)} - t_{d(i-1)} &= \frac{s_n + s_f}{s_f} \frac{v_{on}(t_{i-1} + t_{d(i-1)} + T_{on(i-1)})}{s_r} - T_{CLK} \\ &= \frac{V_{in}}{V_o} \frac{v_{on}(t_{i-1} + t_{d(i-1)} + T_{on(i-1)})}{s_r} - T_{CLK} \\ &= \frac{1}{D} \frac{\hat{r}\sin[2\pi f_m \cdot (t_{i-1} + t_{d(i-1)} + T_{on(i-1)}) + \theta]}{s_r} + (\frac{1}{D}\frac{V_{th}}{s_r} - T_{CLK}) \end{aligned} \tag{A.3}$$

Since V_{th}/S_r is equal to steady-state T_{on}, (A.3) can be written into:

$$\begin{aligned} t_{d(i)} - t_{d(i-1)} &= \frac{1}{D} \frac{\hat{r}\sin[2\pi f_m \cdot (t_{i-1} + t_{d(i-1)} + T_{on(i-1)}) + \theta]}{s_r} \\ &\approx \frac{1}{D} \frac{\hat{r}\sin[2\pi f_m \cdot (t_{i-1} + T_{on}) + \theta]}{s_r} \end{aligned} \tag{A.4}$$

Next, the perturbed inductor current $i_{PFD}(t)$ can be expressed by:

$$i_{PFD}(t)\Big|_{0\le t\le t_M+T_{CLK}} = -I_d \cdot \sum_{i=1}^{M}[u(t-t_i)-u(t-t_i-t_{d(i)})] \tag{A.5}$$

where u(t)=1 when t>0, and I_d is the magnitude of $i_{PFD}(t)$.

Then, Fourier analysis can be performed on the $i_{PFD}(t)$ as:

$$\begin{aligned}
c_m &= j\frac{2f_m}{N}\int_0^{t_M+T_{CLK}} i_{PFD}(t)\cdot e^{-j2\pi f_m t}dt \\
&= \frac{j2\pi f_m}{N\pi}(-\mathrm{I}_d)\sum_{i=1}^{M}\int_{t_i}^{t_i+t_{d(i)}} e^{-j2\pi f_m t}dt \\
&= -\frac{1}{N\pi}(-\mathrm{I}_d)\sum_{i=1}^{M}(e^{-j2\pi f_m(t_i+t_{\mathrm{d}(i)})}-e^{-j2\pi f_m(t_i)}) \\
&= \frac{1}{N\pi}(-\mathrm{I}_d)\cdot\sum_{i=1}^{M}[e^{-j2\pi f_m(t_i)}(1-e^{-j2\pi f_m t_{d(i)}})] \\
&\approx \frac{1}{N\pi}(-\mathrm{I}_d)\cdot\sum_{i=1}^{M}[e^{-j2\pi f_m(t_i)}(1-1+j2\pi f_m t_{\mathrm{d}(i)})] \\
&\approx \frac{j2\pi f_m}{N\pi}(-\mathrm{I}_d)\cdot\sum_{i=1}^{M}[e^{-j2\pi f_m(t_i)}t_{\mathrm{d}(i)}]
\end{aligned} \tag{A.6}$$

where c_m is the Fourier coefficient of $i_{PFD}(t)$ at the perturbation frequency f_m.

Based on (A.4) and (A.6), it is found that:

$$
\begin{aligned}
c_m - c_m e^{-j2\pi f_m T_{CLK}} &= \frac{-\mathrm{I}_d}{s_r D}\frac{j2f_m}{N}\sum_{i=1}^{M}\{e^{-j2\pi f_m(t_i)}\hat{r}\sin[2\pi f_m\cdot(\mathrm{t}_{i-1}+T_{on})+\theta]\} \\
&= \frac{-\mathrm{I}_d\,\hat{r}}{s_r D(\mathrm{j}2)}\frac{j2f_m}{N}\sum_{i=1}^{M}\{e^{-j2\pi f_m(t_i)}[e^{j[2\pi f_m\cdot(\mathrm{t}_{i-1}+T_{on})+\theta]}-e^{-j[2\pi f_m\cdot(\mathrm{t}_{i-1}+T_{on})+\theta]}]\} \\
&= \frac{-\mathrm{I}_d}{s_r D}\frac{f_m}{N}\hat{r}\{\sum_{i=1}^{M}e^{j2\pi f_m\cdot(\mathrm{t}_{i-1}+T_{on}-\mathrm{t}_i)}e^{j\theta}-\sum_{i=1}^{M}e^{-j2\pi f_m\cdot(\mathrm{t}_{i-1}+T_{on}+\mathrm{t}_i)}e^{-j\theta}\} \\
&= \frac{-\mathrm{I}_d}{s_r D}\frac{f_m}{N}\hat{r}\{\sum_{i=1}^{M}e^{-j2\pi f_m\cdot(T_{CLK}-T_{on})}e^{j\theta}-\sum_{i=1}^{M}e^{-j2\pi f_m\cdot[(2\mathrm{i}-3)T_{CLK}+T_{on}]}e^{-j\theta}\} \\
&= \frac{-\mathrm{I}_d}{s_r D}\frac{f_m}{N}\hat{r}\{Me^{-j[2\pi f_m\cdot(1-D)\mathrm{T}_{CLK}]}e^{j\theta}-0\} \\
&= \frac{-\mathrm{I}_d}{s_r D}(\frac{Mf_m}{N})(\hat{r}e^{j\theta})e^{-j[2\pi f_m\cdot(1-D)\mathrm{T}_{CLK}]}
\end{aligned}
\tag{A.7}
$$

So, c_m can be found out as:

$$
c_m = \frac{-I_d}{s_r D T_{CLK}}\frac{e^{-j2\pi f_m(1-\mathrm{D})T_{CLK}}}{(1-e^{-j2\pi f_m T_{CLK}})}(\hat{r}\,e^{j\theta}) \tag{A.8}
$$

Since the Fourier coefficient of v_{on} is $\hat{r}e^{j\theta}$, the describing function of v_{on}-to-i_{PFD} transfer function in the s-domain can be calculated as:

$$
\frac{i_{PFD}(\mathrm{s})}{v_{on}(\mathrm{s})} = \frac{-I_d}{s_r D T_{CLK}}\frac{e^{-s(1-D)\mathrm{T}_{CLK}}}{1-e^{-s\mathrm{T}_{CLK}}} \tag{A.9}
$$

(B) The PLL Implementation which Adjusts S_r to Control T_{on}

Similar methodology is used to model the small-signal property of the PLL-loop implementation in Figure 4.11. As shown in Figure A.2, a sinusoidal perturbation, $v_{on}(t)=0+\hat{r}\sin(2\pi f_m \cdot t+\theta)$, is injected through the on-time control signal v_{on}, when the LPF is disconnected.

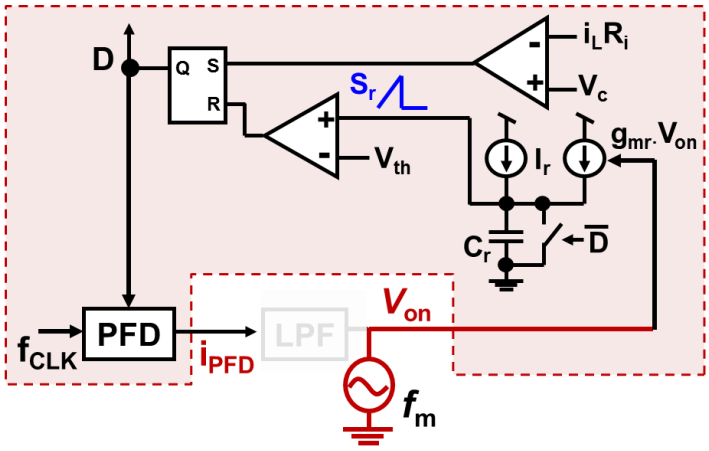


Figure A.2 Modeling for the second PLL-loop implementation of COT control

Based on the modulation law, it is found that:

$$v_c + s_n T_{on(i-1)} = v_c + s_f (T_{CLK} - t_{d(i)} - T_{on(i-1)} + t_{d(i-1)}) \tag{A.10}$$

$$s_r(t_{i-1} + T_{on(i-1)} - t_{d(i-1)}) = \frac{I_r + g_{mr} \cdot v_{on}(t_{i-1} + T_{on(i-1)} - t_{d(i-1)})}{C_r} \tag{A.11}$$

$$T_{on(i-1)} = V_{th} / s_r(t_{i-1} + T_{on(i-1)} - t_{d(i-1)}) \tag{A.12}$$

By substituting (A.12) and (A.11) into (A.10), it is found that:

$$\begin{aligned} t_{d(i)} - t_{d(\mathrm{i}-1)} &= \frac{s_n + s_f}{s_f} \frac{-V_{th} C_r}{I_r + g_{mr} \cdot v_{on}(\mathrm{t}_{i-1} + T_{on(\mathrm{i}-1)} - t_{d(i-1)})} + T_{CLK} \\ &= \frac{1}{D}\left[\frac{-V_{th} C_r}{I_r + g_{mr} \cdot v_{on}(\mathrm{t}_{i-1} + T_{on(\mathrm{i}-1)} - t_{d(i-1)})} + \frac{V_{th} C_r}{I_r}\right] \\ &= \frac{V_{th} C_r}{D}\left\{\frac{g_{mr} \cdot v_{on}(\mathrm{t}_{i-1} + T_{on(\mathrm{i}-1)} - t_{d(i-1)})}{\mathrm{I}_r[I_r + g_{mr} \cdot v_{on}(\mathrm{t}_{i-1} + T_{on(\mathrm{i}-1)} - t_{d(i-1)})]}\right\} \end{aligned} \tag{A.13}$$

Since $I_r >> g_{mr} \cdot \hat{r} \sin[2\pi f_m \cdot (\mathrm{t}_{i-1} + T_{on(\mathrm{i}-1)} - t_{d(i-1)}) + \theta]$, (A.13) can be simplified as

$$\begin{aligned} t_{d(i)} - t_{d(\mathrm{i}-1)} &\approx \frac{V_{th} C_r g_{mr} \cdot \hat{r} \sin[2\pi f_m \cdot (\mathrm{t}_{i-1} + T_{on(\mathrm{i}-1)} - t_{d(i-1)}) + \theta]}{{I_r}^2 D} \\ &\approx \frac{V_{th} C_r g_{mr}}{{I_r}^2 D} \hat{r} \sin[2\pi f_m \cdot (\mathrm{t}_{i-1} + T_{on}) + \theta] \end{aligned} \tag{A.14}$$

Next, the perturbed inductor current $i_{PFD}(t)$ can be expressed by:

$$i_{PFD}(t)\Big|_{0 \le t \le t_M + T_{CLK}} = -I_d \cdot \sum_{i=1}^{M} [u(t - t_i) - u(t - t_i - t_{d(i)})] \tag{A.15}$$

Then, same as to (A.6), Fourier analysis can be performed on the $i_{PFD}(t)$ as:

$$\begin{aligned} c_m &= j \frac{2 f_m}{N} \int_0^{t_M + T_{CLK}} i_{PFD}(t) \cdot e^{-j 2\pi f_m t} dt \\ &\approx \frac{j 2\pi f_m}{N\pi} (-\mathrm{I}_d) \cdot \sum_{i=1}^{M} [e^{-j 2\pi f_m (t_i)} t_{\mathrm{d}(i)}] \end{aligned} \tag{A.16}$$

where c_m is the Fourier coefficient of $i_{PFD}(t)$ at the perturbation frequency f_m.

Based on (A.14) and (A.16), it is found that:

$$\begin{aligned}
&c_m - c_m e^{-j2\pi f_m T_{CLK}} \\
&= \frac{-\mathrm{I}_d V_{th} C_r g_{mr}}{I_r{}^2 D} \frac{j2 f_m}{N} \sum_{i=1}^{M} \{e^{-j2\pi f_m (t_i)} \hat{r} \sin[2\pi f_m \cdot (\mathrm{t}_{i-1} + T_{on}) + \theta]\} \\
&= \frac{-\mathrm{I}_d V_{th} C_r g_{mr} \hat{r}}{I_r{}^2 D(\mathrm{j}2)} \frac{j2 f_m}{N} \sum_{i=1}^{M} \{e^{-j2\pi f_m (\mathrm{t}_i)} [e^{j[2\pi f_m \cdot (\mathrm{t}_{i-1} + T_{on}) + \theta]} - e^{-j[2\pi f_m \cdot (\mathrm{t}_{i-1} + T_{on}) + \theta]}]\} \\
&= \frac{-\mathrm{I}_d V_{th} C_r g_{mr}}{I_r{}^2 D} \frac{f_m}{N} \hat{r} \{\sum_{i=1}^{M} e^{j2\pi f_m \cdot (\mathrm{t}_{i-1} + T_{on} - \mathrm{t}_i)} e^{j\theta} - \sum_{i=1}^{M} e^{-j2\pi f_m \cdot (\mathrm{t}_{i-1} + T_{on} + \mathrm{t}_i)} e^{-j\theta}\} \\
&= \frac{-\mathrm{I}_d V_{th} C_r g_{mr}}{I_r{}^2 D} \frac{f_m}{N} \hat{r} \{\sum_{i=1}^{M} e^{-j2\pi f_m \cdot (T_{CLK} - T_{on})} e^{j\theta} - \sum_{i=1}^{M} e^{-j2\pi f_m \cdot [(2\mathrm{i}-3) T_{CLK} + T_{on}]} e^{-j\theta}\} \\
&= \frac{-\mathrm{I}_d V_{th} C_r g_{mr}}{I_r{}^2 D} \frac{f_m}{N} \hat{r} \{M e^{-j[2\pi f_m \cdot (1-D)\mathrm{T}_{CLK}]} e^{j\theta} - 0\} \\
&= \frac{-\mathrm{I}_d V_{th} C_r g_{mr}}{I_r{}^2 D} (\frac{M f_m}{N}) (\hat{r} e^{j\theta}) e^{-j[2\pi f_m \cdot (1-D)\mathrm{T}_{CLK}]}
\end{aligned} \tag{A.17}$$

Then, after Fourier analysis can be performed on $i_{PFD}(t)$, the coefficient is calculated as:

$$c_m = \frac{-I_d V_{th} C_r g_{mr}}{I_r{}^2 D T_{CLK}} \frac{e^{-j2\pi f_m (1-\mathrm{D}) T_{CLK}}}{(1 - e^{-j2\pi f_m T_{CLK}})} (\hat{r} e^{j\theta}) \tag{A.18}$$

Since the Fourier coefficient of v_{on} is $\hat{r}e^{j\theta}$, the describing function of v_{on}-to-i_{PFD} transfer function in the s-domain can be calculated as:

$$\frac{i_{PFD}(\mathrm{s})}{v_{on}(\mathrm{s})} = \frac{-I_d V_{th} C_r g_{mr}}{I_r{}^2 D T_{CLK}} \frac{e^{-s(1-D)\mathrm{T}_{CLK}}}{1 - e^{-s\mathrm{T}_{CLK}}} \tag{A.19}$$

A.2 Derivation for the PLL Loop of Ramp Pulse Modulation

(A) The PLL Implementation which sums with V_{com} to Control T_{on}

The following derivation is to model the small-signal property of the PLL-loop implementation in Figure 4.25. As shown in Figure A.3, a sinusoidal perturbation with a small magnitude at the frequency f_m is injected through the on-time control signal v_{on}, when the LPF is disconnected. Then, based on the perturbed i_{PFD} waveform, the describing function from the on-time control signal v_{on} to the PLL output signal i_{PFD} can be found by mathematical derivation.

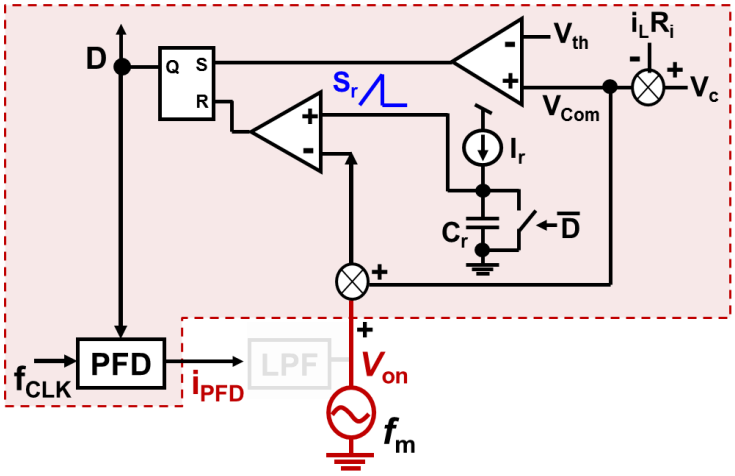


Figure A.3 Modeling for the first PLL-loop implementation of RPM control

The T_{off} and T_{on} are modulated by the perturbation signal: $v_{on}(t)=V_{th}+\hat{r}\sin(2\pi f_m \cdot t+\theta)$, where V_{th} is the steady state value, $\hat{r}$ is the perturbation magnitude, and θ is the initial angle. Based on the modulation law, it is found that:

$$V_{th}-[v_c - s_n T_{on(i-1)}] = V_{th} - \{v_c - s_f [t_{d(i)} + (T_{CLK} - t_{d(i-1)} - T_{on(i-1)})]\} \qquad (A.20)$$

$$T_{on(i-1)} = v_{on}(t_{i-1} + t_{d(i-1)} + T_{on(i-1)}) / (s_r + s_n) \qquad (A.21)$$

where $t_d(i)$ is the i^{th} cycle of i_{PFD} on-time, $T_{on}(i)$ is the i^{th} cycle of PWM on-time, $S_n=R_i(V_{in}-V_o)/L_s$, $S_f=R_iV_o/L_s$, L_s is the inductance of the output inductor, and R_i is the current feedback gain. t_i can be calculated as: $t_i=(i-1)T_{CLK}$.

By substituting (A.21) into (A.20), it is found that:

$$\begin{aligned} t_{d(i)} - t_{d(i-1)} &= \frac{s_n + s_f}{s_f} \frac{v_{on}(\mathrm{t}_{i-1} + t_{d(i-1)} + T_{on(\mathrm{i}-1)})}{s_r + s_n} - T_{CLK} \\ &= \frac{V_{in}}{V_o} \frac{v_{on}(\mathrm{t}_{i-1} + t_{d(i-1)} + T_{on(\mathrm{i}-1)})}{s_r + s_n} - T_{CLK} \\ &= \frac{1}{D} \frac{\hat{r}\sin[2\pi f_m \cdot (\mathrm{t}_{i-1} + t_{d(i-1)} + T_{on(\mathrm{i}-1)}) + \theta]}{s_r + s_n} + (\frac{1}{D} \frac{V_{th}}{s_r + s_n} - T_{CLK}) \end{aligned} \tag{A.22}$$

Since $V_{th}/(S_r+S_n)$ is equal to steady-state T_{on}, (A.22) can be written into:

$$\begin{aligned} t_{d(i)} - t_{d(i-1)} &= \frac{1}{D} \frac{\hat{r}\sin[2\pi f_m \cdot (\mathrm{t}_{i-1} + t_{d(i-1)} + T_{on(\mathrm{i}-1)}) + \theta]}{s_r + s_n} \\ &\approx \frac{1}{D} \frac{\hat{r}\sin[2\pi f_m \cdot (\mathrm{t}_{i-1} + T_{on}) + \theta]}{s_r + s_n} \end{aligned} \tag{A.23}$$

Next, the perturbed inductor current $i_{PFD}(t)$ can be expressed by:

$$i_{PFD}(t)\Big|_{0 \le t \le t_M + T_{CLK}} = -I_d \cdot \sum_{i=1}^{M} [u(t - t_i) - u(t - t_i - t_{d(i)})] \tag{A.24}$$

where u(t)=1 when t>0, and I_d is the magnitude of $i_{PFD}(t)$.

Then, same as to (A.6), Fourier analysis can be performed on the $i_{PFD}(t)$ as:

$$c_m = j\frac{2f_m}{N}\int_0^{t_M+T_{CLK}} i_{PFD}(t)\cdot e^{-j2\pi f_m t}dt$$
$$\approx \frac{j2\pi f_m}{N\pi}(-\mathrm{I}_d)\cdot\sum_{i=1}^{M}[e^{-j2\pi f_m(t_i)}t_{\mathrm{d}(i)}] \quad \text{(A.25)}$$

where c_m is the Fourier coefficient of $i_{PFD}(t)$ at the perturbation frequency f_m.

Based on (A.23) and (A.25), it is found that:

$$\begin{aligned}
&c_m - c_m e^{-j2\pi f_m T_{CLK}}\\
&= \frac{-\mathrm{I}_d}{(s_r+s_n)D}\frac{j2f_m}{N}\sum_{i=1}^{M}\{e^{-j2\pi f_m(t_i)}\hat{r}\sin[2\pi f_m\cdot(\mathrm{t}_{i-1}+T_{on})+\theta]\}\\
&= \frac{-\mathrm{I}_d\,\hat{r}}{(s_r+s_n)D(\mathrm{j}2)}\frac{j2f_m}{N}\sum_{i=1}^{M}\{e^{-j2\pi f_m(t_i)}[e^{j[2\pi f_m\cdot(\mathrm{t}_{i-1}+T_{on})+\theta]}-e^{-j[2\pi f_m\cdot(\mathrm{t}_{i-1}+T_{on})+\theta]}]\}\\
&= \frac{-\mathrm{I}_d}{(s_r+s_n)D}\frac{f_m}{N}\hat{r}\{\sum_{i=1}^{M}e^{j2\pi f_m\cdot(\mathrm{t}_{i-1}+T_{on}-\mathrm{t}_i)}e^{j\theta}-\sum_{i=1}^{M}e^{-j2\pi f_m\cdot(\mathrm{t}_{i-1}+T_{on}+\mathrm{t}_i)}e^{-j\theta}\}\\
&= \frac{-\mathrm{I}_d}{(s_r+s_n)D}\frac{f_m}{N}\hat{r}\{\sum_{i=1}^{M}e^{-j2\pi f_m\cdot(T_{CLK}-T_{on})}e^{j\theta}-\sum_{i=1}^{M}e^{-j2\pi f_m\cdot[(2\mathrm{i}-3)T_{CLK}+T_{on}]}e^{-j\theta}\}\\
&= \frac{-\mathrm{I}_d}{(s_r+s_n)D}\frac{f_m}{N}\hat{r}\{Me^{-j[2\pi f_m\cdot(1-D)\mathrm{T}_{CLK}]}e^{j\theta}-0\}\\
&= \frac{-\mathrm{I}_d}{(s_r+s_n)D}(\frac{Mf_m}{N})(\hat{r}e^{j\theta})e^{-j[2\pi f_m\cdot(1-D)\mathrm{T}_{CLK}]}
\end{aligned} \quad \text{(A.26)}$$

So, c_m can be found out as:

$$c_m = \frac{-I_d}{(s_r+s_n)DT_{CLK}}\frac{e^{-j2\pi f_m(1-\mathrm{D})T_{CLK}}}{(1-e^{-j2\pi f_m T_{CLK}})}(\hat{r}\,e^{j\theta}) \quad \text{(A.27)}$$

Since the Fourier coefficient of v_{on} is $\hat{r}e^{j\theta}$, the describing function of v_{on}-to-i_{PFD} transfer function in the s-domain can be calculated as:

$$\frac{i_{PFD}(s)}{v_{on}(s)} = \frac{-I_d}{(s_r + s_n)DT_{CLK}} \frac{e^{-s(1-D)T_{CLK}}}{1-e^{-sT_{CLK}}} \tag{A.28}$$

(B) The PLL Implementation which Adjusts S_r to Control T_{on}

To model the small-signal property of the PLL-loop implementation in Figure 4.26, a sinusoidal perturbation, $v_{on}(t)=0+\hat{r}\sin(2\pi f_m \cdot t+\theta)$, is injected through the on-time control signal v_{on}, as shown in Figure A.4.

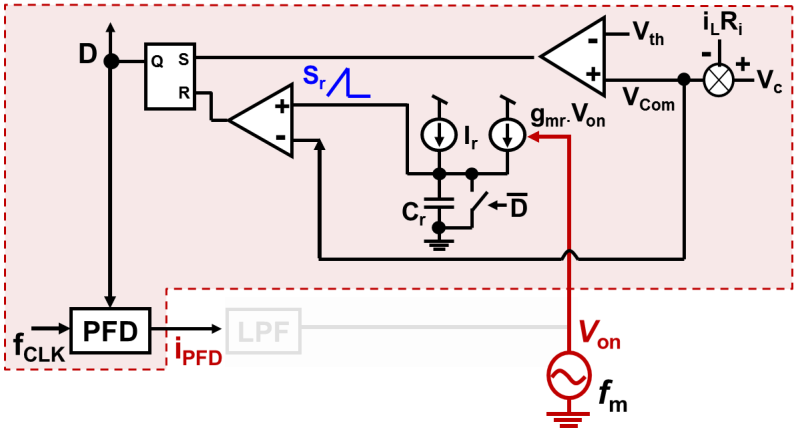


Figure A.4 Modeling for the second PLL-loop implementation of RPM control

Based on the modulation law, it is found that:

$$V_{th} - [v_c - s_n T_{on(i-1)}] = V_{th} - \{v_c - s_f [t_{d(i)} + (T_{CLK} - t_{d(i-1)} - T_{on(i-1)})]\} \tag{A.29}$$

$$s_r(t_{i-1} + T_{on(i-1)} - t_{d(i-1)}) = \frac{I_r + g_{mr} \cdot v_{on}(t_{i-1} + T_{on(i-1)} - t_{d(i-1)})}{C_r} \tag{A.30}$$

$$T_{on(\mathrm{i}-1)} = V_{th} / [s_r(\mathrm{t}_{i-1} + T_{on(\mathrm{i}-1)} - t_{d(i-1)}) + \mathrm{s}_n] \tag{A.31}$$

By substituting (A.31) and (A.30) into (A.29), it is found that:

$$\begin{aligned} t_{d(i)} - t_{d(\mathrm{i}-1)} &= \frac{s_n + s_f}{s_f} \frac{-V_{th} C_r}{I_r + s_n C_r + g_{mr} \cdot v_{on}(\mathrm{t}_{i-1} + T_{on(\mathrm{i}-1)} - t_{d(i-1)})} + T_{CLK} \\ &= \frac{1}{D}\left[\frac{-V_{th} C_r}{I_r + s_n C_r + g_{mr} \cdot v_{on}(\mathrm{t}_{i-1} + T_{on(\mathrm{i}-1)} - t_{d(i-1)})} + \frac{V_{th} C_r}{I_r + s_n C_r}\right] \\ &= \frac{V_{th} C_r}{D}\left\{\frac{g_{mr} \cdot v_{on}(\mathrm{t}_{i-1} + T_{on(\mathrm{i}-1)} - t_{d(i-1)})}{(I_r + s_n C_r)[I_r + s_n C_r + g_{mr} \cdot v_{on}(\mathrm{t}_{i-1} + T_{on(\mathrm{i}-1)} - t_{d(i-1)})]}\right\} \end{aligned} \tag{A.32}$$

Since $I_r + s_n C_r >> g_{mr} \cdot \hat{r} \sin[2\pi f_m \cdot (\mathrm{t}_{i-1} + T_{on(\mathrm{i}-1)} - t_{d(i-1)}) + \theta]$, (4.32) can be simplified as:

$$\begin{aligned} t_{d(i)} - t_{d(\mathrm{i}-1)} &\approx \frac{V_{th} C_r g_{mr} \cdot \hat{r} \sin[2\pi f_m \cdot (\mathrm{t}_{i-1} + T_{on(\mathrm{i}-1)} - t_{d(i-1)}) + \theta]}{(I_r + \mathrm{s}_n \mathrm{C}_r)^2 D} \\ &\approx \frac{V_{th} C_r g_{mr}}{(I_r + \mathrm{s}_n \mathrm{C}_r)^2 D} \hat{r} \sin[2\pi f_m \cdot (\mathrm{t}_{i-1} + T_{on}) + \theta] \end{aligned} \tag{A.33}$$

Next, the perturbed inductor current $\mathrm{i}_{\mathrm{PFD}}(\mathrm{t})$ can be expressed by:

$$i_{PFD}(t)\Big|_{0 \le t \le t_M + T_{CLK}} = -I_d \cdot \sum_{i=1}^{M} [u(t - t_i) - u(t - t_i - t_{d(i)})] \tag{A.34}$$

Then, same as (A.6), Fourier analysis can be performed on the $\mathrm{i}_{\mathrm{PFD}}(\mathrm{t})$ as:

$$c_m = j\frac{2f_m}{N}\int_0^{t_M+T_{CLK}} i_{PFD}(t)\cdot e^{-j2\pi f_m t}dt$$
$$\approx \frac{j2\pi f_m}{N\pi}(-\mathrm{I}_d)\cdot\sum_{i=1}^{M}[e^{-j2\pi f_m(t_i)}t_{\mathrm{d}(i)}] \quad \text{(A.35)}$$

where c_m is the Fourier coefficient of $i_{PFD}(t)$ at the perturbation frequency f_m.

Based on (A.33) and (A.35), it is found that:

$$\begin{aligned}
&c_m - c_m e^{-j2\pi f_m T_{CLK}}\\
&= \frac{-\mathrm{I}_d V_{th} C_r g_{mr}}{(I_r+\mathrm{s}_n\mathrm{C}_r)^2 D}\frac{j2f_m}{N}\sum_{i=1}^{M}\{e^{-j2\pi f_m(t_i)}\hat{r}\sin[2\pi f_m\cdot(\mathrm{t}_{i-1}+T_{on})+\theta]\}\\
&= \frac{-\mathrm{I}_d V_{th} C_r g_{mr}\hat{r}}{(I_r+\mathrm{s}_n\mathrm{C}_r)^2 D(\mathrm{j}2)}\frac{j2f_m}{N}\sum_{i=1}^{M}\{e^{-j2\pi f_m(t_i)}[e^{j[2\pi f_m\cdot(\mathrm{t}_{i-1}+T_{on})+\theta]}-e^{-j[2\pi f_m\cdot(\mathrm{t}_{i-1}+T_{on})+\theta]}]\}\\
&= \frac{-\mathrm{I}_d V_{th} C_r g_{mr}}{(I_r+\mathrm{s}_n\mathrm{C}_r)^2 D}\frac{f_m}{N}\hat{r}\{\sum_{i=1}^{M}e^{j2\pi f_m\cdot(\mathrm{t}_{i-1}+T_{on}-\mathrm{t}_i)}e^{j\theta}-\sum_{i=1}^{M}e^{-j2\pi f_m\cdot(\mathrm{t}_{i-1}+T_{on}+\mathrm{t}_i)}e^{-j\theta}\}\\
&= \frac{-\mathrm{I}_d V_{th} C_r g_{mr}}{(I_r+\mathrm{s}_n\mathrm{C}_r)^2 D}\frac{f_m}{N}\hat{r}\{\sum_{i=1}^{M}e^{-j2\pi f_m\cdot(T_{CLK}-T_{on})}e^{j\theta}-\sum_{i=1}^{M}e^{-j2\pi f_m\cdot[(2\mathrm{i}-3)T_{CLK}+T_{on}]}e^{-j\theta}\}\\
&= \frac{-\mathrm{I}_d V_{th} C_r g_{mr}}{(I_r+\mathrm{s}_n\mathrm{C}_r)^2 D}\frac{f_m}{N}\hat{r}\{Me^{-j[2\pi f_m\cdot(1-D)\mathrm{T}_{CLK}]}e^{j\theta}-0\}\\
&= \frac{-\mathrm{I}_d V_{th} C_r g_{mr}}{(I_r+\mathrm{s}_n\mathrm{C}_r)^2 D}(\frac{Mf_m}{N})(\hat{r}e^{j\theta})e^{-j[2\pi f_m\cdot(1-D)\mathrm{T}_{CLK}]}
\end{aligned} \quad \text{(A.36)}$$

Then, after Fourier analysis can be performed on $i_{PFD}(t)$, the coefficient is calculated as:

$$c_m = \frac{-I_d V_{th} C_r g_{mr}}{(I_r+\mathrm{s}_n\mathrm{C}_r)^2 DT_{CLK}}\frac{e^{-j2\pi f_m(1-\mathrm{D})T_{CLK}}}{(1-e^{-j2\pi f_m T_{CLK}})}(\hat{r}e^{j\theta}) \quad \text{(A.37)}$$

Since the Fourier coefficient of v_{on} is $\hat{r}e^{j\theta}$, the describing function of v_{on}-to-i_{PFD} transfer function in the s-domain can be calculated as:

$$\frac{i_{PFD}(s)}{v_{on}(s)} = \frac{-I_d V_{th} C_r g_{mr}}{(I_r + s_n C_r)^2 D T_{CLK}} \frac{e^{-s(1-D)T_{CLK}}}{1-e^{-sT_{CLK}}} \tag{A.38}$$

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A. Introduction

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