Design, Fabrication and Characterization of a GaAs/$In_xGa_{1-x}As$/GaAs Heterojunction Bipolar Transistor

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ABSTRACT

Designs for PnP GaAs/$In_xGa_{1-x}As$/GaAs heterojunction bipolar transistors (HBTs) are proposed and simulated with the aid of commercial software. Band diagrams, Gummel plots and common emitter characteristics are shown for the specific case of x=1, x=0.7, and x linearly graded from 0.75 to 0.7. Of the three designs, it is found that the linearly graded case has the lowest leakage current and the highest current gain. IV curves for all four possible classes of InAs/GaAs heterojunction (nN, nP, pN, pP) are calculated. A pN heterojunction is fabricated and characterized. In spite of the 7% lattice mismatch between InAs and GaAs, the diode has an ideality factor of 1.26 over three decades in the forward direction. In the reverse direction, the leakage current grows exponentially with the magnitude of the bias, and shows an effective ideality factor of 3.17, in stark disagreement with simulation. IV curves are taken over a temperature range of 105 K to 405 and activation energies are extracted. For benchmarking the device processing and the characterization apparatus, a conventional GaAs homojunction diode was fabricated and characterized, showing current rectification ratio of 10^9 between plus one volt and minus one volt. Because the PnP material for the optimal HBT design was not available, an Npn GaAs/InAs/InAs HBT structure was processed, characterized, and analyzed. The Npn device fails in both theory and in practice; however, by making a real structure, valuable lessons were learned for crystal growth, mask design, processing, and metal contacts.

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I. Introduction

The semiconductor transistor was invented at Bell Laboratories in New Jersey, shortly after the Second World War. By the time of this writing (2014), it has become indispensable in any product with built in-electronics: computers, cell phones, video displays, airplanes, cars, and washing machines. The Bell Labs patent not only described the device which the inventors had made in the lab, but it also made a second speculative claim[1]:

What is claimed is:

1. A solid conductive device for controlling electrical energy that comprises a body of semiconductive material having two zones of one conductivity type separated by a zone of the opposite conductivity type, said two zones being contiguous with opposite faces of said zone of opposite conductivity type, and means for making electrical connection to each zone.

2. A device as set forth in claim 1 in which one of the separated zones is of a semiconductive material having a wider energy gap than that of the material in the other zones.

The second device has come to be known as a heterostructure bipolar junction transistor (HBT) [2, 3]. The HBT is a higher cost, higher performance device that switches faster than the more common bipolar junction transistor (BJT). As the world continues to become more networked and as data rates increase, there is a demand for transistors that can keep up. InGaAs HBT's have achieved f_T = 710 GHz and f_{MAX} = 340 GHz in the academic laboratory [4]. The trend in commercialized HBT materials has gone from GaAs/AlGaAs to InGaAs/InP to SiGe. The last material has the advantage of low cost and ease of integration with conventional CMOS processes. While not nearly as cheap as silicon, a gallium arsenide substrate is still much cheaper than an indium gallium arsenide substrate. If we could take the high performing f_T = 710 GHz device from the lab to the commercial market by changing from the expensive InGaAs to the cheaper GaAs or InP substrate, it would be a step in the right direction.

Figure 1 (after Streetman and Banerjee [5]) is a conceptual illustration of the various components of currents in a pnp transistor. Typically, designers strive to minimize the recombination current in the base (current component 1 in Figure 1), as this allows the collector current (component 2) to be controlled by small changes in the base current. If the reverse biased base-collector junction leaks, then there will be an output current (current component 3), even when the base current is zero. This leakage is noise which prevents the resolution of small base currents. This current will never be zero, but we will explore different designs to reduce it in section II. The externally applied electron current at the base exactly matches the recombination current and maintains charge neutrality. It is the signal that gets amplified in a common emitter configuration. Some electrons will flow from the base to the emitter (current component 5), but the designer can minimize this by exploiting the band-edge offsets of the heterostructure.

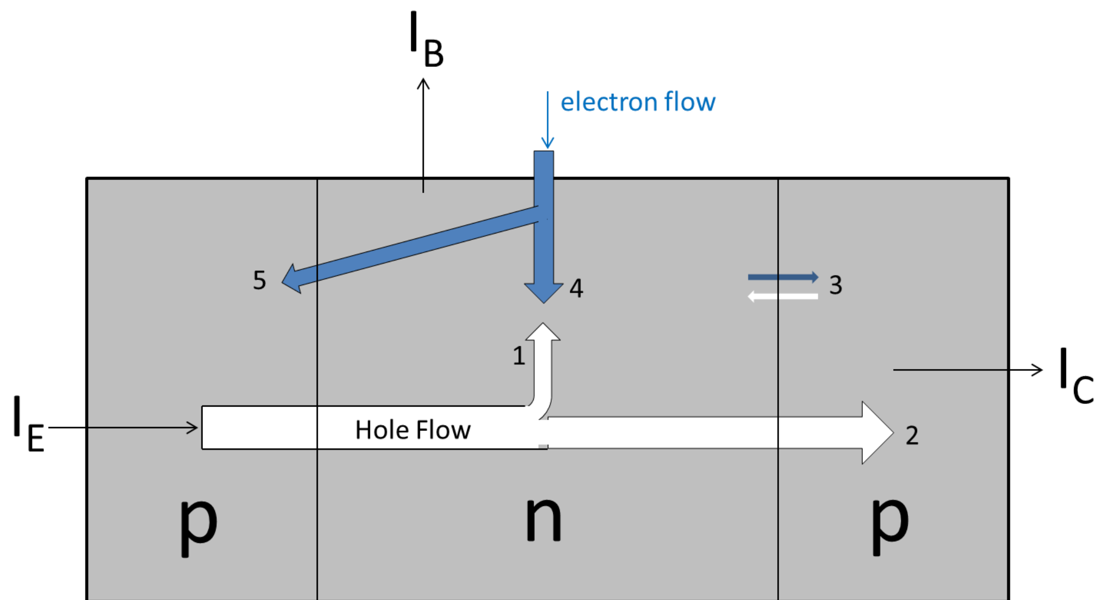


Figure 1. Summary of charge flow in a pnp transistor[5]. 1) Holes lost to recombination in the base. 2) Holes reaching the collector. 3) Leakage current, in the absence of externally supply base current, at the reverse biased base-collector junction. 4) Base recombination current. 5) Electrons emitted across the forward biased emitter junction.

In the equations that follow, let I denote current, with the subscripts E, B, C denoting emitter, base and collector, respectively. The subscript n denotes electrons and the subscript p denotes holes. L is the diffusion length and μ is the mobility. For these two

symbols, in (1.3), the superscript denotes the side of the emitter-base junction. For example, μ_n^p is the mobility of electrons in the p-type emitter. W_b is the length of the neutral material in the base. ΔE_C is the conduction band offset between the emitter and the base (Figure 2). *T* is the temperature in Kelvin and *k* is Boltzmann's constant. (1.4) and (1.5) are definitions of α and β. In (1.6), τ_p is the hole lifetime and τ_t is the transit time in the base.

$$I_C = BI_{Ep} \qquad (1.1)$$

$$\gamma = \frac{I_{Ep}}{I_{En} + I_{Ep}} \qquad (1.2)$$

$$\frac{I_{En}}{I_{Ep}} = \frac{L_p^n n_n \mu_n^p}{L_n^p p_p \mu_p^n} \tanh \frac{W_b}{L_p^n} e^{-\Delta E_C/kT} \simeq \frac{W_b n_n \mu_n^p}{L_n^p p_p \mu_p^n} e^{-\Delta E_C/kT} \qquad (1.3)$$

$$\frac{I_C}{I_E} = \frac{BI_{Ep}}{I_{En} + I_{Ep}} = B\gamma \equiv \alpha \qquad (1.4)$$

$$\frac{I_C}{I_B} = \frac{\alpha}{1-\alpha} \equiv \beta \qquad (1.5)$$

$$\beta = \frac{\tau_p}{\tau_t}, \text{ for } \gamma \approx 1 \qquad (1.6)$$

(1.1) and (1.2) define the *base transport factor*, B, and the *emitter injection efficiency*, *γ*. We will later work with a material system in which ΔE_C is 870meV. Taking kT as 25 meV, $e^{-\Delta E_C/kT}$ is about 10^{-15}. According to (1.2) and (1.3), we have great freedom in choosing values for n_n and p_p, while still keeping γ very close to 1. This is not the case for BJT's in which the emitter injection efficiency is kept high by doping the emitter higher than the base. As long as γ is very close to 1, we can use expression (1.6) for β.

In a mismatched system like GaAs/InAs it is a challenge to make a working HBT let alone one with a large value of β. The designer and process engineer have little control over τ_p: it is a property of the materials and growth conditions. Due to the high number

of dislocations in this heterostructure, the hole lifetime will be shorter than it would be in homojunction device. However, the designer has some control over the transit time, τ_t:

$$\tau_t \approx \frac{W_b}{v_{pb}} \approx \frac{W_b}{\mu_p F} \qquad (1.7),$$

where v_{pb} is the hole velocity in the base and F is the electric field in the neutral base. According to (1.6), to make β large, we should make τ_t small. One way to do this is by making the neutral base width, W_b, small. But for material reasons, we cannot make it arbitrarily small. Measurements that will be presented later show that the surface of InAs grown on GaAs is rough, having depressions or "craters" that are more than 15 nm deep. If the base layer is grown to be 50 nm thick, but it has two craters in the same position, at opposite interfaces, then the base will be 20 nm thick in that place. For this reason, we simulate both a 50 nm thick base as well as a 200 nm thick base. Even though a 200 nm base will have a lower gain, the base is thick enough that the craters should be only a minor perturbation. Another way to make τ_t small is to make the denominator in (1.7) big. We can increase the electric field by grading the base composition so that a local electric field exists in the base and propels the hole.

Lattice mismatch refers to the situation in which two materials of differing lattice constant share an interface. Typically such a structure is formed by epitaxial growth. Unless the thickness of the film is less than a critical thickness, the film will have defects. We adhere to the convention that an upper case letter (N or P) refers to the doping of the larger bandgap material (GaAs) and a lower case letter (n or p) refers to the doping of the smaller bandgap material (InAs). A literature search shows earlier work on growth of InAs on GaAs to make diodes, BJT's and HBT's. Dobbelaere et al. have investigated InAs p-n diodes grown on both GaAs and GaAs on Si [6]. In reverse bias, the current has two temperature regimes. At low temperatures there is weak temperature dependence, implying a tunneling current. At high temperatures, there is an exponential dependence, with the activation energy close to the band gap. AlSb/InAs/AlSb HBT's have been grown on GaAs substrates, but suffer from high leakage current and low gain, attributable to the large lattice mismatch [7].

InAs BJT's on InP substrates have the same issues [8]. Chen *et al*. investigated nN, nP, pN and pP heterojunctions of relaxed InAs on GaP (the convention of lower- vs. upper-case letters was stated on page . In spite of the large lattice mismatch, they obtained nearly ideal diode characteristics with high break-down voltages [9]. InAs BJT's and InAs/ $Al_xIn_{1-x}As$ HBT's have been grown by molecular beam epitaxy on InAs, on GaAs, and on InP with current gains of over 100 [10-13].

To our knowledge, this work contains the first simulation of a GaAs/InAs/GaAs HBT or a GaAs/$In_{0.7}Ga_{0.3}As$ /GaAs HBT.

II. Computer Simulations of GaAs/InAs Heterojunctions

GaAs has a much higher bandgap than InAs, as Figure 2 shows. But because the electron affinity of InAs is 0.87 eV (Table 1) higher than the electron affinity of GaAs, the conduction band of InAs is further from the conduction band of GaAs, compared with the separation of the valence bands. This will have consequences for the performance of pnp HBT's versus npn HBT's made from these materials.

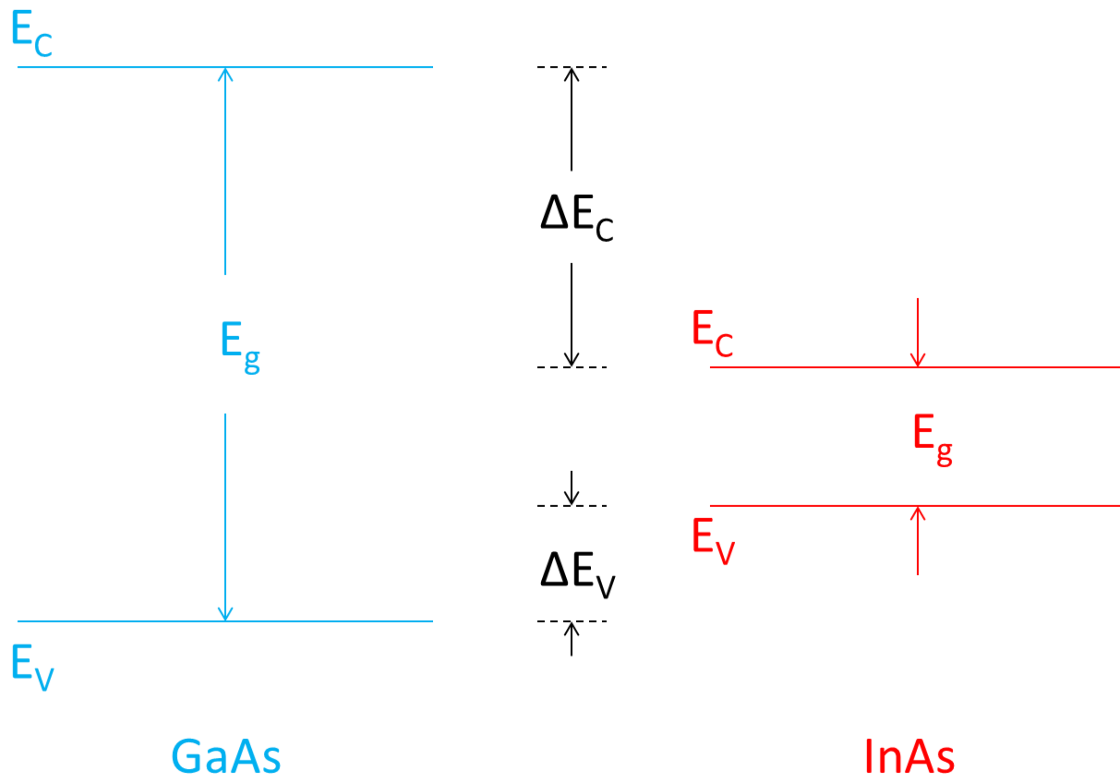


Figure 2. The energy bandgap of GaAs, 1.42 eV, is about four times as large as the energy bandgap of InAs, 0.35 eV. In addition, the conduction band offset between GaAs and InAs, about 0.87 eV, is about four times as large as the valence band offset, about 0.2 eV. These physical facts will favor PnP HBT designs over NpN HBT designs.

Table 1. Partial list of parameters used in simulations [14].

Property	**InAs**	**GaAs**
Bandgap (eV)	0.3501	1.4218

Electron affinity (eV)	4.97	4.1
Electron mass (m_0)	0.024	0.067
Hole mass (m_0)	0.2689	0.3575
Dielectric constant	14.3	12.9

All four classes of GaAs-InAs junction (Pn, Np, Pp and Nn) are simulated in Figure 4 and Figure 5. We choose the doping of Figure 3 because it matches the diode that will be characterized in section 0.

The spikes in the band diagrams of Figure 4 are more prominent (higher and wider) when GaAs is n-doped than when it is p-doped. This is consistent with the current-voltage curves of Figure 5. At moderate forward bias, $0 < V_B < 0.5V$, the current of the Pn junction is several orders of magnitude greater than the current of the Np junction. Later on, and for this reason, we will choose the PnP HBT design, rather than the NpN HBT design. Just as with forward bias, the reverse bias current for the Pn case is greater than the reverse bias current for the Np case. The reverse bias current has a much weaker bias dependence for the Pn case than for the Np case, suggesting that tunneling plays a greater role in the latter. Tunneling also occurs in the Pn junction, but in this voltage range, it is swamped by the diffusive current component. At high forward bias, the current is limited by ohmic resistance. Above 0.6 V, the Nn junction has the highest current of the four because the electron mobility is higher than the hole mobility, both for GaAs and InAs.

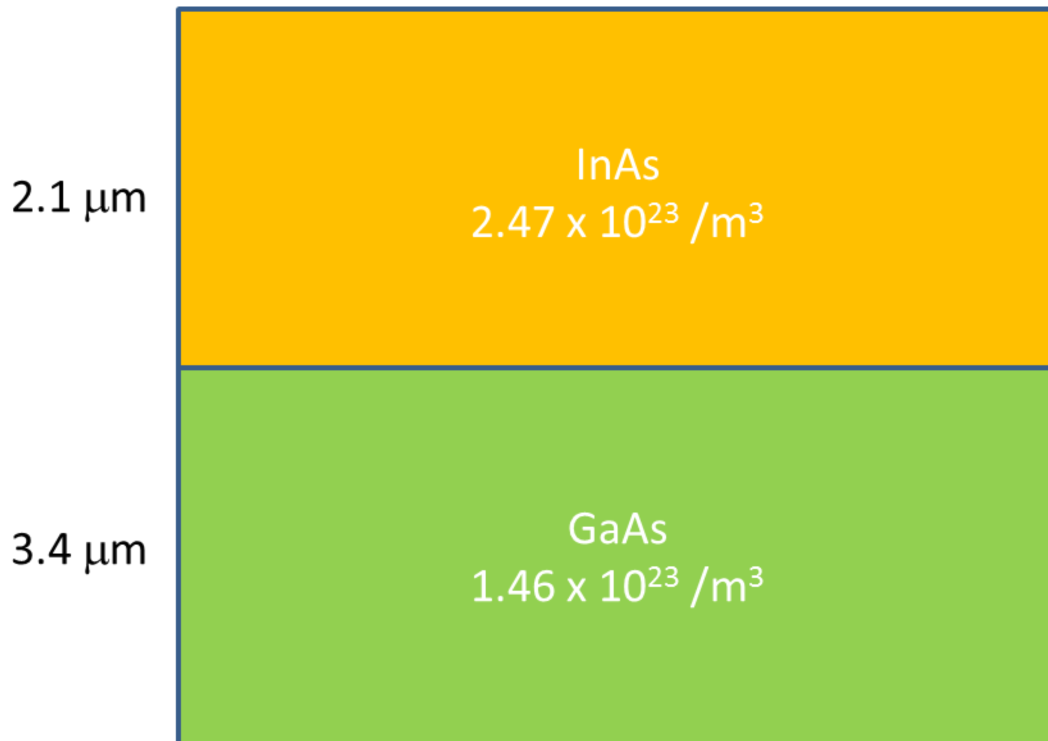


Figure 3. Heterostructure simulated in Figure 4 and Figure 5.

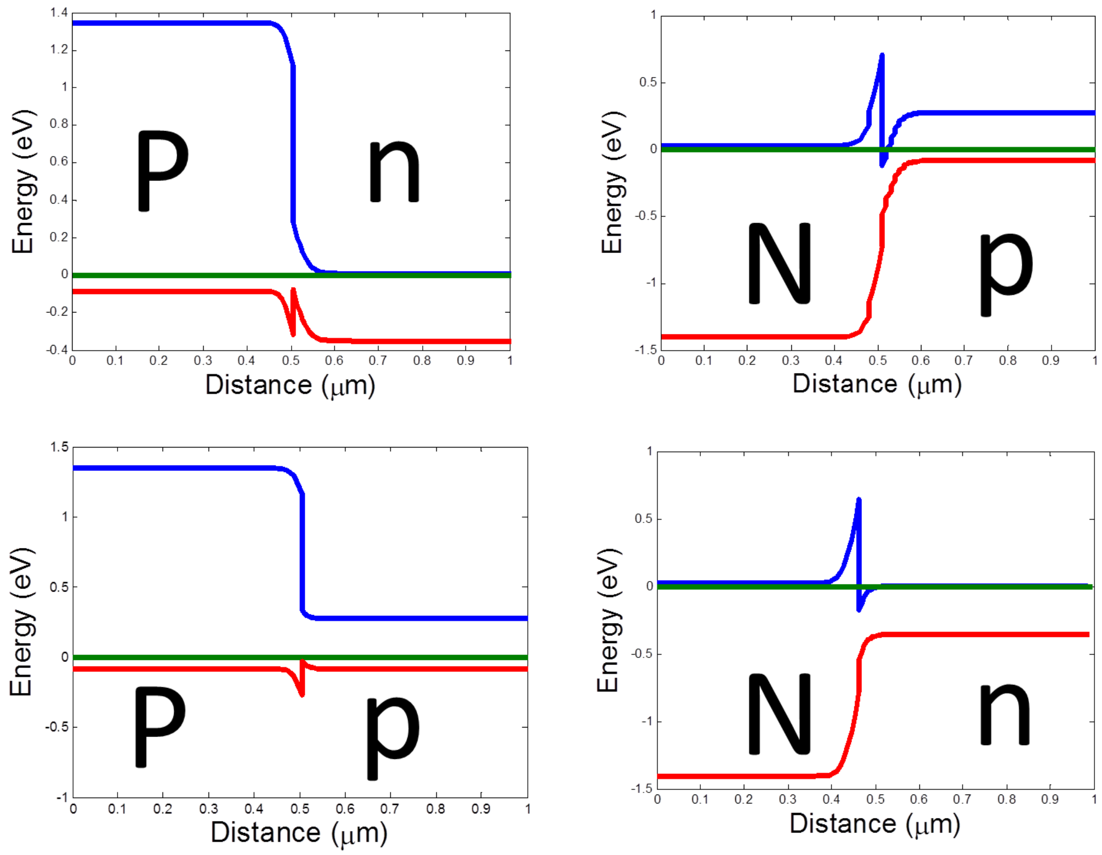


Figure 4. Equilibrium band diagrams for the GaAs-InAs Heterojunction. The upper case letter indicates the type (electron or hole) of doping on the GaAs side, and the lower case letter indicates the type of doping (electron or hole) on the InAs side. GaAs is doped at 1.2 x 10^{17} cm^{-3}. InAs is doped at 2.5 x 10^{17} cm^{-3}.

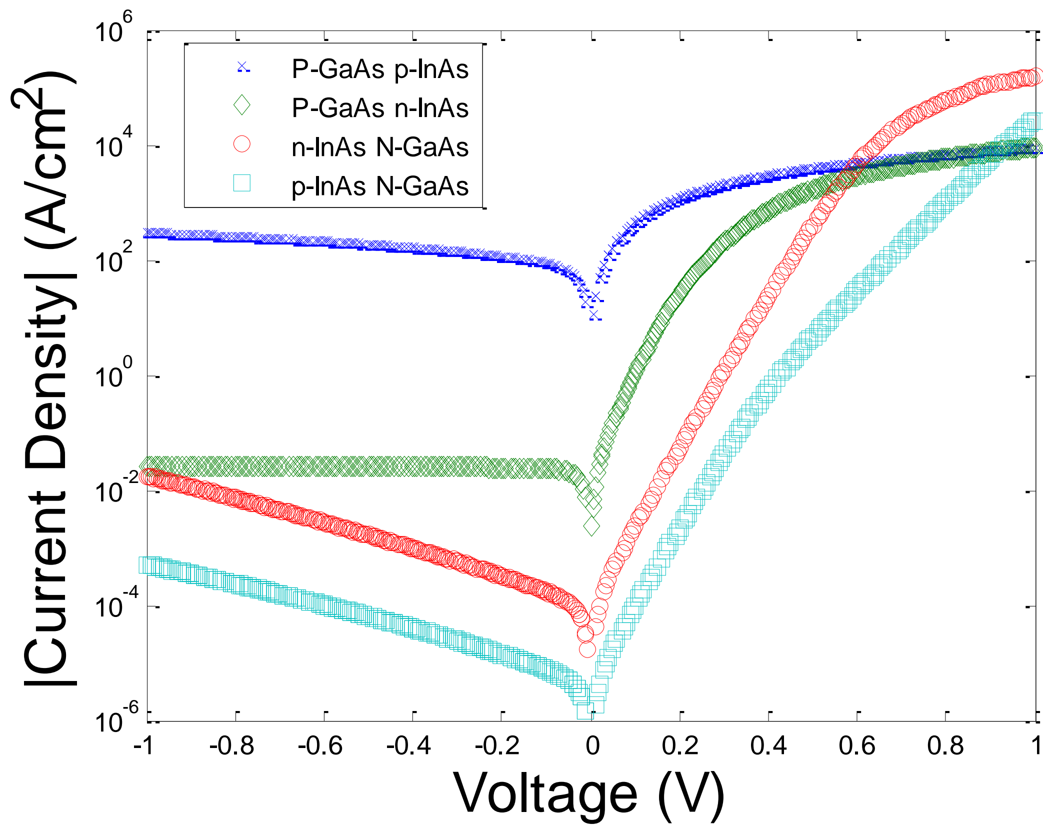


Figure 5. Current voltage curves for the GaAs-InAs Heterojunction. GaAs is doped at 1.2×10^{17} cm^{-3}. InAs is doped at 2.5×10^{17} cm^{-3}

III. Computer Aided Design of a $GaAs/In_xGa_{1-x}As/GaAs$ Heterojunction Bipolar Transistor

Our first design is a PnP GaAs/InAs/GaAs HBT. Figure 6 shows the device in equilibrium, off state, and forward active, on state. In the off state, there is a very narrow tunneling barrier at the collector-base junction which will lead to high leakage current, as we will see shortly in our current-voltage simulations. There is a tradeoff involved in replacing the InAs base with a $In_{0.7}Ga_{0.3}As$ base, as shown in the second design of Figure 7. On the one hand, the change in the energy gap difference between emitter and base is reduced, potentially reducing the gain. On the other hand, the hole barrier in the off state is more robust, reducing leakage current. The simulation includes a highly doped emitter cap for reduced contact resistance. The third and last design improvement uses a compositionally graded base (Figure 8). The indium content of the base is linearly graded from 0.7 to 0.75, from the emitter junction to the collector junction. The grading creates a ramp in the base that propels the hole, reduces transit time, and reduces recombination. This increases the current gain, β.

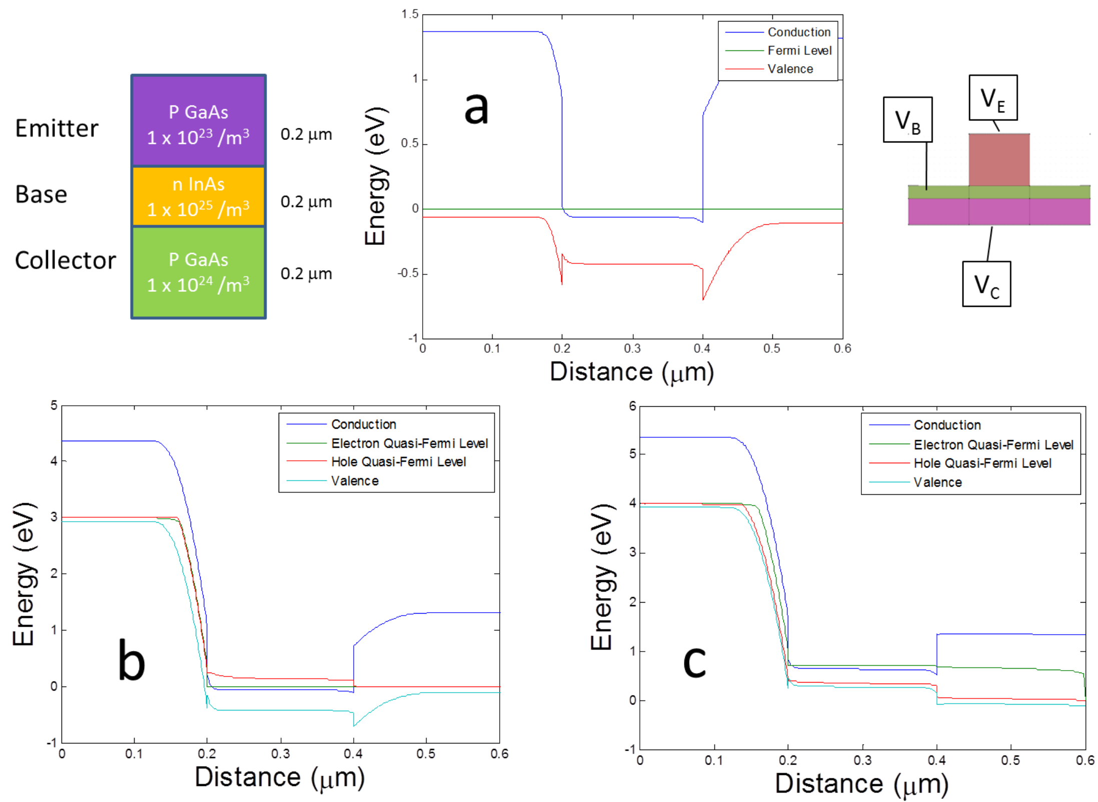


Figure 6. Energy band diagrams with collector at left and emitter at right:

a) Equilibrium. b) $V_{BC} = 3V$, $V_{EB} = 0$. c) $V_{EC} = 4V$, $V_{EB} > 0$.

Top left: Layer structure of PnP GaAs/InAs/GaAs HBT with 200 nm base

Top right: Biasing diagram of mesa structure.

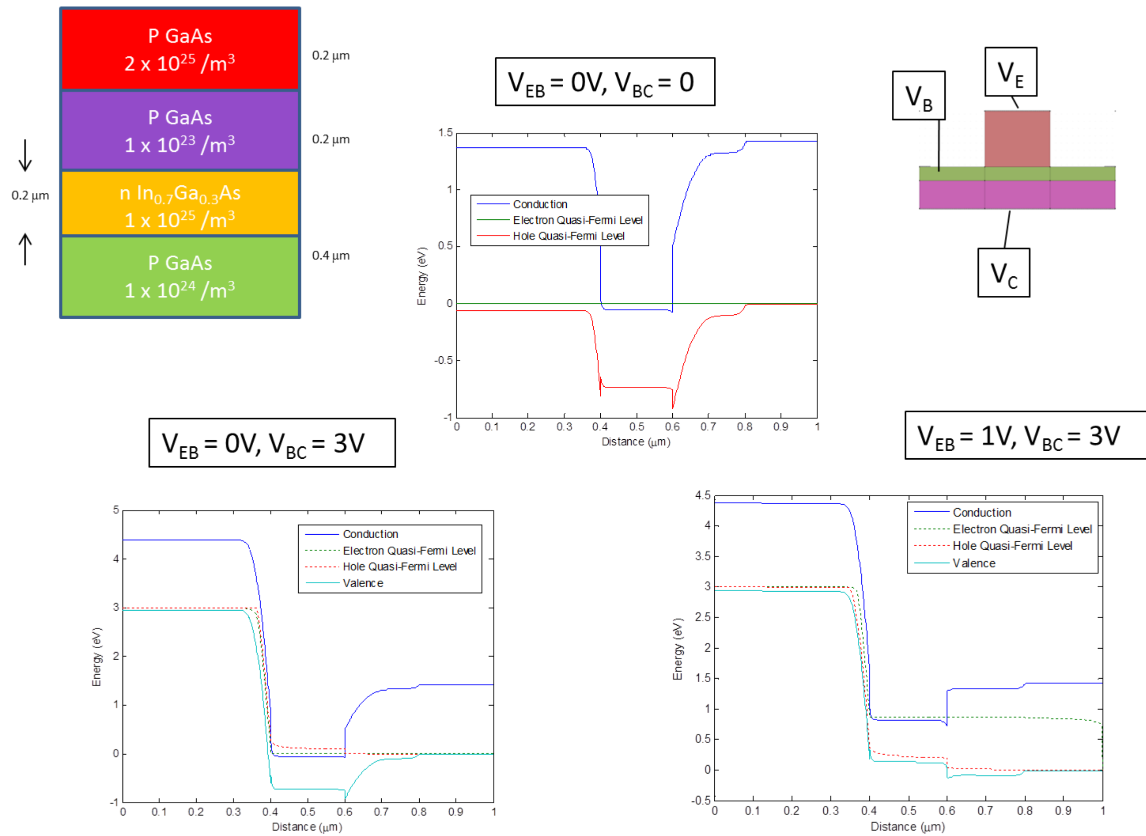


Figure 7. Top center and bottom: Energy band diagrams with collector at left ($0 < x < 0.4$) and emitter at right ($0.6 < x < 1$). Note that the x-axis range is different from previous plots.

Top left: Layer structure of PnP GaAs/$In_{0.7}Ga_{0.3}As$/GaAs HBT with 200 nm base The heavily doped emitter cap reduces contact resistance.

Top right: Biasing diagram of mesa structure

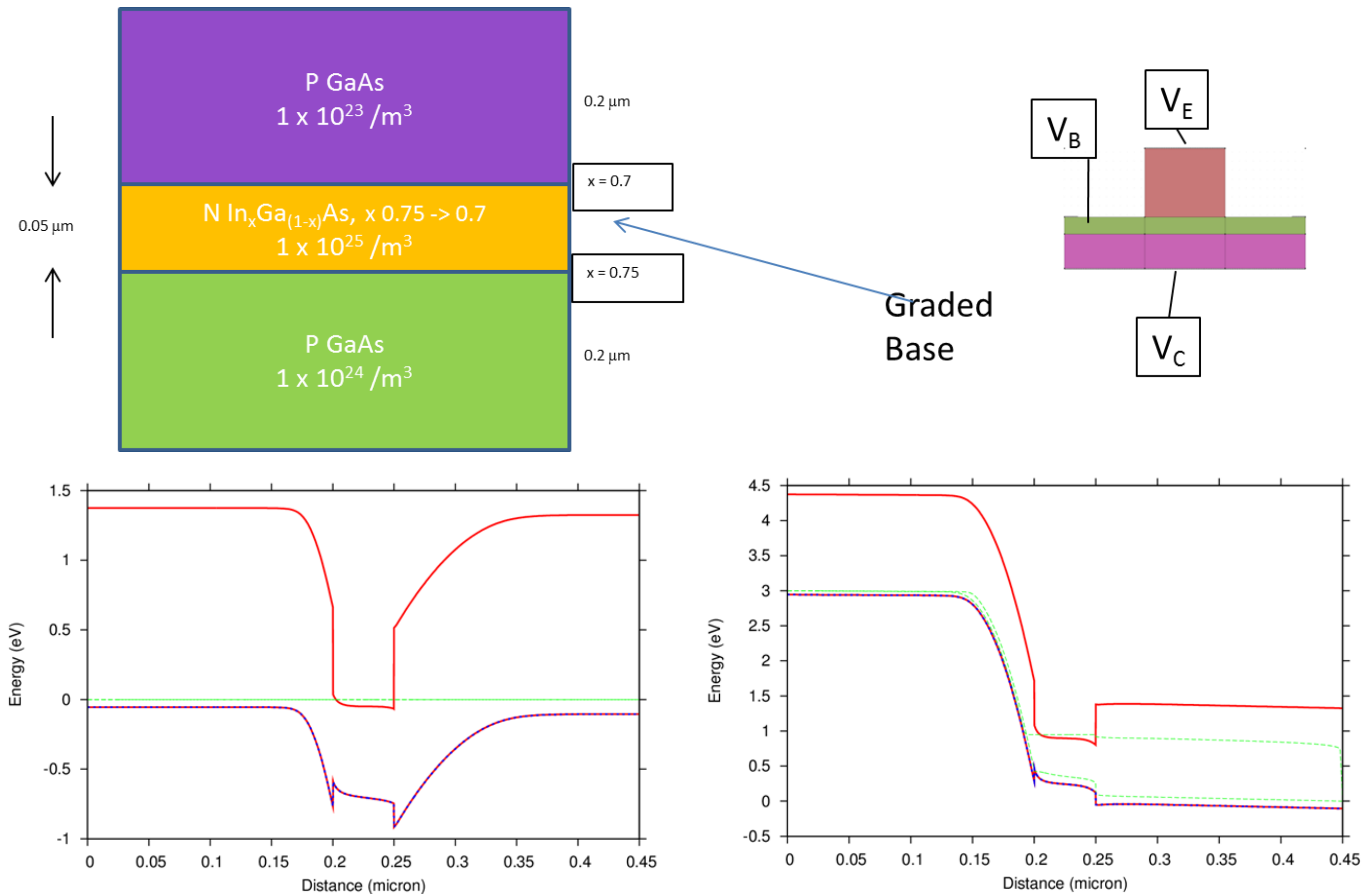


Figure 8. Bottom row: Band diagrams at equilibrium (left) and in forward active mode (right). The grading creates a ramp in the base that propels the hole, reduces transit time, and reduces recombination. This increases the current gain, β. Note that the x-axis range is different from previous plots.
Top left: Layer structure of PnP GaAs/$In_xGa_{(1-x)}As$/GaAs HBT with 50 nm graded base. The indium content of the base is linearly graded from x = 0.7 to x = 0.75, from the emitter junction to the collector junction.
Top right: Biasing diagram of mesa structure

Starting with the our first design we show Gummel and common emitter plots of a PnP GaAs/InAs/GaAs HBT in Figure 9 to Figure 11. Consistent with our observation that the barrier to current flow in the off state of Figure 6b is shallow, we see that although the collector current is sensitive to base current changes on the order of tens of milliamps (Figure 10), it is not sensitive to base current changes on the order of tens of microamps (Figure 11). By changing the base from InAs to $In_{0.7}Ga_{0.3}As$ (Figure 12 - Figure 14), the leakage current is reduced and the collector current responds to base current changes on

the order of tens of microamps. Keeping the same base composition while reducing the base thickness from 200 nm to 50 nm, the current gain β is increased from 106 to 2500 (Figure 15 - Figure 17). If the base is compositionally graded, with indium content changing linearly from 0.75 to 0.7, β is increased from 2500 to 3500 (Figure 18 - Figure 20). Including the physics of tunneling in the simulation changes the collector current only at high emitter-collector bias (Figure 21). All simulations except for Figure 21 included tunneling physics. Table 2 summarizes the results of Figure 6 to Figure 20.

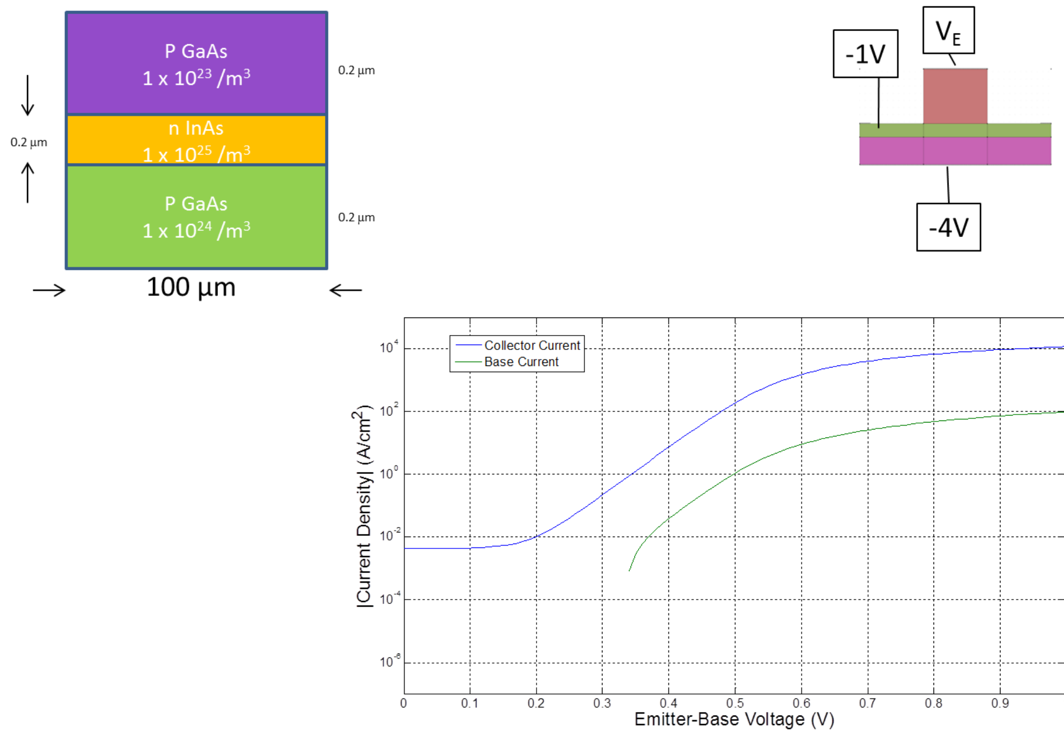


Figure 9. Bottom: Gummel Plot for PnP GaAs/InAs/GaAs HBT with 200 nm base thickness.

Top left: Layer structure.

Top Right. Biasing diagram of mesa structure.

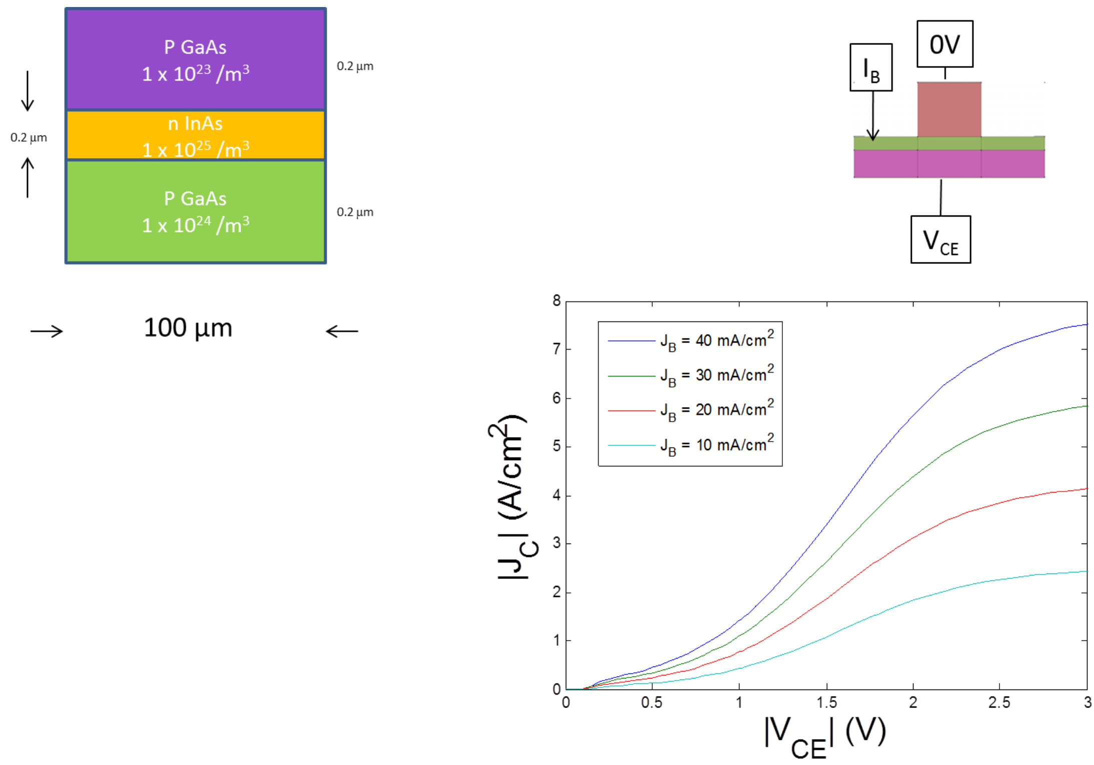


Figure 10. Bottom**:** Common emitter plot for PnP GaAs/InAs/GaAs HBT with 200 nm base thickness, large base current.

Top left: Layer structure.

Top right: Biasing diagram of mesa structure.

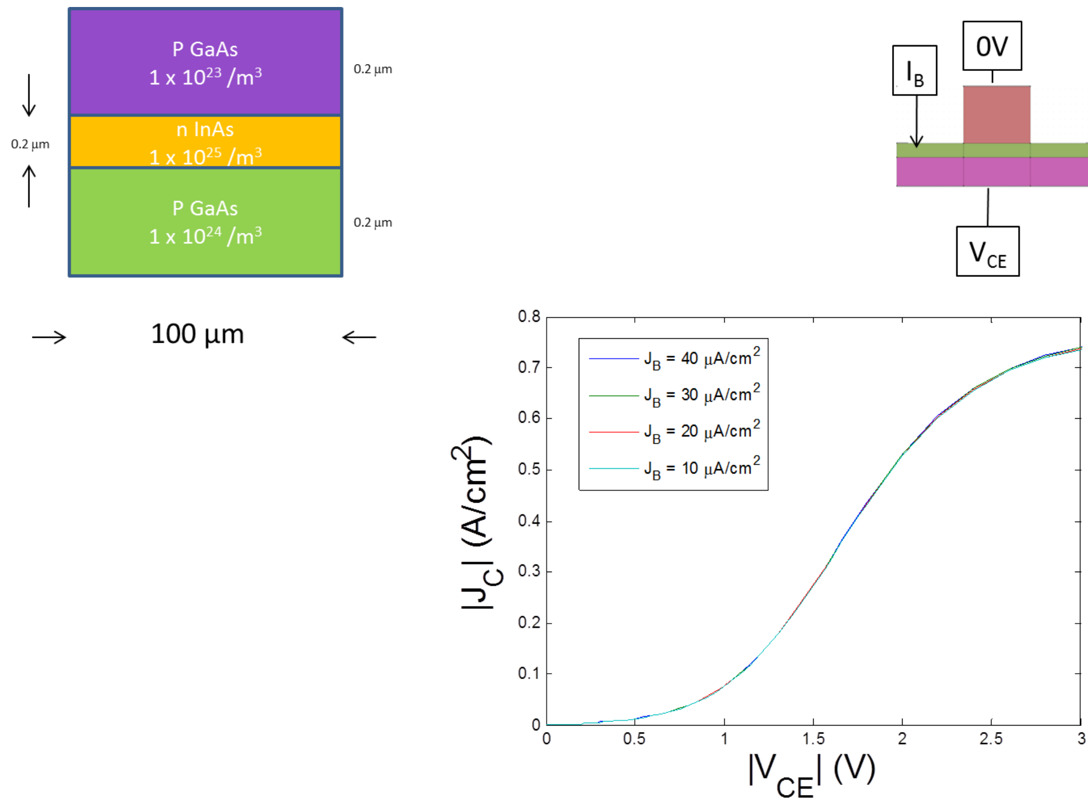


Figure 11. Bottom: Common emitter plot for PnP GaAs/InAs/GaAs HBT with 200 nm base thickness, small base current. Such small base currents get swamped by the leakage current.

Top left: Layer structure.

Top right: Biasing diagram of mesa structure.

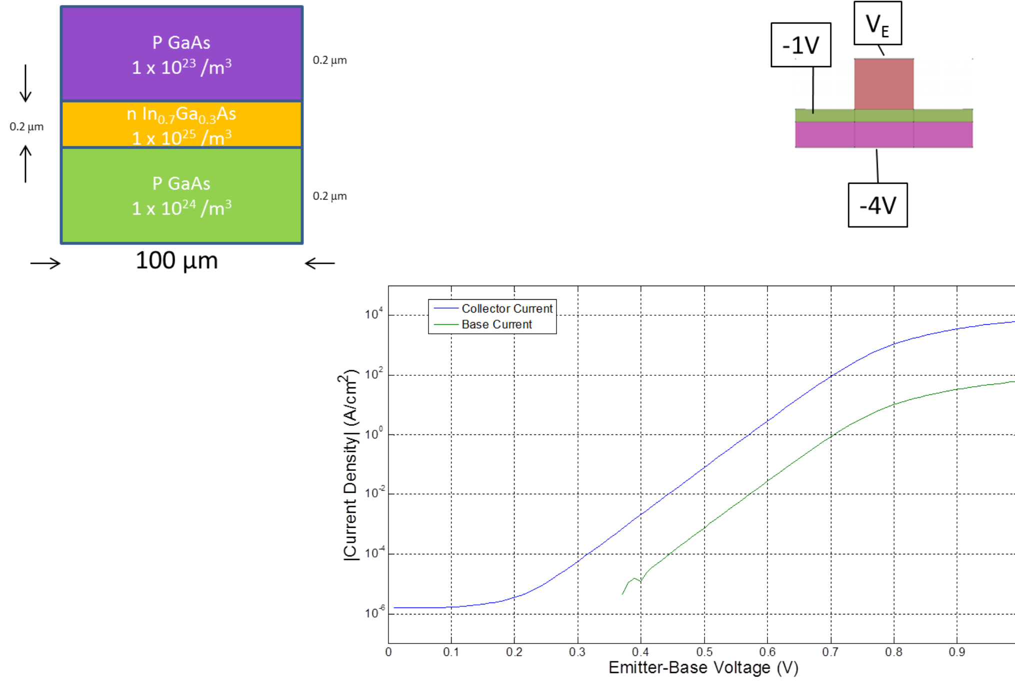


Figure 12. Bottom: Gummel plot for PnP GaAs/$In_{0.7}Ga_{0.3}As$/GaAs HBT with 200 nm base thickness

Top left: Layer structure.

Top right: Biasing diagram of mesa structure.

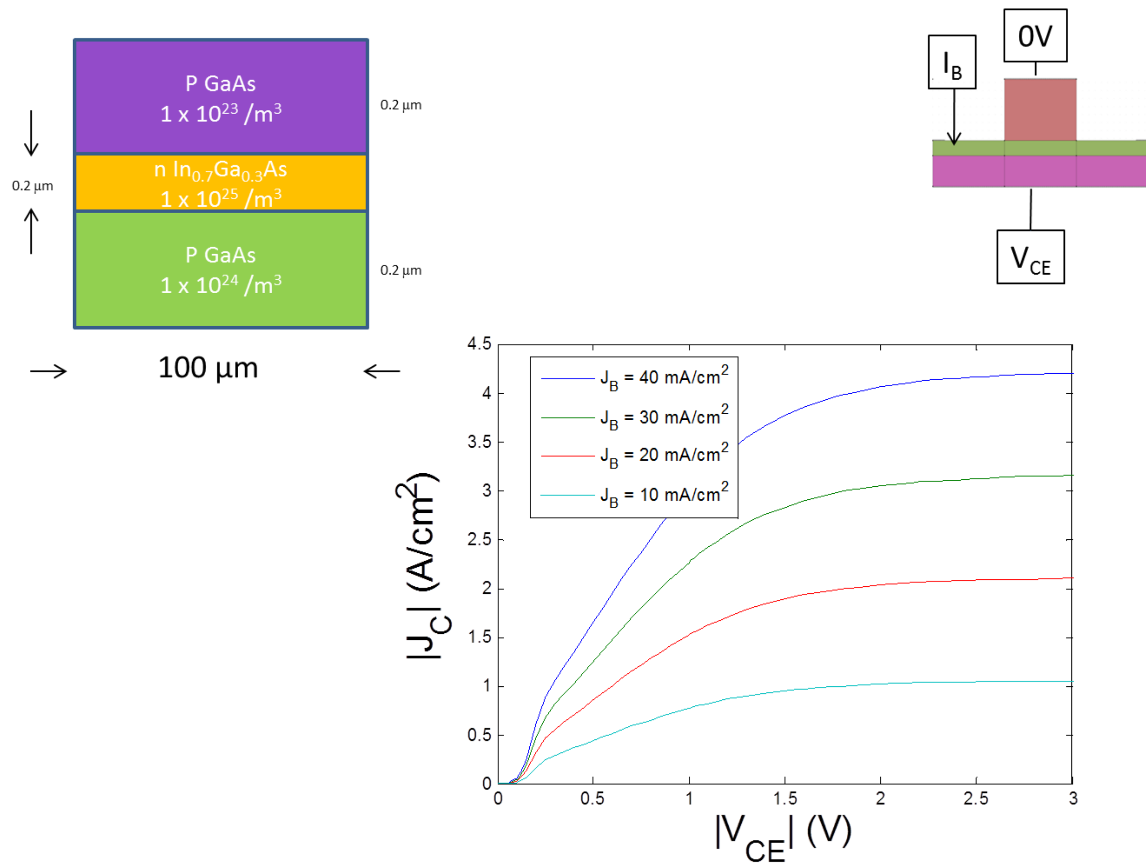


Figure 13. Bottom: Common emitter plot for PnP GaAs/$In_{0.7}Ga_{0.3}As$/GaAs HBT with 200 nm base thickness, large base current.

Top left: Layer structure.

Top right: Biasing diagram of mesa structure.

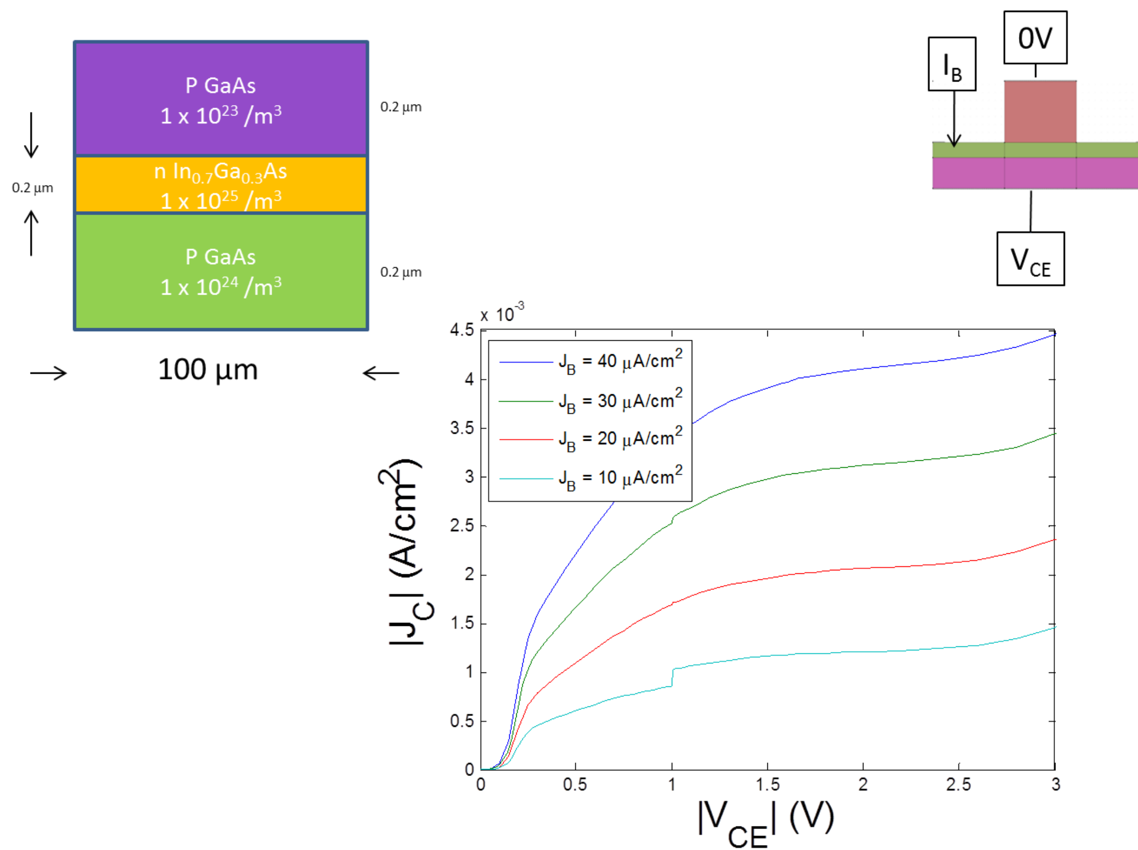


Figure 14. Bottom: Common emitter plot for PnP GaAs/$In_{0.7}Ga_{0.3}As$/GaAs HBT with 200 nm base thickness, small base current.

Top left: Layer structure.

Top right: Biasing diagram of mesa structure.

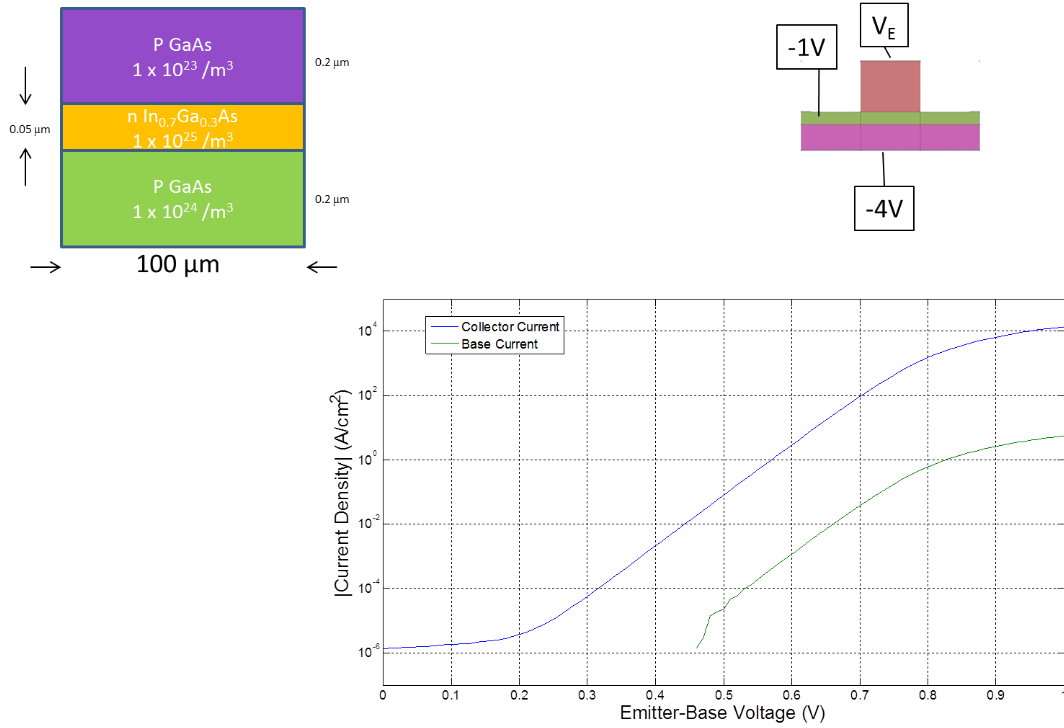


Figure 15. Bottom: Gummel plot for PnP GaAs/$In_{0.7}Ga_{0.3}As$/GaAs HBT with 50 nm base thickness.

Top left: Layer structure.

Top right: Biasing diagram of mesa structure.

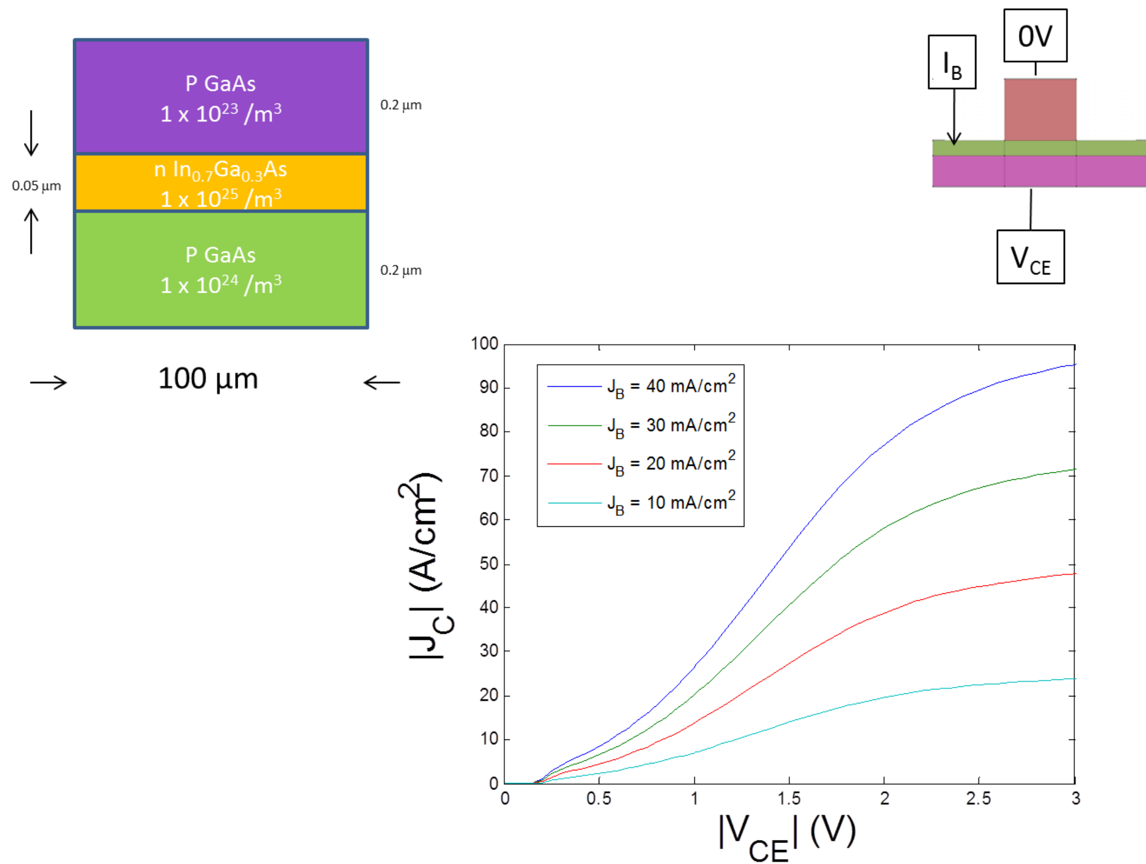


Figure 16. Bottom: Common emitter plot for PnP GaAs/$In_{0.7}Ga_{0.3}As$/GaAs HBT with 50 nm base thickness, large base current.

Top left: Layer structure.

Top right: Biasing diagram of mesa structure.

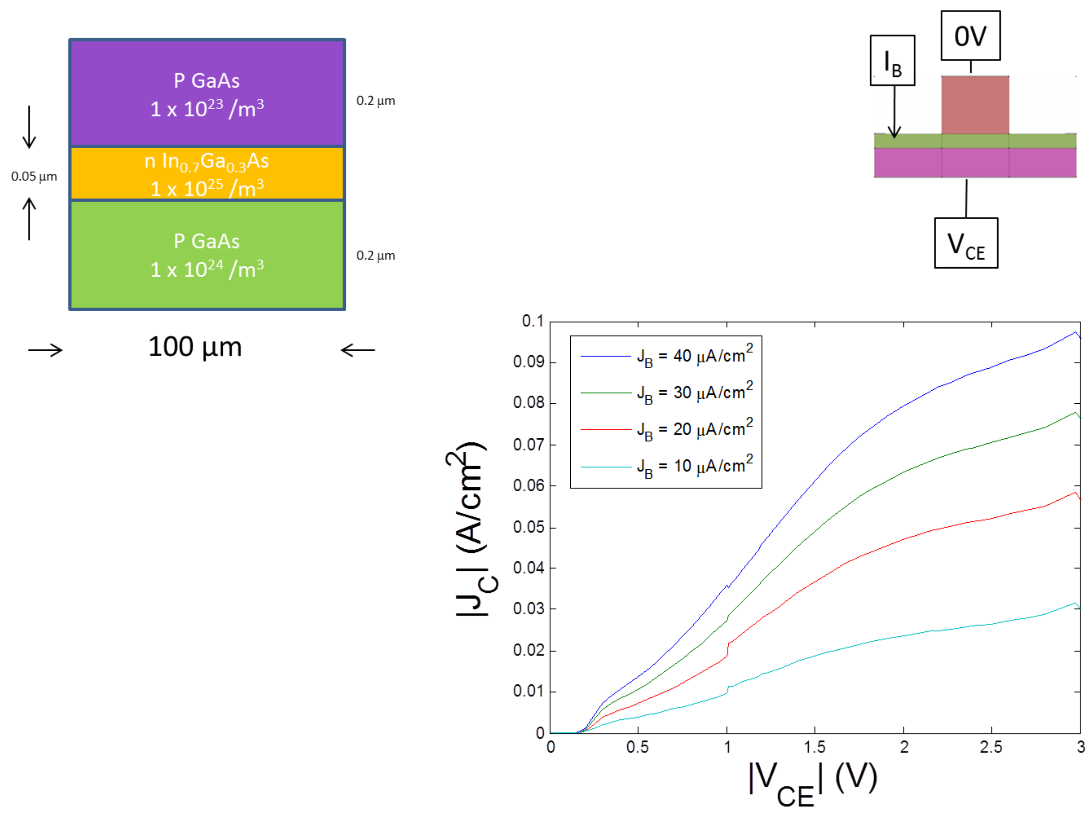
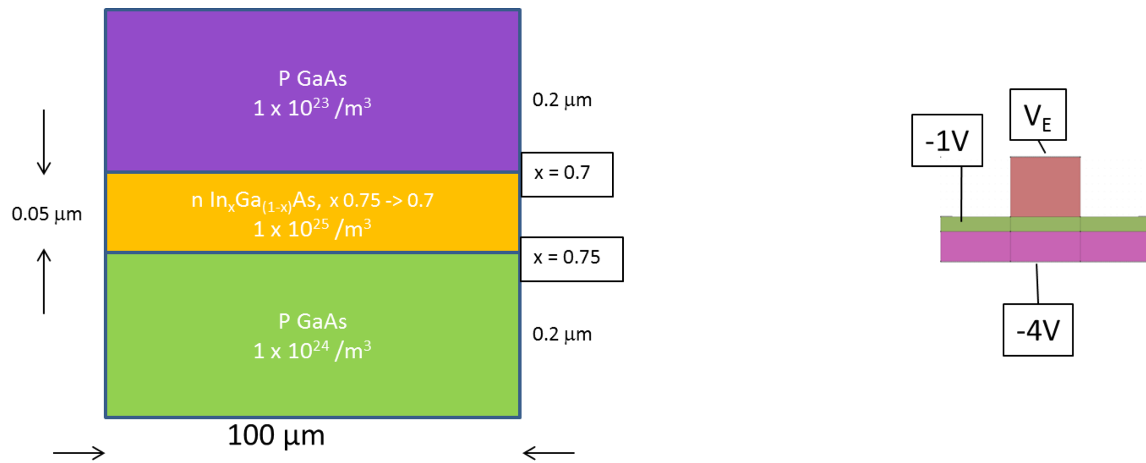


Figure 17 Bottom: Common emitter plot for PnP GaAs/$In_{0.7}Ga_{0.3}As$/GaAs HBT with 50 nm base thickness, small base current.

Top left: Layer structure.

Top right: Biasing diagram of mesa structure.



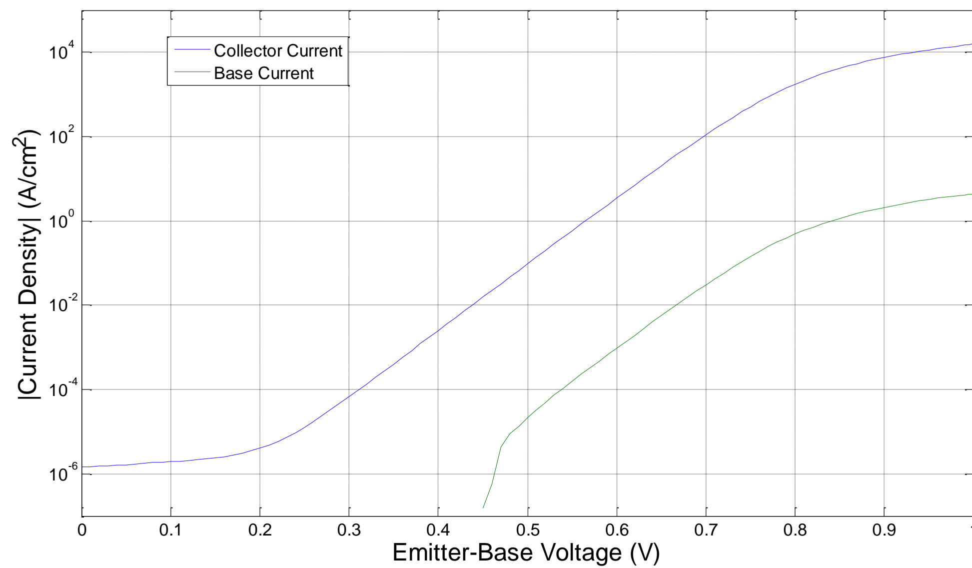
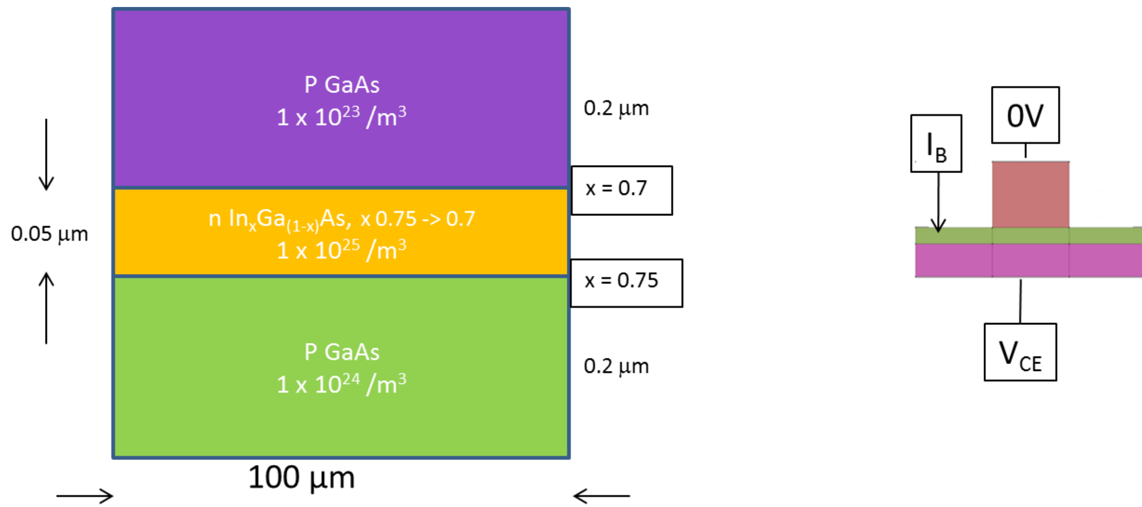


Figure 18. Bottom: Gummel plot for PnP GaAs/$In_xGa_{(1-x)}$As/GaAs HBT with 50 nm base thickness. The base is compositionally graded, with indium content changing linearly from 0.75 to 0.7.

Top left: Layer structure.

Top right: Biasing diagram of mesa structure.



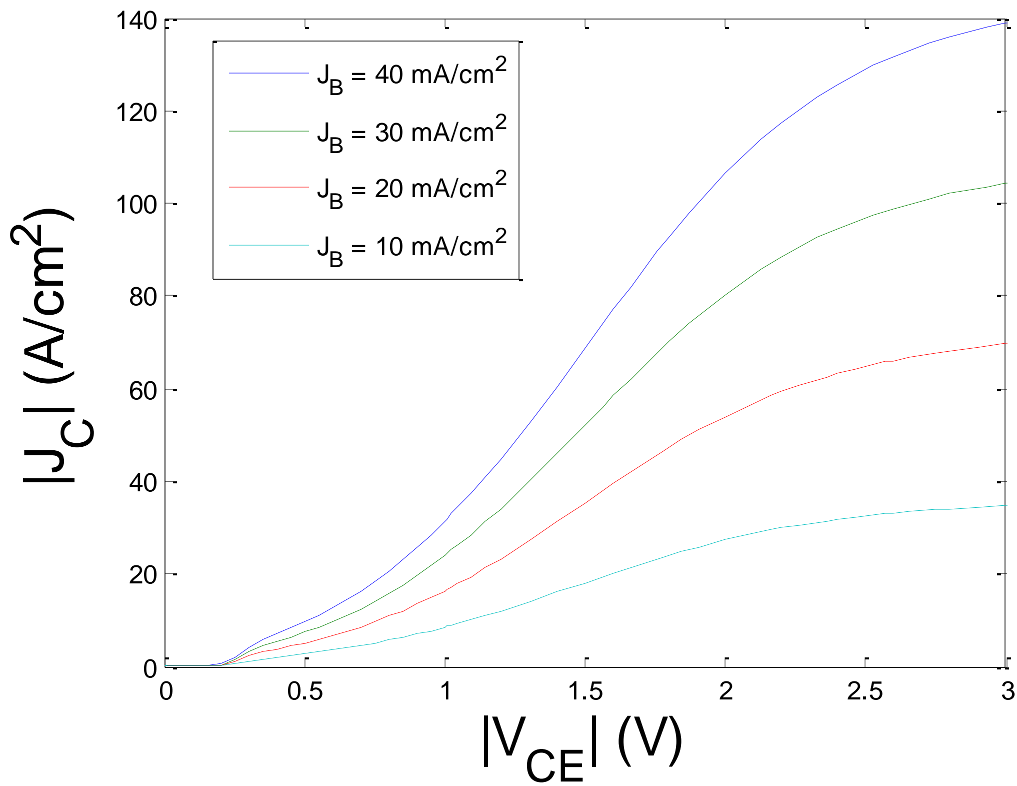
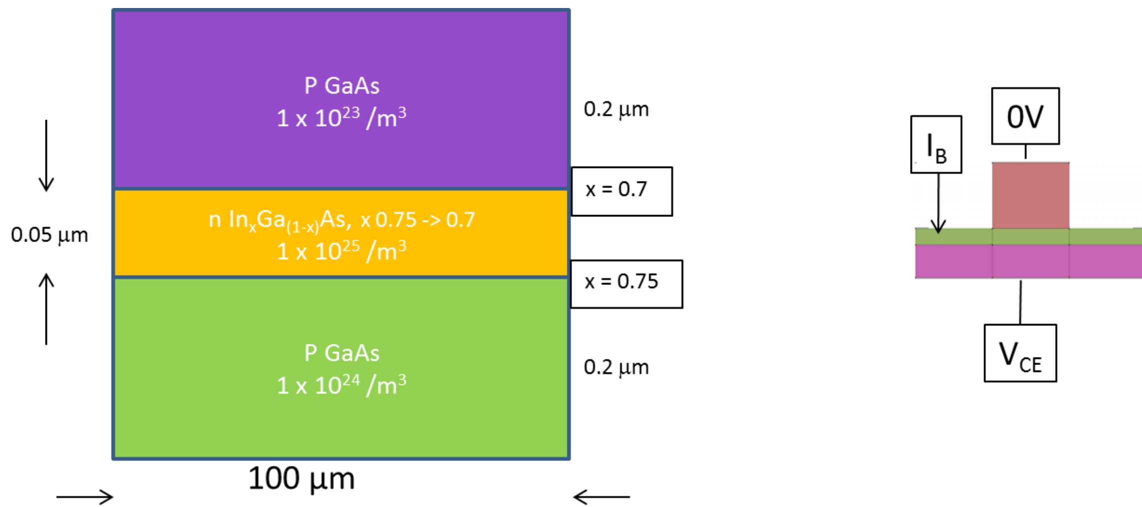


Figure 19. Bottom: Common emitter plot for PnP GaAs/$In_xGa_{(1-x)}As$/GaAs HBT with 50 nm base thickness and large base currents. The base is compositionally graded, with indium content changing linearly from 0.75 to 0.7.

Top left: Layer structure.

Top right: Biasing diagram of mesa structure.



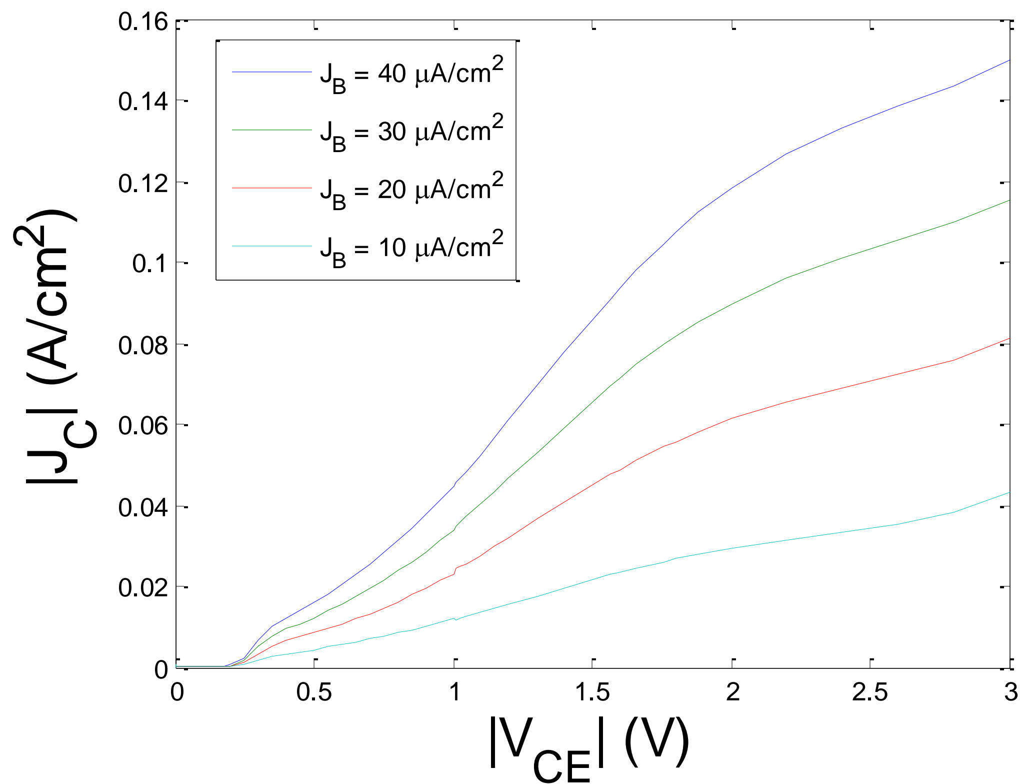
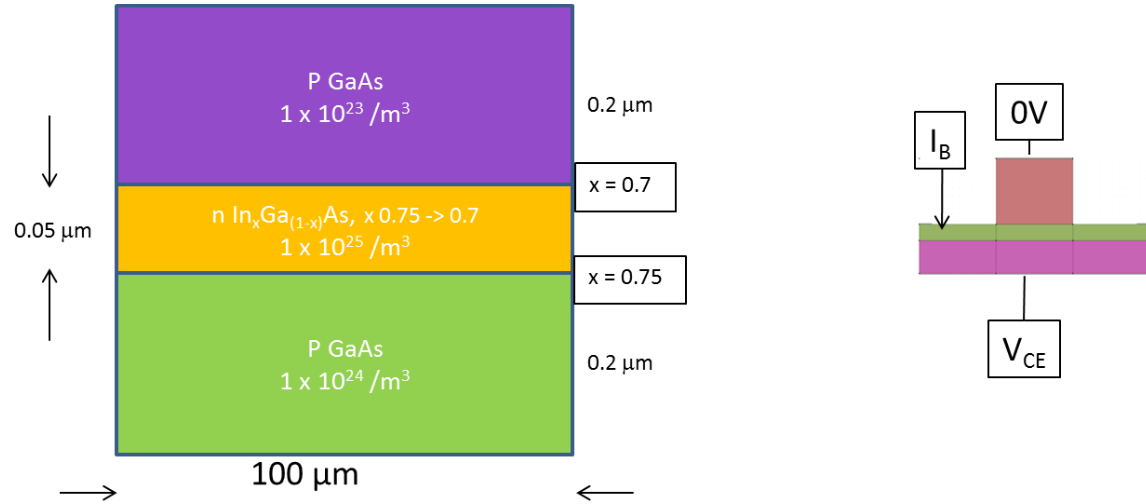


Figure 20. Bottom: Common emitter plot for PnP GaAs/$In_xGa_{(1-x)}As$/GaAs HBT with 50 nm base thickness and small base currents. The base is compositionally graded, with indium content changing linearly from 0.75 to 0.7.

Top left: Layer structure.

Top right: Biasing diagram of mesa structure.



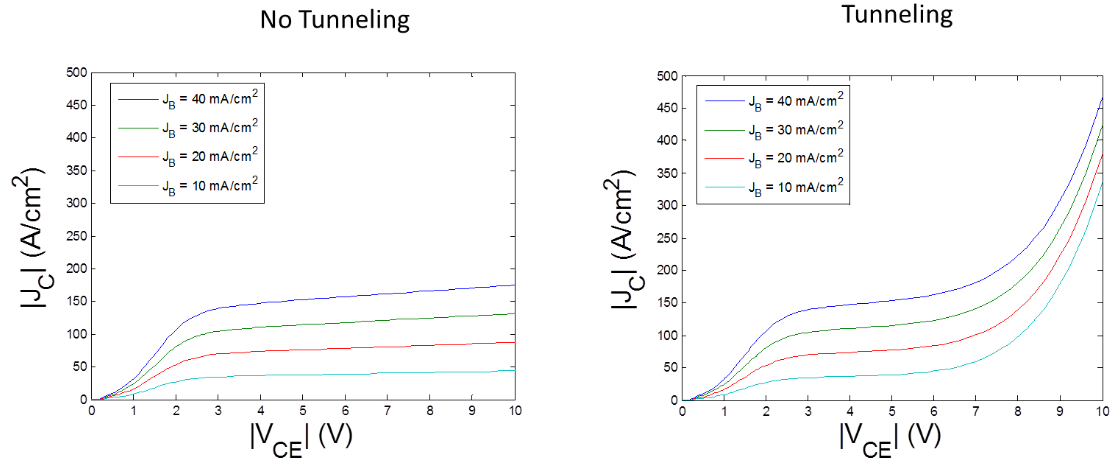


Figure 21. Bottom: Common emitter simulations with and without tunneling.

Top left: Layer structure.

Top right: Biasing diagram of mesa structure.

Table 2. Summary of results of Figure 6 to Figure 20. The device is a PnP GaAs/$In_xGa_{(1-x)}As$/GaAs HBT. The leakage current and β are measured at an emitter-collector bias of 3 V and at an emitter-base bias of 1 V.

Emitter Doping (m^{-3})	Base Doping (m^{-3})	Collector Doping (m^{-3})	Base Composition (x)	Base Thickness (μm)	Leakage Current (A/cm^2)	β
10^{24}	10^{25}	10^{23}	1	0.2	3×10^{-4}	1.4
10^{23}	10^{25}	10^{24}	1	0.2	4×10^{-3}	120
10^{23}	10^{25}	10^{24}	1	0.05	2×10^{-2}	1200
10^{23}	10^{25}	10^{24}	0.7	0.2	1×10^{-6}	106
10^{23}	10^{25}	10^{24}	0.7	0.05	1×10^{-6}	2500
10^{23}	10^{25}	10^{24}	0.75 → 0.7	0.2	1×10^{-6}	175
10^{23}	10^{25}	10^{24}	0.75 → 0.7	0.05	2×10^{-6}	3500

IV. Fabrication of GaAs/InAs Np heterojunction

A. Mesa Etch

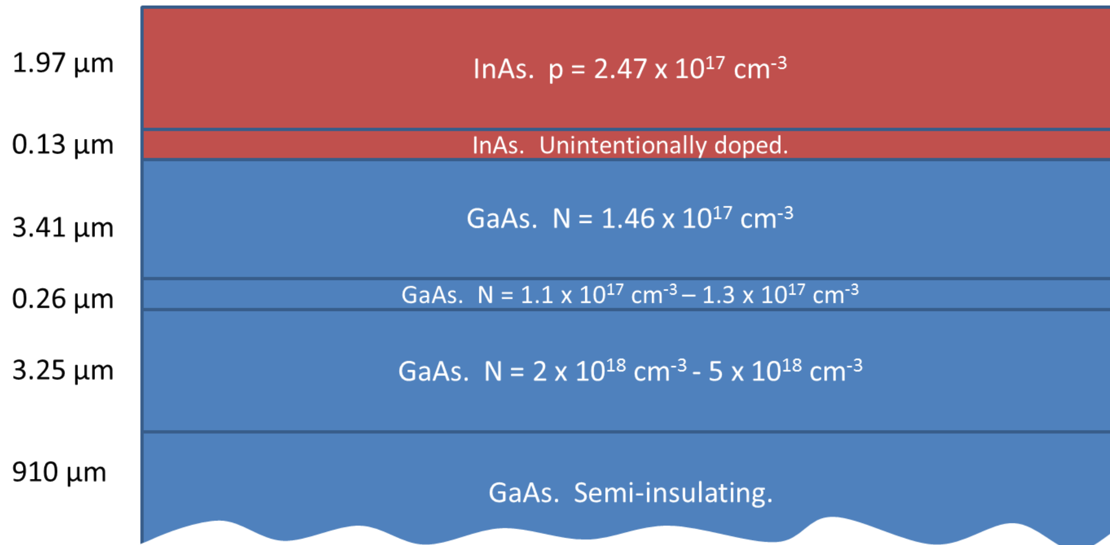


Figure 22. Layer structure for the GaAs/InAs heterojunction.

The layer structure of the GaAs/InAs heterojunction is shown in Figure 22. The sample was cleaned by sequentially soaking in acetone for 10 minutes, soaking in isopropyl alcohol for 10 minutes, soaking in a 10:1 buffered oxide etch (BOE) for three minutes, rinsing in deionized water, and dehydrating on a 124°C hotplate for 5 minutes. Next, the sample was placed on a spinner and coated with AZ9260 photoresist at 1000 rpm for 15 seconds immediately followed by 3000 rpm for 45 seconds. The sample was then placed on a 115°C hotplate for 3.5 minutes. Mesa patterns were photolithographically exposed with a mask aligner using a 301 W beam for 42 seconds. The sample was developed in a 3:1 H_2O:AZ400K solution for seven minutes. The beaker was gently agitated for the first 15 seconds and the last 45 seconds. Lastly, the sample was rinsed in deionized water and blown dry with nitrogen.

An etching solution of 1:8:80 $H_2SO_4 : H_2O_2 : H_2O$ was mixed and left to stand for 20 minutes. This allowed the solution to cool back to room temperature after initially heating because of the exothermic reaction. The etch depth was 6 μm the etch rate was 0.7 μm/min, as measured with a Dektak profilometer,

B. GaAs Metallization

The composition and thicknesses of the metal layers for the GaAs contacts are shown in Table 3 and Table 4. The layers were deposited using a Physical Vapor Deposition (Kurt Lesker PVD 250) system at a vacuum of $4 \pm 2 \times 10^{-6}$ Torr. Immediately prior to loading the chamber, the sample was immersed for 10 seconds of oxide removal in 10:1 BOE, followed by DI rinse and nitrogen blow dry. The thicknesses were monitored using the parameters shown in Table 5. After removal from the chamber, metal lift-off was commenced. The sample was soaked in acetone for 10 seconds, followed by a 10 minute soak in fresh acetone, a 10 minute soak in IPA, a DI rinse and a nitrogen blow dry. The sample was annealed at 320 °C for 5 minutes.

Table 3. Metal stack for n-type GaAs contact. Bottom row is closest to semiconductor. Version 1.

Metal	**Thickness** (Angstroms)
Ag	5000
Ni	500
Sn	2650
Ag	100
Sn	2650
Ag	100
Sn	2650

Table 4. Metal stack for n-type GaAs contact. Bottom row is closest to semiconductor. Version 2.

Metal	**Thickness** (Angstroms)
Sn	2650
Ag	100
Sn	2650
Ag	100
Sn	2650

Table 5. Parameters for monitoring thickness in PVD machine.

Metal	Density	Z-ratio
Sn	7.3	0.724
Ag	10.5	0.529
Ni	8.91	0.331
Ti	4.5	0.628
Au	19.3	0.381

C. InAs Metallization

Table 6. Metal stack for p-type InAs contact.

Metal	**Thickness** (Angstroms)
Ti	300
Au	2000

The same cleaning and photo-processing procedures for the mesa etch were repeated prior to the InAs metallization of Table 6. To lift off the metal, the sample was soaked in still acetone for 20 seconds, placed in an ultra-sonic bath for 10 seconds, and soaked in acetone for another 5 minutes (no ultra-sonic agitation). Finally, it was soaked in IPA for 5 minutes, DI rinsed and blown dry with nitrogen. An image of a processed diode is shown in Figure 23.

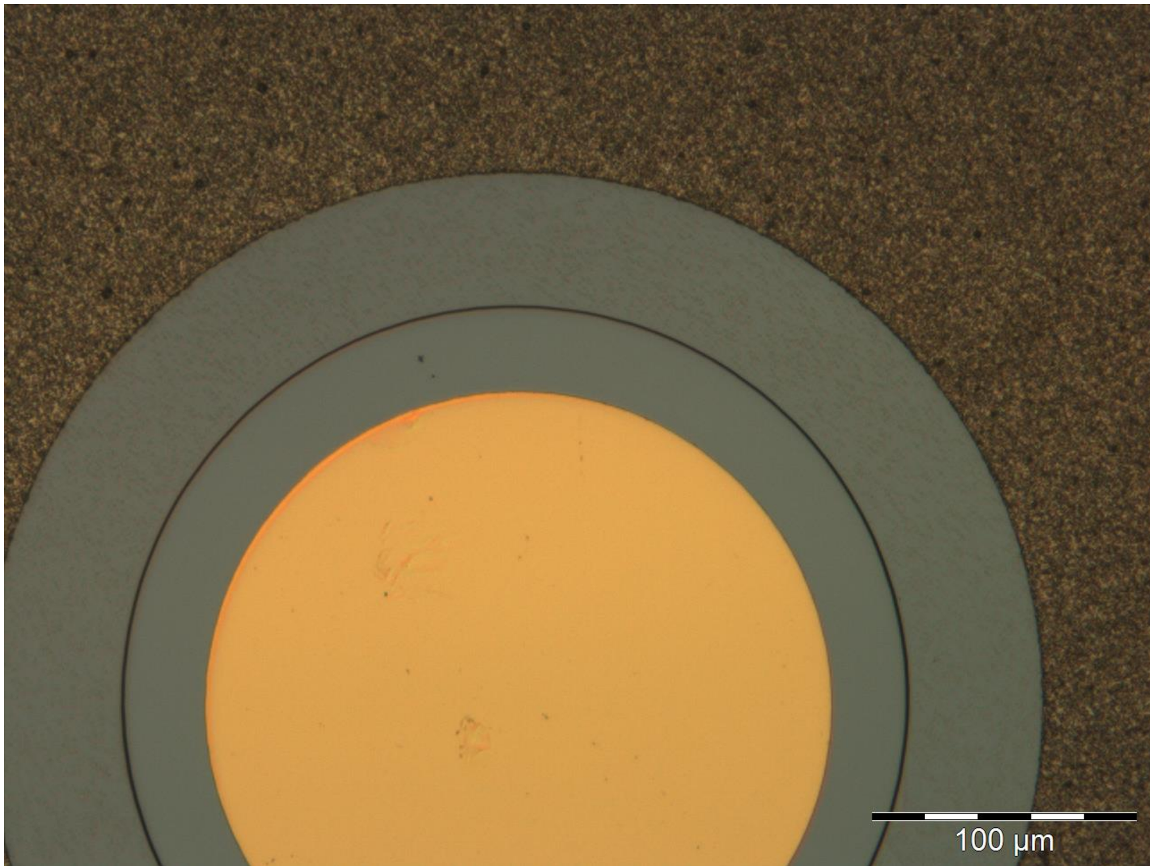


Figure 23. Nomarski micrograph of a processed InAs-GaAs mesa diode. Moving outward in concentric circles of increasing size: the Au/Ti contact on top of p-InAs, the non-etched mesa surface, the non-

metallized GaAs(N^+) surface expose by the mesa etch, and the Ag/Ni/Sn/Ag/Sn/Ag/Sn contact on top of n-GaAs.

V. Fabrication of GaAs/InAs/InAs Npn transistor structure

The process flow for the GaAs/InAs/InAs transistor is quite similar to the process flow for the diode described in section 0. Instead of one etch and two metallizations, there were two etches and one metallization. The two etches created an emitter-base double mesa (Figure 24). For simplicity, a single metallization (Ti/Au) was use for all three contacts, and annealing was not carried out. Nomarski micrographs of the finished devices are shown in Figure 26 and Figure 27. The surface roughness apparent in Figure 24 and Figure 25 is most likely a growth related issue caused by the 7% lattice constant mismatch between InAs and GaAs.

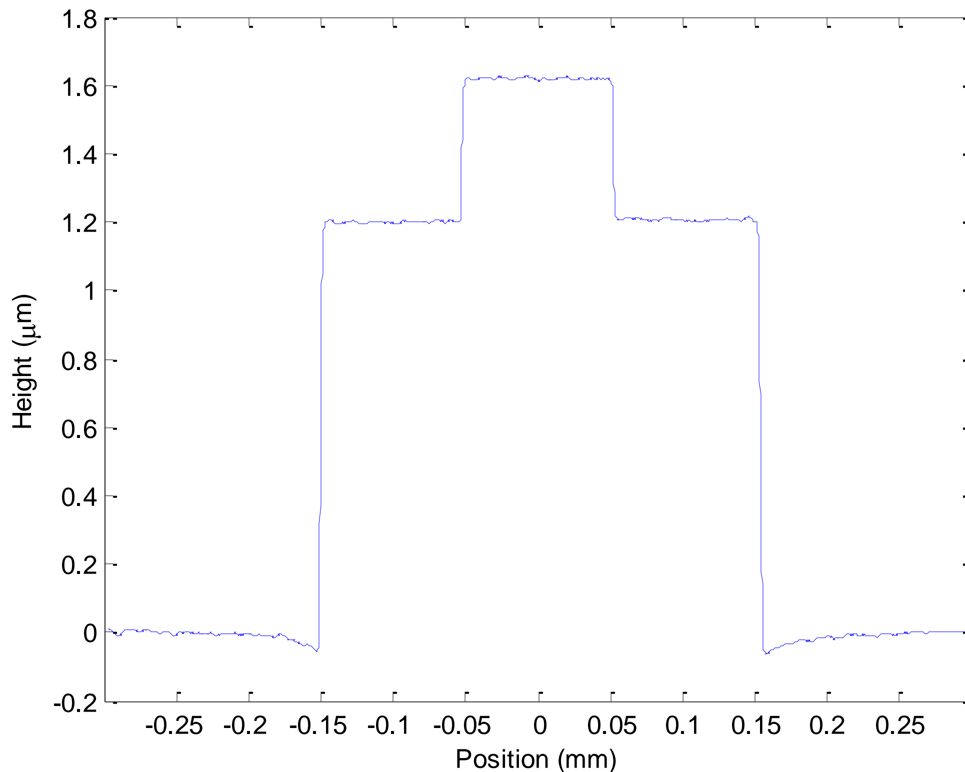


Figure 24. Dektak Profilometer scan of double mesa HBT after second etch.

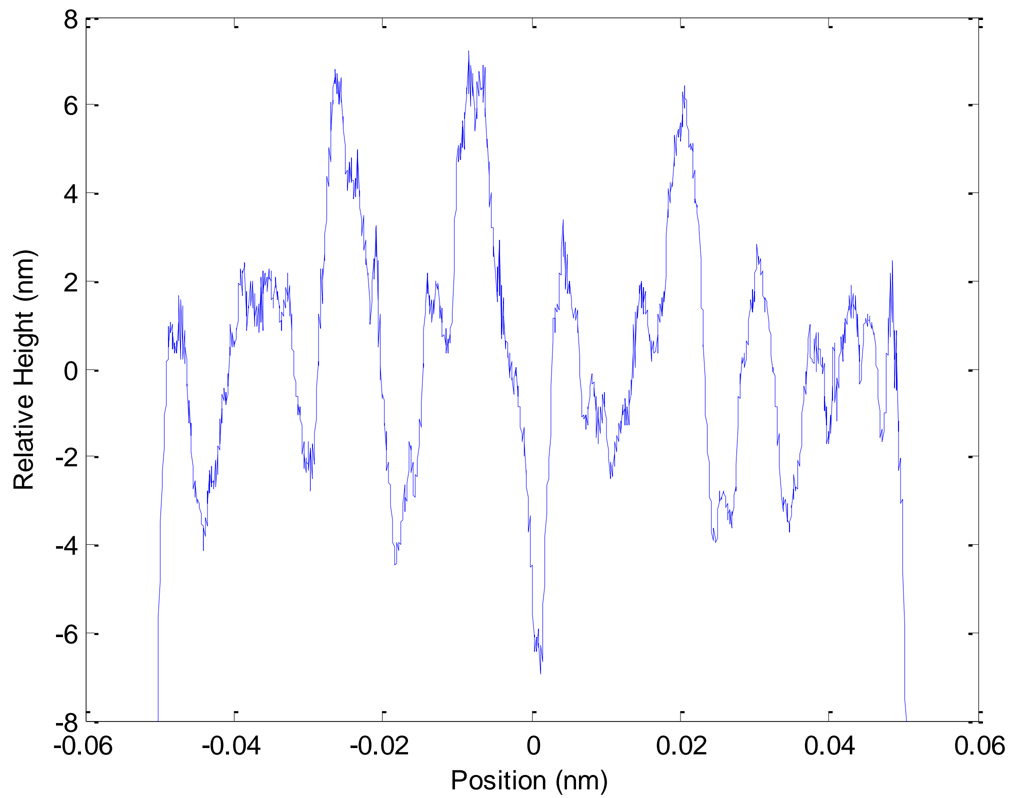


Figure 25. Detail of Figure 24 showing surface roughness of emitter.

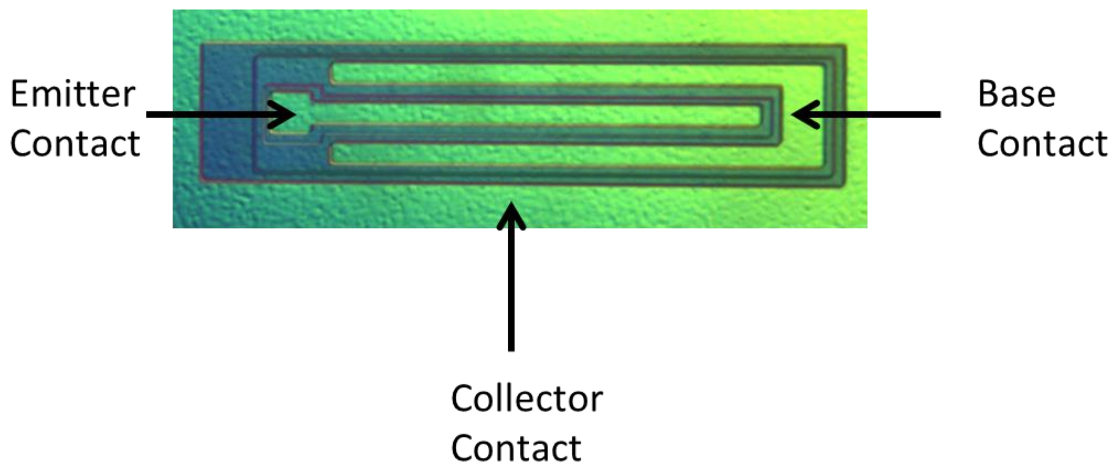


Figure 26. Nomarski micrograph of InAs/InAs/GaAs single heterojunction bipolar transistor. The coloring is false.

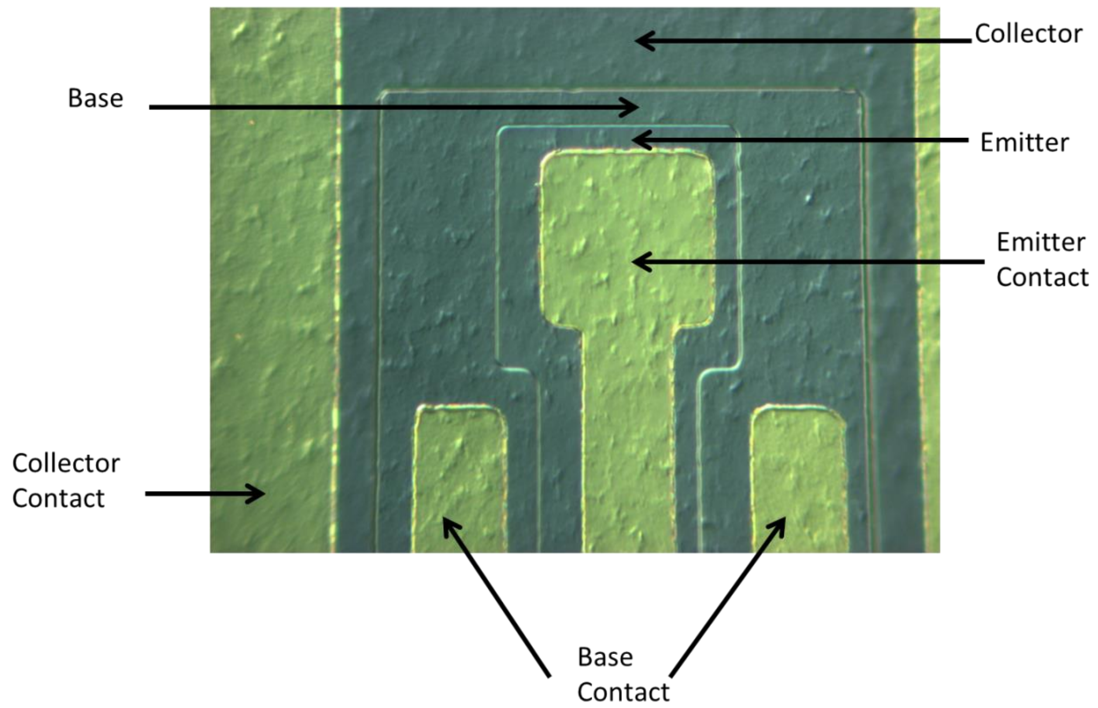


Figure 27. Nomarski micrograph of detail of InAs/InAs/GaAs single heterojunction bipolar transistor. The width of each base contact is 20 microns. Surface roughness is apparent. The coloring is false.

VI. Characterization of GaAs/InAs Np junction

The measured current-voltage plots of three devices are shown in Figure 28. The current has been divided by the mesa area to obtain the current density. The experimental data is fit to a generalized diode equation (1.8) in Figure 29, giving J_0(reverse) = 7 x 10^{-6} A/cm^2 and n(reverse) = 3.17. J_0 (forward) = 1.6 x 10^{-5} A/cm^2 and n(forward) = 1.26.

$$J = \begin{cases} J_0(\text{reverse})e^{q|V|/n(\text{reverse})kT} & \text{for V} < 0 \\ J_0(\text{forward})e^{q|V|/n(\text{forward})kT} & \text{for V} > 0 \end{cases} \quad (1.8)$$

In the forward current, this corresponds to a mix of diffusion current (n=1) and recombination current (n=2). The reverse current is extremely non-ideal, probably caused by the high dislocation density at the heterojunction. Although there is not a clear physical interpretation for it, we may fit the reverse current to an exponential, obtaining J_0 = 7 x 10^{-6} A/cm^2 and n(reverse) = 3.17. This corresponds to two opposite polarity diodes in parallel, one with an ideality factor of 1.26 and the other with an ideality factor of 3.17. This could be caused by an opposite polarity, non-ideal junction at the sidewalls of the mesa. Various groups have studied anomalous IV diode characteristics by going beyond SRH theory [15, 16] . Schenk and Krumbein have modeled anomalous behavior in silicon diodes by generalizing the SRH theory to include more than one trap level [17]. If there is coupling between traps, or direct tunneling between donor and acceptor levels, the ideality factor can be greater than 3; however, it is forward bias-dependent and drops below 2 above 0.5 volts. The authors do not treat reverse bias; hence, there is no direct connection to the behavior observed here.

The metal stack of Table 4 has a composition of 96.2 atomic % tin and 3.8 atomic % silver, corresponding to the eutectic point of the phase diagram in Figure 32, the minimum melting point for the tin-silver alloy. A lower melting point allows for a lower annealing temperature, reducing the damage to the InAs layer. The tin-silver alloy turns into whisker shaped patches after annealing. To compensate for this, extra layers (Table 3) are added. Nickel is supposed to act as a barrier to diffusion of the thick silver layer to the eutectic stack. The top silver layer, with its melting point far above the annealing temperature, is supposed to create a rugged and contiguous surface for probing.

However, in actual fact, the nickel layer may be too thin to prevent the top silver layer from diffusing into the rest of the stack. This would raise the melting point above the annealing temperature and increase contact resistance. This explanation is consistent with Figure 30 and Figure 31. In Figure 30 the exponential behavior ceases at high currents due to ohmic contributions, which are more deleterious for the Ag /Ni/ Sn/Ag/Sn/Ag/Sn stack. Likewise, in Figure 31, the cell-to-cell resistance (see caption for details) is higher for the Ag /Ni/ Sn/Ag/Sn/Ag/Sn stack.

A series of JV curves measured at different temperatures is shown in Figure 33. Counterintuitively, at small voltages and at low temperatures, the resistance is larger in forward bias than in reverse bias. Figure 34 shows this more clearly by plotting the current density against inverse temperature. In Figure 34a, the high temperature data is fit to

$$J = J_0 e^{-E_{\text{activation}}/kT}, \qquad (1.9)$$

where $E_{\text{activation}}$ is the energy barrier over which a thermally excited carrier will pass. $E_{\text{activation}}$ is 0.6 eV.

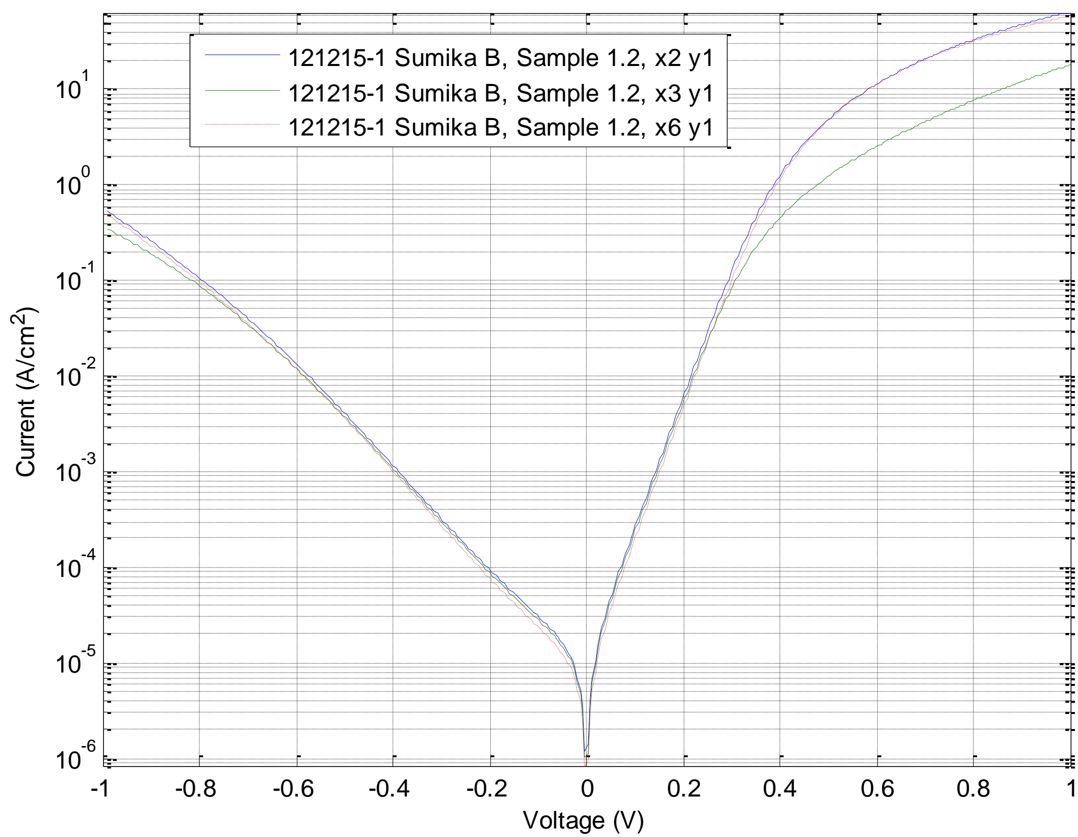


Figure 28. JV curves of GaAs-InAs heterojunction. GaAs is nominally n-doped at 1.2×10^{17} cm^{-3} and InAs is nominally p-doped at 2.5×10^{17} cm^{-3}.

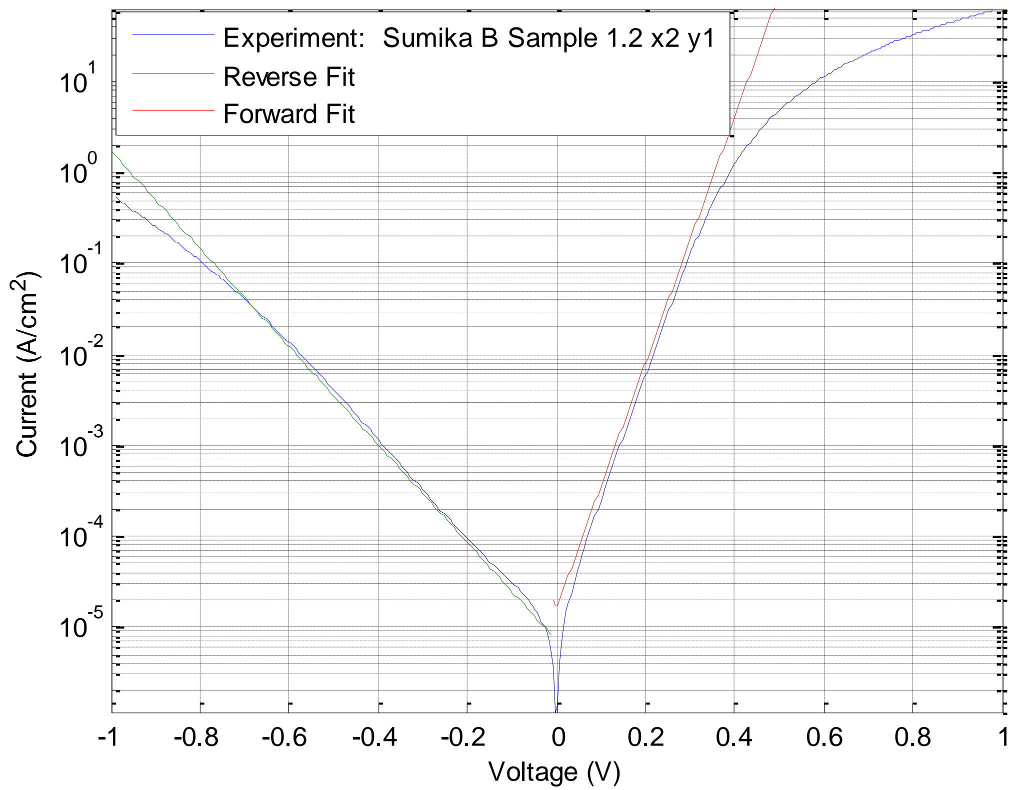


Figure 29. JV curves of GaAs-InAs heterojunction. GaAs is nominally n-doped at 1.2 x 10^{17} cm^{-3} and InAs is nominally p-doped at 2.5 x 10^{17} cm^{-3}. The fit is piecewise exponential, $J = J_0 e^{q|V|/nkT}$. J_0(reverse) = 7 x 10^{-6} A/cm^2 n(reverse) = 3.17. J_0 (forward) = 1.6 x 10^{-5} A/cm^2. n(forward) = 1.26.

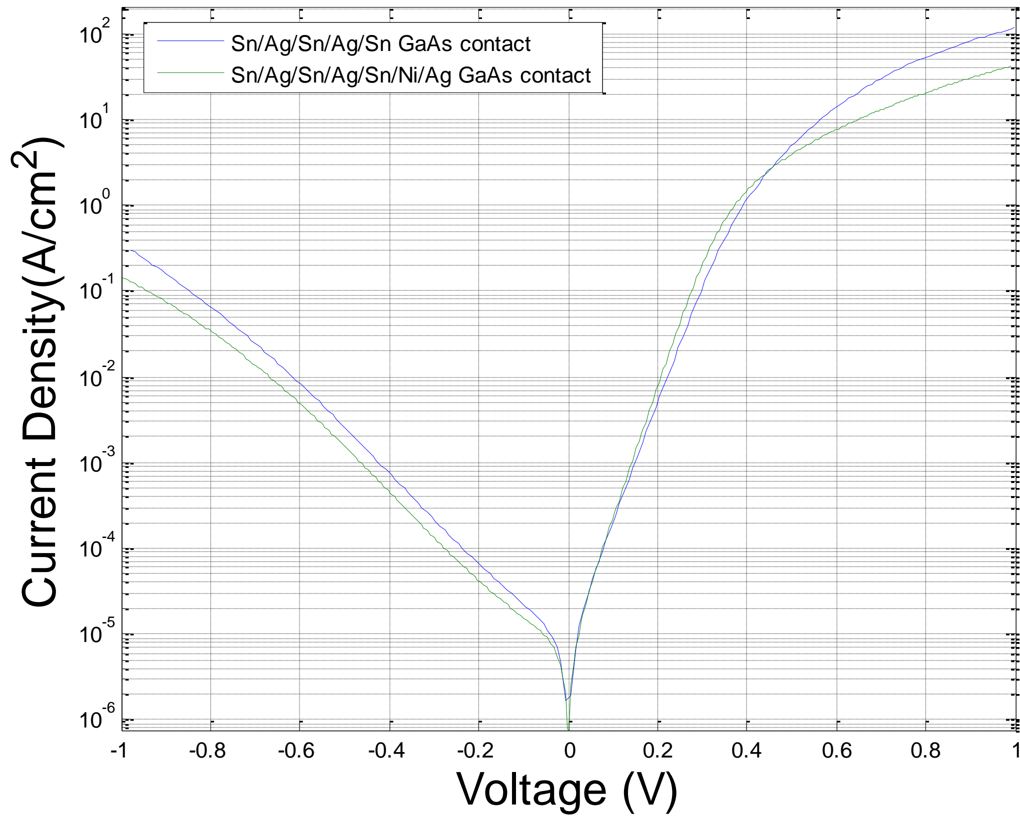


Figure 30. JV curves of GaAs-InAs heterojunction, with different metal contacts to the GaAs layer. GaAs is nominally n-doped at 1.2 x 10^{17} cm^{-3} and InAs is nominally p-doped at 2.5 x 10^{17} cm^{-3}. The samples come from the same wafer, but the blue curve was measured four months after the green curve.

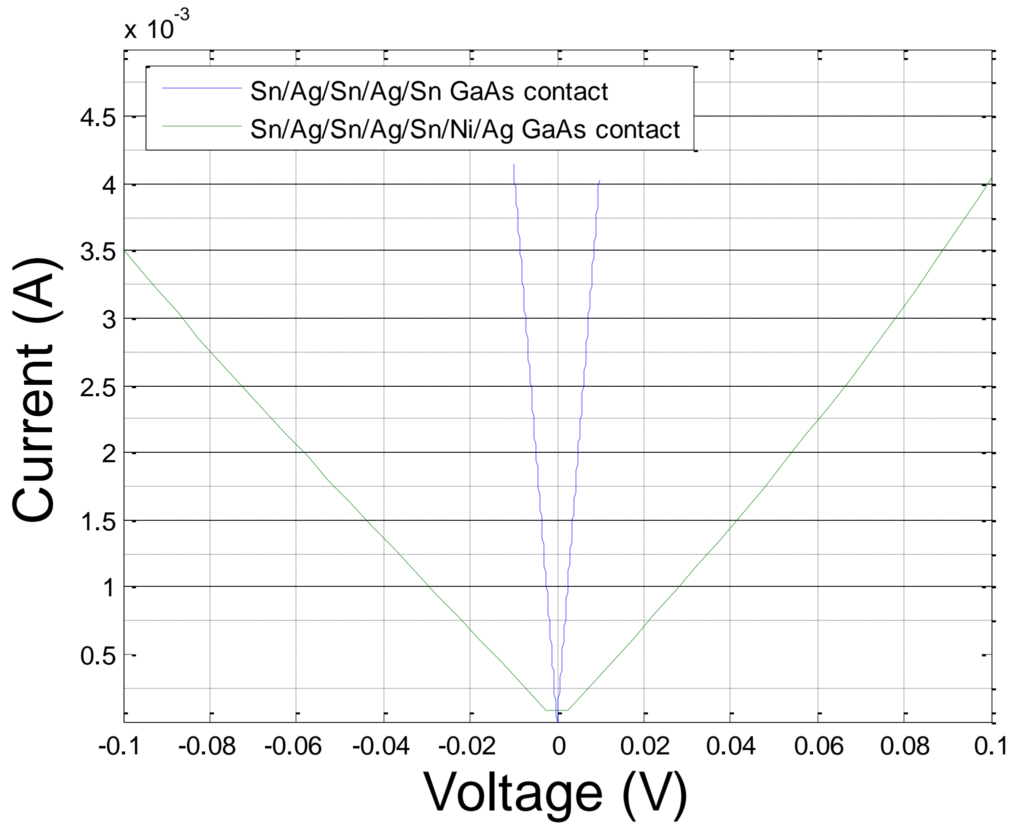


Figure 31. Superposed I-V curves demonstrate the influence of metal stack composition upon contact resistance. The probes are placed on adjacent device unit cells, causing the current to flow from metal of one cell through the semiconductor and back through the metal of the adjacent cell. Compared with the Sn/Ag/Sn/Ag/Sn stack, the Ag /Ni/ Sn/Ag/Sn/Ag/Sn stack is less linear and less conductive. In other words, the Sn/Ag/Sn/Ag/Sn stack provides a better ohmic contact.

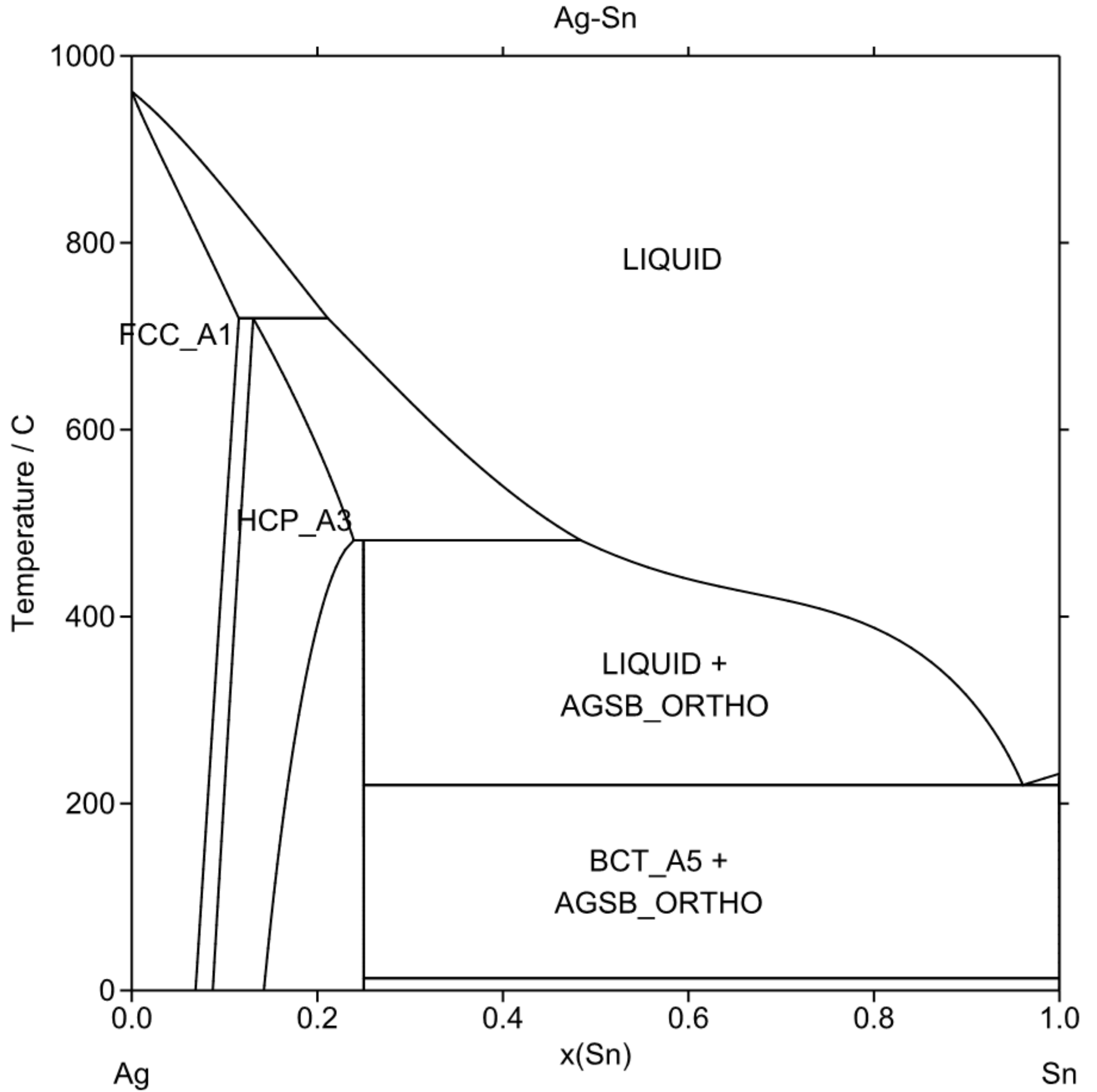


Figure 32. Phase diagram of tin-silver alloy. The eutectic point has 96.2 atomic % tin. [18]

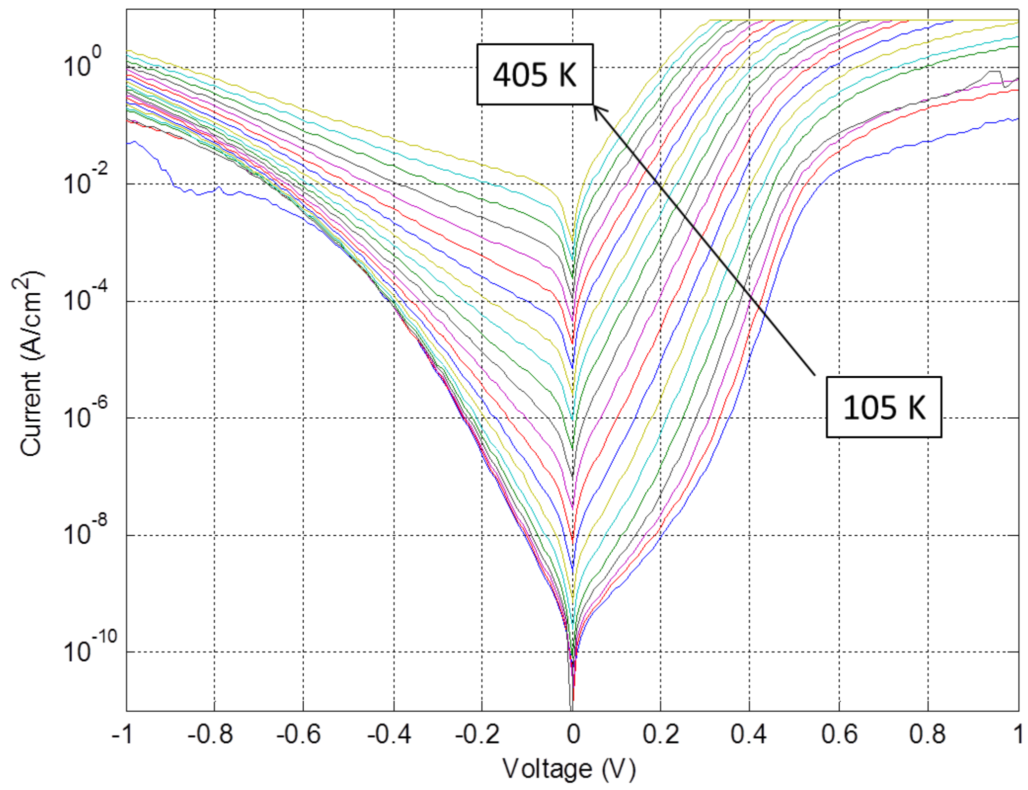
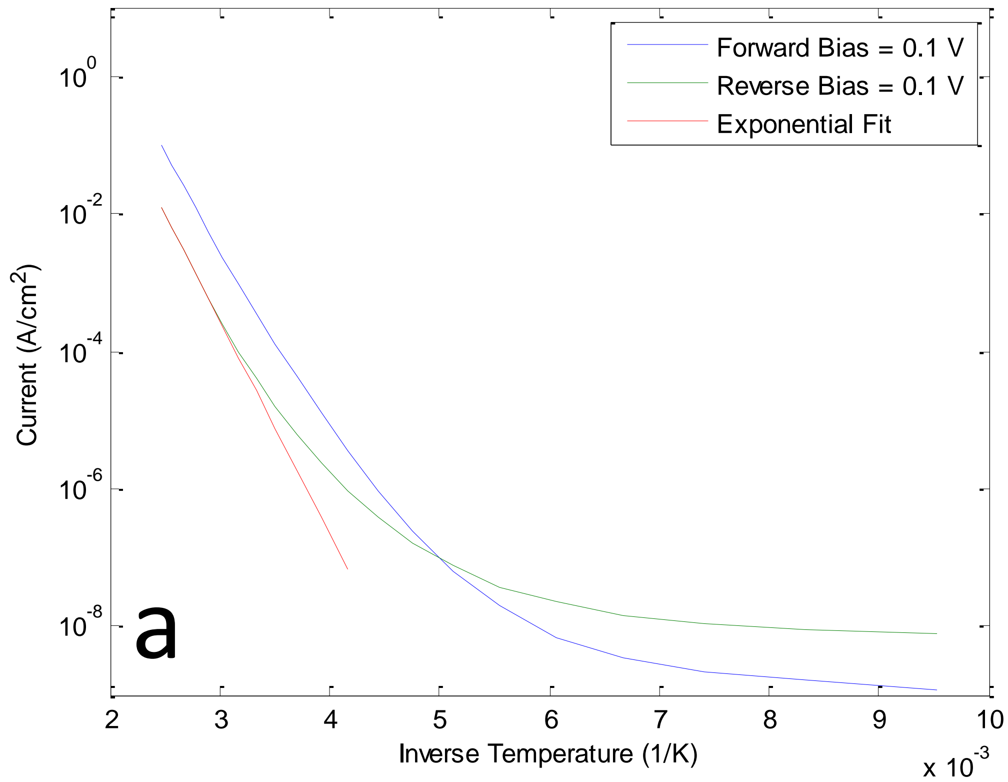
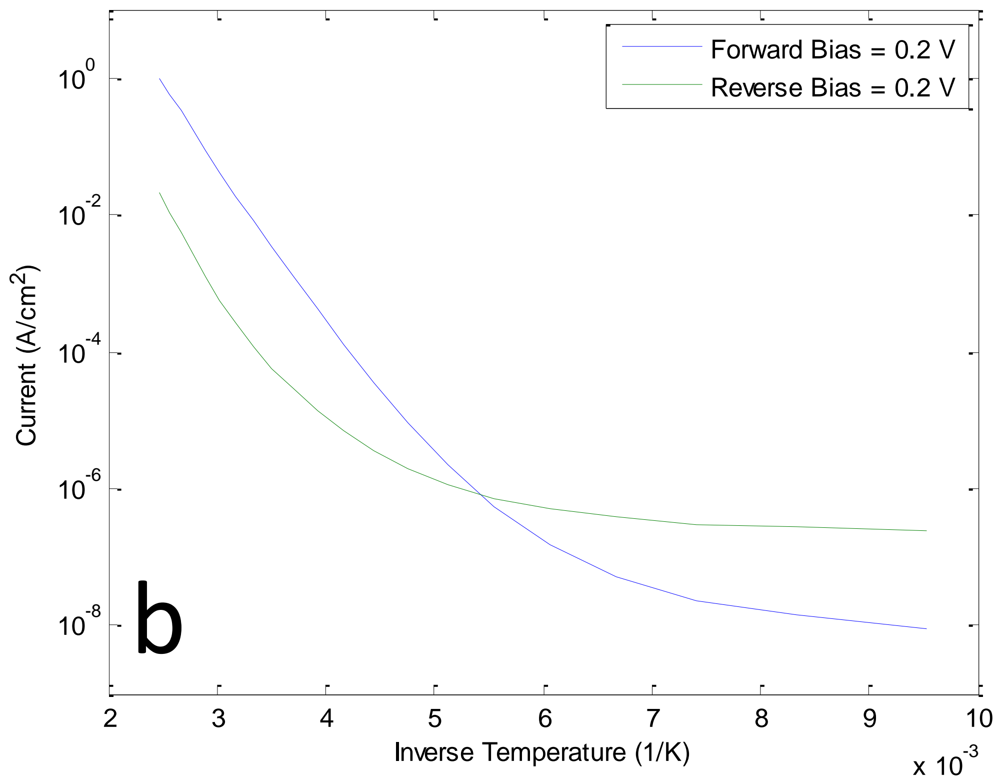


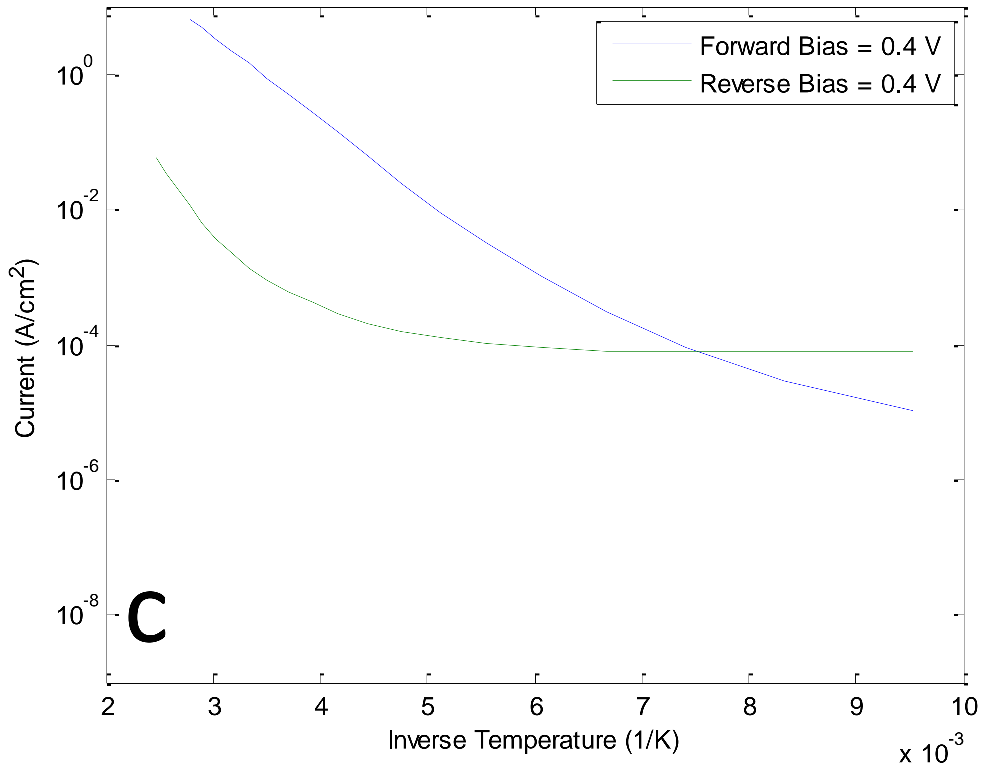
Figure 33. JV curves of GaAs-InAs heterojunction. GaAs is n-doped at 1.2 x 10^{17} cm^{-3} and InAs is p-doped at 2.5 x 10^{17} cm^{-3}. The temperature increment is 15 K.



Forward Bias = 0.1 V
Reverse Bias = 0.1 V
Exponential Fit
Current (A/cm^2)
10^0
10^{-2}
10^{-4}
10^{-6}
10^{-8}
a
2 3 4 5 6 7 8 9 10
Inverse Temperature (1/K)
x 10^{-3}



Forward Bias = 0.2 V
Reverse Bias = 0.2 V
Current (A/cm^2)
10^0
10^{-2}
10^{-4}
10^{-6}
10^{-8}
b
2 3 4 5 6 7 8 9 10
Inverse Temperature (1/K)
x 10^{-3}


Forward Bias = 0.4 V
Reverse Bias = 0.4 V
Current (A/cm^2)
10^0
10^{-2}
10^{-4}
10^{-6}
10^{-8}
C
2 3 4 5 6 7 8 9 10
Inverse Temperature (1/K)
x 10^{-3}

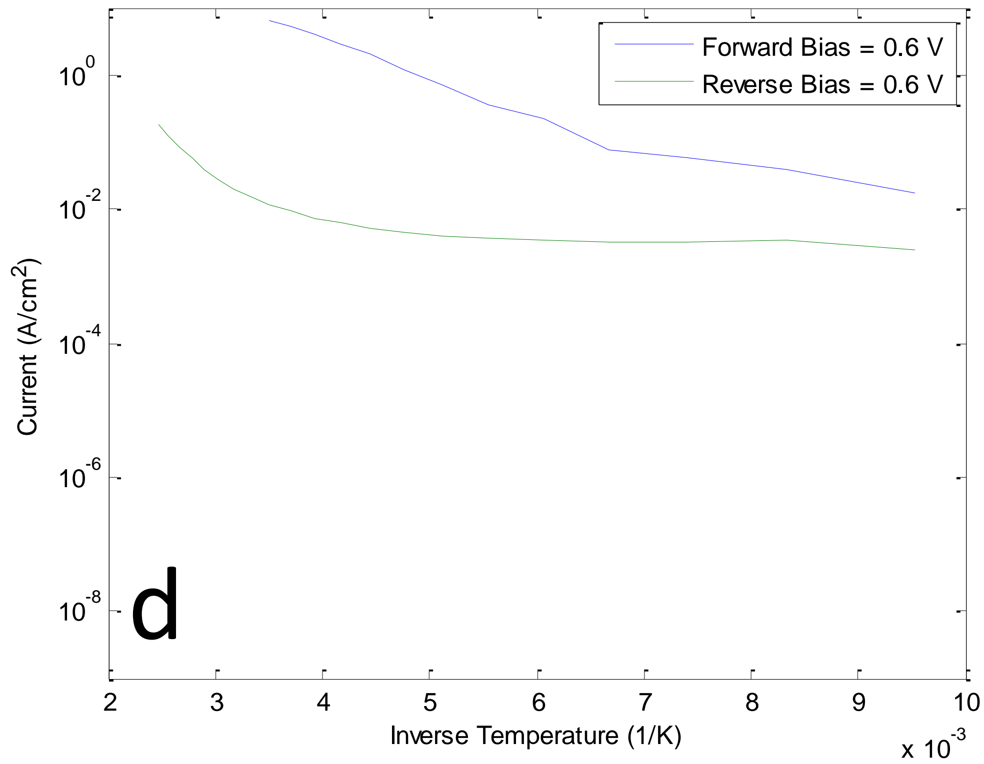


Figure 34. . GaAs-InAs heterojunction current density plotted against inverse temperature. GaAs is n-doped at 1.2 x 10^{17} cm^{-3} and InAs is p-doped at 2.5 x 10^{17} cm^{-3}. a) 0.1 V bias, with high temperature exponential fit. b) 0.2 V bias. c) 0.4 V bias. d) 0.6 V bias.

VII. Characterization of GaAs homojunction

Current-voltage characteristics of a GaAs homojunction are shown in Figure 35 and Figure 36. Because it is a homojunction and there is no lattice mismatch, there are far fewer defects than in the GaAs/InAs heterojunction of section 0. The reverse leakage current increases much less dramatically with increasingly negative bias in the homojunction case compared to the heterojunction case. The "on-off" ratio of current between +1 V and -1 V is more than 9 orders of magnitude. In the mismatched GaAs/InAs heterojunction of Figure 29, the ratio is less than three orders of magnitude. The ideality factor changes from $n \approx 2$ to $n \approx 1$ at about 0.8 V in Figure 36. The fall-off in the slope of the current due to ohmic contact resistance occurs at about 1 V. The ideality factor as a function of voltage is plotted in Figure 37, where we have used

$$n = \frac{qI}{kT \frac{dI}{dV}} \qquad (1.10)$$

(1.10) follows from (1.8).

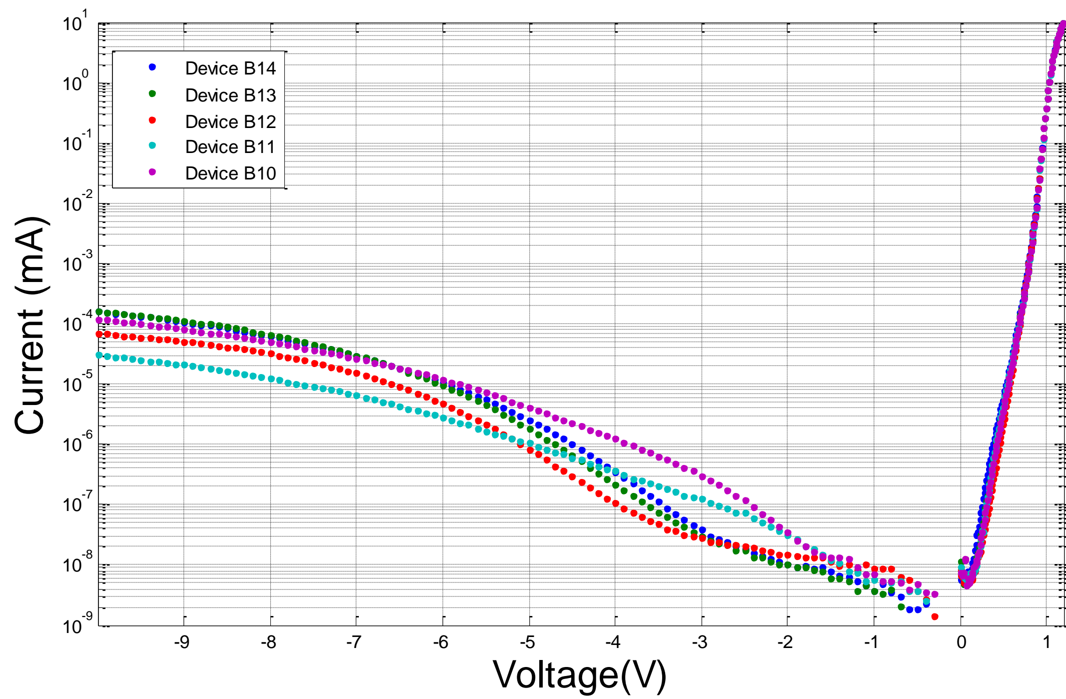


Figure 35. IV curves of GaAs homojunction, with non-annealed Ti/Au metal contacts. The p-side is doped at 2.8 x 10^{18} cm^{-3}, and the n-side is doped at 3.5 x 10^{17} cm^{-3}. The device area is 4.125 x 10^{-3} cm^2.

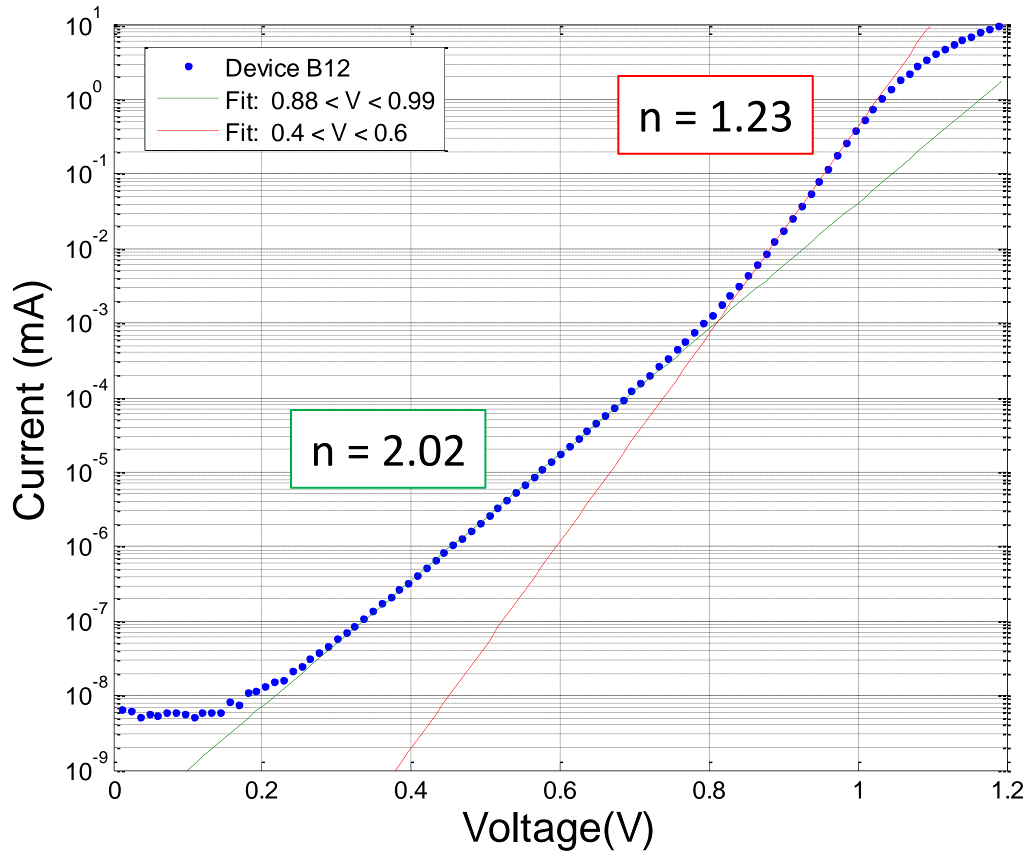


Figure 36. IV curve of GaAs homojunction, with non-annealed Ti/Au metal contacts. The p-side is doped at 2.8 x 10^{18} cm^{-3}, and the n-side is doped at 3.5 x 10^{17} cm^{-3}. The device area is 4.125 x 10^{-3} cm^{2}. The shift of the current minimum away from V=0 is due to ambient light during the measurement. The exponential fit for the voltage range of 0.4 V to 0.6 V gives an ideality factor, n = 2.02. . The exponential fit for the voltage range of 0.88 V to 0.99 V gives an ideality factor, n = 1.23.

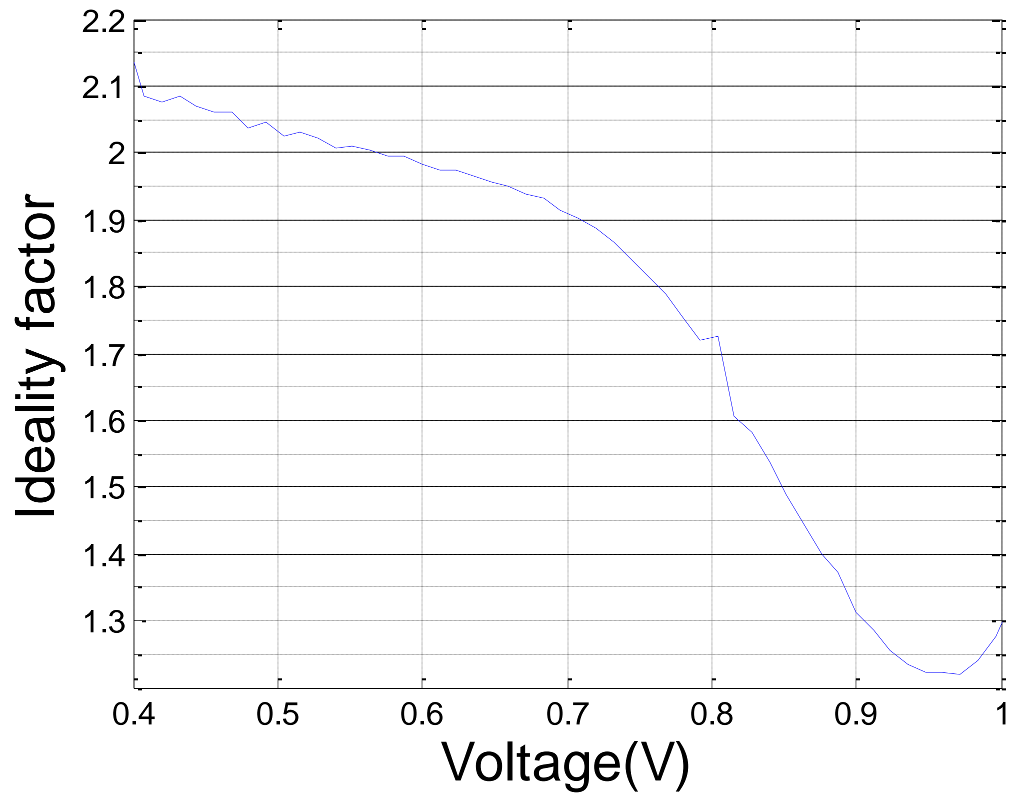


Figure 37. Ideality factor (n) as a function of voltage. The plot is derived from Figure 36 by taking the derivative (dI/dV) and using the expression n = qI/(kT(dI/dV)).

VIII. Characterization of GaAs/InAs/InAs Npn transistor structure

The current-voltage plots of the base-emitter homojunction are shown in Figure 38 and in Figure 39. None of the devices show the expected diode behavior of (1.8), although the devices of Figure 39 show mild rectification. On the other hand, the base-collector heterojunction shows reasonable rectification (Figure 40 and Figure 41).

With a fixed base current, the collector-emitter bias is swept in the common emitter configuration (Figure 42 - Figure 44). Not only is the dI_c/dI_b negligible, it has the wrong sign. Increasing the base current *decreases* the collector current. The small *magnitude* of dI_c/dI_b may be understood with reference to Figure 39, in which the emitter-base junction is not behaving as a diode and thus is not able to modulate the collector current. The *sign* of dI_c/dI_b may be understood with reference to Figure 41 in which the leakage current increases with negative bias. An increase in I_b is accompanied by an increase in $V_{b,}$ decreasing V_{cb} and thus decreasing $I_{c.}$ In addition, even had both junctions been working, the device would not work as a transistor according to simulations of section 0.

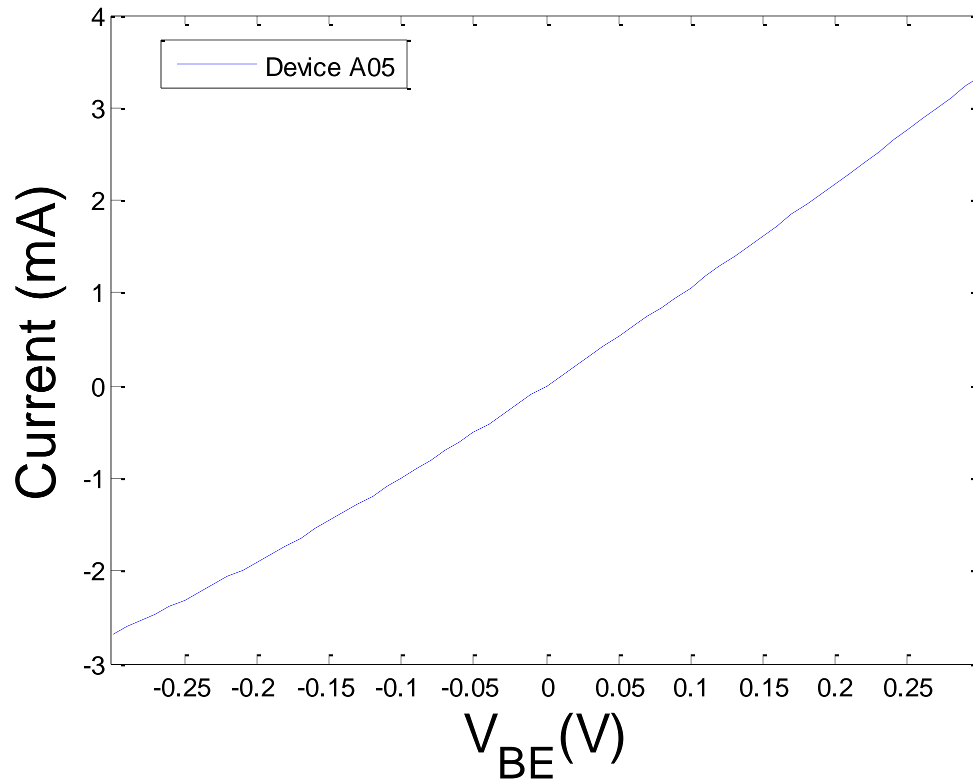


Figure 38. Base-Emitter junction. Emitter mesa area = 1.475 x 10^{-3} cm^2. Base mesa area = 4.125 x 10^{-3} cm^2. InAs base is nominally p-doped at 5 x 10^{18} cm^{-3} and InAs emitter is nominally n-doped at 4.9 x 10^{17} cm^{-3}.

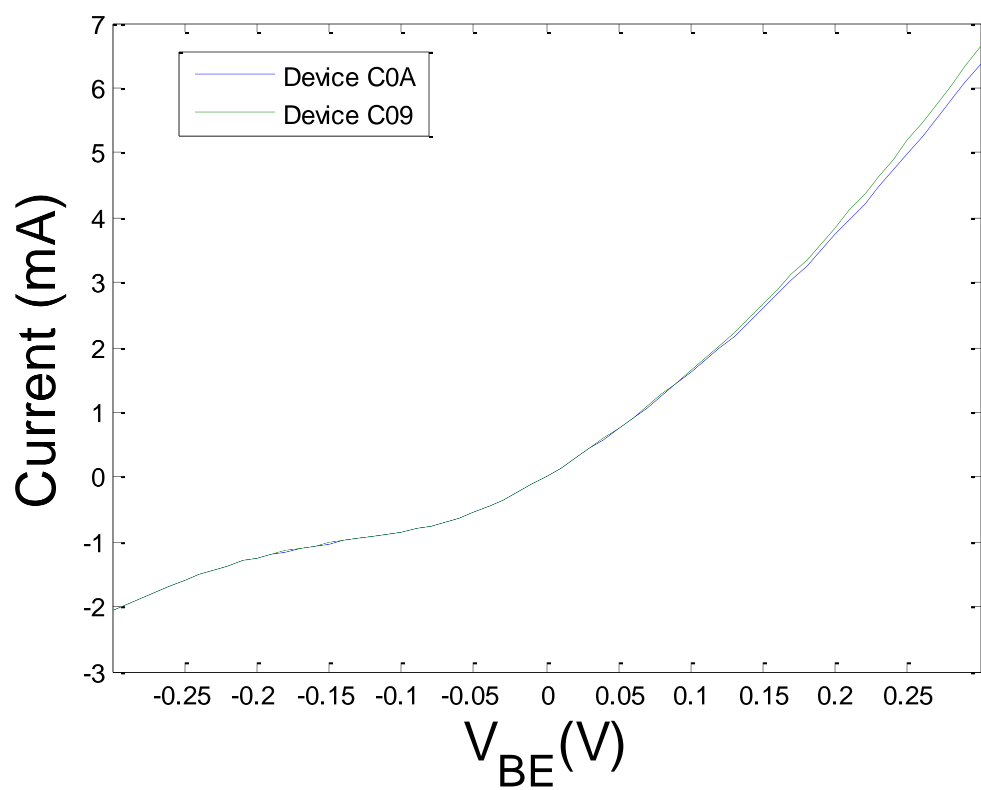


Figure 39. Base-Emitter junction. Emitter mesa area = 2.96 x 10^{-4} cm^2. Base mesa area = 9.64 x 10^{-4} cm^2. InAs base is nominally p-doped at 5 x 10^{18} cm^{-3} and InAs emitter is nominally n-doped at 4.9 x 10^{17} cm^{-3}.

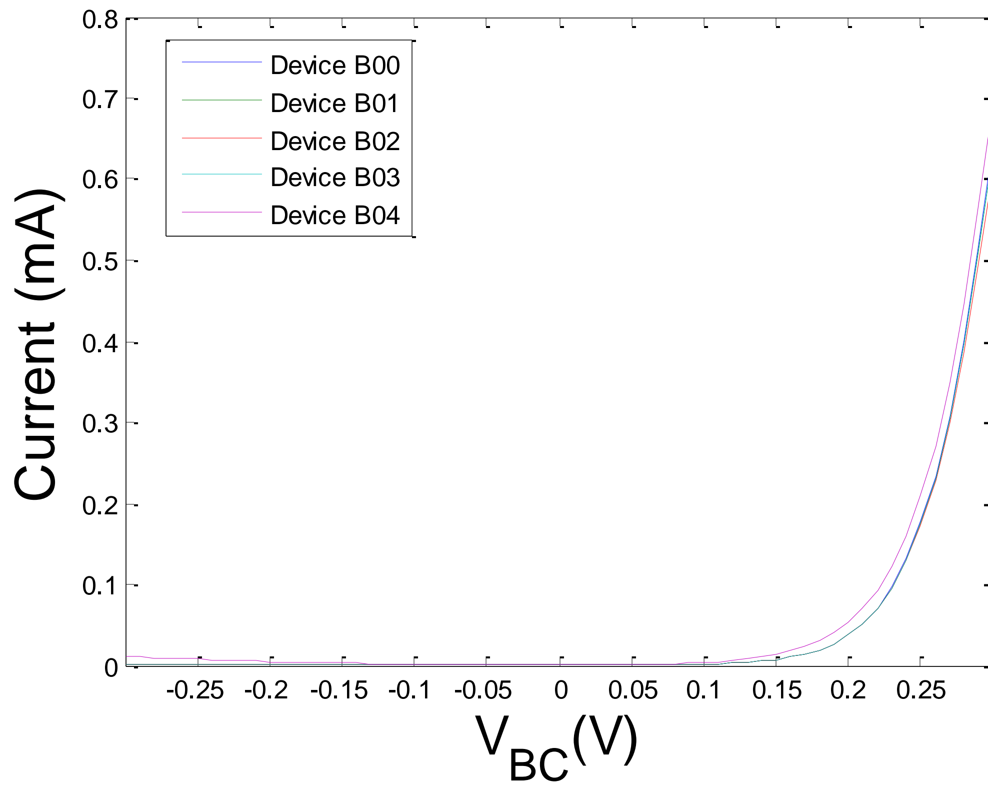


Figure 40. Base-Collector junction. Base mesa area = 4.125 x 10^{-3} cm^2. InAs base is nominally p-doped at 5 x 10^{18} cm^{-3} and InAs collector is nominally n-doped at 3 x 10^{17} cm^{-3}. Linear scale.

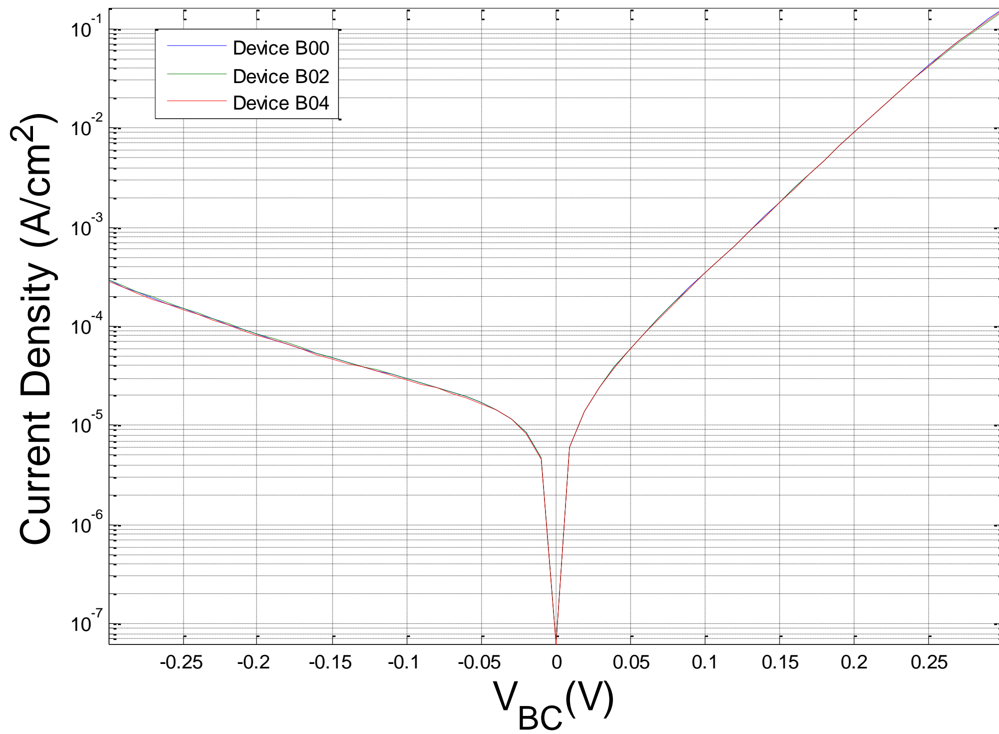


Figure 41. Base-Collector junction. Base mesa area = 4.125 x 10^{-3} cm^2. InAs base is nominally p-doped at 5 x 10^{18} cm^{-3} and InAs collector is nominally n-doped at 3 x 10^{17} cm^{-3}. Semilog scale. Unlike the previous graphs, *current density* rather than *current* is plotted. This plot is in rough agreement (over a smaller voltage range) with Figure 28, even though the doping profile is not the same.

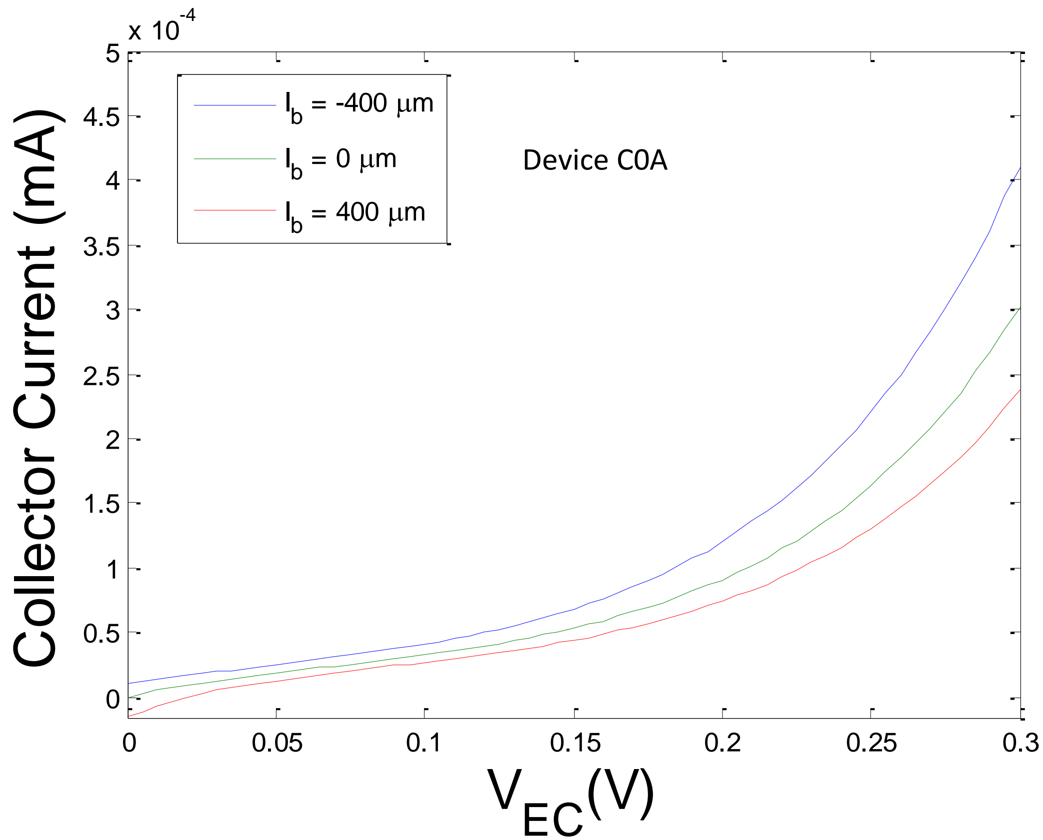


Figure 42. Common emitter measurements for GaAs/InAs/InAs HBT structure. Changing the base current has very little effect on the collector current, and the polarity is wrong. In a working HBT, the collector current should be much larger than the base current, but here the opposite is true. This device does not work.

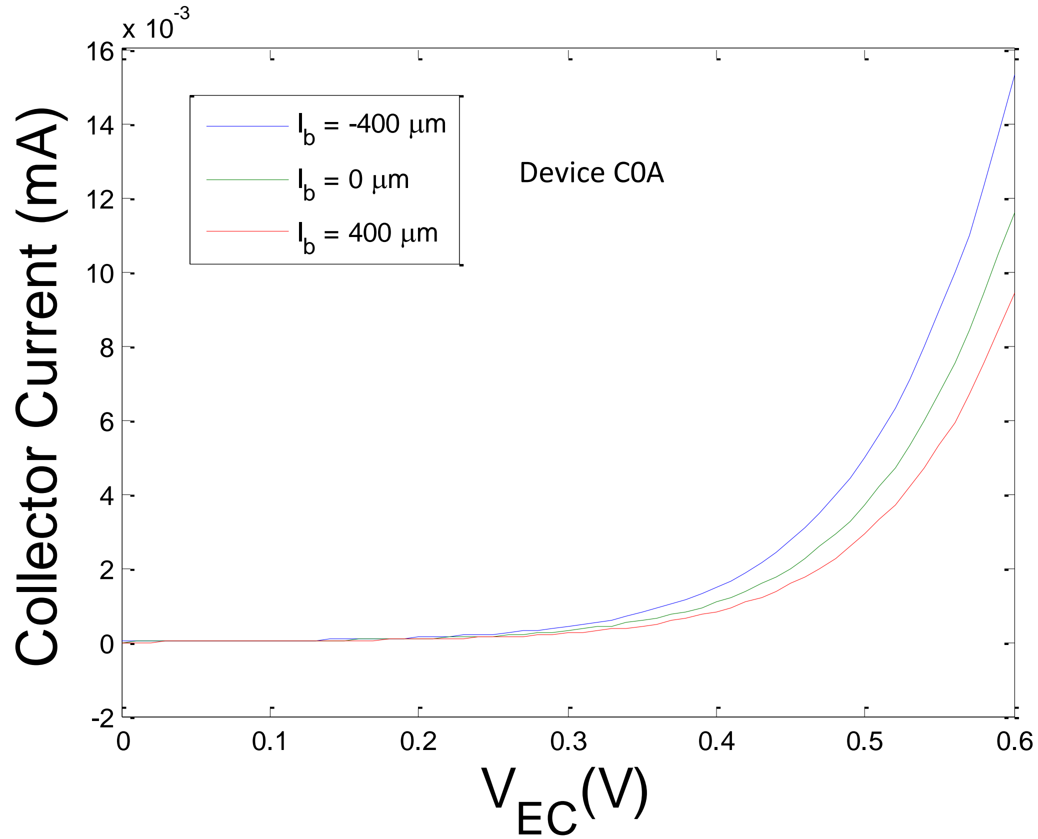


Figure 43. The same device as in Figure 42, with the bias range doubled. The collector current is still much less than the base current. This device does not work.

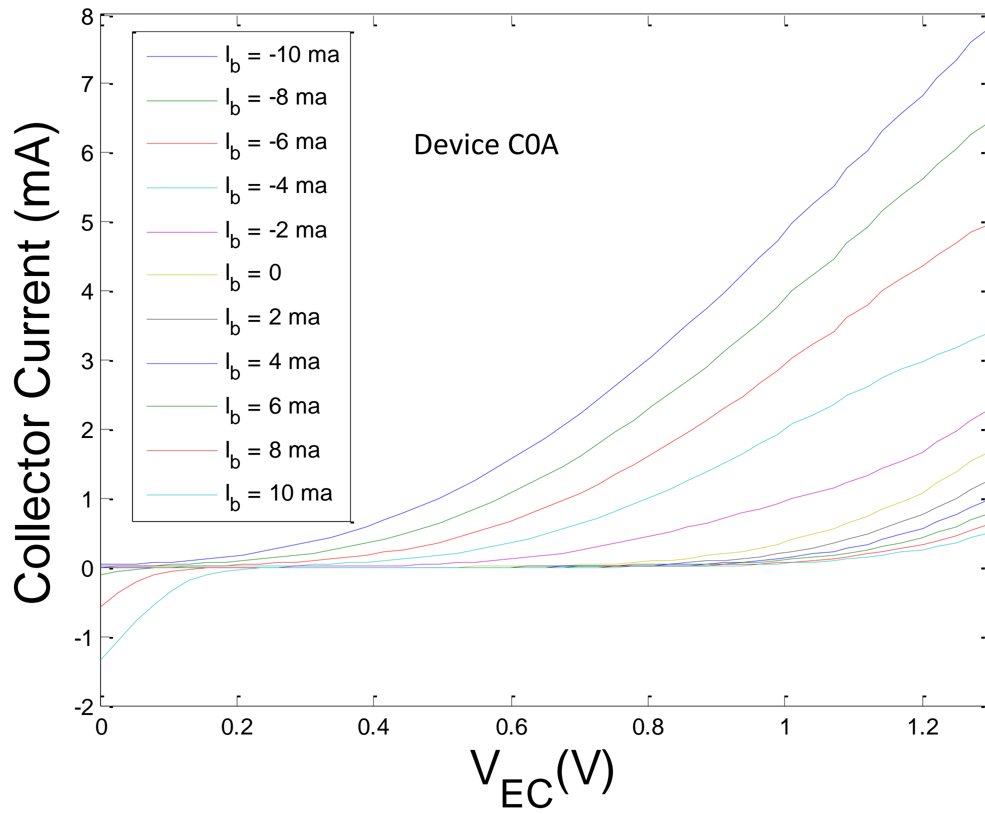


Figure 44. The same device as in Figure 42 with both the bias range and the base current increased. The collector current is still less than the base current. Injecting current into the base (positive valued I_b) decreases the collector current from its leakage level. This device does not work.

IX. Analysis of Npn GaAs/InAs/InAs HBT structure

Before analyzing the experimental data, we will look at simulations of the device structure. It will be seen that this design does not work. In the rightmost band diagram of the bottom row of Figure 45, a large base emitter bias relative to the InAs bandgap is not sufficient to turn the device on. In order for the collector current to flow freely, there should be a non-negative slope of the conduction band edge (red line), from the collector to the emitter. This is not the case in the simulation. The "spike" at the collector-base boundary, as well as the remanent built-in at the base-emitter boundary, will both impede electron flow. The Gummel plot is shown n Figure 46. The common emitter plot of Figure 47 shows that the base current has no significant influence on the collector current. This design does not work.

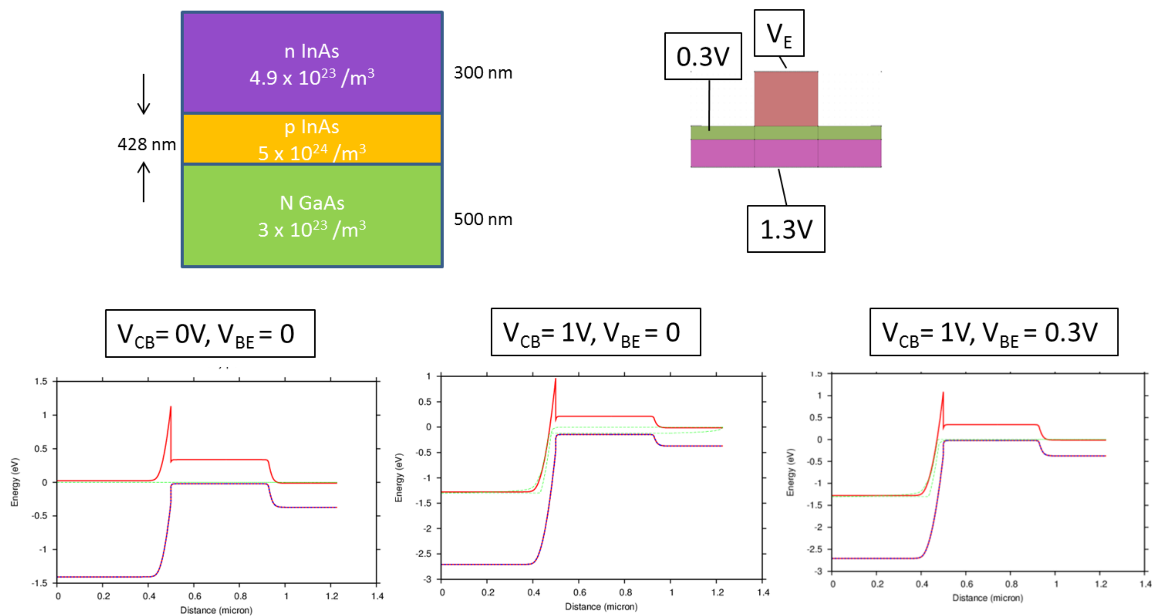
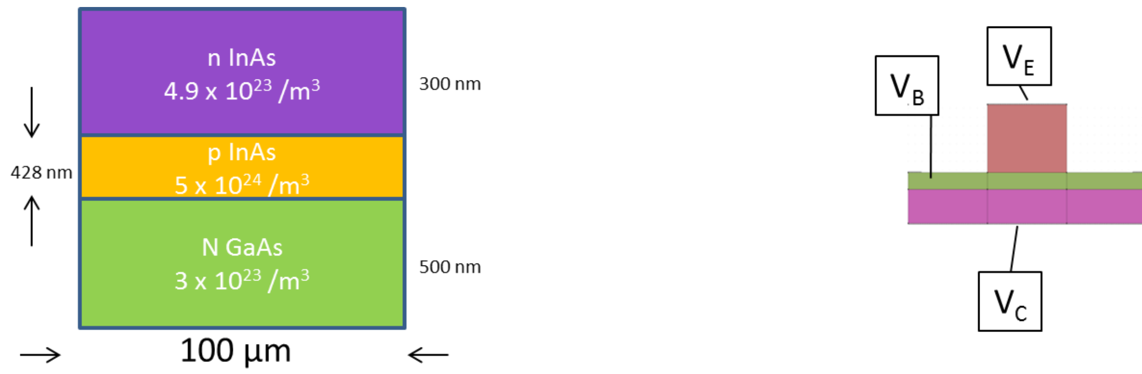


Figure 45. Npn GaAs/InAs/InAs HBT structure with 428 nm base. With this design, very little current will flow in the forward active mode. The "spike" at the collector-base boundary ($x \approx 0.5$ μm), as well as the remanent built-in potential at the base-emitter boundary, will both impede electron flow.



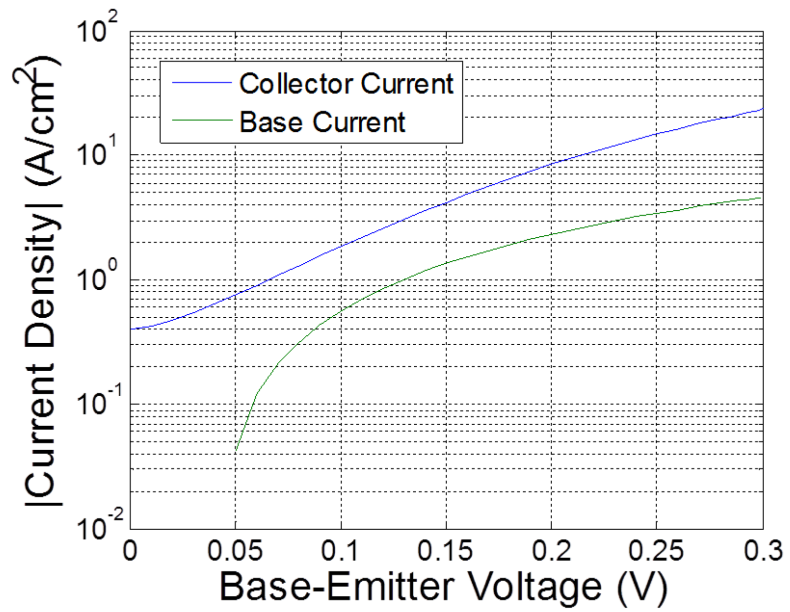


Figure 46. Simulated Gummel plot for Npn GaAs/InAs/InAs HBT structure with 428 nm base. $V_{CB} = 1V$.

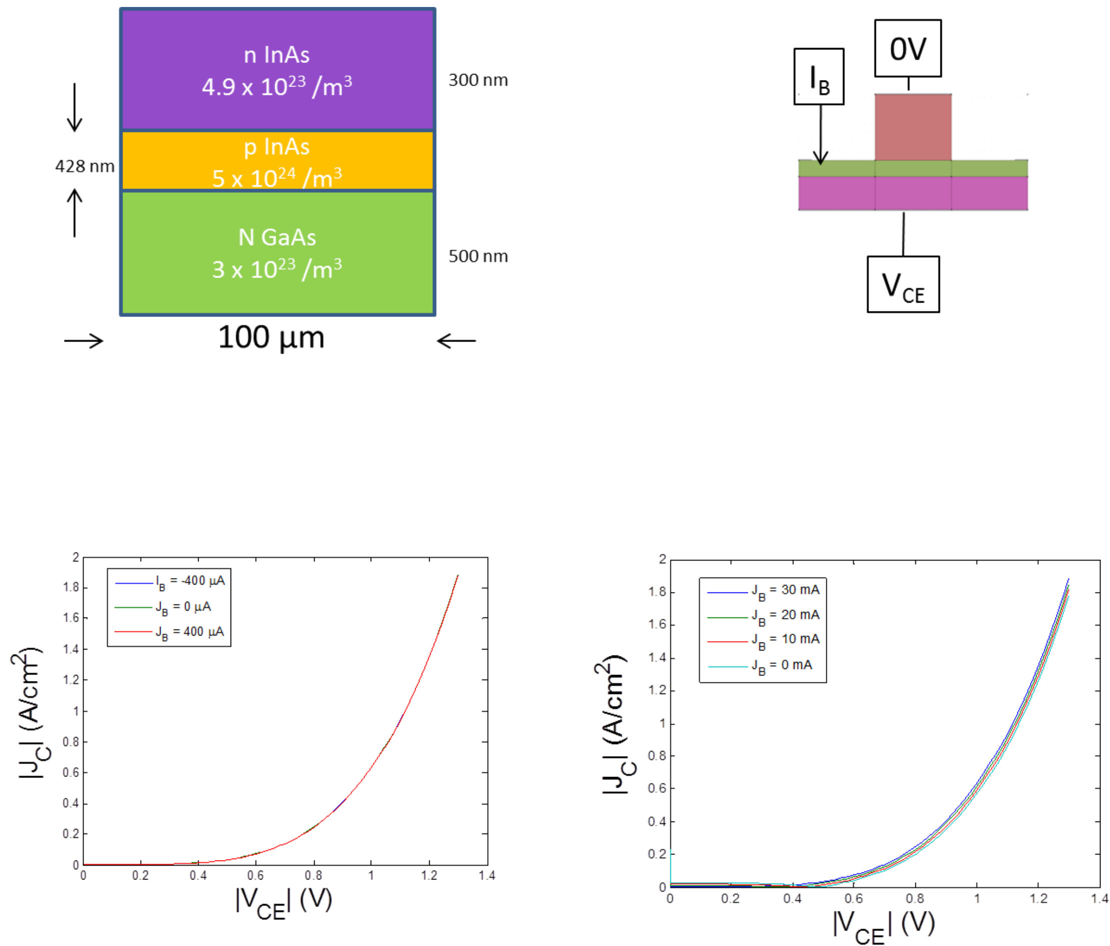


Figure 47. Simulated common emitter plot for Npn GaAs/InAs/InAs HBT structure with 428 nm base. The base current has no significant influence on the collector current. This design does not work.

Even though the design does not work as a transistor, the two junctions should function as diodes when the third terminal is floating. But the measured results show diode-like behavior only at the GaAs-InAs junction, not at the InAs-InAs junction. Since SIMS data are not available at the time of this writing, it is impossible to know if the actual doping of the sample is the same as the nominal specifications. It is also possible that since InAs is a narrow bandgap material, InAs homojunctions with high dislocation density are more susceptible to defect induced leakage current than are InAs-GaAs.

X. Summary and Conclusion

From considerations of the asymmetries of the band offsets of InAs-GaAs interface, it was determined that PnP InAs-GaAs HBTs are more promising than NpN InAs-GaAs HBTs. Three PnP GaAs/$In_xGa_{1-x}As$/GaAs HBTs have been designed and simulated. In order of increasing performance and complexity the three designs were GaAs/InAs/GaAs, GaAs/$In_{0.7}Ga_{0.3}As$/GaAs, and GaAs/$In_xGa_{1-x}As$/GaAs with x linearly graded from 0.7 to 0.75. Changing the base composition from InAs to $In_{0.7}Ga_{0.3}As$ reduces the leakage current, making the device more sensitive to small base currents. Changing the base composition from $In_{0.7}Ga_{0.3}As$ to GaAs/$In_xGa_{1-x}As$/GaAs with graded indium composition creates an electric field in the base that propels the holes and reduces the transit time, increasing the gain.

Diodes and HBTs have been fabricated and characterized. In a conventional homojunction GaAs diode, the measured "on-off" current ratio, I(+1 V)/I(-1 V), was more than 9 orders of magnitude. InAs-GaAs diodes showed a forward bias ideality factor of 1.26, but the leakage current was large and increased rapidly with bias. This may have been due to an effective opposite polarity diode at the surface, in parallel with the bulk diode. More sophisticated characterization and analysis needs to be done to verify this conjecture and to quantitatively explain the reverse ideality factor of 3.17.

Since the PnP material called for by the design was not immediately available, an Npn HBT structure was fabricated. The Npn HBT, while not functioning in simulation or in practice, provides a stepping stone for future work: fabricating one of the three PnP HBT designs from section 0.

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