DEVELOPMENT OF ADVANCED POWER FACTOR CORRECTION TECHNIQUES

by

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(ABSTRACT)

Three novel power factor correction (PFC) techniques are developed for both single-phase and three-phase applications. These techniques have advantages over the conventional approaches with regard to the converter efficiency, power density, cost, and reliability for many applications.

The single-phase parallel PFC (PPFC) technique was established. Different from the conventional two-cascade-stage scheme, the PPFC technique allows 68% of input power to go to the output through only one time high frequency power conversion, but still achieves both unity power factor and tight output regulation. A family of PPFC converters were proposed for different power levels, which are simpler and more efficient than the conventional two-cascade-stage systems. Since isolated boost converters are adopted as the main power stage in some of the PPFC converters, a device based soft-switching technique was proposed for using IGBTs as the main power switches, which ensures the lower cost and higher efficiency benefits of the PPFC technique.

the single-ended boost converter is the most frequently used converter in the single-phase PFC applications. For high power and/or high voltage applications, the major

concerns of the conventional boost converter are the inductor volume and weight, and losses on the power devices, which will affect converter efficiency, power density, and cost. In this dissertation, a novel three-level boost converter was developed, which can use a much smaller inductor and lower voltage devices than the conventional one, yielding higher power density, higher efficiency, and lower cost.

In three-phase applications, the three-phase boost rectifier is the most popular topology for the PFC purpose. A novel high performance boost PFC rectifier was developed, which provides several superior features than the conventional one with nearly no cost increase. It inherently provides six-step PWM operation, which is the optimal PWM scheme with no circulating energy, minimum input ripple current, and minimum switching events. It also greatly reduces the bridge diode reverse recovery loss, which is one of the major switching losses in the conventional three-phase boost rectifier. Furthermore, it can adopt very simple soft-switching techniques even with three independent analog controllers to further improve the performance. Several simple soft-switched three-phase boost rectifiers have been developed. Besides, the bridge shoot-through problem is virtually eliminated. As a result, these new three-phase boost rectifiers have higher efficiency, higher power density, lower cost, and higher reliability compared with the conventional one.

To my parents

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Chapter 1

Introduction

1.1 Background

Most electronics equipment is supplied by 60 Hz utility power; more than fifty percent of the electric power is processed through some kind of power conversion. A large portion of the power conversion equipment employ diode rectifiers or thyristor rectifiers to convert AC voltage to DC voltage before processing it. Such rectifiers produce very poor power factor with large displacement factor and strong harmonic currents [A-1, A-2]; the power line quality is seriously deteriorated. Recently, stringent requirements, such as IEC555-2 have been proposed and will be enforced to limit the harmonic currents drawn by the off-line equipment. As a result, power factor correction (PFC) has become one of the most sought after research topics in power electronics. To achieve good performance, high power density, and low cost, the high frequency switched-mode power conversion techniques have been developed for PFC.

The power factor is defined as the ratio of the average power to the apparent power at an AC terminal [A-3]. Assuming an ideal sinusoidal input voltage source, the power factor can be expressed as the product of two factors, the distortion factor and the displacement factor, as given in Eq. (1.1). The distortion factor k_d is the ratio of the

fundamental RMS current to the total RMS current. The displacement factor k_θ is the cosine of the displacement angle between the fundamental input current and the input voltage.

$$\begin{aligned} PF &= k_d \cdot k_\theta, \\ k_d &= \frac{I_{rms(1)}}{I_{rms}}, \\ k_\theta &= \cos\theta. \end{aligned} \tag{1.1}$$

For a load which draws less than unity power factor, it means that the load absorbs apparent power higher than the real power it consumes. The implication is that the AC power source needs to be rated with higher VA rating than the power consumption of the load equipment it supplies to. Furthermore, the harmonic currents it produces cause the power line quality to deteriorate, which inadvertently affects other users. Various attempts have been made using passive methods (low frequency LC filters) to compensate for the reactive power and harmonic currents created by non-linear loads, such as the diode rectifiers and the thyristor rectifiers. These low frequency LC filters are very bulky and not very effective under wide load variations. The active methods do not employ low frequency LC filters, thus offer significant less weight and volume than the passive methods. Furthermore, they are more suitable for wide line and load range.

Two types of active power factor correction methods are commonly used, the VAR/harmonic compensation method [B-23, B-24, C-25 - C-33] and the off-line PFC method [B-1 - B-22, C-1 - C-24]. The VAR/harmonic compensation method uses a switched-mode converter in parallel with the nonlinear load to supply the necessary reactive power and harmonic currents into the line, so as to cancel the displacement and/or harmonic currents created by the nonlinear load. However, the VAR/harmonic

compensation method cannot eliminate all harmonic currents, requires complicated bi-directional power flow topology and control, and does not provide regulated output to the load. On the other hand, the off-line PFC method uses a high frequency switched-mode converter in series with the nonlinear load as the line-load interface. It shapes the input current into a sinusoidal waveform and it is in phase with the input voltage to produce unity power factor and, at the same time, provides a regulated DC voltage or DC current source to the load.

This dissertation will focus on the off-line PFC techniques. In the following, the current status of both the single-phase and the three-phase off-line PFC techniques will be briefly reviewed, and the contributions of this dissertation will be introduced.

1.1.1 Single-Phase PFC Techniques

PFC Converter Topologies: Among the three basic converter topologies (buck, boost, and buck-boost), the boost topology is the most suitable one for the PFC applications, because the inductor is sitting at the input port giving low ripple continuous input current. However, the output voltage must be higher than the peak input voltage. The buck topology is seldom used for the PFC, except for very particular applications [B-1, B-2], because its step-down feature loses control of the input current when the line voltage drops below the output voltage. The buck-boost topology can also control the average input current properly. However, its power handling capability is limited by the high voltage/current stresses on the semiconductor devices and the pulsating input and output currents.

Non-isolated PFC Converters: The single-ended boost PFC converter as shown in Fig. 1.1 has been widely used [B-3 - B-14], and its control IC chips, such as UC3854 made by Unitrode for average current mode control and ML4812 made by Micro-Linear for peak current mode control, have been available for years. The single-ended boost PFC converter has several superior features which essentially eliminate the use of other single-ended topologies in most applications. First, the continuous input current is suitable for the average input current mode control and requires small EMI input filters. Secondly, the boost converter is very efficient as a PFC converter because the active switch is in a shunt path with respect to the power flow path; its duty-ratio becomes smaller as the sinusoidal input voltage and current reach their peaks.

Although there are variations of the non-isolated boost converters, they usually do not offer advantages over the basic boost topology. For example, the boost inductor can be moved to the AC side, and the one leg of the full bridge diode rectifier can be replaced by an active switch leg as shown in Fig. 1.2. The obtained two-switch boost PFC converter saves one diode conduction loss and seems more suitable for high power applications, since the two active switches share the task. However, the reverse recovery problem of the active switch anti-parallel diodes is severe, and the implementation of soft-switching is not as easy as in the normal single-ended boost converter.

Though the buck-boost converter can control the input current properly, its pulsating input current requires a larger EMI filter, and, more seriously, the buck-boost topology is usually much less efficient than the boost topology, due to the higher current and voltage stresses of the switches.

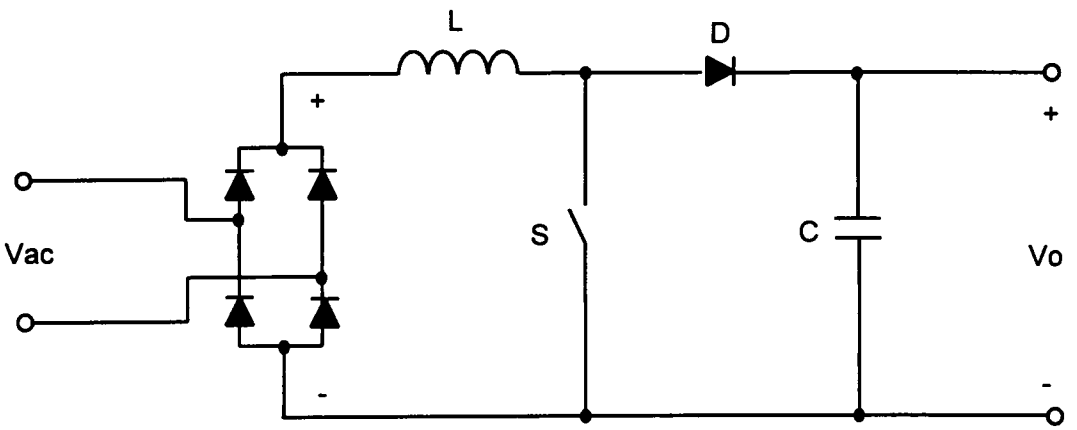


Fig. 1.1 Single-ended boost PFC converter.

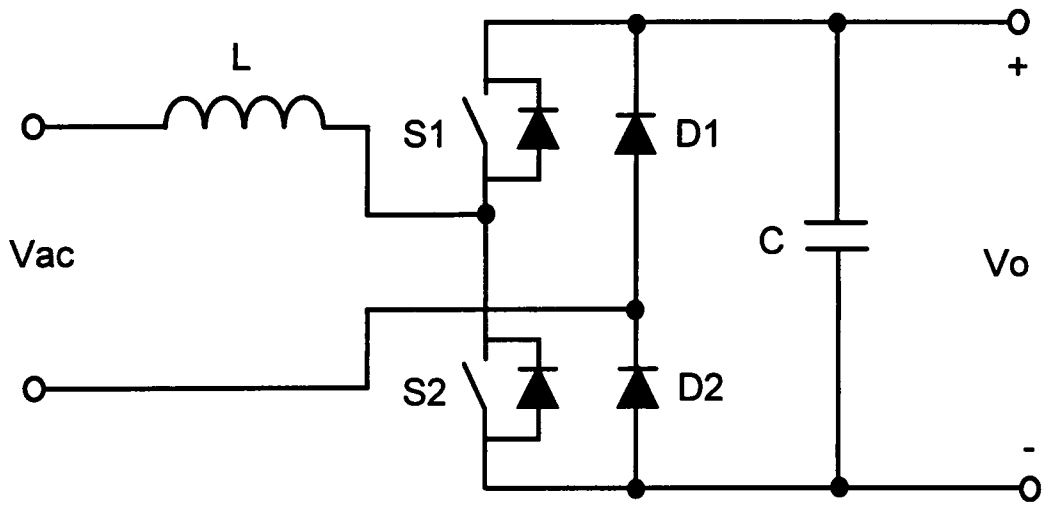


Fig. 1.2 Two-switch boost PFC converter.

For applications where line voltage is too high resulting excessive output voltage, a buck+boost converter can be employed [B-15] as shown in Fig. 1.3. Different from the basic one-switch buck-boost converter, it is a buck converter in series with a boost converter with a common inductor. It works in pure boost mode with the buck switch closed when the instantaneous input line voltage is lower than the output voltage, and otherwise in pure buck mode with the boost switch opened. With regard to the efficiency and the high frequency harmonic contents of the input current, It is much better than the basic single-switch buck-boost converter.

Isolated PFC Converters: The output of the single-ended boost PFC converter must be higher than the peak of the input voltage. For universal line voltage (85V-265V), the output must be set at around 400 Vdc or above. However, in many applications, a low voltage dc bus is required; for example, to provide 48 Vdc bus for telecommunication systems. Also, to meet the safety regulations, the isolation is normally required between the input and the output. So, the isolated boost PFC converter and the flyback PFC converter are thus applicable.

The isolated boost converter has different versions [B-13, D-3], including the full-bridge version as shown in Fig. 1.4 as well as the two-switch push-pull version and the two-inductor version. The principle is the same as that of the single-ended boost PFC converter. The major problem of the isolated boost converters is the conflict between the boost inductor and the transformer leakage, which requires active clamp to limit the voltage stress on the switches; but no simple active clamp scheme is available for high power applications, which favor isolated boost converter other than flyback converter.

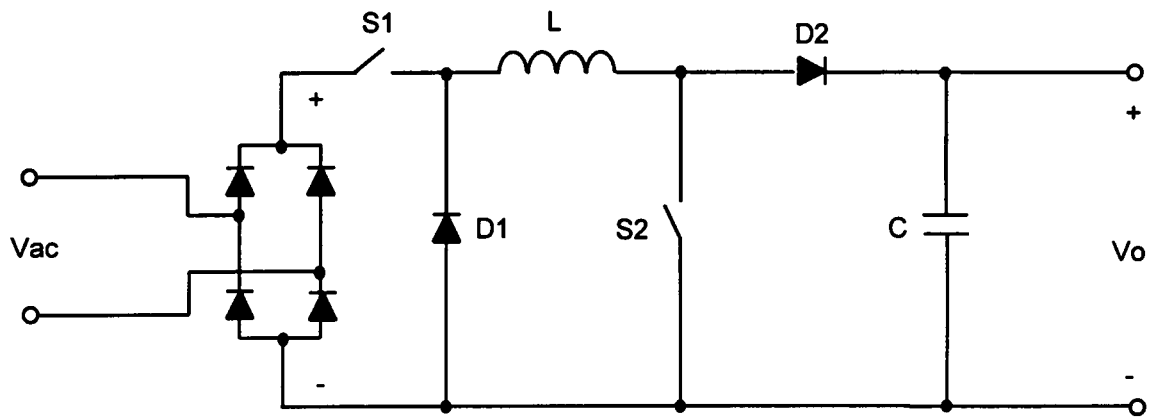


Fig. 1.3 Buck+boost PFC converter.

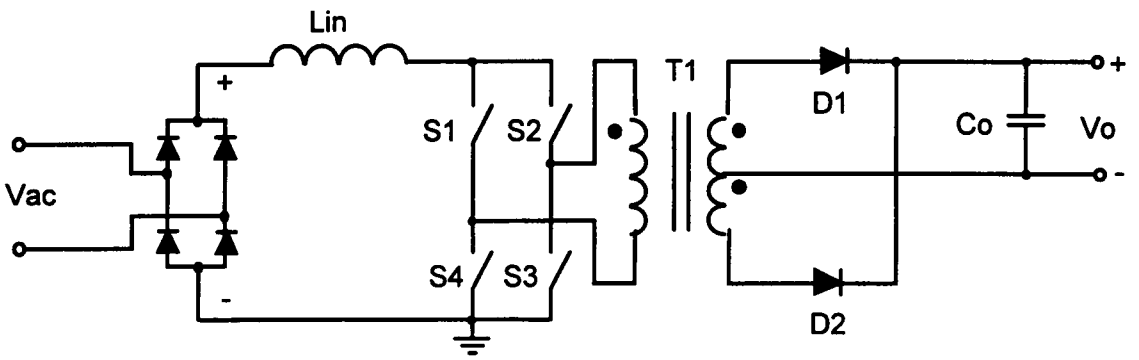


Fig. 1.4 Full bridge isolated boost PFC converter.

Although the single-ended buck-boost converter has never been seen as a PFC converter, its isolated version, the flyback converter shown in Fig. 1.5, is very attractive as a PFC converter [B-16 - B-18], since it only requires one magnetic component and one active switch, and, thus, is much simpler than the isolated boost converters. Another advantage comes from the control. The flyback converter can produce unity power factor with constant duty ratio under discontinuous conduction mode (DCM) operation [B-16]. Also, it has the features of soft start-up and output short-circuit protection. The major drawbacks of the flyback converter are the pulsating input current even under continuous conduction mode (CCM) operation [B-17] and the transformer energy storage requirement which makes it hard to design for high power. Consequently, it is a very nice solution for low power PFC applications (usually below 300 watts).

PFC Converters with Tight Output Regulation: It is important to note that in order to achieve unity power factor of a single-phase input, the input power and the output power of a PFC converter are unbalanced within a half-line cycle. Assuming unity power factor, the input power is a squared sine waveform, and the output power is assumed to be constant, as in most applications. This low-frequency power unbalance has to be handled by an energy storage element, usually a bulk capacitor. For a typical single-stage power converter, this bulk capacitor is the output filter capacitor. This huge output filter capacitor severely limits the output dynamic response. Moreover, though this capacitor is bulky, there is still quite a significant low-frequency voltage ripple appearing at the output. Thus, if a well regulated output is specified, the two-cascade-stage configuration is usually adopted, which means that another DC/DC front-end converter will follow the PFC converter.

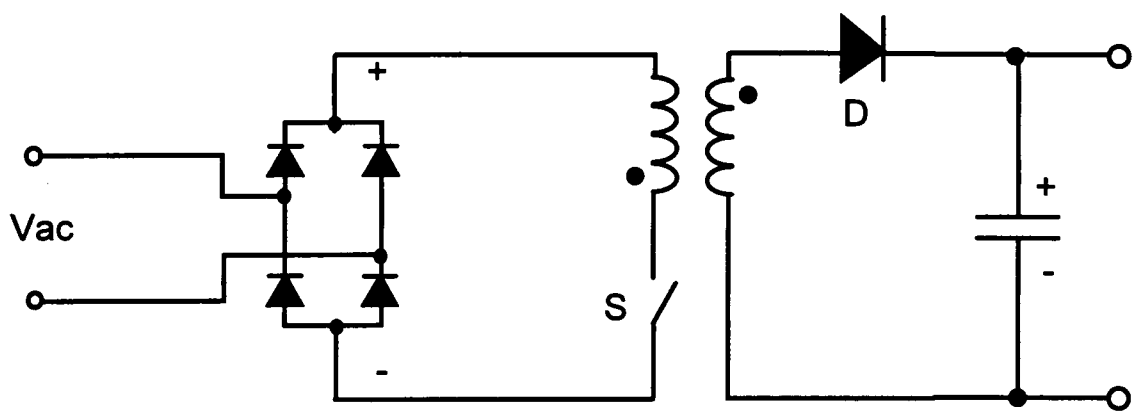


Fig. 1.5 Flyback PFC converter.

In the two-cascade-stage configuration, the single-ended boost converter seems to be superior for the normal input voltage range (85 -265 Vrms). The second stage DC/DC converter provides isolation and tight output regulation. So far, this configuration is almost the only practical solution for fulfilling the tight output regulation requirement.

However, the major drawback of such a two-cascade-stage system is that input power needs to be converted twice to reach the output, which is complex and inefficient. Some simple "single-stage" PFC circuits were proposed by combining the two cascaded stages, such as the BIFRED [B-27], BIBRED [B-27], DITHER [B-28], and some resonant circuits [B-26]. The principle used in these circuits is to allow two cascaded stages to share the active switch(es), so that the power circuit becomes simpler. However, due to the switch sharing, the control freedom is greatly reduced, thus necessitating discontinuous-conduction-mode (DCM) operation, variable frequency, and/or excessive bulk capacitor voltage to achieve both PFC and the tight output regulation [B-30]. Also, the voltage and current stresses of the active switches are much higher than those of the switches in a conventional two-cascade-stage system, resulting in higher conduction and switching losses. So, these "single-stage" PFC converters usually have less efficiency than do the conventional two-cascade-stage systems.

1.1.2 Three-Phase PFC Techniques

Much research has been concentrated on the three-phase inverter aspects. The PWM switched-mode rectifiers, on the other hand, did not receive much attention until recent years. Though most of the PWM techniques developed for the inverters are useful for the rectifiers as well [E-1 - E-8], there are some special aspects of the rectifiers which distinguish them from the inverters and they have not been fully explored at the present

time. The very simple rectifier with superior performance proposed in this dissertation is an example.

A balanced three-phase system has constant instantaneous input power under the assumption of unity power factor. Therefore, the output of the PFC converter will not contain low frequency ripple, and no bulk capacitor is necessary. Both the boost and buck rectifiers are capable of producing unity power factor [C-1 - C-20]. However, the boost rectifier shown in Fig. 1.6 is more desirable. It is simpler and more efficient than the buck rectifier, and it can operate bi-directionally and provide continuous input currents. These features made it desirable for high power applications in general. The buck rectifier, which has higher switching losses and higher conduction losses than the boost rectifier, is applicable only in some limited applications, such as feeding a current source inverter.

Despite of the availability of three-phase bridge converters for PFC, many practicing engineers still favor the use of three single-phase PFC converters to form a three-phase PFC system [C-13]. In this manner, control schemes and soft-switching techniques are easier to apply as compared with the conventional three-phase boost rectifier. It can also be treated as a simple module to form a multi-module system. However, it is not easy to parallel three single-ended boost PFC converters at their outputs due to the interaction among phases; and, though each phase seems simple, the whole system, consisting of three PFC controllers and three soft-switching auxiliary networks are quite complicated.

A very simple three-phase boost rectifier has been reported in [C-6]. It uses the simple three-phase diode bridge and only one active switch on the DC side. The power factor correction is obtained by operating this boost converter in discontinuous conduction

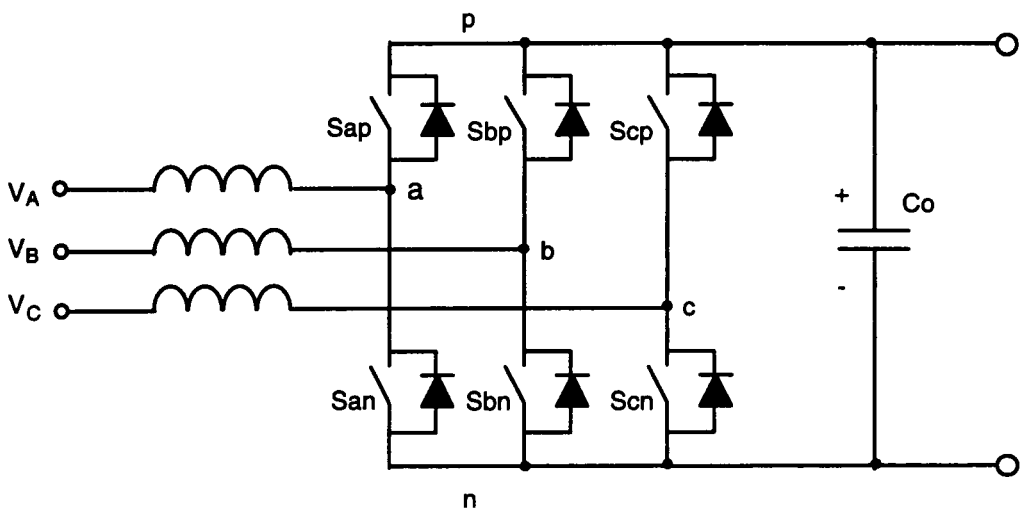


Fig. 1.6 Three-phase boost PFC rectifier.

mode (DCM). Its advantage is its simplicity. However, with this converter, the unity power factor requires excessive output voltage. With a practically acceptable output voltage level, the harmonic distortion will not meet the regulation if the power level is above several kilowatts. Another limitation concerning the power level is the high input current ripple produced by the DCM operation which requires a larger input filter.

Beside the buck and boost AC-DC PFC converters, another type of the off-line three-phase PFC converters are the AC-AC matrix converters [C-21 - C-24]. These converters possess the matrix topology and adopt the space vector control. Their major advantage is their capability of performing four-quadrant operation, while their major disadvantage is complicated control and the difficulty of implementing the four-quadrant switches.

1.1.3 Soft-Switching in PFC Converters

Beside the PFC techniques themselves, the associated soft-switching techniques are also very important. Since magnetic components are used in all PFC converters and EMI filters, and their volume and weight are directly related to the switching frequency, there is always the demand to run those converters at the highest possible switching frequency so as to achieve minimum size and weight. The switching frequency is limited by switching losses. In PFC converters, high voltage semiconductor devices are needed. According to device characteristics, high voltage devices have high switching losses. For example, the reverse recovery losses of high voltage diodes and the turn-off losses of IGBTs are quite significant. Therefore, soft-switching techniques are desired in PFC converters.

To accommodate the high frequency operation, the switched-mode power conversion technologies have evolved from basic hard-switching PWM converters to resonant converters, quasi-resonant converters, multi-resonant converters, and most recently to soft-switching PWM converters. The hard-switching PWM converters process power by abrupt switching, which results in significant switching losses, switching noise, and switching stresses, especially at high switching frequency. To improve the switching condition, several resonant techniques were developed. The resonant converters, which include the traditional series and parallel resonant converters, class-E converters [D-1], quasi-resonant converters [D-2, D-3, D-6], and multi-resonant converters [D-4 - D-7], process power in a sinusoidal or quasi-sinusoidal form. The power switches are commutated with either zero-voltage switching (ZVS) or zero-current switching (ZCS); thus, switching losses and stresses of the resonant converters are significantly reduced in comparison with those of the hard-switching PWM converters. However, due to the resonant nature of the current and voltage waveforms, the operation of the resonant converters usually involves high circulating energy, which results in a substantial increase in conduction losses [D-8]. In addition, due to wide line/load range, most resonant converters operate with a wide switching frequency range, which makes the optimal circuit design difficult.

To overcome the problems of the resonant converters, various soft-switching PWM techniques were recently proposed, aiming at achieving soft-switching while minimizing the circulating energy [D-9]. The principle underline of operation is that in order to obtain the soft-switching condition, the resonant process should occur only during switching transients. When a switching transition is complete, the converter reverts back to the normal PWM operation. In this manner, the circulating energy regard to implementing soft-switching is minimized, and the conduction losses reduced to the

theoretical minimum value. Another important advantage of soft-switching PWM converters over the resonant converters is that they usually operate at constant frequency, which is important for circuit optimization. The zero-voltage-switching PWM (ZVS-PWM) [D-10 - D-11], zero-voltage-transition (ZVT) [D-12, D-13], and zero-current-transition (ZCT) [D-14] techniques belong to this category and are very useful in the PFC applications.

The soft-switching techniques reviewed above were developed solely for the DC/DC converters, but could also be used for the single-phase PFC converters. For example, the ZVT technique is initiated by the need of the single-phase boost PFC converter. For the three-phase systems, there are two types of soft-switching techniques: the AC side technique and the DC side technique. The typical AC side soft-switching techniques are the Auxiliary Resonant Commutated Pole [D-18] and the Zero-Voltage Transition Three-Phase PWM Rectifier/Inverter [D-19]. These AC side soft-switching techniques require quite complicated soft-switching auxiliary networks and sophisticated digital control. The best known DC side soft-switching technique would be the Resonant DC Link (RDCL) technique [D-20, D-21]. The RDCL technique adopts a resonant network on the DC rail to provide a zero-voltage-switching condition for the bridge switches. Since the resonance is accompanied by the power transfer all the time, the switches suffer from high voltage/current stresses, which leads to high losses. In recent years, as the development of the soft-switching PWM technique in the DC/DC converters, some three-phase soft-switching PWM techniques were proposed [D-22 - D-37]. Though most of them are still known as variants of resonant dc link converters, they are principally different from the original RDCL converters, since the resonant process occurs only during the short switching periods; therefore, they still have the basic PWM features.

The above mentioned soft-switching techniques are circuit-based, i.e. soft-switching is implemented using an auxiliary resonant circuit. Another kind of soft-switching method is device-based, which employs an auxiliary switch to alleviate the particular turn-on or turn-off problem of the main power devices, while the voltage/current waveforms are still pure PWM without involving any resonance. The mixed device [D-15 - D-17] is an example which uses the fast device MOSFET to help the slow device IGBT.

1.2 Motivations and Objectives

When a tightly regulated output is required in a single-phase PFC system, the two-cascade-stage configuration is the most commonly used approach. However, due to the two stages in cascade, the circuit is complicated, and the total efficiency is the product of the individual efficiency of each stage. The motivation, therefore, is to simplify the circuit and improve the efficiency of the two-cascade-stage system at the same time.

The single-ended boost converter has been widely used as the front-end PFC converter, due to its step-up voltage conversion ratio, continuous input current, simple topology, and high efficiency. However, there are still some concerns. For high power applications, the boost inductor is physically large and is one of the major factors affecting the system cost, volume, and weight. For high voltage applications, high voltage devices must be used, which produces high conduction losses and high

switching losses. Therefore, the motivation is to use a smaller inductor and lower voltage devices.

The conventional hard-switched PWM three-phase boost rectifier, as the most useful three-phase PFC converter, has severe switching losses; available soft-switching techniques are all complicated and inefficient [D-18 - D-37]. The diode reverse recovery problem causes significant turn-on losses, and the current tail problem of the slow devices like the IGBT, which is preferred for three-phase high power applications, induces high turn-off losses. The optimal six-step operation was normally achieved with digital control, which is more expensive and less reliable than the simple analog control scheme. Besides, the bridge shoot-through is always a concern and raises the complexity of the driver circuits. Hence, the motivation for the three-phase work is to solve these major problems so that the three-phase boost converter can have better efficiency at a much higher switching frequency and higher reliability with simple analog control.

Based on these motivations, the objective of this dissertation is to develop several high performance PFC techniques to improve the conventional techniques in the above mentioned aspects.

1.3 Major Results

The single-phase parallel PFC (PPFC) technique was established. Different from the conventional two-cascade-stage scheme, the PPFC technique allows 68% of input power to go to the output through only one time high frequency power conversion, but still achieves both unity power factor and tight output regulation. A family of PPFC converters were proposed for different power levels, which are simpler and more efficient than the conventional two-cascade-stage systems. Since isolated boost converters are adopted as the main power stage in some of the PPFC converters, a device based soft-switching technique was proposed for using IGBTs as the main power switches, which ensures the lower cost and higher efficiency benefits of the PPFC technique. This technique will be described in Chapter 2 and 3.

As mentioned earlier, the single-ended boost converter is the most frequently used converter in the single phase PFC applications. For high power and/or high voltage applications, the major concerns of the conventional boost converter are the inductor volume and weight, and losses on the power devices, which will affect converter efficiency, power density, and cost. In this dissertation, a novel three-level boost converter was developed, which can use a much smaller inductor and lower voltage devices than the conventional one, yielding higher power density, higher efficiency, and lower cost. This technique will be described in Chapter 4.

In three-phase applications, the three-phase boost rectifier is the most popular topology for the PFC purpose. A novel high performance boost PFC rectifier was developed, which provides several superior features than the conventional one with nearly no cost

increase. It inherently provides six-step PWM operation, which is the optimal PWM scheme with no circulating energy, minimum input ripple current and minimum switching events. It also greatly reduces the bridge diode reverse recovery loss, which is one of the major switching losses in the conventional three-phase boost rectifier. Furthermore, it can adopt very simple soft-switching techniques even with three independent analog controllers to further improve the performance. Several simple soft-switched three-phase boost rectifiers have been developed. Besides, the bridge shoot-through problem is virtually eliminated. As a result, these new three-phase boost rectifiers have higher efficiency, higher power density, lower cost, and higher reliability compared with the conventional one. This technique will be described in Chapter 5.

Chapter 2

Single-Phase Parallel Power Factor Correction (PPFC) Technique

2.1 Introduction

As mentioned in Chapter 1, for single-phase power factor correction with tight output regulation, normally a two-cascade-stage configuration is adopted. In this chapter, a new single-phase power factor correction concept, the parallel PFC (PPFC), will be established, which allows major input power to be processed only once, while still achieving both unity power factor and tight output regulation. This PPFC concept provides an opportunity to achieve simpler and more efficient single-phase PFC converters than the conventional two-cascade-stage approach. Several PPFC schemes and circuit implementations will be proposed for applications of different power levels.

2.2 Parallel Power Factor Correction Concept

Under unity power factor assumption, the input power of a single-phase PFC converter is given in Eq. 2.1.

$$p_{in}(t) = P_m \cdot \sin^2(\omega t); \tag{2.1}$$

where $P_m = V_m \cdot I_m$ is the peak input power; V_m and I_m are the amplitudes of the input sinusoidal voltage and current, respectively.

Since the input power and the output power are balanced in the average sense, the output power, which is assumed to be constant, must equal to the average input power, as indicated in Eq. 2.2:

$$\begin{aligned} P_o = P_{ave} &= \frac{1}{\pi}\int_0^{\pi} P_m \cdot \sin^2(\omega t) d(\omega t) \\ &= \frac{P_m}{2} \end{aligned} \tag{2.2}$$

The input power $p_{in}(t)$ and the output power P_o waveforms are drawn in Fig. 2.1.

With a large amount of power unbalance between the input and the output within a half line cycle (t_0 - t_2), a bulk capacitor has to be used as an energy storage element. In a conventional PFC converter, this large capacitor is part of the output capacitor, which not only slows down the PFC circuit output dynamics but also contains certain line second harmonic (120 Hz) ripple voltage. The PFC stage output voltage loop cross-over frequency, therefore, has to be designed well below 120 Hz. To obtain tight output regulation, the configuration shown in Fig. 2.2 is normally used, where a PFC stage is followed by a DC/DC stage with the bulk capacitor in-between.

The two stages in cascade means a complicated system and low conversion efficiency since it is the product of the efficiency of each individual stage. So far, there has been

little effort reported on improving the efficiency by changing the power stage configuration or topology. Those single-stage PFC converters [B-25 - B30], such as the BIFRED, combine the two stages into one using switch-sharing technique. But switch-sharing does not provide minimum power processing feature because the full input power is still processed twice and the switch-sharing between the first and the second stages only increases switch current stress, causing higher conduction losses. Switch-sharing also reduces the control freedom leading to discontinuous mode operation (DCM), widely variable tank voltage and switching frequency. DCM operation increases the switch current stress and variable tank voltage increases switch voltage stress. High current and voltage stresses produce high conduction and switching losses. Thus, such single-stage PFC converters usually are less efficient than the two-cascade-stage converters and can only be used for low power applications.

By examining the input and the output power relationship shown in Fig. 2.1, one can find out that only the amount of P_2 power, which is the difference between the input power and the output power within a half line cycle, needs to be processed twice in order to achieve PFC and tight output regulation. During period t_0-t_1, when the input power is higher than the output power, the excess energy should be stored somewhere after the first time processing , and during period t_1-t_2, when the input power is less than the output power, the previously stored energy should be released to the load by the second time processing in parallel with the input power

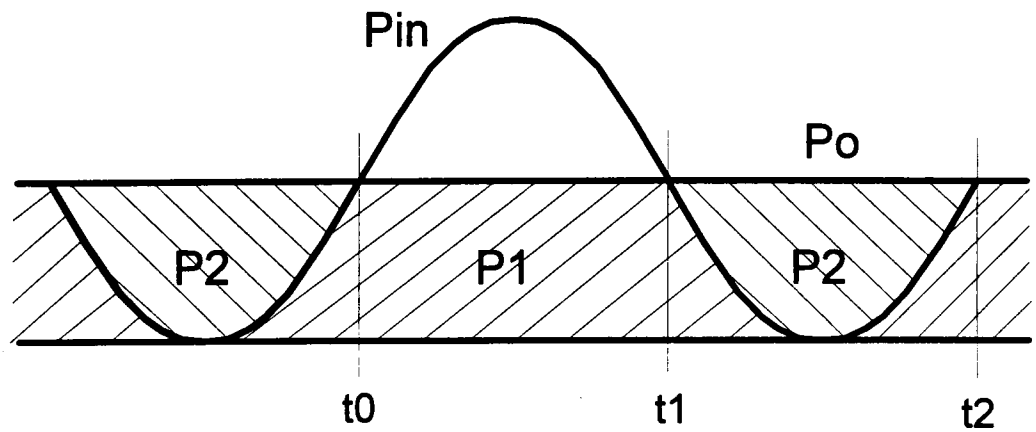


Fig. 2.1 Input and output power of single-phase PFC converters.

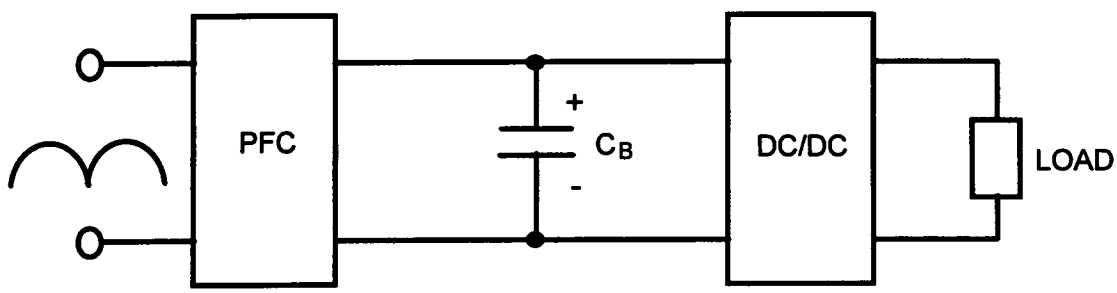


Fig. 2.2. Two-cascade-stage configuration for tight output regulation.

The amount of P_2 power can be calculated with Eq. 2.3.

$$\begin{aligned} P_2 &= 2 \times \frac{1}{\pi} \int_0^{\pi/4} (P_{av} - p_{in}(\omega t)) \cdot d(\omega t) \\ &= \frac{2}{\pi} \int_0^{\pi/4} P_{av} \cdot \cos(2\omega t) \cdot d(\omega t) \\ &= \frac{P_{av}}{\pi} \approx 0.32 P_{av} \end{aligned} \tag{2.3}$$

Thus, the parallel power factor correction (PPFC) concept can be formulated as the following: *To achieve both unity input power factor and tight output regulation, about 68% of the average input power (P_1) can reach the output through one power conversion stage, and only the remaining 32% of the power (P_2), which is the difference between the input and output power within a half line cycle, needs to be processed twice.*

2.3 PPFC Schemes and Circuit Implementations

There are several different ways, in terms of the system configuration and converter topology, to implement the above parallel power factor correction concept. Several schemes and corresponding circuit implementations are proposed in this section.

2.3.1 PPFC Scheme 1 and PPFC Converter 1

The first scheme realizing the PPFC concept is given in Fig. 2.3.

In this scheme, three stages are employed. According to the PPFC concept, this system can be controlled in such a way that stages 1 and 2 only process P_2 power, which is about 32% of the total input power, and stage 3 processes P_1 power, which is about 68% of the total input power. It is easy to see that the stages 1 and 2 never operate at the same time, because stage 1 only operates when $p_{in} > P_o$, and stage 2 only operates when $p_{in} < P_o$. With this scheme, there is still more than one way to control the PPFC operation. One straight method is to use stage 3 to control the input current and use stages 1 and 2 to control the instantaneous input and output energy balance, which is equivalent to regulate the output voltage.

This scheme looks more complex than the two-cascade-stage scheme at first glance. However, for high power applications, where multi modules in parallel are preferred with the conventional two-cascade-stage scheme, as shown in Fig. 2.4, stage 3 in Fig. 2.3 replaces two out of three two-cascade-stage modules, which simplifies both power and control circuits. Stage 3 in Fig. 2.3 is capable of handling higher power due to its higher efficiency than the conventional two-cascade-stage system, which will be demonstrated in the next chapter. This three-stage combination can also be treated as one module, and multi modules can provide higher power. Based on this understanding, this scheme provides simpler circuitry and higher efficiency than the conventional two-cascade-stage system for high power applications.

With the PPFC scheme 1, shown in Fig. 2.3, stage 3 must have a step-up voltage conversion ratio characteristic to achieve input current control within the whole line cycle. Therefore, its topology should be either boost or buck-boost type. Since stage 3

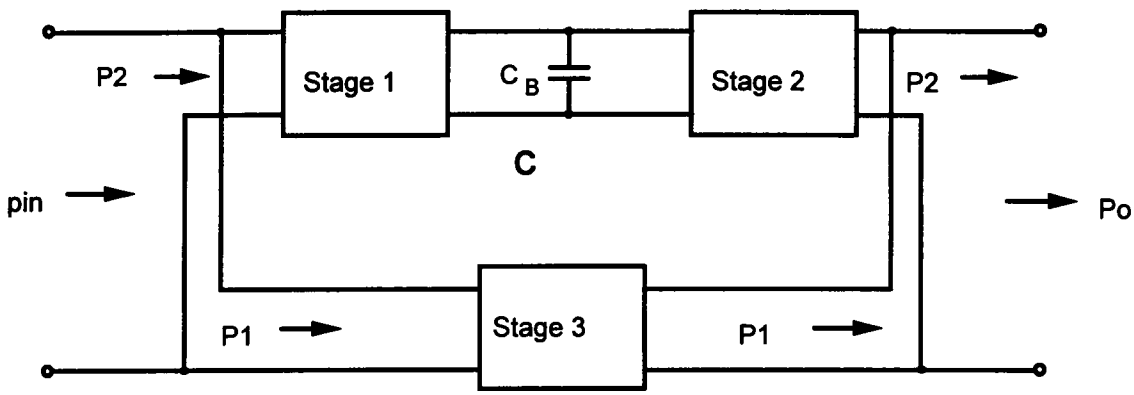


Fig. 2.3 PPFC scheme 1.

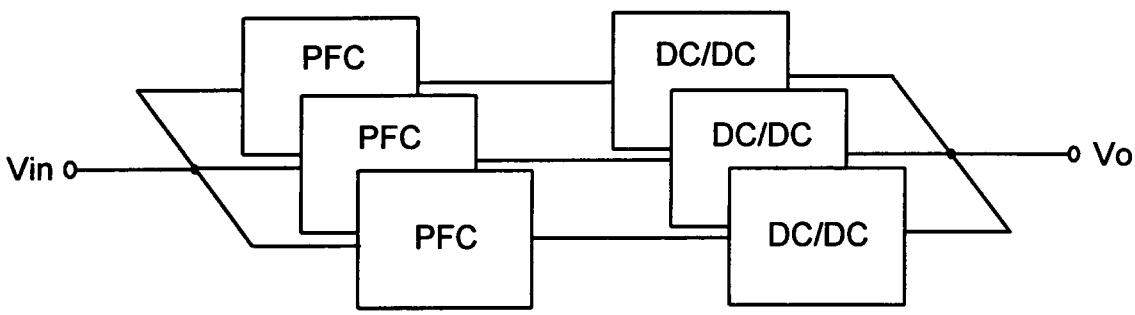


Fig. 2.4 Multi-modules in parallel for high power PFC applications.

is supposed to process quite high power, boost topology is more favorable than the buck-boost topology. Due to the input-output isolation requirement, it should be an isolated boost converter. Stage 1, which operates when the input power is higher than the output power during a normal situation, may need to operate at other times as well during the dynamic process, and its output is connected to the bulk capacitor, which is preferred at high voltage. Hence, stage 1 should also be a step-up topology for which the single-ended boost converter would be the choice. Stage 2 is basically an isolated DC/DC converter, which, though theoretically can be any type of topology, favors the buck type since the output voltage is usually lower than the bulk capacitor voltage, and step-down is needed.

An example circuit called PPFC converter 1 is given in Fig. 2.5, where stage 1 is a single-ended boost converter, stage 2 is a forward converter, and stage 3 is a full-bridge boost converter which can be other isolated boost converters as well.

The control mechanisms are different for the time interval when $p_{in} > P_o$ and the time interval when $p_{in} < P_o$. The input current and three inductor currents over a half line cycle are shown in Fig. 2.6.

During $t_0 - t_1$ and $t_2 - t_3$ when $p_{in} < P_o$, the upper DC/DC forward converter operates to release energy from the bulk capacitor and, therefore, regulates the output voltage. The lower boost converter controls the input current and transfers all the input power to the output. The inductor current i_{L3} is the input current; the output load current is the summation of the inductor current i_{L2} and the secondary reflected current of the isolated boost converter.

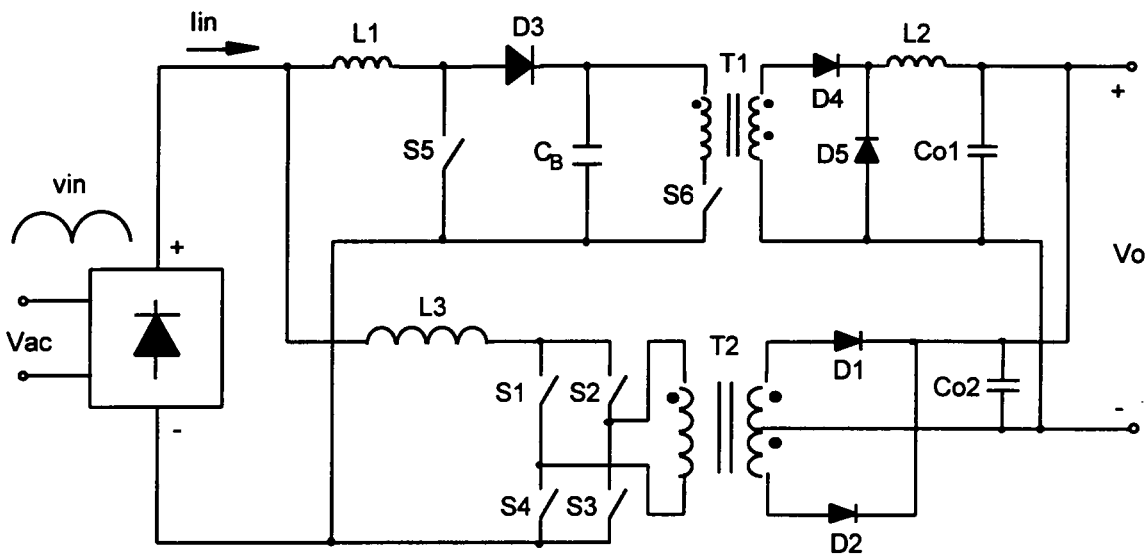
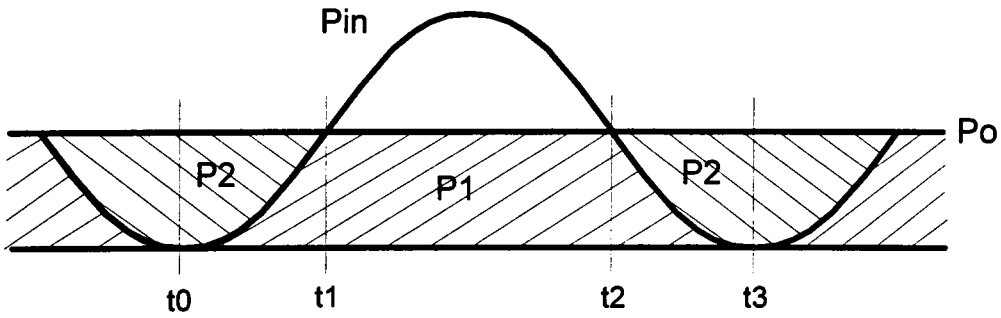
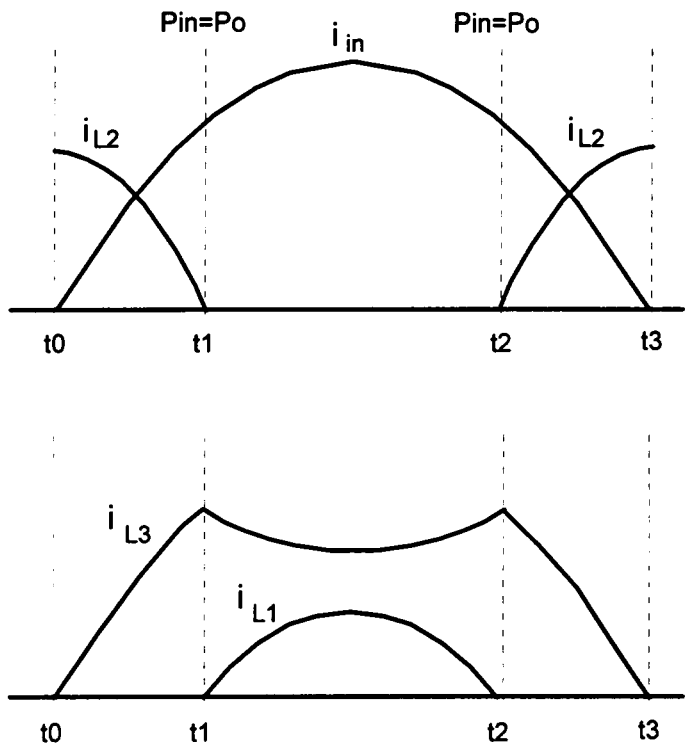


Fig. 2.5 PPFC converter 1 implementing PPFC scheme 1.



(a)



(b)

Fig. 2.6 Low frequency operation waveforms in PPFC converter 1
(a) Input and output power of single-phase PFC converters;
(b) Input and inductor currents in PPFC converter 1.

During t_1 - t_2 when $p_{in} > P_o$, the two boost converters are operating. There are two control variables available, which are the duty-ratios of the two boost converters. It is assigned that the upper single-ended boost converter controls the power flow, and the lower isolated boost converter controls the input current. The input current is the summation of two inductor currents i_{L1} and i_{L3}; the output load current is the output current of the isolated boost converter.

2.3.2 PPFC Scheme 2 and PPFC Converter 2

For applications where power levels are not high enough to justify using three power stages, one way to simplify scheme 1 is to combine stages 1 and 3 together as shown in Fig. 2.7, which is called PPFC scheme 2.

Stage 1 handles the full input power in this case. It has two outputs; one goes to the bulk capacitor, and the other goes to the system output. Here, there is only one way to achieve the PPFC operation. Stage 1 controls both the input current and output voltage when $p_{in} > P_o$. Stage 2 only operates to regulate the output voltage when $p_{in} < P_o$.

This scheme needs only two power stages and is simpler than the first one, but it puts more burden on Stage 1. It is easy to see that scheme 1 favors higher power than scheme 2 The choice between scheme 1 and scheme 2 depends on the circuit implementation, device choice, application specifications, and designer's preference.

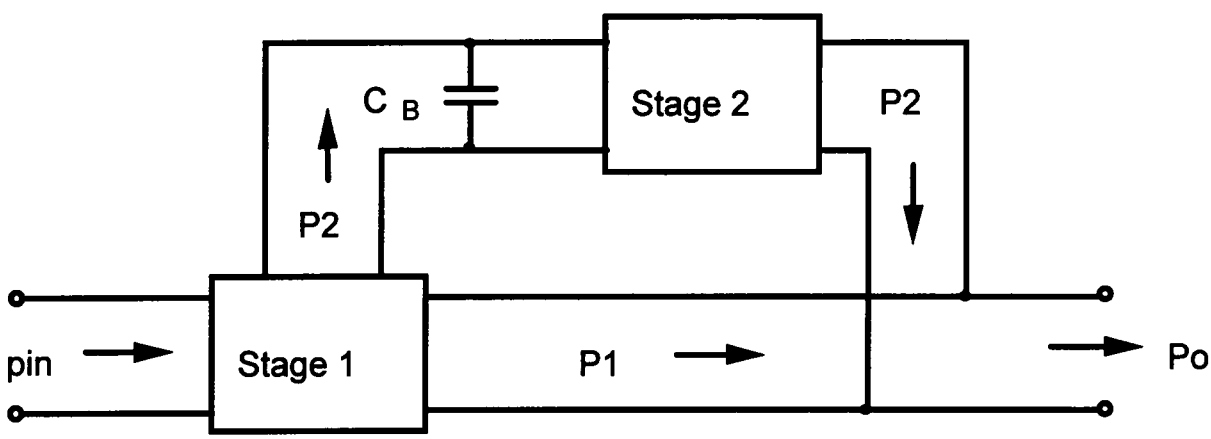


Fig. 2.7 PPFC scheme 2.

The circuit shown in Fig. 2.8 implements PPFC scheme 2, and is named PPFC converter 2. For the same reason as topology choice for scheme 1, the main power stage (stage 1) is an isolated full bridge boost converter. The auxiliary stage (stage 2) here is a forward converter. Compared with PPFC converter 1 in Fig. 2.5, it saves the boost inductor and the boost switch of the upper single-ended boost converter.

The operation waveforms of PPFC converter 2 are shown in Figs. 2.9(a) and (b).

Case 1: $p_{in} > P_o$, see Fig. 2.9(a)

At the beginning of a switching cycle t_0, four bridge switches S_1 - S_4 are turned on, and the input voltage charges the boost inductor. At time t_1, all bridge switches are turned off, forcing the boost inductor current to flow through diode D_1 into the bulk capacitor C_B, and the inductor is discharged by the voltage difference between the bulk capacitor voltage and the input voltage. The instant t_1 is used to control the input current. At time t_2, one pair of the bridge diagonal switches (S_1 and S_3 or S_2 and S_4) are turned on, and the inductor current flows through the transformer to the load. It can be seen that the instant t_2 controls the power flow to the output and, therefore, regulates the output voltage.

Case 2: $p_{in} < P_o$, see Fig. 2.9(b)

In this case, the boost converter and the top forward converter are operating separately. The isolated boost converter controls the input current and the forward converter regulates the output voltage.

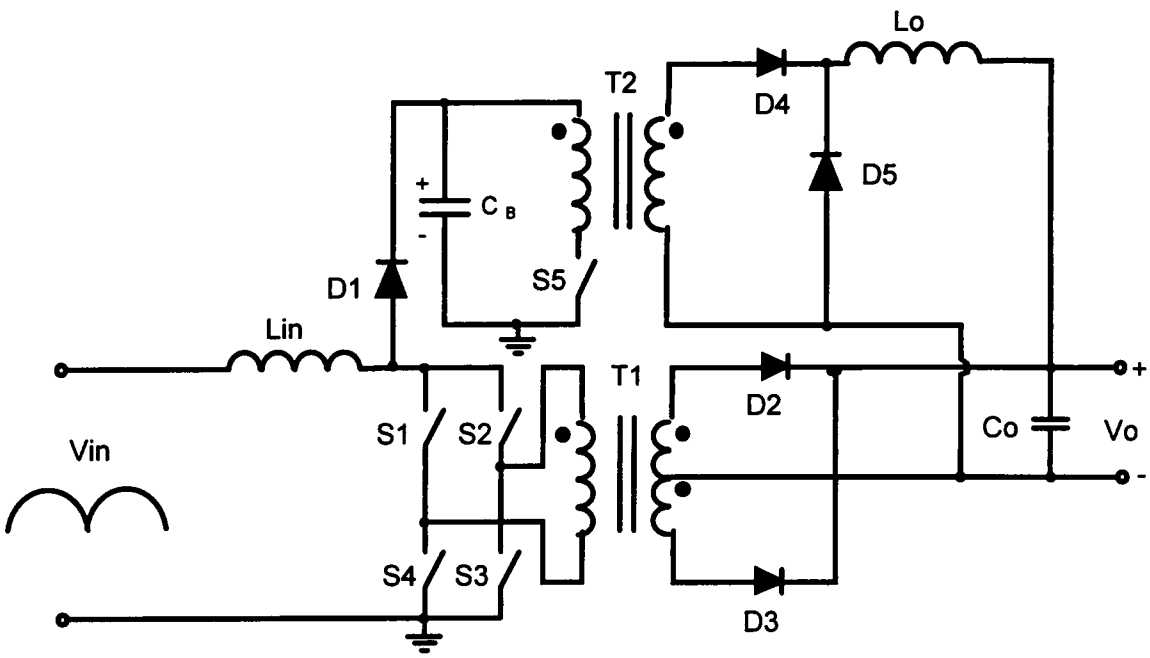


Fig. 2.8 PPFC Converter 2 implementing PPFC Scheme 2.

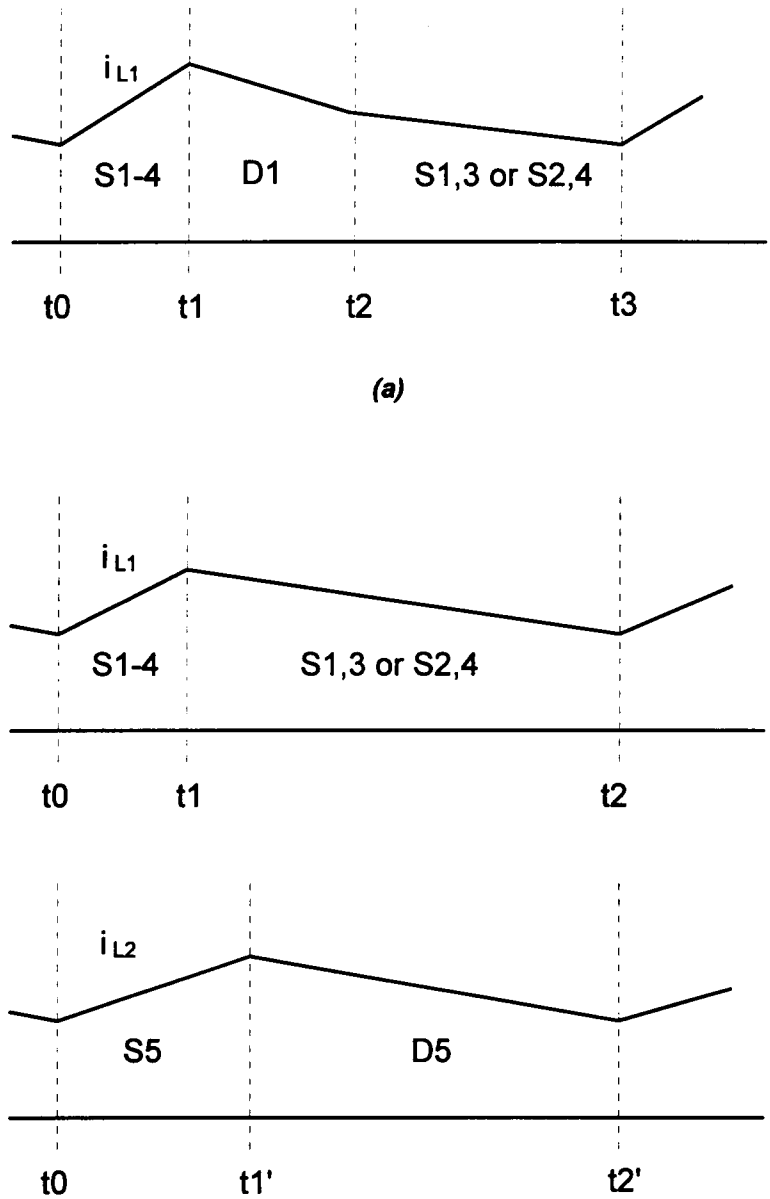


Fig. 2.9 Operation waveforms of PPFC converter 2

(a) $P_{in} > P_o$; (b)$P_{in} < P_o$.

2.3.3 PPFC Scheme 3 and PPFC Converter 3

PPFC scheme 1 and 2 above are essentially good for high power applications because of the use of two isolation transformers. For most of the single-phase applications, the power levels are below 1-2 kW, and two isolation transformers seem too complex and expensive. Scheme 3 shown in Fig 2.10 simplifies the system by confining 32% second-time power processing on the output end, so that only stage 1 needs an isolation transformer.

The drawback of doing this is that the bulk capacitor has to sit on the low voltage end (most single-phase applications need low voltage output), which yields significantly bigger bulk capacitor size than the high voltage bulk capacitor for the same energy storage capability.

The bi-directional operation of stage 2 does not complicate the circuit, since it is a non-isolated topology.

An example circuit implementation of PPFC scheme 3 is given in Fig. 2.11 as PPFC converter 3. Stage 1 is an isolated boost converter, and stage 2 is a bi-directional boost/buck converter. The operation is quite straightforward. The isolated boost converter controls the input current, and the bi-directional boost/buck regulates the output voltage. A major problem of this converter is that the transformer leakage induces voltage spikes on the bridge switches.

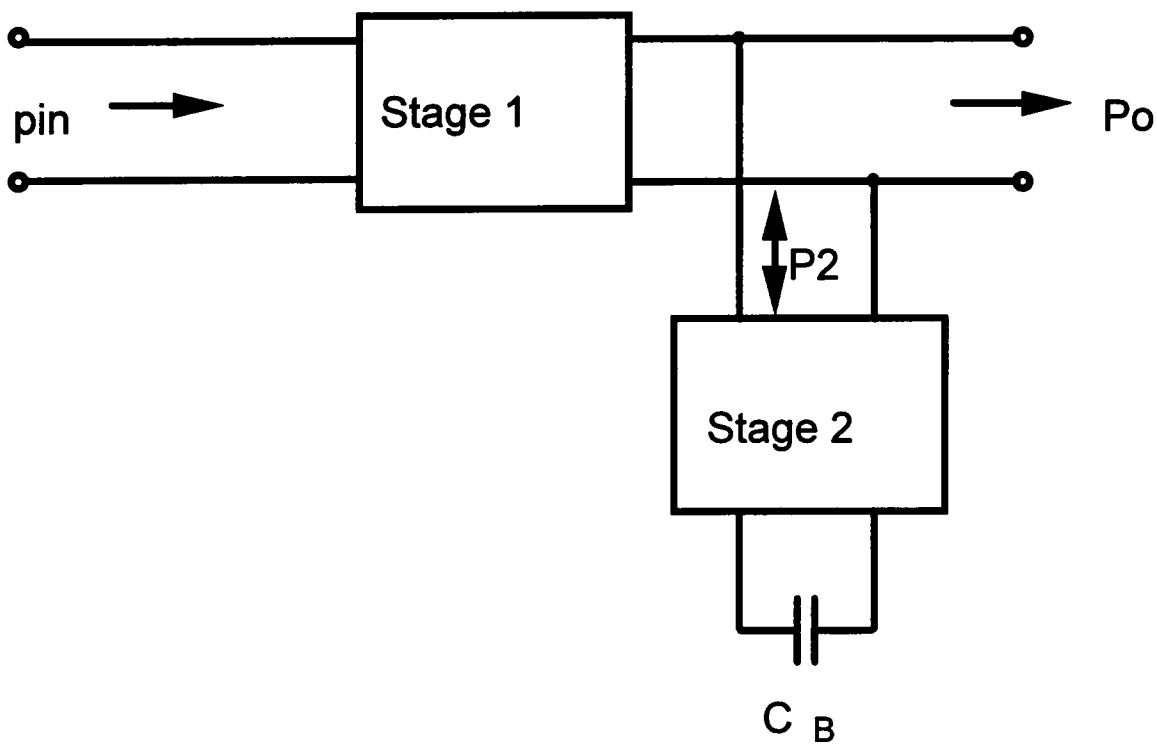


Fig. 2.10 PPFC scheme 3.

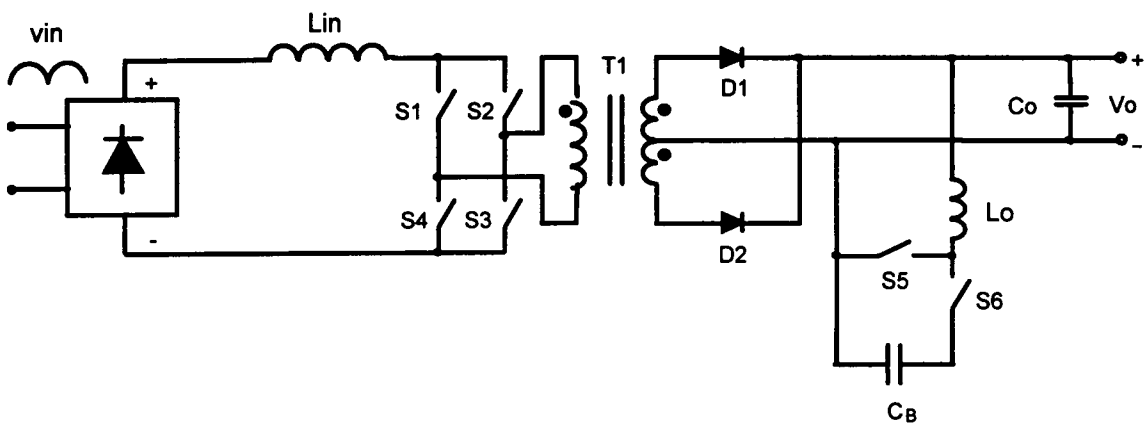


Fig. 2.11 PPFC Converter 3 implementing PPFC Scheme 3.

2.3.4 PPFC Scheme 4 and PPFC Converter 4, 5, and 6

Another way of using only one isolation transformer is PPFC scheme 4 shown in Fig. 2.12. Here, the bulk capacitor is still on the high voltage side and only one power stage is used. This power stage will process both the full input power and the second-time 32% power. Therefore, it is proposed for power levels lower than PPFC schemes 1 and 2 and could fit most single-phase applications.

Based on PPFC scheme 4, several single-stage PPFC converters can be constructed. Two single-stage flyback PPFC converters and one single-stage boost PPFC converter are being introduced in the following.

2.3.4.1. Single-Stage Flyback PPFC Converters

The flyback converter has been recognized to be quite suitable for relatively low power levels of below 200-300 W, since it is the simplest circuit with isolation, step-up/down conversion ratio, soft-start up and overload protection. However, the conventional flyback PFC converter has the bulk capacitor at the output and does not provide tight output regulation. By applying the PPFC concept, this drawback can be overcome. The first single-stage flyback PPFC converter, called PPFC converter 4 is shown in Fig. 2.13. It is obtained by adding an auxiliary network composed of S_2, S_3, and C_b to the normal flyback converter. This auxiliary network controls the power flow to achieve the output regulation. The operation is explained below.

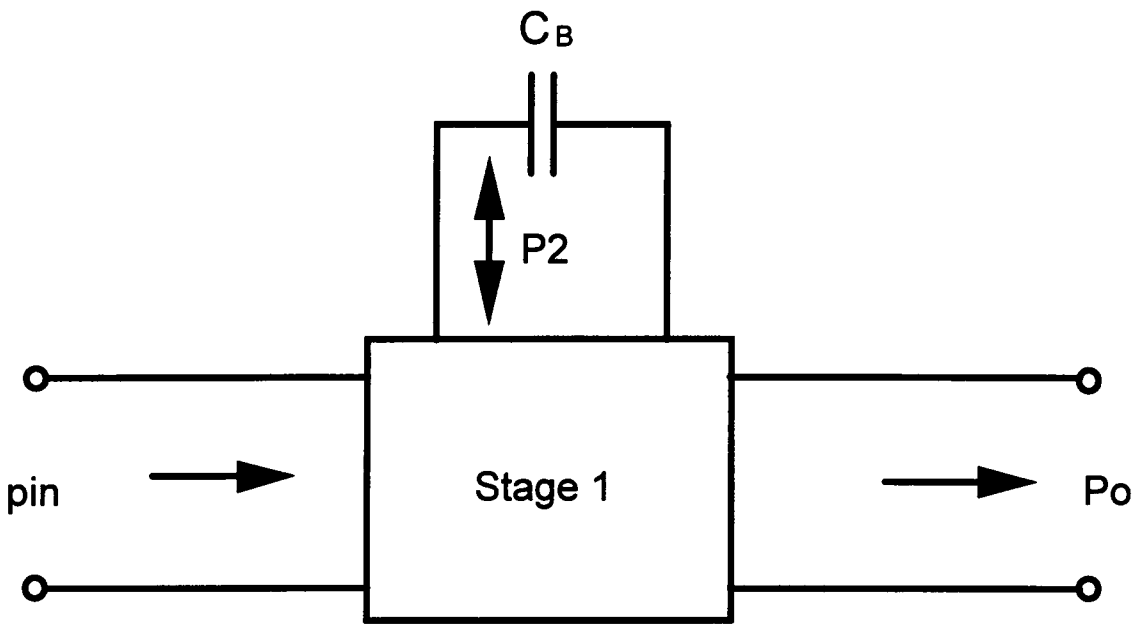


Fig. 2.12 PPFC scheme 4 - single-stage PPFC scheme.

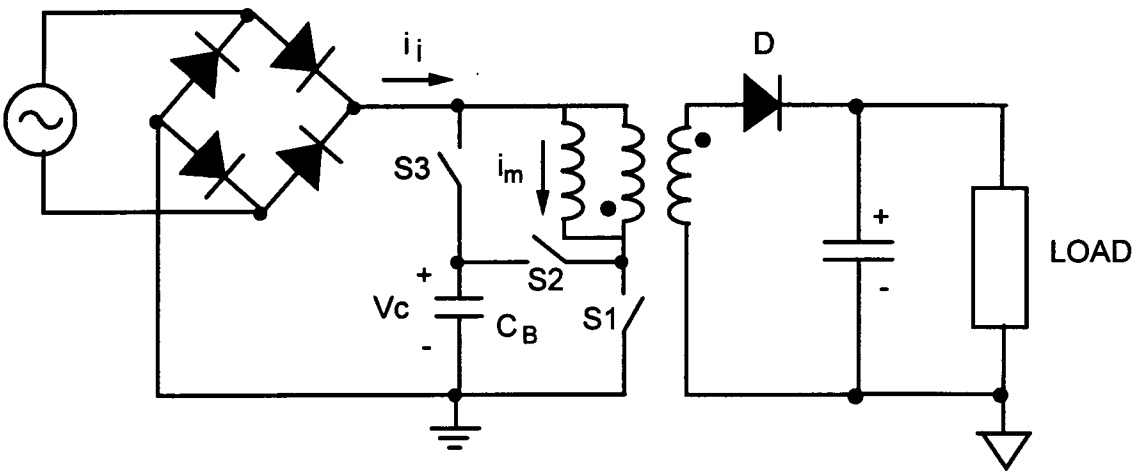
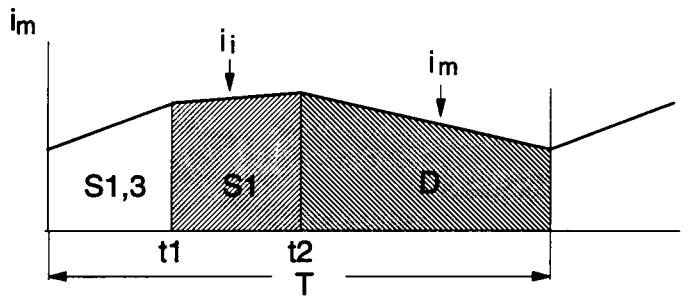


Fig. 2.13 PPFC converter 4 - Single-stage flyback PPFC converter 1.

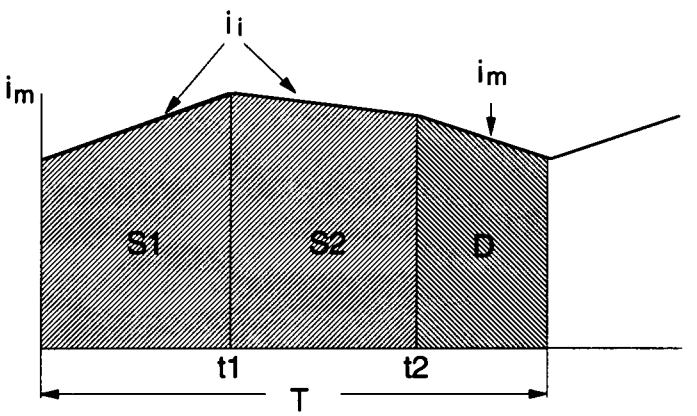
The control waveform for $p_{in}<P_o$ is given in Fig. 2.14(a). At the beginning of a switching cycle, both S_1 and S_3 are turned on, and the bulk capacitor is charging the flyback inductor which is the magnetizing inductor of the flyback transformer. This period corresponds to releasing energy from the bulk capacitor, and, obviously, the time instant t_1 at which the S_3 is turned off can be used to regulate the output voltage. After S_3 is turned off at t_1, the flyback inductor current of the transformer follows from the input until the S_1 is cut off at time t_2. Therefore, the time instant t_2 can be adopted to control the input current for the PFC purpose. After t_2, the flyback inductor releases its stored energy to the output with no current in any primary switch.

The control waveform for $p_{in}>P_o$ is given in Fig. 2.14(b). In this case, S_3 will remain off, since there is no need to release any energy from the bulk capacitor. At the beginning of a switching cycle, S_1 is turned on, and the input voltage is charging the flyback inductor until t_1 when S_1 is turned off. After S_1 is turned off, S_2 conducts, allowing the current to flow into the bulk capacitor, which stores the excessive energy. At time t2, S2 is turned off; the flyback inductor release its stored energy to the output. The input current can be controlled by the time instant t_1, while the output voltage can be regulated by the time instant t_2.

Another drawback of the flyback converter is the larger transformer leakage, which requires active clamping and is the major factor limiting the flyback converter power handling capability. The second single-stage flyback PPFC converter, also implementing PPFC scheme 4 is shown in Fig. 2.15 and called PPFC converter 5. It is obtained from the normal flyback converter by adding an auxiliary network composed of D, S_3, and C_b, and a secondary switch S_2. Due to the diode D, the voltage on the main switch will be clamped to the bulk capacitor voltage, eliminating the leakage problem and allowing higher power handling capability of the flyback converter.



(a)



(b)

Fig. 2.14 Operation waveforms of PPFC converter 4

(a) $p_{in} < P_o$; (b) $p_{in} > P_o$

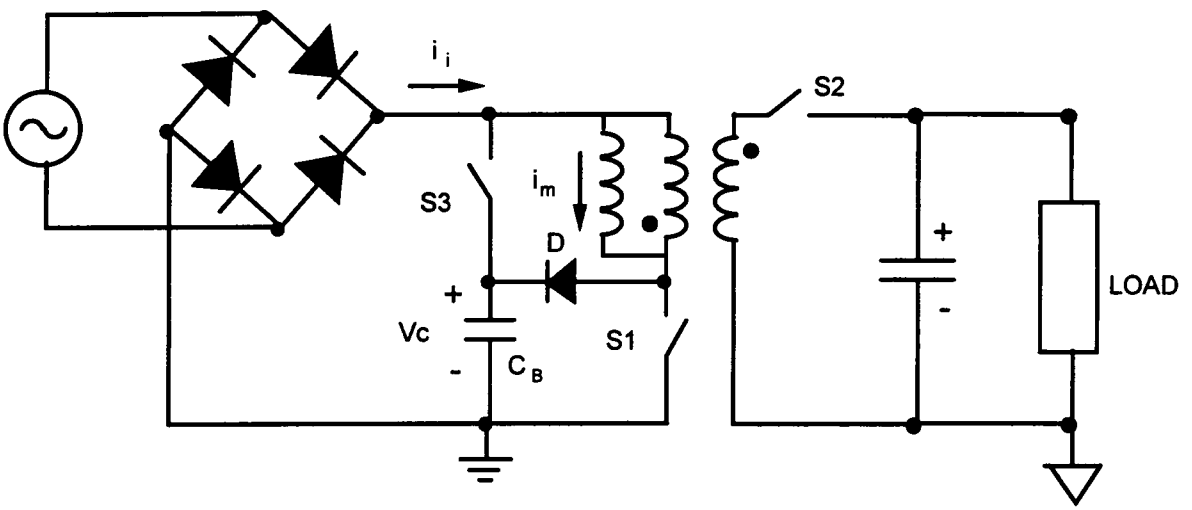


Fig. 2.15 PPFC converter 5 - Single-stage flyback PPFC converter 2.

The control waveform for $p_{in}<P_o$ is drawn in Fig. 2.16(a). The operation in this period is exactly the same as in PPFC converter 4.

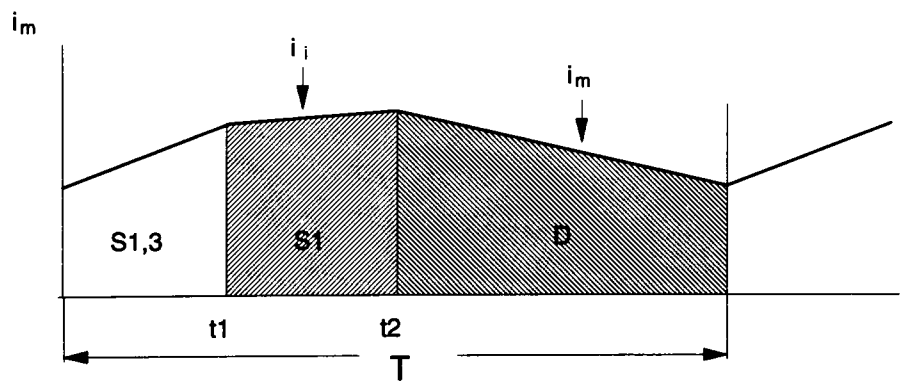
For $p_{in}>P_o$, the control waveform is given in Fig. 2.16(b). The first period, when S_1 is on, is the same as that in PPFC converter 4. At time t_1, S_1 is turned off and S_2 conducts, sending energy to the load. At time t_2, S_2 is turned off, forcing flyback inductor current to flow into the bulk capacitor and storing excess input energy. One can use time instant t_1 to control the input current, and time instant t_2 to regulate the output voltage.

It needs to mention that the bulk capacitor voltage must be properly designed to ensure the proper power flow. In PPFC converter 4, the bulk capacitor voltage must be designed higher than the input rms voltage and lower than the input rms voltage plus the reflected output voltage; in PPFC converter 5, the bulk capacitor voltage must be designed higher than the peak input voltage plus the reflected output voltage. Concerning the flyback transformer leakage problem, the PPFC converter 5 would be more attractive than the PPFC converter 4.

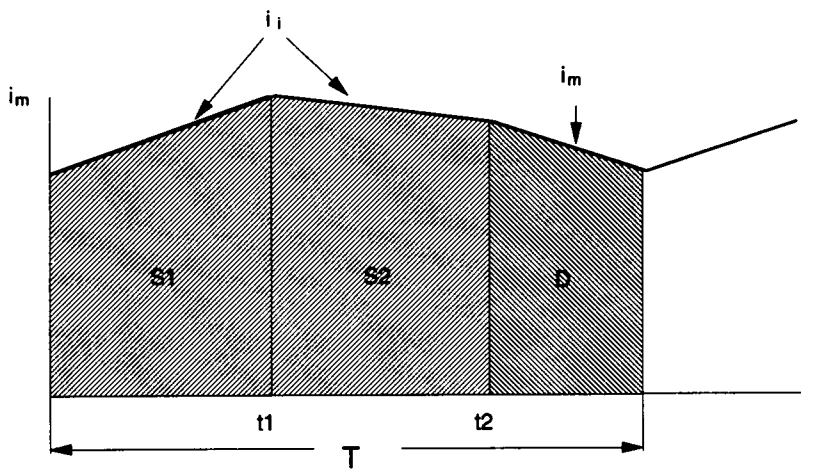
There are many high power applications for which isolated boost converters are more suitable than the flyback converter for its less voltage and current stresses on the switches.

2.3.4.2. Single-Stage Boost PPFC Converter

The single-stage boost PPFC converter, PPFC converter 6 based on PPFC scheme 4 is shown in Fig. 2.17, where a full-bridge boost converter is adopted as the power stage, and an auxiliary network (D_1, C_B and S_5) is added on the primary side.



(a)



(b)

Fig. 2.16 Operation waveforms of PPFC converter 5

(a) pin < Po; (b) pin > Po.

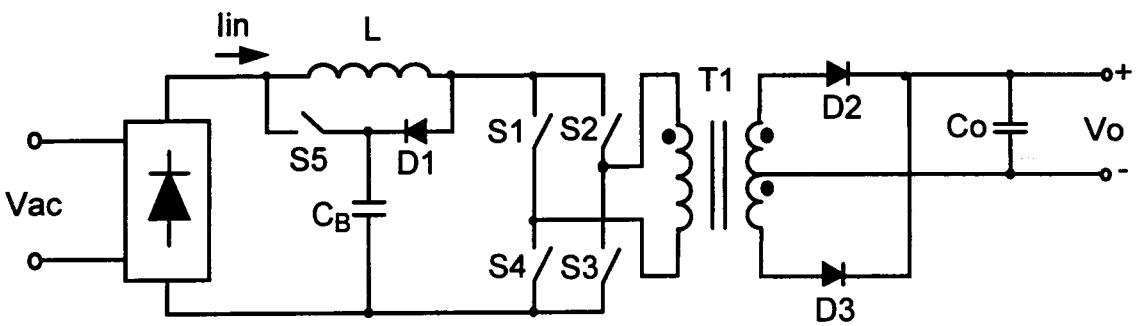
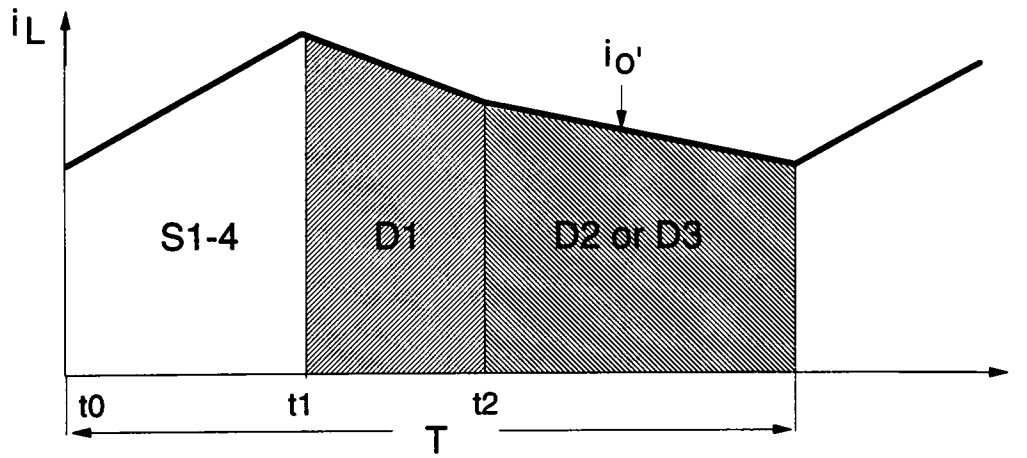


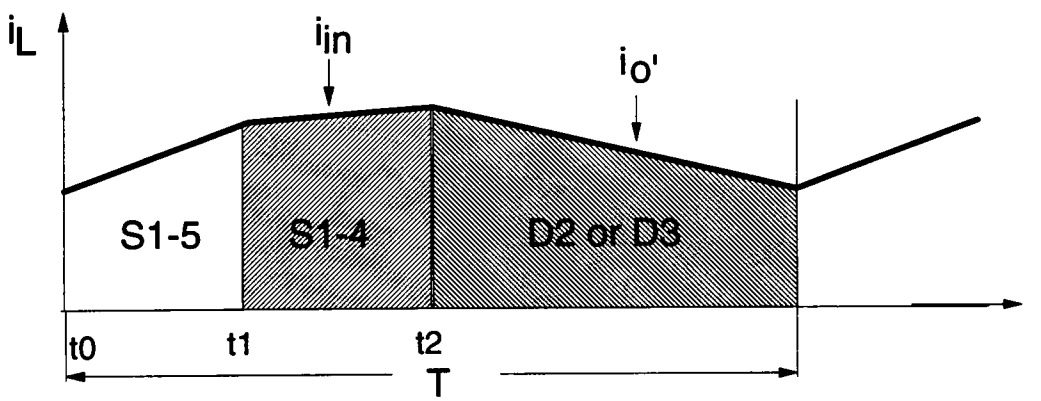
Fig. 2.17 PPFC Converter 6 - single-stage boost PPFC converter.

For $P_{in} > P_o$, the operation waveforms are shown in Fig. 2.18(a). In this case, S_5 does not run at all. At the beginning of a switching cycle t_0, all four boost switches (S_1 - S_4) are turned on, charging the boost inductor with the input voltage. At time t_1, all four bridge switches are turned off, sending energy to the bulk capacitor through diode D_1 and discharging the boost inductor. At time t_2, one pair of the diagonal switches are turned on again, delivering energy to the load through the transformer. Instant t_1 controls the input current just as in a typical boost PFC circuit; instant t_2 regulates the output voltage. Here, the input PFC control and the output regulation are essentially independent, provided that the inductor current discharging slops of the two discharging intervals are not very different. In this case, the inductor current is the input current.

For $P_{in} < P_o$, the operation waveforms are shown in Fig. 2.18(b). At the beginning of a switching cycle t_0, all five switches are turned on, allowing the bulk capacitor to charge the inductor. The input current stays at zero, since the bulk capacitor voltage is higher than the peak of the input AC voltage. The turn-off instant of S_5 (t_1) is determined by the output voltage controller, while the turn-off instant of one pair of the bridge diagonal switches (t_2) is governed by the input current controller. Assuming that S_5 is turned off earlier than the turn-off of the bridge diagonal switches, as seen in Fig. 2.18(b), the inductor current becomes the input current after t_1. Since the input voltage at this moment is low, the inductor current charging slop is quite flat. At time t_2, one pair of the diagonal bridge switches are turned off, so that the inductor current flows to the output through the transformer. The discharging slop after t_2 is determined by the difference between the input voltage and the transformer primary reflected output voltage. It is noticed that a slight distortion will occur at the region near the zero input voltage, since the input current will not be zero due to the operation of S_5. However,



(a)



(b)

Fig. 2.18 Operation waveforms of PPFC converter 6

(a) Control for $p_{in} > P_o$; (b) Control for $p_{in} < P_o$.

analysis in Appendix A proved that this only occurs in a very narrow region and does not deteriorate the power factor. This will also be seen in the experimental results.

The advantages of this boost PPFC converter will be seen in the next chapter, where hardware test results will be reported and comparison with the conventional two-cascade-stage system will be made after employing a new soft-switching technique.

2.4 Conclusions

In this chapter, a novel single-phase PFC concept, the parallel power factor correction, is proposed. With this concept, both power factor correction and tight output regulation can be achieved. One distinct advantage of the proposed schemes is that 68% of input power being delivered to the output through only one power stage. Several PPFC schemes and circuit implementations are also presented. Schemes 1 and 2 are for high power applications. Compared with the conventional two-cascade-stage scheme, they involve one more isolation transformers but may be justified by higher efficiency feature and the fact that multi-modules in parallel may be needed in two-cascade-stage scheme. Schemes 3 and 4 are more suitable for most single-phase power levels than schemes 1 and 2 since only one isolation transformer is employed. An advantage of scheme 4 is that only one power stage is required to perform the task of the conventional two stage system. A drawback of scheme 4 is the coupling between the two fast control loops, the input current loop and the output voltage loop. This complicates the control design and requires further investigation of the small-signal behavior. Another drawback of the boost PPFC converter is that a pulsating input

current occurs when S_5 operates. For all the PPFC converters proposed here, a common disadvantage is the relatively poor performance when dealing with wide input voltage which requires wide variation of the switch duty-ratio, leading to poor transformer performance.

In the next chapter, experimental results and evaluation analysis will be given to show the advantages of the PPFC technique over the conventional two-cascade-stage technique for certain applications.

Chapter 3

Experimental Verification and Evaluation of PPFC Technique

3.1 Introduction

The PPFC concept and several implementation schemes were introduced in Chapter 2. In this chapter, experimental and analytical evaluation results will be given to verify the advantages of the proposed PPFC converters through comparison with conventional two-cascade-stage systems.

The conversion efficiency is one of the major aspects of the comparison. From a practical concern, the converter efficiency depends on not only the converter topology but also the soft-switching techniques, since switching losses are quite significant for high frequency operation. For example, in the conventional two-cascade-stage system, the ZVT technique is desired for the boost PFC converter to overcome the diode reverse recovery and the capacitive turn-on losses. Hence, for a fair evaluation of the PPFC converters, certain types of soft-switching techniques need to be considered as well.

In this chapter, a novel soft-switching technique will first be proposed, which is particularly effective for the isolated boost topologies used in PPFC converters. Then, the experimental results of PPFC converter 6, incorporating the new soft-switching technique, will be given, which verify the PPFC operation principle and show higher efficiency than the conventional two-stage scheme. To have a better understanding of

the PPFC technique, evaluations will be conducted by comparing the PPFC converters with the two-cascade-stage counterparts.

3.2 IGBT Soft-Switching in Isolated Boost Converters

In boost PPFC converters, the main power stage is an isolated boost converter. In the isolated boost converter, the rms currents of the active switches are quite high for high power applications, since the boost inductor current always flows through the active switches. Therefore, the conduction losses of those active switches will be one of the major concerns.

The Power MOSFET is the dominant device used in today's high-frequency switched-mode power converters due to its fast-switching characteristics. However, the MOSFET conduction loss equals to the square of its rms current multiplied by its on-resistance and will be significant in high voltage and high power applications, where both the current and the on-resistance are high. Although this limitation can be alleviated by paralleling a number of MOSFETs or several converter modules, such solutions are usually expensive and complex.

The IGBTs, on the other hand, have a very attractive feature; their on-voltage drops are insensitive to current magnitudes and device voltage ratings, yielding much lower conduction losses than the MOSFETs in high voltage and high power applications. Another advantage is that they are much less expensive than the comparable power MOSFETs. However, such minority carrier devices have poorer switching

characteristics than the MOSFETs, and, especially, their turn-off current tails produce significant switching losses.

To take advantage of the low conduction loss and low cost of IGBTs while operating them at higher switching frequencies, it is necessary to implement certain types of soft-switching techniques to reduce the switching losses.

Zero-current-switching (ZCS) and zero-voltage-switching (ZVS) techniques can greatly alleviate the IGBT turn-off problem. However, since they rely on the resonance of either parasitic or external resonant components, the device voltage or current stresses will be higher than the PWM counterpart, and quite often the soft-switching range is limited. In this section, a unique IGBT soft-switching technique will be proposed for the isolated boost converters, which does not involve any resonant process and is guaranteed under any operating conditions.

3.2.1 Mixed Device

More than a decade ago, several types of combination power devices were proposed [D-17]. One of them is the parallel device configuration, here referred to a mixed device. The mixed device configuration is the fundamental concept of the device-based soft-switching technique and, therefore, will be introduced first. Further developments based on the mixed device concept will then be proposed for the bridge-type isolated boost converters.

The idea of the mixed device is to take advantages of the superior switching characteristic of the fast devices, such as the MOSFETs, and the better conducting property of the slow minority carrier devices, such as the IGBTs. A mixed device, as

shown in Fig. 3.1(a) consists of a MOSFET in parallel with an IGBT so that the MOSFET is in charge of the switching transients, while the IGBT carries the major current during normal conduction periods. Its driving signals are shown in Fig. 3.1(b). The operation principle is that the turn-on and the turn-off of the IGBT always occurs when the parallel MOSFET is on, which allows the IGBT to be turned on and off under zero voltage condition.

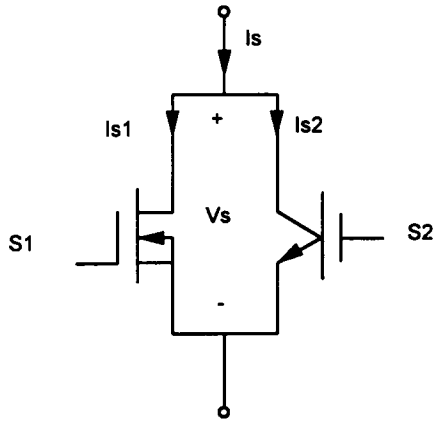
The detailed operation of the mixed device is explained in the following.

1. Turn-on transient t_0 - t_1:

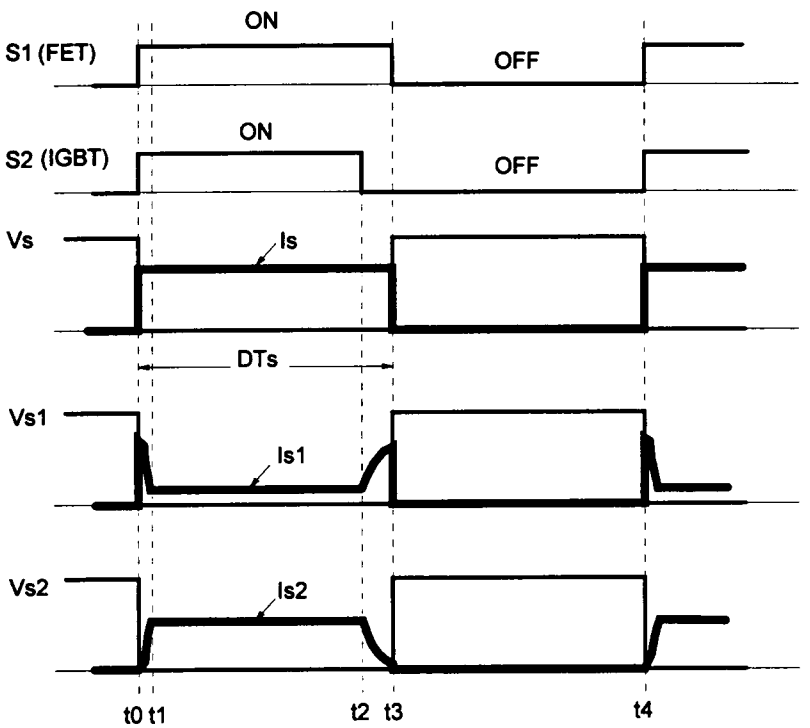
At t_0, both S_1 and S_2 are turned on. Due to the fast switching of S_1, most of current I_s goes through S_1 first. Then I_{s2} builds up, and after a short period rise time, t_r of S_2, most of I_s flows through S_2, due to its lower on-voltage drop. This is a soft turn-on process for S_2, which reduces its turn-on loss. The steady state on-voltage of the mixed device is essentially determined by S_2.

2. Turn-off transient t_2 - t_3:

At t_2, S_2 is turned off while S_1 remains conducting. The current I_{s2} decreases and I_{s1} increases. After a period of turn-off time determined by the current tail time of S_2, I_{s2} becomes very small and I_{s1} is almost equal to I_s. This realizes a lossless turn-off for S_2. At t_3, S_1 is turned off. If the gate-drive current is high enough, the turn-off of MOSFET S_1 can be negligible. Both S_1 and S_2 stay off until t_4 when the next switching cycle begins.



(a)



(b)

Fig. 3.1 Soft-switching of IGBTs with mixed device

(a) Mixed device; (b) Control signal of the mixed device.

It can be seen that this mixed device combines the advantages of both the MOSFET and the IGBT, i.e., it features both low switching loss and low conduction loss. It can replace the active switch(es) in any switched-mode power converters.

Unlike the most frequently used circuit-based soft-switching techniques reviewed in Chapter 1, this device-based soft-switching technique does not involve any circulating energy.

As stated above, IGBTs show advantages over MOSFETs for relatively high power applications, where the bridge-type topologies are often adopted. A clear drawback of the above introduced soft-switching technique is that it requires an auxiliary MOSFET for each IGBT. Then, in a full-bridge converter, four auxiliary MOSFETs are required. This makes the converter too complicated and less attractive in practice. In the following section, several new soft-switched IGBT converters are proposed which easily implement the device-based soft-switching technique.

3.2.2 Device-Based Soft-Switching in Isolated Boost Converters

The mixed device is obtained based on the device only. However, from the circuit point of view, the same concept can be implemented much easier in the isolated boost converters. In this section, two isolated boost converters with soft-switched IGBTs are proposed, which are suitable for PFC applications.

3.2.2.1. Full-Bridge IGBT Boost Converters

A. Four IGBTs + one FET

The proposed circuit is shown in Fig. 3.2 (a), where the main power switches (S_1 - S_4) are IGBTs, and the auxiliary switch S_5 is a MOSFET. With the help of S_5, soft turn-off can be achieved for all four IGBTs. The control signals are given in Fig. 3.2 (b).

Operation principles:

1. t_0 - t_1:

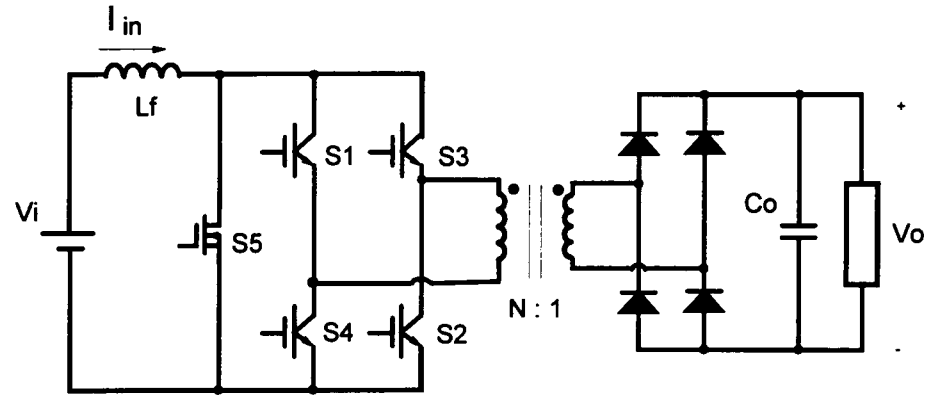
Prior to t_0, all five IGBTs (S_1 - S_5) are conducting, corresponding to the boost inductor charging period. S_3 and S_4 are turned off at t_0. Since S_5 is still on, most of the input current, I_i, is transferred to S_5. The voltage across S_3 and S_4 is almost zero (actually the on-voltage of S_5). This results in zero-voltage turn-off for S_3 and S_4, which is essentially lossless.

2. t_1 - t_2:

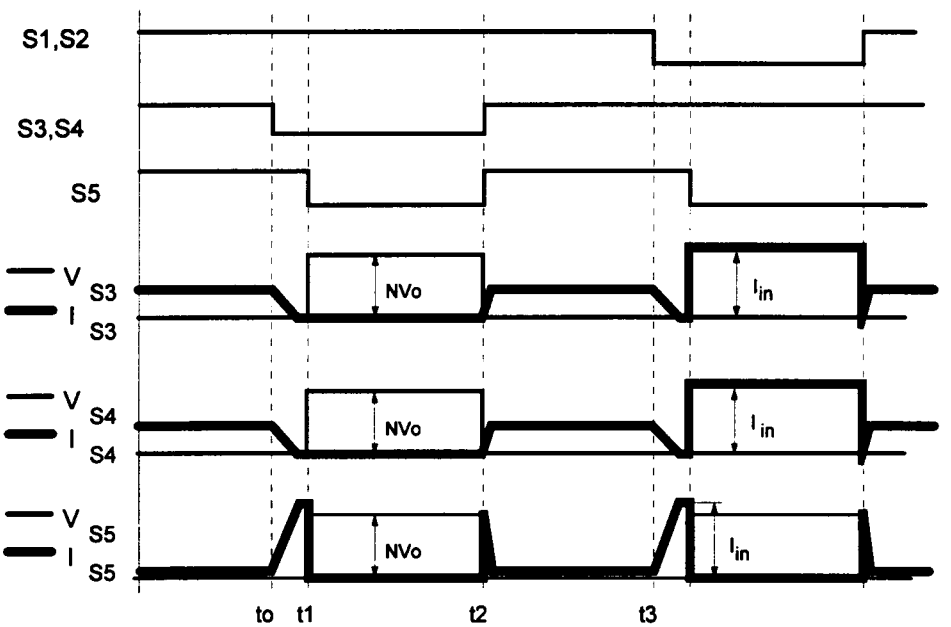
At t_1, after S_3 and S_4 are fully turned off, S_5 is turned off, and the full current, I_i, must flow through IGBTs S_1 and S_2, while the power is transferred to the load through the transformer, corresponding to the boost inductor discharging period.

3. t_2 - t_3:

At t_2, all five switches (S_1 - S_5) are turned on. This initiates the boost inductor charging period. At t_3, S_1 and S_2 are turned off, starting the other half switch cycle which is symmetrical to the first half.



(a)



(b)

Fig. 3.2 Soft-switched IGBT full-bridge isolated boost converter
(a) Four IGBTs + One FET Boost Converter; (b) Control waveforms of the Four IGBTs + One FET Boost Converter.

B. Two IGBTs + Two FETs

Figure 3.3 (a) shows a full-bridge boost converter, where S_1, and S_4 are IGBTs, and S_2 and S_3 are MOSFETs.

Compared with the circuit in Fig. 3.2 (a), it has fewer power switches, but there are two MOSFETs in the main power path; thus the conduction loss will be higher. However, if compared with a conventional four-MOSFET circuit, these two IGBT replacements have their distinct benefits.

The operation waveforms are given in Fig. 3.3 (b), and are explained in the following.

1. t_0 - t_1:

Initially, all S_1 - S_4 are conducting. At t_0, the IGBT S_4 is turned off. Then the currents in S_1 and S_4 reduce quickly and becomes very small after a short period of turn-off time of S_4. Since S_2 and S_3 are conducting during this time interval, the voltage across S_4 stays very low, and thus the turn-off of S_4 is a lossless zero-voltage switching process.

2. t_1 - t_2:

At t_1, S_3 is turned off with full conducting current I_i. As long as the gate drive is strong enough to overcome the "miller" effect, the turn-off loss of S_3 is minimum. After S_3 stops conducting, the full current I_i flows through S_1, S_2, and the transformer. This corresponds to the boost inductor discharging period.

3. t_2 - t_3:

At t_2, all four switches are turned on. Because of the fast switching nature of MOSFETs, most of the current I_i first goes through S_2 and S_3. Then the current I_i will divert to the path of S_1 and S_4 after a period of rise time t_r of the IGBTs. This is a soft

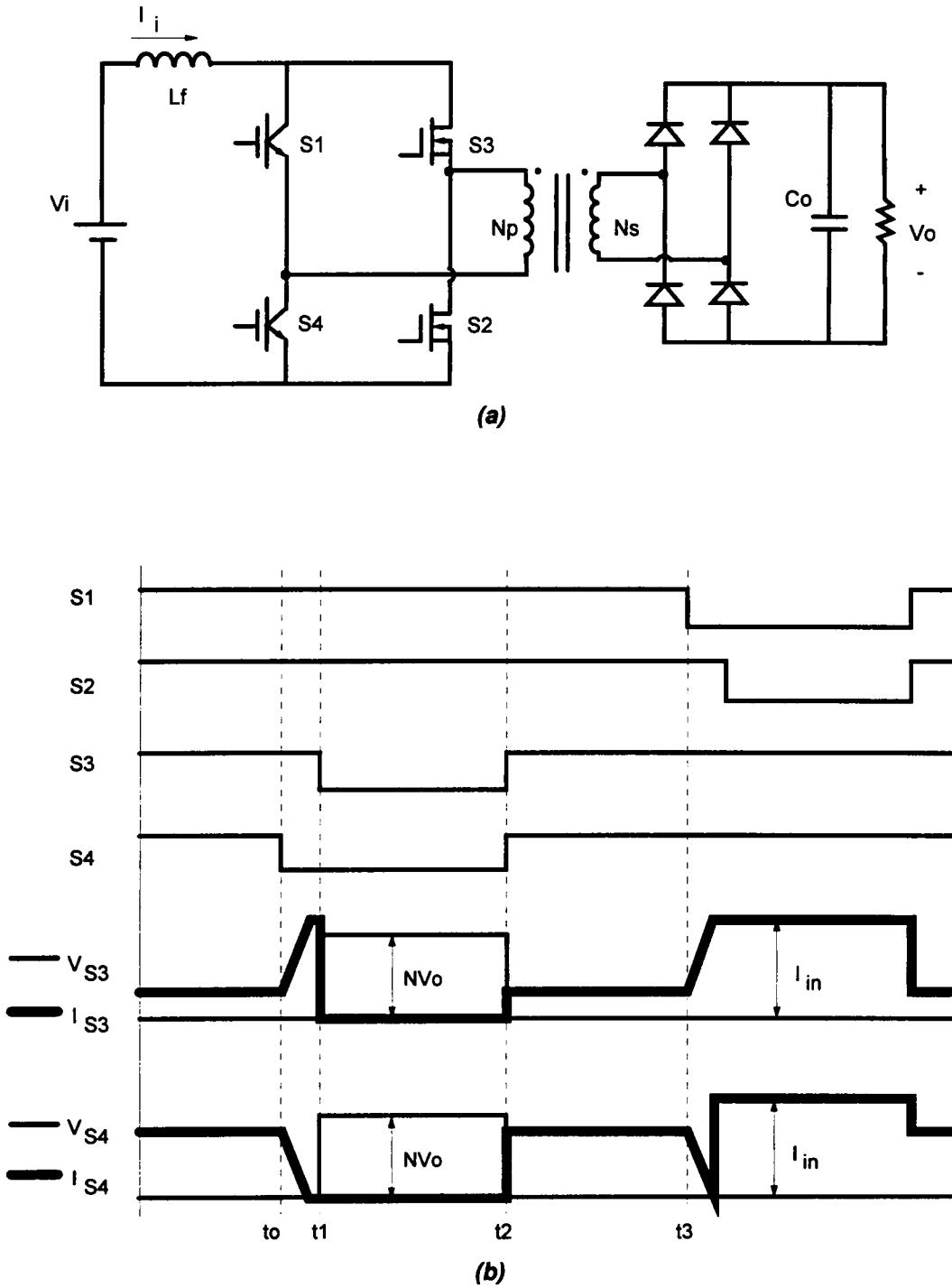


Fig. 3.3 Soft-switched IGBT/MOSFET full-bridge isolated boost converter (a) Two IGBTs + Two FETs Boost Converter; (b) Operation waveforms.

turn-on process for the IGBTs. At t_3, S_1 is turned off. This starts the other half of the switching cycle which is symmetrical to the first half.

3.2.2.2 Half-Bridge Boost Converter

The half-bridge boost converter with soft-switched IGBTs is shown in Fig. 3.4 (a), where the main power switches S_1 and S_2 are IGBTs, and the auxiliary switch S_3 is a MOSFET. The voltage stress of S_3 is half of that of S_1 and S_2.

The operation waveforms are shown in Fig. 3.4(b), which are very similar to the full-bridge boost converter case.

3.2.3 Experimental Results

To verify the methods proposed above, a half-bridge boost converter using two IGBTs and one FET as shown in Fig. 3.4 (a) was tested. Since this circuit is aiming at single-phase power factor correction, the reflected primary voltage has to be higher than the peak of the line voltage. For European line, it needs to be about 400V. Thus, the voltage rating of S_1 and S_2 needs to be 1000V. The output is regulated at 36 Vdc. The switching frequency is 75 kHz for each IGBT. Figures 3.5 (a),(b),(c) show the oscillographs for different MOSFET delay time (the time interval between t_0 and t_1 in Fig. 3.4 (b)).

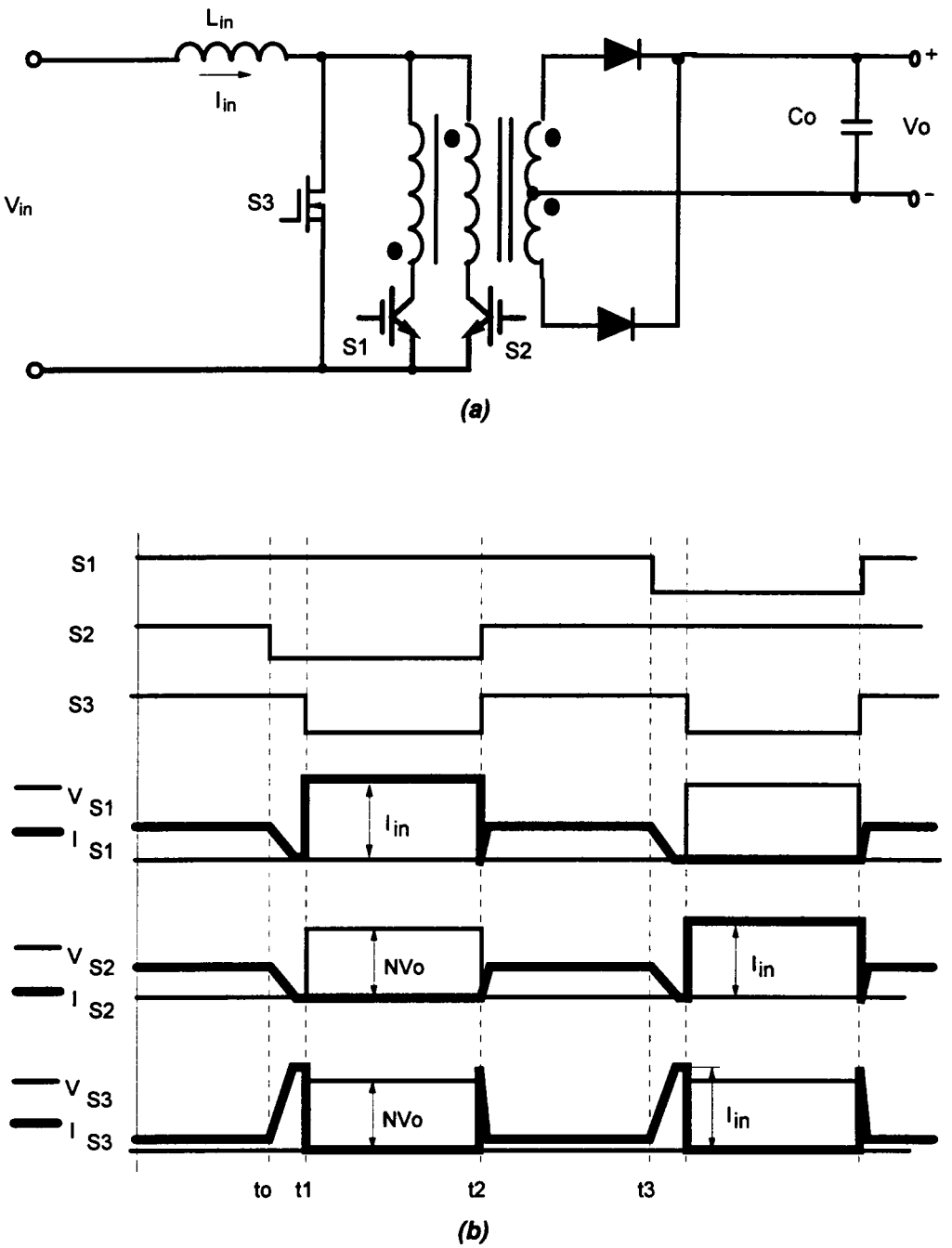
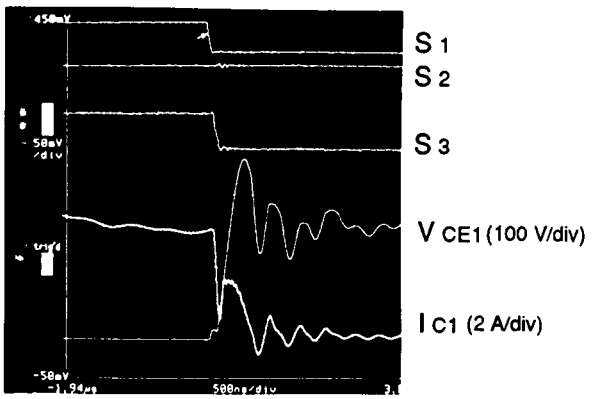


Fig. 3.4 Soft-switched IGBT half-bridge boost converter

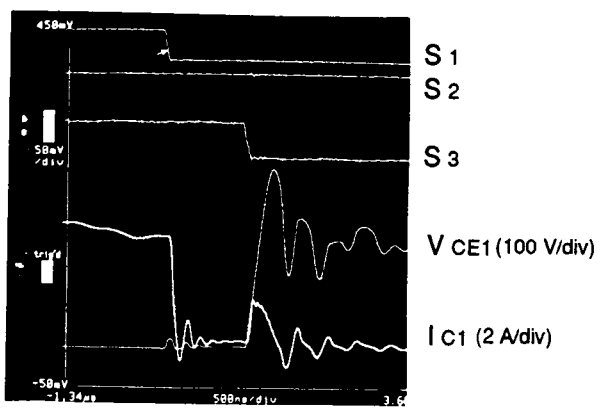
(a) Half-bridge IGBT boost converter; (b) Operation waveforms.

The efficiency measurements of the HB boost circuit are shown in Fig. 3.6. One can clearly see the turn-off current tail problem in Fig. 3.5 (a) with 0.1 μs delay of the MOSFET turn-off. This current tail causes severe turn-off loss, which can be seen from efficiency curve C in Fig. 3.6. In fact, the current tail problem has already been alleviated somewhat due to the 0.1 μs delay time which makes the current first drop to a low level and causes the voltage to stay low for a while. With 1 μs and 2 μs delays, as shown in Figs. 3.5 (b) and (c), the current tail was greatly reduced. It is important to note that under 2 μs delay, the current that appears while turning off the MOSFET is basically the current charging the IGBT junction capacitor.

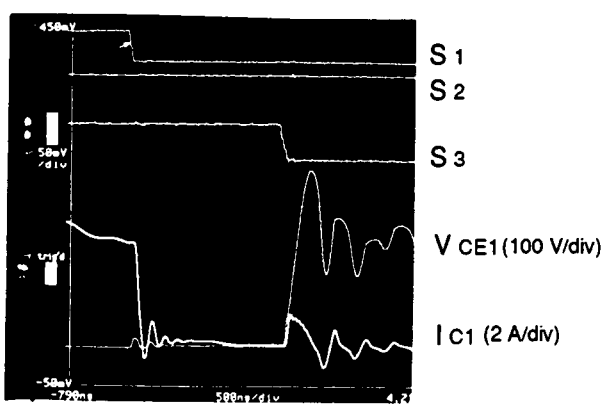
The current tail is a little larger under 1 μs delay, but is still much smaller than that with 0.1 μs delay. The efficiency curves for these two cases are curves A and B in Fig. 3.6. To see the advantage over MOSFET circuit, two MOSFETs are used for S_1 and S_2, and the efficiency is shown as the curve D. It is obvious that this IGBT soft-switching technique is very effective, and will be useful in high power applications.



(a) t_d = 0.1 μs

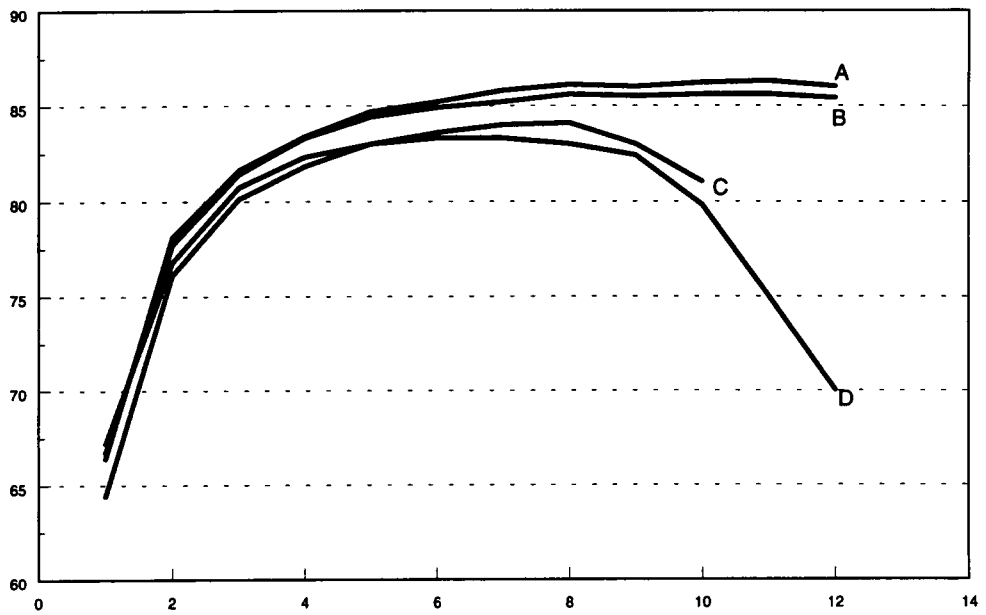


(b) t_d = 1 μs



(c) t_d = 2 μs

Fig. 3.5 Experimental Waveforms of the half-bridge Boost Converter.



A: Two IXYS IXGH25N100 + one IRFP450 with 2us delay

B: Two IXYS IXGH25N100 + one IRFP450 with 1us delay

C: Two IXYS IXGH25N100 + one IRFP450 with 0.1us delay

D: Two IRFP G40

Fig. 3.6 Efficiency measurements of the soft-switched IGBT the half-bridge boost converter.

3.3 Experimental Results of PPFC Converter 6 Using IGBTs

The experiment was carried out on PPFC converter 6 to verify the PPFC concept. The complete system diagram including the control unit is shown in Fig. 3.7. An auxiliary switch (MOSFET) is added to implement the MOSFET-helped IGBT soft-switching technique as explained in the previous section, due to the use of IGBTs as the main power switches for their lower cost and lower conduction losses.

Although the isolated boost converters can operate for universal input range, they have better performance for a narrow input range because of the transformer design. For a wide input range, under low input voltage, the boost duty-ratio will be quite large, leaving only a short period for transformer to deliver the power to the load. This yields much higher rms and peak current in the transformer and the secondary rectifiers, thus creates more losses. On the other hand, with a narrow input voltage range, the boost duty-ratio at the top of the input voltage can be designed quite small, and the transformer can deliver power during a large portion of a switching cycle.

In the experiment, the input voltage was designed to be the European line (185 Vrms - 265 Vrms); the switching frequency was set at 75 kHz. The major components used are listed below:

S_1 - S_4: GBC30U (IGBT); S_5: IRFP450 (MOSFET);

D_1: BYT79 500; D_2 and D_3: 10CTQ150;

L: 300 μH; C_B: 1000 μF (450 V);

C_o: 5000 μF (100 V).

Though the capacitance of the output capacitor is five times larger than the primary bulk capacitor, the major low-frequency energy ripple is still handled by the primary bulk capacitor, since its energy storage capacity at 400 V is much larger than that of the capacitor at 50 V.

There are three closed loops in the system, which are the bulk capacitor voltage loop, the input current loop, and the output voltage loop.

The bulk capacitor voltage loop is used to regulate the voltage of the bulk capacitor against line and load changes. This voltage was designed to be within 380V - 400V in this experiment. Due to the nature of the single-phase system, there is always a certain 120 Hz ripple voltage appearing on this bulk capacitor, and this voltage loop has to be designed slow enough so that the PFC function will not be disturbed. The output of the bulk capacitor voltage compensator multiplies with a signal proportional to the rectified input sinusoidal voltage and provides the input current reference for the input current compensator.

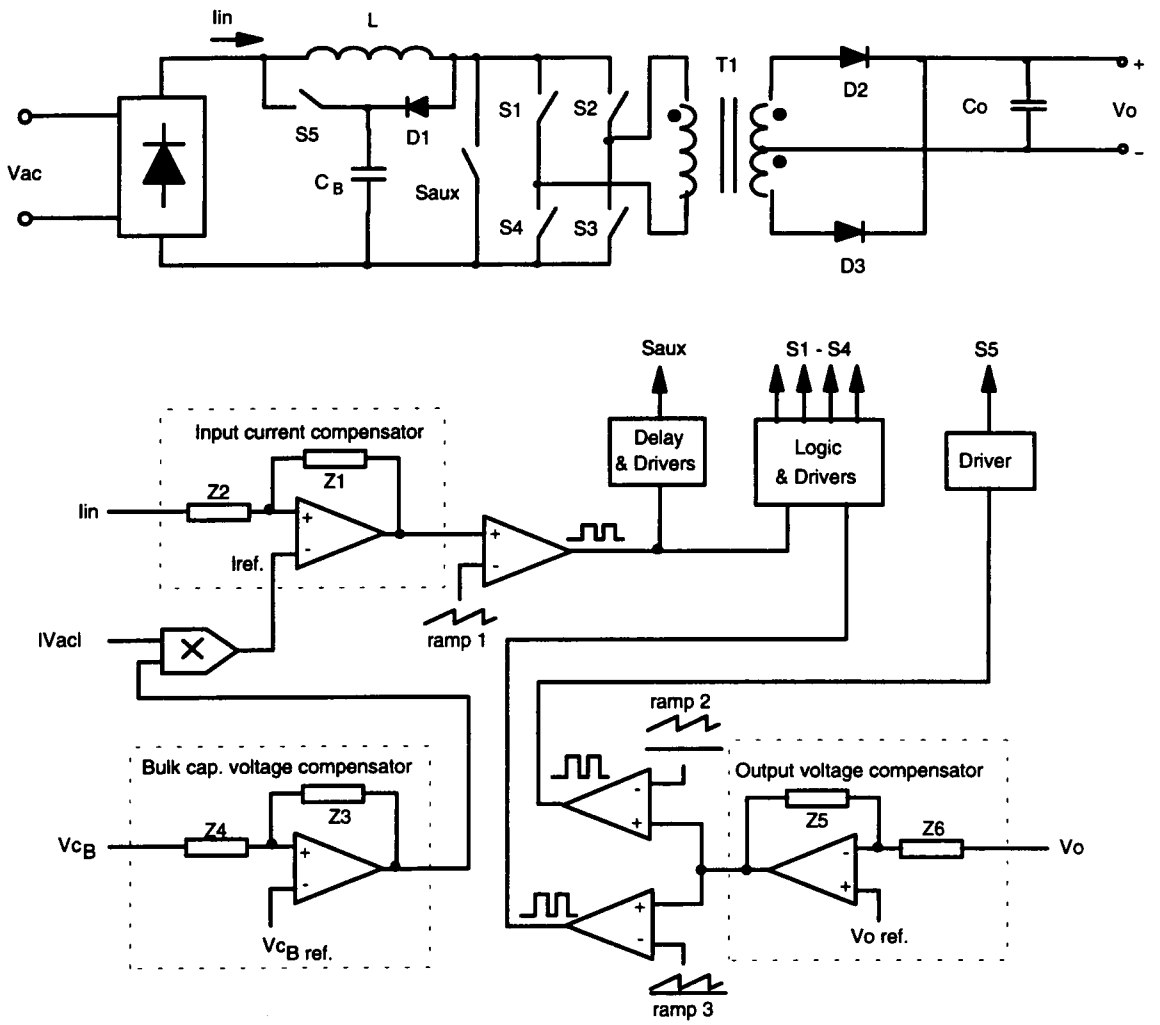


Fig. 3.7 Experimental system diagram of the single-stage boost PPFC converter.

The second loop is the input current loop. The input current compensator amplifies the error between the feedback input current and its sinusoidal reference, and its output compared with ramp 1 produces a PWM signal, which is essentially the boost duty-ratio. This signal regulates the input current to follow the reference. The input current loop has to be fast enough to achieve satisfactory input current control. Since the boost converter here is a four-switch full-bridge topology, the four drive-signals are produced from the original boost duty-ratio signal through certain logic components.

The above two loops work together as in a normal PFC controller.

The third loop is the output voltage loop. The output of the output voltage compensator is compared with two ramps (ramps 2 & 3) to control power follow. Ramp 2 is with certain DC bias and is on top of Ramp 3, as seen in Fig. 3.7. When the input power is not enough ($p_{in} < P_o$), the output voltage will drop and cause the output of the compensator to increase and intersect with ramp 2. The drive-signal S_5 is therefore obtained, which controls releasing energy from the bulk capacitor, corresponding to regulate the output voltage. On the other hand, when the input power is higher than the output power ($p_{in} > P_o$), the output of the compensator will intersect with ramp 3 and produces a signal to disable all bridge switches for a certain time during the boost switch off period, which delivers the extra energy into the bulk capacitor, corresponding to regulate the output voltage as well. For detailed operation, one can refer to Fig. 2.18.

Figure 3.8 shows the oscillograph of the experimental circuit. The top waveform is the drive signal of switch S_5, which occurs at the valley of the input voltage (the top-middle waveform), releasing energy from the bulk capacitor to the output. The bottom-middle waveform is the line current, which is in a nice sinusoidal shape and in phase with the line voltage, indicating good power factor correction. The bottom waveform is the output

voltage, which contains a slight low frequency ripple because there is no output current loop adopted in the test, and the voltage loop gain is practically limited.

Figure 3.9 gives the efficiency measurement obtained at 185 Vrms line and 40 Vdc output. The efficiency obtained at 1 kW is 93%.

The full-bridge boost converter used here is just one of several available isolated boost converters. Others can also be adopted, such as the half bridge version in Fig. 3.4(a), which would be a good choice to take advantage of the high voltage rating of IGBTs and will reduce cost and certain conduction losses.

From these results, one can see the advantage in terms of the efficiency since the conventional two-cascade-stage system, under the same situation, usually has the efficiency of 92% which is the product of the 97% efficiency of the first boost PFC stage and the 94% efficiency of the second DC/DC stage. A detailed comparison with the conventional two-cascade-stage system will be provided in the next section.

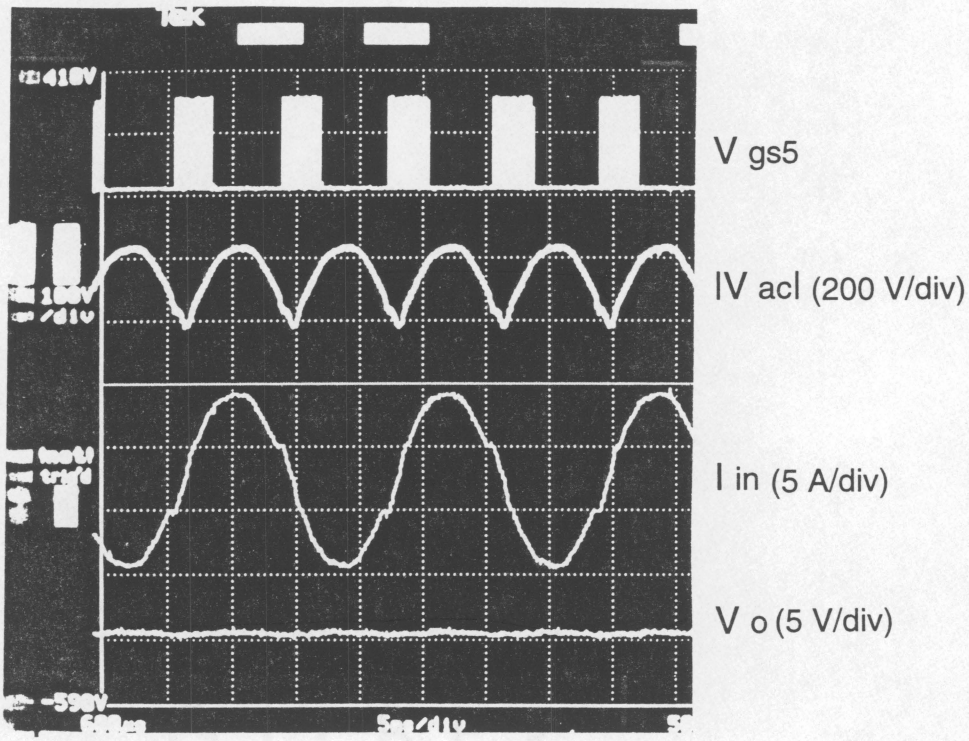


Fig. 3.8 Experimental Waveforms of the single-stage boost PPFC converter.

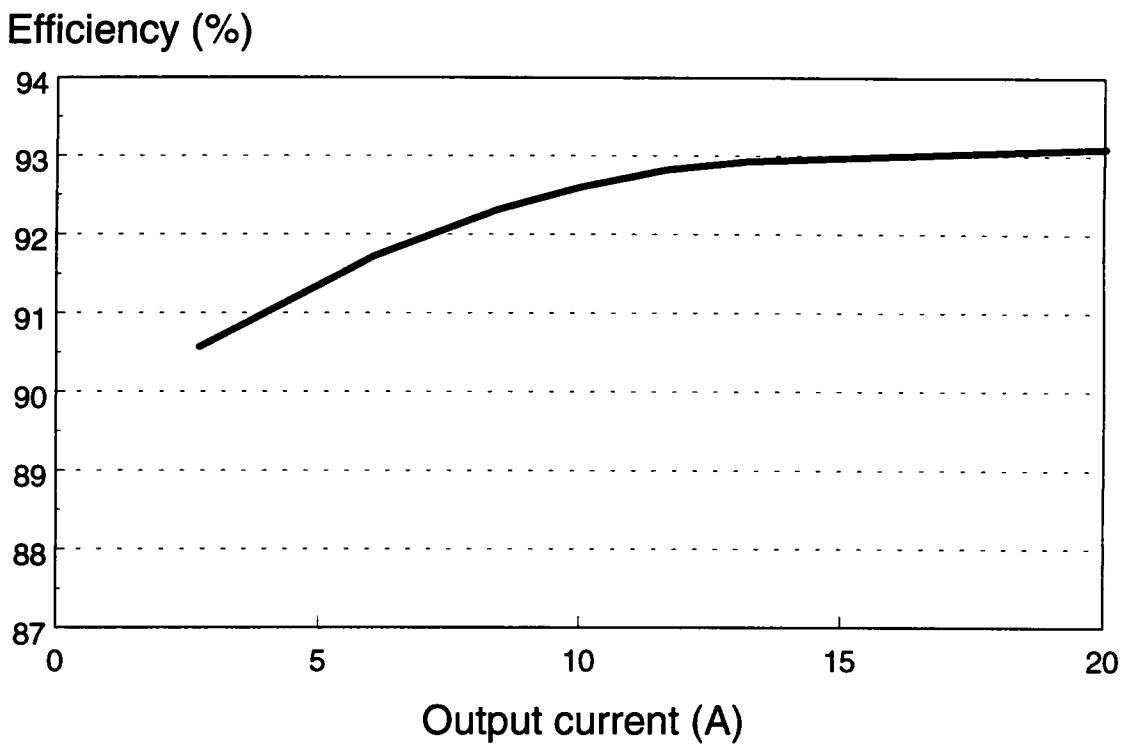


Fig. 3.9 Efficiency measurement of the single-stage boost PPFC converter.

3.4 Evaluation of the PPFC Technique

The evaluation will be made with a comparison between the PPFC converters and the conventional two-cascade-stage system, concerning cost, efficiency, and features. The PPFC boost converter (PPFC converter 6) will first be compared with the conventional two-cascade-stage system consisting of a single-ended PFC boost converter followed by a full bridge PWM buck converter. Then, the flyback PPFC converters will be compared with the conventional two-cascade-stage system of a single-ended boost PFC converter followed by a forward converter.

3.4.1 Evaluation of the Single-Stage Boost PPFC Converter

PPFC converter 6 with the IGBT soft-switching technique is drawn in Fig. 3.10. The conventional two-cascade-stage converter is drawn in Fig. 3.11, which is a single-ended ZVT boost PFC converter followed by a full-bridge PWM buck converter. The comparison will be carried out regarding cost and efficiency based on the following specifications:

V_{ac}=185 - 265 V; V_o=48 V; F_s=100 kHz; P_o=1 kW.

3.4.1.1 Power Components Count

The major components affecting the converter cost are the semiconductor devices and the magnetic devices. The number of the devices for these two converters are listed in Table 3.1.

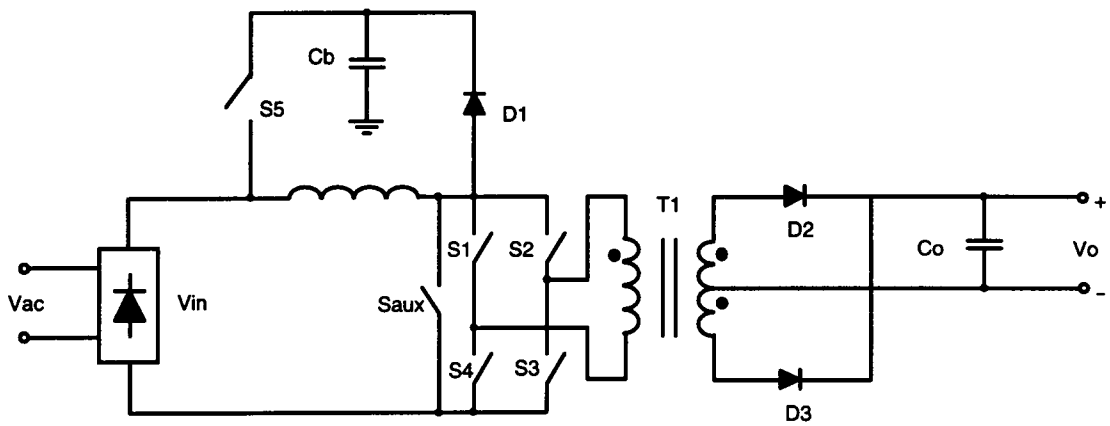


Fig. 3.10 Soft-switched IGBT single-stage boost PPFC converter.

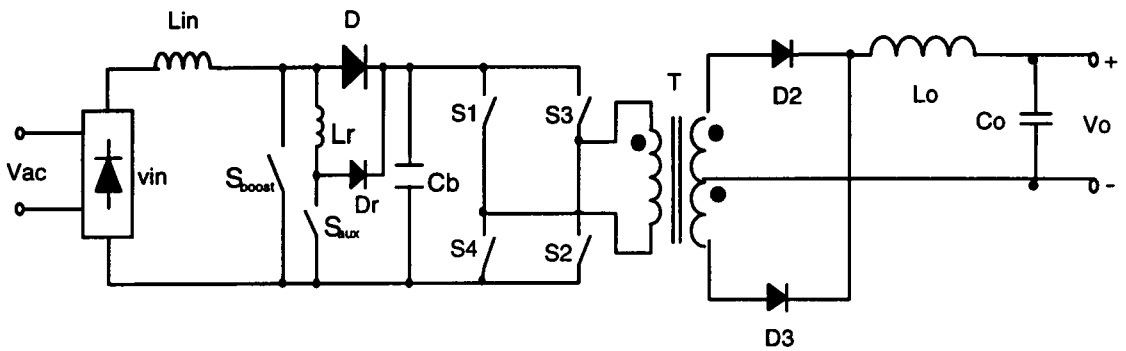


Fig. 3.11 Two-cascade-stage ZVT PFC converter.

Table 3.1 Component List

	MOSFET	IGBT	DIODE	INDUCTOR	TRANSFORMER
One-Stage PPFC	2	4	3	1	1
Two-Stage PFC	6	0	4	3	1

Since a MOSFET requires semiconductor area several times larger than an IGBT counterpart, the cost of the MOSFET is usually much higher than that of the IGBT. For example, in the current market, a 500 V, 25 A MOSFET (IRFP450) costs about $9, while a 600 V, 30 A IGBT (GBC30F) is only about $5. Therefore, the semiconductor devices of the boost PPFC converter are less expensive than that of the two-stage system. Also, the boost PPFC converter saves two magnetic components which reduces the converter cost as well. As a result, the cost of the boost PPFC converter is lower that the two-stage converter.

The soft-switched IGBT technique in the boost PPFC converter is used because the IGBT turn-off loss would be too high with hard-switching; choosing ZVT boost converter in the two-cascade-stage system is based on the fact that the diode reverse recovery would cause too much loss with hard-switching. Therefore, these two soft-switching techniques are important for high frequency operation.

3.4.1.2 Efficiency

One of the major advantages of the boost PPFC converter is its higher efficiency than the conventional two-cascade-stage approach for high power applications due to less conduction losses of using IGBTs. In the following, The conduction losses of both the boost PPFC converter and the two-cascade-stage system will be calculated.

Conduction losses in the PPFC converter 6: For $p_{in}>P_o$ as shown in Fig. 2.18 (a), there are three intervals within a switching cycle: the boost inductor charging interval, denoted as D_1T_s; the all-bridge-switch-off interval, denoted as $D_1'T_s$, when the energy is sent to the bulk capacitor; and the diagonal-switch-on interval, denoted as $D_1"T_s$, when the energy goes to the output.

The duty-ratios of these three intervals when $p_{in} > P_o$ are calculated in Appendix A, and the results are given here:

$$D_1 = 1 - D_1' - D_1" \tag{3.1}$$

$$D_1' = \frac{V_m \cdot (2\sin^2(\omega t) - 1)}{2V_B \sin(\omega t)}; \tag{3.2}$$

$$D_1" = \frac{V_m}{2V_o' \sin(\omega t)}; \tag{3.3}$$

where V_m is the peak of the input voltage; V_B is the bulk capacitor voltage; and V_o' is the transformer primary reflected output voltage.

For $p_{in}<P_o$ as shown in Fig. 2.18 (b), the switch S_5 operates to release energy from the bulk capacitor with the duty cycle of D_{s5}. There are two intervals of the bridge switches. The first interval, in which all four switches are on, is denoted as D_2T_s; the second interval, in which one pair of the diagonal switches are on, is denoted as $D_2'T_s$. Those duty ratios, as derived in Appendix B, are shown in Eq. (3.4) - (3.6).

$$D_{S5} = \frac{1 - 2\sin^2(\omega t)}{1 - 2\sin^2(\omega t) + \frac{2V_B}{V_m}\sin(\omega t)} \tag{3.4}$$

$$D_2 = 1 - \frac{V_m \cdot \sin(\omega t)}{V_o'} - \frac{V_B - V_m \cdot \sin(\omega t)}{V_o'} \cdot D_{s5} \tag{3.5}$$

$$D_2' = 1 - D_2 \tag{3.6}$$

Therefore, the conduction loss of all bridge switch conducting period is:

$$P_1 = \frac{2}{\pi}\left[\int_0^{\pi/4} \frac{1}{1 - D_{s5}} I_m \cdot \sin(\omega t) \cdot 2V_{ce} \cdot D_2 \cdot d(\omega t)\right] + \frac{2}{\pi}\left[\int_{\pi/4}^{\pi/2} I_m \cdot \sin(\omega t) \cdot 2V_{ce} \cdot D_1 \cdot d(\omega t)\right] \tag{3.7}$$

The conduction loss of the bridge switches during $D_1''T_s$ and $D_2'T_s$, i.e., one pair of the bridge switches are carrying current, can be calculated as:

$$P_2 = \frac{2}{\pi}\int_0^{\pi/4} \frac{1}{(1 - D_{s5})} \cdot I_m \cdot \sin(\omega t) \cdot 2V_{ce} \cdot D_2' \cdot d(\omega t) + \frac{2}{\pi}\int_{\pi/4}^{\pi/2} I_m \cdot \sin(\omega t) \cdot 2V_{ce} \cdot D_1'' \cdot d(\omega t) \tag{3.8}$$

The conduction loss of the diode D_1 can be calculated as:

$$P_{d1} = \frac{2}{\pi}\int_{\pi/4}^{\pi/2} I_m \cdot \sin(\omega t) \cdot D_1' \cdot V_{d1} \cdot d(\omega t) \tag{3.9}$$

The conduction loss of the switch S_5 is:

$$P_{s5} = \frac{2}{\pi}\int_0^{\pi/4} [I_m \cdot \frac{sin(\omega t)}{1 - D_{s5}}]^2 \cdot R_{ds(on)} \cdot D_{s5} \cdot d(\omega t) \qquad (3.10)$$

The input rectifier conduction loss is:

$$P_{rec.} = \frac{2}{\pi}\int_0^{\pi/2} I_m \cdot sin(\omega t) \times 2V_{rec.} \cdot d(\omega t) \qquad (3.11)$$

The total conduction loss on the primary side of the single-stage boost PPFC converter is:

$$P_{ppfc} = P_1 + P_2 + P_{s5} + P_{d1} + P_{rec.} \qquad (3.13)$$

Conduction losses in the conventional two-stage PFC converter: the duty-ratio of the boost switch is $D = 1 - \frac{V_m \cdot sin(\omega t)}{V_o}$. Therefore, the boost switch and diode conduction losses are given in Eq. (3.14) and (3.15).

$$P_s = \frac{2}{\pi}\int_0^{\pi/2} (I_m \cdot sin(\omega t))^2 \cdot R_{ds(on)} \cdot D \cdot d(\omega t) \qquad (3.14)$$

$$P_d = \frac{2}{\pi}\int_0^{\pi/2} I_m \cdot sin(\omega t) \cdot V_d \cdot d(\omega t) \qquad (3.15)$$

The conduction loss in the second stage DC/DC converter is:

$$P_{DC/DC} = \left(\frac{P_o}{0.8V_o}\right)^2 \times 2R_{ds(on)} \times 0.8 \qquad (3.16)$$

where the duty-ratio of the transformer is assumed to be 0.8.

Therefore, the total conduction loss on the primary side of the two-cascade-stage system is:

$$P_{two-stage} = P_s + P_d + P_{DC/DC} + P_{rec.} \qquad (3.17)$$

Assuming $R_{ds(on)}$=0.8 ohm (IRFP450 at 120°C junction temperature) and V_{ce}=2.4 V (IRGBC30F), with Eq. (3.13) and (3.17), the conduction losses of both cases under 185 Vrms input can be calculated as shown in Table 3.2.

Table 3.2 Conduction Loss Comparison

Pin (W)	200	400	600	800	1000	1200	1400	1600	1800	2000
PPFC (W)	7.0	14.2	21.6	29.2	37.0	45.1	53.3	61.8	70.4	79.3
2-Stage (W)	3.7	9.3	16.6	25.8	36.9	49.8	64.5	81.0	99.4	119.6

Based on the above analysis, it is clear that when power is higher than a certain level, the proposed boost PPFC converter is cheaper and more efficient than the conventional

two-cascade-stage system. The efficiency advantage has been verified by the experimental results given in the previous section.

3.4.2 Evaluation of the Flyback PPFC Converters

For relatively low power applications, the full-bridge type converters are not preferred for their high cost. Single-ended topologies, which require less semiconductor devices, make more sense in those applications. The single-stage flyback PPFC converters proposed in Chapter 3 are deemed for such low power applications. Here, PPFC converter 5, re-drawn in Fig. 3.12, is chosen as an example.

The first comparison is made with the conventional two-cascade-stage counterpart, consisting of a single-ended boost PFC converter and a forward DC/DC converter as shown in Fig. 3.13.

The cost comparison with the two-stage system is made based on the number of the semiconductor devices and the magnetic components, as indicated in Tab. 3.3. Two more magnetic components and two more diodes make the conventional two-cascade-stage system more expensive than the proposed flyback PPFC converter.

Table 3.3 Component List

	MOSFET	IGBT	DIODE	INDUCTOR	TRANSFORMER
One-Stage PPFC	3	0	1	0	1
Two-Stage PFC	3	0	3	2	1

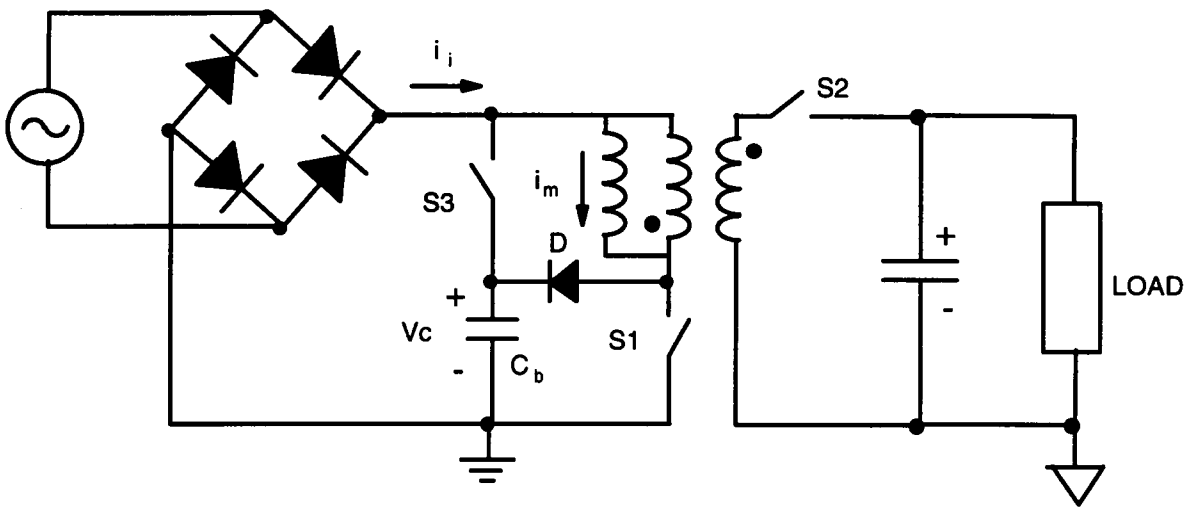


Fig. 3.12 PPFC converter 3.

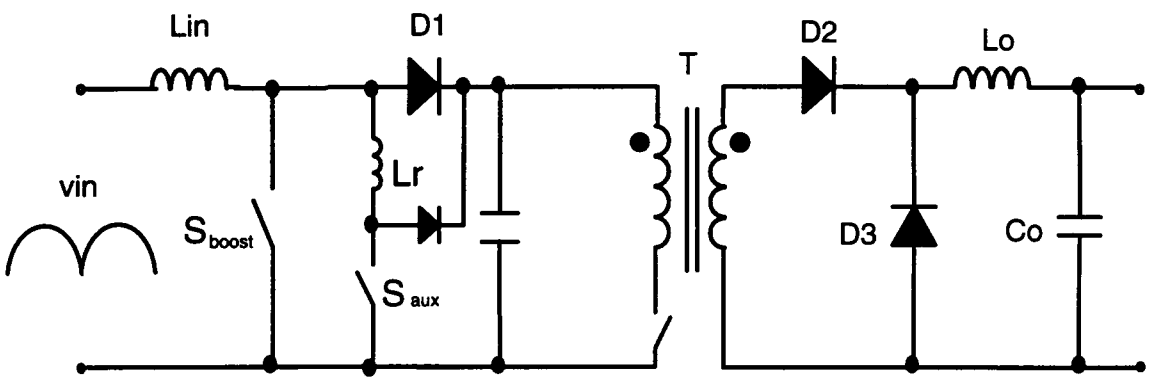


Fig. 3.13 Two-cascade-stage system.

Since it is designed for quite a low power level, though the input and output currents of the flyback PPFC converter are strongly pulsating, the input and output filters are quite small, which will not affect the cost much.

Regarding performance features, the flyback converter can inherently provide the inrush current control and short circuit protection. This is important for the low power applications since any increase of the circuit complexity will strongly affect the cost. Because of this reason, low power flyback PFC converter has been adopted in many industry practices.

Another way of justifying PPFC flyback converters is to compare them with the active clamp flyback PFC converters with high voltage side energy storage [D-37] as shown in Fig. 3.14. The bulk capacitor is charged with an auxiliary network not shown, and S_3 is open during normal operation and only closed during hold-up period. The combination of D_{1a} and D_{1b} is to bypass the slow body diode of S_2 (MOSFET). The diode D_{1b} clamps the voltage across switch S_1 to the capacitor C_r, and switch S_2 recycles the energy to the output. For detail operation of the active clamp technique, one can refer to [B-18]. The flyback PPFC converter in Fig. 3.12 uses about same number of components, but provides the extra important feature of tight output regulation.

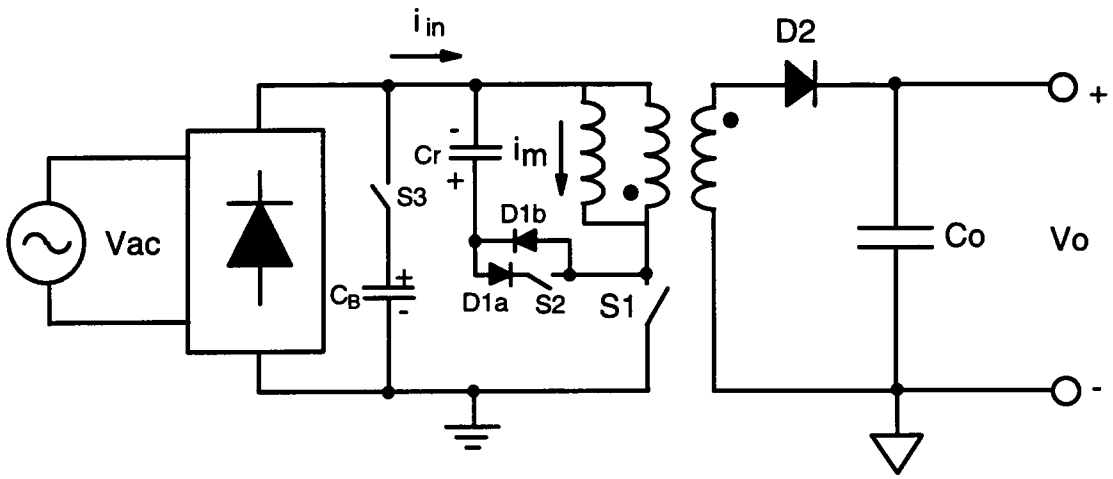


Fig. 3.14 Conventional flyback PFC converter.

3.5 Conclusions

In this chapter, the parallel PFC technique was verified with experiment and evaluated with comparison analysis.

The experiment conducted on the boost PPFC converter (PPFC converter 6) adopts IGBTs as the main power switches as well as a simple device-based IGBT soft-switching technique to alleviate IGBT switching losses. Compared with the conventional two-cascade-stage system adopting MOSFETs, this boost PPFC converter is more efficient and less expensive for power level higher than a certain level. Besides, its input current ripple frequency is twice of the switching frequency of the main switches, which reduces the EMI filter size. However, one drawback is that the transformer operating duty-ratio is changing with the input voltage. Therefore, its performances are hard to optimize for wide input range. Another drawback is that the two fast control loops (the input current loop and the output voltage loop) are coupled, which might require complicated decoupling control to improve the performance.

The proposed flyback PPFC converters are also better than its two-stage counterpart in terms of system complexity and cost. Compared with the conventional flyback PFC converter, which is a common practice for low power applications, it provides tight output regulation and ideal switch voltage clamping without increasing the system complexity. Therefore, the flyback PPFC converters are very attractive for relatively low power applications.

Chapter 4

Single-Phase Three-Level Boost PFC Converter

4.1 Introduction

For single-phase PFC, the single-ended boost converter is the most common practice due to its step-up voltage conversion ratio, continuous input current, simple topology, and high efficiency. However, there are still some concerns. For high power applications, the boost inductor will become one of the major factors affecting the system volume, weight, and cost. For high voltage applications, high voltage devices have high conduction losses and high switching losses. When voltage is higher than a certain level, some types of devices are not available. Therefore, it is very desirable to use a smaller inductor and lower voltage devices for high power and/or high voltage applications.

The multi-level buck converters have been proposed and studied before [F-1 - F3] for the purpose of using low voltage devices in high voltage applications. However, the capability of reducing magnetic component size has not been recognized. The multi-level boost converter has been ignored because there was no need for it until PFC recently became a concern.

With the three-level boost converter proposed in this chapter, the inductance of the boost inductor can be greatly reduced, and the device voltage rating is only half of the output voltage. As a result, the converter power density and efficiency will be

significantly improved, and cost will be reduced for high power and/or high voltage applications.

4.2 Three-Level Single-Ended Boost Converter

The proposed three-level single-ended boost converter is shown in Fig. 4.1. The output has a capacitor voltage divider. The voltage of the center point is $V_o/2$, which is obtained by choosing $C_1=C_2$ and the symmetrical operation of the two boost switches, as explained below.

4.2.1 Operation Principles

There are two regions where this converter can operate, depending on whether the input voltage is lower or higher than half of the output voltage.

Region I ($V_{in} < V_o/2$):

In this region, the boost inductor charging voltage must be V_{in}, since it is the minimum available charging voltage. However, the discharging voltage, which is V_o-V_{in} in a conventional boost converter, can be chosen as $V_o/2$-V_{in}. The operation waveforms are given in Fig. 4.2 (a).

At time t_0, which is the beginning of a switching cycle, the switch S_1 is turned on, and both switches are conducting. The inductor is charged with the input voltage, just as in a conventional boost converter. At time t_1, which is determined by the input current

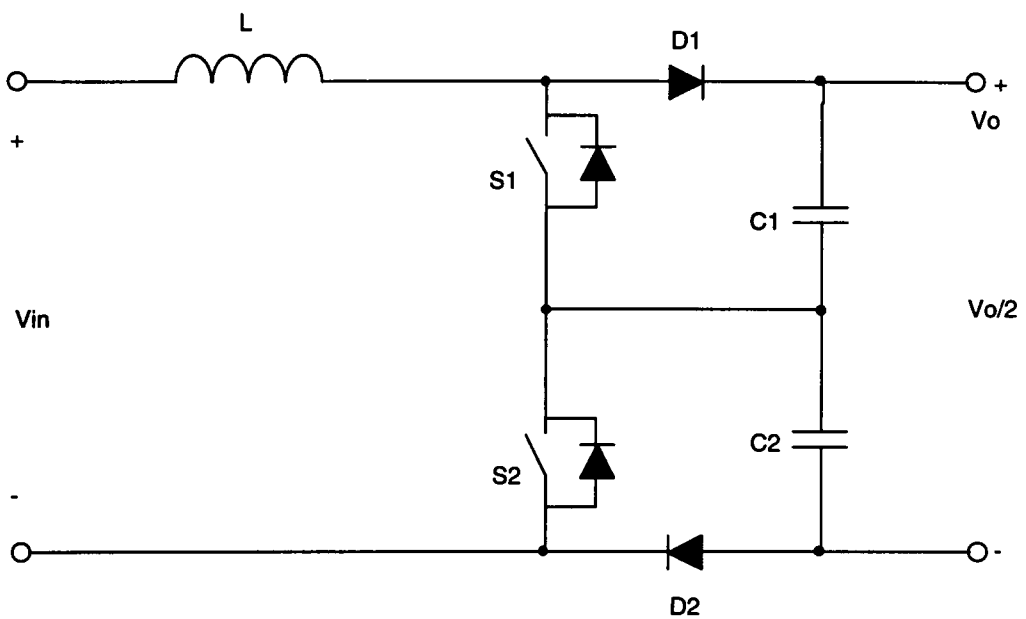


Fig. 4.1 Three-level boost converter.

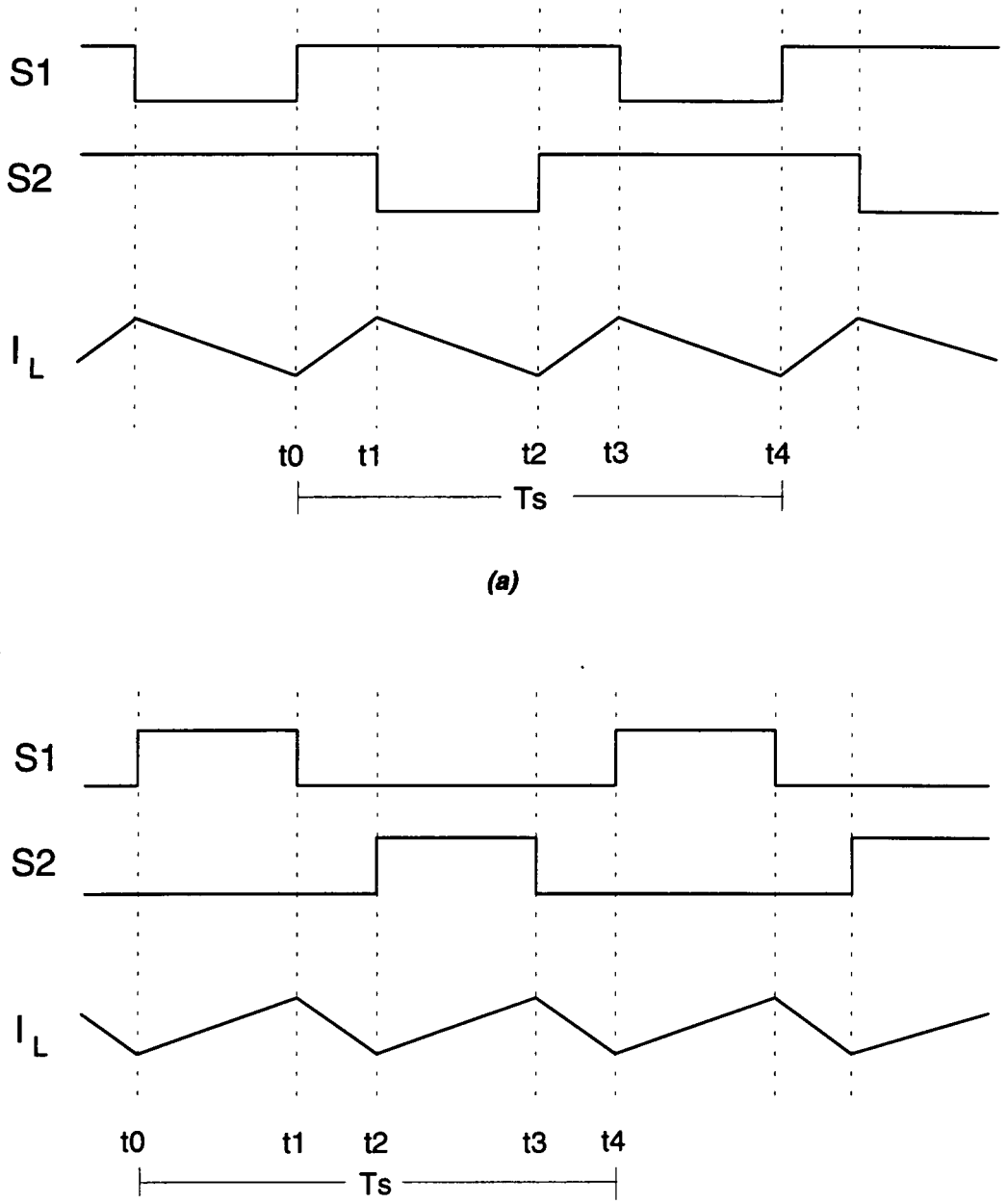


Fig. 4.2 Operation waveforms of three-level boost converter
(a) Vin < Vo/2; (b) Vin > Vo/2.

compensator, S_2 is turned off, forcing the inductor current to flow through the bottom output capacitor C_2 and the bottom diode D_2. Hence, the discharging voltage applied on the inductor is $V_o/2 - V_{in}$. At time t_2, which is fixed at $t_0+T_s/2$, S_2 is turned on, charging the inductor with the input voltage again. At time t_3, S_1 is turned off, and the inductor current will go through D_1, C_1 and S_2, discharged by $V_o/2 - V_{in}$ again. Since the upper and lower capacitors are used alternatively for discharging, their voltages are balanced.

Region II ($V_{in} > V_o/2$):

In this region, the boost inductor charging voltage is chosen to be $V_{in}-V_o/2$, and the discharging voltage will be V_o-V_{in}. The operation waveforms are shown in Fig. 4.2 (b).

At time t_0, which is the beginning of a switching cycle, S_1 is turned on with S_2 left open, the inductor current flows through S_1, C_2 and D_2 and builds up under $V_{in}-V_o/2$. At time t_1, which is determined by the input current compensator, S_1 is turned off, forcing the inductor current to go through D_1, C_1, C_2 and D_2, and to decrease under V_o-V_{in}. In the next half cycle, S_2 repeats the above action so that the voltages of the two output capacitors remain balanced.

In both regions, the advantages over the conventional boost converter can be seen from the following analysis.

4.2.2 Advantages of the Three-Level Boost Converter

Since two active switches are employed in the three-level boost converter, a fair comparison should be made with a conventional boost converter with two switches in parallel, as shown in Fig. 4.3. It needs to be mentioned that paralleling devices is only

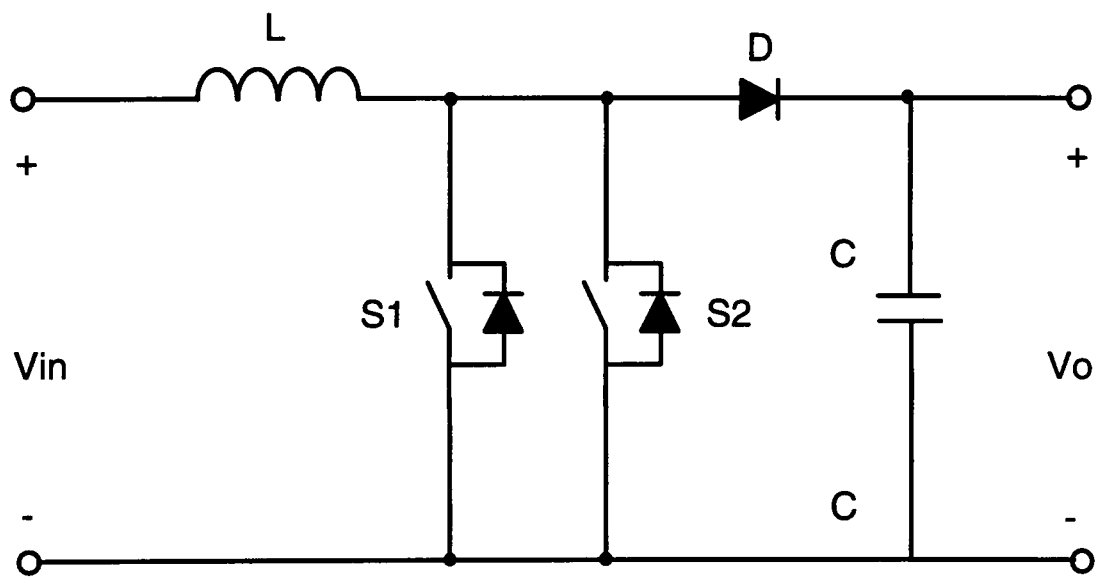


Fig. 4.3 Conventional boost converter with two switches in parallel.

feasible for devices with positive temperature characteristics, such as MOSFETs, for which the current sharing can be obtained without extra efforts. For devices with negative temperature characteristics, the one carrying a larger current intends to gain more current, and, as a result, the current will not be properly shared. Since the diode has negative temperature characteristics, only one diode is used here. It is also assumed that the switching frequency is the same for both converters.

4.2.2.1 Less inductor current ripple

From the above operation principles, one can see that the voltage applied on the boost inductor is reduced in either region compared with the conventional boost converter, due to the use of half of the output voltage. Therefore, less inductor current ripple is expected.

The inductor current ripple of the conventional boost converter is given in Eq. 4.1, with switching frequency of $f_s=1/T_s$ and duty-ratio of $D=1-\frac{V_{in}}{V_o}$.

$$\begin{aligned}\Delta i &= \frac{V_{in}}{L}\cdot D\cdot T_s \\ &= \frac{V_{in}}{L}\cdot(1-\frac{V_{in}}{V_o})\cdot T_s\end{aligned} \tag{4.1}$$

In the three-level boost converter, the inductor current ripple frequency is twice the value of the switching frequency, due to the interleaving operation of the two switches.

In region I, the $V_o/2$ - V_{in} is used to discharge the boost inductor. Therefore, the duty-ratio is $D=1-2\frac{V_{in}}{V_o}$; and Δi is reduced to the value given in Eq. 4.2.

$$\Delta i = \frac{V_{in}}{L} \cdot (1 - 2\frac{V_{in}}{V_o}) \cdot \frac{T_s}{2} \tag{4.2}$$

Using an example of V_{in}=150 V and V_o=400 V, Δi will be reduced 5 times. It can be seen that ripple current reduction is relevant to the input voltage. The closer the input voltage is to the $V_o/2$, the smaller the ripple current will be. Δi=0 when $V_{in}=V_o/2$, where maximum ripple current occurs in the conventional boost converter.

In region II, V_{in}-$V_o/2$ is used to charge the inductor. It can be derived that $D = 2(1 - \frac{V_{in}}{V_o})$, and, therefore, Δi is reduced to the value given in Eq. 4.3.

$$\Delta i = \frac{2V_{in} - V_o}{L} \cdot (1 - \frac{V_{in}}{V_o}) \cdot \frac{T_s}{2} \tag{4.3}$$

Since $V_{in} < V_o$ according to the basic boost converter requirement, then $2V_{in} < V_o+V_{in}$, which means $2V_{in}$-$V_o < V_{in}$. Therefore, the ripple current in Eq. (3) is at least two times less than that in Eq.(4.1). Again, the reduction depends on the input voltage.

Using an example of V_{in}=250 V and V_o=400 V, Δi will be reduced 5 times as well.

The above results also mean that, for a certain current ripple requirement, the required inductance of the boost inductor in the three-level boost converter is less than that in the conventional boost converter and will be greatly reduced if the input voltage is near half of the output voltage.

4.2.2.2 Higher efficiency and higher density

In the proposed three-level boost converter, the two diodes D_1 and D_2 clamp the voltages on the two active switches to one output capacitor voltage, which is half of the

output voltage. On the other hand, the anti-parallel diodes of switches S_1 and S_2 clamp the voltages on the two diodes D_1 and D_2 to $V_o/2$ as well. As a result, all semiconductor devices in the three-level boost converter are subject to only half of the output voltage.

According to device characteristics, higher voltage devices have worse conducting and switching capabilities than the lower voltage devices. Hence, better efficiency can be expected with this new converter topology. Examples will be given in the next section to demonstrate these benefits in single-phase PFC applications.

The inductor size is one of the major factors affecting the converter size; therefore, the three-level boost converter is expected to have higher power density since it requires less inductance.

4.3 Multi-Level Boost Converters

The three-level boost converter can be extended to a multi-level family. A four level boost converter is shown in Fig. 4.4.

However, different from the multi-level buck converters, where the active switches only see one capacitor voltage of V_{in}/n (for n-level), four or higher level boost converters do not posses this feature, and the highest voltage an active switch could be subject to is $(n-1)V_{in}/n$. For example, the switch S_2 in Fig. 4.4 must take $2V_o/3$ (two capacitor voltage) as the top two diodes are conducting. Although the current ripple could be

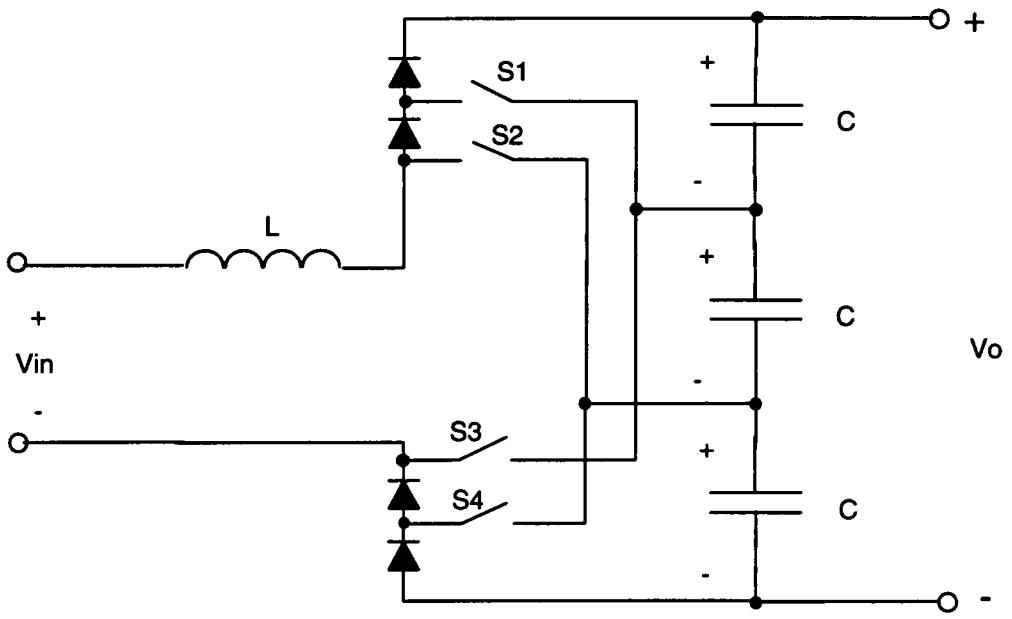


Fig. 4.4 Four-level boost converter.

further reduced in some applications, losing the device low voltage rating advantage makes them much less practical compared with the three-level boost converter.

4.4 Single-Phase PFC Three-Level Boost Converter

Since two active switches are used, this three-level boost converter is more favorable for high power applications; the low device voltage rating benefit is especially important in high voltage applications. From a practical point of view, the best application of the proposed three-level boost converter would be the single-phase power factor correction, where the output voltage is usually at around 400 V or higher, and the power level can be multi-kilo watts.

When the three-level boost converter shown in Fig. 4.1 is used for single-phase PFC purpose as shown in Fig. 4.5, the input voltage is in a rectified sinusoidal waveform, as shown in Fig. 4.6. It will stay in region I under the low line condition and will travel to region II if the input voltage peak is higher than $V_o/2$. The operations in either region are the same as described in the previous section, except that the duty-ratio changes with the input voltage.

The quantitative benefits of the single-phase three-level boost PFC converter over the conventional boost PFC converter are calculated in the following.

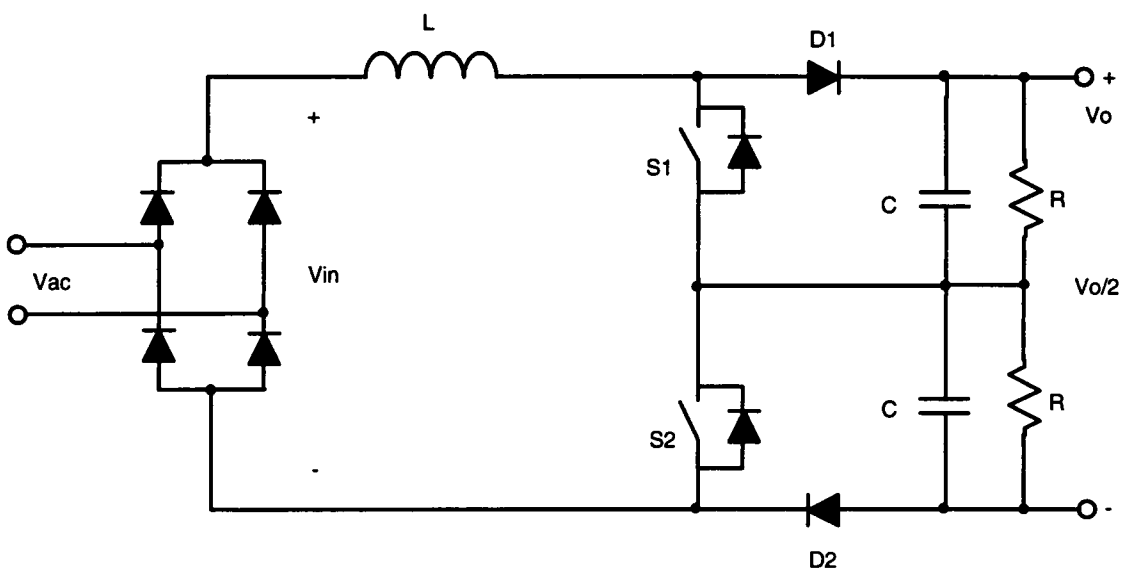


Fig. 4.5 Single-phase three-level boost PFC converter.

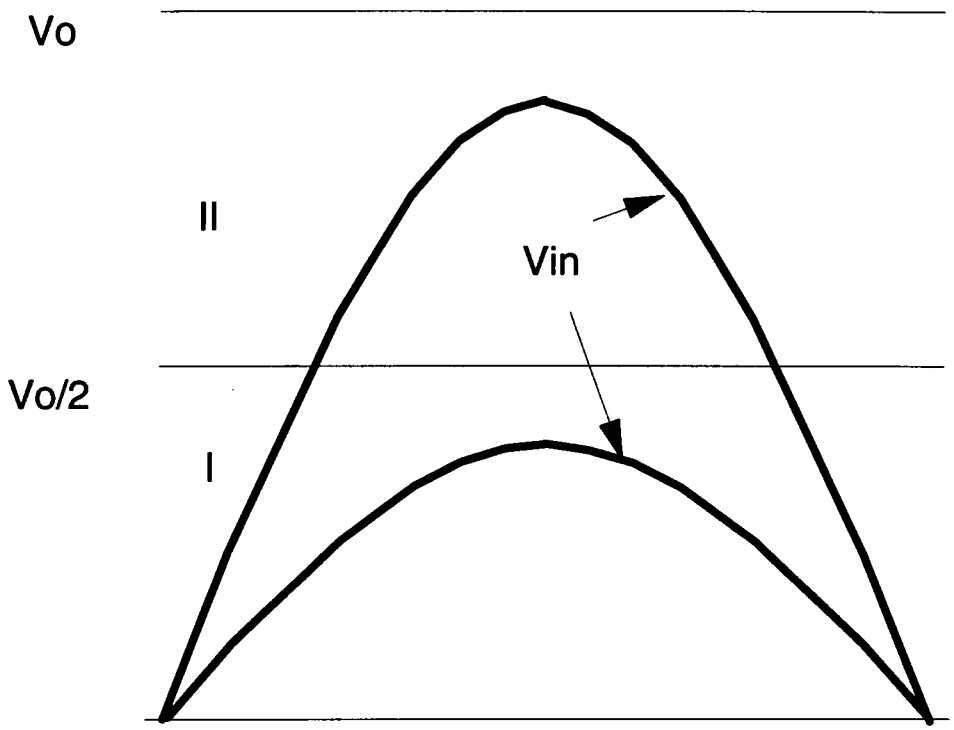


Fig. 4.6 Input voltage of the three-level boost PFC converter.

4.4.1 Less Current Ripple

It can be proven that the maximum inductor current ripple in a conventional boost converter occurs when the boost duty-ratio is 0.5. Considering the universal input line range, the maximum inductor current ripple of a conventional boost PFC converter occurs at $V_{in}=0.5V_o$, and is given in Eq. (4.4).

$$\begin{aligned}\Delta i_{max} &= \frac{V_{in}}{L}\cdot D\cdot T_s \\ &= \frac{V_o\cdot T_s}{4L}\end{aligned} \tag{4.4}$$

For the proposed three-level converter, the maximum current ripple in region I occurs when $V_{in}=0.25V_o$, where the boost duty-ratio is 0.5. The maximum current ripple is given in Eq. (4.5).

$$\begin{aligned}\Delta i_{max1} &= \frac{V_{in}}{L}\cdot D\cdot\frac{T_s}{2} \\ &= \frac{V_o\cdot T_s}{16L}\end{aligned} \tag{4.5}$$

In region II, the maximum current ripple occurs when $V_{in}=0.75V_o$, also corresponding to 0.5 boost duty-ratio. The maximum current ripple is given in Eq. (4.6).

$$\begin{aligned}\Delta i_{max2} &= \frac{V_{in}-0.5V_o}{L}\cdot D\cdot\frac{T_s}{2} \\ &= \frac{V_o\cdot T_s}{16L}\end{aligned} \tag{4.6}$$

Comparing Eqs. (4.4), (4.5) and (4.6), one can see that the inductor current ripple in the three-level boost converter is one fourth of that of the conventional boost converter. In other words, for the same current ripple specification, the three-level boost converter requires four times less inductance than the conventional boost converter does.

Four time less inductance means four time less energy storage capacity. According to magnetics knowledge, the energy storage density of a core is $\frac{1}{2}\cdot\frac{B^2}{\mu}$, which is only determined by the flux density B and the effective permeability μ, which are the same for both cases. Therefore, the inductor in the three-level boost converter is about one fourth the size of that in the conventional boost converter.

4.4.2 Higher Efficiency and Lower Cost

First, the switching loss is a strong function of the voltage. The capacitive turn-on loss of the three-level boost converter is reduced eight times, assuming same output capacitance for devices with different voltage ratings (A lower voltage device actually has less output capacitance from the device data sheet). Diode reverse recovery losses are also reduced, since the reverse voltage is only half of the output voltage, and the diodes with half voltage rating could be faster. Therefore, the total switching losses is reduced.

Secondly, the conduction losses could also be reduced when using MOSFETs as the power switches. The MOSFETs used in the conventional boost converter with above 600 V rating have significantly larger on-resistance than the half voltage rated MOSFETs in the three-level boost converter; therefore, the conduction losses in the

three-level converter could be less. This advantage can be verified with the following two examples.

Example 1 (Universal line):

V_{ac}=90 V (rms), V_o=380 V, and P_o=2 kW

Since the worst efficiency always occurs at low line, 90 Vrms is used in calculation.

In the conventional boost converter, as shown in Fig. 4.3, two 500 V MOSFETs are used, with typical on-resistance of R_{ds1}=0.4 Ω each. The on-voltage drop V_d of the 500 V diode D is assumed to be 1.5 V.

The calculation of the device conduction losses is given in Eq. 4.7.

$$P_1 = \frac{2}{\pi}\int_0^{\pi/2} [i_{ac}^2(\omega t)\times 0.5R_{ds1}\cdot D(\omega t) + i_{ac}(\omega t)\cdot(1-D(\omega t))\cdot Vd]\cdot d(\omega t) \tag{4.7}$$

Using the above data, P_1=78.6 W.

In the three-level boost converter, two 250 V MOSFETs are used, each of which has on-resistance of R_{ds2}=0.08 Ω. The on-voltage drop of the 200 V diode is assumed to be 1 V.

The calculation of the device conduction losses is given in Eq. 4.8.

$$P_2 = \frac{2}{\pi}\int_0^{\pi/2} [i_{ac}^2(\omega t)(2R_{ds2}\cdot D(\omega t) + R_{ds2}\cdot(1-D(\omega t)) + iac(\omega t)\cdot(1-D(\omega t)\cdot V_d]d(\omega t) \tag{4.8}$$

For the same situation, P_2=67.1 W.

Example 2 (European line):

V_{ac}=185 V (rms), V_o=380 V, and P_o=2 kW

The devices used for the conventional boost converter and in the three-level boost converter are the same as in the first example.

The device conduction losses of the conventional boost converter are calculated also with Eq. 4.7, obtaining P_1=17.6 W.

For the three-level boost converter, the conduction losses are calculated with Eq. 4.9.

$$P_2 = \frac{2}{\pi}\int_0^{\alpha} [I_{ac}^2(2R_{ds}\cdot D(\omega t) + R_{ds}(1-D(\omega t))) + I_{ac}\cdot V_d(1-D(\omega t))]d(\omega t) + \frac{2}{\pi}\int_{\alpha}^{\pi/2} [I_{ac}^2\cdot R_{ds}\cdot D(\omega t) + I_{ac}\cdot V_d + I_{ac}\cdot V_d(1-D(\omega t))]d(\omega t) \quad (4.9)$$

Where, the α is the boundary of the two regions.

With the given data, it was calculated that P_2=11.6 W.

In the above two examples, the conduction losses of the three-level boost converter are less than that of the conventional boost converter for either universal or European line. In fact, the above calculation does not count the high frequency current ripple, which will affect the inductor core loss and the conduction losses of both the inductor and the devices.

As to the cost, the 500 V MOSFET with 0.4 Ω on-resistance has roughly the same price as that of the 250 V MOSFET with 0.08 Ω on-resistance. Considering the saving on the boost inductor and the possibility of not using any soft-switching technique due to much less switching losses, the cost of the three-level converter should be lower than that of the conventional boost converter. In fact, the benefit will be more pronounced for higher voltage applications.

From the performance point of view, the more competitive counterpart of the three-level boost converter is the two-interleaved boost converter shown in Fig. 4.7. The inductance of each boost inductor is set at 2L (L is the inductance of the boost inductor in the three-level boost converter), which yields the same energy storage capability for both the two-interleaved boost converter and the three-level boost converter. Since the energy storage density of a core is $\frac{1}{2}\cdot\frac{B^2}{\mu}$, which is only determined by the flux density and the effective permeability which are the same for both cases, the inductor volume can be assumed same for both cases due to the same energy storage capability.

Figure 4.8 shows the two input inductor currents i_1 and i_2 and the total input current i_{in} of the two-interleaved boost converter. Choosing the two inductor currents at the boundary of CCM and DCM facilitates adding them up and estimating the reduction of the total input current ripple compared with each inductor current ripple. It is assumed that these two inductor current waveforms are exactly the same, except for the 180° phase shift. The input current ripple frequency is two times higher than that of the inductor current ripple; therefore, to find out the input current ripple, only a period of $T_s/2$ needs to be analyzed.

Assuming D<0.5, the input current ripple is $\Delta i=(k_1-k_2)DTs$, where $k_1=V_{in}/2L$ and $k_2=(V_o-V_{in})/2L$ are the inductor current charging and discharging slops. Thus,

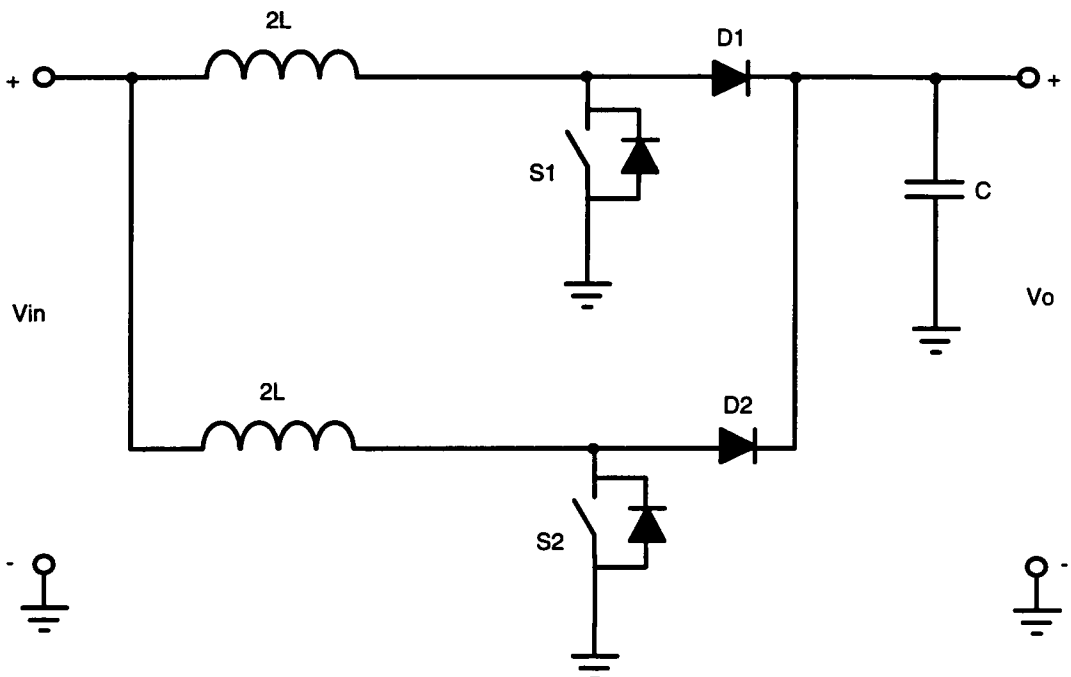


Fig. 4.7 Two interleaved boost converters.

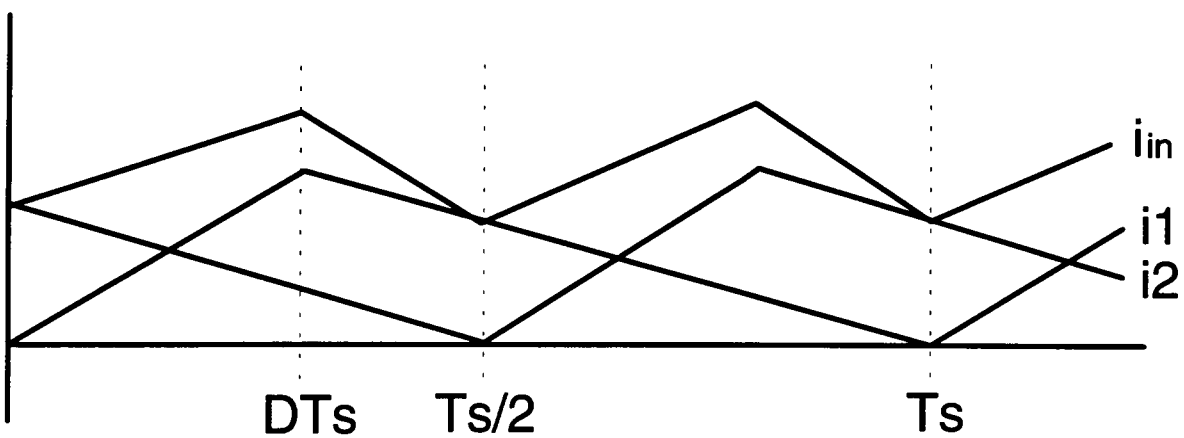


Fig. 4.8 Input current and inductor currents of the two interleaved boost converters.

$$\Delta i = \frac{2V_{in} - V_o}{2L} \cdot (1 - \frac{V_{in}}{V_o}) \cdot T_s \tag{4.10}$$

which is the same as Eq. 4.3. The maximum current ripple occurs at the point where $\frac{\partial \Delta i}{\partial V_{in}} = 0$. This point is $V_{in}=0.75V_o$, which is the same point where maximum current ripple occurs in the three-level boost converter. The current ripple amplitude at this point can be calculated from Eq. 4.10, obtaining $\Delta i = \frac{V_o \cdot T_s}{16L}$, which is also the same as the expression describing the current ripple of the three-level boost converter, as given in Eq. 4.6.

For D>0.5, the input current ripple is $\Delta i=(k_2-k_1)D'T_s$, where $k_1=V_{in}/2L$ and $k_2=(V_o-V_{in})/2L$ are the inductor current charging and discharging slops. Thus,

$$\Delta i = \frac{V_o - 2V_{in}}{2L} \cdot \frac{V_{in}}{V_o} \cdot T_s \tag{4.11}$$

which is the same as Eq. 4.2.

With $\frac{\partial \Delta i}{\partial V_{in}} = 0$, it is found that the maximum current ripple occurs at the point of $V_{in}=0.25V_o$, which is also the same point where the maximum current ripple presents in the three-level boost converter, and the maximum current ripple is also $\Delta i = \frac{V_o \cdot T_s}{16L}$.

Therefore, the maximum current ripple of the three-level boost converter is the same as that of the two-interleaved boost converter.

However, the two-interleaved boost converter has the following drawbacks compared with the three-level boost converter.

- Two complete boost converters are in parallel, including two inductors, two input current sensors, and two PFC controllers with proper interleaving and input current sharing;
- Each inductor has higher ripple current, which causes high core loss in the inductor and high conduction losses in both the inductor and the semiconductor devices;
- More severe diode reverse recovery occurs due to the use of high voltage diodes;
- EMI is higher since the PWM actions are occurring between full output voltage and the ground; and
- High voltage devices are still needed and cannot deal with high input voltage.

These drawbacks make the two-interleaved boost converter much less attractive than the three-level boost converter for high power and/or high input voltage applications.

4.4.3 Control Scheme and Simulation of the Three-Level Boost PFC Converter

One can use conventional single-phase PFC controllers, such as UC3854 to create one of the two driving signals. The only thing beyond that is to generate a phase shifted signal for the other switch. According to Fig. 4.2, the second driving signal should be shifted by half of the switching cycle and preserve the same duty-ratio. There are different ways to do this. One example is to create another saw-tooth ramp, which is shifted from the original ramp by half of the switching cycle. Then, the second signal can be obtained by comparing the current error amplifier output with this shifted ramp (ramp 2), as shown in Fig. 4.9.

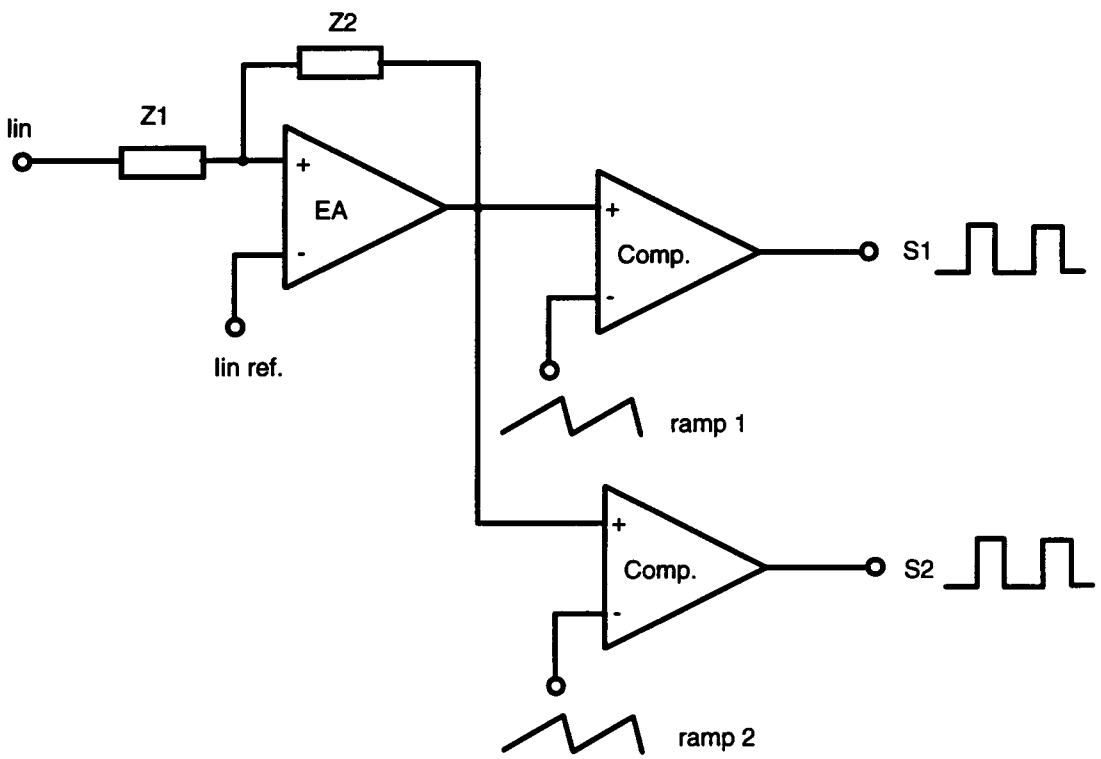


Fig. 4.9 Control scheme 1 for the three-level boost converter.

It can be seen that, when duty-ratio is greater than 0.5, it is running in region I, and when duty-ratio is less than 0.5, it is running in region II. Thus, there is no need to detect whether the input voltage is lower or higher than half of the output voltage.

The large signal simulation of the three-level boost converter under this control is conducted for the condition of V_{ac}=90 V, V_o=400 V, and P_o=2 kW, and the simulated waveforms are given in Fig. 4.10. For the purpose of showing the ripple current reduction, a conventional boost converter with same boost inductance and switching frequency is simulated under the same operating condition, and the ripple current, as seen in Fig. 4.11, is four times larger than that of the three-level boost converter.

However, the above control scheme might have difficulty in practical implementation, since any discrepancy between the two ramps will cause differences between the duty-ratio of the two boost switches and will lead to unbalance between the two output capacitor voltages.

To overcome this drawback, another control scheme is proposed, as shown in Fig. 4.12.

Different from the first control scheme, ramp 2 is on top of ramp 1, and both are in phase. When the current error amplifier output intersects with ramp 1, a duty-ratio signal S_a is produced. The output of the D flip-flop changes every switching cycle so that the driving signal S_a is distributed to switch S_1 and S_2 alternatively. In this case, the signal S_b is low and does not affect outputs S_1 and S_2. It can be seen that the duty-ratios of S_1 and S_2 under this condition are the same and less than 0.5, corresponding to the region II operation. When the current error amplifier output intersects with ramp 2, S_a is high all the time, and a duty-ratio signal will occur at S_b. This signal and the outputs of the D flip-flop go to the "OR" gates and produce S_1 and

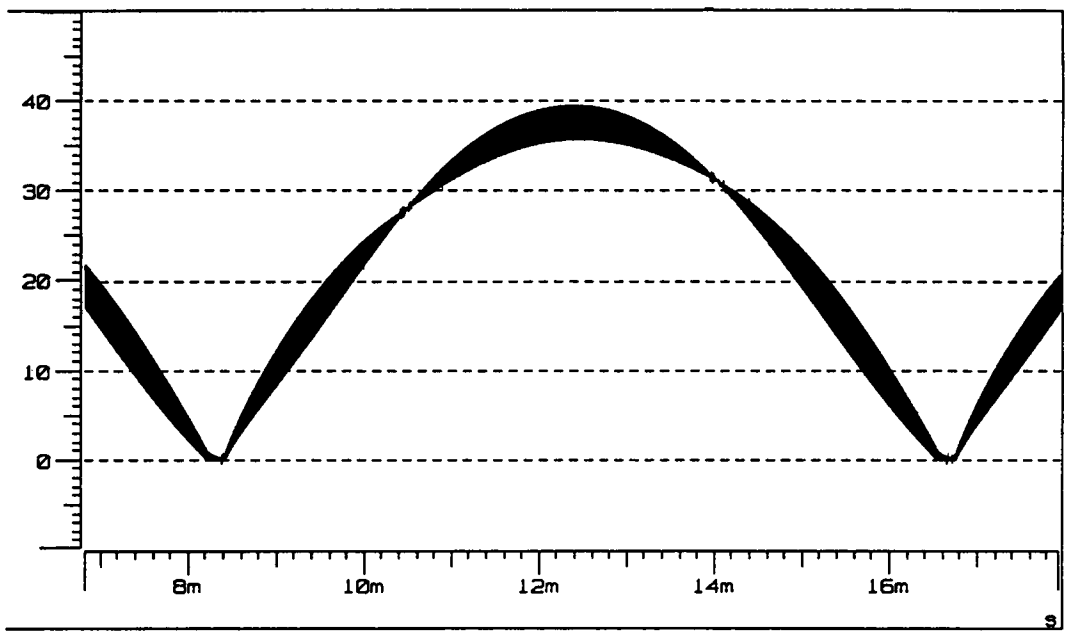


Fig. 4.10 Large signal simulation of the boost inductor current in the three-level boost PFC converter.

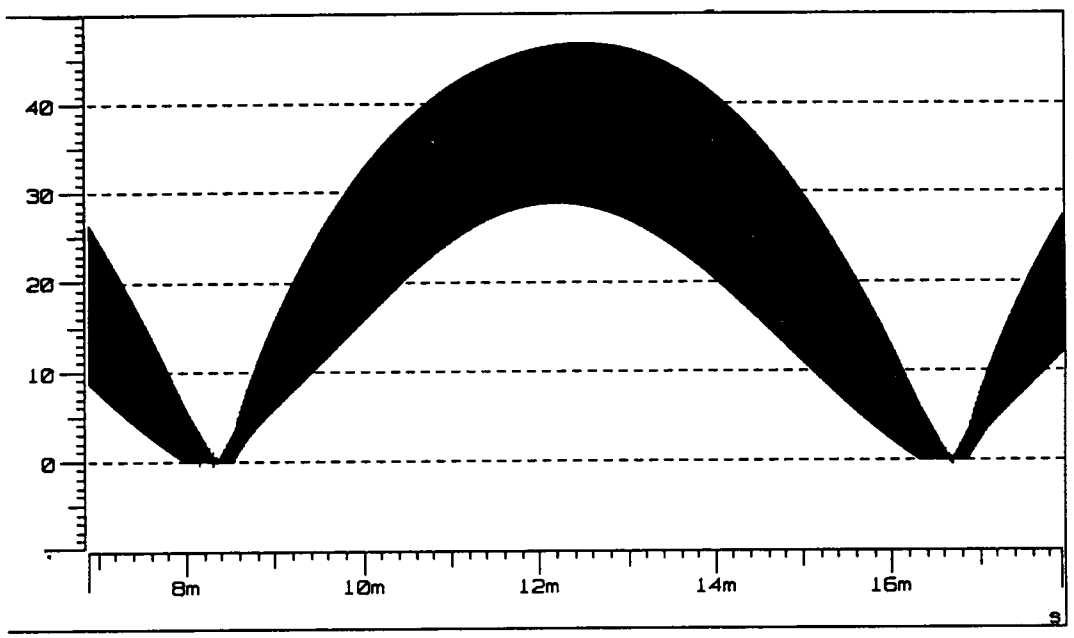


Fig. 4.11 Large signal simulation of the boost inductor current in the conventional boost PFC converter.

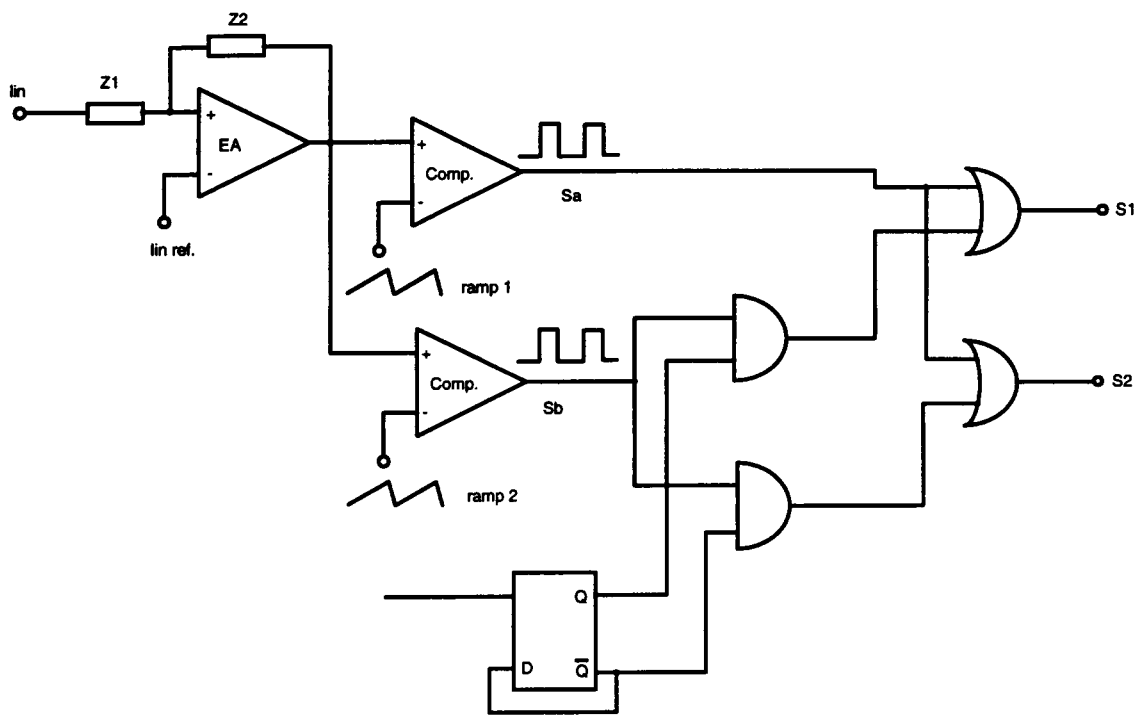


Fig. 4.12 Control scheme 2 for the three-level boost converter.

S_2. The duty-ratios of both S_1 and S_2 are also the same and larger than 0.5, which corresponds to the region I operation. The reason that the same duty-ratio of both switches can be achieved is due to using only one ramp to create the two duty-ratio signals, and, therefore, the drawback of the first scheme is removed.

4.5 Soft-Switching of the Three-Level Boost Converter

Although this three-level boost converter already has less switching losses than the conventional boost converter, the soft-switching technique is still appreciated for high voltage, high power, and high switching frequency applications.

Directly applying the zero-voltage-transition technique [D-12], the ZVT three-level boost converter can be constructed, as shown in Fig. 4.13, by adding two auxiliary resonant networks.

Basically, the top resonant network achieves the ZVS for the top switch S_1, and the bottom resonant network for the bottom switch S_2. Since the turn-on actions of the two main switches are interleaved, the auxiliary networks are also running alternatively. The driving signals are drawn in Fig. 4.14, where the main switch driving waveforms are the same as shown in Fig. 4.2.

The auxiliary switch driving signal is applied a short period before the turn-on of the corresponding main switch, so that a current builds up in the resonant inductor. When the resonant inductor current reaches the boost inductor current, resonance occurs between the resonant inductor and the resonant capacitor, which is the junction

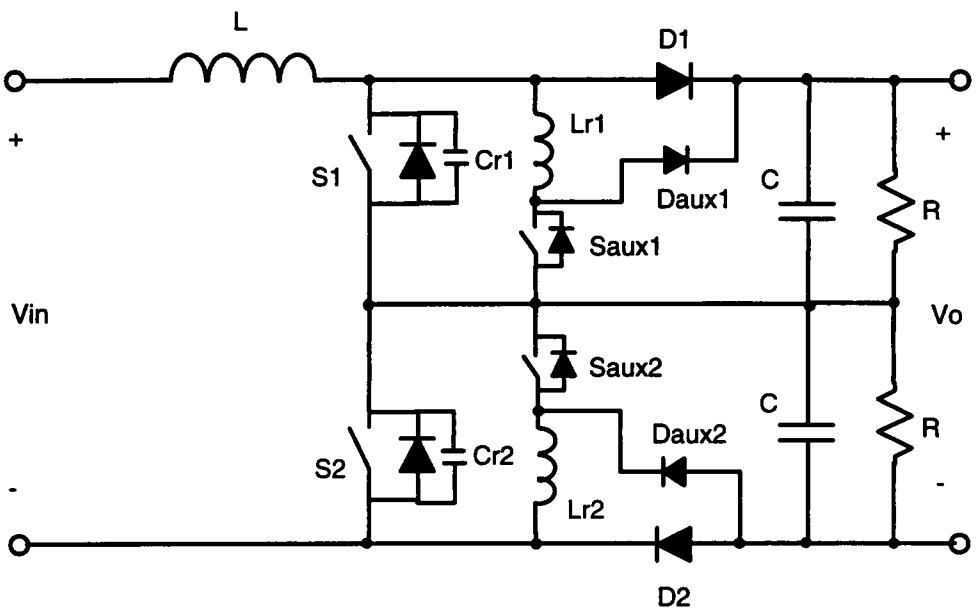
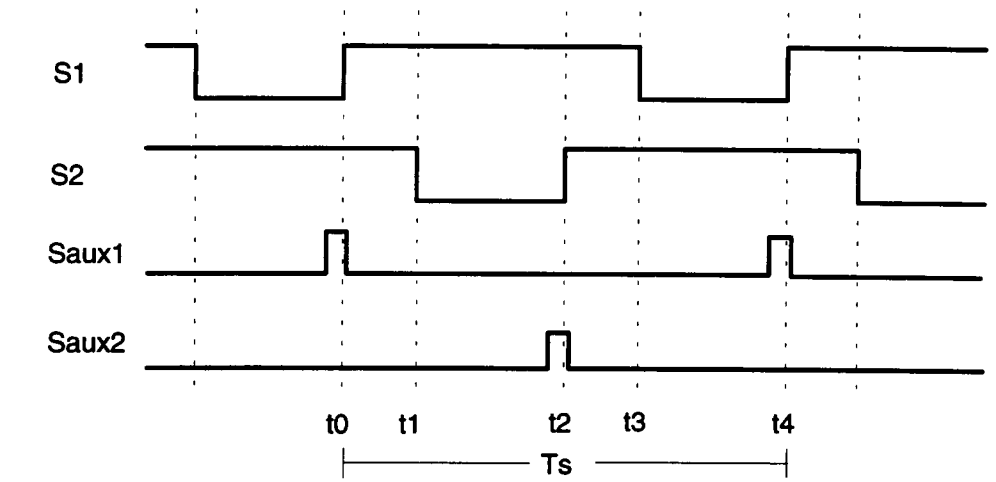
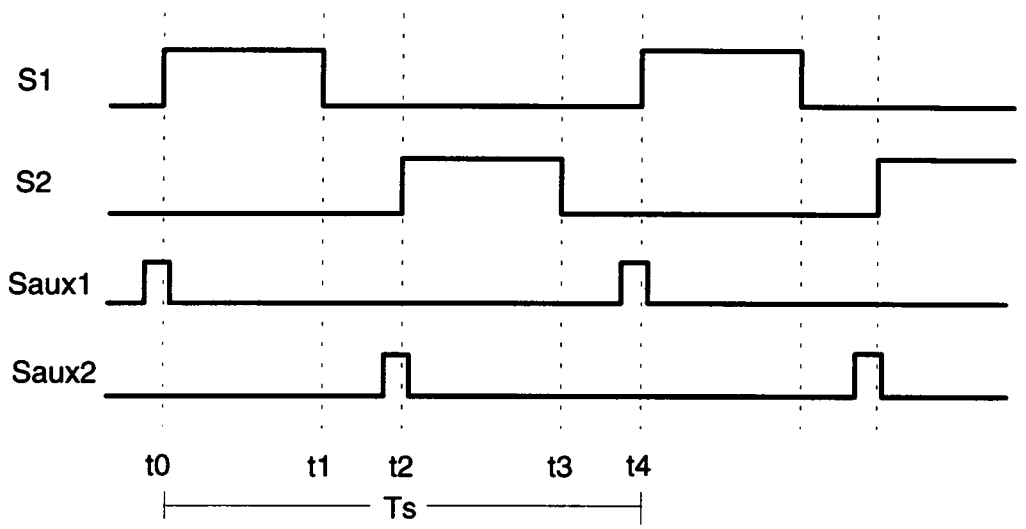


Fig. 4.13 ZVT three-level boost converter.



(a)



(b)

Fig. 4.14 Driving signals of the ZVT three-level boost converter (a) Vin<Vo/2; (b) Vin>Vo/2.

capacitor of the main switch together with external capacitors, if any. This resonance will discharge the resonant capacitor, and the anti-parallel diode of the main switch will then conduct. Therefore, the zero-voltage switching condition is achieved. It is noted that the energy in the upper resonant inductor is released to the upper output capacitor, and the energy in the lower resonant inductor is released to the lower output capacitor, respectively, which ensures the output capacitor voltage balancing.

All the auxiliary devices are also rated at half of the output voltage, which has less conduction and switching losses than auxiliary devices in the conventional ZVT boost converter.

The zero-current-transition technique [D-14] can also be applied by simply replacing the above two ZVT networks with two ZCT networks. In most applications, the half of the output voltage is low enough to use MOSFETs as the main power switches, and their turn-off losses are quite little. In such cases, the ZVS technique will be more useful than the ZCS technique for the purpose of alleviating the diode reverse recovery problem.

4.6 Conclusions

With the three-level boost converter proposed in this chapter, the boost inductor is about four times smaller than that of the conventional boost converter. The device voltage rating is only half of the output voltage, which is desirable for high voltage applications for reducing both conduction and switching losses. Utilization of a smaller inductor and lower voltage devices yields higher efficiency, higher power density, and lower cost.

The ZVT three-level boost converter can further reduce the switching losses, including the diode reverse recovery losses and the capacitive turn-on losses. For high switching frequency operation and reducing EMI, it would be useful.

It is expected that for some PFC applications, where power is higher than a certain level, this three-level boost converter will be the best choice.

Chapter 5

Simple High Performance Three-Phase Boost PFC Rectifiers

5.1 Introduction

For high power applications (say, above 5 kW), three-phase AC power are most frequently used. A balanced three-phase system has constant instantaneous input power under the assumption of unity power factor. Therefore, the output of the PFC converter will not contain low frequency ripple, and no bulk capacitor is necessary. Both the boost and buck rectifiers are capable of producing unity power factor [C-1 - C-20]. However, the three-phase boost rectifier, as shown in Fig. 5.1, has the advantages of continuous input currents, high efficiency, as well as high output DC voltage needed by the voltage-source-inverters (VSI) for AC drive applications. Therefore, it is the most commonly used converter topology in the three-phase unity power factor rectification, though inrush current and output short circuit protection need additional attention.

Most of the previous research efforts in the three-phase converters were concentrated on the PWM VSI for its popular use in AC motor drives and UPS systems. Many PWM current control schemes have been developed [E-1 - E-8], and a number of soft-switching techniques have been proposed as well [D-18 - D-37]. However, not much research efforts have been directed toward the PWM rectifier applications.

The rectifier operation is much simpler, since its only job is to provide power factor correction in most cases; in many applications, only unidirectional power flow is required. Another important difference is that the switching frequency in the rectifier should be as high as possible to minimize the size of the filter inductors. On the other hand, the inverter operation is quite complex due to the high performance requirements of many AC drive systems; the inverters need to handle bi-directional power flow in most cases, and 20 kHz switching frequency is sufficient in most AC motor drive systems to avoid the acoustic noise, since no extra inductors are used.

As to the control scheme, sophisticated digital control, which employs digital signal processor (DSP) to perform the d-q transformation and loop compensation, is quite popular in high performance inverter systems. But, it is unaccustomed to the power supply community and is not very economical for simple rectifier applications. Therefore, simple analog control is preferred for most rectifier applications. However, a conventional analog controlled three-phase boost rectifier has several drawbacks which will be described in the next section.

Several novel three-phase boost rectifiers have been developed and will be introduced in this chapter. These novel rectifiers overcome the major problems of the conventional analog controlled three-phase boost rectifier and provide high performances, such as automatic six-step operation, high reliability, and simple soft-switching schemes, which allow high switching frequency and achieve high efficiency and high power density.

5.2 Drawbacks of the Conventional Boost Rectifier

Before presenting these novel three-phase boost rectifiers, several drawbacks of the conventional one, as shown in Fig. 5.1 will be pointed out so that the advantages of the new ones can be well understood.

For the off-line rectifier, three-phase current control is necessary to achieve unity power factor. The current control schemes developed for the VSI, including linear control, hysteresis control, predictive control, delta modulation, rotating frame control, and more advanced neural and fuzzy control, can all be employed for the rectifier application. However, as mentioned above, the rectifier function is much simpler, and certain types of simple control schemes would be preferable. One simple way of implementing three-phase current control is to use three independent control loops. The three controllers could be of the linear or hysteresis type, and can be implemented with simple analog circuitry without using a digital signal processor (DSP). Fig. 5.2 shows a simple independent analog controlled scheme, similar to what is used for single-phase PFC converters.

To obtain unity power factor, the sinusoidal current reference for each phase is provided by the product of the output of the voltage error amplifier and a signal proportional to the corresponding input phase voltage. The three independent current controllers regulate the three input phase currents to follow the respective sinusoidal references.

Such an analog controlled system is quite simple, but has several drawbacks.

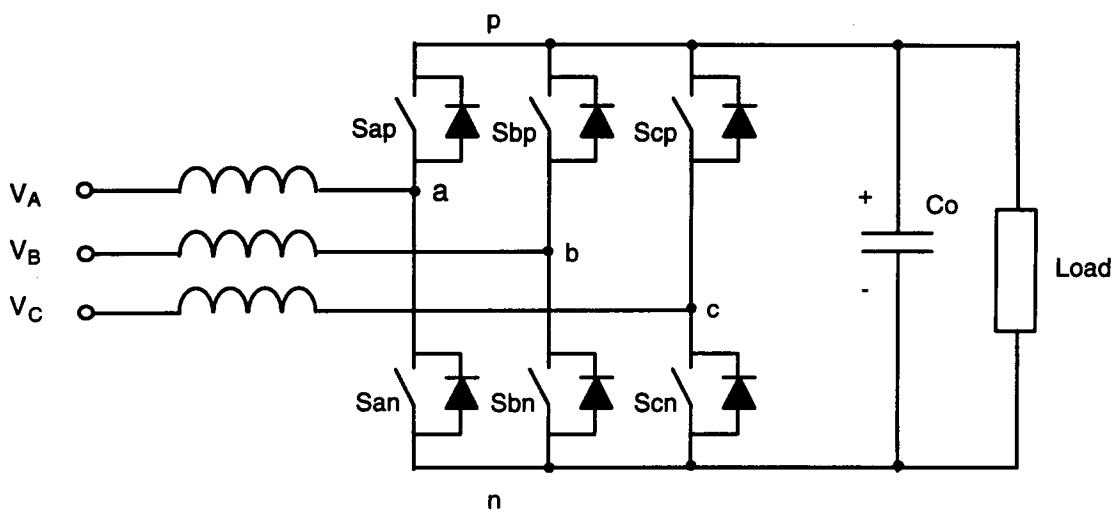


Fig. 5.1 Conventional three-phase boost rectifier.

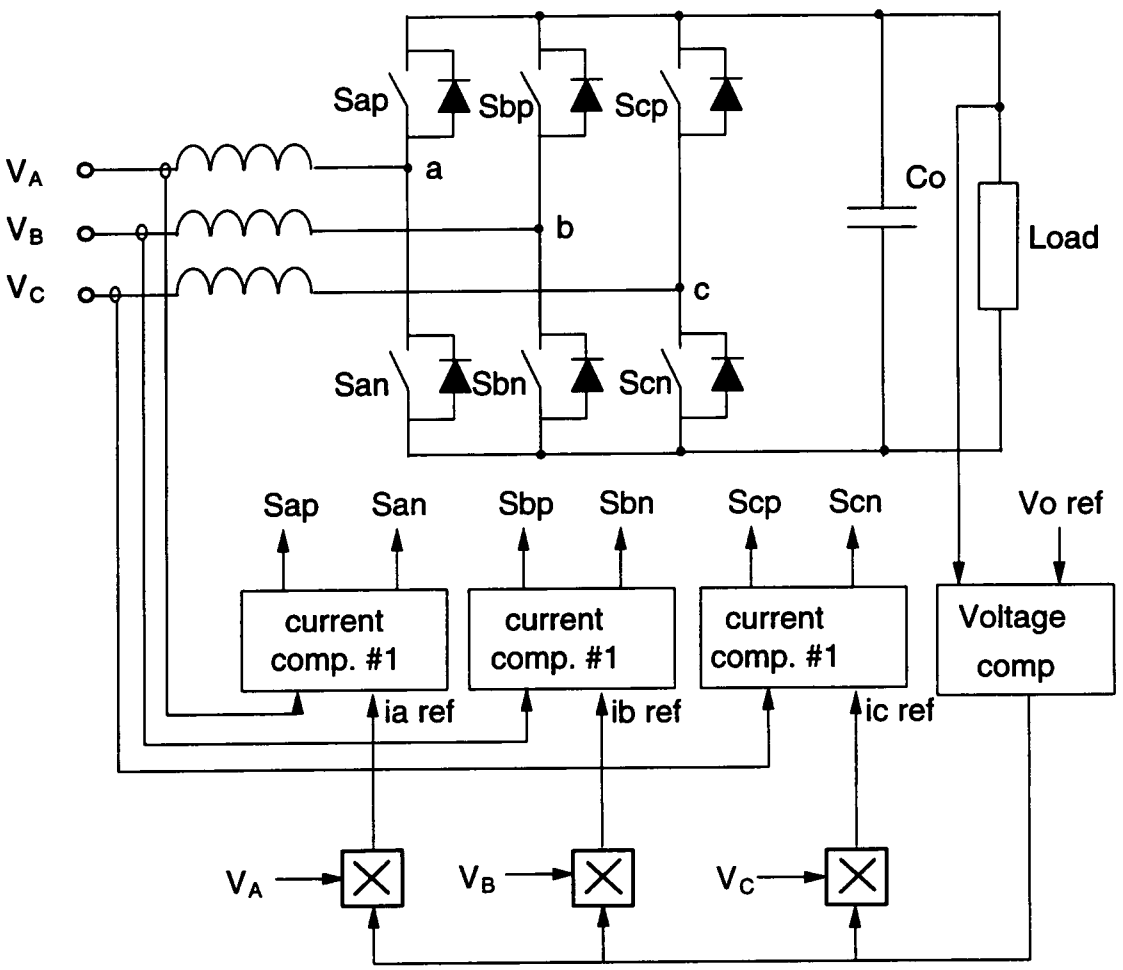


Fig. 5.2 Independent control of three-phase boost rectifier.

First, it does not operate under six-step PWM mode. To have the six-step PWM operation, which yields minimum input current ripple and no circulating energy, a decoder is necessary to precisely detect each 60° interval within a line cycle, and properly disable one of the three running switches. The details will be explained in the next section.

Secondly, because the bridge switch anti-parallel diodes usually have poor switching characteristics, their reverse recovery currents cause severe switching losses. If minority carrier devices, such as BJTs, IGBTs, or GTOs are used, the turn-off current tail problem is also severe. However, there are no simple soft-switching techniques available so far. As a result, it is difficult to run this converter at a desired high switching frequency under hard-switching conditions, due to the large switching losses.

Thirdly, failure mode due to the bridge short-through cannot be eliminated and careful design attention has to be given to mitigate the cause of shoot through.

Finally, as to the soft-switching techniques, almost all developments so far are for VSI, and no simple soft-switching techniques have been reported for the rectifier.

The three-phase boost rectifiers proposed here will eliminate or alleviate the above drawbacks.

5.3 Proposed Three-Phase Boost Rectifier

The proposed three-phase boost rectifier is shown in Fig. 5.3. It is obtained by adding a diode on the DC rail. This single diode provides several important advantages over the conventional one, which will be demonstrated below.

1 Automatic six-step operation

First, the operation of the conventional boost rectifier shown in Fig. 5.1 needs to be examined. All possible bridge voltage vectors (V_a, V_b, V_c) are shown in Fig 5.4(a). Each vector is produced by a switching combination denoted by three letters. The letters, from left to right, signify whether the center points a, b, c are connected to the positive (p) or negative (n) side of the DC rail. In a conventional boost rectifier, all the eight possible vectors, including two zero vectors, are available at any time independently from the position of the input voltage vector (V_A, V_B, V_C). For six-step operation, only the two adjacent vectors of the input voltage vector and the zero vectors should be used.

Consider the example where the input voltage vector V_{in}= (V_A, V_B, V_C) is in the position shown in Fig. 5.4(a).

Under unity power factor, the three-phase input current vector is in the same position as the voltage vector. Therefore, the three phase currents are $i_a>0>i_b>i_c$. With six-step operation, the three phase currents should be regulated by using only the bridge vectors ***ppp***, ***ppn***, ***pnn***. Hence, node "a" is always connected to the positive rail, which means that switch S_{an} is never closed. Current i_a always flows through the upper anti-parallel diode of S_{ap}, and only S_{bp} and S_{cp} are switching and regulating the three

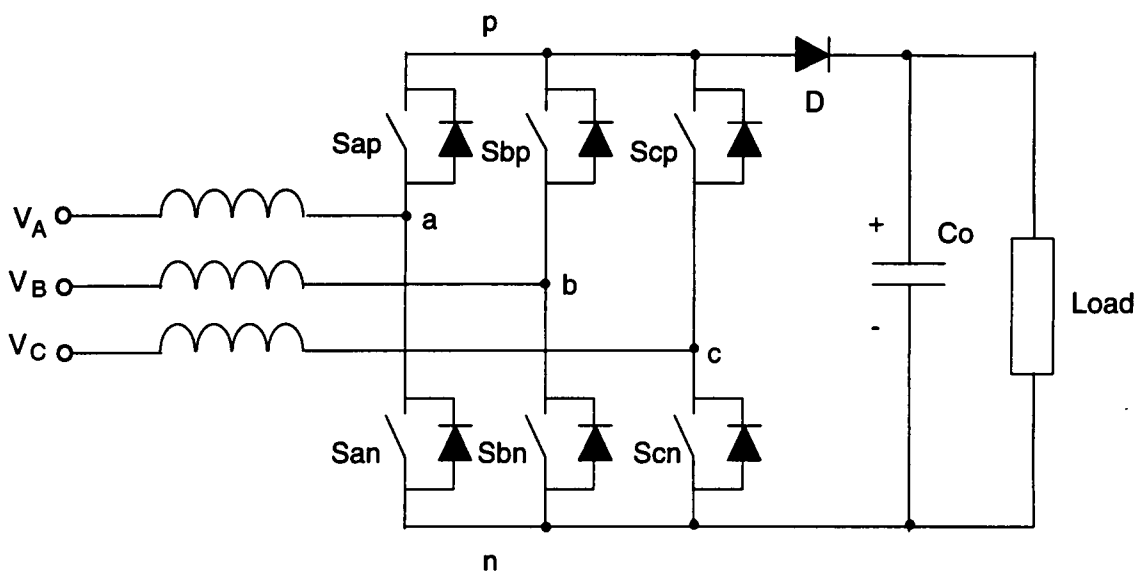
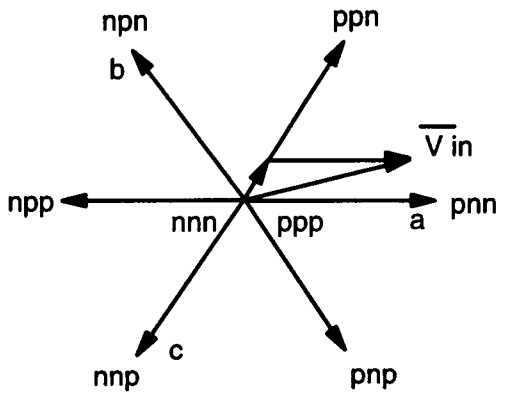
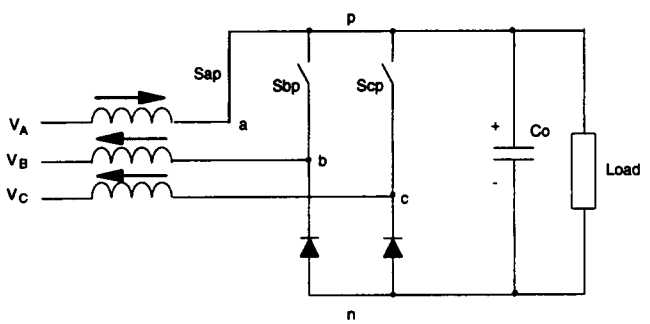


Fig. 5.3 Three-phase boost rectifier with a DC rail diode.



(a)



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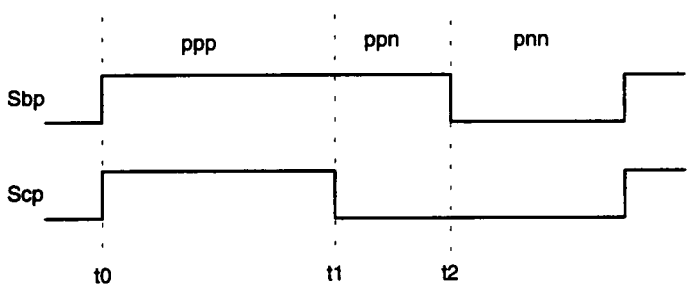


(c)

Fig. 5.4 Bridge voltage vectors and six-step PWM
(a) bridge voltage vectors; (b) equivant circuit; (c) driving signals.

phase currents (only two are independent). If the active switches are synchronized at their turn-on instants, the switch drive signals are shown in Fig. 5.4(c).

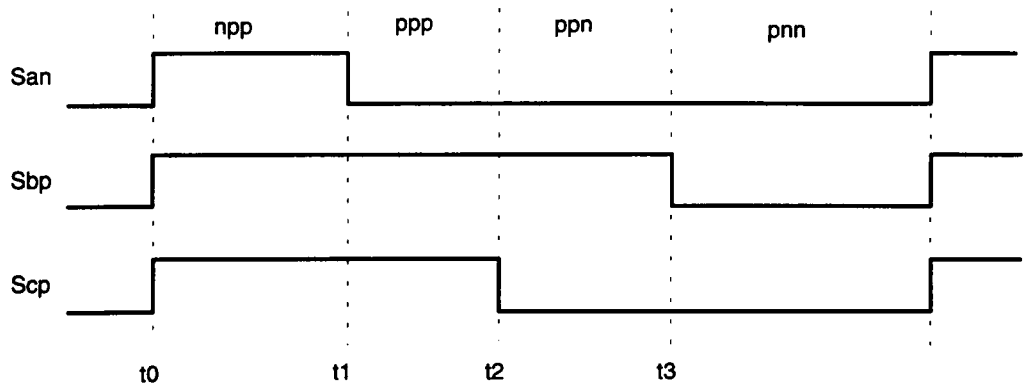
It can be seen that for the six-step operation, the switch in the phase with the largest current amplitude should be disabled. The phase with the largest current amplitude changes every 60°, which requires precious 60° detection. If the three independent current controllers are used without disabling the proper switch, as shown in Fig. 5.2, and if the turn-on instants are synchronized, the switch drive signals are shown in Fig. 5.5(a).

At the beginning of a switching cycle t_0, all three switches (S_{an}, S_{bp}, and S_{cp}) are turned on, and the resulting vector is ***npp***. At time t_1, S_{an} is turned off and the current in phase A will flow through the top diode. Since S_{bp} and S_{cp} are still closed, the bridge voltage vector must be ***ppp***, a zero vector. At time t_2, S_{cp} is turned off, which makes the bridge voltage vector to be ***ppn***. At time t_3, S_{bp} is also turned off and the bridge voltage vector becomes ***pnn***. Hence, the bridge voltage vector sequence within a switching cycle is ***npp - ppp - ppn - pnn***, as indicated in Fig. 5.5(b).

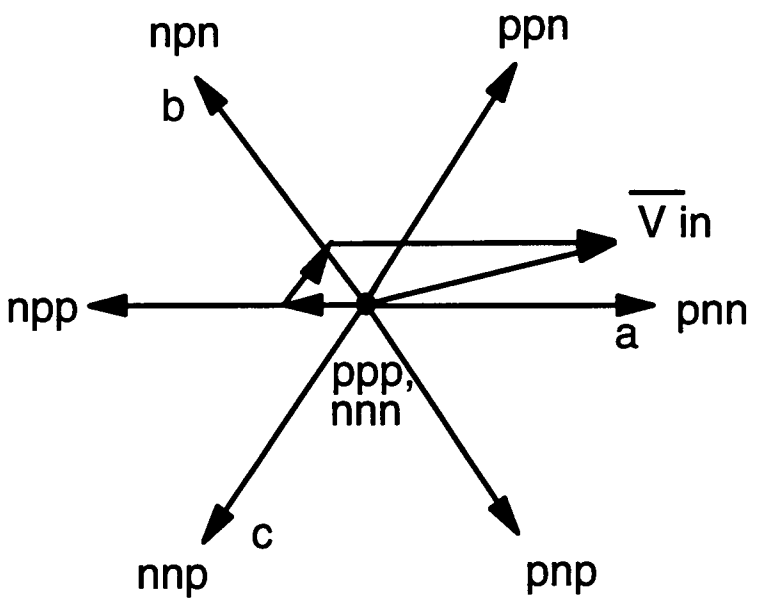
Compared with the six-step PWM described above, the first bridge voltage vector, ***npp***, is not the two adjacent vectors of the input line vector. Therefore, the conventional analog controlled three-phase boost rectifier does not operate under six-step PWM mode.

The non six-step PWM causes high input ripple current and circulating energy.

During the period of the first bridge voltage vector ***npp***, the equivalent circuit is shown in Fig. 5.6(a). The output voltage V_o is in series with the input line voltages, which makes the boost inductor currents increase faster than in the six-step PWM mode which only use the zero bridge voltage vector to charge the boost inductors.



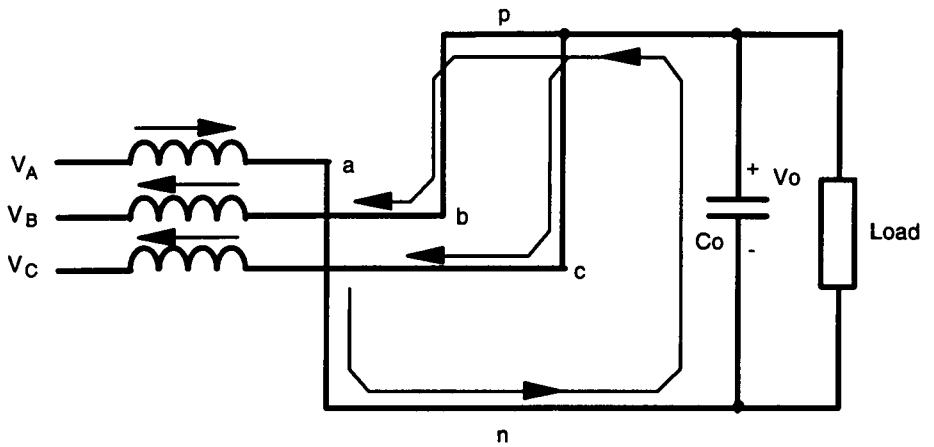
(a)



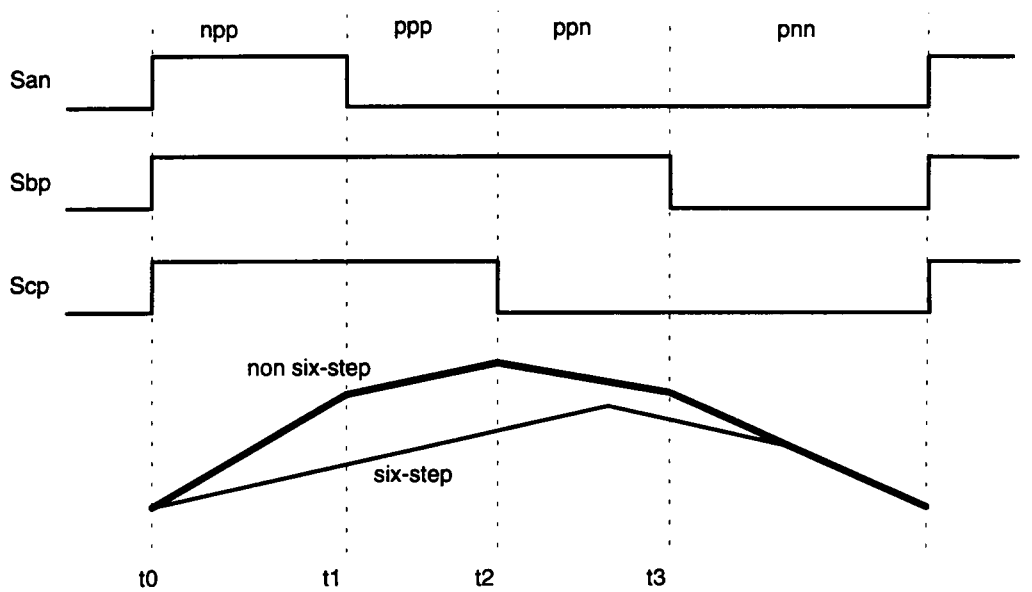
(b)

Fig. 5.5 Non six step PWM operation

(a) driving signals; (b) bridge voltage vectors.



(a)



(b)

Fig. 5.6 Drawbacks of the conventional analog controlled three-phase boost rectifier (a) output voltage in serious with the input voltage; (b) high input ripple currents.

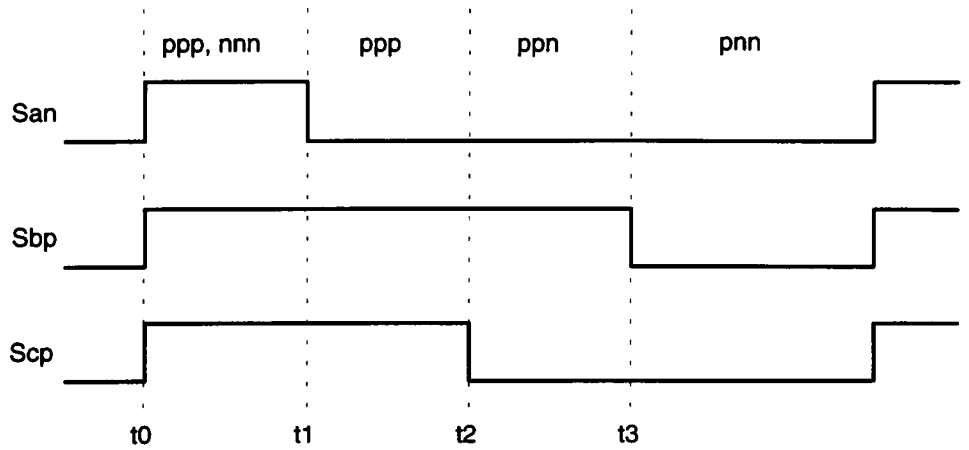
As a result, the input currents have higher ripple amplitudes than the desired ones. Figure 5.6(b) shows the phase A inductor current under both non six-step PWM and six-step PWM modes.

Another drawback is that the dc rail current direction is negative, which means the energy is sending back to the input side. Therefore, certain amount of circulating energy occurs every switching cycle.

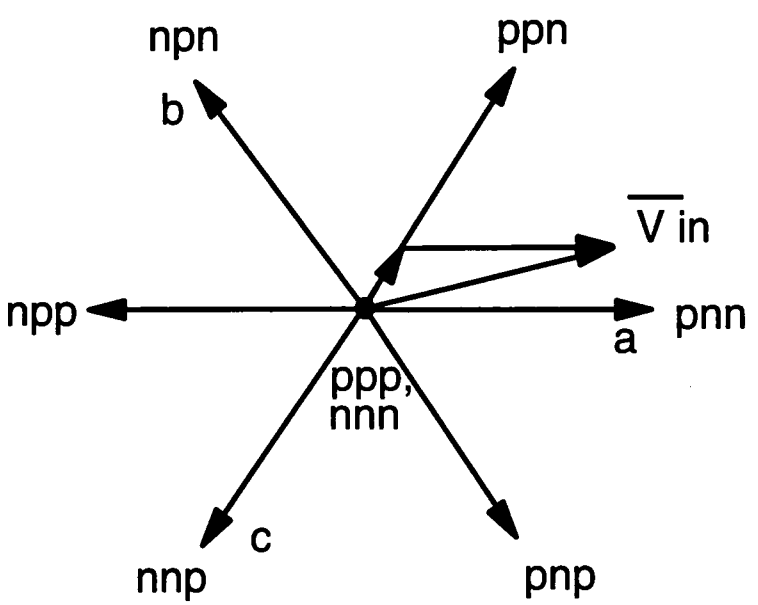
The situation is different in the proposed boost rectifier with a DC rail diode. As shown in Fig. 5.7, the vector ***npp*** will not occur even if S_{an}, S_{bp}, and S_{cp} are on at the same time, because the current cannot flow back from the output to the bridge. Instead, the bridge will stay in zero vector position, both ***ppp*** and ***nnn***, before time t_1. The turn-off of S_{an} at t_1 does not change the bridge zero vector, except for the fact that only ***ppp*** is used after t_1, which has no effect on the current control. Basically, the DC rail diode prevents the undesired vectors from occurring and guarantees the six-step operation even with three independent controllers, and no 60° detector is needed.

2 Alleviating diode reverse recovery

In the conventional three-phase boost rectifier shown in Fig. 5.1, at the moment when an active switch is turned on, the previously conducting diode in the same phase will be turned off with high reverse voltage, which is the output voltage and is above 400 V in most applications, causing severe reverse recovery loss. When MOSFETs are used, an ultra fast recovery diode and a Schottky diode have to be connected with each MOSFET to prevent its very slow body diode from conducting. In this way, twelve more diodes are needed. When using IGBTs, most anti-parallel diodes inside the package



(a)



(b)

Fig. 5.7 Driving signals for three independent controllers with the DC rail diode
(a) bridge switch driving signals; (b) bridge voltage vectors

are still much slower than the currently available ultra fast diodes. For IGBTs without built-in anti-parallel diodes, six external ultra fast diodes are necessary.

However, in the boost rectifier with the DC rail diode, the slow switching characteristic of the anti-parallel diodes will not show up, provided that the DC rail diode is an ultra fast recovery one. Therefore, only one ultra fast recovery diode can significantly alleviate the reverse recovery problem of all the bridge diodes.

3 No shoot-through problem

It is obvious that the DC rail diode eliminates the possibility of the bridge shoot-through. Hence, the most dangerous operational problem of the converter is removed, and system reliability is improved.

4 Implementing soft-switching

The most important advantage of the three-phase boost rectifier with the DC rail diode is that soft-switching can be implemented very easily. Several soft-switched three-phase boost rectifiers will be proposed in the next section.

5.4 Soft-Switched Three-Phase Boost Rectifiers

In rectifier applications, the switching frequency should be as high as possible to minimize the inductor size. Therefore, soft-switching is desired to minimize the

switching losses so that the converter can run at maximum switching frequency. Zero-voltage-switching (ZVS) can completely solve the diode reverse recovery problem and remove capacitive turn-on loss, while zero-current-switching (ZCS) can greatly reduce the turn-off loss of IGBT, GTO, etc.

Previously, the soft-switching techniques are solely developed for inverter operation and are quite complicated in terms of both power circuits and control. There are two types of conventional soft-switching techniques depending on the position of the auxiliary soft-switching network. One is the AC side soft-switching with an auxiliary soft-switching network on the AC side of the bridge (a,b,c); the other is the DC side soft-switching with an auxiliary soft-switching network on the DC side.

The Auxiliary Resonant Commutated Pole (ARCP) Technique [D-18] as shown in Fig. 5.8 is an example of the AC side soft-switching. The auxiliary soft-switching network consists of three bi-directional switches and three resonant inductors, which significantly increases the system complexity and cost. Thus, it does not seem attractive for simple rectifier applications.

The Zero-Voltage Transition Three-Phase PWM Rectifier/Inverter Technique [D-19] as shown in Fig. 5.9 is another example of the AC side soft-switching. The auxiliary soft-switching network is simpler than that of the ARCP rectifier, but still contains many components. Also, its operation requires more switching events of the main bridge switches and very high resonant inductor peak currents, which causes more switching and conduction losses. As a result, ZVS does not show enough advantage over the hard-switching. Besides, all AC side soft-switching techniques require sophisticated control. Therefore, the existing three-phase soft-switching techniques are not attractive for simple rectifier applications.

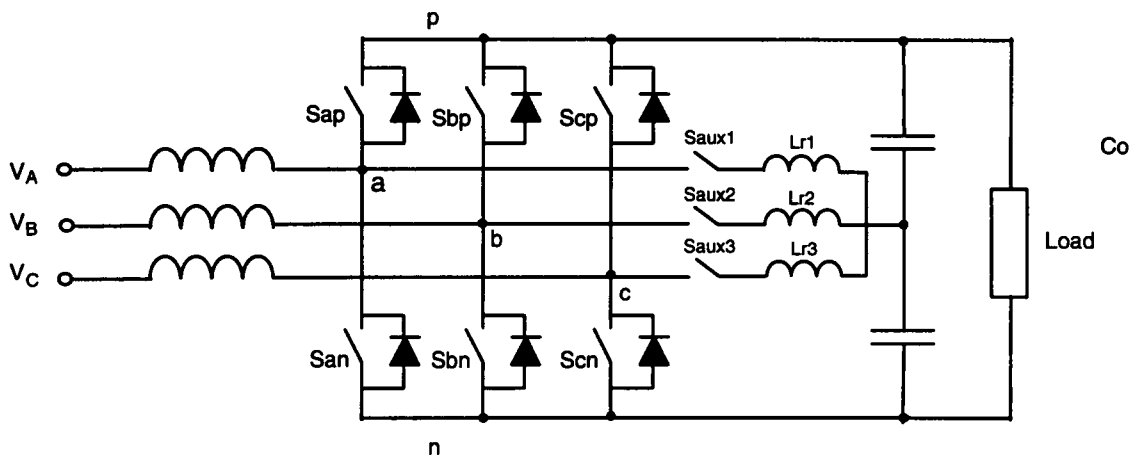


Fig. 5.8 Auxiliary Resonant Commutated Pole Three-Phase Boost Rectifier.

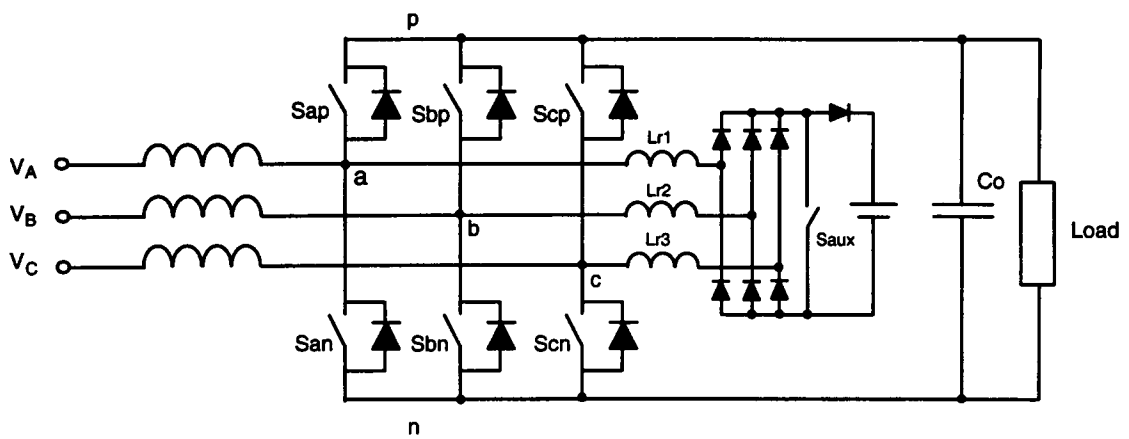


Fig. 5.9 Zero-Voltage Transition Three-Phase PWM Rectifier.

The best example of the DC side soft-switching technique should be the Resonant DC Link Technique [D-20] as shown in Fig. 5.10. It has simpler auxiliary soft-switching network than the AC side soft-switching techniques. But, the resonant components appear in the main power path, causing high voltage and current stresses on the bridge switches and significant amount of circulating energy. It also requires complicated control for the discrete PWM. Therefore, it is also not attractive for simple rectifier applications.

With the DC rail diode, it becomes possible to implement soft-switching PWM techniques on the converter DC side. In particular, the zero-voltage-transition (ZVT) [D-12], zero-current-transition (ZCT) [D-14], as well as the parallel MOSFET [D-15] techniques can be implemented in the same way as in a DC/DC converter.

5.4.1 ZVT Three-Phase Boost Rectifier

The ZVT three-phase boost rectifier is shown in Fig. 5.11, where an auxiliary network, consisting of resonant inductor L_r, switch S_{aux}, and diode D_{aux}, is added on the DC side. The operation principle is exactly the same as in a DC/DC ZVT converter [D-12], provided that the turn-on instants of the bridge switches in are synchronized as shown in Fig. 5.6. The auxiliary network only operates during the short turn-on transient at the beginning of a switching cycle. Before turning on the bridge switches, the auxiliary switch S_{aux} is turned on first, which allows a current to build up in the resonant inductor L_r. When the current in L_r reaches the largest input phase current, the DC rail diode stops conducting, and resonance begins between L_r and the equivalent capacitor across the bridge. This resonant process will bring the bridge voltage V_{pn} down to zero, and then the bridge switches are turned on. It can be seen that the DC rail diode

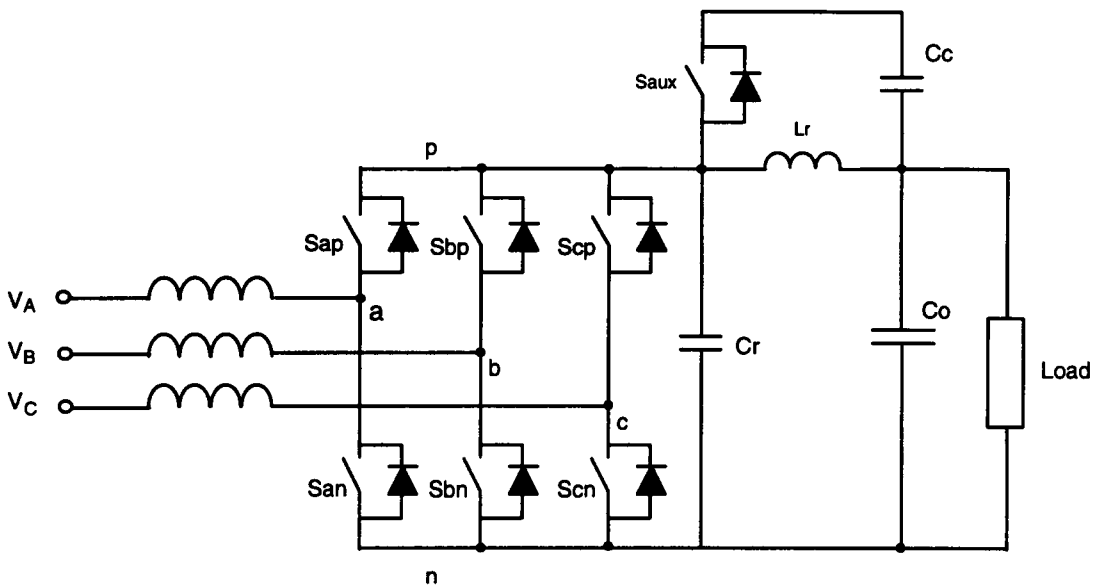


Fig. 5.10 Resonant DC Link Three-Phase Boost Rectifier.

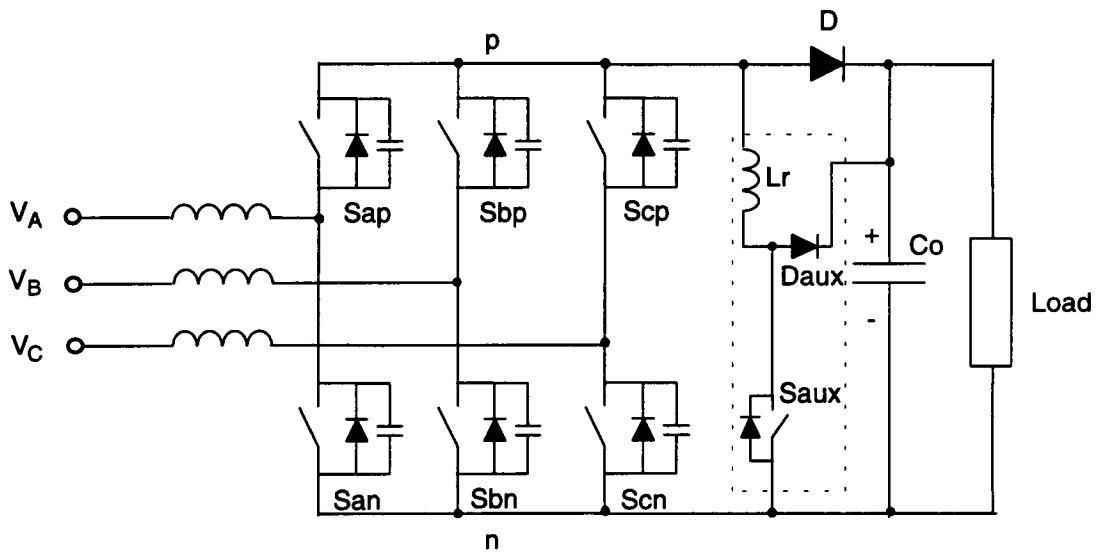


Fig. 5.11 Proposed ZVT three-phase boost rectifier.

is turned off softly, and the bridge switches are turned on under zero voltage condition without producing any turn-on losses theoretically. One can refer to ref.[D-12] for the detailed operation and design of the ZVT technique.

Though the ZVS is intended to eliminate the turn-on losses, it can also help to reduce the turn-off losses of slow devices, such as IGBTs, since external snubber capacitors can be added in parallel with those switches to slow down the voltage rising at the turn-off.

5.4.2 ZCT Three-Phase Boost Rectifier

The proposed ZCT three-phase boost rectifier is shown in Fig. 5.12, where the DC side auxiliary network consists of resonant inductor L_r, resonant capacitor C_r, switch S_{aux}, and diode D_{aux}.

The ZCT network only operates during the short turn-off transients of the bridge switches. In this case, the bridge switches should be synchronized at their turn-off instants so that the auxiliary ZCT network could only operate once per switching cycle. The basic principle is that the auxiliary switch is turned on to initiate a resonance between L_r and C_r before the main switches are turned off. This resonance will draw the currents away from the active switches to provide zero current turn-off condition. One can refer to [D-14] for the detailed operation and design of the ZCT technique.

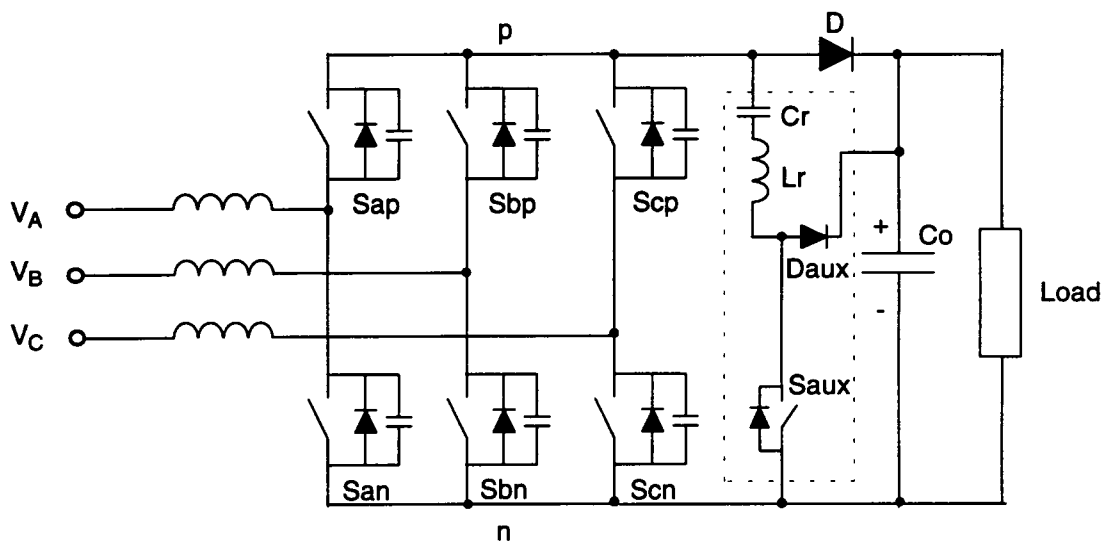


Fig. 5.12 Proposed ZCT three-phase boost rectifier.

5.4.3 MOSFET Helped IGBT Three-Phase Boost Rectifier

Another simple way of alleviating IGBT turn-off losses is to adopt the parallel MOSFET technique proposed in Chapter 3. Here this technique is quite attractive, since only one extra MOSFET is needed to assist all six bridge switches in achieving soft turn-off, as shown in Fig. 5.13.

The principle is that the bridge switches are synchronized at their turn-off; therefore, the last vector within a switching cycle is zero vector during which the auxiliary switch (FET) is turned on. At the instant when the bridge switches are turned off, the auxiliary switch is still closed, and it clamps the bridge voltage V_{pn} at a low level (only the on-voltage drop of the FET). After a short period (usually is 3-5 times of the IGBT turn-off time), the auxiliary switch is turned off, and the bridge voltage will rise. However, the recombination processes inside the IGBTs have been almost completed, and, therefore, very little current tails remain. As a result, the turn-off losses of the bridge IGBTs are greatly reduced. For the detailed operation principle and experimental results, one can refer to [D-15].

5.4.4 Choice of Soft-Switching Techniques

The choice between the ZVS and ZCS is mainly determined by the device characteristics, i.e. it is a trade-off between turn-on losses and turn-off losses. The ZVS technique eliminates turn-on losses and the ZCS technique removes turn-off losses. When using MOSFETs, the reverse recovery of the anti-parallel diodes is the major source of switching losses, and, therefore, the ZVS is more favorable. When using IGBTs, the reverse recovery of anti-parallel diodes and turn-off current tail are two major sources of switching losses. According to the study conducted in [D-38], the

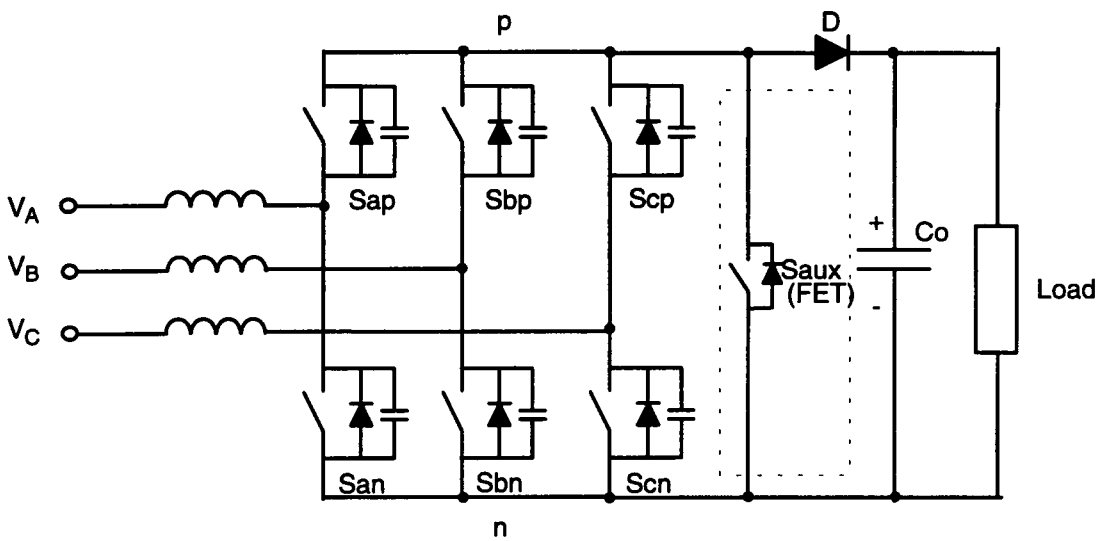


Fig. 5.13 MOSFET assisted IGBT boost rectifier.

diode reverse recovery loss of an ultra fast diode (55 ns reverse recovery time) is higher than the turn-off current tail losses of the currently available ultra fast IGBTs, and, hence, the ZVS still has better effect than the ZCS. However, this conclusion is only based on the particular devices (the diode and the IGBT). For example, if a much faster diode is used, or in certain circuits where there is no diode reverse recovery problem, the ZCS will play an important role in reducing the turn-off current tail loss. One can refer to [D-38] to see the comparison among hard-switching, ZVS, and ZCS techniques.

As to the choice between the ZCS and the parallel FET scheme, it can be seen that the ZCS provides better switching condition for the IGBTs and has less EMI. But, a drawback of the ZCS technique is the circulating energy which increases conduction loss, and sometimes might even worsen converter efficiency. The parallel FET technique will have a slightly higher switching loss than the ZCS since the FET on-voltage is applied on the IGBTs immediately after the IGBTs are turned off. But, it is simpler, and does not involve any circulating energy.

5.5 Experimental Results and Loss Breakdown

To verify the proposed rectifier experimentally, a 5 kW, 50 kHz prototype ZVT three-phase boost rectifier was constructed with three independent analog controllers. The bridge switches are IGBTs (CM50DY-24E), each of which has an anti-parallel diode in the package with 300 ns reverse recovery time. The DC rail diode is a 55 ns ultra fast reverse recovery one (BYT230PIV-800). The three boost inductors are 1 mH each.

Three single-phase PFC controllers (UC3854) are adopted to control the three-phase currents. These three controllers are synchronized at the switch turn-on for ZVT operation. The experimental waveforms of the three-phase currents are given in Fig. 5.14.

The ZVT operation waveforms are shown in Fig. 5.15. The resonant inductor current first builds up and reaches the boost inductor current; then, the resonance occurs, and the bridge voltage reduce to zero before the main switches are turned on.

The efficiency is the upper curve shown in Fig. 5.16. It was measured under 180 V line voltage and 350 V output dc voltage, with 50 kHz switching frequency. The loss analysis indicated that switching losses have been greatly reduced. According to the device test results [D-38], the efficiency of the hard-switched counterpart will be about 1.5% lower as indicated with the lower curve in Fig. 5.12. 1.5% difference of efficiency means 50% loss increase, which will significantly affect the selection of the switching frequency.

The loss breakdown in the following can also prove the effectiveness of the soft-switching technique.

The conduction losses of the bridge devices are calculated by multiplying the largest current of the three phase currents and the on-voltage drop of two devices. Take an example of 180V line voltage, 350V output voltage, 5 kW output power, and 97% efficiency. The phase current is $i = \frac{Po}{3\eta \cdot V_{phase}} = 16.5\,A$. The average current during the 60 degree, when a phase current is the biggest one, is $I = \frac{3}{\pi} \cdot \int_{\pi/3}^{2\pi/3} \sqrt{2} \times 16.5 \times \sin(\omega t)\, d(\omega t) = 22.3\,A$. According to the IGBT data sheet, the

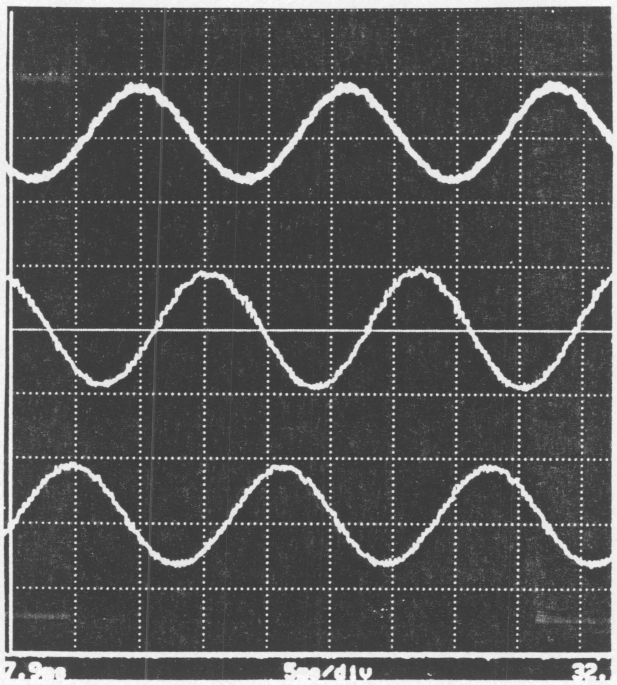


Fig. 5.14 Experimental waveforms of three-phase currents.

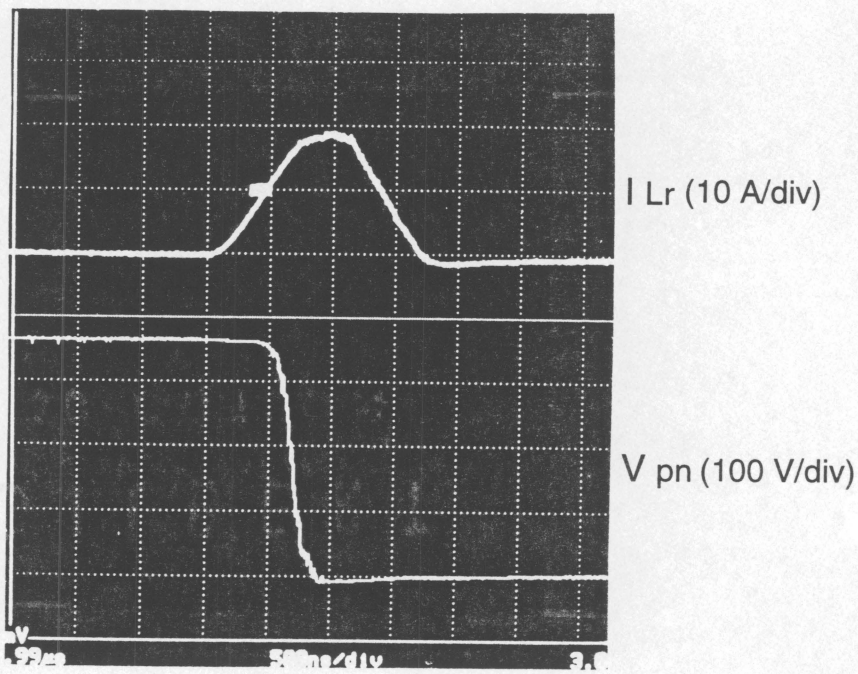


Fig. 5.15 Resonant inductor current and bridge voltage.

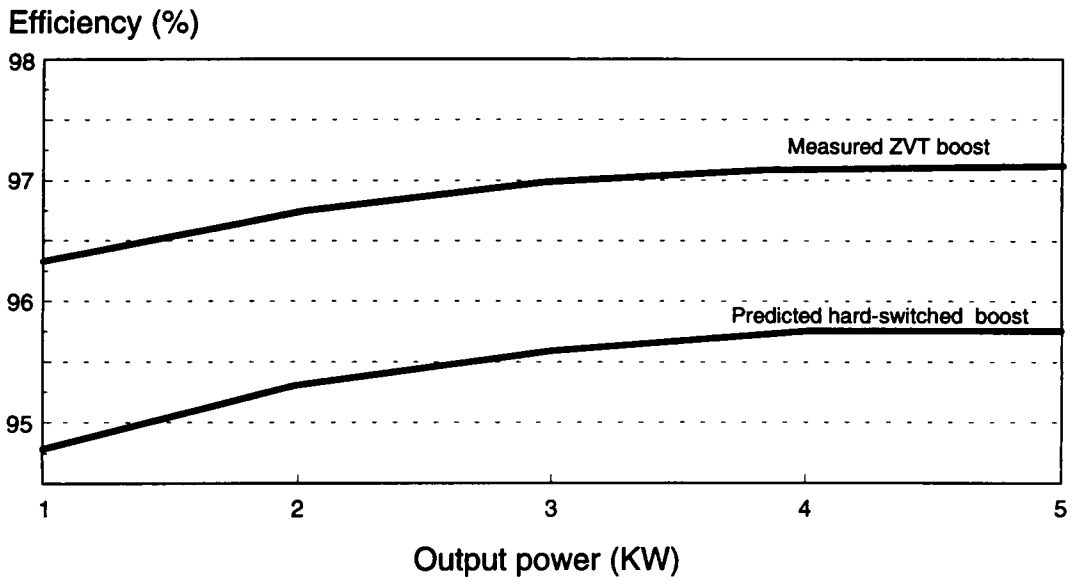


Fig. 5.16 Measured efficiency of the ZVT boost rectifier.

on-voltage of the IGBT and its anti-parallel diode used in the experiment are approximately 2V. Therefore, the conduction losses of the bridge devices are $P_{con1} = 22.3 \times 4 = 89W$. The conduction loss of the DC rail diode, which has 1.8 V on-voltage, is $P_{con2} = \frac{Po}{Vo} \times 1.8V = 26W$. The conduction loss of the ZVT auxiliary switches P_{con3} can be roughly calculated with a square current waveform of 22 A amplitude and 0.05 duty-ratio going through a MOSFET with on-resistance of 0.3 ohm (two in parallel). Hence, $P_{con3} = 0.05 \times 22^2 \times 0.5 = 7W$. If the other conduction loss of 5 W (boost inductor, auxiliary inductor, saturable inductor, and auxiliary diode) is counted, the total conduction losses are 89+26+12=127 W. Since the total losses at 97% efficiency is 150W, the switching losses are, therefore, only about 23W, which is mainly due to the IGBT turn-off current tail by comparing with the device test results [D-38]. So, the ZVT technique completely eliminated the turn-on switching losses.

5.6 Conclusions

The proposed three-phase boost rectifier with a DC rail diode has important advantages over the conventional three-phase boost rectifier. This DC rail diode guarantees six-step PWM operation, which produces the minimum input current ripple and no circulating energy. The bridge diode reverse recovery, which is a major problem in the conventional boost rectifier, can be greatly reduced by using an ultra fast diode on the DC rail. This new rectifier also has higher reliability than the conventional one, since the DC rail diode eliminates the bridge shoot through possibility. Also due to the DC rail

diode, soft-switching can be done on the DC side. Several simple soft-switched three-phase boost rectifiers were developed based on using the DC rail diode, including the ZVT, ZCT, and FET-helped three-phase boost rectifiers. These soft-switching techniques significantly reduce the switching losses and allow the converters to run at high switching frequency to achieve high power density. All these advantages were achieved with three simple independent analog controllers.

Consequently, these new three-phase boost rectifiers is simpler, cheaper, more reliable, and more efficient with high power density than the conventional one.

Chapter 6
Conclusions

This dissertation developed several novel high frequency switched-mode power factor correction techniques, which cover the major aspects of the PFC technology. The proposed techniques provide higher performances than the conventional approaches.

A novel single-phase PFC concept, the parallel PFC (PPFC), was established, which allows a large portion (68%) of the input power to be processed only once while the unity power factor and the tight output regulation are achieved.

Four PPFC implementation schemes were proposed. Scheme 1 utilizes three power stages within which the main power stage handles 68% of the average input power and controls the input current for PFC; while the other two stages handle 32% of the average input power each and regulate the output voltage. This configuration fits high power applications which require multi-modules in parallel when using the conventional two stage approach. However, for most single-phase applications, power levels are limited and such a three stage configuration is too complicated.

Scheme 2 is obtained by combining the two front stages of Scheme 1. The circuit implementation is simpler than that of Scheme 1. But, the transformer of the main power stage works with smaller duty-ratio which causes more conduction losses in the transformer and the output rectifier. Two isolation stages are still required and, therefore, it is only applicable for high power applications for which two isolation stages can be justified.

In Scheme 3, the 32% second time power processing is confined on the output side of the main power stage, which can be done with a bi-directional single-ended topology. Since only one isolation transformer is required, this scheme is simpler than Scheme 1 and 2. However, the bulk capacitor is on the low voltage side and is more bulky than that on the high voltage side as in Scheme 1 and 2.

Scheme 4 uses one power stage to implement the parallel PFC. By adding an auxiliary network together with the bulk capacitor on the primary side of the main power stage, the proper power flow can be achieved. Both flyback and boost single-stage PPFC converters are proposed. From practical point of view, a big advantage of these single-stage PPFC converters is that the bulk capacitor provides ideal clamp of the voltage across the primary switch(es), which is a major problem in current-fed topologies.

A device-based IGBT soft-switching technique was developed based on the mixed device concept. It can be used in isolated boost converters and the proposed three-phase boost rectifier, allowing IGBTs to run at high switching frequency.

Experiment and analysis on the single-stage PPFC converters verified that PPFC converters can have better efficiency and simpler circuitry than the conventional two-cascade-stage systems.

A novel three-level boost converter was proposed. This three-level boost converter requires devices rated at only half of the output voltage, and the input inductor current ripple, under the proposed operation principle, can be four times less in amplitude and twice higher in frequency compared with the conventional boost converter. According to the device characteristics and the magnetics knowledge, this new converter can significantly improve the converter power density and the efficiency for high power and/or high voltage applications. Larger signal simulation verified the proper operation.

This three-level boost converter will be very attractive for single-phase PFC, where high power and high voltage are often encountered.

For the three-phase PFC, a significant improvement was made on the conventional three-phase boost converter, which is the most frequently used converter topology in three phase PFC applications. This improved boost converter, differing from the conventional one with a DC rail diode, has several important advantages.

Due to the DC rail diode, this new boost converter provides automatic six-step PWM operation, which produces minimum input current ripple and no circulating energy. The DC rail diode also prohibits the dangerous bridge shoot-through possibility, and no particular attention needs for the drivers. By using a fast recovery DC rail diode, the severe reverse recovery losses of the bridge diodes, especially when using MOSFETs as the power switches, can be greatly reduced.

For high power and high frequency applications, soft-switching is desired. The DC rail diode allows soft-switching to be accomplished on the DC side very similar to what used in DC/DC converters. Three soft-switching techniques were adopted, including the zero-voltage transition, the zero-current transition, and the parallel MOSFET techniques. These new soft-switched three-phase boost converters, using simple analog controllers, are much simpler and more efficient than any previous ones.

In short, Improvements over the conventional three-phase boost converter can be seen in all major aspects: higher efficiency, higher reliability, simpler control, and easy soft-switching schemes.

The future work for the PPFC technique includes: 1). output current feedback control in the proposed PPFC converters to improve the output regulation performance; 2). hardware testing of the flyback PPFC converters, which would be valuable in many

applications for its simplicity; 3). small-single analysis and optimal design of the control loops of the PPFC converters; 4). other possible PPFC implementation schemes and circuits.

The future work of the three-level boost converter includes: 1). hardware testing to show how much improvement could actually be achieved under practical constrains; 2). control schemes dealing with the voltage balance of the two output capacitors; 3). small-signal analysis and optimal design of control loops; 4). higher level boost converter to fit for higher voltage applications.

The future work of the three-phase boost converter includes: 1). the control schemes dealing with the three-phase input voltage unbalance; 2). small-signal modeling and optimal design of control loops; 3). thorough comparison among the proposed soft-switching schemes based on typical applications.

Appendix A

Switch Duty-Ratios and Input Current Distortion in Single-Stage Boost PPFC Converter - PPFC Converter 6

The PPFC converter 6 is redrawn in Fig. A.1. The operation waveforms for $p_{in}>P_o$ is given in Fig. A.2 which is the same as Fig. 2.18(a).

Let $V_{in}=|V_{ac}|$, which is the rectified input voltage, considering the inductor voltage-second balance, the power relation, and the duty-ration limitation, the following four equations can be formed.

$$V_{in} = D_1' V_B + D_1'' V_o' \tag{A.1}$$

$$I_L V_o' D_1'' = P_o \tag{A.2}$$

$$I_L = p_{in} / V_{in} \tag{A.3}$$

$$D_1 + D_1' + D_1'' = 1 \tag{A.4}$$

Substitute (A.3) into (A.2):

$$\begin{aligned} D_1'' &= \frac{V_{in} P_o}{p_{in} V_o'} \\ &= \frac{V_m \cdot \sin(\omega t) \cdot P_o}{2P_o \cdot \sin^2(\omega t) \cdot V_o'} \\ &= \frac{V_m}{2V_o' \sin(\omega t)} \end{aligned} \tag{A.5}$$

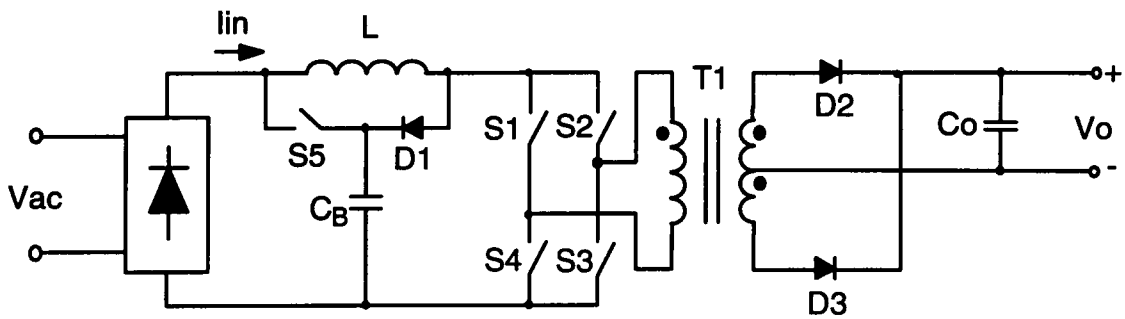


Fig. A.1 PPFC converter 6.

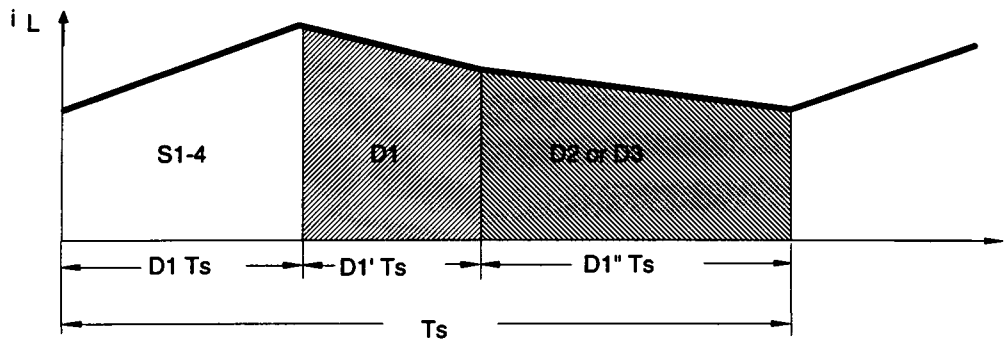


Fig. A.2 Operation waveform of PPFC converter 6 for $p_{in} > P_o$.

Substitute (A.5) into (A.1):

$$\begin{aligned} D_1' &= \frac{V_{in} - D_1'' V_o'}{V_B} \\ &= \frac{2V_m \cdot \sin^2(\omega t) - V_m}{2V_B \cdot \sin(\omega t)} \\ &= -\frac{V_m \cdot \cos(2\omega t)}{2V_B \cdot \sin(\omega t)} \end{aligned} \tag{A.6}$$

Substitute (A.5) and (A.6) into (A.4):

$$\begin{aligned} D_1 &= 1 - D_1' - D_1'' \\ &= 1 + \frac{V_m}{2V_B} \cdot \frac{\cos(2\omega t)}{\sin(\omega t)} - \frac{V_m}{2V_o' \sin(\omega t)} \end{aligned} \tag{A.7}$$

The operation waveform of $p_{in}<P_o$ is shown in Fig. A.3

The duty-ratio of the switch S_5 can be calculated by solving Eq. (A.8) and (A.9).

$$I_L \cdot (1 - D_{s5}) = I_{in} \tag{A.8}$$

$$I_L \cdot D_{s5} \cdot V_B = P_o - p_{in} \tag{A.9}$$

Divide (A.8) by (A.9):

$$\begin{aligned} \frac{1 - D_{s5}}{D_{s5} \cdot V_B} &= \frac{i_{in}}{P_o - p_{in}} \\ &= \frac{I_m \cdot \sin(\omega t)}{P_o(1 - 2\sin^2(\omega t))} \end{aligned} \tag{A.10}$$

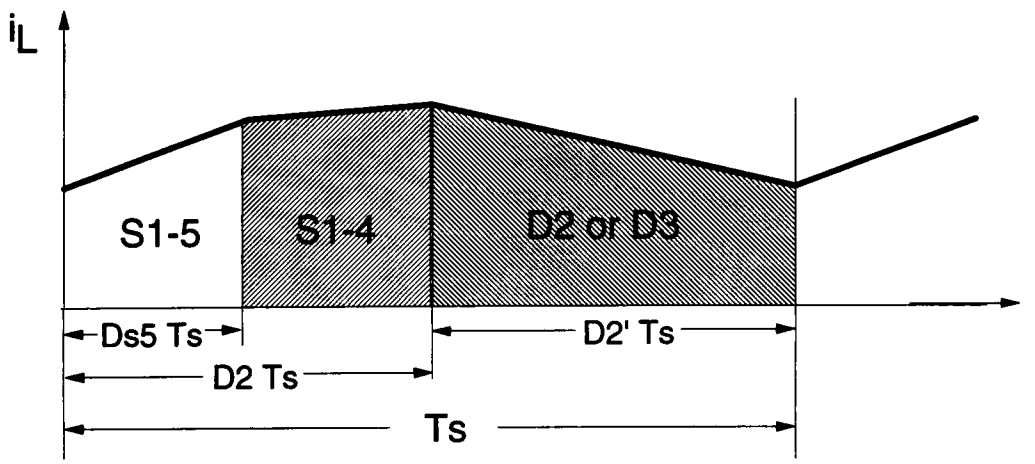


Fig. A3 Operation waveform of the PPFC converter 6 for $p_{in} < P_o$.

Hence,

$$\frac{1}{D_{s5}} = \frac{I_m \cdot V_B \cdot \sin(\omega t)}{P_o(1-2\sin^2(\omega t))} + 1 \qquad \text{(A.11)}$$

which gives:

$$D_{s5} = \frac{1-2\sin^2(\omega t)}{1-2\sin^2(\omega t) + 2\frac{V_B}{V_m}\sin(\omega t)} \qquad \text{(A.12)}$$

The duty-ratio of the bridge D_2 (taking the full-bridge as one switch) can be found from the following by the voltage balance of the inductor:

$$D_{s5} \cdot V_B + (1 - D_{s5}) \cdot V_{in} = (1 - D2) \cdot V_o' \qquad \text{(A.13)}$$

Therefore,

$$\begin{aligned} D_2 &= 1 - \frac{D_{s5} \cdot V_B + (1 - D_{s5}) \cdot V_{in}}{V_o'} \\ &= 1 - \frac{V_{in}}{V_o'} - \frac{V_B - V_{in}}{V_o'} D_{s5} \end{aligned} \quad , \qquad \text{(A.14)}$$

$$D_2' = 1 - D_2 \qquad \text{(A.15)}$$

To this point, all the duty-ratios have been found. The distortion occurring at the input voltage zero-crossing area is analyzed in the following:

The input current will not be able to follow its sinusoidal reference when the bridge boost duty-ratio reaches zero, which means no bridge-short period and the transformer is always operating.

So, let D_2=0, from Eq. (A.14), it is obtained that

$$D_{s5} = \frac{V_o' - V_{in}}{V_B - V_{in}} \tag{A.16}$$

Since the inductor current I_L equals the primary reflected output current I_o' at this time, therefore,

$$\begin{aligned} i_{in} &= I_L(1 - D_{s5}) \\ &= I_o'(1 - D_{s5}) \\ &= I_o' \frac{V_B - V_o'}{V_B - V_{in}} \end{aligned} \tag{A.17}$$

Since this is the boundary where input current starts to be distorted, the input current should still equal to its reference. Hence, from Eq. (A.17), the following equation is obtained.

$$I_m \cdot V_m \cdot \sin^2(\omega t) - I_m \cdot V_B \cdot \sin(\omega t) + I_o'(V_B - V_o') = 0 \tag{A.18}$$

Solving for sin(ωt) in Eq. (A.18) results in Eq. (A.19)

$$sin(\omega t) = \frac{V_B}{2V_m} \pm \frac{\sqrt{(2P_o \cdot V_B / V_m)^2 - 8P_o \cdot I_o'(V_B - V_o')}}{4P_o} \qquad \text{(A.19)}$$

This gives the point where input current distortion starts to occur.

Take an example of V_B=400 V, V_o'=375 V, V_m=127 V, and P_o=1 kW, it can be found from Eq. (A.19) that distortion only occurs within the region of about 1.7° around the input voltage zero-crossing point. Therefore, this effect is negligible, which agrees with the experimental results.

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