

Modeling, Control and Design Considerations for Modular Multilevel Converters

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ABSTRACT

This thesis provides insight into state-of-the-art Modular Multilevel Converters (MMC) for medium and high voltage applications. Modular Multilevel Converters have increased in interest in many industrial applications, as they offer the following advantages: modularity, scalability, reliability, distributed location of capacitors, etc. In this study, the modeling, control and design considerations of modular based multilevel converters, with an emphasis on the reliability of the converter, is carried out. Both modular multilevel converters with half-bridge and full-bridge sub-modules are evaluated in order to provide a complete analysis of the converter. From among the family of modular based hybrid multilevel converters, the newly released Alternate Arm Converter (AAC) is considered for further assessment in this study. Thus, the modular multilevel converter with half-bridge and full-bridge power cells and the Alternate Arm Converter as a commercialized hybrid structure of this family are the main areas of study in this thesis. Finally, the DC fault analysis as one of the main issues related to conventional VSC converters is assessed for Modular Multilevel Converters (MMC) and the DC fault ride-through capability and DC fault current blocking ability is illustrated in both the Modular Multilevel Converter with Full-Bridge (FB) power cells and in the Alternate

Arm Converter (AAC). Accordingly, the DC fault control scheme employed in the converter and the operation of the converter under the fault control scheme are explained.

The main contributions of this study are as follows: The new D-Q model for the MMC is proposed for use in the design of the inner and outer loop control. The extended control scheme from the modular multilevel converter is employed to control the Alternate Arm Converters. A practical reliability-oriented sub-module capacitor bank design is described based on different reliability modeling tools. A Zero Current Switching (ZCS) scheme of the Alternate Arm Converter is presented in order to reduce the switching losses of the Director Switches (DS) and, accordingly, to implement the ZCS, a design procedure for the Arm inductor in the AAC is proposed. The capacitor voltage waveform is extracted analytically in different load power factors and the waveforms are verified by simulation results. A reliability-oriented switching frequency analysis for the modular multilevel converters is carried out to evaluate the effect of the switching frequency on the MMC's operation. For the latter, a DC fault analysis for the MMC with Full-Bridge (FB) power cells and the AAC is performed and a DC fault control scheme is employed to provide the capacitor voltage control and DC fault current limit, and is illustrated herein.

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Chapter 1 Introduction

1.1 Motivation and Application Background

Power electronics are fundamental components in consumer electronics and clean energy technologies [1], [2]. For today's high-power applications, multilevel converters are gaining a lot of attention, and are becoming one of the top clean power and energy conversion choices for new topologies and control in industry and academia [3]–[10]. Currently, multilevel converters are commercialized in standard and customized products that power a wide range of applications, such as compressors, extruders, pumps, fans, grinding mills, rolling mills, conveyors, crushers, blast furnace blowers, gas turbine starters, mixers, mine hoists, reactive power compensation, marine propulsion, high-voltage direct-current (HVDC) transmission, hydropumped storage, wind energy conversion, and railway traction, to name a few [3]–[10]. Several well-known companies offer multilevel converters commercially for these applications in the field [11]–[16]. In Figure 1-1, the applications of multilevel converters are shown. Although the technology of multilevel converters is already developed such that they can be considered a mature and proven technology, they still have quite a few associated challenges. These challenges motivate researchers from all over the world to discover new ways to further energy efficiency, reliability, power density, simplicity for, and reduce costs of,

multilevel converters, and broaden their application field as they become more attractive and competitive than the classic topologies.

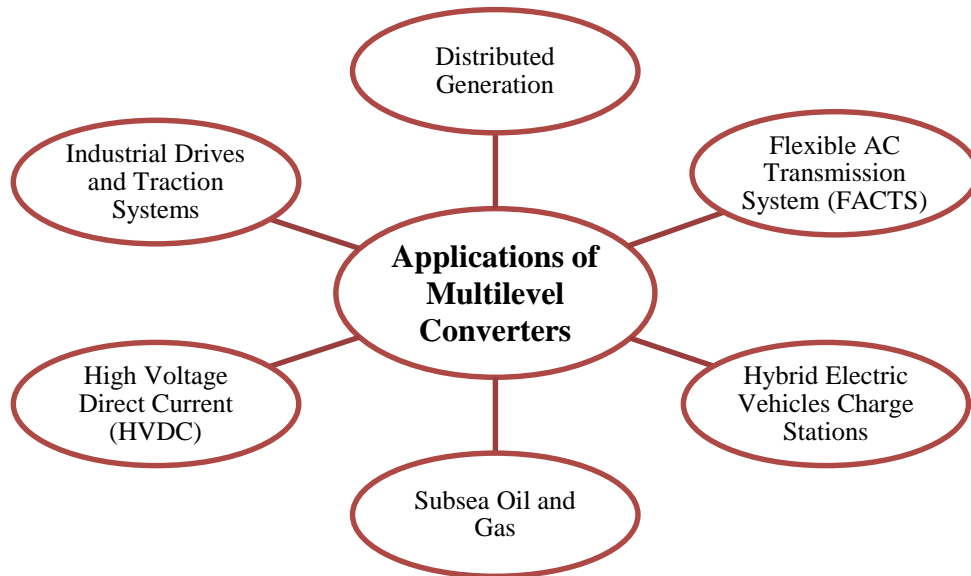


Figure 1- 1: Applications of Multilevel Converters

The idea of multilevel converter topologies began with the introduction of the cascaded H-bridge (CHB) converter in the late 1960s [17]. The first concept was the stepped-wave switching power converter circuit using a series-connected H-bridge. In the same year, the Flying Capacitor multilevel topology was introduced for low-power applications [18]. Afterward, the concept of the diode-clamped converter was proposed in the late 1970s [19]. The three-level Neutral Point Clamped (3L NPC) converter was developed based on the diode-clamped converter concept and was the first commercialized multilevel converter used in medium voltage applications [20]. The concept of the CHB was reintroduced in the 1980s and the technology came into industries in the mid-1990s [21]. Similarly, Flying Capacitor converters reached increased industrial relevance in the early 1990s [22].

These multilevel voltage source converter topologies classifications are shown in Figure 1-2. The topologies of interest in this thesis are shown in the last row of the figure. The hybrid topologies are basically a combination of the existant multilevel converter topologies joined together to obtain a new multilevel structure, which can provide superior performances in some aspects. The Alternate Arm Converter (AAC), from the family of modular based multilevel converters, was recently released as the hybrid VSC converter [23]. The emergence of modular based multilevel converters (MMC) occurred due to a lack of the following features in the multilevel VSC converters: modularity; high availability, including redundant operation; failure management; reliability; and simple structure-based converter design.

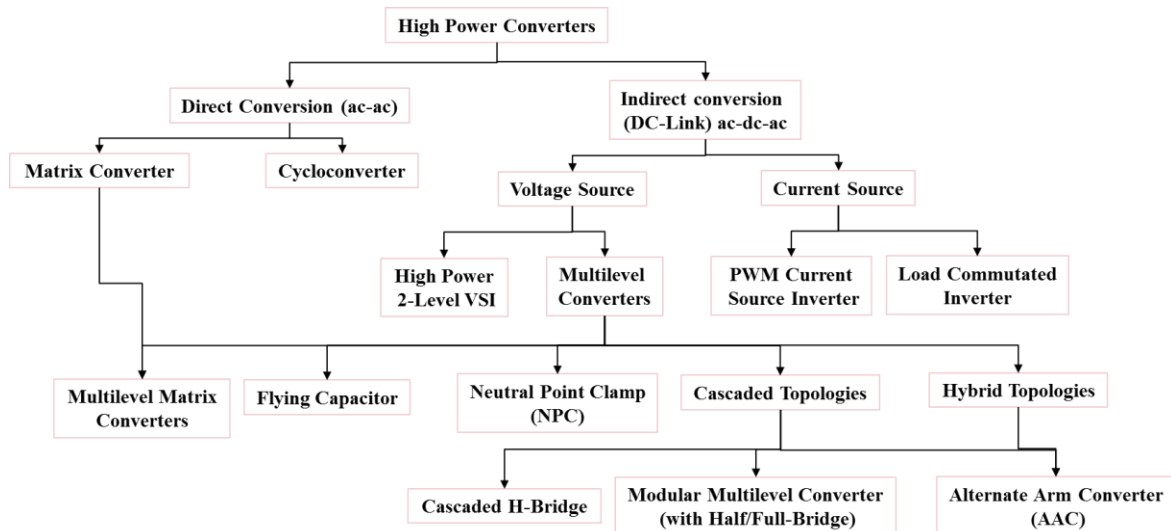


Figure 1- 2: Multilevel Converters' classifications

The Modular Multilevel Converters' technology, as shown in [24], [25] offered the following advantages:

- 1) modular design;
- 2) simple voltage scaling by a series connection of cells;
- 3) distributed location of capacitive energy storage;
- 4) filterless configuration for standard

machines or grid converters [high-level number, low total harmonic distortion (THD)]; 5) high resulting switching frequency; 6) simple realization of redundancy; 7) high front-end flexibility (e.g., 12p, 18p, 24p diode or active); 8) grid connection via standard transformer or transformerless.

There are some disadvantages associated with this topology, the main drawbacks being the higher number of semiconductors and gate units, and the relatively high circulating current existence in the MMC due to its intrinsic features during operation. Furthermore, the total stored energy of the distributed capacitors is distinctly higher as compared to that of a conventional 2L-VSC or 3L-NPC-VSC. Many studies have been done and are ongoing to tackle these problems, and MMCs still have a high potential to become more pervasive in medium and high power applications.

1.2 Topology Evaluations

The conceptual background of the MMC comes back to the two-level voltage source converter when there are top and bottom switches in each arm of the converter. The problem with the two-level converter in medium and high power applications is extremely high converter switching losses, as achieving a desirable harmonic content in the converter, requires a high switching frequency. Therefore, there needs to be an alternative converter that provides lower switching losses while achieving high voltage ratios. Figure 1-3 shows how the modular multilevel converter idea first developed.

By replacing the single switch or series connected switches, which normally is an insulated-gate bipolar transistor (IGBT) with a series of single-phase two-level converters

sub-modules where each SM can be typically realized by the half-bridge converter, the MMC topology was formed [26].

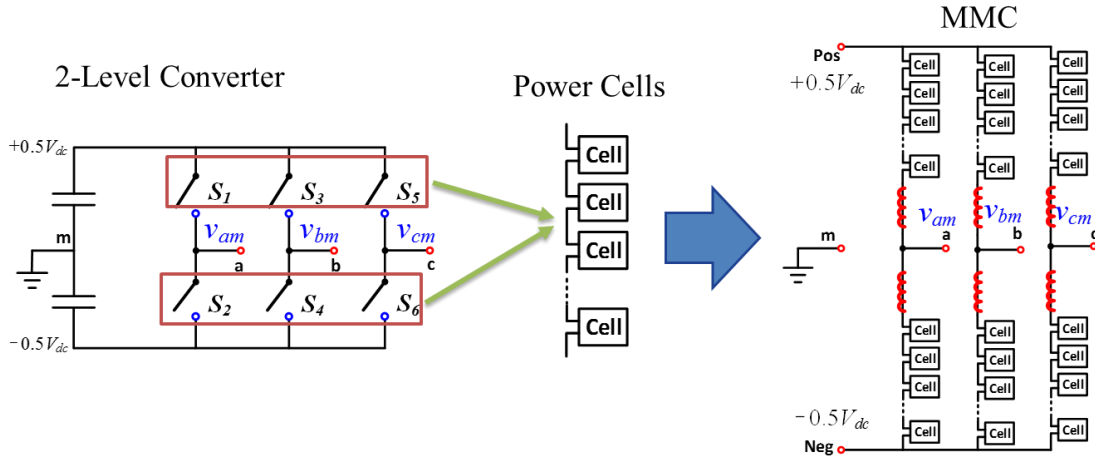


Figure 1- 3: Modular Multilevel Converter conceptual realization

By employing a series of connected half-bridge cells, the switching frequency associated with the converter can be reduced significantly – to frequencies around the line frequency [27]. Figure 1-4 illustrates the single phase voltage waveform in the two level voltage source converter versus the voltage waveform in the realized multilevel level converter in the two level VSC.

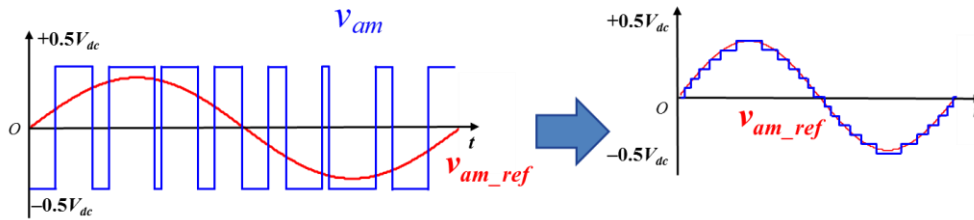


Figure 1- 4: Voltage waveform in the two-level voltage source and Modular Multilevel Converter

Using this knowledge, further topologies can be made by using different circuit topologies as a module in the modular-based multilevel structure. As seen in Figure 1-3, the modular multilevel converters include two arms per phase, where in each arm several

identical sub-modules are connected in series. Conventionally, the topology known as MMC for today's industrial applications consists of series connection of the half-bridge modules in each arm. However, each cell can be a half-bridge, full-bridge, or series of switches (IGBT). Figure 1-5 shows the possible building blocks of the cell in the MMC that can form different topologies from the basic frame of the MMC.

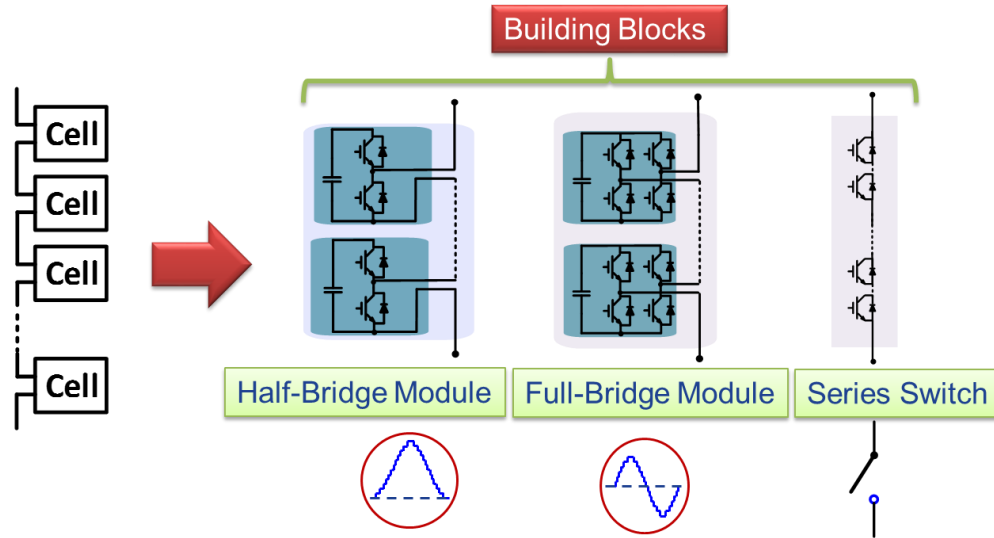


Figure 1- 5: Building blocks for the MMC that have been commercialized so far

The half-bridge power cells can only generate positive voltage, while the full-bridge modules have the ability to produce the negative voltages as well, as shown in Figure 1-5. The series connections of the switches can be used either inside the module to generate modules with higher power rates or in series or parallel to generate so called hybrid modular based multilevel converters [23]. The wave-shaping circuit is used to define the series connected model of the described building blocks [28].

1.3 Hybrid Modular Multilevel Converters

The advantage of the two-level converter is that it contains the smallest total number of semiconductors. The main disadvantage is that it can only have a two-state in the output, and thus requires high switching frequency to obtain a sinusoidal output waveform. The MMC with Half-Bridge power cells provides a solution for the power losses due to high switching frequency in the two-level converter at the expense of having double the number of switches and a very large amount of capacitance. The main disadvantage of the MMC with half-bridge is its inability to block the current path during the DC fault. In contrast, the full-bridge MMC topology permits the ride-through capability of the configuration and suppression of the DC faults, but again, requires twice as many semiconductors. A number of interesting converter topologies which combine the features and advantages of both of the MMC and two-level converters have been highlighted recently in the literature [29].

1.3.1 Hybrid Converter with a Waveshaping Circuit on the AC Side

Figure 1-6 shows the configuration of the hybrid converter with a waveshaping circuit on the AC side. The configuration of the converter consists of a two-level converter, which is connected in series with the waveshaping circuit. The two-level converter operates normally and a squarewave output is produced at its AC terminal; the wave-shaping circuit produces the difference between the two-level converter output and the desired (sinusoidal) output voltage. Using this technique, the two-level converter can operate at a much lower switching frequency than in the case without the waveshaping converter. This enables the two-level converter to operate even at the switching

frequency of only twice per cycle [30]. The advantages of this topology are the DC fault blocking capability and the generation of an almost perfect sinusoidal waveform, although this requires careful synchronization between the two-level converter and wave-shaping circuit. The disadvantages, as noted, are the precise synchronization requirements between the two combined circuits to avoid high voltage spikes, and the power losses of the converter due to the two-level converter bridge required to operate with hard switching and the resultant relatively high switching losses. Since the voltage required in the AC side is symmetric, the full-bridge wave-shaping circuit is required to generate the notch waveform with respect to the square waveform generated by the two-level converter.

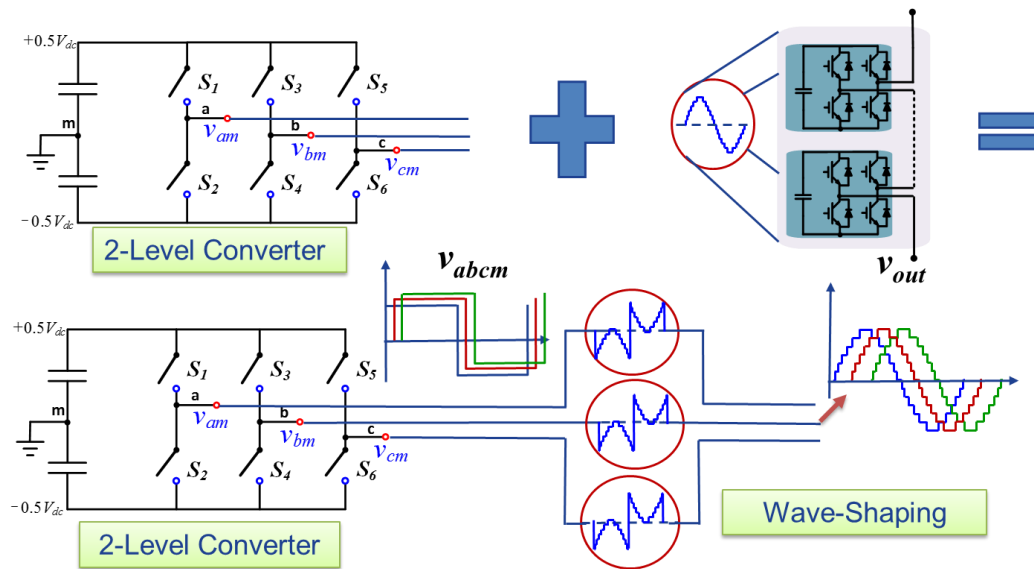


Figure 1- 6: Hybrid Voltage Source Multilevel Converter with Wave-shaping circuit on the AC side

1.3.2 Hybrid Converter with a Waveshaping Circuit on the DC Side

The single-phase, two-level converter full-bridge “H-bridge” converter is a building block in several converters, such as the cascaded H-Bridge converter, etc[31].

Specifically, in high power, high voltage applications, the series of full-bridge converters is used as a STATCOM to compensate for the reactive power [32]. One inevitable fact about the two-level converter is that any voltage ripple on the DC side will be delivered to the AC side, which usually is undesirable. The basic idea of this family of hybrid converter is adopting the wave-shaping circuit on the DC side of the two-level converter and making the DC capacitor active instead of passive. Figure 1-7 shows the concept of the active DC capacitor with a wave-shaping circuit [29], [33].

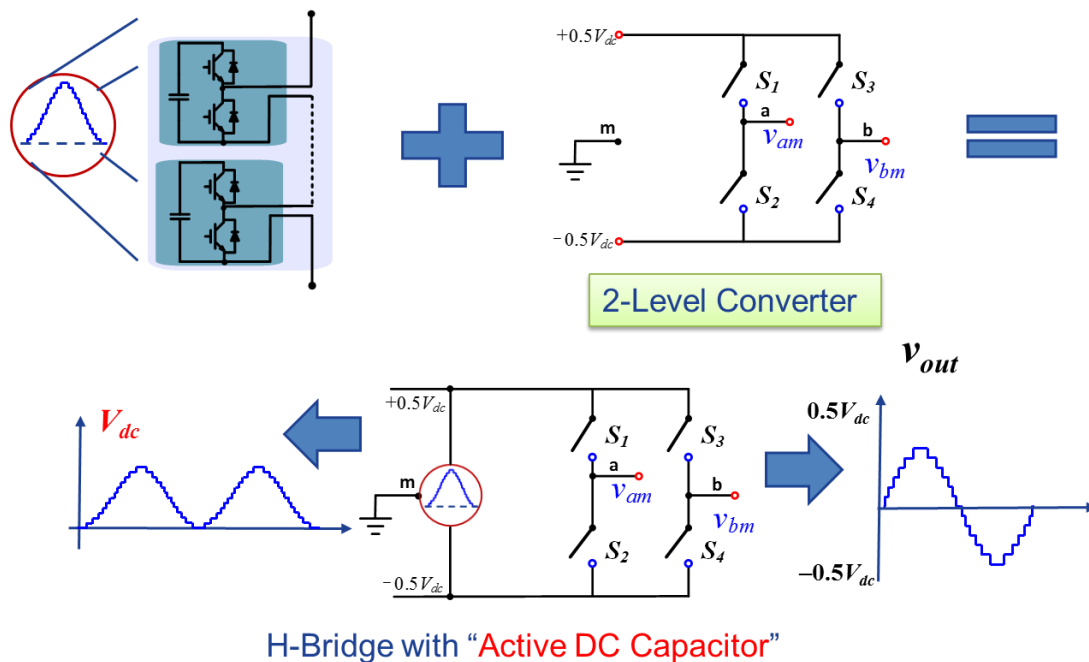


Figure 1- 7: H-bridge converter with Active DC Capacitor and wave-shaping circuit on the DC side

By using the active DC capacitor in parallel with the full-bridge converter, a low harmonic content multilevel-based voltage source converter can be made. A single phase of that is shown in Figure 1-7. To achieve a three-phase structure, three of the single phase structures should be connected in series on the DC side. On the AC side, each should be connected to the separated transformers as shown in Figure 1-8 [34].

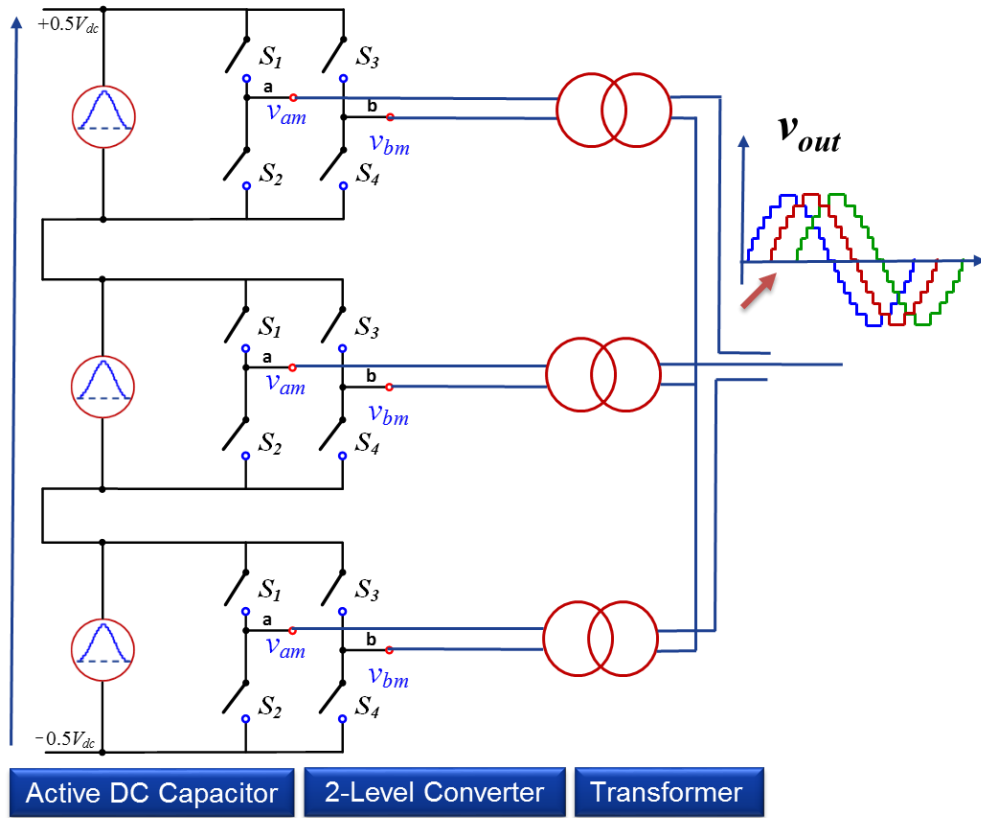


Figure 1- 8: Hybrid Converter with Wave-Shaping circuit in parallel with H-Bridges

There are some advantages to this structure discussed in the literature [35]. First, since the positive voltage is required to be generated on the DC side, the half-bridge power cells are sufficient for use on the wave-shaping circuit. Also in this structure, three wave-shaping circuits are required and these are located outside of the main current path. As a result, the semiconductor power losses are expected to be lower. The fault ride-through capability is another main advantage of this converter, since during the fault the DC side voltage can be controlled to zero [34]. The main drawback of this converter is the existence of the transformer which increases the size and weight of the converter. Furthermore, there are two times as many switches on the converter, and since the two-level converter switches operate at higher losses, this is not desirable.

1.3.3 Alternate-Arm Converter (AAC), Hybrid Converter with Wave-Shaping Circuit on DC side

In the Alternate-Arm Converter structure, the wave-shaping circuits are placed on the DC side of the main two-level converter [36]. In the AAC, the complete converter consists of a standard two-level converter with each arm including both high voltage switches (series of IGBTs) and a wave-shaping circuit in series. Since the wave-shaping circuit should generate negative voltages, full-bridge sub modules are used in this converter. Figure 1-9 shows the formation concept of the AAC.

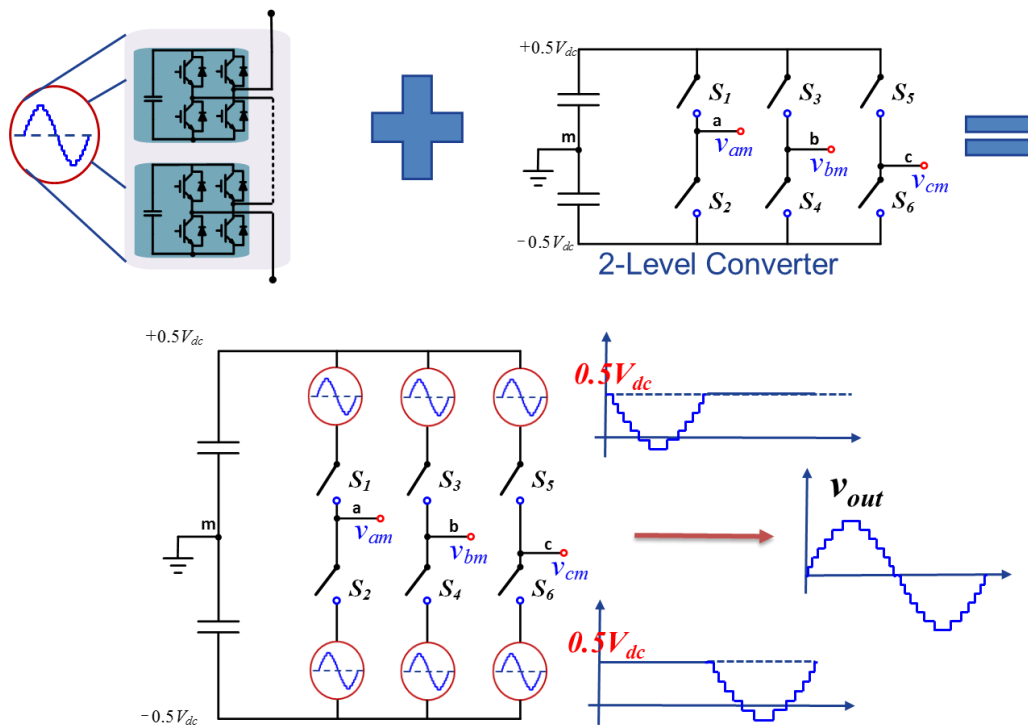


Figure 1- 9: Alternate-Arm Converter: series of director switches with wave-shaping circuit on the DC side

1.3.4 VSC-HVDC Using Multilevel Technology Review

The three manufacturers of VSC HVDC (i.e. ABB, Siemens and Alstom Grid) have recently produced their own solutions for the modular based multilevel converters towards the AC and DC grid side. Figure 1-10 shows the modular multilevel converter with different sub-modules used by each of aforementioned manufacturers. After the introduction of the MMC by Lesnicar and Marquardt [24], the first demonstration of the converter in the HVDC application was performed by Siemens in 2007. Since then, the converter has gained popularity due to its advantages over conventional topologies. The multilevel topology as commercialized by Siemens is called ‘HVDC PLUS’ [37]. ABB proposed its own MMC technology, called ‘HVDC Light,’ using press-pack IGBTs in the valves as in the traditional two-level converter[38]. Also, Alstom developed a multilevel topology, which adopts the hybrid concept for VSC and takes advantage of having the capability to block the DC fault. The MMC converter commercialized by Alstom is called ‘MaxSine’ [23]. Figure 1-11 demonstrates the commercialized VSC-HVDC modular based multilevel converters from Siemens, ABB and Alstom Grid.

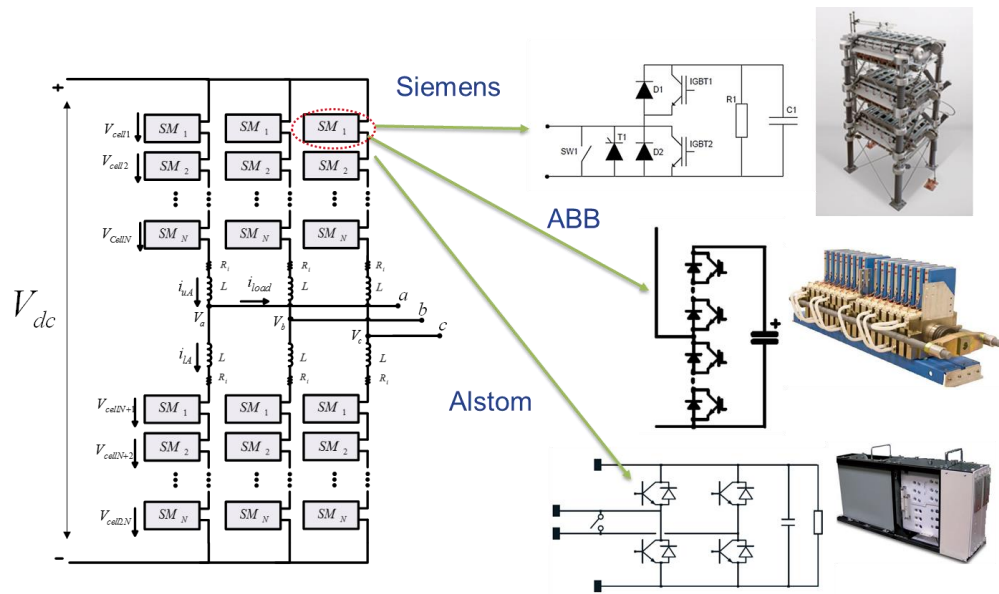


Figure 1- 10: VSC HVDC multilevel technology review [23] Alstom Grid, www.alstom.com/products-services/product-catalogue/electrical-grid-new/hvdc/hvdc-solutions/hvdc-maxsinetm/, 2011, [37] Siemens, www.siemens.com/energy/hvdcplus, 2011 and [38] ABB, www.abb.com/hvdc, 2013. Used under fair use, 2015.

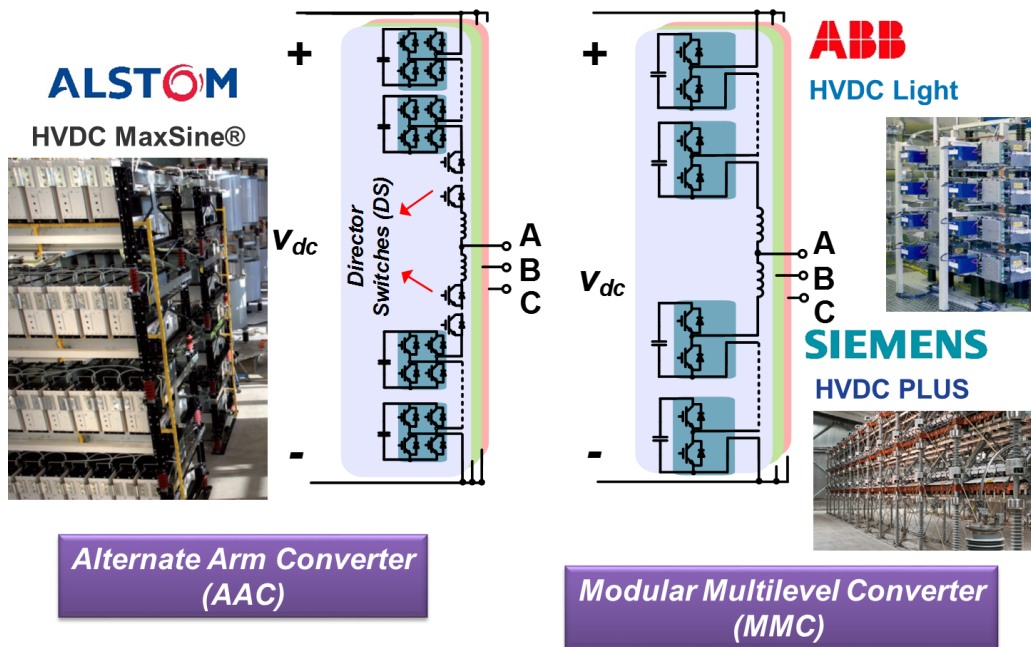


Figure 1- 11: Modular Multilevel Converter manufactured by Alstom Grid, Siemens and ABB, [23] Alstom Grid, www.alstom.com/products-services/product-catalogue/electrical-grid-new/hvdc/hvdc-solutions/hvdc-maxsinetm/, 2011, [37] Siemens, www.siemens.com/energy/hvdcplus, 2011 and [38] ABB, www.abb.com/hvdc, 2013. Used under fair use, 2015.

1.4 Research Objectives

Due to the continuous emergence of Modular Multilevel Converters, many questions about their modeling, control, advantages and disadvantages arise. Consequently, a significant effort has been devoted to developing the converter for medium voltage applications such as motor drives. Since the design of the MMC requires a good understanding of the operation principles of the converter, first the modeling approach should be chosen to provide an analysis of the converter's operation. Another issue to consider will be the design of the MMC controller for the MMC, which can be accomplished by modeling the MMC in DQ reference frame. Next, a detailed control approach to the MMC should be discussed, and the circulating current suppressing controller design and capacitor voltage balance should be considered as one of the important points of the MMC's operation. Some of the main drawbacks of the MMC will be addressed in this study. One of these drawbacks is with regard to the capacitor bank design of the MMC and maximizing the reliability of the converter. A reliability-oriented design of the capacitor bank is therefore considered to be important in the practical setup of the MMC. The design of the capacitor bank and arm inductor will influence the operation of the MMC and therefore explained herein. The switching frequency design of the MMC also needs to be addressed. In high and medium voltage applications, to prevent high semiconductor switching losses, the switching frequency tends to be set as low. However, the operation of the converter in low switching frequencies, means higher voltage ripple stress on the capacitor and IGBT in each cell. Therefore, an even trade-off between switching losses and capacitor voltage ripple should be achieved. This even trade-off can be obtained by using the reliability function of the converter as the objective

function. The reliability of the converter should be extracted by considering the reliability models of the individual components in the MMC. System-level reliability modeling for power electronics converters, especially high power converters such as the MMC, is not discussed in the literature since one of the advantages of the MMC is its high reliability as a result of its modular structure. The Markov model is one of the mathematical approaches that is used in many applications and is one of the great candidates to model the reliability of the MMC, as it models the fault transients of the converter. Therefore, in this thesis, the switching frequency design of the modular multilevel converters is presented using the Markov state-space reliability model of the converter as the objective function that needs to be maximized.

But the main issue regarding the MMC with half-bridge power modules is their lack of DC fault blocking capability, which is a result of their half-bridge structure. In an MMC with half-bridge power cells, there exists an uncontrolled current path during the DC short circuit fault and the only way to remove the fault is using DC or AC circuit breakers, which add more complexity and cost to the converter. One promising way to provide DC fault ride capability for the MMC is to use an MMC with full-bridge power cells or the newly conceived hybrid multilevel converters, among which is the recently commercialized Alternate Arm Converter. The operation of the AAC modeling and control are not completely addressed in the literature and there is wide research headroom available for the AAC. The existence of the series IGBT “director switches” in series with the arm inductor and stacked full-bridge in the AAC, means that it requires zero current switching of the devices, which in turn prevents the converter from huge voltage spikes as a result of the fast di/dt . Therefore, the ZCS operation of the director switches for the

AAC should be studied. The next step will be DC fault analysis of the modular multilevel converters with regard to their interest topologies: MMC with half-bridge, MMC with full-bridge power cells, and the AAC. The DC fault control of the MMC is not discussed in the literature either. So, the following are proposed in this thesis: DC fault control of the MMC with full-bridge and an AAC for use in limiting DC fault as well as in maintaining the capacitor voltage during the DC. This research targets the following goals:

- 1- Modeling of the modular multilevel converters (MMC and AAC).
- 2- Closed-loop control of the circulating current, capacitor voltage and energy balance and closed loop output load current loop as well as DC fault control for the modular multilevel converters (MMC and AAC).
- 3- High Reliability Capacitor Bank Design of the modular multilevel converters.
- 4- Reliability Oriented Switching Frequency Analysis of the modular multilevel converters.
- 5- Operation principles and Zero Current Switching of the director switches in the AAC.
- 6- DC- Fault ride-through capability of the modular multilevel converters (MMC and AAC).

1.5 Thesis Organization

To satisfy the above objectives, this thesis is organized as follows. Chapter 2 introduces the modular multilevel converters' modeling, and provides modeling of the complete switching, average, and DQ reference frame modeling of the MMC, and also

the switching and average modeling of the AAC. Chapter 3 explores the closed loop control of the modular multilevel converters. Particular attention is paid to the Circulating Current Suppressing Control (CCSC) and capacitor voltage balance in the MMC and the overlap time control for the AAC. Chapter 4 evaluates the novel consideration regarding to design of the Modular Multilevel Converters including MMC and AAC. The Zero Current Switching scheme for the director switches in the AAC is proposed in this chapter as well as reliabitliy oriented design of the modular multilevle converters. Chapter 5 presents a DC fault ride through capabiltiy of the modular multilevel converters. Conclusions will then be drawn in Chapter 6, followed by a discussion of the future work.

Chapter 2 Modular Multilevel Converters Modeling

2.1 Introduction

This chapter presents the modeling approach for illustrating the operation principles of Modular Multilevel Converters (MMC) including the MMC with half-bridge power cells and the Alternate-Arm Converter (AAC). Modular multilevel converters have emerged as new multilevel converters that can be used especially in High Voltage Direct Current (HVDC) and Medium Voltage Direct Current (MVDC) applications [25],[39-42]. Generally, the main advantages of the MMC with as compared to other types of multilevel converters are their high modularity and capability for high voltage scalability, which means that they can be connected directly to the grid without using any transformer [43]. The modular multilevel converter structure is shown in Figure 2-1. The MMC generally consists of upper and lower arm power cells, which can be half-bridge or full-bridge. The first model of the MMC was generated by replacing the single switches in a two-level converter with a series of power modules. As mentioned, these power modules can be half-bridge or full-bridge; however, due to the higher number of switches and switching power losses, MMC with half-bridge is more often developed. In order to eliminate inrush current during switching between modules, additional inductors should be added in series with the power modules in each arm

[44]. To have sinusoidal output voltage, the upper arm and lower modules' references should be justified with respect to the DC voltage in order to generate a proper wave-shaping circuit [29]. In the MMC with the half-bridge, the maximum voltage over each module is the DC-link voltage divided by the number of arm modules; however, the MMC with the full-bridge module can work in over-modulation since each module can generate negative voltage as well [45].

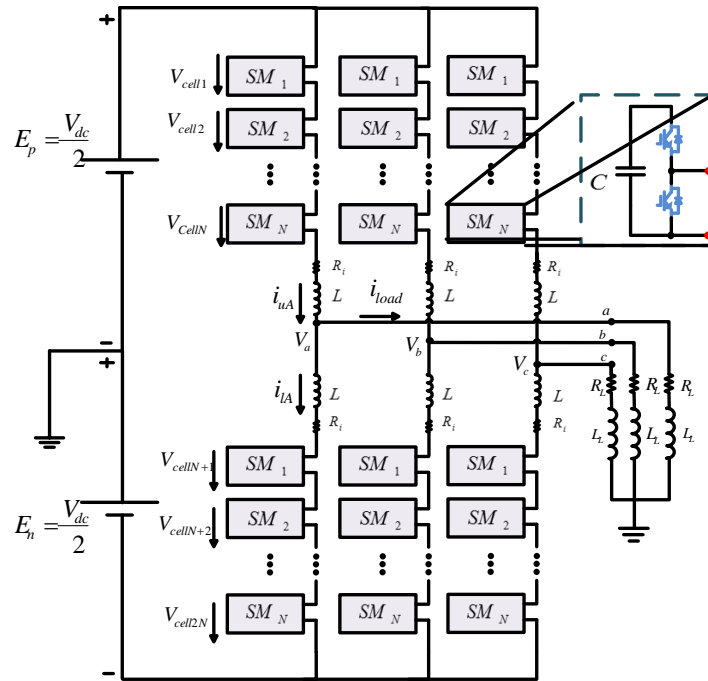


Figure 2- 1: Modular Multilevel Converter topology with each sub-module structure.

One of the disadvantages of the MMC is the existence of relatively high circulating current due to the difference in voltage of the arm inductors [46]-[47]. To limit the circulating current, the arm inductor size should be selected to be quite high or the circulating current suppressing controller should be employed [48]. Another issue regarding this topology is the number of capacitor banks required for each module in the MMC, which can lead to a huge space occupied by capacitors and cause reliability issues

[49]-[50].] Moreover, having a high number of modules makes the control system more complex [51]. Significant efforts have been dedicated to the modeling of the MMC and to a circuit behavior analysis of the converter. Different modeling approaches for the Modular Multilevel Converter (MMC) have been carried out in the literature. In [52], the state-space switching model of the MMC is developed and the complete derivation procedure of that is given. In reference [53], a continuous model of a three phase MMC, which is derived from ordinary differential equations, is developed and described. All the other existent models deal with the three-phase average model of the MMC, and the equations are extracted based on the average model [52-57].

In this chapter, a new modeling approach based on D-Q frame modeling is proposed for use as a model-based converter of the inner and outer loop control design. DQ modeling of the MMC can provide the relations of the duty cycles and arm quantities as well as the output voltage and current of the converter. Also, the proposed DQ model of the MMC is of great value in developing new control methods for the MMC. To obtain the DQ model, the following procedure should be taken. First of all, a three-phase average model of the converter should be derived from the switching model. Then by applying the Park transformation, the DQ model can be achieved. The second order harmonic circulating current is considered as the dominant component of the circulating current and higher order harmonics are considered to be negligible [47]. Therefore, the MMC system can be divided into three-frames of operation: DC, fundamental frequency, and twice the fundamental frequency frame. By assuming the superposition, each of the parameters can be modeled in these three-frames and finally the results can be added together. Indeed, using this model, DC current and circulating current equations can be

decoupled from the load current. By changing the modeling of MMC into three separate models, one will be able to derive the DQ model in each case.

2.2 *Modular Multilevel Converter Modeling (MMC)*

2.2.1 MMC Switching Model

The general state-space switching model is derived based on the simplest MMC configuration: a single-module MMC topology as shown in Figure 2-1 [52]. The state-space model is derived by selecting the inductor currents and capacitor voltages as states of the converter for control purposes. Therefore, five totally independent KVL equations can be written for the converter and i_{Uabc} (Upper Arm Current phase a, b and c), i_{Labc} (Lower Arm Current phase a, b and c) can be chosen as initial independent state variables. However, the DC current, line currents and circulating currents are the most convenient parameters to describe and control the operation of the converter, and the fundamental circuit characteristics of the MMC can be better reflected based on them. Hence, the initial state variables should be changed into another set of independent states in terms of the three latter current components. Figure 2-2 shows the switching model of the MMC.

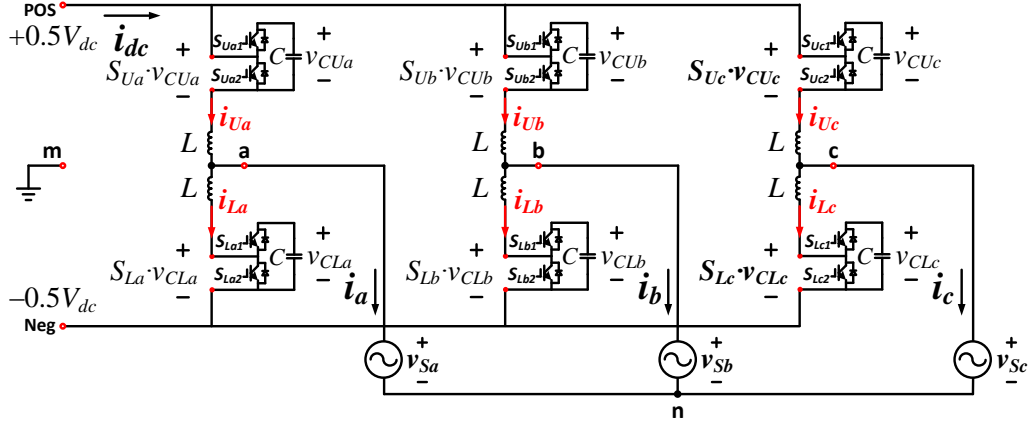


Figure 2- 2: Switching Model of the MMC.

The S_{Ux} and S_{Lx} are defined as the switching functions that can be '1' or '0', where x is a phase identifier, given by (2-1).

$$S_{Ux} = \begin{cases} 1 & \text{UpperArmSwitched} \\ 0 & \text{LowerArmSwitched} \end{cases} \quad (2-1)$$

By using an intermediate state variable transformation as in (2-2) and (2-3), the new state variables can be obtained as the sum of phase-leg currents, named "sum current," and the subtraction of the upper and lower arm current, which gives the line currents. These currents are very important intermediate state variables that will help derive DC current and line current equations.

$$i_{sumx} = i_{Ux} + i_{Lx} \quad (2-2)$$

$$i_x = i_{Ux} - i_{Lx} \quad (2-3)$$

under the assumption (2-4), the DC current equation can be derived using KCL as shown in (2-5),

$$i_{dc} = \sum_{x=a,b,c} i_{Ux} = \frac{1}{2} \sum_{x=a,b,c} (i_{sumx} + i_x) = \frac{1}{2} \sum_{x=a,b,c} i_{sumx} \quad (2-4)$$

$$i_a + i_b + i_c = 0 \quad (2-5)$$

The AC line current equations can be expressed as shown in (2-6), where v_{nm} is the common-mode voltage between the AC neutral and the DC mid-point is given by (2-7):

$$\frac{d}{dt} i_x = \frac{(S_{Lx}v_{Lx} - S_{Ux}v_{Ux}) - 2v_{nm} - 2v_{sx}}{L} \quad (2-6)$$

$$v_{nm} = \frac{1}{6} \sum_{x=a,b,c} (S_{Lx}v_{Lx} - S_{Ux}v_{Ux}) \quad (2-7)$$

Through the intrinsic operation of the MMC, there exists the circulating current which circulates between phase-legs without flowing into the DC bus or the AC lines. Their equation is derived by the KVL equation through the circulating current path as shown below.

$$\frac{d}{dt} i_{circ} = \frac{1}{6L} \left[\sum_{x=a,b,c} (S_{Ux}v_{Ux} + S_{Lx}v_{Lx}) - 3(S_{Ux}v_{Ux} + S_{Lx}v_{Lx}) \right] \quad (2-8)$$

Lastly, the full-rank current equations for the state-space model of the MMC are given in (2-9).

$$\begin{cases} \frac{d}{dt} i_{dc} = \frac{1}{2L} \left[3V_{dc} - \sum_{x=a,b,c} (S_{Ux}v_{Ux} + S_{Lx}v_{Lx}) \right] \\ \frac{d}{dt} i_a = \frac{(S_{La}v_{La} - S_{Ua}v_{Ua}) - 2v_{nm} - 2v_{sa}}{L} \\ \frac{d}{dt} i_b = \frac{(S_{Lb}v_{Lb} - S_{Ub}v_{Ub}) - 2v_{nm} - 2v_{sb}}{L} \\ \frac{d}{dt} i_{cira} = \frac{1}{6L} \left[\sum_{x=a,b,c} (S_{Ux}v_{Ux} + S_{Lx}v_{Lx}) - 3(S_{Ua}v_{Ua} + S_{La}v_{La}) \right] \\ \frac{d}{dt} i_{cib} = \frac{1}{6L} \left[\sum_{x=a,b,c} (S_{Ux}v_{Ux} + S_{Lx}v_{Lx}) - 3(S_{Ub}v_{Ub} + S_{Lb}v_{Lb}) \right] \end{cases} \quad (2-9)$$

The expression for the original inductor currents with new variables can be derived using the inverse transition matrix as shown in [52], given by (2-10).

$$\begin{cases} i_{Ux} = \frac{i_{dc}}{3} + \frac{i_x}{2} + i_{cirx} \\ i_{Lx} = \frac{i_{dc}}{3} - \frac{i_x}{2} + i_{cirx} \end{cases} \quad (2-10)$$

The module capacitor voltage as the state variables can be finally be derived by (2-11) and (2-12).

$$\frac{d}{dt} v_{Ux} = \frac{1}{C} S_{Ux} i_{Ux} \quad (2-11)$$

$$\frac{d}{dt} v_{Lx} = \frac{1}{C} S_{Lx} i_{Lx} \quad (2-12)$$

For the case with more than one module per arm (multilevel case), the complete state-space model can be extended as shown below.

$$\left\{ \begin{array}{l}
\frac{d}{dt} i_{dc} = \frac{1}{2L} \left[3V_{dc} - \sum_{x=a,b,c} \sum_{i=1}^n (S_{Uxi} v_{Uxi} + S_{Lxi} v_{Lxi}) \right] \\
\frac{d}{dt} i_a = \frac{\sum_{i=1}^n (S_{Lai} v_{Lai} - S_{Uai} v_{Uai}) - 2v_{nm} - 2v_{sa}}{L} \\
\frac{d}{dt} i_b = \frac{\sum_{i=1}^n (S_{Lbi} v_{Lbi} - S_{Ubi} v_{Ubi}) - 2v_{nm} - 2v_{sb}}{L} \\
\frac{d}{dt} i_{cira} = \frac{1}{6L} \left[\sum_{x=a,b,c} \sum_{i=1}^n (S_{Ux} v_{Ux} + S_{Lx} v_{Lx}) - 3 \sum_{i=1}^n (S_{Ua} v_{Ua} + S_{La} v_{La}) \right] \\
\frac{d}{dt} i_{cirb} = \frac{1}{6L} \left[\sum_{x=a,b,c} \sum_{i=1}^n (S_{Ux} v_{Ux} + S_{Lx} v_{Lx}) - 3 \sum_{i=1}^n (S_{Ub} v_{Ub} + S_{Lb} v_{Lb}) \right] \\
\frac{d}{dt} v_{Uxi} = \frac{1}{C} S_{Uxi} i_{Ux} \\
\frac{d}{dt} v_{Lxi} = \frac{1}{C} S_{Lxi} i_{Lx}
\end{array} \right. \quad (2-13)$$

where $i=1, \dots, n$, is the number of modules and v_{nm} is defined from (2-7).

2.2.2 Steady-State Harmonic Analysis of the MMC

As is shown in equation (2-10), in MMC, the arm current is made up of mainly three components: DC, fundamental, and 2nd Harmonic, which is the dominant harmonic component [46]. The upper and lower arm current in phase A can be written:

$$\begin{cases} i_{ua} = \frac{i_{dc}}{3} + \frac{I_{a1} \cos(\omega t + \phi)}{2} + I_{a2} \cos(2\omega t + \theta) \\ i_{la} = \frac{i_{dc}}{3} - \frac{I_{a1} \cos(\omega t + \phi)}{2} + I_{a2} \cos(2\omega t + \theta) \end{cases} \quad (2-14)$$

Where i_{dc} is the DC current, I_{a1}, ϕ are the amplitude and phase of the fundamental component and I_{a2}, θ are the amplitude and phase of the 2nd harmonic component. The

average switching functions of the upper and lower arm of the MMC in general form are given by:

$$\begin{cases} d_{ua} = \frac{1}{2} - D_u \cos(\omega t + \psi) \\ d_{la} = \frac{1}{2} + D_l \cos(\omega t + \psi) \end{cases} \quad (2-15)$$

The average capacitor current for the upper arm will be given by:

$$i_{cua} = d_{ua} i_{ua} \quad (2-16)$$

By replacing (2-14) and (2-15) in (2-16), the average capacitor current is obtained as:

$$\begin{aligned} i_{cua} = & \frac{i_{dc}}{6} - \frac{D_u I_{a1} \cos(\psi - \phi)}{4} - \frac{D_u i_{dc} \cos(\omega t + \psi)}{3} + \frac{I_{a1} \cos(\omega t + \phi)}{4} - \frac{D_u I_{a2} \cos(\omega t + \theta - \psi)}{2} - \frac{D_u I_{a1} \cos(2\omega t + \psi + \phi)}{4} \\ & + \frac{I_{a2} \cos(2\omega t + \theta)}{2} - \frac{D_u I_{a2} \cos(3\omega t + \psi + \theta)}{2} \end{aligned} \quad (2-17)$$

From the capacitor current, the capacitor voltage can be obtained by using the following relation:

$$v_{cua} = \frac{1}{C} \int i_{cua} dt \quad (2-18)$$

By replacing (2-17) in (2-18) and taking the integral we have:

$$\begin{aligned} v_{cua} = & V_{dc} + \frac{1}{C} \left(\frac{i_{dc}}{6} - \frac{D_u I_{a1} \cos(\psi - \phi)}{4} \right) t - \frac{D_u i_{dc} \sin(\omega t + \psi)}{3\omega C} + \frac{I_{a1} \sin(\omega t + \phi)}{4\omega C} - \frac{D_u I_{a2} \sin(\omega t + \theta - \psi)}{2\omega C} \\ & - \frac{D_u I_{a1} \sin(2\omega t + \psi + \phi)}{8\omega C} + \frac{I_{a2} \sin(2\omega t + \theta)}{4\omega C} - \frac{D_u I_{a2} \sin(3\omega t + \psi + \theta)}{6\omega C} \end{aligned} \quad (2-19)$$

Where, V_{dc} is the DC-link voltage. From the capacitor voltage, the module voltage can be obtained:

$$v_{ua} = d_{ua} v_{cua} \quad (2-20)$$

By replacing (2-19) into (2-20):

$$\begin{aligned}
v_{ua} = & \frac{V_{dc}}{2} + \frac{D_u I_{a1} \sin(\psi - \phi)}{8\omega C} - \frac{D_u^2 I_{a2} \sin(2\psi - \theta)}{4\omega C} + \frac{v_{cudc} t}{2} - D_u v_{cudc} t \cos(\omega t + \psi) - \frac{D_u i_{dc} \sin(\omega t + \psi)}{6\omega C} \\
& + \frac{I_{a1} \sin(\omega t + \phi)}{8\omega C} - \frac{D_u I_{a2} \sin(\omega t + \theta - \psi)}{4\omega C} - D_u V_{dc} \cos(\omega t + \psi) + \frac{D_u^2 I_{a1} \sin(\omega t + \phi)}{16\omega C} - \frac{D_u I_{a2} \sin(\omega t + \theta - \psi)}{8\omega C} \\
& - \frac{D_u I_{a1} \sin(2\omega t + \psi + \phi)}{16\omega C} + \frac{I_{a2} \sin(2\omega t + \theta)}{8\omega C} + \frac{D_u^2 i_{dc} \sin(2\omega t + 2\psi)}{6\omega C} - \frac{D_u I_{a1} \sin(2\omega t + \psi + \phi)}{8\omega C} + \frac{D_u^2 I_{a2} \sin(2\omega t + \theta)}{4\omega C} \\
& + \frac{D_u^2 I_{a2} \sin(2\omega t + \theta)}{12\omega C} + \text{higher order terms...}
\end{aligned} \tag{2-21}$$

And similarly for the lower arm we get:

$$\begin{aligned}
v_{ia} = & \frac{V_{dc}}{2} + \frac{D_l I_{a1} \sin(\psi - \phi)}{8\omega C} - \frac{D_l^2 I_{a2} \sin(2\psi - \theta)}{4\omega C} + \frac{v_{cldc} t}{2} + D_l v_{cldc} t \cos(\omega t + \psi) + \frac{D_l i_{dc} \sin(\omega t + \psi)}{6\omega C} - \frac{I_{a1} \sin(\omega t + \phi)}{8\omega C} \\
& + \frac{D_l I_{a2} \sin(\omega t + \theta - \psi)}{4\omega C} + D_l V_{dc} \cos(\omega t + \psi) - \frac{D_l^2 I_{a1} \sin(\omega t + \phi)}{16\omega C} + \frac{D_l I_{a2} \sin(\omega t + \theta - \psi)}{8\omega C} - \frac{D_l I_{a1} \sin(2\omega t + \psi + \phi)}{16\omega C} \\
& + \frac{I_{a2} \sin(2\omega t + \theta)}{8\omega C} + \frac{D_l^2 i_{dc} \sin(2\omega t + 2\psi)}{6\omega C} - \frac{D_l I_{a1} \sin(2\omega t + \psi + \phi)}{8\omega C} + \frac{D_l^2 I_{a2} \sin(2\omega t + \theta)}{4\omega C} + \frac{D_l^2 I_{a2} \sin(2\omega t + \theta)}{12\omega C} \\
& + \text{higher order terms...}
\end{aligned} \tag{2-22}$$

At the steady state, we have $D_u = D_l = D$ and $v_{cudc} = v_{cldc} = 0$.

2.2.3 Average Model of the MMC

The MMC switching model with only one cell in each arm is shown in Figure 2-3

(a).

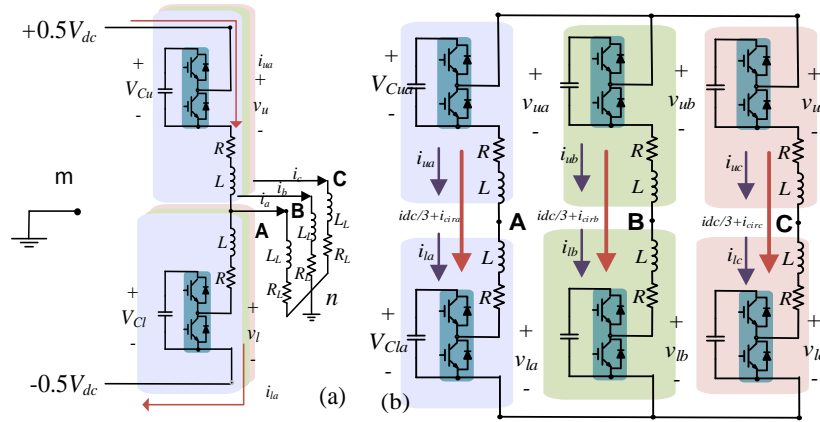


Figure 2- 3 (a) Switching model of MMC with one power cell in each arm, (b) Circulating current switching model in the MMC

From the MMC switching model, by applying KVL in the upper and lower arm, we get the following switching model equations:

$$\begin{cases} (Upper): -\frac{V_{dc}}{2}\vec{1} + \overrightarrow{(S_u v_{cu})}_{abc} + L\frac{d\overrightarrow{i_{uabc}}}{dt} + R\overrightarrow{i_{uabc}} + L_L\frac{d\overrightarrow{i_{abc}}}{dt} \\ + R_L\overrightarrow{i_{abc}} + v_{nm}\vec{1} = 0 \\ (Lower): \frac{V_{dc}}{2}\vec{1} - \overrightarrow{(S_l v_{cl})}_{abc} - L\frac{d\overrightarrow{i_{labc}}}{dt} - R\overrightarrow{i_{labc}} + L_L\frac{d\overrightarrow{i_{abc}}}{dt} \\ + R_L\overrightarrow{i_{abc}} + v_{nm}\vec{1} = 0 \end{cases} \quad (2-23)$$

Where $S_u v_{cu} = v_u$, $S_l v_{cl} = v_l$, S_u and S_l are the switching functions of the upper and lower arm, v_{cu} and v_{cl} are the capacitor voltages of the upper and lower arm capacitors, L and R are the inductance and the resistance of the modules, R_L and L_L are the load resistance and inductor, $\overrightarrow{i_{abc}}$ are the line currents in the phases a, b and c, and v_{nm} is the voltage from the load neutral to the DC side neutral point $v_{nm} = \frac{1}{6} \sum_{x=a,b,c} (S_{lx} v_{clx} - S_{ux} v_{cux})$, and $\vec{1}$ is the column vector given by $\vec{1} = (1 \ 1 \ 1)^T$. Adding the above two equations we get:

$$\begin{cases} \overrightarrow{(S_u v_{cu})}_{abc} - \overrightarrow{(S_l v_{cl})}_{abc} + L\frac{d(\overrightarrow{i_{uabc}} - \overrightarrow{i_{labc}})}{dt} + R(\overrightarrow{i_{uabc}} - \overrightarrow{i_{labc}}) \\ + 2R_L\overrightarrow{i_{abc}} + 2L_L\frac{d\overrightarrow{i_{abc}}}{dt} + 2v_{nm}\vec{1} = 0 \end{cases} \quad (2-24)$$

By replacing $\overrightarrow{i_{uabc}} - \overrightarrow{i_{labc}} = \overrightarrow{i_{abc}}$, equation (2-24) will be changed to:

$$\begin{cases} \overrightarrow{(S_u v_{cu})}_{abc} - \overrightarrow{(S_l v_{cl})}_{abc} + L\frac{d\overrightarrow{i_{abc}}}{dt} + R\overrightarrow{i_{abc}} \\ + 2R_L\overrightarrow{i_{abc}} + 2L_L\frac{d\overrightarrow{i_{abc}}}{dt} + 2v_{nm}\vec{1} = 0 \end{cases} \quad (2-25)$$

The equations for the module capacitors are given by:

$$\begin{cases} \frac{d\overrightarrow{v_{cuabc}}}{dt} = \frac{1}{C} \overrightarrow{(S_u i_{cu})_{abc}} \\ \frac{d\overrightarrow{v_{clabc}}}{dt} = \frac{1}{C} \overrightarrow{(S_l i_{cl})_{abc}} \end{cases} \quad (2-26)$$

Where $\overrightarrow{v_{cuabc}}$, $\overrightarrow{v_{clabc}}$ are the capacitor voltages of the upper and lower arm in phases a, b and c, C is the capacitance of the module, i_u and i_l are the upper and lower arm currents. As is mentioned for the MMC, because of the existence of the arm inductors, there exists a circulating current which doesn't come into the DC side but just circulates through each phase. To account for the circulating current, as can be seen in Figure 2-3 (b), we have the following equations:

$$\begin{aligned} S_{ub}v_{cub} + S_{lb}v_{clb} + L \frac{d(i_{ub} + i_{lb})}{dt} + R(i_{ub} + i_{lb}) \\ - (S_{la}v_{cla} + S_{ua}v_{cua}) - L \frac{d(i_{la} + i_{ua})}{dt} - R(i_{la} + i_{ua}) = 0 \end{aligned} \quad (2-27)$$

Similarly, for the other two phases we get:

$$\begin{cases} S_{uc}v_{cuc} + S_{lc}v_{clc} + L \frac{d(i_{uc} + i_{lc})}{dt} + R(i_{uc} + i_{lc}) \\ - (S_{lb}v_{clb} + S_{ub}v_{cub}) - L \frac{d(i_{lb} + i_{ub})}{dt} - R(i_{lb} + i_{ub}) = 0 \\ S_{ua}v_{cua} + S_{la}v_{cla} + L \frac{d(i_{ua} + i_{la})}{dt} + R(i_{uc} + i_{lc}) \\ - (S_{lc}v_{clc} + S_{ua}v_{cuc}) - L \frac{d(i_{lc} + i_{uc})}{dt} - R(i_{lc} + i_{uc}) = 0 \end{cases} \quad (2-28)$$

Since, $i_{ua} + i_{la} = \frac{2}{3}i_{dc} + 2i_{cira}$ substituting in (2-28) we get:

$$\begin{cases}
S_{ub}v_{cub} + S_{lb}v_{clb} + 2\frac{Ldi_{cirb}}{dt} + 2Ri_{cirb} - (S_{la}v_{cla} + S_{ua}v_{cua}) \\
- 2\frac{Ldi_{cira}}{dt} - 2Ri_{cira} = 0 \\
S_{uc}v_{cuc} + S_{lc}v_{clc} + 2\frac{Ldi_{circ}}{dt} + 2Ri_{circ} - (S_{lb}v_{clb} + S_{ub}v_{cub}) \\
- 2\frac{Ldi_{cirb}}{dt} - 2Ri_{cirb} = 0 \\
S_{ua}v_{cua} + S_{la}v_{cla} + 2\frac{Ldi_{cira}}{dt} + 2Ri_{cira} - (S_{lc}v_{clc} + S_{uc}v_{cuc}) \\
- 2\frac{Ldi_{circ}}{dt} - 2Ri_{circ} = 0
\end{cases} \quad (2-29)$$

Where i_{cira} , i_{cirb} and i_{circ} are the circulating currents in the arms a, b and c, S_{ua} and S_{la} are the switching functions of the upper and lower arm for phase a, S_{ub} and S_{lb} for phase b, S_{uc} and S_{lc} for phase c.

From the above switching model, we can now obtain the average model in abc coordinates by applying the average operator. If third and higher order harmonics are neglected in the analysis, we have $\overline{v_{nm}} = \frac{1}{6} \sum_{x=a,b,c} (\overline{v_{lx}} - \overline{v_{ux}}) = 0$, where v_{lx} and v_{ux} represent the module voltages for the lower and upper arm. Applying the average operator for the fundamental frequency switching model, we have:

$$\begin{aligned}
& \overline{(d_u v_{cu})_{abc}} - \overline{(d_l v_{cl})_{abc}} + L \frac{d(\overline{i_{abc}})}{dt} + R(\overline{i_{abc}}) \\
& + 2R_L \overline{i_{abc}} + 2L_L \frac{d\overline{i_{abc}}}{dt} = 0
\end{aligned} \quad (2-30)$$

And the module capacitor voltage in the average model is obtained as:

$$\begin{cases}
\frac{d\overline{v_{cuabc}}}{dt} = \frac{1}{C} \overline{(d_u i_{cu})_{abc}} \\
\frac{d\overline{v_{clabc}}}{dt} = \frac{1}{C} \overline{(d_l i_{cl})_{abc}}
\end{cases} \quad (2-31)$$

From equation (2-16), the average model for the circulating current can be written

as:

$$\begin{cases} d_{ub}\overline{v_{cub}} + S_{lb}\overline{v_{clb}} + 2L\frac{d(\overline{i_{cirb}})}{dt} + 2R\overline{i_{cirb}} - (d_{la}\overline{v_{cla}} + d_{ua}\overline{v_{cua}}) \\ -2L\frac{d(\overline{i_{cira}})}{dt} - 2R\overline{i_{cira}} = 0 \\ d_{uc}\overline{v_{cuc}} + d_{lc}\overline{v_{clc}} + 2L\frac{d(\overline{i_{circ}})}{dt} + 2R\overline{i_{circ}} - (d_{lb}\overline{v_{clb}} + d_{ub}\overline{v_{cub}}) \\ -2L\frac{d(\overline{i_{cirb}})}{dt} - 2R\overline{i_{cirb}} = 0 \\ d_{ua}\overline{v_{cua}} + d_{la}\overline{v_{cla}} + 2L\frac{d(\overline{i_{cira}})}{dt} + 2R\overline{i_{cira}} - (d_{lc}\overline{v_{clc}} + d_{uc}\overline{v_{cuc}}) \\ -2L\frac{d(\overline{i_{circ}})}{dt} - 2R\overline{i_{circ}} = 0 \end{cases} \quad (2-32)$$

By subtracting upper and lower arm KVL equation from (2-23), we get:

$$-V_{dc} + v_{ua} + v_{la} + L\frac{d(i_{ua} + i_{la})}{dt} + R(i_{ua} + i_{la}) = 0 \quad (2-33)$$

By replacing the sum of the upper and lower arm current by the corresponding circulating current and similarly for phases b and c we get:

$$\begin{cases} -V_{dc} + v_{ua} + v_{la} + 2L\frac{di_{cira}}{dt} + 2L\frac{di_{cira}}{3dt} + 2Ri_{cira} + \frac{2Ri_{dc}}{3} = 0 \\ -V_{dc} + v_{ub} + v_{lb} + 2L\frac{di_{cirb}}{dt} + 2L\frac{di_{dc}}{3dt} + 2Ri_{cirb} + \frac{2Ri_{dc}}{3} = 0 \\ -V_{dc} + v_{uc} + v_{lc} + 2L\frac{di_{circ}}{dt} + 2L\frac{di_{dc}}{3dt} + 2Ri_{circ} + \frac{2Ri_{dc}}{3} = 0 \end{cases} \quad (2-34)$$

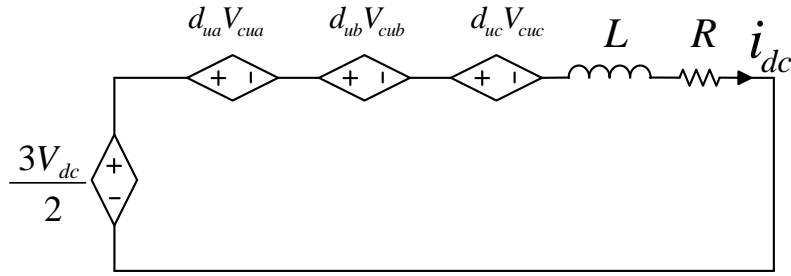
Adding the above three phase equations we get:

$$\begin{aligned} & -3V_{dc} + (v_{ua} + v_{ub} + v_{uc})_{dc} + (v_{la} + v_{lb} + v_{lc})_{dc} \\ & + 2L\frac{di_{dc}}{dt} + 2Ri_{dc} = 0 \end{aligned} \quad (2-35)$$

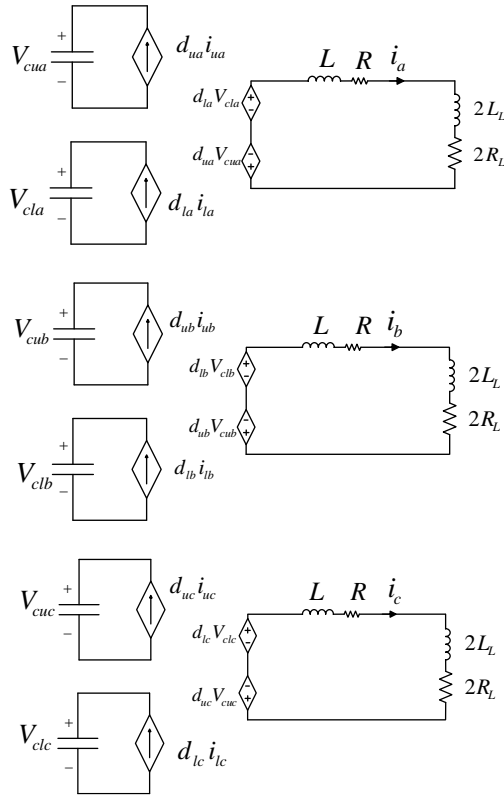
Since the fundamental and harmonic components of the three phases add up to zero, only the DC components are left. As the DC components in all three phases are equal, the DC side equation of the MMC in abc coordinates can be obtained as:

$$-\frac{3}{2}V_{dc} + (v_{ua} + v_{ub} + v_{uc})_{dc} + L \frac{di_{dc}}{dt} + Ri_{dc} = 0 \quad (2-36)$$

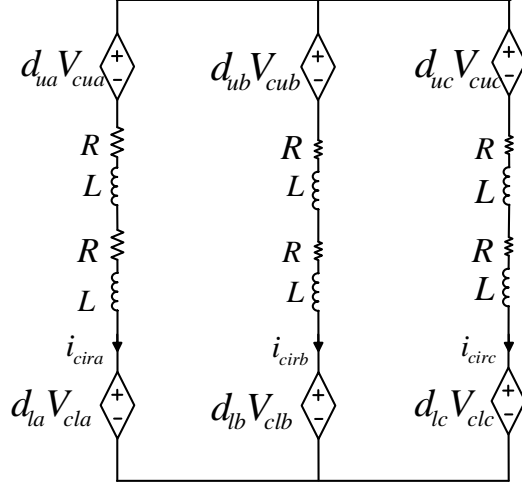
Where V_{dc} is the DC voltage and v_{ua} , v_{ub} and v_{uc} represent the module voltages in the phases a, b and c. From (2-30), (2-31) for phase current model, (2-32) for the circulating current model and (2-10) for the DC current model in three-phase abc coordinates, the average model of the MMC can be derived as it is shown in Figure 2-4.



(a) DC MMC Model in abc



(b) Fundamental Freq. Model in abc



(c) Circulating Current Model in abc

Figure 2- 4 abc Average Model for the MMC.

2.2.4 D-Q Model of the MMC

By obtaining the DC current, phase current, and circulating current in the three-phase abc model, the DQ model from them can be extracted.

2.2.4.1 D-Q Model of Phase Current in the MMC

From the average model of MMC (2-30), the fundamental frequency model frame, we have:

$$\overrightarrow{v_{uabc}} - \overrightarrow{v_{labc}} + L \frac{d(\overline{i_{abc}})}{dt} + R(\overline{i_{abc}}) + 2L_L \frac{d\overline{i_{abc}}}{dt} + 2R_L \overline{i_{abc}} = 0 \quad (2-37)$$

For the phase a, by substituting the fundamental frequency components of v_{ua} and v_{la} from (2-21) and (2-22) in (2-37), we get:

$$\begin{aligned} & -2Dv_{cudc}t \cos(\omega t + \psi) - \frac{Di_{dc} \sin(\omega t + \psi)}{3\omega C} + \frac{I_1 \sin(\omega t + \phi)}{4\omega C} \\ & - \frac{DI_2 \sin(\omega t + \theta - \psi)}{2\omega C} - 2DV_{dc} \cos(\omega t + \psi) + \frac{D^2 I_1 \sin(\omega t + \phi)}{8\omega C} \\ & - \frac{DI_2 \sin(\omega t + \theta - \psi)}{4\omega C} + \frac{Ldi_a}{dt} + Ri_a + 2R_L i_a + 2L_L \frac{di_a}{dt} = 0 \end{aligned} \quad (2-38)$$

Same equation for the phase b and c by shifting the phase ± 120 degree can be achieved. By using the fact that:

$$\vec{d}_{dq} = \sqrt{\frac{3}{2}} D \begin{pmatrix} \cos \psi \\ \sin \psi \end{pmatrix} \quad (2-39)$$

And also for the phase current in DQ:

$$\vec{i}_{dq} = \sqrt{\frac{3}{2}} I_1 \begin{pmatrix} \cos \phi \\ \sin \phi \end{pmatrix} \quad (2-40)$$

And the circulating current in the DQ axis, we have:

$$\vec{i}_{circdq} = \sqrt{\frac{3}{2}} I_2 \begin{pmatrix} \cos \theta \\ \sin \theta \end{pmatrix} \quad (2-41)$$

By applying DQ transformation to (2-38) abc equations using the park transformation:

$$T = \sqrt{\frac{2}{3}} \begin{pmatrix} \cos \omega t & \cos(\omega t - \frac{2\pi}{3}) & \cos(\omega t + \frac{2\pi}{3}) \\ -\sin \omega t & -\sin(\omega t - \frac{2\pi}{3}) & -\sin(\omega t + \frac{2\pi}{3}) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{pmatrix} \quad (2-42)$$

The following equation is obtained:

$$\begin{aligned} & -2V_{dc} \vec{d}_{dq} + \frac{1}{3C} t (d_d i_d + d_q i_q - i_{dc}) \vec{d}_{dq} + \frac{i_{dc}}{3C} \begin{pmatrix} 0 & -1 \\ 1 & 0 \end{pmatrix} \vec{d}_{dq} - \frac{1}{4C} \begin{pmatrix} 0 & -1 \\ 1 & 0 \end{pmatrix} \vec{i}_{dq} - \frac{1}{12C} (d_d^2 + d_q^2) \begin{pmatrix} 0 & -1 \\ 1 & 0 \end{pmatrix} \vec{i}_{dq} \\ & -\sqrt{\frac{3}{2}} \frac{1}{2\omega C} \begin{pmatrix} -d_q & d_d \\ -d_d & -d_q \end{pmatrix} \vec{i}_{circdq} + L \frac{d\vec{i}_{dq}}{dt} + R \vec{i}_{dq} + L \begin{pmatrix} 0 & -\omega \\ \omega & 0 \end{pmatrix} \vec{i}_{dq} + 2L_L \begin{pmatrix} 0 & -\omega \\ \omega & 0 \end{pmatrix} \vec{i}_{dq} + 2R_L \vec{i}_{dq} + 2L_L \frac{d\vec{i}_{dq}}{dt} = 0 \end{aligned} \quad (2-43)$$

Where d_{dq} represents the switching function, i_{dq} represents the line current, i_{circdq} represents the circulating current in DQ frame, ω is the angular frequency, and t represents the time.

2.2.4.2 DQ Model of DC and Circulating Current in the MMC

From the average model of circulating current in abc coordinates (2-32) we get:

$$\begin{aligned}
 (v_{ub} + v_{lb}) + 2 \frac{L \overline{di_{cirb}}}{dt} + 2R \overline{i_{cirb}} - (v_{ua} + v_{la}) - 2L \frac{d \overline{i_{cira}}}{3dt} - 2R \overline{i_{cira}} &= 0 \\
 (v_{uc} + v_{lc}) + 2 \frac{L \overline{di_{circ}}}{dt} + 2R \overline{i_{circ}} - (v_{ub} + v_{lb}) - 2L \frac{d \overline{i_{cirb}}}{3dt} - 2R \overline{i_{cirb}} &= 0 \\
 (v_{ua} + v_{la}) + 2 \frac{L \overline{di_{cira}}}{dt} + 2R \overline{i_{cira}} - (v_{uc} + v_{lc}) - 2L \frac{d \overline{i_{circ}}}{3dt} - 2R \overline{i_{circ}} &= 0
 \end{aligned} \tag{2-44}$$

Substituting the double line frequency values of $v_{ua}, v_{ub}, v_{uc}, v_{la}, v_{lb}, v_{lc}$ from (2-19)

and (2-21) in (2-44), the DQ model of the circulating current can be achieved by:

$$\begin{aligned}
 -3 \frac{DI_1 \sin(2\omega t + \psi + \phi + \frac{2\pi}{3})}{8\omega C} + (1 + 2D^2) \frac{I_2 \sin(2\omega t + \theta + \frac{2\pi}{3})}{4\omega C} + \frac{D^2 i_{dc} \sin(2\omega t + 2\psi + \frac{2\pi}{3})}{3\omega C} \\
 + \frac{D^2 I_2 \sin(2\omega t + \theta + \frac{2\pi}{3})}{6\omega C} + \frac{2L \overline{di_{cirb}}}{dt} + 2R \overline{i_{cirb}} + 3 \frac{DI_1 \sin(2\omega t + \psi + \phi)}{8\omega C} - (1 + 2D^2) \frac{I_2 \sin(2\omega t + \theta)}{4\omega C} \\
 - \frac{D^2 i_{dc} \sin(2\omega t + 2\psi)}{3\omega C} - \frac{D^2 I_2 \sin(2\omega t + \theta)}{6\omega C} - \frac{2L \overline{di_{cira}}}{dt} - 2R \overline{i_{cira}} = 0
 \end{aligned} \tag{2-45}$$

Similarly, for the other two phases, the same equation can be achieved by phase shifting of (2-45) ± 120 degree. Applying the park transformation for the negative sequence 2nd harmonic components as it is given by:

$$T = \sqrt{\frac{2}{3}} \begin{pmatrix} \cos 2\omega t & \cos(2\omega t + \frac{2\pi}{3}) & \cos(2\omega t - \frac{2\pi}{3}) \\ -\sin 2\omega t & -\sin(2\omega t + \frac{2\pi}{3}) & -\sin(2\omega t - \frac{2\pi}{3}) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{pmatrix} \tag{2-46}$$

And using the fact that:

$$\overrightarrow{i_{cirdq}} = \begin{pmatrix} -\frac{1}{2} i_{cird} - \frac{\sqrt{3}}{2} i_{cirq} \\ -\frac{1}{2} i_{cird} + \frac{\sqrt{3}}{2} i_{cirq} \end{pmatrix} \tag{2-47}$$

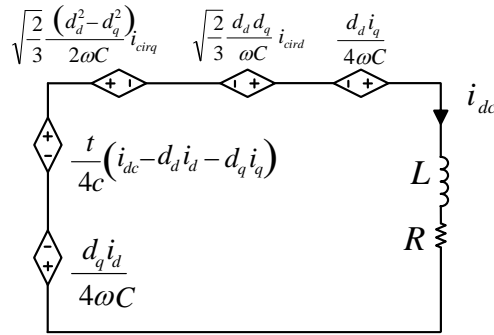
Where $\overrightarrow{i_{cirdq}} = T_2 \overrightarrow{i_{cirabc}}$ and $\overrightarrow{i_{cirdq}} = T_2 \overrightarrow{i_{cirbca}}$, we get:

$$\begin{aligned} \frac{Ldi_{circdq}}{dt} + Ri_{circdq} - \frac{1}{8C} \begin{bmatrix} 0 & -\frac{1}{\omega} \\ \frac{1}{\omega} & 0 \end{bmatrix} i_{circdq} + 2L \begin{bmatrix} 0 & -\omega \\ \omega & 0 \end{bmatrix} i_{circdq} - 2 \frac{(d_d^2 + d_q^2)}{9C} \begin{bmatrix} 0 & -\frac{1}{\omega} \\ \frac{1}{\omega} & 0 \end{bmatrix} i_{circdq} \\ + \frac{\sqrt{6}}{16\omega C} \begin{bmatrix} -d_q & d_d \\ -d_d & -d_q \end{bmatrix} i_{dq} + \frac{i_{dc}}{3\sqrt{6}\omega C} \begin{bmatrix} 0 & 2d_d \\ -d_d & d_q \end{bmatrix} d_{dq} = 0 \end{aligned} \quad (2-48)$$

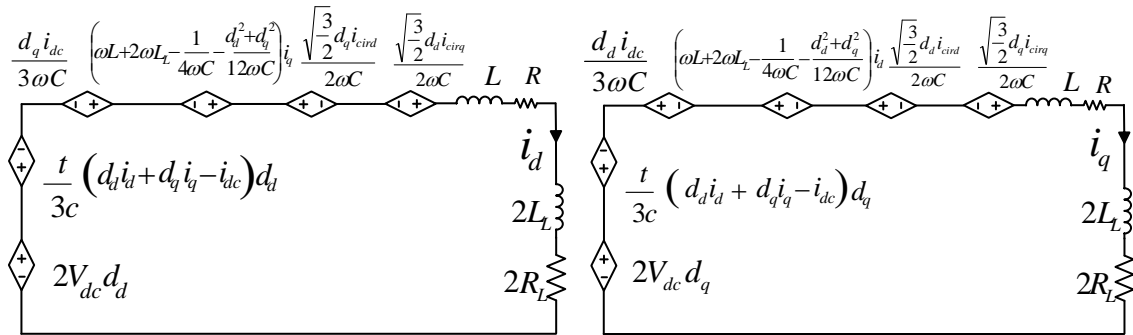
Plus, the DC side equation can also be expressed in d-q coordinates as:

$$\frac{Ldi_{dc}}{dt} + Ri_{dc} - \frac{\sqrt{2}d_d d_q i_{circd}}{\omega C} + \frac{\sqrt{2}(d_d^2 - d_q^2) i_{circq}}{2\omega C} + \frac{d_q i_d}{4\omega C} - \frac{d_d i_q}{4\omega C} + \frac{t}{4C} (i_{dc} - d_d i_d - d_q i_q) = 0 \quad (2-49)$$

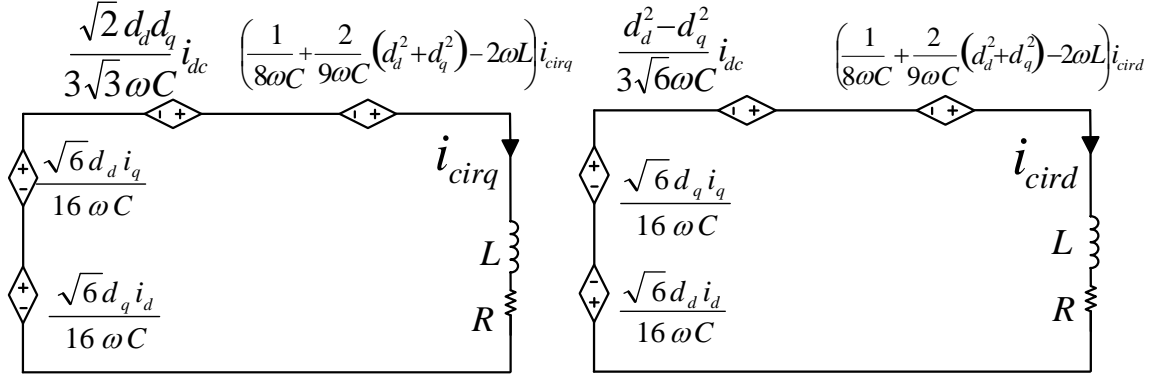
From (2-43), (2-48) and (2-49) the DQ model of the MMC for the phase current, DC current, and circulating current is obtained. The DQ model of the MMC from these equation can be drawn as shown in Figure 2-5.



(a) DC Model in D-Q



(b) Fundamental Freq. Model in D-Q



(c) Circulating Current Model in D-Q

Figure 2- 5 D-Q Frame Model for the MMC.

2.2.4.3 Capacitor Voltage in D-Q Coordinates

To obtain the capacitor voltage in the DQ model, the fundamental frequency component of the capacitor voltage in the average model from (2-19) can be written as:

$$\begin{cases}
 v_{cua1} = -\frac{Di_{dc} \sin(\omega t + \psi)}{3\omega C} + \frac{I_1 \sin(\omega t + \phi)}{4\omega C} - \frac{DI_2 \sin(\omega t + \theta - \psi)}{2\omega C} \\
 v_{cub1} = -\frac{Di_{dc} \sin(\omega t + \psi - \frac{2\pi}{3})}{3\omega C} + \frac{I_1 \sin(\omega t + \phi - \frac{2\pi}{3})}{4\omega C} - \frac{DI_2 \sin(\omega t + \theta - \psi - \frac{2\pi}{3})}{2\omega C} \\
 v_{cuc1} = -\frac{Di_{dc} \sin(\omega t + \psi + \frac{2\pi}{3})}{3\omega C} + \frac{I_1 \sin(\omega t + \phi + \frac{2\pi}{3})}{4\omega C} - \frac{DI_2 \sin(\omega t + \theta - \psi + \frac{2\pi}{3})}{2\omega C}
 \end{cases} \quad (2-50)$$

Using the park transformation T from (2-42), in DQ coordinates we get:

$$\begin{aligned}
 \vec{v}_{cu1dq} &= \frac{i_{dc}}{3C} \begin{pmatrix} 0 & -\frac{1}{\omega} \\ \frac{1}{\omega} & 0 \end{pmatrix} \vec{d}_{dq} - \frac{1}{4C} \begin{pmatrix} 0 & -\frac{1}{\omega} \\ \frac{1}{\omega} & 0 \end{pmatrix} \vec{i}_{dq} \\
 &- \sqrt{\frac{2}{3}} \frac{1}{2\omega C} \begin{pmatrix} -d_q & d_d \\ -d_d & -d_q \end{pmatrix} \vec{i}_{cirdq}
 \end{aligned} \quad (2-51)$$

Similarly, for the lower arm we get $\vec{v}_{cl1dq} = -\vec{v}_{cu1dq}$, and for the 2nd harmonic

component:

$$\begin{cases} v_{cua2} = -\frac{DI_1 \sin(2\omega t + \psi + \phi)}{8\omega C} + \frac{I_2 \sin(2\omega t + \theta)}{4\omega C} \\ v_{cub2} = -\frac{DI_1 \sin(2\omega t + \psi + \phi + \frac{2\pi}{3})}{8\omega C} + \frac{I_2 \sin(2\omega t + \theta + \frac{2\pi}{3})}{4\omega C} \\ v_{cuc2} = -\frac{DI_1 \sin(2\omega t + \psi + \phi - \frac{2\pi}{3})}{8\omega C} + \frac{I_2 \sin(2\omega t + \theta - \frac{2\pi}{3})}{4\omega C} \end{cases} \quad (2-52)$$

Using the transformation T_2 , in DQ coordinates we get:

$$\overrightarrow{v_{cu2dq}} = -\sqrt{\frac{2}{3}} \frac{1}{8\omega C} \begin{pmatrix} -d_q & d_d \\ -d_d & -d_q \end{pmatrix} \overrightarrow{i_{dq}} - \frac{1}{4C} \begin{pmatrix} 0 & -\frac{1}{\omega} \\ \frac{1}{\omega} & 0 \end{pmatrix} \overrightarrow{i_{cirdq}} \quad (2-53)$$

Similarly, for the lower arm we get:

$$\overrightarrow{v_{cl2dq}} = \overrightarrow{v_{cu2dq}} \quad (2-54)$$

From (2-38) and (2-40), the capacitor voltage in the DQ frame can be obtained.

2.2.5 Simulation Results

In this section, simulation analysis has been done to evaluate the new modeling in the DQ frame and to compare it with the three phase abc and switching model. The simulation specifications are given in Table 2-1. All three models (i.e. three-phase switching and average model and DQ model) are simulated in the Simulink/ Matlab. The switching model of the MMC is verified experimentally in the literature [42], [46] and [47].

Table 2- 1: MMC parameters values for DQ model verification

Output Frequency	60 Hz
L	1.2 mH
C	3400 μ F
Ri	0.04 Ω
Vdc	3kV
Modulation Index m	0.9
Output Voltage	3kV L-L
P	0.5MW
Module Voltage	1kV
DC Bus Voltage	3 kV
Modules per arm	3
Load R	6
Load L	9mH

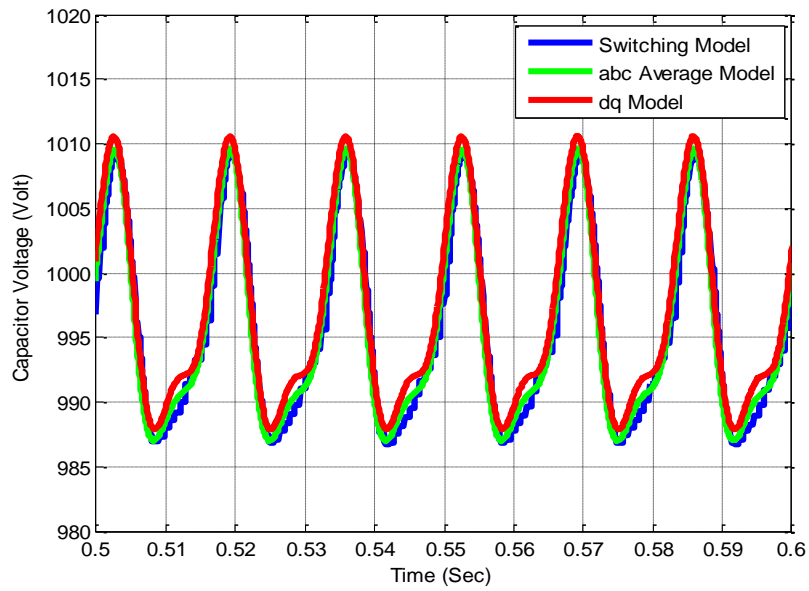


Figure 2- 6: MMC Capacitor Voltage from Switching, abc and DQ model.

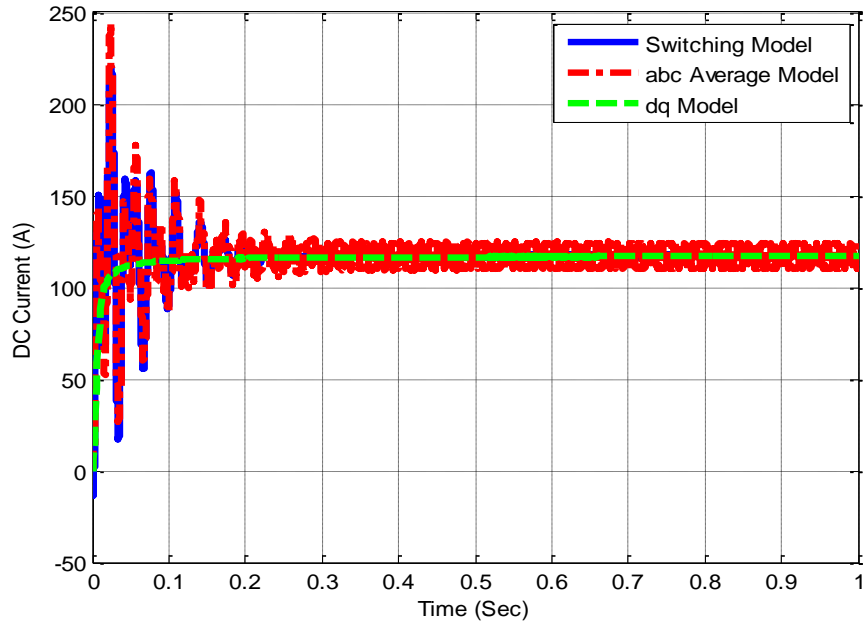


Figure 2- 7: DC Current from Switching, abc and DQ model

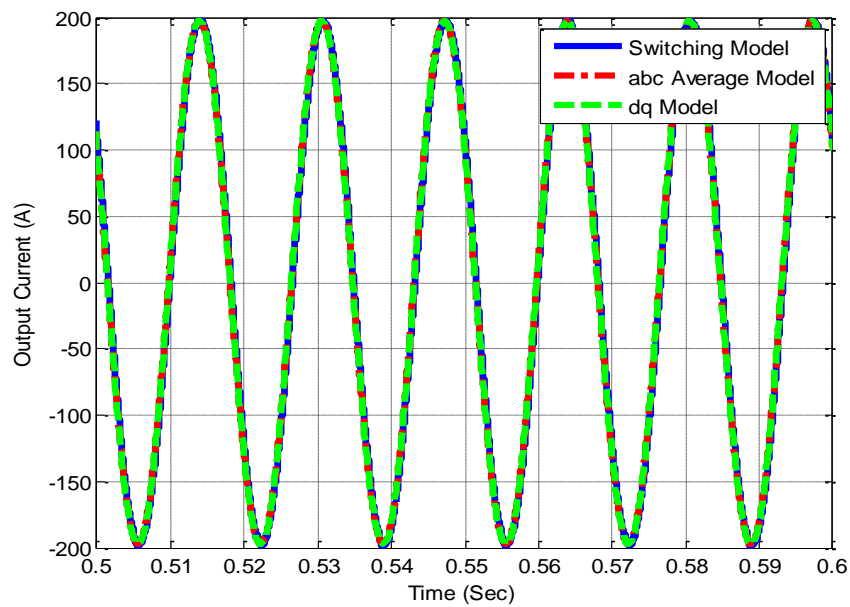


Figure 2- 8: Phase current from switching, abc average and DQ model

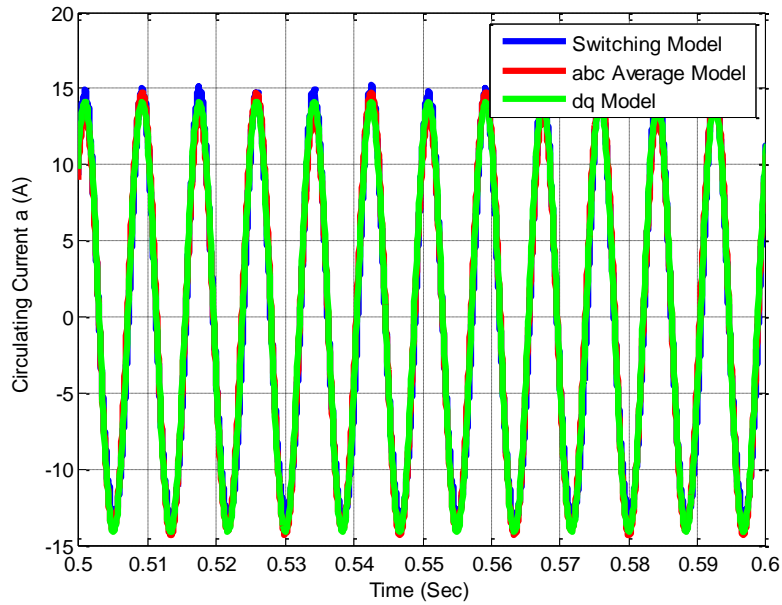


Figure 2- 9: Circulating current from switching, abc average and DQ model

In Figure 2-6, the capacitor voltage from Switching, abc average, and DQ model are shown. As can be seen, the three models are well-matched together. The capacitor voltage from the DQ model has a slight discrepancy because of the elimination of the higher order harmonics greater than the second harmonic. Figure 2-7, Figure 2-8 and Figure 2-9 show the DC current, phase current, and the circulating current in the switching, average and DQ model, respectively. The current waveforms are well-suited with respect to each other. And finally, the output line-to-line voltage is demonstrated in Figure 2-10. The waveforms are compatible in all three models as well.

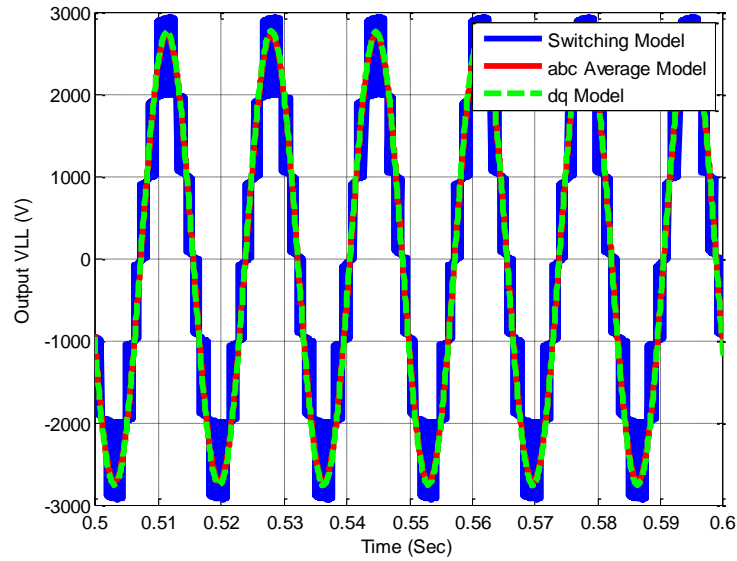


Figure 2- 10: MMC DC, phase, and circulating current from switching, abc average and DQ model

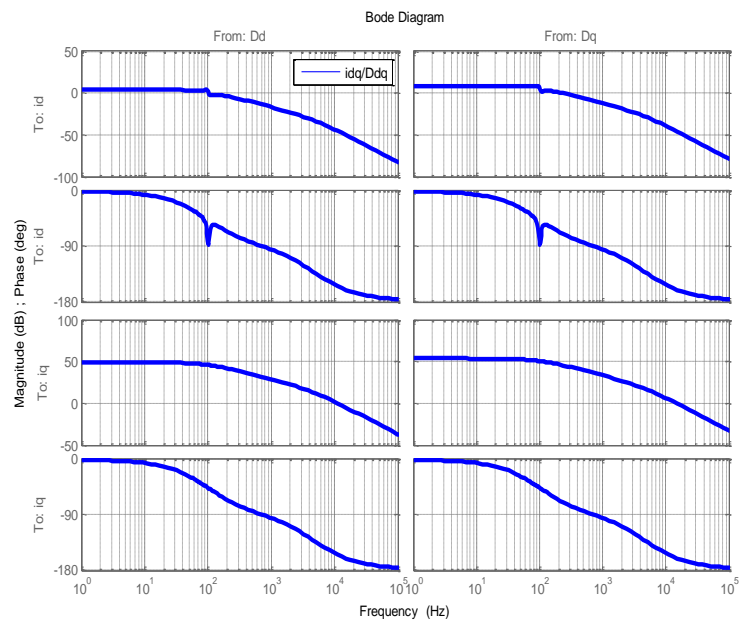


Figure 2- 11: Open loop transfer function of output current to duty cycle in DQ.

Once we have the DQ model, using linearization tools, such as the MATLAB linearization tool, the model can be linearized and the open loop transfer functions can be extracted. In Figure 2-11, the open loop transfer function of the output current to duty

cycle in DQ is shown. By having the open loop transfer function, the desirable controller can be designed for the inner and outer loop of the MMC.

2.2 Alternate-Arm Converter Modeling

2.3.1 Introduction

The operation of the MMC imposes the relatively high circulating current, which reduces efficiency of the converter, increases the junction temperature of the switches, causes further fluctuation of each module capacitor voltage, and decreases reliability. Furthermore, the main issue of the lack of DC fault block capability in the MMC with half-bridge still remains [36],[46],[47],[58].

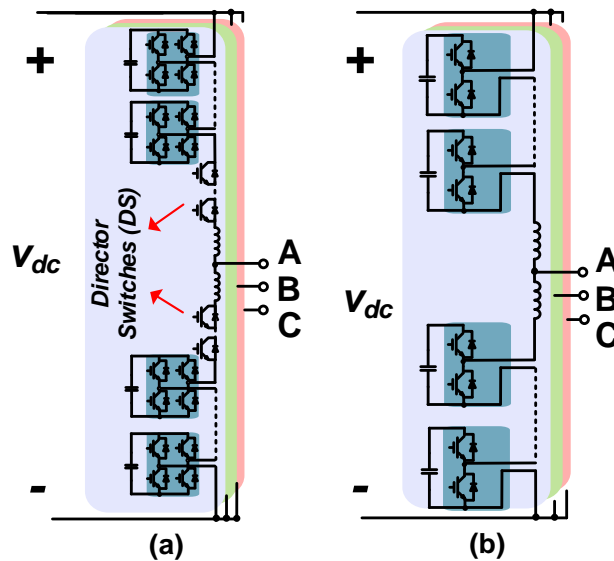


Figure 2- 12: (a) Alternate Arm Converter (AAC), (b) Modular Multilevel Converter (Half- Bridge)

As mentioned in chapter 1, with the appearance of the MMC, an attractive multilevel converter topology was made and defined as the Hybrid Multilevel Converter, using a similar topology, created by combining a two-level converter with a series of Half

or Full-Bridge or Power Electronic Building Blocks (PEBB) [36]. After the AAC introduced by Alstom in 2010, several research projects have been carried out involving the operation and control of the converter [23]. In [29], some interesting innovative concepts for creating the novel Hybrid Multilevel Converters are presented. A 24MW level VSC converter to evaluate different hybrid multilevel topologies from Alstom Grid is studied in [59]. Also, an overview of the Modular Multilevel Converters for HVDC applications is done in [60]. As is mentioned in chapter 1, an Alternate Arm Converter (AAC) can be realized by adding a two-level voltage converter and a wave-shaping circuit on the DC side [23]. The structure is very similar to the Modular Multilevel Converter (MMC), which makes the operation of the AAC similar to the MMC, with the exception that it has switches to alternate the load power between upper arm and lower arm. Figure 2-12 shows the AAC and MMC configurations. As can be seen, the AAC has a series of switches called Director Switches (DS) to alternate the arm current between upper and lower arm. The main advantage of the AAC over the MMC is the capability of DC-Fault ride-through and operation as a STATCOM after DC fault [61]. In Chapter 5, DC fault ride-through of the AAC will be discussed elaborately. In this section, first the operation principle of the AAC will be explained and then the switching model and average model of the AAC will be discussed.

2.3.2 Alternate Arm Converter (AAC) Operation Principles

In Figure 2-13, the single phase schematic of the AAC is shown. AAC consists of the upper and lower arm Cascaded H-Bridges which provide the wave-shaping circuits. The director switches include IGBTs connected in series in order to withstand the

maximum voltage which could be applied across the director switch when it is in the open state.

To provide a sinusoidal voltage, the wave-shaping cascaded-bridge converter should produce the voltage as shown in the Figure 2-13. For standard operation, the three phase-legs operate in the same fashion with phase-legs 'b' and 'c,' lagging leg 'a' by 120° and 240° , respectively. Taking one phase-leg as an example, in the "upper arm active" converter operation state, the upper arm is responsible for synthesizing positive voltages at the converter AC voltage terminal by modulating the upper arm modules when the upper arm director switch is closed. During the "lower arm active state", negative converter voltages are synthesized by modulating the lower arm modules when the lower arm director switch is closed. During these two states, the upper and lower arm director switches act as a complementary pair. An additional state, named "overlap", is used between the two aforementioned states in which both the upper and lower arm director switches are closed, allowing a current that is common to the two arms to flow. This current can be controlled to aid in the capacitor voltage balancing of the modules by modulating the upper and lower arms' power modules appropriately. The overlap time existence principle and control will be discussed in the next chapters.

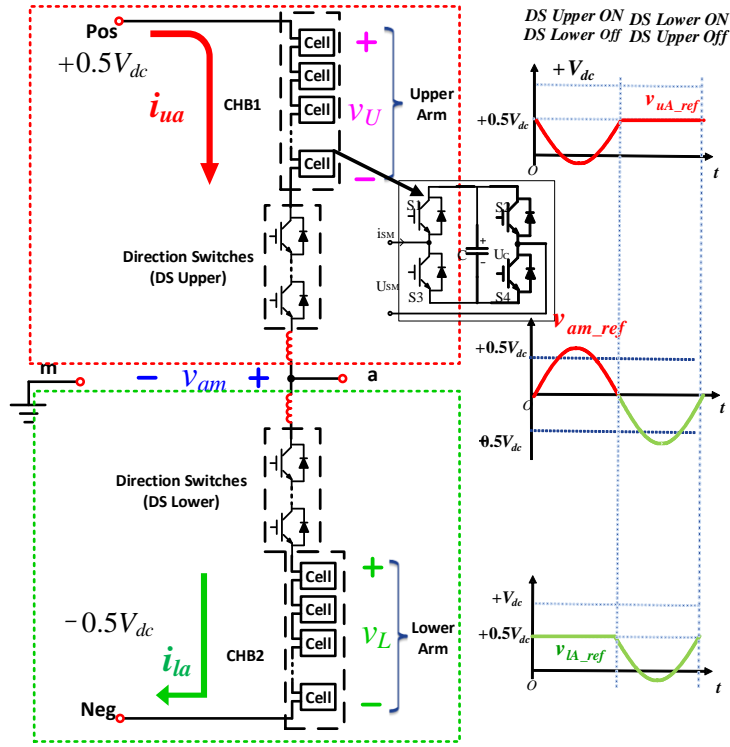


Figure 2-13: Basic operation of the AAC

One of the features of the AAC is that the module of the AAC should be in full-bridge to provide the operation of the AAC in the so-called sweet-spot [61]. As will be shown later, in the sweet spot, the energy between the DC side and the AC side are balanced and the control efforts to balance the capacitor voltage will be easier.

2.3.3 AAC Voltage and Current Specifications

According to Figure 2-13, in order to have a sinusoidal output voltage, the upper and lower arm full-bridge stacks voltage references should be as follows:

$$\begin{cases} V_{uA}(t) = \frac{V_{dc}}{2} - m \frac{V_{dc}}{2} \sin \omega t & \text{if } 0 \leq \omega t < \pi \\ V_{lA}(t) = \frac{V_{dc}}{2} + m \frac{V_{dc}}{2} \sin \omega t & \text{if } \pi \leq \omega t < 2\pi \end{cases} \quad (2-55)$$

By having the references of the upper and lower arm stacks, from upper and lower KVL equations, the output phase voltage can be obtained by:

$$\begin{cases} V_a = \frac{V_{dc}}{2} - V_{uA} - L_{arm} \frac{di_{uA}}{dt} & \text{if } 0 \leq \omega t < \pi \\ V_a = V_{lA} - \frac{V_{dc}}{2} - L_{arm} \frac{di_{lA}}{dt} & \text{if } \pi \leq \omega t < 2\pi \end{cases} \quad (2-56)$$

Notice that the upper arm and lower arm current will conduct the positive and negative side of the output current, respectively. So, the upper and lower arm currents will be:

$$i_{uA} = -i_{lA} = i_{ac} \quad (2-57)$$

2.3.4 Sweet Spot Calculation of the AAC

The operation of the AAC during the positive cycle is shown in Figure 2-13, where the upper arm is conducting the energy. By defining the output voltage and current as:

$$\begin{cases} v_{ac} = V_{ac} \sin(\omega t) \\ i_{ac} = I_{ac} \sin(\omega t + \phi) \end{cases} \quad (2-58)$$

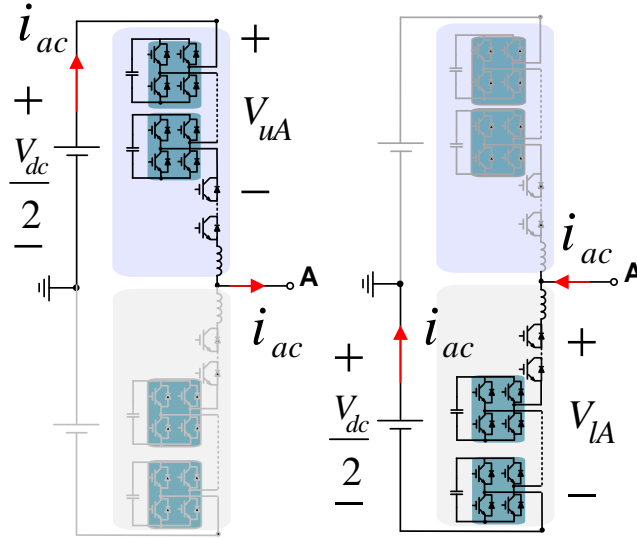


Figure 2- 14 Single phase AAC operation in positive and negative cycles

The DC-side energy equation can be written:

$$E_{DC} = \int_0^{T/2} \frac{V_{dc}}{2} \times i_{ac} dt \Rightarrow E_{DC} = \frac{V_{dc} I_{ac} \cos(\phi) T}{2\pi} \quad (2-59)$$

Where the current in the DC side will be the load current as shown in Figure 2-14.

The AC side energy equation can be found:

$$E_{AC} = \int_0^{T/2} v_{ac} \times i_{ac} dt \Rightarrow E_{AC} = \frac{V_{ac} I_{ac} \cos(\phi) T}{4} \quad (2-60)$$

In order to have balanced energy during the half line frequency cycle, the input and output energy should be equal. By equalizing the energy equations, the modulation index to have balanced energy during the half of line frequency cycle can be obtained:

$$E_{DC} = E_{AC} \Rightarrow \frac{V_{dc} I_{ac} \cos(\phi) T}{2\pi} = \frac{V_{ac} I_{ac} \cos(\phi) T}{4} \Rightarrow V_{ac} = \frac{2}{\pi} V_{dc} \quad (2-61)$$

Equation (2-61) provides the modulation index to be in the over-modulation region as is shown in (2-62):

$$V_{ac} = \frac{4 V_{dc}}{\pi \cdot 2} \Rightarrow M = \frac{4}{\pi} = 1.273 \quad (2-62)$$

From the above equation, we discover that to have balanced energy during the operation of the upper and lower arm, the converter should have a modulation index of $4/\pi$. As the result, the upper and lower arm modules of the AAC should be Full-Bridge to make the negative voltage possible over the stack.

2.3.5 AAC Switching Modeling

This section describes the derivation of the mathematical switching model of the AAC. A simple three-phase AAC circuit with DC-link filter and one full-bridge power module per arm is shown in Figure 2-15, where the converter is connected to the AC grid.

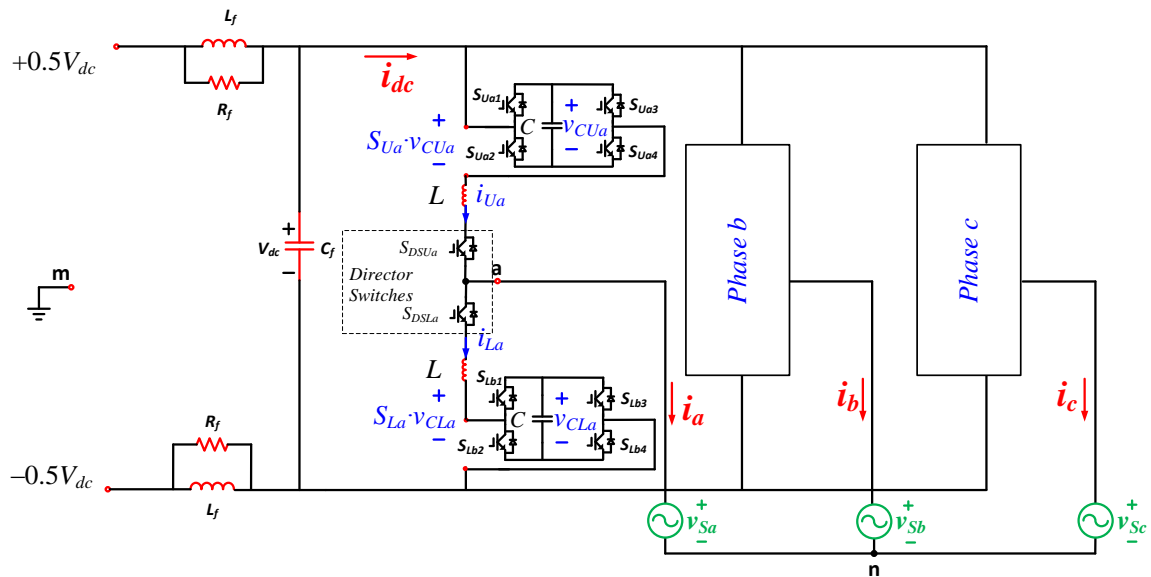


Figure 2- 15: AAC with one module in each arm

Since the AAC has full-bridge power cells with four power switches, the H-bridge switches are modeled using a converter transfer function featuring three states $\{-1,0,1\}$. The director switch, modeled as a conventional switching function $\{0,1\}$, turns off at zero

current with appropriate control. Since operation of the AAC provides relatively high ripple on DC current [62], the DC-link of the converter is connected to a DC-link filter, which provides the interface to the DC-grid. For modeling simplicity, the DC-grid is assumed to be a locally connected stiff voltage source. A state-space model of the AAC can be derived by taking the arm inductor currents, DC-link filter inductor current, and module capacitor voltages as states. The voltage across the part of the DC-link filter in series with the DC-line, v_f , is given by (2-63) or (2-64). Equating (2-63) and (2-64) obtains (2-65), which is the filter inductor current, i_{L_f} , state-space equation, where R_f is the filter resistance, L_f is the filter inductance, and I_{DCg} is the DC-grid current.

$$V_f = L_f \frac{d}{dt} i_{L_f} \quad (2-63)$$

$$V_f = (i_{DCg} - i_{L_f}) R_f \quad (2-64)$$

$$\frac{d}{dt} i_{L_f} = -\frac{R_f i_{L_f}}{L_f} + \frac{R_f i_{DCg}}{L_f} \quad (2-65)$$

The three phase upper arm inductor current state-space equations can be derived by taking a KVL loop from the DC-grid midpoint to the AC-grid neutral via an upper arm and then directly back to the DC-grid midpoint as shown in (2-66), where L is the arm inductance, V_{DCg} is the DC-grid voltage, v_{DSUx} is the voltage across an upper arm's director switch, v_{Sx} is the phase supply voltage, and v_{nm} is the DC-grid midpoint to AC-grid neutral voltage. Similarly, (2-67) gives the three lower arm inductor current state-space equations, where v_{DSLx} is the voltage across a lower arm director switch.

$$\frac{d}{dt} i_{Ux} = \frac{S_{DSUx}}{L} \left(\frac{V_{DCg}}{2} - L_f \frac{d}{dt} i_{L_f} - \sum_{i=1}^n S_{Uxi} v_{Uxi} - v_{DSUx} - v_{Sx} - v_{nm} \right) \quad (2-66)$$

$$\frac{d}{dt}i_{Lx} = \frac{S_{DSLx}}{L} \left(\frac{V_{DCg}}{2} - L_f \frac{d}{dt}i_{Lf} - \sum_{i=1}^n S_{Lxi} v_{Lxi} - v_{DSLx} + v_{Sx} + v_{nm} \right) \quad (2-67)$$

The voltages across the upper (vDSUx) and lower (vDSLx) arm director switches can be defined by (2-68) and (2-69) respectively, by applying KVL to the loop around the DC-grid and a phase-leg, and noting that when a director switch is closed, the voltage across it is zero.

$$v_{DSUx} = (1 - S_{DSUx}) \left(-V_{DCg} + 2L_f \frac{d}{dt}i_{Lf} + \sum_{i=1}^n S_{Uxi} v_{Uxi} + L \frac{d}{dt}i_{Ux} + v_{DSLx} + L \frac{d}{dt}i_{Lx} + \sum_{i=1}^n S_{Lxi} v_{Lxi} \right) \quad (2-68)$$

$$v_{DSLx} = (1 - S_{DSLx}) \left(-V_{DCg} + 2L_f \frac{d}{dt}i_{Lf} + \sum_{i=1}^n S_{Uxi} v_{Uxi} + L \frac{d}{dt}i_{Ux} + v_{DSUx} + L \frac{d}{dt}i_{Lx} + \sum_{i=1}^n S_{Lxi} v_{Lxi} \right) \quad (2-69)$$

Substituting (2-69) into (2-68) allows the lower arm director switch voltage to be eliminated from (2-68); consequently, (2-70) can be obtained. Similarly, for the lower arm director switches, (2-71) can be obtained.

$$v_{DSUx} = \frac{(1 - S_{DSUx})}{(-S_{DSUx} - S_{DSLx} + S_{DSUx}S_{DSLx})} \left(\begin{array}{l} -V_{DCg} + 2L_f \frac{d}{dt}i_{Lf} + \sum_{i=1}^n S_{Uxi} v_{Uxi} + L \frac{d}{dt}i_{Ux} + L \frac{d}{dt}i_{Lx} + \sum_{i=1}^n S_{Lxi} v_{Lxi} \\ + (1 - S_{DSLx}) \left(-V_{DCg} + 2L_f \frac{d}{dt}i_{Lf} + \sum_{i=1}^n S_{Uxi} v_{Uxi} + L \frac{d}{dt}i_{Ux} + L \frac{d}{dt}i_{Lx} + \sum_{i=1}^n S_{Lxi} v_{Lxi} \right) \end{array} \right) \quad (2-70)$$

$$v_{DSLx} = \frac{(1 - S_{DSLx})}{(-S_{DSUx} - S_{DSLx} + S_{DSUx}S_{DSLx})} \left(\begin{array}{l} -V_{DCg} + 2L_f \frac{d}{dt}i_{Lf} + \sum_{i=1}^n S_{Uxi} v_{Uxi} + L \frac{d}{dt}i_{Ux} + L \frac{d}{dt}i_{Lx} + \sum_{i=1}^n S_{Lxi} v_{Lxi} \\ + (1 - S_{DSUx}) \left(-V_{DCg} + 2L_f \frac{d}{dt}i_{Lf} + \sum_{i=1}^n S_{Uxi} v_{Uxi} + L \frac{d}{dt}i_{Ux} + L \frac{d}{dt}i_{Lx} + \sum_{i=1}^n S_{Lxi} v_{Lxi} \right) \end{array} \right) \quad (2-71)$$

The DC-grid midpoint to AC-grid neutral voltage is given by (2-72).

$$v_{nm} = \frac{1}{6} \left(- \sum_{x=a,b,c} \sum_{i=1}^n S_{Uxi} v_{Uxi} + \sum_{x=a,b,c} \sum_{i=1}^n S_{Lxi} v_{Lxi} - \sum_{x=a,b,c} v_{DSUx} + \sum_{x=a,b,c} v_{DSLx} \right) \quad (2-72)$$

The three-phase line current's state-space equations are given by (2-73). By making the state-space variable transformation [52], the three sum current, isumx, state-space equations are given by (2-74).

$$\frac{d}{dt} i_x = \frac{1}{L} \begin{bmatrix} S_{DSUx} \left(\frac{V_{DCg}}{2} - L_f \frac{d}{dt} i_{Lf} - \sum_{i=1}^n S_{Uxi} v_{Uxi} - v_{DSUx} - v_{Sx} - v_{nm} \right) \\ - S_{DSLx} \left(\frac{V_{DCg}}{2} - L_f \frac{d}{dt} i_{Lf} - \sum_{i=1}^n S_{Lxi} v_{Lxi} - v_{DSLx} + v_{Sx} + v_{nm} \right) \end{bmatrix} \quad (2-73)$$

$$\frac{d}{dt} i_{sumx} = \frac{1}{L} \begin{bmatrix} S_{DSUx} \left(\frac{V_{DCg}}{2} - L_f \frac{d}{dt} i_{Lf} - \sum_{i=1}^n S_{Uxi} v_{Uxi} - v_{DSUx} - v_{Sx} - v_{nm} \right) \\ + S_{DSLx} \left(\frac{V_{DCg}}{2} - L_f \frac{d}{dt} i_{Lf} - \sum_{i=1}^n S_{Lxi} v_{Lxi} - v_{DSLx} + v_{Sx} + v_{nm} \right) \end{bmatrix} \quad (2-74)$$

As the converter DC-link current can be defined by (2-75), (2-76) can be written by substituting (2-66) into (2-75) completing the model derivation for the AAC.

$$i_{dc} = i_{Ua} + i_{Ub} + i_{Uc} \quad (2-75)$$

$$\frac{d}{dt} i_{dc} = \frac{1}{L} \sum_{x=a,b,c} S_{DSUx} \left(\frac{V_{DCg}}{2} - L_f \frac{d}{dt} i_{Lf} - \sum_{i=1}^n S_{Uxi} v_{Uxi} - v_{DSUx} - v_{Sx} - v_{nm} \right) \quad (2-76)$$

So the complete state-space model is given by (2-77).

$$\left\{ \begin{array}{l}
\frac{d}{dt} i_{dc} = \frac{1}{L} \sum_{x=a,b,c} S_{DSUx} \left(\frac{V_{DCg}}{2} - L_f \frac{d}{dt} i_{Lf} - \sum_{i=1}^n S_{Uxi} v_{Uxi} - v_{DSUx} - v_{Sx} - v_{nm} \right) \\
\frac{d}{dt} i_a = \frac{1}{L} \left[\begin{array}{l}
S_{DSUa} \left(\frac{V_{DCg}}{2} - L_f \frac{d}{dt} i_{Lf} - \sum_{i=1}^n S_{Uai} v_{Uai} - v_{DSUa} - v_{Sa} - v_{nm} \right) \\
- S_{DSL a} \left(\frac{V_{DCg}}{2} - L_f \frac{d}{dt} i_{Lf} - \sum_{i=1}^n S_{Lai} v_{Lai} - v_{DSL a} + v_{Sa} + v_{nm} \right)
\end{array} \right] \\
\frac{d}{dt} i_b = \frac{1}{L} \left[\begin{array}{l}
S_{DSUb} \left(\frac{V_{DCg}}{2} - L_f \frac{d}{dt} i_{Lf} - \sum_{i=1}^n S_{Ubi} v_{Ubi} - v_{DSUb} - v_{Sb} - v_{nm} \right) \\
- S_{DSL b} \left(\frac{V_{DCg}}{2} - L_f \frac{d}{dt} i_{Lf} - \sum_{i=1}^n S_{Lbi} v_{Lbi} - v_{DSL b} + v_{Sb} + v_{nm} \right)
\end{array} \right] \\
\frac{d}{dt} i_{sumx} = \frac{1}{L} \left[V_{DCg} - 2L_f \frac{d}{dt} i_{Lf} - \sum_{i=1}^n S_{Uxi} v_{Uxi} - \sum_{i=1}^n S_{Lxi} v_{Lxi} \right] \\
\frac{d}{dt} v_{Uxi} = \frac{1}{C} S_{Uxi} i_{Ux} \\
\frac{d}{dt} v_{Lxi} = \frac{1}{C} S_{Lxi} i_{Lx}
\end{array} \right. \quad (2-77)$$

where $i=1, \dots, n$, is the number of modules. The average and DQ model of the AAC include the director switches switching function which adds nonlinearity to the model and leads to the complicated analytical model.

2.3 Conclusion

In this chapter, the switching, average and DQ frame model of the MMC is derived. For extraction of the DQ model, the capacitor voltage is assumed to be constant, the second order harmonic of the circulating current is assumed to be dominant, and the other harmonic components are neglected. The DQ model is extracted from the average model in a separate reference frequency and the superposition is applied to obtain the

final DQ model from different frequency references. Although the extracted model is complicated in the DQ frame, by using the proposed DQ model, the design of the inner and outer loop controller of the converter can be simplified. By implementing the obtained model in a simulation software such as SIMULINK/MATLAB and using linearization tools, the bode diagram of the required transfer functions can be extracted for converter control design purposes.

Furthermore, the AAC operation principles are discussed in this chapter. Since the modeling of this converter is more complex than the MMC, the switching model of the AAC is presented here, and further extraction of the DQ model leads to a very complicated nonlinear model. During the “upper arm active” and “lower arm active” states, the AAC line currents are controlled by the upper and lower arm modules respectively. However, in the “overlap” state, the AAC shares very similar features to the MMC. Hence, both the MMC and AAC at “overlap” have the same state equations for the line currents. In both the MMC and AAC, the capacitors of the power modules act as intermediate energy storage between the DC and AC terminals. Thus, to ensure a balanced voltage operation among these capacitors, a zero net change requirement of total stored energy must be enforced over a fundamental frequency period. The actual power balance is achieved by the flowthrough of the sum current, which, along with DC offset, is indispensable for both converters. However, the “overlap” states in the AAC only occur in one phase-leg at a time, that is, only one phase-leg can have both director switches on simultaneously. This is a fundamental difference with the MMC in terms of circulating current, since the circulation of current between phase-legs, present in the

MMC, is not present in the AAC. This distinguishes the converters from each other in the way that each can balance their capacitor voltages.

Chapter 3 **Modular Multilevel Converters Control**

3.1 Introduction

In this chapter, the arm balancing, module capacitors voltage balance, and closed loop output power control associated with modular multilevel converters will be discussed. The control method used in this work is based on Makoto Hagiwara and Hirofumi Akagi's arm balancing and output current control method [42],[63]. Based on this method, the power cell capacitor's voltage control of the modular multilevel converters is divided into: the capacitor voltage average control or energy balancing, individual capacitor voltage control, and arm-balancing control. The normal operation of the MMC deals with internal even harmonics current, which circulates through the arms in each phase. This circulating current causes more power losses and more ripple on capacitor voltage. Since the MMC involves interaction between capacitor voltage and the circulating current [46], the internal capacitor control should be equipped with circulating current suppressing control. Using a circulating current controller can reduce the stress over the capacitors as well as the arm current, which results in lower thermal stress throughout the module components. Using circulating current suppressing control will change the design process of the arm inductor. This will be discussed in the next chapter. Many studies have been carried out to control and reduce the circulating current of the converter. In [48], a reduced switching-frequency modulation method based on the

sorting algorithm by using a phase-shifted carrier is proposed. The circulating current suppression control in [48] is modeled and design in the DQ frame, where, due to the need for PLL, it increases the complexity of the circuit. To avoid using PLL, the Circulating Current Suppressing Control (CCSC) for the MMC is implemented using a Proportional-Quasi-Resonant (PQR) controller, as described in [58]. In this thesis, the Proportional-Quasi-Resonant (PQR) controller will be considered in the design of the CCSC for a modular multilevel converter based on the same method proposed in [58]. To study the circulating current, the following mathematical modeling of the MMC is performed. Figure 3-1 shows the circuit schematic of the MMC under consideration, featuring N power modules per phase-arm (positive and negative phase-arm within the phase-leg), and $2N$ power modules per phase-leg. These power modules are connected in series as shown in the figure, where in this case all power modules are constructed with half-bridge circuits feeding a flying capacitor, although other configurations using a full-bridge or alternative circuit configurations may be used as well, depending on the application objectives and requirements.

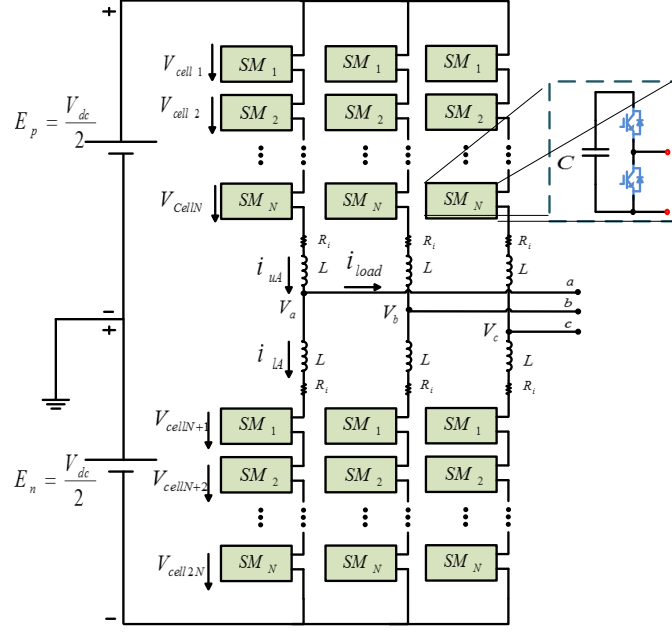


Figure 3- 1: Modular Multilevel Converter topology with each power module structure

As shown in [46], the upper phase-arm and lower phase-arm currents contain even order harmonics, with the second order component being the most significant one.

Per Figure 3-1, the upper and lower phase-arm currents are given by

$$I_{uA} = \frac{I_{dc}}{3} + \frac{I_a}{2} \sin(\omega t + \varphi) + I_{h2} \sin(2\omega t + \theta) \quad (3-1)$$

$$I_{lA} = \frac{I_{dc}}{3} - \frac{I_a}{2} \sin(\omega t + \varphi) + I_{h2} \sin(2\omega t + \theta) \quad (3-2)$$

Employing an average model for the half-bridge converter of the power module, and neglecting the resistive voltage drop across each phase phase-arm, it follows that the reference voltage waveforms for the upper and lower phase-arm modulation signals are:

$$V_{uAref} = \frac{V_{dc}}{2} - m \frac{V_{dc}}{2} \sin \omega t \quad (3-3)$$

$$V_{lAref} = \frac{V_{dc}}{2} + m \frac{V_{dc}}{2} \sin \omega t \quad (3-4)$$

As such, when summing (3-3) and (3-4), which corresponds to measuring the voltage from positive to negative rail, the AC component in these equations cancels out leaving V_{dc} as the result of this sum. Likewise, and taking into consideration a $\pm 120^\circ$ phase-shift between converter phase-legs, when the voltage between two different phases is measured, the DC component ($V_{dc}/2$) cancels out, leaving only the AC term between them.

In normalized terms, (3-3) and (3-4) may be rewritten as shown below, where N_{uA} and N_{lA} correspond to the normalized voltage reference for each power module, which in turn correspond to the average duty cycle of their respective half-bridge switching function.

$$N_{uA} = \frac{1}{2} - m \frac{1}{2} \sin \omega t \quad (3-5)$$

$$N_{lA} = \frac{1}{2} + m \frac{1}{2} \sin \omega t \quad (3-6)$$

Accordingly, the average voltage of the power module capacitors for the upper and lower phase-arms are given by:

$$v_{Cu} = \frac{1}{C\omega} \int N_{uA} I_{uA} d\omega t \quad (3-7)$$

$$v_{Cl} = \frac{1}{C\omega} \int N_{lA} I_{lA} d\omega t \quad (3-8)$$

The total average voltage of the MMC phase-leg is then given by:

$$V_{leg} = V_{uA} + V_{lA} = N \left(\frac{1}{2} - \frac{1}{2} \sin(\omega t) \right) \frac{1}{C} \int N_u i_{uA} dt + N \left(\frac{1}{2} + \frac{1}{2} \sin(\omega t) \right) \frac{1}{C} \int N_l i_{lA} dt \quad (3-9)$$

The difference between the DC voltage component and the total voltage across the phase-leg corresponds to the voltage across the phase-arm inductors, which is the

driving voltage for the circulating current of the MMC. Accordingly, this voltage is defined as:

$$V_{cir} = V_{dc} - V_{leg} \quad (3-10)$$

Regarding the voltage across the power module capacitors, [47] presents a derivation showing that the first, second and third order harmonic components of this voltage can be expressed as:

$$\left\{ \begin{array}{l} \Delta u_{cp}^{(1st)}(t) = \frac{MI_{dc}}{6\omega_1 C_d} \cos(\omega t) - \frac{\sqrt{2}I_a}{4\omega_1 C_d} \cos(\omega t + \varphi) - \frac{MI_{h2}}{4\omega_1 C_d} \sin(\omega t + \theta) \\ \Delta u_{cn}^{(1st)}(t) = -\frac{MI_{dc}}{6\omega_1 C_d} \cos(\omega t) + \frac{\sqrt{2}I_a}{4\omega_1 C_d} \cos(\omega t + \varphi) + \frac{MI_{h2}}{4\omega_1 C_d} \sin(\omega t + \theta) \\ \Delta u_{cp}^{(2nd)}(t) = \frac{\sqrt{2}MI_a}{16\omega_1 C_d} \sin(2\omega t + \varphi) - \frac{I_{h2}}{4\omega_1 C_d} \cos(2\omega t + \theta) \\ \Delta u_{cn}^{(2nd)}(t) = \frac{\sqrt{2}MI_a}{16\omega_1 C_d} \sin(2\omega t + \varphi) - \frac{I_{h2}}{4\omega_1 C_d} \cos(2\omega t + \theta) \\ \Delta u_{cp}^{(3rd)}(t) = \frac{MI_{h2}}{12\omega_1 C_d} \sin(3\omega t + \theta) \\ \Delta u_{cn}^{(3rd)}(t) = -\frac{MI_{h2}}{12\omega_1 C_d} \sin(3\omega t + \theta) \end{array} \right. \quad (3-11)$$

This set of equations shows that the first and second order harmonic voltage components of capacitor voltage ripple not only relate to the circulating current but also to the DC and phase current, showing how the circulating current component may be used to limit these voltage components by partially cancelling out the effect of both DC and AC currents.

Additionally, the second order voltage across the phase-arm inductor V_{cir} can be written as [46],

$$V_{cir} = \frac{N}{2C} \left(\frac{3M}{8\omega} \sqrt{2} I_a \cos(2\omega t + \varphi) - \frac{M^2}{6\omega} I_{dc} \cos(2\omega t) \right) - \frac{N}{2C} \left(\frac{3+2M^2}{6\omega} I_{h2} \cos(2\omega t + \theta) \right) \quad (3-12)$$

From the above equation, and knowing that $V_{h2}^{(2)} = L di_{h2}/dt$, the equation for the circulating current can be obtained by [47]:

$$I_{h2} = \frac{\sqrt{\frac{1}{2}[(A \cos \varphi + B)^2 + (A \sin \varphi)^2]}}{1 - \frac{N}{16\omega_1^2 LC} - \frac{M^2 N}{24\omega_1^2 LC}} \quad (3-13)$$

where,

$$A = \frac{3\sqrt{2}MNI_a}{64\omega_1^2 LC}, B = -\frac{M^2 NI_{dc}}{48\omega_1^2 LC} \quad (3-14)$$

$$\theta = \arctan \frac{A \cos \varphi + B}{A \sin \varphi} \quad (3-15)$$

The above equation can be used to show how the circulating current affects the voltage ripple across the capacitor of a power module, and to study the effect of the circulating current suppressing controller on each phase-arm's quantities.

3.2 Closed Loop Control of the MMC

3.2.1 Design of the Circulating Current Suppressing PR Controller

The voltage balancing control method and the circulating current suppressing controller are shown in Figure 3-2 [42],[58],[63].

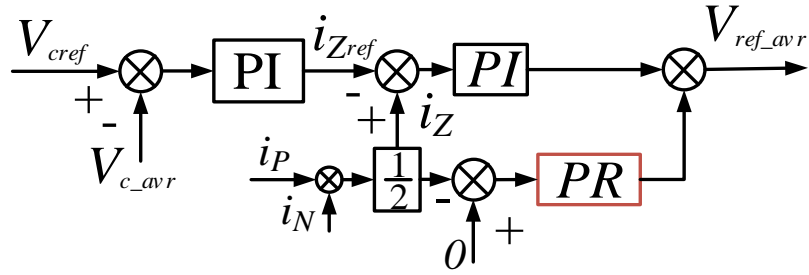


Figure 3- 2: The capacitor average voltage balance control with circulating current suppressing control

The average voltage balance control of the MMC controls the average voltage of the leg to be the reference value. The average control of the capacitors, in fact, controls the energy of the capacitors in the leg during the line cycle to balance the energy between the DC side and the AC side. In the above control scheme, the total capacitor voltage is divided by the number of cells per leg and is compared with the rated capacitor voltage of the cell (i.e. V_{dc}/N). The error through the PI converter defines the value of the reference circulating current, which is needed to make the energy balanced. The reference circulating current is then compared with the actual circulating current and the error passes through a PI controller again to provide the reference voltage. Notice that the sign of the circulating current is negative with respect to the energy exchange between the DC and AC side, so the average voltage is multiplied by the negative sign in the feed forward loop as shown in Figure 3-2. Circulating current suppressing control is implemented on the energy balance control as shown in Figure. The desired value of the circulating current is zero, which means tuning the controller through use of the harmonic regulator PQR for 2nd and 4th order harmonics and dominant harmonic factor of the converter.

In addition to the average voltage control on the MMC, each module needs to have an individual capacitor voltage control to regulate the module's capacitor voltage. In fact,

the individual capacitor voltage can be replaced by the simple sorting algorithm, which is used throughout the literature [43]. Figure 3-3 shows the individual capacitor voltage control for the MMC.

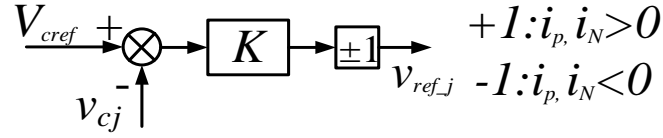


Figure 3- 3: Individual cell capacitor voltage balance control

Individual capacitor voltage control measures the actual value of the capacitors in each cell and it compares that value with the rated value. Through the proportional controller and, depending on the arm current direction, it tunes the controller such that the voltage balance reaches each cell. Using this scheme, the reference voltage for each power module is given by adding the output current reference, the reference achieved by the capacitor average control, and the individual capacitor voltage balance control:

$$\begin{aligned} V_{ref_up} &= V_{ref_avr} + V_{ref_j} + V_{ref_PA} \\ V_{ref_low} &= V_{ref_avr} + V_{ref_j} + V_{ref_NA} \end{aligned} \quad (3-16)$$

A Proportional Quasi-Resonant (PQR) controller is used as a Circulating Current Suppressing Controller (CCSC) as was mentioned before, with the structure shown below.

$$G_{QPR} = K_p + \frac{2\omega_{c1}K_{b1}s}{s^2 + 2\omega_{c1}s + (2\omega_0)^2} + \frac{2\omega_{c2}K_{b2}s}{s^2 + 2\omega_{c2}s + (4\omega_0)^2} \quad (3-17)$$

This controller is used to regulate specific harmonics of a given signal. In the case of the MMC, when controlling the circulating current, the second and the fourth order harmonics are the most significant ones, hence the controller is tuned to these two components. The parameters of the controller are designed for at least 20dB gain on the

tuned harmonics. The MMC circuit parameters used for the design of the controllers is described in Table 3-1. The parameters of the controller are designed to provide the corresponding gain are shown in Table 3-2. The Bode plot of the controller is shown in Figure 3-4. As shown, the resonant frequencies correspond to 120 Hz and 240 Hz.

Table 3- 1: MMC parameters values for closed-loop control simulation

Output Frequency	60 Hz
Switching Frequency	540 Hz
L	3.7 mH
C	4000 μ F
Ri	0.004 Ω
Modulation Index m	0.9
Output Voltage	6kV L-L
P	3MW
Voltage Over each Module	1kV
DC Bus Voltage	10 kV
Number of Module per arm	10

Table 3- 2: The CCSC controller parameters

ω_0	60Hz
ω_{c1}	10Hz
ω_{c2}	10Hz
K_{b1}	10
K_{b2}	10
K_p	1

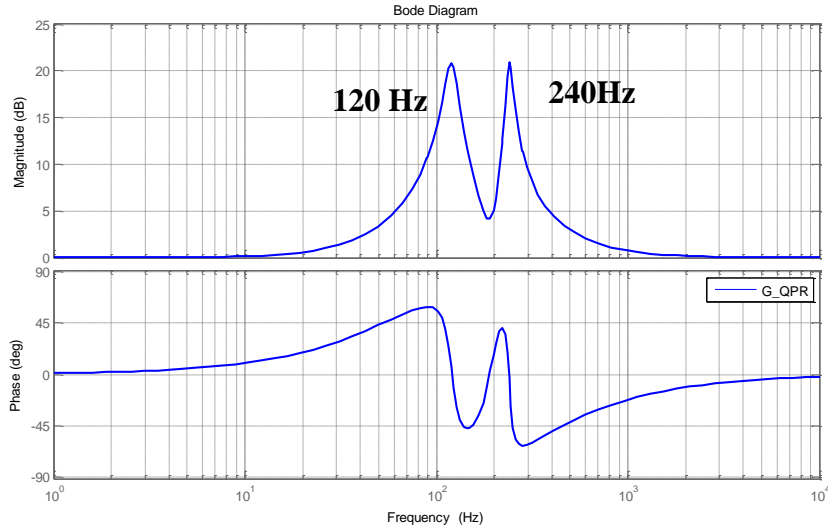
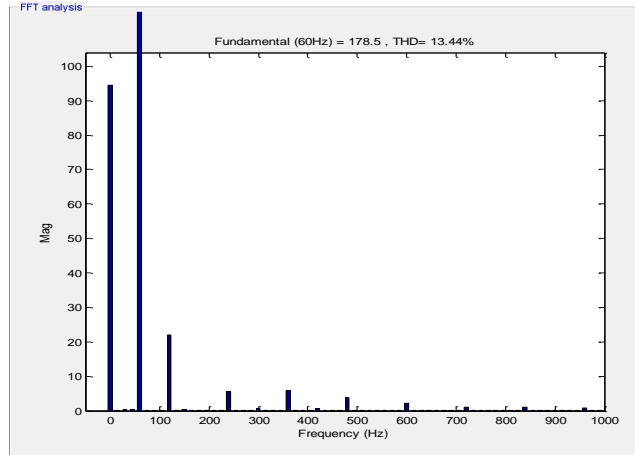


Figure 3- 4: Bode plot of the circulating current suppressing Proportional Quasi Resonant (PQR) controller

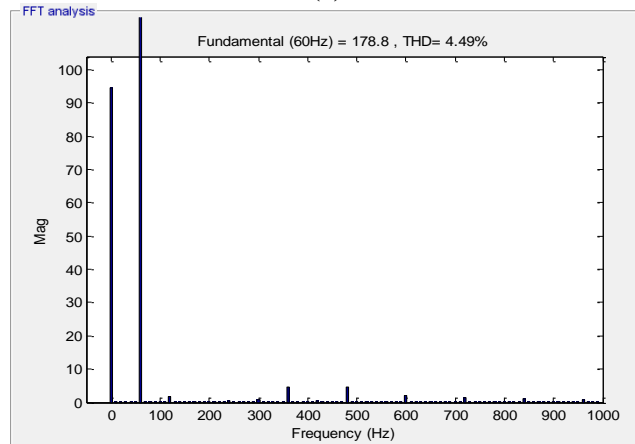
In order to show the circulating current suppressing controller at work and gauge its impact, simulations using the model developed are conducted. In Figure 3-5, the upper phase-arm current harmonic contents are shown. The harmonic analysis for the upper phase-arm current, the capacitor voltage ripple, as well as the output voltage and current is then performed when the Circulating Current Suppressing Controller (CCSC) is active. The results are compared to the case without the controller and shown in Table 3-3, which illustrates the positive impact that this controller has on all converter variables, with only a slight increase in the converter output's current distortion. Specifically, both the capacitor voltage and current improved their harmonic distortion, translating to lower losses and less voltage stress for the IGBTs of the power module. The phase-arm current also saw its distortion diminished, resulting in lower thermal stress for all IGBT and capacitors in the converter structure.

Table 3- 3: Stress Analysis With/ Without Circulating Current Suppressing Controller

Modulation Technique	IuA THD	Vcu THD	Voll THD	Io THD	Icap THD
PSC WO CCSC	13.94%	43.69%	6.87%	1.06 %	160.14%
PSC WI CCSC	4.86%	38.23%	6.7%	1.21%	149.39%



(a)



(b)

Figure 3- 5: Upper phase-arm current harmonic contents a) without the circulating current suppressing controller b) with circulating current suppressing control

3.2.2 Closed Loop Output Current Control of the MMC

The closed loop output power control of the MMC in inverter mode is shown in Figure 3-6. As shown, the complete closed loop control of the MMC mainly consists of three parts: the output current controller, the decoupling control, and finally a voltage

balance and circulating current control. The outer loop controller of the MMC needs to be designed so that the circulating current suppressing controller has no impact on the output. This can be accomplished by having higher bandwidth for the inner current loop and lower bandwidth for the outer one.

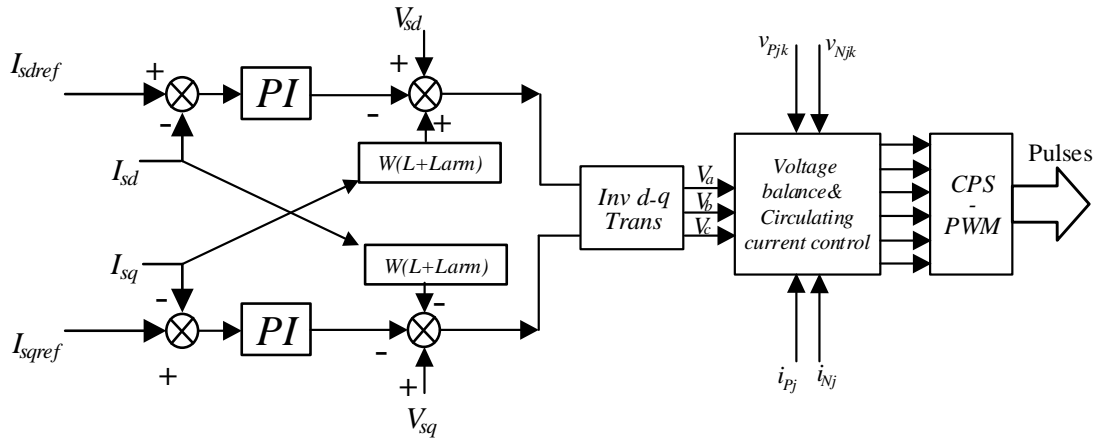


Figure 3- 6: Closed loop control of the MMC

The closed-loop current control measures the three-phase output current and through the PLL, the three-phase current is transformed to the DQ current axis. The DQ current axis is compared with the reference currents and through the PI controller the signal goes to the decoupling part where the DQ axis decoupled [63]. Then the output current reference going to the capacitor, the voltage balance and circulating current control (discussed in previous parts of this thesis), and the total reference of each module will be achieved by summing up the three control references.

3.3 Closed-Loop Control of the AAC

In this section, the closed-loop control, which is required for the Alternate-Arm Converter will be discussed. First, the details of energy balancing in the arm will be

explained and the average and individual capacitor voltage control will be proposed based on the same control method used for the MMC.

3.3.1 Capacitor Voltage Analysis of each Module in the AAC

The capacitor voltage waveform is important since it can indicate the capacitor voltage balance that needs to be achieved for AAC. In Figure 3-7, the cell capacitor and its current and voltage in one module is shown. Let's choose the Heaviside step function H as follows:

$$H(x) = \begin{cases} 0 & x < 0 \\ 1 & x \geq 0 \end{cases} \quad (3-18)$$

Defining S as the switching function, the relation between the arm current and the capacitor current is shown in Fig.6, and can be written as:

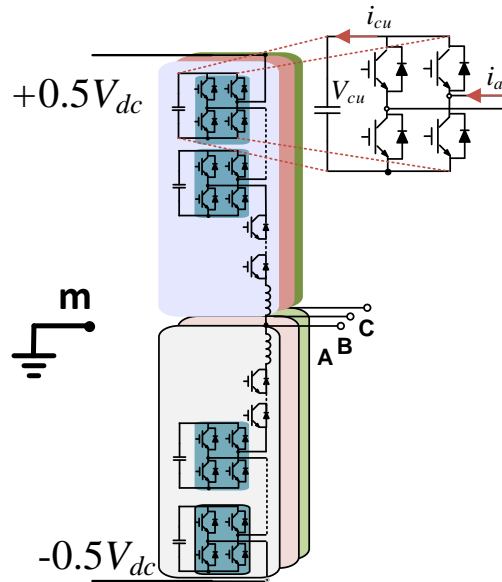


Figure 3- 7: Capacitor Voltage Analysis of the AAC

$$C \frac{dv_{cu}}{dt} = i_{cu} = H \times Si_a \quad (3-19)$$

Equation (3-19) can be expanded as:

$$\begin{aligned}
&= H(\sin \omega t) \times \left(\frac{1}{2} - \frac{M}{2} H(\sin \omega t) \sin \omega t \right) I_m \sin(\omega t - \varphi) \\
&= H(\sin \omega t) \times \left(\frac{1}{2} - \frac{M}{2} \sin \omega t \right) I_m \sin(\omega t - \varphi) \\
\Rightarrow C \frac{dv_{cu}}{dt} &= \frac{I_m}{2} H(\sin \omega t) (\sin(\omega t - \varphi) + M \cos(2\omega t - \varphi))
\end{aligned} \tag{3-20}$$

By taking the integral from (3-20) from $0 \leq \omega t < \pi$, the capacitor voltage ripple can be obtained by:

$$\Delta v_{cu} = \frac{I_m}{4C\omega} (M \sin(2\omega t - \varphi) - \cos(\omega t - \varphi)) \quad 0 \leq \omega t < \pi \tag{3-21}$$

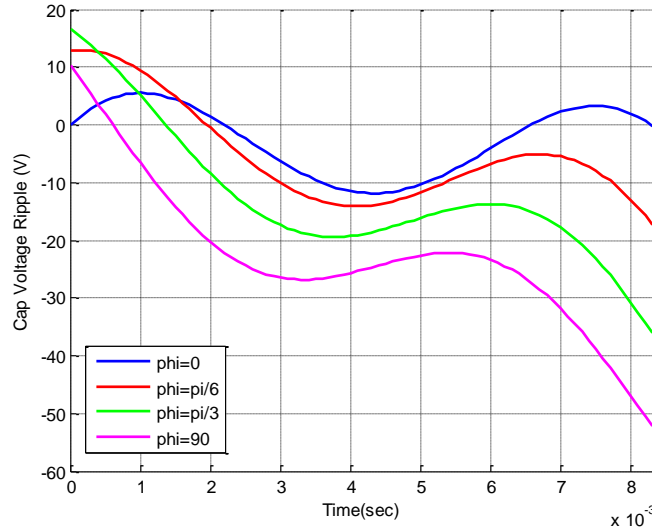


Figure 3- 8: Capacitor voltage ripple in different load power factors

Equation (3-21) finds the capacitor waveform in different load power factors in the half-line frequency. The capacitor voltage ripple is shown in Figure 3-8. It can be inferred that the capacitor voltage ripple in inductive loads needs to be balanced at the half-line frequency cycle. This can be achieved by introducing overlap time between director switches.

3.3.2 Capacitor Voltage Balance Control and Energy Balance Control

Schemes

From Figure 3-8, it can be deduced that the capacitor voltage of the AAC needs to be balanced during the half-of-line frequency. This can be achieved by introducing overlap time between the upper and lower arm DS. Introducing overlap time provides energy balance between each module and DC-side. During the overlap time, all the capacitors will be inserted and the output voltage will be about zero. In Figure 3-9, upper and lower arm voltage references are shown in the presence of the overlap time. This overlap time is controlled by the control system to provide appropriate overlap time between the upper and lower arms. Another function of the overlap time is to provide the zero current switching condition for the DS in order to minimize stress voltage due to turning off the switch in the inductive loads. The ZCS operation of the DS switch will be discussed later. The control schemes for the AAC will be explained in the following subsections:

3.3.3 Overlap Time Control of the AAC

The required overlap time between the upper arm and the lower arm can be achieved by the control scheme shown in Figure 3-10. In this control scheme, U_z , the output of the controller, shows the average voltage which is required to charge the capacitor to the reference value. The value of the overlap time can be found by solving following equation:

$$\begin{cases} V_m \sin(\omega t_{ov1}) = U_z \\ V_m \sin(\omega t_{ov2}) = -U_z \end{cases} \Rightarrow T_{OV} = t_{ov1} + t_{ov2} \quad (3-22)$$

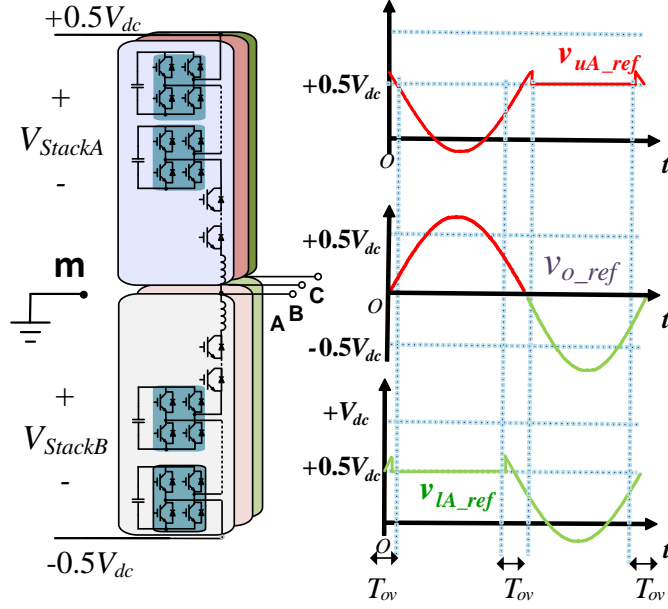


Figure 3- 9: The upper and lower arm references with Overlap

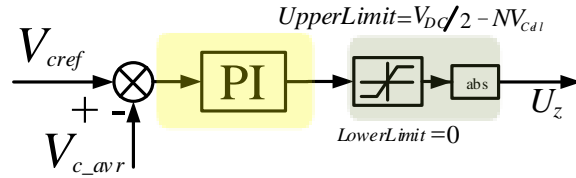


Figure 3- 10: The overlap time control between upper and lower arm DS

The overlap time can be achieved by directly introducing U_z into the step function, as shown in (3-23):

$$DS = H(\sin \omega t - U_z) \quad (3-23)$$

The analytical equation of the delay time can be carried out as follows:

$$\begin{cases} t_1 = \frac{1}{\omega} \arcsin \frac{U_z}{U_m} \\ t_2 = \frac{1}{\omega} \left(\pi - \arcsin \frac{U_z}{U_m} \right) \\ t_3 = \frac{1}{\omega} \left(\pi + \arcsin \frac{U_z}{U_m} \right) \\ t_4 = \frac{1}{\omega} \left(2\pi - \arcsin \frac{U_z}{U_m} \right) \end{cases} \Rightarrow T_{ov} = t_2 + t_3 \quad (3-24)$$

3.3.4 Individual Capacitor Voltage Control of the AAC

The proposed method in this work for the capacitor balance control takes the control schemes of reference [42] for the MMC and applies the same concept to the AAC first instead of using a sorting algorithm. The individual capacitor voltage control is shown in Figure 3-11. The controller used is PI in order to make the DC error as small as possible.

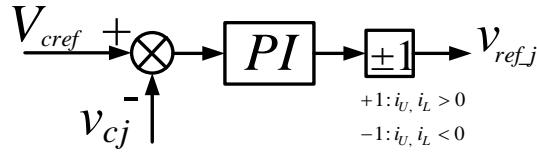


Figure 3- 11: Individual capacitor voltage control

The reference voltage from this controller will be added to the reference voltage of the upper and lower arm to make the final reference of the upper and lower stack voltages. The final reference can be obtained thusly:

$$\begin{aligned} v_{ref_up} &= v_{ref_j} + v_{ref_uA} \\ v_{ref_low} &= v_{ref_j} + v_{ref_lA} \end{aligned} \quad (3-25)$$

Where, v_{ref_uA} and v_{ref_lA} are given from the output current control.

3.2.5 Closed-loop Output Current control of the AAC

A similar control scheme for the MMC shown in Figure 3-6 can be utilized for the AAC. The output current measurements are transformed to the DQ axis current and the values are compared with the reference DQ axis current. The signals are then fed through the PI controller to the decoupling control to obtain the reference DQ voltages. The reference voltages in DQ are transformed in three-phase form and the references will be

added by the individual capacitor voltage balance to obtain the reference signals for the modulation. The overlap time control signal will be used prior to the modulation stage to form the desired reference signals for the upper and lower arm as shown in Figure 3-9. The carrier phase shift modulation technique is used to modulate reference waveforms to the PWM signals. In the next chapter, more details on the operations of the AAC and the overlap time will be discussed.

3.4 Conclusion

Chapter 3 describes the closed-loop control scheme, which is used to operate the modular multilevel converters. The implemented control method is based on average and individual capacitor voltage control, supplied with the Circulating Current Suppressing Control (CCSC), and using Proportional Quasi-Resonant (PQR) tuned for the most dominant circulating current harmonics (i.e. 2nd and 4th) order harmonics. Moreover, The Output current closed-loop control in DQ reference is provided for both the MMC and the AAC. AAC also requires overlap time control for its operation and energy balancing of the arm. The similar control method expanded for the AAC features individual capacitor voltage balance and overlap time control and the same output control method. In the next chapters, the closed-loop control discussed here will be used to provide further analysis of the modular multilevel converters in terms of design considerations and DC fault ride-through capability.

Chapter 4 Modular Multilevel Converters Design

Considerations

4.1 Introduction

This chapter describes the specific design considerations of modular multilevel converters. Since the size of the DC-link distributed capacitor in each cell is relatively high so as to reduce the voltage ripple over in each module, and there are usually a high number of power cells, the capacitor bank should be carefully designed to provide overall high reliability for the converter. The reliability-oriented design of the capacitor bank for the modular multilevel converter will be studied in this chapter. The comparison among different modulation techniques for the modular multilevel converter will be performed and, moreover, the design of the each module capacitor bank size and the arm inductor will be explained. The modular multilevel converter's switching frequency is usually selected to be low to avoid semiconductor losses and increase the efficiency of the converter. Furthermore, the equivalent switching frequency is interleaved by the number of cells and the equivalent switching will be higher than each power cell's switching frequency. To design the switching frequency, a balance should be achieved between the semiconductor losses and the capacitor voltage ripple in each cell since the switching frequency decreases as the capacitor voltage ripple increases. This chapter will present a

reliability-oriented switching frequency analysis for the modular multilevel converter with half-bridge power cells.

There is different design requirement for the Alternate Arm Converter (AAC) since the operation principles are totally different than those of the MMC. This chapter will discuss design of the number of the power cells, Director Switches, capacitor bank, and the arm inductor and will illustrate the Zero Current Switching operation of the AAC by selecting the appropriate size of the arm inductor. Finally, a comparison between the MMC and AAC in terms of the semiconductor losses and size will be performed in this chapter.

4.2 High Reliability Capacitor Bank Design for Modular Multilevel Converters

In Figure 4-1, the failure cause distribution over a power electronics converter component is shown [64]. As shown, capacitors are the most susceptible elements to failure among the various components. The number and ratio of the capacitors can be even higher when there is need for a high energy storage in the converter especially in modular structure converters. Capacitors play an important role in the operation of the converter. One of the MMC's issues is the large number of high-power capacitors that should be placed in each module, especially in high-power applications. This high number of capacitors can cause complexity and reliability problems and can restrict the lifetime of the converter [49]. Also, design of the capacitor bank and its effect on the other parameters design needs to be carefully studied. Several studies have addressed the

capacitor design issue for the MMC in the literature [65]. Dimensioning for the sub-module capacitor in the MMC is been presented in [66].

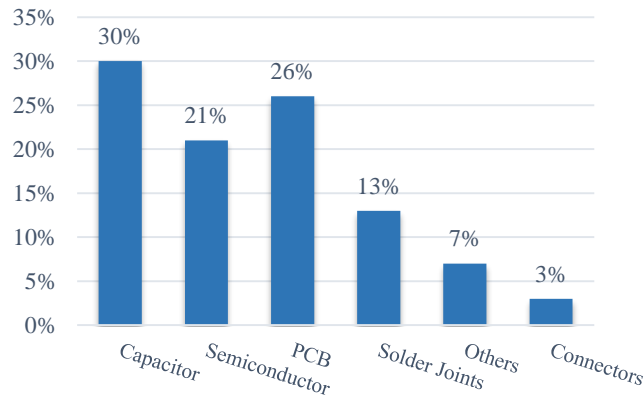


Figure 4- 1: Failure cause probability in power electronics systems

In [67], a more detailed study of the energy-storage needed for the MMC is performed. Although in the literature, the energy requirement for the MMC is discussed, the empirical design and reliability issues of these capacitor banks have never been addressed. To address the essence of reliability investigations, it is imperative to assess the reliability of the capacitor banks that are used in the modular topologies. A very good survey on the reliability of power electronics systems has been done in [68]. Reliability calculations of multilevel converters, especially for the ANPC and the medium voltage multilevel converters MMC, have been carried out in [69] and [70] respectively. In [71] and [72], the reliability oriented design for the high power DC-link capacitor and different aspects for the reliability of power electronics have been studied.

In this section, a reliability evaluation of the capacitor bank for the Modular Multilevel Converter (MMC) based on two common types of the DC-Link capacitors (i.e. Aluminum Electrolytic and Film) is carried out. Because of the high current ratio through the capacitor in the MMC, it becomes evident that the Film capacitor offers lower core

temperature increases than Aluminum Electrolytic Capacitors due to the low ESR and power loss. Case studies for the reliability function were carried out based on three sample designs using ALE and Film capacitors. The results show that the Film capacitor bank design offers the highest reliability and the longest life solution in each design. In order to improve lifetime and reliability of the Aluminum Electrolytic Capacitor, adding a Film Capacitor to the ALE capacitor bank is presented as a viable option. Reliability modeling of the capacitor bank for the Modular Multilevel Converters (MMC) based on the Markov State-Space Model (MSSM) was also carried out and then, using a case study, the reliability of the capacitor bank is evaluated considering both Aluminum Electrolytic (ALE) Capacitor Bank (CB) and Film CB designs. Furthermore, the comparison among the reliability modeling methods (i.e. Part-Count, Combinatorial and Markov Model) was carried out and shows that the Markov Model result is expected to be more accurate and to have more useful results compared to other reliability models, as it considers the fault tolerance and redundancy for the capacitor bank.

4.2.1 Capacitor Bank Size Design in Modular Multilevel Converter

Considering the average model and negligible voltage over each arm resistance as presented in Chapter 2, the equation for the reference of the upper arm and lower arm modulation signal can be obtained as follows:

$$V_{uA} = \frac{V_{dc}}{2} - m \frac{V_{dc}}{2} \sin \omega t \quad (4-1)$$

$$V_{lA} = \frac{V_{dc}}{2} + m \frac{V_{dc}}{2} \sin \omega t \quad (4-2)$$

The upper and lower arm currents have three-significant elements: DC current, phase current, and even order harmonics circulating current, shown as follows:

$$I_{uA} = \frac{I_{dc}}{3} + \frac{I_a}{2} \sin(\omega t + \varphi) + \sum_{h=2}^{2n} i_h \quad (4-3)$$

$$I_{lA} = \frac{I_{dc}}{3} - \frac{I_a}{2} \sin(\omega t + \varphi) + \sum_{h=2}^{2n} i_h \quad (4-4)$$

Where, $h=2n$ and $n=1 \dots \infty$. Considering the ESR for the practical floating DC-Link capacitor, the voltage across the sub-module capacitor bank in the upper arm is:

$$C \frac{d}{dt}(v_{cu} - ri_{cu}) = i_{cu} \quad (4-5)$$

Where, i_{cu} is the current through the capacitor bank and r is the ESR. The current through the capacitor can be obtained using the following equation:

$$i_{cu} = N_{uA} I_{uA} \quad (4-6)$$

By replacing the modulation signal equation for the upper arm, the current through the capacitor is calculated by:

$$i_{cu} = \left(\frac{1}{2} - \frac{m}{2} \sin \omega t \right) \left(\frac{I_{dc}}{3} + \frac{I_a}{2} \sin(\omega t + \varphi) + \sum_{h=2}^{2n} i_h \right) \quad (4-7)$$

And the voltage across the capacitor bank can be extracted by solving the differential equation:

$$v_{cu} = v_{cu}(0) + \frac{1}{C\omega} \int i_{cu} d\omega t + ri_{cu} \quad (4-8)$$

$$v_{cu} = v_{cu}(0) + \frac{1}{C\omega} \int \left(\frac{1}{2} - \frac{m}{2} \sin \omega t \right) \left(\frac{I_{dc}}{3} + \frac{I_a}{2} \sin(\omega t + \varphi) + \sum_{h=2}^{2n} i_h \right) d\omega t + r \left(\frac{1}{2} - \frac{m}{2} \sin \omega t \right) \left(\frac{I_{dc}}{3} + \frac{I_a}{2} \sin(\omega t + \varphi) + \sum_{h=2}^{2n} i_h \right) \quad (4-9)$$

The same procedure can be used to determine the voltage over the lower arm capacitor bank. The above equations demonstrate that the voltage over the capacitor bank is related to the load current, power factor of the load, modulation index, even harmonics which are circulating through the MMC, and the output frequency.

From equation (4-9), the problem with using MMC for low output frequency applications such as the three-phase motor drive can be observed. The voltage equation over the capacitor bank demonstrates that existence of the ESR not only means power loss and decreasing efficiency but also means increased ripple over the voltage of the capacitor bank, which can cause reliability issues within the capacitor bank.

The capacitor size is specified by a maximum allowed peak-to-peak voltage variation over the module. The equation for the capacitor size is given by [48], [73], and [74]:

$$C_{SM} = \frac{P_3 \cdot V_{dc}}{3\omega \cdot N \cdot V_c \cdot \Delta V_c \cdot V_{pa} \cdot \cos(\varphi)} \sqrt{\left(1 - \frac{\left(\frac{V_{pa}}{V_{dc}}\right)^2 \cdot \cos^2(\varphi)}{4}\right)^3} \quad (4-10)$$

4.2.2 Simulation Analysis to Evaluate Reliability of CB

A simulation analysis using Simulink/MATLAB is presented in this section. The circuit parameters are considered in the simulation are given in Table 4-1. To study the effect of ESR on each module capacitor, voltage 200mΩ ESR is assumed in the simulation based on the high voltage and low capacitance ratio aluminum electrolytic capacitors [75] in order to better understand the ESR effect. The result is presented in Figure 4-2. As shown in the equation (4-9), ESR causes AC ripple over the voltage of the

capacitor in MMC. So, as the Film capacitor has a low ESR, its use is will be preferred so as to decrease the ripple.

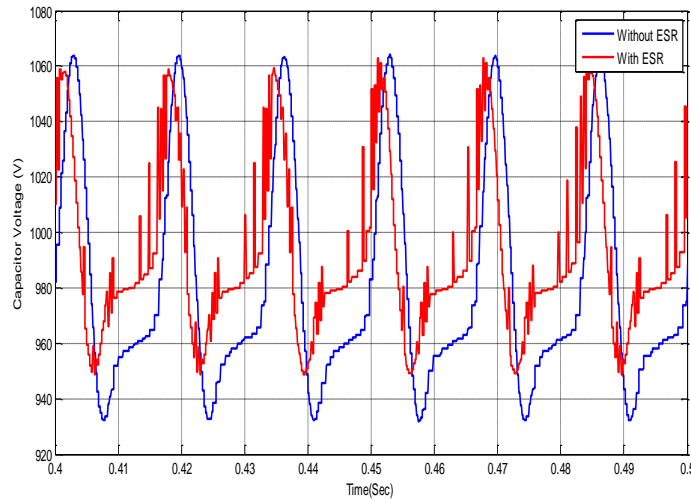


Figure 4- 2: The effect of ESR on each module capacitor voltage

Table 4- 1: Circuit Parameters value

Circuit Parameters	Value
Output Frequency	60 Hz
Switching Frequency	2100 Hz
L	1.2 mH
C	3400 μ F
Ri	0.04 Ω
Vdc	3kV
Modulation Index m	0.9
Load_L	9mH
Load_R	6 Ω
P	500kW
Voltage Over each Module	1kV

4.2.3 Case Study for Capacitor Bank Design

In this section, design of the capacitor bank is carried out based on three case studies for the size of the capacitor for each module, . For each case, three sample designs using Aluminum Electrolytic and Film capacitors are presented. A performance comparison of these two main types of the capacitor for high power applications is

presented in [71]. To evaluate the design characteristics of the capacitor bank using Aluminum Electrolytic and Film capacitors and look into the pros and cons of each, cases have been chosen to cover instances where the current ripple through the capacitor is from low to high, respectively.

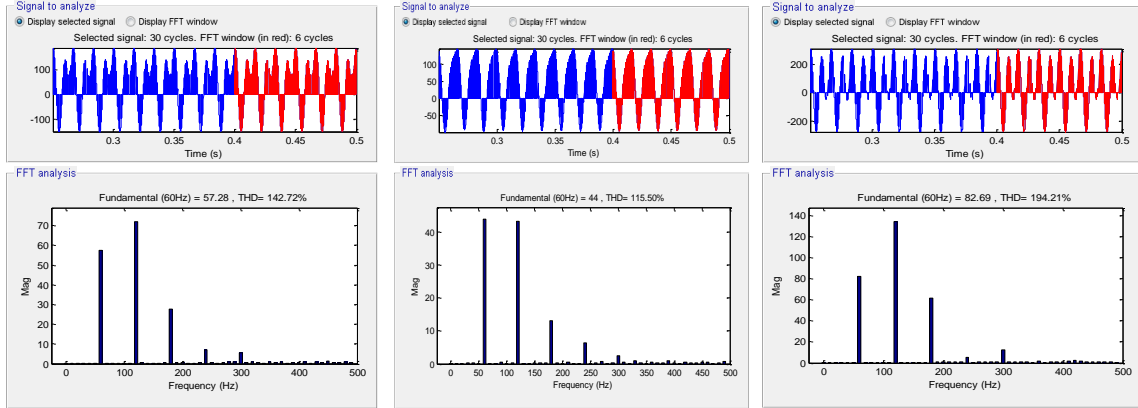
Table 4- 2: Three Capacitor bank Design Case Studies for different voltage and current ripple

Case	C (μF)	Voltage Ripple	Current Ripple
Case1	3400	Normal	Normal
Case2	6000	Low	Low
Case3	2500	High	High

Each case is shown in Table 4-2. These values in each case follow the equation (4-10). The current through the capacitor and FFT analysis for the capacitor current in each of the three cases are shown in Figure 4-3 a, b and c.

4.2.3.1 Aluminum Electrolytic Capacitor

By choosing 1700 μF (500 V) Type 450C 105 °C Ultra-Ripple, Long-life, Inverter Grade and Radial Leaded [75], the design for case 1 was made using an ALE capacitor. Because each module's voltage is 1kV where the reserved voltage factor is defined as 1.5, and considering the nominal current through the capacitor, it is determined that three ALE capacitors are needed in series in each parallel branch. Also, because there is nominal current passing through each capacitor, the capacitor bank needs six parallel branches.



(a) Irms=80.5A (b) Irms=54A (c) Irms=145A

Figure 4- 3: Current waveform through Capacitor and FFT analysis for each three-Case a) Case 1, b) Case 2 and c) Case 3

4.2.3.2 Film Capacitor

By growing the film capacitors' technology, they can be made to offer high operating current, low ESR, and high voltage; however, the capacitance value still is much lower than it is for Aluminum Electrolytic capacitors. In order to design the capacitor bank to provide the value specified for case one, two different film capacitors are selected. First is the 1500 μF , 800 V, Type 947C Polypropylene, Film DC-Link Capacitor from Cornell Dubilier [76], [77] Secondly, the 1040 μF , 1500 V, E50 Electronicon Film [78] capacitor is considered. The design samples illustrations for case one using CDE Aluminum, CDE Film, and Electronicon Film capacitor are shown in Figure 4-4. The design procedure for the other cases is presented following. In cases two and three, the number of series capacitors are same as in case one. However, in case two C is equal to 6 mF, and for the ALE capacitor three parallel branches are needed, for CDE Film eight are needed and for Electronicon Film five parallel branches are needed. In case three, where C is 2500 μF , for CDE Film four and for Electronicon Film two parallel branches are required. In case three, the Aluminum Electrolytic Capacitor is

selected from KEMET, 330 μF and 500 V [79], so it needs 36 parallel branch to overcome the high ripple current.

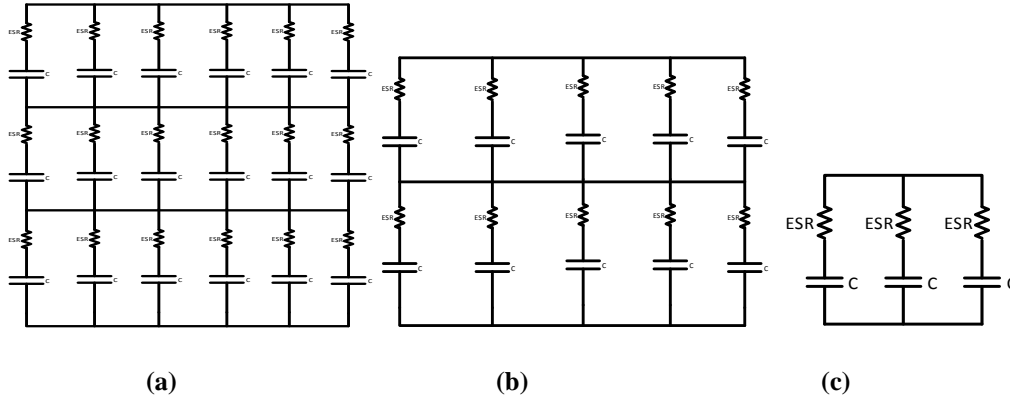


Figure 4- 4: Three sample designs illustration for capacitor bank in case 1 $C=3400\mu\text{F}$ (a) CDE ALE Capacitor Bank Design, (b) CDE Film Capacitor Bank Design, (c) Elecronicon Film Capacitor Bank Design

4.2.4 Power Loss, Hot Spot, Failure Rate and Reliability Calculations of the Capacitor Bank

In order to calculate power loss and hot spots in the capacitor bank, it is assumed that ESR is constant over frequency. The equations of the power loss and hot spot temperature based on the true RMS value, ESR, and thermal resistance of the capacitor bank are shown as follows:

$$P_{Loss} = ESR \times I_{rms}^2 \quad (4-11)$$

$$T_h = T_a + P_{Loss} \times R_{th} \quad (4-12)$$

T_a is ambient temperature, which is assumed to be 45°C . Generally, the failure rate of the capacitor can be estimated by using reliability predication model handbooks such as [80] and [81]. However, based on the applied technology, many manufacturers provide their own failure rate calculation method for their product. As an example, the failure rate equation for CDE Aluminum Electrolytic Capacitors is given in [82].

The reliability model for the series and parallel networks of the capacitor bank shown in Figure 4-5 based on a combinatorial reliability model [68] can be calculated by:

$$R(t) = \left[1 - \left[(1 - e^{-\lambda_1 t})(1 - e^{-\lambda_2 t}) \dots (1 - e^{-\lambda_M t}) \right] \right] \times \dots \times \left[1 - \left[(1 - e^{-\lambda_{N1} t})(1 - e^{-\lambda_{N2} t}) \dots (1 - e^{-\lambda_{NM} t}) \right] \right] \quad (4-13)$$

Based on the defined three case studies, the power loss, hot spot temperature, and the failure rate (from manufacturer model) for each design are calculated and shown in Table 4-3.

Table 4- 3: Failure Rate Evaluation For Each Design

	Power Loss W		
	Case1	Case2	Case3
ALE	10.314	6.383	5.145
CDE Film	0.466	0.02	0.555
Electronicon Film	0.12	0.02	0.123
	Hot Spot Temperature °C		
	Case1	Case2	Case3
ALE	75.94°C	64.15°C	60.44°C
CDE Film	46.44°C	45.06°C	46.66°C
Electronicon Film	45.13°C	45.02°C	45.135°C
	Failure rate (FIT)		
	Case1	Case2	Case3
ALE	17.65	9	8
CDE Film	1.8	1	2
Electronicon Film	0.2	0.2	0.2

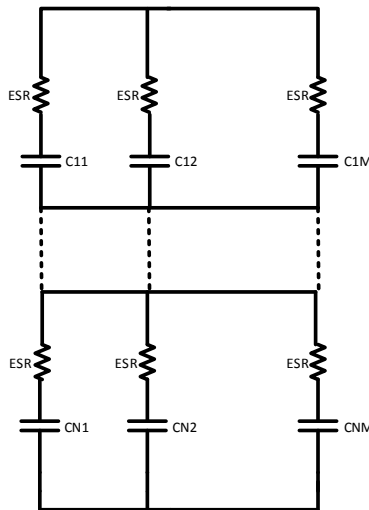


Figure 4- 5: N series and M parallel capacitor bank

4.2.5 Comparison Among Reliability of Each Case

Due to the necessity of calculating the reliability curve of each sample design in each case, equation (4-13) is used for each design. Then, by replacing calculated failure rates of each design, which are given in Table III, the reliability function can be achieved. The reliability curves for each case are shown in Figure 4-6 a, b and c.

As Figure 4-6 shows, in each case, the reliability of the film capacitor bank designs versus time are higher than that of the ALE capacitor bank.

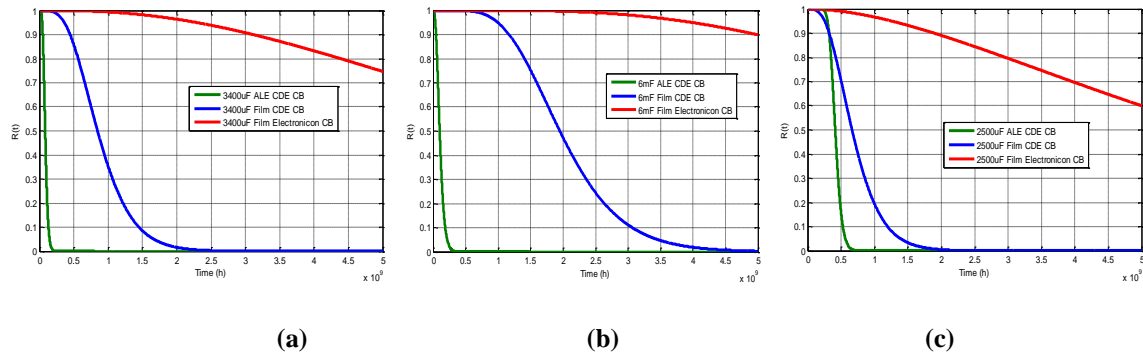


Figure 4- 6: Reliability function comparison among three different cases a) Case 1 b) Case 2 and c) Case 3

4.2.6 Difference Between Reliability of the Internally Parallel Connected and Non-Connected Capacitor Bank Considering Failure Mode Of the Capacitor

Failure modes and failure mechanisms of the capacitors used in the DC-Link application are given in [71]. Considering open and short circuit failure modes of the capacitors, two different approaches for the design of the capacitor bank can be proposed. The first approach is based on what has been discussed in the previous section, and which is called the internally parallel connected capacitor bank. This is used when the dominant failure mode of the capacitor is open circuit. The second approach is just to use no internally connected parallel caps; this is used for the design when the dominant failure

mode of the capacitor is short circuit. These two approaches are shown in Figure 4-7 based on the CDE Film design in case study 1.

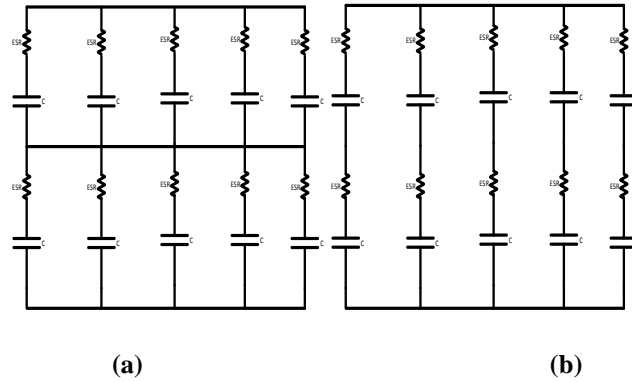


Figure 4- 7: Two- Design of CB a) Internally Parallel Connected for open circuit dominant failure mode b) not internally connected for the short circuit dominant failure mode

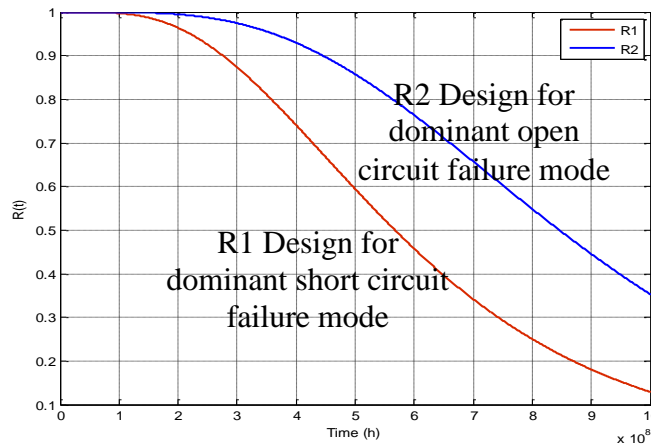


Figure 4- 8: Reliability comparison for two- design approach of the Capacitor Bank (CB) R1 with dominant short and R2 with dominant open failure mode

Based on the combinatorial reliability modeling, the reliability model of the design with N series and M parallel capacitor bank not internally parallel connected as in Figure 4-7 (b) is as follows:

$$R(t) = \left[1 - \left[(1 - e^{-\lambda_{11}t} e^{-\lambda_{21}t} \dots e^{-\lambda_{N1}t}) \dots (1 - e^{-\lambda_{1M}t} e^{-\lambda_{2M}t} \dots e^{-\lambda_{NM}t}) \right] \right] \quad (4-14)$$

In Figure 4-8, the reliability comparison between two approaches is carried out and results show that the design of the capacitor bank as shown in Figure 4-7 (a) for the dominant open failure mode of the capacitor has superior reliability and lifetime.

In the previous section, since the dominant failure mode of the ALE and Film capacitors is open circuit failure mode, the design comparison has been done based on the open circuit dominant failure mode. However, as is shown in Figure 4-9 to ensure the open mode failure mode of the capacitor, internal fuses can be used.

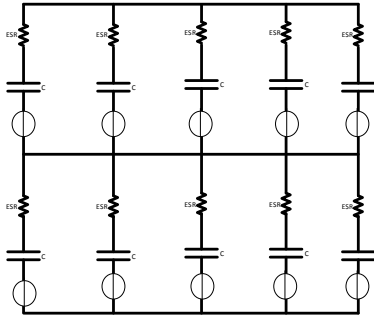


Figure 4- 9: Open circuit failure mode with adding fuses to the each capacitor branch

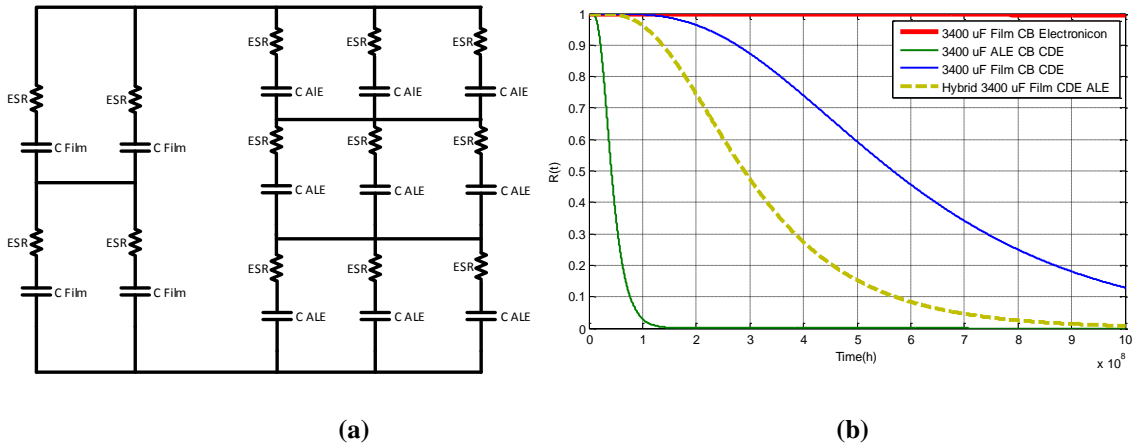


Figure 4- 10: (a) Hybrid Film and ALE capacitor bank for case 1, (b) Reliability Comparison among the Hybrid Film and ALE capacitor bank in case 1

4.2.7 Enhancement of the Reliability of the ALE Capacitor Bank by Adding Film Capacitor

For the DC-Link capacitor bank, it is possible to use the ALE and Film capacitor together to enhance the reliability of the Aluminum Electrolytic Capacitor. The sample design for case one is shown in Figure 4-10 (a).

The reliability curve of the hybrid DC-link capacitor is shown in Figure 4-10 (b). As can be seen in this figure, the reliability of the ALE Capacitor is improved by adding a film capacitor. Due to unbalanced current sharing between ALE and Film Capacitors, the ability of the film capacitor to handle higher current than the ALE capacitor means that it can be used to decrease the power loss and temperature rising and also improve reliability issues. The proposed structure can be designed for higher energy density than the pure film capacitor and with higher reliability and longer life than a pure ALE capacitor bank.

4.3 Reliability Modeling of the Capacitor Bank for MMC Using Markov State-Space Model

One of the drawbacks to the reliability modeling of systems with a high number of components is that in those systems, a high number of simulations or calculations should be executed in order to find the system's characteristics in each state. One solution to reduce the time and complexity of simulations based on real time models, may be using the mathematical model of the system. In this study, to estimate the voltage and current of one cell after the failure of one of the capacitors in the capacitor bank, the converter mathematical modeling approach is used.

A sub-module of the MMC is modeled as a current source converter in order to decouple the operation of one module with the operation of the whole converter. Based on the switching model obtained in Chapter 2, the mathematical equations describing the dynamic behaviors of the N-modules MMC converter is given by:

$$\begin{aligned}
\frac{di_{p-u}}{dt} &= \frac{1}{L_1} \left[E_p - \sum_{i=1}^N (S_i \cdot V_{C_i}) - R_1 i_p - V_{a-u} \right] & \text{where } u = a, b, \text{ or } c \\
\frac{di_{n-u}}{dt} &= \frac{1}{L_1} \left[E_n - \sum_{i=N+1}^{2N} (S_i \cdot V_{C_i}) - R_1 i_n + V_{a-u} \right] \\
\frac{dV_{C_i}}{dt} &= \frac{1}{C} (i_{p-u} \cdot S_i) & i = 1, \dots, N \\
\frac{dV_{C_i}}{dt} &= \frac{1}{C} (i_{n-u} \cdot S_i) & i = N + 1, \dots, 2N \\
\frac{d}{dt} C_{i-upper}^{-1} &= 0 \\
\frac{d}{dt} C_{i-lower}^{-1} &= 0 \\
y_1 &= i_{p-u} \\
y_2 &= i_{n-u}
\end{aligned} \tag{4-15}$$

Where i_{p-u} , i_{n-u} , S_i , V_{C_i} and V_{a-u} are upper/lower arm currents, gating signal of upper gate, capacitor voltage of i -th cell, and phase- u voltage, respectively. The gating signal of the lower gate is the complementary of S_i .

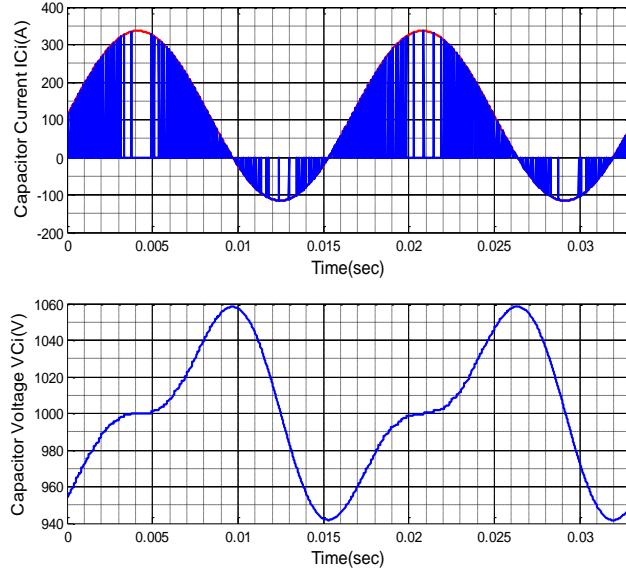


Figure 4- 11: The current and voltage through the capacitor bank of one module

The simulation result through the modeling of the MMC with the specifications set forth above is shown in Figure 4-11. Since the objective is designing the capacitor

bank for each module, the voltage and current through each cells is a concern. The rms current passes through the capacitor, is shown in Figure 4-11, is 81 A. This will be used to design the capacitor bank in the next section in order to determine the number of parallel branches for the capacitor bank.

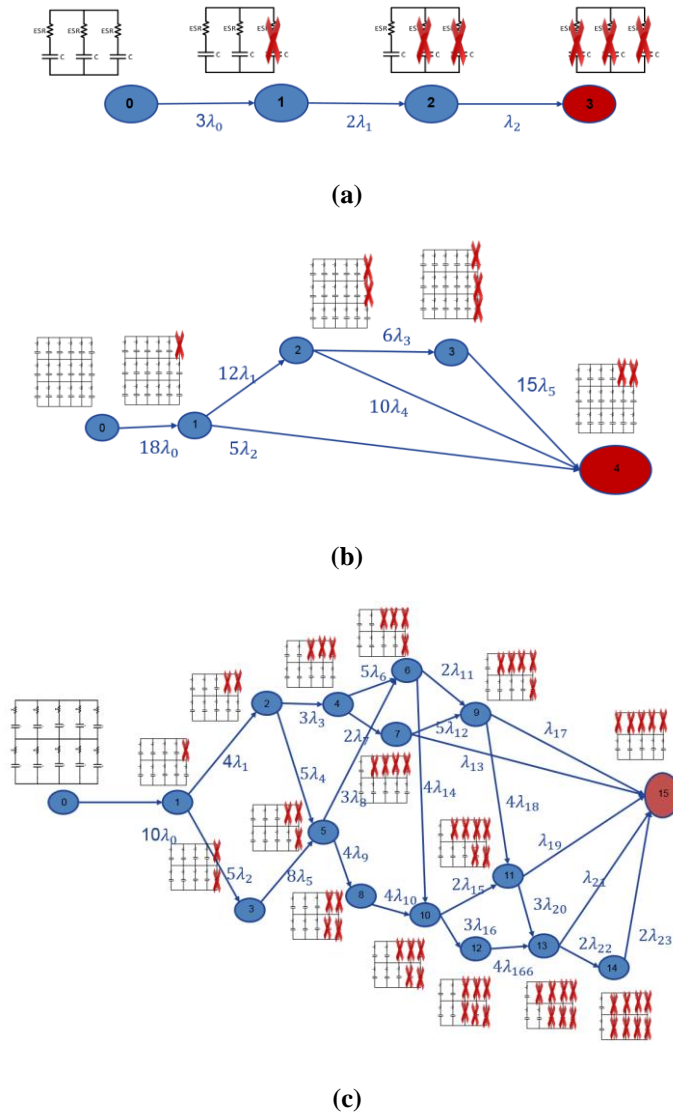


Figure 4- 12: Markov State-Space Model of the three different design of capacitor bank, (a) Film Electronic (b) CDE ALE (c) CDE Film

4.3.1 Markov State-Space Model

The Markov model is a graphical representation of the system's corresponding states after a unique sequence of component failures and transitions among these states [68]. The basics of the Markov state-space model can be found in reliability modeling text books [83] and [84].

The capacitor bank of 3400 μF is designed using three different types of capacitors. The Aluminum Electrolytic capacitor of 1700 μF (500 V) Type 450C 105 °C Ultra-Ripple, Long-life, Inverter Grade, and Radial Leaded [75] has been chosen for the ALE type capacitor bank. For the Film type capacitor bank two different film capacitors are selected. First, the 1500 μF , 800 V, Type 947C Polypropylene, Film DC-Link Capacitors from Cornell Dubilier [76], [77] and secondly the 1040 μF , 1500 V, E50 Electronicon Film [78] capacitor are considered. By using the structure of parallel internally connected capacitors within the capacitor bank, the CDE ALE design leads to six parallel branches with three series capacitors in each leg. The CDE film design has five parallel branches with two series individual capacitors and the Electronicon will have three parallel capacitors. Markov state-space modeling has been done for each of the three capacitor bank designs. In Figure 4-12, reliability modeling based on the Markov state space model is shown for each of the three different capacitor banks.

In Figure 4-12, the zero state represents system operation without failure, and the failure rate to the next system is the failure rate of the component in the corresponding state. The system failure state called the absorbing state is determined when the current through the capacitors of the capacitor bank goes higher than the rated current. Knowing this, it can be deduced that the Film capacitor can last longer after a failure of one

capacitor within the CB due to its ability to handle more AC current. To calculate the failure rate in each state, the failure model of the capacitors are required. The failure rate of the Electronicon Film capacitor and Cornell Dubilier Capacitors are given by [76] and [82] respectively. The matrix expression of the Markov State-Space equation for Figure 4-12 (a) can be written as:

$$\left\{ \begin{array}{l} \frac{d}{dt} \begin{bmatrix} P_0 \\ P_1 \\ P_2 \\ P_3 \end{bmatrix} = \begin{bmatrix} -3\lambda_0 & 0 & 0 & 0 \\ 3\lambda_0 & -2\lambda_1 & 0 & 0 \\ 0 & 2\lambda_1 & -\lambda_2 & 0 \\ 0 & 0 & \lambda_2 & 0 \end{bmatrix} \begin{bmatrix} P_0 \\ P_1 \\ P_2 \\ P_3 \end{bmatrix} \\ R(t) = [1 \quad 1 \quad 1 \quad 0] \begin{bmatrix} P_0 \\ P_1 \\ P_2 \\ P_3 \end{bmatrix} \end{array} \right. \quad (4-16)$$

Where, P_0 , P_1 , P_2 and P_3 are the failure probability of each state, λ_0 , λ_1 , λ_2 are the failure rate of the single component prior the next failure in each state, and $R(t)$ is the reliability of the capacitor bank based on the Markov model.

Also, for Figure 4-12 (b), the Markov model is applied as shown by (4-17) in the matrix form:

$$\left\{ \begin{array}{l} \frac{d}{dt} \begin{bmatrix} P_0 \\ P_1 \\ P_2 \\ P_3 \\ P_4 \end{bmatrix} = \begin{bmatrix} -18\lambda_0 & 0 & 0 & 0 & 0 \\ 18\lambda_0 & -12\lambda_1 - 5\lambda_2 & 0 & 0 & 0 \\ 0 & 12\lambda_1 & -6\lambda_3 - 10\lambda_4 & 0 & 0 \\ 0 & 0 & 6\lambda_3 & -15\lambda_5 & 0 \\ 0 & 5\lambda_2 & 10\lambda_4 & 15\lambda_5 & 0 \end{bmatrix} \begin{bmatrix} P_0 \\ P_1 \\ P_2 \\ P_3 \\ P_4 \end{bmatrix} \\ R = [1 \quad 1 \quad 1 \quad 1 \quad 0] \begin{bmatrix} P_0 \\ P_1 \\ P_2 \\ P_3 \\ P_4 \end{bmatrix} \end{array} \right. \quad (4-17)$$

The P states parameters represent the failure probability, the λ parameters show the failure rate of the corresponding states and components, and $R(t)$ is the reliability of

the capacitor bank based on the Markov model. For Figure 4-12 (c), the same procedure can be used to derive the state-space model. By calculating the failure rate in each state for each of the three cases, the reliability model of the capacitor bank using the Markov State-Space Model is achieved.

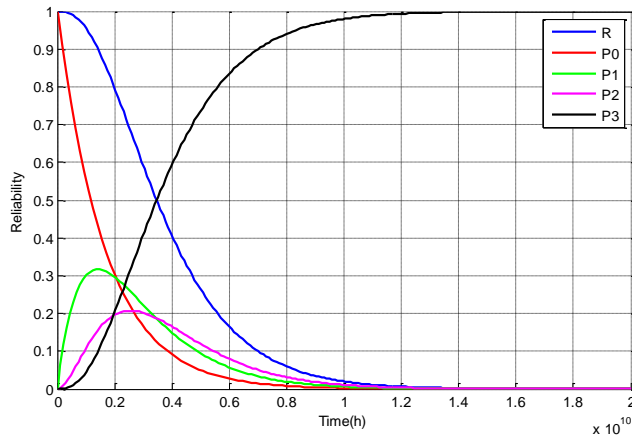


Figure 4- 13: The Markov reliability model of the capacitor bank which is modeled in Figure 4-12 (a)

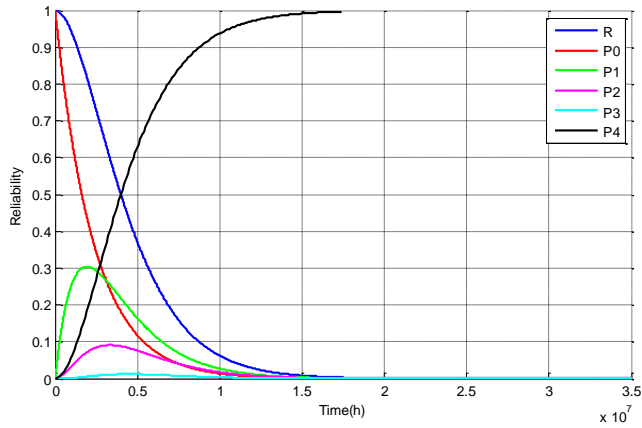


Figure 4- 14: The Markov reliability model of the capacitor bank which is modeled in Figure 4-12 (b)

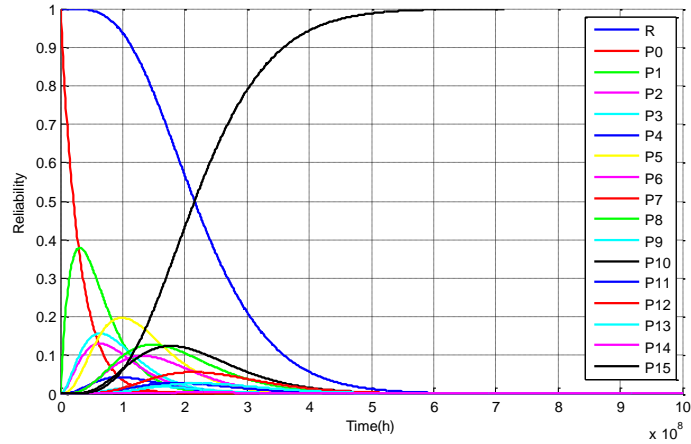


Figure 4- 15: The Markov reliability model of the capacitor bank which is modeled in Figure 4-12 (c)
 In Figure 4-13, the reliability model of case a, which is shown in Figure 4-12 (a), is illustrated. The Markov-reliability model for case b and c in Figure 4-12 is extracted in the same manner as case a. In Figure 4-14 and 4-15, the reliability model of the corresponding capacitor bank is depicted. As can be seen in these figures, the reliability of each state is displayed separately in order to understand the transition that occurs from the fault free state to the absorbing state.

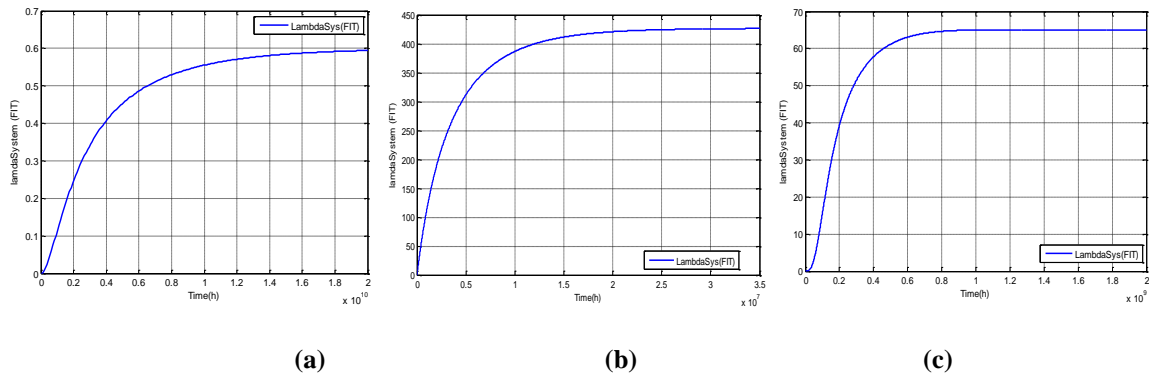


Figure 4- 16: The failure rate of the system extracted from Markov Model, (a) Film Electronicon, (b) ALE CDE and (c) Film CDE

The last state in the reliability model shows the probability of the failure of the entire system, which can be expressed as the reliability of the system. For calculation of the

reliability of a system, it is necessary to simulate and analyze the system in each state to update the failure rate of the system in each state.

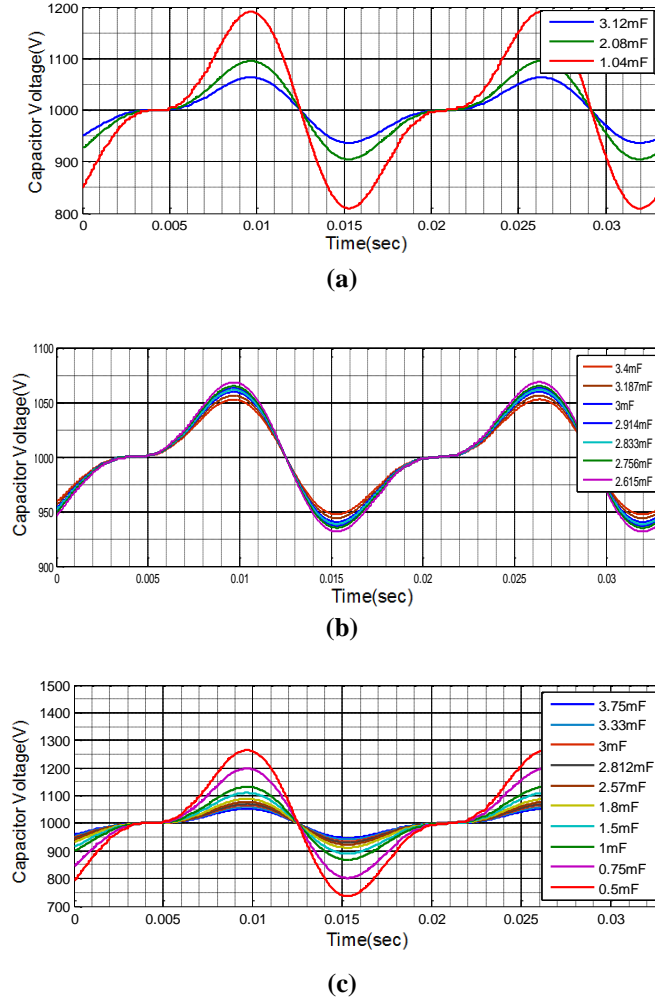


Figure 4- 17: The voltage variation over the capacitor bank in each module (a) for Film Electronic design Figure 4-12 (a). (b) For ALE CDE design Figure 4-12 (b). and (c) for Film CDE design Figure 4-12 (c)

In the Markov state-space model, the failure rate of the system is modeled as (4-18):

$$\lambda_{sys}(t) = -\frac{1}{R(t)} \cdot \frac{dR(t)}{dt} = \frac{P_N(t)}{1 - P_N(t)} \quad (4-18)$$

Where, $P_N(t)$ is the possibility of failure of the last state; this can be determined by using the Markov Model. The failure-rate of the system using the Markov model by employing the equation (4-18) can be obtained in each model. In, Figure 4-16 a, b and c, the failure rate of each capacitor bank is obtained.

As can be seen, the failure rate of the system is the function of time, and in the beginning, the transient of the failure rate is zero, which means that the system failure rate after the infant mortality stage of the bathtub curve is too low. As time passes, the failure rate reaches its final value depending on a time constant. which is related to the failure rate of the system in each state of the Markov model. The current source modeling of one module, as mentioned, would decouple the module from the whole converter's operation operation after a failure.

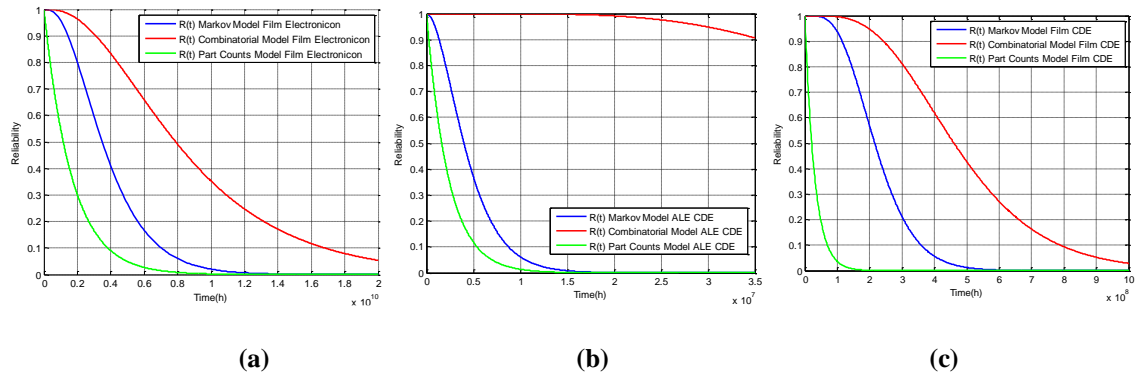


Figure 4- 18: The different reliability modeling of the capacitor bank using part counts, combinatorial and Markov model (a) for Film Electronic design Figure 4-12.a (b) For ALE CDE design Figure 4-12.b and (c) for Film CDE design Figure 4-12.c

The voltage through the module in each state of the Markov model is shown in Figure 4-17 a. b. and c. for each case. From the results, it can be seen that the film capacitor can last longer than the ALE capacitor due to the handling of high current ripple rate and low ESR. Since the rated RMS current and voltage ripple are higher for

the film capacitors, in Figure 4-17 a. and c., there are more transient states to the absorbing state after a failure of one of the capacitors in the capacitor bank. So, using Film capacitors will mean long life and high reliability in the capacitor bank design in power electronics systems, especially for the MMC.

4.3.2 Comparison with Three-Reliability Models

This section presents a comprehensive exploration of and comparison among the results corresponding to the different reliability assessment models of the three reliability modeling methods mentioned in the previous section, which include the part-count, combinatorial, and Markov model. In the reliability modeling techniques, the part-count model provides a simple modeling approach in which the failure of one element causes the failure of the whole system. This modeling approach gives conservative results in spite of having simple principles. On the other hand, the combinatorial model leads to optimistic reliability modeling and allows for the system to work after the failure of its components. Under this definition, the combinatorial model is used to model the reliability of redundancy systems. The third modeling method is based on the Markov state-space model and can model the failure transient of the system as well as the fault tolerance capability of the system. In Fig. 10.a.b. and c, the comparison among the different reliability models for each case is shown.

As can be interpreted from the results, modeling of the ALE capacitor bank with the combinatorial model leads to a very optimistic reliability estimation of the CB, which realistically hold true. By comparison, the Markov reliability model leads to results that seems to be closer to the true reliability model of the system in real situations.

4.3.3 Conclusion

In this chapter, the reliability of the capacitor bank for Modular Multilevel Converters (MMC) is modeled using the Markov State-Space Model. The MMC is modeled mathematically in order to be used for reliability calculations in different states of the Markov model. Based on a sample case study, the reliability of the capacitor bank for three different sample designs of the capacitor bank using real capacitors, Film and Aluminum Electrolytic types, is evaluated using the Markov Model. For each design, Markov reliability modeling is achieved and based on that, the reliability of each system is obtained. By using the Markov model, the failure rate of the system for each case is estimated and finally, a comparison among the results of the reliability modeling of the system is performed by using the aforementioned three different reliability modeling techniques (i.e. part-count, combinatorial, and Markov model). The results shows= that reliability modeling using the Markov model tends to be closeest to the realistic reliability model of the system.

4.4 Modulation Techniques' Influence on the Cap Voltage and Arm Current Ripple

In this section, the modulation technique's effects on the stress over the sub module capacitor and the IGBT will be discussed. The evaluation is done based on the harmonic analysis over the arm quantities. For the phase deposition methods, the carrier rotation technique [85], [86] and [87] is utilized. To evaluate the effect of adopting each modulation technique, the case study converter parameters shown in table I are used for the simulation.

Table 4- 4: MMC Parameter values for modulation technique evaluation

Output Frequency	60 Hz
Switching Frequency	540 Hz
L	3.7 mH
C	4000 μ F
Ri	0.004 Ω
Modulation Index m	0.9
Output Voltage	6kV L-L
P	3MW
Voltage Over each Module	1kV
DC Bus Voltage	10 kV
Number of Module per arm	10

The Total Harmonic Distortion (THD) of the upper arm current, voltage and current of the capacitor, output line to line voltage, and current is shown in Table. II.

Table 4- 5: Stress Analysis in Different Modulation Technique

Modulation Technique	IuA THD	Vcu THD	Voll THD	Io THD	Icap THD
PD	21.97 %	76.22%	6.24 %	2.74 %	193.63%
POD	17.80 %	73.98%	7.73 %	3.57 %	197.56%
APOD	16.71%	70.33%	7.84%	3.36%	188.45%
PSC	<u>13.44%</u>	<u>56.38%</u>	7.22%	<u>0.62 %</u>	<u>187.30%</u>

As shown in the table above, the simulation result shows that the Phase-Shifted Carrier Modulation method has less harmonic distortion, which is desirable. So, the Phase-Shifted Carrier modulation technique is chosen for the MMC.

4.5 Design of the L and C with Circulating Current Controller

Design of the arm inductor and the size of the sub-module capacitor should be performed taking into consideration that the circulating current suppressing controller is utilized. By considering the CCSC effect, the second order harmonic through the upper arm current would be negligible, and by assuming that the direct modulation scheme is used, the instantaneous power of the upper arm cells can be written as:

$$p_c = v_c i_c = v_{sm} i_{Ua} \quad (4-19)$$

And by replacing the voltage over the upper arm and the upper arm current, the instantaneous power of the upper arm can be written as:

$$p_c = \frac{V_{dc}}{2} (1 - M \sin \omega t) \left[\frac{1}{3} I_{dc} + \frac{\sqrt{2}}{2} I_a \sin(\omega t - \varphi) \right] \quad (4-20)$$

By assuming that the peak to peak voltage ripple over the capacitor bank is $2\Delta V$, the maximum energy stored the capacitor will become as follows:

$$\Delta W_{\max} = \frac{1}{2} C (V_{dc} + \Delta V)^2 - \frac{1}{2} C (V_{dc} - \Delta V)^2 = 2C V_d \Delta V \quad (4-21)$$

The equation above should be equal to the maximum energy of the upper arm, which can found by the integral of equation 20. From this equation, the equation for the size of the capacitor can be found:

$$C = \frac{\int_{t_1}^{t_2} p_c dt}{2V_d \Delta V} \approx \frac{P}{3\omega_1 N M V_d \Delta V \cos \varphi} \sqrt{\left(1 - \left(\frac{M \cos \varphi}{2}\right)^2\right)^3} \quad (4-22)$$

By neglecting the second order harmonic current, the voltage across the inductor becomes as follows [46]:

$$V_{cir} = \frac{N}{2C} \left(\frac{3M}{8\omega} \sqrt{2} I_a \cos(2\omega t + \varphi) - \frac{M^2}{6\omega} I_{dc} \cos(2\omega t) \right) \quad (4-23)$$

The maximum switching frequency circulating current can be written as follows:

$$I_{PP_Max} = \frac{V_{cir}}{2L_{arm}} T_s \quad (4-24)$$

So, from equation (4-23), the arm inductor size necessary to limit the switching frequency circulating current can be obtained by [44]:

$$L_{arm} = \frac{NM}{8I_{PP_Max}\omega C f_{sw}} \left(\sqrt{\frac{9}{16}I_a^2 + \frac{M^2}{9\omega}I_{dc}^2 - \frac{1}{2}MI_a I_{dc}} \right) \quad (4-25)$$

There are three main criteria for the arm inductor, which are as follows: (i) selection of the arm inductor to limit the DC side fault current [88], (ii) the inductor size should be selected such that it is prevented from the second order harmonic resonant frequency [46], (iii) The inductor size should be chosen to limit the circulating current as it is given in equation (4-25). The size of the inductor would be the maximum of size as determined from these items.

4.6 Reliability-Oriented Switching Frequency Analysis for the Modular Multilevel Converter (MMC)

4.6.1 Harmonic Components Analysis of MMC for Low Switching Frequency Applications

Modular Multilevel Converters are preferably operated at low switching frequency in order to reduce switching loss of the converter. However, switching frequency can impact the circulating current magnitude though the arm and can cause the high distortion of the arm current. The switching frequency circulating current components of the upper arm can be written as:

$$i_{Va}(t) = I_{dc} + \frac{\sqrt{2}}{2} I_a \sin(\omega t + \varphi) + I_{sw} \sin(\omega_p t + \theta) \quad (4-26)$$

$$\omega_p = \omega_s \pm \omega$$

Where ω_p is the switching frequency component's angular frequency. Since triangular phase-shifted carrier modulation is used and each module is Half-Bridge, according to the double Fourier transformation [89], the switching harmonics would be as follows:

$$v_{a0}(t) = \frac{V_{dc}}{2} - \frac{MV_{dc}}{2} \sin(\omega t + \varphi) + \quad (4-27)$$

$$\sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \frac{2V_{dc}}{m\pi} J_n \left(M \frac{m\pi}{2} \right) \cos \left[\frac{(m+n)\pi}{2} \right] \cos [m(\omega_c t + \theta) + n(\omega t + \varphi)]$$

J_n is the Bessel function. From the above equation it can be inferred that $(m+n)$ should be an odd number for the the line frequency of the MMC since it is desirable that the switching frequency component not have any effect on the output voltage and current. So, the switching frequency of the components throughout the arm currents would be as follows:

$$\omega_p = (2p+1)\omega \pm \omega = 2k\omega, p, k = 0..n \quad (4-28)$$

Using same procedure, the voltage ripple across the capacitor can be calculated as follows:

$$\left\{ \begin{array}{l} \Delta v_{cu}^1 = -\frac{\sqrt{2}I_a}{4C\omega} \cos(\omega t + \varphi) + \frac{I_{dc}M}{2C\omega} \cos(\omega t) \\ \Delta v_{cu}^2 = \frac{\sqrt{2}I_a M}{16C\omega} \sin(2\omega t + \varphi) \\ \Delta v_{cu}^{\omega_p - \omega} = -\frac{I_{sw}M}{4C(\omega_p - \omega)} \sin((\omega_p - \omega)t + \theta) \\ \Delta v_{cu}^{\omega_p} = \frac{I_{sw}M}{2C\omega_p} \cos(\omega_p t + \theta) \\ \Delta v_{cu}^{\omega_p + \omega} = \frac{I_{sw}M}{4C(\omega_p + \omega)} \sin((\omega_p + \omega)t + \theta) \end{array} \right. \quad (4-29)$$

And based on equation (3-12), the line frequency and switching frequency voltage across the arm inductor becomes as follows:

$$V_{cir} = \frac{N}{2C} \left(\frac{3M}{4\omega} \sqrt{2}I_a \cos(2\omega t + \varphi) - \frac{M^2}{2\omega} I_{dc} \cos(2\omega t) \right) \quad (4-30)$$

$$\left\{ \begin{array}{l} V_{cir}^{(\omega_p - 2\omega)} = -2N \left(\frac{I_{sw}M^2}{16C(\omega - \omega_p)} \right) \cos((\omega_p - 2\omega)t + \theta) \\ V_{cir}^{(\omega_p)} = -2N \left(\frac{I_{sw}}{4C\omega_p} - \frac{I_{sw}M^2\omega_p}{8C(\omega^2 - \omega_p^2)} \right) \cos(\omega_p t + \theta) \\ V_{cir}^{(\omega_p + 2\omega)} = 2N \left(\frac{I_{sw}M^2}{16C(\omega + \omega_p)} \right) \cos((\omega_p + 2\omega)t + \theta) \end{array} \right. \quad (4-31)$$

From equation (4-29) it can be seen that decreasing the switching frequency causes an increase in the voltage ripple over the capacitor. And in equation (4-31), it can be shown that decreasing the switching frequency causes an increase of the circulating voltage and current. The same result can be achieved by analyzing the switching frequency effect though an inverter LC filter [90].

In Figure 4-19, the switching frequency effect on the voltage and current ripple of the capacitor and arm inductor of the MMC are shown.

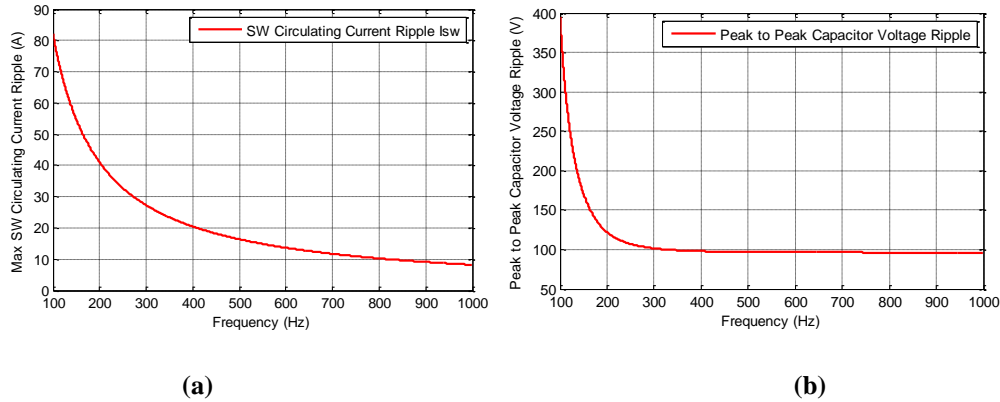


Figure 4- 19: The switching ripple of the arm current and the capacitor voltage with respect to the frequency

As shown in the above equation, the current ripple over the inductor and the capacitor will increase at a lower switching frequency. So, choosing the switching frequency for the MMC will be a trade off between IGBT power loss and maximum allowable voltage and current ripple through the module capacitor and arm inductor. Also, the selection of the switching frequency has an impact on the THD of the output current, which according to IEEE standard 519, should be less than 5% for the weak power system network [91]. Table 4-6 shows simulation results of the effect of switching frequency on the THD of the MMC's output current, the peak to peak voltage ripple of the capacitor, and the upper arm total harmonic distortion in different frequency ranges. The choice of switching frequency should be based on the requested specification from the MMC (i.e. the maximum acceptable voltage ripple over the capacitor is 10% Vdc).

Table 4- 6: Stress Analysis for Different Switching Frequencies

Frequency	Io (THD)	Vcu (pp-ripple)	IuA (THD)
60×5	2.38%	102(V)	39.31%
60×7	<u>0.61%</u>	<u>79 (V)</u>	<u>13.44%</u>
60×9	<u>0.51%</u>	<u>74 (V)</u>	<u>13.4%</u>

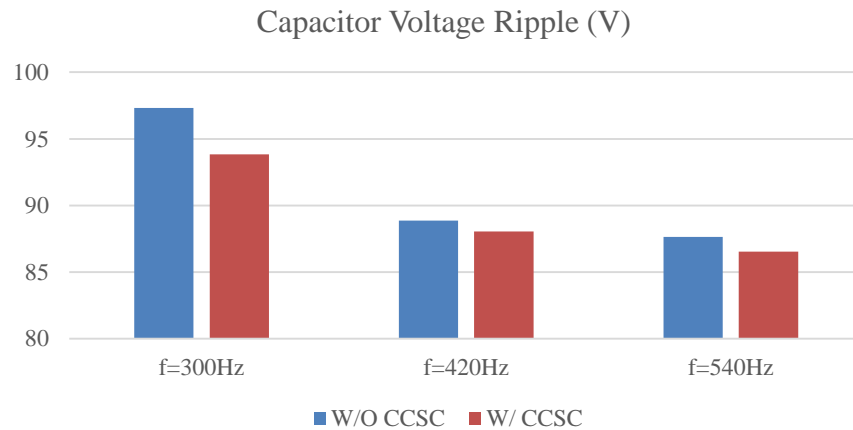
As shown, a switching frequency of less than 60×7 Hz can exceed the voltage ripple within the allowable range. The output frequency also has an effect on the stress over the capacitor voltage and the upper arm current. Especially at low output frequency, the stress over the capacitor voltage and the arm current increases drastically [92], [93]. Future work may include an investigation of the stress and finding a way to decrease the stress at low output frequency, mainly using common mode voltage injection.

4.6.2 Power Loss Calculation of the MMC With and Without Circulating Current Suppressing Control

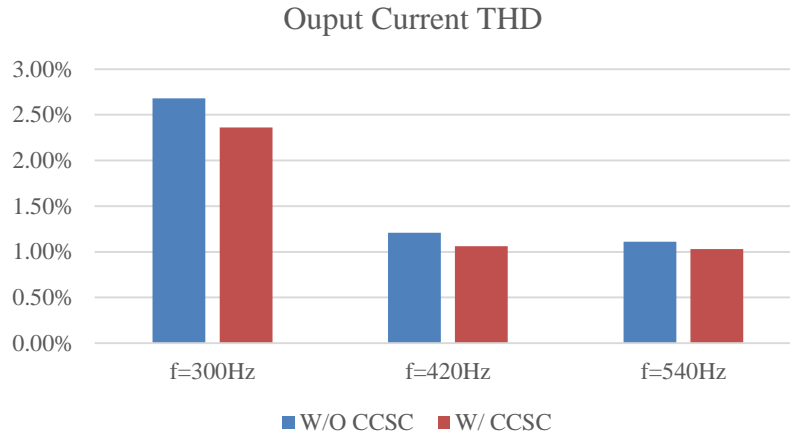
In this section, the power loss calculation of the MMC under different operating frequencies with and without Circulating Current Suppressing Control (CCSC) will be presented. The circulating current suppressing controller's effect on converter power loss is determined as well. Semiconductor losses considered include conduction and switching losses, and are calculated based on the corresponding datasheets. The specific IGBT and diode have been selected and details regarding that will be presented later. Specifically, diode and IGBT conduction losses can be measured using the method presented in [94] and the devices' datasheets.

As previously noted, equation (4-31) explains how reducing the switching frequency increases the circulating current through the phase-arm, which will in turn increase the conduction loss through the IGBTs. Accordingly, switching loss will increase as the switching frequency increases, as expected. This is illustrated in Figure 7 for the diode and IGBT respectively.

These figures show the effectiveness of the circulating current suppressing control in decreasing the semiconductor losses regardless of the switching frequency employed, with a slightly higher effect at lower switching frequencies. The voltage ripple across the IGBT and capacitor bank increases for lower switching frequencies, indicating that switching frequency selection for the MMC is a critical parameter with crucial tradeoffs in terms of reliability. The following subsection will investigate the impact and effect of this. .



(a)



(b)

Figure 4- 20: Peak-to-peak voltage ripple of the capacitor and the output current total harmonic distortion in the different frequency ranges

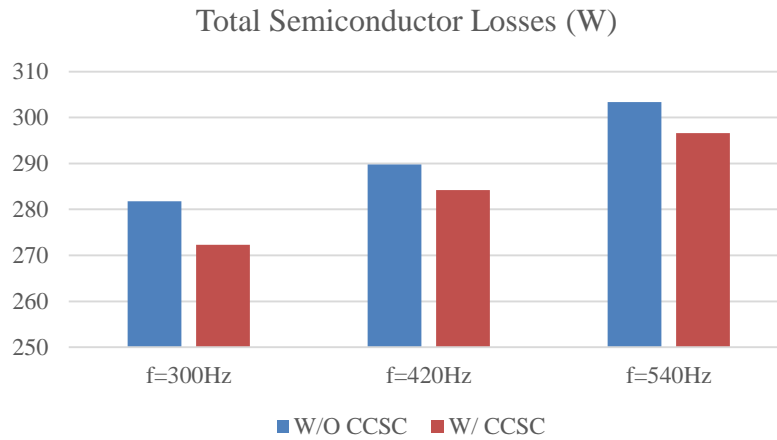
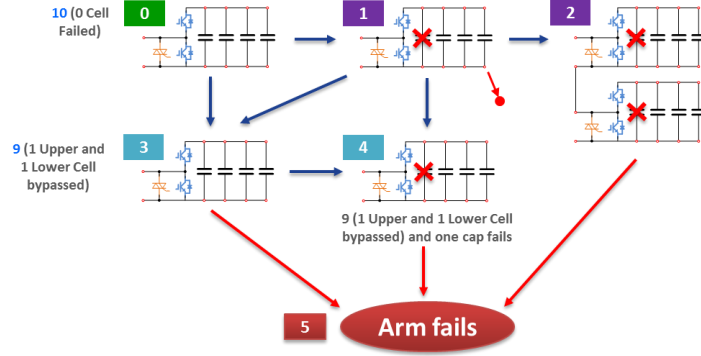


Figure 4- 21: Switching losses of the IGBT in different frequencies, with and without CCSC

4.6.3 Reliability Modeling of the MMC Based on the Markov-State Space Model

A maximum voltage overshoot of 40 % at turn-off was assumed for the IGBT devices of the power modules, corresponding to a 400 V overshoot for the 1 kV DC bus design. Accordingly, the maximum limit for the capacitor bank's peak-voltage is 1,300

V, at which point the IGBT blocking voltage rating would be surpassed (1,700 V). The voltage rating chosen for the DC bus film capacitors is consequently 1,300 V, to which a 5 % tolerance is then added by the capacitors' own specifications. The Markov Chain model of the conventional power module is shown in Figure 4-22, where State 0 indicates ten modules operating normally. State 1 indicates that if one capacitor in any power module fails, the converter can still operate without distorted line current or capacitor overvoltage. State 2 indicates that if two capacitors in any two power modules fail, the converter can still keep operating. Any component fault at State 0, 1 and 2 can possibly lead to a transition to State 3, State 4 or State 5, where the phase-arm is considered failed. In State 3, a faulty power module is bypassed, requiring a corresponding power module in the opposite phase-arm to be bypassed in order to maintain the capacitor voltage balance. This operation does not affect any of the other two converter phase-legs. There is no remaining fault part in State 3. In State 4, if one capacitor in any of the remaining nine power modules fails, the converter can still keep working without exceeding its operational limits and triggering its protection system. In Figure 4-22, the respective waveforms for States 0 through 4, illustrate, from top to bottom, the phase and line-to-line AC voltages of the converter, line currents, circulating currents, phase-arm currents, DC current, and the power module voltages. The progressive deterioration of the distortion of these waveforms, aside from the AC variables, shows how the converter can still operate as long as its internal voltage and current limits are not exceeded.



$V_{Peak} > 1300V$, CELL fails

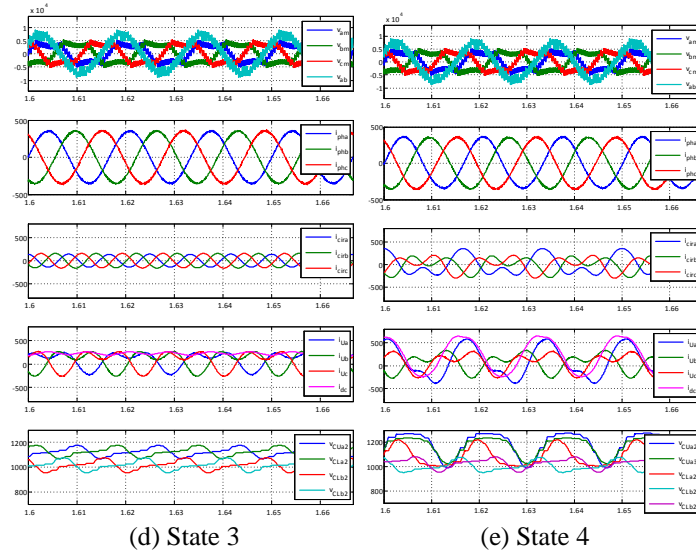
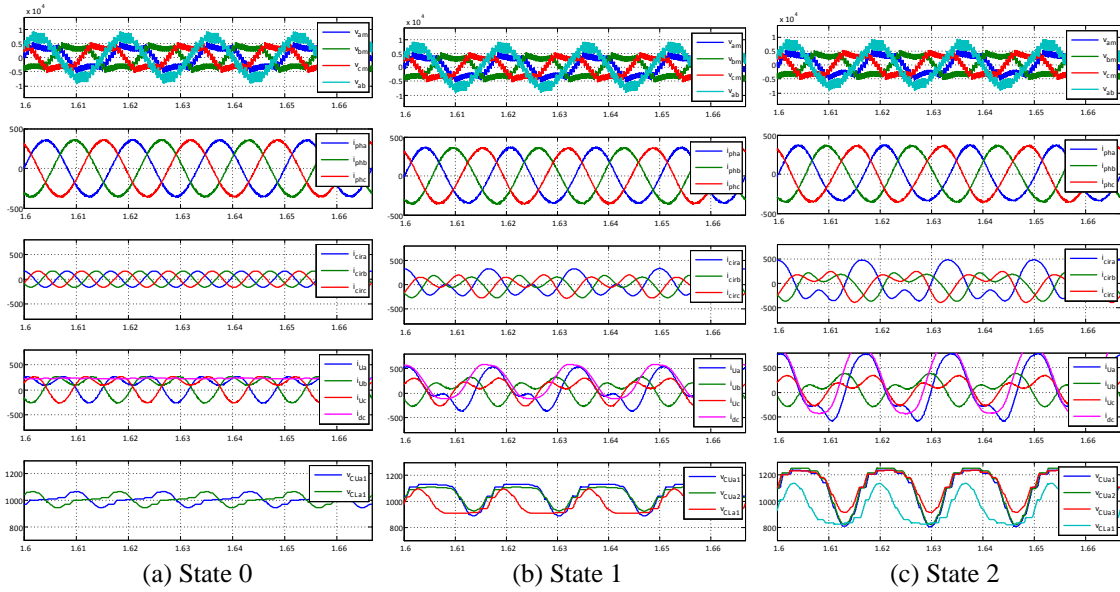


Figure 4- 22: Reliability Model of the Modular Multilevel Converter with three-phase output voltage, current, circulating current, upper arm, DC current and capacitor voltage in each failure state

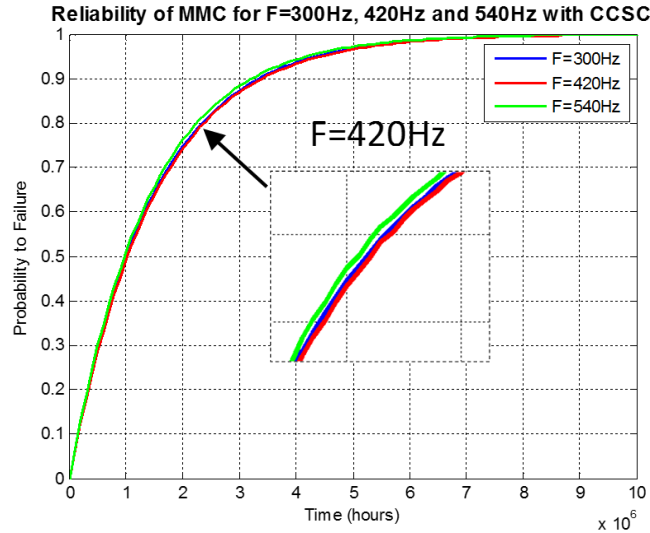


Figure 4- 23: Markov Reliability Model of the MMC with Circulating Current Suppressing Controller in different frequencies

4.6.4 Reliability Comparison of MMC Under Different Frequencies With and Without Circulating Current Controller

The full Markov reliability model of the MMC and the corresponding analysis results were presented in the previous section. What follows focuses on the non-redundant reliability model of the MMC, investigating reliability tradeoffs under different switching frequencies with and without CCSC. Figure 4-23 shows a plot of the probability for failure in time for the MMC operating at a switching frequency of 300 Hz, 420 Hz, and 540 Hz, with and without CCSC, where it can be concluded that the circulating current controller does have a positive impact on the converter's reliability. As a final comparison, the reliability models obtained for each switching frequency with CCSC are depicted in Fig. 9 for comparison purposes. As shown, the 420 Hz case achieved the best reliability performance, although only a minor overall impact was determined. This result shows that although fewer semiconductor losses are incurred

when operating at lower switching frequencies, the increase of the voltage ripple across capacitors and IGBTs can detrimentally affect the reliability of the converter, illustrating one of the key tradeoffs when designing the MMC.

4.6.5 Conclusions

This section presents a reliability oriented switching frequency analysis for the MMC in different applications. The stress analysis of the MMC for phase-arm currents and voltages, as well as the converters' output voltage and current, is conducted by evaluating the impact of switching frequencies' harmonic components in the low switching rate. The effect of a circulating current suppressing controller is also investigated. The switching frequency evaluation showed an optimum point favoring a medium switching rate, as the circulating current harmonic content was seen to increase at lower frequencies, resulting in heightened conduction losses for the devices and a higher voltage ripple for the power-cell capacitors.

4.7 AAC Design Considerations

4.7.1 Number of Cells in the AAC

One of the promising features of the AAC is that to provide the same voltage level as the MMC, the AAC needs only about half the number of power cells, comparatively. The voltage over each module is almost half the rated voltage of modules in the MMC. To calculate the voltage over the stack, if assuming that the voltage over the arm inductor is negligible and that the AAC works in the sweet spot, the voltage of the upper stack can be written as:

$$\begin{cases} V_{stackmax} = \frac{V_{DC}}{2} \\ V_{stackmin} = \frac{V_{DC}}{2} (1-M) \end{cases} \Rightarrow \Delta V_{stack} = \frac{V_{DC}}{2} (1+0.27) = \frac{V_{DC}}{2} (1.27) \quad (4-32)$$

The above voltage range compared to the stack voltage in the MMC is almost half, as shown in (4-33):

$$\begin{cases} V_{stackmax} = \frac{V_{DC}}{2} + \frac{V_{DC}}{2} \\ V_{stackmin} = 0 \end{cases} \Rightarrow \Delta V_{stack} = \frac{V_{DC}}{2} (1+1) = V_{DC} \quad (4-33)$$

So, the AAC with a full-bridge module has almost the same number of cells as the MMC half-bridge when the voltage level is assigned.

By having the rated voltage of each cell for the AAC, the number of cells can be defined as:

$$N_{cellAAC} = \frac{2 V_{DC}}{\pi V_{Cell}} \quad (4-34)$$

In contrast, the number of cells for the MMC can be written as:

$$N_{cellMMC} = \frac{V_{DC}}{V_{Cell}} \quad (4-35)$$

4.7.2 Number of Director Switches in the AAC

The number of director switches can be calculated based on the maximum voltage over the DS, which is the difference between the output voltage and the voltages of the same arm stacks when DS is off. In Figure 4-24, the voltage over each DS can be seen in the average mode. So for the upper and lower arm, voltage over DS switches can be obtained by:

$$V_{DS} = +v_{ac} + \frac{V_{DC}}{2} - v_{stack} \quad (4-36)$$

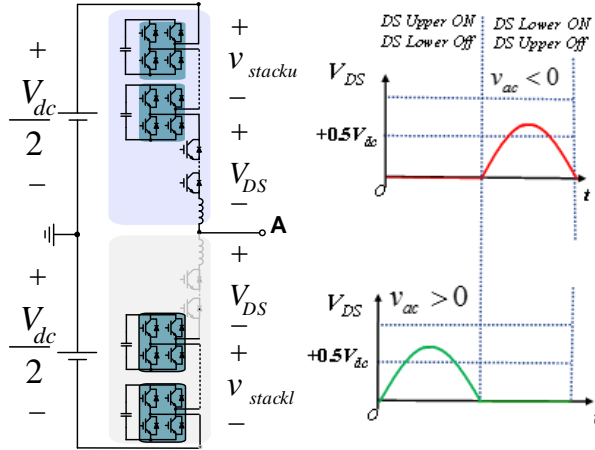


Figure 4- 24: Voltage over the Director Switches in each cycle

The maximum voltage over the director switches can be obtained by:

$$V_{DS\max} = V_{ac\max} + \frac{V_{DC}}{2} - V_{stack\max} = \frac{4 + \pi}{2\pi} V_{DC} - V_{stack\max} \quad (4-37)$$

From the above equation, one can determine the number of required cells to withstand the maximum possible voltage.

4.7.3 DC- Fault Management and Ride-Through of the AAC

Since the AAC consists of full-bridge modules, the stack can be negative. This feature makes the operation of the AAC during the DC-Fault, as STATCOM. From equation (4-32), the stack voltage can be written as:

$$v_{stack} = \frac{v_{dc}}{2} - v_{ac} \stackrel{v_{dc}=0}{\Rightarrow} v_{stack} = -v_{ac} \quad (4-38)$$

As shown in the above equation, in case of a short circuit on the DC side, the stack voltage should produce negative line voltage. In this situation, the AAC converter converts to STATCOM, which enable the transfer of reactive power to the system. Different possible modes of the AAC are shown in Figure 4-25. In case of DC Fault, in

one scenario, both DS switches can be turned on, and the upper and lower arm both operate as the STATCOM, or just one of the upper or lower arms can be connected to the grid. These scenarios are shown in Figure 4-25.

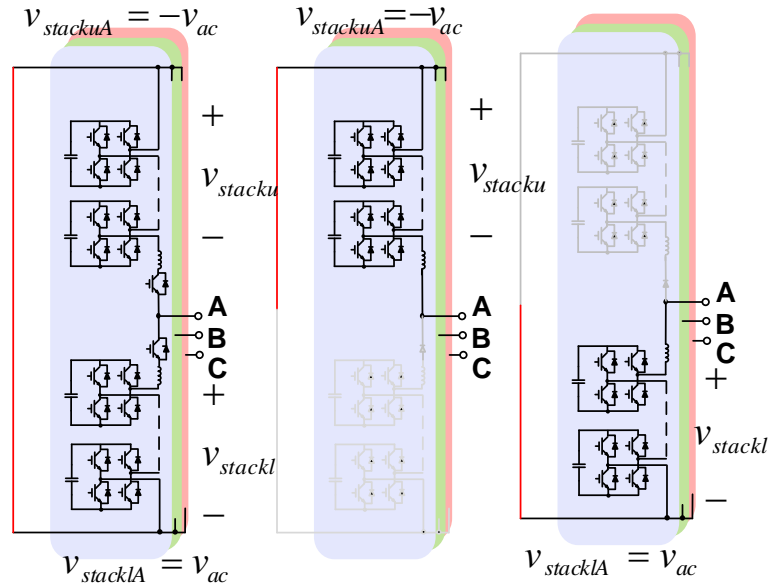


Figure 4- 25: Three different scenarios of DC-fault ride-through of the AAC

4.7.4 Zero Current Switching (ZCS) Operation of the Director Switches in RL loads

One of the AAC's crucial issues is that the operation of the director switches will lead to high switching loss and conduction loss. The existence of the series of the load and Arm inductor with the IGBT series causes switching to occur in non-zero current, which it makes high di/dt, creating voltage spikes and stress over the DS and power cells. To address this issue, the overlap time consideration of the AAC is used as a way to provide ZCS of the DS in ACC.

A. Zero Current Switching Scheme of the DS

In Figure 4-26, hard switching vs. soft switching of the DS in the AAC is shown. As shown in Figure 4-26, using overlap time between the upper and lower arm DS, the current through the resonant LC circuit can go to negative values and the ZCS can be achieved. As will be shown later, during the overlap time, all the cells will be inserted into the arm, and the voltage difference of the DC voltage and arm voltage will be disbursed over the arm inductor, which will be negative. This voltage makes the current through the arm become negative and provides Zero Current Switching.

B. Consideration of ZCS operation of DS and proposed scenario for Overlap time

To enhance the ZCS operation of the DS, the voltage over the inductor should be the maximum possible value that can be achieved. Therefore, the stack voltage during the off DS cycle should be keep as high as possible. The proposed scenario, which enhances the ZCS operation of the director switches, is shown in Figure 4-27. The important parameter to consider for ZCS operation of the DS is the arm inductor, which must be designed carefully to provide ZCS. The inductor should be designed to provide appropriate resonant frequency as well as desirable switching frequency ripple for the current during the overlap time.

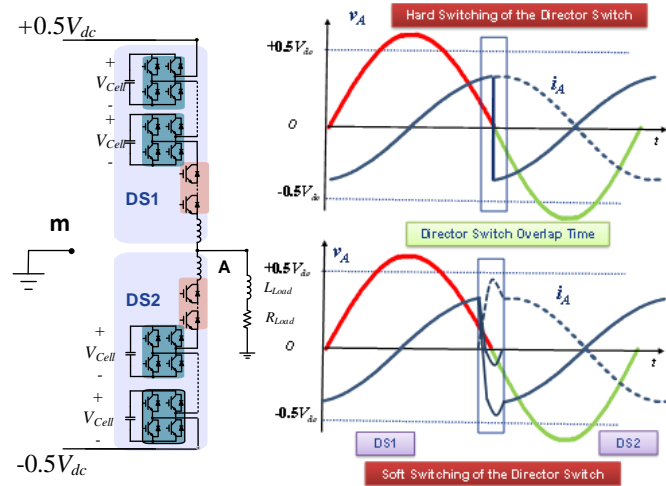


Figure 4- 26: Zero Current Switching realization in AAC vs. Hard Switching

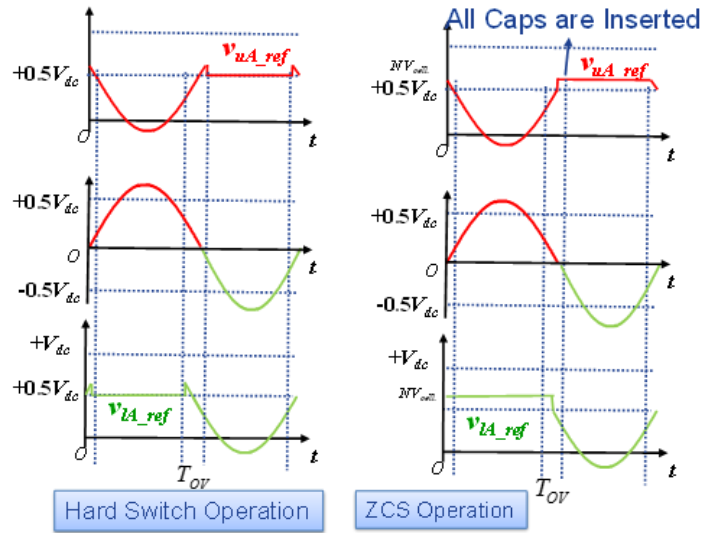


Figure 4- 27: Proposed overlap time scenario for the DS

4.7.4.1 ARM Inductor Design of the AAC for ZCS

To design the arm inductor, the behavior of the AAC during the overlap time will be discussed first. The behavior of the AAC during the overlap time is shown in Figure 4-28. The equivalent circuit will be a series LC resonant circuit. The equation during this time can be written by assuming the arm resistance is negligible. In Figure 4-28, it is assumed to have four-H-bridge for simplicity of the drawing. During the overlap time, all

capacitors are connected positively to the arm, so that the equivalent circuit will be simply L and C circuit. Notice that during overlap the output voltage is close to zero. So, the upper and lower arm can be separate from the two resonant LC series converter. The equivalent circuit is shown in Figure 4-29. By assuming that the current in this mode is $i(t)$ and the direction of that is in a negative direction of the load current, the current equation can be written as:

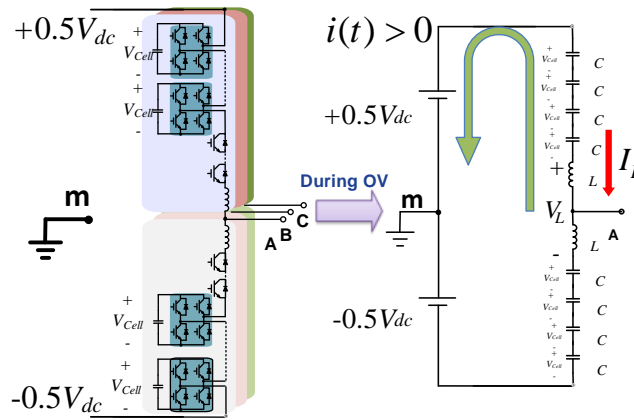


Figure 4- 28: The behavior of the AAC during the overlap time

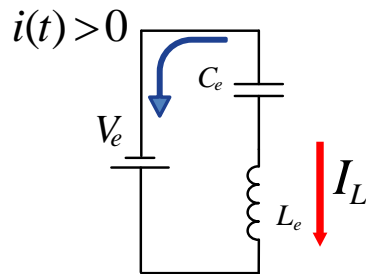


Figure 4- 29: The equivalent circuit of the AAC during overlap

$$i(t) = -I_L \cos(\omega_r t) - \frac{V_e}{Z_n} \sin(\omega_r t) \quad (4-39)$$

$$\omega_r = \sqrt{\frac{1}{L_e C_e}}, Z_n = \sqrt{\frac{L_e}{C_e}}$$

Where, V_e is the equivalent voltage over the inductor as:

$$V_e = NV_{Cell} - \frac{V_{DC}}{2} \quad (4-40)$$

Notice that during overlap time we have $2NV_{cell} > V_{DC}$. So the negative voltage will be across the inductor.

To provide ZCS, the $i(t)$, the current of the equivalent circuit, should make the initial negative load current positive. So, in order to provide ZCS, the current should be positive, as:

$$i(t_{ov}) > 0 \quad (4-41)$$

From condition (4-41) and equation (4-39), the condition for the inductor will be obtained as follows:

$$\tan(\omega_r t_{ov}) \geq -\frac{Z_n I_{max} \sin \varphi}{V_e} \quad (4-42)$$

One of the simple ways to find the value of the maximum inductor is by noticing that for $\omega_r t_{ov} \geq \pi$, the current will be positive, so the maximum inductor will be as follows:

$$L_e \leq \frac{1}{C_e} \left(\frac{t_{ov}}{\pi} \right)^2 \quad (4-43)$$

Where, t_{ov} is the overlap time between the upper and lower DS. Since during the overlap time the load inductor load has nothing to do with the inner loop, the value of the inductor cannot be set to low because of the switching frequency ripple. To ensure appropriate current frequency ripple, the inductor selection should meet minimum requirements. The voltage over the arm inductor can be written as:

$$V_{L\max} = 2L \frac{dI}{dt} \quad (4-44)$$

$$\begin{cases} V_{L\max} = 2NV_{cell} - V_{DC} \\ V_{L\max} = 2L \times \Delta I \times F_s \Rightarrow \Delta I = \frac{V_{L\max}}{2L \times F_s} \\ \Delta I \leq \Delta I_{\max} \end{cases} \quad (4-45)$$

Where F_s is the equivalent frequency of the converter considering interleaving. From (4-45), the condition for the arm inductor to provide the required switching frequency ripple is obtained as:

$$L \geq \frac{V_{L\max}}{2\Delta I_{\max} \times F_s} \quad (4-46)$$

From (4-43) and (4-46), the required size of the arm inductor will be determined. Since, in the AAC, there is no circulating current between the upper and lower arm, the size of the inductor will be expected to be relatively low in comparison to the arm inductor for the MMC.

4.7.4.2 Power Cell Capacitor Bank Design

The capacitor bank design for each module is taken from Reference [62]. The required capacitor bank size can be obtained by following the equation. The procedure used to find the capacitor size is same as for that of the MMC. Results show that the required capacitor size for the AAC is almost half of the capacitor size of each module in the MMC. The capacitor sizes of the AAC and the MMC are shown in (4-47):

$$C_{cell} = \frac{\Delta E_{stack}}{2N_{cell} V_{cellN} \Delta V} \quad (4-47)$$

$$\begin{cases} C_{cell\ MMC} = \frac{|S|}{3\omega V_{DC}} \frac{1}{\Delta V} \\ C_{cell\ AAC} = \frac{|S|}{3\omega V_{DC}} \frac{0.505}{\Delta V} \end{cases} \quad (4-48)$$

Where, ΔV is the allowable voltage ripple over the module, S is the power rate of the converter and ω is line frequency. Equation (4-48) is obtained by finding the maximum energy difference in both the MMC and the AAC, and results show that ΔE_{max} for the AAC is about $\frac{1}{3}$ that of the MMC.

Table 4- 7: Case study of AAC specifications

Power rate	600kW
DC Line Voltage	4kV
Line to Line Voltage	3.3 kV
RL Load	10 Ω 0.02mH
R	15 Ω
Switching Frequency	1kHz
Module Rated Voltage	637 V
Pole Voltage Levels	9
Cell Cap size for $\Delta V < 30$	4mF
Arm Inductor	600mH

4.7.5 Simulation Analysis

A simulation analysis has been done through Simulink/Matlab to verify the proposed scheme for Zero Current Switching and the analytical analysis of the capacitor voltage ripple, as well as operation of the AAC in resistive and RL loads. The specifications of the case study for the AAC are shown in Table 4-7. The simulation was done for pure resistive loads of 15 Ω and resistive and inductive load of RL. The simulation is shown in the following sections.

4.7.5.1 Simulation Result in Resistive Load

In this section, the AAC is simulated defining the load as resistive. In Figure 4-30, the upper and lower arm key waveforms are shown. The upper and lower arm current, and capacitor voltage and phase and DC line current can be seen in this figure.

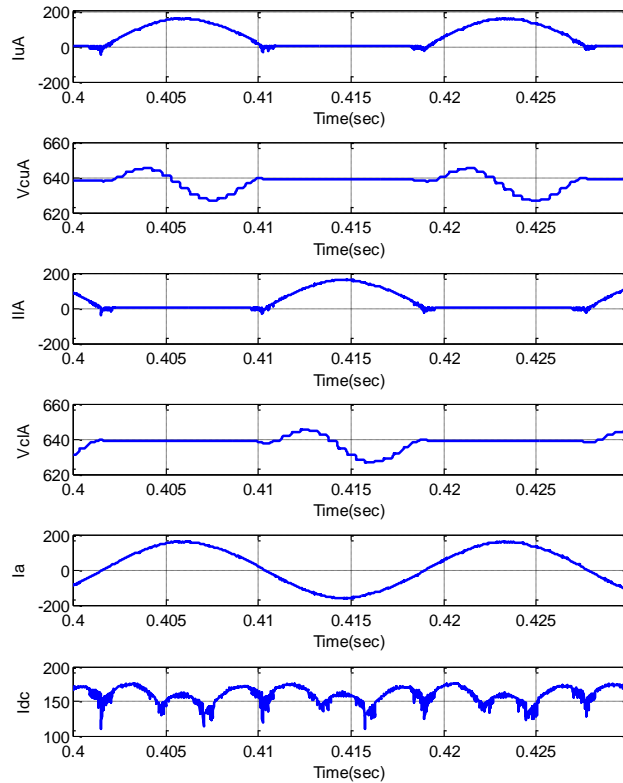


Figure 4- 30: Arm, DC and Phase Current and cap voltages

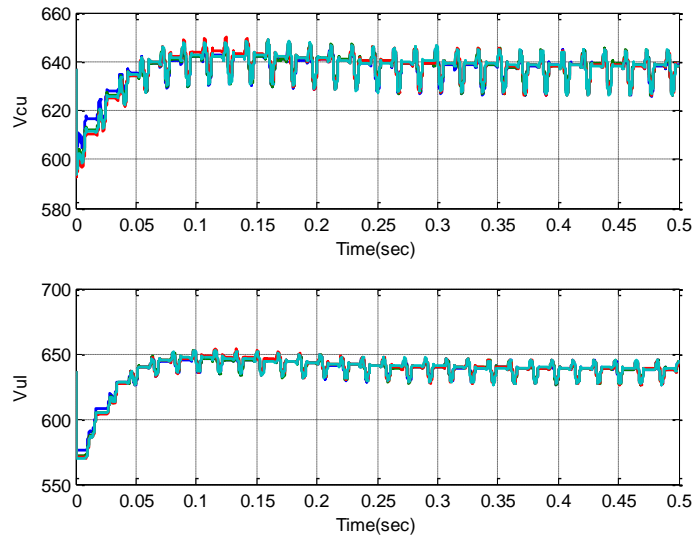


Figure 4- 31: Capacitor voltage balance scheme

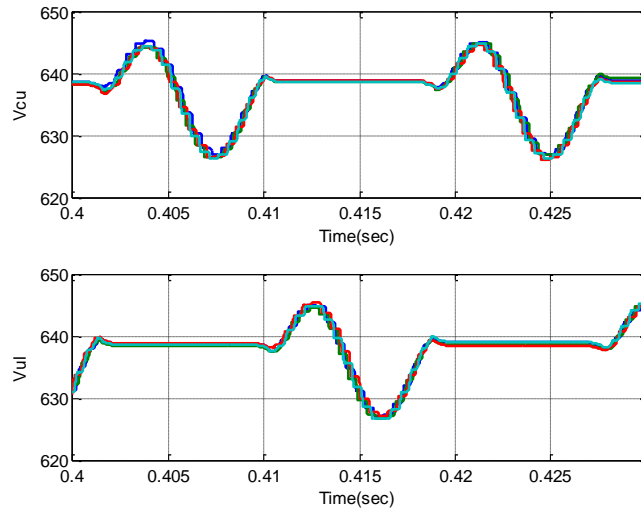


Figure 4- 32: Capacitor voltage waveform

Capacitor balancing is shown in Figure 4-31, and the capacitor voltage waveform is shown in Figure 4-32. The capacitor voltage waveform is determined in the same manner as was the analytical capacitor waveform, as explained in chapter 3. The three-phase current is shown in Figure 4-33. The three-phase output line-to-line voltage and pole voltage can be seen in Figure 4-34 and Figure 4-35.

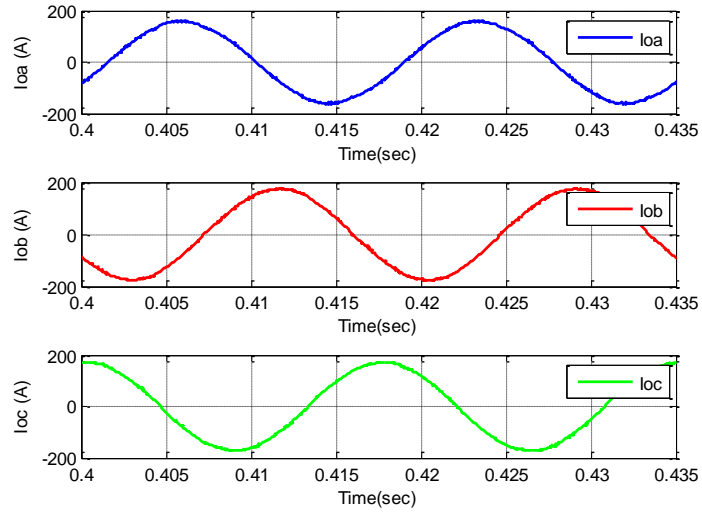


Figure 4- 33: Three-phase output current

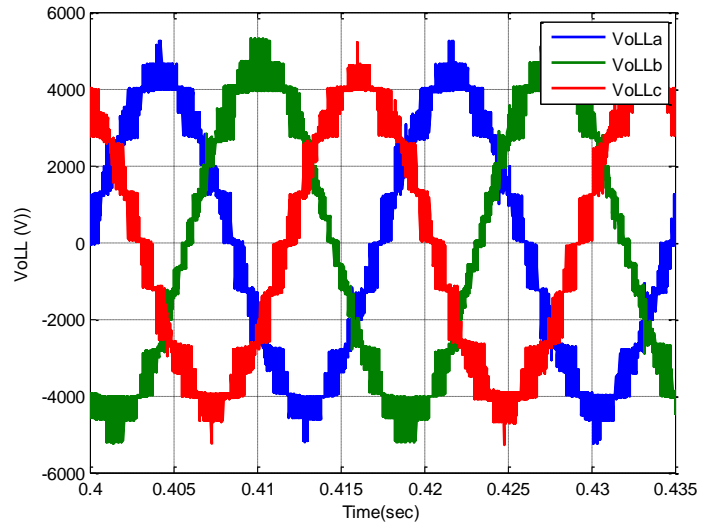


Figure 4- 34: Three Phase output line-to-line voltage

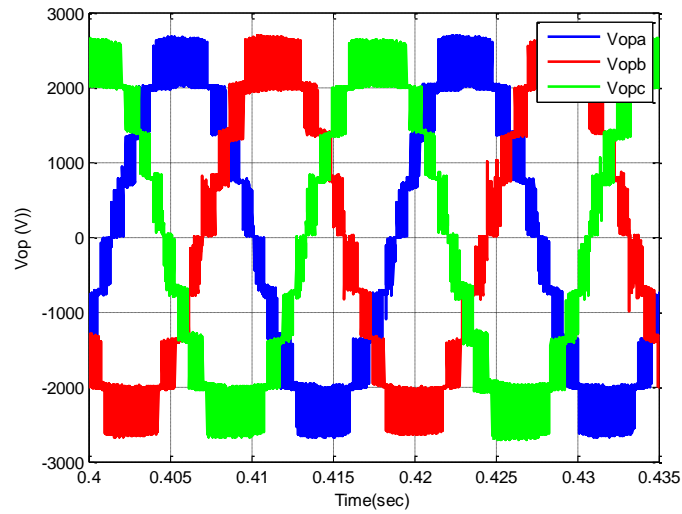


Figure 4- 35: Three Phase output pole voltages

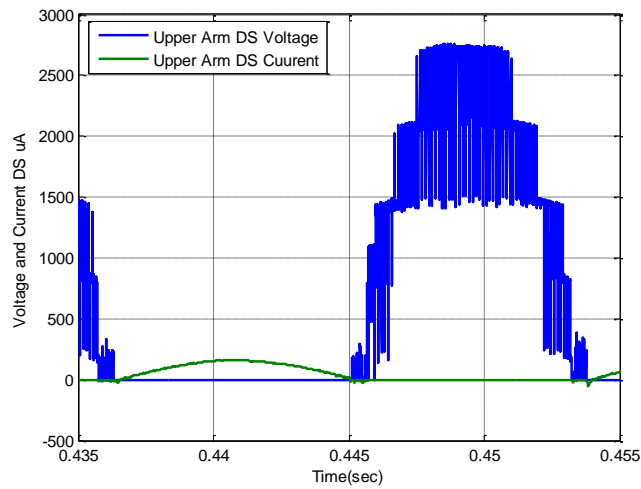


Figure 4- 36: Upper Arm DS voltage and current

As shown, the output three-phase pole voltage has 9 levels and the line-to-line voltage has 19 levels when the number of cells are 4 full-bridge. The upper arm DS voltage and current are shown in Figure 4-36.

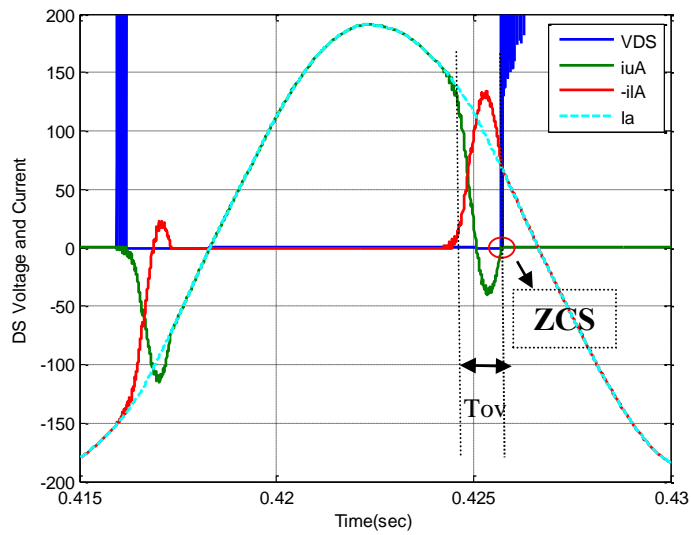


Figure 4- 37: DS voltage and current

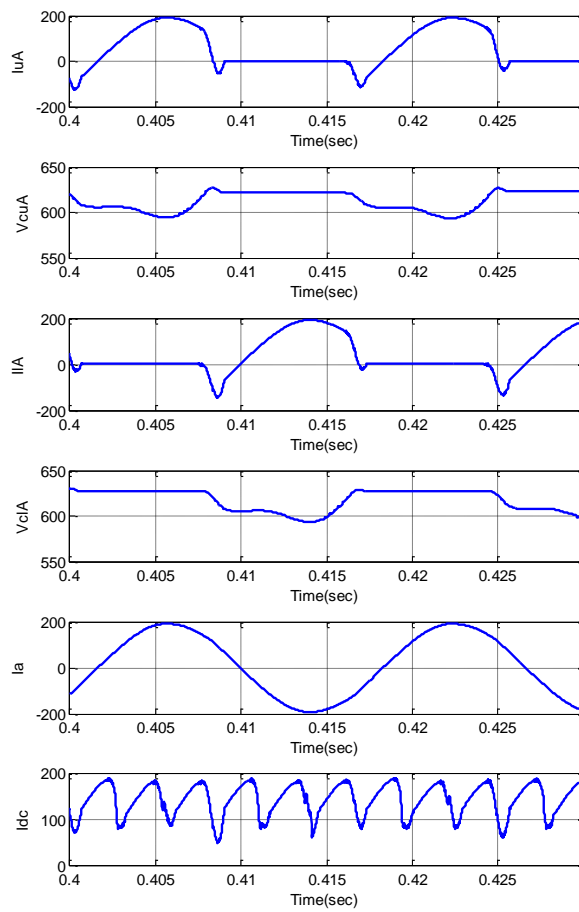


Figure 4- 38: Arm, DC and Phase Current and cap voltages

4.7.5.2 Simulation Result for RL Load

The simulation was done with an inductive load to verify the ZCS operation of the AAC in this condition. To see how the ZCS can be achieved for DS, the upper arm Direct Switch is chosen and the upper arm, lower arm, and phase current are shown with respect to that in Figure 4-37. As shown, the turn off of the DS switch happens when the current is zero. The voltage and current waveforms of the upper and lower arm with the phase and DC line current are shown in Figure 4-38. The capacitor voltage balancing and capacitor voltage waveform are shown in Figure 4-39 and Figure 4-40. The waveform of the capacitor is determined by analysis, which is explained in chapter 3. The output current and line-to-line voltage waveforms in this case are shown in Figure 4-41 and Figure 4-42, respectively.

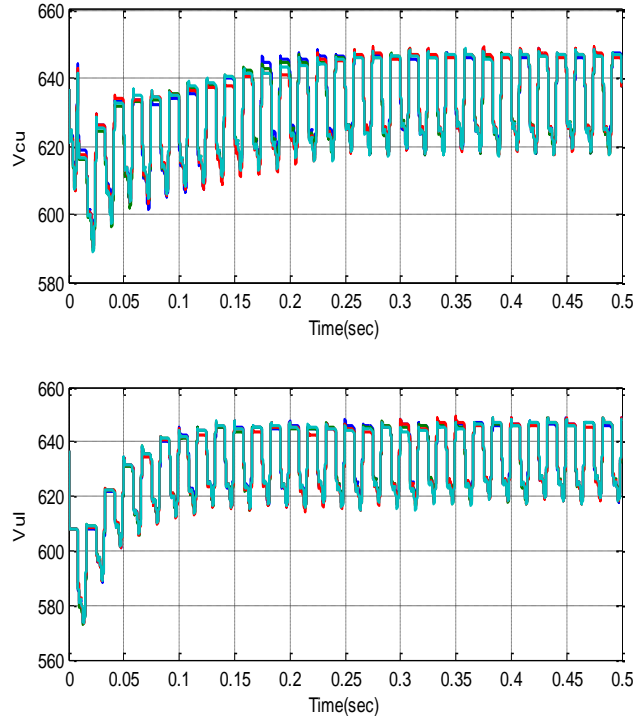


Figure 4- 39: Capacitor voltage balance scheme

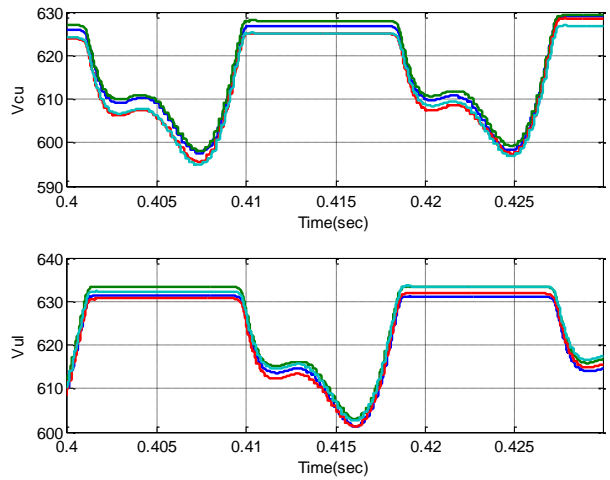


Figure 4- 40: Capacitor voltage waveform

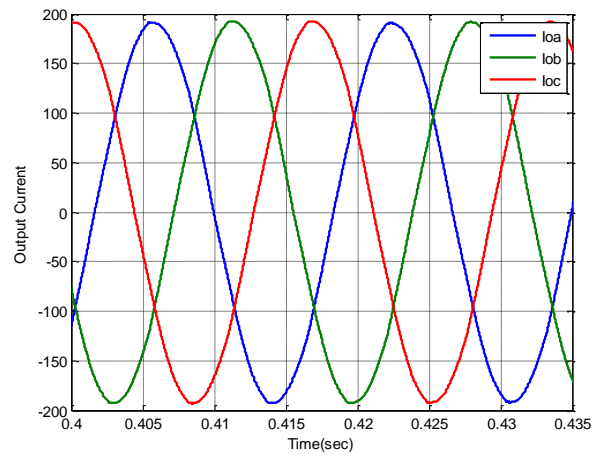


Figure 4- 41: Three Phase output line to line voltage

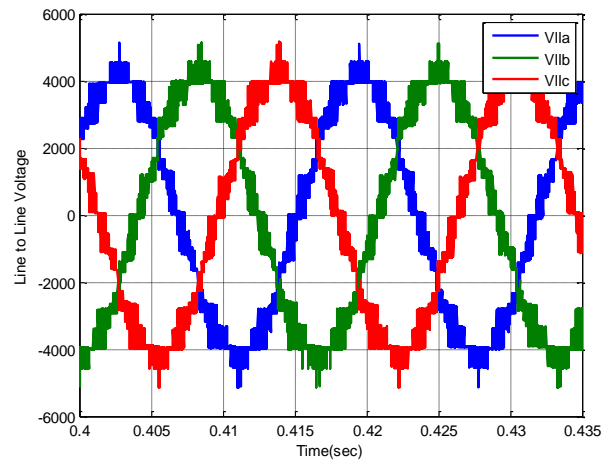


Figure 4- 42: Three-phase output current

4.8 Design and Switching Losses Comparison Between AAC and MMC

In this section, the design comparison between the AAC and Half Bridge MMC will be discussed. The specification is shown in Table 4-7 for both AAC and MMC. The design procedure is shown in the following.

To achieve the required pole voltage level, the number of half-bridge cells can be obtained for both the MMC and AAC as given in:

$$\begin{cases} Level = 2N_{cellAAC} + 1 = 9 \Rightarrow N_{cellAAC} = 4 \\ V_{CellAAC} = \frac{2}{\pi} \frac{V_{DC}}{N_{cell}} = 637 \end{cases} \quad (4-49)$$

And for MMC, we have:

$$\begin{cases} Level = N_{cellMMC} + 1 = 9 \Rightarrow N_{cellMMC} = 8 \\ V_{DC_NEW} = 1.27 \times V_{DC} \cdot V_{CellMMC} = \frac{V_{DC_NEW}}{N_{cell}} = 637 \end{cases} \quad (4-50)$$

Notice that since the MMC cannot work in over-modulation mode to produce the same voltage rate at the output, we assume that the DC voltage will be boosted to $1.27 \times V_{DC}$ to provide same voltage range. From equation (4-37), the voltage over the director switches can be obtained. A reliability-oriented selection method for IGBT has been done in [95]. By using the IGBT module FZ800R12KE3, 1.2kV, and 800 A rated current, the design of the module and DS for both the MMC and AAC has been carried out. In Table 4-8, the number of IGBT switches, capacitor size, and required arm inductor are given for the MMC and AAC.

Table 4- 8: Number of switches in AAC and MMC

Number of SW	AAC	MMC (Half-Bridge)
Module	32	32
DS	12	0
ARM Inductor	0.6mH	3mH
Module Cap Size $\Delta V < 30$	4mF	8mF

The AAC and MMC (half-bridge) switching losses are shown in Figure 4-43 and Figure 4-44. The conduction losses and switching losses are estimated based on [94]. As shown, the switching losses and conduction losses in MMC are a little higher because of the relatively high circulating current in the MMC. The director switches also have high conduction and switching losses, which is not desirable. The total switching losses of the AAC vs. the MMC (half- bridge) is shown in Figure 4-45.

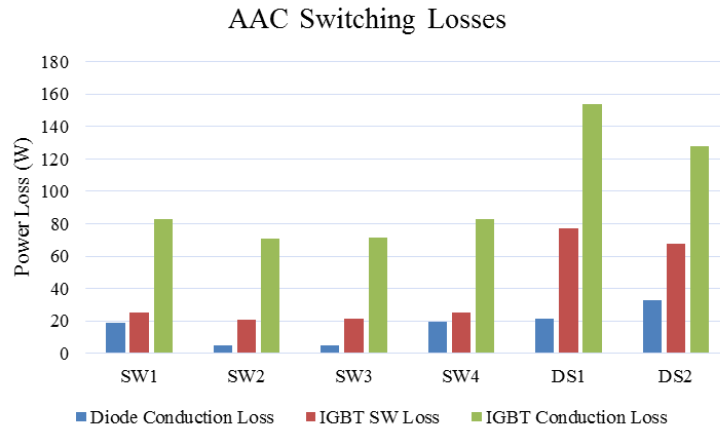


Figure 4- 43: AAC switching power losses

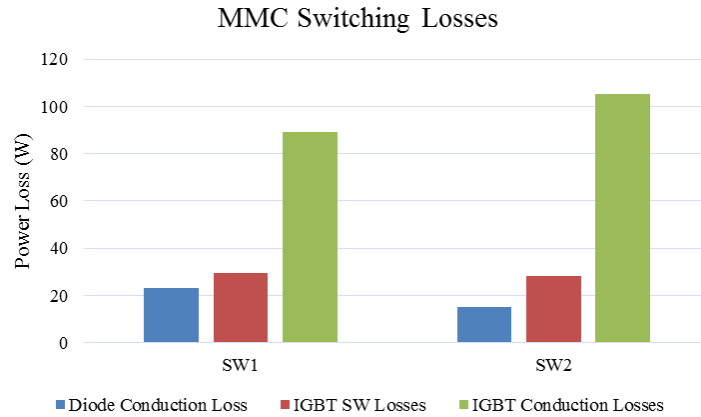


Figure 4- 44: MMC (half-bridge) switching power losses

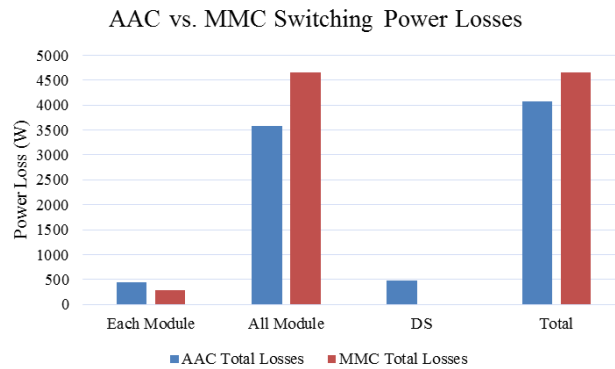


Figure 4- 45: MMC (Half Bridge) and AAC total switching losses

As shown, despite the AAC having an overall higher number of switches, the switching power losses of the AAC are estimated to be lower than those of the MMC, mainly because of the absence of circulating current in the AAC, and alternating of the load current during each half-line frequency cycle. However, in the AAC, the director switches suffer from high switching losses.

4.9 Conclusions

In this work, the operation principles and design procedure of the AAC have been explained. The operation of the AAC under resistive and inductive resistive loads are discussed and the Zero Current Switching operation of the director switches in the AAC

in order to avoid high voltage spikes in arm devices is illustrated. The design procedure of the arm inductor for the AAC is developed based on providing appropriate resonant frequency to achieve ZCS in DS. The AAC operation analysis is supported by the simulation analysis carried out in SIMULINK/Matlab where the operation of the AAC and ZCS workings of the DS are simulated. Finally, a design and switching power loss comparison between the AAC and half –bridge MMC has been done in a sample case study. The results show that the AAC, despite having a higher number of switches, will have fewer switching power losses, mainly because of the lack of circulating current and alternating of the load power. However, the AAC also suffers from high switching power losses on the director switches.

Chapter 5 DC Fault Ride-Through Capability of Modular Multilevel Converters

5.1 Motivation

One of the main issues of Modular Multilevel Converters with half-bridge power cells is their lack of DC-fault blocking capability. To tackle this issue, a full-bridge power cells-based structure should be employed to rid the MMC of an uncontrollable current path in case of a collapse of the DC bus voltage. Either the MMC structure with full-bridge building blocks or the recently developed AAC can be used to solve this problem. In this chapter, the fault ride-through capability of the MMC with full-bridge power cells and the AAC during a local terminal to terminal short circuit of the DC-link for medium voltage DC applications is illustrated. The employed control scheme provides blocking of the fault current as well as capacitor voltage control during the DC fault. The simulation analysis is carried out using SIMULINK/ MATLAB for both the MMC with full-bridge power cells and the AAC during both normal operation and DC fault interrupt in order to illustrate the operation of the adopted fault control scheme. Finally, an overall comparison is presented for the MMC with full-bridge cells and the AAC in terms of the DC fault blocking capability and other related aspects.

5.2 Introduction

One of the main issues of the conventional MMC structure with half-bridge power cells is their inability to block current during DC side faults. Basically, the conventional MMC suffers from poor DC fault performance that requires fast circuit breakers to disconnect the converter by opening from the AC side [96],[97]. In addition, time delay associated with the opening of the circuit breaker on the AC side imposes high fault currents through the uncontrolled path of the antiparallel diode in the half bridge MMC [88]. The other solution for tripping the DC fault current in the VSC converter for high and medium voltage applications is interrupting the DC fault by using DC circuit breakers [98]. However, the technology is neither mature nor cost effective and will add more complexity since the DC circuit breakers have to provide the following functionality: (i) Make a current zero crossing to interrupt the current, (ii) dissipate the energy stored in the system inductance and (iii) withstand the voltage response of the network after current interruption [99]. In Figure 5-1 (a) the conventional MMC with half-bridge modules is shown during the DC fault. The modular multilevel converters (MMC) include two arms per phase, where in each arm several identical sub-modules are connected in series. To limit inrush currents and other current transients (circulating currents) that occur due to the intrinsic switching-action voltage difference between the converter phase-legs during normal operation [100], two arm inductors will be added in series with other cells. Each cell in the modular multilevel converter can be realized as a half-bridge or full-bridge circuit or it can be a series connections of switches in the so-called hybrid topologies of the modular multilevel converters [23], [29],[36]. As previously mentioned, the half-bridge topology of the MMC suffers from the

uncontrollable antiparallel diode path exists in each SM, which, in the case of the DC-side fault, leads to the breakdown of the converter. To resolve the issue, the full-bridge realization of each cell should be utilized to enhance the DC side controllability of the converter. Using the full-bridge SM can generate negative voltage to block the DC fault current in terms of the DC terminal short circuit. Figure 5-1 (b) depicts the MMC containing full-bridge power cells during a DC short circuit. Using the new breed of hybrid multilevel voltage source converters can improve the MMC with full-bridge cells in terms of semiconductor losses, efficiency and converter size [36],[101].The recently developed AAC, which is from the family of the hybrid multilevel voltage source converters, is shown during the DC fault in Figure 5-1. (c).

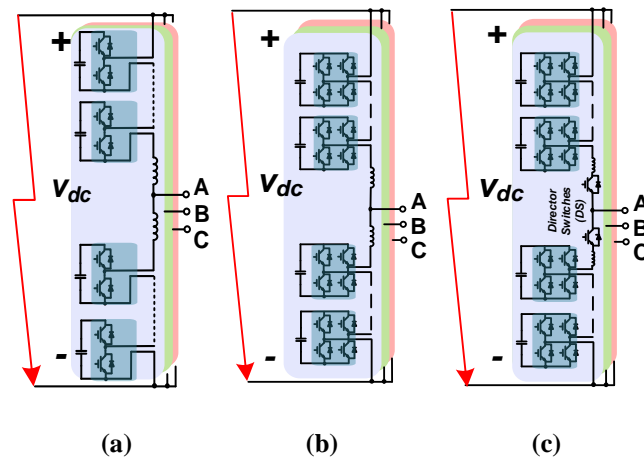


Figure 5- 1: DC Fault Occurrence in (a) Modular Multilevel Converter (MMC) with Half-Bridge Power Cells (b) Modular Multilevel Converter (MMC) with Full-Bridge Power Cells and (c) Alternate Arm Converter (AAC)

Several studies have been carried out in the literature to tackle and analyze the MMC's DC fault problem. An innovative topology, which is adopting the Double-Clamp-SM in the MMC, is presented in [102-103]. This technology enables the desired current limiting and voltage clamping functionality. The simplified version of the

Double-Clamp SM is shown in Figure 5-2 in normal operation and during the DC fault. In normal operation, the module represents an equivalent of two half-bridge SMs. The total losses are increased to some extent, due to the additional switch T5, which is normally on. DC fault current blocking will be achieved by simply turning off the additional switch.

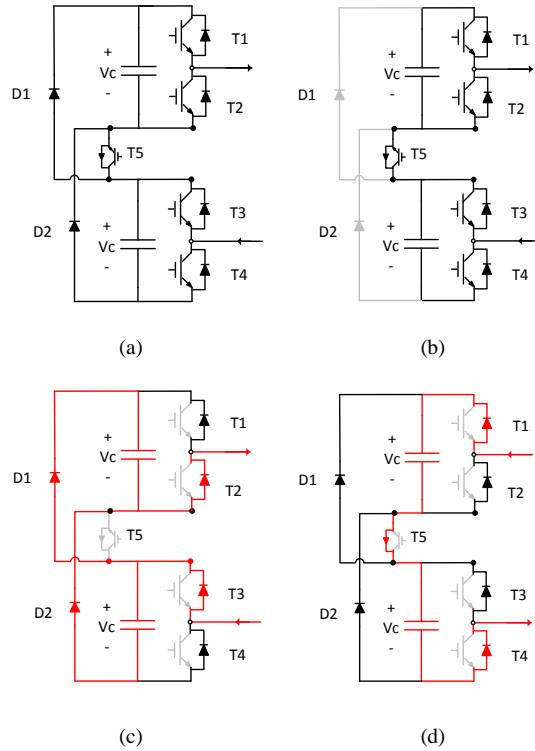


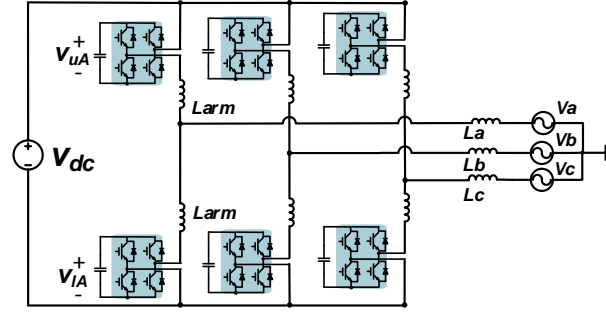
Figure 5- 2: (a) Simplified version of the Double-Clamp submodule (b) normal operation T5 is on, (c) T5 is off during fault, current limiting in positive current direction and (d) T5 is off during fault in negative current direction.

In [9], the fault current stress for power switches in the MMC is analyzed. First, a detailed theoretical study of the pole-to-pole and pole-to-ground fault in the MMC is presented, and then the fault current stress of the diode and its relation to the arm inductor size is extracted. The MMC with full-bridge power cells hasn't been attractive so far because of the higher number of semiconductors and higher semiconductor losses;

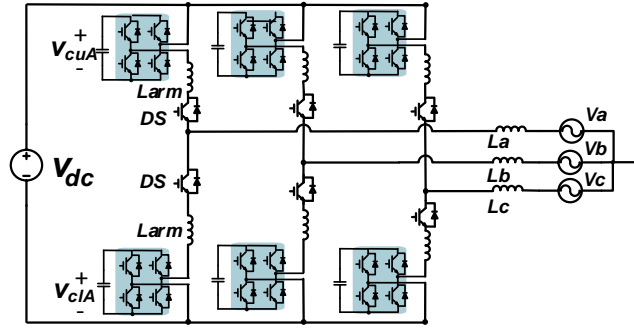
however, more studies on the AAC and its ride-through capability of DC fault is currently ongoing. The AAC consists of two substantial parts: (i) Cascaded N series H-bridge sub-modules (SMs); (ii) direction switches (DS), composed of series of IGBTs with antiparallel diodes. Each phase has two arms, conducting alternately. Each arm is comprised of a DS and CHB [21]. A comprehensive study of the DC fault ride-through capability of the AAC and its STATCOM mode of operation is carried out in [61],[104-107] A detailed control structure and comprehensive study of the DC fault blocking of the AAC and the MMC-FB is still not available in the literature.

5.3 DC Fault Analysis of MMC Full-Bridge and AAC

For simplicity, as shown in Figure 5-3, a three-phase, grid-tied MMC with full-bridge cell and an AAC with a single module per arm are considered for analysis during the pole-to-pole DC fault. The protection command for clearing the DC fault in this analysis is to turn off all the IGBTs throughout the converter. By turning off the director switches, the current will be passed through the antiparallel diode, and the rest of the circuit will be the same for both the MMC with full-bridge cells and the AAC. Since the MMC-FB and AAC have the same model during the DC fault, the extracted model will be valid for both; however, the dynamic will be different due to the different designs of the arm inductors and the power cell capacitors.



(a)



(b)

Figure 5- 3: A three- phase grid tied (a) MMC with Full-Bridge cell, (b) AAC

To analyze the fault, the following definition of voltage and current in the MMC and AAC is considered.

The AC source voltage is considered as:

$$v_A = V_m \sin(\omega t + \delta) \quad (5-1)$$

Where, δ is the phase difference between grid voltage and the pole voltage of the MMC. The phase voltage and current of the MMC is expressed as:

$$v_{ao} = V_m \sin(\omega t) \quad (5-2)$$

$$i_{ao} = I_m \sin(\omega t + \theta) \quad (5-3)$$

Where, $V_m = m \frac{V_{dc}}{2}$. By defining the output voltage, the reference voltage of the

upper and lower arm for the MMC and AAC are defined as:

$$v_{ua} = \frac{V_{dc}}{2} - V_m \sin(\omega t) \quad (5-4)$$

$$v_{ua} = \frac{V_{dc}}{2} + V_m \sin(\omega t) \quad (5-5)$$

And the upper and lower arm current will consist of the DC current and phase current in the AAC. In the case of the MMC full-bridge, the circulating current will be added to the arm currents. By assuming a balanced three-phase, and identical components in each arm, the upper and lower arm currents can be defined as:

$$i_{ua} = \frac{i_{dc}}{3} + \frac{i_{ao}}{2} + (i_{cir}) \quad (5-6)$$

$$i_{ua} = \frac{i_{dc}}{3} - \frac{i_{ao}}{2} + (i_{cir}) \quad (5-7)$$

After defining the converter voltage and currents, the converter DC fault model can be analyzed in the next step. The all fault period of the converter up to the fault current clearance time is divided into three parts:

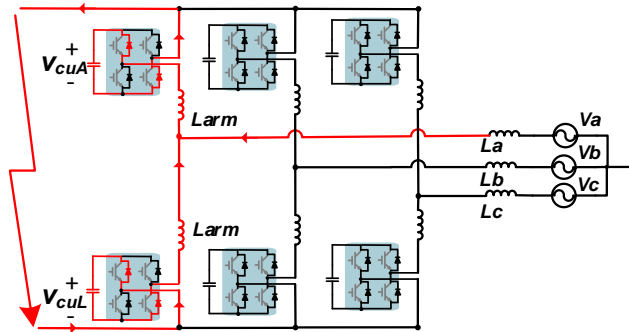


Figure 5- 4: DC Fault path through the antiparallel diodes

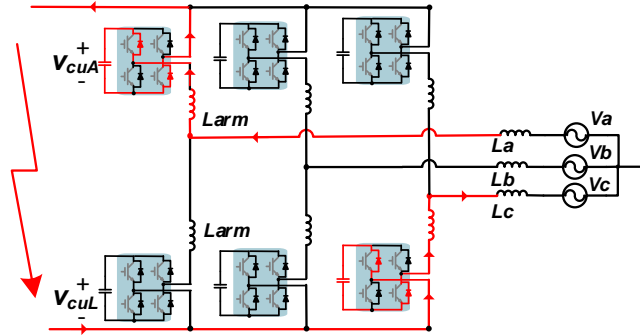


Figure 5- 5: DC Fault path at the final stage of fault clearance

5.3.1 During Fault Detection Time (t_0 to t_1)

The fault detection time is defined from the time that the actual fault happens up to the time that the fault is declared inside the converter and the protection process is begun. This time, which is typically about a microsecond to a millisecond, depends on the delay time of the voltage and current sensors and the processor, and the defined maximum fault voltage and current within the converter. The current through the converter will be increased and the capacitors will be discharged within the normal operation of the MMC-FB and AAC during DC fault. During normal operation of the MMC with FB power cells, the sum of the upper and lower voltages is equal to the DC side voltage. This is true on the condition that the negative voltage generation of the full-bridge is not required in order to have voltage greater than DC voltage at the output of the converter and that the operation of the MMC with full-bridge cells is similar to the conventional half-bridge MMC.

During the fault detection time, the upper and lower arm currents of phase a are obtained as follows:

$$i_{uA}(t_1) = \frac{i_a(t_1)}{2} + \frac{i_{dc}}{3} + \frac{V_{uA} + V_{lA}}{2L_{arm}}(t_1 - t_0) \quad (5-8)$$

$$i_{lA}(t_1) = -\frac{i_a(t_1)}{2} + \frac{i_{dc}}{3} + \frac{V_{uA} + V_{lA}}{2L_{arm}}(t_1 - t_0) \quad (5-9)$$

According to equations (5-8) and (5-9), during fault detection the upper and lower arm will be increased depending on the arm inductor size and the sum of upper and lower arm voltages.

5.3.2 During IGBT's Turned-off Time in Which Fault Currents Flow Through Diodes (t₁ to t₂)

After detecting the fault through the fault detection algorithm within the control processor of the converter, the simple command for the MMC-FB and the AAC is to set all the IGBTs to be turned-off. The current path through the diodes is shown in Figure 5-4. In this situation, the capacitor voltage will be connected in the arm negatively and the DC fault current will be blocked by the negative voltage of the capacitors. The upper and lower arm current at this time is shown in (5-10) and (5-11):

$$i_{uA}(t_2) = i_{uA}(t_1) - \frac{V_{cuA} + V_{clA}}{2L_{arm}}(t_2 - t_1) \quad (5-10)$$

$$i_{lA}(t_2) = i_{lA}(t_1) - \frac{V_{cuA} + V_{clA}}{2L_{arm}}(t_2 - t_1) \quad (5-11)$$

The fault path through the antiparallel diodes of SM makes the capacitor voltages drop negatively, and this will prevent the DC fault current from increasing further.

5.3.3 During Fault Currents' Flow Through Diodes and the Fault Current

Blocking Time (t_2 to t_3)

During fault current blocking time, the current passes through the upper or lower arm of the phase, depending on the operational point of the converter, and the arm current returns through the other phase arm as shown in Figure 5-5 until the fault current reaches zero. During this time, the arm current can be obtained by:

$$i_{uA}(t_3) = i_{uA}(t_2) - \frac{V_{cuA} + V_{clB}}{2L_{arm}}(t_3 - t_2) \quad (5-12)$$

The complete blocking of the DC fault current will occur whenever the total voltage of the capacitors in the fault path become higher than the line-to-line AC voltage. Therefore, the time of complete DC fault current clearance corresponds with the following condition:

$$v_{stackA} + v_{stackC} > v_{ac} \quad (5-13)$$

The fault current waveform during each time interval up to the complete DC fault clearance for both the MMC with full-bridge power cells and the AAC is shown in Figure 5- 6.

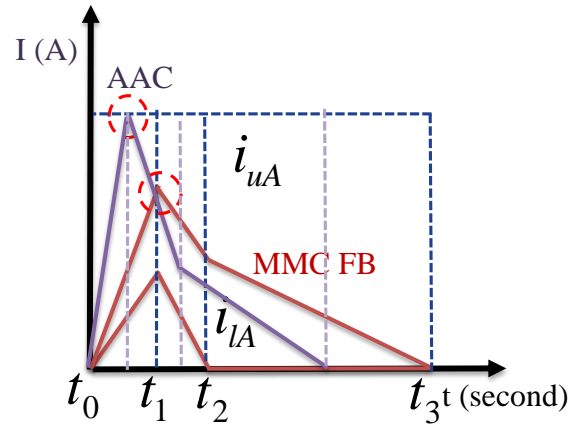


Figure 5- 6: the upper and lower arm current for Full-Bridge MMC and AAC

Since in the AAC, there is no circulating current from alternating the phase current within the arms, the inductor size will be lower than the MMC and the capacitor size will be about half that of the MMC [62]. Therefore, the AAC will have a higher peak DC fault current but a faster transient during the fault.

5.4 DC Fault Closed Loop Control Strategy of MMC Full-Bridge and AAC

Both the MMC with full-bridge sub-modules and the AAC can generate negative voltage in their arms, an advantage which helps these converters remove DC fault. Even when changing the functionality of the converter during the DC fault, these converters can operate as a STATCOM [104-107]. The full-bridge MMC can operate as two parallel Cascaded H-Bridge converters during the DC fault. The AAC can have three modes of STATCOM depending on whether the director switches are opened or closed. In the STATCOM mode, the voltage reference of the cascaded H- Bridges should be changed such that the CHB generates the voltage equal to and in the same direction of the grid

voltage. This chapter concerns only the medium voltage application of the MMC and AAC. So the ability of the converter to inject reactive power to the grid is no longer of interest. However, a control strategy corresponding with the output closed-loop control of the converter is required during the fault, mainly to maintain the capacitor voltage at a specified value and limit the DC fault current. The closed-loop control of the MMC with H-Bridge cells and the AAC during the DC fault is shown in Figure 5-7.

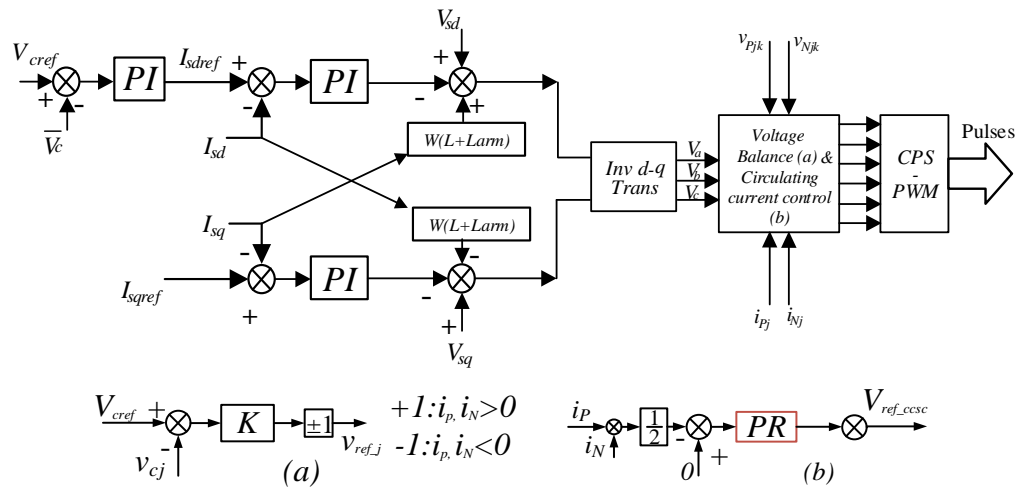


Figure 5- 7: The closed-loop control of FB MMC and AAC during the DC Fault

Control strategy during the fault is similar to the closed-loop control of the MMC and AAC [63], except in this situation the d axis reference current is about zero and it is fed by capacitor voltage control loop to maintain the capacitor voltage of each SM at its nominal value. In this mode, the capacitor voltage balance control and circulating current are design requirements for stable operation of the converter during the fault. Since there is no requirement to inject reactive power to the grid in the medium voltage DC application, the reference of the q axis current is set to zero. The polarity of the d-q axis current can be changed in inverter or rectifier operation mode of the converter.

Table 5- 1: Case study MMC with FB and AAC specifications

Parameters	MMC-FB	AAC
Power rate	600kW	600kW
DC Line Voltage	5kV	4kV
Line to Line Voltage	3.3 kV	3.3 kV
RL grid	1 Ω 1mH	1 Ω 1mH
Switching Frequency	1kHz	1kHz
Module Rated Voltage	637 V	637 V
No of Module	8	4
Pole Voltage Levels	9	9
Cell Cap size for $\Delta V < 40$	6mF	3mF
Arm Inductor	3mH	600mH

5.5 Simulation Result

In this section, the operation of the MMC with full-bridge power cells and the AAC with closed-loop control under DC fault is simulated using Simulink/Matlab. To provide an accurate simulation, the DC bus short circuit is modeled by a small resistor that can be in order of 10 to 0.001 ohms. The converter is operating in grid-tied inverter mode prior to the fault occurrence. The case study parameters are specified as presented in Table 5-1. The simulation is run for different scenarios, and the following facts are assumed through the simulation of each fault scenario. First, a time of 10 msec is considered for a fault detection time, during which period the peak DC fault current takes place and the power cell capacitor voltage is discharged. Secondly, the short circuit resistor, R_{sc} is assumed to be 0.01 Ω , and for ideal conditions, the case with R_{sc} 10 Ω is

simulated as well. A very small inductor is used for a more accurate model of the short circuit. The assumed DC fault scenario is shown in Figure 5-8. Each of the following cases are considered for the simulation analysis:

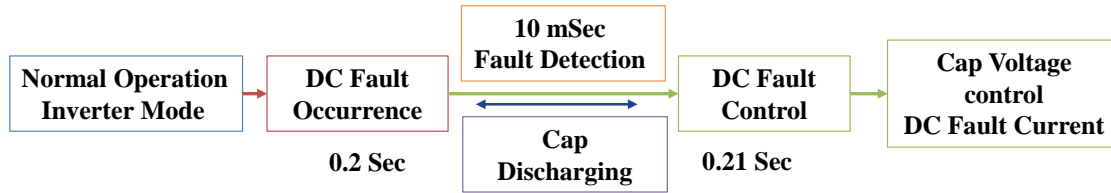


Figure 5- 8: DC Fault scenario for Full-Bridge MMC and AAC

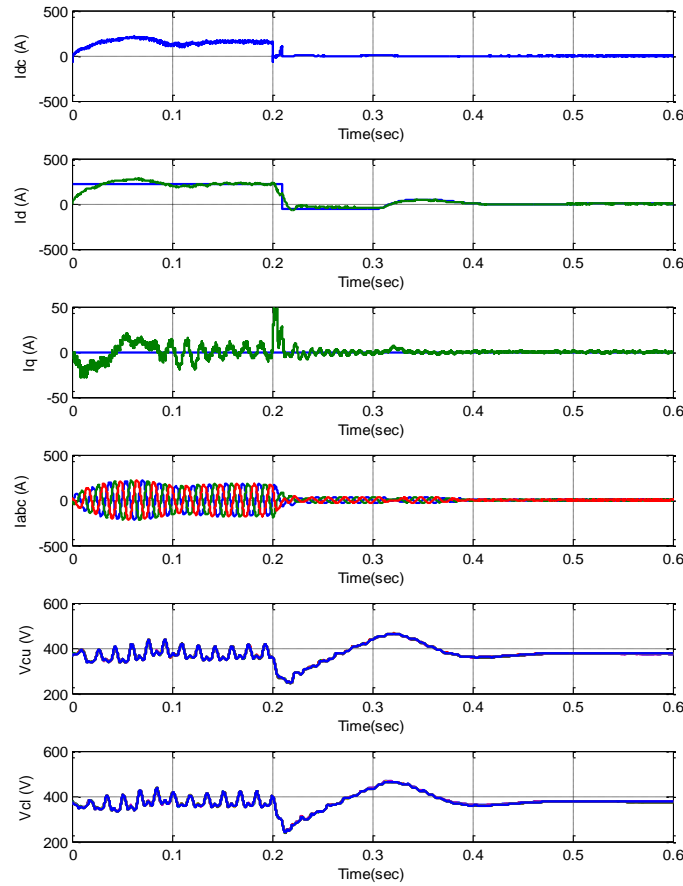


Figure 5- 9: DC Fault simulation under Rsc 10 Ω for MMC-FB

5.5.1 DC Fault Simulation With Rsc 10 Ω for MMC-FB

For this state, DC fault behavior of the MMC-FB is simulated with the assumption of using a higher short circuit resistor. The DC fault current, three-phase AC current, d-q axis current, and cap voltage are shown in Figure 5-9 during the normal operation and during DC fault. Since the short circuit resistor is high, the 2nd harmonic circulating current is damped to the zero in a few cycles and the fault clearance time is soon achieved.

5.5.2 DC Fault Simulation With Rsc 0.01 Ω for MMC-FB

The simulation results of this case are shown in Figure 5-10. A similar scenario occurs as that shown in Figure 5-8. In this situation, which occurs more often where the positive and negative rail terminals are connected with fewer fault resistors, the circulating current will be damping through the oscillatory arm inductor and SM capacitors. The amount of peak current still depends on the design of the arm inductor and the capacitor for the MMC, as well as fault detection time.

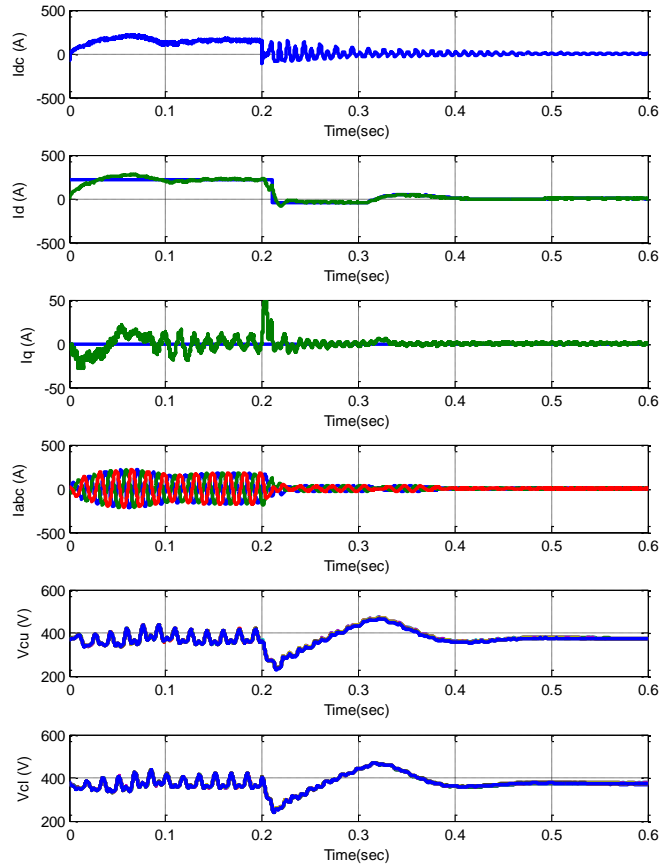


Figure 5- 10: DC Fault simulation under $R_{sc} 0.01 \Omega$ for MMC-FB

5.5.3 DC Fault Simulation With $R_{sc} 0.01 \Omega$ for AAC

In this section, the AAC with specified parameters is simulated under the defined DC fault scenario. The power rating of the AAC is the same as the MMC-FB in order to provide further comparison of the performance of the AAC and MMC-FB under the DC fault condition. In the STATCOM operation mode of the AAC there are three scenarios, depending on the director switches' on or off states [61], [104-107]. The case where the AAC operates alternately under DC fault is not practical, as it results in higher power losses. So, in this paper, the AAC configuration under the DC fault is simulated assuming the conditions that one or both of the upper and lower arm CHBs are utilized by turning

both on or via the DS, and that alternating between the upper and lower arms no longer exists. To have the same conditions for the MMC-FB, the AAC under fault is considered to be transformed to two parallel CHBs, which in this mode causes DC fault blocking time to be faster. The simulation result is shown in Figure 5-11 for the DC current, d-q axis output current, three-phase currents, and the capacitor voltages. The upper and lower arm currents are shown in Figure 5-12 as well.

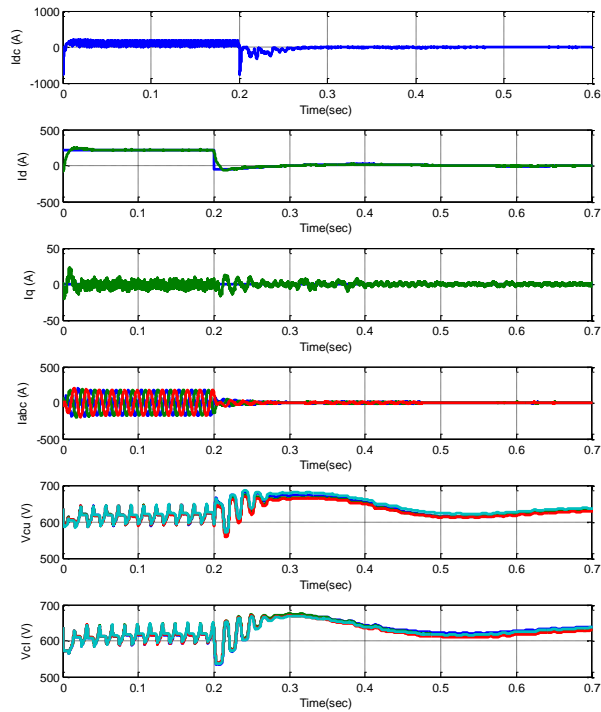


Figure 5- 11: DC Fault simulation under Rsc 0.01 Ω for AAC

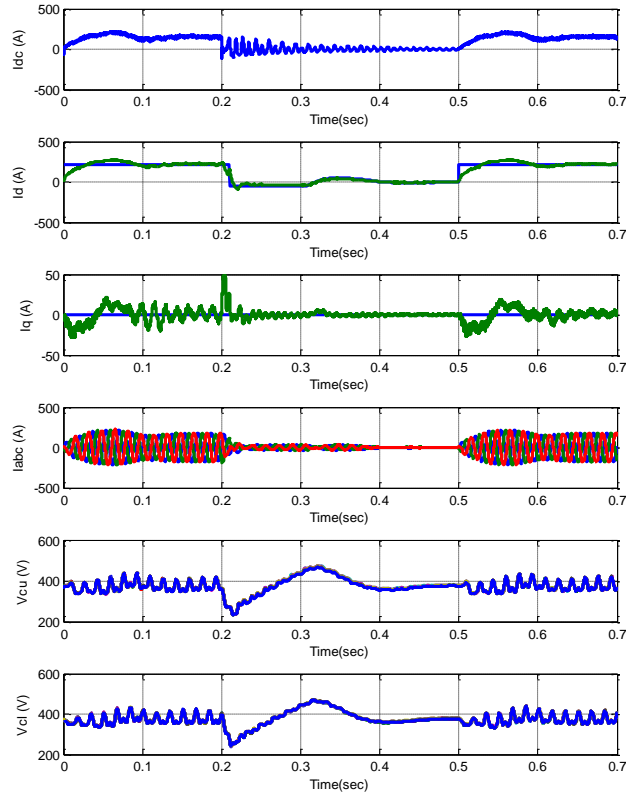


Figure 5- 12: DC Fault interruption simulation under $R_{sc} 0.01 \Omega$ for MMC-FB

5.5.4 DC Fault Interrupt Simulation With $R_{sc} 0.01 \Omega$ for MMC- FB

Some of the DC faults would be removed after some cycles. Therefore, the normal operation of the converter after the fault clearance is of concern. Hence, in this section, the DC fault interrupt and normal operation of the converter after the DC fault is illustrated. In this scenario, the DC fault is going to be removed after 0.5sec and the DC fault has occurred, as seen in Figure 5-8, prior the fault clearance. In Figure 5-13, the DC fault interrupt simulation result for the DC fault current, the d-q axis, and three- phase output current and the capacitor voltages are shown.

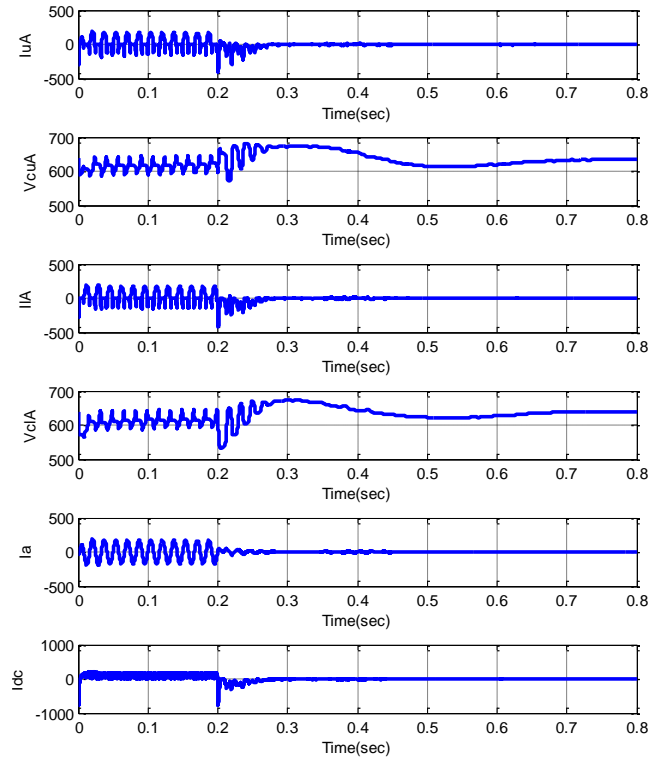


Figure 5- 13: DC Fault simulation under $R_{sc} 0.01 \Omega$ for MMC-FB

As far as a comparison, as shown by the MMC-FB and AAC simulation results, the AAC peak DC fault current is about 600A, whereas the MMC-FB has a peak DC fault current of about 60A. The reason for the difference is that in the MMC, since there is a circulating current, inductor size is chosen based on its ability to provide the most desirable circulating current. The bulky inductor design means a considerable reduction of peak current during the DC fault. However, in the AAC, preference is given for an inductor with a low enough size to provide ZCS for the director switches, thereby improving the efficiency and size of the converter. This also makes the converter susceptible to high peak DC fault current, which imposes further stress over the antiparallel diodes of the IGBTs. Thus, in the AAC, the fault detection time should be small enough to avoid the DC fault current increase from the specified fault values.

5.6 Conclusions

In this chapter, the DC fault ride-through capability of the MMC, particularly the MMC with full-bridge power cells, and the recently developed AAC is investigated. Theoretical fault analysis is performed to show the intrinsic ability of the MMC with full-bridge cells to contain the DC-side short-circuit fault current. Then, closed-loop control of the MMC-FB and AAC is employed during the DC fault to substantially control the capacitor voltage and provide fault current limit. The simulation is carried out to illustrate the performance of the converters' operation during the DC fault in the MMC-FB and the AAC. Simulation results show that the AAC, since it has a lower arm inductor and power cell capacitor in its structure, has a faster transient response; however, it suffers from higher peak DC fault current. The simulation is performed for a high and low short-circuit resistor and for the case where there is a DC fault interrupt, the operation of the converter is shown with the adopted DC fault current control. The DC fault blocking capability of the MMC-FB and the AAC is a promising factor for providing intrinsic DC fault-blocking in high and medium voltage applications.

Chapter 6 Summary, Conclusions and Future Work

6.1 Summary

In this thesis, modeling, control, and design consideration was performed for the modular multilevel converters with the main focus on the Alternate Arm Converter (AAC) and the MMC with half-bridge power cells. The basic principles of the formation of MMC's and the second generation of the modular multilevel converters, called hybrid Alternat Arm Converters, was discussed. The mathematical approach for modeling the behavior of the converter was extracted and the switching, average, and DQ model of the MMCs were obtained. Then, the closed-loop control approach of the MMC and the AAC was illustrated and the average and individual capacitor voltage balance control were shown. The existence of circulating current in the MMC was discussed for and the Circulating Current Suppressing Control (CCSC) was designed using the Proportional Quasi-Resonant (PQR) controller. In chapter 4, design considerations for MMCs were presented. The reliabilty-oriented capacitor bank design for MMCs using the Markov-State Space model was discussed. The design of the arm inductor and capacitor bank was explained and the optimum switching frequency analysis of the MMCs was carried out by investigating the reliability of the converter. One of the important factors for the AAC is the operation of the Director Switches (DS) within the converter. Hence, the Zero Current Switching operation of the DS for the AAC was illustrated and the design of the

arm inductor for the AAC was presented. The main advantage of the AAC over the MMC with half-bridge power cells is the DC fault ride-through capability, which can be attained by full-bridge power cells. The DC-fault ride-through capabilities of the AAC and the MMC with full-bridge cells were studied and the DC-fault control approach for medium voltage application of the AAC and the MMC with FB cells were proposed. The performed mathematical analysis was verified by the simulation analysis using MATLAB/SIMULINK in each part.

6.2 Conclusions

The main contributions of this work are presented as follows with the corresponding conclusions:

1- The DQ model of the modular multilevel converter can be obtained from the average model to ease the design of the controller. The AAC average model has director switch functionality, but the average model and the DQ model of the AAC also has nonlinear complications.

2- The control method for the AAC is expanded upon, based on the same control approach used for the MMC with half-bridge cells.

3- High reliability capacitor bank design for the MMCs was done using component and system-level reliability modeling. The Markov model is proposed for use in modeling the capacitor bank for the MMC. The reliability function of the capacitor bank was extracted and compared for three different capacitor bank designs using Aluminium Electrolytic and film capacitors. Using the Markov model, the failure rate of

the system for each case was estimated and, finally, a comparison among the results of the reliability modeling of the systems was performed using the following three reliability modeling techniques: part-count, combinatorial, and Markov model. The results show that reliability modeling using the Markov model tends to be closest to the realistic reliability model of the system.

4- The reliability oriented switching frequency analysis for the modular multilevel converters was carried out. The stress analysis of the MMC for phase-arm currents and voltages, as well as the converters' output voltage and current, was done along with an evaluation of the impact of switching frequencies harmonic components in the low switching rate. The effect of a circulating current suppressing controller was also investigated. The switching frequency evaluation showed an optimum point favoring a medium switching rate, as the circulating current harmonic content was seen to increase at lower frequencies, resulting in heightened conduction losses for the devices and a higher voltage ripple for the power-cell capacitors.

5- A design and switching power losses comparison between the AAC and half – bridge MMC in a sample case study was done. The results show that the AAC, despite having a higher number of switches, will have fewer switching power losses, mainly due to the lack of circulating current and load power alternating. However, AACs also suffer from high switching power losses in the director switches.

6- The DC fault ride-through capability of the MMC, particularly for the MMC with full-bridge power cells, and the recently developed AAC was investigated. Theoretical fault analysis was performed to show the intrinsic ability of the MMC with full-bridge cells to contain the DC-side short-circuit fault current. Closed-loop control of

the MMC-FB and the AAC was then employed during the DC fault to substantially control the capacitor voltage and provide fault current limit. The simulation result was carried out to illustrate the performance of the converter's operation during the DC fault in the MMC-FB and the AAC. Simulation results show that since the AAC has lower arm inductor and power cell capacitors in its structure, it has a faster transient response. However, it also suffers from higher peak DC fault current. The simulation was performed for high and low short-circuit resistors and for the case where there is a DC fault interrupt, the operation of the converter is shown with the adopted DC fault current control. The DC fault blocking capability of the MMC-FB and the AAC is promising, as it provides intrinsic DC fault for these converters in high and medium voltage applications.

6.3 Future Work

In order to finish the study on MMCs with regard to modeling, control and design considerations, as well as the DC fault ride-through capability of the MMC, the following works should be conducted in the future:

- 1) Nonlinear modeling of the AAC to attain the average and the DQ model along with additional analysis in order to understand the interaction between the arm quantities.
- 2) Study of new control techniques to evaluate the required overall time for the AAC.
- 3) Experimental verification of the proposed analysis and methods for the AAC and the MMC.

- 4) Reliability modeling verification of the capacitor bank in practice, using acceleration tests.
- 5) AAC hardware setup testing to verify the operation of the AAC and the validity analysis of the utilized control techniques for the capacitor voltage balance and the overlap time.
- 6) Switching frequency design verification of the MMC taking into consideration the trade-off between the capacitor voltage ripple and semiconductor power losses.
- 7) Evaluation of the DC fault control technique proposed for the MMC with FB and AAC experimental verification using the prototype hardware.

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