MOS-BIPOLAR COMPOSITE POWER SWITCHING DEVICES

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(ABSTRACT)

Two MOS-Bipolar composite power semiconductor switching devices are proposed and experimentally demonstrated. These devices feature high voltage and high current capabilities, fast switching speeds, simple gate drive requirements, savings in chip area, reverse bias second breakdown ruggedness and large safe operating areas. Application characteristics of the devices for high frequency power inverter circuits are discussed. Monolithic integration of the two composite devices are also proposed.

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Chapter I

INTRODUCTION

In recent years, power semiconductor devices have undergone tremendous growth. In addition to traditional power devices such as Thyristors (SCRs), Bipolar Power Transistors (BJTs), Bipolar Darlington Transistors and power MOSFETs, new power semiconductor devices are being proposed [1.1]: Junction Field Effect Transistors (JFETs), Static Induction Transistors (SITs), MOS-Gated Thyristors (MOS-SCRs), Field Controlled Thyristors (FCTs), Gate Turn-off Thyristors (GTOs), and Insulated Gate Transistors (IGTs by G.E., Conductivity Modulated MOSFETs or COMFETs by RCA, Gain Enhanced MOSFETs or GEMFETs by Motorola), etc. These devices can be classified into two basic types: Bipolar and FET. Generally speaking, bipolar devices offer advantages such as a large current conduction capability and a low conduction voltage drop. FET devices, on the other hand, feature high switching speeds and a simple drive requirement. Very recently, there has been a trend toward attempting to combine the advantages of the BJT and the FET into a single device. The MOS-SCR and the IGT mentioned above are two such examples.

In this dissertation, two MOS-Bipolar composite devices are proposed. One device consists of a BJT and two power MOSFETs. The BJT is gated on and off by the two power MOSFETs, hence, it is referred to as "FET-Gated Bipolar Transistor" or "FGT". The other is composed of a GTO, an IGT and a MOSFET. This device is named "Insulated Gate Turn-off Thyristor" (IGTO). Both FGTs and IGTOs are intended for high voltage, high current and high frequency applications. Because of the basic conduction mechanism, the IGTO is intended for even higher voltage applications than the FGT (1000V vs. 400V).

The results presented in this dissertation have been accumulated over the past four years [1.2] - [1.6]. Some were published in IEEE Journals by the author. With the presentation of this dissertation, the FGT configuration is introduced in Chapter II. Description of the basic operating principle and selection of the various individual components will also be given. Experimental results prove the feasibility of the FGT. In Chapter III, the IGTO configuration is presented with experimental results. Application characteristics of the two composite devices are discussed in Chapter IV. It should be noted that all the experimental results presented were obtained by using

discrete devices to form the composite devices. Monolithic integration of the composite devices is beyond the scope of this dissertation; however, conceptual monolithic structures of both the FGT and the IGTO are proposed in Chapter V. Finally, Chapter VI concludes the dissertation with suggestions for future work.

Chapter II

THE FET-GATED BIPOLAR TRANSISTOR

In this chapter, a composite switching power device consisting of a bipolar power transistor (BJT) and power MOSFETs is presented. This composite transistor combines the advantages of both the BJT and the MOSFET into a single power switching element. The intent of the composite device is for high voltage, high current and high frequency applications where neither the single MOSFET nor the single BJT is technically suitable or economically feasible.

A brief review of the comparison between a bipolar power device and a power MOSFET will be given at the beginning of this chapter. A good understanding of the differences between the two types of power devices makes it easier to appreciate the composite device proposed. The new composite device configuration will be described next, followed by the operating principle and discussions of its advantages and disadvantages. Experimental results obtained by using discrete devices to form the composite transistor will also be presented. This new device will be referred to as FET-Gated Bipolar Transistor (FGT) throughout the dissertation.

2.1 COMPARISONS OF BIPOLAR POWER TRANSISTORS AND POWER MOSFETS

Table 2.1 summarizes some basic differences between bipolar power transistors and power MOSFETs. Each category of comparison is briefly described in this section.

2.1.1 Conduction Mechanism

The conduction current of a BJT is composed of the diffusion current and the drift current due to the minority carriers. In contrast, a MOSFET conducts the current by majority carriers only.

2.1.2 Drive Requirement

A bipolar transistor is controlled by an input current while a MOSFET is controlled by an input voltage. Because the current gain of a bipolar power transistor is typically in the range of 10, the base drive has to supply an appreciable input current. To drive a MOSFET, only charging and discharging currents for the MOSFET input capacitance are needed. Therefore, the drive circuit is simpler for a MOSFET than for a BJT.

TABLE 2.1

Comparisons of Bipolar Power Transistors and Power MOSFETs

Comparison	Bipolar	MOSFET
Conduction Mechanism:	Minority Carriers	Majority Carriers
Drive Requirement:	Current Control	Voltage Control
Chip Area: (Same Voltage and Conduction Drop)	Small	Large
Relative Cost:	Low	High
Conduction Drop: (Same Voltage and Chip Area)	Low	High
Switching Speed:	Slow (Temperature-dependent)	Fast (Temperature-independent)
Surge Capability:	Low	High
Paralleling:	Difficult	Easy
Reverse Bias Second Breakdown:	Observed	Not Observed

2.1.3 Chip Area

To achieve an equivalent conduction voltage drop for the same voltage and current ratings, the chip area of a bipolar power transistor can be made smaller than that of a power MOSFET. The conductivity modulation mechanism in the BJT contributes to the smaller chip area requirement. Chip areas of both the BJT and the MOSFET, however, increase rather rapidly with the voltage rating. The chip area increases as the 2.5 power of the device voltage rating [2.1] for devices having breakdown voltages above 200V.

2.1.4 Relative Cost

The device cost is mainly related to the chip area requirement and the manufacturing process. Because a power MOSFET requires a larger chip area and a more involved manufacturing process, it is more costly than a comparable bipolar power transistor.

2.1.5 Conduction Drop

For the same voltage rating and chip area, the conduction voltage drop of a bipolar power transistor is

less than that of a power MOSFET. Again, this is due to the conductivity modulation effect associated with the bipolar power transistor [2.2]. Consequently, the power MOSFET has to dissipate more power during conduction due to its higher forward voltage drop.

2.1.6 Switching Speed

Being a majority carrier device, the power MOSFET is not plagued by the long storage time accompanying the bipolar power transistor during turn-off. The power MOSFET can usually be turned off in sub-microseconds and the switching time is relatively temperature-independent [2.3]. By contrast, a bipolar power transistor has relatively long temperature dependent storage and fall times. The faster switching speed reduces switching losses.

2.1.7 Surge Capability

Should the load vary such that the collector current suddenly increases and the base current is not able to increase proportionally to keep the BJT in the saturation region, failure will usually occur in the BJT. This catastrophic effect does not usually afflict a power MOSFET because it is driven by a voltage source.

2.1.8 Paralleling

The ON-resistance of a power MOSFET has a positive temperature coefficient. If one of several paralleled power MOSFETs conducts a higher current than the rest, its ON-resistance will increase. Therefore, the current will be redistributed to be equally shared. Conversely, the bipolar power transistor has a negative temperature coefficient and current hogging or thermal runaway will follow due to the imbalanced conduction current.

2.1.9 Reverse Bias Second Breakdown

Reverse biasing is frequently used to turn off bipolar power transistors. This method can reduce storage and fall times if the base drive circuit is properly designed. However, the problem of Reverse Bias Second Breakdown (RBSB) has to be taken into account, otherwise the BJT may be destroyed [2.4]. No RBSB has been observed in regard to the failure of power MOSFETs.

2.2 FGT DEVICE CONFIGURATION

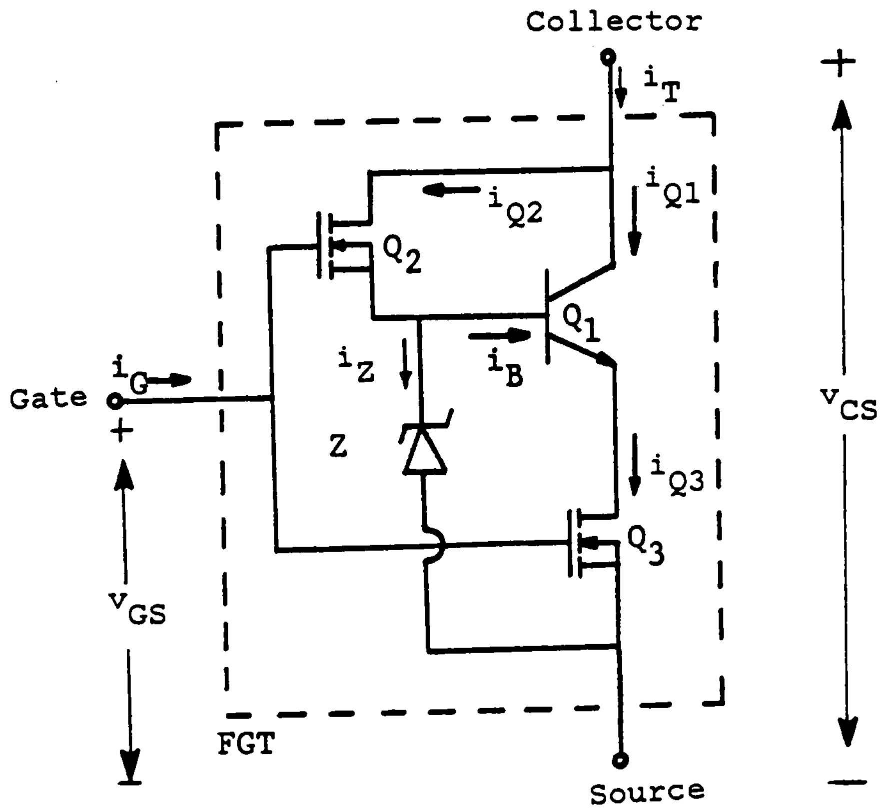
Figure 2.1 shows the schematic diagram and associated current waveforms of a FET-Gated Bipolar Transistor (FGT), in which Q_1 is the main bipolar power transistor, Q_2 and Q_3 are power MOSFETs, and Z is a zener diode. The gates of Q_2 and Q_3 are connected to form the gate (Node G) of the FGT, the collector of Q_1 and the drain of Q_2 are connected to form the collector (Node C) of the FGT. The source terminal (Node S) of the FGT is formed by connecting the source of Q_3 and the anode of Z. As can be seen from Figure 2.1, Q_1 is in a Darlington configuration with Q_2, and is in an emitter-open configuration with Q_3.

2.3 FGT OPERATING PRINCIPLE

The output I-V characteristics of an FGT are shown in Figure 2.2. The operating principle of an FGT is discussed in the following.

2.3.1 Turn-on

When the gate voltage is high, both Q_2 and Q_3 conduct. Q_2 supplies the base current to Q_1 through the base-emitter



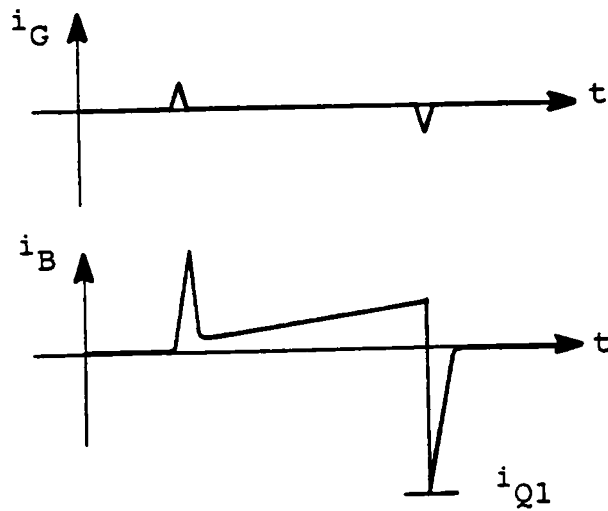
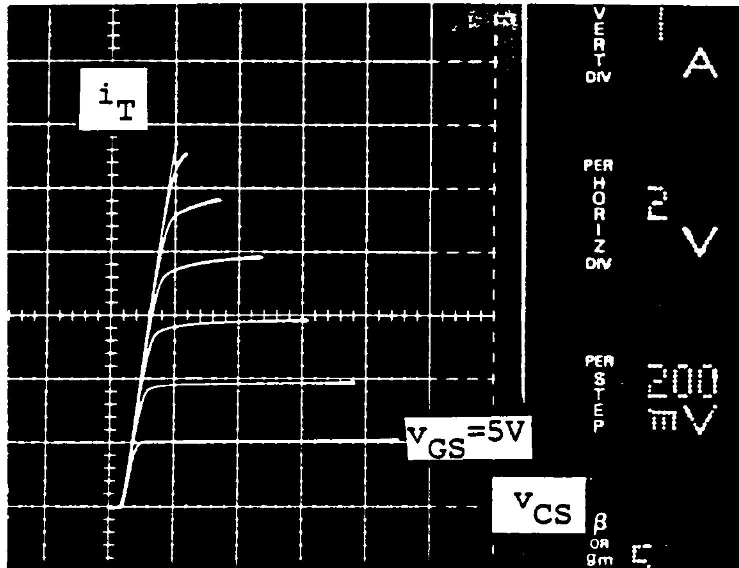


Figure 2.1: FGT Configuration and Associated Current Waveforms



i_T:	1 Ampere/Division
v_{CS}:	2 Volts/Division
v_{GS}:	200 Millivolts/Step
Q_1:	General Semiconductor 2N6655
Q_2:	RCA RFP3N50
Q_3:	Siemens BUZ15
Z:	TCG135A

Figure 2.2: FGT I-V Characteristics

junction of Q_1 to turn on Q_1. The FGT is, therefore, turned on by a voltage drive. The base current needed to drive Q_1 is actually derived from the load instead of the gate drive circuit. At the instant of turn-on, due to the fast switching of Q_2, most of the load current goes through Q_2, which provides an initial base current "kick" to Q_1. Because of the current kick, the FGT can be turned on very quickly.

2.3.2 Conduction

Once the FGT is turned on, Q_1 is in the quasi-saturation state [2.5] due to its Darlington configuration with Q_2. Therefore, the base drive current of Q_1 is proportional to the collector current of Q_1. The load current distribution depends on the DC current gain of Q_1 and the ON-resistance of Q_2. Q_3 carries the total current comprising of the Q_1 and Q_2 currents during the conduction state.

2.3.3 Turn-off

When the gate voltage is low, both Q_2 and Q_3 are turned off. The collector current of Q_1 is forced to flow out of the base-collector junction of Q_1 to the ground through the zener diode, Z. The reverse current gain equals unity, which results in rapid emitter-open turn-off [2.6]. Due to the emitter-open turn-off scheme, Q_1 is free from RBSB stemming from emitter current crowding in conventional reverse bias turn-off [2.7].

As seen in Figure 2.1, the base current provides an ideal base drive for the high frequency operation of a bipolar power transistor [2.8]. Large current spikes are available for rapid turn-on and turn-off and a proportional base drive is provided during the conduction period. It should be pointed out that such an ideal base drive current is difficult to obtain from a conventional base drive circuit. In the FGT configuration, however, it is an inherent characteristic accomplished with very small gate current pulses during switching. In other words, the base current of Q_1 is effectively derived from the load circuit instead of a gate drive power supply.

2.3.4 Purpose of Zener Diode Z

The zener diode, Z, is used for two purposes. One is to provide the reverse current path for the base current of Q_1 during turn-off. The other is to provide the current path for discharging the Q_2 gate capacitance at turn-off.

2.4 SELECTION OF COMPONENTS

For an FGT with a voltage rating of V_X and a current rating of I_X, the individual components should be selected according to the following guidelines.

2.4.1 Selection of Q1

Since Q_1 is turned off by the emitter-open scheme, RBSB is avoided. The device can, therefore, safely operate up to its collector-base junction breakdown voltage rating, BV_{CBO} [2.7]. The BV_{CBO} of Q_1 should be used for the FGT's voltage rating, V_X. During the conduction period, the load current is shared by Q_1 and Q_2 due to the Darlington configuration. Therefore, the collector current of Q_1 should be rated at $I_C=I_X/(1+1/\beta)$, where β is the DC current gain of Q_1 at I_C. Due to the emitter-open turn-off, the base terminal of Q_1 should handle the peak collector current.

2.4.2 Selection of Q2

Since Q_2 is connected across the collector and the base of Q_1, the drain-source breakdown voltage of Q_2, BV_{DSS}, should be rated at V_X. During the conduction period, the drain current of Q_2, i_D, is equal to the base current of Q_1.

The load current distribution between Q_1 and Q_2 during the conduction period depends on the DC current gain of Q_1 and the ON-resistance of Q_2. For a bipolar power transistor, the DC current gain is typically in the range of 5 to 10 [2.9]. Therefore, Q_2 conducts about one-tenth to one-fifth of the load current during the conduction state. At the instant of turn-on, however, Q_2 draws a large portion of the total load current because Q_2 turns on much faster than Q_1. This turn-on current spike provides a base current kick to rapidly turn on Q_1. The current distribution between Q_1 and Q_2 at turn-on depends on the turn-on delay time of Q_1. Generally speaking, the current ratio at this moment is about 2 to 1 (Q_1 : Q_2). In the theoretically worst case, Q_2 takes all the load current at turn-on. As a result, the surge current rating of Q_2 has to be much greater than its steady state value. Fortunately, this surge current requirement can be satisfied by the existing

MOSFETs. The typical surge current capability for a power MOSFET is about ten times that of the continuous current rating [2.10]. Therefore, with Q_2 selected according to the steady state current requirement, it also meets the turn-on surge current spike rating.

2.4.3 Selection of Q3

During the OFF state, most of the applied voltage is across Q_1 allowing a low voltage rating to be used for Q_3. This is because the depletion layer of the P-N junction of Q_1 establishes a potential barrier which shields the drain potential of Q_3 from the supply voltage [2.11]. The variation of the MOSFET drain voltage with the supply voltage for an emitter-open configuration is shown in Figure 2.3. Here the drain voltage of Q_3 is less than 50V even at a supply voltage of 1000V. Therefore, a MOSFET having a breakdown voltage rating of 50V will serve well as Q_3. The drain current of Q_3 should be rated at the FGT current rating, I_X, since Q_3 has to carry the total load current during conduction period.

It is clear from the above discussion that Q_2 is a high voltage but low current MOSFET, Q_3 is a high current but low

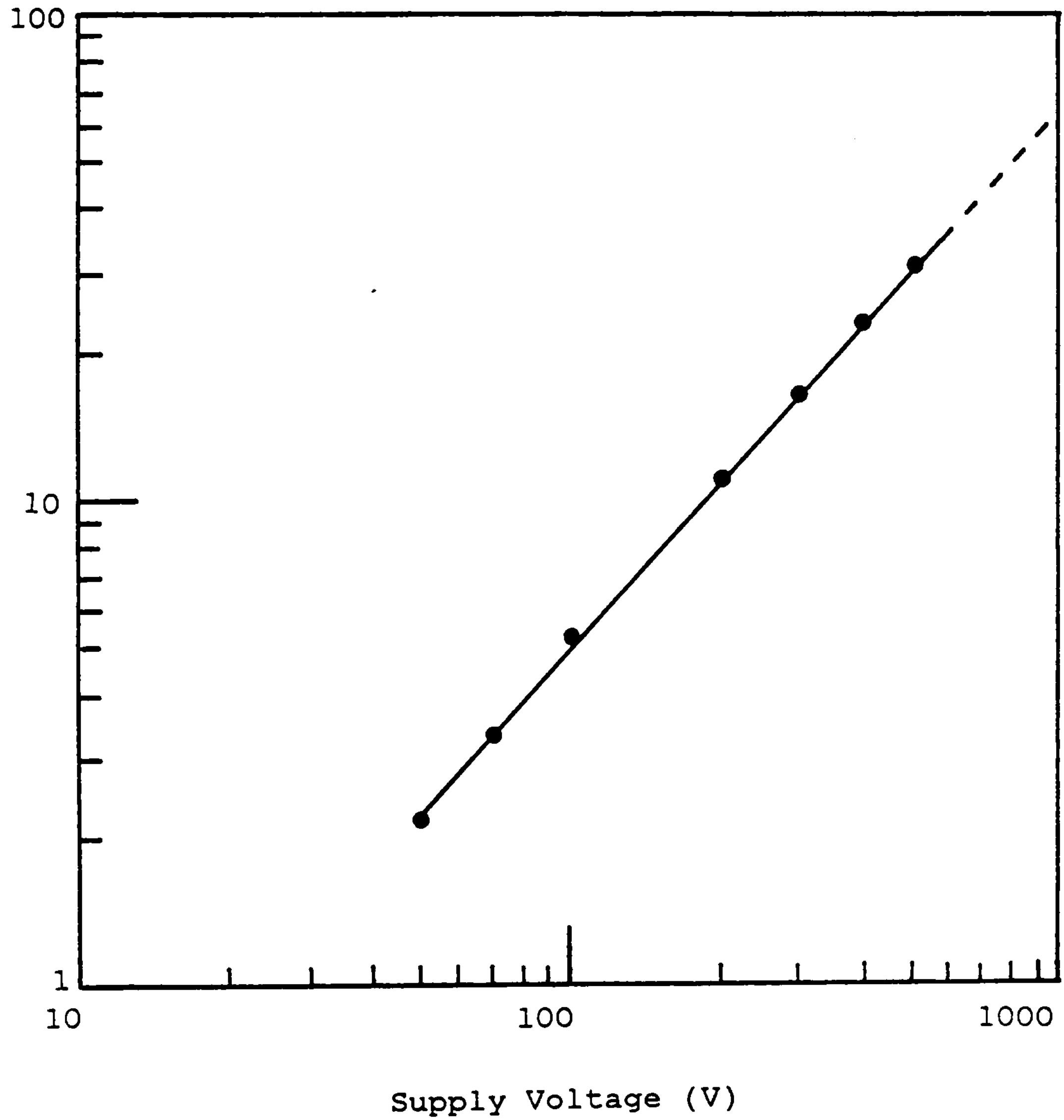


Figure 2.3: Variation of Q3 Drain Voltage Versus Supply Voltage During OFF State in Emitter-open Configuration [After 2.11]

voltage MOSFET, and the FGT is a high voltage and high current device with the voltage rating and the current rating matched to Q_2 and Q_3, respectively. Therefore, a high-current voltage-controlled FGT can be constructed by using two MOSFETs with relatively small chip areas and a BJT with a moderate chip area. As will be shown later in Tables 2.3 and 2.4, the saving in the chip area is very significant compared to a high voltage high power MOSFET.

2.4.4 Selection of Z

During the conduction period, the zener diode breakdown voltage must be greater than the sum of the base-emitter saturation voltage of Q_1 and the voltage drop of Q_3. In this way the base current of Q_1 is not diverted through the zener diode. During the Q_1 storage time, all the load current is flowing through the zener diode. The zener diode surge current is therefore rated at I_X.

Power dissipation of the zener diode, which normally limits the choice of the zener diode, Z, is determined by the zener breakdown voltage, V_Z, the FGT current rating, I_X, and the FGT operating frequency. The reverse gate-source voltage applied to Q_2 during turn-off is equal to the

difference between the zener clamping voltage and the gate voltage. The lower the zener clamping voltage, the lower will be the reverse voltage across the gate-source junction of Q_2. The reverse gate-source breakdown voltage of a power MOSFET is usually 20V [2.3]. Therefore, the zener breakdown voltage should be as small as possible, so long as it does not divert the current during the FGT conduction period.

2.5 EFFECTS OF COMPONENT SELECTION ON FGT PERFORMANCE

The guideline for selecting the components outlined above is rather general. Once the guideline is followed, the voltage and the current ratings should be satisfied. However, the switching time and the conduction drop of the FGT will be affected by the components selected as described below.

2.5.1 Switching Time

2.5.1.1 Turn-on Time

If Q_2 has a larger ON-resistance, the turn-on process of Q_1 will be slower, hence the FGT is turned on more slowly.

2.5.1.2 Turn-off Storage time

The selection of the ON-resistance of Q_2 affects the storage time of Q_1. Because of the Darlington configuration of Q_1 and Q_2, Q_1 is in quasi-saturation during conduction. The MOSFET Q_2, with a higher ON-resistance, poses a higher voltage drop across the collector-base junction of Q_1. Q_1 is, therefore, operated farther away from deep-saturation so that the storage time of Q_1 will be shorter.

2.5.2 Conduction Drop

Although a Q_2 with a high ON-resistance may reduce the storage time of Q_1, a higher conduction drop for Q_2 results in a higher conduction drop of Q_1. This makes the FGT's conduction drop higher.

2.6 ADVANTAGES AND DISADVANTAGES OF THE FGT

The advantages and disadvantages of the FGT are described in the following subsections.

2.6.1 Reverse Bias Second Breakdown Ruggedness

Reverse bias second breakdown of a bipolar power transistor occurs during turn-off due to the emitter current crowding phenomenon [2.4]. During the conventional reverse bias turn-off of a bipolar power transistor, a large lateral voltage drop in the base region under the emitter finger delays turn-off of the center of the emitter finger, due to the distributed base resistance. Accordingly, the emitter current focusing toward the center of the emitter finger forms a current filament as other areas cut off. The current filament and a high electrical field during turn-off leads to avalanche injection [2.4] and RBSB. In the case of an FGT, since Q_1 is turned off by emitter-open, the emitter current crowding phenomenon is eliminated [2.6] and RBSB is avoided. Therefore, the FGT can be operated up to BV_{CBO} rather than the collector-emitter breakdown voltage, BV_{CEO}. The ratio of BV_{CBO} to BV_{CEO} depends on the transistor current gain, among other things. Generally speaking, the ratio (BV_{CEO}: BV_{CBO}) ranges from 50% to 80%.

2.6.2 High Voltage and High Current Capabilities

When the conduction drop is to be kept at a reasonable level, the chip area of a power MOSFET increases rapidly with the voltage rating. For a rating higher than 200V, the chip area increases in proportion to the voltage rating to the 2.5 power. As a consequence, it is not economically feasible to fabricate power MOSFETs possessing high voltage and high current capabilities simultaneously. In the case of an FGT, Q_2 is a high voltage but low current MOSFET, while Q_3 is a high current but low voltage MOSFET. The chip areas of Q_2 and Q_3 are much reduced, since they are not rated for both high voltage and high current. Table 2.2 shows a relative comparison of chip areas for power MOSFETs of different voltage and current ratings.

2.6.3 Simple Gate Drive Requirement

As mentioned earlier, the base drive current of Q_1 is derived from the load circuit rather than the gate drive power supply. Compared with a bipolar power transistor of the same rating, an FGT essentially requires no steady state drive current. The only appreciable drive current required is the small surge current pulses for charging and

TABLE 2.2

Chip Area Comparisons for Power MOSFETs of Various Ratings

Device Rating	Chip Area
50V/5A MOSFET	1 Unit
50V/50A MOSFET	10 Units
500V/5A MOSFET	9.9 Units
500V/50A MOSFET	99 Units

discharging gate capacitances of Q_2 and Q_3 during switching. If compared with a similarly rated power MOSFET, the chip areas of both Q_2 and Q_3 are much smaller, as are the gate capacitances. Consequently, the surge current requirement of the gate drive for the FGT is much reduced as compared to that of a bipolar power transistor or even a comparably rated power MOSFET.

2.6.4 Fast Switching Speed

The switching speed of an FGT is primarily limited by that of the main bipolar power transistor, Q_1. Now that Q_1 is inherently provided with a nearly ideal base drive current, the FGT can switch much faster than a comparable bipolar power transistor. As will be seen later in Table 2.6, the storage time is improved by at least a factor of 3, and fall time by a factor of 2, as compared with those obtained from a conventional turn-off scheme.

2.6.5 Enhanced dv/dt Capability

Because both Q_2 and Q_3 could have small chip sizes, the gate capacitances are much reduced, as well as the dv/dt effect. Moreover, Q_3 is OFF in the OFF state, so that any

false triggering current can not flow through the base-emitter junction of Q_1. These effects help enhance the dv/dt capability of an FGT.

2.6.6 Small Chip Areas

A comparative estimate of chip areas is given below for a power Darlington, a power MOSFET and an FGT. Assuming the chip area of the conventional power Darlington output transistor is 1 unit, and that of the driver transistor is 0.2 units for an optimum design, the total area of the power Darlington transistor is 1.2 units. For a comparable MOSFET, the chip area is approximately 2.5 units.

The estimate process of the total chip area of the FGT is more involved. As mentioned earlier, for a power transistor or a power MOSFET with voltage ratings greater than 200V, the chip area increases at a rate proportional to the 2.5 power of the device voltage rating [2.1] to achieve the same conduction voltage drop. Since Q_1 is free from RBSB and can be operated up to BV_{CBO} instead of BV_{CEO}, the voltage rating of the same chip is greatly enhanced. In other words, for the same voltage rating, the chip area of Q_1 can be significantly reduced with respect to a comparable

bipolar power transistor using conventional reverse bias turn-off. Q_1 requires only $(1*0.5)^{2.5} = 0.2$ units because Q_1 can be operated up to BV_{CBO}, which is about twice the BV_{CEO} of the output transistor of a conventional power Darlington transistor. The chip area of Q_2 is 2.5 times that of the Darlington driver transistor and requires 0.5 units. Q_3 is a low voltage MOSFET rated at 50V and is estimated to be 0.2 units. To reduce the conduction voltage drop of the FGT, the chip areas of Q_1 and Q_2 are both increased by a factor of 2. This leads to Table 2.3, which shows, for a power Darlington transistor, a power MOSFET and an FGT, the chip areas of 1.2 units, 2.5 units and 1.3 units, respectively. For higher voltage devices, the comparison favors the FGT even more. Table 2.4 lists estimated chip areas for 800V devices. The estimate process resulting in this table is the same as of Table 2.3. For the 800V case, an FGT occupies the smallest chip area (5.5 units), followed by a Darlington transistor (6.8 units) and a MOSFET (14.1 units).

2.6.7 Disadvantages

The main disadvantage of the FGT is its structural complexity. It may appear that the conduction drop is a

TABLE 2.3

Chip Area Estimate for 400V Darlington, MOSFET and FGT

Relative Chip Area	Darlington	MOSFET	FGT
Q_1	1.0	2.5	0.4
Q_2	0.2	0.0	0.5
Q_3	0.0	0.0	0.4
Total (Units):	1.2	2.5	1.3

TABLE 2.4

Chip Area Estimate for 800V Darlington, MOSFET and FGT

Relative Chip Area	Darlington	MOSFET	FGT
Q_1	5.7	14.1	2.3
Q_2	1.1	0.0	2.8
Q_3	0.0	0.0	0.4
Total (Units):	6.8	14.1	5.5

serious disadvantage of an FGT. However, compared to a MOSFET with a similar rating and same chip size, the conduction drop of the MOSFET is two times that of the FGT for 400V devices, and 2.5 times for 800V devices. The advantages of the FGT outweighs the disadvantages in high voltage applications. In comparison with a BJT, the reduction of switching losses outweighs any disadvantages particularly for high voltage and high frequency applications.

2.7 EXPERIMENTAL RESULTS USING DISCRETE COMPONENTS

Four sets of discrete components have been used to form FGTs. The low current set is rated at 2A, the two medium current sets are rated at 8A and the high current set is rated at 25A. Table 2.5 summarizes the discrete components used. Snubber circuits are not used unless otherwise indicated.

2.7.1 Drive Waveforms

The upper trace in Figure 2.4 shows the base current of Q_1. The lower one is the load current waveform. Spikes of the load current are caused primarily by the reverse recovery of the free-wheeling diode in the test circuit. As seen from Figure 2.4, a large base current kick occurs at the instant of turn-on to rapidly turn on Q_1. At the instant of turn-off, a large reverse base current, which equals the collector current, is provided to rapidly turn off Q_1. During the conduction period, the base current is proportional to the collector current. As mentioned in Section 2.3, such an ideal base drive current is obtained from the load circuit instead of the gate drive circuit.

TABLE 2.5

Discrete Components Used for FGT Testing

Low Current FGT

Component	Part
Q_1:	Toshiba T1115(1500V/3A)
Q_2:	International Rectifier IRF730(400V/3.5A/1 ohm)
Q_3:	International Rectifier IRF530(100V/10A/0.18 ohm)
Z:	TCG135A(5.1V/1W)

Fast Medium Current FGT

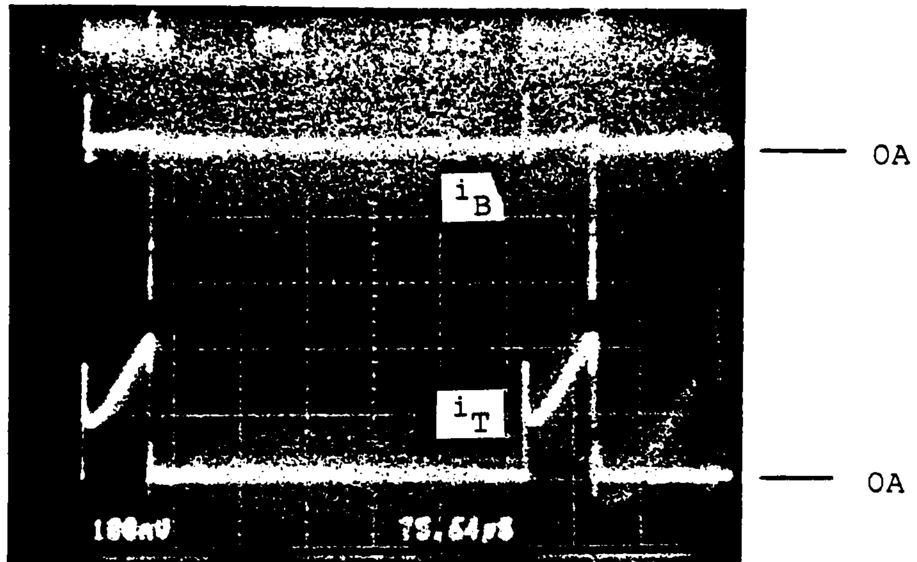
Component	Part
Q_1:	General Semiconductor 2N6655(400V/20A)
Q_2:	International Rectifier IRF730(400V/3.5A/1 ohm)
Q_3:	International Rectifier IRF530(100V/10A/0.18 ohm)
Z:	TCG135A(5.1V/1W)

Slow Medium Current FGT

Component	Part
Q_1:	Motorola MJ12004(1500V/4A)
Q_2:	International Rectifier IRF730(400V/3.5A/1 ohm)
Q_3:	International Rectifier IRF150(100V/28A/0.055 ohm)
Z:	TCG135A(5.1V/1W)

High Current FGT

Component	Part
Q_1:	Westinghouse D60T(450V/40A)
Q_2:	International Rectifier IRF730(400V/3.5A/1 ohm)
Q_3:	International Rectifier IRF150(100V/28A/0.055 ohm)
Z:	Motorola HEPZ3516(15V/10W)



i_B: 2 Amperes/Division
i_T: 2 Amperes/Division
time: 10 Microseconds/Division

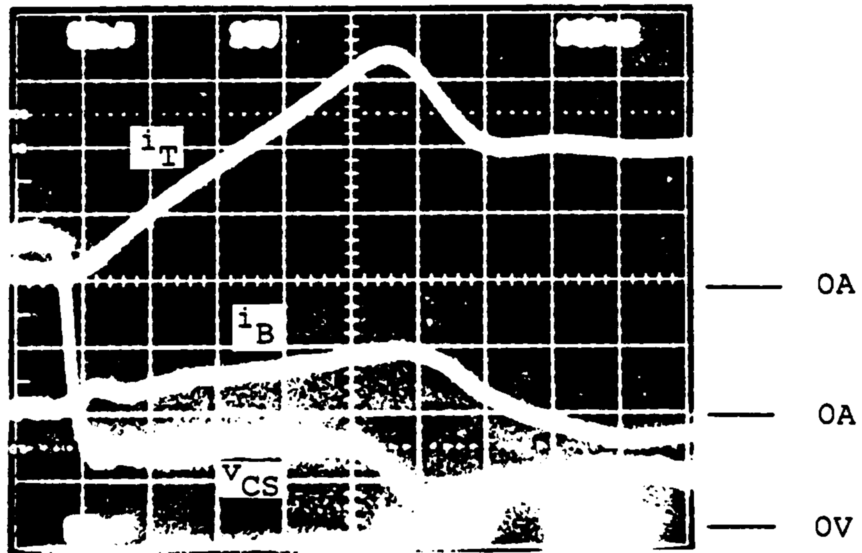
Q_1: General Semiconductor 2N6655
Q_2: International Rectifier IRF730
Q_3: International Rectifier IRF530
Z: TCG135A

Figure 2.4: Continuous Current Mode Waveforms of Q1 Base and FGT Collector Current (with Snubber)

2.7.2 Turn-on Waveforms

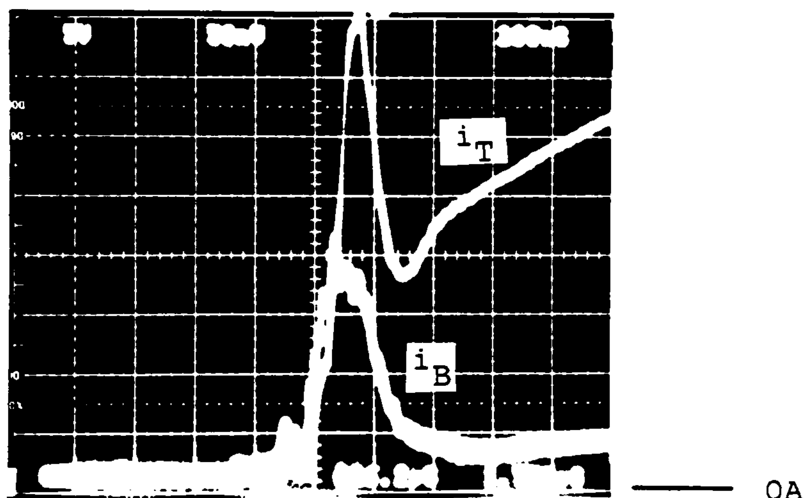
Figures 2.5 and 2.6 show the turn-on waveforms for the medium and high current FGTs in the continuous current mode of operation with an inductive load. As shown in Figure 2.5, the collector-emitter voltage of Q_1 drops very quickly, which minimizes the turn-on loss. As seen from Figure 2.6, before Q_1 is completely turned on, a good portion of the load current flows through Q_2 to provide the base current kick to Q_1, so that Q_1 can be turned on very rapidly. After Q_1 is completely turned on, most of the load current flows through Q_1, so Q_2 conducts only a small amount of the load current.

The ratio of the collector current of Q_1 to the base current of Q_1 at the instant of turn-on depends on the turn-on delay time of Q_1. This ratio is about 2:1, as seen from Figure 2.6. Although the surge current capability of Q_2 can be as high as ten times its continuous current rating [2.10], the turn-on delay time of Q_1 is normally short enough that Q_2 is not likely to conduct all the load current during turn-on. Furthermore, there is a negative feedback mechanism inherent in the FGT configuration to prevent such an occurence. The longer the turn-on delay time of Q_1, the



i_T:	1 Ampere/Division
i_B:	1 Ampere/Division
v_{CS}:	100 Volts/Division
time:	100 Nanoseconds/Division
Q_1:	General Semiconductor 2N6655
Q_2:	International Rectifier IRF730
Q_3:	International Rectifier IRF530
Z:	TCG135A

Figure 2.5: Turn-on Waveforms of a Fast Medium Current FGT (with Snubber)



i_T: 2 Amperes/Division
i_B: 2 Amperes/Division
time: 200 Nanoseconds/Division

Q_1: Westinghouse D60T
Q_2: International Rectifier IRF730
Q_3: International Rectifier IRF150
Z: Motorola HEPZ3516

Figure 2.6: Turn-on Waveforms for a High Current FGT (with Snubber)

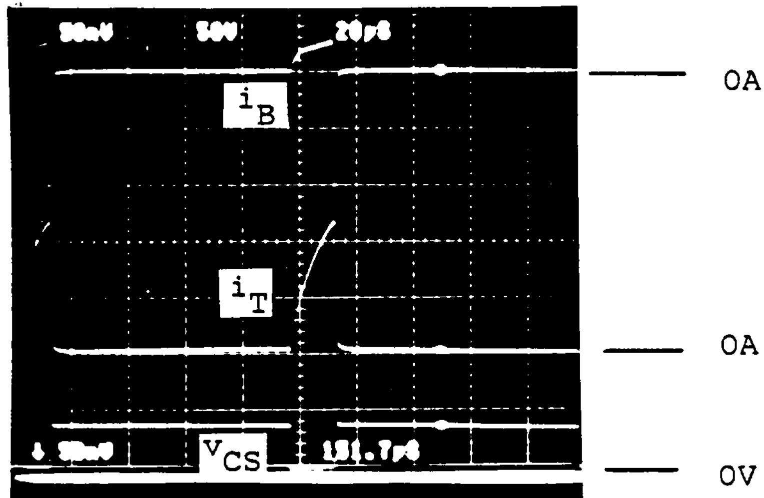
larger the base current spike. A larger base current spike, however, speeds up the turn-on of Q_1 and, therefore, reduces the current spike of Q_2. Because of this negative feedback mechanism, the variation of the current spike of Q_2 (due to the temperature change or the device variation) is minimized.

In the discontinuous current mode of operation, the inductive load current is zero at the instant of turn-on, so the base current kick is zero. Figure 2.7 shows the waveforms for a discontinuous current mode of operation using a low current FGT.

2.7.3 Turn-off Waveforms

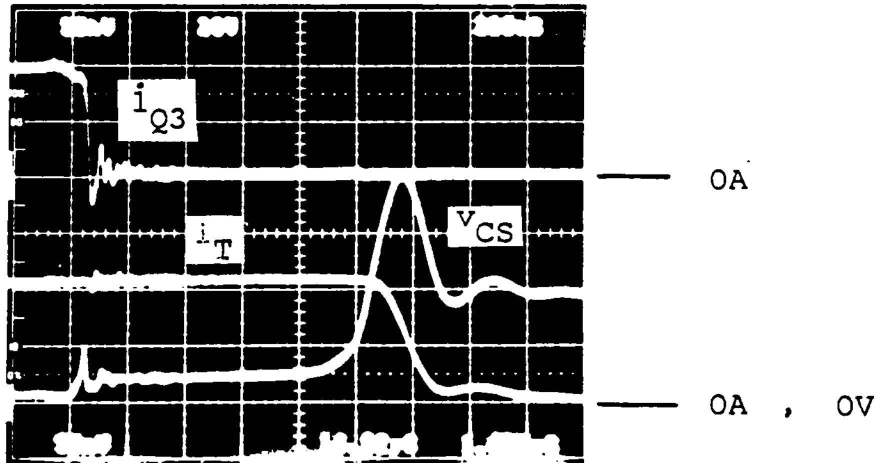
Since the turn-off characteristic of an FGT depends primarily on Q_1, several types of BJTs were used for Q_1 in the tests. Figures 2.8 and 2.9 show the turn-off waveforms of an FGT using a high-voltage, low-current, slow transistor as Q_1.

In Figure 2.8, the load current is decreased approximately 1.2 µs after the drain current of Q_3 ceases. The fall time of the load current is about 0.2 µs, which is



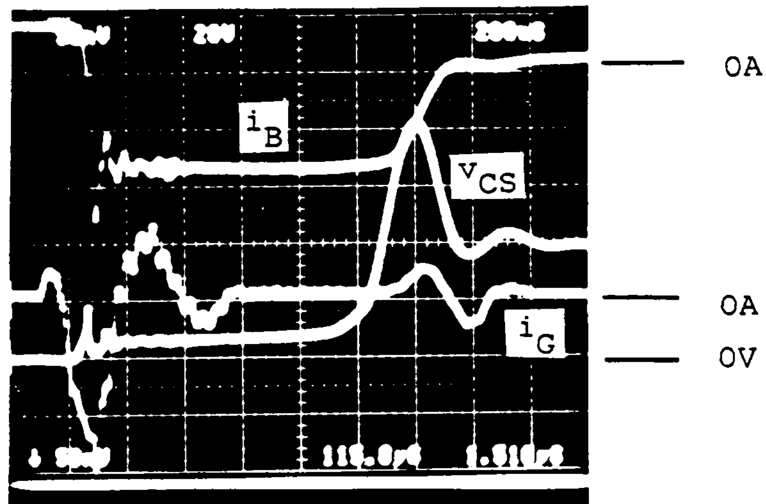
i_B:	1 Ampere/Division
i_T:	1 Ampere/Division
v_{CS}:	50 Volts/Division
time:	20 Microseconds/Division
Q_1:	Toshiba T1115
Q_2:	International Rectifier IRF730
Q_3:	International Rectifier IRF530
Z:	TCG135A

Figure 2.7: Discontinuous Current Mode Waveforms of Q1 Base Current and FGT Collector Current and Voltage (with Snubber)



i_{Q3}:	1 Ampere/Division
i_T:	1 Ampere/Division
v_{CS}:	20 Volts/Division
time:	200 Nanoseconds/Division
Q_1:	Toshiba T1115
Q_2:	International Rectifier IRF730
Q_3:	International Rectifier IRF530
Z:	TCG135A

Figure 2.8: Turn-off Waveforms of a Low Current FGT



i_B: 1 Ampere/Division
v_{CS}: 20 Volts/Division
i_G: 0.2 Amperes/Division
time: 200 Nanoseconds/Division

Q_1: Toshiba T1115
Q_2: International Rectifier IRF730
Q_3: International Rectifier IRF530
Z: TCG135A

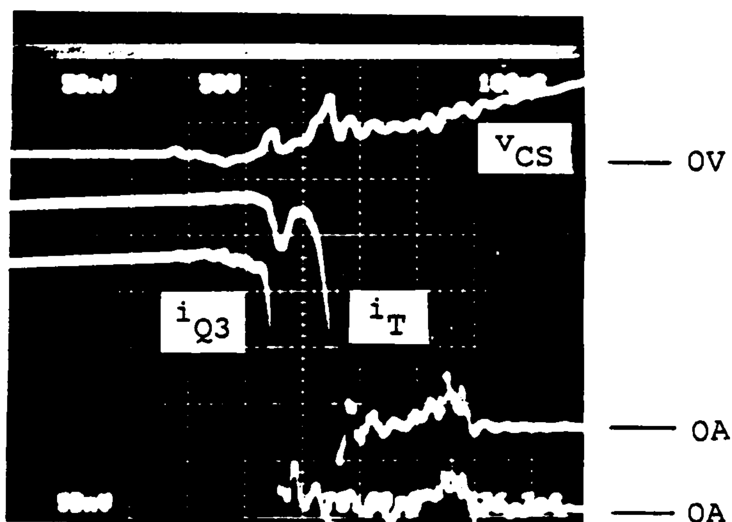
Figure 2.9: Turn-off Waveforms for a Low Current FGT

very fast for this slow transistor, Q_1. During the storage time, which is the period between fall-off of the emitter current and the load current, the collector-emitter voltage of Q_1 is clamped at the breakdown voltage of Z, i.e., at about 5V. The Q_1 collector-emitter voltage starts to increase a relatively long time after the emitter current is has ceased. Consequently, the reverse bias second breakdown is eliminated. Figure 2.9 shows the base and gate current waveforms for the same devices used in Figure 2.8. The reverse gate current is about 0.6A, which is easily obtained from a simple gate drive circuit.

Figures 2.10 and 2.11 show the FGT turn-off waveforms using a medium-current fast Q_1. As seen from Figure 2.10, the storage time is about 100 ns and the fall time is about 60 ns. The reverse base current and the load current are shown in Figure 2.11.

Figure 2.12 shows turn-off waveforms using a medium-current slow Q_1. The storage time is about 800 ns and fall time is about 200 ns.

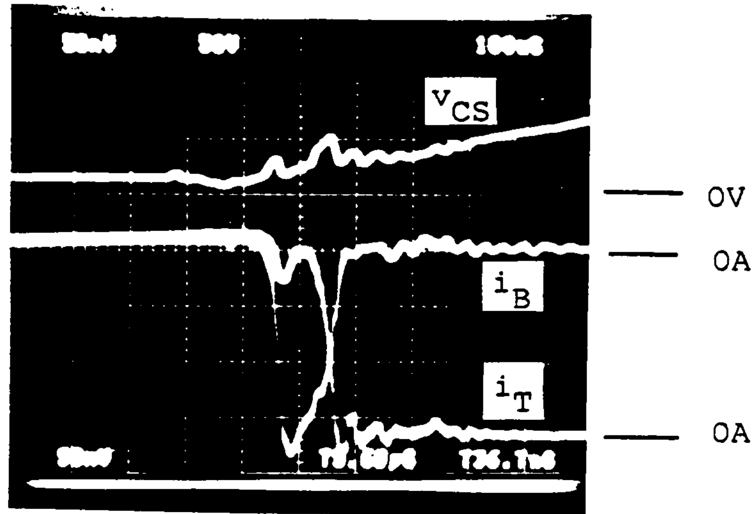
Figure 2.13 shows the FGT turn-off waveforms using a high-current Q_1 switched at 25A with a snubber circuit. The storage time is 0.5 µs and the fall time is 0.2 µs.



v_{CS}: 50 Volts/Division
i_T: 1 Ampere/Division
i_{Q3}: 1 Ampere/Division
time: 100 Nanoseconds/Division

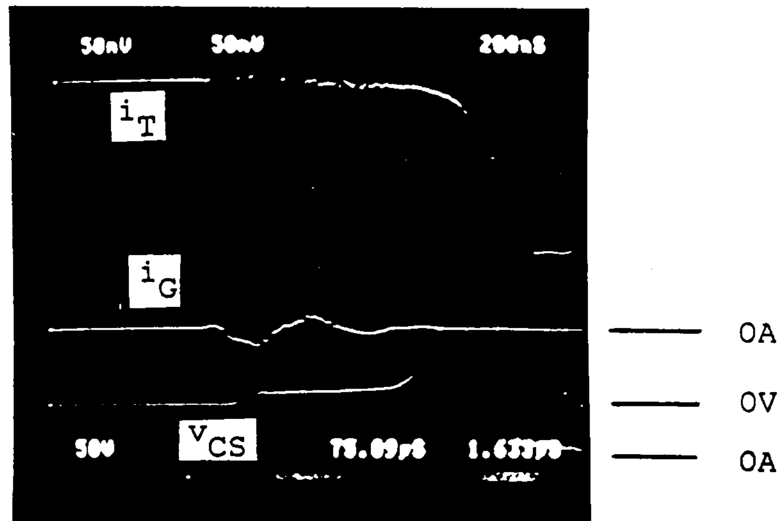
Q_1: General Semiconductor 2N6655
Q_2: International Rectifier IRF730
Q_3: International Rectifier IRF530
Z: TCG135A

Figure 2.10: Turn-off Waveforms of a Fast Medium Current FGT



v_{CS}:	50 Volts/Division
i_B:	1 Ampere/Division
i_T:	1 Ampere/Division
time:	100 Nanoseconds/Division
Q_1:	General Semiconductor 2N6655
Q_2:	International Rectifier IRF730
Q_3:	International Rectifier IRF530
Z:	TCG135A

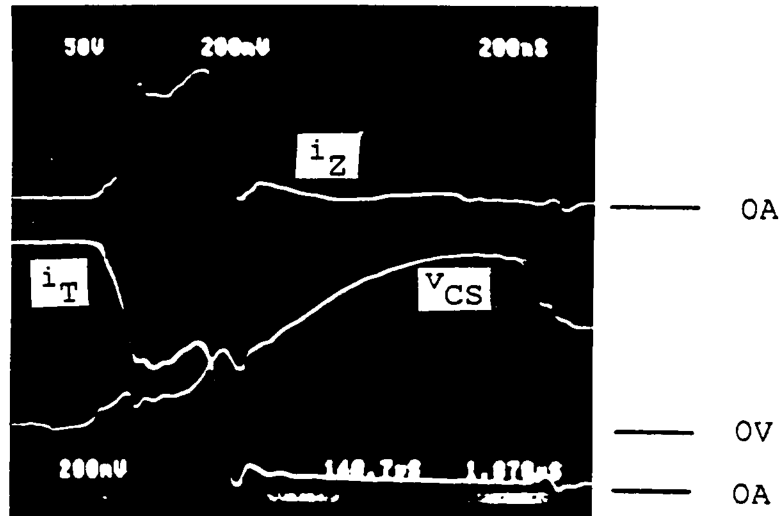
Figure 2.11: Turn-off Waveforms of a Fast Medium Current FGT (with Snubber)



v_{CS}: 50 Volts/Division
i_G: 1 Ampere/Division
i_T: 1 Ampere/Division
time: 200 Nanoseconds/Division

Q_1: Motorola MJ12004
Q_2: International Rectifier IRF730
Q_3: International Rectifier IRF150
Z: TCG135A

Figure 2.12: Turn-off Waveforms of a Slow Medium Current FGT



i_Z:	6 Amperes/Division
v_{CS}:	50 Volts/Division
i_T:	6 Amperes/Division
time:	200 Nanoseconds/Division
Q_1:	Westinghouse D60T
Q_2:	International Rectifier IRF730
Q_3:	International Rectifier IRF150
Z:	Motorola HEPZ3516

Figure 2.13: Turn-off Waveforms of a High Current FGT (With Snubber)

At first glance, the load current waveform in Figure 2.13 seems to exhibit a two-step turn-off. However, the first drop of the load current waveform corresponds to the first step rise of the collector-source voltage of the FGT. The snubber circuit shunts the current, resulting in a step change of the FGT current waveform. The second drop of the FGT current waveform is due to a part of the real fall time of the FGT. It is observed in Figure 2.13 that the zener diode conducts during the storage time. The first step rise of the collector-source voltage of the FGT is the zener clamping voltage.

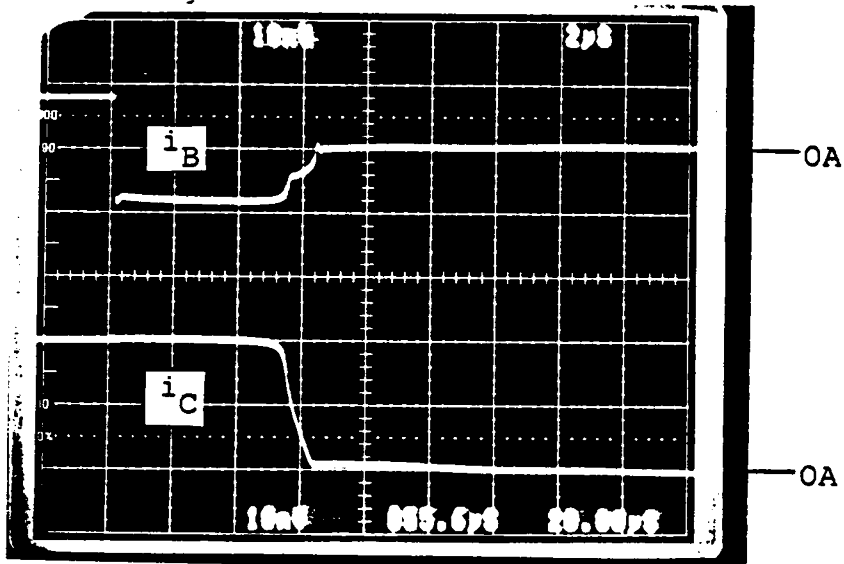
2.7.4 Storage Time and Fall time

Figure 2.14 shows waveforms of the base and the collector currents of a single BJT (T1115) using conventional turn-off. The very same device was also used to form an FGT of which the switching waveforms were previously shown in Figure 2.8. The forward current gains of the BJT and Q_1 of the FGT are equal to 5. However, the reverse current gain is 5 for the BJT and 1 for Q_1 of the FGT. The storage time for the BJT turned off conventionally is 5.4 μs and the fall time is 1.0 μs. Using the FGT configuration, the storage and fall times are 1.2 μs and 0.2

μs, respectively. Table 2.6 summarizes the improvement of the storage time and fall time in an FGT as compared to those of BJTs using conventional turn-off. As can be seen from Table 2.6, the improvement is quite significant.

The storage time of the FGT depends on the characteristics of Q_1 and Q_2. Because of the Darlington configuration, Q_1 is never operating in deep-saturation. The degree of saturation of Q_1 depends on the forward voltage drop of Q_2. The choice of Q_2 with a small chip area decreases the degree of saturation of Q_1 and the storage time, at the expense of the conduction voltage drop.

The fall time of a bipolar transistor can also be significantly reduced by the emitter-open turn-off scheme. A collector current tailing phenomenon may occur in a bipolar power transistor during turn-off. The current tailing phenomenon refers to the slow current fall time during the final phase of turn-off, and is a major source of power loss in high frequency applications. This phenomenon may result from two causes. One is the inability of the base drive circuit to pull out the base current in the final stage of turn-off. This may be due to the base drive circuit design or a large device impedance during that



i_B: 0.5 Amperes/Division
i_C: 1 Ampere/Division
time: 2 Microseconds/Division

Device: Toshiba T1115

Figure 2.14: Reverse Bias Turn-off Waveforms of a BJT

TABLE 2.6

Summary of Improvement Using FGT Configuration

Device	Storage Time	Fall Time
T1115 (forward gain=5)	5.4	1.0
When Used in FGT	1.2	0.2
2N6655 (forward gain=10)	0.5	0.2
When Used in FGT	0.1	0.06
MJ12004 (forward gain=5)	3.2	0.6
When Used in FGT	0.8	0.2
D60T (forward gain=10)	2.7	0.3
When Used in FGT	0.6	0.1

.Tested at same forward current gain for each BJT and the associated FGT
.Reverse current gain = 5 for testing single BJTs
.Time in microsecond

period. The second cause may be the recombination of excessive carriers trapped in the N^- region of the bipolar transistor. In the case of an FGT, Q_1 acts as a diode in recovery because of emitter-open turn-off [2.12]. The excess carrier profile at t=0 (preceding turn-off) could be similar to that in either Figure 2.15 or Figure 2.16, depending on the degree of device saturation before the turn-off signal is applied.

In Figure 2.15, when the device is in deep-saturation before turn-off, the excess carriers are still trapped in the N^- region and subsequently allowing the current tailing phenomenon to occur. However, Q_1 never operates in deep-saturation because of its Darlington configuration with Q_2 in the FGT structure. The carrier profile of the FGT is thus similar to that in Figure 2.16 for the quasi-saturation case and current tailing will not occur because the excess carriers trapped in the N^- region are significantly reduced.

2.7.5 Reverse Bias Second Breakdown Test

A non-destructive Reverse Bias Second Breakdown Tester [2.13] was used to demonstrate the RBSB ruggedness of the FGT. Because of the non-destructive nature of the RBSB

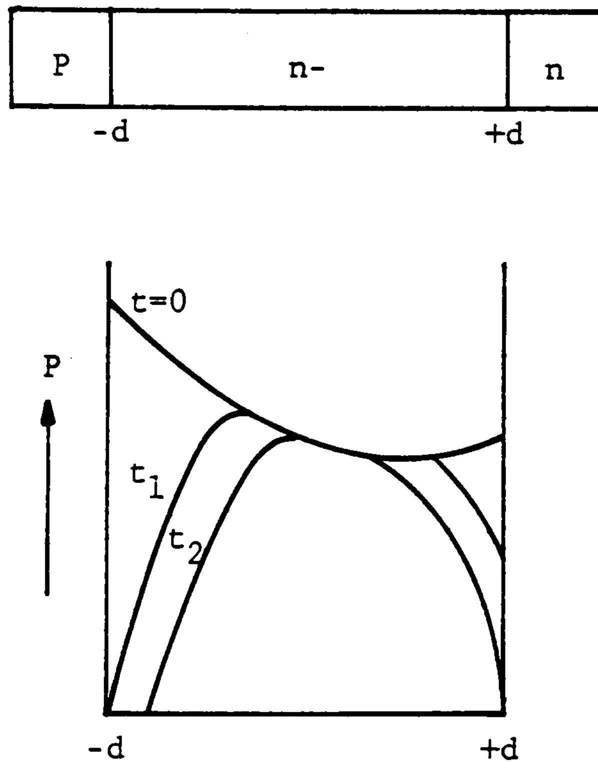


Figure 2.15: Carrier Profiles for Deep-Saturation

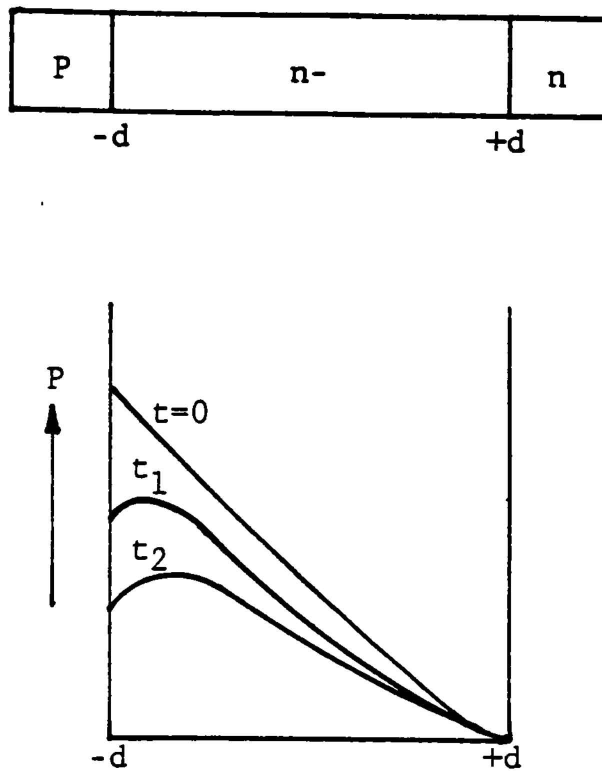


Figure 2.16: Carrier Profiles for Quasi-Saturation

test, the same device can be tested under several drive conditions and meaningful comparisons can be made.

A bipolar power transistor, RCA 2N6249 (measured BV_{CEO}=360V, BV_{CBO}=700V), was chosen as the device under test which was turned off during conventional drive conditions. Table 2.7 summarizes the test results. The same device was used to form an FGT of which the test results are also included in Table 2.7.

As can be seen from Table 2.7, when the collector current of Q_1 is less than 9A, there is no RBSB observed in the FGT in testing up to 700V (=BV_{CBO} of Q_1). Figure 2.17 shows the v_{CS} waveform of the FGT at turn-off. The same BJT, tested under a conventional bias condition (forward base current = 2A, reverse base current = 4A), exhibits RBSB at 350V, as shown in Figure 2.18.

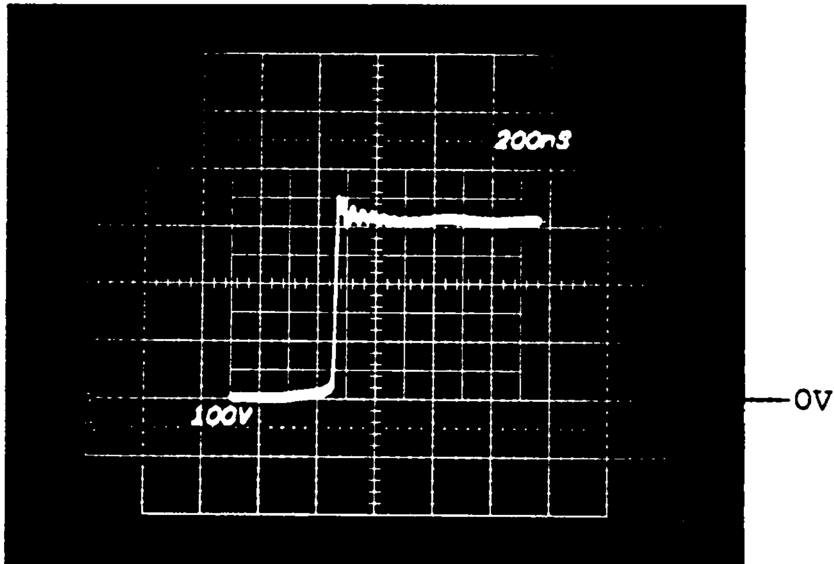
When the current exceeded 9A, however, RBSB was observed in the FGT, even though the breakdown voltage was significantly higher than that of the conventionally turned off BJT. Figure 2.19 shows the voltage waveform of the FGT tested at 10A.

TABLE 2.7

Test Results of Reverse Bias Second Breakdown

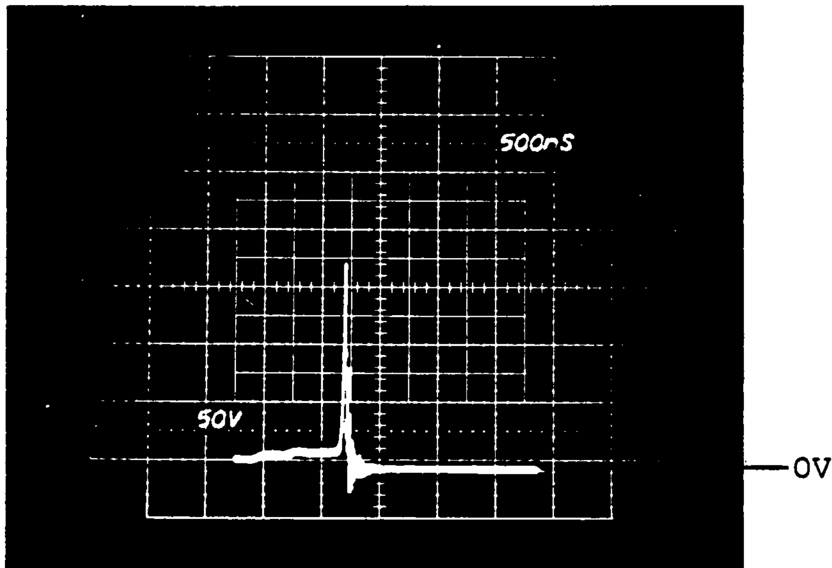
	BJT(2N6249) I_{BR}=2A	BJT(2N6249) I_{BR}=4A	FGT
I_C=5A	RBSB@380V		v_{CS} rises up to 700V
I_C=6A	RBSB@380V		v_{CS} rises up to 700V
I_C=7A	RBSB@380V		v_{CS} rises up to 700V
I_C=8A	RBSB@370V	RBSB@350V	v_{CS} rises up to 700V
I_C=9A	RBSB@350V	RBSB@340V	RBSB@480V
I_C=10A	RBSB@350V	RBSB@320V	RBSB@450V

.Test Condition for BJT: Forward Base Current = 2A
.Test Condition for FGT: Gate Drive Voltage = +/- 15V



v_{CS}:	100 Volts/Small Division
time:	200 Nanoseconds/Small Division
Q_1:	RCA 2N6249
Q_2:	International Rectifier IRF730
Q_3:	International Rectifier IRF530
Z:	TCG135A

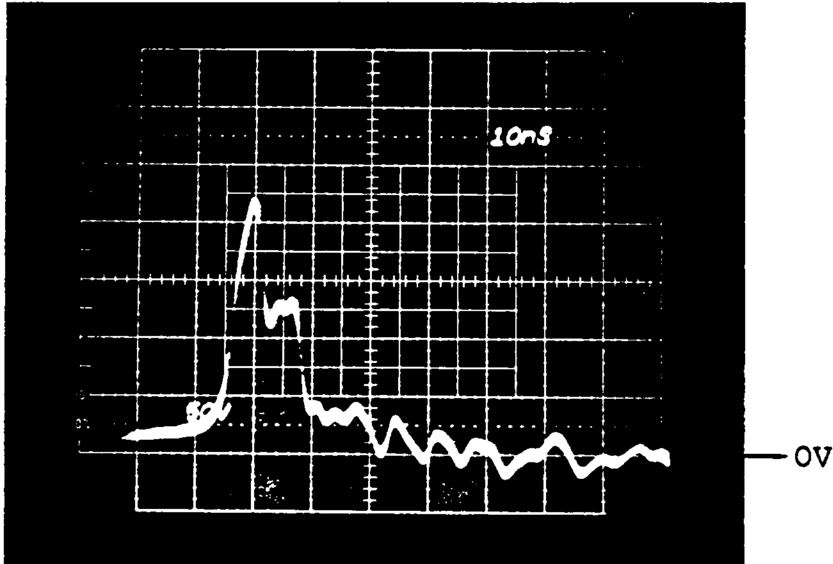
Figure 2.17: RBSB Test for an FGT at 8 Amperes



V_{CE}: 50 Volts/Small Division
time: 500 Nanoseconds/Small Division

Device: RCA 2N6249

Figure 2.18: RBSB Test for a BJT at 8 Amperes

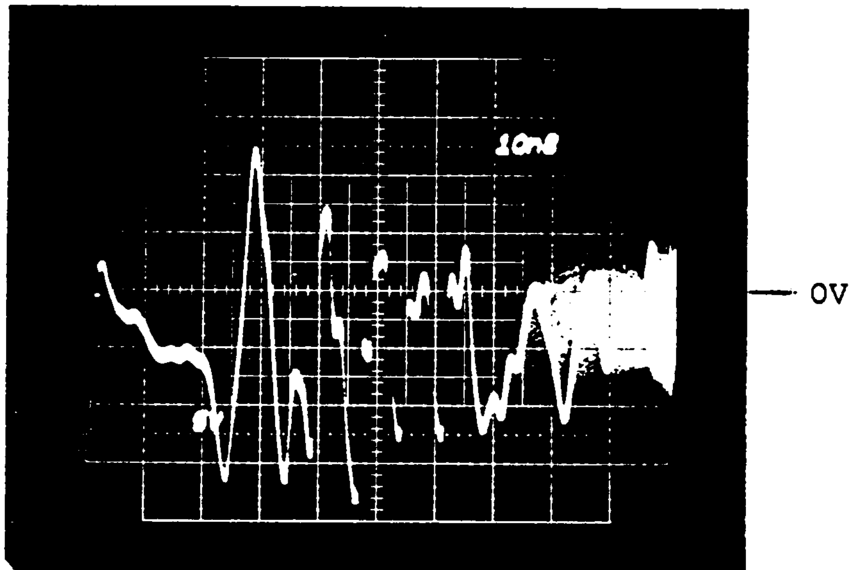


V_{CS}:	50 Volts/Small Division
time:	10 Nanoseconds/Small Division
Q_1:	RCA 2N6249
Q_2:	International Rectifier IRF730
Q_3:	International Rectifier IRF530
Z:	TCG135A

Figure 2.19: RBSB Test for an FGT at 10 Amperes

This observation seems to contradict the belief that RBSB does not occur in an FGT. However, the observed breakdown has an explanation which has been verified during the testing. Q_1 of the FGT used during the testing is not exactly emitter-opened during turn-off when the current level is high. Also during turn-off, Q_3 turns on again when it is supposed to be completely OFF. This is due to the gate voltage of Q_3 oscillating after the turn-off signal, so Q_3 is turned back on momentarily. In other words, Q_1 is not truly emitter-opened. Figures 2.20 and 2.21 show the evidence for this reasoning. When the collector voltage starts to increase, Q_3 must be held OFF completely during the final phase of turn-off in order to avoid the RBSB occurrence.

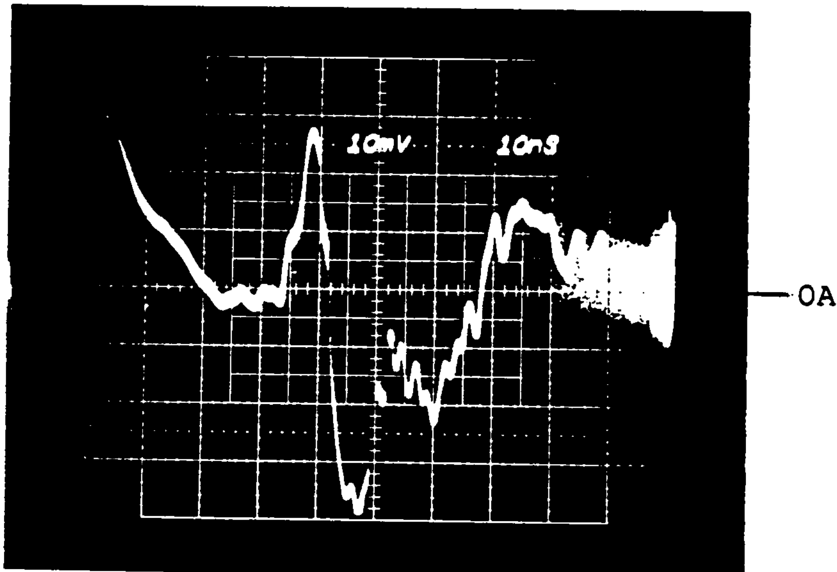
Because the non-destructive RBSB tester was originally designed for testing bipolar power transistors, a base drive current source was used. Since a voltage drive is needed for an FGT, a clamping voltage was set for the base drive of the non-destructive RBSB tester. Due to the long wiring in the base drive assembly, parasitic inductances contributed to the oscillations of the FGT gate voltage, momentarily turning on Q_3 and causing RBSB to occur.



v_{GS}: 5 Volts/Small Division
time: 10 Nanosecond/Small Division

Q_1: RCA 2N6249
Q_2: International Rectifier IRF730
Q_3: International Rectifier IRF530
Z: TCG135A

Figure 2.20: Q3 Gate Voltage Waveform During Turn-off at 10 Amperes



i_{Q3}:	1 Ampere/Small Division
time:	10 Nanoseconds/Small Division
Q_1:	RCA 2N6249
Q_2:	International Rectifier IRF730
Q_3:	International Rectifier IRF530
Z:	TCG135A

Figure 2.21: Q3 Drain Current Waveform During Turn-off at 10 Amperes

2.8 REPLACING THE ZENER DIODE WITH A P-CHANNEL MOSFET

The zener diode, Z, used in the basic FGT configuration conducts during the storage time of Q_1. A P-channel MOSFET can be used to replace the zener diode. The FGT configuration with a P-channel MOSFET (Q_4) is shown in Figure 2.22. With a high gate voltage, Q_2 and Q_3 are turned on while Q_4 is OFF, and the FGT operates in the same way as described in Section 2.3. When the gate voltage is low, both Q_2 and Q_3 are cut off, but Q_4 is turned on. The collector current of Q_1 flows out of the Q_1 base terminal through Q_4 to the ground. Therefore, Q_4 plays the same role as the zener diode did. The Q_4 current waveform is shown in Figure 2.23. It will be shown in Chapter V that an FGT with a P-channel MOSFET can be integrated into a monolithic chip.

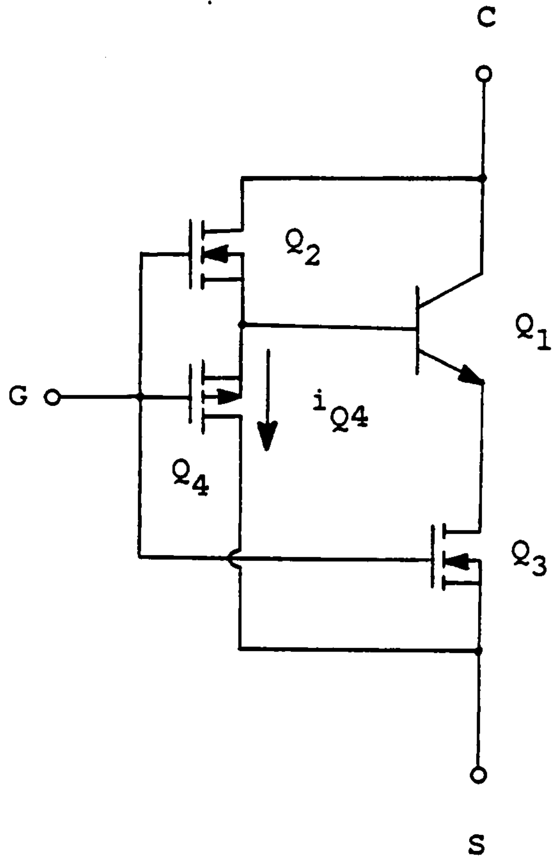
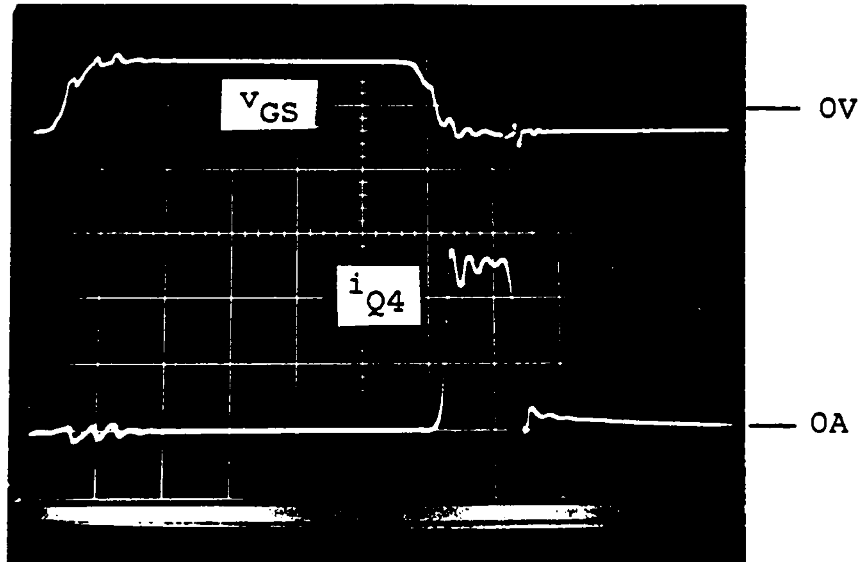


Figure 2.22: FGT Configuration with Z Replaced by Q4



v_{GS}:	20 Volts/Division
i_{Q4}:	5 Amperes/Division
time:	500 Nanoseconds/Division
Q_1:	Westinghouse D60T
Q_2:	International Rectifier IRF730
Q_3:	Siemens BUZ15
Q_4:	International Rectifier IRF9531

Figure 2.23: Q4 Current Waveform

Chapter III

THE INSULATED GATE TURN-OFF THYRISTOR

In this chapter, another MOS-Bipolar composite power device is proposed and investigated. It is named the Insulated Gate Turn-off Thyristor (IGTO) and consists of a Gate Turn-off Thyristor (GTO), an Insulated Gate Transistor (IGT) and a power MOSFET. The device configuration is similar to that of the FET-Gated Bipolar Transistor (FGT) presented in Chapter II. Due to the unique characteristics of the GTO and the IGT used in this new composite configuration, the voltage capability is much enhanced. The intended application area is for voltages above 1000V.

Because a GTO and an IGT are used in the new composite configuration, a brief review of the two relatively new devices is presented first in this chapter. The device configuration and the operating principle of the IGTO is discussed next. Experimental results obtained by using discrete components to form this composite device are also given.

3.1 BRIEF REVIEW OF THE GATE TURN-OFF THYRISTOR

3.1.1 GTO Device Structure

The basic device structure and a two-transistor equivalent circuit of a Gate Turn-off Thyristor (GTO) are shown in Figure 3.1. The output I-V characteristics of the GTO are shown in Figure 3.2.

As seen from Figure 3.1, a GTO is a four-layer P^+-N^--P-N^+ device where P^+, N^- and P regions correspond to the emitter, base and collector of the equivalent PNP transistor. The N^+, P and N^- regions correspond to the emitter, base and collector of the equivalent NPN transistor.

3.1.2 GTO Operating Principle

3.1.2.1 Turn-on

When a positive current pulse is applied to the gate of a GTO, the NPN transistor inside the GTO structure is turned on. This in turn provides the base current to turn on the internal PNP transistor and the GTO latches. The turn-on process is similar to that of a conventional thyristor (or Silicon Control Rectifier, SCR).

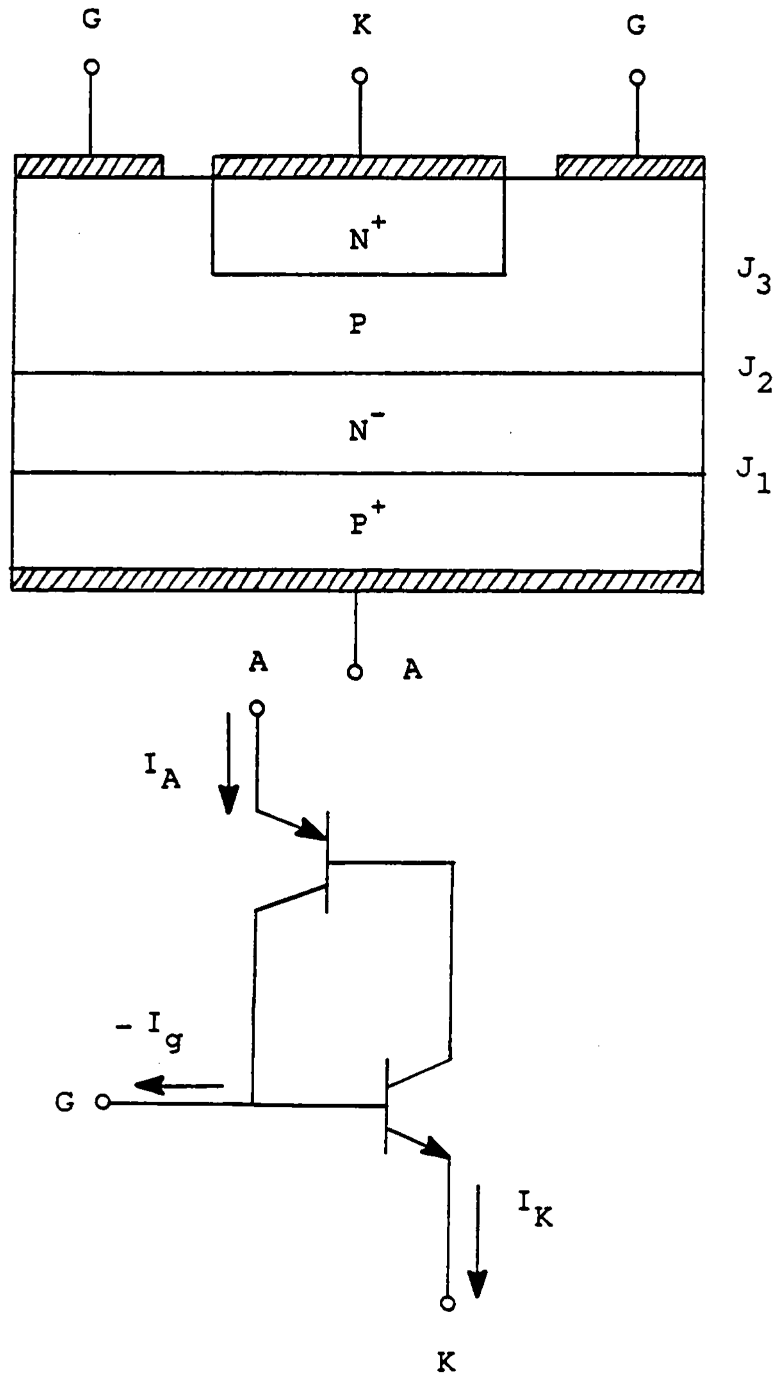


Figure 3.1: GTO Device Structure and Equivalent Circuit

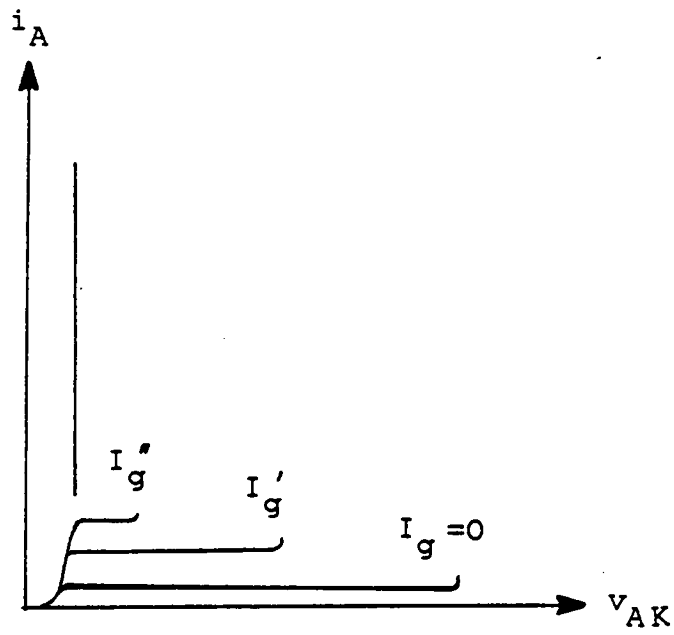


Figure 3.2: GTO I-V Characteristics

3.1.2.2 Conduction

Once the GTO is turned on it latches and, theoretically, no external gate current is needed to keep the GTO in conduction. During the conduction period, the ungated N^- region is "conductivity-modulated" by excess carriers, so that the GTO conducts at a low forward voltage drop.

3.1.2.3 Turn-off

A reverse gate current pulse is required to turn off a GTO. The turn-off gain (or reverse current gain), which is the ratio of the anode current to the reverse gate current, is closely related to the turn-off time, and more importantly, to the gate turn-off capability of the GTO. A brief description of the GTO turn-off process is given below.

<u>Storage Time</u>

When a GTO is turned off by a reverse bias voltage, the base-emitter junction of the NPN transistor will be reverse biased by the negative potential. A negative gate current flows out of the gate of the GTO, so that stored charges in

the P region are removed. Because of the lateral voltage drop caused by the lateral gate current flow in the P-base, junction J_3 becomes less positively biased near the gate contact than below the center of the cathode stripe. Eventually the part of J_3 closest to the gate contact will become reverse biased. Therefore, all the conducting current will be "squeezed" toward the center of J_3 which is still forward biased. This is a progressive process until the remaining charges in the P region are removed. This "squeezing" process is similar to the emitter current crowding phenomenon observed in a bipolar power transistor. Therefore, a GTO is subjected to RBSB as observed in a bipolar power transistor.

Maximum Turn-off Gain

The maximum turn-off gain is derived [3.1] as

$$\beta_{off,max}=1+4L_n^2/W_p^2$$

where L_n is the effective diffusion length and W_p the width of the P region. The maximum turn-off gain, ranging between 5 and 10, corresponds to the minimum reverse gate current required to take the GTO out of saturation during turn-off. There is a trade-off between the storage time and the turn-off gain. The lower the turn-off gain is (i.e., the larger

the reverse gate current), the shorter the storage time will be . The large reverse gate current requirement is a significant disadvantage of the GTO. For example, turning off a 200A anode current using a turn-off gain of 5 requires a 40A reverse gate current. This makes the GTO gate drive circuit bulky, noisy and expensive.

Fall Time and Tailing Time

At the end of the storage phase, the entire J_2 junction comes out of saturation. Afterwards, the forward current is reduced to zero and junction J_2 becomes reverse biased. The negative gate current helps remove the carriers in the P region. However, the remaining carriers in the ungated N^- region must either drift or diffuse to J_2 and be collected or recombine in the N^- region [3.2].

Two time constants are observed for the GTO anode current during turn-off, as shown in Figure 3.3. The first one corresponds to the fall time, t_f, during which the anode current quickly drops to a finite value. The second time constant corresponds to the tailing time, t_t, during which the remaining carriers in the N^- region recombine and the anode current gradually decays to zero.

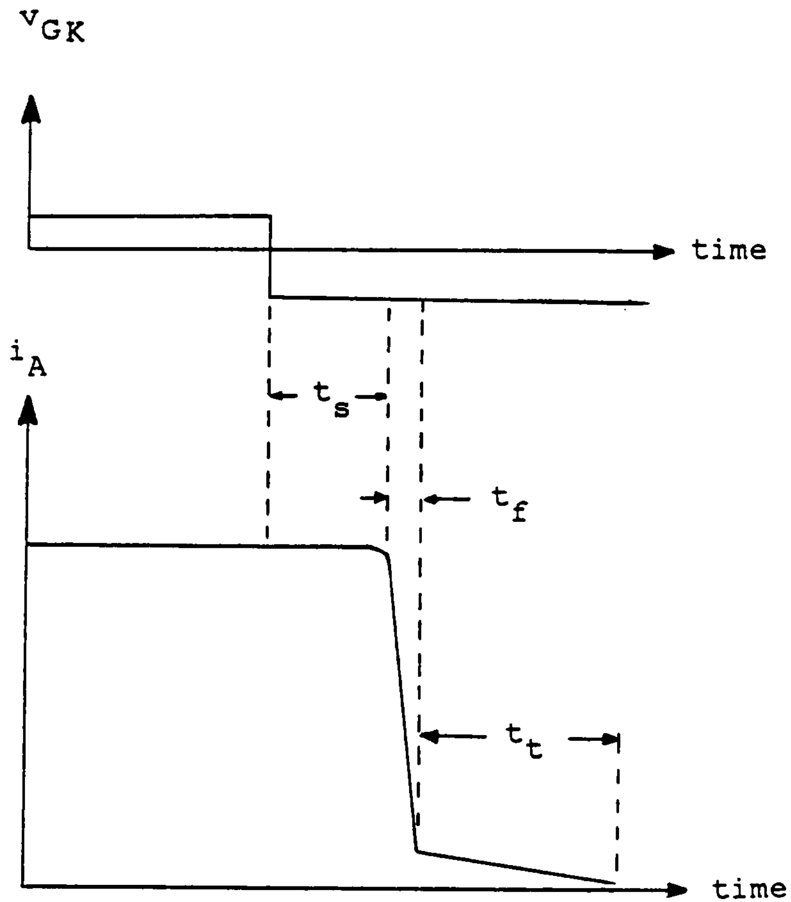


Figure 3.3: GTO Anode Current Waveform During Turn-off

To help reduce the tailing time, gold doping or an electron irradiation technique [3.3] is used to shorten the carriers' life time in the N^- region at the expense of a higher conduction voltage drop.

3.1.2.4 Unique GTO Characteristics

Although a GTO features a gate turn-off capability, the turn-off gain usually ranges between 3 and 5 and requires a complicated gate drive circuit. During turn-off, RBSB may occur because of the "squeezing" mechanism that causes the local cathode current density to sharply increase [3.4]. If the dv/dt limit is exceeded, a junction displacement current may falsely trigger the GTO which could destroy the device. These disadvantages could be eliminated by the IGTO configuration as discussed in Subsection 3.4.4.

3.2 BRIEF REVIEW OF THE INSULATED GATE TRANSISTOR

The Insulated Gate Transistor (IGT) is a voltage controlled device with gate turn-off capability. The main difference between an IGT and a conventional MOSFET is that the conduction voltage drop of an IGT is kept at a low level by the conductivity-modulation mechanism. This makes it feasible to have a high voltage IGT (>1000V) with a small chip area.

3.2.1 IGT Device Structure

The device structure of an IGT is similar to that of an n-channel power MOSFET [3.5], except that an N^- epitaxial layer is grown on a P^+ substrate instead of an N^+ substrate. The device structure and the equivalent circuit of an IGT are shown in Figure 3.4.

As shown in Figure 3.4, an IGT is a four-layer P^+-N^--P-N^+ device with a MOS-gated channel. The equivalent circuit indicates a parasitic thyristor in the IGT structure. Suppression of this parasitic thyristor action is a very important consideration in the IGT design. Otherwise, the parasitic thyristor may latch and the IGT loses its gate turn-off capability.

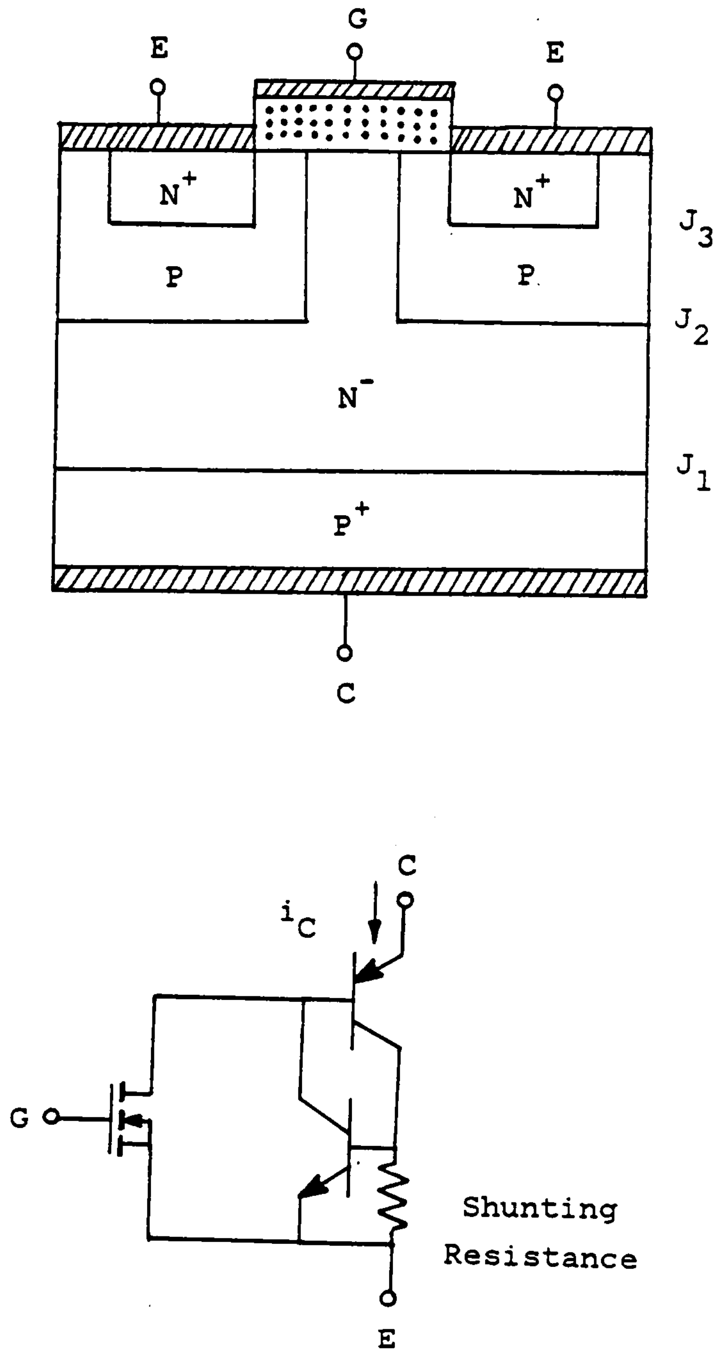


Figure 3.4: IGT Device Structure and Equivalent Circuit

In order to suppress this parasitic thyristor action, a shunting resistance, R_S, is used to lower the current gain of the NPN transistor, α_{npn}, so that $\alpha_{npn}+\alpha_{pnp}<1$ and latching of the parasitic thyristor is avoided. In other words, if the P-N^+ junction of the NPN transistor is forward biased by more than 0.7V due to any lateral current flowing in the P region, the N^+ region will begin to inject electrons into the P base during device operation, causing α_{npn} to increase. In this case the electron concentration is high throughout the P base region under the emitter, as expected in the characteristics of a thyristor, and the current no longer has to flow to the emitter via the MOSFET channel. Therefore, the four-layer device latches. This can be circumvented by keeping the P base sheet resistance low and designing narrow N^+ emitter regions, resulting in the small shunting resistance, R_S, to suppress the thyristor action [3.6].

3.2.2 IGT Operating Principle

3.2.2.1 Turn-on Waveforms

If a positive collector-emitter voltage, v_{CE}, is applied with the gate-emitter voltage, v_{GE}, exceeding the threshold voltage (typically 5V), the surface of the P

region under the gate is "inverted" into N type, and electrons can flow into the N^- epitaxial region (base of the PNP transistor) from the emitter through the inversion layer. These electrons lower the potential of the N^- epitaxial region, causing the P^+ region to inject holes into the N^- epitaxial region, and the IGT is turned on [3.6].

3.2.2.2 Conduction

The excess electrons and holes in the N^- epitaxial region modulate the conductivity of the high-resistivity N^- epitaxial region and significantly reduces the ON-resistance of the device. The device operates at a high current density similar to a forward-biased p-i-n diode [3.5].

Since the ON-resistance of the conductivity modulated N^- region is determined by the concentrations and mobilities of the excess carriers, as in a p-i-n diode [3.7], rather than by the background doping of the epitaxial layer, a very low ON-resistance is still obtainable even from devices designed for high voltage applications. It is reported that the ON-resistance at 20A for a 400V device is less than 0.1 ohm, approximately 10 times less than that of a comparable power MOSFET [3.6].

The output I-V characteristics of an IGT are shown in Figure 3.5 [3.5]. It is noted that an IGT has an inherent reverse blocking capability which is an attractive feature for AC circuit applications. A 0.7V offset from the origin in Figure 3.5 is the voltage required to forward bias junction J_1 before the current can sharply increase [3.5].

3.2.2.3 Turn-off Waveforms

To turn off an IGT, it is necessary to switch the gate bias off, either by shorting the gate to the emitter or by applying a negative gate-emitter voltage. This will remove the inversion layer and terminate the supply of electrons to the N^- region.

At the instant of turn-off, the electron concentration in the epitaxial region at junction J_1 is still large and significant electron injection into the P^+ collector occurs while a corresponding hole current flows into the P base. As the electron concentration decreases, the electron injection into the P^+ collector also decreases, leaving a plasma of electrons and holes in the epitaxial region that decays by recombination [3.5]. As a result, the collector current waveform during turn-off exhibits two time

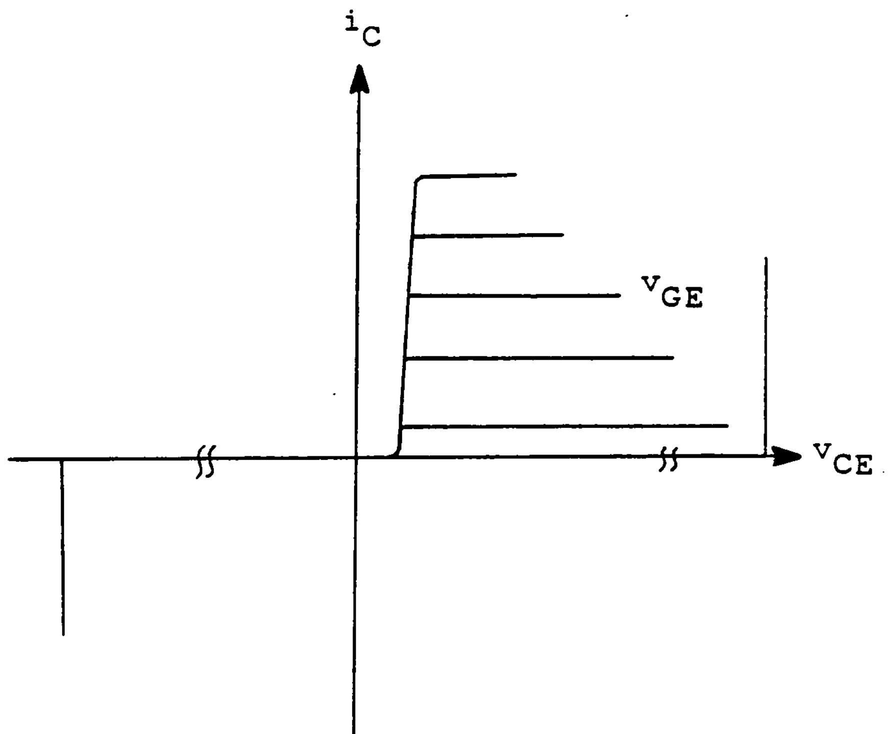


Figure 3.5: IGT I-V Characteristics

constants, as shown in Figure 3.6. The first time constant corresponds to the fall time, t_f, during which the collector current decreases rapidly due to the turn-off of the MOS portion. The second time constant corresponds to the tailing time, t_t, during which the excess carriers in the epitaxial region decay by recombination resulting in a current tailing phenomenon [3.8].

3.2.2.4 Forward Blocking

When a positive v_{CE} is applied to an IGT with $v_{GE} = 0$, the IGT blocks current flow because junction J_2 is reverse biased. The IGT is now in the forward blocking mode.

3.2.2.5 Reverse Blocking

When a negative voltage is applied to the collector with respect to the emitter, junction J_1 is reverse biased and current flow is blocked. This is the reverse blocking mode of operation of an IGT.

3.2.2.6 Unique IGT Characteristics

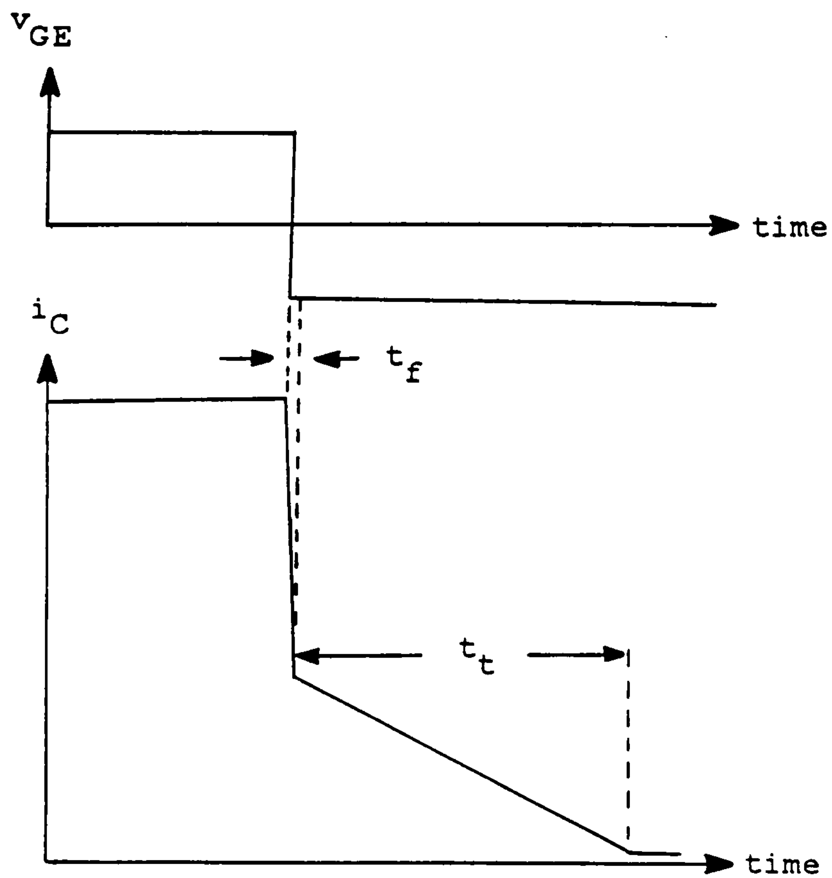


Figure 3.6: IGT Current Waveform During Turn-off

Although the IGT features advantages such as simple gate drive requirements, a high conduction current density at a low forward voltage drop, etc., it is plagued by two unique characteristics: turn-off current tailing and device latching. These disadvantages can be eliminated by the IGTO configuration as discussed in Subsection 3.4.4.

Turn-off Current Tailing

As just mentioned, the current tailing is caused by the recombination of excess carriers in the N^- region during turn-off. It can be reduced by gold doping in the N^- region. In so doing, however, the conduction drop is increased. Therefore, it is a trade-off between the current tailing and the conduction drop in the IGT design.

Device Latching

An IGT will latch if the condition for latching, $\alpha_{npn}+\alpha_{pnp}=1$, is reached. This could be caused by the following factors:

1. Large collector current: A large collector current surge causes αs to increase to reach the latching condition, $\alpha_{npn}+\alpha_{pnp}=1$.

2. Fast rate of change of v_{GE} (dv_{GE}/dt) at turn-off: Slow turn-off permits a larger collector current without latching. In other words, rapid turn-off leads to latching at a lower collector current level in the same device because carriers are forced through the NPN transistor during rapid turn-off, causing α_{npn} to increase. This leads to the latching condition, $\alpha_{npn}+\alpha_{pnp}=1$. Slow turn-off prevents latching from happening, because the induced channel turns off slowly and partially shunts the NPN transistor, keeping α_{npn} sufficiently low to avoid latching [3.6].

3. Fast rate of change of v_{CE} (dv_{CE}/dt) at turn-off: When the collector-emitter voltage of an IGT increases too quickly, the displacement current from the junction capacitances will cause α's to increase, which leads to the device latching.

3.3 IGTO DEVICE CONFIGURATION

The IGTO configuration is shown in Figure 3.7, in which Q_1 is a GTO, Q_2 is an IGT and Q_3 is a MOSFET. This configuration requires small current pulses for turn-on or turn-off, similar to the FGT. However, using the IGT instead of a power MOSFET for Q_2, and a GTO rather than a BJT for Q_1 results in a higher voltage capability for the IGTO. This is mainly because both the GTO and the IGT are more efficient high voltage devices.

As mentioned in Section 3.2, an IGT is conductivity-modulated during conduction, while a MOSFET is not. As the voltage rating exceeds 400V, the conduction current density requirement of a power MOSFET becomes very severe to allow a low conduction drop. In other words, it takes a very large chip area to keep the conduction drop at a reasonably low value for a high voltage MOSFET. This is one of the main reasons why power MOSFETs are not cost competitive with bipolar power transistors at voltage ratings higher than 400V. For the IGT, however, the device chip area increases slowly with the voltage rating because of the conductivity modulation effect.

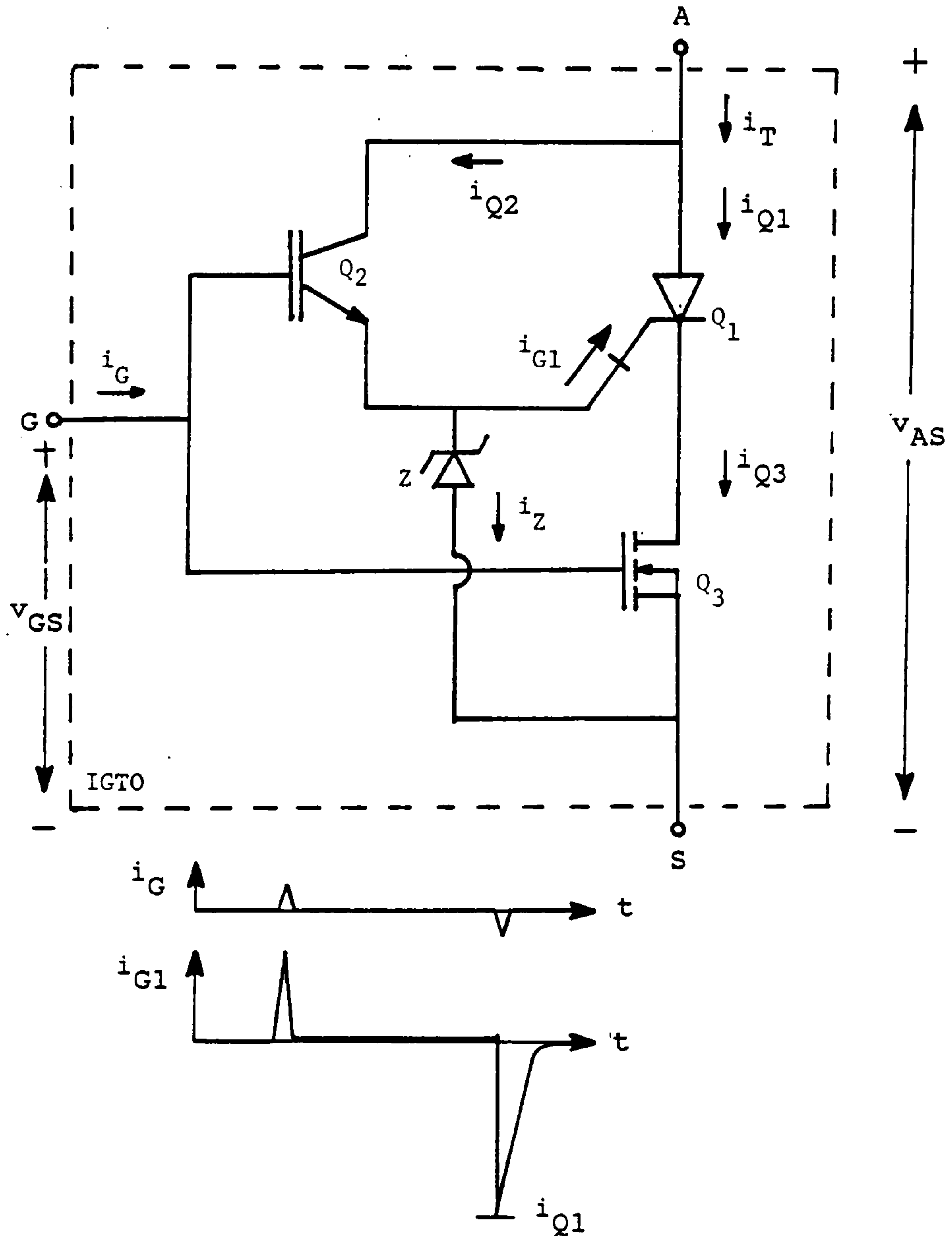


Figure 3.7: IGTO Configuration and Associated Current Waveforms

As the voltage rating exceeds 1000V, a GTO is preferred to a bipolar power transistor when comparing chip area. The IGTO structure presented in this chapter is, therefore, suited for a voltage rating above 1000V. A comparison of the forward current density for a GTO, IGT, BJT and MOSFET devices, with voltage ratings of 600V and 1000V, is shown in Figures 3.8 and 3.9 [3.9]. The chip area requirement is inversely proportional to the current density.

3.4 IGTO OPERATING PRINCIPLE

The basic operating principle of an IGTO is similar to that of an FGT as described in Chapter II.

3.4.1 Turn-on

When the gate drive voltage is high, both Q_2 (IGT) and Q_3 (MOSFET) are turned on. The Q_2 output current serves as the turn-on gate current for Q_1, and the IGTO is turned on.

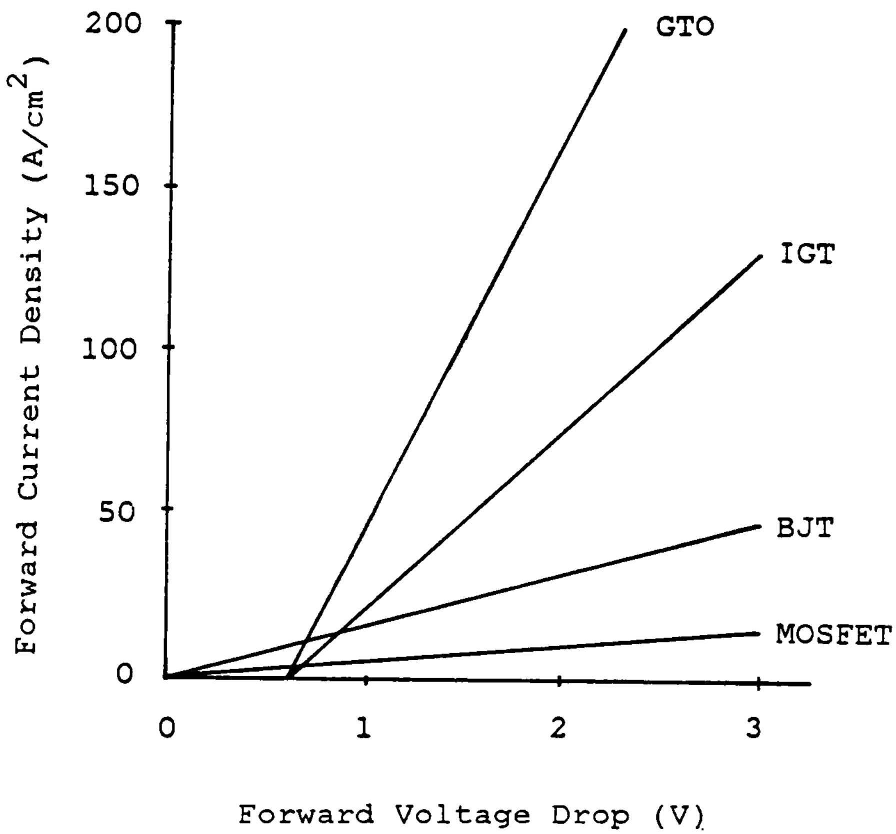


Figure 3.8: Chip Area Comparison Among 600V GTO, IGT, BJT and MOSFET (After [3.9])

3.4.2 Conduction

During the conduction state, the GTO latches and conducts nearly all of the load current. However, the IGT still conducts a very small portion of the load current and feeds it into the GTO gate. This gate current, during conduction, lowers the GTO voltage drop and ensures the GTO is in the conduction state. The I-V characteristics of an IGTO are shown in Figure 3.10.

3.4.3 Turn-off

When the gate drive voltage is low, both Q_2 and Q_3 are turned off and Q_1 is turned off by cathode open. The anode current of Q_1, therefore, flows out of the Q_1 gate terminal to ground through the zener diode, Z. The cathode-open turn-off makes the reverse gate current of the GTO equal to the GTO's anode current, resulting in reliable, fast turn-off.

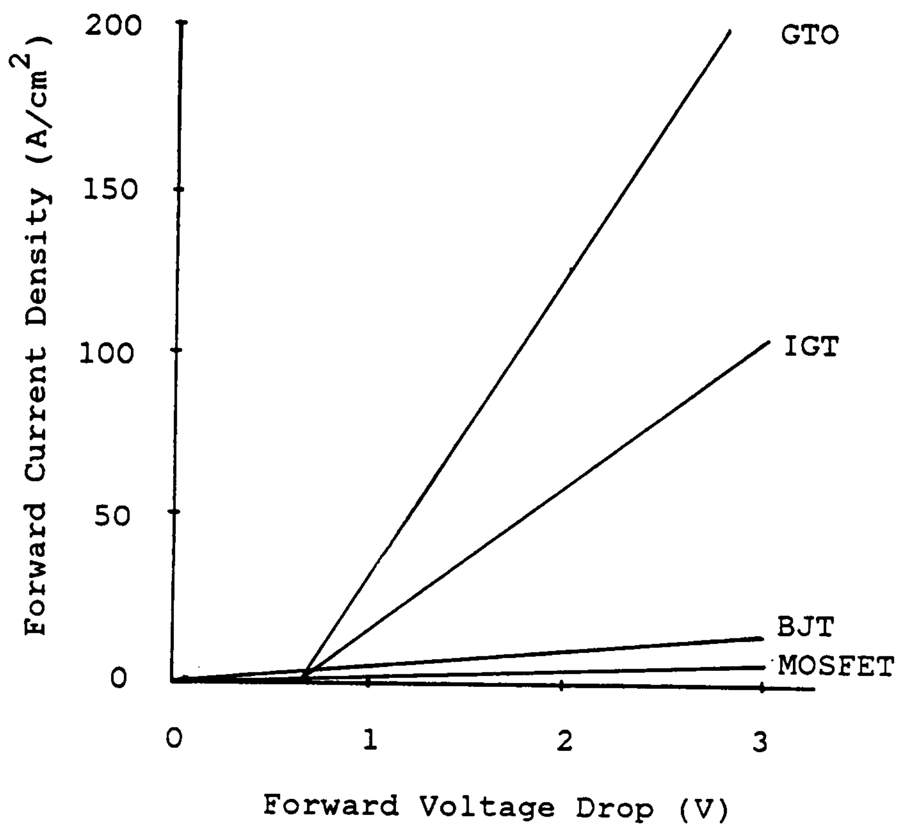
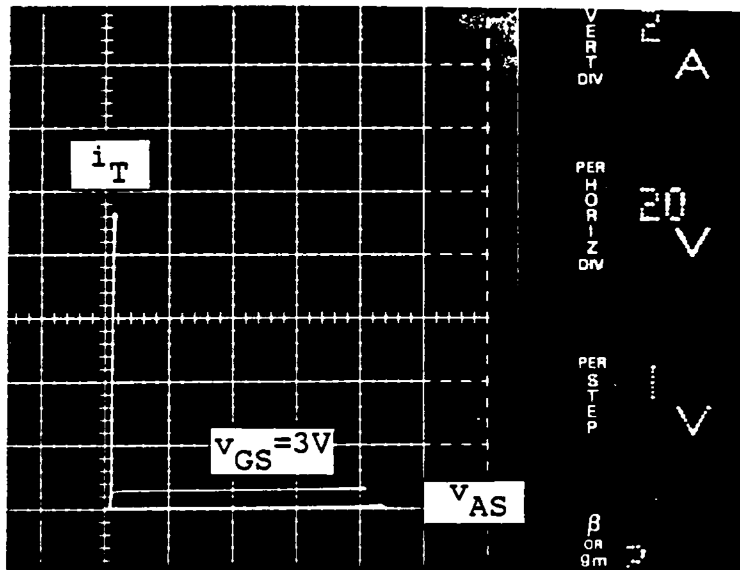


Figure 3.9: Chip Area Comparison Among 1000V GTO, IGT, BJT and MOSFET (After [3.9])



i_T: 2 Amperes/Division
v_{AS}: 20 Volts/Division
v_{GS}: 1 Volt/Step

Q_1: Amperex BTV58-600R
Q_2: General Electric D94FQ4
Q_3: Siemens BUZ15
Z: TCG 135A

Figure 3.10: IGTO I-V Characteristics

3.4.4 Unique IGTO Characteristics

As described in Sections 3.1 and 3.2, there are disadvantages associated with the GTO and the IGT. These disadvantages, however, can be eliminated by using the IGTO configuration as explained below.

Disadvantages of the GTO

1. Requirement of a large reverse gate current for reliable turn-off. A turn-off gain of 3 to 5 is normally required for a GTO. This implies that a large reverse gate current (1/3 to 1/5 the anode current) is needed to turn off a GTO, which is relatively difficult to accomplish in practice. On the contrary, the IGTO has a unity turn-off gain inherently achieved by the cathode-open turn-off scheme. The gate drive circuit for the IGTO is relatively simple.

2. Relatively low dv/dt capability. The GTO has a relatively low dv/dt capability as compared to a bipolar transistor. False triggering of a GTO may occur if the dv/dt limit is exceeded. In the IGTO, the dv/dt capability

is enhanced because Q_3 holds OFF in the blocking state, and consequently a false triggering current can not flow through the gate-cathode junction.

3. Reverse bias second breakdown. The current crowding phenomenon occurs during turn-off because of the "squeezing" process described in Subsection 3.1.2. Therefore, a GTO is susceptible to reverse bias second breakdown. The RBSB ruggedness is improved in an IGTO because the current crowding phenomenon is avoided due to the cathode-open turn-off.

Disadvantages of the IGT

1. Device latching at turn-off. The IGT may latch if the condition, $\alpha_{npn}+\alpha_{pnp}=1$, is satisfied. This is avoided in the IGTO configuration because Q_2 (IGT) conducts a very small amount of current during the conduction state of the IGTO. Therefore, the latching is unlikely to occur. Latching caused by dv/dt is also eliminated because Q_1 (GTO) is operating in the storage time when Q_2 is turned off, so the voltage rise of Q_2 during turn-off is slow.

2. Current tailing. Current tailing is caused by the recombination of a large amount of excess carriers in the N^-

region during turn-off. Since the Q_2 current of an IGTO is very small before turn-off, the current tailing problem plaguing the IGT is eliminated.

3.5 SELECTION OF COMPONENTS

For an IGTO rated at V_X and I_X, the individual components should be selected according to the following guidelines.

3.5.1 Selection of Q1

Because of the cathode-open turn-off, Q_1 is operated to its anode-gate breakdown voltage. Unlike a BJT which may have a V_{CBO} much higher than the V_{CEO}, the anode-gate breakdown voltage is about the same as (or only slightly higher than) the anode-cathode breakdown voltage. This is because the PNP transistor in the GTO structure is normally designed to have a very small current gain. Therefore, the anode-cathode breakdown voltage is used to rate the IGTO voltage rating, V_X.

During conduction, Q_1 takes almost all the load current and Q_2 conducts a very small current equal to the Q_1 gate

current. Therefore, the anode current of Q_1 should be rated at the IGTO's current rating, I_X.

3.5.2 Selection of Q2

Since Q_2 is connected across the anode and gate of Q_1, the voltage rating of Q_2 should be rated at V_X. The current rating of Q_2 depends on the gate drive voltage and load current. During turn-on, Q_2 has a tendency to conduct all the load current. A higher gate drive voltage allows Q_2 to conduct a higher current at turn-on. Nevertheless, as explained in Section 3.4, a higher Q_2 current makes Q_1 conduct more quickly. In addition, Q_1 requires only several hundred milliamperes to turn on. Therefore, Q_2 can be an IGT with a small current rating and a high surge current ability. Fortunately, this requirement corresponds to the IGT characteristics. An IGT can withstand a surge current up to 200 times its steady state current rating.

3.5.3 Selection of Q3

The guideline for selecting Q_3 is the same as in the case of an FGT. Because Q_1 shields the supply voltage from Q_3, Q_3 is not subjected to a high voltage during the OFF

state. A 50V power MOSFET serves well as Q_3. Since Q_3 carries all of the load current during conduction, it should be rated at I_X.

3.5.4 Selection of Z

During conduction, the zener diode breakdown voltage must be greater than the sum of the gate-cathode voltage of Q_1 and the voltage drop of Q_3. During the storage time of Q_1, all the load current is flowing through the zener diode. The zener diode surge current is, therefore, rated at I_X.

Power dissipation of the zener diode, which normally limits the choice of the zener diode, Z, is determined by the zener breakdown voltage, V_Z, the IGTO current rating, I_X and the IGTO operating frequency. The reverse gate-source voltage applied to Q_2 during turn-off is equal to the difference between the zener clamping voltage and the applied reverse gate voltage of the IGTO. The lower the zener clamping voltage is, the lower the reverse voltage across the gate-source junction of Q_2 will be. Therefore, the zener breakdown voltage should be as small as possible, so as not to conduct during the IGTO conduction state.

3.6 EFFECTS OF COMPONENT SELECTION ON IGTO PERFORMANCE

The guideline for selecting the components outlined above is rather general. Once the guideline is followed, the voltage and current ratings should be satisfied. However, the overall IGTO performance will be affected by the components selected.

3.6.1 Selection of Q1

In order to achieve a faster turn-off speed, some GTOs are fabricated with an anode-short structure. The anode-shorted GTO, however, features a degraded di/dt capability and reduced utilization of the chip area. Since the IGTO has an inherent unity turn-off gain, the anode-short is not needed for Q_1 and the chip area utilization of Q_1 is improved.

3.6.2 Selection of Q2

If a slow IGT is used as Q_2 for high frequency and low duty cycle applications, the IGT current may still be high enough at turn-off for latching to occur. A faster IGT can be employed, as Q_2, to relieve this problem, but the conduction drop will be higher.

3.7 ADVANTAGES AND DISADVANTAGES OF THE IGTO

3.7.1 High Voltage and High Current Capabilities

The operation of an IGTO is such that both Q_1 (GTO) and Q_2 (IGT) are subjected to high voltage (equal to the power supply voltage) and Q_3 (MOSFET) is subjected to less than 50V. Both the GTO and the IGT are inherently efficient high voltage devices in conjunction with the bipolar conduction mechanism, while a power MOSFET is an inherently efficient low voltage device. Therefore, the IGTO configuration represents the best combination of various power devices into a single switching device for high voltage applications.

3.7.2 Simple Gate Drive Requirement

Although the GTO is suited for high voltage applications when considering chip area utilization, the gate turn-off current requirement remains so severe (about one-fifth of the conduction anode current) that the GTO is not widely accepted by users. With the proposed IGTO approach, the drive requirement of the GTO is tremendously reduced. A unity reverse current gain for Q_1 is inherent in the IGTO configuration, and the GTO can be reliably turned

off. The only drive current needed for the IGTO is the small surge current during switching for Q_2 and Q_3.

3.7.3 Fast Switching Speed

The IGTO switching speed is mainly determined by the GTO. At turn-on, a good portion of the load current flows through the IGT (Q_2) and functions as the GTO gate current. This large current spike speeds up turn-on of the GTO. During turn-off, because of cathode-open turn-off, a large reverse gate current spike, which is equal to the conduction anode current in magnitude, significantly reduces the GTO's storage time and fall time. Therefore, both turn-on and turn-off switching speeds of the GTO are greatly improved.

3.7.4 Small Chip Areas

Anode shorts are introduced by some GTO manufacturers to improve turn-off characteristics [3.2]. These shorting resistances are intended to increase the switching speed of the GTO during turn-off. However, the shorting resistances reduce the GTO conduction area. Since the IGTO features a fast turn-off speed, due to a unity reverse current gain caused by employing the cathode-open technique, anode shorts

are not necessary and better chip area utilization is possible. As mentioned in Section 3.3, when the voltage rating exceeds 1000 volts, the GTO and the IGT are preferred over the BJT and the power MOSFET, respectively, from the viewpoint of better utilization of the chip area. Since Q_2 is a high voltage but low current device, while Q_3 is a high current but low voltage device, the chip area requirement for both Q_2 and Q_3 is much reduced.

3.7.5 Enhanced Turn-Off Reliability

Since Q_2 and Q_3 can be small chip area devices, the junction capacitances are much smaller than those of comparable individual devices , so the dv/dt capability is enhanced. The dv/dt capability of Q_1 is also enhanced because Q_3 holds OFF in the blocking state, therefore, no false triggering current can flow through the gate-cathode junction of Q_1.

It should be pointed out that a GTO often fails if it latches. The latching of a GTO might be caused by an insufficient reverse gate current during turn-off. On the contrary, the GTO used in the IGTO configuration never latches, because it is turned off by using the cathode-open

scheme. The cathode-open turn-off scheme features a unity turn-off gain which ensures reliable turn-off.

As described in Section 3.2, an IGT may latch during turn-off if a large current is switched. In the IGTO structure, however, the IGT current is reduced to a low current level before turn-off so the latching problem is eliminated.

3.7.6 Disadvantages

The major disadvantage of the IGTO is the complexity of its configuration. It may appear that the conduction drop of Q_3 is a serious disadvantage. However, the significant reduction of switching and gate drive losses outweigh this disadvantage.

3.8 EXPERIMENTAL RESULTS USING DISCRETE COMPONENTS

Listed in Table 3.1 are the four sets of discrete components used to form IGTOs. The low current set is rated at 5A, the medium current set is 15A and the two high current sets are 50A and above. The highest current tested was 100A and the highest voltage was 850V. The gate drive circuit is essentially the same as that used for the FGT testing in Chapter II. No snubber circuit was used in the IGTO tests.

3.8.1 Drive Waveforms

Figure 3.11 shows the gate drive waveforms. Only small charging and discharging current pulses (less than 0.5A) are needed to switch the IGTO on or off.

Figures 3.12 and 3.13 show the GTO gate current for the low and medium current IGTO, respectively. At turn-on, a large current spike is inherent, which rapidly turns on the GTO. At turn-off, a large reverse gate current spike is withdrawn from the GTO anode current which then quickly turns off the GTO. Therefore, fast turn-on and turn-off of a GTO can be accomplished with very little current pulse from the gate drive circuit.

TABLE 3.1

Discrete Components Used for IGTO Testing

Low Current IGTO

Q_1: Amperex BTV58-600R(600V/25A)
Q_2: General Electric D94FQ4 (400V/10A)
Q_3: Siemens BUZ15(50V/35A/0.03 ohm)
Z: TCG 5130A(15V/5W)

Medium Current IGTO

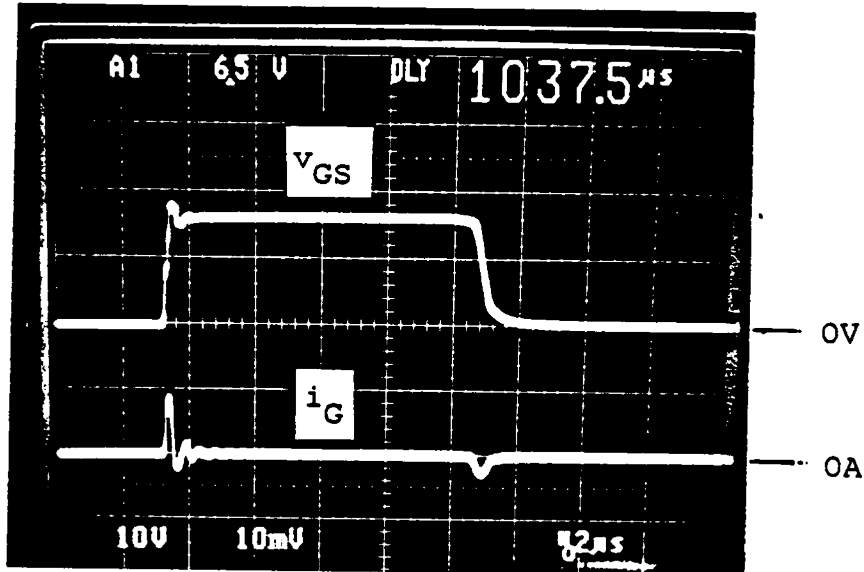
Q_1: Hitachi GFT20A6(600V/25A)
Q_2: RCA RCM10N40 (400V/10A)
Q_3: Siemens BUZ15(50V/35A/0.03 ohm)
Z: TCG 5130A(15V/5W)

High Current IGTO

Q_1: Westinghouse GDM11210(1200V/100A)
Q_2: General Electric D94FQ4(400V/10A)
Q_3: Siemens BUZ15(50V/35A/0.03 ohm)
Z: TCG 5292A(10V/50W)

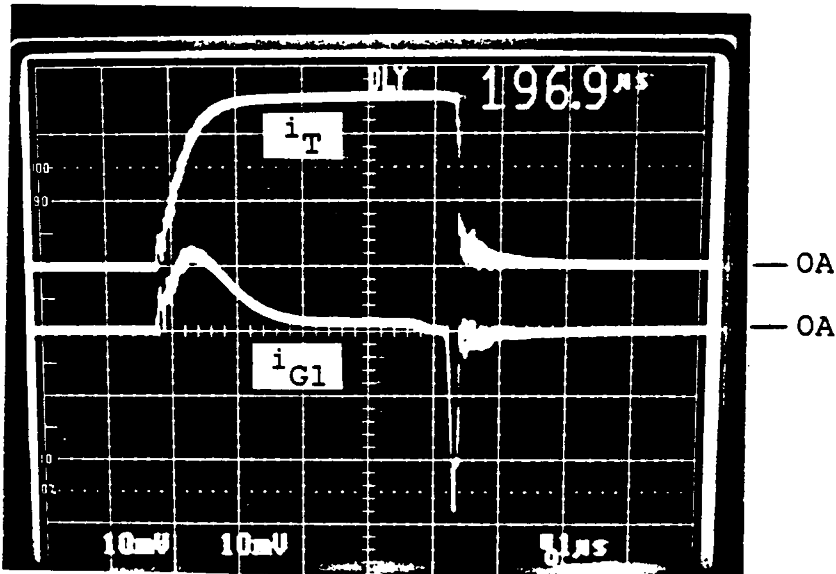
High Voltage High Current IGTO

Q_1: Westinghouse GDM11210 (1200V/100A)
Q_2: Siemens BUZ83 (800V/2.9A/4 ohm)---MOSFET
Q_3: Siemens BUZ15 (50V/35A/0.03 ohm)
Z: TCG 5292A (10V/50W)



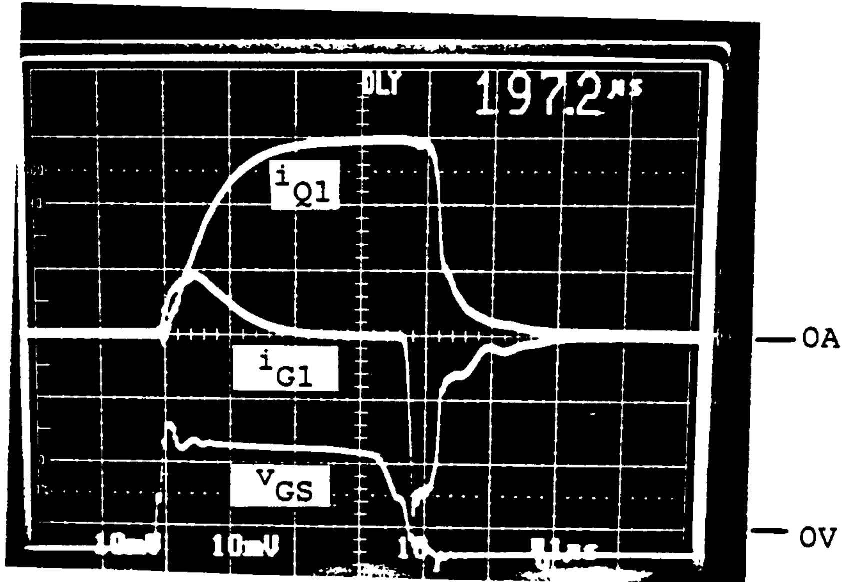
v_{GS}:	10 Volts/Division
i_G:	0.5 Amperes/Division
time:	2 Microseconds/Division
Q_1:	Westinghouse GDM11210
Q_2:	General Electric D94FQ4
Q_3:	Siemens BUZ15
Z:	TCG 5292A

Figure 3.11: IGTO Gate Drive Waveforms



i_T:	2 Amperes/Division
i_{G1}:	2 Amperes/Division
time:	1 Microsecond/Division
Q_1:	Amperex BTV58-600R
Q_2:	General Electric D94FQ4
Q_3:	Siemens BUZ15
Z:	TCG 5130A

Figure 3.12: IGTO Anode and Q1 Gate Current Waveforms of a Low Current IGTO



i_{Q1}:	5 Amperes/Division
i_{G1}:	5 Amperes/Division
v_{GS}:	10 Volts/Division
time:	1 Microsecond/Division
Q_1:	Hitachi GFT20A6
Q_2:	RCA RCM10N40
Q_3:	Siemens BUZ15
Z:	TCG 5130A

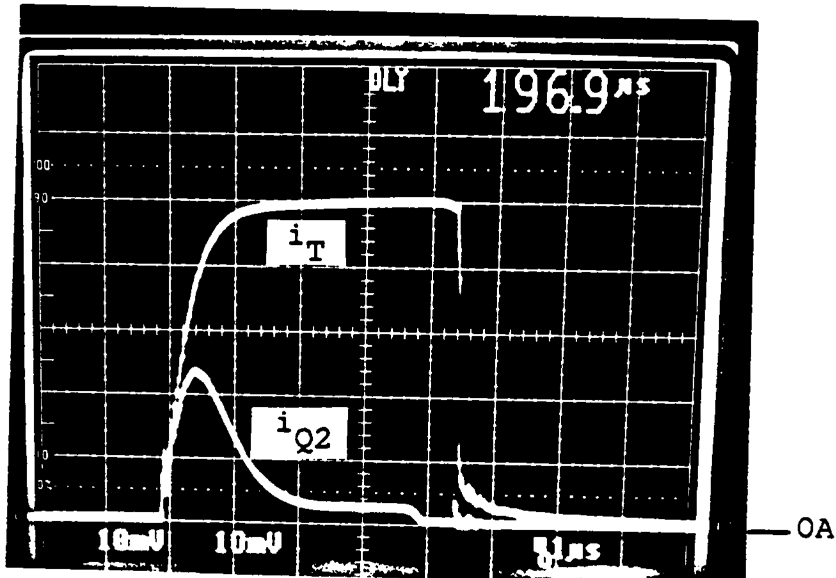
Figure 3.13: Q1 Anode and Gate Current Waveforms of a Medium Current IGTO

The duration of the turn-on current pulse of the Q_1 gate current depends on the choice of Q_1 and Q_2. A slow turn-off Q_2 has a lower conduction voltage drop and tends to have a longer pulse duration.

3.8.2 Turn-on

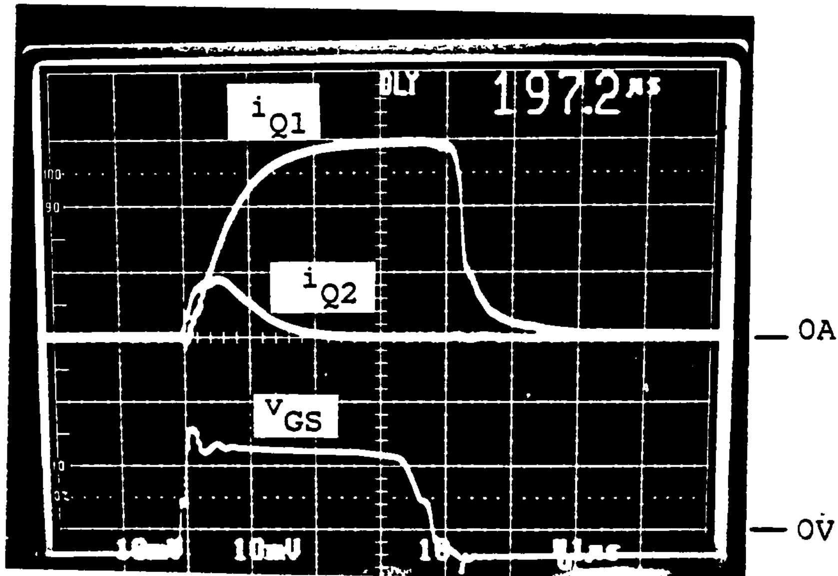
Figures 3.14 and 3.15 show the Q_2 current waveform of the low and medium current IGTO, respectively.

It can be seen that Q_2 has a large current spike during turn-on, but the current is reduced before turn-off. This feature is very important in two respects. Firstly, the large current spike speeds up the turn-on of a GTO. Figure 3.16 shows the GTO is turned on in less than 0.2 μs. Secondly, the tapering off of the Q_2 current greatly reduces the possibility of Q_2 latching at turn-off. An IGT may temporarily enter the latching mode of operation at the beginning of turn-on, but it will unlatch and regain the gate turn-off capability as the current reduces at turn-off. Using an IGT, instead of a MOSFET as Q_2, has another advantage. , Due to the large surge current through Q_2 during turn-on, a high turn-on loss occurs when a MOSFET is used. Since the IGT is conductivity modulated, its conduction drop is smaller than that of a power MOSFET.



i_T:	1 Ampere/Division
i_{Q2}:	1 Ampere/Division
time:	1 Microsecond/Division
Q_1:	Amperex BTV58-600R
Q_2:	General Electric D94FQ4
Q_3:	Siemens BUZ15
Z:	TCG 5130A

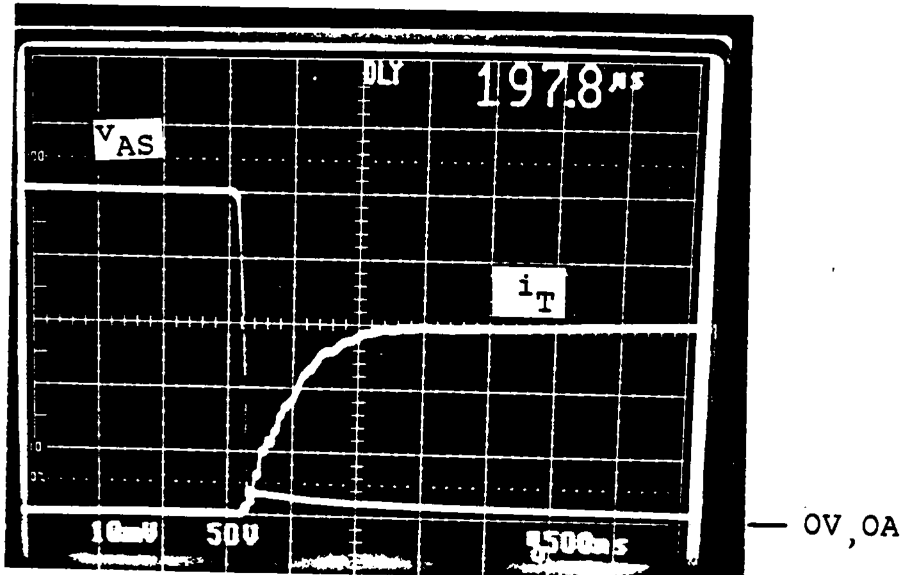
Figure 3.14: IGTO Anode and Q2 Current Waveforms of a Low Current IGTO



i_{Q1}: 5 Amperes/Division
i_{Q2}: 5 Amperes/Division
v_{GS}: 10 Volts/Division
time: 1 Microsecond/Division

Q_1: Hitachi GFT20A6
Q_2: RCA RCM10N40
Q_3: Siemens BUZ15
Z: TCG 5130A

Figure 3.15: Q1 and Q2 Current Waveforms of a Medium Current IGTO



i_T:	5 Amperes/Division
v_{AS}:	50 Volts/Division
time:	500 Nanoseconds/Division
Q_1:	Hitachi GFT20A6
Q_2:	RCA RCM10N40
Q_3:	Siemens BUZ15
Z:	TCG 5130A

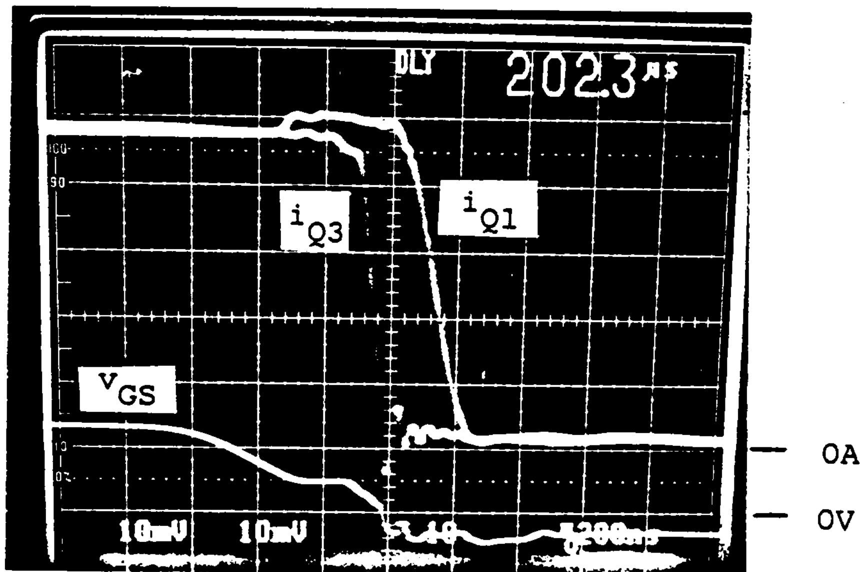
Figure 3.16: IGTO Anode Voltage and Current Waveforms at Turn-on

3.8.3 Turn-off

Figures 3.17 and 3.18 show Q_1 and Q_3 currents at turn-off. It can be seen from both figures that Q_3 turns off very quickly because Q_3 is a MOSFET.

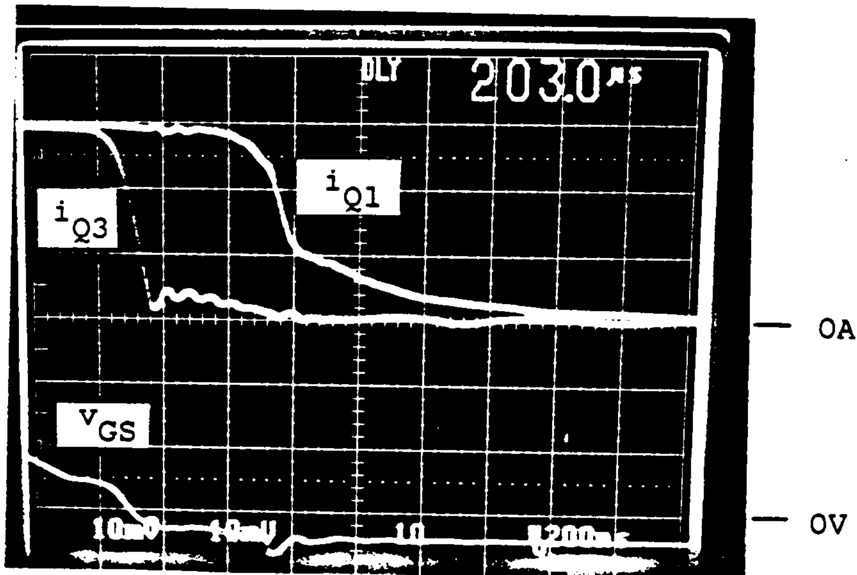
For the low current IGTO, the storage time is about 100 ns, the fall time is 200 ns and the tailing time is 800 ns. For the medium current IGTO, the storage time, fall time and tailing time are 500 ns, 200 ns and 800 ns, respectively. During turn-off the reverse gate current of Q_1 is equal to the anode current, as shown in Figures 3.19 and 3.20 for the low and medium current IGTO, respectively. Figure 3.21 shows the anode voltage waveform of the IGTO. Because the zener diode Z conducts during the storage time of Q_1, the anode voltage is clamped at the zener breakdown voltage.

The high current IGTO has been tested at 100A and 300V, as shown in Figure 3.22. Fast turn-on and turn-off can be seen in Figures 3.23 and 3.24. The current storage time, fall time and tailing time are 1.5 μs, 0.2 μs and 2.5 μs, respectively, as illustratesd in Figure 3.24.



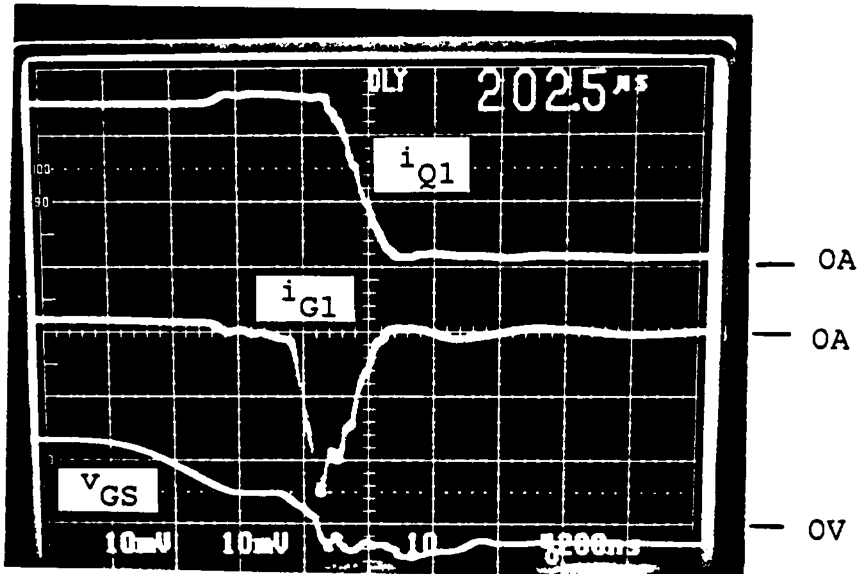
i_{Q1}:	1 Ampere/Division
i_{Q3}:	1 Ampere/Division
v_{GS}:	10 Volts/Division
time:	200 Nanoseconds/Division
Q_1:	Amperex BTV58-600R
Q_2:	General Electric D94FQ4
Q_3:	Siemens BUZ15
Z:	TCG 5130A

Figure 3.17: Q1 and Q3 Current Waveforms of a Low Current IGTO at Turn-off



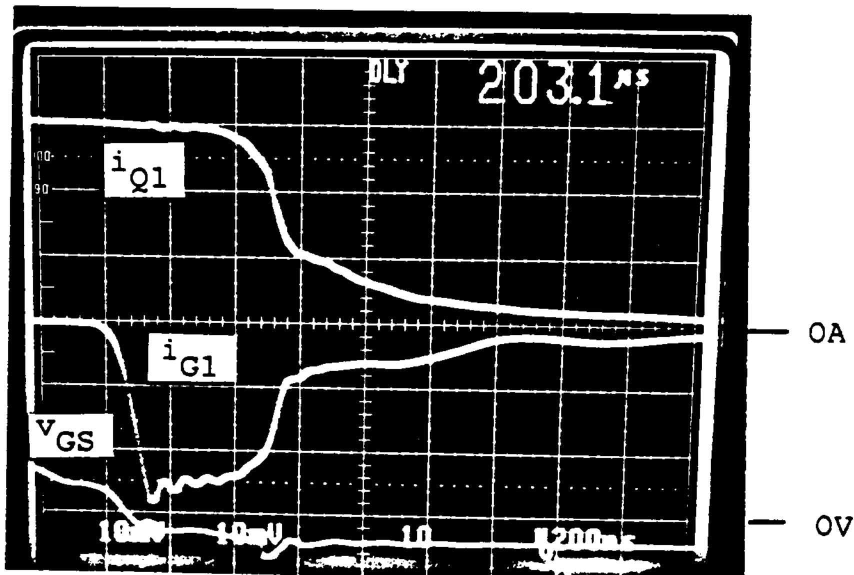
i_{Q1}:	5 Amperes/Division
i_{Q3}:	5 Amperes/Division
v_{GS}:	10 Volts/Division
time:	200 Nanoseconds/Division
Q_1:	Hitachi GFT20A6
Q_2:	RCA RCM10N40
Q_3:	Siemens BUZ15
Z:	TCG 5130A

Figure 3.18: Q1 and Q3 Current Waveforms of a Medium Current IGTO at Turn-off



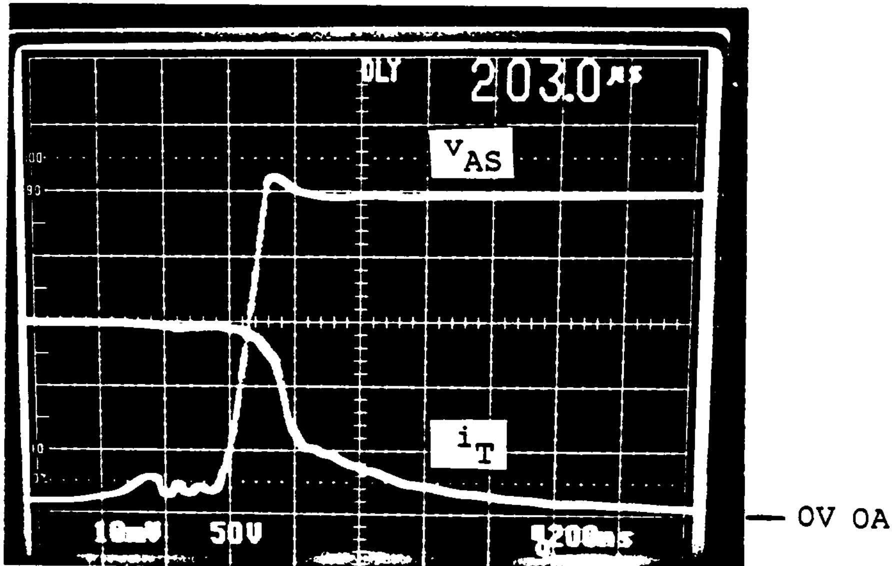
i_{Q1}:	2 Ampere/Division
i_{G1}:	2 Ampere/Division
v_{GS}:	10 Volts/Division
time:	200 Nanoseconds/Division
Q_1:	Amperex BTV58-600R
Q_2:	General Electric D94FQ4
Q_3:	Siemens BUZ15
Z:	TCG 5130A

Figure 3.19: Q1 Anode and Gate Current Waveforms of a Low Current IGTO at Turn-off



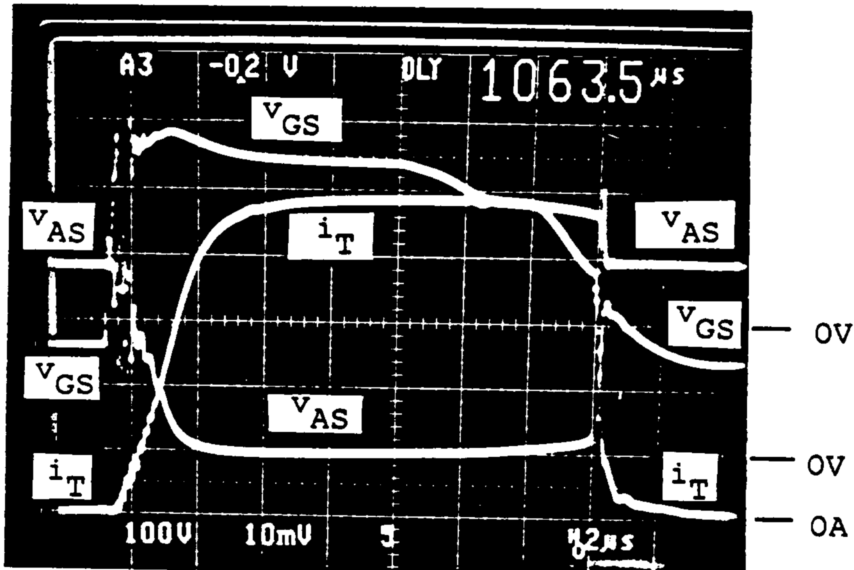
i_{Q1}:	5 Amperes/Division
i_{G1}:	5 Amperes/Division
v_{GS}:	10 Volts/Division
time:	200 Nanoseconds/Division
Q_1:	Hitachi GFT20A6
Q_2:	RCA RCM10N40
Q_3:	Siemens BUZ15
Z:	TCG 5130A

Figure 3.20: Q1 Anode and Gate Current Waveforms of a Medium Current IGTO at Turn-off



v_{AS}:	50 Volts/Division
i_T:	5 Amperes/Division
time:	200 Nanoseconds/Division
Q_1:	Hitachi GFT20A6
Q_2:	RCA RCM10N40
Q_3:	Siemens BUZ15
Z:	TCG 5130A

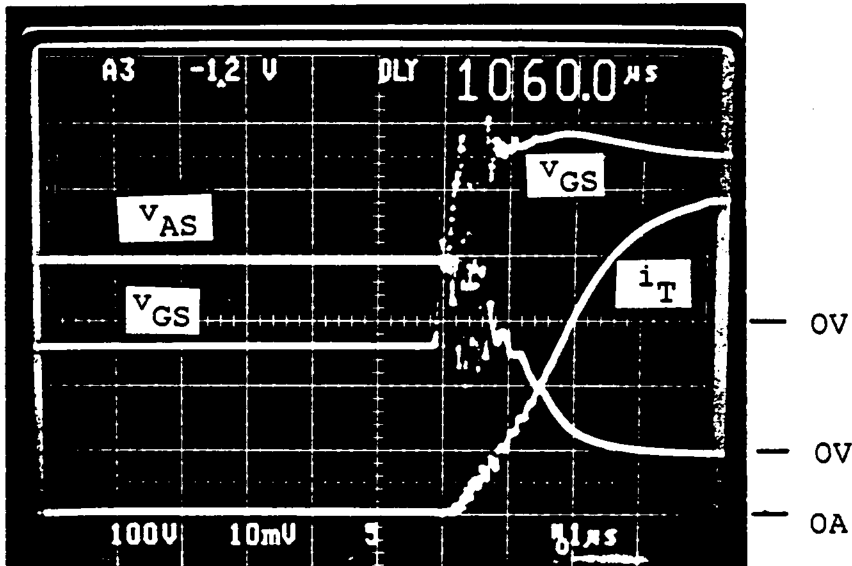
Figure 3.21: IGTO Anode Voltage and Current Waveforms at Turn-off



v_{GS}: 5 Volts/Division
v_{AS}: 100 Volts/Division
i_T: 20 Amperes/Division
time: 2 Microseconds/Division

Q_1: Westinghouse GDM11210
Q_2: General Electric D94FQ4
Q_3: Siemens BUZ15
Z: TCG 5292A

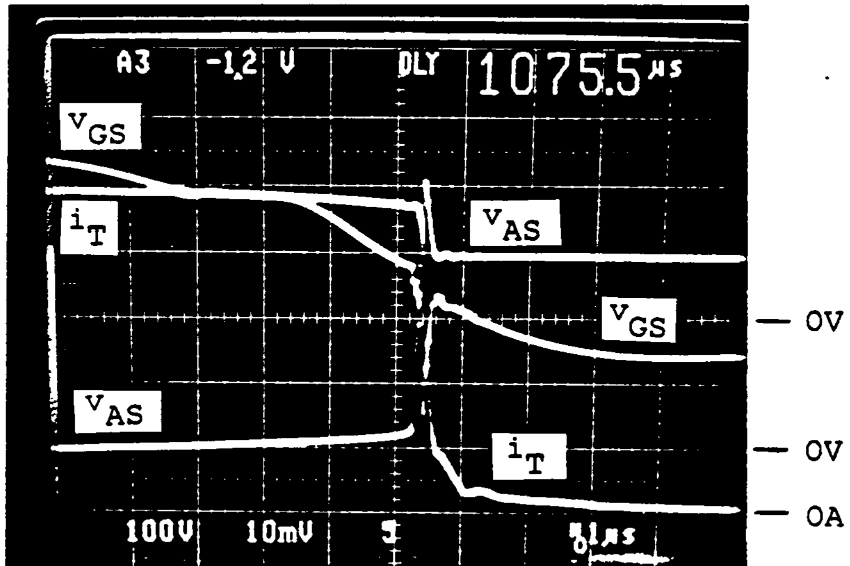
Figure 3.22: IGTO Switching Waveforms of a High Current IGTO at 300V and 100A



v_{AS}: 100 Volts/Division
v_{GS}: 5 Volts/Division
i_T: 20 Amperes/Division
time: 1 Microsecond/Division

Q_1: Westinghouse GDM11210
Q_2: General Electric D94FQ4
Q_3: Siemens BUZ15
Z: TCG 5292A

Figure 3.23: IGTO Turn-On Waveforms of a High Current IGTO at 300V and 100A



v_{AS}:	100 Volts/Division
v_{GS}:	5 Volts/Division
i_T:	20 Amperes/Division
time:	1 Microsecond/Division
Q_1:	Westinghouse GDM11210
Q_2:	General Electric D94FQ4
Q_3:	Siemens BUZ15
Z:	TCG 5292A

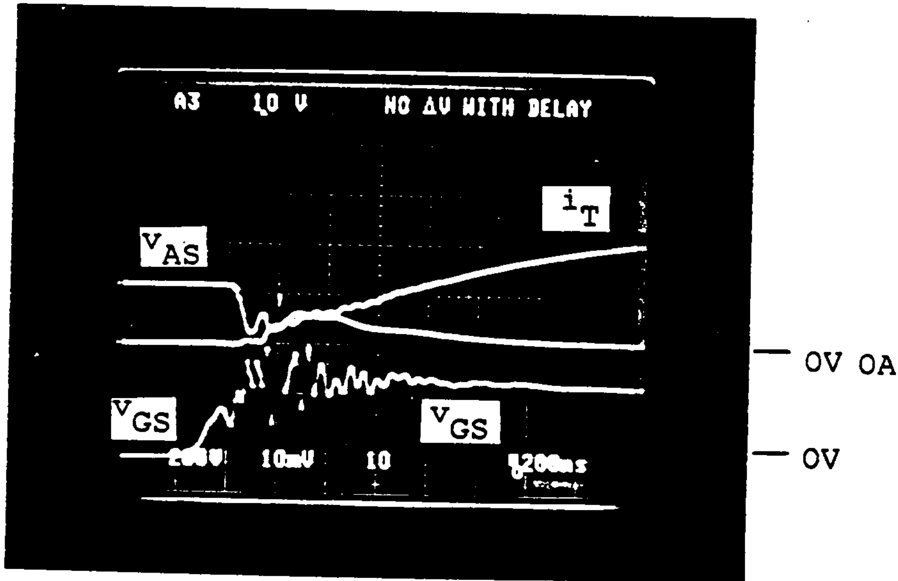
Figure 3.24: IGTO Turn-Off Waveforms of a High Current IGTO at 300V and 100A

Because the highest voltage rating of the IGT currently available is 500V, a high voltage power MOSFET (BUZ83, measured BV_{DSS}=900V) is instead used as Q_2 for the high voltage (850V) and high current (50A) test. The switching waveforms at turn-on and turn-off are shown in Figures 3.25 and 3.26, respectively. As shown in Figure 3.25, the anode voltage waveform of this high voltage IGTO exhibits a high conduction drop during turn-on. This is caused by the voltage drop across Q_2 (MOSFET) which has a high ON-resistance.

The improvement of turn-off speeds as compared to those of the GTO turned off conventionally is summarized in Table 3.2.

3.8.4 Reverse Bias Second Breakdown

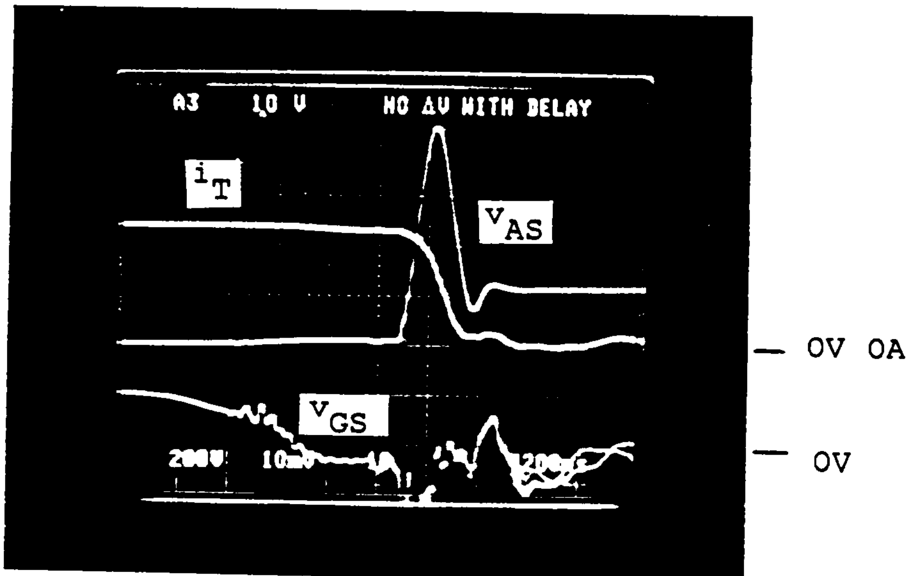
The RBSB phenomenon in the GTO is seldom discussed in the literature. It is generally believed that the RBSB phenomenon occurring in the GTO is similar to that in the BJT. During turn-off, the lateral voltage drop, caused by the lateral gate current flow, "squeezes" the anode-cathode current toward the center of the cathode stripe, resulting in an intense local current density. This high current



v_{AS}: 200 Volts/Division
i_T: 20 Amperes/Division
v_{GS}: 10 Volts/Division
time: 200 Nanoseconds/Division

Q_1: Westinghouse GDM11210
Q_2: Siemens BUZ83
Q_3: Siemens BUZ15
Z: TCG 5292A

Figure 3.25: IGTO Anode Voltage and Current Waveforms of a High Voltage and High Current IGTO at Turn-on



v_{AS}: 200 Volts/Division
i_T: 20 Amperes/Division
v_{GS}: 10 Volts/Division
time: 200 Nanoseconds/Division

Q_1: Westinghouse GDM11210
Q_2: Siemens BUZ83
Q_3: Siemens BUZ15
Z: TCG 5292A

Figure 3.26: IGTO Anode Voltage and Current Waveforms of a High Voltage and High Current IGTO at Turn-off

TABLE 3.2

Summary of Improvement Using IGTO Configuration

Device	Storage Time	Fall Time	Tailing Time
BTV58-600R @ 5A Turn-off gain = 2.5	0.4	0.3	5.0
When Used in IGTO:	0.1	0.2	0.8
GDM11210 @ 50A Turnoff gain = 3	3.5	0.5	5.0
When Used in IGTO:	1.5	0.2	2.5

.Same GTO forward gate current (0.4A) for each case
.Time in microsecond

density, together with a high field, causes an avalanche injection in the P-N^+ junction, and RBSB occurs. There is no mechanism for the current constriction to reach avalanche injection in the IGTO configuration, because the cathode current is zero once Q_3 turns off. However, this conclusion has not yet been experimentally verified. To verify this conclusion, a non-destructive GTO RBSB tester is needed, which is, as yet, unavailable.

Since the PNP transistor in the GTO structure has a very small current gain, the difference between the anode-gate breakdown voltage, V_{AGO}, and the anode-cathode breakdown voltage, V_{AKO}, is small. For example, the measured values of V_{AKO} and V_{AGO} are 1300V and 1400V, respectively, for the Amperex GTO BTV58-600R. Therefore, the improvement of Reverse Bias Safe Operating Area (RBSOA) in the IGTO is not as great as that of the FGT. However, for the same voltage rating, the maximum interruptible anode current for the IGTO is much greater than that of a conventionally turned off GTO. This is due to the inherent unity turn-off gain of the IGTO.

3.9 REPLACING THE ZENER DIODE WITH A P-CHANNEL IGT

A zener diode is able to withstand a very high pulsed power, depending on the duty-cycle and the pulse width. For high-current, high-frequency applications, however, the power dissipation of the zener diode, Z, may exceed its steady-state power rating. For example, if an IGTO is to be switched at 100A and 50KHz with a storage time of 1 microsecond, then 50W will be dissipated on a 10V zener of the IGTO. An alternative to the zener diode is replacing Z with a P-channel IGT. Figure 3.27 shows an IGTO employing a P-channel IGT instead of the zener diode. When the gate voltage is high, Q_2 and Q_3 are turned on while Q_4 is off. When the gate voltage is low, Q_4 is gated on but Q_2 and Q_3 are turned off. The GTO anode current flows through Q_4 to ground during the storage time. Therefore Q_4 functions in the same way a zener diode does. Figure 3.28 shows the Q_4 current waveform of an IGTO using a P-channel IGT as Q_4. The P-channel IGT has been reported [3.10] but is not commercially available.

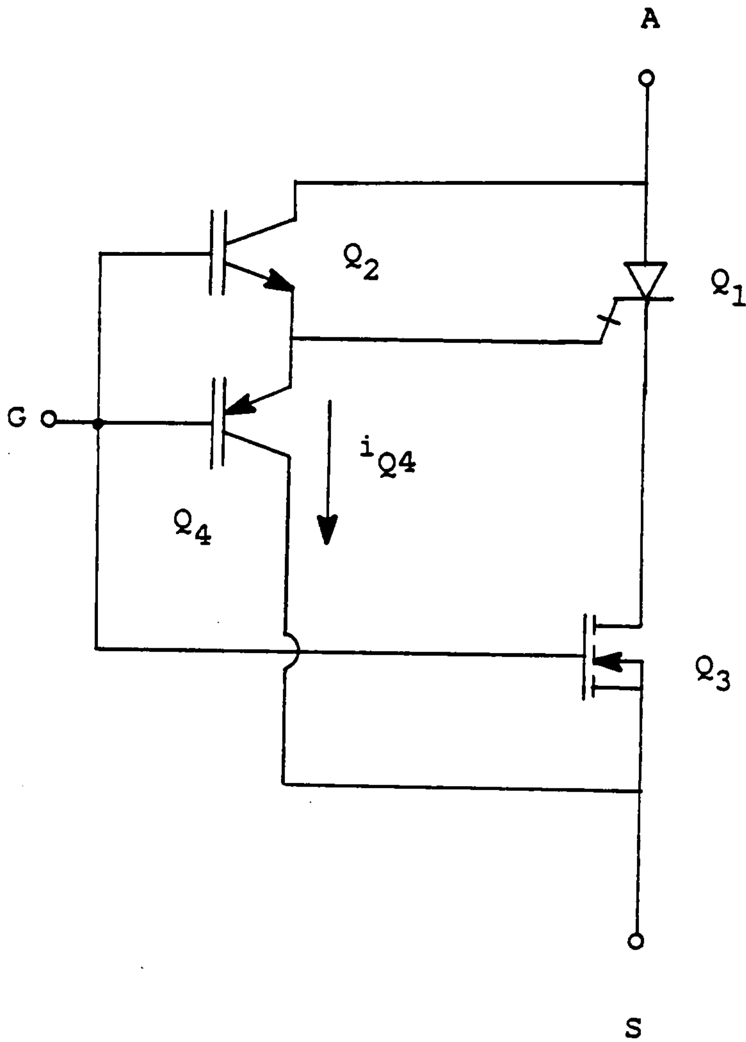
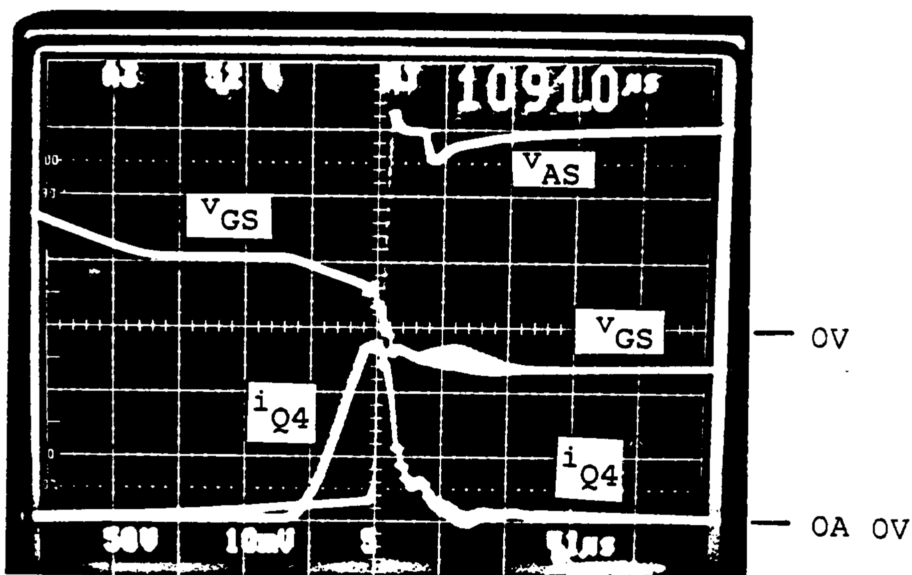


Figure 3.27: IGTO Configuration with Z Replaced by a P-channel IGT



v_{GS}: 5 Volts/Division
i_{Q4}: 5 Amperes/Division
v_{AS}: 50 Amperes/Division
time: 1 Microsecond/Division

Q_1: Westinghouse GDM11210
Q_2: General Electric D94FQ4
Q_3: Siemens BUZ15
Q_4: International Rectifier IRF9530

Figure 3.28: Q4 Current Waveform

Chapter IV

APPLICATION CHARACTERISTICS

In this chapter, application characteristics of both the FGT and IGTO are investigated. Presented in this chapter are: device reverse blocking capability; temperature effect on the forward voltage blocking capability, on switching times, and on conduction voltage drop; paralleling of the devices; and power loss distribution. Two half-bridge inverters were built and tested to study the performance of the IGTO in high frequency inverter applications. Projection of the device ratings and the ultimate device limitation is also presented.

4.1 REVERSE BLOCKING CAPABILITY

A device's reverse blocking capability is required in some applications. An FGT has no reverse blocking capability. An IGTO may or may not have the reverse blocking capability depending on the design of both the IGT and the GTO.

4.1.1 FGT Reverse Blocking Capability

An FGT is inherently a reverse conducting device. The reverse current paths are shown in Figure 4.1. Because a reverse diode is normally associated with a MOSFET, due to the necessity of emitter shorting to minimize the dv/dt problem [4.1], both Q_2 and Q_3 could conduct the current in the reverse direction. As shown in Figure 4.1, the reverse current, path 1, flows from the FGT's source through the reverse diode of Q_3, through the reverse active region of Q1 to the FGT's collector. Path 2 is from the source terminal of the FGT through the zener diode, Z, and through the reverse diode of Q_2 to the FGT's collector.

4.1.2 IGTO Reverse Blocking Capability

The reverse blocking capability of the IGTO depends on the design of both the GTO and the IGT [4.2]. If either is designed to have the reverse conducting capability, then the IGTO cannot block the reverse current, as shown in Figure 4.2. Path 1 begins at the source of the IGTO and continues through the reverse diode of Q_3 and through the GTO to the IGTO's anode. Path 2 is from the IGTO's source through the zener diode and the IGT to the anode of the IGTO.

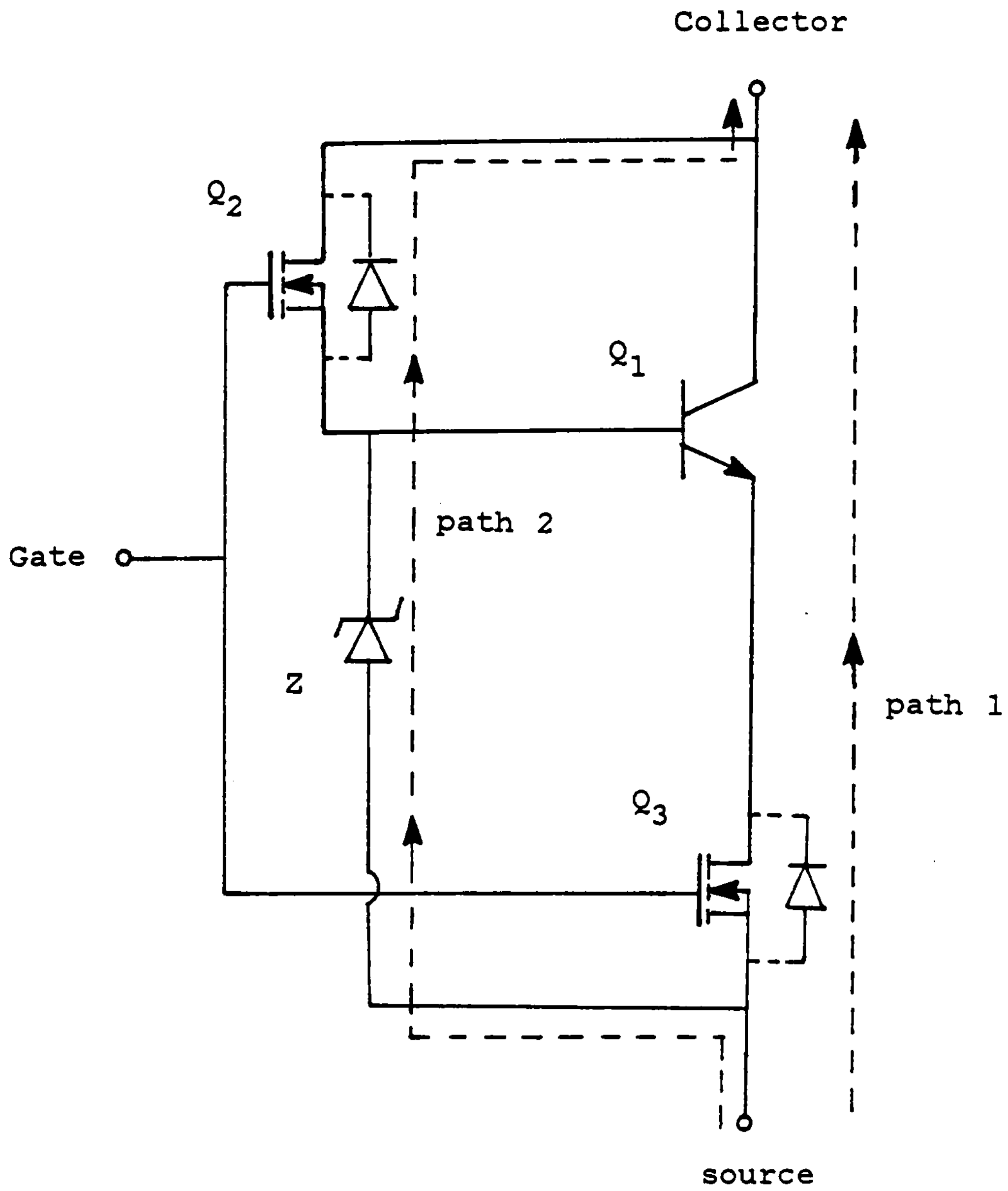


Figure 4.1: Reverse Current Path of FGT

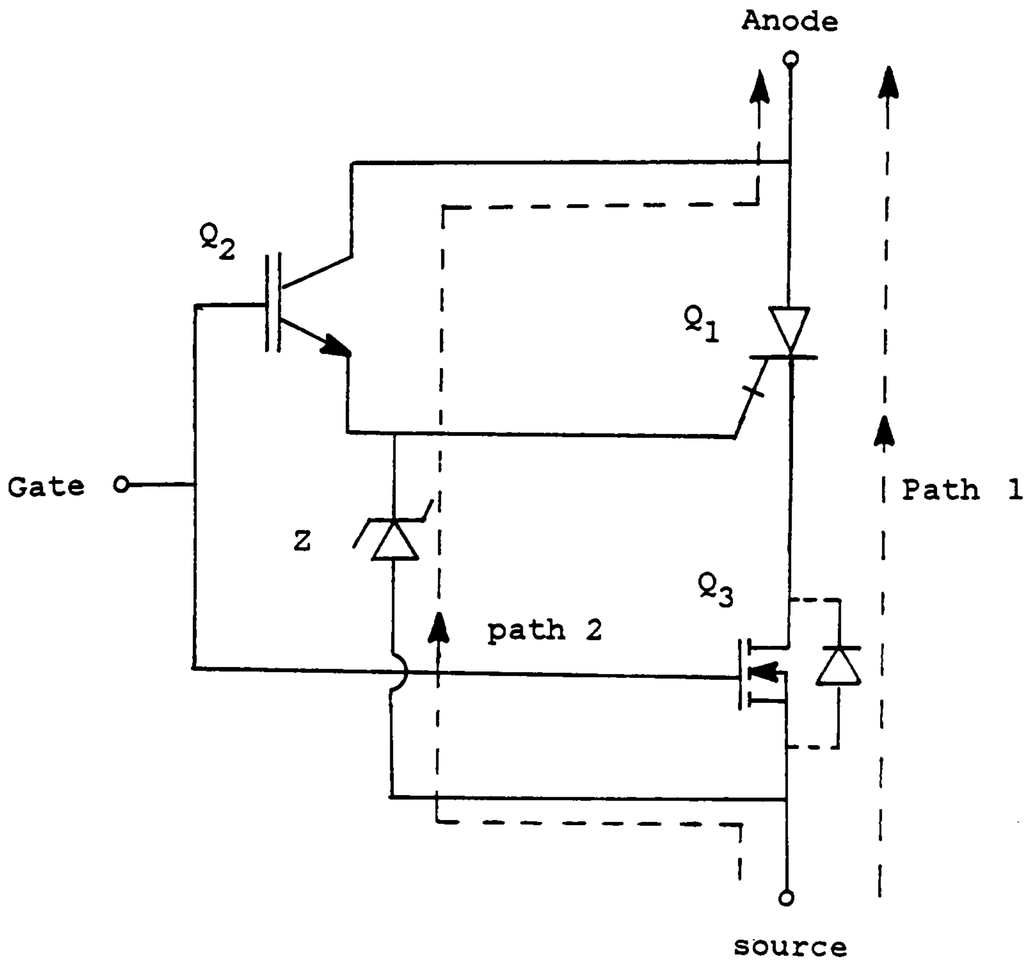


Figure 4.2: Reverse Current Path of IGTO

4.2 TEMPERATURE EFFECT

The temperature effect plays an important role in the performance of power devices as they are usually operated at elevated temperatures. The influence of temperature on the switching time, conduction voltage drop and forward blocking voltage for both the FGT and IGTO is discussed in this section.

4.2.1 Temperature Effect on Switching Time

4.2.1.1 FGT Switching Time

The switching time of an FGT is mainly determined by Q_1 (BJT). Since the life time of minority carriers increases with increasing temperature, the turn-off time will increase with increasing temperature. Figure 4.3 shows the variation of the storage time and the fall time with the temperature for a BJT (T1115) and an FGT. As shown in Figure 4.3, both the storage time and the fall time of a single BJT increase with increasing temperature, whereas there is no noticeable change in the FGT's switching time.

4.2.1.2 IGTO Switching Time

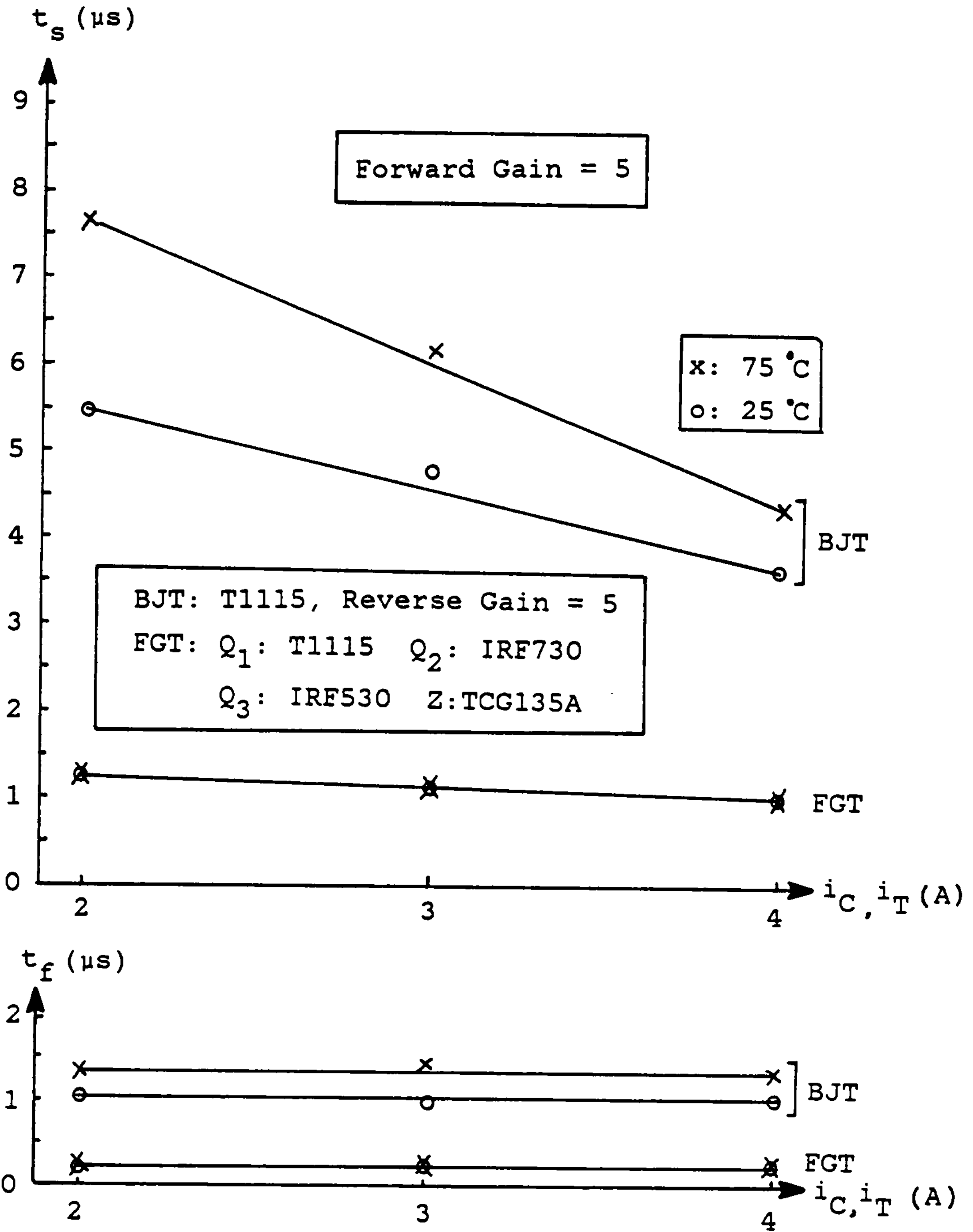


Figure 4.3: Temperature Effect on Switching Time for BJT and FGT

The IGTO's switching time is mainly determined by that of the GTO (Q_1). Figure 4.4 shows the variation of the storage time, fall time and tailing time with temperature for a GTO (GDM11210) and an IGTO. Because of the increase in the carriers' life time with a higher temperature, the switching time is increased at elevated temperatures in the single GTO. Although the IGTO's switching time also increases with increasing temperature, the temperature effect is much less pronounced, due to the significant reduction of the switching time by a unity turn-off gain.

4.2.2 Temperature Effect on Voltage Drop

4.2.2.1 FGT Voltage Drop

The conduction voltage drop of the FGT is attributed by the voltage drop across Q_2, the base-emitter voltage of Q_1 (BJT) and the voltage drop across Q_3 (MOSFET). The base-emitter saturation voltage decreases by 0.1V to 0.2V for a temperature variation from 25 degrees to 125 degrees [4.3]. Since the ON-resistance of a power MOSFET almost doubles from 25 degrees to 125 degrees [4.4], the ON-resistance of Q_2 increases as temperature increases, but the DC current

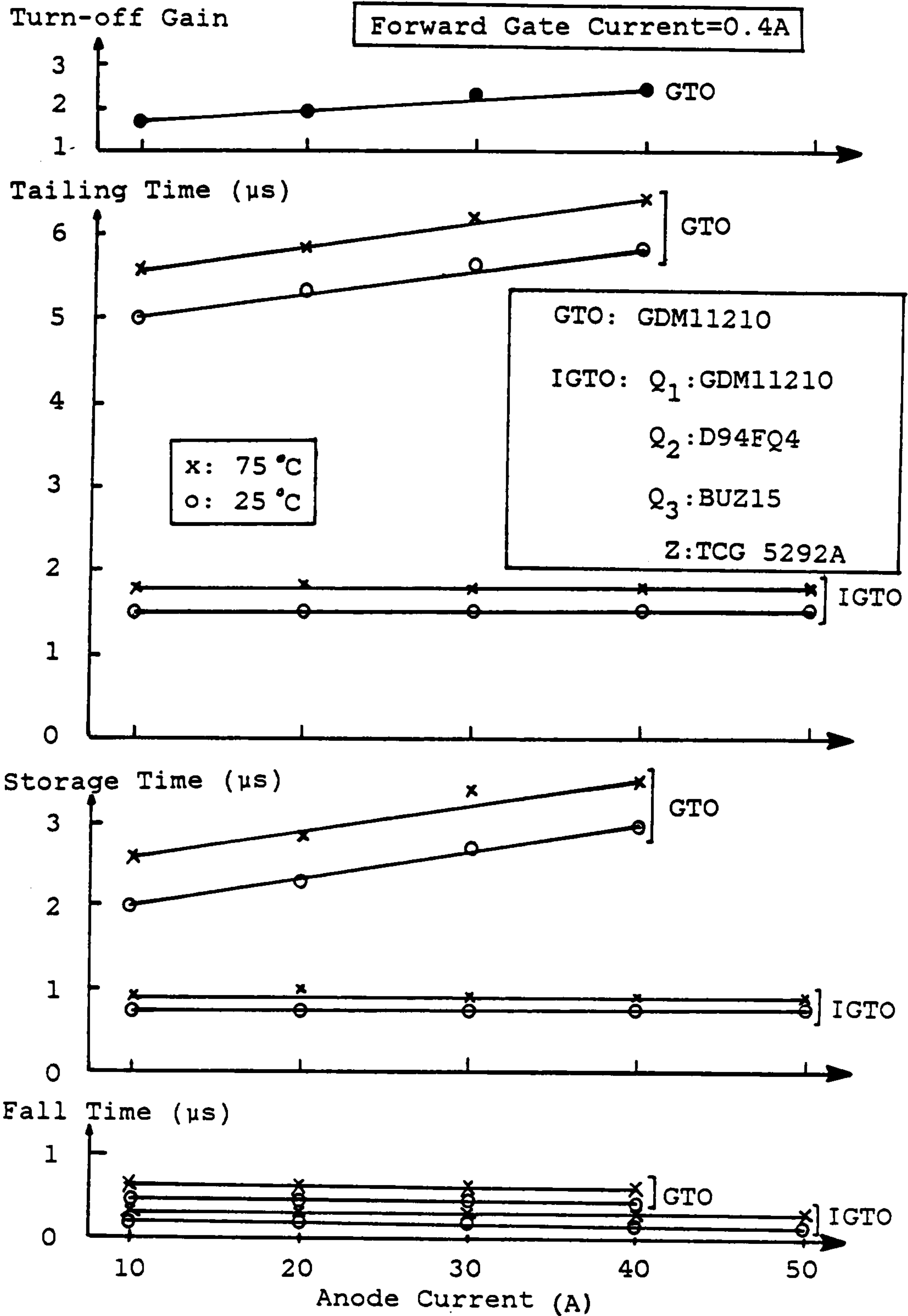


Figure 4.4: Temperature Effect on Switching Time for GTO and IGTO

gain of Q_1 (BJT) also increases with increasing temperature [4.5]. As the total conduction drop is the sum of the voltage drop of Q_2, the base-emitter voltage of Q_1 and the voltage drop of Q_3, the overall temperature effect is that the voltage drop of an FGT increases with increasing temperature.

4.2.2.2 IGTO Voltage Drop

The conduction voltage drop of an IGTO increases with increasing temperature as well. The ON-resistance of the IGT (Q_2) is modulated during conduction so that the temperature effect is small. The conduction drop of Q_1 decreases a few tenths of a volt from 25 degrees to 125 degrees [4.6], but R_{ON} of Q_3 almost doubles over the same range of increasing temperature. Therefore, the conduction voltage drop of an IGTO increases with increasing temperature.

4.2.3 Temperature Effect on Forward Voltage Blocking Capability

Figure 4.5 shows the forward voltage blocking capability of various power semiconductor devices. The voltage blocking capability of a power diode increases with increasing temperature due to the decrease of the ionization coefficient with a higher temperature [4.7]. For a GTO without a cathode-short, the forward voltage blocking capability decreases rather rapidly with increasing temperature [4.8]. However, for a cathode-shorted GTO, the decrease is less steep, because the cathode-short diverts the leakage current from the base-emitter junction of the NPN transistor in a GTO structure. For a BJT, the forward voltage blocking capability decreases with the increasing temperature because of the increase of leakage current and, consequently, current gain at low current levels [4.5]. The forward voltage blocking capability of a power MOSFET increases with increasing temperature [4.9], even a parasitic NPN transistor is existent. Because of the use of the emitter-short to suppress the effect of the parasitic transistor, the breakdown voltage of a power transistor is determined by that of the P-N$^+$ junction which increases at a temperature. Regarding the FGT and the IGTO, the forward voltage blocking capability remains constant or even

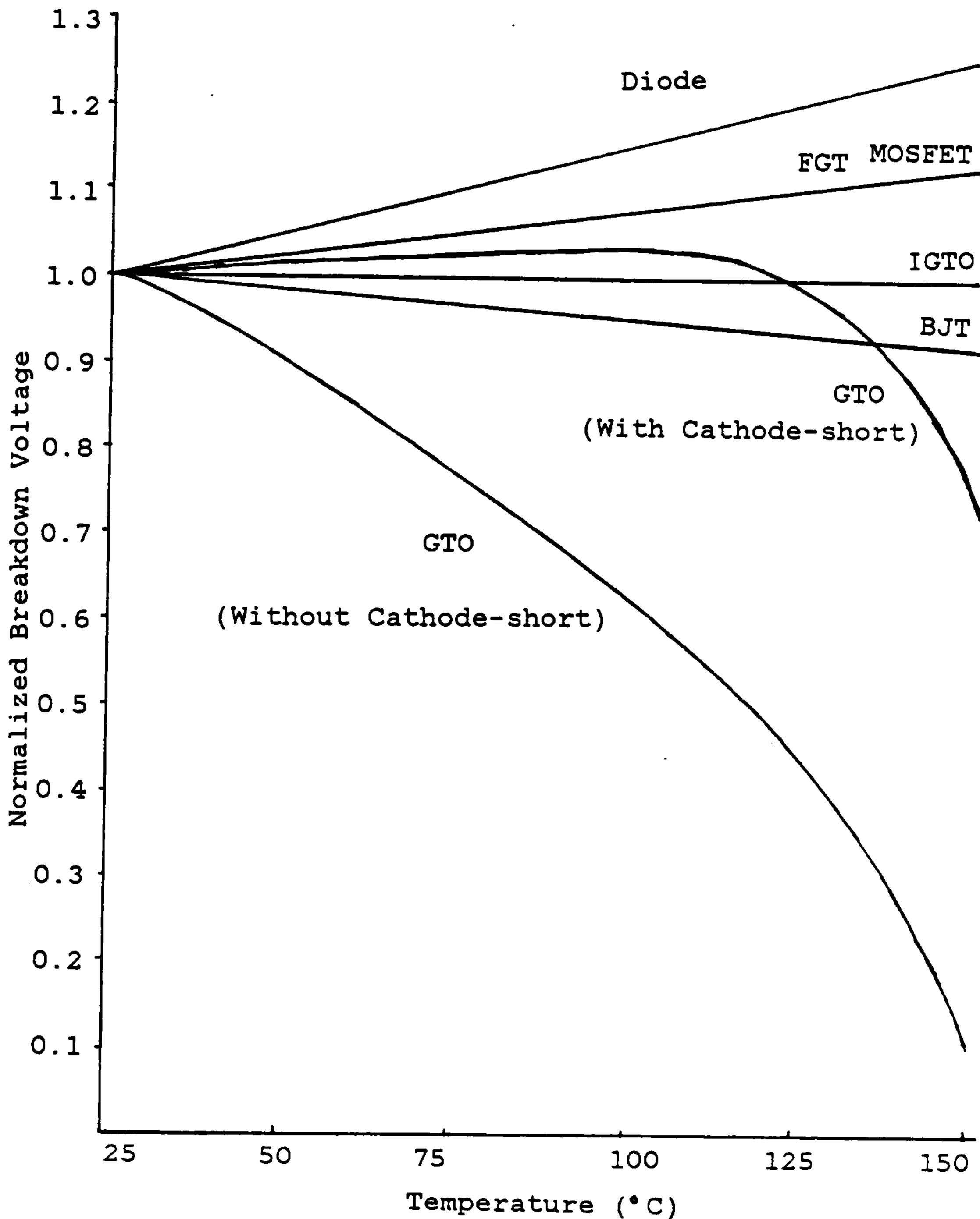


Figure 4.5: Variation of the Blocking Voltage Capability for Various Power Semiconductor Devices with the Temperature

increases slightly with increasing temperature, as described in the following.

4.2.3.1 FGT Forward Voltage Blocking Capability

Q_1 is off during the OFF state of an FGT and the reverse-biased collector-base junction blocks the high voltage. As mentioned earlier, the avalanche breakdown voltage of this junction increases at a higher temperature. Also Q_2 has a positive temperature coefficient for breakdown voltage. Therefore, the forward blocking capability of an FGT increases with increasing temperature.

4.2.3.2 IGTO Forward Voltage Blocking Capability

The P-N^- junction of the GTO (Q_1) is reverse biased in a forward blocking mode when blocking full voltage. Since the N^- epitaxial layer is very wide in a practical thyristor design, the breakdown behavior of the wide base PNP transistor approaches the avalanche breakdown of a reverse biased P-N diode. The transistor action is nonexistent due to a negligible base transport factor. Because the

avalanche breakdown voltage of a reverse biased P-N diode has a positive temperature coefficient, Q_1 of the IGTO dose also. Also Q_2 has a positive temperature coefficient for its breakdown voltage [4.10]. Therefore, the forward blocking capability of an IGTO increases with the temperature.

4.3 DEVICE PARALLELING

When paralleling devices it is important to assure safe operation of each paralleled device. The key parameter to be monitored is the current shared among paralleled devices during both the conduction period and the switching period [4.11].

4.3.1 Paralleling FGT

Paralleling BJTs is not as easy as paralleling power MOSFETs because the former exhibits a negative temperature coefficient of the collector-emitter voltage. During turn-off, the BJT with the longest storage time must take full load current once the other devices, with shorter storage times, turn off. This may cause a BJT failure if the current rating is exceeded.

4.3.1.1 Current Sharing During Conduction

As described in Section 4.2, the conduction drop of an FGT increases with increasing temperature. This characteristic makes it easier for current sharing among paralleled FGTs during conduction.

4.3.1.2 Current Sharing During Turn-on

The threshold voltage of the FGT has to be matched in order to assure proper current sharing during turn-on, since an FGT with the lowest threshold voltage tends to conduct the current earlier.

4.3.1.3 Current Sharing During Turn-off

The storage time of Q_1 is the key parameter to be matched for a proper current sharing during turn-off. This is similar to the device paralleling of conventional bipolar power transistors; however, in the FGT configuration, the effect of the storage time mismatch is minimized. The storage time of a BJT depends on the device recombination rate as well as the reverse current gain. In the FGT, the reverse current gain of Q_1 (BJT) is unity, which is the

predominant factor in determining the storage time. In other words, the variation of the storage time among the paralleled devices is minimized, which makes the paralleling easier.

4.3.2 Paralleling IGTO

A GTO is a bipolar device which needs precautions [4.12] to assure proper device paralleling. In the IGTO configuration, the device paralleling is made easier as described in the following.

4.3.2.1 Current Sharing During Conduction

As described in Section 4.2, an IGTO has a positive temperature coefficient for its conduction voltage drop. This makes it easier for current sharing among paralleled IGTOs.

4.3.2.2 Current Sharing During Turn-on

The threshold voltage of the IGTO has to be matched in order to assure current sharing during turn-on because an IGTO with the lowest threshold voltage tends to conduct full load current at turn-on.

4.3.2.3 Current Sharing During Turn-off

The storage time of Q_1 should be matched to have proper current sharing during turn-off. In the IGTO configuration, the effect of the storage time mismatch is minimized. When a slower IGTO is paralleled with others, the initial anode current of the slower IGTO will increase when other IGTOs come out of the storage phase. The higher anode current, however, will speed up the turn-off process of the slower IGTO, because a larger reverse gate current is provided to turn off the slower IGTO. Therefore, the device paralleling of the IGTO is easier.

4.4 POWER LOSS DISTRIBUTION

The power loss distributions for an FGT operated at 400V and 20A, under operating frequencies of 20KHz, 50KHz and 100KHz, are listed in Table 4.1. The load is assumed to be an infinite inductor and the FGT is assumed to operate at a 50% duty-cycle. Device parameters for calculating the loss are included in Table 4.1, according to the switching performances of the FGT presented in Chapter II.

TABLE 4.1

Power Loss for 400V/20A FGT

Loss (W)	Q_1	Q_2	Q_3	Z	FGT
@20KHz					
Conduction	18.2	0.9	6.0	0.0	25.1
Switching	25.7	5.5	0.8	0.4	32.4
Total	43.9	6.4	6.8	0.4	57.5
@50KHz					
Conduction	18.2	0.9	6.0	0.0	25.1
Switching	64.3	13.8	2.0	1.0	81.1
Total	82.5	14.7	8.0	1.0	106.2
@100KHz					
Conduction	18.2	0.9	6.0	0.0	25.1
Switching	128.5	27.5	4.0	2.0	162.0
Total	146.7	28.4	10.0	2.0	187.1

Assumptions:
Constant inductive load current, 50% duty-cycle.
FGT: Q_1: $V_{BE(ON)}$=1V, $t_r=t_s=t_f$=200ns, h_{FE}=10.
Q_2: R_{ON}=0.55 ohm, $t_r=t_f$=200ns.
Q_3: R_{ON}=0.03 ohm, $t_r=t_f$=200ns.
Z: 5V

As shown in Table 4.1, most of the FGT's loss is contributed by Q_1 (BJT) since Q_1 is the main power device. The predominant loss in Q_2 is due to switching, because Q_2 is subjected to a high voltage during the OFF state and to an initial current surge during turn-on. The conduction loss of Q_2 is much less than its switching loss, since Q_2's current during the conduction state is quite small. The major portion of Q_3's loss is conduction loss because Q_3 carries the total load current during conduction. The switching loss of Q_3 is much smaller than the conduction loss, not only because Q_3 switches quickly, but also because Q_3 is subjected to a low voltage during the OFF state. The zener diode loss in this example is not significant for two reasons. First, the FGT conducts only 20A. Second, the storage time of Q_1 is quite short (200ns). If Q_1 has a long storage time while switching a high current, the zener diode loss may exceed the power rating of the zener diode. This might happen in the case of a high voltage, high current IGTO, as shown in Table 4.2.

Table 4.2 lists the power loss distributions for an IGTO operated at 1000V and 100A, under operating frequencies of 2KHz, 10KHz, 20KHz and 40KHz. The power loss for a Triple Darlington transistor is also included for comparison

TABLE 4.2

Power Loss for 1000V/100A IGTO and Triple Darlington

Loss (W)	Q_1	Q_2	Q_3	Z	IGTO	Triple Darlington
@2KHz						
Conduction	97.6	0.3	100.0	0.0	197.9	148.2
Switching	50.5	2.0	0.4	2.1	55.0	599.4
Total	148.1	2.3	100.4	2.1	252.9	747.6
@10KHz						
Conduction	90.1	0.5	99.6	0.0	190.2	
Switching	252.5	9.9	2.0	10.5	274.9	
Total	342.6	10.4	101.6	10.5	465.1	
@20KHz						
Conduction	80.9	0.7	99.2	0.0	180.8	
Switching	505.4	20.0	4.0	21.0	550.4	
Total	586.3	20.7	103.2	21.0	731.2	
@40KHz						
Conduction	61.5	1.1	98.4	0.0	161.0	
Switching	1009.8	40.0	8.0	42.0	1099.8	
Total	1071.3	41.1	106.4	42.0	1260.8	

Assumptions:
Constant inductive load current, 50% duty-cycle.
IGTO: Q_1: $V_{GK(ON)}$=1V, t_s=1us, t_f=0.2us, t_t=1.5us
steady-state gate current=0.5A,
initial tailing current amplitude=10A.
Q_2: $V_{CE(ON)}$=1V, t_r=t_f=200ns,
initial current pulse=10A, pusle width=5us.
Q_3: R_{ON}=0.02 ohm, t_r=t_f=200ns.
Z: 10V
Triple Darlington: $V_{CE(ON)}$=3V, t_s=15us, t_r=t_f=3us.

in Table 4.2. Because a Triple Darlington transistor normally has a long storage time (typically 15 μs) and is not suitable for high frequency applications, its loss is calculated for 2KHz operation only. As shown in Table 4.2, Q_1 contributes most of the IGTO's loss. As explained for the FGT, Q_2 has a higher switching loss than conduction loss, while the conduction loss of Q_3 is higher than its switching loss. The zener diode loss is determined by the storage time of Q_1, the zener breakdown voltage, the load current and the operating frequency. Because Q_1 (GTO) has a long storage time (1μs) and conducts a large current (100A), the zener diode loss may exceed the power rating of the zener diode during high current and high frequency operation, as evidenced in Table 4.2.

Because of the unique IGTO configuration, the switching speed is much improved and switching loss significantly reduced. Compared to a Triple Darlington transistor with the same voltage and current ratings, the total loss of the IGTO operated at 20KHz is still less than that of a Triple Darlington transistor operated at 2KHz, under similar working conditions.

4.5 HALF-BRIDGE INVERTER EXPERIMENTAL RESULTS

Two half-bridge inverters were built and tested using IGTOs as switching devices. One operates up to 4A peak current at 100KHz, using an Amperex GTO (BTV58-600R, 400V continuous off-state voltage, 10A average on-state current) as Q_1 of the IGTO. The other inverter operates up to 30A peak current at 40KHz using a Westinghouse GTO (GDM11210, 960VDC. off-state voltage, 20A average on-state current) as Q_1 of the IGTO. No snubber circuit is used.

The purpose of such tests was to demonstrate that the IGTOs work properly in a commonly used inverter circuit of multiple switches, and to show the improvement of the IGTO over a single GTO in practice. The switching waveforms are shown in Figures 4.7 to 4.10.

Figure 4.7 shows the anode-source voltage, as well as the current waveform of the IGTO and the anti-parallel diode. The expanded waveforms are shown in Figure 4.8. As can be seen from Figure 4.8, the storage time is less than 100 ns and the current fall time is about 100 ns.

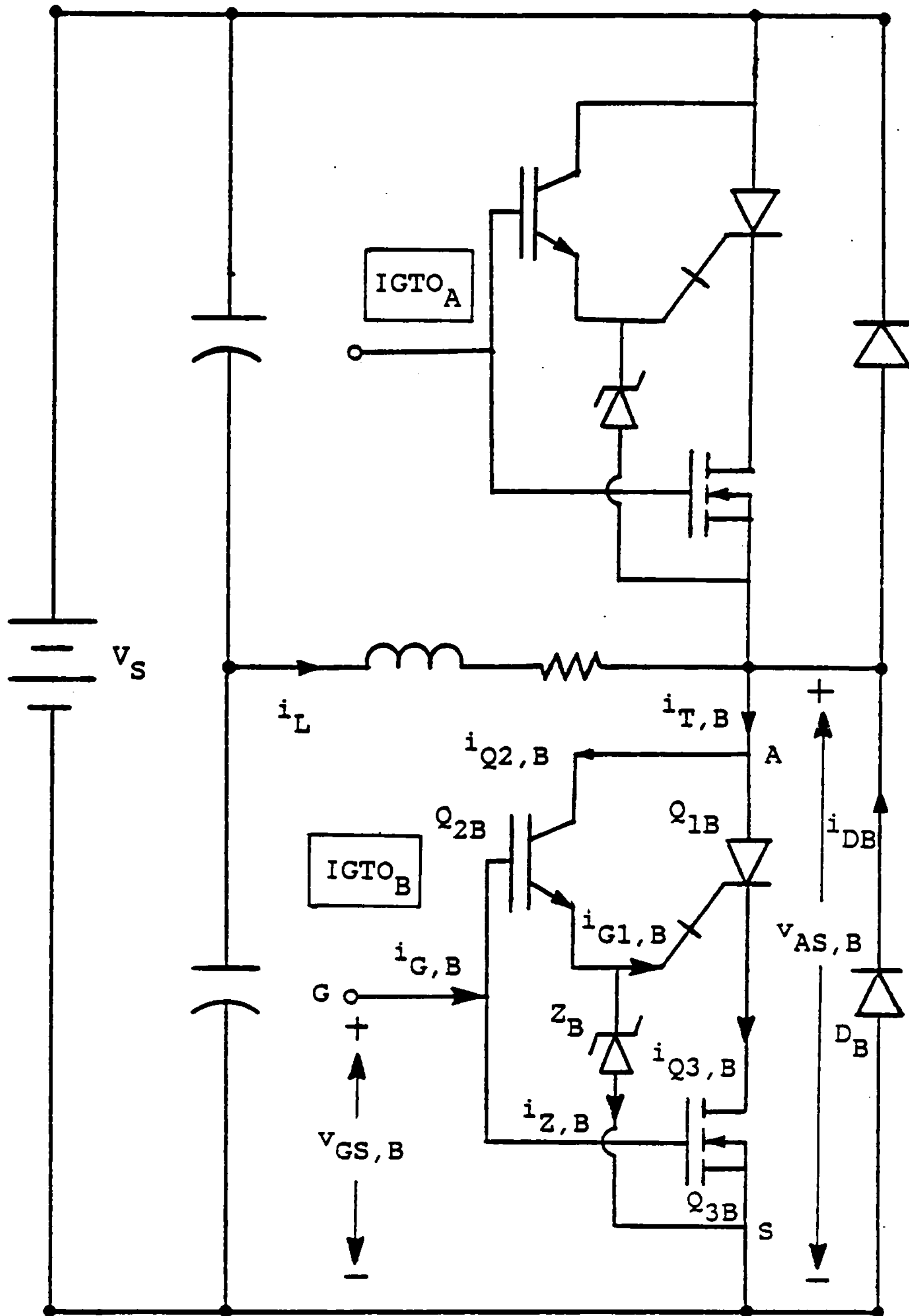
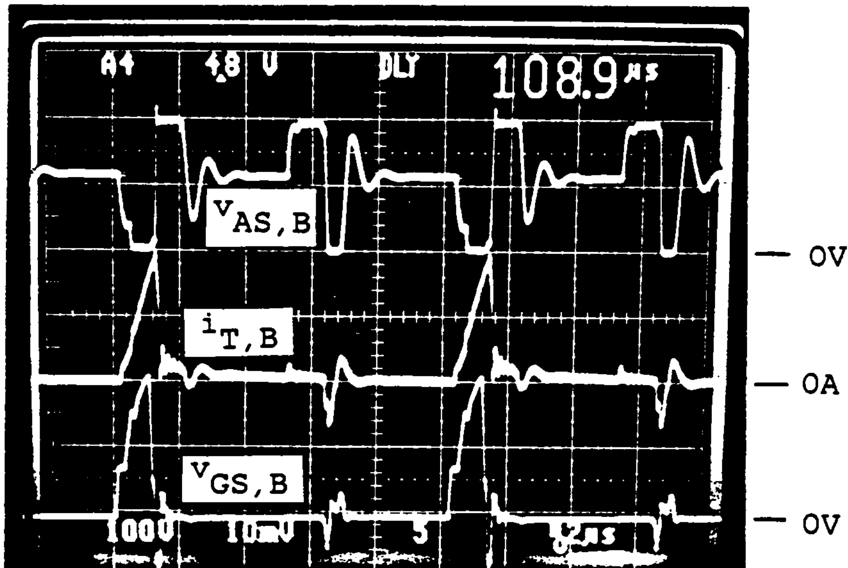
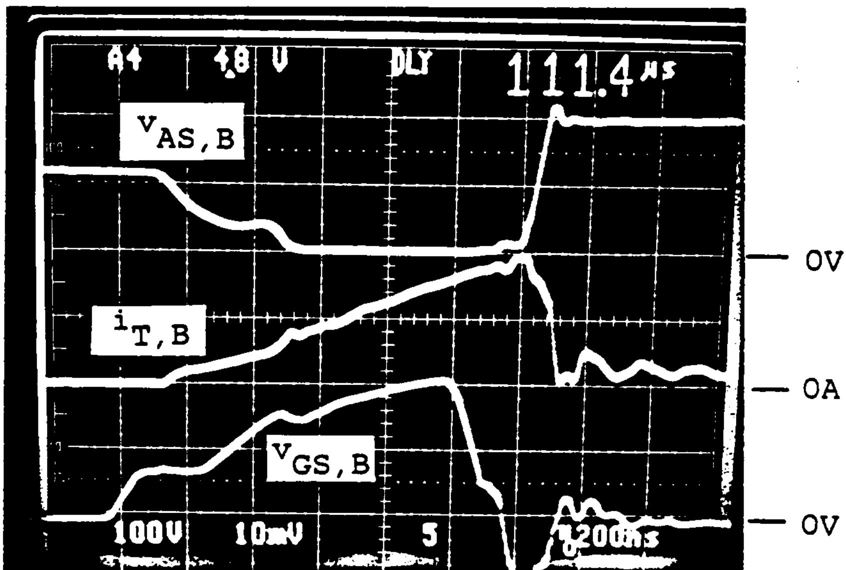


Figure 4.6: A Half-bridge Inverter Employing IGTOs as Switching Devices



$v_{AS,B}$:	100 Volts/Division
$i_{T,B}+i_{DB}$:	2 Amperes/Division
$v_{GS,B}$:	5 Volts/Division
time:	2 Microseconds/Division
Q_1:	Amperex BTV58-600R
Q_2:	General Electric D94FQ4
Q_3:	Siemens BUZ15
Z:	TCG 5243A
D:	Motorola MR826

Figure 4.7: Switching Waveforms of a 100KHz/4A Half-bridge Inverter

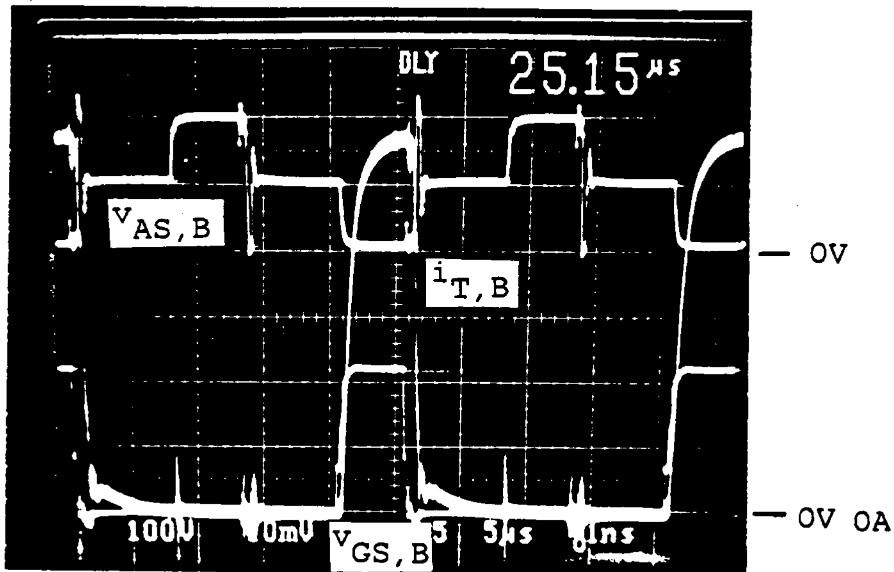


$v_{AS,B}$:	100 Volts/Division
$i_{T,B}$:	2 Amperes/Division
$v_{GS,B}$:	5 Volts/Division
time:	200 Nanoseconds/Division
Q_1:	Amperex BTV58-600R
Q_2:	General Electric D94FQ4
Q_3:	Siemens BUZ15
Z:	TCG 5243A
D:	Motorola MR826

Figure 4.8: Expanded Switching Waveforms of a 100KHz/4A Half-bridge Inverter

The switching waveforms for the half-bridge inverter using high current IGTOs are shown in Figures 4.9 and 4.10. As shown in Figure 4.10, the IGTO storage time is about 800 ns, the fall time is about 200 ns and the tailing time is about 1.5 μs, when switched at 30A.

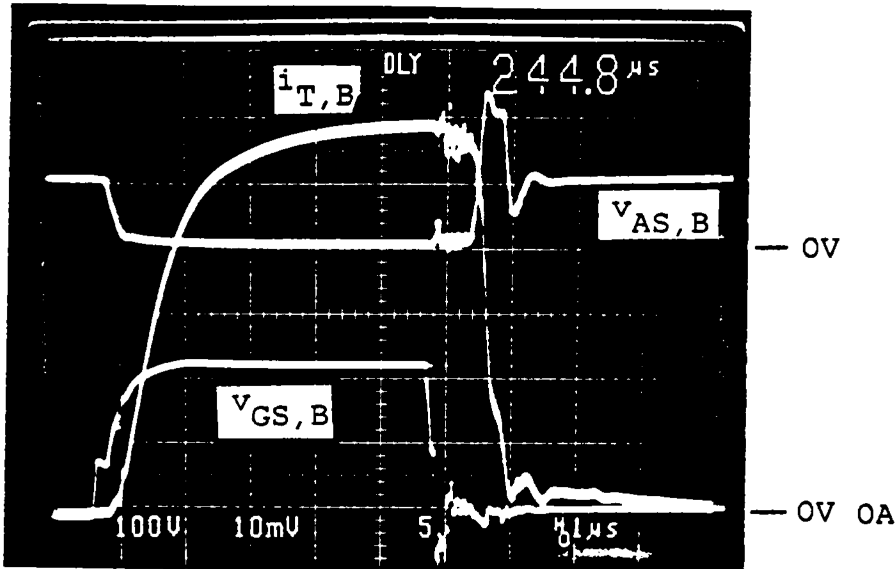
The tests demonstrate that IGTOs operate properly in an inverter circuit. There is no abnormality observed in the waveforms. Because of the improved switching time associated with the IGTO, the frequency capability is much enhanced. As previously shown in Chapter III, the GTO switching time is highly dependent on the turn-off gain. It is normally recommended the GTO be operated at a frequency less than 5 KHz. Using the IGTO approach, however, the operating frequency is enhanced by an order of magnitude.



$v_{AS,B}$: 100 Volts/Division
$i_{T,B}$: 5 Amperes/Division
$v_{GS,B}$: 5 Volts/Division
time: 5 Microseconds/Division

Q_1: Westinghouse GDM11210
Q_2: RCA RCM10N40
Q_3: Siemens BUZ15
Z: TCG 5243A
D: Motorola MR826

Figure 4.9: Switching Waveforms of a 40KHz/30A Half-bridge Inverter



$v_{AS,B}$:	100 Volts/Division
$i_{T,B}$:	5 Amperes/Division
$v_{GS,B}$:	5 Volts/Division
time:	1 Microseconds/Division

Q_1:	Westinghouse GDM11210
Q_2:	RCA RCM10N40
Q_3:	Siemens BUZ15
Z:	TCG 5243A
D:	Motorola MR826

Figure 4.10: Expanded Switching Waveforms of a 40KHz/30A Half-bridge Inverter

4.6 PROJECTION OF DEVICE CAPABILITIES AND LIMITATIONS

4.6.1 Voltage Limitation

The voltage capability of the FGT and the IGTO is limited by the ratings of Q_1 and Q_2. Table 4.3 shows the voltage ratings of the devices currently available and those predicted in the future.

The voltage rating of the FGT is limited by Q_2 (MOSFET). MOSFETs having breakdown voltage ratings of 1000V are commercially available, but the voltage rating is not likely to increase because the chip area requirement of the MOSFET has already been stretched. Even though the voltage limitation of the FGT is 1000V, the optimal voltage rating is about 500V.

For the IGTO, the voltage rating is set by the IGT (Q_2). IGTs having breakdown voltage ratings of 500V are available commercially, but higher voltage IGTs will soon be introduced. An experimental 1200V IGT has been reported. Although the IGT is projected to reach 1200V and 100A [4.13], devices with higher than 1200V ratings are economically feasible if the current rating is lowered. In the case of an IGTO, the steady state current rating of Q_2

TABLE 4.3

Voltage Ratings of Various Power Devices

Device	Currently Available	Projected Limitation
BJT	1500V (BV_{CBO})	1500V
MOSFET	1000V	1000V
FGT	1000V	1000V
GTO	2500V	2500V
IGT	500V	2000V
IGTO	500V	2000V

(IGT) can be small, therefore, the IGT used in an IGTO can be a low current high voltage device.

4.6.2 Current Limitation

The current rating of either the FGT or the IGTO is limited by two factors. One is the current rating of the Q_3. The otherlimitation is the parasitic inductances associated with the wires between the emitter of Q_1 and the drain of Q_3, and between the base of Q_1 and the cathode of the zener diode. The highest current rating of low voltage MOSFETs commercially available is 200A in a single package. A higher current MOSFET can be obtained by paralleling several MOSFETs. However, parasitic inductance prevents the current rating from going higher.

4.6.3 Frequency Limitation

The limitation on the operating frequency is primarily placed by the following considerations.

4.6.3.1 Storage Time of Q1

For both the FGT and the IGTO, the storage time of Q_2 is nearly zero. Therefore, the storage time of Q_1 is to be considered.

4.6.3.2 Tailing Time of the GTO

Although the storage time and fall time of the GTO is greatly reduced by the IGTO configuration, the tailing time still exists. The tailing time could be reduced by further reducing the carriers' life time at the expense of the forward voltage drop.

4.6.3.3 Latching of the IGT

As mentioned in Section 3.2, the IGT may latch during turn-off if a large current is rapidly switched. For the sake of reliable turn-off of the IGTO, the conduction period has to be long enough for the IGT current to taper off before turn-off is initiated. Figure 4.11 shows the Q_2 current waveform using a slow turn-off IGT as Q_2. The pulse width is 10 μs with no latching problem encountered. If the pulse width is reduced, the possibility of latching is increased, as shown in Figure 4.12. As can be seen from Figure 4.12, the Q_2 current at turn-off increases for a 4 μs

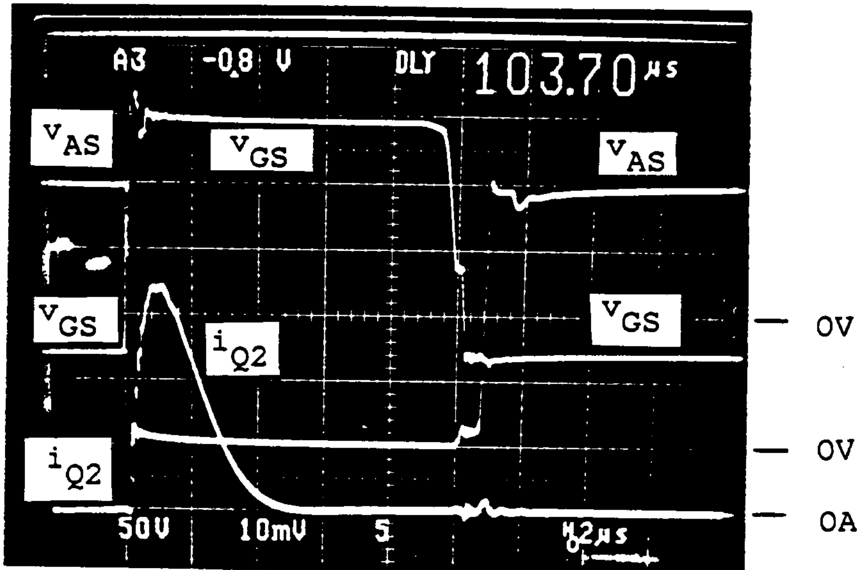
pulse. This situation can be improved if a fast IGT is used for Q_2. In Figure 4.13, the IGT has a faster turn-off which does not latch for a 4 μs pulse width. In this work, the IGTO has been tested up to 25 KHz (at 250V and 75A without a snubber circuit) with a 5 μs conduction time, as shown in Figures 4.14 and 4.15.

4.6.3.4 Power Dissipation of the Zener

A zener diode is able to withstand very high pulsed power, depending on the duty-cycle and the pulse width [Ref. 4.14]. For high-current high-frequency applications, however, the power dissipation on the zener diode Z may exceed its steady-state power rating. A P-channel IGT can be used to replace the zener diode, as described in Section 3.9.

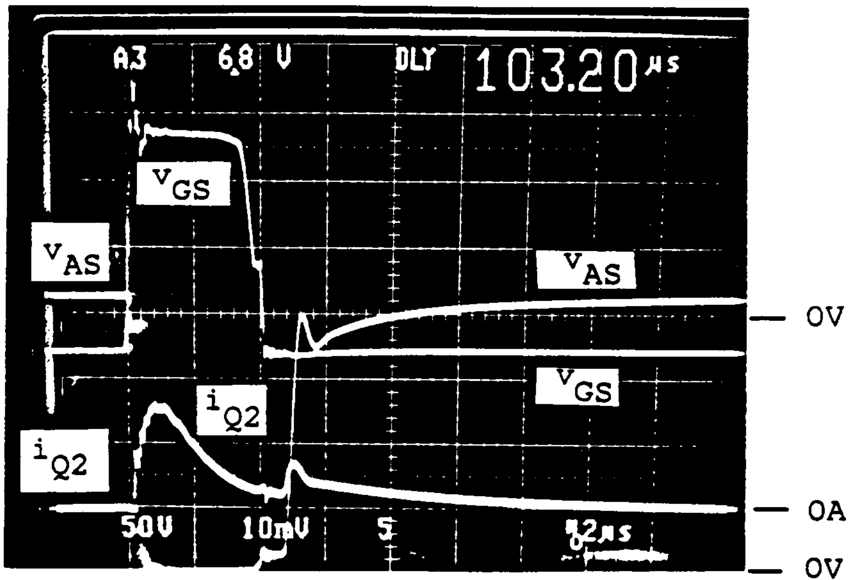
4.6.4 Effects of Parasitic Inductances

The proper operation of an FGT or an IGTO is affected by parasitic inductances. Figure 4.16 shows the parasitic inductance, L_3, associated with Q_3, and L_Z associated with the zener diode. Switching waveforms associated with Q_1 and Q_3 in the presence of L_3 and L_Z are depicted in Figure 4.17.



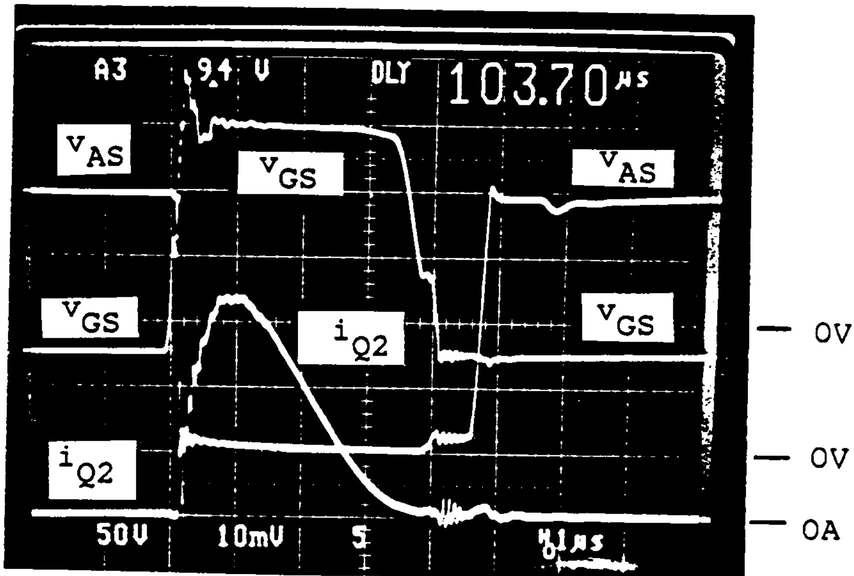
v_{GS}:	5 Volts/Division
v_{AS}:	50 Volts/Division
i_{Q2}:	1 Ampere/Division
time:	2 Microseconds/Division
Q_1:	Westinghouse GDM11210
Q_2:	General Electric D94FQ4
Q_3:	Siemens BUZ15
Z:	TCG 5125A

Figure 4.11: Current Waveform of a Slow Q2 for a Long Pulse



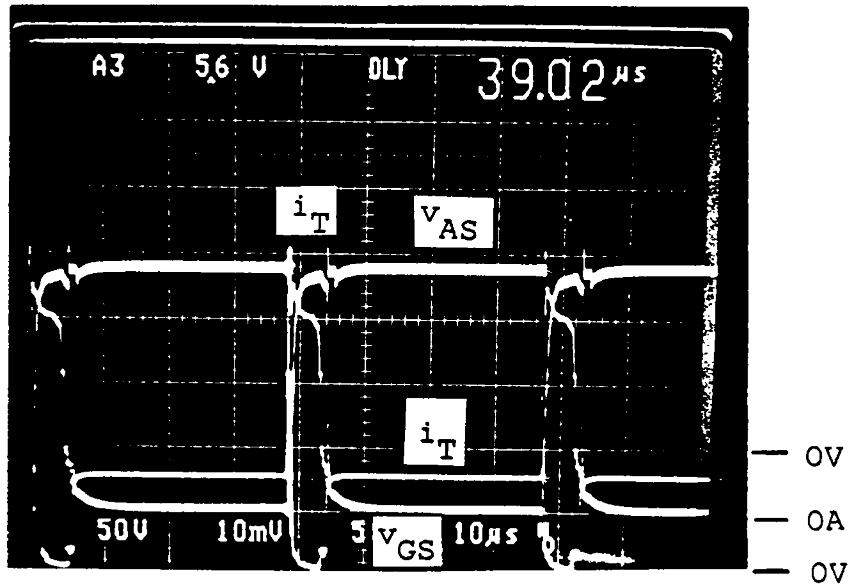
v_{GS}:	5 Volts/Division
v_{AS}:	50 Volts/Division
i_{Q2}:	2 Amperes/Division
time:	2 Microseconds/Division
Q_1:	Westinghouse GDM11210
Q_2:	General Electric D94FQ4
Q_3:	Siemens BUZ15
Z:	TCG 5125A

Figure 4.12: Current Waveform of a Slow Q2 for a Short Pulse



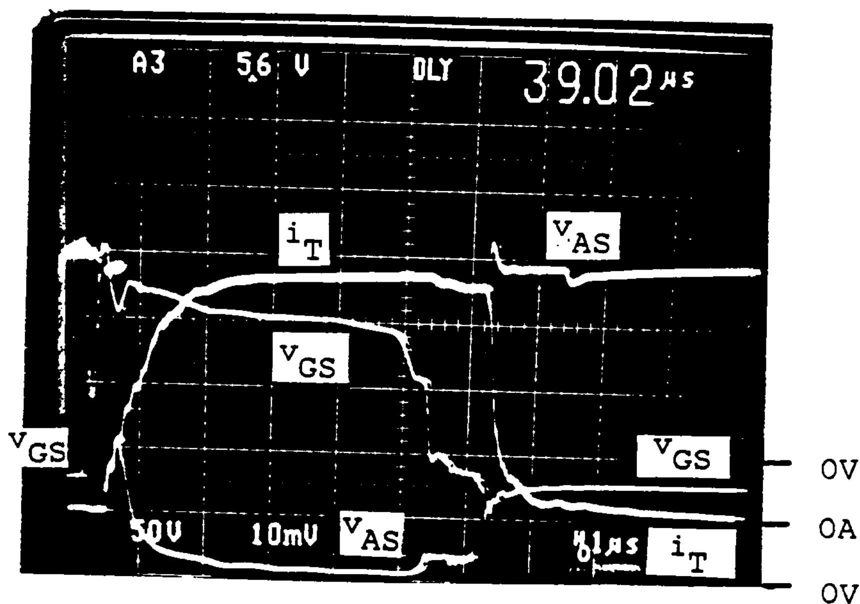
v_{GS}:	5 Volts/Division
v_{AS}:	50 Volts/Division
i_{Q2}:	1 Ampere/Division
time:	1 Microsecond/Division
Q_1:	Westinghouse GDM11210
Q_2:	RCA RCM10N40
Q_3:	Siemens BUZ15
Z:	TCG 5125A

Figure 4.13: Current Waveform of a Fast Q2 for a Short Pulse



v_{GS}:	5 Volts/Division
v_{AS}:	50 Volts/Division
i_T:	20 Amperes/Division
time:	10 Microseconds/Division
Q_1:	Westinghouse GDM11210
Q_2:	RCA RCM10N40
Q_3:	Siemens BUZ15
Z:	TCG 5125A

Figure 4.14: IGTO Switching Waveforms at 250V/75A/25KHz



v_G:	10 Volts/Division
v_{AS}:	50 Volts/Division
i_T:	20 Amperes/Division
time:	1 Microsecond/Division
Q_1:	Westinghouse GDM11210
Q_2:	RCA RCM10N40
Q_3:	Siemens BUZ15
Z:	TCG 5125A

Figure 4.15: Expanded IGTO Switching Waveforms at 250V/75A/25KHz

The analysis of the parasitic inductance effect is given below for different periods of time.

• During Q_3 current fall time, $0<t<t_{Q3f}$. During this period of time, the drain current of Q_3, i_{Q3}, is decreasing and the reverse base current of Q_1 is increasing. The drain voltage of Q_3, v_{Q3}, has an overshoot as shown in Figure 4.17. The base voltage of Q_1, v_B, equals the sum of the zener clamping voltage, V_Z, and the induced voltage across L_Z. Since the base-emitter junction of Q_1 is still forward biased, v_{BE} is about 1V. The overshoot of v_{Q3} is determined by the switching speed of Q_3, magnitude of i_{Q3} and parasitic inductance, L_3. The governing equations are given below.

$$\begin{aligned} L_3\, i_{Q3} &= \int \Delta v\, dt = \text{shaded area of } v_{Q3} \text{ waveform} \\ &= \int (v_{Q3} - v_E)\, dt \\ &= \int (v_{Q3} - v_B + 1)\, dt \\ &= \int (v_{Q3} - v_Z - v_{LZ} + 1)\, dt \end{aligned}$$

Approximating $v_{Q3}(t)$ by a constant voltage, V_{Q3}, and rearranging the above equation, the drain voltage of Q_3 can be expressed by

$$V_{Q3} = (L_3\, i_{Q3} / t_{Q3f}) + V_Z + V_{LZ} - 1$$

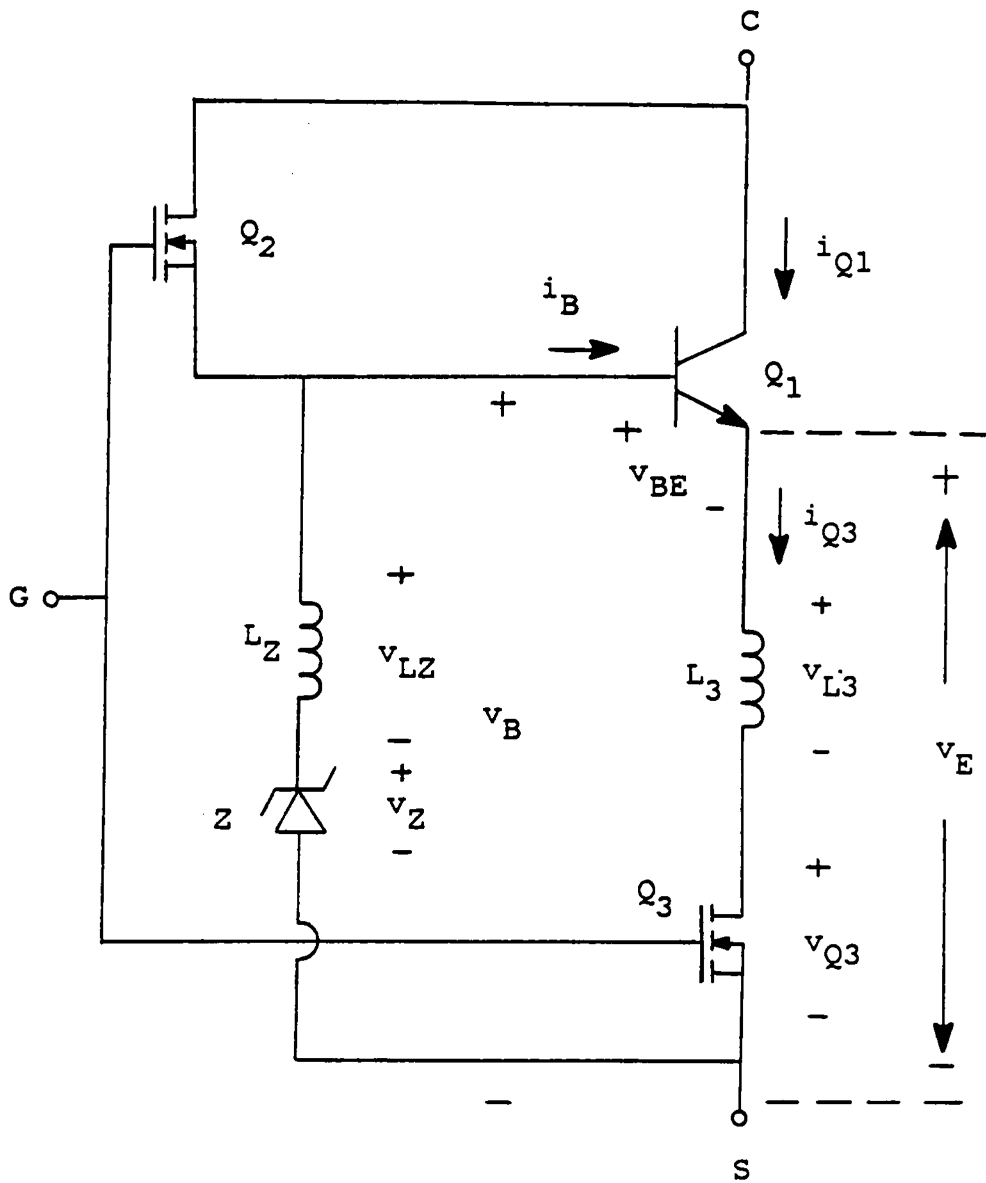


Figure 4.16: Parasitic Inductances Associated with Q3 and Z

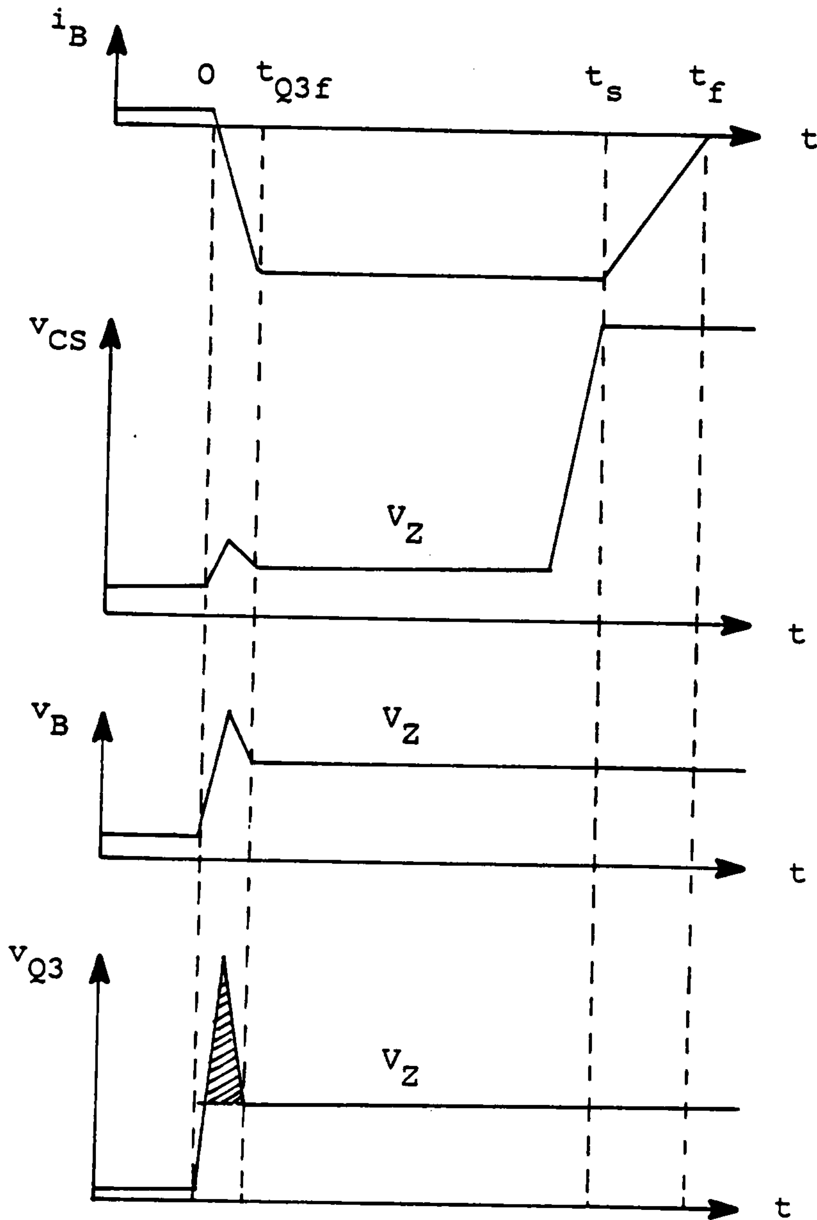


Figure 4.17: Q1 and Q3 Switching Waveforms in the Presence of Parasitic Inductances

If t_{Q3f} = 100ns, i_{Q3} = 100A, V_Z = 10V, $L_3 = L_Z$ = 20 nH, then v_{Q3} = 49V.

• During the FGT storage time, $t_{Q3f}<t<t_s$. The reverse base current of Q_1 equals the collector current of Q_1, and can be considered fairly constant during this period of time. The voltage across L_3 or L_Z is essentially zero, thus L_3 and L_Z have no effect during this period, and v_{Q3} is equal to v_E which is clamped by the zener diode voltage, V_Z.

• During the FGT fall time, $t_s<t<t_f$. The collector current as well as the reverse base current of Q_1 is decreasing during this period of time. The decreasing reverse base current induces a negative voltage across L_Z, i.e. $v_{LZ} < 0$. Since $v_B = V_Z + v_{LZ}$, the base voltage of Q_1 is pulled down, as are the emitter voltage of Q_1 and the drain voltage of Q_3.

• After the FGT fall time, $t_f<t$. The drain voltage of Q_3 is shielded by Q_1, as explained in Section 2.6. The parasitic inductances have no effect during this period.

Four conclusions can be drawn from this analysis:

A. The drain voltage of Q_3 during turn-off may exceed its voltage rating. If a high voltage MOSFET is required for Q_3, then the FGT loses its advantage of small chip area because of the high voltage Q_3. Therefore, the parasitic inductances place the ultimate limitation on the switchable current for the FGT and the IGTO.

B. During t_{Q3f} when the drain current of Q_3 is decreasing and the reverse base current of Q_1 is increasing, the current crowding phenomenon may occur. However, RBSB will not happen because v_{CE} of Q_1 does not increase until the FGT storage time is over; however, the emitter current of Q_1 has already been transferred to the base by then. As mentioned in Section 2.1, a high electric field is required with a high current density to induce RBSB. The only possibility for RBSB to occur in an FGT is when the storage time is extremely short. This implies that, even in the FGT configuration, an ultra-fast Q_1 may suffer from RBSB if a parasitic oscillation keeps the emitter current from becoming zero when the FGT voltage starts to increase.

C. Breakdown of the base-emitter junction is unlikely because the inductance of the base-emitter junction is

small, even though the parasitic lead inductance between the emitter of Q_1 and the drain of Q_3 might be large. Under conventional reverse-bias turn-off, the BJT's emitter-base junction and the GTO's gate-cathode junction occasionally suffer from avalanche breakdown. This may cause concerns about the long-term reliability of the devices. This can be avoided in the FGT and the IGTO configurations.

D. Due to the presence of L_Z, the source voltage of Q_2 (i.e., the base voltage of Q_1) will increase during the fall time of Q_3. The gate-source voltage rating of Q_2 might be exceeded during this period. Therefore, the minimization of the parasitic inductances is deemed necessary.

Chapter V

DEVICE INTEGRATION

The concepts of the FGT and the IGTO described in Chapters II and III, respectively, were conceived from the consideration of device applications. The configurations proposed best utilize capabilities of individual devices to achieve power switches with capabilities not available before.

However, the necessity of using several discrete devices to form a power switch imposes limitations on it from the technical and economical viewpoints. As mentioned earlier, parasitic inductances of the connecting wires put ultimate constraint on the technical performance of the proposed switches. To be accepted by users, the monolithic integration of these devices deems necessary.

In this chapter, conceptual monolithic structures for both the FGT and the IGTO are presented. Undesirable parasitic transistors or thyristors are inherent in the proposed structures, but methods of suppressing the effects of these parasitic elements are proposed. The structures shown in this chapter are meant to be only a conceptual

realization. The practical fabrication of the proposed switches, nevertheless, is beyond the scope of this dissertation.

Two structures are proposed for both the FGT and the IGTO. One is the partial integration in which only Q_1, Q_2 and Q_3 are integrated, so a discrete zener diode, Z, must be used. The other is the full integration of Q_1, Q_2, Q_3 and Z, using a P-channel MOSFET or a P-channel IGT to replace the zener diode.

5.1 DEVICE STRUCTURE FOR PARTIALLY INTEGRATED FGT

Figure 5.1 illustrates the cross-sectional structure of a partially integrated FGT. As shown in Figure 5.1, Q_1 is an N^+-N^--P-N^+ bipolar power transistor, Q_2 is a vertical power MOSFET, and Q_3 is a lateral power MOSFET. The zener diode, Z, is not integrated on the same chip. To have an FGT in a single package, a discrete zener chip is added to the partially integrated chip.

The lightly doped N^- region serves as the extended collector region of Q_1 and the extended drain region of Q_2. The P-well serves as the base of Q_1, and part of it is to be

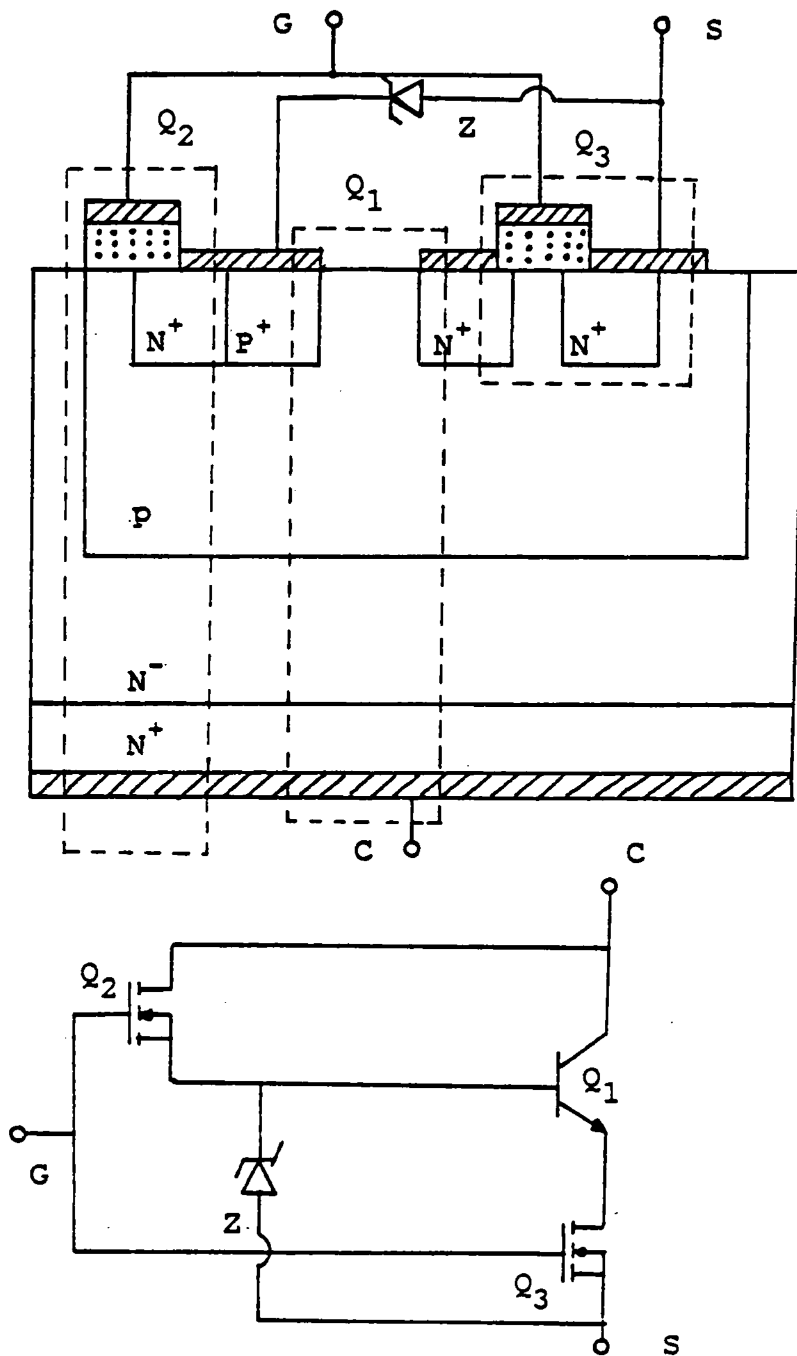


Figure 5.1: Device Structure for a Partially Integrated FGT

inverted by the gate of Q_2 and Q_3 during conduction. The N^+ regions in the P-well form the emitter region of Q_1, the source region of Q_2, and the drain and source regions of Q_3.

The collector metalization allows the silicon chip to be soldered to the header, and good electrical contact to be made to the silicon. The heavily doped N^+ substrate provides the silicon chip with the mechanical rigidity and a buffer between the N^- epitaxial layer and the metal contact.

5.2 DEVICE OPERATION FOR PARTIALLY INTEGRATED FGT

5.2.1 Turn-on

Figure 5.2 shows the current path for the FGT during turn-on. When a positive gate voltage is applied, the P region underneath the gate electrode of Q_2 is inverted to N type, so that a channel is created to allow the Q_2 current to flow. The Q_2 current functions as the turn-on base current of Q_1. Because a channel is also created underneath the gate electrode of Q_3 by the positive gate voltage, Q_3 is also turned on and the FGT is turned on.

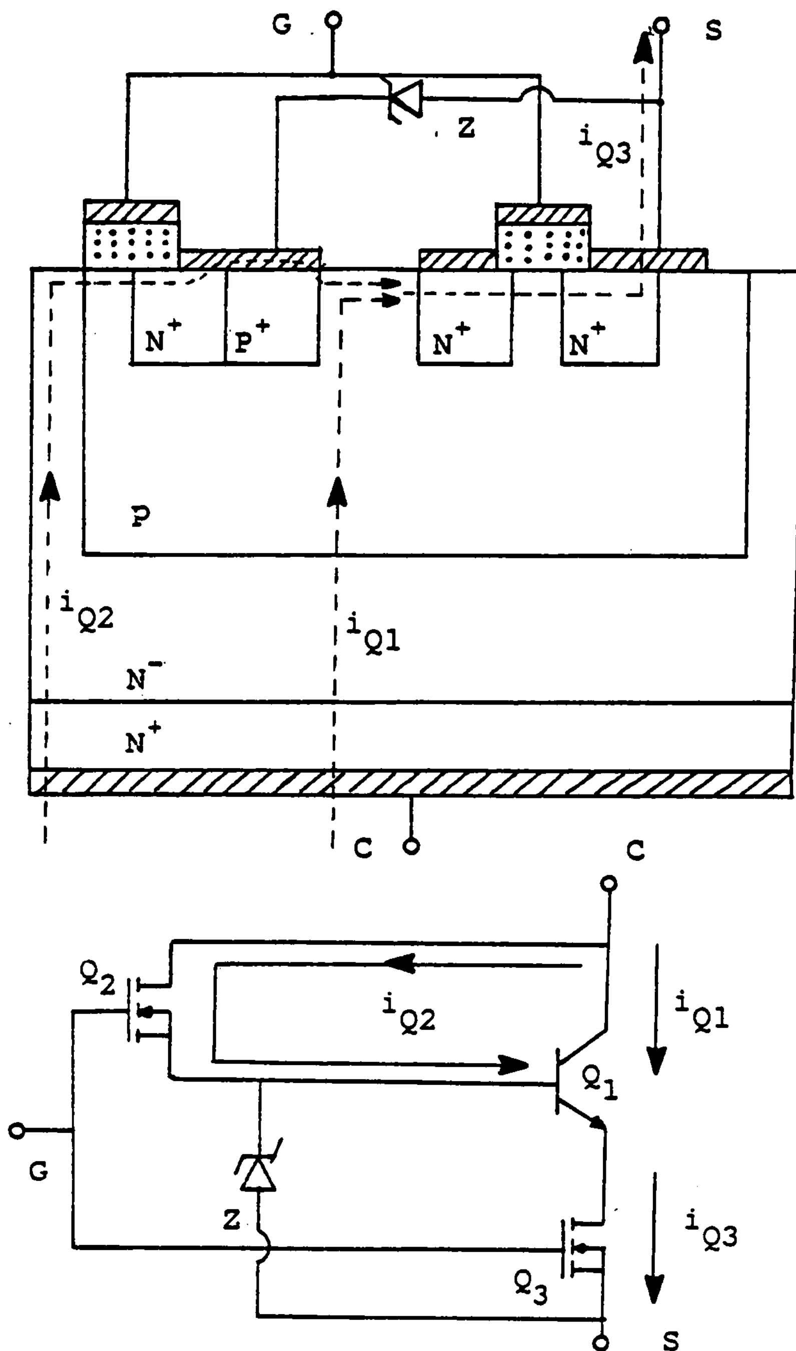


Figure 5.2: Current Path of a Partially Integrated FGT During Turn-on

5.2.2 Conduction

During conduction, the N^- epitaxial layer of Q_1 is fully conductivity-modulated by excess carriers, so the conduction voltage drop is reduced.

5.2.3 Turn-off

Figure 5.3 shows the current path of the FGT during turn-off. When the gate voltage is low, the channels of Q_2 and Q_3 are cut off. The collector current of Q_1, therefore, flows out of the Q_1 base terminal through Z to ground, resulting in emitter-open turn-off.

5.2.4 OFF State

Once the excess carriers are depleted, the P-N^- junction blocks the applied voltage, so Q_3 is not subjected to a high voltage in the OFF state. Because the N^- region is much more lightly doped than the P region, most of the voltage is dropped across the N^- region. The thickness and the doping density of the N^- region is determined by the voltage blocking requirement of the FGT.

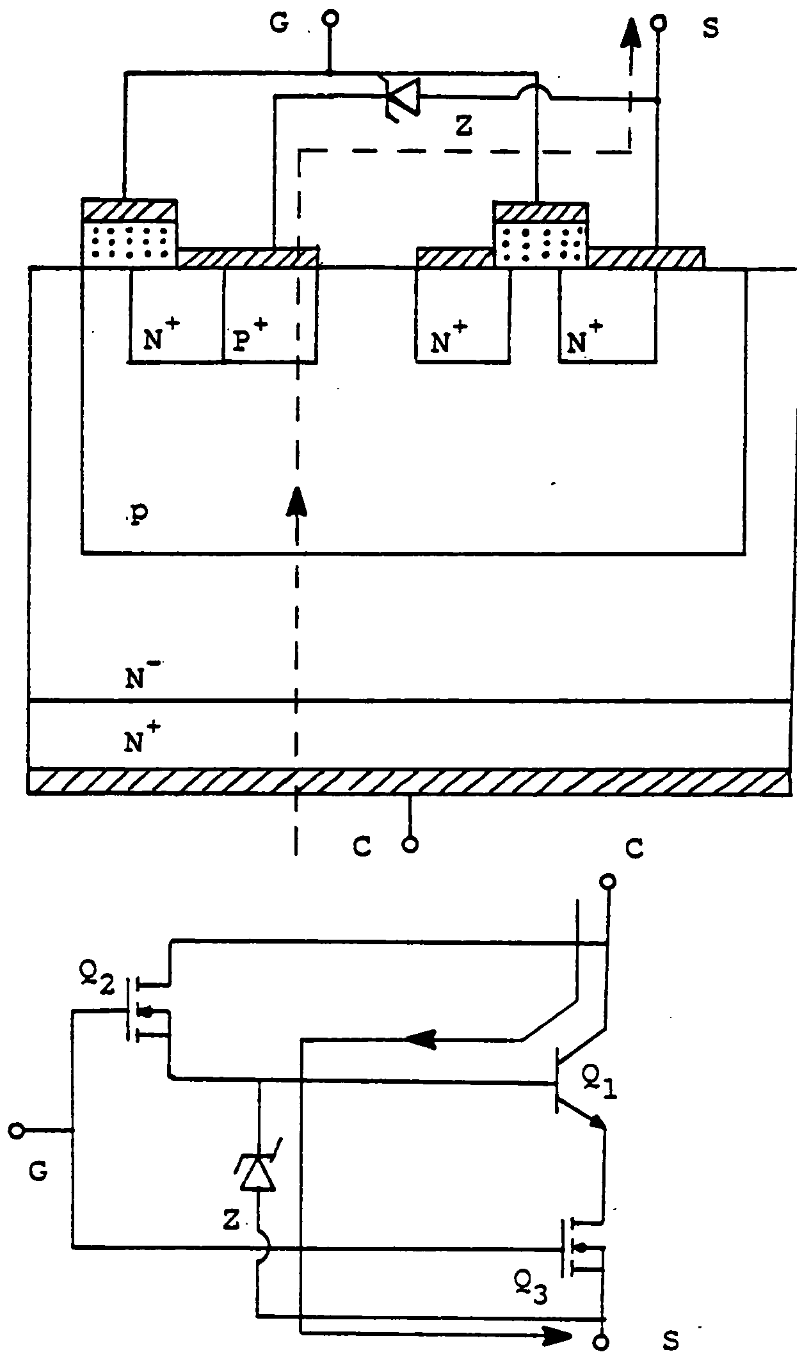


Figure 5.3: Current Path of a Partially Integrated FGT During Turn-off

5.2.5 Parasitic Components

Parasitic transistors and diodes may arise from the proposed FGT structure. Figure 5.4 shows parasitic transistors, Q_A, Q_B and Q_C, and parasitic diodes, D_A, D_B and D_C.

5.2.5.1 Parasitic NPN Transistors

As seen from Figure 5.4, the N^+ source of Q_3, the P-base of Q_1, the N^- epitaxial layer and the N^+ substrate form the emitter, base and collector of a parasitic bipolar transistor, Q_A. When a positive voltage is applied across the drain and the source of the FGT, a depletion region forms at the reverse biased junction between the N^- epitaxial layer and the P-base region. The width of the depletion region depends on the doping density on either side of the depleted junction and the applied voltage. If the rate of rise of the applied voltage (dv/dt) is high enough, the displacement current of the junction capacitance may activate the parasitic bipolar transistor, Q_A.

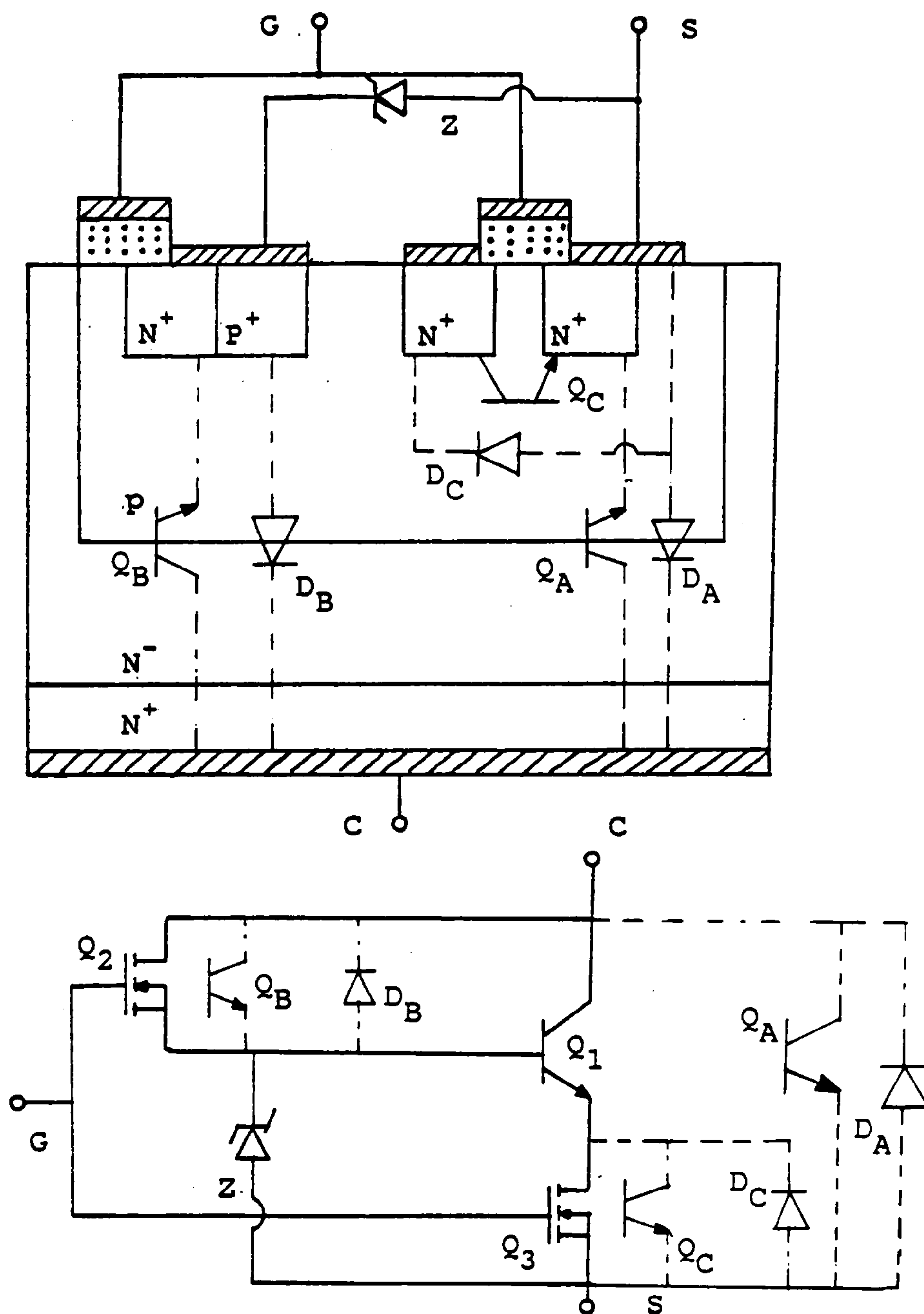


Figure 5.4: Parasitic Components in a Partially Integrated FGT

Q_B is formed across Q_2, and Q_C across Q_3. The undesirable parasitic transistor action of Q_A mentioned above also applies to Q_B and Q_C. These parasitic transistors must be suppressed to avoid malfunction of the FGT. A method of suppressing the effects of these parasitic transistors, using an "Emitter-short" technique, will be briefly discussed in Section 5.3.

5.2.5.2 Parasitic Diodes

Parasitic diodes, D_A, D_B and D_C, shown in Figure 5.4 are created in the process of using the emitter-short to suppress the effects of the parasitic transistors. A better understanding of how these diodes are created will be provided in the next section. These diodes, however, do not interfere with the normal function of the FGT but provide the device with reverse conduction ability.

5.3 SUPPRESSION OF THE PARASITIC NPN TRANSISTORS

5.3.1 Principle of Emitter-short

The basic principle of suppressing the parasitic bipolar transistor using the emitter-short can be explained with the aid of Figure 5.5 [5.1], in which a shunting resistor, R, is connected between the base and the emitter of an NPN transistor.

The common-base current gain of the NPN transistor, α_{npn}, is given by

$$\alpha_{npn}=I_C/I_E$$

where I_C and I_E are the collector and the emitter currents, respectively. With the shunting resistor R, the common-base current gain of this "composite" transistor is given by

$$\alpha=I_C/(I_E+I_R)=\alpha_{npn}/[1+(I_R/I_E)] < \alpha_{npn}$$

where I_R is the current through R. The common-emitter current gain of the NPN transistor, in the absence of the shunting resistor R, can be expressed by

$$\beta_{npn}=\alpha_{npn}/(1-\alpha_{npn})$$

With the shunting resistor, the common-emitter current gain of this "composite" transistor is

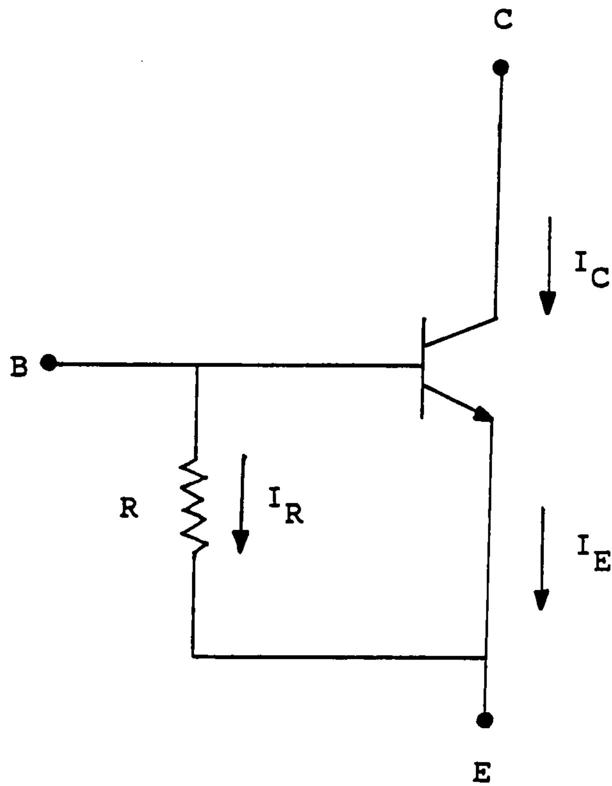


Figure 5.5: An NPN Transistor with a Shunting Resistor

$$\beta=\alpha/(1-\alpha)=\alpha_{npn}/[1-\alpha_{npn}+(I_R/I_E)] < \beta_{npn}$$

From the above equations, it is clear that the emitter shunting resistor effectively reduces the current gains of the parasitic transistor. However, it is effective at low current but does not drastically alter the current gain at the normal current level, as shown in Figure 5.6 [5.1].

Since all the parasitic transistors described above are open-base transistors, the transistor action can only be activated by a dv/dt displacement current or a leakage current at elevated temperatures. With the shorting resistor, these prospective activating currents will be diverted, and the parasitic transistor action can be suppressed without affecting the normal current gain required for non-parasitic transistors.

5.3.2 Forming the Shunting Resistor

The shunting resistor, R, can be formed by overlapping metalization on base-emitter junctions of parasitic transistors. The resistance value is determined by the sheet resistivity of the P-base and the lateral dimension of the overlapping. The emitter-short method is widely adopted

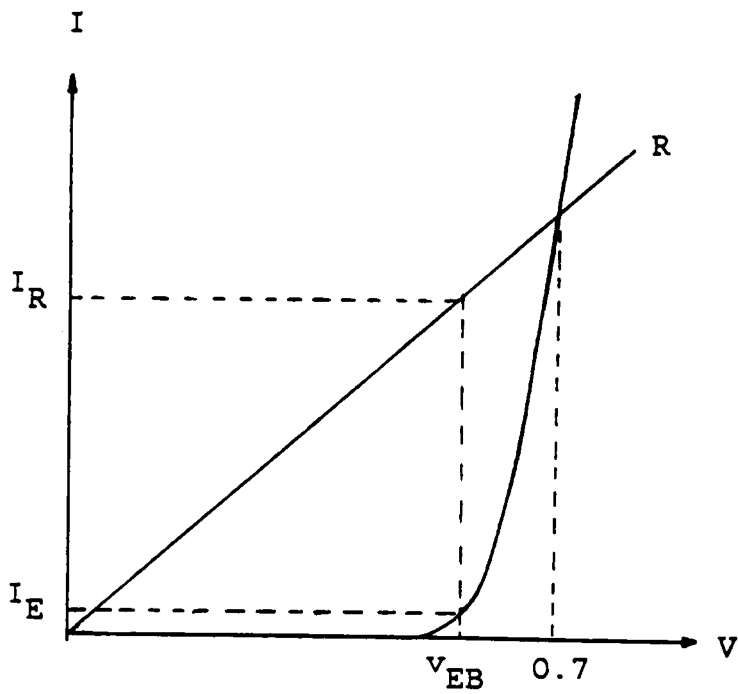


Figure 5.6: Effect of Junction Voltage on Current with Emitter-short

by power MOSFET manufacturers to suppress the parasitic bipolar transistor in a vertical power MOSFET [5.2]. Figure 5.7 shows that the base of a parasitic bipolar transistor is common to the channel of the power MOSFET, the emitter is common to the N^+ source, and the collector is common to the N^- epitaxial region. In order to suppress this parasitic bipolar transistor, the N^+ source and the P-well are electrically bonded. Hence, the displacement current will be diverted through the short. The forward biasing of the base-emitter junction of the parasitic bipolar transistor is very unlikely.

5.3.3 Effect of Emitter-short

In addition to suppressing the effects of the parasitic transistors, the shunting resistor offers other advantages. Although the shorting is done at the expense of the channel packing density, it increases the device operating voltage from the open-base transistor breakdown value to the avalanche breakdown voltage, BV_{CER}, of the junction between the P-base and N^- region [5.3]. Moreover, the shorting also broadens the safe operating area (SOA) since RBSB due to the

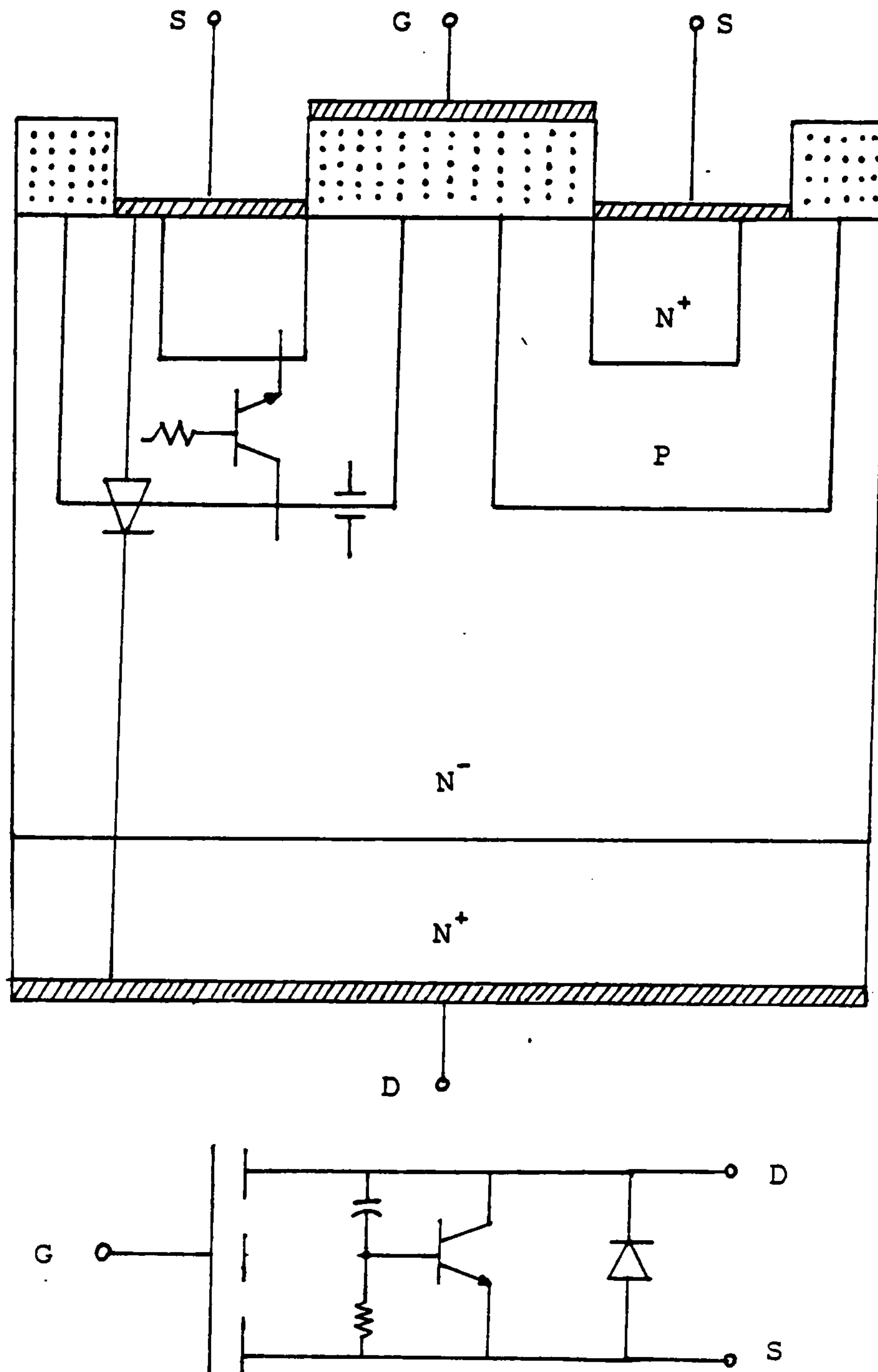


Figure 5.7: Suppressing Parasitic Bipolar Transistor in a Power MOSFET by Emitter-short

presence of the parasitic bipolar transistors Q_A and Q_B is unlikely to occur.

5.3.4 Creation of Anti-parallel Diodes

Because of using the emitter-short to form a shunting resistor, three anti-parallel diodes, D_A, D_B and D_C, are created as shown in Figure 5.4. D_A is formed across the collector and the source of the FGT, D_B between the drain and the source of Q_2, and D_C across Q_3. As mentioned earlier, these diodes pose no threat to the normal operation of the FGT. In fact, in some applications it is an advantage to have an anti-parallel diode.

5.4 FULL INTEGRATION OF FGT

A fully integrated FGT can be achieved by replacing the zener diode with a P-channel MOSFET or a P-channel IGT. Figure 5.8 shows a fully integrated FGT using a P-channel MOSFET Q_4 to replace Z. As described in Section 2.8, this concept has been experimentally demonstrated by using discrete devices.

The portions of the diagram corresponding to Q_1, Q_2 and Q_3 are the same as described in Section 5.3. The P-channel MOSFET Q_4 is obtained by doping a P^+ region in the P-well as its source and an additional P^+-well as its drain. The sources of Q_2 and Q_4 are bonded together. The drain of Q_4 is tied to the source of Q_3.

5.5 DEVICE OPERATION FOR A FULLY INTEGRATED FGT

5.5.1 Turn-on

Figure 5.9 shows the current path for the fully integrated FGT during turn-on. When a positive gate voltage is applied, the P region underneath the gate electrode is inverted to N type, so that a channel is created to allow the Q_2 current to flow. The drain current of Q_2 functions

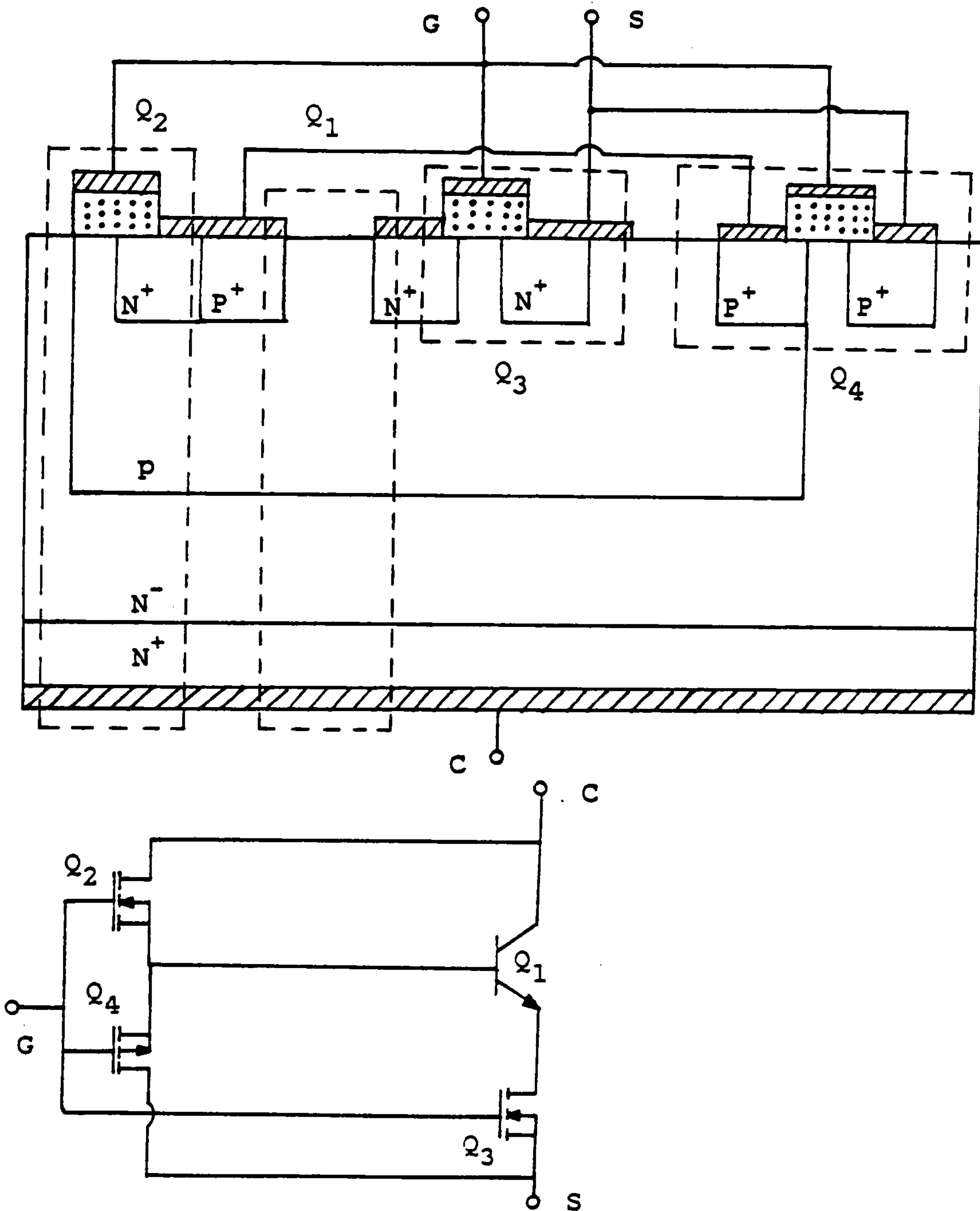


Figure 5.8: Device Structure for a Fully Integrated FGT

as the base current of Q_1 to turn on Q_1. Because a channel is also created underneath the gate electrode of Q_3 by a positive gate voltage, Q_3 is also turned on and the FGT is turned on. Q_4 is cut off during this period because of the positive gate voltage.

5.5.2 Conduction

During conduction, the N^- epitaxial layer of Q_1 is fully conductivity-modulated by excess carriers to reduce the conduction voltage drop, similar to the case of a partially integrated FGT. Q_4 is not turned on unless the gate voltage is negative.

5.5.3 Turn-off

Figure 5.10 shows the current path of a fully integrated FGT during turn-off. When the gate voltage is low, the channels of both Q_2 and Q_3 are opened. But a P type inversion layer is created underneath the gate electrode of Q_4 by the negative gate voltage, so Q_4 is turned on. The collector current of Q_1, therefore, flows out of the Q_1 base terminal through Q_4 to ground. Thus Q_4 plays the same role as the zener diode does.

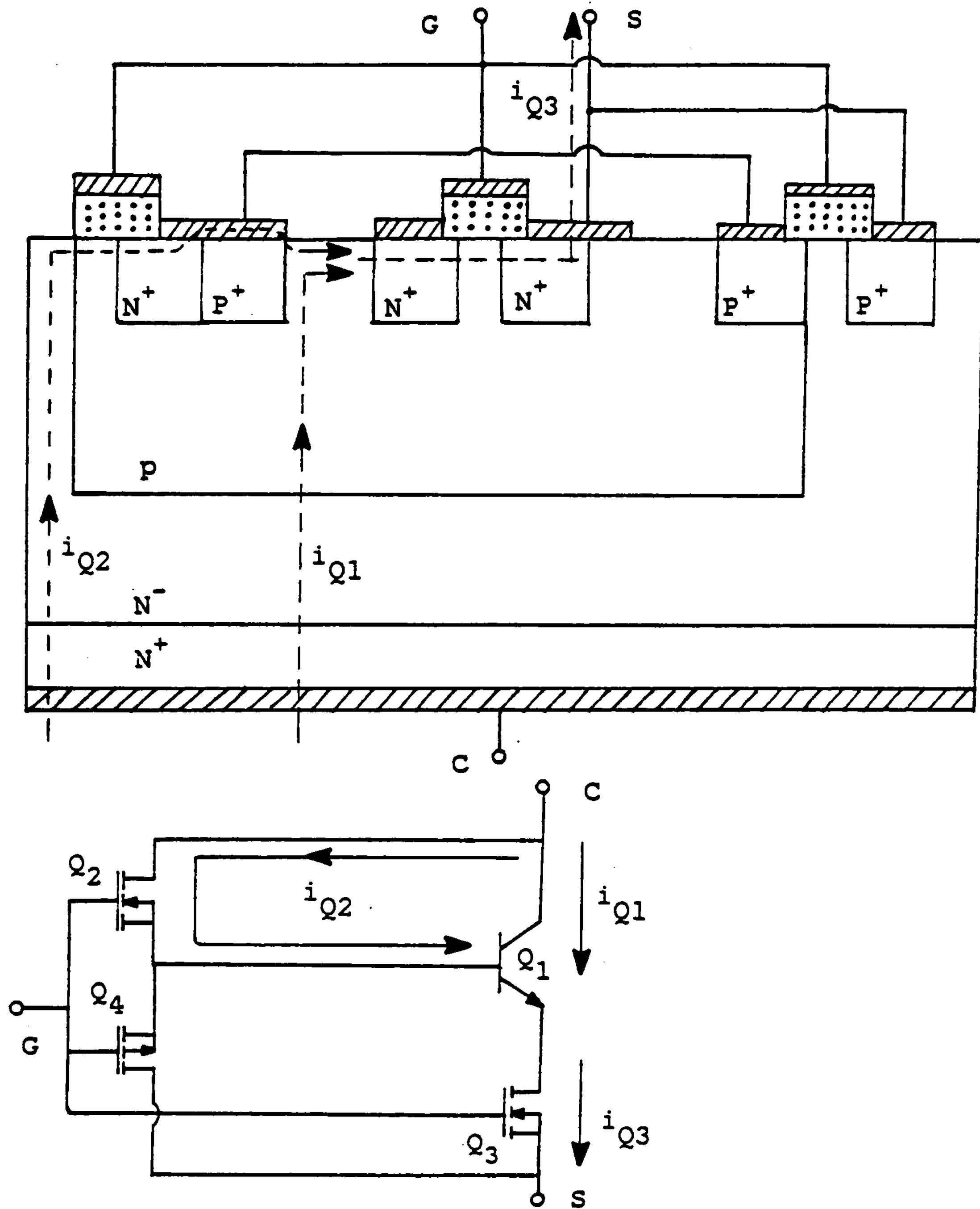


Figure 5.9: Current Path of a Fully Integrated FGT During Turn-on

5.5.4 Parasitic Components

Because the source of Q_4 is tied to that of Q_2, and the drain of Q_4 is connected to the source of Q_3 to replace the zener diode, no parasitic element is formed in addition to those existing in a partially integrated FGT.

5.6 COMMENTS ON INTEGRATED FGT

5.6.1 Fabrication Steps

To fabricate a partially integrated FGT, a lightly doped N^- region is epitaxially grown on a N^+ substrate (Step 1), followed by diffusing a P-well into the N^- epitaxial region (Step 2). N^+ regions are subsequently diffused into the P-well (Step 3). A P^+ region can be incorporated in the P-well, either by diffusion or by ion implantation (Step 4), to reduce the metal-semiconductor contact potential between the Q_2 source metalization and the Q_1 base. Afterwards, the zener diode is hybridized in the same package (Step 5). For a fully integrated FGT, Step 1 to Step 4 are the same as for a partially integrated FGT, but the P^+ regions of Q_4 can be done simultaneously in Step 4.

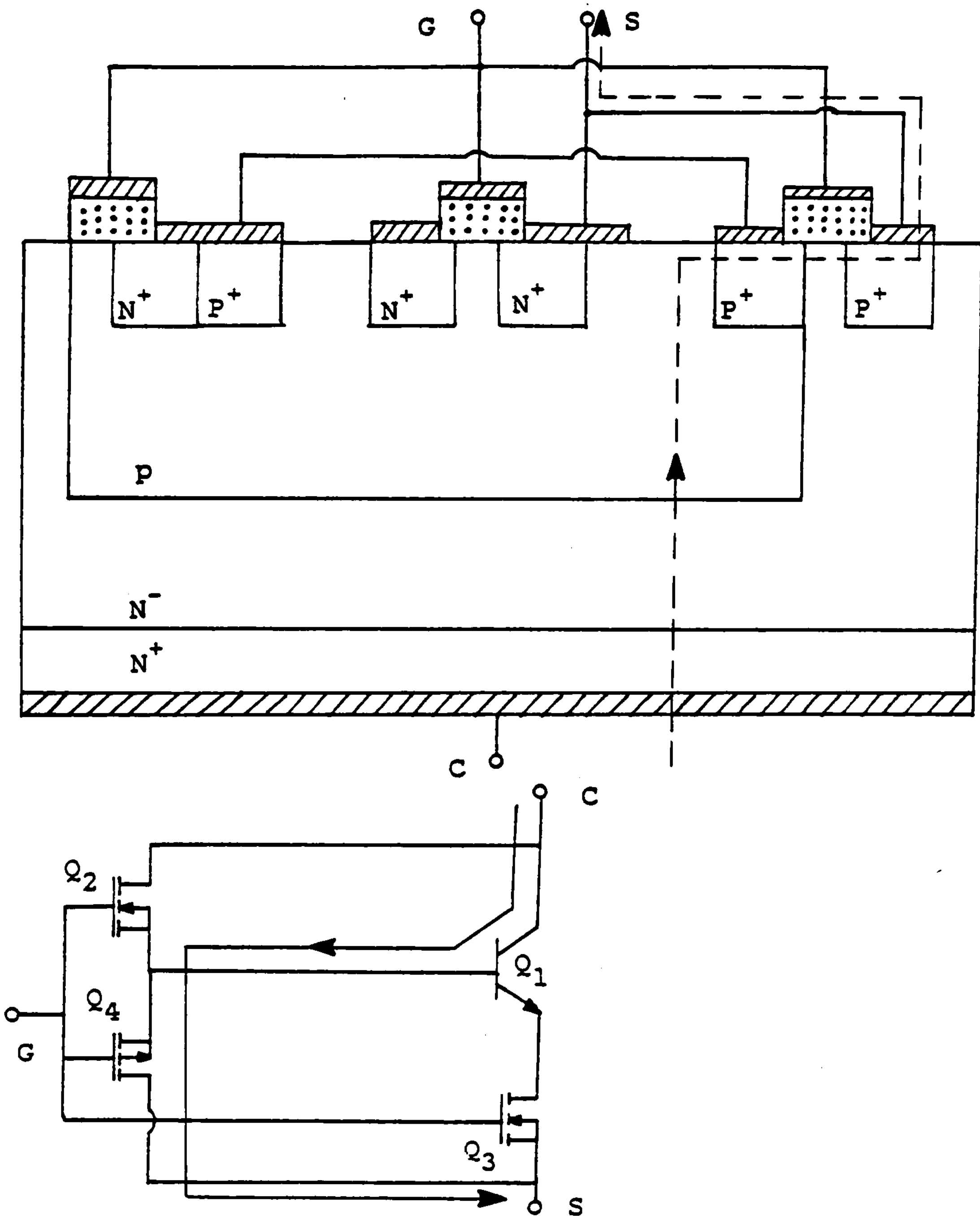


Figure 5.10: Current Path of a Fully Integrated FGT During Turn-off

5.6.2 Design of Q1

High voltage bipolar power transistors are conventionally fabricated with a triple-diffused process. One of the reasons for using the triple-diffused process is to increase the device reverse-bias turn-off ruggedness. Although RBSB occurs in epitaxial transistors as well as triple-diffused ones, an epitaxial transistor is normally more susceptible to RBSB because of an abrupt junction formed in the epitaxial process [5.4]. In the case of an FGT, however, Q_1 is turned off by emitter-open so RBSB can be avoided. Therefore, the selection of an epitaxial transistor for Q_1 not only gains a ruggedness characteristic, but also retains the advantages of epitaxial transistors, such as the better quality control, a higher voltage blocking capability for the same average N^- collector resistance (or a smaller conduction voltage drop for the same voltage blocking capability), etc.

5.6.3 Utilization of Chip Area

Q_1 and Q_2 are both vertical devices and have the same N^- region thickness, which is determined by the breakdown voltage requirement. Figure 5.11 shows the collector and the drain characteristics for Q_1 and Q_2 having the same N^- doping and thickness [5.5]. If Q_1 is turned off conventionally, it can only sustain BV_{CEO} instead of BV_{CBO}. Therefore, the voltage capability of Q_2 is not fully utilized.

In the case of an FGT, Q_1 is operated up to BV_{CBO}, so the voltage capability of both Q_1 and Q_2 are the same. The static blocking capability of the monolithic FGT, however, is now limited by BV_{CER} since shorting resistances are needed to suppress the parasitic components.

5.6.4 Lateral MOSFET Q3

Conventionally, a lateral power MOSFET requires large chip areas to reduce the conduction voltage drop. For the purpose of monolithic fabrication, a lateral Q_3 requires larger chip area than a vertical one in order to reduce the voltage drop across it during conduction.

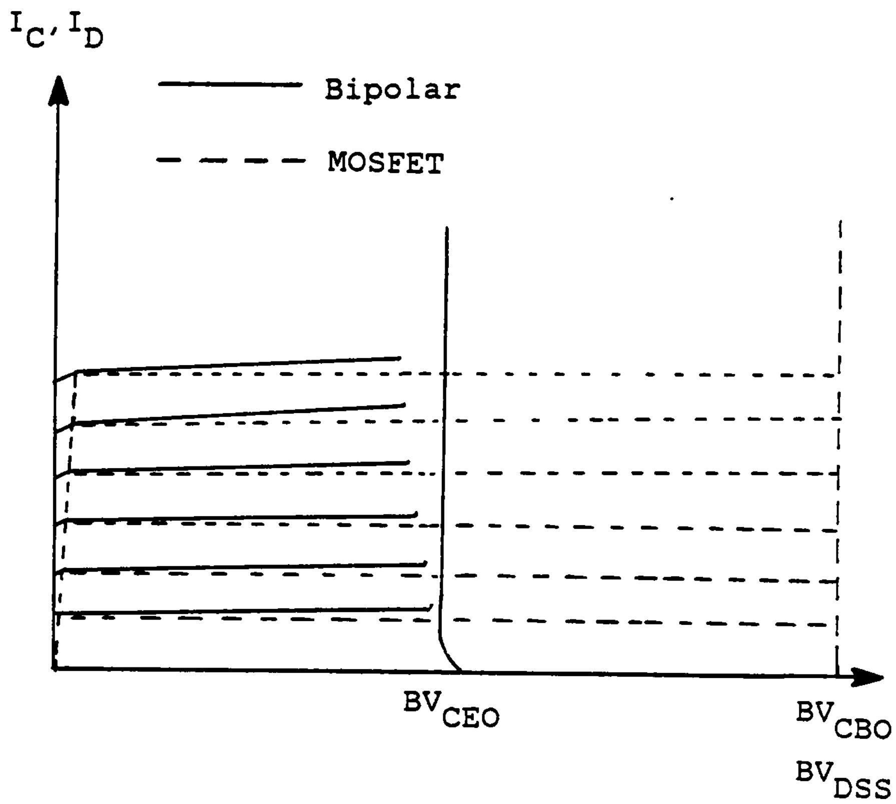


Figure 5.11: Collector and Drain Characteristics for Q1 and Q2 Having the Same Doping and Thickness of N-Region

Q_3, in Figure 5.1, is fabricated by doping two N^+ regions as its drain and source. Since the channel length of a low voltage MOSFET is inversely proportional to the transconductance as well as the ON-resistance [5.2], the lateral Q_3 may have a higher ON-resistance and a higher threshold voltage. One way to achieve a lower ON-resistance is to fabricate Q_3 using a double-diffused process, in which the P channel is determined by the difference in the diffusion constant of P and N material. A double diffused MOSFET offers a lower ON-resistance because of a shorter channel length. It also features a lower threshold voltage, since the P region under the gate electrode is more easily to be converted to an N type inversion layer.

Yet, an N^- substrate is needed on which a double-diffused short-channel MOSFET can be fabricated. An N^- region is not available in the P-well of the FGT, unless the dielectric isolation technique is used to allow a double-diffused MOSFET Q_3 to be formed inside the P-well. However, the dielectric isolation technique is an expensive approach which may not be economically attractive.

5.6.5 Partial Integration or Full integration

The device configuration of a fully integrated FGT differs from that of a partially integrated one in replacing the zener diode, Z, of the latter by a P-channel MOSFET Q_4 in the former. Full integration provides an advantage when considering fabrication. However, a P-channel MOSFET is associated with a larger conduction resistance, because the mobility of holes is three times that of electrons. The conduction voltage drop of Q_4 is high unless a larger chip area is used. Therefore, the power dissipation of Q_4 should be taken into account in designing a fully integrated FGT.

5.6.6 Reverse Conduction

Both the partially and the fully integrated FGT have an inherent reverse conducting capability. The reverse current can flow from the source of the FGT to the collector through the anti-parallel diode, D_A.

5.7 DEVICE STRUCTURE FOR PARTIALLY INTEGRATED IGTO

Figure 5.12 illustrates the cross-sectional structure of a partially integrated IGTO. Q_1 is an P^+-N^--P-N^+ GTO, Q_2 is a vertical IGT and Q_3 is a lateral power MOSFET. If a single package is required, a discrete zener chip needs to be added to the partially integrated chip.

The thickness and the doping density of the N^- region is determined by the breakdown voltage requirement of the IGTO. The P-well serves as the gate of Q_1, and part of it is to be inverted by the gates of Q_2 and Q_3 during conduction. The N^+ regions inside the P-well form the cathode of Q1, the source of Q_2, and the drain and source regions of Q_3. The heavily doped P^+ substrate serves as the anode of Q_1 and the collector of Q_2. The anode metalization allows the silicon chip to be soldered to the header, and good electrical contact to be made to the silicon

5.8 DEVICE OPERATION FOR PARTIALLY INTEGRATED IGTO

5.8.1 Turn-on

Figure 5.13 shows the current path for a partially integrated IGTO during turn-on. When a positive voltage is

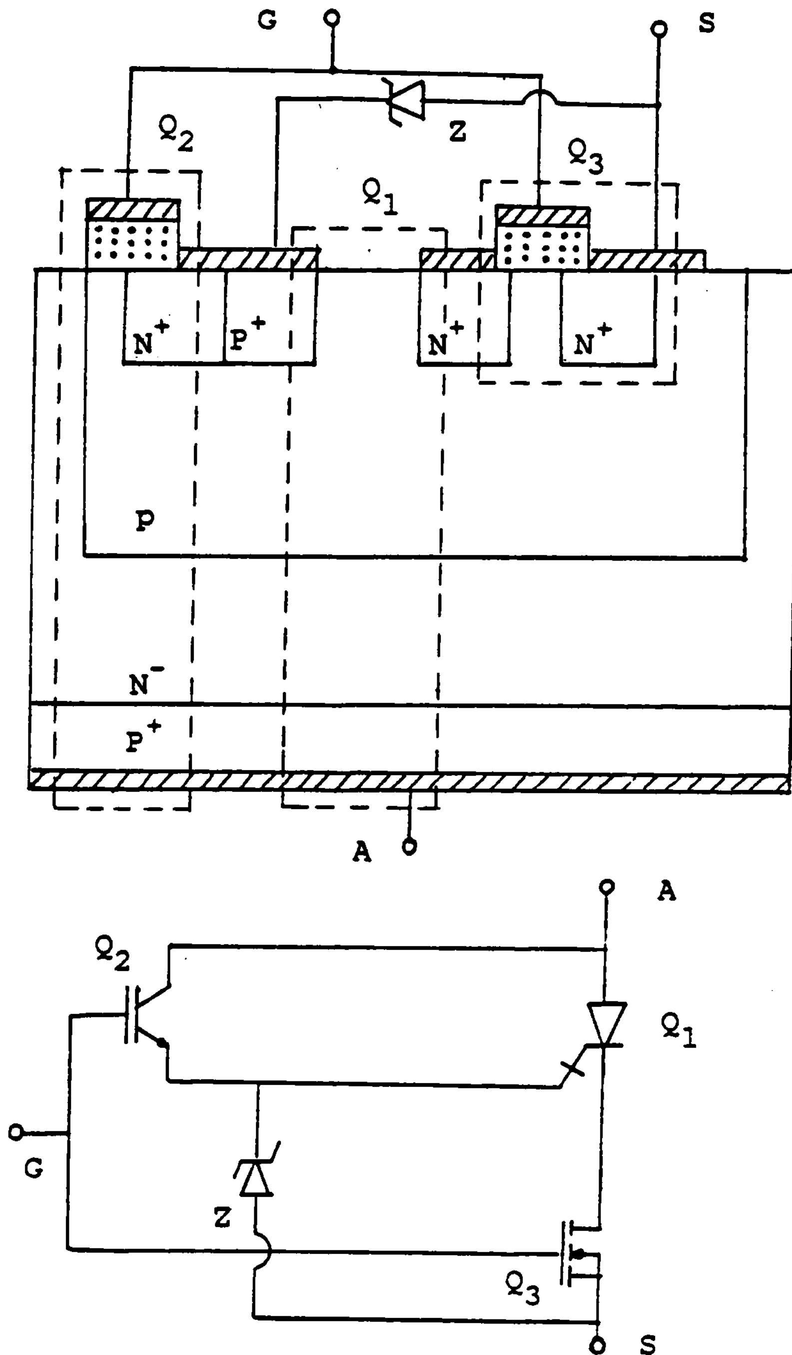


Figure 5.12: Device Structure for a Partially Integrated IGTO

applied to the gate of Q_2 and Q_3, the P region underneath the gate electrode is inverted to N type, so channels are created to allow the currents from Q_2 and Q_3 to flow. The drain current of Q_2 functions as the gate current of Q_1 to turn on Q_1. The IGTO is, therefore, turned on by a positive gate voltage.

5.8.2 Conduction

During conduction, the N^- epitaxial layer is fully conductivity-modulated by excess electrons and holes injected from the source and the anode, respectively. Once the GTO portion latches, the IGT current is reduced to a minimal value.

5.8.3 Turn-off

Figure 5.14 shows the current path of a partially integrated IGTO during turn-off. When the gate voltage is low, the channels of both Q_2 and Q_3 are opened. The anode current of Q_1, therefore, flows out of the gate of Q_1 through Z to ground, resulting in cathode-open turn-off.

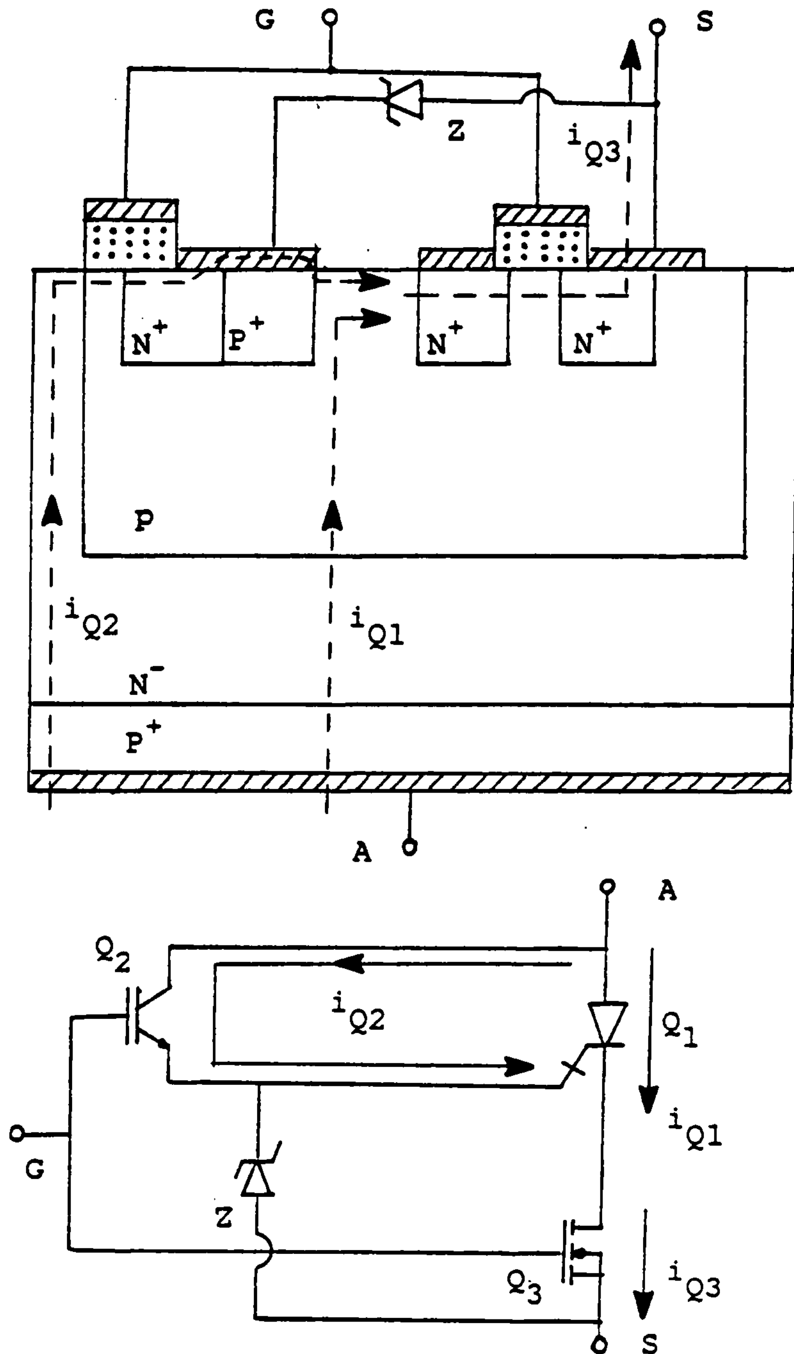


Figure 5.13: Current Path of a Partially Integrated IGTO During Turn-on

The remaining excess electrons and holes in the N^- region then recombine, giving rise to a tail in the anode current waveform.

5.8.4 OFF State

Once the excess carriers are depleted, the $P\text{-}N^-$ junction blocks the applied voltage so that Q_3 is not subjected to a high voltage in the OFF state. The thickness and doping density of the N^- region is determined by the voltage blocking requirement of the IGTO.

5.8.5 Parasitic Components

Parasitic thyristors, transistors and a diode may arise from the proposed IGTO structure, as shown in Figure 5.15 by dotted lines. These include two parasitic thyristors, Q_A and Q_B, a parasitic NPN transistor, Q_C, two parasitic PNP transistors, Q_D and Q_E, and a parasitic diode, D_A.

5.8.5.1 Parasitic Thyristors

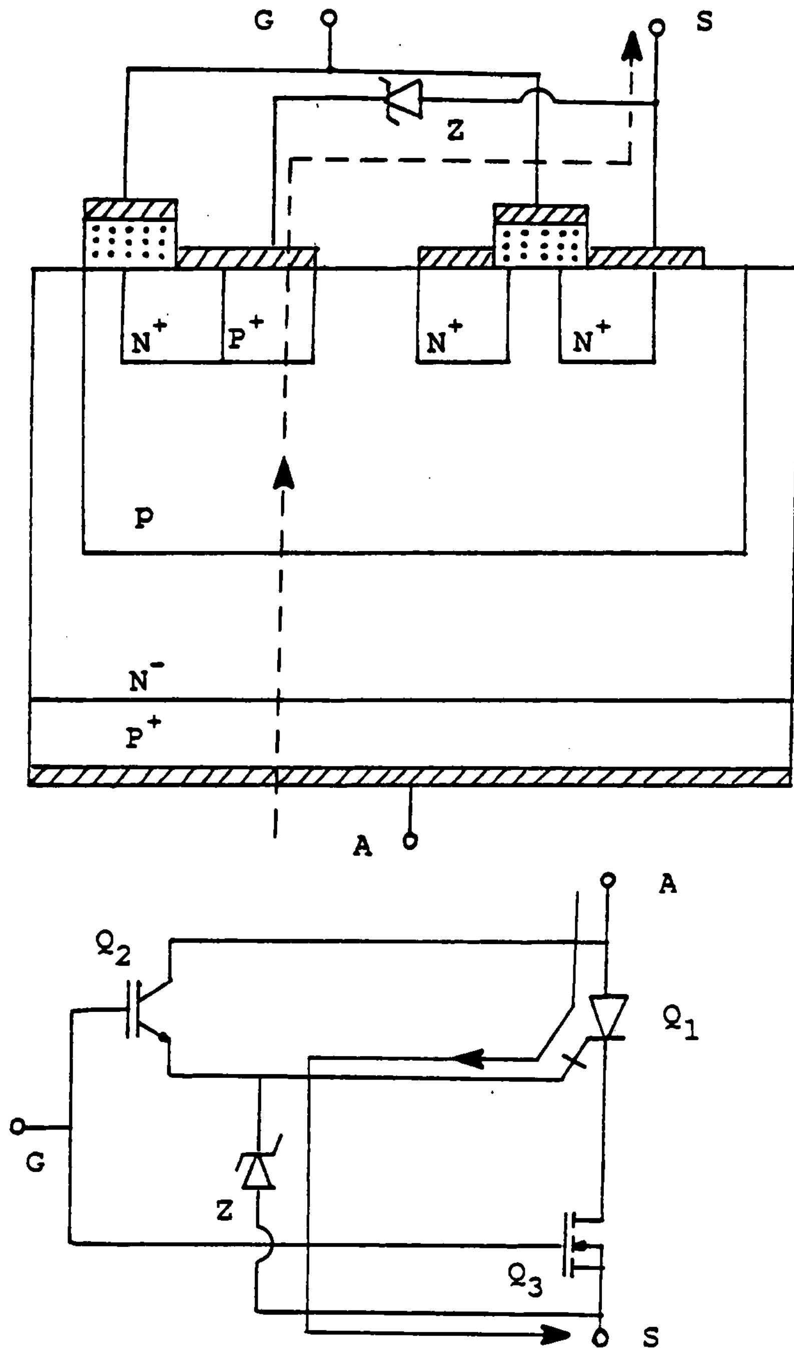


Figure 5.14: Current Path of a Partially Integrated IGTO During Turn-off

As shown in Figure 5.15, the N^+, P, N^- and P^+ regions form the parasitic thyristors Q_A and Q_B. Under a high dv/dt condition, the displacement current of the depletion region is injected into the P-well and functions like a gate current to Q_A and Q_B. The parasitic thyristor action, therefore, starts and Q_A and Q_B may latch. This thyristor action must be suppressed to insure the proper operation of the IGTO. A method of suppressing the effects of these parasitic thyristors is given in Section 5.9.

5.8.5.2 Parasitic NPN Transistor

A parasitic NPN transistor, Q_C, is formed across the drain and source of Q_3. This parasitic transistor can be suppressed by the emitter-short approach as described in Section 5.3.

5.8.5.3 Parasitic PNP Transistors

Parasitic PNP transistors, Q_D and Q_E, are created in the process of suppressing the parasitic thyristor action. Details of the creation of these two PNP transistors will be discussed in the next section.

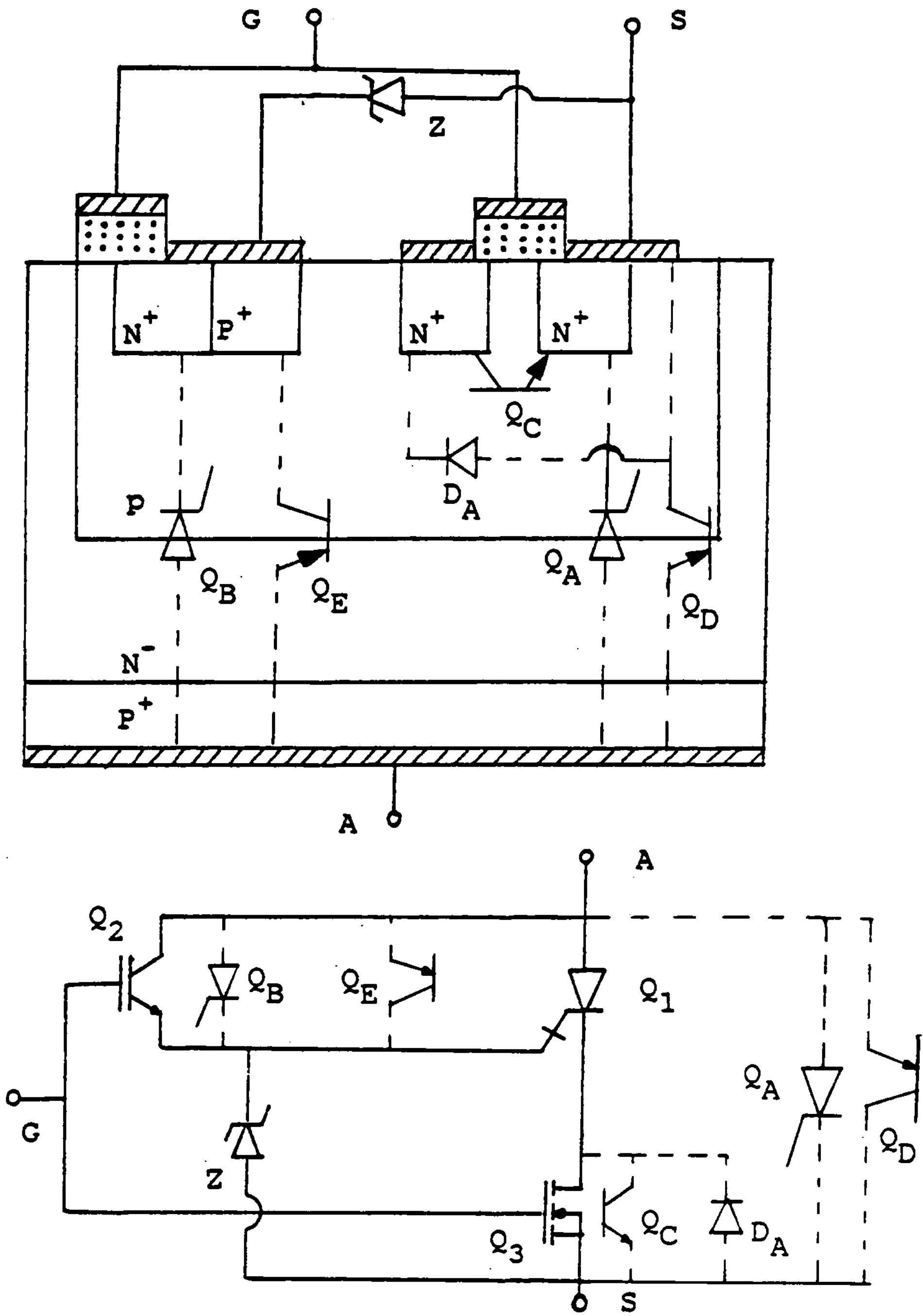


Figure 5.15: Parasitic Components in a Partially Integrated IGTO

5.9 SUPPRESSION OF THE PARASITIC THYRISTORS

5.9.1 Principle of Cathode-short

The principle of suppressing the parasitic thyristors is very similar to that of parasitic transistors. Consider a two-transistor equivalent circuit of a thyristor with a shunting resistor between the gate and cathode, as shown in Figure 5.16 [5.1].

Under a zero gate bias condition, the anode current is given by

$$I_A=MI_o/[1-M\alpha_{pnp}-M\alpha_{npn}(I_K/I_A)]$$

where M is the multiplication factor, I_o ($=I_{co,npn}+I_{co,pnp}$) the reverse saturation current of the base-collector junctions, α the common-base current gain and I_K the cathode current.

If the shunting resistor, R, is absent, $I_A=I_K$ so that

$$I_A=MI_o/(1-M\alpha_{pnp}-M\alpha_{npn})$$

and breakover occurs if $M=M_1= 1/(\alpha_{pnp}+\alpha_{npn})$. When R is present, I_K is much less than I_A so that

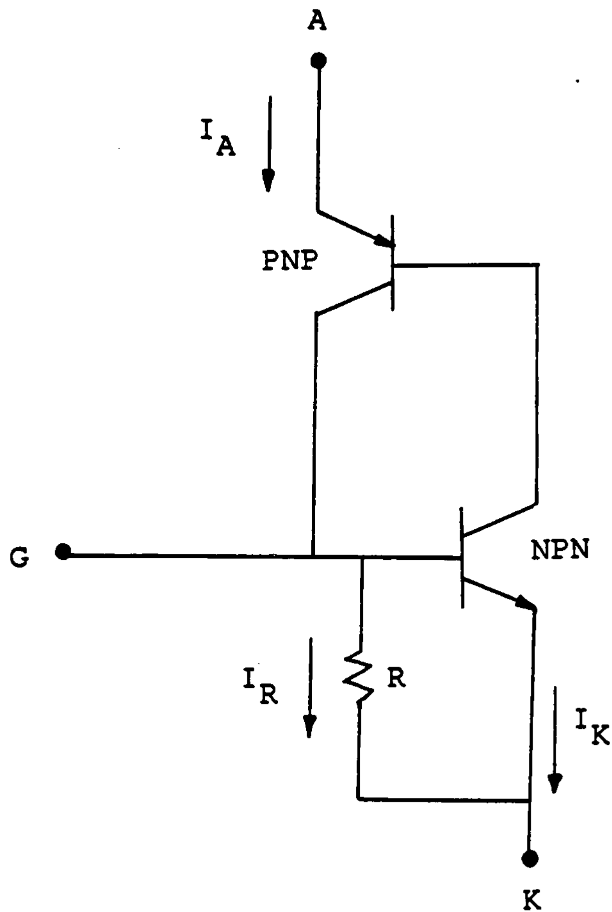


Figure 5.16: A Thyristor with a Shunting Resistor Between Gate and Cathode

$$I_A = MI_o/(1-M\alpha_{pnp})$$

and breakover occurs when $M=M_2= 1/(\alpha_{pnp})$. Since M_2 is greater than M_1, the thyristor with a shunting resistor is less susceptible to turn-on than the one without it.

5.9.2 Forming the Shunting Resistor

The shunting resistor, R, can be formed by overlapping the metalization on the gate-cathode junctions of the parasitic thyristors. This metalization overlap is normally referred to as a "Cathode-short". The shunt resistance value is determined by the sheet resistivity of the P-base and the lateral dimension of the overlapping.

5.9.3 Effect of Cathode-short

Although the cathode-short improves the dv/dt capability, it is done at the expense of larger chip areas for the IGTO. Since the cathode-short shunts the injection gate current away from the GTO, turn-on of P regions between the shorts will be affected, and the di/dt rating will be somewhat degraded [5.6].

5.9.4 Creation of PNP Transistors

Because of the use of cathode-short to form the shunting resistor, two PNP transistors, Q_D and Q_E, are created. Q_D is formed across the anode and source of the IGTO, and Q_E is formed between the collector and emitter of Q_2. These two PNP transistors have no adverse effect on the IGTO operation. Because the N^- region (corresponding to the bases of the PNP transistors) is very wide, the base transport factor of the wide-base PNP transistors is very small. Therefore, these PNP transistors have very low current gains, so the transistor action is very unlikely to happen.

5.10 FULL INTEGRATION OF IGTO

A fully integrated IGTO can be achieved by replacing the zener diode with a P-channel MOSFET or a P-channel IGT. Figure 5.17 shows a fully integrated IGTO using a P-channel IGT, Q_4, to replace the zener diode, Z.

The portions corresponding to Q_1, Q_2 and Q_3 are the same as described in Section 5.9. The P-channel IGT, Q_4, is obtained by doping an N^+ region as the collector of Q_4, and a P^+ region inside an N region as its emitter.

5.11 DEVICE OPERATION FOR FULLY INTEGRATED IGTO

5.11.1 Turn-on

Figure 5.18 shows the current path for the fully integrated IGTO during turn-on. When a positive gate voltage is applied, Q_2 and Q_3 are turned on but Q_4 is not. The Q_2 current functions as the gate current of Q_1 to turn it on. Q_4 is cut off because of the positive gate voltage.

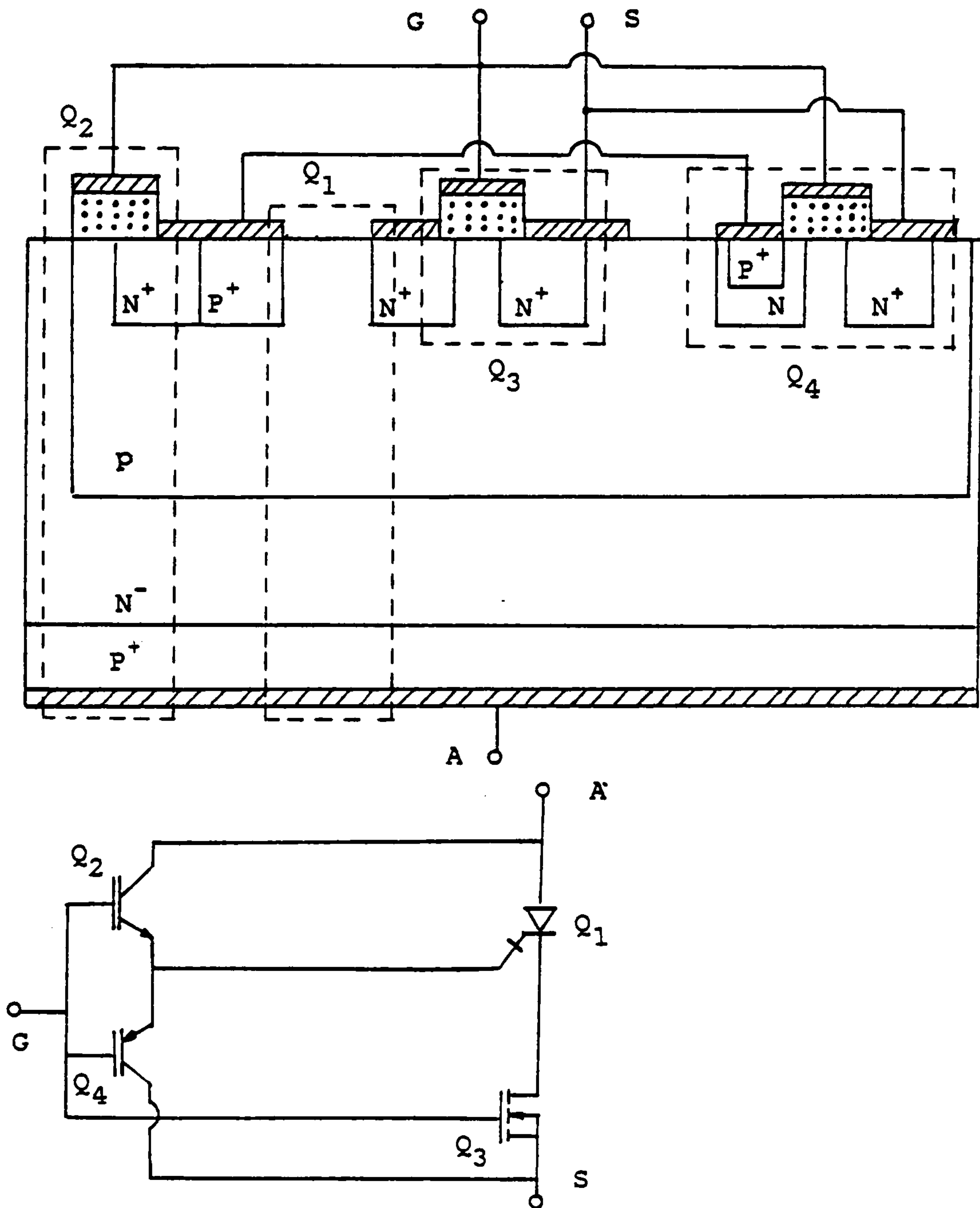


Figure 5.17: Device Structure for a Fully Integrated IGTO

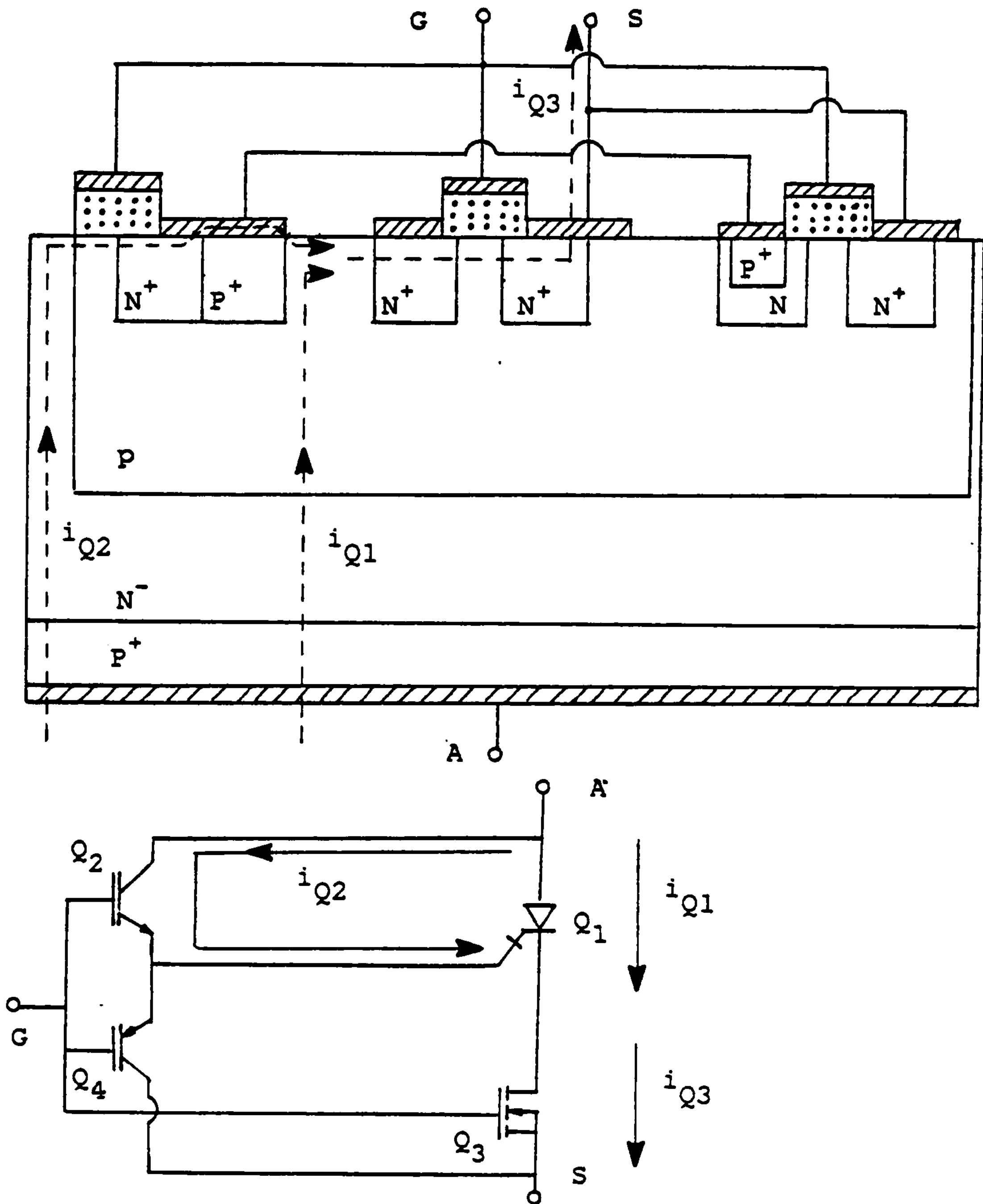


Figure 5.18: Current Path of a Fully Integrated IGTO During Turn-on

5.11.2 Conduction

During conduction, the N^- epitaxial layer is conductivity-modulated by excess carriers injected from the anode and the cathode. Once the GTO latches, the collector current of Q_2 is reduced to a minimum value.

5.11.3 Turn-off

Figure 5.19 shows the current path of a fully integrated IGTO during turn-off. When the gate voltage is low, channels of both Q_2 and Q_3 are cut off, but Q_4 is turned on. The anode current of Q_1, therefore, flows out of the Q_1 gate terminal through Q_4 to ground. Thus Q_4 plays the same role as the zener diode does.

5.11.4 OFF State

Once the excess carriers are depleted, the P-N^- junction blocks the applied voltage.

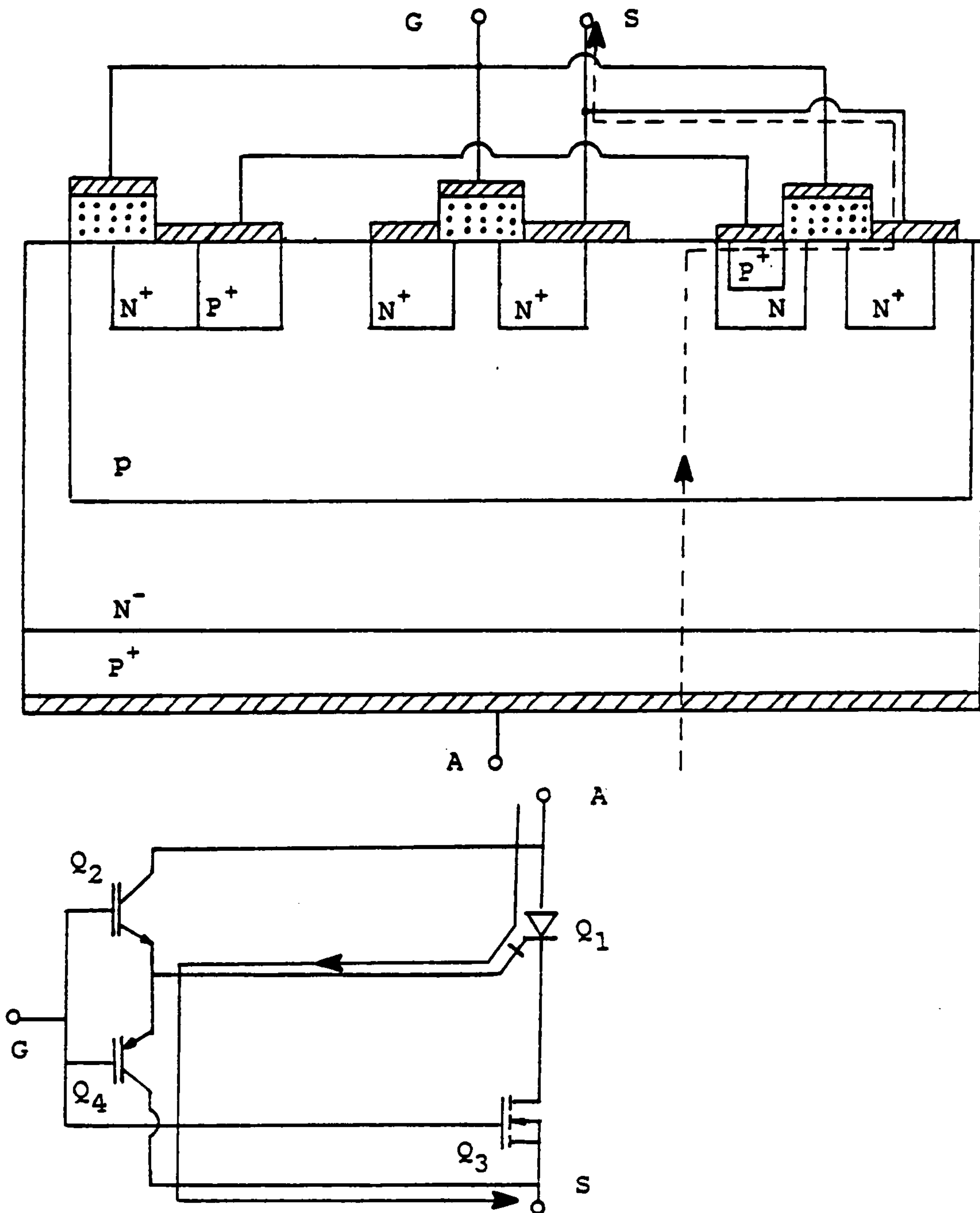


Figure 5.19: Current Path of a Fully Integrated IGTO During Turn-off

5.11.5 Parasitic Components

Because the emitter of Q_4 is tied to the emitter of Q_2 and the collector of Q_4 is connected to the source of Q_3 to replace the zener diode, no parasitic element will be formed in addition to those existing in a partially integrated IGTO.

5.12 COMMENTS ON INTEGRATED IGTO

5.12.1 Chip Area

Since cathode shorts are used to suppress the effects of the parasitics in an integrated IGTO, the device chip area is increased. If the IGTO is to be formed by using discrete devices, the cathode shorts may not be necessary, since the dv/dt capability is significantly enhanced as Q_3 holds OFF in the blocking state.

5.12.2 Conduction Drop

Because the IGTO is intended for higher power applications, the power dissipation of the zener diode, Z, for a partially integrated IGTO will be very high. The power loss is smaller for a fully integrated IGTO since a conductivity-modulated P-channel IGT (Q_4) has a lower conduction drop [5.7].

5.12.3 Lateral MOSFET Q3

Since a lateral MOSFET Q_3 is used in both the FGT and the IGTO, the comment on the lateral Q_3 discussed in Subsection 5.6.4 applies to the integrated IGTO as well.

Chapter VI

CONCLUSIONS AND SUGGESTIONS FOR FUTURE WORK

6.1 CONCLUSIONS

Two high voltage MOS-Bipolar power switching devices, the FET-Gated Bipolar Transistor (FGT) and the Insulated Gate Turn-off Thyristor (IGTO), were proposed and experimentally demonstrated. Both the FGT and the IGTO have desirable features for power switching devices: fast switching speeds, a voltage-driven requirement, high voltage and high current capabilities, an improved safe operating area and a small chip area requirement. The application characteristics of these two devices have been rather thoroughly investigated, which include: reverse blocking capability; temperature effect on the forward voltage blocking capability, on switching times, and on conduction voltage drop; paralleling of the devices; and power loss distribution. Half-bridge inverter circuits were built to test the switching performance of the IGTO for low current, high frequency application (4A/100KHz) and high current, medium frequency application (30A/40KHz). In a single-switch switching circuit, the FGT has been tested up to 300V and 30A, and the IGTO has been tested up to 300V and 100A.

Because of the availability of the high voltage Insulated Gate Transistor (IGT), the IGTO was tested up to 850V by substituting a MOSFET for an IGT.

It is noted that one of the main advantages of the FGT and the IGTO, from the viewpoint of chip area utilization, is that the emitter-open or cathode-open transistor, Q_3, is a low voltage device. As pointed out in Subsection 4.6.4, parasitic inductances associated with the leads increase the voltage requirement of Q_3. If the voltage requirement of Q_3 exceeds 200V, then the advantages of either the FGT or the IGTO are diminishing. A practical limit of the current achievable in these devices is estimated to be approximately 200A.

Due to the chip area requirement of the main power device, Q_1, and the drive transistor, Q_2, the intended voltage level is between 400V to 800V for the FGT and is between 800V to 2000V for the IGTO. Both the FGT and the IGTO should provide circuit designers with voltage controlled power switching devices for application territory beyond what is economically or technically achievable today.

6.2 SUGGESTIONS FOR FUTURE WORK

1. Due to the current availability of the IGT, the IGTO has been experimentally verified only up to 500V. Substituting a MOSFET for an IGT, the IGTO has been tested up to 850V. When IGTs with higher voltage ratings are available, it would be interesting to extend the IGTO concept demonstrated in the dissertation to a voltage level higher than 1200V.

2. It is believed that the IGTO should exhibit no reverse bias second breakdown characteristics because there is no mechanism for the current crowding phenomenon to occur. But this has not been experimentally verified. It is suggested that further investigation be pursued once a non-destructive RBSB tester for voltage-controlled devices is available.

3. Neither the FGT nor the IGTO has been experimentally fabricated in an integrated form. The integrated structure for both devices were proposed in the dissertation. It is suggested further effort be directed toward fabricating the integrated devices.

4. Recently, resonant converter circuits have received a lot of attention. The switching element in the resonant converter is either naturally commutated or turned off at a low current level. Turn-off stress of the switching element is, therefore, much reduced. However, the turn-on stress is still the same as in non-resonant converters. If either an FGT or an IGTO is used in a resonant converter, Q_3 and Z (or Q_4) can be eliminated. The remaining devices, Q_1 and Q_2, should provide good turn-on characteristics. The turn-off drive has to be achieved by a reverse base current for the FGT or a reverse gate current for the IGTO. However, the reverse current requirements are small in this case because they are turned off naturally or at a low current level. Further work in this area is recommended.

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