DEVELOPMENT OF A HIGH–DENSITY, OFF–LINE, QUASI–RESONANT CONVERTER USING HYBRID TECHNIQUES

by

DOUGLAS CHARLES HOPKINS

Dissertation submitted to the Faculty of the

Virginia Polytechnic Institute and State University

in partial fulfillment of the requirement for the degree of

DOCTOR OF PHILOSOPHY

In

Electrical Engineering

APPROVED:

F.C. Lee, Co–Chairman

F.W. Stephenson, Co–Chairman

G.S. Brown

L.C. Burton

D.Y. Chen

D.J. Nelson

August, 1989

Blacksburg, Virginia

DEVELOPMENT OF A HIGH–DENSITY, OFF–LINE, QUASI–RESONANT CONVERTER USING HYBRID TECHNIQUES

by

Douglas Charles Hopkins

Co–Chairmen: F.C. Lee and F.W. Stephenson
Electrical Engineering

(ABSTRACT)

The advancement of Very Large Scale Integration (VLSI) technology has reduced the size and increased the speed of information processing circuits. Consequently, power supplies for such circuits have had to meet increasing demands for power, yet simultaneously decrease in size. This need for higher power density in the supplies can be met with higher circuit operating frequencies and by using high–density circuit fabrication techniques.

Generally, when the conversion frequency of conventional Pulse–Width–Modulated (PWM) supplies approaches 1 MHz, the switching loss becomes very large. This sharply reduces the efficiency of the supply. A quasi–resonant topology reduces much of this loss. For a Zero–Current–Switched (ZCS) Quasi–Resonant Converter (QRC) the turn–off loss is nearly eliminated.

It was the objective of the research reported here to combine the quasi–resonant technology with thick–film hybrid microelectronics technology to produce a high density dc–dc converter.

For this research endeavor an off line, half–bridge ZCS–QRC was used. The circuit processed 300V and up to 20A with switching frequencies in the 1MHz to 2MHz range. The voltage and current levels exemplify the high electric field and current densities that must be considered in the design of most QRC circuits that process power up to 100W. Only available materials for thick–film hybrid processing were used although some characteristics were modified. No special magnetic or capacitive components, or semiconductors were developed.

To combine technologies the following were performed:

1. identification of critical power electronic circuit and hybrid component parameters such as maximum voltages and currents, thermal and electrical component impedances;
2. assessment of thick–film hybrid microelectronic materials and their compatibility in circuits having high voltage and current levels;
3. development of a complete thick–film power hybrid process; and
4. design, fabrication and evaluation of a power hybrid QRC that has high power–processing density.

ACKNOWLEDGEMENTS

I would like to thank my committee: Professors G.S. Brown, L.C. Burton, D.Y. Chen and D.J. Nelson, and in particular, my co–chairmen Professors F.C. Lee and F.W. Stephenson for their valuable advice and support. I would also like to thank and from the Digital Equipment Corporation, from Unitrode, from DuPont and from Micrasem also for their valuable advice and support. I would like to thank the Digital Equipment Corporation and the Virginia Center for Innovative Technology for providing funding, and International Rectifier, Ulano and Unitrode for providing materials for the research. Special thanks go to my colleagues, and , for giving help and perspective.

Above all I would like to recognize my parents and , the late and my family, and These eight people have most influenced my life and from each I have drawn something immeasurable and invaluable, which can never be forgotten.

TABLE OF CONTENTS

Abstract		ii
Acknowledgements		iv
Chapters		
1	INTRODUCTION	
1.1	Background	1
1.2	Objective	5
1.3	Summary of Results	7
2	ANALYSIS OF ZCS–QRC	
2.1	Introduction	12
2.2	Circuit Analysis and Design Equations	12
2.3	Calculation of Critical Parameters	18
3	MATERIALS AND CONDUCTOR EVALUATION	
3.1	Introduction	21
3.2	Material Testing	21
3.3	Conductor Resistivity	24
3.4	Conductor Resistance	25
3.5	Optimum Conductor Thickness	28
3.6	Selection of Conductor Width	30
3.7	Summary	34
4	PROCESS DEVELOPMENT	
4.1	Introduction	43
4.2	Process Development	45
4.3	Parameters Affecting Fabrication	46
4.4	Thick Printing Process	51
4.5	Printing Results	55
4.6	Electrical Characteristics	57
4.7	Wide Conductor Printing	58
4.8	Summary	61
5	DESIGN, FABRICATION AND TESTING OF THE ZCS–QRC	
5.1	Introduction	71
5.2	Circuit Design	71
5.3	Thermal Analysis of Semi–conductors	74
5.4	Circuit Performance	82

6 SUMMARY 102

References 105

Appendix

A ZCS–QRC CIRCUIT ANALYSIS
A.1 Circuit Analysis 116
A.2 Primary–Circuit Analysis 121
A.3 Critical Design Parameters 123

B DETERMINATION OF CONDUCTOR THICKNESS AND WIDTH FOR POWER HYBRID CIRCUITS
B.1 Introduction 131
B.2 Current Distribution 132
B.3 Conductor Impedance 135
B.4 References 137

Curriculum Vitae 140

TABLES

3.1	Conductor Resistivities	36
3.2	Thick–Conductor Resistivities	37
4.1	Fired Thickness for Selected Substrates	62
4.2	Conductor Resistance	63
5.1	Design Requirements of Hybridized ZCS–QRC	85
5.2	Calculated Component Values and Circuit Parameters for Hybridized ZCS–QRC	86
5.3	Parts List for Hybridized ZCS–QRC	87
5.4	Properties of Materials	88
5.5	Component Dimensions for Semiconductors and Materials	89

ILLUSTRATIONS

2.1	Schematic of an off–line zero–current–switched quasi–resonant converter.	20
3.1	Test pattern developed for material selection of conductor inks.	38
3.2	Typical thickness profile of a fired conductor showing the conductor cross section.	39
3.3	Test pattern developed for testing silver migration at varied electric field intensities.	40
3.4	Test pattern for determing adhesion and resolution.	41
3.5	Variation of resistance factor due to Γ_r.	42
4.1	Cross section of screen and emulsion.	64
4.2	Test pattern for measurement of resistivity, adhesion and resolution.	65
4.3	Fired test pattern with conductor thickness greater than 50 μm (2 mils) and resolution better than 175 μm (7 mils).	66
4.4a	Distribution of adhesion failures caused by separation of the conductor from the substrate.	67
4.4b	Distribution of adhesion failures caused by separation of the conductor from the substrate. Tests were performed after 2300 hours of storage at room temperature and low humidity.	68
4.5	Illustration of patterned screen ready to be placed over pillars.	69
4.6	Example circuit substrate for a 100 W, 2 MHz switchmode power supply.	70
5.1	Substrate for HB ZCS–QRC.	90
5.2	Two–dimensional nodal network.	91

5.3a	Cross section of hybrid circuit with two transisters mounted in close proximity.	92
5.3b	Temperature profile of structure of Fig.5.3a.	93
5.4	Temperature profile of rectifiers with anode–to–substrate connection.	94
5.5a	Gate–to–source voltage across lower switch transistor.	95
5.5b	Drain–to–source voltage for lower switch at half load (10 A) and with a source voltage of 300V.	96
5.5c	Drain–to–source voltage for lower switch at full load and with a source voltage of 300 V.	97
5.6	Efficiency vs output current for low and nominal input voltages. Output voltage $V_o = 5$ V.	98
5.7	Switching frequency (half of conversion frequency) vs. output current for low and nominal input voltages.	99
5.8	Measured closed–loop gain and phase at full load and nominal input voltage.	100
5.9	Hybridized HB ZCS–QRC.	101
A.1	Schematic of HB, HW ZCS–QRC.	126
A.2	Reduced schematic for ZCS–QRC analysis.	127
A.3a	Primary–circuit schematic of half–bridge converter.	128
A.3b	Equivalent circuit for inductor charging stage.	129
A.3c	Equivalent circuit for resonant stage.	130
B.1	Strip conductor.	138
B.2	Current distribution in strip conductor.	139

CHAPTER 1
INTRODUCTION

1.1 Background

Power electronics is an application–driven technology and, as such, has responded to the needs of industry and government. One segment of the technology, encompassing switchmode dc–to–dc conversion, has responded particularly to the needs of the computer and aerospace industries. Here, power supplies with higher power–processing densities, more efficient operation and faster response are needed.

One method for achieving higher density is to increase operating frequency. But an increase in frequency must be accompanied by a decrease in switching loss to avoid a decrease in power conversion efficiency. Limited by the present day components and materials, when the frequency increases to hundreds of kilohertz the switching loss in square–wave converters becomes very large. This has caused converter operation to be limited to lower frequencies generally below 100 kHz [1–3].

In the late 1970s and early 1980s, a new power–processing technology called quasi–resonant conversion was introduced [4–7] which allowed higher operating frequencies by significantly reducing switching losses. The quasi–resonant approach uses an auxiliary resonant circuit in series with the switching device to shape the current or voltage waveforms to be quasi–sinusoidal during turn on and turn off, hence reducing switching loss.

If the auxiliary resonant circuit uses an inductor in series with the switching device, then, during turn on of the device, current rise is delayed while the switch voltage collapses, thus minimizing the volt–amp product of power dissipated during turn on. The current through the switch will flow until the auxiliary resonant circuit makes the current resonate to zero. The switch can then be turned off. At turn off the volt–amp product is zero. Hence, this scheme is termed zero–current switching (ZCS). Unfortunately, prior to turn on any voltage across the switch represents stored charge in the interelectrode capacitance of the switch. This charge is dissipated within the switch and represents switching loss during turn on.

If the auxiliary resonant circuit uses a capacitor in parallel with the switch, then, during turn off, current is commutated to the capacitor and the switch simultaneously has nearly zero voltage across it. Hence, the volt–amp product is minimized and the voltage across the switch will resonate to zero. The switch can then be turned on and the current can thus commutate from the capacitor to the switch. The volt–amp product of the switch during turn on is zero. This method is known as zero–voltage switching (ZVS).

Each method allows for higher frequencies of operation than in square–wave converters. The ZCS technique allows operation up to a few megahertz [4,8] while the ZVS method allows operation at tens of megahertz [9].

The use of quasi–resonant techniques alone can provide great gains in increased frequency and, consequently, reduced component size and faster response. But to achieve higher density, the circuit size must be reduced.

To achieve reduced circuit size a high–density circuit fabrication technique must be used. Conveniently, such a technique is also needed when operating frequencies are at megahertz and higher. At such high frequencies the parasitic inductances and capacitances of the circuit and its components have significant effects on circuit operation. Some parasitics such as the leakage inductance of a transformer in a forward converter can be used as a resonant inductance when applying the quasi–resonant technique. Other parasitics, such as transistor gate lead inductances, are not desirable and must be minimized.

In high–frequency quasi–resonant converters, the method of fabrication becomes an integral part of the circuit development. It is important, then, to select a technique that is reproducible beyond the laboratory.

The ultimate technique for highest density fabrication presently available would be monolithic integration. However, for power circuits certain components such as inductors and large volume capacitors are not integrable. The technique for the next densest fabrication uses surface mounting of which there are two forms. One form, which has had a recent revival, mounts packaged components on the surface of printed circuits and

has application in the microelectronics packaging industry. As compared to the traditional printed circuit board method of through–hole circuits there are no large hole prints that occupy space. Another form of surface mounting also used in the microelectronics industry is known as thick–film hybridization. This technique allows the mounting of large area components directly onto a thermally conductive, dielectrically isolating substrate and the direct mounting of unpackaged semiconductors. These last two features are of great importance because interconnect inductances and thermal resistances are minimized when direct mounting is used and component packages are eliminated.

Thick–film hybrid microelectronics circuit fabrication techniques have been used for several decades for the development of very–high–frequency and ultra–high–frequency circuits in the communications field. This technique has also been used in the production of simple planar power circuits such as 20kHz dc chopper circuits and for packaging of multiple power semiconductors in, for example, a three phase, full–bridge FET module. However, the technique has not been widely used for the development of power supply circuits, especially those that operate at low megahertz frequencies. In fact, the use of power hybridization for the fabrication of high–frequency circuits that operate in the 50W to 1kW range and at low megahertz is not commonplace. Its use as a development tool is apparently new as judged by the availability of so few references [10–43] for the period of 1969 through 1985.

1.2 Objective

The advancement of VLSI continues to reduce the size and increase the speed of information processing circuits. Consequently, power supplies for such circuits must meet ever increasing demands for power while simultaneously decreasing in size. This need for higher power density in the supplies can be met through proper selection of circuit topologies, circuit operation at higher frequencies and by using high–density circuit fabrication techniques.

In 1985, the Digital Equipment Corporation (DEC) and the Virginia Center for Innovative Technology sponsored research into a high frequency, high–power– density power converter applicable to a low–end computer line. Such a converter should operate off line (from 300Vdc nominal) and deliver 5V at 100W. A goal of 25W/cu.in. was set representing a five to ten times improvement over what was available commercially. A topology described by Liu [44] and suggested by Heyman with modification for half–wave operation [45] was adopted for development. The topology for the off–line application was a half–bridge (HB), zero–current switched (ZCS) quasi–resonant converter (QRC) operating in half–wave mode with secondary–side resonance. Jovanovic [46,47] showed this topology to be optimum for the application.

The objective of the research reported here was to combine the quasi–resonant technology with the thick–film hybrid microelectronics

technology to produce a high density converter using the HB ZCS–QRC as the vehicle. The research assessed the critical electrical parameters in the QRC operation such as voltage, current and frequency that limited application of the existing hybrid technology in the areas of materials, thermal management and process compatibility in its application to the power stage of the QRC. Research was then conducted to establish a thick–film power hybrid process applicable to the QRC.

The scope of the research was divided into three distinct thrusts:

1. to design a ZCS–QRC hybrid power circuit that would operate at megahertz frequencies;

2. to fabricate a ZCS–QRC circuit with a minimum of 25W/cu.in; and

3. to develop a thick–film power hybrid process for low–voltage circuits having tens of amps of current flow and low–current circuits having hundreds of volts.

An off–line HB ZCS–QRC was used for this research endeavor. The circuit is feasible for practical dc–to–dc conversion and processes 300V and up to 20A with switching frequencies in the 1MHz to 2 MHz range. The voltage and current levels exemplify the high electric field and current densities that must be considered in the design of most QRC circuits that process power up to 100W. Only available materials for thick–film hybrid processing were used although some material characteristics were modified.

No special semiconductor, magnetic or capacitive components were developed. For a description of the characterization of operation development of the control of the ZCS–QRC and a discrete implementation of the design, which was used in this research, the reader should refer to works by Milan M. Jovanovic [8,46–49, 68, 70, and others].

To combine technologies the following tasks were performed:

1. identified critical power electronic circuit and hybrid component parameters such as maximum voltages and currents, and thermal and electrical component impedances;

2. assessed thick–film hybrid microelectronic materials and their compatibility in circuits having high voltage and current levels, and assessed the limitations of the thick–film process relevant to the fabrication of power electronic circuits;

3. evolved and empirically verified a complete thick–film power hybrid process;

4. designed, fabricated and evaluated a power hybrid QRC that has high power–processing density; and

5. assessed the benefits and limitations of combining the technologies pertinent to high–frequency, high–density, dc–to–dc converters.

1.3 Summary Of Results

A program was written to determine the component values of the HB ZCS–QRC when operating with line voltage variations and to determine the

maximum voltages and currents occurring in the circuit under worst–case conditions [48]. These maximum parameters were used to determine the limitations of materials and process; and to determine physical circuit design and layout.

Thick–film conductor and dielectric materials were also assessed. Since sufficiently accurate data about very low resistivity conductor pastes were not readily available from the manufacturers and, in some instances, not known, a test procedure was developed [49]. Resulting data was used for the hybrid circuit design.

Since hybrid circuits have traditionally not been used at voltage levels above 100V, the presence of greater than 300V as used in the ZCS–QRC can produce electric field strengths that cause interelectrode surface electromigration of the metallic conductors. Studies [50–58] have shown that suitable encapsulation of conductors can retard migration. Dielectric materials were assessed and an experiment devised to determine the suitability of encapsulants of silver conductors in low humidity environments. Test results for three dielectrics show no migration for 3000 hours at 100°C.

Traditionally, the thick–film hybrid process produces conductor thicknesses of approximately 15 microns. Thicker conductors are needed for power hybrids. However, at the low megahertz operating frequencies of the ZCS–QRC, the ac resistance is of concern. Unfortunately, no appropriate

conductor models exist for determining conductor thickness and width. Such a model was developed [67] for prediction of the electrical characteristics of the conductors and determination of their geometries.

Other assessments made included calculating hybrid circuit parasitics such as interconductor capacitances formed between conductors by electric field coupling across the surface and through a metal heat sink. The effect of parasitics on circuit operation was also evaluated. Because of the planar shape of the conductor, the low dielectric constant of substrate materials, and the large spacings between the conductors and heat sinks, the parasitic capacitances were found to be negligible (some in the atofarad range). Thermal conductivities of materials were assessed and used as part of the evaluation.

Assessment of resistor materials was limited. It was determined that the typical application of resistors in ZCS–QRCs is for snubbers, which is noncritical, and no special testing or processing was needed.

Evaluation other materials such as substrates and attachment materials are given in [49] and [68]. Using information from above and working within available laboratory resources, the author determined that standard materials could be used for hybridization of the ZCS–QRC. However, a suitable hybrid process was not available from any known source. The development of the process was undertaken. It can be divided into one major and three minor thrusts.

The major thrust was concerned with conductor thickness. Because of the limited current carrying capability (with low power loss) for traditionally printed thick–film conductors, a process was developed to thick print thick–film conductors. Techniques for changing paste viscosity, preparing and patterning screens with very thick emulsions, printing of conductors with wet thicknesses exceeding 150 microns, drying of conductors and avoiding flow out, and firing to attain high electrical conductivities were established in the laboratory. A process yielding 50–microns–thick conductors with better than 175–microns resolution resulted directly from this work [69].

The firing techniques yielded sintered resistivities that were only 8.2% greater than pure metal. This is the first documentation [69] of such low resistivities in the industry.

Also developed for the power hybrid process were process rules for the printing of a thick dielectric layer across thick conductors, attachment of substrates with a predictable thermal interface, and a method of semiconductor attachment. For the latter, heavy aluminum wire was used for top–surface transistor connections. The method of semiconductor attachment was not new for the industry, although it was new to the laboratory, and was shown to be compatible with the thick–printing process. In particular, wire bonding to thick conductor prints was extremely successful.

The development culminated with the hybridization of the power stage of a 100W, off–line, half–bridge ZCS–QRC by the author. Its maximum

switching frequency was 1.1 MHz (2.2 MHz conversion frequency) when delivering 5V at 20A from a 300 Vdc input and with 78% efficiency. The efficiency is one to two percentage points better than attainable by a discrete version operating at lower frequency at the same power level. The power–processing density of the power circuit is 3.1 W/cu.cm (50 W/cu.in). This power stage uses thick printed conductors having stepped thicknesses of 38 microns and 55 microns.

A two–dimensional analysis was performed to determine thermal profiles within the hybridized ZCS–QRC. The profiles show peak temperatures in semiconductor junctions and surface temperatures of other components. The information identifies limitations on component placement and thermal impedances of attachment materials.

CHAPTER 2

ANALYSIS OF ZCS–QRC

2.1 Introduction

To assess the application of the thick–film hybrid technology to the development of the ZCS–QRC, limitations of the technology must be determined. The limitations depend on certain critical parameters in the ZCS–QRC. These parameters are maximum currents in conductors, which are used to determine conductor widths and methods for component attachment; maximum circuit voltages, which are used to determine conductor and component spacing; and component operating characteristics, particularly those that are frequency dependent, which are used to compute power losses and thermal profiles in the hybrid circuit.

Before the critical parameters for the ZCS–QRC can be evaluated the circuit must be analyzed and a specific design implemented. The following two sections present the analysis, design and calculated critical parameters.

2.2 Circuit Analysis and Design Equations

The specific application to which research was applied required that a dc–to–dc converter circuit operate off–line, i.e., from 300 Vdc; provide 5 Vdc at 100 W; and have a power density of 25 W/cu.in. or higher. To obtain the high density, frequencies of operation in the megahertz range were needed.

When the operating frequency of conventional PWM converters approaches 1 MHz, the switching loss becomes large, thereby sharply reducing the efficiency of the supply. A quasi–resonant topology reduces much of this loss. For a ZCS–QRC the turn–off loss is nearly eliminated [4]. It has been shown that when comparing the flyback, forward, and half–bridge ZCS–QRC topologies for off–line applications, the half–bridge topology operating in half–wave mode with secondary–side resonance is preferred [46]. The topology can offer a high efficiency of operation and provides better core utilization and automatic flux reset of the transformer.

The operation of the ZCS–QRC, shown in Fig. 2.1, is described in [46] and a large signal analysis is given in Appendix A. Design equations are obtained from the analysis and provide the necessary basis for calculation of the critical circuit parameters.

The design equations need to include worst–case operating conditions. The following parameters are used as the independent variables in the equations. Note that, since high–frequency operation of the circuit is desired, it is assumed that the transformer is wound with minimum secondary leakage inductance, and the inductance value is considered to be an independent variable for calculations. The leakage inductance also represents the total resonant inductance in the design equations. The parameters are:

supply voltage:	high line	V_s^{max}
	low line	V_s^{min}

output:	nominal voltage	V_o
	allowed ripple (p–p)	V_o^δ
	minimum load	R_L^{max}
	maximum load	R_L^{min}
filter inductor:	ripple current (p–p)	I_f^δ
transformer:	turns ratio	N
	leakage inductance	L_r

These parameters are used in the following design equations to determine component values. The component values will be used in the following section to compute critical circuit parameters, such as maximum currents and voltages. The critical parameters are then used in the hybrid design.

RESONANT CIRCUIT:

From the condition that the resonant current must be greater than the output current by some margin (derived from Eqs. A.7 and A.8) to maintain zero–current switching, the resonant capacitor value is:

resonant capacitor:

$$C_r = L_r \frac{(2NV_o)^2}{(0.9V_s^{min}R_L^{min})^2} \quad (2.1)$$

The following can then be calculated:

resonant frequency: $F_r = 1/(2\pi\sqrt{L_r C_r})$ (2.2)

resonant impedance: $Z_r = \sqrt{L_r/C_r}$ (2.3)

conversion frequency: $F_C^{max} = 2NV_oF_r/V_S^{min}$ (2.4)

switching frequency: $F_S^{max} = F_C^{max}/2$ (2.5)

The 0.9 factor in (2.1) gives a 10% margin to assure that the resonant current is greater than the output current under worst–case conditions, thereby maintaining zero–current switching.

INPUT CAPACITOR BRIDGE:

The capacitor values are calculated from an energy transfer equation describing the input energy delivered from the capacitors to the remaining circuitry and load [49]. Hence:

$$C_1 = C_2 > \frac{10V_o^2}{R_L^{min} F_C^{max} (V_S^{min})^2} \quad (2.6)$$

This assumes a maximum $\pm\, 0.1V_S^{min}$ variation of the center point voltage of the divider and an 80% efficient converter. (The actual converter built and tested provided 78% efficiency.)

SWITCHING TRANSISTOR SELECTION:

From Jovanovic in [64]

$$R_{ds}^{opt} = \sqrt{kF_r/3}\ \frac{2NV_s^{max}\ R_L^{min}}{3V_o} \tag{2.7}$$

where k is a constant value of R_{ds} (on) × C_{oss} for a particular transistor family. The C_{oss} is the output switch capacitance. For example, the IRF7xx family has k ≃ 12 ps. The voltage across the device is clamped to the supply voltage. However, the voltage rating of the transistor should be greater than V_s^{max} by some safety margin.

OUTPUT RECTIFIER SELECTION:

The maximum rated rms current: $I_{rec}^{max}=1.18\ \frac{V_o}{R_r^{min}}\sqrt{\frac{F_s^{max}}{F_r}}$ (2.8)

Peak reverse voltage: $V_{rec}^{max} = 3V_s^{max}/N$ (2.9)

OUTPUT FILTER VALUES:

From Vorperian [71], the filter inductance can be calculated from the resonant inductance, i.e.

$$L_f = L_r(A + B)\ \frac{E_c\ M^{max}}{E_f\ M^{min}} \tag{2.10}$$

A $= (1 - M^{min})[\pi - \cos^{-1}(1 - M^{min})]$

B $= \sqrt{(2-M^{min})}\ M^{min}$

M^{min} $= 2V_oN/V_s^{max}$

$M^{max} = 2V_oN/V_s^{min}$

$Q_P^{min} = R_L^{min}/\sqrt{(L_r/C_r)}$

$E_c = Q_P^{min}/M^{max}$

$E_f = I_f^{\delta}R_L^{min}/2V_o$

For steady state, the output filter capacitance is:

$$C_f = \frac{0.125 I_f^{\delta}}{V_o^{\delta} F_c^{min}} \tag{2.11}$$

where, again from [65],

$F_c^{min} = 4\pi M^{min}/X_{m,q}$

$Q_P^{max} = R_L^{max}/\sqrt{L_r/C_r}$

$Q_m = Q_P^{max}/M^{min}$

$X_{m,q} = \pi + \sin^{-1}(1/Q_m) + 1.5\, Q_m + (Q_m^2 - 1)^{1/2}$

The maximum ESR of the filter capacitor is:

$$ESR^{max} = V_o^{\delta}/I_o^{\delta} \tag{2.12}$$

where

$$I_o^{\delta} = \frac{V_o}{R_L^{min}} - \frac{V_o}{R_L^{max}} \tag{2.13}$$

The ESR^{max} accounts for voltage drops due to current through the capacitor and does not account for variations due to stored energy in the filter inductor which should be considered for step load changes, particularly from full load to light load.

2.3 Calculation Of Critical Parameters

The above design equations are used to determine component values which will, in turn, be used to determine critical circuit parameters. These input data selected to satisfy the needs of the associated application and the resulting design data are given in Chapter 5 for the design of the ZCS–QRC.

For the circuit shown in Fig. 2.1 and from the equations in Appendix A:

1. the maximum voltage stress in the primary side is V_{ds};
2. the maximum current through the primary side switches and connecting conductors is I_{rec}^{max}/N;
3. the maximum current through the capacitors and connecting conductors is one half of the above value;
4. the maximum current through the secondary rectifiers, resonant capacitor and associated conductors is I_{rec}^{pk};
5. the current through the freewheeling diode, output filter and associated conductors is I_o;
6. the maximum voltage at the secondary of the transformers is V_s/N;

7. peak voltage between the rectifiers and the filter inductor is 2 V_s/N;
8. the voltage at the output is V_o;
9. the maximum frequency that must be considered for current conduction is the conversion frequency, F_c.

These values will be used in the following chapters, particularly Chapter 5, to determine the QRC design parameters and the criteria for evaluating materials.

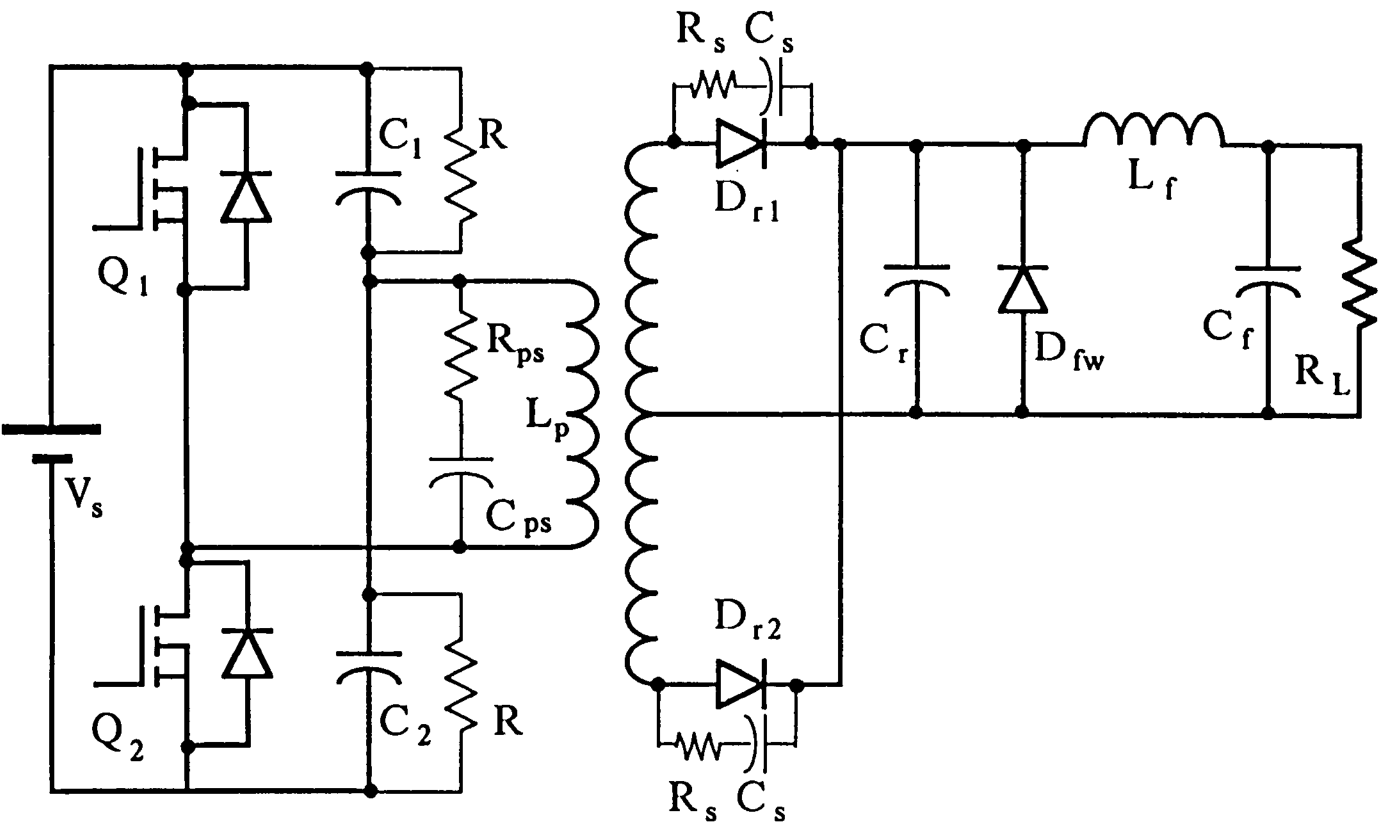

Fig. 2.1 Schematic of an off–line zero–current–switched quasi–resonant converter.

CHAPTER 3

MATERIALS AND CONDUCTOR EVALUATION

3.1 Introduction

Material selection is a critical part of the design of a high frequency, off line, thick–film–hybrid converter since characteristics such as electrical conductivity, high–field metal migration and thermal conductivity can limit the frequency and power density of the converter [72]. The materials used in the thick–film hybrid design can be divided into four categories: substrates, interconnects, dielectrics, and attachments.

Substrate materials such as aluminum nitride, beryllia and porcelainized steel were not considered because of high cost, poor availability or unproven reliability. Conductor materials such as copper and gold were also not considered for similar reasons. An alumina substrate and a silver–based metal conductor were selected for evaluation because of their desirable electrical and thermal characteristics [55]. Since the focus of the research was the design and development of the converters, only suitable materials rather than optimal materials were required.

3.2 Material Testing

Materials can be evaluated for their chemical, mechanical and electrical characteristics. The concerns for power hybrids in this research, however, were limited to electrical characteristics, specifically, conductor resistivity and electromigration.

There appears to be no information available about fired ink resistivities in the literature or from power hybrid circuit manufacturers. Hence,it is not well known what the resistivities of thick–film silver inks are after firing. Since manufacturers do not use highly accurate techniques for resistivity measurements, only approximate values are generally available. These values may be orders of magnitude above the actual value.

The pattern shown in Fig. 3.1 was developed and used for characterizing conductor resistivities. The bifilar serpentine pattern, shown to the left in the figure, was designed to have 200 squares of material with each square 0.5 mm (20 mils) wide. The remaining patterns were not used.

To obtain the resistivities, both resistance and geometrical profiles of the patterns were measured. An example of such a profile is shown in Fig. 3.2. The accuracy of the resistivity measurement depended on the accuracy of the profile measurement. Because of the significant thickness variation in the conductor cross section, only an average thickness could be used.

Two silver–based materials from each of three manufacturers were evaluated in a standard thick–film process using this serpentine pattern. The resulting resistivity measurements are shown in Table 3.1. Resistivity was measured at both room temperature (25°C) and with varying temperature (dr/dt). The material by DuPont, No.6160 (DuP6160), has the lowest tested resistivity at 0.89 mΩ–mils (2.26 μΩ–cm). (The manufacturer's data gives the resistivity as 2 mΩ–mils (5.09 Ω–cm)). It should be noted that the change in resistance due to temperature is appreciable. For a 100°C

increase the resistivity increases 38%. This significant increase affects the conductor skin depth which will be discussed in the following section.

Besides resistivity, electromigration of the conductor was considered. This topic has been studied at length [50–58]. Conclusions show that forming a hermetic encapsulation of the conductor inhibits hydroxal ions from significantly contributing to the surface transport of charge through the encapsulating medium as might occur in multilayer dielectrics. Thus, proper encapsulation and the elimination of trapped impurities by proper cleaning causes the rate of migration to be extremely slow. The method of cleaning used was to air fire the substrate just prior to processing.

To verify the abatement of migration, the test pattern shown in Fig. 3.3 was designed which contains four duplicate patterns. Each duplicate provides eight lines with each pair of lines having stepped conductor spacings varying from 0.5 mm (20 mils) to 2.5 mm (100 mils). The conductors forming the lines were energized with 1000 V and thus provided electric field intensities of 2,000 V/mm to 400 V/mm, respectively. The edges of the steps which form the line patterns are rounded to avoid field concentration.

Each test substrate had half of its patterns coated with compatible dielectric coatings or migration–resistant overglazes. The coatings were DuPont 5704, ESL 4904 (from Electro Science Laboratories), and TFS 1151 (from Ferro). Six substrates, two for each manufacturer, were energized with 1,000 Vdc, heated to 100°C and maintained in a low humidity environment

with less than 10% R.H by using a desiccant. To detect surface migration a visual inspection was conducted and leakage current was measured. Neither indicator showed any change after 3100 hours of testing. Hence, the coatings provided sufficient migration abatement.

3.3 Conductor Resistivity

An important issue when using thick–film techniques to develop power supply circuits is the use of low resistance conductors. Thick–film silver ink was selected for processing because of its low resistivity but, as discussed in the previous section, an accurate value of its resistivity was not generally known, and the preliminary measurements only provided basic information for material selection. An accurate knowledge of the resistivity is needed, however, in the circuit development to be discussed in Chapter 5.

Besides resistivity, a good knowledge of the ac resistance (due to skin effect) is needed when medium to high frequency effects are included. Thus, to determine accurately the value of conductor resistance both resistivity and skin effect must be accurately determined.

Determination of resistivity was achieved by measuring the dc resistance of a processed silver conductor of known geometrical shape. Inaccuracy in the determined value was due to the difficult geometrical measurement. However, using a thick–printed conductor, as described in Chapter 4, the geometrical error was significantly reduced.

The geometry problem is illustrated in Fig. 3.2. The average thickness of the cross–section of a typical thick–film conductor is approximately 15 microns (0.6 mils) with a variation of approximately three microns. The thick–printing process described in Chapter 4 gives an average conductor thickness of 50 microns to 60 microns with the same absolute thickness variation. The measurement error of the cross section of area is now less than 10%. Thus, the dc resistivity can be determined to within 10%.

Figure 3.4 shows a DuPont pattern used for developing the thick printed conductor process and for determining resistivity. The serpentine pattern to the left was used for resistance measurements. Using this pattern, twelve thickness measurements were taken and then averaged to obtain an effective area for the cross section of the conductor. Table 3.2 summarizes the dc conductor resistance and thickness measurements, and the calculated resistivities (from Eq. 4.2) of five sample substrates. The shape of the cross section of a conductor is trapezoidal and is considered in the calculation. The average resistivity is calculated at 1.72 microhm–cm which is within 10% of the absolute resistivity for pure rolled silver (1.58 microhm–cm). This value is the key to calculating the ac resistance of the conductor.

3.4 Conductor Resistance

Not all the currents flowing in the ZCS–QRC will be uniformly distributed within the cross section of the conductors because of skin effect which is caused by the moderately high frequency of operation. A typical model for the ac resistance of a conductor is [59]:

$$R_\delta \propto \frac{\zeta}{2 \; \sigma \; \delta} \qquad (3.1)$$

where the skin depth

$$\delta = (\pi \, f \, \mu \, \sigma)^{-1/2} \qquad (3.2)$$

and ζ is length to width ratio

σ is conductor conductivity (S/cm),

f is frequency (Hz), and

μ is conductor permeability.

This formula is for a conductor that is infinitely thick relative to the skin depth δ. For the ZCS–QRC, which is operating between 1 MHz to 10 MHz, this assumption of infinite thickness is not valid in our case. If a physical conductor thickness is between 0.1δ and 2δ skin depth thickness, then the total resistance is best expressed as

$$R = R_\delta \frac{\sinh \; v \; + \; \sin \; v}{\cosh \; v \; - \; \cos \; v} \qquad (3.3a)$$

and

$$v = t/\delta \qquad (3.3b)$$

where t is the actual conductor thickness. This equation has been developed in detail in Appendix B.

For large values of v ($t >> \delta$) which occur at high frequencies the conductor appears very thick relative to the skin depth and

$$R \longrightarrow R_\delta \tag{3.4a}$$

where the ac resistance is given by;

$$R_\delta = \zeta/2\sigma\delta \qquad (t >> \delta) \tag{3.4b}$$

The ac power dissipated in such a thick conductor is equivalent to the dc power dissipated in a conductor of thickness δ carrying a uniform current density, i.e.,

$$R_\delta^{v>5} = R_{dc}^{v\,=1} \tag{3.5}$$

where R_{dc} is a dc measured resistance. It can also be shown [59] that the phase angle of the total conductor impedance is 45° under these conditions ($t>>\delta$).

The conductor thickness of thick–film power hybrid circuits seldom exceeds 50 μm with typical prints being 15 μm thick. For a hybrid circuit using a 2.5 $\mu\Omega$–cm silver conductor, the skin depth at 1 MHz is 80 μm and at 10 MHz is 25 μm. Hence, the skin depth exceeds the conductor thickness. For the high–frequency 2 MHz ZCS–QRC being developed here (3.3a) will be used to determine the resistance and to predict power loss.

3.5 Optimum Conductor Thickness

It is important in power hybrid circuits to have as low a sheet resistance as possible. By combining (3.3a) and (3.4a) the conductor resistance can be expressed as

$$R = R_\delta \Gamma_\gamma \tag{3.6a}$$

where

$$\Gamma_\gamma = \frac{\sinh v + \sin v}{\cosh v - \cos v} \tag{3.6b}$$

From these two equations it can be seen that the resistance is composed of two functions; one dependent on thickness, the other on the number of squares of area.

Figure 3.5 shows the value of Γ_γ for various thickness ratios v. Solving for the minimum of Γ_γ or from the graph it can be shown that the minimum Γ_γ for a given skin depth and resistivity occurs when the total conductor thickness is

$$t = \pi\delta \tag{3.7}$$

and that

$$\Gamma_{\gamma}^{min} = \tanh \pi/2 \quad (3.8)$$

Hence, a conductor thickness of $t = 3\delta$, rather than $\pi\delta$, has less than a 1.2 percent higher sheet resistance. This is insignificant compared with changes in resistance due to process variations. For $t = 2\delta$ the increase is 20 percent, and having $t = \delta$ gives more than 40% increase in resistance. If $t >> \delta$, there is less than a 10 percent increase in calculated resistance above the optimum.

Proximity Effects

The current distribution and, hence, conductor impedance can be altered by a magnetic field generated by a conductor in close proximity. This situation may occur, for example, in the high current conductors in the output filter of a hybridized SMPS where ceramic capacitors bridge two conductors and bring the conductors into close proximity.

Burton [60] empirically investigated the proximity effects on two identical, parallel, rectangular conductors. He showed that the effects became significant when the facing edges were within a distance equal to three times the perimeter of one conductor. Furthermore, he proposed an equation that predicts the approximate increase in ohmic loss, λ, when the conductors move from infinite to zero separation, i.e., at the touching point

$$\lambda = 1 + \frac{t / w}{2 + t / w}$$

where t is the thickness and w is the width of the conductor.

For power hybrid circuits w is usually very large relative to t. If t/w > 1/20, then the worst case increase in ohmic loss with two conductors infinitesimally close will be less than three percent. This increase is negligible when the conductors are separated by a distance greater than 2w. Burton's results are empirical and include edge and corner effects. Therefore, the three percent represents the worst case error.

3.6 Selection of Conductor Width

Though total conductor resistance R in (3.6) can be reduced by using an optimum thickness Γ_{γ}^{min} (3.8), and by minimizing the resistance R_{δ}, i.e., from (3.4):

$$R_{\delta}^{min} = \zeta^{min}/2\sigma\delta \qquad (3.9)$$

where σ and δ are constants. The ζ^{min} is the minimum number of squares for a conductor. Theoretically, ζ^{min} can be zero indicating the conductor would have zero length or infinite width. However, the length of a conductor is never less than the spacing between two interconnected components. This spacing is determined from a consideration of thermal interactions of components, minimization of component stresses due to electric fields, safety standards, room for test probes, etc. The length is seldom zero and is usually beyond the control of the circuit designer. The width of a conductor,

however, is independently selected by a designer. It is then appropriate to select a ζ^{min} by determining a maximum width rather than a minimum length. The following develops an equation for determining the optimum width for a conductor.

Since, from (3.9), an infinite conductor width would give minimum resistance, an opposing expression of penalty for excessive width is needed. Note that excessive width in the conductor also implies excessive volume in the circuit. Therefore, a function to minimize the width and, hence, the volume is needed. One such expression, though not unique but adequate for this application, is for conductor volume, C, such that

$$C = M\ell wt \tag{3.10}$$

with M being a conversion or weighting factor with units of ohms per unit volume. Since conductor thickness is independently determined by (3.7), the penalty for increasing conductor volume occurs because of the increasing of conductor width. The penalty may be imposed because of increases in the circuit area (including substrate, heat sink and enclosure area) or because of increases in conductor resistance. Unfortunately, any selection process of width will require some subjective determination of M by the designer.

The optimum width is found by combining (3.9) and (3.10) into a function, F, such that

$$F = M\ell tw + \ell/2\sigma\delta w \qquad (3.11)$$

where w is constrained to $10\ t < w < \infty$ and M is independent of w, and then minimizing the resulting function. Since functions R_δ and C are monotonic, the minimum of F exists when its derivative with respect to w is zero. Hence,

$$0 = M\ell t - \ell/2\sigma\delta w^2 \qquad (3.12)$$

and the optimum width that minimizes the effects of R_δ and C, for an optimum thickness, $t = \pi\ \delta$, is

$$w = 1/\delta(2\pi\sigma M)^{1/2} \qquad (3.13)$$

Note that this equation, unfortunately, is not dependent on current density. Therefore, if the designer computes an optimum conductor width for one part of the circuit, the same width would be applied elsewhere. A proportioning factor, N, is introduced to make w dependent on the current, I, flowing through the conductor. The N may be thought of as a weighting of importance in minimizing R_δ at different current levels.

Inserting N into (3.11)

$$F = M\ell tw + N\ell/2\sigma\delta w \qquad (3.14)$$

and minimizing F as before gives

$$w = (N/2\pi\sigma M)^{1/2}/\delta \tag{3.15}$$

The N can have many forms. If it is desired that, for varying widths, the conductor have constant power dissipation, then

$$(N)^{1/2} = I^2_{norm}, \tag{3.16}$$

or for constant power density or constant voltage drop

$$(N)^{1/2} = I_{norm} \tag{3.17}$$

The I_{norm} is the per unit conductor current that has been normalized by a nominal current, I_o, which has been selected by the designer. The I_o is also used to compute the weighting factor M as discussed below.

As an example of this procedure consider a conductor design for a ZCS–QRC having a 32A pseudo–sinusodial current flowing at 2 MHz during full load operation. The conductors must then be sized to accommodate these currents. For a copper conductor system with a nominal current of 10A the following parameter values result.

$$N = 32A/10A = 3.2$$

$$\sigma = 0.6 \text{ X } 10^6 \text{ S/cm}$$

$$\delta = \text{skin depth} = 46\ \mu\text{m}$$

Using these values and a process value of M = 0.65 $m\Omega/mm^3$, which may have been determined by a manufacturer for his process, gives the optimum width of a conductor, from (3.15), as w = 2.5 mm.

This direct calculation of w by (3.15) was not used for the ZCS–QRC described in this dissertation since an empirical value for M could not be obtained from the low circuit volume occurring in the laboratory. In the final circuit the conductors widths were printed as wide as possible to provide the lowest resistance. The conductor widths were constrained either by physical circuits widths dictated by components size or by electrical safety requirements (which are discussed in Chapter 5). The use of a value for M that is nearly an order of magnitude less than for the example above would still be within reason for the thick printing process which was developed for the ZCS–QRC.

3.7 Summary

Since the focus of this research was the design and development of a converter, only suitable materials rather than optimal materials were required. Therefore, a qualitative evaluation of possible material systems was performed and a silver conductor system on alumina was selected. Two

silver systems from each of three manufacturers (see Table 3.1) were evaluated to determine which had a conductor material with the lowest relative resistivity. The DuPont 6160 conductor system was selected. The actual resistivity was measured and found to be 1.72 microhm–cm on average. This information is used in the final circuit design.

Testing was conducted to determine if silver migration would be a problem during circuit development. It was found that no migration occurred with electric field intensities as high as 2 kV/mm, with and without the use of an encapsulant. This conclusion allowed the separation of conductors and components to be determined by other factors such as safety criteria or thermal interactions.

Since the converter under development would operate at frequencies in the megahertz range, the ac resistance of the conductors was considered. It was found that the total conductor resistance was dependent on both frequency and thickness and is described be (3.3a). From (3.3a) it was concluded that a conductor of thickness pi times the skin depth of current in the conductor would have minimum resistance; however, such a thickness may be unachievable by the hybrid process and (3.3a) would be used just for calculations.

TABLE 3.1 Conductor Resistivities

Manufacturer	Material	Resistivity (mΩ - mil)	
		@25°C	dr/dt(°C^{-1})
DuPont	6160(Ag)	0.89	3.4×10^{-3}
	6134(Pd-Ag)	12.4	9.1×10^{-3}
Electro Science Laboratories	9562(Pd-Ag)	2.25	4.5×10^{-3}
	9601(Pd-Ag)	1.84	4.1×10^{-3}
Ferro	3424(Pd-Ag)	2.44	4.9×10^{-3}
	3754(Pt-Ag)	——	7.8×10^{-3}

TABLE 3.2 Thick-Conductor Resistivities

Sample No.	Resistance (mΩ)	Conductor Thickness (μm)	Resistivity (mΩ/sq)	Resistivity (μΩ·cm)
4	85	59.9	.702	1.78
8	112	41.1	.636	1.61
9	107	41.1	.622	1.58
10	115	40.6	.645	1.64
11	130	43.9	.788	2.01
		Average:	.679	1.72

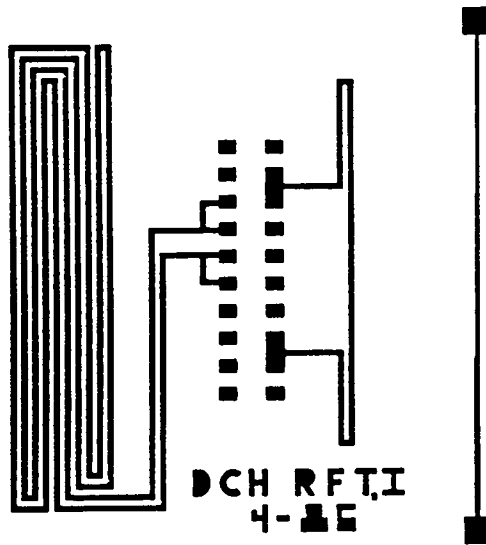

Fig. 3.1 Test pattern developed for material selection of conductor inks.

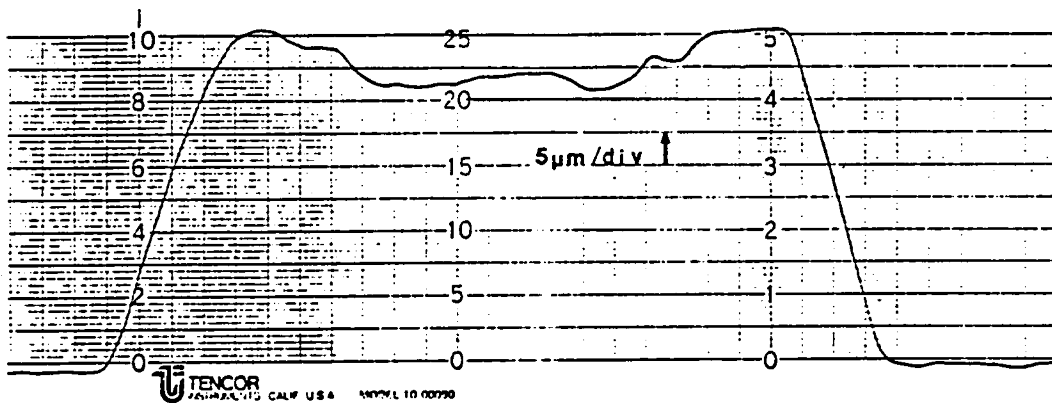

Fig. 3.2 Typical thickness profile of a fired conductor showing the conductor cross section.

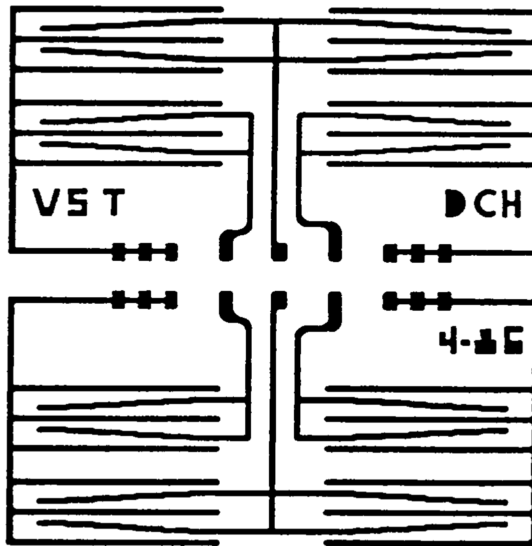

Fig. 3.3 Test pattern developed for testing silver migration at varied electric–field intensities.

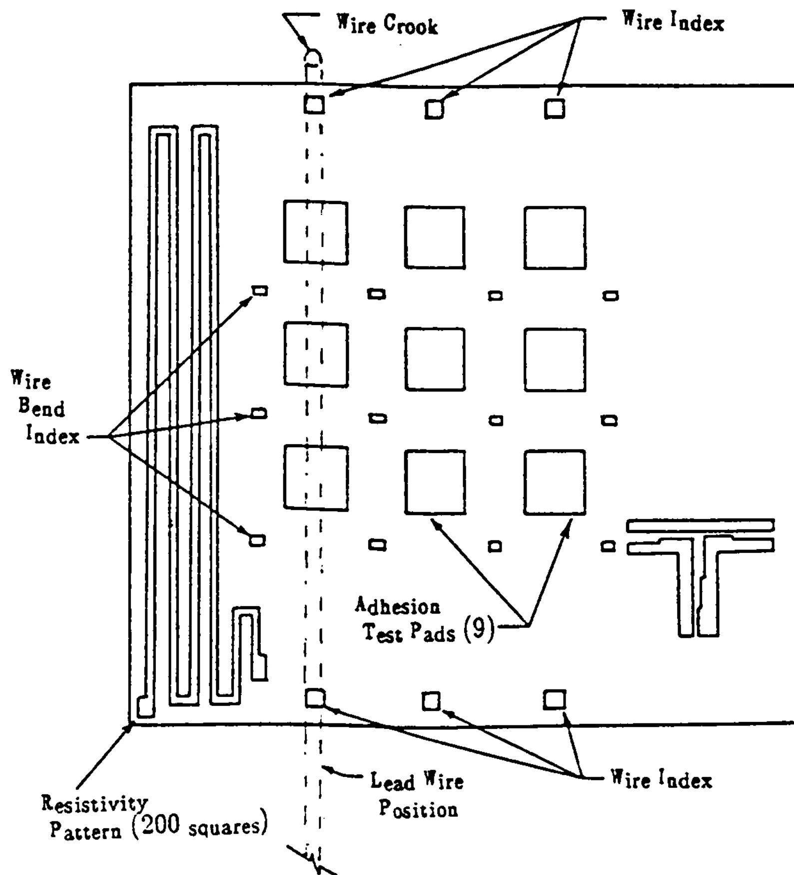

Fig. 3.4 Test pattern for determing adhesion and resolution.

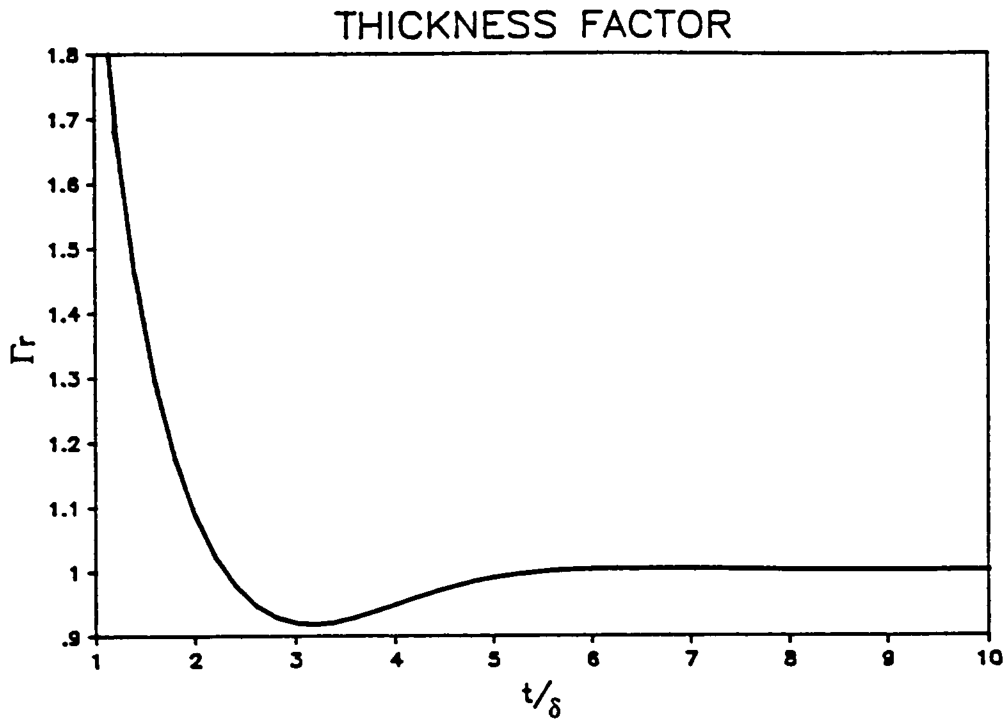

Fig. 3.5 Variation of resistance factor due to Γ_r.

CHAPTER 4

PROCESS DEVELOPMENT

4.1 Introduction

During the past half decade, circuit operating frequencies of switchmode supplies have risen to such high levels that circuit packaging is becoming an integral part of the circuit design. The dependence of design on packaging is a situation that already exists in the communications industry where surface mounting of components on ceramic substrates has produced high–frequency, high–density circuits. If the circuits dissipate greater than a few watts then power hybridization is used for circuit fabrication.

Certain operating characteristics of power supply circuits are not the same as with communication circuits such as currents of tens of amps and voltages of hundreds of volts. These characteristics determine the type of power hybridization.

A power hybrid has been used for many years for the packaging of discrete power semiconductors. It was not the high frequency capability, but thermal management, which was desirable from hybridization. However, due to higher device switching speeds, such as those occurring in MOSFETs, the high frequency capability is now important. This power hybridization technique has been developed to provide high current interconnects of hundreds of amps and packaging of devices to operate up to 1500 V.

Looking at what hybrid circuit fabrication techniques have done for communications circuits which operate at high frequencies and discrete devices which have high electrical stresses, it appears that the general application of power hybridization to switchmode supplies is very suitable.

Methods Of Circuit Fabrication

There are three conventional methods used to form a hybrid circuit. The first method deposits and etches thin films of oxides and metals. This thin–film process is not used for power hybridization except in military microwave applications. This method uses a batch process that is considerably more expensive than the other methods to be discussed.

The second method uses thick conductive, dielectric or resistive pastes that are sintered to form capacitors, conductors and resistors. This thick–film process is suitable for supplies, but is limited because of conductor thickness ($<50\ \mu m$).

The third process, that of copper–on–ceramic, forms conductor patterns by cladding or plating copper onto a ceramic substrate. It cannot create capacitors or resistors, but only interconnects. This method is also suitable for power supplies of limited complexity.

Over the past several years another circuit fabrication technique has been developed for surface mounting components on a printed wiring board (PWB). Unlike conventional PWBs the leads of packaged components are

attached to surface conductors rather than plated through holes. This method, which uses surface mount technology (SMT) [2], is very similar to copper–on–ceramic. Instead of using a ceramic substrate, materials such as epoxy–glass are used. Because the SMT boards (substrates) have relatively poor thermal conductivities and high coefficients of expansion, only packaged power devices are used. If devices need heat sinking, they are mounted to have a separate heat sink attached. The SMT process provides very good high–density packaging of control and monitoring circuitry. The use of SMT and hybrid circuits (if a distinction can be made) should be considered during the partitioning and initial design of a power supply system.

SMT boards with laminated construction (such as copper–invar–copper) provide good thermal conductivity and tailored coefficients of expansion. These boards, however, are rather expensive and do not offer the high–voltage isolation of ceramic.

4.2 Process Development

The standard thick–film silver process produces a conductor thickness of approximately 17 μm (0.67 mil). For the final circuit layout of the ZCS–QRC, a single 17 μm thick conductor that could carry the required 20A to 32A would need to be over 19 mm (746 mils) wide. Two output conductors would then occupy over half the substrate width.

A technique is described in the following sections for printing conductors 50 microns (2 mils) thick in one print cycle. The technique uses high silver content paste (DuP 6160) and achieves a resolution better than 175 microns (7 mils) with adhesion better than 21 N. A method for printing thick conductors wider than 1.5 mm (60 mils), but using two print cycles, is also described.

During development of the technique, 0.25 mm (10 mils) of wet thickness was found to be the limit for printing and firing. Above this limit the conductors lose adequate adhesion. However, this may vary depending on the type of drying and firing method used, e.g., infrared.

Electrical tests on the thick–printed conductors showed an average resistivity of 1.72 $\mu\Omega$–cm (0.68 mΩ/sq). An example power hybrid substrate had an absolute sheet resistivity of 0.34 mΩ/sq. at an average thickness of 50 microns (2 mils).

Conductor adhesion, component solder attachment and wire bondability were excellent. Dielectrics and overglazes, which are designed for thick printing, remained compatible with thick conductors. A technique was also developed for thick printing over very wide areas.

4.3 Parameters Affecting Fabrication

Three factors significantly affect the thickness of printed conductors during fabrication. They are: paste composition, including the amount of binder and the viscosity; printer setup, specifically screen snap off, squeegee

speed and pressure; and processing, specifically drying profile and peak firing temperature.

Paste Composition

The paste composition has much to do with the final resolution and adhesion of the fired conductor. Since thick conductors are printed to wet thicknesses exceeding 175 microns, a considerable amount of printing vehicle and binding agent can be present at the conductor surface and conductor–substrate interface. Too much vehicle and binder can cause flow out during drying and firing because of the large internal lateral pressure occurring in the conductor during the densification.

Since low resistivity conductors are needed, the paste should have a high metal content. Reported here are results using DuPont 6160 Ag conductor paste which is a mixed bonded system having a low binder concentration. The fired concentration is approximately one percent glass and one percent oxide. This low binder concentration helps abate any flow out during firing.

It was found from repeated printing failures that the paste viscosity was too low for thick printing. A paste with low viscosity makes it difficult to achieve thick wet prints that retain good resolution during printing and drying. The high static pressure in the wet print can expand the sidewalls of the print causing poor definition. The viscosity of the paste was modified as described later.

Printing

In his assessment of the ink transfer process in screen printing, Reimer [61] quantitatively showed the importance of snap off. For a conventional patterned screen, where the emulsion fills the entire screen fabric, a sufficient snap off distance is needed to avoid a "cling zone." This occurs when the fabric behind the squeegee, as the squeegee is printing, clings to the substrate. In this cling zone, the thixotropic paste will linger and increase in viscosity making it more difficult to be cleared from the fabric. A qualitative assessment of ink flow during thick printing is given below which should explain the occurrence of a large cling zone and the need for an ever larger snap off distance than used when printing inks for conventional thicknesses.

This thick–printing technique uses a screen that has a significant build up of emulsion on the print side as shown in Fig. 4.1. The amount may equal or exceed the thickness of the mesh fabric. The passage of ink through the mesh during the printing process can be qualitatively viewed as a combined process of stenciling and screen printing.

Similar to stenciling, paste will be cleared from any open area in the lower portion of the patterned screen, Area B Fig. 4.1, only when forces due to sidewall adhesion which are normal to the substrate are less than either the force causing separation of the paste in the open area or the adhesive forces of the paste at the substrate surface. This last condition directly affects the cling zone.

Similar to screen printing, to clear paste from any open area in the upper portion of the patterned screen, Area A in Fig. 4.1, two characteristics of the paste and screen movement must be considered. As paste is sheered through the screen fabric in Area A its viscosity decreases and fills Area B between the fabric and substrate. The viscosity profile within Area A, however, is not uniform and the paste at the squeegee–fabric interface will be more viscous than that in all of Area B since it has not experienced sheering by the fabric. This indicates that it will be more difficult to clear the higher viscosity paste from the fabric mesh in Area A than from the fabric–to–substrate area, Area B. To clear paste from Area A, forces acting on the paste within the fabric and essentially normal to the substrate must be greater than the forces exerted by the mesh as it is moving through the paste. This is, again, modeled by Reimer [61] and further refined by Huner [62]. However, in these references, the removal of paste is modeled as a hydraulic action that occurs within the fabric as it is lined from the substrate. For thick printing, the hydraulic action within the fabric differs in that it occurs as the fabric lifts from the lower viscosity paste in Area B. Paste removal from the fabric then requires that the force exerted on the paste within the fabric mesh, as the mesh is snapping off, be less than the separation force of the paste in Area B.

The force exerted on the paste within the fabric can be reduced if the snap off velocity of the fabric is reduced by decreasing the snap off distance

and slowing the squeegee speed. Unfortunately, the reduction in squeegee speed also reduces the sheer force on the paste which is being pushed through Area A into Area B and lessens the decrease in paste viscosity. The effect of reducing the snap off is verified by Reimer [61].

Unfortunately, there are undesirable effects occurring with decreased snap off. An important parameter for achieving suitable printing, as discussed earlier, is the reduction of the cling zone. Increasing snap off decreases this zone. In thick printing, the large surface area of the sidewalls of the patterned emulsion, Area B Fig. 4.1, will cause a large force normal to the substrate to be exerted on the screen mesh. This, in addition to the forces caused by hydraulics [61], must be countered by the tension of the mesh. Hence the clearing force can be increased by increasing snap off.

The optimum printing conditions for thick printing can then be approached by using an increased snap off distance and a slow squeegee speed. This is in keeping with the empirical observation.

Processing

With wet–print thickness exceeding 175 microns (7 mils), the drying profile has much to do with the final print resolution and success in firing. Rapid drying causes the outer surface of the wet print to harden and to slow further drying of the inner portion of the print [63]. A drying profile is then needed which is different and usually longer than conventional drying cycles.

It is also important to consider the method of drying. If infrared is used with a material having a high absorption, such as copper, then the drying cycle can be shorter than, for example, silver using convection drying.

Another factor affecting the success of thick printing is the firing profile. The profile must have adjusted rates of temperature rise and peak firing temperature suitable to allow for complete sintering and removal of organics. The peak firing temperature is critical to obtaining good resolution and adhesion. With higher peak temperatures, there is a greater densification of the metal solids and a greater accumulation of binder at the print surfaces. The greater densification is desirable since it reduces conductor resistivity.

4.4 Thick Printing Process

This section describes the test pattern and fabrication process for achieving thick thick–film conductors. The results show that a fired thickness of 42 microns (1.7 mil) for a large area and 50 microns (2 mil) for a narrow line were achieved with a single print–dry–fire cycle. Minimum adhesion for the conductors was 21N and resolution of line separation greater than 125 microns (5 mils) was achieved.

Test Pattern

The test pattern shown in Fig. 4.2 is described in the publication, "Method of Test for Wire Peel Adhesion of Soldered Thick Film Conductors

to Ceramic Substrates," A–74672, by E.I. DuPont De Nemours and Co., Electronics Division. Three sections of the pattern allow for four tests to be performed. The serpentine pattern provides approximately 200 squares of conductor material to be used for dc resistance measurement. The rectangular 2 mm x 2 mm (80 mils x 80 mils) pads are used to measure the thickness of "wide conductors". The pads are also used for adhesion measurements. The lower right "T" pattern is used for measuring the resolution of the print. In the "T" pattern the narrowest spacing between conductors is at the upper right with 105 microns (4.1 mils). The spacings at the left and bottom, are approximately 175 microns (6.9 mils). Of main interest is the 105 micron pattern.

Using the serpentine pattern an accurate resistivity measurement can be made only if the number of squares and the cross–sectional area of the conductors can be accurately determined. For the actual printed pattern as shown in Fig. 4.3 it was determined from profiling that the conductor base width was 440 microns (17.3 mils); therefore, the pattern has 231 squares. A correction factor for the conductor area was also determined since the sides of the conductors sloped at approximately 35 degrees. The total conductor cross section for peak thicknesses between 40 microns and 60 microns can be calculated from

$$A_c = T_p \times W_b \times 0.81 \qquad (4.1)$$

where T_p is conductor thickness (thickness variation within the top 15% is averaged);

W_b is conductor width at the base

The measurement of resistivity for thick conductors can be relatively accurate because the top–surface profile variation is small compared to the overall thickness. It was observed that the profile variation was limited to 15% of the thickness. By using the 35 degree approximation in the surface variation the resistivity can be determined to within 10%.

Because of the close proximity of adjacent conductor and narrow end radii, meaningful measurement of the ac resistance cannot be made.

Paste Preparation

The paste viscosity listed by the manufacturer is between 85 to 115 Pa–s. This viscosity is too low to achieve good columniation of the conductor during printing causing loss of resolution, particularly, during initial drying. Paste viscosity was, therefore, altered.

Two methods of drying were explored. The first method used a vacuum system to lower the ambient pressure of the paste. In vacuum, the printing solvents with low partial pressures are extracted. However, two difficulties precluded this method. The roughing pump in the vacuum system became severely loaded when gases were liberated. Also, during evacuation, the paste temperature decreased making the solvents, at lower partial pressures, harder to extract.

An alternative procedure for drying paste is heating to dispel solvents. This is less desirable because of the higher probability of oxidation and contamination. However, this procedure was adopted and great precaution was taken to prevent contamination. The paste was heated slowly on a hot plate for 10 minutes to just below 100°C and continually stirred. The increased viscosity was 215 Pa–s as measured with a Brookfield HBF Viscometer [64] with an SC4–14/6R spindle and water cooled chamber at 10 rpm and 25°C $\pm$ 1°C. There was a measured change of approximately 10 Pa–s/°C. (which should also be considered during printing).

Other paste samples were dried to 165 Pa–s, 285 Pa–s and 414 Pa–s. It was empirically determined from successive attempts at printing with different pastes that viscosities of 200 to 225 are preferred.

Printing and Processing

It was empirically determined that to attain pattern thicknesses of approximately 50 microns (2 mils) with good resolution the optimum range of printer settings for patterns using 5 in. by 5 in. screens are: a snap–off distance between 1.0 mm (40 mils) and 1.3 mm (50 mils); squeegee speed between 14 mm/s and 28 mm/s; and an attack angle between 39° and 45° (40° preferred). A 60 durometer squeegee was used. Pressure was the independent adjustment. (There was no provision in the equipment for measurement of pressure.) Screens were prepared using Ulano Incorporated CDF–7 direct film emulsion resulting in a total thickness of 155 microns

(6.1 mils) of emulsion (including fabric thickness) on 230 count mesh. The emulsion was applied using Ulano's prescribed techniques.

Patterns were printed on 96% alumina substrates with a single printing pass. The substrates settled for a minimum of 10 minutes at room temperature and a minimum of 20 minutes each at 75°C and 150°C. Substrates were then fired with a 900°C, 60 minute profile in a four zone convection furnace.

4.5 Printing Results

Shown in Table 4.1 are results for 11 selected test substrates. The two key parameters, forward squeegee speed and snap off, which were discussed in the previous section, are given along with the acceptance (e.g. reject, good, very good). Acceptance was determined by visual evaluation of print quality and resolution. All rejects had loss of resolution and smudging in the "T" pattern. Dried and fired thicknesses are tabulated as averaged data. The narrow trace data represent an average of twelve measurements taken across the 500 microns (20 mils) wide traces of the serpentine pattern shown in Fig. 4.2. The measurements varied in fired thicknesses from 60 microns (2.4 mils) to 41 microns (1.6 mils). The center thicknesses of the large–area conductor pads which are 2 mm (80 mils) square vary from 32.3 microns (1.27 mils) to 35.6 microns (1.40 mils).

The substrates that were not acceptable had poor resolution and were processed with printer settings outside the ranges mentioned in the previous section. Samples 1 and 2 had low squeegee speeds and inadequate snap off distance. Sample 3 had excessive speed. Samples 10 and 11 had adequate speed and snap off but lower squeegee pressure than the other samples. (The pressure is not listed.)

All the acceptable substrates have printed patterns resolved to better than 175 microns (7 mils). The "Very Good" substrates resolved better than 127 microns (5 mils). A printed test pattern with very good resolution is shown in Fig. 4.3.

Adhesion

To conclude the development of the thick–printing technique, adhesion testing was conducted using the "Method of Test for Wire Peel Adhesion of Soldered Thick Film Conductors to Ceramic Substrates," A–74672, by E.I. DuPont De Nemours and Co., Electronic Division. Three modes of failure exist. The first mode is due to solder adhesion failure when the test wire which is soldered to a test pad lifts from the solder leaving the pad intact. This yields inclusive results; three substrates fell into this category.

The second mode of failure is the internal fracture and separation of the pad. The third mode is separation at the conductor–substrate interface where the pad lifts from the substrate. These latter two modes test the

adhesiveness of the paste directly. The physical fracture and separation failures were all typical for these types of tests. The tests were conducted on an Instron Incorporated instrument. The failure distributions are graphically presented in Fig. 4.4 for paste and interface failures, respectively. All the tension forces are above the minimum acceptable, particularly the interface failures. These tests were conducted after 2300 hours of room temperature and very low humidity aging.

4.6 Electrical Characteristics

The serpentine pattern on the test substrates was used for the measurement of the conductor resistance. Five substrates were measured and the results and computed resistivities are shown in Table 4.2. The conductor thicknesses as given in Table 4.1 are used and an equivalent conductor cross–sectional area is computed using (4.1) with a measured base width of 440 microns (17.3 mils). The conductor resistivity is then

$$R = R_{dc} \times T_p \times 3.50 \times 10^{-3} \qquad (4.2)$$

where R_{dc} is the dc measured resistance of the serpentine trace

T_p is the conductor thickness.

The 1.72$\mu\Omega$–cm (0.68$m\Omega$/sq.) average resistivity is quite close to pure silver which is 1.59$\mu\Omega$–cm. Measurement of ac resistance was not possible because of proximity effects induced within the pattern.

Other processed substrates using lower firing temperature profiles were nearly 30% higher in resistivity. It is generally thought that higher firing temperatures cause a higher densification to occur and, hence, lower resistivity results [65]. This appears true for the thick–printed silver conductors processed here.

4.7 Wide Conductor Printing

When conductor widths exceed approximately 1.5 mm (60 mils) the printing of a thick conductor with a uniformly thick cross section becomes very difficult. The difficulty arises because of the large deflection of the screen in the center of a wide pattern. Consequently, at the edges of the pattern where thick emulsion suspends the screen from the substrate, a thick deposit of conductor paste occurs. In the center only deposits resulting from the thickness of the screen mesh are left.

A method to print wide thick conductors has been developed which uses pillars to support the screen in the center area of a wide pattern. The method is as follows. Referring to Fig. 4.5, pillars are placed symmetrically throughout the inner area of a wide pattern at distances no further than 1.5 mm (60 mils) from each other or from the sides of the wide pattern.

Different pillar shapes, such as rectangular, can be used. Regardless, one or more horizontal dimensions of the pillar should not exceed 1.5 mm (60 mils), otherwise the pillar itself may not have uniform thickness.

After the pillars are printed, dried, and depending on conductor thickness, fired, the entire wide pattern is then printed over the pillars, as shown schematically in Fig. 4.5. The edge definition of the wide pattern is retained since the pillars are placed away from the edges. The fabrication cycle is completed by drying and firing.

The following equations are used to determine emulsion thickness for the screens and are derived from the wet thickness equations used for stencil systems [66]. Assume the same screen mesh is used for both. If the pillars are printed, dried, and fired, then the thickness of the emulsion build–up for the printing of pillars is

$$\mathrm{Te_x} = \mathrm{Tp}/\delta^2 - \mathrm{T}m\,\mathrm{A}(1+\delta)/\delta \qquad (4.3)$$

where Tp is the desired fired thickness of pattern;

δ is the decimal equivalent percentage of the reduction from wet to fired;

Tm is the mesh thickness;

A is the decimal equivalent percentage of open area.

The thickness of the emulsion build up for printing the pattern is

$$Te_p = Tm\,A(1 + \delta)\delta + Te_x\delta \qquad (4.4)$$

It may be advantageous not to fire the pillars but to use their height after drying to support the screen. The emulsion build–ups then are

$$Te_x = Tp/\delta_d\delta_f - Tm\,A(1 + \delta_d)/\delta_d \qquad (4.5)$$

and

$$Te_p = Tp/\delta_f - Tm\,A\,\delta_d \qquad (4.6)$$

where δ_d is reduction from wet to dry and
δ_f is reduction from wet to fired.

During the development of the thick printing process it was determined that the cofiring of dried pillars which were layered by the dried pattern and having a combined dried thickness above approximately 200 microns (8 mils) caused a loss of adhesion of the pillars. However, the method of firing the pillars first was successful in providing the thickest fired patterns. This became the limit to cofiring thick thick–film conductors.

Shown if Fig. 4.6 is the thick printed substrate for the ZCS–QRC. The overall substrate dimensions are 5.8 cm (2.3 in.) by 4.3 cm (1.7 in.). The

pillars, which are shown on the right, create a thick layer sufficient to conduct thirty–two amperes. The fired pillar thickness is approximately 60 microns (2.4 mils) and thickness between pillars is approximately 40 microns (1.6 mils). The absolute sheet resistance for the average thickness is $0.34 m\Omega$/sq.

4.8 SUMMARY

A technique is described for printing conductors 50 microns (2 mils) thick in one print cycle. The technique uses high silver content paste (DuPont 6160) and achieves a resolution better than 175 microns (7 mils) with adhesion better than 21N. A method for printing thick conductors wider than 1.5 mm (60 mils) but using two print cycles is also described.

During development of the technique 0.25 mm (10 mils) of wet thickness was found to be the limit for printing and firing. Above this limit the conductors lose adequate adhesion. However, this may vary depending on the type of drying and firing method used, e.g. infrared.

The electrical tests on the thick–printed conductors showed an average resistivity of $1.72 \mu\Omega$–cm ($0.68 m\Omega$/sq). An example power hybrid substrate had an absolute sheet resistivity of 0.34 $m\Omega$/sq. at an average thickness of 50 microns (2 mils).

TABLE 4.1

Fired Thickness for Selected Substrates

Sample No.		Forward Speed mm/s	Snap Off mm	Dried Thickness: Narrow Trace µm (mils)	Dried Thickness: Center of Pad µm (mils)	Fired Thickness: Narrow Trace µm (mils)	Fired Thickness: Center of Pad µm (mils)
1	Reject	13	1.0	64 (2.5)	67 (2.6)	29 (1.2)	29 (1.1)
2	Reject	13	1.3	68 (2.7)	65 (2.6)	41 (1.6)	40 (1.6)
3	Reject	43	1.4	82 (3.2)	77 (3.0)	56 (2.2)	53 (2.1)
4	Good	29	1.4	89 (3.5)	68 (2.7)	60 (2.4)	41 (1.6)
5	Good	29	1.4	90 (3.5)	70 (2.8)	58 (2.3)	42 (1.7)
6	V. Good	15	1.4	84 (3.3)	73 (2.9)	57 (2.9)	41 (1.6)
7	V. Good	15	1.4	66 (2.6)	65 (2.6)	41 (1.6)	31 (1.5)
8	V. Good	15	1.1	68 (2.7)	62 (2.4)	41 (1.6)	36 (1.4)
9	V. Good	15	1.1	68 (2.7)	64 (2.5)	42 (1.7)	36 (1.4)
10	Reject	15	1.1	66 (2.6)	66 (2.6)	41 (1.6)	37 (1.5)
11	Reject	15	1.1	69 (2.7)	65 (2.6)	44 (1.7)	38 (1.5)

TABLE 4.2

Conductor Resistance

Sample No.	Resistance (mΩ)	Conductor Thickness (μm)	Resistivity (mΩ/sq)	(μΩ·cm)
4	85	59.9	.702	1.78
8	112	41.1	.636	1.61
9	107	41.1	.622	1.58
10	115	40.6	.645	1.64
11	130	43.9	.788	2.01
		Average	.679	1.72

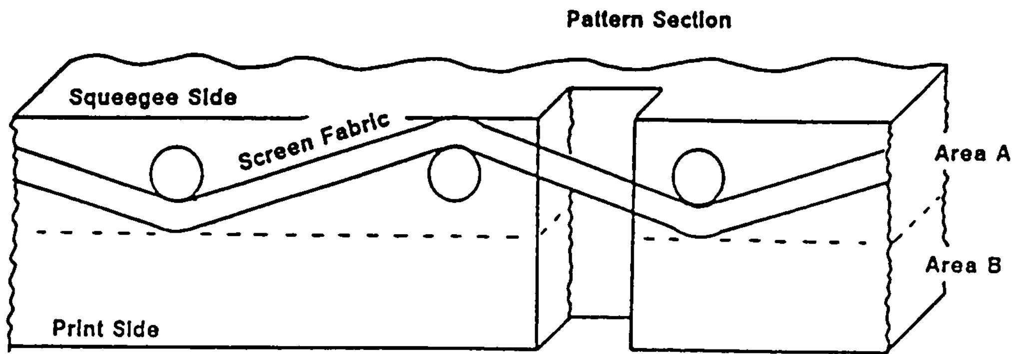

Fig. 4.1 Cross section of screen and emulsion. The thick build up is needed for thick printing.

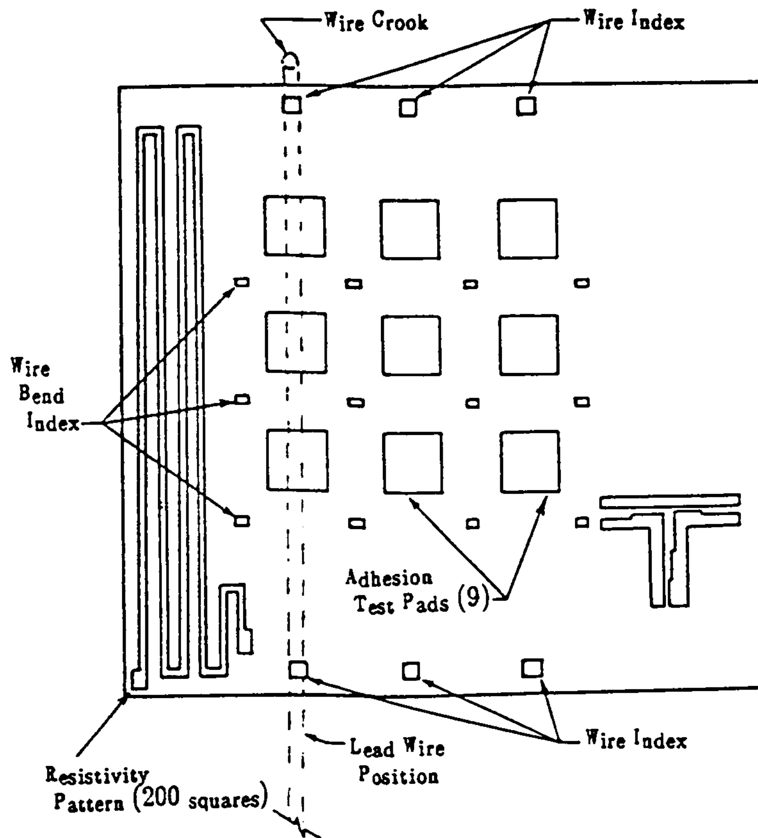

Fig. 4.2 Test pattern for measurement of resistivity (serpentine pattern), adhesion (square pads) and resolution ("T" pattern).

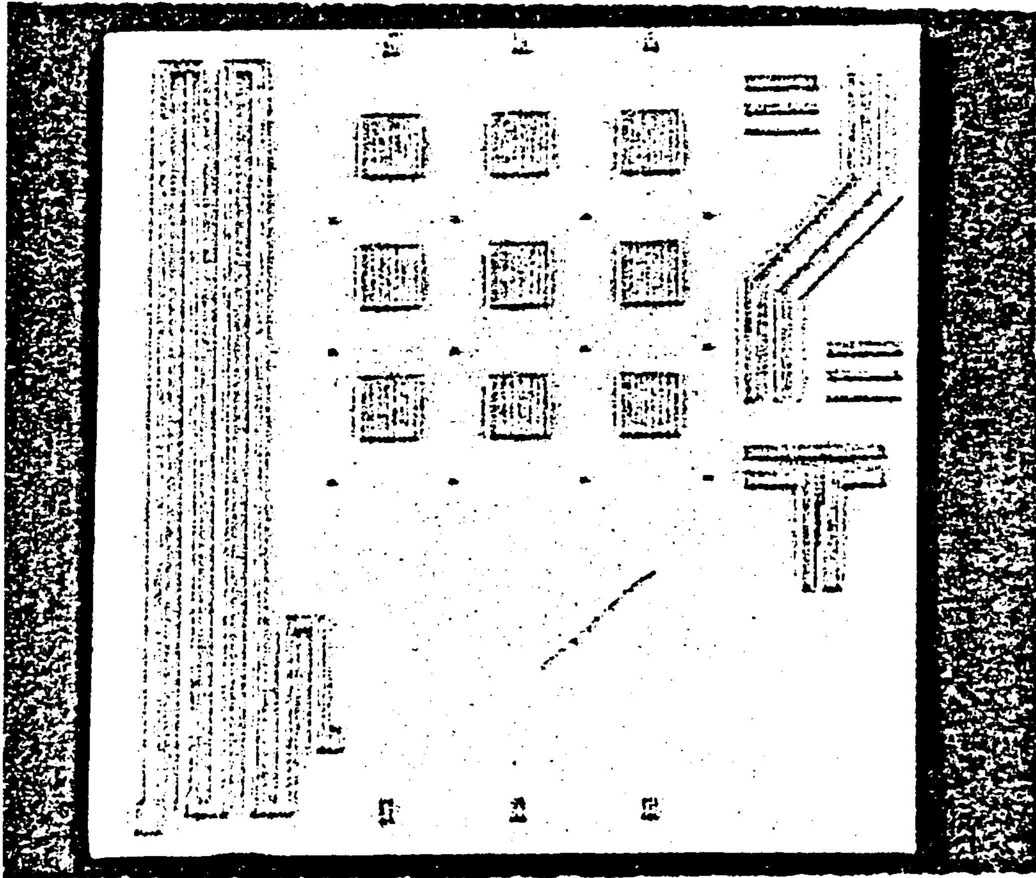

Fig. 4.3 Fired test pattern with conductor thickness greater than 50 μm (2 mils) and resolution better than 175 μm (7 mils).

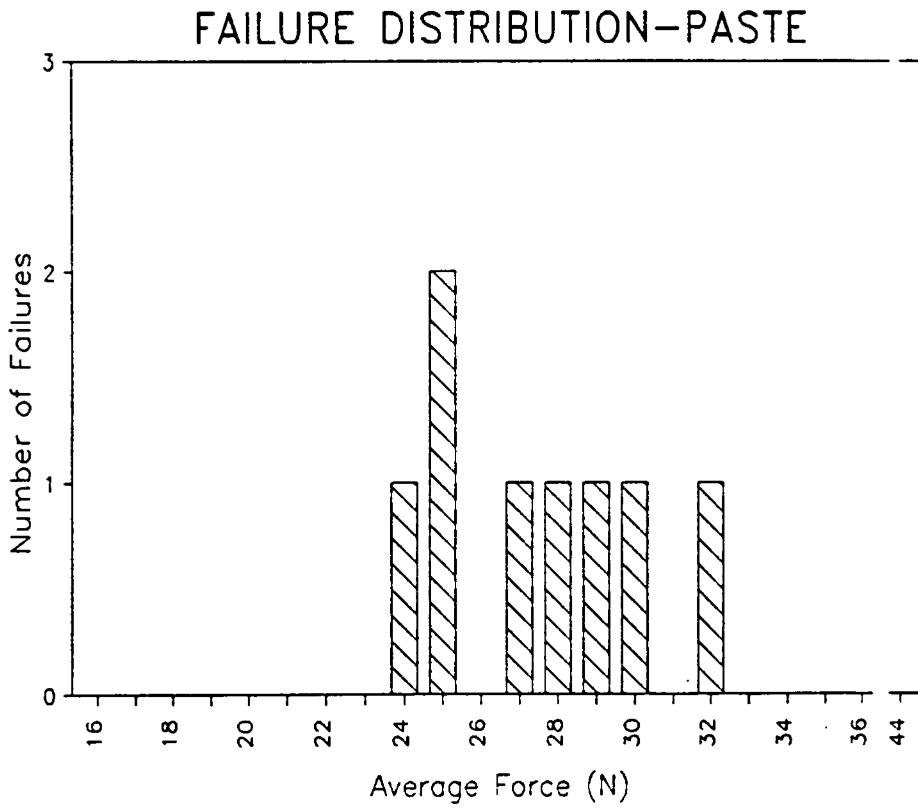

Fig. 4.4a Distribution of adhesion failures caused by internal fracturing of the conductor. Tests were performed after 2300 hours of storage at room temperature and low humidity.

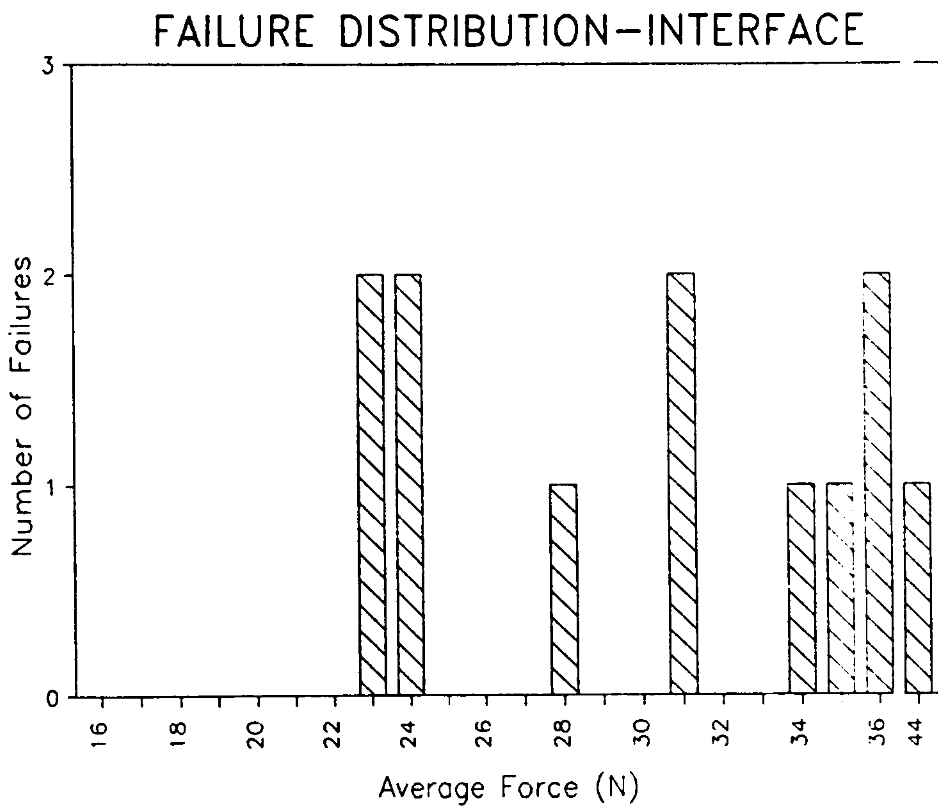

Fig. 4.4b Distribution of adhesion failures caused by separation of the conductor from the substrate. Tests were performed after 2300 hours of storage at room temperature and low humidity.

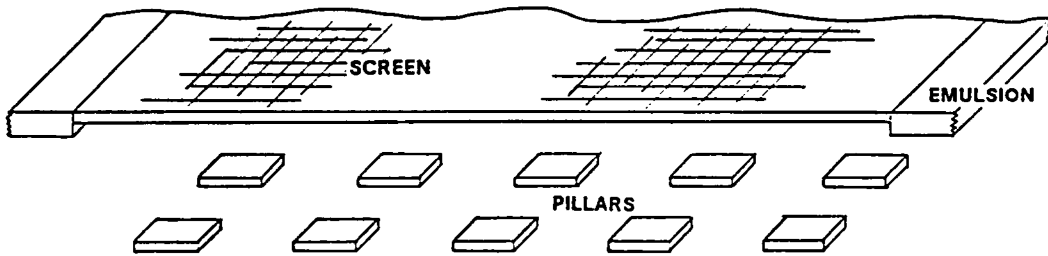

Fig. 4.5 Illustration of patterned screen ready to be placed over pillars. The pillars support the center of the screen while the screen emulsion defines the thickness and resolution of the edge pattern.

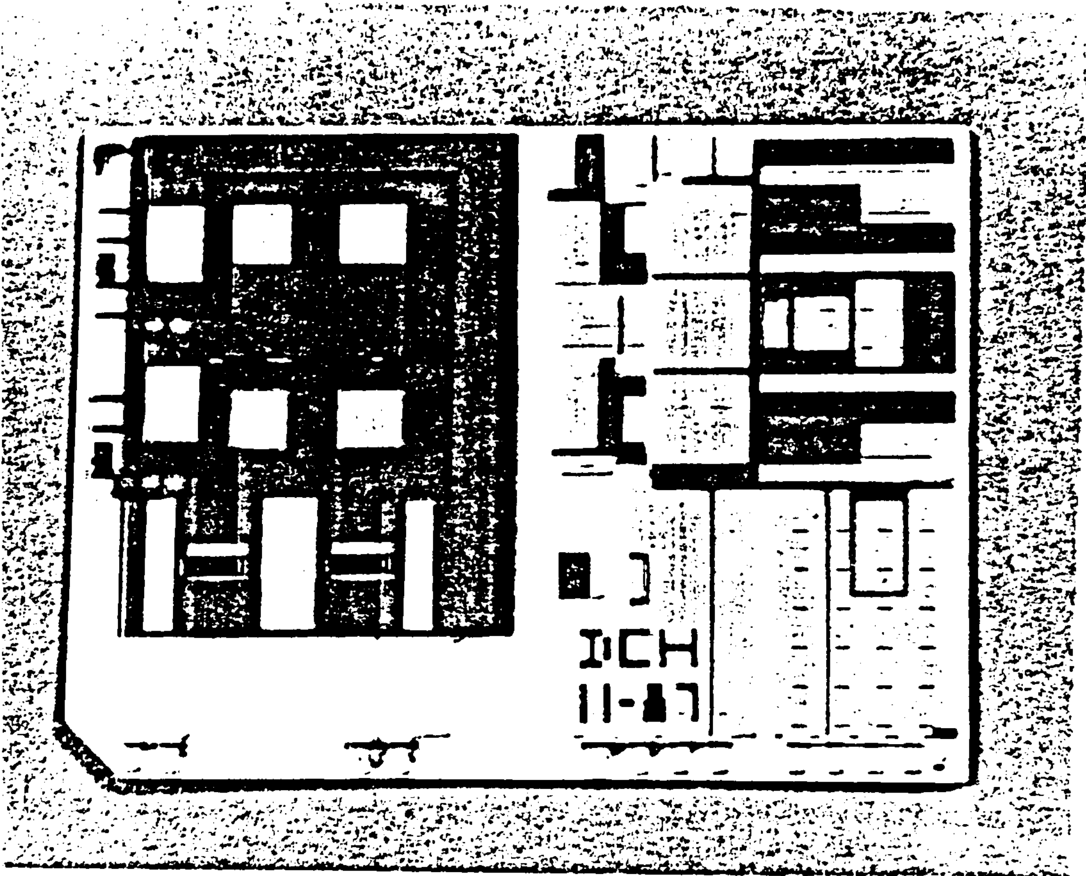

Fig. 4.6 Example circuit substrate for a 100 W, 2 MHz switchmode power supply. The right side was printed using pillars and bars to support the wide pattern. An absolute sheet resistance of 0.34 mΩ/sq. resulted.

CHAPTER 5

DESIGN, FABRICATION AND TESTING OF THE ZCS–QRC

5.1 Introduction

This chapter finalizes the development of the ZCS–QRC. Analysis and design equations were developed in Chapter 2, materials used to fabricate the circuit were evaluated and selected in Chapter 3, and a fabrication process which was developed is given in Chapter 4. What remains is to combine the design equations, materials and fabrication process to design a specific ZCS–QRC which will have the highest density and efficiency.

5.2 Circuit Design

A precursor to the circuit is the determination of design requirements which are shown in Table 5.1. Most of these parameters can be considered typical for a 100W off–line ZCS–QRC and were recommended by the research sponsor. The parameter L_r is the minimum available from the transformer structure that was used during the development. As discussed in Chapter 2 it is desirable to have this value be as low as possible. The lower the L_r the higher the resonant frequency and, consequently, higher the operating frequency. This provides for smaller components and higher density. Also, decreasing L_r decreases the resonant output impedance and provides operation at higher loads. More detail regarding the design trade offs are provided in [68] and [70].

Specific component values for the ZCS–QRC can now be calculated from equations developed in Chapter 2 and Appendix A. Table 5.2 lists the name, equation numbers in parentheses, label and calculated value for circuit components. The specific components selected from these values are listed in Table 5.3 along with details of the transformer that was used.

Also listed in Table 5.2 are critical design parameters which were discussed in detail in Section 2.3. The current parameters are used to determine conductor design, the voltage parameters are used to determine conductor spacing and both parameters to determine power losses.

The conductor fabrication is given in detail in Sections 4.5 and 4.7. The conductor width was not optimized using the technique discussed in Section 3.6, but rather was made as wide as possible to have minimum resistance. The conductor widths were limited by overall component widths and safety requirements.

The conductor spacing or circuit layout is dominated by two criteria which apply respectively to the primary and secondary sides of the circuit. For the primary side, the layout is determined by safety design criteria because of the relatively high voltages (up to 350 V) that are present. The secondary–side layout is determined by component size and widths which are as wide as allowable. The safety criteria are given below and encompass UL and VDE requirements. (UL and VDE are U.S. and European associations, respectively, that set safety regulations for the design of electronic products. Since this research was in support of an industrial development, the safety criteria were incorporated in the design.)

Primary Circuit:

Primary to Primary–

Basic insulation,
uncoated but protected for 240 V:
Clearance 2 mm (79 mils)
Creepage 3 mm (118 mils)

Primary to Secondary–

Reinforced insulation,
uncoated for 340 V peak:
Clearance 8 mm (315 mils)
Creepage 8 mm (315 mils)

Primary to Secondary–

Reinforced insulation,
Coated for 373 V peak:
Clearance 2 mm (79 mils)
Creepage 2 mm (79 mils)

Secondary Circuit:

If < 43 V peak, coated or uncoated:
no requirement

If < 50 Vrms, coated:
no requirement

If > 43 V peak but < 85 V peak, uncoated:
Clearance .38 mm (15 mils)
Creepage 0.72 mm (28 mils)

The thickness of the coating material should not be less than 0.03 mm (1.2 mils). Also assumed in the layout design is the use of a dielectric coating which will cover all high–voltage, primary–circuit conductors, and that the

semiconductors and the primary circuit chip components will be coated with an elastomer. The fired conductor thickness averaged 50 microns (2 mils). The absolute sheet resistance of the printed output conductors for the HB ZCS–QRC is 0.34 $m\Omega$/square.

Shown in Figure 5.1 is the thick printed thick–film substrate. The left portion of the circuit is the primary side or high–voltage side. The right side is low voltage. Note the wide conductor prints on the right side for carrying currents in excess of 20A. The darker pattern is the DuP 5704 dielectric coating.

Except for the conductor processing discussed in detail in Chapter 4 the fabrication of the hybrid circuit followed typical traditional techniques. Mounting of components was done with silver 36/62/2 tin–lead–silver solder and 8 mil aluminum wire bonding. The power diodes were obtained from the manufacturer with molybdenum tabs attached. The manufacturer used 95/5 lead–indium solder to attach the tabs.

5.3 Thermal Analysis of Semiconductors

To assure long term reliability of the converter, the junction operating temperatures should not exceed 100°C for the transistors and 125°C for the Schottky diodes [72]. There are three factors affecting the temperature: the power loss within the device, the thermal impedance between the device and heatsink including any thermal interaction with surrounding components,

and the ambient temperature. To determine the junction temperatures, a two–dimensional, finite–difference analysis was performed on the transistors and diodes.

There are three forms of heat transfer considered in the ZCS–QRC: conduction (diffusion), convection and radiation. For an emissivity of 0.3, which is approximately the value for silver, alumina and silicon, the total radiated power loss at 100°C from the entire surface of the ZCS–QRC was calculated to be less than 2% of the total electrical energy lost by the ZCS–QRC. The 2% is insignificant when compared with uncertainties in the constants used in the calculations. Also, the neglecting of radiation loss provides for a worst case for cooling by conduction and convection. Radiation effects were neglected for the semiconductors.

The convective heat transfer is difficult to determine accurately because it depends on many material and environmental factors. Fortunately, the convective heat transfer is not the dominant part of the overall transfer process. The convective heat flow from a transistor in the ZCS–QRC was calculated to be less than 0.4% of the heat flowing from the entire structure. This was based on a 100°C difference between surface and ambient. Any convection from the sides of the transistor would be half this value and proportionately less by the ratio of the side area to surface area. The heat flow due to convection is assumed negligible and the convecting surfaces are

modelled as insulated surfaces. Similar calculations and conclusions are made for the ZCS–QRC diodes. The total heat flow in the ZCS–QRC is modelled only for conduction.

The numerical approach for finding the temperatures uses a two–dimensional grid of temperature nodes to define temperatures at descrete positions within a two–dimensional model of the ZCS–QRC structure. A two–dimensional model was selected because of its improved accuracy over a one–dimensional model, yet, not having extreme computational complexity as in a three–dimensional model. In the two–diminsional model heat flow is constrained to be in two dimensions by isolating the plane (front and back) in the third dimension. Disallowing heat flow in the third dimension causes the calculated temperature to be higher than actual. This approach is well documented in textbooks such as Holman [73].

A control volume is defined at each node, as shown in Fig. 5.2, and an energy balance for heat flow is imposed. Energy flowing into and generated within the control volume must be equal to the energy leaving. Fourier's equation, expressed as a finite difference, is used to describe the energy per unit time flowing in and out. The heat generated, q_G, internal to the control volume uses the volumetric heat–generation density, q''', i.e.

$$q_G = q''' \Delta x \Delta y \Delta z$$

Following are the heat flow equations and the resulting nodal temperature equations for two configurations of nodes. The first set of equations represent a configuration with heat flow in a uniform medium. The second set represents flow between two materials having dissimilar thermal conductivities which divide the control volume into North and South regions. For nonconvective, nonradiating and insulated nodes, the node temperature is set equal to the adjacent node, i.e., $T_{m,n} = T_{m,n+1}$. The nomenclature is given below (refer to Fig. 5.2).

Δx, Δy and Δz are the incremental distances [m]

k is the thermal conductivity of the material North, South, East or West relative to the figure position, [W/m/°C]

q is the heat flow from the North, South, East or West (relative to the figure position on the page) and Generated, [W]

q''' is the volumetric heat–generation density, [W/m³]

$T_{m,n}$ is the temperature of a node at row m and column n, [°C]

T_∞ is the temperature of the surrounding environment [°C]

Interior node with generation

$$q_N = -k\,\Delta x \Delta z \left[T_{m,n} - T_{m-1,n}\right]/\Delta y$$

$$q_S = -k\,\Delta x\Delta z\left[T_{m,n} - T_{m+1,n}\right]/\Delta y$$

$$q_E = -k\Delta y\Delta z\left[T_{m,n} - T_{m,n+1}\right]/\Delta x$$

$$q_W = -k\Delta y\Delta z\left[T_{m,n} - T_{m,n-1}\right]/\Delta x$$

$$q_G = q'''\Delta x\Delta y\Delta z$$

For $\Sigma q = 0$, the node equation for temperature is

$$T_{m,n} = \frac{\frac{\Delta x}{\Delta y}\left[T_{m-1,n} + T_{m+1,n}\right] + \frac{\Delta y}{\Delta x}\left[T_{m,n+1} + T_{m,n-1}\right] + \frac{q'''\Delta x\Delta y}{k}}{2\left[\frac{\Delta x}{\Delta y} + \frac{\Delta y}{\Delta x}\right]} \quad (5.1)$$

Interior node with generation and dissimilar materials (k_N and k_S)

$$q_N = -k_N\Delta x\Delta z\left[T_{m,n} - T_{m-1,n}\right]/\Delta y$$

$$q_S = -k_S\Delta x\Delta z\left[T_{m,n} - T_{n+1,n}\right]/\Delta y$$

$$q_E = -\left[k_N\Delta y\Delta z + k_S\Delta y\Delta z\right]\left[T_{m,n} - T_{m,n+1}\right]/2\Delta x$$

$$q_W = -\left[k_N\Delta y\Delta z + k_S\Delta y\Delta z\right]\left[T_{m,n} - T_{m,n-1}\right]/2\Delta x$$

$$q_G = q'''\Delta x\Delta y\Delta z$$

For $\Sigma q = 0$ the node equation for temperature is

$$T_{m,n} = \frac{\frac{\Delta y}{2\Delta x}\left[k_N + k_S\right]\left[T_{m,n+1} + T_{m,n-1}\right]}{\left[k_N + k_S\right]\left[\frac{\Delta x}{\Delta y} + \frac{\Delta y}{\Delta x}\right]}$$

$$+ \frac{\frac{\Delta x}{\Delta y}\left[k_N T_{m-1,n} + k_S T_{m+1,n}\right] + q''' \Delta x \Delta y}{\left[k_N + k_S\right]\left[\frac{\Delta x}{\Delta y} + \frac{\Delta y}{\Delta x}\right]} \tag{5.2}$$

Equations (5.1) and (5.2) are used in a two–dimensional array to represent a physical distribution of temperatures in the transistors and diodes. The thermal conductivities and physical geometries are listed in Tables 5.4 and 5.5, respectively. The analysis is applied first to the transistors and then to a diode.

Shown in Fig. 5.3a is the cross section of the hybrid circuit with two transistors mounted in close proximity. The area denoted with solid lines is sufficient for analysis because of thermal symmetries. In the analysis, the area is discretized by superimposing a mesh of nodes on the area. Equations 5.1 or 5.2 are applied to each control volume to generate a two–dimensional array of nodal temperature equations. A spreadsheet is used as an equation processor which solves for temperatures at each node as a function of surrounding temperatures. The solution of the temperature equations using such a processor is given in great detail by Eid [74].

The volumetric heat–generation density, q''', was determined as follows. The power dissipated in the transistor (from Jovanovic in [70]) is

$$P_t = \frac{F_c \; C_{oss} \; V_s^2}{3} + \frac{R_{ds} \; I_{rec}^{max}}{N} \qquad (5.3)$$

where the terms are as defined in Chapter 2 and Appendix A. For the ZCS–QRC developed here the F_c = 2.2 MHz, C_{oss} = 80pF, V_s = 300 V, R_{ds} = 1.5Ω, and I_{rec}^{max}/N = 0.42 A, and the power dissipated is then P_t = 5.5 W.

It is assumed that heat is generated uniformly in the upper 25% of the FET chip excluding its surface. The volumetric heat–generation density is

$$q''' = P_t/0.25 \; X_{xtr} \; Y_{xtr} \; Z_{xtr} \qquad (5.4)$$

where X_{xtr}, Y_{xtr} and Z_{xtr} are the width, thickness and depth of the transistor, respectively, and are given in Table 5.5. The density is then calculated to be q''' = 3.3 mW/m^3, and is used in (5.1) and (5.2) for the transistor profile.

The resulting two–dimensional temperature profile of the structure given in °C is shown in Fig. 5.3b and represents the area described in Fig. 5.3a for two transistors that are separated by 2 mm. The horizontal spacing between nodes is 0.1 mm. The vertical spacing of layers (except heatsink) are in relative proportion with specific dimensions given in Table 5.5. As seen in

Fig. 5.3b under worst–case conditions there is a 30°C difference from center chip (upper left corner) to heatsink, or 5.5°C/W. Most of the heat flow is vertical with minor heat spreading in the x direction. The amount of spreading shown, however, indicates some interaction of other closely spaced transistors, though not appreciable. Also, the profile shows that much of the thermal impedance, 3.1°C/W, is dropped across the mounting material for the substrate and heat sink.

This analysis applies directly to the ZCS–QRC fabricated during this research. Temperature measurements of the circuit with a noncontact probe showed a 53°C surface temperature and a 27°C ambient temperature. The temperature difference of 26°C is well within the calculated temperature difference of 30°C. The 15% error is acceptable since the properties of the materials are not accurately known and the analysis is limited to two dimensions.

The same analysis technique and assumptions were used to analyze the temperature profile of the Schottky rectifers. The maximum power loss in the rectifiers was computed to be 4.9 W. The physical structure and temperature profile (in °C) for a single diode is shown in Fig. 5.4 with an anode–to–substrate connection. The connection uses a 0.13 mm (5 mils) thick copper ribbon which directs approximately 10% of the heat flow from the surface. The horizontal spacing between nodes is 1.0 mm. The vertical spacing of layers (except for heatsink) are in relative proportion with actual

dimensions given in Table 5.5. It is assumed that all the heat is generated in the upper half of the silicon. For this structure there is a 15°C drop from semiconductor to heatsink, or an equivalent 3.2°C/W thermal impedance. Again, there is mostly vertical heat flow, and the same assumptions about component interactions can be made as for the transistors.

From the analysis, it is shown that the ambient temperature should be kept at less than 70°C if the transistor junction temperature is not to exceed 100°C. The profile should be corrected for actual heatsink efficiency and any margin of error due to approximations of the thermal properties of the materials.

5.4 Circuit Performance

The hybridized power stage was connected in the laboratory to a 0–300 V supply and a hybridized controller. The voltage supply was varied up to 300 V. Shown in Figs. 5.5a, b and c are switching transistor voltages. Figure 5.5a shows the gate–to–source voltage on transistor Q2 (see Fig. 2.1). The oscillation occurring nearly half–way up the rising edge of the voltage waveform indicates the precise time the device is turned on. This is the time that the equivalent Miller capacitances are charged or discharged appropri– ately. Figures 5.5b and 5.5c show the drain–to–source voltages at half load (10 amps) and full load (20A) with the supply voltage at 300 V. Under full load the circuit ran at a conversion frequency of 1.6 MHz. With a supply

voltage of 250 V and full load, the conversion frequency increased to 1.9 MHz. Initial difficulties with symetrical operation of a gate drive circuit during turn off of transistor Q1 caused oscilltions in Fig. 5.5c (during turn off). The use of a different driver allowed operation to a full 2.2 MHz, however, no waveforms are available. An increase of the resonant capacitance to a value higher than initially calculated (to 200 nF) was needed. This indicates that a factor of 0.8 rather than 0.9 in (2.1) should be raised to calculate the resonant capacitor value.

The circuit efficiency for low line (250 V) and nominal line (300 V) is shown in Fig. 5.6. The efficiency for the power stage is 78% $\pm$ 1% for an output current range from 6 A (30 W) to a full load of 20 A (100 W). As shown in the figure, the losses due to higher switching frequencies at low line are nearly equal to the losses due to high line voltages (occuring at lower frequencies). Having a similar efficiency for both line voltages is coincidental. The full–load low line conversion frequency is 2.2 MHz and conductor loss is lower than measurable. Compared with a printed– wiring breadboard version of this circuit, the frequency is 10% to 20% higher at the same efficiency; however, the power density is much greater. The variation of frequency due to load is shown in Fig. 5.7.

The converter uses a single–loop control. The measured closed–loop gain and phase at nominal line and full load are shown in Fig. 5.8. There is approximately 10 db of gain margin and a 37° phase margin. Gain crossover is at 13 kHz.

The power circuit is shown on the left side in Fig. 5.9 and is adjacent to a hybridized control circuit. The substrate of the two circuits is 5.8 cm (2.3 in.) long and 4.3 cm (1.7 in.) wide. However, the circuit portion is only 3.6 cm (1.4 in.) wide. Excluding heatsink and control, the power stage has a density of 3.1 W/cu.cm (50 W/cu.in.); with heatsink and control, the density is 2.1 W/cu.cm (35 W/cu.in.). Further size reduction can be made by repositioning the filter inductor, decreasing the present circuit size to fit the shorter transformer (which is shown) and locating source and output terminals on opposing sides. Such reduction could add 30% to the density.

TABLE 5.1

Design Requirements of Hybridized ZCS–QRC

Min. Input voltage – V_s^{min}	150 V
Max. Input voltage – V_s^{max}	425 V
Output voltage – V_o	5 V
Output voltage ripple (p–p) – V_o^δ	50 mV
Max. load resistance – R_L^{max}	2.5 Ω
Min. load resistance – R_L^{min}	0.31 Ω
Filter inductor ripple current (p–p) – I_f^s	1 A
Turns ratio of transformer – N	12
Leakage inductence of transformer –L_r	20 nH

TABLE 5.2

Calculated Component Values and Circuit Parameters

for Hybridized ZCS–QRC

COMPONENT	VALUE
Resonant capacitance (2.1) – C_r	162 nF
Max. switch breakdown voltage – BV_{ds}^{min}	425 V
Peak switch current (A.18) – I_s^{max}	5.9 A
Optimum on–resistance (2.7) – $R_{ds}^{opt}(on)$	0.7 Ω
Average rectifier current. (A22) – I_{rec}^{max}	10 A
Peak reverse rectifier voltage (A23) – V_{rec}^{max}	53 V
Average freewheeling diode current (A24) – I_{dfw}^{max}	20 A
Peak reverse freewheeling diode V (A20) – V_{fw}^{max}	35 V
Filter inductance – (2.10) L_f	4.8 μH
Filter capacitance (2.11) – C_f	6.7 μF
Filter capacitance ESR (2.12) – ESR^{max}	7.2 mΩ

TABLE 5.3

Part List For Hybridized ZCS–QRC

COMPONENT	PART
Primary Switch Q_1, Q_2	IRFC330
Transformer Core:	TDK LP 23/8 (H_{7c4})
Turns Ratio (N)	12
# of Prim. Turns (N_1)	12T, Litz 100/42
# of Sec. Turns (N_2)	1T, 2 mil Cu foil
Leakage Ind.	15 nH @ secondary
Resonant Ind. (L_r)	leak. induct. of transformer
Resonant Capapacitor	162 nF NPO
Rectifiers	IR60CNQ045
Filter Inductor (L_f)	MPP 55125 7T AWG# 16
Filter Capapcitor (C_f)	2 X 265L 6301 336–1 (2 X 33 μF tant. chip (Matsuo))
Input Capacitors (C_i)	0.1 μF X7R

TABLE 5.4
Properties of Materials

Material	Thermal Conductivity [mW/mm-°C]
Attachment	
CF561K*	1.5
561K*	0.88
Metals	
Aluminum	222
Copper	391
Molybdenum	151
Silicon	147
Silver	419
Solder	
92Pb,5In,2.5Ag	38.7
Substrates	
Alumina	26
Aluminum Nitride	150
Silcon Carbide	90

*Epoxy filled fiberglass mesh by Ablestick, Inc.

TABLE 5.5

Component Dimensions For Semiconductors and Materials

Component	Width [mm]	Depth [mm]	Thickness [mm]
For transistor analysis			
Transistor	4.45	3.68	0.406
Solder	4.45	3.68	0.127
Silver	5.22	3.98	0.1051
Substrate	8.56	7.79	0.635
Attachment	8.56	7.79	0.102
Heatsink	20.6	19.8	4.01
For diode analysis			
Diode	5.28	5.28	0.297
Solder	5.28	5.28	0.127
Molybdenum	5.28	5.28	0.329
Substrate	55.0	43.9	0.635
Attachment	55.0	43.9	0.102
Heatsink	55.0	43.9	4.01

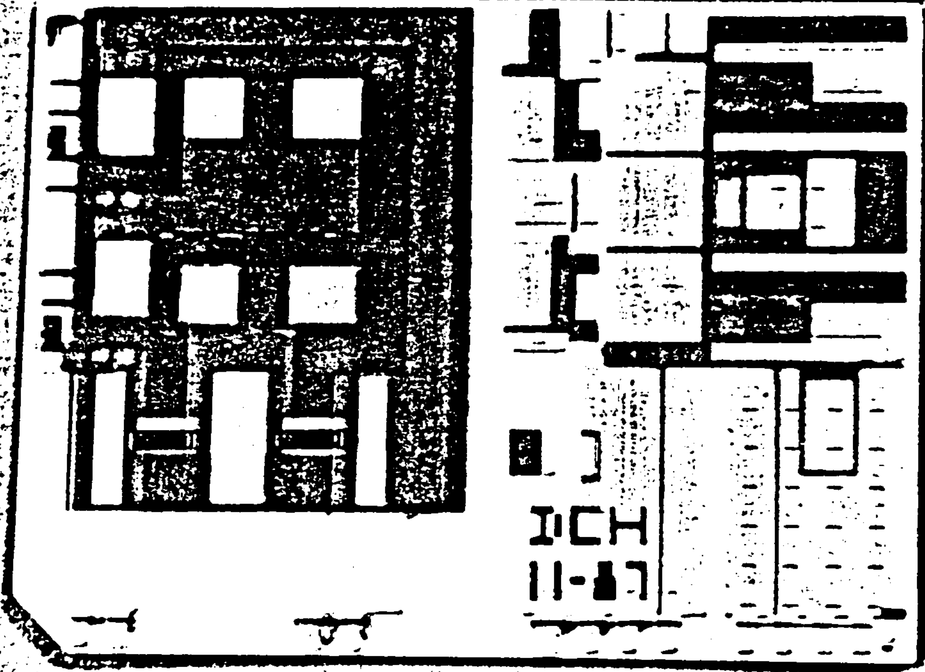

Fig. 5.1 Substrate for HB ZCS–QRC

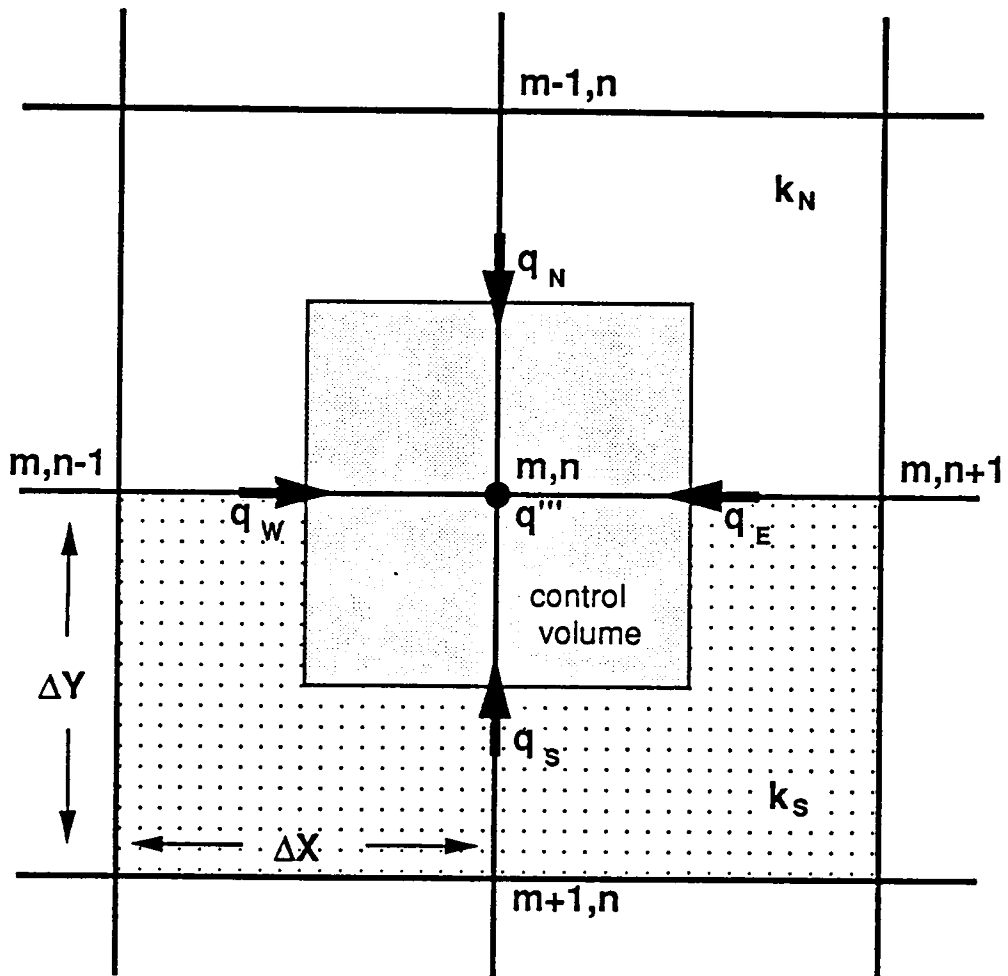

Fig. 5.2 Two–dimensional nodal network

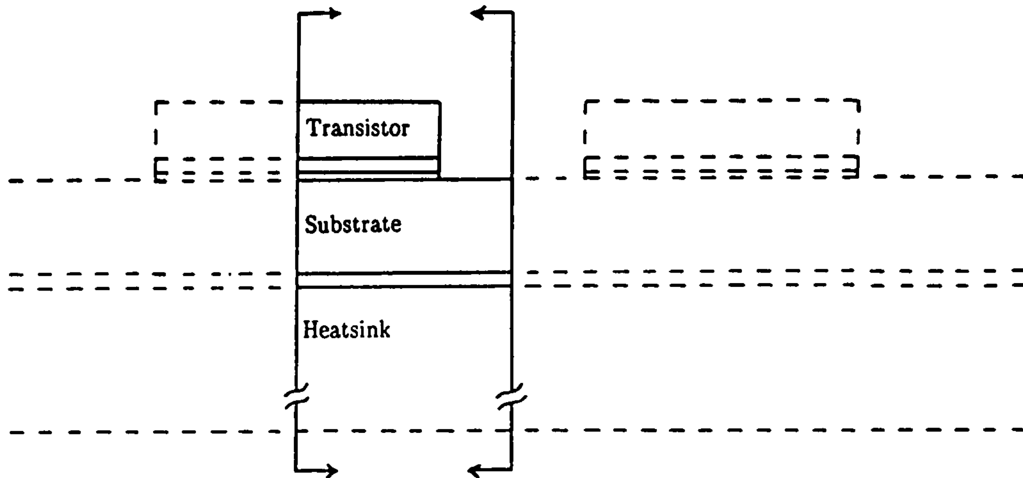

Fig. 5.3a Cross section of hybrid circuit with two transistors mounted in close proximity

```
 ______________________________________________________________________________
|                                                                              |
* 29.52 30 29 29 29 29 29 29 29 29 29 29 29 29 29 29 28 28 28 28 28 28        *
|                             TRANSISTOR                                       |
* 29.22 29 29 29 29 29 29 29 29 29 29 29 29 28 28 28 28 28 28 28 28 28        *
|                                                                              |
* 28.94 29 29 29 29 29 29 29 29 29 28 28 28 28 28 28 28 28 28 28 27 27        *
|______________________________________________________________________________|
|                               SOLDER                                         |
* 28.33 28 28 28 28 28 28 28 28 28 28 28 28 28 27 27 27 27 27 27 26 26        *
|                                                                              |
|______________________________________________________________________________________________
|                               SILVER                                 :                   |
|                             (neglected)                              :                   |
|__________________________________________________________________________________________________________________
|                                                                      :                                           |
|                                                                      :                                           |
* 27.16 27 27 27 27 27 27 27 27 27 27 27 26 26 26 26 26 26 25 25 24 23 21 20 18 18 17 16 16 15 15 15              *
|                                                                                                                  |
* 25.77 26 26 26 26 26 26 26 25 25 25 25 25 25 25 24 24 24 23 23 22 21 20 19 18 17 17 16 16 15 15 15              *
|                                          SUBSTRATE                                                               |
* 24.40 24 24 24 24 24 24 24 24 24 24 24 24 23 23 23 23 22 22 21 21 20 19 18 17 17 16 16 15 15 15 15              *
|                                                                                                                  |
* 23.05 23 23 23 23 23 23 23 23 23 23 22 22 22 22 22 21 21 21 20 19 19 18 17 17 16 16 15 15 14 14 14              *
|                                                                                                                  |
* 21.70 22 22 22 22 22 22 21 21 21 21 21 21 21 21 20 20 20 19 19 18 18 17 16 16 15 15 14 14 14 14 14              *
|                                                                                                                  |
|_________________________________________ATTACHMENT_______________________________________________________________|
* 18.73 19 19 19 19 19 19 19 18 18 18 18 18 18 18 18 17 17 17 16 16 15 15 14 14 13 13 12 12 12 12 12              *
* 14.10 14 14 14 14 14 14 14 14 14 14 14 14 13 13 13 13 13 13 12 12 12 11 11 10 10 10 10  9  9  9  9              *
* 9.478  9  9  9  9  9  9  9  9  9  9  9  9  9  9  9  9  9  8  8  8  8  8  7  7  7  7  7  6  6  6  6              *
* 4.854  5  5  5  5  5  5  5  5  5  5  5  5  5  5  5  5  4  4  4  4  4  4  4  4  4  4  4  4  4  4  4              *
|__________________________________________________________________________________________________________________
* 1.845  2  2  2  2  2  2  2  2  2  2  2  2  2  2  2  2  2  2  2  2  2  2  2  2  2  2  2  2  2  2  2              *
|                                           HEATSINK                                                               |
:                                                                                                                  :
* .6053 .6 .6 .6 .6 .6 .6 .6 .6 .6 .6 .6 .6 .6 .6 .6 .6 .6 .6 .6 .6 .6 .6 .6 .6 .6 .6 .6 .6 .6 .6 .6              *
 __________________________________________________________________________________________________________________
         0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0  0
```

Fig. 5.3b Temperature profile of structure of Fig. 5.3a.

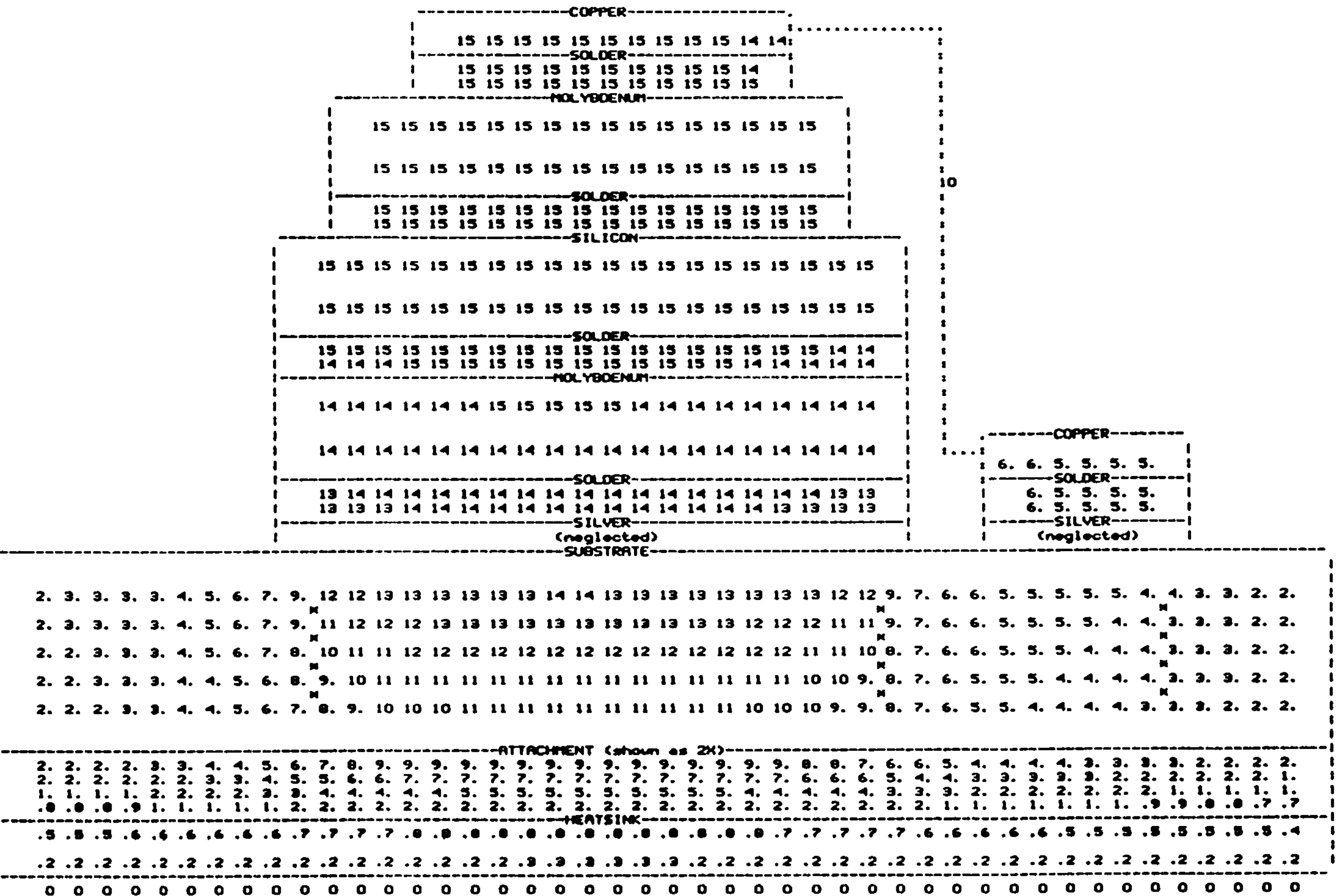

Fig. 5.4 Temperature profile of rectifiers with anode–to–substrate connection

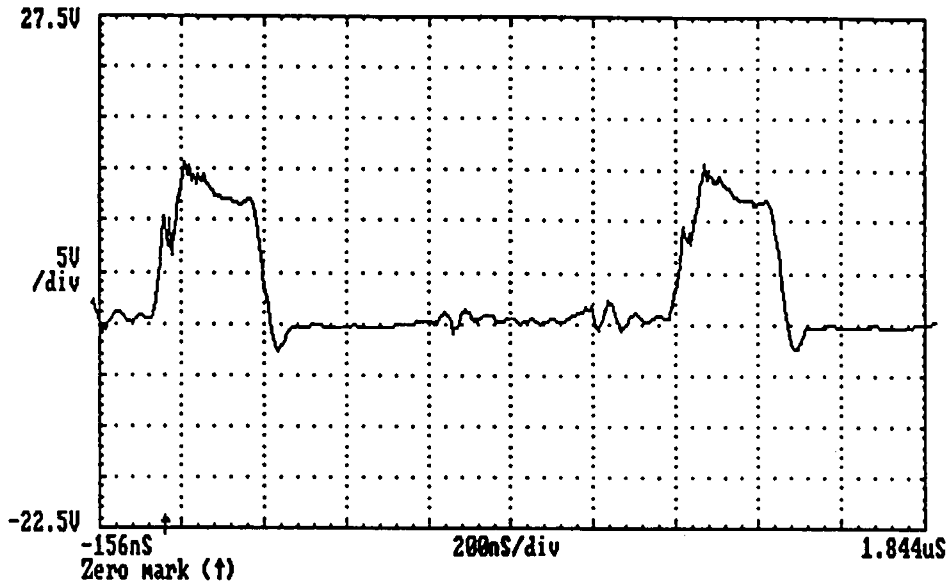

Fig. 5.5a Gate–to–source voltage across lower switch transistor

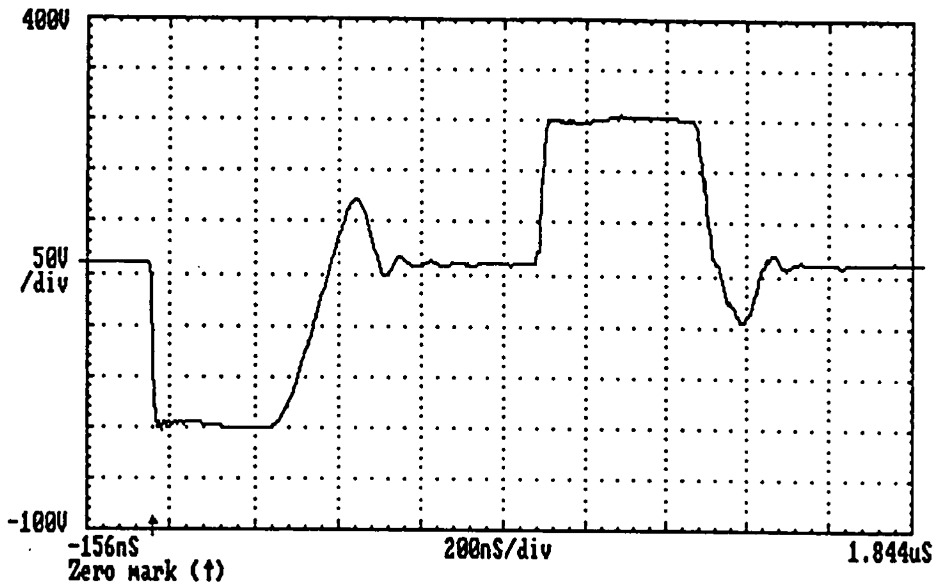

Fig. 5.5b Drain–to–source voltage for lower switch at half load (10A) and with a source voltage of 300 V

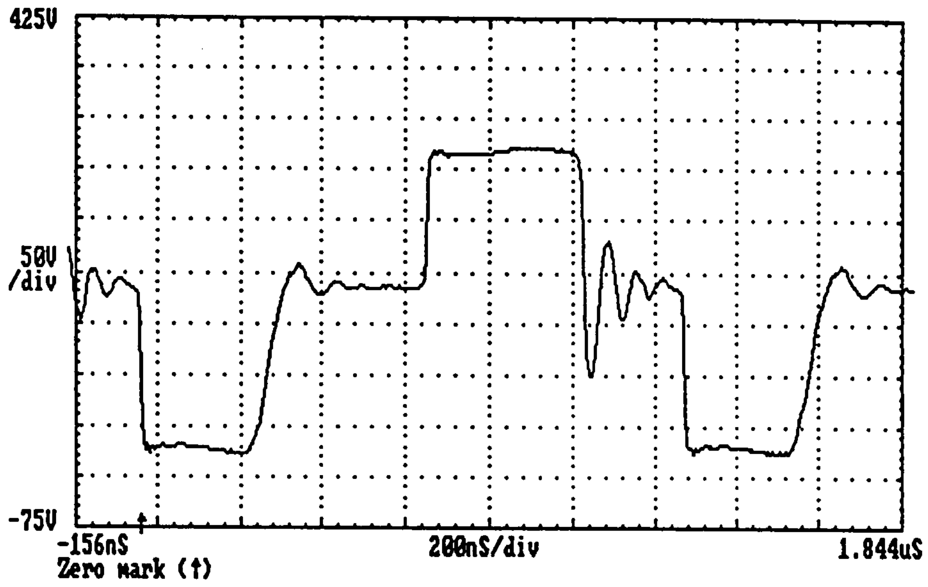

Fig. 5.5c Drain–to–source voltage for lower switch at full load and with a source voltage of 300 V

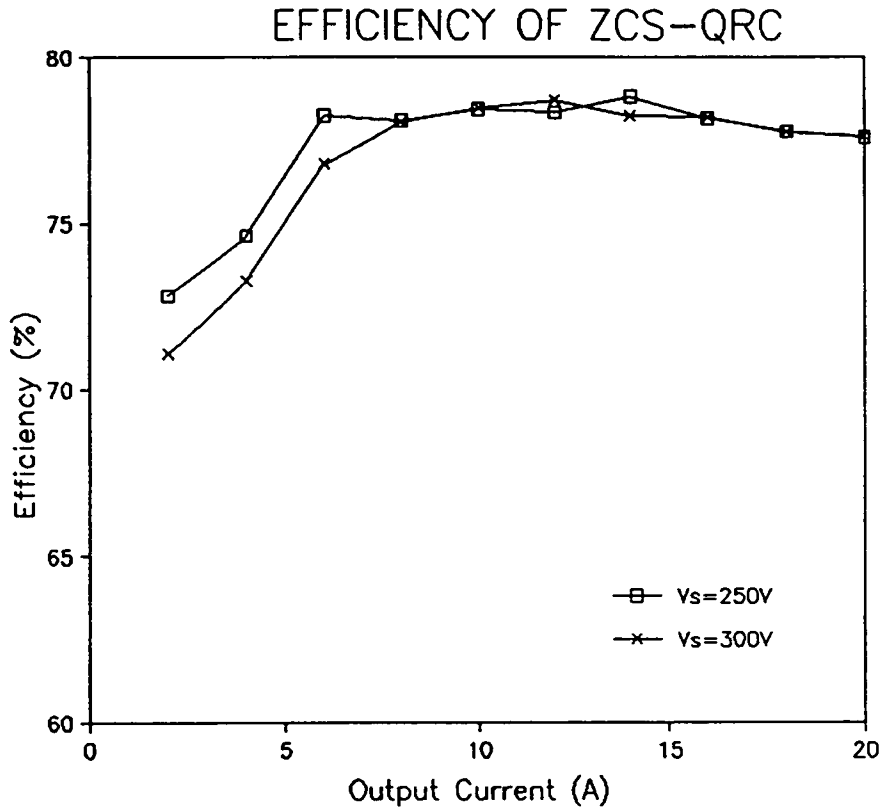

Fig. 5.6 Efficiency vs. output current for low and nominal input voltages. Output voltage $V_o = 5$ V

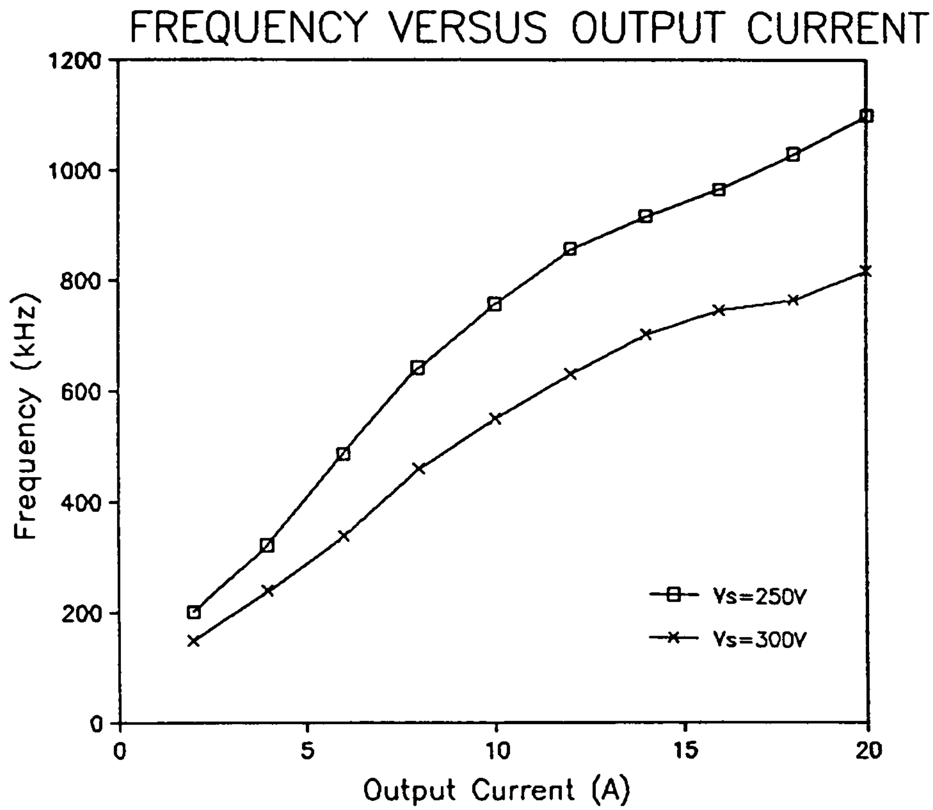

Fig. 5.7 Switching frequency (half of conversion frequency) vs. output current for low and nominal input voltages

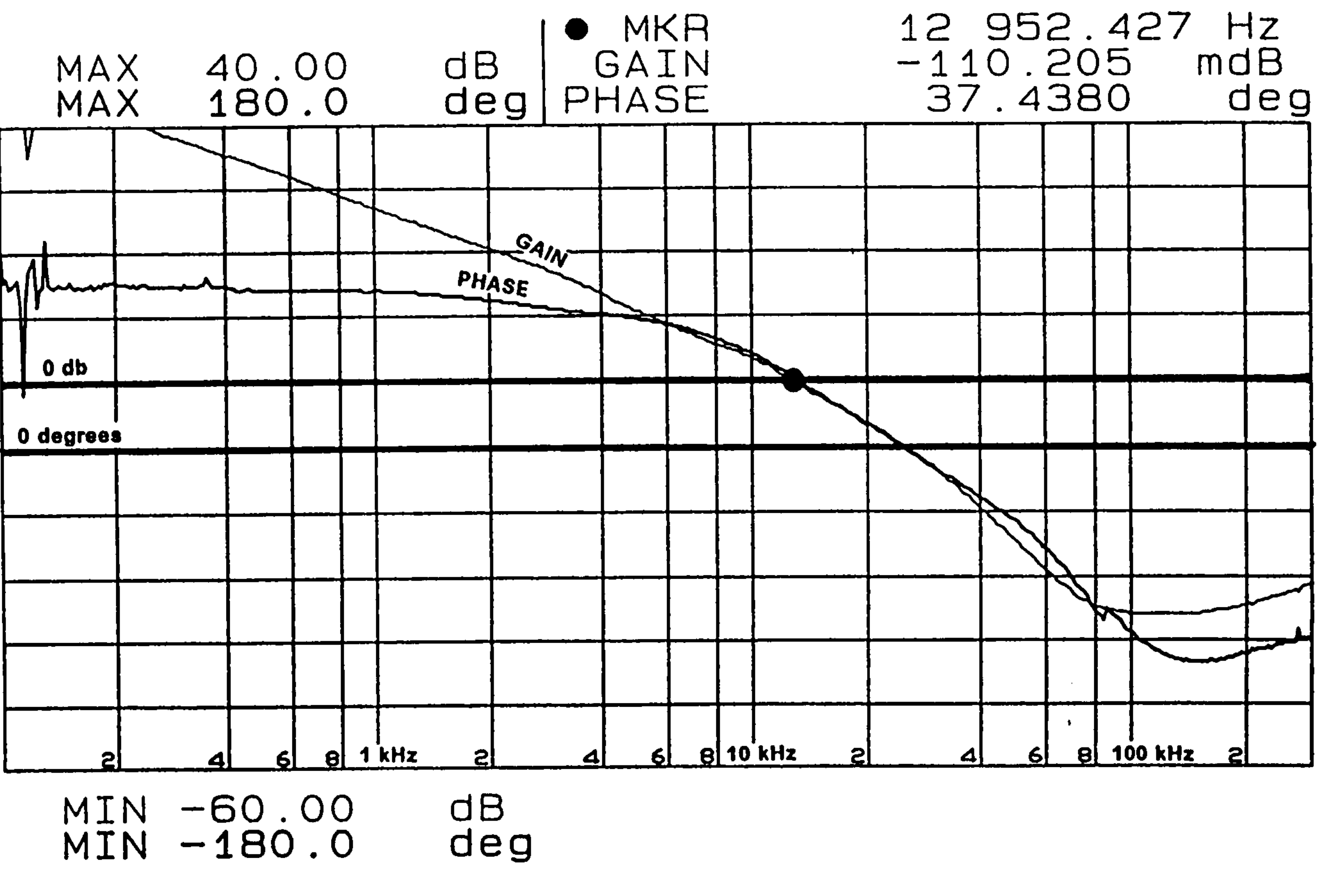

Fig. 5.8 Measured closed–loop gain and phase at full load and nominal input voltage

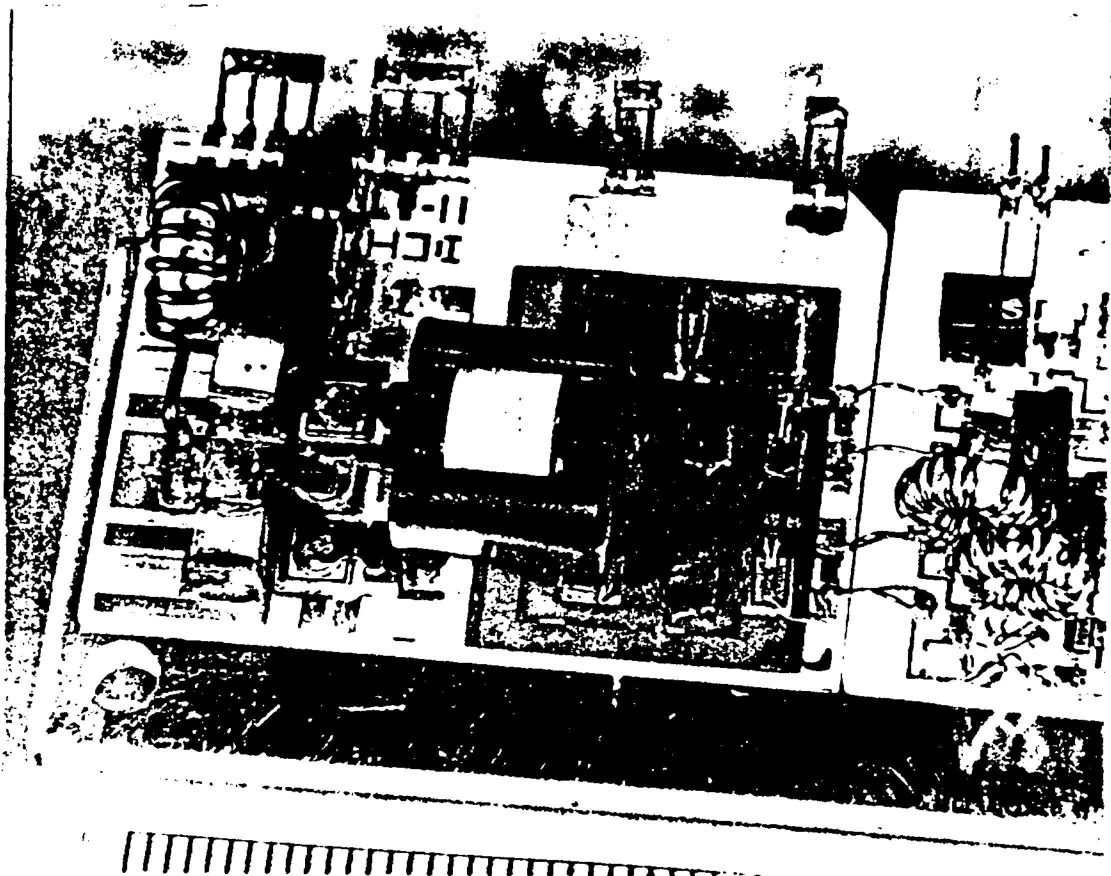

Fig. 5.9 Hybridized HB ZCS–QRC

CHAPTER 6

SUMMARY

The initial goal of the research was the development of a high density dc to dc converter for off–line use. A power density greater than 25 W/cu.in.. was targeted. The state of the technology at the time research began was such that off–line converters were at less than 10 W/cu.in. and operated with PWM techniques.

To achieve higher density a reduction in both component size and circuit size was necessary. The operating frequencies of the converters needed to be raised substantially to reduce component size. However, with PWM techniques, increasing the frequency led to sharp increases in losses. A solution was to use a zero–current quasi–resonant switching technique. This allowed the converter to operate at megahertz frequencies and assured the use of smaller components. To support circuit development at the higher frequencies and provide a reduction in circuit size a thick–film hybrid microelectronic process was used to fabricate the circuits.

At megahertz frequencies the physical and electrical circuit topologies are strongly interdependent. Parasitic elements, such as inductances and capacitances, which occur easily in the physical layout of a circuit, can provide beneficial or detrimental effects in the electrical circuit. Hence, the fabrication process was electrically characterized for its use in the converter

development. It was found that the coupling capacitances in the power circuit were negligible, but the lead and interconnect inductances were significant. It was determined that that the ac conductor resistance was significant at the low megahertz frequencies of interest. To have the conductor resistance be less than 20% above the dc value the thickness of the circuit conductors needed to be equal to or greater than one skin depth. At low megahertz frequencies a skin depth of 45 microns or more was expected. Since traditional hybrid microelectronic fabrication process was not able to provide the needed conductor thicknesses, a thick–printing process was developed to provide 50 micron–thick conductors.

Preliminary to the power hybrid circuit and process development, which the author was undertaking, a breadboard version of the converter circuit was being developed by M.M. Jovanovic, who developed the quasi–resonant technique for off–line applications.

Developments from the breadboard were combined with the hybrid work to produce a hybridized converter power stage. At the culmination of this research effort a chip and wire version of the ZCS–QRC power stage was produced which operated at 100 W with a 78% efficiency including control, and having a 3.1 W/cu.cm (50 W/cu.in.) density (for the power stage only). A thermal analysis was performed on the circuit predicting approximately a 30°C rise at full power and was confirmed through lab measurements.

It is suggested that future work to achieve higher density supplies continue in three areas. The first area is well underway with the use of the zero–voltage quasi–resonant and multi–resonant techniques. This, hope–fully, will push the frequency to much higher levels without sacrificing efficiency and help reduce the size of components. With zero–current switching there remains significant loss during turn on when the charged terminal capacitances of the switches are discharged through the switches. The zero–voltage technique eliminates this loss. A similar loss occurs for the diodes. The use of thick–film techniques will be more applicable since higher frequencies will be used.

Throughout this research the magnetic components, specifically the transformer and filter inductor, have been physically difficult to use with hybridization techniques. Also the repeatability of obtaining critical parasitic values of leakage inductance has been poor. Future work should concentrate on reducing the size of magnetic components, particularly making the magnetics more planar, and improving electrical characteristics of the materials.

The third area for future work should investigate what methods are available for fabricating power hybrid circuits and, if possible, the selection of an optimum method. Since higher density implies closer spacing of components, besides smaller components, then techniques for packing circuits should be investigated, particularly, those that are compatible with magnetic components.

REFERENCES

[1] R. Redl, N.O. Sokal, "High–Frequency Switching–Mode Power Converters: General Considerations and Design Examples at 0.6, 1 and 14 MHz," Tutorial – High Frequency Power Conversion Conference Record, Virginia Beach, VA., May, 1986.

[2] B. Carsten, "Switchmode Design Techniques Above 500kHz," ibid.

[3] F. M. Totten, "Practical Design Considerations for High Frequency Avionic Flyback Power Systems," High Frequency Power Conversion Conference Record, Washington, DC, pp.235–243, April, 1987.

[4] H. Liu and F. C. Lee, "Resonant Switches – A Unified Approach to Improve Performances of Switching Converters," IEEE Int'l. Telecommunications Energy Conference Record, Tokyo, Japan pp.334–341, October 1984.

[5] E. Buchanan and E.J. Miller, "Resonant Switching Power Conversion Technique," Proceedings of the IEEE Power Electronics Specialists Conference, Culver City, California, pp.188–193, 1975.

[6] E.J. Miller, "Resonant Switching Power Conversion," Proceedings of the IEEE Power Electronics Specialists Conference, Cleveland, Ohio pp.206–211, 1976.

[7] E.J. Miller, "Resonant Switching Converter," U.S. Patent, 4,138,715, 1979.

[8] D.C. Hopkins, M.M. Jovanovic, F.C. Lee and F.W. Stephenson, "One–Megahertz, Off–Line Converter Hybridization," Virginia Power Electronics Seminar, Virginia Polytechnic Institute and State University, Blacksburg, Virginia, pp.134–149, November 1986.

[9] W.A. Tabisz, P. Gradzki, F.C. Lee, "Zero–Voltage–Switched Quasi–Resonant Buck and Flyback Converters – Experimental Results at 10 MHz," Proceedings of the IEEE Power Electronics Specialists Conference, Blacksburg, Virginia, pp.404–413, June 1987.

[10] H.M. Wick, Jr. and S. Capodici, "A Design for Thick Film Microcircuit DC–to–DC Converter Electronics," IEEE Transactions on Aerospace and Electronic Systems, Vol.AES–7, No.3, pp. 528–531, May 1971.

[11] J. Kociecki, U.B. Goerke and W.W. Burns III, "A High Power–Density DC–DC Converter Board," Proceedings of the IEEE Applied Power Electronics Conference, San Diego, California, pp.169–180, 1987.

[12] F.S. Kamp and J.C. Sondermeyer, "A Hybrid 100–Watt Linear Audio Amplifier," Proceedings of the IEEE Spring Convention on Broadcast and Television Receivers, Chicago, Illinois, pp.15–23, June 1969.

[13] W. Schultz, "A Major Step in Power Hybrids," Proceedings of the IEEE Electronic Components Conference, Washington, DC, pp.159–162, May 1971.

[14] Y.S. Sun and J.C. Driscoll, "A New Hybrid Power Technique Utilizing a Direct Copper to Ceramic Bond," IEEE Transactions on Electron Devices, Vol.ED–23, No.8, pp.961–967, August 1976.

[15] C.V. Cox, et al., "A New Thick Film Materials System for Aluminum Nitride–Based Power Hybrid Circuits," ISHM Int'l. Journal for Hybrid Microelectronics, Vol.10,No.3, pp.8–12, September 1987.

[16] J.F. Dickson and D.R. Asher, "A Versatile High Performance Hybrid Power Package," Proceedings of the ISHM Int'l. Symposium on Microelectronics, Anaheim, California, pp. 343–348, November 1985.

[17] C.B. Jones and J.P. Vergez, "Application of PWM Techniques to Realize a 2MHz Off–Line Switching Regulator With Hybrid Implementation," Proceedings of the IEEE Applied Power Electronics Conference, New Orleans, Louisiana, pp. 221–227, 1986.

[18] R.J. Guttmann, "Application of RF Circuit Design Principles to Distributed Power Converters," IEEE Transactions on Industrial Electronics and Control Instrumentation, Vol.IECI–27, No.2, pp.156–164, May 1980.

[19] S.G. Konsowski, J.A. Olenick and R.D. Hall, "Evaluation of Advanced Ceramics for High Power and Microwave Circuitry," Proceedings of the ISHM Int'l. Symposium on Microelectronics, Anaheim, California, pp.213–217, November 1985.

[20] S.G. Konsowski, et al., "Evaluation of Advanced Ceramics for High Power and Microwave Circuitry – Part II," ISHM Int'l. Journal for Hybrid Microelectronics, Vol.10, No.3, pp.13–18, September 1987.

[21] L.R. Kaufman, "Fabrication of a Power Hybrid Semiconductor Module," ISHM Int'l. Journal for Hybrid Microelectronics, Vol.5, No.2, pp.125–129, November 1982.

[22] M.R. Neider, "High Density Power Hybrids and Their Design Considerations," Proceedings of the ISHM Int'l. Symposium on Microelectronics, Dallas, Texas, pp.330–332, 1984.

[23] W.R. Peterson, "High–Power Hybrids," Design Electronics (GB), Vol.8, No.1, pp.38–39, October 1970.

[24] G. Nippert and G. Kohler, "Highly Integrated Bridge–Circuits for High Power Applications," Power Conversion and Intelligent Motion (PCIM) Magazine, Vol.14, No.2, pp.15–19, February 1988.

[25] J.C. Gioia, "MIC Package Using Thick Film and Direct Bond Copper for 100–W L–Band Power Amplifier," Proceedings of the ISHM Int'l. Symposium on Microelectronics, Los Angeles, California, pp.214–218, 1979.

[26] R.F. Peluso, "Material and Design Considerations for Power Hybrid Packages," ISHM Int'l. Journal on Hybrid Microelectronics, Vol.6, No.1, pp.302–306, October 1982.

[27] W.L. Wright, "Multi–Chip Power Hybrid Module," IBM Technical Disclosure Bulletin, Vol.24, No.11B, pp.6189–6190, April 1982.

[28] E. Foodim and R. Gold, "New Developments in Power Hybrids for Voltage Regulators," National Solid–State Power Electronics Conference (POWERCON–1) Record, pp.166–169, March 1975.

[29] B. Dance, "New Power Hybrid Circuits," Australian Electronic Engineering, Vol.8, No.12, pp.19–23, December 1975.

[30] J. Steel, "Power Hybrid Circuits," Powertechnics Magazine, Vol.3, No.2, pp.24–26, February 1987.

[31] J. Parry and H.J. Biagi, "Power Hybrid Design Considerations," Hybrid Circuit Technology Magazine, Vol.3, No.5, pp.37–41, May 1986.

[32] M.J. Wood, "Power Hybrid Thick Film Modules," Proc. of the Conf. on Hybrid Microelectronics, Canterbury, England, pp.265–273, September 1973.

[33] R.D. Gold, "Power Hybrid Voltage Regulators for Computer and Instrumentation," Proceedings of the ISHM Int'l. Symposium on Microelectronics, Chicago, Illinois, pp.4–9, October 1971.

[34] R.C. Newton, Jr. and D.G. Frey, "Power Hybridization – Key to Reducing Avionics Power Supply Weight and Volume," NAECON Record, Vol.2, Dayton, Ohio, pp.698–703, 1979.

[35] Darnell Research Inc. "Power Hybrids," Powertechnics Magazine, Vol.3, No.7, pp.14–18, July 1987.

[36] R.P. Daniel, "Power Hybrids: A New Approach," ISHM Int'l. Journal for Hybrid Microelectronics, Vol.5, No.2, pp.110–114, November 1982.

[37] F.F. Cilyo, "Power Transistor Module for High Current Applications," IEEE Industry Applications Society Conference Record, Atlanta, Georgia, pp.464–466, 1975.

[38] R. Weiss, "Resonant Switching Supply Delivers Power Density of 2.9W/cu in at 400V," Electronic Design Magazine, Vol.32, No.22, pp.163–170, November 21, 1985.

[39] D.E. Neill, "The Direct Bonding of Copper to Ceramic and Resulting Advantages and Applications," Proceedings of the Int'l. Conference on Mfgr. and Packaging Tech. for Hybrid Circuits, Paris, France, pp.239–247, 1976.

[40] A. London, et al., "Thick Film Material Requirements for Power Hybrids on Beryllia," Proceedings of the ISHM Int'l. Symposium on Microelectronics, Dallas, Texas, pp.13–18, 1984.

[41] A.A. Mohammed, "Thick Film Metallizations and Performance of a Power Hybrid Module on Alumina Nitride Substrates," Proceedings of the ISHM Int'l. Symposium on Microelectronics, Anaheim, California., pp.218–224, 1985.

[42] C. Zardini, et al., "Use of Thick Film Copper Technology for High Power Hybrid Circuits," Toute l'electronique, No.492, pp.47–51, March 1984.

[43] G.W. Smith, "Voltage Regulator Capabilities Using Hybrid Techniques," WESCON Tech. Papers/Western Electronic Show and Convention, San Francisco, California, 13–05–17/2–69, pp.1–8, August 1969.

[44] K.H. Liu and F.C. Lee, "Secondary–Side Resonance for High–Frequency Power Conversion," Proceedings of the IEEE Applied Power Electronics Conference (APEC), New Orleans, Louisiana, pp.83–89, April 1986.

[45] A.M. Heyman "Low–Profile High–Frequency Off–Line Quasi–Resonant Converter," Proceedings of the IEEE Applied Power Electronics Conference, San Diego, California, pp.157–167, 1987.

[46] M.M. Jovanovic, D.C. Hopkins and F.C. Lee, "Design Aspects for High–Frequency Off–Line Quasi–Resonant Converters," High Frequency Power Conversion Conference Record, Washington, DC, pp.83–97, April 1987.

[47] M.M. Jovanovic and F.C. Lee, "Stability Analysis of Push–Pull and Bridge–Type Zero–Current–Switched Quasi–Resonant Converters," Proceedings of the IEEE Power Electronics Specialists Conference, Kyoto, Japan, pp.533–540, April 1988.

[48] F.C. Lee, et al., "High–Performance High–Frequency Distributed Computer Power Supply Technology," Phase II Report for the Digital Equipment Corporation, prepared by the Virginia Power Electronics Center, VPI&SU, Blacksburg, Va., February 1988.

[49] D.C. Hopkins, M.M. Jovanovic, F.C. Lee and F.W. Stephenson, "Two–Megahertz, Off–Line Hybridized Quasi–Resonant Converter," Proceedings of the IEEE Applied Power Electronics Conference, San Diego, California., pp. 105–114, March 1987.

[50] M. Shatzkes and J.R. Lloyd, "A Model for Conductor Failure Considering Diffusion Concurrently with Electromigration Resulting in a Current Exponent of 2," Journal for Applied Physics, Vol.59, No.11, pp.3890–3893, June 1986.

[51] J.R. Lloyd and P.M. Smith, "The Effect of Passivation Thickness on the Electromigration Lifetime of Al/Cu Thin Film Conductors," Journal for Vacuum Science Technology, Vol.2, No.2, pp.445–458, April 1983.

[52] A. Hornung, "Electrical Properties of a Silver Contaminated Borosilicate Glass," Proceedings of the IEEE Electronics Components Conference, Los Angeles, California, pp.119–123, 1979.

[53] A. DerMarderosian, "The Electrochemical Migration of Metals," Proceedings of the ISHM Int'l. Symposium on Microelectronics, Minneapolis, Minnesota, pp.134–141, 1978.

[54] J.R. Lloyd, "Electromigration," Journal of Metals, Vol.36, No.7, pp.54–56, July 1984.

[55] D.E. Riemer, "Material Selection and Design Guidelines for Migration–Resistant Thick–Film Circuits with Silver–Bearing Conductors," Proceedings of the IEEE Electronic Components Conference, Atlanta, Georgia pp. 287–292, 1981.

[56] G. DiGiacomo, "Metal Migration (Ag,Cu,Pb) in Encapsulated Modules and Time–To–Fail Model as a Function of the Environment and Package Proprties," Proceedings of the IEEE Int'l. Reliability Physics Symposium, San Diego, California, pp.27–33, March 1982.

[57] J.R. Lloyd, "On the Log–Normal Distribution of Electromigration Lifetimes," Journal for Applied Physics, Vol.50, No.7, pp. 5062–5064, July 1979.

[58] H.M. Naguib and B.K. MacLaurin, "Silver Migration and the Reliability of Pd/Ag Conductors in Thick–Film Dielectric Crossover Structures," IEEE Transactions on Components, Hybrids, and Manufacturing Technology, Vol.CHMT–1, No.2, pp.196–207, June 1979.

[59] S. Ramo and J.R. Whinnery, Fields and Waves in Modern Radio, John Wiley and Sons, New York, p.240, 1953.

[60] R.W. Burton, "Proximity Effects for Parallel Rectangular Conductors in Nontransmission–Line Mode", IEEE Transactions on Antennas and Propogation, pp. 583–585, July 1973. (Note: Eq. 5 should be $1 + [(B/A)/(2 + B/A)]$.)

[61] D.E. Reimer, "The Function and Performance of the Stainless Steel Screen During the Screen–Print Ink Transfer Process," International Journal for Hybrid Microelectronics, Vol.10, No.2, pp.1–8, 2 Qtr 87.

[62] B. Huner, "Comments on: 'The Function and Performance of the Stainless Steel Screen During the Screen–Print Ink Transfer Process'," International Journal for Hybrid Microelectronics, Vol.10, No4, pp.6–13, 4 Qtr 87.

[63] P.J. Holmes and R.G. Loasby, Handbook of Thick Film Technology, Electrochemical Publications Limited, pp.102–104, 1976.

[64] J.W. Robbins, "A Quick Reliable Method For Measuring Yield Value, Plastic Viscosity and "Mac Michael" Viscosity of Chocolate," Manufacturing Confectioner, Vol.59, No.5, pp.38–40,42–44, May 1979.

[65] J.P. Brown, Private Communication, DuPont Electronics, Wilmington, Delaware, 1988.

[66] S.G. Stalnecker, Jr., and R.A. Wyant, "New Stencil Screen Developments for Thick Film Printing," Solid State Technology, pp.141–146, October 1983.

[67] D.C. Hopkins, F.W. Stephenson and F.C. Lee, "Determination of Conductor Thickness and Width for Power Hybrid Circuits," Virginia Power Electronics Center Seminar, VPI&SU, Blacksburg, Virginia 20461, pp.92–97, September 1988.

[68] D.C. Hopkins, M.M. Jovanovic, F.W. Stephenson and F.C. Lee, "Hybridized Off–Line 2–Mhz Zero–Current–Switched Quasi–Resonant Converter," IEEE Transactions on Power Electronics, Vol.4, No.1, pp.147–154, January 1989.

[69] D.C. Hopkins, F.W. Stephenson and F.C. Lee, "Printing of Thick Thick–Film Conductors for Power Hybrid Circuits," Proceedings of the ISHM Int'l. Symposium on Microelectronics, Seattle, Wash., pp.95–101, October 1988.

[70] M.M. Jovanovic, D.C. Hopkins and F.C. Lee, "Evaluation and Design of Megahertz–Frequency Off–Line Zero–Current Switched Quasi–Resonant Converters," IEEE Transactions on Power Electronics, Vol.4, No.1, pp.136–146, January 1989.

[71] V. Vorperian, "Design and Analysis of dc–dc Resonant Converters," Chapter 2, Final Report to IBM–Owego, Contract No.85–0513–10, Virginia Power Electronics Center, VPI&SU, Blacksburg, Virginia, 1986.

[72] J.J. Baxter and J.W. Andow, "High Temperature Thermal Characteristics of Microelectronic Packages," IEEE Transactions on Parts, Hybrids, and Packaging, Vol.PHP–13, No.4, pp.385–389, 1977.

[73] J.P. Holman, Heat Transfer, McGraw–Hill Book Company, New York, 6th ed., p.409, 1986.

[74] J.C. Eid, "Thermal Modeling with PC Spreadsheets," Proceedings of the Fourth IEEE Semiconductor Thermal and Temperature Measurement Symposium, San Diego, California pp.40–49, February 1989.

APPENDIX A

ZCS–QRC CIRCUIT ANALYSIS

A.1 Circuit Analysis

This appendix provides equations for peak stresses which can be used for the selection of components for the circuit design described in Chapter 2. Figure A.1 shows the reduced schematic of the half–bridge zero–current–switched quasi–resonant converter which has secondary–side resonance and operates in the half–wave mode. Energy from the source, V_s, is switched across the primary of the transformer by switches Q_1 and Q_2. As energy passes across the transformer it charges the inductance of the transformer and then resonates with the secondary–side capacitor, C_r. During resonance, energy is also stored in the filter inductor L_f, and passed to the load. After resonance, energy that is stored in C_r is passed to the load. The energy flow of the circuit can be divided into four stages: that of resonant inductor charging, resonance, resonant capacitor discharging, and freewheeling (when energy only from the filter components, L_f and C_f, supply the load). These four stages are used as the basis for the large–signal analysis.

Simplification of the circuit shown in Fig. A.1, along with certain assumptions, can be made to aid the analysis. Only the secondary circuit is analyzed with a secondary–side voltage source, V, instead of V_s; i.e.,

$$V = V_s/2N$$

where N is the transformer turns ratio. The output filter is approximated to the first order by a constant current source of value I_o. The MOSFET switches and the diodes are assumed ideal. The reduced circuit used for the analysis is shown in Fig. A.2. Individual branch currents will be set to zero to change the active topology during the analysis.

The circuit will be analyzed for each stage of energy flow. Assume that, prior to the first stage being activated, the circuit is freewheeling; i.e., no switch is on and output current I_o is flowing only through diode Dfw.

Inductor Charging Stage: $t_o \leq t \leq t_1$.

Initially, switch Q2 is closed and switch Q1 is open (Fig. A.1), hence

$i_1(t_o) = 0$ $\qquad$ $i_d(t_o) = I_o$

$i_2(t) = 0$ $\qquad$ $v_c(t) = 0$

$i_c(t) = 0$

Summing currents in active branches gives

$$i_1(t) + i_d(t) + I_o = 0$$

$$\frac{1}{L_r} \int (v_c(t) - V)\, dt + i_1(t_o) + I_o = 0 \qquad (A.1)$$

$$-\frac{V}{L_r}(t - t_o) + I_o = i_d(t) \qquad (A.2)$$

where L_r is the secondary–side leakage inductance of the transformer.

This stage ends when all source current flows directly through the load and the diode current decreases to zero, i.e., $i_d(t_1) = 0$; then, from (A.2),

$$t_1 - t_o = I_o L_r / V \tag{A.3}$$

Resonant Stage: $t_1 \leq t \leq t_2$

Initially, switch Q_2 is closed and Q_1 open (Fig. A.1).

$$i_1(t_1) = -I_0 \qquad i_d(t) = 0$$

$$i_2(t) = 0 \qquad v_c(t_1) = 0$$

$$i_c(t_1) = 0$$

Summing currents in active branches gives

$$i_1(t) + i_c(t) + I_o = 0 \tag{A.4}$$

$$\frac{1}{L_r}\int (v_c(t) - V)dt + i_1(t_1) + C_r\frac{dv_c(t)}{dt} + I_o = 0 \tag{A.5}$$

$$v_c(t) = V\,\{1 - \cos[\omega_o(t-t_1)]\} \tag{A.6}$$

$$i_c(t) = \omega_o C_r V \sin[\omega_o(t-t_1)] \tag{A.7}$$

$$i_1(t) = \frac{-V}{\omega_o L_r} \sin[\omega_o(t-t_1)] - I_o \qquad \text{(A.8)}$$

where $\omega_o = 1/\sqrt{L_r\ C_r}$

This stage ends when secondary current through the rectifiers reverses direction, i.e. $i_1(t_2)=0$; then, from (A.8),

$$t_2-t_1 = \frac{1}{\omega_o} \arcsin\left(-\frac{I_o \omega_o L_r}{V}\right) \qquad \text{(A.9)}$$

At the end of this stage the switches are turned off at zero current.

Capacitor Discharging Stage: $t_2 \leq t \leq t_3$

Initially, no switches are conducting.

$i_1(t) = 0$	$i_d(t) = 0$
$i_2(t) = 0$	$v_c(t_2) = V - (V^2 - I_o^2 Z_n^2)^{1/2}$
$i_c(t_2) = -I_o$	where $Z_n = (L_r/C_r)^{1/2}$

Summing currents in active branches gives

$$i_c(t) + I_o = 0 \qquad \text{(A.10)}$$

$$v_c(t) = \frac{1}{C_r} \int i_c(t)\, dt + v_c(t_2)$$

$$= -\frac{I_o}{C_r}(t-t_2) + [V - \sqrt{V^2 - (I_o Z_n)^2}] \qquad \text{(A.11)}$$

where $$Z_n = (L_r/C_r)^{1/2} \qquad \text{(A.12)}$$

This stage ends when the capacitor voltage reverses and the diode begins conducting, i.e., $v_c(t_3) \leq 0$; then, from (A.11)

$$t_3 - t_2 = \frac{C_r}{I_o} [V - \sqrt{V^2 - (I_o Z_n)^2}] \qquad \text{(A.13)}$$

Freewheeling Stage: $t_3 < t \leq t_4 \equiv t_o$

Initially, no switches are conducting.

$i_1(t) = 0$ $\qquad$ $i_d(t_3) = -I_o$

$i_2(t) = 0$ $\qquad$ $v_c(t) = 0$

$i_c(t) = 0$

Summing currents in active branches gives

$$i_d(t) = -I_o \qquad \text{(A.14)}$$

This stage ends either when a switch, Q_1 or Q_2, is closed or when the output current becomes discontinous, in which case (A.14) is no longer valid.

A.2 Primary–Circuit Analysis

In the previous analysis an ideal transformer was assumed and effects due to magnetizing inductance were not included. Given below is an analysis of the primary–circuit currents which flow through switches Q_1 and Q_2 when magnetizing inductance effects are included.

Shown in Fig. A.3 is the primary–circuit schematic that will be used for the large signal analysis. Evaluation of the four stages of energy flow as described in the previous section shows that current flows through the switches only during the inductor charging and resonant stages. Therefore, the analysis will develop an equation for the switch current, $i_s(t)$, during theinterval $t_o \leq t \leq t_2$. It is assumed that the change in the midpoint voltage between C_1 and C_2 is zero and the midpoint voltage is one half the supply voltage.

Inductor Charging Stage: $t_o \leq t \leq t_1$

Initially, switch Q_1 is closed and Dfw (Fig. A.1) is conducting. The equivalent circuit of the active branches is shown in Fig. A.3b.

Since $L_m >> L_r N^2$ (where L_m is the magnetizing inductance of the transformer) for the off–line circuit that is to be designed in Chapter 5, then

$$i_s(t) = V_s(t-t_o)/2L_rN^2 \qquad (A.15)$$

For this monotonic function the maximum current occurs at time t_1. Using (A.3) the maximum current is

$$i_s^{max} = I_o/N \qquad (A.16)$$

Resonant Stage: $t_1 \leq t \leq t_2$

Initially, switch Q_1 is still closed but Dfw is not conducting, and L_r and C_r are resonating. Using (A.7), the switch current is

$$i_s(t) = i_m(t) + i_r(t) =$$

$$\frac{V_s\ (t-t_1)}{2L_m} + \frac{V_s}{2Z_nN^2}\sin[\omega_o(t-t_1)] + \frac{I_o}{N} \qquad (A.17)$$

where $$Z_n = \sqrt{L_r/C_r}$$

The maximum current for this stage occurs at $t = t_1 + 1.58/\omega_o$ for the ZCS–QRC described in Chapter 5. Therefore,

$$I_s^{max} = V_s^{max}\left(\frac{4}{5\omega_oL_m} + \frac{1}{2Z_nN^2} + \frac{I_o^{max}}{NV_s^{max}}\right) \qquad (A.18)$$

The two right most terms within the bracket represent the current passed through the switch and transformer. The remaining term represents the current through the switch and magnetizing reactance. The magnitude of this current is less than 10% of the total switch current at full load for the ZCS–QRC considered here. Therefore, it does not appreciably affect the current rating of the switch. However, it does affect the minimum level of switch current during light–load conditions.

The minimum switch voltage is equal to the maximum input source voltage.

A.3 Critical Design Parameters

The maximum currents and voltages within the circuit are used to determine component values. The equations for the maximum currents and voltages are derived from the preceding section and the input data information listed in Section 2.2.

From (A.7), the maximum resonant–capacitor current is

$$I_{C_r}^{max} = \frac{V_S^{max}}{2N \ Z_n} \tag{A.19}$$

and the maximum capacitor voltage from (A.6) (with an argument of π rad/sec.) is

$$V_{c_r}^{max} = V_s^{max}/N \tag{A.20}$$

From (A.4) and (A.8), the maximum rectifier current is

$$I_{rec}^{max} = I_{c_r}^{max} + I_o + I_f^s/2 \tag{A.21}$$

where I_f^s is maximum filter–inductor ripple current. The maximum average current is

$$I_{rec}^{max} = \frac{1}{T_o}\int_0^{\tau} \left(\frac{V_s^{max}}{2NZ_n}\sin(\omega_o t) + \frac{V_o}{R_L^{min}} + \frac{I_f^s}{2}\right)dt$$

$$= \frac{F_s}{2F_r}\left(\frac{V_s^{max}}{\pi NZn} + \frac{V_o}{R_L^{min}} + \frac{I_f^s}{2}\right) \tag{A.22}$$

where $T_o = 1/F_s$, $\tau = 1/4F_r$. The $I_f^s/2$ will be of negligible value for the ZCS–QRC developed here.

The maximum reverse voltage is

$$V_{rec}^{max} = \frac{3V_s^{max}}{2N} \tag{A.23}$$

The current through the freewheeling diode is not affected by the magnetizing inductance of the transformer. The diode is conservatively rated to have capacity for long off times in switching, such as during shut down. The maximum rated current in the freewheeling diode is

$$I_{dfw}^{max} = \frac{V^{max}}{R_L^{min}} \tag{A.24}$$

The maximum reverse voltage is the same as the maximum capacitor voltage, see (A.20). These equations are used in Chapter 5 to determine conductor widths and component spacings.

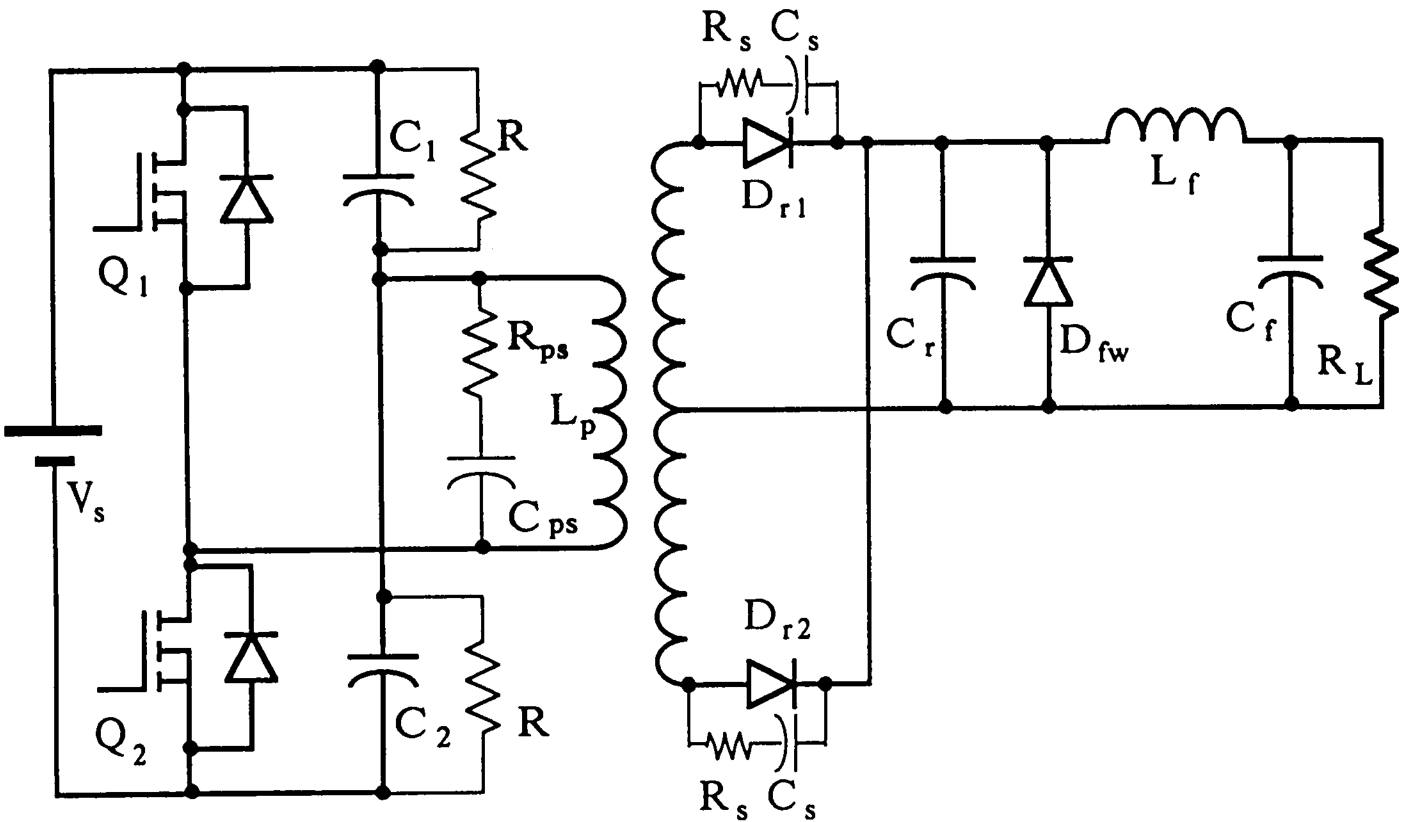

Fig. A.1 Schematic of HB, HW, ZCS–QRC.

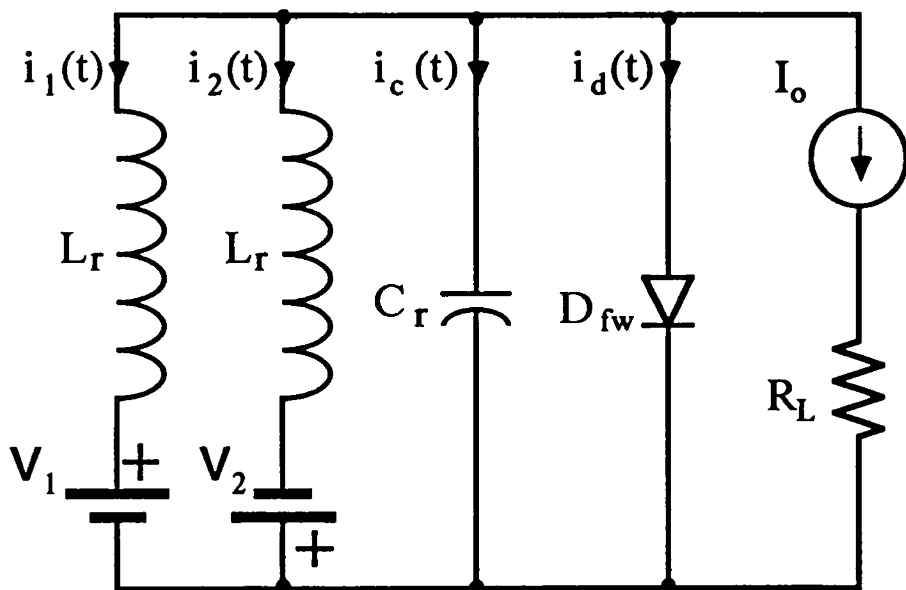

Fig. A.2 Reduced schematic for ZCS–QRC analysis.

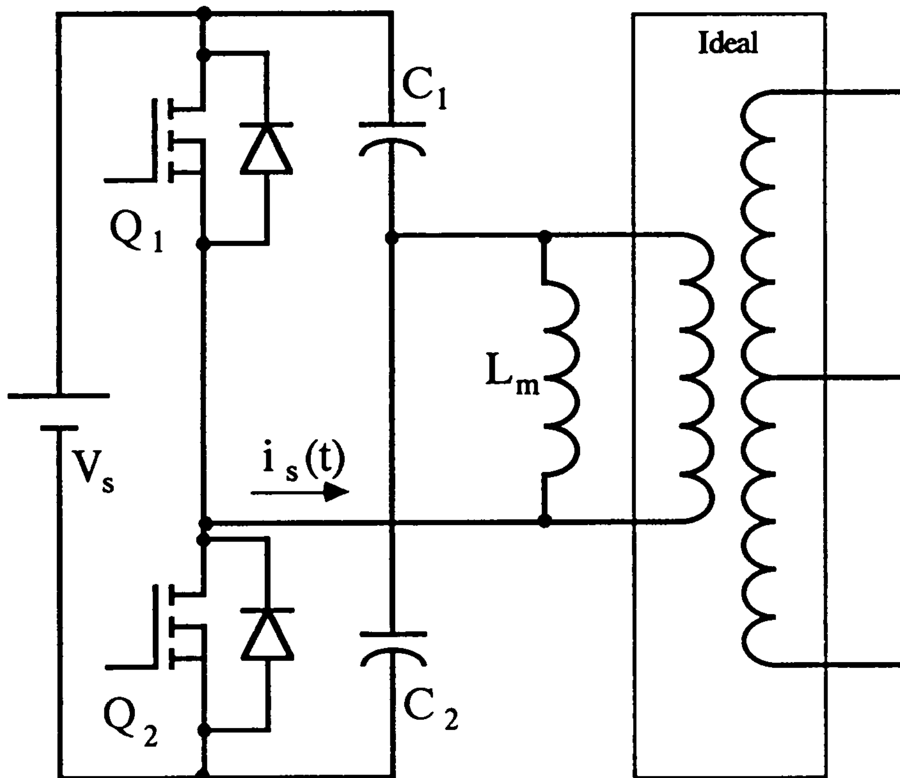

Fig. A.3a Primary–circuit schematic of half–bridge converter.

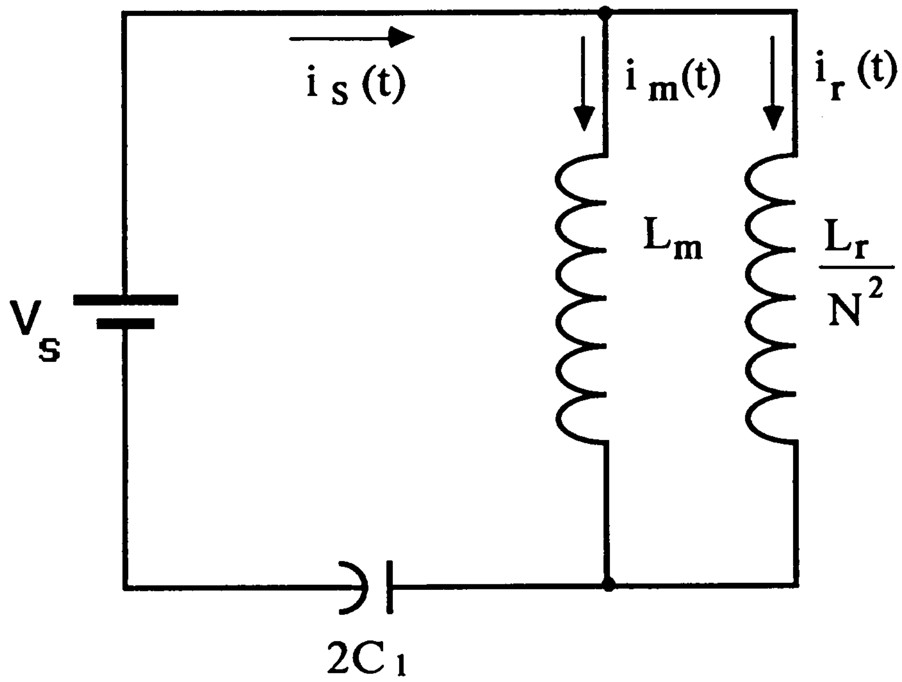

Fig. A.3b Equivalent circuit for inductor charging stage.

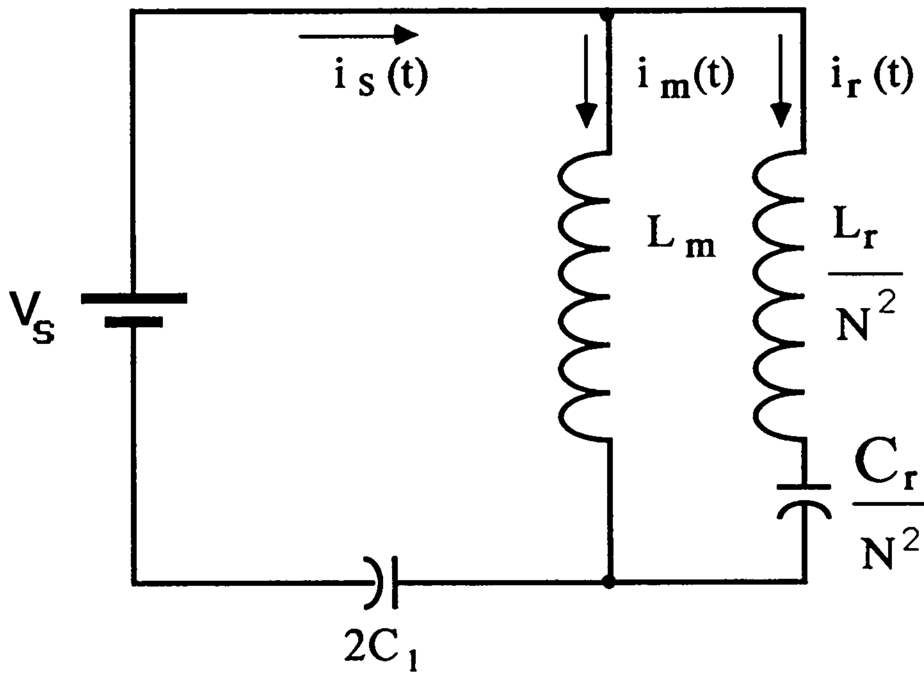

Fig. A.3c Equivalent circuit for resonant stage.

APPENDIX B

DETERMINATION OF CONDUCTOR THICKNESS AND WIDTH FOR POWER HYBRID CIRCUITS

B.1 Introduction

Any interconnecting conductor in a nonsuperconductive circuit has a finite internal impedance, i.e. a finite resistance and reactance within the conductor. In signal level circuits the impedance is usually negligible. However, in power circuits, particularly thick–film power hybrid circuits, the impedance is of considerable concern. For instance, in circuits where hybridization is used to reduce circuit size, conductors with relatively large cross sections are not readily attainable. Consequently, the use of narrow conductors may double or quadruple the impedance found in conventional circuits.

The impedance of a conductor can also increase with frequency since the current distribution within the conductor becomes nonuniform and the effective thickness of the electrical path is reduced as shown in Fig. B.2. This may cause problems for hybridized switchmode power supplies (SMPS) that operate above 1 MHz. Other factors can affect the impedance. If conductors are in close proximity, the internal current distribution may concentrate towards the edge of the conductor and further limit its effective width. Also, if the conductor has sharp corners, e.g., in a conductor with a rectangular cross section, fringing effects change the distribution of current.

In this appendix design rules are developed for selecting the thickness and width of a flat strip conductor as used in a thick–film hybrid circuit or printed circuit board. Edge and proximity effects from adjacent conductors are considered and will be found to be negligible for power circuits.

B.2 Current Distribution

Figure B.1 shows a rectangular strip conductor of length, ℓ; width, w; and thickness, t. This conductor might be printed on a hybrid substrate or etched into a printed circuit board. If edge effects are negligible (which will be shown to be true), current crowding in the conductor corners is negligible, i.e. w >> t. Also, assume a current is flowing in the z direction. The wave propagation for this conductor is described by Maxwell's equations for a lossy region.

$$\nabla \times \mathrm{E} = -j\omega\mu\, H \tag{B.1}$$

$$\nabla \times H = +j\omega\epsilon\, E + \sigma E \tag{B.2}$$

where

ω is the frequency of the current [rad/s]

μ is the permeability of the medium [H/m]

ϵ is the permitivity of the medium [F/m]

σ is the conductivity of the medium [S/m].

The right side of (B.2) contains the terms for the displacement current and conduction current, respectively. Since this development is for a "good conductor", $\sigma/\omega\epsilon >> 1$, then (B.2) need only contain the conduction current term, i.e., $+\sigma E$.

In Fig. B.1, the current density, J, (= σE), is assumed to be a vector quantity with unit direction in z and having magnitude and phase variation in the y direction. Substituting J into (B.1) and (B.2) and combining gives

$$\frac{d^2 J_z(y)}{dy^2} = -j\omega\mu\sigma J_z(y) \qquad \text{(B.3)}$$

Using the definition for skin depth [b.1], $\delta = (\pi f\mu\sigma)^{-1/2}$, the solution of (B.3) is

$$J_z(y) = J_1 e^{(1+j)y/\delta} + J_2 e^{-(1+j)y/\delta} \qquad \text{(B.4)}$$

For the strip conductor in Fig. B.1 the current is symmetric about the y = 0 plane. Therefore, $J_z(y) = J_z(-y)$ implying $J_1 = J_2$. Setting y = 0 and, solving for the integration constants,

$$J_z(y) = 1/2\ J_z(0) \cosh(1 + j)y/\delta \qquad \text{(B.5)}$$

The current distribution in the conductor is

$$J_z(y) = J_z^{surf}\left[\frac{\cosh(1 + j)y/\delta}{\cosh(1 + j)v/2}\right] \tag{B.6}$$

where $v = t/\delta$, the ratio of total thickness to skin depth, and $J_z^{surf} = J_z(t/2)$ which is the current density at the surface.

To better view the distribution of this complex current density, the magnitude of the current normalized by the surface value is computed as

$$|J_z^{norm}| = |J_z(y)/J_z^{surf}| = \left[\frac{\cosh 2y/\delta + \cos 2y/\delta}{\cosh v + \cos v}\right] \tag{B.7}$$

and is plotted in Fig. B.2. The vertical axis gives the magnitude of the current within the conductor relative to the surface value. (Note: $J_n = J_z^{norm}$. The horizontal axis gives the position in the conductor relative to the skin depth. The family of curves represent different conductor thicknesses relative to the skin depth. Hence, for a conductor two skin depths thick (i.e. $v = 2$), the current at the center of the conductor (where $y/\delta = 0$) is approximately 80% of the surface value but is equal to the surface value when at the surface where $y/\delta = 1$. As can be seen, the current density can be appreciable at the center of the conductor ($y \to 0$).

Edge Effects

The above development assumes no transverse current distribution in the x direction and no current crowding at the edges of the conductor. King [b.2]

shows there is some transverse distribution due to skin effect and, for a perfect conductor, ($\delta = o$) 20% of the current flows in the outer 5% of the conductor's width (2.5% of each edge). He also points out that, for a conductor with finite conductivity, the skin effect is diminished and a much smaller percentage of current flows in the outer most edges. Therefore, neglecting a transverse distribution of current will introduce little error in the following development of the conductor impedance. However, because of symmetry about the $x = w/2$ plane, the development for the optimum conductor thickness will remain exact and the selection of conductor width, which is done empirically, will not be affected by neglecting the transverse distribution.

B.3 Conductor Impedance

The total current per unit width [b.3] is

$$\frac{I_z}{w} = \int_{-t/2}^{t/2} J_z(y)dy = \frac{2 J_z^{surf} \delta}{(1 + j)} \tanh \frac{(1 + j)v}{2} \qquad \text{(B.8)}$$

The voltage drop per unit length is

$$V_z/\ell = J_z^{surf}/\sigma \qquad \text{(B.9)}$$

Hence, the internal impedance of the conductor can be represented as

$$Z = \frac{V_z}{I_z} = R + jX \tag{B.10}$$

where

$$R = \frac{\zeta}{2\sigma\delta} \frac{\sinh v + \sin v}{\cosh v - \cos v} \tag{B.10a}$$

$$X = \frac{\zeta}{2\sigma\delta} \frac{\sinh v - \sin v}{\cosh v - \cos v} \tag{B.10b}$$

and

$$\zeta = \ell / w \tag{B.10c}$$

which is the number of squares of area.

In power hybrid circuits the resistance is of greatest concern since higher currents can cause appreciable power loss in highly resistive conductors. For instance, in SMPSs with outputs of 5 V and 100 W, currents of 20 A can flow through the interconnects of rectifiers and filters at conversion frequencies in the low megahertz range.

Equation (B.10a) gives the total resistance of the conductor at any frequency.

B.7 REFERENCES

[b.1] R.G. Brown, R.A. Sharpe, and W.L. Lewis, Lines, Waves and Antennas, the Ronald Press Company, New York, p. 184, 1961.

[b.2] R.W.P. King and C.W. Harrison, Jr., "Current Distribution and Impedance per Unit Length of a Thin Strip", IEEE Transactions on Antennas and Propagation, Vol. AP–14, p. 252, March 1966.

[b.3] P. Hammond, Applied Electromagnetism, Pergamon Press Ltd., Oxford, p. 210, 1971.

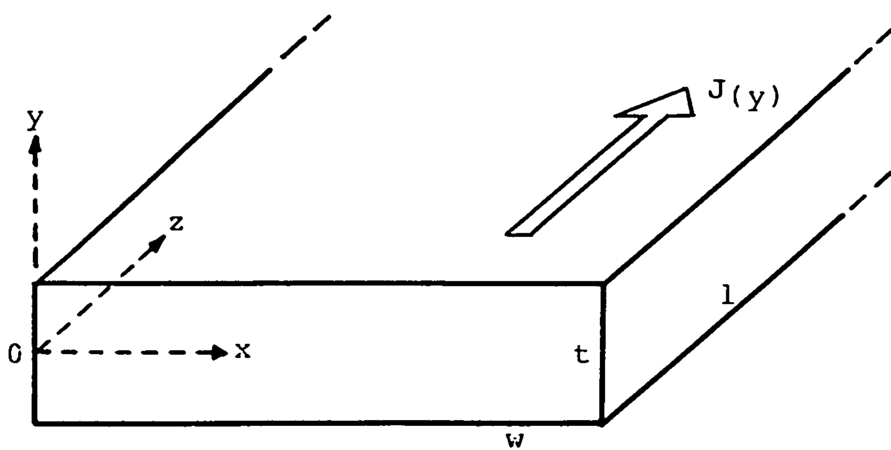

Fig. B.1 Strip conductor

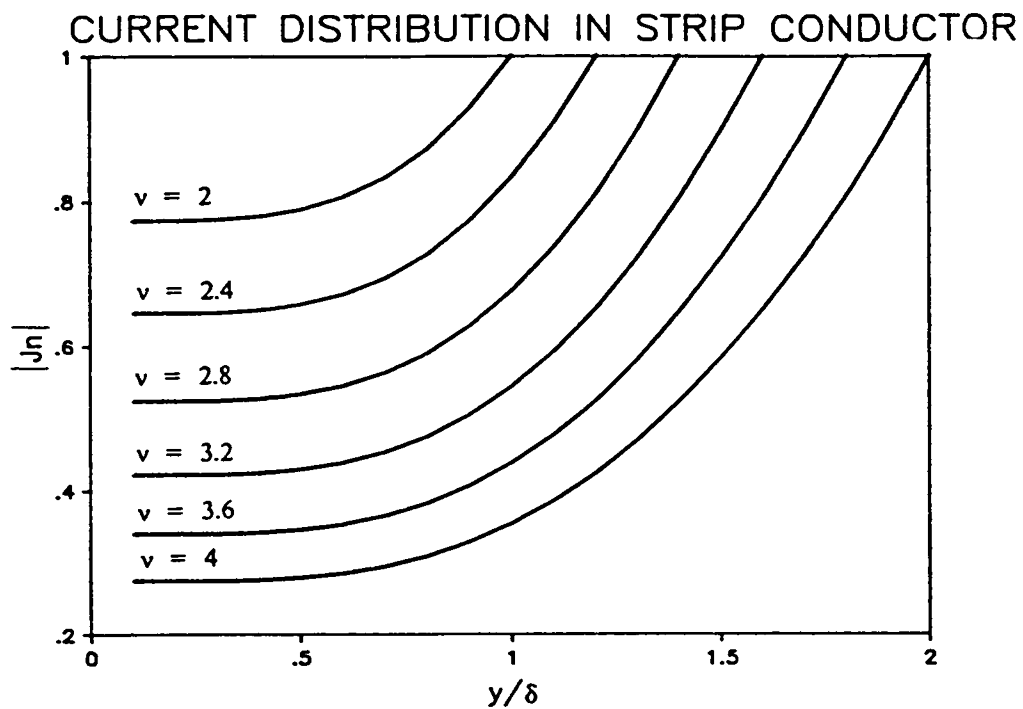

Fig. B.2 Current distribution in strip conductor

The vita has been removed from the scanned document